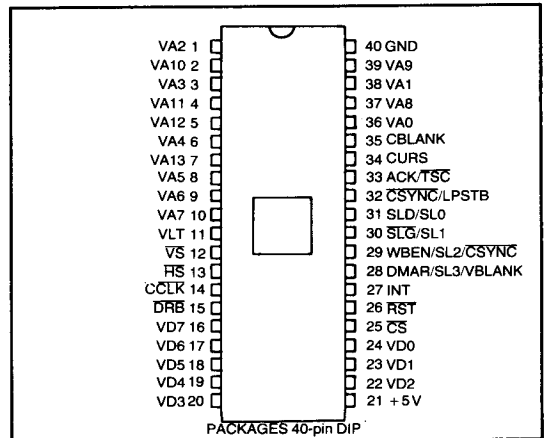


CRT Video Processor and Controller
VPAC™

FEATURES

- Fully Programmable Display Format
 - Characters per Data Row (8-240)
 - Data Rows per Frame (2-256)
 - Raster Scans per Data Row (1-32)
- Programmable Monitor Sync Format
 - Raster Scans/Frame (4-2048)
 - Front Porch—Horizontal (Negative or Positive)
 - Vertical
 - Sync Width—Horizontal (1-128 Character Times)
 - Vertical (2-256 Scan Lines)
 - Back Porch—Horizontal
 - Vertical
- Direct Outputs to CRT Monitor
 - Horizontal Sync
 - Vertical Sync
 - Composite Sync
 - Composite Blanking
 - Cursor Coincidence
- Binary Addressing of Video Memory
 - Row-Table Driven or Sequential Video Addressing Modes
 - Programmable Status Row Position and Address Registers
 - Bidirectional Partial or Full Page Smooth Scroll
 - Attribute Assemble Mode
 - Double Height Data Row Mode
 - Double Width Data Row Mode
 - Programmable DMA Burst Mode
 - Configurable with a Variety of Memory Contention Arrangements
 - Light Pen Register
 - Cursor Horizontal and Vertical Position Registers
 - Maskable Processor Interrupt Line
 - Internal Status Register
 - Three-state Video Memory Address Bus
 - Partial or Full Page Blank Capability
 - Two Interlace Modes: Enhanced Video and Alternate Scan Line

PIN CONFIGURATION



- Ability to Delay Cursor and Blanking with respect to Active Video
- Programmable for Horizontal Split Screen Applications
- Graphics Compatible
- Ability to Externally Sync each Raster Line, each Field
- Single +5 Volt Power Supply
- TTL Compatible on All Inputs and Outputs
- VT-100 Compatible
- RS-170 Interlaced Composite Sync Available

GENERAL DESCRIPTION

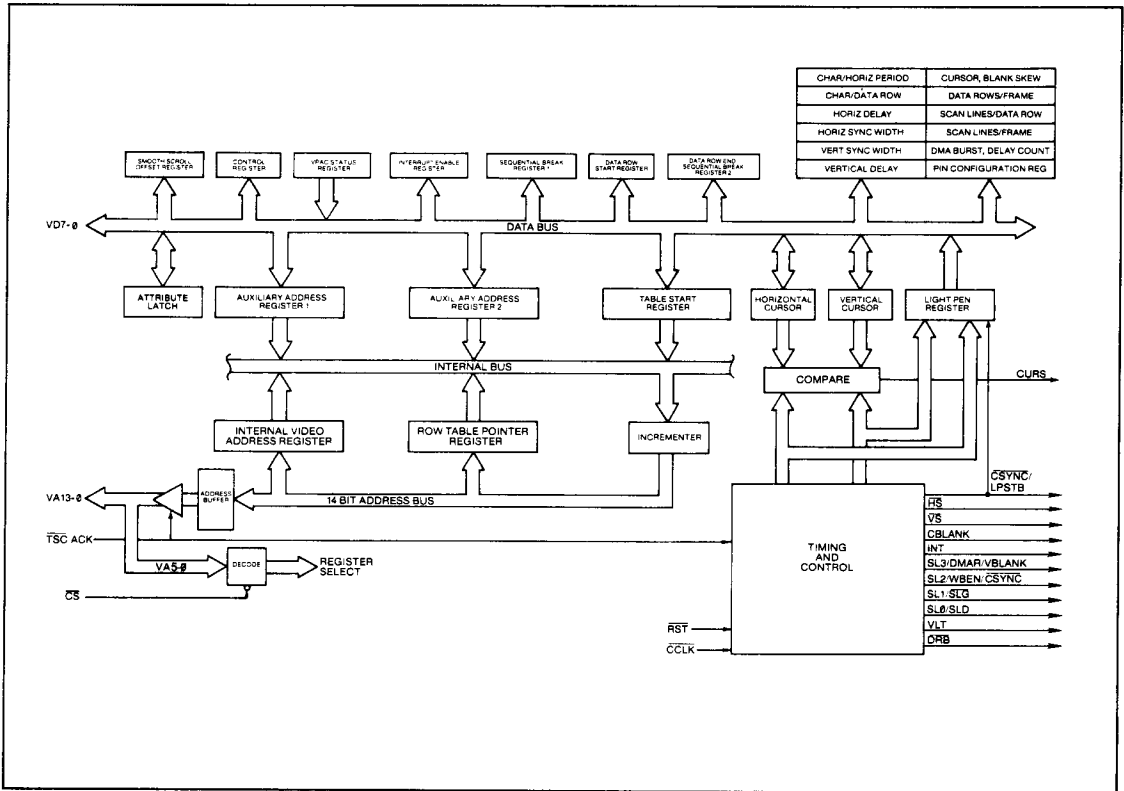
The CRT 9007 VPAC™ is a next generation video processor/controller—an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the VPAC™ provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode, each row in the video display is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The VPAC™ works with a variety of memory contention schemes including operation with a Single Row Buffer such as the CRT 9006, a Double Row Buffer such as the CRT 9212, or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessible internal registers provide such features as light pen, interrupt enabling, cursor addressing, and VPAC™ status. Ten of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 10 registers contain the "vital screen parameters".



DESCRIPTION OF PIN FUNCTIONS

PROCESSOR INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
7, 5, 4, 2, 39, 37, 10, 9, 8, 6, 3, 1, 38, 36	Video Address 13-0	VA13-VA0	<p>These 14 signals are the binary address presented to the video memory by the CRT 9007. The function depends on the particular CRT 9007 mode of operation. VA13-6 are outputs only. VA5-0 are bidirectional.</p> <ul style="list-style-type: none"> —Double Row Buffer Configuration: VA13-0 are active outputs for the DMA operations and are in their high impedance state at all other times. —Single Row Buffer Configuration: VA13-0 are active outputs during the first scan line of each data row and are in their high impedance state at all other times. —Repetitive Memory Addressing Configuration: VA13-0 are active outputs at all times except during horizontal and vertical retrace at which time they are in their high impedance state. <p>If row table addressing is used for either single row buffer or repetitive memory addressing modes, VA13-0 are active outputs during the horizontal retrace at each data row boundary to allow the CRT 9007 to retrieve the row table address. For processor read/write operations VA5-0 are inputs that select the appropriate internal register.</p>
16, 17, 18, 19, 20, 22, 23, 24	Video Data 7-0	VD7-VD0	<p>Bidirectional video data bus: during processor Read/write operations data is transferred via VD7-VD0 when chip strobe (CS) is active. These lines are in their high impedance state when CS is inactive. During CRT 9007 DMA operations, data from video memory is input via VD7-VD0 when a new row table address is being retrieved or when the attribute latch is being updated in the attribute assemble mode. VD7-VD0 are outputs when the external row buffer is updated with a new attribute in the attribute assemble mode.</p>
25	Chip strobe	CS	<p>Input: this signal when active low, allows the processor to read or write internal CRT 9007 registers. When reading from an internal CRT 9007 register, the chip strobe (CS) enables the output drivers. When writing to an internal CRT 9007 register, the trailing edge of this signal latches the incoming data. Figure 2 shows all processor read/write timing.</p>
26	Reset	RST	<p>Input: this active low signal puts the CRT 9007 into a known, inactive state and insures that the horizontal sync (HS) output is inactive. Activating this input has the same effect as a RESET command. After initialization, a START command causes normal CRT 9007 operation. See processor addressable registers section, Register 16 for the reset state definition.</p>
27	Interrupt	INT	<p>Output: an interrupt to the processor from the CRT 9007 occurs when this signal is active high. The interrupt returns to its inactive low state when the status register is read.</p>

DESCRIPTION OF PIN FUNCTIONS CONT'D

CRT INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
11	Visible Line Time	VLT	Output; this signal is active high during all visible scan lines and during the horizontal trace times at vertical retrace. This signal can be used to gate the character clock (CCLK) when supplying data to a character generator from a single or double row buffer.
12	Vertical Sync	VS	Open drain output; this signal determines the vertical position of displayed text by initiating a vertical retrace. Its position and pulse width are user programmable. The open drain allows the vertical frame rate to be synchronized to the line frequency when using monitors with DC coupled vertical amplifiers. If the VS output is pulled active low externally before the CRT 9007 itself initiates a vertical sync, the CRT 9007 will start its own vertical sync at the next leading edge of horizontal sync (HS).
13	Horizontal Sync	HS	Open drain output; this signal determines the horizontal position of displayed text by initiating a horizontal retrace. Its position and pulse width are user programmable. During hardware and software reset, this signal is inactive high. The open drain allows the horizontal scan rate to be synchronized to an external source. If the HS output is pulled low externally before the CRT 9007 itself initiates a horizontal sync, the CRT 9007 will start its own horizontal sync on the next character clock (CCLK).
14	Character Clock	CCLK	Input; this signal defines the character rate of the screen and is used by the CRT 9007 for all internal timing. A minimum high voltage of 4.3V must be maintained for proper chip operation.
15	Data Row Boundary	DRB	Output; this signal is active low for one full scan line (from VLT trailing edge to VLT trailing edge) at the top scan line of each new data row. This signal can be used to swap buffers in the double row buffer mode. It indicates the particular horizontal retrace time that the CRT 9007 outputs addresses (VA13-VA0) for single row buffer operation. There will always be one extra DRB signal which will become active during the first scan line of the vertical retrace interval.
34	Cursor	CURS	Output; this signal marks the cursor position on the screen as specified by the horizontal and vertical cursor registers. The signal is active for one character time at the particular character position for all scan lines within the data row. For double height or width characters, this signal is active for 2 consecutive CCLK's in every scan line within the data row. For double height characters, this signal can be programmed to be active at the proper position for 2 consecutive data rows. CURS is also used to signal either a double height or double width data row by becoming active during the horizontal retrace (CBLANK active) prior to a double height or double width scan line. The time of activation and deactivation is a function of the addressing mode, buffer configuration and the scan line number. See section of Double height/width for details.
35	Composite Blank	CBLANK	Output. This signal when active high, indicates that a retrace (either horizontal or vertical) will be performed. The signal remains active for the entire retrace interval as programmed. It is used to blank the video to a CRT.

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USER SELECTABLE PINS: (see Tables 4 and 5)

PIN NO.	NAME	SYMBOL	FUNCTION
28, 29, 30, 31	Scan Line 3-Scan Line 0	SL3-SL0	Output; these 4 signals are the direct scan line counter outputs, in binary form, that indicate to the character generator the current scan line. These signals continue to be updated during the vertical retrace interval. SL3 and SL0 are the most and least significant bits respectively.
28	Direct Memory Access Request	DMAR	Output; this signal is the DMA request issued by the CRT 9007. It will only become active if the acknowledge (ACK) input is inactive. It remains active high throughout the entire DMA operation.
28	Vertical Blank	VBLANK	Output; this signal is active high only during the vertical retrace period.
29	Write Buffer Enable	WBEN	Output; this active high signal is used to gate the clock feeding the write buffer in a double row buffer configuration.
29 or 32	Composite Sync	CSYNC	Output; this signal provides a true RS-170 composite sync waveform with equalization pulses and vertical serrations in both interlace and noninterlace formats. Figure 3 illustrates the CSYNC output in both interlaced and noninterlaced formats.
30	Scan Line Gate	SLG	Output; this active low signal is used as a clock gate. It captures the correct 5 or 6 CCLK's and, in conjunction with SLD (pin 31), allows scan line information to be loaded serially into an external shift register.
31	Scan Line Data	SLD	Output; this signal allows one to load an external shift register with the current scan line count. The count is presented least significant to most significant bit during the 5 or 6 CCLK's framed by SLG. With this form of scan line representation, it is possible to define up to 32 scan lines per data row. The external shift register must be at least 5 bits in length. Even though 6 shifts can occur one should only use the 5 last bits shifted to define the scan line count. The extra shift occurs in interlace or double height character mode to allow the scan line count to be adjusted to its proper value. Figures 4 and 5 illustrate the serial scan line timing.
32	Light Pen Strobe	LPSTB	Input; this signal strobes the current row/column position into the light pen register at its positive transition.
33	Acknowledge	ACK	Input; this active high signal acknowledges a DMA request. It indicates that the processor bus has entered its high impedance state and the CRT 9007 may access video memory. It is not recommended to deactivate this signal during a CRT 9007 DMA cycle because the CRT 9007 will not shut down in a predictable amount of time.
33	Three State Control	TSC	Input; this signal, when active low, places VA13-VA0 in their high impedance state.

OPERATION MODES

Single Row Buffer Operation

The CRT 9007 configured with a CRT 9006 Single Row Buffer is shown in figure 6. The use of the CRT 9006 Single Row Buffer requires that the buffer be loaded at the video painting rate during the top scan line of each data row. However, after the CRT 9006 is loaded, the CRT 9007 address lines enter their high impedance state for the remaining N-1 scan lines of the data row, thereby permitting full proces-

sor access to memory during these scan lines. The percentage of total memory cycles available to the processor is approximately $[(N-1)/N] \times 100$ where N is the total number of scan lines per data row. For a typical system with 12 scan lines per data row this percentage is 92%. Figure 7 illustrates typical timing for the CRT 9007 used with the CRT 9006 Single Row Buffer.

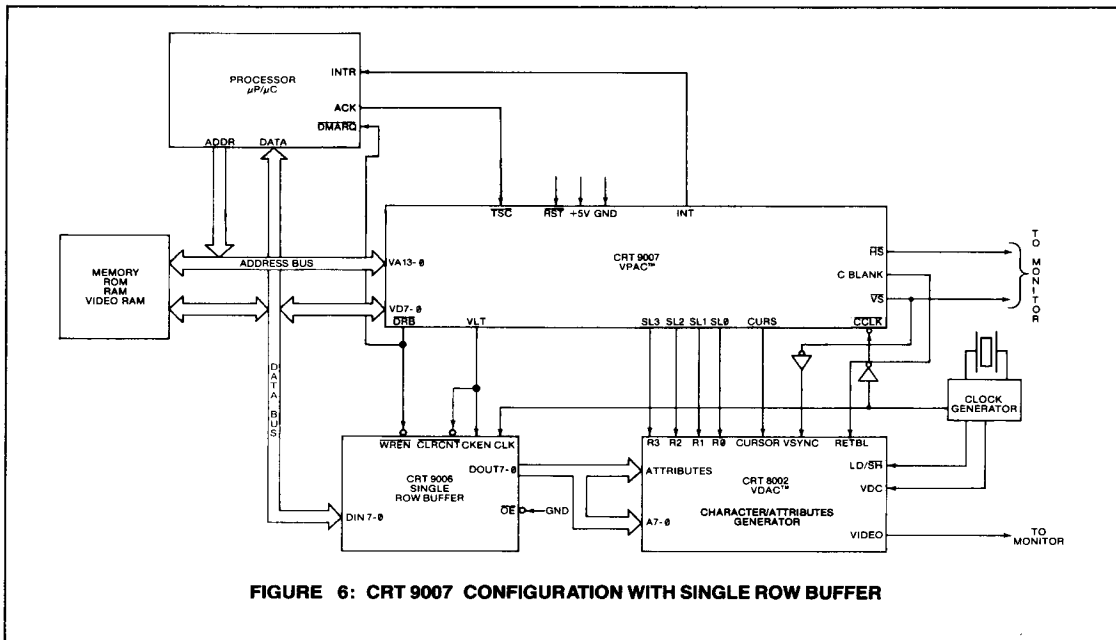


FIGURE 6: CRT 9007 CONFIGURATION WITH SINGLE ROW BUFFER

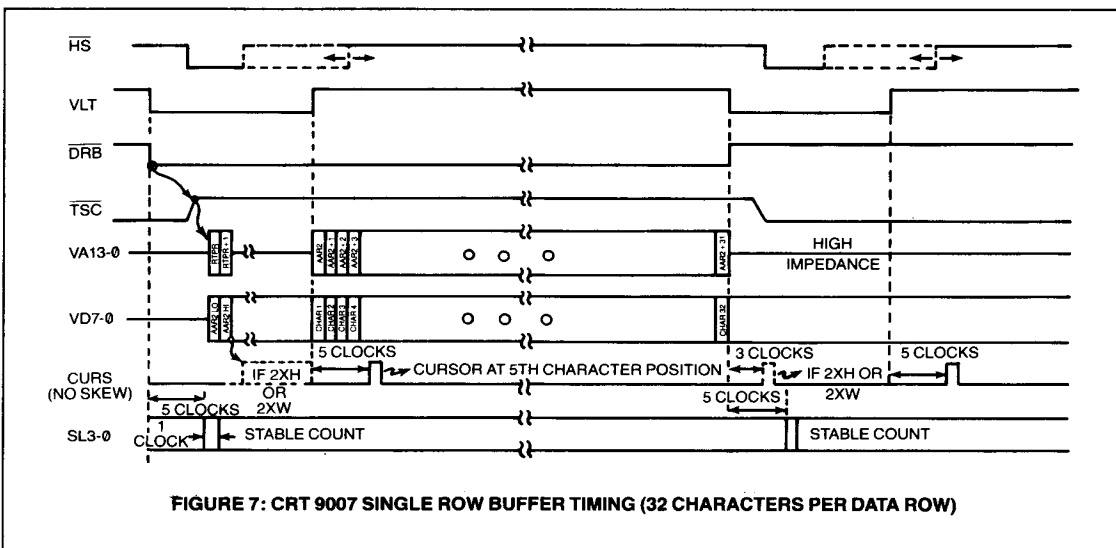


FIGURE 7: CRT 9007 SINGLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

Double Row Buffer Operation

Figure 8 shows the CRT 9007 used in conjunction with a CRT 9212 Double Row Buffer. The Double Row Buffer has a read buffer which is read at the painting rate of the CRT during each scan line in the data row. While the read buffer is being read and supplying data to the character generator for the current displayed data row, the write buffer is being loaded with the next data row to be displayed. This arrangement allows for relaxed write timing to the write buffer as it may be filled in the time it takes for N scan lines on the CRT to be painted where N is the number of scan lines per data row. Used in this configuration, the CRT 9007 takes advantage of the relaxed write buffer timing by stealing memory cycles from the processor to fill the write buffer (Direct memory access operation). The CRT 9007 sends the DMAR (DMA request) signal, awaits an ACK (acknowledge) signal and then drives out on VA13-VA0 the address at which the next video data resides. The CRT 9007 then activates the WBEN (write buffer enable) signal to write the data into the buffer. If for example there are 80 characters per data row, the CRT 9007 performs 80 DMA operations. The user has the ability to program the number of DMA cycles performed during each DMAR-ACK sequence, as well as

the delay between each DMAR-ACK sequence, via the DMA CONTROL REGISTER (RA). If 8 DMA operations are performed for each ACK received, 10 such DMAR-ACK sequences must be performed to completely fill the write buffer. The programmed delay allows the user to evenly distribute the DMA operations so as not to hold up the processor for an excessive length of time. This feature also permits other DMA devices to be used and allows the processor to respond to real time events. In addition, the user has the ability to disable the CRT 9007 DMA mechanism. Figure 9 illustrates typical timing for the CRT 9007 used with the CRT 9212 Double Row Buffer.

Since the CRT 9212 Double Row Buffer has separate inputs for read and write clocks (RCLK, WCLK), it is possible to display proportional character widths (variable number of dots per character) by reading out the buffer at a character clock rate determined by the particular character. The writing of the buffer can be clocked from a different and constant character clock. Figure 10 illustrates the CRT 9007 used with two double row buffers and a CRT 9021 Video Attributes Controller chip to provide proportional character display.

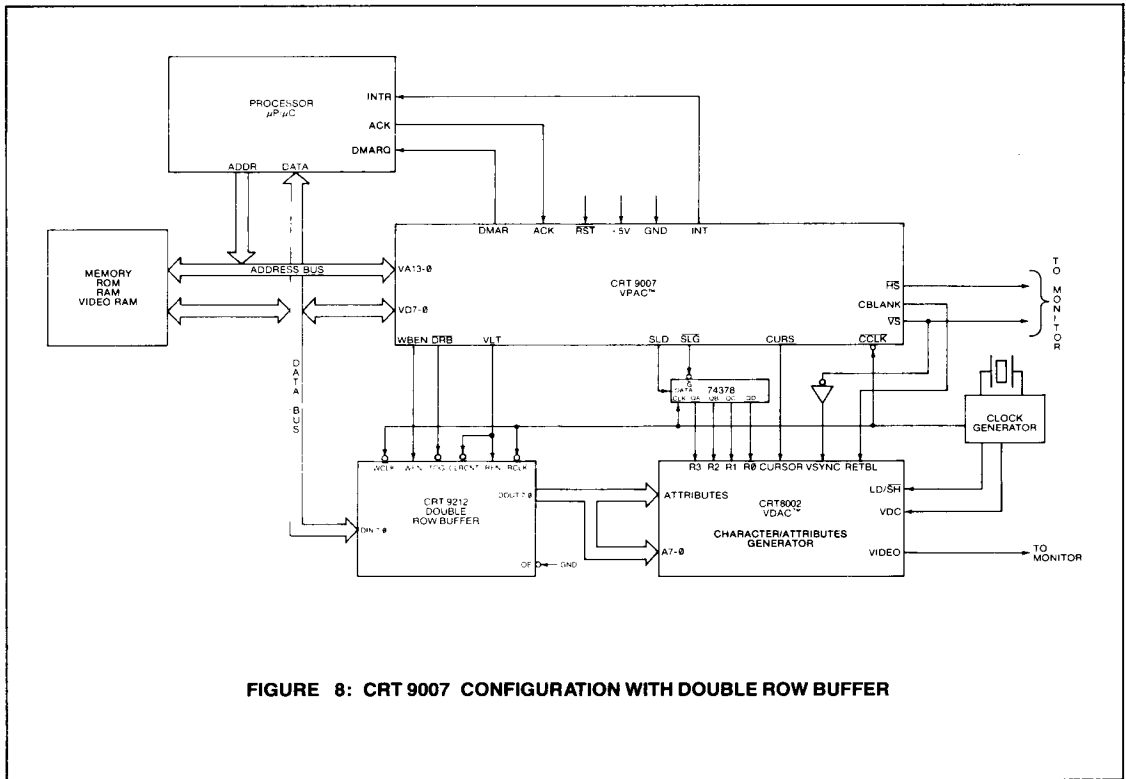


FIGURE 8: CRT 9007 CONFIGURATION WITH DOUBLE ROW BUFFER

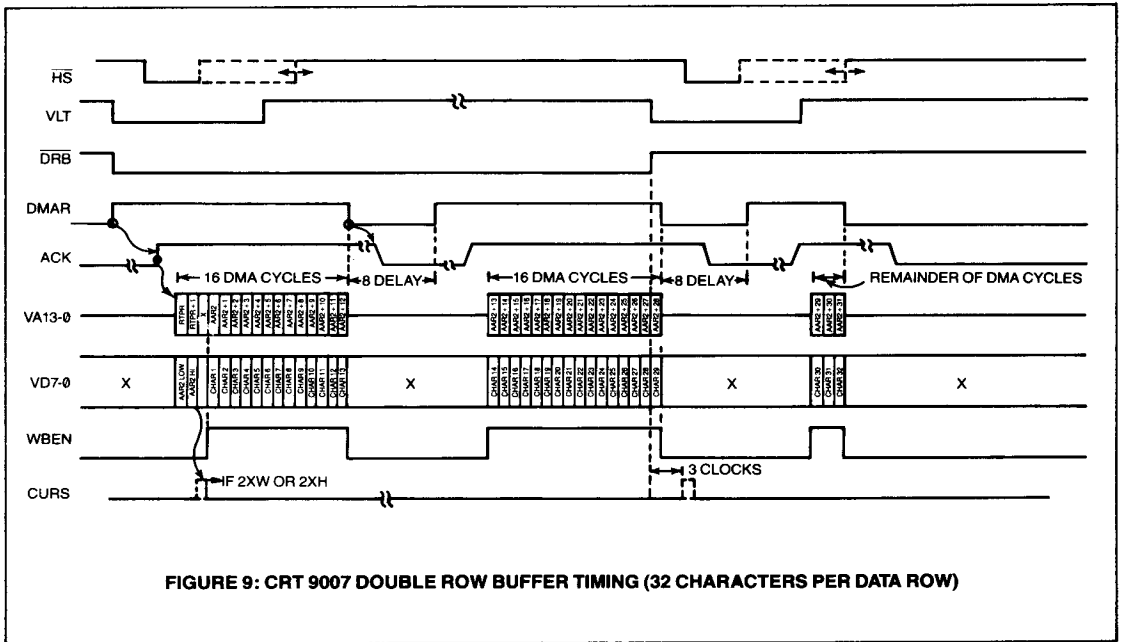


FIGURE 9: CRT 9007 DOUBLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

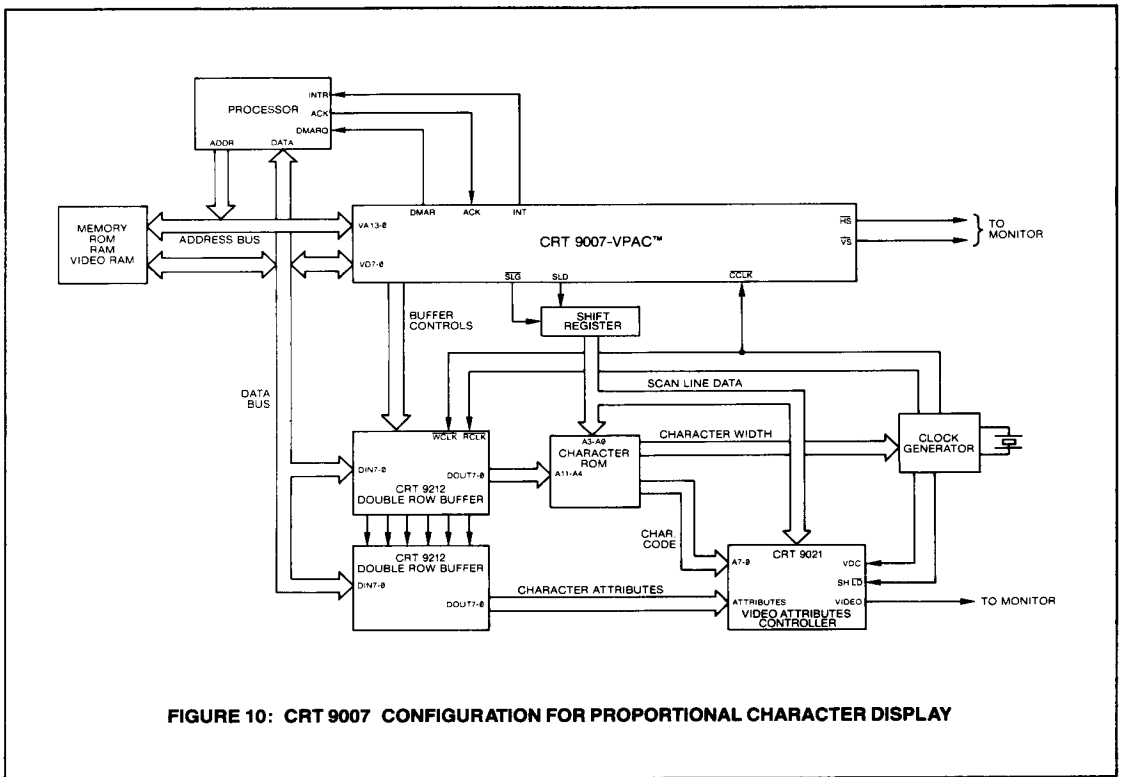


FIGURE 10: CRT 9007 CONFIGURATION FOR PROPORTIONAL CHARACTER DISPLAY

Repetitive Memory Addressing Operation

In this operation mode, the CRT 9007 will repeat the sequence of video addresses for every scan line of every data row. The CRT 9007 address bus will enter its high impedance state during all horizontal retrace intervals (except the retrace interval at a data row boundary if the CRT 9007 is configured in a row driven addressing mode). This arrangement allows for such low end contention schemes as retrace intervention (the processor is only allowed access to video memory during retrace intervals)

and processor priority (the processor has an unlimited access to video memory). A high end contention scheme can be employed which uses a double speed memory such that in a single character period both the processor and the CRT 9007 are permitted access to video memory at predetermined time slots. Figure 11 illustrates the CRT 9007 configured with a double speed memory. Typical timing for this mode is illustrated in figure 12.

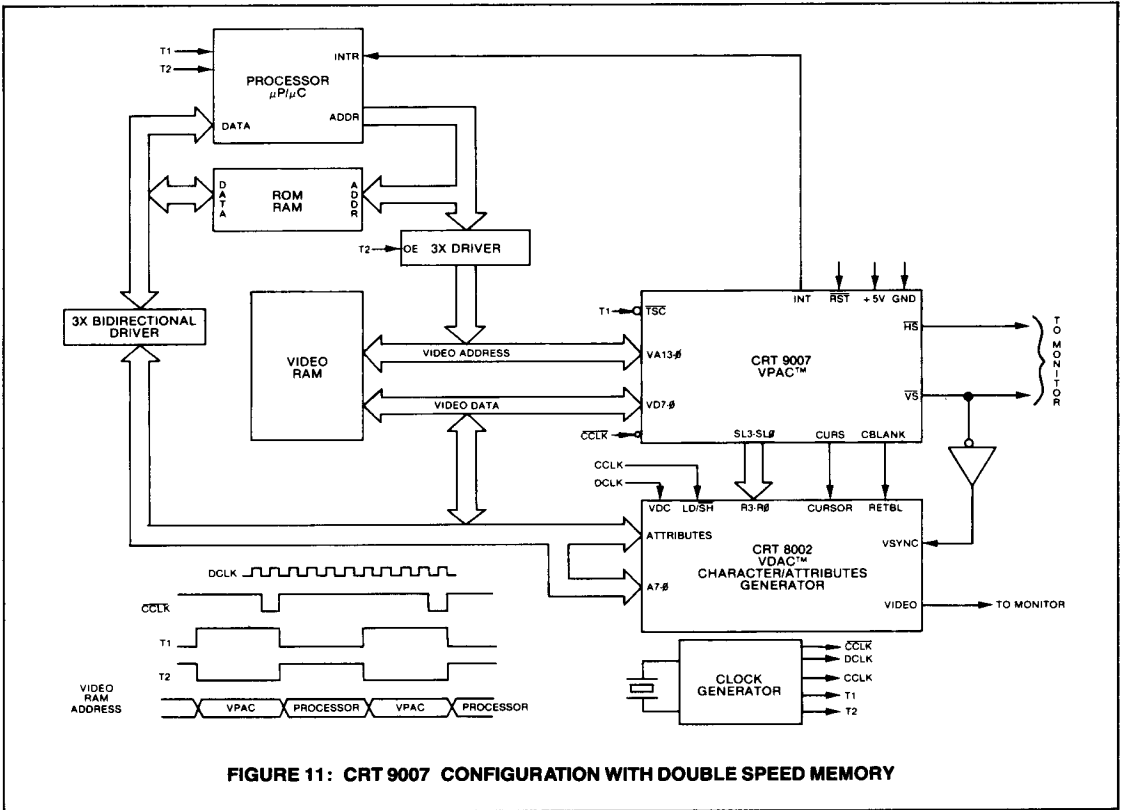


FIGURE 11: CRT 9007 CONFIGURATION WITH DOUBLE SPEED MEMORY

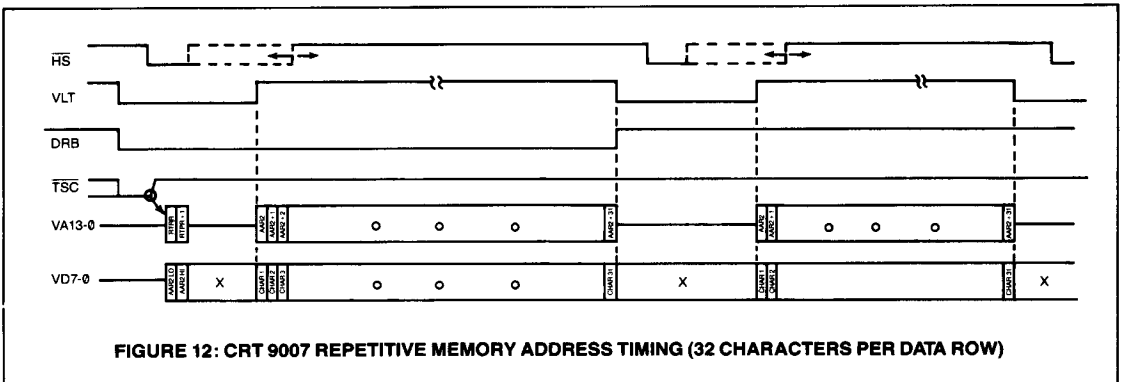
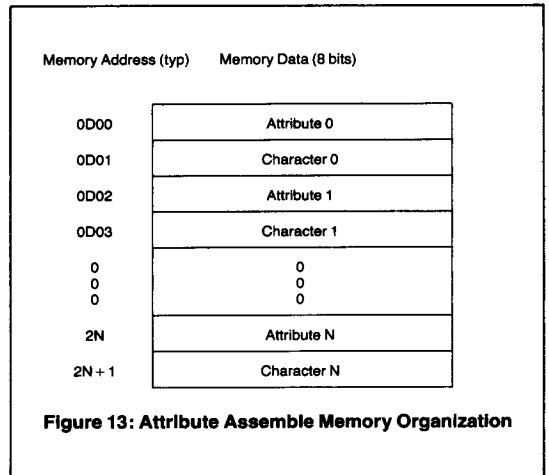


FIGURE 12: CRT 9007 REPETITIVE MEMORY ADDRESS TIMING (32 CHARACTERS PER DATA ROW)

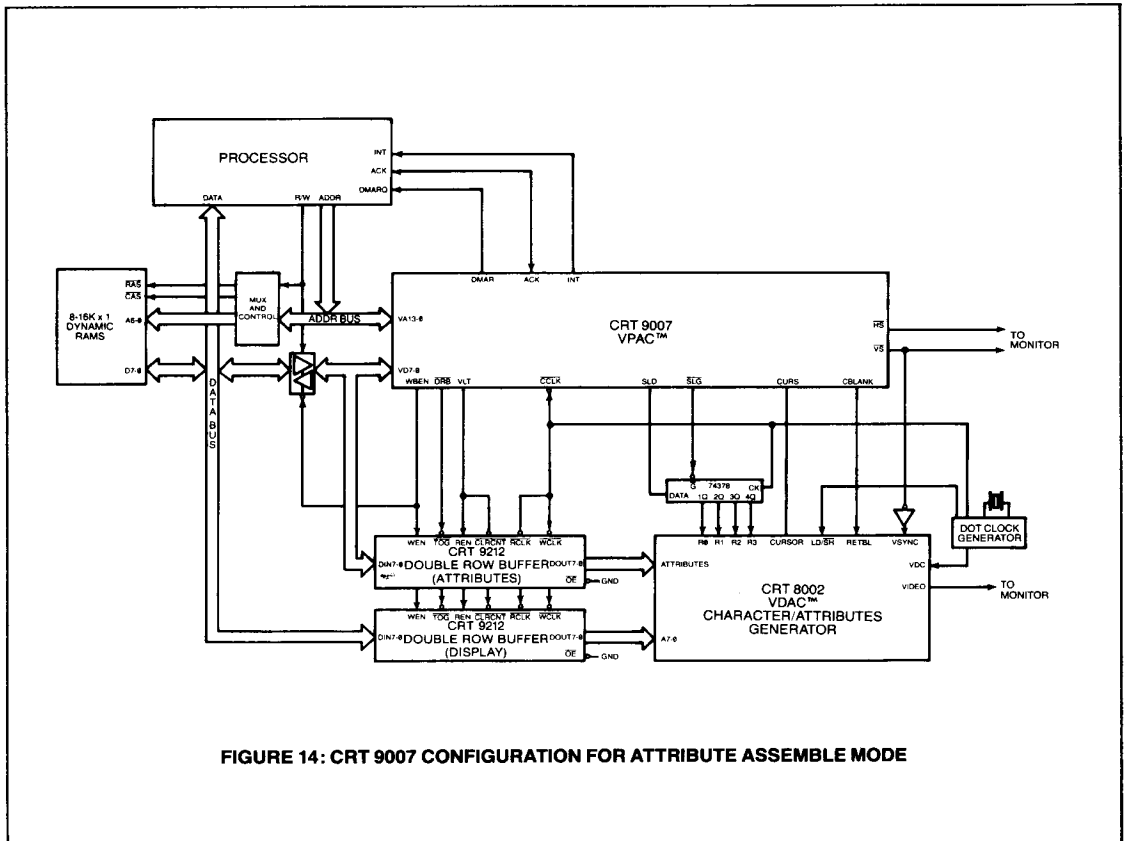
Attribute Assemble Operation

This configuration allows the user to retain an 8 bit wide video memory in which attributes occupy memory locations but not positions on the CRT. This mode assumes that every other display position in video memory contains an attribute. During one clock cycle, attribute data is latched into the CRT 9007; during the next clock cycle a character location is addressed. The attribute data is driven out along with a WBEN signal allowing the character plus its associated attribute to be written simultaneously to two 8 bit double row buffers. Figure 13 illustrates the memory organization used for the Attribute Assemble mode. The first entry in each data row must begin with an attribute.

Figure 14 shows the CRT 9007 configured in the Attribute Assemble mode used with two CRT 9212 Double Row Buffers and 8, 16Kx1 dynamic RAMS. This mode, since it retains an 8 bit wide memory while providing all the advantages of a 16 bit wide memory, lends itself to some cost effective designs using dynamic RAMS. The CRT 9007 will refresh dynamic RAMS because twice the number of the programmed characters per data row are accessed sequentially for each data row.* Figure 15 illustrates typical timing of the CRT 9007 used in the Attribute Assemble mode.



*Note: For 50 Hz operation there usually is about 3 milliseconds extra vertical blanking where refreshing might fail. In this situation the CRT 9007 can be programmed with about 5 more "dummy" data rows while extending the vertical blank signal. This allows the CRT 9007 to start addressing video memory much earlier within the vertical blanking interval and hence provide refresh to the dynamic RAMS. When displaying double height or double width data rows, only half as many sequential locations are accessed each data row and dynamic RAM refresh might fail.



ADDRESSING MODES

Row Table Addressing

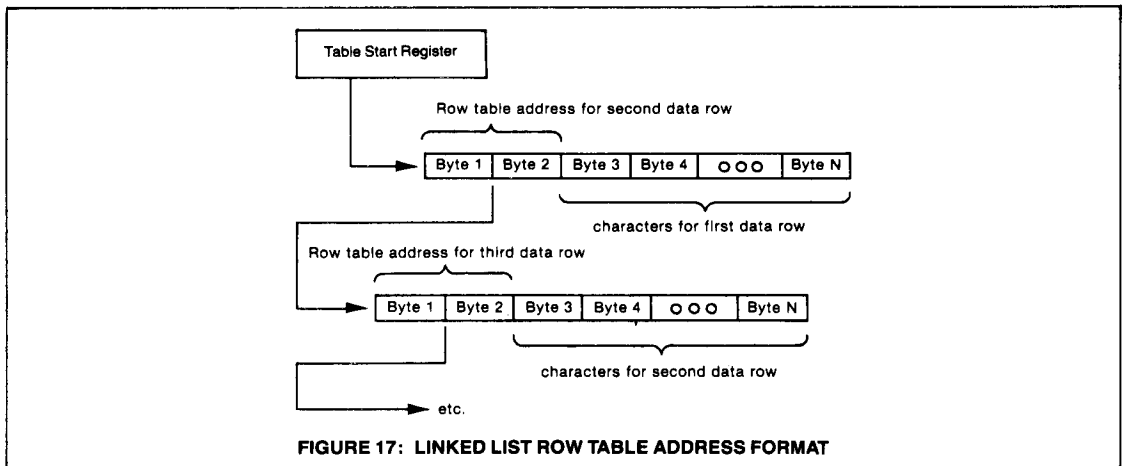
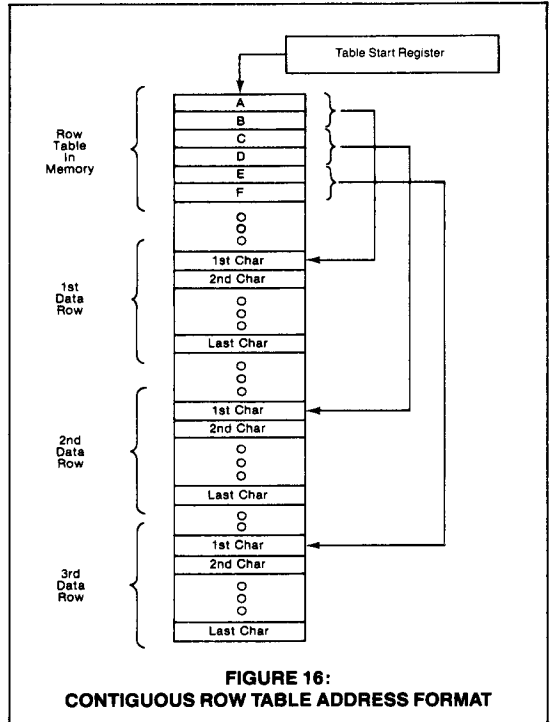
In this addressing mode, each data row in video memory is designated by its own starting address. This provides greater flexibility with respect to screen operations than with other addressing schemes used by previous CRT controllers. The row table, which is a list of starting addresses for each data row, can be configured in one of 2 ways. The choice of row table format is highly dependent upon the particular application and the programmer's preference since each format allows full utilization of the CRT 9007 features.

Contiguous Row Table Format

In this format, the TABLE START REGISTER (RC and RD) points to the address where the row table begins. The contents of the first 2 locations define the starting address of the first data row. These 2 bytes define a 14 bit address where the first byte is the low order 8 bits and the second byte is the high order 6 bits. The 2 most significant bits of the second byte define double height/width characteristics to the current data row. The contents of the third and fourth locations define the address where the second data row begins. Figure 16 illustrates the contiguous row table organization in video memory.

Linked List Row Table Format

In this format the TABLE START REGISTER (RC and RD) points to the memory location which starts the entire addressing sequence into operation. The first byte read is the lower 8 bits and the second byte read is the upper 6 bits of the next data row's start address. The 2 most significant bits of the second byte define double height/width characteristics for the data row about to be read. The third, fourth, fifth, etc., bytes read are the first, second, third, etc., characters of the current data row. Figure 17 illustrates the linked list row table organization in video memory.



Sequential Addressing¹

In this addressing mode, characters on the display screen are located in successive memory locations. The TABLE START REGISTER (RC and RD) points to the address of the first character of the first data row on the screen. In this mode the TABLE START REGISTER does not point to the start of a table but the start of the screen. As each character

is read by the CRT 9007 for display refresh, the internal video address register is incremented by one to access the next character.

For more versatile systems operation in the sequential addressing mode, SEQUENTIAL BREAK REGISTER 1 (R10) and SEQUENTIAL BREAK REGISTER 2 (R12) may be used to define the data rows at which two additional

¹SEQUENTIAL BREAK 2 is not functional in the repetitive memory addressing mode. It is fully functional in all other operation modes.

sequential display areas begin. Note that DATA ROW END REGISTER (R12) is defined as SEQUENTIAL BREAK REGISTER 2 (R12) for the sequential addressing mode only. The starting addresses for these two additional display areas are defined by AUXILIARY ADDRESS REGISTER 1 (RE and RF) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14). When the raster begins painting a data row equal to the number programmed in one of the sequential break registers, the CRT 9007 addresses the video memory sequentially starting with the address specified by the corresponding auxiliary address register. Figure 18 illustrates a display with 80 characters per data row having sequential breaks at data rows 3 and 6.

Using the sequential addressing mode with 2 breaks, it is possible to roll a portion of the screen and keep the rest of the screen stable. Double height/width characteristics can be attached to the 2 sequentially addressed screens defined by SEQUENTIAL BREAK REGISTERS 1 and 2 by using the 2 most significant bits of AUXILIARY ADDRESS REGISTERS 1 and 2. See the description of these 2 registers for their bit definition.

TABLE START REGISTER = 1000
 AUXILIARY ADDRESS REGISTER 1 = 2000
 AUXILIARY ADDRESS REGISTER 2 = 0800
 SEQUENTIAL BREAK REGISTER 1 = 3
 SEQUENTIAL BREAK REGISTER 2 = 6

Data Row	Address range
0	1000 to 104 F
1	1050 to 109F
2	10A0 to 10EF
3	2000 to 204F (Break 1)
4	2050 to 209F
5	20A0 to 20EF
6	0800 to 084F (Break 2)
7	0850 to 089F
8	08A0 to 08EF
	○
	○
	○

Figure 18: Sequential Addressing Example With Two Breaks

Double Height/Width Operation

When double height/width characters (2XH/2XW) are displayed, the following will occur:

1. the CRT 9007 will address half as many characters for each data row by incrementing its address every other character clock.
2. the high speed video shift register supplying serial video to the CRT must shift out dots at half frequency.
3. For double height, the scan line counter outputs (SL3-SL0 or SLG, SLD) are incremented every other scan line.

The CRT 9007 is informed of the double height or double width display modes via the 2 most significant bits of the row table address or the 2 most significant bits of the AUXILIARY ADDRESS registers depending on the selected addressing mode. In any case, once the information is obtained by the CRT 9007, it must initiate the 3 tasks listed above. Tasks 1 and 3 are performed as appropriate and task 2 is performed using the CURS output of the CRT 9007 during CBLANK (horizontal retrace) to signal the external logic that a change in the dot shift frequency is required. The exact time of activation and deactivation of the CURS signal during horizontal retrace is a function of addressing mode, operation mode and actual scan line number to be painted. Tables 1 and 2 show the cursor activation and deactivation times as a function of the buffer configuration and addressing mode for the top scan line of a new data row. Tables 1 and 2 assume a cursor skew of zero. A cursor skew will effect the cursor position during trace as well as retrace time. For all subsequent scan lines, the CURS signal is activated 3 CCLK's after VLT trailing edge and stays active for exactly 1 CCLK assuming no cursor skew. When the cursor is placed on a double height or double width data row, it will become active for 2 CCLK's to allow the cursor to be displayed as double width. If the cursor position is programmed to reside

in the top half of a double height data row, it may become active for all scan lines in both the current and next data row to allow the cursor to be displayed as double height.

For row driven addressing, a particular data row or pair of data rows can appear in one of the following ways as a function of the two most significant bits of the row table address (bits 15 and 14).

- Single height, single width (Row table address bits 15, 14 = 00). The CRT 9007 will display the particular data row as single height, single width.
- Single height, double width (Row table address bits 15, 14 = 01). The CRT 9007 will display the particular data row as single height double width by accessing half as many characters as appear in a single width data row. The CURS signal becomes active during horizontal retrace in the manner described previously.
- Double height, double width top half (Row table address bits 15, 14 = 10). In addition to providing the special timing associated with single height double width data rows, the scan line counter is started from zero and incremented every other scan line until N scan lines are painted (N is the number of scan lines per single height data row). In this way, new dot information appears every other scan line and the top half of the data row appears in N scan lines.
- Double Height, Double Width Bottom Half (Row table address bits 15, 14 = 11)—Same as Double Height, Double Width Top except the scan line counter is started from N/2 (or (N-1)/2 if N is odd), and incremented every other scan line until N scan lines are painted. In single row buffer operation, a double height bottom data row can only stand alone during a smooth scroll operation; otherwise it is assumed to follow a double height top data row.

OPERATION MODE	ADDRESSING MODE	
	Row Driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Single row buffer	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Double row buffer	1 CCLK after high byte of row table read	1 CCLK after ACK leading edge

Table 1: Double Height/Width CURS activation for top scan line of new data row.

OPERATION MODE	ADDRESSING MODE	
	Row driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	at the leading edge of VLT	at the leading edge of VLT
Single row buffer	at the leading edge of VLT	at the leading edge of VLT
Double row buffer	1 CCLK after leading edge of CURS	1 CCLK after leading edge of CURS

Table 2: Double Height/Width CURS deactivation for top scan line of new data row.

PROCESSOR ADDRESSABLE REGISTERS

All CRT 9007 registers are selected by specifying the address on VA5-0 and asserting CS. All 14 bit registers are written or read as two consecutive 8 bit registers addressed low byte first. Only the VERTICAL CURSOR REGISTER and the HORIZONTAL CURSOR REGISTER are read/write registers with 2 different addresses for read or write operations. The register address assigned to each register represents the actual address in hexadecimal form that must appear on VA5-0. Figure 2 illustrates all processor to CRT 9007 register timing. Tables 3a, 3b, and 3c summarize all register bits and provide register addresses.

HORIZONTAL TIMING REGISTERS

The following 4 registers define the horizontal timing parameters. Figure 19 relates the horizontal timing to these registers.

CHARACTERS PER HORIZONTAL PERIOD (R0)

This 8 bit write only register, programmed in units of character times, represents the total number of characters in the horizontal period (trace plus retrace time). This register is programmed with the binary number N where N is the total characters in the horizontal period. The horizontal period should not be programmed for less than 12 characters.

CHARACTERS PER DATA ROW (R1)

This 8 bit write only register, programmed in units of char-

acter times, represents the number of displayable characters during the horizontal trace interval. The difference R0 minus R1 represents the number of character times reserved for horizontal retrace. This register is programmed with the binary number (N-1) where N is the displayable characters per data row.

HORIZONTAL DELAY (R2)

This 8 bit write only register, programmed in units of character times, represents the time between the leading edge of horizontal sync and leading edge of VLT. This register is programmed with N where N represents the time of horizontal delay. By programming this time greater than the horizontal blank interval, one can obtain negative front porch (horizontal sync begins before the horizontal blank interval).

HORIZONTAL SYNC WIDTH (R3)

This 8 bit write only register defines the horizontal sync width in units of character times. The start of the sync pulse is defined by the HORIZONTAL DELAY REGISTER and the end is independent of the start of the active display time. This register is programmed with N where N is the horizontal sync width. However this register must be programmed less than or equal to $\lfloor (A/2) - 1 \rfloor$ where A is the programmed contents of REGISTER 0 rounded to the smallest even integer.

VERTICAL TIMING REGISTERS

The following 5 registers define the vertical timing parameters. Figure 20 relates the vertical timing to these registers.

VERTICAL SYNC WIDTH (R4)

This 8 bit write only register defines the vertical sync width in units of horizontal periods. The start of this signal is defined by the delay register (R5) and the end is independent of the start of the active display time. This register is programmed with N where N is the vertical SYNC width.

VERTICAL DELAY (R5)

This 8 bit write only register, programmed in units of horizontal periods, represents the time between the leading edge of vertical sync and the leading edge of the first VLT after the vertical retrace interval. This register is programmed with (N+1) where N represents the time of the vertical delay.

VISIBLE DATA ROWS PER FRAME (R7)

This 8 bit write only register defines the number of data rows

displayed on the screen. This register is programmed with (N-1) where N is the number of data rows displayed.

SCAN LINES PER DATA ROW (R8)

The 5 LSBs of this write only register define the number of scan lines per data row. These 5 bits are programmed with (N-1) where N is the number of scan lines per data row. When programming for scan lines per data row greater than 16, only the serial scan line pin option (SLD, SLG) can be used.

SCAN LINES PER VERTICAL PERIOD (R8; R9)

Registers R9 and the 3 most significant bits of R8 define the number of scan lines for the entire frame. R8 contains the 3 most significant bits of the 11 bit programmed value and R9 contains the 8 least significant bits of the 11 bit programmed value. The 11 bits are programmed with N where N is the number of scan lines per frame. In the 2 interlace modes, the programmed value represents the number of scan lines per field.

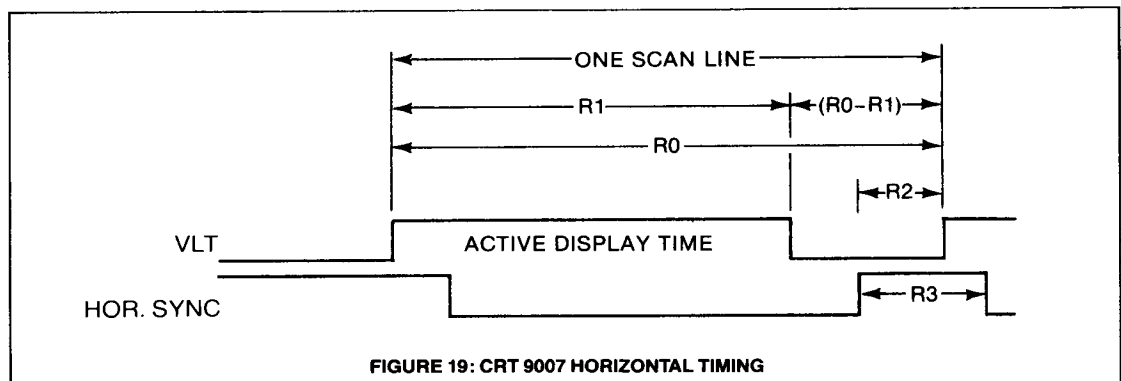
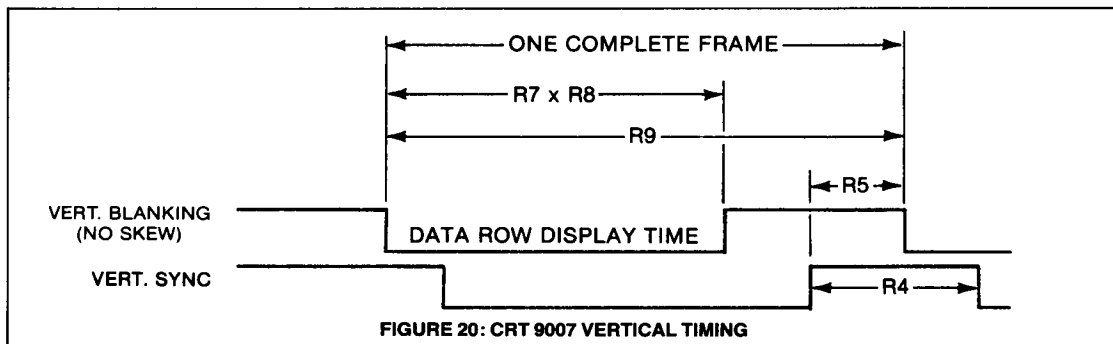


FIGURE 19: CRT 9007 HORIZONTAL TIMING



PIN CONFIGURATION/SKEW BITS REGISTER (R6)

This 8 bit write only register is used to select certain pin configurations and to skew (delay) the cursor and the blank signals independently with respect to the video signal sent to the monitor. The bits take on the following definition:

Bit 7, 6 (Pin Configuration)

These 2 bits, as illustrated in tables 4 and 5, define all pinout configurations as a function of double row buffer mode and non double row buffer mode. (The buffer mode is defined in the CONTROL REGISTER bits 3, 2, and 1.) The attribute assemble mode is assumed to be a double row buffer mode and obeys table 4.

Bits 5, 4, 3 (Cursor skew)

These three bits define the number of character clocks the cursor signal is skewed (delayed) from the VLT signal. The

VLT signal is active for all characters within a data row and a non skewed cursor will always become active within the active VLT time at the designated position. The cursor can be skewed from 0 to 5 character clocks (Bits 5, 4 and 3 programmed from 000 to 101, bit 5 is the most significant bit; bit 3 is the least significant bit). For double height/width data rows, the cursor signal appearing during horizontal retrace is also skewed as programmed.

Bits 2, 1, 0 (Blank skew)

These three bits define the number of character clocks the horizontal blank component of the CBLANK signal is skewed (delayed) from the VLT signal. The edges of VLT will line up exactly with the edges of the horizontal component of the CBLANK signal if no skew is programmed. The CBLANK can be skewed from 0 to 5 character clocks (Bits 2, 1 and 0 programmed from 000 to 101, bit 2 is the most significant bit; bit 0 is the least significant bit).

REGISTER R6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	1	DMAR	WBEN	SLG	SLD	CSYNC	ACK
1	1	DMAR	WBEN	SLG	SLD	LPSTB	ACK
0	0	NOT PERMITTED					
1	0	NOT PERMITTED					

Table 4: Pin configuration for double row buffer and attribute assemble modes.

REGISTER 6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	0	SL3	SL2	SL1	SL0	CSYNC	TSC
1	0	SL3	SL2	SL1	SL0	LPSTB	TSC
1	1	VBLANK	CSYNC	SLG	SLD	LPSTB	TSC
0	1	NOT PERMITTED					

Table 5: Pin configuration for Single Row Buffer and Repetitive Memory Addressing Modes.

DMA CONTROL REGISTER (RA)

This 8 bit write only register allows the user to set up a DMA burst count and delay as well as disable the DMA mechanism of the CRT 9007. The register bits have the following definition:

Bit 7 (DMA Disable)

A logic one will immediately force the CRT 9007 DMA request to the inactive level and the CRT 9007 address bus (VA13-VA0) will enter its high impedance state. After enabling the DMA mechanism by setting this bit to a logic zero, a start command must be issued (see START COMMAND, R15).

Bits 6, 5, 4 (DMA Burst Delay)

These 3 bits define the number of clock delays (\overline{CCLK}) between successive DMAR-ACK sequences. Bit 6 is the most and bit 4 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will delay for 4 (N + 1) clock cycles before initiating another DMA request. If 111 is programmed, however, this will result in a zero delay allowing all characters to be retrieved from video RAM in one DMA burst regardless of the value programmed for the DMA burst count.

Bits 3, 2, 1, 0 (DMA Burst Count)

These 4 bits define the number of DMA operations in one DMAR-ACK sequence. Bit 3 is the most and bit 0 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will produce 4 (N + 1) DMA cycles before relinquishing the bus. When programmed with 0000, the minimum DMA Burst will occur ($4 \times 1 = 4$) and when programmed with 1111 the maximum DMA Burst will occur ($4 \times 16 = 64$). When bits 6, 5, and 4 are programmed with 111, no DMA delay will occur and the Burst count will equal the number of programmed characters per data row as specified in R1. Refer to figures 9 and 15 which illustrate a DMA burst of 16 and a DMA delay of 8 for double row buffer and attribute assemble modes respectively. For single row buffer operation, no DMA delay is permitted and bits 6, 5, 4 must be programmed with 000.

CONTROL REGISTER (RB)

This 7 bit write only register controls certain frame operations as well as specifying the operation mode used. Internal to the CRT 9007, this register is double buffered. Changes in the register are reflected into the CRT 9007 at a particular time during vertical retrace. This allows the user to update the CONTROL REGISTER at any time without running the risk of destroying the frame or field currently being painted.

The bits take on the following definition:

Bit 6 (PB/SS)

- = 0; The smooth scroll mechanism is enabled permitting the SMOOTH SCROLL OFFSET REGISTER (R17) to be loaded in the scan line counter (SL3-0 or SLG, SLD signals) allowing for a scroll on the screen of a predetermined number of scan lines per frame or field. The starting and ending of the smooth scroll operation is defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.
- = 1; The page blank mechanism is enabled. The CBLANK signal is made active high for a continuous period of time starting and ending at the data row defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

Bits 5, 4 (Interlace)—these 2 bits define one of 3 displayed modes as illustrated in figure 21

- = 00; Non interlaced display
- = 10; Enhanced video interlace. This display mode will produce an interlaced frame with the same dot information painted in adjacent odd/even scan lines.
- = 11; Normal video interlace. This display mode will produce an interlaced frame with odd scan lines of characters displayed in odd fields and even scan lines displayed in even fields. This mode can be used to allow the screen to show twice as many data rows at half the height since it effectively doubles the character density on the screen.
- = 01; This combination is not permitted.

Bits 3, 2, 1 (Operation modes): These 3 bits define the various buffer configuration modes as follows:

- = 000; (Repetitive memory addressing)—In this mode the address information (VA13-VA0) appears during every visible scan line and the address bus enters its high impedance state during all retrace intervals. When using a row driven addressing mode (linked list or contiguous), the address bus is in the high impedance state for all retrace intervals except the horizontal retrace interval prior to the top scan line of a new data row. This period can be distinguished from other retrace intervals because the DRB (data row boundary) signal is active.
- = 001; (Double row buffer)—In this mode, the CRT 9007 will address a particular data row from video memory one data row prior to the time when it is displayed on the CRT. During vertical retrace, the first data row is retrieved and loaded into the double row buffer. At the next data row boundary (in this case at the end of vertical retrace), the first data row feeds the character generator while the second data

row is retrieved from video memory. The address bus will enter its high impedance state in accordance with the DMA mechanism for address bus arbitration.

- = 100; (Single row buffer)—In this mode, during the first scan line of each data row, the CRT 9007 will address video memory, load the buffer and feed the character generator at the painting rate of the CRT. If the CRT 9007 is used in a row driven addressing mode, it will drive the address bus during the retrace period prior to the first scan line of each data row in order to retrieve the row table address. It will automatically enter the high impedance state at the end of the first visible scan line of each data row. If the CRT 9007 is used in a sequential addressing mode, it will drive the address bus only during the visible line time of the first scan line of each data row.
- = 111; (Attribute assemble)—In the attribute assemble mode, character data and attribute data are shared in consecutive alternating byte locations in memory. When the CRT 9007 reads an attribute byte, it loads it into its internal attribute latch. During the next memory access, a character byte is fetched. At this time the CRT 9007 isolates its bus from the main system bus and outputs the previously latched attribute. A WBEN signal is produced during every character byte fetch to allow the character and its associated attribute to be simultaneously latched into two double row buffers. This mode assumes that there exists twice as many byte locations as there are displayable character positions on the CRT. The first byte of every data row is assumed to be an attribute.

All other combinations of the CONTROL REGISTER bits 3, 2, 1 are not permitted.

Bit 0 ($\overline{2XC}/1XC$): This bit allows for either single or double height cursor display when the cursor is placed within a double height data row as follows:

- = 1; (Single height cursor)—The CURS signal will appear during every scan line for single height data rows and will appear only during the top half or bottom half of a double height data row depending upon where the VERTICAL CURSOR REGISTER (R18, R38) defines the CURSOR data row.
- = 0; (Double height cursor)—If the VERTICAL CURSOR REGISTER (R18, R38) places the cursor in the top half of a double height data row, the CURS signal will appear during every scan line of the top half (the current data row) and the bottom half (the next data row) of the double height data row. If the cursor is placed in the bottom half of a double height data row or if it is placed in a single height data row, the CURS signal will only appear during the one particular data row.

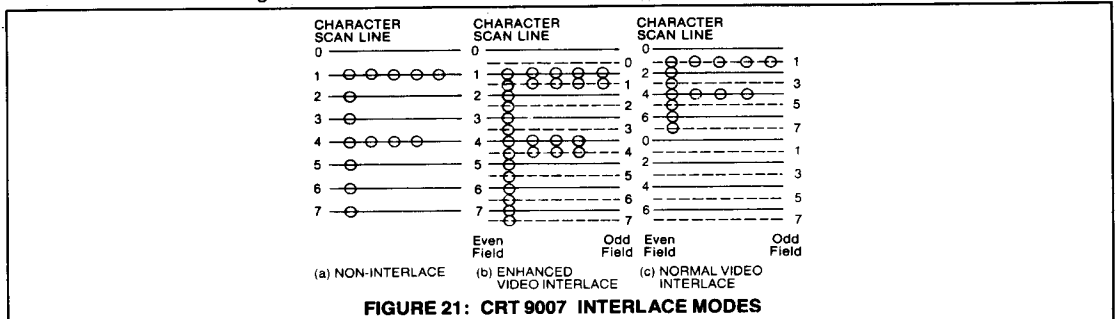


TABLE START REGISTER (RC AND RD)

This 16 bit write only register contains a 14 bit address which is used in a variety of ways depending on the addressing mode chosen; the 2 remaining bits define the addressing mode. Register C contains the lower 8 bits of the 14 bit address. The 6 least significant bits of register D contain the upper 6 bits of the 14 bit address. The 2 most significant bits of register D define four addressing modes as follows:

Register D bits 7, 6:

- = 00; (Sequential addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. 2 sequential breaks are allowed as defined by SEQUENTIAL BREAK 1 (R10) using AUXILIARY ADDRESS REGISTER 1 (RE and RF) and SEQUENTIAL BREAK 2 (R12) using AUXILIARY ADDRESS REGISTER 2 (R13 and R14).
- = 01; (Sequential roll addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. SEQUENTIAL BREAK REGISTER 1 and AUXILIARY ADDRESS REGISTER 1 can be used to cause one sequential break as described in the sequential addressing mode. A second break in the sequential addressing can be defined by SEQUENTIAL BREAK REGISTER 2 (R12) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14) permitting up to 3 separate sequentially addressed screens to be painted.
- = 10; (Contiguous row table mode)—The CRT 9007 will address video memory according to the contiguous row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define an address that points to the beginning of the contiguous row table.
- = 11; (Linked list row table mode)—The CRT 9007 will address video memory according to the linked list row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define the address at which the second row table entry and the first data row reside.

AUXILIARY ADDRESS REGISTER 1 (RE and RF)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER F contain the upper order 6 bits of the 14 bit address and REGISTER E contains the 8 lower order bits of the 14 bit address. When the current data row equals the value programmed in SEQUENTIAL BREAK REGISTER 1 (R10) the remainder of the screen is addressed sequentially starting at the 14 bit address specified in this register. This sequential break overrides any row driven addressing mode used prior to the sequential break.

The 2 most significant bits of REGISTER F allow one to attach double height and/or double width characteristics to every data row in this sequentially addressed area in the following way:

For Double row buffer or attribute assemble mode REGISTER F Bits 7, 6

- = 00; single height single width
- = 01; single height double width
- = 10; even data rows are double height double width top half odd data rows are double height double width bottom half
- = 11; odd data rows are double height double width top half even data rows are double height double width bottom half

For Single row buffer or repetitive memory addressing mode REGISTER F Bits 7, 6

- = 00; single height single width
- = 01; single height double width
- = 10; odd data rows are double height double width top half even data rows are double height double width bottom half
- = 11; even data rows are double height double width top half odd data rows are double height double width bottom half

SEQUENTIAL BREAK REGISTER 1 (R10)

This 8 bit write only register defines the data row number in which a new sequential video address begins as specified by AUXILIARY ADDRESS REGISTER 1 (RE and RF). To disable the use of this break, the register should be loaded with a data row count greater than the number of displayable data rows on the screen.

DATA ROW START REGISTER (R11)

This 8 bit write only register defines the first data row number at which a page blank or smooth scroll operation will begin. Bit 6 of the CONTROL REGISTER determines if a page blank or smooth scroll operation will occur.

DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12)

This 8 bit write only register has a dual function depending on the addressing mode used. For row driven addressing (contiguous or linked list as specified by the 2 most significant bits of the TABLE START REGISTER) this register

defines the data row number which ends either a page blank or smooth scroll operation. The row numerically one less than the row defined by this register is the last data row on which the page blank or smooth scroll will occur. To use the page blank feature to blank a portion of the screen that includes the last displayed data row, this register must be programmed to zero. For sequential addressing, this register can cause a break in the sequential addressing at the data row number specified and a new sequential addressing sequence begins at the address contained in AUXILIARY ADDRESS REGISTER 2.

AUXILIARY ADDRESS REGISTER 2 (R13 and R14)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER 14 contain the upper order 6 bits of the 14 bit address and REGISTER 13 contains the 8 lower order bits of the 14 bit address. In the row driven addressing mode, this register is automatically loaded by the CRT 9007 with the current table address. The two most significant bits of REGISTER 14 specify one of four combinations of row attributes (for example double height

double width) on a row by row basis. Refer to the section entitled Double Height/Double Width operation for the meaning of these 2 bits. In the sequential addressing mode, this register can be loaded by the processor with a 14 bit address and a 2 bit row attributes field. The bit positions are identical for the row driven addressing mode. When the current data row equals the value programmed in DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12), the remainder of the screen is addressed sequentially starting at the location specified by the programmed 14 bit address. The 2 most significant bits of register 14 allow one to attach double height and or double width characteristics to every data row in this sequentially addressed area. The bit definitions take on the same meaning as the 2 most significant bits of AUXILIARY ADDRESS REGISTER 1 and affect the display in an identical manner.

START COMMAND (R15)

After all vital screen parameters are loaded, a START command can be initiated by addressing this dummy register location within the CRT 9007. A START command must be issued after the DMA mechanism is enabled (DMA CONTROL REGISTER bit 7).

RESET COMMAND (R16)

The CRT 9007 can be reset via software by addressing this dummy location. Activation of the RST input pin or initiating this software command will effect the CRT 9007 in an identical manner. The reset state of the CRT 9007 is defined as follows:

CRT 9007 outputs	Reset state
VA13-0	High impedance
VD7-0	High impedance
HS	High
VS	High
CBLANK	High
CURS	Low
VL	Low
DRB	High
INT	Low
Pin 28	Low
Pin 29	Low
Pin 30	Low
Pin 31	Low
Pin 32	Low

SMOOTH SCROLL OFFSET REGISTER (R17)

This register is loaded with the scan line offset number to allow a smooth scroll operation to occur. The offset register causes the scan line counter output of the CRT 9007 to start at the programmed value rather than zero for the data row that starts the smooth scroll interval. The start is specified in the DATA ROW START REGISTER (R11). Typically, this register is updated every frame and it ranges from zero (no offset) to a maximum of the programmed scan lines per data row (maximum offset). For example, if 12 scan lines per data row are programmed (scan line 0 to scan line 11) an offset of zero will cause an unscrolled display. An offset of one will cause a display starting at scan line 1 and ending at scan line 11 (eleven scan lines total). An offset of eleven will cause a display starting at scan line eleven.

The next scan line will be zero, starting the subsequent data row. To allow smooth scroll of double height rows, the programmed range of the register is from zero to twice the programmed scan lines per data row. Whenever the offset register is greater than the programmed scan lines per data row, bit 7 of the register must be set to a logic 1 (offset overflow). It must be set to a logic zero at all other times. The 6 bit offset value occupies bits 6 through 1. Bit 0 must always be programmed with a logic zero. By setting the offset overflow (bit 7) to a logic 1, it is possible to have the bottom half

of a double height data row stand alone in Single Row Buffer Mode by programming the scrolled data row as double height top half and loading R17 with the proper value.

VERTICAL CURSOR REGISTER (R18 or R38)

This 8 bit read/write register specifies the data row in which the cursor appears. To write into this register it is addressed as R18 and to read from this register it is addressed as R38.

HORIZONTAL CURSOR REGISTER (R19 or R39)

This 8 bit read/write register specifies the character position in which the cursor appears. To write into this register it is addressed as R19 and to read from this register it is addressed as R39.

It should be noted that the vertical and horizontal cursor is programmed in an X-Y format with respect to the screen and not dependant upon a particular location in video memory. The cursor will remain stationary during all scroll operations.

INTERRUPT ENABLE REGISTER (R1A)

This 3 bit write only register allows each of the three CRT 9007 interrupt conditions to be individually enabled or disabled according to the following definition:

Bit 6 (Vertical retrace interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when a vertical retrace (i.e., the start of the vertical blanking interval) begins.

Bit 5 (Light pen interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when the LIGHT PEN REGISTER (R3B, R3C) captures an X-Y coordinate. This interrupt, which occurs at the beginning of vertical retrace, reflects the occurrence of a LPSTB input on the frame or field just painted. This interrupt need not be enabled when other CRT 9007 interrupt conditions are enabled since the STATUS REGISTER (R3A) will flag the occurrence of a light pen update and servicing can be done off of other interrupts.

Bit 0 (Frame timer)—This bit, when set to a logic one, allows the CRT 9007 to activate the INT signal once every frame or field at a time when a potential smooth scroll update may occur. In this way the user can use the frame timer interrupt as both a real time clock and can service smooth scroll updates and other frame oriented operations by using the appropriate status bits. This interrupt will occur after the last row table entry is read by the CRT 9007. In single row buffer operation, this will occur one data row before the start of vertical retrace. In double row buffer operation, this will occur two data rows before the start of vertical retrace.

STATUS REGISTER (R3A)

This 5 bit register flags the various conditions that can potentially cause an interrupt regardless of whether the corresponding condition is enabled for interrupt. In this way some or all of the conditions can be reported to the processor via the STATUS REGISTER. If some of the conditions are enabled for interrupt, the processor, in response to an interrupt, simply has to read the STATUS REGISTER to determine the cause of the interrupt. The bit definition of the STATUS REGISTER is as follows:

Bit 7 (Interrupt Pending)—This bit will set when any other status bit, having its corresponding interrupt enabled, experiences a 0 to 1 transition. In this manner, when the processor services a potential CRT 9007 interrupt, it only has to test the interrupt pending bit to determine if the CRT 9007 caused the interrupt. If it did, the individual bits can then be tested to determine the details of the CRT 9007 interrupt. Any noninterruptable status change (corresponding interrupt enable bit reset to a logic 0) will not be reflected in the interrupt pending bit and must be polled by

the processor in order to provide service. The interrupt pending bit is reset when the status register is read. All other bits except Light Pen Update are reset to a logic 0 at the end of the vertical retrace interval. The light pen update bit is reset to a logic 0 when the HORIZONTAL LIGHT PEN REGISTER is read.

Bit 6 (Vertical Retrace)—A logic 1 indicates that a vertical retrace interval has begun.

Bit 5 (Light Pen Update)—A logic 1 indicates that a new coordinate has been strobed into the LIGHT PEN REGISTER. It is reset to a logic zero when the HORIZONTAL LIGHT PEN REGISTER is read. The light pen coordinates may have to be modified via software depending on light pen characteristics.

Bit 2 (odd/even)—For a normal video interlaced display, this bit is a logic 1 when the field about to be painted is an odd field and is a logic zero when the field about to be painted is an even field.

Bit 0 (Frame timer occurred)—This bit becomes a logic 1 either one or two data rows before the start of vertical retrace. Since this bit is set when the CRT has finished reading the row table for the frame or field just painted, it permits row table manipulation to start at the earliest possible time.

VERTICAL LIGHT PEN REGISTER (R3B)

This 8 bit read only register contains the vertical coordinate captured at the time the CRT 9007 received a light pen strobe signal (LPSTB).

HORIZONTAL LIGHT PEN REGISTER (R3C)

This 8 bit read only register contains the horizontal coordinate captured at the time the CRT 9007 received a light pen strobe signal. When a coordinate is captured, the appropriate status bit is set and further transitions on LPSTB are ignored until this register is read. The reading of this register will reset the light pen status bit in the STATUS REGISTER. The captured coordinate may have to be modified in software to allow for light pen response.

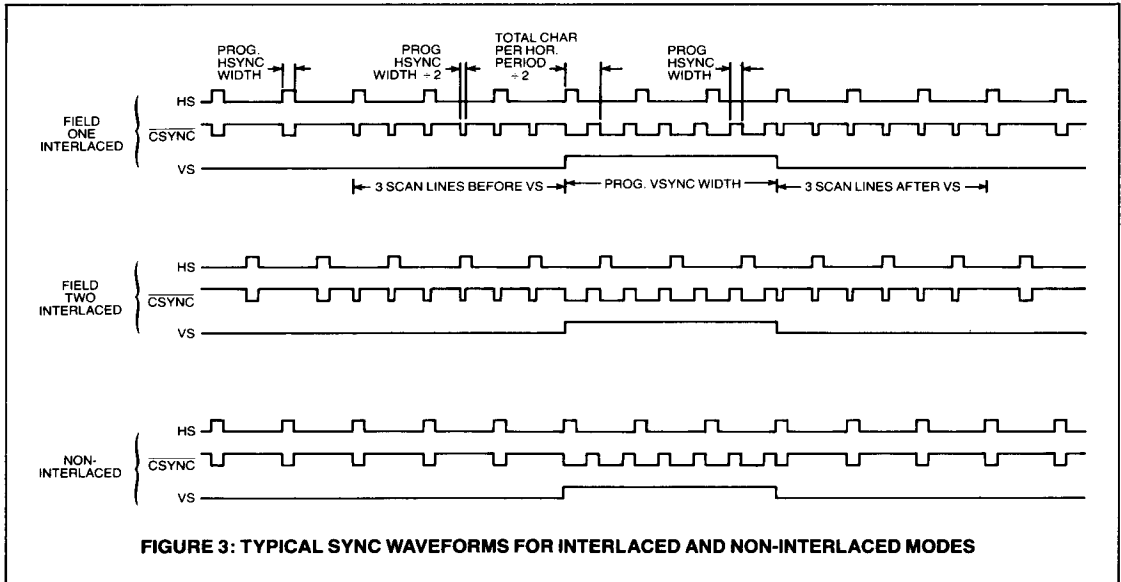


FIGURE 3: TYPICAL SYNC WAVEFORMS FOR INTERLACED AND NON-INTERLACED MODES

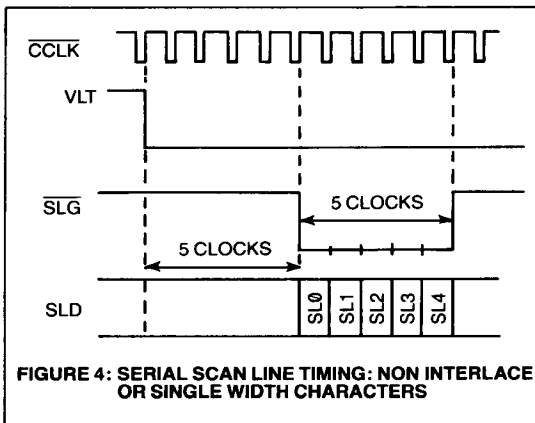


FIGURE 4: SERIAL SCAN LINE TIMING: NON INTERLACE OR SINGLE WIDTH CHARACTERS

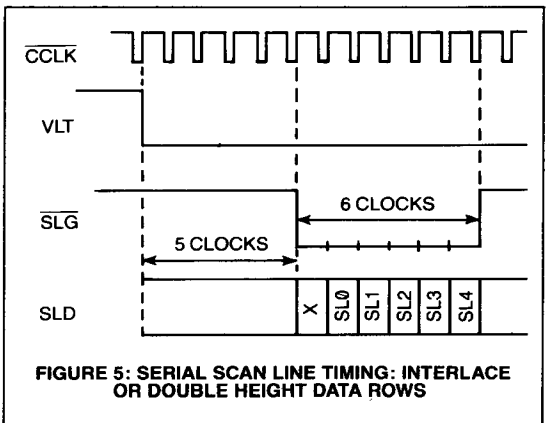


FIGURE 5: SERIAL SCAN LINE TIMING: INTERLACE OR DOUBLE HEIGHT DATA ROWS

CRT9007A/CRT9007B/CRT9007C

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0° to 70°C
Storage Temperature Range	-55° to + 150°C
Lead Temperature (soldering, 10 sec.)	+ 325°C
Positive Voltage on any Pin, with respect to ground	+ 8V
Negative Voltage on any Pin, with respect to ground	-0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
Input voltage			0.8	V	
V _{IL} Low				V	all inputs except $\overline{\text{CCLK}}$ $\overline{\text{CCLK}}$ input; see note 4
V _{IH1} High	2.0			V	
V _{IH2} High	4.3			V	
Output voltage			0.4	V	
V _{OL} Low				V	I _{OL} = 1.6 mA I _{OH} = 100 μ A
V _{OH} High	2.4			V	
Input leakage current			10	μ A	0 ≤ V _{IN} ≤ 3.5V; excluding $\overline{\text{CCLK}}$ V _{IN} = 5V; for $\overline{\text{CCLK}}$ V _{IN} = 0V; for $\overline{\text{CCLK}}$
I _{L1}			50	μ A	
I _{L2}			-300	μ A	
Input capacitance		10		pF	all inputs except $\overline{\text{CCLK}}$ $\overline{\text{CCLK}}$ input
C _{IN1}		25		pF	
Power supply current		100		mA	170

AC ELECTRICAL CHARACTERISTICS²; T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
t _{CV} Clock: Clock period	290		1200	ns	CRT9007A double row buffer CRT9007B or attribute assemble CRT9007C CRT9007A all other operation CRT9007B modes CRT9007C
	330		1200	ns	
	400		1200	ns	
	270		1200	ns	
	300		1200	ns	
	400		1200	ns	
t _{CKL} Clock low	90			ns	measured from 0.8V to 3.5V level measured from 90% to 10% points
t _{CKH} Clock high	150			ns	
t _{CKR} Clock rise time			15	ns	
t _{CKF} Clock fall time			10	ns	
t ₀₁ Output Delay ¹ :			150	ns	CRT9007A/B CRT9007C CRT9007A/B CRT9007C CRT9007A/B CRT9007C CRT9007A/B CRT9007C CRT9007A measured to the 2.3V CRT9007B or 0.5V level on CRT9007C VA13-VA0
			240	ns	
			150	ns	
			240	ns	
			150	ns	
			200	ns	
			150	ns	
			200	ns	
		25	100	ns	
		25	115	ns	
		25	125	ns	
			500	ns	
			185	ns	
			200	ns	
			185	ns	
			200	ns	
			185	ns	
			240	ns	
t _{VDS}	50			ns	
	55			ns	
	60			ns	
t _{VDH}	10			ns	
t _{VDO}			185	ns	
t _{SLG}			240	ns	
t _{SLD}			185	ns	
			240	ns	

AC ELECTRICAL CHARACTERISTICS³; T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
t _{D7}			240 185 240 300 310	ns ns ns ns ns	cursor skew of zero CRT9007A/B cursor skew of one CRT9007C through five CRT9007A/B CRT9007C
t _{D6}					
Processor Read/Write ² :					
t _{AS}	100 110			ns ns	CRT9007A CRT9007B/C
t _{AH}	0			ns	
t _{PW}	165			ns	
t _{CSH}	650			ns	
t _{PDS}	100			ns	
t _{PDH}	0			ns	
t _{PDA}			140 189	ns ns	CRT9007A/B CRT9007C
t _{PDD}	10		85	ns	
t _{IRR}			400 410	ns ns	CRT9007A/B CRT9007C
Miscellaneous Timing:					
t _{ATS}	25		115	ns	measured from the 0.4V level of ACK or TSC falling edge
t _{RW}	4t _{cy}			ns	measured from the 0.4V level falling edge to 0.4V level rising edge
t _{AKW}	50			ns	see figure 24
t _{AKS}	50			ns	see figure 24

NOTE:

- Timing measured from the 1.5V level of the rising edge of $\overline{\text{CCLK}}$ to the 2.4V (high) or 0.4V (low) voltage level of the output unless otherwise noted.
- Reference points are 2.4V high and 0.4V low.
- Loading on all outputs is 30 pF except where noted.
- This level must be reached before the next falling edge of $\overline{\text{CCLK}}$.

CRT9007A1/CRT9007A2**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	-55°C to + 150°C
Lead Temperature (Soldering, 10 sec)	+ 325°C
Positive voltage on any pin (WRT ground)	+ 8V
Negative voltage on any pin (WRT ground)	-0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
V _{IL}	Input voltage: Low			0.8	V	All inputs except $\overline{\text{CCLK}}$ $\overline{\text{CCLK}}$ input; see Note 4
V _{IH1}	High	2			V	
V _{IH2}	High	4.3			V	
V _{OL}	Output voltage: Low			0.5	V	I _{OL} = 1.6 mA
V _{OH}	High	2.4			V	I _{OH} = 100 μ A
I _{L1}	Input leakage current:			10	μ A	0 ≤ V _{IN} < 3.5V; excluding $\overline{\text{CCLK}}$
I _{L2}				50	μ A	V _{IN} = 5V; for $\overline{\text{CCLK}}$
I _{L3}				-200	μ A	V _{IN} = 0V; for $\overline{\text{CCLK}}$
C _{IN1}	Input capacitance:		10	15	pF	All inputs except $\overline{\text{CCLK}}$ at 1 MHz
C _{IN2}			25	50	pF	$\overline{\text{CCLK}}$ input at 1 MHz
I _{CC}	Power supply current:		100	TBD	mA	

PRELIMINARY
Notice: This is not a final specification
Some parameters limits are subject to change

AC ELECTRICAL CHARACTERISTICS³ T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	
t _{cy}	Clock: Clock period	155 200		TBD TBD	ns	CRT9007A2 All operation modes CRT9007A1 CRT9007A2 CRT9007A1 CRT9007A2 CRT9007A1 Measured from 0.8V to 3.5V level Measured from 90% to 10% points
t _{ckl}	Clock low	50 75			ns	
t _{ckh}	Clock high	80 100			ns	
t _{ckr}	Clock rise time			15	ns	
t _{ckf}	Clock fall time			10	ns	
Output delay ¹ :						
t _{d1}				100	ns	CRT9007A2 Measured to the 2.3V or 0.5V lev CRT9007A1 on VA13-VA0
t _{d2}				100	ns	
t _{d3}				100	ns	
t _{d4}				100	ns	
t _{VA}		25		TBD	ns	
t _{DBL}		25		80	ns	
t _{d5}				500	ns	
t _{d6}				135	ns	
t _{dBY}				135	ns	
t _{VDS}		TBD			ns	
t _{VDH}		30			ns	CRT9007A2 Valid for loading auxiliary addr CRT9007A1 register 2 or the attribute latch CRT9007A2 CRT9007A1 C _L = 50 pF
t _{VDO}		TBD			ns	
t _{SLB}				TBD	ns	
t _{SLD}				135	ns	
t _{d7}				135	ns	
t _{d8}				200	ns	Cursor skew of one thru five
Processor read/write ² :						
t _{AB}		100			ns	
t _{AH}		0			ns	
t _{PW}		165			ns	
t _{CSH}		650			ns	
t _{PDS}		100			ns	
t _{PDH}		0			ns	
t _{PDA}				140	ns	
t _{PDO}		10		85	ns	
t _{IRR}				400	ns	
Miscellaneous timing:						
t _{ATB}		25		115	ns	Measured from the 0.4V level of ACK or TSC falling edge Measured from the 0.4V level falling edge to 0.4V level rising edge
t _{rw}		4t _{cy}			ns	
t _{AKW}		50			ns	
t _{AKB}		50			ns	

NOTE:

1. Timing measured from the 1.5V level of the rising edge of CCLK (-) to the 2.4V (high) or 0.4V (low) voltage level of the output unless otherwise noted.
2. Reference points are 2.4V high and 0.4V low.
3. Loading on all outputs is 30 pF except where noted.
4. This level must be reached before the next falling edge of CCLK (-).

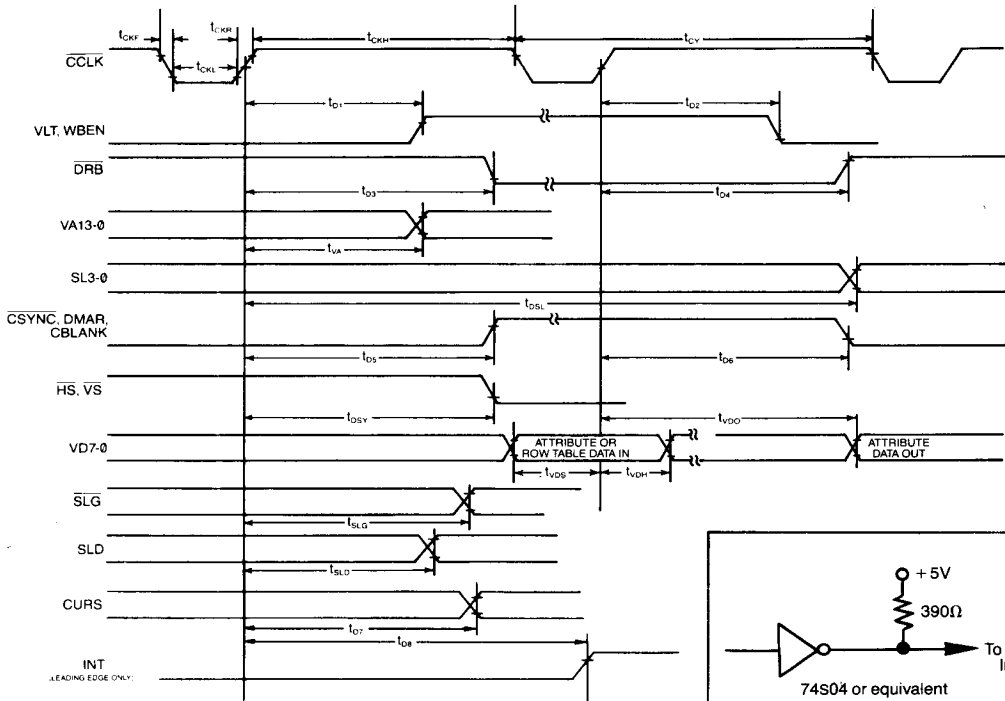


FIGURE 22: CRT 9007 TIMING PARAMETERS: OUTPUT SIGNALS

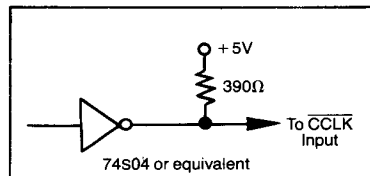


FIGURE 25: RECOMMENDED CCLK DRIVER CIRCUIT

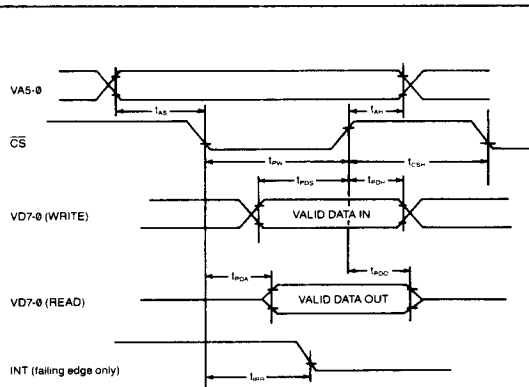
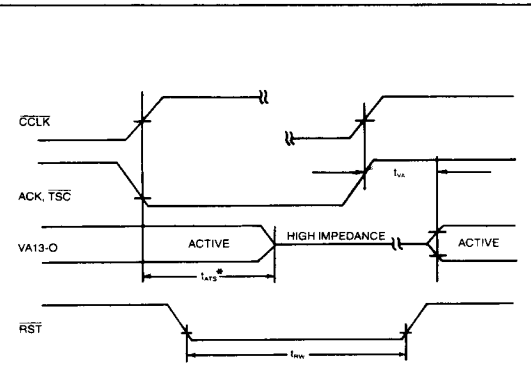


FIGURE 2: CRT 9007 PROCESSOR READ AND WRITE TIMING PARAMETERS



* t_{A13} is controlled directly from ACK or TSC or from the particular CCLK that ends a DMA burst cycle.

FIGURE 23: CRT 9007 MISCELLANEOUS TIMING PARAMETERS

Register Type	ADDRESS DECODE						BIT DEFINITION								REGISTER NUMBER (HEX)				
	VA5	VA4	VA3	VA2	VA1	VA0	D7	D6	D5	D4	D3	D2	D1	D0					
WRITE	0	0	0	0	0	0	MSB CHARACTERS PER HORIZONTAL PERIOD LSB								R0				
WRITE	0	0	0	0	0	1	MSB CHARACTERS PER DATA ROW LSB								R1				
WRITE	0	0	0	0	0	1	0	MSB HORIZONTAL DELAY LSB								R2			
WRITE	0	0	0	0	1	1	MSB HORIZONTAL SYNC WIDTH LSB								R3				
WRITE	0	0	0	1	0	0	MSB VERTICAL SYNC WIDTH LSB								R4				
WRITE	0	0	0	1	0	1	MSB VERTICAL DELAY LSB								R5				
WRITE	0	0	0	1	1	0	PIN CONFIGURATION		CURSOR SKEW		BLANK SKEW		MSB LSB		R6				
WRITE	0	0	0	1	1	1	MSB VISIBLE DATA ROWS PER FRAME LSB								R7				
WRITE	0	0	1	0	0	0	SCAN LINES FRAME (B10)				SCAN LINES PER DATA ROW (B8)				MSB LSB				R8
WRITE	0	0	1	0	0	1	(B7)				SCAN LINES PER FRAME				MSB (B0) LSB				R9

Table 3a: CRT 9007 Screen Format Registers

Register Type	ADDRESS DECODE						BIT DEFINITION								REGISTER NUMBER (HEX)	
	VA5	VA4	VA3	VA2	VA1	VA0	D7	D6	D5	D4	D3	D2	D1	D0		
WRITE	0	0	1	0	1	0	DMA DIS-ABLE		DMA BURST DELAY		DMA BURST COUNT				RA	
WRITE	0	0	1	0	1	1	X	PB/SS		INTERLACE MODES		OPERATION MODES		ZXC/1XC	RB	
WRITE	0	0	1	1	0	0	MSB TABLE START REGISTER (LS BYTE) LSB								RC	
WRITE	0	0	1	1	0	1	ADDRESS MODE		TABLE START REGISTER (MS BYTE)						MSB LSB	RD
WRITE	0	0	1	1	1	0	MSB AUXILIARY ADDRESS REGISTER 1 (LS BYTE) LSB								RE	
WRITE	0	0	1	1	1	1	ROW ATTRIBUTES		AUXILIARY ADDRESS REGISTER 1 (MS BYTE)						MSB LSB	RF
WRITE	0	1	0	0	0	0	MSB SEQUENTIAL BREAK REGISTER 1 LSB								R10	
WRITE	0	1	0	0	0	1	MSB DATA ROW START REGISTER LSB								R11	
WRITE	0	1	0	0	1	0	MSB DATA ROW END/SEQUENTIAL BREAK REGISTER 2 LSB								R12	
WRITE	0	1	0	0	1	1	MSB AUXILIARY ADDRESS REGISTER 2 (LS BYTE) LSB								R13	
WRITE	0	1	0	1	0	0	ROW ATTRIBUTES		AUXILIARY ADDRESS REGISTER 2 (MS BYTE)						MSB LSB	R14

Table 3b: Control and Memory Address Registers

Register Type	ADDRESS DECODE						BIT DEFINITION								REGISTER NUMBER (HEX)			
	VA5	VA4	VA3	VA2	VA1	VA0	D7	D6	D5	D4	D3	D2	D1	D0				
READ OR WRITE	0	1	0	1	0	1	START COMMAND								R15			
READ OR WRITE	0	1	0	1	1	0	RESET COMMAND								R16			
WRITE	0	1	0	1	1	1	OFFSET OVER-FLOW		OFFSET VALUE						MSB LSB 0	R17		
WRITE	0	1	1	0	0	0	MSB VERTICAL CURSOR REGISTER (ROW COORD.) LSB								R18 or R38			
WRITE	0	1	1	0	0	1	MSB HORIZONTAL CURSOR REGISTER (COL. COORD.) LSB								R19 or R39			
WRITE	0	1	1	0	1	0	X VER-TICAL RE-TRACE		LIGHT PEN		INTERRUPT ENABLE REGISTER				FRAME TIMER	R1A		
READ	1	1	1	0	1	0	INT PEND-ING		VER-TICAL RE-TRACE		LIGHT PEN		STATUS REGISTER				ODD/EVEN X FRAME TIMER	R3A
READ	1	1	1	0	1	1	MSB VERTICAL LIGHT PEN REGISTER (ROW COORD.) LSB								R3B			
READ	1	1	1	1	0	0	MSB HORIZONTAL LIGHT PEN REGISTER (COL. COORD.) LSB								R3C			

Table 3c: Cursor, Light Pen, Offset, and Status Registers

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