adaptec, inc.

The Winchester Controller Chip

AIC-100

DESCRIPTION

The Winchester Controller Chip is a Silicon Gate NMOS device that provides the major portion of hardware necessary to build a Winchester disk controller. It is intended to be used with a microprocessor of the Intel 8085 family. The 40-pin package requires only a single +5VDC supply.

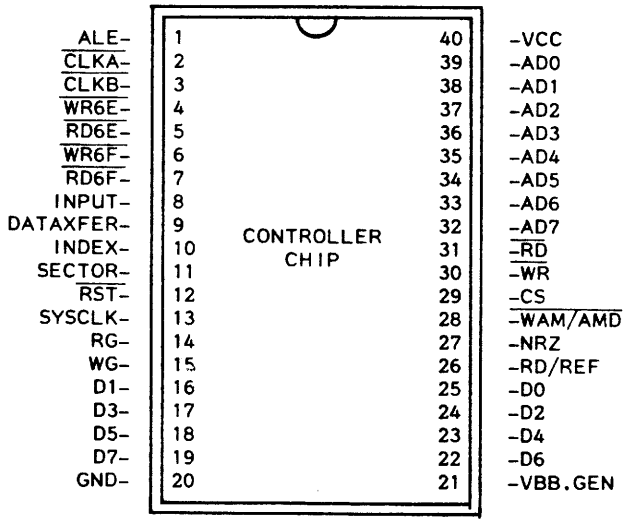
This device is designed to work with an external data separator, such as the two chip implementation available from Adaptec. This combination of devices, along with host memory bus interface chips, provides the system designer a versatile control unit design capability at a minimum chip count. As disk manufacturers increase track density, bit density, and the number of heads per drive in their future products, the Adaptec Winchester Controller Chip will easily accomodate these changes.

FEATURES

Up to 10 MHz bit rate
Multiple sector read/write
32 bit ECC polynomial
High speed correction support
Single +5V supply
NRZ serial interface
High Speed Data Search
Sector defect handling
Variable sector size capability in multiples of 128 bytes
Hard Sectored Disk Capability

APPLICATIONS

Seagate ST506, ST412 compatible drives
Shugart SA1000 compatible drives
SMD drives
ANSI compatible interface drives



FUNCTIONAL DESCRIPTION

Internal to the Controller Chip are three functional blocks:

Microprocessor interface decoder
Sector format sequencer
Data flow

The microprocessor interface is an 8085 family interface. There are 19 registers that provide for operation control, ECC control, drive interface and format control. The device architecture is structured to allow the firmware of an NMOS processor to determine what functions are to be incorporated in the control unit design.

The sector format sequencer performs the basic read/write functions for a disk drive which include:

Read ID
Read ID & Read Data
Read ID & Write Data
Write ID & Write Data

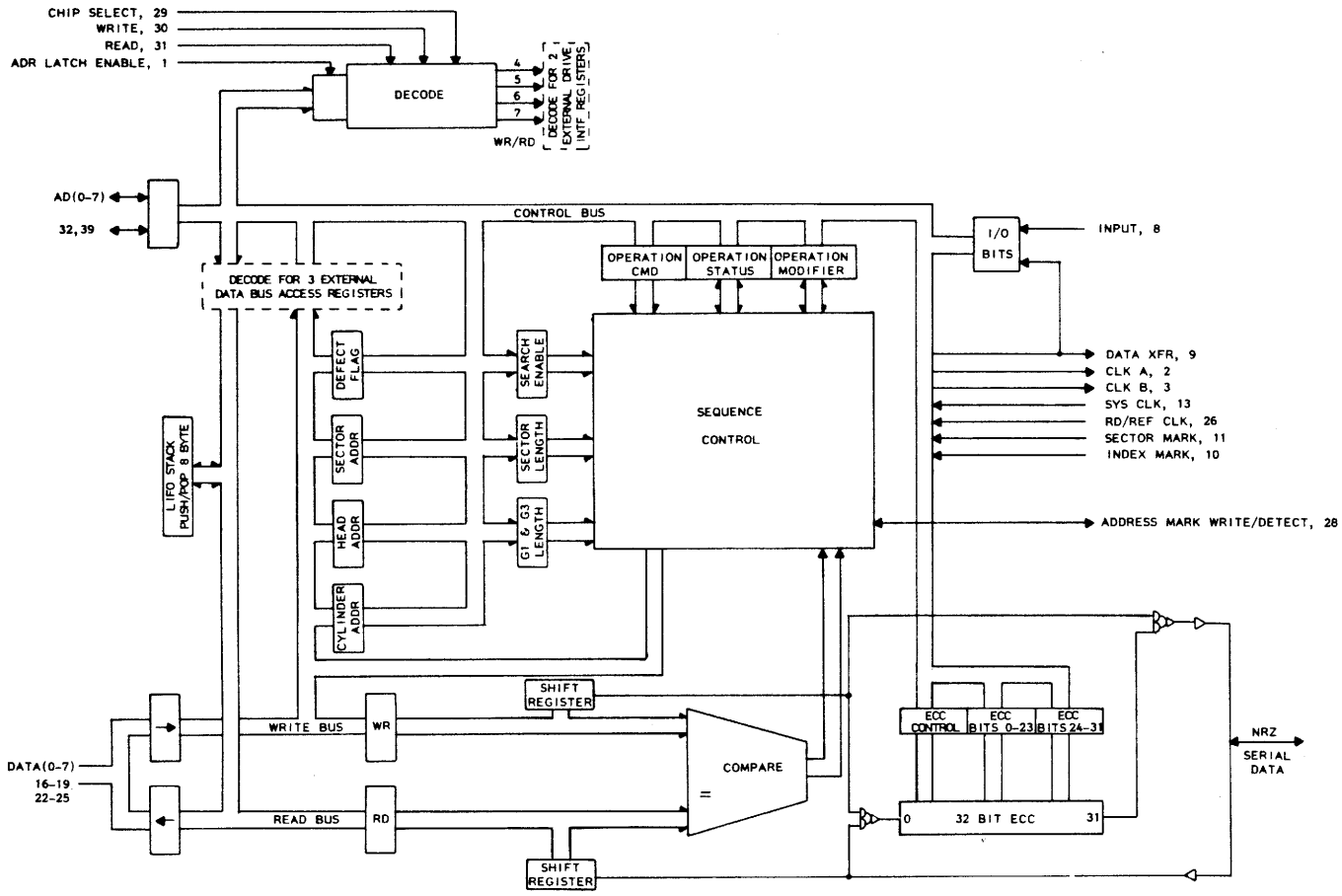
These functions can be modified to perform the search data or verify data functions.

The track format is the same as that recommended by several disk manufacturers except for the addition of a flag byte in the ID field, providing defect flagging at the sector level, and 4 bytes of ECC rather than 2 CRC bytes. The addition of these bytes in ID and data fields is accommodated by a corresponding decrease in the VFO sync fields. A 256-byte data field requires a total of 315 bytes per sector.

The Winchester Controller Chip interfaces with the bidirectional data bus which is connected to an external RAM buffer. The CS, WE and address increment signals required for the sector buffer are derived from the Clock A and Clock B outputs.

The **dataflow** portion of the controller chip is composed of a 32-bit ECC and a serializer/deserializer. Data to be written to the disk enters the device in 8-bit parallel format. It is serialized, and run through a 32-bit ECC generator. The controller chip outputs NRZ serial data followed by 4 bytes of ECC check burst.

The 32-bit ECC does not use the industry standard polynomial. Adaptec has employed a polynomial that will correct 8-bit single burst errors with an extremely low probability of miscorrection and a lower probability of undetected errors.



BLOCK DIAGRAM

FUNCTIONAL OPERATION

The Winchester Controller Chip is designed to be used with an NMOS processor rather than the high speed bit slice designs required for controllers in the past. This NMOS processor is used to maintain "loose" synchronization with what is happening in real time on the disk through the OP Command (R78) and Sequencer Status (R79) registers. The Winchester Controller Chip in return maintains the "close" synchronization of data to and from the disk and provides the signals necessary to control this path. With this device, a lower total part count can be achieved with the same or greater performance than that of a bit slice processor design.

Because the Winchester Controller Chip controls primarily the high speed signals associated with the Winchester disk, the designer is free to choose which type of drive to interface, e.g., ST506, ANSI, SMD, etc. Each of these interfaces can be accommodated with the 4 signal pins RD6E, WR6E, RD6F, and WR6F. An example of an ST506 application is shown in the diagram. These 4 signals are used to read or write drive control lines.

The basic read/write and format sequences are described in the following pages. Note that for the read or write operations a match between the cylinder, head, and sector registers and ID field being read must occur before the operation continues. If a match does not occur, the operation will stop and must be restarted until the desired sector is found. In either case, the last ID field read may be "popped" from the stack (R7F).

If an ECC error is detected after a read data operation, the syndrome is saved in the ECC register and will not be reset until a new read OP is started. By employing registers 71, 72 and 73 the microprocessor can determine if the error is correctable, and if so, the error pattern and displacement from the beginning of the sector. The ECC polynomial is a computer selected code that will correct 8-bit single burst errors. After the error pattern is determined, it is EXORed with the data byte (bytes) in the RAM buffer.

The flag byte of the ID field is used for defective sector handling. When an ID field is read, the flag register and the flag byte from the disk are not compared. The flag byte is pushed onto the LIFO stack along with the cylinder head and sector. The flag byte can be used to implement one of the many defect handling schemes the control unit designer deems appropriate.

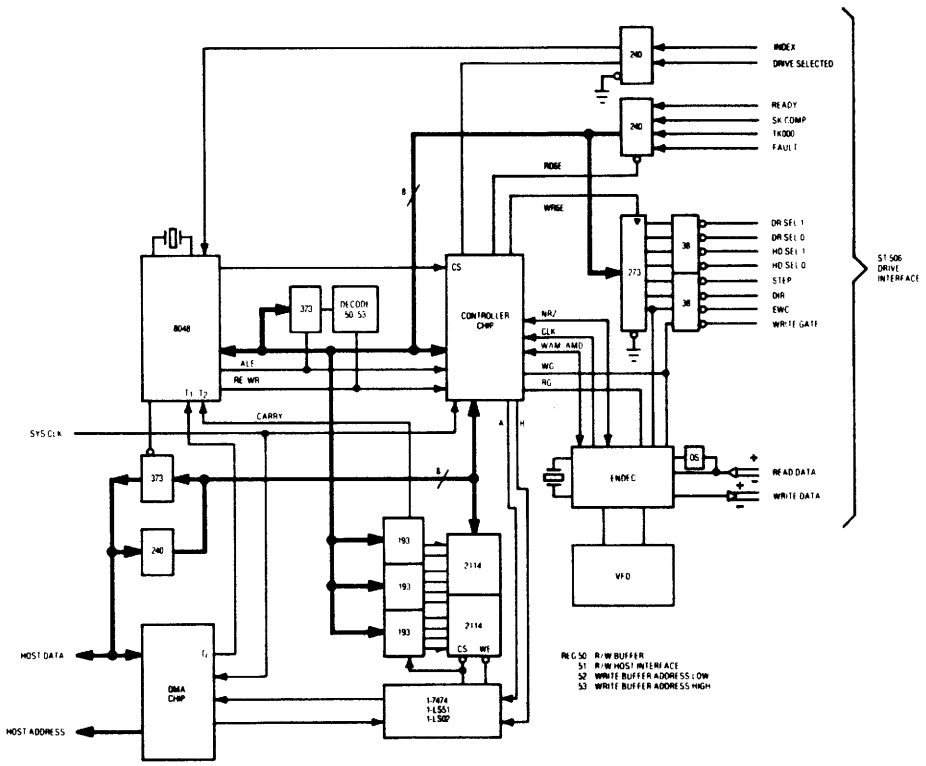
ClkA, ClkB and DataXfer outputs are used to control the external RAM buffer address counter and along with RG and WG generate the CS and WE signals to the RAM. ClkB should be interpreted as the beginning of a Controller Chip memory access with a Clock A period equal to the RAM access time. The D(0-7) pins will contain valid data during that time of the cycle when ClkA is high.

REGISTER ASSIGNMENT

The Winchester Controller Chip has register address locations between 50 hex and FF hex. Most of these locations are not used; however, unused locations above address 70 must not be used by the system since they are not fully decoded by the chip. These registers are intended to be memory mapped in an address block XX50 to XXFF. The upper byte of the address is decoded to provide the chip select function. Table 1 gives a summary of the registers and their functions. Following the table is a detailed discussion of these functions.

REG	TITLE	R=READ; W=WRITE	FUNCTION
50	Buffer data	R/W	Buffer data access
51	Data Bus	R/W	Host Command/Status
6E	Driv Intr 0	R/W	Drive Interface Port 0
6F	Driv Intr 1	R/W	Drive Interface Port 1
70	Not Used		
71	ECC Control	W	ECC correction control
72	ECC 0-23	R	ECC syndrome bits
73	ECC 24-31	R	ECC ERR pattern
74	ECC POLY	W	Low Order Bits
77	ECC POLY	W	High Order Bits
78	OP Command	W	Read/Write sequence control
79	Start OP/Stat	R/W	Operation Status & Go bits
7A	OP Modifier	R/W	Operation Modifiers
7E	Special I/O	R	Input & Data transfer bits
7F	Pop Stack	R	LIFO Stack Read
D0	Gap 1 & 3 Len	W	5-bit Gap1 & Gap3 Length
E0	Cylinder	R/W	Block address Cyl byte
E1	Head	R/W	Block address Head byte
E2	Sector	R/W	Block address Sector byte
E3	Flag	R/W	Block address Flag byte
A4	Search bit	W	Enables Search Co.
C4	Length Sector	W	Programmable Sector Length

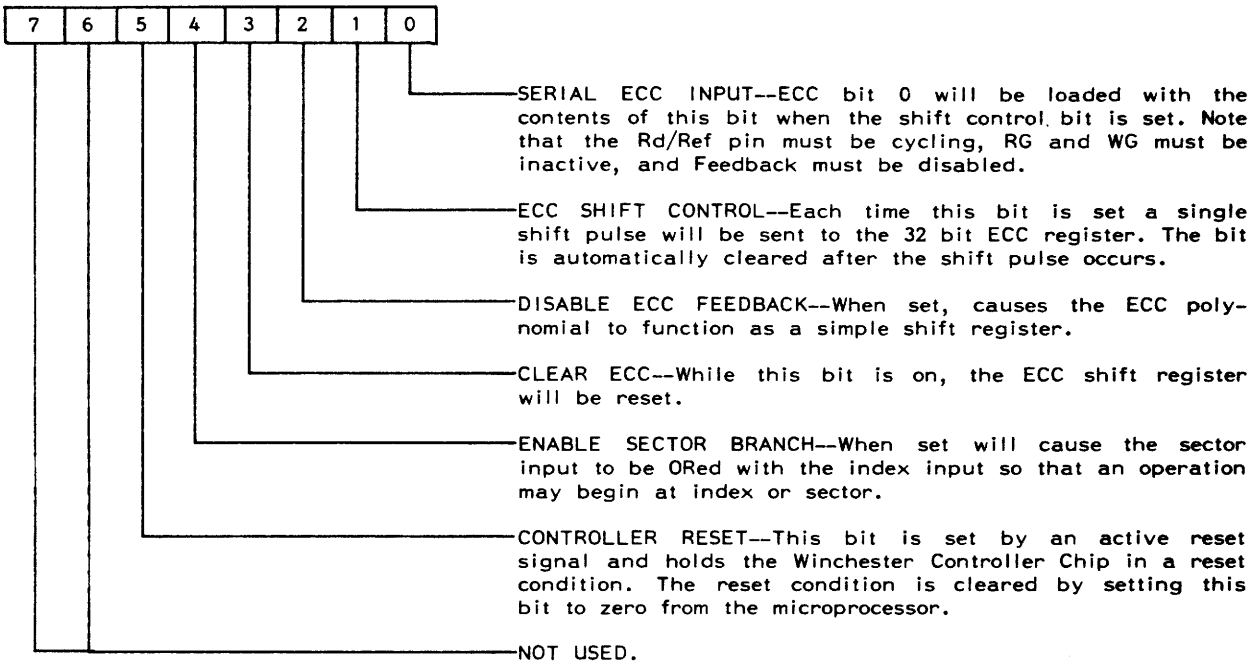
TABLE 1



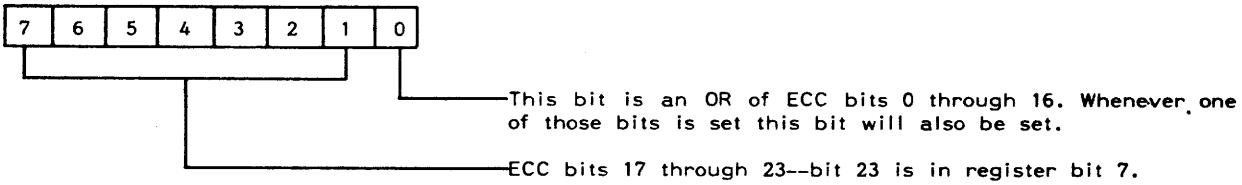
ST-506 Application

INTERNAL REGISTER DESCRIPTION

71 ECC CONTROL (WRITE ONLY)

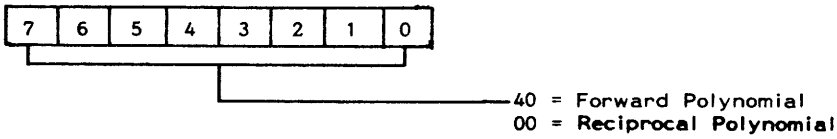


72 ECC (0-23) (READ ONLY)

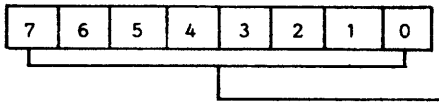


73 ECC (24-31) (READ ONLY)

74 ECC POLYNOMIAL (Bits 0-7)

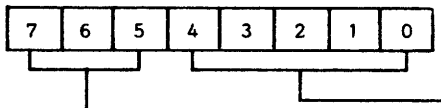


77 ECC POLYNOMIAL (Bits 24-31)



00 = Forward Polynomial
01 = Reciprocal Polynomial

78 OPERATION COMMAND (WRITE ONLY)



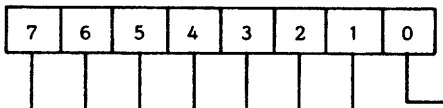
08 = Read ID & start Read Data
09 = Read ID & start Write Data
14 = End Read Data or End Write Data
10 = Wait for index and start writing 4E hex
11 = Format Write ID field
12 = Format Write Data field
13 = At end of format data field write 4E until index

NOT USED.

See OP Command sequence for proper timing as to when these registers are loaded.

79 CONTROLLER CHIP STATUS (READ/WRITE)

READ



COMPARE EQUAL--When set, indicates an equal comparison between the ID registers and the data field. The bit is valid after the ECC has been read.

COMPARE LOW--Same as above except that the data buffer or ID registers were less than the read data.

ECC ERR--After the last bit of ECC data is read, this bit is either set or reset depending on whether all bits in the ECC are zero.

NOT USED. (Always zero)

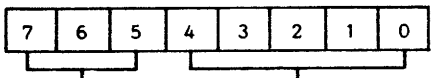
STOPPED--The Winchester Controller Chip has stopped. The ECC contents have not been reset and read gate and write gate are reset. (A new start command can only be sent when this bit is on.)

BRANCH ACTIVE--This bit is set whenever new operation command can be taken. The bit is reset by a read of this register.

DATA TRANSFER--This bit is on whenever data is being transferred either to or from the buffer memory

AM ACTIVE—Is set by reading or writing an AM or sync byte and is reset by reading or writing the ECC bytes. The bit is also reset by a stopped condition.

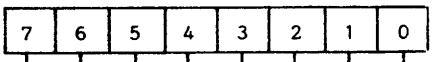
REG 79 CONT'D
WRITE



05 - Start a Read, Update, Write or Search of a sector.
15 - Start a format operation.

NOT USED.

7A OPERATION CONTROL (READ/WRITE)



INDEX PAST--Index point from the device has been detected since the last time this register was accessed. (READ ONLY) This bit is reset when read.

SECTOR PAST--Sector pulse has been received from the device since the last access of this register. (READ ONLY) This bit is reset when read.

NRZ DATA IN--An input of "1" on the NRZ data pin while read gate was on has occurred since the last time this register was accessed. (READ ONLY) This bit is reset when read.

NOT USED.

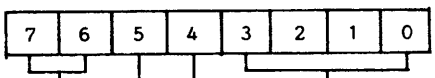
SEARCH OPERATION--This bit must be set whenever a data field compare is required.

SUPPRESS XFER--ClkB will not be generated when this bit is on. Also during WG the data field will be written with 6C.

NOT USED.

INHIBIT DATA FIELD CARRY--When set the carry/load of the micro engine for the data field will be inhibited. After a carry has occurred this bit will be reset.

7E I/O BITS (READ ONLY)



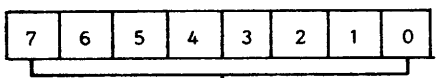
NOT USED.

INPUT--When set the input pin is high.

DATA XFER--Same as R79 bit 6.

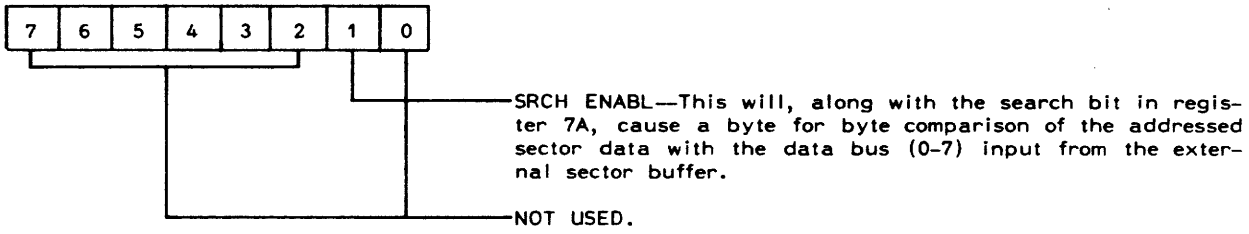
NOT USED.

7F STACK (READ ONLY)

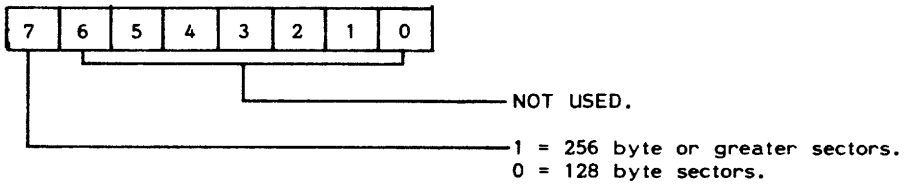


Every time an ID field is read from the disk it is pushed on to the stack. A read of the LIFO stack will pop the flag, sector, head & cylinder bytes of the last ID field read, whether it is matched or not.

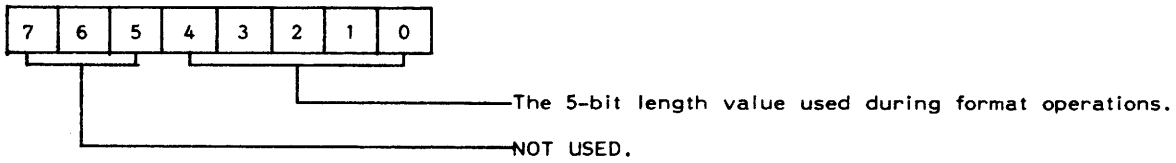
A4 SRCH ENABL (WRITE ONLY)



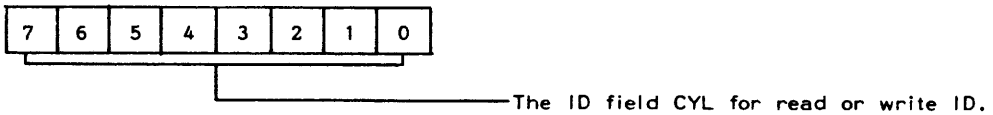
C4 DATA LENGTH (WRITE ONLY)



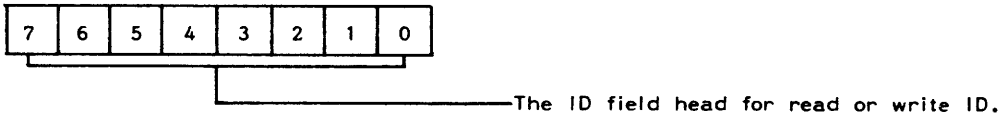
D0 GAP 1 & 3 LENGTH (WRITE ONLY)



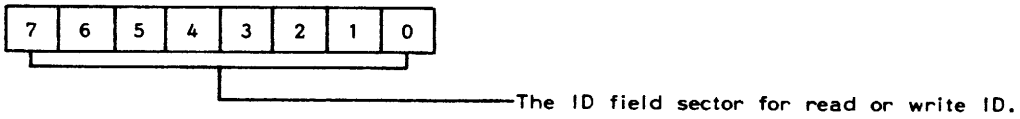
E0 CYL BTYE (READ/WRITE)



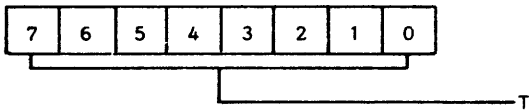
E1 HEAD BYTE (READ/WRITE)



E2 SECTOR BYTE (READ/WRITE)



E3 FLAG BYTE (READ/WRITE)



The ID field flag for read or write ID. Note that this byte does not affect the result of the comparison status.

EXTERNAL REGISTERS

The Winchester Controller Chip has 5 registers decoded that do not exist within the device. Their purpose is to provide versatile control unit design capability.

Registers 50, 51, and 70, when decoded, provide for a bidirectional connection of the microprocessor data bus with the buffer data bus through the Winchester Controller Chip on RD or WR. By designing register 50 as a HOST INTERFACE REGISTER and register 51 as the SECTOR BUFFER ACCESS REGISTER, some external components are not necessary. Register 70 is a spare.

Register 6E and 6F are decoded and a read or write to one of these addresses will generate a negative pulse on one of 4 pins. These signals are then used to enable a 74LS244 onto the microprocessor bus or to latch the bus into a 74LS373. In this manner the drive interface to several types of drives can be accommodated.

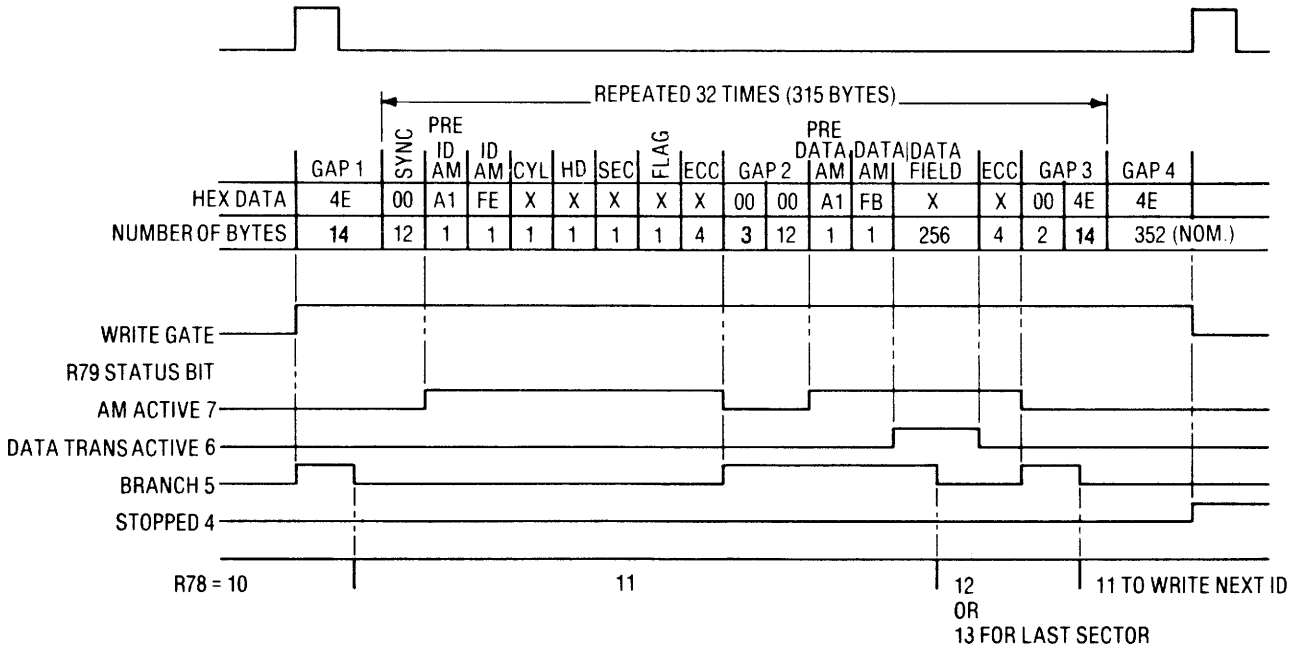
OP COMMAND SEQUENCES

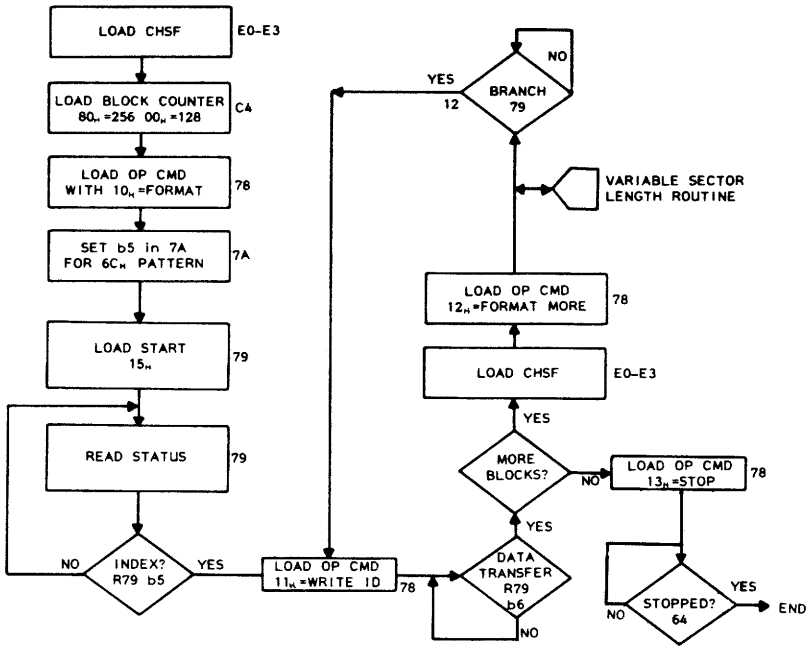
FORMAT DISK

A standard Winchester format employs 256 byte sectors and MFM encoding. This format yields 32 sectors per track. The following examples use this soft sectored 32 format. Any sector size which is a multiple of 128 may be employed (discussed later).

The format track command sequence is as follows:

1. Set RE0, E1, E2, & E3 with the first sector ID and RD0 with GAP1 & GAP3 length.
2. Set C4 with either 00 (128 byte count) or 80 (256 byte count).
3. Set R78 with 10. This will format GAP1 after Index.
4. Set R79 with 15. This will cause the Winchester Controller Chip to wait for Index, then write GAP1.
5. Wait for Branch active (R79 bit 5) to occur, which indicates GAP1 is being written.
6. Set R78 with 11. This will cause the ID to be written.
7. Wait for Data Xfer (R79 bit 6). The data field is now being formatted.
8. Set R78 with 12 and update RE0 through E3 with the next ID field to be written. If R7A bit 5 (suppress) was set before the operation started, 6C Hex will be written in the data field. If not, the contents of the sector buffer is written. If this is the last sector of the track, set R78 with 13 instead of 12 and wait for R79 bit 4 (stopped).
9. Wait for Branch active (R79 bit 5). GAP3 is being written.
10. Repeat steps 6, 7, 8 and 9 for 31 times or the number of sectors to be formatted.





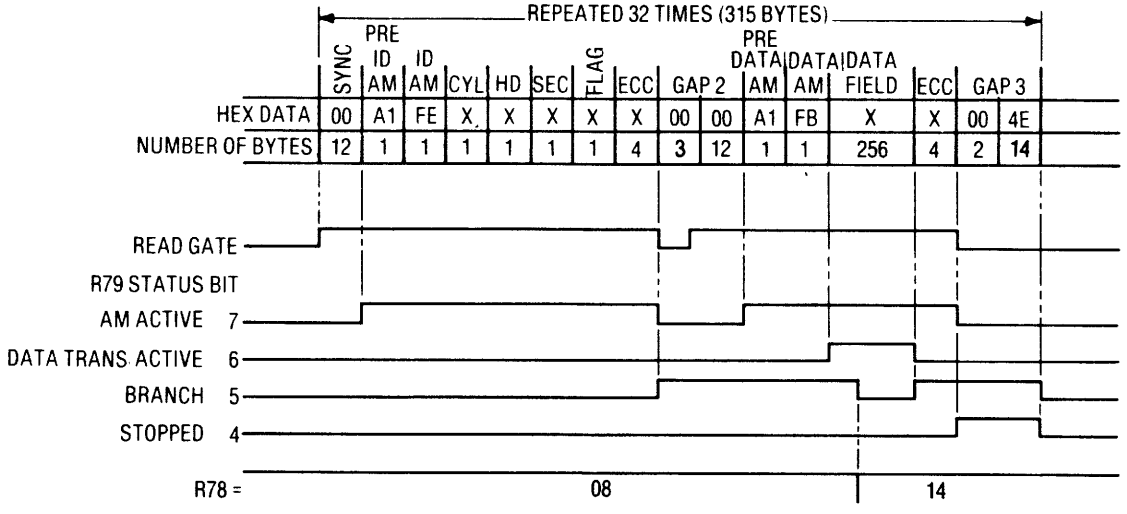
1. To format other than 6C data, do not set b5 in 7A. Sector buffer is then used.

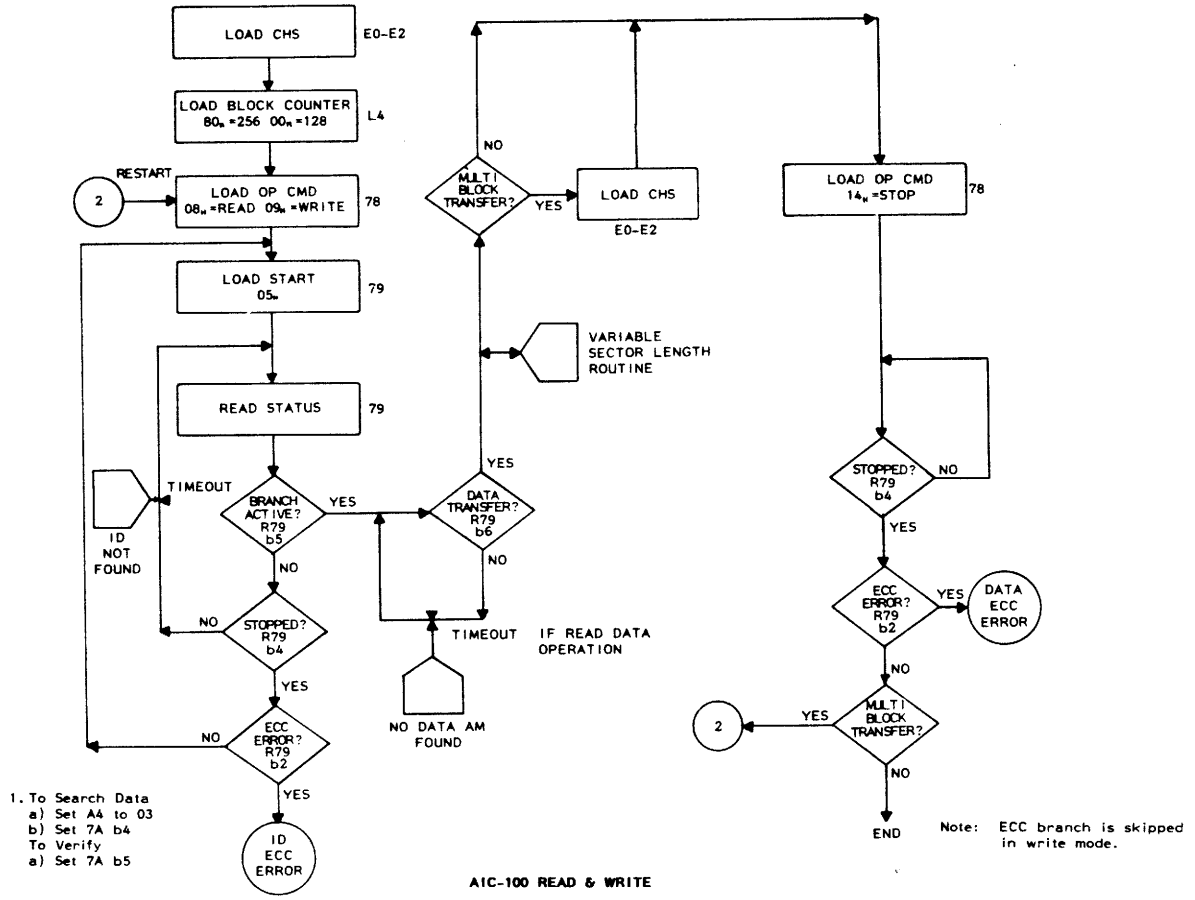
AIC-100 FORMAT

READ DATA

A read data operation is performed as follows:

1. Set RE0, E1, E2 and E3 with the desired sector ID.
2. Set C4 with either 00 (128 byte counter) or 80 (256 byte counter).
3. Set OP command (R78) with 08, the read data command.
4. Set Start Reg (R79) with 05. This will turn on Read Gate and enable the VFO to look for an address mark.
5. Wait for Branch active (R79 bit 5). If the correct ID field was read, the Winchester Controller Chip will continue on to read the data field. If an ID ECC error or incorrect sector was encountered, the stopped bit in R79 will be set. If so, go back to step 4.
6. Wait for Data Xfer active (R79 bit 6). Read data is now being transferred to the sector buffer.
7. If this is a multi-block transfer, update E0-E2 with next sector ID while data is being transferred.
8. Set OP command (R78) with 14. This will stop the Winchester Controller Chip at the end of the data field ECC.
9. Wait for stopped (R79 bit 4).
10. Test ECC error bit (R79 bit 2). If it is set, go to the error correction routine. If not, continue on to read the next sector (step 3) or end.



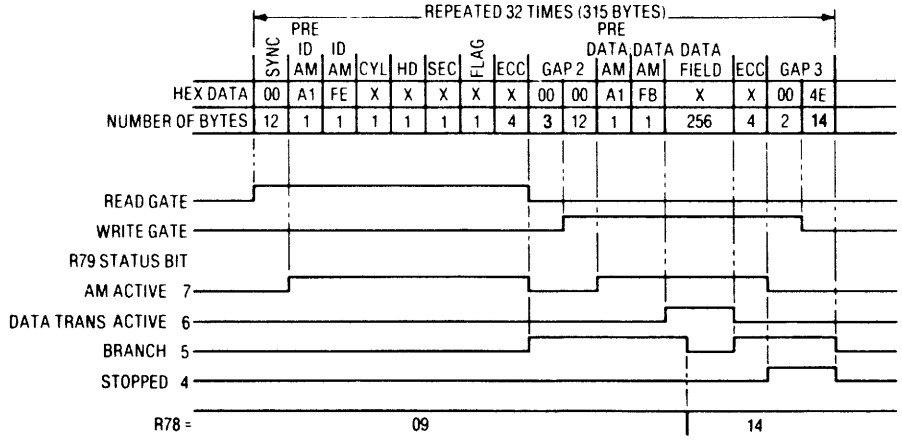


A1C-100 READ & WRITE

WRITE DATA

A write data operation is performed as follows:

1. Set RE0, E1, E2 and E3 with the desired sector ID.
2. Set C4 with either 00 (128 byte counter) or 80 (256 byte counter).
3. Set OP command (R78) with 09, the write data command.
4. Set Start Reg (R79) with 05. This will turn on Read Gate and enable the VFO to look for an address mark.
5. Wait for Branch active (R79 bit 5). If the correct ID field was read, the Winchester Controller Chip will continue on to write the data field. If an ID ECC error or incorrect sector was encountered, the stopped bit in R79 will be set. If so, go back to step 4.
6. Wait for Data Xfer active (R79 bit 6). Write data is now being transferred from the Sector Buffer.
7. If this is a multi-block transfer, update E0-E2 with next sector ID while data is being transferred.
8. Set the OP command reg (R78) with 14. This will stop the write at the end of ECC. Continue to next sector (step 3) or end.



Multi Sector Read or Write

Multiple sector reads or writes are accomplished by loading the next sector address to be found while Data Xfer is active for the present sector and restarting the read or write at step 3 immediately after the stopped bit is set.

Verify Sector

A Verify sector is accomplished by setting the suppress bit (bit 5) on in the OP Modifier reg (R7A) and then performing the read data command sequence. This will verify that the ECC is good for the data field without generating a ClkB.

Search Sector Data

A search of the data field is performed by setting OP Modifier, R7A, bit 4 and the A4 reg bit 2 then entering the read data sequence. The contents of the section buffer will be compared, byte for byte, with the data read from the disk. The result of this comparison is latched in R79 bit 0 and 1. Be sure to reset both R7A-4 and RA4-2 after completion of search.

Variable Sector Size

The Winchester Controller Chip has an 8-bit data field length counter. The most significant bit of this counter is programmable by setting or resetting register C4 bit 7. 0 in this bit will cause 128 byte sectors to be read or written and 1 = 256 byte records.

For multiples of 128 or 256 byte record lengths bit 7 of the OP Modifier (R7A) reg must be employed.

By setting this bit during Data Xfer active before the first 128/256 byte count has expired, the Winchester Controller Chip will be inhibited from going on to ECC and another 128/256 bytes of data will be transferred. OP Modifier bit 7 (R7A bit 7) will be automatically reset whenever the counter overflows, so, by testing this bit, a count of blocks may be accomplished.

PROGRAMMING 5-BIT ECC CORRECTION

After each read data operation a read error may have occurred. This may be determined by reading register 79. If bit 2 is set, an error did occur and the following procedure is employed to determine if the error is correctable. Note that the majority of read errors are soft (i.e., caused by noise) and that the correction algorithm is time consuming. It is recommended that the record be re-read before attempting correction.

The general flow of the algorithm for 5-bit correction is as follows:

1. Off-load the 32-bit syndrome into local RAM.
2. Shift the syndrome back into the ECC register in reverse order, swapping the syndrome end for end.
3. Change the ECC polynomial from forward to reciprocal.
4. Shift the ECC until all bits except the high order (27-31) bits are zero (correctable) or the number of shifts are greater than the number of bits in the record (uncorrectable).
5. If correctable, the number of shifts represent the displacement of the error from the end of the record (the last bit of the ECC). The error pattern is located in bits 27-31 of the ECC register. This pattern is exclusive OR'd with the appropriate bits in memory to correct the error.

Note that 8-bit correction is accomplished by allowing bits 24-31 to be non-zero in step 4.

DETAILED PROGRAMMING STEPS

A detailed flow of error correction for the AIC-100 chip is as follows:

1. After a read error is detected, disable feedback by setting R71=04_H.
2. Store contents of R73 in RAM(x), bits 24-31.
3. Shift ECC 8 times by setting R71=06_H eight times.
4. Store contents of R73 in RAM(x+1) bits 16-23.
5. Shift ECC 8 times by setting R71=06_H eight times.
6. Store contents of RAM(x+2) bits 8-15.
7. Shift ECC 8 times by setting R71=06_H eight times.
8. Store contents of R73 in RAM(x+3) bits 0-7.
9. Clear ECC and disable feedback by setting R71 to 08 and then to 04.
10. Right rotate location RAM(x+3) and test if carry is set: (i.e., test bit 0)
    if set, then load R71=$C7_H$
    if not set, then load R71=$C6_H$
    repeat operation 7 more times to load entire byte.
11. Repeat step 10 for RAM locations X+2, X+1 and X until all 32 bits of the syndrome are loaded into the ECC in reverse order.
12. Load R74=00_H & R77=01_H to enable the reciprocal polynomial and disable the forward polynomial.
13. Enable feedback by setting R71=00_H.
14. Shift ECC once by setting R71=02_H and increment a software counter.
15. Test to see if the software counter is greater than the record length;
    if yes, the error is uncorrectable, re-enable the forward polynomial and end operation.
16. Test to see if R72=00_H;
    if yes, go to step 17.
    if no, go to step 14.
17. For 5-bit correction test to see if R73 bits 0, 1 and 2 are zero;
    if yes, go to step 18.
    if no, go to step 14.
    or, for 8-bit correction, go directly to step 18.

Note that for a 256 byte record length in bits is:

4*8+256*8+2*8 = 2096 bits
ECC+Data+AM & SYNC =# of bits per data field

18. Subtract hardware offset of 24 from the shift count. If a correctable error is located within the ECC or the SYNC & AM bytes, the data field is good and no further action is required. (Count $\leq$ 48). R73 bits 3-7 are the mirror image of the error pattern for 5-bit correction (0-7 for 8-bit). The value of the software counter equals the bit displacement from end of the record.
19. Mirror (invert) the data in R73 for exact error pattern.
20. The bit displacement must now be converted to a byte count and the error pattern shifted to the appropriate byte boundary.
21. The error pattern may now be EXORed with the data in memory to correct the error.

PIN ASSIGNMENTS/FUNCTION

SIGNAL	PIN	DESCRIPTION
AD0-AD7	32-39	Bidirectional Address/Data bus used for microprocessor interface to 8085 family bus.

INPUT PINS

SIGNAL	PIN	DESCRIPTION
ALE	1	Address Latch Enable from microprocessor
WR	30	Write signal from u processor that will latch AD(0-7) data in the appropriate reg.
RD	31	Read signal from u processor enables the contents of appropriate reg. onto the AD(0-7) bus.
CS	29	Chip select input from u processor must be high only during bus cycles for the Winchester Controller Chip.
RST	12	Reset stops all operations within the chip and drops the RG, WG, WAM & NRZ data outputs. Registers 71 through 7E are reset.
SYSCLK	13	System Clock is a 3 to 5 MHz signal used internally by the Winchester Controller Chip.
RD/REF CLK	26	This input is a multiplexed signal from the data encode/decode circuit. The frequency of this clock is the bit rate clock of the drive. During Read Gate this pin is sourced from the VFO oscillator. At all other times it must be driven from the write oscillator.
INDEX	10	Index is an input from the disk drive that occurs once per revolution and is a minimum pulse width of 9 bit times.
SECTOR	11	When a sectored disk is used, this pin is the minimum byte wide sector pulse input.
INPUT	8	A general purpose input pin that is sampled by reading register 7E.

OUTPUTS

SIGNAL	PIN	DESCRIPTION
RG	14	Read Gate output enables the VFO to lock onto the read data from the drive. After RG goes high, all clocking within the Winchester Controller Chip stops and waits for an AMD input. Once AMD is active, the NRZ input is enabled and the Winchester Controller Chip will deserialize data after an "A1" hex pattern is detected.
WG	15	Write Gate output is used to enable writing of the NRZ data output to the disk drive.
CLK A	2	Clock A is an output that is the SYSCLK divided by 2 when the Winchester Controller Chip is not reading or writing data and is the Rd/Ref clock divided by 4 when it is reading or writing.
CLK B	3	Clock B is a pulse at the beginning of every byte transferred between the buffer and the Winchester Controller Chip. Clock B will always overlap the high to low transition of Clock A.
RD6E	5	READ REGISTER 6E--This output will go low during the RD input if address 6E has been latched in the Winchester Controller Chip when CS is active.
WR6E	4	WRITE REGISTER 6E--This output will go low during the WR input if address 6E has been latched in the Winchester Controller Chip when CS is active.
RD6F	7	READ REGISTER 6F--This output will go low during the RD input if address 6F has been latched in the Winchester Controller Chip when CS is active.
WR6F	6	READ REGISTER 6F—This output will go low during the RD input if address 6F has been latched in the Winchester Controller Chip when CS is active.
DATA XFER	9	DATA TRANSFER--This output is high when data is being input or output on D(0-7).

BIDIRECTIONAL

SIGNAL	PIN	DESCRIPTION
D0-D7	16-19, 22-25	Data 0-7 are byte parallel bidirectional lines that contain the data to be written or read from the sectors on the disk.
NRZ	27	NRZ Read/Write data is the serial data to the disk when WG is active and serial data input from the disk when RG is active.
WAM/AMD	28	Write Address Mark/Address Mark Detected. This pin is an output during WG and will be and active low one-bit wide pulse whenever an address mark is to be written. Address Mark Detected input is an active low one byte wide pulse whenever RG is active. This input indicates to the Winchester Controller Chip to enable clocking the NRZ input.

POWER

SIGNAL	PIN	DESCRIPTION
VCC	40	+5V +/- 5%
VBB	21	No Connection
GND	20	+5V Return

INPUTS All inputs except NRZ RD/WR Data, RD/REF & WAM/AMD

	MIN	MAX	UNITS
VIL DC		0.4	V
VIH DC	2.4		V
VIL AC		0.8	V
VIH AC	2.0		V
Cin		10	pf
IIL		-40.0	uA

Note: Reset input has approximately 1.5V hysteresis.

INPUTS NRZ RD/WR DATA, RD/REF CLOCK & WAM/AMD

	MIN	MAX	UNITS
VIL DC		0.3	V
VIH DC	4.0		V
VIL AC		0.6	V
VIH AC	3.5		V
Cin		10	pf
IIL		-40.0	uA

OUTPUTS

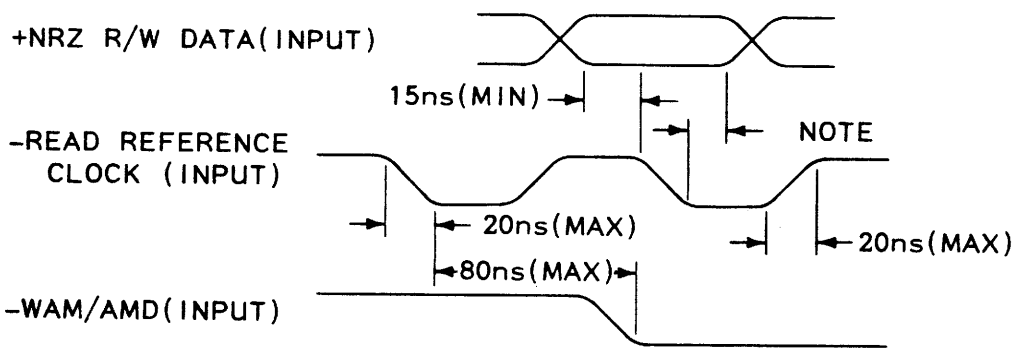
	MIN	MAX	UNITS
VOL DC		0.4	V
VOH DC	2.4		V
VOL AC		0.8	V
VOH AC	2.0		V
Cext		30	pf
IOL	2.0*		mA

*+Read Gate & Write Gate have 5.0 mA IOL (Min) output current.

OPERATING CONDITIONS

Power: +5Vdc +/- 5%
Temperature: 0 to +50 degrees C

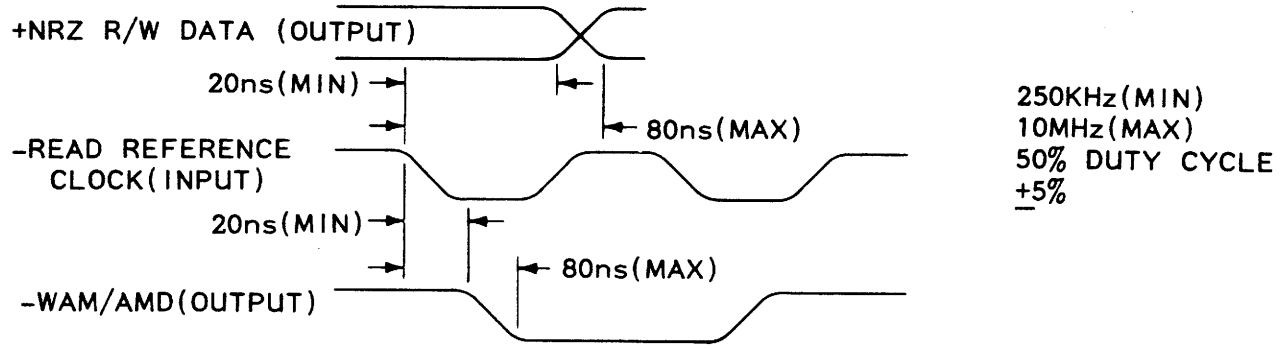
A. +READ GATE=1, +WRITE GATE=0



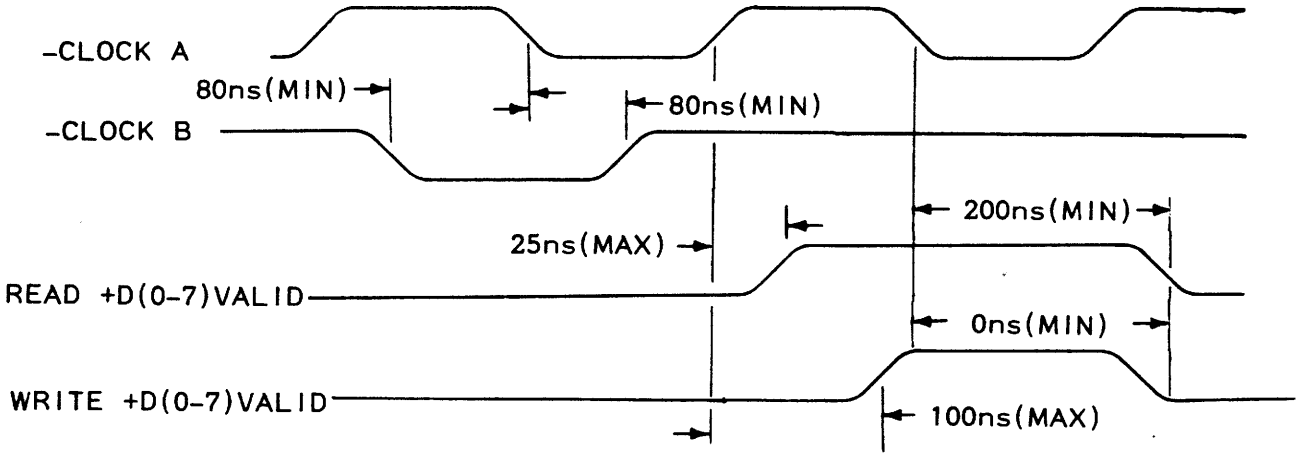
250KHz(MIN)
10MHz(MAX)
50% DUTY CYCLE
±5%

Note: Data must be valid until Rd/Ref clock falls to 0.6V.

B. +READ GATE=0, +WRITE GATE=1



C. READ/WRITE DATA VALID UNDER DATA XFER



D. DATA BUS VALID TIMING (D0-D07)