TECHNICAL PROPOSAL
COMPUTER FOR
SIMPLIFIED INERTIAL GUIDANCE SYSTEM

THE ELECTRONICS DIVISION OF GENERAL MOTORS CORPORATION

MILWAUKEE 1, WISCONSIN

TECHNICAL PROPOSAL

COMPUTER FOR SIMPLIFIED INERTIAL GUIDANCE SYSTEM

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AC SPARK PLUG
The Electronics Division
of
General Motors Corporation

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SECTION I

INTRODUCTION

The guidance computer for the Simplified Inertial Guidance System (SIGS) is an advanced airborne guidance and steering computer using the latest techniques and devices commensurate with high reliability, performance, availability, and low costs. The SIGS computer is a special-purpose, digital, high-speed machine using a unique hybrid incremental and whole number computing technique.

Figure 1-1 shows a cutaway drawing of the SIGS computer that has been designed to perform the steering and guidance function for short-range missiles. The prototype computer weighs six pounds, occupies less than 0.1 cubic foot, and consumes 16 watts of power. The production version has the same weight and volume characteristics but will only consume eight watts of power because of the use of lower power integrated circuit elements. Power can be supplied either by a battery pack or by a compatible power supply packaged in a modular fashion.

Among the unique design features for this computer are: the use of glass delay lines for its memory, complete logical implementation by molecular integrated circuits, and modular packaging concepts that readily adapt a basic computer package to a variety of missions and applications.

In Figure 1-2, an exploded view of the prototype computer illustrates the simplicity of design. The two center sections shown are the top and bottom portions of the structure, which contain the glass delay lines, memory electronics, interface circuitry, oscillators, and power regulators. The integrated circuits are mounted on multilayer interconnection boards held by frames, as shown at both sides of the center sections.

The SIGS computer results from an extensive study by the Computer Research and Development Laboratory within AC Spark Plug of the special problems of tactical missile guidance. A prototype of this computer is currently being fabricated within the Research and Development Laboratory. Integration and checkout of this computer will commence during the first quarter of 1964. A mechanical test model of the computer will undergo testing in January 1964 and will be subjected to environmental conditions equal to or greater than those specified for the SIGS computer.

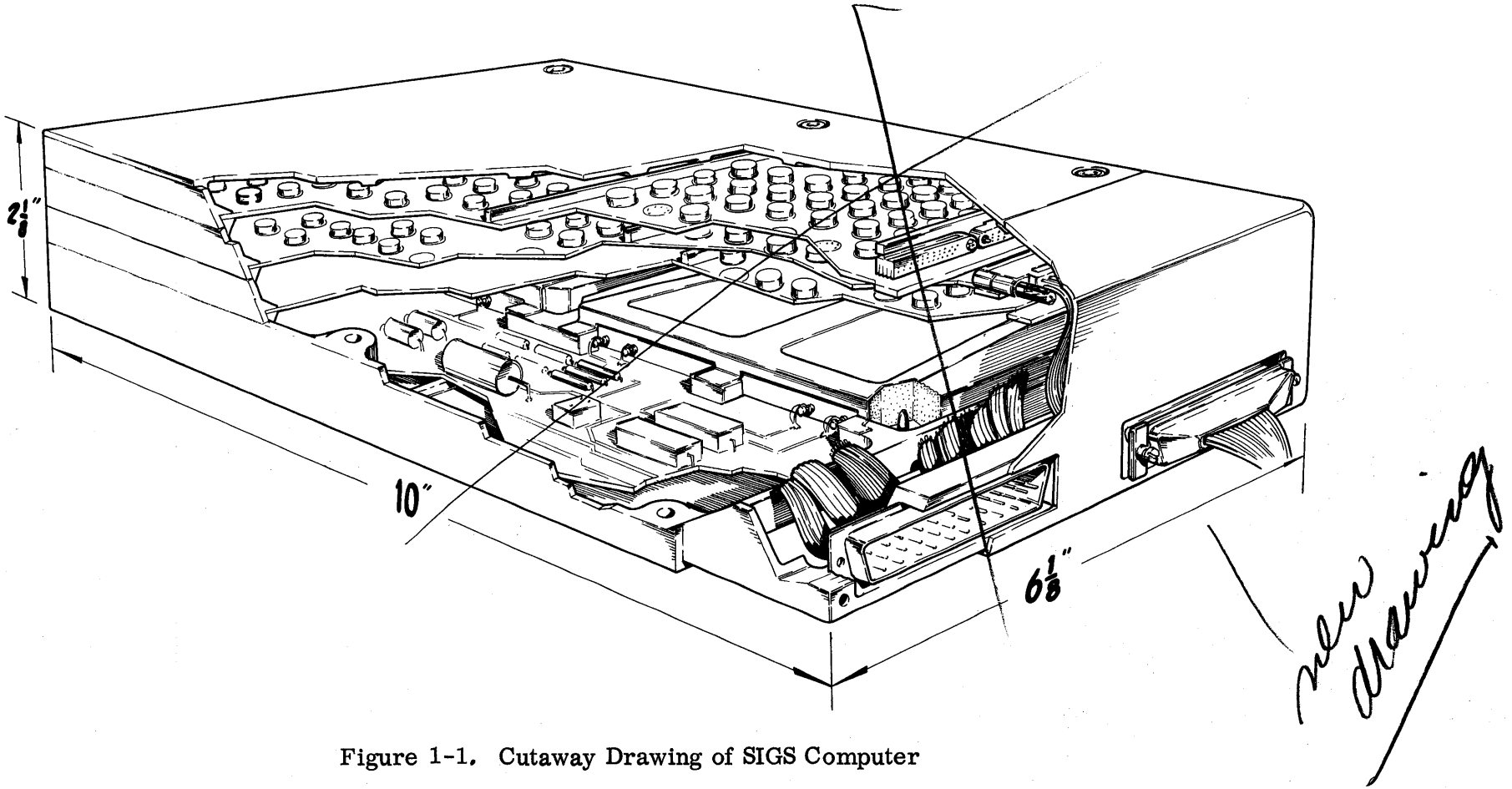

Figure 1-1. Cutaway Drawing of SIGS Computer

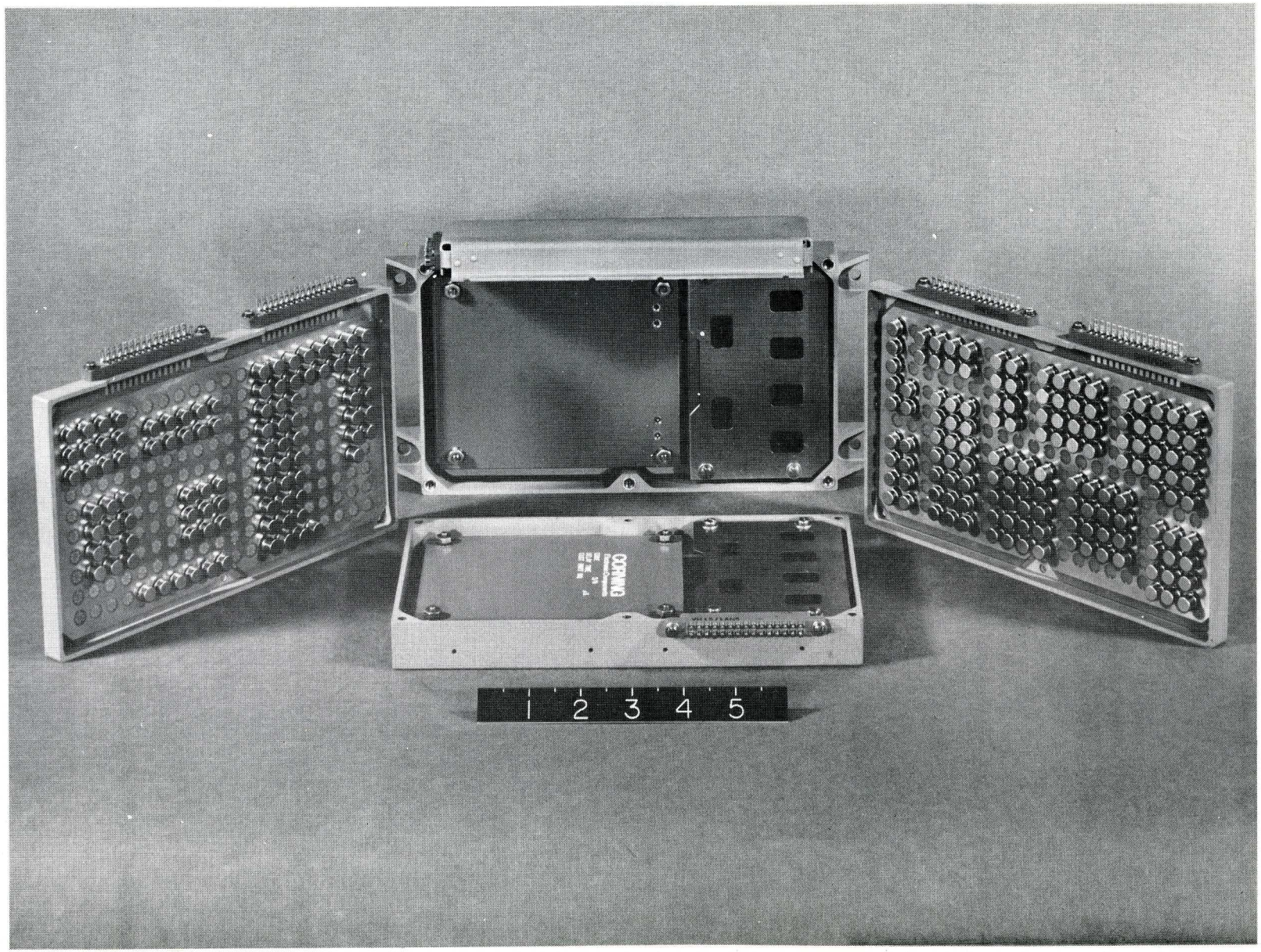

Figure 1-2. Exploded View of the SIGS Prototype Computer

SECTION II

COMPUTER FUNCTIONAL REQUIREMENTS *

2.1 System Equations

The guidance and steering computer receives inputs from the three accelerometers of a stabilized platform, performs the necessary navigation and steering calculations, and transmits two steering signals to the missile autopilot. In addition, arming and fusing of the warhead are performed by the computer as a function of range-to-go and platform gimbal stop signals.

Guidance computations are performed continuously from launch in order to provide information which is necessary for steering computations.

The steering function is performed in two phases. During the first, or boost, phase the computer output to the autopilot is zero in the cross-range direction and is a constant pitch rate in the down range direction. Thus, the boost phase is performed open loop. This phase is expected to have a fixed duration for missile ranges of 17 to 50 miles, and cutoff is not commanded by the computer. During the second or terminal flight phase the computer assumes a more active role and performs cross-product steering to guide the missile to the burst or impact point. It is anticipated that there will be no sustainer engine and that directional control will be achieved by means of aerodynamic surfaces.

The manipulation within the pitch plane is illustrated, for a given trajectory, by Figure 2-1. The pitch plane guidance consists of two phases: an initial, open-loop constant-pitch-rate phase, and a terminal, closed-loop cross-product-steering phase. The open-loop phase occurs during the powered portion of the flight and orients the missile in position and velocity such that with a fixed burn time targets within 17 to 50 nm can be accommodated. The effect of the terminal guidance is to force the missile velocity to be along the range-to-go vector. Changes in pitch are commanded at a rate proportional to the cross product of the velocity vector with the range-to-go vector.

The intent of the yaw guidance is to keep the missile in the pitch plane throughout the flight. Figure 2-2 depicts a trajectory projected onto the launch point tangent plane which has acquired a crossrange displacement and potential displacements; both, however, are subsequently nulled. It should be noted that the proposed guidance scheme steers the missile in a non-ballistic trajectory.

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*The missile system requirements described in this Section and the mechanization description in Section III of this proposal were received from Lockheed Missile and Space Company as part of an independent joint development effort with Lear Siegler, Inc. on the Diverse Missile Guidance System. These are included for completeness.

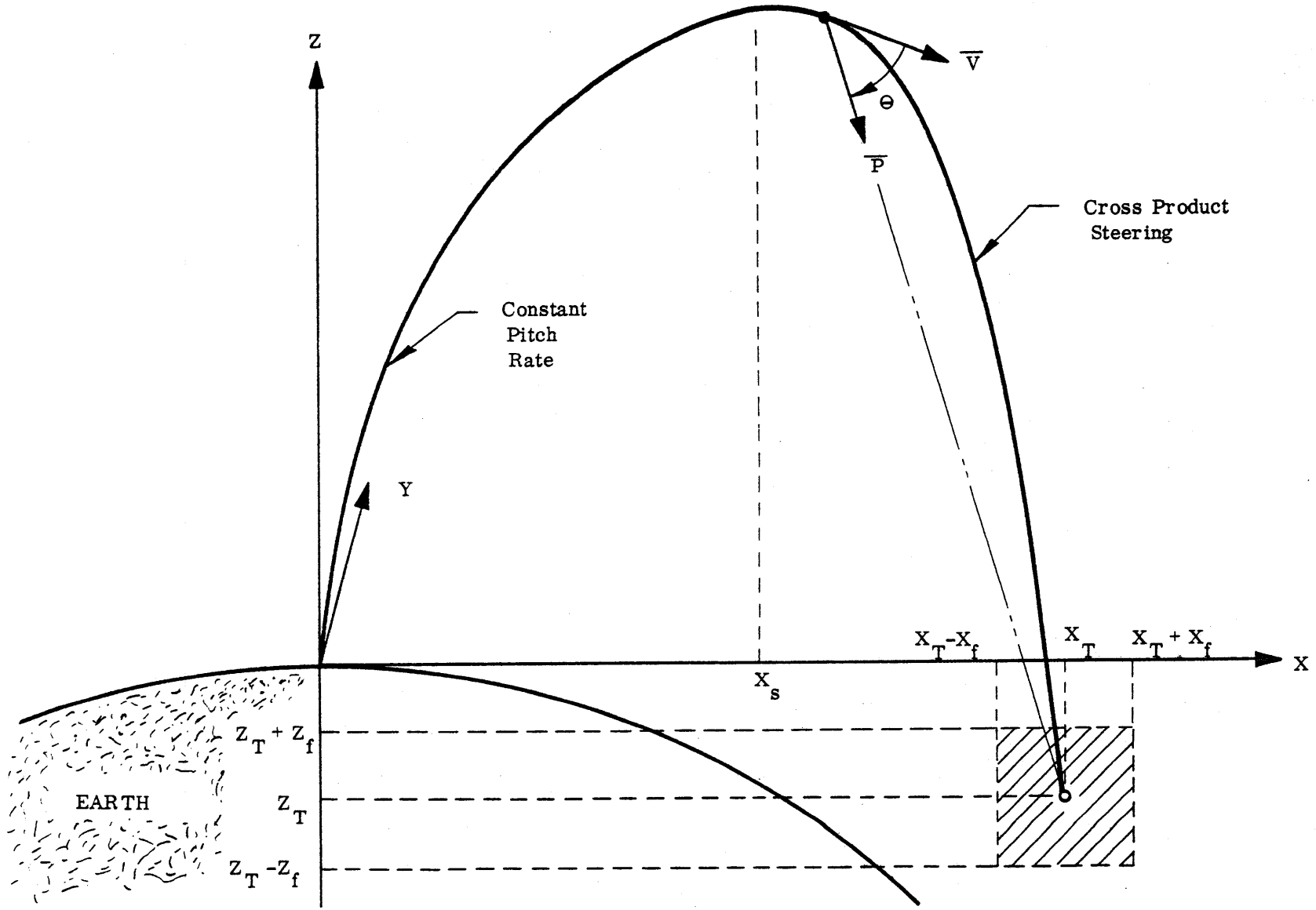


Figure 2-1. Pitch Plane Missile Trajectory

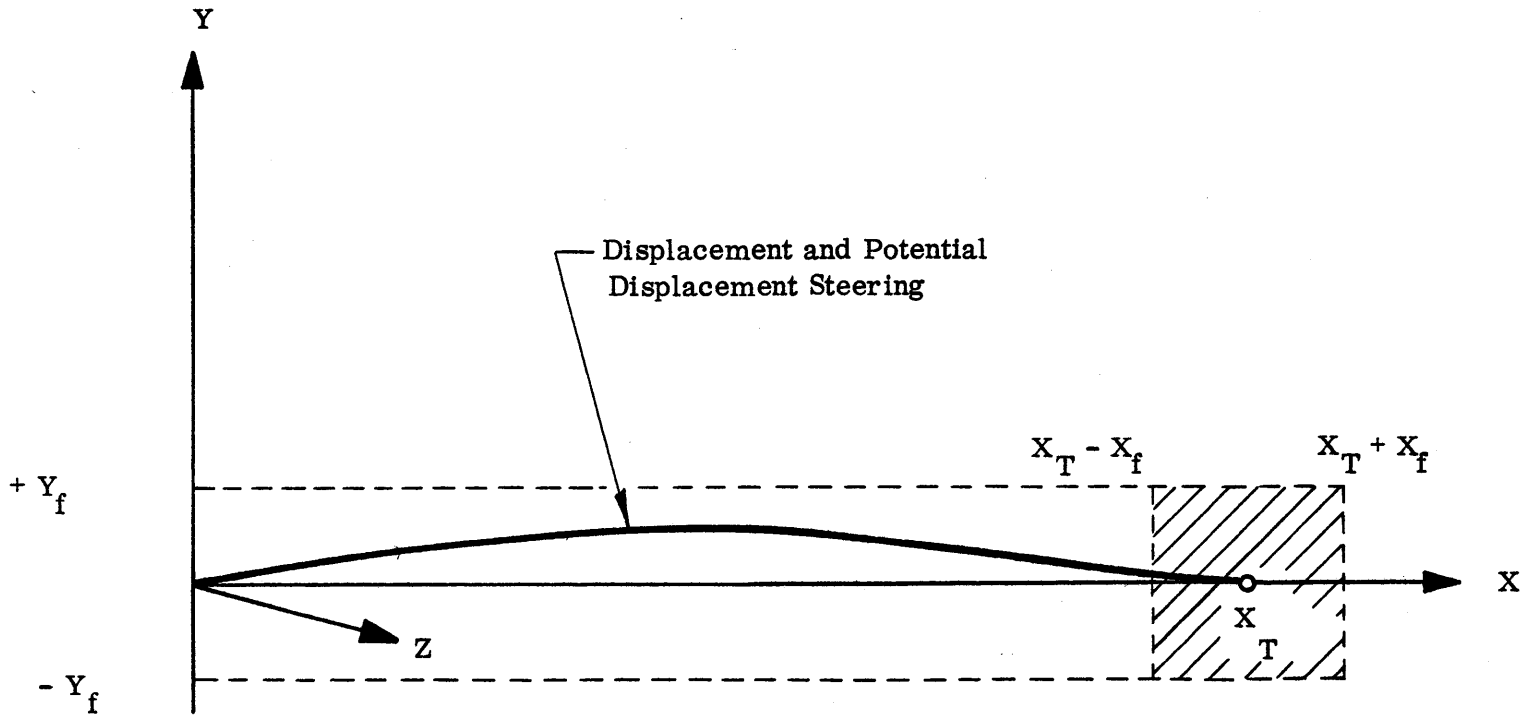


Figure 2-2. Yaw Plane Missile Trajectory

2.1.1 Coordinate Systems

The coordinate system is fixed with respect to the earth and rotates at earth rate. Three accelerometers are mounted on an inertially stabilized platform and the sensitive axes of these instruments define the coordinate system axes.

a. The X axis is down range, positive toward the target.

b. The Y axis is cross range, positive to the left.

c. The Z axis is vertical at launch point, positive up.

d. The X and Y axes define a plane which is horizontal at launch point.

e. The X and Z axes define the pitch plane which contains the launch point, the offset target point, and the center of the earth. An ideal missile trajectory would lie wholly on the pitch plane.

2.1.2 Velocity Computations

The velocity equations are summations of the changes in velocity as indicated by the accelerometer inputs along the three axes, and are as follows:

a. X-Axis

$$V_x = V_{xi} + \Sigma \Delta V_x$$

b. Y-Axis

$$V_y = V_{yi} + \Sigma \Delta V_y$$

c. Z-Axis

$$V_z = V_{zi} + \Sigma \Delta V_z - \Sigma g_n \cdot \Delta t$$

where V_{xi}, V_{zi}, and V_{yi} are initial values of velocity, g_n is the acceleration due to gravity (assumed constant) and Δt is the computer iteration time.

2.1.3 Position Equations

The equations which determine the missile's present position in X, Y, and Z are as follows:

a. $X = \Sigma V_x \cdot \Delta t$

b. $Y = \Sigma V_y \cdot \Delta t$

c. $Z = \Sigma V_z \cdot \Delta t$

2.1.4 Steering Commands

Computer generated steering commands are limited to missile pitch and yaw axes. It is assumed that the missile is restrained from rolling by a separate stabilization loop in the autopilot.

The target location is designated as X_T, Y_T, Z_T. The positional target quantities contained in the computer must have been adjusted for the earth's rotation during missile flight time, and for the burst height desired.

The equation which generates the pitch rate command ($\dot{\theta}_c$) is

$$\dot{\theta}_c = K_B \qquad \text{for } X < X_s$$

$$\dot{\theta}_c = K_T \{ (Z_T - Z) V_X - (X_T - X) V_z \} \qquad \text{for } X \geq X_s,$$

where K_B is a constant determined by the missile dynamics. K_T is approximately the reciprocal of the range to go, and is calculated according to the following:

$$K_T = \frac{C_0}{\rho} + C_1 + C_2\rho + C_3\rho^2 + C_4\rho^3 + C_5\rho^4,$$

where:

$\rho = (X_T - X)$ if $|X_T - X| > |Z_T - Z|$ and if $(X_T - X)$ is positive, or

$\rho = -(X_T - X)$ if $|X_T - X| > |Z_T - Z|$ and if $(X_T - X)$ is negative, or

$\rho = (Z_T - Z)$ if $|Z_T - Z| > |X_T - X|$,

$C_0, C_1, C_2, C_3, C_4, C_5$ are system gain constants.

The equation which generates the yaw command is:

$$\psi_c = K_L Y + K_N V_y$$

where K_L, K_N are the yaw system gain constants.

2.1.5 Fusing and Arming

Fail-safe control signals are generated by the computer for arming and fusing the warhead. Issuance of these signals is dependent upon achieving a certain range to go and on satisfactory guidance system operation as indicated by the inertial platform gimbals not having hit certain preset stops.

The conditions for arming are $\left| X_T - X \right| < X_a$ and $\left| Y \right| < Y_a$, and gimbals have not hit stops.

The conditions for fusing are $\left| X_T - X \right| < X_f$ and $\left| Y \right| < Y_f$, and gimbals have not hit stops.

2.2 Interface

In Tables 2-1 and 2-2 definitions of the computer input and output signals are shown. The computer accepts inputs from the three platform accelerometers in the form of pulse trains and outputs two dc voltages for the pitch rate and yaw commands to the autopilot. In addition to these signals, discrete inputs are received from the gimbal stop contacts, and two discrete outputs are sent to the missile warhead for arming and fusing functions. The iteration pulse from the computer is sent to the pulse torque restrained pendulous accelerometer electronics. Signals required for loading information and for monitoring during the sled or flight test are not shown but will be added as better definition for the instrumentations is received.

2.3 Digital Mechanization Error

This section deals with the errors generated by the digital computer in processing the SIGS navigation and guidance and steering equations. The computer equations used as a basis for the error analysis are given in Figure 2-3.

The SIGS computation involves: (1) the integration of a system of ordinary differential equations to get present position, and (2) steering computations for pitch rate and cross range corrections. The differences in computed present position and known target coordinates are used to compute steering information. Errors in computed present position will be translated directly as miss error. Present position computational errors are introduced each computer iteration, and these errors can accumulate for the duration of the mission. The effects of these errors can be isolated and accounted for separately.

The effect of errors in the steering computation cannot be accurately assessed because the missile dynamic characteristics are not known. Computer generated errors in the steering computations are generally small and will not significantly contribute to total guidance error for the following two reasons. First, steering

Name	Source	Source Element	Load Element	Range	Resolution	Scale Factor	Notes
X-axis Change of Velocity (ΔVx)	Converter	Gate	Input Buffer	$\pm$10 g's	0.16 feet per second	1 pulse =0.16 feet per second	Sign is determined by the state of second wire.
Y-axis Change of Velocity (ΔVy)	Converter	Gate	Input Buffer	$\pm$2 g's	0.16 feet per second	1 pulse = 0.16 feet per second	Sign is determined by the state of second wire.
Z-axis Change of Velocity (ΔVz)	Converter	Gate	Input Buffer	$\pm$10 g's	0.16 feet per second	1 pulse = 0.16 feet per second	Sign is determined by the state of second wire.
Gimbal and Stop Contact (STP)	Inertial Platform	Contact Relay or Micro-switch	Input Buffer	Not Appli-cable	Not Appli-cable	Not Appli-cable	

Table 2-1. Computer Input Definition

Name	Source Element	Load	Load Element	Range	Resolution	Scale Factor	Notes
Command Pitch Rate ($\dot{\Theta}_c$)	Kirchoff Adder	Autopilot	Operational Amplifier	±3.75 degrees per second	0.0586 degrees per second	6 volts = 3.75 degrees per sec	Load should be greater than or equal to 5K ohms.
Command Yaw (ψ_c)	Kirchoff Adder	Autopilot	Operational Amplifier	±10 degrees	0.156 degrees	6 volts = 10 degrees	Load should be greater than or equal to 5 K ohms.
Iteration Pulse (IP)	Output Buffer	Converter	Gate	Not Applicable	Not Applicable	Not Applicable	
Warhead Arm (ARM)	Output Buffer	Warhead	Unknown	Not Applicable	Not Applicable	Not Applicable	
Warhead Fuse (FUS)	Output Buffer	Warhead	Unknown	Not Applicable	Not Applicable	Not Applicable	

Table 2-2. Computer Output Definition

information is recomputed from present position information each iteration time so that errors do not accumulate from previous iterations in the same manner as present position. Second, the closed-loop nature of its steering computation is such that its error will be below the uncertainties associated with the autopilot and missile dynamics.

Most errors involved in a digital computation can be classified as either truncation or round-off errors. Truncation errors are present in the SIGS mechanization because of: (1) the difference equations used for integration, (2) the use of an average value for the gravity function, and (3) the approximating function for the reciprocal of "range-to-go" in the cross product steering computation. Round-off errors are present in the SIGS system because of the finite word length in the computer. In determining the computer-generated errors for SIGS, round-off errors and only truncation errors involved in the integration procedure will be considered. The truncation errors in (2) and (3) above are not due to the computer mechanization.

Finally there is the effect of transport lag upon accuracy. Transport lag affects present position accuracy only very slightly because of the high iteration rate. Because of the manner in which a division is performed in the steering computation, the effect of transport lag has been examined in detail for that operation.

Table 2-3 is a summary of the SIGS computer-generated errors for a typical mission. These errors are based upon a mission having the following characteristics.

a. Duration of trajectory: 100 seconds

b. Acceleration: 10g maximum down range,
2g maximum cross range

c. Velocity of missile at the target: 1000 ft/sec downrange.

2.3.1 Error Analysis

Computer-generated errors involve truncation, round-off, and transport lag errors. Truncation errors due to numerical integration can be bounded for each integration step using the known error function associated with the method, and they can be bounded for an entire trajectory by assuming worst case accumulation of the error at each step. Integrations are performed using a difference equation of the form

TOTAL PRESENT POSITION ERROR AT TARGET			
	DOWN RANGE	CROSS RANGE	ALTITUDE
Integration truncation error			
Worst case upper bound	16 ft	3.2 ft	16 ft
Round-off			
Worst case upper bound	16 ft	16 ft	32 ft
Transport lag			
Worst case upper bound	1 ft	.1 ft	1 ft

Table 2-3 Summary of SIGS Computer Generated Errors for 100 sec, 10g Mission

VELOCITY AND PRESENT POSITION

$$V_{xk} = V_{xI} + \sum_{j=1}^{k} \Delta V_{xj}$$

$$V_{yk} = V_{yI} + \sum_{j=1}^{k} \Delta V_{yj}$$

$$V_{zk} = V_{zI} + \sum_{j=1}^{k} (\Delta V_{zj} - \Delta V_{gj})$$

$$\Delta V_{gj} = g_n \Delta t$$

$$(X_T - X)_k = X_T - \sum_{j=1}^{k} V_{xj} \Delta t$$

$$(Z_T - Z)_k = Z_T - \sum_{j=1}^{k} V_{zj} \Delta t$$

$$Y_k = \sum_{j=1}^{k} V_{yj} \Delta t$$

STEERING COMPUTATIONS

$$K_{Tk} = \sum_{j=1}^{k} [C_0 \Delta \left(\frac{1}{\rho}\right)_j + \Delta(C_1 + C_2\rho + C_3\rho^2 + C_4\rho^3 + C_5\rho^4 + C_6\rho^5)_j]$$

$$[(Z_T - Z)\, V_x]_k = \sum_{j=1}^{k} [(Z_T - Z)_j\, \Delta V_{xj} + V_{xj} \Delta (Z_T - Z)_j]$$

$$[(X_T - X)\, V_z]_k = \sum_{j=1}^{k} [(X_T - X)_j\, \Delta V_{zj} + V_{zj} \Delta (X_T - X)_j]$$

$$\dot{\Theta}_{ck} = \sum_{j=1}^{k} \Delta \{ K_T (Z_T - Z)\, V_x - K_T (X_T - X)\, V_z \}_j$$

$$= \sum_{j=1}^{k} \{ K_{Tj} \Delta [(Z_T - Z)_j\, V_{xj}] + (Z_T - Z)_j\, V_{xj} \Delta K_{Tj}$$

$$- K_{Tj} \Delta [(X_T - X)_j\, V_{zj}] - (X_T - X)_j\, V_{zj}\, \Delta K_{Tj} \}$$

$$\psi_{ck} = K_L Y_k + K_M V_{yk}$$

Figure 2-3 SIGS Computer Equations

$$U_{n+1} = U_n + \dot{U}_n \Delta t$$

Using this integration procedure introduces an error at each step given by

$$E_{un} = \frac{1}{2} \Delta t^2 \ddot{U} \ (t_n + \alpha \Delta t). \qquad 0 \leq \alpha < 1$$

An upper bound on E_{un} is therefore

$$\left| E_{un} \right| \leq \frac{1}{2} \Delta t^2 \left| \ddot{U} \right|_{max}.$$

And, if this procedure is applied repeatedly for N steps, a pessimistic upper bound for accumulated truncation error is

$$\left| \bar{E}_u \right| \leq \frac{1}{2} N \Delta t^2 \left| \ddot{U} \right|_{max}.$$

The various computer quantities are subject to round-off error because of finite word length. Let W_v be the weight of the least significant bit of the result v generated in a computer operation. Then if the computer operation is chopped, an upper bound on the round-off error, R_{vj}, for that operation is W_v. If the operation is performed N times then the total accumulated round-off error is bounded; i.e., $|R_v| < NW_v$. Obtaining the total accumulated round-off errors in this manner leads to a pessimistic bound for the error. For round-off errors generated in an application such as SIGS, it is generally safe to assume that round-off errors are random variables distributed uniformly and that their accumulation is also random. Consequently, a statistical analysis would yield error estimates somewhat less than the pessimistic upper bounds.

Transport lag error (L) in SIGS can be handled very simply for any variable U by use of:

$$\left| L_u(t) \right| \leq \left| \dot{U}(t) \right| \ \delta t \leq \left| \dot{U} \right|_{max} \Delta t$$

where δt is transport lag time and Δt is iteration time.

The one exception is the division procedure to obtain the reciprocal of ρ in cross product steering. The division is mechanized by the following algorithm. Let Q_n be a trial quotient for the n^{th} iteration. The product ρQ_n is formed. If $\rho Q_n \geq 1$, then

$Q_{n+1} = Q_n - 1$; whereas if $\rho Q_n < 1$ then $Q_{n+1} = Q_n + 1$, where 1 is a one in the least significant bit position of Q. This algorithm for division will result in a lag as ρ gets close to zero. To evaluate this effect the differential of $1/\rho$ is

$$\Delta(\frac{1}{\rho}) = -\frac{1}{\rho^2}\frac{d\rho}{dt}\Delta t.$$

Transport lag error occurs when the change $\Delta(1/\rho)$ becomes greater than the least significant bit of Q in one iteration. In the SIGS mechanization the least significant bit position of $1/\rho$ has a weight of approximately 0.2×10^{-5} feet. Assuming a terminal velocity $d\rho/dt$ of 1000 ft/sec, and an iteration time Δt of 10^{-3} second, and solving for ρ it turns out that transport lag does not enter into this operation until ρ reaches the value

$$\rho = [\frac{d\rho}{dt}\frac{\Delta t}{\Delta(\frac{1}{\rho})}]^{1/2} \approx 700 \text{ ft.}$$

2.3.2 Present Position Errors

Computations for down range and cross range velocities consist of summing velocity increments. Because the summing is done without error the computed velocities are always in agreement with measured velocity to within at least one pulse (0.16 ft/sec). For the vertical velocity computation, additional error is introduced by the gravity computation due to round-off. However, due to the manner of mechanization, the total error in vertical velocity due to the gravity computation never exceeds 0.16 ft/sec, the same weight assigned to velocity increments. Consequently, vertical velocity errors are greater. Velocity errors are summarized in the following table.

Maximum Errors at any Time

Down range velocity	0.16 ft/sec
Cross range velocity	0.16 ft/sec
Vertical velocity	0.32 ft/sec

These errors are carried forward as round-off errors in the integration for present position described next.

Truncation errors in present position are given by the formula

$$\bar{E}_u \leq \frac{1}{2}N\Delta t^2 \ddot{U}_{max} = \frac{T}{2}\Delta t \ddot{U}_{max}$$

where $\tau = N\Delta t$ is total mission time in seconds. The table below shows the total truncation errors for various mission times and accelerations using an iteration time of 1 ms.

τ(sec)	A_x max	A_y max	A_z max	E_x(ft)	E_y(ft)	E_z(ft)
100	10g	2g	10g	16	3.2	16
100	20g	4g	20g	32	6.4	32
200	10g	2g	10g	32	6.4	32
200	20g	4g	20g	64	12.8	64

Table 2-4. Truncation Errors

Round-off errors in present position are derived from the errors in velocity discussed earlier, and these errors are summarized in the following table assuming an iteration interval of 1 ms.

τ(sec)	WORST CASE (ft)		
	R_x	R_y	R_z
100	16	16	32
200	32	32	64

NOTE: $R_{xj} = R_{yj} = 0.16 \times 2^{-10}$ ft

$R_{zj} = 0.32 \times 2^{-10}$ ft

} Round-off errors per iteration

Table 2-5. Round-off Errors

Finally, errors in present position due to transport lag are very simply determined. Assuming a terminal velocity of 1000 ft/sec and an iteration interval of 1 ms, the error introduced due to transport lag is no more than 1 foot which is negligible compared to other errors.

SECTION III

COMPUTER ORGANIZATIONAL DESIGN

3.1 Design Philosophy

The SIGS computer requirements described in the RFP define guidance and steering as separate functions. However, the nature of digital mechanization is such that inefficiencies result when two separate devices are mechanized to perform these functions because the task of each is then very limited. For this reason, the SIGS computer is designed to perform the combined guidance and steering functions.

The design of this computer is based on a hybrid of incremental and whole word techniques which perform the algebraic operations on information stored in a serial dynamic memory. A glass memory, schematically represented in Figure 3-1 and described in Section IV, Paragraph 4.2, contains all the data words which it recirculates in a serial manner. The complexity of the control and arithmetic units is greatly reduced by restricting transfer of information, or updating of information, to operations such as incrementing, adding, and multiplying by either ONE or ZERO. Remaining within these constraints has greatly minimized design complexity.

The system equations, as shown in Section II, Paragraph 2.1, were solved by limiting the type of instructions to add, integrate, multiply, divide, and test. The add and integrate instructions are easily implemented with a serial adder. The multiplication process is a mechanization of the equation:

$$X \cdot Y = (X \text{ old} + \Delta X)\ (Y \text{ old} + \Delta Y)$$

If both the ΔX and ΔY quantities are correctly scaled, the product can be generated by two multiplications of a ZERO, or a plus or minus increment and two serial additions. Here scaling is critical to assure that the product does not unduly lag the multiplier and multiplicand.

The divide mechanization can be described as a trial and error method in which the divisor is multiplied by a trial quotient and the resultant product is compared with the dividend. The convergence of the divide mechanization is sensitive to the proper selection of scale factors on the increments, and on the rate at which the operation is performed. The test operation is mechanized by examining the sign of the sum after the variable quantity is compared with a given bound.

Detailed scaling on all quantities used for the guidance mechanization is shown in Paragraph 3.4.

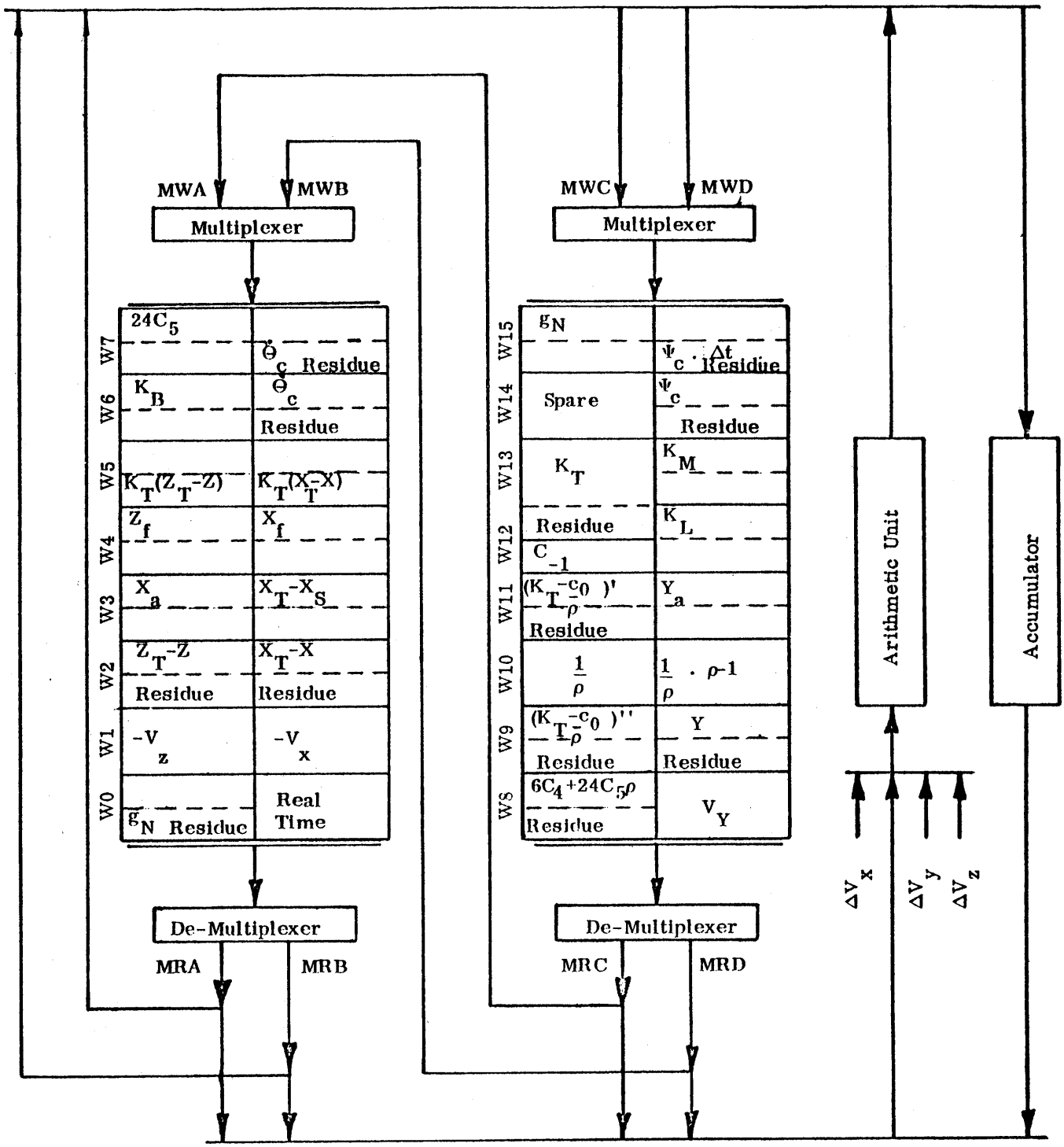


Figure 3-1. Data Storage and Computer Organization

3.2 Computer Organization

Figure 3-1 illustrates the computer organization; each block in the figure is related to a functional block. The two most prominent blocks are glass memories which provide the desired serial dynamic storage; both blocks are labeled to indicate the physical location of the stored quantities at the beginning of the memory's natural period. For example, Xa is available at "MRA" at word time three. The multiplexers are circuits which receive two streams of bits, interlace these two streams bit-by-bit, and transmit the resultant stream of bits at twice the bit rate at which it received the two original streams. The de-multiplexer performs the reverse process. The arithmetic unit is a two input serial adder which works into the twenty bit accumulator and the variable inputs to the multiplexer. The function of the accumulator and shift register, is to provide a variable delay. This variable delay is needed to alter one word as a function of another word that is not available immediately. Also, the accumulator provides the parallel transfer capability which enables an instantaneous updating of the hold register which, in turn, controls the digital-to-analog converter. An instantaneous updating capability is highly desirable because it eliminates jitter on the steering signals.

The dynamic memory will store 1,280 bits at an internal bit rate of 2,621,440 bits/sec. That is, a different bit will be inserted into the memory at the internal bit rate; further, each bit will come out the other end of the memory exactly 1/2048 seconds after it was inserted.

Note that the effect of the multiplexers, glass lines, and de-multiplexers is to provide two separate (but synchronized) memories, or a total of four data channels. The four channels are then connected such that there are two memories of sixteen words each with monitoring capabilities at the half-way point.

Time is kept by a set of counters which are clocked by the same precision source that is used to insert bits into the memory. This set of counters consists of a bit counter, a word counter, and a quadrant counter. The bit counter is a sequential binary counter of 40 states. When decoded, the bit counter specifies where a word begins and ends within the two serial streams of bits from the memory and the relative position of all the bits within the word. Also, the last state of the bit counter is the cue for the sixteen state word counter to advance.

When the word counter is decoded, it specifies words of 40 bits within each of the two serial streams of bits from the memory. Also, the last state of the word counter is the cue for the 4-state quadrant counter to advance.

The bit and word counters are sufficient to track all 1,280 bits, but the complexity of the updating procedure necessitates 4 complete passes, or iterations,

before all the algebraic operations can be accomplished; therefore, the quadrant counter is used to extend the sequence of the count to 5, 120 bit times. This implies that all information routing must be repetitive with a period of $1/2^9$ seconds or be conditional on something other than the state of the counter. In other words, the set of counters is the master controller of the entire digital operation.

3.3 Program Mechanization

The system equations are essentially "wired" into the interconnection of the logic elements, providing the most reliable means for storage of instructions. The wired nature of the program, however, necessitates rewiring if any changes to the instruction are required. In the SIGS computer design, this problem has been alleviated by packaging the interconnect boards in a manner such that the removal and replacement of the boards is greatly facilitated.

A method of updating stored data with the specified equipment has been determined and is shown in Tables 3-1a, b, c, and d. These four tables define the input to the accumulator and the two inputs to the glass memory which are not automatically recirculated.

Most of the symobls were defined in Section II, however, some additional comments are in order. During word time zero (Table 3-1a), the $g_n \cdot \Delta t$ term is generated by adding a constant to a residue at a constant rate, therefore, generating and detecting an overflow at a rate proportional to the constant. At word time four the input to the accumulator is conditional upon "ΔK_T", which can be in the ZERO or $\pm$ONE state. Therefore, the accumulator can be recirculated, multiplied by minus ONE, or ZEROed. Also, during word time ten, an input to the adder is gated by an incremental condition, as indicated for Memory Write Channel D. "TER" is a discrete signal indicative of the pitch plane steering phase.

3.4 Scaling

Table 3-2 is a specification of all increments used by the computer. Note that the sign and magnitude of each bit requires a storage element. Also, the bits must be used before the storage element is reset; the logical equations are somewhat complicated by this consideration. In some cases, redundant storage is required to achieve the desired units for a given increment. The resultant unit, or scale factor, of each increment is listed under the "Weight" column; the "Maximum Rate" column specifies the maximum rate at which the storage element may change state.

Figures 3-2a and b illustrate computer operation, except that they do not reflect the serial nature of the machine. They do, however, clearly illustrate the dual role some registers play, that is, the lower order portion of a register can be used to accumulate a value that is less than an increment, and the higher order portion automatically sums a spill or overflow. This dual role is a unique design feature of the SIGS computer, resulting in an added feature of design flexibility. For example, multi-state increments up to and including whole words can be inexpensively implemented.

PROGRAM

WORD TIME	ITERATION QUAD ZERO		
	Accumulator	Memory Write Channel C	Memory Write Channel D
0		$Acc + g_n \cdot \Delta t$ Residue	$t + \Delta t$
1	$-(V_z + \Delta V_z - g_n \cdot \Delta t)$	$-(V_z + \Delta V_z - \Delta g_n)$	$V_x + \Delta V_x$
2	$Acc + (Z_T - Z)$	$Acc + (Z_T - Z)$	$X_T - X$
3	Acc	X_a	$X_T - X_S$
4	$Acc \xrightarrow{\Delta K_T}$	Z_f	X_f
5	$Acc + K_T (Z_T - Z)$ $\xrightarrow{\Delta 4Vx}$	$Acc + K_T (Z_T - Z)$	$K_T (X_T - X)$
6	$K_B \xrightarrow{\overline{TER}}$, $Acc + \dot{\Theta}_C \xrightarrow{TER}$	K_B	$Acc + \dot{\Theta}_C$
7	$24C_5 \xrightarrow{\Delta\rho}$	$24C_5$	$Acc + \dot{\Theta}_C$ Residue
8	$6C_4 + 24C_5 \cdot \rho \xrightarrow{\Delta\rho}$	$Acc + (6C_4 + 24C_5\rho)$	$V_y + \Delta V_y$
9	$2C_3 + 6C_4\rho + 12C_5\rho^2 \xrightarrow{\Delta\rho}$	$Acc + (2C_3 + 6C_4\rho + 12C_5\rho^2)$	Y
10	Acc	$\frac{1}{\rho} + \Delta(\frac{1}{\rho})$	$(\frac{1}{\rho} \cdot \rho - 1) + \rho\, \Delta \frac{1}{\rho}$
11	$C_2 + 2C_3\rho + 3C_4\rho^2 + 4C_5\rho^3$ $\xrightarrow{\Delta\rho}$	$Acc + (C_1 + 2C_2\rho + 3C_3\rho^2 + 4C_4\rho^3)$	Y_a
12	$Acc + C_0 \cdot \Delta \frac{1}{\rho}$	C_0	K_L
13		$Acc + K_T$	K_M
14	ψ_c		ψ_c
15	g_n	g_n	$Acc + \psi_c \cdot \Delta t$ Residue

Figure 3-2a. Program Specification

Word Time	ITERATION QUAD ONE		
	Accumulator	Memory Write Channel C	Memory Write Channel D
0		$Acc + g_n \cdot \Delta t$ Residue	$t + \Delta t$
1	$-(V_x + \Delta V_x)$	$-(V_z + \Delta V_z - \Delta g_n)$	$V_x + \Delta V_x$
2	$Acc + (X_T - X)$	$Z_T - Z$	$Acc + (X_T - X)$
3	Acc	X_a	$X_T - X_S$
4	$Acc \xrightarrow{\Delta K_T}$	Z_f	X_f
5	$Acc + K_T (X - X_T) \xrightarrow{\Delta 4V_z}$	$K_T (Z_T - Z)$	$Acc + K_T(X_T - X)$
6	$K_B \xrightarrow{\overline{TER}}$, $Acc + \dot{\Theta}_c \xrightarrow{TER}$	K_B	$Acc + \dot{\Theta}_c$
7		$24C_5$	$Acc + \dot{\Theta}_c$ Residue
8	$V_y + \Delta V_y$	$6C_4 + 24C_5\rho$	$V_y + \Delta V_y$
9		$2C_3 + 6C_4\rho + 12C_5\rho^2$	Acc + Y
10		$\frac{1}{\rho}$	$(\frac{1}{\rho} \cdot \rho - 1) + \frac{1}{\rho} \Delta\rho$
11		$C_2 + 2C_3\rho + 3C_4\rho^2 + 4C_5\rho^3$	Y_a
12	$A_{cc} + K_L (4\Delta V_y)$	C_0	K_L
13	$A_{cc} + K_M (\Delta Y)$	K_T	K_M
14	$Acc + \psi_c$		$Acc + \psi_c$
15	g_n	g_n	$Acc + \psi_c \cdot \Delta t$ Residue

Figure 3-2b. Program Specification

Word Time	ITERATION QUAD TWO		
	Accumulator	Memory Write Channel C	Memory Write Channel D
0		$Acc + g_n \cdot \Delta t$ Residue	$t + \Delta t$
1	$-(V_z + \Delta V_z - \Delta g_n)$	$-(V_z + \Delta V_z - \Delta g_n)$	$V_x + \Delta V_x$
2	Acc	$Acc + (Z_T - Z)$	$X_T - X$
3	Acc	X_a	$X_T - X_S$
4	Acc $\xrightarrow{\Delta[K_T (X_T - X)]}$	Z_f	X_f
5	Acc	$K_T(Z_T - Z) + K_T\Delta(Z_T - Z)$	$K_T(X_T - X)$
6	$K_B \xrightarrow{\overline{TER}}$, $Acc + \dot{\Theta}_C \xrightarrow{TER}$	K_B	$Acc + \dot{\Theta}_C$
7	$24C_5 \xrightarrow{\Delta\rho}$	$24C_5$	$Acc + \dot{\Theta}_C$ Residue
8	$6C_4 + 24C_5\rho \xrightarrow{\Delta\rho}$	$Acc + (6C_4 + 24C_5\rho)$	$V_y + \Delta V_y$
9	$2C_3 + 6C_4\rho + 12C_5\rho^2 \xrightarrow{\Delta\rho}$	$Acc + (2C_3 + 6C_4\rho + 12C_5\rho^2)$	Y
10	Acc	$\frac{1}{\rho} + \Delta(\frac{1}{\rho})$	$(\frac{1}{\rho} \cdot \rho - 1) + \rho\Delta\frac{1}{\rho}$
11	$C_2 + 2C_3\rho + 3C_4\rho^2$ $4C_5\rho^3 \xrightarrow{\Delta\rho}$	$Acc + (C_2 + 2C_3\rho + 3C_4\rho^2 + 4C_5\rho^3$	Y_a
12	$Acc + C_0 \cdot \Delta\frac{1}{\rho}$	C_0	K_L
13		$Acc + K_T$	K_M
14	ψ_c		ψ_c
15	g_n	g_n	$Acc + \psi_c \cdot \Delta t$ Residue

Figure 3-2c. Program Specification

Word Time	ITERATION QUAD THREE		
	Accumulator	Memory Write Channel C	Memory Write Channel D
0		Acc + g_n Residue	$t + \Delta t$
1	$V_X + \Delta V_X$	$-(V_z + \Delta V_z - \Delta g_n)$	$V_x + \Delta V_x$
2	Acc	$Z_T - Z$	Acc + $(X_T - X)$
3	Acc	X_a	$X_T - X_S$
4	Acc $\xrightarrow{\Delta [K_T(Z_T - Z)]}$	Z_f	X_f
5	Acc	$K_T (Z_T - Z)$	$K_T(X - X_T) + K_T \Delta(X_T - X)$
6	$K_B \overline{TER}$, Acc + $\dot{\Theta}_C$ TER	K_B	Acc + $\dot{\Theta}_C$
7		$24C_5$	Acc + $\dot{\Theta}_C$ Residue
8	$V_y + \Delta V_y$	$6C_4 + 24C_5\rho$	$V_y + \Delta V_y$
9		$2C_3 + 6C_4\rho + 12C_5\rho^2$	Acc + Y
10		$\frac{1}{\rho}$	$(\frac{1}{\rho} \cdot \rho - 1) + \frac{1}{\rho} \Delta\rho$
11		$C_2 + 2C_3\rho + 3C_4\rho^2 + 4C_4 P^3$	Y_a
12	Acc + $K_L (4\Delta V_y)$	C_0	K_L
13	Acc + $K_M (\Delta Y)$	K_T	K_M
14	Acc + Ψ_C		Acc + Ψ_C
15	g_n	g_n	Acc + $\Psi_C \cdot \Delta t$ Residue

Figure 3-2d. Program Specification

Name	Allowed States	Weight	Maximum Rate	Source	Destination
ΔV_X	0, $\pm$ 1	0.16 ft./sec	2,000/sec	X-Axis Accel	V_X
ΔV_Y	0, $\pm$ 1	0.16 ft./sec	2,000/sec	Y-Axis Accel	V_y
ΔV_z	0, $\pm$ 1	0.16 ft./sec	2,000/sec	Z-Axis Accel	V_z
ΔK_T	0, $\pm$ 1	2^{-12}/320 ft.	500/sec	K_T	$K_T(Z_T-Z)$, $K_T(X_T-X)$
$\Delta (X_T-X)$	0, $\pm$ 1	10 ft.	500/sec	X_T-X	$K_T(X_T-X)$
$\Delta (Z_T-Z)$	0, $\pm$ 1	10 ft.	500/sec	Z_T-Z	$K_T(Z_T-Z)$
ΔY	0, $\pm$ 1	10 ft.	1000/sec	Y	ψ_c
$\Delta K_T(X_T-X)$	0, $\pm$ 1	$\frac{1}{64}$ ft/ft	500/sec	$K_T(X-X_T)$	$\dot{\Theta}_c$
$\Delta K_T(Z_T-Z)$	0, $\pm$ 1	$\frac{1}{64}$ ft/ft	500/sec	$K_T(Z_T-Z)$	$\dot{\Theta}_c$
$\Delta 4 V_X$	0, $\pm$ 1	.64 ft/sec	500/sec	V_x	O_c
$\Delta 4 V_z$	0, $\pm$ 1	.64 ft/ sec	500/sec	V_z	$\dot{\Theta}_c$
$\Delta 4 V_y$	0, $\pm$ 1	.64 ft/sec	1000/sec	V_y	ψ_c
$\Delta 1/\rho$	$\pm$ 1	$\frac{2^{-14}}{320}$	1000/sec	$\rho(\frac{1}{\rho}) - 1$	K_T
$g_N \Delta t$	$\pm$ 1	0.16 ft/sec	2000/sec	g_N Residue	V_z
Θ_c	$\pm$ 1	0.001825^o	2000/sec	Θ_c Residue	Dig/Anal. Converter
$\psi_c \Delta t$	$\pm$ 1	0.005^o sec	2000/sec	$\psi_c \cdot \Delta t$ Residue	Dig/Anal. Converter

Table 3.2. Program Scale Factor

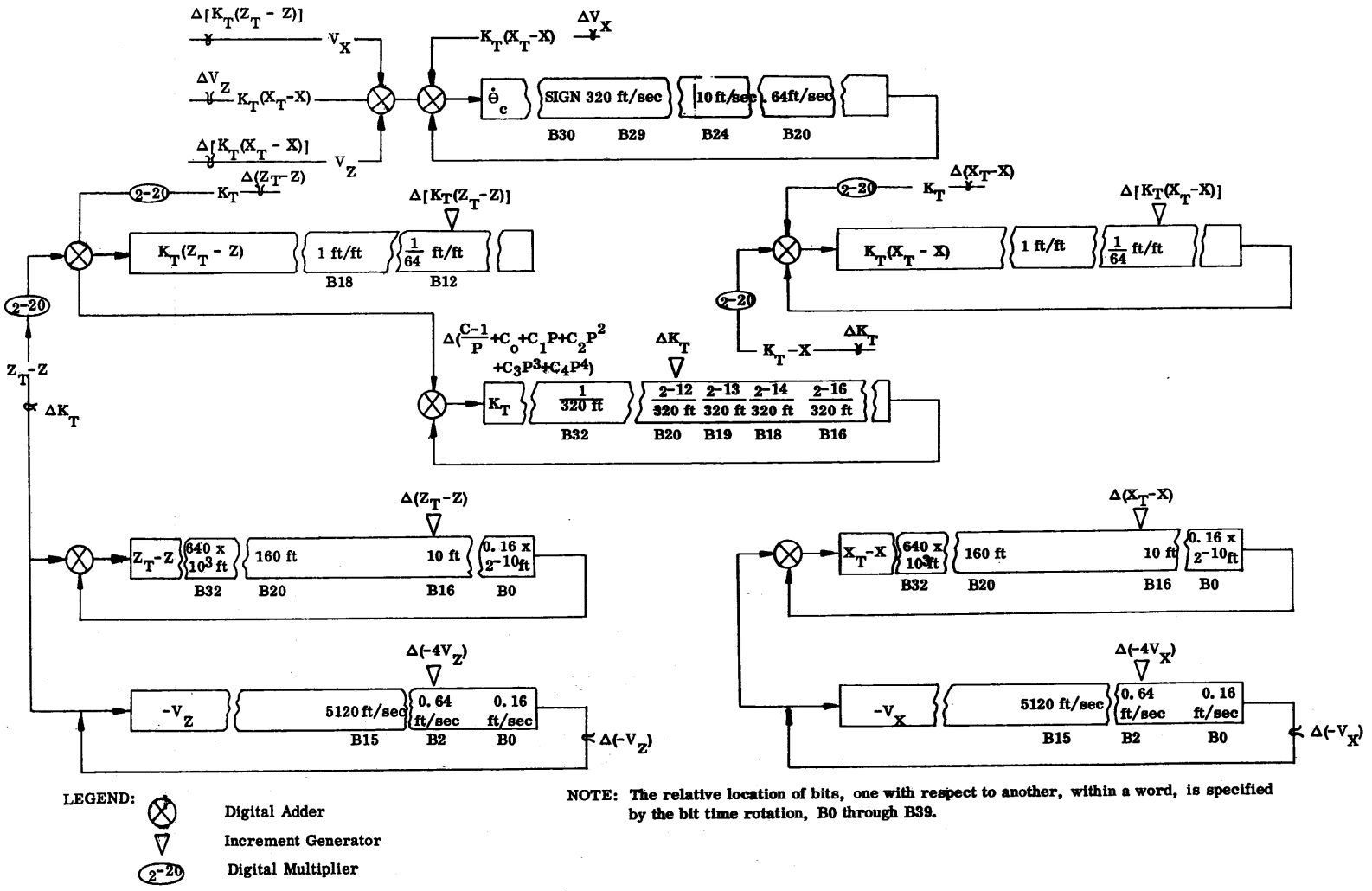


Figure 3-2a. Scaling Program

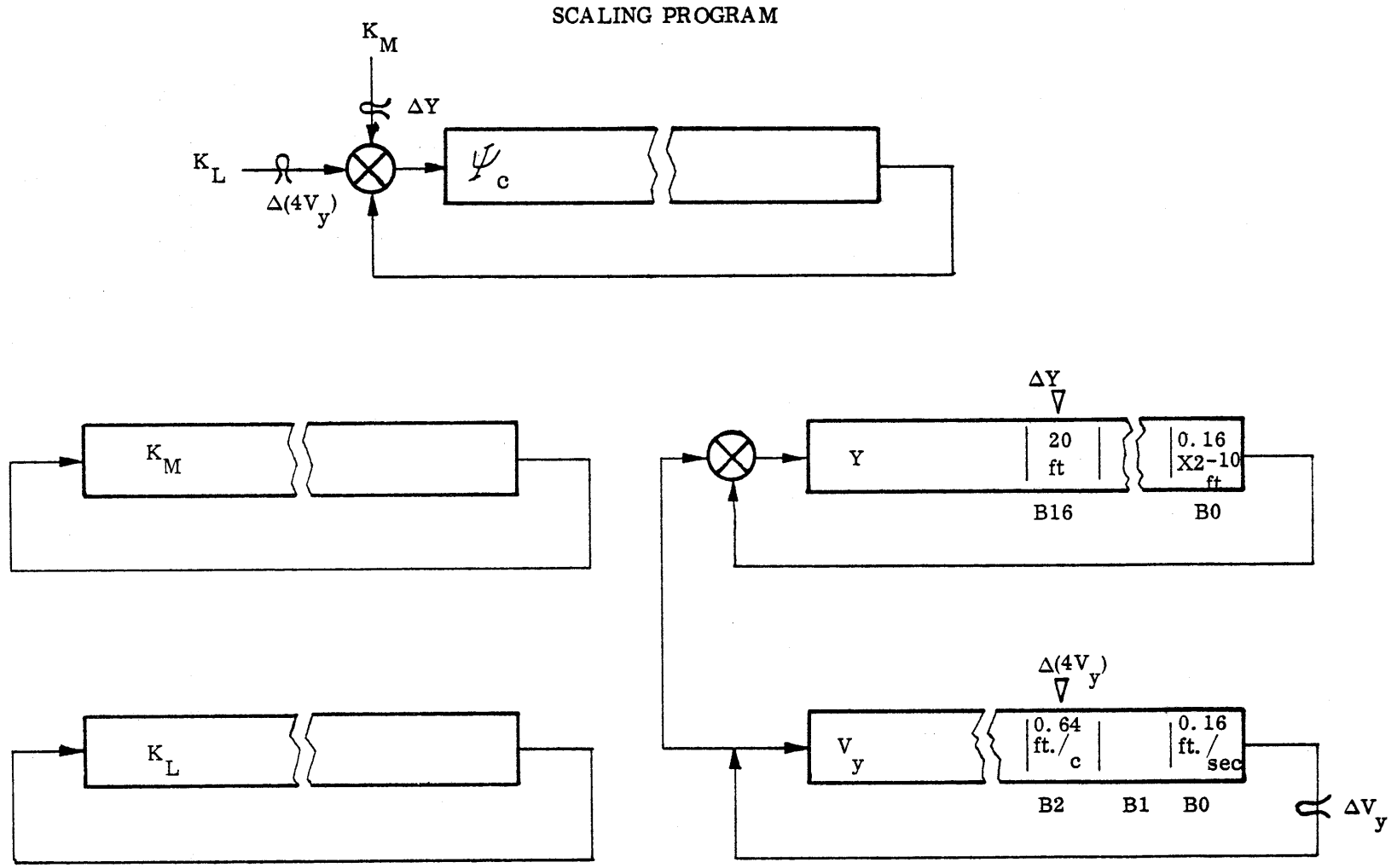


Figure 3-2b. Scaling Program

3.5 Implementation of Logic Functions

In the SIGS computer, all logic functions will be implemented using Fairchild micrologic elements. These elements represent the first, of numerous approaches in the development of molecular electronics, to become available in production quantities. Elements in this class offer important advantages in reliability, physical size, and economics for digital computers.

Six different logic functions are implemented with the micrologic elements. Actually, all the logic necessary for a computer could be implemented using only two of these; the remaining four improve the efficiency of the logic and thus reduce the total component count. Two of the elements implement rather complicated functions and are therefore used to a somewhat lesser extent. The six elements, shown in Figure 3-3, implement the following logic functions:

1. A three input NOR gate,
2. A flip-flop, together with the input transistors for setting it to either state,
3. A half-shift register element, which includes the logic necessary for shifting in a bit from an exterior flip-flop,
4. A buffer element, which acts as a signal amplifier,
5. A half adder, which produces both the sum and carry bits resulting from the addition of two binary variables,
6. The counter adapter, which implements the logic needed for the carry bit in a binary counter.

The prototype version of the SIGS computer will use the micrologic elements shown in Figure 3-3. However, it is anticipated that the lower power micrologic elements shown in Figure 3-4 will be available in production quantitites for use in the production version of the SIGS computer.

The use of the micrologic integrated circuits permits computer mechanization of the logic functions without the need of any other components. An example of the micrologic layout for a portion of the logic is shown in Figure 3-5. Interconnection of the integrated circuit elements is accomplished using multilayer circuit boards as shown in Figure 3-6.

The elements are carried on multilayer, etched circuit boards attached to aluminum frames. The circuit layer closest to the micrologic cans is a continuous sheet for the +3v power; ground plane is next, followed by three circuit layers for signals.

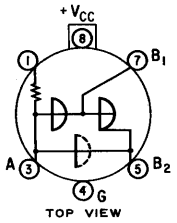
PRELIMINARY CHARACTERISTICS

MICROLOGIC ELEMENT "B"

BUFFER

SUPPLY VOLTAGE + 3 V_{dc} ± 30%
POWER DISSIPATION 25 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$B_1, \bar{B}_2 = \bar{A}$



INPUT (TERMINAL 3) - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT - 2.2 MICROLOGIC LOADS

OUTPUT (TERMINAL 5) - CAN DRIVE UP TO 25 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL (TERMINAL 7) - CAN DRIVE UP TO 5 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL
(NOTE - TERMINALS 5 AND 7 MAY NOT BE USED CONCURRENTLY)

AVERAGE DELAY - (TERMINAL 5) -60 nsec., (TERMINAL 7) - 50 nsec.

MULTIVIBRATOR OPERATION - CONNECTING TERMINALS 1 AND 8 PROVIDES A POSITIVE RETURN FOR A CAPACITOR INPUT TO TERMINAL 3.

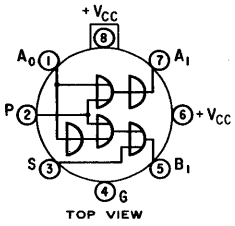
PRELIMINARY CHARACTERISTICS

MICROLOGIC ELEMENT "C"

COUNTER ADAPTER

SUPPLY VOLTAGE +3 V_{dc} ±30%
POWER DISSIPATION 75 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$\bar{A}_1 = \bar{A}_0 \bar{P}$
$\bar{B}_1 = A_0 \bar{P} + S$



INPUT - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT.
A_0, P (TERMINALS 1,2) - 2 MICROLOGIC LOADS
S (TERMINAL 3) - 1 MICROLOGIC LOAD.

OUTPUT (TERMINALS 5,7) - CAN DRIVE UP TO 5 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.

AVERAGE DELAY - 100 nsec.

NOTE - THE NODE RESISTORS OF THE OUTPUT INVERTERS ARE RETURNED TO TERMINAL 6 WHICH IS NORMALLY CONNECTED TO THE SUPPLY VOLTAGE.

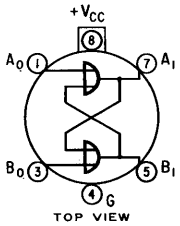
PRELIMINARY CHARACTERISTICS

MICROLOGIC ELEMENT "F"

FLIP - FLOP

SUPPLY VOLTAGE + 3 V_{dc} ± 30%
POWER DISSIPATION 30 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$\bar{A}_1 = B_1 + A_0$
$\bar{B}_1 = A_1 + B_0$



INPUT (TERMINALS 1,3) - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT - 1 MICROLOGIC LOAD.

OUTPUT (TERMINALS 5,7) - CAN DRIVE UP TO 4 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.

AVERAGE DELAY - 50 nsec.

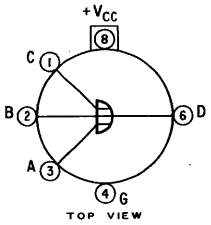
PRELIMINARY CHARACTERISTICS

MICROLOGIC ELEMENT "G"

GATE

SUPPLY VOLTAGE + 3 V_{dc} ± 30%
POWER DISSIPATION 15 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$D = (\overline{A + B + C})$



INPUT (TERMINALS 1,2,3) - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT - 1 MICROLOGIC LOAD.

OUTPUT (TERMINAL 6) - CAN DRIVE UP TO 5 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.

AVERAGE DELAY - 50 nsec.

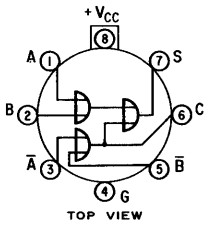
PRELIMINARY CHARACTERISTICS

MICROLOGIC ELEMENT "H"

HALF ADDER

SUPPLY VOLTAGE + 3 V_{dc} ± 30%
POWER DISSIPATION 45 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$S = A\bar{B} + \bar{A}B$
$C = AB$



INPUT (TERMINALS 1,2,3,5) - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT - 1 MICROLOGIC LOAD.

OUTPUT (TERMINAL 6) - CAN DRIVE UP TO 4 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.

OUTPUT (TERMINAL 7) - CAN DRIVE UP TO 5 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.

AVERAGE DELAY - (TERMINAL 6) - 50 nsec., (TERMINAL 7) - 100 nsec.

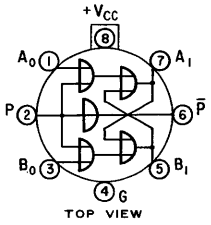
PRELIMINARY CHARACTERISTICS

MICROLOGIC ELEMENT "S"

HALF SHIFT REGISTER

SUPPLY VOLTAGE + 3 V_{dc} ± 30%
POWER DISSIPATION 75 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$\bar{A}_1 = B_1 + \bar{A}_0 \bar{P}$
$\bar{B}_1 = A_1 + \bar{B}_0 \bar{P}$



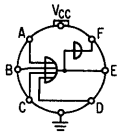
INPUT - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT.
A_0, B_0 (TERMINALS 1,3) - 1 MICROLOGIC LOAD.
P (TERMINAL 2) - 3 MICROLOGIC LOADS.

OUTPUT (TERMINALS 5,7) - CAN DRIVE UP TO 4 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.
(TERMINAL 6) - CAN DRIVE 5 OTHER MICROLOGIC LOADS.

AVERAGE DELAY - 100 nsec.

Figure 3-3. Micrologic Logic Table (Prototype)

GATE ELEMENT, G



The G element provides a four-input NAND/NOR gate with true and complementary outputs.

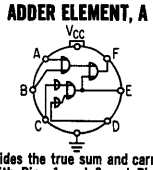
$E=\overline{A+B+C+D}$ (Positive logic)

$F=A+B+C+D$

ELECTRICAL PERFORMANCE
(Worst case) V_{CC}=3V; −55°C to +125°C

Input Loading — Pins A, B, C, D	1 Load
Fan-Out — Pin E	3 Loads
— Pin F	4 Loads
Signal Propagation Delay — Output E (Note 3)	40 nsec
— Output F	70 nsec
Power Consumption	5.0 mW

ADDER ELEMENT, A



The A element provides the true sum and carry of inputs A and B when connected with Pins 1 and 3 and Pins 2 and 5 shorted together; the generalized function of A, B, C, D is

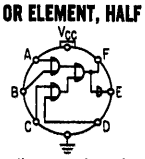
$E=CD$ (Positive logic)

$F=(A+B)\ (\overline{C}+\overline{D})$

ELECTRICAL PERFORMANCE
(Worst case) V_{CC}=3V; −55°C to +125°C

Input Loading — Pins A, B, C, D	1 Load
Fan-Out — Pin E	3 Loads
— Pin F	4 Loads
Signal Propogation Delay — Output E	70 nsec
— Output F	100 nsec
Power Consumption	12.5 mW

EXCLUSIVE OR ELEMENT, HALF ADDER, H



The H element provides the true and complement of the exclusive OR of A and B with A and B applied to Pins 1 and 2, respectively, and $\overline{A}$ and $\overline{B}$ applied to Pins 3 and 5, respectively. The following functions can be obtained:

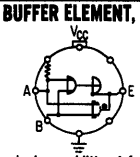
$E=(A+B)(\overline{C+D})$ (Positive logic)

$F=(A+B)(C+D)$

ELECTRICAL PERFORMANCE
(Worst case) V_{CC}=3V; −55°C to +125°C

Input Loading — Pins A, B, C, D	1 Load
Fan-Out — Pin E	4 Loads
— Pin F	3 Loads
Signal Propagation Delay — Output E	100 nsec
— Output F	70 nsec
Power Consumption	10 mW

BUFFER ELEMENT, B



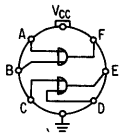
The B element is used where additional fan-out is required. The buffer can be gated and the resulting function is shown below. In addition, a pull-up resistor is provided for multivibrator applications.

$E=\overline{A+B}=\overline{AB}$ (Positive logic)

ELECTRICAL PERFORMANCE
(Worst case) V_{CC}=3V; −55°C to +125°C

Input Loading — Pins A, B	2 Loads
Fan-Out — Pin E	30 Loads
Signal Propagation Delay — Output E (Full Load)	60 nsec
Power Consumption — 50 percent duty and full load	12.5 mW

DUAL GATE ELEMENT, D



The D element provides a pair of two-input NAND/NOR gates with complemented outputs.

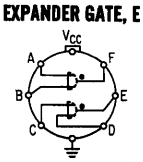
$E=\overline{C+D}$ (Positive logic)

$F=\overline{A+B}$

ELECTRICAL PERFORMANCE
(Worst case) V_{CC}=3V; −55°C to +125°C

Input Loading — Pins A, B, C, D	1 Load
Fan-Out — Pins E, F	4 Loads
Signal Propagation Delay — Pins E, F	40 nsec
Power Consumption	5.0 mW

EXPANDER GATE, E

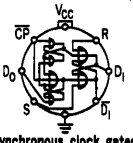


The E element is used to increase the fan-in capabilities of the family. The E is similar to the D element except that the output node resistors are omitted. The E can extend the fan-in of any other element, except the Buffer, up to a maximum of 4 additional inputs without exceeding the guaranteed electrical performance of the other elements.

ELECTRICAL PERFORMANCE
(Worst case) V_{CC}=3V; −55°C to +125°C

Input Loading — Pins A, B, C, D	1 Load
Fan-Out — Pins E, F (Note 2)	N.A.
Signal Propagation Delay — Pins E, F	40 nsec
Power Consumption (Note 2)	N.A.

REGISTER ELEMENT, R



The R element is a synchronous clock gated flip-flop with asynchronous set and reset. This element can be used both as a full shift register stage or as a complementing binary flip flop. The complementing function is achieved by coupling back $\overline{D}_1$ to D_0. Data at D_0 are entered during a one-to-zero transition of $\overline{CP}$. The data bit D_0 must be present a minimum of 70 nsec before, and 20 nsec after the 50-percent point of a one-to-zero transition of $\overline{CP}$.

$D_1=S+CPD_0$

$\overline{D}_1=R+CP\overline{D}_0$

ELECTRICAL PERFORMANCE
(Worst case) V_{CC}=3V; −55°C to +125°C

Input Loading — Pins D_0, S, R	1 Load
— Pin $\overline{CP}$	2 Loads
— Pins D_1, $\overline{D}_1$	3 Loads
Signal Propagation Delay — Synchronous Entry	Note 1A
— Asynchronous Entry	Note 1B
Power Consumption	15 mW

NOTES:

1A. Synchronous entry of data: When data are being entered through the D_0 input, the 50-percent points of the D_1 and $\overline{D}_1$ waveforms shall occur within 120 nsec of the one-to-zero transition of $\overline{CP}$.

1B. Asynchronous set and reset: When the R element is set or reset through the R and S inputs, the 50-percent points of the D_1 and $\overline{D}_1$ waveforms shall occur within 70 nsec of the 50-percent point of the R or S pulse.

2. The fan-out and power consumption for the E element are not applicable. The ratings for the element being expanded apply.

3. The maximum signal propagation delay is defined for the entire temperature range of −55°C to +125°C and any combination of the rated loading. Measurement is made between 50-percent points input-output with a G element as a driver.

Figure 3-4. Micrologic Logic Table (Alternate)

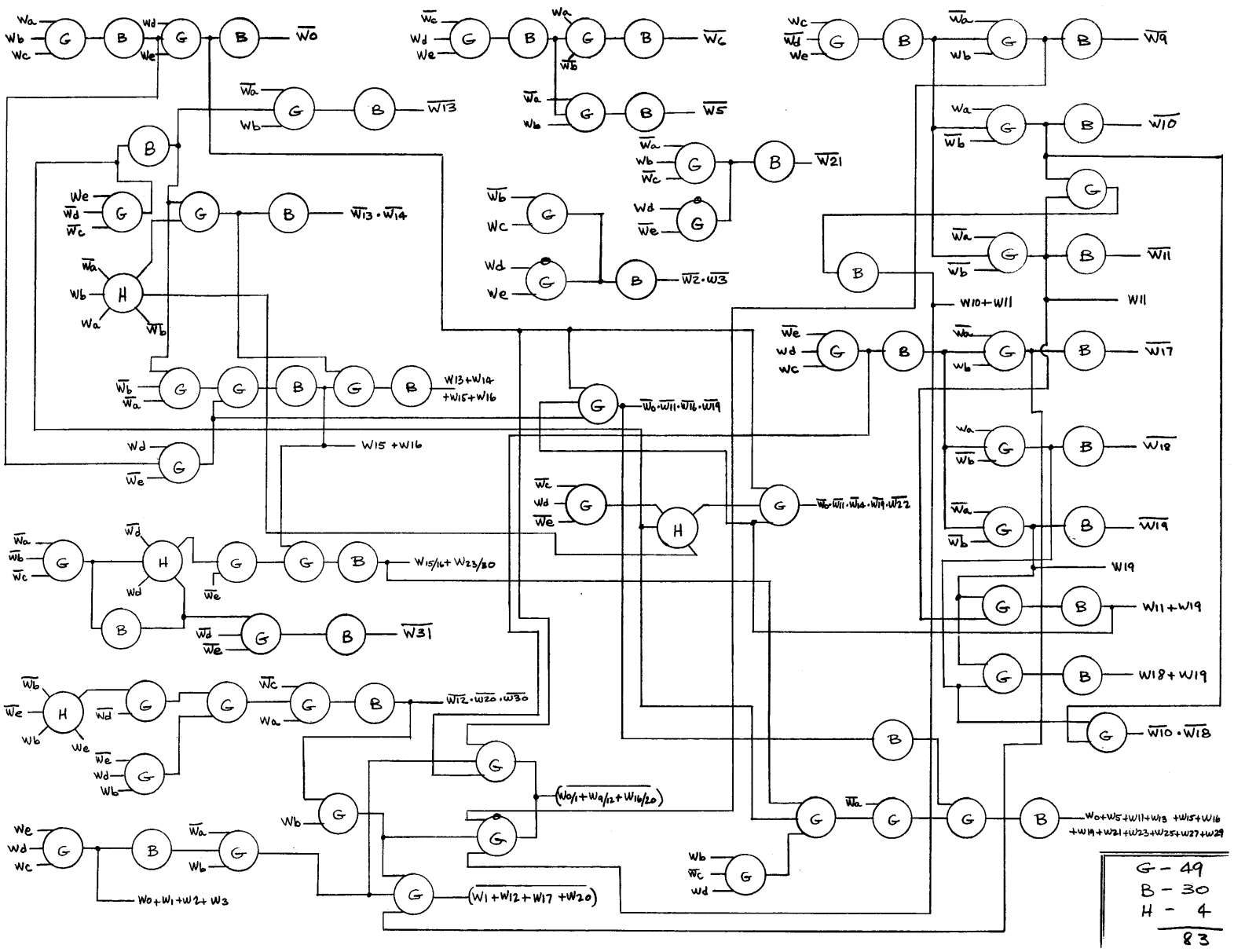


Figure 3-5. Typical Micrologic Layout

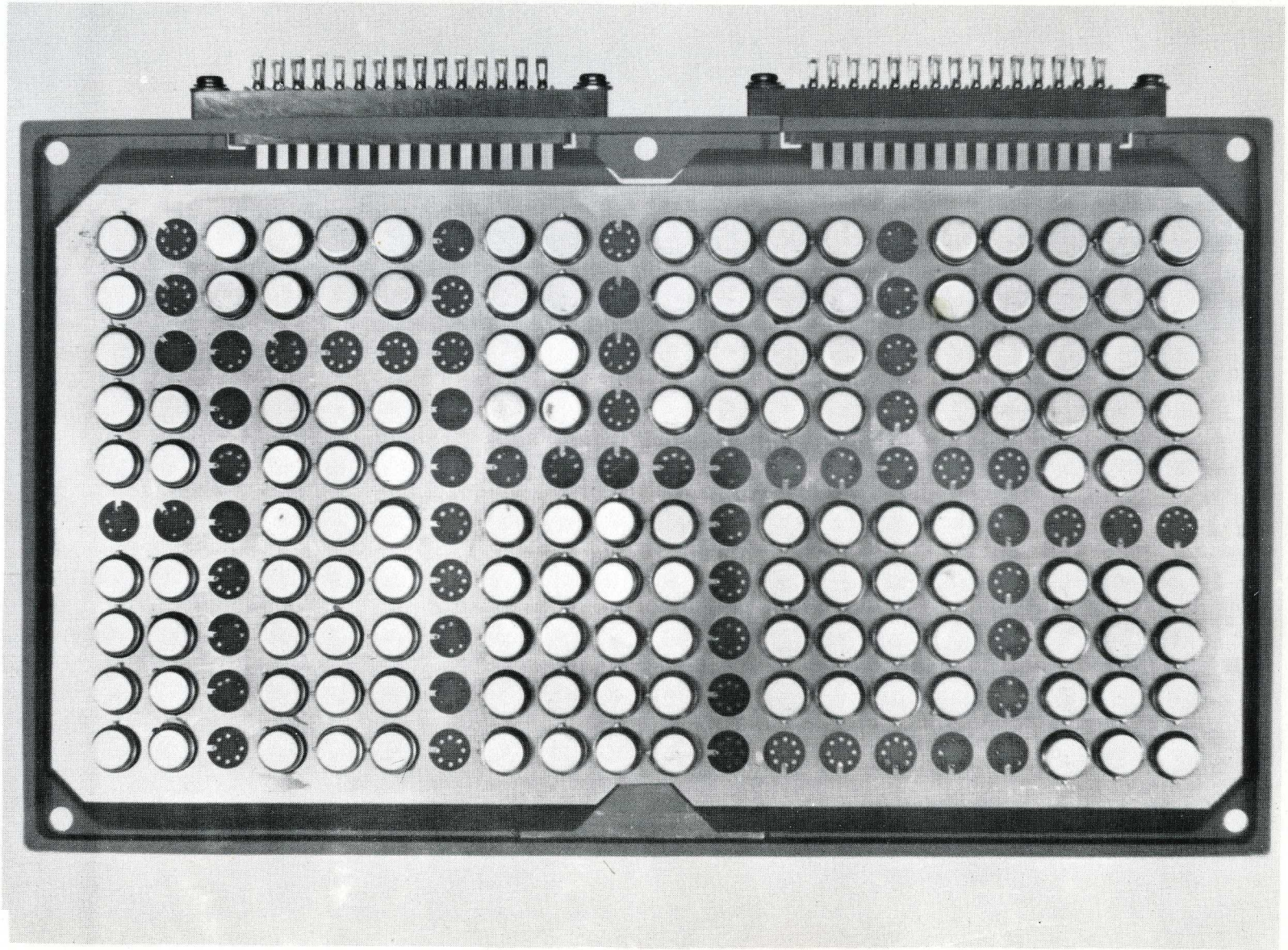


Figure 3-6. Multilayer Logic Board

The ground plane serves two useful purposes. First, it provides a low impedance ground reference for every micrologic circuit. Secondly, the proximity of the signal conductors to the ground plane reduces the self- and mutual-inductance effects of these wires. The logic boards will accommodate all circuits required for sizable units of the computer to minimize the number of signal wires that must pass through edge connectors.

3.6 Modular Concept

Modularity of packaging is defined as the ability to satisfy a wide variety of guidance applications through easy replacement of the logic boards which essentially define the computer program. Because all classes of missiles require some form of memory and interface electronics, these are packaged in the top and bottom sections and would be common for all applications. It is assumed that some standardization for the various missile classes is possible; for example, all accelerometer inputs would be in pulsed form and all autopilot outputs would be dc voltages. Variations between the requirements for the longer versus the shorter range missiles would be reflected in the interconnections within the logic boards and in the number of logic boards needed. For example, the prototype computer was designed for the Advanced Pershing Missiles class wherein two logic boards were used. For the shorter range tactical missiles, the guidance function might be specified using a single logic board.

Since 70 to 80 percent of the material cost of this computer is concentrated in the integrated circuits held by the logic boards, substantial savings might be realized by removing all unnecessary elements prior to any particular firing by replacing appropriate boards.

3.7 Low-Cost Design Features

One of the primary design goals of this computer study was to establish low initial and maintenance costs. Selection of materials, fabrication, and computer techniques were all directed toward this end. The glass delay line is a good example of this effort. This digital device has high-speed performance, good reliability potential, simple construction, no requirement for calibration or adjustment, and yet is probably the most inexpensive memory element available. Since memory cost is one of the major considerations in the total computer cost, the use of low-cost glass delay lines proves to be an important factor.

The use of multilayer etched circuit boards to interconnect the integrated circuits also contributes to computer low cost. The use of these boards, combined with batch soldering techniques, greatly simplifies the assembly task and reduces checkout time and cost because of the elimination of wiring errors.

The integrated circuits are the largest cost factor in the SIGS computer. Even in the relatively early stage of this new technology, the price of integrated circuits is competitive with equivalent assemblies of conventional components. As the market for these devices increases with time, the price per device should reflect the same dramatic decrease which has been evident in individual semiconductor devices. Transistors used in military systems, for example, have decreased in price by an order of magnitude within a period of three to four years.

The design goals of low cost and high reliability have been achieved in the SIGS design. The hybrid computing technique, simplicity of packaging, and careful selection of materials have resulted in a computer design that is competitive in cost with other computing techniques such as electromechanical, or pure electronic analog computers, yet retains superior performance in terms of accuracy, speed, flexibility, maintainability, and relability.

3.8 Expansion Capability

Although the SIGS computer is designed primarily to perform guidance and steering functions, its speed, computing capability, reliability, and low cost give it ready expansion capability. This expansion capability might, for example, include in-flight data reduction for instrumentation, system monitoring, attitude control, or forward control function. Further, its modular packaging allows it to accept additional computing tasks by inserting new logic and programming boards as well as additional memory lines or interface equipment.

SECTION IV

COMPUTER HARDWARE

The SIGS computer incorporates the latest in digital technology in terms of material, components, and techniques. Unique features of this computer include the use of solid-state, glass acoustic delay lines for the main memory, molecular integrated logic circuits, and multilayer etched interconnection boards.

4.1 Circuit Design

4.1.1 Integrated Circuits

The SIGS computer will use Fairchild micrologic integrated circuits for the implementation of all logic functions. The Fairchild micrologic element is fundamentally a complex semiconductor device fabricated with the same techniques that are now used in transistor manufacturing. There are several different types of elements, each capable of implementing a particular logic function using DCTL-type circuits. Each micrologic element consists of from one to five DCTL NOR gates. The circuit components — resistors and silicon planar transistors — are diffused into a single slab of silicon, and metal interconnections are deposited on top of the slab. The device is then packaged in an eight-lead TO-18 or modified TO-5 transistor can. Figure 4-1 illustrates a typical micrologic element in a TO-5 can. The schematic diagram and logic diagram of a typical element, the flip-flop, is shown in Figure 4-2.

All the transistors and resistors are fabricated simultaneously in a sequence of steps corresponding to those used to fabricate a single planar silicon transistor. The bases of all transistors, for example, are diffused simultaneously into the appropriate collector areas in one step through the use of an appropriate mask; this corresponds to the step for a single transistor in which the base is diffused into the collector area. Essentially, the same sequence of steps is used regardless of the particular micrologic element being fabricated; however, different masks are used to obtain the appropriate number of devices and the desired interconnection arrangement.

Connections from the element to the leads of the package are made by means of thermocompression bonds. A conventional cap is then welded onto the header to form a hermetically sealed semiconductor device.

From the schematic diagram of Figure 4-2 it can be seen that the circuitry implemented with the micrologic element is very simple and straightforward. It is the well-known DCTL circuitry, in which transistors are used as current switches and resistors are used as current sources for the switches; no other components are needed in the circuits.

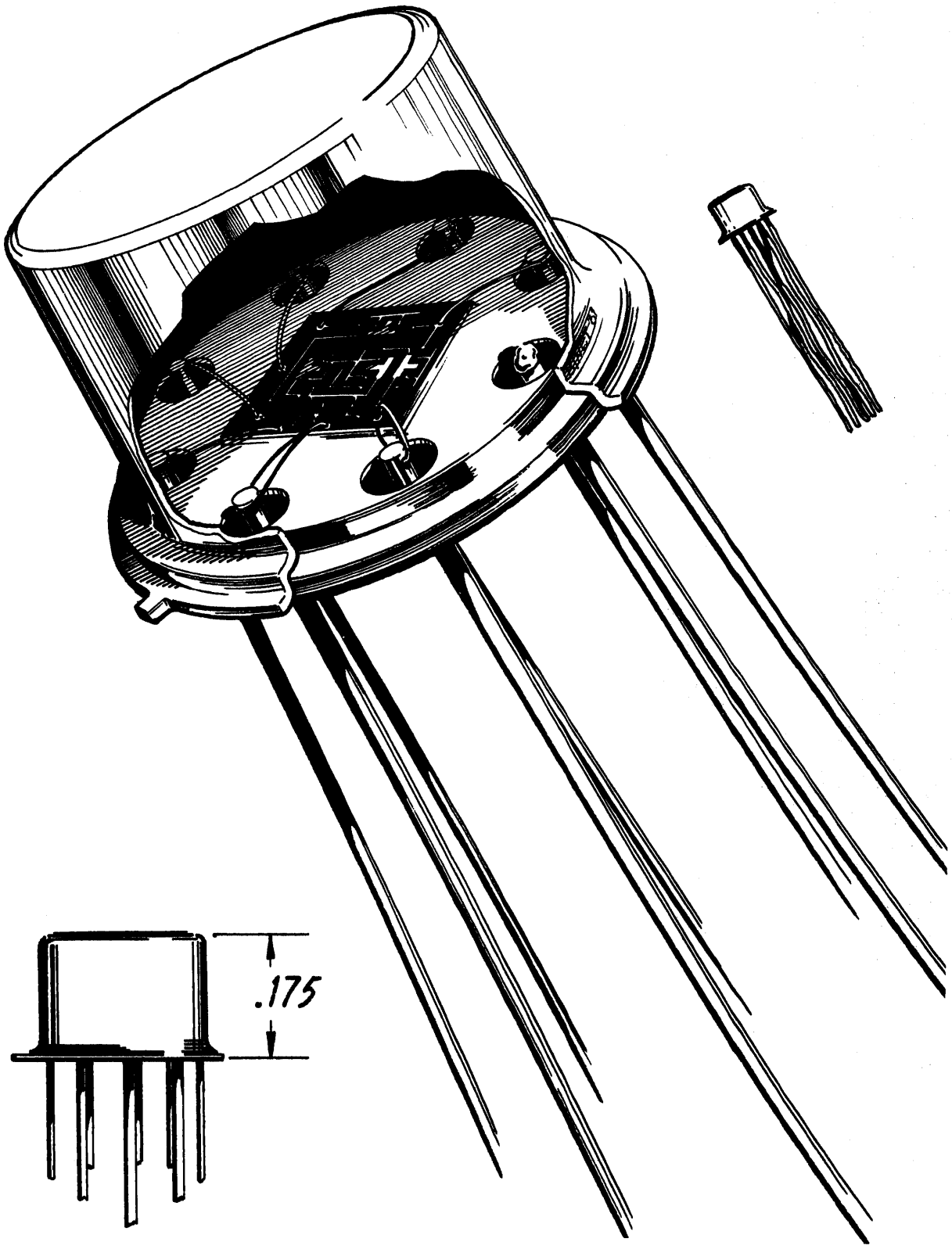
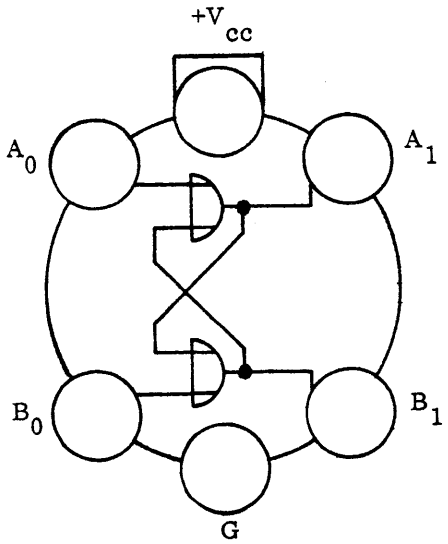


Figure 4-1
Cutaway Drawing of Micrologic "S" Element



$$\overline{A}_1 = B_1 + A_0$$

$$\overline{B}_1 = A_1 + B_0$$

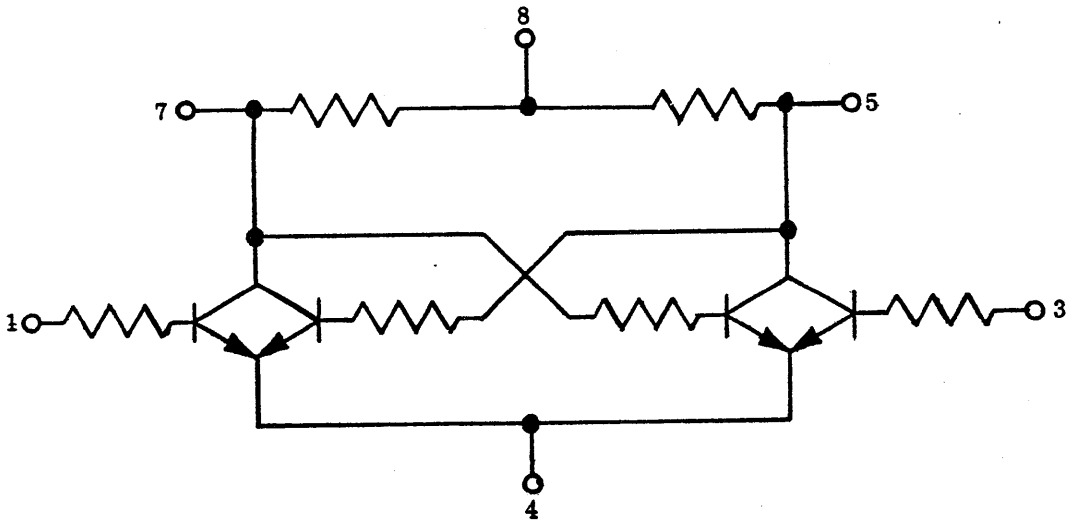


Figure 4-2. Micrologic "F" Element

Serious disadvantages would be encountered if conventional components were used to implement DCTL. Among these are the special characteristics needed for the DCTL transistors, the number of semiconductor devices that are needed, and the dependence of circuit speed upon the storage time of the transistors. These disadvantages are, in large measure, overcome in the micrologic approach. With conventional components, the large number of transistors leads to high cost and potentially low reliability. Because of the similarity of the manufacturing processes, the cost of micrologic elements should not be very much higher than the cost of equal-quality single transistors, and the reliability of the elements should be many times better than the reliability of an equivalent number of individual transistors. The transistors in the micrologic elements are specially designed to provide the characteristics needed for a DCTL transistor, without any necessity for compromising these characteristics to make the transistors suitable for other applications. It is easy to design a transistor with low storage time characteristics because of the low voltage requirements of DCTL circuits. As a consequence of these factors, DCTL is particularly attractive for micrologic implementation.

Micrologic elements are manufactured in two forms: high-power and low-power. The high-power micrologic elements are currently available and will be used to mechanize the prototype computer. The low-power micrologic elements were developed under Government contract by Fairchild and will shortly be available in production quantities.

Both types of micrologic elements have been designed to operate over a temperature range from -55 to +125^{o}C. They will provide a logic fan-out up to five over this range, and will have an average signal propagation delay of less than 50 nanoseconds per circuit stage. This operating speed is more than adequate for use at a 1-megacycle clock rate.

4.1.2 Digital-to-Analog Conversion

Six-digit-plus-sign digital-to-analog conversion is performed by the Kirchoff Adder circuit of Figure 4-3. The circuit consists of a feedback amplifier having an input current summing node into which seven weighted currents may or may not be switched, depending on the state of the digital input bit controlling each weighted current. The magnitude of the weighted currents decreases exponentially from the sign bit to the least significant bit. When cut off, an input transistor allows its weighted current to flow into the summing node, while a transistor fully conducting into saturation diverts the current away from the node. The seven input transistors are driven by outputs of a seven-stage micrologic register.

The net current entering and leaving the node must equal zero. A constant bias current flowing through the "zero setting resistor" and equalling the magnitude of the sign current places the mid-scale analog output at zero volts. Any difference

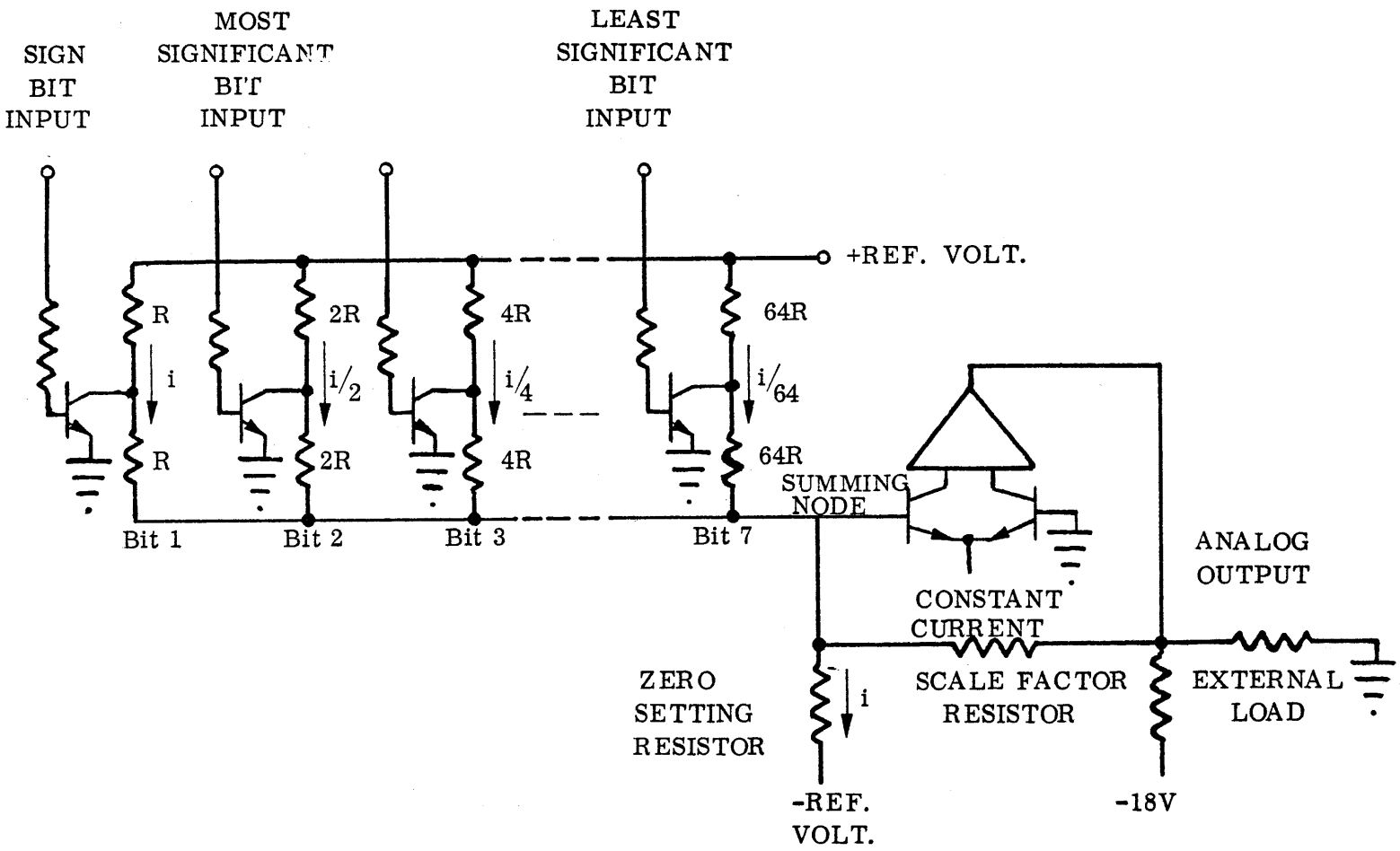


Figure 4-3. Kirchoff Adder Used for Digital-to-Analog Conversion

between the sum of the weighted currents and the bias current must flow in a plus or minus direction through the scale-factor resistor to place the output voltage at a prescribed level between +5.9 and -6.0 volts, the two end points which correspond to inputs of +63/64 and -1.0, respectively.

The voltage at the summing node is maintained at zero volts by use of a balanced differential transistor input stage grounded on one side. This input stage operates at such low current levels that even the worst-case differential transistor base current is negligibly small when compared with the least significant weighted current.

The amplifier circuit is presently designed to drive ±2.5 milliamperes, at ±6 volts into a grounded load with an output impedance less than 20 ohms. The analog output will track to within ±1 percent of half-scale (±0.060 volts) at its zero volt mid-scale setting, and to within ±3 percent of half-scale (±0.180 volts) at the ±6 volt end points over a +70° to -50°C temperature range. Tracking at higher temperatures is limited by the leakage currents of cutoff input transistors.

4.1.3 Clock Timing Circuitry

Figure 4-4 shows the timing logic used to derive the computer clock system from the 3.932 megacycle crystal oscillator source, $\overline{P}$. Clocks CP and CR are used by the computer as two-phase clocks. CR, $\overline{CR}$, and CW are used by the glass memory multiplexing and decoding logic.

Two one-shot multivibrator circuits, M and N, are used to generate two 320 nanosecond pulses on opposite phases of the $\overline{P}$ square wave. Each pulse must be wide enough to span between two and three $\overline{P}$ phases, that is, two and one-half ±one-half of a phase time. The tolerance on the pulse width generated by each one-shot multivibrator is therefore ±20 percent.

The proper width of the CW clock, used by the glass memory, was derived by dividing the basic 763 nanosecond computer clock period into 6 equal 127 nanosecond intervals.

4.2 Glass Memory

The two acoustic glass memory lines used in the computer offer distinct advantages for tactical missile application. Each is a solid-state device with no moving parts and is extremely simple in construction, low in cost, has very high operating speed, and has a composition which is both time and temperature invariant. Temperature insensitivity is achieved by carefully choosing the glass composition such that temperature variation in the acoustic propagation time is nearly offset by the

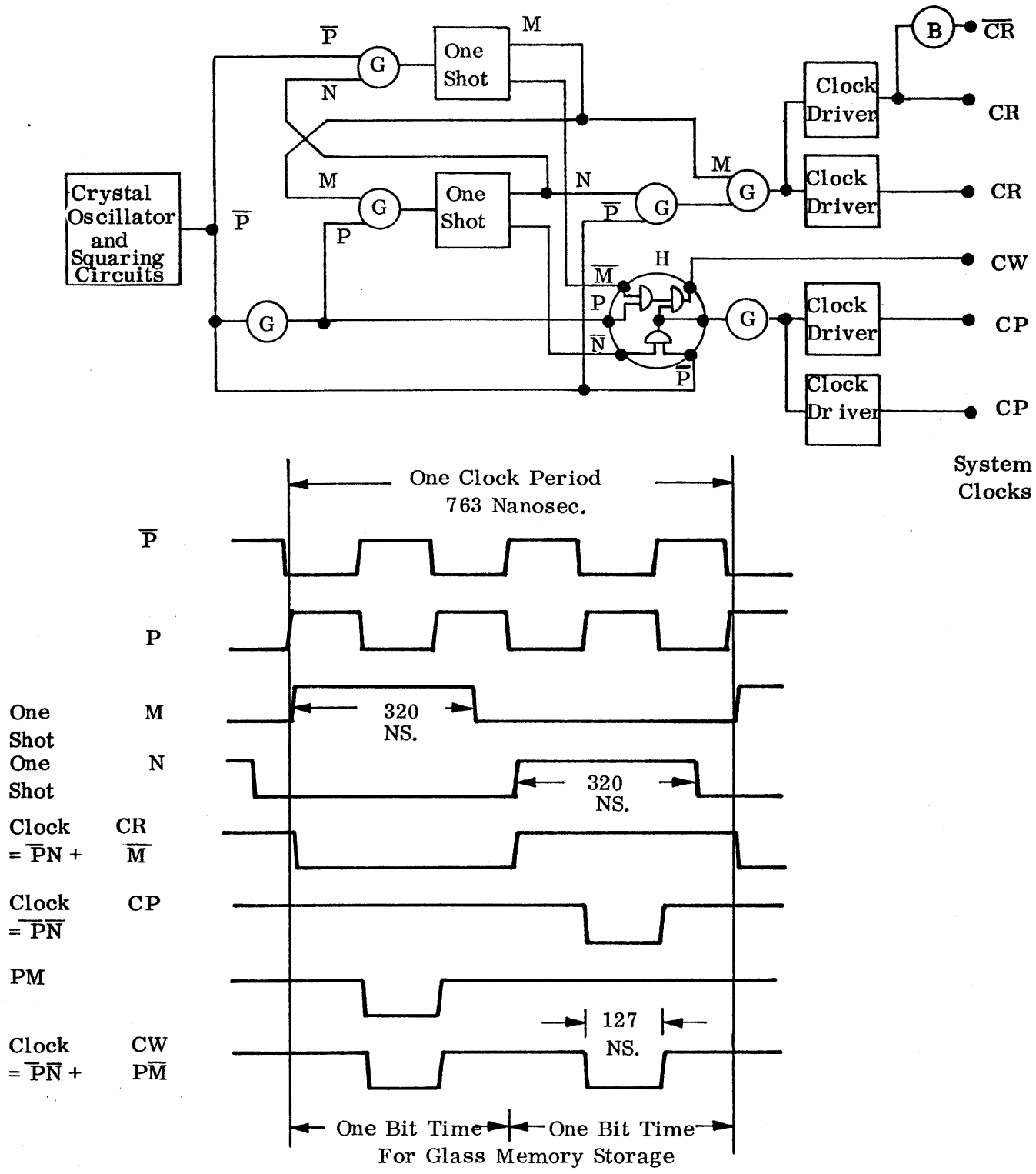


Figure 4-4. Clock Timing Logic

temperature coefficient of expansion. Thus, the variation in delay time is extremely small over a wide temperature range. The maximum variation of the 240 microsecond line is ±25 nanoseconds for a temperature range of -50 to +100°C. Time delay stability is assured by curing the glass stock for several years before grinding to the specified length. Glass delay line ruggedness is achieved by embedding the slab of glass with its transducers in a resilient foam. This construction permits operation under vibrations up to 80 g's over a wide frequency range. A photograph of a typical glass delay line is shown in Figure 4-5.

Operation of the line may be described briefly in the following manner. Input and output transducers convert electrical energy to mechanical energy and vice versa. An input voltage pulse is converted into a compressional wave which propagates through the glass medium at a speed of approximately 10 microseconds per inch of travel. Varying delay times are achieved by reflecting the impulse off the multisided faces on the glass block. Precise grinding of the glass faces permits delay length accuracy to one-fifteenth of a bit time. The acoustic impulse is converted back into electrical energy by the output transducer. Voltage attenuation through the memory is approximately 40 db, producing a 120 millivolt output signal peak from a 12 volt driving source.

The 242.5 microsecond delay line used for the SIGS computer stores 640 bits of information interlaced into two channels by a time multiplex scheme. Each channel has a 1.3 megacycle bit rate, with the multiplexed line operating at a 2.6 megacycle rate. Resonance of the transducers at 4 megacycles requires a 127 nanosecond input pulse for return-to-zero (RZ) recording. As shown in Figure 4-6, the response of the output transducer is a triplet waveform, the center portion of which is confined to 127 nanoseconds. Only the center portion of the triplet is detected by the readback circuitry.

4.2.1 Read and Write Circuitry

The glass memory read and write circuitry, pictured in Figure 4-7, consists of a driver circuit, a sense amplifier, and multiplexing and decoding logic for each of the two glass lines; typical waveforms are shown in Figure 4-6.

Each line receives inputs from two 1.3 megacycle sources of data which are interwoven at a 2.6 megacycle rate on alternate phases of bit clock CR by the multiplexing logic. A data ZERO is gated through the logic, shaped to a 127 nanosecond width by clock CW, and amplified by the memory driver circuit to a 12 volt pulse with 40 nanosecond rise and fall times. A data ONE is blocked by the logic and appears in the memory as the absence of a stored pulse.

The response of the glass line from a data ZERO input pulse is a triple-peaked output (triplet) signal emerging after 318 clock periods (242.615 microseconds) of

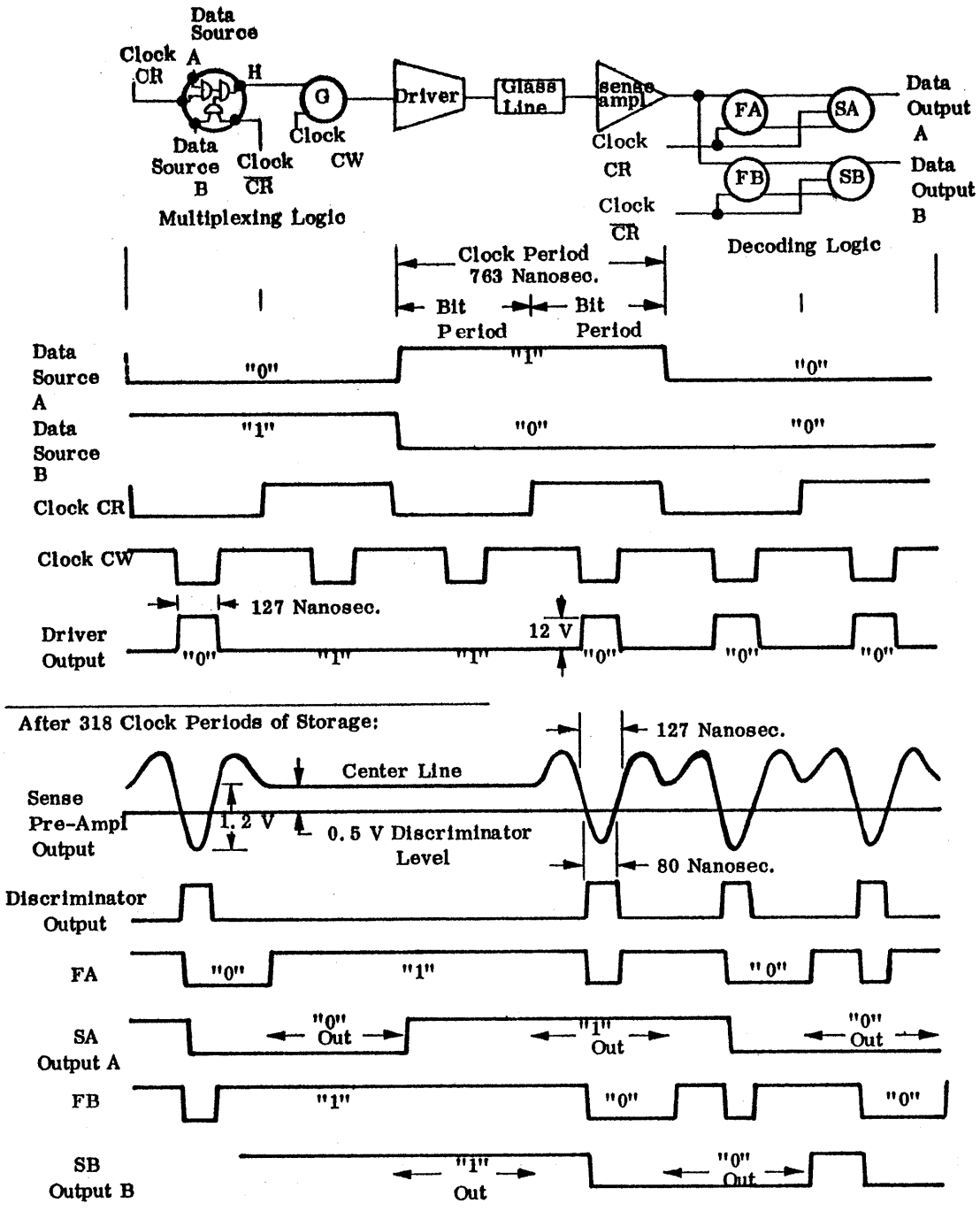


Figure 4-6. Glass Memory Logic and Waveforms

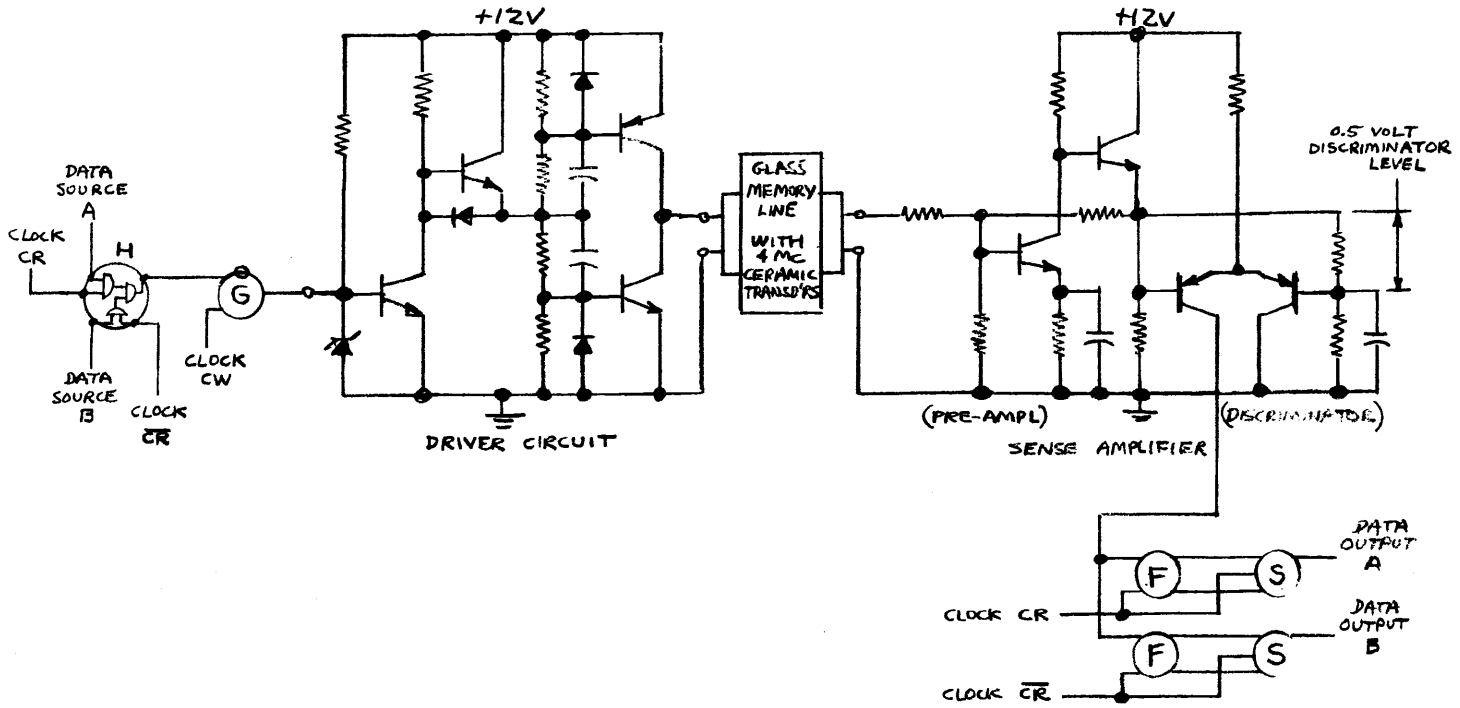


Figure 4-7. Glass Memory Logic and Circuits

storage. After linear amplification of approximately 10 in the sense preamplifier, the negative 1.2 volt center portion of the triplet is passed through the 0.5 volt noise-rejecting level of the discriminator circuit.

The purpose of the decoding logic is to separate data associated with bit clock CR from that of $\overline{CR}$ as they both emerge from the sense amplifier output. During each bit period, the micrologic S element of one of the channels is left unblocked to receive data, while the S element of the other channel is blocked by the clock. The F element of the blocked channel is set to the ONE state by clock control.

The F element of the unblocked channel can receive a data ZERO pulse anytime during the bit period, thereby allowing for a maximum of approximately plus or minus one-half bit of jitter between the bit clock and the memory output. One or more of three sources could contribute to jitter; these are,

1. Variations in glass line delay time due to temperature changes. Jitter from this source will not exceed one-fifteenth of a bit time.
2. Variations in clock frequency. An oscillator crystal variation of one part in 10^4 would result in a jitter of only one-fifteenth of a bit time.
3. Variations in read and write circuit propagation time. A circuit delay time of 115 nanoseconds has been allowed between the CW clock gating in the multiplexing logic and the input of the S element of the decoding logic. A 25 nanosecond variation in this time would cause a jitter of one-fifteenth of a bit time.

4.3 Mechanical Design

The SIGS computer has been mechanically designed to operate within the environmental specifications of tactical ballistic missiles. The specific design proposed herein was influenced primarily by cost considerations, although reliability and maintainability strongly influenced design decisions.

The computer configuration is a rectangular box 2-1/8" x 6-1/8" x 10", occupying 0.08 cubic foot, and weighing approximately 6 pounds. In Figure 4-8, a prototype model of the SIGS computer is shown to illustrate the modularity of the "box". Four modules (refer to Figure 1-2) are nested together to form an easily assembled, rigid structure. The computer can be mounted directly to the missile by means of four through bolts or to any supporting structure by means of attaching a base plate. Two 25-pin external connectors are conveniently located for interface and checkout functions.

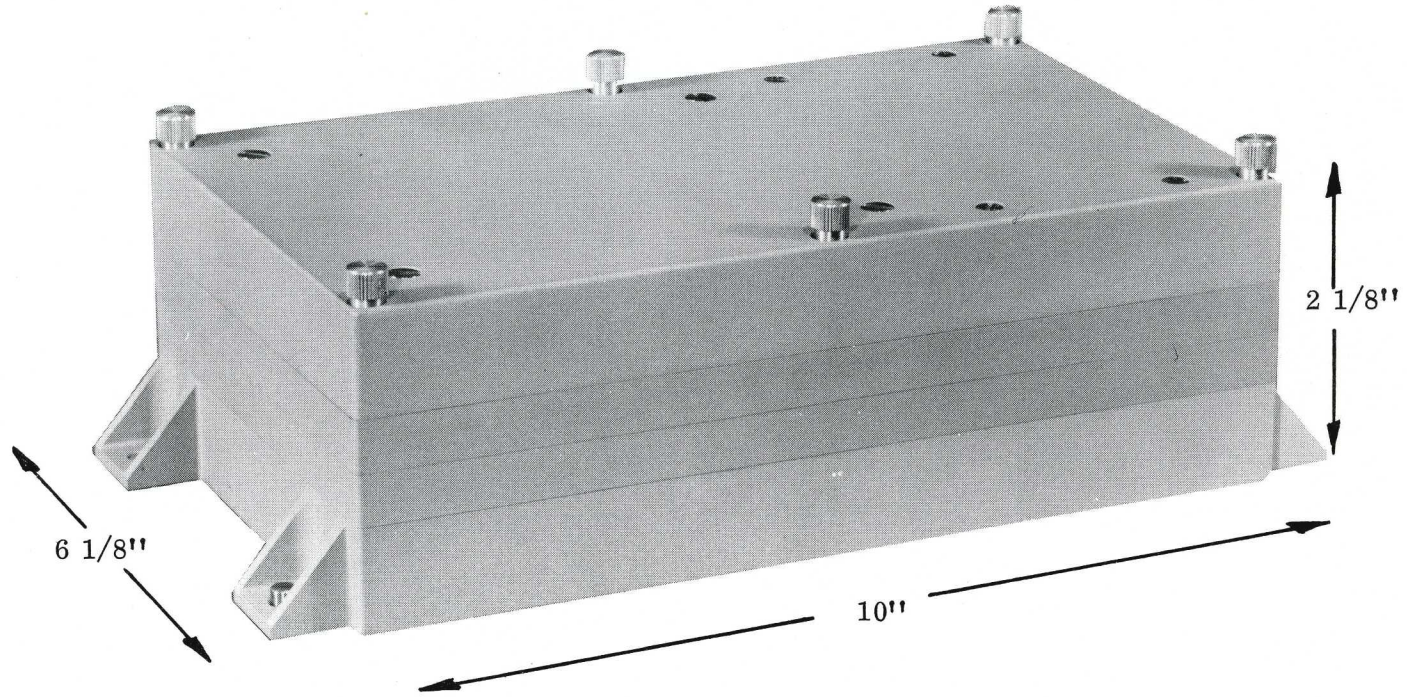


Figure 4-8. SIGS Guidance and Steering Computer

4.3.1 Logic Modules

The logic section of the computer is completely mechanized using integrated circuits (micrologic elements) interconnected on multilayer printed circuit boards. The boards are bonded to die-cast aluminum frames which form part of the computer structure. This integral construction provides support without incurring a weight penalty. All required micrologic elements are mounted on two boards.

The use of multilayer printed circuit boards affords distinct advantages for packaging of integrated circuits. Among these are low cost, high density, and increased reliability through a reduction in the number of interconnections. Each six-layer board includes a continuous ground plane to minimize induced noise, a +3 volt power plane, and four signal layers, with plated-through holes providing the required interlayer connections.

A test program conducted at AC Spark Plug has established that multilayer boards can be qualified in accordance with applicable Military Specifications, and that they operate reliably in the required missile environment.

4.3.2 Memory Module

The memory module comprises one of the outer covers (another casting) into which two glass delay lines and all associated memory electronics have been mounted. Memory electronics are packaged as discrete components on etched circuit boards.

4.3.3 Power Supply Module

The power supply module will be supplied with the production computer assembly. A description of the power supply is contained in Paragraph 4.4. The power supply will be packaged as an attached module. High thermal dissipation devices are heatsinked to the structure directly.

4.3.4 Interconnections

Intermodule connections are provided at one end of the computer by a harness that is permanently attached to the memory module. External connectors are also mounted on this module and interconnected with the harness. Access to the harness is provided by removing the end dust cover.

4.3.5 Environmental Protection

Environmental protection is provided, on the module level, by conformally coating each completed assembly with a polyurethane film approximately 1/32 inch

thick. This coating acts as a vibration damper, provides mechanical support for mounted components, and seals the assembly against moisture. The box structure and the through bolt mounting arrangement yield a strong, lightweight, serviceable assembly.

4.4 Power Supply

The production SIGS computer requires 8 watts of power, 760 ma at 3 volts, 400 ma at 12 volts, and 50 ma at -18 volts. A 3-volt supply with a 10 percent tolerance is adequate for the micrologic, and 5 percent will suffice for the +12 and -18 volt supplies. Since none of the load currents will vary appreciably, line regulation should be all that is necessary to provide the required voltages.

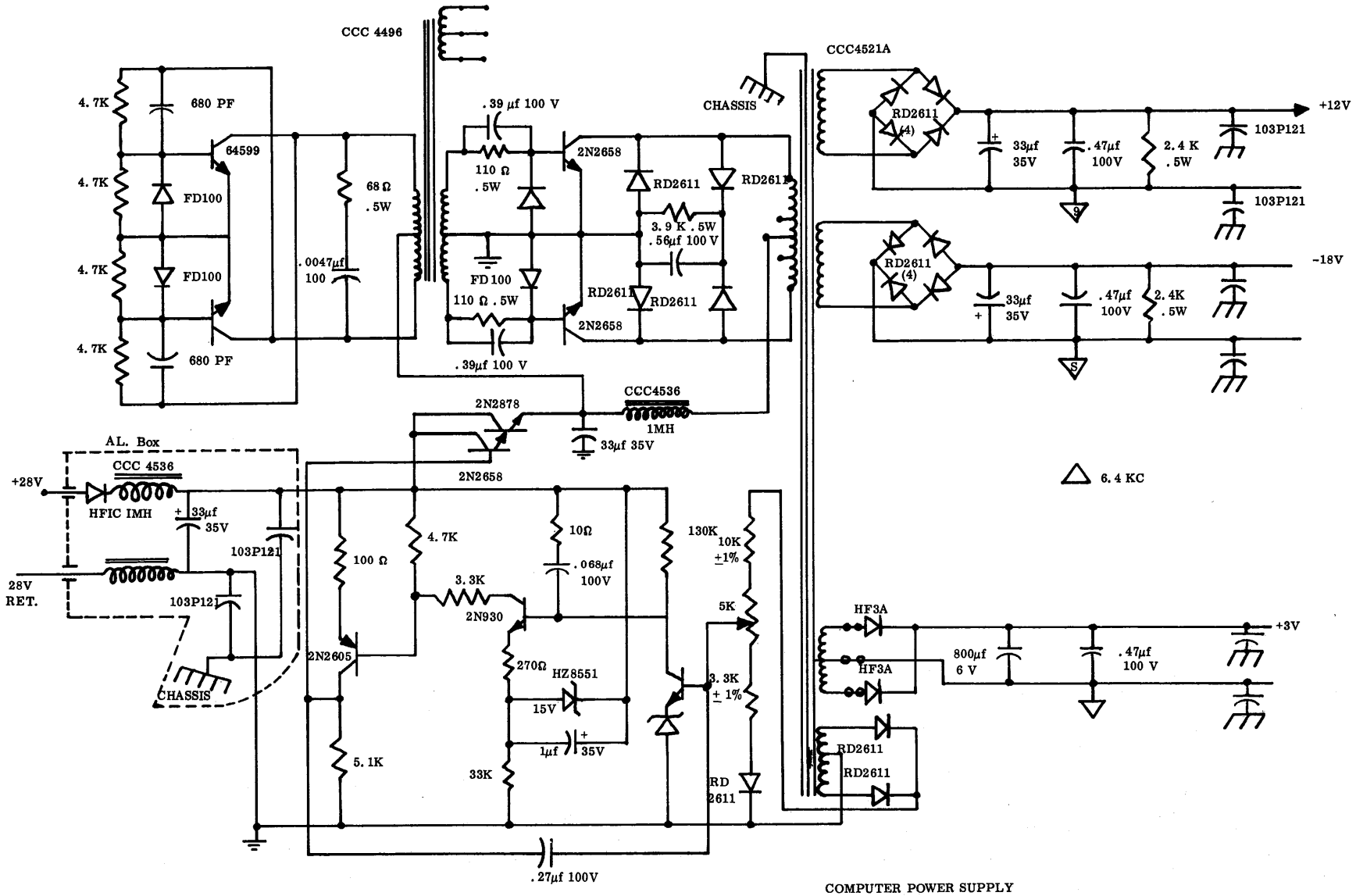
Figure 4-9 illustrates the power supply for the computer. The supply consists of a series regulator supplying a constant voltage to a static inverter. The inverter is transformer-coupled to three sets of rectifiers. The design goals for this supply are simplicity, cost, efficiency, and accuracy. A series regulator can be inserted in the input without serious loss of efficiency because the specification on the input voltage is 28 ± 2 volts.

The following comments note some of the features of this supply. The feedback for the regulator is taken from a winding on the secondary such that primary losses in the transformer are included in the feedback. Thus, the only losses affecting regulation are the secondary copper losses of the transformer and the rectifier losses. In the comparator circuit, reference is made to a rectifier diode to thermally compensate for the output rectifiers. It must be noted that bridge rectifiers are used for the low current supplies while a full wave center tapped winding is used for the high current supply. The bridge circuit requires twice the diodes and one-half the transformer turns of the center tapped circuit. Thus, where low current is required and diodes are small, wire is saved reducing the size of the transformer. Where high current is required, the extra wire eliminates the need of two large expensive rectifier diodes.

R. F. filters are included at the input to the power supply to keep external noise from entering the computer and computer noise from entering external circuits. Another noise precaution in this supply is the isolation of input power ground and computer signal ground.

4.5 Reliability Estimates

One of the primary objectives of the SIGS computer design, in addition to low cost, is reliability. Three major factors in the achievement of this goal were: 1) the use of an efficient computer organization using both incremental and whole



NOTES:

1. ENTIRE POWER SUPPLY ENCLOSED IN AN ALUMINUM CASE.
2. FEED-THRU CAPACITORS-SPRAGUE 103P121
3. TANTALUM CAPACITORS ARE TYPE 150D

Figure 4-9. Computer Power Supply

number computing techniques, 2) the use of integrated circuits for all logic mechanization, and 3) the elimination of point-to-point wiring by multilayer etched circuit boards. The MTBF calculations using individual component failure rates are shown in Table 4-1. The estimated MTBF for the SIGS computer is 15,300 hours; further improvements of this figure are anticipated as better quality control methods are incorporated into the newer devices.

Item	No. of Items	Item Failure Rate	Total Failure Rate
		10^6 hrs	10^6 hrs
Logic Circuits	398	0.125	49.75
Transistors	61	0.05	3.05
Diodes	30	0.02	0.60
Zener diodes	12	0.04	0.48
Resistors	113	0.01	1.13
Capacitors	19	0.05	.95
Thermistors	2	0.60	1.20
Crystals	1	.1	.10
Delay line drivers	4	.7	2.80
Transducers	4	1.00	4.00
Connector points	200	.007	1.4
Total			65.46

TFR = Total Failure Rate = $65.46/10^6$ hrs

$$\text{MTBF} = \frac{1}{\text{TFR}} = 1.53 \times 10^4 \text{ hrs}$$

Table 4-1. Reliability Calculations

SECTION V

SUPPORT EQUIPMENT

5.1 Warm-up Provisions

The solid state nature of the computer and careful selection of components have eliminated any requirements for warm-up provisions in the guidance computer.

Associated with the warm-up provision, however, are requirements of system initialization. Certain key quantities concerned with individual missions must be inserted into the computer prior to launch. This information includes such items as present position, target location, burst height, and pitch programming coefficients. The computer loading operation is accomplished by means of GSE and is described in the following paragraphs.

5.2 Ground Support Equipment

A limited amount of ground support equipment is required to support the SIGS computer. The first requirement of the GSE is the capability of initializing the computer. The initializing procedure consists of loading the glass memory and forcing some flip-flops within the computer to particular states. The second requirement is that the GSE be capable of supporting the computer debugging program. The debugging operation is easy to achieve because of the inherent periodic nature of the computer.

Figure 5-1 is a sketch of the control panel. The Display Selector is a seven-position rotary switch that determines the monitor point for the Data Display lights. This means that the lights will be reset once each iteration as a function of the bits emanating from the selected monitor point. It is expected that this monitor point selection capability will aid in fault isolation during checkout.

The Data Display register, containing 14 octal readout lights, is capable of displaying any selected word. A particular word is selected on the basis of a comparison of the computer counters and the state of the Iteration and Word Counter selection switches. Upon receipt of a "Compare" signal, the selected information is gated into the display lights.

The Data Register is a bank of switches that holds information to be gated into the computer upon command. The command signal will be up only when the Enter Data Register button is depressed; the button remains depressed until information has been gated into the computer and the comparison of the co-selection switches and the computer counters is achieved.

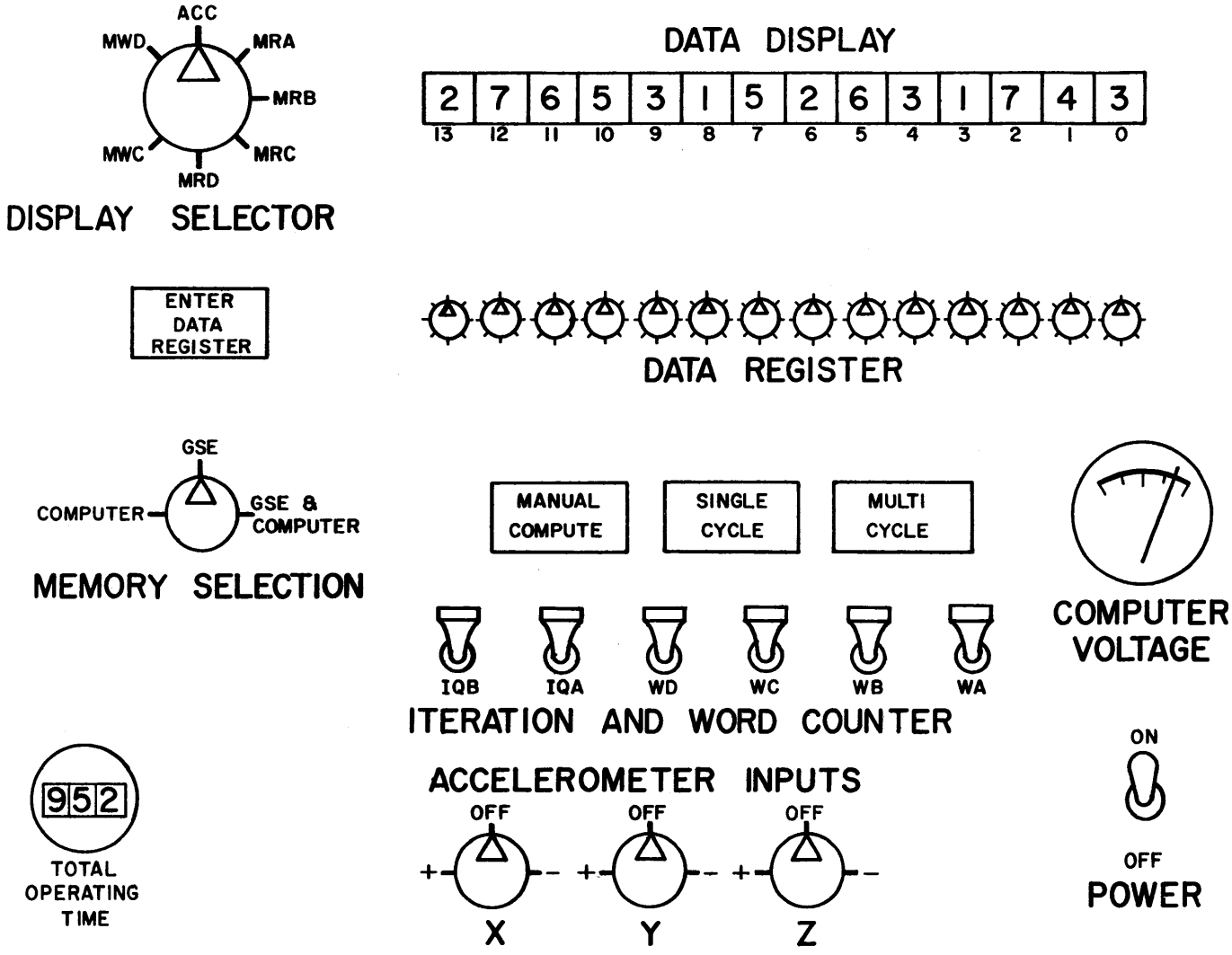


Figure 5-1. SIGS-GSE Control Panel

When the Enter Data Register button is depressed, the Iteration and Word Counter is incremented so that information can automatically be set into the succeeding word of memory. This feature allows filling without resetting the Iteration and Word Counter switches.

The Computer Voltage meter simply reflects the voltage level of the power supply.

The Total Operating Time indicator shows elapsed time.

The Accelerometer Input switches consist of three, three-position switches which allow simulation of an acceleration input. Although a variable rate input could be achieved, it would not really contribute to the capabilities of the GSE equipment and, therefore, will not be implemented.

The Memory Selection switch has three positions that permit a choice of the memory to be filled; these are the computer memory, the GSE memory, or both. The computer memory and the GSE memory are identical; the purpose of the GSE memory is to provide a multicycle mode of checkout. The multicycle mode checkout is highly desirable in that it can be used to reproduce the output signal over a variable period of time. In the multicycle mode, the desired number of iterations can be specified by filling the number of iterations into the time word-slot of the GSE memory.

The Manual Compute button transfers control to the operator or can release control of the computer, that is, allow it to go into a free-running mode.

The Single Cycle button permits the operator to break into the program loop and advance one iteration per depression of the button; which, of course, allows interpretation of the generated data.

5.3 Telemetry Output Provision

The serial nature of the computer information contained in the memory allows for easy access of data for telemetry. Due to the uncertainties in the test vehicle and consequently, the requirement for the types of data required, this proposal does not contain provisions for detailed mechanization of the telemetry box. There are three problems associated with the design of the telemetry box. First, the synchronization problems due to the difference in frequencies of the computer clock and the rate at which the IRIG transmitter can accept new data. The computer memory information frequencies will be in the order of 4 megacycles, whereas the telemetry data rate is in the order of 30 kilocycles. This requires the inclusion of a buffer box which will accept information at higher frequencies and shift out information at lower frequencies. The second problem associated with the telemetry box is that of "flagging" the information so that it can be correctly identified. Associated with this, is the difficulty of

selecting appropriate data from computer memory since it is not possible to readout the total contents of the memory. The third type of problem involves conditioning signals for compatibility with the transmitter unit. Conditioning includes: establishing the correct voltage levels and swings, furnishing necessary power, and establishing necessary rise times through cabling.

In addition to the requirement for transmitting data such as acceleration, velocity, displacement, and gimbal angles, the telemetry unit may be used to measure critical environmental conditions during sled or flight test. For the digital subsystem, acceleration and vibration type of environment are not expected to pose a significant problem. Any difficulty in this area will be determined during the engineering shake, shock, and linear acceleration tests. One of the parameters measured during sled or flight tests will be temperature, since the design relies primarily on thermal-inertia. This will be measured by locating thermocouples at appropriate points, probably between the two logic boards.

SECTION VI

ACCEPTANCE AND ENGINEERING TESTS

6.1 General

Two basic categories of testing will be accomplished at AC Spark Plug prior to delivery of the computers herein proposed. These tests are intended to verify to LSI the quality of the subsystem equipment prior to conducting system tests at LSI.

6.2 Acceptance Tests

A computer acceptance specification will be prepared by AC Spark Plug and submitted 30 days prior to the scheduled acceptance of the first computer. This specification, subject to mutually agreed modification as the program dictates, will be used to accept all deliverable computers.

The acceptance test cycle will include, at least:

1. Visual inspection for compliance to the computer drawings.

2. Vibration while operating in a diagnostic routine to thoroughly exercise all of its circuitry. The GSE, as proposed, will be utilized as the monitoring tool. Vibration criteria for this test shall be:

Input	Input Axes	Time
Linear:		
5 g, 10 - 3000 cps	3 major axes	3-minute logarithmic sweep (up only)
3 g at 7 cps	3 major axes	30 seconds

3. Additional non-vibrating tests will include application of representative voltages to the computer and the various outputs monitored with the GSE.

All operating time records on each computer will be recorded and submitted as part of the permanent records to accompany each computer.

6.3 Engineering Tests

Engineering tests to be conducted on the second computer prior to delivery to LSI will be performed to demonstrate the adequacy of the mechanical design when subjected to specified environments. Complete test procedures will be detailed in a specification to be submitted 30 days prior to beginning the engineering tests. Criteria for these tests will include, but will not be limited to the following.

6.3.1 Vibration

While operating the computer shall be subjected to the vibration specification described in Paragraph 6.2 above.

6.3.2 Acceleration

The computer will demonstrate the ability to withstand the following acceleration environments:

1. Longitudinal and vertical - 10 g acceleration +2 g noise vibration,
2. Transverse - -6 g acceleration +2 g noise vibration.

6.3.3 Shock

The computer will be subjected to three 20 g shocks (duration 11 milliseconds) in each direction along three mutually perpendicular axes. These shocks will be applied through the normal mounting points of the computer.

6.3.4 Ambient Temperature

The computer will be operated and its performance monitored while undergoing a temperature cycle test ranging from $+40^{o}$ F to $+160^{o}$ F.

SECTION VII

DEVELOPMENT SCHEDULE

7.1 General

Figure 7-1 presents the major milestones planned to occur during the demonstration phase of the Simplified Inertial Guidance System program.

It is separated into hardware and data items. The computer and GSE equipment to be delivered are described elsewhere in this proposal. Data and reports criteria is summarized below.

7.2 Data and Reports Criteria

In accordance with the RFP requirements, drawings, specifications, and parts lists will be prepared in accordance with good engineering practice. Drawings, although not full Military Specification, will be sufficient, in laboratory drawing format, to define the hardware to be delivered.

Reports will be informal progress letters to allow easy integration into the LSI report to APL, and will be completed on or about the 15th of each month, covering the progress of the previous month.

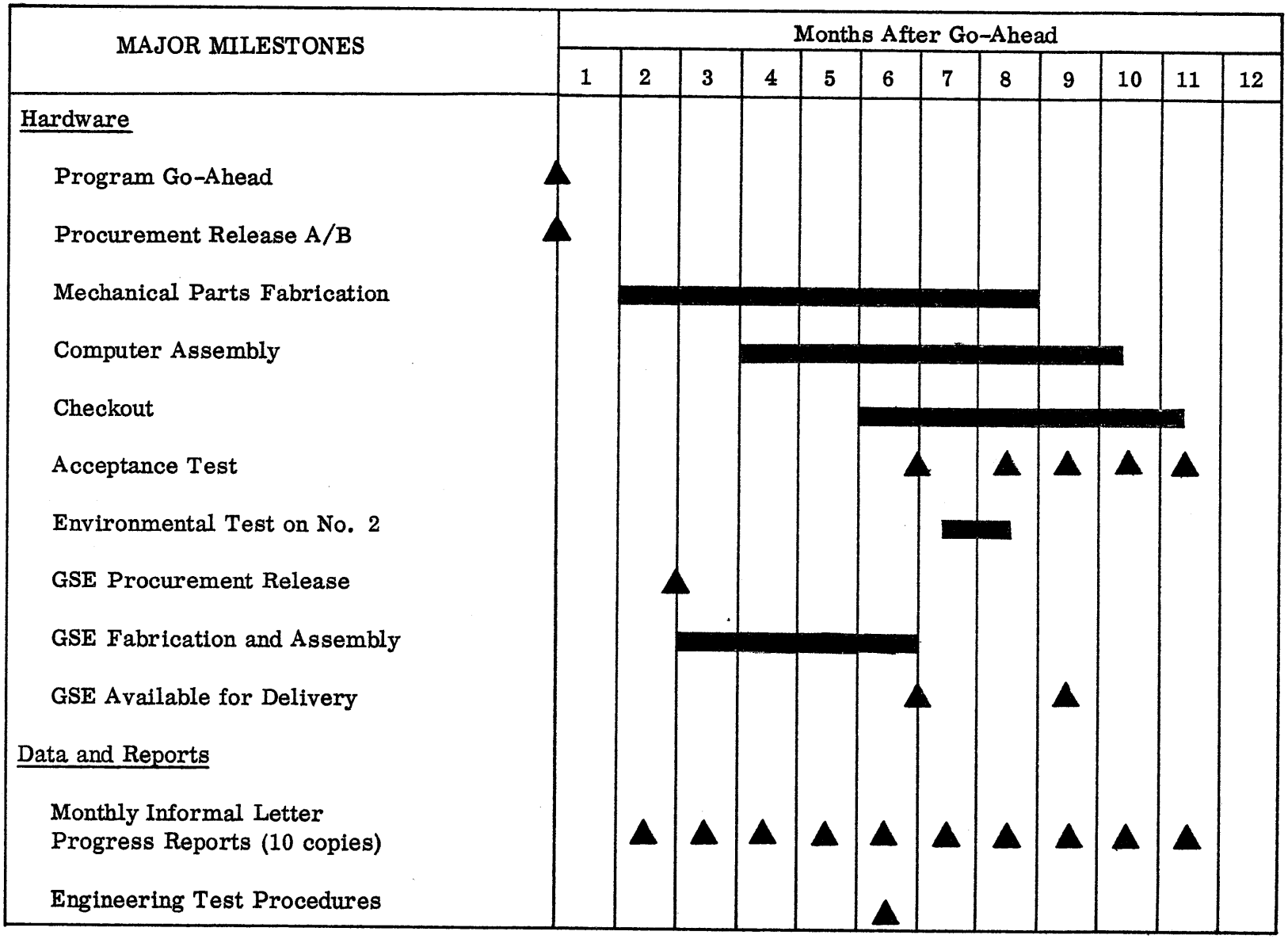


Figure 7-1. SIGS Computer Milestones

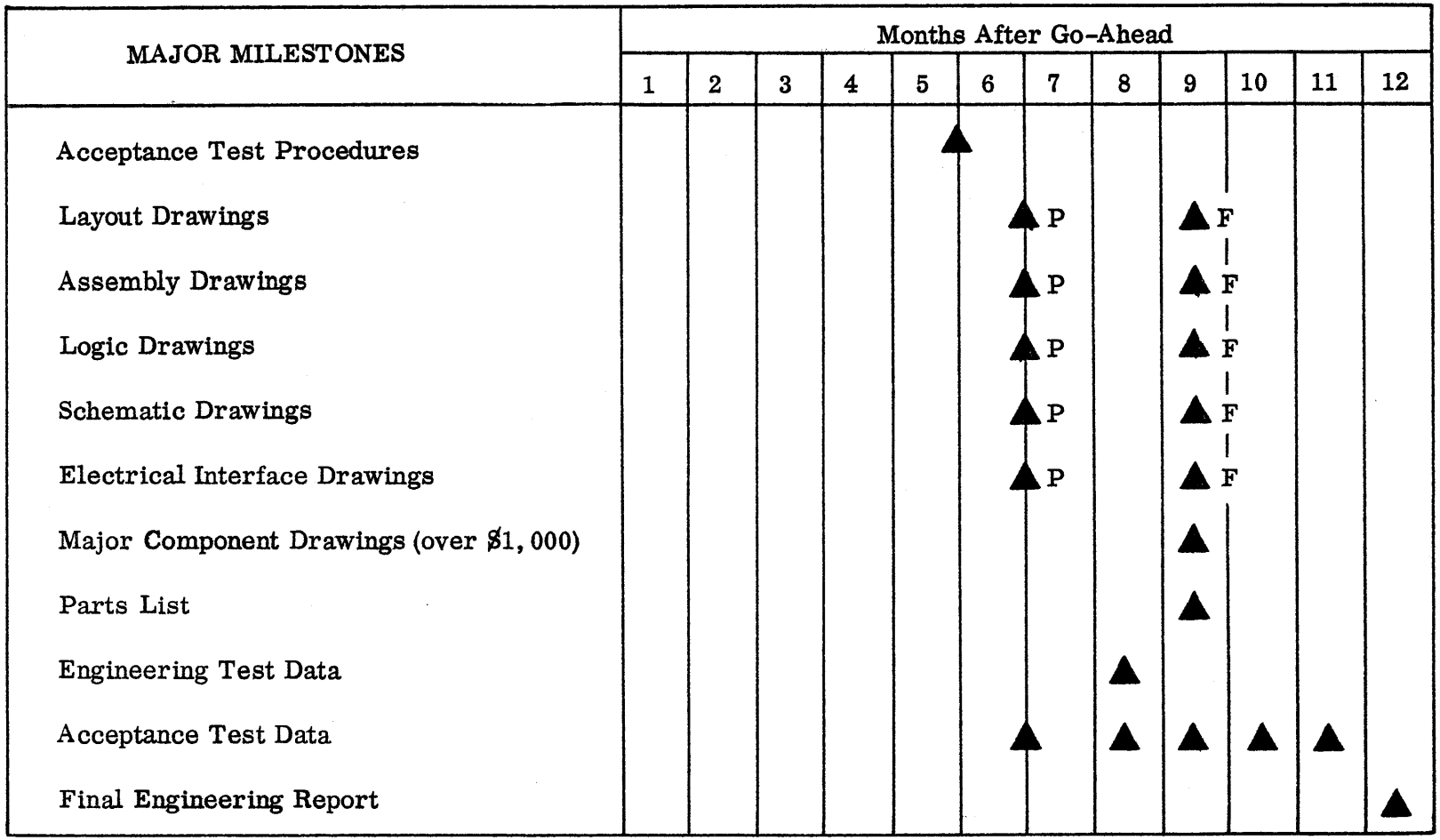


Figure 7-1. SIGS Computer Milestones (contd)

SECTION VIII

PERSONNEL AND FACILITIES

8.1 Background and Facilities

AC Spark Plug possesses a unique capability to undertake the prototype development and production fabrication effort required to supply the digital computer for all phases of the Simplified Inertial Guidance System Program.

A strong computer development organization and facilities for producing and testing prototype quantities exists within the Los Angeles R and D Laboratory. It is in this laboratory that the initial phase of the program will be conducted.

Closely tied to the activities of the Research Laboratories, the Milwaukee Operation has a long standing record of proficiency in the production of precision military guidance and navigation equipment.

These capabilities complement one another and will, therefore, bring to the program the required developmental flexibility and precision production capability.

8.1.1 Computer R and D Activities

Primary emphasis has, since the establishment of the Computer R and D organization in 1959, been placed on basic state of the art improvements in computer technology. Eight major areas of digital technology are currently being directed toward a more efficient and reliable guidance system computer. These eight areas are: computer functions in advanced systems, logic design, circuit and subsystem design, input-output techniques, programming techniques, reliability techniques, auxiliary digital equipment, and circuit fabrication. They are discussed below.

a. Computer functions in advanced systems. Computer requirements for particular systems are being analyzed and studies are being made of general factors which determine whether a particular system function should be included within the computer.

b. Logic design. Techniques are being developed to effectively utilize high component speeds to improve accessibility to delay line memories, and to make use of the advantages and limitations of new logical components.

c. Circuit and subsystem design. Studies are being made in the areas of advanced memory systems, more effective configurations for transistorized logic circuits, and techniques for exploiting the advantages and minimizing the difficulties of using new circuit devices.

d. Input-output techniques. Studies are being made of techniques for conversion between analog and digital forms of information which will lead to simpler and more efficient input and output equipment.

e. Programming techniques. Development of advanced computer programming techniques are underway to improve the programs used in guidance computers and to make use of existing computers in the design and development of new systems.

f. Computer reliability techniques. Studies are being made of techniques which will provide substantial improvements in effective computer reliability with only moderate increases in complexity and physical size. A combination of several different techniques will be needed to accomplish this objective. Areas of concentration for this purpose include: computer organization, logic design techniques, special programming methods, and new circuits and devices.

g. Auxiliary digital equipment. Equipment used for operation and support of the solid-state MAGIC computer was developed and built during 1962. Further studies are underway of equipment which will utilize the guidance computer to aid in the checkout of entire guidance systems.

h. Circuit fabrication. A number of approaches to the problem of reducing physical size are being studied, including experimental evaluation of micro-miniature elements for immediate system applications, development of vapor deposition techniques for component fabrication, and studies of interconnection arrangements for complicated miniaturized systems.

The overall objective in advanced digital circuit fabrication is to provide techniques for the fabrication of electronic circuits which will lead to substantial reduction in physical size or significant improvements in reliability, or both. Although it is expected that these techniques will eventually be applicable to a wide variety of circuits, work at this time is directed toward digital circuits since, in many ways, the problems here are better defined and more easily controlled. The program includes three different kinds of effort. The first is concerned with a thorough evaluation of components and devices obtained from other manufacturers that might provide special advantages to the AC Spark Plug Division. The second is devoted to study and improvement of techniques for assembling electronic components into digital assemblies. The third is devoted to the development of techniques for fabricating circuits by vapor-deposition processes. The objectives of this latter effort are: close control of circuit parameters, interconnection methods in keeping with miniature circuits and large component counts, and fabrication of thin-film devices. Micromodules are being produced with the aid of a miniature welder designed specifically for this work.

8.1.1.1 MAGIC Computer

Having gained considerable experience in the area of inertial guidance, it was a natural extension of AC Spark Plug's capability to design and develop the MAGIC Digital Computer. This decision was prompted further by the expanding role of airborne digital computers whereby initially they were used for navigation; later they were employed for navigation, steering computations, instrument calibration, preflight checkout, staging control, thrust cut-off computations, and warhead pre-arming computations.

The history of the MAGIC computer extends over approximately a three-year span. It was the outgrowth of several studies of particular computer techniques and of system studies of missile and earth navigation inertial guidance systems. The computer has been completely fabricated, assembled, and debugged. It has been, for some time, used in an extensive program of laboratory evaluation.

Four major objectives of the MAGIC computer endeavor are of particular interest.

a. The computer was designed to meet all the requirements of both earth navigation and ballistic missile, stellar-inertial, guidance systems.

b. The computer demonstrated the present feasibility of using molecular electronic devices in a full-scale system.

c. The computer demonstrated the performance that can be obtained from a magnetic core memory when operated in a serial mode.

d. The computer incorporated a logic design that is matched specifically to the computer requirements for a real-time guidance system.

These four objectives were chosen in recognition of specific problem areas in airborne computer technology.

A second generation of the MAGIC computer has earned acceptance as part of the Low Altitude Inertial Navigation System (LAINS, Contract AF 33(657)-11601). This computer is an advanced airborne guidance and navigation computer using the latest techniques and devices commensurate with high reliability, performance, flexibility, weight, power, and availability. The MAGIC II computer is a lightweight, general-purpose machine using both destructive-and nondestructive-readout, random-access, core memories. It is anticipated that much of the logic and hardware design will be applicable to a wide variety of future guidance systems.

8.1.1.2 TAWC

Another series of digital computers has evolved from the need to satisfy the low-cost lightweight requirements imposed upon computers utilized in applications such as tactical weapons, attitude control, in-flight data reduction and airborne navigation. Reduced size, weight, and cost consistent with required flexibility were paramount criteria used in developing the TAWC (Tactical Weapons Computer) herein proposed. These criteria, coupled with a strong computer research background, have enabled a digital computer to be developed that will completely satisfy the requirements of the Simplified Inertial Guidance System Program.

8.1.2 Production Capability

The ability to adapt the techniques of high-volume production to the manufacture of precision airborne electronic systems has been acquired by AC Spark Plug over the past 15 years, since the Milwaukee Operations has been in existence. Today AC Spark Plug has the skilled personnel and specialized equipment to meet the state-of-the-art requirements of missiles and space vehicles.

The skills and facilities required for the production of the SIGS computer are logical extensions of those required for production of earlier systems, such as THOR, TITAN II and III, and APOLLO, and are exactly those required for the digital computers for the LAIN system.

These include precision machining, multilayer circuit board fabrication, micro-miniaturized circuit design and production, component and logic circuit testing as well as total computer testing. Each of the above is required for the deliverable items, in addition to the facilities required for flight proofing and environmental testing. This section reviews AC Spark Plug's capabilities in each of these areas.

The Milwaukee Operations total about 1.6 million square feet of floor space and approximately 8,000 employees. The Oak Creek Facility, shown in Figure 8-1, has a total floor space of over 750,000 square feet. This plant was designed specifically for the manufacture of precision equipment and includes a number of temperature-controlled and dust-free areas for the fabrication, assembly, and test of extremely precise parts and components.

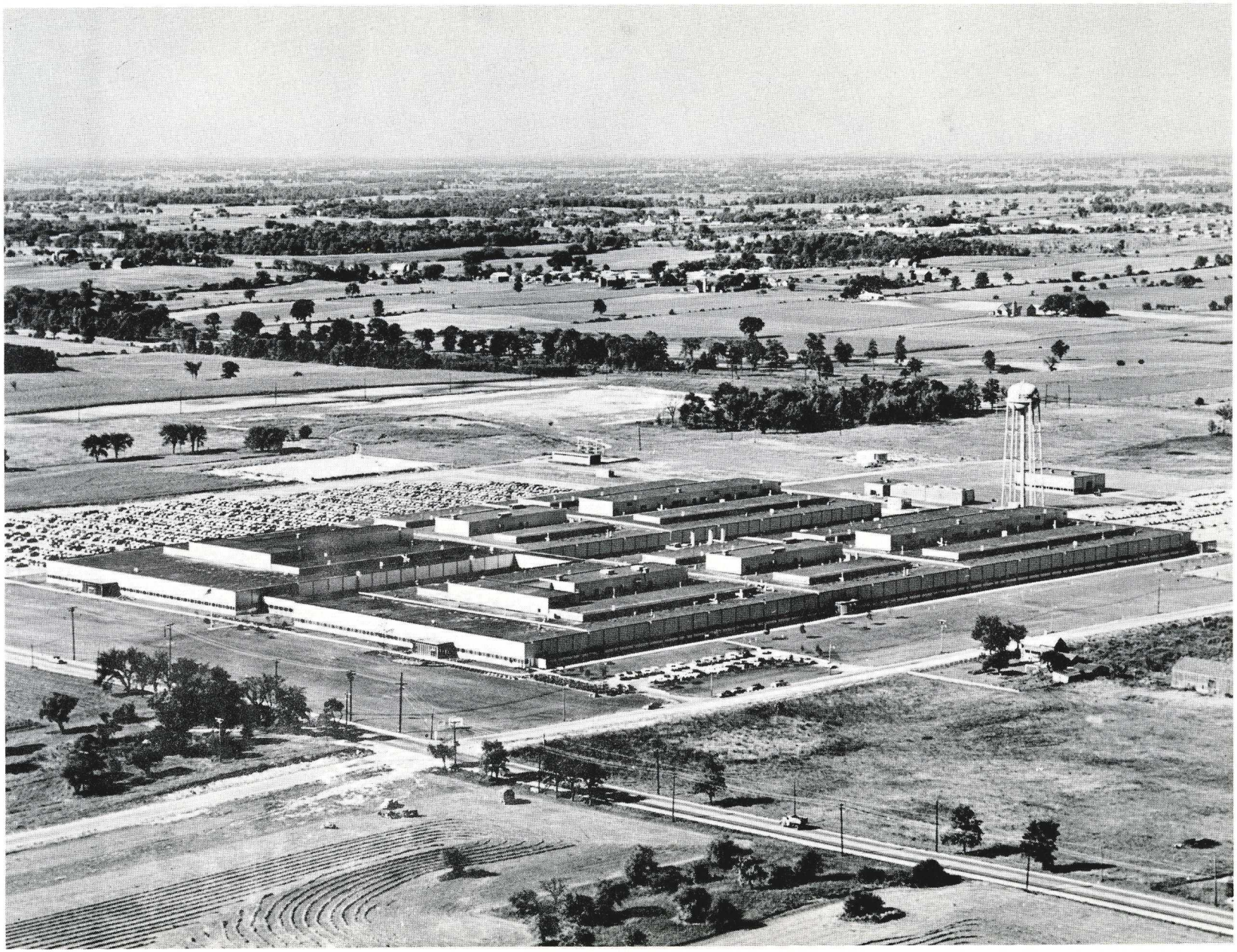


Figure 8-1. AC Spark Plug Division — Milwaukee Oak Creek Facility

8.1.2.1 Machining

8.1.2.1.1 General-purpose machining

The machining facilities include approximately 400 varied machine tools for machining operations on electrical and electromechanical precision parts. It has been the policy of AC Spark Plug Division to distribute these machines in accordance with current production needs.

8.1.2.1.2 Precision machining

Ultra-precision operations, peculiar to the industry, have been established in several areas. A universal in-line production capability makes it possible, with a minimum amount of tooling, to quickly adapt the machine tools to an economical production run. Included in this group of equipment are machine tools such as the Heald No. 422 and the Excello No. 17-A, along with several special boring machines manufactured by AC Spark Plug, which are equipped with air gages to give the operator control of the size of the finished product.

8.1.2.2 Printed Circuits

AC Spark Plug's printed circuit facility began production in January of 1959. Approximately 3,000 square feet are allocated to negative preparation, printing, and fabrication of the printed circuit boards. The manufacturing facilities include a precious-metal plating operation.

The photo-etch technique chosen yields sharp definition and close tolerances of the photographic image. A complete laboratory is devoted to the development and improvement of the processes used. The laboratory includes a 24-inch process camera and its associated dark room as well as printing and etching equipment. Figure 8-2 shows the vacuum contact printing frame in use.

The method used for circuit board fabrication depends upon the quantity and the type of board material. When produced in small quantities, epoxy fiberglass boards are rough drilled, and the profile is then finished by use of a pantograph router. Regular production military boards are consistently and accurately drilled by a tape-controlled drill with four drill heads shown in Figure 8-3.

An intensive evaluation and development program was initiated with the advent of multilayer circuit boards. First an evaluation was performed on multilayer boards purchased from available manufacturers. Second, a production capability was developed for multilayer circuit boards. The test boards were designed so as to fully check the plated through-holes which form the interlayer connections as well as the printed circuits themselves. A complete environmental evaluation program was

Figure 8-2. Vacuum Contact Printing Frame

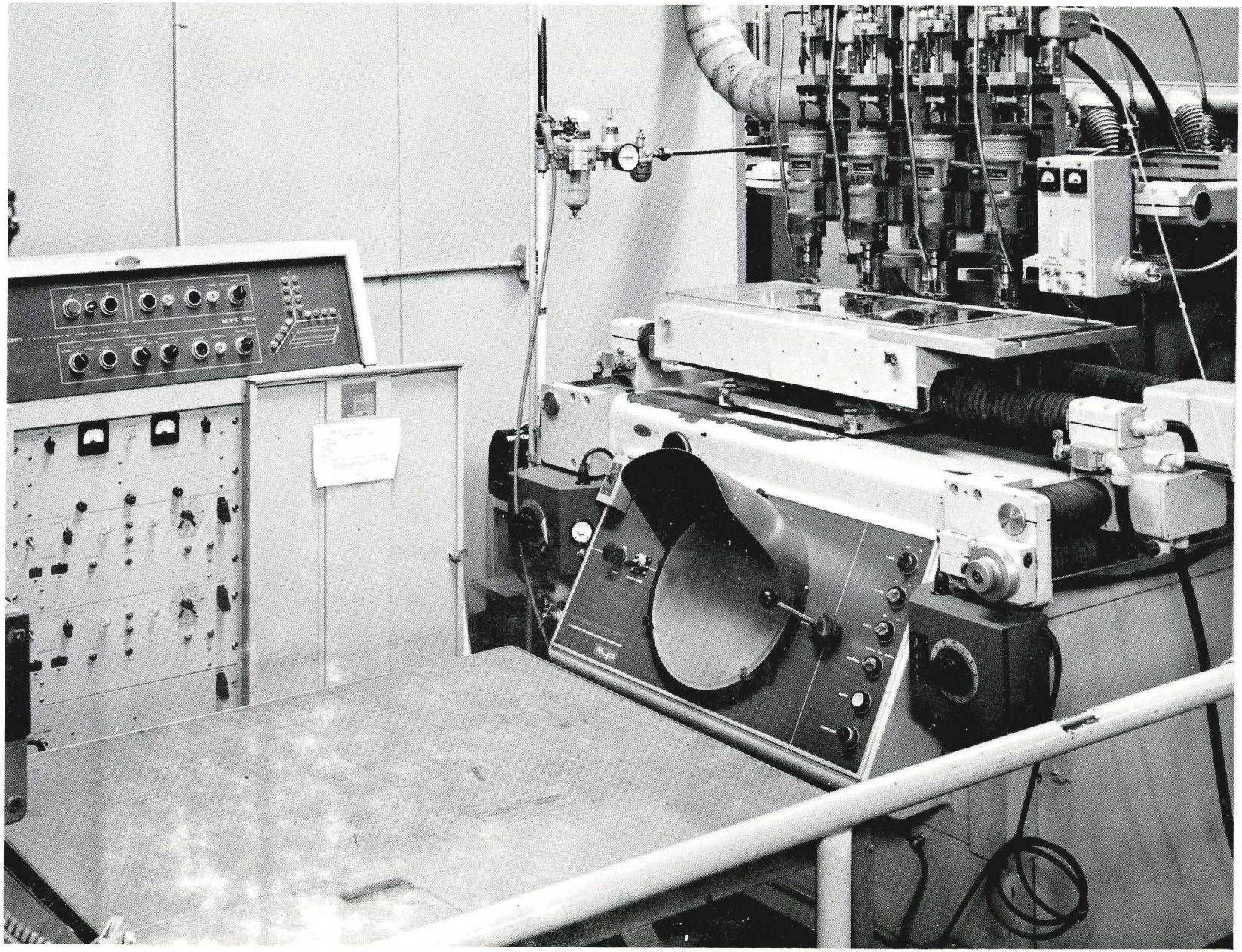


Figure 8-3. Tape Controlled Drill

carried out including thermal shock and vibration. An example of one of the multilayer test boards built by AC Spark Plug is shown in Figure 8-4. Multilayer boards such as this are being supplied by AC Spark Plug for the LAINS computer presently being produced.

8.1.2.3 Quality Assurance

The nature of AC products demands high assurance of successful operation at first-unit delivery. The limited numbers of units built, high cost per unit, short lead time, and early obsolescence preclude extensive follow-on verification, redesign, and retooling to eliminate areas of weak quality. The number of elements contained in a system, and the total dependence on each element for successful system operation, make quality an even more significant factor.

AC Spark Plug's Quality Assurance organization has evidenced a functional growth that parallels technological growth. Quality Assurance is a part of the Reliability Division, a staff-level organization. Many changes have been made in this area over the past few years, such as utilization of statistical quality control methods, in-process controls, and improved evaluation equipment and techniques. Furthermore, production surveillance has increased to where there is an average ratio of 1 inspector to 5 production employees.

As part of the expanded scope of the Quality Assurance activity, a Quality Engineering Group has been formed which includes QA Planning, Quality Engineering Analysis and Audit, Electrical Measurements Certification, and Mechanical Measurement Certification functions. The Metrology Laboratory (whose standards are traceable to the National Bureau of Standards), the Electrical Secondary Standards Laboratory, and employee training programs are but a few of the accomplishments and responsibilities of this group.

At present, the Quality Assurance system is based on the requirements of MIL-Q-9858, and is approved by the U. S. Air Force. In addition, certain areas have been adjusted to conform with the more rigid requirements of MIL-Q-21549A. A Navy survey in this regard gave AC Spark Plug's system 521 points out of a possible 560. AC Spark Plug is currently expanding its system to conform with the requirements of NPC 200-2, as part of its APOLLO effort for NASA.

8.1.2.4 Environmental Testing

The component and systems environmental test laboratories provide test facilities and a staff of specialists for evaluation of equipment under simulated environmental conditions equal to or more stringent than actual operating conditions. The laboratories are equipped with the following major facilities.

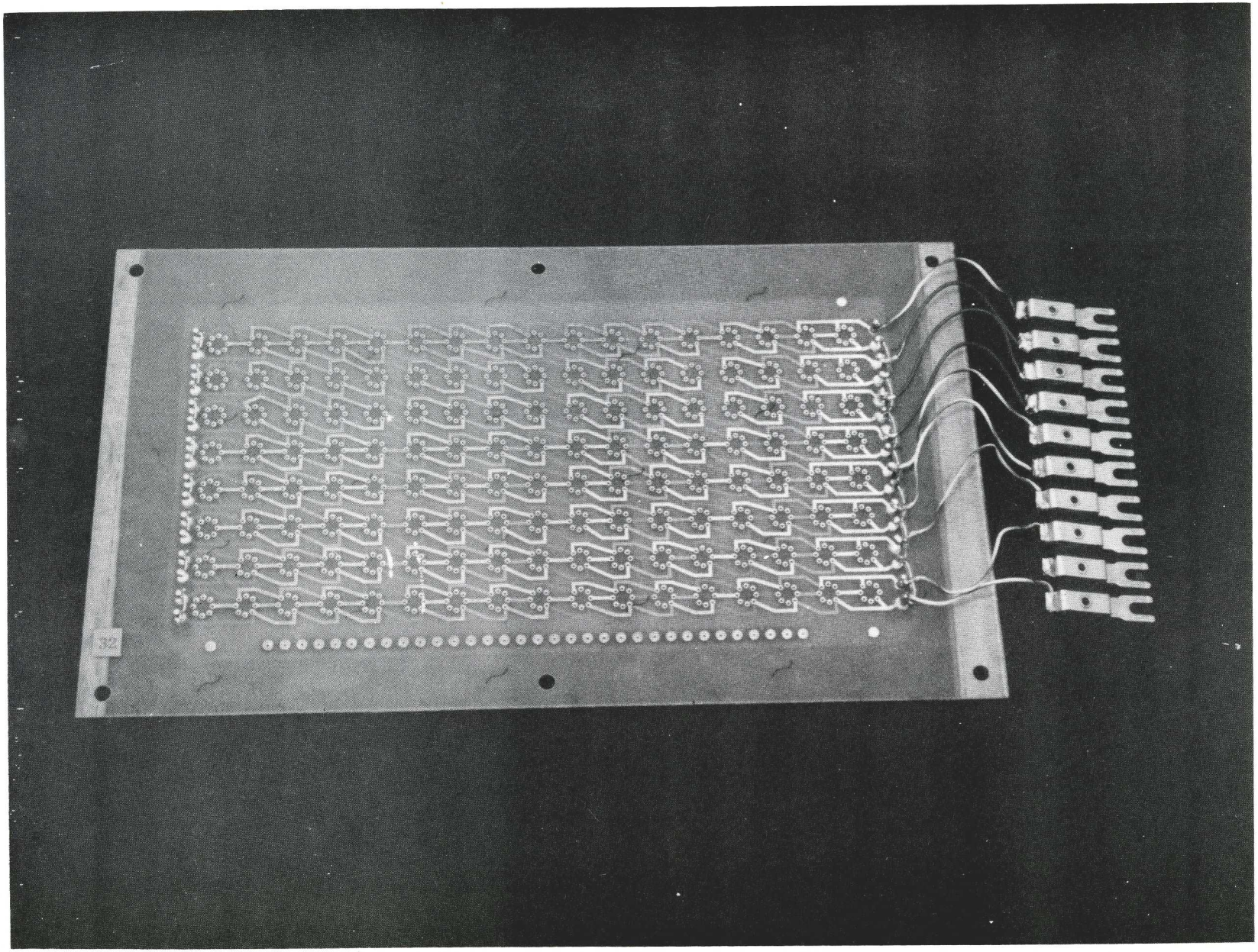


Figure 8-4. **Multilayer Circuit Board**

Vibration Test Facilities - 2-15,000 pound force, 2 to 2,000 cps vibration heads - capable of sinusoidal or random noise

Explosion Test Chamber - 28 cubic foot - meets MIL-E-5272C requirements - including variable altitude and temperature

Walk-in Temperature-altitude Vibration Test Chamber - - 100°F to + 200°F - altitude to over 200,000 feet

Walk-in Temperature-humidity Test Chamber - - 100°F to + 300°F humidity controlled from 20 percent to over 95 percent

Ultra-high-altitude Test Chamber - to below 0.5 micron of pressure in ten minutes

Centrifuges - 2 large centrifuges - one 6-foot radius and one 100-inch radius

8.2 Organization and Personnel

8.2.1 General

The proposed program will be conducted by a select group of personnel from the AC Spark Plug Computer Research and Development Laboratory at Los Angeles. They will be assisted by specialists in the necessary disciplines from the AC R and D organization.

In the following paragraphs, the key individuals who will work directly on the program are identified. Relationships of this group to the overall Milwaukee Operations are brought out. Resumes of all key personnel, whose qualifications bear upon the successful implementation of the program, are also presented.

8.2.2 Program Organization

As presently planned, this program will be directed by Mr. W. S. Fujitsubo. The fabrication and testing of the equipment to be delivered on the prototype program will primarily be accomplished at the Los Angeles Computer R and D Laboratory. Printed circuit boards and other sub-assemblies will be manufactured in Milwaukee utilizing the capabilities discussed in the Facilities Section.

To maintain a smooth flow of that portion of the effort to be accomplished in Milwaukee, Mr. Ralph Brown of the Computer Development Department in Milwaukee will act in a liaison capacity. As the program progresses toward the production phase additional planning and preparatory activities will be executed by this department.

Mr. E. Malavolti will report to Mr. Fujitsubo as SIGS Computer Project Engineer. Both of these men have been instrumental in the development of the proposed computer and will coordinate and direct the activities of laboratory personnel, now available, to the successful completion of the Demonstration Phase of the SIGS Program. The organization proposed to conduct the program is presented in Figure 8-5. Figure 8-6 depicts the AC Spark Plug Organization Chart. Resumes follow.

WILLIAM S. FUJITSUBO - Program Director

Mr. Fujitsubo received the Bachelor of Business Administration and Master of Business Administration degrees from the University of Michigan in 1950 and 1951, respectively, and a B. S. degree in Electronic Engineering from the University of California at Los Angeles in 1956, where he has also done postgraduate study. He is a member of Tau Beta Pi, the Honorary Engineering Society.

Mr. Fujitsubo has had nine years of engineering experience in the field of analog and digital computers. His experience includes work at the University of California at Los Angeles as problem leader on an electronic and mechanical differential analyzer. He was also Systems Engineer on the NCR 304 Data Processing Computer while with the National Cash Register Company. While employed at Litton Industries, Mr. Fujitsubo was the System Project Engineer on the A2F Attack Navigational Computer, the AIDE IV Attack Navigational Computer, Logic Designer and Programmer for the MIT Skipper Guidance Computer and Head of the Logical System Section. He has also served two years as Engineering Officer with the U. S. Coast Guard after receiving a commission from the OCS program at the U. S. Coast Guard Academy.

Mr. Fujitsubo joined AC Spark Plug Division in April 1960 and was appointed to his present position of Section Head, Logical Design and Programming Section in March of the following year. Mr. Fujitsubo's responsibilities in that position are in the area of system design, logic design, and programming of advanced digital computers for airborne and space guidance systems.

Patents held or pending for Mr. Fujitsubo include the Minigram Uniregister Incremental Computer, "Nonlinear" extrapolation technique, and Self-Compensation Color Storage Technique.

EMIL MALAVOLTI - Project Engineer

Mr. Malavolti received the BSEE degree from the University of Illinois in 1960. He has accrued additional credits toward the MSEE.

Prior to joining AC Spark Plug, Mr. Malavolti participated in the logic design of the GAM-87A Guidance Computer at Nortronics.

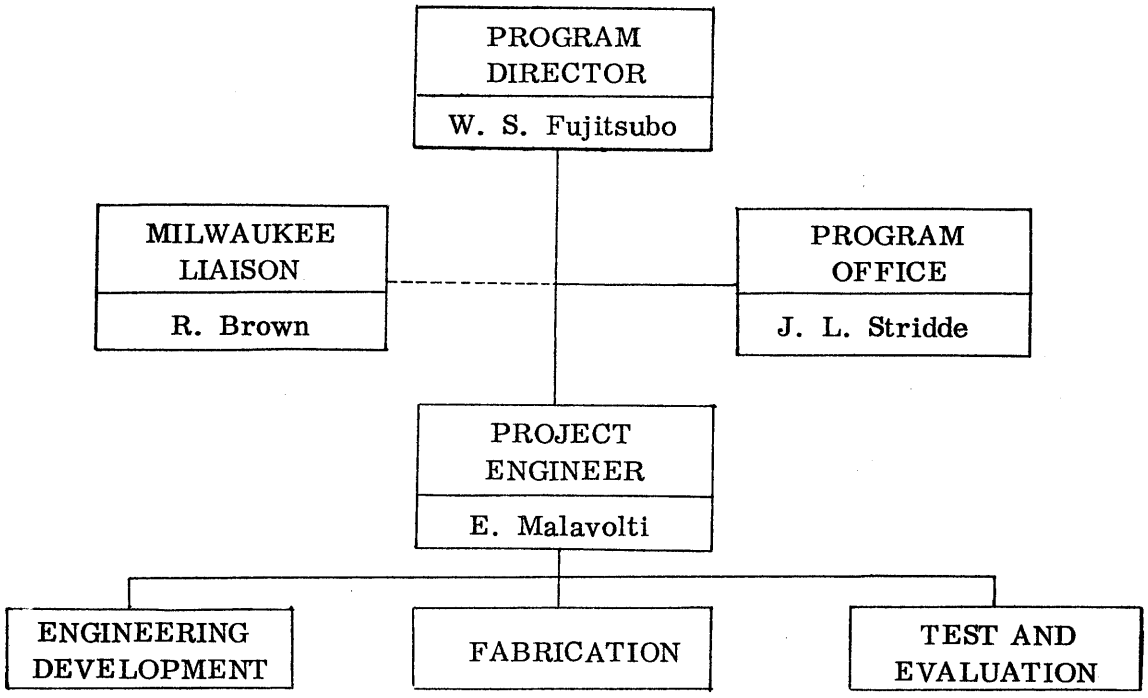


Figure 8-5. SIGS Program Organization

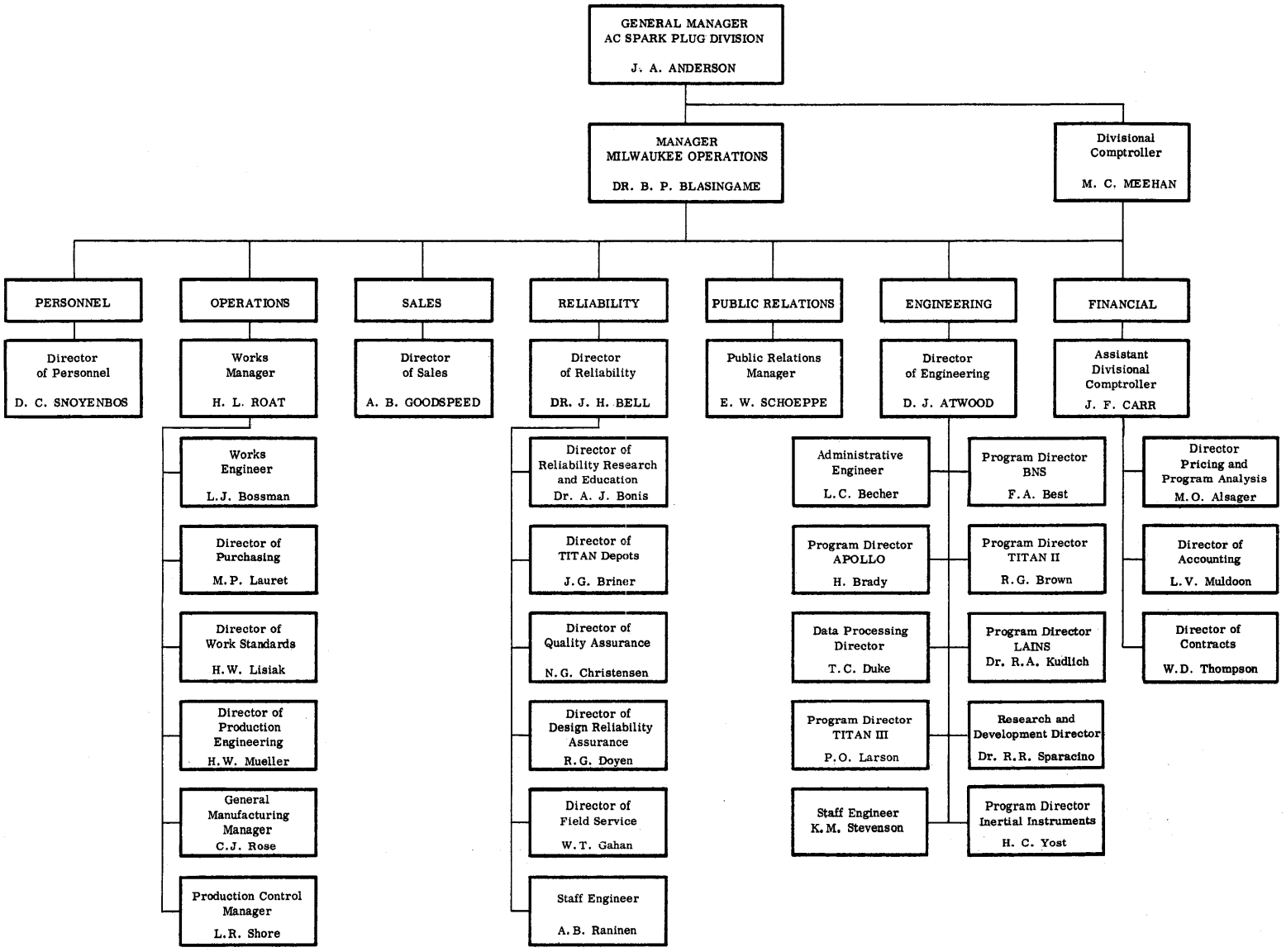


Figure 8-6. AC Spark Plug Organization

He has been active in the Logic Design and Programming Section concerned primarily with the detailed design of the TAWC. His assignments prior to the current effort have included debugging the interface between the PB 250 computer and advanced AC Spark Plug inertial platforms, and development of hybrid incremental whole word computers for high accuracy warhead delivery systems.

JACK L. STRIDDE - Head, Program Office

Mr. Stridde received the Bachelor's degree in Business Administration from Drake University in 1950.

He began his professional career at AC Spark Plug Division, where he has accrued extensive experience in engineering administration, sales and contracts. Positions he has held include: Program Office Coordinator on the Stellar Inertial Bombing System and RASCAL programs, Business Manager for the THOR program, and Product Manager for the TITAN program. For the past two years, Mr. Stridde has been concerned with administration of R and D programs of the AC Research and Development Laboratory operations. These duties have included those of Program Office Head for the Dormant Inertial Guidance System study program, and the TRFCS study program.

In the course of his duties at AC Spark Plug, Mr. Stridde has gained wide experience in in-plant coordination and control of engineering programs, in the preparation and presentation of program information, and in the conducting of liaison and negotiation with Air Force procurement agencies.

RALPH B. BROWN - SIGS Computer, Milwaukee Liaison

Mr. Brown received the BSEE degree from the University of Kentucky in 1951 and the MSEE from the same university in 1953. He then joined the Philco Radio Corporation as a Senior Engineer. In 1955 he was promoted to Group Engineer in charge of the Airborne Control Computer Group. In 1957, Mr. Brown was appointed Senior Project Engineer at Delco Radio Division of General Motors Corporation in charge of Delco's semiconductor evaluation program. From 1958 to October 1963 he served as Manager of the Semiconductor Military Projects Department covering two general areas: development of solid-state precision power supplies for missile and space applications, and development of transistorized digital equipment.

In November 1963, Mr. Brown was transferred to AC Spark Plug, where he is presently responsible for effecting the transition of digital packaging processes and techniques developed by the Research and Development Laboratories to production.