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ELECTRONIC DESIGN®

A PENTON PUBLICATION U. S. $10.00 DECEMBER 5, 1991

POWER-MISER OP AMP DRAWS CURRENT ONLY WHEN AWAKENED

- SPECIAL REPORT: THE PROS AND CONS OF VHDL
- TEST AND MEASUREMENT UPDATE: COMMUNICATIONS TEST EQUIPMENT
- MULTIPLE PROCESSORS ADD MUSCLE TO DMM

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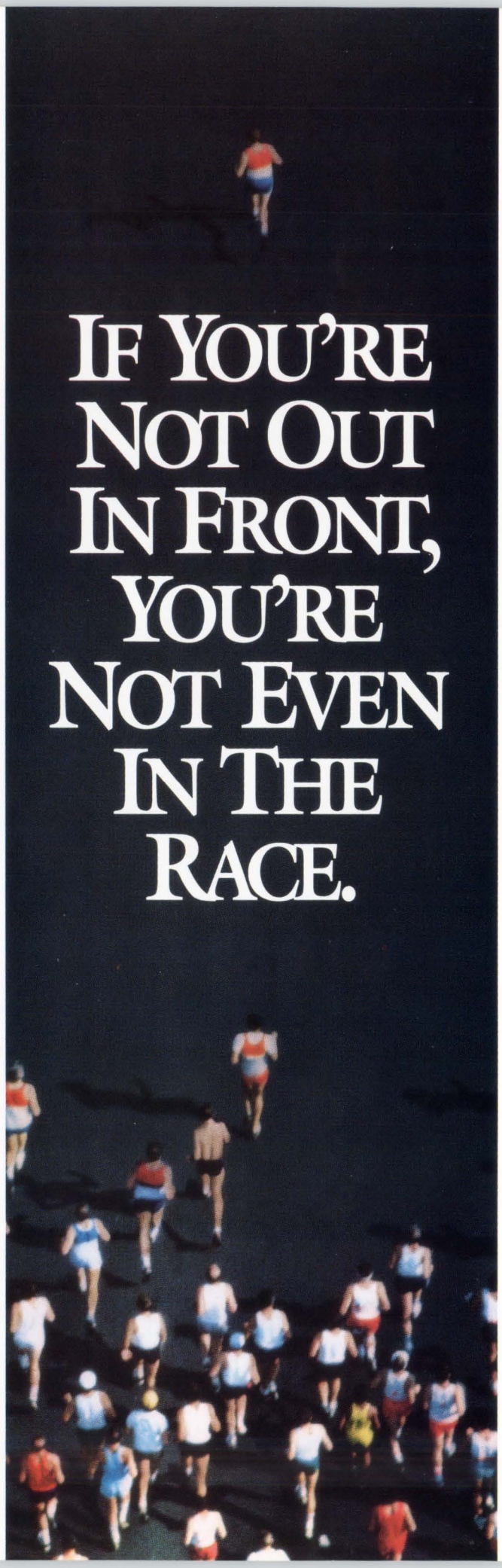

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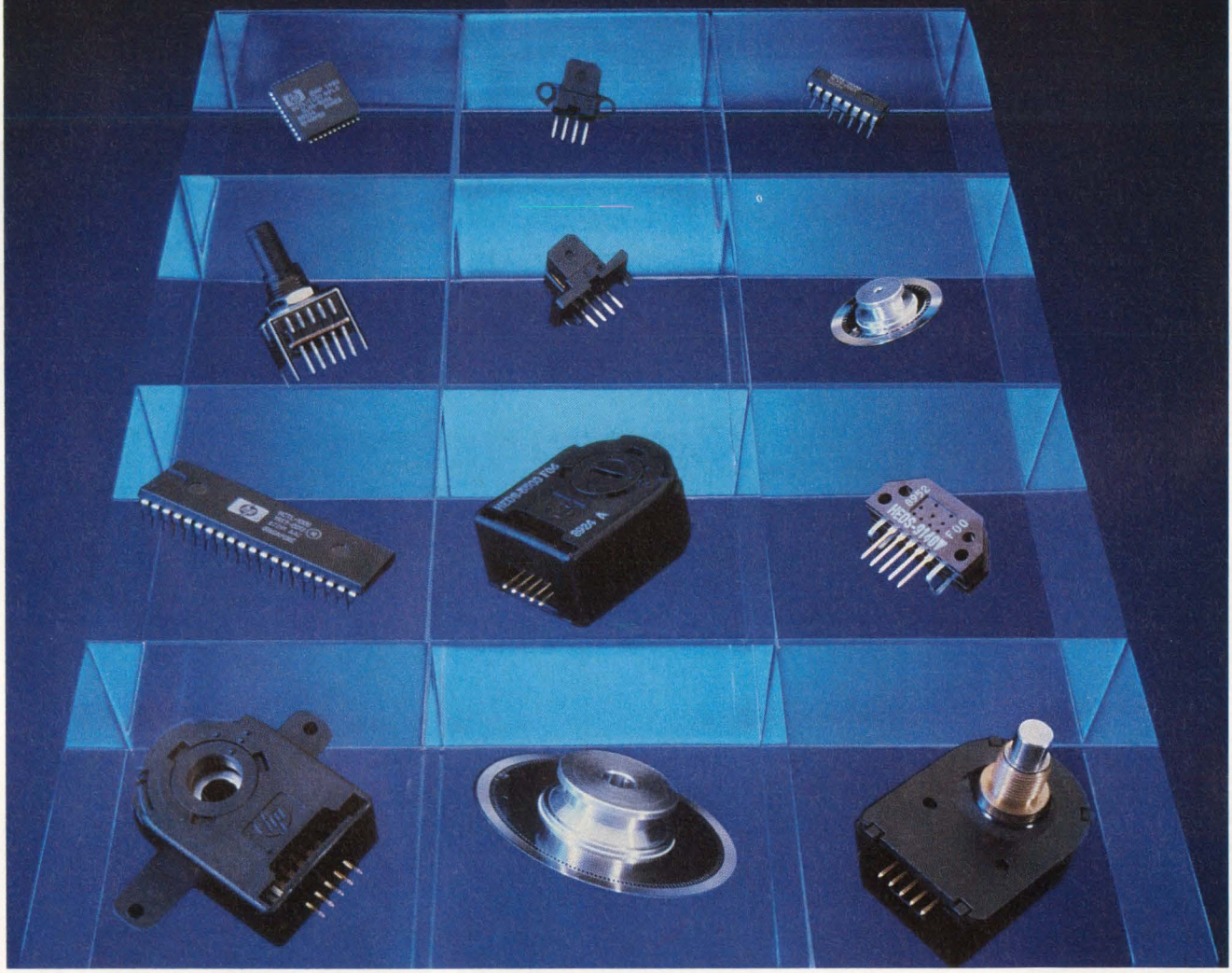

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CIRCLE 218

The Yellow Page

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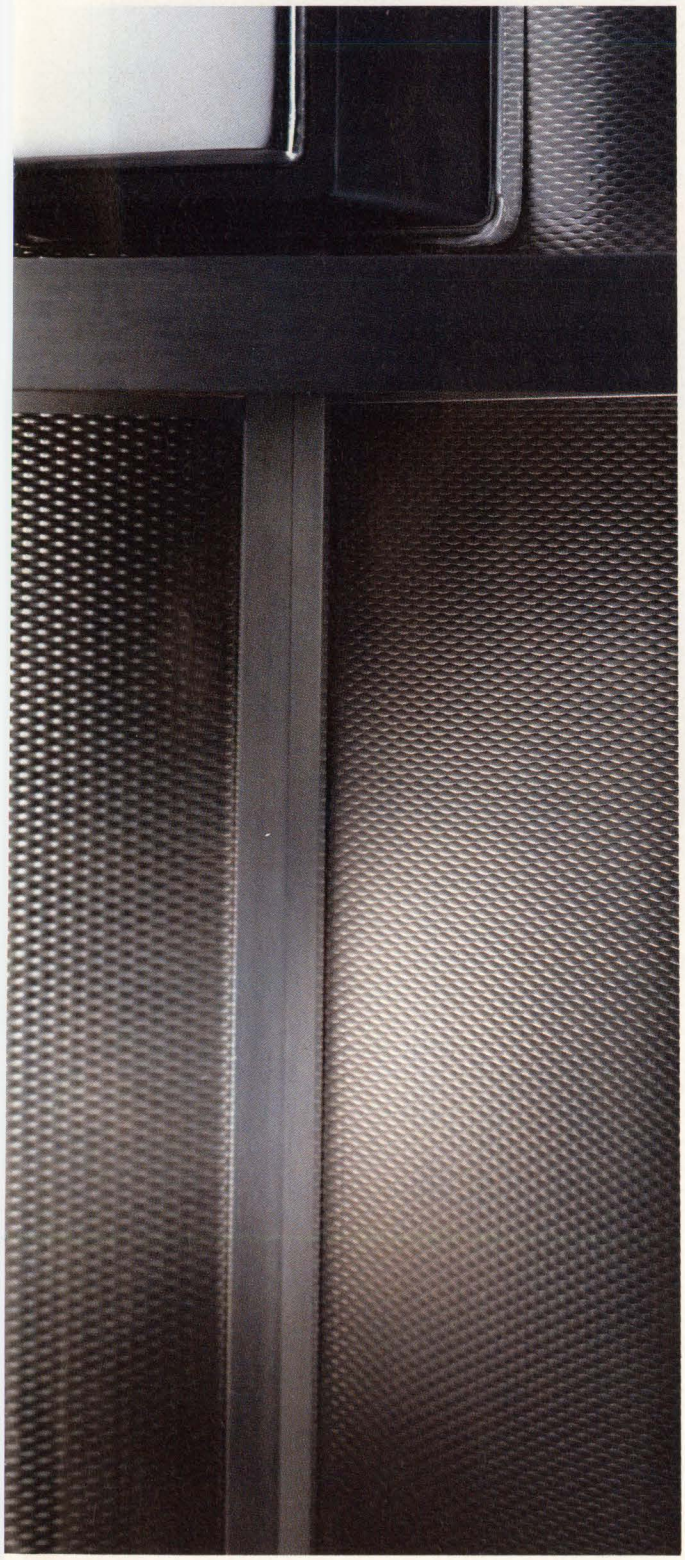

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DECEMBER 5, 1991 VOL. 39, NO. 23

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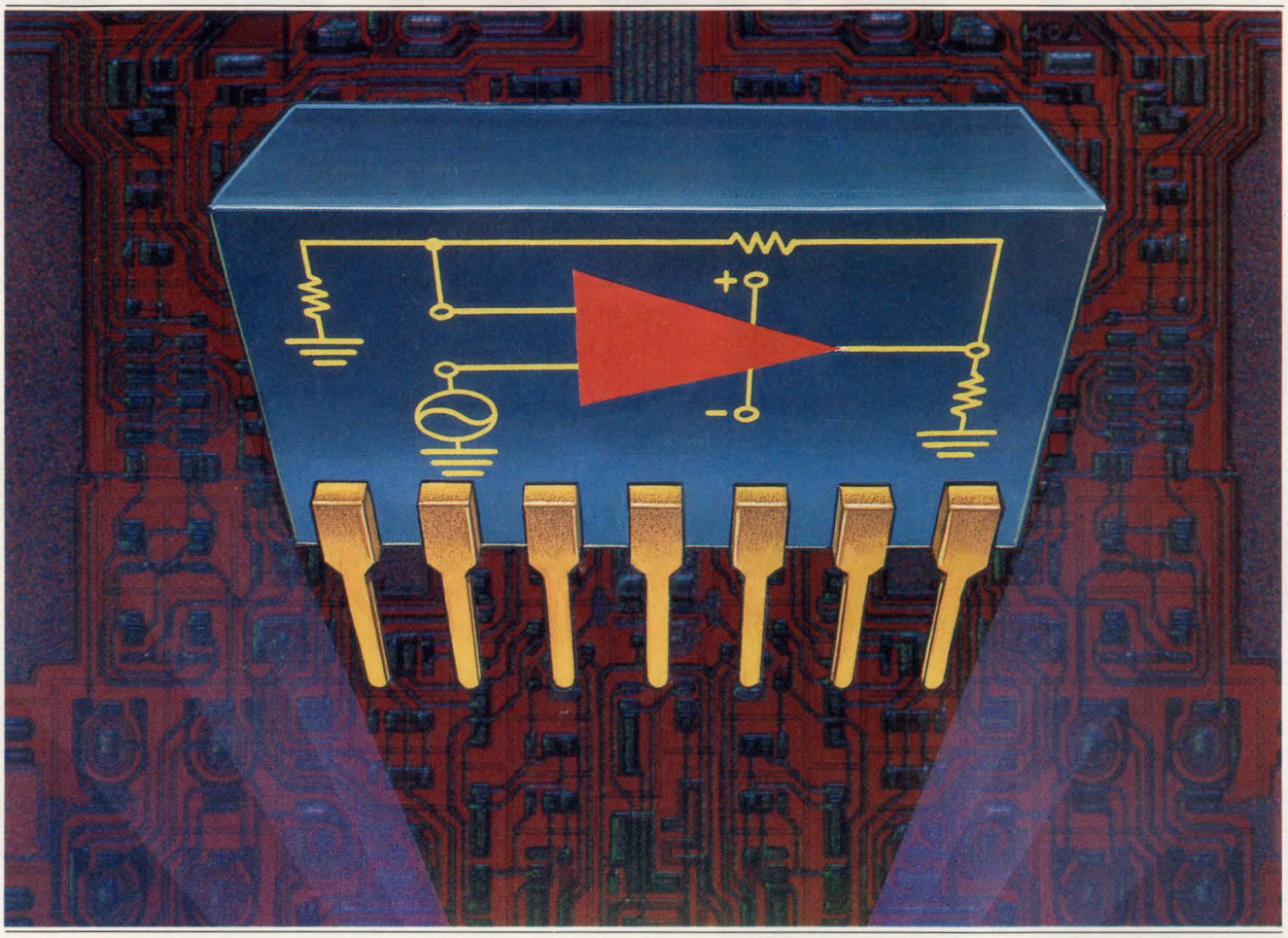

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Technology Advances
QuickLook

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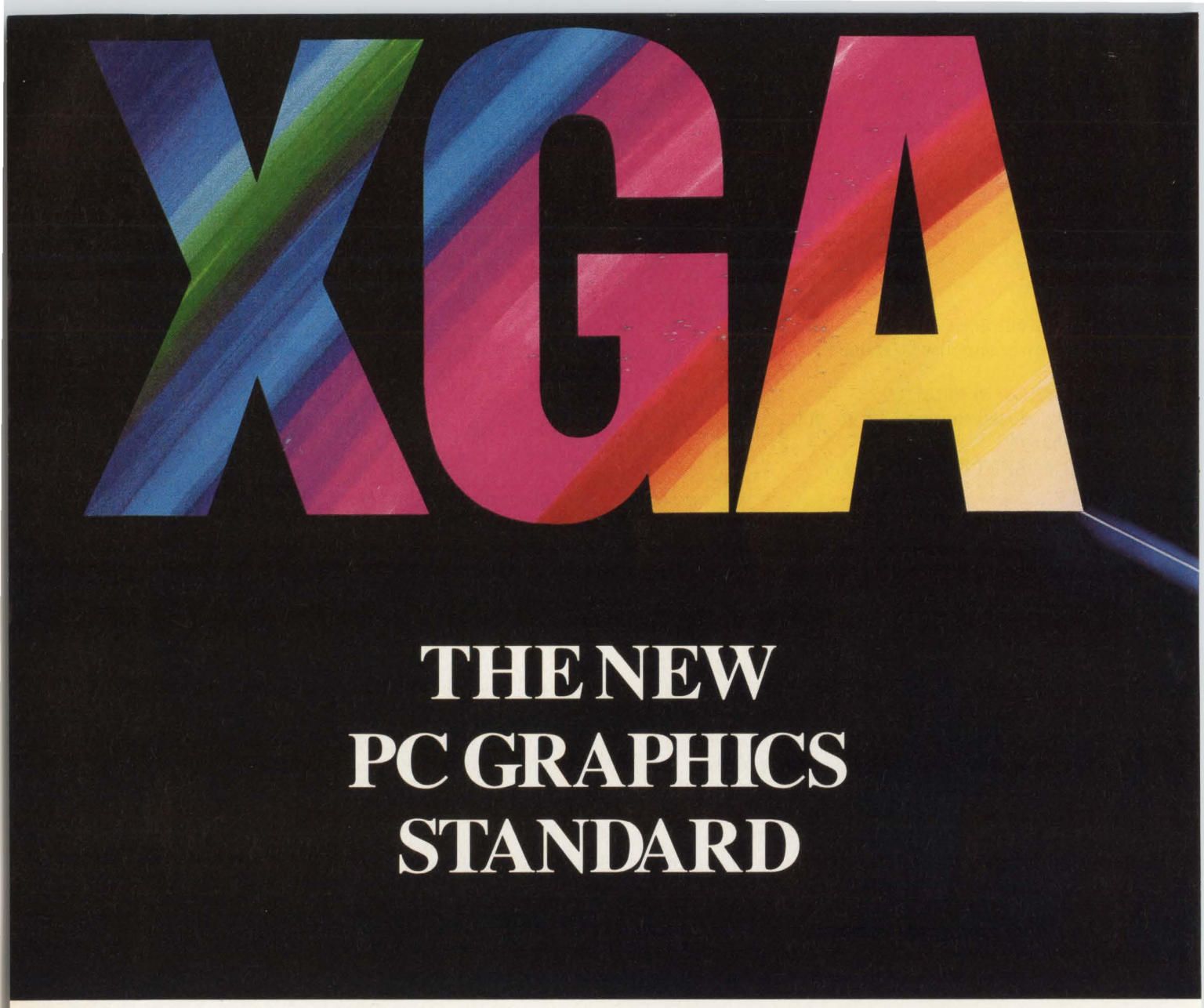

THE NEW PC GRAPHICS STANDARD

The new XGA standard has opened up an era of higher performance for PC graphics. And when IBM licensed their technology to INMOS, a division of SGS-THOMSON Microelectronics, as manufacturer and sole supplier of the IBM XGA chipset, they did it to ensure that the XGA parts got to the market quickly and reliably, setting the stage for XGA to become the next volume standard in PC graphics. Specifically designed for PCs, XGA is already available to support the MicroChannel Architecture bus, and an AT bus-compatible version is under way. The new XGA standard offers significant enhancements over VGA with:

- higher speed
- higher resolution (up to 1024 × 768)
- more colors (256 up to 64K) giving photo-realistic multimedia-style images
- optimized graphics interface for better windowing
- optimization for use with latest generation processors

Fully VGA compatible, XGA performance specs offer a package that is way ahead:

- 132 column text mode
- extended graphics function mode, including hardware sprite and coprocessor hardware drawing assist
- 90% faster than IBM VGA under DOS, 55% faster under OS/2
- 67% faster running Microsoft Windows applications

TWO CHIPS THAT SET THE STANDARD

The IBM compatible XGA chipset consists of two advanced VLSI chips, the INMOS IMS G190 XGA Serializer Palette DAC in a 144 pin CQFP and the INMOS IMS G200 XGA Display Controller in a 184 pin PQFP. A major advantage of the IMS G200 is its on-chip coprocessor which offloads tasks from the host processor and allows it to support:

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FULL SOFTWARE SUPPORT is offered for the IBM compatible XGA chipset with the following drivers available:

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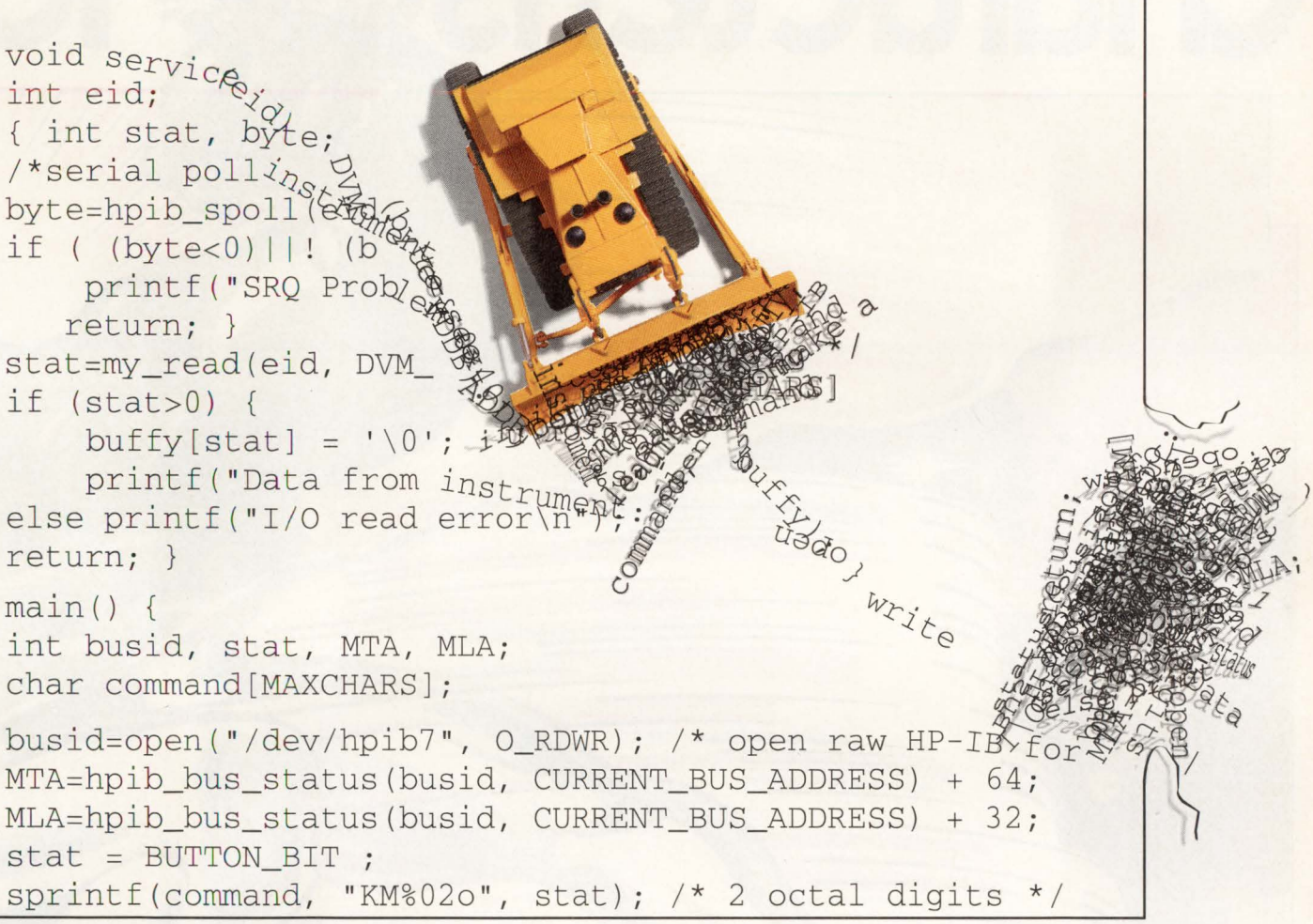
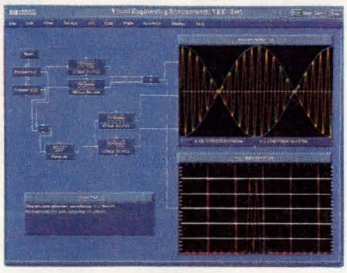
Finally, engineering software that clears the way to problem solving without programming.



```
void service(eid)
int eid;
{ int stat, byte;
/*serial poll instrument*/
byte=hpib_spoll(eid);
if ( (byte<0)||! (b
    printf("SRQ Prob
   return; }
stat=my_read(eid, DVM_
if (stat>0) {
    buffy[stat] = '\0'; i
    printf("Data from instrument:
else printf("I/O read error\n");
return; }

main() {
int busid, stat, MTA, MLA;
char command[MAXCHARS];

busid=open("/dev/hpib7", O_RDWR); /* open raw HP-IB for
MTA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
MLA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
stat = BUTTON_BIT ;
sprintf(command, "KM%02o", stat); /* 2 octal digits */
```



With HP VEE, you simply link the icons.

Computers are great for problem solving, if only programming didn't get in the way and slow you down. And now, it doesn't have to. Because the HP visual engineering environment (HP VEE) lets you solve problems without programming.

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There are two HP VEE software packages for prototyping, experimentation, and problem modeling. HP VEE-Engine, at $995*, is a general-purpose tool for analysis and presentation of existing data. HP VEE-Test includes HP VEE-Engine and adds extensive I/O capability, including soft panels and device I/O objects for $5,000*.

So, if programming is keeping you from solutions, call **1-800-752-0900.** Ask for **Ext. 2382**, and we'll send a brochure on clearing the way with HP VEE.

* U.S. list prices.

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It Takes Some Characteristics To

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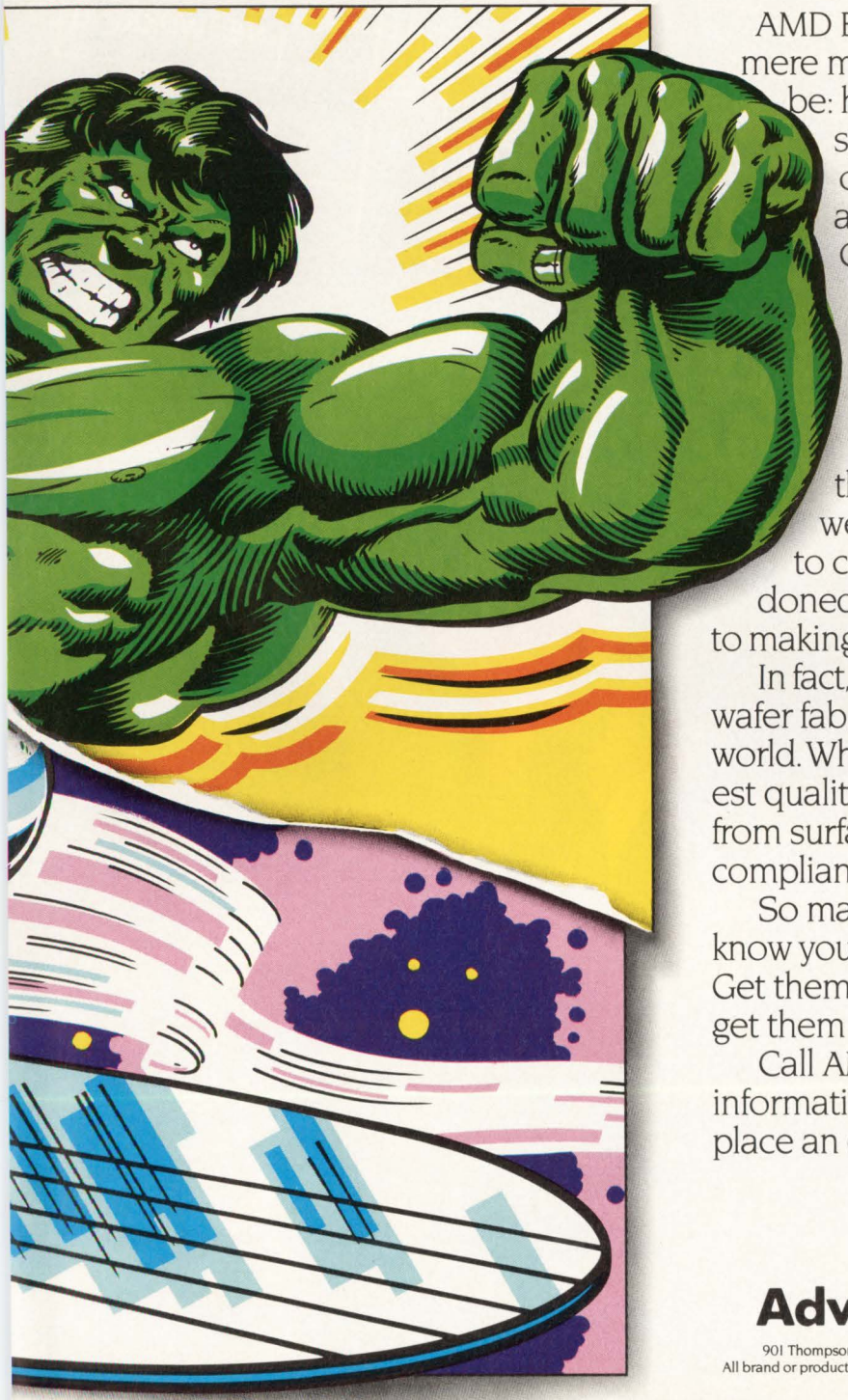

AMD EPROMs today are what other mere mortal EPROMs can only aspire to be: high density, of course. But also high speed. Able to store massive amounts of information, with lightning fast access times. All in our superior CMOS technology.

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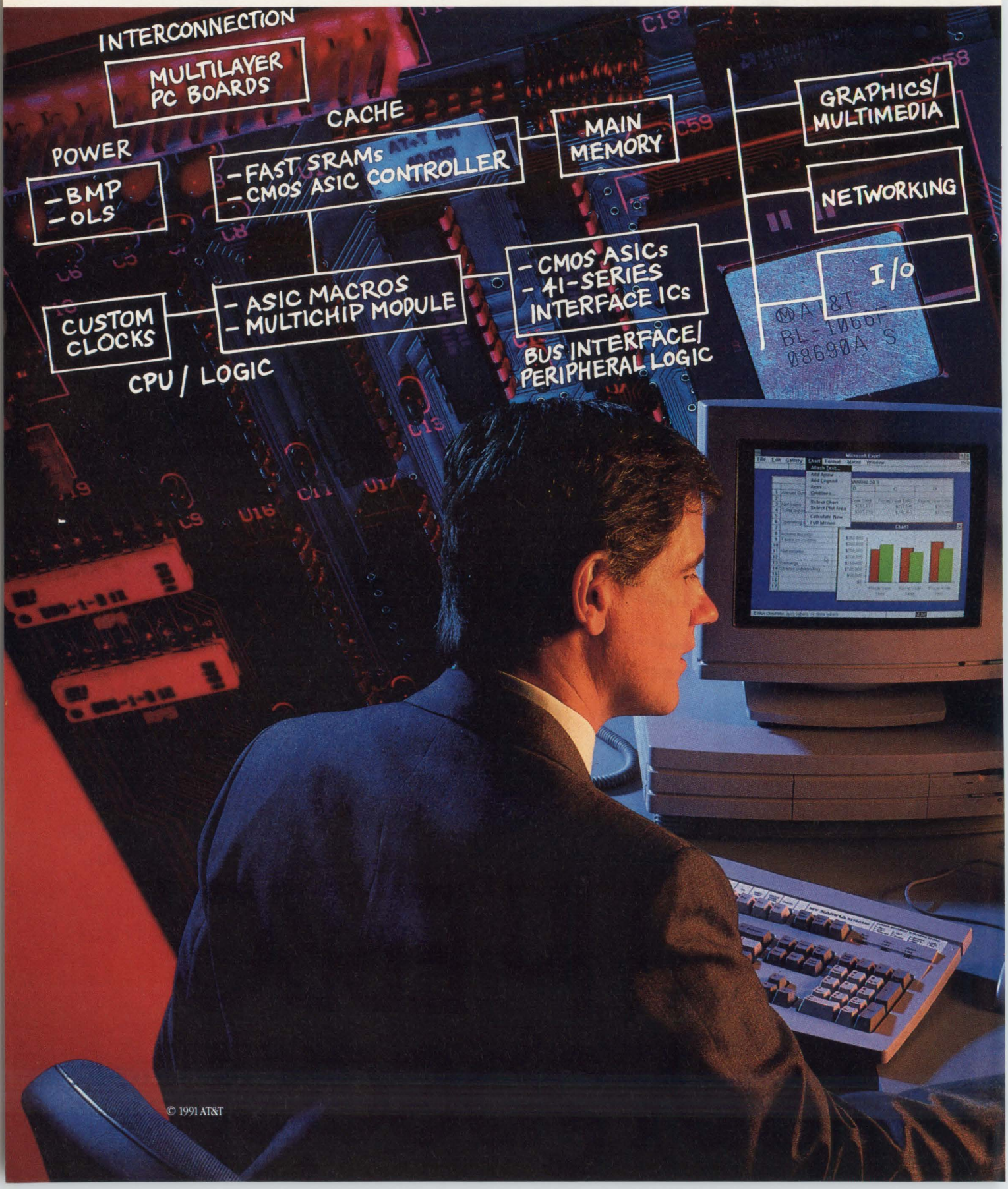

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"Customerizing" means providing the component solutions and support technology your systems need to help keep pace with CPU speeds up to 50 MHz and beyond.

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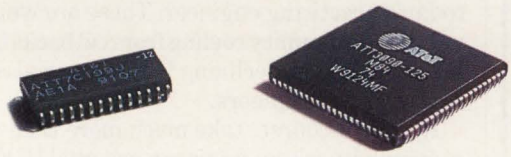

32Kx8 12 ns SRAMs | 125 MHz FPGAs | 400 Mbits/s Interface ICs

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IEEE In '92: A Focus On Members

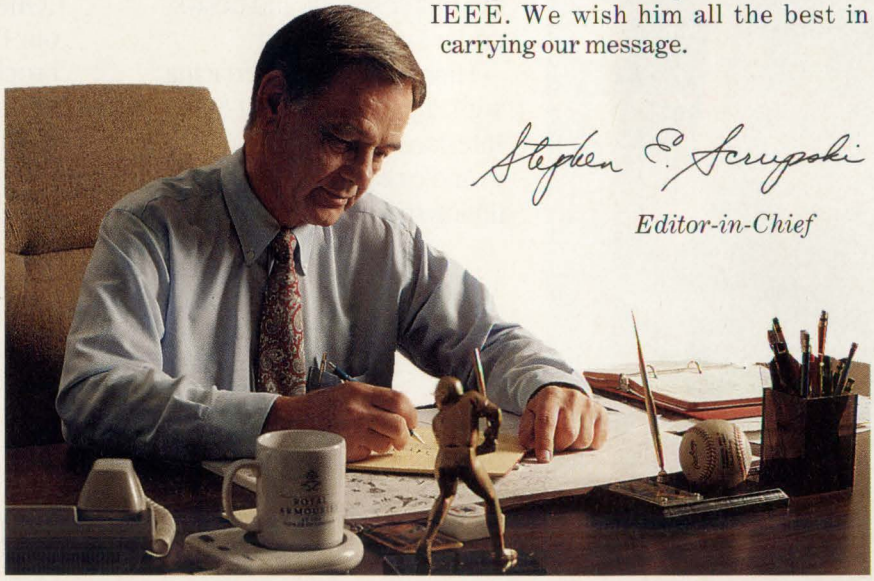
The IEEE has always excelled in disseminating technical information through its conferences and publications, in its standards groups, in offering technical expertise in government testimony, or in other technology-based activities. Those are important areas. Without the hard efforts of the many volunteers who serve on the IEEE committees, our industry would suffer. However, there's one area where the Institute has not done a good job: In helping its grass-roots, working-engineer members on bread-and-butter issues, such as job security, salaries, pensions, etc. Now it appears that the IEEE, the world's largest technical society with its 320,000-plus members, may be in for some changes.

Next year's IEEE president, Merrill W. Buckley, Jr., recently spoke at a meeting of the Professional Activities Committee for Engineers of the North Jersey Section of the IEEE. "I want to be remembered as a president who was concerned with the members," said Buckley, who was elected as a petition, rather than a board-nominated, candidate. Buckley offered a wide-ranging series of candid opinions that clearly revealed his concerns about the welfare of today's practicing engineer. These are welcome comments, indeed, to an engineering community reeling from cutbacks in defense spending, an economy still in the doldrums, declining U.S. industrial competitiveness, and a surplus (not a shortage) of engineers.

It will, of course, take much more than Buckley's one-year term, or even a revamped working-engineer-oriented IEEE, to solve these problems. The first steps toward remedying this situation must come from organizations like the IEEE and the engineers themselves. Next year will offer some excellent opportunities to do this.

The campaign oratory in the 1992 presidential election will undoubtedly be filled with claims and counterclaims about which party can best rebuild this country's industrial competitiveness. There's a growing awareness – and discomfort – among the general public regarding the level of foreign ownership of U.S. real estate and manufacturing resources. The high-tech community must get its message through to the candidates at all levels of government—that technology is essential to the future well-being of this country and its workers. And engineers are the primary adders of value in high-technology products.

All in all, 1992 promises to be an eventful year: A presidential election, the Common Market in Europe, the re-emergence of Eastern Europe as market-driven economies, continued innovation in electronics, and, closer to home, a new, engineer-oriented president for the IEEE. We wish him all the best in carrying our message.



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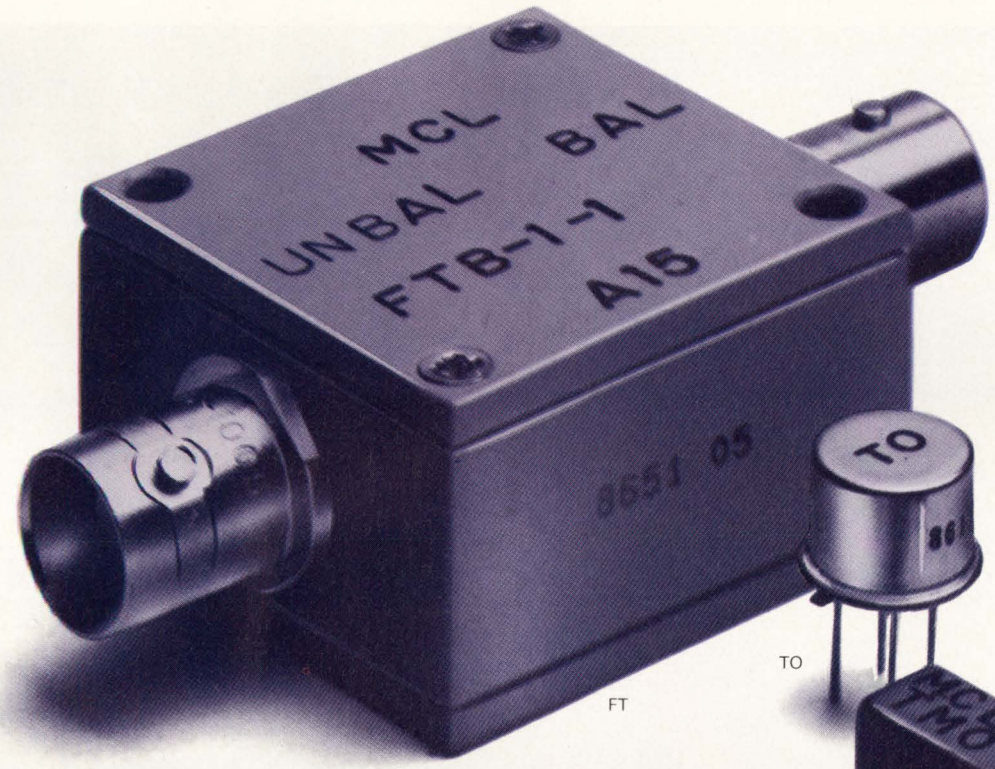

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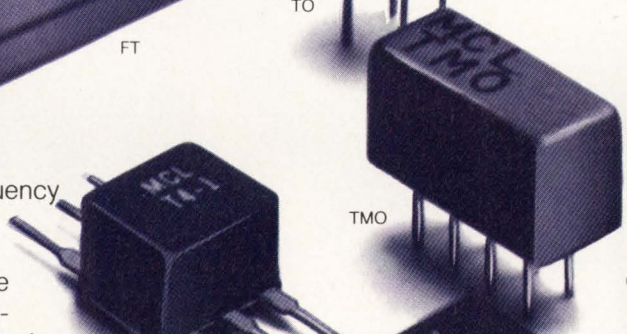
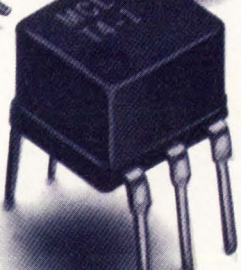
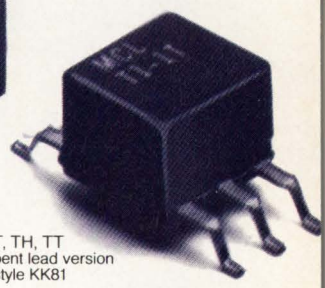


TMO

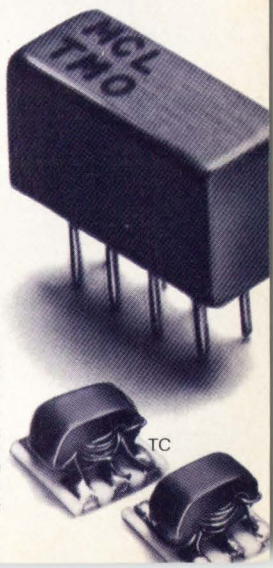
T, TH, TT



T, TH, TT
bent lead version
style X 65



T, TH, TT
bent lead version
style KK81



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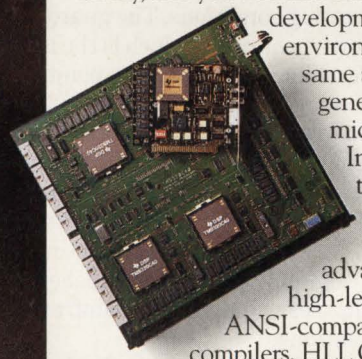

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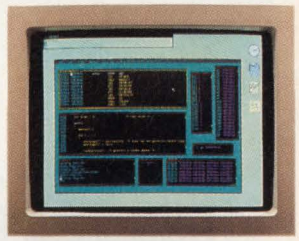

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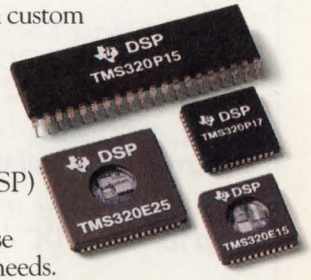

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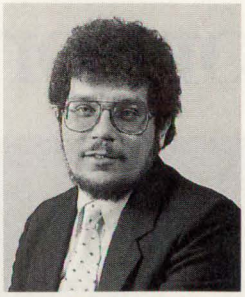

DAVID MALINIAK
COMPONENTS & PACKAGING

Is the industry ready for a real mechanism for grading power supplies? When you buy a power supply, how do you really know what kind of quality you're getting? Is an arbitrary set of specifications or random testing a real predictor of field reliability? Those questions are posed by Norm Berkowitz and Ron Koslow of Power Solutions Inc., Northport, N.Y. Berkowitz and Koslow offer a grading proposal that's based on the ISO-9000/UL-90 standards now being adopted in Europe and North America as a measure of reliability and application utility.

The scheme, as outlined here, proposes grading non-military supplies as a function of the "guard bands" put on each component and the representative end use that the supply is meant for. The guard band is the amount that each component is derated from the manufacturer's maximum allowable stress condition. In addition, a supply's grade depends on the guard band that its design allows under worst-case published or specified operating conditions. The guard band is measured from the full rated power and/or current point, which is the maximum point on the supply's actual voltage-current characteristic. The point of reference will be a function of the grade ascribed to the supply by the manufacturer.

The highest grade, Grade One, is meant for quasi-military, ruggedized operation and harsh environments. This means use in high-end products where reliability comes first and cost and size come later. Grade One products are guaranteed to MIL-STD-810 shock and vibration standards and must operate from –40 to +71°C. Internal component derating guard bands are in excess of 20% of maximum ratings at the supply's published worst-case conditions. Uses include high-reliability test equipment; mainframe computers; and remote site, untended installations.

For the industrial marketplace, Grade Two supplies must offer superior reliability with high package density at competitive pricing. These products are meant for use in demanding settings, though not as severe as Grade One conditions. Typical component deratings are about 15 to 20% from maximum ratings at the supply's published worst-case conditions. Grade Two supplies run from –20 to +60°C. Their uses include process control, industrial ATE, materials handling, and telecommunications.

Grade Three supplies are for commercial users for whom the price-performance ratio is key. Typical internal guard bands on Grade Three range from not less than 10% to a maximum of 15% derating at the supply's published worst-case operating conditions. Grade Three supplies operate from –10 to +60°C. Uses are in equipment like point-of-sale materials and office-automation devices.

The lowest grade is for the consumer and low-performance office-automation and computer markets. Grade Four supplies are for products where price is king and performance and power density lag behind. Typical guard bands on the internal components for Grade Four product range between 0 and 10% from the component manufacturers' maximum ratings when measured at the supply's worst-case operating conditions. The supplies' operating range is 0 to +60°C. Most applications are in systems such as low-end office equipment and PCs.

While not claiming it's a panacea, the authors believe their proposal would help end the confusion in specifying power supplies. They're also calling for organizations such as UL and CSA to take up the cause and elevate the concept of power-supply grading to a "legal" definition. If precise definition from an independent body with "expert standing" is accepted, Berkowitz and Koslow assert that system designers can at last know exactly what they're getting in a power supply. Fax your opinion of the proposal to David Maliniak at (201) 393-0204.

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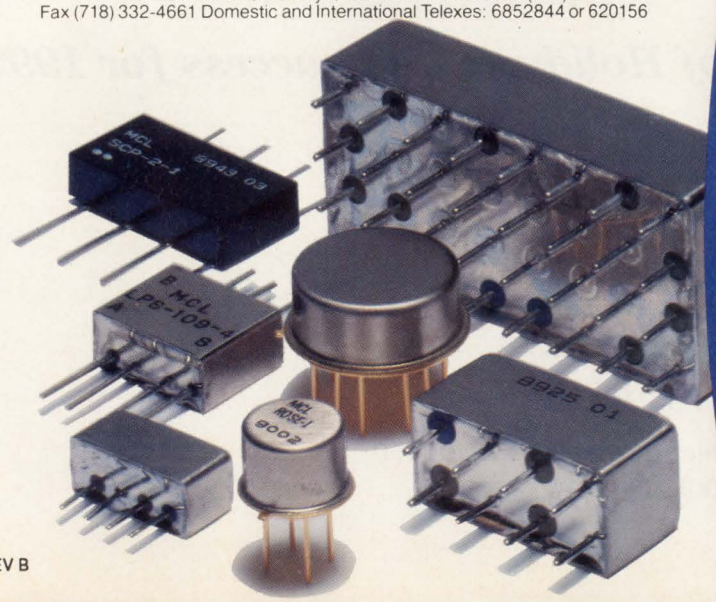

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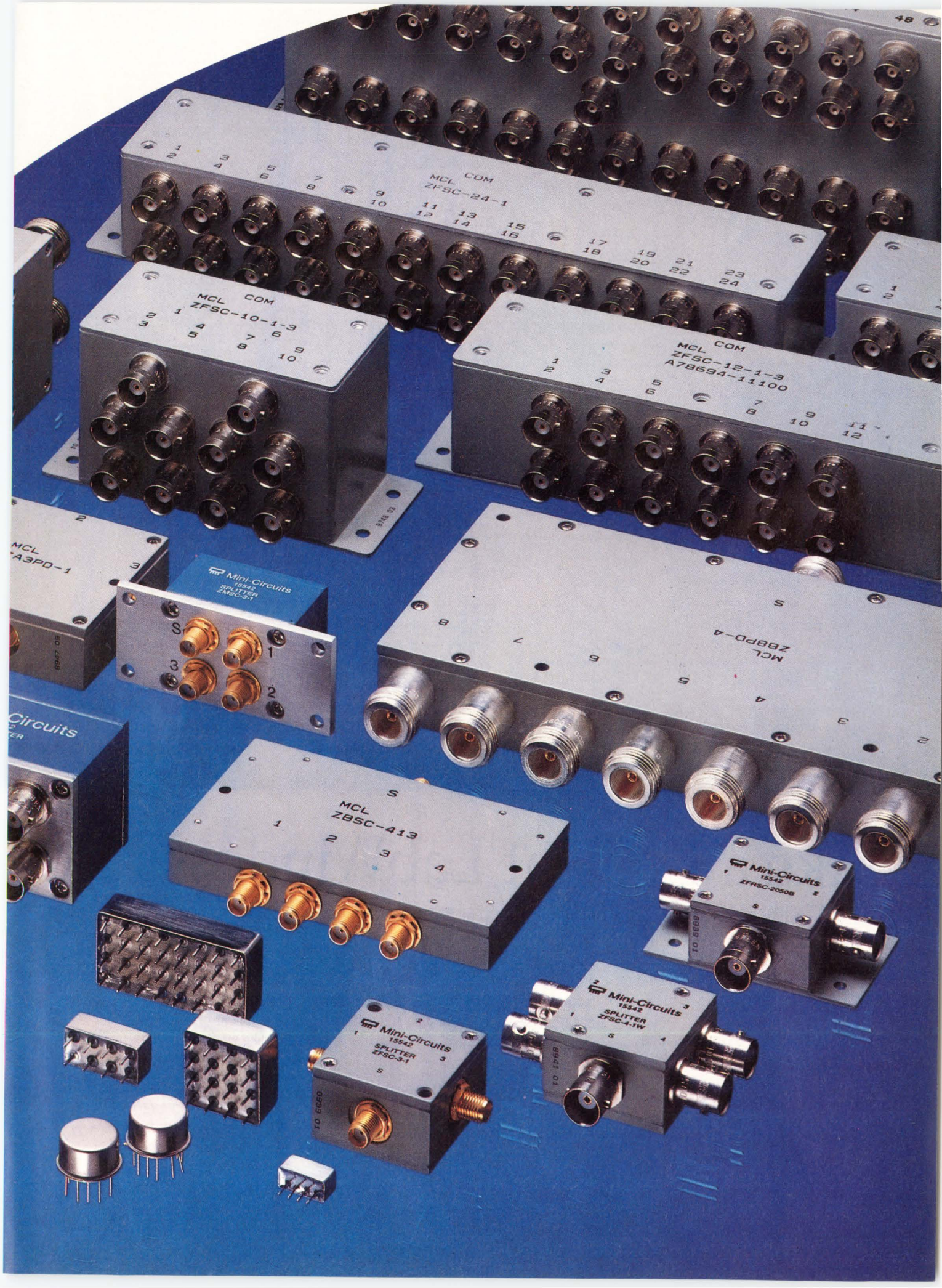
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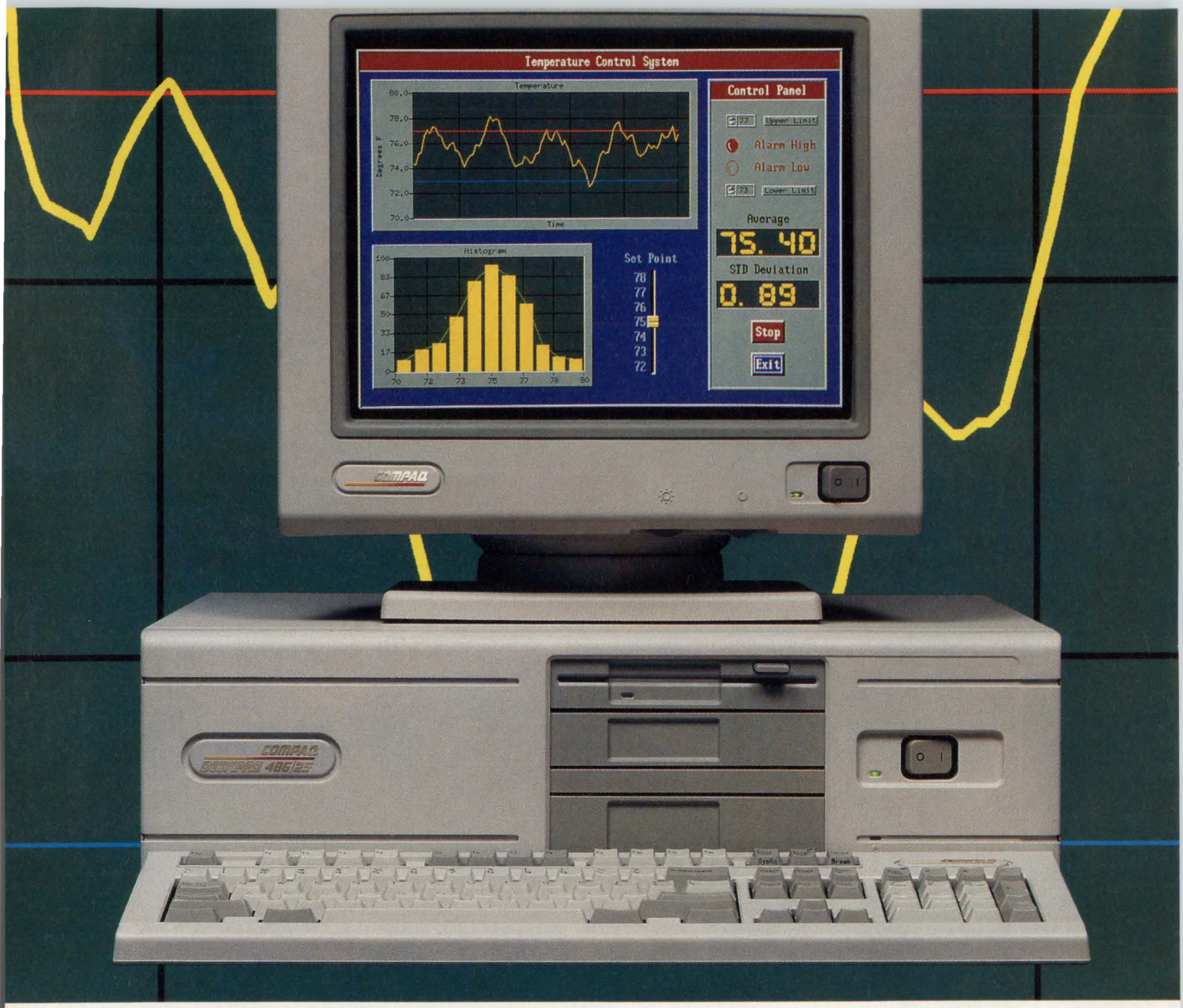

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IC For Closed-Caption TV To Cut Costs Sharply

The cost of decoding text broadcasts along with TV signals in the United States for the Closed-Captioning Service for the hearing impaired will drop dramatically from $200 to less than $10 next year. That's the assessment of Philips Semiconductor when it starts volume production of a dedicated Line 21 decoder chip. Dubbed LITOD (Line Twenty One Decoder), the device will offer various on-screen text formats, including scrolling, painting, and pop-on, on the four-line subtitles. The chip will also allow text, which can be indented and in color, to be positioned anywhere on-screen. It will also support accented characters to provide Spanish and other non-English text. And if needed, it can provide a full page of text. According to Richard Bugg, technical consultant at the firm's consumer-IC development center in Southampton, United Kingdom, they're well ahead of schedule in developing a chip that will fit between the RF and video sections of a TV.

The service that encodes data on line 21 of the 525-line NTSC signal was originally intended to offer TV subtitles for the hearing impaired. "Since the service was introduced ten years ago, many other applications have been found," Bugg says. These include assisting primary-school children in their reading and providing subtitles for non-English-speaking viewers, and use in areas where ambient noise drowns out TV sound. The U.S. Congress has now passed a law insisting that from mid 1993 on, all TV receivers sold in the U.S. with a screen size greater than 13 in. must have a built-in decoder. "That's 20 million TV receivers a year," Bugg says.

Bugg explains that currently, reception of closed captions is achieved by means of an external adapter connected through the antenna socket. That retails in the U.S. for around $200. Philips' new chip will completely replace the external box, Bugg claims, and adds that he expects the 24-pin chip will cost around $5 in commercial quantities. First silicon for sampling is expected during the first quarter of 1992. For more information, contact Philips Semiconductors in the United Kingdom at +44 071 560 6633. *PF*

3-Pin MOSFET Holds Protection Circuits

Philips Semiconductors, Eindhoven, the Netherlands, has crafted what it believes is the first 3-pin power MOSFET with integrated short-circuit, over-temperature and overvoltage protection. Housed in a standard TO-220 package, the BUK101-50 TOPFET—for temperature and overload protected FET—needs no additional protection components. It can be driven directly from conventional logic-level FET driver circuitry. Consequently, it can be used as a fully ruggedized replacement MOSFET in existing equipment as well as for new designs. The device suits the switching of lamps, motors, and solenoids in automotive electronics, but it should also find uses in general industrial applications.

The n-channel, enhancement-mode FET has on-resistance of 60 mΩ and a continuous-current rating of 26 A (100 A peak). The protection circuitry automatically switches the device into the off state when the junction temperature exceeds a safe value—typically 180°C—due to inadequate heat-sinking or short-circuit load currents. The over-temperature and short-circuit protection circuits incorporate a latch that maintains the device in the off state until its control input is driven low. *JG*

IBM, Credence Work On Multi-Time-Domain Test

Coming up with a new way to directly test high-performance VLSI devices with multiple time domains is the focus of IBM Corp.'s Boca Raton Div. in Florida and Credence Systems Corp., Fremont, Calif. The program's goal is to exercise and verify the operation of multiple time domains in environments that approximate the device's intended application. The procedure is based on a test algorithm created by IBM-Boca, in which two or more groups of pins are referenced to independent clock cycles. The test program stimulates the device under test at full speed on an LT-1101 digital tester developed by Credence's Beaverton Business Unit in Oregon. The tester supplies up to eight independent domains. Simulation responses are generated for each domain and its associated pins. Print charts for each response are then processed through automated-test-program generation tools created by IBM-Boca. The result is the required LT-1101 files, which are then compiled, linked, and executed for comparison with the target device. *JN*

VESA Adds Three SVGA Extensions

At a recent meeting of the Video Electronics Standards Association (VESA), San Jose, Calif., three new extensions were added to the Super VGA (SVGA) PC graphics standard, making it more versatile, powerful, and accessible. The first extension, the SVGA protected-mode interface, establishes a standard programming interface between protected-mode applications and SVGA display modes. With the interface, applications can query the graphics hardware directly from the protected mode. The second

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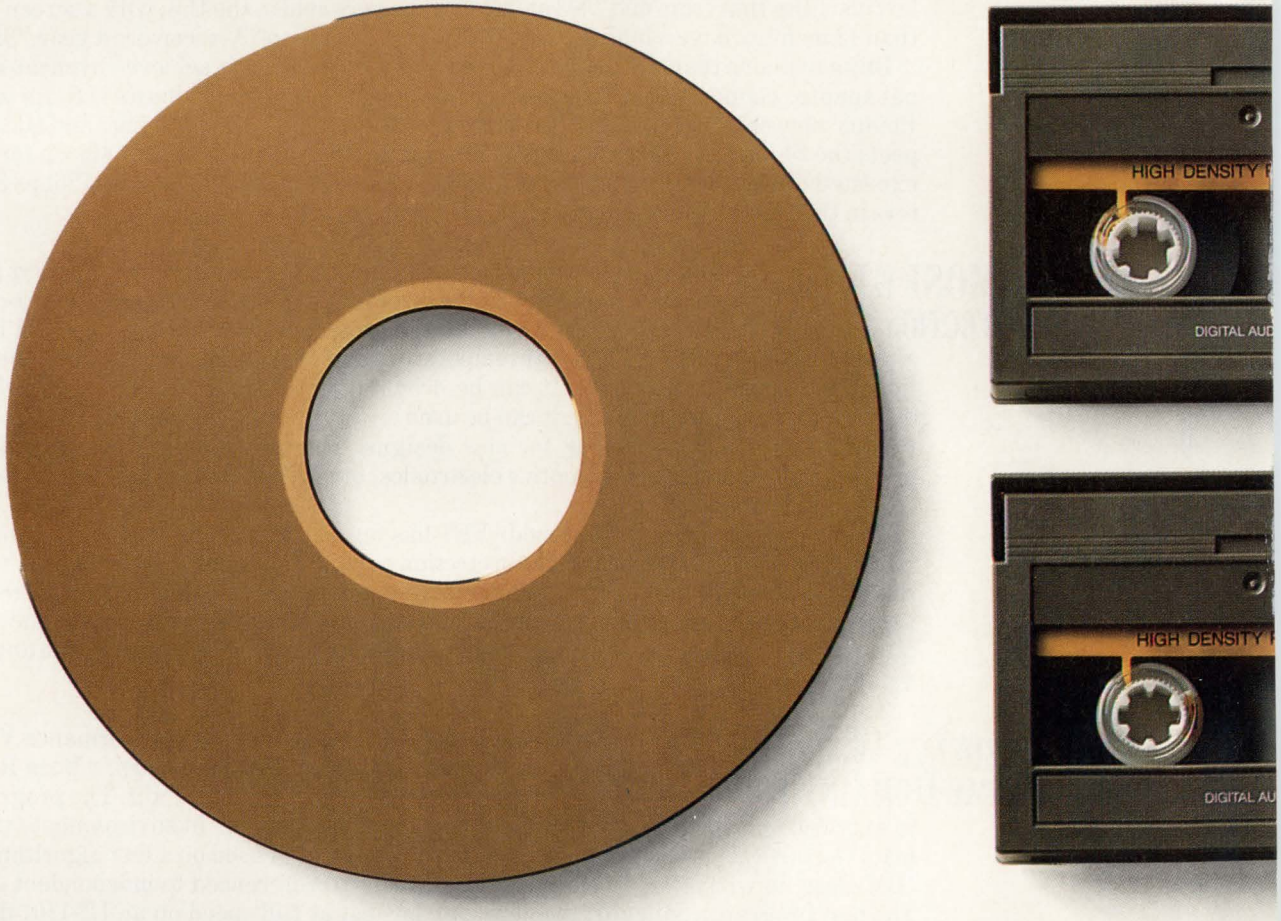

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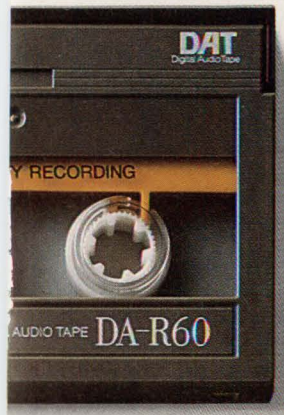

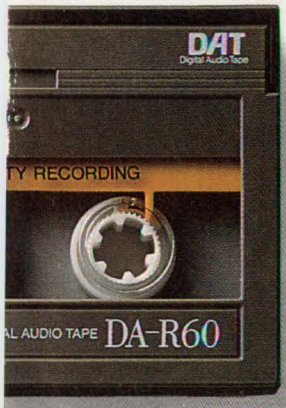

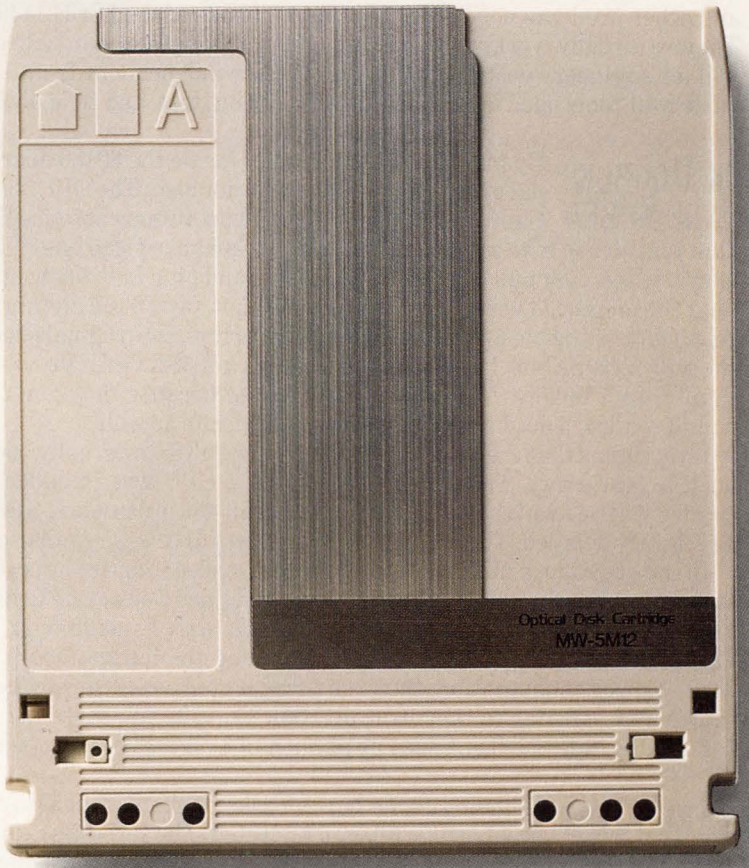

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TERADYNE, TI COOPERATE ON BOUNDARY-SCAN WORK

Teradyne Corp., Boston, Mass., and Texas Instruments Inc., Dallas, have agreed to collaborate on boundary-scan technologies and products. The two companies will integrate TI's Asset, a PC-based boundary-scan design debug tool, with the Virtual Interconnect Test (VIT) module from Teradyne's Victory boundary-scan test software. They'll develop common interfaces to ensure that the two products work smoothly together. TI will sell the VIT module for use with Asset. The module analyzes a board-level net list to identify boundary-scan nodes, then generates test patterns needed to diagnose pin faults on the nodes. Production shipments of the combined tools is scheduled for the third quarter of 1992. In addition, the companies will work together to develop standards and other products needed to encourage the use of the IEEE-1149.1 boundary-scan standard. They're already working on a common interchange format, called Serial Vector Format, that will let engineers write portable test vectors independent from 1149.1 controller ICs and the variety of tools used in design, manufacturing, test, and field diagnostics. *JN*

CLOCK DOUBLES 486-UPGRADE SPEED

By putting a clock doubler inside the 80486 microprocessor, the chip's internal operating speed can be doubled. The CPU, from Intel Corp., Santa Clara, Calif., executes all internal operations at twice the speed of its external bus. Due for release in the first half of 1992, the enhanced i486 has 8 kbytes of on-chip cache and is easy to use—just pull out the old processor and plug in the new one. Or, as Intel recommends, plug the enhanced version into an extra socket, put on the motherboard by the system designer, and leave the old processor in. Upon insertion, the original processor is disabled, similar to the way a 487SX math coprocessor disables a 486SX CPU. Previous generations of the 80X86 family can't benefit from the clock doubling because they don't have the on-chip cache and would require a doubling of the bus transfer rate as well.

Intel claims that the next generation of the 80X86 (internally code-named P5) series is still at least a year away. Therefore, the upgraded CPU was intended as a "mid-life kicker." Upgrades will be available in 1992 for all current 486 processors; the 50-MHz 486DX version may be slightly delayed. The company also expects to release similar parts for P5-based systems.

In the upgrade, a 2X clock generates four cycles to drive the core and two to drive the bus, instead of a 1X clock that generates two phases per clock cycle to drive the core logic in present 486 chips. The 1.2-million transistor 50-MHz part is made with Intel's triple-metal, 0.8-μm, CHMOS V process on 6-in. wafers. Doubling the internal clock rate, however, doubles the core's power consumption, thus requiring a heat sink. The power drawn by the bus interface scales in proportion to the bus utilization. Considering these factors, the power requirement for the upgrade chip increases by about 40% over a part with a similar external clock rate. *RN*

BENCHMARKS TEST NOTEBOOK PC BATTERIES

By using three benchmarks to simulate real-life usage, a notebook-computer's battery life can be tested. The three tests, dubbed the Steeplechase, the Sprint, and the Marathon, make up the Olympiad Suite from VeriTest Inc., Santa Monica, Calif. The Steeplechase simulates a typical user profile and takes place entirely within the enhanced mode of Microsoft Windows 3.0. The test script includes timed pauses, printing, and live keystrokes in Microsoft's Word for Windows and Excel applications. While running this test, all power-management features of the systems are enabled. The Sprint is identical to Steeplechase, except that power-management features are disabled. Running these two tests side-by-side offers insight into the system's power-management features.

The Marathon measures the amount of current that's drawn from the battery, in a completely suspended state, while the computer is running Windows in the enhanced mode. Dividing the result into the battery's total rated storage capacity yields an estimate of how long the computer can remain in its suspended mode.

VeriTest was recently contracted by Intel Corp. to run these benchmarks on a 386SL-based laptop. The SL-based machine lasted 7.58 and 2.73 hours in the Steeplechase and Sprint modes, respectively. In the Marathon test, it lasted 12 days. *RN*

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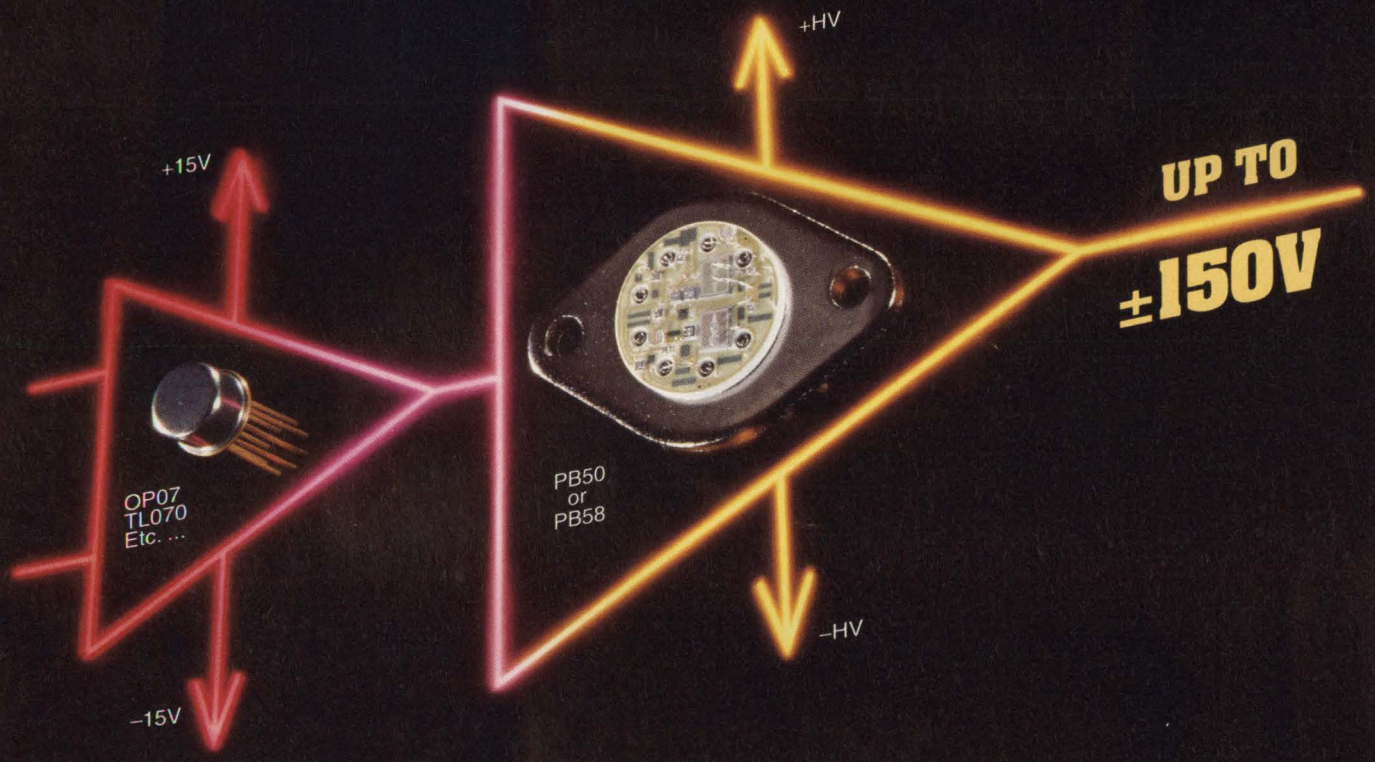

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The FS700 system includes a remote active 8-foot whip antenna, capable of driving up to 1000 feet of cable. The receiver contains six adjustable notch filters and a frequency output which may be set from 0.01 Hz to 10 MHz in a 1-2-5 sequence. A Phase detector is used to measure the phase shift between this output and another front panel input, allowing quick calibration of other timebases. An analog output with a range of ±360 degrees, provides a voltage proportional to this phase difference for driving strip chart recorders, thus permitting continuous monitoring of long-term frequency stability or phase locking of other sources.

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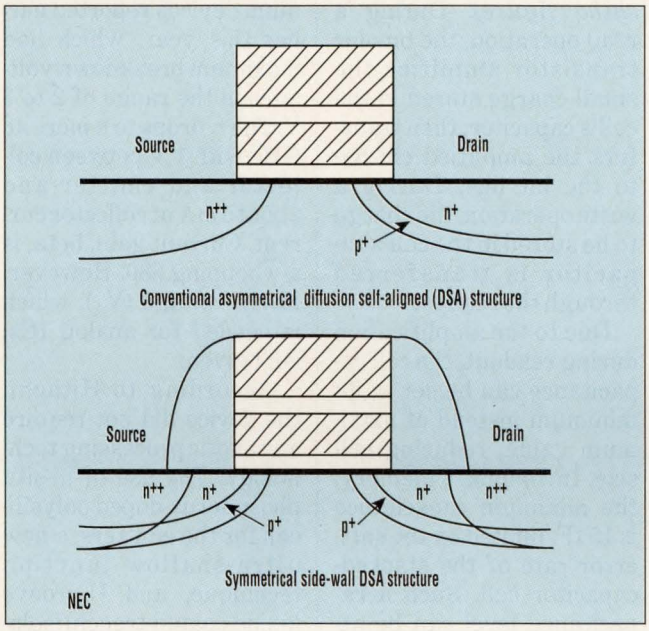
MEMORY STRUCTURES, FAST TRANSISTORS, AND POWER ICS ADVANCE AT IEDM

Advances in just about every aspect of semiconductor technology will be unveiled at next week's International Electron Devices Meeting in Washington, D.C. However, of all the developments, the latest cell structures for nonvolatile memories and dynamic RAMs show off the best in process technologies. The first details will be presented on memory cells for 64-Mbit flash EPROMs as well as for 4-Mbit flash EEPROMs. In addition, multiple papers will unveil DRAM storage-cell structures, some requiring less than 2 μm^2 and usable for 256-Mbit DRAMs.

With feature sizes of just 0.4 μm, a stacked-gate memory cell developed by NEC Corp., Sagamihara, Japan, shows promise for use in high-density, 64-Mbit flash memories. The source and drain regions of the symmetrical, side-wall diffusion self-aligned cell employ triple junctions formed from lightly doped n^+, heavily doped n^{++}, and diffusion-self-aligned p^+ regions *(see the NEC figure)*. The structure scales well and can achieve a 10-μs programming time with a 5-V drain voltage.

Even with the 5-V level, the cell has a reasonable drain-disturb immunity of 10^4 seconds, which is equivalent to about 1 million write/erase cycles for each sector (1-kbit sector and 10 μs/bit programming time). A uniform-erasing scheme, referred to as channel erase, applies a negative bias to the gate. Furthermore, the endurance and the gate-disturb characteristics of the scheme used by the cell are better than the non-uniform schemes used by existing flash memories. Another novel flash cell structure, a source-side-injection scheme employing a cell made by Texas Instruments' FAMOS process, will be described by the Dallas-based company.

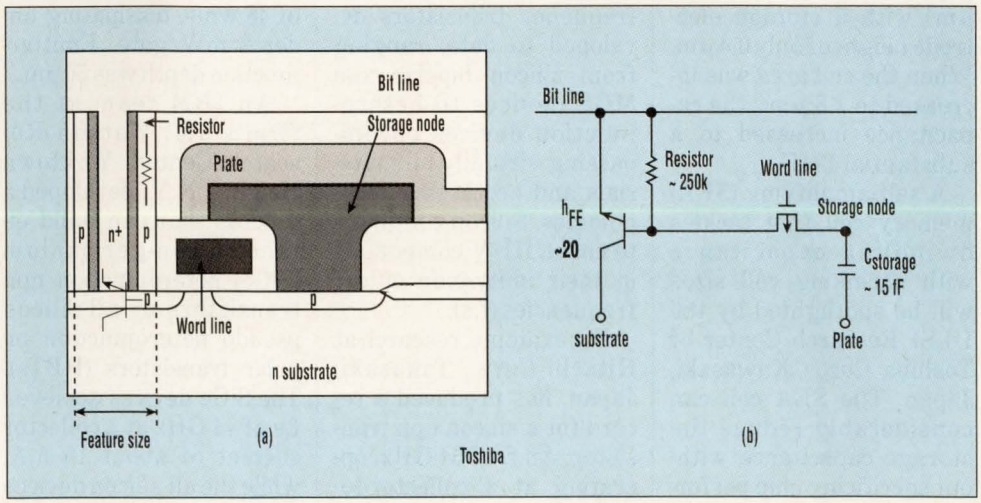


For high-density EEPROMs, researchers at Mitsubishi Electric Corp., Itami, Japan, will describe a compact EEPROM cell that occupies less than 9.6 μm^2 when fabricated with 0.8-μm design rules—about the same area as a DRAM cell fabricated with the same design rules. To save space, the floating and control gates are stacked on top of the select gate. The select gate, the oxide tunnel region, and the floating gate are set up in series between the bit-line contact and the source line, forming a merged one-transistor structure.

The cell's small size gives the full-feature EEPROM array a density equivalent to DRAMs. A cell-programming current of just 80 μA will allow an on-chip bias generator to create the programming voltage from a 5-V supply, enabling the chip to operate completely from a 5-V supply. Furthermore, by changing the process rules to 0.5-μm minimum features, the cell design can be scaled to create 16-Mbit full-featured EEPROMs.

Also expecting to produce 16-Mbit flash EEPROMs, designers at the VLSI Research Laboratory at Sharp Corp., Tenri City, Japan, have created a virtual-ground stacked flash EEPROM cell. Occupying just 2.59 μm^2, the cell is programmed by the high-efficiency source-side injection of channel hot electrons. Cell programming time is less than 1 μs—that's almost 10 times faster than conventional stacked flash cells.

A dual polysilicon 15-



μm^2 EEPROM cell structure has been created by Xicor Inc., Milpitas, Calif. The structure, which has 0.7-μm lines, isn't as compact as the Mitsubishi cell, but it exhibits an endurance 100 times better—over 1 million cycles versus 10,000. Cell current is similar to that of the Mitsubishi cell, allowing on-chip programming-voltage generation and making it possible for all chip operations to be controlled externally by 5 V and by TTL-compatible signals.

Flash and EEPROM cell sizes are nearing those of today's DRAM cells, yet DRAM makers continue to work on future cell structures that employ even smaller features—down to about 0.4 μm. This reduces the cell area to less than 2 μm^2, as will be demonstrated by Matsushita Electric Industrial Co. Ltd., Osaka, Japan, in a paper that details a spread vertical-capacitor (SVC) cell. The SVC cell is a low-height structure with high capacitance achieved by using oxide-nitride-oxide dielectric layers. The structures, fabricated with 0.4-μm design rules, have a capacitance of 24 fF. However, they occupy an area of just 0.45 μm^2 with a storage electrode height of only 0.4 μm. When the cell area was increased to 1.8 μm^2, the capacitance increased to a substantial 43 fF.

A self-amplifying (SEA) memory cell that tackles dwindling capacitance with shrinking cell sizes will be spotlighted by the ULSI Research Center of Toshiba Corp., Kawasaki, Japan. The SEA cell can considerably reduce the storage capacitance without sacrificing chip performance. In the cell, a bipolar transistor and a resistor are merged into a bit-line contact region *(see the Toshiba figure)*. During a read operation, the bipolar transistor amplifies the small charge stored in the cell's capacitor, then transfers the amplified charge to the bit line. During a write operation, the charge to be stored in the cell's capacitor is transferred through the resistor.

Due to the amplification during readout, the cell capacitance can be set at its minimum instead of maximum value, reducing cell size. In Toshiba's memory, the minimum capacitance is 15 fF, limited by the soft-error rate of the stacked-capacitor cell. Such a capacitance level can be attained without resorting to a complex "crown" or "fin" cell structure. Another storage scheme developed by Toshiba shows promise for 256-Mbit DRAMs: A surrounding isolation merged-plate electrode (Simple) cell offers the smallest area for cells that employ a planar transfer-gate transistor.

Fast Devices

Each year's IEDM is *the* showcase for the highest-frequency transistors developed to date, ranging from silicon bipolar and MOS devices to heterojunction devices encompassing virtually all materials and processing technologies. Silicon continues to chase III/V compounds in their unity-gain cutoff frequencies (f_ts).

For example, research at Hitachi Corp., Takasaki, Japan, has produced a record for a silicon npn transistor: An f_t of 64 GHz, operating at a collector-to-emitter voltage of 3 V and a collector current of about 8 mA. This puts the device in the class of silicon-germanium devices reported earlier this year, which had maximum breakdown voltages in the range of 2 to 3 V. The f_t drops to a mere 48 GHz with 1 V between collector and emitter and about 5 mA of collector current. Current gain, beta, is a whopping 680. However, Early Voltage (V_A), which is needed for analog ICs, isn't given.

According to Hitachi, the device did not require any exotic processing technology. The use of in-situ phosphorus-doped polysilicon for the emitters, a new ultra-shallow junction technique, and U-groove (oxide-coated-trench) isolation did the job. Emitter-base junction depth was 100 nm.

With trench isolation, researchers at Siemens' Central Research Development Group in Munich, Germany, achieved npn f_ts of 34 GHz, with 3 V between collector and emitter and collector currents as low as 3 mA. Ring oscillators built with current-mode logic (CML) achieved measured gate delays of just 24 ps and current gain of 48 while dissipating under 2 mW/gate. Emitter-junction depth was 50 nm.

An IBM team at the firm's T.J. Watson Research Center, Yorktown Heights, N.Y., developed a process that can build either silicon-germanium (SiGe) heterojunction npn transistors or all-silicon pseudo heterojunction bipolar transistors (HBTs). The SiGe devices achieved f_ts of 44 GHz at a collector current of about 15 mA, while the all-silicon devices reached 37 GHz at a collector current of 20 mA. In a ring oscillator built from ECL gates, gate delays ran about 24 ps for the SiGe units and about 28 ps for the all-silicon devices.

Though these f_ts sound high compared with the 10-to-15-GHz transistors used in the fastest ICs readily available today, III/V-compound transistors still overshadow them. For example, researchers at NTT, Atsugi, Japan, have built a form of HBT, called a ballistic collection transistor (BCT), from an AlGaAs/GaAs compound. Built into the transistor is a "launcher," which ballistically transports electrons to reduce collector transit time without increasing base-collector capacitance. The BCT's f_t runs 160 GHz with a current gain of 60. Not just an isolated device, its developers successfully built both a 2:1 multiplexer and a linear amplifier. The multiplexer contains over 200 of the BCTs, runs at 19 GHz, and provides an output swing of 1 V. The two-stage amplifier employs negative feedback around both the input and output stages. It achieves a transimpedance of 52 dBΩ, a 3-dB bandwidth of 18.5 GHz, and a gain of 21 dB.

Working with AlGaAs/GaAs HBTs that have f_ts of 40 GHz (about where silicon and SiGe devices are arriving at), a team at Rockwell's International Science Center, Thousand Oaks, Calif., built "high-power" HBTs and an X-band amplifier. This was a joint effort with General Electric Co., Syracuse, N.Y. The HBTs put out 540 mW at 10 GHz while providing 8.9 dB of gain. The X-band amplifier puts out 2

W and supplies 3.2-dB gain from 8 to 11 GHz. A change in doping should raise the f_t to 53 GHz.

HIGH POWER ICS

Novel device designs for high-voltage operation and application in high-temperature environments will also be disclosed at the IEDM. Toshiba Research and Development Center, Kawasaki, has developed a silicon-on-insulator (SOI) technology to replace conventional dielectric-isolation methods for fabricating high-voltage power ICs operating above 200 V.

Experiments indicate that a high breakdown voltage can be realized even on a thin SOI layer by applying a large share of the applied voltage to the bottom oxide. Placing a proper amount of positive-charge layer (arsenic ion implant) on the bottom oxide further enhances breakdown-voltage capability. A thin positive-charge layer on the bottom oxide reduces the electric field inside the silicon and shields the increased electric field within the oxide. The intensified field within the silicon is confined to a narrow portion of the silicon-oxide interface, and contributes little to avalanche multiplication. Researchers have obtained a breakdown voltage of 650 V using a 14-μm-thick SOI layer on 3-μm-thick bottom oxide. The proposed SOI device structures combined with deep-trench isolation techniques promise to spawn candidates for future VLSI ICs with high-voltage power functions.

Researchers at North American Philips Corp., Briarcliff Manor, N.Y., are hunting for alternative technologies to make power ICs that combine high current and moderate voltages. Such devices are used in automotive and low-voltage motor-control applications. Their costs are dominated by the power elements that occupy over 50% of the chip area.

Interest at Philips focuses on a high-side switch design that combines a DMOS power structure with CMOS and bipolar control circuits. The 10-A, 60-V switch uses only 30% of the die surface for the power element, and is fabricated with 12 masking steps and standard LOCOS process isolation for low-voltage CMOS logic. Switch features include reverse-battery and short-circuit protection, and current-limiting circuitry.

ICs used in instruments that control jet engines, nuclear reactors, and cars must operate reliably in ambient temperatures exceeding 300°C. Yet the maximum operating temperatures of conventional silicon ICs are limited to 80 to 120°C, because leakage current increases at high temperature. To circumvent this limitation, engineers at the Toyota Technical Institute, Nagoya, Japan, propose using a reverse bipolar-transistor structure. Here, the collector is isolated from the substrate and emitter, with high carrier concentration contacted to the substrate.

When using this technique in an inverter test circuit implemented in integrated injection logic, the researchers observed a steady low-level output voltage of 45 mV between 50 and 370°C. The high-level output voltage decreased with increasing temperature at 1.8 mV/°C to 215 mV at 370°C, where the signal swing is 80 mV. The power-delay product is 58 pJ per stage, and the maximum frequency response is 7.6 MHz at 370°C.

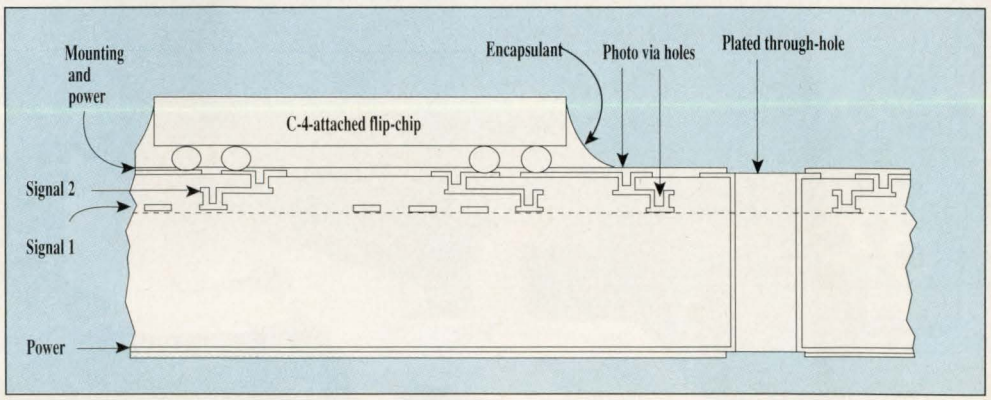
DAVE BURSKY, FRANK GOODENOUGH, and MILT LEONARD

SURFACE-LAMINAR-CIRCUIT TECHNOLOGY REDUCES COST OF DIRECT-CHIP ATTACHMENT

One major barrier that prevents the filtering down of direct-chip attachment from large computer systems to portable systems is the cost of the technology. To address this issue, researchers at IBM Corp.'s Yasu Technology Applications Laboratory, Yasu, Japan, developed a packaging technology called surface laminar circuit (SLC), which permits the mixing of flip-chip components, SMT devices, and through-hole components. The technology cuts board-production costs by its use of standard, commercial materials and production methods.

By using photosensitive epoxy to create insulating layers, the wiring density of SLC technology is double that of conventional pc-board technology. That's because the 130-μm-diameter photoetched vias are much smaller than those made by drilling. Plated through-holes can also be on the boards, though.

Although IBM doesn't consider it a multichip-module (MCM) substrate technology first and foremost, SLC technology is a big step toward reduced costs in direct-chip attachment, and could eventually be applied to MCMs more directly. What it does do is



enable IBM to fully exploit the densities advantages that surface-mounted components allow.

In fabricating the double-sided glass-epoxy boards, a copper-clad layer is etched with the wiring footprint. Then, a photosensitive epoxy resin is applied to the top side of the first signal layer to produce the first insulation layer, in which via holes are photoetched. The epoxy is then treated with permanganate to anchor the plating of a second copper signal layer. The signal lines are etched, a second insulating layer is applied, and a pad layer is plated and patterned on the mounting surface *(see the figure)*.

To achieve its cost reductions for portable electronics, the SLC technology uses standard, commercially available materials. It's also a process innovation in that C-4 flip-chips are attached using ordinary eutectic solder, which melts at 183°C instead of the 310°C for normal C-4 processing. This enables IBM to attach flip-chips in a board-assembly environment rather than a costlier, more tightly regulated MCM-assembly environment.

The boards, which can be as large as 500 by 600 mm in size, can handle flip-chip components with as many as 200 I/O lines, as well as TAB devices, plastic quad flat packs, and through-hole components such as PGAs.

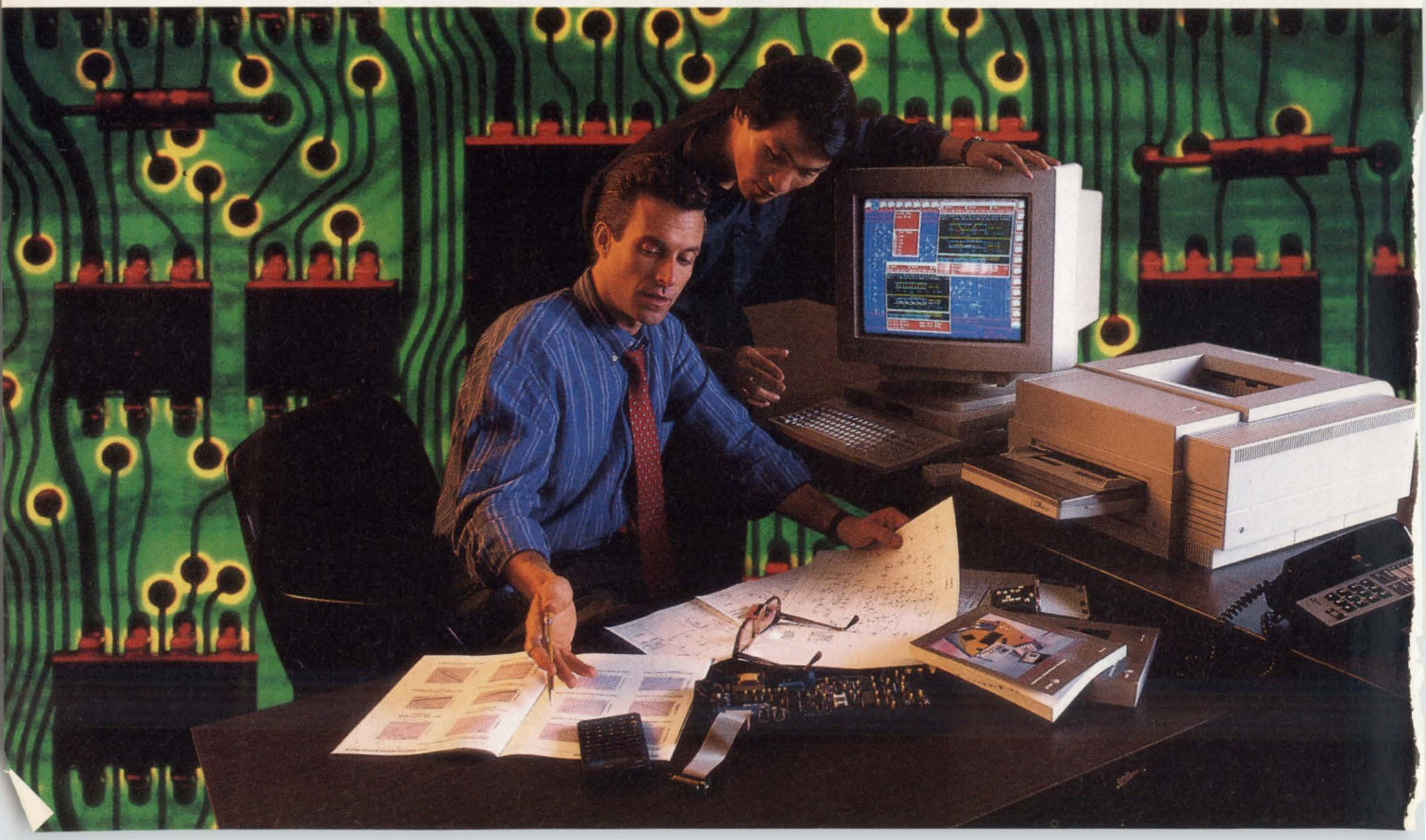
DAVID MALINIAK

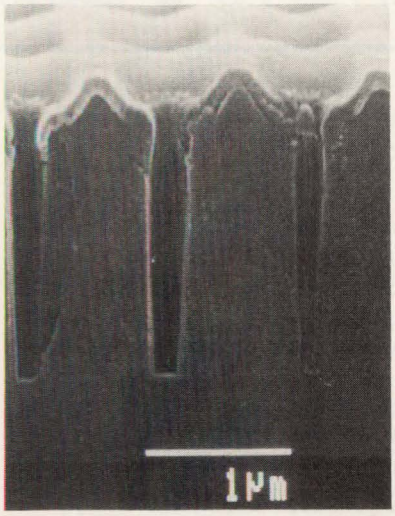
PHOTORESIST EXTENDS OPTICAL LITHOGRAPHY TO BEYOND 0.3 μm

A photoresist system developed at the corporate research laboratories of Siemens AG, Munich, Germany, allows IC structures to be made with feature dimensions below 0.3 μm, using conventional optical techniques. The Siemens researchers even succeeded in producing samples with even smaller dimensions—down to 0.25 μm, in some cases. Such a development has given photolithography a new lease on life, before such means as X-ray lithography must be used to get structures far down into the submicron range.

IC makers have already obtained structures far below 1 μm by purely optical techniques under production-line conditions, by improving the exposure equipment, employing sophisticated photoresist systems, and by computer simulation of the photolithographic process. But there are limits. Because of constraints imposed by physics, the exposure-equipment's depth of focus diminishes as light wavelengths become shorter and the apertures become larger. To get around this dilemma, Siemens developed the resist system.

The two-layer resist, in contrast to standard re-





sists, requires only a very thin and uniform film to be exposed. Siemens enlists a novel scheme in which the resist pattern is transferred, after exposure, onto a second underlying resist film by anisotropic dry etching. This underlying film, which is much thicker then the top one, ensures ideal exposure conditions for the thin film and at the same time constitutes a sufficiently stable mask for the etching processes.

To achieve the necessary etching resistance, the thin resist film is subjected to a simple chemical after-treatment. This process permits controlled expansion of the optically transferred structure and hence a controllable miniaturization of the free interstices exposed to the etching agent.

The chemical expansion of resist lines, the so-called CARL technique worked out at the labs, allowed 0.15-µm vias and isolation troughs to be produced *(see the photograph)*. The technique, however, requires the use of exposure equipment with an optical resolution of 0.4 µm.

While researchers at the Siemens laboratories in Erlangen came up with the two-layer resist system, their counterparts in Munich developed the CARL lithographic process. Mastery of this process enabled them to produce the 0.3-µm test structures on silicon wafers plus occasional 0.25-µm samples.

Together with improved high-aperture krypton-fluoride laser-exposure devices being developed at various places, the CARL technique will also be usable for regular 0.25-µm line-width technology. Also, because of its absorption properties, the resist system can be restructured for future argon fluoride laser exposure equipment with a 193-nanometer wavelength. A resolution below 0.20 microns would then be attainable.

By selectively modifying the phase position of the light at the mask level and at the exposure equipment's lens system (IBM is pursuing this approach) optical techniques will some day be practical to obtain dimensions down to 0.1 microns, Siemens says. Such dimensions would correspond to those of future gigabit memory chips.

JOHN GOSCH

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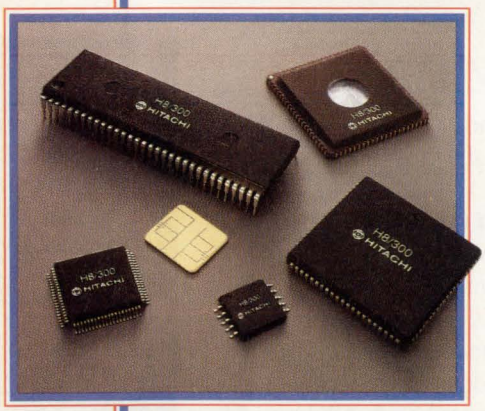

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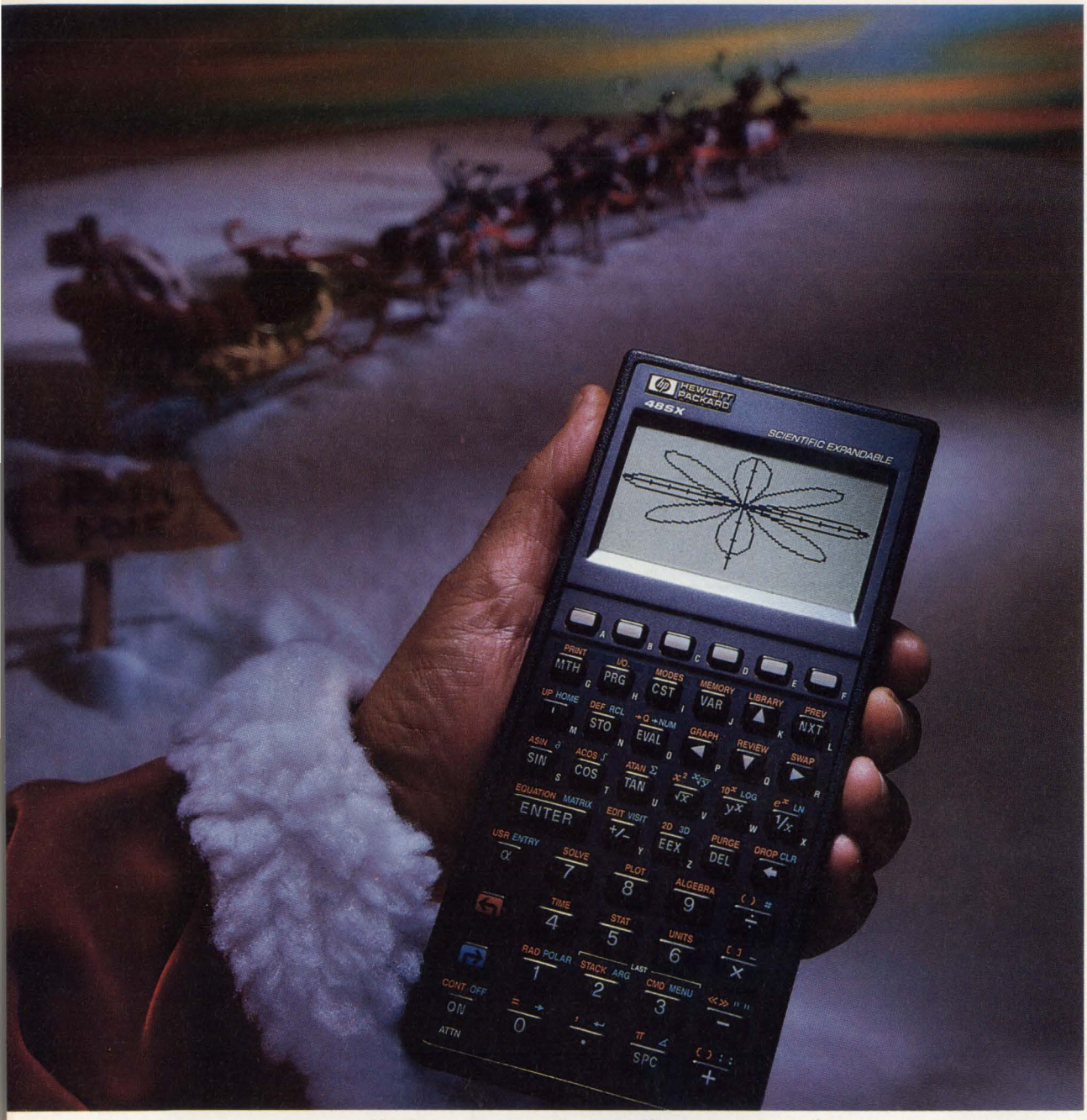

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A SENSOR MATERIAL WITH UNIQUE CHARACTERISTICS FINDS ITS WAY INTO AN ARRAY OF APPLICATIONS.

PIEZOELECTRIC-FILM SENSORS LEAVE NICHES BEHIND

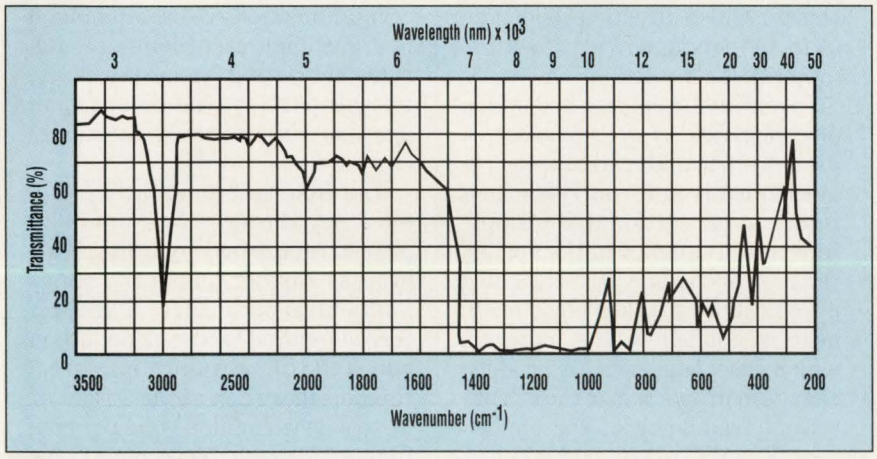
DAVID MALINIAK

Piezoelectric polymer film is an answer waiting for questions to solve. That's not to say that it isn't solving problems already in the areas of electronic switching, force and motion sensing, pyroelectrics, acoustics, ultrasound, and others. But after years of being overlooked and underutilized, these films, which transform a mechanical force into an electrical response, and, conversely, an electrical signal into a mechanical deformation, are exploding into a range of applications that expands almost daily.

Polyvinylidene fluoride (PVDF) film has a number of characteristics that make it uniquely applicable as a sensor material. It has a broad frequency response from close to zero up to the gigahertz range. Little resonant background noise is produced by the material, which is why some users regard it as one of the quietest sensor materials available. The material's acoustic impedance is very close to that of water, making it nearly ideal for hydrophonic applications. It's flexible, tough, easily configured into many shapes, and highly dimensionally stable. It also can be made in continuous lengths.

It was only in the early 1970s that PVDF film was brought to light as a new transducer *(see "PVDF's industrial origins," p. 38)*. Considering that only about a dozen transduction materials exist, the discovery of a new one should be the basis for a whole new segment of the sensor industry. Curiously, few manufacturers have taken up the banner of PVDF film, and not many more have seen fit to expand its applicability as a sensor material. But because the material is both piezoelectric and pyroelectric, it lends itself to many applications. PVDF film is available from two U.S. sources. It's called Kynar by Atochem Sensors Inc., Valley Forge, Pa., and Solef by Solvay Technologies Inc., New York, N.Y.

For its part, Atochem Sensors has seen fit to package the material in sensors and switches for various applications. Atochem's hope is to see its sensor and switch products incorporated into end-product designs. According to George Gerliczy, vice president of Solvay Technologies, the film is more likely to find its uses in new developments in which piezo film is the transducer of choice from the start of the design cycle. "I don't see piezo film as a replacement for

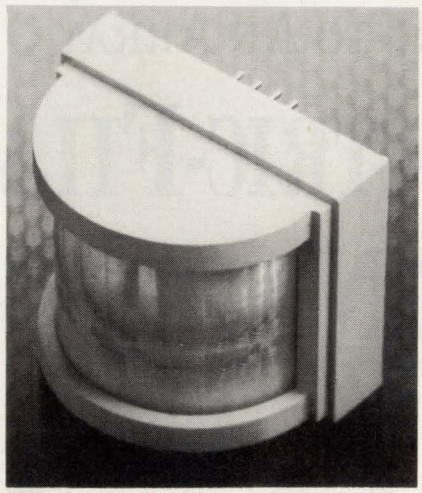


1. THE INFRARED absorption spectrum of piezoelectric polymer film shows a pronounced dip in transmittance in the 7-to-10-μm range, which corresponds to the infrared energy emitted by people. This accounts for the material's applicability as an environmental-control and security sensor.

devices already existing in other technologies," Gerliczy said.

The first broad application area is sonar. PVDF film is a very close match with water in terms of acoustic impedance and is very light in weight. And because it's matched to water, it's efficient as a receiver and even as a transmitter of acoustic energy into water. That attribute lends the film to a number of sonar applications, including hull-mounted as well as towed sonar arrays for submarine detection. In addition, the film can be produced in very large pieces of up to a kilometer in length, which is impractical with ceramic transducers. That makes fixed-installation sonar possible for piezoelectric film.

The second large group of applications is infrared detectors, for which PVDF-based sensors are an attractive alternative to more costly piezoelectric crystals. According to Victor Chatigny, president of Atochem Sensors, the future of piezo-film sensors for infrared detection lies in the area of complex infrared arrays. "Because PVDF film can be made in sheets less than 10-μm thick and can have very complex electrode patterns applied to it, we can produce an infrared array on one sheet of film rather than building an elaborate mosaic of tiny crystal chips," Chatigny explained. This infrared array can then sense infrared energy and the output of each pixel is proportional to the amount of infrared energy absorbed by the material. The end result is a kind of camera, or, more precisely, a pyroelectric charge-coupled device.



2. THANKS TO its flexibility, piezo film can be curved into an infrared sensor with a 180° field of view. This module's dense beam pattern detects motion more than 20 feet away.

The development of such applications began with energy-management systems, which remain a growing and popular application. Piezo film exhibits excellent pyroelectric response, particularly in the 7-to-10-μm range, which happens to correspond with the infrared energy radiated by human beings *(Fig. 1)*. Therefore, these sensors can detect the presence of a person in a room and control lighting, heating and air conditioning, or both.

In most cases, infrared detectors in a room are corner mounted. It would be preferable to have them located at the light switch, but because they don't offer a 180° field of view, such arrangements are impractical; corner mounting is required to observe the whole room.

PVDF'S INDUSTRIAL ORIGINS

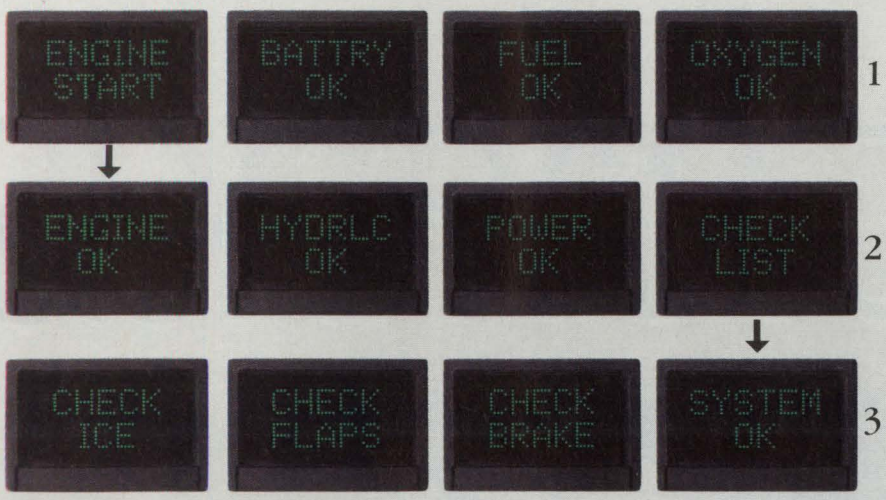
Since its discovery by the Curies over 100 years ago, the piezoelectric effect has found most of its practical application in sonar. Quartz, which was the original natural material found to exhibit the effect, was augmented during World War II by poled ceramics. Then, in the late 1960s, researchers discovered that a polymer known as polyvinylidene fluoride (PVDF) was more strongly piezoelectric than any other known substance. The polymer, a cousin of Teflon, had been used for years as a weatherproofing coating for buildings, a wire-wrap material, and an anticorrosive lining for pipes.

Piezoelectricity takes the first part of its name from the Greek word for pressure, which provides a clue to its nature. Applying pressure to a piezoelectric material (which includes quartz crystals, polarized ceramic, PVDF, and human bone, among others) causes the material to produce a charge proportional to the applied force. Conversely, the material draws in charge when the pressure is relaxed. The effect can be compared to water in a sponge. The frequency of the produced charge is also directly proportional to the frequency at which the material is stressed.

In addition, applying an outside electrical field to two surfaces of a piezoelectric material causes it to mechanically deform. This effect is also in proportion to the amplitude and frequency of the applied field. A secondary effect, called pyroelectricity, takes place when heat is applied to the material, which also causes it to produce charge in proportion to the quantity and frequency of the applied heat. The PVDF polymer is one of few materials that can interconvert electrical and mechanical energy (piezoelectric) as well as thermal and electrical energy (pyroelectric).

Piezoelectric polymers are formed by extruding or casting a sheet of the plastic, and then orienting the material by stretching it. Stretching, which is performed at ratios of up to 5:1, aligns the crystalline molecule chains much like uncoiling a garden hose. Besides imparting some piezoelectric properties, the orientation process substantially strengthens the film.

The film isn't inherently piezoelectric, though, but must be primed for the task by poling. This process further aligns the film's molecular structure. The preferred method is corona poling, in which the film is subjected to a corona discharge in air at a field of up to several million volts per centimeter for 40 to 50 seconds. This method permits continuous poling for production of large quantities of film, which reduces its cost.



AN APPLICATIONS EXAMPLE. While the following example is for aircraft, it could apply to any air, land, sea or space system.

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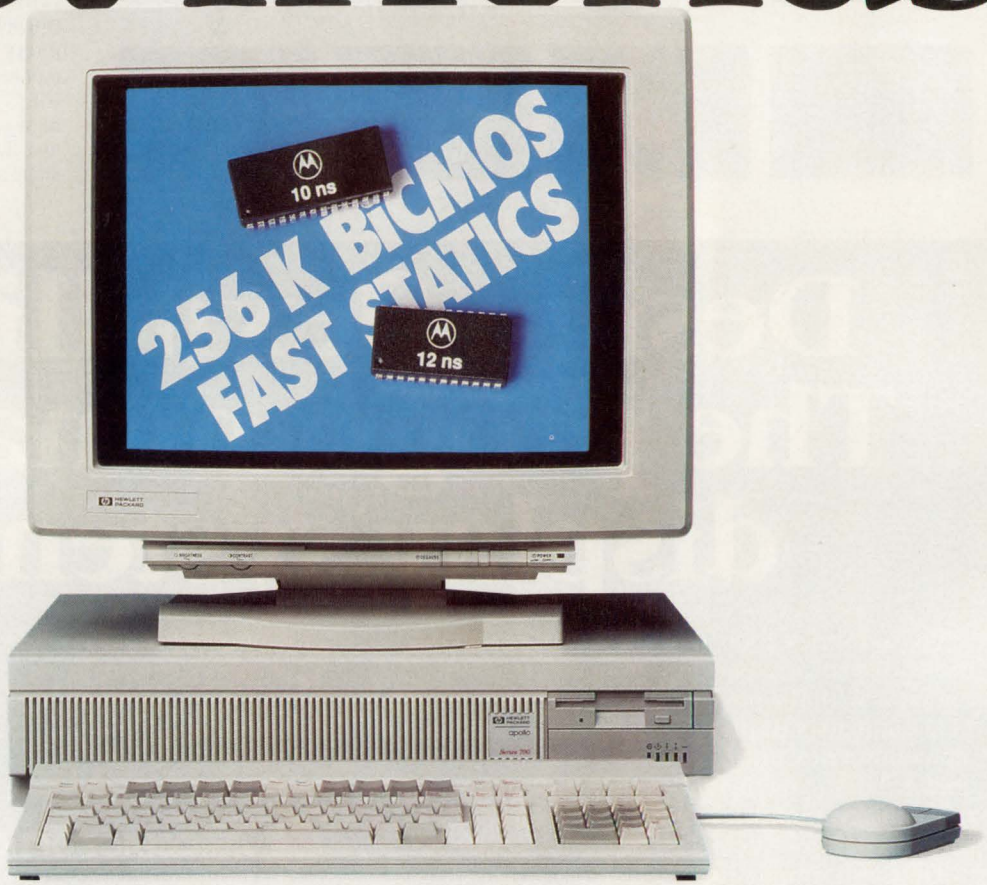

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PIEZO-FILM SENSORS

That's where PVDF film has an advantage compared with crystal-based sensors. The flexibility of piezo film permits it to be curled into 180° hemispheres. A complex array can be applied to the surface of the polymer by sputtering, etching, or laser trimming (or any electrode-depositing technique), yielding a very densely patterned, wide-angle sensor that can replace the mechanical switch at the light-switch location and "see" the whole room. In addition, because of the complexity of the metalized pattern (down to 1-mil pitch), so many different beam patterns and signals can be produced that at a distance of 20 to 25 feet, a wave of the hand is enough to retrigger the circuit. Also, the film-based sensors have sensitivity equivalent to that of crystal-based sensors.

Earlier this year, Atochem Sensors rolled out a detector and lens in a plastic package and called it a passive infrared module *(Fig. 2)*. This fall, they'll introduce the next generation: a 0.5-in.-thick infrared detector and lens combination with a 180° field of view and a range of 15 to 20 feet. The device's profile would be no greater than that of a wall switch.

The future of infrared detection is in increasingly complex arrays, which range from low-resolution to very-high-resolution imaging. An example of low-resolution imaging would be the ability to distinguish a human being from a dog. A more complex array might be found in the night-vision scope of an M16 rifle. A very complex array would be used in satellite-based reconnaissance. As complexity grows, the film's advantages become more apparent.

Another major application field for piezo film is accelerometers and vibration sensors. The relatively inexpensive film can readily be fashioned into a very broadband, highly sensitive acceleration sensor. Piezo film can be configured as either a beam-type sensor for low-frequency seismic applications or a mass-loaded accelerometer design for broadband, high-shock applications. According to Chatigny, a piezo-film-based acceleration sensor, which can be produced for less than $5 in OEM quantities, delivers performance in applications such as automotive airbags equivalent to many instrumentation-grade accelerometers that cost $500 or more. The alternative, which is quartz or piezo ceramic, must be polished or ground and often prestressed to be able to withstand the shock that these units are exposed to. This fabrication process is time-consuming and requires a high degree of precision. But because it can be extruded into thin and very uniform sheets, piezo polymer can be cut into any desired shape. And because the film can withstand shock loads several orders of magnitude higher than ceramic or quartz, the film doesn't need to be prestressed and the mass it's applied to doesn't have to be bolted down.

Piezo-film-based accelerometers compare favorably to those based in other technologies, including micromachined-silicon types, Chatigny claims. "We have consistently been told that the performance of our piezo sensors is equal or superior to that of micromachined silicon sensors," said Chatigny. One caveat when considering piezo film as opposed to micromachined silicon, however, is the film's inability to produce a dc response. The lowest frequency piezo film can observe is about 0.001 Hz. The most compelling advantage for piezo film, however, is that it offers simplicity of design, which may imply a reliability that may be missing from some more exotic options. It's also available as a solution today at a highly competitive price.

As for its technical advantages as an accelerometer, piezo film can withstand very large shocks. The Department of Defense has used it to measure underground weapons-testing shocks of 300,000 atmospheres, says Chatigny. In addition to being inexpensive, the film has very high sensitivity, and withstands temperatures to 135°C.

In the field of vibration and acceleration, some of the earliest work with piezo film was in contact microphones. A piece of film could literally be attached to a surface with double-sided tape and tied into either an oscilloscope, tape recorder, or datalog-

PIEZO-FILM SENSORS

ger. Thanks to a frequency response that ranges from 0.001 Hz to 10 GHz, the film reproduces the incoming vibrational energy. Its frequency response is very flat in the audio range and is even flat at tens to hundreds of megahertz. This lends the film to applications as an acoustic pickup for guitars and violins. As a strain gauge, it has been used in frequencies from a fraction of a hertz to a few hertz to tens of hertz.

According to Chatigny, engineers seem to be more comfortable working with accelerometers to measure vibration than they are with stick-on dynamic-strain-gauge tapes. "That's a whole new technology; we spend a great deal of time on that area to help people realize that in some of these applications, an accelerometer can be easily replaced with a contact microphone to measure bulk-wave vibration sensing," Chatigny said.

One of the most active areas of development for piezo-film sensors is active vibration damping. Basically, piezo film is both a speaker and a microphone. For example, the film can be mounted on the fuselage of an aircraft. As a microphone, it can listen to the incoming vibration frequency, and in real time, a second piece of film can, at 180° out of phase, cancel that vibrational energy. Atochem Sensors is working on military and aerospace applications in noise cancellation. Automotive applications are another possibility. Noiseless mufflers and passenger compartments are potential uses for these active vibration systems in the commercial and industrial marketplace. The potential for automotive applications, however, is limited by the film's heat tolerance. At a maximum 135°C, it can melt when placed directly on a muffler.

Another major application area for piezo film is in switch and impact sensors. Atochem markets what it calls its Smart Switch, which is a monolithic switch that doesn't rely on switch closure. Even so, the switch is passive in the sense that it doesn't require application of an electrical signal. When touched lightly, the film develops 10 V into a 10-MΩ input impedance. That's more

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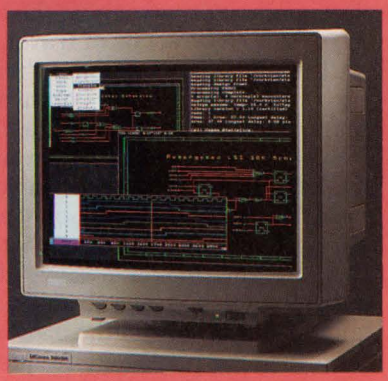

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than suitable for directly driving CMOS circuitry as a wake-up switch.

As a switch, the film produces a signal that is dynamic, not static. Touching it produces a positive-going pulse. Conversely, releasing it produces a negative-going pulse. So output is induced only for changes in stress, not static stress levels. Using high-impedance circuitry, however, signals from 10 to 40 ms in duration can be produced with finger pressure. This appears to the circuitry as a conventional switch closure.

The material's dynamic nature makes it impossible to interrogate the switches' instantaneous state (open or closed) directly. One can, however, use the piezo effect to make the switch appear static rather than dynamic. This is done by bonding two piezo films to opposite sides of a substrate. One film (the output, or "speaker") is driven with a frequency corresponding to the substrate's resonant frequency. The induced mechanical vibration generates a corresponding charge in the other (the input or "microphone") film. Then, any physical contact with the assembly will change or suppress the substrate's resonant frequency. The system can then determine whether the switch is "singing" (open) or "gagged" (closed).

Yet another advantage of piezo switches is their thinness. At dimensions as low as 28 μm, they're useful in ultra-thin packaging designs such as palmtop-computer keyboards or armored switch plates, where low deflections of a stiff metal plate must be sensed reliably.

Piezo-film switches respond proportionally to the amount of input, allowing for calibrated switches. In some applications, designers may want the film to respond in one way if the impact is soft and another if it's harder. Examples might include sports scoring, measuring the speed of a thrown ball, determining where a golf ball hits a target, or what its trajectory might have been. In other instances, the switches might serve applications in which the threshold levels are established and a response is required only if the impact force is at a certain level or higher.

Impact switches are also useful when it's important to know the amplitude of the input event. This applies especially well in traffic counting and vehicle classification by roadway sensors. A piezo-film sensor can tell not only how many axles pass over it, for example, but also what the weight of each one was. On an airport taxiway at night, the sensors can tell traffic controllers the class of aircraft moving on the taxiway and their direction of travel.

Ultrasound applications, divided into the broad categories of medical imaging and nondestructive testing, are yet another major area for piezo sensors. In medical applications, piezo film as thin as fractions of a mil can be wrapped around catheters, making it suitable for invasive ultrasound imaging. Such transducers can probe deep within the body and, because of the film's high frequency response, they do so with very high

PIEZO-FILM SENSORS

resolution. "The film's advantage in such applications is its good acoustic-impedance match with water, which, of course, is a major constituent of the body," said Solvay's Gerliczy.

Other medical applications include monitoring vital signs and apnea monitors for sudden-infant-death syndrome. In such cases, the film can be used to monitor respiration and heartbeat. It's also useful for gauging blood flow and pressure.

Nondestructive testing with piezo film applies especially well to the emerging classes of advanced composite materials. A skin of piezo film is applied to these materials, and upon pulsing the material with ultrasound, it can sense delaminations, voids, or cracks. The transducer is activated and identifies the location and size of the defect. Piezo film, which is well matched to the materials, can be fabricated in very-large-area, complex electrode skins that are thin, lightweight, and offer very high resolution. Operating frequencies run from 40 kHz to 10 MHz.

In niche applications, there's plenty of room for imagination in using piezo film. Its many and varied properties give designers a great deal of latitude in situations where ceramic just won't do. One interesting use for the film takes advantage of its inherent capacitance, which Atochem specifies at 380 pF/cm^2 for 28-μm-thick film.

According to Jim Hewlett, senior staff engineer at KDI Precision Products Inc., Cincinnati, OH, that capacitance is what forms the basis of his company's safe and arming fuse for 20-mm ammunition shells. When stressed by the acceleration of firing, a piece of film inside the shell generates and stores charge. When the shell hits its target, a switch closes and applies the film's stored electrical energy to a detonator, which in turn explodes the shell. The fuse makes the shell safe for handling because only the acceleration of firing generates enough charge to explode the detonator.

"Piezo ceramic is more sensitive and is capable of generating more energy for a given stress," Hewlett explains. "But the advantage of piezo film lies in the fact that the ceramic is brittle and breaks. The plastic film can be stressed repeatedly, which permits me to test it before installing it in a shell."

Some potential and as yet unexploited applications for piezo polymer film include energy generation on a large scale. Chatigny envisions using piezo film in large sheets for ocean-wave power generation. The films could be suspended in the ocean using submerged flotation barges. As ocean waves pulse the films, they would produce 5 W per pound of high-voltage, very-low-frequency power, which could then be transferred directly to the on-shore power grid.□

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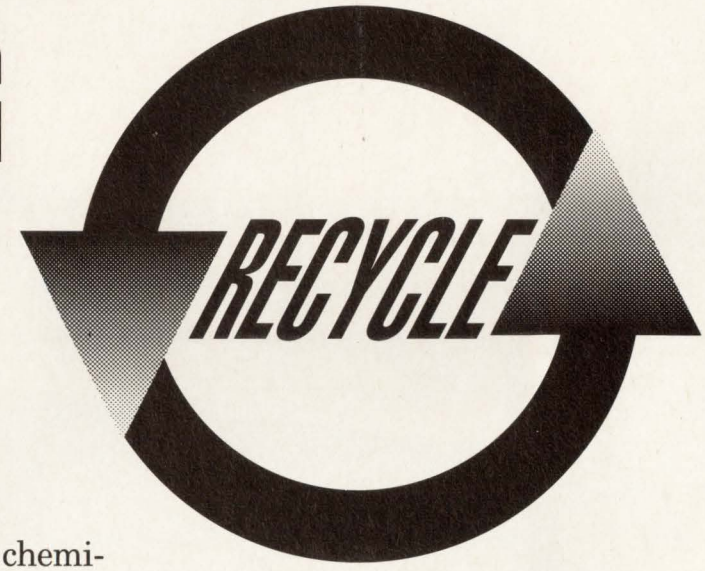

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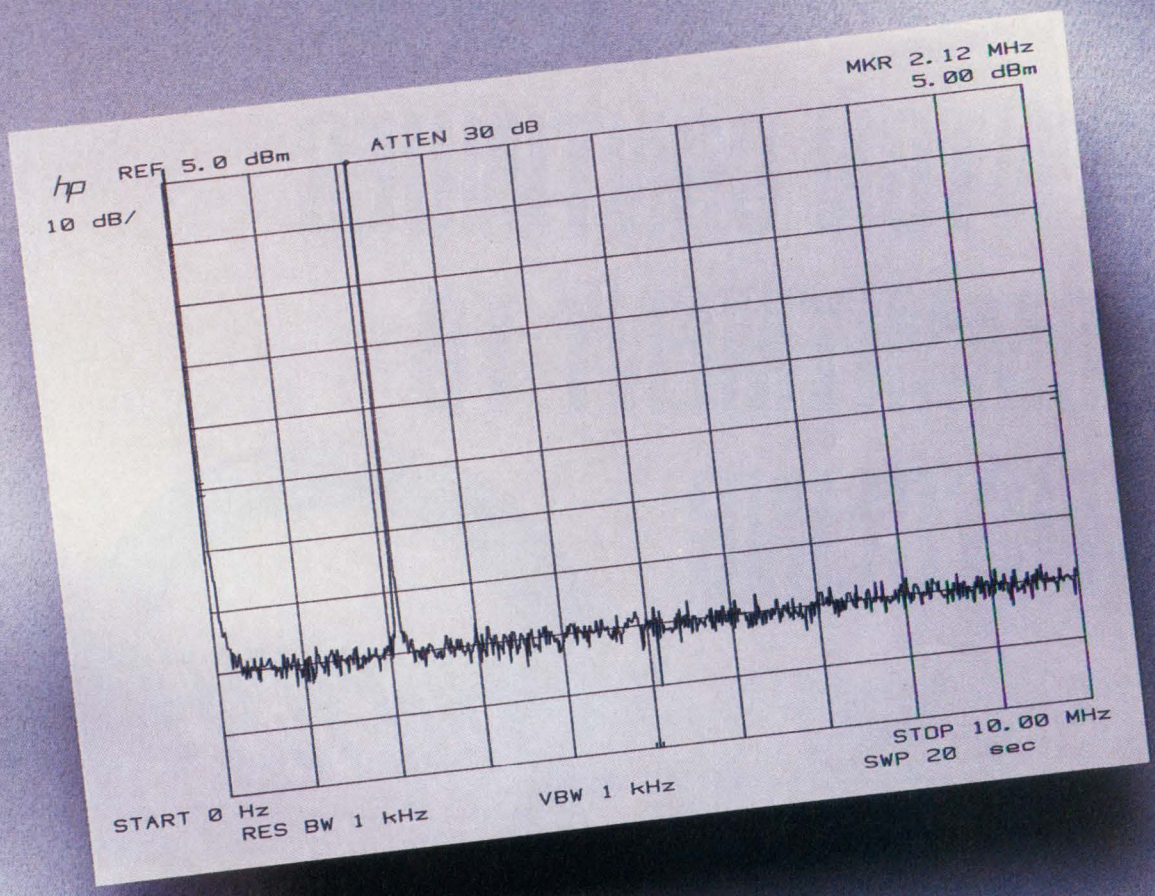

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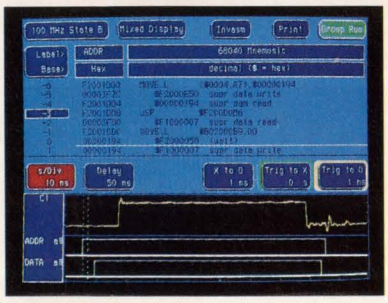

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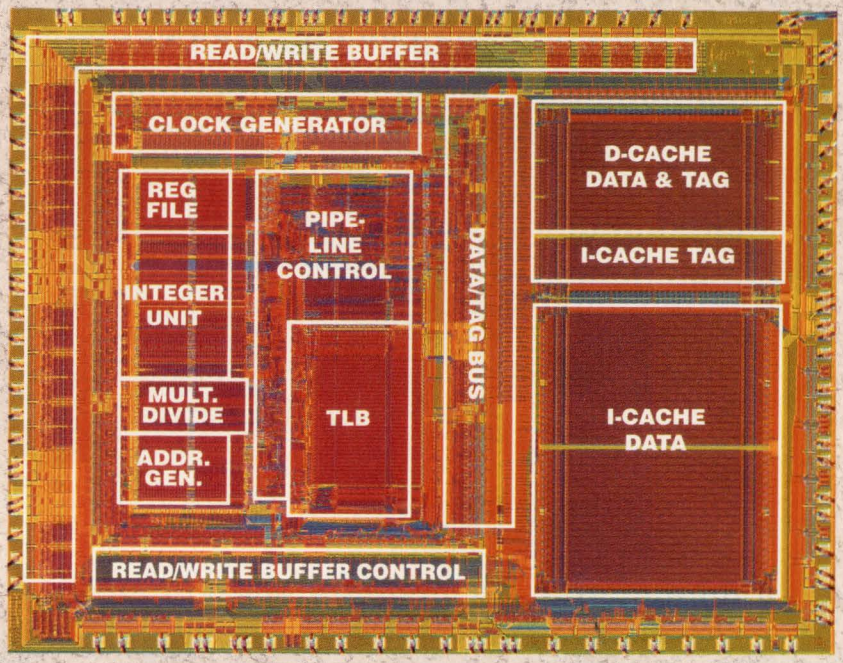

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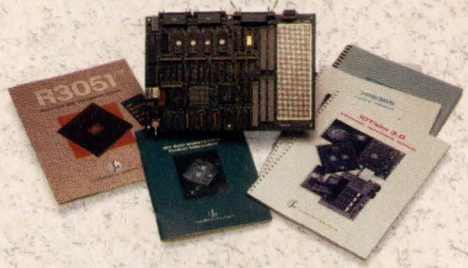

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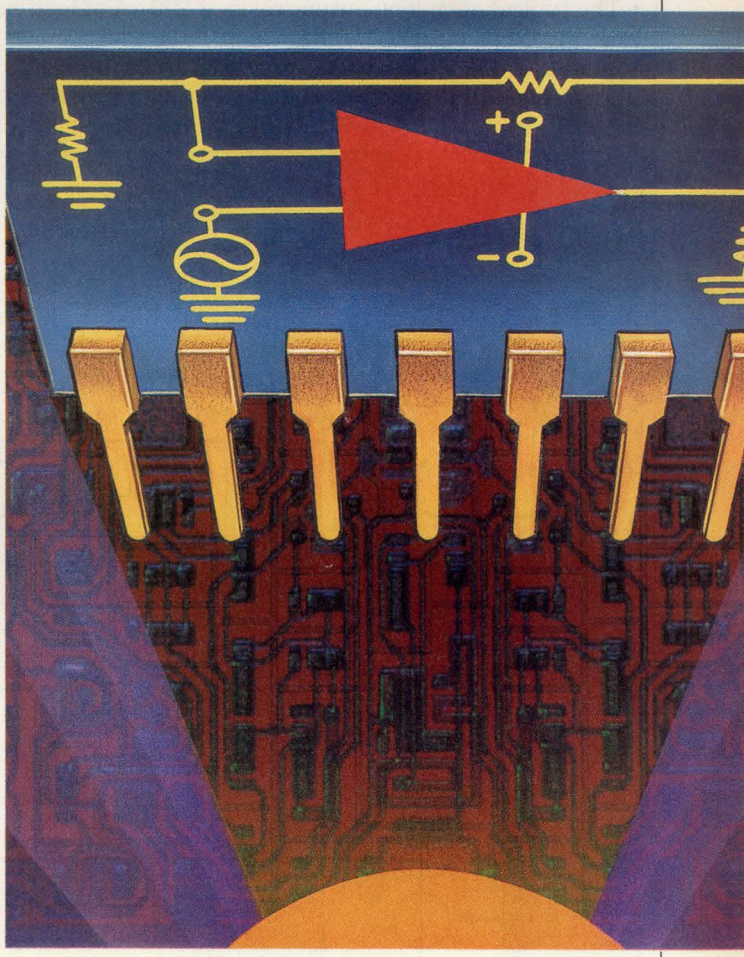


In many applications—laptop PCs and automobiles being two standouts— amplifiers are not required to drive the output load continuously. In these applications, energy efficiency (spelled "battery life") is highest if circuits operate in a mode that consumes just enough power to detect incoming signals. Once they detect a signal, they can shift to a high-performance mode on demand. That's the thinking behind a patented circuit topology from Motorola called "Sleep Mode." The company's MC33102, a dual op amp with a standard miniDIP pinout, represents the first of a broad family of ICs using the new technique.

ICs incorporating Sleep Mode draw minimum current from the supply rails unless sourcing current from or sinking current to a load. The technology is initially aimed at two application areas: those now usually filled by so-called "micropower" ICs offering limited drive capability, bandwidth, and precision; and those that need only offer high performance intermittently.

Guaranteed to run off supply rails from ±2.5 to ±15 V, each of the MC33102's two op amps draws a maximum of 65 μA from the supply rails under no-load conditions. When the load current of either op amp exceeds 200 μA, internal circuits automatically increase each op amp's operating current to 900 μA. Each op amp can then put ±13.6 V of 20-kHz audio across 600 Ω without cross-over distortion. Unlike earlier micropower op amps, once the MC33102 is awake, neither output-drive power, slew rate, bandwidth, nor open-loop gain are sacrificed.

Even while asleep, the circuits still operate as true op amps. The load current of each remains a function of its input signal, closed-loop gain, and load resistance, while operating (quiescent) current determines output resistance, slew rate, and open-loop gain. A circuit in each op amp continually senses load current and switches in additional operating current when the load-current threshold is exceeded. Waking up takes just 4 μs *(Fig. 1)*.

During the wake-up process, the added operating current changes the op amp's basic

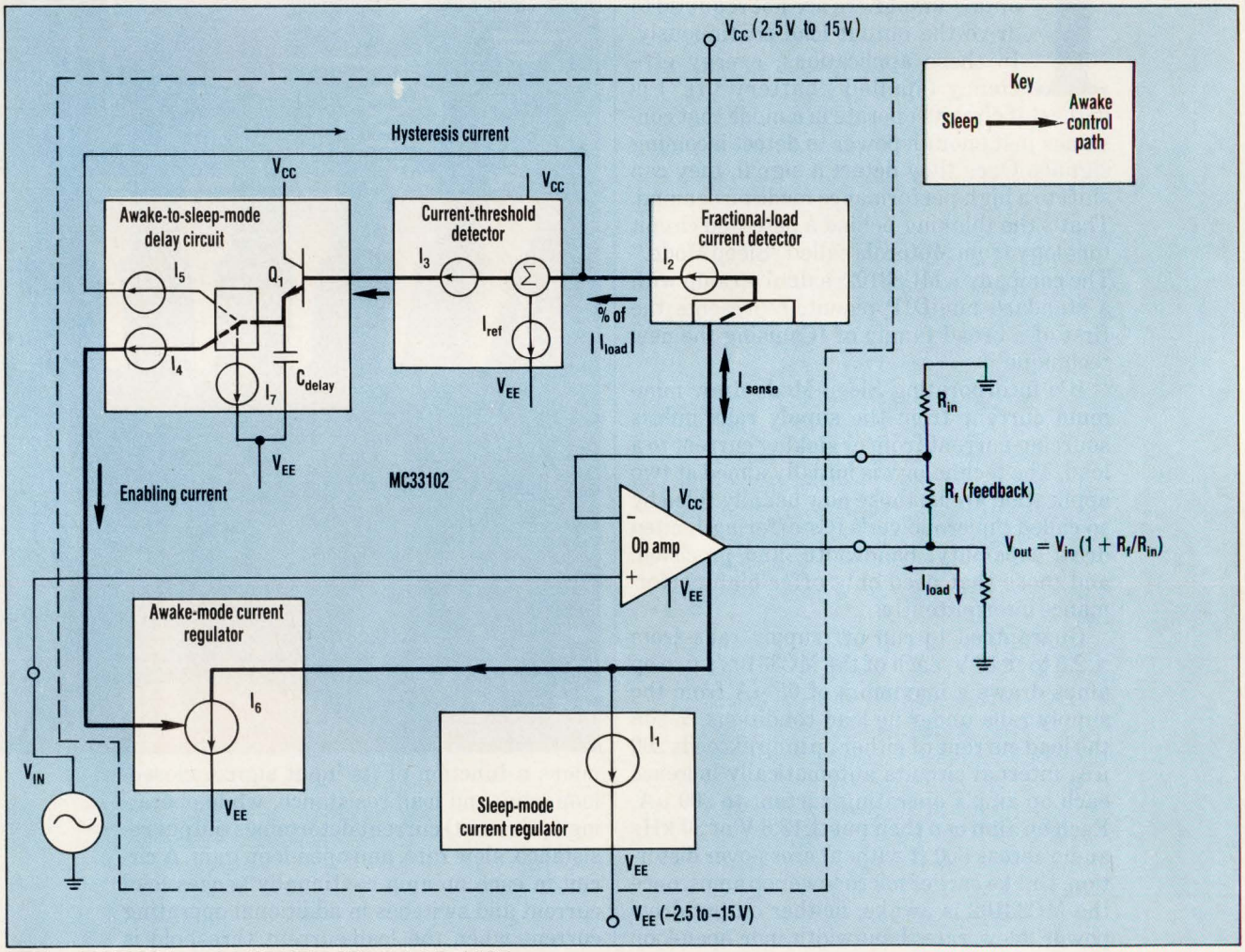
dynamic specifications in the following manner:

- The minimum open-loop gain increases from a very useful 88 dB, while asleep and driving 1 MΩ, to 94 dB while awake and putting ±13.6 V across 600 Ω.
- The minimum gain-bandwidth product of these unity-gain-stable op amps goes from 250 kHz, measured at 10 kHz, to 3.5 MHz measured at 20 kHz.
- The minimum slew rate goes from 0.1 V/μs to 1 V/μs, which translates into a typical full-power bandwidth of 20 kHz while awake.
- The typical open-loop output resistance drops from 1000 Ω while asleep to under 100 Ω while awake, resulting in an output-current capability increase from 150 μA to 50 mA. And output current doesn't start to be limited until it reaches 100 mA.

To eliminate oscillation between sleeping and waking conditions, which could be decidedly annoying in most applications, about 20 μA of hysteresis insures that the load current drops below 140 μA before the op amp falls asleep. In actuality, the mode-change transition currents are a function of supply voltage, the values stated previously applying at ±15 V. However, the chip typically starts to function with about ±1 V on the supply rails. With ±2.5-V rails, it will typically wake up with 200 μA of load current and go back to the sleep mode when load current drops to 180 μA. The MC33102's data sheet provides plots of both on and off threshold currents for supply voltages between (and outside) the range of specified values.

No Crossover

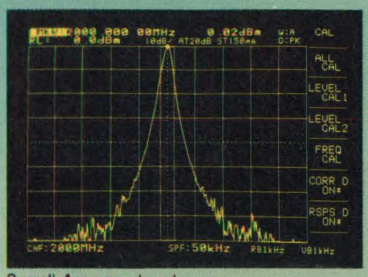
If by now you think this might be a nice chip for portable audio products (and it is), you're already asking the question, what happens every time an ac signal goes through zero? Doesn't the circuit go to sleep, causing a disaster in the form of severe crossover distortion *(Fig. 2a)*? The answer to that lies in a simple circuit that delays turn-off time by 1.5 s, permitting operation well below 1 Hz *(Fig. 2b)*. Any effects of turn-off would show up as total harmonic distortion (THD). In fact, while the op amp is awake and putting 2 V pk-pk across 600 Ω, THD typically runs 0.005%, 0.016%, and 0.031%, at 1 kHz,

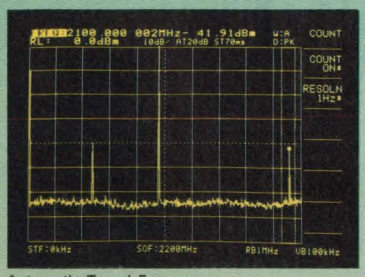


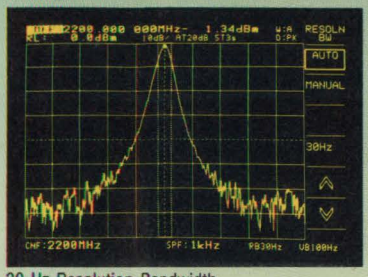
1. THE MC33102 SLEEP-MODE OP AMP wakes up when the load current, I_{load}, exceeds a preset threshold (about 160 μA) as sensed by the fractional-load-current detector and compared with the reference current I_{ref}. When the threshold is exceeded, the awake-mode current regulator turns on, providing the op amp with the operating current (about 800 μA) needed to put ±10 V of 20-audio across 600 Ω.

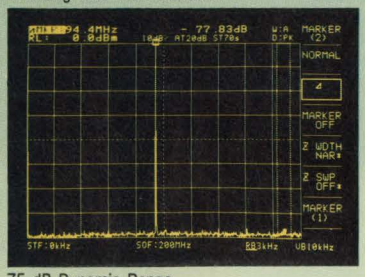
MULTIPLE CHOICE

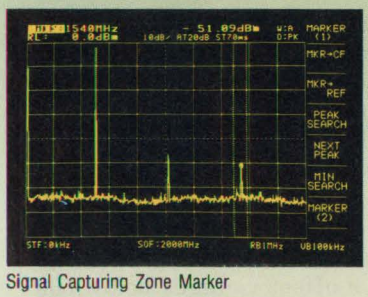
12 More Reasons For Taking A Closer Look At The MS2601B Spectrum Analyzer

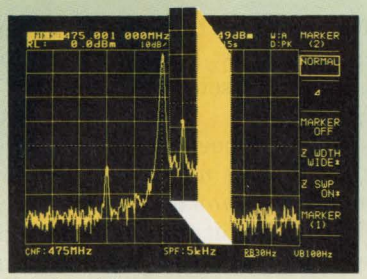

Overall Accuracy Level of ±1dB

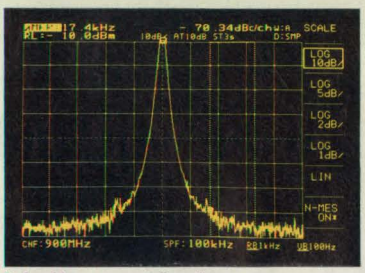

Automatic Tuned Frequency Counting with 1Hz Resolution

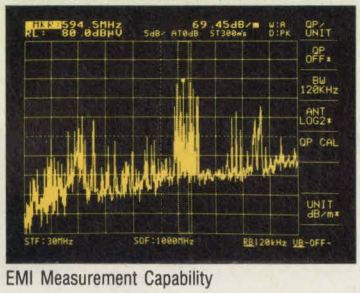

30 Hz Resolution Bandwidth

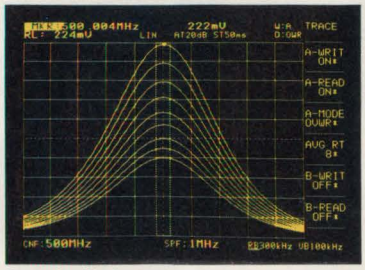

75 dB Dynamic Range

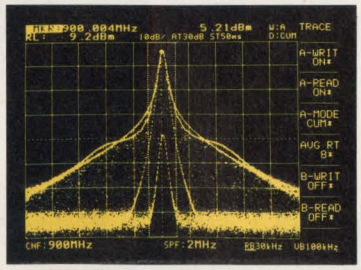

Signal Capturing Zone Marker

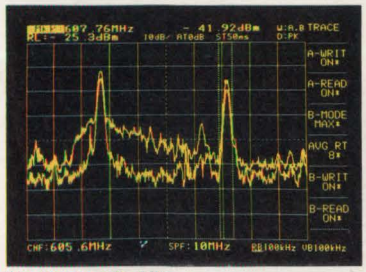

Reduction of Measurement Time Through Zone Sweeping

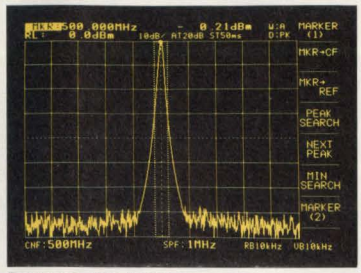

Noise Measurement Functions


EMI Measurement Capability


Overwrite Display


Cumulative Display


Simultaneous Dual-Trace Display


Frequency Axis Scrolling Function

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- Dynamic Range: 75 dB
- Frequency Response: ±0.5 dB (100 Hz~2 GHz)
- Built-In Quasi Peak Detector (VDE/FCC)
- Noise Measurement Capability dBc/Hz
- High Speed Measurement with Zone Marker and Zone Sweep

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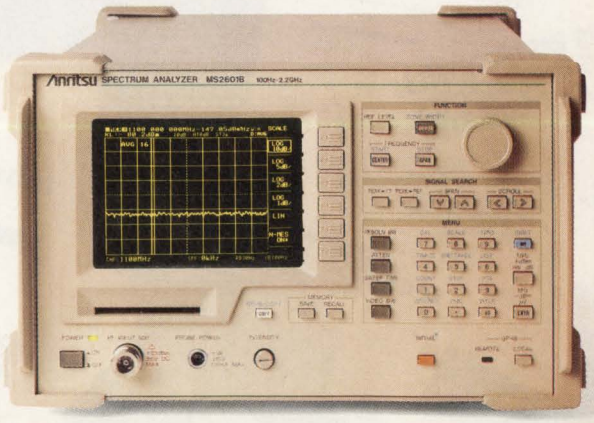
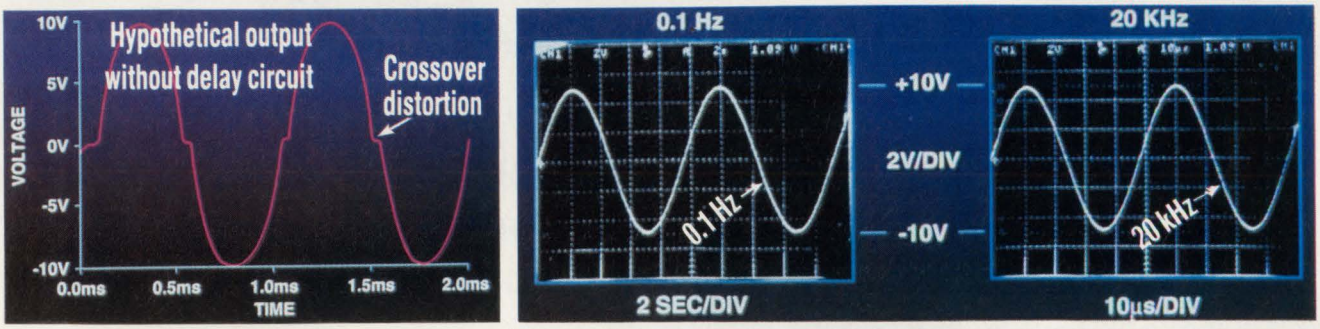


CIRCLE 90 FOR U.S. RESPONSE

CIRCLE 91 FOR RESPONSE OUTSIDE THE U.S.

SLEEP-MODE OP AMPS



2. NO CROSSOVER DISTORTION at sine-wave zero crossings (a) is achieved by a one-second delay circuit which permits operation of the sleep-mode op amp from below 1 Hz to beyond 20 kHz (b).

10 kHz, and 20 kHz, respectively.

On the other hand, since the MC33102's dual op amps are true op amps in either mode, these amplifiers can be used for dc instrumentation. That's because their full-power bandwidth is still more than 1 kHz when asleep, well above the frequency at which they drop off to sleep. Moreover, they offer a reasonably good maximum offset voltage of 2 mV and an offset-voltage temperature coefficient (tc) of just 1 μV/°C. Furtl ermore, typical offset voltage is just 150 μV.

Good application engineers learn early on to tell customers *never design to typical specifications*. However, the order-of-magnitude discrepancy between guaranteed and typical MC33102 specifications (such as this offset voltage) demands an explanation, and maybe a change in the admonition "*never*". That's because for several years *all* guaranteed specifications of virtually all Motorola ICs have been held to 6-sigma quality standards. That is, only about one MC33102 in a million will have an offset voltage beyond $\pm$2 mV—and a very large percentage will have offset voltages below 500 μV. So if you have the ability to accu-

SLEEP-MODE OP AMPS

rately test offset voltage fast, you may be able to get a lot of low-offset-voltage op amps for less than a dollar each. And with an offset-voltage tc under 1 μV/°C, albeit typical, the price will stay low.

Additionally, if kept asleep by driving a high-impedance load, say more than 100,000 Ω, the MC33102 can be employed as a micropower op amp down to dc. It will wake up if needed in just 4 μs while driving 600 Ω. It takes only 15 μs to wake up while driving 10 kΩ.

Battery-powered applications for these op amps range from microphone amplifiers to musical-instrument amplifiers. Other applications include general-purpose signal generators, special-purpose telecommunications test equipment, cordless and cellular telephones, and 24-hour (or more) EKG and other medical recorders. While initially aimed at consumer, automotive, telecommunications, medical and industrial applications, the range of uses should take off once designers of military systems get wind of these op amps. With the rush to multimedia applications accelerating, they could find their way into laptop PCs as well.

While Motorola is playing its cards close to the vest on future sleep-mode chips, it's not hard to envision new members of the family. To start, a single-supply version will find many additional applications. And since the turn-off delay is implemented with a capacitor, it can be made user-settable by bringing out a pin on which to attach an external capacitor. A package with additional pins could fit the bill, or a single-op-amp version could be put in an 8-pin DIP or SOIC. Since the present circuit charges the capacitor rapidly (4 to 15 μs) and lets the charge leak off slowly, however, an increase in delay time may increase wake-up time.

Other potential versions include a logic-level-flag output to let a processor know whether the op amp is asleep or awake, and/or a control input to let the processor change the mode as required. A high-power version, say 10 to 20 W, seems capable of saving lots of battery power in portable audio amplifiers. Since video amplifiers and buffers are real power hogs, moving the technology to a high-speed process and building the op amp into video circuits could truly save battery life in future video systems of all types (for example, camcorders). Other possibilities emerge when considering adapting sleep-mode technology to comparators, analog-to-digital and digital-to-analog converters, and even low-drop-out linear and switching voltage regulators—no load current and no quiescent current.

OK, Now Wake Up

The chip is built on a new, fine-geometry, standard (non-complementary), 36-V bipolar process called EPIMAX. At its heart lies an op-amp block employing a relatively conventional IC op-amp design, albeit using

an all-npn, class-AB output stage to optimize bandwidth. Five additional circuits, however, provide the chip with its unique performance: the fractional-load-current detector, the current-threshold detector, the awake-to-sleep-mode delay circuit, the awake-mode current regulator, and the sleep-mode current regulator *(see Fig. 1, again)*.

When asleep, the amplifier's operating current is set by the sleep-mode current regulator, a current source I_1. When an input signal (V_{in}) is applied to the amplifier, creating an output voltage and a load current (I_{load}), the fractional-load-current detector subtracts the dc operating current in the output stage from the load current and sends I_2, a small fraction of the absolute value of the load current, to the threshold detector. Absolute-value circuitry (precision full-wave rectifiers) permits the detector to handle the load current, whether the output is sourcing or sinking current.

The threshold detector is essentially a current-in current-out comparator. When its input current (I_2) from the load-current detector exceeds the preset threshold current I_{ref}, current source I_3 turns on and drives the awake-to-sleep mode-delay circuit. I_3 charges the capacitor C_{delay} quickly through emitter-follower transistor (Q_1), its (Q_1's) base being driven by the input current I_3. When the capacitor is charged, the delay circuit's two current source outputs, I_4 and I_5, turn on. I_4 enables the awake-mode current regulator I_6, while I_5 represents the on-chip positive feedback that provides the hysteresis current. The awake-mode current regulator I_6 gives the op amp the operating current it needs to drive low-impedance loads at audio frequencies.

When the load current drops below the threshold established by the current-threshold detector, I_3 turns off, then Q_5 turns off, and the storage capacitor starts its one-second discharge via I_7. At the end of one second, I_4 turns off, in turn, turning off I_6. The op amp then goes back to sleep. □

Price And Availability

Rated for the extended-industrial-temperature range, the MC33102 dual sleep-mode op amp offers the industry standard footprint for dual IC op amps in both 8-pin DIP and 8-pin SOIC packages. In quantities of 10,000, both package versions go for $1.60 each.

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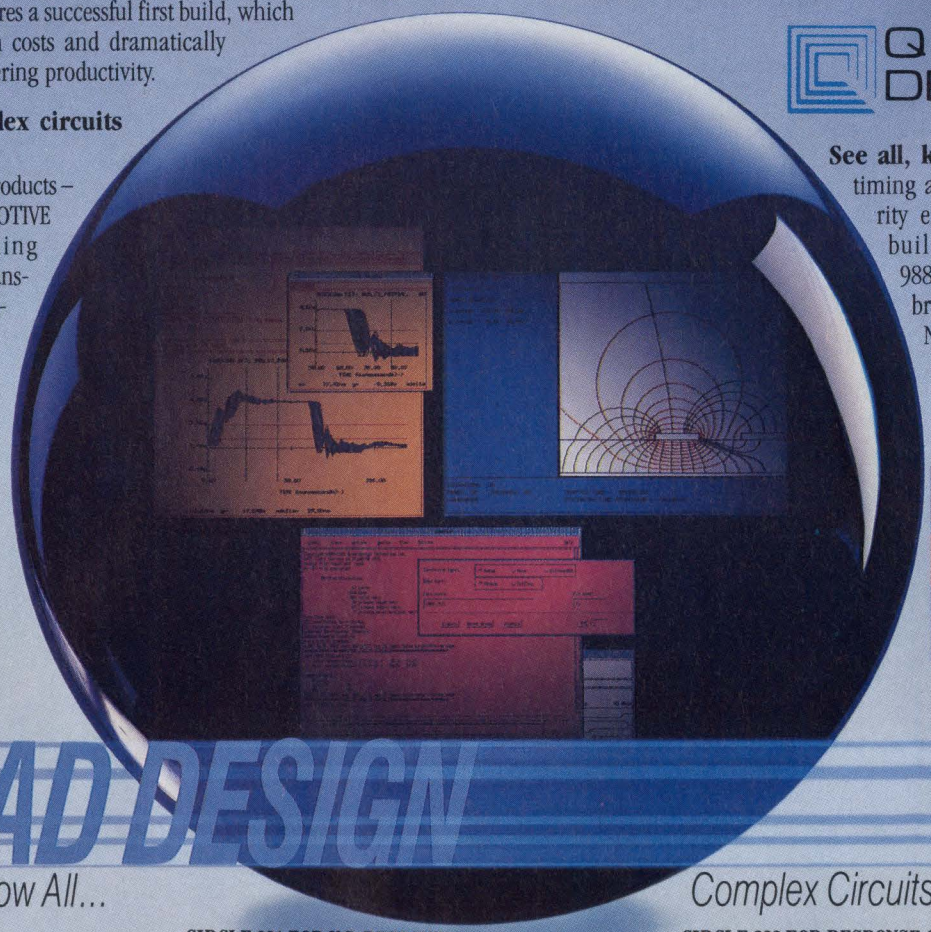

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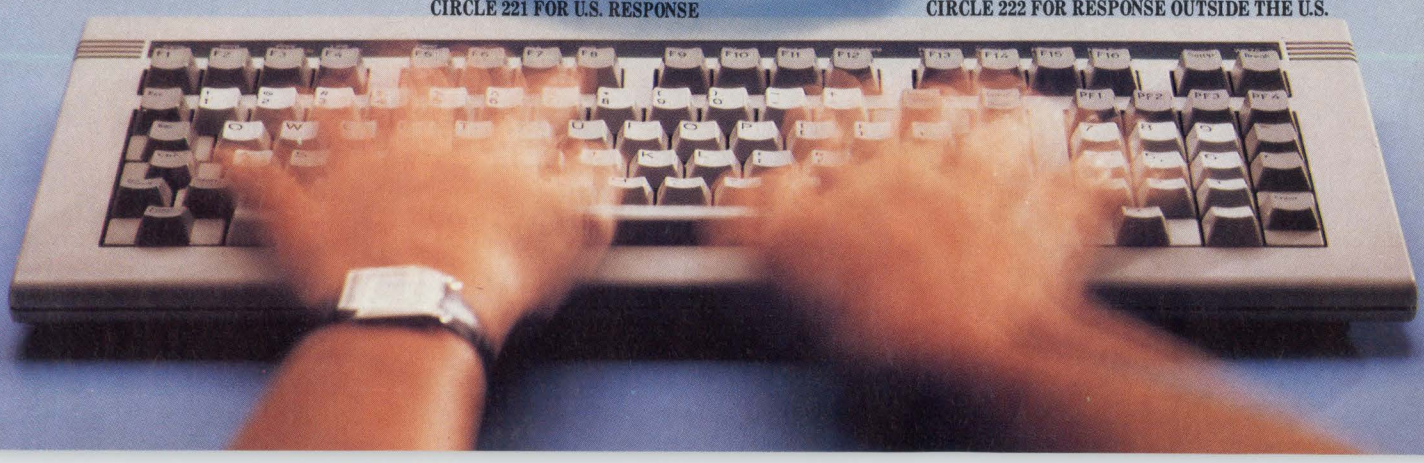
CIRCLE 221 FOR U.S. RESPONSE

CIRCLE 222 FOR RESPONSE OUTSIDE THE U.S.



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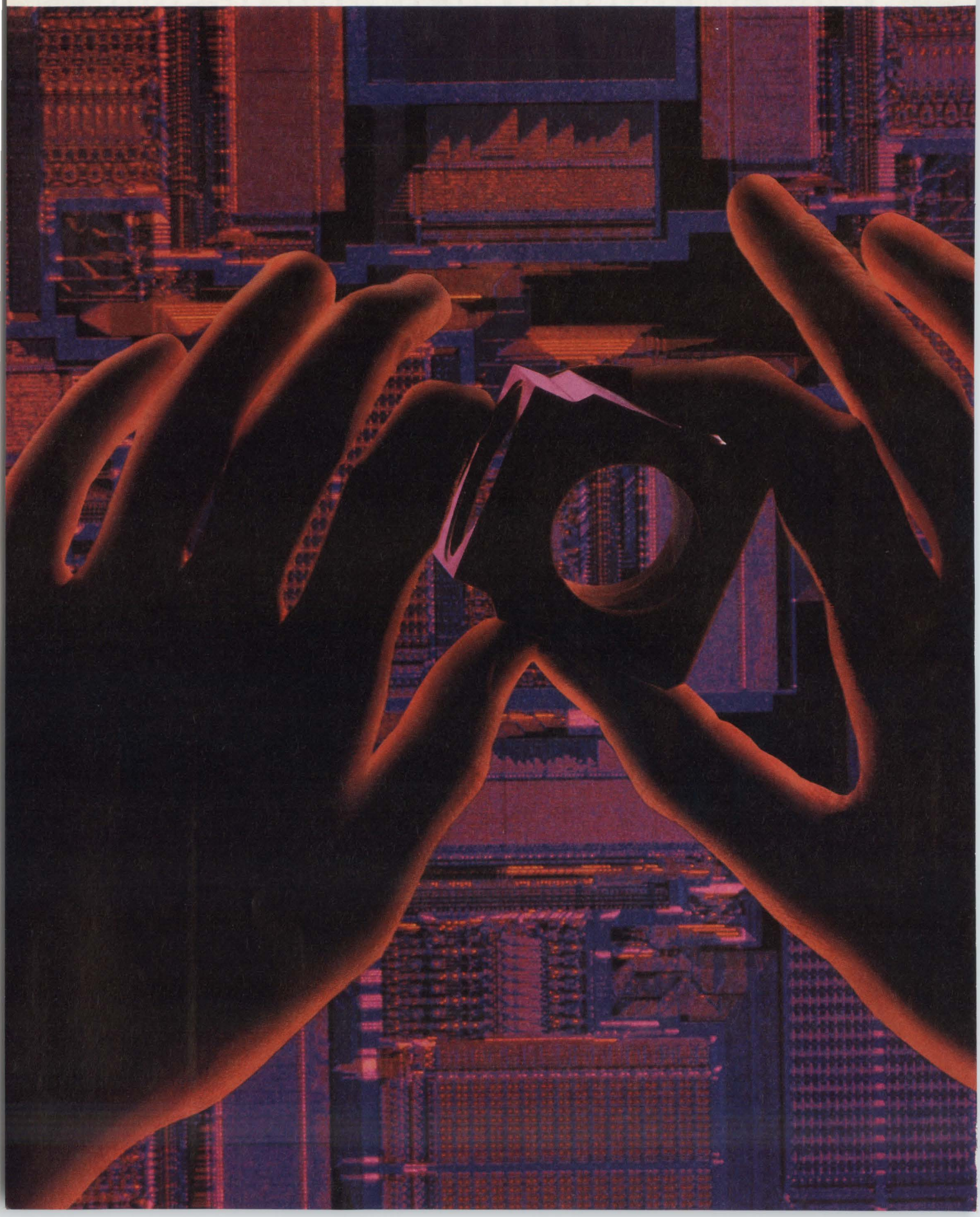
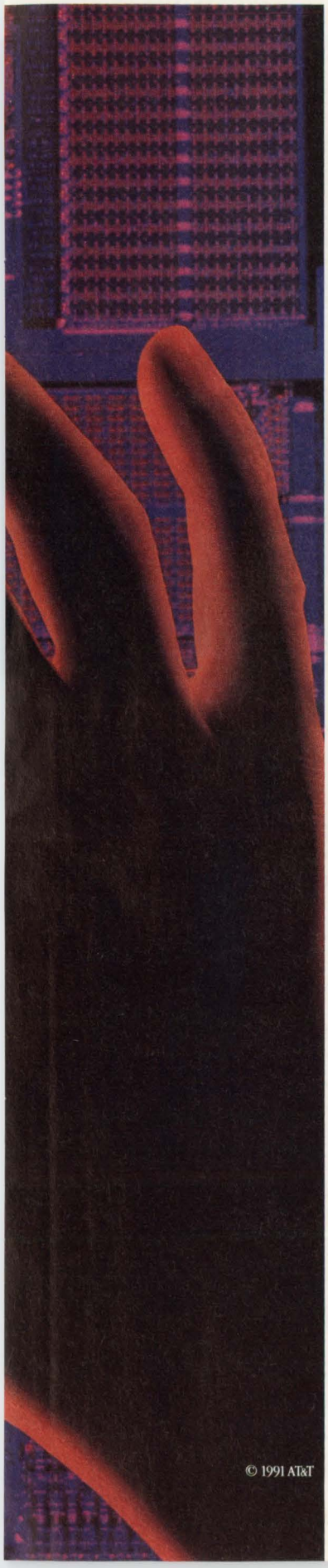


the portable market.



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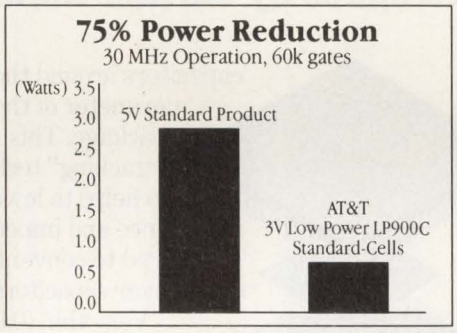

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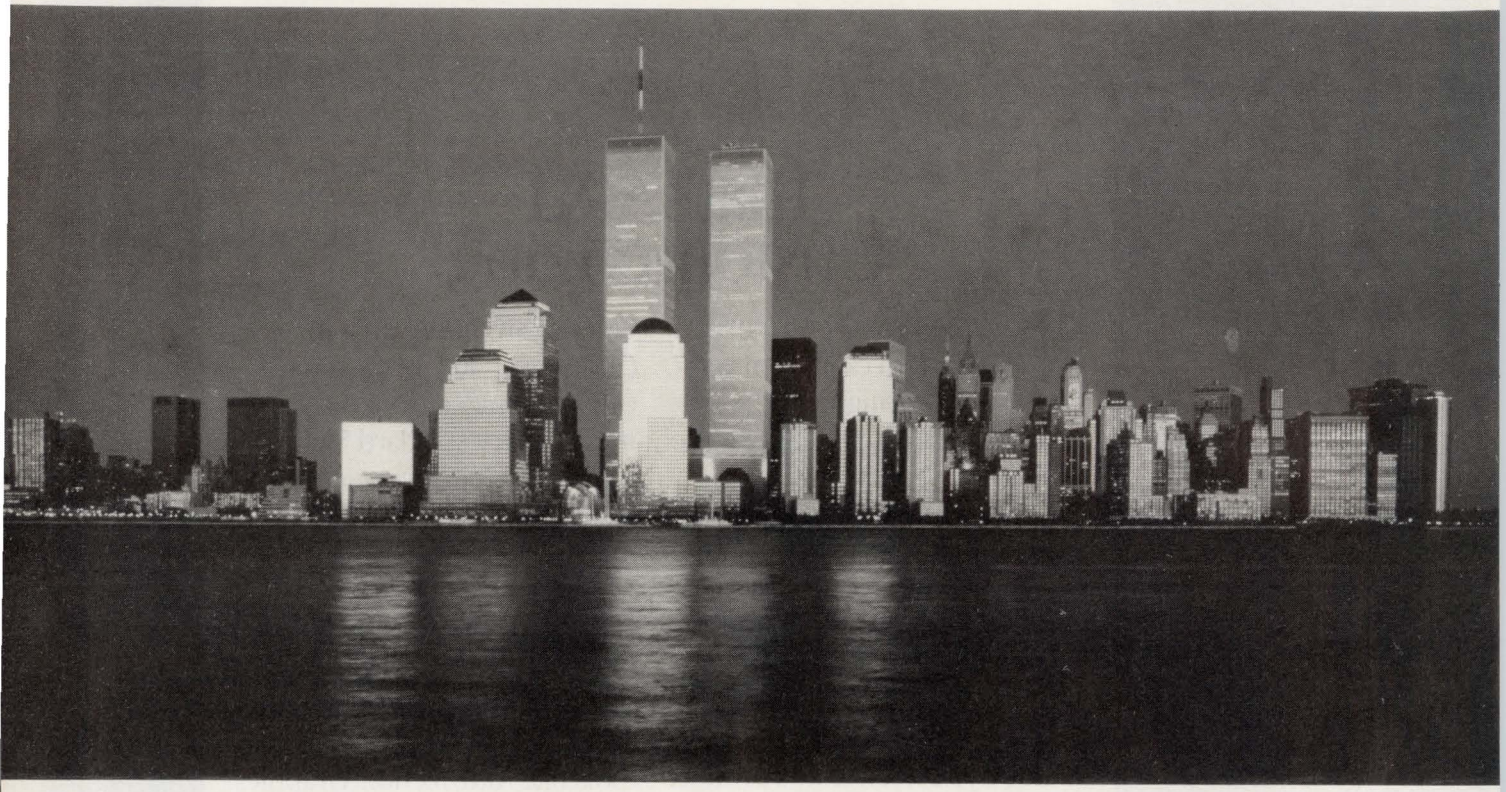
CIRCLE 210 FOR U.S. RESPONSE

CIRCLE 211 FOR RESPONSE OUTSIDE THE U.S.

When space is at a premium, stacking makes a lot of sense.



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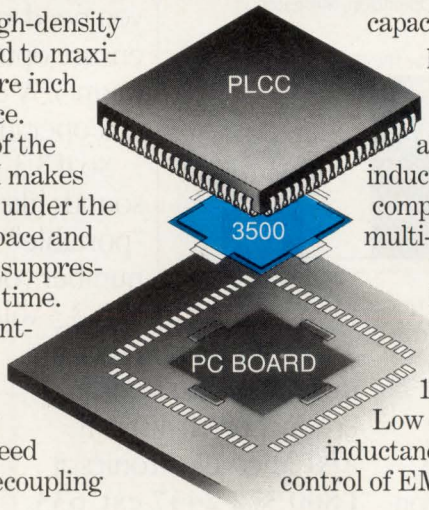
In today's high-density designs, you need to maximize every square inch of PC board space. The low profile of the Micro/Q 3500SM makes it easy to mount under the PLCC, saving space and improving noise suppression at the same time.

Surface mounting under the PLCC increases board density by eliminating the need for traditional decoupling capacitors around the perimeter of the IC package. This "stacking" technique also helps to lower inductance and impedance compared to conventional multi-layer capacitors.



Very thin (0.020" MAX) metallic-parallel plate construction results in less than 1nH of inductance. Low decoupling loop inductance value improves control of EMI/RFI. Besides providing superior noise reduction, the Micro/Q 3500SM also absorbs CTE mismatch and prevents electrical failure caused by cracks typical of MLC chips.

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CIRCLE 176 FOR U.S. RESPONSE

CIRCLE 177 FOR RESPONSE OUTSIDE THE U.S.

EXPERIENCE REVEALS VHDL'S QUESTIONS AND ANSWERS

The EDA industry has been debating the pros and cons of the VHDL hardware-description language (HDL) for years. It's an IEEE standard with a wide range of descriptive capabilities. But it's also a verbose language that runs slow in simulation. As it matures, questions continue to surface about its practicality. The good news, however, is that experience reveals viable solutions to most any VHDL question that engineers can think of.

The following articles, written by eight VHDL experts, explore some issues associated with VHDL. For example, the first piece, written by Robert Mendes Da Costa of Mentor Graphics, elaborates on the problems that crop up when graphically-oriented engineers encounter language-based design. Also, the conversion of an EDA design system to VHDL may appear to be a daunting task. It doesn't have to be, according to Valid Logic's Vahan Kassardjian. The trick is to ease into the transition gradually.

The fact that VHDL is an IEEE standard is appealing to many engineers for an array of reasons. But can one standard fill the needs of so many? The answer is no. Moe Shahdad, chairman of the IEEE committee in charge of revising the standard, explores the revision process and describes some changes that will be made .

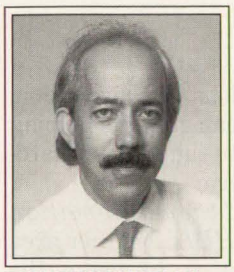
To be a practical design alternative, VHDL must be supported by many of the ASIC libraries. That has not happened yet. Prabhu Goel of Cadence explains how that doesn't have to be a problem. He asserts that engineers can use the wealth of existing Verilog libraries to exploit VHDL for ASIC design today.

Slow gate-level simulation can be another VHDL shortcoming, as explained by John Willey of Vantage Analysis Systems. But Willey goes on to say that existing hardware accelerators can solve the speed problem.

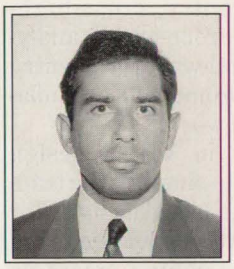
Adding VHDL to synthesis technology results in top-down design, often touted as the direction in which most design teams are headed. It's a big change, though—how can engineers know when they're ready for it? The answer given by Steve Carlson of Synopsys, who has penned several books on the subject, is that every engineer can handle the change if it's made gradually.

The timing flexibility inherent in VHDL models is both a benefit and a drawback. Teradyne's Mark Milligan, drawing from his experience in working with VHDL customers, explains why timing problems may exist and how development of standard model-writing techniques can help overcome them.

Finally, Steve Goldman of Protocol discusses the potential problems in using VHDL as a system-validation tool. Model portability and software performance, for example, are factors that engineers should consider when planning to verify an entire system using the VHDL language.



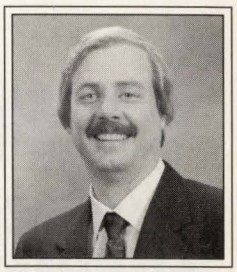
ROBERT MENDES DA COSTA is a marketing manager at Mentor Graphics. He holds a BSEE and BSCS from the University of Calif., Berkeley.



VAHAN KASSARDJIAN is the VHDL product marketing manager at Valid Logic Systems. He has an MSEE from the University of Southern Calif., Los Angeles.

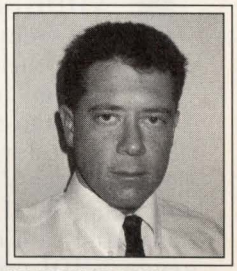
MOE SHAHDAD, strategic program manager at Viewlogic Systems, is the chairman of the IEEE committee managing the 1992 VHDL standardization effort.

PRABHU GOEL is the president of Cadence Design Systems' CAE Div. He has an MS and a PhD in electrical engineering from Carnegie-Mellon University, Pittsburgh, Pa.



JOHN T. WILLEY, vice president of marketing for Vantage Analysis Systems, holds a BSEE and MBA from Auburn University, Ala.

STEVE CARLSON, methodology consulting manager for Synopsys, has BSCS, BSEE, and MSEE degrees from the University of Colorado, Boulder.



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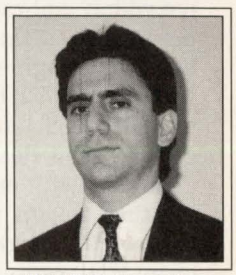

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TEACHING ENGINEERS A NEW DESIGN PARADIGM

VHDL'S BIGGEST STUMBLING BLOCK IS EDUCATION ABOUT LANGUAGE-BASED DESIGN

Top-down design based on VHDL can become a strategic weapon as companies shift their focus from shortening individual design tasks to compressing the entire product-development process. Engineers use VHDL to create and verify high-level design representations. And as a documentation language, VHDL provides a non-ambiguous, executable and portable description of the design. Finally, VHDL is widely embraced by EDA suppliers.

Despite VHDL's great potential, however, the design community has not widely embraced this new design practice; less than 5 percent of all hardware engineers today use any HDL at all. VHDL's power can go unrealized if engineers view language-based design methodologies as too difficult or incompatible with existing design practices. To most engineers, design techniques based on an HDL represent a major education hurdle. Specifically, the primary obstacle for engineers is learning a new design paradigm—a significant shift from how they currently design. To understand why, look at how engineers work today.

The universal design language being used today is graphics. Due to education or preference, engineers think, organize their thoughts, innovate, and implement using graphics-based methods. Ask any engineer to describe his or her system, and he or she will invariably draw state diagrams, schematics, or block diagrams—not code.

Although VHDL is an excellent HDL that offers a host of hardware-oriented constructs, such as time, components, signals, and ports, engineers still view its use as a foreign, program-oriented design practice. This issue is not just problematic to VHDL, but to HDLs in general. In fact, engineers who have learned to use languages still tend to mentally translate their graphical thought processes to text, a process that presents both technical and practical inefficiencies.

To complicate matters further, today's synthesis tools constrain and complicate HDL use. For example, not all VHDL constructs can be synthesized with today's synthesis tools, and each synthesis tool requires a unique design approach to get optimum results. Therefore, engineers must learn how to write not only functional VHDL code, but also code that can be synthesized.

These educational barriers can deter any engineer from adopting VHDL, or any HDL for that matter. Fortunately, these barriers can be overcome if VHDL can be made to blend with, versus contend with, current design practices. Practically speaking, there are three ways to advance the education and use of VHDL.

Change how it's taught. Courses and text books that approach VHDL like a software programming language only serve to alienate and confuse graphics-oriented hardware engineers, who don't view themselves as programmers. Engineers need applications-oriented courses and text books that teach how to describe common hardware functions and how to approach real-world design problems using VHDL. They should include real-life examples, and ideally should have electronic formats of VHDL descriptions for execution. These examples can go far in helping engineers learn to think about hardware in VHDL terms.

Improve how design-automation tools support VHDL. Another area for improvement is to make the VHDL EDA environment more appealing to hardware engineers. For example, the user-interface paradigm can become more consistent with what engineers already know. VHDL support that includes interactive schematic entry, cross-highlighting, "point-probe-click" analysis, and graphical-waveform entry and display will promote its assimilation in the design world.

Improvements in VHDL design entry can also help simplify the transition to language-based design. For example, context-sensitive editors can help uncover syntax errors as soon as they're entered, and libraries of VHDL templates and model generators can automatically produce error-free code ready for synthesis and simulation.

Change the perception of VHDL's role. Finally, the industry can remove the perception that engineers have to jump to VHDL all at once. This impression is especially unsettling to non-English users, who must not only learn a new design methodology, but English as well. VHDL doesn't have to be an all-or-nothing proposition. One step toward changing this perception is creating design environments that accept both high-level graphics and VHDL text as inputs.

To lower the potential friction generated by this new technology and to accelerate its acceptance in the design community, three things are needed: application-oriented education, an EDA environment that takes responsibility for much of the learning curve, and realistic expectations about its use, understanding that VHDL is just one way to pursue top-down design. The EDA community, in fact, is already responding to address these concerns.□

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DESIGN TOOLS CAN EASE THE TRANSITION TO A VHDL ENVIRONMENT

INTERACTIVE, GRAPHICAL ENTRY METHODS HELP SMOOTH THE PATH FROM GATES TO VHDL

Early adopters of industry-standard full VHDL have been harvesting the benefits of this powerful, high-level, system-design and description language for more than five years. Broad market acceptance has been slow, however, because VHDL comes along with a steep learning curve. The vast majority of today's engineers cannot afford to risk delays in product development in favor of learning an entirely new design methodology. Further, hardware engineers accustomed to gate-level, graphical representations of their designs are reluctant to make the transition to language-based design. In essence, they object to being "forced" to become software programmers. To encourage broader acceptance of VHDL and deliver its benefits to the average engineer, EDA-software companies must provide users with a gradual path to the use of languages and must simplify the programming task.

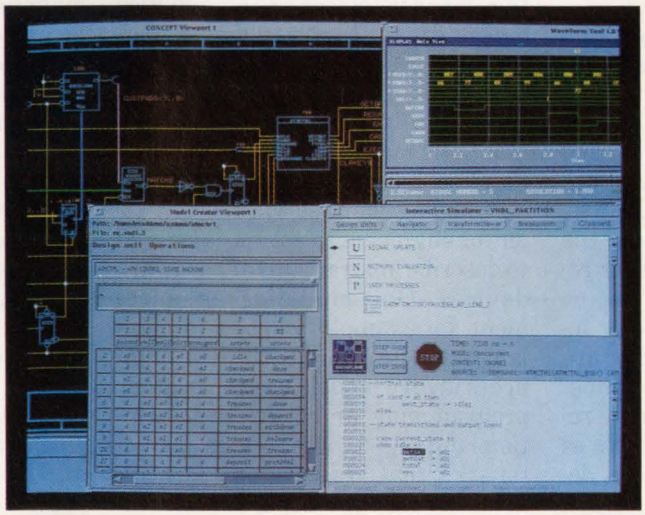
For engineers to make a smooth transition to VHDL, design-entry tools must support multiple (or compound) capture methods in a block-oriented approach, in which each design representation is embodied in blocks that are graphically connected to form a design. This block-oriented capability should not be limited to VHDL. Instead, it should allow the engineer to specify a design at any level in the design hierarchy, whether behavioral, RTL, or structural, using a variety of design-entry methods including block diagrams, schematics, truth tables, state machines, or VHDL. The availability of a module creator for truth tables or state machines is particularly important for the novice VHDL engineer. With this type of tool, an engineer can simply specify his or her inputs in a familiar graphical or table format, and the module creator automatically optimizes the logic network and generates VHDL source code. This process can save a tremendous amount of design time for experienced VHDL engineers as well.

While a compound approach can ease the transition to VHDL, sooner or later engineers must still become proficient in using the VHDL language. For this reason, today's VHDL environment needs to offer capabilities that help users learn to write proper VHDL formats and grammar. Especially useful are built-in templates that prompt the user with various legal options for certain code segments, and an on-line language analyzer that notifies the user of errors as it reviews syntax and semantics. Because engineers are flagged immediately if a correction needs to be made, they can fix the designs at the start and avoid costly and frustrating errors caused by wayward VHDL design descriptions.

Another programming feature needed to help users make the transition to VHDL is a check that analyzes the VHDL description and tells the user whether it conforms to a synthesizable subset. This accelerates the top-down design process and provides hardware-oriented engineers with a safety net, ensuring them that the semantics and design style are synthesizable.

The beginning VHDL user also needs a way to simplify the verification of his VHDL code. An interactive, source-level debugging capability shuld be available that combines all the power of CASE-like tools along with features found in hardware-debugging tools *(see the photo)*. These tools should not only let the engineer perform line-by-line debugging, but also let him or her monitor and trace signals with just a click of a cursor to the VHDL source. These tools would allow users to immediately understand errors in the design, whether caused by misuse of the language or by flaws in design and functionality.

VHDL's steep learning curve will only be overcome through the adoption of flexible intuitive design tools that help ease the engineer's transition from low-level physical implementations into high levels of abstractions. Tools that meet these requirements are now becoming available from some broad-line EDA suppliers. They are allowing engineers to expend their efforts on designing oand not on learning the nuances of VHDL, without compromising the power of the language.□



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EVOLVING VHDL INTO A MORE USEFUL STANDARD

MODELING, SIMULATION, AND SYNTHESIS CHANGES WILL ADORN THE 1992 REVISED IEEE STANDARD

Although hardware-description languages have many benefits, only VHDL enjoys the advantage of being an IEEE standard. However, because it's hard for one standard to fill all engineers' needs, the standard must periodically be revised. The newest version of the IEEE 1076 VHDL standard is due to be finalized in 1992. Better knowledge of the evolution process will help engineers understand where the VHDL standard came from and where it's going.

IEEE's VHDL Analysis and Standardization Group (VASG) is heading an international effort to re-standardize the current version of VHDL (VHDL 87), and arrive at a revised standard by December 1992. Both the European and Asian-Pacific VASG chapters have joined the the North American chapter in their re-standardization efforts.

The standardization process includes five major activities that are carried out almost in sequence. These are: definition of language requirements, definition of objectives for the design of the language, design of the language, documentation of the language definition, and validation of the language design.

The first two of the above five activities are already completed, and the third, language design, is scheduled to be completed by this February. The first step resulted in a document containing about 280 requirements in the areas of modeling, simulation, synthesis, and analog design.

Due to the high volume of requirements, the working group has established specific objectives for the design of the language. These objectives fall into four categories: design requirements, design goals, study topics, and discontinued objectives. Design requirements are those objectives that have the highest priority, and must therefore be met with VHDL 92 revision. Study topics are those requirements that are not clear enough to express in terms of specific design objectives or design goals. Most of the study topics for VHDL 92 address analog requirements. A separate VASG working group was established to address these requirements and propose extensions to the VHDL language to support analog design.

Upcoming changes to VHDL are mainly driven by design requirements. From a user viewpoint, implementation of these requirements will improve the language in the areas of modeling, simulation, and synthesis. These requirements are implemented either by generalizing the existing capabilities of the language or by enhancing the language through introduction of new features.In addition, inconsistencies and ambiguities detected in the current language definition, VHDL 87, are also being resolved. Finally, the language documentation is targeted for improvement, to make it more usable for both tool builders and users.

Modeling changes will make it easier for engineers to use the language to describe abstractions of hardware devices. One modeling enhancement, for example, will be a foreign-language interface that lets engineers invoke models written in other programming or hardware-description languages. Also, device characteristics that are currently identifiable only through using default features of the language will be explicitly identifiable in the future.

Changes in the simulation area will increase the timing and functional accuracy of VHDL models. They also will make it possible, or easier, for the engineer to guide the operation of the synthesis tools. One example is letting engineers express relationships among entities in a model. This will increase the documentation power of the language, allowing a particular circuit realization to be shared among a set of entities. Also, engineers will be able to label sequential statements in a model. That label can then be appropriately attributed to guide synthesis software.

VHDL 92 documentation will include a VHDL 92 annotated Language Reference Manual (LRM), highlighting all the deletions from, and additions to, the VHDL 87 LRM. It will also have a summary of changes to the language, an index, and an appendix that identifies those language constructs which may be non-portable.

Upward compatibility, which ensures that all VHDL 87 models will produce the same result when executed by VHDL 1992 tools, arises as an important issue in changing VHDL. Not only does this requirement constrain the design of language changes, but in cases of inconsistencies or ambiguities in VHDL 1987, upward compatibility may not be achievable. Upward compatibility, then, will be examined individually for each change that's made to the langauge, and not as an across-the-board requirement.

Various types of validation will ensure that the new language design conforms to the specified requirements. The first is benchmarks that consist of design examples encoded in VHDL 1992. Second, prototype design tools could unveil potential inconsistencies or ambiguities in the language definition. Finally, development of formal semantics could also unveil problems.□

Moe Shahdad, Viewlogic Systems Inc., 293 Boston Post Rd. West, Marlboro, MA 01752-4615; (508) 480-0881.

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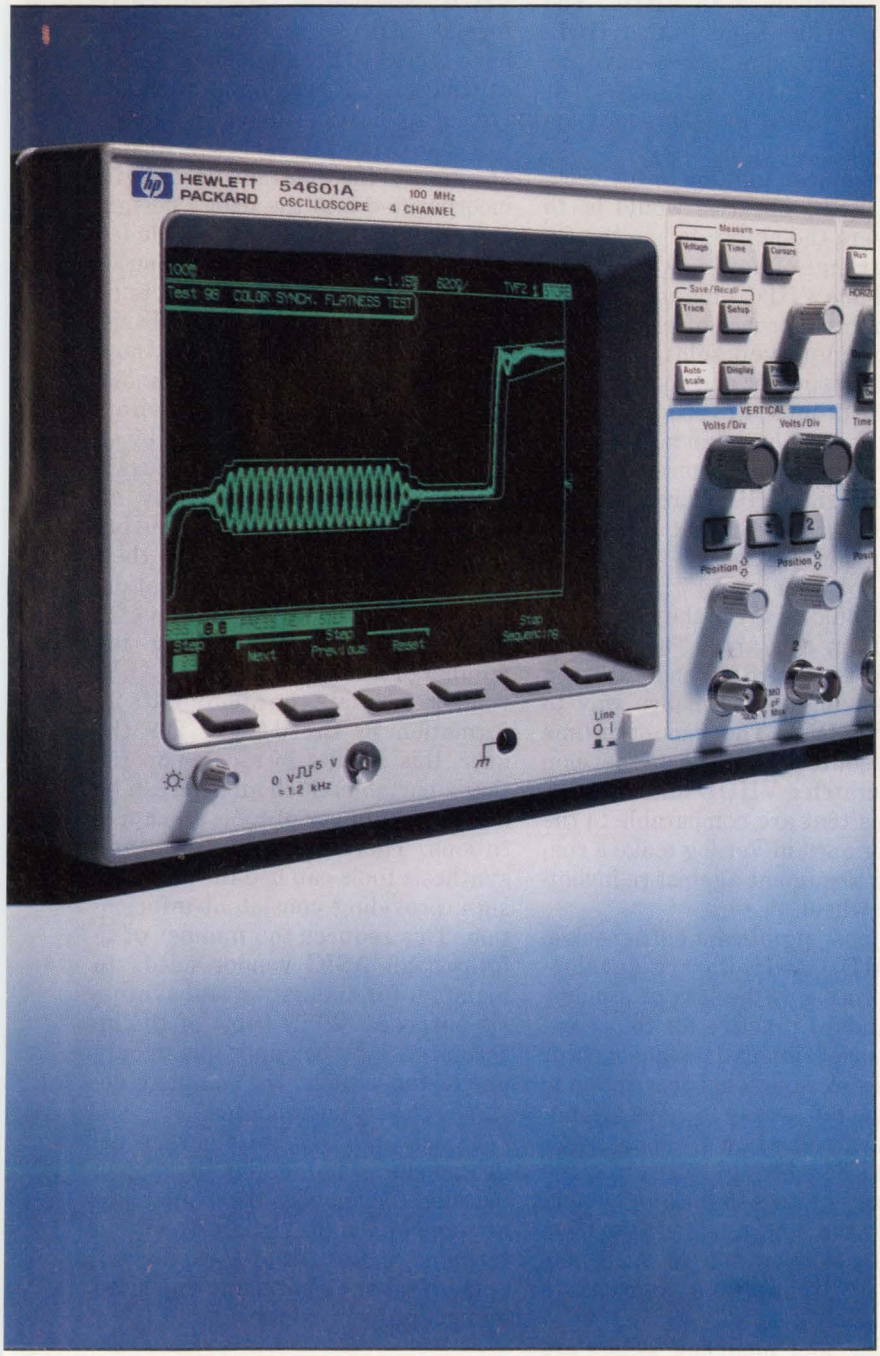

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CIRCLE 137

LIMITED VHDL LIBRARY SUPPORT CAN HINDER ASIC DESIGN

USERS CAN DESIGN ASICS WITH VHDL TODAY BY CAPITALIZING ON EXISTING LIBRARIES

Hardware-description languages broke new ground in the 1980s by offering hardware engineers an efficient, flexible, and powerful approach to describing electronic products they sought to develop. Once early-adopter engineers became accustomed to the ability to work at the higher levels of abstraction that HDLs offered, the days of all-gate-level design became numbered.

Today, VHDL is on the brink of industry acceptance as an HDL of choice. Unfortunately, it doesn't yet come with many production-worthy tools. The most common complaint from users is that ASIC design with VHDL today is impractical, if not impossible. Such is the dilemma commonly associated with standards because they tend to move slowly and adapt gradually to the needs of the real world. However, users are demanding working solutions today and cannot afford to wait for standards committees and vendors to come to terms with critical issues like timing and modeling standards.

The most conspicuous void in practical VHDL use is library support. Without library support from leading ASIC vendors, VHDL will continue to fall short of its potential. ASIC vendors will be slow to develop VHDL libraries without a major push from users. Therefore, there needs to be a mechanism to leverage the production-proven, HDL-based technology developed by companies like Cadence and Synopsys in the 1980s and apply it to VHDL. The years of effort behind other HDL-based design approaches have resulted in valuable advances that could be applied in a standard approach to this methodology.

The simplest solution to the problem of ASIC libraries would be to give users the ability to use the extensive range of Verilog ASIC libraries within a VHDL environment. Although this approach offers a viable, production-proven solution today, it's vendor specific and doesn't deliver on the promise of vendor independence inherent in a standard.

However, if the requirements for ASIC design in VHDL are examined carefully, it's clear that through a more general adoption of proven methodologies and processes, VHDL could be given the jump start it needs in this area. The primary problem is that ASIC vendors need a low-cost, high-performance way to support VHDL. The amount of time and resources needed to develop from scratch a VHDL suite of ASIC libraries that are comparable to the existing ones in Verilog make a convincing argument against re-inventing the wheel.

The most significant bottleneck in the VHDL ASIC-library development process is the lack of a industry-standard practice for the representation of timing data in models or libraries. A functional description in VHDL is fairly easy to generate, but the characterization of timing information is less straightforward given some weaknesses in the language itself (for example, pin-to-pin timing, a critical consideration in ASIC design, is difficult to express in VHDL).

Timing and modeling issues are high priorities for the IEEE, and some progress has been made already. A draft for a standard, multi-valued logic (MVL) package is currently in review. In fact, it's included in the latest releases of many vendors VHDL tools. Essentially, a standard MVL package offers a common nomenclature and semantic for logic types, facilitating the correct application of delay values, and thus, more accurate simulation.

What still needs to be addressed in VHDL, however, is a standard delay format (SDF) so that all tools may have access to the same data. Delay calculation and back-annotation are typical applications in which data (in this case delay values) is specified in an external file that then needs to be incorporated into the user's design. Generally, delay values are included as part of a component's generics list, thus allowing these values to be set on an instance-by-instance basis. This, however, is not currently supported in VHDL. Existing technology in Verilog HDL-based environments could solve the problem by allowing a common file of accurate timing data to be shared by all VHDL simulators and by allowing engineers to continue to use their proven methods of delay calculation.

An SDF has proven to be an efficient process for simplifying the number of utilities needed by a ASIC vendor to update the appropriate information in the design. For the user, this results in a common file that's portable. Such an SDF can be used by a number of tools and applications. Therefore, simulation and synthesis tools can use the same design, providing consistent information. This reduces the number of libraries an ASIC vendor needs to maintain for simulation and synthesis purposes. While some of the information may be applicable to only one of those tools, the complete design is clearly documented.

Clearly, VHDL ASIC library development is not going to happen overnight, even with the availability of some of the previously-discussed technology. Results of library development must be carefully validated against proven, existing data.□

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GATE-LEVEL SIMULATION IN VHDL DOES NOT HAVE TO BE SLOW

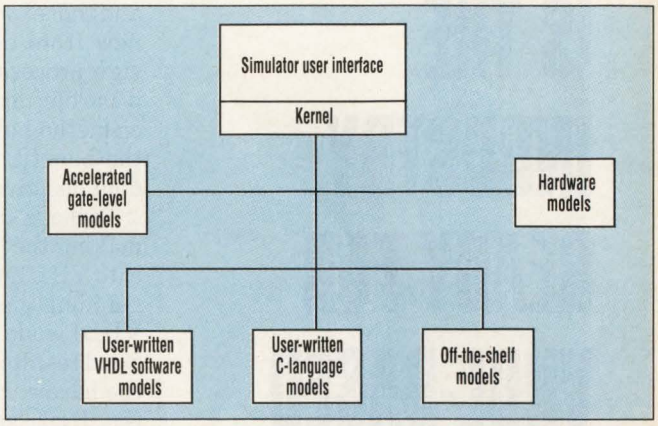
LINKS TO HARDWARE ACCELERATORS CAN BRING GATE-LEVEL VHDL SIMULATION UP TO SPEED

Even though VHDL is a very capable simulation language providing advantages ranging from power to flexibility, it's no secret that it's not the fastest gate-level simulation language. That's because VHDL's complexity includes features that can work against performance. Several solutions can overcome the inherent problems of added complexity. Hardware-assisted simulation is the most promising of these.

All simulators need a base element on which to build a circuit. Logic simulators have a relatively fixed set of low-level primitives from which complex circuits are constructed. The advantage to this approach is that the primitives can be highly tuned for both speed and memory utilization.

VHDL is a behavioral modeling language, so it does not include lower-level primitives, and consequently resolves the lack of flexibility inherent in earlier generations of simulators. The trade-off is that it's difficult to optimize at the gate level.

VHDL has other features that increase user flexibility but tend to reduce gate-level simulation speed. One of these is the lack of a predefined, hardcoded logic-state system. State systems, along with the rules for exception reporting, are traditionally built into all simulators. Much like built-in primitives, they're highly optimized. VHDL simulators are the exception. In VHDL, state systems are defined by users at will. The net effect is that VHDL users have the freedom to define a state system of virtually any size they want. This level of flexibility brings with it clear advantages, but also can impede performance.



Also, unlike other simulators, VHDL is not limited to bit-type (1 and 0) signals. Signals may be bits, characters, arrays, records, and several other things. How, then, does the simulator handle a case in which two signals drive a single node, one with the value Red and the other Green? It doesn't, at least not directly. Rather, the simulator calls a separate user-written (and very likely non-optimized) function each time it needs to check contention resolution.

There are a few obvious solutions to this speed problem. Simulation vendors can write better code. Or, users can run the simulator on faster hardware. A less obvious solution is to embed an optimized gate-level simulator into a full VHDL simulator. This might work, and although flexibility would be curtailed when using this engine, the performance boost might overcome it.

Hardware accelerators, in conjunction with software simulators, may provide the horsepower necessary to provide both flexibility and performance. Specifically, what's required is a coprocessor that will allow a mixture of accelerated and non-accelerated components to be simulated simultaneously. And further, the use of this engine must be transparent to the user.

Such a device broadens the definition of a simulator to include a control kernel linked with a variety of models. The ideal simulator would draw on a wide range of modeling techniques *(see the figure)*. In the context of acceleration, the software-hardware connection needs the following features:

1. The ability to parse the input VHDL, locating and processing the "acceleratable" portion without user intervention. This parsing should begin at the bottom of the design hierarchy and proceed upward until constructs are reached that are not based on the simulator's built-in primitive set. That way, purely structural VHDL would all be downloaded, while mixed structure-behavior would not.

2. The VHDL compiler should be modified to point some architectures at the accelerator rather than to require VHDL code for each. This requirement solves the security, size, and prep-time concerns library vendors might have.

3. The connection to the simulator-accelerator must be completely controllable by a single user interface.

4. Full, mixed simulation must be transparent to the user.

5. The control and communications overhead must be written so that mixed behavioral and structural circuits execute at least as fast as they do in pure software.□

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IS THE INDUSTRY READY FOR VHDL-BASED SYNTHESIS?

JUMPING FROM GATE-LEVEL DESIGN TO VHDL-BASED SYNTHESIS ISN'T HARD IF IT'S DONE GRADUALLY

VHDL-based design with synthesis has begun to hit the mainstream. Many projects using VHDL design methods have been in full production for well over a year. But for those who have not yet made the switch to synthesis-based VHDL design techniques, the question "Am I ready?" has been difficult to answer.

It's a difficult question because there are obstacles to adopting the technology and adapting to the new methodology necessary for HDL-based design. There's an industry perception, moreover, that the adoption of HDL-based design with synthesis requires scrapping the existing design environment and design methods. Some would have you believe that it takes months and months of training before any of the new techniques can be successfully applied. This is not true. A gradual movement toward VHDL-based synthesis will not disrupt existing design methodologies, yet will reap swift rewards.

Properly viewed, HDL-based design tools for optimization are an adjunct to traditional gate-level design, and those tools for VHDL entry are a new front end to the traditional design process. Synthesis brings with it the optimization of net lists, a faster method of creating a net list, and the benefits of technology-independent design descriptions.

Perhaps the most difficult part of making the transition from gate-level to VHDL-based design is in understanding the correlation between the VHDL code written and the synthesized results. Engineers must realize the hardware consequences of all of the HDL source code written because coding style is the most powerful way to control the final design implementation. In addition, engineers must also cope with the fact that, for synthesis, writing legal VHDL is not enough—the VHDL must be from the set of constructs supportable by synthesis technology. Once the initial hurdle of understanding VHDL design capture is overcome, the rest of the HDL methodology is so similar to old design methods that it is a very natural process.

Although not universally observed, the adaptation to the next generation of digital-design techniques follows a fairly consistent pattern. The steps below allow a gradual transition:

1. *Traditional schematic engineer (no synthesis)* : Schematic entry for design capture on a computer-aided-engineering system, gate-level simulation for design validation and verification.

2. *Traditional design and optimization* : Same as traditional design, but after the initial design is captured (via schematic entry) and validated, the net list is fed through a synthesis program for logic optimization. The result is a net-list schematic that can be accepted or rejected, constituting essentially a no-risk use of synthesis.

3. *Traditional design and optimization and test synthesis* : As an optional piece of synthesis technology, test synthesis can automatically insert test structures into a design and generate manufacturing test vectors. This step can be tried very quickly, and if the engineer isn't satisfied with the result, he or she needn't use it.

4. *Traditional design and partial VHDL entry and synthesis* : The engineer captures that part of the design that seems natural to describe in VHDL. One of the most common blocks, for example, is a state machine. This VHDL description can then be synthesized quickly. The resulting net list is transferred into the existing computer-aided-engineering environment for integration with the rest of the design, which is being captured with traditional schematic entry.

5. *Full VHDL-based design with synthesis* : Over time, the engineer gains confidence in the synthesis tools as understanding of the new methodology grows. More and more of the design is captured in VHDL and synthesized automatically down into gates until, finally, entire designs are entered via the hardware description language.

Given this very low-risk of technology adoption and methodology change, it's possible, practical, and competitively prudent to begin using VHDL-based synthesis now. The technology and tools have matured, and industry acceptance is accelerating. VHDL-based design is obviously here, and will dominate the CAE world within a year's time.□

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Steve Carlson, Synopsys Inc., 700C E. Middlefield Rd., Mountain View, CA 94043; (415) 962-5000.

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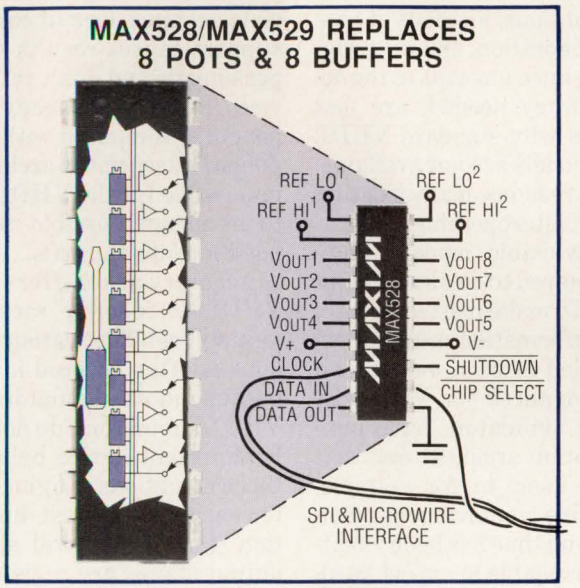

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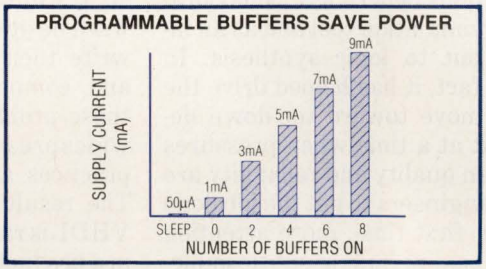

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CIRCLE 148 FOR U.S. RESPONSE

CIRCLE 149 FOR RESPONSE OUTSIDE THE U.S.

DYNAMIC TIMING CAN CAUSE SNAGS IN VHDL MODELS

GUIDELINES WOULD HELP USERS WRITE ACCURATE, MORE STANDARDIZED VHDL MODELS FOR VERIFICATION

VHDL has shown tremendous benefit as a behavioral simulation tool and as an input to logic synthesis. In fact, it has helped drive the move toward top-down design. But at a time when pressures for design quality and reliability are forcing engineers to get the job done right the first time, more attention must be paid to finding subtle implementation problems through simulation. Accurate timing analysis and the ability to realistically model circuit behavior over component and operating variations are required to find implementation errors. VHDL has many of the capabilities needed to perform the necessary timing verification. However, a concerted effort is needed to overcome standardization problems and the few remaining technical hurdles, and successfully use VHDL as a production-quality dynamic timing simulator.

VHDL has tremendous flexibility for handling timing in models. For example, PTV derating factors, separate rise and fall times based on intrinsic delays, wire capacitance and output loadings, and state-dependent delays all may be included in a model. Because there's no direct way to attach delay to a signal, wire delays are placed on the pins. The timing information may be placed in the architecture defining the component functionality, or placed in a separate file. Back-annotation is possible, but cumbersome.

That same model flexibility, however, is also a problem. Name and format conventions, methods of handling back-annotation, and most significantly, disagreement as to the degree of accuracy needed, are just some reasons why standard VHDL component models are not available. For the same reasons, many existing models aren't interoperable.

Without available models, engineers are required to do all modeling themselves. To make matters worse, the timing information must be explicitly handled in each model (and packager). Advanced non-VHDL dynamic-timing simulators have optimized simulation architectures that don't require users to, for example, explicitly define what happens when a model's set-up time has been violated. It's unreasonable to expect hardware-design teams using VHDL to write their own timing algorithms and component models. Many of these problems can be resolved by widespread adoption of standard practices and modeling guidelines. The result today, however, is that VHDL is rarely used to verify timing in a production environment.

For example, state-dependent, worst-case analysis is required to accurately find timing problems over the full range of component variations and operating ranges. Worst-case analysis is not simply min-max simulation, but the simultaneous accumulation of both minimum and maximum delay of each signal, at each node, as it propagates through the circuit during simulated operation. It takes into account the ambiguity regions caused by the variable delay a signal will encounter across a device under different conditions.

Note that timing ambiguity is different from an unknown event. In an unknown event, both the event nature and its timing are unknown. In timing ambiguity, only the timing is unknown. This is difficult, but possible, to model in VHDL. It requires special signal-state definitions to define the notion of timing rather than state unknowns. Separate code would be needed in each model to handle these conditions, but no current popular VHDL package has provisions for this idea.

Although it's possible to model worst-case timing in VHDL with special packages, lack of core simulator support causes results that are too pessimistic and don't reflect real devices. Because the behavior of a component is computed within that component's associated architecture, it's impossible for the VHDL simulation to ascertain possible relationships between input signals.

Accuracy also suffers when using VHDL to identify race conditions and spikes. This category of problems is often ignored in simulation, because most simulators (including VHDL simulators) do not realistically represent device behavior under these conditions. Engineers have often assumed the best during simulation (that spikes will settle before output stages are registered). However, this small category of problems can be important, particularly for designs subject to temperature or component variations.

Although simulation can be used to find these problems, VHDL is not well suited to this task. VHDL allows either an inertial or transport model to be used for a given signal assignment. The inertial model swallows the pulse, the transport passes the pulse through. Neither model is particularly accurate.

A better approach is to pass an ambiguity region through during the spike. Attempts to use this signal in an evaluation during this time would cause an error, and if no evaluation is made until the signal has settled, no error occurs. Again, the flexibility of VHDL allows ways of achieving this objective through creative code, but it is not directly supported as a signal-assignment mode. In addition, no standard exists to describe how to implement this function.□

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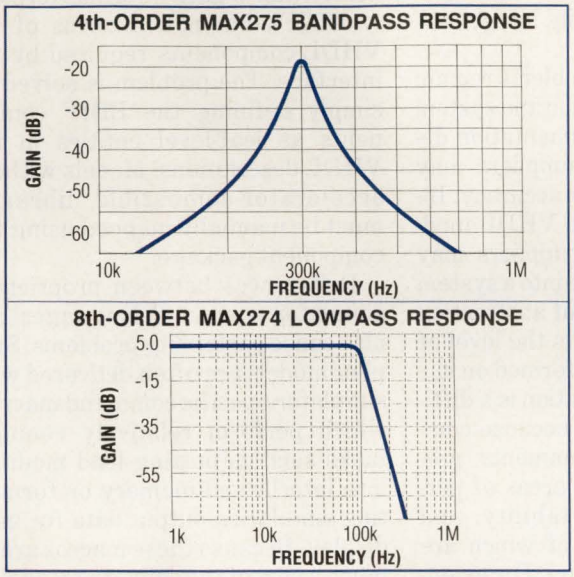

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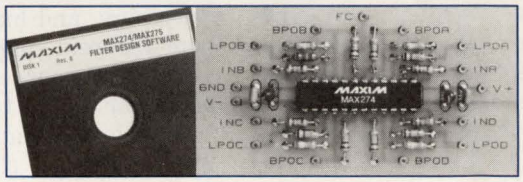

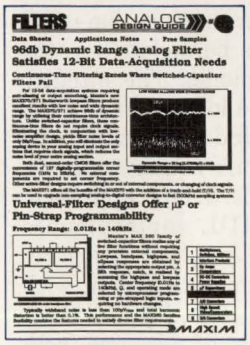

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CIRCLE 229 FOR U.S. RESPONSE

CIRCLE 230 FOR RESPONSE OUTSIDE THE U.S.

SYSTEM VALIDATION CAN BE TRICKY WITH VHDL

MODEL PORTABILITY AND SOFTWARE PERFORMANCE POSE PROBLEMS FOR VHDL SYSTEM SIMULATION

Both the military and commercial sectors are moving toward standardization in the development of complex electronic systems. The use and re-use of bus protocols, microprocessor architectures, software libraries, and even entire system components are becoming common practice. Along with the cost and time savings associated with standardization, however, comes the need for validation. Subsequently, HDLs such as VHDL are being evaluated for use as validation tools.

Since 1988, the U.S. Department of Defense (DOD) has required that all design documentation for digital systems be described in VHDL. This was a significant step in the right direction, because the way to standardize specification metrics and measurement procedures is to first call for a common design-documentation approach.

In the past several years, VHDL has grown in popularity within the commercial sector as well. As a result, most major EDA vendors support the language with a myriad of tools, including schematic browsers, editors, compilers, and simulators. This is good news for both DOD and commercial suppliers because these VHDL tools should simplify the system validation requirements of product warranties. Suppliers, with a wide selection of commercial EDA tools to choose from, will move away from their proprietary design environments. In this way, validated VHDL component architectures can be passed from supplier to integrator in a standard, easily integrated, electronic format.

In the meantime, problems remain for component validation and system integration. Test documentation delivered by different suppliers may have wide variations in accuracy. Independently-developed VHDL models from component suppliers may be difficult to integrate into a system model. Also, the level of abstraction of a VHDL model limits the level of testing that can be performed on it.

VHDL system validation is a difficult process primarily because commercial VHDL environments present limitations in the areas of performance, model portability, and software support, all of which are key to system simulation. For example, to perform validation testing for a typical system module, VHDL models of ASICs, commercial microprocessors, and bus-interface units from different suppliers must be integrated. The size of the integrated model can be up to 50,000 lines of code, representing 200,000 gates. Experience has shown that even smaller models, representing between 5000 and 15,000 gates, are often too large to be simulated in a reasonable time on a workstation.

Some tool vendors have taken a stab at this problem by developing simulator kernels that are optimized for a specific primitive subset. But this is often ineffective, because the system model is simply too big for memory, and a performance bottleneck is caused by excessive disk swapping on the host. Other vendors have chosen a hardware acceleration approach, which is effective for models described using structural libraries. Some VHDL environments even support mixed-level simulation, in which behavioral code runs on the workstation and structural portions are ported to the accelerator.

Once performance issues have been addressed, model portability is the next stumbling block. Because accelerator interfaces require models that can be described using an acceleratable component package, supplier design libraries have to be converted. In some cases, supplier libraries already exist in the accelerator's native format (typically EDIF), but not in terms of the VHDL components required by the interface. The problem is solved by simply defining the EDIF components as leaf-level entities in the VHDL descriptions. Models without accelerator-compatible libraries must be manually mapped using the component package.

Differences between proprietary simulator command languages can also cause portability problems. Supplier models are often delivered with simulator-specific command macros, which perform relatively complex tasks such as putting load modules into interleaved memory or formatting simulation output data for user display. Because these macros are as much a part of the delivered model as the VHDL code, tools should provide some sort of command-language export-import mechanism.

The development of validation suites at the binary interface level is a formidable and time-consuming task. A better approach is to develop tests in terms of system source code. This, in turn, requires that hardware interface software such as the BIOS or device drivers be included in the VHDL system model. The integration, test, and validation of system models that include hardware and embedded software require either a static or dynamic debug approach. Commercial VHDL environments provide the basic capabilities required to perform static debug with native interface code. The same is not true, however, of dynamic techniques requiring cross-compilers and interactive high-order language debuggers.□

Steven Rood Goldman, Protocol, a Div. of Zycad Corp., 500 International Dr., Mt. Olive, N.J. 07828-1381; (201) 347-7900.

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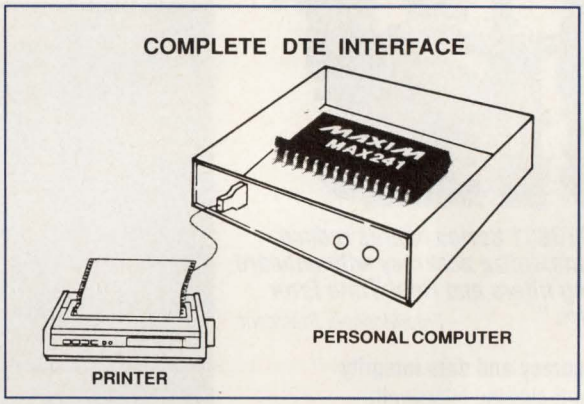

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MAX232	2	2	4x1μF	No/No
MAX233	2	2	None	No/No
MAX234	4	0	4x1μF	No/No
MAX235	5	5	None	Yes/Yes
MAX236	4	3	4x1μF	Yes/Yes
MAX237	5	3	4x1μF	No/No
MAX238	4	4	4x1μF	No/No
MAX239	3	5	2x1μF	No/Yes
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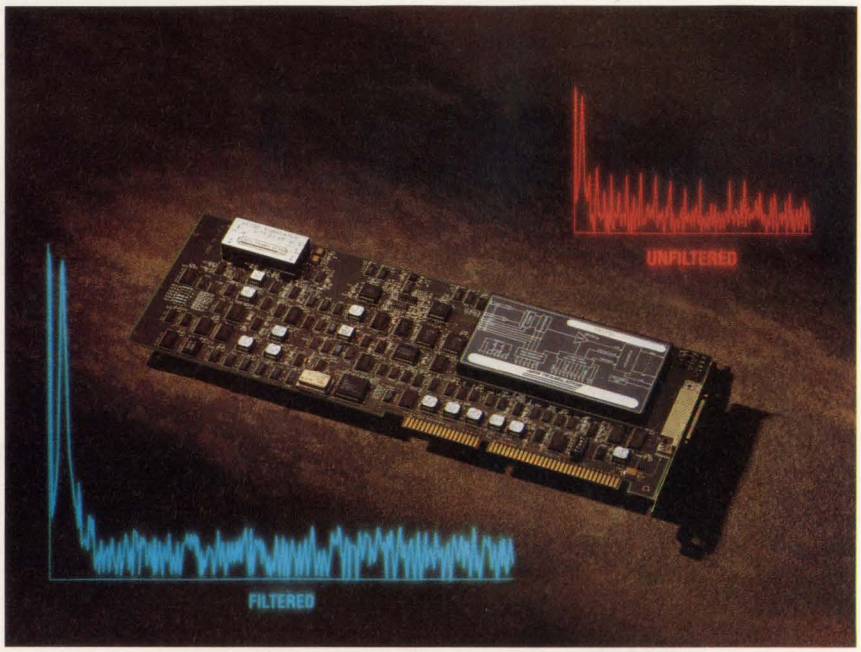

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CIRCLE 122 FOR U.S. RESPONSE CIRCLE 123 FOR RESPONSE OUTSIDE THE U.S.

GET F-V CONVERTERS TO SETTLE FAST WITHOUT RIPPLE

MODIFYING CONVENTIONAL FVCS CAN ELIMINATE RIPPLE AND CUT SETTLING TIME 1000-FOLD.

R. MARK STITT and ROD BURT
Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; (602) 746-7445.

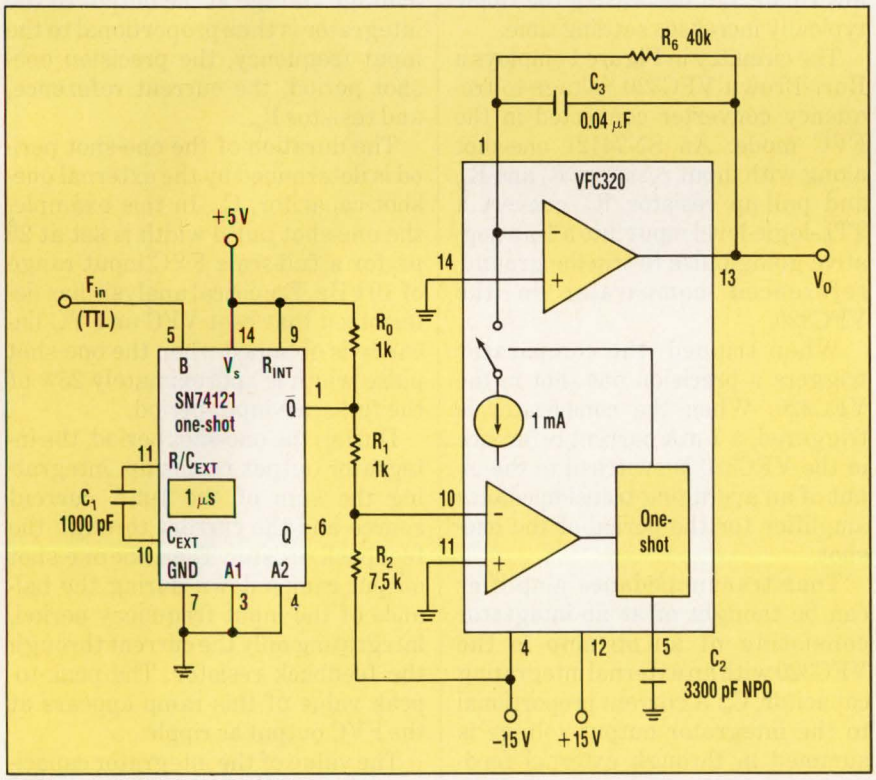
Over the past two decades, frequency-to-voltage and voltage-to-frequency converters (FVCs and VFCs) have performed a wide range of control, measurement, and isolation tasks. Although FVCs have progressed over the years, there's still room for improvement. This article details a novel scheme that modifies conventional FVC circuitry to eliminate ripple from the output and improve settling time by more than 1000:1. Moreover, the dc precision of the FVC isn't affected. The combination of improved features opens new doors to solving real-world problems. That's because with the modified FVCs, measurements can be taken faster and less post-conversion signal conditioning is needed.

Frequency of rotation is one of the most commonly made measurements for mechanical devices—the world is replete with rotating machinery from motors to automobile wheels. Very often, the frequency of rotation must be converted into an analog voltage signal. But that conversion raises the question of how to perform the conversion quickly, accurately, and without ripple.

Another major application for FVCs involves their ability to isolate high-voltage analog signals. High-voltage analog isolation amplifiers (iso amps), such as the Burr-Brown ISO121, can isolate signals of up to 8 kV. Voltage isolation of tens-of-thousands or even millions of volts, as in utility-power-transmission line monitoring, nuclear event monitoring, and protection from lightning strikes, calls for other techniques. One can get virtually unlimited isolation by using a VFC to digitize an analog signal and transmit it over a fiber-optic link to an FVC, where the signal is then reconstructed.

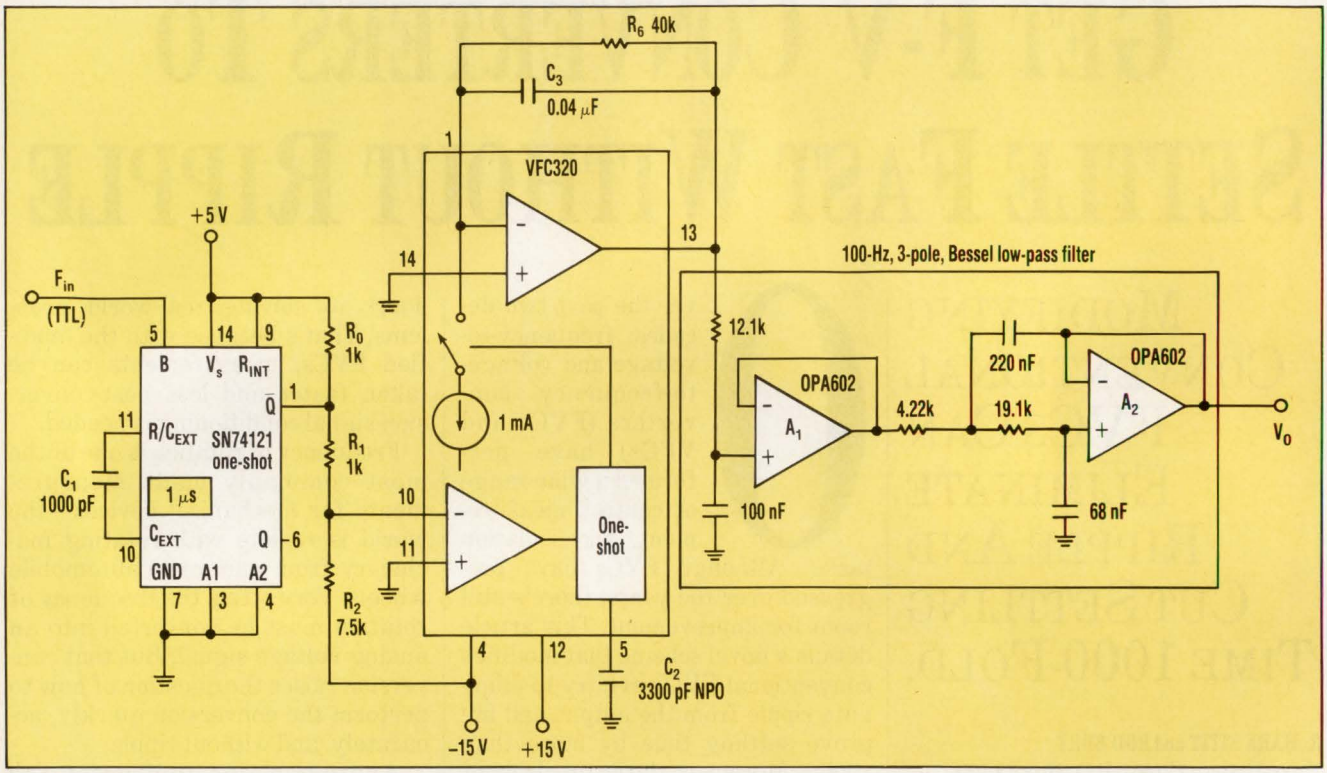
The FVCs and VFCs do this almost naturally since non-contacting frequency detection schemes can isolate the mechanical device or pulse-generating device being measured from the voltage generated by the converter, or vice-versa. A VFC can isolate a voltage being measured by generating a representative variable pulse train that might drive an isolating optical coupler (or some other device or scheme) that receives the pulses and then feeds the pulse train into an FVC to regenerate the voltage level.

Often, VFCs are favored for ana-



1. A CONVENTIONAL frequency-to-voltage converter can be made by connecting a Burr-Brown VFC320 voltage-to-frequency converter in the FVC mode. Capacitor C_3 should be selected for the best ripple/settling-time trade-off.

FAST SETTLING FVCs



2. ADDING A 3-POLE, low-pass Bessel filter to a conventional FVC's output reduces the ripple to less than 1 mV at 1.2 kHz.

log-to-digital conversion because of their integrating input characteristic and high resolution (modern sigma-delta analog-to-digital converters are really a variation of a VFC with digital filtering and encoding). An analog signal digitized by a VFC can be transmitted to a remote receiver serially over a twisted-pair cable or isolated with an optical isolator. At the other end, the digital signal can be both digitally processed and reconstructed to analog.

An analog signal is often required, for instance, in medical applications for bedside monitoring on a CRT or LCD display. The fast-settling, ripple-free characteristics of the improved FVC described here makes the converter ideal for these kinds of applications.

THE CONVENTIONAL FVC

In a conventional FVC, the output of a one-shot-controlled current reference is averaged *(Fig. 1)*. However, the conventional FVC's performance is the result of trade-offs between ripple and settling time. To improve converter resolution demands low ripple, but decreasing the ripple typically increases settling time.

The circuitry in Figure 1 employs a Burr-Brown VFC320 voltage-to-frequency converter connected in the FVC mode. An SN74121 one-shot along with input resistors R_1 and R_2, and pull-up resistor R_0, convert a TTL-logic-level input into a 1-μs negative-going pulse to trip the ground-referenced comparator in the VFC320.

When tripped, the comparator triggers a precision one-shot in the VFC320. When the comparator is triggered, a 1-mA current reference in the VFC320 is switched to the input of an averaging transimpedance amplifier for the period of the one-shot.

That transimpedance amplifier can be thought of as an integrator consisting of an op amp in the VFC320 with an external integrating capacitor, C_3. A current proportional to the integrator output voltage is summed in through external feedback resistor R_6. Both the periodic 1-mA current pulse and the current through R_6 are integrated in C_3. The average voltage at the output of the integrator is thus proportional to the input frequency, the precision one-shot period, the current reference, and resistor R_6.

The duration of the one-shot period is determined by the external one-shot capacitor, C_2. In this example, the one-shot pulse width is set at 25 μs for a full-scale FVC input range of 10 kHz. Empirical analysis has determined that best VFC or FVC linearity is obtained when the one-shot pulse width is approximately 25% of the full-scale input period.

During the one-shot period, the integrator output ramps up, integrating the sum of the 1-mA current source and the current through the feedback resistor. Then, the one-shot output ramps down during the balance of the input frequency period, integrating only the current through the feedback resistor. The peak-to-peak value of this ramp appears at the FVC output as ripple.

The value of the integrator capacitor affects the FVC output ripple, but doesn't affect the average dc output voltage. Increasing the ca-

FAST SETTLING FVCs

pacitance value decreases the voltage ripple but increases the time needed by the integrator output to settle due to a change in input frequency. Settling time follows a single-pole response.

FILTERED FVC PERFORMANCE WITH BESSEL FILTER

Filter Order	f-3dB [Hz]	settling (0.01%) [s]	ripple (@ 1.2kHz) [mV]	ripple (@ 400Hz) [mV]
2	35	38	1	8
3	100	18	1	25
4	155	17	1	59
5	205	17	1	134

The following relationships apply for the conventional FVC:

$V_O = F_{in} \times T_{OS} \times I_R \times R_6$ (same for conventional and fast-settling FVC)

$RIPPLE \approx T_{OS} \times I_R / C_3$

$t_S = R_6 \times C_3 \times \ln(100/\%)$

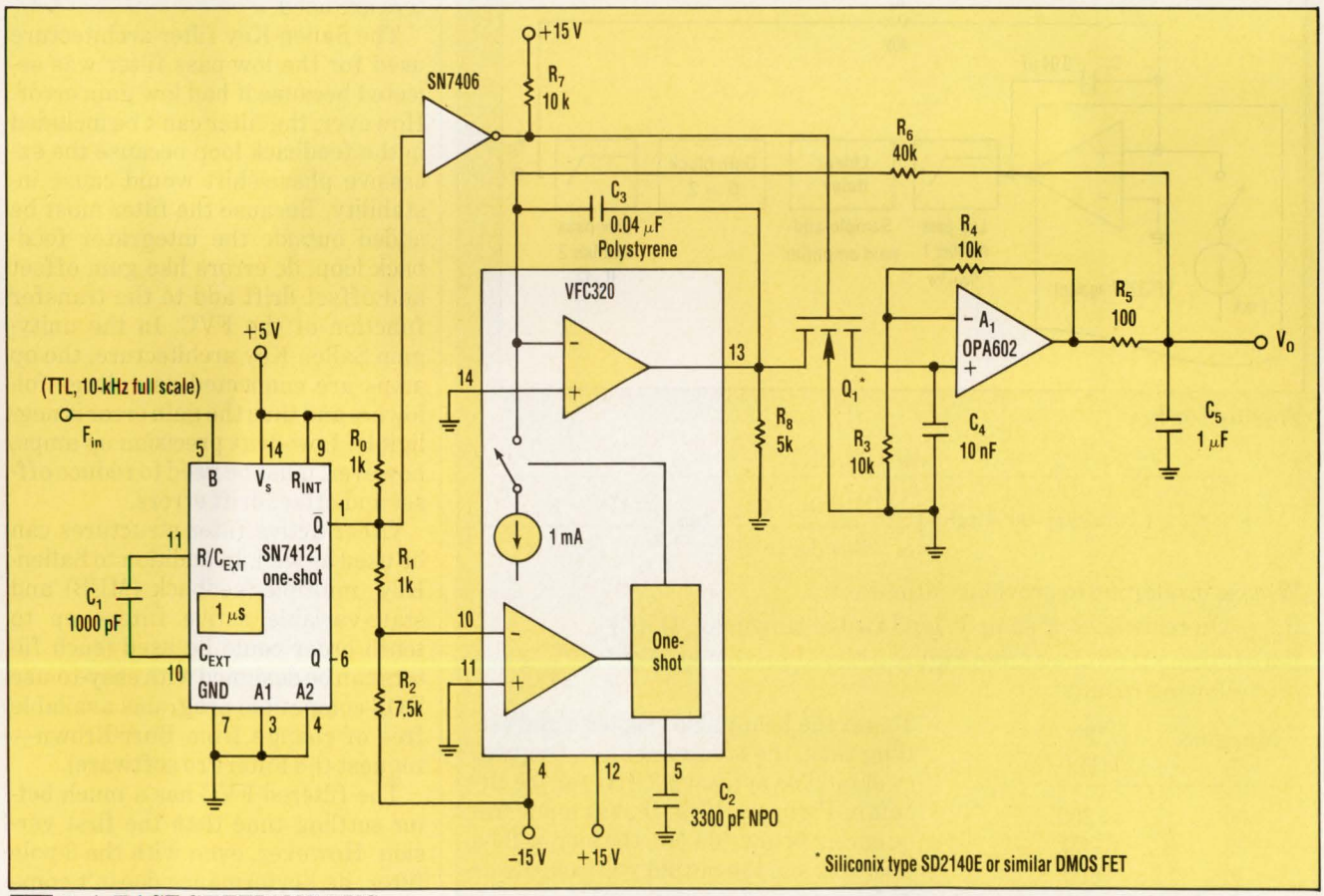
Where:

V_O = Average output voltage (V)
F_{in} = Input frequency (Hz) (10 kHz full-scale in this example)
I_R = Current reference (A) (1 mA for the VFC320)
T_{OS} = One-shot period (s) (25 μs in this example)
t_S = Time for the output to settle to desired tolerance (s)
R_6 = Integrator feedback resistor (Ω) (40 kΩ for a 10-V full scale output with a 10-kHz input)
RIPPLE = Variation in V_O ($V_{pk\text{-}pk}$)
C_3 = Value of integrator capacitor (F)
% = Desired precision of the output signal (% of full-scale)

The conventional FVC has excellent dc performance, but poor dynamic performance. For instance, in the previous example, the conventional FVC achieves a resolution to within 0.01% (with 1 mV of ripple), with C3 set to 25 μF. Those component values result in an unacceptably long settling time of 9.2 seconds.

In practice, the settling-time/ripple trade-off of the conventional FVC can be improved substantially by filtering the FVC output with a higher-order low-pass filter *(Fig. 2)*. In this approach, a conventional FVC is designed with relatively high output ripple so that it will settle fast. Then a high-order low-pass filter is added in series with the FVC output to reduce the ripple.

As in Figure 1, this modified circuit also adjusts R_6 to 40 k to set a 10-V full-scale output for a 10-kHz input. The value for C_3 drops to just 0.04 μF, which results in a maximum ripple of about 625 mV. This is an ar-



3. A FAST-SETTLING FVC is formed by adding a sample-and-hold amplifier in the feedback loop of the conventional FVC. The improved converter can settle to 0.01% in 7.4 ms without ripple. Because the SHA is in the feedback loop, FVC precision is unaffected.

FAST SETTLING FVCs

STABILITY OF FAST-SETTLING FVCS

Stability in sampled systems depends on sampling frequency. Since SHA in the feedback loop of the fast-settling FVC is controlled by the input frequency, there's a minimum input frequency required to assure loop stability. As input frequency decreases, delay through the SHA increases, thereby decreasing phase margin of the integrator loop. The feedback-loop block diagram gives a fairly accurate stability-criteria analysis. Phase margin of the loop is as follows:

$\text{Margin} = 180° - 90° - \text{delay}_1 - \text{delay}_2 - \text{delay}_3$

Where:

Margin = phase margin of the loop

90° = phase delay of the R_6-C_3 dominant pole

delay_1 = delay of sample-hold switch, Q1, and hold capacitor, C4

$\text{delay}_1 = \text{Tan}^{-1}(f_{UG} \times 2 \times \pi \times R_{Q1} \times C_4)$

delay_2 = delay due to R_5-C_5 output filter

$\text{delay}_2 = \text{Tan}^{-1}(f_{UG} \times 2 \times \pi \times R_5 \times C_5)$

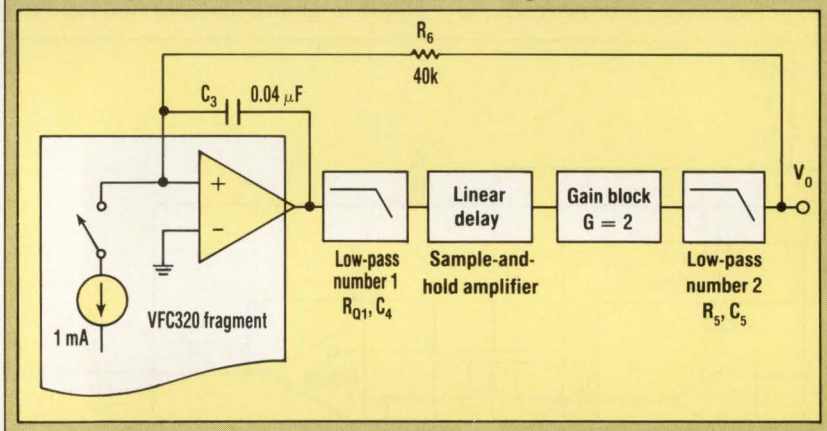
delay_3 = delay due to sample period

$\text{delay}_3 = (360 \times f_{UG}) / (2 \times F_{in})$

f_{UG} = unity-gain frequency of the overall integrator loop

$f_{UG} = \text{GAIN}/(2 \times \pi \times R_6 \times C_3)$

GAIN = gain of the SHA in the feedback loop



Solving for F_{in},

$$f_{in} = \frac{-90° \times \text{GAIN}}{\pi \times C_3 \times R_6 \left(\text{margin} - 90° + \tan^{-1}\left(\frac{\text{GAIN} \times R_5 \times C_5}{R_6 \times C_3}\right) + \tan^{-1}\left(\frac{\text{GAIN} \times R_{Q1} \times C_4}{R_6 \times C_3}\right)\right.}$$

Where, in addition to previous definitions:

R_{Q1} = On-resistance of sample/hold switch-transistor, Q_1 (Ω)

Substituting the values from Figure 3 *(p. 75)*, and using 25 Ω for R_{Q1}, gives the following results:

Margin (°)	F_{in} (Hz)
60	1200
45	780
30	600
0	400

To get the best pulse response and settling time, the minimum input frequency should be at least 1.2 kHz for the circuit in Figure 3. Note that at input frequencies below 400 Hz, the loop will be unstable and the output will oscillate or lock up.

bitrary but adequate value to give excellent linearity for the 10-V full-scale output. Higher ripple would reduce the linear output range of the FVC because, at full-scale, the FVC output must swing 10 V plus approximately one half the ripple voltage.

There are many output filter structures that can be used to implement a filtered FVC. Because of its excellent pulse response a Bessel filter gives the fastest settling of any standard filter type *(see the table)*. Bessel filters with orders from 2 to 5 are compared for performance as an output filter. The 3-pole Sallen-Key Bessel filter gives a good settling-time versus complexity trade-off. Such a filter is used in the enhanced FVC shown in Figure 2. With the filter $f_{-3\,dB}$ frequency set to 100 Hz, ripple at 1.2 kHz is below 1 mV and settling time to within 0.01% drops to just 18 ms. Note, however, that ripple increases dramatically below 1.2 kHz when higher-order output filters are used.

The Sallen-Key filter architecture used for the low-pass filter was selected because it had low gain error. However, the filter can't be included in the feedback loop because the excessive phase-shift would cause instability. Because the filter must be added outside the integrator feedback loop, dc errors like gain offset and offset drift add to the transfer function of the FVC. In the unity-gain Sallen-Key architecture, the op amps are connected as voltage-followers and thus the gain error is negligible. Low-drift precision op amps, however, must be used to reduce offset and offset drift errors.

Other active filter structures can be used as well. In addition to Sallen-Key, multiple-feedback (MFB) and state-variable active filters up to tenth order could be used (such filters can be designed with easy-to-use DOS-compatible programs available free of change from Burr-Brown—request the FilterPro software).

The filtered FVC has a much better settling time than the first version. However, even with the 3-pole filter, its performance doesn't come close to the fast-settling FVC. With the same values for R_6 and C_3, the

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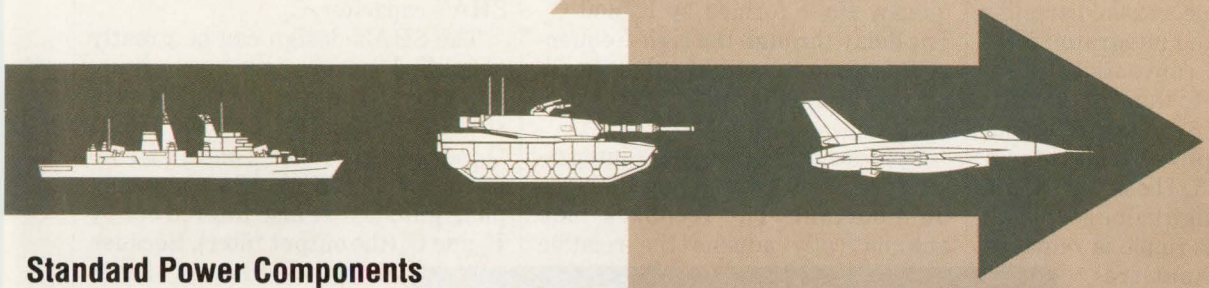

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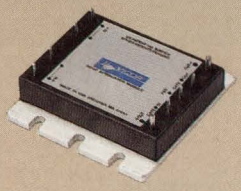

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FAST SETTLING FVCs

novel modifications to the FVC trim the settling time to 7.4 ms for resolution to within 0.01% and produce less than 1 mV of ripple at any frequency.

THE FAST-SETTLING FVC

Instead of using a filter in series with the output, the fast-settling FVC uses a sample-and-hold amplifier (SHA) inside the integrator feedback loop of the conventional FVC *(Fig. 3)*. One way to think of the fast-settling FVC is as a conventional FVC with an adaptive N-pole filter in the feedback path. The order, N, approaches a very high value so that all integrator output ripple is removed regardless of input frequency.

In comparison, the output ripple of the filtered FVC increases with decreasing frequency. Furthermore, delay of the adaptive filter is low so that it can be included in the feedback loop to the integrator without adversely affecting stability. That would not be possible with a conventional filter. With the filter included in the feedback loop, such dc filter errors (SHA errors) as gain, offset, and offset drift are divided down to negligible levels by the loop gain of the integrator amplifier.

Although the same values for R_6 and C_3 are used in the example, a smaller value could be used for C_3 in the fast-settling FVC to achieve an even better settling time. Ripple at the output is eliminated by using a SHA to sample the VFC320 integrator output. The only constraint on ripple voltage is that it must be within the linear output-swing range of the integrator amplifier. Gain can be added in the SHA to reduce the peak amplitude needed from the integrator output. In the filtered approach, added gain would also amplify the ripple.

In the fast-settling FVC, the SHA acquires a feedback signal from the integrator output ramp in approximately 1 μs. That translates the ramp's ripple to a higher frequency. The ripple is substantially eliminated by a simple single-pole, high-frequency filter formed by R_5 and C_5. The delay through the high-frequency filter is low enough so that the filter can also be included in the feedback loop.

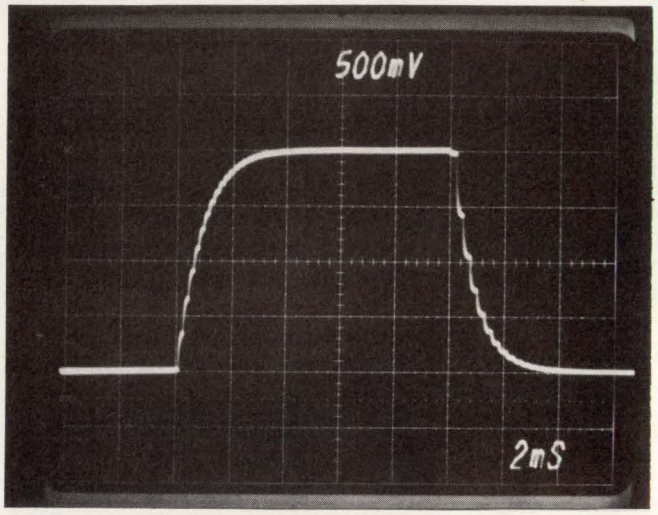
Because the SHA is in the integrator's feedback loop, trigger timing is unimportant. The feedback loop automatically adjusts the relative level of the integrator output signal for proper alignment with the trigger pulse. The SHA is controlled by the 74121 one-shot through a 7406 open-collector inverter that forms a level shifter. Pull-down resistor R_8 is added at the output of the integrator amplifier to boost output drive to the SHA's capacitor, C_4.

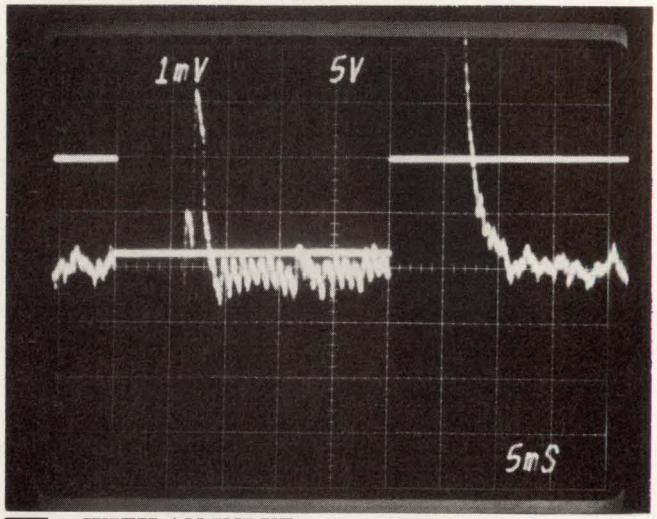
The SHA's design can be greatly simplified because dc accuracy is unimportant. The complete SHA consists of a general utility DMOS FET, Q_1; a hold capacitor, C_4; and a FET-input op amp, A_1. High-frequency sampling glitches are also filtered out by R_5 and C_5 (the output filter). Because the glitch filter is also in the integrator feedback loop, associated dc errors are eliminated and low dc output impedance is maintained.

SHA gain is set to 2 V/V by R_3 and R_4. The gain setting attenuates (by two) the maximum output excursion necessary from the VFC320 integrator output. That allows both a comfortable +10-V full-scale output from the FVC and a large ripple signal at the integrator output.

Gain in the feedback loop of the integrator also increases slew rate and bandwidth. With a high slew-rate op amp used for A_1, the FVC slew rate is limited by the integrator's op amp. Furthermore, because the actual SHA gain isn't critical, adding a gain of two in the feedback loop doubles the FVC slew rate. However, because the amplifier is in the feedback loop, gain errors in the sample-and-hold circuit don't affect the gain of the FVC or degrade its accuracy.

The fast-settling FVC has the same dc transfer function as the simple FVC, but without ripple at the output. Measured dc performance of the fast-





4. WITH AN INPUT signal of 6 to 8 kHz, the FVC provides a small-signal step response of ±1 V (actually +6 to +8 V) that settles very quickly and is very stable (a). Actual measurement of the FVC's settling time of about 7.4 ms to within 0.01% shows good agreement with the theoretical value. The residual error waveform is superimposed on the square theoretical output signal (b).

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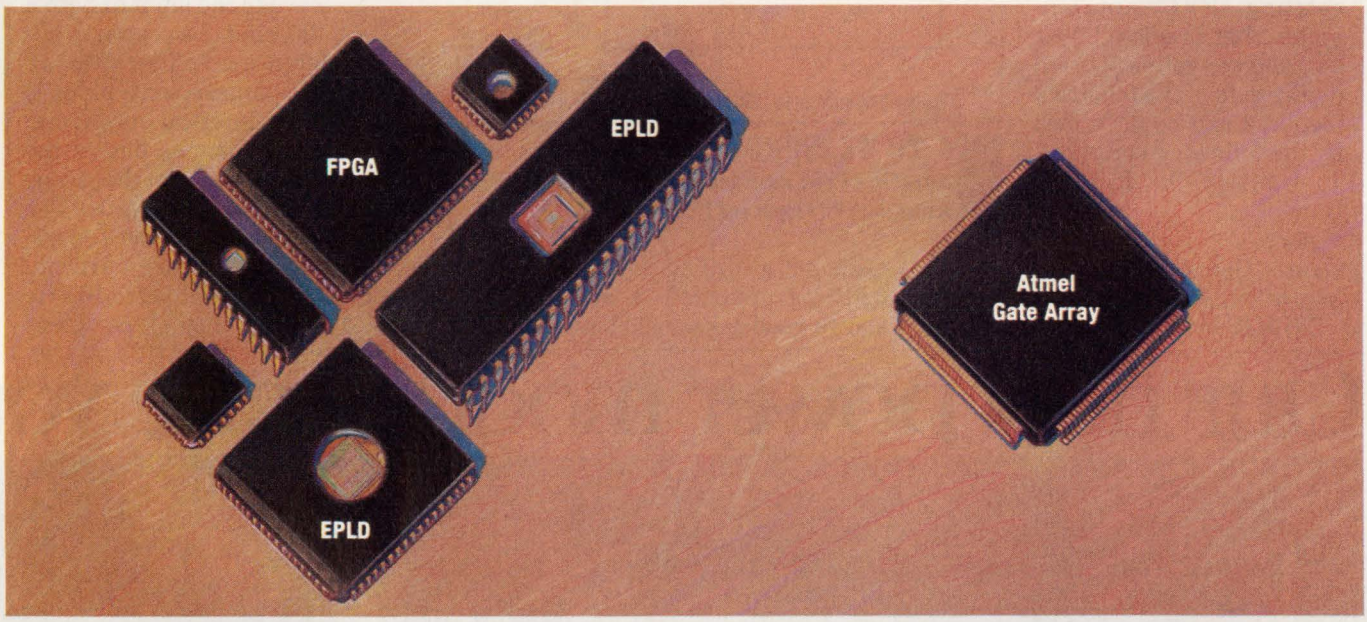

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FAST SETTLING FVCs

settling FVC delivers nonlinearity better than 10 ppm (better than 16 bits). A view of the signal shows the excellent small-signal ±1 V (actually +6 to +8 V) output step response for the FVC with a 6-to-8-kHz input frequency change *(Fig. 4a)*. If the phase margin were low, this signal would exhibit overshoot and ringing.

Settling time of the fast-settling FVC approximates that predicted by a single-pole system boosted by the gain in the feedback loop and can be described by the following equation:

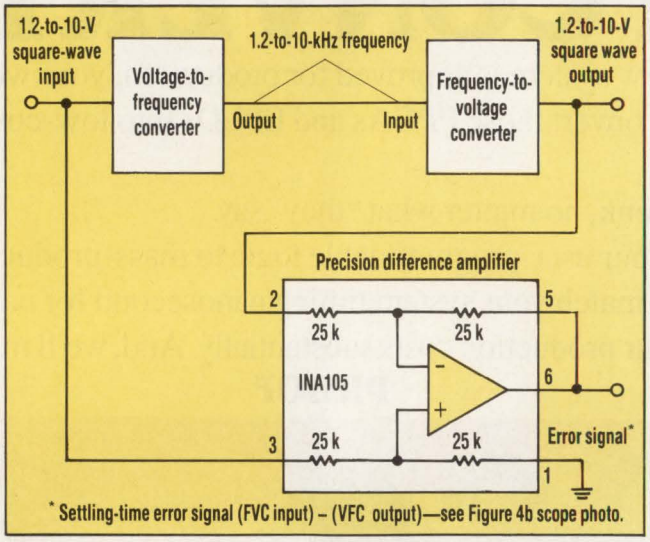
$T_S = \ln(100/\%) \times R_6 \times C_3 / \text{Gain}$

Where:

Gain = Gain of SHA in the feedback loop of integrator

With $R_6 = 40\ k\Omega$, $C_3 = 0.04\ \mu F$, and Gain = 2, a settling time of 7.4 ms to 0.01% is predicted. A scope photo shows good agreement between theoretical and measured settling time for a large signal, +1.2-to-+10-V, output step due to a 1.2-to-10-kHz input frequency change *(Fig. 4b)*. In the photo, the residual error signal is superimposed on the theoretical output signal. Each graticule division is approximately 0.01%.

The circuit used to measure settling time applies a +1.2-to-+10 V square wave to the input of both a VFC and to a precision difference amplifier *(Fig. 5)*. This square-wave input is the theoretical output signal—shown as one of the two traces on the scope photo *(Fig. 4b, again)*. The VFC converts the square-wave input voltage square wave into a modulated TTL-level 1.2-to-10-kHz signal. The frequency signal feeds



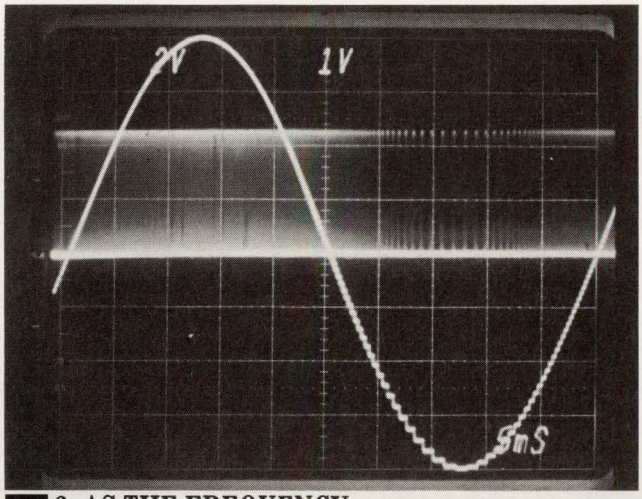
5. TO MEASURE the FVC settling time, connect a VFC's output to a FVC's input and place a precision difference amplifier across the VFC's input and FVC's output.

FAST SETTLING FVCs

directly into the FVC under test.

The output of the FVC, ideally a delayed reproduction of the input square wave, feeds into the inverting input of the difference amplifier. The difference amplifier subtracts the FVC output from the VFC input. The output of the difference amplifier, (FVC output)-(VFC input), is the residual error signal—shown as the second trace on scope screen shot *(Fig. 4b, again)*. For this method to work, the VFC must have small dynamic error compared to the FVC. The VFC used in these measurements was the Burr-Brown VFC320.

Figure 6 presents a qualitative picture of a sine-wave-modulated, 1-to-9-kHz, TTL-level (0 to 5 V) FVC input signal superimposed on the 1-to-9-V FVC output. The waveform was generated by driving a 1-to-9-V sine-wave signal into the test circuit and looking at the FVC input and output.



6. AS THE FREQUENCY on the input of the FVC changes over a 1-to-9-kHz range, this dual-trace scope waveform shows the FVC's ripple-free 1-to-9-V output.

At the lower 1-kHz frequency input, the steps between frequency-input pulses, seen on the sine-wave output, show excellent settling between pulses.□

Mark Stitt, a senior engineer at Burr-Brown, received his BSME from the University of Arizona, Tucson, and holds 15 U.S. and numerous foreign patents.

Rod Burt, also a senior engineer at Burr-Brown, received his BSEE from the University of Arizona and holds 10 U.S. patents.

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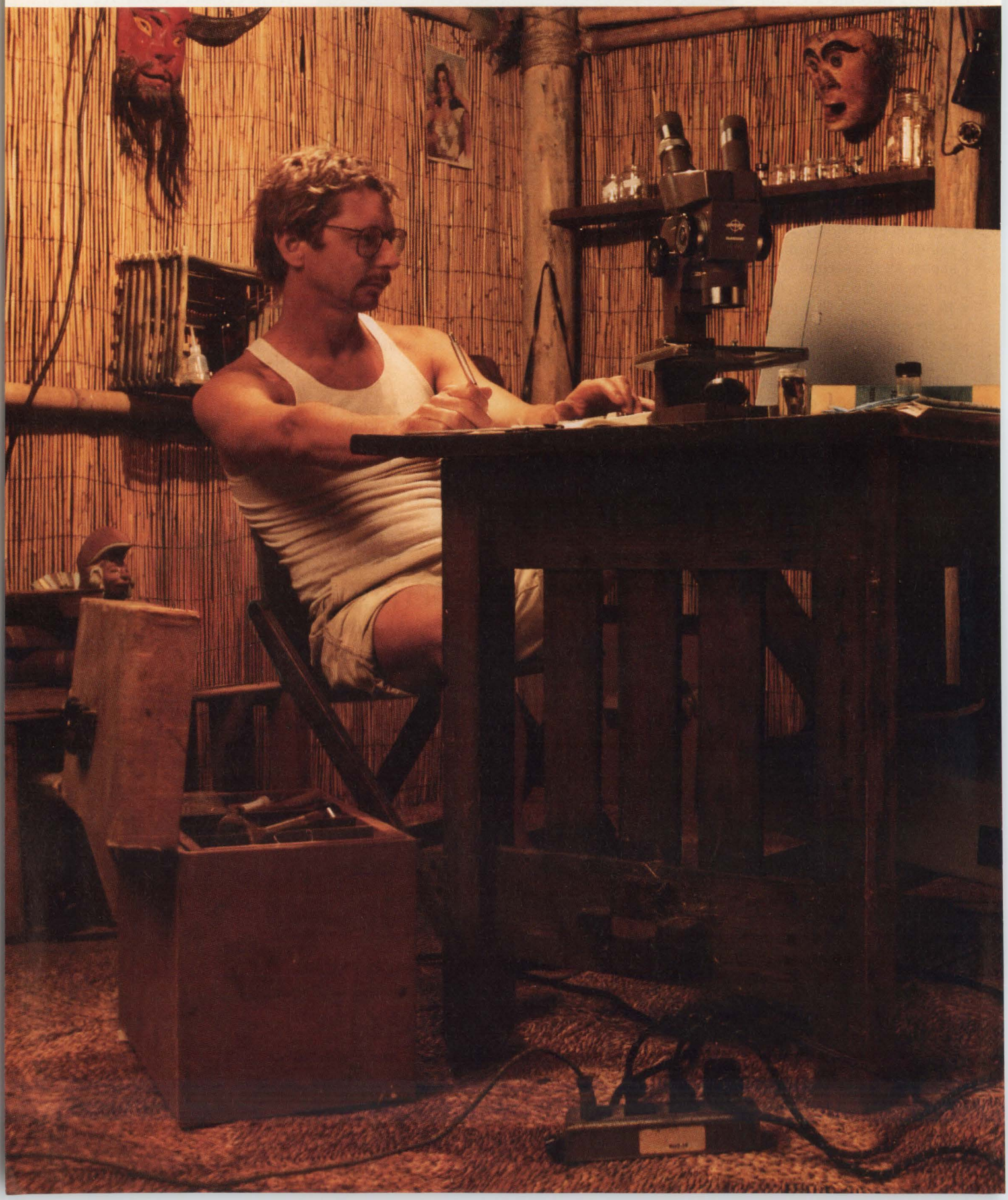

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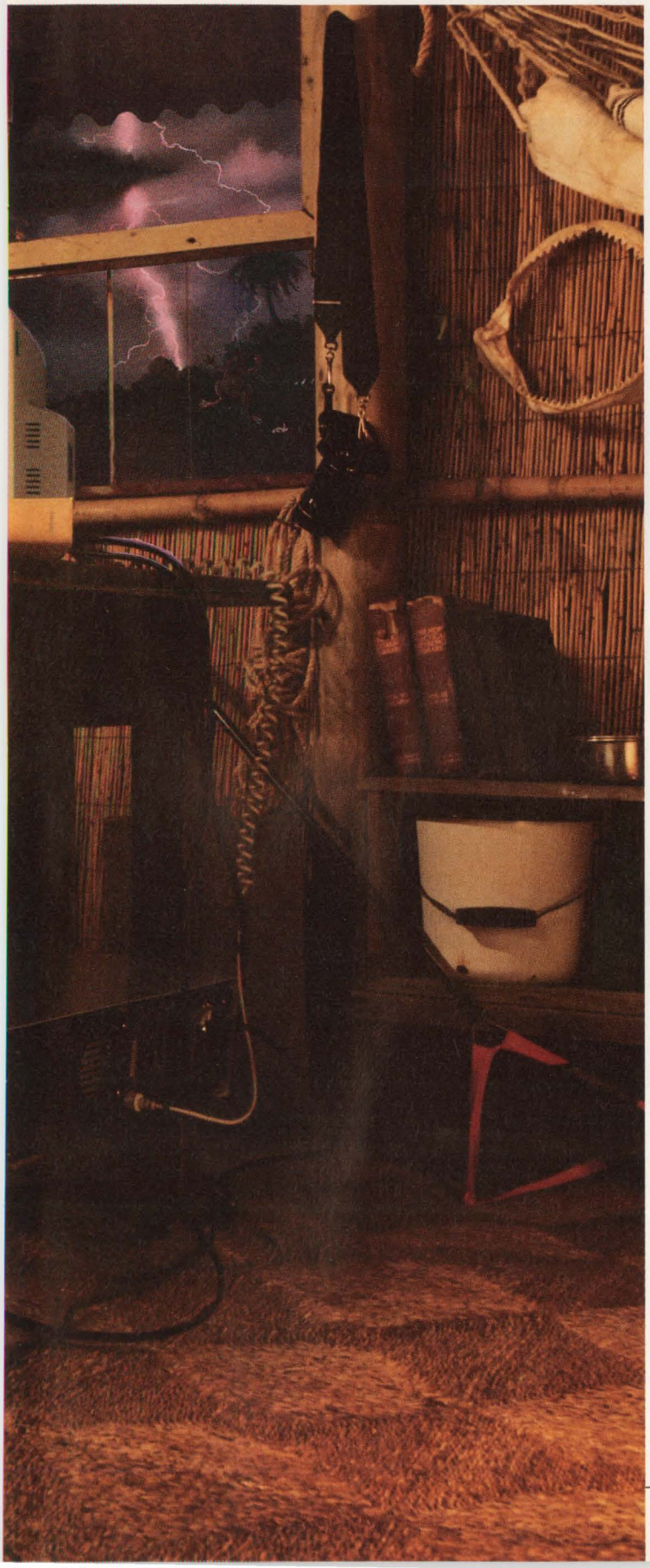

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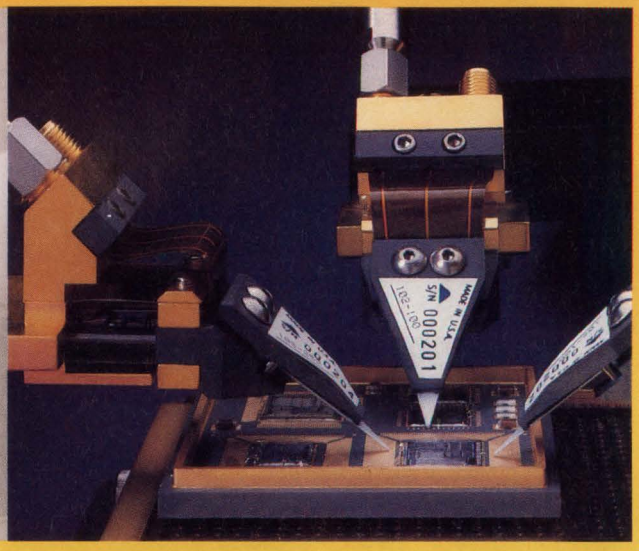

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Designers adapting to new test techniques

Fast fiber-optic telecommunciations systems create a new set of test-and-measurement problems.

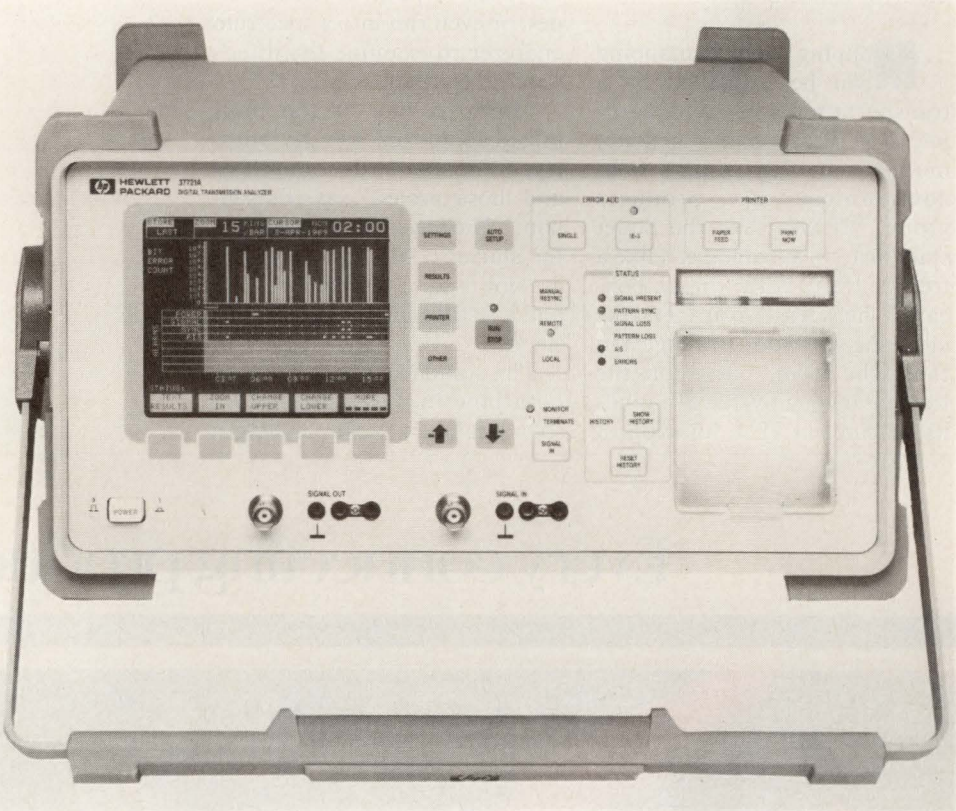
BY JOHN NOVELLINO

The burgeoning field of high-speed telecommunications is presenting new test-and-measurement challenges to engineers who may be unfamiliar with terms such as bit-error rate (BER), jitter, and wander. Most of the new systems are fiber-optic-based, and adding to the challenge is an array of standards, both operational and test oriented, that in many cases are still evolving.

Much telecommunications testing involves waveform analysis on oscilloscopes or specialized signal analyzers, using templates and masks *(see "New communications standards require specialized test," p. 89)*. Other measurements, such as BER and jitter tests, may use dedicated systems.

A BER test system consists of a pattern generator and a receiver with an error detector. These two components may be in separate instruments or combined into one unit. An interface in the generator ensures that the signal has the proper code format and output level for the applicable telecommunications standard.

The generator creates a pseudorandom binary sequence (PRBS), using a feedback shift register driven by a very stable clock source. The exact pattern needed depends mainly on the system-under-test's transmission rate, according to Alex Peake, a product marketing manager in Hewlett-Packard's Santa Clara Division. Higher bit rates need longer patterns. However, he notes that there are internationally agreed-upon standard patterns to send, ranging in length from $2^{15} - 1$ to $2^{23} - 1$ bits for high-speed systems.



On the receiving end, the incoming signal is decoded by an appropriate interface. The recovered clock drives a reference PRBS generator that creates a pattern identical to the test signal. After the system is synchronized, the receiver compares the incoming code to the locally-generated reference pattern and counts the errors.

Another subject of measurement concern, and the primary cause of bit errors, is jitter. This is also an area in which industry groups are doing much standards work. Jitter is the short-term variations in time of "significant instants" (typically edges) of a digital signal from their ideal positions. Because it is a normalized measurement, jitter is usually specified in unit intervals (UI) peak-to-peak, which is the equivalent of one clock period.

Since these time variations are themselves typically changing continuously, jitter also has a measurable jitter frequency. At very low frequencies, below 10 Hz, the variations in time are

called wander, rather than jitter.

Two basic types of jitter exist: Line jitter is essentially the frequency variations caused by imperfections in the circuity generating the clock and performing other functions, such as multiplexing, switching, or regeneration. The other type of jitter is payload mapping/demapping jitter, which results from the packaging and unpackaging of data signals into the proper formats for transmission.

Mapping and demapping can be explained by a transportation analogy, according to V. Prasannan, a product manager in Tektronix's telecommunications products group. "If you take the Sonet standard, for instance, it's like a freight train with empty boxcars," he says. "You can take anything you want, package it in the right form, put it on the train, and you now have the ability to carry it. The function of packaging it and putting it on the train is what mapping is all about."

Typically, jitter measurement involves recovering the clock signal from the incoming data and comparing it against a locally-generated high-quality clock signal. The process usually involves a phase-locked loop (PLL) whose error signal represents the phase errors or jitter. The results can be filtered to get the peak-to-peak or RMS values, or even run into a spectrum analyzer to examine the jitter's spectral content.

"Jitter is one of the most talked about topics in the industry, in the standards committees and those circles," says Prasannan. "The reason is it's complex, for starters. Also, most people are not used to testing for jitter, and it's still a large unknown for them."

The standards work involves both how to measure jitter, so that engineers using different test equipment can be assured of consistent results, and how much jitter a communication system or its components can tolerate. The latter is important because jitter tolerance varies greatly depending on the jitter frequency; at low jitter frequencies the PLLs in a system can actually track relatively large amounts of jitter. At jitter frequencies approaching the definition of wander, a system can handle up to 15 UI of jitter. At about 65 kHz, however, that tolerance drops to 0.15 UI.

In the past, most of the measurement standards work has revolved around fiber characterization. But in the last year or so the emphasis has switched to measuring the electronic signals themselves, and compliance with specific protocols and standards, according to Steve Blazo, a principal engineer in Tektronix's telecommunications products group. Blazo is working with the standards committee of

the Telecommunications Industry Association, which is affiliated with the Electronics Industry Association.

The industry groups want to make the test procedures as generic as possible, while at the same time ensuring consistent results, says Blazo. Manufacturers of telecommunications equipment must be able to test their units for compliance with the operating standards, which generally require multivendor capability.

A number of procedures are under consideration. Jitter-tolerance measurements on line-terminating equipment is one. That procedure will define how to inject jitter at various levels and frequencies while monitoring the unit under test for proper operation. Another standard will describe how to measure the jitter generated by a piece of line-terminating equipment. The procedure will have to standardize things like the signal to be injected at the device's input and the bandwidth over which over jitter will be measured at the output.

Several procedures are already in the balloting process and should be approved by early next year, says Blazo. They will then probably be submitted to the American National Standards Institute for approval as an industry-wide standard.

HP's Peake notes that a relatively new technique developed by his company, called modulation-domain analysis (MDA), can also be used to measure jitter. Unlike an oscilloscope, which presents a signal's amplitude vs. time (the time domain), or a spectrum analyzer, which displays amplitude vs. frequency (the frequency domain), MDA presents frequency, phase, or time-interval measurements vs. time.

"What we do is directly measure the variations in time of the edges," says Peake. "So we don't use PLLs, which have some inherent drawbacks." One problem with PLLs is that they're essentially filters, so the jitter measurement is somewhat distorted, he says. Also PLLs can't handle very large amounts of jitter, nor can they deal with very low-frequency jitter.

"Because the MDA technique measures jitter directly, it doesn't have any of the interfering effects of a PLL," says Peake. "And it can handle extremely large amounts—almost unlimited amounts—of jitter." Furthermore, the technique can characterize jitter at very low frequencies. Since the procedure is digital, any filtering can be done digitally.

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New Communication Standards Require Specialized Test

Mask and template techniques offer fast solutions for FDDI and SDH/SONET compliance testing.

BY V. PRASANNAN and KEVIN SMITH

Tektronix Inc., Telecommunications Product Lines, P.O. Box 500, MS 39-777, Beaverton, OR 97077; (503) 627-7231.

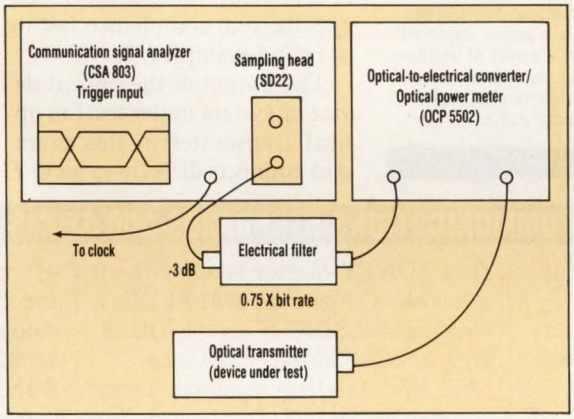
Evolving communications standards—ISDN, FDDI, and SDH/SONET in particular—will simplify and streamline voice and data links both locally and globally. At the same time, however, designers and manufacturers of digital communications equipment must adopt new test philosophies and capabilities for efficiently evaluating compliance with the new standards. Prime examples are pulse template and eye-diagram mask testing, which are recommended by the new standards themselves.

Templates and masks are graphic devices that use similar methods to specify allowable limits for waveforms. A simple, unipolar data pulse is a good example. The pulse can be specified by a list of parameters and limits: top amplitude, ±2.5% of nominal; overshoot, less than 25% of nominal top; 50% width, nominal ±0.725 ns, and so forth. Alternatively, the specification limits can be presented as normalized points on a graph.

Connecting the upper-limit points with straight lines establishes an upper boundary for the pulse shape. Similar connection of the lower-limit points establishes a lower boundary. Together the two boundary lines create an envelope—or template—that defines a region in which the pulse shape is acceptable. In other words, any pulse that fits within the template is an acceptable pulse.

Similarly, masks are devices for graphically expressing data signal specifications. But masks outline regions of unacceptability, rather than acceptability. Data conditions that intrude into a masked region are out of compliance with the mask specification.

Because the general concepts are so similar, the terms "template" and "mask" are often used interchangeably. In any case, templates and masks are a convenient and comprehensive means of graphically specifying data waveshapes.



1. A typical SDH/SONET eye-diagram test setup uses the recovered data clock for external triggering. If the device under test has an optical output, an optical-to-electrical converter is needed.

Templates and masks can also be a quick and convenient way to ensure that waveforms comply with the new communication standards. To do so, the FDDI data pulse or SDH/SONET data eye diagram is displayed on an oscilloscope. Then the corresponding template or mask is overlaid on the waveform display. If the displayed waveform fits the template or mask, the waveshape is in compliance. Designers don't need to measure a multitude of individual waveform parameters. They just make sure the waveform fits the specified template or mask.

The concept of template testing is quite straightforward. To implement it, however, designers must consider several requirements. These include capturing pulse waveforms at high data rates, providing optical-to-electrical conversion in the capture system, adding template or mask overlays to the data displays, and analyzing the results.

Because waveshapes must be observed and, possibly, some parameters measured, an oscilloscope is a basic test tool for FDDI and SDH/SONET compliance testing. The type of oscilloscope and the bandwidth needed depend on the testing method chosen and the system's data rates. A wide range of general-purpose oscilloscopes can meet the bandwidth requirements for viewing 125-Mbps FDDI waveforms. The data rates used in SDH/SONET channels, however, are another matter *(see the table)*.

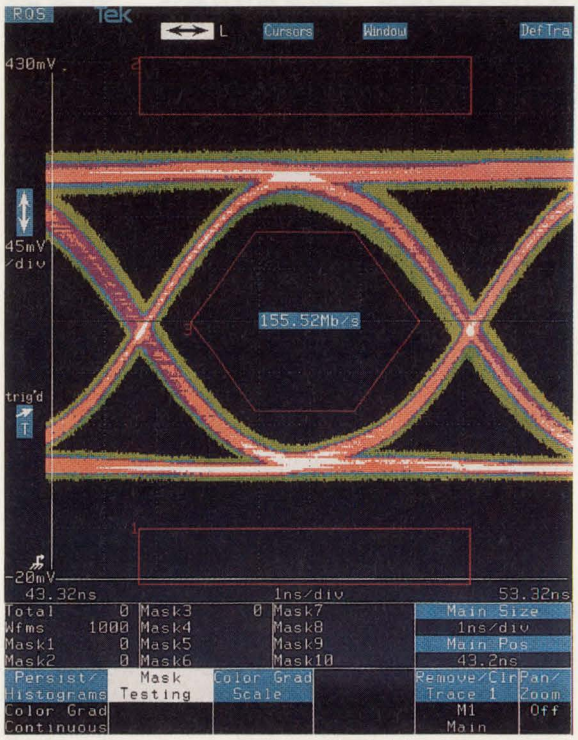
For example, 2488.32-Mbps waveforms (SDH-16/SONET STS-48 signals) may require an oscilloscope bandwidth as high as 20-GHz for accurate measurement of rise times, fall times, jitter, and other waveform parameters specified by the standard. High triggering bandwidths are also needed to create eye diagram displays at such speeds.

Generally, gigahertz-bandwidth acquisition means using an oscilloscope with direct-input sampling heads—that is, a scope with no preamplifier

ahead of the sampling bridge. The signal being acquired goes directly to the sampling bridge for sequential sampling. The advantage in this technique is that the only input bandwidth limit is that of the sampling bridge. Today's direct-input sampling technology delivers oscilloscope bandwidths to 50 GHz, allowing coverage of the highest SDH/SONET channels.

While direct-input sampling offers a tremendous bandwidth advantage, the tradeoff is an input-signal dynamic range limited to 1 Vpk-pk. However, a 3-GHz oscilloscope amplifier plug-in has recently been introduced. This amplifier can capture signals up to SDH-16/STS-48 through a scaled preamplifier, offering 10-mV/div. to 1-V/div. display ranges, rather than the 1-Vpk-pk maximum of direct input sampling.

Along with waveform acquisition and analysis capability, it's also important to keep in mind that FDDI and SDH/SONET are optical-based systems. As a result, optical-to-electrical (O-E) conversion will be needed for any testing done on the optical side of the system. A test setup for SDH/SONET eye-diagram compliance testing is a good example *(Fig. 1)*.



2. An eye diagram is formed by overlaying multiple SDH/SONET data pulses captured in a series of oscilloscope sweeps, each triggered by a data-clock pulse.

The output of the optical device or system under test (an optical transmitter in this example) connects directly to an O-E converter. The converter's electrical output goes to a filter specified by the SDH/SONET test standard. The filter's output is then fed to the oscilloscope's direct-input sampling head. The scope is externally triggered by the system data clock to provide an eye-diagram display *(Fig. 2)*.

If the O-E converter used in this setup has a power meter, optical components can also be evaluated for compliance with average optical power requirements. If the converter doesn't have an integral power meter, a separate optical power meter must be added to the system.

A similar test setup—minus the O-E converter—can be used to test the electrical side of FDDI or SDH/SONET systems. The electrical output (of an optical receiver, for example) can be connected directly to the scope's sampling head or amplifier plug-in.

To simulate the random data patterns of digitized voice and other data communications signals, the test engineer applies pseudorandom bit sequence (PRBS) patterns to the

COMMUNICATIONS STANDARDS AND TERMS

ANSI—American National Standards Institute

CCITT—International Telephone and Telegraph Consultative Committee

CEPT—European Conference of Postal and Telecommunications Administrative Service

ECSA—Exchange Carriers Standards Association

FDDI—Fiber distributed data interface. A standard specified by ANSI X3T9 and developed primarily for standardized protocols and equipment for optical communications in local area network (LAN) and computer applications. FDDI data transmission rates of 100 to 125 Mbps can map directly into an SDH/SONET STM-1 or STS-3 frame.

OC-1—Optical carrier level 1. The first SONET carrier level, with an equivalent clock rate of 51.84 Mbps. The highest SONET level is OC-48, with a 2488.32-Mbps clock rate.

OSI model—Open systems interconnect model. A framework for developing and assigning communications protocols in a seven-layer, hierarchical fashion.

ISDN—Integrated services digital network. A complete network architecture following the guidelines of the OSI model. The B-ISDN standard from ANSI and the CCITT allows voice, data, and video on the same network, which can include both wire and optical fiber paths.

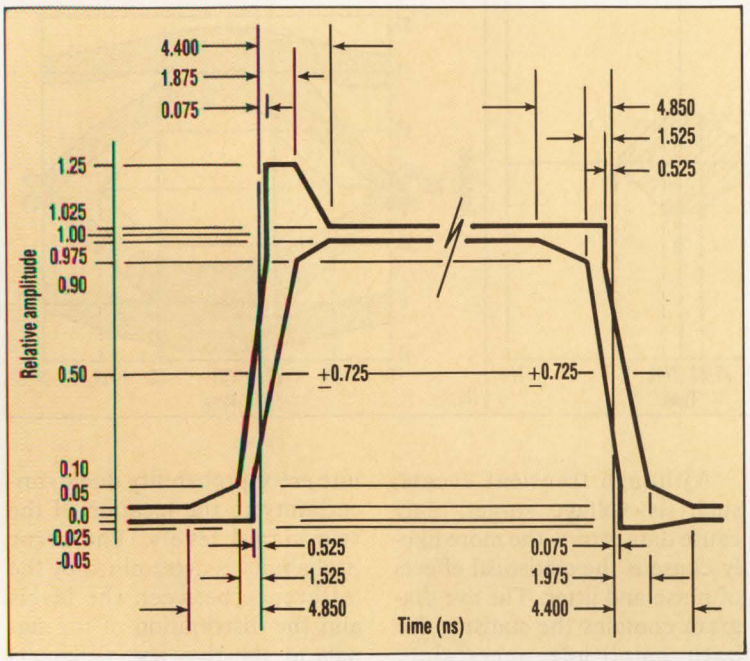
ISO—International Standards Organization

SDH—Synchronous digital hierarchy. A standard developed by ECSA and CCITT to define a family of optical transmission channels for transmitting voice, data, and video at rates from 51.84 Mbps to 2488.32 Mbps.

SONET—Synchronous optical network. The US equivalent of SDH, with some additional frequency channels.

STM-1—Synchronous transport module level 1. The basic signal level in SDH/SONET applications outside the US. Its 155.52-Mbps transfer rate is equivalent to an STS-3 signal.

STS-1—Synchronous transport signal level 1. The basic signal level in SDH/Sonet applications in the US. It is an electrical signal that's converted to or from an SDH/SONET optically based signal. STS-1 is the electrical equivalent of the OC-1 51.84 Mbps signal.

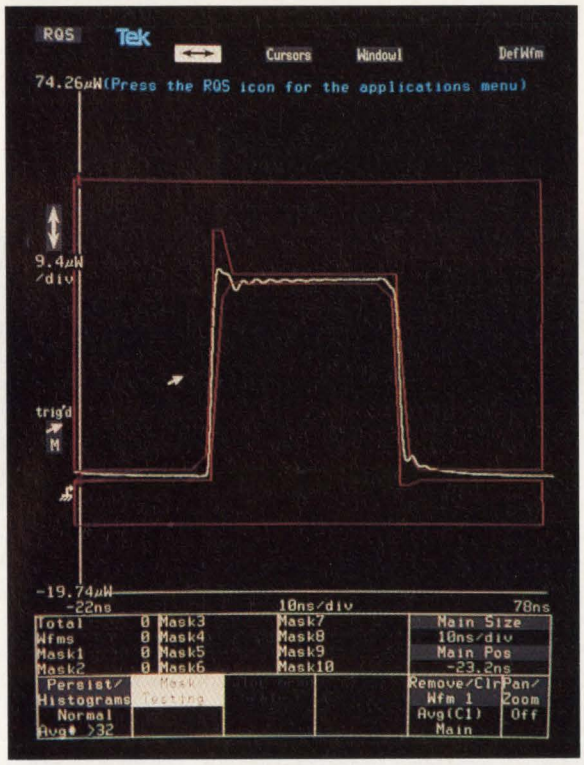


3. An FDDI pulse template defines the limits within which a pulse must fall. This graphical test technique is much faster than measuring numerous pulse parameters to verify compliance with the standard.

receiver or transmitter to be tested. A pattern generator can be used for this. In addition to containing the PRBS, however, the generator output must conform to the applicable FDDI or SDH/SONET standards. For example, for SDH/SONET, the instrument must generate a frame that contains both the payload (the PRBS used for testing) and the path overhead.

The simplest way to obtain a PRBS in the necessary transport format is to use the pattern generator from a SONET- or FDDI-compatible bit-error-rate tester. The output of this type of generator can be applied to the device or system being tested, and the example test setup can be used to capture the data waveforms and verify compliance to the standard.

As noted, FDDI compliance testing can be done by measuring individual pulse parameters: transition times, duration, amplitude, aberrations, symmetry, and so forth. Or compliance can be verified by making sure the data pulse fits within a specified FDDI pulse template *(Fig. 3)*. Although the FDDI standard specifies pulse templates, the concept is not an FDDI innovation. In the past, telephone equipment manufacturers have developed templates for checking waveshape compliance against their own internal standards as well as external standards. The benefits have been speed and simplicity.



4. Template testing can be automated with an oscilloscope that fits the data waveform to the template and logs any waveform points exceeding the template bounds.

The template technique, however, hasn't always been as efficient as it might be. The reason is that the traditional approach is to scribe or print the pulse template on a sheet of plastic cut to fit over an oscilloscope faceplate. The scope display of the data waveform is then positioned for the best fit within the template. Any portions of the waveform not fitting within the template bounds are considered template violations.

The problem is that the traditional approach is entirely manual. It relies heavily on the skill and attention of the person doing the test for proper positioning of the waveform within the template. Furthermore, the operator must still make rise-time, fall-time, and other measurements to document violations for any unit failing the test.

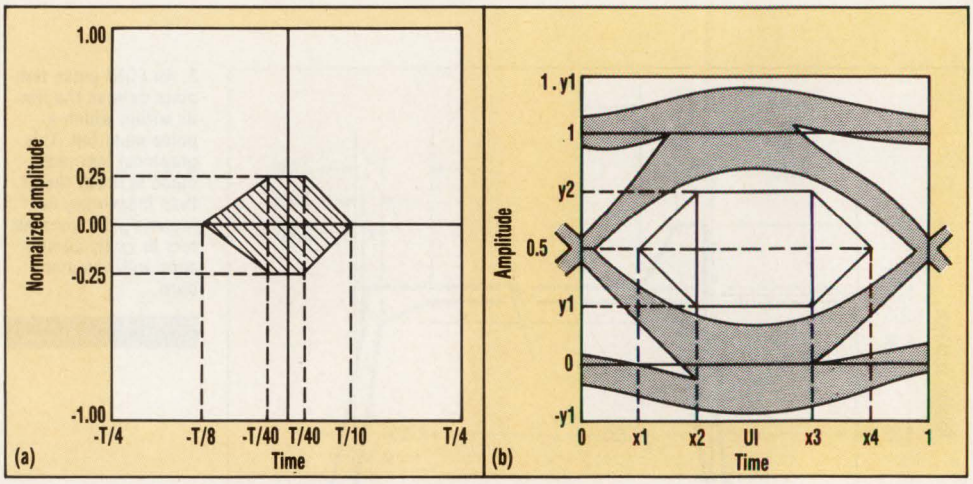
A more efficient approach is to use a digitizing oscilloscope with envelope or reference-waveform processing capabilities. These scopes can electronically create a template envelope on-screen along with the data waveform display. Control software then automatically fits the data waveform to the template and logs any waveform points exceeding the template bounds. The scopes can also automatically measure and display key waveform parameters such as rise and fall times *(Fig. 4)*. If needed, the entire screen display can be sent to a printer to document the results.

Besides automating the procedure, a digitizing scope also offers the advantage of allowing templates for different data rates and standards to be stored in software. These templates, whether electrical or optical, can be quickly retrieved as needed. Additionally, templates can be modified in software or new ones created to keep pace with evolving test needs.

A similar template concept can be used for SDH/SONET eye-diagram testing, which evolved because of the higher

data rates of SDH/SONET systems. At 155 Mbps and up, it's difficult to pick out one pulse for template testing as is done in a lower speed system. As a result, SDH/SONET specifies an eye diagram, which is a composite of multiple pulses captured as a series of oscilloscope sweeps, each triggered by a data-clock pulse *(Fig. 1, again)*. The variations in the data waveforms on the scope's vertical input channel are seen as multiple overlaid data pulses synchronized with the clock. These overlaid pulses form the eye diagram, which should fall within the limits defined by the appropriate masks. *(Fig. 5)*.

If the data pulses were ideal—that is, with instantaneous transitions and no noise or jitter—the eye diagram would be a series of end-to-end boxes *(Fig. 6a)*. But real-life pulses have finite transition times, which create the crossing points on either side of the eye opening. And uncertainties due to noise and jitter broaden the displayed signals and cause closing of the eye in the diagram *(Fig. 6b)*.



5. SDH/SONET eye-diagram masks vary depending on the data rate and interface being tested. A mask for STS-3 signals at the cross connect (a) differs from that for the optical transmit signal (b).

Although transient events, such as voltage surges, may cause data errors, the more likely cause is the statistical effects of noise and jitter. The eye diagram contains the statistics for both amplitude uncertainty (noise) and timing uncertainty (jitter). These statistics can be extracted by using histograms to construct distributions for the two levels and two adjacent crossings in the eye diagram.

Communication theory states that any binary signal has a finite error probability due to uncertainty in the location of the two signal levels. The error probability is determined by the difference between the levels and the distribution of the signals at the two levels. Signals with large level differences and a smaller standard deviation at each level are less likely to contain errors. Thus these two factors, the difference between the two levels and the level distributions, help determine the opening height of eye-pattern masks.

THE NEW COMMUNICATIONS STANDARDS

Not only do communications standards already exist, there are too many of them. In the US, ANSI-defined data rates differ from those defined by CEPT in Europe. Japan uses the same data rates as Europe, but with a different protocol.

The new standards are designed to eliminate these conflicts and provide a common data-transport method. For example, FDDI aims at standardizing LANs and other data communications. The specification increases data rates to 100 Mbps and uses the token-ring concept, but with a different protocol. On the other hand, the ISDN standard defines a network architecture and protocols for transmitting voice, data, and video from subscriber premises through local ISDN exchanges. Both FDDI and ISDN systems can be connected to the high-speed fiber-optic links defined by SDH/SONET.

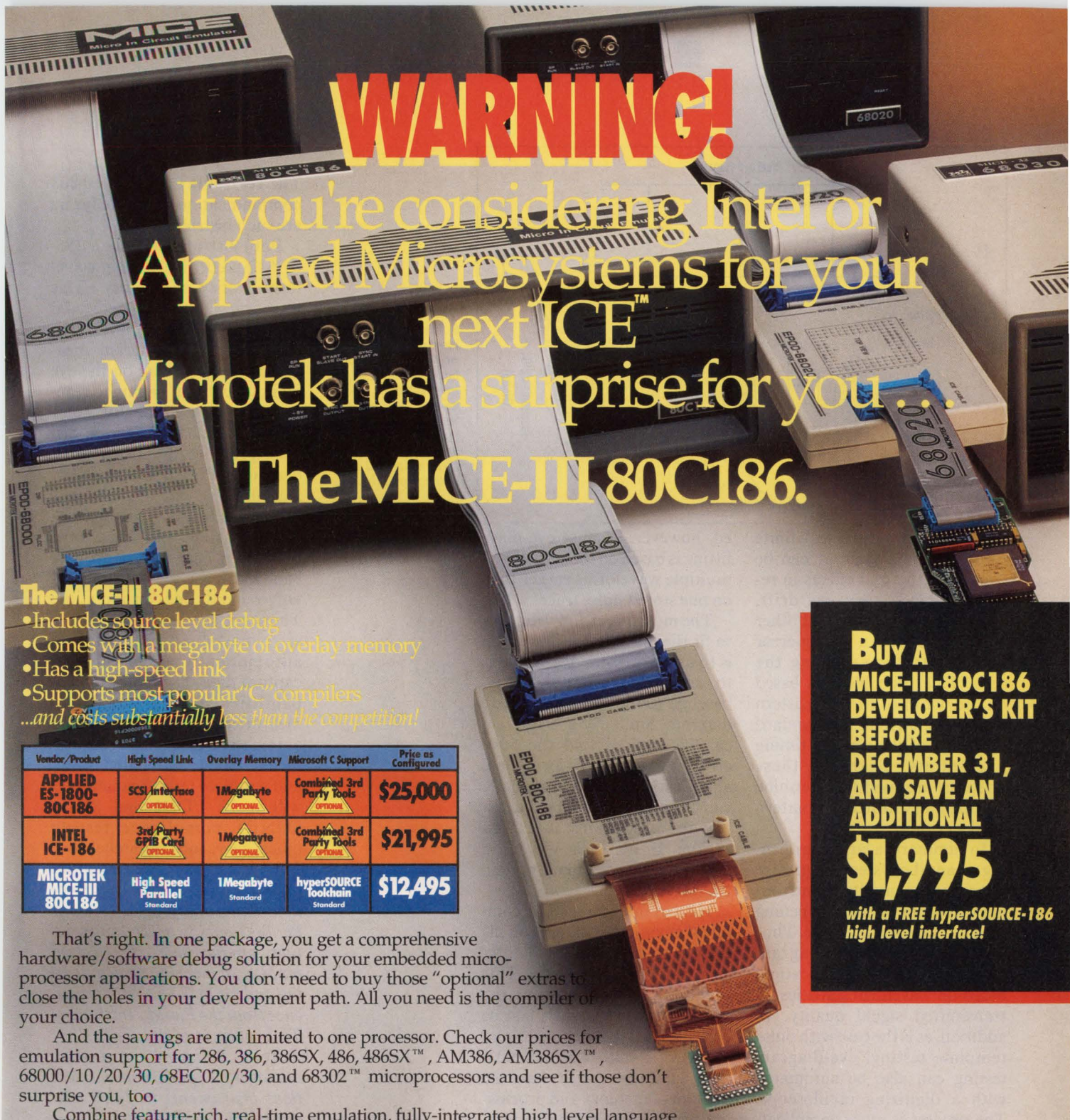
SDH, which was developed by the CCITT, and its US equivalent, SONET, create a common transport medium by defining standard data rates and a way to packetize information. SONET's base-level signal is STS-1, which runs at 51.84 Mbps. Higher-level signals are integer multiples of STS-1.

The specifications also establish a standard multiplexing format that uses any number of STS-1 signals as building blocks or frames. Each frame contains the payload (voice, data, etc.) and overhead (operations, administration, maintenance, and provisioning) for managing end-to-end routing of the payload.

Time-division multiplexing, byte interleaving, pointers, and synchronous transmission allow an assortment of digital information sources, called tributary types, to have equal access to channels and to transport information in standardized packets. Payload mappings, called virtual tributaries, divide STS frames into subframes, allowing systems to transport slower signals within the STS frame.

Unlike previous standards, SDH/SONET places substantial emphasis on overhead and makes overhead proportional to data rates. This is the only way to ensure compatible end-to-end mixing of equipment from different vendors.

SDH/SONET opens up a multivendor, global market for communications systems, subsystems, and components. But to take advantage of this market manufacturers must test their products for compliance with the standards. Such compliance testing begins at what is called the physical layer, which is the electrical and optical signals, in the OSI seven-layer model.



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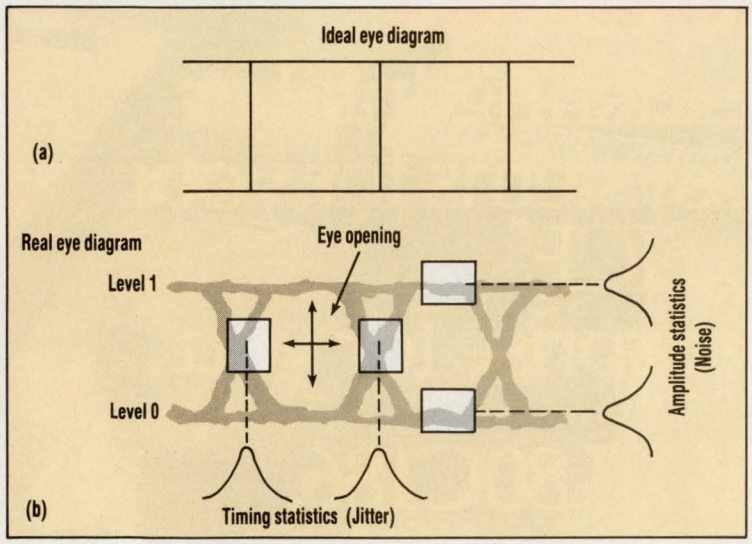

6. The eye diagram for ideal data pulses would be a series of boxes end-to-end (a). In a real-world eye diagram, variations in level amplitude and the transition crossing provide information about noise and jitter in the signal (b).

Similarly, jitter creates a finite error probability. Jitter can be caused by thermal effects in receivers, clock recovery drift, clock asynchronisity, and other effects that cause a timing-error probability for sampling the data. This probability is based on the width of the eye-pattern opening relative to the standard deviation of the signal's timing uncertainty. Therefore these statistics are used to determine the opening width of eye-pattern masks.

In summary, a large eye opening means the system has greater tolerance for amplitude and timing variations; a smaller opening means a smaller tolerance. Thus SDH/SONET eye-diagram masks offer a clear indication, based on waveform statistics, of transmitted signal quality. In addition, as is the case with pulse template testing, eye-diagram testing can also be automated with a digitizing oscilloscope. The process is more complicated, however, because eye-mask fitting is based on the statistics of multiple waveforms rather than on one stored pulse trace.

The most direct and valid way to fit the mask to the waveform is to use histogram distributions to define topline (100%) and baseline (0%) levels on the eye diagram. Similarly a histogram can be used to find the 50% crossing level. This information, along with standard mask data, can be used to compute and display the mask against the eye diagram. If no data waveform points fall into the mask region, the test is passed.

Histograms can also be computed at various locations on the eye diagram to measure jitter and noise distributions. This presumes, however, that the eye-diagram waveforms can be continuously acquired and stored in a statistical database. Only a few instruments have the amount of memory and processing power needed for this task. The Tektronix CSA 404 and 803 communication signal analyzers are such instruments.

Both instruments have a 256-by-512-point, 16-bit deep waveform statistics memory. This memory, along with dedicated statistical processing, allows the user to make histogram measurements anywhere on the eye diagram without having to reacquire data. Additionally, color grading of the eye-diagram display provides a quick, visual overview of trace statistics *(Fig. 2 again)*.

Because of its key role in compliance testing, the scope must be chosen carefully. Adequate bandwidth for the data rate involved is only one consideration. The scope should also be able to store masks and templates and automatically apply them to capture data. Other desired capabilities include statistical measurements, histograms, and automatic parameter measurements. Such automated mask and template testing capabilities will make FDDI and SDH/SONET compliance testing quick, easy, and comprehensive.

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Kevin Smith is the product manager for optical communications instruments in Tek's telecommunications products line. He received his B.S. in chemistry from Miami University in Oxford, Ohio and a Ph.D. in phyical chemistry from the University of Illinois in Urbana.

SDH/SONET SIGNAL HIERARCHY

Electrical signal	Optical signal	Data Rate (Mbps)	CCITT designation
STS-1	OC-1	51.84	STM-0**
STS-3	OC-3	155.52	STM-1
STS-9*	OC-9	466.56	
STS-12*	OC-12	622.08	STM-4
STS-18*	OC-18	933.12	
STS-24*	OC-24	1244.16	
STS-36*	OC-36	1866.24	
STS-48*	OC-48	2488.32	STM-16

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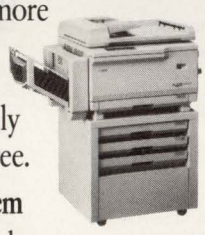

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CIRCLE 4

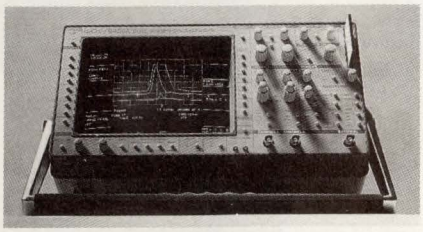
▼ PROTOCOL TESTER CHECKS LANS TO 2 MBITS/S

The HP PT502 is a 2-Mbit/s LAN interconnection protocol tester for switched multimegabit data service (SMDS) and frame-relay applications. The unit serves as a fast, high-performance test platform for SMDS monitoring and for the recently introduced HP IDACOM frame-relay software. Completely self-contained, the HP PT502 includes a color display, 7 to 11 Mbytes of internal memory, a 40-Mbyte hard-disk drive, and two 3.5-in. floppy-disk drives. The system permits real-time testing at full bandwidth for the T1/E1 (CEPT), fractional T1 and E1 (CEPT), or H0, H11, and H12 standards. Four interface configurations are available: T1/WAN, CEPT(E1)/WAN, WAN, and dual-port WAN. The V.35, V.36, and V.11/X.21 WAN ports are available. Prices for the HP PT502 range from $26,000 to $52,000, depending on the interface, software, and options selected. Delivery is within 6 weeks.

Hewlett-Packard Co.
19310 Pruneridge Ave.
Cupertino. CA 95014
(800) 752-0900
▶ **CIRCLE 661**

▼ MEMORY CARD INCLUDES TELECOM TEMPLATES

A memory card for a line of digital oscilloscopes stores 23 standard templates needed to test a broad range of telecommunications signals. The card, called the 94XX-MC-TC1, includes a complementary mask for each primary template, bringing the total to 46. The card works with LeCroy Models 9410, 9414, 9424, 9430, and 9450A oscilloscopes, which have a built-in memory card system. The templates are write-protected and take up about 190 kbytes on the 512-kbyte card, which complies with the Personal Computer Memory Card International Association standard. After a template is transferred to the oscilloscope's internal memory, the instrument's autosetup function selects the acquisition conditions to fit the waveform within the template. The 94XX-MC-TC1 card costs $700 and is available immediately.



LeCroy Corp.
700 Chestnut Ridge Rd.
Chestnut Ridge, NY 10977-6499
(914) 425-2000
▶ **CIRCLE 662**

▼ PROTOCOL DECODE KIT IS USER-DEFINABLE

The U Decode Tool Kit expands the FDDI decode capabilities of the Lanhawk 575X network analyzer beyond the Station Management, Media Access Control, DecNet, and InterNet protocols. The tool kit allows users to quickly add unique protocol decode capability to their standard Lanhawk 575X. As a result, they can decode virtually anything, including proprietary protocols, within the FDDI logical link layer. This capability allows greater troubleshooting flexibility and increased responsiveness. The U Decode Tool Kit costs $1000 and is available from stock. The Lanhawk 575X costs $28,000 to $50,000 depending on configuration. The Lanhawk 575X is available in 30 days.

Digital Technology Inc.
2300 Edwin C. Moses Blvd.
Dayton, OH 45408
(513) 443-0412
▶ **CIRCLE 663**

COMMUNICATIONS TEST EQUIPMENT MANUFACTURERS

American Reliance Inc.
7912 E. Baldwin Pl.
El Monte, CA 91731
(818) 575-5110
(DPG) (NWT)
CIRCLE 600

Analogic Corp.
8 Centennial Dr.
Peabody, MA 01961
(508) 977-3000
(DTA) (ISD) (JIG) (JIM)
CIRCLE 601

Anritsu Corp.
15 Thornton Rd.
Oakland, NJ 07436
(201) 337-1111
(BER) (BSA) (DTA) (DPG) (ISD) (LAN) (MOA) (NWT) (NOT) (OPM) (OTR) (OEC)
CIRCLE 602

B&K Precision
6470 W. Cortland St.
Chicago, IL 60635
(312) 889-1448
(BSA)
CIRCLE 603

Biomation Corp.
19050 Pruneridge Ave.
Cupertino, CA 95014
(408) 864-7777
(PRO)
CIRCLE 604

Boonton Electronics
791 Route 10
Randolph, NJ 07869
(201) 584-1077
(MOA) (TRA)
CIRCLE 605

Bytex Corp.
Southborough Office Park
120 Turnpike Rd.
Southborough, MA 01772-1886
(617) 661-7900
(LAN) (NWT) (PRO)
CIRCLE 606

Digital Technology Inc.
2300 Edwin C. Moses Blvd.
Dayton, OH 45408
(513) 443-0412
(NWT) (PRO)
CIRCLE 607

EIP Microwave Inc.
1589 Center Pointe Dr.
Milpitas, CA 95035
(800) 232-3471
(CSA) (FLO)
CIRCLE 608

GenRad Inc.
300 Baker Ave.
Concord, MA 01742
(508) 369-4400
(BER) (DTA) (ISD) (JIG) (JIM)
CIRCLE 609

Guide Technology Inc.
920 Saratoga Ave.
Suite 215
San Jose, CA 95129
(800) 288-4843
(MOA)
CIRCLE 610

Hewlett-Packard Co.
19310 Pruneridge Ave.
Cupertino, CA 95014
(800) 752-0900
(BER) (BSA) (CER) (CSA) (DTA) (DMT) (DPG) (DSA) (INT) (ISD) (JIG) (JIM) (LAN) (MOA) (NWT) (NOG) (NOT) (OTR) (PRO) (TRA)
CIRCLE 611

Interface Technology
196 University Pkwy.
Pomona, CA 91768
(714) 595-6030
(DPG)
CIRCLE 612

International Test Instruments
15550-B Rockford Blvd.
No. 100
Irvine, CA 92718
(714) 770-5711
(JIT) (TIA)
CIRCLE 613

LeCroy Corp.
Signal Sources Div.
700 Chestnut Ridge Rd.
Chestnut Ridge, NY 10977-6499
(800) 553-2769
(DPG)
CIRCLE 614

Marconi Instruments
3 Pearl Ct.
Allendale, NJ 07401
(201) 934-9050
(BSA) (CER) (CSA) (FLO) (MOA) (NOT)
CIRCLE 615

New Wave Instruments
128 W. 3100 N.
Provo, UT 84604
(801) 373-4909
(CER) (DPG)
CIRCLE 616

Pacific Electro Data
14 Hughes
Suite B-205
Irvine, CA 92718
(800) 676-2468 or (714) 770-3244
(PRO)
CIRCLE 617

Photon Kinetics Inc.
9405 S.W. Gemini Dr.
Beaverton, OR 97005
(503) 644-1960
(FLO) (NWT) (OTR)
CIRCLE 618

Protek Inc.
154 Veterans Dr.
Northvale, NJ 07647
(201) 767-7242
(BSA)
CIRCLE 619

Racal-Dana Instruments Inc.
Instruments Div.
4 Goodyear St.
Irvine, CA 92718
(714) 236-0400
(CER) (JIM) (MOA)
CIRCLE 620

(see p. 101 for key)
(continued on p. 101)

WE'VE GOT TWO WORDS FOR PEOPLE LIKE YOU.

FAX VOdem™ \faks-vō-dem\ *n* [origin: Yamaha LSI] **1**: world's first single-chip **multimedia communications device** **2**: Fax/data/ ADPCM voice and caller I.D. **3**: transfers data, fax and voice via a single line

If you're one of those people who goes around integrating communications devices into PCs, laptops and other hardware, we've got two words for you — FAX VOdem™.

What do they mean? In a word, plenty. Yamaha defined FAX VOdem on September 26,1991, as a major breakthrough in multimedia communications. And now it's going to change the way you communicate. Because with FAX VOdem, you'll be able to integrate Fax. Data. ADPCM voice communications. And caller I.D. All on a single line. And all with a single-chip LSI that'll give your products multimedia communications capabilities you never thought possible.

Sound too good to be true? It's not. And we'd like to prove it to you. Just fill out the coupon below and fax this ad to us at (408) 437-8791. We'll send you all the nitty gritty technical details that wouldn't fit in this ad. We'll even send you a FREE desk calendar that'll define FAX VOdem still more.

So start integrating FAX VOdem into your new products. And when your colleagues notice what a great communicator you've become, just tell them you've got two words for people like them.

Send me the details on FAX VOdem.™ And don't forget my desk calendar.

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Offer expires December 31, 1991. Good while supply lasts.

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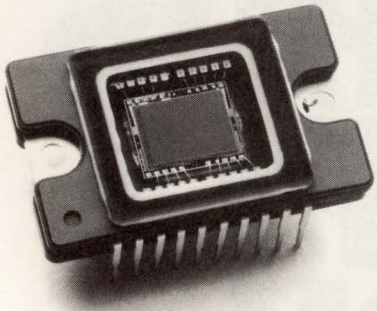
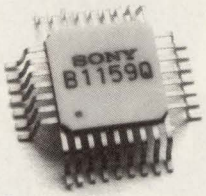
Systems Technology Division

CIRCLE 227 FOR U.S. RESPONSE CIRCLE 228 FOR RESPONSE OUTSIDE THE U.S.

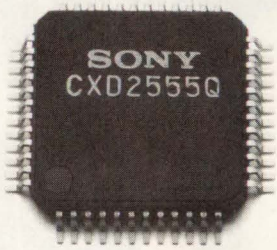
No guts.



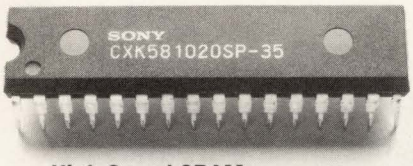
CCD Image Sensors
The CCD technology that led to Sony's leadership in color video cameras is now available to you.



ECL Standard Logic
Wide range of high-speed, high-performance ECL logic devices. Low cost and design simplicity.



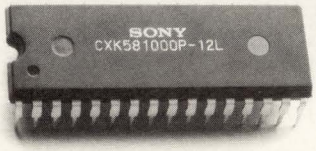
Digital Audio
Consumer-based leading-edge technology. Compact design. Small package. Capable of CD-ROM interface.



High Speed SRAMs
Broad family covers all your fast-processor, cache-memory requirements.

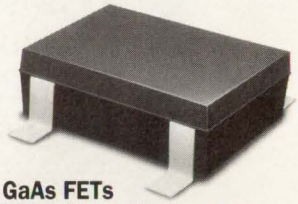
ECL Gate Arrays
Super high-speed operation combined with low power consumption and extensive I/O interfaces.

Interactive Video
Sony's A/V IC leadership applies directly to new multimedia systems. Superior bipolar linear technology in encoder/decoder.

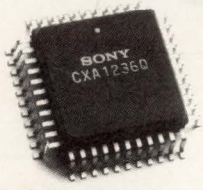


1-Meg SRAMs
Largest, most diverse family in the industry. The first products scheduled to come from our new San Antonio fab.

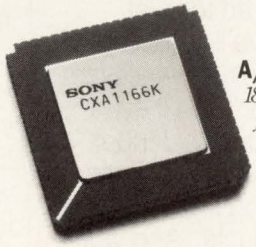
STRAM
High speed performance, self-timed RAM with register, synchronous SRAM.



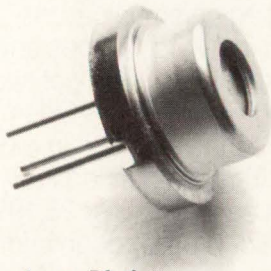
GaAs FETs
State-of-the-art performance, reliability and uniformity. Ideal when low noise is critical.



D/A Converters
High speeds to 500 MHz, low glitch energy, and low power consumption in very small packages.

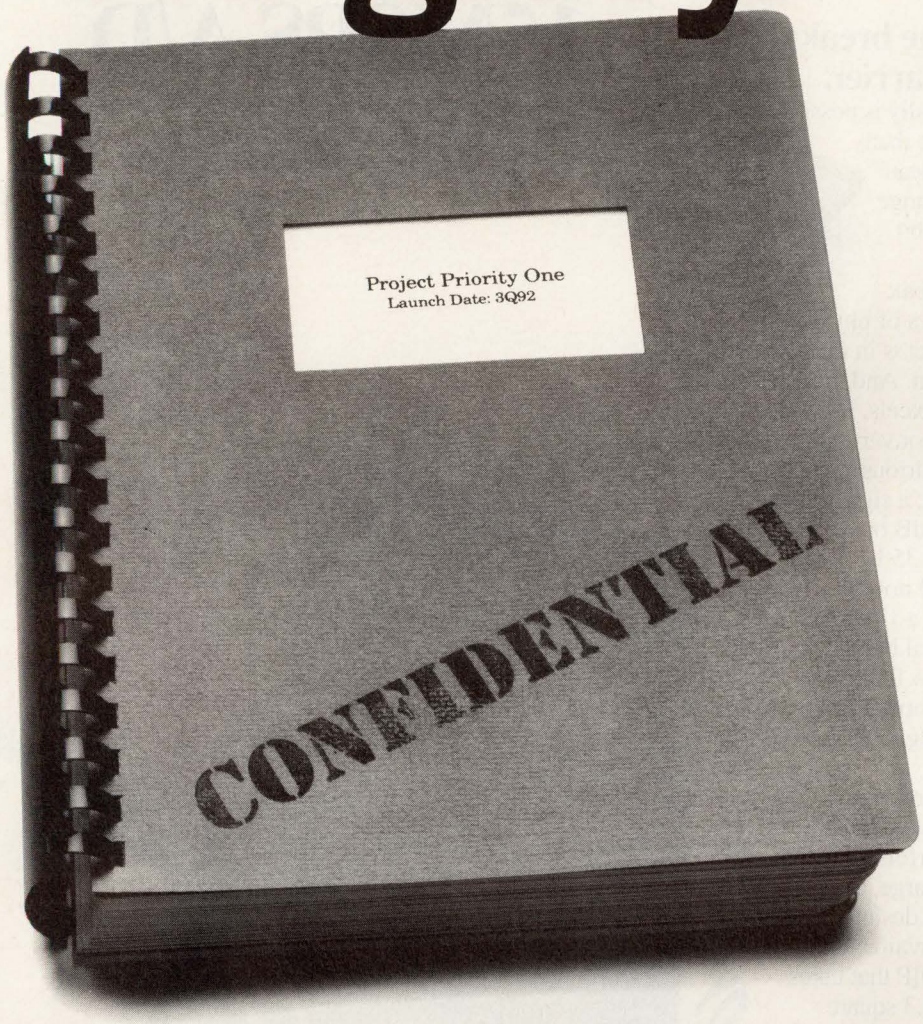


A/D Converters
18 models including the world's fastest. Fewer pins, smaller packages, low power consumption, and guaranteed low error rates.



Laser Diodes
Wide power range, high reliability, huge selection. Ideal for optical disk, laser printer and microsurgery designs.

No glory.



If you can't get the parts you need, you can't get your best designs out the door.

And that's where we can help. With cutting edge SRAMs—high and low speed. With high speed A/D and D/A converters. With high speed ECL logic chips. And with a long list of other components—the same components that have made Sony's consumer electronics so successful.

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To learn more about our custom design support, our competitive prices, and our full line of components, just call us today at (714) 229-4331 or (416) 499-1414 in Canada. You can even FAX us your current requirements at (714) 229-4285 or (416) 499-8290 in Canada.

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Sony Corporation of America, Component Products Company, 10833 Valley View Street, Cypress, CA 90630.
Sony Canada, 411 Gordon Baker Road, Willowdale, Ontario M2H 2S6.

CIRCLE 186 FOR U.S. RESPONSE **CIRCLE 187 FOR RESPONSE OUTSIDE THE U.S.**

Because you're thinking fast...

Off-the-chart performance in a new 12-bit, 15MSPS A/D converter.

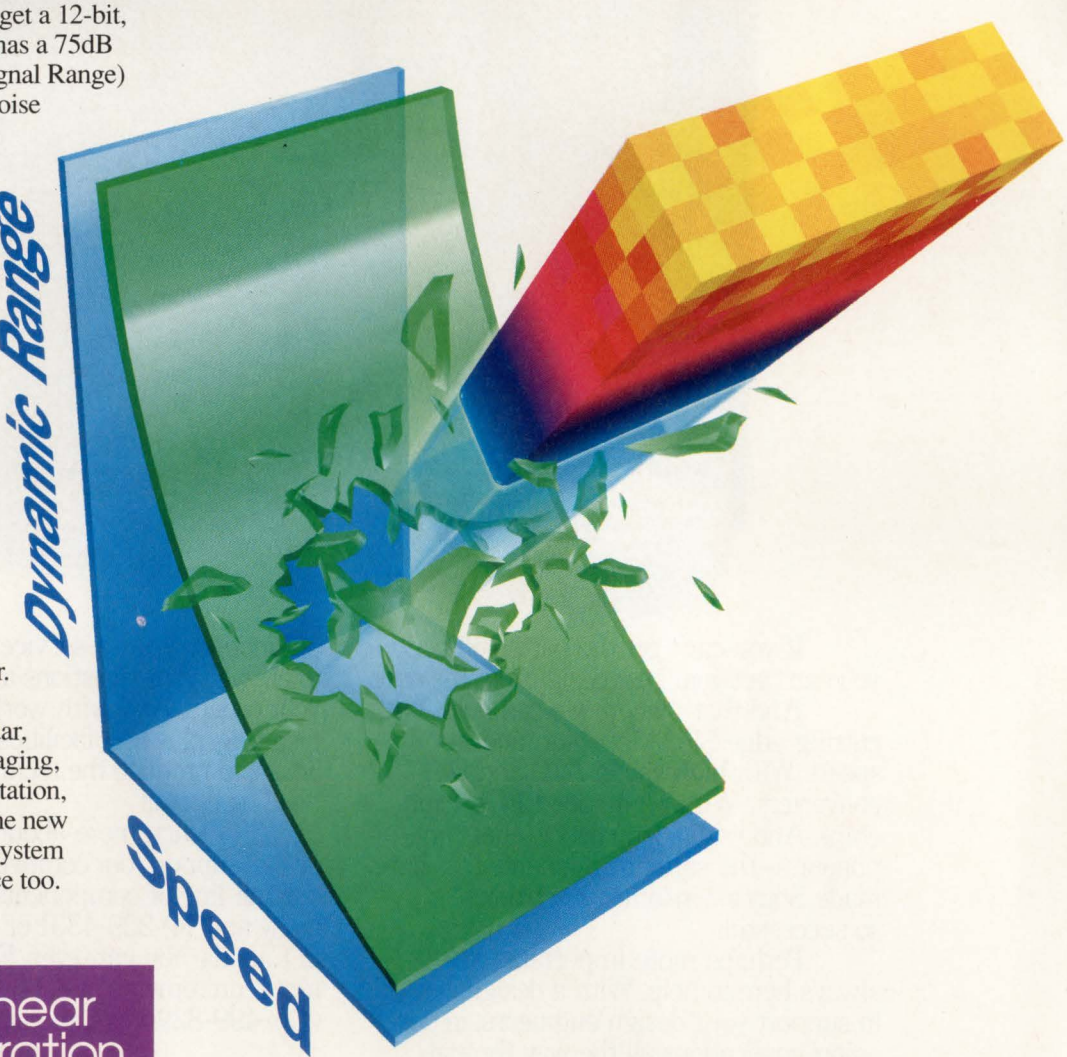
This one breaks the 74dB barrier.

Yes, it really is possible to get more than 74dB of "clean" dynamic range from a 12-bit converter... without breaking the laws of physics.

The secret is in the track-and-hold design. And that's where the CLC935 excels. So you get a 12-bit, 15MSPS converter that has a 75dB SFSR (Spurious Free Signal Range) at 7.5MHz, a signal-to-noise ratio of 67dB out to Nyquist, 0.35 LSB differential non-linearity, and a 135MHz small-signal bandwidth. Now that's a true performance breakthrough in an A/D.

Before now, the only way you could get this performance was with large, expensive board designs. Now, it's available in a 40-pin DIP that takes less than 2.3 square inches of board space. And only 5.2W of power.

So if you're bumping against A/D limits in radar, infrared and medical imaging, ultrasound, or instrumentation, call for details. Maybe the new CLC935 can give your system off-the-chart performance too.



Comlinear Corporation

Solutions with speed

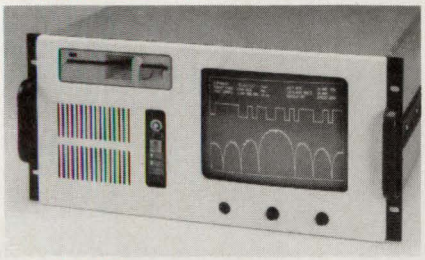
4800 Wheaton Drive
Fort Collins, CO 80525
(303) 226-0500
1-800-776-0500 (USA)

CIRCLE 114 FOR U.S. RESPONSE

CIRCLE 115 FOR RESPONSE OUTSIDE THE U.S.

▼ SPREAD-SPECTRUM UNIT TESTS COMM SYSTEMS

The LRS-200 spread-spectrum generator creates pseudorandom sequences for developing and testing spread-spectrum and conventional data-communication systems. The sequences are generated by a configurable 32-stage shift register using linear feedback. Operators can program the register length, feedback pattern, initial register contents, and the length of the linear recursive sequence, either manually using a soft menu on the display or via an optional IEEE-488 interface. Operating modes include BPSK, QPSK, GOLD/JPL, offset, and burst, with a maximum bit rate of 25 MHz. Semicustom configurations are available. The unit is housed in a rack-mount, IBM PC/AT-style computer with built-in display and comes with a rack-mount keyboard. The LRS-200's base price is $16,000. Delivery is from stock to 60 days.



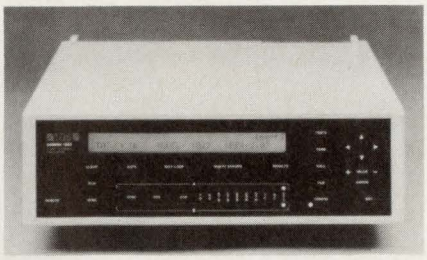
New Wave Instruments
128 W. 3100 N.
Provo, UT 84604
(801) 373-4909
▶ **CIRCLE 664**

▼ MULTITONE GENERATORS TEST LINEAR AMPS

A line of multitone RF signal generators simplifies intermodulation-distortion measurements of linear power amplifiers. Standard models available combine from 3 to 16 individual carriers into one output, providing a clean input signal for the amplifier under test. The generators can be ordered for rack mounting or as freestanding units. Versions are available for all popular frequency bands at prices starting at $5900. Delivery is in 6 to 12 weeks.

Teslatronics Inc.
1 Progress Blvd.
No. 25
Alachua, FL 32615
(904) 462-2010
▶ **CIRCLE 665**

▼ DUAL DATA ANALYZER TESTS MODEM RELIABILITY



Designers can test the call setup and handshake reliability of high-speed dialup modems with the Gemini 1022 dual-terminal emulator, Version 2.1. The unit has a call-connect reliability test feature that, when used with the company's Telephone Network Emulator, can ensure robust modem handshaking and data transmission under a variety of network conditions. This test is possible because the Gemini has two complete data analyzers, so the system can do the connect-reliability test while tracking modem responses and data transmission in real time. The unit also does standard bit-error-rate tests and polling tests. ROM files store standard test setups for industry-standard modems, and users can store their own tests in a nonvolatile RAM. Gemini Version 2.1 is available from stock for $5950. A software upgrade for older systems costs $750.

Telecom Analysis Systems Inc.
34 Industrial Way East
Eatontown, NJ 07724
(201) 544-8700
▶ **CIRCLE 666**

▼ VXIBUS WORD GENERATOR WORKS TO 50 MHZ

A C-size message-based VXIbus digital word generator creates 16 channels of 50-MHz data at 1-Hz resolution. The DG600VXI also features a memory depth of 16 kbits/channel. The memory is enhanced by tabling and timing simulator features that allow the module to generate iterative and mixed-timing data patterns. Each DG600VXI supports up to three 32-channel DG605VXI expansion modules. Halving the speed of the modules doubles their channel counts to 32 and 64, respectively. Additional features include cycle-to-cycle tristate control and a synchronized output strobe. The DG600VXI costs $5450 and the DG605VXI is priced at $2450. Both are available 8 to 10 weeks after ordering.

Interface Technology Inc.
2100 E. Alosta Ave.
Glendora, CA 91740
(818) 914-2741
▶ **CIRCLE 667**

COMMUNICATIONS TEST EQUIPMENT MANUFACTURERS

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433 N. 34th St.
Seattle, WA 98103
(206) 547-8311
(BSA) (DPG) (DSA)
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Lanham, MD 20706-4352
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CIRCLE 622

Sencore Electronics
Cable/Broadcast
3200 Sencore Dr.
Sioux Falls, SD 57107
(800) 736-2673
(CSA)
CIRCLE 623

Stanford Research Systems
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Sunnyvale, CA 94089
(408) 744-9040
(DPG) (DSA) (JIM) (NOG)
CIRCLE 624

Tekelec
26580 W. Agoura Blvd.
Calabasa, CA 91302
(800) 835-3532
(BER) (DTA) (ISD) (LAN)
(PRO) (TRA)
CIRCLE 625

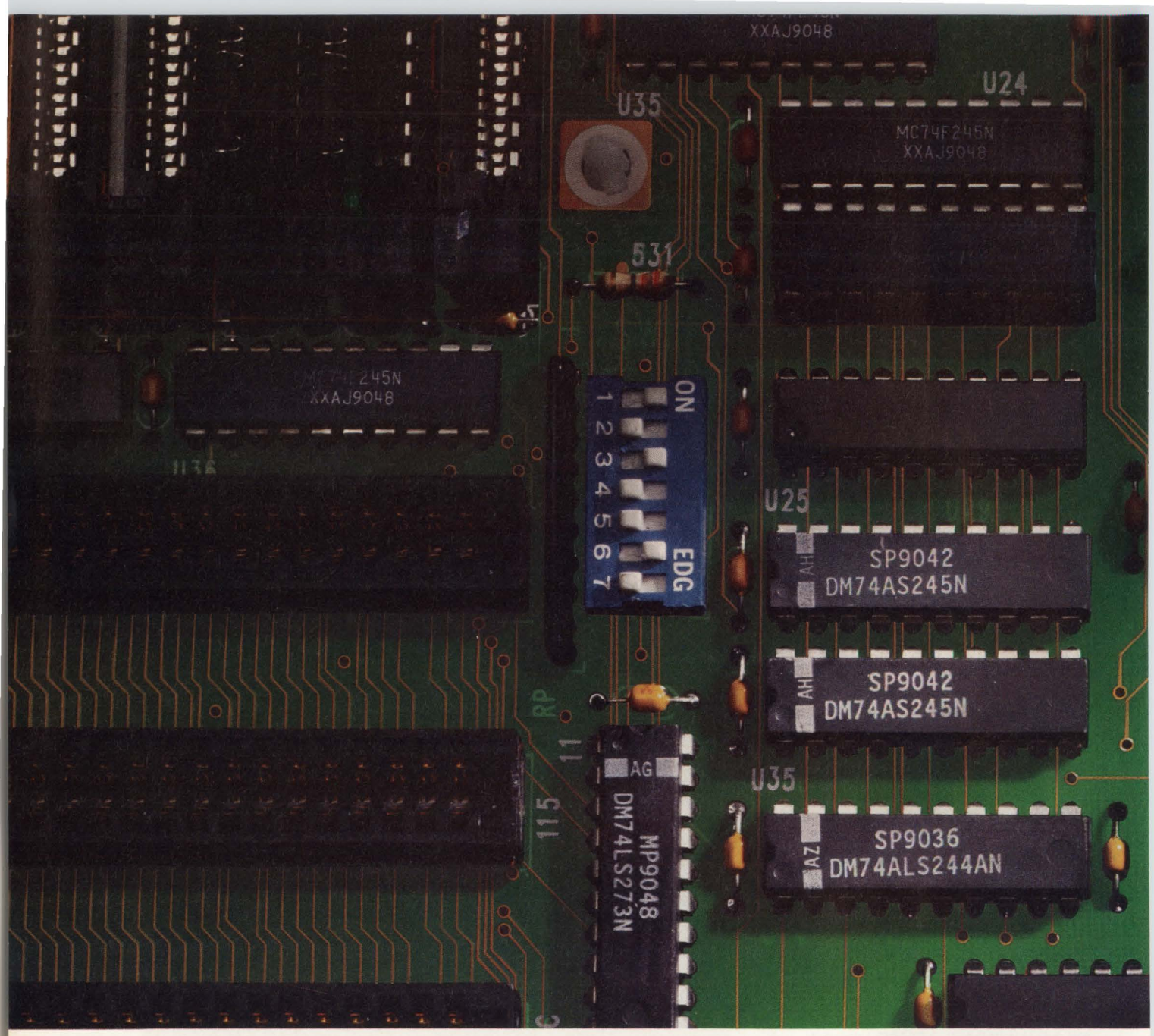
Tektronix Inc.
Telecommunications Product Line
P.O. Box 1520
Pittsfield, MA 01201
(800) 426-2200
(BER) (BSA) (CSA) (DPG)
(FLO) (ISD) (JIM) (MTR)
(OPM) (OTR) (OEC)
CIRCLE 626

Telecom Analysis Systems
34 Industrial Way E.
Eatontown, NJ 07729
(908) 544-8700
(BER) (DTA) (ISD) (JIM)
(NWT)
CIRCLE 627

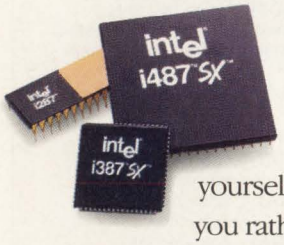
Wiltron Co.
490 Jarvis Dr.
Morgan Hill, CA 95037
(408) 778-2000
(DSA) (FLO) (NWT) (TDR)
CIRCLE 628

KEY

(BER) Bit-error-rate testers
(BSA) Broadband spectrum analyzers
(CER) Cellular radio test sets
(CSA) Communication signal analyzers
(DTA) Digital data transmission analyzers
(DMT) Digital modulation testers
(DPG) Digital pulse generators
(DSA) Dynamic signal analyzers
(FLO) Fault locators
(INT) Interference testers
(ISD) ISDN test equipment
(JIG) Jitter generators
(JIM) Jitter measurement
(LAN) LAN analyzers
(MTR) Metallic time-domain reflectometers
(MOA) Modulation analyzers
(NWT) Network test sets
(NOG) Noise generators
(NOT) Noise test sets
(OPM) Optical power meters
(OTR) Optical time-domain reflectometers
(OEC) Optical-to-electrical converters
(PRO) Protocol analyzers
(TDR) Time-domain reflectometers
(TIA) Time-interval analyzers
(TRA) Transmission analyzers

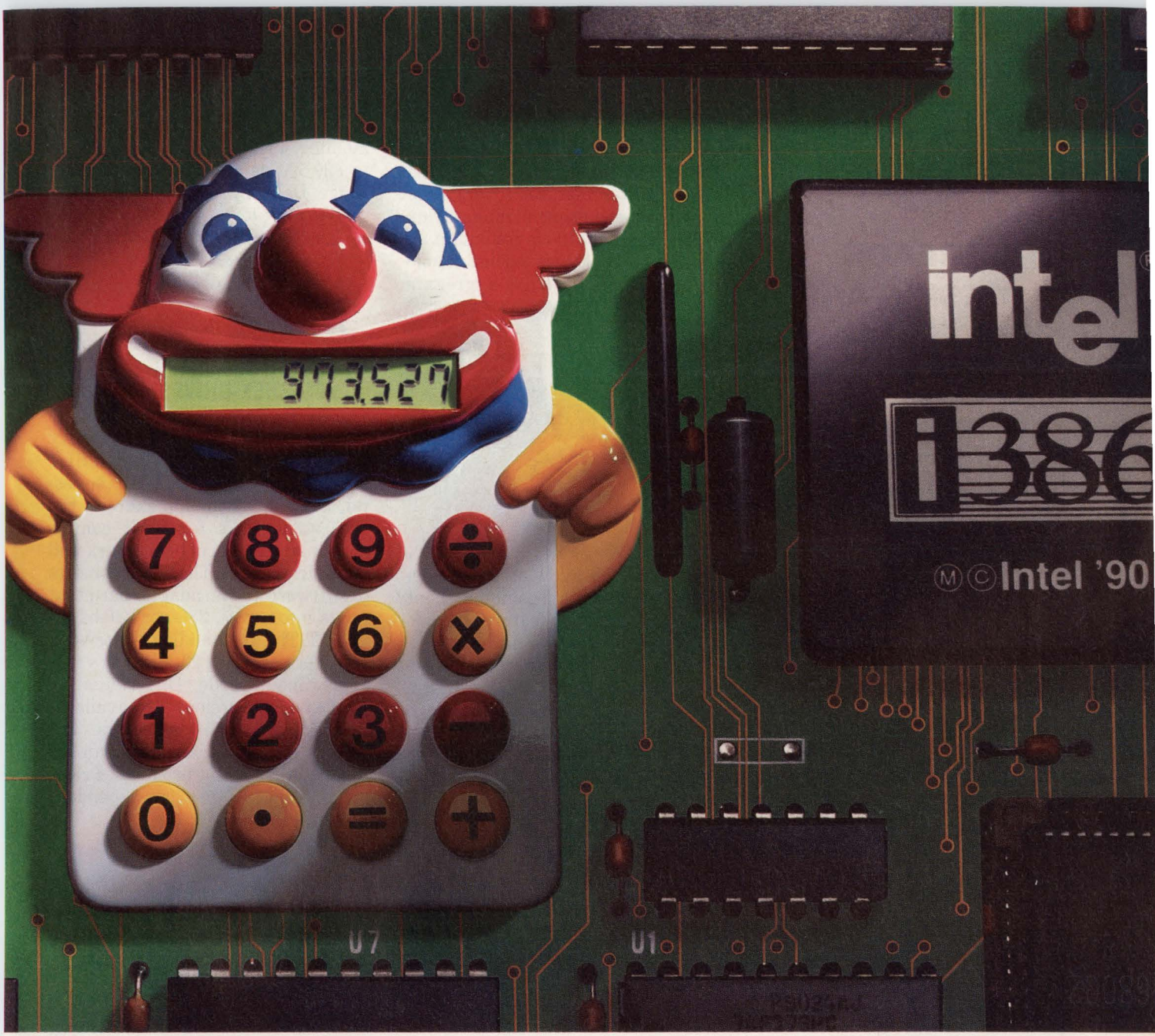


Ask for genuine Intel or who knows what yo



If you need a math coprocessor to speed your power applications, ask yourself this question: Which would you rather have sitting next to your Intel microprocessor — an Intel Math CoProcessor or something you may know nothing about? Because if you don't specify Intel, that's basically what you're getting — a big question mark. With Intel, however, there's simply no question. You're getting quality.

That's because Intel has the longest track record with math coprocessors. In fact, we've manufactured



Math CoProcessors, u'll have to count on.

and sold millions more than all the others combined. And we've tested every one of them with the most exhaustive battery of tests in the industry. All to assure you absolute reliability.

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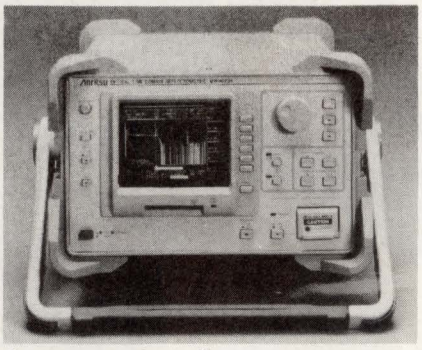
The Computer Inside.™

CIRCLE 1

COMMUNICATIONS TEST

▼ OTDR HAS WIDE DYNAMIC RANGE, DEEP MEMORY

The MW9040A optical time-domain reflectometer features a very wide dynamic measurement range of up to 250 km with a 10-cm resolution. In addition, a 25,000-wavepoint memory and fast full-range aggregate



data averaging allow users to zoom in on any arbitrary position without reaveraging. Other features include one-touch selection of several functions, such as auto-splice measurement, auto-attenuation, waveform comparison, and file handling. Softkey labels are displayed on the right-hand side of the CRT screen. The MW9040A comes with a GPIB input that's compatible with IEEE-488.2. The unit conforms to military specification MIL-T-28800C, Class 3, Style C. Prices range from $23,600 to $38,400, depending on options, and delivery is in 8 weeks.

Anritsu
15 Thornton Rd.
Oakland, NJ 07436
(201) 337-1111
▶ CIRCLE 668

▼ SYSTEM COMBINES SWEPT SOURCE, ANALYZER

By integrating an advanced scalar network analyzer with a built-in swept microwave source, the 5400A scalar measurement system offers the stability and accuracy of a synthesized sweeper for the cost of a typical analyzer-sweep-generator combination. Six models cover a wide frequency range: 10 MHz-8.4 GHz, 2 to 8.4 GHz, 8 to 12.4 GHz, 10 to 16 GHz, 12.4 to 20 GHz, and 17 to 26.5 GHz. Features include a 71-dB dynamic range, smoothing, averaging markers and cursors, trace memory, complex limit testing, custom X-axis capabilities, and buffered printer and plotter outputs. The built-in monochrome display is complemented by an output for an external VGA monitor. Prices range from $14,580 to $20,520 depending on frequency range. Delivery is in 4 weeks.

Wiltron Co.
Microwave Measurements Div.
490 Jarvis Dr.
Morgan Hill, CA 95037
(408) 778-2000
▶ CIRCLE 669

▼ TESTER QUALIFIES SCSI DISK DRIVES

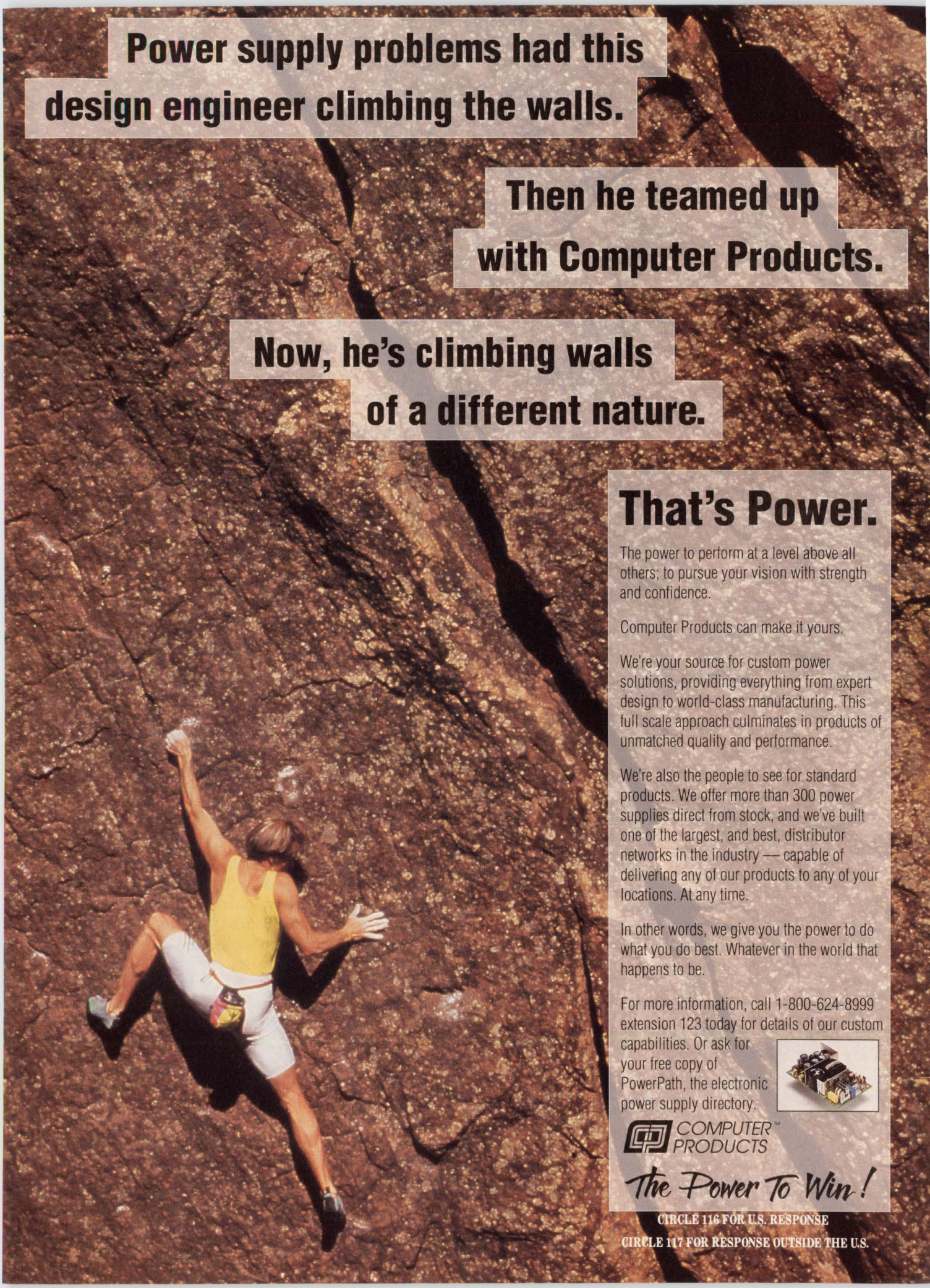
The AWS series disk testers can be easily programmed to test a variety of functions for qualifying SCSI 1 and SCSI 2 disk drives. With the tester, users can scan and exercise the bus, audit disks for SCSI conformance, and perform benchmark and reliability checks. The tester consists of software and an adapter card that plugs into a 286-, 386-, or 486-based PC/AT. The unit handles 2-byte-wide transfers at up to 20 Mbytes/s in a synchronous mode. Differential or single-ended versions are available with 50- or 68-pin connectors. The testers are also available as an option on other Ancot products. Prices range from $900 to $3900 depending on configuration.

Ancot Corp.
115 Constitution Dr.
Menlo Park, CA 94025
(415) 322-5322
▶ CIRCLE 670

▼ VXI MODULE SIMULATES DIGITAL INTERFACES

The Model BE-64 bus emulator/word-generator module bring full bus-emulation capabilities to VXI-based test systems. The one-slot C-size module can simulate any digital interface, including custom interfaces. Features include 52 timing and control signals running at 50 MHz, 64 bidirectional data channels running at 25 MHz, a 32-kbyte memory, and 24 programmed set/sense lines. The unit offers multiple timing sets, multiple tables, and multiple looping. It uses message-based macrocommands. The BE-64 costs $12,000, with delivery within 8 to 10 weeks.

Talon Instruments
150 E. Arrow Hwy.
San Dimas, CA 91773
(714) 599-0690
▶ CIRCLE 671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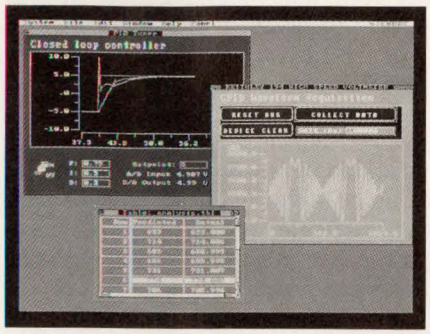
▼ DATA ACQUISITION SOFTWARE ENHANCED

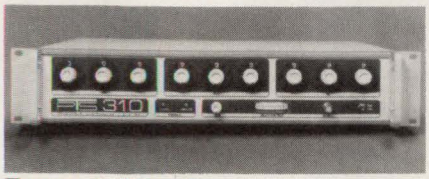
IEEE-488 and RS-232 instrument interfacing have been added to Version 2.0 of Viewdac, which is a comprehensive data acquisition, analysis, and graphics software package for 386- and 486-based PCs. The new release also adds an external language interface, Lotus 1-2-3 file I/O capa-



bilities, and graphics outputs for HPGL and PostScript printers. All features are integrated in a multitasking, windowing environment. Users set up applications by selecting items from lists and answering prompts from menus, rather than writing code. The external language interface makes it easy to import custom analysis routines written in C or assembly language into the system. Viewdac 2.0 is available for immediate shipment at a price of $2495, which includes 90 days of telephone technical support.

Asyst Software Technologies Inc.
100 Corporate Woods
Rochester, NY 14623
(800 348-0033 or (716) 272-0070
▶ CIRCLE 672

▼ LOW-NOISE SYNTHESIZER OFFERS FAST SWITCHING

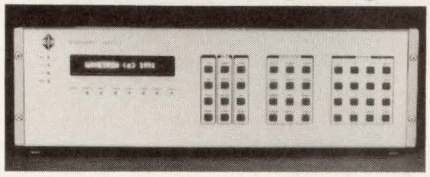


Fast switching times and a low-noise output make the PTS 310 ideal for applications requiring a broadband signal source. The frequency synthesizer combines direct analog and direct digital synthesis technologies to cover 0.1 to 310 MHz with a 1-Hz resolution (0.1 Hz is optional). Switching times range from 1 to 20 μs, depending on frequency, and switching is phase-continuous. Two models are available. The type 1 features 65-dB spurious suppression and the type 2 has 60-dB suppression. Both occupy only 3.5 in. of rack space. OEM versions are also available for integration into OEM systems. The PTS 310 type 1 costs $5650 and the type 2 costs $5100. OEM versions go for $300 less. Delivery is in 60 days.

Programmed Test Sources Inc.
9 Beaver Brook Rd.
Littleton, MA 01460
(508) 486-3008
▶ CIRCLE 673

▼ DSP SYSTEM RUNS AT UP TO 80 MIPS

A general-purpose digital-signal-processing system, the DSPS-2601, performs complex-signal-processing tasks at up to 80 MIPS in a mixed-signal environment. Each system consists of a mainframe and up to eight field-installable digital-signal-

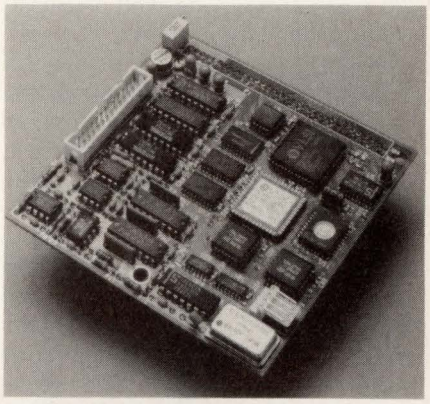


processing modules. A range of performance specifications are available, but each module includes analog signal conditioning, a variable anti-alias filter, and a precision, high-speed analog-to-digital converter. Users can invoke up to eight applications programs per installed channel by pressing a key. Typical applications include real-time data acquisition, FFT spectrum analysis, real-time phase and frequency analysis, and arbitrary waveform generation. A one-channel unit costs $3500 and each additional channel costs $1000. Delivery is in 2 to 4 weeks.

Wavetron Microsystems
800 El Camino Real West
Mountain View, CA 94040
(415) 903-2267
▶ CIRCLE 674

▼ 16-BIT A-D MODULE OFFERS 16 CHANNELS

The PCI-20364M-1 high-accuracy analog-input module offers 8 differential or 16 single-ended input channels with up to 18 bits of measurement resolution. The maximum sampling rate is 500 Hz at 12-bit resolution, 50 Hz at 16 bits, and 12.5 Hz at 18 bits. All options are software programmable. No jumpers or switches are needed. In addition to internal auto-calibration, the converter board allows auto-calibration with user-defined external signals. And unlike converters with standard unipolar



ranges that abruptly stop responding at 0 and full scale, the PCI-20364M-1 has ±20% over-range capability. The converter works with all the company's PCI carriers and multifunction I/O boards that accept plug-in modules. It's available for immediate delivery at a price of $595.

Intelligent Instrumentation
1141 Grant Rd.
MS 131
Tucson, AZ 85705
(602) 623-9801
▶ CIRCLE 675

▼ REAL-TIME EMULATOR HANDLES 8XC196MC

The AN196-MC real-time emulator supports Intel's 8XC196MC motor-control microcontroller with full-speed, no-wait-state emulation. The unit emulates all of the device's memory configurations, including ports 3, 4, and 5, and performs ROM emulation with or without additional external memory. The real-time-trace facility stores up to 16,384 processor states. Trace and processor execution can be controlled by defined bus activity (address, data, or cycle type), processor I/O pin states or transitions, external test equipment, or a sequence of these factors. Both symbolic debugging and display of source code are possible. The AN196-MC costs $8999.

Annapolis Micro Systems Inc.
190 Admiral Cochrane Dr.
Suite 130
Annapolis, MD 21401
(301) 841-2514
▶ CIRCLE 676

TEST & MEASUREMENT PRODUCTS

▼ VISUAL SOFTWARE ENVIRONMENT ENHANCED

The latest version of the HP VEE-Engine and HP VEE-Test visual engineering-environment software runs on the HP Apollo 9000 Series 700 workstations, as well as Series 300 and 400 workstations. The software supports HP-UX Versions 7.X through 8.0 on an X-Window system. Also, 25 drivers for HP instruments have been added to HP VEE-Test, which is specifically intended for instrument control. Thirty on-line software examples have been added to the packages to help users learn their operation. HP VEE-Engine and HP VEE-Test let users perform engineering tasks by linking icons rather than writing code. They're designed for a broad range of computer-aided applications. HP VEE-Engine costs $995, and HP VEE-Test costs $5000. Delivery is in 4 weeks.

Hewlett-Packard Co.
19310 Pruneridge Ave.
Cupertino. CA 95014
(800) 752-0900
▶ CIRCLE 677

▼ FLEXIBILITY HIGHLIGHTS ARBITRARY GENERATOR

A library of 20 standard functions, two graphical editing techniques, and an optional waveform sequence generator make the Model 2411A arbitrary waveform generator easy to use. The generator features a waveform sampling rate of 0.1 Hz to 2 MHz, 16-bit resolution, and 64 kwords of battery-backed waveform memory. The waveform sequence generator permits different waveform segments to be repeated by looping them the required number of times and then linking them to another waveform. The sequence can be built from a library of up to 100 segments. Sequence programming can have 1000 segments, and a maximum of 100 sequences can be stored in memory. The 2411A costs $2495, and the waveform sequence generator goes for $895. Delivery is from stock.

Pragmatic Instruments Inc.
7313 Carroll Rd.
San Diego, CA 92121-2319
(619) 271-6770
▶ CIRCLE 678

▼ 400-MHz DSOs ARE FULLY PROGRAMMABLE

The 4060 series digital storage oscilloscopes offer 400-Msample/s sampling, 150-MHz bandwidth, and 8-bit vertical resolution. Two scopes are available: the 2-channel 4062 and the 4-channel 4064. The latter lets users view all channels simultaneously and provides identical control over all four input signals. Both scopes are fully programmable and have 16 nonvolatile waveform memories, on-screen signal measurement and analysis functions, and optional internal thermal printers or four-color plotters. The scopes' 7-in. display incorporates an electronically generated graticule for parallax-free measurements. IEEE-488.2 and RS-232C interfaces are included. Prices for the 4060 series start at $5200, with delivery within 30 days.

Gould Inc.
Test and Measurement Group
8333 Rockside Rd.
Valley View, OH 44125
(216) 328-7263
▶ CIRCLE 679

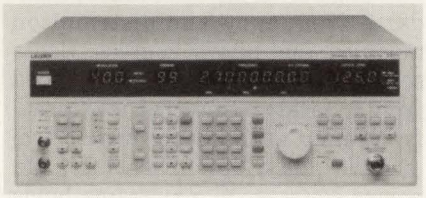
▼ LOW-COST BOARD TEST PACKAGE SUPPORTS 1149.1

The GR227X Essential Test Collection (ETC) is a low-cost, full-featured manufacturing board test and diagnostic solution. The ETC supports the entire test process, from design through manufacturing test, with the addition of information software for quality improvement programs. The system consists of an expanded GR2275 or GR2276 board test system, the new BasicSCAN test software, the PC-based Test Palette software with TestFlo Manager, an IEEE interface kit, and Remote Tester Support, a modem-based system for remote access. The software offers automated test generation and allows the hardware to test boards with IEEE-1149.1 boundary-scan devices. GR227X ETC prices start at $86,900 for a typical configuration. Delivery is within 6 weeks.

GenRad Inc.
300 Baker Ave.
Concord, MA 01742-2174
(508) 369-4400
▶ **CIRCLE 680**

▼ SYNTHESIZED GENERATOR WORKS TO 2.7 GHz

A synthesized signal generator, the Model 3221, delivers frequency accuracy within 0.05 ppm and SSB phase noise of less than 120 dBc to 2.7 GHz. The unit's modulation capabilities include seven modes (pulse, logic, DC-FM, and internal and external AM



and FM) with 14 simultaneous combination modulation modes. Users can select between dBm and dBμ for output units, with 0.1-dB resolution. Three presets are included for commonly used RF output levels. In addition, 100 preset memories store complete front-panel settings. An IEEE-488 interface and a GaAs FET pulse modulator are standard. The Model 3221 costs $12,300 and delivery is from stock.

Leader Instruments Corp.
380 Oser Ave.
Hauppauge, NY 11788
(800) 645-5104 or (516) 231-6900
▶ **CIRCLE 681**

▼ LOGIC-ANALYZER OPTION TESTS BOUNDARY SCAN

Board designers using boundary-scan techniques can debug their prototypes with the PM 8660/30, which is an automatic test-program generator and boundary-scan option for the PF 3580-series logic analyzers. The package tests for opens, shorts, and bridges, and also supports cluster testing. Thus, engineers can quickly locate process faults on their prototypes. The package is one of a series of products that provide quick solutions to the test-access needs of engineers using the latest ICs and pc-board technology. The PF 8660/30 boundary scan kit costs $19,800.

John Fluke Mfg. Co. Inc.
P.O. Box 9090
Everett, WA 98206-9090
(206) 347-6100
▶ **CIRCLE 682**

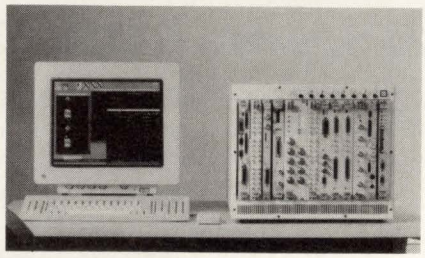
TEST & MEASUREMENT PRODUCTS

▼ MODULAR TIME-FREQUENCY SYSTEM IS VERSATILE

With its many choices of inputs and outputs, the Model 9480 modular time and frequency system can be configured for a wide range of applications, from an uncomplicated distribution system to a stand-alone frequency standard. The system's basic building blocks are a frequency standard, frequency and distribution modules, and power sources. Users select the components they need from a variety of internal or external frequency standards, output frequencies, distribution schemes, and power sources. A mainframe holds up to eight modules, each with up to five outputs. Multiple mainframes can be connected together. Prices depend on configuration, but a system with 40 outputs and an ovenized crystal oscillator costs $6545. Delivery is in 8 weeks.

Racal-Dana Instruments Inc.
4 Goodyear St.
Irvine, CA 92718
(800) 722-3262
▶ **CIRCLE 683**

▼ VXI-BASED SYSTEM OFFERS REAL-TIME PROCESSING



The S760VXI is a VXIbus application-specific core test architecture. The system's dual-processor design permits distributing processing capability for real-time execution and control of the user-selected VXI instrumentation. For maximum efficiency and throughput, the system includes two operating systems, Unix and VxWorks, so each can do the tasks for which it is best suited. The S760VXI comes with a unified, customizable test-development framework called Computer-Aided Test Engineering (CATE). A newly added tool is Instrument Workbench, an object-oriented graphical environment for managing, programming, and debugging VXIbus and GPIB instruments. S760VXI systems start at less than $75,000, with delivery in 60 to 120 days.

Schlumberger Technologies
ATE Div.
1601 Technology Dr.
San Jose, CA 95110-1397
(408) 437-5129
▶ **CIRCLE 684**

▼ HANDHELD COUNTER WORKS TO 2.4 GHz

A handheld frequency detector-counter features 10-mV sensitivity up to 900 MHz and 8-digit resolution to 2.4 GHz. The dynamic range of the Model 2300 Handi-Counter is 1 MHz to 2.4 GHz. A convenient display-hold switch retains the last reading. An optional 600 mA-hr NiCad battery pack is available. State-of-the-art techniques contribute to the counter's small size and low price. The unit employs two ICs: a one-chip CMOS frequency counter and an ECL-based frequency scaler. The input circuitry uses dual high-performance MMIC amplifiers. The Model 2300 costs $99 and is available from stock. The battery pack costs $29.

Optoelectronics Inc.
5821 N.E. 14th St.
Fort Lauderdale, FL 33334
(800) 327-5912 or (305) 771-2050
▶ **CIRCLE 685**

▼ ACTIVE PROBE BOASTS 750-MHz BANDWIDTH

A 750-MHz bandwidth, less than 2 pF of input capacitance, and a 1-MΩ input resistance, make the P6205 active FET probe ideal for testing high-speed digital circuitry. Additionally, the probe's ±10-V linear dynamic range allows access to most logic families using standard logic levels. The 10X attenuation readout reduces confusion and measurement errors. The probe was designed for use with the Tektronix CSA, DSA, TDS, and 11000-series oscilloscopes, from which it draws the needed power. However, the optional Tektronix 1103 Tekprobe power supply allows two P6205s to work with any 50-Ω or 1-MΩ scope using conventional BNC connectors. The P6205 active FET probe costs $495 and is available within 5 weeks after ordering.

Tektronix Inc.
P.O. Box 1520
Pittsfield, MA 01201
(800) 426-2200
▶ **CIRCLE 686**

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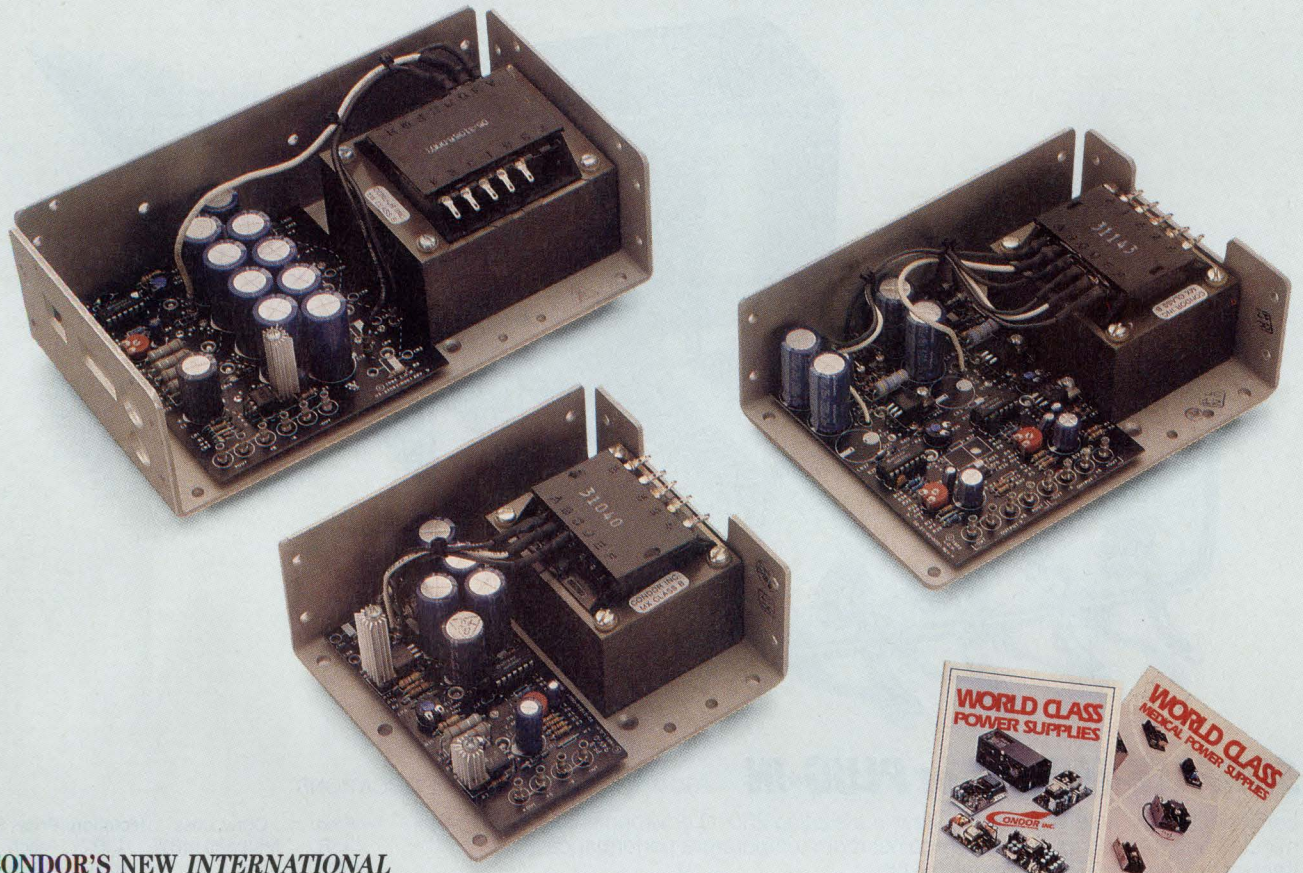

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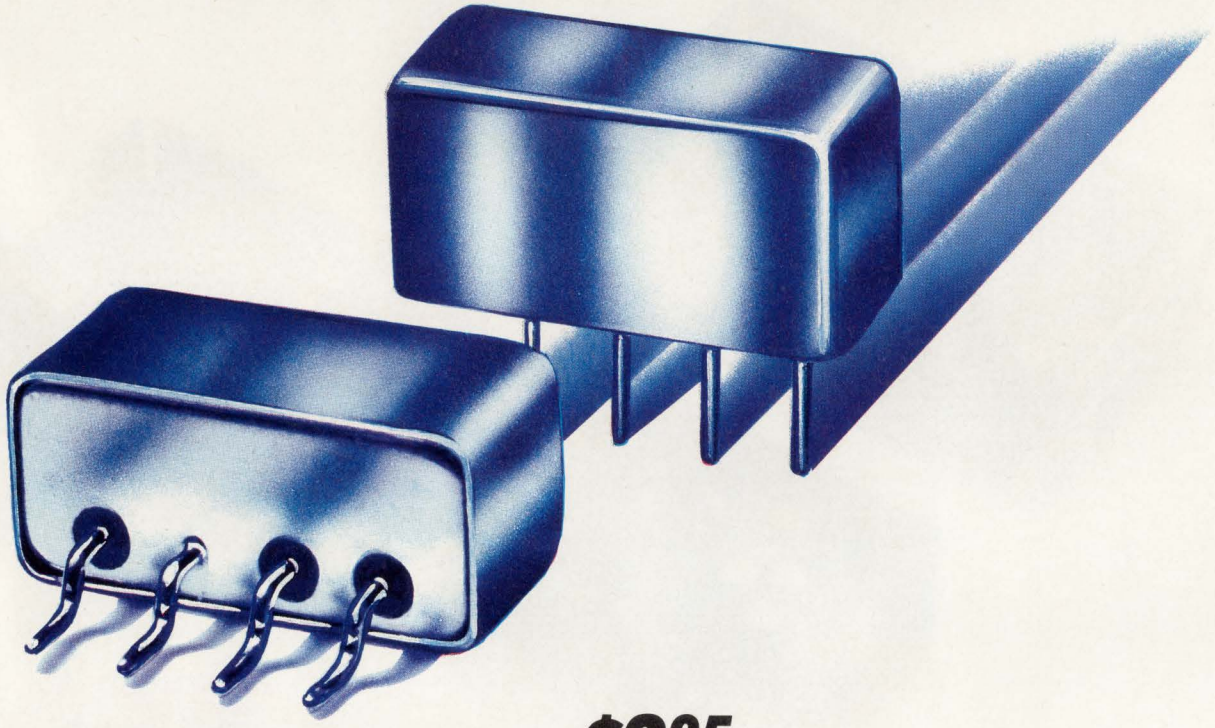
ALL-WELDED 0.15-1500MHz



SURFACE-MOUNT or PLUG-IN

FROM $3.95 (10 qty)

Let Mini-Circuits' new TUF-mixers stew in a sizzling 250°C environment for five minutes and then compare specs against room temperature performance... no trace of degradation. That's a tough mixer!

TUF-mixer components can take the extreme shock and vibration stresses of MIL-STD-28837 as well as more than 200 cycles of thermal shock ranging from -55° to +100°C; the Ultra-Rel diodes used can withstand 168 hours at 300°C.

Performance features include very low conversion loss (flat over the entire band), high isolation (LO-RF, LO-IF), and well-matched VSWR at all ports. A fully-detailed database on all performance characteristics is available, along with an experienced application staff to guide users upon request.

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Tough, tiny, and with tight repeatability... Mini-Circuits' Ultra-Rel™ TUF-mixers, with a 5-yr. guarantee, priced from $3.95... only from Mini-Circuits.

SPECIFICATIONS

Model	Freq. L-R (MHz)	Conv. Loss Midband (dB) $\bar{X}$	δ	Isolation L-R (dB)	Price, $ each (10 qty)
TUF-3 TUF-3SM	0.15-400	4.7	.02	46	5.95
TUF-1 TUF-1SM	2-600	5.9	.04	42	3.95
TUF-2 TUF-2SM	50-1000	5.9	.07	47	4.95
TUF-5 TUF-5SM	20-1500	5.7	.04	42	8.95

$\bar{X}$ = mean δ = deviation

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F145 REV. C

CIRCLE 160 FOR U.S. RESPONSE

CIRCLE 161 FOR RESPONSE OUTSIDE THE U.S.

CIRCLE 521 VARY CAPACITANCE TO POSITIVE OR NEGATIVE

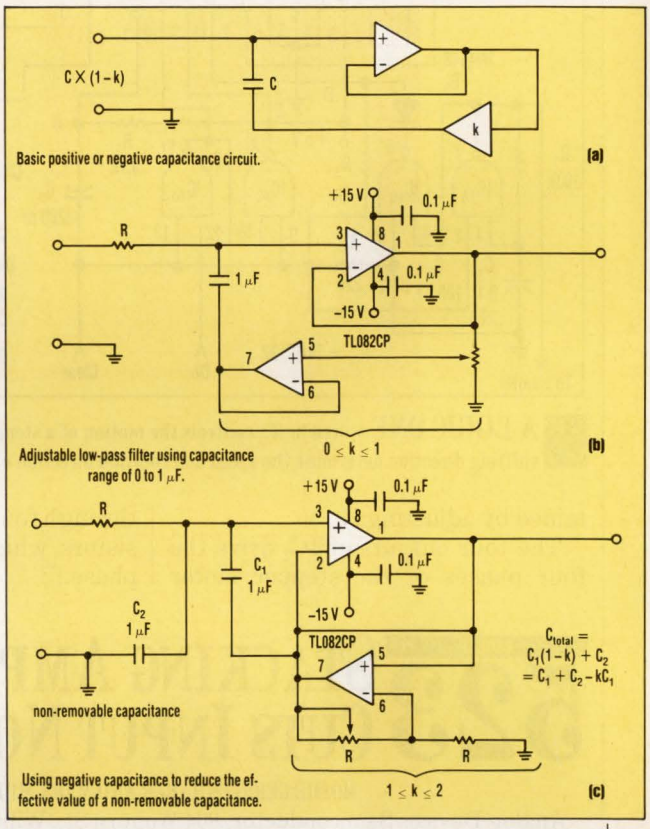
JOHN DUNN
181 Marion Ave., Merrick, NY 11566.

There are at least two reasons to use this basic circuit whose equivalent capacitance can be made positive or negative *(Fig. 1a)*. First, variable capacitances can be obtained in value ranges not readily available in physical structures. Second, an existing shunt capacitance can be made adjustable either above or below its existing value.

The circuit's equivalent capacitance is $C \times (1 - k)$, where k is adjustable. The effective capacitance is varied by adjusting k. Consider a simple low-pass filter *(Fig. 1b)*. If C = 1.0 μF, adjusting k from 1 to 0 gives a 0- to 1.0-μF variable capacitance, effectively varying the filter's cutoff frequency. When k is greater than one, a negative capacitance is obtained. Thus, if a circuit has a large, unwanted, and nonremovable capacitance to ground, that capacitance could be reduced by paralleling it with an adjustable negative capacitance *(Fig. 1c)*. As before, if $C_1 = 1.0$ μF, adjusting k from 1 to 2 gives a 0- to –1.0-μF capacitance.

The absolute value of the negative capacitance shouldn't be greater than the positive value being paralleled or the circuit will oscillate.□

1. THE equivalent capacitance of this circuit can be made positive or negative by varying k (a). By setting k from 1 to 0, a variable capacitance of 0 to 1 μF is obtained. This varies the cutoff frequency of a simple low-pass filter (b). Non-removable capacitance can be reduced by paralleling it with an adjustable negative capacitance (c).



CIRCLE 522 DRIVERS FOR STEPPER MOTORS GET SIMPLER

YONGPING XIA
Dept. of Electrical and Computer Engineering, West Virginia Univ., Morgantown, WV 26506-6101.

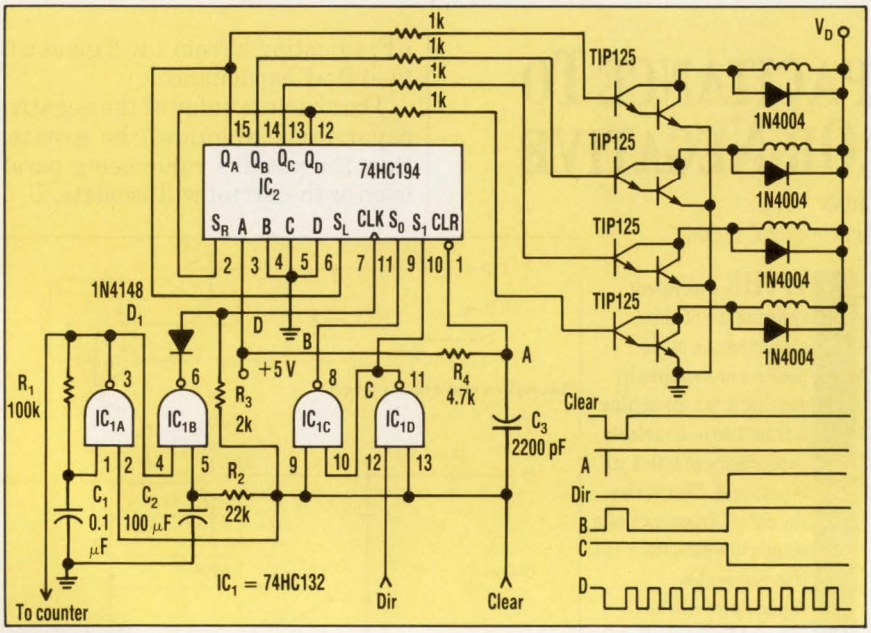
This design for a stepper-motor driver was inspired by two previously published circuit designs (ELECTRONIC DESIGN, *May 10, 1990, p. 103, and May 23, 1991, p. 120)*. Simpler than its predecessors, it uses only two common integrated circuits, yet contains its own clock generator.

The heart of the driver is a 74HC194 4-bit bidirectional shift register, IC_2, which assigns the motor steps *(see the schematic diagram)*. The register shifts either left or right depending on its S_0 and S_1 inputs. When $S_0 = 0$ and $S_1 = 1$, it is a left shift register. If the signals are reversed, so is the shifting direction. The shift left (S_L) and shift right (S_R) inputs are connected to Q_A and Q_D, respectively.

Thus, if a logic ONE is somehow stored in the register, it can be shifted right or left by the clock. At any time there is one and only one active phase, and its shifting direction determines the motor direction.

The trick is to insert the logic ONE into the shift register. That is accomplished by the Clear signal, with capacitor C_3 and resistor R_4, which form a differentiator. When the Clear signal goes from high to low *(see the timing diagram)*, the differentiator produces a narrow negative pulse at Point A to reset IC_2. As the Clear signal remains low, points B and C are kept high, which sets IC_2 into Load mode. Then the low-to-high jump of the Clear signal acts as an extra clock pulse, loading a ONE into input A of IC_2. Because inputs B, C, and D are tied to ground and thus constrained to be ZEROs, the required single ONE is thus loaded.

With the Clear signal high, the clock generator formed by NAND gate IC_{1A}, resistor R_1, and capacitor C_1 begins to work. The motor speed is controlled by the clock frequency, hence the desired speed can be ob-



A LOGIC ONE stored in IC_2 controls the motion of a stepper motor. Its speed and shifting direction determine the speed and rotation direction of the motor.

tained by adjusting R_1.

The four outputs of IC_2 drive the four phases of the stepper motor through four Darlington power transistors, which can drive up to 3 A per phase.□

CIRCLE 523

STACKING AMPLIFIERS CUTS INPUT NOISE

MOSHE GERSTENHABER AND MARK MURPHY
Analog Devices Semiconductor, 804 Woburn St., Wilmington, MA 01887; (617) 937-2200.

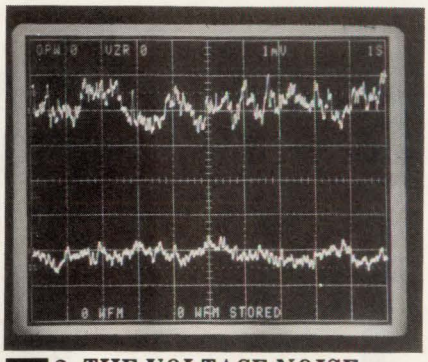
Designers with a need to amplify low-level signals from high source impedances are often caught in a quandary. Although bipolar op amps have very low voltage noise, their bias current noise is high. When passed through a high source impedance, that current noise translates into a high noise voltage.

FET-input op amps have the opposite characteristic. Their bias current noise is down in the femtoampere region, but their voltage noise is considerable. No matter which the designer chooses, he winds up with a noisy signal.

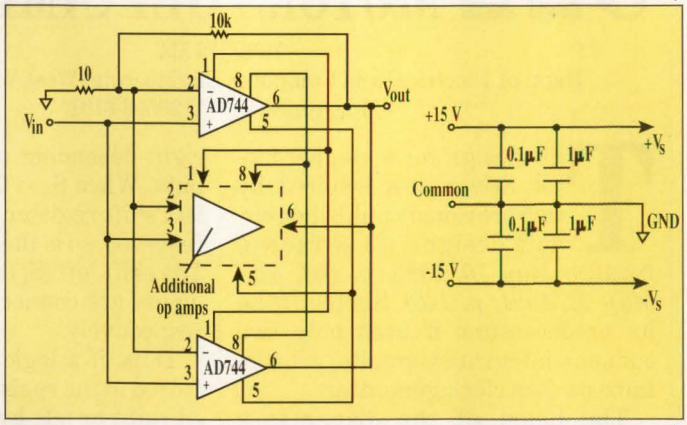
However, if a new stacking topology is used, several FET-input op amps can be put in parallel *(Fig. 1)*. That arrangement takes advantage of the fact that the voltage noise of a FET varies inversely with both the FET area and the current. Because connecting FETs in parallel effectively increases both of those quantities, it tends to decrease the noise voltage. More specifically, the stacked arrangement of amplifiers reduces the system voltage noise by the square root of the number of stacked FET-input amplifiers.

For the op amps to work properly in parallel, it's necessary to parallel certain internal nodes as well as the inputs and outputs. Fortunately, the nodes that must be paralleled are the ones made available by the compensation pins on externally compensated amplifiers. This technique is thus limited to op amps of that type.

To verify the technique, four AD744s were connected as shown in Figure 1. Then their noise performance was compared with that of a single unit *(Fig. 2)*. As the scope traces show, the four-amplifier combination did indeed exhibit only half the peak-to-peak noise of the single unit. In addition, it displayed better power-supply rejection, better common-mode rejection, less offset voltage, and—of course—more output drive capability.□



2. THE VOLTAGE NOISE of a single amplifier (upper trace) is dramatically reduced when four of them are stacked (lower trace). Both traces show voltage noise from 0.1 Hz to 10 Hz referred to the output. Amplifier gain is 1000, and scope sensitivity is 1 mV/div.



1. CUT VOLTAGE NOISE by stacking biFET op amps in parallel. The trick is to parallel the external compensation pins as well as the input and output. The technique will work with just about any externally compensated FET-input op amp.

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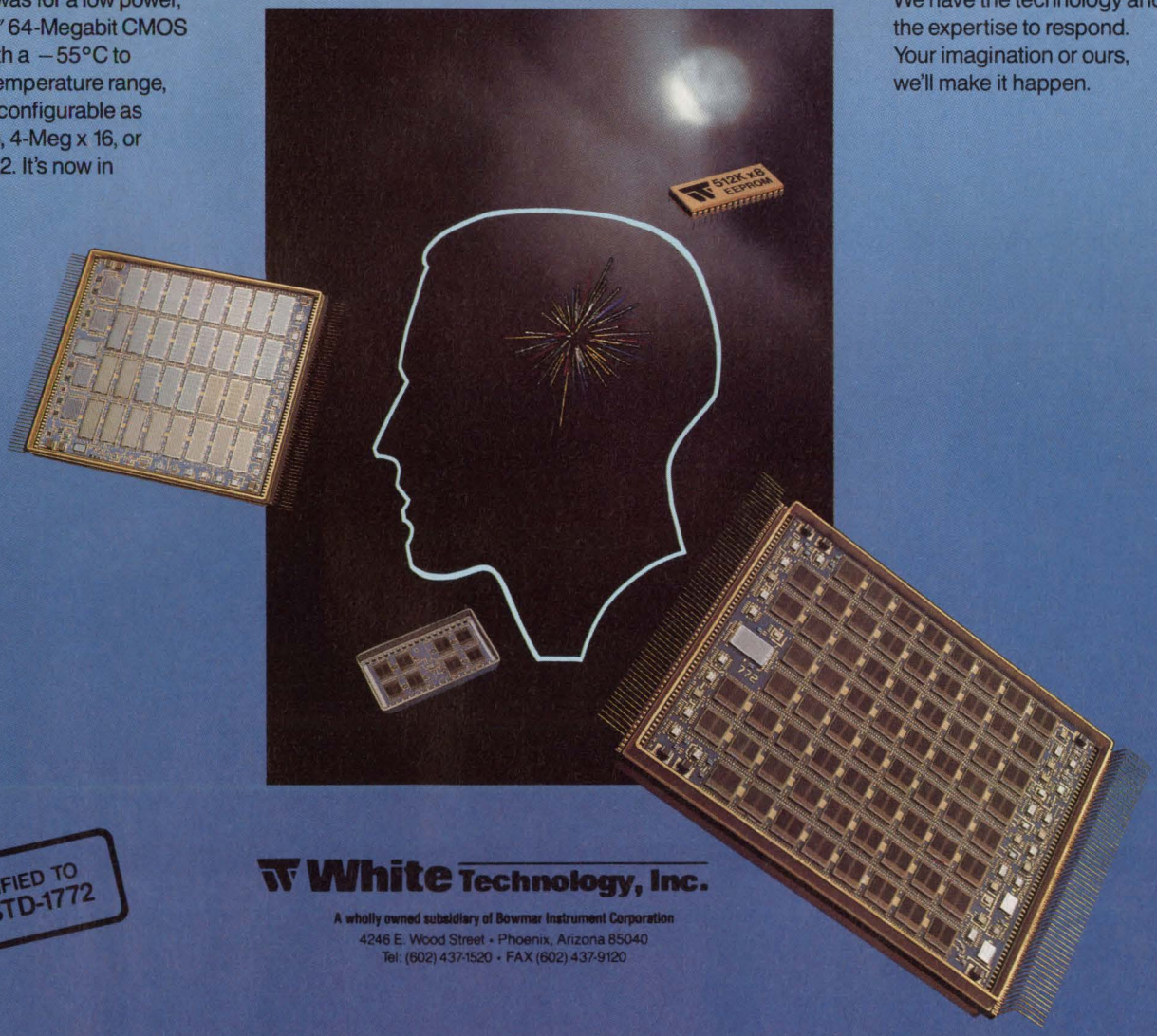

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CIRCLE 202 FOR U.S. RESPONSE CIRCLE 203 FOR RESPONSE OUTSIDE THE U.S.

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Schematics provides a menu-driven interface for specifying analysis parameters and running simulations directly from the schematic display. If device simulation parameters need adjustment after running a simulation, they can be easily modified and the simulation rerun. Netlists for PSpice are generated automatically and can be examined on the screen.

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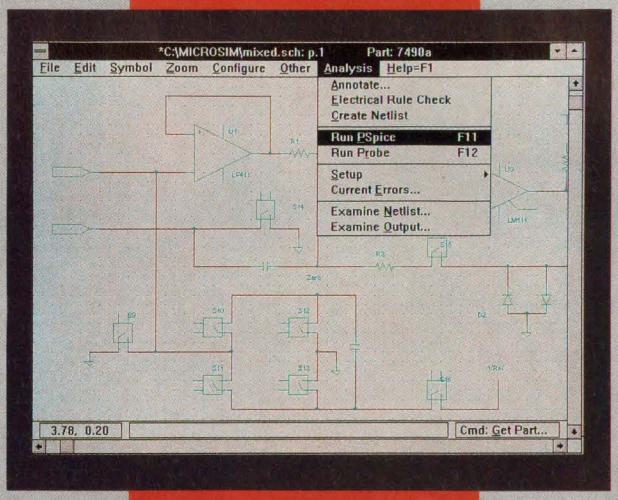
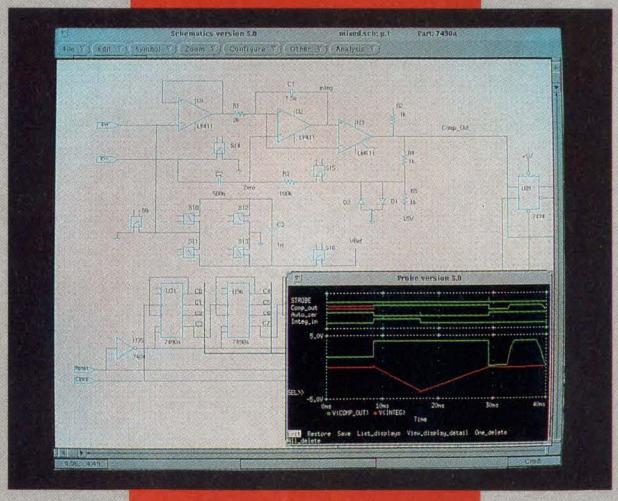
For further information on Schematics, or any other MicroSim Corporation product, call toll free at (800) 245-3022 or FAX at (714) 455-0554.



Schematics as a Windows 3.0 application



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CIRCLE 150 FOR U.S. RESPONSE **CIRCLE 151 FOR RESPONSE OUTSIDE THE U.S.**

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

TALES FROM THE SKUNK WORKS

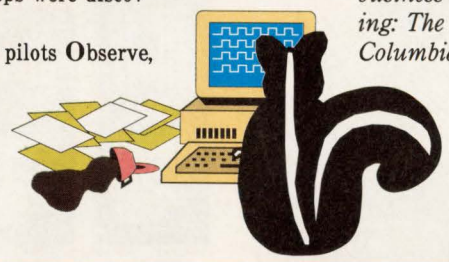
A skunk works needs winning people, and wise men through the ages have tried to discern the characteristics that distinguish them. The same attributes crop up again and again: perseverance, integrity, courage, and competency.

It is illegal to discriminate or factor people into the valuation of a public corporation. Reality says the opposite: *people matter more than anything else.* The Japanese monitor patent filings from key people. Venture capitalists invest primarily in exceptional teams, and clients hire consultants based on personal confidence.

It is rare for the first product in a new market to be profitable. In my book, I devote an entire chapter to the Japanese manner of rolling waves of products into attractive markets. It is like watching a steam drill pound through granite: study, target, niche, boom, niche, boom, niche, boom! The first product does not decide the winner, but perseverance does.

Considerable research has been devoted to a similar problem. The Air Force to its surprise found that some fighter pilots were consistent winners against equally skilled and equipped adversaries. With some additional research, OODA loops were discovered.

Winning fighter pilots **O**bserve, **O**rient, **D**ecide, and **A**ct in tight fast decision loops. The pilot who moves through OODA loops faster and with more perseverance gains significant advantage. He slowly pressures his opponent into an inferior position, and from there the kill is simple. So it is with high-tech products. And that is one reason a good skunk works wins consistently. It has the tightest, fastest, decision loops of any organizational form.



Much of what we teach in our business schools is dysfunctional to high-tech product warfare. We manage the scoreboard, not the game. In the U. S., if a new product fails, we customarily blame the leader and demolish the team. If it succeeds, we generally stop, disband, and take profits. Starting the next generation product immediately delays profits, but embodies less risk and investment. Today, in highly contested markets, a few world-class companies start their next products well before the predecessor is finished.

The best skunk works are interdependent. Their creativity enables, but production and sales generate the money. To exploit a skunk works fully, keep it rolling. Effectively transfer its fruits, when appropriate, to efficient, rapid cycle time, continually improving production teams. The skunk works starts the process, but production and sales generate sustained revenue, jobs, and profit.

John D. Trudel lectures and provides business development consulting: The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax (503) 543-6361. To order High Tech with Low Risk: *(503) 962-3755.*

DID YOU KNOW?

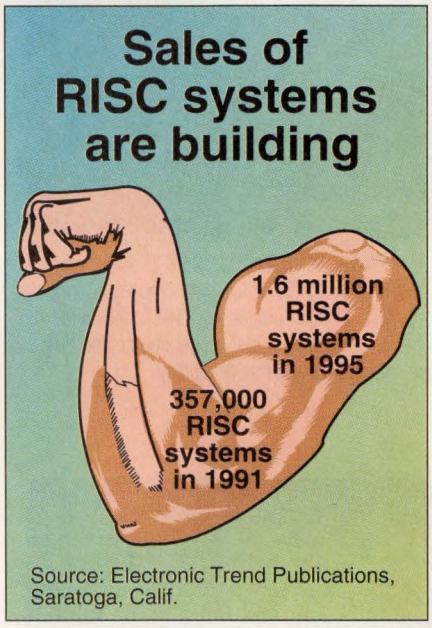
. . . that a typical high technology venture capital firm reviews 1000 startup business plans in a seven-year period, funds six of those, and sees 10% of the plans funded reach the initial public offering (IPO) stage. That means that fewer than one out of 47,000 business plans submitted reach IPO. Among the many causes for failure are poorly thought-out business plans and flawed market strategies.

from *High Tech Startup* by John Nesheim, president of Saratoga Venture Finance and published by Electronic Trend Publications, Saratoga, Calif.

MARKET FACTS

Reduced instruction-set computing became commercialized in technical workstations, with Unix the prevailing operating system. Workstation vendors touted their figures of millions of instructions per second (MIPS); users, meanwhile, found the RISC systems excelled at 3-D modeling, CAD/CAM/CAE, and software engineering.

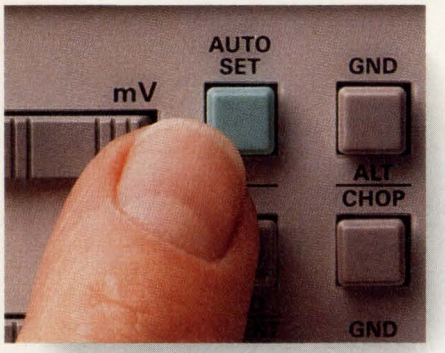
As a result, RISC is gaining ground in the computer market, from the low end, PC segment—where prices have dropped to $5,000 per seat—all the way into the realm of small mainframes. In purchasing RISC machines, users are less concerned with raw MIPS specs than with reaping the benefits of open systems and networking under Unix and running complex applications with ease.



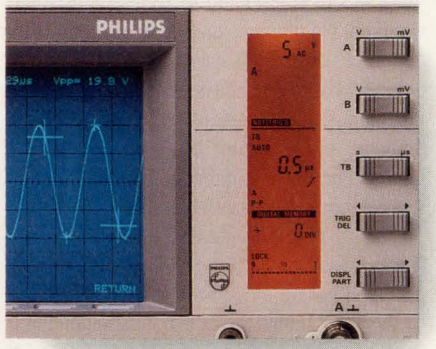
This year, 357,000 RISC units are shipping. But that number should increase to at least 1.6 million RISC systems by 1995. according to Electronic Trend Publications' market report *RISC Impact on the Computer Market.* Revenues from sales of RISC systems will climb from $5.8 billion this year to $15.8 billion in 1995, predicts the Saratoga, Calif., market researcher.

FLUKE®

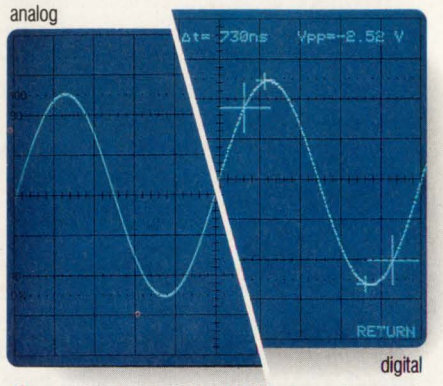
Before You Buy a Count



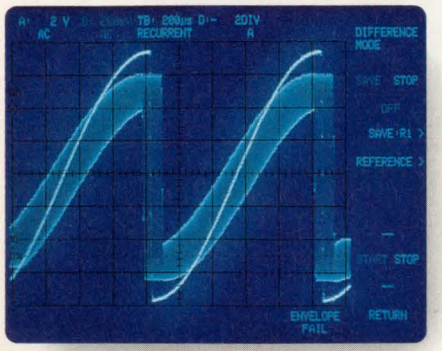
1. EASE OF USE/AUTOSET. *Unknown signals are captured quickly. Troubleshooting is a breeze.* Philips' unique AUTOSET selects the proper channel, amplitude, trigger source and timebase setting for an optimum display.



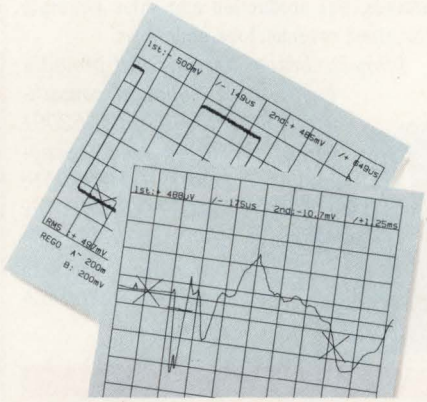
2. PARALLEL OPERATION/ERGONOMICS. *No frustration from "digging" through menus to get one control.* All main functions have individual controls with adjacent LCD or CRT readouts that tell you what you're doing at a glance.



3. COMBINATION SCOPE. *Ease-of-use and ease-of-mind.* 5 scope models combine *both* true Analog and powerful DSO performance with a choice of up to 250 MS/s and 100 MHz.



7. AUTOMATION/PASS-FAIL TESTING. *Built-in automation, features advanced measurements on complex waveforms.* Here we see the Pass/Fail function automatically indicating signals that fall outside preset limits—set by the scope, or downloaded from an external computer.



8. HARDCOPY. *Get documentation in hand.* All Philips DSOs output to printers and plotters, as well as computers.

9. MONEY. *More scope, for less money.* Philips scopes from Fluke not only perform more functions than comparable Tek and HP models, they cost less.

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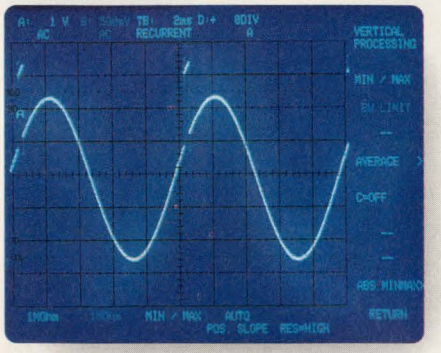
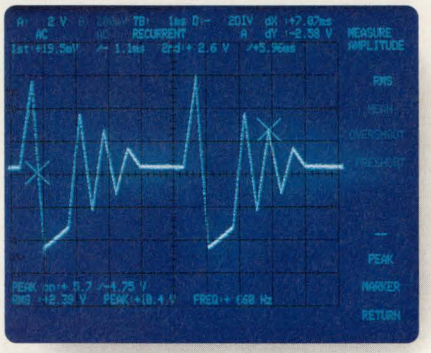


4. ACQUISITION-CATCH GLITCHES 300 MHz/500 MS/s. *Assures accuracy in display, measurement, analysis and automation tasks.* Up to 500 MS/s with 10 bit and 2 ns resolution, real-time sampling capabilities. Capture glitches as short as 3ns at lower timebase settings!



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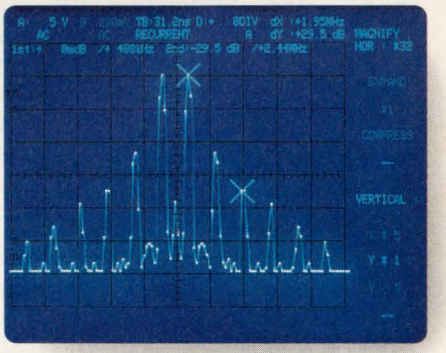

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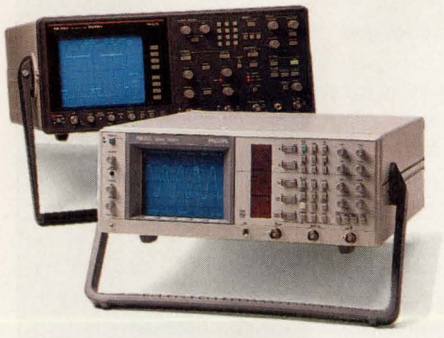

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QUICKLOOK

HOT PC PRODUCTS

Berlitz Interpreter is PC software that translates word to word in English, French, Italian, Spanish, and German. The program from Microlytics has 12.500 words per language. When a word is typed, it is translated into the other four languages. The software displays the European character set; accented characters can be entered from any keyboard.

The interpreter software is also available under license for word-processing, database, laptop, palmtop, and notebook companies and for use on memory cards. Two-language versions and highly compressed versions of the Berlitz database are available for implementing in ROM. The Windows-compatible program runs on any IBM PC, XT, AT, 386, PS/2 or compatible with DOS 3.3 or higher in 5k of RAM. Versions for the Mac and a Windows version will be available early in 1992. List price is $59.95. Contact Microlytics, Two Tobey Village Office Park, Pittsford, NY 14534; (716) 248-9150; fax 248-3868. CIRCLE 451

Sidebar software reduces the icon and window clutter in Windows. With the program from Paper Software, users can tile, size, optimize, minimize, or hide all windows on the screen by pressing one of six arrange buttons. The software, which can start up to five programs at once, also enables users to temporarily close the Windows shell to free system resources. SideBar, at $99.99, has a 60-day money-back guarantee, discounted upgrades, and unlimited customer support by toll-free hotline. Contact Paper Software, P. O. Box 567, New Paltz, NY 12561; (800) 551-5187. CIRCLE 452

A cross-reference tool from ConVal Software works with all the files that make up a software application—language source code, MAKE files, DOS batch files, and ASCII documentation. Given a list of file names in an application, FileXref scans files, producing cross-reference information, showing file names and files that reference them. With a list of symbols and symbol patterns, each marked for inclusion or exclusion, FileXref supplies information on matching symbols and shows the files that reference them. Information can be produced as a report or in a format for importing to a database. The program, which can be viewed online or printed, has a list price of $25. Contact ConVal Software Inc., 11607 E. Butter Creek Rd., Moorpark, CA 93021; (805) 529-6847. CIRCLE 453

QUICK NEWS: EDUCATION

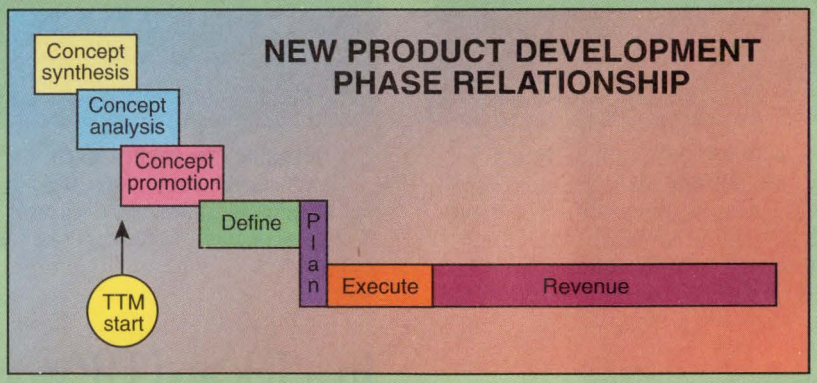
The University of Wisconsin–Madison, Department of Engineering Professional Development, will offer the course "Interfacing Sensors with the IBM PC" Jan. 15–17, 1992 on the Madison campus in the Wisconsin Center conference facility. The course aims to give students an understanding of sensor characteristics and how to choose the best interface between the sensor and its associated electronics. The sensor seminar also covers transmitting data over various distances using different types of connecting media. Cost is $750 per person, $1350 for two persons enrolled together. Contact E. K. Greenwald, Department of Engineering Professional Development, University of Wisconsin–Madison, 432 N. Lake St., Madison, WI 53706; (800) 462-0876 or (608) 262-2061; fax 263-3160.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

I'm often asked: When does the measurement of time to market start and end? Providing the answer requires structuring the discussion around a common seven-phase model. The phases are concept synthesis, concept analysis, concept promotion, product definition, product planning, product development execution, and revenue generation. An approximate time line for each phase is shown in the figure.

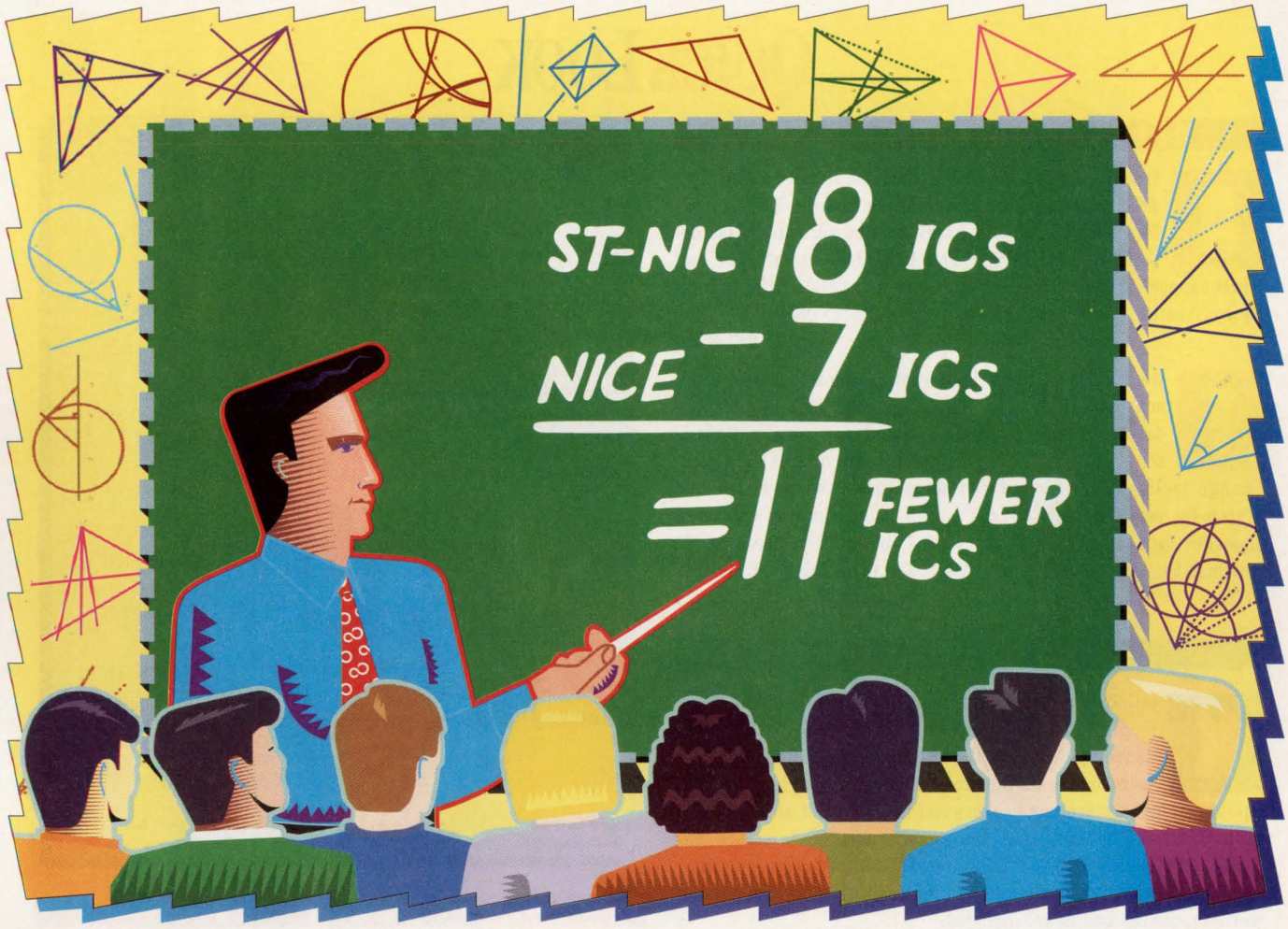


Concept synthesis usually starts with an idea being generated for a new product by an individual or very small group. The individual, or close-knit team, works with the idea and transforms it into a format that can be communicated (sometimes with extreme difficulty) to others. The time when those not part of the original creation team begin to understand and critique the idea begins the concept analysis phase. The concept cycles between analysis and synthesis over time as meat is added to the skeleton.

At some point in its embryonic state, the idea will be documented in a rudimentary fashion. This preliminary representation of the idea usually fits one or two pages of paper. Initial thoughts on a product description, customer benefits, specifications, development costs and risks, development resources and schedule, and sales potential are recorded. It is at this point that the measurement of time to market begins!

The stop-watch starts ticking away when the product concept has had some review by individuals external to its synthesis, some concept analysis has taken place, and the concept is simply documented on a few sheets of paper.

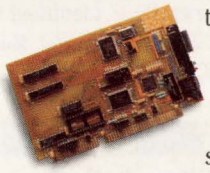
For almost any product idea, it's usually very easy to identify when these conditions have been satisfied. In the next column, I'd like to continue to discuss marking the beginning and ending of measuring time to market.



NICE and simple math exposes the myth of ST-NIC.

It doesn't take a mathematical wizard to see the superiority of the NICE® Ethernet solution from the Advanced Products Division of Fujitsu Microelectronics. We think the numbers speak for themselves.

Our NICE solution, for example, requires far fewer ICs than ST-NIC's™ so-called single-chip solution—7 vs. 18.* And that means fewer passive components as well. Making Ethernet LAN board design easier. Faster. And more cost effective than ever before.



Then, add on another factor—that NICE products are competitively priced—and systems designers clearly have a proven formula.

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CIRCLE 130 FOR U.S. RESPONSE CIRCLE 131 FOR RESPONSE OUTSIDE THE U.S.

QUICKLOOK

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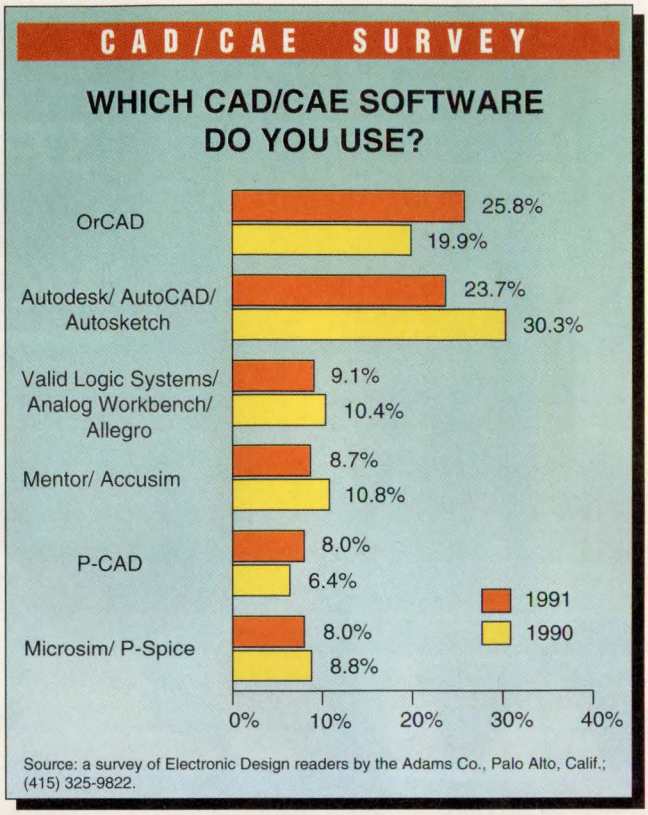
A free catalog from National Instruments describes IEEE-488.2 interfaces, data-acquisition boards, VXI controllers, along with DSP hardware and software. Also described are LabView and LabWindows software and GPIB support products. Contact the company at 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488; (512) 794-0100.

CIRCLE 454

Two brochures detail Transition Automation Inc.'s products for fine pitch SMT manufacturing. The first brochure describes the company's manual and semi-automatic screen printers. The printer brochure details the QuickChange tooling plate for reduced setup times, the precision cam system for vertical stencil lift off, as well as the company's powered squeegee for semi-automatic operation. Contact the company at 131 Stedman St., Unit 16, Chelmford, MA 01824; (508) 459-5300; fax 459-7779.

CIRCLE 455

CAD/CAE SURVEY



Source: a survey of Electronic Design readers by the Adams Co., Palo Alto, Calif.; (415) 325-9822.

QUICK REVIEWS

Keith Brindley sets out to demystify automatic test equipment in his book, *Automatic Test Equipment*, published by Butterworth-Heinemann Ltd. (1991). Brindley succeeds: he defines terms, describes various types of equipment and fixtures, and covers test methods and processes and various buses. He describes the general-purpose interface bus (GPIB), along with VME and VXI buses. The 230-page book is well illustrated with photos, drawings, and tables. A glossary and a list of world standards bodies are included.

A quibble is that the table of contents and the index are too brief to help readers dip into the material as needed. List price is $70. Contact Butterworth- Heinemann, 80 Montvale Ave., Stoneham, MA 02180; (617) 438-8464; (800) 366-2665.

CIRCLE 456

The *Integrated Circuit and Waveform Generator Handbook* by R. M. Marston is a straightforward guide to basic principles of waveform generator techniques and circuits, published by Butterworth-Heinemann (1990). Designers often generate square and pulse waveforms by means of a timer IC, or 555 type. Accordingly, the handbook has many examples of such circuits, containing more than 300 circuits, diagrams, and tables in all. The book has a list price of $22.95. Contact Butterworth-Heinemann, 80 Montvale Ave., Stoneham, MA 02180; (617) 438-8464; (800) 366-2665.

CIRCLE 457

QUICK NEWS

With cutbacks in defense spending likely for some equipment and programs, companies working in these areas need an edge. Listing more than 2,000 active design programs, *The Defense Contractor Program Atlas* is a reference guide to current military defense equipment programs and those contractors receiving government funding. The atlas locates companies and targets their participation in funded design activities. With the atlas, suppliers can identify customers of funded military weapon systems such as LHX, ATF, and the Patriot missile.

The atlas is arranged both by program and by contractor. Each program is listed with a brief description. Prime and subcontractors are identified by name and location. List price is $795. Contact Dave Trotz, Target Marketing, 1308 Centennial Ave., Suite 266, Piscataway. NJ 08854; (908) 424-0551; fax 424-0552.

CIRCLE 458

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *Art of Electronics, 2nd ed.*, by Paul Horowitz and Winfield Hill. Cambridge University Press, 1989. ***$54.50.***
2. *C Language Algorithms for Digital Signal Processing* by Paul Embree and Bruce Kimble. Prentice-Hall, 1990. ***$55.***
3. *Noise Reduction Techniques in Electronics* by Henry Ott. Wiley, 1988. ***$47.95.***
4. *Spice for Circuits and Electronics Using PSpice* by Mohammed Rashid. Prentice-Hall, 1990. ***$55.***
5. *PSpice and Circuit Analysis* by John Keown. Macmillan, 1991. ***$24.***

COMPUTER SCIENCE:

1. *C++ Programming Language*, second edition, by Bjarne Stroustrup. Addison-Wesley, 1991. ***$34.50.***
2. *C Programming Language* by Brian Kernigan and Dennie Ritchie. Prentice-Hall, 1989. ***$33.***
3. *Advanced C++ Programming Styles and Idioms* by James Coplien. Addison-Wesley, 1991. ***$33.50.***
4. *C++ Primer*, second edition, by Stanley Lippman. Addison-Wesley, 1991. ***$32.25.***
5. *Unix System Administration Handbook* by Evi Nemeth, Garth Snyder, and Scott Seebass. Prentice-Hall, 1989. ***$38.***

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; (415) 326-0681; fax (415) 326-0693.

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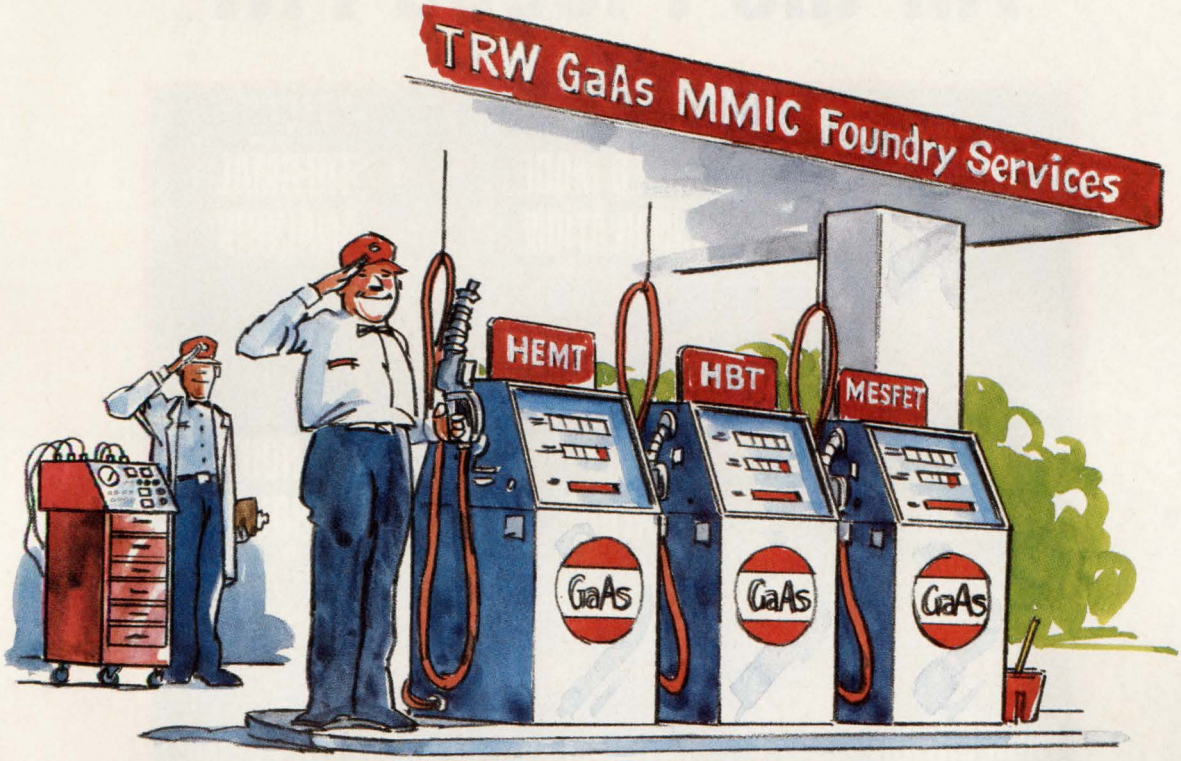

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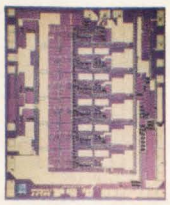

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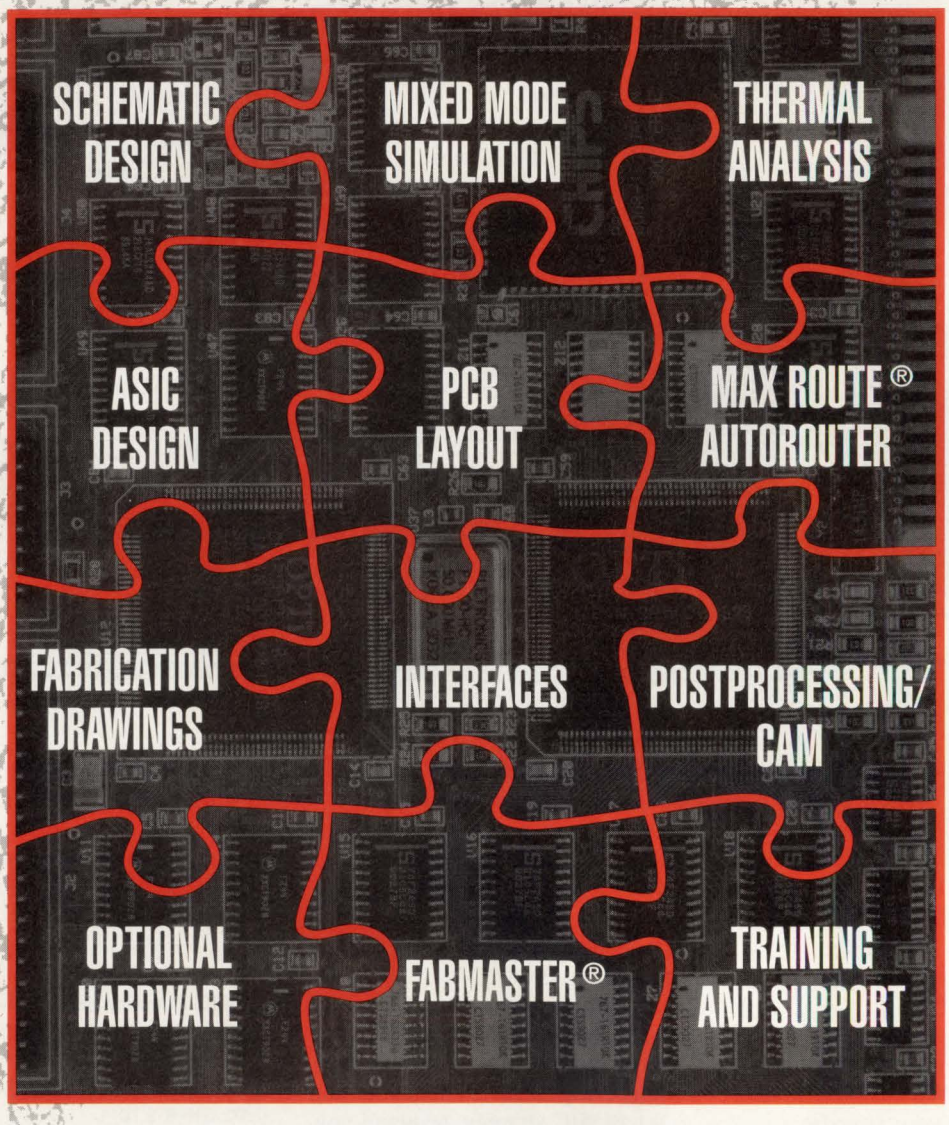

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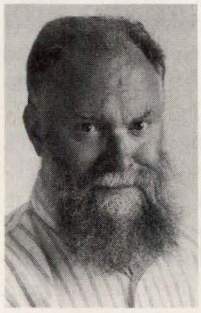
WHAT'S ALL THIS REFLEX RESPONSE STUFF, ANYHOW?

I must have been quite small when I learned that if I dropped something heavy, I should jump so as to pull my feet out of the way of the falling object. For example, if I dropped a brick that fell toward my right foot, I didn't have to worry about my left foot, but my right foot had better clear out quickly. Obviously, just about everybody learns this early enough that you have no recollection or memory of how you learned it.

At a somewhat later age, I learned that if I dropped my glasses, or my watch, or any delicate object, it was pretty easy to swing one foot underneath that object. Even if I could not entirely prevent my glasses from hitting the floor, I could deflect them so it would only be a glancing blow. And I have developed that knack, so it's pretty automatic for me.



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Then, the other day – in the summer of 1990 – I dropped something, and I did not move my foot either to catch nor to avoid the object. Well, I asked my leg, what is this that you're so blasé about? I reached down and picked up – a stick of butter. My leg had apparently made a decision that a 4-ounce stick of butter was not worth worrying about, one way or the other. Smart leg!

I mentioned this at work, and a friend (who has a lot of experience as an auto mechanic) said, "Okay, here's the fourth situation – the fourth quadrant. Let's say you are working on a Porsche, and you leave the starter motor up on a bench. Suddenly you notice that the starter has just rolled off the bench and is on its way to the floor. It weighs 30 pounds. It costs $900. NOW, what do you do with your leg?"

After some consideration, I figured that I would try to kick the starter with my toe, pretty hard, about 16 inches off the ground, so my toe would not get crushed, but it would have a chance of slowing down that heavy object. But I haven't gone to try it out.

Now, there's a very good and very serious application for this kind of preplanning, pre-judging what kind of a reflex reaction you will make, instantly, in a particular situation. Let's say you're driving along a freeway, and suddenly you spot a dog in front of you. You may blow your horn, but some dogs really don't pay much attention (some of them are deaf, and others are stupid enough, they might as well be deaf). Okay. What do you do? You might hit the brakes, but if there were a truck on your tail, he could do *lots* of damage to you. You might swerve. That's a better way to avoid the dog (unless the dog dodges in the same direction as you do – I've seen that happen). But what if there's a car passing you? You could easily wreck your car and any number of other cars, too, depending on how many cars are around you. Or, if you dodge really hard, you could go off the road and cause additional trouble. A woman was observed trying to dodge a dog on Route 93 in Medford, Mass., about 20 years ago. She missed the dog but went off the road, down an embankment, and was killed. Bad move.

Now, I'm not suggesting that you just hit the dog. In many states, if you hit a dog, you have to file a report with the police, and you might have to cart in an injured animal to the vet – no fun at all. Nobody really wants to cause pain to the dog, even if the dog is out where it shouldn't be. So, it's worth some effort to try to avoid the dog. But, what is the right answer?

The answer, I'm convinced, is to keep aware at all times of how much traffic there is behind you and beside you. If you're convinced there's nobody beside you, you can cut the wheel hard and avoid the dog. If the road is empty, you can also brake. Just try to avoid losing control. You might damage your car if you hit a big dog, but you might wreck it if you lose control completely.

And if you know there's heavy traffic all around you, well, you can try squeezing to one side of your lane to give the dog a chance to miss you. And all of the time you must have your thumb on the horn. Maybe the dog isn't deaf, just a little hard of hearing. And, after all that, if you do hit the dog, you have tried your darnedest to avoid hitting it. You did your best. But you can't do your best without being aware of traffic, and without planning in advance.

Now, if you're really aware of what's around you, you will also be prepared to dodge a deer, or a concrete block, or a loose wheel – or a child. Obviously, it's worth a lot to try to avoid a deer, because at 50 mph, almost every car will have several thousand dollars of damage if you nail that deer. And you'll be lucky if you don't wind up with the deer in the front seat with you. As for dodging a child – I hope you never have to do it. But just in case, I hope this column helps you to plan what to do. I know that in Massachusetts there's a truck line (the Crystal Freight Co., Wakefield, Mass.), and on every truck they have painted a scene with the caption: "Crystal says: After the bouncing ball... comes a running child." The scene shows a kid about to chase a bouncing ball out into a busy street. I used to laugh at that because it seemed so far-fetched. Then one day, *two*

PEASE PORRIDGE

times, a bouncing ball sprang out from behind a parked car, into the street, right in front of me. In each case, a kid stood hesitantly by the car, wise enough not to run into the street. But I stopped laughing at Crystal and her silly sayings after that.

Here's another angle on safe driving. Suppose you think you see *something* up ahead in your lane, and you're not sure if it's a blob of cardboard, or a dog, or whatever. As soon as you get at all suspicious, bring your foot over and give the brakes a tiny *tap* and start looking around for a clear lane behind you or on one side. If there's somebody behind you, it will catch their attention pretty quickly, so if you *do* have to hit the brakes hard, the driver behind you will be alert, too. Sometimes this is called defensive driving, and it sounds a little silly, but if you can use these techniques on the rare occasion there really *is* a dog or large object blocking your lane, you won't feel so foolish about tapping your brakes a little early, before you get all your plans made up.

When the N.Y. Giants played the S.F. 49ers in December 1990, the football experts said that Giants quarterback Phil Simms was playing much better that year. He had learned to throw the ball away or take a sack, rather throw into a crowd. Now that's a sensible reflex reaction. But on the game's last play, with the Giants losing 7-3, Mr. Simms could not find an open receiver and wound up getting sacked. The wisdom of refusing to throw into a crowd is imperfect if there's only one play, and you don't have any other chance to win. Every habit should be accompanied by an awareness that there are times when it doesn't apply.

Now, at this point, I wanted to give you some sage advice on how to use pre-planning and reflex response to help you in the electronics business. I had written this far, and could not think of a good example. But Frank Goodenough read my first draft and came to the rescue. He pointed out an old saying, "Never try to catch a falling knife." No matter how fast you think you are, it's very unlikely that you can grab for a falling knife 10 times without getting your hand seriously sliced at least once. Even if the knife isn't moving very fast, your hand is coming over rapidly, and it's astonishing how deep a cut you can make in that situation. In other words, it ain't worth it, and you had best plan your reflex response in advance so your head will automatically tell your hand, "Don't try it."

In the electronics business (see, I told you I would get there eventually) there's a good analogy: "Never try to catch a falling soldering iron." The odds are about as poor as trying to catch a falling knife, and the payback is equally painful. So, it's worthwhile to have a holster where the iron can be kept safely without likelihood of falling. Then drill the idea into your head, that if the soldering iron *does* fall, well, *let it*.

Frank related the story of the technician who was kneeling on the floor in front of his bench, looking for a part he had dropped. When he found it, he reached up and set it on the bench. Then, being an agile and sprightly fellow, he decided to *spring* to his feet. He put his hands on the bench, and gave a great LEAP – followed by roars of pain. He had inadvertently put one of his hands down really hard on the business end of his soldering iron, which was not in any holster. He was lucky to get out of the heavy bandages in a few weeks, but he got a very painful lesson about leaving hot items where they can be contacted accidentally.

Frank also proposed that I extend the analogy to a stack of lab equipment – a pulse generator on top of three power supplies on top of a scope on a cart. If you live in California, you know there's always a 0.05% chance of having your set-up topple in case of a 'quake. Even if you don't work out here, somebody could stumble and bump into the cart. And then you have the privilege of diving to see if you can *intercept* a couple of those valuable pieces of equipment before they hit the floor. It's a little outrageous, but valuable things do sometimes take a dive. Just make sure that your head *automatically* decides that if there is a soldering iron, *that* is not a good thing to try to grab. And perhaps you could set up your equipment so that the stack is unlikely to topple. Maybe you can wire it together, or tape or strap it up so it cannot fall.

Once upon a time, when virtually all electronic equipment ran on vacuum tubes, it was easy to remember that you could easily get a shock from almost any node of a circuit you were troubleshooting. So the rule developed: When probing or trouble-shooting a circuit, *always* keep one hand in your pocket rather than hold onto a chassis or rack. Then if you brush against a high voltage, it will not cause a lot of milliamperes to flow *right past your heart*. The odds of being electrocuted used to be greatly reduced by this simple precaution.

These days, the new transistorized circuits are all at low voltage – except when they aren't. There are line-operated switch-mode power supplies, and high-voltage boosters that can put out ±80 volts – and suddenly that old precaution of keeping one hand in your pocket is beginning to look pretty smart again.

So, whenever I start work on a high-voltage circuit, I tack in a neon lamp in series with a 100k resistor across the high-voltage busses. Then when I see the neon's glow, I'm graphically reminded that this really *is* a high-voltage circuit, and that the power is still ON (I don't care what the power switch says) and I should revert to the mode of High-Voltage Cautions. If I grab onto a really hot wire, the shock might not injure me, but I might convulse and jerk backwards. That's not a good idea if I'm standing on top of a ladder, for instance. So, looking for the glow of a neon lamp is a way to remind me to be serious, and I recommend it for you, too.

Please do try to keep aware at all times while you're driving, whether there's anybody beside you or behind you, so if you do have to make an emergency swerve, you will know if it's safe. It may save your life, or it might save your car. Be careful out there! And, keep one hand in your pocket when working on high-voltage circuits.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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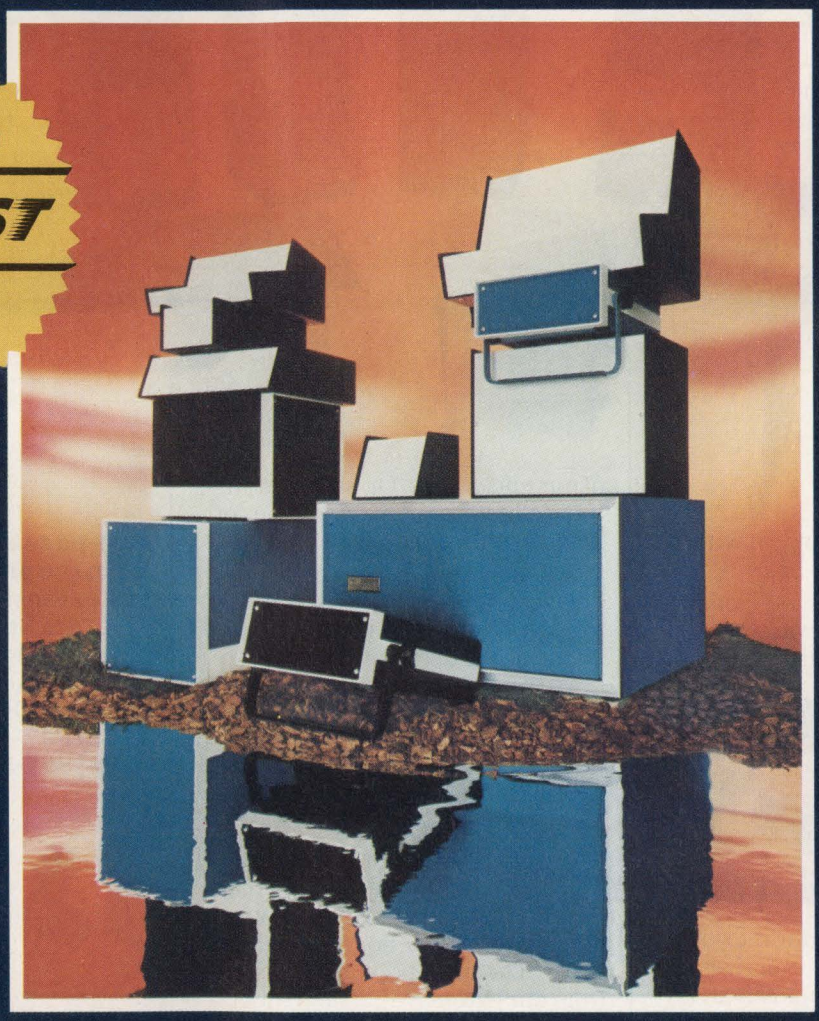

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ONE TOOLSET CREATES FPGAS IN ANY TECHNOLOGY

LISA MALINIAK

Field-programmable gate arrays (FPGAs) are the fastest growing segment of the semiconductor market for several reasons. To start with, FPGAs provide an efficient way for system engineers to consolidate random logic into as few chips as possible. In addition, FPGAs can help ASIC engineers shorten the prototype-debug-implementation cycle of chip designs. But FPGA vendors offer their own proprietary design tools and, in some cases, different tools for each of their unique architectures. As a result, engineers must either be locked into one FPGA architecture, or learn a different design system for each programmable-logic architecture they wish to use.

A better solution is to have one design toolset that addresses all FPGA architectures. A new company called NeoCAD Inc. is providing just that: the industry's first device-independent computer-aided-design (CAD) tools specifically for the design and layout of FPGAs. The new tools, called FPGA Foundry, support technology-transparent design—the ability to design without targeting a specific architecture implementation during schematic capture. FPGA Foundry is a CAD toolset that includes a timing estimator, circuit optimizers, device mappers, timing-driven automatic place-and-route capability, a graphical editor, back-annotation, and report-file generation.

One key element of NeoCAD's strategy is its Partnership Program, under which the company works closely with existing and prospective FPGA vendors to guarantee optimal support for their devices. The program includes several levels of involvement, beginning with cooperative efforts to ensure that NeoCAD's tools support the unique features of a particular vendor's FPGA architectures. At the highest level of involvement, NeoCAD may act as a second source or as the primary tool supplier for new generations of programmable-logic architectures.

A SOLID FOUNDATION

The Foundry tools are built on a device-independent data structure, which lets them support multiple device architectures while still providing full support of device-specific features. The key to these capabilities is a software backplane that uses a hierarchy of algorithms, cost tables, and routines to perform device-independent place-and-route routines without sacrificing performance or functionality. In addition, the modular structure of the software backplane lets users quickly and easily add support for new architectures and device features as they become available.

Foundry's timing- and constraint-

driven design environment puts the engineer in complete control of all design priorities at the start. To take advantage of this feature, the designer identifies nets requiring critical-path delays, minimum clock speeds, and any other desired constraints. Knowledge-based software called the Timing Estimator then analyzes the design based on clock speeds and the design hierarchy. It automatically generates the additional path-delay and constraint information required by the Mapper and Place-and-Route modules.

The Mapper module combines this timing and constraint information with the device-independent database and device-specific files, and uses synthesis algorithms to determine how the logical design description will best fit into the physical device. Then, the Mapper module automatically assigns the logical description to elements within the device's physical blocks.

An Automatic Place-and-Route (APR) module, driven by the same timing and constraint data as the Mapper module, places the compiled logic into specific logic blocks on the chip and routes the connections between them. APR algorithms continuously converge toward an optimal set of interconnections. Both modules use tightly-coupled automatic feedback mechanisms to arrive at an optimal design.

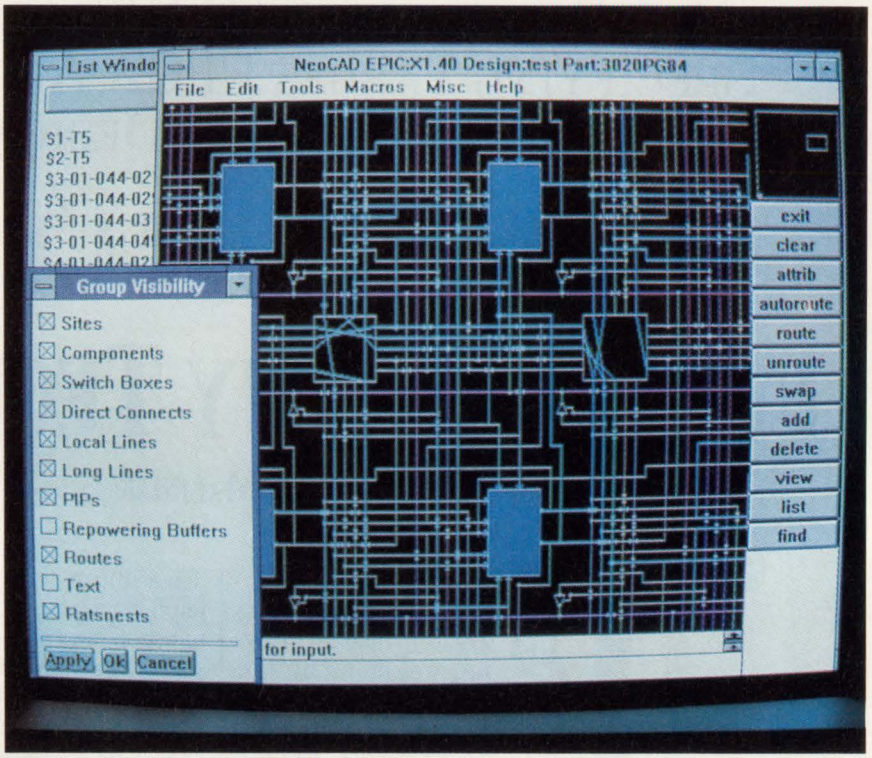
If engineers choose to route critical nets interactively, NeoCAD's Editor for Programmable ICs (EPIC) software provides interactive editing capabilities *(see the figure)*. EPIC meets the requirements of a wide range of users, from push-button users interested in highly automated functions, to power users who need to select and perform operations on almost any element of the design.

EPIC's graphical interface supports menu-driven and command-line editing. Also, it allows for place-and-route tools to be run incrementally. A user-configurable select-list helps users operate on one block, groups of blocks, I/O blocks, placed or unplaced logic, signals, and routed or unrouted nets. In addition, EPIC can highlight signals by delay characteristics.

The FPGA Foundry software also includes a report generator and back - annotation tools. The report generator provides a delay report that lists the path and net delays within the programmable-array design. It also lists logic-block and I/O utilization, and available resources. Back - annotation tools supply timing data to simulators, and also output net lists in various electronic formats.

FPGA Foundry is fully compatible with the major CAE vendor's design-entry and simulation tools. It accepts designs in standard descriptions, including EDIF 2.0.0 and Library of Parameterized Modules (LPM). FPGA Foundry also accepts vendor-specific net-list formats, such as the Xilinx XNF format and the Actel ADL format. In addition, the complete toolset is designed to run under most popular CAE frameworks.□

THE TOOLS SUPPORT MULTIPLE ARCHITECTURES WHILE STILL EXPLOITING DEVICE-SPECIFIC FEATURES.



USERS CAN VIEW AND EDIT the physical layout of a circuit with the Editor for Programmable ICs (EPIC) that's included in the FPGA Foundry toolset. EPIC's graphical interface features menu-driven and command-line editing.

PRICE AND AVAILABILITY

Pricing for FPGA Foundry starts at $18,000. It's shipping now on Unix-based workstations running X-Windows and 80386- and 80486-based PCs running Microsoft Windows. The initial release of FPGA Foundry will support Actel and Xilinx devices. Additional devices will be added within six months.

NeoCAD Inc., 2585 Central Ave., Boulder, CO 80301; (303) 442-9121. CIRCLE 512

HOW VALUABLE?	CIRCLE
HIGHLY	550
MODERATELY	551
SLIGHTLY	552

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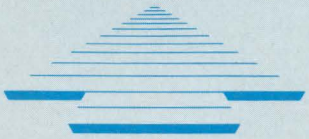

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CIRCLE 106 FOR U.S. RESPONSE CIRCLE 107 FOR RESPONSE OUTSIDE THE U.S.

1. THE MODEL 2001 DMM HAS a 52-character display that can indicate multiple measurements on the same signal simultaneously. The unit is built into a half-rack-size case.

FIVE PROCESSORS BOOST DMM'S PERFORMANCE

A SEPARATE PROCESSOR FOR EACH MAJOR FUNCTION HELPS OPTIMIZE THE HIGH-RESOLUTION UNIT'S SPEED, ACCURACY, AND SENSITIVITY.

JOHN NOVELLINO

Microprocessors in test-and-measurement instruments are certainly commonplace today. Many units have one or two devices controlling the instrument's operation, and at least one oscilloscope family incorporates three microprocessors. But the new standard for microprocessor control of discrete instruments is a digital multimeter (DMM). Using a total of five processors, the new meter racks up an excellent combination of resolution, accuracy, sensitivity, and speed.

The Model 2001 from Keithley Instruments also performs a number of measurements other DMMs don't make or don't make directly, such as ac crest factor, peak spikes, and ac peak, average, and true-RMS values. And the ac bandwidth is a very wide 2 MHz. A separate frequency measurement capability works to 15 MHz. All this is available in an economical instrument, housed in a half-rack-size package *(Fig. 1)*.

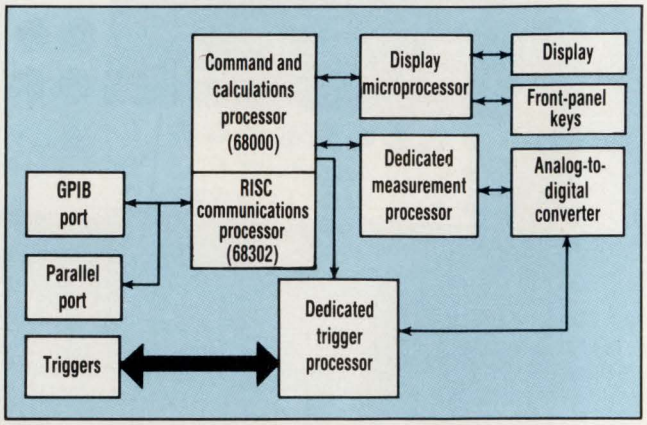
Users can select 4-1/2- to 7-1/2-digit resolution. Unlike some digital multimeters, which average multiple 6-1/2-digit readings to extend their resolution to 7-1/2 digits, the Model 2001 has true 7-1/2-digit, 28-bit capability. The result is a wider dynamic range and greater ac and dc measurement integrity

FIVE PROCESSORS BOOST DMM

over a wide measurement range.

Keithley is aiming the Model 2001 at two types of users. The first includes those who want but can't afford to move up from a 5-1/2-digit meter to a 6-1/2-digit unit. The second group is already using 6-1/2-digit DMMs but needs higher performance at that resolution.

Most DMMs employ one microprocessor to control the instrument's five primary functions: analog-to-digital conversion, triggering, front-panel display, front-panel keys, and GPIB communications. A single-processor architecture, however, can get bogged down trying to handle all these functions. To keep performance specifications and speed at high levels, Keithley assigned separate processors to each function *(Fig. 2)*.



2. A FIVE-PROCESSOR ARCHITECTURE ensures that the Model 2001 maintains high performance even in demanding test situations.

A recently introduced Motorola 68302, which combines a reduced-instruction-set computer and a communications processor, handles GPIB communications. A dedicated measurement processor in an ASIC controls the a-d conversion. Another ASIC forms the trigger processor, which permits fast triggering without the timing uncertainties of older architectures.

A separate processor supplies extremely fast response to keystrokes and ensures that the real-time display does not slow down measurements being made elsewhere in the circuit. Finally, a 16-bit Motorola 68000 performs high-speed command processing and calculations.

The meter complies with the Standard Commands for Programmable Instruments (SCPI) standard, which includes a well-structured trigger-programming scheme. Trigger-Link, a function built around this SCPI model, makes it easier to build multi-instrument systems with very precise timing and synchronization. Conventional systems may limit triggering to a pair of instruments or may require a separate relay to select different triggers for different parts of a test. In addition, in conventional DMMs the microprocessor that runs the instrument typically handles the triggering also.

SYNCHRONOUS TRIGGERING

IEEE-488 instruments typically support only one type of triggering, 2-wire asynchronous, notes Keithley. In applications requiring larger test systems, a one-line synchronous trigger enhances operation by automatically coordinating the operation of multiple instruments. This scheme helps protect against damage to devices caused by running a test before all instruments have stabilized. It also reduces bad readings at the beginning of a measurement sequence.

Trigger-Link, on the other hand, combines six independent software-selectable trigger lines on one connector. The result is simple, direct control over all instruments in a system. Also, the delay between a trigger and the beginning of a measurement can be cut by several orders-of-magnitude, to 20 μs. Trigger uncertainty is less than 2 μs.

A unique feature is a proprietary technique that measures current without breaking the circuit. The procedure uses Ohms' law and takes advantage of the meter's sensitive resistance measurement, very-low-noise dc measurement, and "offset compensated" ohms capabilities.

The meter's basic ac-voltage accuracy is within 0.05%; basic dc-voltage accuracy is within 18 ppm for 90 days and 7 ppm for 24 hrs. A high-resolution resistance range features a resolution of 1 $\mu\Omega$. Range and function changes are made in 20 to 150 ms, and autoranging is 10 to 100 times faster than competitive units, according to Keithley.

Users can program each channel on the 10-channel scanner to handle a different function. The DMM's 52-character display presents multiple measurements on the same signal simultaneously. Stored data is time stamped. The instrument also performs extensive mathematical operations.

The Model 2001 supports both resistance temperature detectors (RTDs) and thermocouples for temperature measurements, and offers four separate outputs linked to limits for binning operations. The unit has an 1100-V input rating and is protected to 1600 V. Its built-in self-testing feature covers more than 75% of all of its components.

At 4-1/2-digit resolution, the Model 2001 takes up to 2000 readings/s. Even at 6-1/2-digit resolution and full accuracy, 45 readings/s are possible. If desired, the user can set the resolution and let the meter default to the speed that ensures the best accuracy. Conversely, the user can specify the reading rate and the instrument will default to the proper resolution for that speed. The ability to specify a reading rate simplifies the effects of non-line-cycle noise on measurements.□

PRICE AND AVAILABILTY

The Model 2001 digital multimeter costs $2695 and is available 6 weeks after receipt of order.

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, OH 44139; (800) 552-1115 or (216) 248-0400. **CIRCLE 513**

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

INTELLIGENT SCSI CONTROLLERS DELIVER END-TO-END SOLUTION

DAVE BURSKY

Designers controlling high-performance data movement have an end-to-end solution—a pair of controllers for the small computer systems interface (SCSI). One controller is optimized for use in peripherals and the other optimized for integration on ISA and EISA motherboards or with host adapter cards.

The Adaptec AIC-8010 controller fits right into peripherals such as disk drives and automates many of the common bus control sequences and buffer management for SCSI operations, moving data over SCSI at up to 10 Mbytes/s. The other chip, the AIC-7770 provides a 32-bit host bus interface for ISA or EISA motherboards or host adapters and two independent 8-bit channels or one 16-bit SCSI channel that have an aggregate transfer rate of 20 Mbytes/s.

Designed to meet the SCSI-2 performance levels, the AIC-8010 transfers data over the SCSI bus at the 10 Mbyte/s fast-SCSI rate, or the 5 Mbyte/s asynchronous or synchronous SCSI-1 rate. Transfers are done with up to a 15-byte offset and over either a directly driven single-ended interface or with external buffers, over a differential cable. The chip can implement SCSI-2 features such as caching and command queuing while reducing microprocessor involvement and SCSI command overhead. The use of the high-level SCSI command set not only decreases the amount of microprocessor intervention required, but also reduces the overall SCSI command overhead while increasing bus utilization, since multiple phases are automatically managed.

The controller supports high data transfer rates from the read head—non-return to zero coded serial data streams move at 36 Mbits/s on the peripheral side of the chip, while on the host-bus side the SCSI port transfers data at a maximum rate of 10 Mbytes/s (synchronous fast-SCSI). An off-chip buffer composed of either SRAM (256 kbytes, maximum) or DRAM (1 Mbyte, maximum) has a maximum bandwidth of 15 or 12 Mbytes/s, respectively, which allows the SCSI-bus transfers to run at maximum for the depth of the buffer RAM employed in the subsystem.

Incorporating many software-programmable and hardware-selectable features, the 8010 includes an on-chip sequencer that is a superset of the one employed in the previously released AIC-7100 family. The sequencer can be programmed to handle disk format, or read or write operations and support constant-density recording (CDR) and defect skipping. The enhanced sequencer RAM is 48 words deep by 32 bits wide (an increase from 31 words in the 7100 family). The company supplies standard code to configure the RAM in the driver software. Nonetheless, users can customize the code to implement unique track formats and other features.

Designed in high-speed CMOS, the AIC-8010 keeps power consumption low by offering microprocessor-selectable disk block power-down and/or SCSI block power-down (with auto wake-up) modes. The chip works in conjunction with a local microprocessor that communicates by writing to and reading from various internal registers. The microprocessor interface is a high-speed eight-bit multiplexed address/data bus that can interface directly with a variety of microcontrollers or microprocessors.

The error-detection and correction block on the 8010 supports industry standard 32- and 56-bit computer-generated codes and an 88-bit noninterleaved Reed-Solomon code (all fixed). The standard 16-bit CRC-CCITT polynomial can be used for error detection on the ID/header.

The buffer control block manages a true four-port architecture (including priority resolution) and gives users four independent 22-bit pointers for the disk, host, microprocessor, and correction ports, respectively. The 8010 allows buffer segmentation from 1 kbyte to the maximum RAM size. Up to 4 kbytes of data buffer in the lowest segment can be allocated for use by the microprocessor as a scratch pad area. This scratch pad can be used for microprocessor program variable storage or for microprocessor to SCSI and/or microprocessor-to-disk transfers.

Tackling the needs of motherboard and host adapter designers, the AIC-7770 with its TwinChannel (a dual SCSI bus) interface gives designers the most compact solution when multiple SCSI ports must be implemented within a system. Able to operate as a bus master, the chip contains two independent SCSI controller cores with 8-bit I/O buses. Each core can be independently configured for single-ended or differential cabling as well as for synchronous or asynchronous operation with either standard- or fast-SCSI timing. Furthermore, the two cores can be used in tandem to implement a wide-SCSI (16-bit) interface.

A 256-byte FIFO register on chip buffers data transfers, maximizing the DMA transfer rate while reducing host bus-hold time. A RISC-like controller core on the chip—dubbed the PhaseEngine—delivers 8 MIPS of internal processing power.

The AIC8010 comes in either a 100-lead thin quad-sided flat package (TQFP) or a standard 100-lead QFP. In lots of 1000, the 8010 sells for $18.95 apiece. A 160-lead plastic QFP will be required to house the AIC-7770 EISA/ISA to SCSI controller, which will sell for $50 each in lots of 1000. Samples of the 8010 are available now, but the 7770 won't be sampled until the first quarter of 1992.

Adaptec Inc., 691 South Milpitas Blvd., Milpitas, CA 95035; for the 8010, call Ken Chuang at (408) 945-8600 and for the 7770 contact Byron Smythe at (408) 945-6761.

CIRCLE 460 for the 8010
CIRCLE 461 for the 7770

SINGLE CHIP MANIPULATES REAL-TIME VIDEO DATA

Able to continuously scale and filter motion video images, the CL-Px0070 video window generator delivers 250 MIPS of processing power for applications such as multimedia, video teleconferencing, and others. Developed by Pixel Semiconductor Inc., a division of Cirrus Logic, the chip can solve most of the problems associated with integrating TV-based video into a windowing environment such as found on most desktop computers. Although the chip delivers 8-to-24-bit color images, its signal-processing architecture coupled with a proprietary algorithm lets the chip provide 8-bit/pixel images that look as if they were created on 24-bit systems.

On the chip are a format and color converter, a linear resampler, an output pixel processor, a output FIFO buffer 16 pixels deep, and a programmable control unit. The programmable controller is key, because it can solve many of the coordination problems associated with real-time video and interactive multimedia. The input block accepts digitized video in YUV format and converts it back to RGB, as required by computer monitors. The linear resampler performs independent X and Y axis real-time scaling of the RGB video data with single-pixel resolution; in contrast, most other scaling implementations scale in increments of multiple pixels. Windows of any size, displaying real-time video, can be placed anywhere on the screen. The output pixel processor on the chip can be programmed to handle between 2 and 8 bits per RGB channel.

The CL-Px0070 comes in an 80-lead PQFP and operates from a 5-V supply. Samples are immediately available and in lots of 1000, the chip sells for $55. apiece. A free-standing 24-bit/pixel development board sells for $3900.

***Cirrus Logic Inc.**, 3100 West Warren Ave., Fremont, CA 94538; (415) 623-8300.* CIRCLE 477

■ *DAVE BURSKY*

HIGH-GATE-COUNT ARRAYS USE 2- OR 3-LEVEL METAL

Packing 32,000 to over 360,000 available gates, the TC165G family of CMOS arrays give the user an optional level of usability through their use of two or three levels of metal interconnection layers. Developed by the Vertex Semiconductor subsidiary of Toshiba America, the array family employs a channelless architecture and is implemented with 0.8-μm design rules. An offshoot of the family, the TC165E, allows embedded functions to replace portions of the array to create customized masterslices.

The maximum gate utilization is determined by the number of metal-routing layers—with three levels, the chips achieve about 60% utilization, while with two layers of metal, the percentage drops to about 45%. There are 10 masterslices in the family and to accompany the large gate counts. The chips also have a large number of I/O pads—from 160 for the smallest chip to 504 pads for the largest (from 212 to 680 if TAB is used).

Internal gate delays are less than 262 ps for a lightly loaded gate operating from the nominal 5-V supply. When run from 3.3 V, a standard NAND gate has a 400-ps delay. Typical gate power consumption is about 3 μW/MHz. Although the chips are designed for 5-V operation, they do have an option to implement a 3.3-V I/O interface.

During the design phase, the support tools can automatically insert a clock tree to keep skew to less than 390 ps. In addition, they can add a phase-locked loop to curtail chip-to-chip skew to less than 1 ns. Embedded functions such as static RAM can be added as well—when implemented by metallization, a 32-word-by-32-bit block accesses in 8.4 ns, while a diffused, 32k-by-8 block accesses in 10 ns.

Non-recurring engineering charges start at about $30,000. For a typical design, a 102,000-gate chip with two layers of metal and housed in a 208-lead PQFP—the ICs go for about $42 apiece in lots of 10,000. Samples require about three weeks from netlist signoff.

***Vertex Semiconductor**, 1060 Rincon Circle, San Jose, CA 95131; Kirby Kish, (408) 456-8900.* CIRCLE 478

■ *DAVE BURSKY*

FAST 8-BIT MCUS APPLY RISC APPROACHES

Delivering processing throughput several times that of most other microcontrollers, the PIC17C42 series of 8-bit CMOS processors employs a RISC-like architecture to achieve single-cycle execution of most instructions. The short execution time—250 ns—allows the processor to perform many more instructions than other 8-bit controllers. The PIC17C42's pipelined, dual-bus architecture with separate program and data buses is partially responsible for the performance improvement. Furthermore, the streamlined instruction set of just 55 commands minimizes programming complexity.

At a 16-MHz clock, the processor delivers a throughput of about 4 MIPS. Higher-performance versions are planned as the clock frequency increases to 25 and 32 MHz in 1992. Besides the streamlined CPU core, the microcontroller contains 2 kwords by 16-bits of EPROM and can address up to 64 kwords. It can directly or indirectly address 232 byte-wide data-memory locations or file registers and 48 special-function registers. All special-function registers, including the program counter, are mapped into the data memory. The highly orthogonal instruction set allows the CPU to carry out any operation on any register using any addressing mode, making the chip's programming very simple and efficient.

Additional on-chip resources include three 16-bit timer-counters (one can be configured as two 8-bit units), and two pulse-width-modulated outputs, each capable of resolving 10 bit at 15.6 kHz (or 8 bits at 62.4 kHz).

A full synchronous or asynchronous serial port with its own baud-rate generator, two 16-bit 10-ns capture latches, and 11 external/internal interrupts are also available for control and communications. In addition, the CPU includes a sleep mode to minimize power drain when inactive.

In lots of 10,000, the plastic-encased 40-pin DIP version of the PIC17C42 sells for $6.25 apiece. Samples are available from stock.

***Microchip Technology Inc.**, 2355 W. Chandler Blvd., Chandler, AZ 85224-6199; George Rigg; (602) 963-7373.* CIRCLE 479

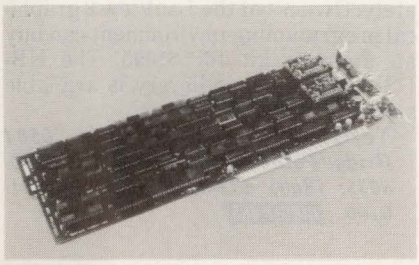
■ *DAVE BURSKY*

DEVELOP EXPENSIVE MILITARY BOARDS ON A LOW-COST PC

Using the Navigator II family of military-to-PC interface boards, PCs can emulate expensive military computers and peripherals. The family contains members that support all three types of serial NTDS (Navy Tactical Data System) data communications; MIL-STD-1397 type J (for fiber-optical data), type E (for low-level serial data on a triaxial cable), and type D (for serial data on a coaxial cable).

The family's system-integrity features can test for parity and frame errors and illegal conditions. Error conditions can be forced for diagnostic and confidence testing as well. The boards support bursts of up to 256 concatenated words at 10 Mbits/s. On-board FIFO buffers act independently of the host PC's speed.

Resident software drivers decrease



the effort that's required to develop and integrate military systems. The software is compatible across the entire family of boards. As a result, applications developed for one type of board can be ported to the others. The boards sell for $2900 each. Large quantity discounts are available.

***Sabtech Industries Inc.**, 5411 East La Palma Ave., Anaheim, CA; (714) 970-5311.* **CIRCLE 462**

■ *RICHARD NASS*

LINK BRINGS TRANSPUTER POWER TO SPARCSTATION

Plugging a BBK-S4 Transputer interface into a Sparc-compatible workstation turns that platform into a host for large-scale multiprocessor Transputer systems. The SparcStation becomes a scalable system on which users can perform system development or scientific research without the performance limitations of a single-processor system. The BBK-S4 serves as a high-speed bus bridge, transferring large amounts of data from the S-bus to the Transputer system at 8.8 Mbytes/s. The interface, functioning as a slave, uses a T225 Transputer as a controller chip to multiplex bidirectional serial data from the S-bus in up to four parallel streams. Communication using standard-link protocol between the Transputer network and the S-bus is jumper selectable between 5 and 20 Mbytes/s. The interface costs $3950 and is available now.

Parsytec Inc., Bldg. 9, Unit 60/61, 245 W. Roosevelt Rd., West Chicago, IL 60185; (708) 293-9500. **CIRCLE 463**

MEGOHMMETER MAKES INSULATION TESTS

The Model 1865 megohmmeter/insulation-resistance tester incorporates a number of features that make it suitable for a wide variety of applications. As a megohmmeter, the unit offers both a handler interface and an optional IEEE-488 interface. Results are dispayed in plain, user-friendly terms. As an insulation-resistance tester, the Model 1865's test cycle is programmable in four phases: charge, dwell, measure, and discharge. The instrument measures resistance to 1000 tera-ohms, with a basic accuracy with 0.5% below 1 tera-ohm. Test voltage is programmable to 1000 V. A custom keypad speeds data entry, and a high-resolution LCD graphics screen displays menus that help users set up tests. The Model 1865 costs $3595, and initial orders will be shipped in January.

QuadTech Inc., 45 Main St., Route 117, Bolton, MA 01740-1107; (508) 779-8300. CIRCLE 464

TOOLKIT AVAILABLE FOR MAC II DSP BOARDS

Designers who are developing applications for the NB-DSP230X series of digital-signal processing and analysis accelerator boards may find their task is eased. With the LabView DSP Developer Toolkit, designers can work faster and less expensively. The NB-DSP230X boards for the Macintosh II family use the Texas Instruments TMS320C30 digital signal processing chip to perform calculations much faster than the computer's general-purpose 680X0. The Toolkit contains LabView 2, a graphical programming environment for developing data-acquisition and control systems. In addition, the kit contains the NB-DSP230X series analysis library and interface utilities. The Toolkit also contains the Texas Instruments Developer Toolkit. The LabView DSP Developer Toolkit costs $2995. The Toolkit is available immediately. Owners of the LabView 2 graphical programming environment can buy an upgrade kit for $1495. The NB-DSP230X analysis library is available separately for $695.

National Instruments Corp., 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100. CIRCLE 465

VXI MODULES DO DIGITAL, WAVEFORM TESTING

Two one-slot, C-size VXIbus modules can be combined to form the heart of a mixed-signal production tester. The VX4820 digital test module offers a functional pattern source with data rates of up to 20 MHz. The production tester also supplies pin electronics, fixturing interconnect, and local pass/fail evaluation for high throughput. Combined with other support hardware, multiple VX4820 tester units can create a 768-channel system. The other module, the VX4250 waveform tester/analyzer, acquires waveforms at up to 100 Msamples/s and has a 100-MHz bandwidth. It has 8-bit resolution. The unit stores complete measurement sequences, including amplitude, time, and waveform limits. The tester/analyzer unit can make up to eight parametric measurements (from a selection of 19 types) on the data acquired in one test iteration. A 64-pin Model VX4820 costs $13,000, and a 32-pin version is $9000. Delivery is in 6 weeks. The VX4250 tester sells for $6500. Delivery is in 8 weeks.

Tektronix Inc., Test and Measurement Group, P.O. Box 1520, Pittsfield, MA 01202; (800) 835-4894. CIRCLE 466

1-GHZ TEST RECEIVER HAS 60-DB DYNAMIC RANGE

The Model R-110 test receiver covers 1 kHz to 1 GHz with 26 built-in bandwidths ranging from 200 Hz to 15 MHz. The receiver's noise figure is 12 dB or better, with 8 dB typical; the dynamic range is 60 dB. The R-110 receiver, which is fully synthesized, offers a timing resolution of 1.0 Hz or less to 15 MHz and 100 Hz from 15 MHz to 1 GHz. Users can control the receiver through a built-in IEEE-488 interface. However, the test receiver unit also stores internally a variety of test configurations, including automatic sweep. A high-efficiency, low-noise linear power supply allows the receiver to operate over a wide range of input voltages. An optional downconverter, the R-1180, extends the frequency range to 18 GHz. The R-110 test receiver sells for $50,000. The downconverter costs $98,500. The estimated delivery time for both units is from stock to 90 days.

Dynamic Sciences Inc., 19808 Nordhoff Pl., Chatsworth, CA 91311-5009; (818) 718-3100. CIRCLE 467

POWER MODULES OPERATE IN MICROWAVE REGION

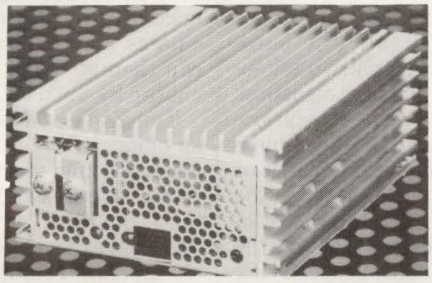
Two series of miniature microwave power amplifier modules are for use in high-power satellite communications equipment. Six different modules provide fixed power outputs of 10 W, 30 W and 50 W in the 1600-MHz region. Three modules, the series STM1628, operate from 1608 MHz to 1628 MHz and the other three, the STM1645 series, work from 1625 MHz to 1645 MHz. All units are for 28-V operation and have 50-Ω input/output impedances.

Key features of the new modules include high-power class C performance, typical power gains ranging from 7.0 to 35.0 dB, and an operating temperature range from –35°C to +70°C. In addition, use of hybrid technology results in small size and light weight and also helps in reducing design and manufacturing time.

Price for the STM1628-10 and STM1645-10 power modules is $90; the STM1628-30 and STM1645-30 series sell for $165. The STM1628-50 and STM1645-50 modules go for $150, all in 1000-unit quantities. Delivery takes about 90 days.

SGS-Thomson Microelectronics, I-20041 Agrate Brianza, Via C. Olivetti 2, Italy; (0039) 39-6035-597. Contact Maria Prestini. CIRCLE 468

300-W SWITCHER IS SMALLEST WITH ONE OUTPUT



The smallest 300-W switching supply with one output is the ALS301, a universal-input model that switches at 200 kHz. The supply, which is only 6.5 in. long, 5 in. wide, and 2.5 in. high, relies on a two-MOSFET forward-converter topology for extremely high efficiency and a power density of 3.7 W/in.^{3}. Available output voltages include 5, 12, 15, and 24 V dc. Production quantities are delivered in 12 to 14 weeks. Call for pricing.

Astec, 401 Jones Rd., Oceanside, CA 92054; (619) 757-1880. CIRCLE 469

UPS COMBINES EFFICIENCY, POWER IN SMALL PACKAGE

An ac/ac uninterruptible power supply provides a 1500-VA supply to maintain a continuous output from switched-mode power supplies and thus keeps key electronic systems operational. The PE5221/10 UPS offers up to 200% overload for 1 s. The new compact design has a 30% higher power density than competitive supplies.

A power-factor correction circuit incorporated in the UPS gives a power factor of 0.99. The power factor correction circuit is a high-frequency switching converter, which, with an adequate control of its duty cycle, can work with an active rectifier, producing a sinusoidal input current, and a pre-regulated output voltage, for example, of 380 V.

The unit's overload capability suits it for starting up devices with high inrush currents. Price is available on request.

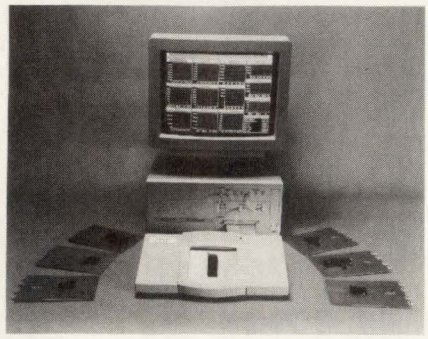
Philips Test and Measurements Div., P. O. Box 218, 5600 MD Eindhoven, The Netherlands; (0031) 40-788620. Contact Christa Horrocks. CIRCLE 470

AFFORDABLE SOFTWARE MANAGES EDA DATA

The EDMVault data-management software from Computervision is available until the end of the year for the entry-level price of $24,900. This new price makes data management an affordable option for 5- to 25-seat engineering departments. The entry-level EDMVault software runs on Sparc-based workstations and servers and supports one user at a time. It's accessed via EDMClient software, an interface from users' workstations to the EDM system. Benefits of the EDMVault system include ensuring that all engineers are working on correct versions of data, that access to the data is limited to appropriate personnel, and that design approvals and release procedures are implemented. EDMVault also supports automatic data backup and recovery. Users can upgrade their entry-level, single-user software within a year for an EDMVault system that supports many users simultaneously.

Computervision, a Prime Co., 100 Crosby Dr., Bedford, MA 01730-1480; (617) 275-1800. CIRCLE 471

CREATE ANALOG BEHAVIORAL MODELS WITH REAL-LIFE MEASUREMENTS



The ModelStation from Zeelan technology lets engineers create accurate analog and mixed analog-digital models in hours using data measured from physical devices under actual operating conditions. The product consists of a stimulus and acquisition system attached to an industry-standard workstation, intelligent test fixtures, and an analysis software package. ModelStation supports analog behavioral models, Spice macromodels, and Spice primitive models that can be used with a variety of popular simulators. In addition, prototype verification is supported through the direct comparison of simulated results with actual prototype performance.

The ModelStation combines hardware that exercises devices under real-life conditions, and software that controls the hardware and then automatically extract mathematical models from the data. Four main elements comprise ModelStation. The first is the ModelStation Mainframe, the hardware that generates signals to stimulate an actual device and then measures the device's response. Also, MasterModel extraction packages are combinations of intelligent fixtures for test of various classes of devices, plus the software to control them and extract models. A workstation or PC acts as the host computer, and helps in specifying parameter ranges, storing data, and extracting the model from measured data. A display shows input waveforms, response waveforms generated by the device, model coefficients, and the system's curve-fitting of the model to the response curve.

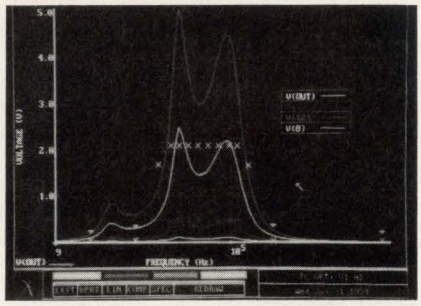
To develop a model, users insert a sample of the required device into the fixture and complete a short menu-based set-up routine specifying operating voltages, output loads, and other operating parameter ranges. The system generates appropriate pulses, measures the device response, and calculates model parameters. The model can then be extracted to the accuracy chosen by the user.

The Zeelan ModelStation will start shipping in the first quarter of next year. Pricing starts at $80,000. Additional releases next year will include Spice device-level models for discrete and active components.

Zeelan Technology, 8305-D S.W. Creekside Pl., Beaverton, OR 97005; (503) 520-1000. CIRCLE 472

■ *LISA MALINIAK*

ANALOG OPTIMIZER AND SIMULATOR RUNS ON PCS



The PC-OPT+ circuit optimization and simulation tool, which runs on PCs, determines the best values for a set of circuit parameters to ensure that the circuit meets target specifications. Specifications can consist of target values for the response or can be in terms of upper and lower limits on a response. Graphical specification entry lets users draw the time or frequency response they want to achieve. The tool's simulator provides Spice-like simulation across the ac, dc, and time domains. The PC-OPT+ software is packaged in a graphical, mouse-driven environment. It accepts standard Spice net lists. In addition, it is net-list compatible with other PC-based circuit simulators and can interface to schematic-capture programs that output Spice files. PC-OPT+ is shipping now and sells for $1695. Quantity discounts are available. A free demonstration kit, including a disk, is available by calling the company.

Electrical Engineering Software Inc., 4675 Stevens Creek Blvd., Suite 200, Santa Clara, CA 95051; (408) 296-8151. CIRCLE 473

DIAGNOSTIC SOFTWARE RUNS UNDER WINDOWS

QAPlus/WIN is an extension of a previous diagnostic product that now runs under Windows 3.0. The software helps users analyze, test, and tune their systems for optimum performance. It also helps to access and edit files that require alterations when problems occur. More than 40 screens, including system configuration and performance and Windows information and resources, let users view and edit files that can be accessed by a mouse or hot keys. Context-sensitive help files are readily available throughout the program. QA-Plus/WIN is available now for $159.95.

DiagSoft Inc., 5615 Scotts Valley Dr., Number 140, Scotts Valley, CA 95066; (408) 438-8247. CIRCLE 474

SOFTWARE HELPS USERS DESIGN FOR QUALITY

Engineers can design products for manufacturing and quality using the Simultaneous Engineering Design System (SEDS) from Pacific Numerix that combines the company's pc-board analysis tools into one system. SEDS provides software for thermal, vibration, fatigue, soldering, and transmission-line analysis. In addition, this analysis can take place before the board is routed. The company claims that when products are run through the system, they will pass through manufacturing easier and will be of higher quality. SEDS runs on all Unix workstations that use the X-Windows and Motif standards. Pricing starts at $20,000 for a standalone system and $30,000 for a network version of the system.

Pacific Numerix, 1200 Prospect St., Suite 300, La Jolla, CA 92037; (619) 587-0500. CIRCLE 475

REAL-TIME OS RUNS ON STD BUS

The QNX real-time operating system takes on modular, reliable, and cost-effective applications on the STD bus. QNX, previously available for the PC bus, is a Unix-like multitasking, multiuser OS that can be networked using WinSystems' STD-AT platforms. Up to 57 users can run 250 concurrent tasks. Each task takes 76 μs to switch on a 16-MHz 386 computer. QNX uses a 16-level prioritized time-slice scheme with preemptive scheduling. Distributed processing is done over an Arcnet token-passing network. Tasks can reside on any node. The software costs $595. The run-time version, without documentation, sells for $550.

WinSystems Inc., 715 Stadium Dr., Suite 100, Arlington, TX 76011; (817) 274-7553. CIRCLE 476

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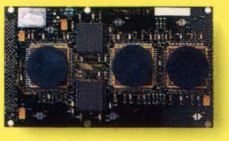

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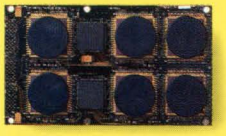

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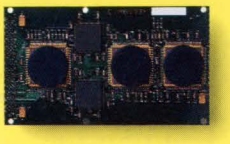

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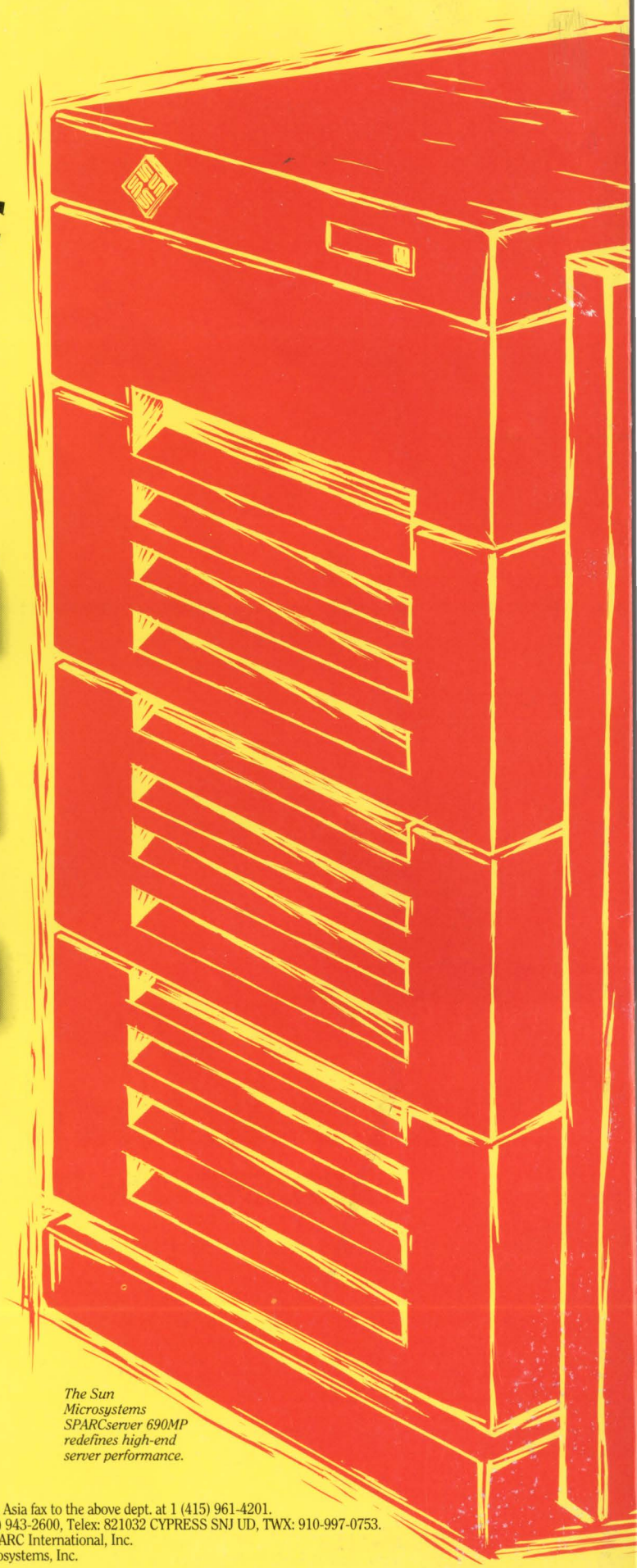

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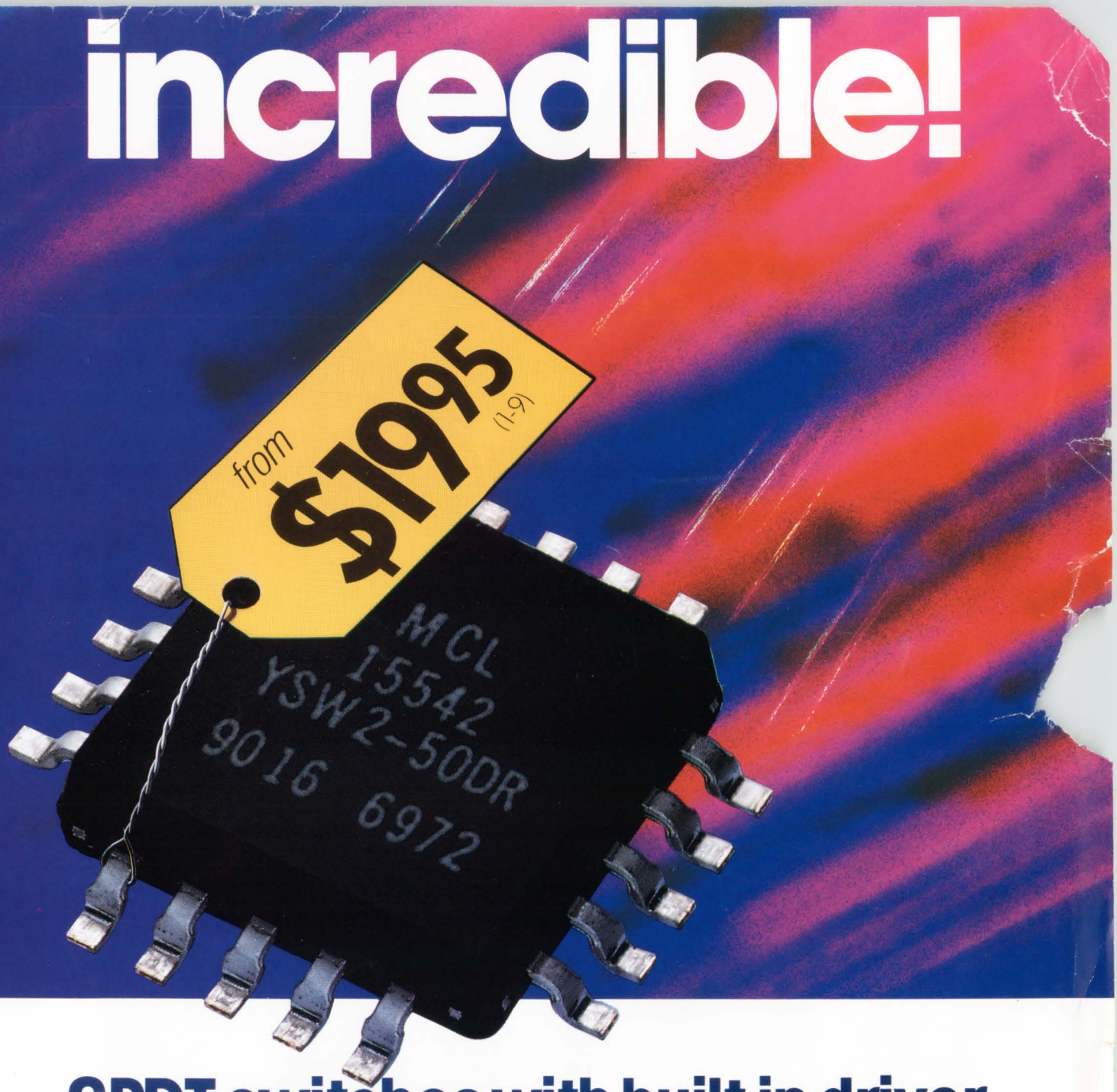

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