CASE AIDS IN OBJECT-ORIENTED PROGRAMMING

SIMULATE AUDIO TRANSDUCERS WITH SPICE

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

ELECTRONIC DESIGN

A PENTON PUBLICATION U. S. $10.00 NOVEMBER 7, 1991

PICK THE RIGHT TOOL FOR YOUR PLD OR FPGA DESIGN

•LOW-POWER 386 CPU WORKS FROM JUST 3.3 V

QUICK LOOK

THIS IS A BIG TIME GAL.®

Time is finally on your side. Our new **GAL20RA10-15**, with ten individually programmable clocks and a 15ns propagation delay, offers the world's fastest performance. A combination that delivers the ultimate in design flexibility and speed, all in a 24-pin E²CMOS® GAL device.

For example, design engineers can independently clock, reset and preset each of ten output logic macrocells. These individually programmable clocks enable asynchronous designs, taking your system performance to even higher levels.

If your design is ready for the big time, call **1-800-FASTGAL**, and ask for dept. 203. We'll send you free samples and a data-book describing our entire line of high speed E²CMOS GAL devices. Fast.

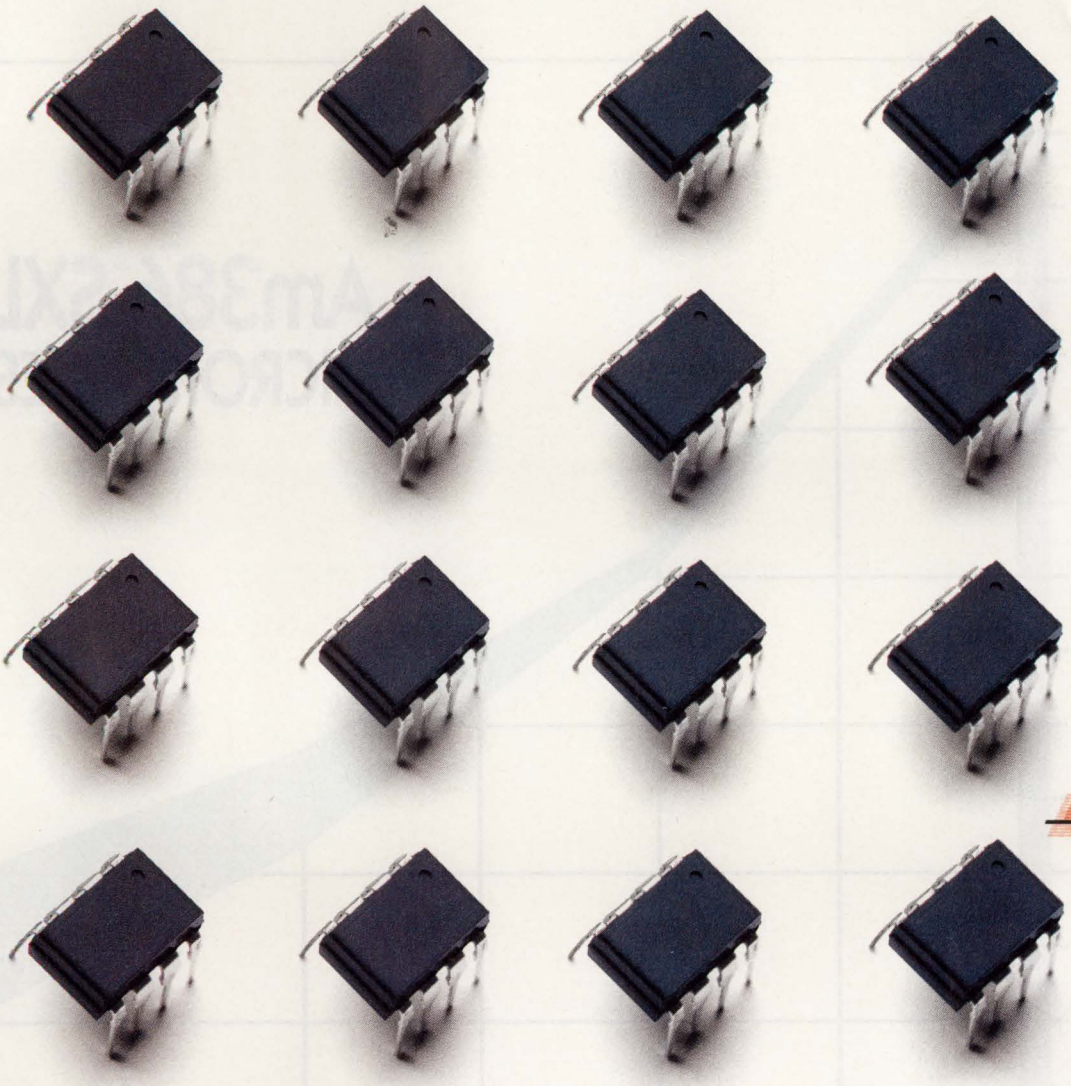
Lattice Semiconductor Corporation™

5555 Northeast Moore Court • Hillsboro, Oregon 97124

Leader in E²CMOS PLDs.™

CIRCLE 214 FOR U.S. RESPONSE CIRCLE 215 FOR RESPONSE OUTSIDE THE U.S.

No two alike.



VALUE
HAMILTON/AVNET

While HP's high-performance plastic optocouplers may all look alike, the similarity is only skin deep.

Because as the largest optoelectronic supplier in the U.S. and one of the world's leading suppliers of optocouplers, we can actually offer you six completely different lines of plastic devices with an equally wide range of performance options. That includes our breakthrough CMOS optocoupler, the world's fastest.

Such as an innovative dual-channel design that combines a photon-emitting diode with a high-speed photon detector to produce data rates up to 65 MBd.

You also get high-output gain from low-input current or high-speed logic gates. Wide Vcc from 4.5 to 20 volts. And a unique AC/DC interface.

Plus, they're compatible with TTL, STTL, LSTTL, and, in many cases, CMOS logic families.

All of which makes HP's optocouplers the ideal solution for problems caused by ground loops and induced common mode noise.

No wonder HP sets the standard for quality, reliability, and innovation. To find out more about HP's optocouplers and the name of your nearest Hamilton/Avnet location—HP's largest electronic components distributor—call **1-800-752-0900, ext. 2717.**

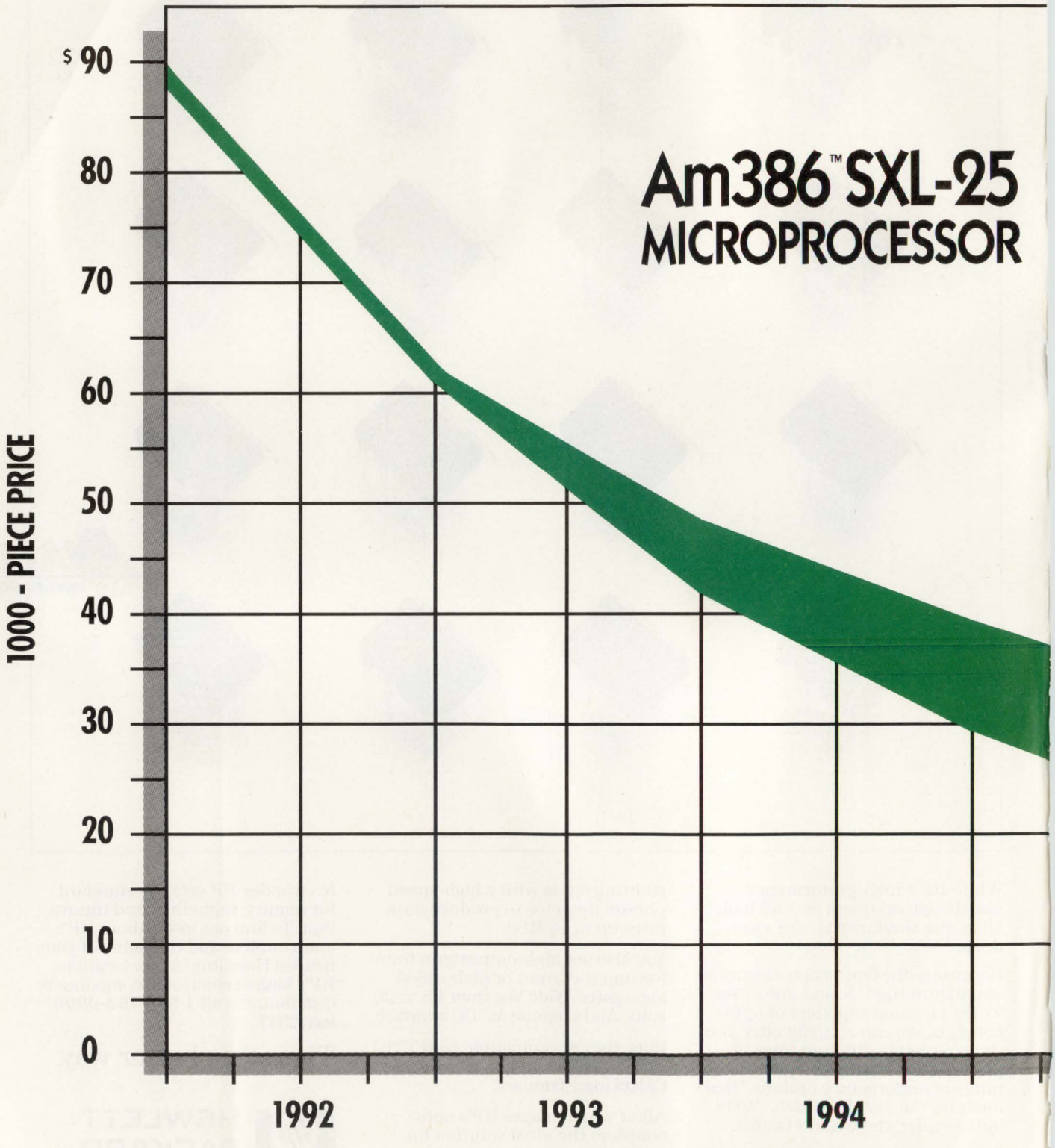
There is a better way.

HEWLETT PACKARD

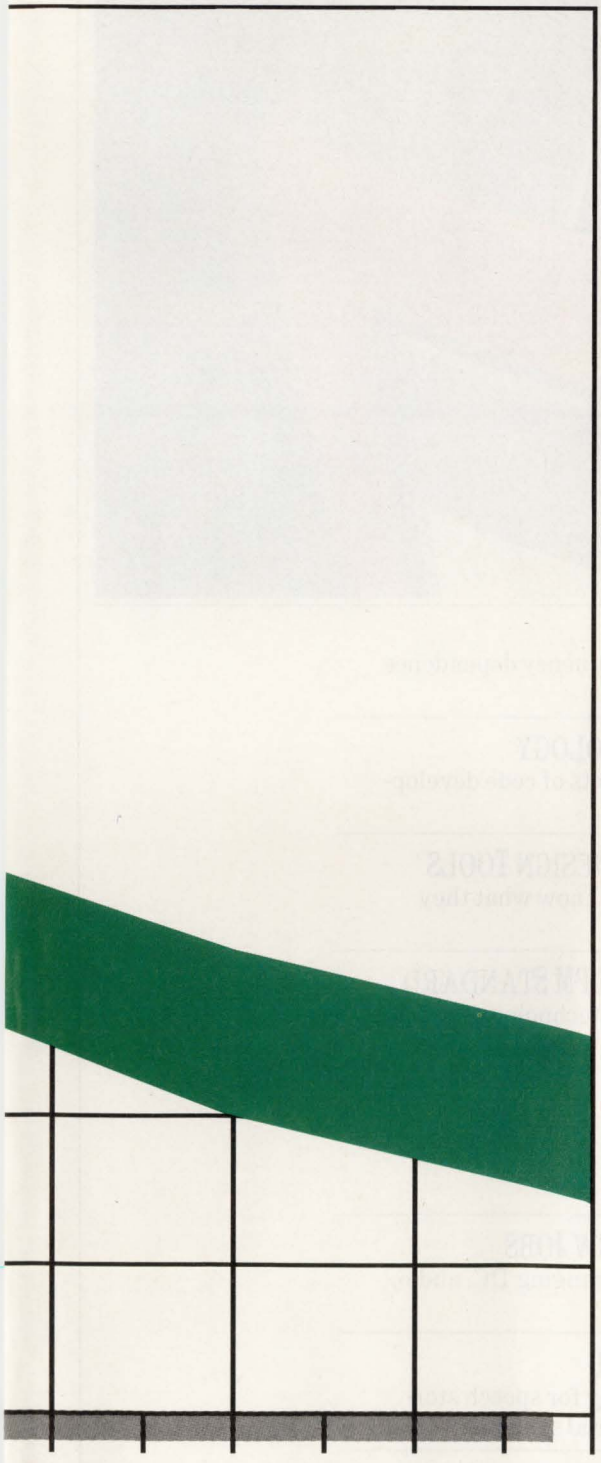
CG08907A/HA1

CIRCLE 194

The Microproces



sor For The Masses.



AMD Reintroduces Learning Curve Pricing With The Am386™ SXL-25 Microprocessor.

It's no ordinary 386SX.

It's the Am386SXL-25 microprocessor. A higher speed, lower power, plug-in replacement for the 386SX microprocessor.

And with it, AMD resurrects learning curve pricing.

That means aggressive, predictable price reductions between 20% and 30% each year.

Best of all, it's available today, available in quantity, and available to everyone.

That's why the Am386SXL-25 CPU is *the microprocessor for the masses.*

To get your hands on your own supply of Am386SXL-25 microprocessors, call AMD today at **1-800-222-9323.**

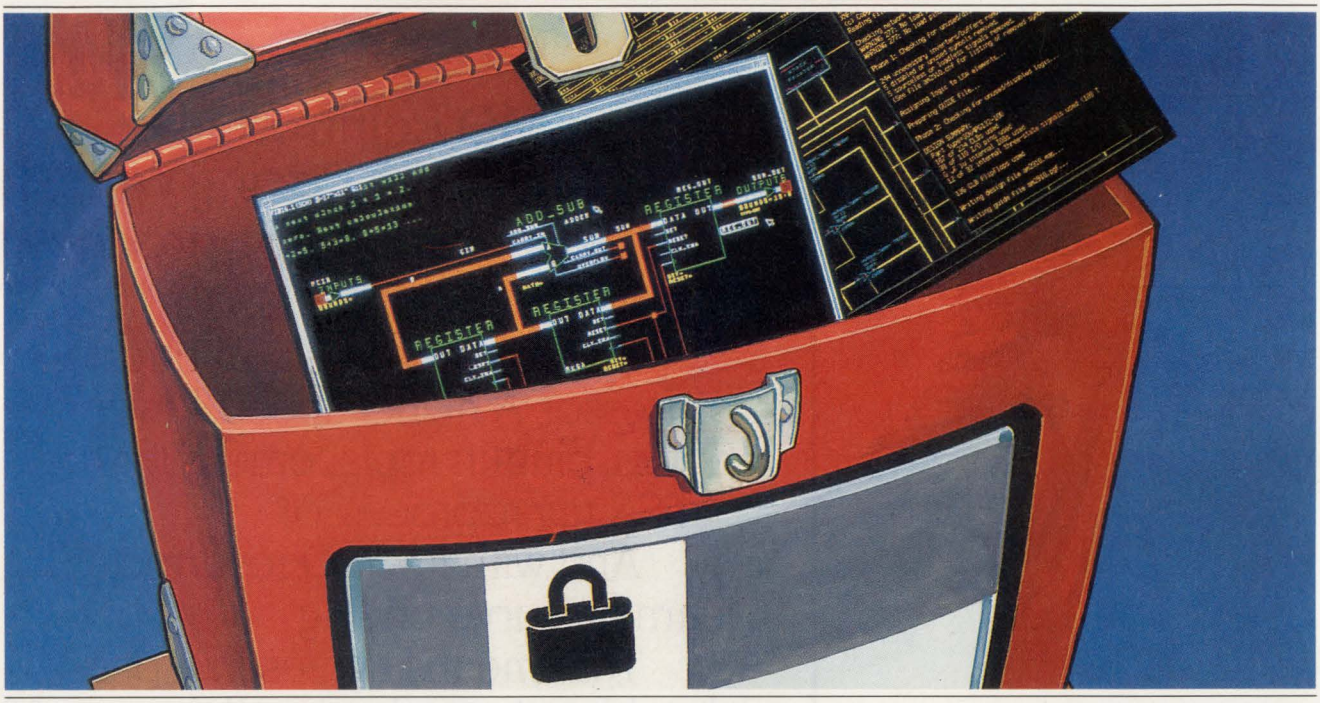
Advanced Micro Devices

"We're Not Your Competition."

CIRCLE 82 FOR U.S. RESPONSE CIRCLE 83 FOR RESPONSE OUTSIDE THE U.S.

NOVEMBER 7, 1991 VOL. 39, NO. 21

ELECTRONIC DESIGN



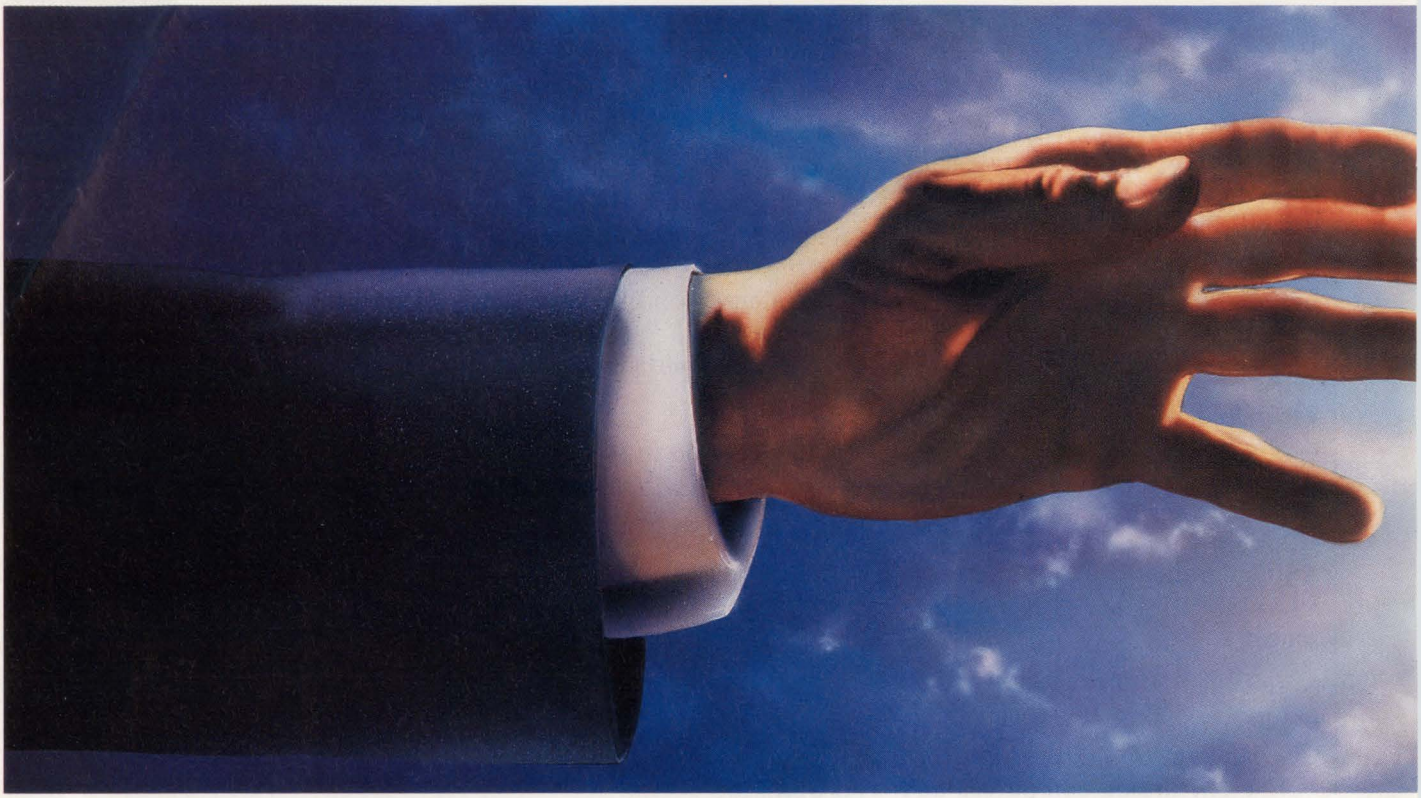
COMING NEXT ISSUE
- A survey of system designers' use of mixed-signal ASICs
- New FPGAs smooth transition to gate arrays
- How to goof-proof your clock circuits
- Cut I/O transfers with an I/O cache
- Easing x86-based designs with new standard-cell libraries
- Gyroscope design revolutionizes pointers for 3D screen images
- First details on new VHDL tools that span specification to test
- A preview of upcoming Wescon technical papers and products
- Evaluating the properties of piezoelectric polymer films
- Special Section: PIPS—Power, Interconnections, Passive Components, Switches and Relays
- Choosing the right substrate for a multichip module
- A survey of manufacturers of electronic packaging and materials
- PLUS:
Ideas for Design
Pease Porridge
Technology Advances
QuickLook

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published semi monthly by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $85 U.S., $160 Canada, $230 International. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204.

For subscriber change of address and subscription inquiries, call (216) 696-7000.

POSTMASTER: Please send change of address to ELECTRONIC DESIGN, Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543.

SIEMENS



Global Reach.

Siemens provides an extensive range of reliable advanced semiconductors for companies that manufacture and market worldwide.

For organizations with worldwide marketing and manufacturing interests, it is essential to have a global supplier who is responsive to your needs. Siemens is that partner, with the worldwide products, services and accessibility which has made us a leader in supplying solutions to organizations with global requirements.

Innovative 8-bit microcontroller designs.

With 197 manufacturing plants in 37 countries, Siemens provides world-class service, support, and manufacturing capabilities. And we back this commitment with over $40 billion in financial strength, as well as quality components, from the most common to the most technologically advanced ICs on the market. Complete with the European content you need to stay competitive in the World Market of 1992.

Temperature and voltage protected power transistors.

Siemens has a reputation for innovative, reliable products spanning a variety of markets. And our latest advancements prove that we're keeping that innovation alive, supplying state-of-the-art solutions which can put the answer to your IC problem within reach.

Siemens offers the most comprehensive communication IC family in the world, which includes innovations such as the industry's first single-chip solution in CMOS for echo cancellation circuit functions in ISDN. And all our

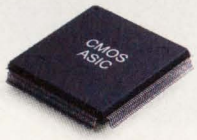
communication ICs feature ISDN Oriented Modular Architecture (IOM®), the de facto industry standard pioneered by Siemens. Providing you with complete IC solutions which ease the incorporation of data, speech and graphics.

High-integration echo cancellation transceiver for ISDN.

We're also the only European DRAM manufacturer, providing high-quality 1-Mb and 4-Mb DRAMs. They're available worldwide and in volumes which have doubled since 1989. In fact, we're becoming one of the world's leading DRAM suppliers, and are continuing to develop advanced DRAM technology with our 16-Mb and 64-Mb DRAM programs.

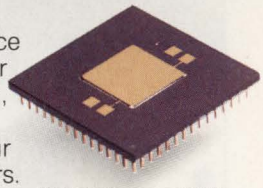
Reliable 1-Mb and 4-Mb DRAMs.

Siemens CMOS ASIC technology features both Sea-of-Gates and standard-cell product families. Our 1.5, 1.0 and sub-micron technologies are compatible with Toshiba even at the GDS2 database level, for true alternate sourcing worldwide. And they're fully supported by our ADVANCAD and industry-standard workstations and simulators, as well as the best service in the industry.



ASIC solutions in both Sea-of-Gates and standard-cells.

Plus, we supply the MIPS RISC microprocessor family, the only 32-bit CMOS microprocessors with five certified sources. Our superior manufacturing processes produce devices with lower power dissipation, and finer performance within your design parameters. And we're the sole European supplier for these devices, which are ideal for workstations, file servers and multiprocessor systems, as well as embedded control applications.



High-performance 32-bit RISC microprocessors.

For details on our world-class products, call **(800) 456-9229**. Or write:

Siemens Components, Inc.
2191 Laurelwood Road
Santa Clara, CA 95054-1514.

Ask for literature package M11A 012.

Siemens
World Wise, Market Smart.

CIRCLE 168 FOR U.S. RESPONSE
CIRCLE 169 FOR RESPONSE OUTSIDE THE U.S.

ELECTRONIC DESIGN

Editor-in-Chief: Stephen E. Scrupski

Executive Editor: Roger Allan

Managing Editor: Bob Milne

Senior Editors: Frank Goodenough, Milt Leonard, John Novellino

Technology Editors:
Analog & Power: Frank Goodenough
Communications & Industrial: Milt Leonard (San Jose)
Components & Packaging: David Maliniak
Computer-Aided Engineering: Lisa Maliniak
Computer Systems: Richard Nass
Semiconductors: Dave Bursky (San Jose)
Software: Sherrie Van Tyle
Test & Measurement: John Novellino

Field Bureaus:
West Coast Executive Editor: Dave Bursky (San Jose)
Boston: Lawrence Curran
Dallas: Jon Campbell
Frankfurt: John Gosch
London: Peter Fletcher

Chief Copy Editor: Roger Engelke, Jr.

Contributing Editors: Ron Kmetovicz, Robert A. Pease

Editorial Production Manager: Lisa Iarkowski

Production Coordinator: Pat A. Boselli

Associate Art Director: Tony Vitolo

Staff Artist/Designer: Tom Pennella

Editorial Support Supervisor: Mary James

Editorial Assistant: Ann Kunzweiler

Editorial Secretary: Bradie Guerrero

Editorial Offices: (201) 393-6262

Advertising Production: (201) 393-6093 or FAX (201) 393-0410

Production Manager: Michael McCabe
Production Assistants: Donna Marie Bright, Lucrezia Hlavaty, Eileen Slavinsky

Circulation Manager: Robert Clark

Promotion Manager: Clifford Meth

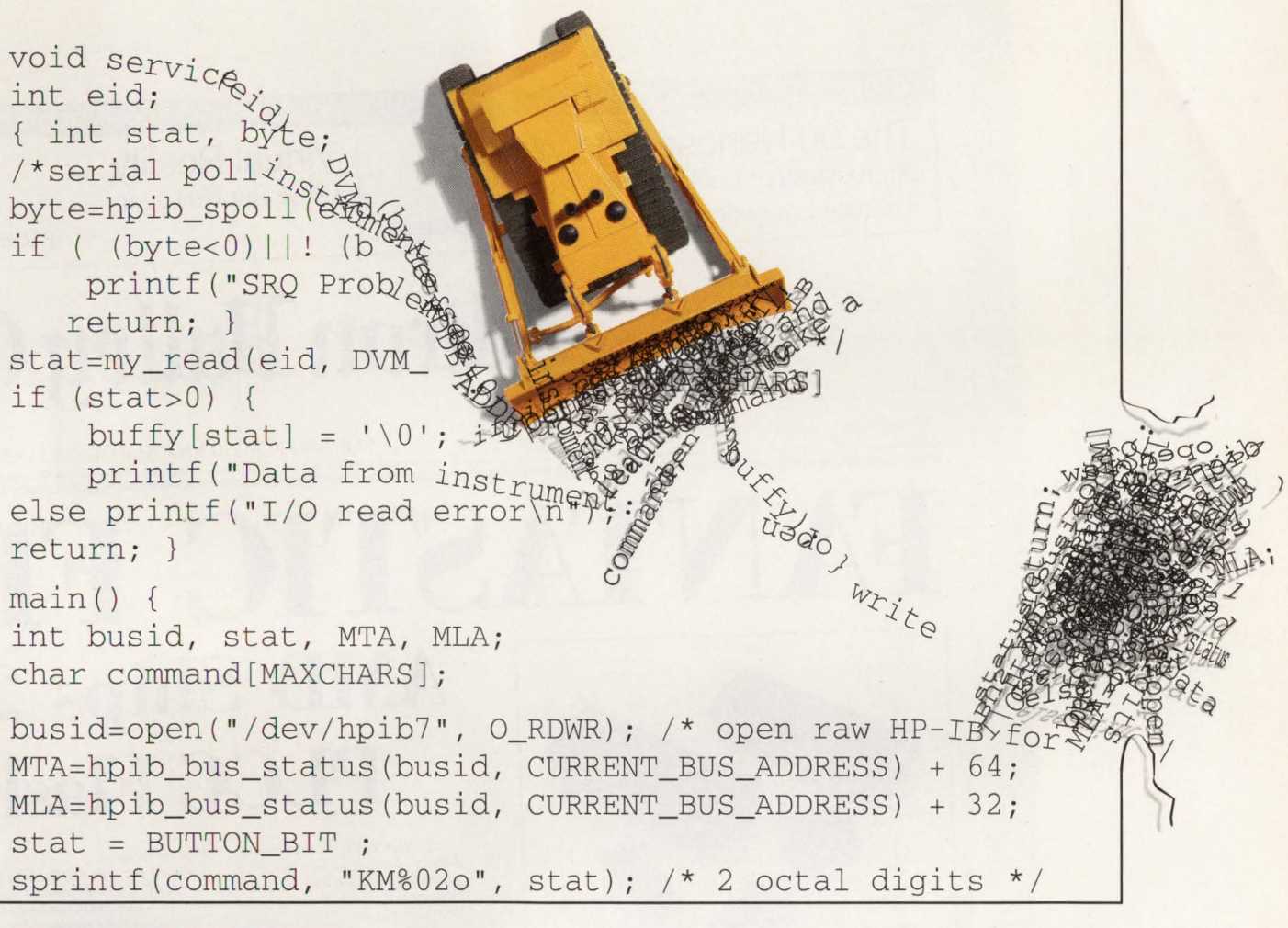
Reprints: Helen Ryan 1-800-835-7746

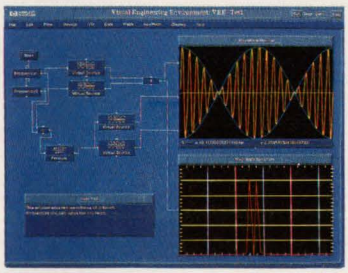
Group Art Director: Peter K. Jeziorski

Published by Penton Publishing
Vice President-Editorial: Perry Pascarella

Publisher: Paul C. Mazzacano

Finally, engineering software that clears the way to problem solving without programming.





With HP VEE, you simply link the icons.

Computers are great for problem solving, if only programming didn't get in the way and slow you down. And now, it doesn't have to. Because the HP visual engineering environment (HP VEE) lets you solve problems without programming.

With HP VEE, you explore solutions visually by arranging and linking icons on the CRT. Each icon represents and executes a specific function for data collection, analysis—from simple mathematics to complex algorithms—and presentation. You don't have to write a single line of code.

There are two HP VEE software packages for prototyping, experimentation, and problem modeling. HP VEE-Engine, at $995*, is a general-purpose tool for analysis and presentation of existing data. HP VEE-Test includes HP VEE-Engine and adds extensive I/O capability, including soft panels and device I/O objects for $5,000*.

So, if programming is keeping you from solutions, call **1-800-752-0900.** Ask for **Ext. 2382**, and we'll send a brochure on clearing the way with HP VEE.

* U.S. list prices.

There is a better way.

HEWLETT PACKARD

CIRCLE 190 FOR U.S. RESPONSE

CIRCLE 191 FOR RESPONSE OUTSIDE THE U.S.

News Flash

SPORTS

The 90 Nanosecond Workout
An Exhaustive Look At High Tech Training Equipment
PAGE 2B

SCIENCE AND TECHNOLOGY

Virtual Reality
Close But No Cigar
PAGE 8H

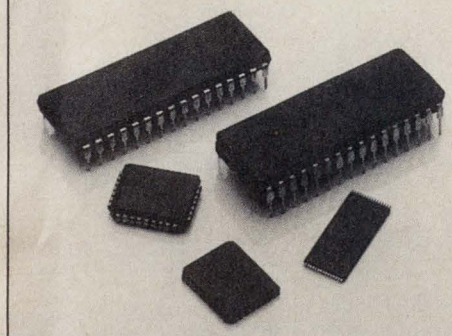
Silicon Valley G

25 CENTS

SERVING NORTHERN CALIFORNIA SINCE 199

FANTASTIC FL

AMD Ships 2 PLCC Flash



How Fast Is A Flash? A Direct Comparison

Density	AMD	Fastest Competitor
256K	90ns	120ns
512K	90ns	120ns
1 Mbit	90ns	120ns
2 Mbit	90ns	150ns

SUNNYVALE — The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc.

Flash memory is a high-density, reprogrammable, non-volatile technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications.

Flash memory also has the potential to eliminate mechanical hard disks and the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook computer applications.

Today, Flash memory is the most cost effective replacement technology for UV EPROMs and EEPROMs in applications that require in-system programming. Flash memories can literally be reprogrammed in a flash — hence the name.

Standard, But With A Little More Flash

AMD's Flash memory family effectively etches in silicon the de-facto standard for this burgeoning technology that is compatible with Intel's initial Flash architecture.

Because AMD Flash memories are pin-for-pin compatible with the now standard architecture, AMD is positioned as an alternate source for design engineers and purchasing agents alike.

"Alternate source may be an inadequate term," said Jerry Sanders, chairman and CEO of Advanced Micro Devices. "Given our speed and feature set, our customers think of us as a superior resource."

Indeed, AMD's Flash memory family offers designers significant performance advantages (see chart), with speeds almost twice as fast as the nearest competitor.

Engineer Spontaneously Combusts At Meeting

Vice Pre

From AMD.

FOOD

Chips And Salsa

A Business Person's Guide To Silicon Valley Restaurants

PAGE 7F

tzette

MORNING EDITION

ASHES!

Megabit, 90ns, Memories

The AMD Flash family offers designers and purchasers many packaging options. Particularly popular is AMD's advanced 2 Megabit, PLCC part. Other packaging options include PDIP, CDIP and LCC in 256K, 512K, 1 Mbit and 2 Mbit capacities. TSOP packages will be available in the second half of this year. (LCC not currently available in 2 Mbit.)

AMD's 2 Mbit Flash memories come complete with embedded program and erase algorithms on board. These automatic algorithms speed up the design process and considerably shorten time to market. Previously, engineers were required to develop tedious and time-consuming algorithms to implement in-system reprogrammability. AMD's automatic algorithms also allow several Flash memories to be written or erased at once, without tying-up the CPU. The system is now free to perform other tasks while these operations are in progress. AMD plans to include embedded algorithms in a future release of its 1 Mbit part.

The Ultra-Violet Blues

Flash technology is particularly suited to applications requiring reprogramming in place, because these devices can be reprogrammed in seconds, and within the system.

To update the code on a UV EPROM, the part must first be removed from the system. Once removed, erasure can take up to a full 20 minutes. After reprogramming, the part is then plugged back into the system. The process can result in damage to other components, costly service calls, and headaches.

Flash memories, on the other hand, can be bulk erased in about one to two seconds, without system disassembly. Reprogramming can then be accomplished via floppy disk, over phone lines, or even ISDN

(continued)

sident To Speak

Stop the presses!

Advanced Micro Devices makes big news again—this time with an enhanced family of Flash memory devices.

That's good news for veteran and new Flash users alike.

Because our Flash devices are pin-for-pin compatible with Intel's existing Flash memory architecture, they establish the *de facto* industry standard.

Our standards, however, are a bit higher.

And so are yours.

That's why our Flash Memory family offers densities, speeds and packaging options that improve performance and save board space. For instance, our advanced 2 Mbit PLCC part with a scant 90 nanosecond delay.

You can also choose from Flash devices in 256K, 512K and 1 Mbit densities. As well as packaging options that fit your design best, including CDIP, PDIP, LCC, TSOP, and PLCC.

And you'll find implementation faster and easier than ever, because we've included automatic programming algorithms on all our 2 Mbit devices, and soon on our 1 Mbit parts, too. So you'll spend less time writing code, and take less time getting products to market.

To keep up to date with all the latest and greatest in Flash memory, call AMD today at **1-800-222-9323.** And start making some headlines of your own.

Advanced Micro Devices

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088.

CIRCLE 186 FOR U.S. RESPONSE CIRCLE 187 FOR RESPONSE OUTSIDE THE U.S.

Tapping the power of

today's fastest CPUs.

That's AT&T "Customerizing."

"Customerizing" means providing the component solutions and support technology your systems need to help keep pace with CPU speeds up to 50 MHz and beyond.

Faster CPUs demand higher-performance cache, I/O bus, peripheral logic and interconnect: bigger, faster, denser, smarter. We have what it takes to close this CPU I/O gap, while reducing chip count and development costs.

CPU/Logic and Bus Solutions

Industry-pacing submicron Standard Cell CMOS ASICs for high speed, highly integrated core logic.

ECL ASICs with up to 2.2 GHz I/O buffer speeds and delays under 140 ps.

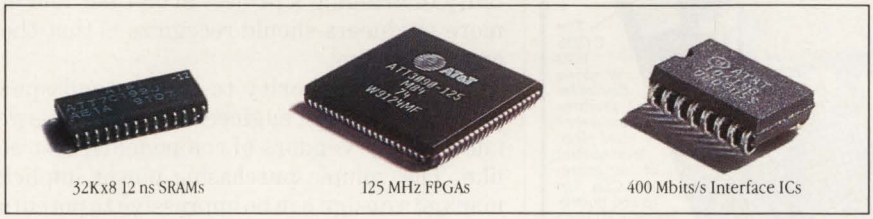
High speed bus interfacing with 200-400 Mbits/s 41-Series Interface ICs.

And custom clocks to meet the tight timing specs of today's fastest CPUs.

Cache Solutions

Microprocessor-specific, fast SRAMs for 10 to 15 ns cache tag and data.

And a proven ASIC capability for differentiated Cache Controllers.



32Kx8 12 ns SRAMs | 125 MHz FPGAs | 400 Mbits/s Interface ICs

Interconnection Solutions

Up to 22-layer PC Boards with 5 mil line density.

And Multichip Modules that can reduce interchip delays to under 1 ns.

AT&T also provides Application Teams to work with your team, along with the expertise of AT&T Bell Laboratories.

For more about AT&T's "One-Stop-Shop Solutions," get our PC/Workstation Solutions brochure.

Just give AT&T Microelectronics a call at **1 800 372-2447, ext. 636.**

In Canada, call: **1 800 553-2448, ext. 636.**

AT&T Microelectronics

CIRCLE 96 FOR U.S. RESPONSE

CIRCLE 97 FOR RESPONSE OUTSIDE THE U.S.

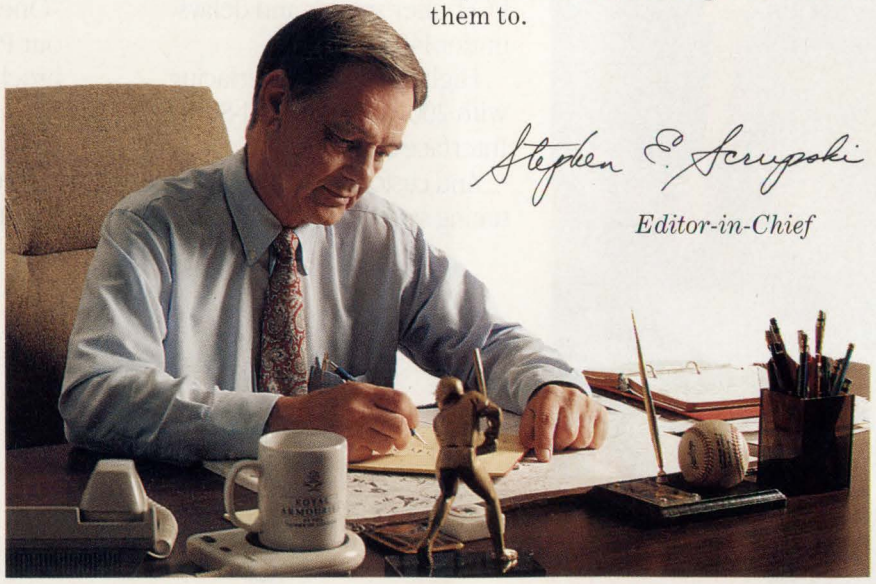
LET THE HORNS BLOW

Most design engineers focus their best efforts on the difficult technical problems they face in getting their designs to meet performance specifications. They spend much of their day investigating ways to improve their designs, juggling the benefits and drawbacks of making mid-project design changes when a clearly better component suddenly appears, all the while hoping that the delivery promises made by their key suppliers will be kept. Few engineers have the time or the inclination to become involved in company politics, or blow their own horns outside their companies. Such self-centered characteristics are foreign to most engineers – they are basically technology-oriented in their approach to the job, and that's the way it should be.

However, it's still true that engineers are sometimes a little too retiring, sometimes too focused on the technical aspects of the job, and they can suffer a loss of prestige from all this modesty. Most engineers know that they have clout within their own companies because they have been given the responsibility of bringing a project in on time, and on budget. However, what many more engineers should recognize is that they have clout outside their own companies, too.

With the authority to recommend specific vendors for high-volume purchases, design engineers are prime targets of the marketing campaigns launched by vendors of components, test equipment, subsystems, and the like. The volume purchasing power implicit in an engineer's authority to manage a design can be impressive to potential suppliers. With their detailed knowledge of what will work and what won't, engineers have expert opinions about trends in technology that are highly sought after by market researchers. Engineers also are often their company's best representatives in dealing with customer problems, because the combination of their technical knowledge and authority to change something to satisfy customers is unmatched within most companies.

We would like to see more of that well-known engineering judgment and confidence in their own abilities applied to the problems that engineers face in pursuing their careers. Medical doctors and lawyers seem always ready to use their clout to speak out about trends they deem harmful to their professions and, of course, to their livelihoods. Engineers – and the organizations that represent them – are going to have to learn a little more about horn-blowing if they want to achieve all that their education, hard work, and innate intelligence entitle them to.



Stephen E. Scrupski

Editor-in-Chief

SPDT & SP4T SWITCHES

WITH BUILT-IN DRIVERS

10 to 3000MHz from $39.95

Now, high-speed, high-isolation switches with with built-in drivers, tough enough to pass stringent MIL-STD-202 tests. There's no longer any need to hassle with the complexities of designing a TTL driver interface and then adding yet another component to your subsystem... it's already included in a rugged, low-cost, compact assembly. Available in the popular hermetically-sealed TO-8 package or a small EMI-shielded metal connectorized case, these tiny PIN-diode reflective switches, complete with driver, can operate over a 10 to 3000MHz span with a fast 2μsec switching speed.

Despite their small size, these units offer isolation as high as 40dB(typ), insertion loss of only 1.1dB(typ), and a 1dB compression point of +27dBm over most of the frequency range. All models are TTL-compatible and operate from a dc supply voltage of 4.5 to 5.5 V with 1.8mA quiescent current. Switch to Mini-Circuits for highest quality innovative products... and leave the driving to us.

SPECIFICATIONS

	TOSW-230 ZFSW-230DR		TOSW-425 ZFSW-425DR	
Freq. Range(MHz)	10-3000		10-2500	
Insert. Loss (dB)	typ.	max.	typ.	max.
10-100MHz	1.3	1.9	1.3	1.7
100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ.	max.	typ.	max.
	1.3	1.6	1.3	1.6
Switching Time (μsec) (from 50% TTL to 90% RF)	typ. 2.0	max. 4.0	typ. 2.0	max. 4.0
Oper. Temp.(°C)	-55 to +100		-55 to +100	
Stor. Temp.(°C)	-55 to +100		-55 to +100	
Price (10-24)	$39.95		$59.95	
(1-9)	$89.95		$109.95	

finding new ways...
setting higher standards

Mini-Circuits

A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156

WE ACCEPT AMERICAN EXPRESS

CIRCLE 130 FOR U.S. RESPONSE

CIRCLE 131 FOR RESPONSE OUTSIDE THE U.S.

F126 REV. A

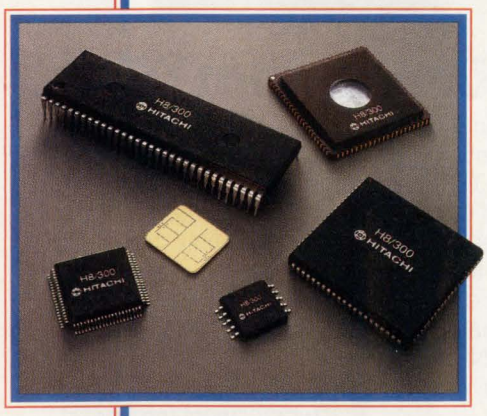
When it comes to microcontrollers...
The Choice Is Not Always Plain.

Hitachi's new H8/300 Family of 8-Bit Microcontrollers is beefier, and includes all the extras: The best in price/performance. High-level language capability. ZTAT™ one-time user-programmable EPROM. The most on-chip peripherals.

Hitachi's new and growing H8/300 Family of Microcontrollers takes 8-bit beyond the ordinary, offering the right mix of ingredients to satisfy your embedded-control appetite. Hitachi's new H8/300 Series' recipe for success includes:

The best price-performance. Put more spice into your applications with the new CMOS H8/300 Family. These microcontrollers combine a modern, general-purpose register architecture with fast processor speeds, and include a CPU core with a maximum 10 MHz clock speed for minimum instruction cycle times of 200ns... 16-bit adds and subtracts in a mere 200ns... 8 x 8-bit multiplies or 16/8-bit divides in only 1.4µs...and up to 32 Kbytes of ROM.

High level language capability. Enjoy fast development and easy maintenance, without the slow program execution typical of old-fashioned software. Hitachi's H8/300 microcontrollers work with "C", Forth, and real-time operating systems, like Hitachi's µITRON. You can also use fuzzy logic compilers to put advanced capabilities, such as artificial intelligence, into embedded systems—quickly and easily.



ZTAT. Get to market *fast* with Hitachi's ZTAT (Zero Turn-Around Time) one-time user-programmable EPROM. With these low-cost plastic package devices, production can start the very same day you finish development—with no mask charges, lead times, or large quantity commitments. You have a choice for every phase of your product's life cycle: Ceramic windowed devices for development...ZTAT for quick, small-to-medium-scale production...mask ROM devices for lowest-cost large-scale production.

On-chip peripherals. Now you can reduce your whole embedded control system to a single chip, thanks to the H8/300 Family's right mix of on-chip peripherals. Choose from a variety of timers, interrupts, and I/O ports, 8-bit A/Ds, serial communications channels, PWM timers, EEPROM, and much more.

Description	H8/310 Smart-Card IC	H8/322 General-Purpose Real-Time Controller	H8/323 General-Purpose Real-Time Controller	H8/324 General-Purpose Real-Time Controller	H8/325 General-Purpose Real-Time Controller	H8/330 High-End Real-Time Controller	H8/350 Servo-Positioning Controller
ROM/RAM/EEPROM	10K/256/8K	8K/256/0	16K/512/0	24K/1K/0	32K/1K/0	16K/512/0	32K/512/0
Timers		3				5	10
Serial Channel		2				1	2
A/D Converter						8-Bit, 8 Channel	8-Bit, 16 Channel
Interrupts		4 External 16 Internal				9 External 19 Internal	9 External 47 Internal
I/O Ports	1-Bit I/O Common	47 I/O 4 Input Only				58 I/O 8 Input Only	50 I/O 16 Input Only
Other Features	Security Function	Parallel Handshake Port Programmable Pull-up for All I/O				15-Byte DPRAM, Prog. Pull-up for I/O	One 19-Bit Timer, Timer Network
Package	Die Form COB* SOP-10	DP-64S QFP-64 DC-64S w/Window				PLCC-84 QFP-80 LCC-84 w/Window	PLCC-84 QFP-80 LCC-84 w/Window

*Call your Hitachi representative for availability.

Serving it up... The H8/300 Family includes comprehensive development support: Documentation, easy-to-use cross-development tools, in-circuit emulators, and evaluation boards (with additional choices from third-party vendors).

The new Hitachi H8/300 Family of Microcontrollers. We've added all the right ingredients, so your next design can go beyond the ordinary. For more information, call or write today.

Literature Fast Action: For product literature only, CALL TOLL FREE, 1-800-285-1601; ask for literature number M21A001.

For Literature Only Circle #112

To Have a Hitachi Representative Call Circle #113

Hitachi America, Ltd.
Semiconductor & I.C. Division
Hitachi Plaza
2000 Sierra Point Parkway
Brisbane, CA 94005-1819

HITACHI®

Our Standards Set Standards

THE MICROPROCESSOR AT 20

DAVE BURSKY
SEMICONDUCTORS

This week's Microprocessor Forum at the Hyatt Regency Hotel, Burlingame, Calif., marks the 20th anniversary of the microprocessor. Over the last two decades, the microprocessor has evolved from a simple 4-bit PMOS device containing a few thousand transistors to complex 64-bit CMOS, biCMOS and ECL processors, some of which contain several million transistors. During those years, the market has divided into two basic categories – the general-purpose reprogrammable segment and the dedicated, embedded processor segment. In some cases, the same chip is used in both application areas, but often the two areas demand different sets of features and on-chip functions, as well as a re-ordering of performance criteria. Unfortunately, it is becoming harder than ever for a system designer to decide which CPU to select.

Today's reprogrammable devices, the key elements in desktop computers, workstations, and compute servers, range in performance from a few MIPS to close to 50 MIPS. Two trends seem to be emerging. First, architectures in the RISC and CISC worlds seem to be converging, as each type CPU increasingly incorporates similar functions – cache, memory management, floating-point math acceleration, etc. This commonality of functions is making it difficult to distinguish one CPU from another without extensive application benchmarking. Second, both the RISC and CISC worlds have incorporated – or will soon incorporate – such enhancements as superpipelining or superscalar structures to exploit on-chip parallelism and perform multiple instructions during each clock cycle.

Most of the second-generation RISC processors apply superscalar or superpipelining structures to achieve throughputs that in some cases will peak at over 100 MIPS. The forum will highlight some of these latest RISC chips – the "Snakes" CPU from Hewlett-Packard Co., the i860XP from Intel Corp., the 88110 from Motorola Inc., the R4000 from MIPS Inc., the SuperSparc from Texas Instruments Inc., and even yet-to-be released chips such as the single-chip implementation of IBM Corp.'s RISC System 6000. In another session, speakers will project future directions for the Advanced Computing Environment and results from the Apple-IBM alliance.

On the CISC side, the focus turns to the Intel 386/486 family, as well as the alternate sources – the Am386 family from Advanced Micro Devices Inc., the Super386 family from Chips and Technologies Inc., the F86 multichip solution from NexGen Microsystems Inc., and of course new implementations from Intel. Papers will detail improved low-power processors, higher-performance implementations, and even higher-integration solutions such as the all-in-one CPU chip developed by Chips and Technologies for palmtop and embedded applications.

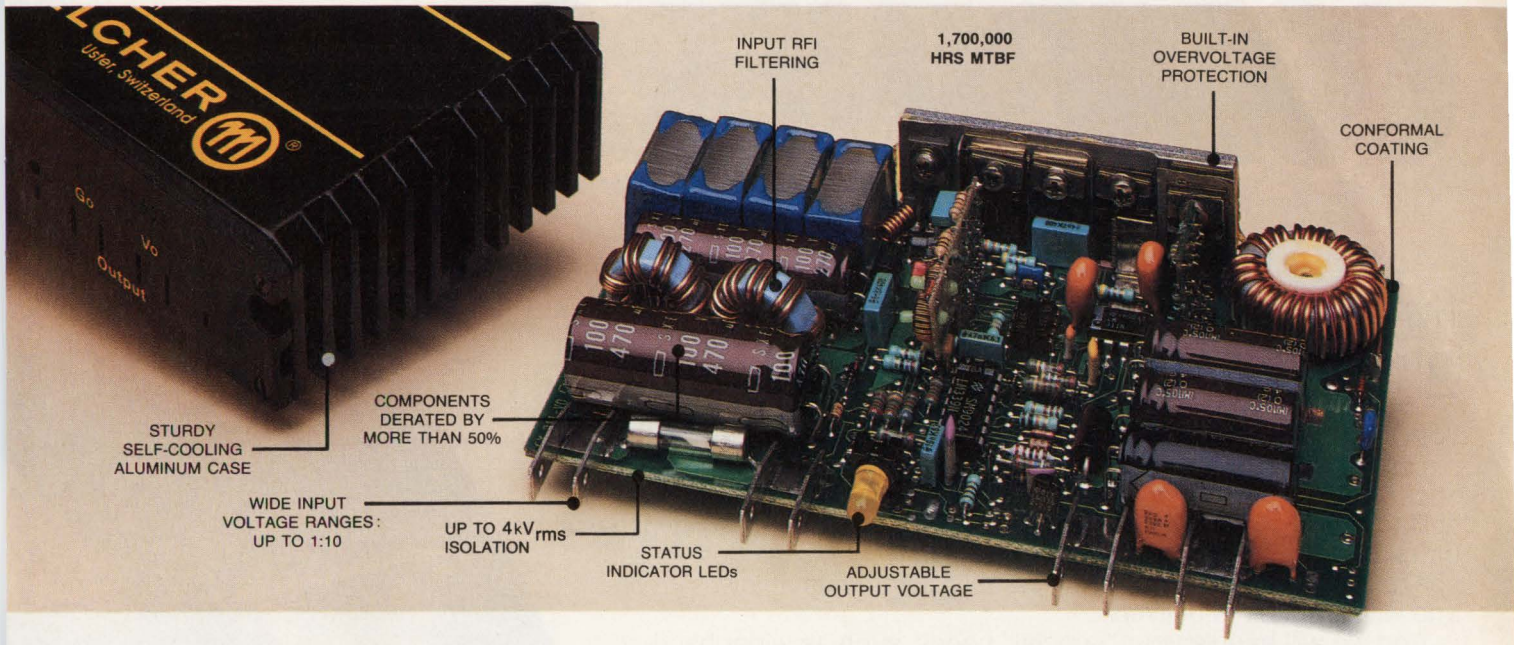
As for embedded processors, four of the latest RISC-based devices will be examined: New versions of AMD's 29000, a new offering from Advanced RISC Machines Ltd. (a startup in England funded by Apple, VLSI Technology, and Acorn Ltd.), an improved version of the i960 from Intel, and a Sparc-family processor for event control from the Advanced Products Div. of Fujitsu Microelectronics Inc.

Finally, the forum also offers an opportunity to step back and view 20 years of microprocessor history and gain perspective on the orders-of-magnitude advances in performance. CPU performance gains have somewhat obviated the need to make a choice based just on performance. Application software choices and time-to-market have become critical decision factors. In the embedded world, easy-to-use development tools and the ability to reuse existing software are being valued more highly as aids to reducing time-to-market.

(Post-conference transcripts of the presentations and related discussions, along with the slides presented during the sessions can be ordered. For details contact The Microprocessor Forum, 874 Gravenstein Highway South, Suite 14, Sebastopol, CA 95472, (707) 823-4004; fax: (707) 823-0504.)

MELCHER Industrial Power Supplies

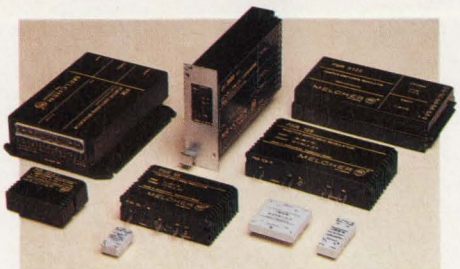
Guaranteed* to function to the outer limits of *heat, cold, voltage & vibration*



When you can't compromise on your power supply, start your search with MELCHER . . . because for almost 20 years, the world's most demanding OEMs have depended on MELCHER's remarkable ability to handle their wide temperature fluctuations, intense shock and vibration and input voltage surges. In fact, MELCHER industrial power supplies can maintain full load capability over an ambient temperature range of −40 °C to +85 °C!

Each MELCHER unit is a total power supply solution — in its own compact, self-cooling, EMI/RFI-shielded aluminum case ready for mounting. And, because shock and vibration tolerance are critical in telecommunications and mobile applications such as rail, air, and shipborne systems, MELCHER power supplies are tested in strict accordance with MIL STD 810 to ensure they'll endure the harsh bumps and shakes many such environments impose. They are also designed with ultra-sophisticated voltage protection mechanisms to guard against surges and transients which so easily push less extraordinary power supplies well beyond their limits. Actual field data confirms MELCHER PSR units perform reliably with an average MTBF of almost 2 million hours!

There is a great deal more to tell about MELCHER performance and quality in the finest Swiss tradition, and also about our in-depth customer service and applications engineering programs. We invite you to call our 800 number for a copy of our fact-filled, full line catalog where, among other things, you'll learn about MELCHER's 24-hour 100% burn-in testing . . . just one of the vital steps in MELCHER's total Quality Management Program.



A wide range of standard and custom designs

For a copy of our full-line catalog, or to speak directly with an applications engineer, call:

1-800-828-9712

MELCHER

MELCHER INC., 200 Butterfield Drive, Ashland, MA 01721
Fax (508) 881-5082

* ALL MELCHER POWER SUPPLIES CARRY A FULL YEAR WARRANTY AGAINST ALL MANUFACTURING DEFECTS

CIRCLE 120

POWER SPLITTERS/ COMBINERS

the world's largest selection 2KHz to 8GHz from $4.95

With over 300 models, from 2-way to 48-way, 0°, 90° and 180°, a variety of pin and connector packages, 50 and 75 ohm, covering 2KHz to 8000MHz, Mini-Circuits offers the world's largest selection of off-the-shelf power splitter/combiners. So why compromise your systems design when you can select the power splitter/combiner that closely matches your specific package and frequency band requirements at lowest cost and with immediate delivery.

And we will handle your "special" needs, such as wider bandwidth, higher isolation, intermixed connectors, etc. courteously with rapid turnaround time.

Of course, all units come with our one-year guarantee. Unprecedented 4.5 sigma unit-to-unit repeatability also guaranteed, meaning units ordered today or next year will provide performance identical to those delivered last year.

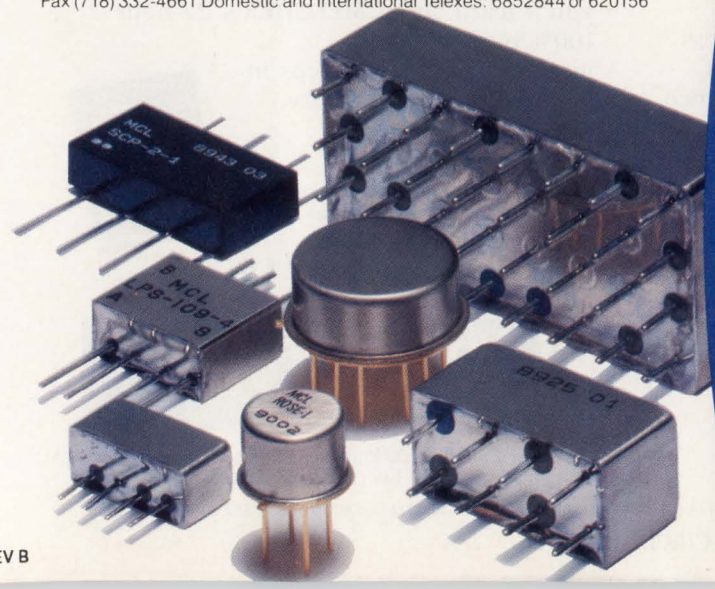
For detailed specs and performance data, refer to the MicroWaves Product Directory, EEM or MIni-Circuits RF/IF Signal Processing Handbook, Vol. II. Or contact us for our free 68-page RF/IF Signal Processing Guide.

CIRCLE 128 FOR U.S. RESPONSE **CIRCLE 129 FOR RESPONSE OUTSIDE THE U.S.**

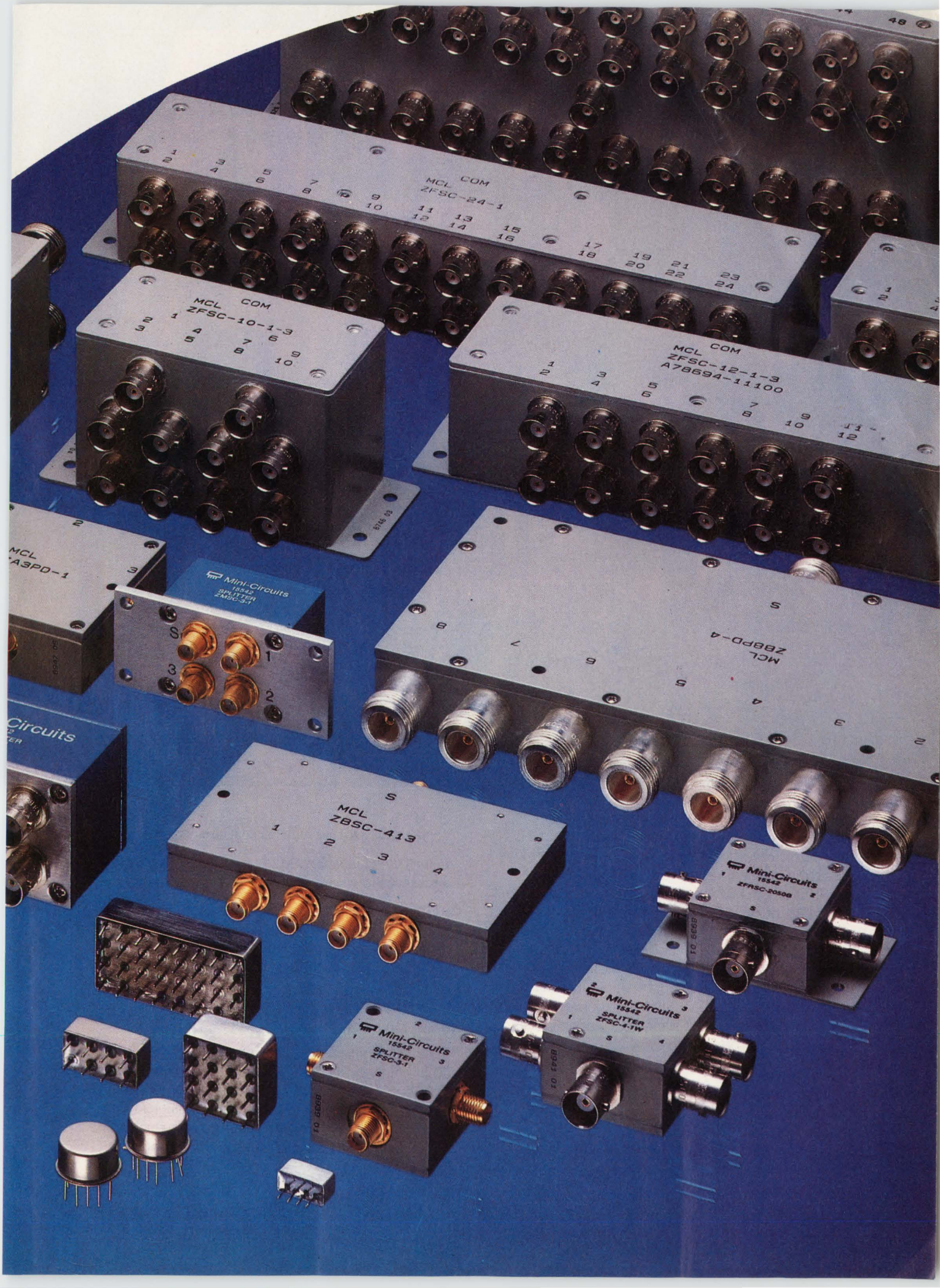
finding new ways ...
setting higher standards

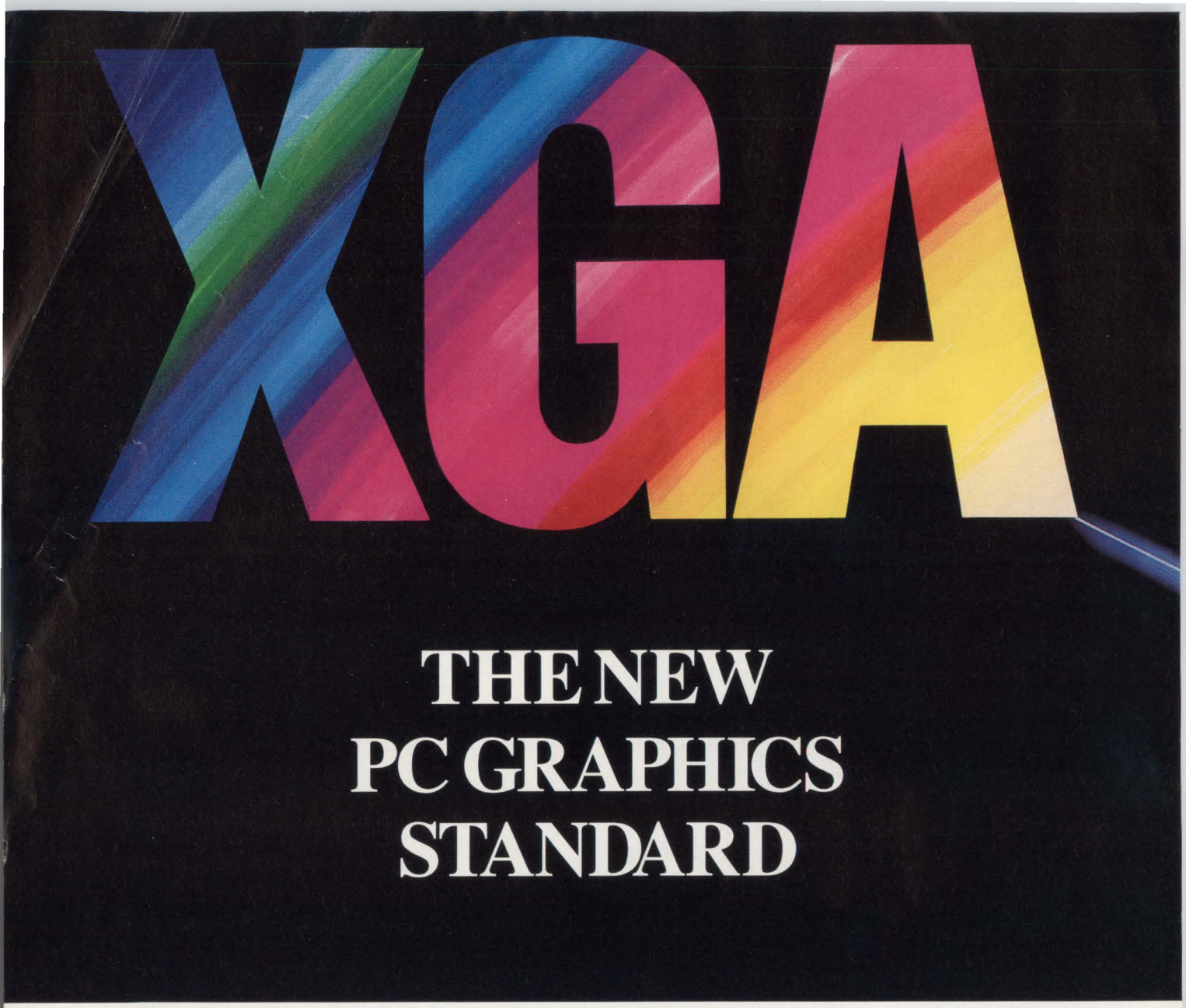
Mini-Circuits

A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156



F134-1 REV B


MCL COM
ZFSC-24-1
MCL COM
ZFSC-10-1-3
MCL COM
ZFSC-12-1-3
A78694-11100
MCL
ZBSC-413
MCL
ZBPD-4
Mini-Circuits
15542
SPLITTER
ZMSC-3-1
Mini-Circuits
15542
SPLITTER
ZFSC-3-1
Mini-Circuits
15542
SPLITTER
ZFSC-4-1W
Mini-Circuits
15542
ZFRSC-2050B



THE NEW PC GRAPHICS STANDARD

The new XGA standard has opened up an era of higher performance for PC graphics. And when IBM licensed their technology to INMOS, a division of SGS-THOMSON Microelectronics, as manufacturer and sole supplier of the IBM XGA chipset, they did it to ensure that the XGA parts got to the market quickly and reliably, setting the stage for XGA to become the next volume standard in PC graphics. Specifically designed for PCs, XGA is already available to support the MicroChannel Architecture bus, and an AT bus-compatible version is under way. The new XGA standard offers significant enhancements over VGA with:

- higher speed
- higher resolution (up to 1024 × 768)
- more colors (256 up to 64K) giving photo-realistic multimedia-style images
- optimized graphics interface for better windowing
- optimization for use with latest generation processors

Fully VGA compatible, XGA performance specs offer a package that is way ahead:

- 132 column text mode
- extended graphics function mode, including hardware sprite and coprocessor hardware drawing assist
- 90% faster than IBM VGA under DOS, 55% faster under OS/2
- 67% faster running Microsoft Windows applications

TWO CHIPS THAT SET THE STANDARD

The IBM compatible XGA chipset consists of two advanced VLSI chips, the INMOS IMS G190 XGA Serializer Palette DAC in a 144 pin CQFP and the INMOS IMS G200 XGA Display Controller in a 184 pin PQFP. A major advantage of the IMS G200 is its on-chip coprocessor which offloads tasks from the host processor and allows it to support:

United States Tel. + 1 602 867 6259 Fax. + 1 602 867 6290 **Asia/Pacific** Tel. + 65 482 1411 Fax. + 65 482 0240

IBM ARCHITECTURE IN SILICON EXCLUSIVELY FROM SGS-THOMSON

- 1, 2, 4, and 8 bit pixel and bit block transfers
- line draw
- area fill
- logical and arithmetic pixel mixing
- map masking
- scissoring
- X, Y axes addressing

FULL SOFTWARE SUPPORT is offered for the IBM compatible XGA chipset with the following drivers available:

- DOS Application Interface (DOS AI)
- OS/2 Presentation Manager (OS/2 PM)
- Windows 3.0
- Double Byte character set

Plus a programmer's guide so you can develop your own BIOS software.

AVAILABLE NOW

Yes, the standard IBM MicroChannel Architecture-compatible XGA chipset is available right now. Just call or fax one of the SGS-THOMSON locations listed below and get details on delivery and price.

SGS-THOMSON MICROELECTRONICS

access to technology

Europe Tel. + 33 1 4740 7506 Fax. + 33 1 4740 7910 **Japan** Tel. + 81 3 280 4125 Fax. + 81 3 280 4131

CIRCLE 234 FOR U.S. RESPONSE

CIRCLE 235 FOR RESPONSE OUTSIDE THE U.S.

Build a Better Test System

Developing a PC-based test system with standard hardware and software saves valuable development time and produces a higher quality system. That's why National Instruments hardware and software products are built upon industry standards.

Our GPIB boards use the NAT4882™ chip for complete IEEE-488.2 compatibility. And our LabWindows® software combines powerful development tools with standard programming languages.

With LabWindows, you have the software tools you need to integrate all of the hardware in your test system. Use high-level 488.2 routines to simplify system programming or use drivers from the LabWindows Instrument Library to control your GPIB and VXI instruments without programming them at all.

LabWindows has tools for all phases of your development–data acquisition, analysis, and presentation. You can even create a graphical user interface so your test system is easy to operate.

See Us At WESCON, Booth 2642

To learn how to build a better test system, give us a call.

NATIONAL INSTRUMENTS®
The Software is the Instrument®

Corporate Office
6504 Bridge Point Parkway
Austin, TX 78730-5039
512) 794-0100
(800) 433-3488 (U.S. and Canada)

CIRCLE 138 FOR U.S. RESPONSE

CIRCLE 139 FOR RESPONSE OUTSIDE THE U.S.

NEW BJT STRUCTURE INTEGRATES BiCMOS

Fujitsu Laboratories in Japan has fabricated a transistor structure that combines the advantages of lateral-bipolar-junction-transistor (BJT) design and biCMOS technology. The device is a thin-base lateral BJT fabricated on a silicon-on-insulator (SOI) structure. Where conventional vertical BJTs suffer from high power dissipation, low packing densities, and production complexity, the lateral design plus the high-quality crystal of the bonded SOI structure and a thin base cuts the number of fabrication steps in half. Fujitsu reports that the device has a high cutoff frequency of 4 GHz, high current gain, and a high breakdown voltage. A mass-production process is being developed to produce these transistors for use in mainframe computers and other high-speed applications. *ML*

FAULT SIMULATOR RUNS CYCLE-BASED ALGORITHM

Unlike most fault simulators using concurrent-processing technology, the ADAS Fault Simulator from ADAS Software Inc., Santa Clara, Calif., employs a cycle-based algorithm based on parallel differential fault simulation. The result is a reduction in both simulation time and hardware-memory requirements. ADAS can use the proprietary algorithm because the behavior of most digital ICs is cycle-based, or well-defined within each clock cycle. The simulator uses less memory than most other fault simulators because it records only the difference between each faulty machine and the master copy of the good machine at circuit memory elements such as latches and flip-flops. This recording mechanism can save up to an average of 90% of system memory usage when compared with concurrent fault simulation. In addition, the cycle-based fault simulator can run large circuits without partitioning fault lists. For more information, call ADAS at (408) 988-3846. *LM*

IC HANDLES CAR-RADIO SIGNAL PROCESSING

A single-chip processor contains all the circuits necessary for processing amplitude- and frequency-modulated (AM and FM) audio-frequency stereo signals in a car radio. The CAP processor, from the ITT Semiconductors Group in Freiburg, Germany, also controls the audio variables and performs a number of additional jobs, such as automatic interference suppression, demodulation of multiplexed signals, as well as demodulation and IF processing of AM signals. The heart of the CAP is a universal digital signal processor with a 16-bit data-word width and 15-MIPS of computing power. The circuits are accommodated in a digital and analog block. The digital block contains hard-wired digital filters, modulators for the pilot sound, a suppression circuit, a synthesizer and serial digital interfaces, including a programmable interface for connecting a CD player. The analog block includes input selector switches and converters. The two analog outputs can drive four output amplifiers via four independently variable volume controls. The CAP processor is made by a 1.2-μm CMOS process and comes in a 68-pin plastic leaded chip carrier package. *JG*

GAP NARROWS BETWEEN ELECTRONICS, OPTICS

In a speech at a recent international meeting of the IEEE in London, Ian Ross, president emeritus of AT&T Bell Laboratories, said the field of optoelectronics is rapidly melding the disciplines of electronics and optics. He predicted that tomorrow's photonic transmission systems will be based on many innovations currently being developed in research labs—most notably optical amplifiers and solitons. Op amps are segments of optical fiber that contain the rare-earth element erbium, which boosts optical signals without converting them to electronic signals and back again. Solitons are pulses of light that retain their shape over long distances. Ross added that lithium-niobate and SEED (self-electro-optic effect device) technologies will contribute to next-generation photonic-switching components. Lithium-niobate technology is a platform of electrically controlled optical waveguides, which include light modulators and switch-coupler crosspoints (input-output links). SEEDs are optical transistors. Symmetrical SEEDS (S-SEEDs) were the building blocks of the first optical switching fabric; both were invented at Bell Laboratories. *ML*

PHYSICS-BASED IGBT MODEL IS MORE ACCURATE

The first commercially-available model of an insulated-gate bipolar transistor (IGBT) that's based on physics more accurately predicts IGBT switching losses and transient characteristics than would a macromodel composed of low-voltage signal transistors. Developed by the National Institute of Standards and Technology (NIST), the model was implemented in the Saber simulator from Analogy Inc., Beaverton, Ore. Its greater accuracy is the result of the basic differences in the equations that govern transistor behavior. It accurately estimates current, voltage, and charge characteristics of both steady-state and switching transient waveforms for all loading conditions. In addition,

Imagine com
without a ge

Mixed-Signal IC Solutions

You're staring that gap right in the face. Unless key components in your modem, laptop PCs, LAN and telecommunications product designs can connect with, and address, the technological needs of tomorrow.

Thankfully, you can close that gap by tapping into the power and experience of Silicon Systems.

Our approach to every solution using Mixed-Signal Integrated Circuits —MSICs™— is to design and bring to market products with a built-in migration path to the future. Compatibility forwards and backwards. And a tuned-in sensitivity for the latest industry standards.

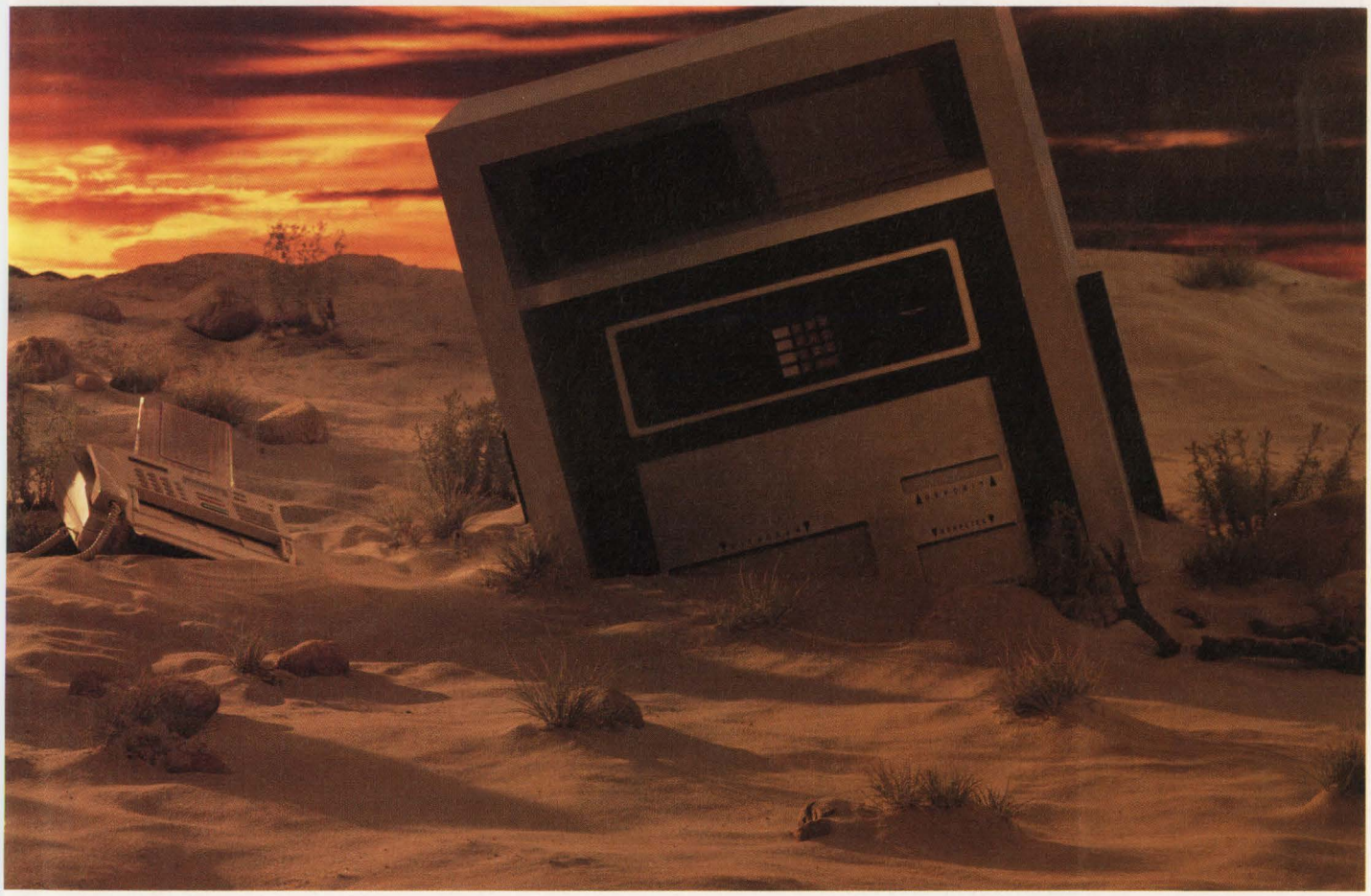
In the short run this helps speed your products to your customers. In the long run you'll rest assured that today's innovations won't be making a premature arrival at tomorrow's scrap heap.

Our pin/software compatible K-Series of 1200 bit/s and 2400 bit/s single-chip modems, for example, are well-connected to a variety of current and emerging world standards, along with being the lowest power 5-volt products you can buy.

Our newest thinking on PC/FAX includes a built-in pipeline to

Circle 170 for Product Info (U.S. Response)
Circle 171 for Career Info (U.S. Response)

mmunications
neration gap.



future FAX standards.

And in telephone communications, our latest line interface ideas will continue to flourish in the coming SONET world.

Upgradability isn't something we tack on. It's ingrained in our design culture. A distinct advantage, your advantage, as you gear up to compete successfully in the exploding telecommunications marketplace.

Our point should be clear. Generation gaps are avoidable, not inevitable. To walk our migration path, talk with your nearest Silicon Systems representative or distributor. Or call us for literature package CPD-8.

Circle 172 for Product Info (Response Outside U.S.)
Circle 173 for Career Info (Response Outside U.S.)

Silicon Systems, Inc.,
14351 Myford Road, Tustin, CA 92680
Ph 1-800-624-8999, ext.151 Fax (714) 669-8814
European Hdq. U.K. Ph (44) 79 - 881-2331 Fax (44) 79 - 881-2117

silicon systems®
A TDK Group Company

users can emulate switching losses and characterize the model to actual components. Analogy is shipping the IGBT model now as part of its generic library. For more information, call (503) 626-9700. *LM*

CONTROLLER CARD UPS CD-ROM PERFORMANCE

A CD-ROM controller card can be used in any personal computer with an ISA or EISA bus architecture. With the CDD167 card from Philips Interactive Media Systems in Eindhoven, the Netherlands, any of Philips' serial CD-ROM drives, either built into the PC or external to it, can be connected to the PC and will operate as a CD-ROM-XA (extended architecture) drive. The new controller card offers a simple and economic method for users of Philips serial CD-ROM drives who wish to upgrade to the CD-ROM-XA format. It adds graphic and audio information to the basic CD-ROM text data. The CDD167 replaces the company's CDD157 controller and features a higher degree of integration, which gives the new card improved performance and functionality. Additional CDD167 enhancements include the ability to handle external CD-ROM drives and support for the Unix S.5 operating system. *JG*

DESIGN SOFTWARE EASES FPGA-TO-ASIC MIGRATION

Engineers wishing to migrate their field-programmable gate arrays (FPGAs) to CMOS ASICs can preserve pin-to-pin and package-footprint compatibility for direct board replacement of devices if they use the SoftPath software from AT&T Microelectronics, Berkeley Heights, N.J. Almost no training is needed to use the tool: Engineers need only enter a one-line command to perform the entire conversion process, which includes optimization and mapping of I/O buffers. SoftPath, which re-synthesizes a functionally-equivalent CMOS gate-array net list from an existing FPGA net list, converts AT&T's FPGAs into the company's recently introduced ATT656 Series CMOS gate arrays. The ATT656 Series mask-programmable arrays are compatible with NEC's CMOS6/6A family of arrays. They're manufactured in 1-μm-channel-length, silicon-gate, double- and triple-layer-metal technology. Typical gate delay is less that 270 ps, and power consumption is less that 8 μW/gate/MHz. Ten pre-processed base arrays are available for customization, with 5000 to 177,000 usable gates and up to 448 I/O pins. For more information on the SoftPath tool and the ATT656 Series CMOS arrays, call the AT&T Customer Response Center at (800) 372-2447, ext. 817 and 818, respectively. In Canada, call the same extensions at (800) 553-2448. *LM*

LOW-COST RISC AIMED AT EMBEDDED CONTROL

Although 32-bit RISC processors make high-performance embedded controllers, most have chip areas that make them too costly for many applications. In answer to this, designers at Advanced RISC Machines (ARM) Ltd., in both Cambridge, U.K., and Los Gatos, Calif., have released details of their ARM 60 and 600 RISC processors. Both 32-bit processors have the industry's smallest RISC CPU cores, which can run at 20 to 25 MHz. The CPUs are available as inexpensive stand-alone chips or as megacells on the company's standard-cell design system.

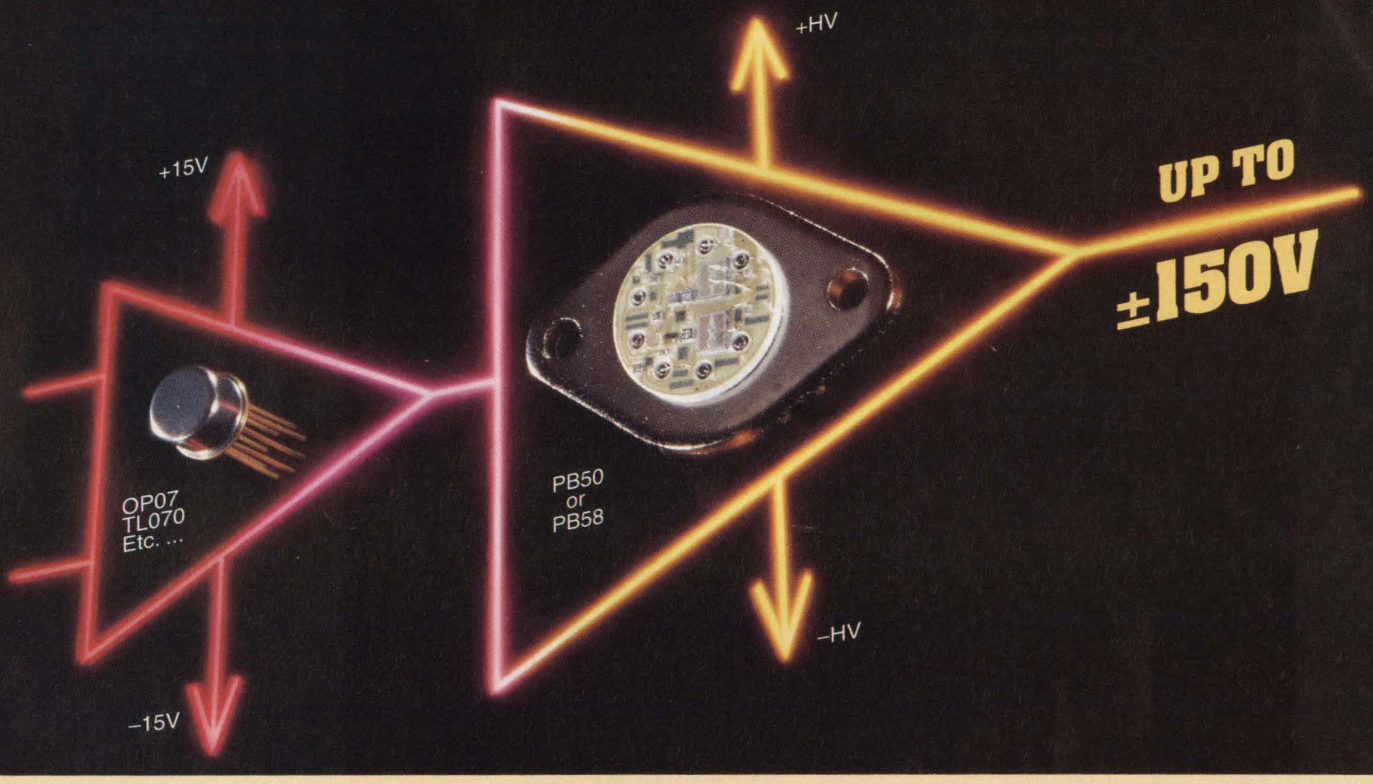
The RISC design enhances the CPU core technology licensed from Acorn Computers Ltd., U.K., one of the founders of Advanced RISC Machines and creator of the Arm architecture. The other companies supporting ARM are Apple Computer and VLSI Technology. If the Arm processors sound vaguely familiar, that's because VLSI Technology, San Jose, Calif., has had a license from Acorn for several years to manufacture, design, and sell the Arm architecture. The forthcoming ARM 60 and 600 include redesigned CPU cores that are implemented with fully static CMOS logic to minimize standby power, and both will include JTAG test ports to ease in-system testing.

Housed in a 100-lead package, the ARM 60 is an extension of the ARM 2 processor sold by VLSI, and includes full and separate 32-bit data and address buses, as well as a low-overhead interrupt controller. During standby, the CPU core consumes just 10 μA, while when active the power increases to 1.5 mA/MHz. An 84-pin version, the ARM 61, can drop into ARM 2 sockets and allows designers to trim system power by replacing the older dynamic CMOS part with the fully-static CMOS version. The ARM 600 is a major enhancement of the architecture and includes a 4-kbyte cache, an on-chip MMU, a co-processor interface, and additional functions. Unlike standard memory managers, the ARM 600's includes special features to enhance operation for object-oriented software. Those features improve control of access permission, perform concurrent garbage collection, handle persistent object store clients, and provide an 18-bit permission store and 20 bits of address mapping. Call Tim O'Donnell, (408) 399-5195. *DB*

COST EFFECTIVE INNOVATIONS

HIGH VOLTAGE BOOSTERS

HIGH OUTPUT CURRENT



PB50

- Up to ±100V Supply
- Up to ±2A
- 100 V/µs Slew Rate
- $54.90 in 100s

THE PB50 AND PB58 PROVIDE DESIGN FLEXIBILITY BY BOOSTING SMALL SIGNALS UP TO ±150V AT ±2A WITHOUT RISK OF SECOND BREAKDOWN.

PB58

- Up to ±150V Supply
- Up to ±2A
- 100 V/µs Slew Rate
- $64.90 in 100s

APEX® µtech
DEDICATED TO EXCELLENCE

APEX MICROTECHNOLOGY CORPORATION
5980 N. SHANNON ROAD, TUCSON, ARIZONA 85741

For Immediate Product Information Call **1-800-448-1025** or FAX **(602) 888-3329**

For Applications and Product Selection Assistance Call Newly Expanded Hotline **1-800-421-1865**

CANADA (416) 821-7800 DENMARK (42) 24 48 88 GERMANY (6152) 61081 SPAIN (1) 4094725 FINLAND (0) 8041-041 FRANCE (1) 69 07 08 24 HONG KONG 8339013 ISRAEL (3) 9345171 INDIA (212) 339836 ITALY (2) 99041977 JAPAN (3) 3244-3787 NETHERLANDS (10) 4519533 NORWAY (2) 50 06 50 KOREA (2) 745-2761 AUSTRIA (1) 505 15220 SWITZERLAND (56) 26 54 86 SINGAPORE 284-8537 SWEDEN (8) 795 9650 TAIWAN (02) 721-9533 UK (0844) 278781 BELGIUM/LUXEMBOURG (3) 828-3880 AUSTRALIA (08) 277-3288

"APEX HYBRID & IC HANDBOOK" — Order Your Free Copy Of The New 5th Edition Today!

CIRCLE 90 FOR U.S. RESPONSE

CIRCLE 91 FOR RESPONSE OUTSIDE THE U.S.

If you think DSPs are priced Our TMS320 family starts at

out of reach, think again. just $3.

Cost is no longer a barrier to using DSPs. At Texas Instruments, our TMS320 family is well within your reach, thanks in large part to a decade of DSP leadership.

16-bit DSPs as low as $3

Our 16-bit, fixed-point solutions begin at $3. At that, they are on a price par with microcontrollers and are as easy to use, yet give you 10X the performance.

These DSPs are extremely well suited to high-volume applications, providing you with opportunities to optimize price/performance ratios. In fact, our 16-bit DSPs are replacing microcontrollers in mainstream applications such as answering machines and disk drives.

32-bit DSPs starting at $25

You can get floating-point performance at a fixed-point price. Starting as low as $25, our 32-bit floating-point DSPs are finding widespread use in embedded, cost-sensitive applications. Performance is superior to RISC processors because of highly paralleled architectures.

In addition to a low unit price, several features contribute to overall cost-effectiveness. These devices are inherently easy to use and are optimized for use with high-level-language compilers, which helps you get to market faster.

When you require a custom approach, we have the unique capability to adapt our 16- and 32-bit DSPs to your needs.

The entire TMS320 family is supported by an extensive array of development tools, readily accessible applications help and full documentation to help enhance your productivity and cut development time.

Passing savings on to you

In the 10 years since TI introduced its first single-chip DSP, we have shipped tens of millions of these devices worldwide. And we have applied the principles of manufacturing excellence learned from our commitment to DRAM manufacturing. This has resulted in the economies of scale that enable us to provide you with true value and dependable prices.

To put TI's DSPs within reach, call 1-800-336-5236, ext. 3537

We'll send you information on our TMS320 family, world-class support and cDSP capability.

08-1208

TEXAS INSTRUMENTS

ABSOLUTE VALUE.

High performance LCR meters from SRS. 0.05% accuracy, 100 kHz frequency. Absolutely lowest price.

Value. It means getting your money's worth.

For passive component measurement, the new standards in value are the SR720/715 LCR meters from SRS. Meters that offer significant advantages in performance and price. Performance like .05% basic accuracy, 100 kHz test frequency, and fast measurement rates up to 20 per second. Features like a built in Kelvin fixture, averaging, binning and limits, stored setups, and quick calibration. With the standard RS232 and optional GPIB and Handler interfaces, the SR720/715 solves your incoming inspection and automated test needs. All for a price well below what you'd expect.

The SR720/SR715. Absolute values in a complex world. Call **(408)744-9040** today for more information about the SRS advantage.

SR720 **$2295**

- 0.05% basic accuracy
- 100 Hz to 100 kHz measurement frequency
- Two 5 digit displays for simultaneous readout of major and minor parameters.
- Auto, R+Q, L+Q, C+D, C+R, Series and Parallel measurement modes
- 100 mV to 1.0 V test signals
- Internal and External Bias
- Binning and Limits for production testing and component inspection.
- RS232 interface
- GPIB and Handler interface (optional)

SR715 **$1495**

Same as SR720 except:

- 0.2% basic accuracy
- 100 Hz to 10 kHz measurement frequency

SRS **STANFORD RESEARCH SYSTEMS**

1290 D Reamwood Avenue, Sunnyvale, CA 94089 TEL (408)744-9040 FAX 4087449049 TLX 706891 SRS UD

CIRCLE 176 FOR U.S. RESPONSE

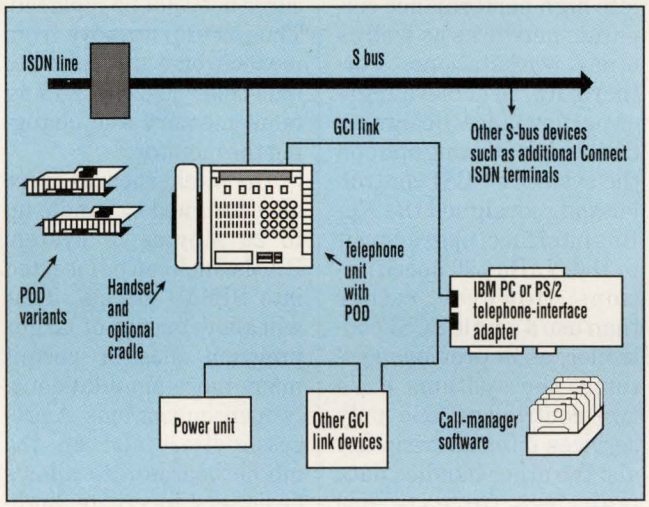
CIRCLE 177 FOR RESPONSE OUTSIDE THE U.S.

TELEPHONE WITH MODULAR PLUGINS PAVES THE WAY FOR ISDN SERVICES

A digital telephone launched in the United Kingdom uses plug-in modules to provide a range of existing and future integrated voice and data network features, making it compatible with the Integrated Services Digital Network (ISDN). It can be used with personal computers and standard communications software to provide a high-speed replacement for modems. Using international basic-rate ISDN telecomunications standards, the telephone can handle data rates of up to 38.4 kbits/s on either of the two ISDN B channels running simultaneously at 64 kbits/s, for dialup voice or data calls.

The telephone, named Connect, was jointly developed by GEC Plessey Telecommunications Ltd. (GPT) and Hayes Microcomputer Products Inc. The two firms worked together on software for the telephone. Bill Pechey, engineering manager for Hayes in the United Kingdom, says that the result is the Hayes AT-ISDN language, a super-set of the well-established Hayes AT set of commands and instructions used with conventional analog modems. "A PC can see the telephone as a very high-speed modem which protects users' investment in communications software" explains Pechey.

David N Wright, GPT's general manager for ISDN terminals explains that the base unit, a fully featured loudspeaking unit with two LCD screens and a side-mounted handset cradle, is a universal "chassis" that acts as a carrier for personality modules. But that description belies the sophistication of the unit—for it's much more than a mere royal blue plastic shell. "It's a miniature digital switching system" Wright says *(see the photograph).*



It uses a standard bus architecture based on an IOM2 general-circuit interface (GCI) link to connect a range of peripherals and terminals for access to information carried on both 64-kbit/s B channels and the 16-kbit/s D channel. The GCI bus also supports interprocessor communications between all attached units. Switching and control of this bus is managed by the internal electronics of the base unit.

The base unit has been designed by GPT to be all things to all approval authorities. At present, Wright says, the telephone supports British Telecom's basic-rate ISDN service in the United Kingdom and the AT&T ESS # 5 and Northern Telecom DMS-100 ISDN Centrex standards in the U.S.A. and Canada. GPT and Hayes are also working to ensure that the telephone will work with whatever emerges as the U.S. National ISDN standard, and are negotiating trials with a number of Regional Bell holding companies, including Ameritech, Bell Atlantic, and U.S. West.

With the insertion of any one of a range of Pluggable Option Devices (PODs), the telephone takes on new characters *(see the figure).* So far, three PODs have been announced. The first, POD-0, simply supports voice telephony using all the facilities of the ISDN B channel. The second two PODs, POD-1 and POD-2, add data-communications facilities and make the unit a true integrated voice and data terminal. In addition to voice functions, POD-1 provides 38.4-kbits/s asynchronous data communications via a standard RS232 interface. Applications include high-speed asynchronous file transfers for international networking using V.120 rate adaptation, access to X.25 resources, and interconnection of local-area networks using bridging units with V.24 interfaces.

But it's when POD-2 is fitted that the Connect really comes into its own as an integrated voice and data terminal, offering full 64-kbit/s data transfer. POD-2 also includes the software needed to terminate a GCI link to a future product, and an adapter card for internal fitting in a personal computer.

A telephone interface adapter (TIA) is engineered for both the 16-bit IBM PC industry-standard internal bus and for PCs

based around IBM's proprietary Micro Channel Architecture (MCA). Wright says the GPT card interfaces with the ISDN via the GCI bus and the digital telephone. Like the PODs, the TIA supports the Hayes standard AT command set for ISDN and appears to its host PC as standard asynchronous adapter. But it also contains shared memory to support the Hayes ISDN-BIOS low-level interface control system.

Also supported is V.110 and V.120 rate adaptation between the data rate set by a PC application and the 64-kbit/s B Channel. X.25 support is provided, allowing direct calls to public and private packet switched networks. Up to eight simultaneous sessions can be take place. Finally, the card includes adaptive differential pulse-code-modulation (ADPCM) circuits that makes 32-kbit/s digitized speech available through the PC.

Wright says that the Connect telephones and the first two PODs will be available during the last quarter. Production is beginning at GPT's Beeston, Nottingham plant. In the United Kingdom, the telephone fitted with PD-0 will sell for £499, and with POD-1 for £899.

The Connect chassis will also form the base for a video-telephone due for introduction this month. GPT's Videophone will provide all the digital telephony features of the Connect and adds a full-color 5-in. LCD screen and full-color built-in camera. The videophone will have a price tag of around £10,000.

PETER FLETCHER

NEW MACINTOSH COMPUTERS ADD 68040 CPU, ETHERNET, AND IMPROVED NUBUS AND VIDEO

The first 68040-based Macintosh systems from Apple Computer Corp., Cupertino, Calif., were released last month at Comdex in Las Vegas. Expected ever since Motorola unveiled details of its 68040, they run the 68040 at 25 MHz and deliver a throughput close to twice that of the Mac IIfx, Apple's fastest system.

The Quadra systems are also the first by Apple to include Ethernet as a *standard* built-in feature. This will allow the systems to tie into high-performance corporate networks as well as other workstations. Furthermore, to achieve higher performance, designers doubled the throughput on the system's SCSI controller and redesigned the NuBus interface, upgrading it to the NuBus 90 specifications. However, rather than use a single SCSI controller, as in previous systems, the systems have two controllers: one only services internal peripherals; the other handles data transfers for external SCSI devices.

The NuBus 90 specifications call for the bus to transfer data at 20 MHz, which is double the rate of Apple's current NuBus implementation. As a result, data can transfer twice as fast over the NuBus, and twice as fast over the SCSI ports. That combination of higher data rates will push the performance of the new Quadra 68040-based systems into the workstation realm. However, even with the improved interface, previously-designed peripherals that plug into the older NuBus should work just as well on the enhanced NuBus. One limitation of the SCSI port, however, is that Apple has still not implemented a peer-to-peer version of SCSI—the host system must always be the initiator.

A new video subsystem on the Quadra systems allows users to select the pixel depth (from 1 to 32 bits) by simply adding video RAM. This simple approach reduces the upgrade cost to the system user because the video cards need not be replaced. Thus, users can move from monochrome to color to true-color just by adding more memory and changing the monitor.

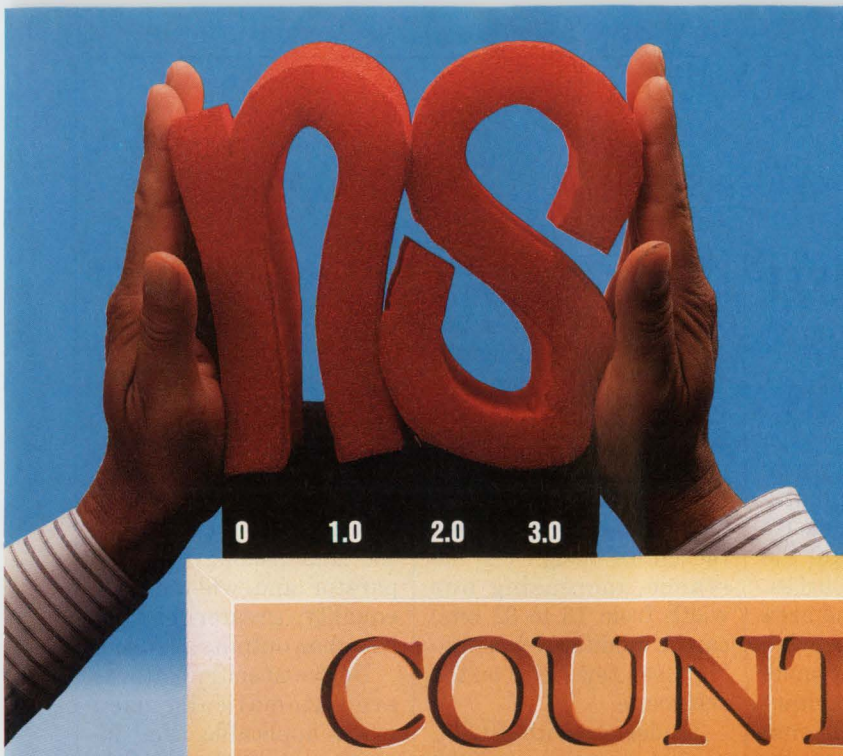
The motherboards were also designed to handle up to 20 Mbytes of system RAM which can be inserted into SIMM sockets. That will allow for use of larger program files or permit many more simultaneously open applications. A processor-direct slot on the motherboards also allows designers to create high-performance support cards that can take advantage of the direct processor interface, bypassing the overhead of the NuBus.

There are two initial models in the new family. At the top of the line, the Quadra 900 is the first Macintosh designed specifically as a "tower" and has plenty of expansion space and a 300-W supply to power multiple disk drives and up to five option cards. The other model, the Quadra 700, uses the same case and supply used by the Macintosh IIci and can be set up as either a desktop or a mini tower. The 700 has just two NuBus expansion slots—but two should suffice because Ethernet and video interfaces are built in.

Both systems are configured to run System 7.01 or AUX 3.0 and come with 80- or 160-Mbyte drives and 4 Mbytes of RAM in their base models. As with all new Macintosh computers, audio input and output ports are included, as is the 1.4-Mbyte floppy Superdrive that can read both Apple and IBM-compatible DOS diskettes. The Apple desktop bus (ADB) was beefed up so that more peripherals can be connected to the ADB. On the Quadra 700, the bus can handle 200-mA loads, while the Quadra 900 permits 500-mA loads. (The keyboard and mouse combination draws 105 to 160 mA.)

The high-end Quadra 900, configured with 4 Mbytes of RAM, a 160-Mbyte hard-disk drive, and 1 Mbyte of video memory for 8-bit color (plus 5 NuBus expansion slots and a 300-W power supply) will list for $8699. The Quadra 700 mini-tower has 4 Mbytes of RAM, an 80-Mbyte drive, and 512 kbytes of VRAM and lists for about $6500. The video memory subsystem on both computers can be expanded up to 2 Mbytes. In the second quarter of 1992, Mac IIci users will be able to exchange motherboards to upgrade their systems, effectively turning a IIci into a Quadra 700. Contact Apple at (408) 996-1010.

DAVE BURSKY



COUNT ON IDT

When Every Nanosecond Counts

Squeeze critical nanoseconds from your high-speed logic interface with the fastest FCT logic available. IDT's FCT-CT family offers speeds that are 50% faster than standard FCT or FAST logic families—as fast as 3.4ns (typical)!

The Perfect System Solution

As a system designer, you need the perfect combination of:

1. ***Fastest speed***
2. ***Low ground bounce***
3. ***Low power consumption***

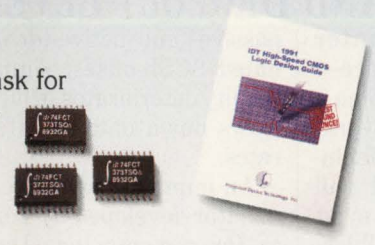
FCT-CT logic has true TTL compatibility for ease of design. The reduced output swings and controlled output edge rate circuitry ensure low system noise generation. No other technology offers higher speeds or lower power consumption.

The FCT-CT family is completely pin- and function-compatible with FCT logic, and is available today in all standard packaging.

FUNCTION	PROPAGATION DELAY (Max)	OUTPUT ENABLE (Max)	OUTPUT DISABLE (Max)
Buffers	4.1ns	5.8ns	5.2ns
Transceivers	4.1ns	5.8ns	4.8ns
Registers	5.2ns	5.5ns	5.0ns
Latches	4.2ns	5.5ns	5.0ns

Free Logic Design Kit

Call our toll-free hotline today and ask for Kit Code 3061 to get a *1991 High-Speed CMOS Logic Design Guide* and *free FCT-CT logic samples.*



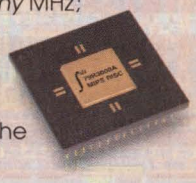
(800) 345-7015 • FAX: 408-492-8674

12ns 256K SRAMS

Fastest cache solutions for RISC and CISC CPUs. 36+ ultra-high-speed sub-micron SRAMs for 33MHz processing & beyond are in the **SRAM Data Book**.

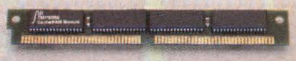
35mips RISC CHIPS AND MODULES

R3000A for the most mips at *any* MHz; R3051 for CPU, cache, & buffers on one chip. Modules, eval. boards & software complete the family. See them in the **RISC Data Book**.



HIGHEST-PERFORMANCE MEMORIES

Fast FIFOs, dense dual-ports, BiCEMOS ECL, & memory modules. 120+ FIFOs & multi-port memories, 5ns ECL, & multi-chip modules are in the **Specialized Memories Data Book**.



Call today for your new IDT data books with complete technical specifications and application information.

Integrated Device Technology, Inc.

RULES-BASED ALGORITHMS HELP HIGH-LEVEL DESIGN SOFTWARE EXPLOIT FPGA ARCHITECTURES

Existing gate-level design tools become ineffective as field-programmable gate arrays (FPGAs) push usable densities of 10,000 gates and more. This is because most engineers think of components as complete logic functions with certain attributes, not as groups of gates and flip-flops. Also, an engineer using FPGAs ideally should understand the devices' underlying architecture so they can fully exploit the capabilities of an FPGA. For instance, techniques borrowed from 7400-series TTL don't fully utilize FPGA or ASIC features. Consequently, to manage growing design complexity, engineers need a design-tool technology that will abstract functions to a higher level while still taking advantage of a device's low-level architectural features.

A new design technology from Xilinx Inc., San Jose, Calif., called Xilinx BLOX, uses module generators to keep design complexity in control and automate the gate implementation, but still exploit architectural features. With the BLOX module generators, users build systems more naturally out of functional descriptions instead of gates, and then obtain efficient implementations with rules-based algorithms *(see the figure)*. The algorithms, which were written with the Quintus artificial-intelligence programming language, contain the expert knowledge for the target FPGA architecture.

The 30 BLOX parameterized modules optimize design speed and density by taking into account the best use of chip resources, system features, and area placement. They provide thousands of logic implementations for various popular logic functions. Users can also include gate-level primitives in the BLOX block-diagram descriptions. In addition, the module generators handle multi-bit operations and full data paths, which are common in large designs.

Datapath design is simple with the BLOX technology. Users specify the width and type of a bus once, anywhere along the datapath. The widths and types of data carried on a bus are automatically propagated throughout the design and through levels of hierarchy. The size of the entire design (for instance, increasing bus width from 16 to 32 bits) can be modified by changing just a few fields on the schematic.

To design with BLOX, engineers call up individual function modules from a library while still in a standard schematic editor. Each module's symbol has a parameter sheet attached to it where users enter the specifications for that particular application. These specifications may include bus widths and operating modes.

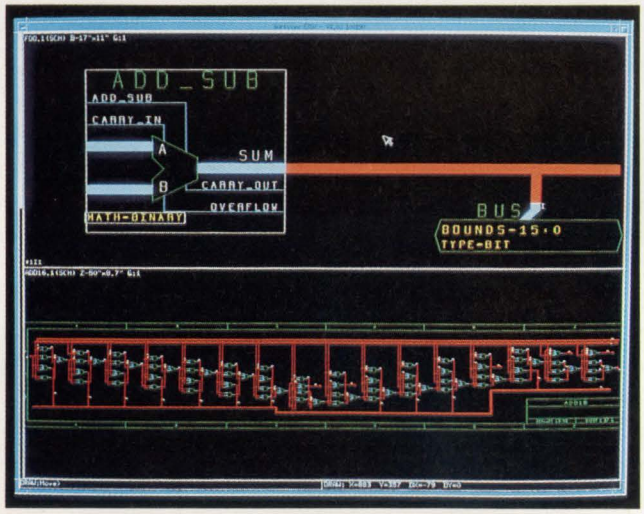
The module generator then custom-tailors the implementation to the specific needs of each module. The implementation of a comparator, for example, will depend on the size of the data feeding the comparator and whether the equality, greater-than, or less-than outputs are used.

Device-specific features are automatically used when applicable. For instance, clocking or high-fanout signals are assigned to special high-drive buffers, and reset logic is automatically assigned to fast-routing paths. Also, the software will intelligently move flip-flops to the FPGA's perimeter to be closer to I/O pins.

Also, using the block-diagram approach to FPGA design saves time. For example, the design-entry time for one design is more than two hours using a schematic-capture program, and about five minutes with Xilinx BLOX.

Xilinx BLOX runs in the company's XACT development system. It will ship in January and will cost $2995 for the PC version and $4995 for Unix workstations.

LISA MALINIAK



IMPROVED SCSI TERMINATOR TIGHTENS GRIP ON OUTPUT AND DROPOUT LEVELS

The small-computer systems interface—SCSI—has become a standard feature on workstations and Apple Macintosh computers, and will soon find its way into most IBM PCs and compatibles. However, as more peripherals get attached to passive- and active-terminated SCSI buses, signal quality deteriorates, which slows down data-transfer rates.

An improved active terminator developed by Texas Instruments Inc., Dallas, Tex., promises to improve signal quality sufficiently to bring back data-transfer rates to near-maximum levels. Those maximum rates are 5 Mbytes/s for SCSI 2 buses, and 10 Mbytes/s for fast SCSI buses.

Simple resistor terminators tend to limit asynchronous SCSI-bus data trans-

Get Caught Speeding!

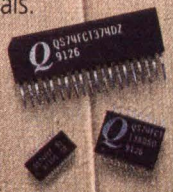
'D' Speed FCT Logic

QSFCT®, the fastest family of logic chips available, period! That's right, **guaranteed** 'D' speed! Quality Semiconductor's QCMOS® process gives you the speed of BiPolar and BiCMOS parts with the low power consumption and reliability properties of CMOS. Quality gives you guaranteed propagation delays as low as 3.8ns max.

QSI offers you extremely clean signals.

The Quality logic family is not only fast, but super clean. With a controlled output swing of 0 to 3.5v, ground bounce is virtually eliminated. The inclusion of edge rate controls and standard hysterisis of .2v on all inputs, combined with optimized device fall times, gives you extremely clean – fast signals.

Complete line of QSFCT Logic.



Available in QSOP, Zip, and SOIC packages, our 'D' speed parts extend a complete line of FCT logic products that are already offered in A, B, & C speeds. In addition, we offer a complete FCT2000 series incorporating on-chip serial resistors, thus saving valuable board space while delivering consistently clean signals.

QSI – your source for high-performance CMOS ICs.

Quality Semiconductor has the high-speed, low noise logic, memories & FIFOs you need to make the most of your high-speed designs. For your copy of Quality's High-Performance CMOS data book call today, **(408) 450-8027.**

Quality Products

PART	SPEED	PART	SPEED
240D (Buffer)	3.8	373D (Latch)	4.2
244D (Buffer)	3.8	374D (Register)	4.5
245D (Transceiver)	3.8	646D (Transceiver)	4.8
138D (Decoder)	4.0	821D (Register)	5.3
139D (Decoder)	4.0	823D (Register)	5.3
521D (Comparator)	4.1		

Quality Semiconductor, Inc.

851 Martin Avenue ▮ Santa Clara, CA 95050
Tel: (408) 450-8027 ▮ Fax: (408) 496-0773

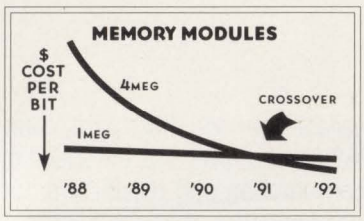
CIRCLE 156 FOR U.S. RESPONSE CIRCLE 157 FOR RESPONSE OUTSIDE THE U.S.

SAMSUNG NOW

IN MEMORY MOD
CROSSOVER HAS J

You've heard the old saying, "we'll cross that bridge when we come to it." Well, we have.

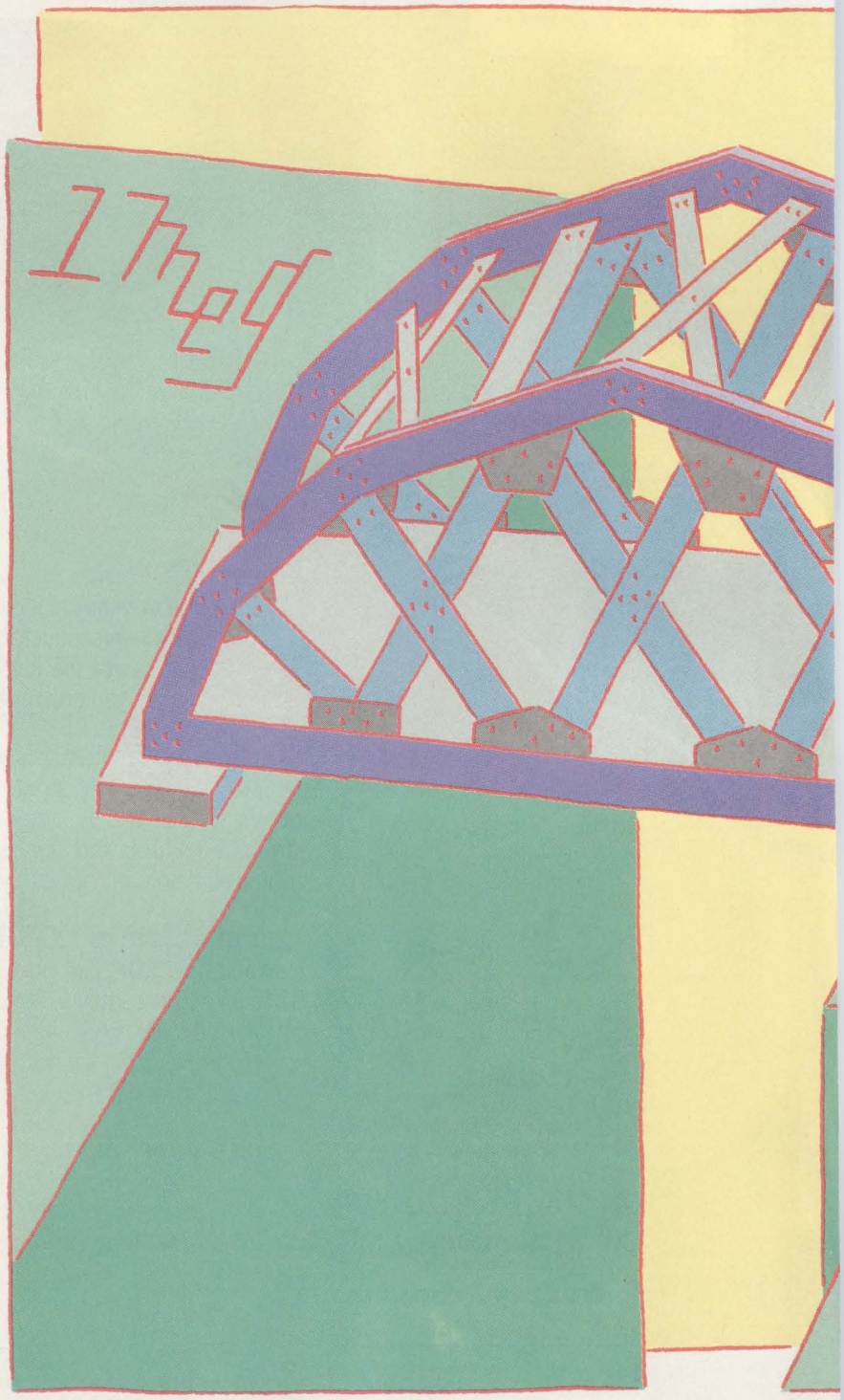
Cost crossover today makes 4-meg DRAMs more economical per bit than 1-meg DRAMs. And given all the benefits in reliability and board real estate, that's good news.



People are lining up to take advantage of it.

One specific advantage is in memory modules. Samsung 4-meg-based modules are actually more cost-effective today than their 1-meg-based counterparts.

All the modules listed here have reliability specs based on 600 temperature cycles (0-125°C) and 500 hours (85°C, 85% RH). Available features include 70, 80, and 100 ns access



ULES, COST-PER-BIT UST BEEN COMPLETED.

times, fast page mode, low-power versions, gold lead finish, and customer-specific labeling.

SAMSUNG MEMORY MODULES BASED ON 4-MEG DRAMs

Megabytes	*Part Number*	*Organization*
1	KMM581000AN	1M x 8
1	KMM591000AN	1M x 9
4	KMM584000A	4M x 8
4	KMM594000A	4M x 9
4	KMM5321000A	1M x 32
4	KMM5331000A	1M x 33
4	KMM5361000A	1M x 36
8	KMM5322000A	2M x 32
8	KMM5332000A	2M x 33
8	KMM5362000A	2M x 36

Samsung is one of the world's leading manufacturers of both DRAMs and memory modules. Our outstanding quality, reliability, and availability have helped us gain this leading position.

For data sheets on our 4-meg DRAMs and 4-meg-based modules, call 1-800-423-7364 or (408) 954-7229 today. Or write to Memory Module Marketing, Samsung Semiconductor, 3725 No. First St., San Jose, CA 95134.

SAMSUNG

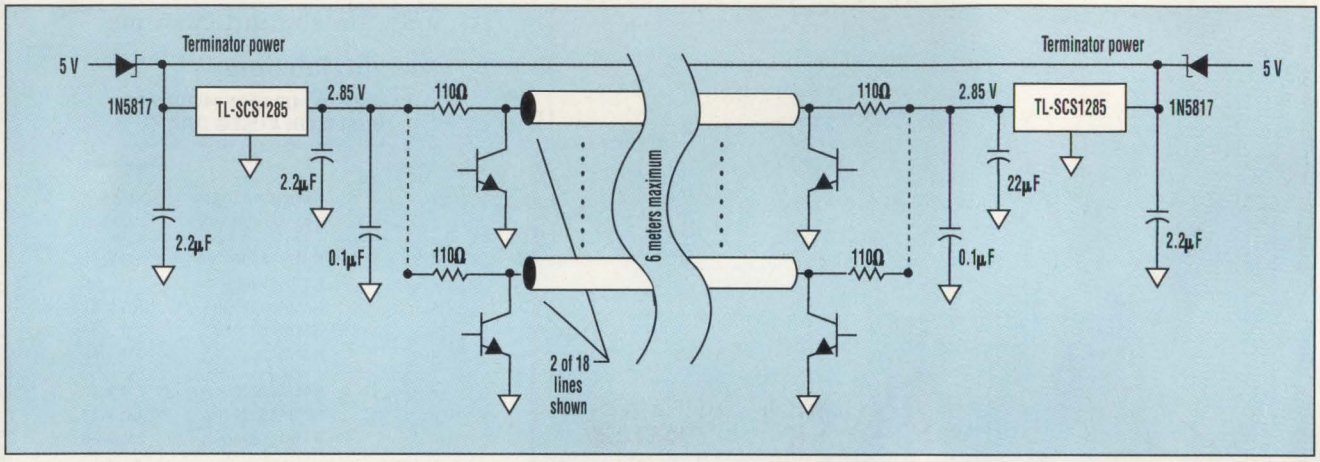
Technology that works for life.

CIRCLE 164 FOR U.S. RESPONSE

CIRCLE 165 FOR RESPONSE OUTSIDE THE U.S.

fers to about 1 Mbyte/s, even for short distances. To get faster data transfers, bus bandwith can be improved with the use of active termination—the placement of the Thevenin equivalent of the passive resistance in series with an active regulator with low-drop-out capability. That combination provides the current and noise margin needed to ensure low error rates and high-quality signals. Referred to as the Boullet terminator after the engineer who created it, the active termination scheme has become a de facto standard.

An improved active terminator circuit developed by Texas Instruments meets and exceeds all parameters for SCSI 1 alternative 2 termination *(see the figure)*. It provides the current needed by the 18 lines that have to be driven, while maintaining a drop-out voltage of just 0.6 V, rather than the 1.3 to 1.4 V that other terminators specify. That means that the chip can operate from a



3.5-V power supply—a key requirement in portable systems to ensure operation as battery voltages drop during use.

To achieve the low dropout voltage, designers at Texas Instruments created a fixed-voltage active terminator that delivers a 2.85-V output with a maximum output tolerance of within just 1% at a temperature of 25° C and an absolute tolerance of within 2% over all conditions (temperature, reference and line variations, and loading).

Laser-programmed fuses on the circuit are cut to trim the terminator to the desired tolerance. Furthermore, in designing the chip, Texas Instruments' engineers actually made the chip larger than called for in the basic design, so that the circuit geometries could be optimized to minimize parameter variations.

The 2.85-V voltage level is needed to keep the noise margin on the bus lines within proper levels. Thus the terminator circuit must maintain both the output level and the dropout voltage level over all conditions. Such consistent performance is needed as computer manufacturers now specify guaranteed performance levels over a wide range of operating conditions.

To deal with out-of-tolerance conditions, the regulators also include several protection circuits. For starters, an overcurrent-limiting circuit will limit the output current to 1 A—that's about a 33% overload over the 750 mA maximum rated load.

A thermal overload circuit also kicks in at a temperature of 175° C, and overvoltage protection will shut the terminator circuit down if a voltage of more than 30 V is sensed by the chip.

The regulator will be housed in several package options. These include a TO-220 3-terminal transistor-style case, as well as 14-pin DIPs and 20-pin thin scaled small-outline packages (TSSOPs).

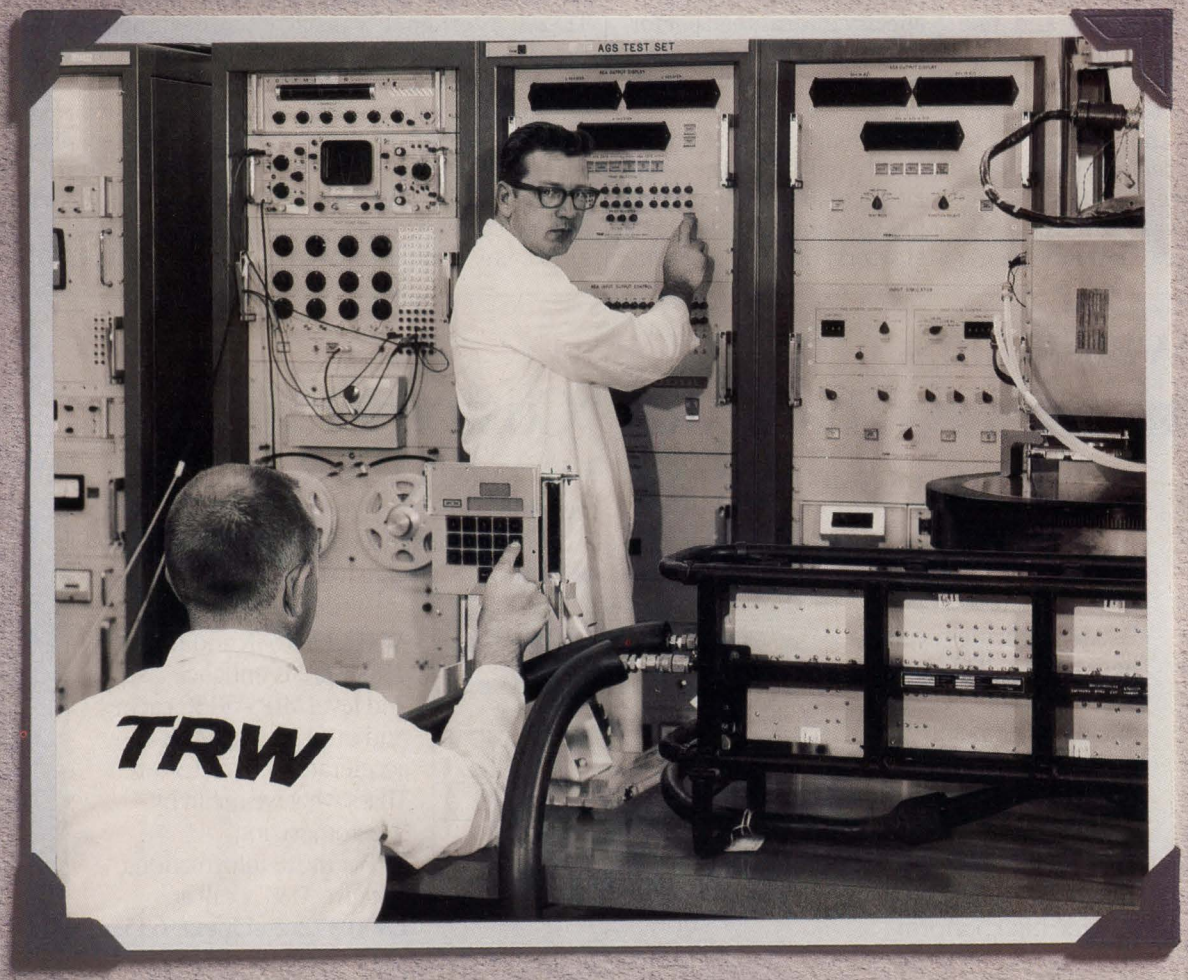
Most of the pins on the DIP and TSSOP packages are no-connect lines and serve as heat-removal paths, since termination typically adds between 1 and 2 W to the system power budget. In the quiescent state, though, the active terminator circuit consumes only a fraction of the power that passive termination would require.

In lots of 1000, the device will sell for $1.64 each. Some potential users of the chip are even considering embedding the terminator right inside the SCSI connector, thus saving the system designer the trouble of implementing the termination.

For more information on this active terminator circuit, contact Mark Granahan at Texas Instruments at (214) 997-5955.

DAVE BURSKY

WE DESIGNED THE BEST A/D CONVERTER IN NO TIME AT ALL. BUT THEN, WE HAD A 30-YEAR HEAD START.



8-bit resolution. 40 Msps. Two-step architecture and CMOS technology that reduces power dissipation to less than 180mW.

All with a significant cost advantage. And all from a single +5 Volt power supply.

That is the TMC1175, developed in only months by TRW LSI Products Inc. But then, that's what you can expect from the industry leader in high-performance A/D converters.

Our years of setting standards have given us the ability to respond quickly to changing needs in the industry, continually improving our line of products in terms of performance and cost. The same dedication to perfection that earned us an Emmy award in 1989 for video technology.

With the TMC1175, video driving amplifiers can be eliminated. The Track-and-Hold circuit is built-in; so is the voltage reference. All digital inputs and three-state outputs are TTL-compatible. And all performance specifications are guaranteed over the -20°C to 75°C temperature range.

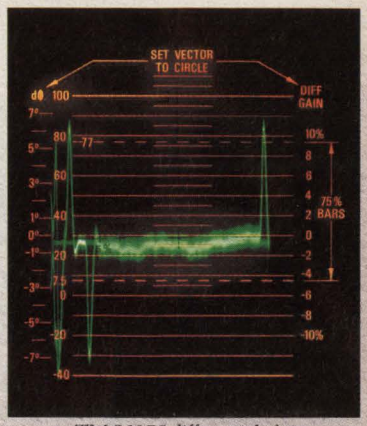
All of which makes the TMC1175 excellent for Digital Television designs. Video Digitizing. Image Scanners. Multimedia. And low cost, high speed Data Conversion. It can even be used in PC video board designs.

The TMC1175 is available in 24-pin plastic skinny DIP, 28-lead PLCC and 24-lead plastic SOIC (small outline) suitable for surface mount applications.

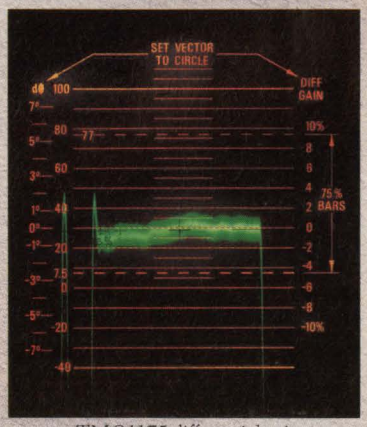
And of course, TRW LSI backs you with all the support you need. With field and in-house application engineers. Application notes. And a full line VLSI Data Book.

All with the full spec performance that is synonymous with TRW standards.

Ask for the Data Sheet, applications and other information on the TMC1175 today. You'll agree, it's an A/D converter that meets your standards. From the company that has been setting them for years.



TMC1175 differential phase



TMC1175 differential gain

Call or write: TRW LSI Products Inc.,
P.O. Box 2472, La Jolla, CA 92038
(619) 457-1000, FAX (619) 455-6314
(800) TRW-LSIP (800) 879-5747

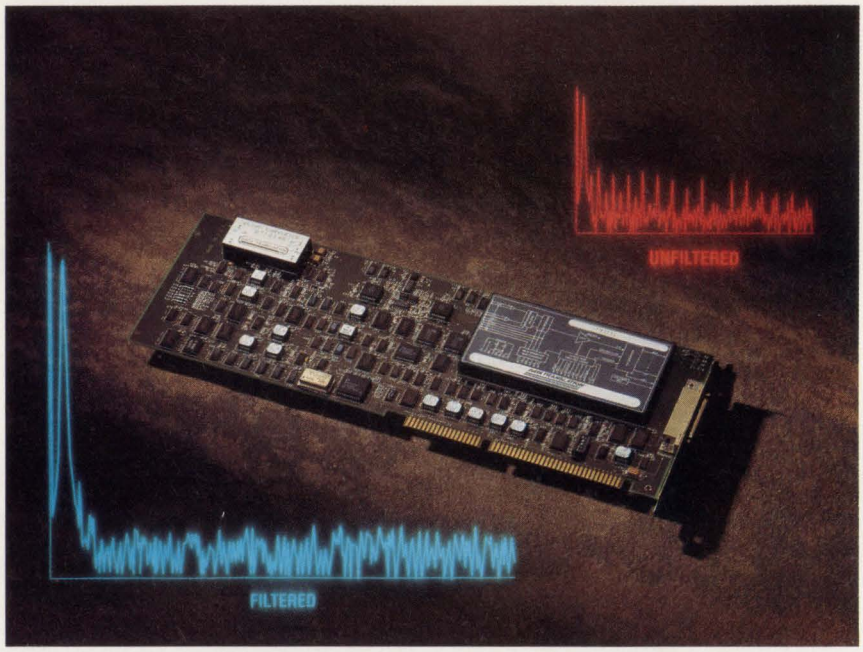
TRW LSI Products Inc.

STANDARDS SET. STANDARDS TO BE MET.

CIRCLE 203 FOR U.S. RESPONSE

CIRCLE 204 FOR RESPONSE OUTSIDE THE U.S.

FILTER OUT NOISE WITH NEW DATA ACQUISITION BOARDS



"Our new DT3831 Series boards reduce noise and maximize accuracy with onboard anti-aliasing filters and Real-Time Error Prevention™." *– Fred Molinari, President*

Superior accuracy and data integrity

- Onboard anti-aliasing filters with software-selectable cutoff frequencies
- *Real-Time* Error Prevention™
  On-the-fly offset and gain, correction for each combination of input channel, gain and range

High performance features

- Up to 250kHz gap-free DMA data transfer
- Simultaneous A/D and D/A
- Eight differential analog input channels
- Two analog output channels
- Two 16-bit counter/timers (Am9513A)
- Onboard data buffer, eight digital I/O lines

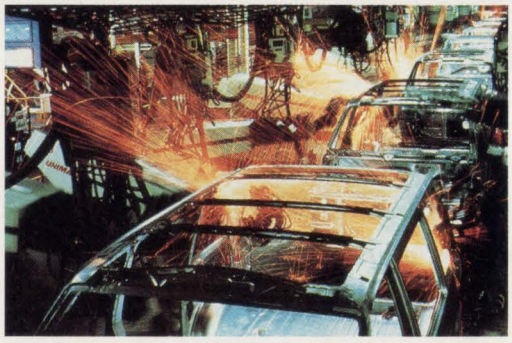
Complete software support for OEMs and end users

- FREE device driver and subroutine library
- GLOBAL LAB® application software

Member of the "Hands-Off"series

- Total software configuration and calibration of all board functions

Quantity pricing available ▪ Fast 5 day delivery



Combat Noise in the Harshest of Environments

Call for FREE catalog

(508) 481-3700

In Canada, call (800) 268-0427

THE LEADER IN DATA ACQUISITION AND IMAGE PROCESSING

DATA TRANSLATION®

World Headquarters: Data Translation, Inc., 100 Locke Drive, Marlboro, MA 01752-1192 USA, (508) 481-3700, Fax (508) 481-8620, Tlx 951646
United Kingdom Headquarters: Data Translation Ltd., The Mulberry Business Park, Wokingham, Berkshire RG11 2QJ, U.K., (734) 793838, Fax (734) 776670, Tlx 94011914
Germany Headquarters: Data Translation GmbH, Im Weilerlen 10, 7120 Bietigheim-Bissingen, Germany 7142-54025, Fax 7142-64042
International Sales Offices: Australia (2) 699-8300; Austria 22-236-7660; Belgium (2) 466-8199; Brazil (11) 240-0598; Canada (416) 625-1907; China (1) 513-7766 x 1222; Denmark 42 274511; Finland (0) 3511800; France (1) 69077802; Greece (1) 361-4300; Hong Kong (5) 448963; India (22) 23-1040; Israel 52-545685; Italy (2) 82470.1; Japan (3) 502-5550, (3) 5379-1971; Korea (2) 718-9521; Malaysia 3-2486788; Netherlands (70) 399-6360; New Zealand (9) 415-8362; Norway (2) 53 12 50; Poland (22) 580701; Portugal (1) 7934834; Singapore 338-1300; South Africa (12) 803-7680/93; Spain (1) 555-8112; Sweden (8) 761 78 20; Switzerland (1) 386-8686; Taiwan (2) 3039836

CIRCLE 100 FOR U.S. RESPONSE

CIRCLE 101 FOR RESPONSE OUTSIDE THE U.S.

AN ANALOG-BEHAVIORAL-MODELING APPROACH ACCOUNTS FOR FREQUENCY DEPENDENCE IN SYSTEM TRANSFER FUNCTIONS.

SIMULATING AUDIO TRANSDUCERS WITH SPICE

JEREMY AGNEW
Starkey Laboratories Inc.,
P.O. Box 8100,
Colorado Springs, CO 80933;
(719) 632-9331.

Simulation of electronic circuits during their design is essential both as a design tool and as a functional check. But simulating just one portion of a circuit, such as an IC op-amp block, isn't enough to fully understand system performance. Today's trend in circuit simulation is toward a comprehensive system-simulation approach. Current estimates are that 75% of circuit simulators are now also used for total system design, rather than just to simulate separate subcircuits or functional blocks within a design.

The standard simulation tool for analog-circuit design is Spice. At the PC level, the evolving standard is PSpice, which is a direct Spice derivative. For circuits with an electrical input and output, Spice is a capable and accurate tool for circuit simulation. Also, electronic-circuit modeling with Spice has become well-established. Moreover, accurate device models are available for common electronic components, such as transistors, resistors, diodes, inductors, and capacitors. Unfortunately, simulation models of audio transducers to interface with electronic circuits aren't readily available.

This lack of transducer models presents a particular problem for designers of audio-amplifier ICs, who must link their circuits with electro-acoustic devices, such as microphones, earphones, and loudspeakers. Audio designers are typically interested in the overall acoustic response of their system, manipulating the design's electronics to achieve the desired acoustic results. Thus, the overall design is often approached from the point of view of the system acoustic-transfer function. For designers of audio ICs in particular, the lack of electro-acoustic models of microphones, earphones, and loudspeakers for direct inclusion into simulations decreases the likelihood of successfully integrating silicon on the first pass.

SUBTLE FACTORS

Audio-amplifier-IC design would seem to be straightforward, but subtle factors often must be accounted for when transducers are attached to the amplifier input and output. Most early audio-amplifier designs concentrated on simple voltage amplification. Today, however, newer techniques in IC design can alter amplifier output impedance, transducer loading, current drive, and voltage amplification at different frequencies. These alterations optimize the acoustic design and compensate for undesired peaks and valleys in the acoustic system response. These undesirable fluctuations in frequency response often result in altered perceptions of sound, some of which may be quite significant in terms of sound quality and intelligibility for the listener.

Because of several interactions that occur between microphone, speaker,

SIMULATING AUDIO TRANSDUCERS WITH SPICE

and amplifier in an audio system, it's advantageous to use simulation techniques. For example, it's well known that audio amplifiers behave differently when attached to different loads. Part of this is because dynamic output transducers, such as loudspeakers or earphones, don't present a constant impedance to the amplifier that drives them. That's due to the inductive effects of their electromagnetic coils. This impedance variation will affect the compensation and stability that must be designed into the output stage. In a similar manner, mismatching of impedance characteristics between the microphone output and an amplifier's input stage can affect overall performance of the system.

A different example involves using the inductive load of a high-impedance electromagnetic earphone, especially in a push-pull configuration. In such conditions, the peak-to-peak output driving voltage can rise higher than the power-supply voltage. This effect can't happen when substituting a resistor load for an earphone during simulations.

Another design factor to consider is that the loading reflected back to the amplifier from an output transducer will vary according to the acoustic conditions of its use. These conditions may include radiation into open air (for example, a loudspeaker) or into a closed ear cavity (an earphone). Such changes typically reflect back to the output amplifier as impedance variations in the circuit.

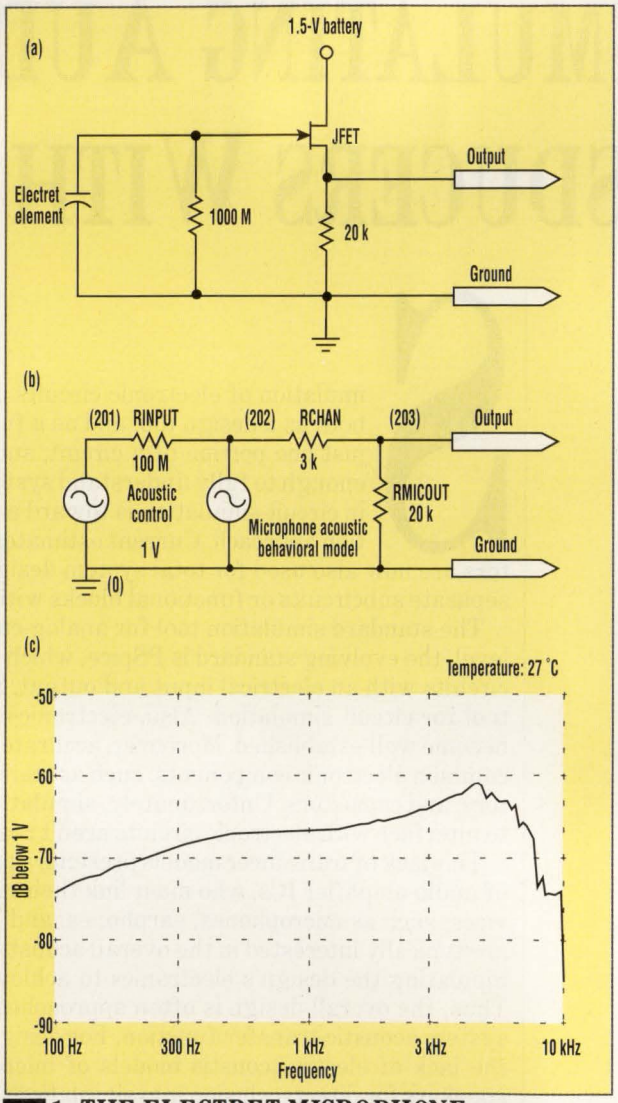
Other interacting electrical parameters of the amplifier and its load include: the amplifier's output impedance, the dc resistance and ac impedance of the load, the variation of ac impedance with frequency, and the dc current through the earphone's coil. The latter must often be set at a predetermined value to bias the device into its linear operating region.

Very few simulation models account for all of these factors. Hence, the author was unable to find any microphone and earphone models usable for ac and dc Spice simulations of acoustic systems which did so. The commonly available acoustic models were developed primarily by using electrical analogs to analyze and simulate acoustic results. Typically, these analog-based models represent acousto-mechanical parameters, including acoustic mass, mechanical stiffness, damping, compliance, and radiation resistance of loudspeakers or earphones in terms of electrical quantities. Equations are developed using these analogs to represent the dynamic acoustic behavior of the transducer, and then are solved by standard methods of analyzing electrical networks.

These analog electrical quantities are merely a convenience to model the device's acoustic and electromechanical behavior. They're not exact electrical equivalents to be used for ac and dc analysis during circuit simulation. Consequently, very few of these models can be included directly in amplifier-design simulations to predict overall system performance. Very often, these models also contain inaccuracies thanks to simplifying assumptions made about such factors as mechanical and acoustic damping, acousto-mechanical coupling coefficients, and mechanical compliance. All of those factors may vary with frequency, drive voltage, and the acoustic load on the transducer.

The traditional approach to modeling system transfer functions is by means of polynomial equations. Although standard Spice and PSpice implementations of controlled sources allow polynomial controlling functions, they have three limitations. For one, many transfer functions aren't well represented by polynomials. Also, specification of the polynomial is usually quite difficult. Finally, polynomial modeling doesn't allow frequency-dependent behavior to be specified.

In general, the polynomial tech-



1. THE ELECTRET MICROPHONE to be modeled contains a built-in FET source follower (a). Its equivalent PSpice electrical circuit models the microphone's electrical parameters, along with the control generators used to simulate the acoustic output (b). The output of a PSpice simulation run shows the microphone model's acoustic frequency-response curve, which agreed well with the manufacturer's data sheet (c).

Limited Only By Your Imagination

Remember how quickly you could turn a concept into reality with a set of quality building blocks? How you always seemed to have just the right parts and how well they fit together? How easily you could modify your creation to explore creative alternatives?

Our VI-200 and VI-J00 families of high density converters, along with a host of compatible modular peripheral products, are designed to "plug and play" perfectly... offering you the flexibility, ease-of-use, quality and repeatability needed to implement virtually any power system solution. And with hundreds of standard models to choose from...input ratings from 10 to 400 Volts, outputs from 2 to 95 Volts and power expansion from Watts to kiloWatts... you won't be stuck at the last minute with "missing" parts.

You're not playing with toys anymore...which may be the most important reason for specifying Vicor's component-level "building blocks" for your next power system.

Component Solutions For Your Power System

VICOR

23 Frontage Road Andover, MA 01810
TEL: (508) 470-2900 FAX: (508) 475-6715

CIRCLE 180 FOR U.S. RESPONSE

CIRCLE 181 FOR RESPONSE OUTSIDE THE U.S.

SIMULATING AUDIO TRANSDUCERS WITH SPICE

TABLE 1: PSPICE ANALOG MODEL INPUT-FILE SYNTAX

<model name>	<+node>	<–node>	FREQ	{<control source>} =
+	<frequency>	<magnitude value>	<phase value>	
+	<frequency>	<magnitude value>	<phase value>	
+	<frequency>	<magnitude value>	<phase value>	
+	etc.			

nique is limited to relatively simple circuit analysis, or to the solution of equations that might be solved by La-Place-transform techniques. As a more specific problem for audio designers, acoustic transducers typically have frequency responses that require some method of simulation that considers frequency dependence.

The analog-behavioral-modeling technique of PSpice bypasses these limitations. This simulation technique enables a device's transfer function to be described by a voltage source that's controlled by a frequency-response table containing the magnitude of the response for each frequency. Using this method, acoustic models of transducers may be developed from measurements made on real devices under the real-world conditions of interest, and the resulting data included in a PSpice input file for exact circuit simulation.

LITTLE TO GO ON

Because of the newness of this technique, very little published reference material exists. For more specific details on behavioral modeling, there's the *PSpice Operating Manual, Version 4.04*.[1] Other various standard sources are available for more detailed information on the general use of Spice and PSpice for simulation.[2,3,4]

The transducer modeling described in this article aimed at accurate simulation of electro-acoustic transducers for connection to different audio amplifiers during integrated-circuit design. Once a particular transducer model was developed, it simulated the acoustic effects of changes in design aspects of the integrated-circuit amplifiers, such as the effects of stability compensation and varying internal circuit-feedback loops. The simulations also aided in modifying the electronic design to compensate for the nature of the earphone's acoustic frequency response. That's because electrical and acoustic resonances of microphones and earphones have a major impact on determining the overall frequency response of the entire system.

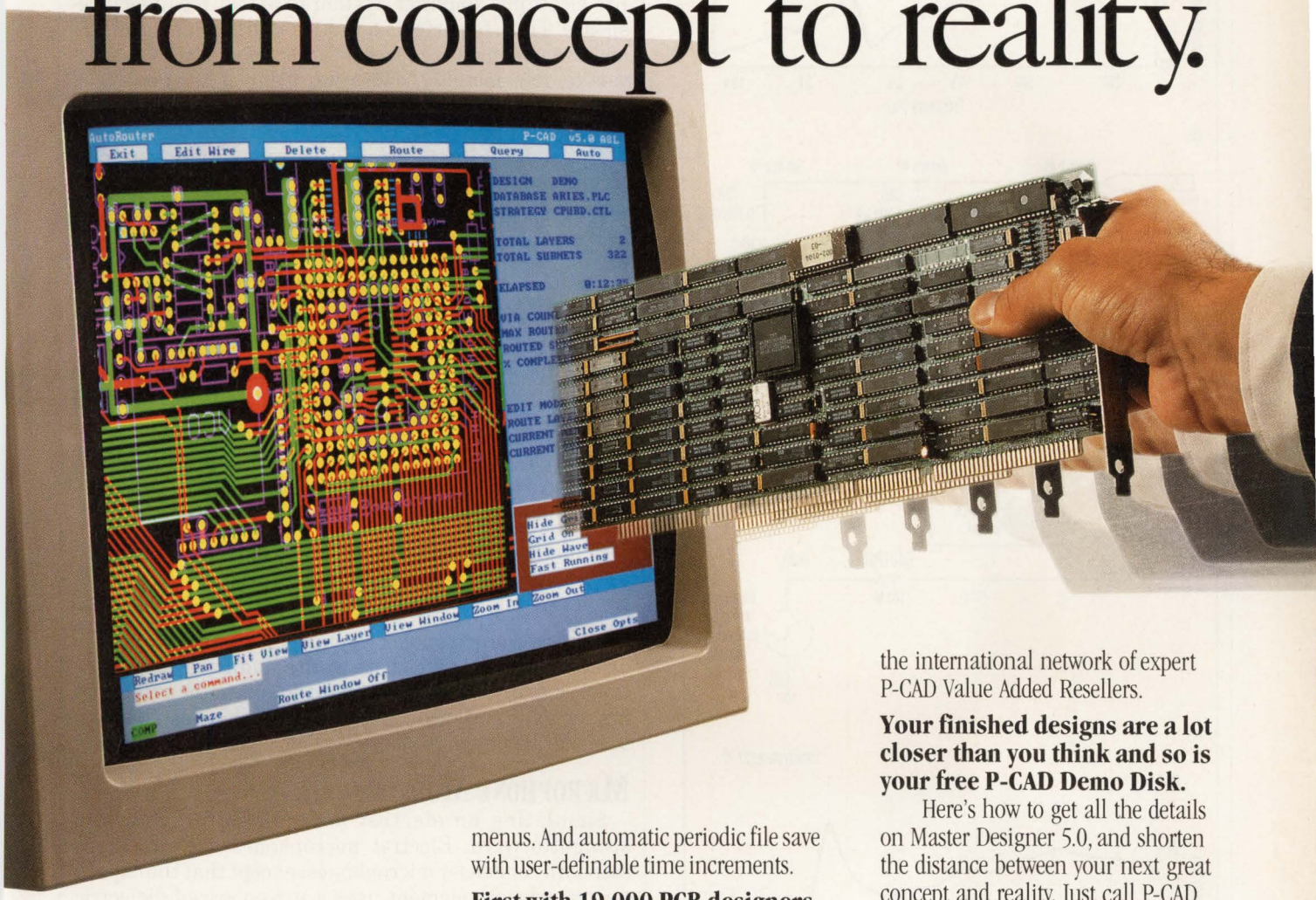
The two examples described here illustrate the general techniques used to model and simulate an input transducer (an electret microphone) and an output transducer (an electromagnetic earphone), and then to connect these two models as input and output transducers for an IC design to produce a small audio-amplifying system. An electret microphone was chosen to give variety to the examples, though a model for a dynamic microphone could have been developed with a technique similar to that used for the earphone.

In addition to acoustic models of these transducers, it was necessary to create electrical models of both input

TABLE 2: MODEL OF EK3024 MICROPHONE FOR PSPICE

```
* EK3024 behavioral model with 60-dB input *
VIN          201      0      AC   1
RMIC           9      0      44 kΩ
RINPUT       201    202      100 MΩ
RCHAN        202    203      3 kΩ
RMICOUT      203      0      20 kΩ
EEK3024      202      0      FREQ {V(201,0)} =
+   100,    -73.0,    -27
+   125,    -71.4,    -77
+   150,    -70.8,    -110
+   175,    -69.7,    -128
+   200,    -69.4,    -132
+   250,    -68.3,    -133
+   300,    -67.4,    -135
+   400,    -66.3,    -149
+   500,    -65.7,    -152
+   600,    -65.7,    -153
+   700,    -65.6,    -155
+   800,    -65.5,    -162
+   900,    -65.4,    -167
+  1000,    -65.3,    -169
+  1100,    -65.2,    -169
+  1200,    -65.2,    -171
+  1300,    -65.2,    -173
+  1400,    -65.0,    -174
+  1500,    -64.9,    -175
+  1600,    -64.6,    -174
+  1700,    -64.5,    -176
+  1800,    -64.3,    -177
+  1900,    -64.1,    -178
+  2000,    -64.2,    -179
+  2100,    -63.9,    -180
+  2200,    -63.8,     180
+  2300,    -63.7,     179
+  2400,    -63.5,     179
+  2500,    -63.4,     176
+  2600,    -63.2,     175
+  2700,    -62.9,     173
+  2800,    -62.8,     172
+  2900,    -62.7,     171
+  3000,    -62.6,     170
+  3200,    -62.1,     167
+  3400,    -61.6,     164
+  3600,    -61.3,     160
+  3800,    -61.0,     155
+  4000,    -61.0,     150
+  4250,    -60.3,     143
+  4500,    -59.5,     134
+  4750,    -59.4,     124
+  5000,    -61.4,     114
+  5250,    -60.7,     104
+  5500,    -61.6,      95
+  5750,    -61.8,      85
+  6000,    -61.6,      77
+  6250,    -62.9,      69
+  6500,    -61.9,      65
+  6750,    -64.8,      61
+  7000,    -64.2,      58
+  7250,    -64.8,      57
+  7500,    -65.5,      55
+  7750,    -67.4,      55
+  8000,    -73.7,      56
+  8250,    -70.2,      56
+  8500,    -73.1,      55
+  8750,    -73.0,      51
+  9000,    -73.0,      51
+  9250,    -73.1,      50
+  9500,    -73.2,      49
+  9750,    -71.7,      49
+ 10000,    -83.2,      49
```

Master Designer 5.0, the shortest distance from concept to reality.



Master Designer™ 5.0 is the shortest distance from PCB design concept to reality. And the fastest, most productive and reliable way to get your designs to market using an IBM® or compatible PC.

And now Master Designer 5.0 has been enhanced with more than 100 new features, requested by PCB master design engineers like you.

New features, more productivity.

Master Designer 5.0 shortens the entire design cycle with new features like extended memory for 4-times larger designs. Automatic real-time on-line design rule checking. User configurable menus. And automatic periodic file save with user-definable time increments.

First with 19,000 PCB designers.

You can rely on Master Designer 5.0 for the quality and dependability that has made it the choice of more than 19,000 PCB designers worldwide.

Master Designer 5.0 gives you the interactive support of Master Layout™ to handle surface mount, analog, and digital technology. The flexibility of Master Schematic™, fully automated optional Rip-n-Route, and our optional Master Placer™. Not to mention the plus of a consistent menu-driven interface.

With Master Designer 5.0, you're backed by CADAM, the world's leading CAD/CAM/CAE software supplier, and the international network of expert P-CAD Value Added Resellers.

Your finished designs are a lot closer than you think and so is your free P-CAD Demo Disk.

Here's how to get all the details on Master Designer 5.0, and shorten the distance between your next great concept and reality. Just call P-CAD toll-free today and we'll send your free Master Designer 5.0 Demo Disk absolutely free.

1-800-255-5710

World Class PCB CAD Productivity

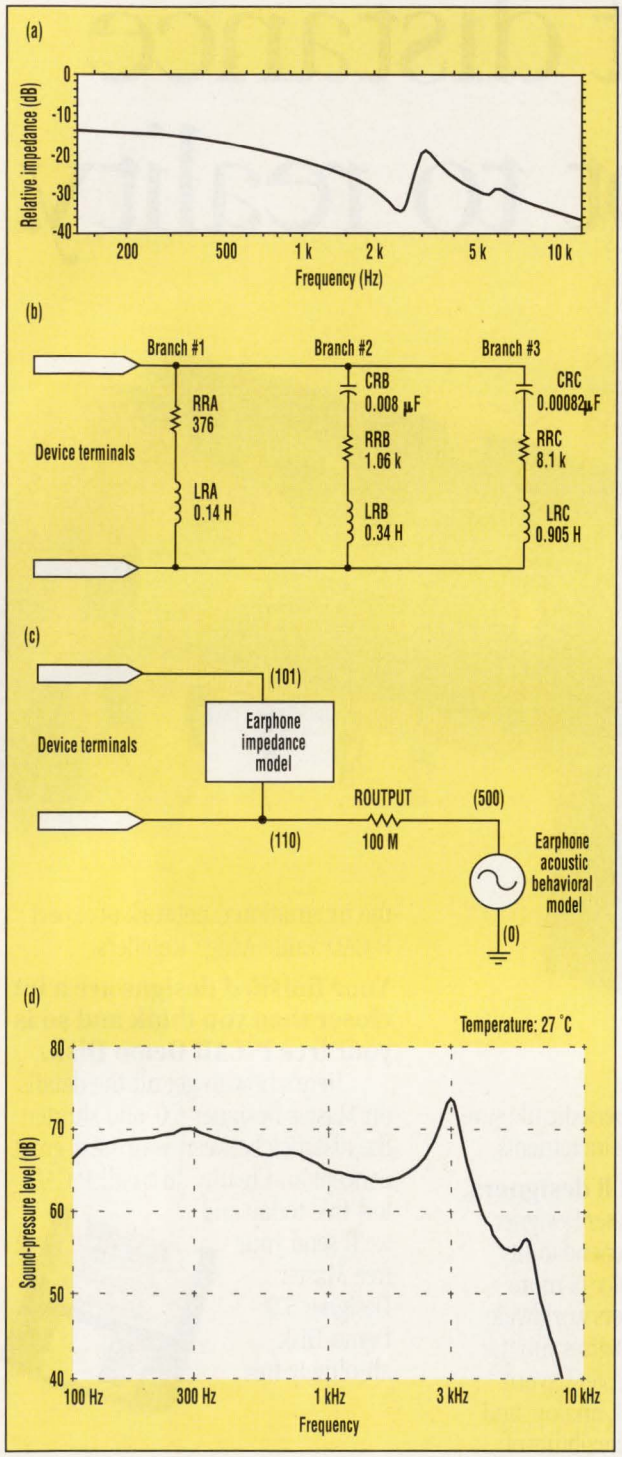
p-cad®

PRODUCTS FROM CADAM, AN IBM COMPANY

See Us At WESCON, Booth #'s 1235 to 1238

CIRCLE 146 FOR U.S. RESPONSE **CIRCLE 147 FOR RESPONSE OUTSIDE THE U.S.**

SIMULATING AUDIO TRANSDUCERS WITH SPICE



2. A GRAPH plots the impedance versus frequency for the dynamic earphone (a). An electrical network models this relationship (b). This network was used as a direct ac and dc load for PSpice simulation. A diagram of the model used to simulate the acoustic output from the earphone incorporates the electrical model (c). The output of a PSpice simulation run shows the acoustic-output-versus-frequency curve of the earphone model, which complied with the manufacturer's data sheet (d).

and output devices for PSpice that could be directly connected to the circuit. These models were needed to accurately simulate their electrical effects on acoustic performance. Electrical-transducer parameters may interact with feedback loops and other design features of the entire electronic-amplifier system to affect frequency response. Thus, to perform a total amplifier simulation, dc and ac modeling were essential. Spice performs a dc analysis to determine the operating point of the active devices in the circuit before performing the subsequent ac analysis.

The audio-system modeling described here was performed in five steps:

1. Creation of an electrical model of the microphone that could be connected to an audio-amplifier input.

2. Creation of an electro-acoustic-behavioral model of the microphone that gives a frequency-dependent electrical-output signal in relation to the acoustic input.

3. Creation of an electrical model of an earphone that could be used as a direct electrical ac and dc load on an amplifier.

4. Creation of a frequency-dependent, electro-acoustic-behavioral model of the earphone to simulate an acoustic-output level in relation to input-drive voltage.

5. Connection of the microphone and earphone models to the amplifier model and simulation of the overall system frequency response.

Though the particular application of this technique and the examples given here were actually developed for the design of hearing-aid ICs (to simulate the effects of highly nonlinear earphones), this technique can be used to model any audio transducers.

MICROPHONE MODELING

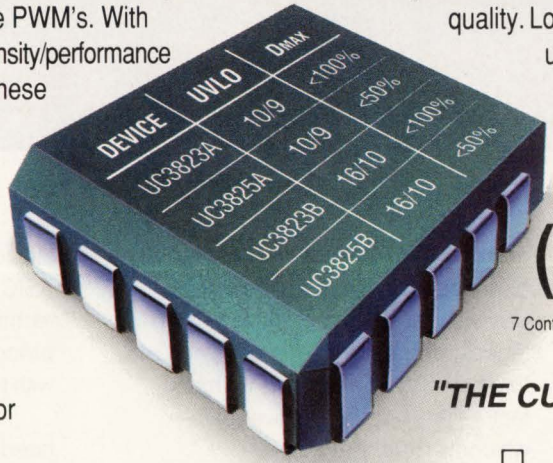
Simulating an electret microphone is relatively straightforward. Electret microphones are similar to standard condenser microphones, except that the capacitor transducing element uses a pre-polarized dielectric between the capacitor plates instead of using a high-voltage power supply to polarize the dielectric. An electret microphone typically contains a built-in FET source follower to convert the high impedance of the capacitor transducer element to a low output impedance suitable for matching to a bipolar-amplifier input stage. This type of microphone is often used in portable tape recorders, sound-level meters, PA systems, and for other general-purpose microphone uses.

The equivalent schematic circuit of the microphone example can be illustrated *(Fig. 1a)*. The empirically derived electrical circuit model for PSpice can also be shown *(Fig. 1b)*. RMICOUT simulates the microphone output resistance as it was measured on the bench. RCHAN models the channel-resistance effects of the FET used for impedance matching. The 1000-MΩ resistor from gate to ground is so large that it can be ignored for modeling purposes *(Fig. 1a, again)*.

All It Takes Is The *Right* Power

Unitrode Integrated Circuits announces the next generation of industry standard current mode PWM's. With increased demands on higher density/performance power supply designs, consider these features of the **UC3823A** and **UC3825A** family:

- Adjustable blanking of leading edge current noise
- Trimmed oscillator discharge for accurate frequency and dead time control
- Latched over current comparator
- Full cycle restart after fault
- Outputs active during UVLO
- Optional UVLO thresholds
- MHz+ performance



We guarantee a continued commitment to uncompromised quality. Look to Unitrode Integrated Circuits to provide unique solutions for your design needs. For more information on the **UC3823A** and **UC3825A** family, contact your Unitrode Representative or call:

(603)424-2410

7 Continental Boulevard, Merrimack, NH 03054 FAX (603) 424-3460

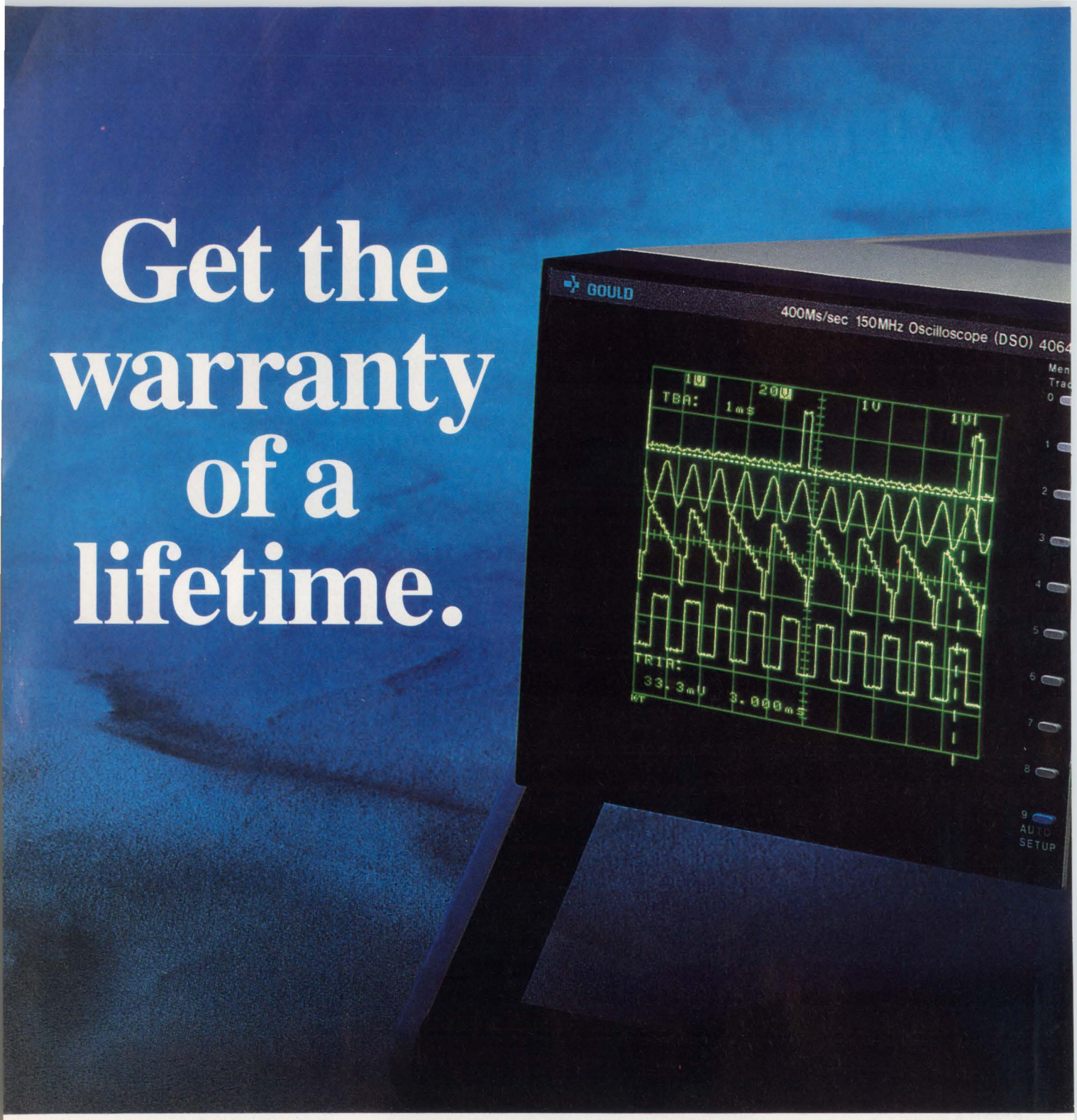
"THE CURRENT MODE PWM LEADER"

INTEGRATED CIRCUITS
UNITRODE

CIRCLE 222 FOR U.S. RESPONSE

CIRCLE 223 FOR RESPONSE OUTSIDE THE U.S.

Get the warranty of a lifetime.



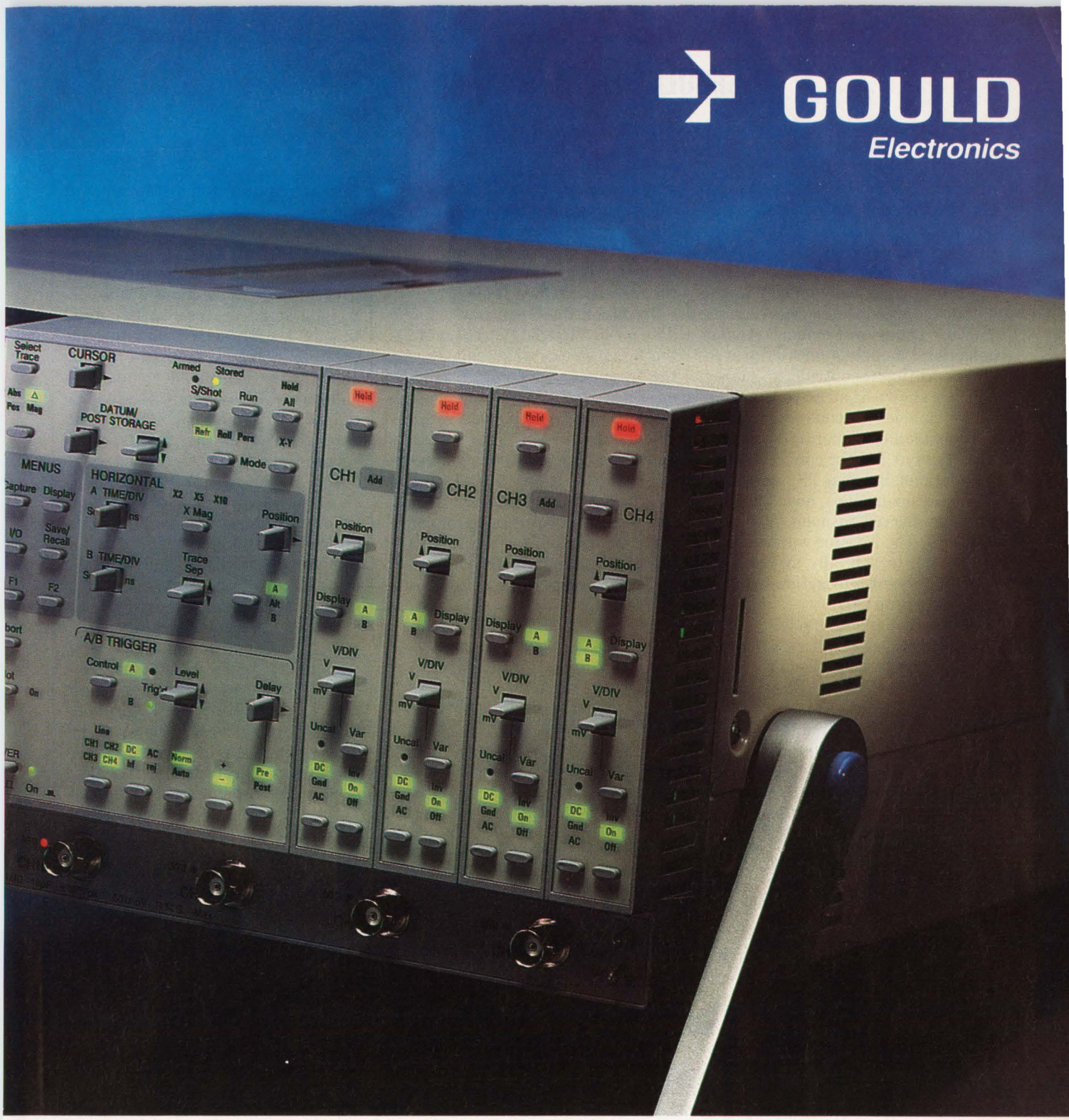
At Gould, we're so sure about the reliability of our new 4060 family of high-performance digital storage oscilloscopes, we back them with the longest warranty in the industry. You're fully covered for as long as we manufacture the product—or five years—whichever is longer.

How can we make that promise? With complete confidence.

Because we control quality every step of the way. Everything from our ASIC and advanced surface-mount technology to our sophisticated burn-in process is designed to provide you with the most reliable DSO made.

And the high performance you need for both repetitive and transient signal capture.

Available in 2- and 4-channel versions, the 4060 gives you 400MS/sec sampling at a 150MHz



bandwidth, 8–bit resolution, on-screen signal measurement and analysis, plus glitch capture. What's more, you can get IEEE-488.2 and RS-423 interfaces, and an integral 4-color pen plotter or thermal array printer for instant hardcopy. Our intuitive push-button panel makes everything strikingly simple to use.

In fact, about the only thing we haven't built into the 4060 series is a high price. It's about half of what you're used to paying.

And you'll find the same advantages across Gould's entire line of new oscilloscopes.

For an on-site demonstration, and details regarding the warranty, call Gould at (216) 328-7000. You'll be glad you did for years to come.

CIRCLE 104 FOR U.S. RESPONSE

CIRCLE 105 FOR RESPONSE OUTSIDE THE U.S.

Yes! ☐ Rush me a free 4060 brochure
☐ Have a Gould representative call to arrange a demonstration
☐ Send me a free DSO catalog

Name: _____

Title: _____

Company: _____

Street: _____

City: _____ State: _____ Zip: _____

Telephone: _____

Send to: Gould Inc., Test and Measurement Group, 8333 Rockside Road, Valley View, Ohio 44125.
Fax: (216) 328-7400.

ED 11/91

SIMULATING AUDIO TRANSDUCERS WITH SPICE

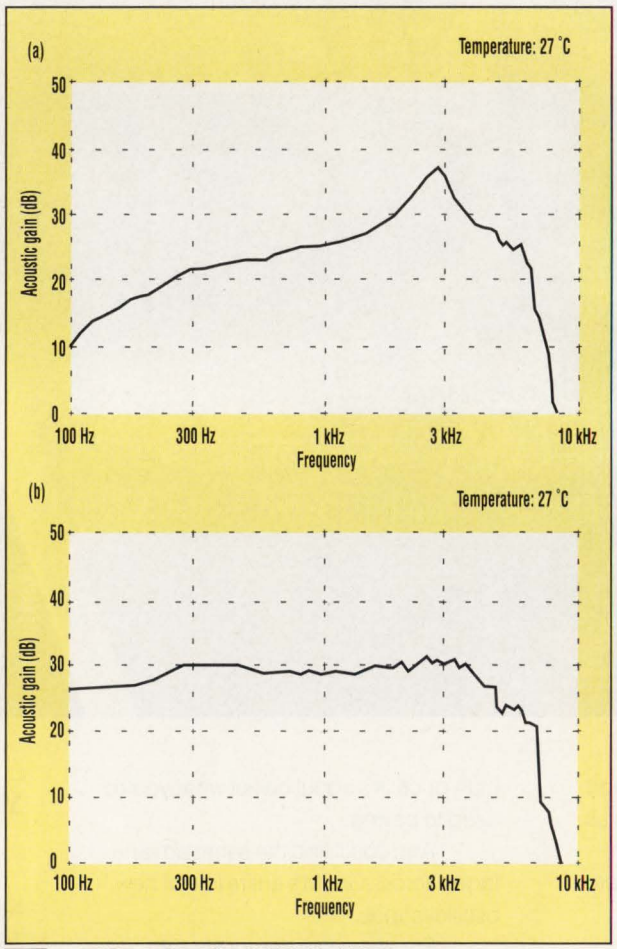
Using analog behavioral modeling, the microphone's electrical output was simulated as an ac voltage source with a specific frequency response. The electrical output from the microphone was modeled as the voltage source labeled "microphone acoustic-behavioral model." Analog behavioral modeling with PSpice requires an input-controlling source, which is shown as an ac-voltage generator labeled "acoustic control." This controlling generator was arbitrarily set at 1 V for convenience of calculations. Because PSpice doesn't allow any open nodes, node (201) had to be connected to node (202) with RINPUT. The resistor value was set at 100 MΩ (essentially an open circuit) to prevent interaction between nodes (201) and (202).

Analog behavioral modeling with PSpice requires a specific syntax for values in the input file *(Table 1)*. The term <magnitude value> is expressed as the magnitude, in decibels, of the response at each frequency with respect to the controlling voltage. Because the controlling voltage in Fig. 1b was arbitrarily set at 1 V, each magnitude value for the PSpice model was calculated as decibels below 1 V. The term <phase value> is the phase of the electrical output with respect to the acoustic input. This phase information is generally useless in IC simulation. As a result, if it can't be conveniently measured, this column of the model may be filled with zeros without affecting the frequency-response simulation results.

To create the data for the model, a "standard" microphone was measured on the bench. The microphone was placed in a constant sound field with a 60-dB sound-pressure level (SPL), which is roughly the acoustic level of conversational speech at 1 meter. Other sound levels could be just as easily measured to create the model, or substituted during simulation by raising or lowering the control generator in Fig. 1b by the desired number of decibels, using 1 V = 60-dB SPL as the reference point *(Table 2)*.

To obtain the frequency-response data needed for the PSpice input file, the signal source was stepped across the frequency spectrum at suitable intervals and the output voltage from the microphone was recorded at each frequency. This measured output-voltage data was converted into decibels below 1 V. To do so, standard computerized data-acquisition techniques were used for convenience. A text editor was employed to put the resulting frequency-versus-output-magnitude data into the format required for a PSpice input file.

As an example of the simulation format, the full electret-microphone model is given *(Table 2, again)*. VIN lists the node connections of the controlling ac generator and its magnitude of 1 V. Directly below this are the four resistors from the model, along with their node connections and values. Below them is the acoustic model, named EEK3024, with data entered in the frequency-response-table format described previously. A printout of a PSpice analysis of the microphone model's acoustic output shows its nonlinear frequency response *(Fig. 1c)*. A comparison of this graph with the manufacturer's data sheet for this microphone showed the results to be accurate.



3. THE PSPICE-SIMULATED system acoustic frequency response for the audio amplifier, microphone for acoustic input, and earphone for acoustic output shows an undesirable peak of 3 kHz and excessive low-frequency roll-off (a). A subsequent simulation, with a redesigned amplifier, represents an effort to smooth out the response curve (b).

Constructing the electrical model of the earphone was somewhat more complex. A dynamic earphone produces an acoustic output by means of ac current flowing through a coil wound around a magnet as the motor element. This drives a diaphragm to create a varying sound pressure. Because of this construction, an earphone (or a loudspeaker, which is very similar) has a large inductive, as well as resistive, component. The ac impedance and acoustic output are both frequency-specific because of various mechanical and acousto-mechanical couplings within the device.

For this example, it was necessary to simulate the earphone impedance versus frequency *(Fig. 2a)*. This impedance was specified and measured for the actual conditions of use. That's because changes in acoustic loading on the earphone will reflect backwards through acousto-mechanical couplings and produce variations in impedance presented to the amplifier. The impedance variations will shift

GOULD
Electronics

More guaranteed good news.

Good news travels fast.

Because now you can get the industry's longest warranty on the fastest digital storage oscilloscope in its class.

The new Gould 465 portable DSO.

The 465 gives you 100MHz bandwidth with a full 200MS/sec sampling on two channels—which is up to 20 times faster than similarly priced DSOs. Combined with 2GS/sec equivalent time sampling, the 465 excels at capturing both repetitive and transient signals.

That's in addition to all the advanced features packed into this small DSO, like automatic on-screen measurements, persistence mode, glitch capture, IEEE-488.2 (SCPI) and RS-423 interfaces, and a built-in 4-color pen plotter. All intuitively simple to use.

And like the rest of Gould's new line of DSOs, the 465 is warranteed as long as Gould manufactures the product—or a full five years—whichever is longer.

For an on-site demonstration, and details regarding the warranty, call Gould today at (216) 328-7000. You'll like what you see. Guaranteed.

Yes! ☐ Rush me a free 465 brochure
☐ Have a Gould representative call to arrange a demonstration
☐ Send me a free DSO catalog

Name: _____
Title: _____
Company: _____
Street: _____
City: _____ State: _____ Zip: _____
Telephone: _____

Send to: Gould Inc., Test and Measurement Group, 8333 Rockside Road, Valley View, Ohio 44125.
Fax: (216) 328-7400.

ED 11/91

CIRCLE 188 FOR U.S. RESPONSE

CIRCLE 189 FOR RESPONSE OUTSIDE THE U.S.

SIMULATING AUDIO TRANSDUCERS WITH SPICE

the frequency and amplitude of the resonant peaks appearing in the graph at 3 kHz and 6 kHz. Changes in the ratio of current feedback to voltage feedback within the driving amplifier can make significant differences in the system electrical loading and the overall frequency response, particularly in the region of these resonant peaks or the slopes leading up to the peaks.

By using an empirical approach, and monitoring the results with PSpice, it was possible to construct an impedance model for this earphone in the form of a ladder network of cascaded filter sections. This was done using electrical-network-synthesis techniques. Network-synthesis methods are covered in standard texts.[5] The generalized network developed to simulate the earphone impedance is shown *(Fig. 2b)*. The overall change in impedance with frequency is simulated by branch #1 of the network, and the secondary resonant peaks in the curve are simulated by branches #2 and #3 of the ladder. At dc, the model defaults to the value of dc resistance (in this case, 376 Ω) given in the manufacturer's specifications. Subsequent PSpice simulation of the impedance network showed the results to be very close to the curve given *(Fig. 2a, again)*.

An earphone's acoustic output is proportional to the voltage impressed across its terminals within its linear operating range. That range, which is below distortion levels, is the region of interest. Thus, an acoustic-behavioral model was created by applying a voltage across the earphone's electrical-impedance model at different frequencies and using analog behavioral modeling to predict the corresponding acoustic SPL output levels. Like the microphone, the earphone's acoustic output was modeled using analog behavioral modeling to create an ac-output voltage with a specific frequency response, controlled by an ac-input voltage. The ac-output voltage was used as an analog to correspond to direct acoustic SPL output. A primary advantage of using behavioral modeling to simulate acoustic performance is that the models are derived from actual use conditions, which means that they're extremely accurate for those conditions.

The generalized electro-acoustic model of the earphone is shown *(Fig. 2c)*. The block marked "earphone impedance model" is the electrical model *(Fig. 2b, again)*. As before, because of the requirements of PSpice, the electrical and acoustic impedance models are linked with a 100-MΩ resistor to prevent the formation of open nodes.

Similar to the method used to develop the microphone model, the output of a "standard" earphone was

TABLE 3: MODEL OF ED1913 RECEIVER FOR PSPICE

```
* ED1913 impedance model *
RRA      101      102      376
LRA      102      110      0.14 H
CRB      101      103      0.008 mF
RRB      103      104      1.06 kΩ
LRB      104      110      0.34 H
CRC      101      105      0.00082 mF
RRC      105      106      8.1 kΩ
LRC      106      110      0.905 H

* ED1913 behavioral model *
ROUTPUT  110      500      100 MΩ
EED1913  500      0        FREQ {V(110)} =
+  96,   40.80,   175
+  112,  42.88,   140
+  128,  43.10,   110
+  144,  43.48,   81
+  160,  43.76,   54
+  176,  43.85,   24
+  192,  43.93,   –7
+  208,  43.98,   –32
+  224,  44.32,   –55
+  240,  44.44,   –72
+  256,  44.81,   –88
+  272,  45.02,   –98
+  288,  45.12,   –109
+  304,  44.80,   –117
+  320,  44.48,   –125
+  336,  44.30,   –132
+  352,  44.13,   –139
+  384,  43.77,   –150
+  416,  43.45,   –159
+  448,  43.33,   –167
+  496,  42.61,   –176
+  528,  42.15,   176
+  576,  41.80,   171
+  640,  42.15,   166
+  688,  42.19,   162
+  752,  42.03,   151
+  816,  41.57,   143
+  896,  40.89,   134
+  976,  40.27,   128
+  1072, 39.86,   122
+  1168, 39.63,   116
+  1264, 39.26,   111
+  1392, 39.24,   105
+  1520, 38.69,   99
+  1664, 38.76,   94
+  1808, 39.07,   88
+  1984, 39.52,   81
+  2032, 39.84,   79
+  2080, 39.92,   76
+  2128, 40.34,   74
+  2176, 40.44,   71
+  2224, 40.71,   69
+  2272, 40.93,   66
+  2320, 41.13,   64
+  2384, 41.54,   61
+  2432, 42.13,   58
+  2480, 42.49,   55
+  2544, 43.37,   51
+  2608, 43.99,   46
+  2656, 44.64,   43
```

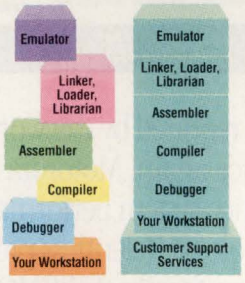
(continued at right)

```
+  2720, 45.65,   35
+  2784, 46.86,   27
+  2848, 47.83,   16
+  2912, 48.39,   2
+  2976, 49.07,   –15
+  3056, 48.31,   –36
+  3120, 47.46,   –51
+  3184, 46.08,   –63
+  3264, 44.54,   –74
+  3344, 42.99,   –83
+  3408, 42.01,   –88
+  3488, 40.71,   –95
+  3568, 39.49,   –100
+  3648, 38.42,   –104
+  3744, 37.18,   –108
+  3824, 36.31,   –110
+  3920, 35.19,   –114
+  4000, 34.57,   –117
+  4096, 33.85,   –120
+  4192, 33.41,   –123
+  4288, 32.95,   –126
+  4384, 32.26,   –130
+  4480, 31.80,   –131
+  4592, 31.34,   –135
+  4688, 31.13,   –137
+  4800, 30.64,   –141
+  4912, 30.53,   –144
+  5024, 30.35,   –147
+  5136, 30.16,   –151
+  5264, 30.34,   –156
+  5376, 30.45,   –160
+  5504, 30.27,   –166
+  5632, 30.73,   –173
+  5760, 31.27,   177
+  5904, 31.85,   165
+  6032, 31.45,   150
+  6176, 30.83,   133
+  6320, 29.44,   116
+  6464, 27.85,   103
+  6608, 25.85,   93
+  6768, 23.90,   85
+  6928, 22.68,   79
+  7088, 21.55,   72
+  7408, 19.57,   60
+  7760, 17.79,   43
+  7936, 16.79,   34
+  8320, 13.55,   19
+  8512, 11.91,   14
+  9104, 8.06,    –1
+  9584, 3.88,    –11
+  9984, 0.94,    –16
```

Maybe you're throwing the wrong things at your development problems.

You're looking at a fairly common approach to solving sticky embedded design problems.

Hurling more money and engineers may have worked on smaller-scale projects. But it often falls short of the mark with today's more complex 16- and 32-bit designs.



Mismatched, nonintegrated development tools can throw off a design team's efforts in no time.

At Applied Microsystems, we're helping software and hardware teams develop better embedded systems more efficiently with high-performance, integrated development systems.

With our tools and support, your project's cost is more manageable. Your design team is more productive. And the end product is more of what you envisioned from the beginning.

This may all sound too good to be true, but Applied Microsystems has the solutions and experience to make it real. Witness the fact that we've set up over 15,000 development systems worldwide.

What to look for in a development systems company. And what to look out for.

To learn more, call us for details or free literature at 1-800-343-3659 (in WA, 206-882-2000).

We'd like to throw a few solutions your way.

Applied Microsystems Corporation

Where it all comes together.

In the U.S. and Canada, call 1-800-343-3659 (in Washington, 206-882-2000). Or contact Applied Microsystems Corporation, P.O. Box 97002, Redmond, WA 98073-9702 USA. **For the name of your nearest distributor in Europe, call 44-(0)-296-625462.** Europe Fax 44-296-623460. Or contact Applied Microsystems Corporation, Ltd., AMC House, South Street, Wendover, Aylesbury, Bucks, HP22 6EP, England. **In Japan, call 03-493-0770.** Japan Fax 03-493-7270. Or contact Applied Microsystems Japan, Ltd., Nihon Seimei, Nishi-Gotanda Building, 7-24-5 Nishi-Gotanda, Shinagawa-KU, Tokyo T141, Japan. AMC-42.

CIRCLE 92 FOR U.S. RESPONSE CIRCLE 93 FOR RESPONSE OUTSIDE THE U.S.

Fast friends.

Motorola and Hewlett-Packard.

Once our Fast Statics met up with Hewlett-Packard, the attraction was obvious.

With new 256K BiCMOS devices, Motorola helped unleash the speed to empower HP's hottest workstations: The HP Apollo Series 700.

What made our 64K x 4 and 32K x 8 Fast SRAMs such a design-in favorite at HP? Performance for one thing. Availability for another.

With both 10 and 12ns versions already shipping, these TTL-compatible devices provide the sheer speed required by the world's fastest workstations.

Once again, Motorola has what it takes to enhance system performance. Like preeminent technology. Relentless product support. And a growing family of BiCMOS devices to accelerate your next design.

Want to give our BiCMOS Fast SRAMs a try? Just complete and send in the coupon on the opposite page. We'll introduce your design to powerful new friends. Faster than you thought possible.

If you like what's new, wait 'til you see what's next.

MOTOROLA

SIMULATING AUDIO TRANSDUCERS WITH SPICE

measured on the bench. An electrical input voltage was applied to the earphone terminals at different frequencies. The corresponding acoustic output was measured with a computer-controlled sound-level meter for data acquisition. The resulting data was edited with a text editor into the format required for a PSpice input file. The completed PSpice model for the earphone is shown *(Table 3)*. The table's general format is the same as that described earlier for the microphone. The first part of the model is the electrical model, along with node connections for each component *(Fig. 2b, again)*. The second section of the model is the acoustic-behavioral model, designated EED1913. As with the microphone model, electrical-to-acoustic phase data is generally useless for integrated-circuit design, but was retained for use by interested acoustical designers.

A printout of a PSpice analysis shows the earphone acoustic simulation *(Fig. 2d)*. The graph shows the typical frequency response that's often encountered when using this type of subminiature earphone. The peak near 3 kHz is related to the resonant peaks in the impedance curve *(Fig. 2a, again)*. A comparison to the manufacturer's data for this type of earphone showed the results to be accurate.

System Simulation

Finally, to achieve a useful result, these models were connected to the model of an audio-amplifier IC design and the overall acoustic-transfer function was simulated. The results of the simulation are shown *(Fig. 3a)*. The graph shows a large, undesirable resonant peak in the frequency response, which is caused by interactions between the circuit, the earphone impedance and acoustic resonances, and the microphone's acoustic-transfer characteristics. The simulation results compared very well with the measurements that can be obtained from a hard-wired breadboard circuit.

Having obtained this basic frequency-response curve, the electronic circuit was manipulated in simulation in an effort to reduce the effects of the undesired resonances and to smooth out the curve. The final simulated system results obtained with a modified circuit design are displayed *(Fig. 3b)*. It was then possible to build a breadboard from the simulation schematic with a reasonable assurance that the system would perform as desired.

The results from these examples show that PSpice analog behavioral modeling can be a useful tool for the simulation of audio transducers. The same general simulation technique described here can also be used to develop models for other electro-acoustic transducers, such as earphones, electro-magnetic loudspeakers, tape-recorder heads, phonograph pickups, all types of microphones, and piezoelectric tweeters. It provides useful electronic-amplifier-load and system acoustic simulation for all audio-circuit designs.□

References:

[1] *PSpice Operating Manual, Version 4.04.* Irvine, Calif.: Microsim Corp., 1990, Chapter 11.

[2]Nagel, L. W. *Spice2: A Computer Program to Simulate Semiconductor Circuits (Memo No. M520).* University of California, Berkeley, 1975.

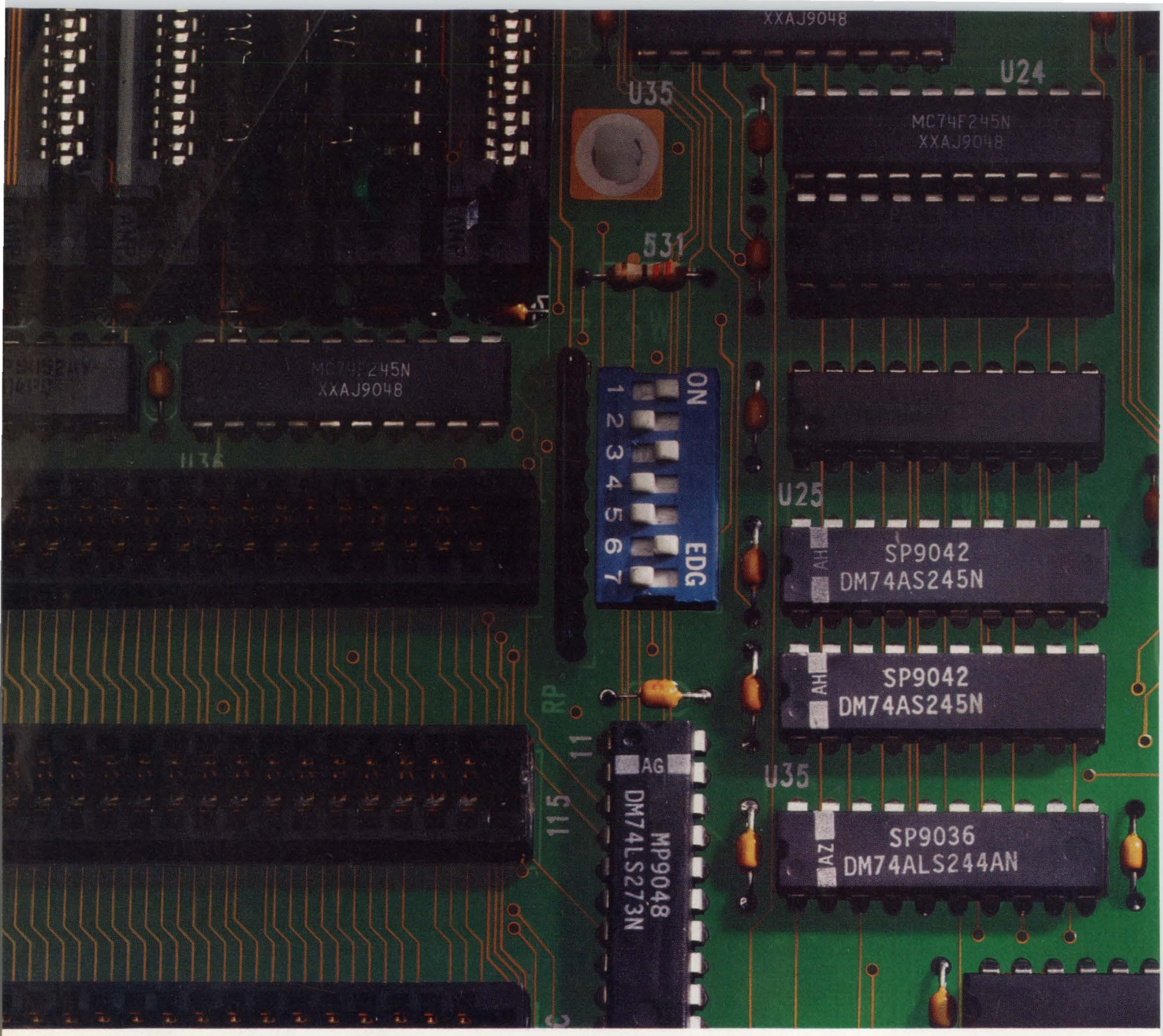
[3]Banzhaf, W. *Computer-Aided Circuit Analysis Using Spice.* Englewood Cliffs, N.J.: Prentice-Hall, 1989.

[4]Tuinenga, P.W. *Spice: A Guide to Circuit Simulation and Analysis Using PSpice.* Englewood Cliffs, N.J.: Prentice-Hall, 1988.

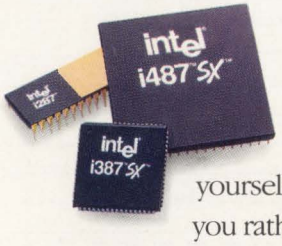
[5]Balabanian, N. *Network Synthesis.* Englewood Cliffs, N.J.: Prentice-all, 1958.

Jeremy Agnew, director of product development for Starkey Laboratories Inc., holds undergraduate degrees in physics and electrical engineering and an MS and PhD in engineering from California Coast University, Los Angeles.

How Valuable?	Circle
Highly	535
Moderately	536
Slightly	537

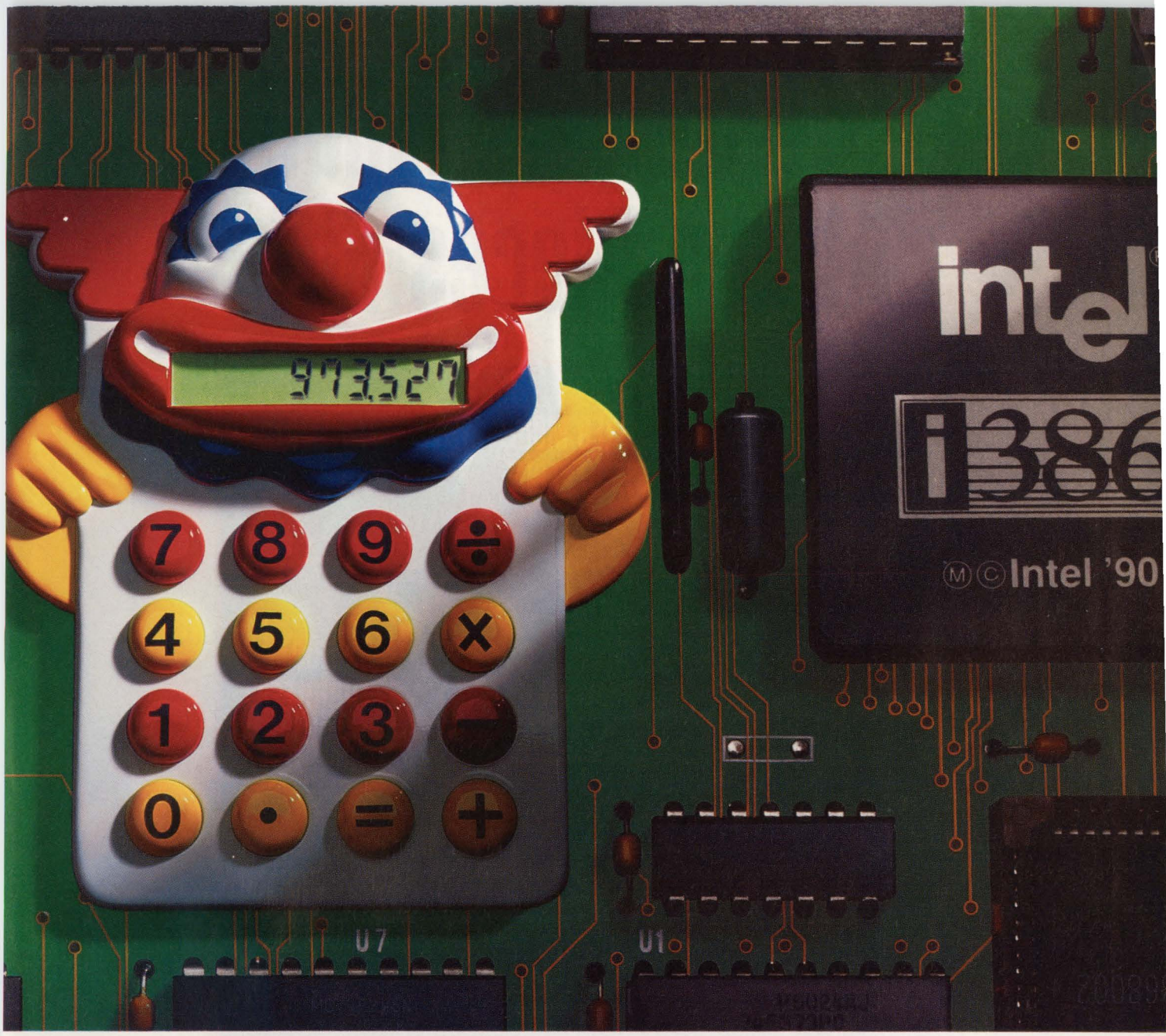


Ask for genuine Intel or who knows what yo



If you need a math coprocessor to speed your power applications, ask yourself this question: Which would you rather have sitting next to your Intel microprocessor — an Intel Math CoProcessor or something you may know nothing about? Because if you don't specify Intel, that's basically what you're getting — a big question mark. With Intel, however, there's simply no question. You're getting quality.

That's because Intel has the longest track record with math coprocessors. In fact, we've manufactured



Math CoProcessors, u'll have to count on.

and sold millions more than all the others combined. And we've tested every one of them with the most exhaustive battery of tests in the industry. All to assure you absolute reliability.

So ask for Intel Math CoProcessors. Or there's no calculating what you'll end up with.

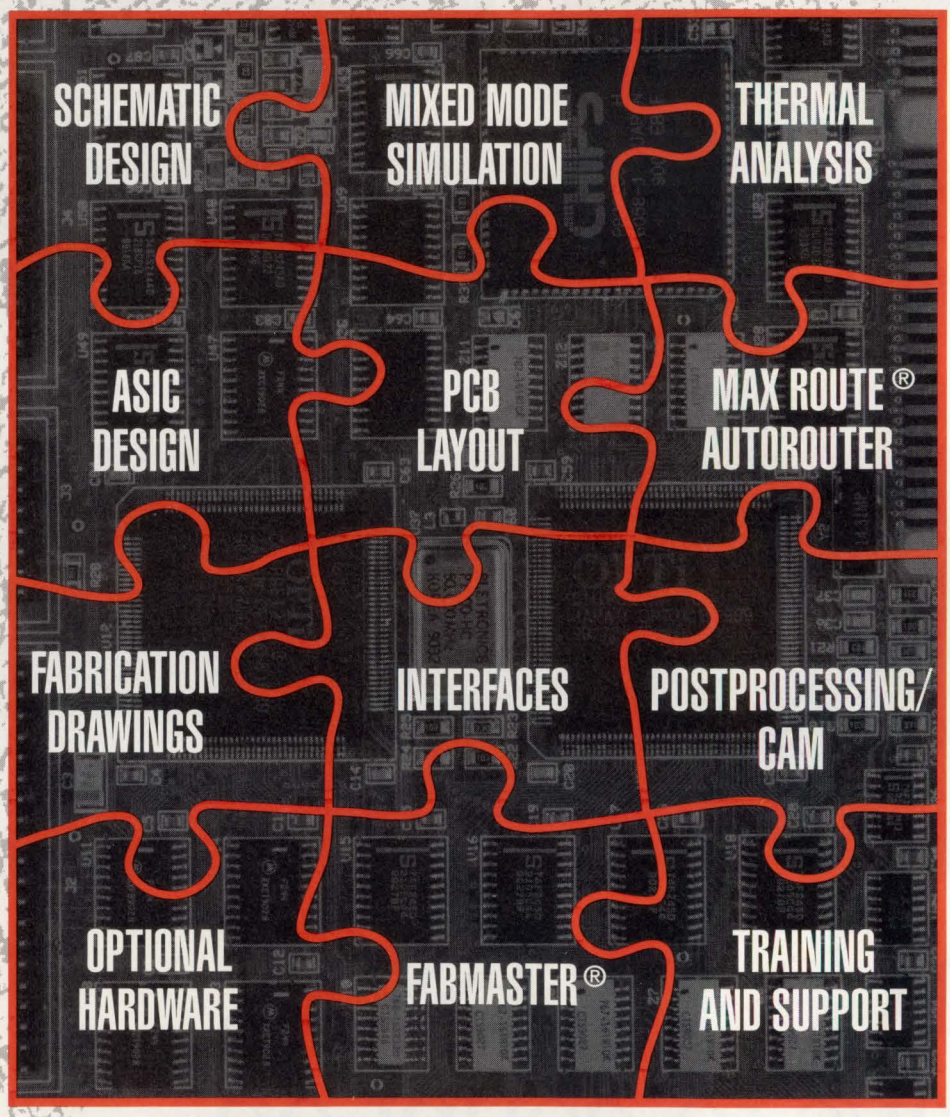
For a free information packet, including our new low prices, call **(800)538-3373.**

intel®

The Computer Inside.™

CIRCLE 1

EE DESIGNER: Finally, All the Pieces Fit!



For more information, or to place an order, call: 1-800-553-1177

DISCOVER VISA MasterCard AMERICAN EXPRESS

SEE US AT WESCON BOOTH # 1332/34

TEAM VISIONICS

2953 Bunker Hill Lane, Suite 201, Santa Clara, CA 95054, Fax: (408) 492-1380

CIRCLE 224 FOR U.S. RESPONSE **CIRCLE 225 FOR RESPONSE OUTSIDE THE U.S.**

BUILDING A CASE FOR OBJECT-ORIENTED TECHNOLOGY

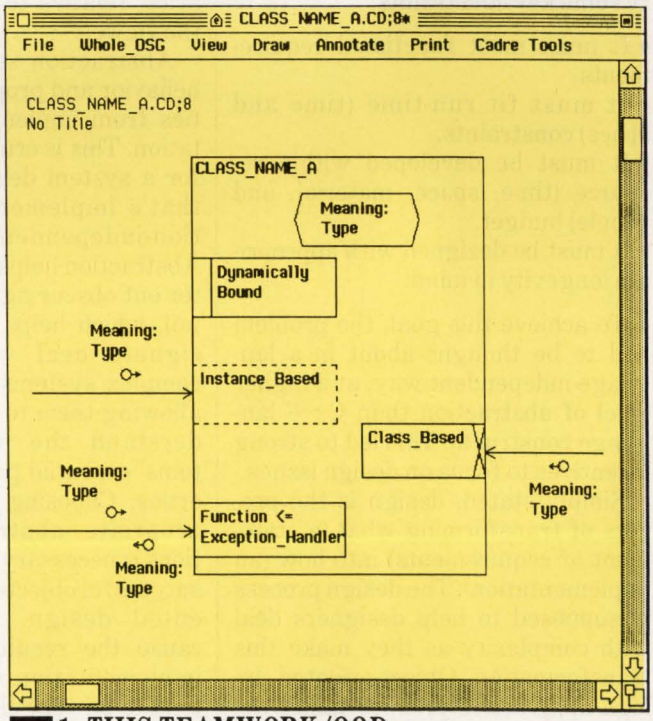
EXPERIENCE SHOWS THAT OBJECT PARADIGMS TOUCH MANY ASPECTS OF CODE DEVELOPMENT IN SURPRISING WAYS.

Object-oriented technology has evolved into one the most talked about topics in the electronics field these days. There are many claims that it will make development problems easier. In fact, object paradigms touch many aspects of development, often in surprising and not so obvious ways.

Many people hear the term object-oriented and immediately think of a programming language like Smalltalk, C++, or Eiffel. These languages all provide language-level abstractions to create and manage hierarchies of communicating objects that serve as the implementation of user requirements. Some very powerful programming environments have been developed that support these languages by providing special-purpose editors, browsers, and debuggers. These programming environments are good because they make it easy to deal with complex collections of code. They're bad because they tend to focus on implementation or language issues at the expense of higher-level design or requirements issues.

Cadre started using C++ in 1986, when the language and tools were fairly primitive. The company spent much time learning the language, which was not an easy task, and just getting basic things to work. Consequently, it took awhile to realize that object-oriented development means more than using an object-oriented language.

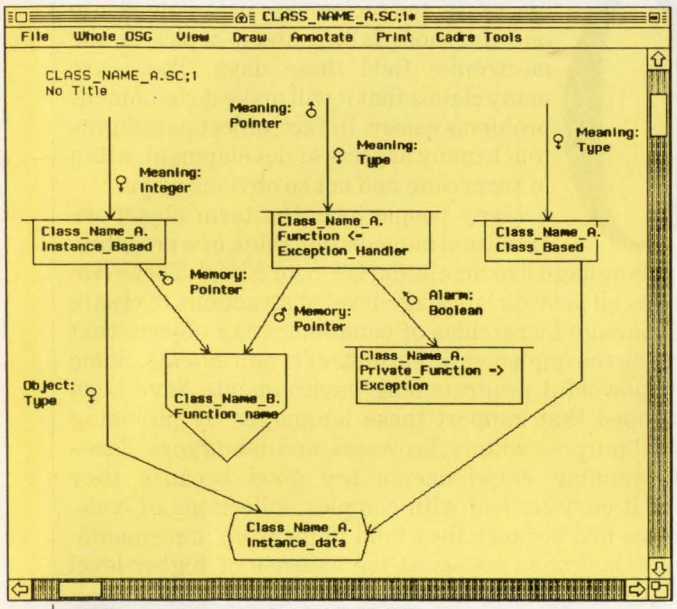
After a few false starts that resulted in unwieldy class hierarchies and sluggish code, the decision was made to step back from the coding problem and ask what was



1. THIS TEAMWORK/OOD class diagram defines a class, its logical data structure, public operations (methods), and parameters (messages). In addition, any deferring operations or exceptions are also noted.

READ FLEMING AND LOU MAZZUCCHELLI
Cadre Technologies Inc., 222 Richmond St., Providence, RI 02903; (401) 351-5950.

OBJECT-ORIENTED TECHNOLOGY



2. A CLASS STRUCTURE chart shows code structure for a class and the flow of data and control within the class. Modules, foreign modules, invocations, and instance data are all easily depicted.

really wanted from a problem-solution standpoint. Regardless of whether or not object-oriented technology is used, a solution must satisfy some key constraints:

- It must meet functional requirements.
- It must fit run-time (time and space) constraints.
- It must be developed within resource (time, space, material, and people) budget.
- It must be designed with appropriate longevity in mind.

To achieve this goal, the problem had to be thought about in a language-independent way, at a higher level of abstraction than C++ language constructs. This led to strong incentives to focus on design issues.

Simply stated, design is the process of transforming what (a statement of requirements) into how (an implementation). The design process is supposed to help designers deal with complexity as they make this transformation. Object-oriented design approaches promise faster development, more reuse, and smaller and more maintainable implementations. If these promises are be realized, it's because good design sense is applied, not because object-oriented dust is sprinkled on the problem to make it disappear.

In *Object Oriented Design with Applications*[1], its author lists seven concepts that describe a reasonable object-oriented design space:

1. Abstraction
2. Encapsulation
3. Modularity
4. Hierarchy
5. Typing
6. Concurrency
7. Persistence

Let's examine each of these in a bit more detail.

1. Abstraction: "An abstraction denotes the essential characteristics of an object that distinguish it from all other kinds of objects and thus provide crisply defined conceptual boundaries, relative to the perspective of the viewer."[1]

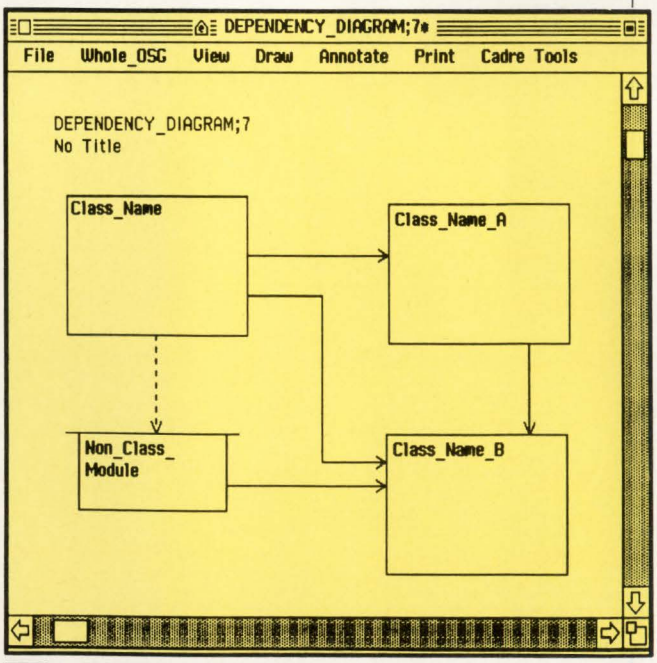
Abstraction separates essential behavior and properties from implementation. This is crucial for a system design that's implementation-independent. Abstraction helps filter out obscuring detail, which helps designers deal with complex systems by allowing them to understand the systems' essential properties. Choosing appropriate abstractions is necessary for successful object-oriented design, because the resulting implementation will tend to be very close to the higher-level abstractions.

There are many kinds of abstractions. Unfortunately, no standards exist for most of them. Here are three of the most important general-purpose abstractions for software designers:

- Entity: Models a problem-domain entity. Examples are flap actuator, student, and mathematical set.
- Action: A generalized set of operations, applied to more than one kind of object. A common example in computer systems is *print*.
- Virtual Machine: A set of operations used by a level of control. Examples include communication protocol layers (each is a virtual machine) and microcode implementations of computer instruction sets (layers of interpreters).

2. Encapsulation: "Encapsulation is the process of hiding all of the details of an object that do not contribute to its essential characteristics."[1]

Encapsulation is sometimes known as information hiding. This is a complementary notion to abstraction, but can be thought of as slightly lower level because non-essential object details are typically side-effects of a particular design or implementation strategy. Encapsulation is desirable because it limits dependencies,



3. USERS CAN SEE all of the data-dependency relationships with a class-dependency diagram.

OBJECT-ORIENTED TECHNOLOGY

and therefore can help minimize the impact of change. Some programming languages (Ada, Modula 2) support encapsulation by separating interfaces (specifications) from implementations (bodies). These and others also permit "private" data and functions.

3. Modularity: "Modularity is the property of a system that has been decomposed into a set of (strongly) cohesive and loosely coupled modules."[1]

Cohesion and coupling are concepts that were developed as part of structured design in the mid-1970s[2]. The concepts apply equally well today. Cohesion measures of logical connectivity among the elements of a particular module. It answers the question "To what degree do these parts belong together?" Coupling measures the strength of association established by a connection from one module to another. It can also be seen as a measure of dependence, and how amenable a system is to change.

Modularity is typically concerned with physical partitioning and packaging. One of the differences between classical structured design and object-oriented design is that structured design focuses on modularity, rather than object relationships and hierarchies.

4. Hierarchy: "Hierarchy is the ranking or ordering of abstractions."[1] Two kinds of hierarchy are identified as important in software systems:

- Aggregation: "is a part of"
- Inheritance: "is a kind of"

Languages like C++ and Eiffel support aggregation and inheritance, and consequently are considered true object-oriented languages. Ada supports aggregation, but not inheritance, leading object-oriented purists to call it an object-based language. Still, it's possible to build object-oriented systems with Ada.

5. Typing: "Typing is the enforcement of the class of an object, such that objects of different types may not be interchanged, or at the most, they may be interchanged only in very restricted ways."[1]

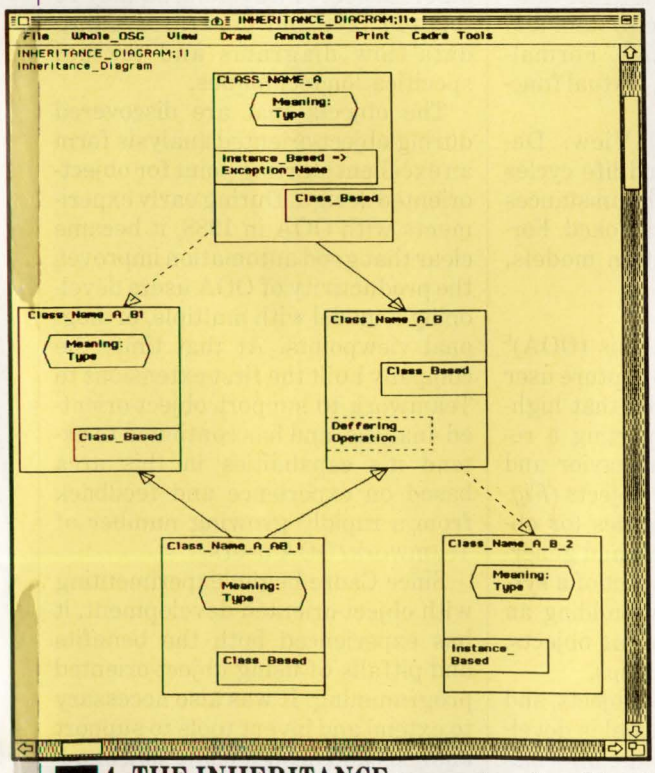
Strongly typed languages (like Ada and Pascal) enforce type consistency at compile time. Other languages may defer type checking to bind or run time, or ignore it completely. In general, strong typing is desirable because it allows errors to be found sooner in the development process, and can aid system verification and validation. Loosely typed languages can offer some advantages during early development and prototyping, but can give developers a false sense of security about a systems' completeness or reliability.

6. Concurrency: "Concurrency is the property that distinguishes an active object [which has its own thread of control] from an inactive one (which does not)."[1]

Concurrency focuses on process abstraction and synchronization. It helps deal with the parallelism that may be inherent in a problem. Some programming languages facilitate implementations of concurrent processes with tasks and a task-communication protocol. If these don't exist in an implementation language, they must be explicitly accounted for in the system design.

7. Persistence: "Persistence is the property of an object through which its existence transcends time (i.e., the object continues to exist after its creator ceases to exist), and/or space (i.e., the objects' location moves from the space in which it was created)."[1]

Database or object-management systems are ways to support the abstraction of objects that persist between program executions, although simpler mechanisms often suffice (for example, a simple file for error logging). Some programming languages directly support persistence with dynamic storage allocation and I/O, where others (notably C) depend on a standard library of functions to provide these services.



4. THE INHERITANCE diagram shows the public and private inheritance relationships, called the class hierarchy, between the classes of a program, library, or environment.

MODELING DESIGN

Cadre desired a design model that accommodated these ideas, so that it could visualize the essential structure of a system with references to object-oriented design concepts. In addition, the design model had to map easily to a target implementation language. This was accomplished for Ada and C++ using an approach originally proposed by R.J.A. Buhr[3], and later extended by Cadre and Project Technology[4] to handle additional concepts and programming languages.

The notation used is called the Object-Oriented Design Language (OODLE). Different types of diagrams depict four significant aspects of a design:

- A Class Diagram shows the external view of a single class. It's intended to illustrate the details of the interface that the class presents to cli-

ents. There's one class diagram per class *(Fig. 1)*.

- A Class Structure Chart shows the internal structure of the code. The notation is based on traditional structure charts[2], extended with additional object-oriented constructs *(Fig. 2)*.
- A Dependency Diagram shows the invocation and friend relationships between classes *(Fig. 3)*.
- An Inheritance Diagram shows the inheritance relationships between classes *(Fig. 4)*.

Some notations proposed for object-oriented design attempt to show all of the information in a single view[5], on one kind of diagram. This approach leads to a complex symbology, which is necessary to uniquely represent each concept, and unwieldy diagrams, even for small problems. The notation must be organized and partitioned to reflect the differing viewpoints and separation of concerns that arise in doing real-world software design. Consequently, OODLE uses the four views listed above. Each of the four diagrams has a clear purpose and a straightforward symbology.

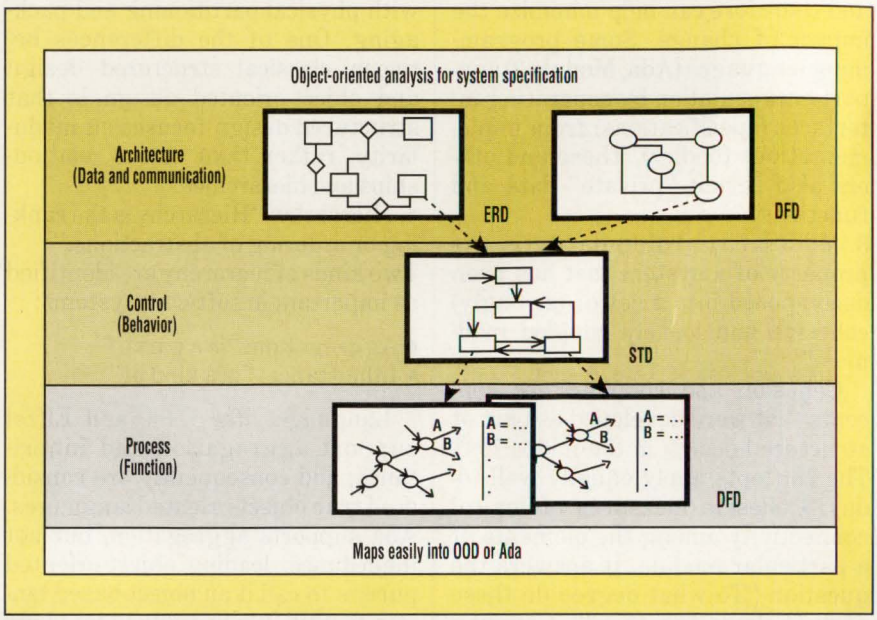
An integrated set of tools (Teamwork/OOD) helps create and manage all of the OODLE diagram types, and provides navigation between views with simple point-and-click operations. Design-rule checkers can ensure consistency, and other tools generate C++ source code from an OODLE design model.

THE REAL WORLD

While a comprehensive design method supported by powerful CASE tools can help ensure a good implementation, the problem still must be understood before designing a solution. An analysis model represents what the designer knows about the problem.

An analysis model comprises these three essential views of any system:

- Data/Object/Entity View: Describes what data/objects/entities are in the system. Formalism: Information (entity-relationship-attribute) model.



5. A SCHEMATIC VIEW of object-oriented analysis shows three levels. The architectural-level view is composed of entity-relationship diagrams (ERDs) that show objects (entities) and the data relationships between them. Message relationships between objects are shown with a data-flow diagram (DFD). In addition, the control-level view uses a state-transition diagram (STD) to show an object's behavior over time. Finally, a process-level view uses data-flow diagrams to model active functions.

- Function View: Describes the functions performed by the system and their data dependencies. Formalisms: data-flow models, textual functional specifications.
- Behavioral/Control View: Describes the behavior and life cycles of the entities and the circumstances in which functions are invoked. Formalisms: state transition models, state charts.

Object-oriented analysis (OOA)[6] has evolved as a way to capture user requirements in a model that highlights the objects supporting a requirement, and their behavior and relationship with other objects *(Fig. 5)*. It assumes that entities (or objects) are the most stable and generally well-understood aspect of a system, so OOA starts by building an information model, showing objects, attributes, and relationships.

Behavior is mapped to objects, and an appropriate state model is developed for each object in the information model (sometimes this is called an *entity-life-history* model). Functions are assumed to be the most unstable aspect of a system, so they're treated last and described using data-flow diagrams and textual specification techniques.

The objects that are discovered during object-oriented analysis form an excellent starting point for object-oriented design. During early experiments with OOA in 1988, it became clear that good automation improves the productivity of OOA users developing a model with multiple, orthogonal viewpoints. At that time, the company built the first extensions to Teamwork to support object-oriented analysis, and has continued to extend it's capabilities in this area based on experience and feedback from a rapidly growing number of Teamwork/OOA users.

Since Cadre began experimenting with object-oriented development, it has experienced both the benefits and pitfalls of using object-oriented programming. It was also necessary to extend and invent tools to support analysis and design using object approaches. This work has resulted in about 250,000 lines of C++ code, which is now shipping in Cadre prod-

DESIGN APPLICATIONS

OBJECT-ORIENTED TECHNOLOGY

ucts. Based on this experience, there's a continuing effort to develop and use object technologies and tools, and Cadre considers them an important part of the product-development effort.□

References:

[1]Booch, Grady, *Object Oriented Design with Applications*, Benjamin/Cummings, 1991.

[2]Page-Jones, Meilir, *The Practical Guide to Structured Systems Design, 2nd Edition*, Englewood Cliffs, N.J.: Yourdon Press/Prentice-Hall, 1988.

[3]Buhr, R. J. A., *System Design with Ada*, Englewood Cliffs, NJ: Prentice-Hall, 1984.

[4]Hecht, Alan; Hywari, Wayne; Mellor, Stephen J.; and Shlaer, Sally, *Teamwork Support for OODLE: A Language Independent Notation for Object-Oriented Design*, Cadre Technologies, 1991.

[5]Muller, Robert J.; Pircher, Peter A.; and Wasserman, Anthony J., *The Object-Oriented Structured Design Notation for Software Design Representation, Computer*, Vol. 23, No. 3, IEEE Computer Society, March, 1990.

[6]Mellor, Stephen J. and Shlaer, Sally, *"Understanding Object-Oriented Analysis,"* Hewlett-Packard Design Center Magazine, January, 1989.

Additional reading material:

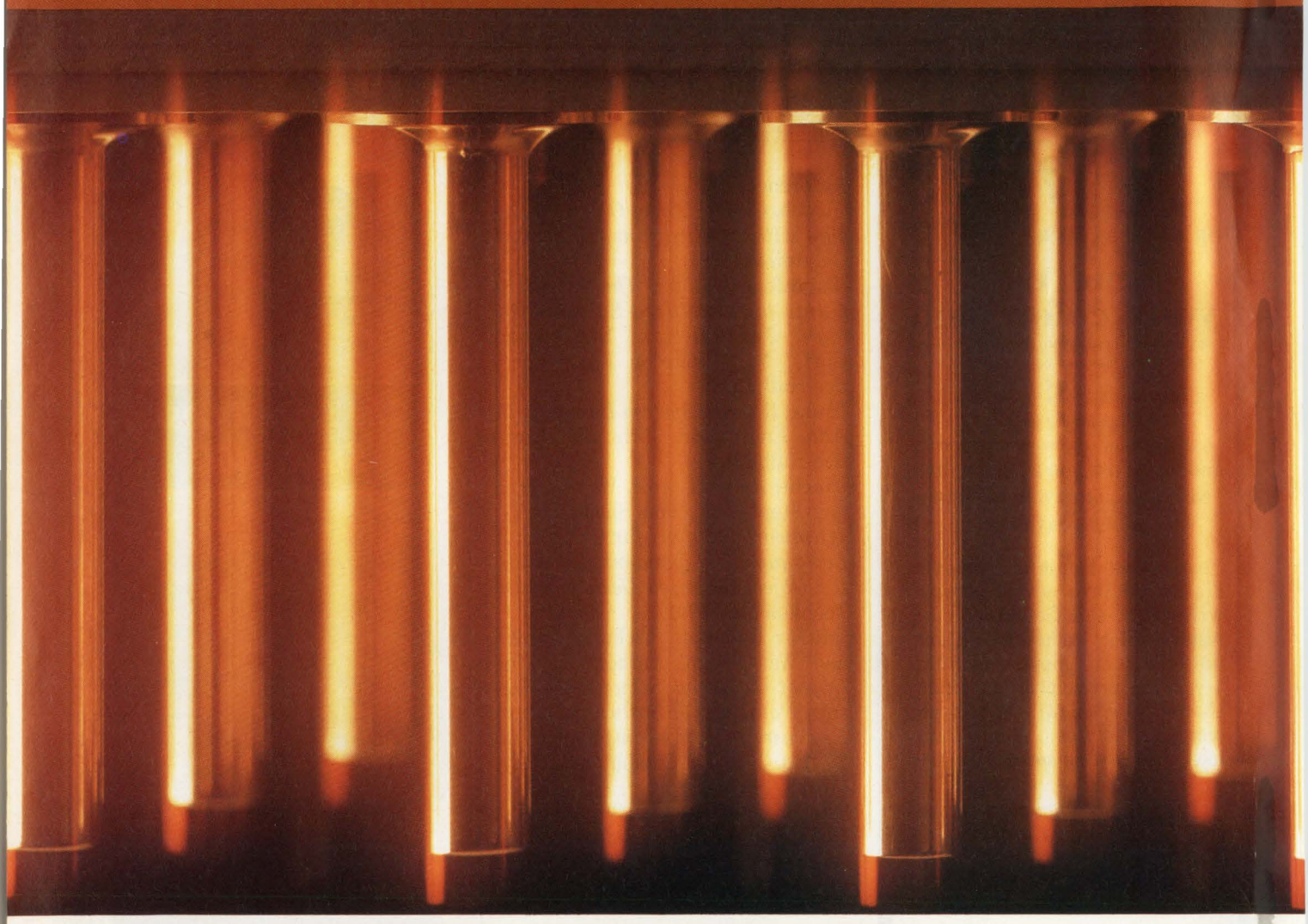
Wybolt, Nicholas, *"Boostrapping Object-Oriented CASE,"* Hotline on Object-Oriented Technology, Vol. 2, No. 3, SIGS Publications, January, 1991.

Read Fleming, vice president, co-founder, and fellow of Cadre, has an ScB from Brown University, Providence, R.I.

Lou Mazzucchelli, vice president, co-founder, and chief technical officer at Cadre, holds an AB in artificial intelligence from Brown University, Providence, R.I.

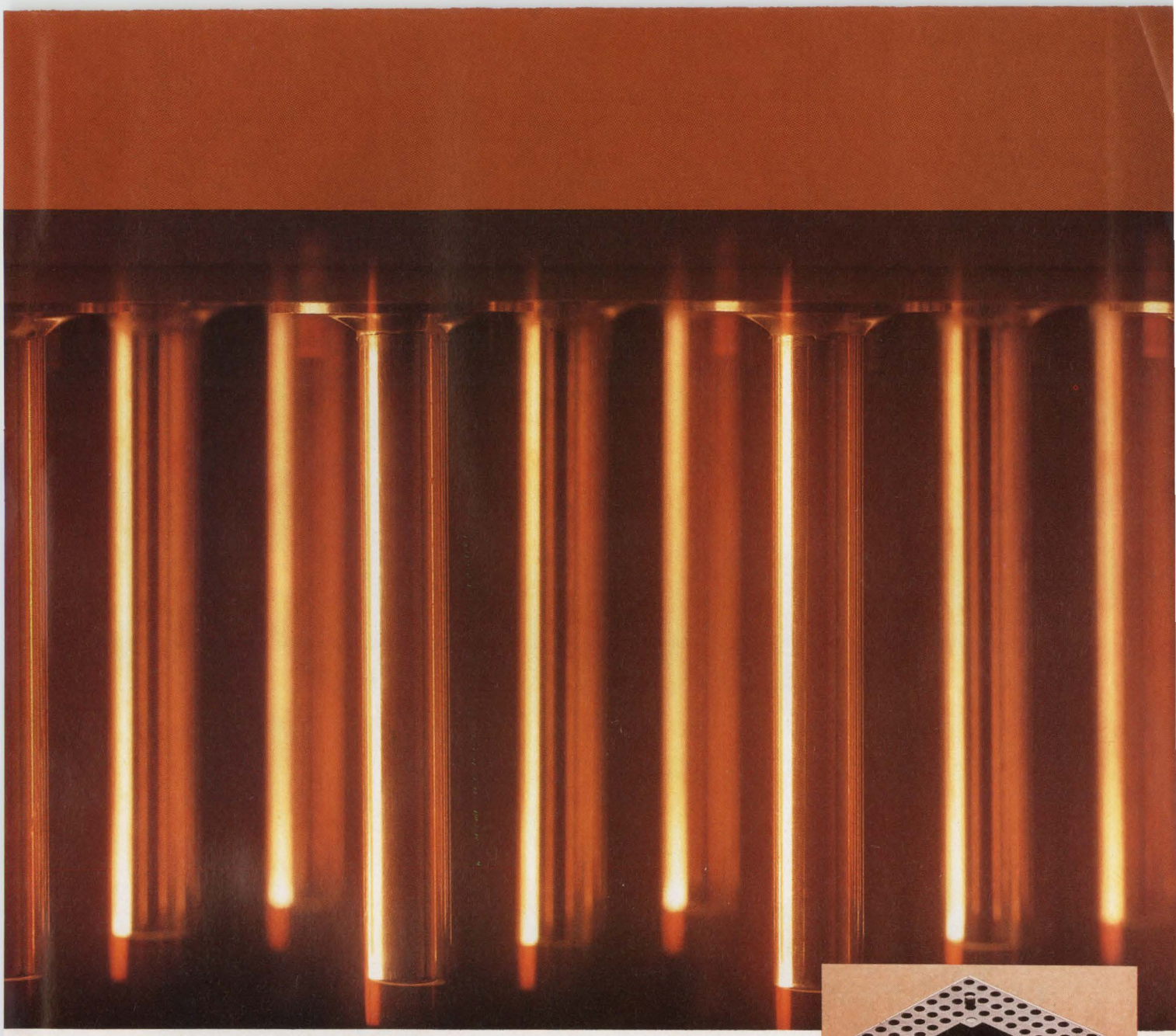
HOW VALUABLE?	CIRCLE
HIGHLY	538
MODERATELY	539
SLIGHTLY	540

Helping production cope with the pressures of high pincount packages.



THIS IS AMP TODAY.

*J. B. Cullinane, "A User's Evaluation of Pin Grid Array Sockets", *Connection Technology*, June 1990.

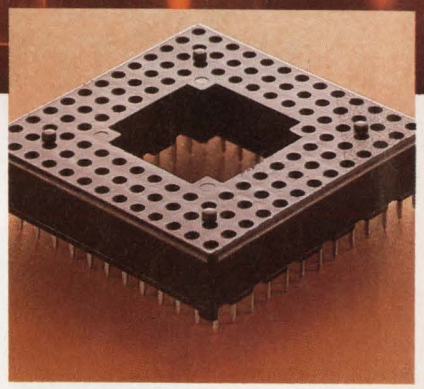


As PGA pincounts go up, so do the insertion/withdrawal forces required to socket them. When counts reach about 121, conventional socket contacts put your total insertion force in the 28 to 50 pound range—hardly conducive to efficient manufacturing.

Not so with AMP LIF PGA sockets. We use a dual-beam contact, and we stagger contact row heights to reduce insertion force requirements dramatically. For the same 121-pin package, our socket design requires an average 13.1 pounds insertion force*, 50-75% lower than conventional sockets. This can make a significant difference in everything from operator fatigue and device stress to board integrity and ease of field service.

And our exclusive design provides excellent normal contact force as well—the contacts utilize a long beam geometry, providing ample deflection with no compromise between normal force and insertion/extraction force.

Sizes: 10x10 to 25x25, with quick turnaround on special patterns. For more information, call the AMP Product Information Center at 1-800-522-6752 (fax 717-561-6110). In Canada call 416-475-6222. AMP Incorporated, Harrisburg, PA 17105-3608.



Dual-beam contact LIF PGA

AMP

CIRCLE 84 FOR U.S. RESPONSE

CIRCLE 85 FOR RESPONSE OUTSIDE THE U.S.

NEW
2900/3900
Programming Series starts at $2995!

The new 3900 takes you wherever technology goes.

At the speed technology is advancing, you need to be ready for anything. On a limited budget.

The NEW 3900 Programming System keeps up with your most advanced designs while keeping device-programming costs down. It offers leading-edge support for FPGAs, PLDs, memory devices, and microcontrollers up to 88 pins, with future device and package capabilities built in. Yet this support is offered in device libraries so you pay for only what you need, when you need it. And you can get into the 2900/3900 Programming Series for as little as $2995.* Move up to 88-pin support and beyond with a simple upgrade.

Find out how the 3900 can make your future affordable.

Call today for more information and we'll also send you a FREE copy of Data I/O®'s all-new, and expanded 1991 Wall Chart of Programmable Devices (a $24.95 value).

To qualify, just call us with the brand name and serial number of any programmer you are currently using.

1-800-3-DataIO
(1-800-332-8246)

*U.S. list price only.

The Personal Silicon Experts

DATA I/O
Corporation

Data I/O Corporation 10525 Willows Road N.E., P.O. Box 97046, Redmond, WA 98073-9746, U.S.A. (206) 881-6444
1-800-3-DataIO (1-800-332-8246)
Data I/O Canada 6725 Airport Road, Suite 302, Mississauga, Ontario L4V 1V2 (416) 678-0761
Data I/O Europe World Trade Center, Strawinskylaan 537, 1077 XX Amsterdam, The Netherlands + 31 (0)20-6622866
Data I/O GmbH Lochhamer Schlag 5A, 8032 Graefelfing, Germany, 089 858580
Data I/O Japan Sumitomoseimei Higashishinbashi Bldg., 8F, 2-1-7, Higashi-Shinbashi, Minato-Ku, Tokyo 105, Japan
033 432 6991/Telex 2522685 DATAIO J
Data I/O Limited 660 Eskdale Road, Winnersh, Wokingham, Berkshire, United Kingdom RG11 5TS, 0734 440011

PLD/FPGA DESIGN TOOLS

A SPECIAL EDITORIAL FEATURE

Avoid pitfalls in selecting the right programmable-logic design tools

Confusing terminology can mislead designers unless they know what they need and how to find it.

BY BILL SCHULZE

MINC Inc., 6755 Earl Dr., Colorado Springs, CO 80918; (719) 590-1155.

Over the last few years, programmable-logic use in system design has grown by leaps and bounds. Users have realized the benefits of reduced time-to-market and increased flexibility, and have taken the technology from acceptance by early adopters to a mainstream design practice today. The growth in using both CMOS and complex programmable-logic-device (PLD) architectures over the next few years far outpaces the overall growth in the logic market, and indicates the continued popularity of these devices for logic system design *(Fig. 1)*.

The appearance of more powerful design tools to support these complex architectures continues to be instrumental to the growth in acceptance of programmable-logic technology. However, designers using or considering the use of programmable logic for an upcoming design project are now faced with selecting the most appropriate device architecture and choosing the most appropriate design tool from a field of competitors often touting similar and confusing features. As a result, the very same software that drives the continued growth in the use of programmable logic also becomes a limiting factor for many designers.

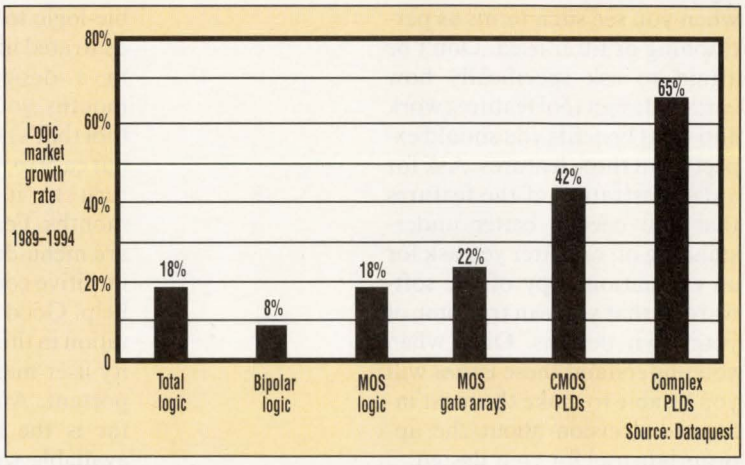
This article will provide designers with some insight into the key issues and concerns surrounding the selection and application of design tools for the programmable logic design task.

TERMINOLOGY: CAVEAT EMPTOR!

When you're evaluating programmable-logic design software, beware of the differences in terminology used by vendors. Similar or sometimes identical terms are often used to describe product features that are very different in the way they operate and the value they deliver. The same terms are sometimes even used to mean different things, depending on the architecture under consideration.

One such example is the term "partitioning." Many programmable-logic-design-tool vendors today advertise that their product provides or allows partitioning of a design across multiple PLD devices. At first glance, prospective users would be lead to believe that everyone supports partitioning. However, closely examining this claim shows that the actual capabilities each vendor offers in this area are quite different. In some cases, these capabilities consist of simple utilities or documentation to aid the designer in manually splitting up the design into multiple devices. In other instances, the software provides fully automatic partitioning of the logic across multiple devices and architectures. The real issue is the effort required by designers to realize an efficient design implementation using these capabilities. As the different approaches suggest, this can range from a great deal of manual effort to no additional effort at all.

We're now beginning to see partitioning used in reference to the capabilities of field-programmable-gate-array (FPGA)

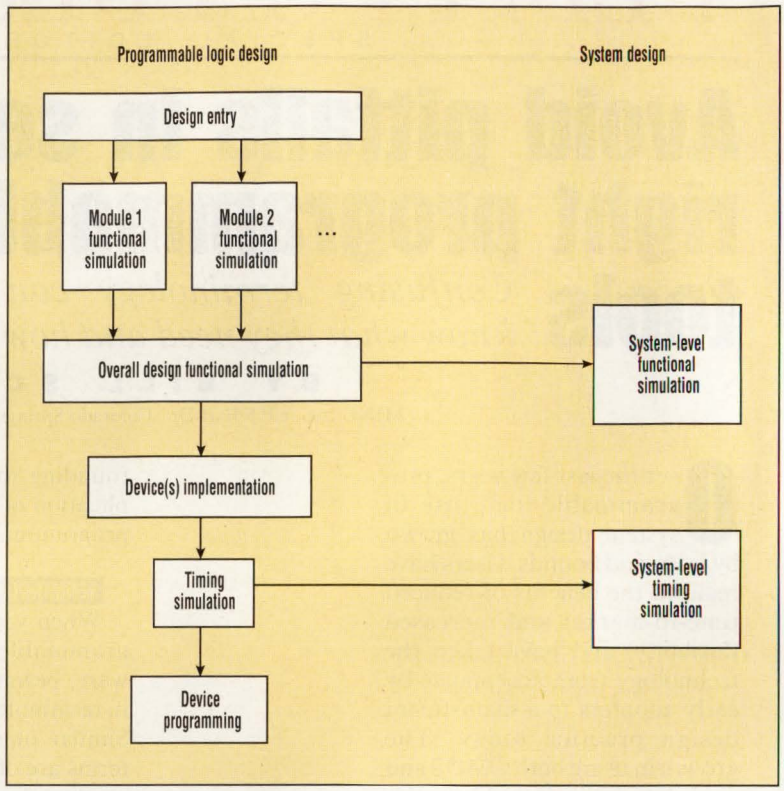


1. The trends in the logic market's growth rate show that users will continue to have strong acceptance of programmable logic. With heavy growth evidenced in CMOS and complex PLDs, it's obvious that programmable logic is now a mainstream design practice.

design tools also, but this typically refers to a different type of partitioning. The internal architecture of many of today's FPGAs consists of a number of programmable logic blocks that are connected by programmable routing resources. A design to be implemented in such a device must therefore be partitioned among these logic blocks in a way that produces an efficient implementation of the required functions. Hence, another meaning for the same term.

Another example of confusing terminology is the term "fitter." Most programmable-logic-design-tool vendors today use this word to describe their software's ability to implement logic in a specific architecture. But when the term fitter is used, it must be known what specific functions the vendor is referring to. Many users expect a fitter's output to be a programming file for the selected device (such as a JEDEC file for a PLD), but this may not be the case for all architecture types, particularly more complex FPGA architectures. As the term is used today, some fitters don't produce programming information but only provide the manipulation of the logic into an appropriate form for the architecture. Programming information is then generated by another tool or set of tools.

The point here for users is that you know exactly what the design tool vendor is referring to when you see such terms as partitioning or fitter used. Don't be afraid to ask specifically how certain design tool features work and what benefits you should expect from these features. Ask for a demonstration of the features that you need a better understanding of; or better yet, ask for an evaluation copy of the software so that you can try some of your own designs. Only when you understand these issues will you be able to make the most informed decision about the appropriate tool for your design.



2. The simulation methodology for your programmable-logic designs should match your overall development approach. This may call for simulation at several stages of the design process.

USER REQUIREMENTS

A recent industry survey asked programmable-logic users what the most important features were when considering the purchase of a design tool. Let's take a brief look at each of these features, in the order of their importance as ranked by the users surveyed.

EASE OF USE

The most mentioned feature was the tool's ease of use. Because the use of a programmable-logic tool will likely be concentrated into a few weeks within a design cycle of several months, you'll want to look for a tool that's not only easy to learn, but easy to re-learn when you return to it after a couple of months. Features that help here are menu-driven interfaces with intuitive commands and on-line help. Good reference documentation in the form of a high-quality user manual can also be important. Another thing to look for is the level of automation available with the tool. For instance, the more of the task that can be effectively automated, the easier the tool tends to be on users, because less detailed knowledge is required.

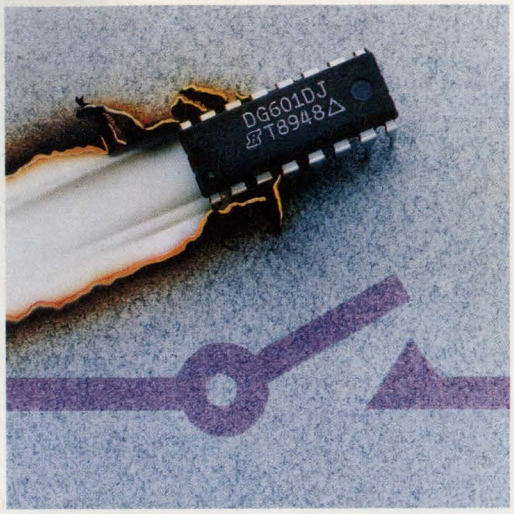
SIMULATION SUPPORT

Simulation is becoming increasingly important as design complexity grows and circuit speeds climb. The ability to accurately simulate the design under development can save considerable time and effort in debugging versus having to isolate these problems much later in the design process, where it's more difficult and expensive to make changes. You should look for the ability of the tool to simulate the design consistent with the way you develop it *(Fig. 2)*.

If you develop your design one function or module at a time, as many do, make sure that you can simulate each individual module. Then assemble the modules into a system and resimulate to verify their interactions. For system designers using simulation, search for the

FUTURE IS UNIQUE

YOUR FAST SOURCE FOR ANALOG SWITCHES



Looking for the perfect analog switch or multiplexer? With Future's broad inventory from Siliconix, we've got exactly what you need. Everything from low-cost, industry-standard analog switches, such as the DG211, to fast fault-protected multiplexers, like the DG458, and specialized high-performance video crosspoint switches, like the DG884.

SPST, DPST, SPDT, duals, quads — all the popular switch configurations are on the shelf and ready for your manufacturing lines.

Take advantage of Siliconix' advanced technologies for your new designs. The DG400 family of silicon-gate CMOS switches offers lower leakages, higher accuracy, and faster operation in functional and pin-for-pin replacements for industry-standard part numbers. The DG400 series provides enchanced electrostatic discharge protection (4000V minimum).

The DG400s are TTL and CMOS compatible. And they're versatile, operating from a variety of voltages, ranging from single +5-V to ±22-V supplies.

KEY FEATURES	SPEC	DEVICES
Lowest On-Resistance	10Ω	DG180, DG183, DG186
Lowest Leakage, $I_{s(off)}$	0.25 nA	DG411, DG412, DG413
Fastest Turn-On Time	45 ns	DG601
Lowest Charge Injection	2 pC	DG441, DG442
Highest Bandwidth	500 MHz	DG540, DG541
Lowest Power Consumption	35 µW	DG401, DG403, DG405
Fastest Fault-Protected Multiplexer	200 ns	DG458
Best Video Crosspoint	300 MHz	DG884
Smallest Physical Size	SO-8	DG417, DG418, DG419

For your high-performance designs, Siliconix' video switches boast bandwidths to 500 MHz. This means your crosstalk and off-isolation performance can be improved by 20 to 30dB. These switches, multiplexers, and crosspoint arrays reduce board space, power dissipation, component count, and costs while simplifying system design and improving reliability.

And you can count on Future Electronics' delivery performance to match the quality and performance of Siliconix' analog switches and multiplexers. Call Future Electronics for your next analog switch order. And profit from immediate, off-the-shelf delivery — and unmatched product expertise.

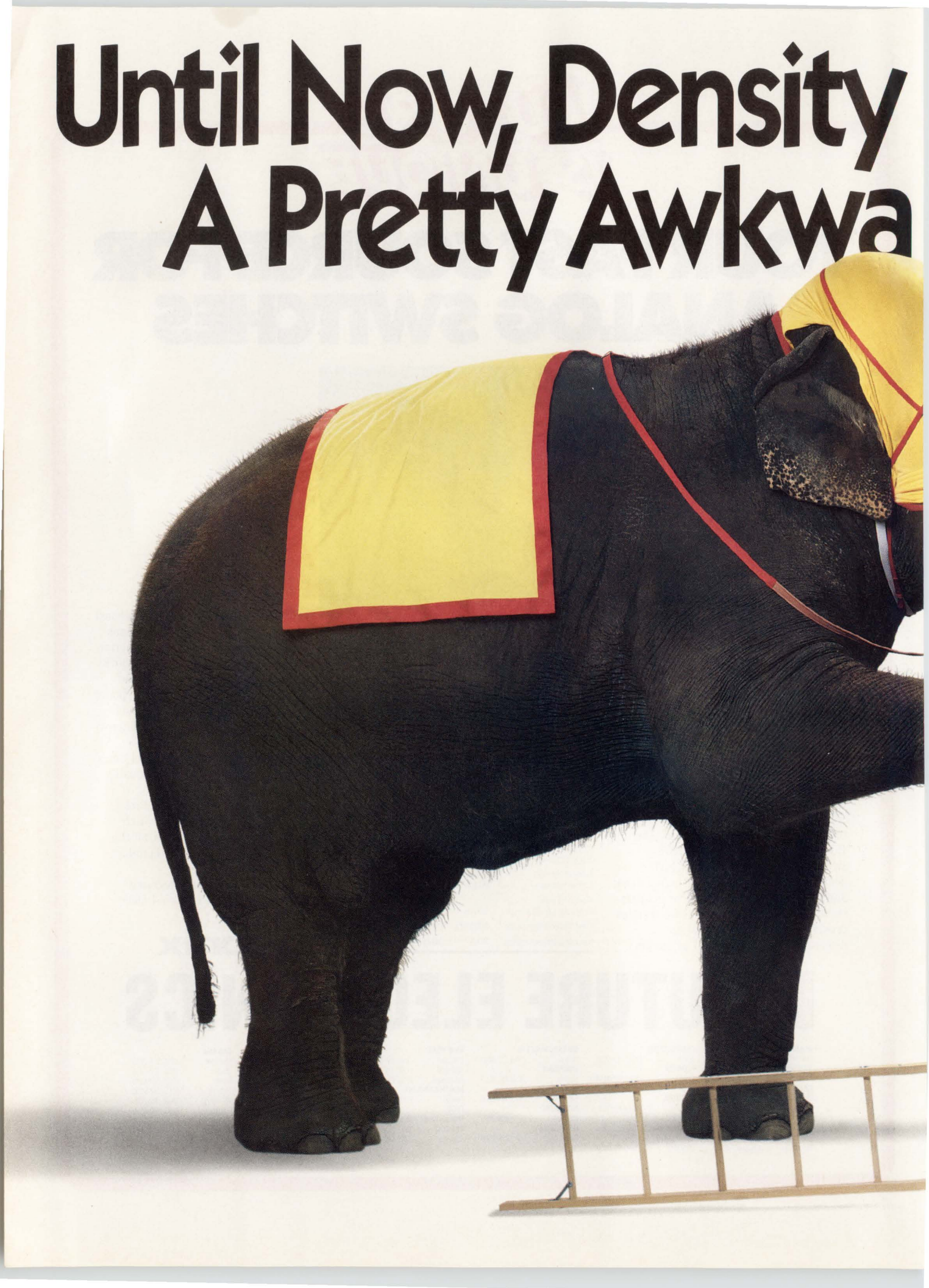
For the latest Siliconix Integrated Circuits Data Book, call 1-800-554-5565, ext. 567.

Siliconix

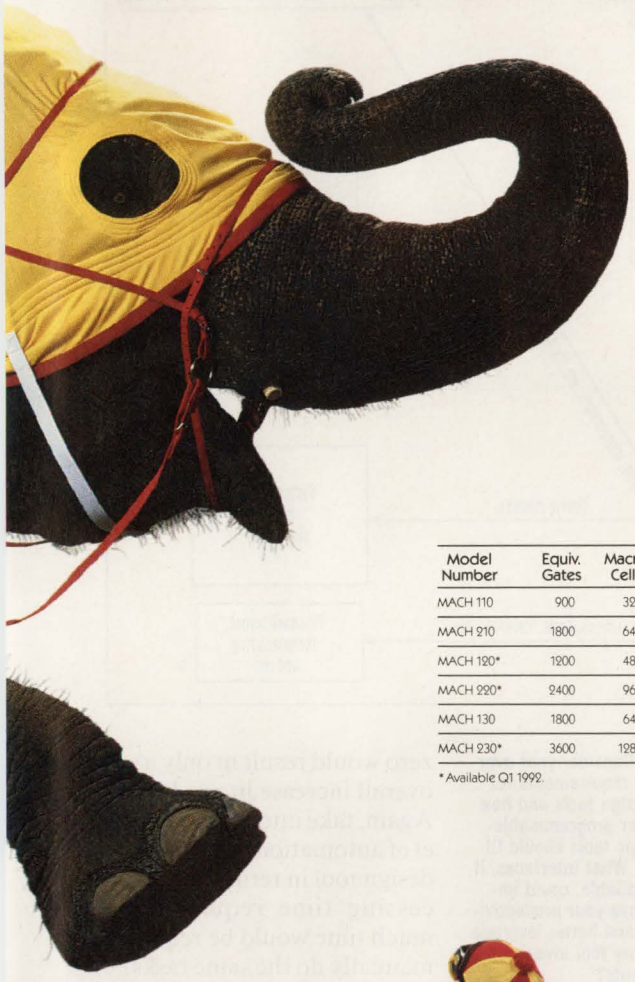
FUTURE ELECTRONICS

ALABAMA
Huntsville (205) 830-2322
ARIZONA
Phoenix (602) 968-7140
CALIFORNIA
San Jose (408) 434-1122
Chatsworth (818) 772-6240
Irvine (714) 250-4141
San Diego (619) 278-5020
COLORADO
Broomfield (303) 421-0123
CONNECTICUT
Bethel (203) 743-9594
FLORIDA
Orlando (407) 767-8414
Largo (813) 530-1222
GEORGIA
Norcross (404)441-7676
ILLINOIS
Hoffman Estates (708) 882-1255
MARYLAND
Columbia (301) 290-0600
MASSACHUSETTS
Bolton (508) 779-3000
MICHIGAN
Livonia (313) 261-5270
MINNESOTA
Eden Praire (612) 944-2200
MISSOURI
St. Louis (314) 469-6805
NEW JERSEY
Parsippany (201) 299-0400
NEW YORK
Liverpool (315) 451-2371
Rochester (716) 272-1120
Hauppauge (516) 234-4000
NORTH CAROLINA
Raleigh (919) 790-7111
OHIO
Mayfield Heights (216) 449-6996
OREGON
Beaverton (503) 645-9454
PENNSYLVANIA
Marlton (609) 778-7600
TEXAS
Houston (713) 556-8696
Richardson (214) 437-2437
UTAH
Salt Lake City (801) 972-8489
WASHINGTON
Redmond (206) 881-8199
WISCONSIN
Waukesha (414) 786-1884
CANADA
Montreal (514) 694-7710
Quebec (418) 877-6666
Ottawa (613) 820-8313
Toronto (416) 612-9200
Winnipeg (204) 786-7711
Calgary (403) 250-5550
Edmondton (403) 438-2858
Vancouver (604) 294-1166

Until Now, Density A Pretty Awkwa



And Speed Were rd Combination.



AMD Presents The MACH™ Family Of High Speed, High Density PLDs.

Nothing can squash an elegant, high density design faster than a slow, unpredictable and expensive PLD. That's why we've developed the MACH PLD family—for both density, and speed.

The MACH family gives you everything you need in a PLD on state-of-the-art CMOS: Densities up to 128 macrocells or 3600 equivalent gates. Clock speeds up to 66.7 MHz. And absolutely predictable, worst-case delays as low as 12ns per 16 product term macrocell.

And they work for peanuts. The MACH family can bring your costs down as low as a penny per gate—up to 40% less than other high density PLDs.

Model Number	Equiv. Gates	Macro Cells	Max. Delay	System Speed	I/O Pins	Hard-Wired Option
MACH 110	900	32	12ns	66.7 MHz	44	MASC 110
MACH 210	1800	64	12ns	66.7 MHz	44	MASC 210
MACH 120*	1200	48	15ns	50 MHz	68	MASC 120
MACH 220*	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230*	3600	128	15ns	50 MHz	84	MASC 230

* Available Q1 1992.

With the MACH family you'll get to market faster, too. Because it's supported by most popular design tools: Including ABEL,™ CUPL,™ LOG/iC,™ MINC, OrCad,® and AMD's own PALASM® software. There's also hardware and software support from over 20 additional FusionPLD partners.

Every MACH part migrates easily to a pin-compatible hard-wired MASC™ counterpart—for high volume orders with no redesign, no NRE, no performance glitches, no problems.

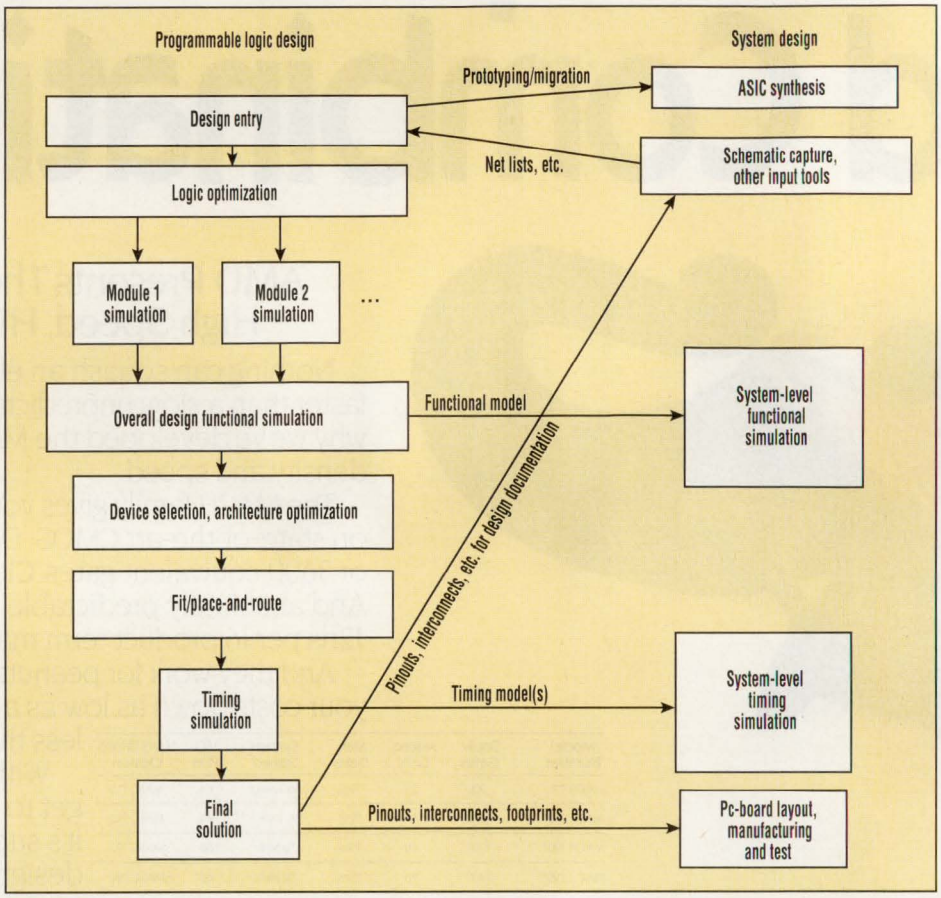
So don't horse around with slow, unpredictable, high density PLDs—start designing with the MACH family from AMD. Call **1-800-222-9323** for more information.

Advanced Micro Devices

CIRCLE 230 FOR U.S. RESPONSE

CIRCLE 231 FOR RESPONSE OUTSIDE THE U.S.

appropriate support of the programmable-logic elements in the context of the system-level simulation tools you're using. For example, does the tool generate the appropriate models to allow functional simulation of the design description at the system level? And after the final device implementation, is timing simulation (including the programmable elements) available to verify the system's overall performance?



PERFORMANCE

There are many aspects to a tool's performance, but the key ones for programmable-logic tools are typically optimization performance, overall speed of generating a solution, and capacity. Good optimization performance centers around the tool's ability to generate device solutions that require the minimal amount of device resources for a given logic function. Logic-reduction algorithms eliminate redundant elements while preserving the required functionality. Typically, not much differentiation exists among tools in this area. However, for the most flexibility, look for a choice of reduction levels and/or algorithms. Also make sure that you have the ability not to reduce particular nodes in your design. Therefore, you can exercise more control if needed.

The second area related to optimization performance is that of optimization for the target architecture. For PLD architectures, this means that the automatic use of DeMorgan's theorem to generate the smallest equations for a given device should be available. In addition, the system should allow you to take advantage of "don't care" conditions to aid in more efficient design implementations.

Another key to this ability is the efficiency of the fitting software to take complete advantage of the architecture. FPGA architectures vary widely and typically require their own unique optimization approaches. The bottom line is that different architectures often require different optimization techniques to maximize their use. If there's some lingering doubt about this issue, try a specific design in your two favorite programmable-logic design systems and compare the final result. You'll easily see any advantages that one has over the other (at least for that particular design).

SPEED

Compilation speed is a much-talked-about issue that's typically very visible. Though it's nice to have fast processing speeds, don't get too bogged down with this issue. Consider the overall amount of time spent on your programmable-logic-design process and what portion is consumed during compilation. For most users, reducing this time to zero would result in only a small overall increase in productivity. Again, take into account the level of automation provided by the design tool in return for the processing time required. How much time would be required to manually do the same tasks?

3. Consider your overall requirements for design tools and how your programmable-logic tools should fit in. What interfaces, if available, could improve your productivity and better leverage other tool investments?

CAPACITY

Capacity is an issue often overlooked by users evaluating design tools for programmable logic, but it's becoming more and more of a concern. Until recently, the typical programmable device was relatively simple, and provided logic densities up to a few hundred equivalent gates. Today, however, we're seeing a strong emphasis from device manufacturers on developing more complex and dense architectures that range up to many thousands of equivalent gates *(Fig. 1, again)*.

This trend is placing serious

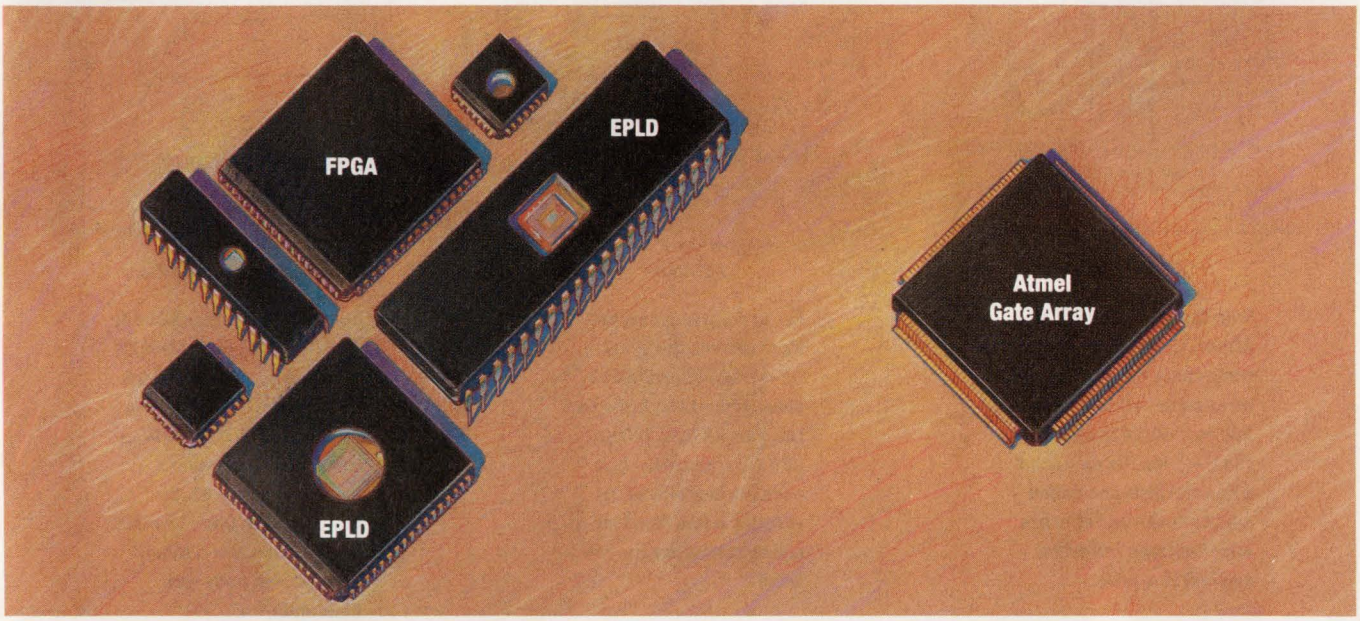
ISN'T IT TIME YOU CONVERTED?

Face it, now that your new system is approved for production, your work is really only half over. Now's the time to convert those FPGAs and EPLDs into low-cost, highly efficient gate arrays.

It's easier than you think, no matter what "they" say.

Atmel will transfer your user-programmable logic to mass-produced gate arrays, painlessly and quickly. We'll match your system timing nanosecond for nanosecond using your design files. We'll cut your production costs substantially. And, we'll make it easy. Need proof?

PROOF



BEFORE		AFTER
$175.00	*Component Cost*	$15.00
8 square inches	*Component Area*	2.5 square inches
90 mA	*Supply Current*	10 mA
40 MHz	*Performance*	40 MHz

How can Atmel manage this? Because we've been designing and manufacturing both user-programmable logic and factory-programmed gate arrays from day one.

Just give us your JEDEC files or netlist and we'll put your logic into the best gate arrays in town. We'll make you a convert.

ATMEL®

The people who make the difference.

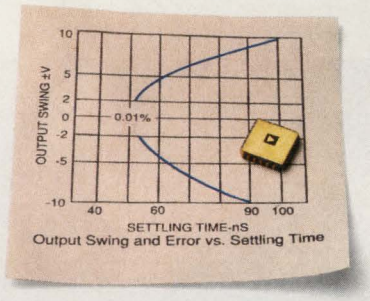
ATMEL CORPORATION
2125 O'Nel Drive
San Jose, CA 95131

Tel. 1-800-292-8635
Tel. (408) 441-0311
FAX (408) 436-4200

CIRCLE 228 FOR U.S. RESPONSE

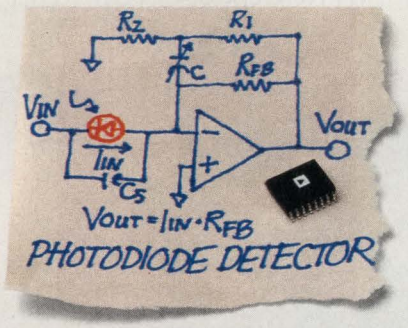
CIRCLE 229 FOR RESPONSE OUTSIDE THE U.S.

Whether you fax it, fire it, send it, measure it, wire it, compute it, The Analog family of



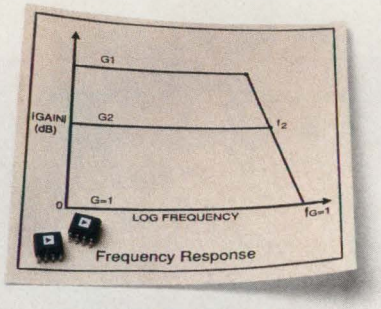
Precision

With the AD840, AD841 and AD842, there's no need to trade speed for accuracy. All three settle to 0.01% within 100 ns (840/842) and 110 ns (841) – critical in data acquisition and instrumentation applications – and offer low offset voltages and drifts, and fast slew rates.



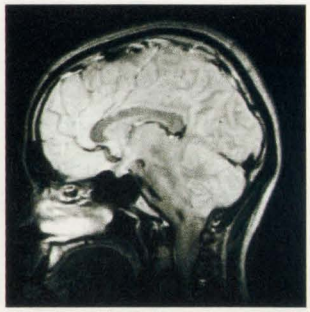
FET Input

For op amps requiring low input current, the OP-42, OP-44, AD845 and AD843 are all remarkably fast – slew rates are 58, 120, 100 and 250 V/μs, respectively. In addition, they offer offset voltages of less than 1 mV and extremely low current noise.



Transimpedance Amplifiers

The OP-160, OP-260, AD844, AD846, AD9617 and AD9618 all utilize a current feedback architecture to achieve slew rates from 450 to 2000 V/μs without compromising stability – even in hostile environments. Other benefits include low power dissipation and high unity-gain bandwidth.

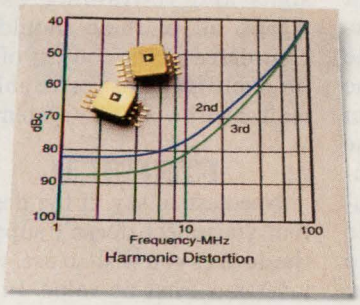


If whatever it is you're trying to do involves high-speed op amps, Analog Devices is the company to call. With our current products and new introductions, we have the broadest line of high-speed op amps available. A line that gives you the right combination of speed, precision, noise and price. So chances are, we've got exactly what you need for

Authorized North American Distributors: *Alliance Electronics* 505-292-3360 • *Allied Electronics* 817-595-3500 • *Anthem Electronics* 408-453-1200 • *BBD Electronics, Inc.* 416-821-7800 • *Bell Industries*

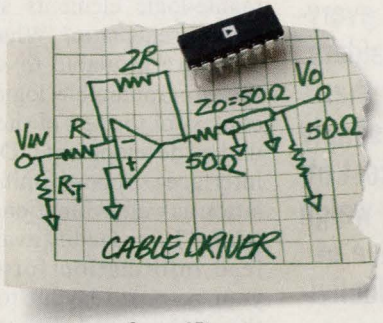
shoot it, launch it, land it, test it, display it or air it, we've got it.

high-speed op amps.



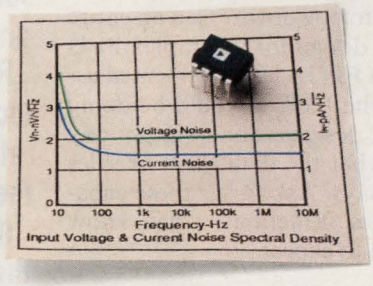
Buffers

If you're looking for extremely low distortion buffers, look at the specs of the AD9620 and AD9630 – distortion at 20 MHz: −73 dBc and −66 dBc, respectively; fast settling time: less than 8ns to 0.02%; and extremely low noise: 2.2 nV/√Hz.



General Purpose

With the right combination of speed, precision, power dissipation and high output drive capability, the AD827, AD829, AD847, AD848, AD849 and OP-64 are ideal general purpose solutions. And they're ideally priced solutions – most singles are under $3, and duals are under $5.



Low Noise

It used to be you had to choose between speed or low noise. But with the AD829, you get both. It features voltage noise of 2 nV/√Hz and current noise of 1.5 pA/√Hz with a 50 MHz unity-gain bandwidth. Those specs, combined with the low price of $2.95/100s, make it ideal for both audio and video applications.

whatever application you're working in. Call us at 1-800-262-5643, or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106, for a complete high-speed op amp selection guide and a *free copy of our SPICE model library.*

ANALOG DEVICES

Analog Devices, One Technology Way, Norwood, MA 02062-9106. Distribution, offices and applications support available worldwide.

213-826-6778 • *Future Electronics* 514-694-7710 • *Hall-Mark Electronics* 214-343-5000 • *Newark Electronics* 312-784-5100 • *Pioneer Standard* 216-587-3600 • *Pioneer Technologies Group* 1-800-227-1693

CIRCLE 220 FOR U.S. RESPONSE CIRCLE 221 FOR RESPONSE OUTSIDE THE U.S.

demands on programmable-logic design tools, though, because many of these tools were never designed with the requirements of these newer architectures in mind. When considering this issue, ask the tool vendor about the ability to handle large, complex designs. What features are available to simplify the description of complex circuit constructs? How large can a design description be before the tool begins to bog down? Can an entire chip design for a complex PLD or an FPGA be implemented using the tool? If you'll be doing such designs, don't simply rely on what the data sheet or sales rep says. Ask to see these capabilities in action so you know what to expect.

Price is an issue that everyone considers. Rather than looking simply at the cost of the tool, weigh the value of the productivity increase you'll receive.

DESIGN ENTRY

When considering design-entry options, think about the types of circuits you design. The best design-entry method is usually a function of the type of circuit you wish to implement. Boolean equations or schematics often work well for basic glue-logic applications. Truth tables make sense for decoding functions or other simple logic functions. Hardware-description languages that incorporate state-machine constructs are usually more efficient for more complex logic, such as control functions. Many tools offer more than one design-entry mechanism, so look for the ones that best meet the requirements for your circuit designs and still provide enough flexibility to handle future applications.

INTERFACES

The need to tie your programmable-logic design tool to other design tools is obviously a function of your specific design environment. Many designers who previously used standalone solutions are now discovering the productivity improvements available through better integration of design tools and functions. These capabilities vary widely, so look for the key elements required to support your design-tool environment. Draw a diagram to help you assemble the elements of the environment that are meaningful to you, and ask questions *(Fig. 3)*.

For example, can the programmable-logic system interface with your schematic-capture tools? How are programmable-logic elements specified in the schematic? What interfaces are available to simulate the programmable logic in the context of the rest of the system under development? Do these interfaces support timing simulation as well as functional simulation? Is the facility available to feed information forward to your pc-board-layout tools (i.e. the package and pinout used)? You may also have requirements for, or wish to take advantage of, interfaces to other advanced design tools, such as ASIC synthesis or automatic-test-vector generation.

PRICE

Of course, price is an issue that no one forgets to consider. But rather than looking simply at the cost of the tool, weigh the value of the productivity increase you'll receive. Saving a few hundred dollars by purchasing a lower-cost tool can be far overshadowed by the extra time spent overcoming that tool's limitations. Scrutinize the price-performance of the tool for your application—don't be afraid to choose a higher-priced system if it best meets your needs. The extra up-front investment can often mean significant savings in engineering resources that translate into an overall savings in project cost. Many users realize this savings with the first design project, but even more savings will result for the second and follow-on projects.

Other costs to consider are those associated with owning and maintaining the tool. Are there upgrades available to improve the tool's capabilities as your designs grow? What's the cost of obtaining the most current device support? Are maintenance contracts available or must you purchase product upgrades when new features become available? If you're considering replacement of an existing tool with a new one, don't forget the costs of migrating designs and re-training users. Again, all of these should be considered in the context of the productivity gains you're able to realize with your new system.

DEVICE SUPPORT

Needless to say, if the design tool you select doesn't support the devices you wish to use, your investment has no value. In addition to checking for the support of the devices you plan to use, don't overlook issues of quality and completeness of support. Quality of the support speaks to the vendor's development and testing process. This can give you an indication of what to expect in terms of usable device support. Completeness refers to the software's ability to take advantage of the unique attributes of the desired architecture. It's one thing to have support for a device, but without the ability to exploit its best (and usually most unique) features, the support may be of little value. If you plan to use an architecture with special features, make sure they're supported.

OTHER ISSUES

One leading issue often dismissed by users is the design methodology supported by the tools. What's the basic design flow and designer's approach to using the tool? Plan to select a tool that matches your expectations for design methodology. Many tools supplied by the device vendors support only devices from that manufacturer. Other tools are universal in nature and support many, if not all,

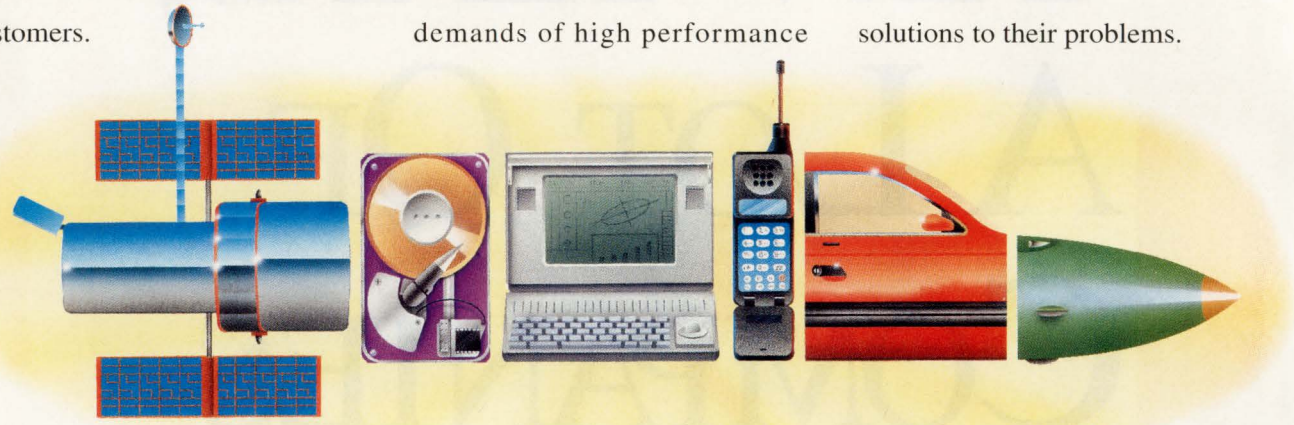
FOR TEN YEARS, A LOT OF COMPANIES HAVE GIVEN US PROBLEMS.

THE HISTORY OF LINEAR TECHNOLOGY FOR THOSE OF YOU WHO LIKE DETAILS (AND PICTURES).

It's crazy, isn't it? One day a bunch of enterprising young turks start a company.

Next thing you know it's a worldwide business doing $100M a year and you're celebrating your tenth anniversary.

See the companies listed in the border of this ad? Those are our customers.



Regretfully, we couldn't list them all. But over the last ten years, all of them have given us problems. Problems that required a cost effective, high performance linear solution. Which is good because when we started this business we figured the best way to become successful was to become the best at solving high performance linear application problems.

You might say that was our niche in the beginning. And it's still our niche today. In applications for computers, instruments, avionics, telephones, military and aerospace, all our energy is focused on delivering high performance linear solutions. Customers rely on us for analog products that meet the increasing demands of high performance systems. For high accuracy instrumentation, we've developed low noise operational amplifiers, references, and comparators. For high performance systems we provide high efficiency power supply ICs. We've created high speed amplifiers, interface circuits and A/D converters for data acquisition. For battery powered applications, we supply a wide range of micropower devices. And for communication systems, we offer high performance filters. We've advanced the state-of-the-art in areas of precision, speed, efficiency, quality and reliability as well as providing more complete solutions on a single chip. Our customers receive the most cost-effective solutions to their problems.

And every product we make is backed by a worldwide network of service and support.

How are we doing? So far, so good. Join the companies we've worked with over the last ten years — send us *your* problems. After all, that's what we're here for. And we've got a history of delivering the best high performance linear solution for the job. For more information please call 800-637-5545.

BRITISH AEROSPACE GENERAL DYNAMICS METTLER CONNER PERIPHERALS MITAC ALCATEL BOSCH

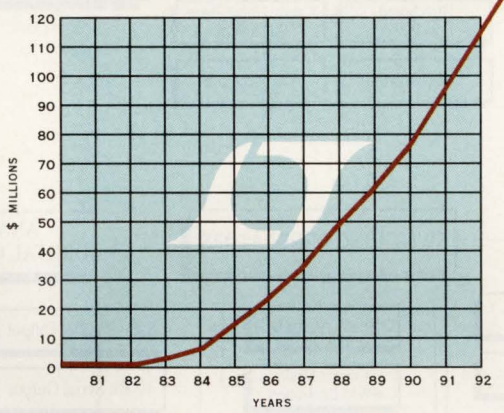
IBM NOKIA PHILIPS SIEMENS TANDY HITACHI LITTON ASTEC DAEWOO WESTERN DIGITAL MATSUSHITA

AND FOR THE REST OF YOU.

SO FAR,

10 Years $100 M/Year

SO GOOD.

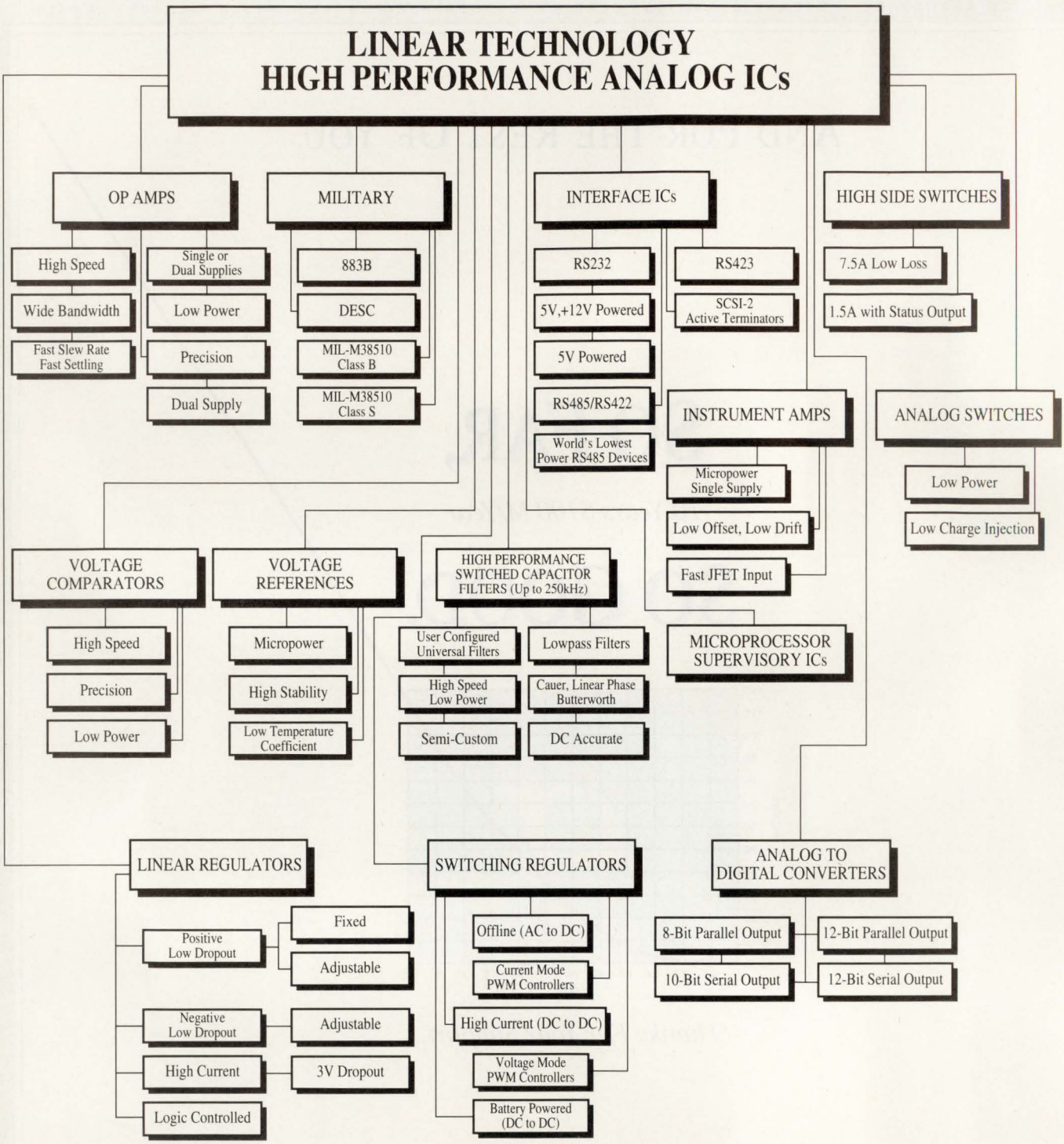


Thanks For Your Support.

LINEAR TECHNOLOGY

Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035

HUGHES SAMSUNG TEKTRONIX FUJITSU UTC BONDWELL FLUKE TEXAS INSTRUMENTS



LINEAR TECHNOLOGY

World Headquarters

Linear Technology Corporation
1630 McCarthy Boulevard
Milpitas, CA 95035-7487
Phone: (408) 432-1900
FAX: (408) 434-0507
Telex: 499-3977

CIRCLE 118 FOR U.S. RESPONSE

CIRCLE 119 FOR RESPONSE OUTSIDE THE U.S.

devices available. If you anticipate using devices from more than one manufacturer, one universal tool can provide significant benefits over multiple device-specific tools.

Also consider the design approach. The ability to easily retarget your design to alternate implementations depends on the approach. This is evidenced by the use of such techniques as device-independent design descriptions and support for multiple device partitioning.

Platform support and availability of training are two of a number of other issues that may be considered by some users. Applications support is also essential. Because the expectation for programmable-logic design is that designs can be done quickly, users often have short schedules to complete a design task. When a problem arises, the availability of good applications support can mean the difference between being frustrated and getting the job done. You may find that the level of support and responsiveness you get varies widely between vendors. The best way to judge this is to evaluate the applications support along with the tool.

Platform support and availability of training are two of a number of issues that may be considered. Applications support is also essential.

CONCLUSIONS

Many of the aforementioned issues were brought up by designers as important considerations when selecting a programmable-logic design tool. Realistically, most designers won't perform in-depth analyses in each area, and this isn't meant to suggest that they must.

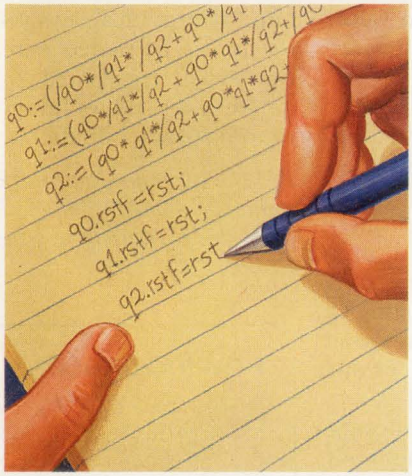
Programmable-logic design tools continue to become more capable and sophisticated with the growth in popularity of the architectures they support. As a result, the ensuing issues become more critical. Take the time to consider the items of greatest importance to you in the context of your design environment. With these items in mind along with an awareness of the topics presented here, you can be better prepared to focus on the real issues of importance to your specific situation.

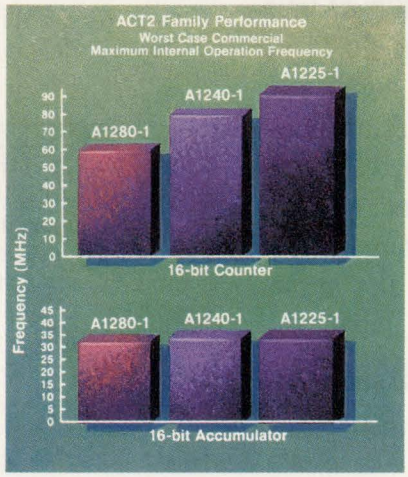
Bill Schulze, product marketing manager at Minc, has a BSEE from the University of Missouri, Rolla.

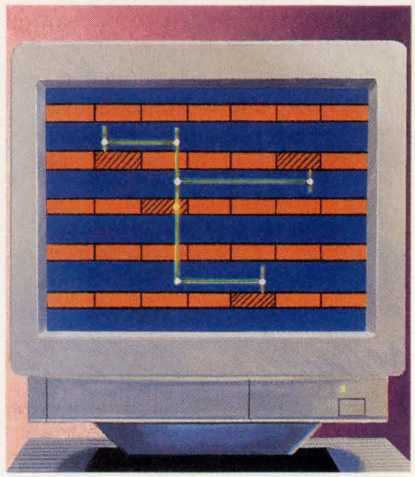
HOW VALUABLE?

HIGHLY	CIRCLE 544
MODERATELY	CIRCLE 545
SLIGHTLY	CIRCLE 546

You Design Actel FI
You Do A PLD. But Th







Use PLD Tools.

You design Actel FPGAs using the same tools as you would a PLD: ABEL,™ CUPL,™ LOG/iC™ and PGADesigner.™ But that's where the similarity ends.

Fast. Fast. Fast.

Our FPGAs are real speed demons. Whatever application you may be working on, our parts will give you the kind of performance you're looking for.

100% Automatic Place And Route.

Coupled with your PLD tools, Actel's Action Logic™ System (ALS) software lets you create your own FPGAs—using a 386 PC or workstation—right at your own desk. With Auto Place and Route that's proven in thousands of applications.

Announcing A Simple Way To Get From PLDs To FPGAs.

If you're a PLD designer with an interest in fast, flexible FPGAs, but you think you don't have time to learn new design techniques, we'd like to change your mind.

First of all, you don't have to give up your existing PLD design tools or Boolean equations. Actel's ALES™ 1 program translates the output of PLD tools like CUPL™ and LOG/iC™ into logic optimized for our ACT™ devices. ABEL™ 4.0 includes optimization for Actel devices. Entire FPGA designs can be developed with PGADesigner.™

Actel devices offer everything you want in an FPGA. Like high I/O and flip-flop counts. And 100% automatic place and route gets you to market fast.

Once your FPGA is designed, our Action Logic™ System (ALS) converts the captured design into a completed device in minutes. To give you true, high-density, field-programmable, channeled gate arrays.

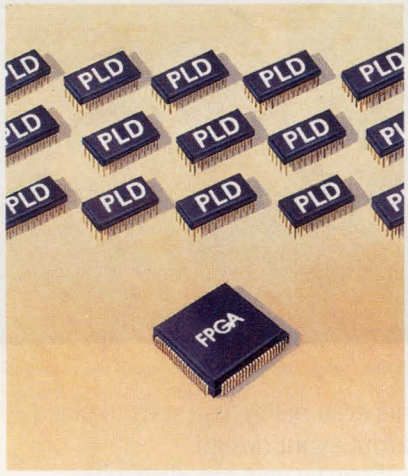
Other FPGA manufacturers fall short on design verification. Our exclusive Actionprobe® diagnostic tools, give you 100% observability of internal logic signals. So you don't have to give up testability for convenience.

It's never been easier to make your innovative designs a reality. We offer you a complete family of powerful FPGAs, like the A1010 and A1020, available in 44, 68 and 84 pin PLCC versions and implementing up to 273 flip-flops or up to 546 latches. And the first member of our ACT 2 family, the power-

'GAs The Same Way
e Similarity Ends There.

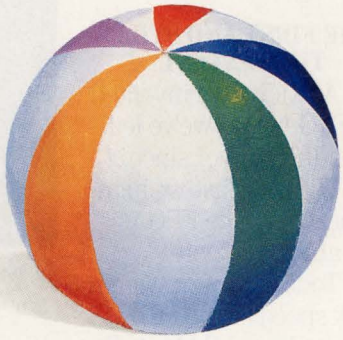
More Flexibility And Capacity.

Designing with Actel FPGAs gives you more freedom than you ever imagined. More gates. More flip-flops. More I/O. In fact, our new A1280 is the largest FPGA in the world.



Small Footprint.

Actel FPGAs give you far more gates per square inch. As much as ten times as many as the densest PLDs. That can save a lot of real estate.



More Fun.

Designing Actel FPGAs is so simple that you'll have more time to do the things that made you want to become an engineer in the first place. Or just relaxing. You've earned it.

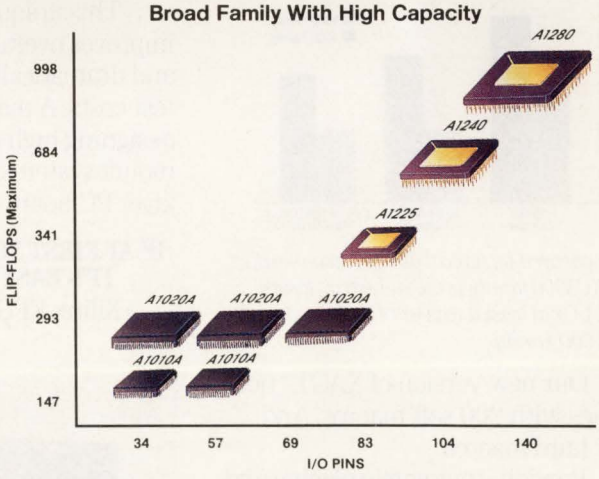
ful A1280. With 8,000 gates, up to 998 flip-flops, and 140 I/O pins, it's the highest capacity FPGA today. And our A1240-1 is the fastest. In the A1240-1, 16-bit counters run at 75 MHz, 16-bit accumulators at 33 MHz. Enough capacity and speed to handle almost any application.

The superior speed, capacity, and auto place and route capabilities of our FPGAs are made possible by Actel's revolutionary PLICE® antifuse programming element. The advanced technology that makes our family of FPGAs an ideal way to unleash your engineering creativity.

The FPGA Design Guide

Call **1-800-228-3532** for your free FPGA Design Guide.

Broad Family With High Capacity



Actel

Risk-Free Logic Integration

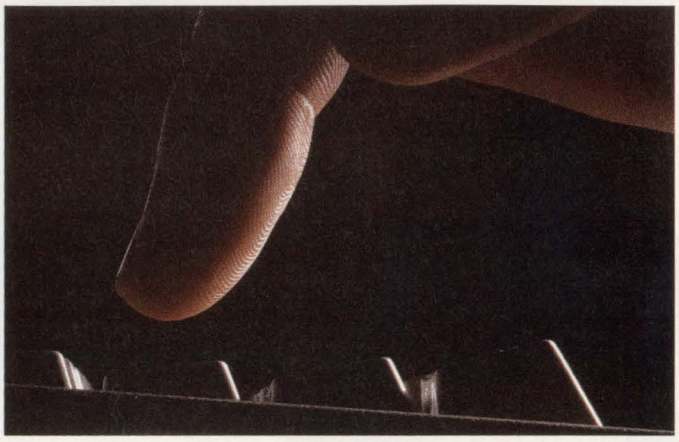
CIRCLE 184 FOR U.S. RESPONSE

CIRCLE 185 FOR RESPONSE OUTSIDE THE U.S.

IN THE TIME IT TAKES TO READ THIS AD, YOU COULD ROUTE THE WORLD'S FASTEST FPGA.

Believe it or not, it only takes about 150 seconds to place and route a Xilinx FPGA.

It will probably take you longer to read this ad.



Our new push-button software makes programming other logic devices seem positively tedious.

THE FIRST AND STILL THE FASTEST.

At Xilinx we invented the FPGA. And we've led the industry ever since.

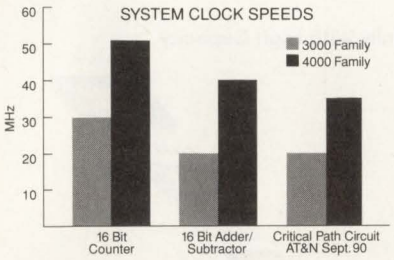
With the fastest, highest performance FPGAs available anywhere.

Today, we offer system clock speeds of 60 MHz. With on-board RAM. And on-chip wide decode.

Making our newest FPGAs ideal for everything from FIFOs to address decoding.

NEW ENHANCED SOFTWARE PROVIDES PUSH BUTTON SOLUTION.

To make Xilinx FPGAs even faster and easier to program, we've redesigned our software.



As measured by typical design benchmarks, the XC3000 family is the industry's fastest FPGA. Or at least it was until we introduced the 4000 family.

Our new version of XACT™ now comes with 200 soft macros. And fifty hard macros.

Providing automatic placing and routing for virtually all designs. With greater than 90% gate utilization.

If you've worked with Xilinx FPGAs before, you'll see improvements even before you start to place and route your design.

If you've never worked with Xilinx FPGAs before, you'll find every other logic device to be positively tedious by comparison.

WHEN IT COMES TO SYSTEM TESTING, WE PASS WITH FLYING COLORS.

Our newest FPGAs offer you the industry's first on-chip JTAG boundary scan for easy testing of PC boards and device I/Os.

This unique Xilinx offering improves overall system testability and dramatically reduces board test costs. A major boost for those designing high-density, surface mount systems or complex, multilayer PC boards.

IF AT FIRST YOU DON'T SUCCEED, IT'S EASY TO TRY AGAIN.

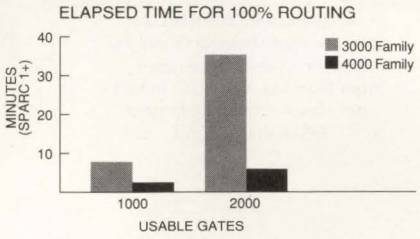
Xilinx FPGAs can be quickly reprogrammed an unlimited number of times.

Our FPGAs save you an enormous amount of time right up front. And they also save you time later when you need to make those "last minute" enhancements.

It's one more way we make it easier for you to get your product to market as fast as possible.

GETTING AN EDGE OVER YOUR COMPETITORS IS JUST A PHONE CALL AWAY.

If you've read this far, you could have already placed and routed one of our FPGAs.



New algorithms have reduced place and route times by a factor of four.

So don't delay. No other programmable logic company offers you the many exclusive features of Xilinx FPGAs.

Call 1-800-255-7778. Or in California, 408-559-7778. And we'll send you more information on how our FPGAs can give you the competitive edge.

But you better hurry.

Some of your competitors have already finished reading this ad.

XILINX

The Programmable Gate Array Company.SM

CIRCLE 182 FOR U.S. RESPONSE

CIRCLE 183 FOR RESPONSE OUTSIDE THE U.S.

Streamline programmable-logic design with the proposed LPM standard

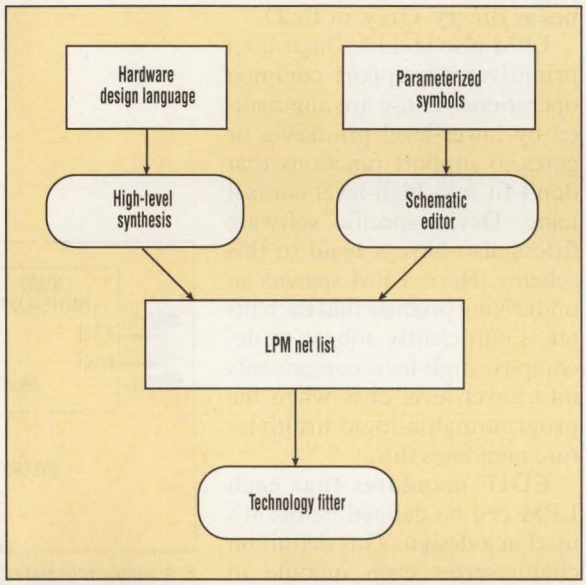
An up-and-coming PLD and FPGA standard will allow for technology-independent design.

BY MICHAEL HOLLEY
Data I/O Corp., 10525 Willows Rd. N.E., P.O. Box 97046, Redmond, WA 98073-9746; (206) 881-6444.
AND CECIL KAPLINSKY
Plus Logic Inc., 1255 Parkmoor Ave., San Jose, CA 95126; (408) 293-7587.

Today's system designers enjoy an embarrassment of riches in programmable-logic-device (PLD) and field-programmable-gate-array (FPGA) architectures, and more continue to be available. There's a host of benefits associated with the growing array of devices, but the catch is having to buy separate, proprietary development tools for each architecture.

Buying separate tools translates into two major downsides for system designers. One drawback is being forced to learn and utilize new and incompatible silicon vendors' tools with each PLD or FPGA architecture they select. The second drawback is that even if third-party front-end tools for these newer architectures are available, users are bound by limitations because each PLD or FPGA maker has a proprietary net-list format that the CAE supplier must support.

These issues are addressed by an interface that's been proposed as a standard by a group of over 30 silicon and tool vendors. Called the Library of Parameterized Modules (LPM) standard, its objectives include handing engineers using PLDs and FPGAs more efficient, easier access to various architectures through synthesis tools; keeping designs technology independent longer in the design flow; and providing a generic, technology-independent set of logical primitives for structuring a high-performance design, regardless of the technology that will be used to build the chip.



1. The LPM net list is generated from design entry, either through a high-level design language or a schematic editor. The net list is then sent to a technology fitter for implementation.

LPM takes into account tool structures and a design flow so that engineers can maintain one design environment, yet opt for a wide variety of silicon implementations. Design entry tools, whether they're hardware description languages (HDLs) or schematic capture, will output an LPM net list either directly or through a high-level synthesis tool. The net list then becomes input to the technology-implementation tools, which are called device fitters. These tools are currently produced by programmable-logic vendors and third-party tool houses *(Fig. 1)*.

At the heart of the proposed LPM standard lies a set of 25 parametrized modules used in creating a net list that describes a logic design. Most of the module-creation work was done by Steve Kelem of Xilinx, Dave Allen of Viewlogic, and William Wright of Mentor Graphics. The net list is based on EDIF 2.0.0, and conforms to all syntax detailed in the EIA EDIF standard. To meet LPM's objectives, the modules can completely specify a design, and make it easier and faster to implement dense designs. In addition, the proposed LPM standard provides an avenue to any implementation technology: ASIC, FPGA, PLD, or medium-scale-integration (MSI) components.

The 25 modules were selected on the basis of the array of engineering benefits given to designers, including completeness, or-

TABLE 1. LPM PRIMITIVES CATEGORIES

Small primitives: Constant, Inverter, AND gate, OR gate, XOR gate, Multiplexer, and Tristate.
Arithmetic primitives: Adder, Compare, Multiplier, Shifter, Decoder, Incrementer/Decrementer/Negate, and Absolute value module.
Storage primitives: Latch, D flip-flop, T flip-flop, Counter, RAM-DQ, and RAM-IO. The RAM-DQ represents a RAM with separated inputs and outputs, and the RAM-IO is similar to SRAM ICs with a single data bus for input and output.
Pad primitives: Inpad, Outpad, and Bipad for input, output, and bidirectional ports, respectively.
Table primitives: Truth table and a Finite state machine.

TABLE 2. SOURCE CODE FOR AN LPM REGISTER CELL

```
(cell MYREG (cellType Generic) (view view_1 (viewType Netlist)
    (interface
        (port ACLEAR (property Polarity (string "Invert")))
        (port DATA3) (port DATA2) (port DATA1) (port DATA0)
        (port RESULT3) (port RESULT2) (port RESULT1) (port RESULT0)
        (port TESTENB) (port TESTIN) (port TESTOUT)
        (port Clock)
        (property LPMTYPE (string "DFF"))))
```

thogonality, popularity, and getting rid of the difficulty associated with decompiling. LPM supplies a complete set of logic functions so that any Boolean function can be implemented. To address orthogonality, the modules reduce the duplication of functions implemented in different ways. For example, while a shift register isn't included in LPM, it can be structured with the optional shift I/O of the proposed standard's D flip-flop module. Another option is to have the adder module become a subtracter by complementing the inputs. Only the most common functions were defined as separate modules to maintain a reasonable number. Lastly, logic functions too difficult to recognize after low-level gate decomposition are included in the LPM standard.

Modules fall into five primitives categories: small, arithmetic, storage, pad, and table *(Table 1)*. Configurability of these modules is the essence of LPM. Each module comes with several different options for customizing functionality. Foremost is the ability to handle inputs of any width. For instance, the AND module can have any number of inputs, which can also be buses of any width. Consequently, it's possible to create a 7-input AND gate so that each input is a 4-bit bus, and the output is 4 bits wide. Moreover, each of the parameterized module's inputs and outputs can be individually inverted.

Storage-primitive options include scan test path, asynchronous and synchronous sets and resets, and others. Also, some modules carry properties to modify their functions. An example is the counter module, which has a representation property for accepting such values as Binary, Grey, or BCD.

LPM also includes high-level primitives to support common operations. Those are augmented by lower-level primitives or gates to support functions that don't fit into high-level control logic. Device-specific software fitters also have a hand in this scheme. Here, LPM spawns an underlying premise that each fitter is sufficiently robust to decompose high-level components into lower-level ones when the programmable-logic architecture mandates this.

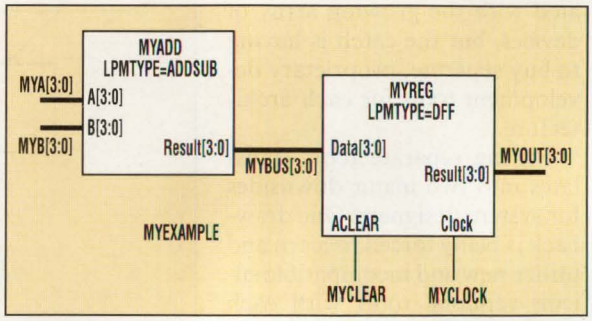
EDIF mandates that each LPM cell be defined before it's used in a design. This definition characterizes each module to the specific configuration that satisfies the requirement. That's done by specifying the name, pins, and properties associated with a given module.

Names appear as a string value property called LPMTYPE, such as: (property LPMTYPE (string "DFF")). Module parts are defined so that their names characterize each module, which has some required, optional, and illegal combination pins. Though some pin names aren't explicitly named in the LPM specification, they're named symbolically, such as decoder output pins or EQn (n = an integer or value to be decoded). A valid port in this instance is (port EQ4).

Vector pin names are specified utilizing the "_" character as a delimiter. A good example is a 3-input AND module that has 4-bit buses as inputs. The part name for the third bit in the second input is (part DATA1_2).

Next, as the name implies, required pins must be in each LPM module definition. Otherwise, errors occur. An example is the data-input pin (DATAn) on a D flip-flop. On the other hand, optional pins generally add other functions. Examples include scan-test inputs on storage primitives or the carry-out signal on the adder module.

Some modules have pins that can't be simultaneously specified, which are called illegal combination pins. Using them in a cell definition usually leads to errors. An example is combining the asynchronous constant pin (ACONST) with the asynchronous set pin (ASET) on the latch module.



2. A simple schematic called MYEXAMPLE is created using two LPM modules—an adder and a register. This circuit adds two numbers and stores the result in a register until the next clock cycle.

Lastly, most modules have associated properties. They can be a constant-load value in storage primitives, assumed representation of the signed or unsigned input in the compare module, or the module operations table for the finite-state machine. Properties are attached to the cell definition through the standard EDIF property mechanism with the desired value. The proposed LPM standard then specifies the values that are valid for all recognized properties. Otherwise, non-standard values for standard properties are regarded as errors.

Two exceptions are the LPMHINT and Polarity prop-

Don't be boxed in by ABEL™-FPGA's 1,000-gate capacity.

PGADesigner's 27,500-gate capacity gives you some breathing room.

By their own admission, "...ABEL™-FPGA can safely handle 1,000 gates..." With today's FPGAs pushing 10,000 gates, a 1,000-gate design tool just won't cut it. You have to slice-up your design into "modules" and do it a piece at a time.

That doesn't make sense. Not when MINC's PGADesigner gives you the design capacity for today's largest FPGA... and then some. You'll not only have elbow room now, but room to grow, too.

Unlike ABEL-FPGA, which is based on the ABEL™ PLD compiler, PGADesigner is a design synthesis system which allows you to design entire FPGAs in a single file for device design, optimization and simulation. By simulating entire designs, you can check functionality without going through place and route... another time and money saver.

It's performance like this that's made MINC the choice of Xilinx and Actel. And why PGADesigner is being fully integrated and resold by the leading CAE vendors. It's also one of many reasons we have more installed seats for PLD and FPGA design tools on UNIX systems than any other supplier of programmable design synthesis tools.

So unwind and call us today! Ask for our FPGA Design Capacity Analysis and find out what you can do with a *real* FPGA design tool. And for a limited time, we'll include a FREE FPGA device library when you purchase PGADesigner.

P G A Designer MINC

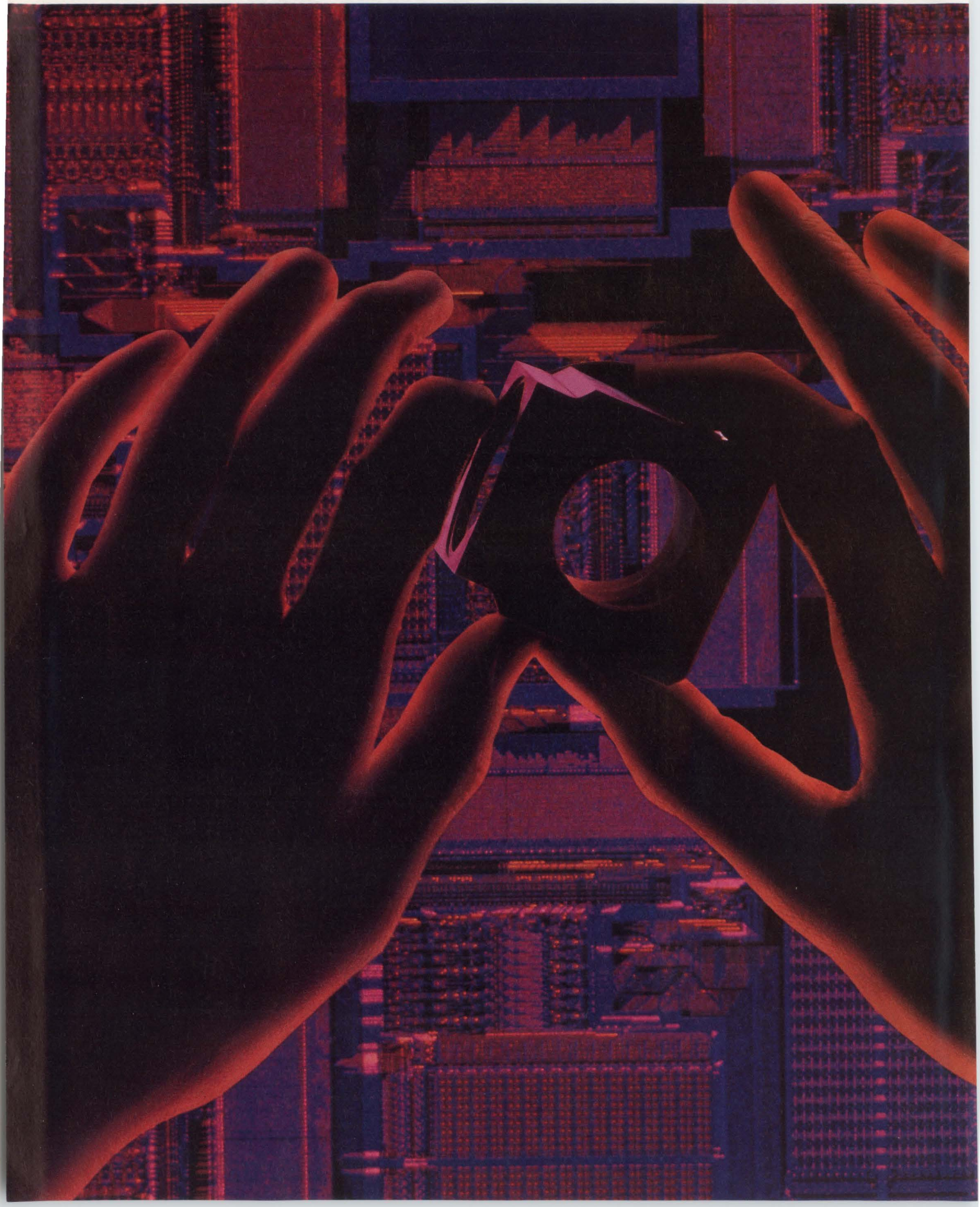
MINC

INCORPORATED

MINC Incorporated, 6755 Earl Drive, Colorado Springs, CO 80918 (719) 590-1155 Fax: (719) 590-7330

CIRCLE 126 FOR U.S. RESPONSE CIRCLE 127 FOR RESPONSE OUTSIDE THE U.S.

Putting you 3.3V ahead of



the portable market.

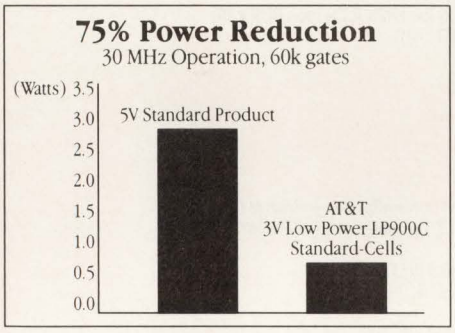
That's AT&T "Customerizing."

These days, a dream design for a portable system can become a nightmare overnight. By the time you launch, you may be late to market.

"Customerizing" means helping you differentiate your product. By providing a 3.3 volt, reduced-heat route to a smaller, lighter, longer-operating notebook, disc drive or cellular system. And by giving you all the latitude you need to add product enhancements of your own.

3 times longer battery life

Our 3.3V ASIC solution enables you to slash system power requirements. Lets you pack more circuit gates within inexpensive plastic packages. And achieve tighter IC packaging densities.



3.3 volt CMOS ASIC library

Speed and simplify your 3.3 design-in with AT&T's exclusive LP900C 3.3V library. A 0.9 micron, CMOS ASIC library that includes over 400 3.3V standard cells, optimized from our existing, industry-standard 5V library.

Our 3.3V performance also extends to industry standard PC macrocells including RAM, ROM, a DMA controller, UART and 80C51-compatible microcontroller.

More 3.3V ASICs design tools

Our libraries are ported to CAD tools like AT&T, Mentor Graphics, Synopsys, Verilog and Viewlogic, providing the symbols, simulation models and ERC tools you need to ensure optimum 3.3V circuit operation.

So if 3.3 sounds like a "portable" number you'd like to try, ask for our 3.3 Volt ASIC Information Package, including Data Book and Product Brief. Just call AT&T Microelectronics at 1 800 372-2447, ext. 633.

AT&T Microelectronics

CIRCLE 209 FOR U.S. RESPONSE

CIRCLE 210 FOR RESPONSE OUTSIDE THE U.S.

erties. The former is optional. It can contain further technology-specific data to be used in silicon-vendor tools. Though no standard values for this field exist, the option to include this property rests with design-tool suppliers and field-programmable-gate-array makers to use as needed.

Polarity for inverting any signal, on the other hand, can be attached to any port during a module's cell definition. Control I/O can thus be either active high or active low. An input's polarity defaults to positive active, meaning no inversion is performed. So here, the only accepted value for this property is "Invert". An example is (portACLEAR (property Polarity (string "Invert")).

One example pulls these elements together to define a complete LPM cell *(Table 2)*. It describes a 4-bit register structured for the D flip-flop module. Included are scan test circuitry and an asynchronous clear input (ACLEAR). In this instance, ACLEAR's polarity is inverted to produce negative active. Also, because all ports default to no inversion or positive active, the remaining ports specify no polarity property.

EDIF's pervasiveness and maturity, as well as relevant features, suit it for designing the LPM net list on top of it. Because this net-list information existed, it made sense to reference it rather than invent new information.

The EDIF net lists adhere to a strict declaration-before-use rule. This means every component must be defined in a library before it can be used. Accordingly, an EDIF net list of LPM modules must have a number of cell definitions before the net list appears. Cell definitions can therefore be regarded as fully described modules in the proposed standard's library. Once defined, any number can be instantiated in the net list.

For example, the AND module is parametrized in the number and width of inputs. Before using a 2-input AND gate for 16-bit buses, a cell must be defined and named in the EDIF net list. If an LPM net list contains two different AND modules, such as a 2-input AND gate for 16-bit buses and a 3-input AND gate for 8-bit buses, then two separate cell definitions are required. Each of these cell definitions will have the property LPMTYPE with the value AND, but the port declarations and names of the cells will be different. However, if the net list contained two instances of the 16-bit-wide, 2-input AND, then only one cell de-

TABLE 3. LPM EDIF SOURCE CODE FOR MY EXAMPLE

```
(edif myexample (edifVersion 2 0 0) (editLevel 0) (keywordMap) (keywordLevel 0))
    (library MYEXAMPLE
        (editLevel 0)
        (technology (numberDefinition (scale 1 (E 1 12) (unit Capacitance))))

        (cell MYADD
            (cellType Generic)
            (view view
                (viewType Netlist)
                (interface
                    (port A3) (port A2) (port A1) (port A0)
                    (port B3) (port B2) (port B1) (port B0)
                    (port RESULT3) (port RESULT2) (port RESULT1) (port RESULT0)
                    (property LPMTYPE (string "ADDSUB")))))

        (cell MYREG
            (cellType Generic)
            (view view
                (viewType Netlist)
                (interface
                    (port ACLEAR)
                    (port Clock)
                    (port DATA3) (port DATA2) (port DATA1) (port DATA0)
                    (port RESULT3) (port RESULT2) (port RESULT1) (port RESULT0)
                    (property LPMTYPE (string "DFF")))))

        (cell MYEXAMPLE
            (cellType Generic)
            (view view
                (viewType Netlist)
                (interface)
                (contents
                    (instance (rename INST1 "$1|1") (viewRef view (cellRef MYADD)))
                    (instance (rename INST2 "$1|2") (viewRef view (cellRef MYREG)))
                    (net MYBUS0 (joined
                        (portRef DATA0 (instanceRef INST2))
                        (portRef RESULT0 (instanceRef INST1))))
                    (net MyBUS1 (joined
                        (portRef DATA1 (instanceRef INST2))
                        (portRef RESULT1 (instanceRef INST1))))
                    (net MYBUS0 (joined
                        (portRef DATA2 (instanceRef INST2))
                        (portRef RESULT2 (instanceRef INST1))))
                    (net MYBUS0 (joined
                        (portRef DATA3 (instanceRef INST2))
                        (portRef RESULT3 (instanceRef INST1))))
                    (net MYA0 (joined (portRef A0 (instanceRef INST1))))
                    (net MYA1 (joined (portRef A1 (instanceRef INST1))))
                    (net MYA2 (joined (portRef A2 (instanceRef INST1))))
                    (net MYA3 (joined (portRef A3 (instanceRef INST1))))
                    (net MYB0 (joined (portRef B0 (instanceRef INST1))))
                    (net MYB1 (joined (portRef B1 (instanceRef INST1))))
                    (net MYB2 (joined (portRef B2 (instanceRef INST1))))
                    (net MYCLEAR (joined (portRef ACLEAR (instanceRef INST2))))
                    (net MYCLOCK (joined (portRef CLOCK (instanceRef INST2))))
                    (net MYOUT0 (joined (portRef RESULT0 (instanceRef INST2))))
                    (net MYOUT1 (joined (portRef RESULT1 (instanceRef INST2))))
                    (net MYOUT2 (joined (portRef RESULT 2 (instanceRef INST2))))
                    (net MYOUT3 (joined (portRef RESULT 3 (instanceRef INST2))))
(design ROOT
        (cellRef MYEXAMPLE
            (libraryRef MYEXAMPLE))))
```

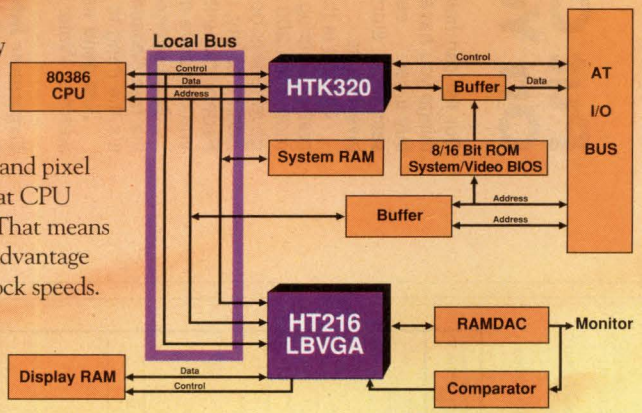
Local Bus Graphics Solutions

The Next Standard in VGA Performance

The industry's first local bus VGA controller, the HT216, dramatically improves the performance of all graphics applications.

Local Bus CPU Implementation—The Bus of the Future

The standard VGA controller is limited by the 8MHz ISA Bus bottleneck. The HT216's CPU local bus allows commands and pixel data to be transferred at CPU speeds up to 33MHz. That means the HT216 takes full advantage of fast 386 and 486 clock speeds. The result—greatly improved performance without the high cost of a graphics co-processor.



Optimizes Windows™ Performance

The HT216 features a 32-bit system address bus interface, and an independent dot and memory clock, which permit the processing of asynchronous events. By placing the VGA graphics controller on the CPU local bus and incorporating Windows raster operations functions, the HT216 displays Windows applications two to four times faster than standard VGA controllers—at very little added cost.

Core Logic that Supports Local Bus

Headland also offers a family of 386SX/DX core logic products that supports the local bus HT216.

The HTK320 supports the 386DX at system frequencies of up to 40MHz and supports local bus peripherals, including the HT216. The HT15 runs at zero wait states with the 386SX to 20MHz—offering the best price performance for an entry level 386SX system.

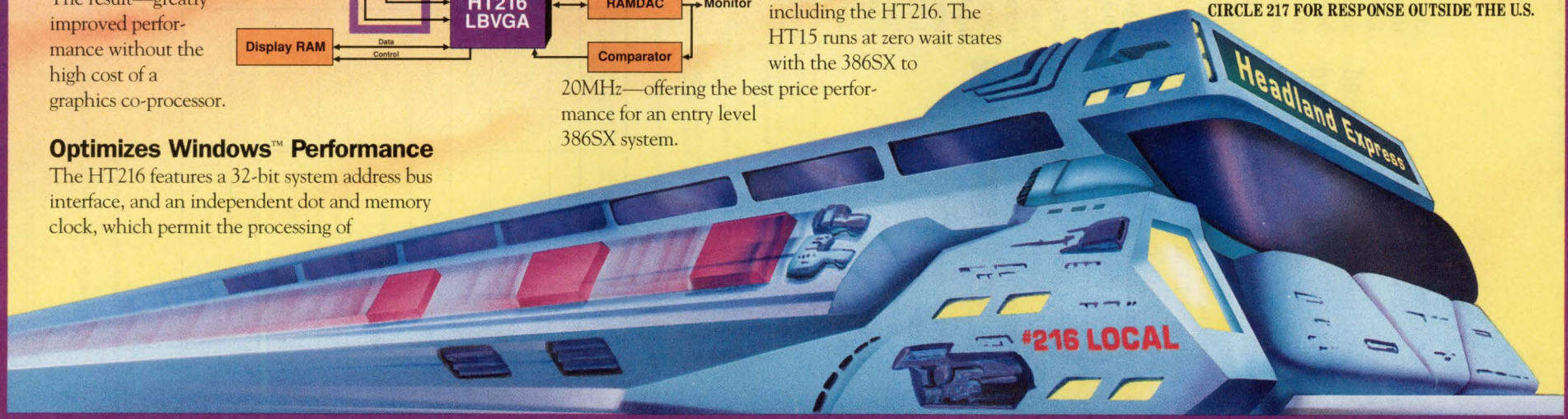
Catch the Bus of the Future

Call Headland Technology to find out more about the HT216 and our other local bus graphics and core logic products. Catch the local bus now. Don't get left behind.

Headland
Technology Inc
Call 800-238-0101

CIRCLE 216 FOR U.S. RESPONSE

CIRCLE 217 FOR RESPONSE OUTSIDE THE U.S.



CATCH THE LOCAL BUS

scribing it would be necessary and two instances would exist within the net list.

EDIF 2.0.0 can be interpreted in several ways for bus notation. In some implementations bus rippers are used to indicate connections between nets. In other instances, name association is used to indicate connections between nets. The proposed LPM standard uses a least-common denominator of these two interpretations. At the present time, the EDIF standards committee is addressing some bus notation concerns for EDIF 2.1.0. When that specification is complete, a more efficient LPM implementation can build on it.

In LPM net lists today, each bus wire must be represented by a single net, and each pin or bus port must be represented by a single pin. Though this is inefficient, it's the implementation that will be understood by all EDIF net-list packages. An example is the best way to show how a design appears using the proposed library modules *(Fig. 2 and Table 3)*.

The proposed LPM standard has an immediate positive impact on logic designs because it helps make the designs technology-independent.

The proposed LPM standard has an immediate positive impact on logic designs. It helps make designs technology-independent, and can transfer designs from one chip architecture to another. It doesn't solve all of the problems, however, so some areas need further work. One such area is fitter estimator interaction. Problems in this area could be solved with a standard tool interface that allows high-level synthesis tools to omit LPM modules which can't be handled by an implementation technology. In addition, a standard set of behavioral simulation models for LPM modules would be valuable in a CAE tool set. Subsequently, these original LPM primitives could be expanded to a wider class of functions. That's likely as FPGAs continue to absorb increasingly larger designs, thus giving rise to LPM II.

Mike Holley, a senior staff engineer with Data I/O, holds a BSEE from Seattle University, Wash.

Cecil Kaplinsky, consultant at Plus Logic, has BS and MS degrees in physics from the University of Cape Town, South Africa.

HOW VALUABLE?

HIGHLY	CIRCLE 547
MODERATELY	CIRCLE 548
SLIGHTLY	CIRCLE 549

Statement of Ownership, Management and Circulation of ELECTRONIC DESIGN (ISSN 0013-4872) for October 1, 1991 compliance. Published semimonthly at 1100 Superior Avenue, Cleveland, Ohio 44114-2543 (Cuyahoga County).

The publisher of ELECTRONIC DESIGN is Paul C. Mazzacano; the editor is Stphen E. Scrupski; and the managing editor is Bob Milne. They are located at 611 Route 46 West, Hasbrouck Heights, NJ 07604.

ELECTRONIC DESIGN is owned by Penton Publishing, Inc. 1100 Superior Avenue, Cleveland, Ohio 44114-2543, a wholly owned subsidiary of Pittway Corporation, 200 So. Wacker Dr., Suite 700, Chicago, Illinois 60606.

The known bondholders, mortgagees, and other security holders owning 1% or more of total bonds, mortgages, or other securities are: none.

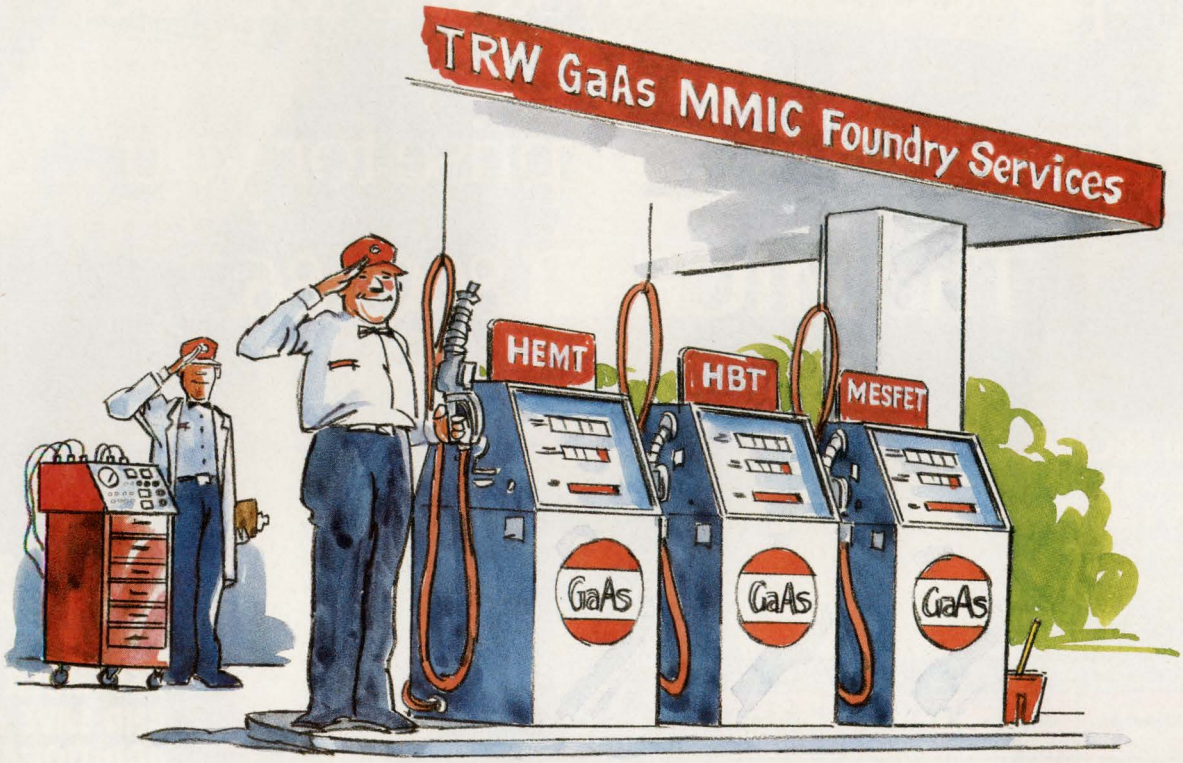
EXTENT AND NATURE OF CIRCULATION	AVERAGE NO. COPIES EACH ISSUE DURING PRECEDING 12 MONTHS	ACTUAL NO. COPIES OF SINGLE ISSUE PUBLISHED NEAREST TO FILING DATE
A. TOTAL NO. COPIES (*Net Press Run*)	175,578	174,609
B. PAID AND/OR REQUESTED CIRCULATION 1. SALES THROUGH DEALERS AND CARRIERS, STREET VENDORS AND COUNTER SALES	-0-	-0-
2. MAIL SUBSCRIPTION (*Paid and/or requested*)	170,459	169,995
C. TOTAL PAID AND/OR REQUESTED CIRCULATION (*Sum of 10B1 and 10B2*)	170,459	169,995
D. FREE DISTRIBUTION BY MAIL CARRIER OR OTHER MEANS SAMPLES COMPLIMENTARY, AND OTHER FREE COPIES	3,426	3,133
E. TOTAL DISTRIBUTION (*Sum of C and D*)	173,885	173,128
F. COPIES NOT DISTRIBUTED 1. OFFICE USE, LEFT OVER, UNACCOUNTED, SPOLIED AFTER PRINTING	1,693	1,481
2. RETURN FROM NEWS AGENTS	-0-	-0-
G. TOTAL (*Sum of E, F1 and 2—should equal net press run shown in A*)	175,578	174,609

SUBSCRIPTION RATES — 1 Year
U.S. — $85.

I certify that the statements made by me above are correct and complete.

Sal F. Marino, Chairman and CEO, Penton Publishing, Inc.

TRW — Your Full Service GaAs Station



TRW's GaAs foundry pumps out a full selection of custom MMIC design, fabrication, and testing services. Our three grades of GaAs technology — HEMT, HBT, and MESFET — deliver world class performance for analog signal processing applications from dc to more than 60 GHz.

What's more, we're easy to do business with. We custom fit our services around your specific foundry needs — regardless of your MMIC experience level.

For veteran MMIC users, for example, we offer traditional foundry services: you design a MMIC using our process design rules, then we'll fabricate, test, and deliver wafers or die to our established process control monitor specifications.

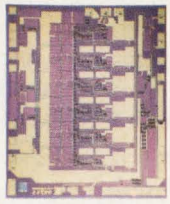
If you're traveling the MMIC road for the first time, our full-service engineering staff will help you map out a MMIC strategy, acquaint you with our foundry design rules, then show you how to get the most mileage out of our MMIC fabrication, testing, and dicing services.

If you'd like to fill up on our GaAs MMIC foundry services, please call: **1-800-GETMMIC.**

MMIC Foundry Services Manager
TRW Electronics & Technology Division
One Space Park
Redondo Beach, CA 90278
FAX: 213.812.7011

Now available at TRW's GaAs pump:

Technology	f_{MAX}
0.2 µm HEMT	60 GHz
2.0 µm Emitter HBT	20 GHz
0.5 µm MESFET	20 GHz



65 dB Dynamic Range HBT Log Amp

TRW

CIRCLE 178 FOR U.S. RESPONSE

CIRCLE 179 FOR RESPONSE OUTSIDE THE U.S.

WARNING!

If you're considering Intel or Applied Microsystems for your next ICE™ Microtek has a surprise for you . . .

The MICE-III 80C186.

The MICE-III 80C186

- Includes source level debug
- Comes with a megabyte of overlay memory
- Has a high-speed link
- Supports most popular "C" compilers

...and costs substantially less than the competition!

Vendor/Product	High Speed Link	Overlay Memory	Microsoft C Support	Price as Configured
APPLIED ES-1800-80C186	SCSI Interface OPTIONAL	1 Megabyte OPTIONAL	Combined 3rd Party Tools OPTIONAL	$25,000
INTEL ICE-186	3rd Party GPIB Card OPTIONAL	1 Megabyte OPTIONAL	Combined 3rd Party Tools OPTIONAL	$21,995
MICROTEK MICE-III 80C186	High Speed Parallel Standard	1 Megabyte Standard	hyperSOURCE Tookhain Standard	$12,495

BUY A MICE-III-80C186 DEVELOPER'S KIT BEFORE DECEMBER 31, AND SAVE AN ADDITIONAL

$1,995

with a FREE hyperSOURCE-186 high level interface!

That's right. In one package, you get a comprehensive hardware/software debug solution for your embedded microprocessor applications. You don't need to buy those "optional" extras to close the holes in your development path. All you need is the compiler of your choice.

And the savings are not limited to one processor. Check our prices for emulation support for 286, 386, 386SX, 486, 486SX™, AM386, AM386SX™, 68000/10/20/30, 68EC020/30, and 68302™ microprocessors and see if those don't surprise you, too.

Combine feature-rich, real-time emulation, fully-integrated high level language interfaces, and a full-time technical support team with applications experience in targets ranging from aerospace to ultrasound, and it's no surprise that Microtek has over 26,000 emulator installations worldwide.

Save money. Save time. Call MICROTEK today at 1-800-886-7333, ext. 1.

CIRCLE 124 FOR U.S. RESPONSE CIRCLE 125 FOR RESPONSE OUTSIDE THE U.S.

MICROTEK

The Leader in Development Systems Technology™

MICROTEK INTERNATIONAL, INC. Development Systems Division
3300 N.W. 211th Terrace, Hillsboro, OR 97124 • (503) 645-7333 • Fax (503) 629-8460

PROGRAMMABLE LOGIC DESIGN TOOLS

Company	Product	Platform	Design entry	Output	Features	Price	Type
Accel Technologies Inc. 6825 Flanders Dr. San Diego, CA 92121-2986 (800) 488-0680 CIRCLE 601	Tango-PLD	D	L,S,B,SM,TT	J	LO,FS	$595	NDS
Actel Corp. 955 E. Arques Ave. Sunnyvale, CA 94086 (408) 739-1010 CIRCLE 602	Action Logic System 2.1	D	L,S,B,SM	N	LO,FS	$2,950	DS
	Actel Logic Optimizer	D	L,S,B,SM	N	LO	$995-$1,495	DS
Advanced Micro Devices Inc. 901 Thompson Pl. Sunnyvale, CA 94088-3453 (800) 538-8450 CIRCLE 603	Palasm 4	D	S,B,SM	J	LO,FS	$125	DS
Altera Corp. 2610 Orchard Pkwy. San Jose, CA 95134 (408) 984-2800 CIRCLE 604	Max+Plus II	D,U	L,S,W,B,SM,TT	N,J,O	LO,FS,MDP,ADS	$4,995-$10,995	DS
Atmel Corp. 2125 O'Nel Dr. San Jose, CA 95131 (408) 441-0311 CIRCLE 605	Atmel-Abel-4	D	L,S,B,SM,TT	J	LO,FS,ADS	$350	DS
AT&T Microelectronics 555 Union Blvd. Allentown, PA 18103 (800) 372-2447 CIRCLE 606	AT&T FPGA Design Tools	D,U	L,S,B,SM	N,O	LO,FS,MDP	$500-$8,000	DS
Cadence Design Systems Inc. 555 River Oaks Pkwy. San Jose, CA 95134 (408) 943-1234 CIRCLE 607	Programmable Logic Design System (PLDS)	U	L,S,B,SM	N,J,O	LO,FS,MDP,ADS	$12,000-$15,000	NDS
Capilano Computing 1168 Hamilton St. Vancouver, B.C. Canada V6B 2S2 (604) 669-6343 CIRCLE 608	MacAbel	M	L,B,SM,TT,O	J,O	LO,FS,ADS	$1,995-$3,995	NDS
Cypress Semiconductor 3901 N. First St. San Jose, CA 95134 (408) 943-2600 CIRCLE 609	Warp1	D	L,B,SM,TT	J	LO,FS	$195	DS
	PLD Toolkit	D	L	J	FS	$95	DS
	Max+Plus	D	L,S,B,SM,TT	O	LO,FS,ADS	$3,995	DS
	Max+Plus II	D	L,S,W,B,SM,TT,O	N,O	LO,FS,MDP,ADS	$9,995	DS
Data I/O Corp. 10525 Willows Rd. N.E. Redmond, WA 98073 (206) 881-6444 CIRCLE 610	Abel	D,M,U	L,S,B,SM,TT,O	N,J,O	LO,FS,MDP,ADS	$495-$9,995	NDS
Dazix, an Intergraph Co. One Madison Industrial Park Huntsville, AL 35894-0001 (205) 730-8502 CIRCLE 611	Abel FPGA	U	L,S,B,SM,TT,O	N,J	LO,FS,MDP,ADS	$5,000+	NDS
Exemplar Logic Inc. 2550 Ninth St., Suite 102 Berkeley, CA 94710 (800) 552-3742 CIRCLE 612	Exemplar Logic Synthesis System	D,U	L,S,W,B,SM,TT	N,O	LO	$2,000-$24,000	NDS

Key: D=DOS; M=Macintosh; U=Unix
L=Language; S=Schematic; W=Waveform; B=Boolean; SM=State machine; TT=Truth table; O=Other
N=Net list; J=JEDEC; O=Other
LO=Logic optimization; FS=Functional simulation; MDP=Multiple device partitioning; ADS=Automatic device selection
DS=Device-specific tools (specific to the company); NDS=Non-device-specific tools (universal tools)

▼ BETTER PLD TOOLS CUT DESIGN TIME

Major enhancements to Signetics' Snap PLD design tools cut development time, improve testability, and boost the performance of low- and medium-density Signetics PLD designs. Snap version 1.6 includes a fault simulator, a logic optimizer, a Boolean-equation extractor, a friendly user interface, and new documentation. The tool accepts waveforms, Boolean equations, and state equations as input. It also takes Orcad and Futurenet schematics. Snap then merges these inputs, synthesizes a net list from the result, and performs functional and fault simulation. Accurate gate-level simulation allows for precise timing and performance analysis, as well as internal node tracing prior to selecting a logic device for programming. The functional and fault simulator generates a report listing all undetected or potentially undetected faults and coverage efficiency. Snap version 1.6 runs on personal computers. It's shipping now for $795.

Signetics Co., a div. of North American Philips Corp.
811 E. Arques Ave.
P.O. Box 3409
Sunnyvale, CA 94088-3409
(408) 991-2000
▶ CIRCLE 633

PROGRAMMABLE LOGIC DESIGN TOOLS

Company	Product	Platform	Design entry	Output	Features	Price	Type
GEC Plessey 1500 Green Hills Rd. Scotts Valley, CA 95066 (408) 438-2900 CIRCLE 613	ERA Design Kit	D	S	N	FS	$2,990-$4,995	DS
Gould AMI 2300 Buckskin Rd. Pocatello, ID 83201 (208) 234-6668 CIRCLE 614	Place	D	B,SM,O	J	LO,FS	$695	DS
	APEEL	D	B	J	LO,FS	Free	DS
Intel Corp. 1900 Prairie City Rd. Folsom, CA 95630 (800) 548-4725 CIRCLE 615	PLDshell	D	B,SM,TT	J	LO,FS	Free	DS
ISDATA Inc. 800 Airport Rd. Monterey, CA 93940 (800) 777-1202 CIRCLE 616	LOG/ic	D,U	L,S,B,SM,TT	J,O	LO,FS,MDP,ADS	$1,480-$9,000	NDS
Lattice Semiconductor Corp. 5555 N.E. Moore Ct. Hillsboro, OR 97124 (503) 681-0118 CIRCLE 617	pLSI Development System	D	B	J	LO,FS	<$1,000	DS
	pLSI Development System Plus	D,U	S,B	N,J	LO,FS	<$5,000	DS
Logical Devices Inc. 1201 N.W. 65th Pl. Ft. Lauderdale, FL 33309 (305) 974-0967 CIRCLE 618	CupL	D,M,U	L,S,B,SM,TT	N,J,O	LO,FS,MDP,ADS	$49-$2,295	NDS
	CupL Integrated Synthesis Tools	D,U	L,S,W,B,SM,TT,O	N,J,O	LO,FS,MDP,ADS	$2,295-$2,795	NDS
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070 (503) 685-7000 CIRCLE 619	PLDSynthesis	U	L,S,B,SM,TT	N,J,O	LO,FS,MDP,ADS	$14,900	NDS
	AutoLogic FPGA	U	L,S,B,SM,TT,O	N,O	LO,FS	$34,900	NDS
MINC Inc. 6755 Earl Dr. Colorado Springs, CO 80918 (719) 590-1155 CIRCLE 620	PLDesigner	D,U	L,S,W,B,SM,TT,O	N,J,O	LO,FS,MDP,ADS	$1,995+	NDS
	PGADesigner	D,U	L,S,W,B,SM,TT,O	N,J,O	LO,FS,MDP,ADS	$2,500+	NDS
National Semiconductor Corp. 2900 Semiconductor Dr. Santa Clara, CA 95052 (800) 272-9959 CIRCLE 621	Opal	D,U	B,SM,TT	J	LD,FS	$495+	DS
	Opal Jr.	D	B	J		Free	DS
Omation Inc. 801 Presidential Dr. Richardson, TX 75081 (800) 553-9119 CIRCLE 622	Schema PLD	D	S,B,SM,TT	J	LO	$495	NDS

Key: D=DOS; M=Macintosh; U=Unix
L=Language; S=Schematic; W=Waveform; B=Boolean; SM=State machine; TT=Truth table; O=Other
N=Net list; J=JEDEC; O=Other
LO=Logic optimization; FS=Functional simulation; MDP=Multiple device partitioning; ADS=Automatic device selection
DS=Device-specific tools (specific to the company); NDS=Non-device-specific tools (universal tools)

▼ SOFTWARE TURNS OUT PLDs IN HOURS

Users are able to turn out PLDs within their first few hours using the Slice PLD tools from Signetics. The package was designed so that users could rapidly produce a functioning PLD design without going through the time-consuming learning curve that accompanies most other tools.

The Slice environment is fully menu driven, and reduces the PLD design process to a series of simple steps. To use the tool, engineers simply select the target PLD and assign input and output pins. They then enter equations in either Boolean or state form, and finally download the JEDEC fuse map generated by Slice to the programmer. Slice runs on personal computers, and is available free of charge to qualified Signetics PLD customers.

Signetics Co., a div. of North American Philips Corp.
811 E. Arques Ave.
P.O. Box 3409
Sunnyvale, CA 94088-3409
(408) 991-2000
▶ CIRCLE 634

PROGRAMMABLE LOGIC DESIGN TOOLS

Company	Product	Platform	Design entry	Output	Features	Price	Type
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881 CIRCLE 623	Release IV Programmable Logic Design Tools	D,U	L,S,W,B,SM,TT	N,J,O	LO,FS	$495-$1,495	NDS
Plus Logic Inc. 1255 Parkmoor Ave. San Jose, CA 95126 (408) 298-7587 CIRCLE 624	Plustran	D	S,B	J,O	LO	$475-$975	DS
ProLogic Systems 557-O Burbank St. Broomfield, CO 80020 (303) 460-0103 CIRCLE 625	ProLogic V3.0	D	L,B,SM,TT	J	LO,FS	$100-$250	NDS
QuickLogic Corp. 2933 Bunker Hill Ln. Santa Clara, CA 95054 (408) 987-2000 CIRCLE 626	pASIC Toolkit	D	S,B	O	LO,FS	$3,995	DS
Signetics Co., a div. of North American Philips Corp. 811 E. Arques Ave. Sunnyvale, CA 94088-3409 (408) 991-2000 CIRCLE 627	Snap	D	L,S,W,B,SM,TT	N,J	LO,FS	$795	DS
	Slice	D	B,SM	N,J	LO	Free	DS
Teradyne EDA, Teradyne Inc. 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 CIRCLE 628	MultiSim Interactive Designer for Programmable Logic	U	L,S,W,B,SM,TT	N,J	LO,FS,MDP,ADS	$29,500+	NDS
Texas Instruments Inc. P.O. Box 655012 M/S 57 Dallas, TX 75265 (214) 995-6611 CIRCLE 629	LogicEnhancer/ Synthesizer Tool	D	B,SM,TT	N	LO	$950-$1,500	DS
	Action Logic System	D	S	N		$4,000-$14,000	DS
	ProLogic V2.0	D	L,B,SM,TT	J	LO,FS	Free	DS
Valid Logic Systems Inc. 2820 Orchard Pkwy. San Jose, CA 95134 (408) 432-9400 CIRCLE 630	SystemPLD/ SystemPGA	U	L,S,W,B,SM,TT,O	N,J,O	LO,FS,MDP,ADS	$13,500+	NDS
Viewlogic Systems Inc. 293 Boston Post Rd. Marlboro, MA 01752 (508) 480-0882 CIRCLE 631	View PLD	D,U	L,O	N,O	LO,FS,MDP,ADS	$7,500-$15,000	NDS
	Retargeter	D,U	L,S,O	N	LO,FS	$30,000 (Unix)	NDS
Xilinx Inc. 2100 Logic Dr. San Jose, CA 95124 (408) 559-7778 CIRCLE 632	XACT Development System	D,U	L,S,W,B,SM,TT	N,O	LO,FS,ADS	$995-$13,450	DS

Key: D=DOS; M=Macintosh; U=Unix
L=Language; S=Schematic; W=Waveform; B=Boolean; SM=State machine; TT=Truth table; O=Other
N=Net list; J=JEDEC; O=Other
LO=Logic optimization; FS=Functional simulation; MDP=Multiple device partitioning; ADS=Automatic device selection
DS=Device-specific tools (specific to the company); NDS=Non-device-specific tools (universal tools)

▼ TOOLKIT SPEEDS FPGA SIMULATIONS

Thanks to library support for the Xilinx FPGA families, engineers can now use Ikos' simulation accelerators to simulate systems containing FPGAs. The Xilinx Toolkit for Ikos simulations provides Xilinx FPGA libraries and an interface to the Xilinx XACT design system for net-list translation. Ikos simulation systems include software and a parallel, highly pipelined hardware architecture to perform logic and fault simulation of as many as 1.2 million gates. Engineers can choose pre- and post-layout simulation, as well as functional or timing simulation paths. A post-layout Xilinx Net list (XNF) generated by the Xilinx XACT system can be input to the Ikos translator to create net-list and timing files for the Ikos processor. The Xilinx Toolkit is available now for $7500, and runs on Apollo or Sun workstations.

Ikos Systems Inc.
145 N. Wolfe Rd.
Sunnyvale, CA 94086
(408) 245-1900
▶ CIRCLE 635

▼ CREATE PLDs ON YOUR MACINTOSH

Capilano's Apple Macintosh-based MacAbel 4.0 programmable logic design system is now shipping. MacAbel 4.0 is based on the Abel-4 design system from Data I/O Corp. The new release includes increased device coverage, new features for device-independent design, and the new Open-Abel modular device support. Also, users can integrate PLD designs with a complete system design entered in the company's DesignWorks schematic-capture and simulation package. A series of enhancement modules will be released over the next few months, including a DevSel device-selector module that assists users in selecting the right part for a given application. In addition, fitter modules will help users take advantage of specific PLD features. Call for pricing.

Capilano Computing Systems Ltd.
501-1168 Hamilton St.
Vancouver, B.C.
Canada V6B 2S2
(604) 669-6343
▶ CIRCLE 636

▼ PLD TOOL RUNS IN A GRAPHICAL SHELL

The Opal software package is a PC-based PLD development tool that accepts state-machine, truth-table, and Boolean-equation entry. It performs optimization, verification, and implementation in a wide range of National Semiconductor PLDs. The software package consists of a graphical shell environment, executable modules, a graphical simulation package, a device library, examples, and an overall demonstration of the tool. Because Opal is an open-architecture language, the modules can communicate with third-party software. Engineers can create designs by starting new files, or by modifying the example files. Opal is available now, starting at $495. A subset of the complete Opal environment, called Opaljr, is available free of charge. Opaljr contains five Opal demonstrations and can be used as equation-entry PAL/GAL design software. Users can create Boolean descriptions and translate them to JEDEC files in a PAL or GAL format.

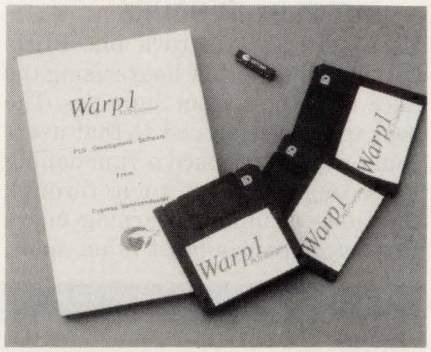
National Semiconductor Corp.
2900 Semiconductor Dr.
M/S 16-177, P.O. Box 58090
Santa Clara, CA 95052-8090
(800) 272-9959
▶ CIRCLE 637

▼ PLD TOOLS AT AN AFFORDABLE PRICE

Engineers can design PLDs without breaking their budget with ProLogic Version 3.0, priced at $249.95. ProLogic is a PLD compiler that accepts Boolean-equation, truth-table, and state-machine design inputs to create a standard JEDEC fuse map. The design can then be tested with the built-in simulator prior to committing to device programming. The ProLogic software was designed for ease of use. It is distributed by Texas Instruments, but this release supports many additional devices from a variety of manufacturers. ProLogic Version 3.0 runs on PCs and is shipping now. The software costs on $199.95 when purchased with the company's PLD programmer.

ProLogic Systems
557-O Burbank St.
Broomfield, CO 80020
(303) 460-0103
▶ CIRCLE 638

▼ VHDL COMPILER CREATES PLDs



Warp1, the first VHDL compiler for PLDs, helps users create designs for the Cypress CY7C361 with state machines described in a high-level language. The Warp1 software optimizes at both the state and logic levels, and performs final placement and routing. In addition, it provides a state-machine syntax that helps users describe their concepts in VHDL, even when the concepts involve concurrency. Optimization is done in two passes. Warp1 is only the first element of a tool chain. It creates an assembly language file that's used by the Cypress PLD Toolkit. Warp1 and the Cypress PLD Toolkit run on a personal computer. Pricing for the bundled software is $195.

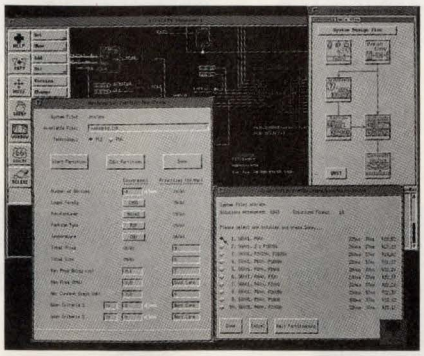
Cypress Semiconductor Corp.
3901 N. First St.
San Jose, CA 95134-1599
(408) 943-2600
▶ CIRCLE 639

▼ FPGA TOOLS MESH WITH SIMULATOR

Teradyne is offering FPGA design tools that are tightly integrated with the company's MultiSim interactive simulator. The MultiSim Interactive Designer for Programmable Logic (MSID/PL) combines the synthesis technology from MINC's PGADesigner tool with Teradyne's simulation technology. The composite environment supports the design process from entry through post-layout, board-level simulation. Design kits are currently available for Actel, Altera, and Xilinx devices. Pricing for the workstation-based MSID/PL starts at $29,500.

Teradyne Inc.
321 Harrison Ave.
Boston, MA 02118
(617)482-2700
▶ CIRCLE 640

▼ UPGRADE EASES PLD, FPGA DESIGN



Version 2.0 of Valid's SystemPLD/SystemPGA design software features a new user interface, support for more devices, and improved delays for more accurate simulation. In addition, the tools have automatic de-Morganization to optimize users' design descriptions for best utilization of the target device's features. The newly incorporated ValidFrame user interface, which is based on the X-Windows Motif standard, boasts many ease-of-use features. For instance, a design-process-diagram walks users through each step in the design flow, from set-up and design entry through simulation and device synthesis. At each step in the process, users simply click on an icon to perform the desired task. Version 2.0 of the SystemPLD and SystemPGA software is available now for DEC, IBM, and Sun workstations. Pricing for SystemPLD/SystemPGA starts at $13,500.

Valid Logic Systems Inc.
2820 Orchard Pkwy.
San Jose, CA 95134
(408) 432-9400
▶ **CIRCLE 641**

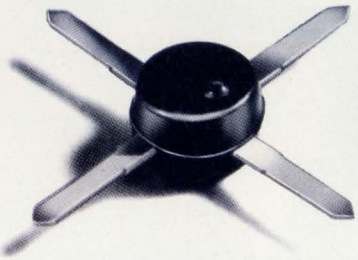
▼ DEVICE FITTER TARGETS MACH LOGIC

Engineers using Data I/O's Abel design software can now target AMD's MACH family of CMOS programmable logic. A new device fitter, which is based on proprietary Data I/O technology, lets users compile and simulate designs aimed at MACH devices. It uses a Mincut and Bin Packing technique to partition logic across the multiple blocks of the MACH architecture. This minimizes routing between the blocks and ensures high utilization within the blocks. Once partitioned, Placement and Routing routines assign logic to a macrocell, and route the signals between the blocks. A ripup-and-retry mode is invoked if a signal can't be placed or routed based on the initial partitioning. Routing and product-term steering algorithms look-ahead as many levels as required to ensure optimum distribution. The MACH fitter is available now for $495. It works with the Abel-4 and Abel-FPGA design systems running on personal computers and Sun workstations.

Data I/O Corp.
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
▶ **CIRCLE 642**

99¢

from



dc to 2000 MHz amplifier series

SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	•MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.
• 1dB Gain Compression
□ +4dBm 1 to 2 GHz

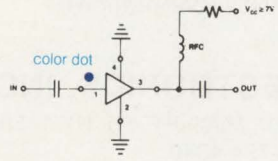
Unbelievable, until now…tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

designers amplifier kit, DAK-2

5 of each model, total 35 amplifiers

only $59.95



Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 220, 470, 680, 1000 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047. .068, .1μf

† Minimum Order 50 per Value

☐ Designers kit, KCAP-1, 50 pieces of each capacitor value, only $99.95

finding new ways...
setting higher standards

Mini-Circuits

A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156

CIRCLE 132 FOR U.S. RESPONSE

CIRCLE 133 FOR RESPONSE OUTSIDE THE U.S.

C113-Rev. D

CIRCLE 521

CIRCUIT PASSES ONLY HIGH-SPEED DATA

IVO SEKSO-TELENTO
University of Zagreb, 41000 Zagreb, Kolarova 18/I, Yugoslavia;
Tel: 38-41-629-999, Fax: 38-41-611-396.

Serial data communications lines sometimes carry a mixture of narrowband and wideband information *(Fig. 1, top line)*. If it's desirable to use the wideband signal and ignore the lower-speed component—to extract a clock, for example—a simple one-shot circuit can do the job *(Fig. 2)*.

The circuit is essentially a timed gate that opens when the high-frequency signal is present, and stays closed at all other times. The gate is controlled by a pair of one-shots whose on-time (t_{os}) is chosen to be greater than the period of the high-frequency signal but shorter than half the period of the low-frequency one.

The gate passes the input signal only while both one-shots are on—while both of their outputs are low. At all other times, the output of the OR gate simply stays high. The one-shots are retriggerable so their outputs stay low and the gate stays open continuously as long as the high-frequency input is present.

Gate IC_2 can be realized in a number of ways. One of the simplest is as a combination of 74LS32 quad two-input OR gates.

If the high-frequency signal has a frequency f_H (with a corresponding period T_H) and the low-frequency signal has a frequency f_L (with a corresponding period T_L), then the condition for passing the higher frequency and suppressing the lower one is:

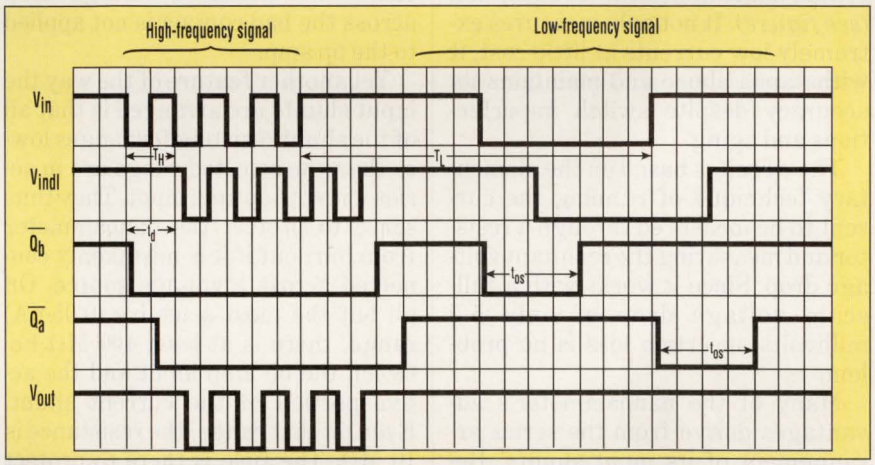
$$T_H < t_{os} < T_L/2.$$

Frequencies between f_L and f_H are not permitted.

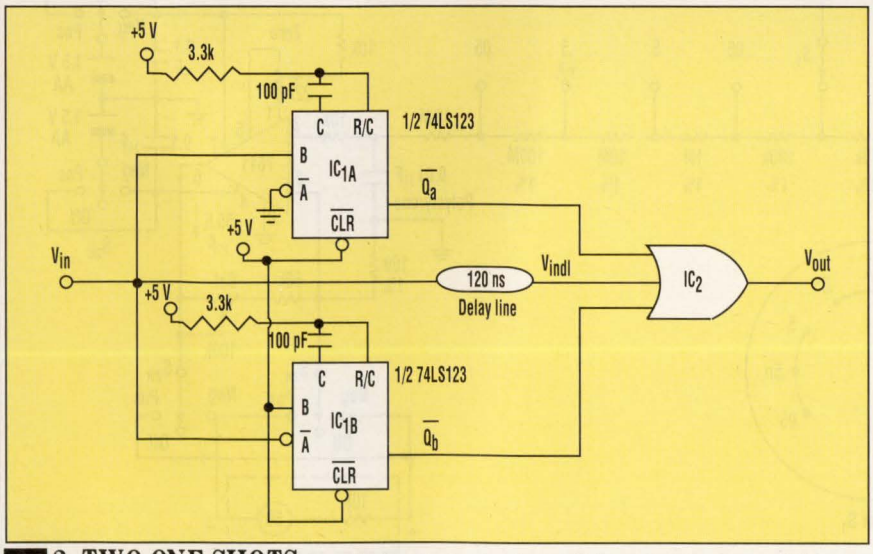
The delay line introduces a small fixed delay, t_d, into the main signal path to give the one-shots time to change state. Doing so ensures that the one-shot propagation delay time, t_p, does not cause the first bit in the data stream to be lost. The condition for saving the first bit is:

$$(T_{os} - T_H/2) > t_d > (T_H/2 + t_p).$$

Because component tolerances and variations in the frequency of the input signal can affect circuit operation by causing a frequency to fall into the forbidden region, it is best to allow generous margins when configuring a system. The circuit of Figure 2, for example, is designed for a maximum T_H value of 125 ns, a minimum T_L value of 500 ns, a t_{os} of 200 ns, and a t_d of 120 ns. It is thus rated to pass all frequencies above 8 MHz and to block all frequencies below about 2 MHz with comfortable margins. For the numbers in the example, the condition on T_H and T_L (first inequality) becomes: 125 ns < 200 ns < 250 ns.□



1. SERIAL BIT STREAMS often contain a mixture of high- and low-frequency components (V_{in}). A gate controlled by signals $\overline{Q_b}$ and $\overline{Q_a}$ can suppress the low-frequency signal, leaving just the high-speed data out.



2. TWO ONE-SHOTS form the heart of a simple circuit for extracting fast-switching signals from a serial bit stream. When built with the component values shown, the circuit will pass all frequencies above 8 MHz and block those below about 2 MHz.

CIRCLE 522

NANOAMMETER IS RUGGED

M.J. SALVATI
Flushing Communications, 150-46 35th Avenue,
Flushing, NY 11354; (718) 358-0932.

Sensitive measuring instruments aren't generally known for their ruggedness. When subject to abuse or the inevitable ravages of time, they tend to lose accuracy or even to cease working altogether. This battery-operated nanoammeter is an exception *(see figure)*. It not only measures extremely low currents at little cost, it withstands abuse and maintains its accuracy despite switch imperfections and aging.

The circuit is based on the elementary technique of running the current to be measured through a resistor and measuring the resultant voltage drop. Since it works with a full-scale voltage drop of only 5.5 millivolts, insertion loss is no problem.

Many of the nanoammeter's advantages derive from the series arrangement of its input shunts. Because of that arrangement, a momentary loss of contact in the range switch (caused by dirt, aging, range switching, etc.) does not open the op amp input; hence, it will not lead to pegging the meter. Similarly, poor switch contact resistance does not affect measurement accuracy because the increased voltage drop across the bad contact is not applied to the op amp.

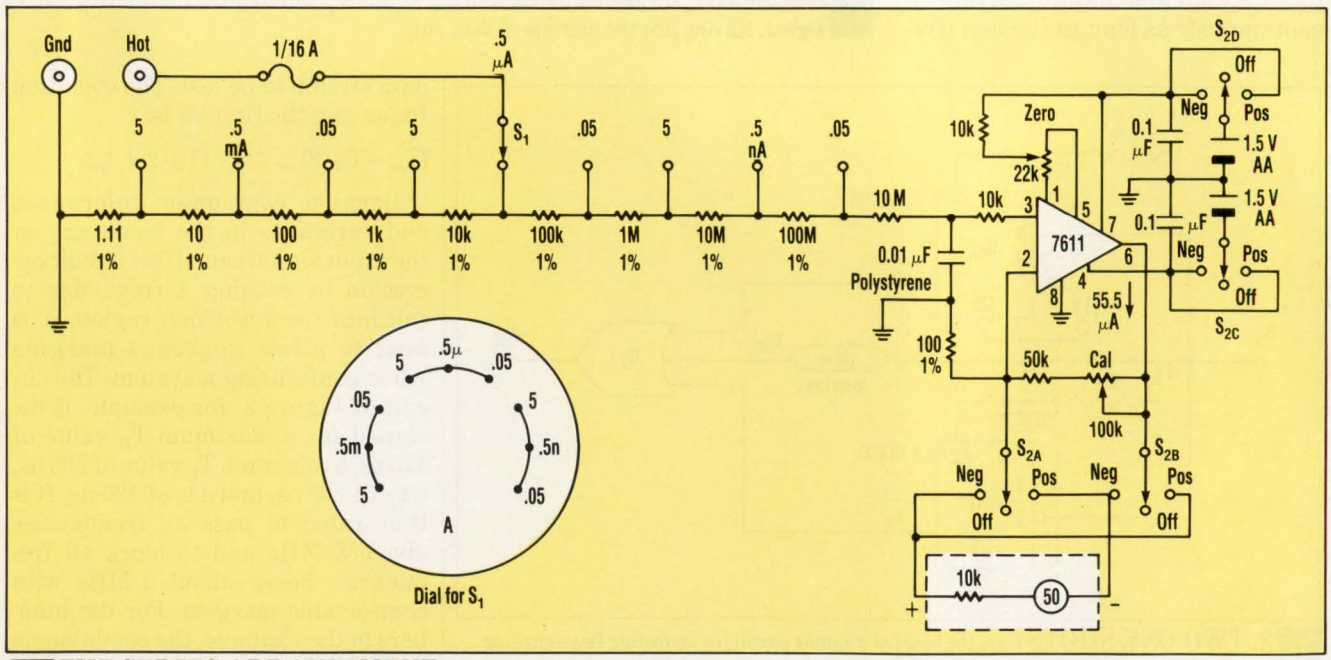
Yet another feature of the way the input shunts are arranged is that all of the shunt resistors for ranges lower than the selected range are in series with the op amp input. They thus serve to protect the nanoammeter from burnout if it is mistakenly connected across a voltage source. On all but the most sensitive (0.05-nA) range, there is at least 100 MΩ between the op amp input and the active portion of the current shunt. Even on that range, the resistance is 10 MΩ. The fuse is there to protect the low-value *resistors*.

Send in Your Ideas for Design
Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

Because of the resistor in series with the 50-μA meter movement, the op amp output at full scale is 0.5 V. Since the supply voltage is 1.5 V, the maximum possible meter current is limited to triple its full-scale value. Consequently, the meter won't be damaged by voltage or current overload.

Further contributing to the instrument's robustness is the location of the calibrating pot. Placing it across the meter-resistor combination, rather than across the meter alone, allows it to have a high resistance value. Since the wiper contact resistance is small with respect to the calibrating resistance itself, changes in contact resistance with age will have little effect on the meter calibration.

The only caveat in building this circuit is to be sure that the switch, circuit board, and input filter capacitor have extremely high insulation resistances.□



THE SERIES ARRANGEMENT of its input shunts contributes to the ruggedness of this low-cost nanoammeter. It protects the meter against both overloads and switching transients.

CIRCLE 523

GET ±15-V SQUARE WAVES FROM +5 V

V. LAKSHMINARAYANAN
Centre For Development of Telematics, Sneha Complex, 71/1 Miller Rd., Bangalore - 560 052, India; tel. 91-812-27890, or fax 91-812-74856.

This low-cost circuit should prove useful when bipolar square waves are needed and only 5-V system power is available. It's much less expensive than the more obvious expedient of buying a dual-output dc-dc converter. Although this implementation generates ±15-V square waves, slight modifications, such as using different zeners, can be made to yield other voltages. The heart of the circuit is a 556 dual timer, half configured as a variable-frequency astable multivibrator (A) and the other as a dc-dc converter (B) *(see the figure)*.

The output of the 556's "B" half is a 100-kHz signal that drives transistor Q. Because the collector load on Q is the primary of a 1-mH pulse transformer, the switching of the collector current generates a train of voltage spikes (about four times the supply voltage, or around 20 V in this case) at the collector of Q. The spikes are rectified by diode D_2, filtered by the 20-μF capacitor, and regulated by a 15-V Zener diode to yield a +15-V supply rail. In a similar fashion, the output of the transformer secondary is rectified by D_1 and used to form a –15-V rail.

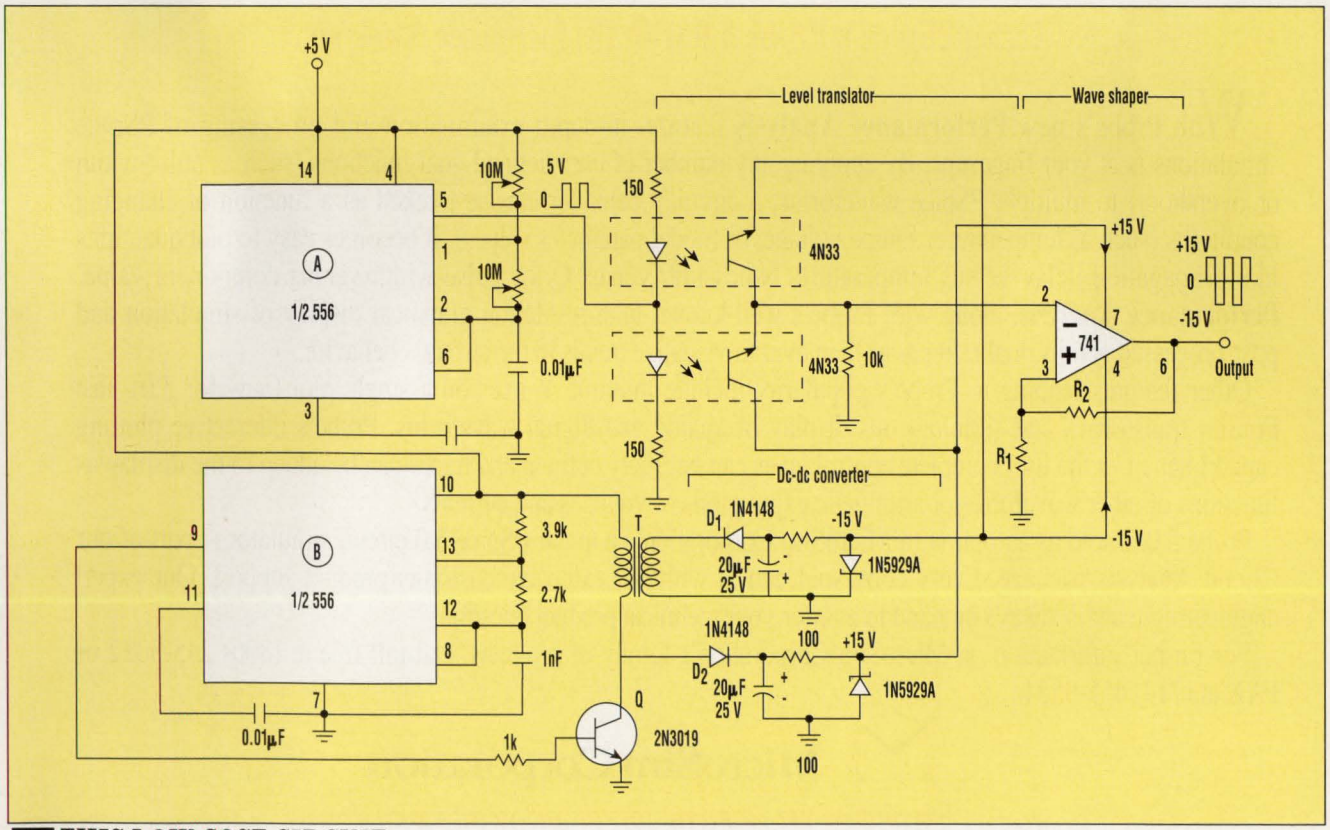
With the ±15-V rails established, they can be used to power the output transistors in a pair of 4N33 optocouplers, whose inputs are driven by the "A" half of the 556. As the diagram shows, the common output of the 4N33s is terminated by a 10k load and fed through a wave shaper to form the output of the generator. The wave shaper is a Schmitt trigger circuit based on an op amp.

The generator output is a bipolar pulse train with a peak-to-peak swing of 30 V. Its frequency and duty cycle can be varied by adjusting the two 10-MΩ pots on astable multivibrator "A." The circuit thus serves as a variable-frequency square-wave generator with a variable pulse width.□

IFD WINNER

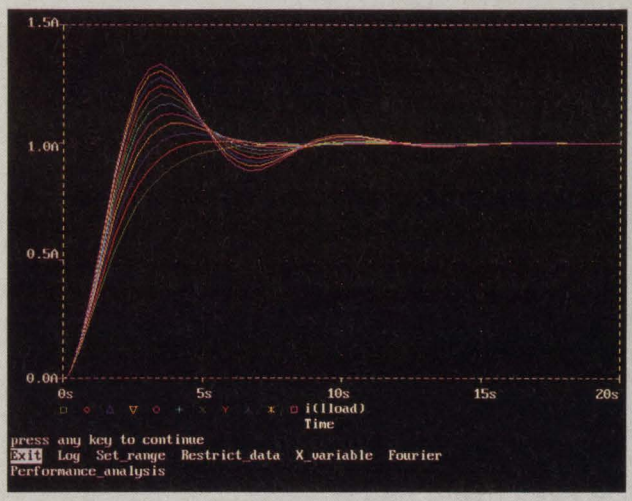
IFD Winner for June 13, 1991

Yongping Xia, West Virginia University, Dept. of Electrical and Computer Engineering, Morgantown, WV 26506. His idea: *"Circuit Converts Period to Voltage."*

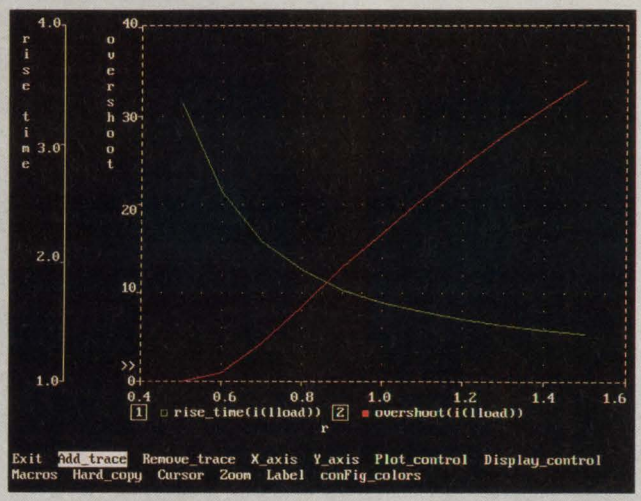


THIS LOW-COST CIRCUIT, based on a 556 dual timer, generates variable-frequency ±15-V square waves with variable duty cycle from a single +5-V supply. The "B" half of the 556 acts as a dc-dc converter, and the "A" half functions as an astable multivibrator.

We Deliver Answers



Current through an inductor with stepped resistance



Rise time and overshoot as a function of resistance

Explore the Intricacies of Your Circuit Design...

Using PSpice's Probe 5.0 with Performance Analysis

With Probe's new **Performance Analysis** feature, in-depth examination and processing of PSpice simulations is at your fingertips. By applying any number of user-defined goal functions (such as pulse-width or overshoot) to multiple PSpice waveforms, a circuit's behavior can be tracked as a function of changing conditions (such as temperature, source voltage, or model parameter values). It becomes easy to plot quantities like propagation delay versus temperature, bandwidth versus Q, or pulse-width versus component value. **Performance Analysis**, along with Probe's well-known high-resolution graphical display of simulation and post-processed results, makes it easier than ever to visualize trends in the circuit's behavior.

Other features lending to Probe's popularity include multiple Y axes on a single plot (new for 5.0), fast Fourier transforms, and simultaneous display of analog and digital waveforms. Probe's interactive plotting capabilities offer the user complete control; axes can be freely defined and traces can be added to the display as functions of other waveforms or arithmetic expressions of voltages and currents.

Probe 5.0 is sold as an option to MicroSim Corporation's popular PSpice 5.0 circuit simulator— part of our Circuit Analysis package. Every copy sold comes with our extensive customer/product support. Our expert engineering team is always on hand to answer your technical product questions.

For further information on MicroSim Corporation's family of products, call toll free at (800) 245-3022 or FAX at (714) 455-0554.

MicroSim Corporation

Expanding the Standard for Circuit Simulation

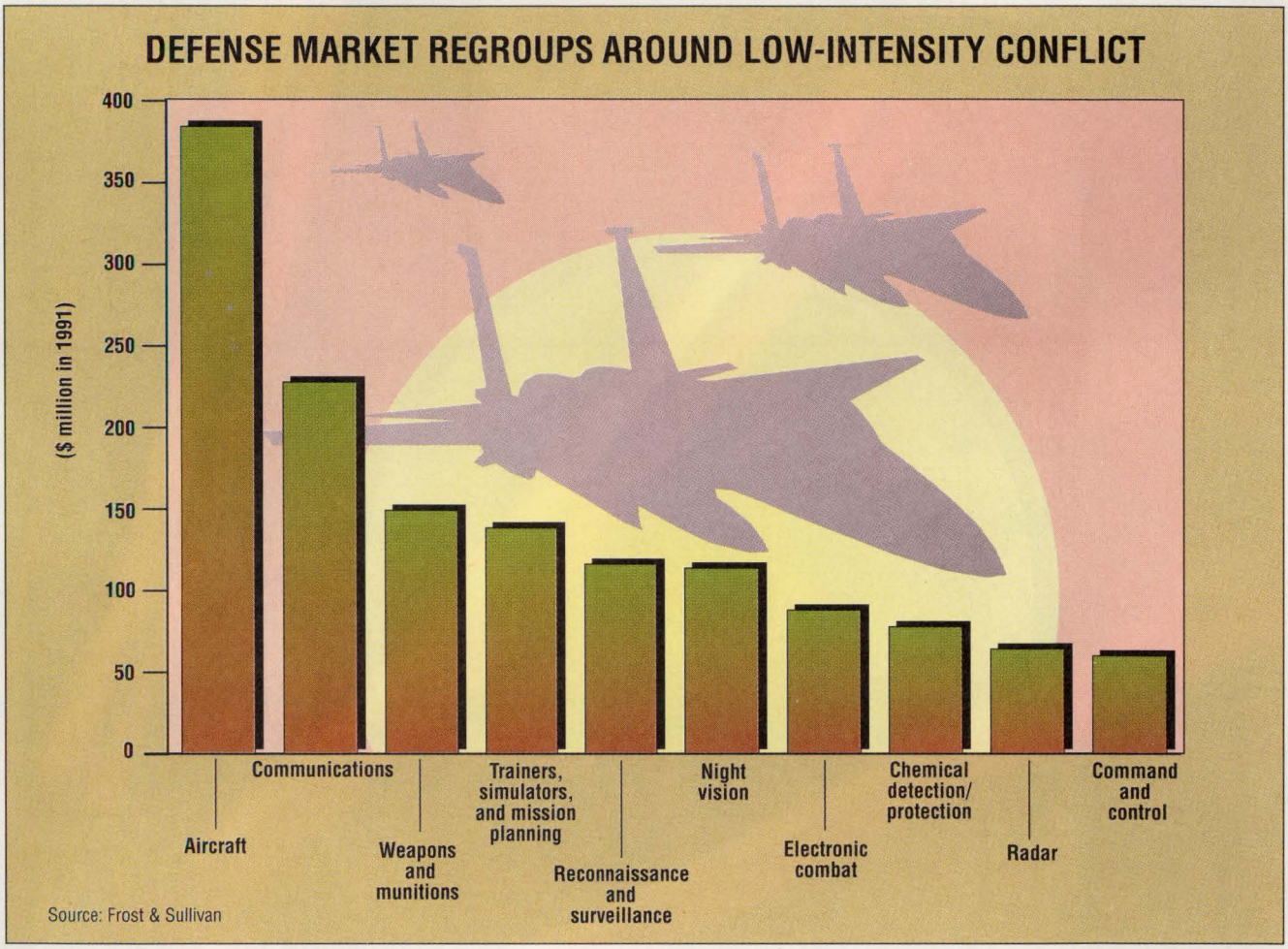
20 Fairbanks • Irvine, California 92718 USA

CIRCLE 122 FOR U.S. RESPONSE **CIRCLE 123 FOR RESPONSE OUTSIDE THE U.S.**

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE



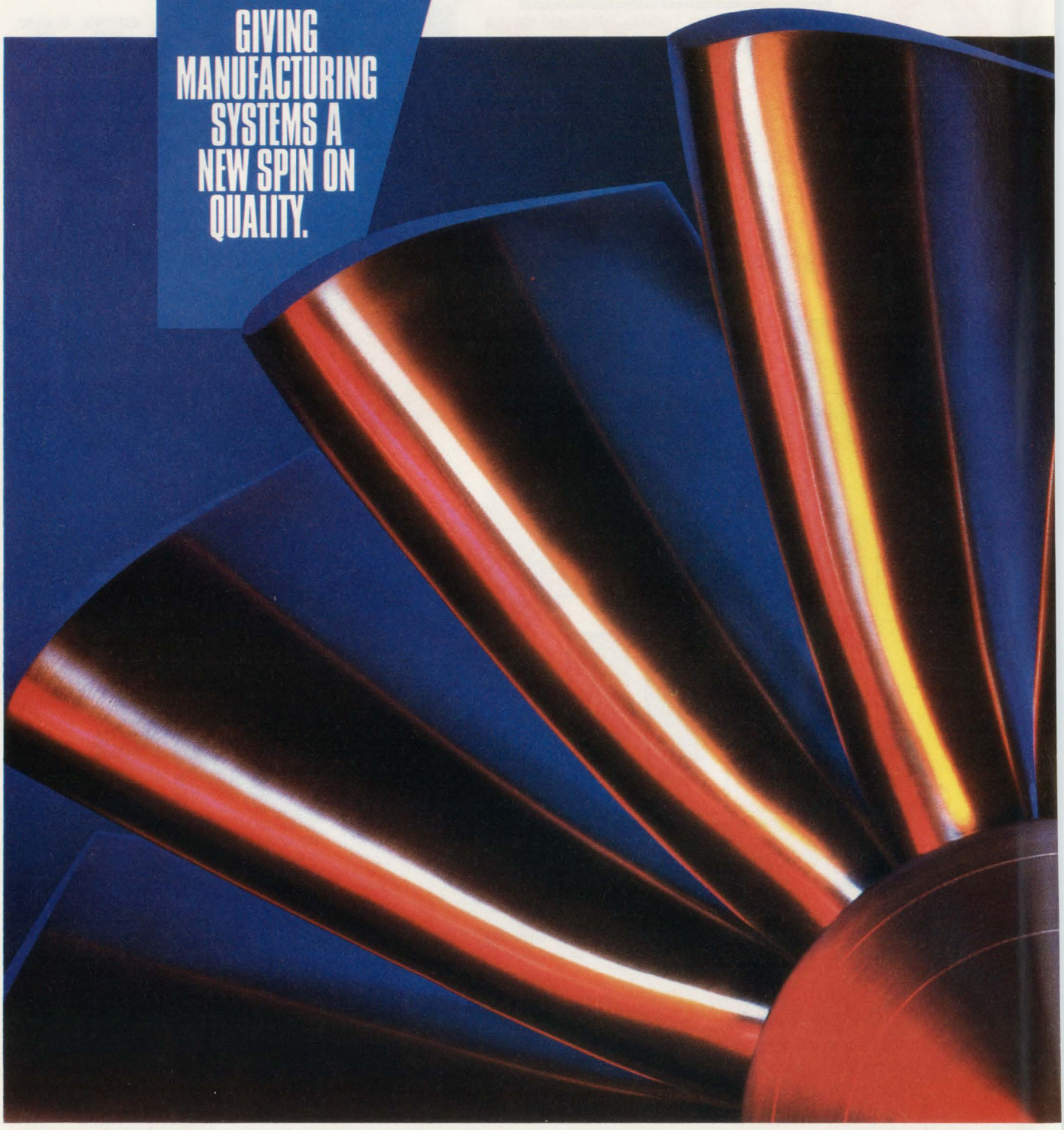
MARKET FACTS

On the heels of the Persian Gulf War, the splitting of the Eastern bloc, and the unraveling of the U.S.S.R., the U. S. Department of Defense is adjusting its procurement strategy. The Defense Department will emphasize handling the threat of smaller, regional conflicts—what is known in defense circles as low-intensity conflict, or LIC. From 1990 to 1996, the DOD will spend $12.3 billion to respond to threats quickly with lighter, mobile, more lethal forces reinforced with firepower and supported by a logistics lifeline, according to Frost & Sullivan Inc.

The New York market researchers predict that annual spending for LIC will increase from $1.42 billion this year to reach $1.91 billion by 1996. Already U. S. companies are developing technologies for LIC aircraft, communications equipment, trainers and simulators, along with weapons and munitions.

Procurement for LIC will show the most activity, with spending increasing from $1 billion in 1991 to $1.5 billion by 1996. In contrast, research, development, testing, and evaluation will move up from $387 million to $417 million in the same period. The Army will be the biggest customer for LIC gear, spending more than half a billion dollars this year or one-third of the LIC market.

Next in line is the Special Operations Command, which supports the war on drugs, such as training Drug Enforcement Administration agents. The command is homing in on communications systems. The Air Force is expected to spend $255 million this year, which should increase to $386 million by 1996. The Marine Corps will spend $115 million in 1991 and $178 million by 1996. The Navy, which has earmarked $74 million this year for LIC, is expected to spend $126 million by 1996. Aircraft and communications will account for the biggest volumes, followed by trainers, simulators, and mission planning. Biggest contract winners last year were Rockwell, Boeing, and Lockheed.



SIGNAL PROCESSING AND

POWER CONTROL FROM HARRIS.

CIRCLE 211 FOR U.S. RESPONSE

CIRCLE 212 FOR RESPONSE OUTSIDE THE U.S.

QUICKLOOK

OFFERS YOU CAN'T REFUSE

Sun Microsystems is offering free seminars on Unix System V Release 4, commercial software development, multiprocessing, relational database management, and network technologies this month and next in the northeastern U. S. Sites range from Lincoln, Mass. to Somerset, N. J. For more information on dates and sites, or to register, call (800) 423-6936.

MagneTek has free switch mode magnetic sample kits for EMI suppression inductors, gate drive transformers, current sense inductors, and rod core output filter inductors. The company's literature has specification charts and schematics are given for common mode EMI suppression inductors (with E-core construction or toroidal construction); gate drive transformers; current sense inductors; and output filter inductors. The literature also gives custom details about converter power transformers and mag amp inductors.

Contact MagneTek Inc., 1124 E. Franklin St., Huntington, IN 46750; (219) 356-7100; fax (219) 356-0311. CIRCLE 451

Write for a free user's guide to NIST. The guide lists research opportunities, facilities, and services of the National Institute of Standards and Technology. It summarizes NIST research programs that could become the basis for cooperative R&D agreements with industry.

The guide also describes the standards institute's research facilities for industrial use and details the institute's services to industry. Names of project managers and phone numbers are listed as well.

Copies of *Research, Services, Facilities* are available with a self-addressed mailing label from the NIST Public Affairs Division, A903 Administration Bldg., NIST, Gaithersburg, MD 20899; fax (301) 926-1630.

An evaluation package is free for CODAS, a recording system for waveforms for the IBM PC AT, PS/2 Micro Channel, or compatibles. CODAS, from Dataq Systems, delivers instant waveform monitoring of every data point as it happens, recording to disk up to 16 waveforms at up to 50,000 samples/s.

Contact Dataq Instruments Inc., 825 Sweitzer Ave., Akron, OH 44311; (800) 553-9006 or (216) 434-4284. CIRCLE 452

QUICK REVIEWS

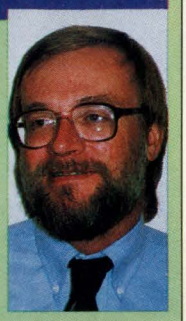
If you like the Pease Porridge column, you'll love Bob's book, *Troubleshooting Analog Circuits*. Here's a chance to take advantage of his years of experience designing analog circuits—and working the bugs out of them. This book is for you whether you're designing analog circuits at the board, box, system, or IC level. It's for technicians working alongside a designer, student EEs, and teachers of analog design. Even one bug-finding technique recovered from the book more than pays for it. But the best part may just be in the reading—its pure Pease. Never before has such potentially dry material been so much fun to peruse—you may have to keep it locked in your desk except when in use.

The 208-page, hard-cover book lists for $32.95 and is published by Butterworth-Heinemann, 80 Montvale Ave., Stoneham, MA 02180; (800) 366-2665. Or mail $35.95 (includes tax and shipping) to Robert Pease, 682 Miramar Ave., San Francisco, CA 94112-1232.

Frank Goodenough

KMET'S KORNER

...Perspectives on Time-to-Market

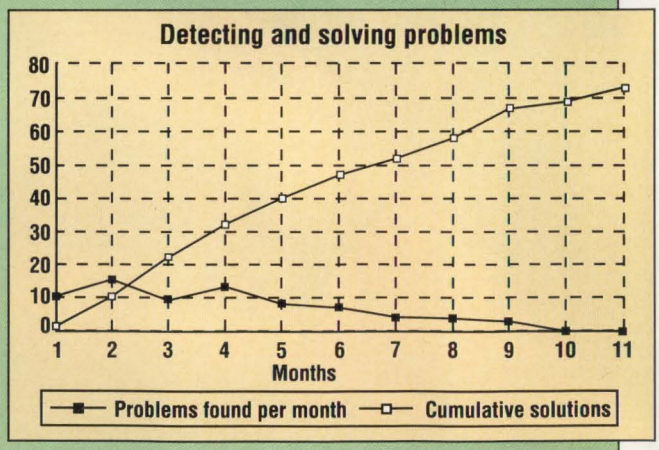


BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

Mistakes happen! Some are worse than others. Some occur randomly. Some can be predicted if properly observed. A simple, effective way to visually record the detection and solution of problems during the execution phase is given below. A working associate at Hewlett-Packard, Dave Gildea, introduced me to it.

Each imperfection detected in product and process is totaled for the month; solutions are illustrated cumulatively. In the first month, 10 problems are detected. By month 10, no problems remain to be found. Solutions begin to appear by the second month and by the eleventh month all known problems are solved.

For obvious reasons, errors in system design tend to have greater effect on project milestone dates than those in hardware and software modules. Tools and techniques discussed in previous columns can help you deal with random and predictive errors in design.



When an error is detected, the appropriate person or team goes into synthesis mode to figure out a way to deal with the problem. Usually detection of the error is reported well ahead of the solution sequence. Problem solvers can practice a form of management "by wandering around" and get involved with first-hand discussions on the error and methods for a potential solution.

Together with the appropriate solution people, a task network is created and inserted into the plan. Milestone impact is measured to drive another iteration on the error-correction network. Once agreement is reached, the updated plan is communicated and tracked. Tracking and understanding the cause of each error can assist in isolating random errors from predictive ones.

QUICKLOOK

TIPS ON INVESTING

Asset allocation is becoming the most talked-about investment topic of our time. It has become even more important recently thanks to globalization of the world economy, volatile markets, and the collapse of fiscal and political walls. Yet asset allocation is essentially simple: To accomplish your investment goals, how much money should you commit to each of a variety of asset types?

If, like most engineers, you're planning to retire five, ten, fifteen, or more years from now, you're focused on building a nest egg while setting aside resources for the education of children or grandchildren, buying a second home, or paying for the lifestyle you enjoy. Or perhaps you're not planning to retire at all—you'd rather keep working, change careers, start your own business, or go back to school.

Once you've identified your goals, consider your risk tolerance. Are you conservative, moderate, or aggressive with regard to risk? If a 60-year-old engineer and a 40-year-old one both characterize themselves as conservative, they nonetheless would probably not have the same asset allocation.

When you think about risk, consider the importance you attribute to the following:

- Growth—the ability of an investment to appreciate in value over time. Individual stocks, mutual funds, variable annuities, and zero-coupon bonds are growth-oriented investments.
- Income—the ability of an investment to supply current and/or future income. Government and corporate bonds are excellent choices for current income. So are municipal bonds for tax-free income. And fixed annuities supply a method for investing now, tax deferred, for future income.
- Liquidity—the ability to turn an investment into cash as needed with minimal risk or penalty. Money market funds and certificates of deposit provide higher quality yields than ordinary savings while retaining liquidity.
- Taxability—the ability of an investment to maximize after-tax return. Municipal bonds and tax-deferred annuities make sense for tax-sensitive investors. *Every engineer should take advantage of tax-deferred opportunities like IRAs and 401(k) plans.*

Rank these investment characteristics in order of their importance to you. Think about the time horizon of your investment goals. If you're investing for the short-term, your tolerance for risk is somewhat limited, as are your investment choices. Longer term goals give you a wide selection. Regardless of your risk tolerance, every engineer needs an element of growth, income, and liquidity in investments.

Then each engineer should evaluate his or her current holdings. To meet your goals, you may need to make changes, which can be as simple as shifting from money-market funds to short-term CDs or government securities. That way, an investor maintains liquidity and safety while obtaining higher yields.

Consider the higher quality and yields of corporate and municipal bonds as well as mortgage-backed securities. Every investor should consider equity investments as part of long-term investment strategy and as a hedge against inflation. If you'd like a free personal strategic asset allocation report, call or write to me.

Henry Wiesel is a financial consultant for Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221 or (908) 389-8653.

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *Art of Electronics*, second edition, by Paul Horowitz and Winfield Hill. Cambridge University Press, 1990. ***$54.50.***
2. *C Language Algorithms for Digital Signal Processing* by Paul Embree and Bruce Kimble. Prentice-Hall, 1991. ***$55.***
3. *Spice for Circuits & Electronics Using PSpice* by Mohammed H. Rashid. Prentice-Hall, 1990. ***$24.***
4. *Noise Reduction Techniques in Electronics* by Henry Ott. John Wiley & Sons, 1988. ***$47.95.***
5. *PSpice and Circuit Analysis* by John Keown. Macmillian, 1991. ***$24.***

COMPUTER SCIENCE:

1. *C Programming Language*, second edition, by Brian Kernigan and Dennie Ritchie. Prentice-Hall, 1989. ***$33.***
2. *Advanced C++ Programming Styles & Idioms* by James Coplien. Addison-Wesley, 1991. ***$33.50.***
3. *C++ Programming Language*, second edition, by Bjarne Stroustrup. Addison-Wesley, 1991. ***$34.50.***
4. *C++ Primer* by Stanley Lippman. Addison-Wesley, 1991. ***$32.25.***
5. *Internetworking with TCP/IP*, Vol. 1, second edition, by Douglas Comer. Prentice-Hall, 1990, ***$52.***

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; (415) 326-0681; fax (415) 326-0693.

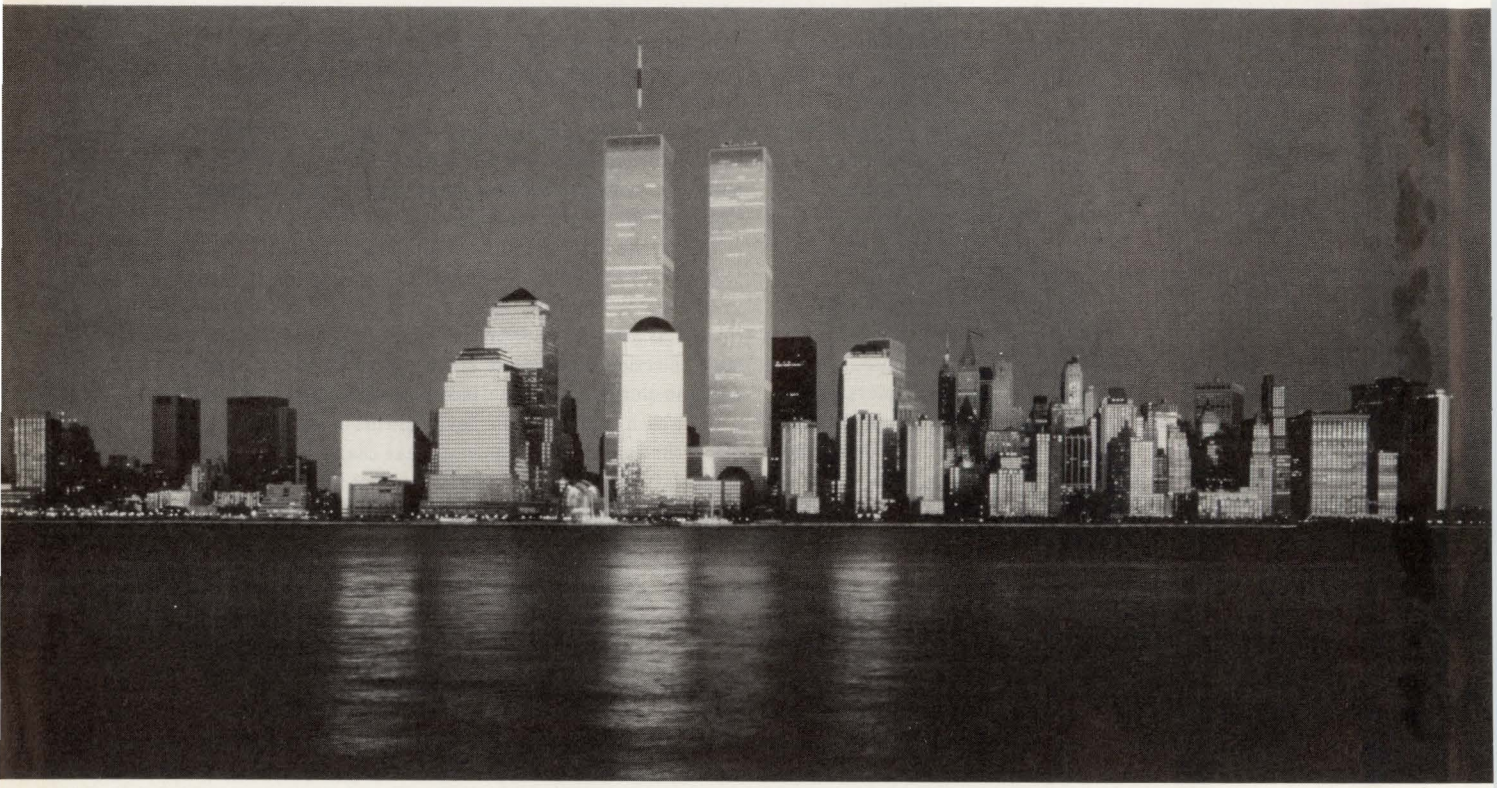
WHICH COUNTRY HAS THE BEST QUALITY REPUTATION?

	U.S. consumers	Japanese consumers	German consumers
Best quality personal computers			
U.S.	48	12	14
Japan	39	80	45
W. Germany	1	1	33
Don't know	12	7	8
Best quality TVs and VCRs			
U.S.	28	2	2
Japan	66	91	59
W. Germany	1	1	37
Don't know	5	6	2
Number of interviews	(1008)	(1446)	(1000)

Source: Gallup Organization, ASQC

Consumers tend to think highly of the goods produced in their own country, except for TVs and VCRs, where the consensus favors Japan. Americans and Germans think Japan has the best reputation for quality in TVs and VCRs. Germans think Japan has the best quality reputation in personal computers. These findings come from The Gallup Organization, which conducted an international quality survey in June for the American Society For Quality Control. Milwaukee, Wis. Gallup polled 1008 consumers in the U.S., 1446 in Japan, and 1000 in West Germany. Sampling error is ± 3%

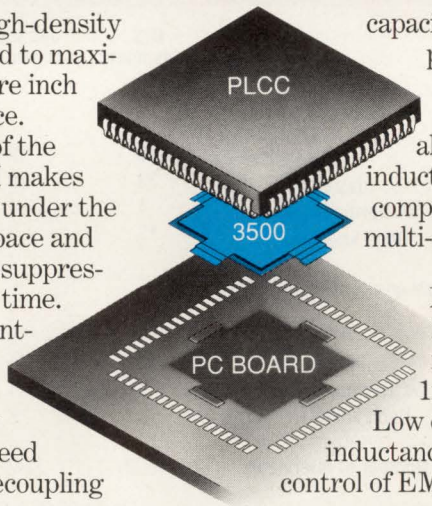
When space is at a premium, stacking makes a lot of sense.



Micro/Q® 3500SM noise decoupling capacitors save valuable board space by surface mounting below PLCC packages.

In today's high-density designs, you need to maximize every square inch of PC board space. The low profile of the Micro/Q 3500SM makes it easy to mount under the PLCC, saving space and improving noise suppression at the same time.

Surface mounting under the PLCC increases board density by eliminating the need for traditional decoupling capacitors around the perimeter of the IC package. This "stacking" technique also helps to lower inductance and impedance compared to conventional multi-layer capacitors.



Very thin (0.020" MAX) metallic-parallel plate construction results in less than 1nH of inductance. Low decoupling loop inductance value improves control of EMI/RFI. Besides providing superior noise reduction, the Micro/Q 3500SM also absorbs CTE mismatch and prevents electrical failure caused by cracks typical of MLC chips.

The device is ideal for wide frequency bandwidth applications such as 16/32 bit MPUs, DSPs, FPPs, gate arrays, standard cells and custom ASICs. Now available in two sizes: 0.520" to fit below 44 and 52 pin PLCCs, and 0.820" for placement under 68, 84 and higher pin-count PLCCs. Choose either X7R or Z5V dielectric, in tape and reel or bulk formats.

Technology for tomorrow built on TQC today.

ROGERS

Rogers Corporation
Circuit Components Division
2400 S. Roosevelt St., Tempe, AZ 85282
Tel: (602) 967-0624, Fax: (602) 967-9385

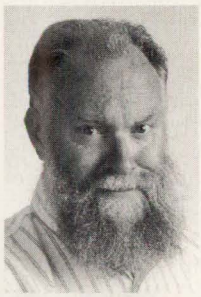
To see how all the advantages stack up, call a Rogers Product Specialist today at (602) 967-0624. Ask for your free Micro/Q 3500SM specifier's kit.

Also available through Mektron Europe, Ghent, Belgium and Rogers Inoac Corp., Nagoya, Japan. Micro/Q is a registered trademark of Rogers Corporation.

CIRCLE 160 FOR U.S. RESPONSE CIRCLE 161 FOR RESPONSE OUTSIDE THE U.S.

WHAT'S ALL THIS PROFIT STUFF, ANYHOW?

Here's another esaeP's Fable. The Class of 1966 was starting to plan its 25th Reunion. The Reunion Committee went around and contacted all the alumni, until they came to Joe. Joe, as duly noted in the Yearbook, was the Person Least Likely to Succeed in Business. That had been a clear choice, back in 1966 – everybody recognized that Joe was a klutz, with no sense of proportion, no head for math nor business. But Joe had filled in his questionnaire: President and CEO of Widget Enterprises – a multi-billion dollar multi-national corporation. And Joe had just donated a new Library to the Business School. How could this be? So it was with great respect and curiosity that the Reunion Committee invited Joe to give the key-note address at the Reunion.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

It was the same old Joe who stood up to give the speech at the Reunion. "I never was much of a speech maker. And I don't have any big secrets about how I do business. I just buy Widgets for $1.00, and I sell them for $10.00. I'm perfectly happy to take just a 10% profit." *End of Fable.*

When I started work at George A. Philbrick Researches in 1960, I observed a secret project going on – a "skunk-works" project to bring out Philbrick's first solid-state operational amplifier. Technicians were testing and grading diodes and transistors, night and day, to generate matched pairs. The data sheet was being rushed to completion. Test engineers were learning how to measure currents in the picoampere range. And Sales hoped to sell a few of these P2 amplifiers, at a selling price of $185, to pay for all this research effort.

Wow. An op amp with just 100 picoamperes input current – with no tubes, no heater power, no mechanical choppers. That must use the finest new silicon transistors. No wonder it sells for $185. But when I got to know the senior engineer, Bob Malter, a little better, he showed me that there were not any silicon transistors in the P2. There were just 7 little germanium transistors in there. *What*? WHAT??

When Bob Malter arrived at Philbrick Researches in Boston in 1957, he was already a smart and accomplished engineer. After designing several analog computer modules (which were the flagships of the Philbrick product line) he became intrigued with the concept of the Varactor amplifier, just about the time that George Philbrick, the founder and chief Research Engineer, was getting frustrated.

George had been trying to make a parametric amplifier, using varactor diodes and germanium transistor amplifiers. When the bridge started out balanced, just a few millivolts of dc input could cause enough imbalance to be amplified and then rectified (synchronously) to drive a dc amplifier. In theory, you could make an operational amplifier that way. But George had worked for many months on an elegant design he called the P7. It used 14 germanium transistors, in a little cordwood assembly with 8 little pc boards packed in between 2 mother boards. He could not get good repeatable results, not for dc accuracy or dynamics or temperature drift.

Now, Bob Malter was a very pragmatic, hard-headed engineer. You would *not* want to bet him that he could not do something, because he would determinedly go out and do it, and prove that he was right – and that you were wrong. Bob had his own ideas on how to simplify the P7, down to a level that would be practical – which he called the P2. I do not know how many false starts and wild experiments Bob made on the P2, but when I arrived at Philbrick as a green kid engineer in 1960, Bob was just getting the P2 into production.

Instead of George's 10 pc boards, Bob had put his circuits all on just two pc boards that lay back-to-back. Instead of 14 transistors, he had a basic circuit of 7 transistors – just one more device than the little 6-transistor AM radios of the day. He actually had 2 little transformers – one to do the coupling from the 5-MHz oscillator down into the bridge, and one to couple out of the balanced bridge into the first of four RF amplifier stages. (If you are really interested in the complete schematics of the P2 and P7, and other technical comments and details, you will want to buy Jim Williams' book.*) Note, 25 years ago, these would have been the center of fantastic technical espionage; but today, it's just a matter of historical curiosity – industrial archaeology – on an obsolete product. You can't buy the parts to make these amplifiers any more, and even when you could, you could build a circuit to follow the schematic, and it wouldn't work.

So what's the big deal? Here's a pretty crude operational amplifier with a voltage gain of 10,000, and an output of ±1 mA at ±10 volts, with a *vicious* slew rate of 0.03 volts per microsecond. Who would buy an amplifier like that??? It turned out that *thousands* and THOUSANDS of people bought this amplifier, because the input bias current at either input was just a few picoamperes. *Picoamperes*? What the heck is a *picoampere*?? Most electrical engineers in 1960 didn't even know what a picofarad was, not to mention a picoampere, but, they figured out it was a heck of a small fraction of a microampere. And for many high-impedance instrumentation applications, the P2 was clearly the only amplifier you could buy that would do the job. And it had this low bias current,

PEASE PORRIDGE

only a few picoamperes, because all those germanium transistors were running at 5 Mcps, and their 5 or 10 μA of dc base current had no effect on the precision of the input current.

The input current was low, thanks to a well-matched bridge of four V47 varicaps. These were sold by Pacific Semiconductor Inc. (PSI) for use as varactors in parametric amplifiers, up in the hundreds of "Megacycles." The "V47" designation meant that they had a nominal capacitance of 47 pF at 4-V reverse bias, which is where most RF engineers would bias them. But Bob Malter biased them right around 0 Vdc, with a minuscule ±60 mV of ac drive. At this bias, the capacitance was 110 pF plus 1 pF per 20 mV – not an extremely high gain slope.

At this level of drive, each diode would only leak 20 or 40 pA. But Bob had a gang of technicians working day and night to match up the forward conduction characteristics and the reverse capacitance voltage coefficients, and he was able to make sets of 4 varactors that would cancel out their offset drift versus temperature, and also their reverse leakage. Of course, there was plenty of experimenting and hacking around, but eventually a lot of things worked OK. After all, when you buy 10,000 V47s, *some* of them have to match pretty well.

So, here's a little do-hickey, a little circuit made up of just about as much parts as a cheap $12 transistor radio, but there was quite a lot of demand for this kind of precision. How much demand? Would you believe $227 of demand? Yes! The P2 originally started out selling for $185, but when the supply/demand situation heated up, it was obvious that at $185, the P2 was underpriced. So the price was pushed up to $227, to ensure that the people who got them were people who really *wanted* and *needed* them.

Meanwhile, what other kinds of "transistorized" op amps could you buy? Well, by 1963, for $70 to $100, you could buy a 6- or 8-transistor amplifier, with I_{bias} in the ball-park of 60,000 to 150,000 pA, and a common-mode range of 11 V. The P2 had a quiet stable input current guaranteed less than 100 pA (5 or 10 pA typical), and a common-mode range of ±200 V. (After all, with transformer coupling, the actual dc level at the balanced bridge could be at any dc level, so there was no reason the CMRR could not be infinite.)

Wow! A $227 *gouge*. (You couldn't call it a "rip-off", because the phrase hadn't been invented, but perhaps that is the only reason....) Obviously, this must be a very profitable circuit. Every competitor – and many customers – realized that the P2 must cost a rather small amount to build, even allowing for a few hours of work for some special grading and matching and testing. So, some people would invest their $227 and buy a P2 and take it home and pull it apart and try to figure out how it worked. The story I heard was that one of our competitors hired a bright engineer and handed him a P2 and told him, "Figure out how they do this. Figure out how we can do it, too." In a few days he had dismantled the circuit and traced it out, and had drawn up the schematic. Then he analyzed it, and began experiments to be able to meet or exceed the P2's performance. But he couldn't get it to work well. He tried every approach, but he never could. After a full year, they gave up.

You see, it turns out there was some interaction between the input of the first RF amplifier and the output of the 4th amplifier, that made the P2 work, when you assembled the two pc boards close together. It would not work with any other layout, orientation, or circuit-assembly technique. So none of our competitors ever second-sourced the P2. And the P2 and P2A and SP2A remained profitable and popular even when the new FET-input amplifiers came along at much lower prices. It was years later before these costly and complex parametric amplifiers were truly and finally obsoleted by the inexpensive monolithic Bifet amplifiers from National Semiconductor and other IC makers. Even then, the FET amplifiers could not compete when your instrument called for an op amp with a common-mode range of 50 or 200 V.

Still, it is an amazing piece of history, that the old P2 amplifier did so many things right. It manufactured its gain out of thin air, when just throwing more transistors at it would probably have done more harm than good. And it had low noise, and extremely good input current errors – traits that made it a lot of friends. The profits from that P2 were big enough to buy Philbrick a whole new building down in Dedham, Massachusetts, where Teledyne Philbrick is located to this day, (notwithstanding a recent name change to Teledyne Components). And the men of Philbrick continued to sell those high-priced operational amplifiers, and popularized the whole concept of the op amp.

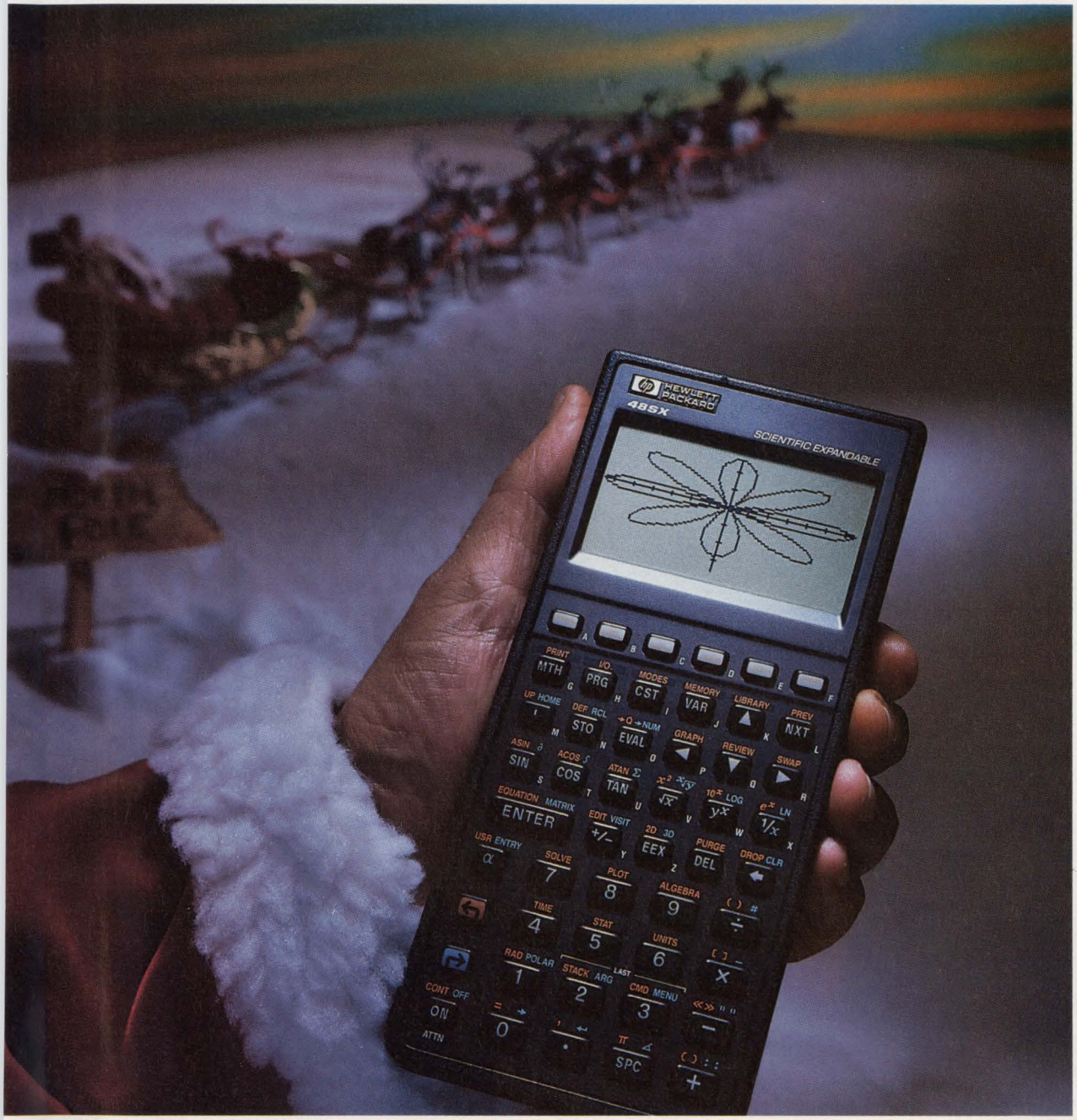
Then when good low-cost amplifiers like the UA741 and LM301A came along, they were readily accepted by most engineers. *Their* popularity swept right along the path that had been paved by those expensive amplifiers from Philbrick. If George Philbrick and Bob Malter and Dan Sheingold and Henry Paynter and Bruce Seddon hadn't written all those applications notes and all those books and stories, heck, Bob Widlar might not have been able to *give* his UA709s and LM301s away! And the P2 – the little junk box made up virtually of parts left over from making cheap transistor radios – *that* was the profit engine that enabled and drove and powered the whole operational-amplifier industry.

One time, I was standing around in front of the Philbrick booth at the big IEEE show in New York City. A couple engineers were hiking past the booth, and the one said to the other, nodding his head toward the booth, "...and there's the company that makes a *big bloody* profit...." Well, at that time George A. Philbrick Researches was indeed making big profits from the P2. We could never deny that. Just like Joe and his Widgets.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

Address:
Mail Stop C2500A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

**Analog Circuit Design: Art, Science, and Personalities*, by Jim Williams, about $45. Published by Butterworths (617) 438-8464 x255.



As you would expect, the perfect Christmas calculator can do polar plots.

The HP 48SX will revolutionize the way you work.

No wonder the revolutionary HP 48SX is on so many wish lists this year. It's the only scientific calculator that has over 2100 built-in functions and custom capabilities.

You can type an equation just like it appears in a textbook. Graph an equation and determine its characteristics while viewing it. Or, with automatic unit management, enter data in any given unit and get the answer in the unit you want. And all with the option of accessing PCs via a built-in serial I/O.

And when you buy an HP 48SX this holiday season, you'll also be helping America's kids excel! Your purchase of an HP 48SX will help equip selected high schools with a $5,000 set of calculators and other key teaching materials.

So put an HP 48SX on your shopping list now, and see your nearest HP retailer today.

HP calculators. The best for your success.

HEWLETT PACKARD

CIRCLE 108 FOR U.S. RESPONSE

CIRCLE 109 FOR RESPONSE OUTSIDE THE U.S.

C&C Computers and Communications

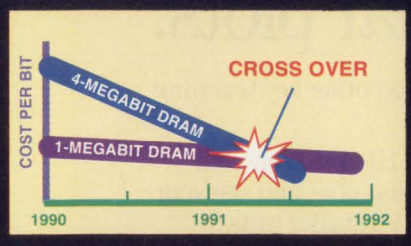
Be cool. Cross over to NEC.

Purchasing won't get hot under the collar.

Now there's something Engineering and Purchasing can agree on: NEC 4-megabit DRAMs.

Engineering gets legendary NEC quality and reliability. Purchasing gets competitive prices and a single vendor for almost every package type and memory organization imaginable.

You won't just save power and board space; you'll save money. That way, nobody gets burned.



The sweetest memories under the sun.

NEC DRAMs come in all the cool flavors: 300/350 mil SOJ, ZIP, TSOP, modules, low power, byte-wide, word-wide, you name it.

And if you need to get to data at a sizzling pace, look no further than NEC. We offer access times from 60 to 100 nanoseconds.

Choose from x1, x4, x8, or x16 memory organizations to meet your present needs. And very soon, you'll be able to select x9 or x18 devices as well. We want to supply all your memory needs, including the most advanced 16 megabit devices.

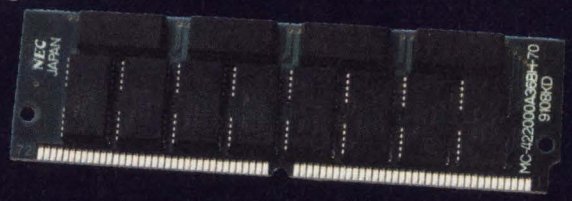
Warm up to Roseville, California DRAMs.

We've invested $600 million in our 72-acre Roseville wafer fabrication facility, located in California's gold country, near sunny Sacramento.

Our California plant has been producing DRAMs in high volume since 1984. It employs more than 700 skilled local workers. They join a worldwide team of more than 80,000 NEC employees that can meet challenges of almost any size.

Whatever your DRAM requirements, we have what you've been looking for. Now's a real cool time to cross over to NEC.

Modules (custom & standard)



ZIP

SOJ

TSOP

Australia Tel:03-267-6355. Telex:38343. **France** Tel:1-3946-9617. Telex:699499. **Germany** Tel:0211-650302. Telex:8589960. **Hong Kong** Tel:755-9008. Telex:54561. **Italy** Tel:02-6709108. Telex:315355. **Korea** Tel:02-551-0450. Fax:02-551-0451. **The Netherlands** Tel:040-445-845. Telex:51923. **Singapore** Tel:4819881. Telex:39726. **Sweden** Tel:08-753-6020. Telex:13839. **Taiwan** Tel:02-719-2377. Telex:22372. **UK** Tel:0908-691133. Telex:826791. **USA** Tel:1-800-632-3531. Fax:1-800-729-9288.

NEC

CIRCLE 140 FOR U.S. RESPONSE

CIRCLE 141 FOR RESPONSE OUTSIDE THE U.S.

CONFIGURABLE CPU DOUBLES UP TIME

EXTEND BATTERY LIFE WITH 3.3-V 386 CPU.

DAVE BURSKY

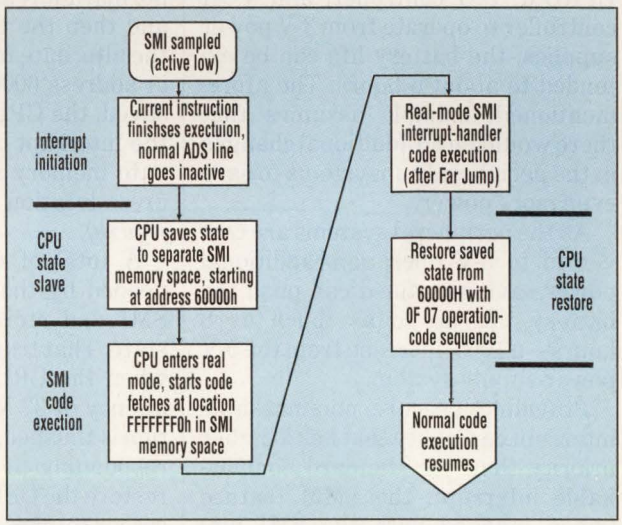
Recently, several companies have released static-logic implementations of the CMOS 80386 microprocessor to compete with Intel's standard 80386 microprocessor family, as well as with Intel's highly-integrated CPU for battery-powered systems, the 80386SL. However, most of the chips require a 5-V power supply for operation. And in the "closed" environment of a battery-powered system, significant power is wasted by every chip in the system.

Responding to this, designers at Advanced Micro Devices created 3-V versions of their Am386 CPUs—the Am386SXLV and DXLV—which will consume just 45% of the power of the 5-V microprocessors. For instance, with the processor operating at 25 MHz from a 5-V power supply, it typically consumes about 210 mA, while at 3.3 V, the CPU's current drain drops to about 95 mA (an 8-MHz, 3.3-V CPU consumes less than 30 mA).

The chips have more to them, though, than just low power—they will include an equivalent to the system-management mode (SMM) that Intel includes in its SL version of the microprocessor.

There are four new signals added to the Am386 CPU pinout, but they don't add new pins because AMD was able to use four of the previous CPU's no-connect pins. The four active-low signals include $\overline{\text{SMI}}$ (System Management Interrupt), $\overline{\text{SMIADS}}$ (SMI Address), $\overline{\text{SMIRDY}}$ (SMI Ready), and $\overline{\text{IIBEN}}$ (I/O Instruction Break Fault). The $\overline{\text{SMIADS}}$ and $\overline{\text{SMIRDY}}$ signals provide the bus-control signals for the separate memory space used in the system-management mode.

The key to a low-power system, though, is to have the entire system operate at 3 V, not just the CPU. In line with this move to a lower power-supply voltage, several DRAM manufacturers have already started shipping DRAMs that operate from a 3-V power supply, and a couple of chip-set suppliers are sampling motherboard-logic chips that run at the reduced power-supply levels. The next piece of the puzzle, the display



THE SMI OPERATING FLOW STARTS by first interrupting the current execution, and then saving the current state of the processor. Once the processor's state is saved, the CPU goes to high memory to find the vector that points to the first instruction of the interrupt-code sequence. With the SMI capability, the CPU can transparently handle functions such as power management, even though the processor chip doesn't have any dedicated logic for power management.

controller, is also moving to 3-V operation as AMD works with various suppliers to create a complete system that can run at that low-voltage level.

Converting To 3 V

The hardest part of the system that has to be converted is the mass-storage subsystem and the serial and parallel I/O ports. The mechanical drive and its control logic will most likely be the last part of the portable system to convert over to 3 V. If memory cards are used rather than disk drives, the memory-card interface standard already specifies a 3-V operating mode in addition to the standard 5-V mode. Thus, new memory cards can be designed directly for the lower power-supply voltage. To tie the 3-V logic into the 5-V sections that will be hanging on, AMD expects to use level translators to provide the correct voltage levels when moving from 3 to 5 V or from 5 to 3 V.

A system built with the Am386SXL CPU running from a 5-V power supply might typically deliver about 4.5 hours of battery life. By moving the CPU, core logic, DRAM, EPROM, I/O controller, and VGA controller to operate from 3-V power supplies, the battery life can be extended to about 6 hours. The aforementioned example assumes that there would be no additional changes in the peripheral subsystems to save even more power.

As the peripheral systems are converted to 3-V operation, additional power savings gained can push the battery life up to as much as 8 hours—a 100% increase from the 5-V power-supply system.

Providing a secure, non-maskable interrupt capability that has a higher priority than the standard nonmaskable interrupt, the SMM feature (when invoked with the SMI pin) causes the processor to switch to a completely separate address space and start executing special interrupt-handling software. (In last past September's introduction from Chips and Technologies, its 80386-compatible CPUs also include a similar system-management feature that Chips and Technologies calls SuperState.)(ELECTRONIC DESIGN, *Sept. 26, p. 53).*

The SMM feature allows such functions as power-management software to be developed by designers, independent of the CPU's operating mode and operating system. This capability, in turn, allows system developers to only write one section of real-mode code rather than the multiple device drivers (one per operating-system or processor mode). Furthermore, if the SMI signal is coupled with I/O-trapping hardware, it can offer users transparent power-off and auto-resume functions when using peripherals that may not even be "power aware."

Transparent Execution

In the alternate address space, the SMM feature allows system and power-management interrupt software to execute transparently to the application or operating system that's running in the standard address space.

When the SMI pin is pulsed low (for four CLK2 cycles), the current instruction finishes execution, the normal address strobe goes inactive, and then the CPU state is saved in the alternate memory space starting at address 60000h. Once the state is saved, the CPU can begin executing the interrupt code held in the alternate memory space, starting at address location FFFFFFF0h *(see the figure).*

A total of 630 CLK2 cycles are needed by the CPU to react to the SMI and store the complete CPU state. That translates to about 9.5 μs when the CPU runs at a clock frequency of 33 MHz. When the execution is finished, 574 CLK2 cycles (corresponding to 8.7 μs) are needed to restore the CPU state before the processor returns to its normal program execution flow.

First Instruction

The first instruction to execute in the alternate memory space is a Far Jump command. This Far Jump command points the CPU to the first interrupt-routine instruction. I/O-transfer cycles are directed to the normal address space, where they would typically be used for power-management operations.

Several new instructions were added to the processor to support SMI software. A UMOV command performs data transfers between the SMI space and the normal system memory space. Software can also invoke the SMI by sending a special operation-code sequence to the processor. By using software to invoke the mode, operating-system-dependent device-driver code can be written for communication with the SMI power-management code. To use software for invoking the SMI, a reserved register bit in the CPU must be set and then a special operation code has to be executed (F1h).

Although the operation of the SMI mimics the functions that Intel's SMI performs, there are some differences—the save-state physical addresses, first code-fetch address, and the resume opcode are all different from the Intel SL chip's codes. Furthermore, the AMD SMI space can hold up to 1 Mbyte of directly addressable code. In contrast, Intel's SMI address space is limited to 64 kbytes. Finally, with the AMD UMOV instruction the CPU can access normal system memory without having to resort to bank-switching tricks.□

Price And Availability

Prices for the Am386SXLV and DXLV are the same as those for the SXL and DXL products, respectively, with the enhanced low-voltage capability and SMI being offered at no price premium. Those prices are $82 and $156 each for the SXL/SXLV and DXL/DXLV, respectively, in 1000-unit quantities, for both 20- and 25-MHz versions. Samples are available now and production is slated for this January. The chips will come in the same package pinouts as the previous SX and DX chips, except four of the no-connect pins on the SX and DX now have special functions associated with System-Management Interrupt signal.

Advanced Micro Devices, Inc., 901 Thompson Pl., P.O. 3453, Sunnyvale, CA 94088; (408) 732-2400. CIRCLE 511

How Valuable?	Circle
Highly	555
Moderately	556
Slightly	557

Know all advanced digital design timing and signal integrity errors before they happen.

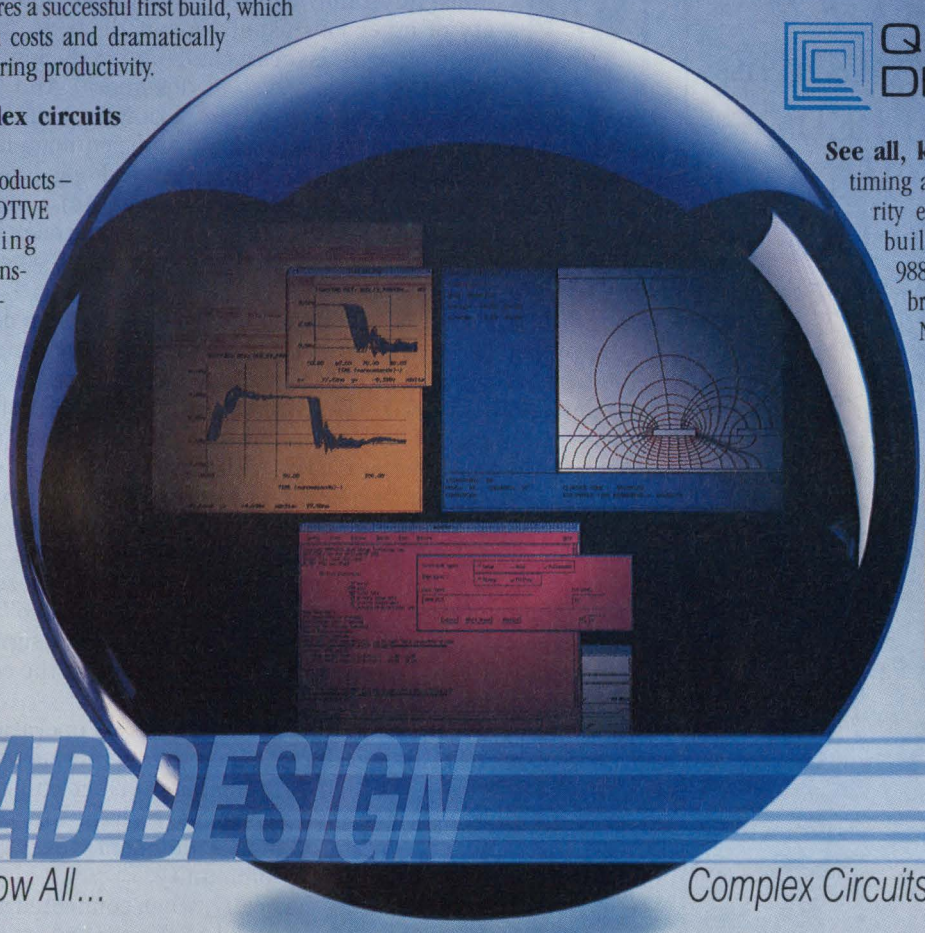
Quad Design makes it easy. Our family of tools — the only practical system-level timing and transmission line analyzers on the market today — resolves timing errors associated with advanced digital designs. Correcting errors while your design is still a vision ensures a successful first build, which reduces re-design costs and dramatically increases engineering productivity.

Analyze complex circuits in minutes.

Quad Design products – which include MOTIVE (Modular Timing Verifier), TLC (Transmission Line Calculator), XTK (Crosstalk Tool Kit) and PDQ (Pre-Route Delay Quantifier) — can be used independently or together to analyze complex digital circuits in minutes. They run on a broad spectrum of industry-standard engineering workstations and automatically interface with a host of popular CAE/CAD environments.

QUAD DESIGN

See all, know all system timing and signal integrity errors before you build. Call (805) 988-8250 for our free brochure. 1385 Del Norte Road, Camarillo, CA 93010... FAX (805) 988-8259.



QUAD DESIGN

See All, Know All... *Complex Circuits in Minutes*

CIRCLE 154 FOR U.S. RESPONSE
CIRCLE 155 FOR RESPONSE OUTSIDE THE U.S.

VOLTAGE-CONTROLLED IC AMPLIFIERS SEEK NEW JOBS

A TRIO OF UNIQUE ICS BRING VOLTAGE-CONTROLLED GAIN TO WIDE-RANGING DC, AUDIO, VIDEO, AND RF APPLICATIONS.

FRANK GOODENOUGH

Many of today's ICs are developed for specific niche applications. But if they happen to be analog building blocks, a variety of other jobs usually await them. In fact, nearly every new analog IC issues a challenge to the ingenuity and imagination of analog system designers. And Analog Devices' SSM-2018 and AD600/602 definitely issue such a challenge. The former was developed for professional audio equipment—the latter, for ultrasonic (medical) scanners. As functional building blocks, they appear similar: Both are voltage-controlled amplifiers (VCAs), a form of analog multiplier. In addition, both are protected by patents, and each represents a new type of analog building block. And that's just about where the similarity ends.

The SSM-2018 is aimed at controlling signal levels from dc through the audio- frequency band. The AD600/602 perform similar functions from dc to well beyond 35 MHz. A dc control voltage can change the gain of the SSM-2018 from –100 dB to over +40 dB. Similarly, a dc control voltage changes the input-to-output gain of both amplifiers in the AD600 from 0 dB to +40 dB and the gain of the amplifier pair in the AD602 from –10 to +30 dB.

The SSM-2018 looks and operates like a cross between an op amp and an analog multiplier *(Fig. 1)*. The AD600/602 are more like a cross between a multiplying digital-to-analog converter and an op amp *(Fig. 2)*. The audio part came from ADI's PMI Div., Santa Clara, Calif., but was designed by Douglas Frey of Lehigh University, Bethlehem, Penn. The "video" band chips from ADI's Semiconductor Div., Wilmington, Mass., were designed by Barrie Gilbert (inventor of the Gilbert-cell analog multiplier) at the company's Northwest Laboratories, Beaverton, Ore.

Frey and his PMI cohorts call the SSM-2018 an operational-voltage-controlled element (OVCE) and they even created a unique symbol for it *(Fig. 1a)*. For the first time, the SSM-2018 combines on one chip the functions of a circuit known as a VCA, for mixing consoles, with the functions of an op amp. While long used in professional-audio equipment, the VCA has remained virtually unknown outside of that community.

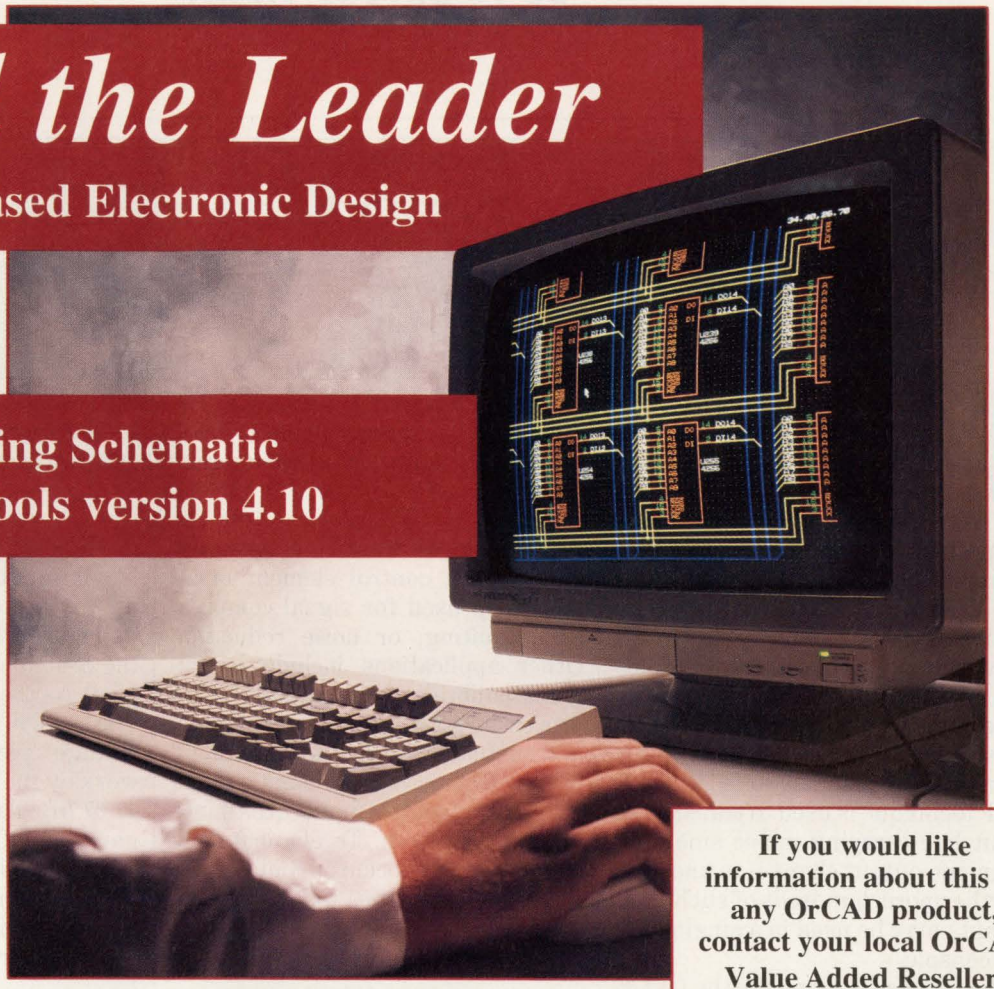
What does the SSM-2018 do? Basically, when connected as a follower, a dc voltage between 4 V and –1.5 V applied to the control input (V_C) varies the gain, between the differential input and the output, from –100 dB to over +40 dB, respectively *(Fig. 1b)*. A conventional fixed gain is achieved between the input and the 1–G output according to the equation

$$\text{Closed-loop gain} = (R_f + R_g)/R_g)$$

in addition to the gain controlled by V_G *(Fig. 1c)*. The control voltage operates with a scale factor of approximately 1 dB of gain change for a 28 mV control-voltage change, or 36 dB/V. Alternatively, like an op amp, a network defining a transfer function can be inserted in the feedback loop *(Fig. 1d)*. The device can also be connected as voltage-controlled potentiometer (VCP) to perform a balance or panning function by shifting the gain between the two

Still the Leader

in DOS based Electronic Design



Introducing Schematic Design Tools version 4.10

The leader in PC based EDA tools.

Why? Because we never stop improving our products. One example is our world famous *Schematic Design Tools* package with the *ESP framework.*

OrCAD has just released version 4.10 with these new features.

- dramatic increase in capacity
- utilities like netlist output have increased speed
- introducing new "hotkeys" in the ESP framework

The ESP Framework

The *ESP framework* is the first PC based framework that allows seamless integration between OrCAD tools and those of third party vendors. ESP framework is a part of Schematic Design Tools; no need to pay extra.

The OrCAD Difference

Schematic Design Tools still comes with the features you'd expect to pay more for:

- A library of over 20,000 unique parts you can browse through in a breeze.
- Utilities to generate Bill-of-Materials, electrical rules check, create custom library parts.
- Support for over 30 netlist formats.
- Over a hundred supported display adapters, 50 printer drivers, a dozen plotter drivers.
- User definable "smart" macros

As ever, all OrCAD products come with one year of product updates, telephone technical support and 24 hour BBS, and a subscription to The Pointer newsletter.

Call (503)690-9881 or write today for your FREE demo disk!

OrCAD ®

3175 N.W. Aloclek Drive
Hillsboro, OR 97124
FAX (503)690-9891

If you would like information about this or any OrCAD product, contact your local OrCAD Value Added Reseller.

WA, OR, MT, ID, AK, WY
Avcom/EDA
(206) 462-4040

N. CA, HI, Reno NV
Elcor Associates Inc.
(408) 980-8868

So. CA
Advanced Digital Group
(714) 897-0319

Las Vegas NV, UT, AZ, NM, CO
Tusar Corporation
(602) 998-3688

TX, OK, AR, LA
Abcor, Inc.
(713) 486-9251

ND, SD, MN, MI, WI, IL, IN, OH, KY, WV, W. PA, NE, KS, IA, MO
MacKellar Associates, Inc.
(313) 335-4440

VA, TN, NC, SC
Tingen Technical Sales
(919) 870-6670

E. PA, NJ, NY, DE, MD, DC
Beta Lambda, Inc.
(800) 282-5632

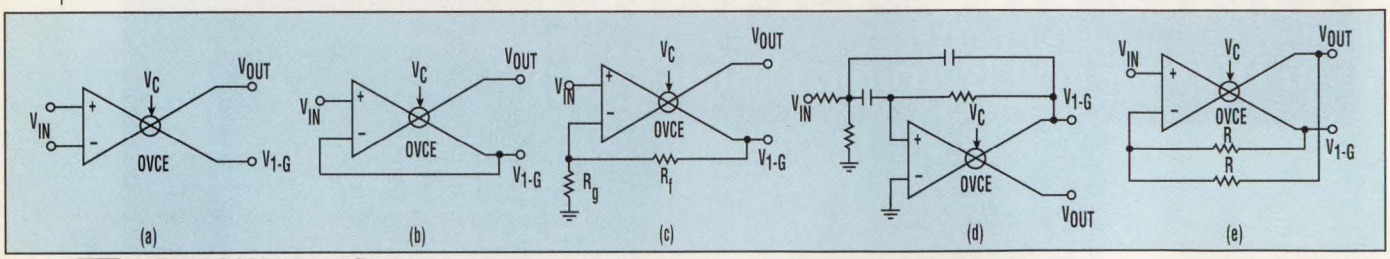
CT, RI, MA, VT, NH, ME
Tri-Logic
(508) 658-3800

CANADA
Pegasus Circuits
(416)567-6840

CIRCLE 144 FOR U.S. RESPONSE

CIRCLE 145 FOR RESPONSE OUTSIDE THE U.S.

DC-TO-BEYOND-VIDEO, VOLTAGE-CONTROLLED AMPLIFIER ICs



1. THE SSM-2018 IC operational-voltage-controlled-element or OVCE represents a new analog-circuit building block demanding a new graphic symbol (a). A voltage applied to the control input (V_C) sets the gain between V_{IN} and V_{OUT}. Combining the functions of an op amp and a voltage-controlled amplifier, it can be connected as a follower circuit (b), a follower circuit with gain (c), a filter circuit (d), or a voltage-controlled potentiometer (e).

outputs from 0 to 6 dB *(Fig 1e)*. That is, at one extreme of the control voltage V_G, a gain of 0 dB exists between the input and V_{OUT}, and a gain of 6 dB between the input and the V_{1-G} output. Taking the control voltage to its other limit smoothly interchanges these gains.

In the professional-audio field, the VCP technique is used to transfer an input line carrying music smoothly from one output channel to another. Furthermore, hundreds of such VCP circuits may be used in a single mixing console.

Basic specifications for the OVCE include a typical small-signal, gain-bandwidth product of 12 MHz, a typical full-power bandwidth of about 30 kHz, and a typical slew rate of 10 V/μs. That's while putting over 20 V pk-pk across 10 kΩ, the nominal load for most specifications. An external bias resistor puts the circuit into either class A or class AB operation. The former offers lower distortion, the latter lower noise. While running in the class A mode and putting out 1-kHz, 1-V rms sine waves, the OVCE's total harmonic distortion runs a maximum of 0.015%. Under similar conditions, class-AB operation results in 0.02% total harmonic distortion. Output noise is down a minimum of 85 dB while running in the class-A mode, and 95 dB running in the class-AB mode, from 20 Hz to 20 kHz, with a 1-V rms signal. Input resistance runs 4 MΩ.

Besides using it in audio-mixing consoles, an OVCE makes for a low-cost, gain-control circuit which can be remotely controlled by a distant front-panel potentiometer, host processor (with a DAC), or a wireless infrared link. Alternatively, it can act as the gain control element in an AGC loop used for signal compression, limiting, or noise reduction. Other applications include instrument calibration (potentially by a processor), trimming sensor signals, and matching signal levels. Applying a full-scale voltage change to the SSM-2018's control input turns it into an analog switch. To eliminate the click which can occur in audio applications if it switches too fast, a simple RC network is added in series with the control voltage.

Quirky Circuits

The OVCE, like its VCA predecessors, carries one little quirk, which when first discovered might cause a user to panic—a control-function temperature coefficient (tc) of –2700 ppm/°C. But don't panic. To compensate, add a resistor divider with a tc of +2700 ppm/°C in series with the control voltage. Many audio applications use similar circuits in the signal path presenting a +2700-ppm/°C tc, and the OVCE compensates for it.

The AD600/AD602 differ from the SSM-2018 *(Fig. 2, again)*. Each contains two, completely-independent, cascadable circuits capable of providing 40 dB of gain control. The AD600 nominally provides 0 dB to +40 dB of gain, and its cohort nominally provides –10 dB to +30 dB of gain. Their input signals are applied to seven-section R-2R ladder networks which produce 42.14 dB of attenuation between input and output. An imaginary wiper connected to an op amp (A_1) moves along the network under the control of an analog voltage applied to the gain-control input V_G. The AD600's op amp amplifies the voltage "picked off" the ladder network by the wiper, by a fixed gain of 41.07 dB. The AD602 op amp's fixed gain is 10 dB less, or 31.07 dB. The extra gain in the amplifiers permit trimming the gain-control scale factor to a nominal 32 dB/V and nominal gain to 30 or 40 dB.

Imaginary Elements

At the signal input (left) end of the network, the wiper (and thus the op amp's input) see the full input signal. At the ladder network's center, the signal is attenuated by 21.07 dB. Thus, the input-to-output signal gain of the AD600 is 20 dB (–21.07 dB + 41.07 dB). At the output (right) end of the network, the signal has been attenuated 42.14 dB and input-to-output signal gain is –1.07 dB (–42.14 dB + 41.07 dB). With its op-amp gain fixed 10-dB lower (31.07 dB), the wiper of AD602 varies the AD602's input-to-output gain from –11.07 to +31.07 dB.

The characteristic input resistance of the untrimmed ladder net-

TABLE 1: AD600/602 SPECIFICATIONS

Model	Control voltage (mV)	Gain (db) Minimum	Nominal	Maximum
AD600	–0.625	–0.5	0	0.5
	0	19.8	20	20.2
	0.625	39.5	40	40.5
AD602	–0.625	–10.5	–10	–9.5
	0	9.8	10	10.2
	0.625	29.5	30	30.5

WHEN YOU PLUNGE INTO ASIC DESIGN, YOU WANT SUPPORT TOOLS THAT WORK.

Oki's Advanced ASIC Tools Reduce Your Risk.

As an ASIC designer, you know the sinking feeling of working for weeks on a high-density design—only to have it crash. You know the risks involved using tools that offer no assurances.

Oki's advanced tools provide the lift you need to dive comfortably into high-level ASIC design:

Timing-driven layout - for an improved design-to-silicon match.

Clock tree structures - for optimized clock distribution.

Power calculator - for increased overall system reliability.

Coupled with our 0.8µm SOG technology and high-level support—such as Verilog, Synopsys, and IKOS—these Oki software tools optimize ASIC performance *and* design time.

So take the plunge. Call 1-800-OKI-6388, Dept. 050, for Oki's ASIC capabilities brochure. See how risk-free ASIC design can be.

Oki ASIC Design Tool Support for 0.8µm, 1.0µm, & 1.2µm

Vendor	*Platform*	*Operating System/Application*
Cadence	Sun/Solbourne	Verilog: Simulation, fault grading, design verification
IKOS	IKOS	Simulation, fault grading
Mentor Graphics	HP/Apollo Sun/Solbourne	Design capture, simulation Parade: Layout, clock and timing structures
Synopsys	Sun-4 Interface to Mentor, Valid, Viewlogic	Design synthesis, test synthesis
Valid	Sun/Solbourne DECstation 3100 IBM RS6000	Design capture, simulation Design check GED, ValidSIM, RapidSIM
Viewlogic	Sun-4 PC386	Design capture, simulation Design check

OKI Semiconductor

785 North Mary Avenue
Sunnyvale, CA 94086-2909
1-800-OKI-6388, Dept. 050

TRANSFORMING TECHNOLOGY INTO CUSTOMER SOLUTIONS

work runs between 100 and 150 Ω. However, a shunt resistor across the input (not shown) is laser-trimmed to provide an input resistance within ±2% of 100 Ω. If optimum performance is to be provided by these ICs, particularly over their full bandwidth of 35 MHz, this low input resistance must be driven by a low-impedance source such as a fast op amp. Alternatively, the 100 Ω can represent all or part of the terminating resistance of a coaxial cable or transmission line.

The wiper is moved by swinging the high impedance 1-MΩ differential input of the gain-control amplifier from –0.625 to +0.625 mV, essentially moving the wiper from the output end of the ladder (minimum-gain condition) to the input of the ladder (maximum-gain condition). The scale factor is trimmed to 32 dB/V ±0.3 dB/V *(see the table)*.

The gain of the AD600 in dB is easily calculated for any given control voltage by the simple equation: Gain (dB) = 32 V_G + 20, where V_G is the control voltage in volts. Similarly, the gain of the AD601 = 32 V_G + 10. The gain-control circuits can slew the gain at a rate of about 40 dB/μs; that is the gain can be changed a full 40 dB in 1 μs.

In addition to the smooth control of gain offered by these devices, their gain is brought to zero in just 1 μs, if their gate-control input is pulled to logic (TTL/CMOS) high. Bringing the input low returns the gain to the selected value, also in 1 μs. *(For details describing how this circuit works, contact Analog Devices for a copy of Gilbert's paper "A low-noise, wideband, variable-gain amplifier using an interpolated ladder attenuator.")*

The Gauntlet Thrown

As noted earlier, the AD600 and AD602 voltage-controlled amplifiers were developed for medical ultrasound equipment. These are the noninvasive scanners replacing X-ray machines, when possible, to avoid exposing the human body to ionizing radiation. Like sonar-type fish finders, they send pulses of acoustic energy into the medium being examined and create a picture on a CRT from the returning echoes. The acoustic signal is attenuated exponentially as it passes through the body. Thus, the greater the distance into the body, the weaker, and the later, the returned pulses.

To maximize the dynamic range of the system, the gain of the receiver is increased exponentially with time, starting just after the outgoing pulse is transmitted (the amplifier is gated off during the transmitted pulse) and continuing until the last echo is received. The technique is called time-gain control. Being an open-loop technique (unlike most AGC circuits), it requires the precision offered by these amplifiers. Note that for all three ICs, a linear change in the control signal provides a linear dB change in gain and thus actually a logarithmic/exponential change in gain (gain in dB = 20 $\log_{10}$ X V_{OUT}/V_{IN}).

The AD600/602 drop into numerous other echo-ranging sonic and ultra-sonic applications. These include active sonar and non-destructive test equipment. For non-destructive testing, the acoustic pulses are deployed into the structural members of, for example, operational aircraft. Echoes are returned from cracks invisible to the human eye. With a 3-dB bandwidth of 35 MHz and a response time of 1 μs, these amplifiers can become the heart of precision AGC loops in IF and RF amplifier chains. Added to the front end of a high-speed data-acquisition system, they can extend its dynamic range at least 4 bits.

Other specifications for the AD600/602 while operating from nominal ±5-V supply rails include a maximum input voltage of ±2 V, a maximum output swing of ±2.5 V driving 500 Ω, a typical group delay from 1 to 10 MHz of ±2 ns (with a similar value over the full range of gain), and total harmonic distortion of –60 dB. Quiescent current runs a maximum of 32 mA. While pulse-handling characteristics are not specified, the low group delay of the AD600/602 should ensure minimum pulse degradation when controlling the amplitude of pulses.□

Price And Availability

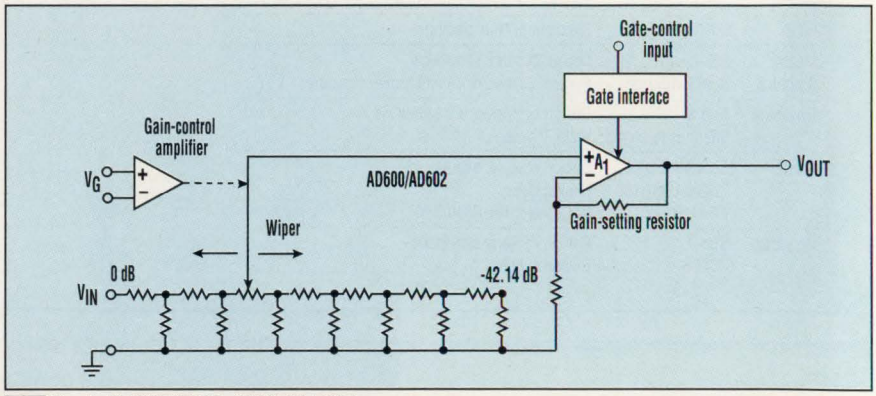
The SSM-2018 comes in 16-pin plastic DIPs and SOICs. It meets its specifications over the extended-industrial-temperature range. In quantities of 100, it goes for $3 and $3.25 each in the DIP and SOIC, respectively. Delivery is from stock.

Analog Devices Inc., Precision Monolithics Div., 1500 Space Park Dr., Santa Clara, CA 95052; Dan Parks, (408) 562-7513. **CIRCLE 515**

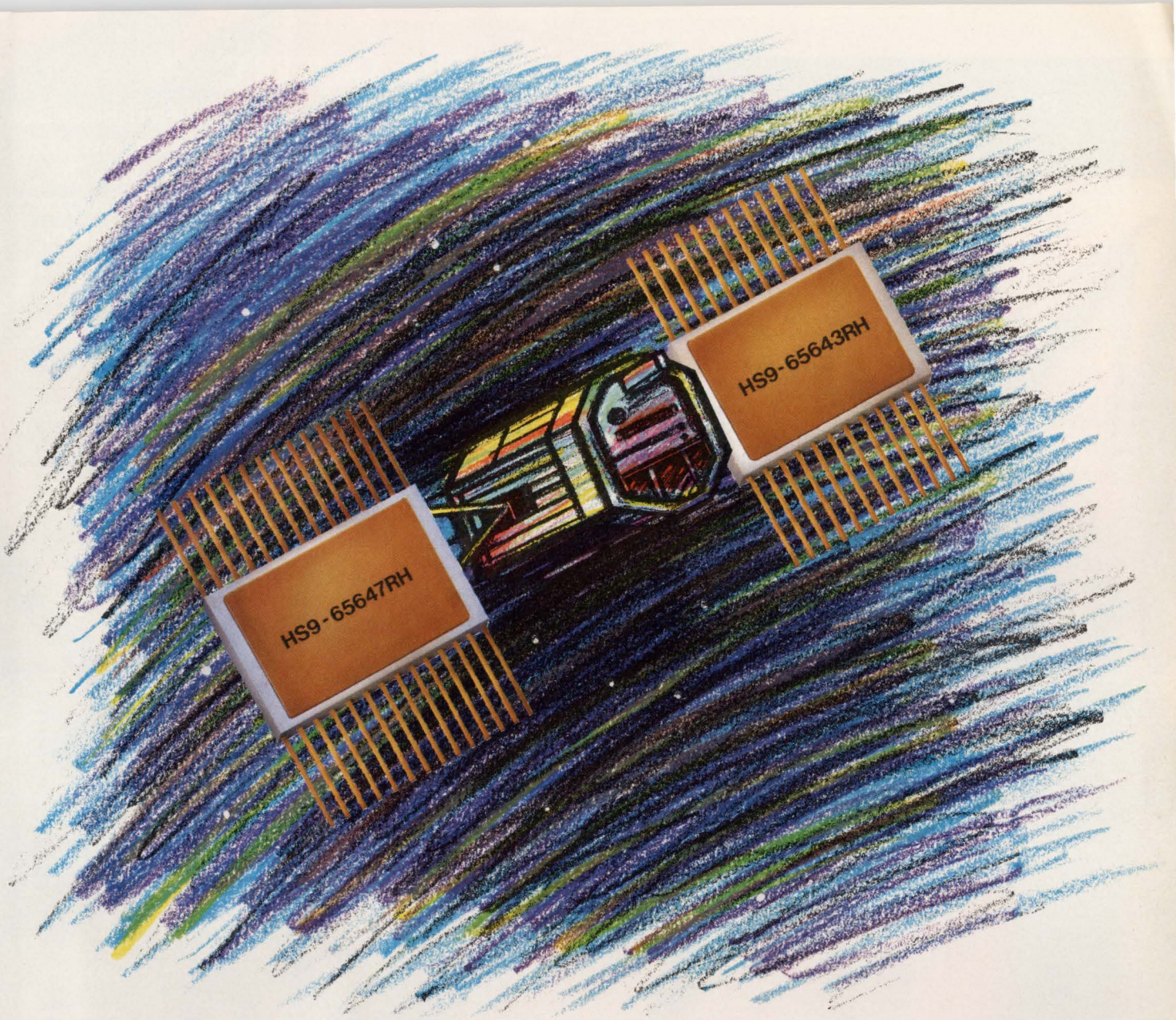
The AD600 and AD602 come in 16-pin plastic DIPs and SOICs and operate over the commercial-temperature range. Pricing starts at $15 each in hundreds.

Analog Devices Inc., Semiconductor Div., 181 Ballardvale St., Wilmington, MA 01887; Tom Varney, (617) 937-2508. **CIRCLE 516**

How Valuable?	Circle
Highly	558
Moderately	559
Slightly	560



2. A CONTROL VOLTAGE V_G applied to an imaginary wiper in the AD600 varies the gain between V_{IN} and V_{OUT} from 0 to +40 dB. A similar control voltage applied to the AD602 moves its gain from -10 to +30 dB.



The world's fastest 64K SRAMs for space applications.

Give your space applications the boost they need. With two new Rad Hard 64K SRAMs from Harris. Our 64K SRAMs aren't only the world's fastest for high-dose radiation environments. They're the world's most accurate.

Process:	1.25 micron TS0S4
Configuration:	64K x 1, 8K x 8
Access Speed:	50 ns
SEU Error Rate:	$<1 \times 10^{-12}$ Errors/Bit Day
Functionality:	Beyond 1M rad (si)

How does 50 ns access speed, an SEU error rate of less than 1×10^{-12} Errors/Bit Day, and full functionality beyond 1M rad sound? (Pretty out of this world, wouldn't you say?) And remember, Harris is the largest Class S Rad Hard supplier in the universe. So if it sounds like we're handing you the best of all possible worlds, it's because we are.

So don't delay. Make immediate contact with a Harris 64K SRAM. Call 1-800-4-HARRIS, Ext. 1023. And give all your systems a go.

HARRIS SEMICONDUCTOR

CIRCLE 106 FOR U.S. RESPONSE

CIRCLE 107 FOR RESPONSE OUTSIDE THE U.S.


CONNOISSEUR
CLASS
BERTH OF A NEW ERA.
It's comforting news. Our state of the art business class seats, with adjustable footrests, are wider than ever before. Just seven per row on the 747, and 6 per row on the 767.
Equally comforting is the fact that many of our new seats are available on the smoke-free upper decks of our vast 747 fleet.
Connoisseur Class,SM offered only by United. Where attention to detail elevates international business class to its highest form of civility. Available now on all trans-Atlantic and most trans-Pacific flights.
Come fly the airline that's uniting the world. Come fly the friendly skies.
UNITED AIRLINES

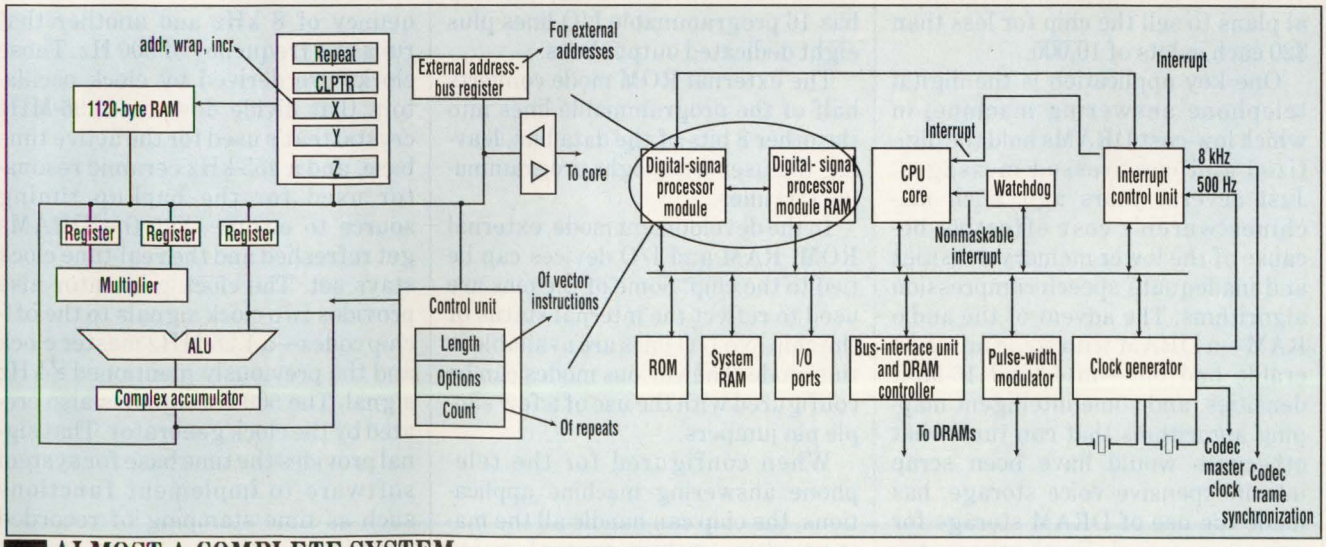
BY ADDING A DSP BLOCK TO A POWERFUL CPU, VOICE PROCESSING FOR SPEECH STORAGE OR PLAYBACK CAN EASILY BE ADDED TO CONSUMER OR INDUSTRIAL SYSTEMS.

ADD VOICE TO SYSTEMS WITH COMBO CPU/DSP IC

DAVE BURSKY

For at least half a dozen years, designers have had the ability to capture, digitize, compress, and then store speech for future playback, or recognize the words to perform a control operation. Dedicated speech-synthesis or -recognition chips give designers the fundamental speech-input/output capabilities they need. But for additional system functions, the extra controllers and support chips required make most voice-I/O systems too costly for consumer and industrial applications.

National Semiconductor now thinks it has solved these cost and systems integration problems. The solution was found by integrating a programmable DSP block onto the same piece of silicon as a 32/16-bit general-purpose processor core. The company also added most of the typically needed support func-



ALMOST A COMPLETE SYSTEM on a chip, the NS32AM160 from National Semiconductor combines a general-purpose CPU and a high-performance digital-signal processor block on the same chip with two blocks of RAM, a large ROM, as well as many system support functions. Thanks to the on-chip DSP block, and the CPU, both speech processing as well as system control functions can be handled by the single chip. Thanks to a dedicated multiplier and arithmetic and logic unit in the DSP block, as well as a local RAM, the DSP section can quickly execute the speech-processing algorithms (inset).

tions onto the same IC chip.

With such a chip, the company hopes to open up markets such as tape-less telephone answering machines, voice servers, voice-recognition systems, voice-annotation applications, intelligent terminals, voice prompting for appliance control or equipment maintenance, and many others. But to fit these markets, the chip must be inexpensive, pack most of the system on one chip, and have sufficient performance to satisfy users regarding voice quality in the case of playback or synthesis, or recognition accuracy for control applications.

More For Less

The NS32AM160 combines a core CPU from the company's 32000 series of general-purpose processors with a 16-bit integer vector sub-processor architected specifically for DSP applications *(see the figure)*. The chip also holds RAM and ROM, a real-time clock with 2-ms resolution, a watch-dog timer, and an 8-bit pulse-width modulator. In addition, there are dual clock generators (for the active and standby modes), an interrupt controller, a dynamic RAM controller, codec clock-generation and interface circuitry (for TP5512 or compatible codecs), and I/O lines. With all of these capabilities, National plans to sell the chip for less than $20 each in lots of 10,000.

One key application is the digital telephone answering machine, in which low-cost DRAMs hold the digitized and compressed messages. Just several years ago, such machines weren't cost effective because of the lower memory densities and inadequate speech-compression algorithms. The advent of the audio RAM—a DRAM with some unrecoverable bad bits—in 4- and 16-Mbit densities, and some intelligent mapping algorithms that can turn what otherwise would have been scrap into inexpensive voice storage, has made the use of DRAM storage for voice economical. Furthermore, the use of DRAM has to be closely coupled with the development of efficient compression algorithms (with silence detection) that can turn 64-kbit/s pulse-code-modulated data streams into intelligible speech played back at rates from 13 kbits/s down to 8.1 kbits/s.

At the heart of the 32AM160 are the dual processors—the CG 32-bit general-purpose core (with a 16-bit data bus) with its 1008 bytes of internal RAM and 25 kbytes of ROM, and the DSP core with its own 1120-byte RAM. The data bus between the CPU and both RAM arrays is 16-bits wide, while the DSP-core-to-RAM interface is 32-bits wide, allowing the DSP block to access two words every cycle to feed its multiplier and arithmetic and logic unit. When the DSP block is performing calculations, the CPU cannot access the DSP's RAM. The on-chip ROM also transfers data over a 16-bit memory bus.

The chip can operate in three basic modes: the internal, non-expandable mode that uses the internal 25-kbyte ROM and RAM, an external ROM mode with a 16-bit address bus and upper- and lower-byte strobes that can access up to 128 kbytes of off-chip ROM, and a development mode that provides an 18-bit address bus and support to address up to 512 kbytes.

In the internal mode, the external data bus is just 8-bits wide and two read cycles are required to bring in a 16-bit word. In that mode, the chip has 16 programmable I/O lines plus eight dedicated output lines.

The external ROM mode converts half of the programmable lines into the other 8 bits of the data bus, leaving the user with eight programmable I/O lines.

In the development mode, external ROM, RAM and I/O devices can be tied to the chip. Some of the pins are used to reflect the internal status of the chip. No I/O lines are available in this mode. The various modes can be configured with the use of a few simple pin jumpers.

When configured for the telephone answering machine applications, the chip can handle all the major tasks—system control, voice compression/decompression, and the dual-tone detection for subsequent control. System control includes functions such as keyboard control, display handling, line-activity monitoring, timekeeping, and power-failure detection. The on-chip DSP block handles the speech algorithms such as sub-band coding, linear predictive coding, and GSM (Groupe Speciale Mobile, the European compression standard for mobile communications). Part of the DSP functions also decode any tone inputs which designers can then use to perform remote system control (playback, erase, message change, etc.).

Compatible Processor

The general-purpose 1-MIPS core processor is compatible with the core used in the company's previously released NS32FX16 processor with only a few exceptions. The new NS32AM160 has a reduced interrupt latency since it now only supports the direct-exception mode. It does not support some of the instructions and addressing modes and does not perform clock scaling. The four-level interrupt controller monitors the on- and off-chip interrupt sources and resolves priority through a fixed arbitration scheme.

Four interrupt sources can be handled—three internal and one external. The three internal sources include the DSP block, and two low-speed clocks, one that runs at a frequency of 8 kHz and another that runs at a frequency of 500 Hz. Those clocks are derived by clock oscillators that divide down a 40.96-MHz crystal that's used for the active time base, and a 455-kHz ceramic resonator used for the backup timing source to ensure that the DRAMs get refreshed and the real-time clock stays set. The clock generator also provides two clock signals to the off-chip codes—a 1.28-MHz master clock and the previously mentioned 8-kHz signal. The 500-Hz signal is also created by the clock generator. That signal provides the time base for system software to implement functions such as time stamping of recorded messages.

Controlling all internal and external accesses, the bus-interface block and DRAM controller provides control signals for the internal cycles to

SINGLE-CHIP SPEECH AND SYSTEM CONTROLLER

the other on-chip blocks and to the different external devices. Four types of external device interfaces can be controlled—DRAM, ROM or RAM, codec, and I/O port. The controller handles four different DRAM accesses—the usual read, write and refresh cycles during normal operation, and a special slow refresh when the chip switches into its low-power mode.

The DRAM controller can tie into either one or two 1-Mword-by-4-bit or 4-Mword-by-4-bit audio-grade DRAMs that have a cycle time of 500 ns and an access time of 350 ns (worst case). DRAM control is specifically set up for a 24.32-MHz system while the refresh is set for 20.48 MHz—that permits the controller to run at any frequency between those two points, thus maximizing system flexibility.

When running from the internal ROM, the chip has three 8-bit I/O ports (A, B, and C), one of which is output only (port C). Each line in the A or B ports can be individually programmed as an input or an output. In the other two operating modes, ports B and C serve dedicated functions, but with some additional logic the functionality of port C and some of port B can be recaptured.

Development Tools

With any DSP function, the biggest challenge designers have to face is the development of the code needed to implement the functions such as tone detection or speech compression, or other operation. Similarly, for applications such as the answering machine, front-panel control functions can also consume a lot of development time. To solve many of the development issues and allow designers to get the first prototypes up and running quickly, National Semiconductor also developed a software library and some evaluation boards that can quickly let code be compiled and tested.

Routines included in the library are a Speech and DTMF handler that detects the dual tones and provides a control function based on the detected tones, an interrupt handler that designers use to set the system response to various conditions, and the speech-coding/decoding algorithms. The speech-processing portion of the library includes routines for voice recording, voice synthesis, and voice recognition. On the hardware side, designers will have a choice of several items—a full-fledged development board, the AM160EDB; a beta-site level prototype proof card; and a small 2-by-2-in. module that can be used as a production vehicle.

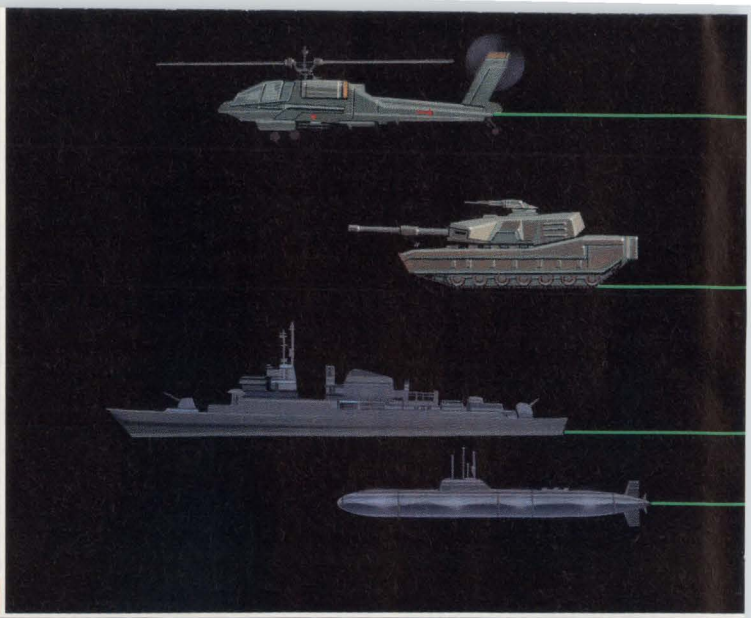
The full development board includes the 32AM160 configured in the development mode, and off-chip memory—space for DRAM, sockets for EPROM or ROM, 64 kbytes of static RAM, and I/O ports, as well as a breadboard area where user-specific blocks can be implemented. The processor runs a monitor program supplied in 256 kbytes of EPROM (two 128k by 8 chips), and ties to a host system through an RS-232 serial port. A second serial port is also available on the board. The card also has 16 programmable I/O lines, each individually configurable, as well as 8-bit latched output. A codec is on the card as well, thus simplifying the interface to digital speech files. Multiple switches on the card allow users to control various settings, and an LED display provides some local diagnostic readout.□

Price And Availabilty

Prices for the NS32AM160 with or without the 25-kbyte ROM in a plastic 68-lead chip carrier will be about $18 apiece in lots of 10,000. The chip is immediately available. A version with a 32-kbyte ROM will be ready in the first quarter of 1992, and it will sell for about $19.50 each, also in 10,000-unit lots. The full evaluation board sells for $2000 in single-unit purchases, while the verification board will sell for about $700. The small, production-size module goes for about $200 in small quantities, but in large volumes application-specific versions of it will cost less than $25. Prices for the various software packages are not yet established.

National Semiconductor Corp., 2900 Semiconductor Dr., M/S 16-320, P.O. Box 58090, Santa Clara, CA 95052-8090; Ronny Gorlicki, (408) 721-4429. **CIRCLE 513**

How Valuable?	Circle
Highly	568
Moderately	569
Slightly	570



The programmable display system:

Design applications for land, sea or air.

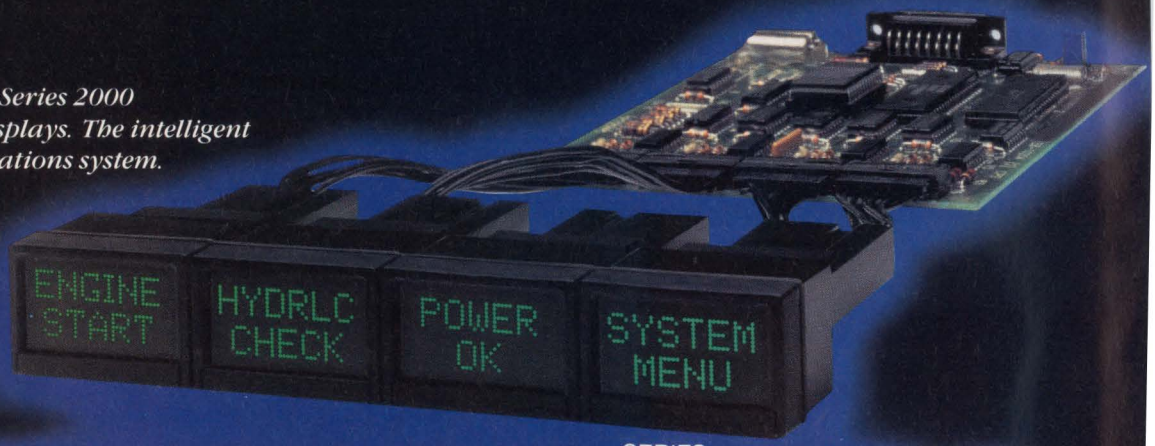
Vivisun Series 2000, now the leading programmable display pushbutton system, interfaces the operator with the host computer. The user-friendly LED dot-matrix displays can display any graphics or alpha-numerics and are available in green, red or amber. They can efficiently guide the operator through any complex sequence with no errors and no wasted time.

They also simplify operator training as well as control panel design. One Vivisun Series 2000 programmable display system can do the work of 50 or more dedicated switches. In short, Vivisun Series 2000 gives the design engineer more control over the design.

Contact us today.

AEROSPACE OPTICS INC.
3201 Sandy Lane, Fort Worth, Texas 76112
(817) 451-1141 • Telex 75-8461 • Fax (817) 654-3405

Vivisun Series 2000 programmable displays. The intelligent communications system.



SERIES

VIVISUN 2000™

CIRCLE 80 FOR U.S. RESPONSE
CIRCLE 81 FOR RESPONSE OUTSIDE THE U.S.

VMEbus Can Be Simulated Without Developing Complex Models For Other Boards Within The System.

Speed VME Board Designs Through Simulation

Richard Nass

Building a computer board that complies with industry-standard specifications has many advantages, not the least of which is the availability of debugging tools. The ability to simulate a bus and the stimuli that appears on the bus is a great help to board designers, and a tool that does just that on the VMEbus is SimuBus from Logic Automation Inc., Beaverton, Ore.

With SimuBus, the first nonstandard device model from Logic Automation, designers can set up a system environment that can be used with the board-level simulation. The environment represents a standard bus so that an interface can be built. Then users can set up a system-level model for other boards in the system to obtain the bus cycles for those boards. SimuBus doesn't care what the new design's function is, as long as it's VME-based.

SimuBus actually simulates a VMEbus system's activity, in relation to a particular board. The system can include other boards, such as masters or slaves, on the bus. There's no need to develop models of other boards in the system. By setting up this type of environment, a system atmosphere can be created, where programmable delays or several different types of boards can be added. SimuBus also creates a sophisticated stimuli-generation capability. This lets users realize complex happenings on the bus.

Creating a model helps catch many timing and logical problems in a simulation environment where there are many control functions. Without a model, these problems may still exist in the prototype. Then, questions arise in the design that could produce multiple responses, leaving designers scratching their heads. Though SimuBus just supplies a logical model, it sorts these issues beforehand so designers can concentrate on the physical issues of interfacing the bus.

C-Like Input

SimuBus is controlled by a processor control-language (PCL) file input. The PCL file is the same that's used to control Logic Automation's hardware verification models (microprocessor-model bus functions). PCL uses a C-like language, so designers can do simple modifications to create a given stimulus. The PCL files let users algorithmically configure the bus operations for the system boards. Programmable timing exists to verify the bus's critical signals. In a typical bus environment, a slave won't continually respond with the same delay each time a command is sent. With SimuBus, users can program a range of values to see the interaction

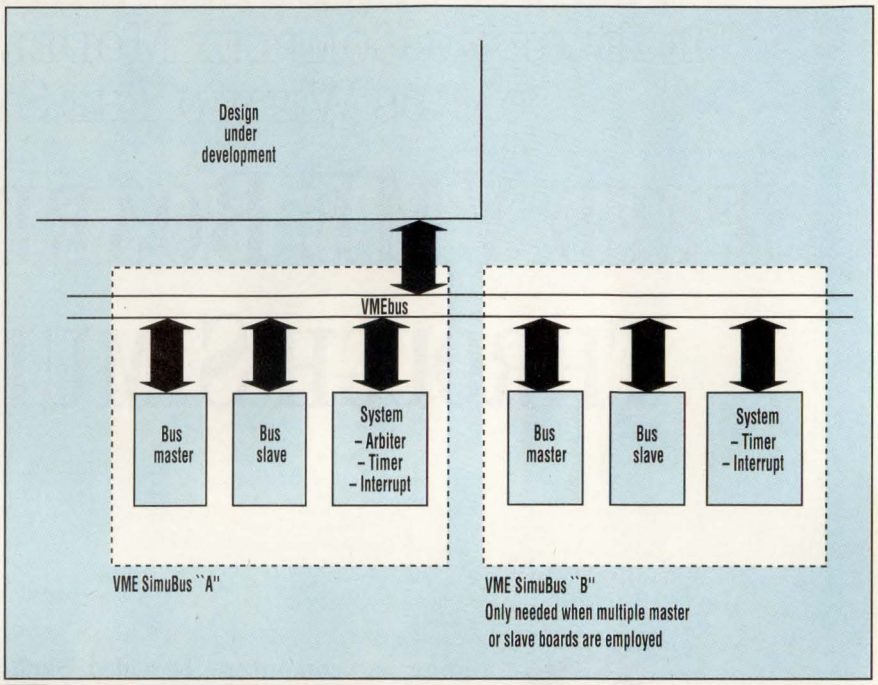
and time intervals between the boards. Then, in a critical interaction, where there's handshaking between boards, delays can be inserted to avoid contention or communication problems. Test cases can also be added to handle such functions as multiple timing delays.

SimuBus supports an incremental debug flow. Hence, designers follow an incremental building process, starting with simple bus reads and writes, rather than waiting until the board is almost built to begin testing. This allows for earlier tests, and for corrections of simple problems before they become more complex. Because of the way the VME model is set up with the PCL input, a specific board environment can be reused on a similar design. This simplifies and shortens the time required for future designs.

In the typical debug sequence, the arbitration is debugged first. Then, simple reads and writes are added. The next sequence involves more complex operations, such as read-modify-write or bus-contention issues with programmable interrupts. Then, if the design is functioning properly, more boards can be added to the system to load it down with as much stimuli as possible to check for other glitches.

The model contains programmable input and output pins to supply additional control over the model's flow of operation. Included is support for set up, hold, pulse width, and other kinds of timing checks on the bus operations, giving users maximum feedback about what's happening in the design. The model's arbitration is completely configurable. After inserting some of the initial required functions, such as arbitration and timing, other pieces can be added incrementally.

Here's where the model's flexibility comes into play. It can be tailored to specific VME design requirements. Multiple copies of the model can be combined to build a system for simulation. But each model can only have one master and one slave executing from a particular piece of code. If multiple masters or slaves are desired, another copy of the model must be built and integrated into the simulation *(see the figure)*. In this configuration, all the models can interact together. The system can be as large as is needed to simulate the design and development. An entire VME environment can be created to drive a board-level simulation. The environment can be flexible enough to fit specific needs.



WHEN MORE THAN ONE master or slave is required in a system, the SimuBus model must be copied. Each model can only have one master and one slave executing from a particular piece of code.

PITFALLS WITHOUT SIMUBUS

Without SimuBus, designers might skip the simulation portion of the board design and deal with any problems arising in the prototype stage. When this happens, functional interaction problems could be confused with physical issues such as capacitive loading or EMI. Or, they could create the stimuli manually. Because this is so difficult, designers often stop short of completion.

A third option is to completely model everything else in the system. Previous designs could provide sufficient data to support a system-level model, but even then, it's often difficult to simulate the entire system. With SimuBus, users just set up the bus cycles that will appear. This offers the maximum flexibility over the bus's conditions and capabilities.

SimuBus adheres to IEEE Standard 1014-1987, meaning that it supports system, master, and slave segments. System segments include the arbitration and timing capabilities. Master and slave boards can be represented by models, enhancing the capabilities for the VME environment. SimuBus supports simple VME operations such as read and write, and some complex operations including interrupts, read-modify-write, and block reads and writes.□

PRICE AND AVAILABILTY

SimuBus is available now. For single users, it costs $10,000; a site license costs $25,000. SimuBus runs with simulators from Mentor Graphics, Valid Logic, and Cadence. During the next few months, Logic Automation says that SimuBus will operate with any simulator that supports the company's behavioral models.

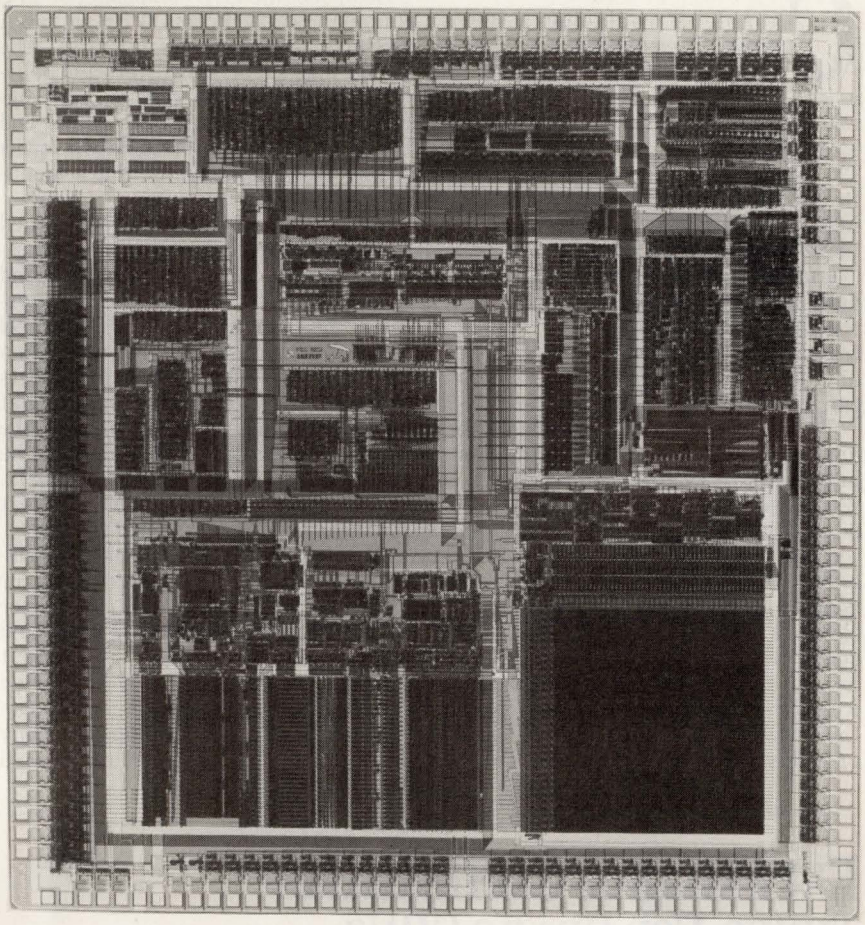
Logic Automation Inc., 19500 N.W. Gibbs Dr., Beaverton, OR 97006; (503) 690-6900. **CIRCLE 514**

HOW VALUABLE?	CIRCLE
HIGHLY	571
MODERATELY	572
SLIGHTLY	573

HIGHLY INTEGRATED 29000-FAMILY MEMBER TARGETED FOR IMAGING CONTROL

DAVE BURSKY

Unlike other RISC CPUs that have on-chip caches and are targeted for embedded control applications, the first highly integrated member of the Am29000—the Am29200—forsakes on-chip RAM or RAM. Instead, to the 29030 core CPU, AMD designers add a video interface aimed at direct connection to laser-printer engines and raster-input devices. Supporting the video interface are ROM and RAM controllers that supply a glue-less interface to low-cost off-chip ROM, SRAM, or DRAM. Other on-chip resources include a two-channel DMA controller, 16 programmable I/O lines, serial and parallel ports, an 8-input interrupt controller, and a 24-bit timer-counter.



The controller is binary and software compatible with the other existing members of the 29K family and provides a much higher level of system integration than other integer members of the family. Besides imaging applications such as laser printers, fax servers, and optical character-recognition systems, the controller could find homes in a wide range of other applications. Some applications are node controllers in FDDI systems or bridges and routers, compression engines for mass storage subsystems, controllers in PABX systems, and robotics.

Initial versions of the chip will run at 16 MHz, but system performance will depend on the off-chip memory support rather than the clock frequency. For example, in a Dhrystone 1.1 test, with the least expensive memory option—2-cycle ROM (16-bit wide) accesses and 3/2 cycle DRAM accesses (also 16 bits wide) the chip delivers a throughput of about 7.5K Dhrystones. If the best memory implementation is used—a 2/1 cycle burst-mode EPROM (32 bits wide), and a 3/2 cycle DRAM (also 32 bits wide)—the chip delivers a throughput of almost 18K Dhrystones.

Thus, the controller can provide roughly 3, 5, 6, or 8 MIPS, and all without changing the system clock frequency. Just the memory configuration need change—from 16-bit wide to 32-bit wide—and from slow memories that require a wait state, to faster memories that impose no wait states. Aimed at imaging applications, the IC has a an effective address space of 4 Gbytes, but only 304 Mbytes are implemented.

The on-chip ROM controller supports four separate banks of ROM or other static memory, and each bank can be either 8-, 16-, 32-bits wide. The ROM banks appear as a contiguous memory area of up to 64 Mbytes. Similarly, the DRAM controller also directly supports four banks of memory, and each can be a different depth and either 16 or 32 bits wide. The DRAM banks also appear as a 64-Mbyte continuous address space.

To support software and hardware development, the company already has an optimizing C compiler (HighC29K) with assembler, linker, ibrary functions, and an architectural simulator. To make the chip and the systems containing the chip easier to test, AMD also include an IEEE 1149.1-compatible (JTAG) test port.

Samples of the Am29200 will be ready in the first quarter of 1992. The chip will be housed in a plastic quad-sided package, with a pin-count that depends on features bonded out. Price for the initial 168-pin version of the chip is about $40 apiece in lots of 10,000. Exact pricing will be announced at time of sampling.

Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, CA 94086; (800) 292-9263 or (512) 462-5651. **CIRCLE 455**

SINGLE-CHIP VIDEO ENCODER SIMPLIFIES RGB-TO-VIDEO CONVERSION

Capable of replacing a large board filled with mixed-signal circuitry, the Bt858 video encoder is the first chip that can convert high-resolution computer graphics (up to 24-bit RGB data) into composite video for TV sets or video tape recorders. The Brooktree encoder chip allows the system to offload desktop video presentations to either NTSC or PAL television standards, or VHS recording standards. Programmable registers allow the chip to switch, under software control, among all the standards without any hardware changes. So one system can handle most needs worldwide.

The video encoder chip merges the digital signals generated by the computer into the desired composite-video waveform. The Bt858 is aimed at studio-quality video and provides a signal-to-noise ratio of between 50 to 62 dB and a bandwidth of about 5 MHz. To achieve studio quality, the encoder includes a triple 10-bit digital-to-analog converter, with each converter containing its own 256-by-10-bit RAM. A 15-word-by-24-bit overlay RAM is also on the encoder. On the output, the encoder provides a four-field 525-line NTSC or 8-field, 625-line PAL composite, or Y/C (luminance and chroma) VHS signal. A slightly lower-resolution unit, the Bt855, packs 8-bit converters and delivers consumer-grade results, with signal-to-noise ratios of 43 to 50 dB and bandwidths of about 4 MHz. In terms of pins and functions, the chip is identical to the Bt858.

Both the Bt858 and 855 are designed to eliminate the incompatible pixel ratios that exist between computers and broadcast video images. In digital systems, the general aspect ratio of pixel width to pixel height is 1:1, while on a TV the ratio is 3:4. The 3:4 ratio distorts the computer-generated image that uses square pixels. To compensate, the chip contains a video clock that can be varied over a range of 12 to 18 MHz. Consequently, the designer can adjust the rate and adjust the pixel shape.

Able to accept either 24-bit RGB color inputs or YCrCB format (4:4:4 or 4:2:2) signals, the encoders can deliver outputs for NTSC, PAL, S-VHS, and RGB. Through software, the output can be configured for any supported standard. Thus, a single board can serve most of the world markets. Only digital data, a clock, power, and ground signals are needed by the chip to do the encoding. Video timing control can be supplied to the chip using horizontal and vertical sync, composite sync, or the CCIR601 H, V, and F control signals. The chip even contains a color-bar generator that allows the system user to calibrate downstream end-user video equipment without an expensive video-signal generator.

The incoming video data is converted to either YIQ (for NTSC operation) or YUV (for PAL systems) signals. The color difference signals are digitally low-pass filtered to 1.3 MHz and then modulated. The rise and fall times of the synchronization signal, as well as the burst envelope and video blanking, are internally controlled to be within composite video specifications.

The CMOS chip dissipates about 900 mA when powered from 5 V. The company has a desktop video-development system that helps designers evaluate a part without purchasing frame buffers or other chips.

In quantities of 100, the Bt858 sells for $67 apiece in a 132-lead plastic quad-sided flat package. Samples are available now. Price and availability for the 855 have not been set.

***Brooktree Corp.**, 9950 Barnes Canyon Road, San Diego, CA 92121; Tom Kovanic, (619) 452-7580.* CIRCLE 456

■ *DAVE BURSKY*

EXPANDABLE CACHE RAMS TUNED FOR SPARC CPUS

Designed to interface with Sparc-processor-family buses, the Pioneer Semiconductor PI2C158 synchronous static RAM is the first cache RAM that readily allows caches up to 256 kbytes. Previous cache RAMs for the Sparc family limited cache expansion to 64 kbytes. The 16-kword-by-16-bit SRAM includes two extra pins that are no-connect pins on other commercial cache SRAMs such as the CY7C157 from Cypress Semiconductor Corp. or Pioneer's own PI2C2157 drop-in equivalent chip.

The two extra pins replace two no-connect pins on the 52-lead plastic leaded chip carrier used for either memory. Those two pins are used as Chip Select lines so that up to four banks (each consisting of two PI2C2158s) of memory-chip pairs can be addressed. If the chip is inserted into a site that previously held the C157 and had the two pin-sites used as tie points, the chip automatically configures itself to act like the PI2C2157 until the two Chip Select lines are free.

With a clock-to-output delay of just 20 ns, the chips are well suited for use with 40-MHz Sparc processors. Faster, 15-ns devices, are being planned for even faster processors. The RAMs have a simple write cycle since a single clock controls the address input registers, byte-write enable registers, and the data input and output latches. The falling edge of the clock triggers the dual-byte Write Enable.

Powered from 5 V, the RAMs consume about 250 mA maximum. In lots of 100, the 20-ns PI2C2158 sells for $58 apiece. Samples are available now.

***Pioneer Semiconductor Corp.**, 3032 Bunker Hill Ln., Suite 103, Santa Clara, CA 95054; Joe Kraus, (408) 748-2169.* CIRCLE 457

■ *DAVE BURSKY*

SINGLE-CHIP CONTROLLER DOES CLOSED CAPTIONS

A single-chip controller, the Z86128, can meet all the Federal Communication Commission specifications for closed-caption, line 21 controllers. The biCMOS, single-chip controller uses scan line 21 to display the encoded information. The chip can be used in set-top decoders too, requiring only the composite video and any horizontal timing pulse and can service many current TVs. Operating mode control, such as turning the decoder function on or off, determining which language to decode, or electing the caption or text display, can all be done either using the chips parallel or serial interfaces. Attributes such as color, underline, italic, and flash are controlled on a character basis along with the on-chip font ROM. Text can be displayed with up to six colors plus monochrome. The controller comes in an 18-pin DIP and in lots of 10,000 sells for $4.18 apiece.

Zilog Inc., 210 East Hacienda Ave., Campbell, CA 95008-6600; (408) 370-8000. CIRCLE 458

MULTIBUS II FAMILY GROWS

A host of Multibus II products are being added to an existing family. In some cases, they offer an easy upgrade path from a 386-based board to a 486 version. The products include an Ethernet card, a communications controller, an interface board, a terminal controller, and a controller board.

The CL 486/296 supplies an Ethernet interface using a 32-bit 596 LAN coprocessor and a Cheapernet interface for point-to-point applications. The CC 486/258 supplies eight high-performance serial channels, each with full-duplex DMA and modem control, and can achieve data rates of up to 2.5 Mbits/s, synchronous. The CC 386/11W offers a high-speed parallel DMA link between Multibus II and DEC computers. Based on a 12.5-MHz 186 CPU, the TC 186/016 supplies 16 asynchronous serial channels supporting data rates up to 19.2 kbaud. Lastly, the IO 386/16X uses a 16- or 20-MHz 386SX microprocessor to control various I/O and memory interfaces including DRAM, EPROM, flash EPROM, and battery-backed RAM. Further expansion is available through an iSBX connector.

***Concurrent Technologies Inc.**, 701 Devonshire Dr., Champaign, IL 61820; (217) 356-7004.* CIRCLE 592

■ *RICHARD NASS*

CONTROLLER ALLOWS CUSTOM KEYBOARDS

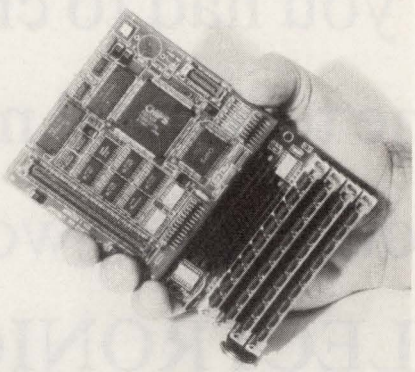
A series of off-the-shelf keyboard controllers can save months of development time. Serving as standard interfaces to custom keyboards and keypads, the KeyCoder implements the IBM-standard keyboard communication protocol by linking a switch matrix of up to 144 keys to a PC-compatible system. It plugs directly into the computer's keypad port. In this configuration, no hardware modifications or software drivers are required. For example, KeyCoder permits input from a custom keyboard to be read by the PC as regular keyboard input. This enables software to be developed independently of keyboard specifics and to be loaded to the target system without any change. The board costs $99.50, with large-quantity discounts available. An evaluation kit is also available.

USAR Systems Inc., 568 Broadway, Suite 405, New York, NY 10012; (212) 226-2042. CIRCLE 593

80386SX SINGE-BOARD COMPUTER OCCUPIES JUST 4 BY 6 IN.

Taking up just 4 by 6 in. of space, Little Monster II from Zykronix Inc. is a single-board computer (SBC) built with a 20- or 25-MHz 80386SX CPU. It's coupled with up to 16 Mbytes of RAM. The board features an IDE hard-disk interface, a floppy-disk controller, dual RS-232 serial ports, and a parallel port. It's suitable for embedded applications due to its low power consumptopn (less than 2.5 W at +5 V) and extened operating temperature range (–20° to +70°C).

The computer comes with an ISA—compatible Zykro-Bus for expansion. Up to eight plug-in modules can be stacked directly on top of the Little Monster II. Zykronix offers a family of expansion cards including VGA graphics, a SCSI controller, an Ethernet adapter, and a PCMCIA memory-card adapter. Without RAM, the single-board computer sells for $889. A development package with 2 Mbytes of RAM, a VGA expansion module, cables, and documentation costs $1695.



***Zykronix Inc.**, 2060 South Xanadu Way, Suite 220, Aurora, CO 80014; (303) 751-7832.* CIRCLE 591

■ *RICHARD NASS*

If you had to choose only
one technical magazine...
Your choice would be
ELECTRONIC DESIGN.

...FIRST with new technology
...FIRST with Ideas for Design
...FIRST with new products
...FIRST on your must-read list

ELECTRONIC DESIGN . . .
Written by engineers for engineers, worldwide

BOARD MONITORS PC'S POWER

The quality of power that's administered to a PC can be monitored with the PC PowerProbe. The add-in card detects power-related failures and bad power supplies in any PC/AT or EISA-based system. Once installed, the PowerProbe monitors the system's internal power supply to determine if it's operating within specifications. The card detects any disturbances and displays the power status on an LED array that's visible from the back of the system. The board sells for under $300. Large-quantity discounts are available.

Applied Physics Inc., Purdue Research Park, 1291-E Cumberland Ave., West Lafayette, IN 47906; (317) 497-1718. CIRCLE 463

68040 SBC SUPPORTS 32 MBYTES OF DRAM

With an architecture that supports up to 32 Mbytes of dual-ported DRAM and an 8-kbyte internal cache, the MZ 7140 single-board computer is suited for power-hungry or real-time VME applications. The board is built with a 25-MHz 68040 processor with internal floating-point and memory-management support. I/O capabilities built into the 7140 include SCSI and Ethernet interfaces, two RS-232 serial ports with internal FIFO buffers, and a Centronics-compatible 8-bit parallel port. The board supports SCSI scripts, a high-level command-chaining language, that lets SCSI operations run faster and with less processor involvement than with traditional intelligent host adapters. The MZ 7140 sells for $3495 with 4 Mbytes of DRAM.

Mizar Inc., 1419 Dunn Dr., Carrollton, TX 75006; (800) 635-0200 or (214) 446-2664. CIRCLE 465

AUDIO BOARD OFFERS 64 TIMES OVERSAMPLING

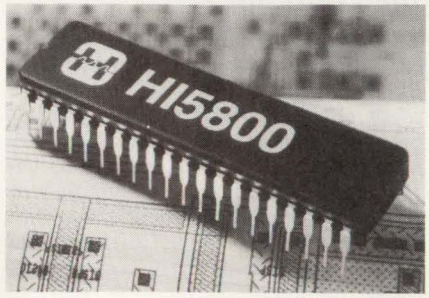
Featuring advanced sigma-delta analog-to-digital converters with 64 times oversampling, the SX-12 is a solid-state, PC-compatible add-in board for direct-to-disk recording and playback of sampled sound. The board is suitable for such applications as broadcast automation, professional audio mastering, post-production work, multimedia, and audio-visual systems. With the SX-12, users can simultaneously record and replay two separate audio channels with full 16-bit resolution at programmable sampling rates from 6.25 to 50 kHz. Tailored to work with any IBM-compatible PC, the board is designed around the Texas Instruments 50-MHz TMS320C25 digital-signal processor. Frequency response is 20 Hz to 22 kHz (±3 dB) with a dynamic range of 92 dB and a signal-to-noise ratio of 90 dB minimum throughout the entire range of sampling rates (6.25 to 50 kHz). Total harmonic distortion is 0.005% in both record and playback modes. The single-unit price is $1695. Large-quantity discounts are available.

Antex Electronics Corp., 16100 S. Figueroa St., Gardena, CA 90248; (800) 266-3092 or (213) 532-3092. CIRCLE 464

12-BIT IC ADC, WITH REFERENCE, SAMPLES AT 3 MHZ

The industry's first 12-bit, IC a-d converter designed to sample its input at up to 3 MHz is now available from Harris Semiconductor. The HI5800 converter, which guarantees no missing codes over temperature, is aimed at a wide range of frequency-domain and time-domain applications now handled by expensive hybrids, including high-speed data acquisition, medical imaging, radar signal analysis, and other jobs requiring spectrum analysis.

Not only does it contain a true, buffered, sample-and-hold amplifier but also has on chip a precision, curvature-corrected 2.5-V bandgap reference.



The latter keeps the maximum full-scale error over temperature below ±2 LSB. It can be used as a system reference, or an external reference can be used. Maximum integral and differential linearity error run ±1 LSB, over temperature.

Like all sampling ADCs, dynamic specifications are supplied. While sampling a ±2.5-V, 500-kHz sine wave at 2.5 MHz signal-to-(noise + distortion) or SINAD, total harmonic distortion (THD) and spurious-free dynamic range typically run –71 dBc, 72 dB, and 74 dB, respectively. Power dissipation is just 2.1 W maximum from ±5-V rails. In quantities of 100, the HI5800 goes for $110 each.

Harris Semiconductor, P. O. Box 883, Melbourne, FL 32901; Gloria Simpson, (407) 724-3739. CIRCLE 466

■ *FRANK GOODENOUGH*

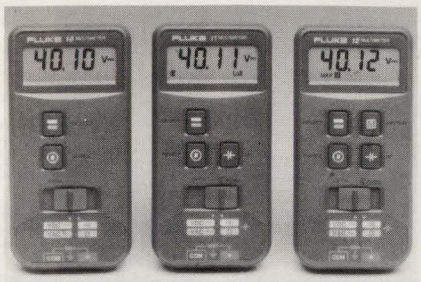
IC SUPPLIES 5 CLOCKS FOR PC MOTHERBOARD

Using multiple phase-locked-loops (PLLs), the AV9128/29 generates (from its single 14.318 MHz crystal oscillator) up to four additional synchronized clocks for a PC's motherboard. The chips, drop-in replacements for the company's earlier AV9127, boast improved performance and functionality. Frequency range has been increased from 80 MHz to 100 MHz; 12 passive components have been brought on chip, and tri-state and additional power-down control inputs have been provided. The latter permits the whole chip, or individual clocks, to be powered down. But the price is up just 25 cents each in OEM volumes. Logic inputs program the four PLL clocks to from two to eight frequencies ranging between 1.8 MHz and 80 MHz. Or the frequencies can be mask programmed for $5000. The standard AV9129 in a 28-pin SOIC goes for $6.80 each in thousands.

Avasem Corp., 1271 Parkmoor Ave., San Jose, CA 95126; Barry Olsen, (408) 297-1201. CIRCLE 467

LOW-COST DMMS OFFER QUALITY, DURABILITY

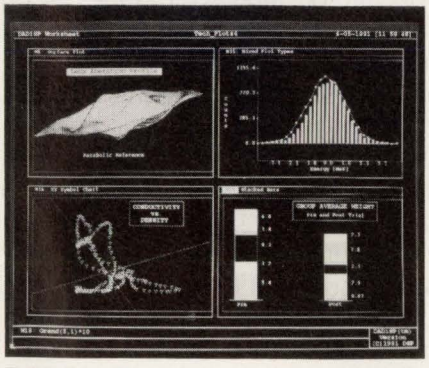
A new series of multifunction, handheld digitial multimeters offers high quality and durability at an economical price. Model 10, the lowest cost unit at $69.95, has a core set of features: volts



ac and dc, continuity and diode test, and resistance. The Model 11, $79.95, adds capacitance measurements. It also features the V-Chek function, an extension of the ohms/continuity mode. When set to V-Chek, the meter tells the user if the circuit is open or continuous, or if voltage is present. If more than 4.5 V is detected, the meter switches from ohms/continuity to volts and displays ac or dc volts, whichever is greater. The Model 12, $89.95, has the same features as the Model 11, plus a min/max recording mode with a relative time clock. This function records the highest and lowest voltages and the time they occurred during a 100-hr. period.

John Fluke Mfg. Co., P. O. Box 9090, Everett, WA 98206; (800) 443-5853 or (206) 347-6100. **CIRCLE 469**

ANALYSIS AND DISPLAY SOFTWARE ENHANCED

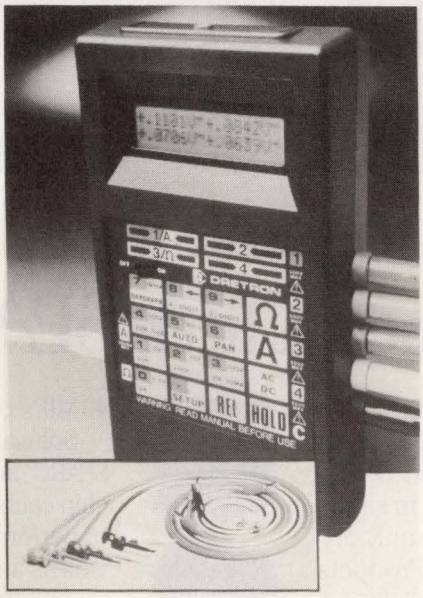


DADiSP Version 3.0 adds many improvements and features to the popular data analysis and display software. New analysis features include error bars on plots, log and log-log plots, and dual data cursors. The package's complement of basic and descriptive statistics has been broadened, and a full range of standard matrix math functions—such as invert, balance, rotate, and others—has been added. Improved graphics features include contour plotting, density plots, XYZ surface plots, spectral 3D plots, 4D plots, and 3D manipulation functions. Other changes enhance the user interface, table manipulation, and hardcopy capabilities. DADiSP runs under X Windows on Concurrent, DEC, Hewlett-Packard, IBM, and Sun workstations and on IBM PC/AT and PS/2 computers and compatibles. DADiSP 3.0 is available immediately at a starting price of $895.

DSP Development Corp., 1 Kendall Sq., Cambridge, MA 02139: (617) 577-1133. **CIRCLE 470**

HANDHELD DMM SCANS FOUR VOLTAGE CHANNELS

A feature-packed handheld digital multimeter includes multiplexed scanning of four input channels. Users can monitor voltage in any of three modes: 4-



channel, 3-1/2-digit display; 2-channel, 4-1/2-digit display; or in a panoramic mode that offers 9-digit resolution on 1 channel. Basic dc accuracy is within 0.2%. Features include autoranging, data hold, relative reference, and a 16-segment bargraph (channel 1 only). Three models include the MM100 with one 200-mA dc-current range ($229.95), the MM100A with one 2-A dc-current range ($229.95), and the MM200 with a 2-A dc-current range and a min-max mode instead of the panoramic mode ($259.95). Delivery is from stock.

HUB Material Co., 33 Springdale Ave., Canton, MA 02021; (617) 821-1870. **CIRCLE 471**

Searching for embedded solutions? Let us shed a little SPARClite.

VISIT BOOTH #1018 AT WESCON

We're blazing a trail for designers of embedded control systems. And now the unparalleled performance, innovation, simplicity and cost efficiency of RISC technology are finally in sight.

Introducing SPARClite.™ A complete family of RISC processors from the Advanced Products Division of Fujitsu Microelectronics. Designed from the ground up for high-performance embedded applications.

Our first SPARClite family member, the MB86930 processor, provides a new generation of solutions that can easily be designed into your embedded applications — for much greater performance at very competitive prices. Operating at clock speeds up to 40 MHz — and providing 40 MIPs peak and 37 MIPs sustained performance.

FUJITSU

Delivering the Creative Advantage.

Software compatible with the industry-standard SPARC® architecture, our MB86930 provides the on-chip cache memory needed to meet the demands of performance-critical real-time routines. As well as a unique cache-locking mechanism and many other on-chip peripheral functions.

What's more, Fujitsu's SPARClite program is complemented by a full range of multi-platform support tools from the leading names in development systems. To help you get to market more quickly than ever before.

So why keep searching in the dark? Call us at 1-800-523-0034. And turn on SPARClite for the best in embedded solutions.

FUJITSU MICROELECTRONICS, INC., Advanced Products Division. 77 Rio Robles, San Jose, CA 95134-1807. Ph: 408-456-1161 Fax: 408-943-9293.
FUJITSU MICROELECTRONICS ASIA PTE LTD. (Head Office, Singapore): Ph: 65-336-1600 Fax: 65-336-1609. HONG KONG SALES OFC: Ph: 852-723-0393 Fax: 852-721-6555.
TAIPEI SALES OFC: Ph: 886-2-757-6548 Fax: 886-2-757-6571. JAPAN SALES OFC: Ph: 81-3-3216-3211 Fax: 81-3-3216-9771. KML CORP. (Rep., Korea): Ph: 82-2-588-2011 Fax: 82-2-588-2017.
PACIFIC MICROELECTRONICS, PTY. LTD., (Rep., Australia): Ph: 61-2-481-0065 Fax: 61-2-484-4460.
FUJITSU MIKROELEKTRONIK GmbH (Dreieich-Buchschlag, Germany): Ph: 06103-6900 Fax: 06103-690122.

CIRCLE 197 FOR U.S. RESPONSE

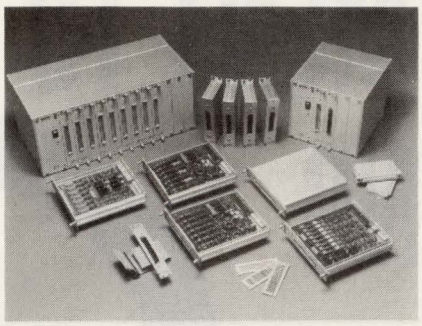
CIRCLE 198 FOR RESPONSE OUTSIDE THE U.S.

EXTERNAL SIGNAL CONDITIONERS UPGRADE PC-BASED DATA SYSTEMS

The performance of data-acquisition systems using PC plug-in boards can be enhanced by a line of signal-conditioning products that work in a mainframe external to the noisy PC chassis. The Signal Conditioning Extensions for Instrumentation (SCXI) products include mainframes, multichannel modules, and cable accessories.

The multichannel modules can be independently configured for different signal types, including thermocouples, strain gauges, resistance-temperature detectors, thermistors, and microvolt, millivolt, volt, 4-to-20-mA, and 0-to-20-mA sources. The system's multichannel cabling and scanning capabilities handle many channels without cabling and connectivity problems. A 4- and a 12-channel mainframe are available, affording a total of 384 channels. Both mainframes have a quiet power supply, an analog bus, and a digital bus for transferring data and control signals. Other modules available are a 32-channel multiplexer amplifier, 8- and 4-channel isolation amplifiers, and an 8-channel sample-and-hold amplifier.

A feedthrough panel simplifies cabling by passing all signals, including those not needing conditioning, from the SCXI front panel to the cable that transfers the signals to the data-acquisition board. Users can design custom SCXI modules with the SCXI-1181 general-purpose breadboard module.



The company will publish the SCXI specification as an open standard so third parties can develop modules.

The 4-slot SCXI-1000 chassis costs $695, and the 12-slot SCXI-1001 chassis goes for $1595. Prices for individual modules, terminal blocks, and other accessories, range up to $1195 for the 8-channel isolation amplifier.

National Instruments Corp. 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100. CIRCLE 472

■ *JOHN NOVELLINO*

VXI CONTROLLERS OFFER RANGE OF PERFORMANCE

A line of C-size VXIbus system controllers makes it easy for users to tailor a test system to their needs. The VX4542 and VX4544 are aimed at low- to mid-range applications. The 20-MHz, 386-based VX4544 is designed for general-purpose measuring, stimulus, and switching applications in which the mainframe uses standard instruments. The 16-MHz, 286-based VX4542 is suitable for applications needing less computation and graphics power. The EPC-2 is a full VXI, VME, and IEEE-488 controller with complete memory-map access and a high-level software toolset for transparent routing of messages. The 20-MHz 386-based system offers super-VGA graphics. All three units support up to 16 Mbytes of DRAM and 200-Mbyte hard-disk drives. The VX4542 costs $4500; the VX4544, $5500; and the EPC-2, $5450.

Tektronix Inc., Test and Measurement Group, P. O. Box 1520, Pittsfield, MA 01202; (800) 835-4894. CIRCLE 473

MULTIFUNCTION DACS OFFER 16-BIT RESOLUTION

A pair of 16-bit IEEE-488.2-compatible digital-to-analog converters offer the capabilities of a precision voltage source, function generator, and arbitrary waveform generator. The DAC488/HR2 (2-channel) and DAC488/HR4 (4-channel) are stand-alone instruments controlled by an independent computer with an IEEE-488 interface. The units' multiple analog output channels use a common update clock generated from four programmable internal sources. The 200-kHz and 5-MHz sources create clock rates from 3 Hz to 100 kHz. The 5.6448-MHz and 6.144-MHz sources generate audio CD-compatible 44.1-kHz and DAT-compatible 48-kHz update rates. Both units feature 500-V dc optical isolation. The DAC488/HR2 and DAC488/HR4 cost $2495 and $3495 each, respectively. Both are available immediately.

IOtech Inc., 25971 Cannon Rd., Cleveland, OH 44146; (216) 439-4091. CIRCLE 474

ELECTRONIC DESIGN

Chairman and CEO: Sal F. Marino
President and COO: Daniel J. Ramella
President, Electronics Group: James D. Atherton

Advertising Sales Staff

Publisher: Paul C. Mazzacano
Hasbrouck Heights, NJ; (201) 393-6060
San Jose, CA; (408) 441-0550

National Sales Manager: Andrew M. Dellins
San Jose, CA; (408) 441-0550

General Manager, European Operations: John Allen
Four Seasons House
102B Woodstock Rd., Witney, Oxford OX8 6DY England
Phone: 0993-778-077 FAX: 44-993-778-246

Hasbrouck Heights: Judith L. Miller, Robert Zaremba
Sales Support Supervisor: Betsy Tapp
611 Route # 46 West, Hasbrouck Heights, NJ 07604;
Phone: (201) 393-6060 TWX: 710-990-5071

Boston: Ric Wasley
400 Fifth Ave., Waltham, MA 02154;
Phone: (617) 890-0891 FAX: (617) 890-6131

Colorado: Lou Demeter (408) 441-0550

Chicago/Midwest: Russell Gerches
Sales Assistant: Susan Johnson
2 Illinois Center Bldg., Suite 1300
Chicago, IL 60601; (312) 861-0880
FAX: (312) 861-0874

Arizona: James Theriault (408) 441-0550

Los Angeles/Orange County/San Diego: Ian Hill
Sales Coordinator: Debi Neal
16255 Ventura Blvd., Suite 300
Encino, CA 91436; (818) 990-9000
FAX: (818) 905-1206

Pacific Northwest: Bill Giller (408) 441-0550

San Jose:
Lou Demeter (408) 441-0550
Bill Giller (408) 441-0550
James Theriault (408) 441-0550
Sales Administrator: Amber Hancock
2025 Gateway Pl., Suite 354
San Jose, CA 95110; (408) 441-0550
FAX: (408) 441-6052 or (408) 441-7336

Texas/Southeast: Bill Yarborough
12201 Merrit Dr., Suite 220, Dallas, TX 75251;
(214) 661-5576 FAX: (214) 661-5573

Direct Connection Ad & DAC Sales Representative:
Jeanie Griffin (201) 393-6080

Canada: Tony Chisholm
Action Communications
135 Spy Court, Markham, Ontario L3R 5H6
Phone: 416-477-3222 FAX: 416-477-4320

Netherlands: W.J.M. Sanders, S.I.P.A.S.
Oosterpark 6-P.O. Box 25
1483 DeRyp, Holland Phone: 02997-1303
Telex: 13039 SIPAS NL Telefax: (02997)-1500

France, Belgium, Spain: Claude Bril
IMS Paris, c/o IDG Communications France
Cedex 65, 92051 Paris la Defense—France
Phone: 33 149 047 900 FAX: 33 149 047 878

Germany, Austria, Switzerland: Friedrich Anacker
InterMedia Partners GmbH
Katernberger Strasse 247, 5600 Wuppertal 1
West Germany Phone: 02-02-711-091/92

Hong Kong: Tom Gorman, China Consultant Intl.
Guardian Hse, Ste 905
32 Oi Kwan Road, Happy Valley, Hong Kong
Phone: 852 833 2181 FAX: 852 834 5620

Israel: Igal Elan, Elan Marketing Group
22 Daphna St., Tel Aviv, Israel
Phone: 972-3-6952967 FAX: 972-3-268020
Toll Free in Israel only: 177-022-1331

Italy: Cesare Casiraghi, Casiraghi Cesare, S.A.S.
Via Cardano 81 1, 22100 Como, Italy
Phone: 39 31 536 003 FAX: 39 31 536 007

Japan: Hirokazu Morita, Japan Advertising Communications
New Gunza Buiding 3-13
Gunza 7-chome, Chuo-Ku, Tokyo 104 Japan
Phone: 011-81-3-3571-8748 FAX: 011-81-3-511-8710

Korea: Young Sang Jo, Business Communications Inc.
K.P.O. Box 1916, Midopa Building 146,
Dangju-Dong, Chongo-Ku, Seoul, Korea
Phone: 011-82-2-739-7840 FAX: 011-82-2-732-3662

Singapore, Australia, New Zealand: Omer Soker
Media Development Ltd., 17B Washington Plaza
230 Wanchai Road, Hong Kong
Phone: 834-5978 FAX: 893-9411

Taiwan: Tomung Lai, United Pacific International
No. 311 Nanking E. Rd., Sec. 3
Taipei, Taiwan R.O.C. Phone: 011-886-27-150-751
FAX: 011-886-27-169-493

United Kingdom: John Maycock
Huttons Buildings, 146 West St.
Sheffield, England S1 4ES Phone: 742-759186

PENTON CONTINUES COMMITMENT TO RECYCLING

Penton Publishing's Camera Department started recycling chemicals from film wastewater 25 years ago... long before the ecologically-smart idea was widely recognized.

For almost as many years, the Penton Press Division has been recycling scrap paper, obsolete inventory, and printing press waste materials. In 1991, Penton Press will recycle some 5500 tons of paper, 9 tons of aluminum plates, and 3 tons of scrap film negatives. Furthermore, the Press Division has invested $500,000 in air pollution control equipment.

Company-wide, the recycling spirit has spread from Cleveland headquarters to offices throughout the country. Penton employees are enthusiastic participants in expanding programs to re-use paper, aluminum cans, and other waste materials.

Penton Publishing believes these practices make a significant quality-of-life difference for people today... and will help create a safer, healthier environment for generations to come.

Penton Publishing

CAD TOOL ANALYZES BIPOLAR DEVICES

GIGA, a time-and temperature-dependent CAD tool, analyzes, designs, and optimizes bipolar-device structures in one or two dimensions. Structures can include diodes, transistors, and thyristors. Users can calculate the non-isothermal dynamic current-voltage characteristics of a packaged rectifier and determine temperature distributions along the structure. Also, the GIGA software helps users estimate the quality of the contacts between different metallic layers of packaged rectifiers to aid in heat-sink design. GIGA accepts an impurity file, device geometry, and information about the cooling package and external circuits. Its outputs include dc and transient performance descriptions, internal parameter distributions, and temperature distributions in the semiconductor structure. GIGA is available now for personal computers and IBM, HP, and Sun workstations. Call the company for pricing.

Silvaco International, 4701 Patrick Henry Dr., Bldg. #3, Santa Clara, CA 95054-1819; (408) 988-2862. CIRCLE 475

VHDL SIMULATOR BOASTS EASY-TO-USE INTERFACE

An easy-to-use graphical interface highlights the VHDL 2000 design-analysis environment that supports the full IEEE 1076 language specification. The system, which is implemented in C++, is completely object oriented. A powerful user interface includes a graphical VHDL design browser; multiple VHDL source display/edit/debug windows for all source-level operations; multiple waveform, tabular, and spreadsheet views of the VHDL signal and variable values; and a graphical what-if expression editor. The hierarchical design browser maintains an aerial view of the design and provides easy access to all the system's functionality. In addition, VHDL 2000 includes a logic analyzer that supports multiple waveform and tabular views, panning and zooming, and signal selection from either the source code or schematics. Pricing for the VHDL 2000 design-analysis environment, which runs on Unix workstations, starts at $40,000. It will ship by the end of the year.

Racal-Redac, 1000 Wyckoff Ave., Mahwah, N.J. 07430; (201) 848-8000. CIRCLE 476

MATH PROGRAM RUNS UNDER X-WINDOWS

Engineers can perform math analysis in the X-Windows environment with the Xmath software. Xmath combines numerical functions, graphics, interactive scripting, and a Motif user interface into an integrated, object-oriented engineering workbench. The software exploits user-interface technology with such features as a spreadsheet-style editor for matrices, point-and-click graphics annotation, on-line hypertext help, and a built-in source-level debugger window for script-based programming. The use of object-oriented technology produces algorithms that are optimized for speed and accuracy. In addition, Xmath generates various plots from data or computations. These plots include 2D scatter plots, 3D surface plots, multiple X and Y plots, and multicurve strip charts. Xmath runs on DEC, HP/Apollo, and IBM workstations. It's selling now for $2495, with discounts available for multiple copies and educational institutions.

Integrated Systems Inc., 3260 Jay St., Santa Clara, CA 95054-3309; (408) 980-1500. CIRCLE 477

ROUTER ENSURES RULE COMPLIANCE

The Graphical Route Editor added to the Crystal V.2.1 pc-board design system lets engineers intervene in the automatic routing process and incorporate special trace configurations without fear of design-rule violation. With the editor, users can make their changes graphically on screen. They select the general path for the router, and it automatically makes all calculations necessary to comply with coupling, impedance, and length rules. Consequently, every wire in the finished route will meet design rules. Besides routing graphically with the Route Editor, users can also manipulate previously routed wires to incorporate design changes. They can move wires from layer to layer, channel to channel, or remove the wires entirely. The Graphical Route Editor is included in the Crystal V.2.1 PCB Design System, which runs on workstations and costs $40,000.

Shared Resources Inc., 3047 Orchard Pkwy., San Jose, CA 95134; (408) 434-0444. CIRCLE 478

USERS CAN DEFINE A DESIGN DATABASE

End users can define a database to intelligently store data for any design environment (electrical, mechanical, software, or packing material) with an application called the Information Modeling Manager (IMM). IMM is part of the Component Information System from Expert Views. Once the database is defined, users can control and view its information with two software tools called ViewMaster and Library Manager. ViewMaster lets users query on any one or a combination of attributes in the database. With Library Manager, users can populate the database and manage the data. No programming or database knowledge is needed to defined the database structure, and users have full control over the appearance of the user interface. Any user-defined database can co-exist with other internal databases, which lets users protect their investments. Information Modeling Manager is shipping now.

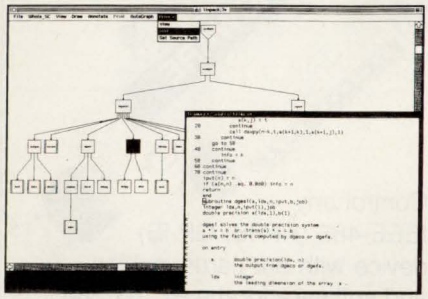
Expert Views Inc., 100 Fifth Ave., Waltham, MA 02154; (617) 890-0333. **CIRCLE 479**

TOOLS HELP OBJECT-ORIENTED PROGRAMMERS

Software developers working in an object-oriented environment will find design assistance in Cadre's Teamwork/OOD CASE tool. Teamwork/OOD consists of a graphical editor, a C++ code-frame generator, a C++ code-capture utility, and an operational interface to the Saber-C++ programming environment. The graphical editor supports OODLE, the company's language-independent graphical notation used by developers to model the architecture of object-based systems while promoting reuse and information hiding. The Teamwork/OOD tools are fully integrated with Cadre's other Teamwork products, including Teamwork/OOA for object-oriented analysis. Teamwork/OOD is shipping now for $2775. It runs on Sun platforms. Cadre offers to Teamwork/OOD users a free course focusing on the proper use of methods essential to managing the complexities of object-oriented languages.

Cadre Technologies Inc., 222 Richmond St., Providence, RI 02903; (401) 351-2273. **CIRCLE 480**

FIND STRUCTURE IN EXISTING FORTRAN CODE



The Teamwork/Fortran Rev reverse-engineering tool graphically reveals the structure of existing Fortran software so that engineers can understand undocumented code, create accurate documentation, identify major components and data structures, and assess the impact of software changes. In addition, because Teamwork/Fortran Rev is tightly linked with the Teamwork family of CASE tools, users will have an easy transition from traditional engineering environments into CASE. Teamwork/Fortran Rev generates Teamwork Structured Design charts from existing Fortran source files. These charts can be displayed graphically, incorporated into documentation, or printed directly. Pricing for Teamwork/Fortran Rev starts at $9700. It will be available on DEC, HP/Apollo, and IBM workstations by the end of the year.

Cadre Technologies Inc., 222 Richmond St., Providence, RI 02903; (401) 351-2273. **CIRCLE 481**

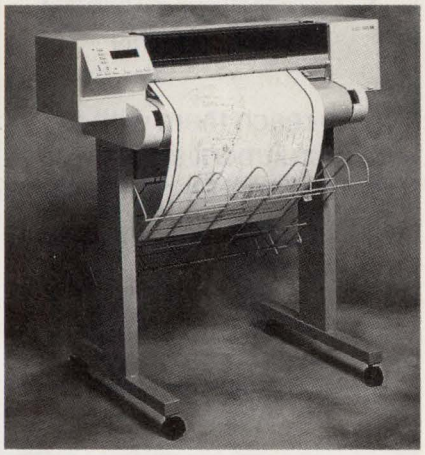
CASE TOOLS DETERMINE SOFTWARE METRICS

SMARTsystem Release 2.0 is a suite of five software-engineering-tool modules for C programmers working on Unix workstations. Besides software-comprehension, development, maintenance, and re-engineering capabilities, SMARTsystem also has metrics capabilities that evaluate the size and complexity of software code to ease engineering decisions. SMARTreport is the add-on metrics package that contains Halstead and McCabe metrics, as well as other counts and selectable preprocessor options. Tailor is the built-in Interface Definition Language that integrates SMARTsystem with external tools. SMARTsystem Release 2.0 will ship by the end of this month. Each module costs $2000, and runs on DEC, IBM, MIPS, and Sun workstations.

ProCase Corp., 3130 De La Cruz Blvd., Suite 100, Santa Clara, CA 95054; (408) 727-0714. **CIRCLE 482**

INK JET PLOTTER PRINTS E-SIZE PLOT IN UNDER 6 MIN.

Based on Hewlett-Packard's DeskJet-printer technology, the DesignJet plotter is a large-format monochrome ink jet plotter that sells for $10,995. At the heart of the plotter is a an Intel i860 embedded RISC processor. As a result, the unit can pump out a 300-dot/in. (dpi), E-size plot in under 6 min. or a 300-dpi, D-size plot in less than 3 min.



Suited for small work groups that use CAD software on PCs or workstations, the DesignJet plotter can be used in a time-saving, draft-quality 300- by 150-dpi mode. Users can fine-tune line differentiation and shading by selecting line widths from 0.2 to 12 mm. Roll media that's either 24 or 36 in. can be accommodated. InkJet film is available in 36-in. rolls. An automatic, one-axis media cutter and an output bin are included for cutting and stacking up to 20 drawings.

The plotter comes standard with Centronics- and serial-interface ports. A modular interface slot is also standard and can accept optional HP interface cards for network or HP-IB connections. Using the optional Ethernet interface card, the plotter can be attached directly to a PC local-area network. The DesignJet should be available by the beginning of next year.

***Hewlett-Packard Co.**, 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900.* CIRCLE 483

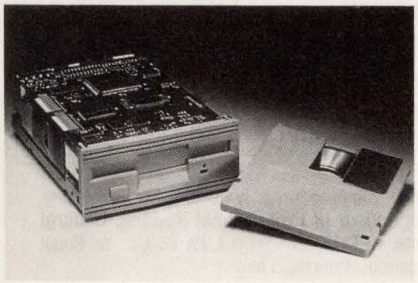
■ *RICHARD NASS*

MULTIFUNCTIONAL OPTICAL DRIVE FITS 3-1/2-IN. FORM FACTOR

Rewritable optical storage that fits in a 3-1/2-in. form factor is available from Teac America Inc. The OD-3000 optical drive features a formatted capacity of 128 Mbytes. The drive features an enhanced 128-kbyte buffer that offers improved system throughput and reduced power consumption when compared to competitive drives. The drive is compatible with both magneto-optical (MO) and optical read-only (OROM) formats.

Teac fit the 3-1/2-in. form factor by using a single-chip CPU that controls all I/O functions, head movement, and operating modes. The drive features an average seek time of less than 42 ms and an average latency of 10 ms. These specifications are achieved by increasing the disk speed to 3000 rpm.

The drive uses just 11 W during read-write operations. Other modes, such as sleep and standby, consume even less power. In addition, a voice-coil motor was used for head positioning to further reduce the power requirement.



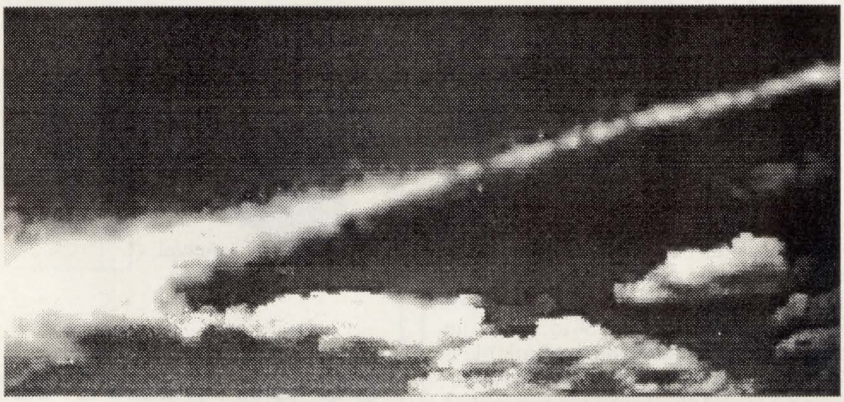
Users can connect the drive using its SCSI II interface. This technology contributes to the drive's asynchronous 2-Mbyte/s transfer rate. The OD-3000's design splits the optical components from the moving element in the head carriage. With the optics fixed in place, the system is subject to less vibration and isn't affected by the higher motor speed. In quantities of 1000, the drive sells for $890. It's available now.

***Teac America Inc.**, Data Storage Products Div., 7733 Telegraph Rd., Montebello, CA 90640; (213) 726-0303.* CIRCLE 484

■ *RICHARD NASS*

EMPLOYMENT OPPORTUNITIES

Engineering



Don't be left behind.

At General Dynamics Fort Worth Division, we're continuing to develop next-generation technologies to increase the F-16's capabilities, and applying them to our new aircraft programs which include the Air Force F-22 (ATF).

The following positions require a BS/MS in EE, ME, AE or Computer Science Engineering, **plus applicable on-the-job technical experience.**

- Ada and OOD
- Aircraft Electrical Power System Design
- Aircraft Lighting Systems
- Aircraft Sub-system Design
- Aircrew Training/ Simulation
- Algorithm Development
- Analog & Digital System Design
- Avionics Circuit Analysis
- Crew Station Design
- Design to Price
- Development Environments
- Electronic Hardware/ Software Design
- Fatigue/Fracture Analysis
- Integrated Diagnostics
- Live Fire Testing
- LSA/LSAR
- Maintainability/Human Factors
- Mathematical/Statistical Model Development
- Mission Analysis
- Operations Research
- Packaging and Installation Design
- Reliability/Systems Safety
- Risk Analysis
- Secondary Power Systems
- Stress Analysis
- Structural Design
- Systems Engineering/ Systems Integration
- Systems Security Engineering
- Weapons Design Integration
- Wind Tunnel/RCS Model Test
- Wiring Installation Design

General Dynamics offers competitive salaries and comprehensive benefits. For immediate consideration, please respond by resume only: **Supervisor of Professional Staffing, General Dynamics Fort Worth Division, P.O. Box 748, Dept. EED02, Fort Worth, TX 76101.** An Equal Opportunity Employer. U.S. Citizenship may be required. Principals only.

GENERAL DYNAMICS
Fort Worth Division

BUSINESS SERVICES

TECHNICAL WITTS, INC. Engineering Consulting Services
Technical Competence High Productivity Reasonable Rates

Power Electronics, Analog, and Digital Circuit Design
Industrial Automation Control System Hardware and Software
Real Time Technical Software, C, Pascal, Windows, MS-DOS, OS/2
Analysis, Requirements Specifications, Design Reviews, Advisement

6319-C W. Villa Theresa Drive
Glendale, AZ 85308
TEL: (602) 439-1833
FAX: (602) 547-1123

HARDWARE AND SOFTWARE DEVELOPMENT SERVICES

- We specialize in developing microprocessor/FPGA based products/systems and embedded software development.
- Custom Windows V3.0 and networking software development.
- Can help with part of or handle the entire project.
- Full Microprocessor Development Systems, I²ICE, CAD/CAM, and PCB layout system.
- Development for LAN, Multibus, VME, PC, MCA, and STD.

Applied Computer Techniques, Inc.
Tel. (407) 851-2525 Incorporated 1978

Looking for
ELECTRONICS ENGINEERS & ENGINEERING MANAGERS?

150,033

Read
ELECTRONIC DESIGN
Twice Monthly

To reach them with a recruitment ad in the Professional Opportunities section

Contact:
Penton Classifieds at 216-696-7000, ext. 2520

Increase Your Profits By Advertising Your Consulting Services in
ELECTRONIC DESIGN
RATES: 6× $125 12× $115
For more information, contact:
Penton Classifieds at (216) 696-7000, ext. 2520.

Don't Wait . . .
FAX YOUR ORDER NOW!

To reserve space, FAX your order to Penton Classifieds,

FAX: (216) 696-1267

Get your technology news where the rest of the world does... first!

Electronic Design: Leader of the pack since 1952

Electronic Design* is the industry's most-often quoted electronics publication.** There's a good reason for this: ***Electronic Design is always the first to report on and describe new technologies as they occur. We're proud of this reputation.

Lots of engineering publications talk about new products, new issues, and new technology. New items are the essence of news reporting.

But when you read about new technology or new implementations of technology in an electronics magazine - *any* electronics magazine - it's likely that the story was first discussed in ***Electronic Design.***

Why do leading manufacturers select ***Electronic Design*** as the vehicle for their significant product introductions? Because they know that ***Electronic Design*** is the ideal environment for their important debuts. Each issue contains the latest information on tools and techniques to help shorten the design cycle, helping our readers to incorporate the latest products and technology into their designs.

Proven leadership in circulation and editorial makes *Electronic Design* *the* source of critical design information for 165,000 global readers. And we're first with the information you need in your job.

After all, why should you wait and read about it somewhere else tomorrow?

YES!
I want my technology news as it happens.

ELECTRONIC DESIGN

YES! I want my technology news as it happens.
Please begin my subscription to *Electronic Design* immediately.

1 year, 24 issues for $85.00.

Name: _____
Address: _____
City: _____ State: _____ Zip: _____

For subscriptions to Canada, add $75.00; foreign subscriptions, add $145.

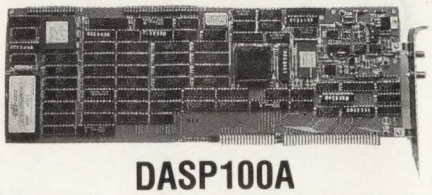
Send to: Penton Publishing, P.O. Box 95759
Cleveland, Ohio 44101; attn: Juanita Roman

ELECTRONIC DESIGN

DIRECT CONNECTION ADS

New Products/Services Presented By The Manufacturer.
To Advertise, Call JEANIE GRIFFIN At 201/393-6080

New!



DASP100A

DATA ACQUISITION & SIGNAL PROCESSING

- ★ 100 MILLION SAMPLES PER SECOND
- ★ 256k SIGNAL MEMORY (EXPAND TO 8 MB)
- ★ 10 MIPS DSP (320C25)
- ★ EXTENSIVE HARDWARE & SOFTWARE SUPPORT
- ★ 3 DATA ACQUISITION MODES
- ★ EXTERNAL CLOCK & TRIGGER

ALSO ASK ABOUT OUR DASP25!

Signatec

357 N. Sheridan St. #119
CORONA, CA 91720
(714) 734-3001
FAX: (714) 734-4356

SIGNATEC CIRCLE 411

FREE! 120 Page Catalog

"Optics for Industry"

ROLYN OPTICS supplies all types of "Off-the-Shelf" optical components. Lenses, prisms, mirrors, irises, microscope objectives & eyepieces plus hundreds of others. All from stock. Rolyn also supplies custom products & coatings in prototype or production quantities. Write or call for our free 120 page catalog describing products & listing off-the-shelf prices. **ROLYN OPTICS CO.**, 706 Arrowgrand Circle, Covina, CA 91722, (818) 915-5707 & (818) 915-5717. TELEX: 67-0380. FAX: (818) 915-1379.

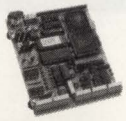
ROLYN OPTICS CIRCLE 412

Instant **Microcontroller**

+

Instant **C**

=



Instant **New Product**

Use our Little Giant™ and Tiny Giant™ miniature microprocessor-based computers to instantly computerize your product. Our miniature controllers feature built-in power supplies, digital I/O, serial I/O (RS232 / RS485), A/D converters (to 20 bits), solenoid drivers, time of day clock, battery backed memory, watchdog, field wiring connectors, and more! Designed to be easily integrated with your hardware and software. Priced from $159. Core modules as low as $59. Low cost, interactive Dynamic C™ makes serious software development easy.

Z-World Engineering

1724 Picasso Ave., Davis, CA 95616 USA
Tel: **(916) 753-3722** Fax: (916) 753-5141
Automatic Fax: (916) 753-0618
(Call from **your fax**, request catalog #18)

Z-WORLD ENGINEERING CIRCLE 405

AIR QUALITY CONTROL

Figaro sensors let you **KEEP IT FRESH:**

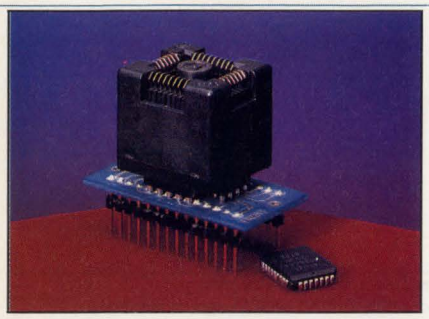
Automatic air cleaning begins with accurate, *continuous* measurement of air quality. Figaro gas sensors are available to meet your most demanding applications.

Write or call for further information:

FIGARO USA, INC.

1000 Skokie Blvd., Ste. 575, Wilmette, IL 60091
Phone: (708) 256-3546 Fax: (708) 256-3884

FIGARO USA CIRCLE 410



PAL/PROM Programmer Adapters

- Any EPROM programmer designed for DIPs can be converted to accept LCC, PLCC, and SOIC sockets in seconds!
- To program, just insert an Adapt-A-Socket™ between the programmer's DIP socket and the circuit to be programmed.
- Designed to fit all types of EPROM programmers, including Data I/O 120/121A, Stag, Logical Devices, etc.
- Quick turnaround on custom engineering services, if needed. For a free catalog, contact:

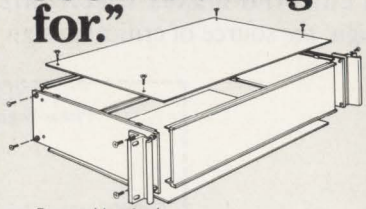
ET

Emulation Technology, Inc.
2344 Walsh Ave. Santa Clara, CA 95051
Phone: 408-982-0660 FAX: 408-982-0664

EMULATION TECHNOLOGY CIRCLE 403

GRAYBOX™
ELECTRONIC INSTRUMENT ENCLOSURES

"Perfect... just what I've been looking for."



- Reasonably priced
- Wide range of stock sizes
- Readily customized by you or us
- Shortens time for prototyping and production
- For literature, pricing, and No-Risk Offer, call:

800-847-3535
Anywhere in the US or Canada

LANSING

LANSING INSTRUMENT CIRCLE 407

Free Circular Connector Catalog from LEMO

LEMO's new circular connector catalog highlights expanded shell and insert designs. Insert configurations are available in single, multi or mixed designs including signal, coaxial, triaxial, high voltage, fiber optic and fluidic/pneumatic. Shell styles are available in standard chrome plated brass, anodized aluminum, plastic or stainless steel.

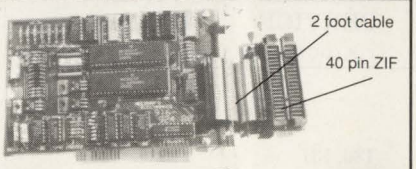
LEMO USA inc
ELECTRONIC CONNECTORS

P.O. Box 11488, Santa Rosa, CA 95406
Phone (800) 444-LEMO Fax (707) 578-0869

LEMO USA CIRCLE 408

EPROM PROGRAMMER

FOR THE PC $139.95



- **2716 to 4 Meg**
- **Programs 2764A in 10 seconds**
  16/32 bit split programming
- Menu driven software
- No personality modules required
- Adapter for 8748, 49, 51, 52, 55, TMS 7742, 27210, 57C1024, and memory cards
- 1 year warranty • 10 day money back guarantee
- Made in the U.S.A.

MasterCard VISA

For more information, call (916) 924-8037
EMPDEMO.EXE available **BBS** (916) 972-8042

NEEDHAM'S ELECTRONICS
4539 Orange Grove Ave. • Sacramento, CA 95841
(Monday - Friday 8:00 a.m. - 5:00 p.m. PST)

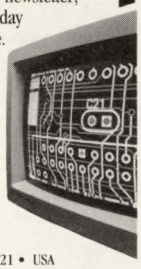
NEEDHAM'S ELECTRONICS — CIRCLE 415

"Tango gives us more than just great CAE/CAD tools."

"We love using every one of the programs in the Tango design suite. But owning Tango tools means more than getting high performance and quality output at an affordable price. It also means getting that extra measure of value with ACCEL's excellent service and support."
Manfred Koch
President, O.E.M. manufacturer

With each Tango design tool for schematic entry and PCB and PLD design, you'll get: thorough documentation; friendly customer service; affordable updates; reliable technical support; BBS; user newsletter; and a 30-day guarantee.

Tango®



See for yourself. Call today for information or a **free** evaluation package.

800 488-0680
619 554-1000 • FAX: 619 554-1019

ACCEL Technologies, Inc.
6825 Flanders Drive • San Diego, CA • 92121 • USA
Contact us for the representative nearest you.

ACCEL TECHNOLOGIES — CIRCLE 406

Instrument Control and Data Acquisition

Free 1992 catalog of instrumentation products for PCs, workstations, and more. Features IEEE-488.2 interfaces and software, plug-in data acquisition boards, VXIbus controllers, DSP hardware and software, and signal conditioning accessories. Application software for complete acquisition, analysis and presentation of data, including graphical interfaces. Application tutorials and training classes also detailed.

National Instruments
6504 Bridge Point Parkway, Austin, TX 78730
(512) 794-0100 (800) 433-3488 (U.S. and Canada)
Fax: (512) 794-8411

NATIONAL INSTRUMENTS — CIRCLE 400

JDR Microdevices®

2233 Samaritan Lane, San Jose, CA 95124

FREE! 84-PAGE CATALOG!

Our new catalog is filled with great buys on thousands of computer products!

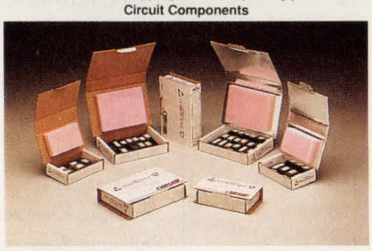
•PCs •Motherboards •Monitors •Drives •Keyboards •Modems •Cables and Connectors •Printers •Software •Programmers •Prototyping products •Test equipment •ICs and Much more!

Call for a free 84-pg. catalog
800-538-5000
Key Code 1524

JDR MICRODEVICES — CIRCLE 409

CHIPSHIP™

For Safely Shipping and Transporting your Circuit Components



These double folded, crushproof, shock and vibration resistant IC mailers with ESD protection are a low cost, time saving solution for transporting small quantities of components. Complete with bonded anti-static foam cushioning and high grade conductive foam inserts, they are available with and without EMI/RFI foil lining.

Model	Size	IC Capacity 8 pin	16 pin	28 pin	40 pin	Features	Prices (10-49)
ChipShip™ **800**	5 1/2" x 3" x 1 1/2"	55	26	7	5	Standard	$ 2.95
ChipShip™ **850**						Foil Lined	$ 3.95
ChipShip™ **900**	6 1/2" x 4 1/2" x 1 1/2"	120	70	19	12	Standard	$ 3.60
ChipShip™ **950**						Foil Lined	$ 4.95

iTOI ENTERPRISES
P.O. Box 59, Newton Highlands, MA 02161
TEL: (617) 332-1010

iTOI ENTERPRISES — CIRCLE 413

PROTÉUS – UNIVERSAL DEVICE PROGRAMMER from $1295*

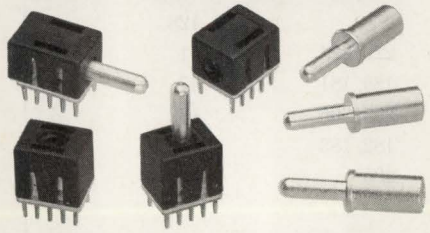
- Programs virtually all **Memory & Logic Devices** on the market
- **40 pins standard**; Upgradeable internally to **104 pins**, and via external adapter module to a total of **296 pins**; DAC generated programming voltages
- Interfaces to any IBM-PC/XT/AT/PS2 **via parallel port** (cable included)
- Optional snap-in **palmtop PC** for stand-alone operation
- User friendly menu driven software with built-in full screen memory, fuse map and test editor; Fully integrated **Algorithm Development Environment** allows users to add parts to the device library or modify existing devices
- Powerful **Macro Language** allows for **Batch Mode Operation**
- True State Machine Testing capability (all pins clocked simultaneously)
- Fully **overcurrent & overvoltage** protected pin drivers (risetime < 100ns)
- Reads / Programs 1MB EPROMs in 10 / 35 seconds (using 16MHz PC)
- **Gang / Set / Split** programming capability; Register preload for logic devices
- Software selectable pin decoupling capacitors and clock sources
- True **100% Hardware Self-Calibration & Diagnostics** via built-in A/D converter with 25mV resolution
- Device insertion detection (detects reversed and shifted insertions)
- Adapter Modules for **GANG, PLCC, JEIDA Cards**; Device Handler Interface
- Additional Adapter Modules and Software Packages allow reconfiguration as **(PCB) Tester, Data Logger, Controller, Programmable Power Supply**

MC / VISA / AMEX * *U.S. list price only.*

B&C MICROSYSTEMS INC.
750 N. PASTORIA AVE., SUNNYVALE, CA 94086 USA
Tel: (408) 730-5511 Fax: (408) 730-5521

BC MICROSYSTEMS — CIRCLE 404

ICCON™



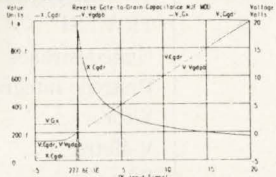
BOARD LEVEL, HIGH-CURRENT CONNECTORS

- High current, low voltage drop
- Power distribution applications
- Board-to-board configurations
- Blind mate capability
- Standard DIP footprint
- Parallel or perpendicular modules

ELCON PRODUCTS INTERNATIONAL COMPANY
P.O. Box 1885, Fremont, CA 94538
PH. (510) 490-4200 • FAX (510) 490-3740

ELCON PRODUCTS — CIRCLE 401

Interactive/Real-Time



ECA-2 *Engineering a Better Way*

Analog Circuit Simulation

- AC, DC, Transient, Fourier, Temperature, MonteCarlo and/or Worst-Case Analysis • Interactive or batch modes
- Full nonlinear simulation •·On-line real time graphics
- Multiple plots • **2 to 50 times faster than SPICE**
- Component optimization sweeping • New 424 pg. manual

All the Features, Twice the Speed at Half the Cost

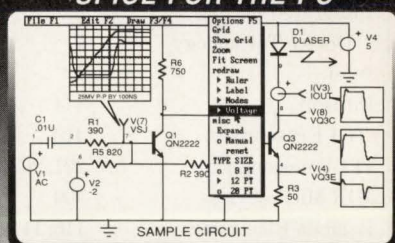
Call for FREE DEMO!

Tatum Labs, Inc.
3917 Research Park Dr. B-1, Ann Arbor, MI 48108
313-663-8810

TATUM LABS, INC. — CIRCLE 402

Analog Circuit Simulation

SPICE FOR THE PC



- **Schematic Entry • SPICE Simulation**
- **Model Libraries • Waveform Graphics**

Intusoft has it all at an Affordable Price!

INTEGRATED, EASY TO USE SIMULATION ENVIRONMENT, FEATURING:
A powerful SPICE (IsSpice) simulator performing AC, DC, Transient, Noise, Fourier, Distortion, Sensitivity, Monte Carlo, and Temperature analyses, Extensive model libraries, Schematic entry, and Waveform processing. Starting at $95 for IsSpice, complete systems are available for $815.

Call Or Write For Your Free Demo and Information Kit!
Tel. 213-833-0710

intusoft
P.O. Box 710 San Pedro, CA 90733-0710
Fax 213-833-9658

INTUSOFT — CIRCLE 414

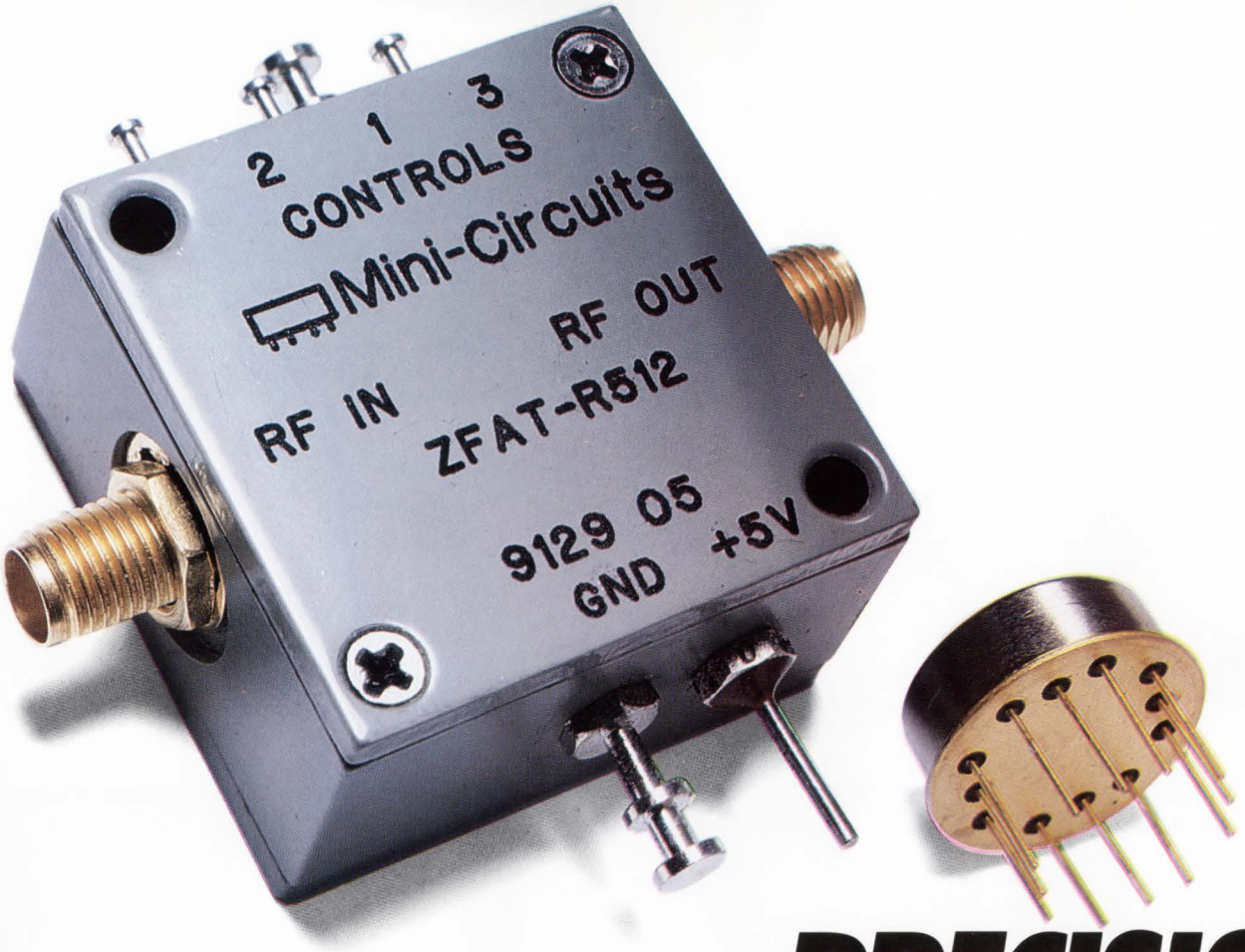
INDEX OF ADVERTISERS

ADVERTISER	READER SERVICE U.S. / OUTSIDE U.S.	PAGE NUMBER
ACCEL Technologies	406	151
Actel	184, 185	86-87
Advanced Micro Device	82, 83	2-3
	186, 187	10-11
	230, 231	74-75
Aerospace Optics	80, 81	132*, 138**
AMP	84, 85	68-69
Analog Devices	220, 221	78-79
Ancot	86, 87	8
	88, 89	137
Apex Microtechnology	90, 91	29*, 125**
Applied Microsystems	92, 93	57
Atmel	228, 229	77
AT&T	96, 97	12-13*
	94, 95	40-41*
	209, 210	92-93*
B&C Microsystems	404	151
Capital Equipment Corp.	98, 99	145
Cybernetic Micro Systems	192, 193	14
Cypress Semiconductor	◊	104A-104H
	◊	Cover IV
Data I/O Corp.	◊	70
Data Translation	100, 101	44
Elcon Products	401	151
Emulation Technology	403	150
Figaro USA	410	150
Frequency Electronics	102, 103	103
Fujitsu	197, 198	142
Gould Test & Measurement	104, 105	52-53*
	188, 189	55*
Harris Semiconductor	211, 212	110-111
	106, 107	127
Headland Technology	216, 217	55**, 95*
Hewlett-Packard Co.	194, 195-196	1
	190, 191	9
	108, 109	117
Hitachi	110, 111	93**, 95**
Hitachi America, Ltd.	112-113	16-17*
Image Watches	3	67
Integrated Device Technology	◊	35
Intel	1	60-61
Intusoft	414	151
iTOI Enterprises	413	151
ITT Semiconductor	201, 202	13**
JDR Microdevices	409	151
Lambda Electronics	116, 117	64A-64D*
Lansing Instruments	407	150
Lattice Semiconductor	214, 215	Cover II
LEMOUSA	408	150
Linear Technology	118, 119	81-84
Melcher	120	19*
MicroSim	122, 123	108
Microsoft	◊	85
Microtek	124, 125	98
Minc, Inc.	126, 127	91
Mini-Circuits Laboratory, a Div. of Scientific Components Corp.	130, 131	15
	128, 129	20-21
	132, 133	104
	134, 135	Cover III
Motorola Semiconductor	◊	58, 59
National Instruments	138, 139	24
	400	151
NEC	140, 141	118
Needham's Electronics	415	151
Nohau	142, 143	140
OKI Semiconductor	◊	125*
OrCAD	144, 145	123
Pacific Hybrid	148, 149	16**, 18*
P-CAD	146, 147	49
Philips Semiconductor	213	17-19**
Philips Test & Measurement	◊	29**, 53**
Pico Electronics, Inc.	152, 153	141, 147
Power Convertibles	226, 227	8
Quad Design	154, 155	121
Quality Semiconductor	156, 157	37
RC Electronics	158, 159	146
Rogers Corp.	160, 161	114
Rolyn Optics	412	150
Samsung Electronics	162, 163	38-39**
Samsung Semiconductor	164, 165	38-39*
SGS-Thompson	234, 235	22-23
Siemens Components	168, 169	6-7
Siemens AG	166, 167	132**
Signatec	411	150
Siliconix	◊	73
Silicon Systems	170-171, 172-173	26-27
Stanford Research Systems	176, 177	32
Stanford Telecommunications	174, 175	67
Tatum Labs	402	151
Team Visionics	224, 225	62
Texas Instruments	◊	30-31
TRW Electronics	178, 179	97
TRW LSI	203, 204	42-43
United Airlines	◊	128
Unitrode Integrated	222, 223	51
Vicor	180, 181	47
V-Metro	205, 206	139
Xilinx	182, 183	88
Z-World Engineering	405	150

* Domestic Advertiser Only

** International Advertiser Only

The advertisers index is prepared as an extra service. Electronic Design does not assume any liability for omissions or errors.



PRECISION TTL- CONTROLLED ATTENUATORS

up to 35dB
10 to 1000MHz

FROM **$5995**

TOAT-R512 ZFAT-R512 Accuracy (dB)	(+/-dB)	TOAT-124 ZFAT-124 Accuracy (dB)	(+/-dB)	TOAT-3610 ZFAT-3610 Accuracy (dB)	(+/-dB)	TOAT-51020 ZFAT-51020 Accuracy (dB)	(+/-dB)
0.5	**0.12**	**1.0**	**0.2**	**3.0**	**0.3**	**5.0**	**0.3**
1.0	**0.2**	**2.0**	**0.2**	**6.0**	**0.3**	**10.0**	**0.3**
1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

Price $ (1-9 qty) TOAT $59.95/ZFAT $89.95

bold faced values are individual elements in the units

Finally...precision attenuation accurate over 10 to 1000MHz and -55°C to +100°C. Standard and custom models are available in the TOAT(pin)- and ZFAT(SMA)-series, each with 3 discrete attenuators switchable to provide 7 discrete and accurate attenuation levels.

The 50-ohm components perform with 6μsec switching speed and can handle power levels typically to +10dBm. Rugged hermetically-sealed TO-8 units and SMA connector versions can withstand the strenuous shock, vibration, and temperature stresses of MIL requirements. TOAT pin models are priced at only $59.95 (1-9 qty); ZFAT SMA versions are $89.95 (1-9 qty).

Take advantage of this striking price/performance breakthrough to stimulate new applications as you implement present designs and plan future systems. All units are available for immediate delivery, with a one-yr. guarantee, and three-sigma unit-to-unit repeatability.

finding new ways...
setting higher standards

Mini-Circuits WE ACCEPT AMERICAN EXPRESS AND VISA

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Telexes: 6852844 or 620156

CIRCLE 134 FOR U.S. RESPONSE **CIRCLE 135 FOR RESPONSE OUTSIDE THE U.S.**

F 140 REV. A

TAKE THE SPEED LEAD.

PAL™ 22V10: 7.5ns.

World's fastest programmable 22V10. Here is the logic for high-performance systems running up to 111 MHz. Set-up is just 3 ns. Fast logic for fast systems. You get the same high speed and low noise with the 22VP10. It offers additional flexibility, including an I/O feedback path to accelerate state machine applications.

BiCMOS. The first BiCMOS 22V10, from the company that delivered the first CMOS 22V10. ECL core path for record-setting performance. CMOS logic outside the speed path, for low power. The speed of smaller PLDs, the convenience of the popular, flexible 22V10 and field programmable too.

The new 7.5 ns field programmable, PLD.

Broad 22V10 PLD family and more. Cypress's 15 ns CMOS 22V10 consumes less power than any electrically erasable alternative. It's just one of a broad range of low-power CMOS PLDs. Also get 28-pin applications-tailored PLDs, and our high-capacity MAX™ PLDs too.

Call Today. Order our PLD Kit and we'll ship it right away. Why wait?

Hotline: 1-800-952-6300.*
Ask for Dept. C3Q.

CYPRESS SEMICONDUCTOR