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ELECTRONIC DESIGN

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JUNE 27, 1991

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- DESIGN-TEAM ISSUES: DESIGN FOR TESTABILITY
- COMBINING IN-CIRCUIT AND SCAN TESTING
- TESTABILITY THROUGH HIERARCHICAL DESIGN

NO INDUCTORS! +5V IN/-5V OUT INVERTER POWERS 100mA LOADS

MAX660 Plus 2 Capacitors Deliver 95% Efficiency

Using two low-cost capacitors, Maxim's new MAX660 charge-pump voltage inverter converts a 1.5V to 5.5V input to a -1.5V to -5.5V output. The charge pump's 100mA output replaces switching regulators, eliminating the need for inductors and their associated cost, size and EMI. For instance, with a 5V input, the MAX660 delivers 100mA at -4.35V. Compact 8-pin DIP and SOIC* packages coupled with a 95% power-conversion efficiency make the MAX660 ideal for battery-powered applications.

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- **10kHz and 45kHz Internal Oscillator**
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- **Voltage Doubler Mode: $V_{OUT} = 2 \times V_{IN}$**
- **1.5V to 5.5V Input Voltage Range**
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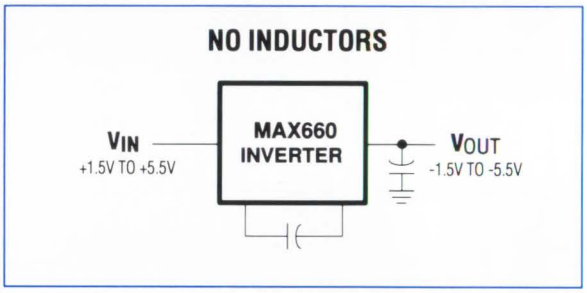
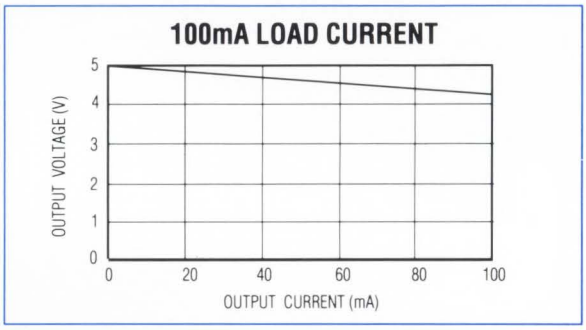
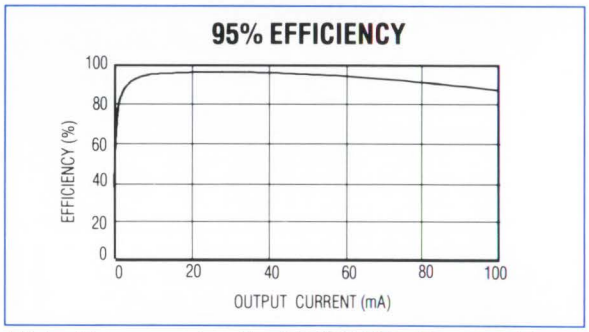


The MAX660 uses only 2 external components and is available in space-saving 8-pin DIP and SO packages.*



Maxim's new MAX660 voltage inverter powers 100mA loads.



High efficiency makes the MAX660 ideal for portable applications.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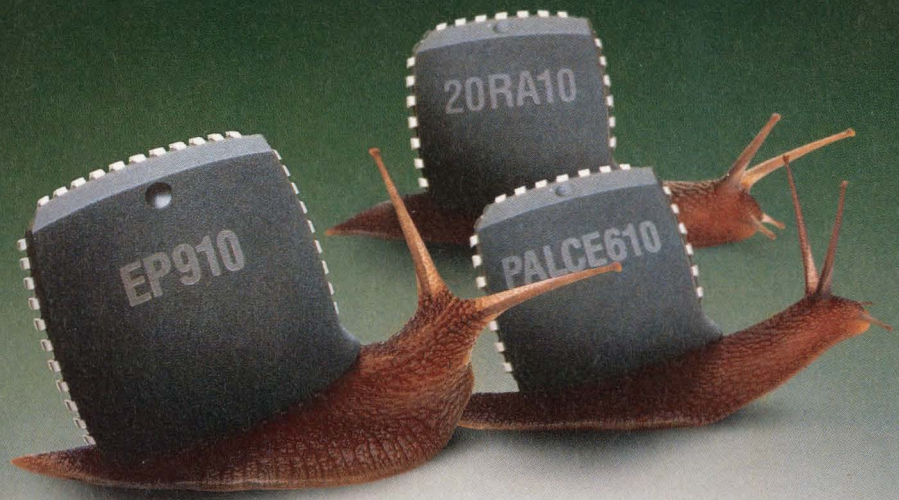
* SOIC packages available after August, 1991 † FOB USA, 1000-up

CIRCLE 183

A question for designers who aren't yet using high-performance µPLDs.



Why the big delay?

Ever feel like your system designs aren't quite up to speed, so to speak? It's probably not your fault. Because PLDs have typically forced designers to sacrifice performance to achieve higher integration.

But not any more.

Now, with Intel's µPLD family of programmable logic devices, you can finally achieve the higher integration you need—with the low total propagation delay you want.

In fact, with t_{PD} figures as low as 10ns, Intel's 16-macrocell 85C060 and 24-macrocell 85C090 are, without question, the fastest integrated PLDs in the industry.

PLD Performance	
PLD	t_{PD}*
Intel 85C060	10ns
PALCE610	15ns
20RA10	15ns
EP610	16ns
Intel 85C090	15ns
EP910	33ns
*Propagation Delay	

So what are you waiting for? Call (800) 548-4725 and ask for Literature Packet #IA81.

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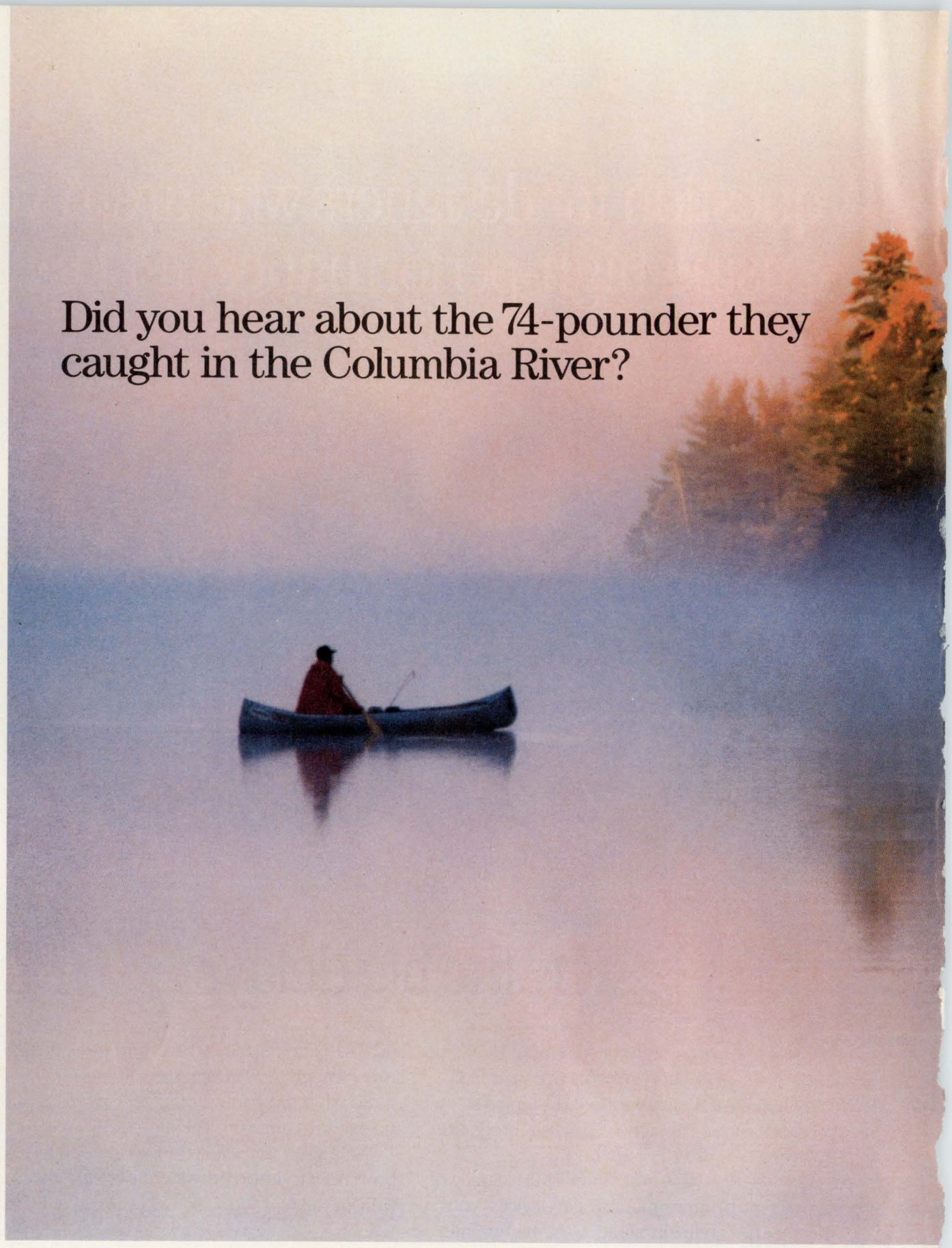
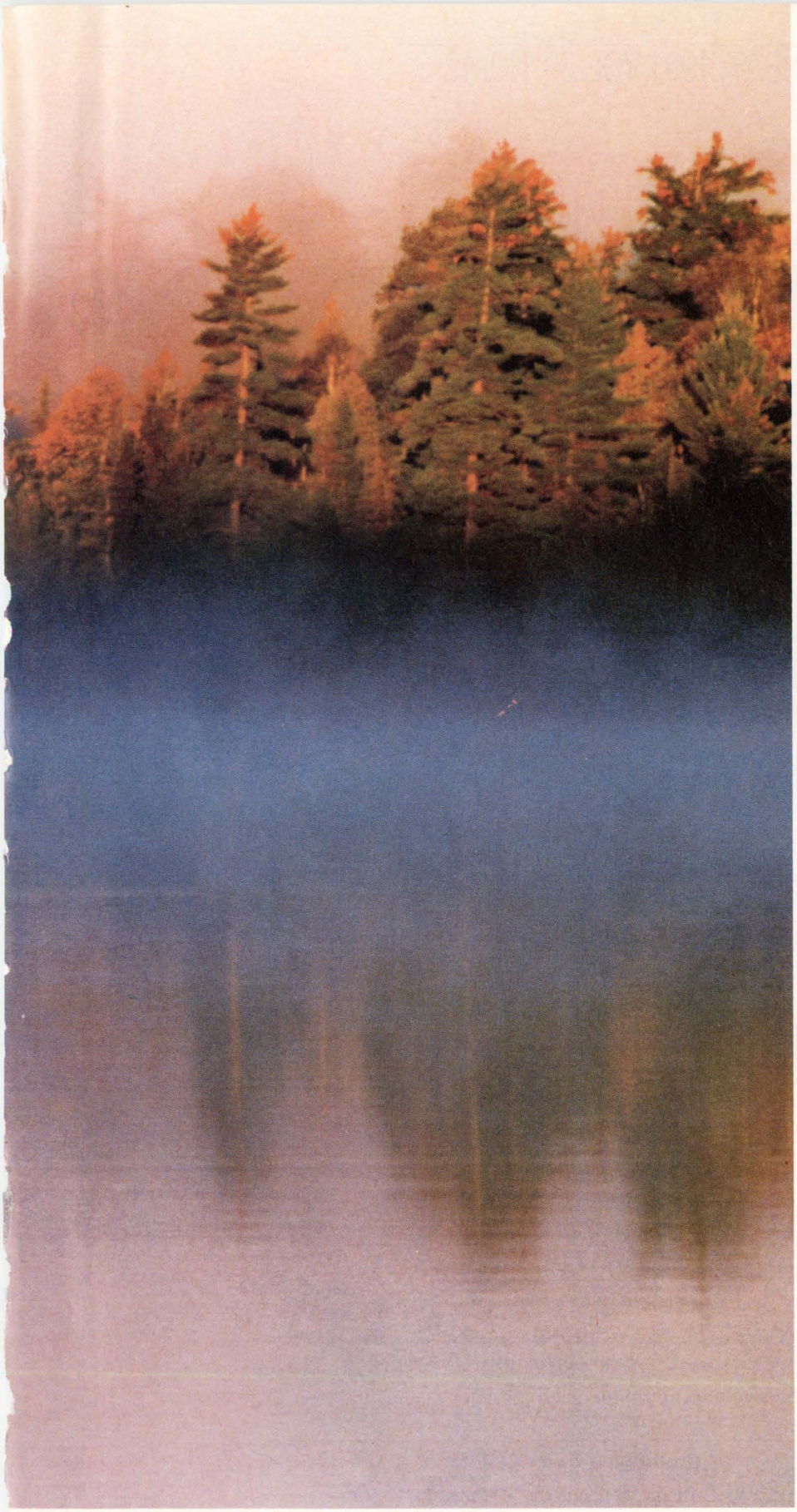
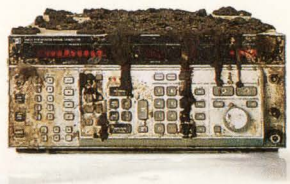






It worked without a snag.

This is a story about the one that got away. And then came back as reliably as ever.

In 1987, bandits stole four HP signal generators from a truck in Spokane, Washington. Luckily, police managed to recover three of them. But the last one disappeared without a trace.

Six months later, a man fishing the Columbia River hauled in a heavy metal box. Well, within a few days, we had the missing signal generator back. There was mud in every nook and cranny.

But rather than clean this catch, one of our Service Engineers decided to plug it in. To his surprise, the instrument emitted a signal. Even more remarkable, it met specifications.

Stories like this underscore why HP rates highest for reliability among engineering managers. We're still not satisfied. In fact, in 1979 we started a Total Quality Control program to increase quality ten-fold in 10 years. We'll reach that goal this year.

It just goes to show you that when design and manufacturing productivity are at stake, there is no reliable substitute for HP. And that sometimes the best fish stories are actually true.

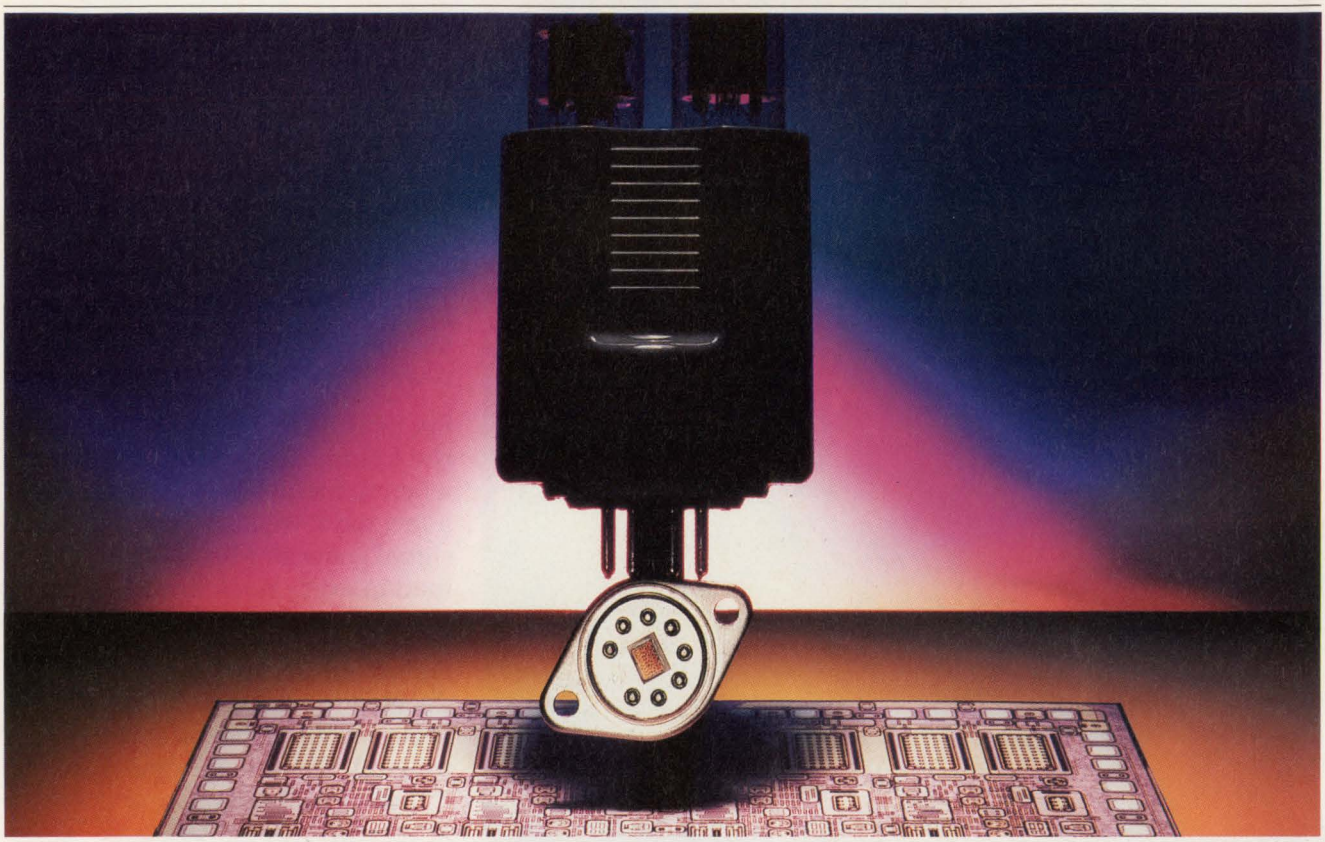
There is a better way.

HEWLETT PACKARD

CIRCLE 164

JUNE 27, 1991 VOL. 39, NO. 12

ELECTRONIC DESIGN



COMING NEXT ISSUE
- Designing cache-memory interfaces for optimum performance
- Special Section: Designing PC Systems
- Boost serial-data throughput with DMA-controlled ports
- Special report: FDDI approaches the desktop computer
- First details on a new network interface IC
- Special Section: Test & Measurement Update
- An overview of digital storage oscilloscopes
- Understanding digital-scope display techniques
- Adding high-power capability to a microcontroller
- PLUS:

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Pease Porridge
Technology Advances
QuickLook

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ON THE COVER:
Apex Technology's new high-voltage op amp. In the background: the classic Philbrick K2 vacuum-tube operational amplifier, which set the standard for high-voltage op amps. Photo by Joe Drivas.

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Now you can really stick it to 'em. And you can be sure they'll get the point. Because our two new MAX® parts will make your next design unbeatable. And get it to market faster.

Introducing Altera's 100-pin EPM5130 and 7500-gate EPM5192. Both packed with I/O and logic unheard of in a CMOS EPLD.

In fact, they're your best programmable alternative to gate arrays yet. Because MAX delivers high logic density and superior 50 MHz *in-system* speed. All thanks to our innovative MAX architecture.

Even design is faster. That's because our new MAX+PLUS® II software takes full advantage of the enhanced memory management and multitasking capabilities of Windows™ 3.0.

MAX+PLUS II can also automatically partition large logic designs into a set of EPLDs. In minutes. So you can deliver your finished design while

S EPLD WITH 100 PINS UR COMPETITION.

your competition's stuck manually partitioning his schematics.

You can even choose from a wide variety of erasable windowed and OTP packages. Including pin grid array, quad flat pack and PLCC package options. Which makes them perfect for full production or gate array prototyping.

Of course, the EPM5130 and EPM5192 are just two members of the modular MAX family. Devices range from 20 to 100 pins, 16 to 192 macrocells. In fact, there's an EPLD for every logic design task. Because we make the industry's broadest line of CMOS PLDs.

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CIRCLE 88

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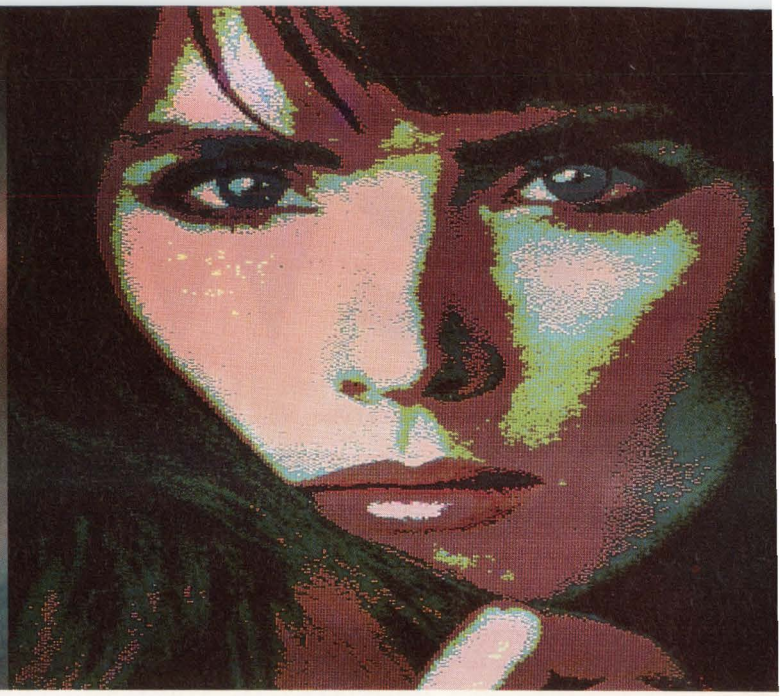
Picture your flat panel display using Cirrus Logic controller chips. They actually add colors to your display capabilities for more realistic shading.



The same panel looks flat without our enhanced VGA capabilities. And it will lose face faster without our optimized power management system.

How To Avoid Losing Face On Your Color LCD Display.

Face it. The first thing everybody notices about your newest laptop is the display quality. Is it bright? Are the images clear and well modeled? Are the colors vivid?

With Cirrus Logic LCD VGA controllers, your answer is yes. Which is why we're the leading supplier of display controller chips in the laptop and notebook market.

For life-like 3-dimensional imaging, Cirrus Logic color LCD controllers offer technology leadership for your color products. With direct support for the latest active-matrix color LCD panels. Our controller chips do more than support your panel's color capabilities — they enhance it with full VGA color support and a fuller color palette. To give you color so good it competes with CRT quality.

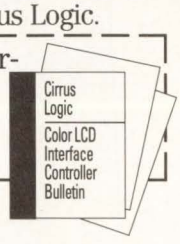
Our monochrome solutions give you displays that *PC Magazine* called "the stars of our VGA color-mapping tests"* with up to 64 shades of gray. And with a lower dot clock rate, your power consumption is lower than other solutions for longer battery operation.

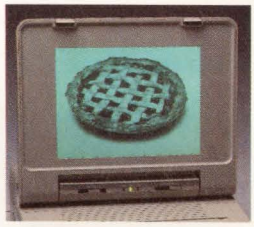
Cirrus Logic LCD controllers are fully compatible with the popular PC video standards and will work with LCD, plasma, or electroluminescent displays.

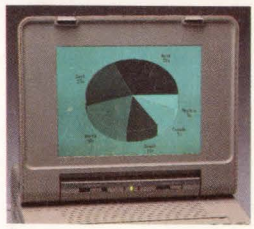
Simplify your design job. A higher level of integration gives you all this in the smallest form factor available. We also supply software and hardware design notes and full design support. You get the results you want quickly and easily.

Design a more competitive product. One that looks better — and makes you look better. That lasts longer on a battery. Use the display solutions from a proven technology leader in laptop and motherboard VGA: LCD controller chips from Cirrus Logic.

Get the picture. Get more information on LCD controllers.
Call 1-800-952-6300, ask for dept. LL34







Cirrus Logic monochrome LCD controllers will also make everything from realistic scanned images to business charts look tastier.

CIRRUS LOGIC

C L O S I N G T H E G A P

 * PC Magazine, March13,1990, p. 204.

News Flash

SPORTS

The 90 Nanosecond Workout
An Exhaustive Look At High Tech Training Equipment
PAGE 2B

SCIENCE AND TECHNOLOGY

Virtual Reality
Close But No Cigar
PAGE 8H

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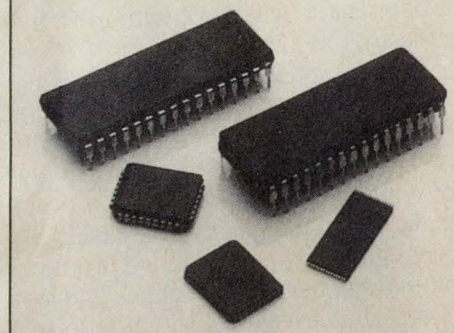


How Fast Is A Flash? A Direct Comparison

Density	AMD	Fastest Competitor
256K	90ns	120ns
512K	90ns	120ns
1 Mbit	90ns	120ns
2 Mbit	90ns	150ns

AMD Ships 2 PLCC Flash

SUNNYVALE — The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc.

Flash memory is a high-density, reprogrammable, non-volatile technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications.

Flash memory also has the potential to eliminate mechanical hard disks and the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook computer applications.

Today, Flash memory is the most cost effective replacement technology for UV EPROMs and EEPROMs in applications that require in-system programming. Flash memories can literally be reprogrammed in a flash — hence the name.

Standard, But With A Little More Flash

AMD's Flash memory family effectively etches in silicon the de-facto standard for this burgeoning technology that is compatible with Intel's initial Flash architecture.

Because AMD Flash memories are pin-for-pin compatible with the now standard architecture, AMD is positioned as an alternate source for design engineers and purchasing agents alike.

"Alternate source may be an inadequate term," said Jerry Sanders, chairman and CEO of Advanced Micro Devices. "Given our speed and feature set, our customers think of us as a superior resource."

Indeed, AMD's Flash memory family offers designers significant performance advantages (see chart), with speeds almost twice as fast as the nearest competitor.

Engineer Spontaneously Combusts At Meeting

Vice Pre

From AMD.

Stop the presses!

Advanced Micro Devices makes big news again—this time with an enhanced family of Flash memory devices.

That's good news for veteran and new Flash users alike.

Because our Flash devices are pin-for-pin compatible with Intel's existing Flash memory architecture, they establish the *de facto* industry standard.

Our standards, however, are a bit higher.

And so are yours.

That's why our Flash Memory family offers densities, speeds and packaging options that improve performance and save board space. For instance, our advanced 2 Mbit PLCC part with a scant 90 nanosecond delay.

You can also choose from Flash devices in 256K, 512K and 1 Mbit densities. As well as packaging options that fit your design best, including CDIP, PDIP, LCC, TSOP, and PLCC.

And you'll find implementation faster and easier than ever, because we've included automatic programming algorithms on all our 2 Mbit devices, and soon on our 1 Mbit parts, too. So you'll spend less time writing code, and take less time getting products to market.

To keep up to date with all the latest and greatest in Flash memory, call AMD today at **1-800-222-9323.** And start making some headlines of your own.

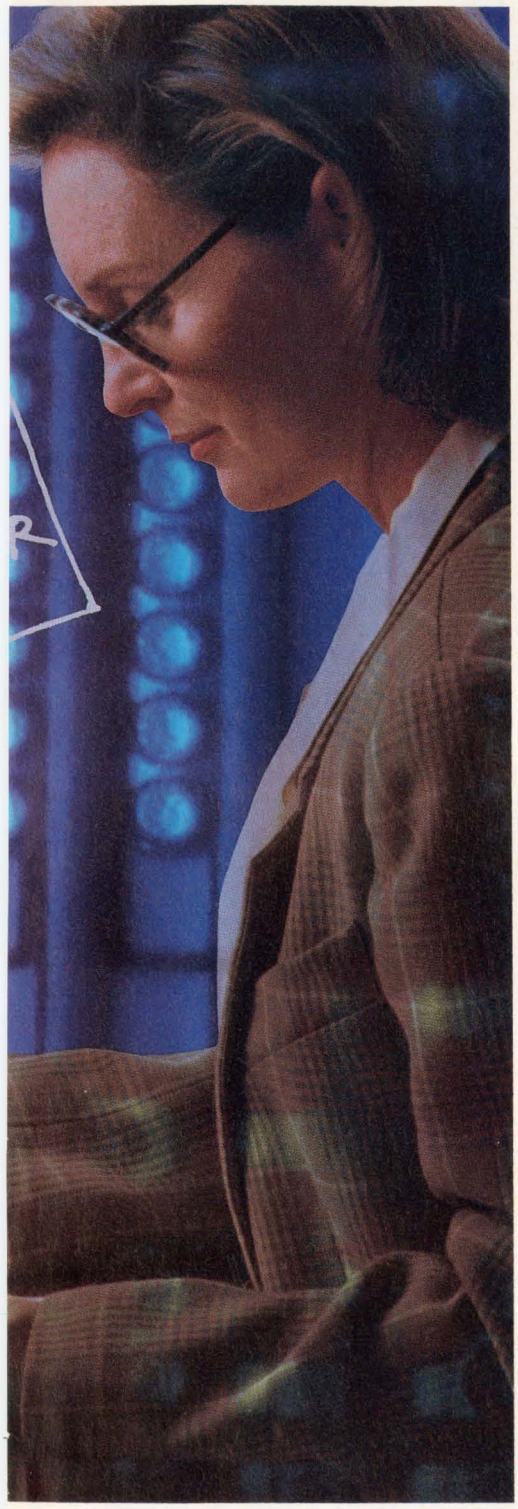
Advanced Micro Devices

CIRCLE 180

Making mighty modems micro.

That's AT&T

"Customer*izing*."



"Customerizing" means helping you develop fast, compact, low-power V.32 modem solutions—with the high-level integration needed for laptop/portable applications. The AT&T V.32 Data Pump consists of only three surface-mountable devices: A single DSP16A digital signal processor—ROM-coded with software to handle receive, transmit and echo cancellation—complies with the V.32 standard, and is compatible with V.22bis, V.22, V.21, V.23, Bell212A and Bell103; a 16-bit linear codec allows for fully digital echo cancellation; and a controller chip integrates CPU bus interface and line interface circuitry. The 0.9 micron CMOS design draws less than 0.5 watt, versus 1.5 to 2 watts in many competing products. Sleep-mode function takes power consumption down to 50 mW. And to speed design-in, EIA/TIA Automode is built into the solution. In addition, your Data Access Arrangement (DAA) can utilize AT&T high-performance solid state relays and transformers. For more on how AT&T "Customerizing" can help you develop better V.32 modem or other datacomm solutions, just give AT&T Microelectronics a call at **1 800 372-2447, Ext. 626.** In Canada, call **1 800 553-2448, Ext. 626.**

AT&T
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CIRCLE 84

DESIGN FOR TESTABILITY

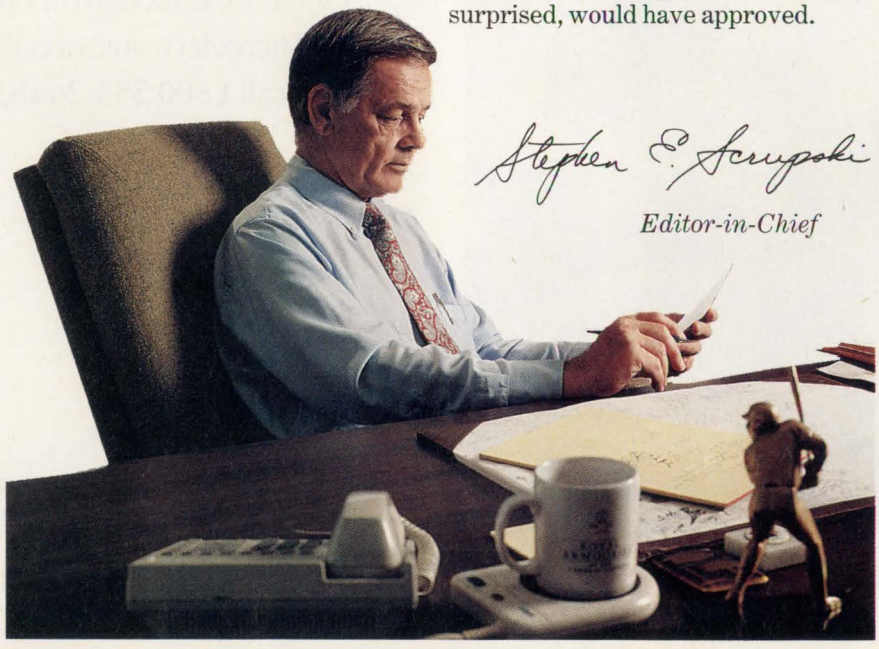
"When you can measure what you are speaking about, and express it in numbers, you know something about it; but when you cannot measure it, when you cannot express it in numbers, your knowledge is of a meager and unsatisfactory kind;..." I know that this quotation, from William Thomson, Lord Kelvin, has been cited previously in this column. But it's worth repeating, particularly in this issue, with its focus on design for testability (see the two articles, which begin on pages 75 and 89).

This idea–unless you can measure something, you don't know anything about it–may seem unduly narrow for anyone not trained in a scientific discipline. But for engineers, it cuts to the heart of the tasks that face them every day. If you can't measure the performance of the system you're designing under all possible conditions, you can't be sure that it will operate reliably.

In a similar vein, testing a digital system for faults is getting more difficult with every advance in semiconductor technology–each increase in circuit density creates nearly an exponential increase in testing difficulty. If you can't control and observe a circuit's internal nodes, you really don't know anything about its faults and their causes. The rapid rise in VLSI circuit complexity stimulated the formation of the Joint Test Advisory Group (JTAG), whose efforts are now embodied in an IEEE specification, 1149.1. Without a scheme like scan-based testing, you would have to spend half a career to develop a program to fully test a system you have designed with the latest VLSI devices.

What exacerbates the situation is the growing pressures created by time-to-market considerations. This problem stems from the same roots–rapid advances in VLSI. These advances cause overlapping generations of equipment, which shorten product lifetimes and thus demand early market entry for product success. One result of this phenomenon is that designers must adopt design-for-testability approaches.

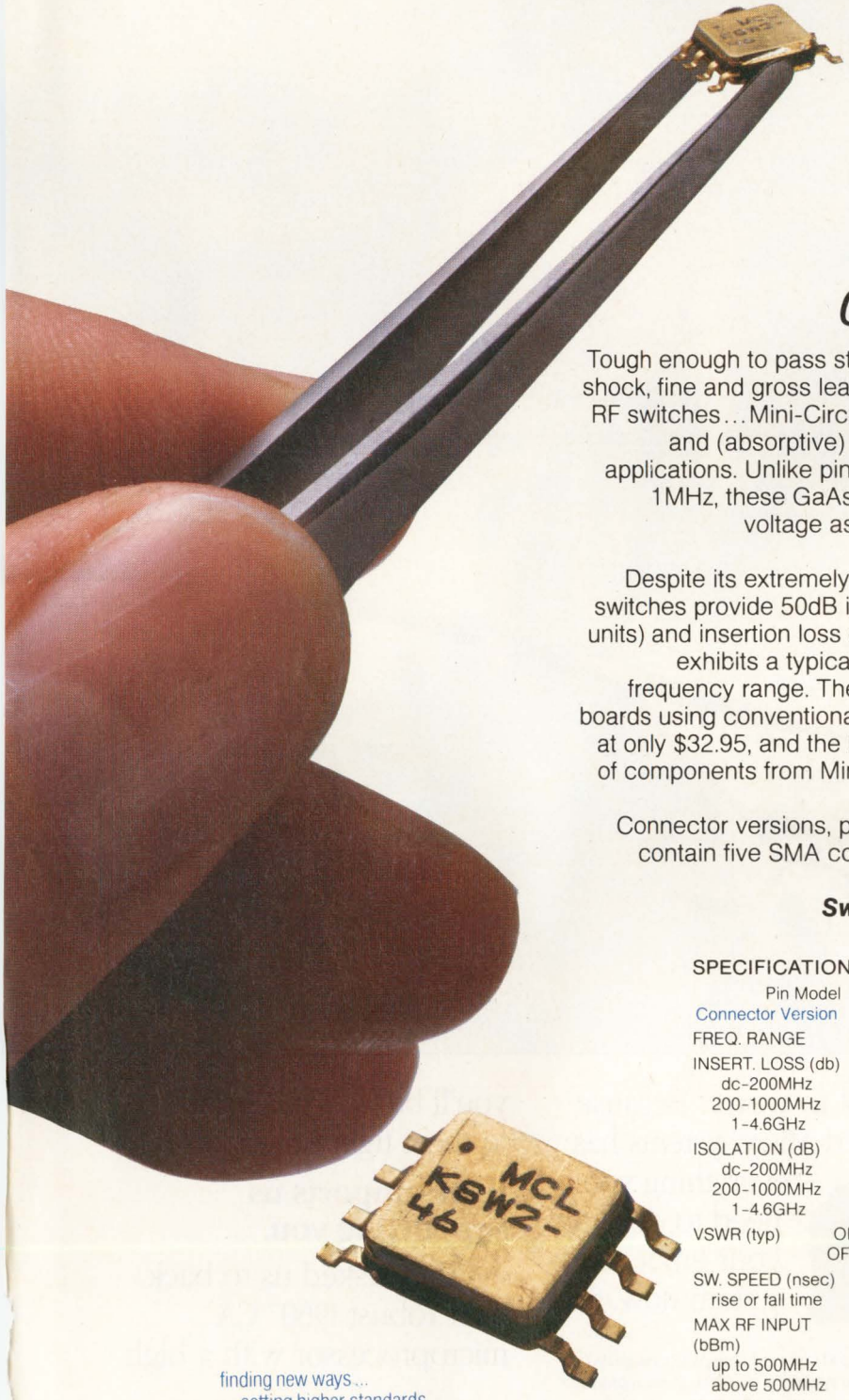
The two articles in this issue, from Xilinx on page 75 and from Expertest on page 89, give some excellent guidance in approaching the testability problem. However, although they offer new techniques, they essentially offer a philosophy that's not new: Design for testability is simply good engineering practice, because a basic responsibility of a designer is to look ahead and anticipate problems. The tools may change, but not the foundations of the profession. LordKelvin, although he would not be surprised, would have approved.



Stephen E. Scrupski

Editor-in-Chief

TINY SPDT SWITCHES
ABSORPTIVE... REFLECTIVE



dc to 4.6GHz from $32.95 (10-24)

Tough enough to pass stringent MIL-STD-883 vibration, shock, thermal shock, fine and gross leak tests... useable to 6GHz... smaller than most RF switches... Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

Switch fast... to Mini-Circuits' GaAs switches.

SPECIFICATIONS

Pin Model	KSW-2-46		KSWA-2-46	
Connector Version	ZFSW-2-46		ZFSWA-2-46	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
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CIRCLE 122

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SAFE PC-BOARD PROCESSES ARE ARRIVING

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After several years of fussing over the prospect of eliminating chlorofluorocarbons (CFCs) from pc-board processing, the electronics industry has finally come to terms with its most pressing environmental problem. CFCs have been linked to the deterioration of the earth's ozone layer, which protects the planet from the sun's harmful ultraviolet radiation. Only a short time ago, it was predicted that no suitable substitute would ever be found for the chemicals. Those predictions have yielded to a flurry of developments that have proved the industry's earlier concerns to be unfounded.

The Montreal Protocol, an international agreement signed by many nations in 1987, calls for its signees to swear off CFCs by the year 2000. The electronics industry accounts for about 20% of CFC use in the United States. A few years ago, an industry expert at DuPont predicted that CFC-113, which is mainly used for pc-board cleaning, would be the most difficult to replace. But many of the industry's largest manufacturers–including IBM, Apple, AT&T, and Texas Instruments–are committed to drastically reducing if not eliminating their use of CFCs. Their efforts are helped in no small measure by a federal tax that has more than doubled the price of CFCs and is scheduled to keep rising.

New techniques to sidestep the hazardous chemicals range from water-soluble fluxes to using inert, safe solvents to not cleaning the boards at all. Apple Computer Inc., Cupertino, Calif., has announced the development of a board-assembly technique that eliminates cleaning altogether. The company's goal is to stop using CFCs by 1993, but it may achieve the goal as early as next year.

In 1987, IBM's disk-drive plant in San Jose, Calif., was the nation's largest source of CFC-113 pollution. But IBM discovered a comparable soap-and-water solution. As a result, CFC emissions are now 95% below the 1987 level, and the plant hopes to rid itself of CFCs by the end of this year–two years ahead of IBM's corporate target date.

One possible solution to the CFC problem is a water-soluble flux that would require no CFCs to dissolve it. Early attempts at such fluxes caused pc boards to absorb water, which resulted in reliability bugs. But scientists at AT&T Bell Laboratories, Napierville, Ill., and AT&T Network Systems, Oklahoma City, received a U.S. patent for a circuit-board flux containing an additive that prevents boards from taking on water. As a result, the flux can be removed from boards easily and economically while completely avoiding CFCs.

The work on the water-soluble flux stems from research at Bell Labs' Princeton, N.J., facility, where scientists developed a substance called BIOACT EC-7, a cleaning solution derived from orange rinds. The flux was developed over the last two years at AT&T Network Systems, which manufactures the company's large telecommunication-switching systems. All of the switching-system pc-board production lines now use the new water-soluble flux rather than rosin-based fluxes, which are difficult to remove without CFCs. Company officials say they've already reached their year-end goal of cutting CFCs by 50%.

Suppliers of fluxes, solders, and board-cleaning equipment are also doing their part to resolve the solvent dilemma. Heraeus Cermalloy, West Conshohocken, Pa., has introduced two series of solder pastes that require no cleaning at all, as well as another that can be washed with water. Alpha Metals, Jersey City, N.J., also offers a water-soluble flux. Kester Solder, Des Plaines, Ill., has rolled out a no-clean flux that's been approved by Bellcore and the IPC. And HMC, Canton, Mass., offers a non-CFC solvent that it claims removes all rosins and most synthetic flux residues. Finally, Vitronics Corp., Newmarket, N.H., has announced a semi-aqueous in-line cleaning system that uses ozone-friendly materials for board cleaning.

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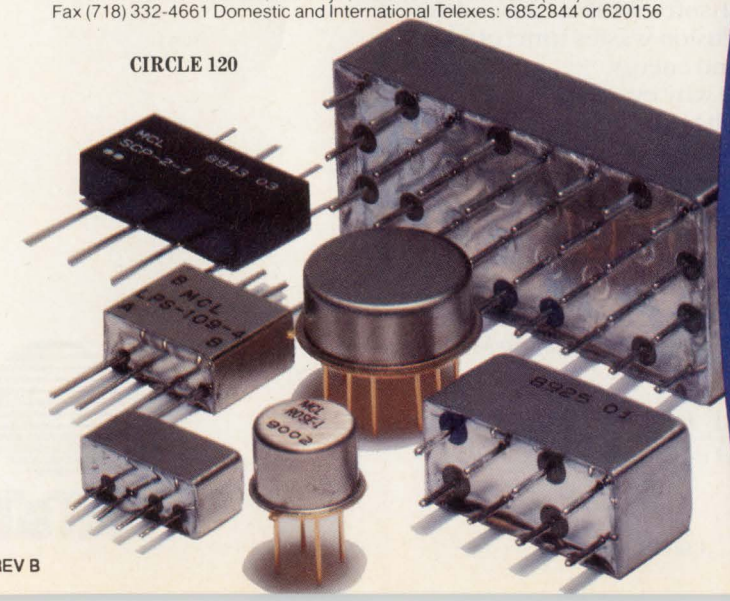
CIRCLE 120



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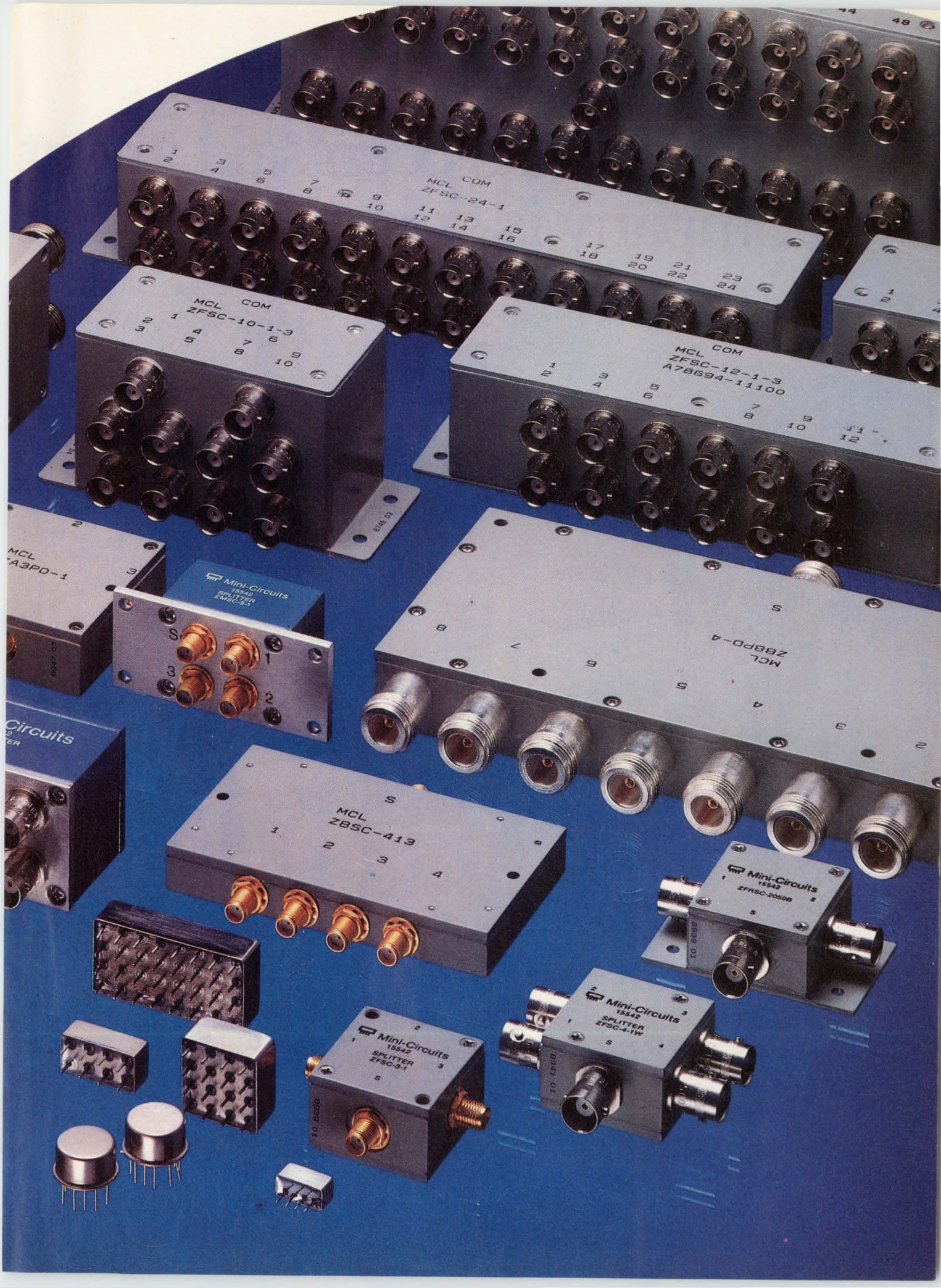
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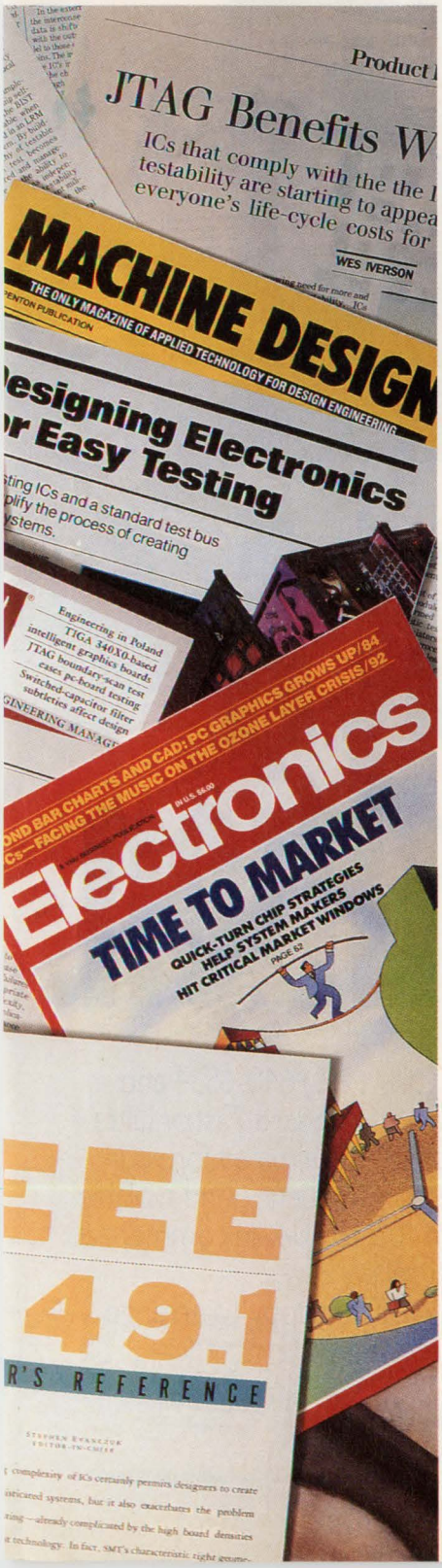
IN THE ERA OF MegaChip™ TECHNOLOGIES

A lot has been said about company is doing a lot about

testability, but only one it. Texas Instruments.



You've seen the headlines and read the stories. Design-for-test (DFT) is a challenge but one that's now easier to live with. The reason: Texas Instruments is the first to develop products for implementing the JTAG/IEEE 1149.1 testability standard quickly and effectively.

To market faster at lower cost

By implementing testability into your system from the outset, you can create one that uses high-performance circuits and is readily manufacturable, one that is lower in total cost and on the market faster. You can expect:

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To simplify and speed your design task, TI has developed its SCOPE™ (System Controllability/Observability Partitioning Environment) family. It is a coordinated, broad-choice set of commercial and military products compatible with the IEEE 1149.1 standard.

Included are bus-interface devices, standard cells, gate arrays, and digital signal processors, as well as our ASSET™ (Advanced Support System for Emulation and Test) diagnostics software.

On the way are diary memories, a series of IEEE 1149.1 stand-alone controllers, and microprocessors with boundary-scan and built-in self-test features.

We are in for the long haul

As a member of the Joint Test Action Group (JTAG), we contributed to the formulation of the IEEE 1149.1 standard and wholeheartedly support it. We are committed to growing our SCOPE family of products so that designing to the IEEE 1149.1 standard will be like second nature.

Your future competitiveness depends upon an engineering methodology where design teams bear the burden of testability, manufacturability, and reliability. The demands of concurrent engineering will be met in part by the extended capabilities accessed via the IEEE standard — from embedded system information that allows realtime availability of data throughout the design cycle to emulation and realtime system analyses capabilities built right into the silicon.

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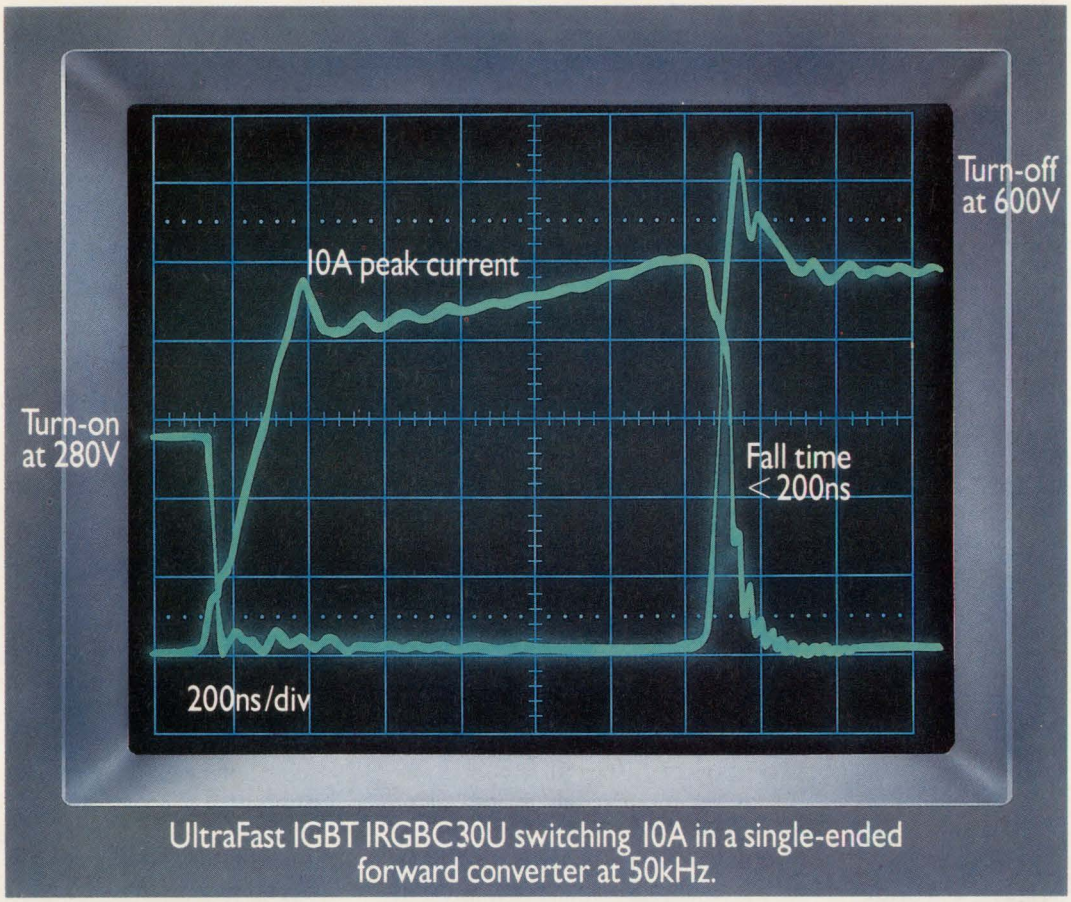
Call 1-800-336-5236, ext. 3909, and we'll send you our unique floppy disk presentation. Just pop it into any MS-DOS™-compatible PC to find out more about DFT and TI's SCOPE testability family. What's more, the disk features a formula that allows you to calculate the cost-effectiveness of implementing testability in your system.

You will continue to read headlines about DFT. We intend to make many of them.

TEXAS INSTRUMENTS



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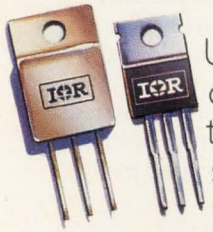

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CIRCLE 153

GaAs ADC Is Error-Free With 1-GHz Input

A sampling rate of up to 1.5 billion samples/second has been achieved for a 4-bit gallium-arsenide analog-to-digital converter. The device was designed by the Fraunhofer Institute for Integrated Circuits in Erlangen, Germany, and fabricated at the Siemens Research Labs in Munich, Germany. While such a sampling rate has been attained by others, the Siemens/Fraunhofer ADC sets a record in accuracy: an effective 3.5 bits for a 1.2-GHz analog input signal. Error-free operation is obtained at 1 GHz. The researchers are now working to cascade two of these 4-bit ADCs to form a converter chip system with a 7-bit resolution. The redundant eighth bit would be used for a digital error-correction circuit.

To implement the basic 4-bit ADC, the Siemens researchers used a new fabrication process for GaAs FETs. Suitable for digital and analog components in the 4-bit ADC, the process involves coating a 0.5-μm tungsten-silicide gate structure with a gold layer. This layer reduces the resistance of the highly temperature-stable but high-impedance tungsten-silicide gate. The result is a transistor with a transit frequency of more than 30 GHz and a maximum oscillating frequency of about 100 GHz. The ADC consists of 16 parallel comparators with associated coding logic and output drivers. It contains 750 transistors, 190 diodes and 120 resistors. The complete 7-bit ADC system will have about 4,000 total components. The new IC is ideal for to use in such instruments as logic analyzers and digital oscilloscopes. *JG*

4-Day Workshop Teaches System-Level Design

Engineers and engineering managers designing complex electronic and computer-based systems may be interested in a system-level design workshop sponsored by CAE Plus, Austin, Texas, and Sun Microsystems, Mountain View, Calif. The 4-day workshop is being offered throughout the country as part of Sun's Educational Services program, and is also available directly from CAE Plus. Dr. Prem Jain, president of CAE Plus, will lead the program. CAE Plus developed and formalized a set of system-level design techniques over the past four years through consulting assignments and Dr. Jain's research with the Computer Sciences Dept. at the University of Texas, Austin. Workshop participants learn these techniques in classroom sessions. Then they apply them to develop and evaluate architectural models of their specific applications in lab sessions with individual assistance and consultation from Dr. Jain. Each participant receives a cartridge tape with a copy of their architectural models upon completing the workshop. The workshops start next month and run through the end of the year in various locations throughout the country. For information, call CAE Plus at (512) 338-0165 or Sun Microsystems at (800) 422-8020. *LM*

TI Second-Sources Sonet IC Line

Under terms of a licensing agreement between Dallas-based Texas Instruments Inc. and TranSwitch Corp., Shelton, Conn., TI will manufacture and market TranSwitch's line of VLSI circuits for operating in the DS3 and the synchronous optical network (Sonet). DS3 is the American National Standards Institute's standard for long-distant and local-loop telecommunications applications. Initially, TI will apply its 1.25-μm biCMOS process to four devices out of the TranSwitch line, which includes multiplexing and termination ICs, cross-connection devices, and Sonet payload and transport devices. Future parts will be made with TI's 0.8-μm biCMOS technology. *ML*

Vendor Group Ensures Proper Tool Integration

The Synthesis Associates' Program established by Vantage Analysis Systems Inc., Fremont, Calif., is designed to help hardware engineers integrate high-level simulation with synthesis tools for top-down design. Vantage is a supplier of VHDL simulation systems. Most developers of today's synthesis technology in the U.S. and Europe belong to the synthesis group, which will use VHDL as a common language for multilevel behavioral simulation and accurate gate-level synthesis. Vantage and the Synthesis Associates members will cross-validate their respective software tools, making certain that a particular synthesizer understands the VHDL constructs and accurately reads the language's semantics. The group's goal is to guarantee to users that the VHDL simulator will work accurately with synthesis tools. Synthesis vendors in the program include: Dessault Corp., LSI Logic, Mentor Graphics Corp., Racal-Redac, and Teradyne Corp. For more information about the Synthesis Associates' Program, call John Willey at (415) 659-0901. *LM*

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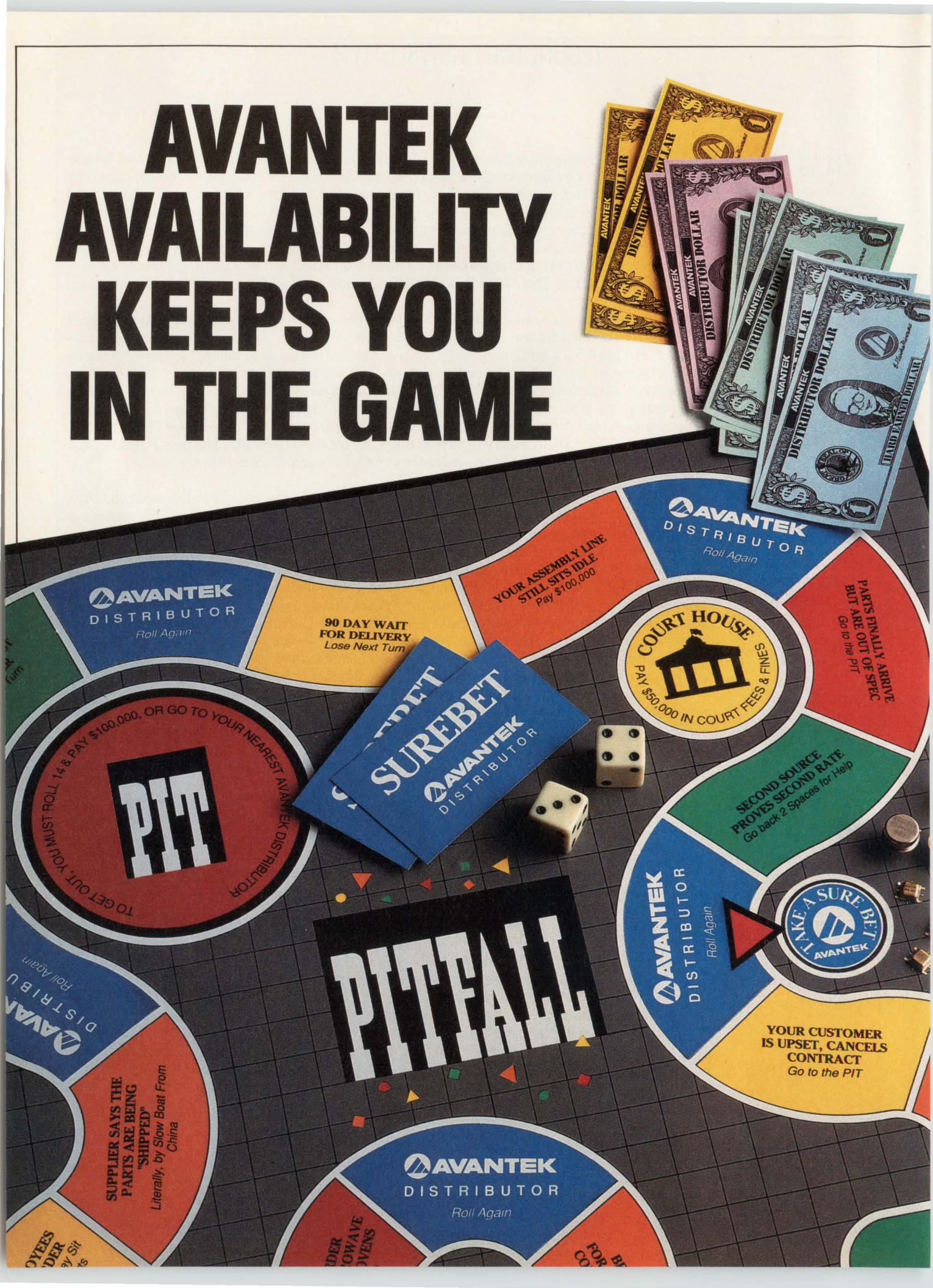

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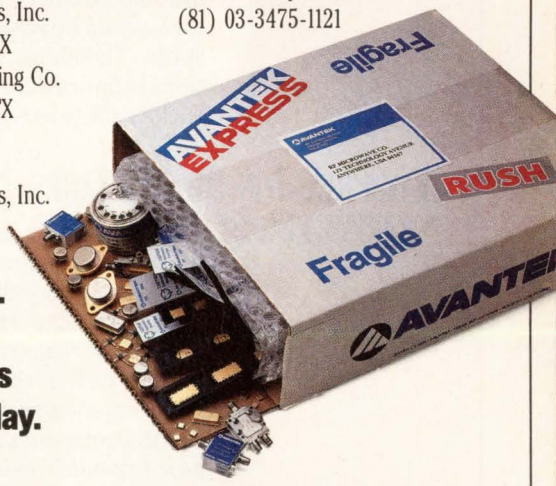

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DESIGNING FOR QUALITY GIVES RISE TO IDEO

With growing emphasis on creating high-quality, efficient products, companies are focusing on improving the front end of product development. To serve those needs, the newly formed IDEO company intends to turn ideas into ready-to-manufacture products through all design stages, from concept generation through design for assembly to product modeling and prototyping. Formed by merging David Kelley Design, Matrix Product Design, and ID Two and European affiliates, IDEO consists of multidisciplinary design teams of engineers, technology experts, human-factors advisers, and industrial designers. Akin to Japanese companies, IDEO does concept-viability forecasting to reduce a company's risk in product development. Separately, the companies have created 500 computer, telecommunications, medical, industrial, and consumer products. With a staff of 125, IDEO is based in Palo Alto, Calif. *SVT*

U.S. FIRM HELPS EDUCATE EUROPEAN ENGINEERS

Meta-Software Inc., Campbell, Calif., developer of the HSpice simulation software, has been chosen to participate in the European Community (EC) Eurochip program, which is part of the larger Esprit program. The program is officially referred to as the VLSI Design Action Group. Its initiative is to meet the projected shortage of VLSI engineers by offering design tools and facilities to engineering students throughout Europe. Services and products from member companies are awarded either free of charge or at a reduced rate to participating institutions from the EC European Free Trade Association countries. Each year, up to 50 students per institution from more than 200 universities and polytechnical colleges will be involved in the program. For more details, call Meta-Software at (408) 371-5100. *LM*

SILICON IGNITOR REPLACES HOT WIRES

By incorporating a heavily doped silicon or polysilicon region on a sapphire or silicon substrate, a low-energy ignitor providing the explosive activation in air-bag restraints and other critical applications improves system safety factors. Because vehicle batteries often get damaged when a collision occurs, the available energy to ignite the gas used to blow up an air bag is minimal. The currently used hot-wire system requires too much current from what might be a dying energy source. The semiconductor bridge ignitor developed at Sandia National Laboratories, Albuquerque, N.M., makes multiple air-bag restraint systems more feasible because it requires less energy—about 1/100 that of the hot-wire—to explode the gas cartridge. The doped semiconductor bridge employs diffused phosphorus in a region that forms the crossbar of an H-shaped pattern on the substrate. The pattern allows good electrical contact with an overlying aluminum connection. As with the hot-wire ignitor, an explosive powder is pressed against the silicon bridge surface and an electrical potential applied across the bridge to ignite the powder. Furthermore, because the semiconductor bridges are manufactured on wafers just like ICs, the chips can incorporate additional circuitry for logic, timing, and safety. Consequently, the semiconductor bridge ignitors would be resistant to the severe, on-board environments that an automobile typically presents. The chips could also be monitored and controlled by the car's computer system. Additional applications include timed-array blasting for mining and weapons systems. Contact Bob Bickes, (505) 846-0559. *DB*

FOCUSED ION BEAM IMAGES NANOMETER-SIZED OBJECTS

Measuring features as small as 6 nm across by producing scanning ion images, a focused ion beam just 8 nm in diameter was created by researchers at Hughes Research Laboratories, Malibu, Calif. The beam, which is about half the size of previously created ion beams, was created with a two-lens microprobe system and a single-isotope gallium ion source. Such beams can be used to "write" ultra-small transistor and circuit structures right on semiconductor substrates. The beam's dimensions are now so small that researchers feel the resolution-limiting factor is now the resist processing that's used to define the regions, and not the beam diameter. When working with structures that have dimensions of less than 10 nm, such effects as ion scattering, atomic recoil, and statistical fluctuations during exposure become dominant error sources. According to the researchers, new types of resist materials with high resolution and contrast, and with lower sensitivity than the popular PMMA resist material, will be needed. *DB*

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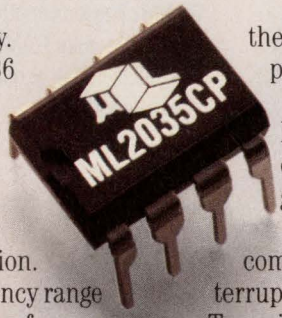

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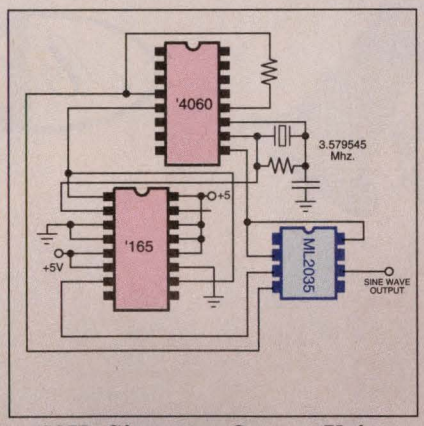
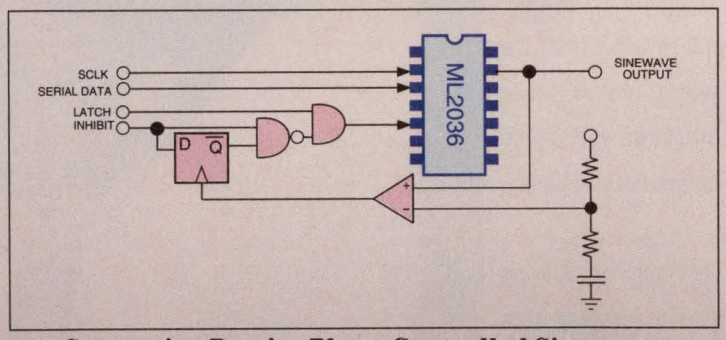
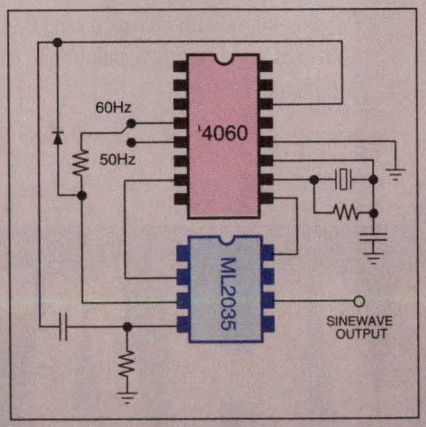
And ask for your copy of our 1991 Data Book, too.



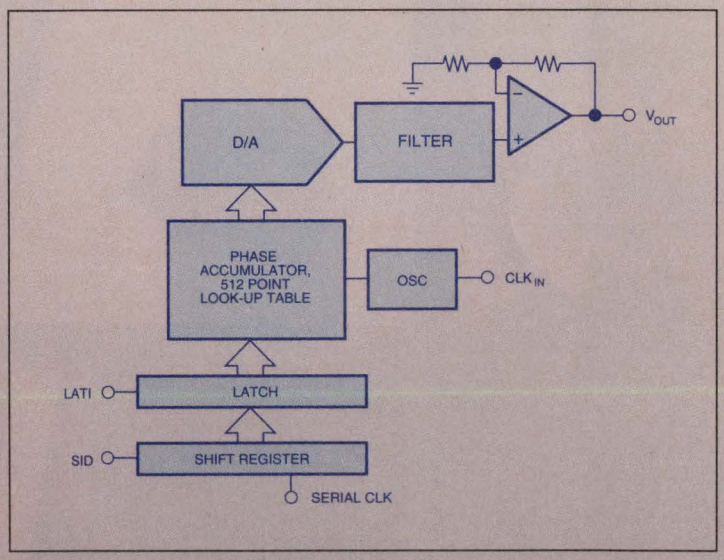
60Hz Sinewave Output Using NTSC Color Burst Crystal



Generating Precise Phase Controlled Sinewaves



Generating Fixed 50Hz and 60Hz Sinewaves



ML2035 Block Diagram

CIRCLE 119

Micro Linear

*Based on lots of 100.

IMAGE ACQUISITION. We've got chip sets that bring image capture to your system with an added dimension: Image quality, made possible by three new 30 MSPS devices that support higher resolutions.

The Bt252 Gray-Scale Image Digitizer, with its onboard lookup table, is perfect for machine vision applications.

The Bt254 Color Image Digitizer's triple Flash A/D's digitize your analog RGB for low noise, high quality multimedia applications.

And our new Bt218 30 MSPS single channel CMOS Flash A/D provides another basic building block for image acquisition.

Team any of the three with our Bt261 30 MHz line lock controller and one of our true-color RAMDACs for a complete image acquisition system on a board.

Convert and optimize its color space in real time,

A/D

Capture an image and digitize it,

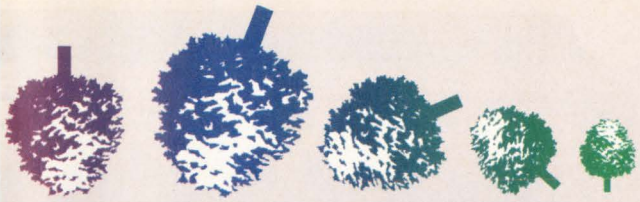
IMAGE RECEPTION. We've got chip sets to send and receive true-color digital video using an 8-bit interface. Our Bt294 CCIR 601/SMPTE RP 125 Decoder works with our upcoming Bt297 ECL-TTL Translator for a complete solution to 4:2:2 digital component video.

INTRODUCING the newest group of Brooktree IC's for image-conscious designers. They add to our rapidly growing family of Image Technologies components. And they underscore the reasons why it makes sense to make Brooktree your prime resource for graphics and imaging power.

We've got IT together, looking at graphics and imaging from a systems architecture point of view. That means chips that work together to simplify your design task. That's IT!

WHAT

Brooktree has got IT: Image Technologies. It's our system-smart approach to packing image acquisition, manipulation,



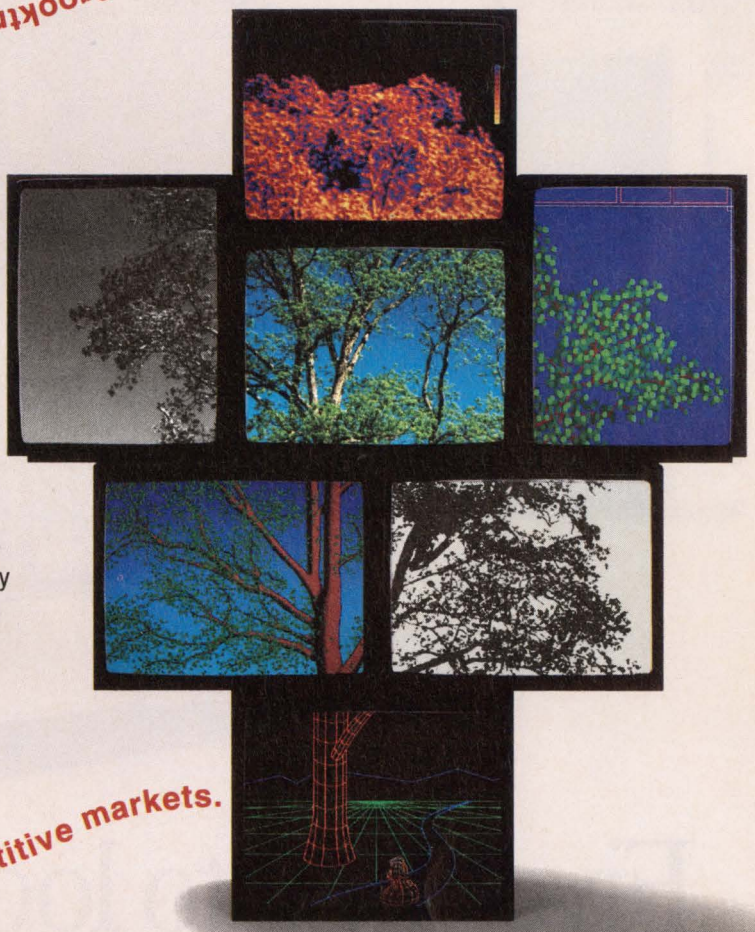
send it and receive it as live color video then display it in high resolution true-color

IMAGE TRANSMISSION. We did say complete solution, didn't we? The Bt291 CCIR 601/SMPTE RP 125 Encoder teams with the upcoming Bt296 TTL-ECL Translator to provide cost effective 4:2:2 digital component video transmission without adjustments or support circuitry. In combination with the Bt294/297 reception devices, they make it easy and economical to add point-to-point video transmission to your multimedia system.

— and do it all with Brooktree's Image Technologies. They make it easy to give your PC or WS design a visual edge in today's competitive markets.

IMAGE PRESENTATION. When it comes to display technology, we're where IT's at: We revolutionized RAMDACs. Now we're setting a new performance standard for super VGA, high-end XGA, 8514/A, TIGA compatible and x. terminal applications. It's the Bt484 true-color RAMDAC.

Its programmable pixel depth means you can run at 4 bits/pixel with 8:1 multiplex, 8 bits/pixel with a 4:1 MUX, 16 bits/pixel at 2:1 MUX or even 32 bits/pixel for 24-bit true color and 8-bit VGA. And its 32x32x2 three-color, user-definable cursor is absolutely awesome.



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CIRCLE 147

SPICE MODEL ACCURATELY REPRESENTS ALL TYPES OF FUSE BEHAVIOR

Because fuses play a vital role in circuit protection, designers working with Spice could profit from an accurate fuse model. Up to now, however, fuses haven't been simulated because of the lack of information from the manufacturers and the complexity required to create an accurate model. However, a fuse model from Intusoft, San Pedro, Calif., breaks the ranks with its ability to accurately simulate fuse behavior.

A Spice fuse model is important because engineers want to see how their circuit will fail in order to build a more tolerant circuit or to investigate and evaluate the component selection criteria. Engineers should know how the circuit will be stressed when its ratings are exceeded so they can decide which components need to be more robust or protected. Also, simulation of fuses is critical because the fuse resistance in low-voltage circuits, especially near or above its rating, can become significant.

Although fuses may seem like simple elements to simulate, they're not. A number of important properties prohibit using a simplified model, such as an ideal current-controlled switch.

For instance, a fuse's rating depends on its dimensions, mounting, enclosure, material, and several other factors that affect its heat-dissipating capacity. Because of the dependencies on heat, temperature, time, and a fuse's nonlinear resistance, a simple current-monitoring switch model can't be used for a realistic simulation.

The Intusoft model overcomes these problems. It accurately represents the time to blow versus load current for currents that are above 135% of the rated value. It also models fuse resistance variations with temperature and current. In addition, it models fuse temperature variations with current, thermal conductance and capacity of the fuse filament, non-repetitive fusing action, and variation in characteristics with current rating.

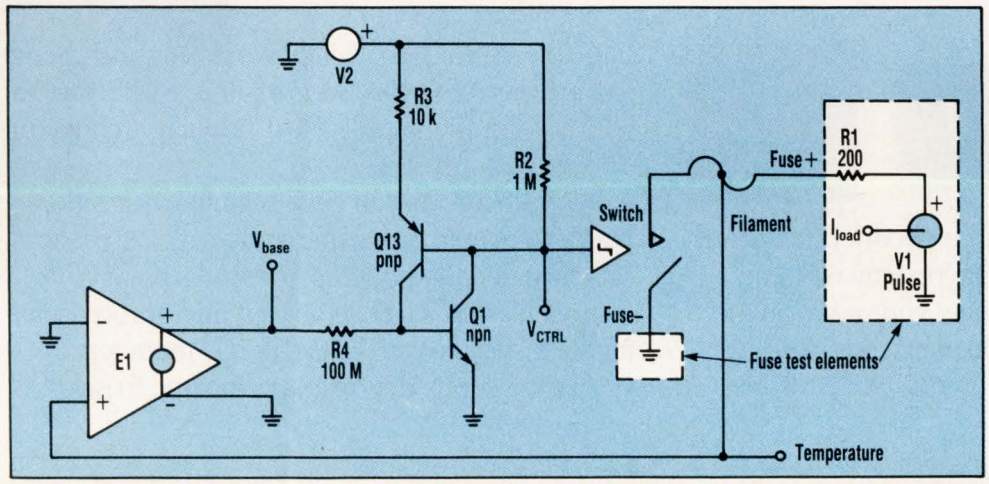
There are two parts to the model: the fuse filament, which encompasses the temperature response; and the fuse-blowing circuit, which allows the fuse connection to be broken when the filament reaches its melting temperature *(see the figure)*. Temperature, however, is usually a constant in Spice. Therefore, it's necessary to use an alternate simulation variable to represent the dynamic nature of temperature in the fuse. The Intusoft model works by using voltage and current relationships as analogs for temperature and heat quantities. Doing this requires that the proper unit conversions be maintained.

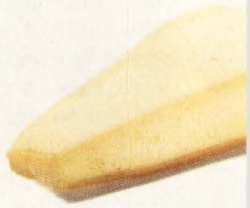
Heat flow through a thermal resistance is analogous to the flow of direct current through an electrical resistance. Both types of flow obey similar equations. The heat flow equation is $q = \Delta T \div R$, where q is the heat flow, ΔT is the temperature potential, and R is the thermal resistance. If the heat flow is replaced by current I, the temperature potential is replaced by the electrical potential E, and the thermal resistance is replaced by the electrical resistance R, the resulting equation is that for electricity flow rate: $I = E \div R$.

Temperature is a critical point because fuses don't blow at a specific current level, but blow at a specific current level as well as a specific time. The model accurately simulates from 135% to 1000% of rating in terms of the time required to blow the fuse. Very accurate representation was achieved by determining the thermal characteristics of the fuse filament and breaking it into two components: thermal conductance and radiation. When a fuse gets really hot, it radiates light and gives off a large amount of energy. If the model doesn't account for that, the fuse would blow too quickly. These two components are used in a polynomial representation of this time-to-blow function. The fuse's input is some power made up of current and the fuse resistance, and the fuse's output is the temperature based on the conductance and the radiation.

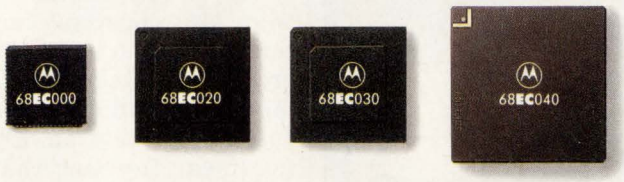
Dc and transient convergence, and proper initialization of the fuse model, were also important factors that had to be considered when developing the model. In addition, the fuse-blow process is a very nonlinear function that needed to be adjusted so that the Spice program could continue with simulation after the fuse had blown.

The fuse model has constants based on the electrical fuse resistances. Users can adjust the constants so





OTHER 32-BIT EMBE OFFER SOMETHI



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that one fuse model can represent a whole family of ratings. The constants relate to whether the fuse being modeled has the characteristics of a slow-, fast-, or normal-blow type.

With the fuse model, engineers can now simulate the conditions that would cause the fuse rating to be exceeded, and study what happens to the circuit. The proper transient behavior will be displayed. And because the fuse accurately represents the time-to-blow versus current characteristics, various fuse types and ratings can be analyzed to provide the best component for the job.

Although the model is complex, it doesn't cause a great deal of slow down in the simulation when the current rating isn't being exceeded. Consequently, there's little penalty paid for including it in a simulation.

Designers can get more details about the fuse model from Intusoft's Spice newsletter. The newsletter is published four or five times a year, and is sent free to designers. Each issue contains Spice application notes, simulation tips, free models, and example circuits. Call the company at (213) 833-0710.

LISA MALINIAK

DAT DRIVE'S LOADER CAPABILITY ALLOWS UNATTENDED BACKUP

Digital audio-tape (DAT) drives are starting to follow in the footsteps of magnetic-tape drives. This trend is evidenced by a new disk-drive development from WangDAT Inc., Irvine, Calif.

Typically, DAT drives can't run in an unattended backup mode, like their magnetic counterparts. The magnetic models employ a loader or a jukebox-type system to fill multiple cartridges. When one cartridge is filled, it's removed from the drive, placed in its holder, and a second cartridge is placed into the drive. Most DAT drives are unable to automatically replace tapes that are full.

With WangDAT's LD series of DAT loaders, that capability is now here. The DAT loaders fit a 5-1/4-in. full-height form factor. And they use a standard DDS format.

Unlike most current DAT loaders, which literally stack a multidrive magazine on top of a base assembly, the WangDAT loader incorporates the loader mechanics within one enclosure *(see the figure)*. The drive's mechanics pull a tape from the magazine, slide it up to the slot, and insert it into the drive. When the tape is filled, it's slid back down into the magazine and replaced by another tape.

This design protects the loader mechanics from operational interference, which can result in electrostatic discharge or other physical damage. To further eliminate loader damage, the LD series of loaders will be equipped in the future with built-in sensors for cassette-position recognition.

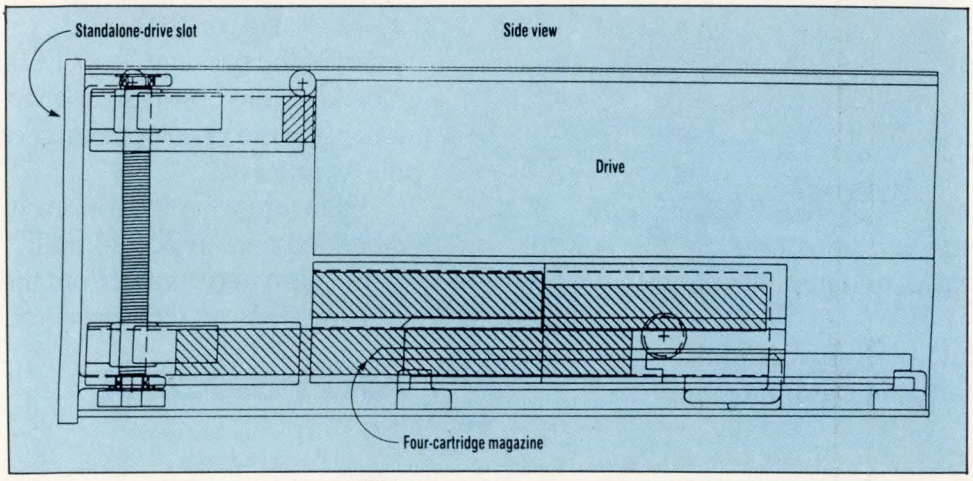
In addition to unattended backup operation, network users would also like to have the option of using the DAT loader as a network resource, permitting on-line management of multiple files, with the files arranged in logical order and randomly accessible. WangDAT's loader accomplishes this task. It also contains support for SCSI-II medium-changer commands.

The drive's four-cassette magazine has an 8-Gbyte storage capacity. Up to 20 Gbytes of data can be stored using data-compression techniques. An eight-cassette version may follow shortly after the LD series is introduced by WangDAT. Multiple loaders (up to six) can be stacked to further increase storage capacity.

To maximize the drive for unattended backup or on-line operation, the loader works in a dual-mode arrangement. By selecting one of two slots on the front of the loader, users can operate the unit as a standalone drive for routine file transfer, software distribution, or local system backup. For true loader operation, all four cassettes within the magazine can be utilized, with a simple change in the SCSI command set to perform full-system backup. Unattended backup can be accomplished using on-board switch options or standard SCSI-II medium-changer commands with the loader addressed as LUN1. Certain minor vendor-specific modifications to the Load/Unload command also allow the unit to operate in SCSI-I system environments.

The loader is scheduled to be available around October. According to WangDAT, the loader will probably carry a mean-time-between-failure rating of 30,000 hours.

RICHARD NASS



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IDT's 64K BiCEMOS™ TTL I/O Static RAMs are the ideal solution for high-density cache systems, and are the perfect match for optimizing the high-performance needs of RISC and CISC processors. These 8ns and 10ns SRAMs provide the highest system speed without sacrificing system chip count or increasing power consumption.

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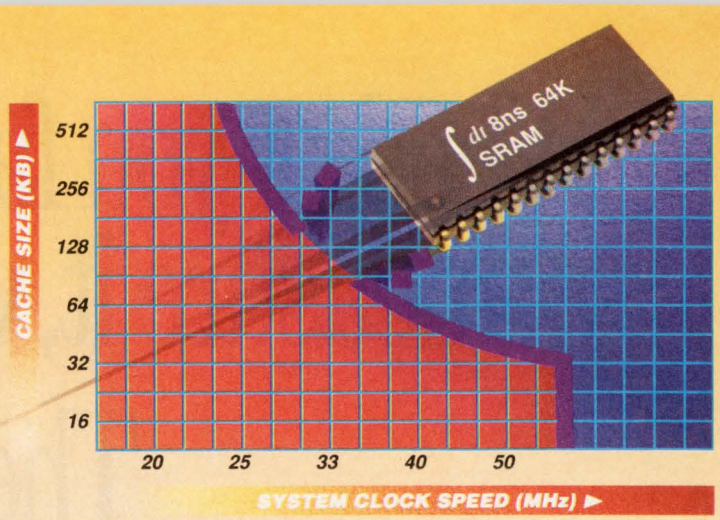

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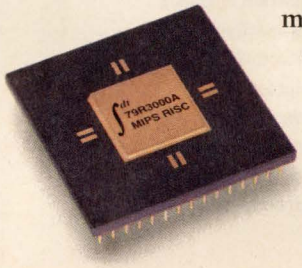

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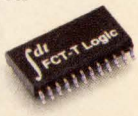

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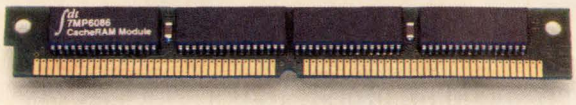

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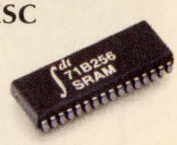

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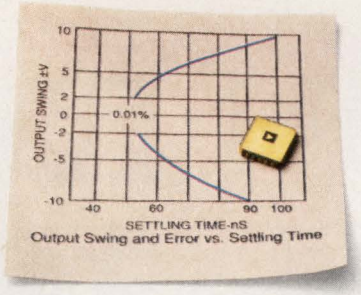
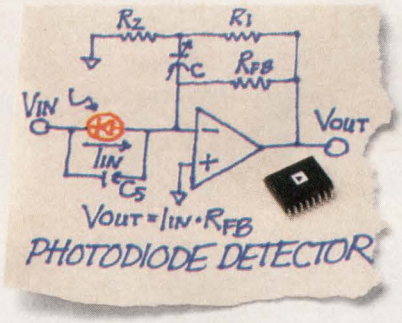


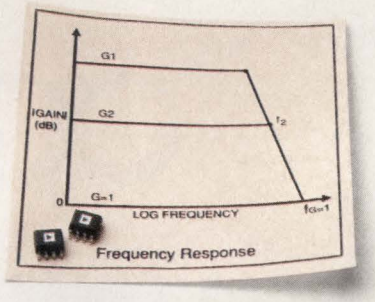
Precision

With the AD840, AD841 and AD842, there's no need to trade speed for accuracy. All three settle to 0.01% within 100 ns (840/842) and 110 ns (841) – critical in data acquisition and instrumentation applications – and offer low offset voltages and drifts, and fast slew rates.



FET Input

For op amps requiring low input current, the OP-42, OP-44, AD845 and AD843 are all remarkably fast – slew rates are 58, 120, 100 and 250 V/μs, respectively. In addition, they offer offset voltages of less than 1 mV and extremely low current noise.



Transimpedance Amplifiers

The OP-160, OP-260, AD844, AD846, AD9617 and AD9618 all utilize a current feedback architecture to achieve slew rates from 450 to 2000 V/μs without compromising stability – even in hostile environments. Other benefits include low power dissipation and high unity-gain bandwidth.

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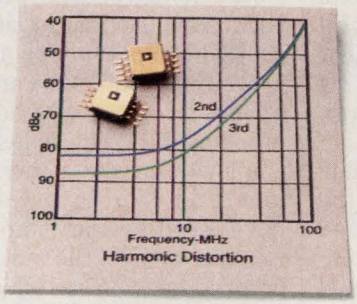
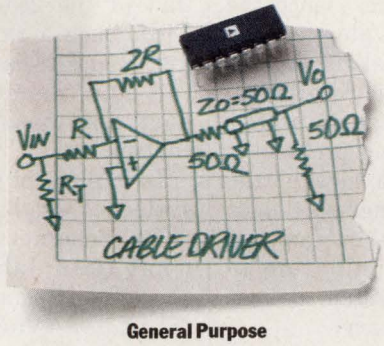


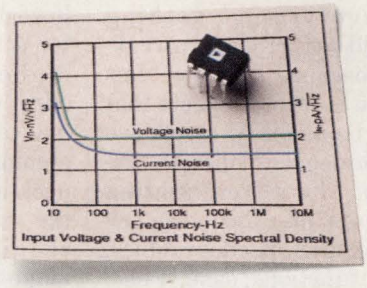
Buffers

If you're looking for extremely low distortion buffers, look at the specs of the AD9620 and AD9630 – distortion at 20 MHz: −73 dBc and −66 dBc, respectively; fast settling time: less than 8ns to 0.02%; and extremely low noise: 2.2 nV/√Hz.



General Purpose

With the right combination of speed, precision, power dissipation and high output drive capability, the AD827, AD829, AD847, AD848, AD849 and OP-64 are ideal general purpose solutions. And they're ideally priced solutions – most singles are under $3, and duals are under $5.



Low Noise

It used to be you had to choose between speed or low noise. But with the AD829, you get both. It features voltage noise of 2 nV/√Hz and current noise of 1.5 pA/√Hz with a 50 MHz unity-gain bandwidth. Those specs, combined with the low price of $2.95/100s, make it ideal for both audio and video applications.

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CIRCLE 80

NEXT-GENERATION PC DESIGNS PUSH SYSTEM PERFORMANCE TO THE LIMIT

Many designers feel that PC and workstation chip sets have, to some extent, made the design of the basic personal-computer system a "cook-book" task. Except for the lowest end of the clone market, where price is everything, nothing could be further from reality, because most systems have multiple aspects that can be modified to achieve some degree of differentiation. The differentiating factors may include such aspects as speed, graphics, I/O functions, ease of use, low power, and many other factors.

Learning how to differentiate a system will be the key to gaining visibility in an already crowded market. Helping designers do just that are over 100 technical papers and tutorials scheduled for presentation at the Silicon Valley Personal Computer Design Conference (SVPC) next month *(see "Want to go?," below)*.

The conference will cover a wide range of topics, including power-management approaches in laptop computer systems, accelerating graphical user interfaces, multimedia systems design, and motherboard, memory subsystem, and I/O card design. Software issues, such as BIOS development and windowing environments, will also be discussed.

Speed (or throughput) is always an area that helps distinguish one computer system from another, whether that speed is achieved through better architectural definition, faster cache design, dedicated silicon to accelerate various functions, or even through better circuit-board design that permits the use of higher system clock frequencies. The problem is analogous to a pail with holes—once the lowest hole is plugged, water starts leaking from a higher hole. Similarly, once the biggest performance-limiting problem is eliminated, a new bottleneck in another portion of the system shows up and requires elimination to make the system deliver top performance.

One way to avoid redesigning a system to handle higher clock rates is to partition it. The CPU and closely coupled functions like the clock, cache, and perhaps a math coprocessor are isolated from the rest of the system. By making the motherboard CPU-speed independent, designers at Toshiba America, Irvine, Calif., can design systems that allow simple performance upgrades by replacing a CPU module rather than an entire motherboard.

Thanks to a system chip set (four chips) developed jointly with Bull Micral, Minneapolis, Minn., the Micro Channel-based PC-compatible motherboard runs at a constant clock rate that's about one-half that of the 25-to-50-MHz CPU. Such a rate is still fast enough to handle all of the main memory, I/O port, and mass-storage control.

To implement a flexible system of this nature, the chips' designers created what they dubbed the short-line interface kernel (SLIK)—a synchronous processor-to-memory interface bus. As part of the motherboard chip set, designers created a controller chip that not only has the synchronous control signals on one side, but also has the asynchronous control signals needed by the rest of the system to tie into the Micro Channel Adapter (MCA) card slots.

The synchronous portion of the SLIK interface runs at the CPU speed, typically 25 to 50 MHz for a microprocessor like the 80486. A memory- and bus-controller chip—one of the chips in the chip set—controls the bus accesses. It also supports both page-mode and page-interleaved memory-addressing schemes.

A similar approach for the Extended Industry Standard Architecture (EISA) bus developed by Intel Corp., Folsom, Calif., yields motherboards with EISA expansion slots and a host CPU bus that can accept an 80386, 80486, or any other microprocessor-based module. The system employs a second-generation EISA chip set, recently released by the company, that shrinks the motherboard logic down to just five different chips *(see the figure)*.

Yet another firm examining better EISA-system architectures is Texas Instruments, Dallas. The company will examine the overall system architecture to optimize the chip set's integration.

Proper design of the accompanying cache subsystem is critical to overall system performance. In a tutorial paper and several technical papers, various aspects of cache design will highlight how to coax the most performance from the system. Employing cache-tag RAMs with address-to-match times of 12 ns to implement caches that can operate with 40- and 50-MHz systems, Texas Instruments analyzes and breaks down the timing factors in the cache-to-CPU data path to pinpoint critical paths, optimizing the interface.

By examining hardware concurrency in write-back caches, Mosel Corp., Sunnyvale, Calif., aims to improve system perfor-

WANT TO GO?

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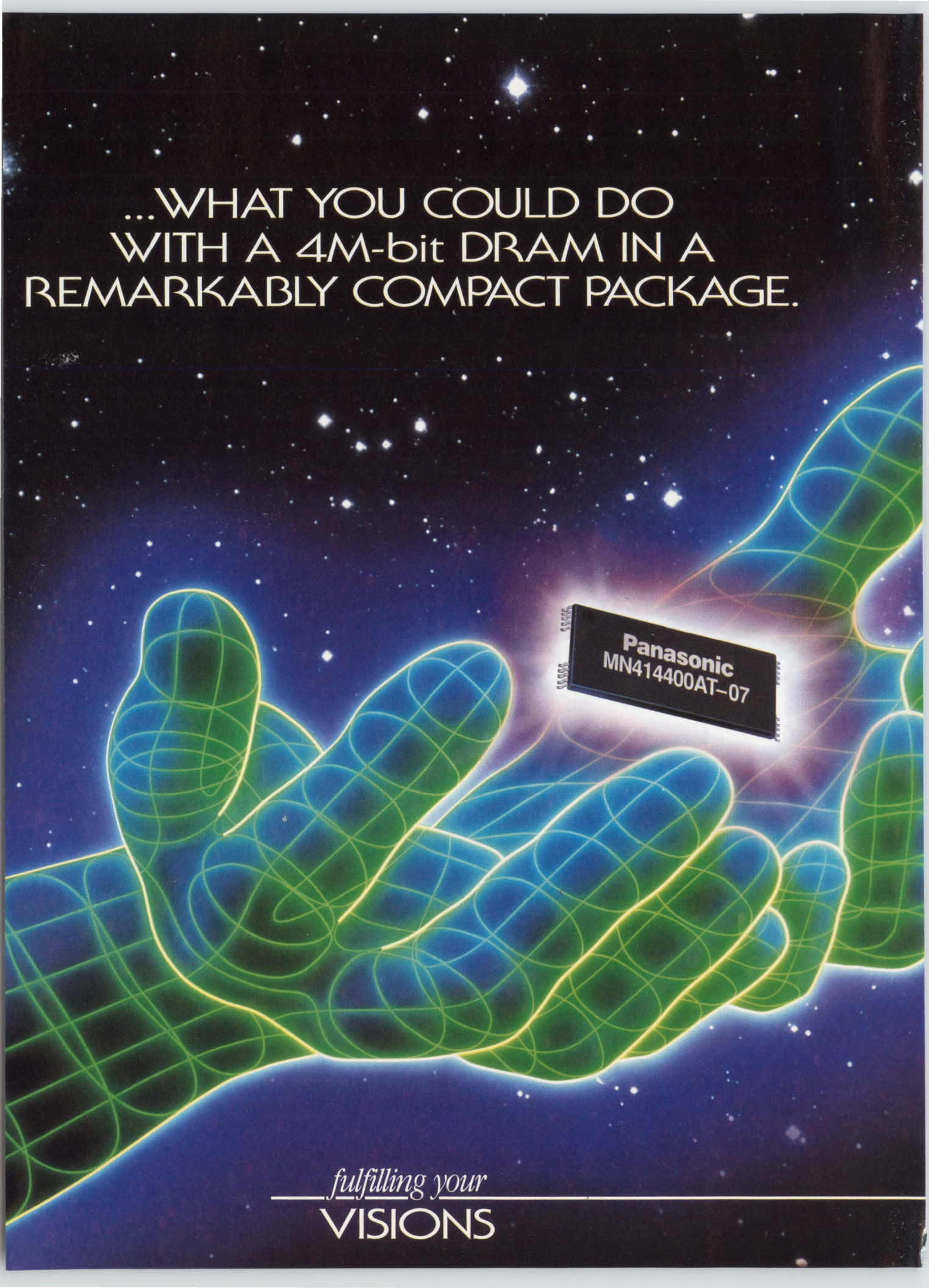
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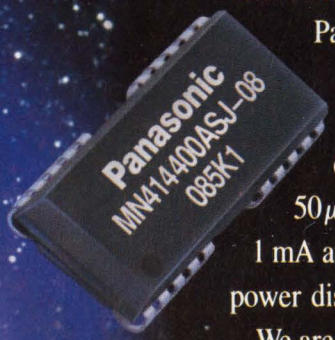

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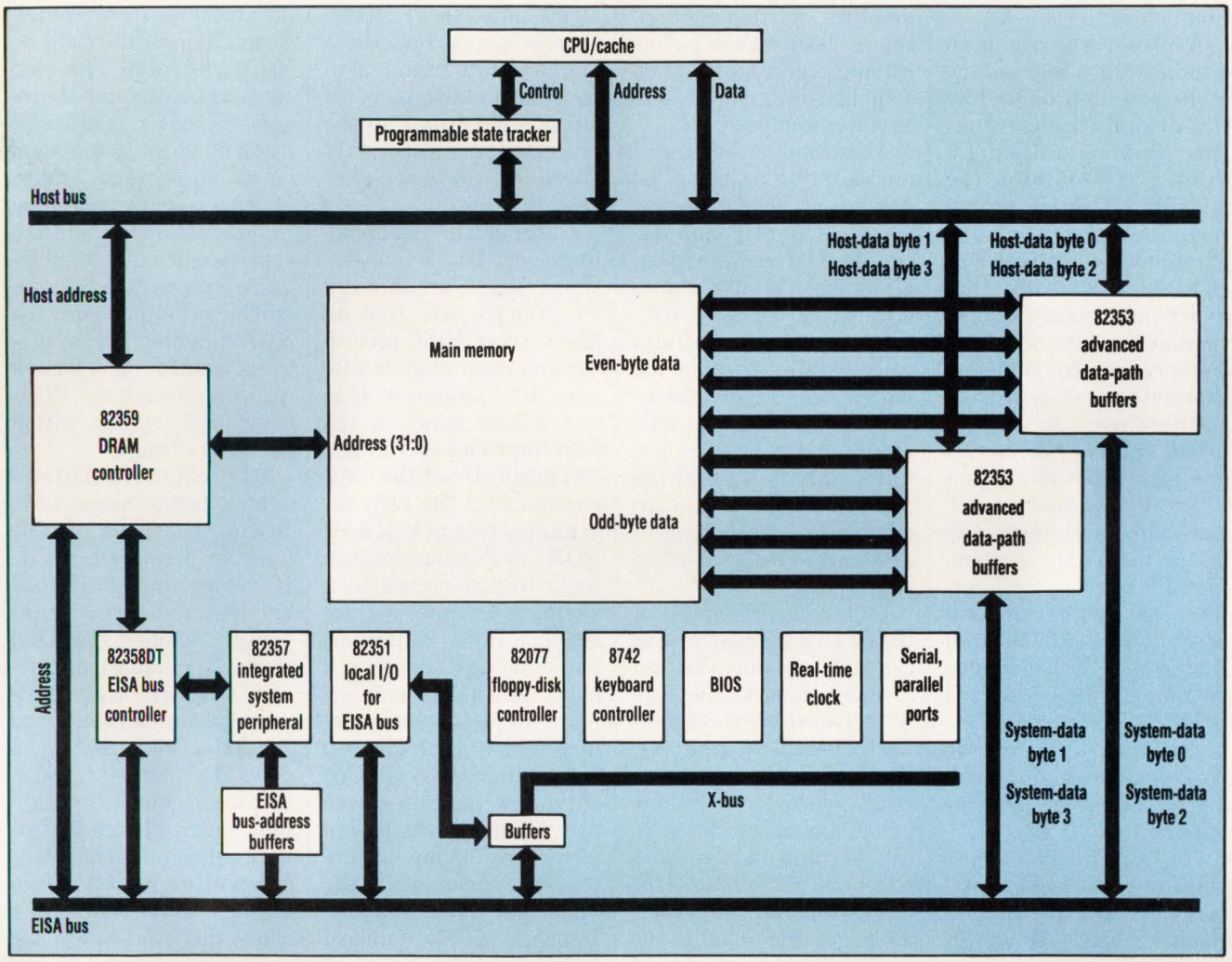

mance. It proposes an intelligent data path that consists of a dual-port data path surrounding a single-port static-RAM memory array. Data leaving the SRAMs is stored in holding registers on both ports to accommodate the slower external bus speeds of the CPU and the system. Similarly, data entering the memory must be first loaded into holding registers to avoid internal bus conflicts and to ensure that the internal bus operates at its peak data rate.

Separate read and write holding registers are used on the system side to resequence the standard write-back cycle to improve performance. An ordinary write-back algorithm spends the first part of its cycle writing dirty data back to the system, and then completes the overhead operations by reading in a new line of data from the main DRAM.

By using the holding registers, the intelligent scheme can empty the dirty cache line into the internal register. Then, it immediately begins the DRAM line read-access to validate the newly allocated cache line in one-half the time. Even more important, the CPU write data that triggered the system port operations can be transferred into its newly allocated cache memory space immediately after the dirty data is moved to the write-back register. That process consumes only one more clock cycle than needed for a typical cache write hit.

Although caches add to the motherboard's complexity, they do substantially boost system performance. Consequently, caches can make sense even for compact systems, such as those based on the 80386SX. This holds particularly true if they can be integrated, as Intel Corp., Folsom, Calif., has done with all of the control logic to form a single-chip subsystem.

Even though the cache memory size isn't as large as might typically be used if a cache is built with separate SRAMs (8 kbytes vs. 32 or 64 kbytes), integrating all of the control logic and memory allows the chip (and thus the system) to deliver performance similar to systems with the larger caches.

Of course, if DRAMs were faster, then systems would not need caches. However, even today's best commercially available multiplexed-address DRAMs still have access times of more than 50 ns, while SRAMs are now commonly available in speed grades with one-half that

time or less.

A novel approach to eliminating a secondary cache will be proposed by Cheetah International Inc., Colorado Springs, Colo. By combining the DRAM and SRAM memories onto one chip, the company developed a distributed cache architecture that overcomes many of the current limitations of today's caches for high-end PCs and workstations.

One alternative to the use of specialty memories or large caches might just be to optimize the memory subsystem architecture to better match the system. Various memory architectures, such as two or four-way interleaving, as well as the use of page-mode memories will be analyzed by NMB Technology Inc., Chatsworth, Calif., to give designers an understanding of their main-memory options.

One of the "easiest" ways to boost system performance is to increase the clock frequency. However, as operating frequencies go beyond 33 MHz, designing system motherboards becomes a very tricky procedure due to noise and clock-skew problems. Examining the typical clock distribution networks, Texas Instruments analyzes the different sources of skew and how they affect overall system performance. Tips and guidelines on loading, pc-board trace layout, and other factors aimed at minimizing such problems will be covered in a technical presentation.

Picking up on the same general topic, Silicon Connections Corp., San Diego, Calif., examines the use of phase-locked clock generators to reduce skew and produce multiple clock copies. Issues such as line loading, termination, and strip-line design approaches will be analyzed.

Addressing other transmission-line analysis issues to ensure high performance, Quantic Laboratories Ltd., Winnipeg, Manitoba, Canada, shows how to use analysis software to model the effects of crosstalk and noise on high-speed circuit boards. Employing its Greenfield software, Quantic Laboratories will step through the analysis of a multilayer circuit board for problems of crosstalk and signal integrity.

Improving the speed of the CPU or the response of the cache are only the first of many aspects that can be tackled to create higher-performance computers. The I/O channel has already grown from the simple XT expansion slot up to the AT, and then to both EISA and MCA options for 32-bit transfers. However, as larger files handle the ever-increasing use of graphics and image data, even faster buses are needed to transfer the data.

As an alternate to EISA or MCA, Digital Equipment Corp., Palo Alto, Calif., is proposing its TURBOchannel local bus as an option that permits data transfers of up to 100 Mbytes/s. The bus is asymmetrical, connecting one system module (a processor and system memory) to a number of peripheral option modules. It permits direct communication between the system module and any of the option modules, but doesn't allow the direct communication of one option module to another. Employing only 44 signal lines, the TURBOchannel bus can operate at any clock rate from 12.5 to 25 MHz, and can serve as either a direct link to the processor or as a special I/O channel for speed-critical data.

Utilizing RISC technology to speed up I/O operations, VLSI Technology Inc., Tempe, Ariz., took its 32-bit Acorn RISC processor and created an intelligent I/O processor that can offload many of the host-controlled operations. The small size of the CPU core enabled the chip designers to pack RAM, ROM, an ISA bus controller, a DRAM controller, a serial interface, a two-channel DMA controller, and other features onto a chip that delivers between 5 and 10 MIPS when running from 10 to 20 MHz. An example is provided to show how the chip solves disk I/O transfers by implementing many of the primitive commands in the Small Computer Systems Interface (SCSI) standard instruction set.

Another area of concern for designers is accelerating the performance of graphics subsystems once the CPU is operating at its peak. New operating-system enhancements, such as graphical user interfaces (GUIs), have initially slowed down many systems due to the high software overhead the GUIs impose on the CPU. To eliminate some of the overhead, enhanced graphics chips with dedicated hardware, which could speed up some of the commonly done operations in GUIs, can make a marked difference in display performance.

Just such a chip will soon be available from Weitek Corp., Sunnyvale, Calif.—the W5086/5186. This chip can accelerate some Microsoft Windows operations by as much as 16-fold, and offers an average 3-times improvement in image-manipulation speed. Unlike coprocessor chips that require a separate VGA controller or implement the VGA function under program control, the Weitek chip will include the VGA-compatible engine within the same silicon.

RISC chips, like the transputer from Inmos Ltd., Bristol, U.K., can also be used to accelerate GUIs. By employing the small credit-card-sized transputer modules (TRAMs) that are available from several sources, a general-purpose accelerator card for GUIs, such as X-Windows or Microsoft Windows, can deliver throughputs several times that of the best commercial VGA-controller-based video cards. Furthermore, because the transputers are available in either integer or floating-point versions, card implementations for 3D graphics, rendering, and image-signal processing can be readily pulled together.

According to Texas Instruments Inc., Houston, the power of its TMS34020 programmable graphics processor, when coupled to the 34082 floating-point coprocessor, lets designers implement workstation-like 3D graphics on PC platforms. The two-chip set, when used on an ISA add-in card, can deliver a drawing throughput of 700,000 10-pixel 3D vectors/s, as well as 70,000 3D Z-buffered polygons/s.

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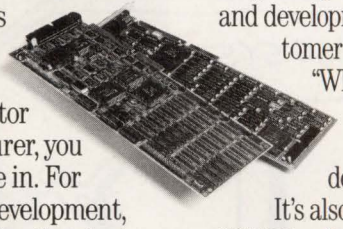

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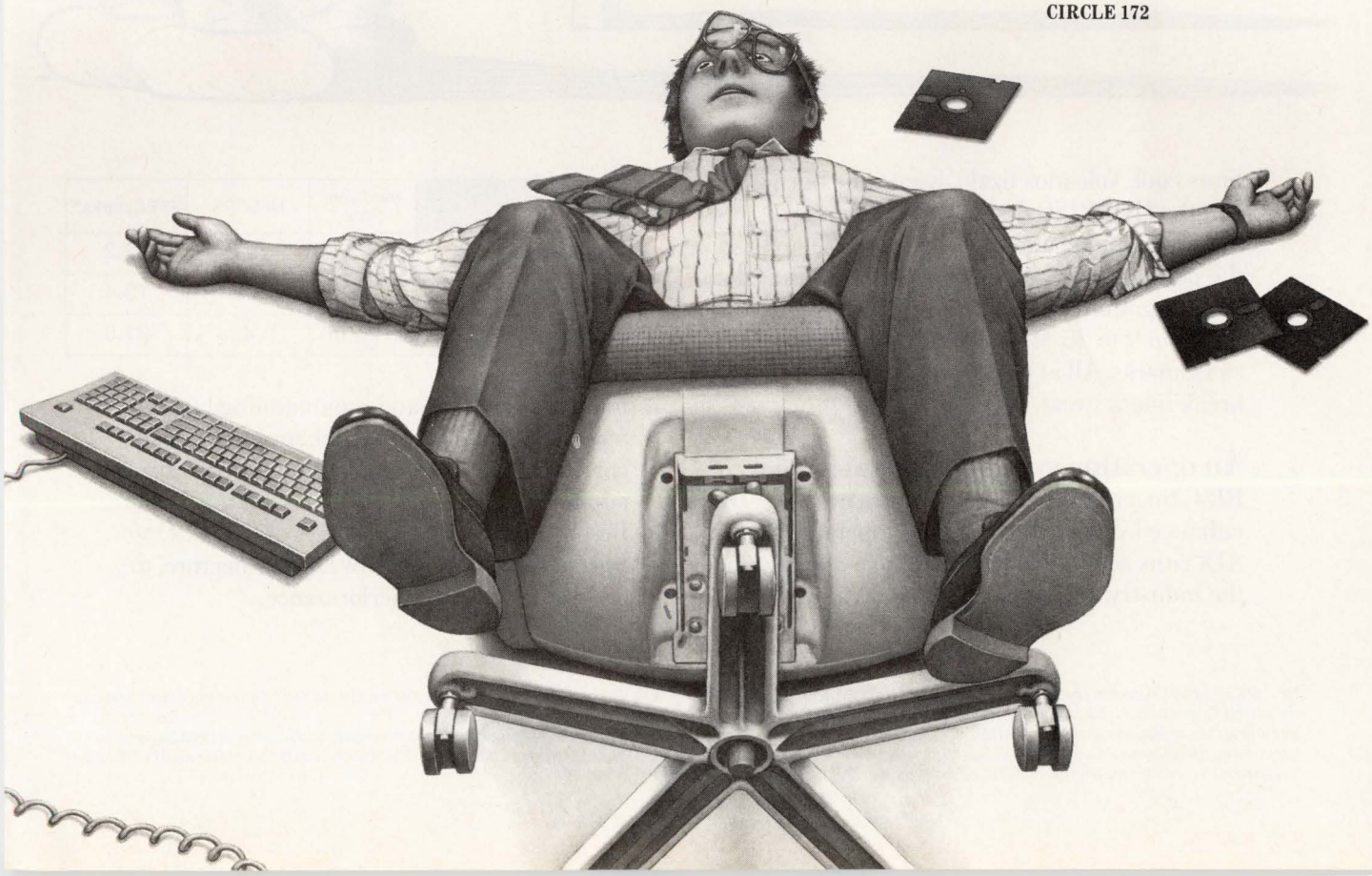

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DECsystem™ 5500	$74,700	4	21.5

MFLOPS are LINPACK double-precision where n=100. AIX XL FORTRAN Version 2.1 and AIX XL C Version 1.1 compilers were used for these tests. SPECmark is a geometric mean of the ten SPECmark tests. All prices current at publication.

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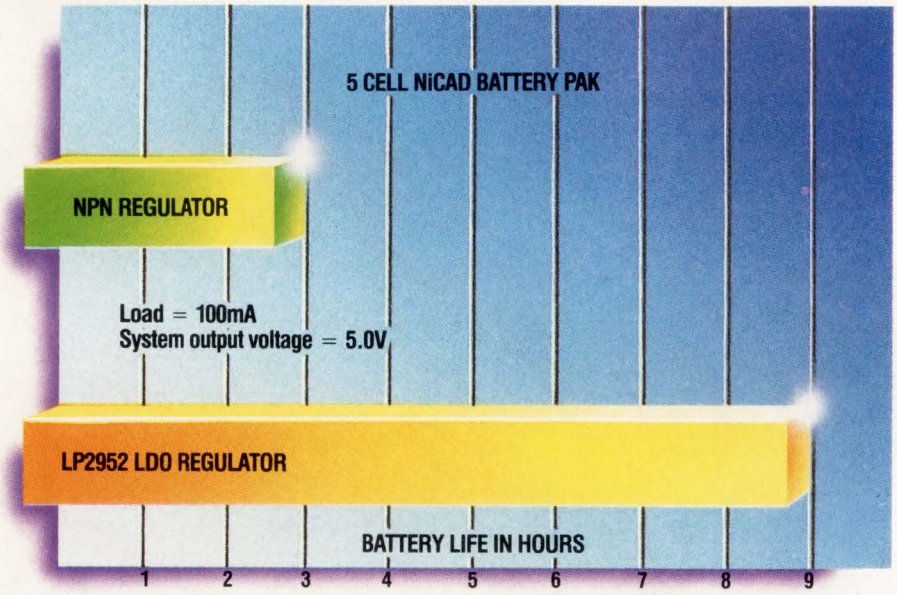

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Vo	5V	5V	1.23V to 29V	1.23V to 29V	1.23V to 29V	5V	5V, 8V, 9V, 10V, 12V, 15V	5V to 20V
Package	Z, M	Z	J, N, M, H	N, M	N, M	T	T	T

H = Metal Can
J = Ceramic DIP
M = Surface Mount
N = Plastic DIP
T = TO-220
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Until now, if you needed an op amp to handle more than about 100 V between its supply pins, the several alternatives available were often unacceptable. Rolling your own circuit from discrete transistors and passive parts represents the most common approach to the age-old "make or buy" decision. Time-to-market pressures tip the scales either toward a new product's success or its failure. Thus, the decision to make rather than buy becomes an unpleasant option, even if you have the know how.

An expensive, chip-and-wire hybrid, such as the Apex PA82 or PA83, is another alternative. They run about $70 each in hundreds. Or, if space isn't a problem (and only a few milliamperes are needed), you can try vacuum-tube op amps—if you can get the tubes. If it's a one-of-a-kind project and only a couple of op amps are required, you might find some old Philbrick K2s in a surplus store, or you can recycle some that you've stashed away.

A few years ago, Apex, the leader in high-voltage op amps, kept running into hybrid customers who had to have a lower-cost high-voltage device in quantity. But they needed IC cost and reliability. Consequently, Apex came up with the PA41, an IC op amp that takes 350 V between its supply pins and swings its output within 12 V of both rails.

Apex chose the just-announced AT&T high-voltage BCDMOS mixed-signal array, the ALA501, for the job. It's fabricated on a dielectrically isolated (DI) process that puts small-signal bipolar and CMOS devices on a chip with 350-V (operating voltage) DMOS transistors, and provides 1000 V of isolation between transistors with silicon dioxide (ELECTRONIC DESIGN, *Aug. 10, 1989, p. 87*).

Some said you couldn't build a true op amp on the ALA501, let alone one that could swing its output ±160 V across 2700 Ω. But Dennis Eddlemon, the designer of Apex's hybrid, MOSFET high-voltage op amps, didn't listen. The result is the PA41 built on the array *(see the opening figure)*. It comes in a TO-3 package, takes 350 V between its supply pins, swings its output within 12 V of each rail, puts out 60 mA continuously, and costs just

HIGH-VOLTAGE IC OP AMP

$39 each in hundreds. Moreover, with a minimum open-loop gain of 94 dB, it's a true op amp. When shown working silicon a few months ago, a PA41 customer told Apex they considered designing their own op amp on the array but decided it couldn't be done.

Who needs such a device? It's great for driving piezoelectric transducers. The transducers, in turn, help build micropositioning systems for small mirrors, which form a part of the large mirrors used to aim and focus "Star Wars" laser beams.

The cost-performance offered by these op amps should challenge the creative juices of all analog designers worth their silicon. So far, Apex has found that potential applications generally break down into three classes: electric-field modulation, piezo drive, and instruments.

Before looking in more detail at potential applications, just consider that driving a PA41 with a 16-bit digital-to-analog converter (DAC) creates a ±165-V, 60-mA voltage-source that's digitally programmable in 5-mV steps. Two PA41s paired in a bridge circuit double the voltage swing across the load to 660 V pk-pk *(Fig. 1)*. One of those two circuits is the heart of many applications.

Electrostatic deflection; shaping; and focusing of electron, ion, or other beams is a natural for PA41s. There are still jobs for vector-scan CRTs. And laser printers haven't totally replaced ink-jet machines. In an ink-jet printer, high-voltage op amps not only deflect the charged ink droplets, but also drive the piezo pump that spits them out. Even if these applications operated continuously, very little power would be required from the op amp. Therefore, it may not require heat sinking, because quiescent current is just 2 mA maximum, or only about 700 mW with 350 V between supply pins.

The piezo-driven micropositioning motors used for the Strategic Defense Initiative (SDI) are similar in concept to devices called "inchworms." They're widely used in optical instruments and systems whose designers continue to search for ways to lower their cost. These applications may not need heat sinking of the package either, due to a very low operational duty cycle. In addition, the load is strictly ac, so dc stability isn't critical.

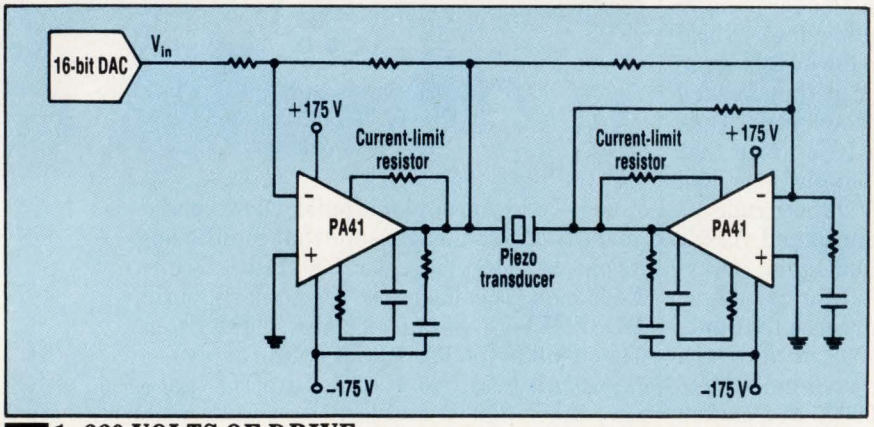
The inchworm is also finding its way into the scanning-tunneling microscope (STM) as the positioning device. Though the STM is currently a research-lab tool, its use will spread to industry as cost comes down, following the lead of the scanning-electron microscope (SEM). These motors can also "tune" the ring-laser gyros used in inertial navigation systems. Piezo drive also includes acoustic applications ranging from phased-array sonars to non-destructive-materials testing and ultrasonic human-body scanning, and may well lend themselves to flat-panel electrostatic loudspeakers.

Instrument applications extend from ATE pin drivers to high-voltage, precision programmable voltage sources, from dc to the PA41's full-power bandwidth (typically 26 kHz). In ATE jobs, the PA41 can supply low-cost, precision testing of high-voltage discrete devices, ICs, electroluminescent and vacuum-fluorescent displays, pc boards, and even systems. It can be connected as an oscillator/multivibrator and produce a waveform itself, or take it from a lower-level source. In a high-voltage power supply, the PA41 can replace the error amplifier, now built from discrete devices. In laboratory biomedical instruments, it can replace the high-voltage op amps which are often still vacuum-tube units (30-to-40-year-old Philbrick K2s), used for muscle and electrochemical stimulation.

Analog computation, which is ideal for some types of real-time simulation, represents another venue where PA41s can replace tubes. High-voltage op amps increase dynamic range. Because the PA41's input transistors are p-channel MOSFETs, the op amp's typical bias current runs 5 pA (50 pA maximum). A formidable integrator could be built with it.

You could build a 0-to-60-mA current source with 350 V of compliance. Such a current source could push 60 mA through 6000 Ω or 0 to 1 μA through 350 MΩ. A difference amplifier, or even an instrumentation amplifier offering a common-mode-voltage (CMV) range limited only by the supply rails could be built. A pair of PA41s produces a high-voltage precision full-wave rectifier (absolute-value circuit). With the ability to handle high CMVs, swing its output 300 V, and put out 60 mA, the chip should find applications as a comparator, with or without hysteresis. A modification of the integrator turns it into a sample-and-hold amplifier.

If you're designing your own high-voltage op amps, or using a hybrid like an Apex PA83 that employs bipolar output transistors, you know that second breakdown of the bipolar output transistors limits maximum continuous power output. Because the PA41's output devices, Q_3 and Q_{14}, are vertical DMOS transistors, you don't have to worry about second



1. 660 VOLTS OF DRIVE is provided by a pair of PA41 op amps, driven by a 16-bit digital-to-analog converter. The voltage drives a piezo transducer in 5-mV increments.

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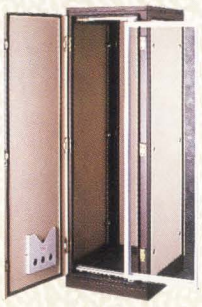

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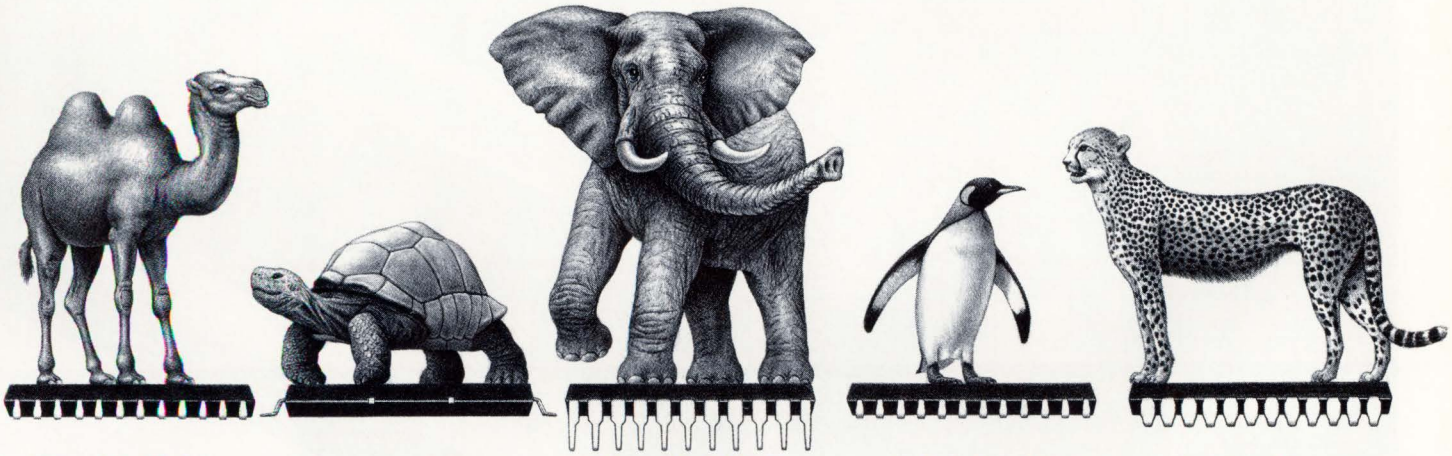

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	CXK581000M	100/120	SOP 525mil	L/LL	B/X	Now
	CXK581100TM	100/120	TSOP (normal)	L/LL	B/X	Now
	CXK581100YM	100/120	TSOP (reverse)	L/LL	B/X	Now
	CXK581001P	70/85	DIP 600mil	L/LL		Now
	CXK581001M	70/85	SOP 525mil	L/LL		Now
	CXK581020SP	35/45/55	SDIP 400mil			Now
	CXK581020J	35/45/55	SOJ 400mil			Now
128Kx9	CXK77910J	17/20	SOJ 400mil		Sync ASM	3/Q '91
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L = Low LL = Low,Low B = 3 Volt X = Extended Temperature

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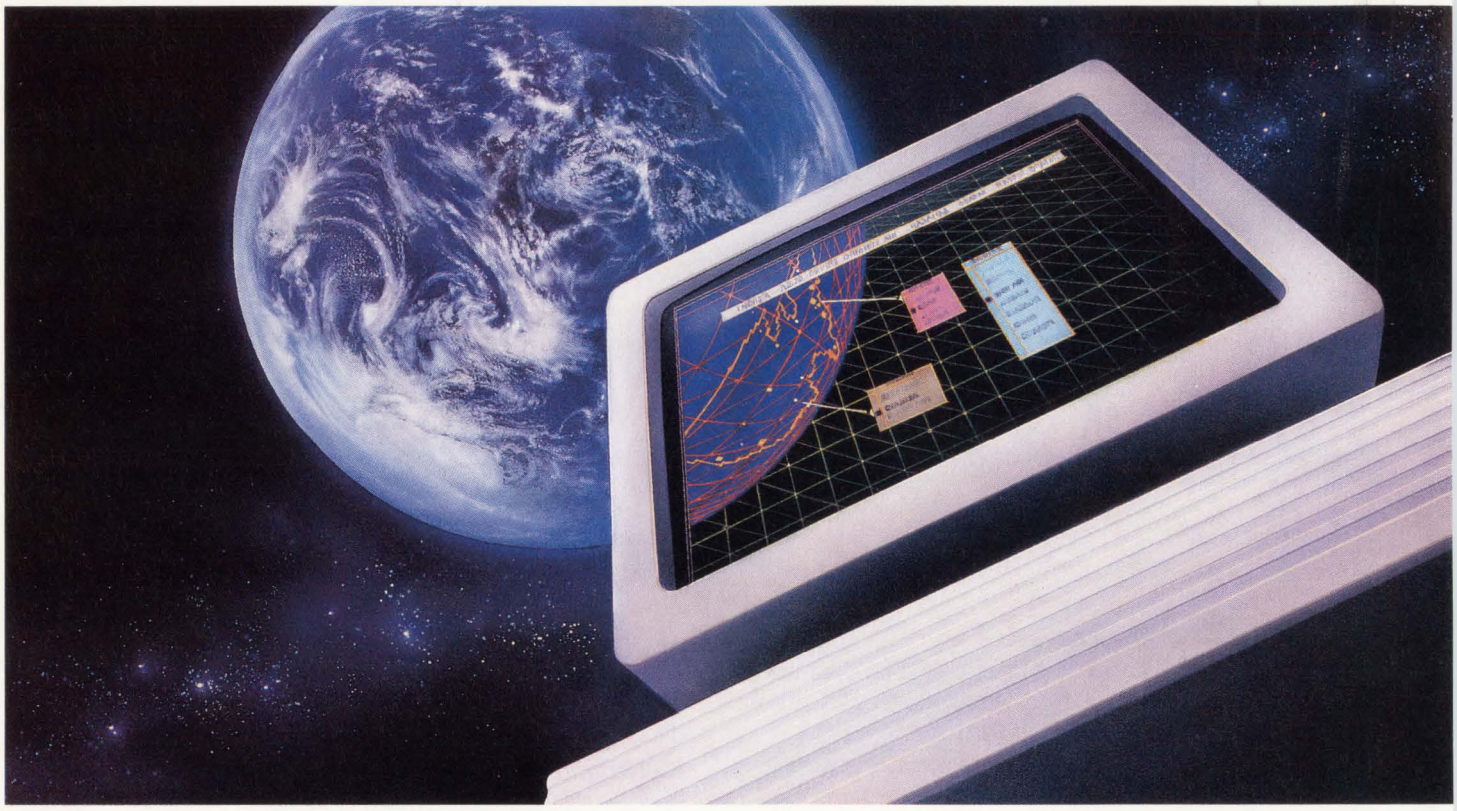

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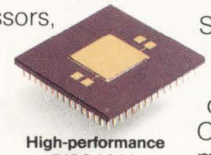

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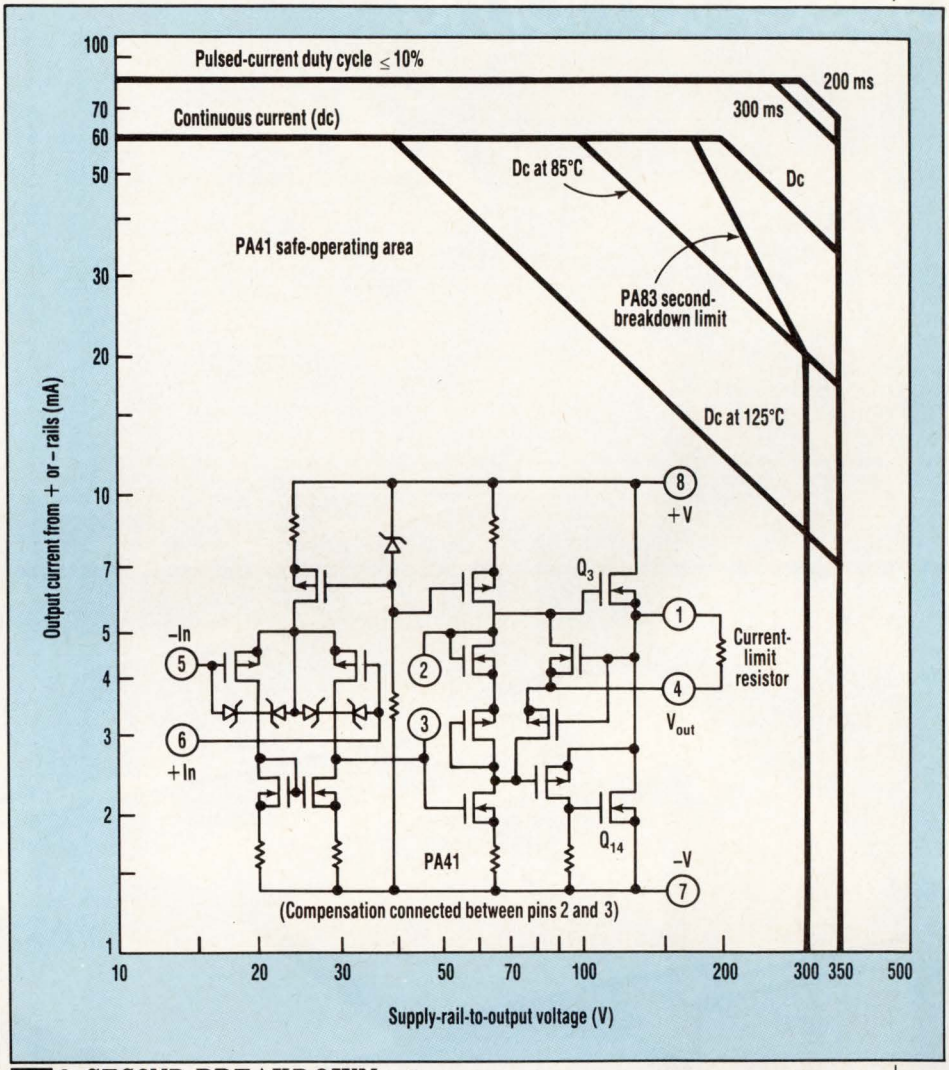
breakdown *(Fig. 2)*. Just keep your operating point within the device's safe-operating area. The chip's power output is limited only by the current-handling capability of the die's metallization, the temperature of the output MOSFETs, and their breakdown voltage. Provision is made for an external current-limit resistor. In addition, the input is protected for CMVs to the supply rails and for differential voltages to 16 V. Differential voltages above 16 V are clipped.

The chip isn't made for video applications. However, it handles audio quite well and a set of distortion curves are supplied. For example, putting 180 V pk-pk across 2 kΩ and running at a closed-loop gain of 20 results in distortion of 0.002%, 0.02%, and 0.2%, at 0.1, 1.5, and 15 kHz, respectively. Distortion is still less than 1% at 30 kHz.

External frequency compensation with just four parts enables users to optimize gain and bandwidth. In this case, use a 2.2-kΩ resistor and 1 of 3 capacitors: 18 pF for gains of 1 to 10, 10 pF for gains from 10 to 30, and 3.3 pF for gains above 30. Unity-gain bandwidth is 1 MHz. The power bandwidth noted earlier occurs when using the 3.3-pF compensation capacitor. Power bandwidth drops to about 8 kHz compensated for unity gain. Small-signal settling time for a 10-V step, to 0.1%, typically runs 12 μs at a gain of –10.

Although really not designed for single-supply operation, by keeping the common-mode voltage at the PA41's inputs biased 12 V inside of either supply rail allows it to perform well in this configuration. Just apply the same biasing tricks you would use with any conventional (non-single-supply) op amp when running off a single supply. But keep in mind that the output can only reach to within 12 V of each rail. Unsymmetrical supplies greatly simplify biasing, making it possible for the output to swing through zero. For example, if the IC is running off a positive high-voltage supply, connect it's negative supply pin to –15 V. If your high-voltage rail is negative, connect the IC's plus-supply pin to +15 V. In most applications, only the chip's quiescent current (2 mA) is required from the extra 15-V rail. A charge pump easily provides it.



2. SECOND BREAKDOWN isn't a problem with the Apex PA41 high-voltage op amp, regardless of the type of load. That's because the op amp's output devices, Q_3 and Q_{14}, are DMOSFETs, rather than bipolar transistors like those used in Apex's earlier PA83.

The PA41's offset voltage runs a maximum of ±30 mV. That may sound high, but it's about the equivalent of a conventional op amp with ±2 mV of offset. If you figure typical applications will use a ±10-V input signal, 30 mV represents 0.3% of full scale. Offset varies 65 μV°C, which only adds another 3.6 mV (0.03% of full scale) over the –25 to +85°C operating range. In an ac application or in a feedback loop, 30 mV of offset voltage won't put the op amp into saturation—even at a gain of 100.□

PRICE AND AVAILABILTY

The PA41 die is mounted on a thin aluminum-nitride substrate that isolates all inputs, outputs, and pins from its hermetically sealed, 8-pin TO-3 metal can. Thus, no insulation is needed between it and a heat sink—regardless of the sink's voltage. In quantities of 100, the PA41 goes for $39 each. Die are also available for use in hybrids at $29 each in hundreds. Both are available from stock.

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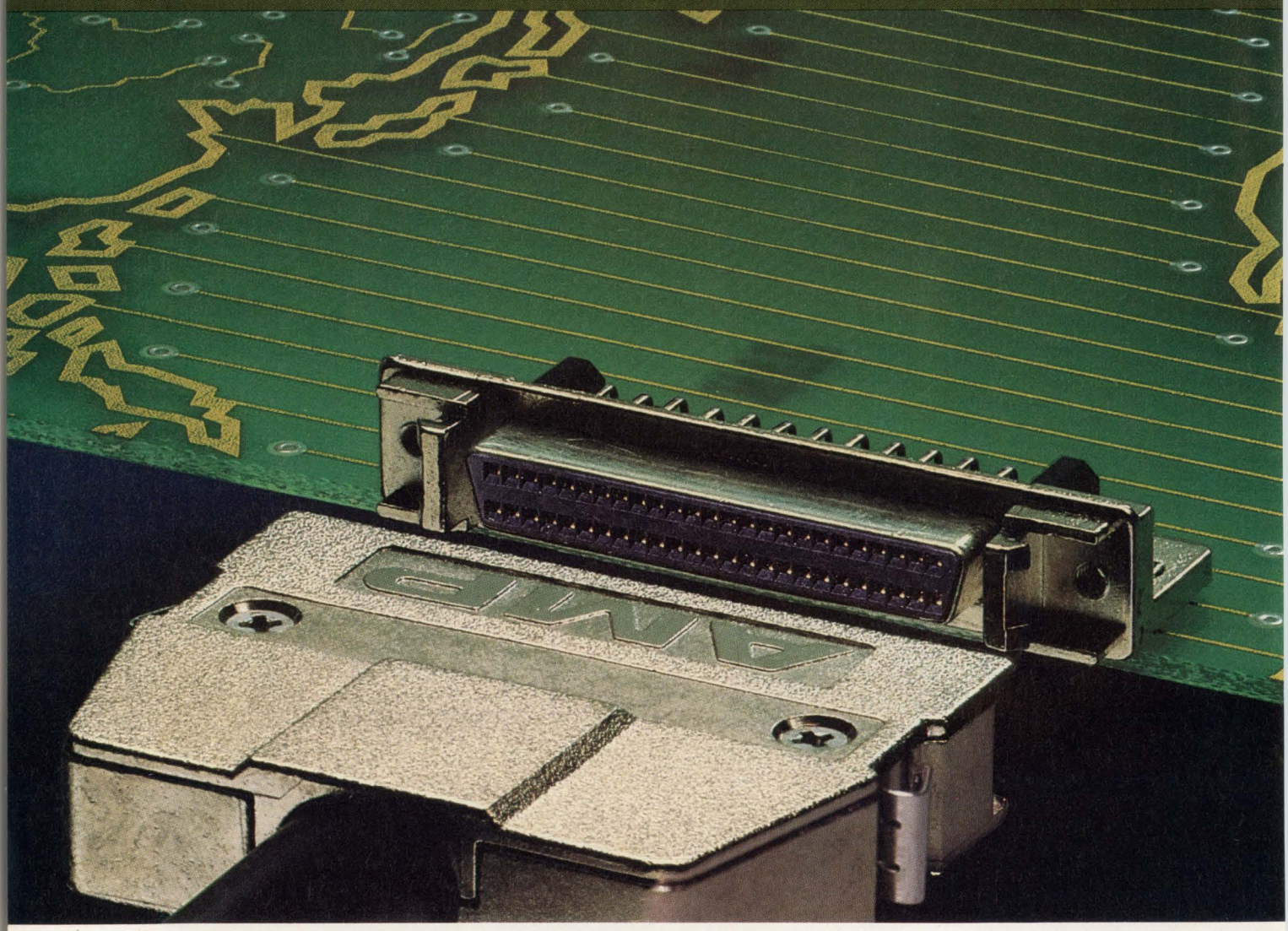

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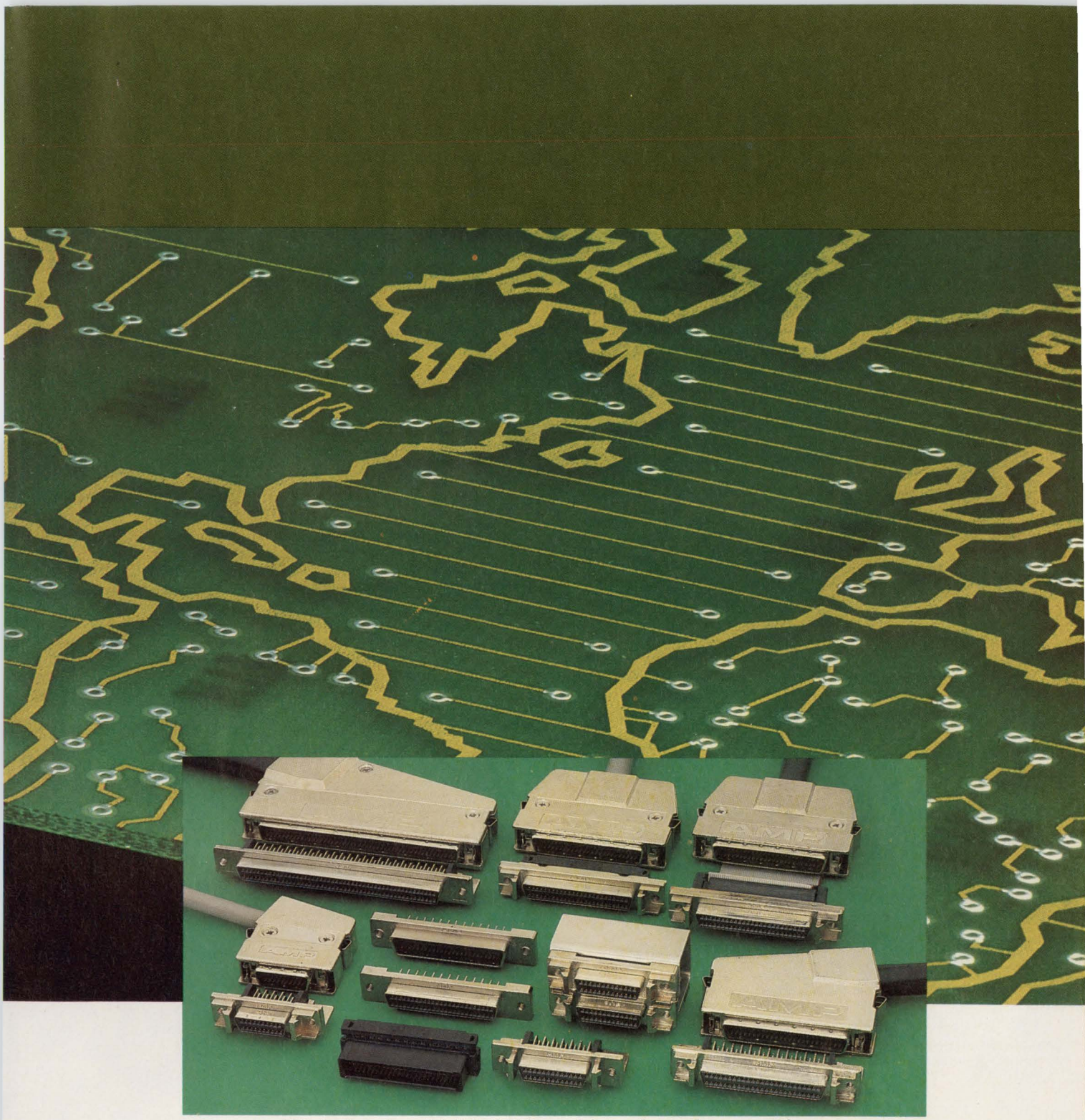

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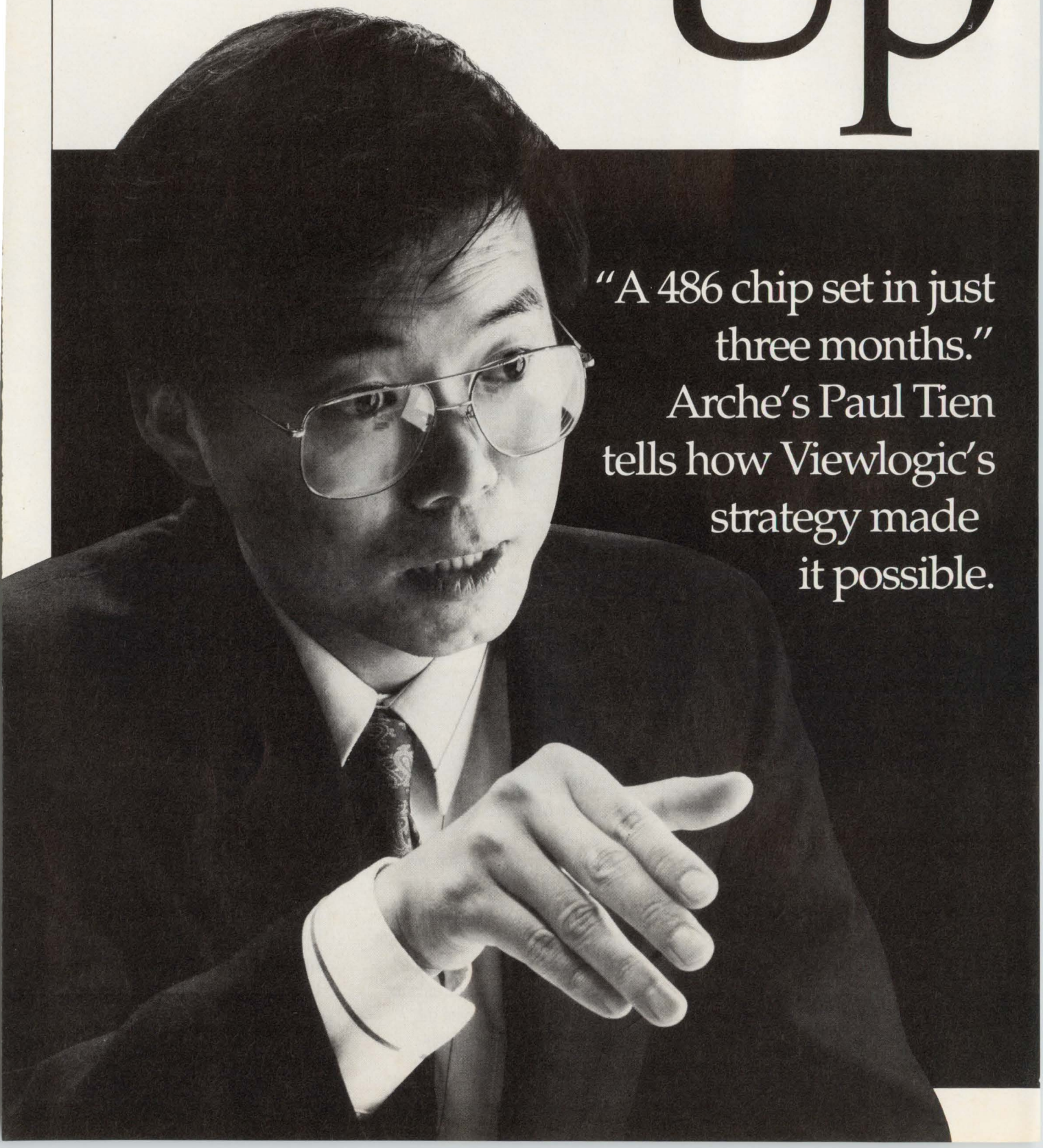
"Up



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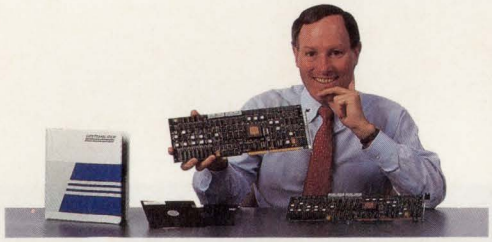

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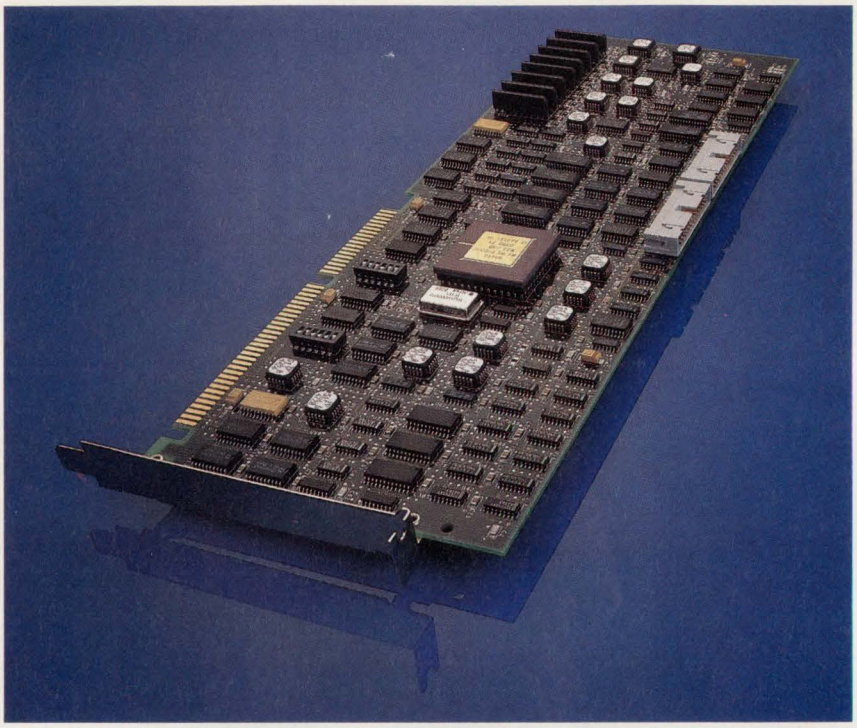

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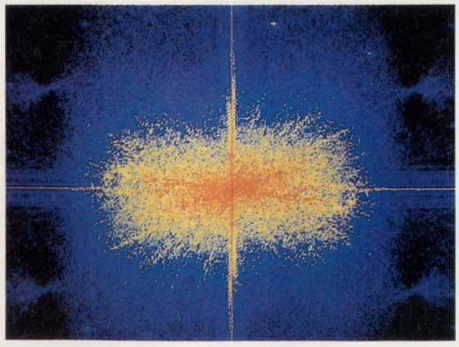

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RISC AND CISC PROCESSORS TARGET EMBEDDED SYSTEMS

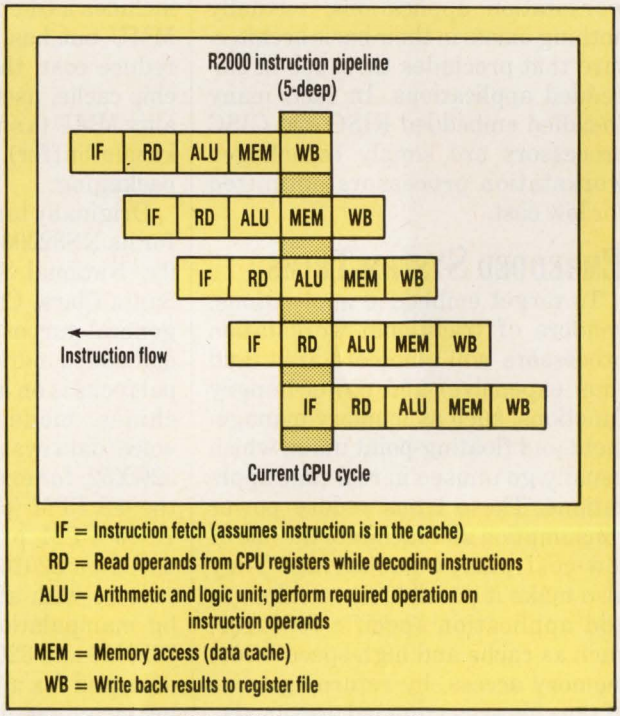
EXPLOIT THE ARCHITECTURAL OPTIONS OFFERED BY RISC AND CISC CPUS TO BEST MATCH A CPU TO THE SYSTEM.

TODD WYNIA
Heurikon Corp., 8000 Excelsior Drive,
Madison, WI 53717; (608) 831-0900.

Originally designed to be the heart of workstations, high-end 32-bit RISC and CISC microprocessors and their offshoots are beginning to target more lucrative embedded systems applications. Among these are laser-printer control, simulation accelerators, factory automation systems, and communications applications, such as protocol processing and high-speed switching.

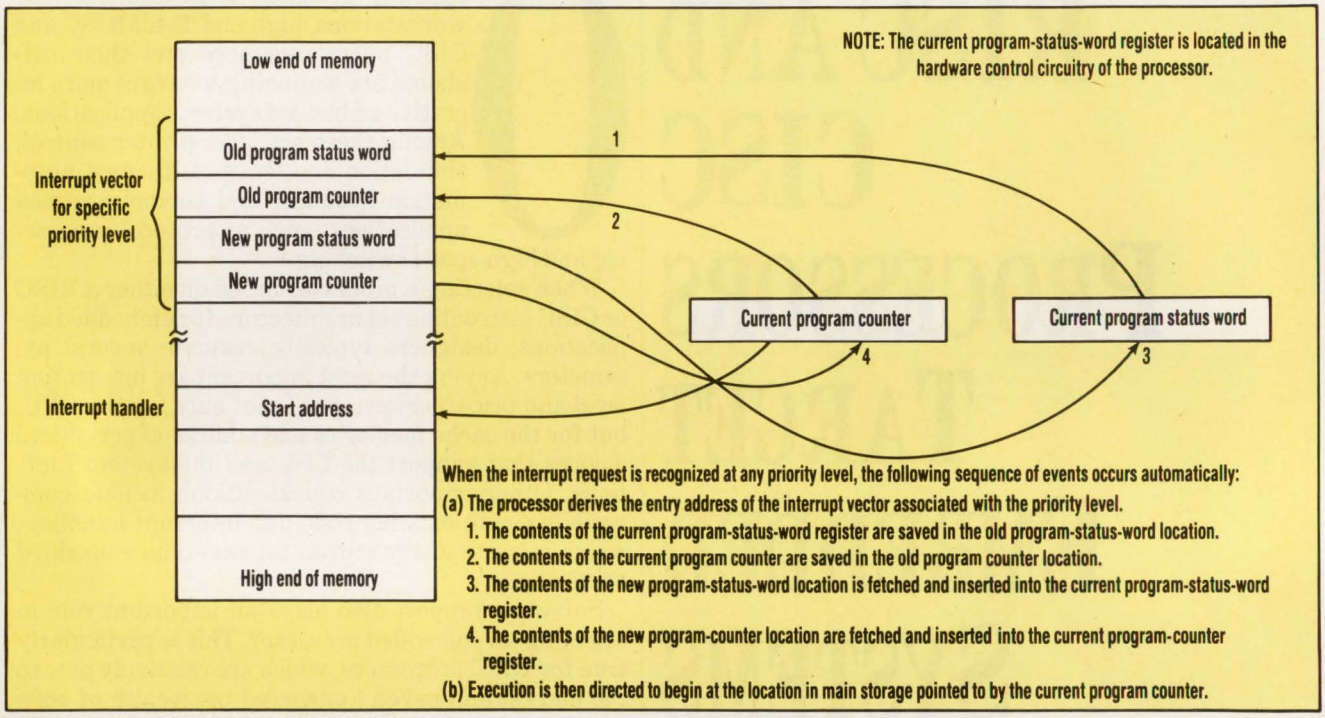
When selecting a processor based on either a RISC or CISC instruction set architecture for embedded applications, designers typically evaluate several parameters. Among the most important are integration level and price/performance—not only for the CPU, but for the cache memories and additional peripheral devices that support the CPU and the system functions. Other important considerations include compatibility with existing code and interrupt handling, which is particularly crucial for real-time embedded applications.

Software support also plays an important role in selecting an embedded processor. This is particularly true for RISC processors, which are relatively new to the market and haven't garnered the wealth of software and hardware support tools already available for many CISC devices. Still, support for RISC processors is improving, with many companies offering high-quality compilers, debuggers, cross development tools, and real-time operating systems.



1. BY EXECUTING PORTIONS of multiple instructions in parallel, thanks to five stages of pipelining, processors like the MIPS R2000 can achieve an instruction execution rate that approaches one per clock cycle.

RISC AND CISC FOR EMBEDDED CONTROL



2. CISC AND RISC PROCESSORS use a similar conceptual model for handling interrupts. They differ primarily in the relative delegation of the those operations to internal microcode, the operating system, and the interrupt handler.

While most high-end RISC and CISC processors were designed for workstation applications, virtually nothing exists in their basic architecture that precludes their use in embedded applications. In fact, many so-called embedded RISC and CISC processors are simply repackaged workstation processors optimized for low cost.

EMBEDDED SYSTEM TRIMS

To target embedded applications, vendors of traditional workstation processors will eliminate area (and thus expensive) and power-hungry functions, such as memory-management and floating-point units, which usually go unused in real-time applications. These trims reduce power consumption and facilitate the use of low-cost plastic packaging. They also make it possible for vendors to add application specific features, such as cache and high-speed direct memory access, by returning some of the chip area trimmed previously.

One vendor taking this approach is Integrated Device Technology Inc., Santa Clara, Calif. IDT offers a family of parts based on the MIPS R3000 CPU. As offered by MIPS Inc., Sunnyvale, Calif., the R3000 processor includes a 64-entry, fully associative MMU but has no on-chip cache. To reduce cost, the IDT 3051 adds on-chip cache, uses a reduced-functionality MMU (a smaller translation lookaside buffer), and employs plastic packaging.

Originally targeting Unix systems for its NS32000 CISC processor family, National Semiconductor Corp., Santa Clara, Calif., has adapted the general-purpose processors for the embedded market. National's principal focus is on laser printers, fax machines, modems, and integrated voice/data systems. The 32CG16 and 32GX32, for example, which address the 4-8 PPM (page per minute) and 10-15 PPM printer markets, are based on 32016 and 32532 core processors with added instructions for bit manipulation and graphics. The 32FX16 and 32GX320 add voice, modem, and fax application capabilities by including digital-signal-processing instructions and a hardware 16-by-16-bit multiplier.

Motorola Inc., Austin, Texas, has gone several routes toward targeting the embedded market with its CISC family. One angle is to offer MMU-less versions of the 68020, 68030, and 68040 in plastic packages. Dubbed the EC Series, these devices are offered at a fraction of the cost of their full-function counterparts.

Another approach used by Motorola to cut control-function costs is to combine the 68000 core with various application-specific I/O functions. The 68302, for example, which targets communications applications, includes a trio of synchronous serial-communications channels, seven DMA channels, and a protocol engine that provides packet-framing and cyclic-redundancy-checking functions. Another chip, the 68332, is targeted at engine-control applications. This processor includes a time-processing unit that measures pulse width and frequency and calculates both rotation rate and the rotation's rate-of-change.

To cut costs for its 960CA, Intel Corp., Chandler, Ariz., omitted the MMU and reduced the on-chip cache's size. Unlike many high-end RISC devices that offer 2 kbytes or more of data and instruction cache,

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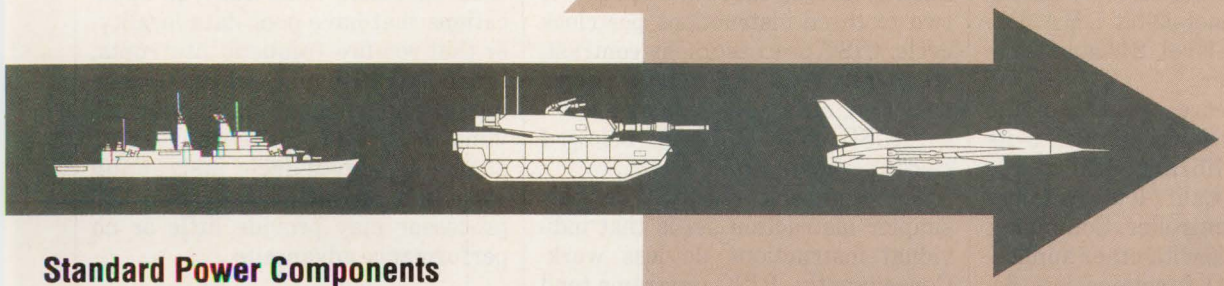

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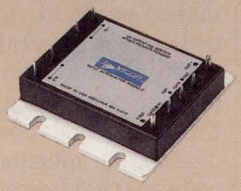

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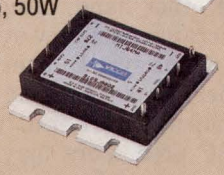

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RISC AND CISC FOR EMBEDDED CONTROL

the 960CA packs just 1 kbyte of 2-way-set-associative instruction cache. In place of a data cache, the chip uses a 1-kbyte memory-mapped on-chip static RAM, which may be used for both data storage and as a register cache. The 960CA also reduces overall system cost by including a four-channel 32-bit DMA controller and a 31-level, 248-source interrupt controller.

By offering core versions of the MIPS and Sparc devices as cells in its standard cell library, LSI Logic Corp., Milpitas, Calif., lets designers roll their own controller. Combining these RISC cores with other application specific I/O functions lets designers develop highly integrated devices that prove cost-effective for very-high-volume applications.

RISC Vs. CISC

One key issue when looking at a system upgrade for a CISC or RISC processor is compatibility with existing code. The advantage of upgrading within a family of CISC processors, such as the 680X0, is that it enables designers to run existing binary programs without recompilation. Switching to a new processor family (from a CISC to a RISC chip, for example), by contrast, requires recompilation of the source code, which may be unavailable. Even if the source code is available, the code may contain hardware dependencies that greatly complicate the conversion effort.

If, on the other hand, designers start from scratch on a new system or go for a major system overhaul, then price/performance is frequently the most important criteria. In this regard, RISC processors may provide the best solution. Because RISC chip suppliers aren't constrained by the need to maintain object code compatibility with previous generation parts, they are free to develop more aggressive architectures.

The reason that RISC processors generally outperform their CISC counterparts is because of their hardwired architecture (little or no microcode) and simpler, more orthogonal instruction sets. This simplicity enables compilers to schedule a RISC processor's pipeline more efficiently, thereby enabling the device to achieve execution speeds that approach one instruction per clock cycle. Superscalar architectures, such as Intel's 960CA, which use multiple execution units, can frequently attain execution speeds of two to three instructions per clock cycle. CISC processors, by contrast, frequently require 5-7 clocks per instruction, although some of the latest CISC chips are well below 4 clocks per instruction.

The drawback to a RISC device's simpler instruction set is that individual instructions do less work. Consequently, RISC programs tend to be 25-100% larger than equivalent CISC programs. From a performance perspective, this increase in code size is generally more than offset by the reduction in average CPI (clocks per instruction). However, the larger code size does put more demand on memory bandwidth and requires that larger, faster, and thus more expensive memories be used. Even given the relatively low cost of memory, this increase in code size may be a negative factor in some applications that are constrained by cost and size.

While a strong case can be made for the superiority of RISC architectures in general, it can't be said that RISC devices outperform CISC devices across the board. The reason is that RISC processors depend more heavily on efficient pipeline scheduling and high cache-hit rates to keep their execution units busy. In applications that have poor data locality, or that require frequent interrupts, branches, or context switches, cache misses and pipeline flushes will prevent the RISC processor from achieving single-cycle instruction execution. In such cases, the RISC processor may provide little or no performance advantage.

Memory Performance

When evaluating the price/performance of a CISC or RISC processor, off- and on-chip memory architectures should be closely scrutinized. This is particularly true for RISC processors. The pipeline in the MIPS R2000 is a typical example of how the various stages interact *(Fig. 1)*. By dividing the pipeline into five stages, as many as five instructions can be in various stages of execution at the same time. To keep their pipelines full, RISC processors must fetch a new instruction on each clock cycle. Unless the data is encoded within the

COMMON OPTIMIZATIONS PERFORMED BY CISC AND RISC COMPILERS

Optimization name	Explanation
High-level	At or near the source level; machine independent
Procedure integration	Replace procedure call by procedure body
Local	Within straightline code
Common subexpression elimination	Replace two instances of the same computation by single copy
Constant propagation	Replace all instance of a variable that is assigned a constant with the constant
Stack height reduction	Rearrange expression tree to minimize resources needed for expression evaluation
Global	Across a branch
Global subexpression elimination	Same as local, but this version crosses branches
Copy propagation	Replace all instances of a variable A that has been assigned X (A=X) with X
Code motion	Remove code from a loop that computes same value each iteration of the loop
Induction variable elimination	Simplify/eliminate array-addressing calculations within loops
Machine dependent	Depends on machine knowledge
Strength reduction	Many examples, such as replace multiply by a constant with adds and shifts
Pipeline scheduling	Reorder instructions to improve pipeline performance
Branch offset optimization	Choose the shortest branch displacement that reaches the target

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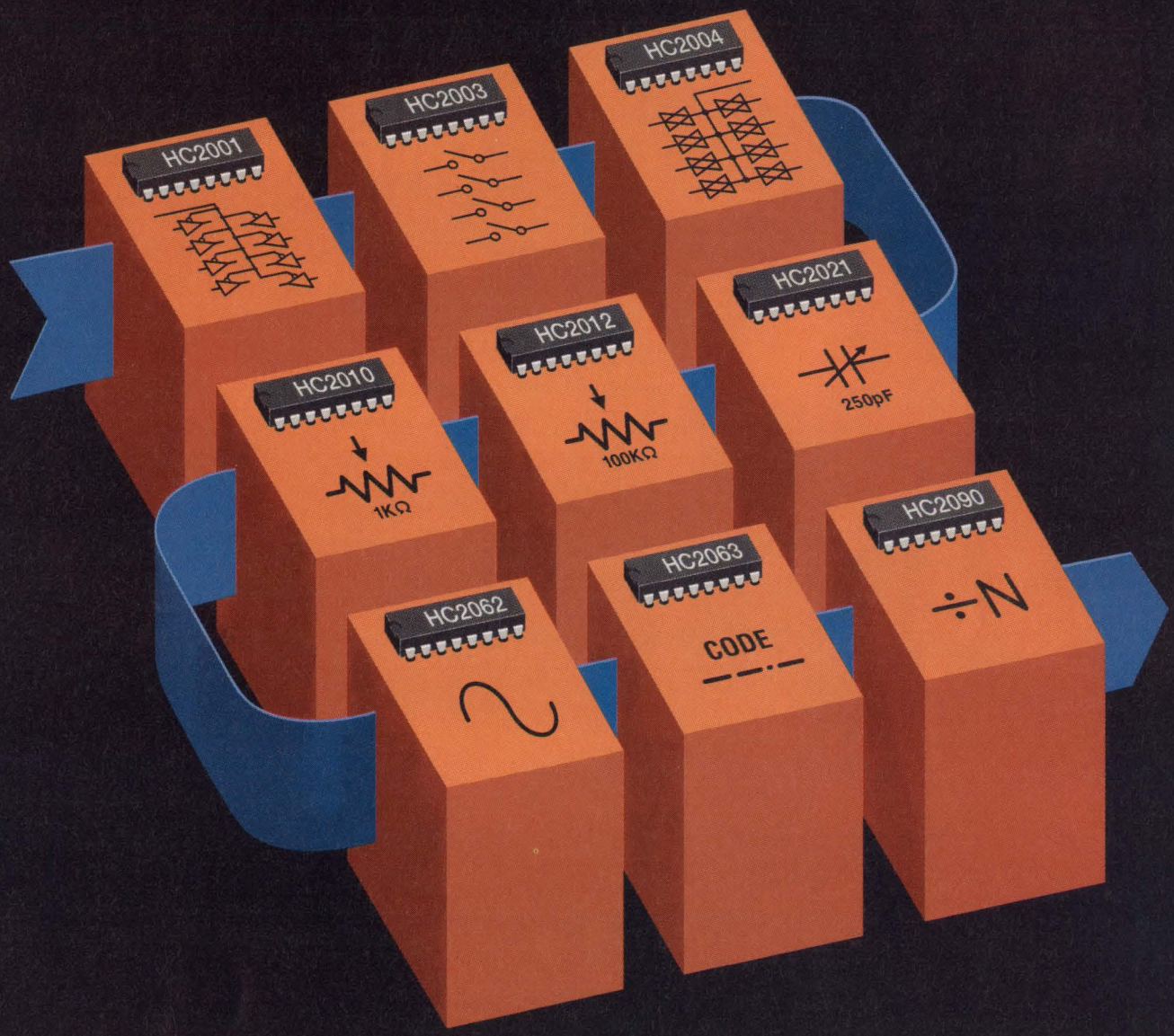

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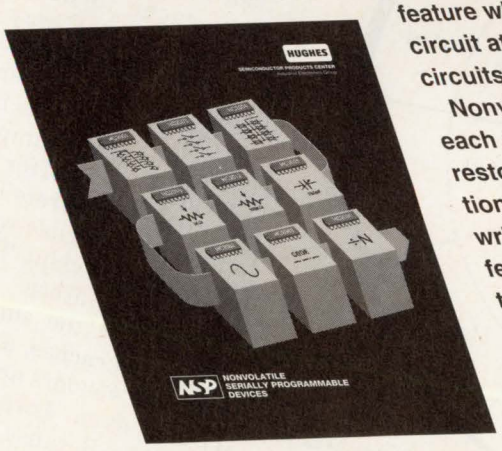

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RISC AND CISC FOR EMBEDDED CONTROL

instruction or stored in an on-chip register, the processor may also need to fetch new data from external memory.

The high cost of designing external no-wait-state memory subsystems is forcing designers of most RISC and CISC processors targeting embedded applications to provide increasingly larger on-chip data and instruction caches. One of the first 32-bit microprocessors to provide on-chip cache was the 68030, which provided 256 bytes each of direct-mapped instruction and data cache. One of the first RISC devices to include cache was the Am29000 from Advanced Micro Devices Inc., Austin, Texas, which provides a 32-word (32-bit words) Branch Target Cache to speed instruction access and a 128-word triple-ported register file to speed data access.

Since then, advances in process technology have made it easier to use much larger caches. The AMD 29030, for example, has substituted an 8-kbyte, 2-way set-associative cache for the 32-word Branch Target Cache used in the 29000. Similarly, the Motorola 68040 substitutes 4-kbyte, 4-way set-associative instruction and data caches for the 256-byte caches provided on the 68030. MIPS, which provided no on-chip cache for its earlier generation parts, added 8 kbytes each of direct-mapped data and instruction cache to the R4000.

CACHE BENEFITS

The availability of large on-chip caches greatly reduces system cost by enabling designers to configure their external memory systems using less expensive dynamic RAM. A 960CA-based HK80/V960E VMEbus board from Heurikon, for example, uses an 8-Mbyte main-memory based entirely on 70-ns static-column dynamic RAMs. By employing a 2-way interleaved architecture, such a memory subsystem can support zero-wait-state accesses for either single-write or burst transfers.

Cache implementations vary widely among RISC and CISC processors, both in size and in architecture. For the most part, the instruction and data caches provided on today's RISC and CISC microprocessors are physical caches—in other words, they store physical, rather than virtual, addresses.

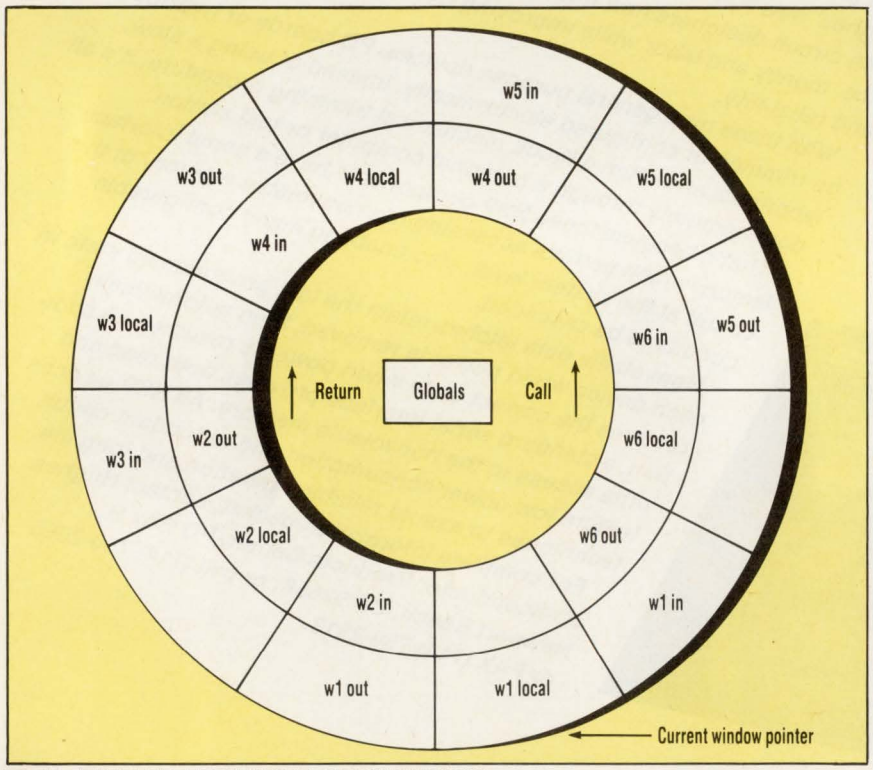
Most of the data caches provided on today's RISC and CISC processors use a "copy-back" strategy of maintaining consistency between the cache and main memory. Relative to write-through caches, which write through to main memory each time an address in the cache is written, copy-back caches update main memory only after a block in the cache (that has been written to) is displaced.

The advantage of a copy-back cache is that writes to the cache can be achieved with zero wait states, because the CPU doesn't have to wait for the data to be written through to main memory. Moreover, if several locations within the same block are modified, then only one write operation to main memory will be required when the block is displaced, thereby conserving memory bandwidth.

SIMPLE CACHES

One way caches will differ is in their level of associativity. The simplest cache to build is a direct-mapped cache (1-way set associative). In a direct-mapped cache, each address in main memory may be stored in only one cache location. Because of their simplicity, direct-mapped caches offer faster hit times (2-10% in a discrete implementation, though negligible when the cache is included on chip). They also require smaller die areas.

Despite the simplicity of direct-mapped caches, an increasing number of vendors are opting for 2-way and even 4-way set-associative caches. Because these caches enable several addresses (for example, two in a 2-way set-associative cache) in main memory to be mapped to multiple addresses in the cache, they offer higher hit rates than direct-mapped



3. THE SPARC IMPLEMENTATION of register windows uses between 6 and 32 (six shown here) overlapping windows, which are organized as a circular buffer. Each window contains 24 working registers and 8 global registers, logically divided into 8 In registers, 8 Local registers, and 8 Out registers. Parameters are passed between one window's Out registers and the next window's In registers. A pointer keeps track of the currently active window.

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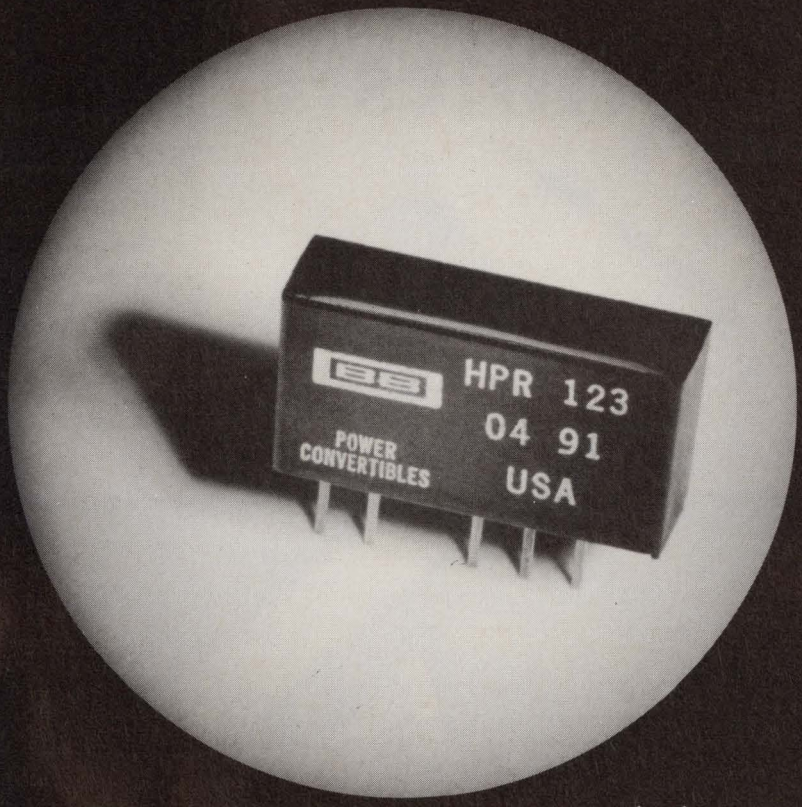

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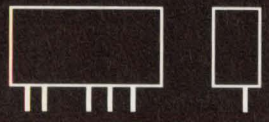

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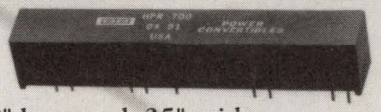

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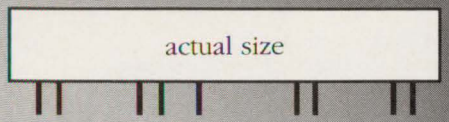

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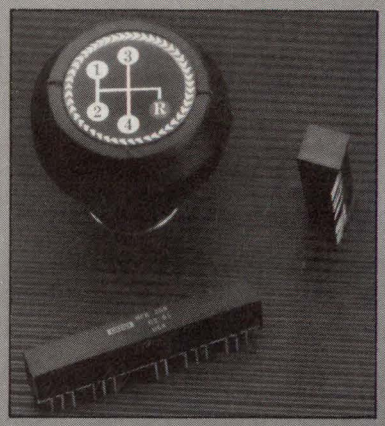

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caches of the same size.

As a rule, increasing cache associativity also increases cache hit rates. However, a point of diminishing returns is quickly reached. Beyond 4-way set associativity, additional increases in associativity provide relatively small increases in hit rate and don't justify the additional expenditure of die area.

CACHE PERFORMANCE

While general comparisons can be made between cache architectures, establishing the hit rate of any particular cache is impossible without considering the application. Because programs generally tend to be stored sequentially and loop frequently, instruction caches have higher hit rates than data caches. However, the hit rate of any particular instruction cache can vary widely depending on the application.

In real-time embedded applications, because programs are often small and have few tasks active simultaneously, even relatively small instruction caches can provide high hit rates. Unix systems, by contrast, tend to have much lower hit rates. This is because Unix systems switch frequently between large programs.

Data cache hit rates are usually even more application dependent. Display processing applications, for example, tend to exhibit very low hit rates. Here, the data set (for example, 1 Mbyte for a 1024-by-1024-by-8-pixel display) greatly exceeds the cache size. Moreover, data isn't typically accessed consecutively or reused frequently.

To see why, consider the movement of a cursor. Here, few of the pixels that form the cursor are located on any one line. Consequently, to draw the cursor (or calculate its new position when it is moved), the processor must change lines frequently. Because consecutive lines are located 1024 bytes apart (for a display with 1024 pixels per line), the processor must step through the data set as much as 1024 bytes at a time in order to calculate consecutive pixel locations. Moreover, once the processor accesses the pixel memory, it's not likely to access that pixel again in the near future.

An example of an application with a high hit rate is Postscript processing, which involves the transformation of a Postscript page description to a bit map. Because the transformation is compute-intensive and requires using multiple operations on the same data, data tends to be reused frequently. Another application that will have large hit rates is missile guidance. Again, because the data (the terrain map) changes slowly with respect to the operations (contour calculations) performed on the data, data is reused frequently and the hit rate is high.

```
Muli    r4,r5,r6     # r6 is scoreboarded
Addi    r6,r7,r8     # add must wait for the previous multiply
                     # to complete
                     .
                     .
                     .
muli    r4,r5,r10    # r10 is scoreboarded
and     r6,r7,r8     # and instruction is executed concurrently with multiply
```

4. REGISTER SCOREBOARDING allows RISC processors like the 960CA to concurrently execute instructions that are out of order by keeping track of register usage and data dependencies, as illustrated with the dual multiplications, an addition, and an AND operation.

INTERRUPT RESPONSE

Another important factor in selecting a RISC or CISC processor for real-time embedded applications is how quickly and predictably the device responds to external interrupts. In a CISC processor, the bulk of the operations that must respond to an interrupt are handled automatically in microcode. RISC processors, by contrast, typically leave more of this functionality to the real-time operating system or interrupt handler.

Conceptually, the interrupt sequence for most CISC and RISC processors is similar to that used in the 68030 and 68040 *(Fig. 2)*. Once the 68040 receives an interrupt, it discontinues execution at the next instruction boundary, which could be asB#[]B(B+B.'B2$B6G clocks later if it just started a multiplication or division operation.

It then initiates an interrupt acknowledge cycle, during which it obtains an interrupt vector from the interrupting device. This vector points to an exception table in main memory (256 32-bit entries), which contains the starting address (program counter value) for the interrupt handler (autovectored devices like the 960CA avoid obtaining an exception vector by associating a specific handler with each interrupt level).

Once the 68040 obtains an interrupt vector, it makes an internal copy of its program counter and processor status word and switches from user mode to supervisory mode. It then stores a four-word stack frame to main memory (under direction of the OS), which includes the program counter, status register, and interrupt vector. The 68040 also saves any registers used by the handler in the stack frame. If the handler is written in C, the entire register set is usually saved.

After storing the stack frame, the 68040 fetches the program counter from the exception table, which supplies the start address for the interrupt handler. The processor then executes the handler. The last instruction in the handler, which is a Return From Exception, reverses the processes and restores the program counter and status register for the interrupted task.

If multiple devices interrupt the 68040 simultaneously, then the 68040 services the highest-priority interrupt. If the 68040 is interrupted while it is servicing another interrupt, it compares the priority of the new interrupt with the current interrupt. If the priority of the new interrupt is higher (except for a nonmaskable interrupt, which is serviced immediately), it saves the context of the current interrupt to a stack frame in main memory and begins servicing the new interrupt. Once it services the new interrupt, it retrieves the context for the previous interrupt from the stack frame and resumes execution of its handler.

Calculating a processor's inter-

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rupt latency (the time from the receipt of the interrupt to the execution of the handler's first instruction) is difficult because it depends on several factors. Among these are the execution time of the instruction that was interrupted, the speed of the external memory, and both the priority level and total number of interrupts that are received.

It also depends on how many registers must be saved in order to restore the interrupted task's context. In the 68040, for example, assuming zero-wait-state memory and that the interrupted instruction completes on the next cycle, the interrupt latency for an individual interrupt is 24 clocks plus 2 clocks for each register that's saved.

Interrupt Response

One advantage that RISC processors have when responding to interrupts is their finer instruction granularity. Because a device can't process an interrupt until it completes its current instruction, the RISC processor's shorter average execution time enables it to respond more quickly. Finer granularity also makes RISC chips less likely to receive an interrupt in the middle of an instruction. That minimizes instruction restarts, thereby improving performance and simplifying memory system design.

On the down side, one disadvantage of many RISC chips is that they pay a greater penalty for the pipeline flushes following the receipt of an interrupt. RISC devices also generally have slower context-switch speeds. This is because they generally have more registers, which increases the time required to save the state of the processor prior to servicing an interrupt.

The AMD 29000, for example, which provides 192 registers, requires at least 192 clocks to save its entire register set to main memory (assuming zero-wait-state memory). This overhead can be diminished by saving only the registers that the interrupt handler uses. However, if the handler happens to be written in a high-level language, then working with a portion of the register set is often difficult.

Register windows used by RISC devices, such as the Sparc and 960CA, help speed context switching (for interrupts and procedure calls) *(Fig. 3)*. The strategy behind register windows is to minimize the number of registers that must be saved to external memory on a context switch by providing a large register stack on chip. Following a context switch, the processor leaves the register contents intact and gives the new process a fresh set of registers by moving the stack pointer to a new window, rather than saving the current process' registers to main memory. This takes only four clock cycles on both the Sparc-family processors and 960CA.

In the 960CA, the register stack is implemented using an on-chip 1-kbyte memory-mapped static RAM. This stack, which may also be used for data storage, provides 5 to 15 windows with 16 local registers each. Following an interrupt or procedure call, the new process is given a new set of 16 registers. Then, when the processor resumes execution of the interrupted process, it simply moves the stack pointer back to that process' window.

Register windows provide a high-speed mechanism for handling individual interrupts. However, in interrupt-intensive applications, such as telecommunications switching, their advantage is diminished. In such cases, the maximum window number may often be exceeded. Therefore, to provide a fresh set of registers for the new process, the processor must write the registers in the least recently used window to a stack frame in main memory.

Optimizing Compilers

Of course, when assessing the performance of RISC and CISC processors, the quality of the optimizing compilers available for that specific CPU can't be overlooked. This is particularly true for RISC processors, whose compilers must be more complex to take advantage of the device's larger register sets and exposed pipelines.

One of the most common optimizations compilers can make—register allocation—is actually one of about a dozen common optimizations done by a compiler *(see the table)*. In register allocation, the compiler moves frequently accessed variables from main memory into on-chip registers, thereby reducing the external memory accesses required at run time.

Another point to consider is that RISC processors offer a number of architectural features that enable optimizing compilers to generate fast-executing code. One is a large general-purpose register set, which enables the compiler to more effectively implement register allocation. Another is a three-operand architecture, which reduces the number of intermediate results that must be saved during many calculations.

In a conventional two-operand CISC architecture, the same register is often used as both a source and destination register for operands. Consequently, to prevent the contents of the source register (for example, if the register contains an intermediate result) from being overwritten, the processor must expend time saving the source register's contents to another register. In a three-operand architecture, this is unnecessary, because the destination register is always separate from the two source registers.

A third RISC feature that facilitates the generation of high-speed code design is its simpler, more orthogonal (all instructions can apply all addressing modes to all registers) instruction set. This simplicity not only reduces the special cases that the compiler must deal with, but enables the compiler to more effectively reorder instructions and schedule the pipeline.

To maximize scheduling efficiency and enable out-of-order instructions to execute concurrently, RISC processors, such as the 960CA and Motorola 88000, use a technique that is known as register scoreboarding. Register scoreboarding enables instructions to execute out of order by keeping track of register usage and data dependencies.

When an instruction is executed, the processor sets a register score-

RISC AND CISC FOR EMBEDDED CONTROL

board bit to indicate that a register or group of registers is being used in an operation. If the instructions that follow don't use registers in that group, the processor can execute those instructions before the prior instruction is completed. Register scoreboarding can be used, for example, to enable single-cycle instructions, such as Add, to execute concurrently with multiple-cycle instructions, such as Multiply and Divide *(Fig. 4)*. Scoreboarding permits the processor to schedule two multiplications, an addition, and an AND operation.

Delayed branching is one example of a scheduling optimization that takes advantage of instruction reordering. In delayed branching, the compiler identifies instructions prior to a branch whose execution doesn't depend on the branch. The compiler then reschedules these instructions so that the processor can execute them while it's waiting for its address generator to calculate the branch address. Unfortunately, scheduling optimizations like delayed branching may not prove to be as effective in the next-generation superscalar machines. However, they are indicative of the extra flexibility the RISC's simpler architecture provides.□

Todd Wynia, manager of product marketing at Heurikon, holds a B.S. in economics and mathematics from the University of Wisconsin at Madison.

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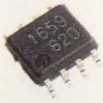

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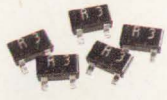

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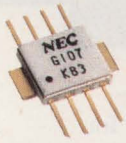

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BOUNDARY SCAN PUTS TOMORROW'S DEVICES TO TEST

BOUNDARY SCAN PROMISES TO CUT TEST-DEVELOPMENT TIME, BUT FOR NOW IT MUST COEXIST WITH IN-CIRCUIT TESTING.

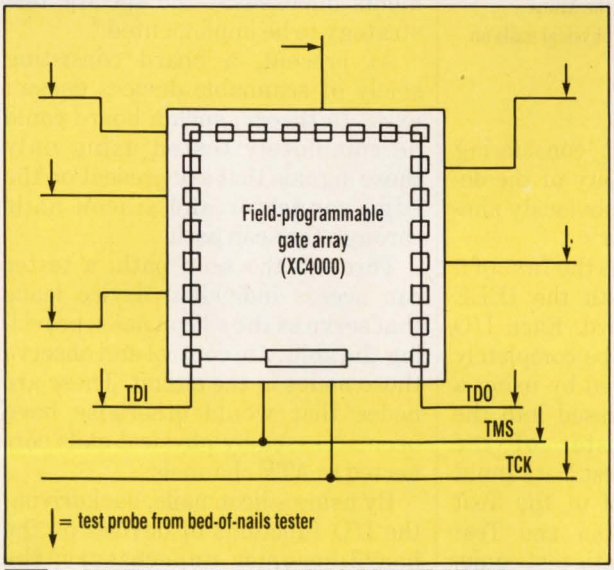
JIM DONNELL
Xilinx Inc., 2100 Logic Dr.,
San Jose, CA 95124; (408) 879-5960.

Although much has been written about the IEEE boundary-scan test standard, only a handful of today's devices meet the IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture. Complete compliance with the standard, which means that designers can choose virtually any device with the assurance that it's boundary-scan compatible, is still about five years away. Until then, printed wiring boards will be a mix of scannable devices that meet the IEEE standard and non-scannable devices. Such boards require test methodologies that employ both bed-of-nails and boundary-scan approaches.

Boundary-scan testing can slash test-development times for complex systems. Ken Parker, a member of the technical staff at Hewlett-Packard's Manufacturing Test Div., estimates that developing test vectors to adequately test the I/O functions of a complex device, like the Motorola 68040, would consume six months of an engineer's time.

In contrast, test vectors for the same device, given boundary-scan capability and the appropriate software tools, could be generated in two minutes. Never has the industry had the promise of such dramatic improvement in test-development time.

Boundary scan also promises to permit testing of systems employing high-density surface-mounted components and complex multilayer pc boards. Today, these systems can be tested with a bed-of-nails approach, but not without a plethora of problems because of the smaller pin geometries of surface-mounting technology. Again, with the right tools and devices that support boundary scan, the entire board could be fully tested using only the boundary-scan path.



1. UNTIL ALL DEVICES MEET IEEE boundary-scan standards, typical board testing will use a mixture of boundary-scan and bed-of-nails test methodologies. Besides the Test Data Input (TDI) and Test Data Output (TDO) lines, boundary scan requires Test Mode Select (TMS) and Test Clock (TCK) lines.

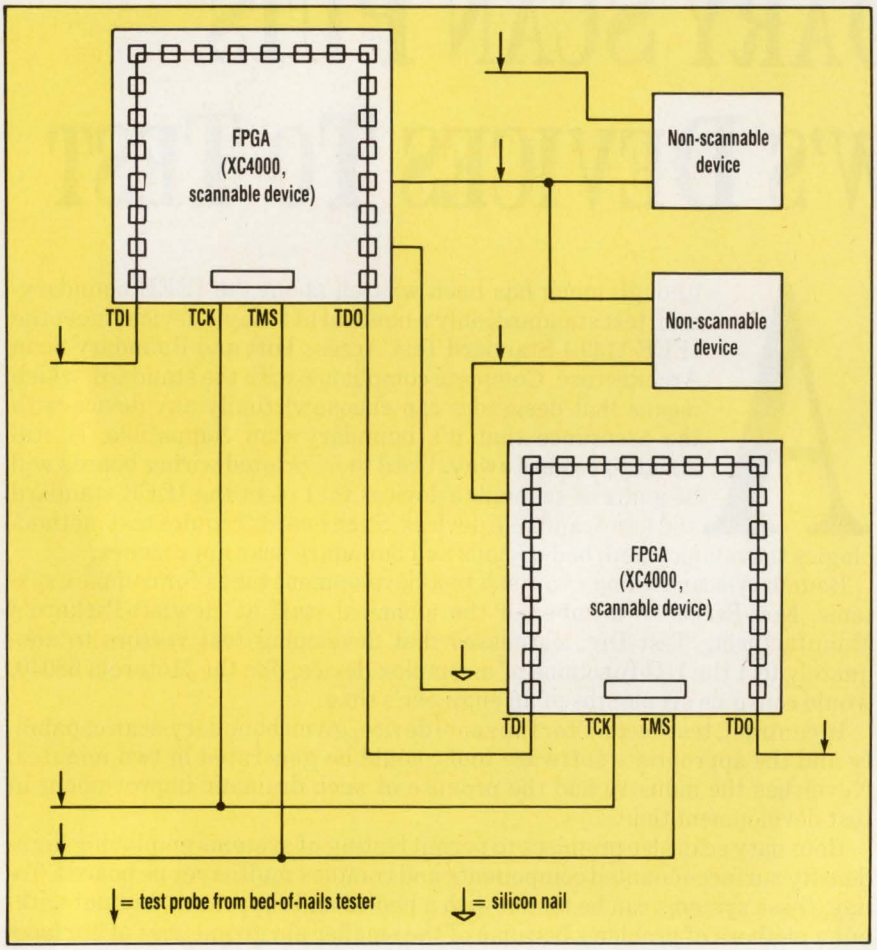
On the other hand, bed-of-nails or in-circuit test methods offer some significant advantages not present in boundary scan. One key advantage of in-circuit testing is the ability to diagnose failures—in the face of multiple failures, on one pass across the test head.

In addition, testing for shorts can be achieved before powering up the board, reducing the board's chance of a catastrophic failure because of shorts between power and ground.[1] In-circuit tests also allow comprehensive analog testing to occur along with digital testing.[2]

Boundary scan, in general, doesn't address testing of analog and passive devices. Until semiconductor manufacturers offer a wide range of devices with boundary scan, boards will be tested using traditional in-circuit tests, applying boundary-scan techniques only where necessary. Contrary to widespread belief, boundary scan and in-circuit tests aren't incompatible. Indeed, using a combination of boundary-scan and in-circuit testing can significantly simplify board testing *(Fig. 1)*.

First, let's address a system with only one scannable device. Assuming that this device is fairly complex and has a high pin count, it's easy to apply a mixed approach of boundary-scan and in-circuit test methodology. Take, for exam-

BOUNDARY-SCAN TESTING



2. FOR PATHS BETWEEN SCANNABLE DEVICES like the Xilinx XC4000 family of field-programmable gate arrays, silicon nails can replace physical nails on a bed-of-nails tester.

ple, the testing of highly integrated devices, such as the Xilinx XC4005 field-programmable gate array (FPGA).

These devices often make up much of a system's glue logic. Testing a device like this quickly becomes a nightmare compared with testing individual SSI and MSI components that originally made up the function. In highly integrated devices, test probes can no longer access internal nodes.

The test engineer then faces the complex problem of determining what stimulus to apply to the device's inputs to force the output to a known state. However, if the device incorporates boundary scan, data can be scanned into the boundary-scan register to set each I/O pin to a known level—without considering the internal functionality of the device under test. This obviously simplifies the test problem.

The XC4005 FPGA is the first of a family compatible with the IEEE boundary-scan standard. Each I/O pin of this device can be completely controlled and observed by using a mix of serial data passed into the boundary-scan register of the XC4005 through the Test Data Input (TDI) pin and control of the Test Mode Select (TMS) pin and Test Clock (TCK) by automatic test equipment (ATE) channels. This stands in contrast to the complexity of stimulating the inputs in order to achieve the same test coverage without boundary scan.

The second generation of printed wiring boards will consist of a mix of scannable and non-scannable devices. Options for testing the board increase with the advent of multiple scannable devices, in which boundary-scan capability allows the path between the two scannable devices to be tested without using a physical nail *(Fig. 2)*.

SILICON NAIL

For paths between scannable devices, designers can use test strategies that employ the concept of a silicon nail, in which designers check signals by capturing the signals in the boundary-scan registers and then shifting that data out the Test Data Output pin (TDO).

For most mixed technology boards, having physical access to some of the board's networks is the most critical factor in determining the economics of test methods. When deciding which networks will have physical access, a designer should have a particular test strategy in mind during board layout.

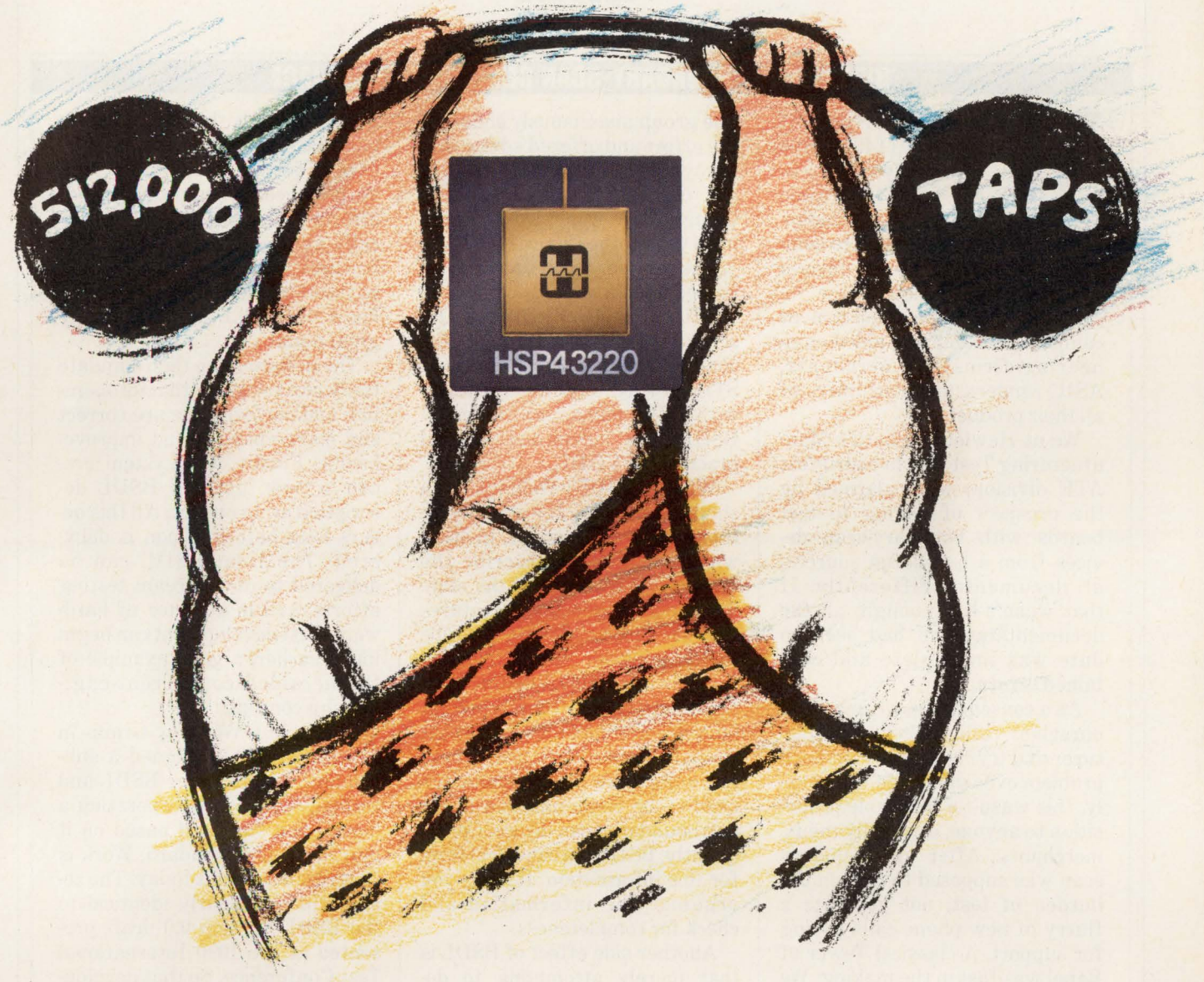
Circuit designers must therefore convey to the people doing board layout both a knowledge of the virtual access provided by silicon nails on the board and the access requirements imposed by the specific test strategy to be implemented.[3]

At present, a board consisting solely of scannable devices doesn't exist. In theory, such a board could be completely tested using only those signals that are present on the edge connector and silicon nails through the scan path.

Through the scan path, a tester can access individual device leads that serve as the silicon nails, providing the ability to control and observe those nodes in the circuit. These are nodes that would otherwise have been accessed by physical nails connected to ATE channels.

By using silicon nails, backdriving the I/O functions of devices on the board becomes unnecessary; the number of test channels is reduced; and the complexity and cost of fixtures for small, fragile test probes is virtually eliminated.

Generating test vectors for the board is also simplified. When



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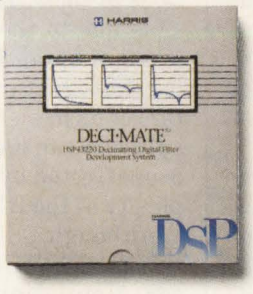

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CIRCLE 175

BOUNDARY-SCAN TESTING

BIRTH OF THE BOUNDARY-SCAN DESCRIPTION LANGUAGE

With the advent of IEEE 1149.1-1990 Boundary-Scan in February 1990 came the realization that many industry segments would need to communicate details about devices with boundary scan. These include automated test-equipment companies, computer-aided-engineering firms, IC merchants, ASIC vendors, and consumers of all their products.

We at Hewlett-Packard's Manufacturing Test Div. (a board-test ATE division) were alarmed by the prospect of having to test boards with boundary-scan devices from a half-dozen sources, all documented differently. If that wasn't bad enough, all the documentation we had seen to date was incomplete and contained errors.

As a consequence, we imagined ourselves calling each manufacturer and trying to weed out each problem over the phone. Obviously, this wasn't a favorable proposition to anyone, especially the IC merchants. After all, boundary scan was supposed to lighten the burden of test, not generate a flurry of new phone calls asking for support. A classical Tower of Babel was fast in the making. We knew we had to act.

In February 1990, HP proposed a first-cut straw man proposal for a description language: Boundary-Scan Description Language (BDL). The language at the time was in proprietary syntax. In the early going, the main concern was that it conveyed complete information. This proposal was circulated among a relatively small group of professionals deeply involved in the boundary-scan standard development. They offered plenty of feedback.

Based on this, we created a second draft in April 1990. This was circulated much more widely and presented formally to the 1149.1 Working Group in Amsterdam. The group unanimously endorsed the effort and offered advice that the syntax be cast into a subset of an existing language. The thought here was, "Do we really need yet another language?"

The answer was no, and we landed upon a suitable candidate, VHDL (VHSIC Hardware Description Language). VHDL, becoming commonplace, is IEEE STD 1076-1987. Upon consultation with VHDL management, we cast BSDL into a "subset and standard practice" of VHDL.

What is BSDL? Well, it's not a simulation model. It's actually orthogonal to 1149.1 itself. In other words, it doesn't describe the mandatory features of the standard, but rather those features that need parameters to describe them. Consider the instruction register in an 1149.1 device: How many bits does it contain? What op codes are implemented? What bit patterns do they use? These and quite a few other parameters need to be communicated about any boundary-scan device. Consequently, BSDL is a canonical form for this information. It helps you organize the information and check for completeness.

Another side effect of BSDL is that merely attempting to describe a boundary-scan device may illuminate a compliance problem. This is important especially in the early days of a standard when mistakes in interpretation may be easily committed.

Based on BSDL, it is possible to automatically develop tests for boundary-scan devices or collections of them. This process is possible due to the structure 1149.1 imposes on an IC design. Knowing this structure and the parameters of its implementation (BSDL) software can create tests. All this is unaffected by the internal complexity of the IC mission logic.

Although BSDL isn't a simulation model, VHDL is well suited for simulation, among other things. Thus, within a VHDL system, BSDL information can be used to derive simulation models. We have heard of some successful efforts to use BSDL to automatically synthesize boundary-scan features within a large ASIC, without a designer having to know the 1149.1 standard in any great detail.

The designer can then simulate the device to ensure that its operation and performance are correct and make changes and improvements. Finally, the system creates a new, updated BSDL description as an output. All this occurs long before silicon is delivered. The final BSDL can be delivered to downstream testing efforts well in advance of hardware. Test development can begin much earlier, a good example of the heralded concurrent-engineering concept.

The 1149.1 Working Group in September 1990 assigned a subcommittee to examine BSDL and formally propose incorporating a description standard based on it into the 1149.1 standard. Work is progressing on this today. The result will look nearly identical to the BSDL Version 0.0 draft presented at the 1990 International Test Conference. So that developers of boundary-scan tools can use BSDL as a front-end and prevent the language from splitting into a myriad of dialects, the computerized specifications of BSDL have been made public. They're free when you send your name/address/e-mail address to the following e-mail address:

bsdl%hpmtx@hplabs.HP.com

by Kenneth Parker

Kenneth Parker, a member of the technical staff at HP's Manufacturing Test Div., chairs the 1149.1 working group's BSDL subcommittee. He has an MS and PhD in electrical engineering from Stanford University.

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CIRCLE 106

BOUNDARY-SCAN TESTING

boundary scan is used, test programs can effectively ignore the complex functionality of a device and generate scan vectors that fully test the interconnection, solder integrity, and I/O structure of the device.

In addition, once the board's layout is defined, test development can proceed independently of the minor logical changes that inevitably happen in the debugging phases of a design.

Boundary scan isn't without limitations, however. On a board without physical access to ATE channels, very little can be determined without applying power to the board. Once power is applied, it may take a few seconds to determine if the scan path is functional.

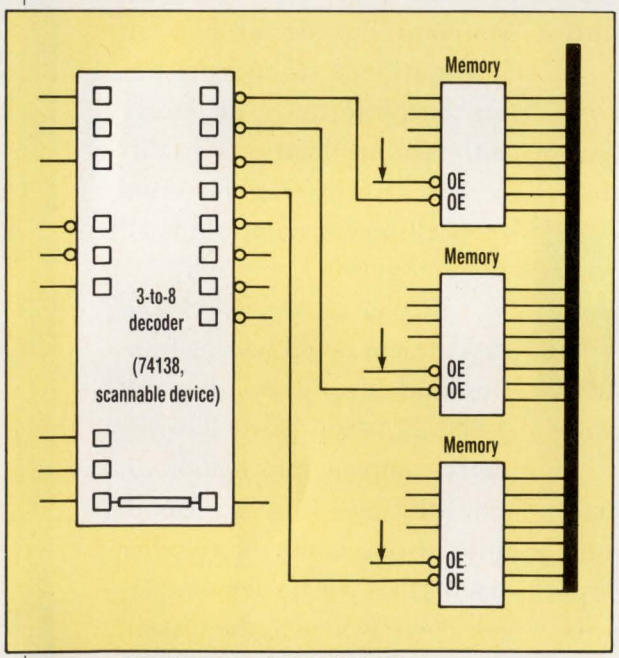
During this time, excessive current conditions could exist because of pins being shorted to power or ground. Assuming parts don't fail, the test engineer must decide if those parts can still be used in the system or if they have been overstressed and should be replaced.

If no catastrophic failures exist once power is applied, the first step is a port sanity check. In its simplest form, the port sanity check consists of clocking data through the boundary-scan path and verifying that data at the board-level Test Data Output (TDO). Because each device's scan register comes up in a reset state, an initial series of zeros of known length are to be expected at TDO.

If this doesn't happen, it indicates a problem with the scan path, and the board must be sent back for analysis and repair. Until the integrity of the boundary-scan path is verified, no other testing of the board can be accomplished. If the port has many problems, multiple passes across the test head may be required.

AVOIDING HAZARDS

Analog components are generally unsuitable for boundary scan, so their board networks would require physical access if analog in-circuit testing is desired. Although mixing scannable and non-scannable devices isn't a problem, special care must be taken to avoid hazards caused by certain features of boundary scan. One example is the case in which a bank of memory is selected by a standard 3-to-8 decoder *(Fig. 3)*.



3. IN MIXING SCANNABLE and non-scannable devices, engineers must be careful to avoid hazards caused by boundary scan. When a bank of memory is selected by a standard 3-to-8 decoder, just one output of the decoder can be asserted at a time. As a result, only one bank of memory is selected and driving the bus. If the decoder is a scannable device, any or all of the outputs may be set to the active state. This in turn directly causes bus contention on the memory's outputs.

In its normal operation, only one decoder output can be asserted at a time. Therefore, only one bank of memory is selected and driving the bus.

Now, let us consider the case in which the decoder is a scannable device: Any or all of the outputs may be set to the active state. This directly causes bus contention on the memory's outputs.

One of several solutions is to use scannable memory devices. These, however, are likely to be in scarce supply.

Yet another solution relies on the fact that most memories have both a Chip Select (CS) and an Output Enable (OE) signal. In many cases, these are tied together in the system.

Separating these two signals and using a physical nail to control one of the memory select signals could ensure that no two banks of memories are enabled at the same time.

Another possible problem in a mixed board is a short to a non-scannable device in the path between two scannable devices *(Fig. 4)*. If the output of the non-scannable device is stuck high or low, or worse yet, oscillating, the data received at TDO will be incorrect or indeterminate.

To the tester, this might indicate a problem with either of the scannable devices. The solution might be to place a physical nail on this signal to force it to a known state. In this case, at least the data received at TDO would be deterministic.

Certainly, many other potential pitfalls lie in mixing scannable and non-scannable devices and test methodologies—some have yet to be discovered. Given the choice, test houses will hold dearly to their existing in-circuit test methodology. Nevertheless, there may not be a choice in the near future.

SOFTWARE

Another limitation, though being addressed, is the availability of software packages to generate test vectors automatically for scannable devices. Various manufacturers were well on their way to defining proprietary device descriptions and software for vector generation.

To avoid the drawbacks of every vendor providing its own description and package, the IEEE assigned a subcommittee to examine a proposal that was submitted by Hewlett Packard called Boundary-Scan Description Language (BSDL) *(see "Birth of the Boundary-Scan Description Language," p. 78)*.

The IEEE Standard 1149.1 presents three alternatives for board-level interconnections conforming to

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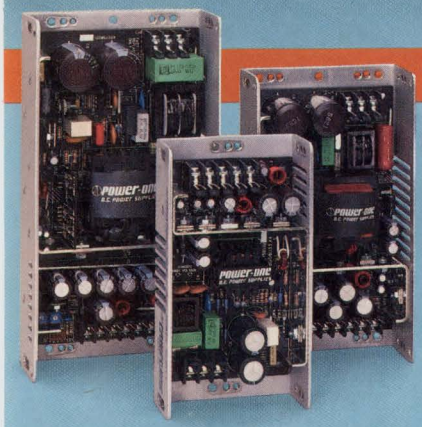

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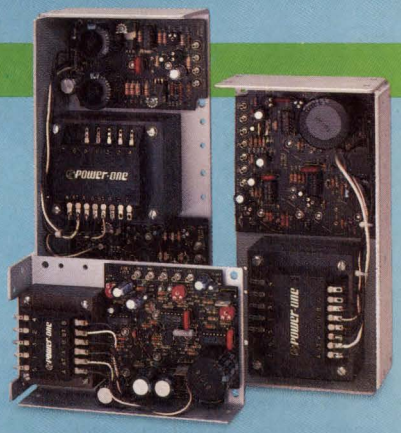

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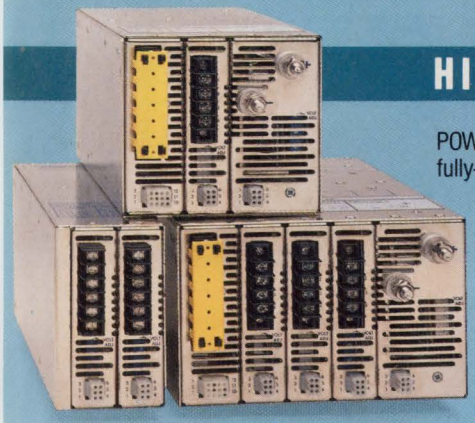

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CIRCLE 158

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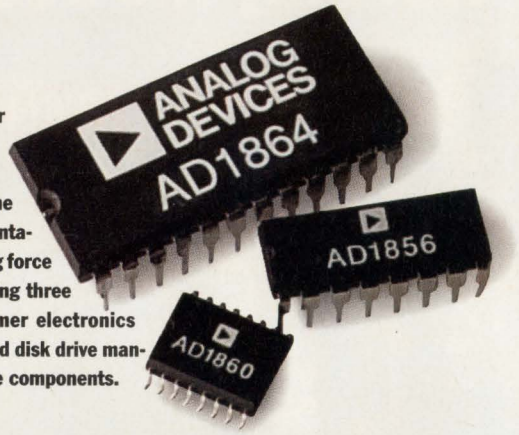

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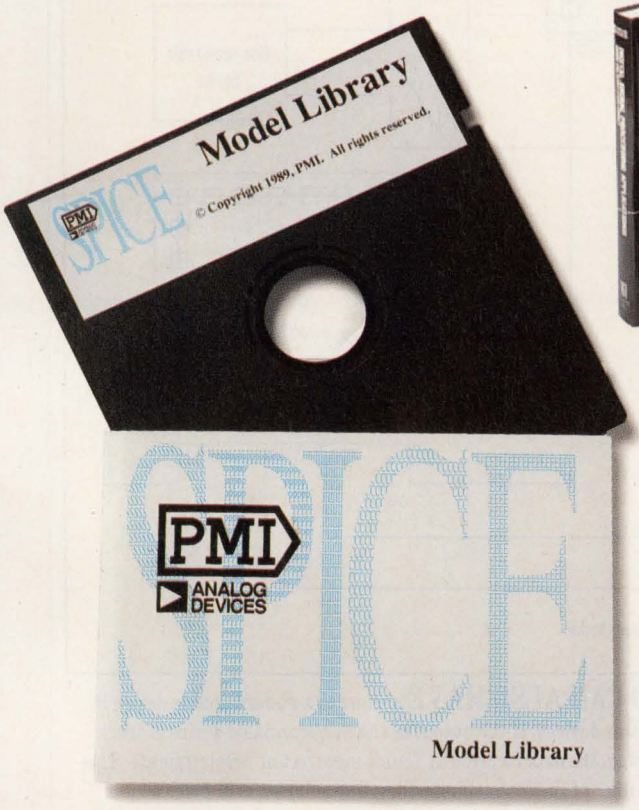

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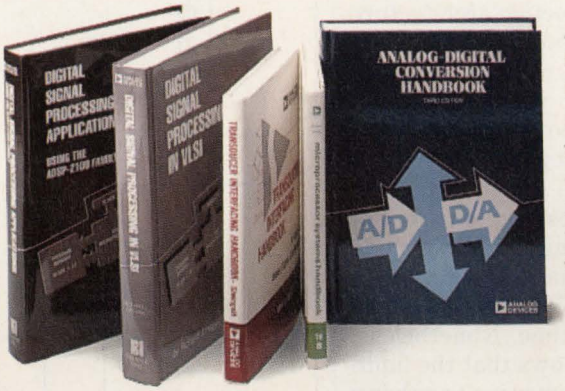

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CIRCLE 159

BOUNDARY-SCAN TESTING

the standard. These include a serial connection of scannable devices using one Test Mode Select (TMS) signal, connection of two parallel chains of scannable devices, or multiple independent paths with common TMS and Test Clock (TCK) signals.[4]

The prime consideration for choosing one interconnection architecture over another should be based on what your ATE software can support. Elaborate interconnection schemes not supported by software just add to the test problem.

Because of the serial nature of boundary-scan testing, one might think that breaking up a long chain consisting of perhaps 10,000 vectors to two paths with 5000 vectors would shorten the test time. Nonetheless, closer analysis shows that the limiting factor in test times isn't applying vectors, but the time required to download the tester disk.

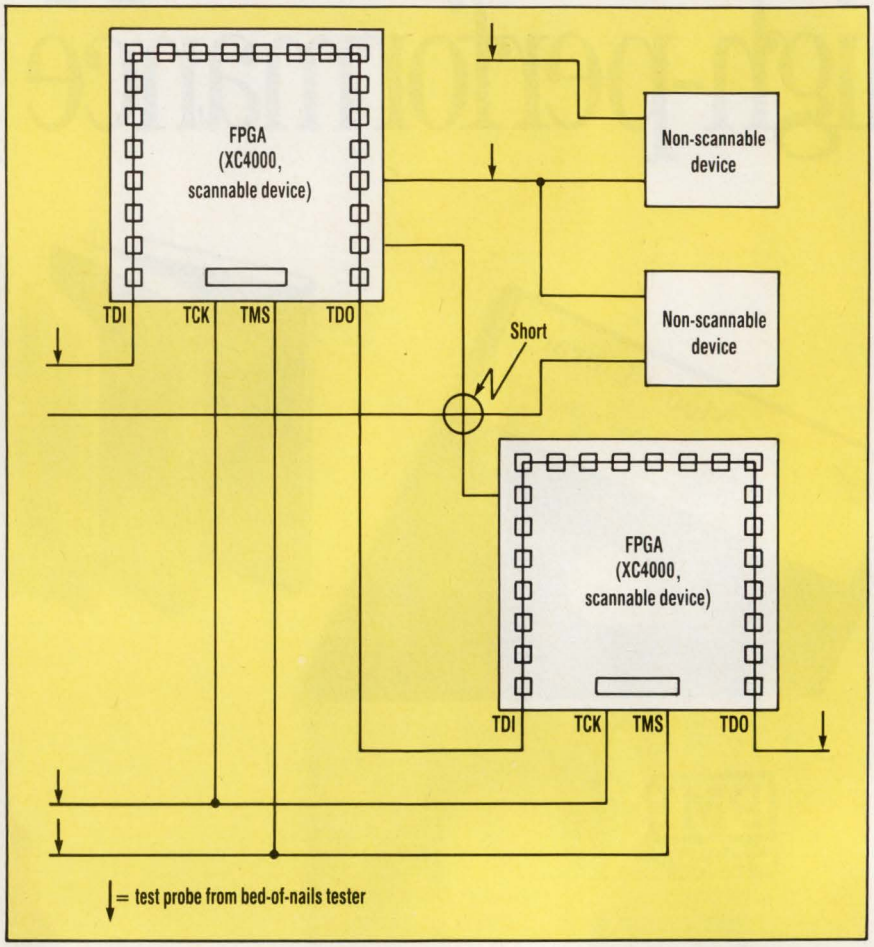
Take the example of clocking 10,000 vectors into a scan chain at a modest rate of 1 MHz. This takes only 10 ms, compared to the seconds it takes to download the test program. As a result, breaking the scan chain in half could actually double the test time.

PRACTICAL APPLICATIONS

Practical application of IEEE 1149.1 boundary scan will come with time. Solutions will start with one scannable device and gradually move to multiple devices, finally ending with a fully scannable board. Where possible, in-circuit test will still be used. Where in-circuit test isn't possible, the industry will overcome the limitations of boundary scan or simply accept those limitations. There may not be a choice.

ATE houses supporting boundary scan will start with the simplest forms of interconnection strategy, supporting those that generate the most requests. In time, one or two will emerge as the standard.

Today, boundary scan offers the only hope of continuing the miniaturization of electronic systems that dominated the 1980s, while enabling designers to maintain or improve quality. As boards and systems keep shrinking, customers continue to demand higher quality and lower cost. Improving testability is a big step toward achieving these goals. Boundary scan is that step.□



4. A MIXED BOARD CAN ALSO HAVE a short to a non-scannable device in the path between two scannable devices. If the output of the non-scannable device is stuck high or low, or if it's oscillating, the data received at TDO is incorrect or indeterminate. This could show a problem with either of the scannable devices. One solution is to place a physical nail on this signal to force it to a known state.

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[1]Peter Hansen, "Taking Advantage of Boundary-Scan in Loaded-Board Testing," *The Test Access Port and Boundary-Scan Architecture*, IEEE Computer Society Press, pp. 81–95.

[2]K. P. Parker, "The Impact of Boundary-Scan on Board Test," *IEEE Design And Test Of Computers*, August 1989, pp. 18–30.

[3]Hansen, p. 87.

[4]IEEE Standard 1149.1-1990, "IEEE Standard Test Access Port and Boundary-Scan Architecture," Institute of Electrical and Electronics Engineers Inc., 345 East 47th St., New York, NY 100017, pp. 3–7.

Acknowledgment:

Special thanks to Ken Parker for his insight into boundary-scan, BSDL, and test methodologies.

Jim Donnell, a field applications engineer at Xilinx, holds a BSEE from Purdue University, West Lafayette, Ind.

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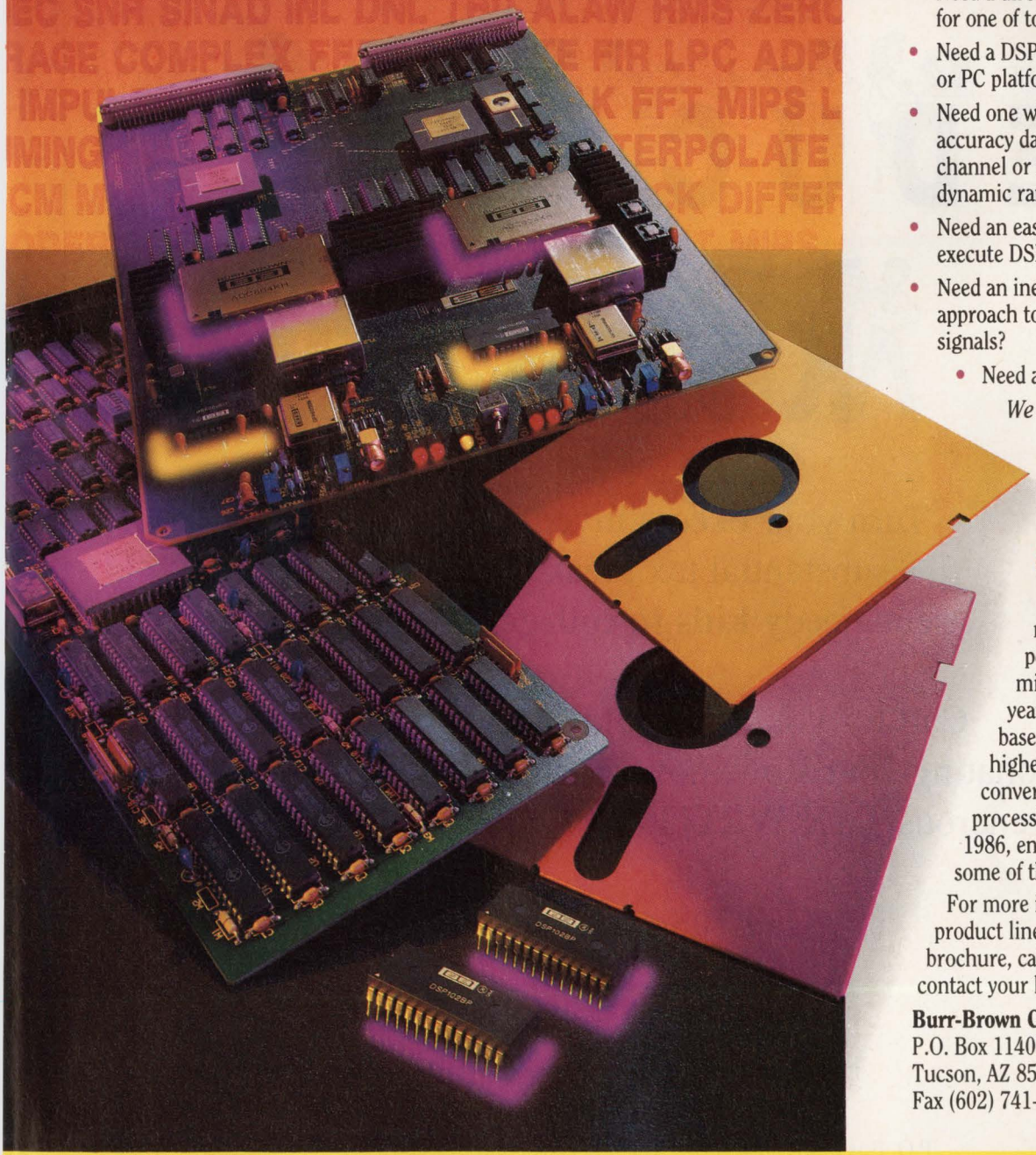

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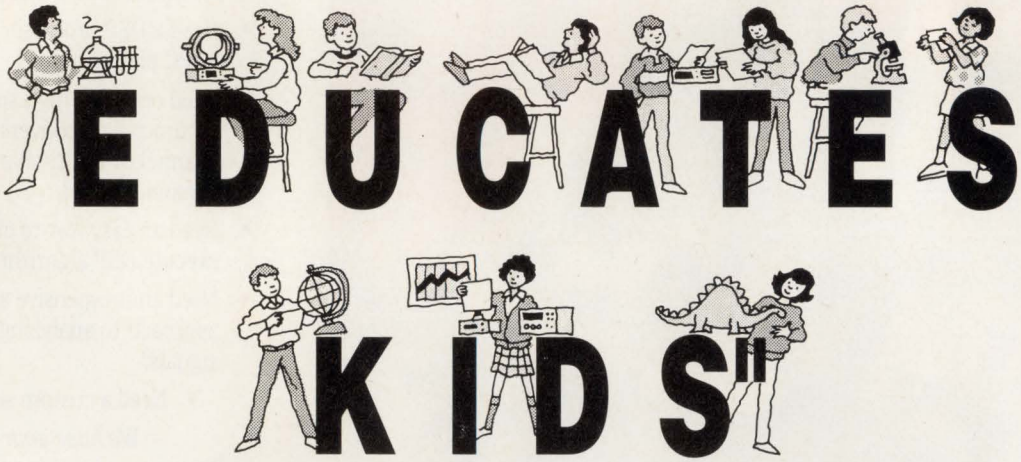

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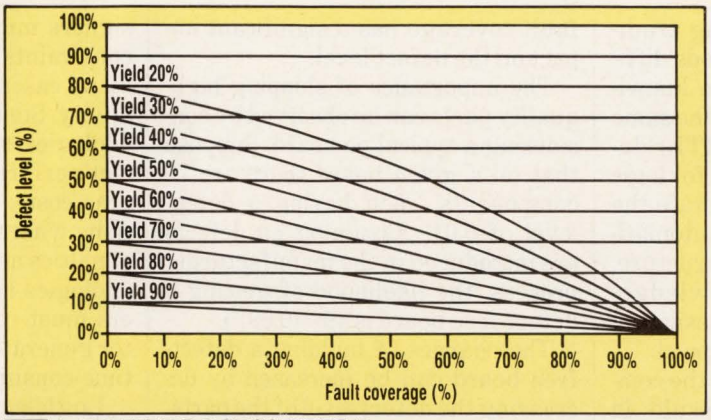

1. BOTH PROCESS YIELD and fault coverage affect the defect level of an IC. For example, the level of fault coverage has a significant impact on the defect level when the process yield is below 95%.

ATTAIN TESTABILITY WITH HIERARCHICAL DESIGN

GENERATE TEST VECTORS AUTOMATICALLY FOR SEQUENTIAL CIRCUITS DESCRIBED IN HARDWARE DESCRIPTION LANGUAGES.

Low process yields require that complex ASICs have test programs with high fault coverage. Unfortunately, conventional methods of automatic-test-pattern generation attempt to create test vectors by considering only the structural description. They don't work well for sequential circuits. On the other hand, manual test-vector generation becomes expensive and time consuming. Designers are thus forced to adopt some design-for-testability (DFT) method when high fault coverage is required. But DFT methods that assure high fault coverage add considerable overhead to chip area and circuit speed.

One promising alternative involves using a knowledge-based automatic-test-pattern-generation (ATPG) tool on sequential circuits. By writing a behavioral model in an HDL, like VHDL or Verilog, it's possible to automatically generate test vectors that provide high fault coverage for sequential circuits, including asynchronous circuits. Care must be taken, though, so that the models aren't written in a manner that will hinder the automatic-test-pattern-generation process. This method is particularly attractive for designers using logic synthesis for ASIC design. With logic synthesis, designers are unfamiliar with the syn-

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TESTABILITY THROUGH HIERARCHICAL DESIGN

thesized structure, making traditional test-generation methods difficult. However, because the knowledge-based ATPG tool uses the same register-transfer-level (RTL) description that was employed for logic synthesis, the tool can generate the test vectors efficiently and automatically for the synthesized structure. The advantage of a knowledge-based ATPG tool is that designers don't pay a price in area or speed.

As mentioned previously, the complexity of today's ASICs results in low process yields and hard-to-test devices. Consequently, test-pattern quality has a major impact on the quality of the shipped parts, especially if the process yield is much below 100%. The defect level (DL), defined as the percentage of bad parts that pass the test, can be calculated from the equation:

$$DL = 1 - Y^{(1-T)}$$

where Y is the manufacturing process yield and T is the test coverage.[1] The defect level can vary for different levels of process yields and fault coverage *(Fig. 1)*. For example, for process yields below 95%, the level of fault coverage has a significant impact on the defect level.

The importance of shipping high-quality parts can be observed by considering a typical pc board. Suppose that on a given board there are 70 components, each having a defect level of 0.01. Assuming no defects are introduced in the manufacturing process, the likelihood of getting a defect-free board is 49% (0.99^{70}).

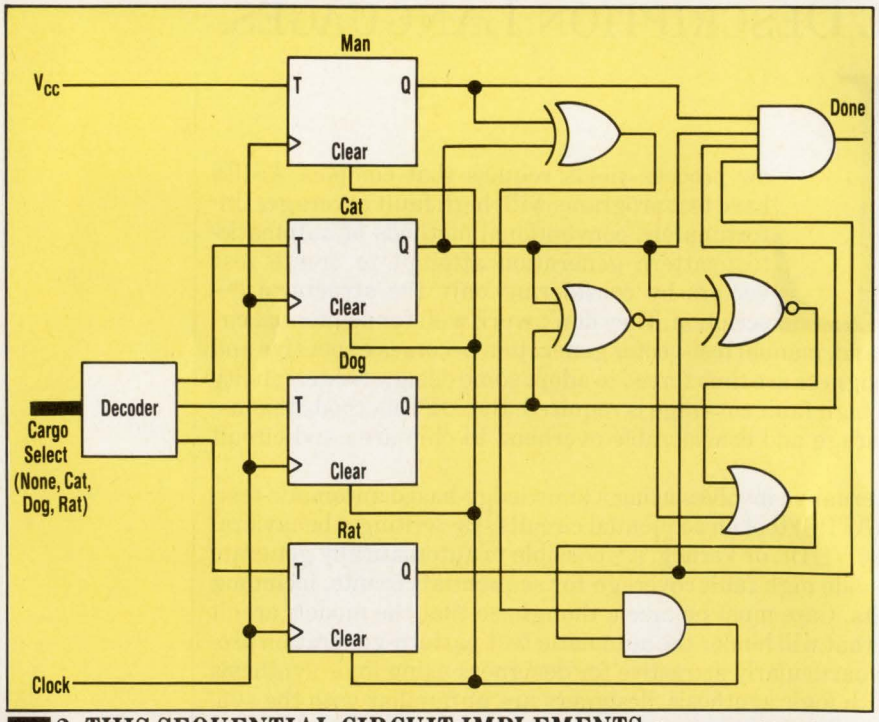
The chances of building a defect-free board can be increased by decreasing the defect level of the parts. Defect levels can be decreased by increasing the process yield or increasing the fault coverage of the test program. Because the submicron-ASIC manufacturing process is pushing the edge of technology, it's unrealistic to expect higher yields. It thus becomes necessary to have tests with high fault coverage to ensure high-quality products.

When it comes to getting high-quality test programs, ASIC designers have very few choices. Most of the conventional automatic-test-vector-generation tools don't work satisfactorily on sequential circuits. In order to use these tools, ASIC designers must put special testability constraints in the design, which in many cases restricts designers' creativity. Some of the testability methodologies, such as scan, degrade circuit performance and increase chip-area costs. There are many applications where the restrictions and the penalties associated with DFT methodologies are unacceptable. Designers must resort to manual test-vector generation, a very expensive and time-consuming process.

Logic-synthesis vendors offer testability solutions that automate some of the existing solutions, but still don't solve the problem of generating test programs for sequential circuits. The solutions offered by the logic-synthesis vendors fall in two different categories: functional-verification vectors and automatic scan insertion. In logic synthesis, the structure is generated automatically from high-level behavior descriptions, so it's relatively easy to also produce the vectors that verify the functionality of the generated structures. These vectors exercise the logic from a functional view. In a non-redundant combinatorial circuit, these functional vectors can provide very-high fault coverage. But in the case of sequential circuits, the fault coverage obtained from functional-verification vectors isn't high enough to be acceptable. Additional vectors that target specific faults have to be generated.

The other solution offered by the logic-synthesis vendors is the automatic insertion of scan cells. Scan-based DFT methods have been successfully used for a number of years. The selection and insertion of scan cells is usually a manual process that designers must consider during the design. There are stringent rules that they must follow for the particular scan methodology. The solution from the synthesis vendors alleviates this problem, and inserts the scan cells automatically without violating the scan design rules.

Scan-based DFT methodology solves the ATPG problem by turning the sequential circuit into a combinatorial one for test-generation purposes. However, it still doesn't solve



2. THIS SEQUENTIAL CIRCUIT IMPLEMENTS the state machine that models the classic puzzle of a man transporting a dog, a cat, and a rat across a river. The states of the animals and the man are represented by state variables held in flip-flops.

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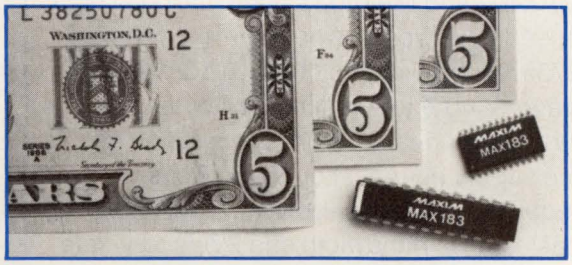

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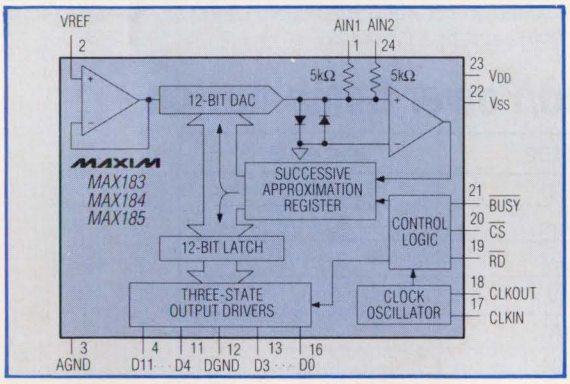

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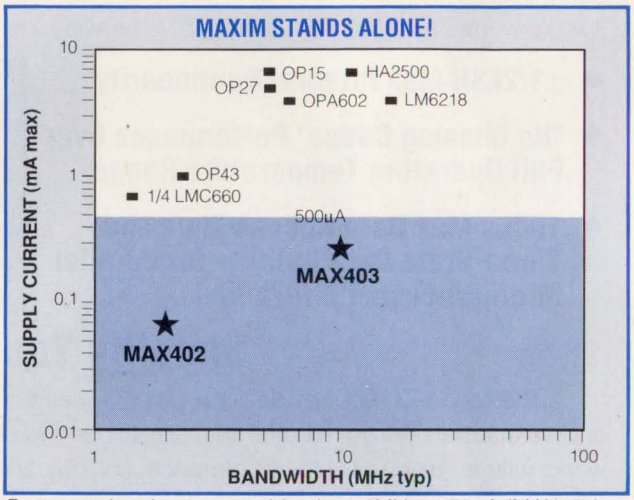

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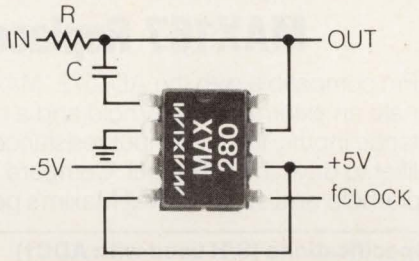

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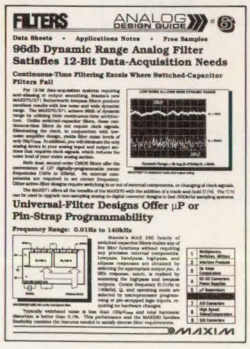
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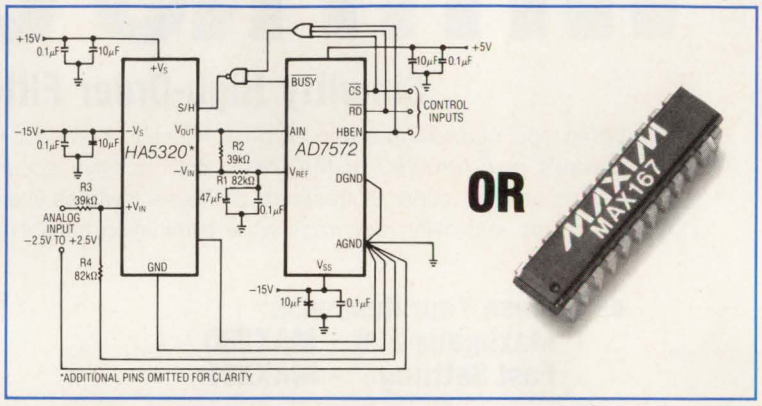

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Specifications (S/H used with ADC†)	MAX167	LF398A†	AD585†	HA-5320†	SHC803†
Hold Step + Offset (LSB max)	6	16	10	8	19
Full Power Bandwidth (MHz typ)	6	0.3	0.6	2	0.6
Acquisition Time (μs max)	1	6	3	1.5	0.35
Aperture Delay/Jitter (ns/ps typ)	25/50	150/?	35/500	25/300	15/50
Power Dissipation (mW typ)	104	270	375	465	835
Price Range**	**$20**	**$27**	**$35**	**$35**	**$140**

† S/Hs assumed to be used with AD7572KN05.
* Price 1,000-up, FOB USA.
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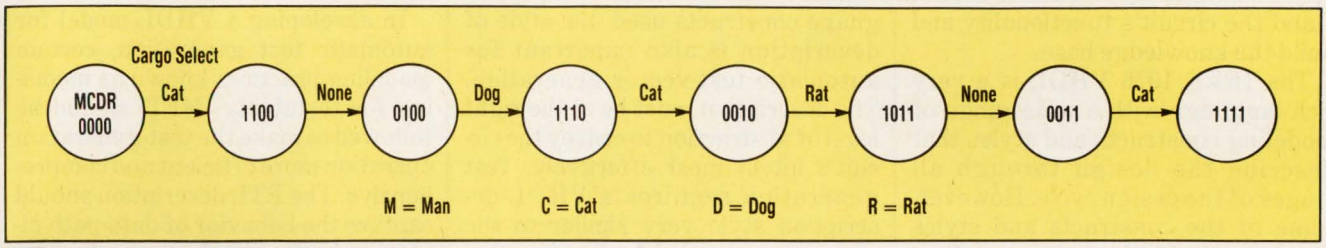


3. THE CORRECT SEQUENCE of state transitions will solve the puzzle. An incorrect sequence resets the circuit.

the test-generation problem for sequential circuits. Designs that can't use scan-based DFT methods due to its overhead can't benefit from the test solution offered by the logic-synthesis vendors.

If given enough time, an experienced test engineer can generate good tests for sequential circuits. Although this approach is expensive and time consuming, it's often the only option for producing high-quality test vectors. Test engineers don't approach the test problem from a structural view alone. Unlike conventional ATPG tools, test engineers understand the circuit's behavior and use this knowledge to create the test. They don't explore all of the combinations of the primary inputs, but know the effect of applying a certain sequence of vectors. Therefore, they can generate high-quality test vectors for sequential circuits. The test sequence can be generated because they understand the cause-and-effect relationships and know how to drive the circuit from one state to another.

The cause-effect relationship that test engineers use in generating the test isn't readily available from the structure description. However, this relationship can be described in a behavioral description written in an HDL. If the ATPG tool could use the behavioral description and comprehend the function of the circuit, it could also generate high-quality test patterns for sequential circuits.

Top-down hierarchical design effectively manages the design of complex ASICs. With the advent of logic synthesis, more ASIC designers are resorting to writing high-level behavior models instead of designing the chip at the gate level. Though logic synthesis facilitates the logic-design task, it further complicates the test-generation task. Because the structure is generated automatically, designers aren't familiar with it. Manually generating test vectors on an unfamiliar circuit isn't efficient or practical. Fortunately, the behavioral model used to generate the structure can produce the test vectors also. A knowledge-based ATPG tool can use the behavioral model to generate test vectors for the structure that's created by the synthesis tools.

The most common level of behavioral description used for logic synthesis is the register-transfer level. The register-transfer level can be thought of as an intermediate step between the high abstract level and the detailed structural level. It contains the detailed architecture description of the design with the control and data paths well defined.

At the RTL level, entire register contents are being manipulated. The contents may be transferred elsewhere, new contents may be loaded in, or logic and arithmetic operations may be performed on the contents of the registers. All of these activities are guided by signals that emanate from the control section.

During the behavioral-description stage of the design phase, designers are primarily concerned with logic functionality and may write the RTL description for efficient logic simulation. Such a model may not be the best for logic synthesis and test generation. By keeping the test-generation objective in mind, they can write the RTL description using the recommended modeling-for-testability (MFT) style. Then they can use the same RTL model for efficient test generation in addition to logic verification and logic synthesis.

The MFT guidelines describe the style of behavioral description that can be efficiently utilized by a knowledge-based ATPG tool, define the level of detail required, and define the language constructs that should be used to write the model. The MFT style for modeling is very similar to the style recommended for logic synthesis. Designers must keep in mind that the two main problems in test generation are controllability and observability. To employ the RTL description for test generation, they must explicitly describe the conditions for controllability and observability so that a knowledge-based ATPG program could make use of it.

To efficiently use such knowledge-based ATPG tools as the Test Design Expert (TDX) from ExperTest, design engineers must write the behavioral description so that all of the control conditions are explicitly described *(see "A knowledge-based ATPG tool," p. 96)*. For example, instead of embedding the control signals in Boolean equations, if-then-else or case statements must be employed. The basic idea is to communicate the intent of the design in an explicit manner, showing all cause-and-effect relationships. Because circuit designers know how to drive their circuit from one state to another, and can differentiate legal states from illegal ones, they should write the behavioral description so that these conditions are clearly described. The TDX can then use this information to generate the test vectors for sequential circuits in a manner very similar to that used by test engineers. TDX models faults at the gate level and the test vectors are generated for the structure, similar to the conventional methods. The behavioral description is primarily used to under-

TESTABILITY THROUGH HIERARCHICAL DESIGN

stand the circuit's functionality and build the knowledge base.

The IEEE 1076 VHDL is a very rich language with a wide range of modeling constructs and styles that describe the design through all stages of the design cycle. However, some of the constructs and styles aren't applicable for test generation, fault simulation, and logic synthesis. Logic-synthesis vendors have tried to overcome this problem in VHDL by defining a subset of VHDL that's targeted towards the logic-synthesis technology they have.

Similarly, ExperTest has defined VHDL-T, a subset of the IEEE 1076 VHDL specifically for test-generation purposes. In addition to the language constructs used, the style of description is also important for automatic test-vector generation. The description must be at the right level of abstraction to convey the circuit's intent most effectively. Test generation requires a VHDL-description style very similar to the style recommended for logic synthesis. The VHDL model should describe what the circuit does rather than how it's implemented. Designers should consider the controllability and observability problems in test generation and write the model in a style that distinctly identifies the cause-and-effect relationships between the data-flow elements and the control signals.

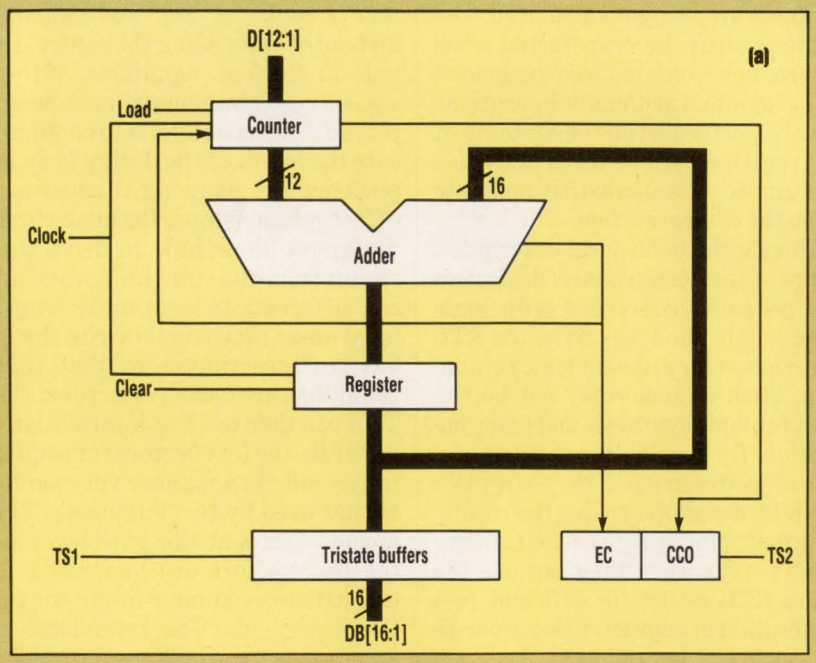
In developing a VHDL model for automatic test generation, certain modeling practices known as modeling for testability (MFT) should be followed to make the test-generation operation more efficient and comprehensive. The RTL description should capture the behavior of data-path elements in the simplest set of statements, while capturing all of the essential behavior of these elements. Essential behavior is defined as any behavior that causes an internal state change or a change in one or more of the output pins. Any essential behavior that results from input changes should be modeled. An effective behavior model for test generation is one that identifies register

A KNOWLEDGE-BASED ATPG TOOL

The Test Design Expert (TDX) from ExperTest is an automatic-test-pattern-generation system that operates on this premise: Successful test-program development for complex digital circuits requires knowledge of circuit behavior far beyond what can be extracted from the net list. The net list is still required, however, because it's the basis for creating the fault models that conform to the structure to be tested.

TDX analyzes the register-transfer-level description written in VHDL or Verilog HDL and builds a knowledge base for the controllability and observability conditions and other cause-effect relationships. This knowledge base is then used by TDX to generate tests for faults modeled at the structure level. Unlike a conventional ATPG, the TDX mimics the process used by the test engineer. In other words, it understands the circuit's behavior and uses this knowledge to generate test vectors. As a result, it can generate test vectors for complex sequential circuits.

With TDX, the structural and the behavioral descriptions are compiled into a knowledge base. A fault-list manager models the stuck-at faults on the structure and manages the fault list during the test-generation process. Users have complete control over the types of faults to be modeled. A fault simulator and a testability analyzer are used by the ATPG module during test generation.



A block diagram of a sequential circuit that poses some interesting situations for a test generation program will best show how TDX works *(Fig. a)*. The counter can be loaded, but no clear input exists. The register at the adder's output can be cleared, but known values must be clocked into the counter before clearing the register. Otherwise, the initial indeterminate values in the counter will simply be clocked back into the register, and initialization will fail. Once the circuit is initialized, the contents of the program counter and the register are summed and clocked back into the register. Only when there's a carry out from the adder can the counter actually perform a count operation. Howev-

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transfers and the control sequences. The model also identifies transformations on data as it passes from one register to another. Incidental glitches caused by races and hazards are ignored at this level. Some modeling practices that result in readable and efficient models are:

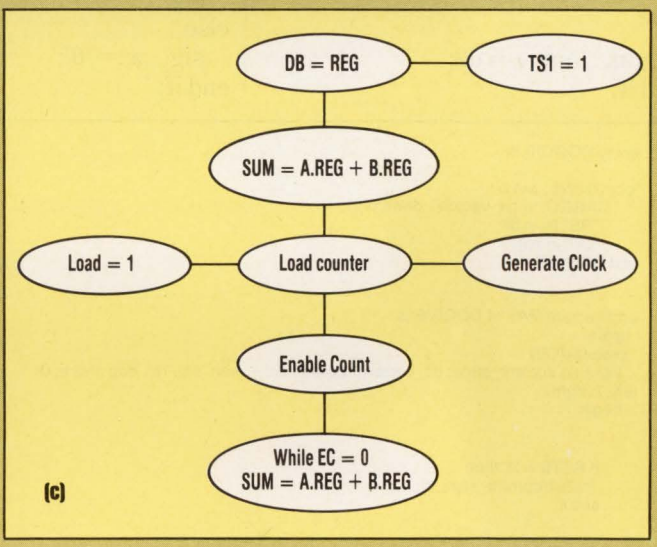
• Registers should be used where possible, emphasizing common clocking. However, flip-flops should not be grouped together into a register if there's no real commonality of purpose. When modeling an existing design from a schematic, one common tendency is to use the physical packaging to group the registers. Though this reflects the physical packaging, it confuses the ATPG tool into thinking that these flip-flops are functionally related. For example, the 74174 package contains six D-flip-flops. If four of them are used as 4-bit counters and the other two are being used for totally different purposes, then the four counter flip-flops should be declared as one 4-bit register and the other two should be declared separately. All six of them should not be grouped together into one register if they're being used for unrelated tasks.

• Temporary variables shouldn't be used to represent more than one point in the logic. It's a common practice in programming to use temporary variables to hold intermediate results. However, the same temporary variable should not be used to hold the value of more than one signal. For, example if a variable X1 is associated with the result of an AND operation of two signals, S1 and S2, then X1 should not be used later to hold the result of another operation.

• The operators and functions available in the language should be used to perform arithmetic and logical operations in a simple, concise manner. VHDL-T has defined special functions for performing certain common operations, such as increment, decrement, shift, and rotate. These functions are recognized by the

(b)

```
entity example is
        port(CLR, CK:      in logic_state;
       D:          in logic_vector(0 to 11);
       LD:         in logic_state;
       TS1, TS2:      in logic_state;
       DB :        out logic_vector(0 to 15);
       DEC, DCC:      out logic_state;
       GND, VCC:      in logic_state);
end example;

architecture behavior of example is
use std_library.all;
begin
   process (CLR, CK, D, TS1, TS2)

   variable A_REG: logic_vector (0 to 11) := (0 to 11 => '0');
   variable B_REG: logic_vector (0 to 15) := (0 to 5 => '0',others => '0');
   variable EC,CCO:logic_state  := '0';
   variable SUM:  logic_vector (0 to 15);
   begin
      if (CLR = '0') then int2bit(B_REG,0);
     end if;

     if (UP_EDGE(CK))
      then int2bit(sum, bit2int(A_REG) + bit2int(B_REG(0 to 15)));

        if not (CLR = '0')
         then if (bit2int(SUM)> 65535)
           then EC := '1';
           else EC := '0';
           end if;

            if ((bit2int(A_REG) = 4095) and (EC = '1'))
           then CCO := '1';
           else CCO := '0';
           end if;

              int2bit(B_REG(0 to 15),bit2int(SUM) mod 65536);
       end if;

       if (LD = '0')
        then A_REG := D;
          CCO := '0';
        elsif (EC = '1')
         then int2bit(A_REG,bit2int(A_REG)+1);
           if (bit2int(A_REG) > 4095)
           then int2bit(A_REG,0);
           end if;
       end if;
     end if;

     if (TS1 = '0')
      then DB  <= B_REG  after 20 ns;
     end if;
        end process;
end behavior;
```



er, because the adder and register are 16 bits wide and the counter is only 12 bits wide, a carry out may require many consecutive add operations.

This level of functional information isn't readily available from a gate-level implementation of the circuit. However, it can be easily derived from a VHDL-T description *(Fig. b)*. The TDX analyzes this description and builds goal trees that clearly define the sequence and conditions for events to happen in order to meet the objectives *(Fig. c)*. The flow of the goal tree is bottom-up, which means the leaf nodes are the first events that must occur and the top-level node or the root node is the last event to occur to meet the desired objective. By analyzing the VHDL-T descriptions and building a knowledge base that contains circuit specific information, such as the goal tree, TDX can successfully generate the test vectors that provide 100% fault coverage for the circuit.

TESTABILITY THROUGH HIERARCHICAL DESIGN

ATPG software and are included in the VHDL-T package.

• Control signals should be clearly identified and shouldn't be mixed with the data signals. For example, a 2-to-1 multiplexer should be expressed via if-then-else constructs instead of using a Boolean equation. It's perfectly legal to describe the behavior of the multiplexer for such simulation purposes as:

```
mux_out <= (d1 AND (NOT sel) )
  OR (d2 AND sel);
```

But in this description, the differentiation between the data signal and the control signal is lost. A much better description for test generation is:

```
if (sel = '0') then
  mux_out <= d1;
else
  mux_out <= d2;
end if;
```

In this description, the control signal is clearly distinguished from the data signal, which helps the ATPG software manipulate the right signals.

• Another example of implicit control that isn't good for an ATPG tool is a description, such as:

```
sig_a := '0';
if (flag = '1') then
  sig_a := '1';
end if;
```

This description has an implicit control, which is that "sig_a" gets 0 when "flag" is 0. The ATPG software will interpret this description as if "sig_a" is always 0 regardless of the state of "flag." The above description should be written as:

```
if (flag = '1') then
  sig_a := '1';
else
  sig_a := '0';
end if;
```

This way, the condition is explicit as to when "sig_a" is 1 and when it is 0.

• Do not specify a control when there isn't any. For example:

```
if (flag = '1') then
  out1 := '1';
  out2 := '1';
else
  out1 := '0';
  out2 := '1';
end if;
```

In the above description, there is no control necessary for "out2" because it gets the same value regardless of the state of "flag." Thus, "out2" should not be assigned inside the if-block.

• Do not specify the union of complementary events in a conditional statement. For example, the conditional statement:

```
if (Rising(clk) OR Falling(clk)) then
```

```
entity DOGGIE is

 port(DONE: out bit;
    CARGO: in bit_vector(1 downto 0);
      RSTB: in bit;
      CP: in bit);
end DOGGIE;


architecture RAT of DOGGIE is
 begin
  process(CP)
   variable current_state: bit_vector(3 downto 0); -- man, cat, rat, dog shore; 0:
left, 1: right.
   begin


      if RSTB = '0' then
       int2bit(current_state,0);
      end if;


    if up_edge(CP) then
     case bit2int(current_state) is
      when 0 => -- all on left shore.
       if (bit2int(cargo)=1) then int2bit(current_state, 12); -- man and cat go to right.
        elsif (bit2int(cargo)=3) then int2bit(current_state, 10); -- man and rat.
        elsif (bit2int(cargo)=2) then int2bit(current_state, 9); -- man and dog.
       end if;
       done <= '0';
      when 1 => -- dog on right.
       if (bit2int(cargo)=1) then int2bit(current_state, 13); -- man, cat, and dog.
        elsif (bit2int(cargo)=3) then int2bit(current_state, 11); -- man, rat and dog.
        elsif (bit2int(cargo)=0) then int2bit(current_state, 9); -- man and dog.
       end if;
       done <= '0';
      when 2 => -- rat on right.
       if (bit2int(cargo)=1) then int2bit(current_state, 14); -- man, cat and rat.
        elsif (bit2int(cargo)=2) then int2bit(current_state, 11); -- man, dog, and rat.
        elsif (bit2int(cargo)=0) then int2bit(current_state, 10); -- man and rat.
       end if;
       done <= '0';
      when 3 => -- dog and rat on right.
       if (bit2int(cargo)=1) then    int2bit(current_state, 15); -- all of em.
        elsif (bit2int(cargo)=0) then int2bit(current_state, 11); -- man, rat and dog.
       end if;
       done <= '0';
      when 4 => -- cat on right.
       if (bit2int(cargo)=3) then int2bit(current_state, 14); -- man rat cat.
        elsif (bit2int(cargo)=2) then int2bit(current_state, 13); -- man dog cat.
        elsif (bit2int(cargo)=0) then int2bit(current_state, 12); -- man cat.
       end if;
       done <= '0';
      when 5 => -- cat and dog on right.
       int2bit(current_state, 0);  done <= '0';
      when 6 => -- cat and rat on right.
       int2bit(current_state, 0);  done <= '0';
      when 7 => -- cat, dog, and rat on right.
       int2bit(current_state, 0);  done <= '0';
      when 8 => -- man on right.
       int2bit(current_state, 0);  done <= '0';
      when 9 => -- man and dog on right.
       int2bit(current_state, 0);  done <= '0';
      when 10 => -- man and rat on  right.
       int2bit(current_state, 0);  done <= '0';
      when 11 => -- man, dog, and rat on right.
       if (bit2int(cargo)=3) then int2bit(current_state, 1); -- only dog left on right.
       elsif (bit2int(cargo)=2) then int2bit(current_state, 2); -- only rat left on right.
       elsif (bit2int(cargo)=0) then int2bit(current_state, 3);
       end if;
       done <= '0';
      when 12 => -- man and cat on right.
       if (bit2int(cargo)=1) then int2bit(current_state,0);
       elsif (bit2int(cargo)=0) then int2bit(current_state,4);
       end if;
       done <= '0';
      when 13 => -- man, cat, and dog on right.
       if (bit2int(cargo)=1) then int2bit(current_state, 1);
       elsif (bit2int(cargo)=2) then int2bit(current_state, 4);
       elsif (bit2int(cargo)=0) then int2bit(current_state, 5);
       end if;
       done <= '0';
      when 14 => -- man, cat, and rat on right.
       if (bit2int(cargo)=1) then int2bit(current_state, 2);
       elsif (bit2int(cargo)=3) then int2bit(current_state, 4);
       elsif (bit2int(cargo)=0) then int2bit(cargo, 6);
       end if;
       done <= '0';
      when 15 => -- all on right! done! hooray!
       done <= '1';
     end case;
    end if; -- up_edge CP.
  end process; -- simulation of problem.
end RAT;
```

4. VHDL DESCRIBES the state-machine transitions at the register-transfer level. When the model is written in this fashion, the TDX ATPG tool can create a test for the circuit.

TESTABILITY THROUGH HIERARCHICAL DESIGN

will evaluate to true every time "clk" changes state from high to low or from low to high. A better way to describe this condition is by using a Process statement with the signal "clk" in its sensitivity list:

```
Process (clk)
```

Another way to express the same condition is to use the Wait statement:

```
Wait on clk;
```

• Attributes such as 'event or 'stable should not be used. These are artifacts of simulation and an ATPG tool usually can't respond to these Attributes. Instead, predefined functions that are supplied in the package must be used. For example, the statement:

```
if (clk'event AND clk = '1') then
```

should be replaced with:

```
if (Rising(clk)) then
```

• Do not use non-events as conditions in a conditional statement. For example, the statement:

```
if (NOT (Rising(clk))) then
```

though legal for simulation, doesn't specify an actual event. The ATPG tool can't create an event that's not the "rising of the clk." Furthermore, real hardware doesn't respond to the absence of an event.

• Timing shouldn't be used to sequence the events. It should be used in a case where if it's ignored, only the timing of the signal change is affected—the behavior would remain unaffected. The following is one example of a bad model for the ATPG tool:

```
Process
  begin
  if (Rising(enbl)) then
    data_out := 1;
    wait for hi_delay;
    data_out := 0;
  end if;
end process;
```

The above description is a model for a one-shot timer. It uses the delay value to sequence the pulse from one to zero. A much better procedure for the ATPG tool is to describe the behavior as follows:

```
Process (enbl, data_out)
  begin
  if (Rising(enbl)) then
    data_out <= '1';
  end if;
  if (data_out = '1') then
    data_out <= '0'
        after hi_delay;
  end if;
end process;
```

• The sensitivity lists for the Process statements should be carefully selected. Many designs respond to only a few signals, such as clock, clear, and reset signal. For these designs, all of the signals need not be included in the sensitivity list.

• State machines are effectively described via a CASE statement or an if-then-else statement. For an incompletely specified state machine (ISSM), the unassigned states shouldn't be included in the CASE statement.

To understand the complexity of test generation for a highly sequential circuit and how modeling for testability can help, consider the classic puzzle about a man, a dog, a cat, and a rat. The man wants to take the animals across a river in a canoe that can only accommodate one animal per trip. The dog and the cat don't get along, and the cat isn't very friendly with the rat either. Thus, the man can't leave the dog and the cat alone, and can't leave the cat and the rat alone. How can the man get all of the animals across the river?

The puzzle can be modeled as a state machine. The state of each animal, including the man, is represented by a state variable. A 0 for the state variable means that the animal is on the left shore of the river, and state 1 means that the animal is on the right shore. The initial state is (0,0,0,0), which means that everyone is on left shore. In the target state of (1,1,1,1) all are on the right shore.

A circuit can implement this state machine *(Fig. 2)*. When the circuit reaches state (1,1,1,1), the flag "DONE" is set to 1. The circuit is designed so that it resets if there's a conflict (if the cat is left alone with the dog or if the cat is left alone with the rat). To generate a test for "DONE" stuck-at-0, the ATPG software has to drive "DONE" to 1, which means that the ATPG software has to solve the puzzle correctly. It must know the illegal states so that it doesn't enter them. Otherwise, the engine will be reset.

The correct sequence of state transitions will solve the puzzle *(Fig. 3)*. An RTL-level VHDL model describes the state-machine transitions *(Fig. 4)*. TDX analyzes this description and builds a knowledge base that identifies the state transitions and the cause-effect relationship. Armed with this knowledge, TDX can determine the correct state transitions, solve the puzzle, and generate the test for "DONE" stuck-at-0.

A conventional ATPG tool working only at the gate level of the state-machine circuit doesn't know the circuit's functionality. For "DONE" stuck-at-0 test, its objective would be to drive "DONE" to 1 and work its way back from "DONE," one gate at a time, along the different paths. At every intermediate gate, it would set new objectives without knowing if it's entering the illegal state. Because the probability of hitting the right solution is very low, a conventional ATPG tool would have a very hard time finding a test for "DONE" stuck-at-0.□

Reference:

[1]T.W. Williams and N.C. Brown, "Defect Level as a Function of Fault Coverage," IEEE Transaction on Computers, Vol. C-30, No. 12, Dec. 1981.

Ghulam Nurie, the director of product marketing at ExperTest, receieved a BSEE and an MSEE from the University of Wisconsin, Madison.

HOW VALUABLE?	CIRCLE
HIGHLY	532
MODERATELY	533
SLIGHTLY	534

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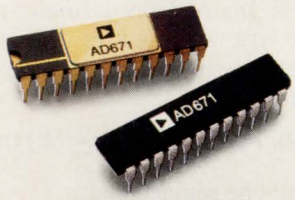

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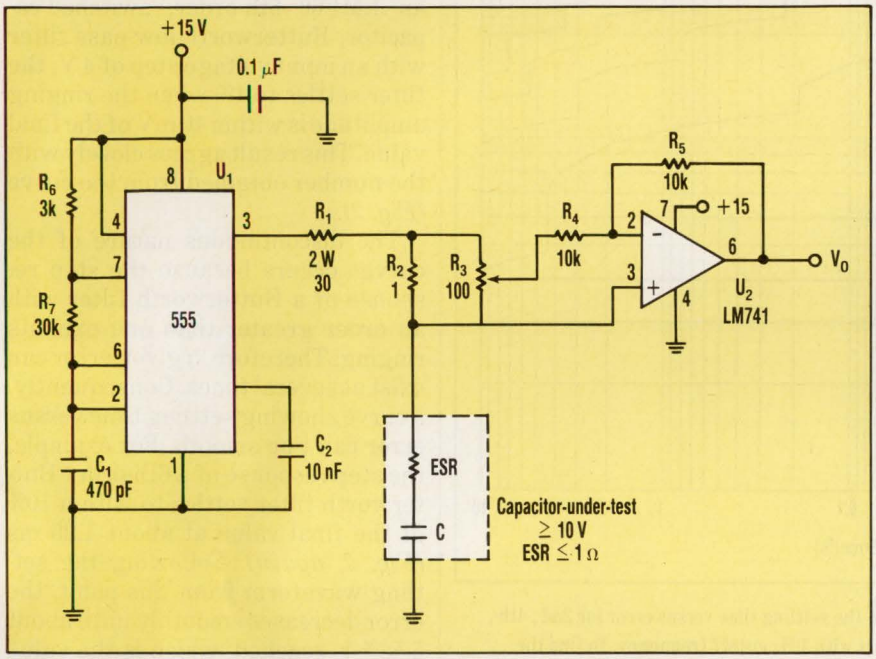
CIRCLE 81

CIRCLE 521

MEASURE ESR OF A CAPACITOR

CARL SPEAROW
Sundstrand Corp., 4747 Harrison Ave., Rockford, IL 61125; (815) 394-3263.



USING THIS CIRCUIT AND AN AC VOLTMETER, the equivalent series resistance of a capacitor can be measured. Adjust resistor R_3 until the output voltage is minimized. Multiply the value of the potentiometer by the value of resistor R_2. Then, that product is the ESR.

The equivalent series resistance (ESR) of a capacitor can be measured using this circuit and an ac voltmeter *(see the figure)*. U_1 functions as a 50-kHz square-wave generator. It drives a current waveform of about ±180 mA in the capacitor-under-test through R_1 and R_2. When R_3 is adjusted to the proper value, the voltage drop across the equivalent series resistor is precisely nulled by the inverting amplifier (U_2). Thus, V_O is the pure capacitor voltage which is the minimum voltage that can be produced at V_O.

To make an ac voltage measurement, adjust R_3 until V_O is minimized. Then note the position of the potentiometer and multiply it by the value of R_2, 1 Ω in this case. That product equals the capacitor's ESR. The capacitor is biased at about 7.5 V. Lower-voltage capacitors won't work with this circuit. By changing the value of R_2, other ranges of ESR can be measured. However, for small R_2 values, the current level should be increased to keep a reasonable voltage across R_2. This will require some sort of buffer. The circuit is intended for capacitors greater than 100 μF. The ripple voltage gets large for smaller values and accuracy decreases.□

IFD WINNER

IFD Winner for January 31, 1991

Jim Williams, Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 954-8400. His idea: *"Drive 100-mA Cable Loads."*

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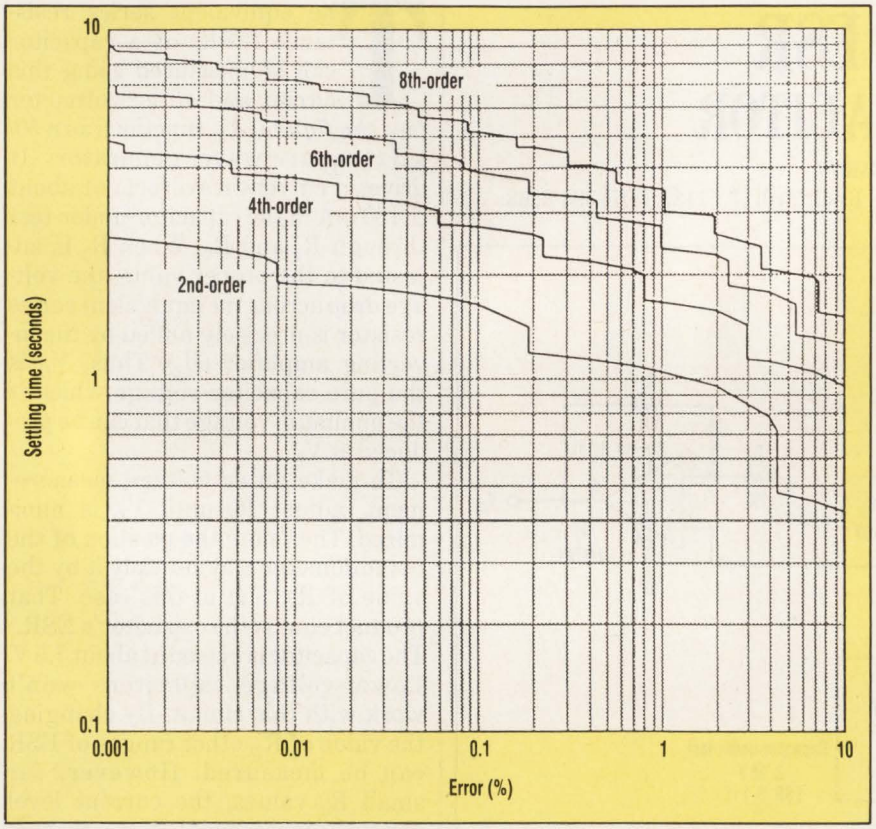
CIRCLE 522

FIND FILTER SETTLING TIME WITH EASE

KERRY LACANETTE
National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-5000.

Anytime a filter is added to a system, its presence affects the system's transient response. This occurs whether it prevents aliasing in an analog-to-digital converter or reduces out-of-band noise at the front-end of an instrument. The filter's settling time depends on its order, its cutoff frequency, and the desired accuracy. Settling time is the time required for output to equal the input within a specified accuracy when the circuit is driven by a step input signal. Determining the settling time of an arbitrary filter analytically is tedious and is usually avoided by the prudent engineer.

The curves shown offer a quick way to find the settling time of a Butterworth low-pass filter with minimal calculation *(Fig. 1)*. The percentage error to which the filter must settle is on the horizontal axis. The vertical axis shows the settling time for a low-pass filter with a 1-Hz cutoff (–3 dB) frequency. For filters with cutoff frequencies other than 1 Hz, sim-



1. THESE CURVES REPRESENT the settling time versus error for 2nd-, 4th-, 6th-, and 8th-order Butterworth low-pass filters with 1-Hz cutoff frequency. To find the settling time of a filter with a different cutoff frequency, divide the settling time obtained from the curve by the filter's cutoff frequency.

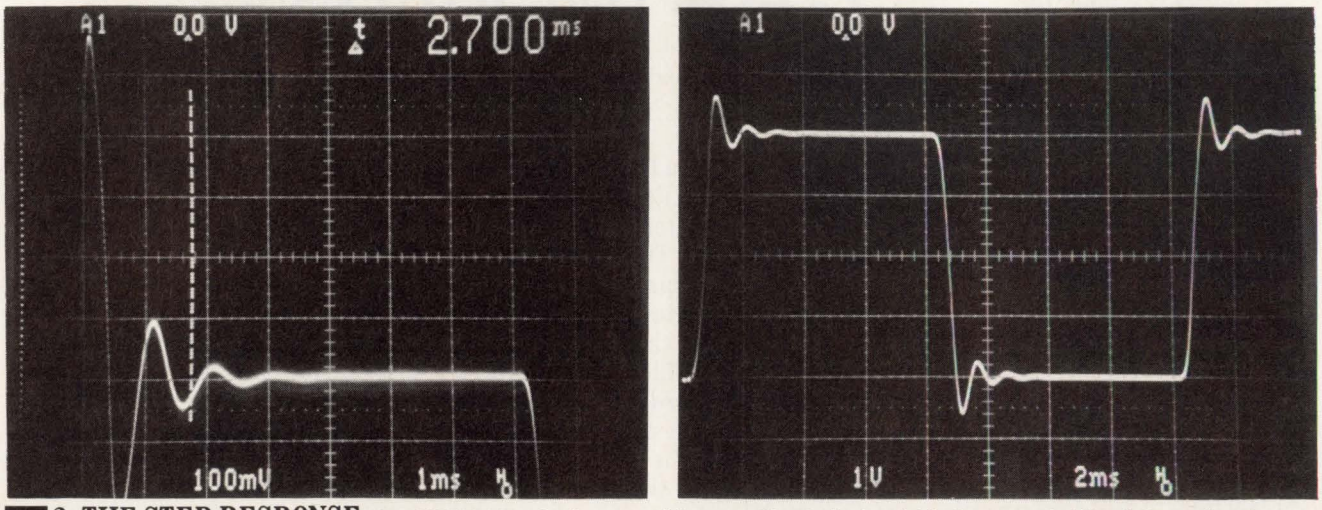
ply divide the settling time obtained from the curve by the filter's cutoff frequency:

$t_S = t_{S1}/f_C$

where t_S represents the filter's settling time, f_C is the value of its cutoff frequency, and t_{S1} is the settling time of a 1-Hz filter as obtained from the curve.

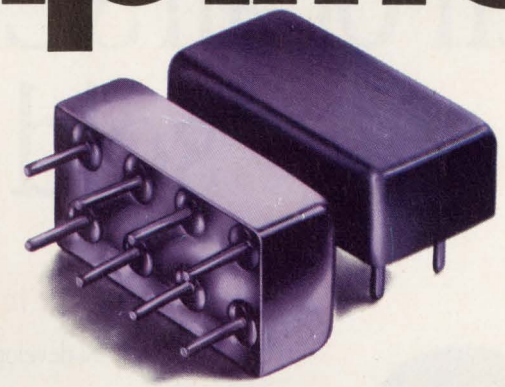
For example, if the settling time to 1% error of a 1-kHz, 6th-order, Butterworth low-pass filter is needed, use the 6th-order curve. The 1% settling time of a 1-Hz filter is $t_{S1} = 2.7$ seconds. Dividing this result by 1000 (the value of f_C) gives the settling time for the 1-kHz filter—2.7 ms. For an LMF60 6th-order, switched-capacitor, Butterworth low-pass filter with an input voltage step of 4 V, the filter settles to 1% when the ringing amplitude is within 40 mV of the final value. This result agrees closely with the number obtained from the curve *(Fig. 2)*.

The discontinuous nature of the curves occurs because the step response of a Butterworth filter with an order greater than one exhibits ringing. Therefore, a given error can exist at several times. Consequently, a curve showing settling time versus error can't be smooth. For example, the step response of a 6th-order Butterworth filter settles to within 10% of the final value at about 1.26 ms *(Fig. 2, again)*. Following the settling waveform from this point, the error decreases smoothly until about 5.52% is reached, which is the value of the error at the step response's first negative-going peak. The settling time then "jumps" from 1.34 to 1.64 ms for an error of 5.52%. Each peak or dip in the step response contributes an additional discontinuity in the settling-time-versus-error curve.□



2. THE STEP RESPONSE of an LMF60 6th-order Butterworth low-pass filter is displayed. The input step is 4 V and the settling time to 1% (40 mV) is about 2.7 ms as predicted by the curve.

rugged plug-in amplifiers



0.5 to 1000MHz from $13.95 (10 to 24 qty)

Tough enough to meet full MIL-specs, capable of operating over a wide -55° to +100°C temperature range, in a rugged package…that's Mini-Circuits' new MAN-amplifier series. The MAN-amplifier's tiny package (only 0.4 by 0.8 by 0.25 in.) requires about the same pc board area as a TO-8 and can take tougher punishment with leads that won't break off. Models are unconditionally stable and available covering frequency ranges 0.5 to 1000MHz, NF as low as 2.8dB, and power output as high as +15dBm. Prices start at only $13.95, *including* screening, thermal shock -55°C to +100C, fine and gross leak, and burn-in for 96 hours at 100°C under normal operating voltage and current.

Internally the MAN amplifiers consist of two stages, including coupling capacitors. A designer's delight, with all components self-contained. Just connect to a dc supply voltage and you are ready to go.

The new MAN-amplifiers series… another Mini-Circuits' price/performance breakthrough.

MODEL	FREQ. RANGE (MHz) f_L to f_u	GAIN dB min	GAIN dB flatness††	MAX. OUT/PWR† dBm	NF dB (typ)	DC PWR 12V, mA	PRICE $ ea. (10-24)
MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
*MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_{u/2}$, ±0.5dB †1dB Gain Compression ◇Case Height 0.3 In.

Max input power (no damage) +15dBm; VSWR in/out 1.8:1 max.

*Active Directivity (difference between reverse and forward gain) 30 dB typ.

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CIRCLE 123

C118 REV. E

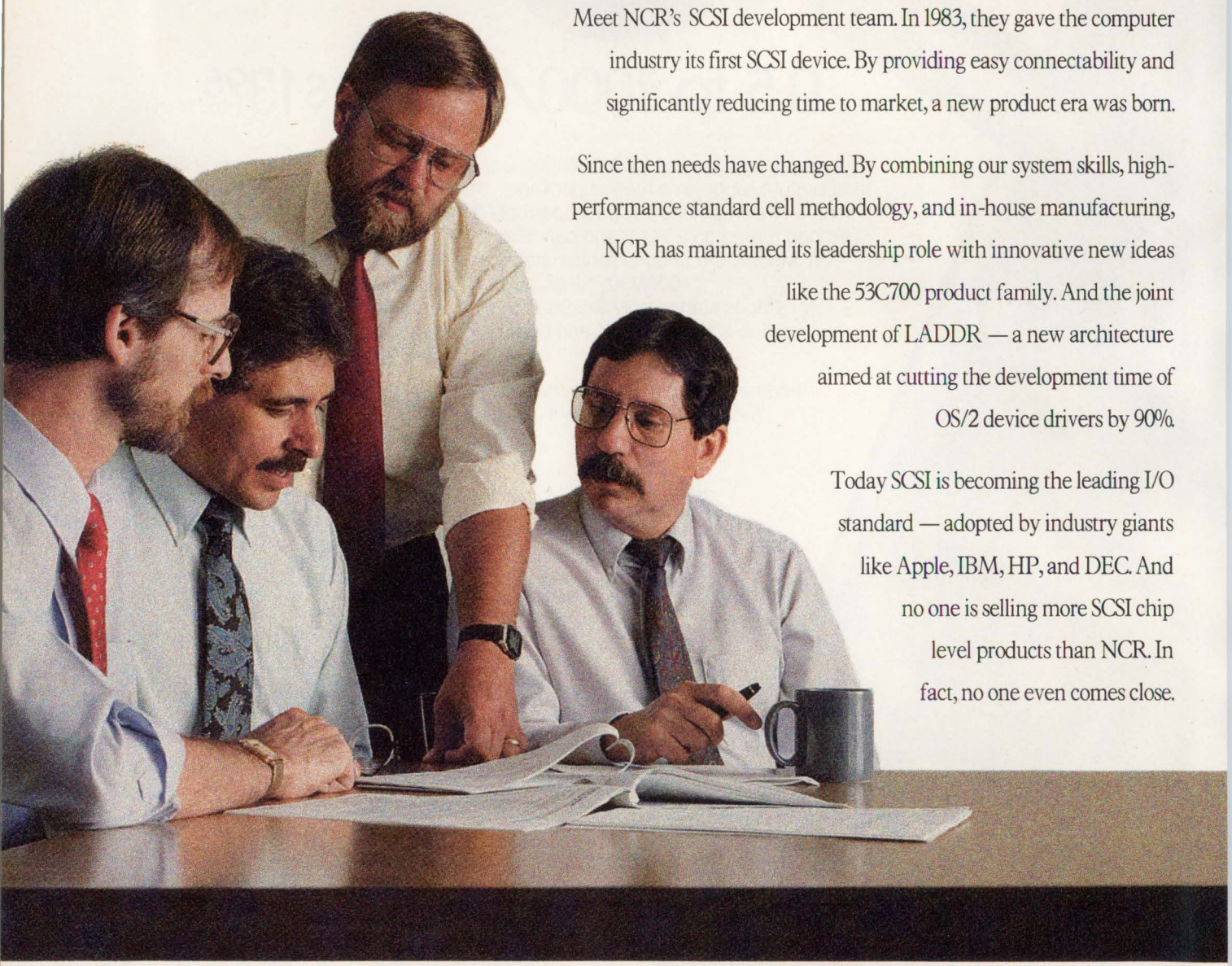
Here's one reason that over half of all SCSI devices sold are NCR.

We created the market... and we still lead the way.

Meet NCR's SCSI development team. In 1983, they gave the computer industry its first SCSI device. By providing easy connectability and significantly reducing time to market, a new product era was born.

Since then needs have changed. By combining our system skills, high-performance standard cell methodology, and in-house manufacturing, NCR has maintained its leadership role with innovative new ideas like the 53C700 product family. And the joint development of LADDR — a new architecture aimed at cutting the development time of OS/2 device drivers by 90%.

Today SCSI is becoming the leading I/O standard — adopted by industry giants like Apple, IBM, HP, and DEC. And no one is selling more SCSI chip level products than NCR. In fact, no one even comes close.



Part of the NCR SCSI Development Team: (left to right) **Jerry Armstrong**, Sr.Software Engineer; **Harry Mason**, Strategic Marketing Manager; **John Lohmeyer**, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and **Dave Skinner**, SCSI ProductManager.

North American Sales Headquarters
1731 Technology Drive, Suite 600
San Jose, CA 95110
(408) 453-0303

Here's another.

The NCR 53C700 SCSI I/O Processor... So good, *Electronic Design* named it the product of the year.

"You can't tell a good SCSI chip just by looking at it..." and according to Electronic Design, NCR's 53C700 is the best there is.

The only third generation SCSI device on the market today, it concentrates all the functions of an intelligent SCSI adapter board on a single, smart and extremely fast, chip... for about 15% of the cost.

As the first SCSI I/O processor on a chip, the 53C700 allows your CPU to work at maximum speed while initiating I/O operations up to thousands of times faster than any non-intelligent host adapter. DMA controllers can burst data at speeds of up to 50 Mbytes/s. This new chip cuts down system time hookup to a fraction of what it has been.

Those are just a few of the reasons Electronic Design's "Best of the Digital IC's" award went to NCR's 53C700 last year.

And now the NCR 53C710!

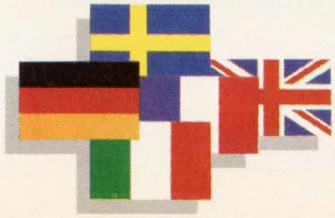
For the complete story on the NCR SCSI product line featuring the new 53C710, as well as the upcoming SCSI seminars with the NCR SCSI Development Team, please call:

1-800-334-5454

NCR

Creating value

CIRCLE 129



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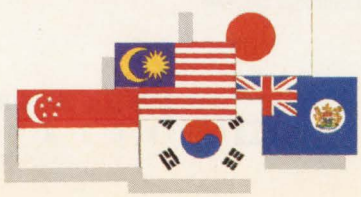

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Hong Kong
825 859 6044

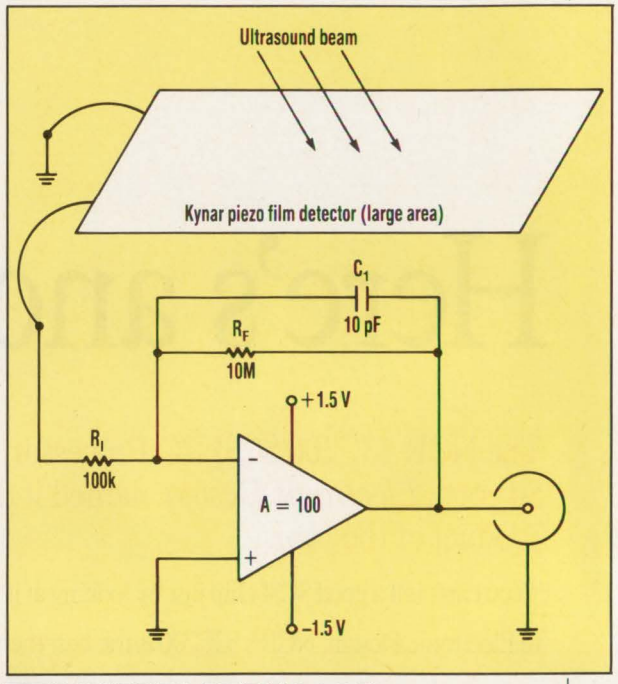
CIRCLE 523

ULTRASONIC AMP NEEDS JUST 3.5 μW

J. VANDANA
46, 52 St. S.W., Kalpakkam 603102, Tamilnadu, India; 04117-508.

The battery life for an ultrasonic amplifier, which is suitable for such applications as a distance finder, echo detector, or remote transducer, can be extended using this low-power circuit. The design consumes less than 3.5 μW with two 1.5-V lithium cells. It's designed for low-frequency ultrasonic waves to cover large distances—the maximum usable frequency is 40 kHz. The piezo-film detector has a typical impedance of 100 Ω at 10 kHz and 10 Ω at 100 kHz (this varies with detector-film thickness). The amplifier input resistance (R_1) can be reduced for higher frequencies as the source resistance of the piezo film diminishes with increasing frequency of the ultrasound signal. The dc gain of the amplifier shown is 100 *(see the figure)*.

Using the MAX406 amplifier's lowest I_Q (about 1.2 μA) increases battery life dramatically. The Kynar piezo film used in the circuit produces its own power output in the form of an ac voltage by employing the mechanical energy that it receives from the ultrasound waves. Hence, no power is wasted in the transducer. The amplifier can be substituted with a low-power, fast response IC to get a better high-frequency amplifier response using the same Kynar piezo transducer film.□



POWERED BY TWO 1.5-V lithium batteries, this ultrasonic amplifier circuit consumes only 3.5 μW. It's designed for low-frequency (up to 40 kHz) ultrasonic waves that cover large distances.

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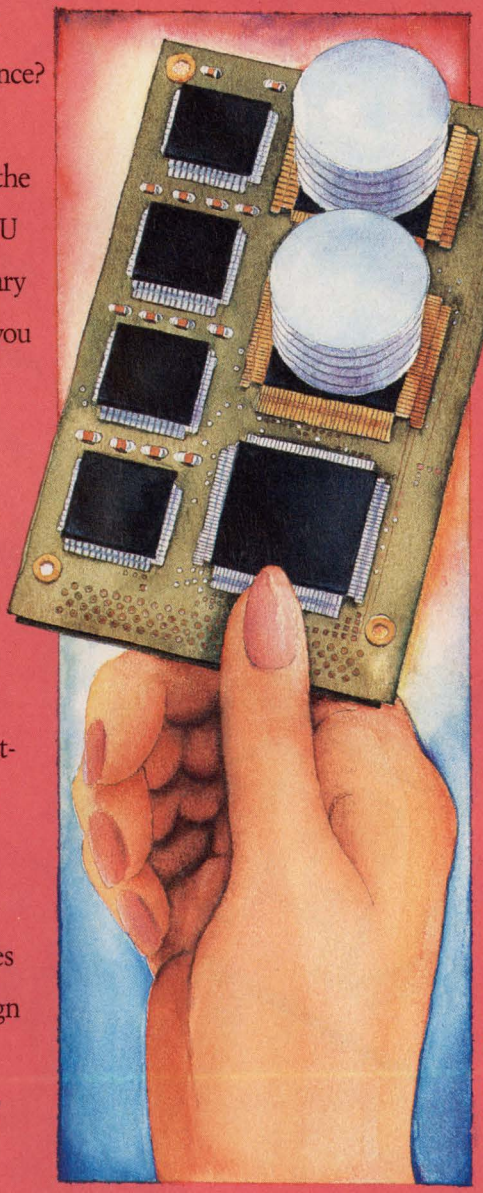

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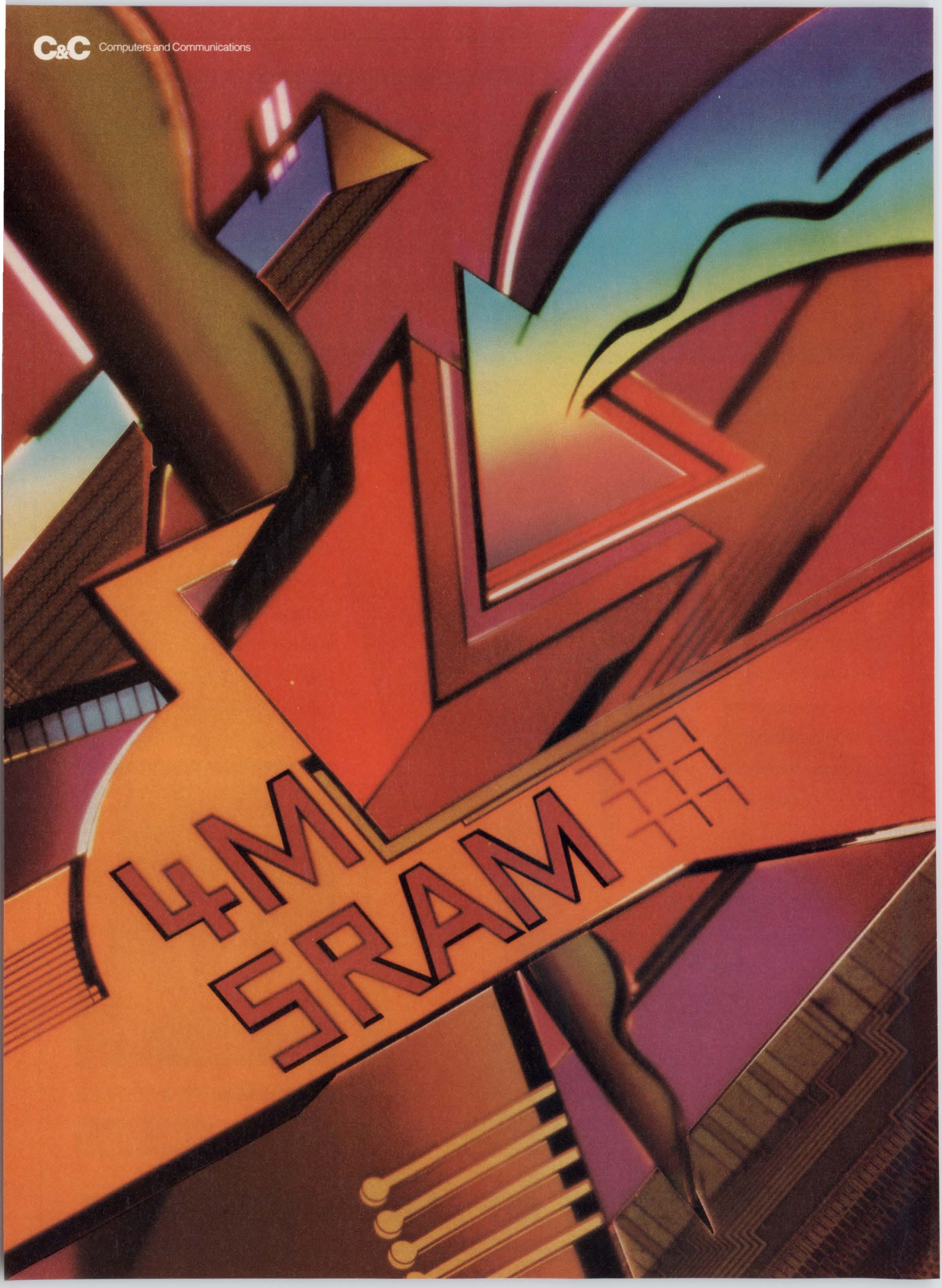

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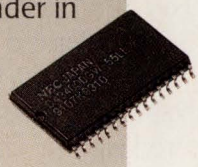

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NEC

CIRCLE 130

New Schematic Capture Front End for PSpice

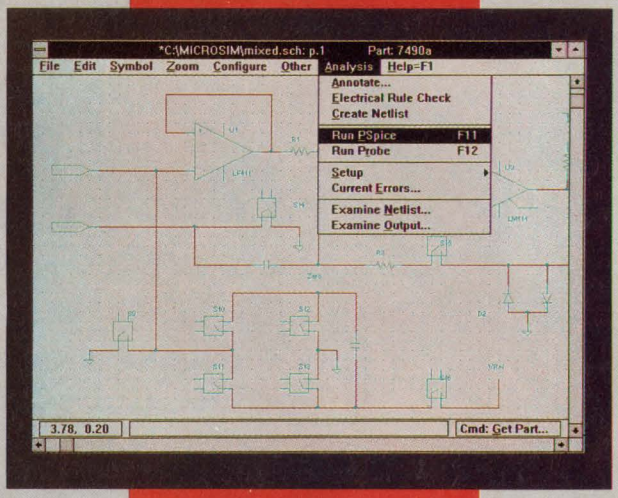
MicroSim Corporation now offers a versatile schematic capture front end, called Schematics, to our popular Circuit Analysis programs, PSpice and Probe. Schematics provides a unified system for designing and editing schematics, running analyses using PSpice, and viewing the results using Probe, all without leaving the Schematics environment. Any mix of analog and digital components can be used when defining a schematic for simulation.

Schematics provides a menu-driven interface for specifying analysis parameters and running simulations directly from the schematic display. If device simulation parameters need adjustment after running a simulation, they can be easily modified and the simulation rerun. Netlists for PSpice are generated automatically and can be examined on the screen.

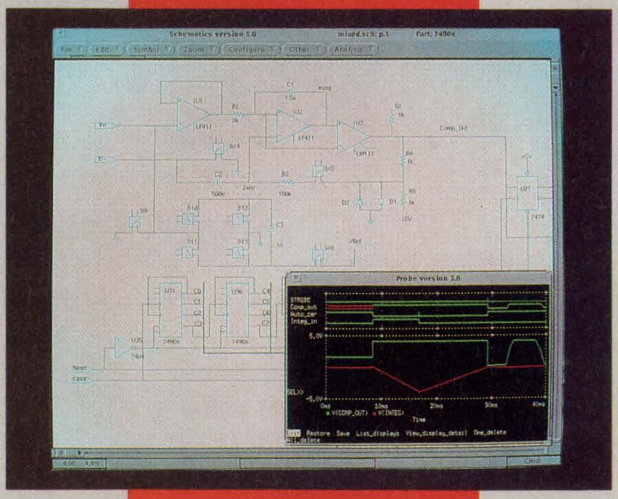
Schematics was designed and written as a native Windows 3.0 application for the PC and is also available as an OpenWindows application for the Sun-4 and SPARCstation. Both packages include the Schematics library with symbols for all parts contained in the PSpice libraries— over 3,500 analog and 1,500 digital components. An integrated symbol editor with full editing capability allows new symbols to be created and new part attributes to be defined while working on a schematic.

Schematics is sold as part of the Genesis package and comes with MicroSim Corporation's extensive customer/product support. Our expert engineering team is always on hand to answer your technical product questions.

For further information on Schematics, or any other MicroSim Corporation product, call toll free at (800) 245-3022 or FAX at (714) 455-0554.



Schematics as a Windows 3.0 application



Schematics with Probe

MicroSim Corporation

Expanding the Standard for Circuit Simulation

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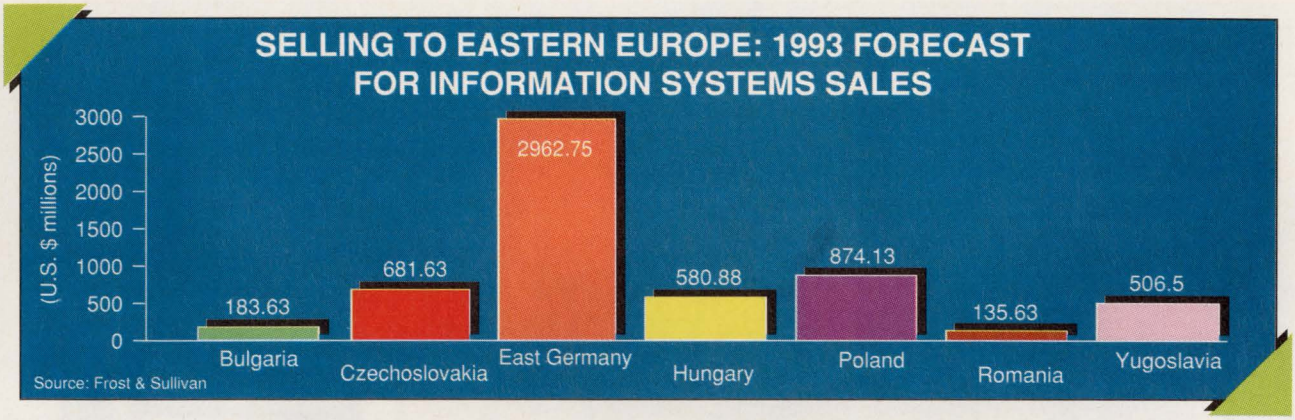
CIRCLE 132

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE



MARKET FACTS

Optimistic predictions of multibillion-dollar sales of computers and equipment to Eastern Europe are ebbing in the face of bureaucratic tangles and lack of cash in Comecon countries. Still, vendors of information-processing and communication equipment will capitalize on a market forecast to hit $3.8 billion to $5.9 billion in 1993. That's up from $1.68 billion in 1990. In selling to Eastern Europe, companies must be prepared to invest many dollars up front and wait for a long-term payoff, according to Frost & Sullivan, a New York, N. Y., market researcher.

As for products, strongest demand in Eastern Europe comes from the personal computer segment. East Germany alone will see early demand for mainframe computers. System suppliers can expect brisk sales of complete configurations, with demand for peripheral equipment and terminals growing in the second half of the decade.

As the most industrialized country of the Comecon block, East Germany should account for half the total shipments to the region. Markets for all equipment in Poland should amount to $719 million in 1993 and in Czechoslovakia to $569 million in 1993.

Some of the best opportunities in Eastern Europe will be for mid-size companies that can offer advice and training to their Comecon counterparts. Also, forming joint ventures with local companies speeds market entry. Among those forming joint ventures are computer makers Bull, Digital Equipment, IBM, and Siemens.

EYECATCHER

Delay in Months	Market Window in Months					
	6	12	18	24	30	36
1	24%	12%	8%	6%	5%	4%
2	44%	24%	16%	12%	10%	8%
3	63%	34%	24%	18%	15%	12%
4	78%	44%	31%	24%	19%	16%
5	90%	54%	38%	29%	24%	20%
6	100%	63%	44%	34%	28%	24%
7	100%	70%	51%	39%	32%	27%
8	100%	78%	57%	44%	36%	31%
9	100%	84%	63%	49%	41%	34%
10	100%	90%	68%	54%	44%	38%
11	100%	95%	73%	58%	48%	41%
12	100%	100%	78%	63%	52%	44%

Source: Logic Automation Ltd.

Delayed product introductions are expensive. As a result, hitting the market window on time has become more and more important for designers and managers. Logic Automation's chart shows just how much revenue is lost in arriving late to market .

QUICK NEWS: THE PROFESSION

Some engineers wish to change fields or want to know where they stand in terms of current knowledge. To help them, the IEEE's educational activities department is developing a skills assessment program (ESAP) for various fields. Developed by working engineers, each package has a field-specific knowledge inventory, a self-assessment test, and guidance information.

A pilot package has been developed for lightwave engineering. Work is under way on assessment packages for radar and navigation engineering, process-control engineering, engineering management, electromagnetic compatibility, and antennas and propagation. Still to be developed are packages for digital signal processing; acoustics, speech, and signal processing; analog circuits; expert-system shells; power electronics; VLSI; microwave engineering; intellectual property management; and communications switching.

To widen the scope of the program, the society seeks volunteers from industry and academia. Engineers interested in the program may contact Bernard Mirowsky, program manager, Engineering Skills Assessment Program at (908) 562-5487.

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-Time, Big-Time.

One glance at the full array of options Motorola offers in real-time, and you'll see why it's become the developer's platform of choice. For both target and host environments, no other single vendor has anything like it.

One reason is our long-time experience with real-time technology, beginning with our pioneering work back in 1980. Another is the broad spectrum of our product line, which includes ICs, boards, systems, and software. In short, Motorola has everything you need to build real-time applications ranging from simulation to industrial automation to imaging and more.

CISC RISC

Yet another reason to choose Motorola is our unending commitment to open standards. Our real-time platform gives you standards-based choices at various levels of integration. The centerpiece of this non-proprietary approach is VMEexec,™ our wide-open, totally integrated development environment. VMEexec allows you to use standard UNIX® interfaces to write a single set of application code, and then reuse it for other projects. Better still, you can combine any software product that conforms to these standards. VMEexec includes a high-performance real-time executive, a strong run-time connection to UNIX-based systems, flexible and efficient real-time I/O and file systems, as well as powerful development and debug capabilities. And because VMEexec is integrated with the hardware, you can begin software development even before the hardware is available.

If you're thinking about real-time, you should be thinking about time to market, and that's all the more reason to think Motorola. Especially when you consider that we can help speed product integration by serving as a single source for boards, software and systems. Add to that the industry's best applications expertise and design support, ranging from small embedded control systems to multi-processor simulation. Then factor in Six Sigma quality control. And remember that Motorola gives you the industry's only true migration path from CISC to RISC in both the development and run-time environments.

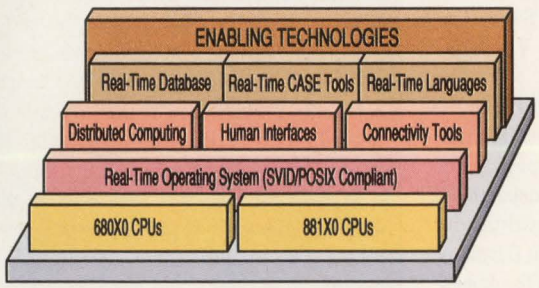
Right now, Motorola real-time systems are hard at work in critical applications worldwide.

Give us a call today at **1-800-624-8999**, ext. 230, and put the real-time resources of Motorola on your side. We think you'll find the benefits are very big, and very real.

We Do Real-Time Full-Time.

At Motorola, we've dedicated an entire division solely to real-time development systems. Our real-time system architecture begins at the microprocessor level in either CISC or RISC, and extends all the way to the end-user. Today, you can use VMEexec to port UNIX applications to an SVID-compliant (and soon, POSIX-compliant) real-time environment, and vice versa. And they can be used for run-time capabilities as well as for development. Several human interfaces are available for UNIX, including Motif, X.11 and DeltaWINDOWS.™ As for networking, Motorola supports all popular protocols, including TCP/IP, NFS, SNA, OSI, and X.400. We also offer database and CASE tools, and you can work in C, LISP, FORTRAN, ADA, BASIC, COBOL, and PASCAL. Put it all together, and you will discover only one company gives you the full story on real-time, and that's Motorola.

INTEGRATED REAL-TIME PLATFORM



MOTOROLA
Computer Group

CIRCLE 126

QUICKLOOK

OFFERS YOU CAN'T REFUSE

For each 18°F increase in temperature, on-line production shutdowns occur twice as often, research shows. A free audio tape gives technical information on Vortex Control coolers for process controls and electronics operating in harsh industrial environments.

Contact the company at 10125 Carver Rd., Cincinnati, OH 45242; (800) 441-7475.

CIRCLE 538

A free catalog from MagneTek Inc. contains applications, specifications, schematics, and technical notes for 17 lines of power transformers, inductors, and audio transformers. For a copy, contact the company at 1124 E. Franklin St., Huntington, IN 46750; (219) 356-7100; fax (219) 356-3148.

CIRCLE 539

Power supplies are described in a catalog on disk from Computer Products/Power Conversion America (PCA). The disk gives details on 400 standard ac/dc and dc/dc power converters. To obtain the PowerPath disk, contact the company at 3797 Spinnaker Ct., P. O. Box 5102, Fremont, CA 94537-5102; (415) 657-6700; fax (415) 683-6400.

CIRCLE 540

Also new is "Cell-Based Products Questions and Answers" (BR746/D). The booklet covers common questions about Motorola's standard-cell family. The brochures are available through Motorola Literature Distribution, P.O. Box 20912, Phoenix, AZ 85036.

CIRCLE 541

A report on mixed analog-digital simulation compares commercial simulators, including Saber/CADAT, Lsim/HSpice, Viewsim/AD/PSpice, and ANDI.

"Mixed-Analog-Digital Simulation in the 1990's" was written by Hans Klein. He organized the first European symposium on mized-signal simulation while department head for circuit design at the Institute for Microelectronics in Stuttgart, West Germany.

The report, which sells for $995 for domestic customers at $1350 for international customers, is available from Technology Information Publishing, 218 Coronado Dr., Aptos, CA 95003; (408) 685-9217.

CIRCLE 542

DID YOU KNOW?

. . . during 1990, nearly 6% of engineers experienced involuntary unemployment, averaging 17 weeks. Also, there is a decline in typical percentage increase and absolute increase in salaries after the age of 54.

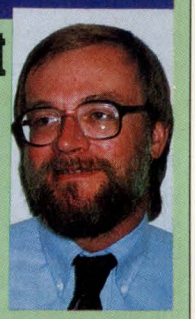
1991 IEEE U. S. Membership Salary & Fringe Benefit Survey

. . . that the U.S. spends more money than any other country in the world on the writing of software, yet just 2% of that software is ever used.

Abraxas Software Inc.

KMET'S KORNER

...Perspectives on Time-to-Market



BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458, fax (408) 253-6085

Experienced participants on new-product-development teams know that a project's execution phase takes place a day at a time. Each day is extremely important: A day wasted working in the wrong direction cannot be made up later. A thorough, well-structured plan produced in the planning phase makes it possible to track the execution of the project on a real-time basis. That way, trends in work progress can be monitored and measured as a function of time. Often, if plan managers are good synthesizers of tactical and logistical maneuvers, problem areas relating strictly to execution can be detected with adequate warning time to take corrective action. Thus, they avoid a slipped project milestone.

Since early warning and immediate action are key ingredients needed to curtail execution problems, a task-tracking system that provides quality information is essential. The computer tools selected for the project perform this function. As time goes by, the date of commencing work on a task is recorded and compared to the start date of the task specified in the plan. Deviations from planned start are observed by the management team. Quite likely questions are asked in those areas that appear to be off to a slow start. As such, the plan has comparative value to help direct attention to potential problems after the execution phase is only a few days old. Once a week or two has gone by, data will become available on whether planned task completions have actually been achieved.

As such, data on actual project performance as compared to plan is used to help the project team make an effective transition into the execution phase. To simplify measurement and to avoid any ambiguity, tasks are considered complete when they are complete. No credit is given for partial accomplishment—the task has to be 100% done to be recorded as complete, or the model must be adjusted to reflect the situation.

This can be done because the resolution of computed task durations contained within the database has been structured so that each resource is scheduled to complete one to two tasks per month. Data spaced at two- to four-week intervals are all that is required to make informed interpretations of trends contained within the data. At four weeks or less into the execution phase, a trend line for each resource appears.

If the first task was completed as planned, it is likely to draw little management attention. However, if at this point the completion of the first task is early or late, determination of preliminary cause is justified. Being early could mean that work quantity was underestimated or that the resource commitment was larger than necessary. Completing a task late may be caused by a low estimate of work quantity, too small a work rate on the task, low productivity, or a combination of the previous factors. So only a few weeks into the execution phase, data has been effective at directing management attention to areas where potential problems may exist.

QUICKLOOK

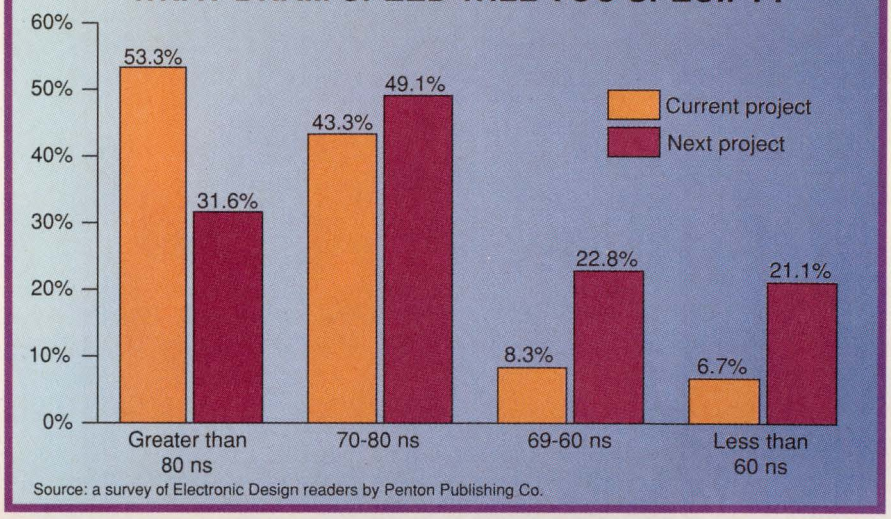
HOT PC PRODUCTS

The latest version of Flow Charting 3 affords laser printer output of single, canvas, and multipage charts in landscape or portrait views. Charts can be changed quickly from one orientation to another.

From Patton & Patton Software Corp., the flow chart program has international character support and stamps for filename, time, and date. Flow Charting 3 version 1.11, which supports shared and networked printers, can convert charts into WordPerfect's graphic format. The program also has point-and-shoot file management. More than 200 shape sizes can be used.

For more information, contact the company at 485 Cochrane Circle, Morgan Hill, CA 95037; (707) 578-0377. CIRCLE 542

DRAM SURVEY



Source: a survey of Electronic Design readers by Penton Publishing Co.

TIPS ON INVESTING

For many engineering investors, the 1990s will present some daunting financial challenges. Among them is reinvestment risk, the danger that lower interest rates will make it difficult to find comparable yields and maintain investment income when their fixed-income investments mature. Understanding reinvestment risk depends on knowing underlying economic forces.

In the 80s, the U.S. economy experienced the longest expansion period in its history. The stock market rose 314% in the decade as measured by the Dow Jones industrial average. Inflation fell from 13% in 1981 to 4.8% by 1989. Yet the 80s saw explosive, and some observers say, irresponsible debt growth, shown by leveraged buyouts, junk bonds, speculation in commercial real estate, materialism, and high consumer debt.

The 90s will be much different from the 80s, thanks to demographic, economic, and market forces. Recession has replaced expansion, at least temporarily. Debt has been repudiated by businesses and individuals. And materialism is giving way to a family-oriented lifestyle, in which saving for the future takes priority. Increased savings and less borrowing for consumer spending will affect inflation, interest rates, and investments.

The tremendous growth of debt since the mid-50s was fueled by high inflation rates. Consumers borrowed to build houses and businesses borrowed to build capacity. Both paid back loans in depreciated dollars. Debt skyrocketed. By the 80s, back-to-back recessions and other factors began to unwind inflation. In 1986, the private sector's total debt growth peaked and has been rising at lower rates since then. Lower interest rates can put first homes within reach of younger engineers. For older and retired engineers, lower inflation rates preserve the purchasing power of assets and of fixed incomes.

For some investors, however, these conditions present reinvestment risk. Income-oriented investors used to cash investments such as CDs. Tresury bills, and money funds yielding between 8% and 9% in the 80s may not be able to find comparable yields when their investments mature in the 90s. For a free copy of "Investing in the 90s—a new Economic Order," call or write to me at the address below.

Henry Wiesel is a financial consultant with Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221; (800) 221-0073 in New Jersey.

QUICK NEWS: EDUCATION

A course on videotape covers using fiber-optic communications in digital transmission systems. From the Information Factory, "Introduction to Fiber Optic Communications" deals with principles of lightwave transmission, components of lightwave systems, installation and use of fiber optics, and digital fiber optic systems.

Other videotape courses, which offer manuals, include introductions to telecommunications, local area networks, and digital transmission, T1, and ISDN.

Programs are available for a 15-day approval or review period. Contact the Information Factory, 208 Charter Oaks Circle, Los Gatos, CA 95030-9957; (408) 374-1235.

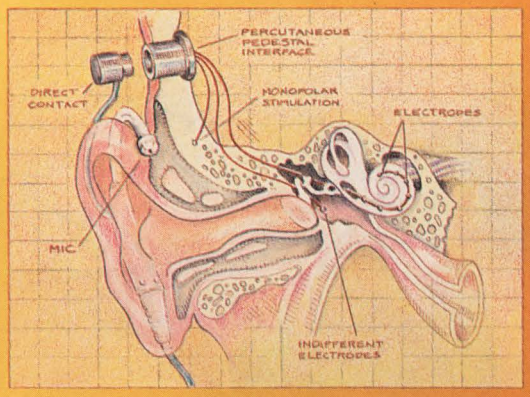
More than 40 engineering courses can be rented on videotape from the University of Illinois at Urbana-Champaign. Digital Signals and Systems (ECE 310), for example, is a basic course on digital signal processing.

It covers discrete-time signals and systems, z-transforms, convolution, sampling theorem, data conversion, digital filter design, discrete Fourier analysis, and the fast Fourier transform, quantization effects, along with some applications.

For further information, contact the Office of Continuing Education, University of Illinois at Urbana-Champaign, 422 Engineering Hall, 1308 W. Green St., Urbana, IL 61801; (217) 333-6634.

We call it a FET Array.

She'd call it a Miracle.



Hammer. Anvil. Stirrup. Drum. Simple names for the complex natural "hardware" that allows us to hear. If it's injured—or congenitally defective—the deafness that occurs can't always be helped by conventional hearing aid.

A co*chlear implant* bypasses the damage, delivering filtered and processed analog signals directly to electrodes implanted deep in the inner ear. These signals stimulate the audio nerves in a natural way, allowing—in most cases—the deaf to hear.

The variety of applications for our new *RFA120* never ceases to amaze us. But then, a linear array that combines *both* bipolar *and* JFET gain blocks can provide some pretty versatile characteristics:

RFA120 FET Array
Operating Range: ±5V to ±15V
Input Offset Voltage: 5 mV typ.
Input Bias Current: 30 pA typ.
Gain Bandwidth Product: 3.0 MHz typ.
Slew Rate (Gain = +1): 8 Vμs

The RFA120 is a low power device that's ideal for signal conditioning applications. One of our favorites also takes advantage of its small size.

It's a *cochlear implant system* that bypasses injured or congenitally defective "hardware" in the ear canal. The system converts audio signals to analog signals, routing them deep into the inner ear to stimulate the natural audio nerves that are "hardwired" to the brain.

We're committed to analog technology.

And we're committed to helping you develop creative, cost effective solutions.

Our *Win-Win* program is a good example. It lets you get to market quickly with a semicustom array, then shift to full custom as sales increase. It's fast, flexible and makes good business sense because it eliminates the risk of going full custom before you're really ready.

If you'd like more information on our analog arrays, give us a call at 1-800-722-7074. We'll send you our new brochure.

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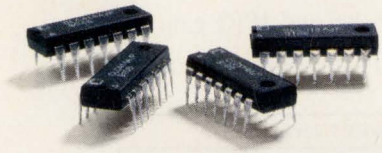
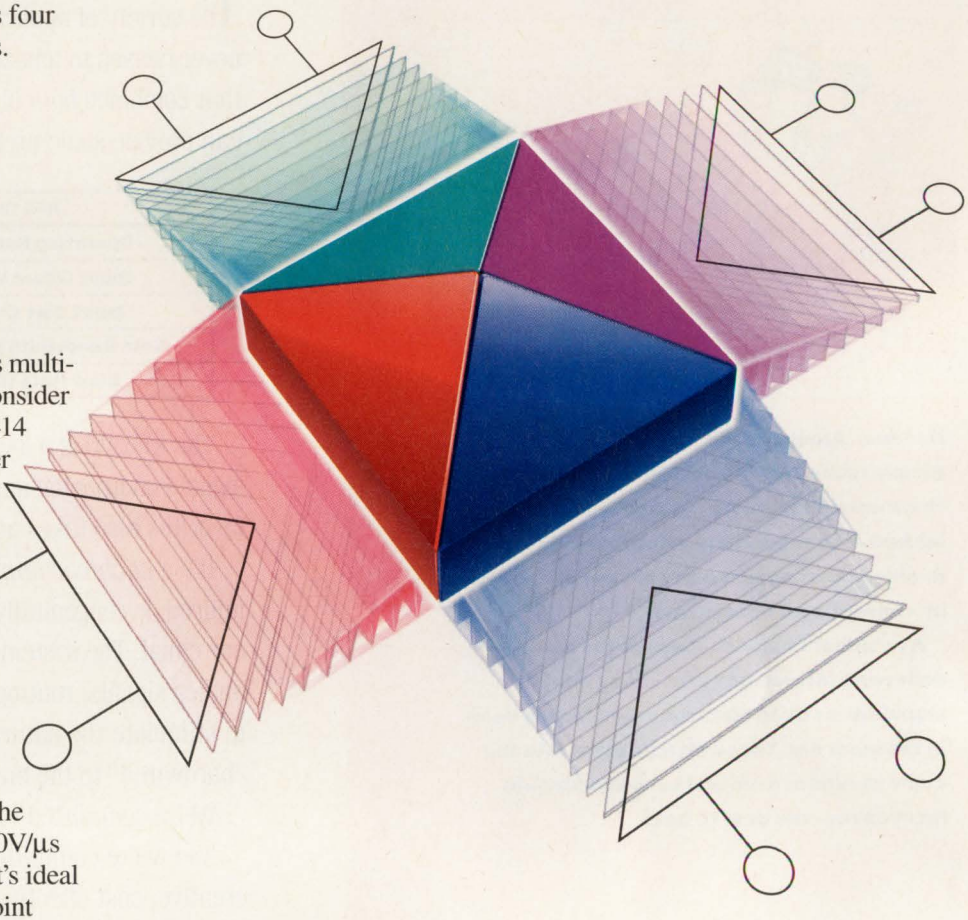
CIRCLE 138

Because you're thinking fast...

Our new high-performance quads compress space and cost.

Multi-channel designs have you in a corner? Want to cut cost and space? Then take a look at Comlinear's four new high-speed quad amplifiers.





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For high-speed designs such as multi-stage active filters and video, consider these quads. The 90MHz CLC414 offers high speed and low power with a 1000V/µs slew rate at just 2mA per channel. And our 160MHz CLC415 combines excellent video specs with a fast 1500V/µs slew rate at only 5mA per channel.

CIRCLE 94

Buffers for video and more.

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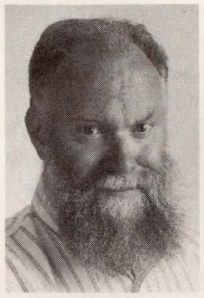
WHAT'S ALL THIS CRITICAL THINKING STUFF, ANYHOW?

Last year, I attended a little conference of Community College Electronics Teachers up at Truckee Meadows Community College in the foothills north of Reno, Nevada. I must admit, I was not very familiar with the exact nature of Community Colleges (two-year colleges). But I wanted to learn more, because we've had some very good luck hiring bright young people from some community colleges, and I wanted to understand why. I wanted to case the joint.

One of the first speakers asked the entire audience of 100-plus teachers, "How many of you built model airplanes when you were young?" To my amazement, about 92% of the people held up their hands. So, he observed that many people who now work in technical electronics were intrigued by building little planes with balsa and glue. These days, I doubt if you would get such a significant show of hands in a classroom, but still I would guess that most electronics engineers now older than 40 once had a hobby of building model planes. So, that's some of our "roots," our common heritage, and we wouldn't have known it if this guy had not asked the question.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Later, there was a panel session on the topic, "What do you look for when you are interviewing a person for a technician's job?" I observed that I looked for a technician or young engineer that could handle a tricky problem of a type that he (or she) has never seen before. I think that's more important than to ask a problem of a fundamental type that all students should be able to handle well. I like to ask obscure questions. I like to see what they say when challenged with a question of a sort they have never heard before. I like to hear the gears clashing and grinding inside their heads....

Then another panelist got up to propose that if he is deciding to hire a new engineer or technician, he looks for their ability to do critical thinking, because Title 5 of the California Education Code calls for all college students to be subjected to courses in Critical Thinking. Boy, did I perk up my ears! What *is* this Critical Thinking? In the simplest sense, Critical Thinking consists of teaching students to be thoughtful and reasoning and to question what they are learning. Does it do any harm to memorize that Napoleon was defeated at Waterloo in 1815? It might seem to do no harm. *But*, in every student's schedule, there is only a limited amount of time. If you waste all of your time learning diddly facts like that, you will not learn *why* things are important. *Why* did Napoleon get beaten at Waterloo? *Why* do we measure the CMRR of an op amp the way we do? If a big expensive tester says an op amp has a gain of 88 dB and we measure 112 dB on the bench, the expensive tester must be correct, right? Oh, but not necessarily so. If my boss asks me to take some data, but I detect a pattern that indicates something is broken–what do I do if my boss isn't around to give me advice? When you think of it, a large amount of your learning is involved in figuring out what makes sense, and what to do when you come up against contradictions.

When I am hiring a technician or an engineer, I am really interested in hiring a person who has good judgment, and is not afraid to question his data, or the machine that's taking the data, or even to question *me* if I ask him to do something that really has an error built into it. One of my readers recently sent me some notes about the Responsibility of the Experimentalist: [1]

"When doing an experiment, it is important for the experimentalist not to accept the data as correct without adequately questioning it:

1. If the data are semi-automatically recorded, then examine the "raw" data closely to determine whether the equipment malfunctioned.

2. After recording the data in your notebook, examine the numbers for observational mistakes. Examination of the numbers may also reveal an equipment malfunction that was not previously detected.

3. Before making use of the techniques for propagating errors through the various intermediate steps and into the final result, use *common sense* and ask yourself whether a given experimental result or error is reasonable. If it's not, there's an excellent chance that either the equipment malfunctioned or you made an arithmetic or observational mistake (note the distinction between *mistake* and *error*). A standard sample or a standard test signal may often be available for the experiment or instrumentation to give a known result. You're urged to devise tests of this sort in order to avoid this kind of mistake."

So, when you take data, or when you run tests, keep aware of how things make sense, and flag it if things don't make sense. As Tom Milligan, one of my old production test managers used to tell his test technicians, "If it looks funny, Record Amount of Funny." We call that "Milligan's Law," in his honor.

Now, getting back more specifically into Critical Thinking, I found a very good book with that title written by Dr. Richard Paul. Its subtitle read "What every person needs to survive in a rapidly changing world". I went out and bought the book, and it makes good

PEASE PORRIDGE

reading.[2] In addition, the people at the Foundation for Critical Thinking sent me a nice brochure about their 11th Annual International Conference on Critical Thinking coming August 4-7, 1991 at Sonoma State University.[3] The brochure said "A critical education...appeals to reason and evidence. Students should not approach their classes as so many unconnected fields, each with a mass of information to be blindly memorized, but rather as organized systems for thinking clearly, accurately, and precisely about interconnected domains of human life and experience."

The converse may well be expressed as, "School is going fine...but I'm too busy cramming content into my skull to think about what I read, let alone develop an intelligent view. When do I get to think for myself? Am I condemned to be a memory bank of meaningless words?" Well, I should hope not. The education that I get, that my children get, that my technicians and engineers get, had better consist of a *lot* of Critical Thinking.

Recently Helen Cage, a furnace operator in National's Arlington, Texas plant, was running a special new low-temperature-oxide process. She was reading in the log books that previous operators had been logging in numbers for phosphine flow. She was surprised because she knew this operation did not require phosphine. She contacted Engineering, who investigated and concluded that the phosphine notation must have been some kind of incorrect entry. The next day, Helen was watching the gas-flow indicators on the next run–and the phosphine was flowing. She contacted Engineering again, and insisted that they find out why the phosphine was flowing when it was required to be off. When they searched a little harder, they found some kind of computer error–phosphine was being turned on for all processes, whether they needed it or not. Helen Cage, by refusing to take *Yes* for an answer, was a hero, because she didn't believe she should just follow instructions without thinking. Now, that's good Critical Thinking. I don't know where Ms. Cage went to school, but she's the kind of person I want on my team!

All for now. / Comments invited! /
RAP / Robert A. Pease / Engineer

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Santa Clara, CA 95052-8090

[1] From the book, *The Art of Experimental Physics*, by Daryl W. Preston and Eric Dietz, John Wiley and Sons, NY.

[2] *Critical Thinking* by Richard Paul; available for $19.95 from the Foundation for Critical Thinking, see below.

[3] Foundation for Critical Thinking, 4655 Sonoma Mountain Road, Santa Rosa, CA 95404; (707) 546-4926.

NEW

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- RTSI bus for multiboard synchronization
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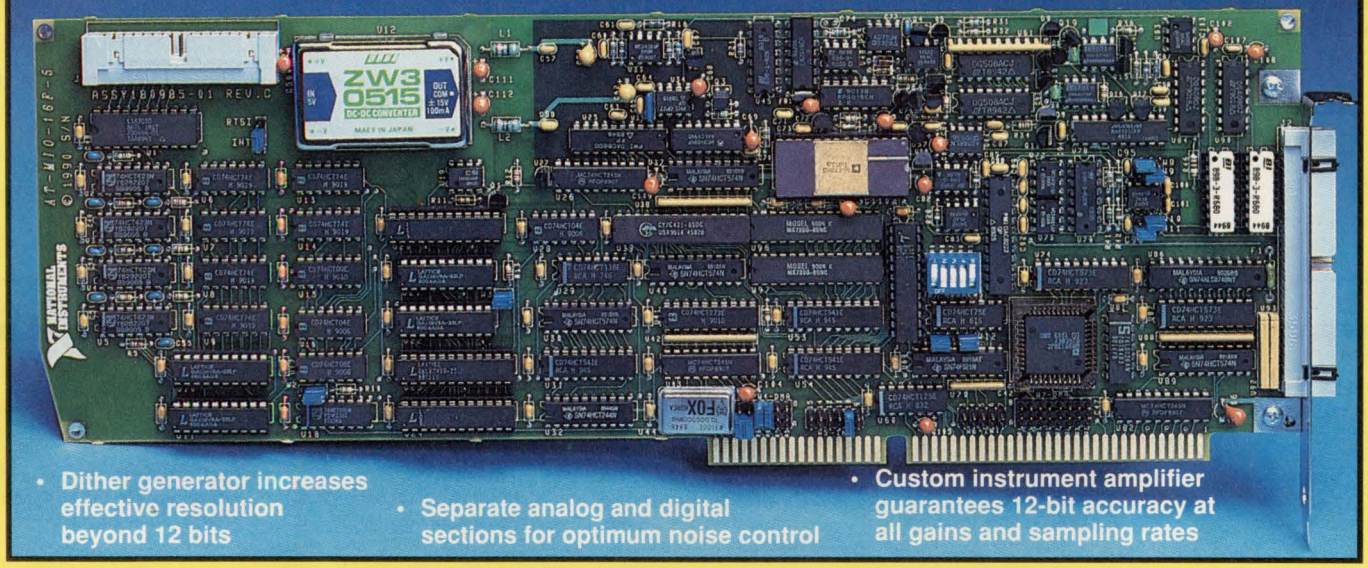

- Dither generator increases effective resolution beyond 12 bits
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The National Instruments AT-MIO-16F-5 Sets the New Standard

It takes a serious commitment to quality to deliver data acquisition boards that reliably meet the most demanding specifications. Our new AT-MIO-16F-5 creates a new standard in excellence with several firsts, including a proprietary ultra high-performance instrumentation amplifier, a dither generator for extended resolution, and self-calibration that eliminates the need for external signals required by other "self-calibrating" boards. The quality, innovation, and performance of our AT-MIO-16F-5 sets the new standard in PC data acquisition. As the table below shows, the rest of our extensive PC product line surpasses industry standards. Each board undergoes a 48-hour burn-in, and passes a thorough system test to guarantee linearity, fast analog input settling, high common-mode rejection, and low noise. At National Instruments, we're serious about data acquisition.

Data Acquisition Board	Computer Bus	Analog Input: Channels*	Max Sampling Rate (samples/sec)	Resolution (bits)	Ranges (V)	Gains	Analog Output: Channels	Resolution (bits)	Digital I/O Channels	Counter/Timers	Software: LabWindows	DOS LabDriver	PC LabDriver	Measure	VisionScope	Third Party
AT-MIO-16F-5	AT	16 SE 8 DI	200,000	12	±5, 0 to 10	0.5, 1, 2, 5, 10, 20, 50, 100	2	12	8	3	√	√				
AT-MIO-16H-9 AT-MIO-16H-15 AT-MIO-16H-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 2, 4, 8	2	12	8	3	√ √ √	√ √ √		√ √ √		√ √ √
AT-MIO-16L-9 AT-MIO-16L-15 AT-MIO-16L-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 10, 100, 500	2	12	8	3	√ √ √	√ √ √		√ √ √		√ √ √
Lab-PC	XT	8 SE	62,500	12	±5, 0 to 10	1, 2, 5, 10, 20, 50, 100	2	12	24	3	√	√	√	√		√
PC-LPM-16	XT	16 SE	50,000	12	±5, 0 to 10 ±2.5, 0 to 5	1	–	–	16†	3	√	√	√			
AT-DIO-32F PC-DIO-96 PC-DIO-24	AT XT XT	– – –	– – –	– – –	– – –	– – –	– – –	– – –	32 96 24	– – –	√ √ √	√ √ √	 √ √			√ √
PC-TIO-10	XT	–	–	–	–	–	–	–	16	10	√	√	√			
EISA-A2000	EISA	4 SE SS	1,000,000	12	±5	1	–	–	–	–	√	√			√	

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Silicon Valley Personal Computer Design Conference

The Conference on New Architectures and Technology for the Design of Personal Computers

SVPC'91 is the only technical conference dedicated to the design of hardware and software for personal computers systems, providing design engineers with SOLUTIONS to many difficult system design and integration problems. Over 100 technical presentations and 10 tutorials will be delivered by well-known professionals amassed from all levels of the personal computer industry, worldwide. SVPC'91 will bring together hundreds of designers and strategic planners to advance the state-of-the-art in desk top computer systems design.

July 8-10, 1991

●

Red Lion Hotel
San Jose, California

The conference is structured such that the first day, July 8th, will provide 10 four-hour tutorials - 5 in the morning and 5 in the afternoon. The remaining 2 days will present, in 3 parallel technical session tracks, over 100 speakers describing innovative design approaches to implementing high performance desktop and portable systems.

Coffee break refreshments as well as lunches are included in the conference registration. Vendor exhibits showing the latest components for system designers will be open for 2 hours starting at noon on Tuesday & Wednesday. A reception in the exhibits area will be held Tuesday evening.

Monday, July 8th -TUTORIALS- (1 through 5; 8:00 AM - 12:00 PM) (6 through 10; 1:00 PM - 5:00 PM)

TUTORIAL 1 Basic Approaches to PC Caches Intel Corp.	TUTORIAL 2 Portable System Design Issues Intel Corp.	TUTORIAL 3 Multifunction Peripherals National Semiconductor	TUTORIAL 4 Basics of SCSI-1 & SCSI-2 NCR Corp.	TUTORIAL 5 Designing with High Speed PLD Intel Corp.
TUTORIAL 6 BIOS Design Award Software	TUTORIAL 7 Portable Power Technology Gates Energy Products	TUTORIAL 8 Data/Image compression Oak Technologies & Adv. Hardware Architectures	TUTORIAL 9 Integrating SCSI with CAM Ballard Synergy	TUTORIAL 10 Bringing Technology to Market Regis McKenna, Inc.

Tuesday, July 9th, 8:00 AM -OPENING KEYNOTE and TECHNICAL SESSIONS-
"Beyond the Single Chip PC" - Gordon Campbell, CEO, Chips & Technologies Inc.

TRACK I

- DISPLAY BASICS -
CRT Display Technology Directions; Advances in Video RAM Architectures; Advances in RAMDACs and Color Palettes; Where to Put Intelligence in Graphics.

- HIGH PERFORMANCE DISPLAY CONTROLLERS -
Understanding VGA Benchmarks; Implementing Advanced Features in VGA Systems; VRAM-Based Ultra-VGA Controllers; Bringing Workstation Graphics to PCs; Implementing 3D Graphics on a PC Add-in Card.

Above papers by: AT&T Microelectronics; Chips and Technologies; Information Associates; Inmos; NCR; Oak Technology; TI; Yamaha Systems Technology Div..

TRACK II

- MOTHERBOARD DESIGN ISSUES -
PC Chip Set Market Trends: Challenges and Opportunities; Designing High-Integration EISA Motherboards; Implement Compact EISA-Based Systems; A CPU-Speed-Independent Micro Channel Motherboard.

- BIOS AND SYSTEM PERFORMANCE ISSUES -
BIOS Architectural Support for New Chip Sets; Flash Memory: The Ideal BIOS Storage Device; Memory Subsystem Architectural Options; An Algorithm for Dynamic Memory Management; A New Enhanced-Mode DRAM for PC-based Workstations; Smaller, Faster, Cheaper, and Hotter: Thermal Problems and Cooling Solutions.

Above papers by: Intel; NMB; Opti; Phoenix; TI; Toshiba.

TRACK III

- BATTERY-POWERED SYSTEM ISSUES -
Designing Low Voltage Systems; Battery Technology: Current Status and Projections; Clock Synthesis for Laptops; Battery System Management.

- LAPTOP SYSTEM DESIGN APPROACHES -
ROM BIOS: The Best Place for Laptop Power Management; BIOS Modifications/Enhancements for Transparent Power Management for the i386SL; Power Management in Laptop Computers; Power Management in Portable Computers; Managing Power in Systems Based on the AM386DXL; Implementing High-Performance Laptops.

Above papers by: AMD; AT&T Microelectronics; Avasem; Benchmarq Microelectronics; Gates Energy Products; Intel; Phoenix; TI; VLSI Technology.

12:00 PM through 2:00 PM LUNCH AND EXHIBITS OPEN

- ACCELERATING GRAPHICS -
Accelerating 3D Graphics on a PC; Implement an Accelerated Windows Graphics Controller; Apply Multiple Processors to Accelerate GUIs; Accelerate GUIs With Smart Bus Control.

- MULTIMEDIA HARDWARE APPROACHES -
Adding Video to PC Graphics; Low-Cost Approaches to Video Compression; Integrating DSP into PC Systems; Developing Application Processors for Multimedia; Implementing Systems with DVI Technology.

Above papers by: Chips and Technologies; Intel; Inmos; Philips Components (Signetics); TI; Spectrum Signal Processing; Weitek.

- ADVANCED CACHE SUBSYSTEM DESIGN -
Choosing the Right Cache Architecture for PC Applications; 50-MHz Cache Solutions; Hardware-Level Concurrency in a 386/486 Write-Back Cache; Managing Cache Coherency; in Multiprocessing Systems.

- IMAGE AND VOICE I/O -
Apply Sampled-Data Storage for PC Analog I/O; Designing High-Speed Modems; Modular Modem Design - A Flexible Solution; Image Communications With PCs; Designing A Combination PC-Fax, Modem, and Voice-Mail Card.

Above papers by: AT&T Microelectronics; Chips and Technologies; Intel; Information Storage Devices; Mosel; National Semiconductor; Opti; TI; Yamaha Systems Technology Div.

- PORTABLE SYSTEM DESIGN ISSUES -
Designing a Two-Chip Notebook PC; Creating State-of-the-Art Notebook Computers; Building a Single-Board SPARC-based Laptop/Desktop Computer; Combining the EISA Bus and the M88000 RISC to Build Single-Board Systems; Memory Management Techniques for Laptops.

- 4:00 PM Panel Discussion -

Above papers by: Chips and Technologies; LSI Logic; Motorola; Oak Technology; VLSI Technology.

5:00 PM EXHIBITOR RECEPTION/EXHIBITS OPEN

Technical Sessions continued on next page

Sponsored by SysTech Research in cooperation with Electronic Design (a Penton publication), Intel Corp., NCR Corp., NMB Technologies, and Yamaha Systems Technology Div.

Wednesday, July 10th, 8:00 AM -OPENING KEYNOTE and TECHNICAL SESSIONS-
"The 10 PCs You'll Never See" - Mike Aymar, VP & General Manager, Microcomputer Div., Intel Corp.

TRACK I

- FLAT PANEL BASICS -
Flat Panel Design Options; Flat Panel Displays for Portable Systems; CGA Graphics for Handheld/Low-end Portables; Controlling Full-Color VGA Flat Panels.

- DEALING WITH GUIs -
A High-Speed Video Digitizer for the Apple Macintosh; System Software Needs of the new Operating Environments: OS/2 and Windows; Designing a CAD Toolkit to Run Under Windows; Developing FAX Communication Interfaces Under Windows; Creating Multifunction User Interfaces; Controlling Instruments Through Windows.

Above papers by: Chips and Technologies; Gebala Systems; Information Associates; QuickLogic; Logical Services; National Semiconductor; Phoenix Technologies; Stanford Resources.

TRACK II

- EXPANSION-BUS ISSUES -
EISA Add-on Card Design - Shaking the AT Mentality; System Design Issues for Intelligent EISA/MCA Cards; A RISC-based I/O Processor for PC Architectures; Increasing I/O Performance in PC Architectures; An Extended Local Bus Architecture for Better System Performance.

- HIGH-PERFORMANCE SYSTEM ISSUES -
Clock Distribution for High-Performance PCs; Care and Breeding of High-Speed Clocks; Applying System-Level Simulation When Designing ASIC Based PC Systems; Streamlining High-Speed System Design With Transmission Line Analysis; Computer-Aided Prototyping For Concurrent PC System Design.

Above papers by: Bull-Micral; Chips and Technologies; EliteGroup Computer Systems; Intel; Quantic Laboratories; QuickTurn Systems; Silicon Systems; Texas Instruments; VLSI Technology.

TRACK III

- NETWORKING -
Putting FDDI on a PC-AT Half-Card For Single Attachment Stations; Interface Ethernet to the EISA Bus; Customizing a LAN Controller For a Single-Chip Solution; Direct Bus Mastering in PCs Improves LAN Performance; Take Advantage of Specialty Memories When Building LAN Interfaces.

- DATA COMMUNICATIONS AND MASS STORAGE -
Employ Serial Packet Controllers for Flexible Protocol Control; Designing Appletalk-Compatible Serial Interfaces; Large Capacity Back-up Systems for Networked PCs/Workstations; Magnetic and Optical Drive Technology: Current Status and Future Directions; Flash Memory: The Optimal Technology for Solid-State Disks; SCSI RAID Subsystems for Redundant, High-Performance Mass Storage.

Above papers by: AMD; Intel; Integrated Device Technology; Maxtor; NCR; Plus Logic; PureData Research/USA; R-Byte; Silicon Systems; Zilog.

12:00 PM through 2:00 PM LUNCH AND EXHIBITS OPEN

- DISPLAY SUBSYSTEM DESIGN -
Local Bus Support for Video Systems; Selecting the Right Bus Interface for Video; Get High-Performance Graphics with Reprogrammable Logic; Developing Low-Cost Bus and Video Timing Control for Apple Macintoshes.

- I/O DEVICE DESIGN -
Reconfigurable Monitor Design Considerations; Designing High-Speed Control Logic With Reprogrammable Logic; Low-Cost Closed-Loop Controllers For Better Printer Accuracy; Designing Custom Keyboards and Interfaces; Evaluating and Testing Keyboards for PC Compatibility.

Above papers by: Cirrus Logic; Highgate Design; Hewlett Packard; HTE/HiTech Equipment; Oak Technologies; Micron Technology; NMB Technologies; Radius and Xilinx.

- APPLYING PROGRAMMABLE LOGIC -
Design Flexible Micro Channel Interfaces with Programmable Logic; Consolidating System Logic With PLDs; High-Density PLDs Simplify System Design; Apply FPGAs To Simplify Add-in Card Logic.

- EMBEDDED PCs FOR REAL-TIME SYSTEMS -
Real-Time Operating Systems for High-Performance Desktop PCs; Turning the PC into a Real-Time Machine; Using the PC/AT Architecture in Embedded Systems; Designing A Real-Time I/O Controller Card for the PC; Linking the Macintosh and VME environments for Real-Time Applications.

Above papers by: Actel; Altera; Ampro Computers; Intel; Lattice Semiconductor; Lynx Real Time Systems; Ready Systems; Nauchny Center, Moscow, USSR; YARC Systems Corp.

Technical Program subject to change

- MASS-STORAGE CONTROL -
SCSI Host Adapter Performance Trends - Using Intelligent OS Caches; Designing an Optimized SCSI Host Solution; Designing RISC-based Caching SCSI Disk Controllers; Tuning Storage Subsystem Drivers for Multi-Threaded Operating Systems.

- MASS STORAGE -
Optimization of I/O Subsystems in an EISA-Based File Server; Write Caching - New Drive Caching Schemes for Higher Performance; Applying the Power-Saving Modes Embedded in Low-Power IDE Disk Drives; System Compatibility Software Design for PCMCIA/JEIDA Memory Card Applications; PCMCIA System Interface Overview for Memory Cards.

Above papers by: Adaptec; Chips and Technologies; Databook; Intel; Interphase; Maxtor; Quantum; Storage Dimensions; VLSI Technology.

FOR MORE PROGRAM INFORMATION CONTACT: Dave Bursky, Chairman SVPC'91
Technical Program. Voice: 408/441-0550, Email: 76366.553@Compuserve.com

FOR EXHIBIT INFORMATION CONTACT: Ken Majithia, General Chairman SVPC'91
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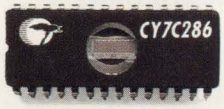

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In a battery-powered system, the worst situation usually is not knowing how much use time remains in the batteries that supply energy to the system. In the PC world, of course, there are chips that will perform some degree of power management by placing portions of the system on standby or shutting them off completely. But none of the logic thus far released actually manages the battery itself. That missing-management requirement is the gap that Benchmarq Microelectronics filled with its bq2001 energy-management unit, a biCMOS chip that provides an energy-gauge function, fast charge control, and sophisticated battery-system management services.

Although the chip is designed to fit into most personal computers, it can easily be tied into almost any microprocessor-based system, from test equipment to cellular telephones to smart battery packs. Power-management hardware in most portable PCs tries to reduce the batteries' load to extend the number of hours the system can be used. The bq2001, on the other hand, offers important services often requested by the system user.

For starters, the 24-lead circuit can determine the battery capacity and available charge. It also offers a fast-charge function so that the recharged battery can quickly return to service. And thanks to the power-management circuitry, the chip also maintains battery capacity at the highest-possible level for the greatest number of recharge cycles. In addition, 11 bytes of electrically erasable, nonvolatile storage enable the chip to store basic battery characteristics. These can be used to provide the initialization values for the system, but can be overridden or rewritten if system characteristics change. Smart battery packs could extensively use the nonvolatile storage to transfer battery characteristics to a host system's controller.

The chip can operate as a standalone controller when powered directly from a system's dc-charging supply, or as a microprocessor peripheral when it uses the system's 5-V logic supply. Multiple system aspects are monitored continuously by the chip's mixed-signal circuitry, including temperature, battery voltage level, energy usage, backup battery condition, and others *(see the figure)*. An on-chip "gas-gauge" register holds the actual charge consumption from the secondary battery and measures the actual battery capacity. With a charge-time register, the energy stored after partial or com-

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BATTERY-MANAGEMENT CONTROLLER

plete recharge can be calculated.

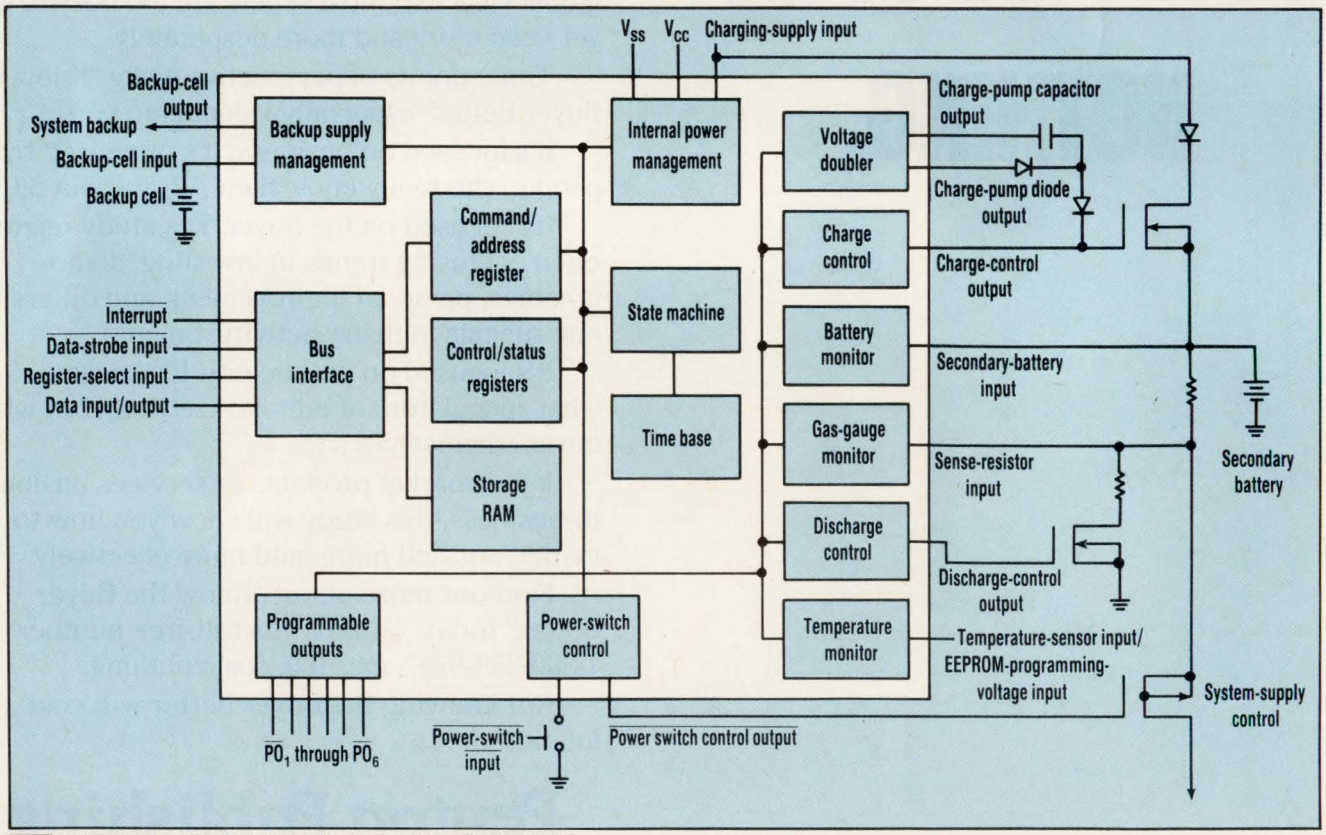
The designer can preselect and set the end-of-discharge voltage (EDV) to suit battery type. The EDV level indicates the deepest discharge point that the designer or battery maker permits to indicate full discharge. In many applications, designers may want to sequentially program multiple EDV thresholds. The first could be used as an early warning. If the battery end-of-discharge roll-off is gradual enough, there will often be a second final warning. The third, and perhaps final EDV threshold, will be the stimulus for the system to shut itself down.

When the dc or battery source is turned on, the gas gauge provides the real measurement of the second battery's charge by metering the current from that battery. As the charge is transferred, the contents of the gas gauge's register are incremented. The gauge is reset by a full recharge, an abort command, or by battery removal. A charge-time register is also part of the monitoring logic. It helps the system determine the amount of charge put into the battery. The register counts the time that a charge phase is enabled in 8-minute intervals. It resets to zero each time a charge phase begins, or when the battery is removed.

The battery discharge rate is monitored by measuring the voltage drop across a sense resistor that's connected across the chip's Sense Resistor Input and Secondary Battery Input pins. The resistor is chosen by fitting it to the system battery-discharge-rate profile. The readings are most accurate (less than 2% relative measurement error) if the sense-resistor voltage drop can be kept between 30 and 170 mV.

Battery management includes charge-control circuits that let the batteries be replenished at standard to fast-charge rates. The full charge is determined by using a negative delta-voltage calculation scheme, a maximum-voltage threshold, and a maximum time limit. The bq2001 can also be configured to inhibit or terminate charging when the battery temperature is outside an acceptable range. Trickle-charge control begins after full charge is determined. Nonoperational discharge before charge can be set up for cell conditioning or capacity measurements. Charge patterns can be programmed to be constant, pulsed, or "burped" (alternating charge discharge) to suit the battery system.

Monitoring provides details of the battery's complete state—fully charged, partially charged, removed/replaced, or faulty. The monitor also reports on the available battery charge by precisely measuring the discharge current over time, and allows the system's firmware to compute the partial charge replacement, and determining the full charge. Finally, the circuit collects the information necessary for the system firmware to recalculate capacity each time the battery goes



BATTERY-MANAGEMENT AND CONTROL are possible from the single-chip bq2001. The device monitors energy consumption and lets designers implement a "gas gauge" reading of available battery usage. Other portions of the chip control battery charge time and can control various subsystems or provide status indicators.

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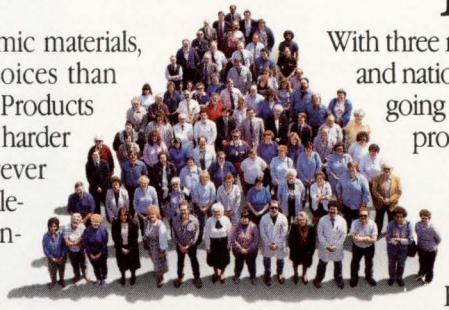

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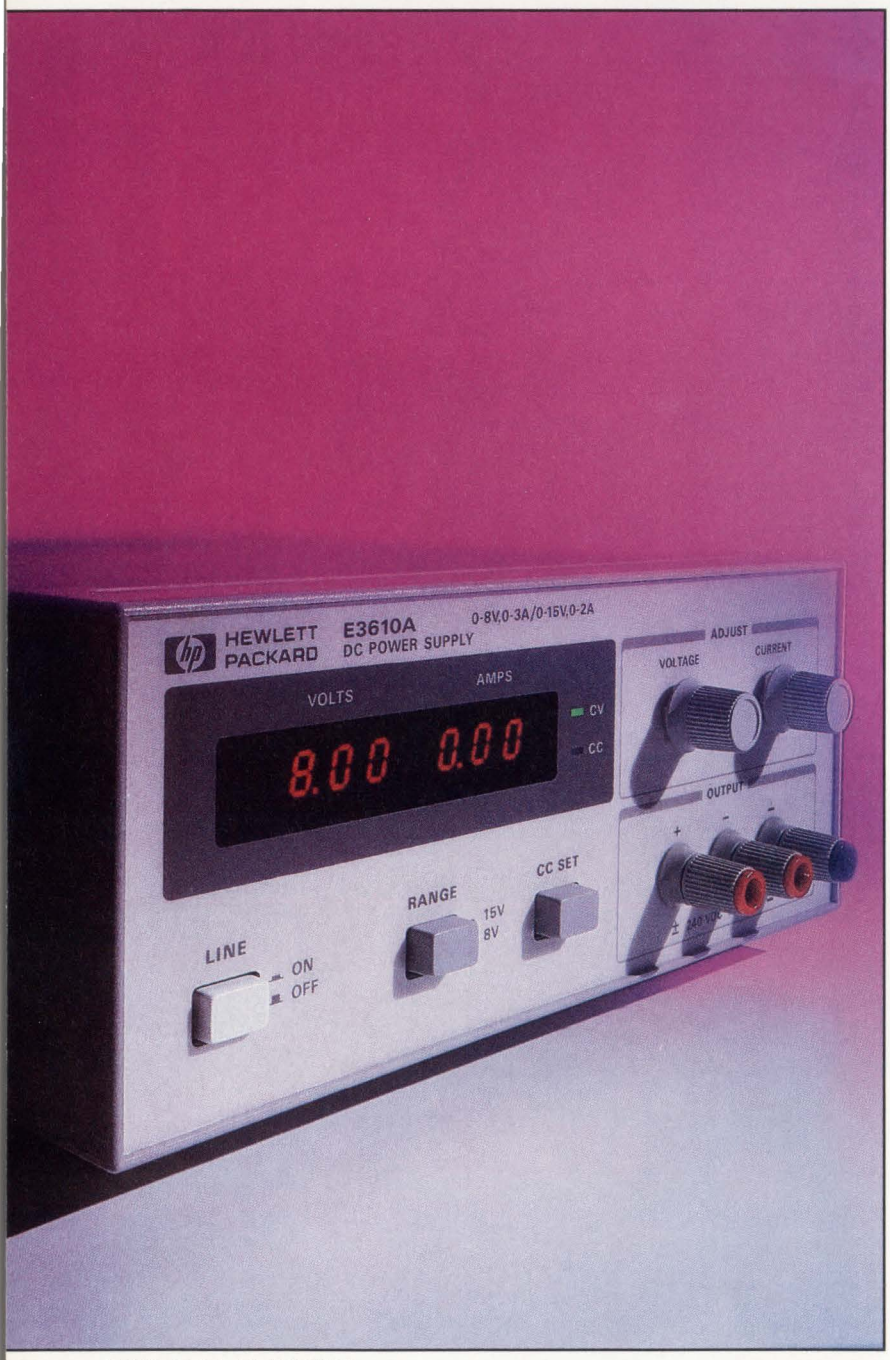

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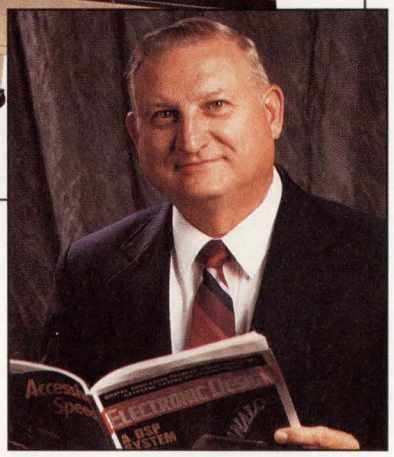

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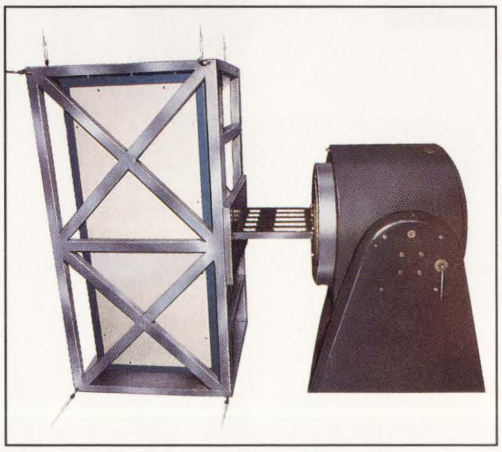

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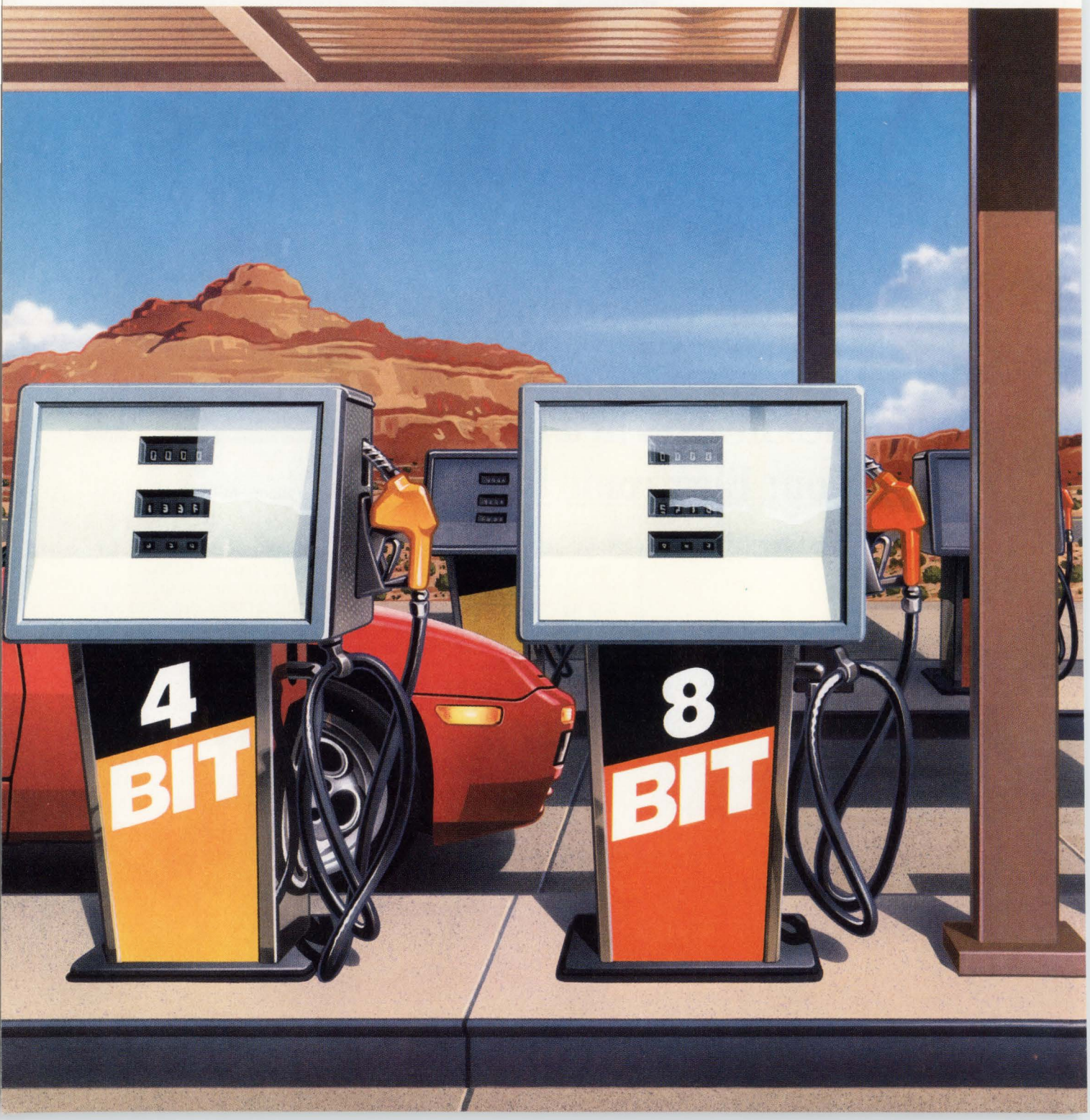

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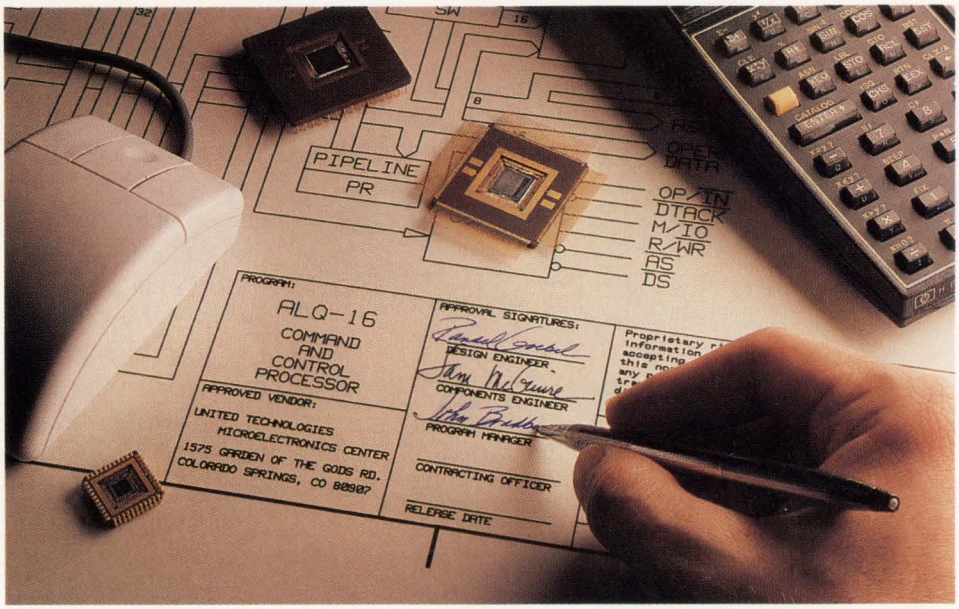

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CIRCLE 149

BATTERY-MANAGEMENT CONTROLLER

from full to empty. The chip collects the Last Capacity register value and the charge-time values and can store a time stamp that can help the system determine self discharge. Diagnostic tests are also performed transparently by the chip in the background, permitting the system to maximize battery life. By prolonging battery life, the chip could also contribute indirectly to a better environment by reducing the number of batteries disposed of each year.

The controller chip can work with battery stacks that have nominal voltages of 4.8 through about 12 V and are implemented with nickel-cadmium, lead-acid, or the new nickel/metal-hydride chemistries. Input voltages to the controller can span from 5.5 to 18 V dc when the chip runs from the recharging supply, and between 4.5 and 5.5 V when powered by the system's nominal 5-V supply. When power is off, the bq2001 regulates the secondary battery input to maintain its programmed state as it sources a backup cell output to maintain a real-time clock or other low-current battery-backed ICs. The backup cell (2 to 6 V) provides system-data-retention current when the secondary battery is depleted or removed. When the system's main power is removed, a small lithium cell is all that's needed for the chip to retain its configuration data—just 100 nA, typical, are consumed by the chip.

There are six open-drain control outputs that can be controlled by the on-chip logic or by an off-chip host processor. The outputs can be allocated for subsystem control, LED activation, status indication, or system power-switching control. A simple three-wire serial interface ties the bq2001 to any host processor—Intel or Motorola microprocessors or microcontrollers for example. The interface, however, is only active when the system supply level is valid. The interface uses command bytes (written to the chip's command register). Those bytes direct the access to 18 bytes that are used for control and status, and to 32 data bytes provided for nonvolatile storage of programmer-defined information.□

PRICE AND AVAILABILTY

The bq2001 energy-management unit comes in a 24-pin 300-mil DIP or a 24-lead small-outline package. In lots of 1000, the SOIC version sells for $11.50 each, while the DIP version comes in at $10 each. Delivery is from stock.

Benchmarq Microelectronics Inc., 2611 Westgrove Dr., Ste. 101, Carrollton, TX 75006; John Landau, (214) 407-0011.

CIRCLE 512

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MODERATELY	544
SLIGHTLY	545

Some Notes About Digital Audio DACs

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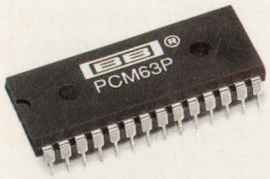
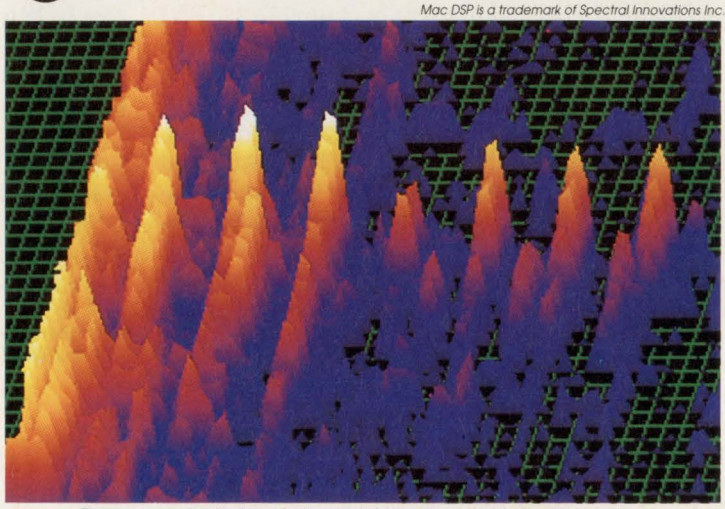
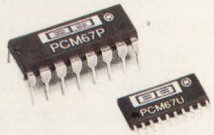




Three seconds of a horn instrumental from a score of classical music.



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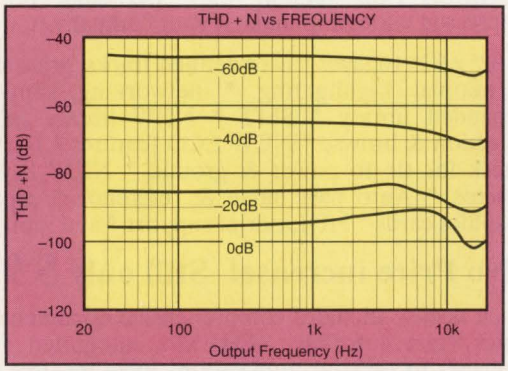
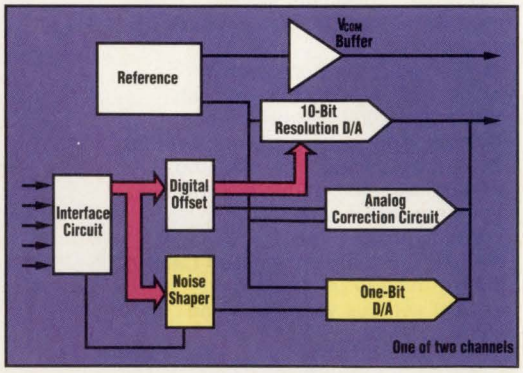
SPECIFICATIONS	PCM63	PCM67
Resolution	20-bits	18-bits
THD+N, Max	–96dB	–92dB
SNR, Min	116dB	110dB
Dynamic Range	108dB	108dB
Gain Error	±1%	±3%
Power Dissipation	225mW	75mW
Oversampling	16X	8X
Channels	Single	Dual
Price*	$12.23	$13.97

PCM63's ultra-low distortion over the audio bandwidth.▼



PCM67 features the best of multibit and one-bit designs. ▼



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CIRCLE 91

SCOPES COMBINE DIGITAL POWER WITH EASE OF USE

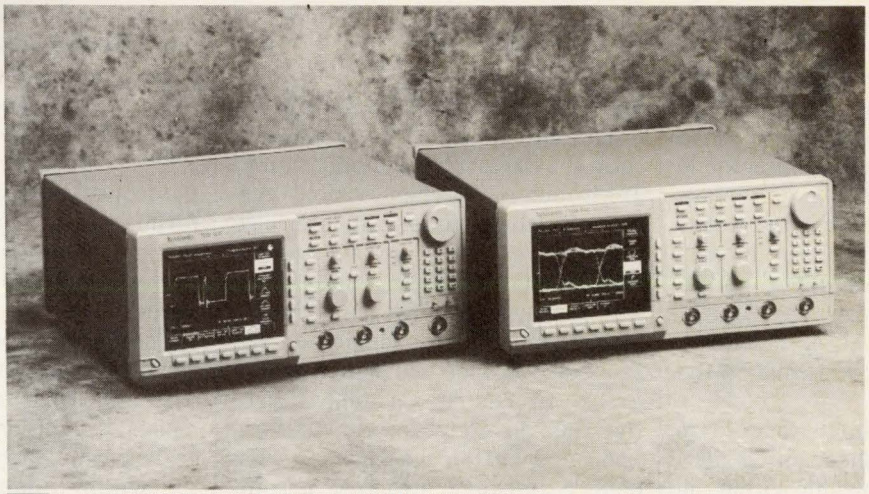
A GRAPHICAL INTERFACE BASED ON A VGA DISPLAY SPEEDS THE LEARNING CURVE FOR TWO POWERFUL MID-RANGE DSOS.

JOHN NOVELLINO

With all of the powerful features and functions added to digital oscilloscopes in recent years, it may be easy to overlook one very important attribute: ease of use. Learning to fish through multilevel menus can be a chore for designers debugging their latest handiwork. Especially frustrating is relearning the scope after several weeks or months away from the bench.

To ease this chore and combat the frustration, Tektronix included an intuitive graphical interface in a pair of full-featured, mid-range digital scopes that introduce the new Tektronix Digitizing Scope (TDS) platform. The importance of the graphical interface is evident in the 640-by-480 VGA display in the TDS 520 and TDS 540 *(Fig. 1)*. But the instruments don't neglect performance issues. A high-speed acquisition system, advanced triggering, and multiprocessor architecture see to that.

The scopes feature a 500-MHz bandwidth, 8-bit vertical resolution, 1% accuracy, and 4-ns glitch capture. The TDS 520 digitizes signals at 250 Msam-



1. FAMILIAR FRONT-PANEL KNOBS and buttons make even infrequent users feel comfortable with the 2-channel TDS 520 (left) and 4-channel TDS 540 (right). The scopes are 500-MHz units with digitizing rates as high as 1 Gsamples/s.

ples/s on two channels or 500 Msamples/s on one channel. The TDS 540 samples from 250 Msamples/s on four channels to 1 Gsamples/s on one channel. A variable record length of 500 to 15,000 samples/channel is standard, with 50,000 samples/channel optional. The TDS units include the fast-overdrive recovery, wide dynamic range, calibrated dc offset, and variable-gain capability found on Tektronix's more-expensive 11000 Series laboratory scopes and DSA 600 digitizing signal analyzers.

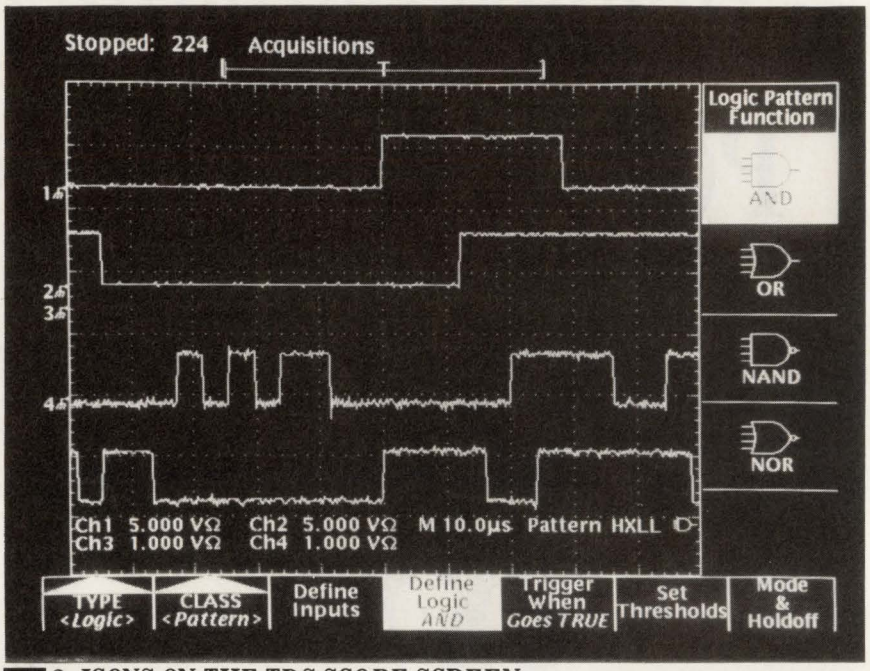
Multiple Triggers

The TDS Series' wide-ranging triggering includes more than 10 functions. Time interval, runt-pulse, and glitch functions help find and characterize transients, anomalies in logic signals, and random glitches. For complex digital designs, the scopes' time-qualified logic, pattern, and state trigger modes—combined with multichannel operation—can reduce the engineer's reliance on logic analyzers.

Moreover, trigger-conditioning circuitry ensures stable triggering when dealing with complex waveforms. Besides the traditional ac and dc coupling, the scopes offer noise-reject, high-frequency reject, and low-frequency reject coupling. The noise and high-frequency rejection circuit filter out unwanted transitions that can cause ambiguous triggers. The low-frequency rejection eliminates low-end signals, like a 60-Hz power-line component, so the scope can trigger on the input's high-frequency components.

Selecting the desired trigger mode is simplified by the iconic interface and high-resolution display. Icons also represent acquisition modes, measurements, and setup conditions. To avoid clutter, the figures are grouped in logical combinations, with no more than five icons on the screen at once.

The icons are distinctive enough to be easily distinguished, but related enough to be recognizable within the groups. Each is named on screen so the user need not memorize them *(Fig. 2)*.



2. ICONS ON THE TDS SCOPE SCREEN make it easy to choose the desired trigger function, as well as acquisition modes, measurements, and set ups. The gates shown on this TDS 540 screen indicate that all four channels can be used as inputs to the desired logic function.

The front panel is also designed to give the user interface a convenient look and feel. Knobs and buttons are arranged in six groups. The familiar vertical, horizontal, and trigger controls are in their conventional locations. Other groups include controls for extended-function menus, screen menus, and numerical entry. If any questions remain in the user's mind, pushing the Help button will bring up the on-line HelpText screen for the selected control.

Listen To The Customer

The interface was designed with the aid of extensive customer input. Tektronix researchers visited customer facilities not only to interview prospective users, but also to observe them and their work habits. The researchers even noted habits like sticking Post-it memos on the scope or marking the screen with a grease pencil. The customers were the final arbiters for icon design, knob and button placement, terminology, and menu structure, according to Tektronix.

For instance, one request implemented in the design is that all of the basic functions needed to acquire and adjust the waveform be immediately accessible from the front panel without going through menus. Also, multiple versions of each icon were put on "flash cards" and shown to customers, who then decided exactly which icons were the most representative images.

A key element of the interface is the TDS Series' high-display resolution and rapid update rate. Both are the result of a proprietary high-performance graphics engine that's part of the scopes' multiprocessor architecture. The three independent processors prevent degradation of the scopes' primary function—waveform acquisition and display—while the instrument is being called on to perform one its many peripheral tasks.

The display processor supplies live waveform data while it reformats data and drives specialized display modes. In addition, the 4-bit intensity scale permits gray-scale coding of the acquired data, which helps the user pick out anomalies in the incoming waveform.

A 16-MHz Motorola 68020 micro-

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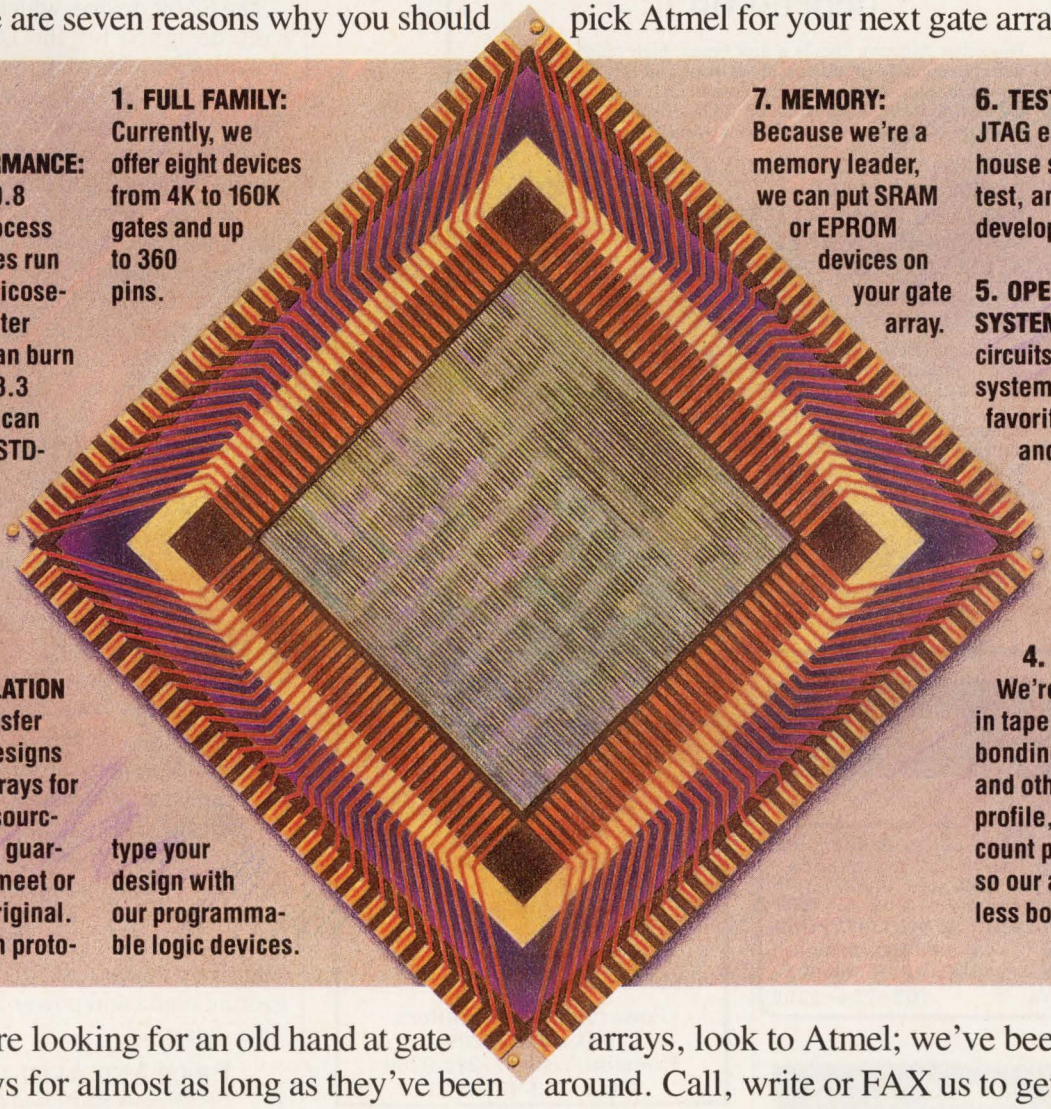

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CIRCLE 162

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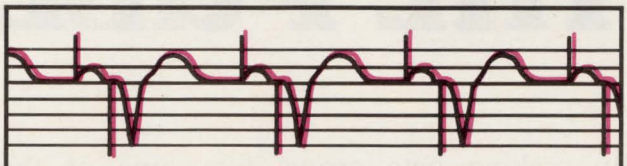

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EASY-TO-USE DIGITAL STORAGE SCOPES

processor handles the user interface and I/O ports, and optimizes data flow within the scope. The instrument's third processor, Tektronix's TriStar digital-signal-processing IC, performs various compute-intensive tasks, such as digital filtering, signal averaging, interpolation, pass-fail decisions, and complex-waveform calculations.

The 32-bit device, which was originally designed for the DSA 600 series, also handles all waveform data. The TriStar's 5-MIPS speed ensures that the scopes can efficiently handle the large volume of data acquired by the high-speed digitizers.

The TDS scopes also feature a high-resolution mode that improves vertical resolution by up to 4 bits on transient events. Because the digitizers always operate at full speed, they produce many data points not used in the display when the unit is operating at less than maximum sweep speed. These points are usually discarded.

In the high-resolution mode, however, a block-averaging algorithm averages all of the extra points, effectively smoothing the waveform on-the-fly. The averaging filters out high-frequency noise and visually simplifies single-shot events. This feature differs from the conventional averaging, which is performed over multiple acquisitions. The TriStar processor performs this function for repetitive signals.

Finally, the scopes are built with surface-mount technology, using both sides of the boards for device placement; this gives better isolation, allowing the use of a continuous ground plane and power plane in the same board.□

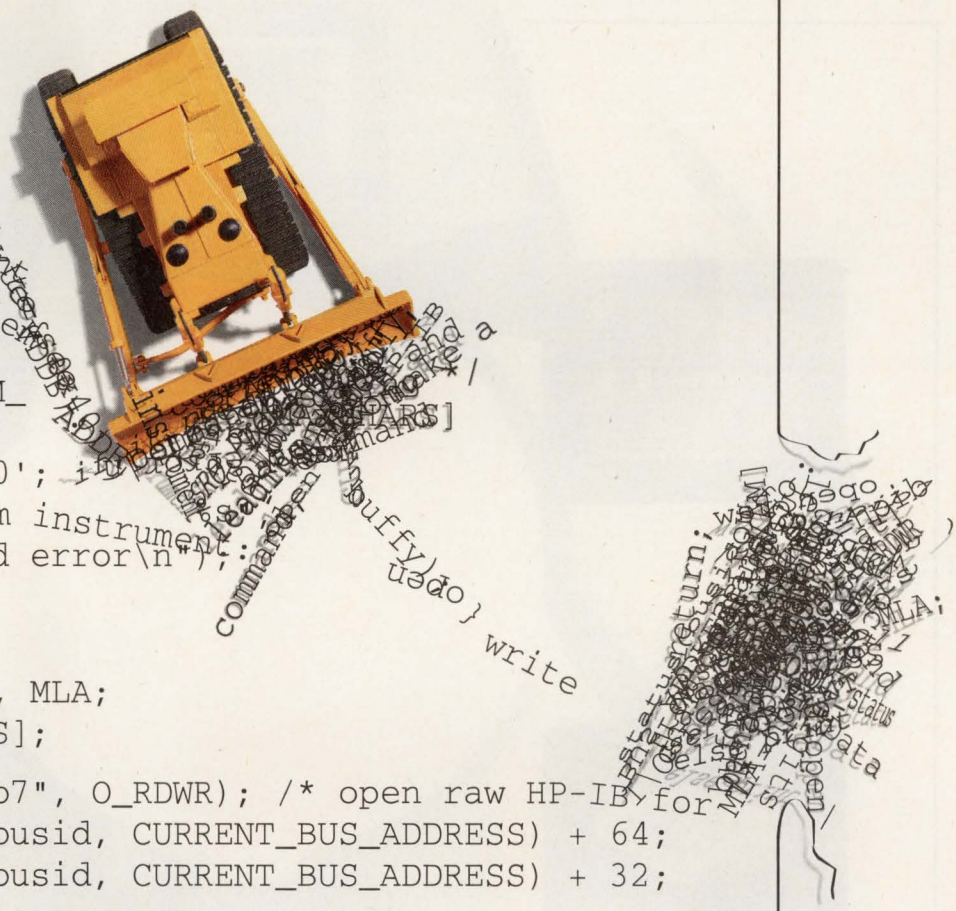
PRICE AND AVAILABILTY

The TDS 520 costs $9490, and the TDS 540 is priced at $13,900, with delivery within 6 weeks. Option 1M, which increases record length to 50-ksamples per channel, is $1500 for the TDS 520 and $1950 for the TDS 540.

Tektronix Inc., P.O. Box 19638, Portland, OR 97219-0638; (800) 426-2200. **CIRCLE 513**

HOW VALUABLE?	CIRCLE
HIGHLY	547
MODERATELY	548
SLIGHTLY	549

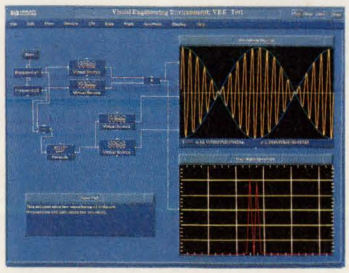
Finally, engineering software that clears the way to problem solving without programming.



```
void service(eid)
int eid;
{ int stat, byte;
/*serial poll instrument
byte=hpib_spoll(eid);
if ( (byte<0)||! (b
    printf("SRQ Prob
   return; }
stat=my_read(eid, DVM_
if (stat>0) {
    buffy[stat] = '\0';
    printf("Data from instrument:
else printf("I/O read error\n");
return; }

main() {
int busid, stat, MTA, MLA;
char command[MAXCHARS];

busid=open("/dev/hpib7", O_RDWR); /* open raw HP-IB for
MTA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
MLA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
stat = BUTTON_BIT ;
sprintf(command, "KM%02o", stat); /* 2 octal digits */
```



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There are two HP VEE software packages for prototyping, experimentation, and problem modeling. HP VEE-Engine, at $995*, is a general-purpose tool for analysis and presentation of existing data. HP VEE-Test includes HP VEE-Engine and adds extensive I/O capability, including soft panels and device I/O objects for $5,000*.

So, if programming is keeping you from finding solutions, call **1-800-752-0900.** Ask for **Ext. 2382**, and find out how HP VEE clears the way.

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HEWLETT PACKARD

CIRCLE 163

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CIRCLE 125

IN-SYSTEM PROGRAMMABLE LOGIC KEEPS DELAYS SHORT

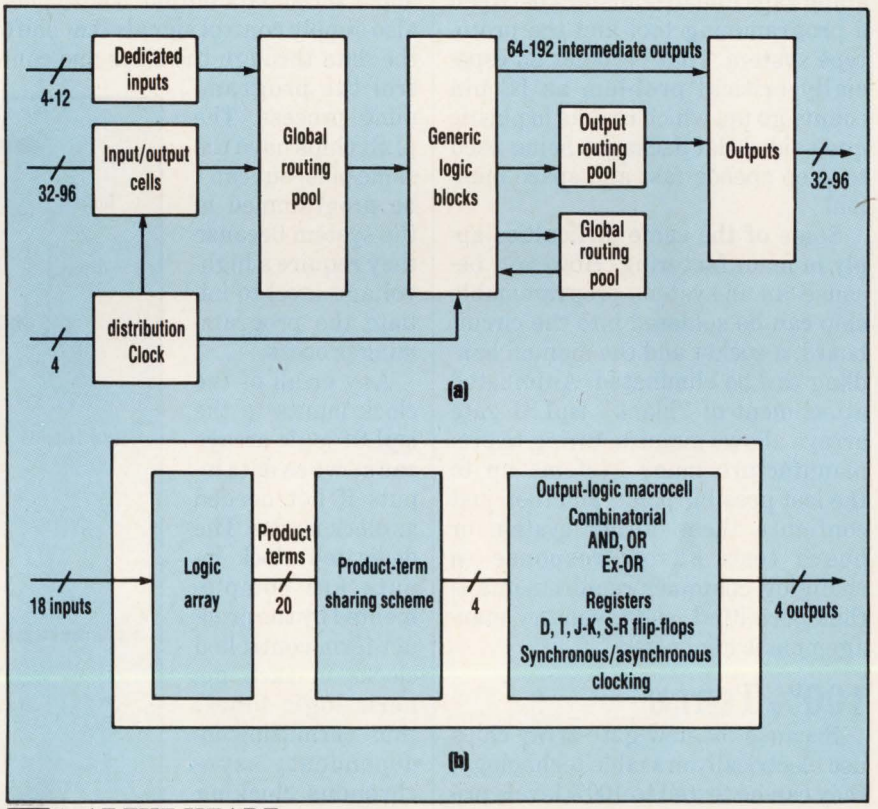
BY MERGING EEPROM CELLS AND 5-V-ONLY OPERATION, AN FPGA FAMILY DELIVERS DENSE, FAST LOGIC.

DAVE BURSKY

Field - programmable gate arrays have already made an impact on designers needing an instant solution for logic blocks with gate counts approaching several thousand gates. However, except for RAM-based FPGAs, which must be loaded with their configuration data each time the system powers up, all current alternatives can't be reconfigured in a system that's being upgraded or fixed. Lattice Semiconductor now expects to fill this reconfiguration gap with a family of in-system programmable large-scale-integration (ispLSI) logic arrays. The logic arrays can be programmed with just a single 5-V external power supply.

The ispLSI chips are based on the company's well-established 0.8-μm CMOS EEPROM technology employed on its high-speed GAL programmable-logic devices. The chips will be able to run at system speeds up to 70 MHz, and will have an input-to-output propagation delay (including I/O buffers) of just 15 ns through one logic level. Furthermore, the submicron process will let the chips contain 2000 to 8000 equivalent PLD gates, and have 32 to 96 I/O lead counts.

Actual device pin counts, including power and ground leads, boost the pin count of the ispLSI logic arrays by 12 to 16 leads. A proprietary routing network provides global interconnectivity over the chip with 100% routability, and achieves over 80% device utilization. If in-system programmability isn't needed, a second family of four architecturally equivalent devices—the pLSI series—provides the same logic functions but requires a PROM program-



1. AT THE HEART of the pLSI and ispLSI logic chips lie the global routing pool and multiple generic logic blocks (a). These sections are in turn connected to output routing pools of additional interconnections and the I/O cells. Each generic logic block contains a logic array that produces 20 product terms from 18 signal inputs. A section within the generic logic block allocates, in any ratio, the 20 product terms among the four output logic macrocells. The OLMCs, in turn, provide the combinatorial or registered outputs (b).

mer for configuration.

In-system EEPROM-based programmable parts, as first released by Lattice Semiconductor even before the RAM-based logic arrays from Xilinx made their debut on the market, gave the designer and the manufacturing team many benefits. However, the low logic complexity of the initial ispGAL PLDs didn't match system designers' needs, and it didn't make significant inroads. The latest offerings, though, give designers enough logic to implement significant portions of a system on just a single chip.

In-System Flexibility

Designers can benefit from the programmability of the new logic arrays because it allows them to revise the patterns right in the system they're trying to develop. This flexibility eliminates the possible headaches associated with bent pins and static zaps due to transfers between a programming tool and the prototype system. That becomes an especially critical problem as IC pin counts go up, which results in plastic quad-sided flat packages being used to keep speeds fast and space minimal.

Some of the same difficulties apply in manufacturing. However, because an in-system programmable chip can be soldered into the circuit board, a socket and the manual handling can be eliminated. Automated attachment of "blank" ispLSI gate arrays allows manufacturing to premanufacture many systems up to the last possible point, and then just configure them during system or board test. Faster response to changing customer requirements is thus permitted, and inventory management is minimized.

100% Testing

Because the new gate-array chips use electrically erasable technology, they can be tested to 100% levels prior to being attached to the pc board, ensuring that only good devices are soldered in place. Reconfigurability is also a key benefit to the system designer.

Once a system is shipped, the cost of servicing it to upgrade a board or fix a flaw is often orders-of-magnitude more than the cost of the new hardware. With the ispLSI gate-array chips, the system manufacturer's service department need only transfer a new software patch (which can be performed via a modem or on floppy disk drive, for example) that can be downloaded into the logic chips.

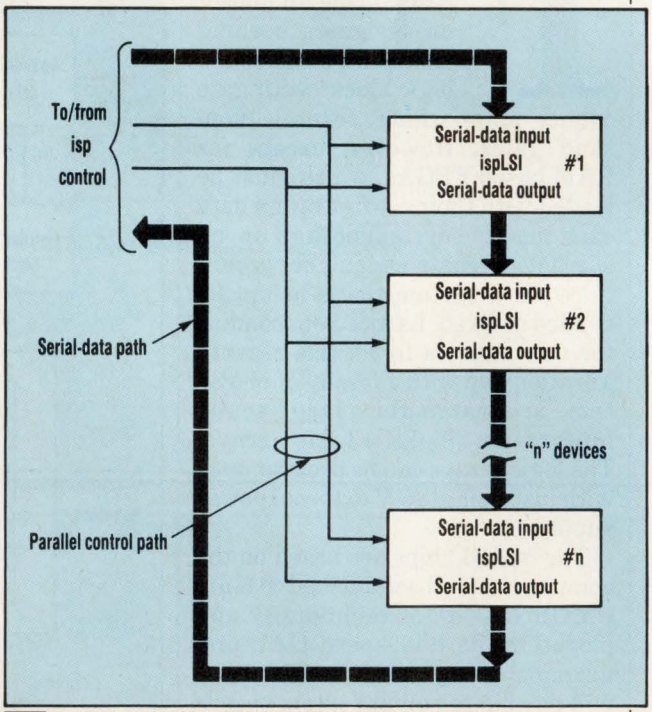
The logic structure of the ispLSI or pLSI chips consists of a core array of generic logic blocks and a global routing pool *(Fig. 1a)*. Closer to the periphery of the chip are output-routing resources called the output routing pool.

All of the logic resources are surrounded by dedicated input cells and bidirectional I/O cells, as well as a clock distribution block that handles 3 or 4 external clock inputs. A set of dedicated pins on the ispLSI logic-array chips provides a serial-data input and a serial-data output. Those pins also supply control signals that shift the data through the chips and control the programming process. The pLSI chips have the same pins, but can't be programmed in the system because they require a high-voltage level to initiate the programming process.

Any or all of the clock inputs to the ispLSI logic arrays can serve as data inputs if not needed as clock inputs. The dedicated clock inputs are complemented by the product-term-controlled clocks in each generic logic block, thus permitting independent, asynchronous clocking of each generic logic block. Data from dedicated inputs, the I/O cells, and every other generic logic block is available to any generic logic block through the global routing pool.

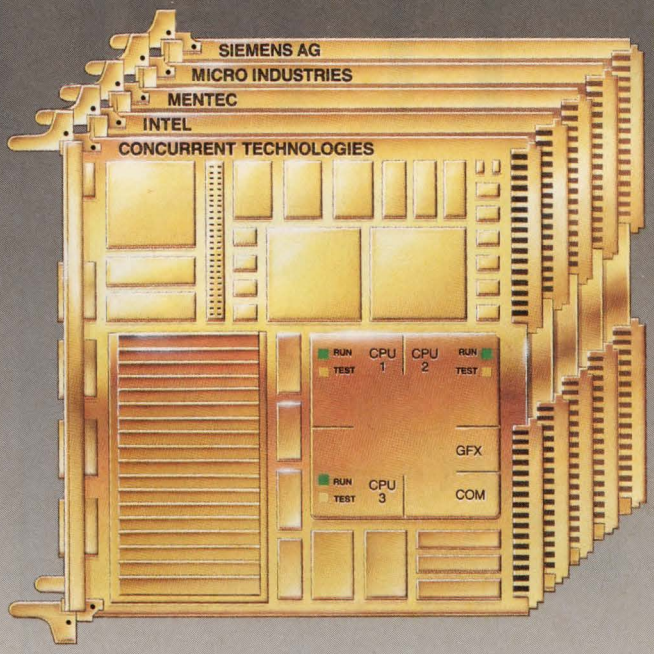
Over 90% of all 4-bit MSI-type logic functions can be implemented with one generic logic block, thanks to all of the product term and logic resources. That further improves system performance and minimizes the overhead of using routing and interconnection resources for multiple-level logic functions. Of course, multiple generic logic blocks can be cascaded by routing the output of one through the global resource pool back to the input of another generic logic block.

Each generic logic block (16 to 48 per chip) consists of a logic array that generates 20 product terms from 18 inputs and a product-term sharing scheme. The scheme, with minimal delay, distributes the product terms as needed across four output-logic macrocells (OLMCs) that are also part of the generic logic block *(Fig. 1b)*. Each OLMC produces an output; two of the outputs are fed to the output routing pool



2. BY DAISY-CHAINING MULTIPLE ispLSI arrays together, a serial loop can be formed. This allows designers to load configuration data into one or more chips, or test the devices in the loop to ensure system integrity. Just two lines are needed for control, in addition to the serial-data input and serial-data output lines.

Live Long.



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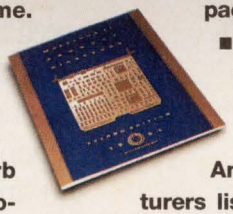

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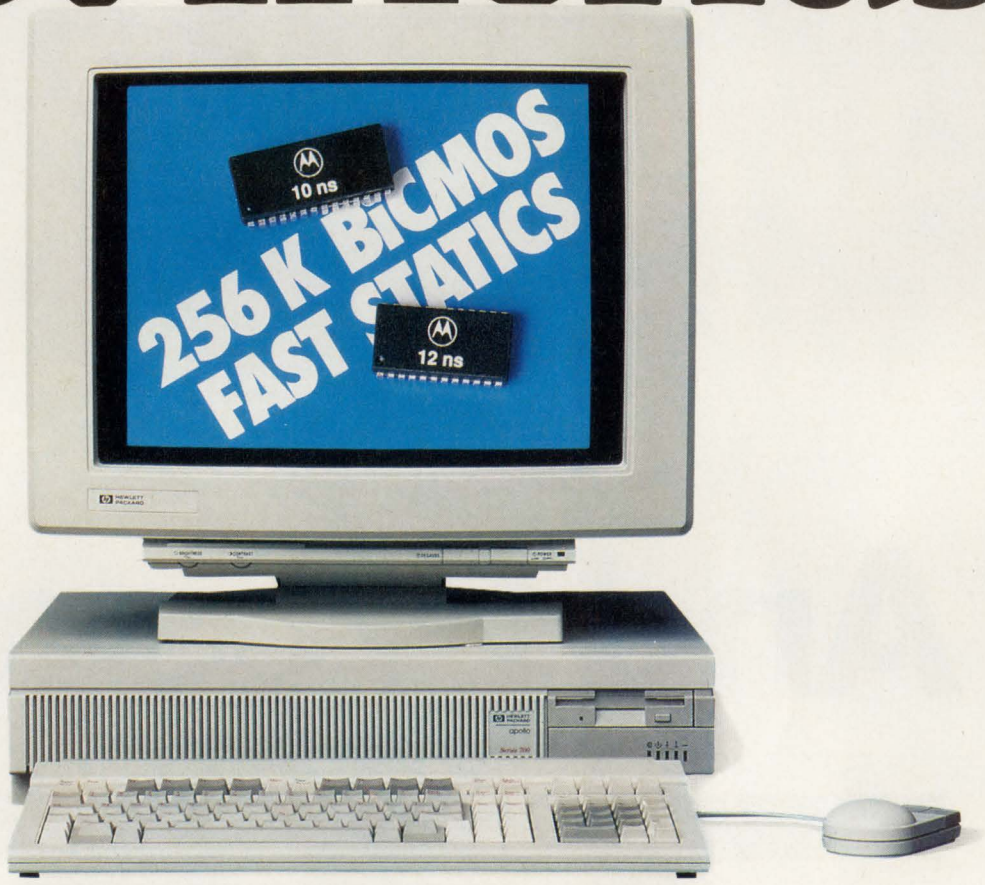

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MOTOROLA

and the other two are fed to the global routing pool. Each of the four outputs can be a registered or combinatorial type. The OLMC performs combinatorial functions, such as AND, OR, Ex-OR, and other operations. It also contains four registers (one associated with each output) that can be configured at D, T, J-K, or S-R type flip-flops. Clocking on the registers can be asynchronous or synchronous.

Statistically designed to provide routing for almost every possible design, the global routing pool allows performance to be maximized while minimizing the derating for logic implementations. The output routing pool serves as the gateway between a group of 16 I/O cells and 8 adjacent generic logic blocks. The routing matrix contains a programmable multiplexer, as well as a set of dedicated high-speed interconnections for critical signal paths. Relatively small in size, this routing matrix makes the performance very predictable and fast, regardless of the type of routing selected.

Each I/O cell obtains its output data from the output routing pool or an adjacent generic logic block. Input data comes from an input register that can be configured in a registered or latched state, with control coming from one of the two common I/O clocks. Input data from an I/O cell is available to all the generic logic blocks through the global routing pool.

The first of the new logic-array chips to appear from Lattice Semiconductor will be the pLSI32 and ispLSI32. They'll contain 32 generic logic blocks, 64 I/O pins, 8 dedicated inputs, and a total of 192 registers (1 in each I/O cell and 4 in each generic logic block).

By using the serial-data input (SDI) and serial-data output (SDO) lines, multiple ispLSI logic-array chips can be cascaded for configuration or test purposes (pLSI logic arrays for testing as well). The daisy-chaining can be done by simply connecting the SDO of the first device to the SDI of the second, and so on. A parallel two-wire control path tells the chips what to do *(Fig. 2)*.

The patterns of the ispLSI logic-array chips in the programming loop can be changed individually, or all together, at the same time. The reprogramming time is short, taking less than 2 seconds, regardless of the number of chips that are in the loop.

False programming and erasures are prevented by a dedicated Program/Normal Operation control input, as well as safeguards in the programming algorithm. Furthermore, an electronic signature is available and can be examined when using the serial loop. The signature is controlled by the designer, and is part of the JEDEC design file. It usually holds the device identification and a pattern-revision value.

Support Tools

A variety of easy-to-use supporting design tools are available for use with the ispLSI and pLSI logic-array chips. These include PC-based entry-level tools with Boolean and Macro inputs, functional-level simulation, and automatic-place-and-route capability.

More complete design-tool packages that run on PCs or workstations include schematic capture, Macrocell libraries, automatic place and route, and logic and timing simulation. Programming tools from many established suppliers—Data I/O, Logical Devices, Stag, System General, SMS Micro, and Advin Systems, for example—will also be available.□

Price And Availabilty

Samples of the pLSI32 will be ready in the mid-to-late third quarter, with the ispLSI32 expected to follow about one-quarter behind. Additional devices will be released in 1992. Beta versions of the software will also be released in the third quarter. A full-market release will take place in the fourth quarter of this year. In lots of 100, the pLSI32 sells for $98.50 apiece.

Lattice Semiconductor Corp., 5555 N.E. Moore Ct., Hillsboro, OR 97124; Dean Suhr, (503) 681-0118. **CIRCLE 514**

How Valuable?	Circle
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Slightly	551

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SIMULATOR HANDLES ANALOG DESIGNS WITH OVER 50,000 TRANSISTORS

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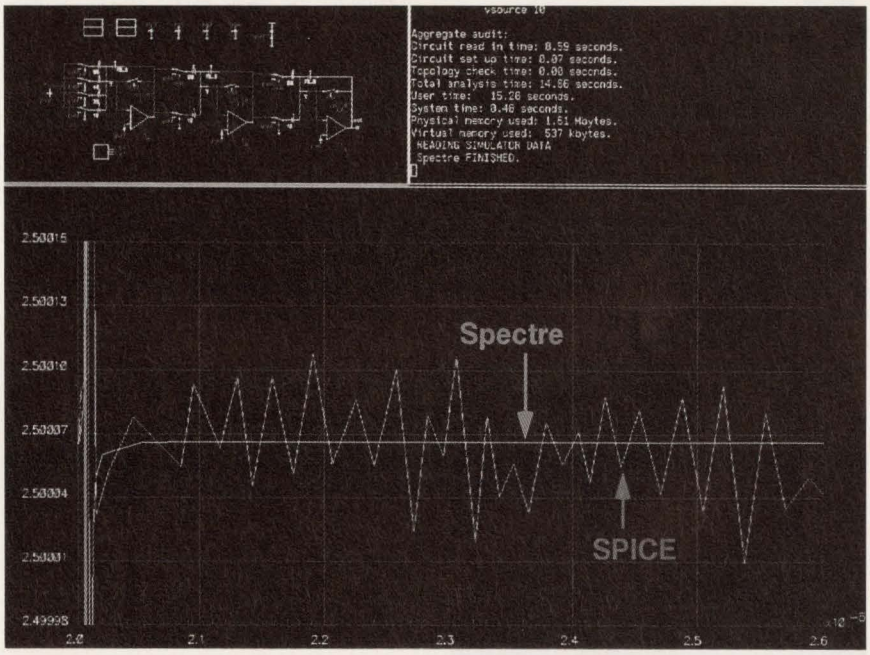


Designers of analog circuits primarily have one option for analog simulation: They can use Spice or Spice derivatives. With Spice, however, simulating analog designs with over 50,000 transistors is nearly impossible. Now another choice called Spectre has arrived on the scene.

The Spectre analog simulator from Cadence Design Systems Inc. is not based on Spice. It can handle complex ICs with up to 10 times the speed of Spice. And it can do so with equal or better accuracy than Spice can provide. Moreover, Spectre power isn't limited by the size of the design being simulated, but rather by the computing resources that are available.

The Spectre software is the culmination of a cooperative effort with university researchers and Cadence Analog Alliance Partners, a Cadence program formed to advance analog technology. Spectre, which will be available within Cadence's Analog Artist Design System, was designed from scratch with a modular architecture in mind. It's written in the C programming language and employs innovations in numerical algorithms that yield faster and more accurate simulations.

Spectre simulates large analog circuits through the use of advanced sparse-matrix techniques and node-based algorithms. It has more robust convergence than Spice simulators. For example, new algorithms employed in Spectre ensure convergence of the Newton-Raphson algorithm in dc analysis. In fact, the Microelectronics Center of North Carolina simulated 65 representative circuits to show that Spectre converged for every circuit, while Spice-based products converged for only 40% of the simulations.

Spectre algorithms also avoid known Spice problems, such as very-small time steps, due to piecewise-linear waveforms with many time points or many transmission lines. Memory-efficient data structures and dynamic re-dimensioning of arrays contribute to the simulator's overall performance. In addition, built-in intelligence algorithms warn users of circuit errors and invalid-model operating regions.

Analog and digital circuits are simulated at the differential-equation level using direct methods. Circuits can contain such elements as microstrip lines, independent voltage and current sources, and voltage- and current-controlled sources.

Unlike Spice-based simulators, Spectre includes a compiled user-defined model capability that makes it possible for CAD developers or designers to add and utilize proprietary models within the simulator. Users incorporate the models, which are written in C, through an interface. Spectre concentrates all model code into one module.

Spectre uses nonlinear device models. These models are built-in so that users need only specify pertinent model parameters. They're the same models employed for Spice simulations. Model equations aren't based on capacitance, as is the case with the Spice models, but are instead based on charge.

The bipolar-junction-transistor model is based on the integral-charge model developed by Gummel and Poon. The diode model may be used for either junction diodes or Schottky barrier diodes, and includes reverse-breakdown effects. In addition, there are no model discontinuities to contend with.

Spectre is compatible with Spice-based simulators, including the company's Cadence-Spice. In addition, Spectre accepts standard Spice input files and analyses. Consequently, Spice users will be able to use Spectre with no change in design methodology. Cadence's Analog Artist simulation environment supports simple and rapid switching between Spectre and Spice-based simulators.

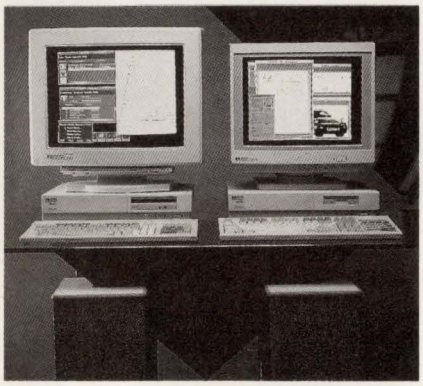
Pricing for the Spectre Advanced Circuit Simulator starts at $30,000 for a single-user license. The simulator is also available in an integrated version within Cadence's Analog Artist Design System running under the Cadence Design Framework architecture.

Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234. **CIRCLE 300**

WORKSTATION PERFORMANCE COMES AT PC PRICE

On the heels of HP's Series 700 workstation announcement (ELECTRONIC DESIGN, *Mar. 28, p. 132)*, the company has added a new member to its Motorola-processor-based Series 400 line. The model 425e incorporates a 68040 processor running at 25 MHz. HP says this system is appropriate for all markets, including commercial, CASE, data-transaction processing, and entry-level CAD. The company also contends that this platform could be an alternative to a high-end PC.

The Unix-based 425e is built in a compact desktop package. It has a performance rating of 22 MIPS and 11 SPECmarks. The system holds 8 to 48 Mbytes of main memory. And there's room for 840 Mbytes of internal disk storage. The 425e has the capabilities for digital audio and an internal CD-ROM drive. Prices start at $5490 for a diskless unit with a 1280-by-1024-pixel gray-scale 19-in. monitor and 8 Mbytes of RAM. A 16- or 19-in. color monitor is also available.



A second offering from HP is the SharedX X-Windows enhancement product. With SharedX, users can open windows on X terminals at multiple locations. What differentiates SharedX from other communications products is that the secondary user, not just the primary user, can manipulate the data in the window. This feature can hasten projects developed by design teams. The HP-system user can push the X display to any platform in the network. Only the sender's display needs to have the SharedX extension. Non-HP displays running standard X Windows can receive shared windows without any modification. The tool incorporates an OSF/Motif user interface. The license fee for SharedX is $500.

***Hewlett-Packard Co.**, 3404 East Harmony Rd., Fort Collins, CO 80525; (303) 229-3800.* **CIRCLE 301**

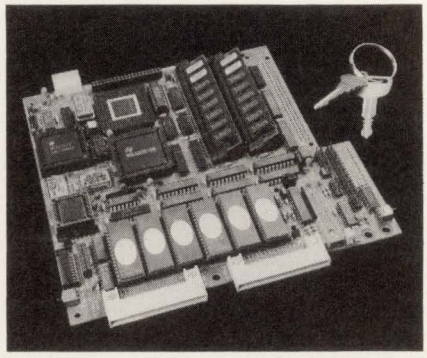
■ *RICHARD NASS*

CUT LASER-PRINTER TIME-TO-MARKET BY TWO-THIRDS

Laser-printer designers can cut their time-to-market by as much as two-thirds using Swift, a laser-printer design kit from National Semiconductor. Swift helps make true PostScript performance affordable.

The kit is based on National's NS32CG160 embedded system processor. It offers a complete, in-printer platform for evaluation, development, and low-volume prototyping of laser printers in the 4- to 8-page/min. range. It includes all of the requirements from pc-board artwork to Appletalk.

Swift fits inside a Canon LX-based printer and hooks directly to the power supply and front panel, supplying a development platform as well as a totally functional printer. Third-party vendors, including Microsoft and Phoenix Technologies, have already ported finished languages to Swift, including PCL 4 and 5 and PostScript-compatible



programs. Swift also supports most standard interfaces, allowing full compatibility with either IBM PC or Apple Macintosh environments. The Swift board is available now for $1200.

***National Semiconductor Corp.**, P.O. Box 58090, 2900 Semiconductor Dr., Santa Clara, CA 95052.* **CIRCLE 302**

■ *RICHARD NASS*

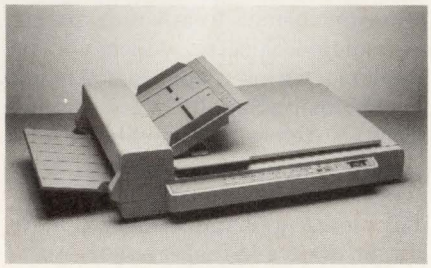
TAPE BACKUP REDUCES COST PER MBYTE

The QFA-700 1/4-in. tape drive and controller board backup system pushes the cost per Mbyte down to $2.28. Holding 700 Mbytes of data, the drive, combined with a DC-6000 tape cartridge, is suitable for network applications. Backing up 40 Mbytes of data in just 4 minutes, the drive comes ready to install in an IBM PC/AT or compatible computer with the company's TC-02 controller. The drive can also be used as an external peripheral.

Standard software is fully DOS-compatible and includes software data-compression and LAN support. Xenix/Unix software is also available. The QFA-700 sells for $1199. The external version costs $1498. The TC-02 controller costs $399 or $499 for Micro Channel computers. Large-quantity discounts apply. The drive is available immediately.

Colorado Memory Systems Inc., 800 S. Taft Ave., Loveland, CO 80537; (303) 679-0401. **CIRCLE 303**

SCANNER READS 20 PAGES/MINUTE



Documents up to 11-1/2 by 17 in. can be scanned using the M3096E+ scanner. The peripheral has an improved throughput, scanning up to 20 letter-size documents per minute at a resolution of 200 dots/in. A SCSI version (M3096G) of the scanner is available for workstation platforms. Advanced optical-character-recognition capabilities are available using an optional dynamic-threshold circuit. This feature automatically scans the page and sets the scanning threshold on a line-by-line basis to account for variations in shading and image quality of the original document. The circuit also filters out noise or random dots that could appear. The M3096E+ scanner, which can be powered from either 110 or 220 V ac, sells for $6720. The dynamic-threshold circuit is priced at $1250.

Fujitsu America Inc., 3055 Orchard Dr., San Jose, CA 95134; (800) 626-4686 or (408) 432-1300. **CIRCLE 304**

FAULT-TOLERANT SYSTEM IS BASED ON RISC

The XA/R Model 20 is a RISC-based midrange fault-tolerant computer that's designed for distributed critical on-line computing. The system runs the Unix System V, Release 4 operating system as well as the company's proprietary operating system. The computer is built around an Intel i860 microprocessor and includes external cache memory and intelligent I/O processors for high-volume, on-line throughput. The XA/R Model 20 is completely duplexed, offering fully redundant components for fault tolerance. It can be configured with a maximum of 96 Mbytes of memory, 7 Gbytes of disk storage, and up to 600 communications lines. The system contains hardware-based self-diagnostics and automatic fault reporting. Available in the third quarter, prices start at $247,000.

Stratus Computer Inc., 55 Fairbanks Blvd., Marlboro, MA 01752; (508) 460-2000. CIRCLE 305

MEMORY-CARD KIT EXPEDITES DESIGNS

By using the Memory Card Evaluation Kit, users can easily design memory-card drives into their systems. The kit comes with Databook's ThinCard drive, software for PC installation, a 512-kbyte SRAM card and connector, and a comprehensive engineering design guide. The guide contains actual schematics of operating memory-card applications as well as hardware and software design tips. With the kit, designers can perform an analysis of card implementation for particular applications. The kit costs $599.

Databook Inc., Tower Bldg., Terrace Hill, Ithaca, NY 14850; (607) 277-4817 CIRCLE 306

POCKET DATA LOGGER SIMPLIFIES PLOTTING

The pocket-sized Tattletale Lite data logger stores up to 512 kbytes of data from eight 15-bit inputs. It also features eight individually programmable I/O lines, a 9600-baud UART, and a liquid-crystal display. A detachable serial-interface cable connects to a host computer for launching and recovery. During launch, the host compiles and uploads the program to the Lite's EEPROM along with all of the information needed to plot and label the logged data. On recovery, the host offloads the program and data and reconstructs the time, value, and units of each measurement. Separate digital-count inputs allow for two channels of pulse accumulation. Two different speeds can be used, one for minimum current drain and one for maximum data-collection rate. The data logger can operate between 0° and 70°C. The 9-V battery-powered unit measures 2.36 by 4.71 by 1 in. It sells for $490.

Onset Computer Corp., P.O. Box 1030, 199 Main St., North Falmouth, MA 02556; (508) 563-9477. CIRCLE 307

PS/2 LINE FIRST TO GET 486SX

IBM's PS/2 Models 90 and 95 are the first to take advantage of the Intel i486SX microprocessor. These two computers are lower-cost alternatives to i486DX-based systems. The 20-MHz Model 90 has an integrated 8-kbyte cache memory for "no-wait" processing. The SX version of the processor doesn't contain a floating-point unit, but has a place on-board for an 80487SX math coprocessor. The desktop system comes standard with 4 Mbytes of RAM, expandable to 32 Mbytes, and an 80-Mbyte drive. Prices start at $8345.

The Model 95 is a deskside unit that's similar to the Model 90 with a few added features. It contains six 32-bit expansion slots, versus the three that are in the Model 90. This computer also comes standard with a 160-Mbyte hard-disk drive. Prices for the Model 95 start at $9995.

IBM Corp., 1133 Westchester Ave., White Plains, NY 10604. CIRCLE 308

TFT DISPLAY SHOWS 24,389 COLORS

CRT-like display quality is now available on an active-matrix thin-film-transistor (TFT) display. The Portable Add-In Computer contains a second-generation full-color display that can generate over 24,000 colors using Chips and Technologies' 82C457 VGA flat-panel controller. High-speed images are possible without limitations on viewing angle over a wide range of ambient lighting. The TFT display is available on four PAC models: the 486-33E, 486-25, 386-33C, and SX-20C. The 10-in. diagonal active-matrix display is priced at $3995.

Dolch Computer Systems Inc., 372 Turquoise St., Milpitas, CA 95035; (408) 957-6575. CIRCLE 309

PC/AT Image Processor Works In Real Time

Critical image-processing operations can be carried out at blazing speeds with the DT2867 integrated image-processor board from Data Translation. The board combines a high-quality frame grabber with a frame processor on one IBM PC/AT board. Histograms, frame averaging, and arithmetic and logic operations are carried out in real time (0.033 seconds); convolutions and morphology take less than two frame times (0.066 seconds). These occur more than 100 times faster than a 33-MHz 80386-based PC without the board. True frame averaging, as opposed to weighted averaging, increases accuracy when random noise needs reducing.

The board processes up to three pixels simultaneously through three parallel processing paths. Each path contains its own ALU and multiplier to achieve an overall processing rate of 75 MHz. However, the processor board doesn't sacrifice accuracy for speed. All processing using the three ALUs is done with 16-bit accuracy, ensuring that data isn't truncated during mathematical operations. The board contains a 16-bit processing buffer with 1 Mbyte of memory.

The DT2867 is supported by several levels of software. A Windows 3.0 application software package is available for powerful analysis that doesn't require any programming. For advanced users, two levels of development software ship with the board. An interface library allows high-level control of the board's hardware functions, and a command builder and driver supply register-level control. The board, shipping now, sells for $6995.

Data Translation, *100 Locke Dr., Marlboro, MA 01752; (508) 481-3700.* **CIRCLE 310**

■ *RICHARD NASS*

AT-Format RISC Machine Yields 14 MIPS

By combining a RISC CPU with low-cost PC motherboard logic and an AT (ISA) expansion bus, Deskstation Technology has created a dual-use RISC-based motherboard, the AT29K. Based on the Am29000 family of RISC CPUs, the motherboard can deliver a throughput of 14 MIPS when running at 25 MHz—a 250% increase in MIPS ratings over standard x86-family motherboards.

Originally developed so that programmers for the Am29000 could have a low-cost native platform on which to develop software, the AT29K also serves well as either an embedded controller or a standalone compute platform. The AT29K comes with eight 16-bit ISA-compatible expansion slots that can be used with standard "AT" support cards. In addition, sockets on the motherboard hold up to 4 Mbytes of RAM and the Am29050 floating-point RISC processor. A Unix-like operating system and a ROM-resident monitor are other available options. Later this year, the company also plans to offer a PC-emulation program that allows the RISC system to run DOS and most PC-based applications.

The motherboard comes standard with a ROM BIOS (256 kbytes) that supports standard PC peripherals, such as the keyboard, serial and parallel ports, floppy- and hard-disk drives, and a VGA display. Also included in the base model are 2 Mbytes of high-speed video RAM (expandable by another 2 Mbytes), a keyboard, a real-time clock, and the Am29000 CPU. An additional 8 Mbytes of data memory can be added via the ISA expansion bus. Options include upgrades to the 29050 floating-point CPU, which can deliver 50 MFLOPS of peak compute power. A real-time multitasking kernel and C compiler, assembler, linker, loader, and librarian are also optionally available. BIOS source code, which is available at no extra charge, permits users to customize the system for an application.

In single-unit lots, the 25-MHz board sells for $3495, while reduced-speed versions at 20 and 16 MHz go for $2995 and $2495 each, respectively. Samples are available from stock.

Deskstation Technology Inc., *13256 W. 98th St., Lenexa, KS 66215; Joe Gutekunst, (913) 599-1900.*

CIRCLE 311

■ *DAVE BURSKY*

VME I/O Processor Handles I/O Operations

Using RISC-like properties of bit-slice architecture, the 4000 Series intelligent I/O processor from Antares executes 10 MIPS in the VME backplane. The board can service many I/O protocols using a piggy-back module containing bus-specific circuitry and PROMs with the microinstruction set for the specific I/O protocol. Various piggy-back modules are available.

As I/O rates climb, it becomes more important to offload the host CPU of the housekeeping chores. The board accomplishes this task using a 2901 bit-slice processor ALU as a 32-bit engine. To improve the speed, microinstruction pipelining is implemented to increase the execution rate.

The microinstruction library is designed specifically to speed I/O transactions, as well as arithmetic and logic operations and interrupt service. The ALU is teamed with a 2910 microsequencer to form the 10-MIPS microengine. Virtually all of the VMEbus' resources are available to the microengine, including memory, analog-to-digital and digital-to-analog converters, and SCSI I/O. The 4000 Series I/O processor board fits in one 6U VME slot. Prices start at $3525.

Antares Group Inc., *4025 Hancock St., San Diego, CA 92110; (619) 223-4311.* **CIRCLE 312**

■ *RICHARD NASS*

Run Sparc Applications On A PC

By incorporating the Sparc-based Opus Series 500 Personal Mainframe family of PC add-in boards, users can run native SunOS and MS-DOS applications simultaneously on a PC/AT computer. The board supports SunView on standard PC monitors and can operate in the Microsoft Windows 3.0 environment. This creates a bridge between DOS and Unix. With the board, all Sparc-based applications (over 2000) can run without buying an expensive high-resolution monitor. The family, which is available now, starts at $6495.

Opus Systems Inc., 329 North Bernardo, Mountain View, CA 94043; (415) 960-4040. **CIRCLE 340**

WIDE SCSI CONTROLLER DELIVERS 20 MBYTES/S

With 16-bit-wide data paths, the 53C720 I/O processor for small-computer-system interfaces (SCSIs) can transfer up to 20 Mbytes/s synchronously and 10 Mbytes/s asynchronously. The processor, which is the third member of the 53C700 family developed by NCR, supports the fast and wide (16-bit) options of the SCSI-2 standard. It includes a cache-line burst mode that transfers four 16-byte back-to-back packets at 105 Mbytes/s.

The C720 chip includes a 32- or 16-bit host-bus interface, a bus-master DMA controller, a 32-bit optimized RISC CPU core, and an intelligent SCSI port. The chip is upwards-compatible with NCR's Scripts SCSI programming language. It supports the 16-bit P-cable extension to the SCSI-2 standard and can address 16 SCSI devices. Like the previous C700 and C710 I/O processors developed by the company, the C720 ties into systems with either Big- or Little-Endian word structures.

The C710's Scripts autostart feature is also included. This feature enables systems to reduce overhead by fetching a Scripts instruction from address location zero and begin execution of that instruction on power-up without processor intervention.

A key issue addressed by the chip involves the handling of odd-byte block sizes. The C720 solves this problem transparently within the chip, relieving the user of that concern. The chip can also execute tailored SCSI sequences from either the main or a local memory on the host-adapter board. Under software control, the user can write to or read inputs from several general-purpose programmable pins available on the controller.

Available in a 208-lead plastic quad-sided flat package, the 53C720 sells for $68 each in lots of 1000. Samples of the device will be available in July, with production quantities available in the fourth quarter.

NCR Corp., 1635 Aeroplaza Dr., Colorado Springs, CO 80916; (719) 596-5612. CIRCLE 313

■ *DAVE BURSKY*

ON-CHIP PLL GIVES GATE ARRAY STABILITY

An on-chip phase-locked loop along with logic that can operate at clock frequencies of up to 1.25 GHz sets apart the Q20P025 bipolar ECL/TTL-compatible gate array. The array contains about 3000 uncommitted gates with typical gate delays of about 100 ps. A smaller version of the array, containing about 900 gates, is also in development.

The on-chip PLL readily allows the arrays to handle applications that require stable timing sources—video and graphics, data and telecommunications, and system clock generation. Macros in Applied Micro Circuits' cell library include cells for frequency synthesis and clock-recovery applications, as well as support for such features as lock detect, loopback, and bit error-rate computation. The PLL can be used in systems requiring operation from 200 MHz up to 1.25 GHz. The peak-to-peak edge jitter is kept to between 50 and 100 ps, while residual bit-error-rate is 10^{-12}. Acquisition time for the PLL is only 1 μs. About 20 pins of a chip are required to handle the loop filter and PLL-related signals.

The configurable logic consumes between 0.5 and 1 mW/gate. The 76 digital I/O lines can be configured for 10K, 10KH, 100K, or positive-referenced ECL, or mixed ECL/TTL levels. Established logic macrocells from the company's Q20000 cell library can be used to create custom circuits. Designs can be done on popular platforms like those from Mentor, Valid, Dazix, Verilog, Cadence, and Lasar.

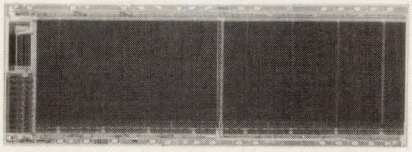
Initial versions of the large array will be offered in 100- and 132-lead chip carriers in commercial- and military-temperature grades. Prices depend on package type, quantity, and screening level. However, according to the company, a typical 100-lead commercial version might sell for about $195 apiece in lots of 2500. Prototypes can be delivered in the fourth quarter.

***Applied Micro Circuits Corp.**, 6195 Lusk Blvd., San Diego, CA 92121; Marc Friedmann, (619) 430-9333.* CIRCLE 314

■ *DAVE BURSKY*

CPU-Specific RAMs Boost System Speed

By offering features that are tuned directly to the forthcoming R4000 RISC processor, a pair of static RAMs will help RISC-based systems run at maximum throughput. The SRAMs not only operate in their pure static mode, but incorporate an extra one-word fast-access mode. With this mode, the host processor can invoke to receive the second



word of a two-word read in half the time required for the first word. This reduces the time needed to service primary-cache misses for the processor.

The PSM44298 is a 256-kbit memory, organized as 64 kwords by 4 bits. The other offering is the PSM44028, a 1-Mbit chip with a 256-k-by-4 architecture. Fabricated in the company's advanced CMOS process, the fast-access RAMs eliminate registers, buffers, and other support logic required when the processor uses commodity RAMs. The 256-kbit chips will be available in access-time grades of 10, 12, 15, 20, and 25 ns for the commercial-temperature range, and 15, 20, 25, or 30 ns for the military-temperature range. The larger 1-Mbit chips are a little slower, and offer access times of 20, 25, 35, and 45 ns for the commercial-temperature range, and the same access times plus a 55-ns unit for military-grade memories.

The 256-kbit PSM44298 will be sampled next quarter and comes in a 28-pin 300-mil plastic or a ceramic DIP, or in a 28-lead plastic SOJ surface-mountable package. The 25-ns version of the 256-kbit chip sells for $15.10 each in 1000-unit lots. The PSM44028 comes in a 28-lead 400-mil-wide sidebraze DIP or a 300- or 400-mil-wide 28-lead SOJ package. Samples of the megabit chip will be ready in the fourth quarter. In 1000-unit lots, the 400-mil-wide SOJ-housed 25-ns RAM sells for $78.22 each.

Paradigm Technology Inc., *71 Vista Montana, San Jose, CA 95134; Steve Taylor, (408) 954-0500.*
CIRCLE 315

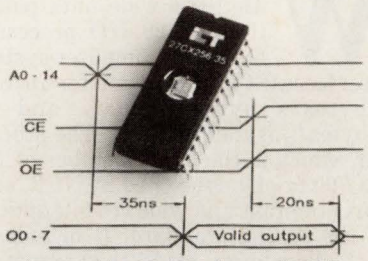
■ *DAVE BURSKY*

CMOS EPROM Claims Speed Crown At 35 ns

Offering a worst-case access time of as little as 35 ns, the 27CX256, a CMOS UV EPROM from International CMOS Technology becomes the fastest-accessing commercial EPROM at the 256-kbit level. Additional speed grades of 45 and 55 ns are also available.

Such high-speed memories will eliminate the need to shadow slow nonvolatile memories with fast RAM, because the 27CX series of EPROMs allows designers to run CPUs at peak clock rates without inserting wait states. By eliminating the shadow memory, board space and system power can be reduced, while system reliability can be improved.

Organized as 32 kwords of 8 bits each, the high-speed EPROMs are also power misers—when active they draw just 50 mA from a 5-V supply. In contrast, most other fast EPROMs draw close to twice that current. And, on standby, the chip draws 25 mA when driving TTL interfaces, and just 1 mA when driving CMOS interfaces. The chip also contains an automatic-select mode that allows EPROM programmers to read an embedded code. With



ICT 27CX256-35 High-Speed EPROM

the code, the programming tool can identify the part type and manufacturer. The tool will thus be able to configure itself automatically to deliver the proper device-programming characteristics.

Available in 600-mil 28-pin windowed ceramic DIPs, the 27CX256 sells for $21.60, $16.50, and $13.20 apiece for the 35-, 45-, or 55-ns versions, respectively, in 1000-unit lots. Delivery is from stock.

International CMOS Technology Inc., *2125 Lundy Ave., San Jose, CA 95131; Ed Nieda, (408) 434-0678.* **CIRCLE 316**

■ *DAVE BURSKY*

Accelerated VGA Interface Soups Up Drawing Operations

By placing key screen-manipulation routines in hardware, the W5086 graphical-device interface can accelerate the most commonly performed Windows graphical-user-interface (GUI) drawing functions by two to five times.

The Weitek chip integrates the bit-block-transfer and line-drawing operations and also includes a full VGA-compatible graphics controller. It can be used in 16- or 32-bit systems and offers up to 2048-by-1024-pixel resolution in its monochrome mode, and resolutions of 1024-by-768 pixels with 16 colors, or 800-by-600 or 640-by-480 pixels with 256 colors. All of the high-resolution modes support noninterlaced or interlaced monitors.

The accelerated bitBLT and line-draw functions allow images in the Window screens to be redrawn two to five times faster. Users can thus do more graphics work in the same amount of time.

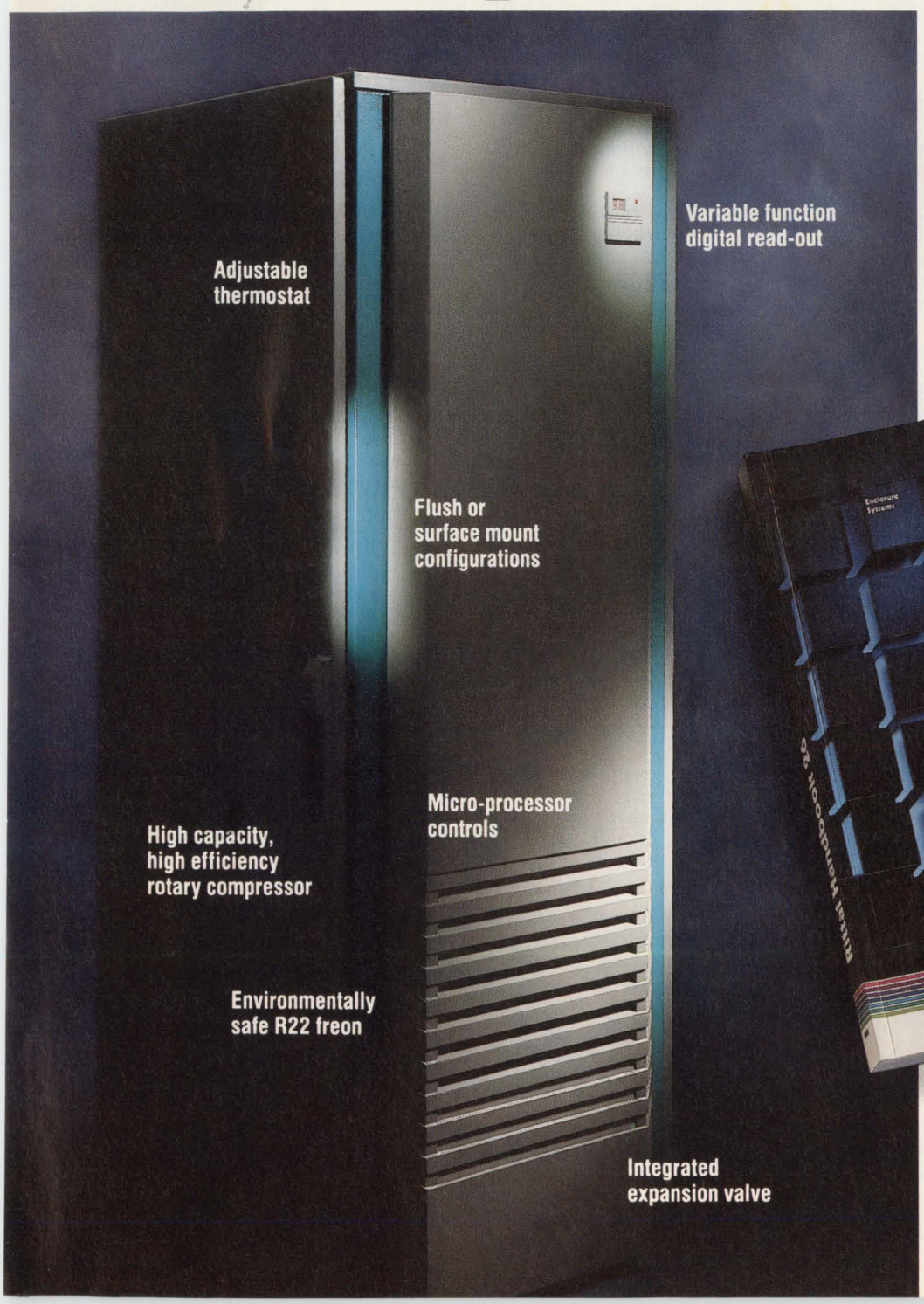
The chip is designed with dedicated drawing hardware as well as a 1024-byte memory-mapped command queue; these two features enable the circuit to perform the two key operations up to 15 times faster than standard VGA circuits. That results in the overall two to fivefold speed improvement.

Both the 70-MHz W5086 and a higher-speed, 80-MHz W5186 are available to suit most system speed requirements. Drivers for Windows 3.0 and AutoCAD release 11, among others, are available for the controllers. The W5086 comes in a 100-lead PQFP and sells for $30 in lots of 1000. Samples will be available this quarter. The higher-speed W5186 will come in a 144- or 160-lead PQFP and will be sampled next quarter.

Weitek–Corp., *1060 Arques Ave., Sunnyvale, CA 94086; (408) 738-8400.* **CIRCLE 317**

■ *DAVE BURSKY*

RITTAL Lowers The Temperature, Not Your Design Expectations.



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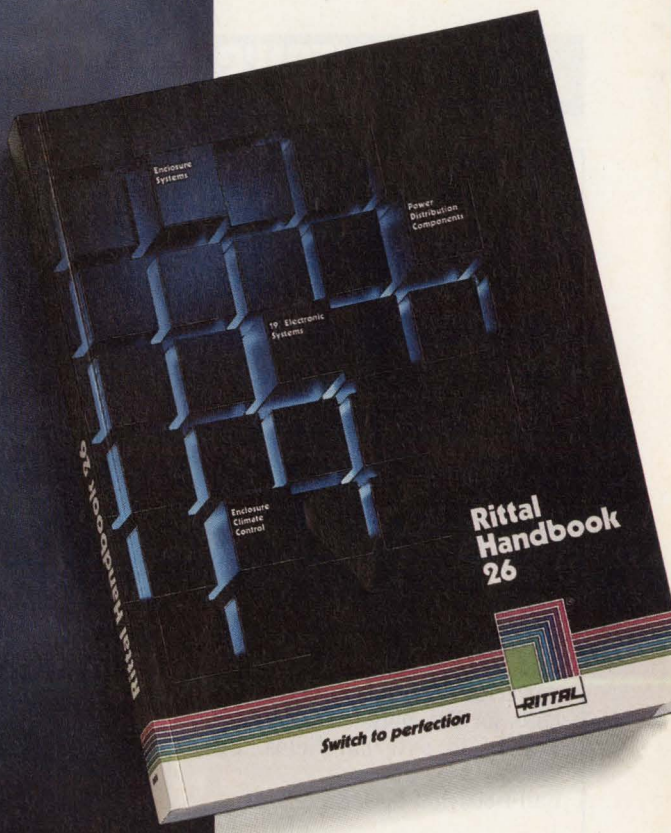


RITTAL Corporation
3100 Upper Valley Pike
Springfield, OH 45504
Phone: 1-(800)-477-4000
Fax: (513) 328-5299

CIRCLE 139

FULLY-STATIC 386SXL REPLACES INTEL 386SX

Just as it recently did with the full 32-bit 80386, Advanced Micro Devices has developed a fully-static CMOS replacement for the Intel Corp. 80386SX, the 16-bit bus-interface version of the 80386DX. Two versions of the replacement will be offered, the Am386SX-25 and the Am386SXL-25, with the SXL being a lower-power sort option from the manufacturing line. Both versions run at 25 MHz—the highest commercially available speed for an 'SX CPU—and can thus produce a system that delivers about 25% higher throughput over the 20-MHz units Intel has released.

The fully-static design keeps the power consumption of the Am386SX and SXL to less than 65% that of the Intel 386SX units when running at the same clock frequencies. Furthermore, in a standby condition, the AMD parts consume just 80 μA (with the clock stopped) versus about 140 mA for the Intel CPU, which requires a 2-MHz minimum clock signal.

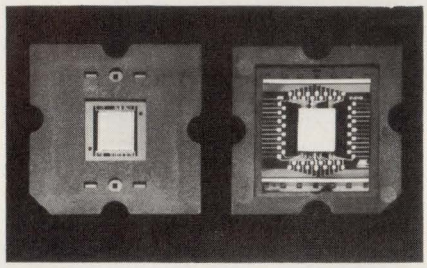
That lower power level will allow portable system manufacturers to extend the battery endurance by close to 25% over systems based on the Intel CPU. Several companies are working with AMD to ensure their PC motherboard chip sets work with the 25-MHz CPUs, which are housed in 100-lead plastic quad-sided flat packages. Prices for the 25-MHz CPUs will be competitive with the 20-MHz versions of the Intel 386SX CPUs.

***Advanced Micro Devices Inc.**, 5900 E. Ben White Blvd., MS-522, Austin, TX 78741; Glen Burchers, (512) 462-5825.* **CIRCLE 318**

■ *DAVE BURSKY*

HIGH-DENSITY PLD PACKS 128 REGISTERS

Boasting about 5000 gates of logic that include 104 flip-flops embedded in 52 I/O logic cells and another 24 buried flip-flops, the ATV5000 array from Atmel provides designers with an alternative to the



popular EPM5128 from Altera Corp. The CMOS UV-EPROM-based chip has "universal" and "regional" buses to interconnect all resources. The universal bus routes true and false signals from each of the 52 I/O pins to all sections of the chip, while the regional buses perform local routing of the Q and $\overline{Q}$ flip-flop outputs within each of the chip's four quadrants.

Each I/O line has an input latch as part of the configurable logic cell. Also in the cell are two more flip-flops, three sum terms and three array inputs. The three sum terms can be combined to provide sum-term options of 4, 5, 9, or 13 product terms. The ATV5000 can also bury both registers in the I/O cell and still deliver a combinatorial signal to an output pin. It can also feed the Q output of its primary logic-cell flip-flop to an I/O pin and simultaneously directly feed back the combinatorial term. Each buried cell contains one sum term with five product terms, a flip-flop, and individual Preset, Clear and Clock terms.

The ATV5000 also has eight dedicated input lines for clock signals or for other logic functions. Standard off-the-shelf third-party software and programming tools can be used to start new designs. The circuit can run at up to 50 MHz and will initially come in a 68-lead windowed, ceramic J-leaded chip carrier or a windowed PGA. In lots of 100, the J-leaded unit sells for $95. Delivery is from stock.

***Atmel Corp.**, 2125 O'Nel Dr., San Jose, CA 95131; Steve Sharp, (408) 441-0311.* **CIRCLE 319**

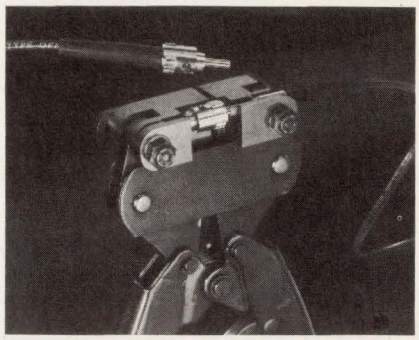
■ *DAVE BURSKY*

FIBER-OPTIC CONNECTOR SIMPLY CRIMPS ONTO CABLE

One of the least-attractive aspects of using fiber-optic connectors has been the epoxy that's needed for assembly. Epoxy significantly increases the cost of each termination and adds extra equipment, time, and, not least, a mess. Generally, earlier attempts at epoxyless connectors haven't had the mechanical strength to retain the fiber. But now, AMP dodges the epoxy headache with its LightCrimp technology, which enables a 2.5-mm bayonet connector to be simply crimped onto fiber-optic cable with no epoxy, oven, or UV curing.

The cornerstone of the technology is its epoxyless fiber-retention system, which, combined with simple hand tools, completes a fiber termination in less than two minutes. All that's required is a two-step crimp, a cleave, and a 30-second polish.

Double clamping is the key to the LightGuide system. A front fiber clamp prevents pistoning, which is an in-and-out movement of the fiber in the connector due to thermal cycling, while a rear buffer clamp increases the termination's tensile strength. The crimping and cleaving tools are inexpensive and



easy to use, requiring minimal skill.

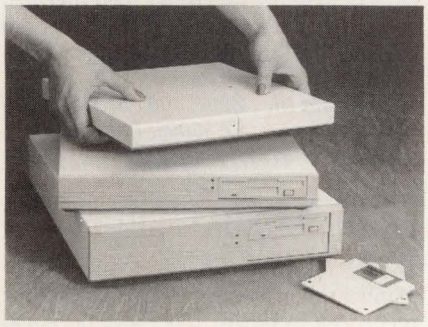
One personal goal AMP set for the epoxyless connectors is insertion loss and mechanical performance equal to that of epoxy connectors. With that in mind, AMP achieved an insertion loss of less than 1 dB, using 62.5-μm multimode cable. Durability is 500 cycles.

The 2.5-mm connector costs from about $6 to $7 apiece, depending on quantity. Total termination cost per connector ranges from $7 to $10. Availability is scheduled for June 1.

AMP Inc., P.O. Box 3608, Harrisburg, PA 17105-3608; (800) 522-6752. CIRCLE 320

■ *DAVID MALINIAK*

LOW-PROFILE ENCLOSURES CONTAIN WORKSTATIONS



Three models of low-profile computer enclosures are now available to save space and cost for workstation builders. Model 1000 is a disk or diskless enclosure measuring 1.25 in. high by 10.75 in. wide by 10.75 in. deep. It holds a system board and modules for video and local-area-network hookups. In a network or as a standalone workstation, the models 1100 and 1200 enclosures can handle larger systems. The 1100 measures 1.75 in. high by 11.5 in wide by 13.88 in. deep. Model 1200 is 2.75 in. high, 11.9 in. wide, and 14.75 in. deep. Both can hold a system board, a 3.5-in. floppy-disk drive, a hard-disk drive, plus three modules for video and communications. The 1200 accommodates two standard ISA boards and a second floppy-disk drive as well. Call for pricing and delivery.

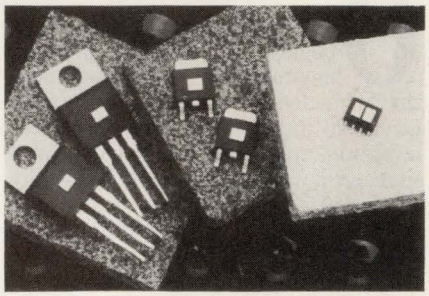
Enclosure Technologies Inc., 256 Airport Industrial Dr., Ypsilanti, MI 48198; (313) 481-2200. CIRCLE 321

X-RAY SYSTEM FITS ON DESKTOP

A microfocus, real-time X-ray system is housed in a self-contained package small enough to fit on a desktop. The Fluoroscan Series 800 inspection system, which can be transported and operated on a cart, inspects a wide variety of components, parts, and assemblies. The system consists of an integrated X-ray cabinet, microfocus X-ray tube, generator, image-forming subsystem, monitor, and multi-axis manipulator. It's well suited for quality-assurance or failure-analysis applications. Call for pricing and delivery.

IRT Corp., 3030 Callan Rd., San Diego, CA 92121; (619) 450-4343. CIRCLE 322

DMOSFET PAIR IN AN 8-PIN SOIC HANDLE POWER OF TWO TO-220S



At first it seems impossible—two power MOSFETs stuffed into just one, tiny, 8-pin SOIC doing the job of a pair of power FETs—each in its own TO-220 package or DPAK. If you need power control in zero volume, Siliconix Si9952DY, Si9953DY, and Si9955DY can do just that for you. These dual DMOSFETs are actually unique power ICs. Both FETs are on the same die, yet still isolated from each other.

The Si9952 contains n- and p-channel FETs each rated at 20 V drain-to-source. The n-channel device carries 3.5 A of maximum continuous current and the p-channel device carries 2.3 A. Peak currents can typically run four times the continuous values. With a gate-to-source voltage of 10 V, on-resistance of the n-channel FET is 100 mΩ maximum while conducting 1 A. Under similar conditions, maximum on-resistance of the p-channel FET is 250 mΩ. This CMOS power pair aims at motor-control applications in next-generation tape and disk drives, and other products where space is at a premium.

The Si9953 and Si9955 hold dual isolated 20-V p-channel and 50-V n-channel FETs, respectively. The former can switch loads in laptop computers, cellular telephones, and modems. The latter can control 24-to-36-V motors in printers, plotters, automobiles (mirror and ventilation-positioning motors), and can also be used for low-power, two-switch dc-dc converters. The p-channel FETs in the Si9953 have specifications similar to the single p-channel device in the Si9952. The 50-V n-channel FETs in the Si9955 can carry 3 A continuously and 7.2 A peak. On-resistance runs a maximum of 130 mΩ.

In lots of 100,000, the Si9952, Si9953, and Si9955 go for $0.92, $0.97, and $1.01 each, respectively.

***Siliconix Inc.,** 2201 Laurelwood Rd., Santa Clara, CA 95054; (800) 554-5565, ext. 1400.* CIRCLE 325

■ *FRANK GOODENOUGH*

FAST RECTIFIERS TAKE 400 V/4 A, 35 V/12 A

Today's switching power supplies operate at frequencies beyond the 1- and 5-MHz circuits in the labs. However, the ubiquitous rectifier limits performance. Now Motorola has announced seven, high-speed, dual rectifiers that can handle the switchers of today and tomorrow. In their 3-lead TO-220 packages, the rectifiers' cathodes are tied together, to the center lead, and to the tab. Six of the duals contain power Schottky diodes; the seventh, the MURH840CT, has two 400-V/4-A-per-leg, ultrafast silicon diodes. It offers a maximum reverse recovery time of 28 ns. Forward drop equals 1.5 V at 4 A. The highest-voltage Schottkys, the MBR20200CT and MBR20150CT, employ a platinum-barrier metal. They're rated at 200 and 150 V, respectively, and at 10 A/leg. Forward voltage drop is 0.9 V at 10 A. They and the other Schottkys handle dV/dts of 10,000 V/μs. The MBR2535CTL and MBR2530CTL are rated at 35 and 30 V, respectively (12.5 A); the remaining pair at 30 and 15 V (10 A). The forward drop of all four is under 55 mV at rated current. In lots of 100, pricing ranges from $1.63 to $2.94 each.

Motorola Inc., Z201, 5005 E. McDowell Rd., Phoenix, AZ 85008; Larry Baxter, (602) 244-5757. CIRCLE 326

LEAD-ACID BATTERIES BOAST LONG LIFE

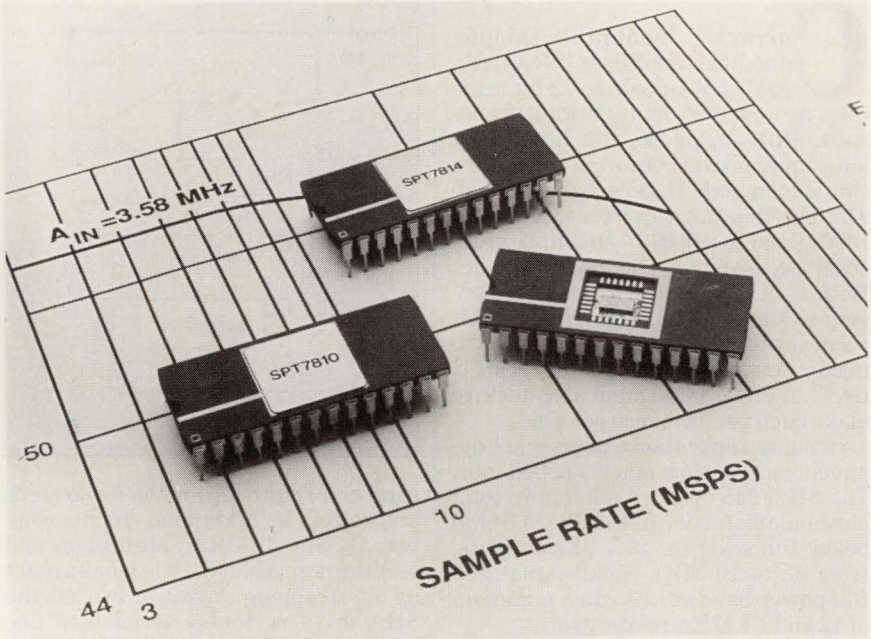
Applications from portable video-tape recorders to power tools and personal computers can be found for the HP-type sealed lead-acid batteries. The Hitachi cells feature maintenance-free construction and can be used for 260 or more cycles at 100% or for five years in standby service. The compact, lightweight cells help reduce the overall cost of a power-supply system. A safety valve detects rising internal pressure and vents gases as necessary. Call for pricing and delivery.

Maxell Corp. of America, 22-08 Route 208, Fair Lawn, NJ 07410; (201) 794-5900. CIRCLE 327

10-Bit Multistep ADC Samples And Converts At 40 MHz

FRANK GOODENOUGH

Until about 18 months ago, a 10-bit 40-MHz sampling-rate analog-to-digital converter (ADC) came on a 5-by-7-in. pc board, took 20 W of power from four separate supplies, needed 500 linear feet per minute of cooling air, and cost in the neighborhood of $4000. Its IC successor, the AD9020, a pure-flash ADC, cut all of those numbers by orders-of-magnitude. Now, startup Signal Processing Technologies (formerly the analog group at Honeywell's Colorado Springs operation) is challenging the flash with a pair of 10-bit ADC chips based on a multistep architecture, the SPT7810 and SPT7814. The SPT7814 runs at minimum word rates to 40 MHz, its cohort at minimum rates to 20 MHz. The SPT7814 is the fastest off-the-shelf, 10-bit ADC that doesn't employ a flash architecture.



The design of these new ICs offers several significant advantages over that of a flash. For starters, they require less silicon area and are thus less expensive, yet they still provide high performance. In hundreds, the top-grade SPT7814, which provides a maximum differential nonlinearity (DNL) of ±1 LSB and guarantees no missing codes, goes for $139 each. Integral nonlinearity (INL) runs a maximum of ±3 LSB. The B-grade SPT7814 offers maximum INLs and DNLs of ±2 and ±5 LSBs, respectively, and costs $109 each in hundreds. Power drain of both ADCs is just 1.5 W from ±5-V rails (about half that of the flash from similar supplies).

The pair's most important and unique feature is its ease of drive. Because the incoming signal looks at the input of a sample-and-hold amplifier rather than a flash ADC's hundreds of comparators, input impedance runs a minimum of just 5 pF in parallel with 250 kΩ. That's compared with the flash chip's input impedance of 45 pF (±1 pF) in parallel with 7 kΩ. With such specs, the difference in drive requirements for a 15-MHz input signal isn't inconsequential. The small input capacitance also keeps the typical overvoltage recovery time (for 500 mV of overdrive) below 10 ns.

Today, virtually all ADCs must give the user ac as well as dc specifications, and these are no exception. With the SPT7814A sampling at 40 MHz, signal-to-noise ratio (less harmonics) runs a minimum of 57, 56, and 50 dB for input signals of 1, 3.58, and 15 MHz, respectively.

All ac specifications run 3 dB poorer for the B-grade units. Under similar input-signal conditions, the effective-number-of-bits (ENOB) rating typically runs 9, 8.5, and 7.5, respectively. Total harmonic distortion (THD) for the A-grade converters at the same three input frequencies runs a minimum of 57, 54, and 46 dB, respectively.

Like flash and many multistep ADCs, the chips contain a 500-Ω reference divider that's driven with ±2.5 V. Three taps on the divider may be driven from adjustable, stiff voltage sources to bring the INL to 12-bit accuracy.

In fact, if 12-bit dc accuracy is required, microcontroller-directed autocalibration could be added around the converters. Just add a 14-bit digital-to-analog converter to drive the input and a trio of 8-bit DACs to trim the divider.

Other specifications include typical small-signal bandwidths of 150 and 120 MHz for the 7814 and 7810, respectively, and an aperture uncertainty of just 5 ps for both. These specifications lend the ADCs to undersampling applications. In addition, the reference dividers have a typical bandwidth of 50 MHz, which can turn the chips into multiplying ADCs. Unique applications will thus result, stimulating the imagination of analog designers. In addition to its 12 ECL data-output lines, an overrange ECL output is available. The ADCs are packaged in 28-pin double-width ceramic DIPs rated for the commercial-temperature range. Military devices will be available in the near future.

Pricing for the SPT7810 starts at just $99 each in 100s.

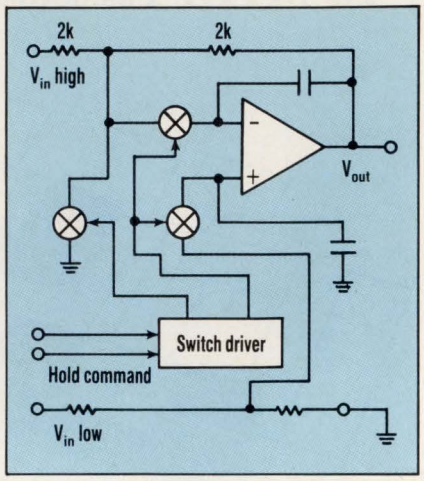
Signal Processing Technologies Inc., 1510 Quail Loop Rd., Colorado Springs, CO 80906; Richard Mintle, (719) 540-3970. **CIRCLE 328**

SHA Grabs 10-V Signals To 16-Bit Accuracy In 500 ns

Currently, monolithic sample-and-hold amplifiers (SHAs) can grab 2-V signals to 12-bit accuracy in under 50 ns (ELECTRONIC DESIGN, *May 23, p. 29).* But it will be a long time, if ever, before a monolithic chip can match Datel's hybrid SHM-945: The chip can acquire a sample of a 10-V signal to 0.00076% (16 bits) of full-scale accuracy in 500 ns maximum. With another 150 ns, it grabs a 20-V step to similar accuracy. If only 14-bit accuracy is needed, those times drop to maximums of 350 and 400 ns, respectively. A differential input architecture make such performance possible.

In many applications, users want dynamic (ac) performance spelled out. The SHM-945 offers a minimum, total harmonic distortion of –96 dB (15.6 bits) below full scale for 10-V pk-pk inputs, from dc to 10 MHz. Small-signal and full-power bandwidths run a minimum of 12 and 1.6 MHz, respectively.

Unlike most SHAs, the SHM-945 has differential input and hold capacitors on both op-amp inputs. The differential input rejects common-mode noise and permits operation from balanced lines. The capacitor on the op amp's plus input turns charge-injection effects (pedestal error) into a common-mode error and rejects it. Additional circuits compensate for dielectric absorption and feedthrough. Gains of 0.5, 1, or 2 are set by pin-strapping. A gain of two lets the SHA drive, a doubly terminated line without a 6-dB loss. In OEM lots, commercial and military grades run $79 and $87 each, respectively.



***Datel Inc.,** 11 Cabot Blvd., Mansfield, MA 02048; Bob Leonard, (508) 339-3000.* **CIRCLE 329**

■ *FRANK GOODENOUGH*

Fastest 8-Bit Flash ADC Samples Signals At 500 MHz

By adding a pair of sample-and-hold amplifiers (SHAs) ahead of a pair of flash ADCs, Micro Networks offers the fastest 8-bit analog-to-digital converter, the MN6900. It samples at a minimum of 500 MHz, but unlike most flash ADCs, it typically provides seven effective bits of accuracy at Nyquist. That is, the ADC samples 250-MHz sine waves at 500 MHz. The effective-bits rating runs 7.6, the most you can expect from an 8-bit ADC handling 10-MHz sine waves. The two-chip ADC comes in an 84-pin, multilayer-ceramic stripline package. The smaller chip is a dual SHA; the larger one is a dual, flash ADC.

The MN6900 attains its speed by letting the two ultra-fast SHAs alternately sample the input. While one SHA acquires the signal, the other holds an earlier sample as its associated ADC converts. The SHAs have aperture jitter of typically just 2 ps. The MN6900's full-power bandwidth of 1200 MHz—over four times Nyquist—adapts it for undersampling (digitizing bandlimited signals greater than Nyquist). The SHAs also provide a differential input and gain, giving the ADC a full-scale input as low as ±135 mV, not the typical 2 V.

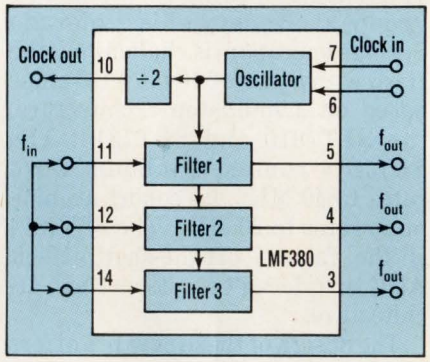
The MN6900 drops the chance of a bad bit to one every 50 days, sampling at 500 MHz. The MN5900's partner, the MN6901, has a single SHA and ADC. It provides similar performance, sampling 125-MHz signals at 250 MHz. In 100s, the MN6900 runs $990 each and the MN6901 costs $450 each. Small quantities are in stock.

***Micro Networks Inc.,** 324 Clark St., Worcester, MA 01606; Russ Mullet, (508) 752-0900.* **CIRCLE 330**

■ *FRANK GOODENOUGH*

Filters Build Real-Time Analyzer

Though digital-signal processing seems to be the technique of choice for frequency analysis, it will quite a while before it replaces most real-time filter applications. And National Semiconductor's LMF380, a triple, one-third-octave, switched-capacitor IC filter will aid the accuracy of that prediction. The chip contains three, 4th-order Chebyshev bandpass sections whose center frequencies are spaced one-third of an octave apart, lending them to real-time spectrum-analysis applications from 0.125 Hz to 25 kHz. Just ten LMF380s in a comb filter can cover the audio band from 24.4 Hz to 20 kHz. One extra IC takes the comb from 15.7 Hz to 25 kHz.



As with all switched-capacitor filters, the center frequency of the LMF380's three Chebyshevs *(filters 1, 2, and 3)* is proportional to the chip's clock. The three center frequencies are located at $f_{clk}/50$, $f_{clk}/62.5$, and $f_{clk}/80$, respectively. An on-chip clock can be built with a crystal between pins 6 and 7, or a clock can be fed to pin 6. In addition to driving the filters, the clock feeds a divide-by-two circuit, the output of which is connected to pin 10 (clock out). That output becomes the clock input to the next lower-frequency filter in the comb. Running off ±5 V, the IC swings its output ±4 V and draws 9 mA. In 100s, the commercial LMF380 goes for $8.50 each in a 16-pin plastic DIP or 20-pin PLCC. Small quantities are available from stock.

***National Semiconductor Corp.,** 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; Kay Hoang, (408) 721-2302.* **CIRCLE 331**

■ *FRANK GOODENOUGH*

10BASE-T TRANSCEIVER BOASTS LOW-POWER CONSUMPTION

Running on one-half to one-third the power used by bipolar equivalents, the 83C94 CMOS 10Base-T transceiver from includes attachment-unit-interface (AUI) features for use in embedded or external media-attachment units (MAUs). The device works with twisted-pair media and draws a typical 35 mA, compared to the 350 mA required by the nearest competitive bipolar product. In addition to a low-power idle mode, the 83C94 draws just 250 μA in a power-down mode.

For embedded applications, the transceiver works with Seeq's 8003 or 8005 Ethernet data-link controllers through the company's 8023 Manchester-code converter or standard Manchester encoder/decoders. For external asynchronous MAU applications, the 83C94 is located on a separate circuit board outside the data-terminal equipment and connects through a standard Ethernet AUI. AUI signals on the 83C94 transmit and receive data, and report collisions. LED outputs are included for MAU functions, such as transmit, receive, link integrity, jabber, collision, and autopolarity detection and correction.

Packaged in a 28-pin DIP or PLCC, the 83C94 is available now. The DIP version is priced at $9.75 each in quantities of 1000.

Seeq Technology Inc., *1849 Fortune Dr., San Jose, CA 95131; (408) 432-7400.* **CIRCLE 332**

■ *MILT LEONARD*

SIGNAL-CODING DSP CHIPS TARGET DIGITAL CELLULAR DESIGNS

Based on the DSP1600 core fixed-point technology of AT&T Microelectronics, the WE DSP1610 and WE DSP1616 are optimized for signal-coding applications in digital cellular-communications systems. Signal-coding algorithms are processed by special bit-manipulation instructions added to the basic DSP core. To accelerate these algorithms, each device has a 36-bit-wide barrel shifter that performs single-cycle left and right arithmetic and logic shifts on data in any accumulator.

Other features include single-cycle data normalization with exponent calculation, and single-cycle bit-field extract and insert instructions. Using only half of its real-time processing capacity, each IC executes the VSELP speech coder/decoder algorithm, which meets the IS-54 standards.

The DSP1610 includes an 8192-word-by-16-bit dual-port RAM for storing downloaded software. Housed in a 132-pin plastic quad flat pack, the 30-MIPS version is now available for $125 each in quantities of 10,000. The 40-MIPS version is available for sampling.

The DSP1616 comes in a 100-pin plastic quad flat pack, and has a 12,288-word-by-16-bit ROM and a 2048-word-by-16-bit dual-port RAM. Samples of both 30- and 40-MIPS versions will be available in October, with production scheduled for the first quarter of 1992. Sample price is $35 each in quantities of 10,000 (30 MIPS).

AT&T Microelectronics, *Dept. 52AL040420, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447, ext. 802.* **CIRCLE 333**

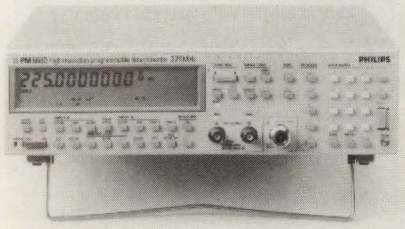
■ *MILT LEONARD*

MODEM MODULE TRIMS BOARD SPACE AND COST

Requiring just 2 in.^{2} of pc-board space, the 0.5-in.-high CH1776 modem module turns the full V.22/212A 1200-baud modem function into a single board-mountable component. The module is fully FCC Part 68 approved and responds to the standard "AT" command structure. Two interfaces are included: a serial port to connect to the host system and a two-wire interface to the telephone. Able to operate from 5 V, the module can be used as a service and diagnostic port for remote diagnostics and update. In 1000-unit lots, the module sells for $39.95 each.

Cermetek Microelectronics Inc., 1308 Borregas Ave., Sunnyvale, CA 94089; Mark McKinnon, (408) 752-5000. **CIRCLE 334**

TIMER-COUNTER FEATURES ANALYSIS FUNCTIONS



The PM 6680 timer-counter includes a wide variety of time- and frequency-analysis tools. In addition to the usual scaling, mean, min/max, and standard deviation, the PM 6680 features inversion and measurement variables (current, previous, and reference). These functions permit easier measurement of drift and drift rate, for example. Measurement rates to 2000 readings/s are possible with normal resolution and to 5000 readings/s with reduced resolution. Trigger arming can be delayed by a discrete number of events or by a selected time period with 100-ns resolution. The instrument also measures phase, duty factor, and peak voltage. The PM 6680's resolution is 500 ps for single-shot time intervals. Basic frequency range is 225 MHz, extendable to 2.7 GHz. Frequency measurements can be made with 9-digit/s resolution. The PM 6680 costs $2000.

John Fluke Mfg. Co., P.O. Box 9090, Everett, WA 98206-9090; (206) 347-6100. CIRCLE 335

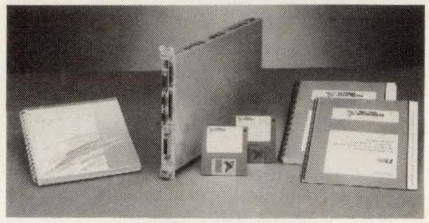
EMBEDDED VXI CPU OFFERS REAL-TIME, DISTRIBUTED CONTROL

With the VXIcpu-030 embedded controller, designers can develop distributed VXI systems with real-time control capability and can network VXI mainframes with standard workstations, PCs, file servers, and terminals. The module is a one-slot, C-size, 68030-based controller that runs the VxWorks real-time operating system from Wind River Systems, Alameda, Calif.

The VXIcpu-030 offers complete VXI functionality, GPIB control, and Ethernet capability, and comes with 2 Mbytes of shared RAM. A SCSI port and two serial ports are provided. Options available include eight additional serial ports, an internal hard-disk drive, a 68882 floating-point coprocessor, and extended RAM.

The unit can directly control VXI registers, memory, interrupts, and triggers. It can also act as a message-based commander with full resource-manager capability. Able to access all VXI address spaces, the VXIcpu-030 can perform 8-, 16-, and 32-bit data transfers. For fast shared-memory communication, the on-board RAM is dual-ported to the VXIbus. The module is compatible with revision 1.3 of the VXIbus standard and with IEEE-488.2.

The VXIcpu-030 has software for real-time programming with the VxWorks operating system. To develop application software to execute on the module, users need a VxWorks development system from Wind River and a VXIcpu-030 software development kit from National Instruments. Designers that have a VxWorks development system for any other 68000-family target processor need only buy a VXIcpu-030 board support package from Wind River.



The VXIcpu-030 base unit costs $5995, with delivery in 8 to 10 weeks. The companion software development kit costs $1595. The VxWorks development system goes for $19,500 and the VXIcpu-030 board-support packages cost $600.

National Instruments Inc., 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100. CIRCLE 337

■ *JOHN NOVELLINO*

PORTABLE GENERATOR SPANS 2 TO 8 GHZ

LSI techniques and GaAs MMIC technology made it possible to create a 2-to-8-GHz programmable signal generator in a handheld package that uses only 10 W of 120-V ac power. The Model 8001 covers its frequency range in 1-MHz steps with a guaranteed output power of +10 dBm. Phase noise at a 20-kHz offset is –80 dBc (–90 dBc typical). An FM modulation input accommodates FM rates to 200 kHz and deviations from 0 to 40 MHz. Programming is through a TTL-compatible parallel BCD data bus. Users can select a 350-ms or 20-ms band-switching speed. The slower speed offers better noise performance. The unit measures 2.52 by 5.57 by 7.45 in. and weighs 2.5 lbs. The Model 8001 costs $3750, with delivery in 30 days.

April Instrument Corp., P.O. Box 62046, Sunnyvale, CA 94088; (415) 964-8379. CIRCLE 336

FAST LOGIC ANALYZERS FEATURE LONG MEMORIES

Two extended-memory logic analyzers aim at applications that require very large memories for proper analysis of microprocessor systems. The T-132D's acquisition memory ranges from 2048 kbits on 8 channels to 512 kbits on 32 channels. The T-132EM records up to 8 Mbits on 8 channels and up to 2 Mbits on 32 channels. Both units feature synchronous and asynchronous recording to 500 MHz, synchronous harmonic recording from an external clock source, three-level triggering to 250 MHz, and an easy-to-learn user interface. Hosted from a PC running Outlook software or a GPIB controller, multiple analyzers can be combined to handle up to 448 channels. The T-132D and T-132EM cost $49,500 and $64,500, respectively. Delivery is within 90 days.

Outlook Technology Inc., 200 E. Hacienda Ave., Campbell, CA 95008; (408) 374-2990. CIRCLE 338

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Dataq Instruments Inc., 825 Sweitzer Ave., Akron, OH 44311; (216) 434-4284. CIRCLE 339

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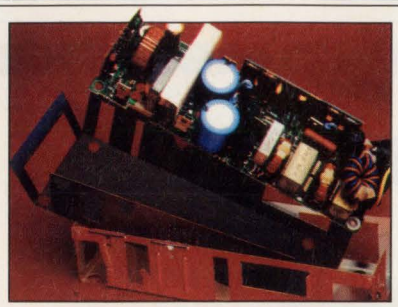

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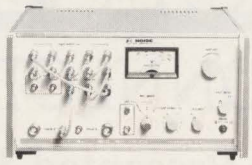

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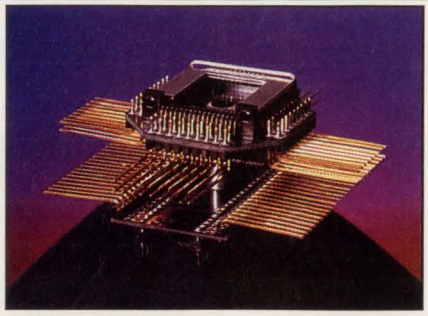

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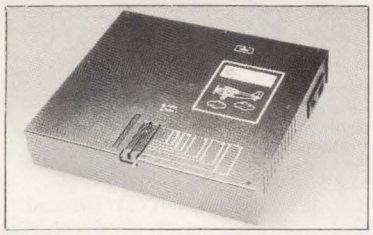

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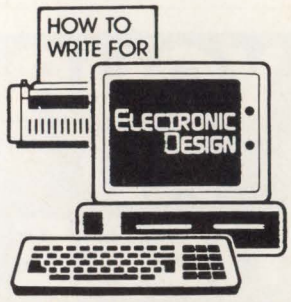

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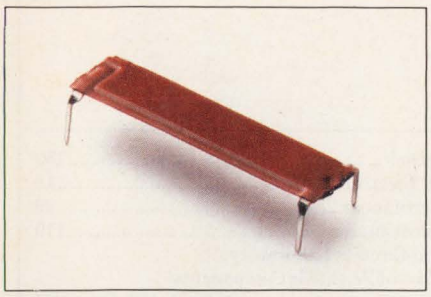

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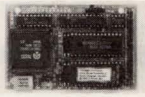

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SPDT switch dc to 5GHz with built-in driver

Truly incredible...a superfast 3nsec GaAs SPDT reflective switch with a built-in driver for only $19.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' YSW-2-50DR?

Check the outstanding performance specs of the rugged device, housed in a tiny plastic case, over a -55° to +85° C span. Unit-to-unit repeatability for insertion loss is 3-sigma guaranteed, which means less than 15 of a 10,000-unit production run will come close to the spec limit. Available for immediate delivery in tape-and-reel format for automatic placement equipment.

New... ZYSW-2-50DR Connector Version (SMA) available, $59.95 (1-9)

SPECIFICATIONS

YSW-2-50DR / ZYSW-2-50DR	dc-500MHz	500-2000MHz	2000-5000MHz
Insertion loss, typ (dB)	0.9	1.3	1.4
Isolation, typ(dB)*	50	40	28
1dB compression, typ (dBm @ in port)	20	20	24
RF input, max dBm (no damage)	22	22	26
VSWR (on), typ	_____	1.4	_____
Video breakthrough to RF, typ (mV p-p)	_____	30	_____
Rise/Fall time, max (nsec)	_____	3.0	_____

PRICE YSW-2-50DR $19.95 (1-9)
ZYSW-2-50DR $59.95 (1-9)

*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

finding new ways...
setting higher standards

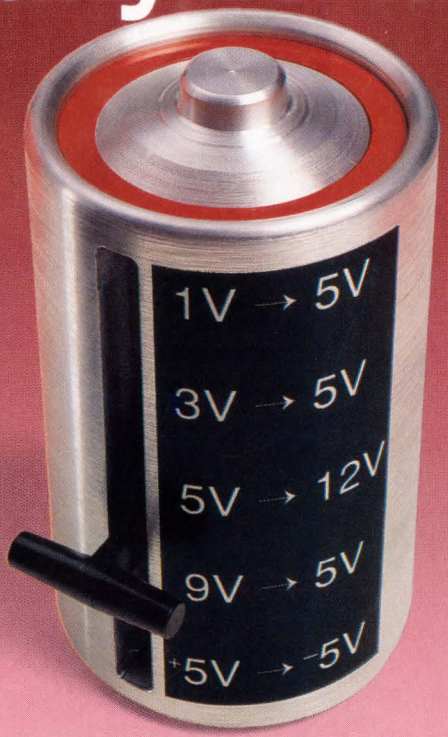
Mini-Circuits WE ACCEPT AMERICAN EXPRESS

CIRCLE 121

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Telexes: 6852844 or 620156

F141 REV.A

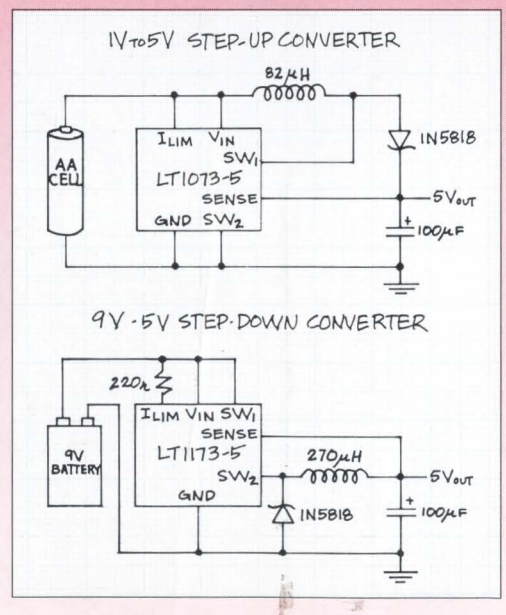
Adjust your battery to any voltage.



Micropower DC to DC converter. 1 volt, 1 inductor, 1 cap.

Finally, a true micropower switching regulator with user-adjustable current limit. Linear's new LT1073 is a versatile micropower switching regulator optimized for single-cell inputs. It's small, simple, efficient, and delivers all the features you need right now.

- Only three external parts needed
- Operates at supply voltages from 1.0V to 12V
- Startup guaranteed at 1.0V
- Consumes only 95μA supply current
- Space-saving 8-pin Mini-DIP or SO8 package
- Works in step-up, step-down, or inverting mode
- Low-battery detector comparator on-chip
- User-adjustable current limit
- Internal 1 amp power switch
- Fixed or adjustable output voltage versions
- Programmable current limit with single resistor
- No frequency compensation required



Operation of the LT1073 is guaranteed down to 1.0V, so you can squeeze more useful energy out of a battery. Its duty cycle is set at 72%, optimizing operation where $V_{OUT} = 3V_{IN}$. And the LT1073 delivers 5V at 40mA from a single cell, and 5V at 100mA from a 3V input.

The LT1173 is optimized for higher input voltages (two or more cells) up to 30V.

It's ideal for low-to-medium power step-down applications. The 1173 features a 50% duty cycle and operates with as little as 2 volts input. Both the LT1073 and LT1173 are available now. Pricing in quantities of 100 are $3.15 for the LT1073CN8 and $2.40 for the LT1173CN8. For true micropower switching solutions and more details on these new parts contact: Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035. Or call toll free **800-637-5545.**

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FOR TOUGH APPLICATIONS.

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