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FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

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JUNE 13, 1991

AUTOMATED TOP-DOWN DESIGN FLOURISHES AT DAC

- MICROPOWER OP AMPS WORK FROM 2-V RAILS
- INTEGRATOR IC CONVERTS PICOAMPERES TO VOLTS
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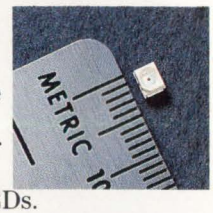
CIRCLE 157 FOR LITERATURE

Once again, HP has its name in lights.



Leave it to HP to premiere the very first SMT LED offering the brightness, clarity, and color choices of through-hole LEDs.

As one of the world's most experienced LED suppliers, HP wrote the book on high-performance LEDs. Now you can see the same star performance on tape, because our new LED is compatible with tape-fed automatic pick & place equipment and SMT solder processes.

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But we haven't let the bright lights go to our head. Our new SMT LED is competitively priced and multi-sourced.

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Once again, HP sets the stage for quality, reliability, and innovation. To get the star treatment from HP, call **1-800-752-0900, ext. 2367,** and ask for our FREE red & green SMT LED sample kit. And see what the biggest name in lights can do for you.

There is a better way.

HEWLETT PACKARD

CG08102

CIRCLE 167

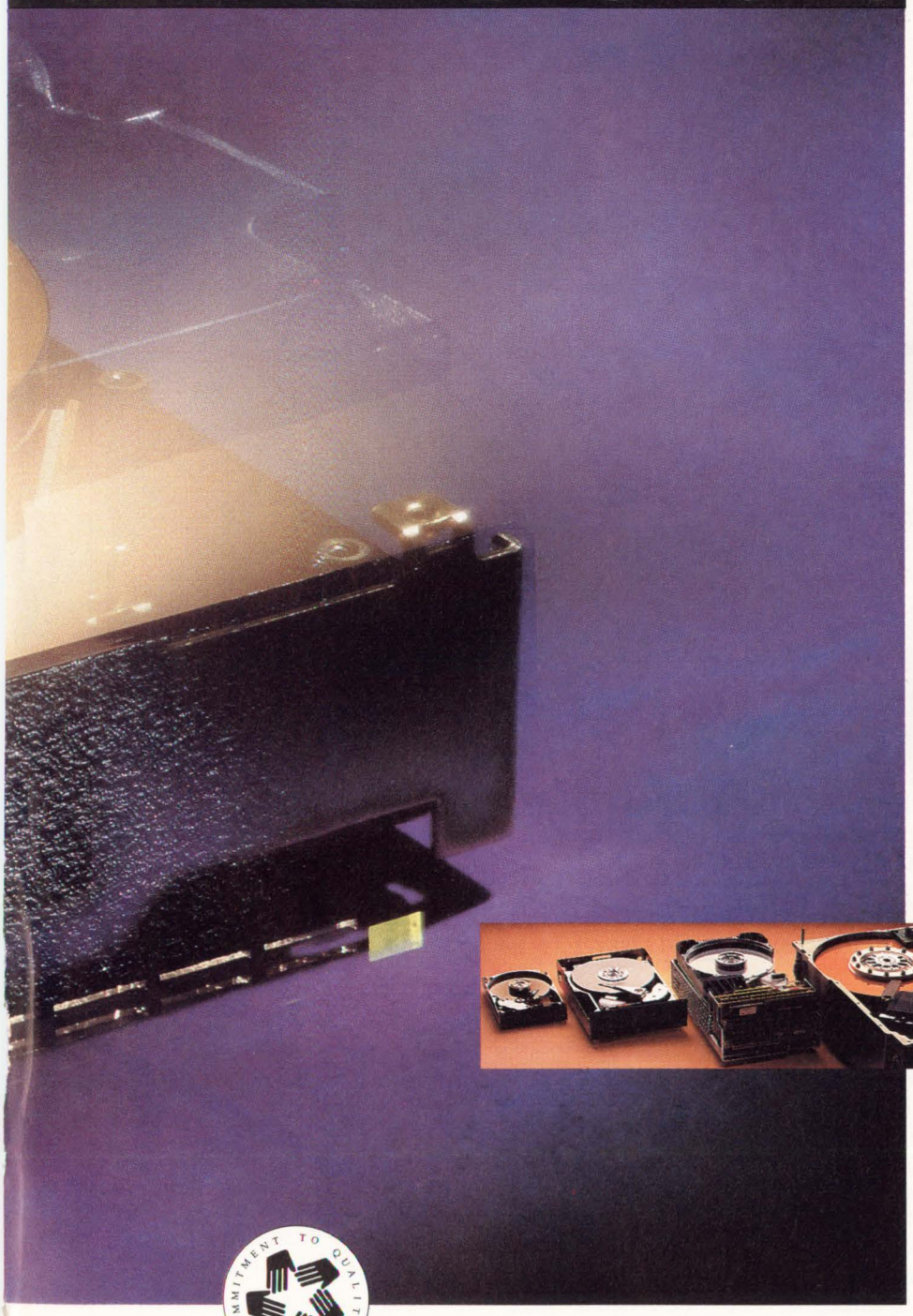
Outside, all disc drives look t
It's really what's inside that co

he same. unts.

Apart from our nameplate, a Seagate disc drive looks much like any other when viewed from the outside. But it's the tangible and intangible elements we put inside that make a Seagate drive really shine.

If you could see inside you'd find the best components available. Many of them—such as discs, motors, semiconductors and thin-film heads—we design and build ourselves, allowing us to control their quality, cost and availability. Most of what we don't manufacture is obtained from a select group of vendors who must meet our strict Supplier Certification Program criteria. This guarantees consistently high quality and continual conformance to our customers' requirements.

H N O L O G Y



Technology is another key Seagate ingredient. As the holder of over 200 disc drive patents, we constantly develop state-of-the-art technologies to enhance the value of our products to our customers. For example, Zone Bit Recording™ increases the amount of information that can be stored on a disc. But besides increasing the drive's capacity and throughput. ZBR™ technology can reduce the required number of heads and discs, thereby reducing costs, increasing performance and making the drive significantly more reliable.

The third major factor that sets Seagate drives apart is our commitment. You see it in the inspired dedication of our employees: like our engineers, who apply the latest technology advances to our current models. In our assemblers and technicians, who are committed to producing defect-free products. And in our sales, customer service and technical support groups, who continually go the extra mile to ensure complete customer satisfaction.

But most of all, Seagate drives are built upon experience: the market insight and technical knowhow that can only come from selling more than 25 million drives since the industry's inception. It's the kind of experience you won't find at any other disc drive company.

To be sure you're getting Seagate quality and technology inside where it counts, make sure there's a Seagate nameplate on the outside. For more information, contact Seagate at 800-468-DISC, or 408-438-6550.

Seagate

The first name in disc drives

CIRCLE 119

JUNE 13, 1991 VOL. 39, NO. 11

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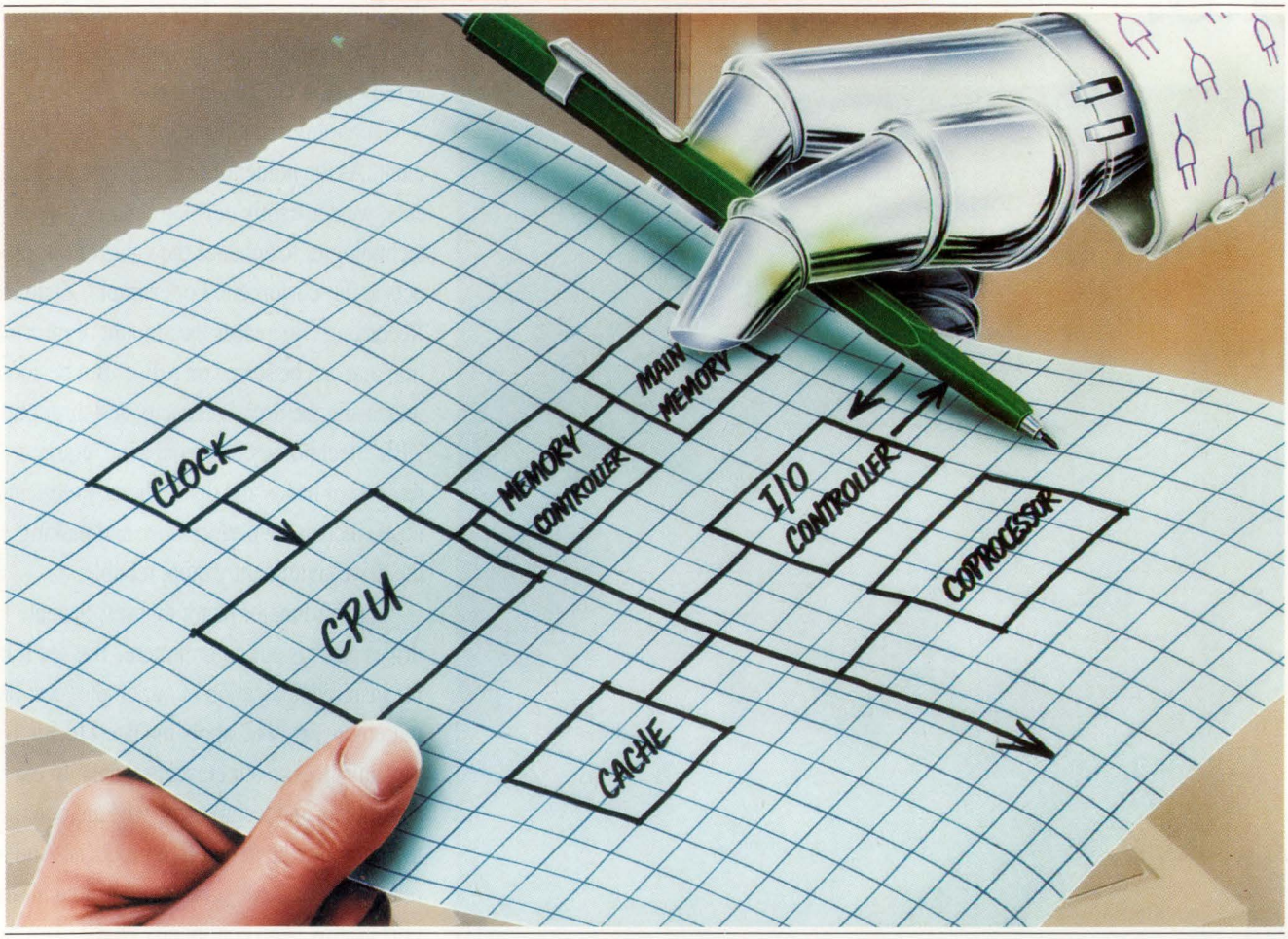

COMING NEXT ISSUE
- Design team issues: Using boundary scan in design for testability
- Attaining testability with hierarchical design
- Sort out RISC and CISC processors for embedded systems
- Using new, powerful mid-range digital storage oscilloscopes
- Innovative energy-management chips for PC battery systems
- First details on new high-voltage op amps
- Flexible programming for FPGAs keeps delays short
- PLUS:

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Certificate of Merit
Winner, 1988
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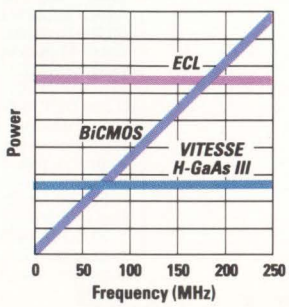

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Our prices won't guzzle your budget either– our GaAs chips can give you better performance for your dollar than BiCMOS.

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FX Arrays	Raw Gates	Usable Gates	Availability
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CIRCLE 130

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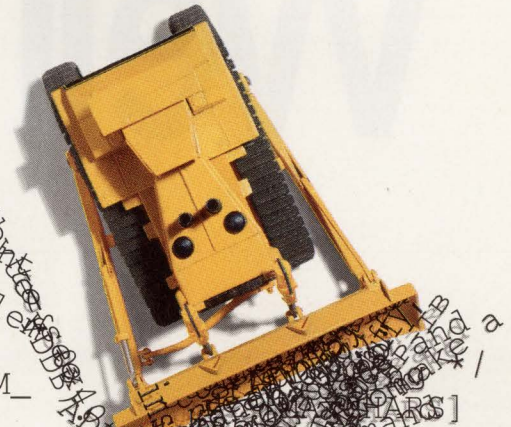
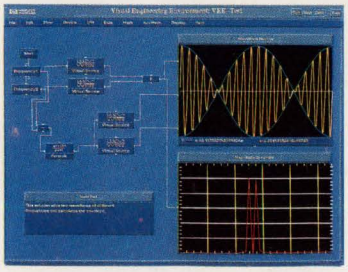
Finally, engineering software that clears the way to problem solving without programming.



```
void service
int eid;
{ int stat, byte;
/*serial poll
byte=hpib_spoll(
if ( (byte<0)||! (b
    printf("SRQ Prob
   return; }
stat=my_read(eid, DVM_
if (stat>0) {
    buffy[stat] = '\0'; i
    printf("Data from instrument:
else printf("I/O read error\n");
return; }

main() {
int busid, stat, MTA, MLA;
char command[MAXCHARS];

busid=open("/dev/hpib7", O_RDWR); /* open raw HP-IB for
MTA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
MLA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
stat = BUTTON_BIT ;
sprintf(command, "KM%02o", stat); /* 2 octal digits */
```



With HP VEE, you simply link the icons.

Computers are great for problem solving, if only programming didn't get in the way and slow you down. And now, it doesn't have to. Because the HP visual engineering environment (HP VEE) lets you solve problems without programming.

With HP VEE, you explore solutions visually by arranging and linking icons on the CRT. Each icon represents and executes a specific function for data collection, analysis—from simple mathematics to complex algorithms—and presentation. You don't have to write a single line of code.

There are two HP VEE software packages for prototyping, experimentation, and problem modeling. HP VEE-Engine, at $995*, is a general-purpose tool for analysis and presentation of existing data. HP VEE-Test includes HP VEE-Engine and adds extensive I/O capability, including soft panels and device I/O objects for $5,000*.

So, if programming is keeping you from finding solutions, call **1-800-752-0900.** Ask for **Ext. 2382**, and find out how HP VEE clears the way.

* U.S. list prices.

There is a better way.

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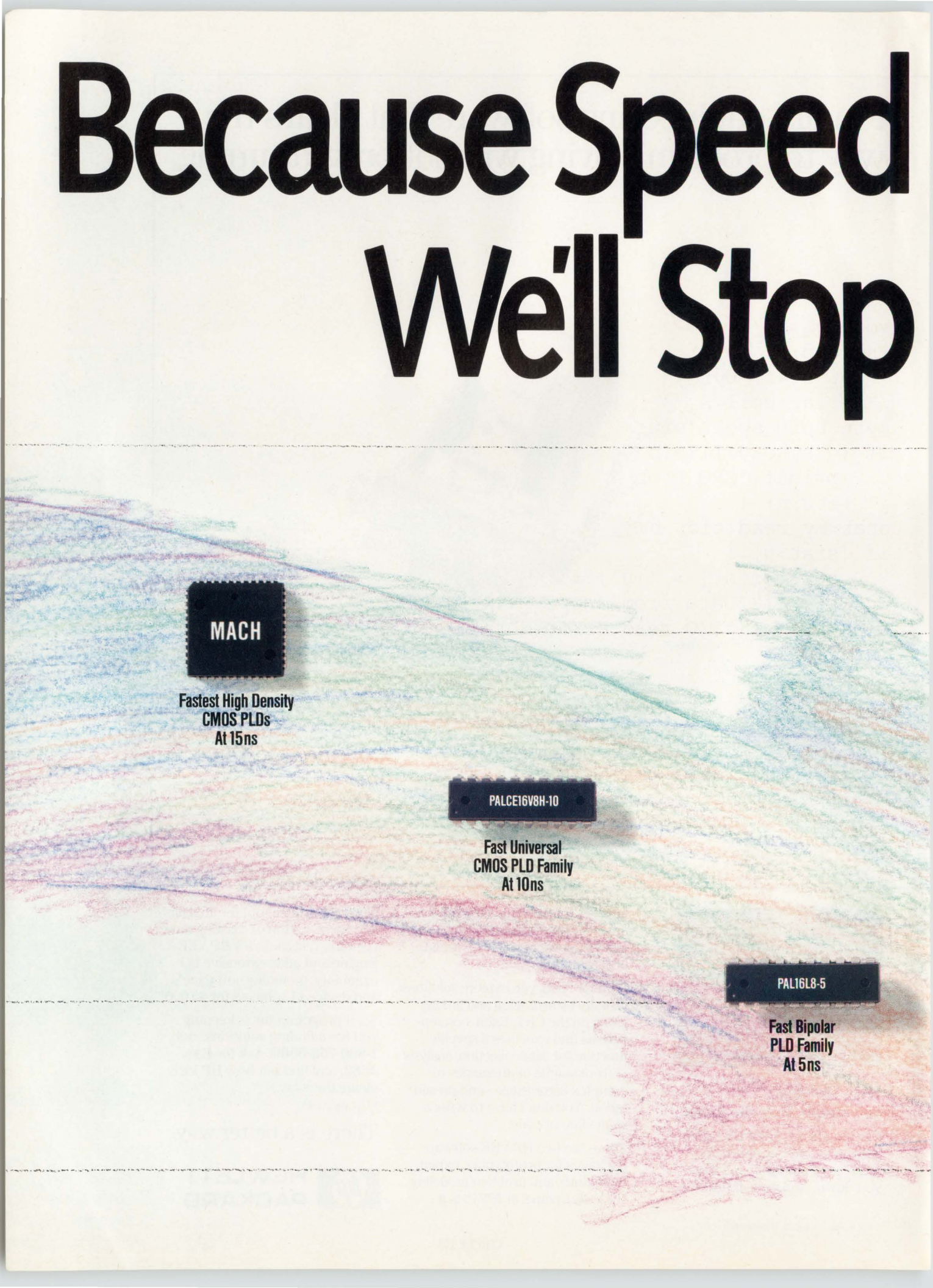
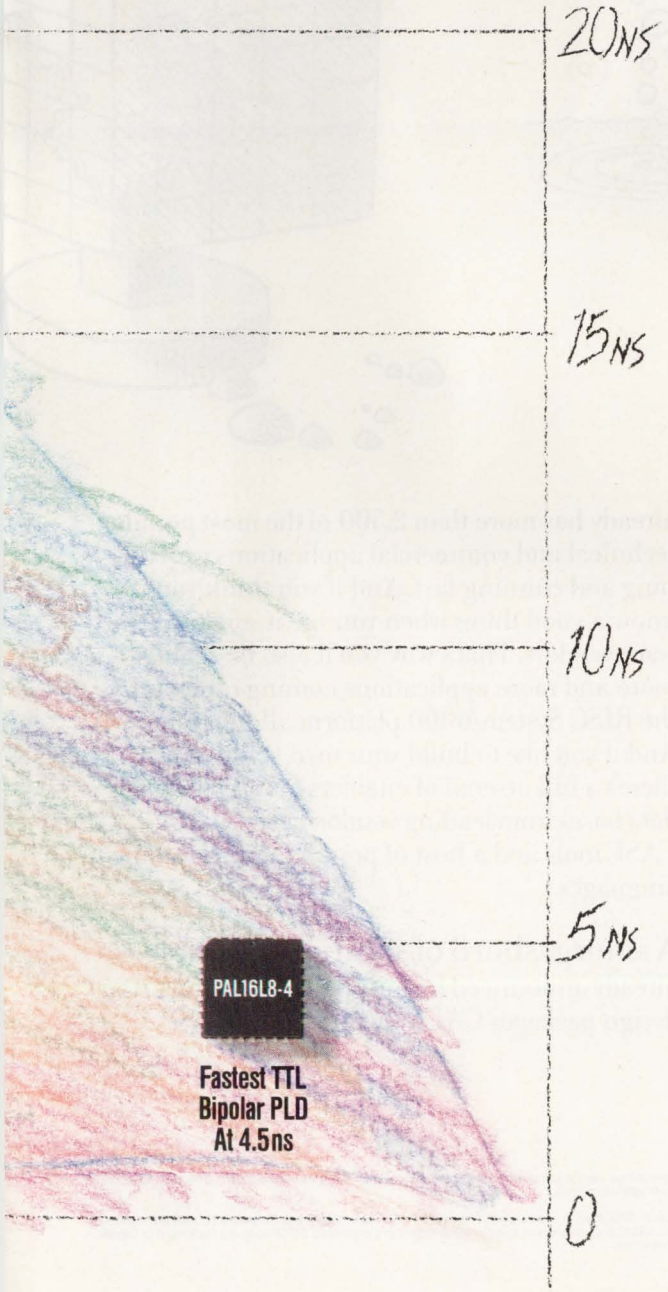
Because Speed We'll Stop



Is Everything. At Nothing.



Whatever kind of PLD you need, the fastest comes from AMD.

We'd love it if all our work amounted to "zero." As in zero delay. And we're not far off.

Not surprising—because AMD invented the PAL® device. That's why we know programmables better. And offer you the most choices of the best devices.

Say you want speed, but can't sacrifice density. Don't. Use our new MACH™ products (Macro Array CMOS High-density) that give you up to 3600 gates and 15ns performance. They're two to three times faster than the competition and cost 40% less.

For more speed, along with low power consumption, try our new 10- and 15-nanosecond CMOS PLDs. Use our 16V8-10s and 20V8-10s anywhere you'd use a GAL® device. Or choose the ever-popular AMD-invented 22V10, at 15ns.

Faster still are our seventh generation bipolar PAL devices. Complete families of 16L8-5s, 20L8-5s, and the 22V10-10s. And for real speed freaks, we're now shipping a 4.5ns bipolar PAL device—the world's fastest TTL programmable logic.

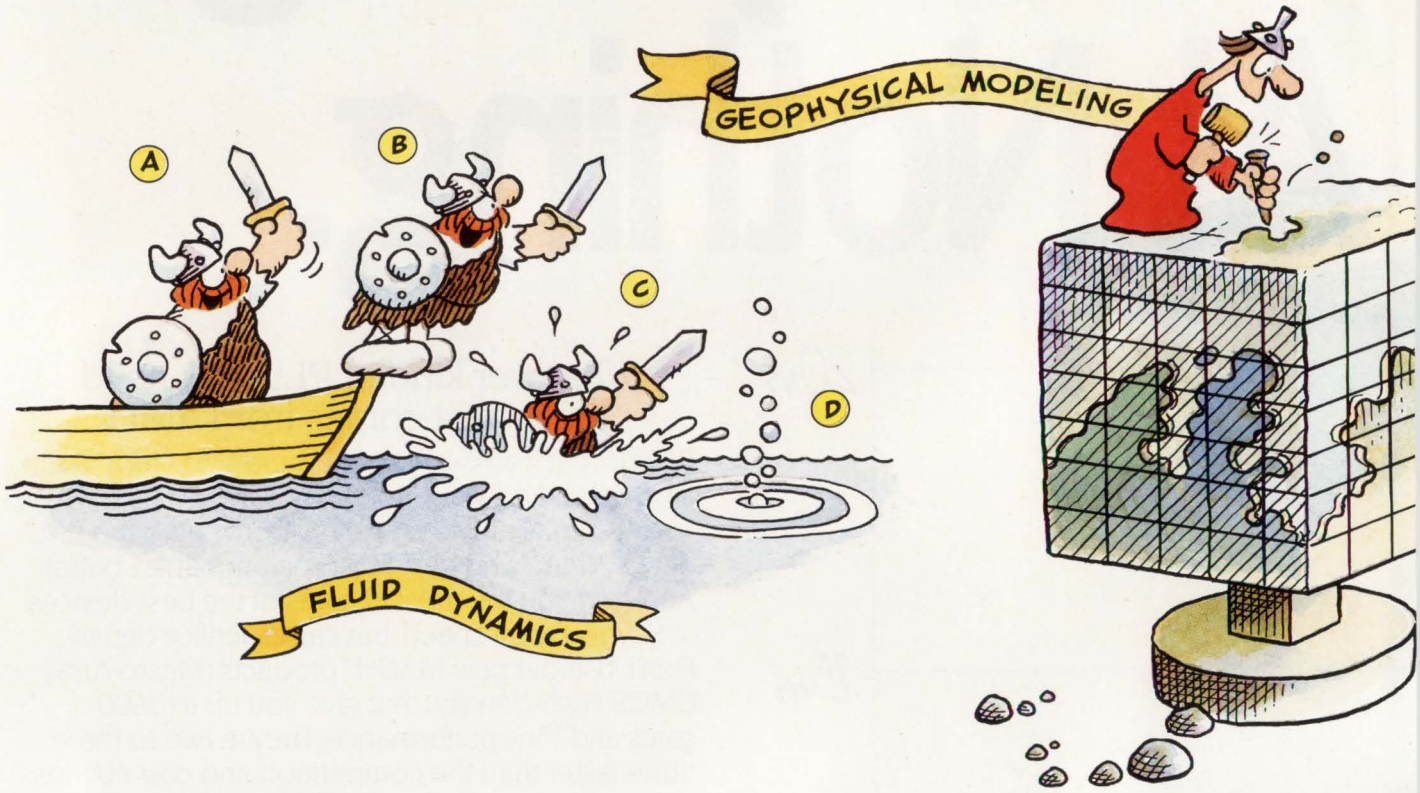
Along with all this speed, we're providing equally fast delivery. In quantity. In fact, we deliver more programmable logic devices than all our competitors combined.

For details, call AMD now at **1-800-222-9323.** And let nothing stand between you and your need for speed.

Advanced Micro Devices

CIRCLE 170

The IBM RISC System/ The power you've been seeking



It's a never-ending quest for power seekers. You're always looking for ways to run your favorite applications faster. Well, search no more. The RISC System/6000™ family of POWERstations and POWERservers gives you power that soars as high as 23 MFLOPS.

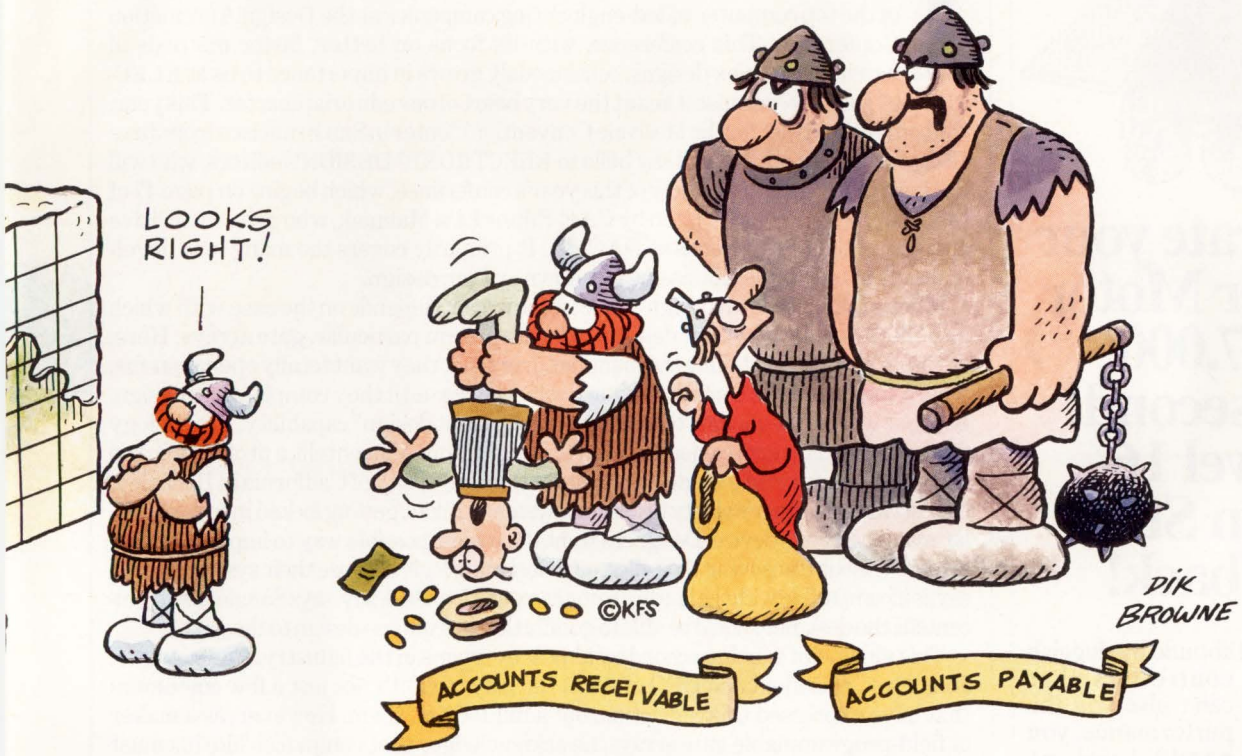
	MFLOPS	MIPS	SPECmark™
POWERstation 320	8.5	29.5	24.6
DECstation 5000-200	3.7	24.2	18.5

When it comes to porting, your ship has come in. Of course, all the speed in the world wouldn't mean much without the applications you need. So the RISC System/6000 family already has more than 2,500 of the most popular technical and commercial applications up, running and running fast. And if you think you know a good thing when you see it, so do software vendors. That's why you'll also be seeing more and more applications coming on board the RISC System/6000 platform all the time. And if you like to build your own solutions, there's a full arsenal of enablers and relational data bases from leading vendors, as well as CASE tools and a host of popular programming languages.

A smorgasbord of solutions. Applications already announced include the IBM engineering design packages CADAM™, CAEDS™, CBDS™,

MFLOPS are the results of the double-precision, all FORTRAN Linpack test 100x100 array suite. The Dhrystone Version 1.1 test results are used to compute RISC System/6000 Integer MIPS value where 1,757 Dhrystones/second is 1 MIPS (Vax 11/780). SPECmark is a geometric mean of ten benchmark tests. All performance data are based on published benchmark information.

6000 family. for all your applications.



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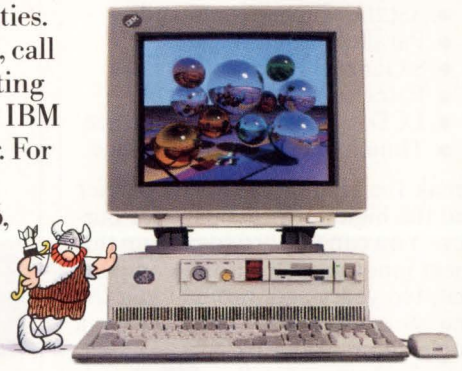
Command enormous processing clout.
The RISC System/6000 family is built to boost the performance of the software power seekers use most. It's got the best floating point processor in the business for numerically intensive applications, plus a new superscalar processor and incredible 3D graphics capabilities. To find out more, call your IBM marketing representative or IBM Business Partner. For literature, call 1 800 IBM-6676, ext. 990.



For the Power Seeker.

IBM®

TECHNOLOGY-TRANSPARENT DESIGN

In recent years, the month of June has come to represent the annual convening of the top computer-aided-engineering companies at the Design Automation Conference. This conference, with its focus on better, faster methods of handling complex designs, continuously grows in importance to us at ELECTRONIC DESIGN because it lies at the very heart of our editorial charter. This year, the conference is set for the Moscone Convention Center in San Francisco from June 16-20 (stop by booth 418 and say hello to ELECTRONIC DESIGN's editors, who will be there in force). Our preview of this year's conference, which begins on page 47 of this issue, is once again written by CAE Editor Lisa Maliniak, who gives an incisive analysis of the major trends at DAC '91. It primarily covers the many new developments in techniques for easing top-down system design.

Much of the top-down design's success, however, depends on the ease with which designers can convert their designs to hardware—in particular, gate arrays. Here, designers are clearly telling the manufacturers that they want totally open systems, where they need not commit to a particular device until they complete the design. In other words, they want "technology-transparent design" capability. Technology transparency is a term coined by Alberto Sangiovanni-Vincentelli, a professor in the EE and Computer Science departments at the University of California at Berkeley, to describe a designer's ability to design a system without getting locked in to a particular manufacturer's device. Designers want the easiest possible way to implement gate arrays without translating their files, or redesigning logic because their system timing, say, is incompatible with the hardware implementation. Basically, says Sangiovanni-Vincentelli, the designer should be able to go effortlessly from one design to the next.

This viewpoint is being echoed by almost everyone in the industry. For example, John East, president and CEO of Actel Inc., says that it's not just a few customers that have expressed this conviction, but a full 100% of them. However, as a maker of field-programmable gate arrays, he acknowledges that companies like his must swallow hard to support this concept. After all, they are loosening their hold on customers by allowing them to change devices at any time during design or production with ease. However, if they don't do it, their competitors will, as has been replayed over and over in recent years. East cites, as an example, the early signals given by automobile buyers, as evidenced in the increased sales of Volkswagens, indicating the public's desire for affordable, gas-efficient automobiles. U.S. auto manufacturers ignored such early warning signals, and have been trying to catch up ever since.

Right now, the electronics industry is also facing early warning signals from its customers. Let's go for total customer satisfaction now with totally transparent technology, and not wait until it's too late.

Stephen E. Scrupski

Editor-in-Chief

SPDT & SP4T SWITCHES

WITH BUILT-IN DRIVERS

SPECIFICATIONS

	TOSW-230 ZFSW-230DR		TOSW-425 ZFSW-425DR	
Freq. Range(MHz)	10-3000		10-2500	
Insert. Loss (dB)	typ.	max.	typ.	max.
10-100MHz	1.3	1.9	1.3	1.7
100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ. 1.3	max. 1.6	typ. 1.3	max. 1.6
Switching Time (μsec) (from 50% TTL to 90% RF)	typ. 2.0	max. 4.0	typ. 2.0	max. 4.0
Oper. Temp.(°C)	-55 to +100		-55 to +100	
Stor. Temp.(°C)	-55 to +100		-55 to +100	
Price (10-24) (1-9)	$39.95 $89.95		$59.95 $109.95	

10 to 3000MHz from $39.95

Now, high-speed, high-isolation switches with with built-in drivers, tough enough to pass stringent MIL-STD-202 tests. There's no longer any need to hassle with the complexities of designing a TTL driver interface and then adding yet another component to your subsystem... it's already included in a rugged, low-cost, compact assembly. Available in the popular hermetically-sealed TO-8 package or a small EMI-shielded metal connectorized case, these tiny PIN-diode reflective switches, complete with driver, can operate over a 10 to 3000MHz span with a fast 2μsec switching speed.

Despite their small size, these units offer isolation as high as 40dB(typ), insertion loss of only 1.1dB(typ), and a 1dB compression point of +27dBm over most of the frequency range. All models are TTL-compatible and operate from a dc supply voltage of 4.5 to 5.5 V with 1.8mA quiescent current. Switch to Mini-Circuits for highest quality innovative products... and leave the driving to us.

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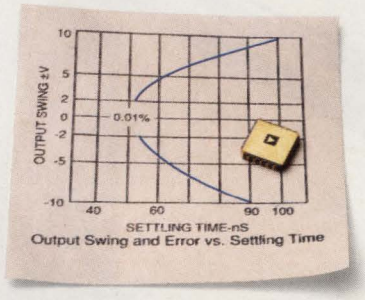
CIRCLE 95

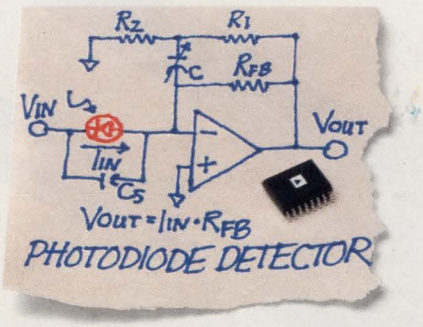
F126 REV. A

Whether you fax it, fire it, send it, measure it, wire it, compute it, The Analog family of



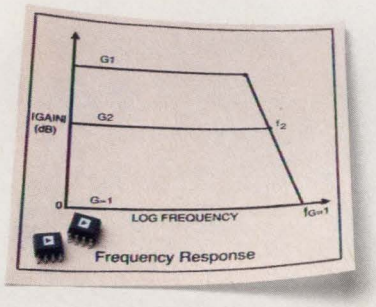
Precision

With the AD840, AD841 and AD842, there's no need to trade speed for accuracy. All three settle to 0.01% within 100 ns (840/842) and 110 ns (841) – critical in data acquisition and instrumentation applications – and offer low offset voltages and drifts, and fast slew rates.



FET Input

For op amps requiring low input current, the OP-42, OP-44, AD845 and AD843 are all remarkably fast – slew rates are 58, 120, 100 and 250 V/μs, respectively. In addition, they offer offset voltages of less than 1 mV and extremely low current noise.



Transimpedance Amplifiers

The OP-160, OP-260, AD844, AD846, AD9617 and AD9618 all utilize a current feedback architecture to achieve slew rates from 450 to 2000 V/μs without compromising stability – even in hostile environments. Other benefits include low power dissipation and high unity-gain bandwidth.

If whatever it is you're trying to do involves high-speed op amps, Analog Devices is the company to call. With our current products and new introductions, we have the broadest line of high-speed op amps available. A line that gives you the right combination of speed, precision, noise and price. So chances are, we've got exactly what you need for

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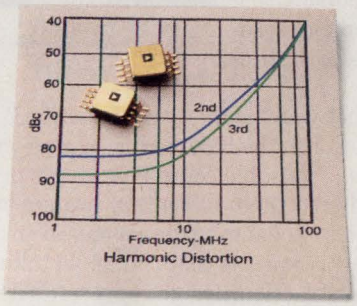
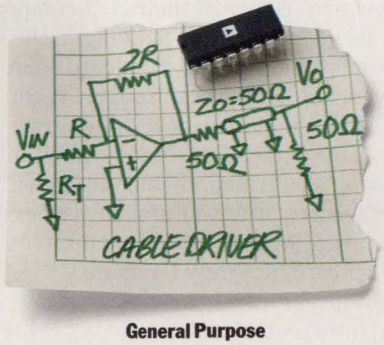
shoot it, launch it, land it, test it, display it or air it, we've got it.

high-speed op amps.



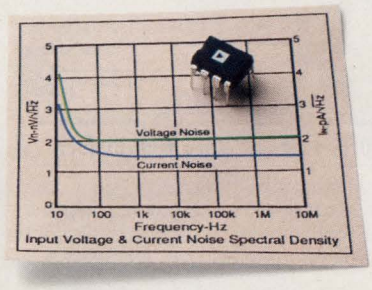
Buffers

If you're looking for extremely low distortion buffers, look at the specs of the AD9620 and AD9630 – distortion at 20 MHz: −73 dBc and −66 dBc, respectively; fast settling time: less than 8ns to 0.02%; and extremely low noise: 2.2 nV/√Hz.



General Purpose

With the right combination of speed, precision, power dissipation and high output drive capability, the AD827, AD829, AD847, AD848, AD849 and OP-64 are ideal general purpose solutions. And they're ideally priced solutions – most singles are under $3, and duals are under $5.



Low Noise

It used to be you had to choose between speed or low noise. But with the AD829, you get both. It features voltage noise of 2 nV/√Hz and current noise of 1.5 pA/√Hz with a 50 MHz unity-gain bandwidth. Those specs, combined with the low price of $2.95/100s, make it ideal for both audio and video applications.

whatever application you're working in. Call us at 1-800-262-5643, or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106, for a complete high-speed op amp selection guide and a *free copy of our SPICE model library.*

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CIRCLE 80

EDA Vendors Validate CFI Efforts

LISA MALINIAK
COMPUTER-AIDED ENGINEERING

A few years ago, serious doubts were raised on whether EDA vendors would rally around industry standards. Despite that sentiment, the CAD Framework Initiative (CFI) has spent the past year working on a set of three specifications that allow EDA tools to be integrated easily and effectively into a CAD framework. The specifications will be demonstrated at CFI's 1991 integration project next week during the Design Automation Conference (DAC) in San Francisco. In addition, several vendors will show prototypes of their CFI-compliant products. The project's success lies not only in the electronic-design-automation industry's ability to create framework standards, but also if it can support them.

CFI's theme for its 1990 integration project was "cooperation in action." It was a first attempt at large-scale standardization in the EDA industry, and was viewed as a trial implementation with lots of disposable code. This year's project focuses on a "real standards for real products" theme. The 1991 project has frameworks and tools from multiple companies exchanging data using the new specifications. Andy Graham, CFI's president, explains that the undertaking introduces entirely new capabilities for tool abstraction, design representation, and intertool communications. "Broad participation in the project enabled validation of many of the concepts in the specifications and accelerated the implementation of CFI specifications in commercial products." And the success of a standard, Graham points out, is market acceptance.

Tools from multiple vendors often can't work together effectively in the current, non-standardized situation. In fact, an end user typically spends more time making tools work together than they do with each individual tool. The three biggest problem areas involve access and modification of design information, adding tools to the design environment, and tool interaction in real time. CFI addresses these problems with a common data model, and tool-encapsulation and intertool-communication standards.

More than 22 organizations were enlisted to modify their tools for the newly developed specifications. According to project coordinator Paul Painter, a researcher at Microelectronics and Computer Technology's (MCC) CAD Framework Laboratory, Austin, Texas, the CFI specifications allow for true "plug-and-play" capability among the various participants. CAD vendors and users from North America, Europe, and Asia worked together to integrate 34 different software products using the same set of CFI-developed interfaces. Integration labs were established at MCC in North America, CADLab in Europe, and at Cadence and Mentor Graphics facilities in Japan to complete the project. Final integration of the tools took place over the past few weeks at MCC CAD Framework Laboratory.

The 1991 integration project consists of three parts. Part one focuses on uniform methods for integrating tools into a framework. The second part emphasizes a single way of representing design data, and the third part allows tools to communicate with each other in an open, non-proprietary fashion. Project participants supplied either a framework cockpit to control the tools, a design-representation server to store design information, or an application tool that produces or consumes net-list information.

Eight project participants will show CFI-compliant product prototypes at DAC. They are: Cadence Design Systems, Computervision, Mentor Graphics, Objectivity, Siemens Nixdorf, Sun Microsystems, Valid Logic Systems, and Viewlogic. Mentor's Mitch Weaver, the chairman of the Electronic Design Automation Companies (EDAC) standards committee, proclaims that "adoption of standards is the key enabler for growing the industry." Apparently, a good portion of the industry is starting to think that way.

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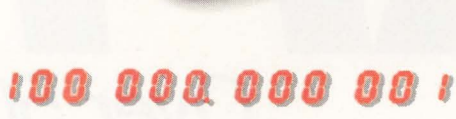

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CIRCLE 152

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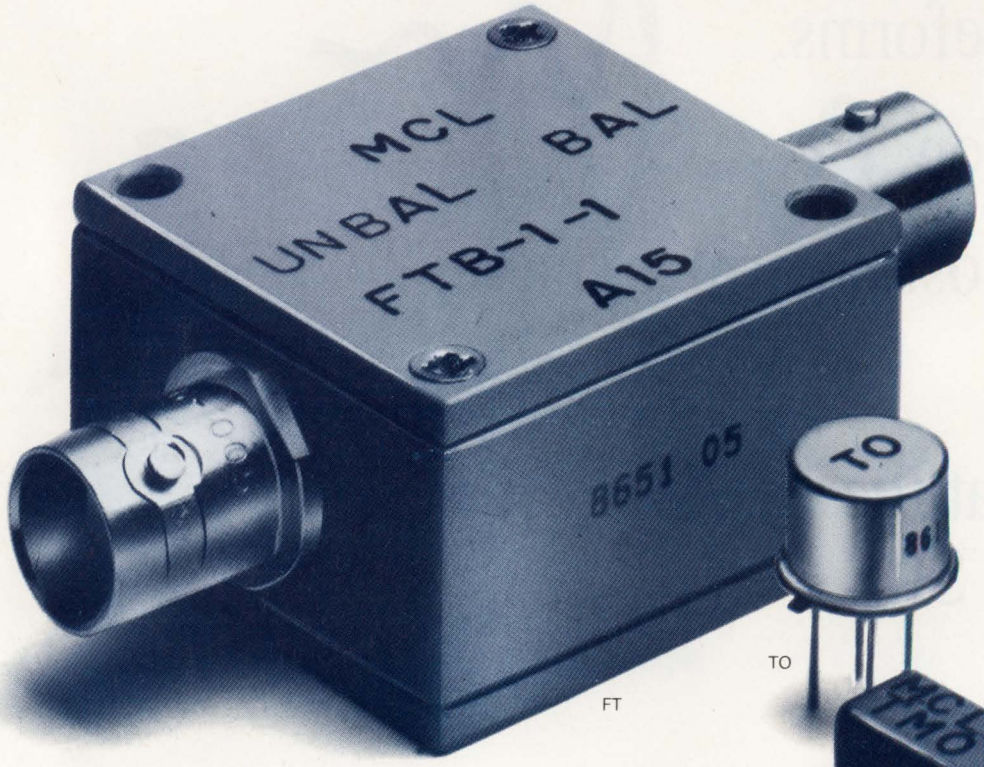

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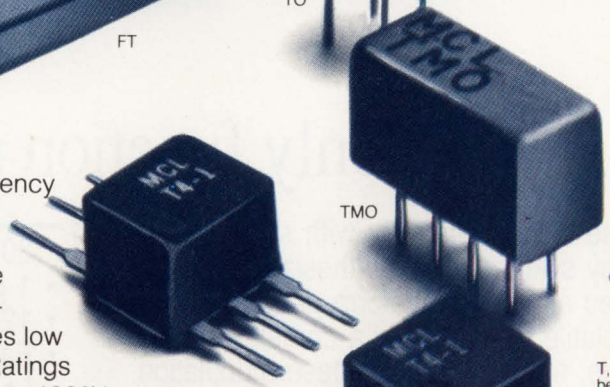
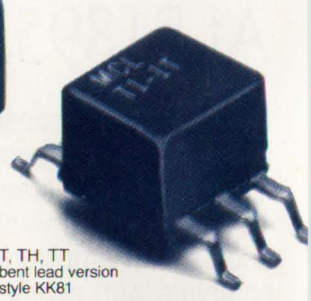
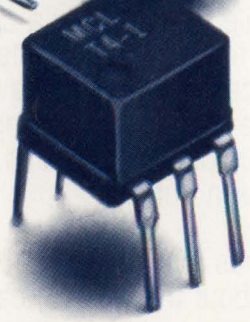


TMO

T, TH, TT



T, TH, TT
bent lead version
style KK81



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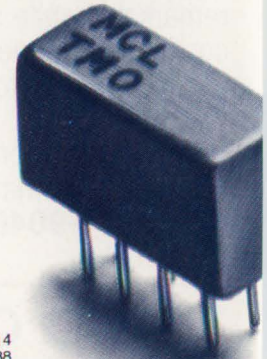

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TMO, case A 11, † case B 13 FT, FTB, case H 16
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MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
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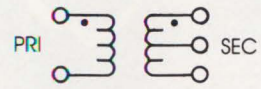
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
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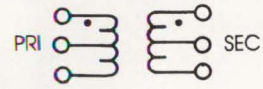
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
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		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
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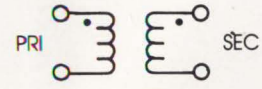
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
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		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
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		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
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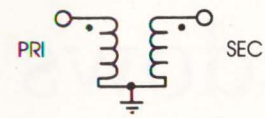
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
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		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
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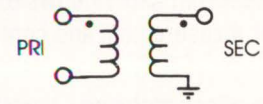
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
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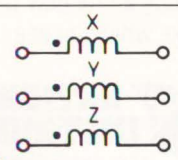
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
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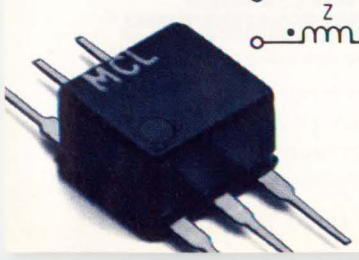

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CIRCLE 92

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CIRCLE 110

LOW-POWER CW LASER WRITES CIRCUIT LINES

A low-power, continuous-wave semiconductor laser diode has been used to directly write circuit lines in recently completed research. The laser is part of an additive dry-conductive-powder process for writing pc-board traces. Somich Technology Inc., Winnipeg, Manitoba, Canada, developed the process. The laser writes the circuit lines on the substrate directly from a CAD/CAM data base. A film of heat-activated adhesive is laid on a substrate and a layer of conductive powder is placed on the adhesive. With output powers as low as 55 mW, the laser defines the circuitry by activating the powder and adhesive. Significant advantages compared with other methods of defining circuit traces include the absence of artwork. In addition, 3D surfaces can have circuitry fabricated on them. There's a high repeatability factor as well as no resists or wet chemicals, which eliminates environmental concerns. Call (204) 694-7287 for more information. *DM*

SSI GETS SIGNETICS' 13-GHz QUBiC PROCESS

Through a licensing agreement, Silicon Systems Inc. (SSI), Tustin, Calif., can now access the proprietary QUBiC biCMOS fabrication process of Signetics Corp., Sunnyvale, Calif., for SSI's mixed-signal ICs. This submicron process, whose npn transistors provide an f_t of 13 GHz, is a true modular mixed-signal process, not just CMOS pasted on a bipolar process or vice versa. It combines high speed and density with low power, useful for building next-generation disk-drive read-channel ICs, a mainstay of SSI. The process should be particularly useful for future generations of the company's voltage-programmable, continuous-time filters, such as the year-old 32F8011 and the just-released 32F8020. Both are 7-pole, Bessel low-pass filters for disk-drive read channels using constant-density recording. The former can be programmed with digital-to-analog converters for a cutoff frequency between 5 and 12 MHz. The latter can be similarly programmed to cutoff anywhere between 1.5 and 8 MHz. The new process should make possible IC filters with useful frequencies that are at least a factor of three higher than what's achievable today. These filters, while now limited to disk drives, should have broad application in communication systems and equipment. For additional information, call 1-(800) 624-8999, ext. 151. *FG*

X-RAY STEPPER CRAFTS FEATURES UNDER 0.35 μM

X-ray lithography, which was long awaited as the means to produce the next generation of IC designs with feature sizes under 0.35 μm, has finally arrived in a commercially available production system. The Series 3500 stepper, from Hampshire Instruments Inc., Rochester, N.Y., is the first commercial appearance of a lithography technology that may eventually meet the 0.25- and 0.15-μm design rules needed for 1-Gbit memories. The system can be the foundation for a process line for new devices, or it can be mixed into existing optical-lithography lines. The mix-and-match capability stems from the fact that the X-ray system uses the same photoresist process as optical systems. Already onboard with the X-ray technology is Cypress Semiconductor, San Jose, Calif., which purchased the $4 million system with an eye toward volume manufacturing of sub-0.3-μm devices. *DM*

POWER, PACKAGES SHRINK FOR LCD DRIVERS

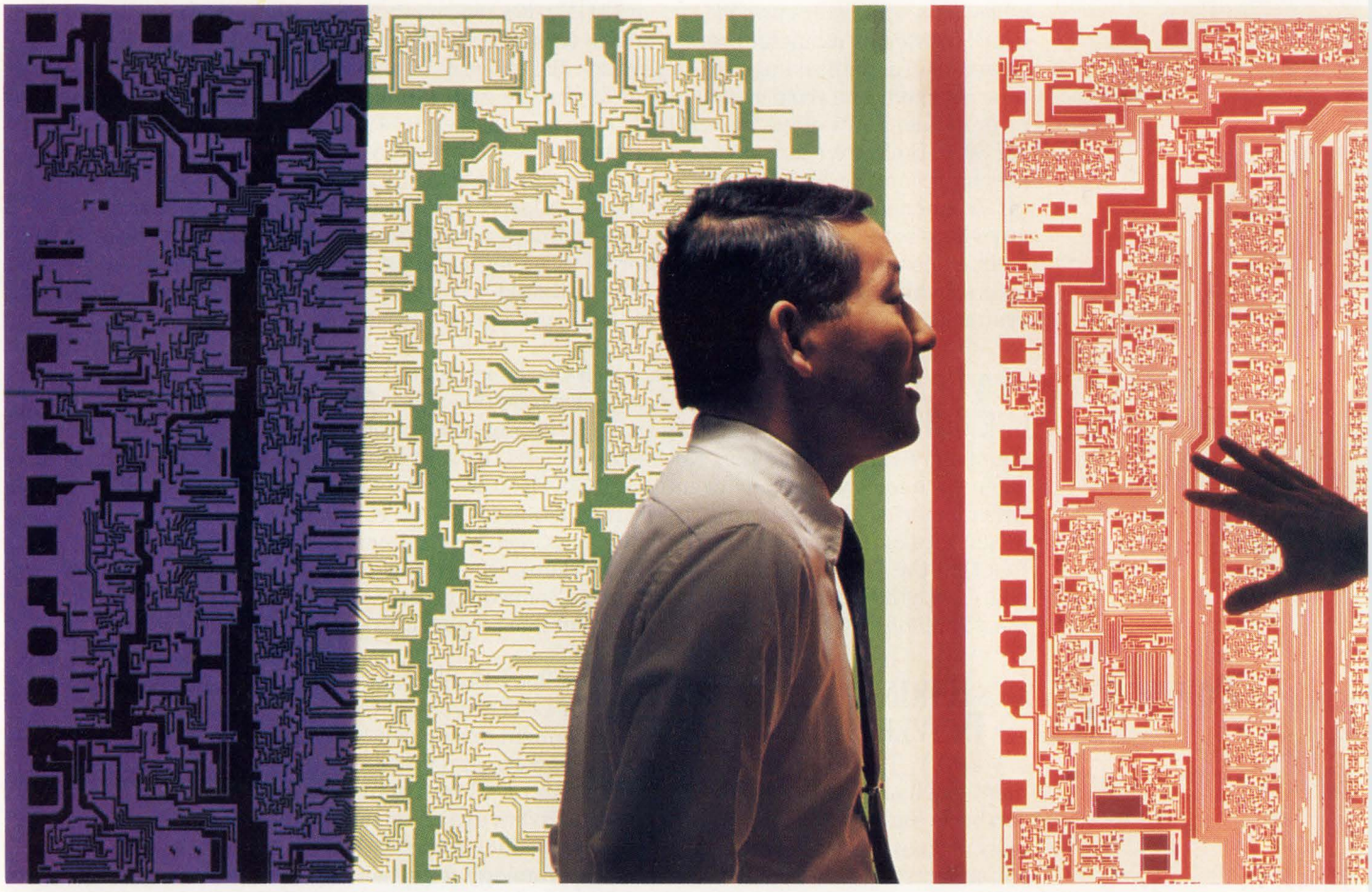
In separate developments, Sharp Corp., Osaka, Japan, reduced both the power consumption and size of LCD drivers. Two new devices, the LH1511 common driver and LH1512 segment driver, can operate from supply voltages as low as 3 V. These drivers fill the need for lower supply voltages in battery-operated equipment, such as notebook and palmtop computers. Clock frequencies for the segment drivers can be as high as 2.5 MHz. In addition, the drivers use an enable-chain scheme that automatically propagates signals to adjacent devices, reducing the load on the display controller.

Concurrently, Sharp developed a new technology with two key elements that combine to dramatically reduce the size of LCD drivers. One is an 8-mm-thick TAB package for the drivers that optimizes the wiring pitch of LCD panels by matching the chip's pad pitch to the outer-lead pitch. The other is a long, thin package profile with a width-to-length ratio of 1:10. The so-called bar chips feature an operating frequency of 6.5 MHz and the ability to drive a 1/240 duty cycle at LCD voltages of 28 V. *DM*

SGS READIES CLASS-0.1 FAB IN GRENOBLE

An ultra-clean, class-0.1 (less than 3.5 particles/m^3) fabrication facility is currently being built in Crolles, France (near Grenoble), by SGS-Thomson in a joint venture with CNET, France's telecommunications authority. Called "Grenoble 92," this "world-class" facility for submicron semiconductor technology will combine advanced-technology research laboratories with a compatible pilot production line for 8-in. wafers. Feature sizes will be as small as 0.3 μm. Grenoble 92 is expected to be fully

How to ge customs witho



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Circle 112 for Career Info

operational with 0.8-μm feature sizes by the end of 1992.

The facility will be devoted to developing digital and mixed-signal CMOS, as well as complementary biCMOS, ICs. Mixed-signal circuits will be based on SGS-Thomson's modular, complementary, 1.2-μm biCMOS process. With 0.8-μm feature sizes, npn-transistor f_ts are expected to be greater than 10 GHz, and pnp-transistor f_ts greater than 3 GHz. Digital-IC line widths are estimated to reach 0.35 μm, while the mixed-signal CMOS and biCMOS devices will stop at 0.5 μm. The facility replaces air 500 times per hour. Its temperature is held at 23°C $\pm$0.1°C, and humidity at 40%, $\pm$2%. Vibration is less than 3.15 μm/s from 5 to 30 Hz. Clean-room cells are pressurized to 50 Pascals above ambient to prevent particle entry. Pressure is maintained when cell doors are opened to prohibit air movement. Electromagnetic interference is kept below 3 milligauss so that electron-beam equipment can be used. *FG*

JEDEC Task Force Eyes Package Standards

With spiraling system speeds, semiconductor-package and connector parasitics are of growing concern to designers. With that in mind, JEDEC, Washington, D.C., has formed a task force to identify these parasitics. It will then standardize terms and definitions, and test conditions, models, and procedures. The group comprises members of existing JEDEC committees on package standardization, memory standardization, ASICs, and gallium arsenide. For more information, contact Carl Cook at (415) 857-7470. *DM*

Software Simplifies System Diagnostics

A complete system analysis, including fault isolation down to the component level, is now possible using QAPlus 4.52 diagnostic software from Diagsoft Inc., Scotts Valley, Calif. The software, which simplifies system diagnostics, allows designers to display the options for correcting identified faults. The self-booting software supports all DOS systems as well as Intel 8086-based OS/2, Unix, and Xenix systems. Included in the latest version of QAPlus is Intruder Alert, which detects a computer virus before it can spread to other systems. It also includes User Installable Diagnostics, which lets users run other diagnostic tests from within QAPlus, then display the results on-screen in dialogue boxes. In addition to CPU, advanced memory, keyboard, and video tests, the software supplies system and hardware configuration information so that I/O devices can be added and configured without any conflict from other devices. *RN*

Multichip-Module Pact Promises Lower Costs

Although multichip-module (MCM) technology is making inroads with workstation manufacturers to combat propagation delays inherent in IC packaging, the technology's cost has kept desktop-system makers at arm's length. To that end, nCHIP Inc., San Jose, Calif., and Sumitomo Metal Mining Electronics, Tokyo, Japan, are teaming up to lower the cost and improve the volume manufacturability of the core technologies used in MCMs. Two targeted areas in the technology agreement are the development of low-cost, non-hermetic packages—a key in cost reduction—and refining key processes critical to high-volume manufacturing of substrates. With the aid of Sumitomo's expertise in copper electroplating, the companies will work toward a means of attaching the modules' leadframes directly to their silicon substrates, which eliminates a wire-bond interconnect level and makes manufacturing simpler. In addition, Sumitomo, which is a leading maker of TAB tape, will push to develop a high-density tape that will complement nCHIP's existing capabilities in wire-bonding and flip-chip assembly techniques. For more information, call Steve Stephansen at (408) 945-9991. *DM*

USAF Contracts MCC For Module Coatings

A revolutionary change in packaging technology—replacing hermetic packages with more cost-effective, lightweight protective coatings for multichip modules—is the goal of a $4 million, four-year research effort. The U.S. Air Force's Wright Laboratory has awarded the Reliability without Hermeticity (RwoH) research contract to the Microelectronics and Computer Technology Corp., Austin, Texas. The joint industry-university-military initiative will investigate the advantages of organic (polymeric) and inorganic coatings, and seeks to eventually gain their acceptance in electronics for military systems, as well as for broad commercial applications. *DM*

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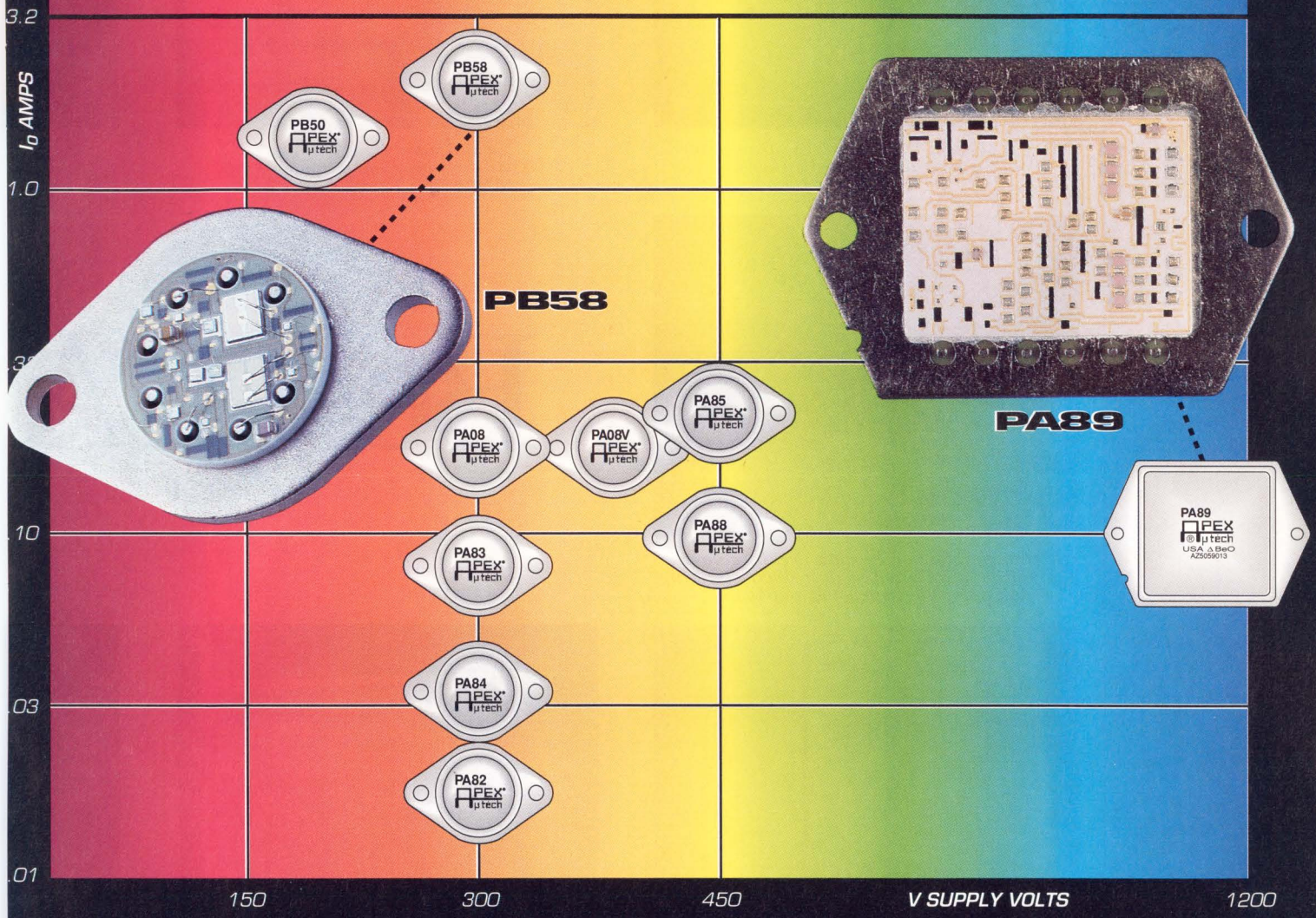

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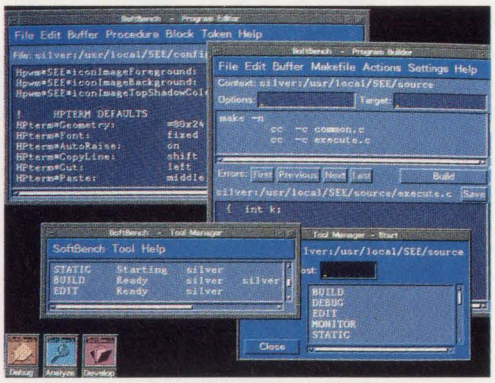
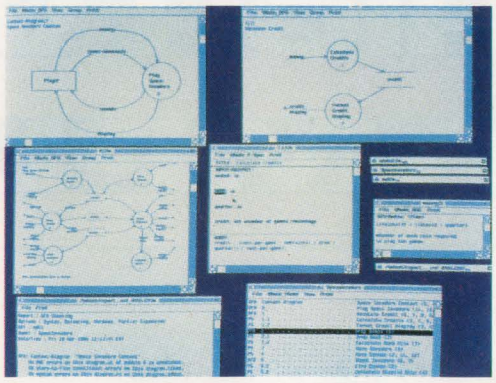
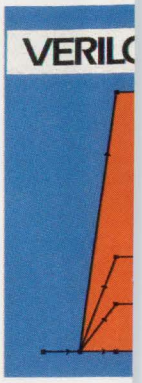
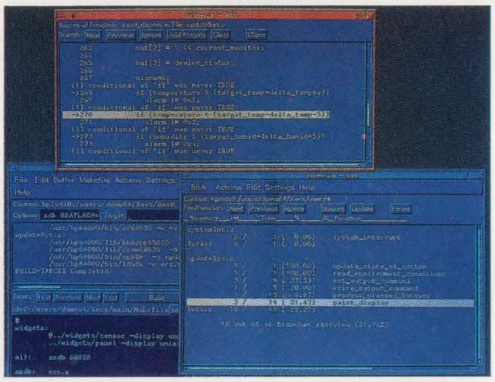


HP's SoftBench: A tool integration framework and a program construction toolset.



Cadre Teamwork: A family of tools that implement system analysis and software design methodologies.





HP Branch Validator: Provides accurate branch information quickly and easily, reducing software test time while increasing confidence.

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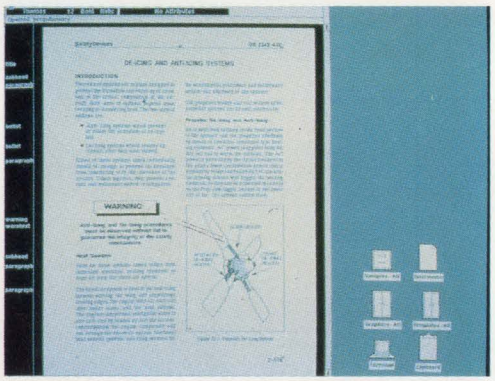
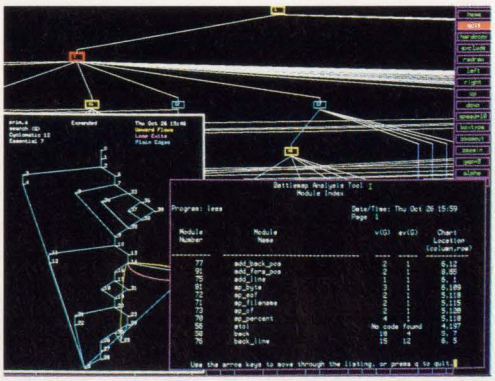
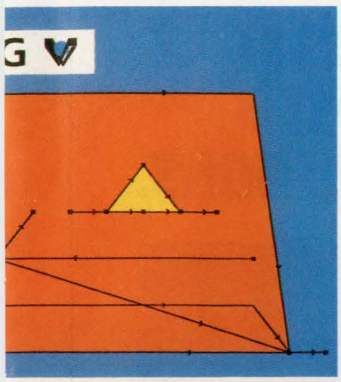


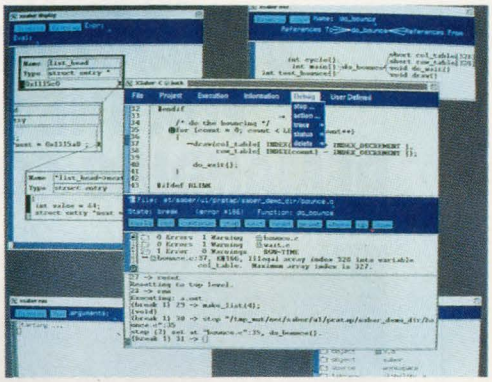
Interleaf Technical Publishing Software: A documentation software and management system that features integrated text and graphics.



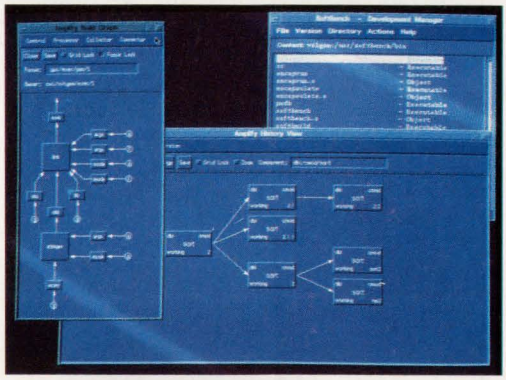
McCabe Test Tools: An automated software testing and reverse engineering application.



Verilog LOGISCOPE: Automated testing of source code analysis for reverse engineering.



Saber-C: A set of integrated tools for development, testing, maintaining and debugging C programs.



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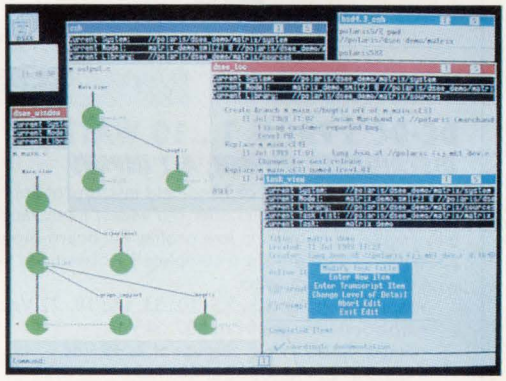

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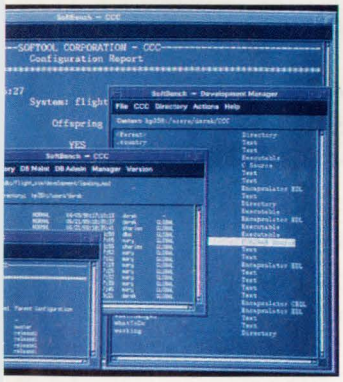
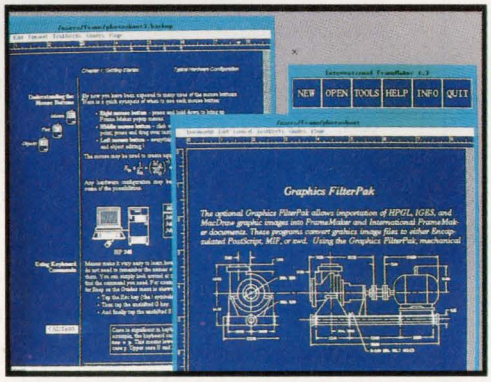


Softool Corporation CCC: A complete, automated solution for change control and configuration management.



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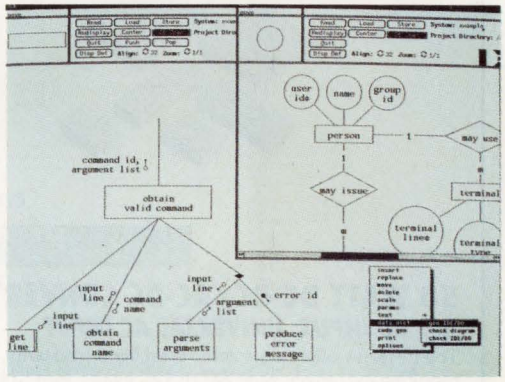

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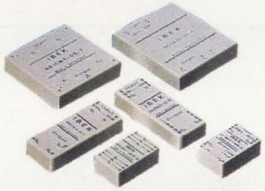

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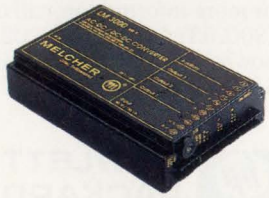

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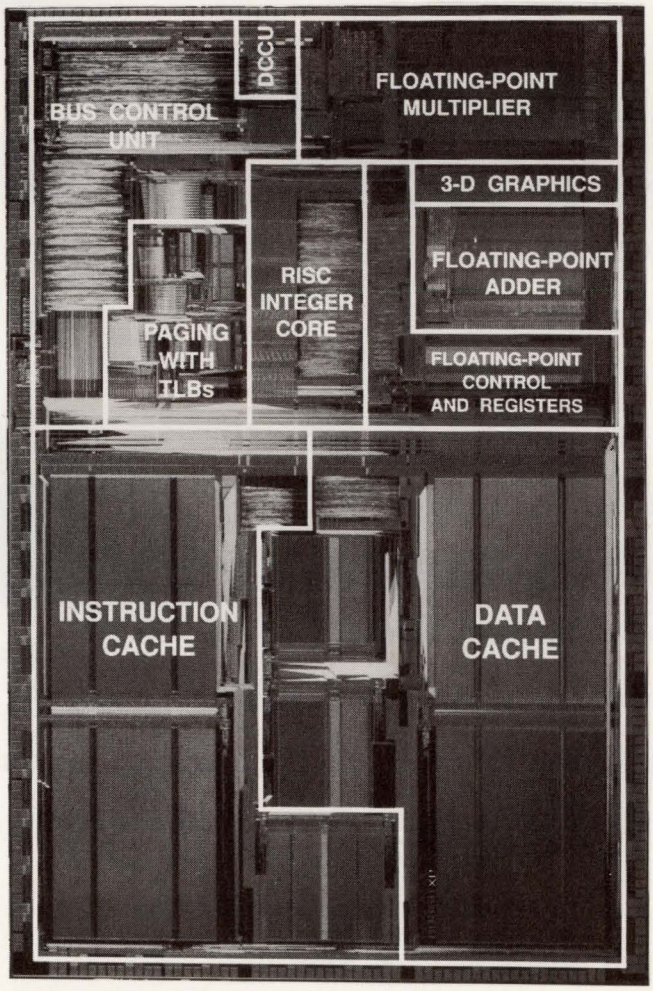
MULTIMILLION-TRANSISTOR BUDGET DELIVERS SUPERCOMPUTER-LIKE CHIP

The latest advances in semiconductor processing have "promised" to give designers more transistors per chip than they know what to do with. But that really hasn't been the case, because most chips are interconnection-limited when they employ just two levels of metal interconnections. However, a combination of three levels of metal and a 0.8-μm CMOS process gave designers at Intel Corp., Santa Clara, Calif., the flexibility and integration levels they needed to pack over 2.5 million transistors onto the latest high-end member of its i860 family, the 860XP.

With the CPU's transistor count more than doubling, Intel's designers knew exactly what to do with the transistors. First, they upped the amount of on-chip cache from 8 kbytes to a total of 32 kbytes, split evenly between independent instruction and data caches *(see the figure)*. The tight packing permitted by the triple metal layers and the submicron processing enables the chip to operate at clock frequencies of 40 to 50 MHz. At the 50-MHz clock rate, the chip delivers a compute throughput of 100 MFLOPS and about 50 MIPS. Wide 64-bit buses give the chip a bus bandwidth of 400 Mbytes/s—a speed approaching the I/O-channel rates of most supercomputers.

In addition to including more memory, the designers enhanced the floating-point and graphics units and fixed several of the perceived shortcomings of earlier i860 family members. First, they shrunk the invalidated cache block from 8 kbytes on the original chip to one cache line, reducing the replacement time. The chip also contains a burst-transfer mode on the bus so that line fills can occur at 50 Mwords/s (64-bit words). Additional support for page-mode dynamic RAMs allows the chip to operate with relatively inexpensive memory. The 860XP's better caching and improved bus I/O speed enable it to execute software 30 to 40% faster when running at the same clock rate as previous 860-family members.

The CPU also includes support for multiprocessor systems—bus snooping hardware and cache-coherency logic are built into the CPU. Included in the on-chip MMU are both virtual and physical tags. In the previous family members, misses in the translation-lookaside buffer limited chip performance because large data structures were used. To remedy the situation, a 4-Mbyte page size was created with just one level of translation on the chip. As a result, the TLB can cover 64 Mbytes with just 256 kbytes of actual space.

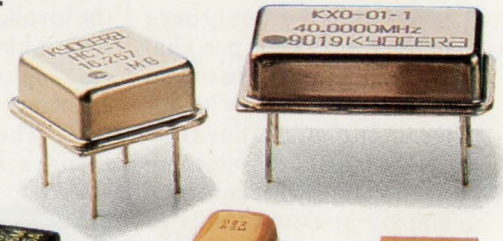


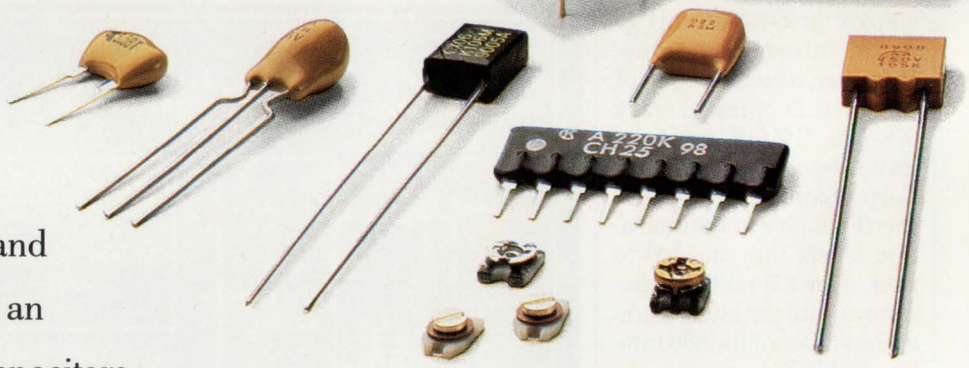
With the virtual tags, external accesses can be started very quickly—just a two-cycle penalty is imposed if a cache miss occurs. The snooping mechanism helps maintain valid cache data. It can invalidate a line and write data back to the external memory. The logic also checks for virtual aliasing to avoid unnecessary cache flushes, solving the context-switching problem associated with the 860 family. Furthermore, more trap information is kept on chip, reducing the amount of decoding needed and improving program throughput.

Sustained performance of 100 MFLOPS is possible thanks to a pipelined floating-point-register arrangement that uses a three-word-deep FIFO. New instructions enable the structure to be used more efficiently with a sort of burst load into the FIFO with a quad-word load command. As with previous family members, the new high-end XP is totally binary-compatible with the other CPUs. The high-performance floating point will greatly improve the chip's overall performance in 3D imaging and graphics applications. Some typical benchmark numbers (simulated at this point) give the 50-MHz chip a Specmark rating of 40.4. The floating-point Specmark rating is 51.1, and the double-precision Linpack rating is 20 MFLOPS.

To support larger caches, Intel developed three additional chips: a cache controller (the

AVX would like to about their expanded product line.





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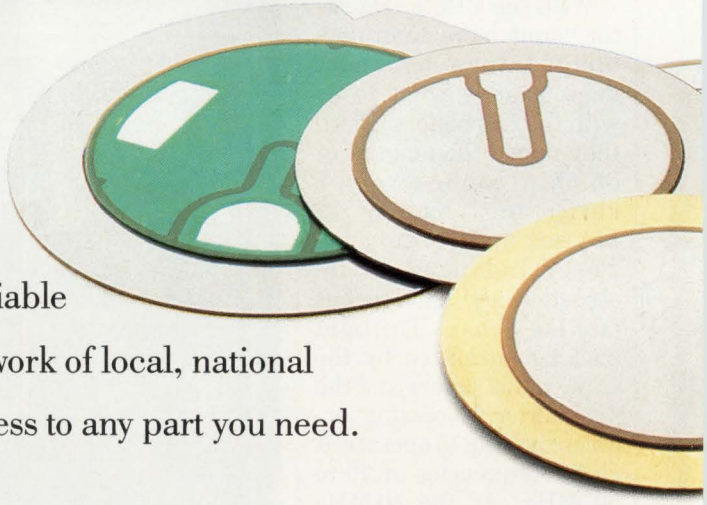

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CIRCLE 124

ng. Tick. Hum."

82495XP), a cache RAM (the 82490XP), and a multiprocessing interrupt and concurrency controller (no part number assigned yet). Together, the three chips along with the 860XP form a multiprocessor, parallel-processing system. The cache controller supports write-back and write-through cache operation with memory sizes from 128 to 512 kbytes. On-chip logic supports both bus snooping and the MESI protocol to readily handle multiprocessor-system designs. The memory-bus interface can be 64- or 128-bits wide, and synchronous or asynchronous. When combined with the 32-kbyte cache RAMs, the cache subsystem diminishes the CPU's use of the main memory bus to less than 15%, thus allowing more bus time for additional CPUs or other hardware.

The cache RAM is not an ordinary high-speed RAM: It is dual-ported and has an on-chip write-back buffer to minimize the bus turnaround time when the CPU writes to external memory. To ensure data integrity, the RAM also includes parity and a self-test mode, so that the chips can test themselves upon system initialization.

Coordinating the CPUs and multiple caches is the multiprocessing interrupt and concurrency controller. The chip actually contains two main function blocks. One block is the multiprocessing interrupt controller. It provides a scalable distributed interrupt architecture that supports up to 256 interrupt vectors. The other block is the concurrency control unit, which is supported by the PAX compilers. This unit provides efficient loop parallelism via code synchronization and serialization, good for iterations with little or no dependencies. The interrupt controller creates its own localized interrupt bus, which can be likened to a packetized bus that transfers small packets of data.

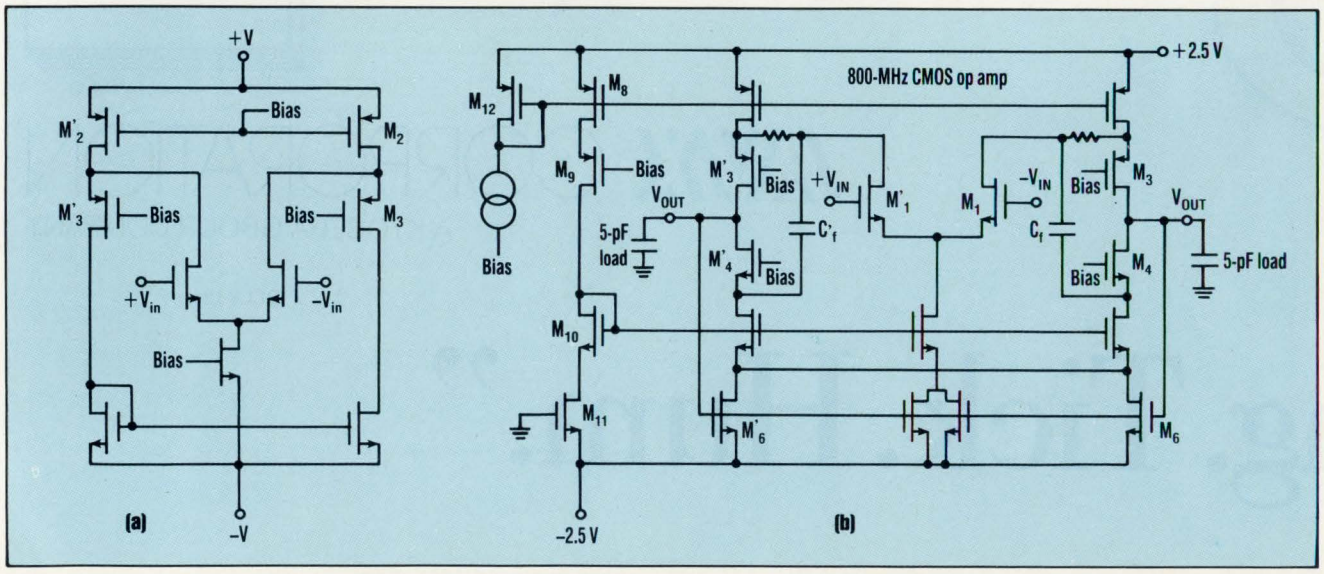
DAVE BURSKY

DIGITAL 1.2-μM PROCESS YIELDS CMOS OP AMP WITH GAIN BANDWIDTH OF 800 MHZ

Op amps built on typical analog CMOS processes with 3-μm and larger geometries are known for low bias and quiescent currents, not for speed and bandwidth. However, fine-line digital CMOS processes can now offer both speed and bandwidth. For example, the cutoff frequency (f_t) of an n-channel MOSFET fabricated on a 1.2-μm digital process can run between 3.5 and 4.5 GHz. As a result, some IC designers are now investigating the potential of putting a few wideband analog circuits on a high-speed digital CMOS chip. F. Op't Eynde of Mietec Alcatel, Brussels, Belgium, and W. Sansen of the Katholieke University of Leuven in Belgium described the results of just such an adventure in techical presentations at the recent Custom Integrated Circuits Conference (CICC) in San Diego, Calif. They designed and built a unity-gain-stable op amp sporting a gain bandwidth of 800 MHz.

Many CMOS op amps employ what is called a folded-cascode architecture in a fully differential configuration for optimum gain and bandwidth *(see the figure, a)*. For stability, when run at a closed-loop gain of unity, the nondominant pole of this circuit (or any op amp) must be well beyond the desired bandwidth. This means the circuit's transistors must have cutoff frequencies that are significantly higher than the pole's frequency. However, in this folded-cascode circuit, the relatively large parasitic capacitance of the p-channel MOS transistors—M_2, M'_2, M_3, and M'_3—locates the pole at about 1 GHz.

To move the pole to a higher frequency (by eliminating p-channel MOS devices from the high-frequency signal path), the designers bypassed the devices with a capacitive



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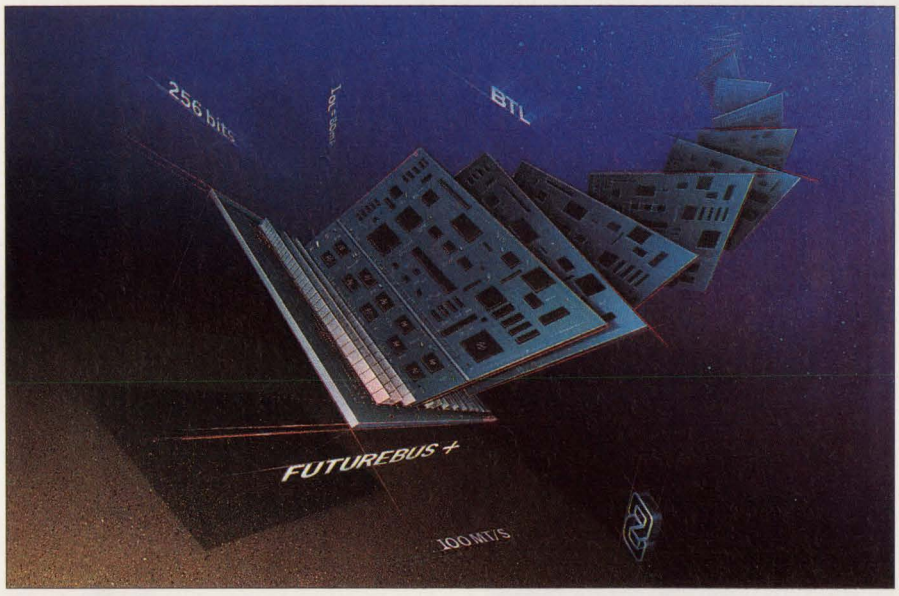

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INTRODUCING the newest group of Brooktree IC's for image-conscious designers. They add to our rapidly growing family of Image Technologies components. And they underscore the reasons why it makes sense to make Brooktree your prime resource for graphics and imaging power.

We've got IT together, looking at graphics and imaging from a systems architecture point of view. That means chips that work together to simplify your design task. That's IT!

IMAGE RECEPTION. We've got chip sets to send and receive true-color digital video using an 8-bit interface. Our Bt294 CCIR 601/SMPTE RP 125 Decoder works with our upcoming Bt297 ECL-TTL Translator for a complete solution to 4:2:2 digital component video.

WHAT

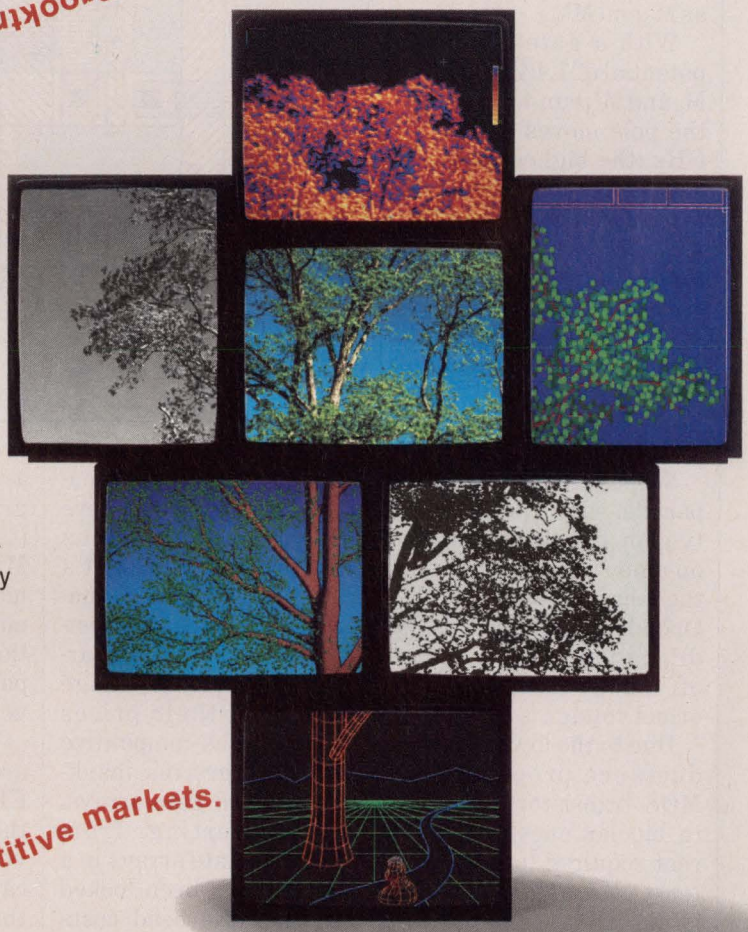
Brooktree has got IT: Image Technologies. It's our system-smart approach to packing image acquisition, manipulation,

send it and receive it as live color video then display it in high resolution true-color / and do it all with Brooktree's Image Technologies. They make it easy to give your PC or WS design a visual edge in today's competitive markets.

IMAGE TRANSMISSION. We did say complete solution, didn't we? The Bt291 CCIR 601/SMPTE RP 125 Encoder teams with the upcoming Bt296 TTL-ECL Translator to provide cost effective 4:2:2 digital component video transmission without adjustments or support circuitry. In combination with the Bt294/297 reception devices, they make it easy and economical to add point-to-point video transmission to your multimedia system.

IMAGE PRESENTATION. When it comes to display technology, we're where IT's at: We revolutionized RAMDACs. Now we're setting a new performance standard for super VGA, high-end XGA, 8514/A, TIGA compatible and x. terminal applications. It's the Bt484 true-color RAMDAC.

Its programmable pixel depth means you can run at 4 bits/pixel with 8:1 multiplex, 8 bits/pixel with a 4:1 MUX, 16 bits/pixel at 2:1 MUX or even 32 bits/pixel for 24-bit true color and 8-bit VGA. And its 32x32x2 three-color, user-definable cursor is absolutely awesome.



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IT IS.

transmission and presentation into highly-integrated, tightly-linked chip sets. Brooktree®

feedforward path via C_f and C'_f *(see the figure, b)*. The signal's high-frequency components are then amplified by the n-channel MOSFETs, M_4 and M'_4, and passed to the outputs. At this point, they're mixed with the signal's low-frequency components that are amplified by the p-channel FETs, designated as M_3 and M'_3.

With a gate-to-source potential of 1.4 V, the f_ts of M_4 and M'_4 run 4.7 GHz and the pole moves out to 1.7 GHz (the highest possible value from the fabrication process). Transistors M_6 and M'_6 form a common-mode feedback circuit, while M_8 through M_{12} generate the bias voltages. Running at a gate-to-source voltage of 1.1 V, the f_ts of the input FETs, M'_1 and M_1, run 3.7 GHz.

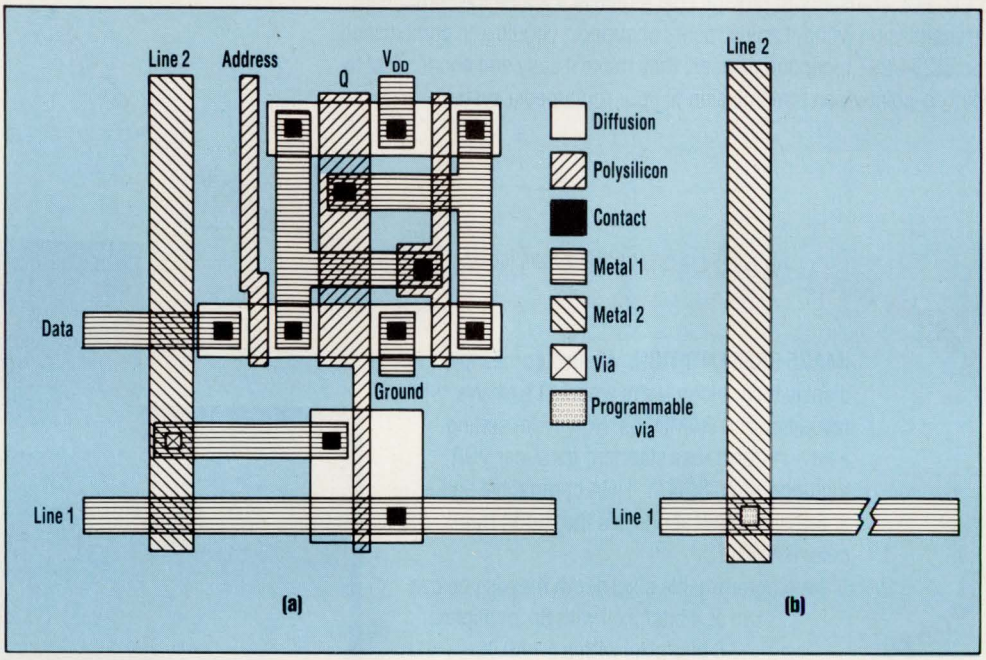
While driving 50 Ω in parallel with 5 pF, the unity-gain bandwidth of the op amp runs 800 MHz and the phase margin is 53°. Open-loop gain at dc is 39 dB, output swing running off ±2.5 V is ±0.8 V, and offset voltage is 5 mV.

Due to the low transconductance properties of MOS transistors (relative to bipolar ones), the current required (per transistor) to get wide bandwidth is significantly greater. The amplifier's core dissipates 180 mW of power, and the bias circuitry another 80 mW of power, for a total current requirement of about 50 mA.

The circuit was built on a single polysilicon, double-metal, 1.2-μm CMOS process. The feedforward capacitors are of the typical polysilicon-oxide-diffusion variety available on fast digital CMOS processes.

FRANK GOODENOUGH

HARDWIRED FPGAS TRIM SYSTEM COSTS ONCE PATTERNS ARE FIRMED UP



Although high-density field-programmable logic chips give designers tremendous flexibility, they do so at a price. In low-volume situations, FPGAs can be cost-effective versus gate arrays. However, as usage increases, their prices cease to be as competitive with smaller-area mask-programmed gate arrays. But converting from FPGAs to gate arrays in a design that's been locked can raise overhead costs and may require costly redesigns. To avoid these pains, Altera Corp. and Xilinx Inc., both in San Jose, Calif., created mask-programmed versions of their FPGAs that can trim component cost without redesign or significant conversion-overhead costs.

The Altera approach has been boiled down to an automatic process that employs the company's Max+Plus II logic design tools. It allows a five-week turnaround for mask-programmed replacements to its UV EPROM-based Max-family chips. The mask-programmed chips maintain pin-to-pin functional and ac timing compatibility to make the conversion very easy.

The difference in chip area, though, between the EPROM-based version and the simpler masked-ROM version is minimal, because EPROM cells aren't that much larger than the ROM cells. However, more area savings can be had by removing the programming logic. The simplified non-EPROM process flow also makes manufacturing easier, reducing chip cost.

The conversion also includes the ability to automatically generate test vectors that guarantee test-fault coverage to be greater than 95%, without significant effort by the designer. Cost reductions of as much as 90% can be obtained for large-volume requirements over the pricing of the UV EPROM-based Max chips. A nonrecurring engineering charge of about $15,000, however, must be amortized over the production run to come up with the actual cost. The company estimates that the mask-programmed approach will be most cost-effective when usage volumes of any configuration hit 10,000 or more units.

The area of the RAM-based Xilinx logic-cell-array (LCA) FPGAs will shrink considerably when converted to mask-programmed equivalents. That reduction is possible because ROM cells are significantly smaller than the RAM-based configuration cells. The bit values represented by the RAM cells *(see the figure, a)* were replaced with mask-programmed via connections

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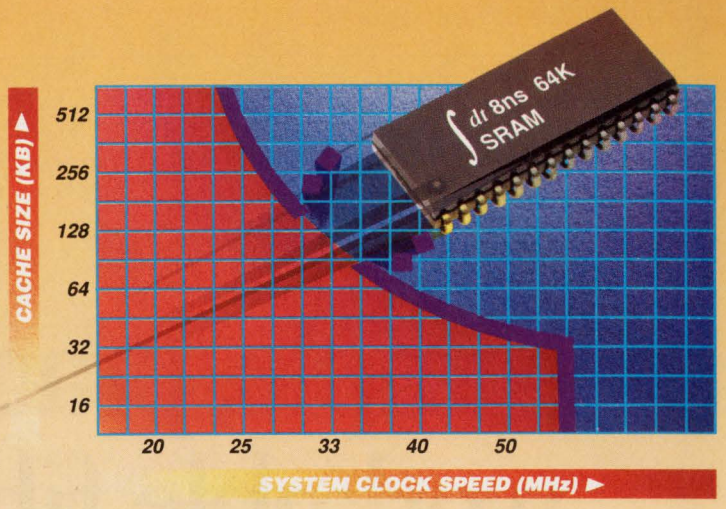

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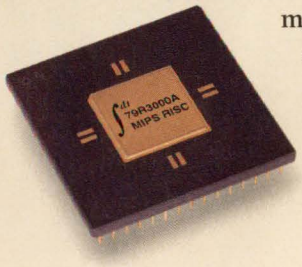

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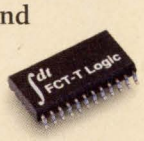

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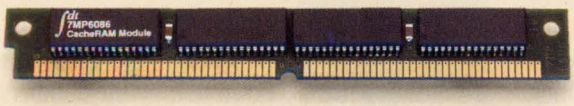

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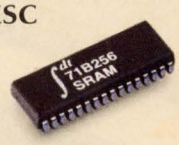

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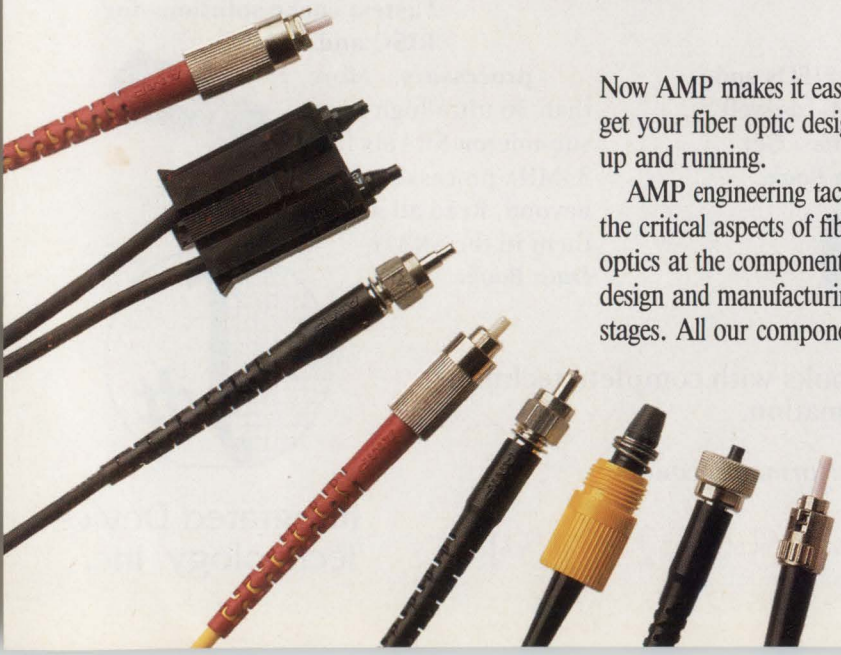

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AMP Interconnecting ideas

CIRCLE 113

between the first and second levels of metal interconnections *(see the figure, b)*. The presence or absence of a connection defines the circuit.

In the LCA, a typical configuration cell employs a 5-transistor RAM cell plus a pass gate for every programmable interconnection point—14,000 to 64,000 such points exist on each LCA chip.

By hardwiring the connection, every element associated with the configuration cell can be eliminated from the chip, bringing the cell's area down to only a fraction of the RAM-based cell's size.

As a result, chip area will come down dramatically, more chips can be fabricated on one wafer, and yield margins should increase. All of those factors should go a long way towards lowering the chip cost. The masking process is also simpler than that for gate arrays, the latter requiring 2 to 5 custom mask levels. In contrast, the simplified configuration cell that results from the HardWire inter-metal via creation lets chips be configured with just a single mask layer for customization.

One issue that might be raised with the ROM-based chips is their ability to directly drop into sockets employing the RAM-based versions. This is more critical for Xilinx than for Altera because the LCAs often load their configuration pattern from an external memory. That means the ROM-based LCA may have to emulate the loading procedure even though the configuration bits are being ignored.

Special circuitry was included on the HardWire chips to make the memory control and programming pins react as if the chip were a RAM-based array, even in cases when multiple LCAs are daisy-chained together.

Testability was also given special attention by Xilinx designers, who included boundary-scan test capability into their chip and created automatic test-generation software that can create design-specific vectors and achieve 100% fault coverage.

Ac performance is tested under two independent methods. In the first, an embedded inverter chain is tested under worst-case conditions during final test. The test chain uses one inverter from each of the LCA's configurable logic blocks, giving a sample speed from each cell of the chip.

The second ac test method uses the scan-path registers that were also used for functional testing. The registers are loaded and driven at high frequency. If any part of these devices is slower than what's called for in the specifications, the part will break the chain and cause a functional failure.

DAVE BURSKY

AUTOMATIC ON-LINE INSPECTION AND REPAIR BOOSTS LCD PRODUCTION YIELD

Pocket TVs, high-definition TVs, personal laptop computers, and workstations all benefit from the high information content of active-matrix, liquid-crystal display (AMLCD) screens. AMLCDs are brighter, have more contrast, and possess quicker response times than older direct-multiplexed, simple-matrix LCDs. However, the same complexity that provides these advantages causes high metallization defect rates, low yield, and thus high cost. These problems may now be eased by a promising in-process inspection and repair technique developed by Photon Dynamics Inc., San Jose, Calif.

An AMLCD panel consists of a thin-film-transistor (TFT) array fabricated on a large glass substrate called the "active plate." The number of TFTs used can exceed 1 million, and the process area can be as large as 350 cm^2. This is a formidable yield challenge even to makers of VLSI and ULSI semiconductors. Building redundant transistor rows or columns isn't viable because the display is visual to the user and no pixels can be duplicated.

The new technique is an extension of inspection methods that use light to measure high-frequency electrical phenomena. Applying a patented 2D electro-optic modulator to the LCD panel produces surface potentials that can be measured with a spatial resolution of about 30 μm and a voltage resolution of under 100 mV. A noncontact sensor scanning the active plate detects surface-potential variations representing point and line defects.

This data is entered into a defect file in a computer that creates a map showing the location and type of defects. Based on the failure signature for AMLCD processes, the technique can also identify defect type, such as short-to-gate, short-to-data, and opens. An automatic display-repair operation uses this information to convert defective or marginally bad displays into functional units.

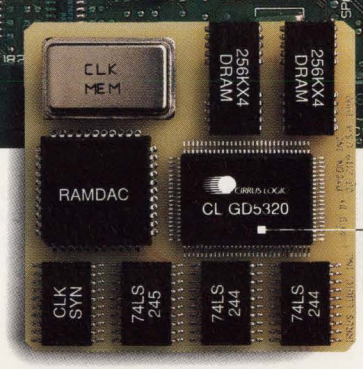
Automatic repair is based on a computer with image-processing capability and equipped with a recipe for laser-cutting and deposition operations for every type of defect. The repair-operation sequence for each defect is programmed into the repair system based on fabrication process, topology, and yield-loss data. Although laser-cutting operations are relatively straightforward, conventional deposition techniques are ruled out for automatic repair. This is because of the high system complexity coupled with low writing speed (about 1 to 5 μm/s) and the need for an operator.

The Photon Dynamics approach first uses a laser to open contact holes in passivation or other layers. A conductive film, which dries up in a few seconds, is then deposited automatically onto specific areas on the display. Next, another laser with a 3- to 10-μm spot diameter writes the metal line with a speed of about 300 μm/s. Such a speed is two orders-of-magnitude faster than a conventional photolytic process.

MILT LEONARD

VGA Get On Board.

Introducing VGA that fits your motherboard and your budget.



To put VGA graphics on your motherboard, you need a cost-efficient, highly integrated, powerful solution that uses minimal board space. You need the new CL-GD5320 Enhanced VGA-Compatible Graphics Chip from Cirrus Logic.

Use it to incorporate full 16-bit or 8-bit VGA into low-cost personal computers. You only need two industry standard 256K x 4 DRAMs and as few as five other ICs. Whatever memory speed you select — 80ns, 100ns, or 120ns — you'll get a complete VGA display system with greater performance than systems using a more expensive solution with 64K x 4 DRAMs.

You don't sacrifice features. You get 16-bit and 8-bit support for the VGA graphics standard, and full, register-level backwards compatibility. For maximum performance, it has an 8/16-bit CPU interface, independent video and DRAM clocks, internal FIFOs, and page mode DRAM access. And it will interface to both analog (PS/2 and multi-sync) and TTL monitors.

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This full 16-bit CL-GD5320 lets you implement 16-bit or 8-bit VGA capabilities on your motherboard with as few as 5 other chips and two 256K x 4 DRAMs. Get a complete solution that saves time, space, power, and expense. You still get all the speed, features and flexibility you're looking for.

CIRRUS LOGIC

C L O S I N G T H E G A P

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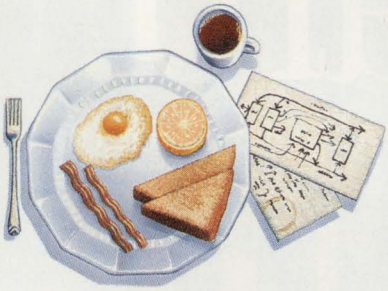
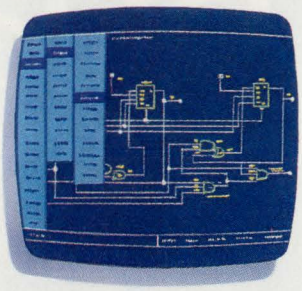
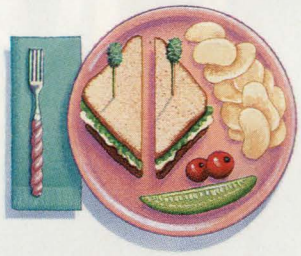


7:05 am: Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am: Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am: Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm: Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

Actel Field Programmable Gate Array Systems.

They're a feast for your imagination.

Actel's ACT™ 1 arrays bring you a completely new approach to logic integration. Not just another brand of EPLD, PAL® or LCA™ chips. But true, high density, desktop configurable, channeled gate arrays.

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And do it in hours instead of weeks. Even between meals.

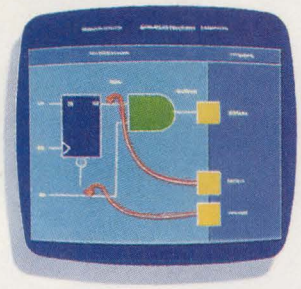
How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most

Actel FPGA Product Family		1010A	1020A
Equivalent Gates	Gate Array	1200	2000
	PLD/LCA	3000	6000
User I/O		57	69
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

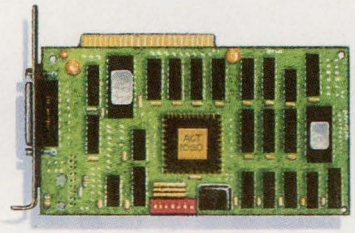
CIRCLE 109

Breakfast And n By Dinner.

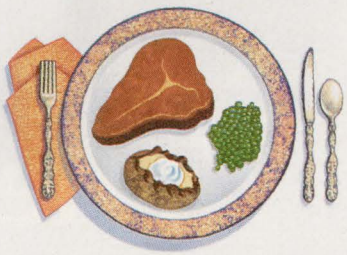
1:15 pm: Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a very quick coffee break while your design becomes a reality.



1:25 pm: Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



4:00 pm: Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished way ahead of schedule! Better think of something to do until 5:00.



6:00 pm: Dinner
Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

tedious part of the job by hand.

Design verification is quick and easy with our Actionprobe™ diagnostic tools, for 100% observability of internal logic signals. Guaranteed. So you don't have to give up testability for convenience.

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Actel

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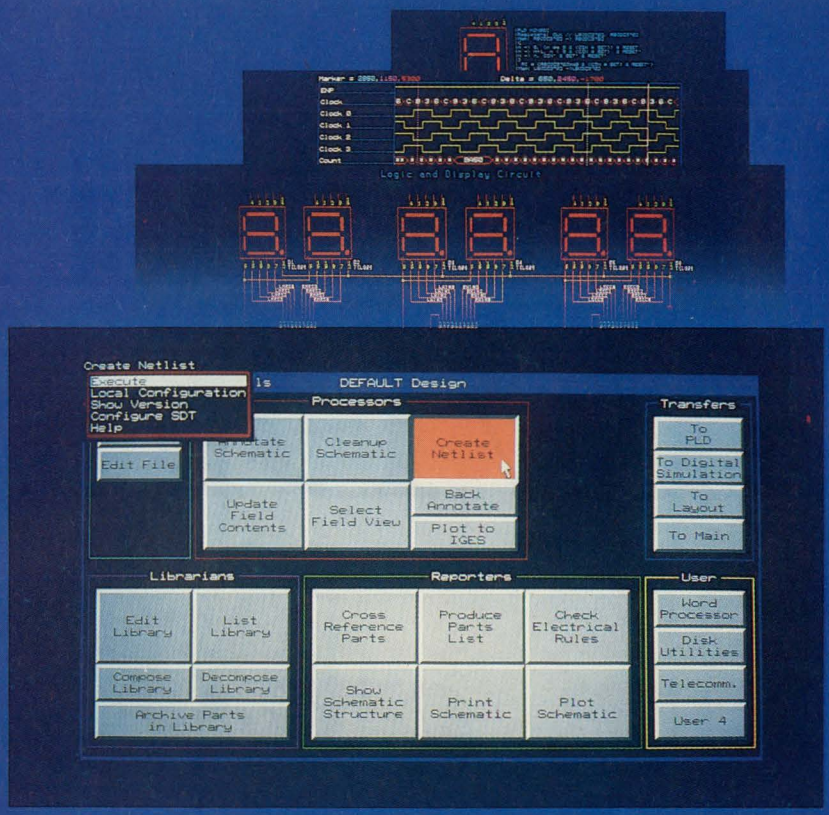
OrCAD presents

Release IV



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CIRCLE 97

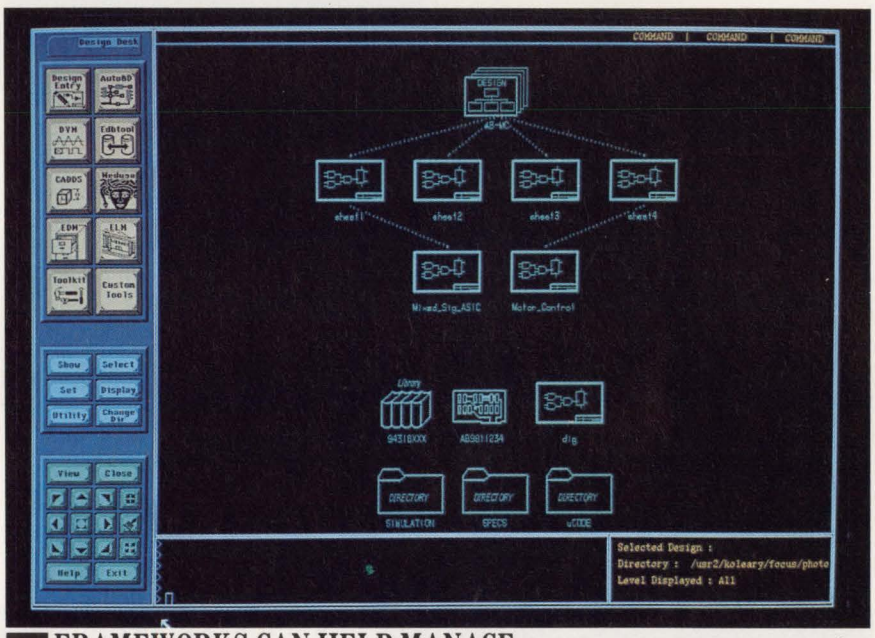
DESIGN AUTOMATION TAKES OVER MORE TASKS EARLY ON

TOP-DOWN DESIGN, LOGIC SYNTHESIS, VHDL, AND CONCURRENT ENGINEERING ARE AMONG THE HOT SPOTS AT DAC.

LISA MALINIAK

Complexity and time-to-market pressures have and continue to reshape the art of designing leading-edge systems. Engineers can no longer craft chips and boards by hand, but instead must rely more and more on EDA tools to handle complex engineering tasks early on and throughout the design cycle. On top of that, they need design environments that allow them to work together concurrently. In light of these changes, it's no surprise that top-down design and concurrent-engineering technology will take center stage at this year's Design Automation Conference (DAC).

Since 1963, DAC has served as a showcase for the latest in design-automation technologies *(see "DAC adjusts its focus," p. 48)*. This year, products and technologies being demonstrated at the show highlight the trend of design automation absorbing more tasks early in the design cycle. Exhibitors and technical sessions emphasize the latest in top-down design, VHDL, logic synthesis, and concurrent engineering, as these technologies mature and spread from early adopters to more mainstream users. In addition, many companies will show their newest field-programmable gate-array (FPGA) tools that were developed to keep up with the boom in programmable-logic use.



FRAMEWORKS CAN HELP MANAGE both tools and data. Computervision's Design Desk Framework is an open environment that provides intertool communications and file management. Users can integrate Computervision applications, third-party tools, and their own internally developed software.

With top-down design, engineers start work at a high level of abstraction so that they can explore trade-offs early in the design cycle and fine-tune a system before even one gate has been drawn. They can't accomplish this, however, without the proper EDA tools. Two DAC technical papers describe tools that automate processes needed early in the design cycle—partitioning and reliability analysis. Although reliability analysis has traditionally been left for measurement and re-designs at the end of a project, it's fast becoming the designer's concern. This is because design cycles shortened by time-to-market pressures won't accommodate that methodology. The Leading-Edge Design Systems ses-

sion on Wednesday morning contains a paper from Carnegie Mellon University, Pittsburgh, Pa., discussing a tool that supports reliability analyses and studies design trade-offs during conceptual development.

The tool is called Sidecar. It's a Unix program that runs interactively or as a slave to a general-purpose schematic-capture tool. Users are free to design with top-down or bottom-up techniques. Sidecar calculates the basic reliability metrics: hazard rate, reliability, mission time, and mean time to failure. The tool also has tables for purchase cost, board area, and power dissipation. In addition, designers use a C-like programming language to create new routines or to use with existing library routines.

Some of today's popular reliability tools are simply databases of device-reliability information. They systematically analyze design components and suggest alternate devices with higher reliability but equivalent form, fit, and function. One problem with this approach is that cost isn't considered. In addition, these types of tools must be connected to a synthesis engine, which prohibits rapid exploration of design changes because a change's effect must be reflected throughout an entire system.

Instead of resynthesizing the design, Sidecar gives its information to the designer through exploration routines. The exploration-of-parts routine is similar to the database-type tools. However, it also lists the changes and gives the cost trade-offs of each. In addition, designers can make changes to arbitrary levels of the hierarchy with Sidecar. Another routine explores the effects of temperature reductions and helps a designer select devices where active cooling methods can be beneficial. A third routine explores each design part's marginal effect on reliability. Finally, after the designer has used these three algorithms to identify possible part changes, temperature reductions, and locations for redundancy, a fourth routine shows the best possible combination of techniques for reliability and purchase cost for each change.

Partitioning impacts system-design complexity, timing, and reliability. Wednesday afternoon's Partition and Placement technical session covers new techniques and ideas for multiple-way partitioning, use of a linear or a quadratic wire-length metric, and a new algorithm to find an optimal solution for macrocell placements.

A paper from the University of Calif., La Jolla, titled "A general-purpose, multiple-way partitioning algorithm," describes an algorithm that solves multiple-way network-partitioning problems, which is the basis for all layout programs. Partitioning divides the system to the board level, the board to the chip level, and the chip to the macrocell level. Traditional two-way partitioning has

DRAWING TIMING DIAGRAMS IS MADE EASIER

Drawing and analyzing timing diagrams for a design can be a tedious and time-consuming task. Chronology Corp.'s TimingDesigner automated the process, relieving engineers from hours of work. Now the newest version of TimingDesigner makes the job even easier. TimingDesigner Version 1.2, with over 20 new features, simplifies modeling synchronous designs and developing and using timing libraries. The tool can automatically detect and analyze reconvergent fan-out situations. In those situations, timing paths are derived from the same signal. Reconvergent fan-out can fool an engineer into thinking a design won't work when, in fact, it will. Two other new features, SmartSnap and SmartGrid, align signal edges and grid lines to one or more clock signals. Added support for the development and use of timing libraries include the ability to update a diagram's existing timing variables from a library and update a library's variables from a timing diagram. TimingDiagram Version 1.2 runs on PCs. It will ship next month for $1495.

***Chronology Corp.**, 2849 152nd Ave. N.E., Redmond, WA 98052-5516; (206) 869-4227.* CIRCLE 460

■ *Booth 665*

DAC ADJUSTS ITS FOCUS

A different focus and a convenient location should make this year's Design Automation Conference (DAC) a big hit with designers. DAC, which will take place at San Francisco's Moscone Center June 17–21, has traditionally been for CAD developers. This year, however, new industry-oriented programs are designed for managers and users of design-automation tools. In addition, users and managers can attend DAC exhibits for free on the first day of the show.

A newly formed DAC Industrial Program Committee (IPC) actually instituted the changes. However, Electronic Design Automation Companies (EDAC) was instrumental to the changes in DAC's focus. In fact, IPC is made up of members from both EDAC and the DAC Executive Committee.

Two industry-oriented panels will confer on Tuesday, June 18. One, "Global strategies for electronic design", will be chaired by Harvey Jones, president of Synopsys Inc., Mountain View, Calif. It will include representatives from semiconductor, systems, and CAE companies worldwide to explore their respective interdependencies. Industry analyst Andy Rappaport will chair the other panel, "Implementing the vision: Electronic design in the 1990s." This panel, which is tailored to project and group managers, investigates what technologies and industry strategies are needed to make integrated CAD systems a reality.

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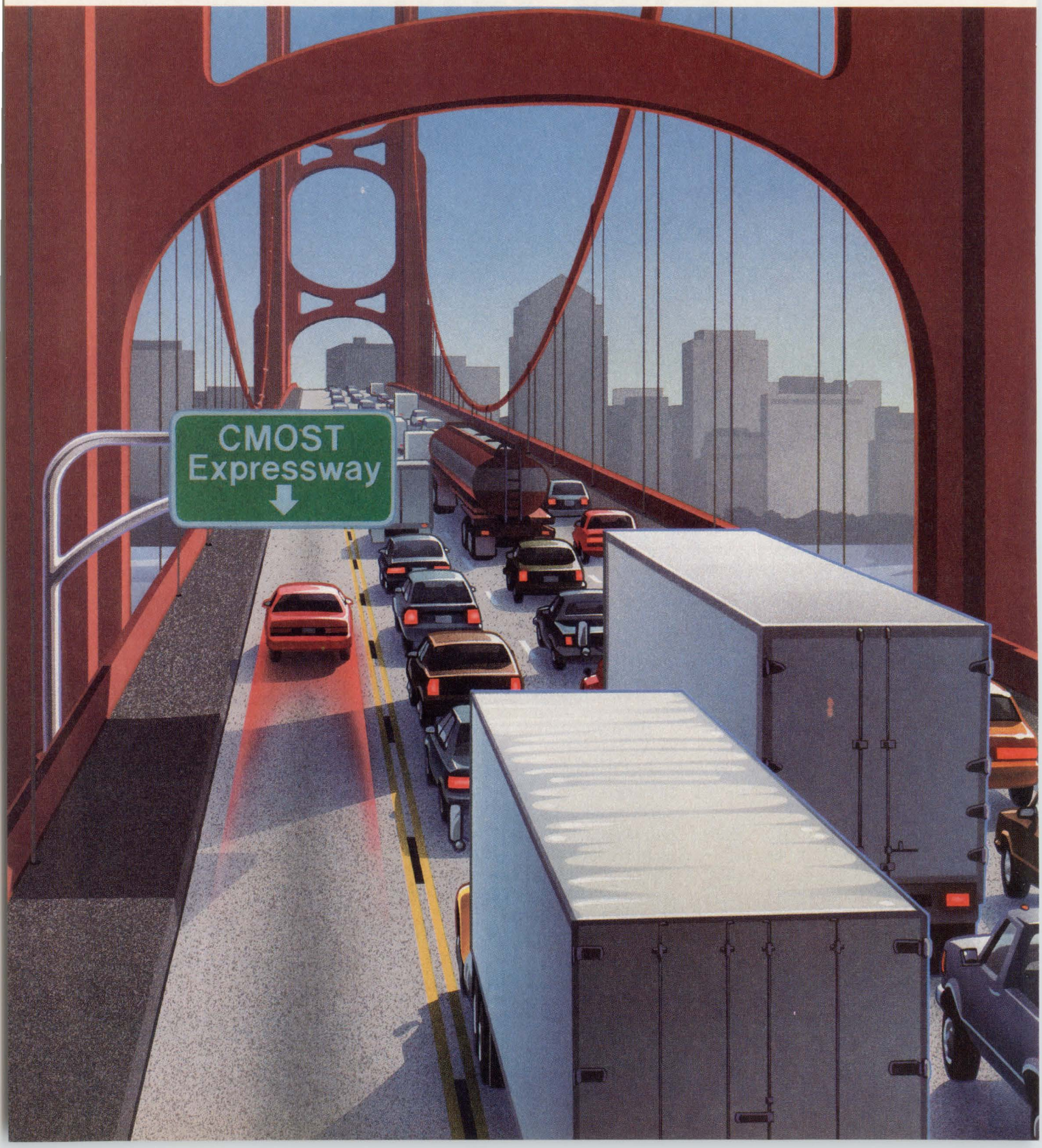

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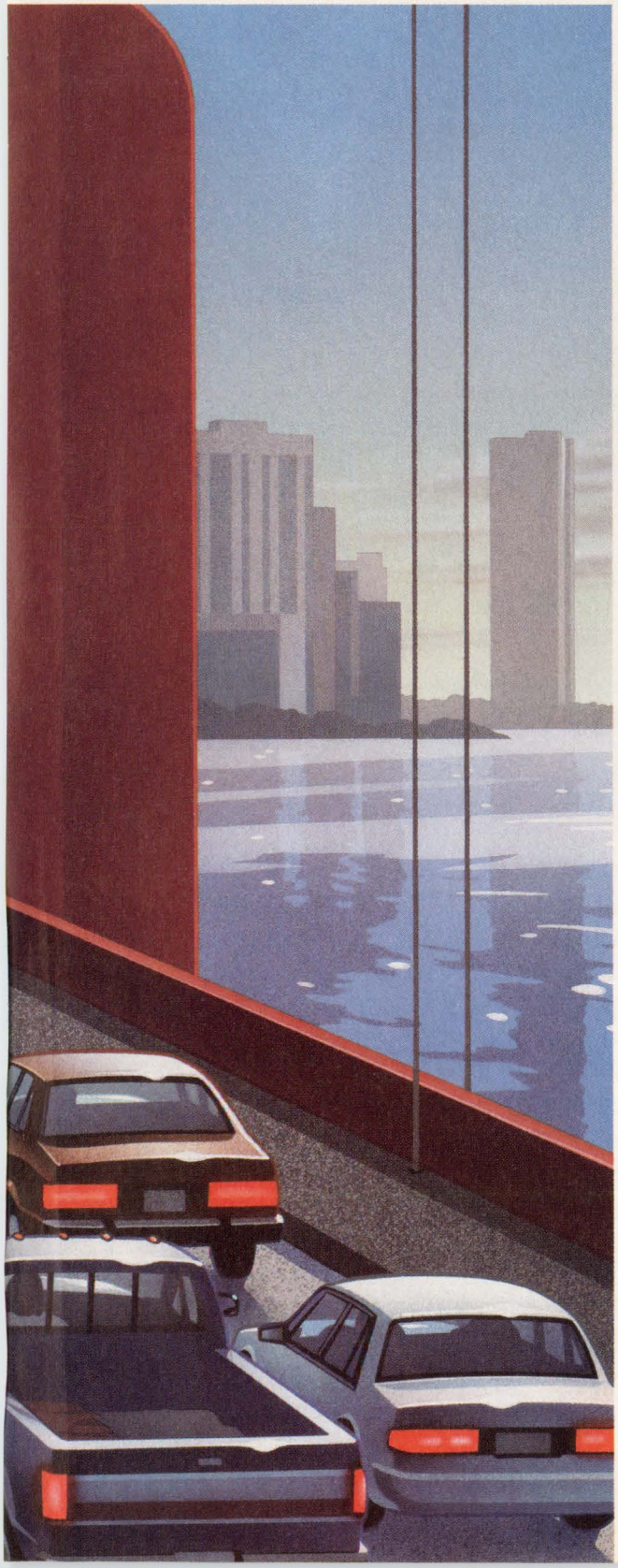

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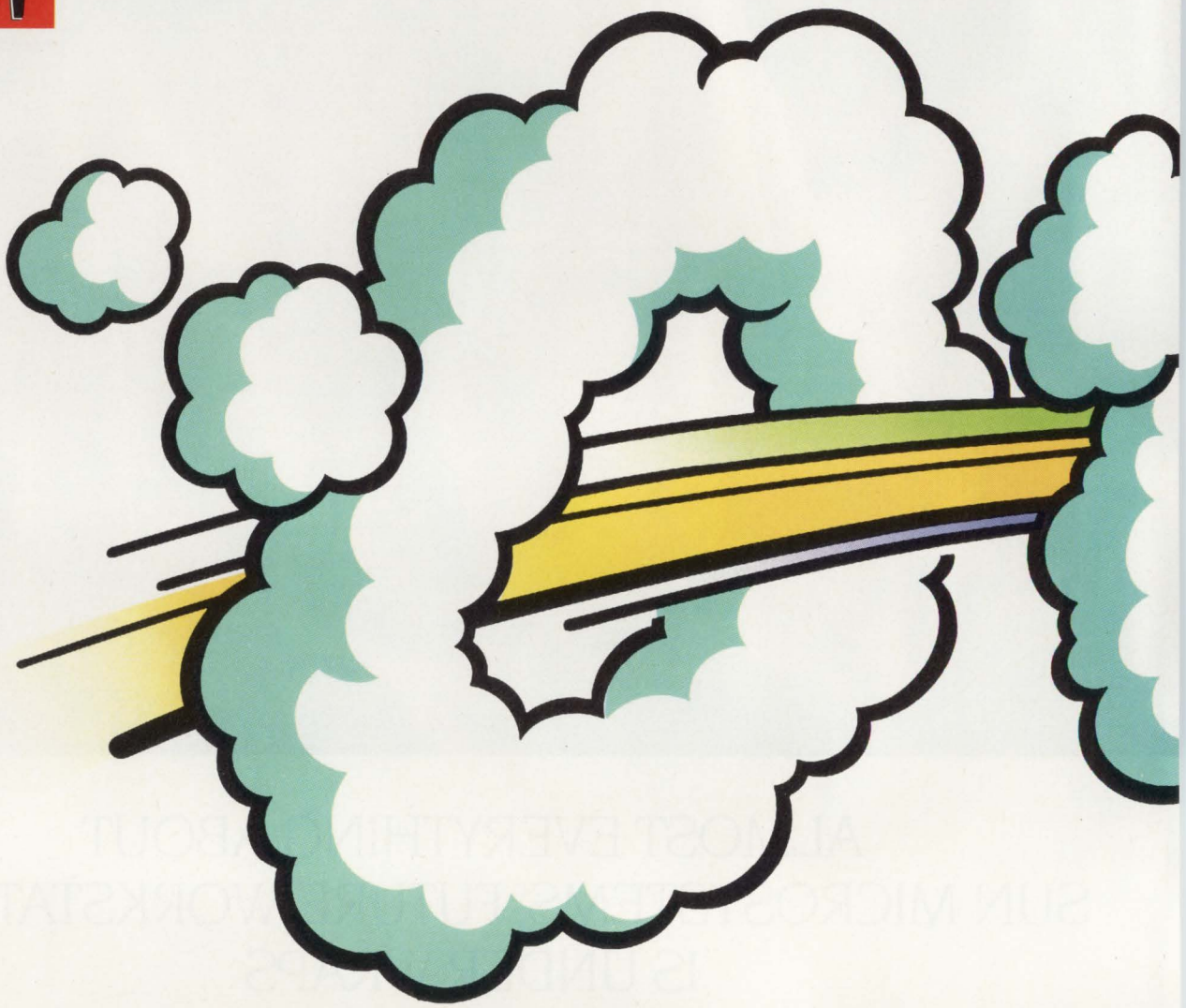

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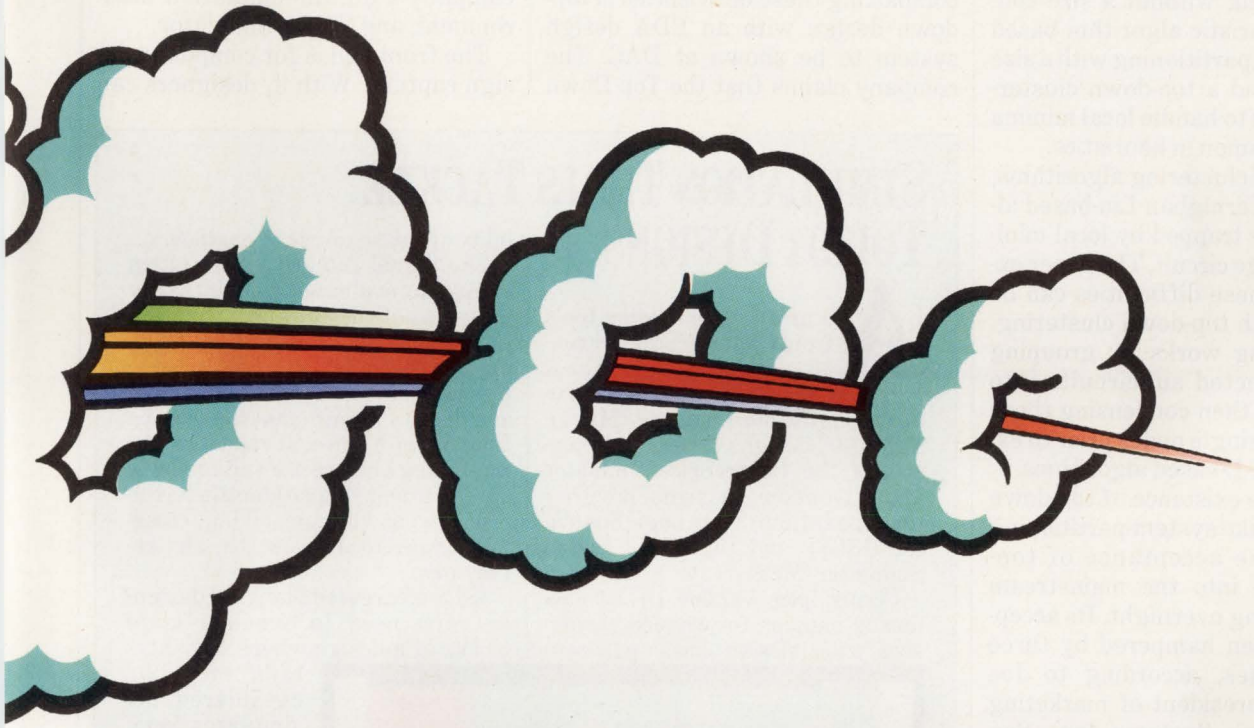

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CIRCLE 118

basic limitations as object functions optimize on different constraints. This paper discusses an algorithm to solve multiple-way partitioning problems under three different object functions: multicommodity flow for partitioning without a size constraint, a heuristic algorithm based on duality for partitioning with a size constraint, and a top-down clustering technique to handle local minima problems common in heuristics.

Traditional clustering algorithms, such as the Kernighan-Lin-based algorithms, are trapped by local minima with a large circuit. The paper explains how these difficulties can be overcome with top-down clustering. The clustering works by grouping highly connected subcircuits into clusters, and then condensing these clusters into single nodes prior to executing the K-L-based algorithms.

Despite the existence of top-down design tools like system-partitioning software, the acceptance of top-down design into the mainstream isn't happening overnight. Its acceptance has been hampered by three primary issues, according to Joe Prang, vice president of marketing at Valid Logic Systems Inc., San Jose, Calif. First, proprietary HDLs have forced designers to adopt vendor-specific top-down methodologies, despite the fact that designers want standards that facilitate vendor and technology independence.

Second, VHDL, which is the industry's only standard HDL, is difficult to use. Designers are having difficulty switching from a hardware orientation to a language-based design method. They're revolting against the idea of being like software programmers. Moreover, it's relatively difficult to write and debug code in VHDL.

A serious investment is needed to learn VHDL. Prang believes that designers will be more inclined to try VHDL if there's a gradual path to using the language, and if its adoption is simplified with alternative entry methods and programming aids.

Lastly, there's been poor integration between VHDL and gate-level simulation environments. This lack of integration has forced designers to work in multiple environments. As a result of these limitations, top-down design has been limited to leading-edge designers who can't use another approach.

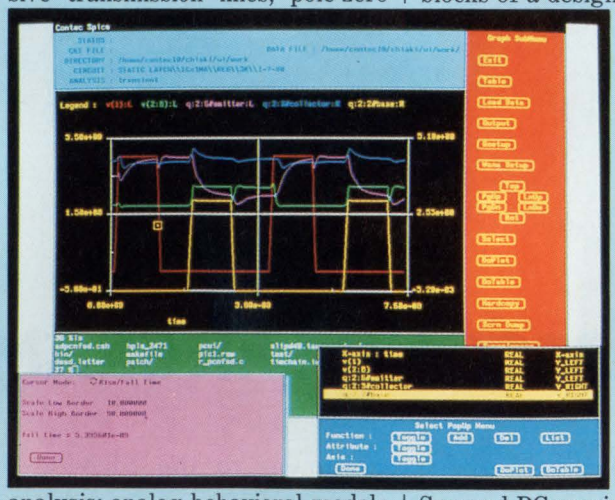
Prang says that Valid Logic is combatting these deficiencies in top-down design with an EDA design system to be shown at DAC. The company claims that the Top-Down Logic Workbench will make it easy for designers to embrace top-down methodologies. The four key components to the system are: a front-end design environment; a simulation backplane; Logic Workbench, the company's digital-simulation environment; and VHDL Simulator.

The front end is for compound-design capture. With it, designers can

SIMULATION TOOLS TACKLE TOUGH DESIGNS

An army of simulation tools from Contec Microelectronics combat the toughest high-speed analog and digital pc-board, multichip-module (MCM), and ASIC designs. These tools consist of the ContecSpice simulator and its options, a signal-integrity tool, the Infinite State Logic Simulator (ISLS), and the Mixed Signal Simulator (MSS).

ContecSpice Version 1.1 is introducing support for coupled, dispersive transmission lines; pole-zero analysis; analog behavioral models of digital devices; a digital-parts library; and transmission-line parameter generation. Version 1.1, which is based on the Spice3c1 simulator, uses piecewise constant polynomials for resistors and capacitors, delay elements, arbitrary independent sources, topology checks, and parameter passing. In addition, some of the extended features that were announced with the simulator last year will be bundled into application-specific packages to give flexibility and ease-of-use to engineers.



The Signal Integrity (SI) system is used to evaluate signal-integrity issues in both design and layout. It's targeted at digital designers building pc boards, MCMs, ASICs, backplanes, connectors, and packaging, and doesn't require that the user be familiar with Spice. SI validates critical timing and precise voltage-level specifications. It also identifies such problems as voltage spiking, crosstalk, impedance mismatch, and reflections.

ISLS is targeted at digital designers who need to simulate large blocks of a design where signal details must be considered. It simulates logic in an infinite-state or analog fashion to produce detailed waveforms. Designers use a logic simulator during the design cycle, and ISLS during the test phase.

ContecSpice Version 1.1 and its analysis options are shipping now. The Sun and PC versions of the simulator cost $5400 and $1450, respectively. Options start at $5000 for Sun machines. SI, ISLS, and MSS run on Sun workstations and cost $20,000, $15,000, and $20,000, respectively. An entry-level SI system costs $3000 for the PC and $10,000 on the Sun.

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■ *Booth 2714*

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mix text and graphics. As a result, they can define blocks at a structural or behavioral level at the outset of their design. Designs can be described with schematics, languages, truth tables, and state machines. The simulation backplane enables behavioral and structural simulators to operate transparently to users by means of automatic partitioning and synchronization of simulation engines. "Today, most designers face two alternatives: full VHDL in a non-integrated environment, or subsets of VHDL in an integrated environment," observes Sanjiv Kaul, senior product marketing manager for Valid. "Valid's simulation backplane automatically partitions and synchronizes simulation engines. This gives users the flexibility to combine full VHDL behavioral simulation and accurate gate-level simulation within a single environment."

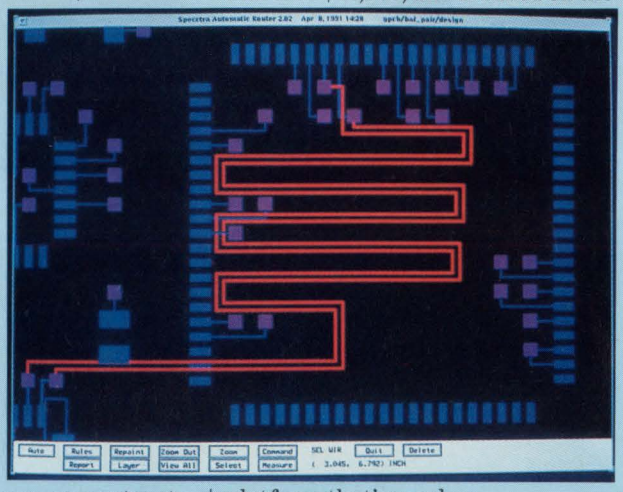
VHDL, which is very flexible, is instrumental to top-down design because it gives engineers a way to describe designs at various levels of abstraction. Its flexibility and ability to describe designs independent of implementation, however, are the very things that slow its progress. This is because it's difficult for vendors to develop simulation and synthesis tools that exploit all of VHDL.

Today, a large percentage of purchased VHDL licenses are in evaluation groups. VHDL is mainly being used by those designers who are "tire kicking," or trying to learn the language and its benefits. However, as VHDL moves into more real projects, engineers will find that the lengthy simulation times involved can cause difficulties. A VHDL simulation accelerator being shown by Ikos Systems Inc., Sunnyvale, Calif., should minimize the problem.

The VHDL accelerator combines the features and flexibility of a software simulator with higher speed and capacity. It accepts VHDL source code as input, and supports about 90% of the language's constructs. Bill Fazakerly, president of Ikos, claims that the product accelerates simulation speed by 100 to more than 1000 times, depending on the design's size. Incremental compilation

PCB Router Caters To High-Speed Circuits

Specctra SP50 is a pc-board autorouter designed to handle the special layout requirements of high-speed circuits. Features that help reduce design times for advanced boards include table-driven crosstalk controls, automatic balanced - pair routing, and length - controlled routing.



As circuit speeds increase, digital engineers face the problem of coupled noise from crosstalk. One common solution is to dedicate different layer pairs to separate ECL and TTL net classes. SP50 employs a new approach that lets users construct a table of parallel rules that emulates a curve of gap versus parallel length allowed between two segments. The flexibility of SP50 crosstalk controls enables Specctra to prevent coupled noise. For very fast dual-polarity circuits, SP50 automatically routes both nets with their associated clearances at the same time.

Specctra SP50 runs on IBM, HP, and Sun workstations. It will ship in August. Pricing for the autorouter starts at $44,900, and is based on the platform that's used.

Cooper and Chyan Technology Inc., *1601 Saratoga-Sunnyvale Rd., Suite 255, Cupertino, CA 95014; (408) 366-6966.* **CIRCLE 462**

■ *Booth 1144*

Company Acquisition Yields Complete EDA Product Line

Since its acquisition of Calay Systems last August, Siemens Nixdorf has developed a complete line of EDA tools to be demonstrated at DAC in the Calay booth. The tools include schematic capture, logic synthesis, analog and digital simulation, hardware modeling, wire-delay calculation, ASIC design, pc-board layout, thermal analysis, computer-aided manufacturing, electromagnetic compatibility, and test engineering. All of the products run under the Siframe framework that was designed within the European JESSI project.

SILOG/ic is a tool for designing PLDs and ASICs. It spans schematic entry through verification and testing to layout and preparation for manufacture. The tool uses different variants, depending on the type of component. For instance, SILOG/ic's optimizers employ Fact, Bruno, and Expresso algorithms.

For those hard-to-test ASICs, the Cerberus rule checker determines when design-for-testability (DFT) rules have been violated. Cerberus can be used during or after design. The company claims that it's the first DFT system that works hierarchically. Because it works hierarchically, there's no need to flatten net lists with lengthy programs.

Calay Systems Inc., *16842 Von Karman Ave., Suite 100, Irvine, CA 92714; (714) 863-1700.*

CIRCLE 463

■ *Booth 539*

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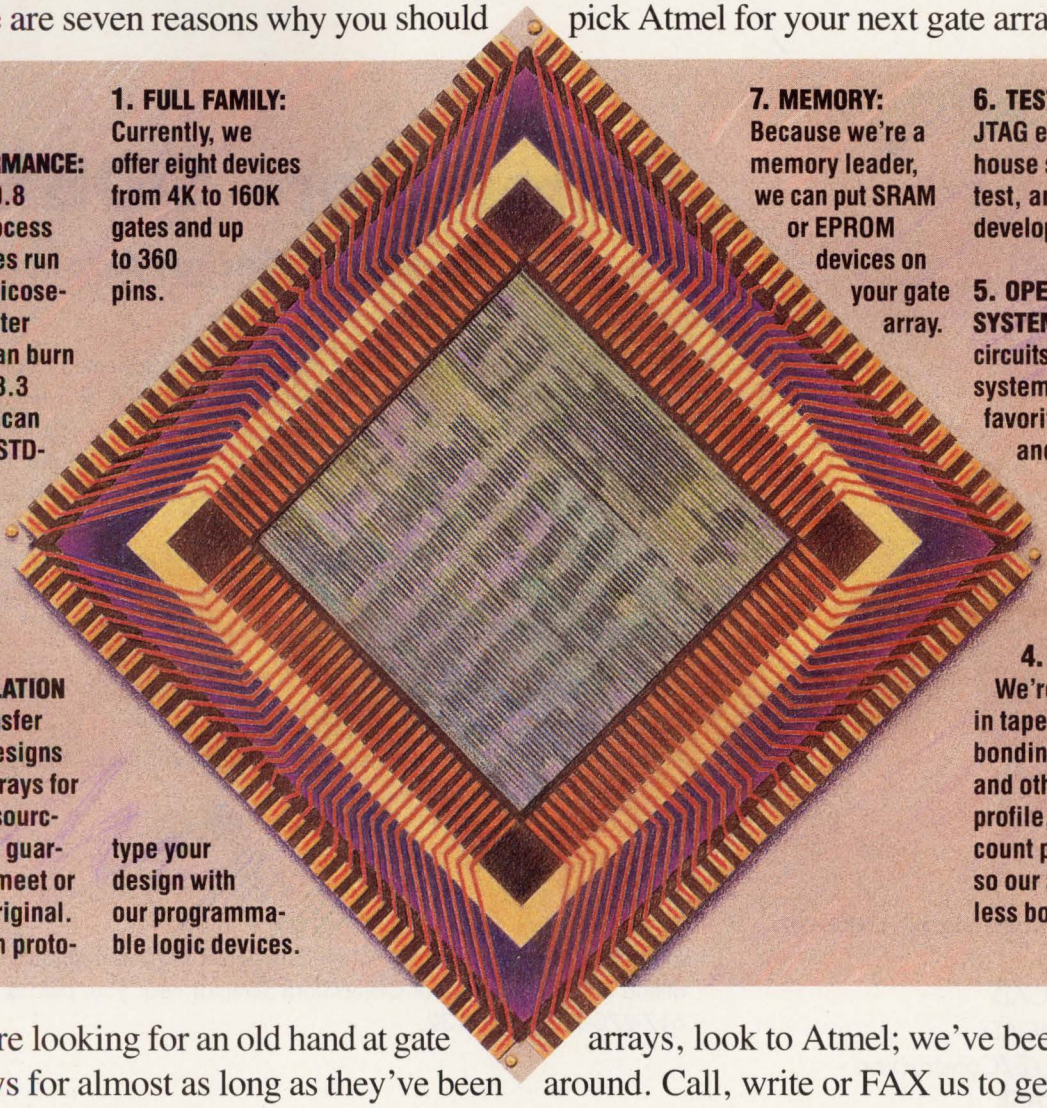

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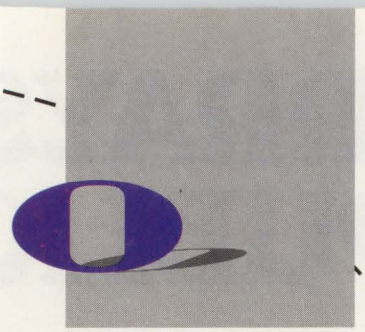

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CIRCLE 143

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speeds simulation time even further. In addition, the accelerator can go to 50,000 or 100,000 lines of code with no problem.

There aren't any trade-offs in compile time from software simulators. The hardware simulator compiles just as fast, if not faster, than software VHDL simulators. No trade-offs are made in the user interface either. And there's complete source-level debug capability. Users can set breakpoints on statements or can breakpoint on variable values. They can also trace variables and signals, display traces, single-step, and do all of the things expected from the source-level debug capabilities, user interface, and simulation control of a software simulator.

Ikos will show the VHDL product at DAC, and will deliver it by the end of the year. Fazakerly emphasizes that there's definitely a need for VHDL acceleration because in the future, almost everyone will use it for top-down design. "There's no question about it, VHDL is the design language of the future." VHDL makes it possible for designers to play with architectures and algorithms without worrying about implementation details. And that, says Fazakerly "is really the promise of top-down design."

VHDL, or any HDL, is useless without synthesis tools. Logic synthesis is hardly an unknown technology to any engineer—over 25% of the technical and panel sessions at the show feature synthesis. As it matures and moves into the mainstream, synthesis must become flexible enough to handle the wide range of applications it's being used for.

Illustrating that flexibility is a digital-signal-processing synthesis environment jointly developed by Comdisco Systems Inc., Foster City, Calif., and Synopsys Inc., Mountain View, Calif. The toolset, which will be demonstrated at DAC, combines Comdisco's workstation-based Signal Processing WorkSystem (SPW) and Synopsys' VHDL synthesis software. Users design DSP algorithms and optimized architectures with the SPW's hierarchical signal-flow-diagram approach. When the architectural-level design is complete, SPW automatically creates a VHDL specification that's read by Synopsys' VHDL synthesis tool to invoke the gate-level implementation.

Paul Titchener, vice president of technology for Comdisco, asserts that the "top-down approach to DSP design is important because it allows system- and architectural-level alternatives to be quickly investigated without having to perform time-consuming low-level implementations." He also points out that because the investigation of a chip-level implementation can begin while the architectural-level design is still being refined, concurrent-engineering concepts can easily be applied.

Also addressing the flexibility of logic synthesis is a technical paper titled "Control optimization based on resynchronization of operations," from Stanford University, Calif. Synthesis can be tuned to optimize control circuits, which determine when and in what order events will occur in synchronous digital systems. Generally, control circuitry is defined as a finite state machine. Designing and optimizing these circuits is becoming increasingly difficult due to increased complexity and concurrency.

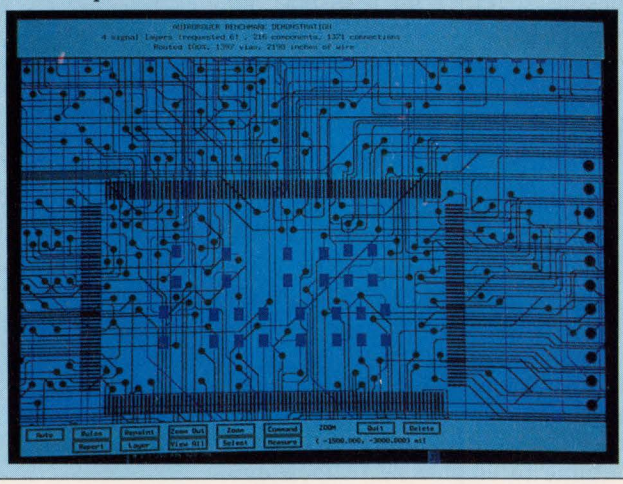
Previous control-optimization approaches used microcode compaction or state-assignment techniques, which turned out to be restrictive. The Stanford University paper outlines a new method based on resynchronization of operations, resulting in lower cost and more efficient circuits. The basic premise is synchronization redundancy. If a control system is defined as a sequence of states with certain states prioritized, it might be possible to delay execution of certain redundant states and then resynchronize them. The resynchronization algorithm categorizes the states and their interdependencies, and then optimally

AUTOMATIC, GRIDLESS ROUTER HANDLES DIFFICULT BOARDS

Freestyle, an automatic, gridless router from Scientific Calculations, is meant for use with the company's Scicards pc-board and hybrid layout system. The router employs a clearance-driven, shape-based architecture that recognizes interconnections as shapes rather than point intervals on a grid. It then combines a rip-up-and-retry algorithm with push-and-shove capabilities to move aside existing etching during the iterative routing process and achieve 100% completion rates. Because it's unrestricted by a grid, Freestyle routes at minimum clearance for maximum use of space. The tool facilitates hybrid design with such features as management of stacked, staggered, and spiral vias; coincident via rules; and via tap-in under surface-mounted pads. The Freestyle router runs on DEC and Sun workstations. It's available now for $29,950.

Scientific Calculations Inc., *7796 Victor-Mendon Rd., P.O. Box H, Fishers, NY 14453; (716) 924-9303.* **CIRCLE 464**

■ *Booth 1432*



structures the state machine.

Another paper on logic synthesis zeros in on a growing problem in timing synthesis—timing faults induced by variables in the manufacturing process. The paper was jointly authored by researchers from IBM Corp., Boulder, Colo.; University of Texas, Austin; and Microelectronics and Computer Technology Corp., Austin, Texas.

The authors assert that as circuit delays approach worst case, a timing margin must be inserted to avoid timing faults resulting from manufacturing-process variables. In the best case, products can simply be speed-selected in the manufacturing process. But in the worst case, design changes might be needed if the process variable is overly large. Logic synthesis optimizes timing with circuit compaction, so there's a high likelihood of process variations causing a timing fault.

The paper contains an extensive mathematical proof, which illustrates that the probability of a path delay in a manufactured circuit exceeding the clock interval increases monotonically as the variation in path delays decreases. To reduce the circuit's sensitivity to manufacturing-process variations, there must be a reasonable timing margin between the worst-case delay and the system-clock interval. Synthesis and test teams will need to employ some concurrent engineering to jointly define reasonable timing margin.

Concurrent engineering has promised a lot: All kinds of engineers working together on a project up front to create a correct-by-design product. Teamwork and cooperation are the first ingredients in the recipe for success. Yet, with increasing automation sneaking into the design cycle, tools and their interaction play a significant role in concurrent engineering. For example, without the proper framework, engineers using different design tools can't interact and share data.

Framework marketing has been overblown over the past several years; the promise didn't live up to expectations. Although vendors will continue to emphasize frameworks and their integration strategies at DAC, it probably won't be their primary focus. Gradually, frameworks will cease to be marketed as the monolithic solution to the integration problem. Instead, framework parts will be referred to as tools. For example, a few months ago, Valid Logic introduced the Design Manager portion of its framework as a tool for design management and tracking.

One of the newest entries into the framework market will be demonstrated at DAC by Computervision, Bedford, Mass. The company claims its Design Desk Framework is an open system that integrates Computervision's Theda EDA applications, third-party applications, and user-

MODULAR EMULATION GOES FROM 10,000 TO 1 MILLION GATES

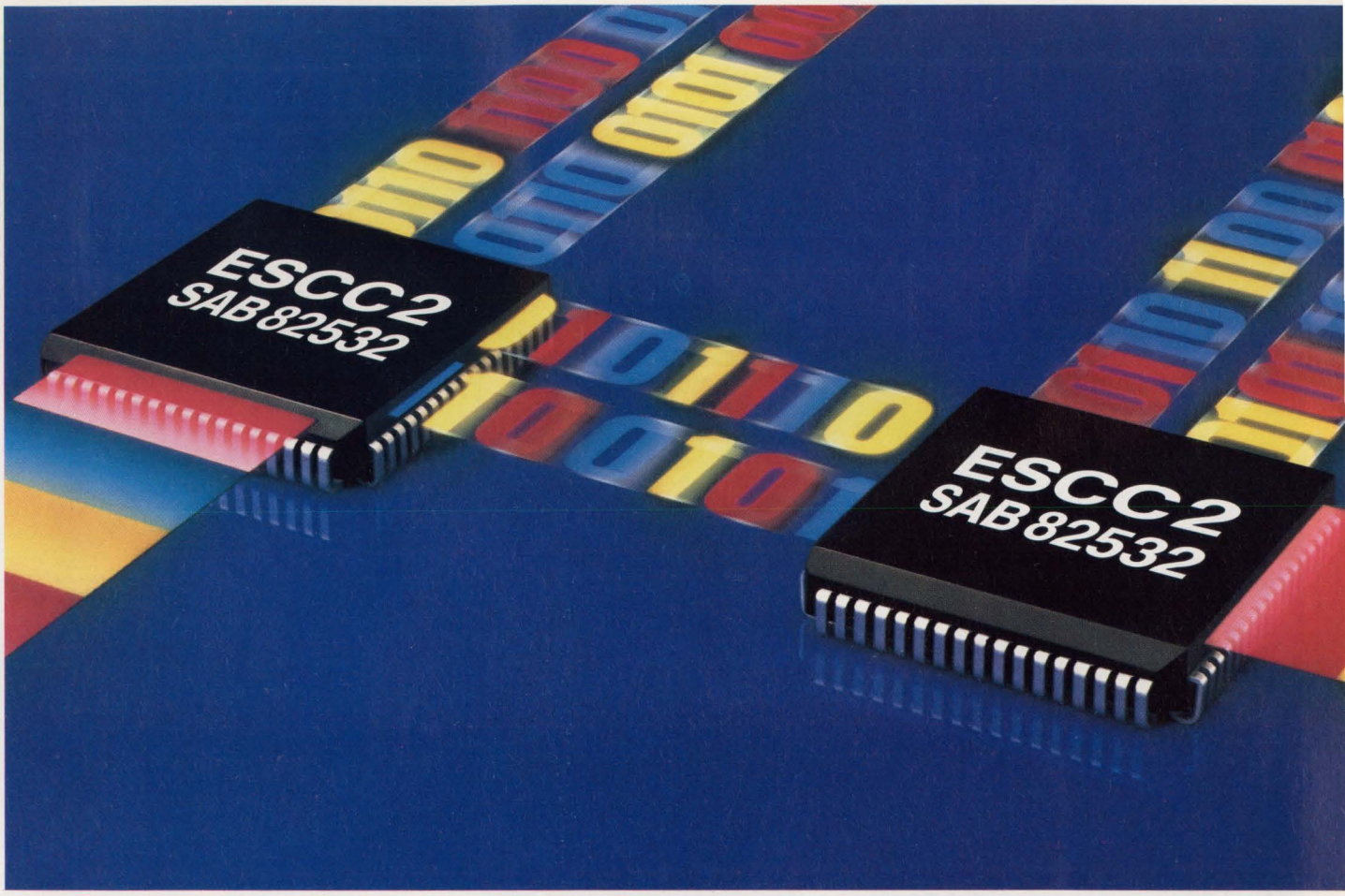
The modularRPM (mRPM) product lets several Quickturn RPM emulation systems be connected and operate as one large emulator that can handle designs of up to 1 million gates. Individual RPM systems come in 10k- and 50k-gate versions. mRPM includes OneView software and MRPM Interconnect Module (mRPM IM) hardware that integrates up to 20 emulators. The software's user interface can determine the connections needed between several RPMs, configure and load several RPMs, and configure and load mRPM Interconnect Modules. The OneView software costs $49,000 for each user license, and can be used with up to 20 RPMs applied to one emulation. mRPM IM is priced at $30,000 for 1080 switched signals. It can be expanded incrementally at $25,000 for each additional 1080 signals, up to a total of 4320 signals. All mRPM tools will begin shipping in the third quarter.

***Quickturn Systems Inc.**, 325 E. Middlefield Rd., Moutain View, CA 94043; (415) 967-3300.*

CIRCLE 465

■ *Booth 757*

SIEMENS



Communications Genius

With the development of the new Enhanced Serial Communication Controller (ESCC2), Siemens has demonstrated a new genius in high-speed multi-protocolling.

The ESCC2 (SAB82532) offers an extraordinary range of protocol options at a high-speed transfer rate of up to 10 Mbit/sec in synchronous mode. Supporting X.25 LAPB, ISDN, LAPD, HDLC, SDLC, and both ASYNC and BISYNC, the ESCC2 offers outstanding capabilities for a wide variety of applications.

And it is as adaptable as it is powerful. The ESCC2's flexible 8/16-bit bus interface allows it to easily adapt to either Intel or Motorola microprocessors. Plus, it provides direct 8/16-bit accessibility to all registers, as well as DMA and both vectoring and non-vectoring interrupt modes. This ensures efficient data transfer to and from host system memory, for fast, accurate and reliable multi-protocolling.

For superior performance and flexibility, the ESCC2 features clock recovery up to 4 Mbit/sec, storage capability of 64 bytes in each of its four on-chip FIFOs and four encoding schemes: NRZ, NRZI, FMx and Manchester. In addition, it offers user-programmable features such as 16/32-bit CRC, time slot assignment, and an 8-bit parallel port. The result is an excellent CMOS device with only 40 mW power consumption for all kinds of multi-protocol applications.

For more information on the ESCC2, or to find out how you can receive your inexpensive PC-based evaluation kit (EASY532), call 800-456-9229, or write:
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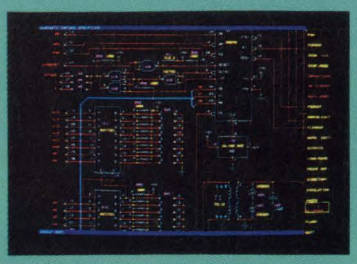
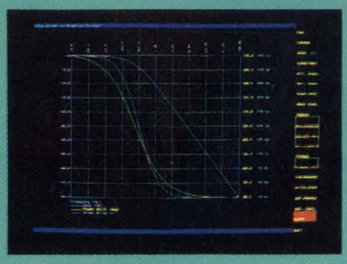
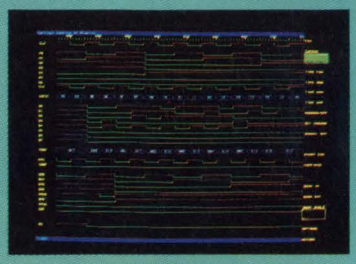


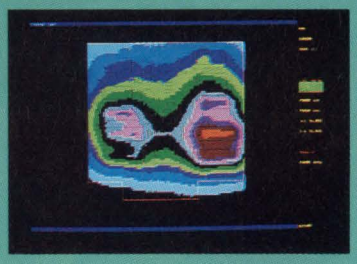
Schematic Capture



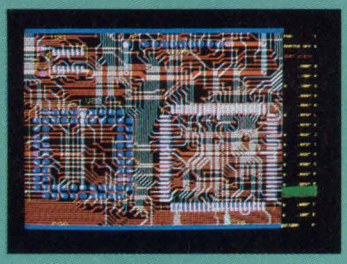
Analog Simulation



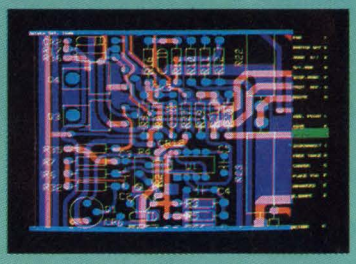
Logic Simulation



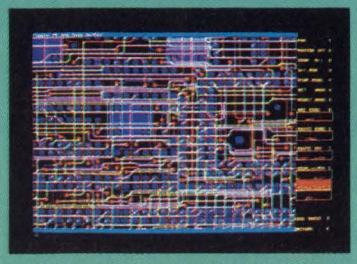
Thermal Analysis



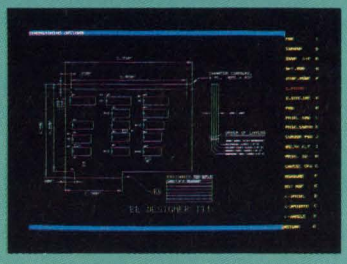
PCB Layout



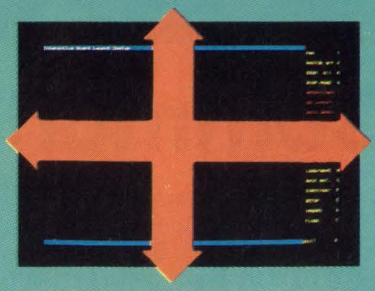
Analog Design



Autorouting



Fabrication Drawings



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developed programs. A graphical interface provides consistent methodology for accessing and using framework-integrated software *(see the figure)*. In addition, the Design Desk Toolkit is a set of utilities that lets users customize the framework.

Emphasis on integration and framework standards will continue to increase. Over the past year, Electronic Design Automation Companies (EDAC) has researched the standards issue, and will present the findings of its study at DAC. It will also propose which "next steps" are needed to enable the EDA industry to adopt standards. Andy Graham, president of the CAD Framework Initiative (CFI), states that "users are saying loud and clear that they don't want a framework unless it adheres to standards and they can get multiple vendors' tools in and out of it." Users want frameworks that help them integrate tools today.

CFI is working to solve the integration problem, and will demonstrate the most recent fruits of its labor at DAC. One of CFI's latest efforts is the formation of a users' group, which will have its first meeting on the last day of the show. The users' group is meant as a new type of forum for the end user and the systems integrator to help define the requirements for solving the integration problem. Inputs from the group meetings will give CFI clearer guidance on how to expand its focus beyond EDA. For instance, CFI would like to spread its activities into the CASE and mechanical CAD areas. Concurrent engineering will require that all of those areas exchange data.

At last year's DAC, CFI demonstrated the results of its integration project. Tools from various vendors exchanged data through a CFI-developed procedural interface (PI). This year's DAC attendees can see CFI's integration project taken one step further because it will involve the work of two other CFI technical subcommittees. The improved version of the design-representation PI will show intertool-communications and tool-encapsulation capabilities. Tool encapsulation brings tools into the desktop of a framework with tool-abstraction specifications.

The DAC demonstration will illustrate the interplay of a framework's major parts: the design representation, tool communication, and the desktop. In addition, vendors will not only show that they implemented the drafted specification, but that they did so with the intention of bringing the implementation to the market as a product. There are 31 participants in the projects, and a fair portion of those will announce plans to bring a compliant product to market.

Among other things, CFI's procedural interface was improved over the past year by adding the ability to represent data hierarchically. The original PI used a scalar, flat data representation. The improved interface can also handle buses and bun-

POPULAR PCB TOOLS MIGRATE TO UNIX WORKSTATIONS

The Pads-2000 pc-board design system will soon run on Unix workstations. Previously, Pads-2000 tools were available only on personal computers. The tools will first run on the Sun Sparcstation under Open Look X-Windows. With the workstation-based Pads there are no design-size limits. In addition, there's a 1-μm database and automatic copper fill. An interactive push-and-shove router handles curved traces. The Unix-based Pads-2000 software, which will be available in late summer through various licensing arrangements, will cost less than $15,000.

CAD Software Inc., *119 Russell St., Suite 6, Littleton MA 01460; (508) 486-9523.* CIRCLE 466

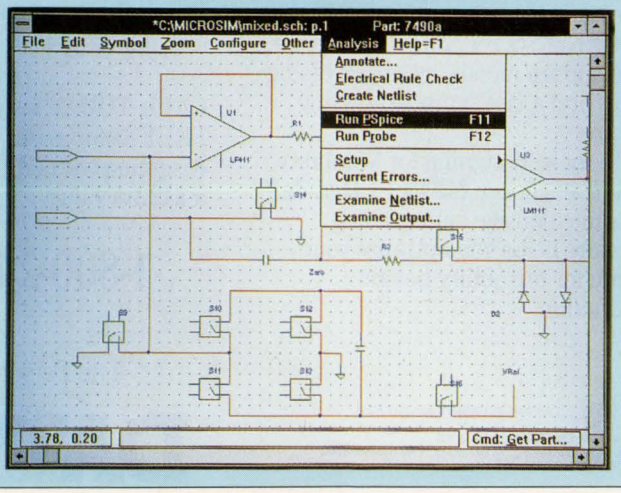
■ *Booth 439*

SCHEMATIC CAPTURE RUNS IN INTEGRATED ENVIRONMENT

Schematics is a new schematic-capture program from MicroSim that provides an integrated environment for graphical definition, simulation, and analysis of circuits. The program achieves the integration by linking directly to the PSpice simulator and Probe waveform analyzer. New symbols and parts attributes are defined with the symbol editor. Schematics runs on PCs as a Windows 3.0 application. It also runs on Sun workstations. Schematics drawings and symbol libraries are interchangeable between the PC and Sun version. Schematics can be purchased as part of a Genesis Windows 3.0 package, which costs $1250 through September. After that, it will cost $1750. The Sun version of Genesis costs $4150 through September, and $5950 after that.

MicroSim Corp., *20 Fairbanks, Irvine, CA 92718; (800) 245-3022.* CIRCLE 467

■ *Booth 1950*



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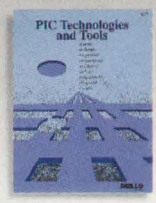

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VERIFICATION SOFTWARE FLAUNTS FULL DISTRIBUTED PROCESSING

Release 8.0 of the SL-Verify suite of design-verification software features full distributed processing, layout-versus-layout capability, and a direct Dracula-rule-set translator. The suite consists of a design-rule checker, an electrical verification tool, a mask-data preparation tool, and software that analyzes and predicts manufacturing yield. Distributed processing can occur in all phases of design verification: design-rule checking, electrical verification, and mask-data preparation. A Dracula-rule-set translator is a free option to existing Dracula customers so that companies can migrate to SL-Verify without losing the time they invested in their existing rule sets. Also included in Release 8.0 are layout-versus-layout and schematic-versus-schematic comparisons. The job-preparation preprocessor allows for variables to specify rules, so engineers can update design rules quickly when changes occur.

***Silvar-Lisco,** 703 E. Evelyn Ave., Sunnyvale, CA 94086; (408) 991-6000.* CIRCLE 468

■ *Booth 819*

dles, which are a minimum requirement for commercial adoption. CFI added some robustness to handle error conditions because with the original PI, there wasn't a graceful way to recover from an error. Finally, the PI is being grouped so that it's used more efficiently. With the original interface, a large number of calls were needed to transfer data because the granularity was high. In the improved interface, there are help functions that are macro versions of some of the PI calls. The macros make transfers more efficient. According to president Andy Graham, the new procedural interface is a solid commercial specification that can be adopted and go to the marketplace.

The quest to bring products to market faster has created a boom in the use of programmable logic. In the past, if a design had more than a few hundred gates it had to go into an ASIC. Today, however, FPGAs are taking their place between lower-density programmable-logic devices (PLDs) and gate arrays.

Gate-array vendors have always attended DAC because ASIC tools are relatively complex and usually integrate into CAE environments. Programmable-logic vendors, however, have not attended DAC. Their tools were generally standalone types that weren't very complex.

This year, Xilinx, a San Jose, Calif.-based FPGA vendor will be at DAC. Lee Farrell, vice president of marketing at the company, says FPGAs are breaking down traditional programmable-logic density and capability barriers. For instance, one of Xilinx' latest devices has 20k gates, including on-chip memory and JTAG logic. Farrell points out that "the more complex the device, the more the device must take a back seat to the design software. FPGA vendors have to start showing their capabilities at places like DAC."

Many vendor-independent programmable-logic tools will also be on display at the show. For instance, Exemplar Logic Inc., Berkeley, Calif., will showcase its latest FPGA toolset. Exemplar Release 1.0 is a suite of tools aimed at designers migrating a TTL design to an FPGA, or those compressing PAL designs into an FPGA.

The software package includes tools for compilation, synthesis, architectural analysis, library generation, and schematic generation. Release 1.0 combines synthesis, speed-area optimization, and mapping into one package. Users enter designs using standard PLD or ASIC methods, and receive optimized vendor-specific FPGA or EDIF net-list outputs.□

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CAE -- Advanced Tools:

An important element of top-down design, logic synthesis allows designers to describe systems at a high level and let the software create the circuitry. Read about it in the August 22 ***Electronic Design.***

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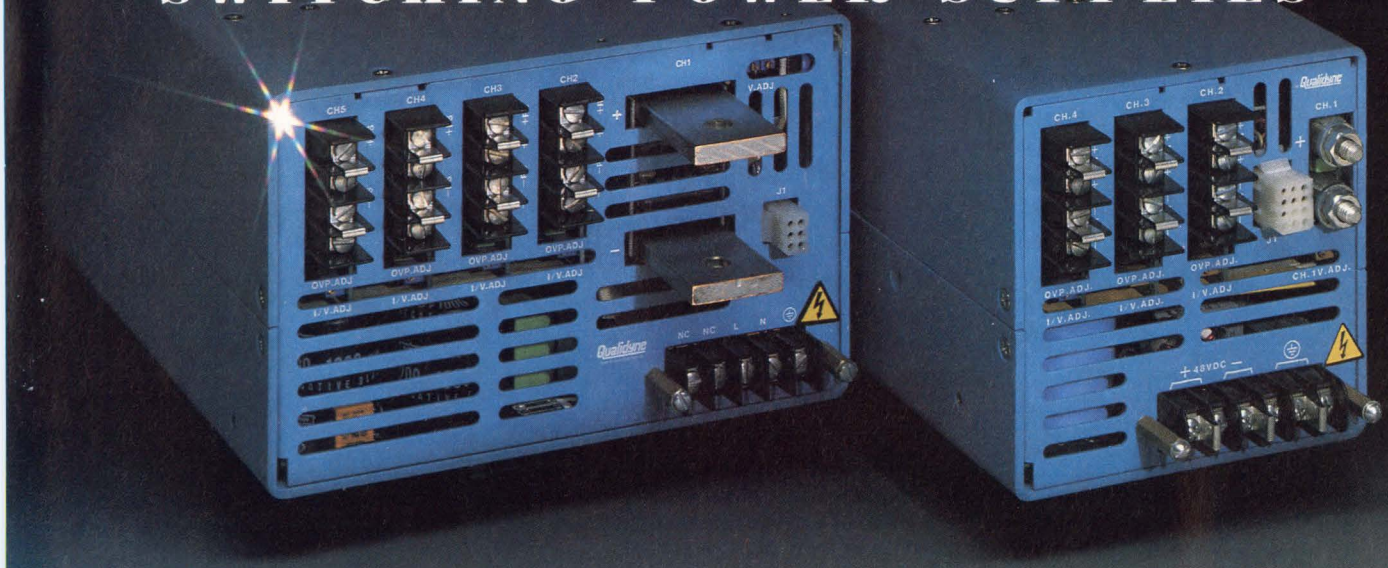

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5x8x11"	1000W	5V/150A	5-15V/20A	5-15V/20A	5-24V/10A	5-24V/10A
5x8x11.5"	1500W	5V/200A	5-15V/20A	5-15V/20A	5-24V/10A	5-24V/10A
5x8x13.75"	2500W	5V/400A	5-15V/20A	5-15V/20A	5-24V/10A	5-24V/10A

Single Output Models (Partial Listing)

Size (HxWxL)	Total Watts	Output Voltage Range/Max. Amps (select one) 2-4VDC	4-6VDC	7-12VDC	12-28VDC	28-56VDC
5x6.5x10"	750W	2-4V/187A	4-6V/150A	7-12V/63A	12-28V/27A	28-56V/14A
5x5x11.5"	1000W	2-4V/250A	4-6V/200A	7-12V/84A	12-28V/36A	28-56V/18A
5x8x11.5"	1500W	2-4V/375A	4-6V/300A	7-12V/125A	12-28V/54A	28-56V/27A
5x8x11.5"	2000W	2-4V/400A	4-6V/400A	7-12V/167A	12-28V/72A	28-56V/36A
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68HC705C8	8K EPROM, 304 RAM, SPI, SCI	68HC05C8 68HC05C4	NOW	M68HC05PGMR M68HC05EVM M68CDS8HC05
68HC705J2	2K EPROM, 64 RAM, Real-Time Interrupt	68HC05J1	NOW	M68HC705J2P9PGMR M68HC05EVM M68HC05P8EVS M68CDS8HC05
68HC705P9	2K EPROM, 128 RAM, A/D, Low-Cost	68HC05P1 68HC05P9 68HC05P7 68HC05P4	NOW	M68HC705J2P9PGMR M68HC05P9EVS M68CDS8HC05
68HC711E9	12K EPROM, 512 EEPROM, 512 RAM, SPI, SCI, A/D, Real-Time Interrupt	68HC11A8 68HC11E9	NOW	M68HC711E9PGMR M68HC11EVB M68HC11EVBU M68HC11EVM
68HC711D3	4K EPROM, 192 RAM, SPI, SCI, Real-Time Interrupt, Event Counter	68HC11D3	NOW	M68HC711D3PGMR M68HC11D3EVB M68HC11D3EVS

Soon To Be Released

OTP Part Number	Features	MCU Emulation	Samples Available
68HC705C5	5K EPROM, 128 EEPROM, 176 RAM, LED Driver, SIOP, 10mA Sink Port, Low Voltage Option	68HC05C5	10/1/91
68HC705C9	16K EPROM, 352 RAM, SPI, SCI, Expanded Port	68HC05C9	7/1/91
68HC705D9	16K EPROM, 352 RAM, SCI, Pulse Width Modulation, 24mA Sink Port	68HC05D9	7/1/91
68HC705E1	4K EPROM, 368 RAM, Phase-Locked Loop, Real-Time Interrupt, Real-Time Clock	68HC05E1	6/1/91
68HC705F6	4K EPROM, 320 RAM, DTMF, Tone Generator, LED Driver, SPI	68HC05F6	7/1/91
68HC705L5	8K EPROM, 256 RAM, 39x4 Segment LCD Driver, Event Counter, SPI	68HC05L5	7/1/91
68HC705T7	8K EPROM, 320 RAM, On-Screen Display, Pulse Width Modulation, I^2C, A/D	68HC05T7	9/1/91
68HC705T10	12K EPROM, 320 RAM, On-Screen Display, Pulse Width Modulation, I^2C, A/D	68HC05T7 68HC05T10	9/1/91
68HC711K4	24K EPROM, 640 EEPROM, 768 RAM, 4 MHz Non-Mux Bus, Real-Time Interrupt, SPI, SCI, A/D, D/A	68HC11K4	6/1/91
68HC711J6	16K EPROM, 512 RAM, SPI, SCI, Real-Time Interrupt	68HC11J6	9/1/91
68HC711L6	16K EPROM, 512 EEPROM, 512 RAM, SPI, SCI, Real-Time Interrupt	68HC11L6	7/1/91

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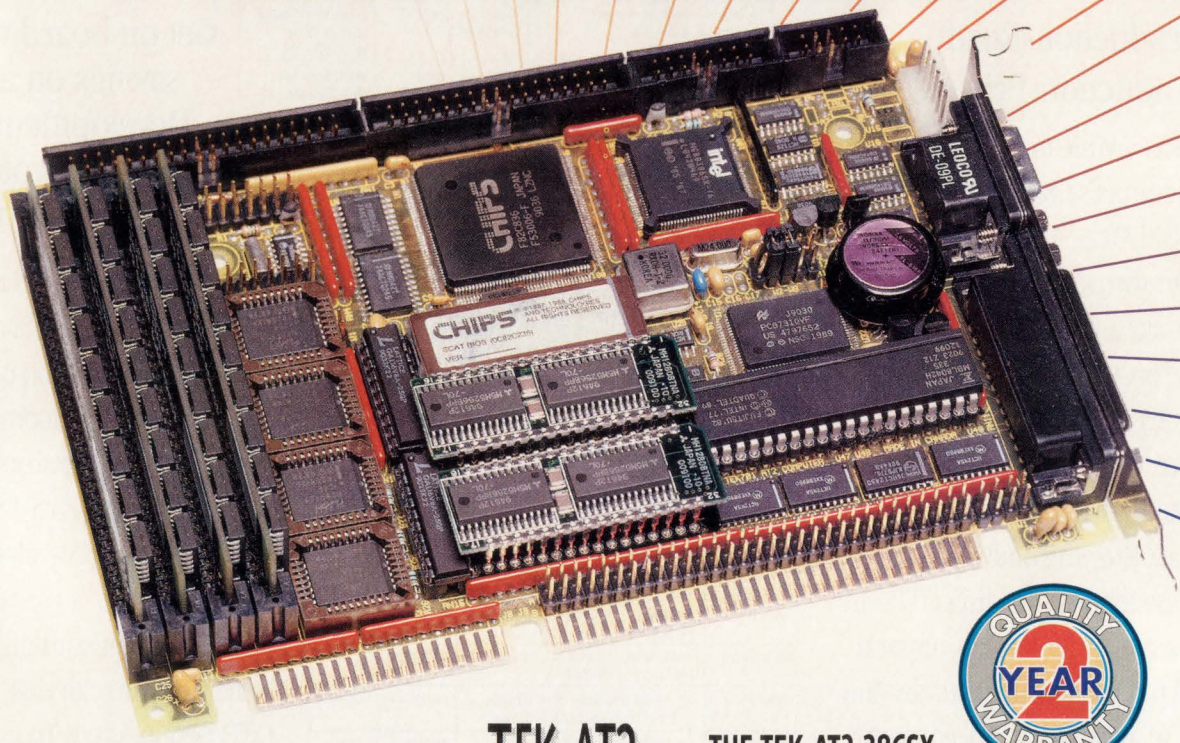

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CIRCLE 169

DESIGN-DATA-MANAGEMENT FRAMEWORKS HELP SOLVE COMPLEX PRODUCT DESIGN-TEAM PROBLEMS

THE RIGHT FRAMEWORK SERVES AS A SOFTWARE INFRASTRUCTURE FOR IMPLEMENTING MULTIDISCIPLINE, CONCURRENT DESIGN PROCESSES.

Over the last decade, narrowing market windows and global competition have forced engineering organizations to rush increasingly complex designs into production as quickly as possible. Although the advent in the 1980s of computer-based design tools eased the crunch somewhat, the ensuing proliferation of ever more sophisticated and specialized tools has clouded the picture.

Computer-based design sped up and automated almost every aspect of the design process from concept to simulation, from verification and test to layout, and from detailed design to documentation. The accuracy and quality of the designer's work benefited greatly. But if four or so tools were enough to design an integrated circuit 10 years ago, today's designs may require 20 tools or more.

Some of the productivity gains promised by design automation never materialized. That's because data produced by one design tool couldn't easily be passed to the next. The tools couldn't manage and provide access to the hundreds of data files that were created during a design project. For a team of designers working together but using several tools, finding the right data, learning how to access the various tools, moving data from one tool to the next, or ascertaining the status of the project as a whole became nearly impossible.

To make matters worse, the design environment is typically a pot-luck assortment of hardware and software. The hardware might include departmental systems, workstations, and dedicated turnkey CAD systems. Operating systems run the gamut of proprietary systems, such as VMS, and cross-platform systems, such as UNIX. Even an all-UNIX environment will involve different UNIX implementations used by the various platform vendors, most of which aren't fully compatible.

The design tools themselves represent an even wider variety. Some are commercial and some are produced in-house. Not only that, the mix of tools rarely stays the same for long. When new systems aren't simply replacing the old ones, then they're just added to the soup. It's no surprise when the new tools don't communicate well with the old.

Then there's the pool of design data, which, during the course of a design, is continually growing. Swelling libraries of active and inactive designs must be managed effectively and reliably. Designers must be able to track the evolution of product data toward a finished design. The data should be accessible to all team members and to management as well as to related functions outside the team, all on-line. The precision needed to accomplish this data management, however, is often lacking.

All these factors add up to errors. According to recent studies, design errors account for an average of 20% of design costs and contribute 37% of product-development time. Any technology that significantly reduces errors is extremely valuable. One answer to this problem is frameworks, which integrate tools and data through a single user interface. In addition to a common interface, these software-support tools, which are built on the vendor's base CAD applications, offer a shared database used by all tools and a high degree of interactivity between tools.

TWO TYPES OF FRAMEWORKS

There are two implementations of framework technology available today: EDA frameworks and design-data-management frameworks. In general, EDA frameworks are specialized and support closely related tasks within a highly integrated EDA environment. EDA frameworks are meant to move design data between applications. Because these frameworks handle product-specific data, such as pins, gates, and geometric shapes, their tool sets tend to be tightly integrated by means of modification of their source code. While EDA frameworks ease data translation and remove

some of the burden of relearning different syntaxes, they generally aren't optimized to acquire and use management data to control the work process effectively. This is where design-data-management frameworks excel. They supply management with data to support high-level functions such as design-version control. They also help with management of configurations, tools and tool runs, and the overall design process. Companies need a combination of EDA frameworks and design-data-management frameworks to address design-management problems throughout the entire span of product development.

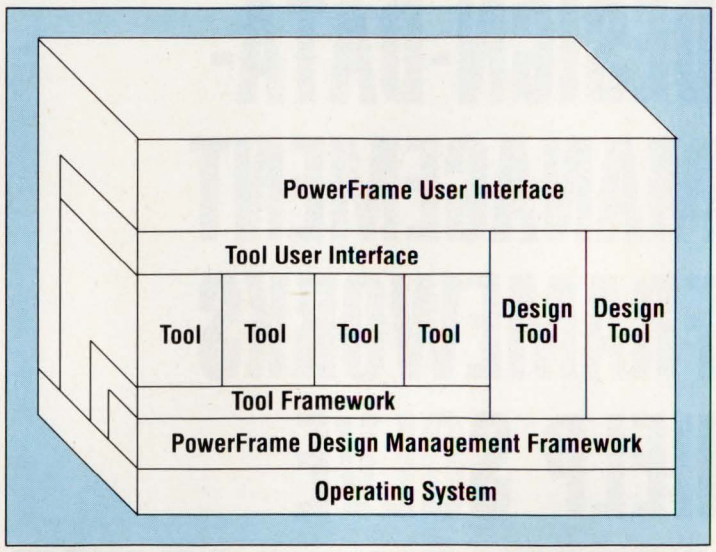
For designers, a successful framework has to support integrated access to the best tools available, offer an uncomplicated interface to all tools, and clearly represent design data and work-in-progress for multiple tools. It must automatically feed a tool the right input file, but it should also offer the flexibility to jump back a few revision levels. The Institute for Defense Analysis estimates that such a framework can reduce product-development time by 40 to 60%. The Technology Research Group estimates that frameworks can increase productivity by as much as 30%.

For engineering management, however, the right framework can mean more than that. Management has to solve the total product-design problem, not just the relatively narrow concerns of individual designers. In most cases, product design is an interdisciplinary effort. Each discipline—mechanical, electronic, and software—has its own set of tools and design-process problems. The framework can help ECAD, MCAD, and CASE to work together efficiently. The framework must manage design data generated by various tools on various platforms in a variety of geographies. It must also manage that data for revision control, configuration control, and design traceability. Moreover, it must enforce a design methodology within this same heterogeneous environment.

Another benefit that project and engineering managers can derive from a framework is the ability to employ concurrent engineering techniques to improve team and organizational productivity. A variety of functional groups must be able to participate in design from the conception stage. That's possible with a multidiscipline design environment under automated control.

The design industry first introduced computer assistance to the design process in the form of frameworks optimized for a specific set of tools. In general, this is a specialized framework that supports a few closely-related tasks, which they serve very well with a highly integrated environment. However, because it's optimized for tight integration rather than flexibility, this approach has limitations:

- It constrains access to new tools and tool technologies
- It can't be easily extended to accommodate multidiscipline design activity
- It can only be used on the platforms that support the base applications



1. Design-data-management frameworks like PowerFrame complement what EDA frameworks can do. PowerFrame brings together applications, design-data management, and design-process management under a consistent graphical user interface across disciplines such as ECAD, MCAD, embedded CASE, and documentation.

Still, if very tight integration is important, and if the tools represented by the base applications are acceptable, then an EDA framework is an excellent solution for a particular design domain. But addressing the entire span of product development calls for a mix of these EDA frameworks from a variety of sources. The result would be pockets of automation in a basically manual design process.

It's clear that a higher order of framework is needed, above and beyond EDA frameworks, to offer coherency and stability for the design environment as a whole as well as the process it supports. It needs to balance the designer's need for flexibility with management's need for control. In addition, the framework must support an open, multivendor solution.

The flexibility provided by an open framework is not so much to enable users to change tools and methodologies in the middle of the design process. It's so you can shape the framework to the environment, rather than the other way around. In an open framework, designers can have the tools and techniques they're comfortable with, regardless of their discipline. The framework's backplane-like openness also lets management adapt the framework to new projects, just as you would upgrade a computer by plugging in new boards. A superior design-management framework should also preserve the CAD manager's investment in workstations and other computing platforms.

To date, the most promising effort to address this open-framework issue is the work of the CAD Framework Initiative (CFI), a consortium of vendors, computer makers, and end users. The group's expressed goal is to define the standards for procedural interfaces between framework components. The idea behind CFI is that if a given framework complies with it's standards, then any tool vendor, computer builder, or in-house tool developer that

respects those standards can play a part in its evolution. Participants can create a customized environment into which new tools and processes can be integrated with a minimum of effort.

UP TO THE STANDARD

There's no such thing as a fully standards-compliant framework yet, but the PowerFrame framework from Digital Equipment Corp., Maynard, Mass., has a good deal of the CFI-specified structure in place. It can provide needed stability to a heterogeneous design environment now.

The PowerFrame software establishes a compatible framework for using applications from diverse design-tool vendors. It offers the freedom and advantages of selecting from the best current application base while integrating those applications into an homogeneous environment based on industry-standard windowing.

On top of that, the PowerFrame framework implements concurrent engineering: it supplies the automated mechanisms to coordinate and drive work-in-progress across multiple engineering disciplines. Concurrent engineering requires a highly interactive framework that will track and enforce design methodologies and data for many tasks being performed in parallel. PowerFrame melds all the tools, data, and engineering disciplines into one common environment to drive the design process according to users' methodologies.

A PowerFrame framework supports a heterogeneous network of CAD workstation users. It runs under the ULTRIX operating system on Digital's RISC and VAX systems, the VMS operating system on VAX systems, and the UNIX operating system on Sun-4, Sun-3, SparcStation, SparcServer,

POWERFRAME SUCCEEDS AT NEC

When NEC Electronics Inc., Mountain View, Calif., set out to offer its high-end ASIC customers a suite of advanced design-automation tools, the company was keenly aware of the need for a fully integrated design environment. "The complexity of ASIC designs is moving well beyond 100,000 gates," said Hiro Hashimoto, associate vice president and general manager of NEC's ASIC business unit. "Providing front-to-back support for advanced-ASIC-design methodologies within a unified environment is the only way to meet our customers' design cycle and performance requirements." With that goal in mind, NEC turned to DEC's PowerFrame design-management framework as the umbrella under which a diverse set of tools from several vendors would coalesce into a streamlined design process.

The objective of the project was to implement a PowerFrame environment for use in their "Open-CAD for Cell-based Design" program. The project was accomplished jointly between NEC and Digital, with the assistance of several tool vendors: Cadence Design Systems Inc., Synopsys Inc., and Viewlogic Systems Inc.

NEC had a number of defined requirements for its PowerFrame implementation, which included, among others, check-point and version management of all design files, maintenance of a top-down methodology, sequential process control, and operation within a distributed-computing environment with many different CPUs, tools, and machines. The integration process was iterative, with many refinements that led to a satisfactory result.

First, to begin its CAD-system analysis, NEC produced a data-flow diagram that included all the tools and files in the process. For design entry, Viewlogic's Workview/Viewdraw tools were chosen for encapsulation within the PowerFrame environment.

On an alternate design path, but also for design entry, was the UNIX vi editor. Edifneto and Verilnet, Viewlogic's translator tools, were also included. Other tools included the Synopsys Design Compiler, used for logic synthesis, the Verilog and Veritime simulation tools, the Edif—flatten and E2V translator tools, and the Cell3 Ensemble tool for triple-layer-metal cell-based layout.

Continuing with the CAD-system analysis, a use model was created to determine the user environment. It was determined at this stage that a top-down methodology would be used. A set of policies was implemented to assure that designers would have access to the latest version of released data. Then, a data model was developed to present data in a task-oriented fashion. The datasets were defined according to separate views: schematic entry, logic synthesis, and simulation.

Over eight possible PowerFrame processes were identified. This was done by grouping tools together within automation boundaries to identify tools that would be used together in a series. After analyzing each tool's inputs and outputs, options, and data relationships, it was determined that eight separate tool agents were required. Similarities of function, design methodology, and input and output allowed one tool agent to encompass more than one tool in some cases.

Finally, NEC arrived at a simplified, yet enhanced ASIC design process in which the burdens of version management and checkpointing, and checkout and change control were lifted from the designer and managed by PowerFrame. The PowerFrame software served as a single, common, easy-to-use interface for all the tools in its environment without limiting their functionality.

Digital, in conjunction with NEC, transformed a CAD process that included many tools from multiple vendors running on different CPUs into a streamlined design process under PowerFrame. NEC's ASIC design environment layered under Digital's PowerFrame software is in use at NEC today.

IF 22 DIFFERENT COMPANIES ARE ALL OPEN TO THE SAME IDEA,

NAS FROM DIGITAL.

IT MUST BE SOME IDEA.

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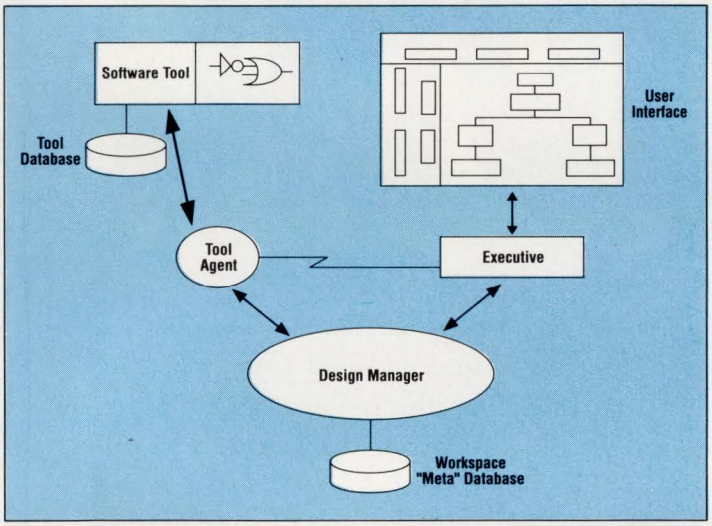
THE OPEN ADVANTAGE.

CIRCLE 158

and HP/Apollo platforms. On UNIX platforms, all PowerFrame systems communicate using the TCP/IP network protocol.

In bringing together applications, design-data management, and design-process management, the PowerFrame software offers *(Fig. 1)*:

- The ability to customize and expand the design environment with the tools of your choice
- Automatic creation and maintenance of design and library data for encapsulated applications (This can complement the EDA frameworks becoming available by providing access to multidiscipline tools from vendors and access to product-data-management systems.)
- Data tracking and configuration control with the ability to link to corporate product-data-management systems
- The ability to construct a hierarchy of design components and libraries to represent the appropriate methodology for a particular project



2. PowerFrame is made up of a set of functional components. The Design Manager Server maintains an active meta database, called a workspace, that tracks design, library, and tool data. The PowerFrame Executive, which is the graphical interface to the system, provides a straightforward method for invoking tools and displaying design, library, and tool data.

- A consistent graphical user interface to all of the resources of the design network, including tool invocation and product-design-data management

PowerFrame can complement the EDA frameworks becoming available by providing access to multidiscipline tools from vendors and access to product-data-management systems.

POWERFRAME COMPONENTS

The PowerFrame software is made up of a set of functional components *(Fig. 2)*. The Design Manager Server maintains an active meta database, called a workspace, that tracks design, library, and tool data. It can include a release tool that enables users to establish a formal beta or stable version of the design, which can then be made available to other team members or released to production.

The PowerFrame Executive, which is the graphical interface to the system, is based on the native windowing systems of the platforms supported by PowerFrame. It provides a straightforward method for invoking tools and displaying design, library, and tool data.

The Frame Administrator Utility configures workspaces according to customized definition files. In them, the various tools, data, and libraries that the design team needs are defined.

Each tool that's integrated into the PowerFrame framework is associated with an Encapsulation. Each Encapsulation includes a tool agent—the program that integrates the application with the framework—and the definition files that support the tool agent. No source-code changes must be made within the application to encapsulate it in the PowerFrame framework. Digital and several tool vendors provide encapsulation for a number of design tools. For those who want to write their own tool-agent programs for integrating unique applications into the framework, Digital provides an optional Integration Toolkit.

Because the tools themselves require no alteration to be encapsulated within the framework, new tools can be added at any time without having to start from scratch. In addition, Digital can continually improve PowerFrame without causing CAD managers to constantly update their tools.

In operation, the framework provides a graphical, universal front end to a group of "integrated tools," making all of the tools seem to be facets of a single system—the PowerFrame system. The framework manages input and output data, the files and file versions the tools generate, and user interactions.

The multiwindow environment that PowerFrame displays at the engineer's workstation is called a workframe. A workframe operates on a workspace, the permanent database used by the framework to manage and store design data. Users can log onto any workspace on the network to which they have access privileges.

The PowerFrame software greatly simplifies design tasks. Its user-friendly graphics interface is consistent no matter what tools are used. The window-based interface is intuitive and largely self-documenting. Menus, icons, and dialog boxes are used to invoke tools and to browse information about tools and data *(Fig. 3)*.

By automating design-data management, the framework does the job of keeping track of the location and organization of files used by the tools. Also, configuration control tracks the versions of data and the relationships between versions through the design steps.

Another key to the PowerFrame software is its ability to manage the design process. The framework can automatically invoke tools in a predefined sequence using the appropriate data for each tool run. This feature ensures that the designer is always working with the right tool on the right data at the right time.

Implementing the PowerFrame framework isn't achieved overnight. But an open framework like

PowerFrame lets you shape it to your design needs and to the environment of your choice, not the other way around. You won't be designing by the framework's rules in a restricted environment. But shaping the PowerFrame software to your needs takes planning *(see PowerFrame Succeeds At NEC, p. 67)*.

The more carefully thought out and planned an implementation is, the better the framework will serve your team. To gain the greatest advantage in any implementation of PowerFrame, it's helpful to follow some guidelines for planning.

An analysis of the user environment is a good place to start. The number of users, users per work group, the distribution of tasks within them, and their physical location are all factors. Other factors include the tools to be encapsulated and the computing environment. Also, a detailed data-flow diagram of the CAD process should be created.

The next step is to design a data model, which determines how data is to be organized and presented to users within PowerFrame. Much of this information will translate directly into the setup of the definition files for tool encapsulations.

One of the most important steps in effectively using a framework is to structure the design data to reflect the design environment. PowerFrame offers predefined, yet flexible data constructs that enable data to be organized and browsed in a number of ways. With the design process and its supporting data organized logically from the start, engineers won't need to be concerned with files and directories. Instead, they can operate on groups of data organized by the task and tool in use.

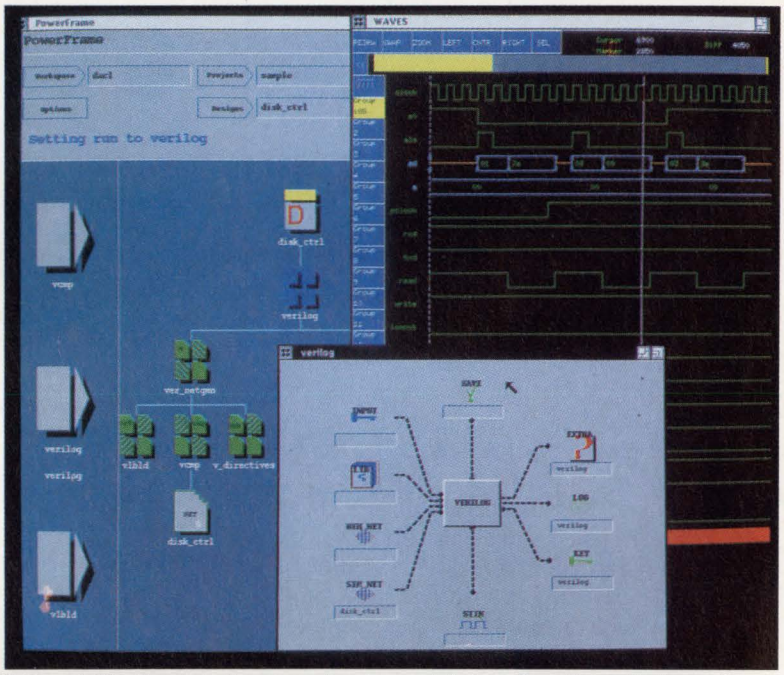
Mapping the CAD process into PowerFrame processes is another crucial planning guideline. A PowerFrame process is a grouping of tools which can be run sequentially with a single invocation. The initial step in mapping the process is to identify the tools and translators that are involved in each phase of the overall process. The goal is to determine which tools may be placed into one PowerFrame process to simplify their use.

After the data model and design processes have been defined, the focus shifts to tool encapsulation. Doing so entails writing a tool-agent program and a set of definition files for each tool. Within those files is information on all of your design tools, what files those tools use and create, which systems the tools and their data reside on, how tools and data objects relate to each other, and the order in which tools should be executed. The tool-agent program invokes the tool and identifies its inputs and outputs. The definition files work together to organize and maintain technology libraries, tools, and design data. Once those files are established, a tool is part of the PowerFrame environment.

LINKS TO PRODUCT-DATA-MANAGEMENT SYSTEMS

PowerFrame manages design data as it relates to the active design process, yet that data has an impact on other activities in the corporation, from marketing to manufacturing. Design teams need a way to distribute that product information effectively and securely where it's needed. Product-data-management systems (PDMS) provide the means to manage product data across an enterprise. Although PowerFrame isn't designed for that purpose, it can ensure that the right data reaches the PDMS.

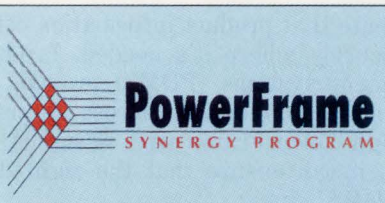
It's difficult to keep a PDMS up to date because it's a burden on engineers to fill out complicated forms every time they make changes. Consequently, the engineers tend to not fill out the forms, or defer their changes and batch many together, which means that at any given time the PDMS may not accurately reflect the current state of the design. This is even a bigger problem when tracking dependencies and versions.



3. By exploiting the windowing power of modern workstations, PowerFrame displays the design environment and the work in progress. Tools are selected and run simply by pointing at their icon.

PowerFrame's tool-encapsulation approach allows this data to be tracked automatically, without bothering the engineers. Each time a tool session is finished, the agent can record all of this information. When the design is released to the PDMS system, the release process can use the information in PowerFrame and convey it to the PDMS—without any additional effort by the engineer.

One of the best features of PowerFrame is that it gives its implementers the freedom to choose the tools they need and fashion the methodology that will make their design process successful. That's in the best interest of both the engineering firm that uses the framework and its tool vendors. The CAD Framework Initiative shows the vendors' recognition of the value of open frameworks. Although CFI is far from completing its efforts, Digital's PowerFrame is a heterogeneous design-management framework that meets several of the CFI ob-



Alliances of vendors and users have proved in the past to be a powerful force in shaping the EDA industry. In that vein, the PowerFrame Synergy program is a cooperative effort that brings together design-framework users, tool developers, and other organizations seeking to influence the continued development and enhancement of the PowerFrame environment.

The initial participants include resellers, joint developers of future enhancements, and application suppliers. In addition to those groups, participation in the program is open to users and standards consultants. One reseller, Harris Corp.'s Scientific Calculations Division, is committed to PowerFrame as an exceptionally strong, comprehensive integration system that responds to the need for increased design-team efficiency and design quality.

According to David J. Marini, Harris/Scientific Calculations' Vice President and General Manager, "Users want to choose the tools, platforms, and process models that meet their specific needs, regardless of vendor, and to manage them efficiently." Each participant in the PowerFrame Synergy program shares a common interest: to promote a design-management framework with a stable architecture and interface standards.

Those attributes, Marini feels, will enable users to reap the benefits of efficient design management while protecting both current investments and future options. "We believe the PowerFrame environment represents at once the most proven and most promising basis for this effort," Marini said.

PowerFrame Synergy Program Members

- ADRA Systems Inc.
- Applied Information Systems Inc.
- Cadence Design Systems Inc.
- Data I/O Corp.
- Digital Equipment Corp.
- GenRad Fareham Ltd.
- Harris Corp./Scientific Calculations Div.
- Logical Devices Inc.
- Matra Datavision
- MCC/CAD Framework Laboratory
- McDonnell Douglas Systems Integration Co.
- Meta-Software Inc.
- Parametric Technology Corp.
- PDA Engineering
- Racal-Redac Inc.
- Schlumberger Technologies CAD/CAM Div.
- Sherpa Corp.
- Silvar-Lisco
- Swanson Analysis Systems Inc.
- Teradyne Inc.
- Valid Logic Systems Inc.
- Viewlogic Systems Inc.

Dirk Wauters, Director of Marketing for Integration Products at Valid Logic Systems Inc., asserts that "our support of PowerFrame through the PowerFrame Synergy Program gives customers the opportunity to create a standard inter-departmental working environment that incorporates different processes, such as electrical and mechanical engineering. The loose coupling of PowerFrame complements the tight integration of tools provided by Valid's Design Process Framework, making it easier for customers to both develop their own integrated software environment and manage their unique design processes."

"PowerFrame will do for design management what Unix did for operating systems," states Tony Zingale of Cadence Design Systems. He continues that "users now have a true open environment that supports the entire product-development process."

Program participants exchange information through meetings and technical forums, and have an opportunity to influence enhancements to the framework through direct contact with developers. The program also supports standards by continuing to build established standards into the PowerFrame system, as well as working in reverse to ensure that key features of PowerFrame are incorporated into future framework standards. In addition, the program provides the foundation and support necessary to quickly integrate a broad range of tools and services under the PowerFrame umbrella.

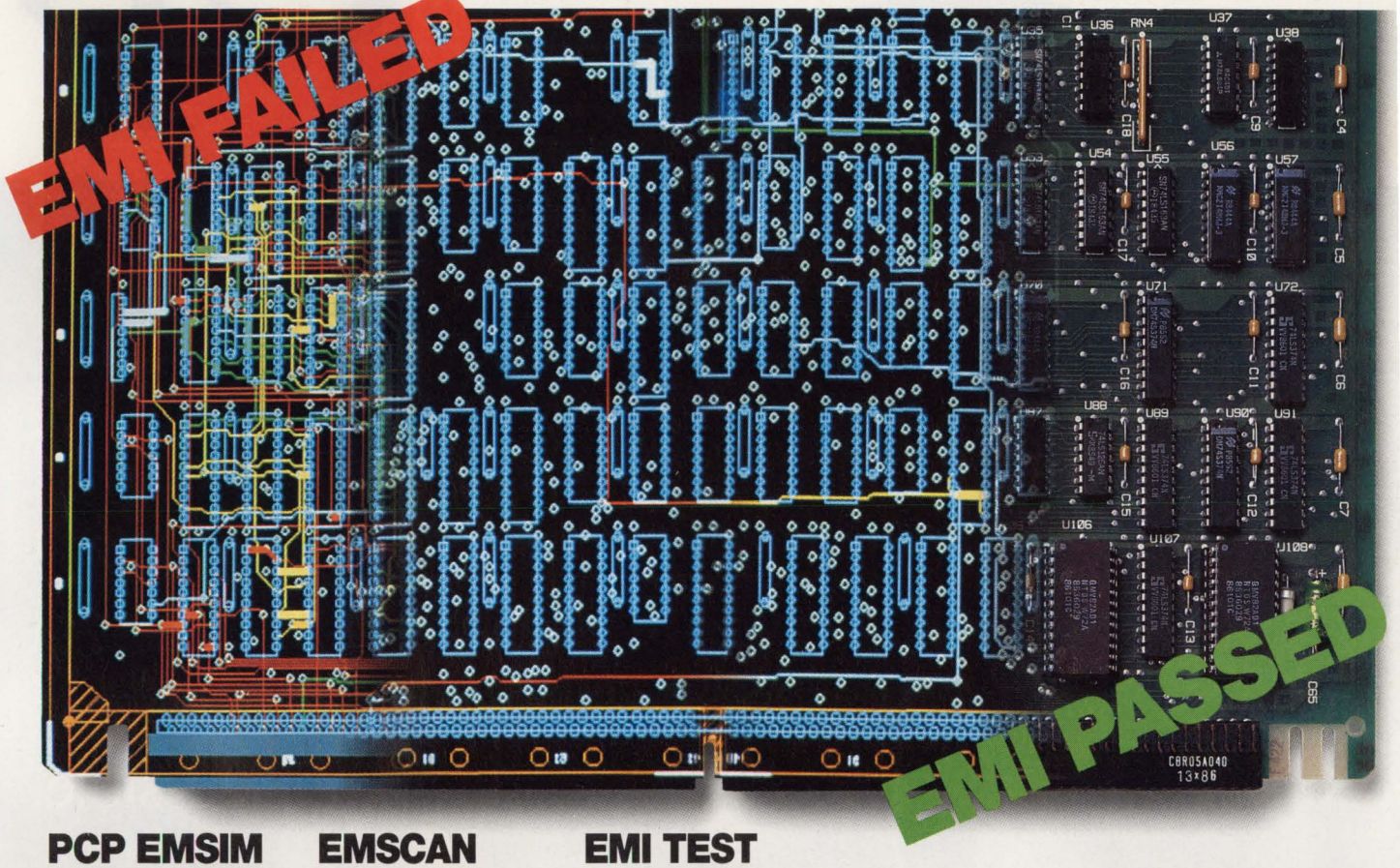
jectives today. By exploiting the key existing standards, PowerFrame provides many of the open features that CFI is striving for.

While the CFI effort to devise standards continues, another cooperative effort, one that focuses on PowerFrame, has sprung up to cement support for the framework and the promise it holds for a truly unified design environment *(see PowerFrame Synergy Program, this page)*. The PowerFrame Synergy Program reflects the rapid acceptance that PowerFrame has garnered from the engineering community.

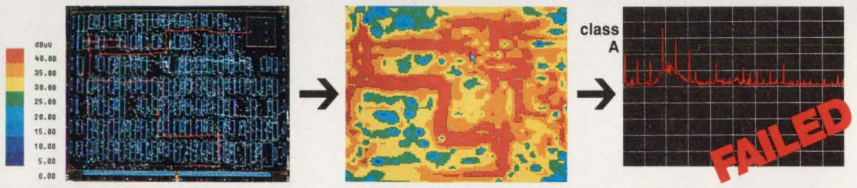
In addition to the industry players that are rallying behind PowerFrame, Digital itself stands ready to support the framework's users. A safety net of service and support specialists can fill any gaps in in-house resources to help ensure that the transition to concurrent, PowerFrame-based engineering is smooth and effective. Networking experts can help link all brands of workstations and mainframes into a seamless system. Software specialists can bridge any application rifts. And PowerFrame experts can encapsulate tools and help set up the system to fulfill design objectives. The overall result is a security blanket of assistance that makes the transition trouble-free.□

Minimize EMI During PCB layout before you build it!

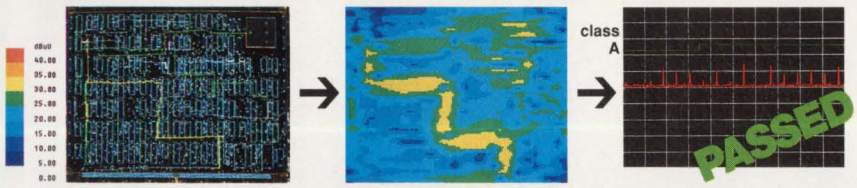
Get your product to market fast and save time and money in the process! Now you can optimize your circuit boards early in the design cycle before hardware prototyping with a simulation tool developed by Bell-Northern Research for Northern Telecom. As a complement to the circuit board design system CBDS, PCP EMSIM allows designers to select, position and route components for minimum EMI emissions, decreasing the risk of failing government regulations, such as FCC, CISPR and VCCI.



PCP EMSIM **EMSCAN** **EMI TEST**



Hot traces (shown in red) identified early at the layout stage with PCP EMSIM indicate that this board design will likely fail EMI radiated emission tests. As shown here, subsequent board testing on the EMSCAN hardware scanner and open field tests confirm the PCP EMSIM results.



Optimizing component selection, placement, and routing using PCP EMSIM enables you to reduce EMI before costly hardware prototyping. Scanning the revised prototype board on EMSCAN confirms the reduction in EMI, which is again verified by open field tests.

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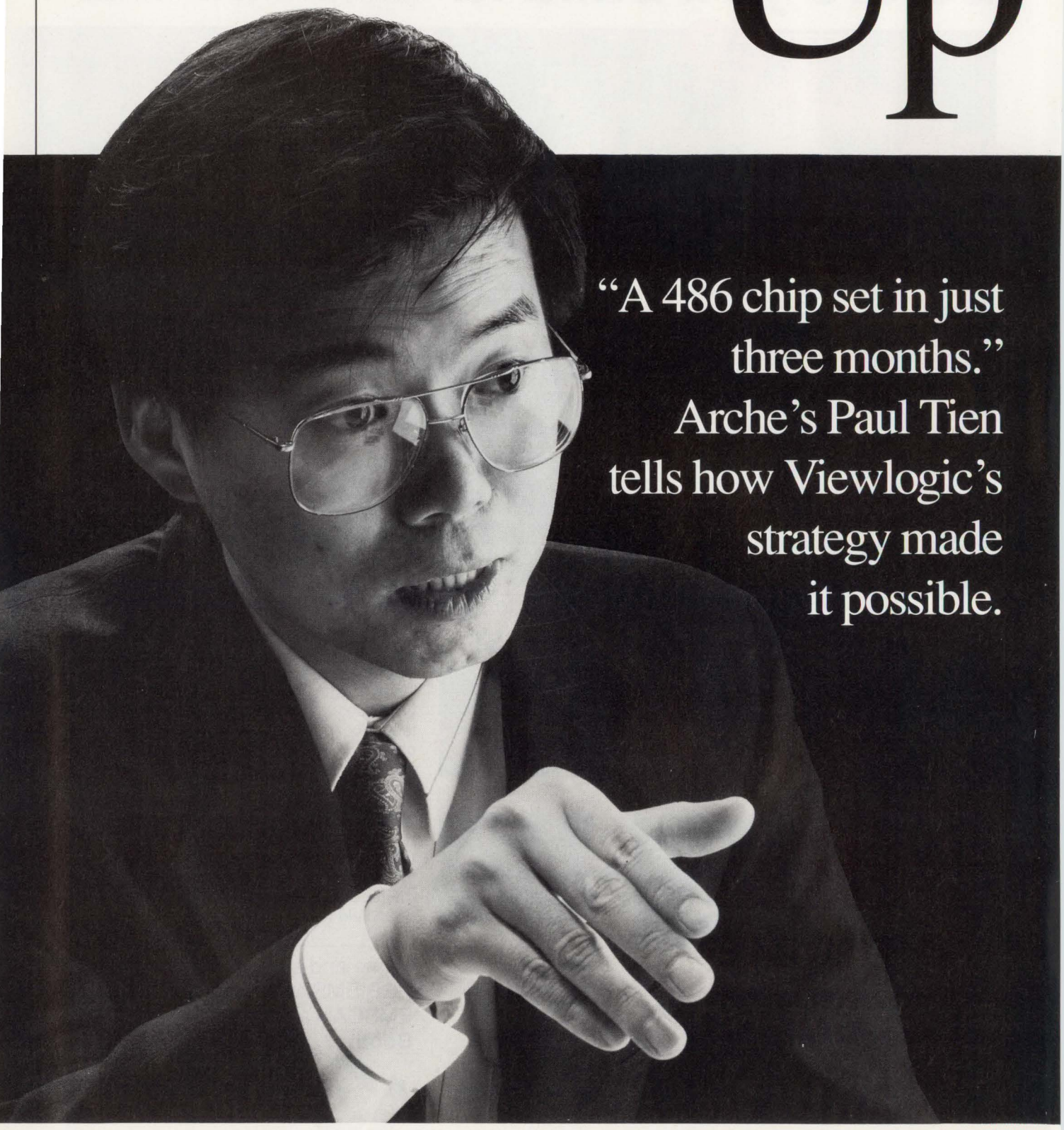

"A 486 chip set in just three months." Arche's Paul Tien tells how Viewlogic's strategy made it possible.

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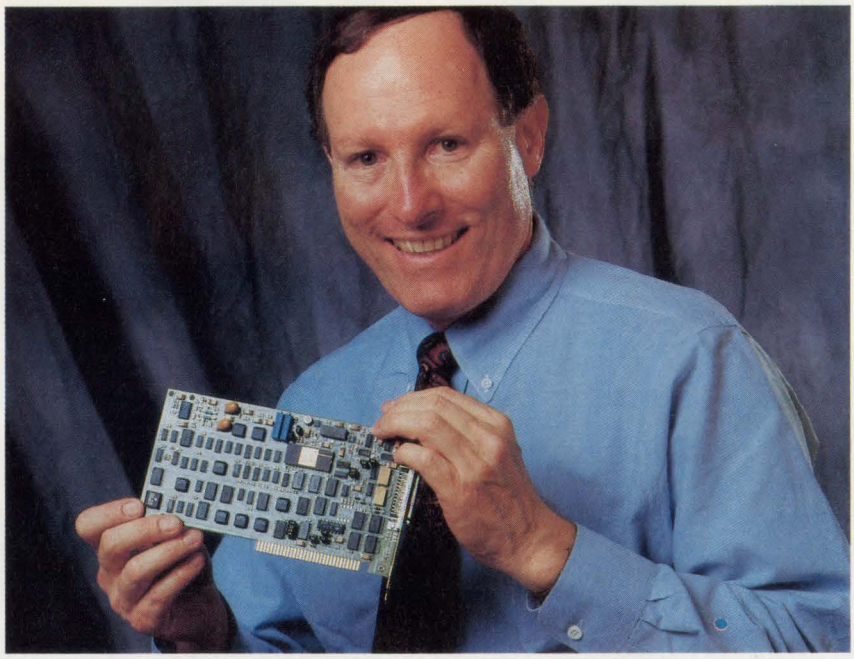

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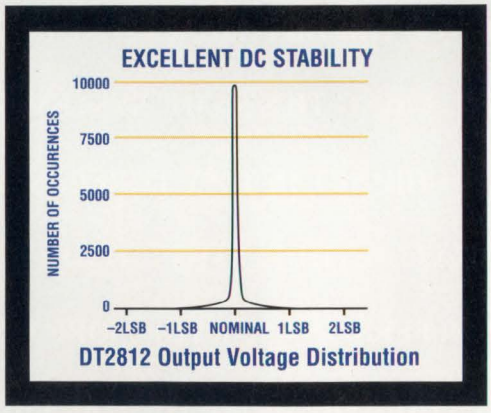

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BRIDGE THE GAP BETWEEN SIMULATION AND HARDWARE PROTOTYPING

THE INTEGRATION OF A DSP DESIGN ENVIRONMENT AND A WAVEFORM GENERATOR LINKS DSP SIMULATION AND TEST.

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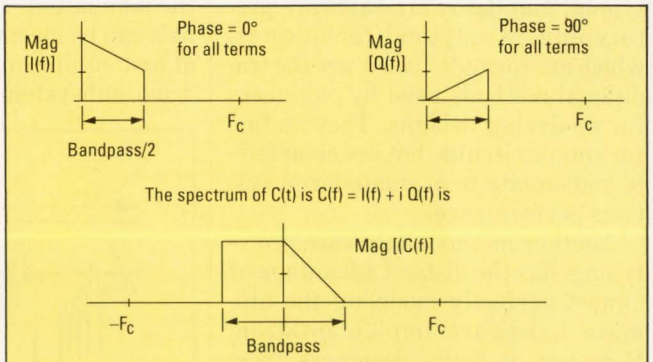
Digital designers can cross the simulation and hardware-prototype phase of a design with relative ease. Within the hardware-prototyping environment, designers can use ASICs, custom chips, or assemblies with the same digital test patterns that were used during the simulation phase. Communication-systems designers, particularly those employing digital-signal processing (DSP), haven't been so fortunate. This is due to the gap between the system simulation environment and the actual hardware under test.

In the last two years, DSP design tools have surfaced that let designers define a communications system at a high level of abstraction and perform what-if analysis on algorithms under consideration. To supply a simulation with signals that the system might actually encounter, designers can construct the test signal using a signal-display editor, compose a signal algorithmically, or capture a real-world signal using digitizing instrumentation. By using these test signals and making algorithmic trade-offs, substituting fixed-precision functional blocks, selecting coefficients, and so forth, the system is completely verified—and it all takes place within the DSP design workstation environment.

Designers then proceed with system-level simulation using the same set of test vectors that were used in the DSP subsystem design environment. Because most DSP systems are built subsystem by subsystem, designers would really prefer to substitute a hardware subsystem in place of the software simulation subsystem, exercise that hardware with actual signals, and return the hardware's output back into the software simulation. As the design progresses, more of the hardware subsystems replace software blocks until finally, the entire system resides in hardware.

This design strategy provides verification and the opportunity to optimize throughout the design cycle. Implementing such a strategy requires the ability to convert node signals in a communications-design block-dia-

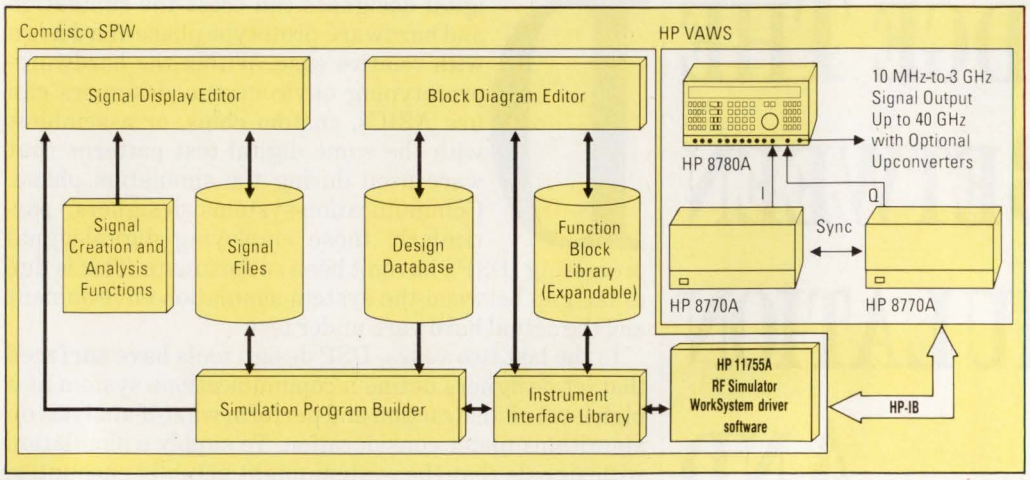


A non-symmetrical complex spectrum is typical when both AM and PM are present. There is no carrier (F_c) term in C(t).

Source: AT&T

1. THE MODULATION SPECTRA within a given passband can be represented by I(t) + j × Q(t). The Mag [I(f)] and Mag [Q(f)] plots added together create the Mag [C(f)].

LINKING DSP SIMULATION AND TEST



2. THE RF SIMULATOR worksystem consists of the Comdisco Signal Processing WorkSystem tightly integrated with two HP 8770A Arbitrary Waveform Synthesizers, each with a 50-MHz baseband bandwidth. The synthesizers drive the I and Q modulation inputs of an HP 8780A Vector Signal Generator.

gram environment into actual electrical signals. Comdisco Systems' Signal Processing WorkSystem (SPW), working with Hewlett-Packard's Vector Arbitrary Waveform Synthesizer, bridges that gap with a methodology that's generally applicable to the integration of DSP design environments and arbitrary waveform generators *(see "Using the Signal Processing WorkSystem," p. 80).*

Simulation facilitates design optimization because designers can readily evaluate many different circuit configurations. System performance can be evaluated four ways: analytical techniques, hardware prototyping, software simulation prototyping, and hardware-software prototyping. Analytical techniques, which are formula-based, are the traditional methods used by engineers for analyzing designs. They're fine for simple circuits, but are completely inadequate to evaluate large systems performance.

Another method, hardware prototyping, has the distinct advantage of almost perfectly modeling the ultimate hardware implementation. However, it limits designers from experimenting with such things as alternative algorithms, approximation methods, and rounding-truncation schemes. In addition, hardware prototyping is often too expensive and takes too much time.

The third method, software-simulation prototyping, uses predefined blocks that are interconnected on a workstation screen. This method gives users an interactive interface to optimize algorithms, bus widths, and coefficients. Using global parameter setting, users can write simulation macros that allow them to automatically launch multiple simulations of various scenarios.

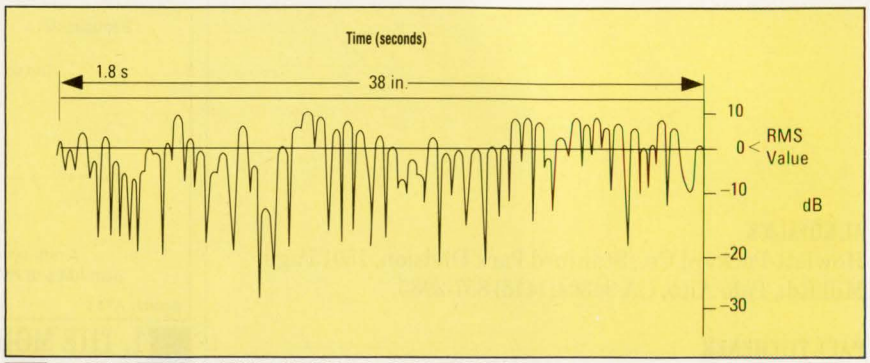
Finally, the fourth method, hardware-software prototyping, goes an important step beyond software-only prototyping. It enables the output node or any intermediate node to be probed, thereby generating the actual electrical signal that's defined mathematically at the probed node in the simulation. These electrical signals can be measured by conventional test equipment or can be used to drive subsystems in the hardware prototype.

The method for modeling communications systems must allow an interface between the software simulation and the hardware that generates real-world signals. In SPW, modeling communications systems involves operating on sampled waveforms.

Sampling theory contends that signals must be sampled at or above twice the frequency of the signal's maximum frequency content. However, in a bandlimited situation, frequencies below the bandpass don't convey any useful information (these components are zero). A more efficient signal-modeling approach is to sample the modulated waveforms am(T) and phase(t), in effect reducing the required sample rate from twice the highest signal component to twice the passband bandwidth. The real signal (polar form) can be expressed as:

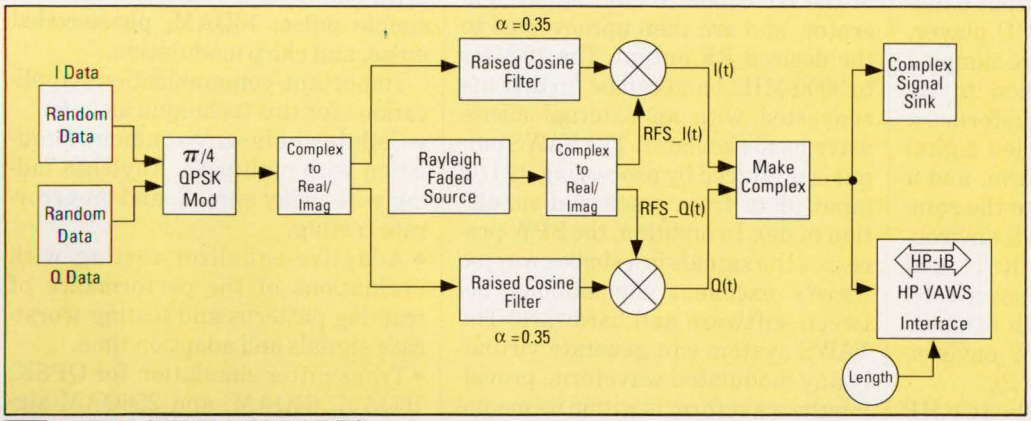
$$\text{Real Signal: } S(t) = am(t) \times \sin(W_c \times t \times \text{phase}(t))$$

Any real signal can be expressed as a function of its amplitude-modulation (AM) and phase-modulation (PM) components. Equivalently, the complex signal C(t), with a magnitude = am(t) and phase = phase(t), can be expressed in rectangular co-



3. PLOTTING THE SIGNAL STRENGTH versus time shows the typical received signal variations at 836 MHz measured at a mobile speed of 15 miles/hr.

LINKING DSP SIMULATION AND TEST



4. THE SIX MAIN PARTS of a single-ray model in a cellular faded channel simulation are (from left to right): a digital source of data, a modulator, the required I and Q Nyquist filtering, a source of Rayleigh distributed signals satisfying the model, mixers to combine the effects of fading on the modulated signal, and the HP VAWS interface block.

ordinates as:

$$C(t) = I(t) + j \times Q(t)$$

where

$$I(t) = am(t) \times \cos(\text{phase}(t)) \text{ and}$$

$$Q(t) = am(t) \times \sin(\text{phase}(t))$$

$$\text{Also, } S(t) = \text{Real}[C(t) \times e^{j \times w_c \times t}]$$
$$= I(t) \times \cos(W_c \times t) - Q(t) \times \sin(W_c \times t)$$

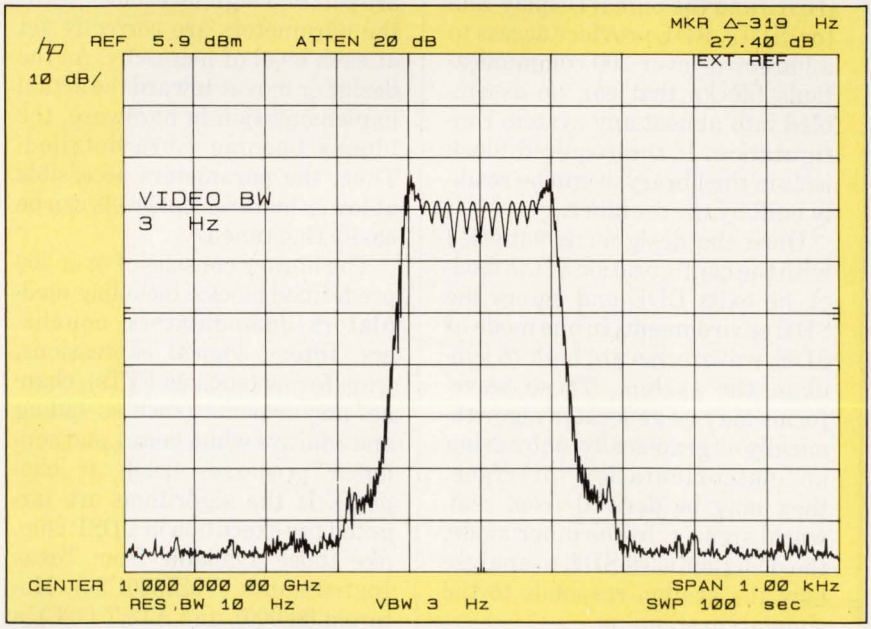
This second form of S(t) expresses the modulated signal in terms of signal components in phase with the carrier, W_c, and in quadrature with the carrier (I and Q components). The signal's modulation is contained in the complex time C(t). This term contains no function of W_c *(Fig. 1)*. Note that the spectrum of C(t) isn't symmetrical around zero frequency, a typical occurrence when S(t) has both AM and PM components. SPW uses the C(t) phasor representations to perform such signal-processing operations as filtering and adding noise.

SPW and the HP Vector Signal Generator can be integrated into the RF Simulator WorkSystem because SPW generates values of I and Q at every node, as represented by C(t), and the HP Vector Signal Generator has I and Q inputs. The C(t) value only contains passband information, not where the passband is located. S(t) is the output of the HP Vector Arbitrary Waveform Synthesizer (VAWS).

The SPW can be linked to hardware. An instrument-driver block can be pointed to any node in the simulation system, and the signals downloaded to a hardware signal-generation system, such as VAWS. The signal-generation system will generate real signals to test hardware prototypes.

VAWS consists of two HP 8770A Arbitrary Waveform Synthesizers (AWS), each with a 50-MHz baseband bandwidth. The synthesizers drive the I and Q modulation inputs of an HP 8780A Vector Signal Generator. The HP 8780A generator (an I/Q modulator) covers the frequency range of 10 to 3000 MHz. One HP 8770A supplies the In-phase input and another provides the Quadrature input. The system is controlled from the SPW software through an IEEE-488 HPIB bus. Each Arbitrary Waveform Synthesizer contains a 512k-sample-point memory. The I and Q values of a simulation result are downloaded to these memories, which then pass through a 12-bit digital-to-analog converter (DAC) and amplifier. The output is a real-life test signal. With 512k 12-bit words (an AWS typically clocked at 125 MHz), up to 4 ms of a 100-MHz bandwidth signal can be simulated. In addition, a divided AWS clock makes it possible to generate an 11-second scenario with 30 kHz of bandwidth at any desired carrier frequency.

The AWS is like a home CD player,



5. THIS PLOT SHOWS the signature spectrum of the channel simulator with a 100-Hz Fdoppler. The modulator was disabled for this signal. As expected, the power spectral density has the "smile" shape.

LINKING DSP SIMULATION AND TEST

but with a much larger output bandwidth (50 MHz). As in a CD player, AWS has a memory to store sampled data waveforms, a method to sequence through these waveforms, a DAC to convert the sampled digital data to an analog waveform, and a low-pass filter to eliminate the sampling energy. In the VAWS environment, the AWSs store I(nT) and Q(nT) sampled data, respectively. The AWSs are loaded with sampled data points from the SPW environment over the HP-IB *(Fig. 2)*.

The analog outputs of the two HP 8770A's are fed to the I and Q inputs of the HP 8780A Vector Signal Generator, and are then upconverted to the desired RF output. The 10-MHz to 3000-MHz band can be further upconverted with an external microwave local oscillator. The VAWS output is produced by processing its I/Q input (data from a selected simulation node). In addition, the SPW processes the signals in a similar way, so there's excellent compatibility between software and hardware. The VAWS system can generate virtually any modulated waveform, providing the waveform is within its memory capability of 512k words and 100-MHz bandwidth. These include AM, simple pulse, 16QAM, phase-coded pulse, and chirp modulation.

Important communications applications for this technique include:

- Cellular-radio-environment simulation with multipath, Rayleigh fading with delay spread, and bit-error-rate testing.
- Adaptive-equalizer testing with evaluations of the performance of training patterns and testing worst-case signals and adaption time.
- Transmitter simulation for QPSK, 16QAM, 64QAM, and 256QAM signals; $\pi/4$ DQPSK, MSK, and GMSK

USING THE SIGNAL PROCESSING WORKSYSTEM

Comdisco Systems' Signal Processing WorkSystem (SPW) is the software-simulation environment used in the hardware-software simulation approach. It's the front-end to Hewlett-Packard's RF Simulation WorkSystem. SPW is a graphical, interactive simulation tool for the design, analysis, and testing of communications systems. It operates on HP/Apollo and Sun workstations.

SPW consists of two environments: the Block Diagram Editor (BDE) and the Signal Display Editor (SDE). BDE provides access to a library of over 300 communications blocks that can be assembled into almost any system configuration. If the required block isn't in the library, it can be readily built by the designer.

Once the designer is satisfied with the configuration of the model, he exits BDE and enters the SDE environment. In one mode of SDE, waveforms are built to simulate the system. These waveforms may be generated algorithmically or graphically, or by using an instrumentation interface, they may be derived from real-world signals. In the other mode, the designer uses SDE to analyze how the system responds to the simulation stimulus.

For example, the designer can "build" a satellite communications system in the BDE and then generate a data stream in the waveform builder of the SDE. Once accomplished, he can analyze the output waveform to determine the bit-error-rate of the output data stream.

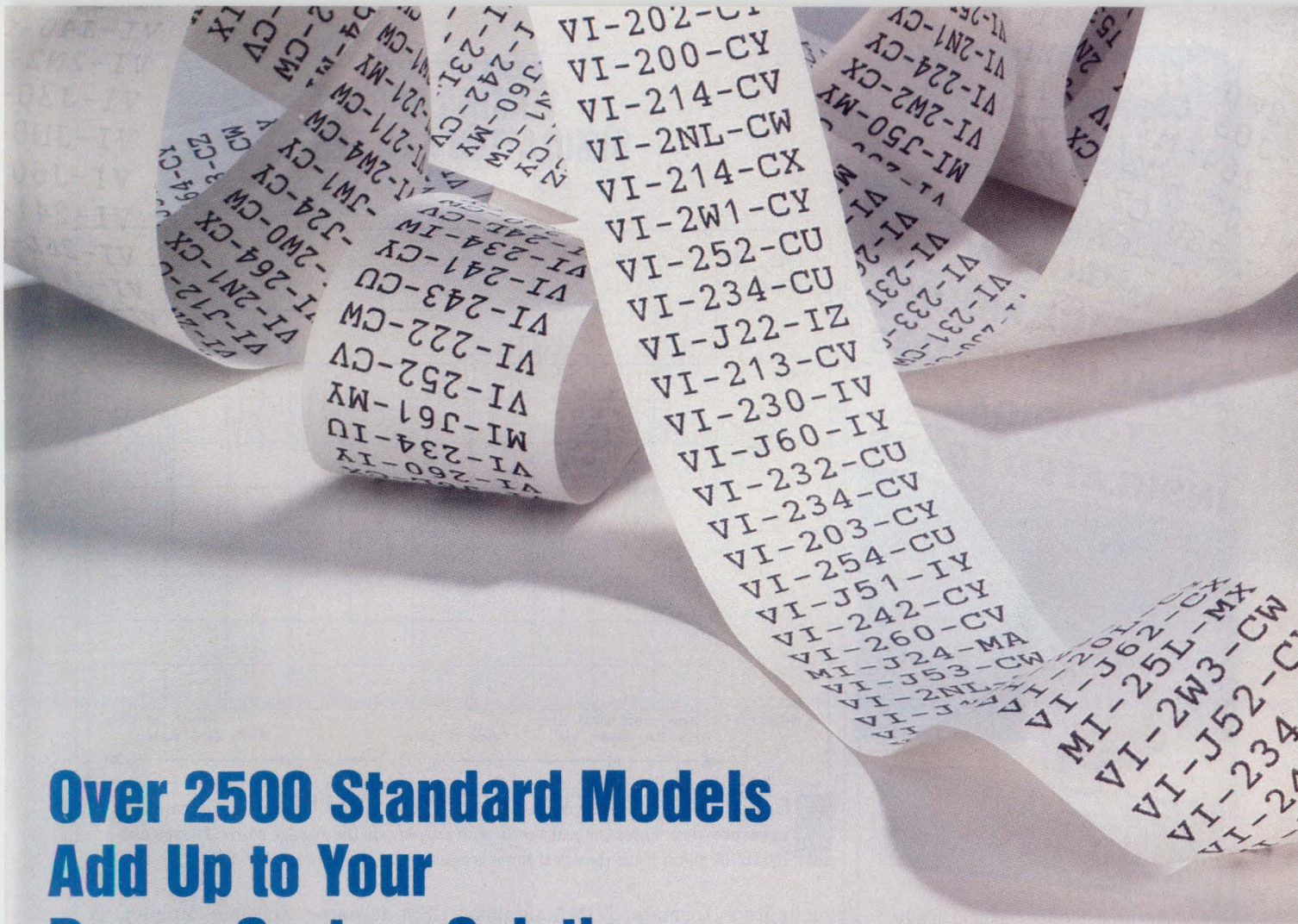
One key feature of SPW is that the blocks are hierarchical. At the beginning of the design cycle, the designer can optimize algorithms without worrying about the detailed structure. This frees him to focus in on the creative thought process. When the parameters are set for a high-level block, all of the parameters are correctly set at each level of hierarchy. As the designer moves toward the actual implementation in hardware, the blocks become more detailed. Thus, the parameters accessible at lower hierarchical levels can be easily fine tuned.

The library consists of over 300 predefined blocks, including modulators/demodulators, equalizers, filters, logical expressions, transforms (such as FFTs), channel impairments (such as fading and additive white noise), and nonlinear processes (such as clipping). If the algorithms are targeted for execution in a DSP chip, like those available from Texas Instruments (TMS320C30), Motorola (96000), and AT&T (32C), a Code Generation System (CGS) is used. CGS outputs code designed to exploit the assembly-language routines that are provided for each processor.

On SDE's analysis portion, results can be displayed in such forms as time plots, frequency plots, eye diagrams, or constellation diagrams. The user can easily analyze the effects of filtering, see the impact of adding (or modifying) channel impairments, or test the limits of the design.

At the beginning of the design process, where algorithmic verification is the key concern, the designer typically uses floating-point arithmetic throughout. However, in the real world, where hardware minimization must be traded for system performance, the designer is often constrained by considerations like fixed multiplier/accumulator widths, bus widths, and coefficient rounding/truncation.

Consequently, fixed precision arithmetic will likely be used. Comdisco's Hardware Design System (HDS) addresses this need by allowing the designer to substitute fixed-precision blocks for floating-point blocks on a one-for-one basis. Each of the fixed-precision blocks has a parameter entry port that's used to set the fixed-precision parameter attributes, like bus width, and the method for handling coefficient rounding/truncation.



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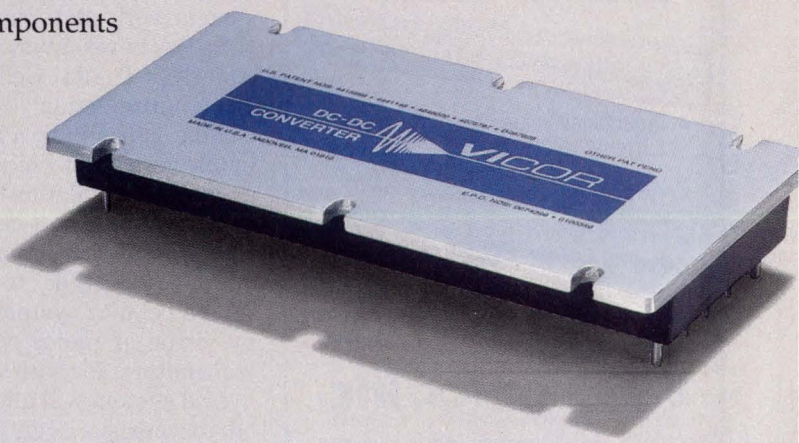

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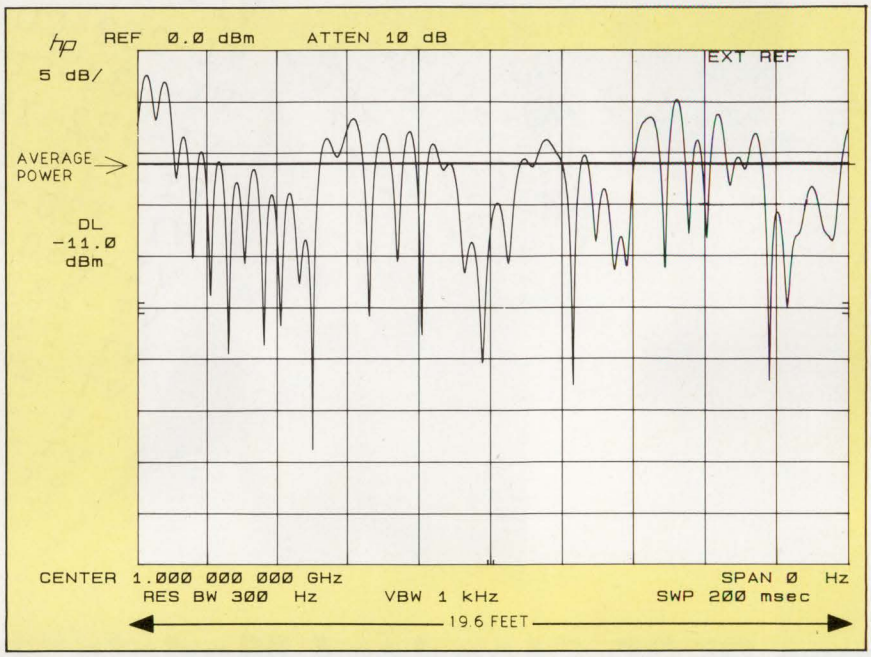

6. THE VAWS CHANNEL SIMULATOR OUTPUT is the signal envelope power over time. Fades and peaks occur with reference to the average power. Fdoppler = 100 Hz (67 m.p.h.), and the signal power is measured over a distance of 19.6 ft.

modulation formats; TDMA signals and signal-plus-noise generation.

One area of intense R&D and marketing interest is cellular communications. For instance, any metropolitan area is full of vehicles with cellular phones. During peak hours, customers often find it difficult to get channel access due to the demand for service. So, it's not surprising that service providers are anxious to increase the number of available channels. One solution to the overcrowding problem is to introduce a new system with more capacity. In the U.S., this new system is called North American Digital Cellular (NADC). Upon introduction, it will increase channel capacity by a factor of three by clever use of voice compression and a new modulation technique. The NADC method will be included in a new hybrid system that will be backwards compatible to the existing AMPS cellular system (Analog FM) by virtue of radios with receivers/transmitters for both standards. The hybrid system will allow each method to coexist. Eventually, though, the AMPS system will be phased out.

In Europe, the emerging standard for cellular communications is called GSM (Groupe Speciale Mobile). It also uses digital methods to compress voice and achieve excellent channel capacity beyond the older analog methods. Japan is forging ahead toward introducing a digital cellular system. Moreover, several large companies are investigating PCN (Personal Communication Network) to provide cellular service for the person on the street. Here, users will carry a small radio and be connected to the network through an arrangement of "microcells." These nascent technologies will become commonplace in a few years.

The surge in new techniques and systems to satisfy the public's appetite for cellular services has produced a corresponding need in laboratories around the world to simulate these systems. Using the SPW environment and accepted channel models, users can simulate a realistic channel environment with multipath fading. By including HP's VAWS hardware, the same users will have available an RF output that corresponds to the simulated channel with fading. Also, users can modify the channel characteristics and transmitter parameters to test the limits

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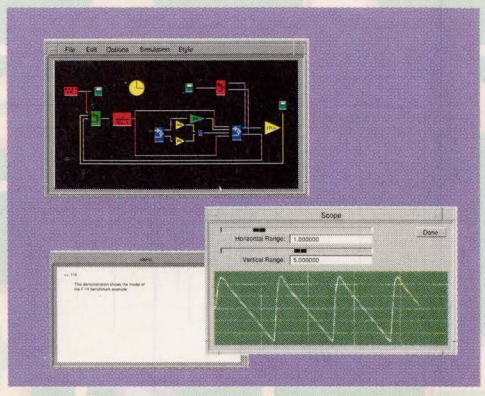

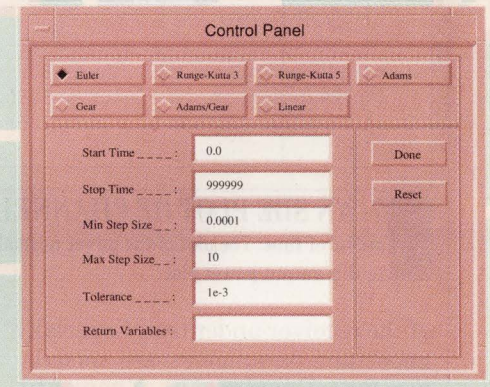

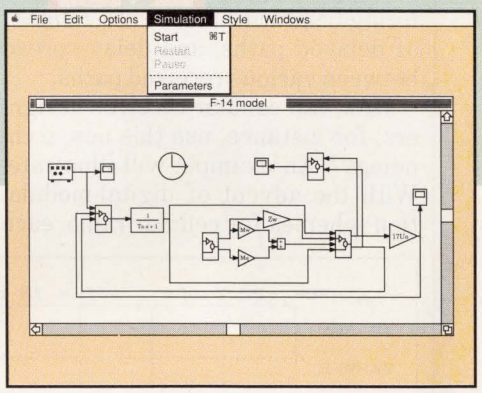

(Top) Use the Scope block to see the "real-time" response of this F-14 model during the simulation; (Center) Specify simulation parameters via dialog boxes or the MATLAB command line; (Bottom) SIMULAB takes full advantage of the X/Motif and Macintosh windowing systems.

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CIRCLE 165

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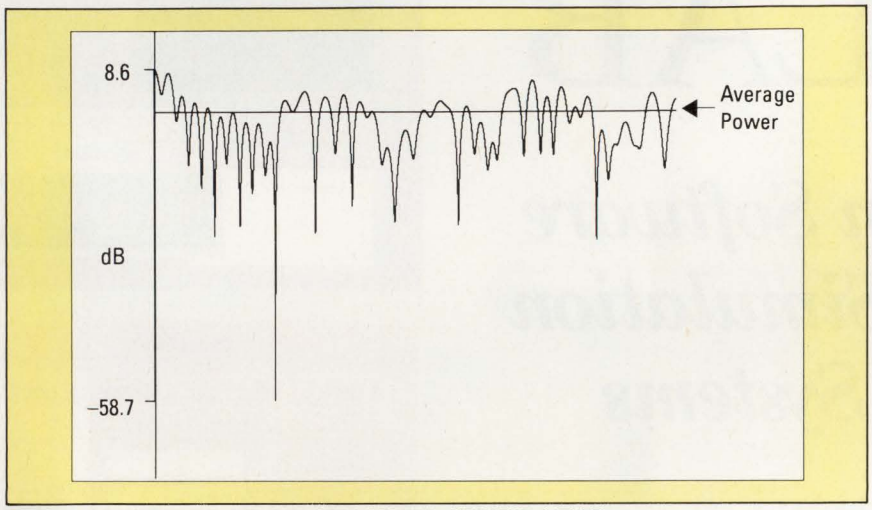
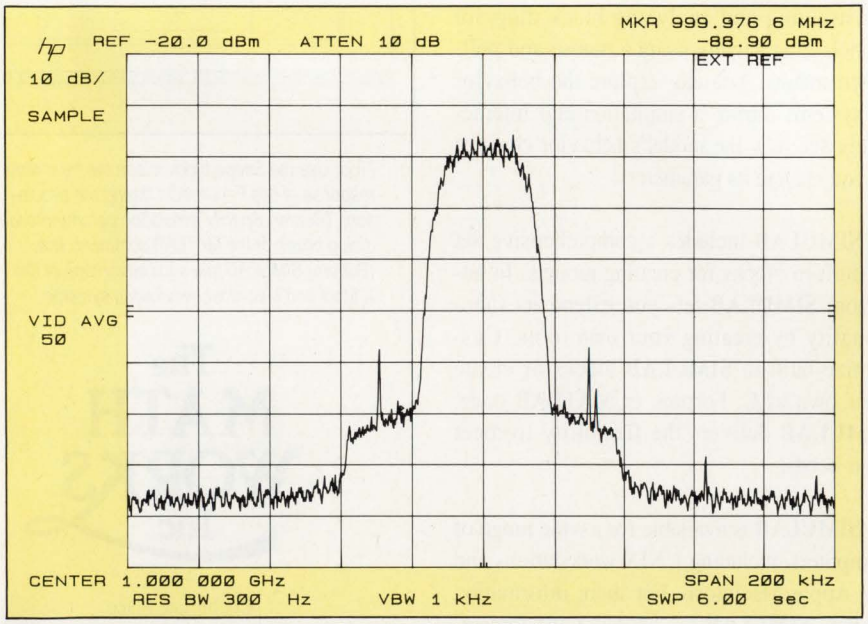


7. AN SDE PLOT OF CHANNEL SIMULATOR output shows power over a period of time. The plot of the power normalized envelope of S(t) in Fig. 6 should be identical to this output-power plot.

of the receiver under test. Especially important parameters are modulation type, Doppler shift, Nyquist filtering bandwidth, fade rate, number of delayed paths, and delay spread between various received paths.

How can cellular-receiver designers, for instance, use this new technology? An example will illustrate. With the advent of digital-modulation schemes for cellular radio, each receiver will have an adaptive filter. The filter adapts to the changing channel and attempts to restore normalcy to it. Designing such a filter is difficult. Users can design and simulate the target filter with the SPW. An SPW channel and transmitter model generates signals to test it as well. Once users are satisfied with the simulation, actual hardware is built. Next, this hardware may be tested using the VAWS output with exactly the same signals that were used during the simulation phase of the design. Thus, the loop between design and bench test can be closed.



8. THE SPECTRUM FOR THE CELLULAR channel signal has a $\pi/4$ differential QPSK modulated, Nyquist-filtered, random data signal. The two spurious signals (–77 dBm) around the main lobe result from power-supply leakage. They're not an artifact of the signal. Also, the effects of fading can't be seen by observing this spectrum.

As an example of closing loop between design and bench test, consider a simulation in SPW of a multipath faded channel and transmitter. To get a feel for the model requirements, imagine the signal received from a moving vehicle antenna. As the vehicle navigates through its environs, the received signal will show a wide range of dips and peaks in received power *(Fig. 3)*. It's unavoidable that these dips or fades occur. They are a result of receiving, while moving, the transmitted signal after it's scattered off stationary objects.

It's necessary to simulate and generate this signal. Traditionally, it's generated by playing back the same signal that was recorded while driving around city streets. With SPW, an equivalent signal will be simulated, using the Rayleigh-faded model for channel simulation. This model produces an equivalent received signal, S(t), with the received envelope power following Rayleigh statistics. A signal with a Rayleigh distributed envelope may be described as:

$$S(t) = I(t) \times \cos(W \times t) - Q(t) \times \sin(W \times t)$$

where I(t) and Q(t) are signals that include the effects of fading and modulation and W is the carrier radial frequency.

The received envelope of S(t) is R(t) and may be described by:

$$R(t) = (I(t)^2 + Q(t)^2)^{0.5}$$

This is the amplitude, in volts, of the AM part of the signal. It's this component that's Rayleigh distributed.

Using SPW to simulate the single-ray channel model is straightforward. Here, the modulator uses the $\pi/4$ Differential QPSK method, a method used by North American Digital Cellular. The six main parts to the model are (from left to right) a digital source of data, a modulator, the required I and Q Nyquist filtering, a source of Rayleigh distributed signals satisfying the model, mixers

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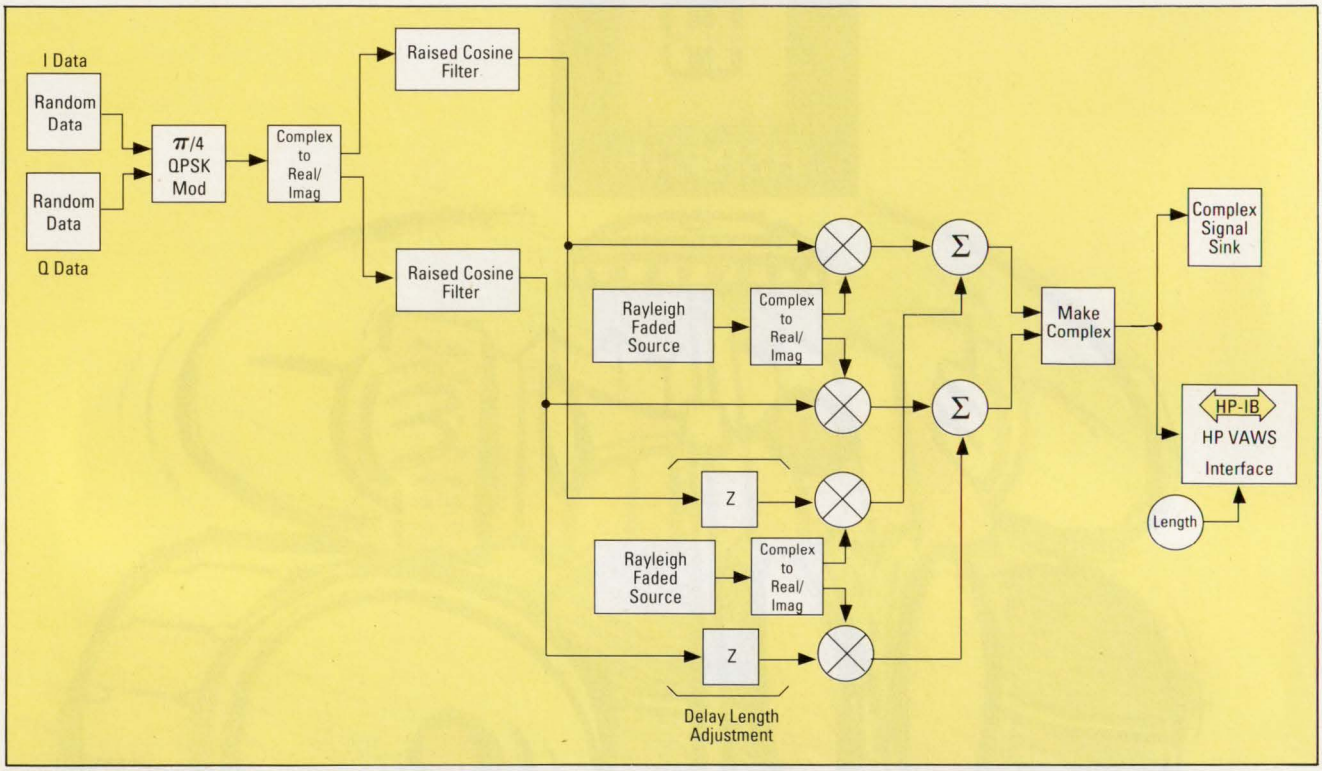

9. ADDING MORE RAYS to the single-ray model causes the received signal to contain delayed and faded versions of the transmitted signal. These added rays are needed to model a received signal in a typical environment with several far and near reflectors.

to combine the effects of fading on the modulated signal, and the HP VAWS interface block *(Fig. 4)*.

The digital data may be any pattern specified by the user. In this simulation example, it's random 1,0 data. The choice of modulator depends on the transmission scheme. The Nyquist filters must limit the transmitted spectrum width. For the NADC receive or transmit channel, the occupied bandwidth is limited to 30 kHz. For the existing non-digital U.S. system, two 30-kHz channels (one transmit, one receive) are required to carry on a single conversation. For the proposed NADC system, three conversations will be time-division multiplexed in the same bandwidth. For the simulation example, the sample clock is 72 kHz, the bit rate is 48 kbits/s, and the symbol rate is 24 ksymbols/s. The Nyquist filter is a 65-tap raised cosine filter with an excess bandwidth parameter (alpha) that equals 0.35.

The block labeled "Rayleigh-faded source" is of particular interest. This block supplies two statistically independent Gaussian-distributed signals, both with a special amplitude weighting. This block is responsible for the required dipping of the signal in the power plot. Because RFS_I(t) and RFS_Q(t) are Gaussian, the output envelope signal, R(t), will be Rayleigh. If the rectangular components of a signal (I and Q) are Gaussian, then the polar amplitude component (envelope) distribution of the same signal is Rayleigh.[1]

The method behind the Rayleigh-faded source is based on the works of W.C. Jakes.[2] In his work, Jakes presents a method to generate the required RFS_I and RFS_Q with relative ease. For the Rayleigh-faded model, the required spectral density of the Gaussian signals must follow the function:

$$A(F) = (1 - ((F - Fcarrier) \div Fdoppler)^2)^{-0.5}$$

for F within Fcarrier $\pm$ Fdoppler. Otherwise, A(F) = 0. F is frequency, Fdoppler is the maximum Doppler shift expected due to the moving vehicle, and Fcarrier is the carrier of the transmitted signal.

The Rayleigh-faded block was prototyped in the SPW's Block Diagram Editor (BDE), then custom coded in C to increase simulation efficiency. The spectrum of RFS_I(t) and RFS_Q(t) was translated to 1 GHz by the VAWS system *(Fig. 5)*. Modulation was disabled for this plot. Therefore, Fcarrier = 1 GHz and Fdoppler = 100 Hz (67-m.p.h. vehicle speed maximum). The power-spectral density of the plot approximates A(F) as required. It has a characteristic "smile" shape. This is an important signature of any method that purports to model a Rayleigh-faded environment. The Jakes method uses the sum of nine oscillators with nonlinear frequency spacing from 0 to Fdoppler, random phase, and unity amplitude to approximate the required Gaussian noise with A(F) shaping. These signals are available as RFS_Q(t) and RFS_I(t). The approximation is better than 0.01%.

Another signature of the channel simulator is its output power versus time *(Fig. 6)*. A plot of the signal en-

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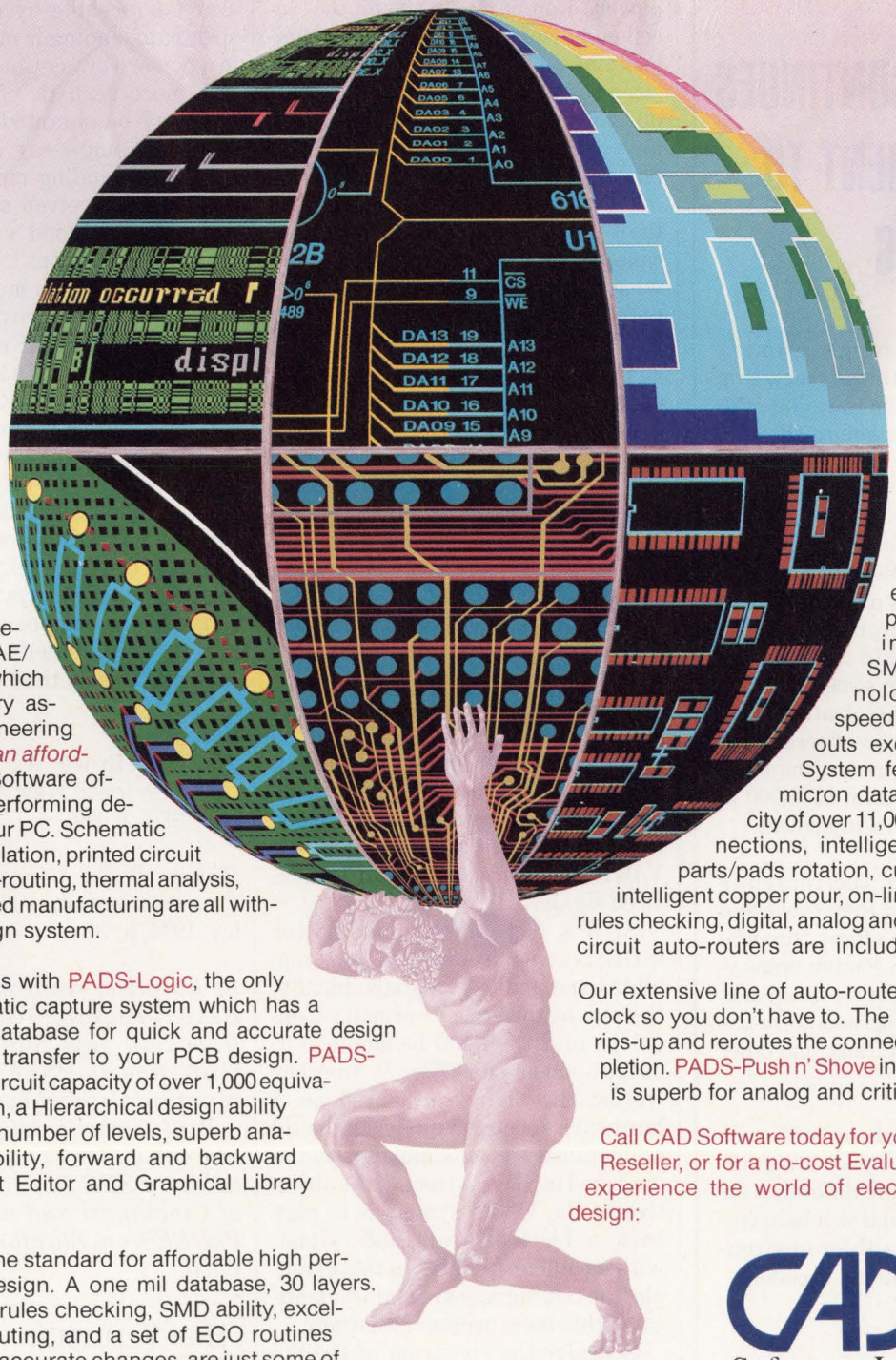

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velope power versus time is obtained from the VAWS system's output measured on a spectrum analyzer in zero span mode. The effects of the modulation have been averaged out.

In general, the modulation has little effect on the received envelope power. Comparing this to the received-power plot reveals the similarity of the signals, which is the desired result *(Fig. 3, again)*. The output-power signal has a peak power level of 8.6 dB above the average power. Also, a fade to –40 dB below the average power will occur less than 0.01% of the observed signal time. These power points are exactly what the ideal Rayleigh-faded channel would exhibit. The rate of fading is another key element for designers: A signal that fades very slowly is easier to work with than one that fades quickly.

Level-crossing rate (LCR) is a useful parameter for a real channel. The LCR is the number of times per second that the received signal power crosses its average value in the positive direction (coming out of a fade). According to theoretical figures, for a Fdoppler (maximum) of 100 Hz, the LCR should be 91 crosses/s. Looking at the signal, the LCR is seen to be 18 crosses in 0.2 seconds. This corresponds to 90 crosses/s. Considering the granularity of this simple measurement, the agreement is excellent. Therefore, the simulation and VAWS hardware generated the desired signal.

SPW's Signal Display Editor (SDE) is an environment that manipulates and analyzes signals. Ideally, the plot of the power normalized envelope of S(t) should be identical to output-power plot *(Fig. 7)*. In other words, the signal measured on a hardware spectrum analyzer should be identical to the simulated signal analyzed in SDE. After all, the objective of the VAWS system is to play back a block-diagram node signal with excellent fidelity. In this example, the two signals are almost identical within measurement accuracy.

Consider the spectrum of the entire modulated signal *(Fig. 8)*. This is a typical spectrum with a $\pi/4$ differential QPSK modulated, Nyquist-filtered, random data signal. The Nyquist filters have bandwidths of about 16 kHz each. The two spurious signals (–77 dBm) around the main lobe are due to power supply leakage, they're not an artifact of the signal. Moreover, the fading effects aren't noticeable by observing this spectrum. Fading is most easily seen in a power-versus-time plot.

A more realistic channel simulation may be obtained by modifying the basic single-ray model *(Fig. 4, again)*. By adding more rays to the model, the received signal contains delayed and faded versions of the transmitted signal. These added rays are needed to model a received signal in a typical environment with several far and near reflectors *(Fig. 9)*. With each ray of a 2-ray model being independently Rayleigh-faded, the second ray becomes distinguished by its "delay spread." The delay spread is the differential delay between the main undelayed ray and the other ray. More rays are easily added to the channel. The only limit to the number of rays is the dynamic range of the composite signal. A 12-ray, Rayleigh-faded signal is practical using this method.□

References:

[1]Carlson, Bruce A., *Communications Systems*, New York: McGraw Hill, 1975, p. 265.

[2]Jakes, W.C., *Microwave Mobile Communications*, New York: Wiley, 1974, p. 70.

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EXPLOIT DIGITAL ADVANTAGES IN AN SSB RECEIVER

IMPROVEMENTS IN DIGITAL CONVERSION TECHNOLOGY HELP RADIO DESIGNERS TAKE ADVANTAGE OF DIGITAL ARCHITECTURES.

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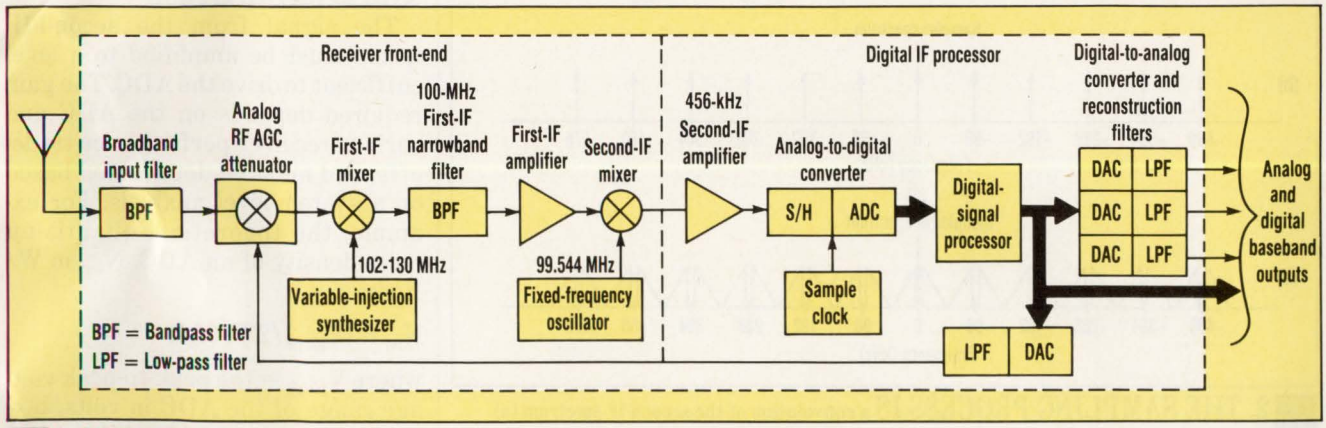
This article is the second of a two-part series on the design of digital radio receivers. The first part (ELECTRONIC DESIGN, May 23, p. 67) covered the fundamentals of digital radio and undersampling techniques, as well as selection criteria for the analog-to-digital converter. Part 2 covers the receiver design in greater detail.

The first step in digital-receiver design is to determine the radio's front-end specifications. The process is somewhat similar to that in a conventional analog design, but it must account for the characteristics of the digital IF processor used by the radio. After the front-end is completed, the designer can proceed to the IF processor, taking advantage of highly integrated devices to simplify the design.

The design example in this article is a 2-to-30-MHz SSB receiver employing undersampling techniques. A 16-kHz front-end bandwidth was chosen to accommodate up to four 3-kHz independent-sideband channels. This bandwidth also allows the digital-signal processor to perform fine tuning over at least a 1-kHz range, simplifying the variable-injection synthesizer *(Fig. 1)*.

The first IF is 100 MHz, which is high enough to ensure that the broadband input filter suppresses the IF and image response by 80 dB, but low enough to allow a low-cost crystal filter to be used as the first-IF narrowband filter. Because the DSP performs the fine tuning in 1-Hz steps, the variable injection synthesizer can tune from 102 to 130 MHz in 1-kHz steps. This "high-side" first-IF mixer injection causes a passband reversal or "flip" in the mixer, which will be corrected by the sampling process.

The first-IF amplifier makes up for losses in the first-IF mixer and filter, and maintains a front-end noise figure of 15 dB. After amplification, the signal is mixed with a fixed-oscillator signal of 99.544 MHz. The result is a second-IF of 456 kHz, which is high enough to allow the second-mixer image response at 99.088 MHz to be attenuated by 80 dB in the first-IF filter, but low enough to be sampled by the analog-



1. THE CHOICE OF 100 MHz for the first IF is high enough to ensure that the broadband input filter sufficiently suppresses the IF and image response but low enough to allow a low-cost crystal filter for the first-IF narrowband filter.

DIGITAL RADIO RECEIVER

to-digital converter (ADC).

If the ADC's sample-and-hold bandwidth is greater than 456 kHz, as is the case with the AD779, the receiver can undersample the second-IF signal efficiently at a sample rate of 96 kHz. Because the analog-to-digital conversion is effectively the result of a convolution of the input signal and the sample-clock impulse spectrum, the sample clock must be as "clean" and jitter-free as the local oscillator or mixer injection signal. Any phase noise present on the clock will be impressed on the signal being sampled, effectively corrupting it. If isolation or buffering is inadequate, the spurious noise picked up by the sample clock can be disastrous.

When the second-IF spectrum is convolved with the sample-clock impulse spectrum, the IF signal is frequency translated to a lower IF of one-fourth the sample frequency, or 24 kHz *(Fig. 2)*. The convolution also creates a passband reversal that counteracts the reversal in the first-IF mixer. As expected, the sampled-IF spectrum repeats at every multiple of the sample frequency.

In this example, increasing the second-IF bandwidth will create aliasing distortion or overlap in the sampled IF spectrum because real-world filters can supply only finite stopband attenuation *(Fig. 2, again)*. But aliasing can be reduced to an acceptable level. In this design, the passband width of 16 kHz must be alias-protected to 60 dB.

This requirement, and a look at the IF sampling process, lead the designer to the bandpass specifications of the first-IF filter *(Fig. 3)*. Because of the sampling frequency and second-IF selected, the filter must have an 80-kHz-wide stopband. Given the 16-kHz-wide passband, the corresponding shape factor is 5 to 1. Attenuation of signals 40 kHz from the passband center of 100 MHz must be at least 60 dB. As noted, another 20 dB of attenuation is also needed at the image-response frequency of 99.088 MHz. A typical passband ripple specification might be 1 dB. A 4- or 5-pole crystal filter might satisfy these criteria.

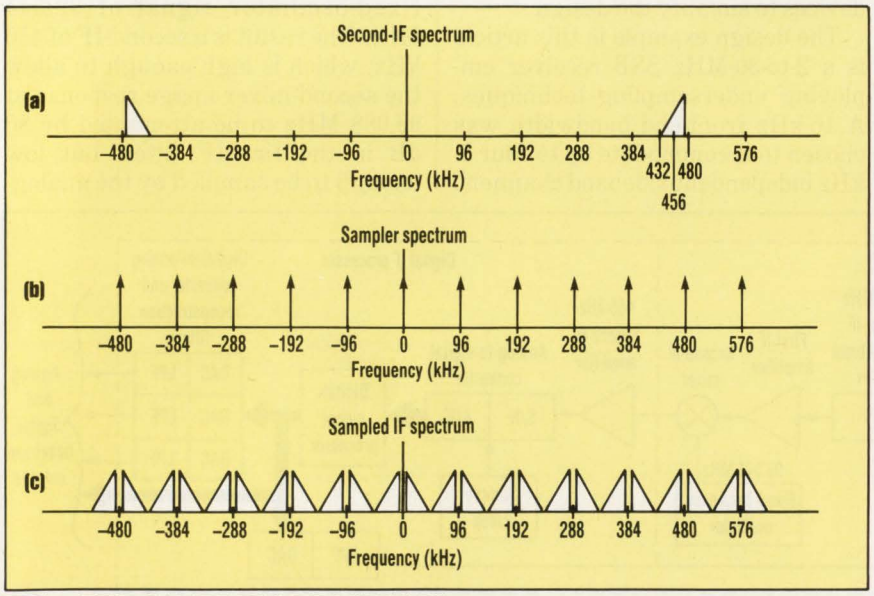
SPREADSHEET OUTPUT

Receiver performance for thermal-noise-limited example

Digital-signal-processor receiver gain distribution and noise performance

Analog RF/IF noise figure	15 dB
ADC resolution	14 bits
ADC full-scale level	5 V peak (23.98 dBm)
ADC quantization level	–60.31 dBm
ADC sample frequency	96 kHz
ADC input bandwidth (BW1)	16 kHz
Information bandwidth (BW2)	3 kHz
Analog AGC threshold	–77 dBm

Antenna signal level (dBm)	Analog RF/IF gain (dB)	ADC signal level (dBm)	Noise at ADC input in BW1 (dBm)	Noise at ADC input in BW2 (dBm)	Quantizing noise of ADC in BW2 (dBm)	Total noise in BW2 (dBm)	Output SNR in BW2 (dB)	Digital processor gain (dB)	Output signal level (dBm)	Antenna overload level (dBm)
–113.00	57.00	–56.00	–59.96	–67.23	–74.11	–66.42	10.42	60.00	4.00	–33.02
–103.00	57.00	–46.00	–59.96	–67.23	–74.11	–66.42	20.42	50.00	4.00	–33.02
–93.00	57.00	–36.00	–59.96	–67.23	–74.11	–66.42	30.42	40.00	4.00	–33.02
–83.00	57.00	–26.00	–59.96	–67.23	–74.11	–66.42	40.42	30.00	4.00	–33.02
–73.00	53.00	–20.00	–63.96	–71.23	–74.11	–69.42	49.42	24.00	4.00	–29.02
–63.00	43.00	–20.00	–73.96	–81.23	–74.11	–73.34	53.34	24.00	4.00	–19.02
–53.00	33.00	–20.00	–83.96	–91.23	–74.11	–74.03	54.03	24.00	4.00	–9.02
–43.00	23.00	–20.00	–93.96	–101.23	–74.11	–74.10	54.10	24.00	4.00	0.98
–33.00	13.00	–20.00	–103.96	–111.23	–74.11	–74.11	54.11	24.00	4.00	10.98
–23.00	3.00	–20.00	–113.96	–121.23	–74.11	–74.11	54.11	24.00	4.00	20.98
–13.00	–7.00	–20.00	–123.96	–131.23	–74.11	–74.11	54.11	24.00	4.00	30.98
–3.00	–17.00	–20.00	–133.96	–141.23	–74.11	–74.11	54.11	24.00	4.00	40.98
7.00	–27.00	–20.00	–143.96	–151.23	–74.11	–74.11	54.11	24.00	4.00	50.98
17.00	–37.00	–20.00	–153.96	–161.23	–74.11	–74.11	54.11	24.00	4.00	60.98



2. THE SAMPLING PROCESS IS a convolution of the second-IF spectrum (a) with the sampler spectrum (b). The resulting spectrum shows that if the second-IF bandwidth is increased, aliasing distortion will occur (c).

THE DIGITAL STAGE

The signal from the second-IF mixer must be amplified to a level sufficient to drive the ADC. The gain required depends on the ADC and various receiver performance trade-offs, and must be determined based on a system-level analysis. For example, the theoretical quantizing noise density of an ADC, N_{0q}, in W/Hz is:

$$N_{0q} = (V_{pk\text{-}pk}/2^b)^2/6f_sR$$

where $V_{pk\text{-}pk}$ = the peak-to-peak voltage range of the ADC in volts, b = the total number of ADC bits including sign, R = the assumed imped-

DIGITAL RADIO RECEIVER

ance in ohms, and f_s = the sampling frequency in hertz.

For a 14-bit ADC with a 10-Vpk-pk range and a sampling frequency of 96 kHz, $N_{0q} = 1.2935 \times 10^{-14}$ W/Hz or –108.9 dBm/Hz, assuming 50-Ω impedance normalization. Other noise includes the thermally generated receiver noise. The level of this noise is the front-end noise figure, 15 dBm/Hz, minus the thermal noise generated in a 50-Ω resistor, –174 dBm/Hz, or –159 dB/Hz.

The receiver's minimum weak-signal gain must be high enough so that the weakest desired usable signal plus the receiver noise is greater than at least one ADC quantizing level. If not, the signal won't be recovered. The best way to ensure a large enough signal is to provide sufficient noise at the ADC input to dither across a quantizing level. To do so, a designer can amplify the in-band receiver thermal noise or add out-of-band noise, which the digital-signal processor can filter out later. Although it may not be the better method, this article discusses the simpler approach of amplifying the receiver thermal noise until it bridges a quantizing level.

For the AD779, one quantizing level is 610 μVpk-pk. The equivalent sine-wave amplitude is then 215.8 μV rms or –60.3 dBm. Therefore, amplifying the receiver noise so that its rms level at the ADC is also –60.3 dBm will guarantee adequate bridging of a quantizing level. With the front-end noise bandwidth (BW) of 16 kHz, the gain required to amplify the receiver noise to this level is:

Gain = quantizing level – thermal noise density – 10log BW
= –60.3 dBm + 159 dBm/Hz – 10log 16,000 Hz
= 56.7 dB

A spreadsheet program can perform these calculations, and others, to interactively examine receiver performance for different ADCs, sample rates, bandwidths, and gain distributions *(see the table)*.

Note that in this example, the analog gain is high enough to allow thermal noise to bridge a quantization level. As a result, the receiver's noise performance is dominated by thermal noise, not analog-to-digital quantization noise. At the sensitivity level, the thermal noise is 7 dB greater than the quantization noise when measured in the 3-kHz information bandwidth.

The output signal-to-noise ratio (SNR) is better than 10 dB at an antenna signal level of –113 dBm. Digital automatic gain control (AGC) holds the output signal level at 20 dB below full scale (+4 dBm) until the RF AGC threshold is reached. The output SNR increases with the antenna signal level until the level at the ADC reaches 44 dB below full-scale (–20 dBm). At this point, the analog AGC holds the ADC input and output levels constant. The output SNR continues to rise to 54 dB until the analog-to-digital quantization noise dominates the receiver noise.

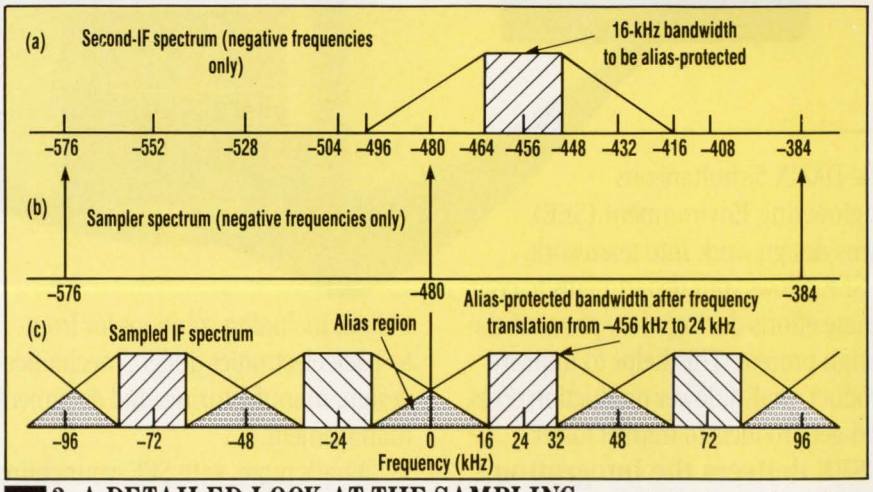
UNWANTED SIGNALS

Another consideration is the antenna overload level, which is the antenna signal level at which an undesired received signal can pass unattenuated through the 16-kHz bandwidth front-end to the ADC and saturate it. Because this undesired signal would be outside of the 3-kHz information bandwidth, it would not affect the normal AGC setting.

As a result, the receiver must maintain some "headroom" to accommodate signal-level peaks. Only desired in-band signals should be present after the final narrowband filtering in the digital-signal processor. Consequently, 20 dB of headroom is sufficient at the digital-signal-processor output. At the ADC input, however, large out-of-band undesired signals may be present. Consequently, at least 40 dB of headroom is required.

The maximum headroom is limited by the SNR required for both noise- or distortion-limited cases. In the example design, the maximum SNR for large desired signals, without interference, is 54 dB. If an out-of-band undesired signal at the ADC has a level of +4 dBm, or –20 dB from the saturation level, the converter will generate harmonic and intermodulation distortion products that will alias and potentially fall inside the desired signal bandwidth. If these products are specified to be 70 dB down (–66 dBm) and the in-band desired signal level at the ADC is –20 dBm, the ultimate signal-to-noise-and-distortion, S/(N+D), ratio will be limited to 46 dB (–20 dBm + 66 dBm).

The next step in the design is the digital IF processor architecture, which will depend on the desired level of functionality and the choice of hardware. In a typical implementation of a digital SSB processor, the digitized IF signal is first processed by the IF translator *(Fig. 4)*. The



3. A DETAILED LOOK AT THE SAMPLING process helps in specifying the first-IF filter. The 456-kHz second IF (a) and 96-kHz sampling frequency (b) are the determining factors. To protect the desired 16-kHz bandwidth from aliasing, the filter must have no more than an 80-kHz-wide stopband, or a 5-to-1 shape factor (c).

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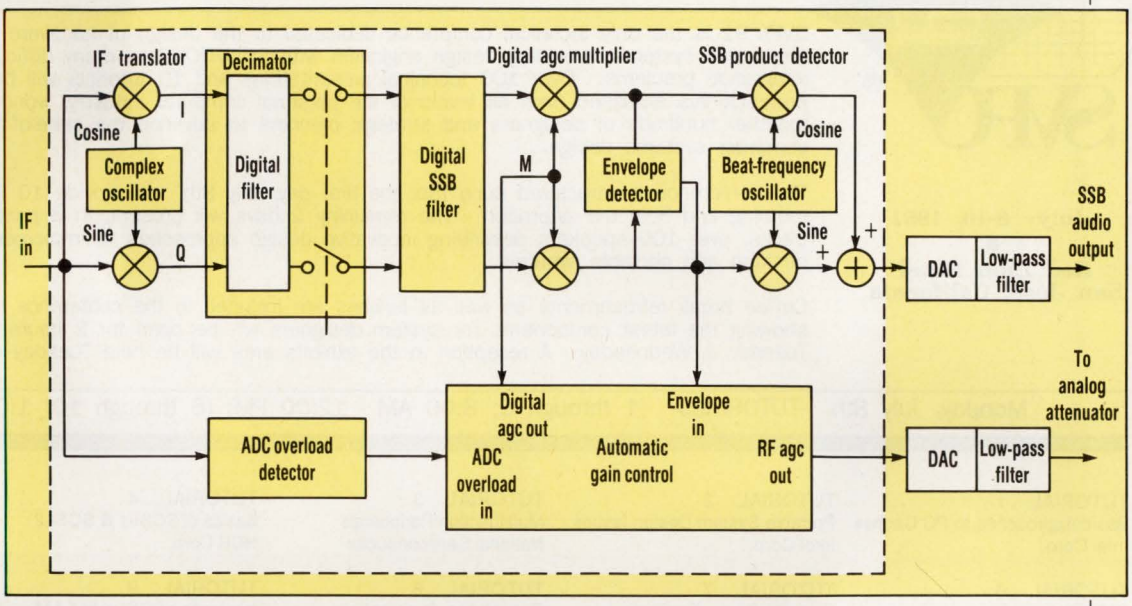
translator shifts the SSB channel's center frequency to dc, or zero frequency, and at the same time converts the "real" IF signal to a complex baseband signal. The resulting real and imaginary components are often referred to as the inphase (I) and quadrature (Q) components, respectively. This representation of the signal as a rotating vector or phasor is commonly used in digital-signal-processing algorithms.[1]



4. THE RADIO'S SSB FILTER, AGC, and demodulator are implemented by the digital-signal-processor chip. The system's sample rate is first reduced by a factor of 10 in the decimator to produce enough instruction cycles between samples to perform the required algorithms.

A complex oscillator and a multiplier perform the frequency translation and complex baseband conversion. Typically, the oscillator consists of a phase accumulator and sine and cosine algorithms *(Fig. 5)*. The phase accumulator is a modulo 2π adder that increments its output each sample period by adding a fixed constant, or phase increment, to its previous sample output. This process produces a continuously changing output phase angle ranging from 0 to 2π radians.

The algorithms then compute the phase angle's cosine and sine to generate the complex oscillator's real and imaginary outputs. Next, the real input signal is multiplied by the oscillator's outputs to produce the I and Q components of the complex baseband signal.

The next step is to implement the SSB filter, AGC, and demodulator in the digital-signal-processor chip. But the system's sample rate must be reduced as much as possible before the digital-signal processor can perform these computationally intensive algorithms. For example, if the DSP's instruction rate is 12 MHz and the sample rate remains at 96 kHz, only 125 instruction cycles will be available to run the algorithms on each point. This figure is insufficient. Therefore, the receiver decimates the sample rate by a factor of 10. The resulting 9600-Hz rate is enough to support the typical 3-kHz SSB bandwidth. It also enables 1250 instruction cycles between the decimated samples, enough to perform the required algorithms.

FILTER THE INPUT

Before the sample rate can be reduced, the input signal must be filtered to attenuate out-of-band signals. Otherwise, these signals can alias back in-band, causing distortion. This decimation filter usually consists of two identical finite-impulse-response (FIR) filters in the I and Q paths. Computer programs for designing FIR filters with arbitrary frequency response are readily available from many commercial sources. The most popular filter design algorithm, used in many of these programs, was distributed by the IEEE Press in 1979.[2]

After decimation, the signal passes through a high-performance receiver IF filter. This SSB filter is an FIR or infinite-impulse-response device. If necessary, the SSB filter's output level is adjusted by the digital portion of the AGC algorithm. The AGC controls the digital gain by multiplying the I and Q components by a positive scalar value, M *(Fig. 4, again)*.

The leveled I and Q outputs are then applied to the envelope detector and SSB product detector. The envelope detector computes the magnitude of the phasor represented by the I and Q components. The output envelope is simply the square root of the sum of the squared I and Q values. The AGC algorithm uses the envelope to adjust the receiver output level by a combination of analog (or RF) and digital gain control. To prevent saturation by strong out-of-band signals, the algorithm also senses any ADC overload and adjusts the RF and digital gain distributions accordingly.

The SSB product detector is a "half-complex" frequency translator that shifts the SSB carrier to its proper frequency. Just as in the IF translator, the circuit uses a complex oscillator, commonly called a beat-frequency oscillator. First, the I and Q signal values are multiplied by the cosine and sine outputs of the oscillator. Then the products are added to produce the receiver's audio output.

The hardware needed to implement the digital IF processor depends on several factors, but nearly

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The conference is structured such that the first day, July 8th, will provide 10 four-hour tutorials - 5 in the morning and 5 in the afternoon. The remaining 2 days will present, in 3 parallel technical session tracks, over 100 speakers describing innovative design approaches to implementing high performance desktop and portable systems.

Coffee break refreshments as well as lunches are included in the conference registration. Vendor exhibits showing the latest components for system designers will be open for 2 hours starting at noon on Tuesday & Wednesday. A reception in the exhibits area will be held Tuesday evening.

Monday, July 8th -TUTORIALS- (1 through 5; 8:00 AM - 12:00 PM) (6 through 10; 1:00 PM - 5:00 PM)

TUTORIAL 1 Basic Approaches to PC Caches Intel Corp.	TUTORIAL 2 Portable System Design Issues Intel Corp.	TUTORIAL 3 Multifunction Peripherals National Semiconductor	TUTORIAL 4 Basics of SCSI-1 & SCSI-2 NCR Corp.	TUTORIAL 5 Designing with High Speed PLD Intel Corp.
TUTORIAL 6 BIOS Design Award Software	TUTORIAL 7 Portable Power Technology Gates Energy Products	TUTORIAL 8 Data/Image compression Oak Technologies & Adv. Hardware Architectures	TUTORIAL 9 Integrating SCSI with CAM Ballard Synergy	TUTORIAL 10 Bringing Technology to Market Regis McKenna, Inc.

Tuesday, July 9th, 8:00 AM -OPENING KEYNOTE and TECHNICAL SESSIONS-
"Beyond the Single Chip PC" - Gordon Campbell, CEO, Chips & Technologies Inc.

TRACK I

- DISPLAY BASICS -
CRT Display Technology Directions; Advances in Video RAM Architectures; Advances in RAMDACs and Color Palettes; Where to Put Intelligence in Graphics.

- HIGH PERFORMANCE DISPLAY CONTROLLERS -
Understanding VGA Benchmarks; Implementing Advanced Features in VGA Systems; VRAM-Based Ultra-VGA Controllers; Bringing Workstation Graphics to PCs; Implementing 3D Graphics on a PC Add-in Card.

Above papers by: AT&T Microelectronics; Chips and Technologies; Information Associates; Inmos; NCR; Oak Technology; TI; Yamaha Systems Technology Div..

TRACK II

- MOTHERBOARD DESIGN ISSUES -
PC Chip Set Market Trends: Challenges and Opportunities; Designing High-Integration EISA Motherboards; Implement Compact EISA-Based Systems; A CPU-Speed-Independent Micro Channel Motherboard.

- BIOS AND SYSTEM PERFORMANCE ISSUES -
BIOS Architectural Support for New Chip Sets; Flash Memory: The Ideal BIOS Storage Device; Memory Subsystem Architectural Options; An Algorithm for Dynamic Memory Management; A New Enhanced-Mode DRAM for PC-based Workstations; Smaller, Faster, Cheaper, and Hotter: Thermal Problems and Cooling Solutions.

Above papers by: Intel; NMB; Opti; Phoenix; TI; Toshiba.

TRACK III

- BATTERY-POWERED SYSTEM ISSUES -
Designing Low Voltage Systems; Battery Technology: Current Status and Projections; Clock Synthesis for Laptops; Battery System Management.

- LAPTOP SYSTEM DESIGN APPROACHES -
ROM BIOS: The Best Place for Laptop Power Management; BIOS Modifications/Enhancements for Transparent Power Management for the i386SL; Power Management in Laptop Computers; Power Management in Portable Computers; Managing Power in Systems Based on the AM386DXL; Implementing High-Performance Laptops.

Above papers by: AMD; AT&T Microelectronics; Avasem; Benchmarq Microelectronics; Gates Energy Products; Intel; Phoenix; TI; VLSI Technology.

12:00 PM through 2:00 PM LUNCH AND EXHIBITS OPEN

- ACCELERATING GRAPHICS -
Accelerating 3D Graphics on a PC; Implement an Accelerated Windows Graphics Controller; Apply Multiple Processors to Accelerate GUIs; Accelerate GUIs With Smart Bus Control.

- MULTIMEDIA HARDWARE APPROACHES -
Adding Video to PC Graphics; Low-Cost Approaches to Video Compression; Integrating DSP into PC Systems; Developing Application Processors for Multimedia; Implementing Systems with DVI Technology.

Above papers by: Chips and Technologies; Intel; Inmos; Philips Components (Signetics); TI; Spectrum Signal Processing; Weitek.

- ADVANCED CACHE SUBSYSTEM DESIGN -
Choosing the Right Cache Architecture for PC Applications; 50-MHz Cache Solutions; Hardware-Level Concurrency in a 386/486 Write-Back Cache; Managing Cache Coherency; in Multiprocessing Systems.

- IMAGE AND VOICE I/O -
Apply Sampled-Data Storage for PC Analog I/O; Designing High-Speed Modems; Modular Modem Design - A Flexible Solution; Image Communications With PCs; Designing A Combination PC-Fax, Modem, and Voice-Mail Card.

Above papers by: AT&T Microelectronics; Chips and Technologies; Intel; Information Storage Devices; Mosel; National Semiconductor; Opti; TI; Yamaha Systems Technology Div.

- PORTABLE SYSTEM DESIGN ISSUES -
Designing a Two-Chip Notebook PC; Creating State-of-the-Art Notebook Computers; Building a Single-Board SPARC-based Laptop/Desktop Computer; Combining the EISA Bus and the M88000 RISC to Build Single-Board Systems; Memory Management Techniques for Laptops.

- 4:00 PM Panel Discussion -

Above papers by: Chips and Technologies; LSI Logic; Motorola; Oak Technology; VLSI Technology.

5:00 PM EXHIBITOR RECEPTION/EXHIBITS OPEN

Technical Sessions continued on next page

Sponsored by SysTech Research in cooperation with Electronic Design (a Penton publication), Intel Corp., NCR Corp., NMB Technologies, and Yamaha Systems Technology Div.

Wednesday, July 10th, 8:00 AM -OPENING KEYNOTE and TECHNICAL SESSIONS-
"The 10 PCs You'll Never See" - Mike Aymar, VP & General Manager, Microcomputer Div., Intel Corp.

TRACK I

- FLAT PANEL BASICS -
Flat Panel Design Options; Flat Panel Displays for Portable Systems; CGA Graphics for Handheld/Low-end Portables; Controlling Full-Color VGA Flat Panels.

- DEALING WITH GUIs -
A High-Speed Video Digitizer for the Apple Macintosh; System Software Needs of the new Operating Environments: OS/2 and Windows; Designing a CAD Toolkit to Run Under Windows; Developing FAX Communication Interfaces Under Windows; Creating Multifunction User Interfaces; Controlling Instruments Through Windows.

Above papers by: Chips and Technologies; Gebala Systems; Information Associates; QuickLogic; Logical Services; National Semiconductor; Phoenix Technologies; Stanford Resources.

TRACK II

- EXPANSION-BUS ISSUES -
EISA Add-on Card Design - Shaking the AT Mentality; System Design Issues for Intelligent EISA/MCA Cards; A RISC-based I/O Processor for PC Architectures; Increasing I/O Performance in PC Architectures; An Extended Local Bus Architecture for Better System Performance.

- HIGH-PERFORMANCE SYSTEM ISSUES -
Clock Distribution for High-Performance PCs; Care and Breeding of High-Speed Clocks; Applying System-Level Simulation When Designing ASIC Based PC Systems; Streamlining High-Speed System Design With Transmission Line Analysis; Computer-Aided Prototyping For Concurrent PC System Design.

Above papers by: Bull-Micral; Chips and Technologies; EliteGroup Computer Systems; Intel; Quantic Laboratories; QuickTurn Systems; Silicon Systems; Texas Instruments; VLSI Technology.

TRACK III

- NETWORKING -
Putting FDDI on a PC-AT Half-Card For Single Attachment Stations; Interface Ethernet to the EISA Bus; Customizing a LAN Controller For a Single-Chip Solution; Direct Bus Mastering in PCs Improves LAN Performance; Take Advantage of Specialty Memories When Building LAN Interfaces.

- DATA COMMUNICATIONS AND MASS STORAGE -
Employ Serial Packet Controllers for Flexible Protocol Control; Designing Appletalk-Compatible Serial Interfaces; Large Capacity Back-up Systems for Networked PCs/Workstations; Magnetic and Optical Drive Technology: Current Status and Future Directions; Flash Memory: The Optimal Technology for Solid-State Disks; SCSI RAID Subsystems for Redundant, High-Performance Mass Storage.

Above papers by: AMD; Intel; Integrated Device Technology; Maxtor; NCR; Plus Logic; PureData Research/USA; R-Byte; Silicon Systems; Zilog.

12:00 PM through 2:00 PM LUNCH AND EXHIBITS OPEN

- DISPLAY SUBSYSTEM DESIGN -
Local Bus Support for Video Systems; Selecting the Right Bus Interface for Video; Get High-Performance Graphics with Reprogrammable Logic; Developing Low-Cost Bus and Video Timing Control for Apple Macintoshes.

- I/O DEVICE DESIGN -
Reconfigurable Monitor Design Considerations; Designing High-Speed Control Logic With Reprogrammable Logic; Low-Cost Closed-Loop Controllers For Better Printer Accuracy; Designing Custom Keyboards and Interfaces; Evaluating and Testing Keyboards for PC Compatibility.

Above papers by: Cirrus Logic; Highgate Design; Hewlett Packard; HTE/HiTech Equipment; Oak Technologies; Micron Technology; NMB Technologies; Radius and Xilinx.

- APPLYING PROGRAMMABLE LOGIC -
Design Flexible Micro Channel Interfaces with Programmable Logic; Consolidating System Logic With PLDs; High-Density PLDs Simplify System Design; Apply FPGAs To Simplify Add-in Card Logic.

- EMBEDDED PCs FOR REAL-TIME SYSTEMS -
Real-Time Operating Systems for High-Performance Desktop PCs; Turning the PC into a Real-Time Machine; Using the PC/AT Architecture in Embedded Systems; Designing A Real-Time I/O Controller Card for the PC; Linking the Macintosh and VME environments for Real-Time Applications.

Above papers by: Actel; Altera; Ampro Computers; Intel; Lattice Semiconductor; Lynx Real Time Systems; Ready Systems; Nauchny Center, Moscow, USSR; YARC Systems Corp.

Technical Program subject to change

- MASS-STORAGE CONTROL -
SCSI Host Adapter Performance Trends - Using Intelligent OS Caches; Designing an Optimized SCSI Host Solution; Designing RISC-based Caching SCSI Disk Controllers; Tuning Storage Subsystem Drivers for Multi-Threaded Operating Systems.

- MASS STORAGE -
Optimization of I/O Subsystems in an EISA-Based File Server; Write Caching - New Drive Caching Schemes for Higher Performance; Applying the Power-Saving Modes Embedded in Low-Power IDE Disk Drives; System Compatibility Software Design for PCMCIA/JEIDA Memory Card Applications; PCMCIA System Interface Overview for Memory Cards.

Above papers by: Adaptec; Chips and Technologies; Databook; Intel; Interphase; Maxtor; Quantum; Storage Dimensions; VLSI Technology.

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FOR EXHIBIT INFORMATION CONTACT: Ken Majithia, General Chairman SVPC'91 Voice: 408/924-3930, FAX: 408/997-8265, Email:majithia @calstate.bitnet

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Tuesday, Wednesday, July 9, July 10, 1991 **(All Technical Sessions, No Tutorials)** (Includes Conference Proceedings, Coffee Break Refreshments, Lunches, Exhibits and Reception admission)	$345	$400	$_____
Three Day Package: Monday - Wednesday, July 8-10 **(Two Tutorials & All Technical Sessions) Circle One PM & One AM: (1) (2) (3) (4) (5) PM: (6) (7) (8) (9) (10).** (Includes all materials of both Short Course and Technical Sessions as described above)	$395	$450	$_____
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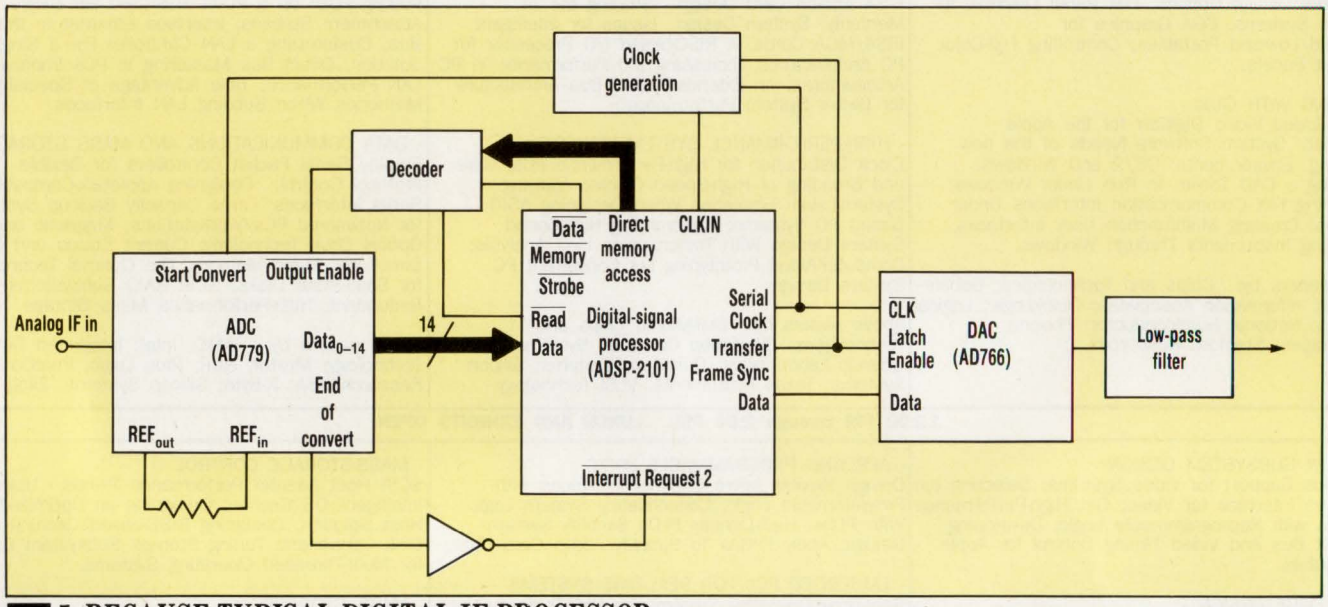

5. BECAUSE TYPICAL DIGITAL IF PROCESSOR architectures are highly integrated, most functions can be implemented in the DSP software. In this example circuit, only a few ICs are needed to perform the functions, as described in Figure 4.

all systems will include certain common components *(Fig. 6)*. The total number of ICs can be minimal, keeping overall system cost low.

Modern communication receivers would typically use a high-performance digital-signal processor, such as the ADSP-2101. This processor is well-suited to many of the operations of a digital receiver and can easily link to the 14-bit parallel output of the AD779. Conversion back to the analog domain is simplified by digital-to-analog converters (DACs), like the AD766. These low-cost, 16-bit, serial-input DACs require no additional glue logic or interface circuitry, have an on-board reference, and are completely tested and specified over temperature.

Additional circuitry performs decoding, clock generation, and output filtering. The decoder handles handshaking between the AD779 and the digital-signal processor. Depending on the number of peripherals connected to the processor, the decoder may be as simple as a few logic gates. Clock signals are typically generated by a high-stability crystal with low phase noise. The crystal can serve as the processor's master clock and can also be divided by counters or other means to generate the ADC and DAC sampling clocks.

On the falling edge of the sampling clock ($\overline{SC}$), the AD779 digitizes the incoming IF signal *(Fig. 6, again)*. Approximately 8 μs later, the conversion is complete and the AD779 asserts End of Convert (EOC). The falling edge of the inverted EOC signal interrupts the digital-signal processor. The control and address lines from the processor are decoded to generate the Output Enable ($\overline{OE}$) pulse for the ADC. The ADC then places the digitized output on the data bus to be read by the processor.

The ADSP-2101 offers several features tailored to communications systems. The ability to fetch two operands (typically a coefficient and a data point), multiply these operands, and then sum the results with previous products in one processor cycle makes FIR filter algorithms extremely efficient. And an internal 40-bit accumulator enables full-precision products to be calculated without round-off noise caused by truncation in the filter computations. Interprocessor communication between multiple DSPs, which is often needed in SSB equipment, is easily implemented with one of the processor's two integrated serial ports.

The digital IF processor's high integration level is indicative of the future of SSB equipment. As the performance of the ADC improves, it will be placed closer to the receiving antenna in the analog front-end. The ultimate goal is to digitize the incoming RF signal directly from the antenna and implement the remaining digital functions in custom ASICs.□

References:

[1] W.E. Sabin and E.O. Schoenike, *Single-sideband systems & circuits*, (McGraw-Hill Book Co., 1987).

[2] J.H. McClellan, T.W. Parks, and L.R. Rabiner; DSP Committee of the IEEE Acoustics, Speech, and Signal Processing Society, *Programs for digital signal processing*, (IEEE Press, 1979), Chap. 5.

Richard A. Groshong, senior design engineer at Rockwell Collins Defense Communications, received a BSEE from the University of Minnesota.

Stephen Ruscak, marketing and applications engineer for Analog Devices Semiconductor, holds a BSEE from Northeastern University, Boston, Mass.

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WHEN DIGITAL SYSTEMS NEED VARIABLE DELAYS, COMMERCIAL DEVICES, HOME-BREW CIRCUITS, OR SEMICUSTOM LSI DESIGNS CAN DO THE JOB.

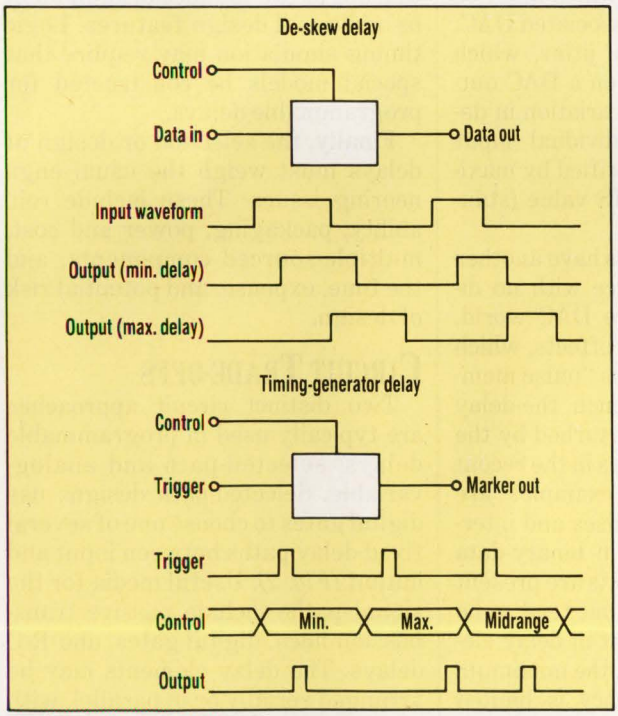
A STEP-BY-STEP GUIDE TO PROGRAMMABLE DELAYS

As programmable time-delay elements become more common in digital systems, designers can satisfy a vast range of application requirements by choosing among several distinct circuit approaches. Each approach, however, comes with its own set of advantages and disadvantages. There's also another point to consider. Even though a wide variety of off-the-shelf components is dedicated to these functions, system requirements can often be met very economically with an application-specific design at the board or IC level. This article presents a brief review of the relevant issues and options.

The term "programmable delay" will be used to mean a digital element whose output transitions follow transitions on a signal input, after a propagation delay that depends on one or more control inputs. Counter and pipeline-type circuits, which make delays in discrete multiples of a clock or reference period, will be skipped.

Most applications for programmable delays may be classified in one of two groups: de-skew and timing generation *(Fig. 1)*. De-skews are programmed to cancel or compensate for the variation of other system components. They're useful in clock distribution, high-speed buses, time-domain instruments and test equipment, and interfaces to data transmission or storage media. They generally have output waveforms similar to the input: both rising and falling edges are propagated, sometimes with independently variable delay.

Timing-generator applications use the delay to initiate events at arbitrary programmable times. They include sampling and marker-pulse generators, test-equipment stimulus and response generators, and other instruments. Often, only one transition polarity is significant. In such cases, the delay is triggered by an edge or pulse, and makes an output edge or fixed-width pulse after the programmed time inter-



1. TWO COMMON uses for programmable delays are de-skew and timing generation. One makes up for variation in other components; the other initiates events at arbitrary times.

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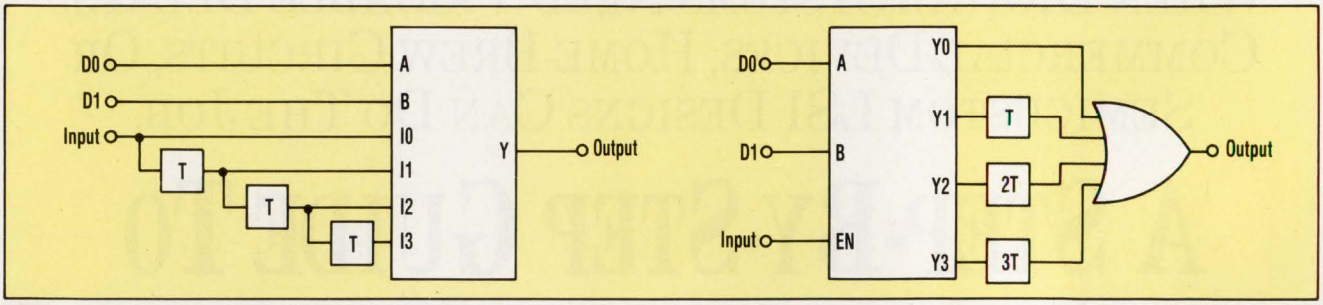
AMCC, 6195 Lusk Blvd., San Diego, CA 92121; (619) 535-6834.

PROGRAMMABLE DELAYS



2. SEVERAL CONFIGURATIONS are possible when delay is controlled by selecting discrete signal paths. Shown are a serial delay arrangement with downstream selection and a parallel arrangement with upstream selection.

val. Some timing generators need dynamic control, which can apply an independent delay setting to each trigger event.

Before discussing circuit implementations, let's review the specification variables of a programmable delay. The primary timing parameters of the signal path are its insertion delay (minimum propagation time) and its programmable range and resolution. Also important are the minimum pulse width and repetition rate of the input signal. If the maximum delay exceeds the minimum interval between inputs, it means the delay element must handle two or more consecutive events concurrently.

The control input may be a digital word or an analog level. When the delay mechanism is intrinsically analog, its programmable level is typically generated by a digital-to-analog converter (DAC), which is often included in the variable-delay block. But a direct analog interface allows several options, such as an economical external DAC, tracking delays with a common control level, many sample-and-holds refreshed independently by one DAC, or delay regulation by analog feedback. The latter is a straightforward variation of the traditional phase-locked loop.

If the control input is dynamic, its setup and hold times with respect to the trigger are specified. Static controls may need a designated settling time to reach a given delay accuracy. In either case, beware that many circuits have an anomalous response if an input arrives very close to a control transition.

The timing-accuracy specification of a programmable-delay circuit begins with a set of terms analogous to those of a DAC, with similar nomenclature. There are the tolerance and stability of insertion delay and full-scale range (which may be adjustable in some implementations), and integral and differential nonlinearity and monotonicity (which typically aren't adjustable). If the delay control interface is analog, there will be nonlinearity in its voltage- or current-to-time transfer which must be added to that of the associated DAC. Finally, there's delay jitter, which corresponds to noise on a DAC output. It's the random variation in delay for different individual input edges, and can be specified by maximum error or by RMS value (standard deviation).

Time-delay elements have another important error source with no direct equivalent in the DAC world. This source is history effects, which are often referred to as "pulse memory." In this phenomenon, the delay of a signal edge is perturbed by the presence of other edges in the recent past. Two common examples are shrinkage of short pulses and intersymbol interference in binary-data streams. History effects are present in all digital circuits, but tend to be particularly significant in delay elements. In many cases, the maximum usable signal frequency is limited not by the delay's functional failure, but rather by accuracy degradation. One way to specify pulse memory is the worst-case delay change from a standard condition over a stated range of input timing.

Input history is usually insignificant when edges are separated by more than a few times the full-scale delay, but critical applications may need to consider effects with time constants in the millisecond-to-second range. These include thermal and other conditions that depend on signal duty cycle, and dielectric absorption in timing capacitors.

Component and system testability deserve particular attention when programmable delays are used. Verifying the control function in production might call for special equipment or additional design features. Logic timing simulation may require that special models be constructed for programmable delays.

Finally, the selection or design of delays must weigh the usual engineering issues. These include reliability, packaging, power and cost, multiple-sourced components, and the time, expense, and potential risk of design.

CIRCUIT TRADE-OFFS

Two distinct circuit approaches are typically used in programmable delays: selected-path and analog-variable. Selected-path designs use digital gates to choose one of several fixed-delay paths between input and output *(Fig. 2)*. Useful media for the signal paths include passive transmission lines, digital gates, and R-C delays. The delay elements may be arranged serially or in parallel, with selection logic upstream or downstream.

In analog delays, the physical path of the signal remains constant, but its propagation time depends on a variable control level. The ramp-and-comparator approach is popular because of its flexibility and naturally

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PROGRAMMABLE DELAYS

linear response *(Fig. 3)*. Here, a transition of the input signal makes a voltage ramp start from a stable initial level. The ramp and a control voltage are applied to the inputs of a high-speed comparator, which switches at a time proportional to the control level.

Other methods which have been used for analog delays achieve control with variable charging current or junction capacitance, but these tend to have nonlinear transfer functions. An interesting exception varies the path delay directly in discrete steps by electronically connecting different fixed capacitors to the timing node.

Selected-path delays are good for de-skews because they propagate both edge polarities, although typically without independent control. With an appropriate medium, the total delay can be substantially greater than the signal period. Dynamic control is simple, but asynchronous path switching can cause an input pulse to be lost, truncated, or replicated. The number of delay choices per stage is usually limited to between 2 and 16, limited by selector-logic fan-in/fan-out and physical packaging. In most cases, the delay times are fixed by design. Unless individual adjustments can be made in production, absolute resolution and accuracy are limited by the matching of paths in the selector logic.

Analog-variable delays can provide single-stage resolution that's limited only by the associated DAC. Such delays remain monotonic even when the absolute step size is extremely small. The delay element itself can be very compact and efficient, but the DAC's area and power may be substantial. This type of circuit is common in timing-generator applications with only one significant edge polarity. In dual-polarity (data de-skew) applications, the delay variation of rising and falling edges tends to be opposite in sign. This can be used for pulse-width or duty-cycle control. Full-scale delay is easy to adjust, but is limited to somewhat less than the input period. That's because the circuit can handle only one edge at a time.

Programmable delays can be combined in various ways to extend range and/or resolution and solve other specific problems. For example, a de-skew application may use a selected-path section in series with two analog stages. The combination may have a wide range with fine-resolution control of rising and falling edges.

When timing accuracy and cost are important, many systems include self-calibration paths, a measurement unit, and sometimes programmable trimming circuits. Range and offset errors can then be tuned out automatically or simply compensated for in software. For example, non-monotonic multistage delays can be linearized by exhaustive calibration and a software or hardware lookup table.

COMMERCIAL DELAYS

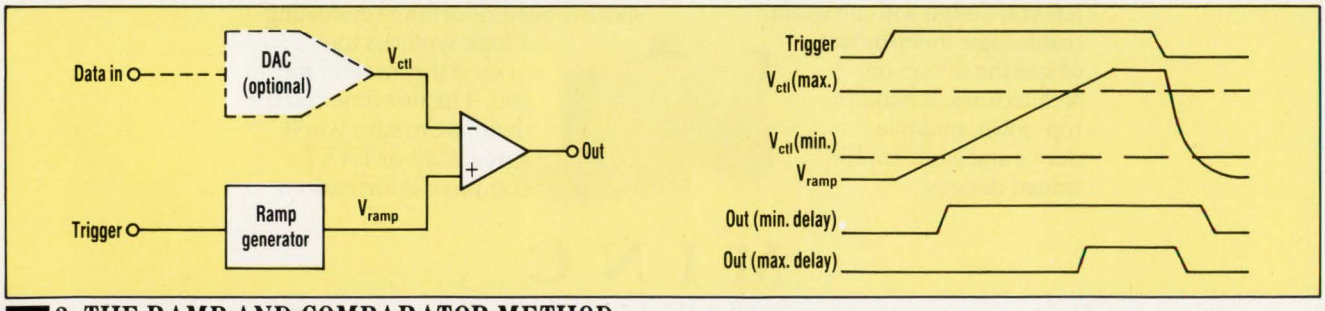
Both types of programmable-delay circuits (selected-path and analog-variable) are available in packages that connect directly to standard logic families. An important caveat is that control-input timing and pulse-memory specifications are often not stated on data sheets. Timing accuracy may be specified for low-frequency periodic inputs, while at the specified maximum signal frequency, only functional operation is guaranteed. When in doubt, users should consult the manufacturer and/or characterize representative components.

Selected-path modules based on uniformly tapped delay lines with an input buffer, a terminator, and a data selector/output buffer are available in a variety of options from several manufacturers, including Elmec Technology of America, Monterey Park, Calif., Engineered Components Co., San Luis Obispo, Calif., and Rhombus Industries, Huntington Beach, Calif. Many versions can handle input periods that are well under half the full-scale delay. TTL and ECL versions are available in configurations ranging from 3- to 8-bit binary and 2-digit BCD, full-scale delays to over 1 μs, and resolutions down to 50 ps.

Gate-chain programmable delays are available in at least two advanced-ECL product lines. The SPECL family from Sony Corp. of America, Cypress, Calif., includes the CXB1139Q delay line/duty-cycle controller. A chain of 2 to 40 gates gives 23 delay choices between 0.8 and 4.7 ns. Timing resolution (piecewise-linear) is 125 ps to 190 ps.

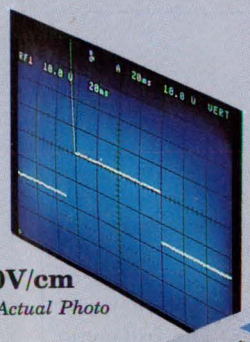
From Motorola, Phoenix, Ariz., comes the ECLIPS Series 10E195/100E195 delay. This device uses seven binary-weighted stages for 2.24-ns range with 17.5-ps resolution, and can propagate a 1-GHz signal. It has latched control inputs and a special cascading feature. The 10E196/100E196 delay adds an analog stage for fine adjustment.

Monolithic ramp-and-comparator



3. THE RAMP-AND-COMPARATOR METHOD gives an analog delay with a linear relationship between voltage and time. A transition on the trigger initiates a voltage ramp. The comparator output switches when the ramp crosses the control level.

Power Surges...



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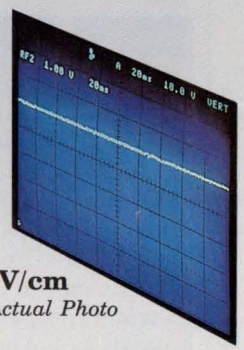

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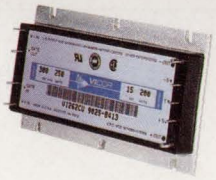

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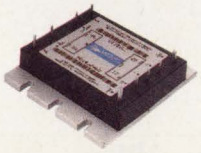

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PROGRAMMABLE DELAYS

delays are now available in several configurations. The AD9500 and AD9501 from Analog Devices of Norwood, Mass., and San Diego, Calif.-based Brooktree's BT604, BT605, and BT606 each include an 8-bit DAC and control data latch. They're triggered by a rising edge and drive their output high after the programmed interval. The devices can be retriggered after an automatic or externally controlled reset signal and a finite recovery period. Full-scale delay is set by an external resistor or current source and/or capacitor to between 2.5 ns (10-ps resolution) and 100 μs. Options include differential ECL or TTL levels. One device uses the trigger signal to latch the control data word for dynamic delay control at up to 125 MHz.

Ramp-and-comparator delays are used differently in the Brooktree Bt622 and Bt624 chips. These are dual and quad channel de-skews with analog-voltage inputs to control overall delay and skew between rising and falling edges. The full-scale range is fixed by design, and there are delay options of 10 ns, 20 ns, and 40 ns.

DESIGNING DELAYS

Often, an application-specific design is necessary or more appropri-

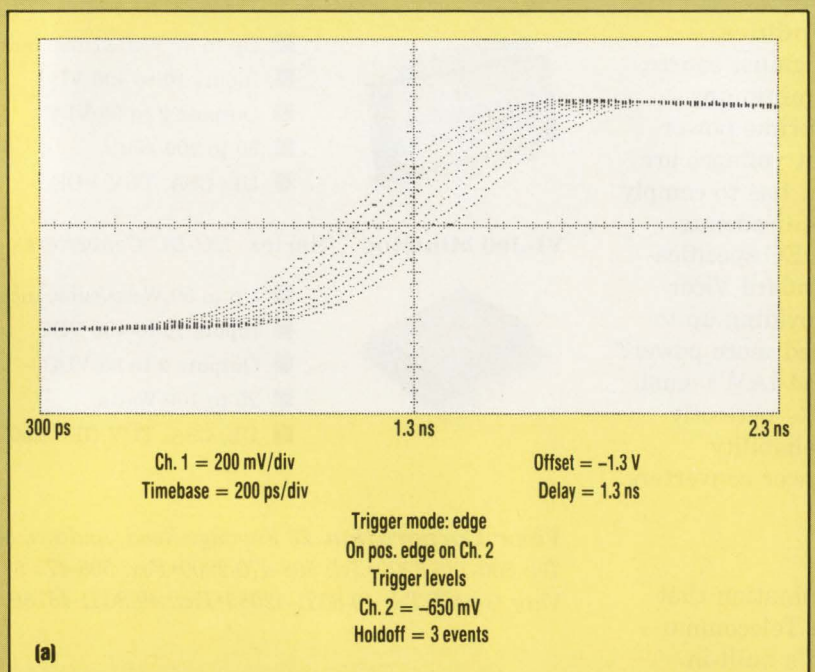
A CUSTOM-GATE-ARRAY DELAY DESIGN

A high-resolution variable-delay function has been implemented as a custom macro on an AMCC Q1300T bipolar digital gate array. The circuit is triggered by falling edges, and generates rising edges at its output after a digitally controlled propagation delay. Its full-scale range is about 320 ps, equivalent to the typical delay of a fast-option gate in this process. Three-bit control makes the timing resolution better than 50 ps *(Fig. A)*. Trigger edges as close as 7 ns can have independent delay settings. The design had to be compact because the array is densely populated by other circuit functions.

The chosen implementation is based on the analog method, using a fast digital-to-analog converter (DAC), ramp generator, and voltage comparator. It occupies four I/O cells and one logic cell. A simplified schematic diagram of the circuit is shown *(Fig. B)*. The delay control code is converted by the DAC to one of eight analog levels. The converter's output is routed to one input of a fast comparator. The remaining comparator input is driven by the output of a ramp generator, which is activated by the trigger input.

As the ramp generator's output voltage changes, the comparator switches state when the ramp voltage passes the voltage at the DAC's output. In this implementation, the trigger input must remain active until after the output pulse has gone high and stayed high for a given period of time. Once the trigger input returns to its initial state, the ramp generator is reset, and the output pulse returns to zero. If required, the vernier can be made edge-sensitive by having the trigger input clock a flip-flop which, in turn, enables the ramp generator. The flip-flop is then reset by the delayed output and can be retriggered.

Several important considerations had to be made to ensure a successful design. The prime concern was the linearity of the delay time with respect to the digital control input. The two main contributors to delay nonlinearity are ramp nonlinearity and DAC nonlinearity. For the ramp generator, the output of a degenerated current source is integrated as the voltage on a capacitor. This method calls for a capacitor with an extremely low voltage coefficient. The need for a high ramp rate (in the range of a volt per nanosecond) made an external capacitor impractical. That's because the presence of parasitic capacitance would mean using an extremely high integration current. In addition, parasitic package inductance would make it hard to achieve a



A. IN THIS DIGITAL GATE ARRAY, a custom macro uses an analog method to get eight time choices within the span of one logic delay.

PROGRAMMABLE DELAYS

ate than a standard component. Programmable delays aren't particularly hard to design. First, the general design issues and pitfalls will be reviewed, then the special constraints of VLSI applications will be considered.

In selected-path stages, the delay medium is used most efficiently in a serial configuration. A parallel configuration, however, can give finer resolution and may have fewer error-contributing components in its long paths. Control data must be stable and valid at the selector logic when any signal edge arrives. Therefore, its timing depends on the gate setup and hold time, the input-signal pulse width, and, if selection is downstream, the full-scale delay. The set-up-and-hold-time performance of the combinatorial-logic elements are often unspecified and may need to be determined by simulation, experiment, or analysis of other ac characteristics. Accuracy and pulse-memory performance are typically limited by the delay-path medium.

Passive delay lines are useful in selected-path designs at the printed-circuit and hybrid levels. Their tolerance and stability are good but hard to adjust in production. They can provide a symmetric response to rising and falling edges, and a total delay much greater than the input inter-

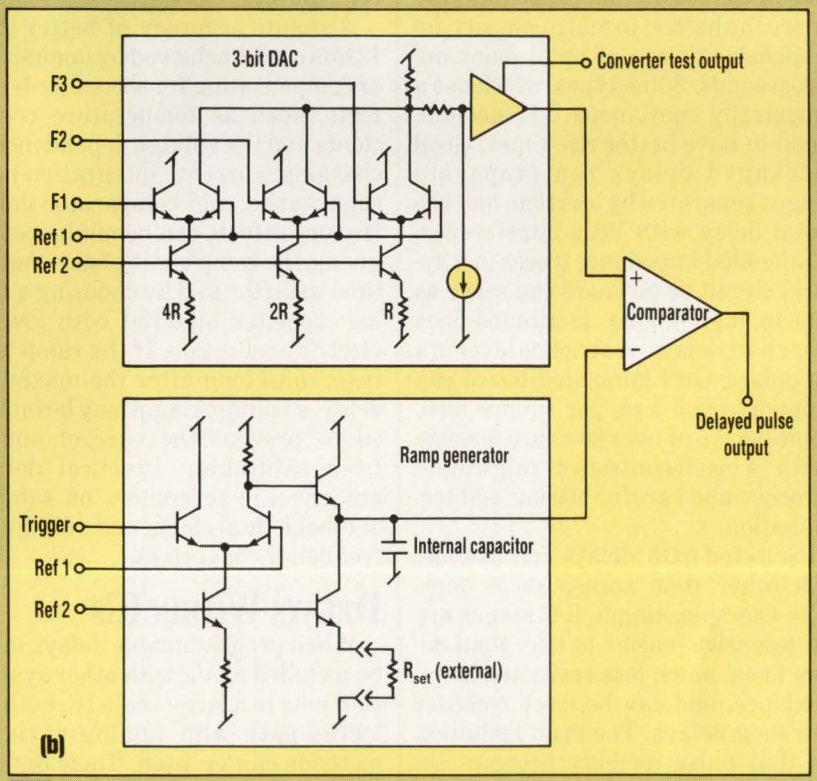
well-settled, linear ramp at these rates. As a result, it was decided to use an on-chip capacitor.

Of the available techniques for generating an on-chip capacitor on the AMCC bipolar process, only a metal-oxide-metal configuration would provide the required voltage linearity. Care must also be taken to set the DAC-output levels so that only the center portion of the ramp is used to generate delays. This sidesteps nonlinearities that occur when the ramp initially starts up and when it reaches its final level. To do so, the converter's offset voltage and full-scale output range must be chosen appropriately.

For external adjustment of the delay span, the ramp current is set with an external resistor in the emitter of the ramp-current source transistor. The voltage at the base of the current-source transistor is set by a bandgap reference that's designed so that the emitter voltage of the current source has a very low temperature coefficient with respect to the negative supply. In this way, if a resistor with a low temperature coefficient is used to set the current, then the overall delay span will display good temperature stability.

DAC linearity is determined mainly by the on-chip resistor and V_{be} matching. If resistor and transistor sizes are carefully chosen, the process itself is capable of better than nine bits of linearity. On a digital gate array, however, one must live with the assortment of devices that have been pre-placed in the base cells. Even within these constraints, it's relatively easy to construct a 3-bit DAC with enough accuracy to virtually avoid any contribution to nonlinearity.

One final consideration involved testability. The timing vernier generates edge delays to a resolution of 50 ps. Because measuring timing to this resolution is very difficult in a production test environment, an indirect method of testing was called for. The solution was to provide a second output from the DAC to a pin on the chip. This offers verification of the timing vernier's functionality by making only dc parametric measurements on the converter's output. Because the converter's linearity and step size can be directly related to the timing resolution, it can provide a method for rejecting parts that may not meet specifications without testing them at full speed.



B. A 3-BIT DAC sums binary-weighted current sources, and is almost as fast as a regular gate. An emitter-follower charges the ramp capacitor quickly, but cuts off early in the negative transition.

PROGRAMMABLE DELAYS

val. The selector-logic family must drive the line impedance, and the loading effect of its inputs on the line delay must be small and predictable. ECL is excellent here. In fact, ECL-system-design handbooks are a good place to find a practical introduction to transmission lines in digital systems.

The useful resolution of selected passive lines is limited to about 50 ps by mismatches in logic delay and loading capacitance. At this scale, the load capacitance may be substantially greater than the line capacitance. If the series resistance of the line is more than a couple of ohms, it may cause objectionable logic-level shifts. The shifts can be controlled, however, by changing the termination voltage and adding a bias-current source at the driver if necessary.

To propagate short and closely-spaced input pulses with minimum memory, a delay line must have a short rise time and accurate termination. Many packaged lines use a ladder of inductors and capacitors (the more the better) to make compact, inexpensive delays of up to many microseconds. Some types, which use a physically continuous L-C medium, tend to have better rise times. Good packaged delays can propagate edges separated by less than half the total delay with little interference. Controlled-impedance traces in a hybrid circuit or pc board can serve as cheap, high-quality distributed lines for short delays. A stripline layer in a standard G-10 laminated board can support over 5 ns per square inch. Line delays of over 20 ns are feasible with a well-controlled fabrication process and careful biasing and termination.

Selected-path delays can use media other than transmission lines. For example, simple R-C stages are inexpensive, easier to trim than delay lines, much less restricted in impedance, and can be more compact for long delays. The main limitation is that pulse memory becomes severe if the delay is more than a small fraction of the input period. This effect is reduced if long delays are made from several shorter ones isolated by buffer gates, but overall tolerance and stability are compromised. Selector-logic skew still limits the minimum absolute timing resolution, but this can sometimes be compensated for by tuning. Parallel, selectable R-C delays adjusted at the factory have been used to make stable delay steps of 50 ps.

Analog delay circuits are recommended for applications that require high resolution, precise linearity, or a tunable range. The ramp-and-comparator approach will be reviewed to illustrate its flexibility and naturally linear control characteristic.

The difficulty of design depends mostly on the linearity requirement. Almost any smooth ramp waveform can make a system's differential linearity comparable to that of the controlling DAC. Sometimes an ordinary logic signal with its finite rise time can do the job. But when integral linearity and range stability are important, it's better to generate the ramp by charging or discharging a fixed capacitor with a constant-current source.

Absolute accuracy of better than 12 bits can be achieved by minimizing or compensating for second-order effects, such as temperature coefficients and the voltage dependence of charging current, integration-node capacitance, and comparator delay. History effects can be minimized by giving the ramp-reset phase enough time to settle, and by choosing a timing-capacitor material with low dielectric absorption. If the ramp isn't reset until long after the maximum delay, a voltage clamp may be included to prevent the current source from saturating. Practical details are given in references on sample-and-hold, dual-slope, and voltage-to-frequency converters.

DELAYS WITHIN ICS

When programmable delays must be included along with other system elements in a large-scale IC, both selected-path and analog-variable methods can be used. Their options and constraints depend on the IC process, logic type, and design level (full-custom, standard-cell, or mask- or field-programmable gate array).

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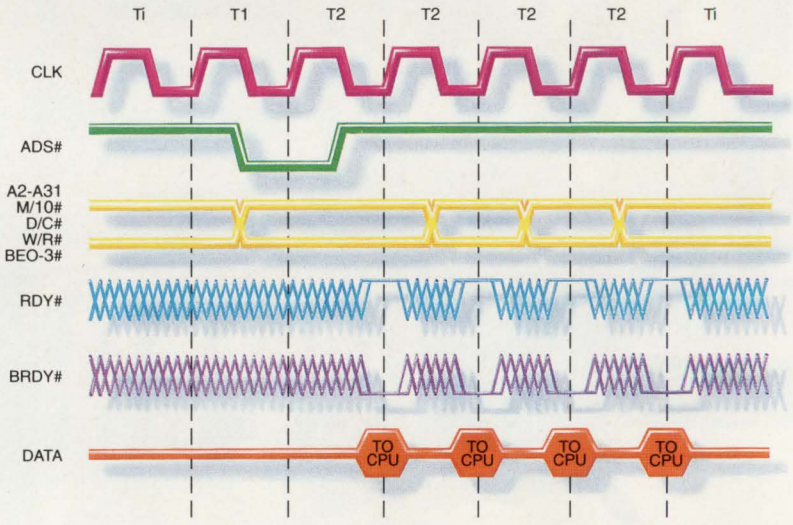

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PROGRAMMABLE DELAYS

Selected-path delays are easily integrated and can use any of the topologies reviewed above. Logic gates are an obvious and almost universally available delay medium. Very long chains are feasible, although in de-skew applications they should use inverting gates to balance the propagation time of rising and falling edges. Delay per unit area can be increased if the design level enables construction of extra-slow gates or delay cells.

An important consideration, especially for long delays, is the sensitivity of gate delays to process variation, temperature, and supply voltage. Published specifications are typically very conservative. Designs that take such specs into account are generally reliable, but often require substantially more gates or selectable paths than designs based on nominal delays. There are several ways to improve stability if transistor-level design is available and a substantial engineering cost is acceptable. Demonstrated methods include on-chip voltage and temperature regulation, gate circuits optimized for delay insensitivity, tuning in production, and active delay regulation. The last two rely on matched-delay gates that depend on a common variable. A feedback circuit can make the delay of a reference chain match an external time signal.

The ability to handle very short or closely spaced pulses without interaction between edges depends greatly on the process and logic type. A figure of merit is the ratio between the propagation delay of a logic transition and the time for the circuit to reach equilibrium. Care should be taken when using circuit simulators to predict the magnitude of pulse memory. The device models associated with a digital process are often tuned to correlate with observed propagation delays, and could still have significant errors in predicting the transition "tails" that cause pulse memory.

Timing resolution of less than a gate delay is available on the chip by selecting from parallel paths that differ only in load capacitance. The flexibility of this approach depends on the design level. Incremental loads can be gate inputs, various types of transistor junctions, or simply extra interconnect wire. The matching of paths in the selector logic is critical, but monotonic programmable steps of well under 10 ps have been made in a bipolar Si process.

Analog-variable programmable delays can also be included in large-scale digital ICs. They may offer improved range or accuracy while using less area and power than selected-path delays. Another benefit is ease of trimming the delay range to compensate for process and environmental variation. The analog option is not restricted to full-custom circuits. Ramp generators, comparators, and DACs linear to a few percent can be made in metal-mask-level designs from the same transistor and resistor set as standard logic gates.

For example, an integrated analog delay is used by Megatest Corp. in the timing generators of its Polaris VLSI tester *(see "A custom-gate-array delay design," p. 102)*. A dynamically controlled vernier (fine-resolution) delay function is included in an ECL gate array. The custom macro implementation of a ramp, DAC, and comparator stage occupies an area similar to that of a couple of fancy flip-flops. It covers a range of about one gate delay with 3-bit resolution. The gate-array approach was chosen for high performance, low cost (large systems have over a thousand of these delay elements), and a short and reliable design cycle.□

Richard Feldman manages development of timing and calibration systems at Megatest's Logic Product Group. He holds a BS in engineering and applied science and an MSEE from the California Institute of Technology, Pasadena.

David Rosky, principal design engineer at AMCC, received a BSEE and MSEE from the University of California at Los Angeles.

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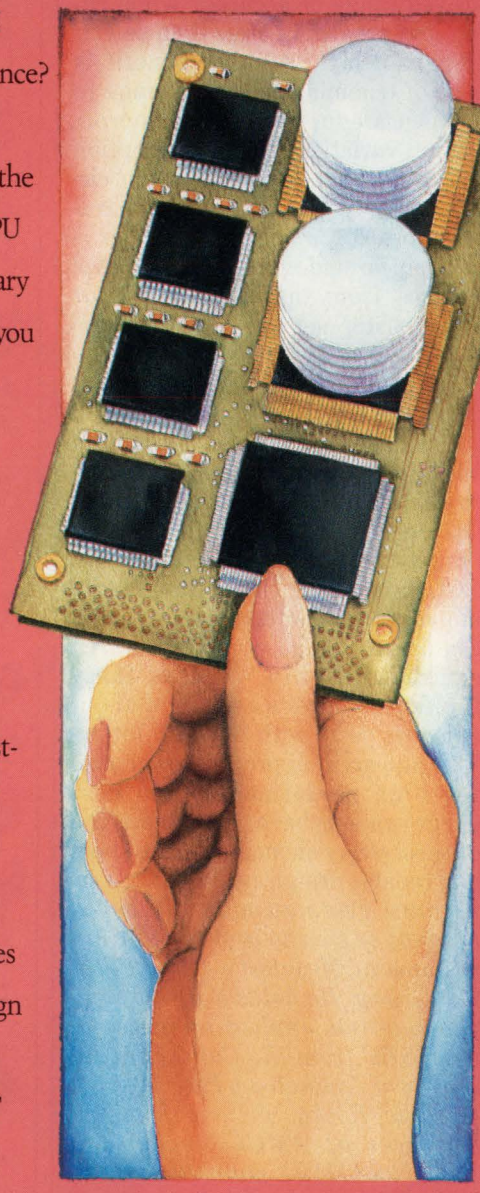

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CIRCLE 521 15-V Supply Is Isolated To 2500 V

SAM OCHI
IXYS Corp., 2255 Zanker Rd., San Jose, CA 95131; (408) 435-1900.

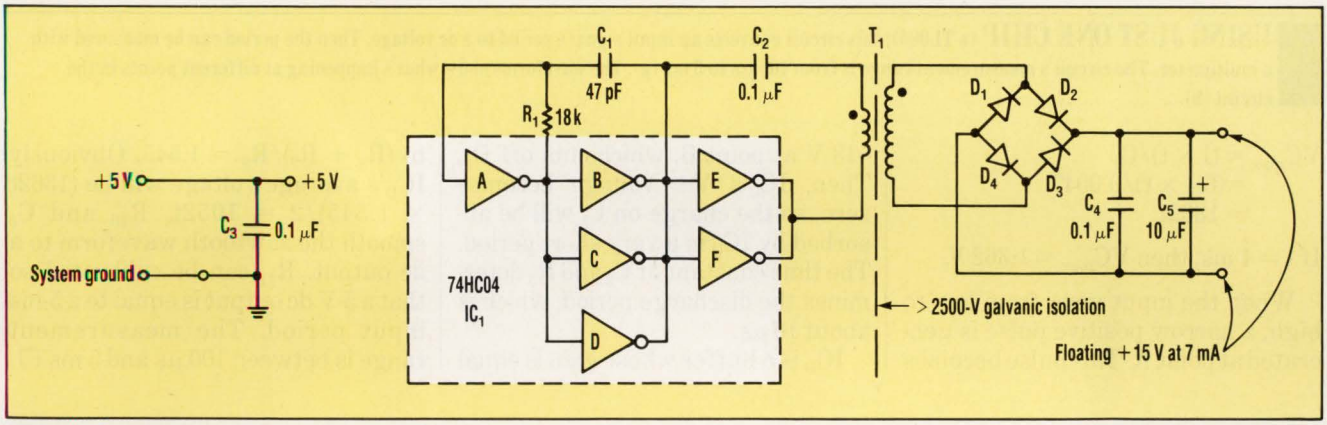
For applications that require a floating 15-V power supply with ±2500 V of isolation, this circuit offers a cost-effective solution. Its parts cost under one dollar. Only the transformer, T_1, sees the full ±2500 V. This makes the circuit low cost because capacitors and resistors rated for ±2500-V operation can be expensive.

The supply takes advantage of the fact that most analog systems don't require very precise power-supply voltages. This is unlike digital-logic circuits, in which ±5% to ±10% power-supply regulation is mandatory for proper operation. Analog-system supplies are constrained by application. For example, a 6-V Zener reference demands at least 7 V to maintain regulation. Typically, many applications requiring high currents only need the high currents for a short time. A variation of this power supply successfully drove high-side power MOS devices with ±2 A of peak gate-drive current.

Two of the 74HC04 inverters are configured as a simple two-inverter oscillator. The values of R_1 and C_1 are chosen to set the oscillator frequency to around 500 kHz. The remaining inverters are placed in parallel to differentially drive T_1 through a dc blocking capacitor, C_2 *(see the figure)*.

T_1 is a ferrite-core toroid transformer whose permeability, μ_o, equals 5000. The ferrite core is available from Fair-Rite, Wallkill, N.Y. (part #5975000201), and costs from 6.5 to 50 cents. The transformer is segment wound with 7 turns in the primary and 25 turns in the secondary. The secondary turns can be adjusted as necessary according to the required load and output voltage. Greater than 2500-V isolation may be obtained by winding, without nicking, both the primary and the secondary with Kynar insulated #30 wire-wrap wire.

A 1N914 diode bridge rectifies the secondary output. A 0.1-μF low equivalent-series resistance and inductance capacitor, in parallel with an aluminum electrolytic capacitor, filters that output. The floating power supply's measured output resistance is about 200 Ω, more than adequate for most low-power analog circuits.□



THIS COST-EFFECTIVE CIRCUIT is a dc power supply isolated to ±2500-V. Because none of the circuit's components (except for the transformer T_1) see the full ±2500 V, expensive high-voltage parts are not needed.

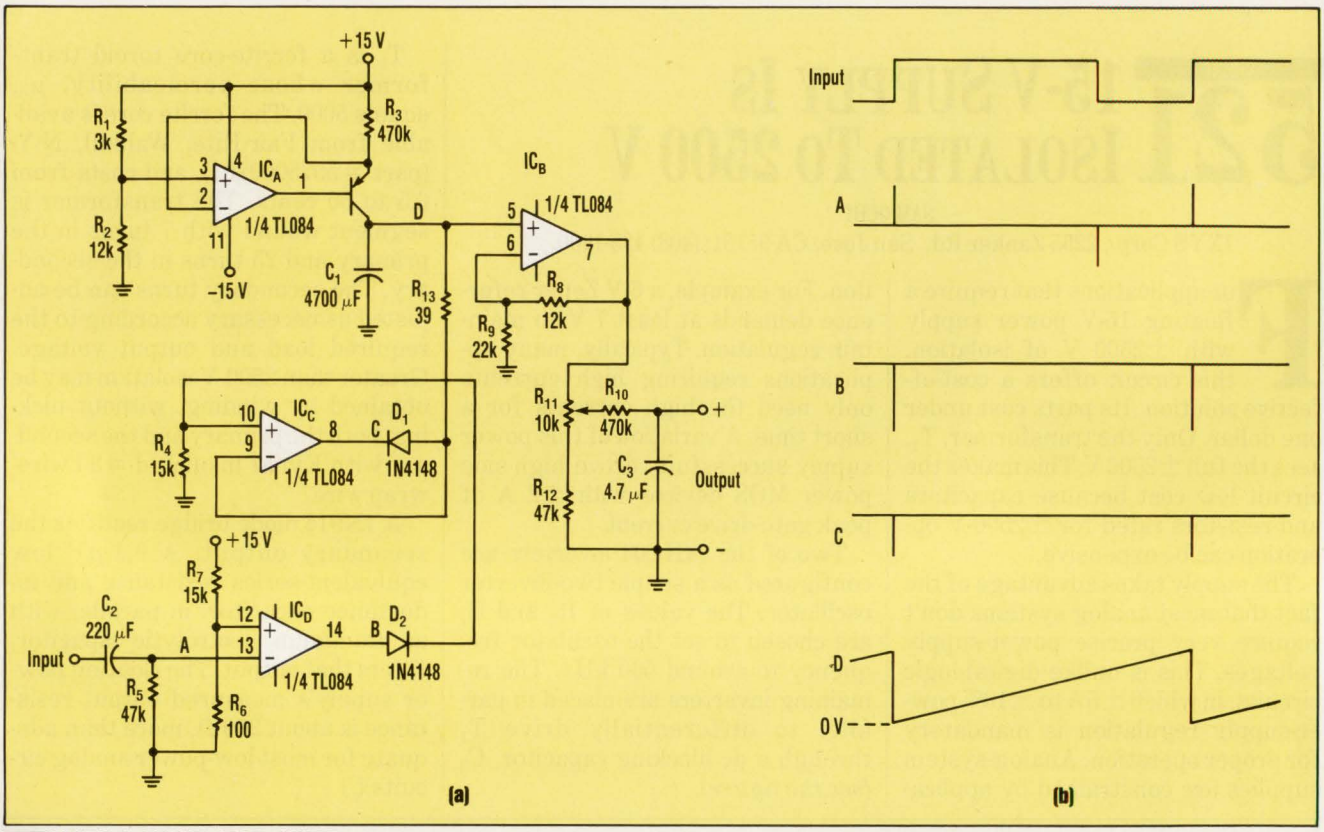
CIRCLE 522 Circuit Converts Period To Voltage

YONGPING XIA
West Virginia University, Dept. of Electrical and Computer Engineering, Morgantown, WV 26506.

If the period of an input signal is converted to a dc voltage, it can be measured using a multimeter. This circuit, built around one TL084 quad JFET input op amp, does just that *(see the figure)*. IC_A, R_{1-3}, and Q_1 form a current source. The current that charges C_1 is given by:

$$I = (V_D \times R_1)/[(R_1 + R_2) \times R_3]$$
$$= (15 \times 3k)/[(3k + 12k) \times 470k]$$
$$= 6.4\ \mu A.$$

The input signal drives IC_D. Because IC_D's positive input (V+) is slightly offset to +0.1 V, its steady state output will be around +13 V. This voltage is sent to IC_C through D_2, setting IC_C's output to +13 V. Therefore, point D is cut off by D_1, and C_1 is charged by the current source. The very high input impedance of the TL084 consumes almost no current, causing the voltage on C_1 to increase linearly. Assuming the initial voltage on C_1 is zero, the maximum voltage (VC_{max}) is given by:



USING JUST ONE CHIP (a TL084), this circuit converts an input signal's period to a dc voltage. Then the period can be measured with a multimeter. The circuit's measurement range is from 100 μs to 5 ms (a). The waveforms show what's happening at different points in the circuit (b).

$$VC_{max} = (I \times t)/C_1$$
$$= (6.4 \times t)/0.0047$$
$$= 1362t.$$

If t = 1 ms, then VC_{max} = 1.362 V.

When the input goes from low to high, a narrow positive pulse is generated at point A. This pulse becomes −13 V at point B, which cuts off D_2. Then, IC_C's V+ voltage becomes zero, so the charge on C_1 will be absorbed by IC_C in a very short period. The time constant of C_2 and R_5 determines the discharge period, which is about 10 μs.

IC_B is a buffer whose gain is equal to $(R_8 + R_9)/R_9 = 1.545$. Obviously IC_D's average voltage will be (1362t × 1.545)/2 = 1052t. R_{10} and C_3 smooth the sawtooth waveform to a dc output. R_{11} can be calibrated so that a 5-V dc output is equal to a 5-ms input period. The measurement range is between 100 μs and 5 ms.□

CIRCLE 523

DIVIDE INPUT CLOCK FREQUENCY

PHILLIP N. DOUGLAS
Memorex Telex Corp., 3301 Terminal Dr., Raleigh, NC 27604; (919) 250-6718.

This circuit, which consists of n clocked flip-flops and one exclusive-OR gate, divides an input clock frequency by 2n − 1 *(Fig. 1)*. With two flip-flops, the circuit divides by three *(Figs. 2a and 2b)*. One main design consideration is that the sum of the delay path from the nth flip-flop's clock input to its Q output (tpff), the dt delay, and the delay through the exclusive-OR gate (tpxr), is at least as long as the flip-flop's minimum clock pulse width (twff):

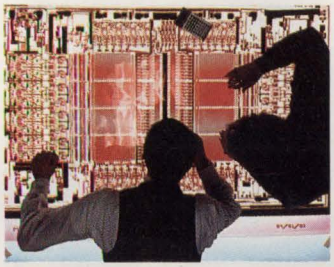
tpff + dt + tpxr > twff.

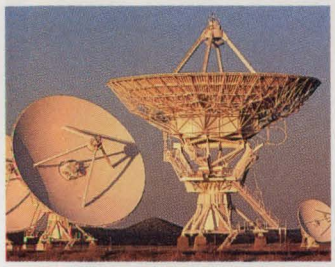
The minimum values for the propagation delays must be used, and in most cases, dt can be zero.

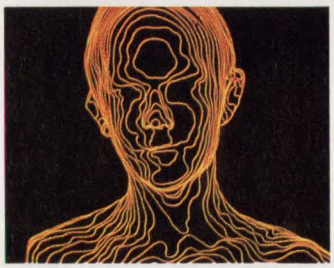
The maximum circuit clock frequency is the lowest frequency determined by three factors. The first is the flip-flop's maximum specified clock frequency (fmax). Second is a frequency that has a period greater than the maximum propagation delay plus the setup time (tsff) for the flip-flop:

Tclk > tpff + tsff.

The third factor is the frequency that has a pulse width (twclk) greater than the sum of the flip-flop's maximum propagation delay plus dt, the exclusive-OR gate's maximum propagation delay, and the minimum clock pulse width required by the flip-flop:







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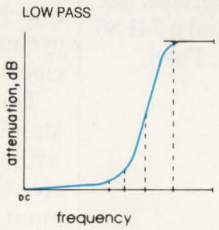
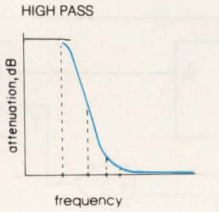


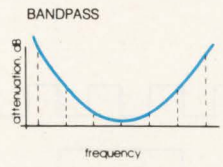
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



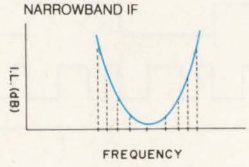
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	PASS BAND, MHz (loss <1dB) Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	STOP BAND, MHz (loss > 10 dB) Max. F4	STOP BAND, MHz (loss > 20 dB) Min. F5	STOP BAND, MHz (loss > 20 dB) Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	STOP BAND, MHz I.L. > 20dB F6	STOP BAND, MHz I.L. > 35dB F7	STOP BAND, MHz I.L. > 35dB F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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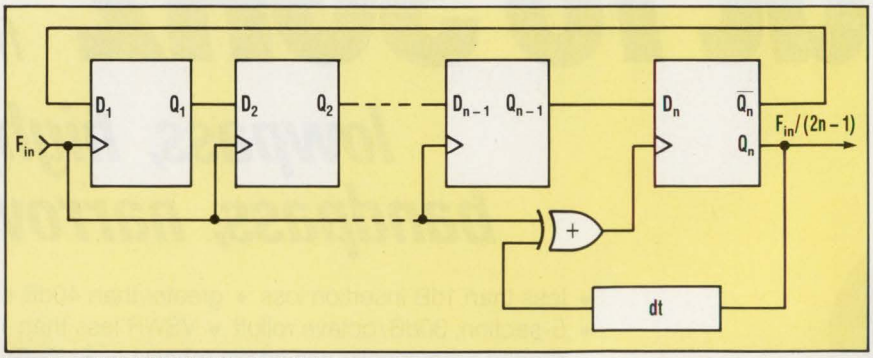
CIRCLE 93

F132-2 REV. ORIG.



1. THE INPUT CLOCK frequency fed into this circuit is divided by 2n − 1. The circuit consists of n clocked flip-flops and one exclusive-OR gate. The dt delay is zero in most cases.

twclk > tpff + dt + tpxr + twff.

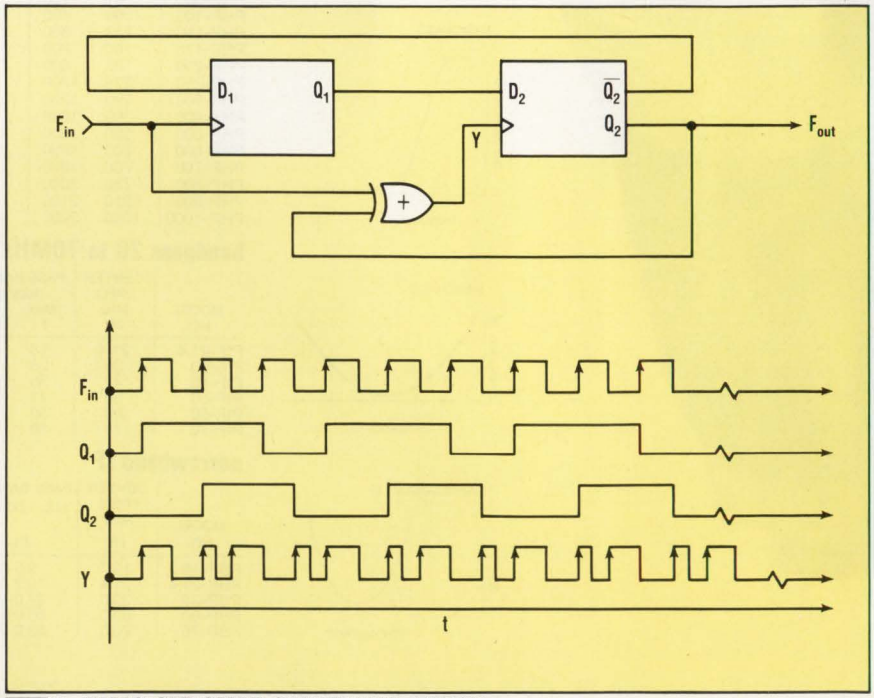
The right side of the inequality should be the minimum pulse width (either up time or down time) of the input clock.

For the divide by three circuit, use 75F74s for the flip-flops and a 74F86 for the exclusive-OR gate. Then,

tpff = 3.8 ns minimum
tpff = 9.2 ns maximum
tw(h) = 4 ns minimum
tw(l) = 5 ns minimum
tsff = 3 ns minimum
fmax = 100 MHz
tpxr = 3 ns minimum
tpxr = 8 ns maximum

Because 3.8 ns + 3 ns > 4 ns, the pulse-width requirement is met when dt = 0. Next, 9.2 ns + 3 ns = 12.2 ns or 81.97 MHz maximum for the second clock-frequency condition. The last condition gives 9.2 ns + 8 ns + 5 ns = 22.2 ns × 2 (for 50% duty cycle) or 44.4 ns, giving a maximum clock frequency of 22.5 MHz.

The circuit, when constructed with standard 74F-type parts, operates without any added delay in the exclusive-OR feedback path and with an input frequency of up to 22.5 MHz. The circuit's output signal will have the same duty cycle as the input clock.□

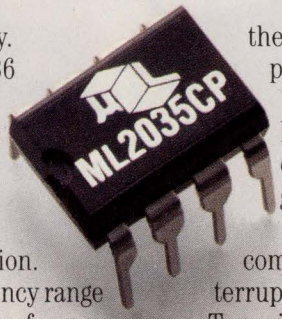


2. THIS CIRCUIT CONFIGURATION divides the input frequency by three (a). The circuit's timing diagram verifies the division (b).

Generate precise sinewaves with just one chip.

Now just one chip does the work of many.

Micro Linear's ML2035 and ML2036 are the industry's first integrated programmable sinewave generators. They're easily programmable from DC to 25kHz (ML2035) or 50kHz (ML2036). Each delivers better than ±.75Hz frequency resolution, and -45dB harmonic distortion.



Absolute error gain over the frequency range is better than ±.1dB. And the frequency reference of the sinewave output is derived from either an external crystal or clock input.

The ML2035 is housed in an 8-pin DIP while the full featured ML2036 is available in a 14-pin DIP or 16-pin SOIC.

At prices starting at $5.95,* the low-cost ML2035 and ML2036 are the perfect single chip solutions to efficient, precise sinewave generation.

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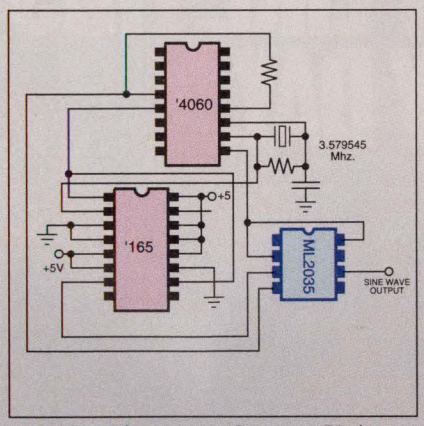
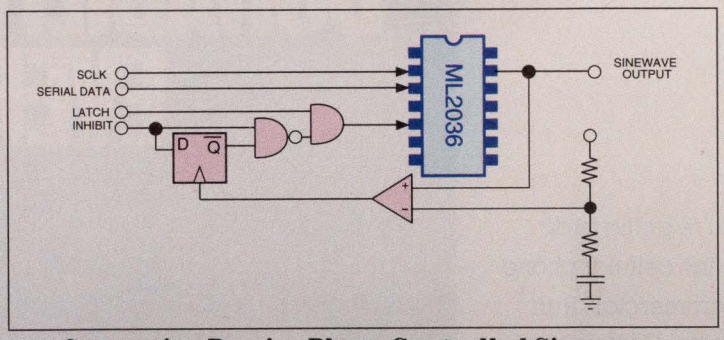
And ask for your copy of our 1991 Data Book, too.

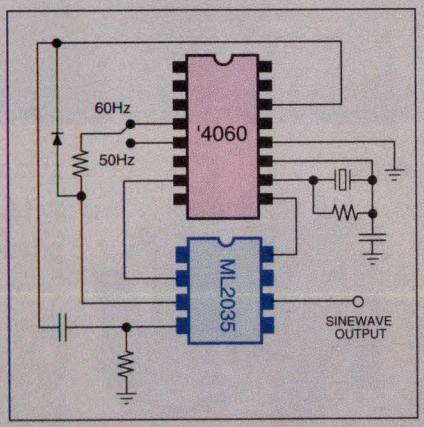
CIRCLE 174



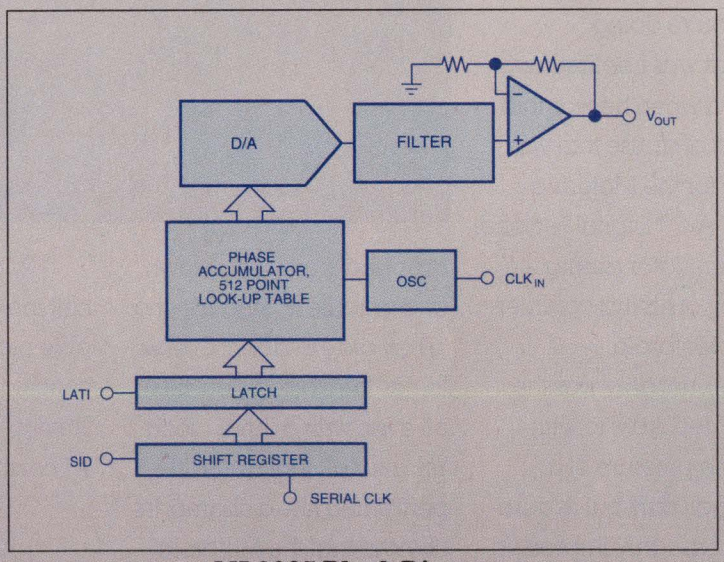
60Hz Sinewave Output Using NTSC Color Burst Crystal



Generating Precise Phase Controlled Sinewaves



Generating Fixed 50Hz and 60Hz Sinewaves



ML2035 Block Diagram

Micro Linear

*Based on lots of 100.

YOU DON'T RUN ACROSS DURABILITY LIKE THIS EVERY DAY.

"You're going to do *what* to the cellular phone in this commercial? Run over it with a golf cart? I sure hope you guys know what you're doing."

That was Lee Trevino's reaction when he was told the kind of abuse that was in store for the Motorola Micro T·A·C™ Digital Personal Communicator during the shooting of his first commercial for Motorola.

Well, not only was the Micro T·A·C able to withstand the pressure of a heavy golf cart, but its durability thoroughly impressed Lee Trevino.

"I saw the Micro T·A·C dropped, bumped, thrown and muddied," said Trevino. "They did just about everything," he added, "but hit it off a tee with a three wood. Yet, after all that abuse, it performed like a champ. It's obvious that the Motorola cellular phone is put together to stay together."

"A lot of people call me a durable player," concluded Trevino, "and if I continue to hold up as well as my Motorola phone, I'll be on the tour for a very long time."

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The way we put them together sets us apart.

CIRCLE 1

CAREER SURVEY

BRINGING A RELIABLE PRODUCT TO MARKET ON TIME—THERE'S THE RUB, ENGINEERS SAY

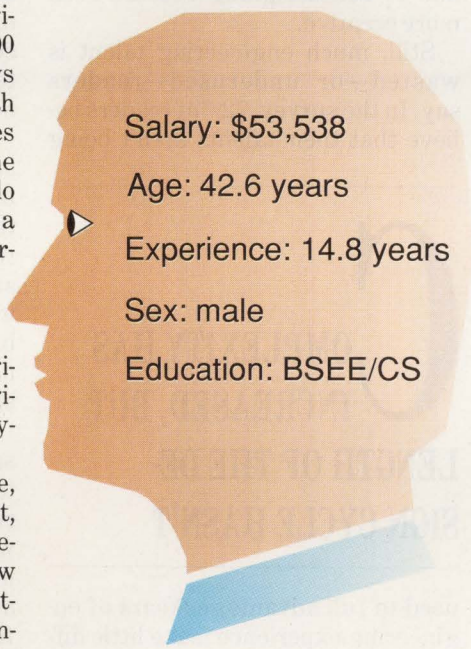
BY SHERRIE VAN TYLE

What's on the minds of design engineers these days? A survey of 1500 ELECTRONIC DESIGN readers shows that engineers are contending with shorter design cycles as companies race to ship new products out the door. "There is only one chance to do it right," says one reader, striking a chord that runs through many survey responses. To come up with quality products and still meet time-to-market deadlines, engineers are turning to concurrent engineering and computer-aided engineering tools—in short, they're trying to get it right the first time.

But the time crunch exacts a price, say engineers: On the work front, there's less time to breadboard designs. "We need to develop new parts faster and manufacture it faster before the customer's design window closes," writes one engineer. As a result, some designers are "forced to cut back on some kinds of testing, especially stress testing."

Fortunately, better design and simulation tools are helping engineers cope with shrinking design cycles. Still, on the personal front, engineers face longer workdays, unpaid overtime, and more stress—this year layoffs have moved up on an engineer's list of concerns. Despite these difficulties and that most engineers surveyed don't think their talents are used to full advantage, most engineers are satisfied with their choice of career.

These findings are drawn from a survey conducted in March. The average reader (respondent) is 42.6 years old, has 14.8 years of engineering experience, and earns $53,538 (more detailed salary information will appear in the Oct. 10 issue of ELECTRONIC DESIGN).



Written responses to the survey show that shorter time to market and a push for higher quality products are weighing heavily on readers' minds this year. That's a big departure from previous surveys in which readers singled out salaries as their biggest career concern.

Still, concern about shorter design cycles and quality isn't altogether surprising. ELECTRONIC DESIGN readers are involved with products both as designers and managers of projects: Of those surveyed, 12.2% manage a project team, 19.9% lead a project, 23.2% manage a technical department or organization, and 39.8% of readers belong to a project team.

The push for quality always affects their job—that's the word from 37% of readers. "There is better awareness on everybody's part as to what *must* happen to bring a quality, reliable product to market," says one reader. Another writes, "It has forced every department to rethink methodologies."

Next in importance is designing with complex components, according to 34% of readers. "The level of complexity has increased," notes one reader, "but the length of the design cycle has not." About 33% of readers say shorter time to market makes their job more difficult. One reader says, "Less time is available to properly verify design and, therefore, there is more fixing after the product is in production."

Separating hardware from software debugging is another thorny problem for 30% of readers. And 27% of readers say they very often have to deal with design for manufacturability; an equal number say their jobs are often affected by multidisciplinary design teams. Shorter design cycles, a reader notes, have "forced a multidisciplinary approach to design for a concurrent cycle."

Compared with the foregoing issues, readers are less concerned about dealing with fewer vendors in the workplace. Just 13% say it very often affects their job. Of negligible concern are military cutbacks: 44%

of readers say a shrinking defense budget never affects their job.

Another problem for readers is developing quality products within a shrinking design cycle. Among readers surveyed, 58% believe the product design cycle has shrunk over the last two years. And 77% of those readers say it has affected their work; 64% of them say a shorter design phase has caused problems for them. As one reader puts it, "Shorter time to market products do not always result in trouble-free products. I've seen many redesigns. The more you rush, the more time you spend fire fighting."

A shorter design cycle can lead to less time for testing. One designer writes, "We have less time for breadboard or prototype evaluation of designs; there's more use of CAD simulation as an alternative."

To cope with shorter time to develop products, readers would like to see standardized interfaces, better design tools, and manufacturing and test objectives being considered up front. One reader comments "We need to do concurrent engineering; we should work with manufacturing engineers early in the design."

Another reader proposes "more reliance on CAE tools and more emphasis on 'right the first time.'" Other readers suggest weekly deadlines. Another notes that "complete and final hardware/software specs are now required before any engineering takes place." Says one engineer, "better definition of products is needed up front. 'Creeping featurism' needs to be controlled."

Another approach is "more thorough design reviews, including customers in the design process more." One reader says he would like to see "better training to shorten the learning curve."

In dealing with shrinking product-development cycles, small companies have the advantage of less overhead, as several readers point out. "In my company, the design cycle to production is 3 months versus 12 to 36 in large corporations," one says.

Notwithstanding the pressures they face as designers, some readers see an up side to shrinking design cycles. Shorter cycles are challenging engineers to work smarter. One writes, "We delegate more work to support groups—purchasing, documentation." Another says, "Better tools have made me more productive." Several readers observe that design tools are becoming more powerful.

Underscoring this, one third of readers believe design has become less by rote in the last three years; 25% believe designing has become more by rote, and 43% believe designing is about the same as it was three years ago. And 84% of readers would like to see designing become even more creative.

Still, much engineering talent is wasted—or underused—readers say. In the survey, 72% of readers believe that their talents aren't being used to full advantage. Years of engineering experience make little difference: 71% of engineers with five or fewer years of experience think talent is being wasted vs. 75% of engineers with 21 or more years in the profession.

COMPLEXITY HAS INCREASED, BUT LENGTH OF THE DESIGN CYCLE HASN'T

That's all the more reason not to buy into reports of an engineering shortage—sparked by a recent National Science Foundation study and bruited in the media. Most readers emphatically don't believe there's a shortage of engineers. A handful say good engineers are in short supply. Others respond that shortages are limited to specialties, like power-related fields and software.

Several readers label such reports company propaganda to keep the labor pool filled and engineering salaries low. Readers also point to attempts by universities to keep a steady influx of engineering students.

Just as contemporary issues, like time to market, are reshaping an engineer's job, tools like computers have already changed the way most engineers work. The PC has become ubiquitous among engineers, the survey shows. Indeed, 97% of readers use a personal computer in their job, for just about every work-related task. Among readers with PCs, 57% perform CAD/CAE, 48% do simulation, 90% perform word processing, and 35% do other various PC-based tasks, such as project management, data acquisition, and automated testing. And just 10% use the PC to do computer-aided software engineering (CASE).

Apart from design concerns, the survey reveals that engineers are more concerned about being laid off this year. In a list of career concerns, readers rank job security second to salary compared with last year, where readers said salary was their biggest concern, followed by the need to keep up with technology. Job security ranked third.

In the 1991 survey, 30% of readers say fair salary is their most important concern, succeeded by job security (28%) and the need to keep up with technology (24%). Readers give much shorter shrift to concerns about ethics (9%); respect for the profession (7%); portable pensions (4%); continuing education (3%); and age discrimination (2%).

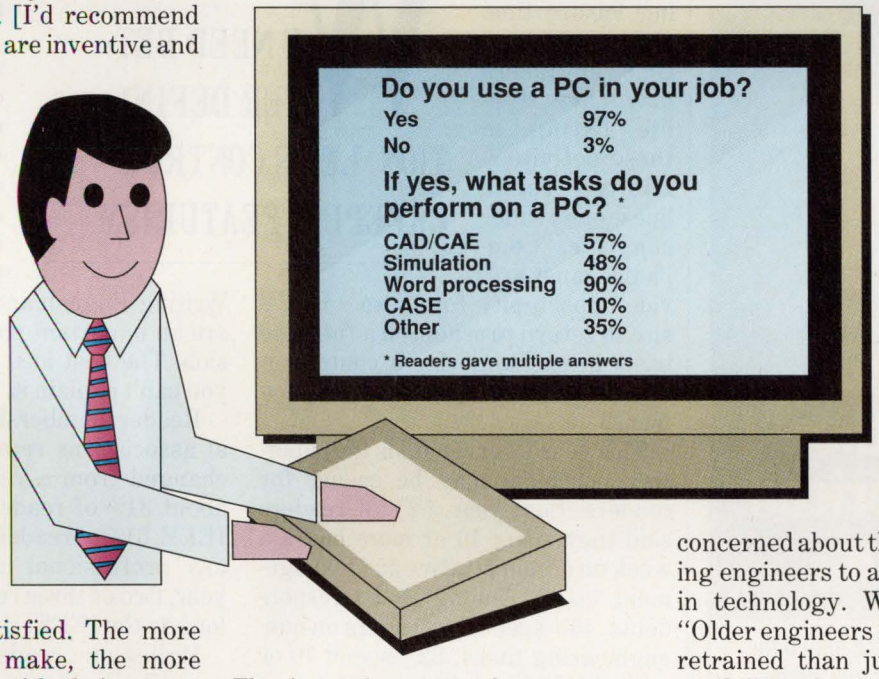
Perhaps reflecting the view that engineering isn't sufficiently appreciated as a profession, some readers believe that they get more recognition from their immediate supervisor than from their company as a whole. Consequently, 81% of readers say their supervisor values their work and 19% disagree. As for the companies they work for, roughly 65% of readers believe their companies give them adequate recognition while about 35% disagree.

About 83% of readers would recommend engineering as a career. One reader finds it, "very demanding. It's sometimes hard to find a happy medium between my profes-

sion and personal—family—life." Another writes, "I consider myself fortunate that my interests have led me into an area, firmware engineering, that is in demand, thus allowing me to remain in engineering and make a good living at it."

Says another, "Engineering is a great career for people who like problem solving, creativity, and 'making things work.'" An engineer notes, "My first love is electronics. For this reason, I feel that I would have been neither as successful nor as satisfied in any other profession."

For these readers, engineering's appeal doesn't lie in salaries. Says one, "If accumulating cash is your main goal—be a lawyer, doctor, or business manager. [I'd recommend engineering] if you are inventive and enjoy this work just for the job of developing and inventing along with a decent salary."



In terms of job satisfaction, overall, 16.1% of respondents described themselves as extremely satisfied with engineering as a career, 51.7% were very satisfied, 28.4% were somewhat satisfied, and just 3.8% were not very satisfied. The more money engineers make, the more satisfied they are with their career choice. Among engineers making $75,000 or more a year, 26.7% were extremely satisfied, 56.7% were very satisfied, and 16.7% were somewhat satisfied. No one in the top salary category was unsatisfied with career choice.

Years of experience, however, had little effect on percentages of job satisfaction or dissatisfaction. Among engineers with 21 or more years of experience, just slightly more than the overall average, or 17.2%, were extremely satisfied, 50.5% were very satisfied, 29% were somewhat satisfied, and 3.2% were not very satisfied. Among respondents with five or fewer years of experience, 14.3% were extremely satisfied with their choice of career, 50% very satisfied, 32.1% somewhat satisfied, and 3.6% not very satisfied.

Although most engineers report themselves as satisfied, readers who are dissatisfied with their career, just as in last year's survey, minced no words in describing the drawbacks of an engineering career. Most common responses were lack of respect for the profession, low salaries, and lack of job security. Writes one, "It takes a certain type of person to be a good engineer. Engineers get very little professional respect. They're at the mercy of accountants and mismanaged as far as job security and corporate direction are concerned. We are just labor pawns in somebody else's chess game."

Says another, "The areas of required expertise change so rapidly that it increases the stress on individuals to stay current."

Among readers comments, a recurring theme is management's lack of understanding and support for the rank and file engineer. One respondent writes, "Very few managers seem to listen to engineers. That's a lot of frustration!" Says another, "Non-technical upper management does not understand engineering, which has lower pay than what a less technical liberal-arts manager [makes]."

On the one hand, most readers believe that their education adequately prepared them for their first job. On the other, some readers find recent graduates ill-prepared to enter the work force.

One-third of respondents have a BSEE/CS, 16.1% have an MSEE/CS degree, 8.4% have an MA/MS, 17.3% took postgraduate engineering courses, and 3% have a doctorate. Female respondents make up just 1% of the 1991 survey.

This year's survey found 77.6% of respondents agreeing that they were prepared for their first job while 75% of 1990's survey responded that they were adequately prepared.

On - the - job training is important for engineering graduates. In fact, engineering has been described as a profession requiring lifelong learning. Readers are thus concerned about the need for retraining engineers to avoid falling behind in technology. Writes one reader, "Older engineers are less likely to be retrained than just hiring a fresh grad." Another says, "Any expertise that an individual develops over a 6- to 18-month period is worthless after 3 to 5 years." According to another reader, "Help is needed on generic training courses for newer technology—ASICs, analog and customer chips, and CAD/CAE for smaller companies."

Readers want better preparation for engineering graduates. Says one reader, "Engineering schools are not providing the latest information to students and do not encourage common sense solutions. Let's encourage a cooperative program, especially during the summer months, to al-

low graduating engineers to have some industry experience." Another writes, "Engineers of the future will need a masters degree as a minimum to jump into the changing market and be able to keep pace."

Readers report that they stay abreast of changing technology by reading trade magazines (91.6%); through personal investigation on the job, (86.7%); working with colleagues (67.1%); reading manufacturers' literature (65.9%); attending special courses and seminars (53.4%); and attending technical courses (37.3%).

With shrinking leisure time and unpaid overtime, engineers may have trouble fitting in these activities. Along these lines, one reader suggests, "Companies must provide opportunity for those who desire to return to school on a full-time basis in exchange for a contract—maybe after 10 years of employment!"

WE NEED BETTER DEFINITION. LET'S CONTROL CREEPING FEATURISM

This year's survey finds the paperwork problem may be easing for readers. Last year, 52% of readers said they spent 10 or more hours a week on administrative and management tasks. Among 1991's respondents, 45% spend 5 to 9 hours on non-engineering tasks, 32% spend 10 or more hours, and 19% spend 1 to 4 hours on these tasks. Just as in last year's survey, however, readers write that administrative tasks, meetings, and clerical tasks gobble up valuable time. Among engineers, a habitual gripe is having to work unpaid overtime: 75% of respondents report working unpaid overtime or on weekends, about the same as last year's survey (77%). And amount of overtime doesn't vary with the number of years of experience.

As in last year's survey, some readers commented on a salary's plateau effect—engineers start off at decent salaries, yet after 15 or so years in the profession, fall behind their professional counterparts in law or medicine.

To counter the plateau effect, an engineer usually becomes a manager. But that's a problem if an engineer chose the career because technology, rather than managing other people, was compelling. One reader writes, "The problem of upward mobility as an engineer is still present in most companies. The only advancement path is into management where the engineering skills are lost, requiring a new set of skills that many engineers either lack or haven't been trained for.

"A poor manager and a lost engineer are the result. For new engineers, I recommend more emphasis on learning how to communicate. Writing English and speaking skills are an important part of the profession. The best idea is of no value if you can't explain it."

Reader membership in professional associations remains largely unchanged from a year ago. In 1991, about 31% of readers belong to the IEEE; 61% of readers don't belong to any professional association. Last year, two of three readers did not belong to the IEEE.

Writes one reader, "Engineering societies are instruments of corporations and universities. They have no concern for the welfare of engineers. We need societies like the AMA, which controls the supply of medical doctors, thus protecting the high income of their members."

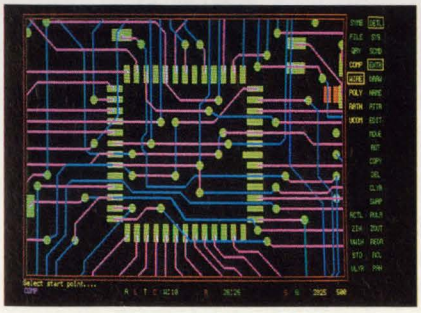
For the survey, readers were chosen at random from the magazine's U. S. circulation. The first 250 questionnaires mailed were tabulated.□

How Valuable?	Circle
Highly	551
Moderately	552
Slightly	553

How P-CAD made the Poqet more productive.

The Poqet PC™ is the complete MS®-DOS PC that's small enough to slip into your pocket. Yet it is powerful enough to run virtually any MS-DOS personal productivity software.

The Poqet PC's small but complex board design made choosing the right PCB design software a very big decision.



P-CAD for DOS-based PC's

P-CAD makes a big thing out of productivity, service and support.

P-CAD gave the Poqet PCB design team the robust functionality and reliability they needed to complete their designs and get their product to market faster. And Poqet chose P-CAD for another very big reason – unparalleled customer service and support.

You see, P-CAD backs customers with technical representatives in 100 nationwide locations. Service from 19 regional training centers. A technical support center and hot-line, user groups, and a 24-hour bulletin board.

Minimum design time for maximum profitability.

Support like this explains why Poqet Computer joined more than 18,000 installations already using P-CAD to minimize design time and maximize profitability.

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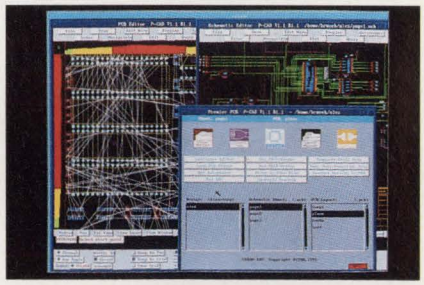

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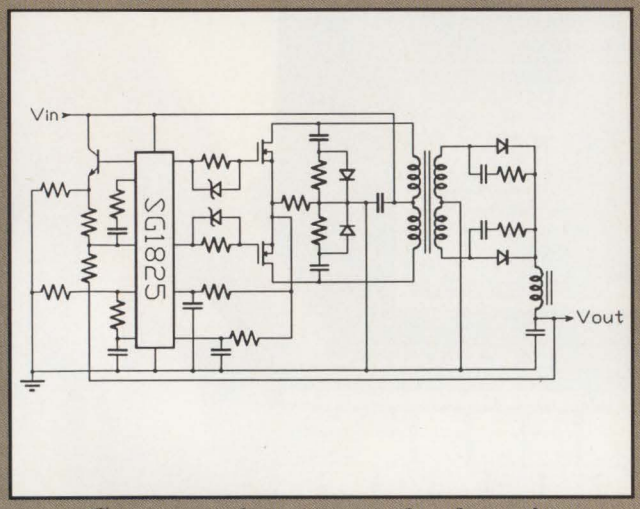
CIRCLE 98

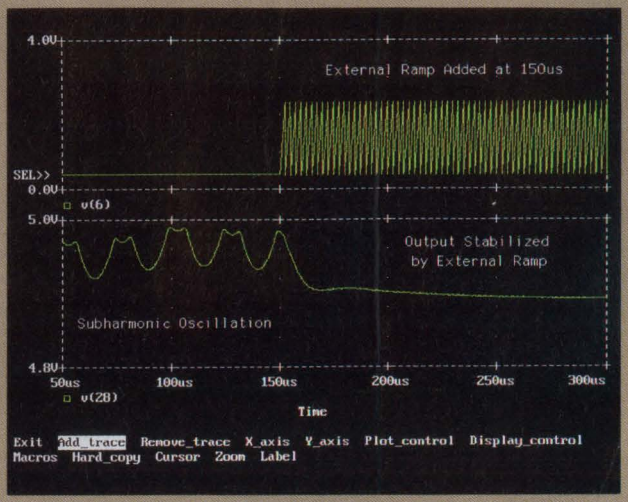
PSpice

MicroSim Corporation

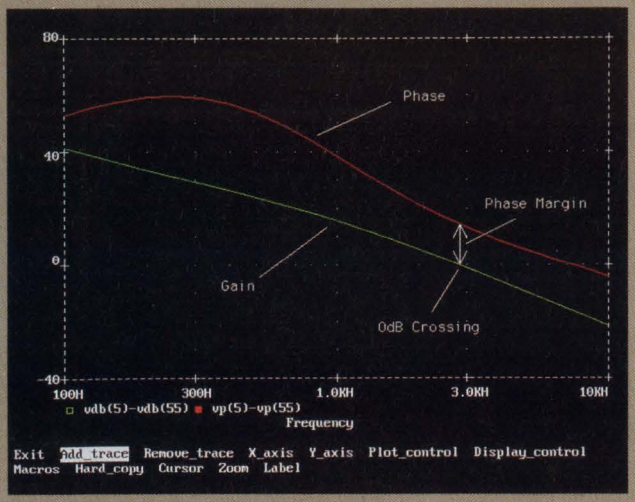
The Standard for Circuit Simulation Switch-Mode Power Supply Design



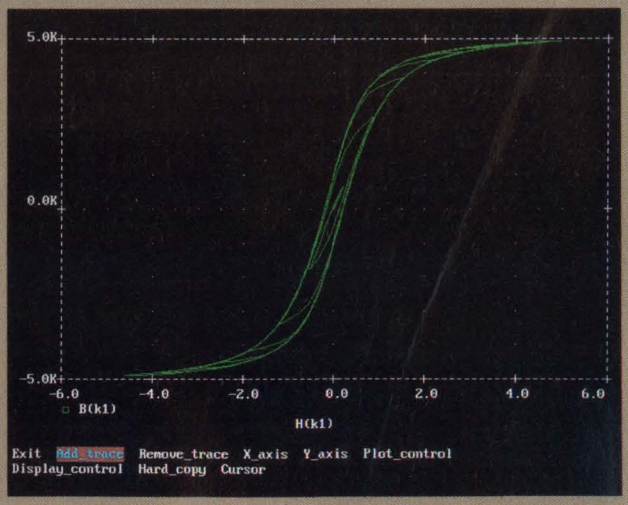
Current mode power supply schematic.



Power supply simulated using mixed analog/digital simulation. Plot shows subharmonic oscillation being suppressed by external ramp.



Simulation using the Vorperian switch model to examine the stability of a power supply.



Hysteresis curve of transformer.

A cycle by cycle simulation of switch-mode power supplies is recognized as a difficult simulation task for SPICE-based simulators, which must cope with timings that can span 4 orders of magnitude. This problem invariably results in very long simulation times, but is improved considerably by MicroSim's approach of building the controller macromodel chips so that a significant section is simulated in the digital domain. PSpice's behavioral modeling and mixed analog/digital simulation capability makes this possible.

PSpice is available on the IBM-PC (running DOS or OS/2); Macintosh II; Sun 3, Sun 4, and SPARCstation; DECstation 2100, 3100, and 5000; and the VAX/VMS families. In addition to the PWM macromodels, the PSpice library contains over 3,500 analog and 1,500 digital parts which can be used in a variety of applications. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022, or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

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CIRCLE 91

ELECTRONIC DESIGN

QUICK LOOK

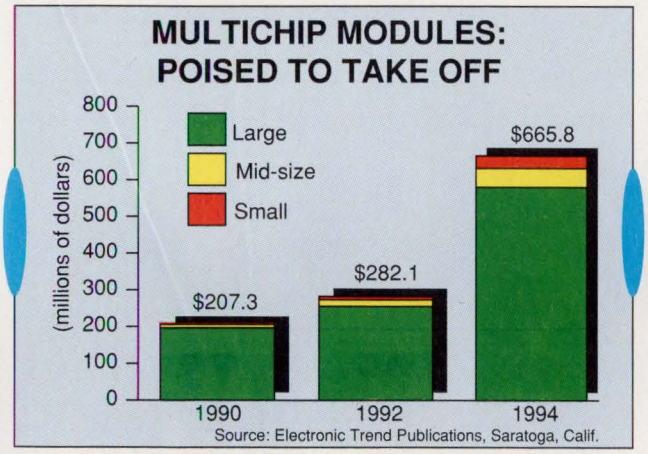
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

The market for multichip modules, once predicted to be worth billions of dollars by 1991, has fallen short of those forecasts. MCMs should generate about $207 million in sales this year, predicts Electronic Trend Publications, a Saratoga, Calif., market researcher. By 1995, the world market is expected to grow 34% a year, with annual sales of roughly $666 million.

Lower than expected growth results from several factors. For one thing, high circuit densities cause heat and electrical problems, which lead to end user difficulties and wariness about the technology. For another, unpackaged die are difficult to test, and ac performance cannot be determined until after assembly.

Steep prices, which range from $50 to $100 per square inch, also dampen sales. As production ramps up, prices should shrink to about $20 to $30 per square inch.



HOT PC PRODUCTS

More and more, long documents and those that mix text and illustration are going onto CD ROM disks. Now IEEE standards documents are on CD ROM. As a result, PC users with CD ROM disks can search for key words, organization names, and document numbers. Once retrieved, pages can be viewed singly or two at once, rotated, or zoomed to read small print and detailed diagrams.

Service will be updated every 60 days. Standards documents cover computers and electronics, instruments, communications, applications, and power. Included is an index to U. S., non-U. S., and international standards.

For prices and other information, contact Information Handling Services, 15 Inverness Way E, Englewood, CO 80150; (800) 241-7827; (303) 790-0600, ext. 59.

TIPS ON INVESTING

Since 1980, the average cost of buying a home has risen almost 50%. In that same time, the cost of tuition, room, and board for a year of college has doubled. But median family income has failed to keep pace with these rising costs, increasing by just 6.4% through the late '80s.

Obviously, engineers with young families have a tougher time reaching fundamental financial goals than their parents did. And older engineers may find themselves helping out their children and grandchildren. A recent survey of homeowners aged 55 to 64 showed that 44% would help their adult children purchase homes, even though only 13% received assistance from their own parents.

You may give each of your children or grandchildren up to $10,000 ($20,000 if you are giving with your spouse) without paying a gift tax. (A gift of any amount is tax-free as long as it is used directly for tuition or for medical expenses.) In fact, your generosity may even reduce your eventual federal estate taxes by removing assets from your estate. However, the recipients of your gifts may have to pay substantial taxes on the income your gift produces. The "kiddie tax" law requires that investment income of more than $1,000 earned by children under 14 will be taxed at their parents' rates. Children 14 and older are taxed at their own rates, which presumably are lower than their parents'.

Perhaps the best way to shift assets to a child under 18 is to establish a custodial account, which are administered on the child's behalf by a custodian whom you designate. Custodial accounts may be established under either the Uniform Gifts to Minors Act (UGMA) or the more recent Uniform Transfer to Minors Act (UTMA). Available in 23 states, UGMAs may contain cash and securities and automatically come under the child's control when he or she turns 18. UTMAs are similar, except that they may also contain real estate, patents, royalties, and paintings. And the child doesn't gain control of the account until age 21 (25 in California). Currently, 27 states and the District of Columbia permit UTMAs.

To minimize taxes and maximize returns, tailor accounts to a child's age. Growth mutual funds are valuable long-term investments giving benefits of professional money management and diversification. Qualified stock, carefully selected and monitored, may produce the best return over the long run.

As your children or grandchildren approach the age of being able to use the money, you may want to shift funds from riskier growth-oriented investments to more secure fixed-income securities such as certificates of deposit (CDs). Zero-coupon Treasury bonds, which give an assured level of income and may be timed to mature when the child reaches a certain age, still have market risks and tax consequences. Zero coupon municipal bonds provide competitive yields on a tax-free basis.

Henry Wiesel is a financial consultant with Shearson Lehman Brothers, (800) 631-2221.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Precise coordination of position, acceleration and power. That's what it takes to torque a discus. Or control precision DC motors. Motors that must start instantly, run up to 100,000 RPM and stop at exactly the right position **every time.**

For brushless or brush-type DC motor control, Motorola has put a new spin on its line of ICePAK™ TMOS Power MOSFETS and Linear motor control ICs. Giving you more efficient techniques for motor control—and perfect torque under pressure.

MC33035 Motor Controller for Maximum Performance

For maximum performance, the MC33035 delivers all the active functions needed for open-loop three or four phase motor control.

- Inputs for speed control, forward/reverse, run enable, dynamic braking
- Rotor position decoder for commutation sequencing
- Error amplifier and PWM comparator for speed control
- Temperature compensated 6.25V reference
- User-selectable 60/300 or 120/240 sensor electrical phasing
- Available 24-pin plastic DIP, −40 to +85°C operating range

MC33033 Motor Controller for Economy of Effort

The low-cost MC33033 motor controller offers the active functions needed for an open-loop three phase or four phase motor control system, either for brush type or brushless motor control.

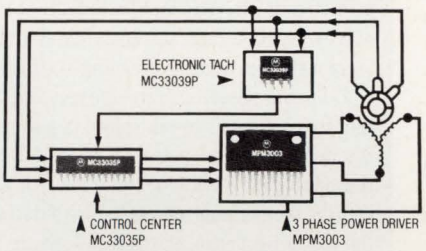
Brush DC motors can be controlled using the MC33033P and the MPM3002 H-bridge for motor drive.

- Rotor position decoder for commutation sequencing
- Error amplifier and PWM comparator for speed control
- Temperature compensated 6.25V reference

MC33039 Closed-Loop Motor Speed Control Adapter

For closed-loop speed control in DC brushless motor control systems, the MC33039 provides motor speed control using Hall Effect sensor signals. It eliminates costly magnetic or optical tachometers for closed-loop applications and enhances low-speed operation by detecting the transitions of all rotor position sensors.

CONTROL OF THREE PHASE BRUSHLESS MOTOR WITH THREE ELEMENTS



- Can be powered from 6.25V reference on MC33035 or MC33033
- Constant speed operation down to 100 RPM

ICePAK™ TMOS Power Modules

To drive brushless motors in three-phase applications, Motorola's MPM3003 "ICePAK" power modules can handle high surge currents at motor start up—to 25A. The MPM3003 is a complete three-phase bridge with three N-channel MOSFETS in the lower legs and P-channel MOSFETS in the three upper legs. This power module can be driven from a three-phase control integrated circuit like the MC33035 with an electronic tachometer (MC33039) to close the loop with minimal cost. Power modules for brush-type designs are the MPM3002 and MPM3004, featuring power MOSFETS in H-bridge configurations.

- Rated at 60 Volts to 100V, 8 to 10 Amps
- P and N channel power MOSFET configuration for improved drive
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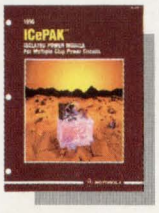

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Please send me Motorola motor control design information.

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QUICKLOOK

OFFERS YOU CAN'T REFUSE

Time to market is a hot topic these days. Along these lines, Logic Automation is offering a free time-to-market kit to design engineers and managers. The kit has a slide rule to compute revenue lost by delay in putting a product on the market. Also included is a booklet, "Electronic Design and Simulation: Cost, Quality, and Time to Market." To request a kit, contact the company at P. O. 310, Beaverton, OR 97075; (503) 690-6920; fax (503) 690-6906.

CIRCLE 524

A 19-page guide, "How the United States Can Compete in the World Marketplace," is free from the IEEE's United States Activities unit. The guide has sections on purchasing, investing in manufacturing processes, overcoming provincialism, improving work force education, and changing government policy.

Also free, a 13-page report, "Electrotechnology in the Federal FY 1992 Research and Development Budget," summarizes 1992 R&D budgets for electrical and electronics technology.

Copies can be obtained through IEEE-USA, 1828 L Street, NW, Suite 1202, Washington, DC 20036-5104; (202) 785-0017.

CIRCLE 525

A demo disk for Spice Optimizer is free from US Logic. Spice Optimizer gets the same results as simulating backward. The industry-standard Spice analog simulator goes from an initial condition to an end result over time, in the transient mode.

Optimizer also works with the transient and ac modes of Spice. A user edits a few simple lines in the Spice netlist and starts the optimizer. A setup screen displays relevant parameters and provides for possible corrections. Then the loop process is started. Contact the company at 1741 Katella Ave., P. O. Box 5922, Orange, CA 92613-5922; (714) 744-1252.

CIRCLE 526

Finding a power supply could get easier with an on-disk catalog from Computer Products. The PowerPath disk catalog gives details on 400 ac/dc and dc/dc power converters. Contact the company at 3797 Spinnaker Ct., P. O. Box 5102, Fremont, CA 94537-5102; (415) 657-6700; fax (415) 683-6400.

CIRCLE 527

DID YOU KNOW?

... that the U. S. robotics industry set a record for new orders and shipments last year. Shipments of $485 million were 9% more than during the previous best in 1984, which was also a boom period for robotics. *Robotic Industries Association*

... that laser disk players are catching on. About 600,000 are in U. S. households. The number of player manufacturers has doubled since last year, to 17. And at least 30 companies make combi players—machines that play laser and compact disks. *Laser Disc Association*

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

Synthesis of thought and motion is usually not associated with the act of carrying an activity to completion. The game of soccer illustrates the point. Rules are set; the game is well-defined. Before kick-off, a game plan has been put into place. With each tick of the clock, the game is played out to determine the eventual winner. Each player on the field works to synthesize the next offensive, or defensive, play opportunity. Within the game's limits, all participants strive to maximize their abilities. The players' minds are working; action stops only when time runs out. Dynamic synthesis is carried out by all persons on the field. Key team members and the coaching staff provide leadership.

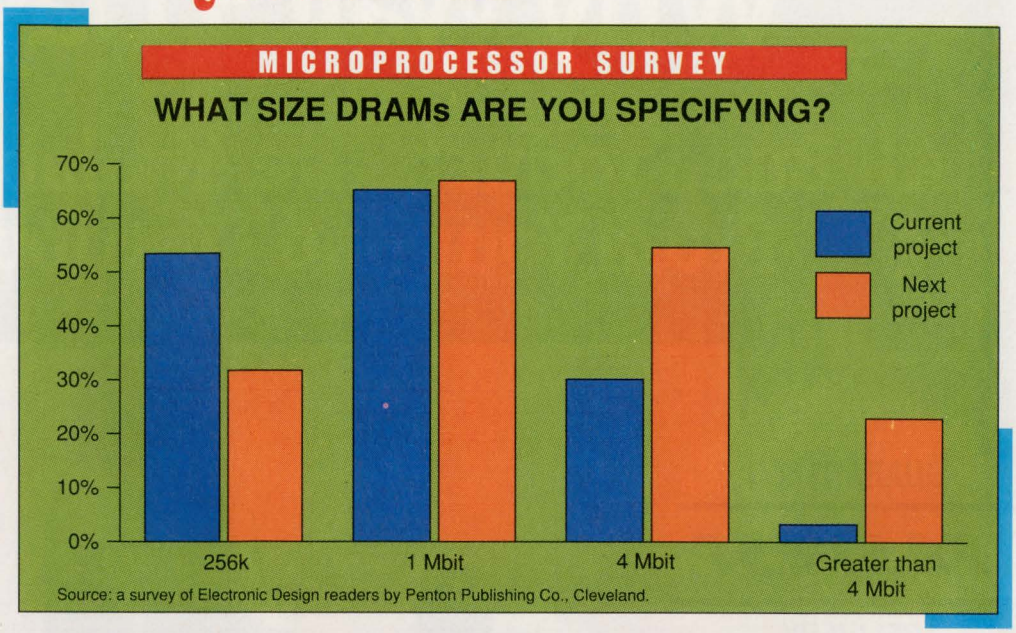
Like the soccer example, executing a project plan is a dynamic process that often requires synthesis to take place in a short time relative to other time pressures felt during the definition and planning phases. Definition decisions tend to have the luxury of a reasonably slow moving clock. There is time pressure. But it can generally be measured in months (sometimes years) before a definition can be properly synthesized. Upon entering the planning phase, the process speeds up. Cross-functional plans can be synthesized in three to six weeks. During the execution phase, decisions need to be synthesized in days or hours. Time becomes very precious. The penalties for letting it slip by are severe. The transition into the executive plans must be managed to ensure that the new product-development team has an effective start.

For process participants, a new perspective on the product-development effort must develop rapidly. Attention shifts from thinking, exploration, and planning to a situation where the team members have to actually produce the abstractions within the product's definition. For some new product developers, this is a difficult period. Engineers and technologists sometimes want to continue refining the technology to create the product; marketing personnel start to have second thoughts about feature sets and performance numbers; and manufacturing may have doubts about how certain critical processes will perform. Also leadership and management styles must undergo a rapid revision.

An informal and sometimes casual control system must be replaced by a system that runs more by numbers and data than by intuition. Too much is happening too quickly on a concurrent basis to comprehend the situation without process measurement and data analysis. Therefore, as team members are making the transition to the production of real output, they also become aware of the fact that what they do will be measured on a periodic basis. In effect, the entire team moves from preparing to be in the execution phase to actually being in the execution phase! The reference plan becomes the competition. If the team can perform to, or slightly ahead of, plan, a winning situation is in progress. When progress departs from the plan, participants must be prepared to make adjustments to recover and retake a lead position with respect to the reference plan. At no time does the process come to rest until end objectives have been achieved.

QUICKLOOK

Dynamic memories are working their way into most systems. To find out just how designers recommend, specify, and authorize purchases of DRAMs, Penton Publishing Co.'s research department surveyed 2000 readers of *Electronic Design*. Responses of those involved with DRAMs were then tabulated and analyzed. Readers, who also were asked about ASICs and other components, were chosen at random from the magazine's U. S. circulation.



BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *C Language Algorithms for Digital Signal Processing* by Paul Embree. Prentice-Hall, 1990. ***$50.***
2. *RF Circuit Design* by Christopher Bowick. Macmillan, 1982. ***$24.95.***
3. *Noise Reduction Techniques in Electronic Systems* by Henry Ott. John Wiley & Sons, 1988. ***$47.95.***
4. *Circuits, Interconnections, and Packaging for VLSI* by H. B. Bakoglu. Addison-Wesley, 1988. ***$47.75.***
5. *Principles of Electronic Packaging* by Donald Seraphim. McGraw-Hill, 1989. ***$56.95.***

COMPUTER SCIENCE:

1. *Object-Oriented Design with Applications* by Grady Booch. Addison-Wesley, 1990, ***$38.50.***
2. *C++ Primer* by Stanley Lippman. Addison-Wesley, 1989. ***$30.50.***
3. *C Programming Language*, second edition, by Brian Kernighan and Dennis Richie. Prentice-Hall, 1989. ***$32.***
4. *PostScript Language Reference*, second edition, Adobe Systems, Addison-Wesley, 1991. ***$28.95.***
5. *The Power of Penpoint* by Robert Carr. Addison-Wesley, 1991. ***$22.95.***

Compiled by Stacey's Bookstore, Palo Alto, Calif.; (415) 326-0681.

THE PROFESSION

North American business is slowly coming to realize that an educated workforce is its key competitive edge. Nowhere is this truer than in engineering, where technology changes ever more rapidly. Nonetheless, several recent surveys show that only 42% of engineers had been involved in any formal continuing education program in the last 6 months.

Continuing education is an individual's responsibility, but the cost of continuing education is prohibitive for many engineers. Employers must encourage, support, and reward their employees' efforts in keeping up to date. They also cannot expect engineers to do it entirely on their own time. The amount of leisure time for the average American has shrunk 37% since 1973. During the same period, the average work week, including commuting, has jumped from less than 41 hours to nearly 47 hours. Employers can offer inducements like time off and promotions, but some employers have to resort to education as an enticement for recruiting new engineers.

Employers should remember that expertise attracts more expertise. IBM's Corp.'s reputation for pure research, enhanced by Nobel prize winners on its staff, helps draw top-rank scientists—75% of those offered jobs accepted. To increase the benefits of education for engineers, information has to flow freely inside and outside of corporations. IBM, for example, attributes the success of its research lab in Zurich, Switzerland, to the ethnic diversity and the multitude of disciplines there. The researcher pool is in constant flux with visiting scientists and summer students.

For its part, Hewlett-Packard promotes communication between employees and eliminates status distinctions that might inhibit the flow of ideas. Researchers, for example, demonstrate their ideas to others in "town centers" to get comments and suggestions from coworkers. Both IBM and H-P encourage people of all disciplines, including secretaries, to propose ideas.

The freewheeling, Western-style brainstorming sessions do not work everywhere, though. In Japan, for example, sessions are more structured (the Japanese learning style is heavily based on rote and memory and doesn't promote creative thinking).

Companies reap benefits from investing in training. Motorola Inc. obtained rates of return of up to 30 times dollars invested and now invests 2.5% of its payroll in training. The company even trains its suppliers because ignorance is costly. Every worker at IBM spends at least 40 hours in the classroom each year while the U. S. average is 4.5 hours per year; Japan's average is 200 hours a year. For the technical workforce, an employer's competitive edge depends on what information or knowledge its staff has access to. Because of increasing family commitments, training needs to be provided during working hours. Engineers can then expect to have a mix of work, teaching, and study as part of future job descriptions.

by Alain Beaulieu, Ottawa, Ontario, Canada. He is a project engineer for Canada's Department of National Defence.

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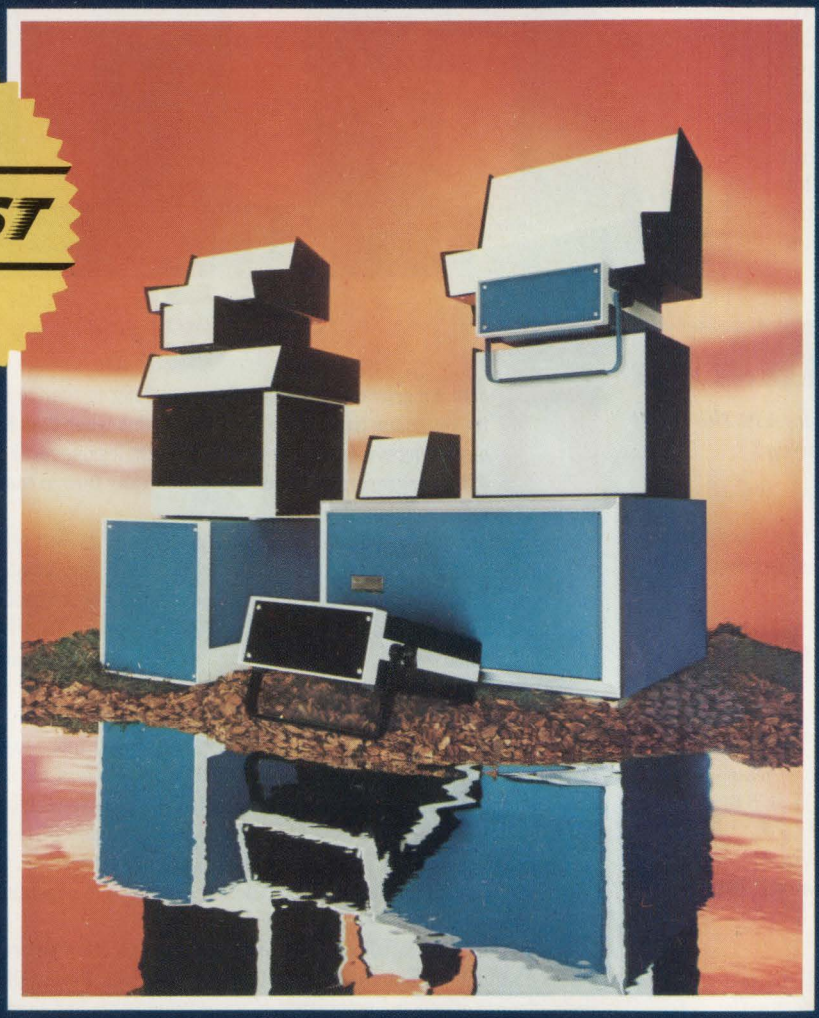

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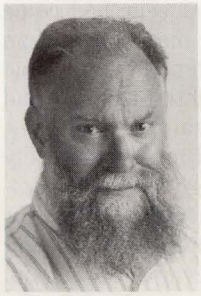
CIRCLE 82

WHAT'S ALL THIS COTTAGE-CHEESE STUFF, ANYHOW?

Once upon a time (to be specific, about 1950), there were no nuclear-powered submarines. So when the U.S. Navy decided that they wanted to plan for some nuclear submarines (that would be able to cruise for many weeks without coming into port for fuel or food), they began to do some very thoughtful planning. They took an old conventional submarine, sealed it up, immersed it, and berthed it at the end of a dock in New London, Connecticut. Then they set up some pretend games that a nuclear submarine would have to play.

A crew of a few dozen seasoned submariners were sent down, with a good supply of food and other standard supplies. Then after a few weeks, they asked the sailors, "What food would you like to have?" The sailors sent up a list that included such things as, "coffee ice-cream, carrots, and cottage cheese." Within a week, the supply crew sent down coffee ice-cream and carrots.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

The next week, the Navy planners sent down a questionnaire again: What would you like to eat? The questionnaires were filled in: fried chicken, Swiss steak, and cottage cheese. Shortly, the Navy fulfilled the sailors' requests for fried chicken and Swiss steak—but for some odd reason the Navy could not supply cottage cheese. Week after week, the brilliant planners asked, "What is missing in your diet?" And every week the sailors renewed their requests. And on every list, the men kept asking for cottage cheese—because when they were making up their new list, they took the previous lists and asked for anything they had not yet received.

After many months, an enterprising young newspaper reporter decided there must be some kind of a story, something around this area of planning for the much-heralded nuclear submarines that he could make a story out of. He requested, and obtained, a large amount of random (but de-classified) information.

Included in the information was the "request list" for various kinds of food. The reporter was bright enough to do a *scientific* analysis of the lists the sailors sent up from their test space. And what was the result of this *scientific* analysis? The sailors kept asking for *cottage cheese*. Every week, the sailors renewed their request for *more* cottage cheese. More and more, the requests rang out, "More cottage cheese!"

My, but a sailor on a nuclear submarine will soon develop a *craving* for COTTAGE CHEESE!!! So the reporter filed his story, and soon the world learned that, if you go down on a long cruise in a nuclear submarine, the isotopes and the synchrotrons and the nuclear physics will lead you to crave COTTAGE CHEESE. It's a well-documented fact.

Of course, the mere fact that the sailors simply asked for everything they had previously asked for (but had never gotten any delivery of) was not a fact available to the bright young reporter. The fact that cottage cheese was one of the few foods that the Navy discovered you could not store in a freezer was not obvious to the bright young reporter. So the artifact of the "craving" was not evident to him, and it took a long time before the hoax of the "craving for cottage cheese" was discovered.

A while back, my boss called a meeting about our new Capital Plan. We should bring a list of Important New Equipment that we will need to fulfill our projects. Now, you probably suspect (correctly) that I am a klutz when it comes to neatly documented plans and paperwork.

So when my boss asked me for a list of equipment we ought to buy, he was astonished when I handed him a neatly typed list of equipment, part numbers, quantity discounts, delivery dates, etc. I mean, the paperwork looked almost neat and coordinated, and my boss was struck by the amazing, *unprecedented* degree of precision and professionalism. He asked, "Bob, why is this list so neat?"

I replied, "It's the same as last year's list. It's all the equipment that we needed to buy last year—the equipment that got disapproved at the last minute...." He replied *"Oh."*

I explained that I only needed this equipment last year, so me and my guys could do our work more efficiently. If I couldn't get it last year, well, it would still be helpful this year, or next year.

I pointed out something I had read, that linear circuit engineers are the most persistent guys in the world. If they can't get the fanciest new computer, or the fanciest software, or a good modern scope or DVM, or the highest resolution fab equipment, well, they can make do with what they have got. It may be a little inefficient, but they get things done, one way or another. *This* year, though, I got my Capital Equipment.

There are a lot of times people ask for things and they don't get them. What do they do next? Sometimes they wait and see. Sometimes they scheme and plot on how to get it anyhow. Other people holler and scream and raise a ruckus, because to acquiesce to a re-

PEASE PORRIDGE

fusal might be interpreted to mean that you really didn't need it very much after all.

One time I needed some power supplies, and even though these little supplies were not a capital item, I could not get authorization to release the funds in this half of the fiscal year. I got in a demo of this power supply, and it was a really nice machine, well designed and really well built.

Just then I got a call from the distributor. The distributor was going out of business (even though the manufacturer was not), and I could get as many as I wanted of these power supplies, at 40% off, if I ordered right away, before the distributor shut down. I knew I could not get authorization to buy these for many weeks.

What to do? After some soul-searching, I gave the guy my credit-card number and told him to send four to my house. They arrived soon, and I brought them in to the lab, where they have been very popular ever since.

Half a year later, I asked my boss to approve a check to pay for all of those nice power supplies that we had been using for several months, since the second half of the fiscal year had come around with a little more funds than the first half. He listened to my whole story. He was delighted that we had gotten such a good deal on the supplies, but then he chewed me out severely because it was going to be very complicated to get a check approved for that long tangled chain of finance. So I promised I would never do *that* again. And I did eventually get a check for the $1400 I had spent. Well, I'll never do that again. I may do something else, but I'll never do *that* again.

It's the same way at my house. If there is something that somebody has requested but has not been able to get, well, that's "Cottage Cheese." At least until we find a way to get what we need.

All for now. / Comments invited! /
RAP / Robert A. Pease / Engineer

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HEWLETT PACKARD

CIRCLE 88

DUAL SWITCHED DEVICE HAS TWO IDENTICAL AND INDEPENDENT INTEGRATORS. EACH OP-AMP INTEGRATOR CONVERTS MINUTE CURRENTS TO VOLTAGES OVER A WIDE DYNAMIC RANGE.

INTEGRATOR IC CONVERTS PICOAMPERES TO VOLTS

FRANK GOODENOUGH

Measuring small currents accurately, at any time, is a tricky business. This is especially the case if it must be done on-line outside of a laboratory, and the currents continuously range from picoamperes to microamperes. The conventional approach is to use a transimpedance amplifier (an op amp connected as a current-to-voltage converter). Such a circuit can be noisy. Moreover, it requires a large, precision, feedback resistor on the order of 10^9 or 10^{10} Ω, an expensive component that's not readily available.

To remedy the situation, Burr-Brown developed the ACF2101, an IC it calls a switched integrator (the chip actually holds two identical integrators). It might be considered a form of sample-and-hold amplifier. Basically, the current source is connected to the summing point of a very low bias-current op amp operating as an integrator. The chip's 100-pF oxide capacitor integrates the input current *(see the figure)*. The output voltage is a function of the current, the capacitance, and the integration time, as defined by:

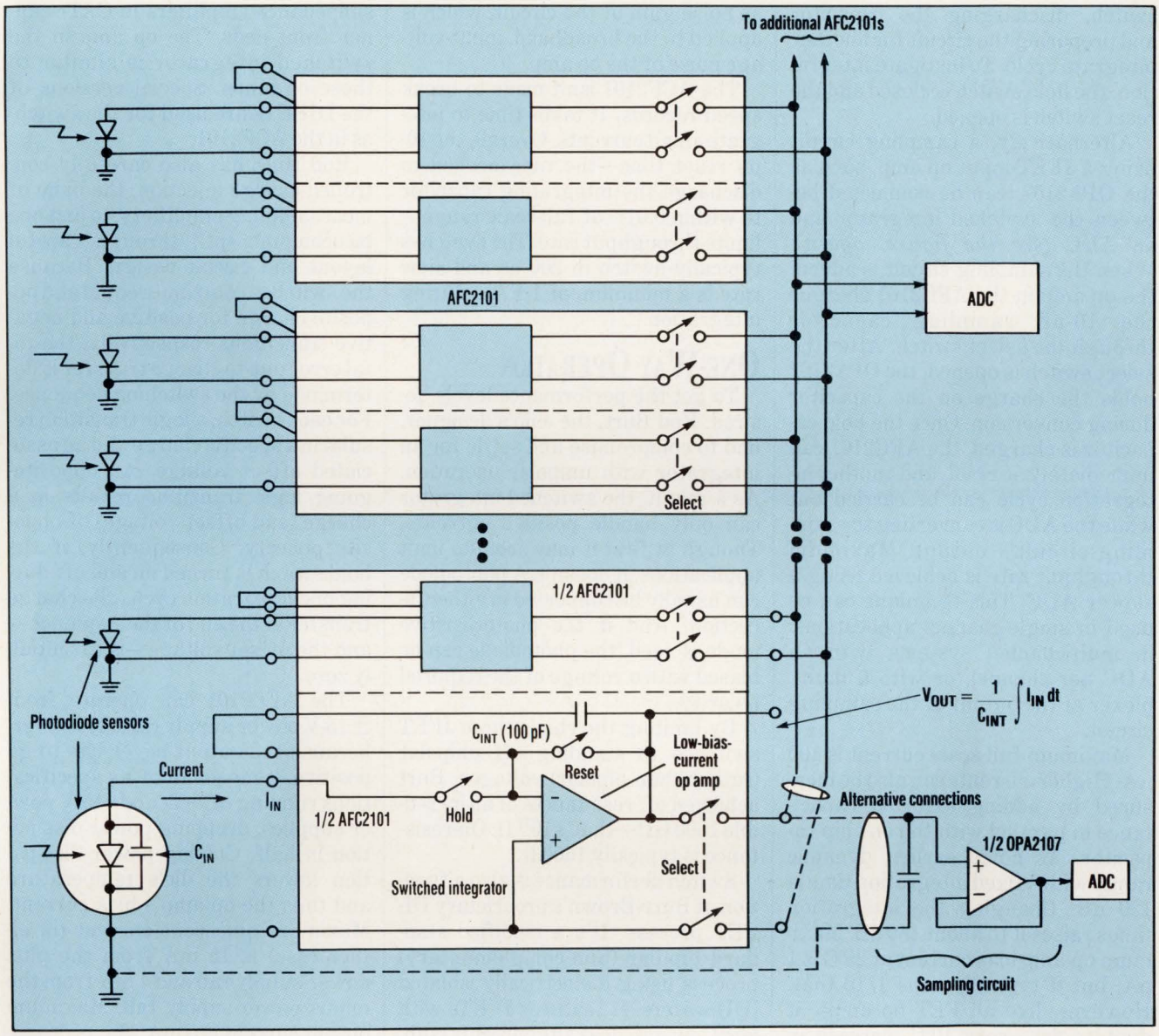
$$V_{out} = -\frac{1}{C_{INT}} \int I_{IN}\, dt$$

The IC was developed for the front ends of CAT scanners that contain 500 to 1000 X-ray detectors. The output of each detector is a photodiode—a current source. The variable density of the material penetrated by the X-rays can result in currents representing a million-to-one dynamic range, creating a huge challenge for instruments making accurate current measurements. For example, the instrument must resolve currents of 10 pA out of a full-scale current of 10 μA. These currents must be converted into voltages that are multiplexed and fed to one or more, high-speed, high-resolution analog-to-digital converters (ADCs).

Most applications for switched integrators are in process control and medical instrumentation. In both applications, they aid in the high-speed, on-line, and accurate chemical analysis of liquid and gas fluids. A leading analysis technique consists of shining a beam of light through a fluid and measuring the change in light intensity and/or color. Photodiodes (current sources) handle the light sensing in these instruments and systems. Flue gas is analyzed in this manner and, of course, photometers and spectrophotometers are a natural for photodiode sensors.

In most single-measurement instruments, a reference channel is also employed. For example, a second light beam is passed through a reference fluid. The difference between the intensity of the reference beam (as sensed by a photodiode) and the measurement beam represents the desired information. Thus, even in a single-

CURRENT-MEASURING DUAL SWITCHED INTEGRATOR



EACH HALF OF THE AFC2101 dual switched integrator converts currents, from a few picoamperes to tens of microamperes, to a voltage. This is done by integrating the current on the chip's 100-pF oxide capacitor. Logic inputs (not shown) control the on-chip hold, reset, and select analog switches.

channel instrument, both halves of the switched-integrator IC are required.

Because both integrators are on the same chip, most drift due to time and temperature will occur in both and appear as common-mode signals. They won't be seen in the difference. Other applications include electrometers, nuclear-particle detectors, and analog computers.

Most sample-and-hold amplifiers operate in just the hold and sample modes. The ACF2101 switched integrator operates in three modes: integrate, hold, and reset. During the integrate mode, the hold switch is closed, the reset switch is open, and the circuit is integrating a positive current source so that the op amp's output goes negative. When enough time passes for the largest expected current to create an output of –10 V full scale, the circuit is put in the hold mode by opening the hold switch, and the op amp's output remains constant.

At this time, if the ACF2101 is connected to an ADC through the "select" switch or from the direct output, the ADC can be given a convert command *(see the figure, part a)*. If multiple ACF2101s are in use, as in a CAT scanner, the select switch has been open. Then, acting as a multiplexer, it's closed, connecting the output to a common bus running to an ADC. Once the select switch closes, analog-to-digital conversion can start. When conversion is completed, the control circuits open the select switch and close the reset

CURRENT-MEASURING DUAL SWITCHED INTEGRATOR

switch, discharging the capacitor and preparing the circuit for another integrate cycle. To instigate integration, the hold switch is closed and the reset switch is opened.

Alternatively, a sampling circuit using a JFET-input op amp, such as the OPA2107, can be connected between the switched integrator and an ADC *(see the figure, again)*. When the sampling circuit is added, the op amp in the AFC2101 charges the 10-nF sampling capacitor through the select switch. After the select switch is opened, the OPA2107 holds the charge on the capacitor during conversion. Once the hold capacitor is charged, the AFC2101 can immediately be reset, and another integration cycle can be carried out while the ADC is converting the sampling circuit's output. Maximum throughput rate is achieved using a slower ADC. This technique can be used in single-channel applications, in multichannel systems with an ADC per channel, or with a multiplexer at the output of the sampling circuit.

Maximum full-scale current is 100 μA. Higher currents can also be measured by adding external capacitance in parallel with the on-chip capacitor. As noted earlier, dynamic range with a fixed integration time is 120 dB. Changing the integration times raises it to about 180 dB. Maximum op-amp bias current at 25°C is 1 pA, but it typically runs 1/10 that. However, like all FET op amps, it doubles for every 10°C increase in temperature. Nonlinearity error runs a maximum of $\pm$0.01% of full scale.

Between 0.1 and 10 Hz, total noise at the output, in any mode, typically runs 2 μV rms. In the hold and reset modes, wide-band noise (between 0.1 Hz and 250 kHz) typically runs 10 μV rms. In the same band, noise during integration is expressed by the following equation:

$$\text{noise} = 10(1 + C_{IN}/C_{INT})\ \mu\text{V rms}$$

where C_{IN} is the capacitance of the sensor connected to the AFC2101's input, and C_{INT} is the integrating capacitor's capacitance. The ratio of the two capacitances represents the ac noise gain of the circuit, which is applied to the broadband, input-voltage noise of the op amp.

The ACF2101 isn't made to break speed records. It takes time to integrate small currents. Overall, the 10-μs reset time—the time needed to discharge the integrating capacitor to within 0.01% of full-scale range—limits throughput rate. The switches typically switch in 200 ns and slew rate is a minimum of 1 V/μs during integration.

ONE-WAY OPERATION

To get the performance levels desired, Rod Burt, the chip's designer, had to compromise and settle for an integrator with unipolar operation. As a result, the switched integrator can only handle positive currents. Though at first it may seem to limit applications, it doesn't. A photodiode can usually be connected in either direction. And if the photoresistive mode is used, the photodiode can be biased with a voltage of the required polarity.

By limiting the chip's three JFET switches to standing off unipolar (rather than bipolar) voltages, Burt achieved off resistances of an incredible 1000 GΩ—that's $10^{12}\ \Omega$. On-resistance is typically 1500 Ω.

Switch performance is also a function of Burr-Brown's proprietary DIFET process. It's a modified standard bipolar (non-complementary) process using dielectrically isolated (DI) wafers. It features JFETs with very low gate leakage currents (subpicoamperes) and very low noise. The JFETs are built in the wafer's oxide tubs along with vertical npn and lateral pnp transistors. The tubs virtually eliminate leakage to the substrate.

Passive devices from the process include thin-film resistors and oxide capacitors. Burr-Brown's designers took advantage of these capacitors because they sport the low dielectric absorption mandatory to store charge accurately. Without that characteristic, off-chip capacitors would be needed.

Burr-Brown developed the process for its low-noise, low-bias-current FET op amps now used as transimpedance amplifiers in CAT-scanner front ends. The op amp in the switched integrator is similar to those op amps. Special versions of the DIFETs are used for the switches in the ACF2101.

Rod Burt has also carefully controlled charge injection, the bane of most sampling amplifiers, to just one picocoulomb (pC) through careful layout and circuit design. Because the switches contribute equal and opposite charge for positive and negative transitions respectively, the total error due to charge transfer is determined by the switching sequence. For each switch, a logic transition results in a specific charge and an associated offset voltage. An opposite-going logic transition results in a charge (and offset voltage) of opposite polarity. Consequently, if the hold switch is turned on and off during one integration cycle, the charge transfer at the end of the sequence—and the offset voltage—is essentially zero.

The AFC2101 can operate from $\pm$15-V power-supply rails. However, because the output never has to go positive, it meets all of its specifications running off +5- and –15-V power supplies, dropping power dissipation in half. Cutting power dissipation lowers the die's temperature and thus the op amp's bias current. Maximum quiescent current (in either case) is 15 mA from the plus power-supply rail and 4 mA from the minus power-supply rail. Maximum output current is 5 mA.□

PRICE AND AVAILABILTY

The AFC2101 comes in 24-pin plastic DIPs and wide-body SOICs. Both meet their specifications from –40 to +85°C and operate to 125°C. In quantities of 1000, they run $16 each. Small quantities are available from stock. A low-cost evaluation board with timing and sampling-output circuits is available.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; John Conlon, 1-(800) 548-6132, or day and night via an electronic bulletin board at (602) 741-3978 (300/1200/2400 8,N,1). CIRCLE 514

HOW VALUABLE?	CIRCLE
HIGHLY	541
MODERATELY	542
SLIGHTLY	543

LOW-VOLTAGE, MICROPOWER OP AMPS COME OF AGE

THREE OP AMPS RUN OFF 2- TO 2.5-V RAILS—THEIR CURRENT DRAINS RANGE FROM 1.2 μA TO 700 μA; SLEW RATES RANGE FROM 3 TO 500 V/MS.

FRANK GOODENOUGH

When most major product innovations come on the scene, they're almost always described as bigger, faster, and more powerful. How about a new direction? Here are three op amps that offer less speed, lower power, and the ability to operate from lower-voltage supply rails. The CMOS MAX406 from Maxim Integrated Products Inc. has a maximum quiescent current of just 1.2 μA. Advanced Linear Devices (ALD) Inc. offers the CMOS quad ALD4706 that needs just 50 μA per op amp. And from Signetics Corp. comes the NE5234, a bipolar quad that can slew at 0.5 V/μs, while needing a huge 700 μA of quiescent current per op amp. All three op amps work with potentials of less than 2 V between their plus and minus power-supply pins, making them ideal for use in a variety of low-power applications.

The demand for battery-powered electronic equipment for industrial, medical, laboratory, telecommunications, and consumer applications is exploding. At the same time, high-performance digital circuits are moving to the long-talked-about 3.3-V CMOS and 2-V ECL power-supply rails. Today, battery-powered applications are crying for micropower linear devices that work off power-supply rails below 3 V. High-performance mixed-signal systems will soon be looking for them too.

Each of the three op amps is unique and fills its own application niche. In each case, its designer made trade-offs in performance to achieve the right operating current and voltage specifications *(see the table)*. In addition, each op amp has its own unique features that can't be compared by numbers alone. For example, the Maxim MAX406 op amp won't oscillate, regardless of load capacitance. The ALD4706 op amp from ALD is a standard cell in an ASIC library. And the output signal from the Signetics NE5234 op amp doesn't invert when the common-mode voltage (CMV) exceeds the power-supply rail.

Besides low-voltage operation, the three op amps have three other areas of commonality—all particularly valuable when powered by a low voltage. These are an input CMV range that can include the power-supply rails (or in the case of the NE5234 op amp exceed it); an output-voltage swing that can come very close to the power-supply rails at rated output current; and operation from a single power-supply line. A look at all three op amps also illustrates the dependence of speed, bandwidth, and output drive on quiescent current. By comparing the bandwidth ratios and the quiescent-current ratios of any pair of the three op amps, you'll find them amazingly similar.

TO BE OR NOT TO BE

No other true op amp approaches the MAX406 op-amp's minimum quiescent current of a mere 1.2 μA. Many op amps have bias currents greater than that. And with an open-loop gain of over 100 dB, it's a *true* op amp. Otherwise, it's strictly a dc device.

According to Maxim's Greg Schaffer, the IC's designer, the MAX406 op-amp's bandwidth is only 4 kHz. If more bandwidth is required and the op amp can operate at a noise gain of two or greater, pulling the MAX406's band-

MICROPOWER OP AMP TRIO

width pin high disconnects the compensation function, which pushes the device's gain-bandwidth product to 20 kHz. That's small signal bandwidth. Full-power bandwidth, however, which is based on slew rate, calculates out to about 250 Hz.

The op amp's gain is specified with a 1-MΩ load, but 1-MΩ loads are few and far between *(see the table, again)*. However, the op amp's output is a transconductance (Gm) stage (patent applied for), which drives current into the load. Gain is thus directly proportional to the load; while driving 10 kΩ, the op amp still has 60 dB left. Of course, if you use the MAX406 op amp to save battery power, a 1-V output across even a 100-kΩ load takes 10 times the op amp's current, so power savings from the low quiescent current are negligible. Some applications have high-resistance loads as the norm, such as the input to a CMOS ADC or a power MOSFET. Particularly important are applications that also take advantage of the op amp's very low bias current, typically less than 100 fA, and its ability to drive highly capacitive loads without oscillating.

The MAX406 op amp lends itself well for application in low-cost, portable pH meters. A pH-meter's probe looks like a 10^{12}-Ω 1400-mV voltage source. The probe wants to see a very high resistance. In typical applications, however, it often must drive a 3-1/2-digit integrating-type ADC load at the end of several feet of low-loss Teflon cable costing several dollars a foot. A MAX406 op amp connected as a follower circuit can be inserted in the probe with one 3-V lithium battery used for power, and the Teflon cable can be replaced with less-expensive coaxial cable.

The op amp can also be operated as a comparator circuit with its output normally at zero. When the output signal goes high, the op amp can source 100 μA of current to turn on a logic-level power FET and switch tens of amperes of current while running from a 5-V power-supply rail.

At just 500 μV, the MAX406 op amp also offers the lowest offset voltage of the three op amps at a temperature of 25°C and over temperature, and provides a pair of offset-nulling terminals as well. The other two op amps—the ALD4706 and the Signetics NE5234, being quads in the standard pinout, will require external circuits for offset adjustment. The two CMOS op amps (not usually famous for precision unless chopper stabilized) come in ahead of the bipolar device on offset-voltage and offset-drift specifications.

The ALD4706 op amp represents a good compromise between bandwidth (200 kHz) and quiescent current (50 μA per amplifier), while still offering the low bias current of a CMOS device. It too makes a good electrometer or transimpedance amplifier. In addition, unlike the MAX406 op amp, it provides typical specifications with ±1-V power-supply rails for open-loop gain, bandwidth, and slew rate. While open-loop gain drops in half with a 2-V supply voltage, slew rate and bandwidth remain unchanged.

Because the ALD4706 op amp can handle 12 V between its power-supply pins (the highest of the trio), and the output can source 200 μA while swinging to within 250 mV of both power-supply rails, it can put ±5 V across 25 kΩ. Running from a single 12-V power-supply rail, it can put 10 V across 50 kΩ. Alternatively, it can put ±2 V across 10 kΩ.

The device employs several nonconventional architectural twists, each of which provides operational features. The input stage uses both p- and n-channel FETs, essentially in parallel. As a result, the CMV can include both power-supply rails. It uses a three-stage amplifier to get the high gain. But its internal compensation circuit still provides a clean, single-pole roll-off with 70° of phase margin, and it can drive a 50-pF load without oscillation. It should make a good active filter except that noise isn't specified. The op amp is also a cell in ALD's analog CMOS standard-cell library, which includes other various op amps as well as comparators, timers, and other circuits—any or all of which can be put on an ASIC.

If cost is an issue, and/or you truly need speed or bandwidth at minimum power and noise, the NE5234 is the way to go. Not only does it have 2-MHz small-signal bandwidth, but its 0.5-V/μs slew rate translates into a full-power bandwidth of 35 kHz. A typical, total harmonic distortion of

MICROPOWER OP-AMP COMPARISON TABLE

Specification	MAX406A	ALD4706A	NE5234
Op amps/chip	1	4	4
Quiescent current per op amp (μA)	1.2	50	700
Operating-voltage range (V)	2-10	2-12	2-5.5
Open-loop gain (dB) (load)	106 (1 MΩ)	80 (100 kΩ)	90 (l kΩ)
Gain-bandwith product (kHz) Gain = +1 Gain = +2	 4 (compensated) 20 (uncompensated)	 200	 2000
Slew rate (V/μs) Gain = +1 Gain = +2	 0.003 (compensated) 0.012 (uncompensated)	 0.170 na	 0.500 na
Bias current (pA)	10 (< 0.1t)	20 (0.1t)	70,000
Offset voltage (mV)	0.5	2	4 (0.2 t)
Offset voltage over temperature (mV)	0.95	2.8	5
Output-voltage swing (V) (load)	±2.45 (1000 Ω)	2.25 (100 Ω)	±2.25 (600 Ω)
Input common-mode voltage range (V)	–2.5 to +1.4	–2.5 to +2.5	–2.75 to +2.75
Packages	8-pin DIP 8-pin SOIC	14-pin DIP 24-pin SOIC	14-pin DIP 14-pin SOIC
Price in 1000s	$4.25	$4.55	$1.45
Process	Silicon-gate CMOS	Silicon-gate CMOS	Oxide-isolated bipolar

(All specifications are maximums or minimums unless noted as t for typical. Specifications are for premium-grade commercial units operating at ±2.5 V and 25°C. na = not applicable).

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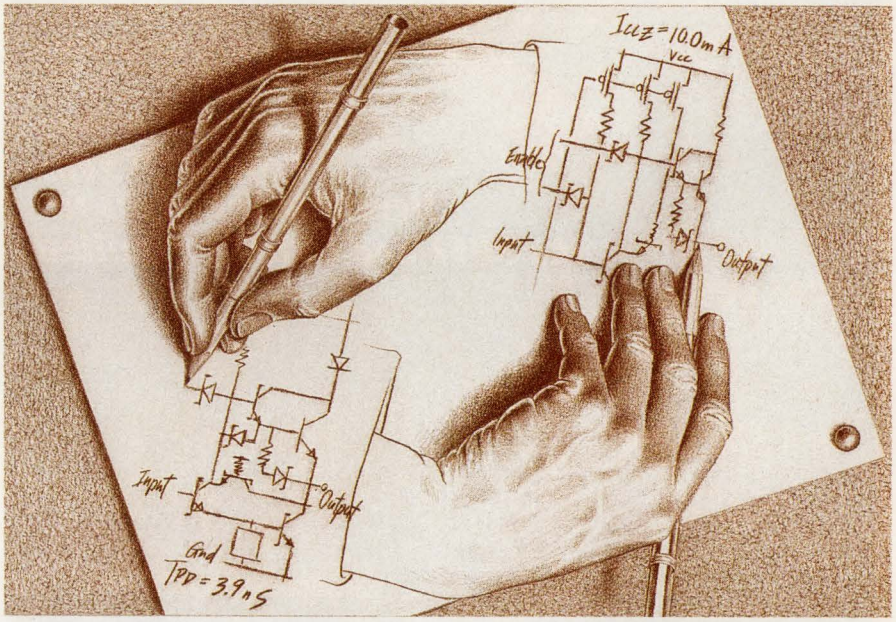

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EXTENDED AC ELECTRICAL CHARACTERISTICS							
Device	Symbol	T_A, V_{CC} = Comm					
		C_L = 50pF				C_L = 250pF	
		1 output switching		8 outputs switching			
		Min	Max	Min	Max	Min	Max
74FR244	t_{PLH}	1.0	**3.9**	1.0	4.8	2.3	7.0
	t_{PHL}	1.0	**3.9**	1.0	4.8	2.3	7.0
74BCT240	t_{PLH}	0.5	5.6	3.0	7.0	3.0	7.7
	t_{PHL}	0.4	4.0	1.5	6.5	1.5	5.0

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MICROPOWER OP AMP TRIO

0.1% is specified for a 1-V pk-pk, 10-kHz sine wave driving 10 kΩ. Thus, it handles audio signals nicely and could drive a small speaker. In fact, its output can source and sink at least 10 mA. All basic specifications hold for supply voltages from 2 to 5 V. Typical settling time to 1% is specified as 1.4 μs. Input voltage noise at 1 kHz typically runs 25 nV/$\sqrt{\text{Hz}}$, about 1/6 that of the MAX406.

While the NE5234's bias current may be excessive at 70 nA and 25°C relative to that of FETs, at 85°C it's still only 100 nA. If bias-current compensation circuitry is used, the increased error over temperature is very small. At a temperature of 85°C, bias current for the MAX406 op amp increases by a factor of 64 to 640 pA. At a temperature of 125°C, bias current is about 10 nA, a 1000-fold increase.

The NE5234's input circuit is similar to that of the ALD4706, except that pnp and npn bipolar-junction transistors replace the MOSFETs. The CMV can enclose the supply rails, and can also exceed both by 250 mV. In addition, unlike the 324 and many other IC op amps, the polarity/phase of the NE5234's output does not reverse/invert when the CMV exceeds the supply rails.□

Price And Availabilty

The MAX406 comes in two performance grades, each available for the commercial, extended-industrial, and military temperature ranges. The ALD4706 comes in three performance grades, each available for commercial and military-temperature ranges. The NE5234 comes in one performance grade that's available for commercial and extended-industrial temperature ranges. All are available from stock. See the table for 1000-piece pricing of premium-grade, commercial-temperature-range models in plastic DIPs.

Maxim Integrated Products Inc., 120 San Gabriel Dr., Sunnyvale, CA 94086; Steve Pratt, (408) 737-7600. **CIRCLE 511**

Advanced Linear Devices Inc., 1180F Miraloma Way, Sunnyvale, CA 94086-4606; Bob Chao, (408) 720-8737. **CIRCLE 512**

Signetics Corp., 811 E. Arques Ave., Sunnyvale, CA 94088-3409; John Lavery, (408) 991-4566. **CIRCLE 513**

How Valuable?	Circle
Highly	544
Moderately	545
Slightly	546

MICROCONTROLLERS DELIVER HIGH-END FEATURES WITH 8-BIT PRICES

DAVE BURSKY

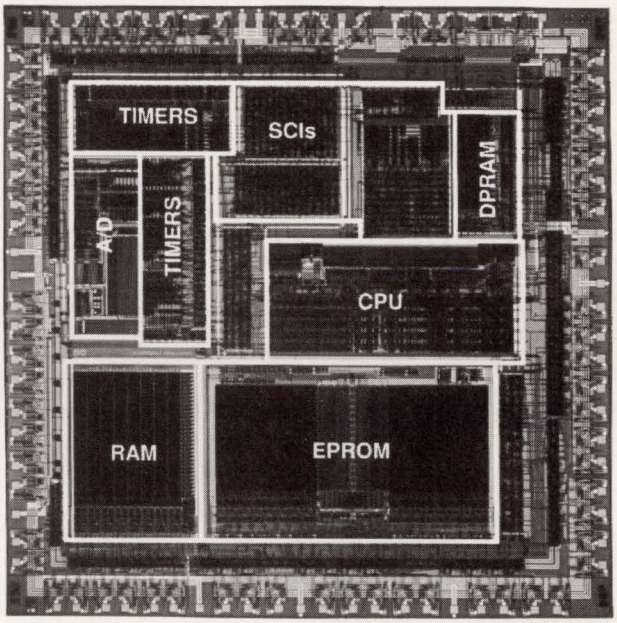
With over half-a-dozen models in its latest release of microcontrollers—the H8/300 family—Hitachi has unveiled processors that can handle most real-time control needs. The H8/300 series includes several general-purpose and a few application-targeted controllers. For general-purpose needs, the H8/330 can tackle high-end applications, while the H8/320 series aims at slightly less-demanding applications.

Four members in the 320 series—the 322, 323, 324, and 325—differ only in the amount of on-chip nonvolatile memory (8, 16, 24, and 32 kbytes, respectively, of ROM or EPROM). For servo-control applications, the H8/350 packs resources for head-positioning control in disk drives, and other applications requiring precision measurement and control. The H8/310, with 8 kbytes of electrically erasable memory, takes aim at smart-card applications.

All processors in the H8/300 family are based on an 8/16-bit core with a configurable register file that can be set as 16 8-bit words. All registers can also be treated as accumulators, making it easier for the core to execute compiled C code. There are 54 basic instructions in the core, and with a 10-MHz clock signal, the instructions take either 200 or 400 ns to execute.

The high-end 330 comes with 16 kbytes of one-time programmable EPROM, 512 bytes of RAM, 15 bytes of dual-port RAM, an on-chip 8-channel ADC with a sample-and-hold amplifier, and a RISC-like 8-bit CPU core that handles 8- and 16-bit operations. The chip also has abundant I/O resources—five timers, a full-duplex serial interface, and nine I/O ports (57 I/O lines plus 9 that are input only).

A masked-ROM version of the HD6473308CP6, the HD6433308CP6 microcontroller, is also available for high-volume requirements. Removing the ADC, some I/O lines, and adding a second serial port and a choice of 20 interrupt sources turns the 330 series of microcontrollers into the 320 series. The 320 series of microcontrollers can find a variety of homes in real-time control, office automation, and mobile-communications hardware.



For servo applications, the H8/350 adds more memory, more ADCs and DACs, and a waveform generator to control general-purpose I/O pins. As much as 32 kbytes of program or data can be stored in the on-chip UV EPROM.

Additional resources include 512 bytes of RAM, nine timers, a timer network, a pulse-width modulated DAC, a two-channel serial communication interface, a 16-channel ADC, and a large number of I/O lines (16 output only, 16 input only, and 50 bidirectional lines).

The timer network, when employed with the nine timers, allows software-programmable configurations, eliminating the need for external hardwiring typically employed for the timers. A masked-ROM version of the H8/300 microcontroller is also available.

With the largest on-chip EEPROM of any commercial microcontroller, the H8/310 should hold much interest to designers working in security - sensitive applications, from data security to inventory control and management. A Write/Erase Inhibit function prevents accidental EEPROM erasures. The processor also includes 10 kbytes of ROM, 256 bytes of RAM, and a 1-bit I/O pad. The 1-bit I/O line allows fast data transmission and can be a key element for contactless communications. Because the chip is aimed at smart-card applications, it will initially be offered as a bare chip.

Prices for the chips range from less than $10 each in large quantities for the H8/310 and less than $9 each for the 8-kbyte ROM-based H8/322, and increase to less than $15 each for the H8/350 and some of the larger ROM versions of the 320 series. One-time programmable versions of the 330 sell for $17.45 each in 100-unit lots, while the OTP version of the H8/350 will sell for $25 each in similar quantities. The 320-series microcontrollers come in 64-lead plastic shrink DIPs and plastic quad-sided flat packages. The 350 comes in 80-lead QFPs, or 84-lead PLCCs and LCCs. The H8/330 sells for $17.45 each in 100-unit lots, and is available in an 80-lead QPFP, an 84-contact leaded chip carrier, and an 84-lead PLCC. Delivery of samples for most of the controllers is from stock.

Hitachi America Ltd., Semiconductor and IC Div., 2000 Sierra Point Pkwy., Brisbane, CA 94005-1819; John Hull, (415) 589-8300

CIRCLE 300

FLASH-MEMORY DEVICES OPERATE AT 90 NS

Offering access times of 90 ns, the Am28F512 and Am28F256 flash-memory devices from Advanced Micro Devices hold 512 and 256 kbits of data, respectively. The devices' die sizes were reduced substantially using the company's 1.0-μm CMOS process. They're housed in 32-pin DIPs and PLCCs that allow users to easily upgrade to higher densities.

The chips support the de facto AMD/Intel standard for 12-V flash memories. The 512-kbit part is organized as 64 kbits by 8 bits, while the 256-kbit part is organized as 32 kbits by 8 bits.

AMD also offers a 90-ns, 2-Mbit flash device with automatic program and erase capabilities. The Am28F020 supports the company's embedded-erase and -program algorithms. The automatic erase function preprograms, erases, and verifies the device. The part then indicates to the system when it's ready for reprogramming. The automatic-program function indicates to the system on a byte-by-byte basis when the device is ready for the next byte of data.

The Am28F020 is backward-compatible with existing manual algorithms for 256-kbit, 512-kbit, and 1-Mbit flash memories. Hence, the 2-Mbit part can lower the chip count in existing 12-V flash designs. It's organized as 256 kbits by 8 bits.

All three parts are available now. The Am28F256 starts at $8.85, the Am28F512 at $10.80, and the Am28F020 at $44, all in 100s.

***Advanced Micro Devices Inc.**, 901 Thompson Pl., P.O. Box 3453, Sunnyvale, CA 94088; (408) 732-2400.* CIRCLE 301

■ *RICHARD NASS*

WIDE-WORD EPROM TARGETS LAPTOP BIOS

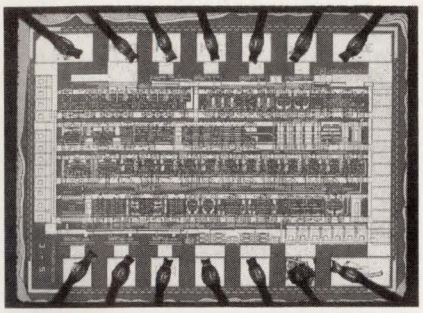
The AT32C16 512-kbit UV EPROM is one of the first sub-megabit EPROMs with a 16-bit-wide data output. By offering a 150-ns device with a 32-kword-by-16-bit configuration, Atmel is trying to replace the dual BIOS EPROMs typically used in most 16-bit 80286- and 80386SX-based PCs with one chip (or with two chips, the multiple EPROMs typically used in 32-bit systems). The chip, running at 5 MHz, consumes 30 mA maximum when powered by 5 V. On standby, it draws just 0.1 mA maximum. Programmable at 0.1 ms/word, the entire chip need only sit in the programmer for less than 4 seconds to be completely configured. Commercial- and industrial-temperature-range versions of the one-time programmable chip will be offered. Options include a 40-lead plastic DIP or a 44-contact plastic leaded chip carrier. In lots of 10,000, the commercial-grade PLCC version sells for $4 apiece. Delivery is from stock.

Atmel Corp., 2125 O'Nel Dr., San Jose, CA 95131; Steve Sharp, (408) 441-0311. CIRCLE 302

FREQUENCY SYNTHESIZER DELIVERS 50 TO 600 MHz

With a simple 10-to-20-MHz input crystal, the PCK 604 frequency synthesizer delivers a 50-to-600-MHz output frequency, phase locked to the input crystal. The chip solves tough clock-distribution issues in systems that require very-high-frequency timing signals. The on-chip phase-locked loop keeps noise jitter under 5% of the output frequency, or 0.25 ns worst case, whichever is greater. The company expects jitter to be much lower and plans to tighten the specification in the near future.

Two input-control signals determine one of four preset frequencies between 40 and 600 MHz. Only a few external components are needed for operation—a crystal, a resistor, and a capacitor. The first release of the PCK 604 will have preset frequency output values of 50, 100, 200, and 400 MHz with a 12.5-MHz input crystal. With an 18.75-MHz crystal, the output frequencies increase to 75, 150, 300, and 600 MHz. A capacitor can be substituted and connected across the crystal inputs. Output duty cycle is 50%, ±5%. Fabricated in gallium arsenide, the chip runs from



a 5-V TTL supply, or −5.2 V, or +2- and −3.2-V ECL supplies. It provides ECL 100K-compatible outputs.

The synthesizer consumes 200 mW and is available as a 14-pin DIP, a small-outline surface-mountable package, or as a bare chip. Outputs can also be three-stated, permitting users to stop the clock. In lots of 10,000, the bare chip sells for $16.59; the SO-package version costs less than $19. Bare chips are available immediately, with plastic-housed versions due in 6 to 8 weeks.

OnChip Systems Inc., *1190 Coleman Ave., San Jose, CA 95110-1105; Doug Curtis, (408) 988-5400.* **CIRCLE 303**

■ *DAVE BURSKY*

VGA CONTROLLER SIMPLIFIES LAPTOPS

By combining high integration to trim parts count and low-power CMOS to reduce standby power drain, the SPC8100 enables a complete VGA display subsystem to be implemented with just five components—the controller, two 64 kword-by-16-bit DRAMs, and two clock oscillators. The special CMOS process employed by S-MOS Systems allows four levels of power-down modes so that intelligent power-management features can be employed by the system.

The lowest of the power-down modes trips the power to just 1% of the chip's active power drain—about 1 W. The less-frugal modes leave different portions of the chip active. The system can thus return to the active mode faster. The three other modes drop the power to 2, 5, or 17% of the active level. All modes can be selected through a "hot" key setting or by software.

Along with the digital logic that performs the VGA control, the chip also contains the triple 6-bit digital-to-analog converters to drive the video display and the 256-word-by-18-bit color lookup table. The chip has interface logic that ties the controller into flat-panel displays with 640-by-480- or 720-by-480-pixel resolution with up to 16 levels of gray. It also contains PS/2 analog monitors, and multifrequency analog color or monochrome monitors. The SPC8100 provides EGA, VGA, and extended-resolution 800-by-600-pixel by 16-color display modes.

A 16-bit bus interface ties the chip into the local screen memory (up to 256 kbytes). And a selectable 8- or 16-bit interface ties the chip into the host PC. A single 144-lead plastic quad-sided flat package holds the chip. In 1000-unit lots, the chip sells for $60 each.

S-MOS Systems Inc., *2460 N. First St., San Jose, CA 95131; Robert Wong, (408) 922-0200.* **CIRCLE 304**

■ *DAVE BURSKY*

LOW-VOLTAGE EPROMS SOLVE PORTABLE NEEDS

One of the first families of UV EPROMs to be characterized for 3-to-5.5-V operation, the AT27LV256R, 512R, and 010R gives designers from 256 kbits to 1 Mbit of storage with a read access time of 300 ns when powered at 3 V. The low-voltage mode also keeps power consumption down: At 3.3 MHz and 3.3 V, the chips have active and standby power of just 26 and 0.33 mW, respectively. At 5.5 V, power consumption is 110 mW for any of the three chips when they're accessed at 5 MHz. Organized as 32-kwords-by-8-bits, 64-kwords-by-8-bits, and 128-kwords-by-8-bits, the EPROMs have CMOS- and TTL-compatible inputs and outputs and an integrated product-identification code for use by intelligent PROM programmers. Just 0.1 ms/byte is needed for programming—about 3.3, 6.5, or 1.3 seconds, respectively, for each chip. The chips come in various package options—one-time-programmable plastic DIPs, small-outline, or J-leaded chip carriers, reprogrammable windowed ceramic DIPs, or leadless chip carriers.

Atmel Corp., 2125 O'Nel Dr., San Jose, CA 95131; Steve Sharp, (408) 441-0311. **CIRCLE 305**

TV DISPLAY CONTROLLER HANDLES DIVERSE TASKS

Approaching a universal solution to control TV and video subsystems, the 83C053/87C054 MTV chip offers a full-featured text display. Based on an extended 80C51 8-bit processor core, the MTV controller contains an on-screen display module, display RAM and a character ROM, PWM outputs (eight 6 bit and one 14 bit), and a software-driven three-channel ADC. The chip can produce attractive, programmable, on-screen displays of characters and icons. This includes a 128-character free-format display with eight shadow modes; choice of character colors on a character-by-character basis; choice of background color or video; double-height, double-sized, and condensed characters; and underlining. The 83C053 has 8 kbytes of ROM; the 87C054 has 16 kbytes of one-time programmable EPROM. In 10,000-unit lots, the C053 sells for $6.25 each. The C054 goes for $17.00 each. Both come in 42-lead reduced-size plastic DIPs.

Philips Components, Signetics Co., 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; Mike Thompson, (408) 991-5207. **CIRCLE 306**

SOFTWARE DISPLAYS CUSTOM GRAPHICS

Unix users can develop and customize graphical displays without complex coding by employing Sammi, a graphical user environment (GUE). Sammi presents, organizes, manipulates, and interprets information interactively from multiple applications and databases, across many hardware and software platforms. The Sammi system consists of three components, a run-time environment, a format editor, and an application-programming interface. The run-time environment, which resides in the operating environment, handles the display, data communications, and end-user commands. Initial development copies, which are available now, range from $12,500 to $25,000, depending on configuration.

Kinesix, 10333 Richmond Ave., Suite 1100, Houston, TX 77042; (713) 953-8300. CIRCLE 307

TWO SOFTWARE TOOLS CREATE DSP CODE

Two new options for digital-signal-processing (DSP) code generation have been added to the Comdisco Signal Processing WorkSystem. First, the DSP ProCoder (DPC) option automatically produces production-quality code for fixed-point digital-signal-processing chips. DPC uses heuristic programming-techniques to convert a signal-flow diagram into assembly code optimized for speed, memory efficiency, and program structure. In addition, the MultiProx (MPX) option uses signal-flow block diagrams to create C programs for execution on multiple digital-signal-processing chips. With MPX, users can partition a block diagram into regions executed by separate processors. The tool then produces separate C programs for each processor. Both products will ship by the end of the year. DSP ProCoder and MultiProx cost $15,000 and $10,000, respectively.

Comdisco Systems Inc., 919 E. Hillsdale Blvd., Foster City, CA 94404; (415) 574-5800. CIRCLE 308

UPDATED DATABASE RUNS ON MORE COMPUTERS

Release 1.1 of the ObjectStore object-oriented database-management system (ODBMS) runs on DEC's DECstation, IBM's RS/6000, and Sun's Sun-3 and Sparcstation computers. ObjectStore is a distributed object-oriented database-management system based on the C++ programming language. New features of ObjectStore Release 1.1 include an interactive query facility for real-time access to information, faster local-mode processing, and faster short transactions. There's also a quicker collections-class library that's more flexible to program. ObjectStore Release 1.1, which is shipping now, is ideally suited for application developers who need to manage complex objects among workgroup-style applications in a networked, client-server environment. It's priced on a per-seat basis, ranging from $2000 to $6000. Run-time licensing is also available.

Object Design Inc., One New England Executive Park, Burlington, MA 01803; (617) 270-9797. CIRCLE 309

VAX VMS USERS CAN NOW REVERSE-ENGINEER

The reverse-engineering capabilities of Cadre's Teamwork/C Rev tool now extend beyond the C-language environment. VAX VMS users working with Fortran, Pascal, Basic, PL/1, Macro, and Bliss can now take advantage of the CASE tool. Teamwork/C Rev simplifies software maintenance, improves product quality, and simplifies the transition to the CASE tools. Using the tool, uses can browse through source code in languages supported by the VAX source-code analyzer (SCA) by selecting modules from the structure charts. VAX SCA is one of six tools in Digital's VAXset. The SCA libraries created include structural information about programs. Teamwork/C Rev extracts this information and produces structure charts in Teamwork's project environment. The new tool is fully integrated with Cadre's entire family of Teamwork products. Teamwork's open architecture enables users to work with the editor of their choice. Teamwork/C Rev for VAX VMS costs $7500 for the Teamwork/C Rev processor and $1000 per seat for the browsing capability. It is supported on VAX VMS systems running versions 5.2 and 5.3, while its SCA interface is supported with VAX SCA versions 3.1 and later.

Cadre Technologies Inc., 222 Richmond St., Providence, RI 02903; (401) 351-5950. CIRCLE 310

68040 VME SBC Bolsters Performance Using ASICs

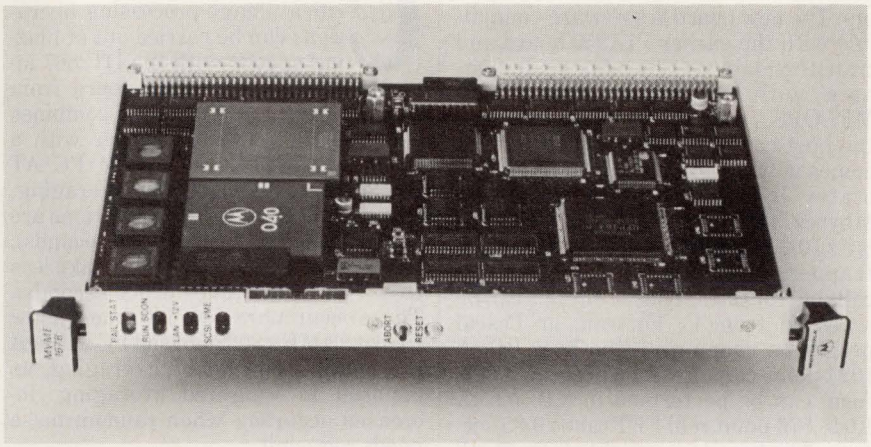
RICHARD NASS

The successor to Motorola's popular MC68030 - based MVME147 single-board computer (SBC) has arrived. The MVME167 is based on the newest member of the company's 68000 family of CISC microprocessors, the MC68040. The new board is built with an architecture that's nearly identical to Motorola's recently announced MVME187 board. The MVME187 is based on the company's MC88100 RISC processor. Both boards use the same advanced, third-generation ASIC and VLSI devices.

These intelligent ASIC controller chips, used for memory, networking, SCSI, VME, and serial and parallel communications, replace discrete circuitry and have been optimized for Unix and real-time applications. Motorola claims that the MVME167 offers users the fastest and most advanced SBC available for the huge installed base of 68000-based VME applications.

The MVME167 contains the processor, memory, and communications capabilities all on one board. And the board requires just one slot in a 6U form-factor enclosure. The only additional hardware that's needed is a power source, peripheral devices, and an enclosure. It's suitable for all types of workstations, multiuser systems, servers, industrial automation, and real-time and process-control applications. The board's programmable VMEbus interrupt handler further suits it for various real-time applications. The ASICs and VLSI devices are optimized to offload instructions from the 68040 processor and reduce the amount of unnecessary bus traffic.

The board achieves a performance level of 20 MIPS due to its 25-MHz 68040 processor, based on Dhrystone 1.1 measurements. With a selling price of $3995, the price-performance ratio is below $200/MIPS. Motorola says that the 167 board is selling for $1000 less than the 147 at its introduction.



The MVME167 has an optimized VME D64-compatible interface that's capable of transferring data at a rate of 40 Mbytes/s. The total power consumption of the board is 15 to 18 W under typical conditions. Motorola says that this is one-third to one-half the power that's consumed by similar SBCs. The board is capable of handling from 4 to 32 Mbytes of four-way interleaved DRAM, 8 kbytes of nonvolatile RAM for a time-of-day clock with a battery, and 128 kbytes of static RAM. Four sockets each hold 512 kbytes of ROM, EPROM, and EEPROM each, for a total of 2 Mbytes.

Motorola claims the board is faster and more integrated than other 68040-based SBCs. Many other 68040 boards are essentially 68030 designs containing a 68040 processor. Therefore, many of the peripherals used for Ethernet, SCSI, etc., are second-generation parts. Motorola designed the MVME167 as a 68040 from the ground up with all third-generation parts. "There's aboslutely nothing on the MVME167 board that was on the MVME147 board," says Jerry Gipper, product marketing manager for VMEbus boards at Motorola. The company used a 32-bit Intel Ethernet controller and a 32-bit NCR SCSI coprocessor.

The board's high integration comes from using high-capacity VLSI controllers and ASICs. Its VMEbus interface is a 299-pin ASIC comprised of 120,000 gates. This chip contains a DMA controller, local and global interrupt handlers, and timers for periodic interrupts, in addition to the VMEbus interface. There are a total of six ASICs on the board. The second ASIC is a peripheral controller (glue-logic part). The other four chips are used for memory control.

All SCSI peripherals, such as disk and tape drives, are handled through the on-board SCSI interface that supports direct memory access between the SCSI bus and the local memory. The SCSI device-driver firmware is updated through software, allowing the SCSI Device Library to be quickly updated. This feature comes in handy when adding new peripherals. In addition, there's a direct 32-bit Ethernet controller that fully supports such protocols as TCP/IP, NFS, and DECnet. The board comes with one parallel port for a printer or other parallel I/O operations, and four RS-232 serial ports.

The MVME167 board comes with diagnostic software. It supports VMEexec real-time development software. Sample quantities will be available in July. Volume shipments are expected in November.

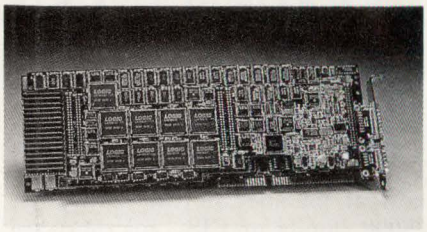
Motorola Computer Group, 2900 South Diablo Way, Tempe, AZ 85282; (800) 624-8999 extension 230. **CIRCLE 311**

PROCESSOR BOARD OPERATES AT 25 MFLOPS

Designed as an upgrade to an earlier board, the PL2500 floating-point array processor runs on ISA-based computers. The new board is software-compatible with the earlier PL1250 board and transfers data six times faster. It operates with a performance of 25 MFLOPS, transfers data to and from the host computer at 3 Mbytes/s, and comes with a minimum of 256 kbytes of static RAM, upgradable to 4.25 Mbytes. The heart of the PL2500 board is its 50,000 lines of code stored in ROM. It appears to the user as a library of 598 callable routines. These routines can be accessed from C, Fortran, or Pascal programs running on the host PC. A 1024-point complex fast Fourier transform can be performed in 3.13 ms. A 1,048,576-point real FFT takes 9.35 seconds. The board is available from stock for $2495.

Eighteen Eight Laboratories, 1247 Tamarisk Ln., Boulder City, NV 89005; (800) 888-1119. CIRCLE 312

PC/AT IMAGE PROCESSOR WORKS IN REAL TIME



Critical image-processing operations can be carried out at blazing speeds with the DT2867 integrated image-processor board from Data Translation. The board combines a high-quality frame grabber with a frame processor on one IBM PC/AT board. Histograms, frame averaging, and arithmetic and logic operations are carried out in real time (0.033 seconds); convolutions and morphology take less than two frame times (0.066 seconds). These occur more than 100 times faster than a 33-MHz 80386-based PC without the board. True frame averaging, as opposed to weighted averaging, increases accuracy when random noise needs reducing.

The board processes up to three pixels simultaneously through three parallel processing paths. Each path contains its own ALU and multiplier to achieve an overall processing rate of 75 MHz. However, the processor board doesn't sacrifice accuracy for speed. All processing using the three ALUs is done with 16-bit accuracy, ensuring that data isn't truncated during mathematical operations. The board contains a 16-bit processing buffer with 1 Mbyte of memory to handle the processed data.

The DT2867 is supported by several levels of software. A Windows 3.0 application software package is available for powerful analysis that doesn't require any programming. For advanced users, two levels of development software ship with the board. An interface library allows high-level control of the board's hardware functions, and a command builder and driver supply register-level control. The board, shipping now, sells for $6995.

Data Translation, *100 Locke Dr., Marlboro, MA 01752; (508) 481-3700.* CIRCLE 313

■ *RICHARD NASS*

286-BASED CPU MODULE MEASURES 3.6 BY 3.8 IN.

Based on Advanced Micro Devices' Am286LX CMOS microprocessor, the CoreModule/286 cpu module fits all of the functionality of a PC/AT motherboard into a module with dimensions of just 3.6 by 3.8 in.

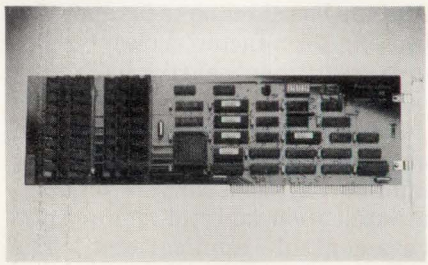
Like its predecessor, the CoreModule/XT, the 286-based version is targeted at embedded and dedicated applications where small size and low power consumption (2.25 W typical) are required. Its modular architecture enables it to serve as a component-like AT engine mounted on a pc board or combined with an expansion module to build a complete system.

The CoreModule/XT cpu module operates over a temperature range of 0 to 70°C. It comes with AT-compatible DMA controllers, interrupt controllers, and sockets for up to 4 Mbytes of DRAM.

The board costs under $200 in large quantities and will be available in September.

Ampro Computers Inc., 990 Almanor Ave., Sunnyvale, CA 94086; (408) 522-2100. CIRCLE 314

MEMORY BOARD CORRECTS ERRORS



To improve the reliability of PC/ATs and compatibles in standalone or network applications, the Parity+Plus memory boards contain built-in error-detection and correction (EDAC). EDAC protects against soft-error-induced system crashes on-the-fly by correcting bit errors. Without the board, users must shut down the system and reboot, possibly losing valuable data. The boards are available now. With 2 Mbytes of memory, the Parity+Plus board costs $295. It's also available with 4, 8, or 16 Mbytes of memory.

Memrel Corp., 15425 N. Greenway-Hayden Loop, Suite A-100, Scottsdale, AZ 85260; (602) 483-1983. CIRCLE 315

SPARC GRADUATES TO SUPERCOMPUTER LEVEL

The Sparc RISC processor is moving out of the workstation class of computers up to the supercomputer level in a new family of systems developed by FPS Computing. The 500 Series Sparc family offers an Integrated Homogeneous Supercomputer environment that teams scalar 64-bit, 15-ns Sparc processors with vector and parallel Matrix processors. This pushes the systems' performance to 13.4 GFLOPS and 533 MIPS. The supercomputers process scalar portions of application code using up to eight Sparc processors running in parallel.

The computers are the result of an agreement between FPS and Sun Microsystems Inc., Mountain View, Calif. FPS is licensing much Sun technology, including the SunOS operating system, Sparc compilers for Fortran and C, the Open Look graphical user interface, and Open Network Computing protocols. FPS has merged SunOS into its FPX implementation of Unix.

The systems can be linked as servers in networks with Sun Sparcstations. In this configuration, the FPS machine executes an application's computationally intensive tasks while the Sun systems do pre- and post-processing and display the supercomputer's output.

Up to 1 Gbyte of main memory can be housed within the systems. The computers are also designed with up to seven VME subsystems to ease I/O bottlenecks. Ethernet, FDDI, and UltraNet systems can run over the VMEbus. For math-intensive applications, the systems use up to 168 Intel i860 RISC processors as math coprocessors.

Because it's Sparc-compliant, the family has access to over 2800 existing applications, and consists of five members with different amounts of memory and varying numbers of CPUs. Low-end systems can be upgraded by adding CPUs and memory. They range from $450,000 to $4 million.

FPS Computing Inc., *3601 SW Murray Blvd., Beaverton, OR 97005; (503) 641-3151.* **CIRCLE 316**

■ *RICHARD NASS*

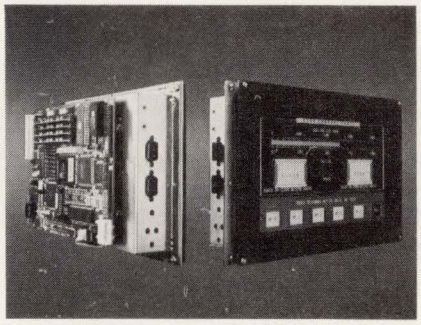
HIGH-END FAMILY GAINS TWO MEMBERS

The AViiON RISC-based family of high-performance systems has two new members, the 7000 and the 8000. The 8000 is a 117-MIPS rack-mounted system that's configured with a 24-Gbyte disk-array subsystem and the DG/UX 5.4 Unix operating system. It can support eight local-area networks and 1275 asynchronous terminals. The model 7000 is a deskside package that also operates at 117 MIPS. It comes with an uninterruptible power supply that initiates a controlled shutdown when extended power interruptions occur. The system comes standard with 128 Mbytes of main memory, expandable to 512 Mbytes. The systems start at $96,000.

Data General Corp., 4400 Computer Dr., Westboro, MA 01580; (508) 366-8911. **CIRCLE 317**

TOUCHSCREEN 386-BASED SYSTEM ADDS EL DISPLAY

One sturdy compact package houses an electroluminescent (EL) display, a 20-MHz 80386 PC/AT computer, and a touch-screen interface. The Display-

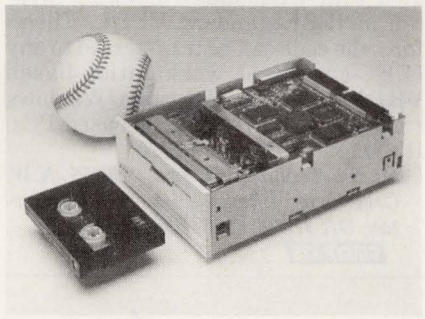


Pac-EL's bright amber EL display has a resolution of 640 by 400 pixels that can be read from an angle of 160 degrees. The computer offers the full complement of PC/AT functions. It comes with 16 Mbytes of DRAM, 1 Mbyte of EPROM, speaker and keyboard ports, two serial ports, a real-time clock, and hard- and floppy-disk interfaces. The board can be booted from its RAM-ROM disk that also stores MS-DOS. Different expansion and configuration options are available. Functions can be added through the PC-bus expansion slots. Prices start at $2195 in OEM quantities. Delivery is stock to 30 days.

Computer Dynamics Inc., 107 S. Main St., Greer, SC 29650; (803) 877-8700. **CIRCLE 318**

DIGITAL 4-MM TAPE DRIVE TRANSFERS DATA FASTER

Forsaking mass-produced 4-mm digital audio-tape drives made by consumer stereo firms, R-Byte has developed a high-reliability mechanism for a family of high-performance 4-mm digital data drives. The RB100 family will start with a drive whose sustained data-transfer rate is



233 kbytes/s—almost 50% higher than that of drives using the audio-tape mechanism. Closed-loop servomotor control speeds up rewind time for a 60-m tape to just 15 seconds—one-third the time of most other DAT drives.

A typical 60-m DAT tape holds 1.34 Gbytes, while the just-released 90-m tapes hold 2.01 Gbytes. The drive performs search operations at 200 times the read/write speed. Error rates are less than 10^{-15} thanks to an embedded 16-bit processor that continually checks and adjusts drive parameters to keep the drive running at like-new specifications. On-line monitors check for dew, mechanism jams, write-current level, memory faults, and error-checking and correction statistics. An RS-232 interface is included.

The low power drain and the elimination of the 20 to 50 adjustments also lets the drive operate over a wider temperature range—5 to 60°C versus about 45°C maximum for the audio drives. With the custom mechanism, the drive can squeeze into a true 3.5-in. disk-drive form factor—1.62-by-4-by-5.75-in. The RB100 will be available in sample quantities in July. Prices for the digital DAT drive start at $975 in lots of 250 or more (with 256 kbytes of buffer RAM).

R-Byte Corp., *2043 Zanker Rd., San Jose, CA 95131; Gerald Boudreau, (408) 452-8860.* **CIRCLE 319**

■ *DAVE BURSKY*

VHDL TOOLS RUN UNDER WINDOWS 3.0

V-System/Windows is a VHDL development system for use on PCs running Windows 3.0. The system includes a VHDL compiler, an interactive digital simulator, and a VHDL source-language debugger. The tools use extended memory to handle designs of 50,000 lines of VHDL code. Designs can be written at the behavioral, RTL, or structural level, or a mixture of all three. With the V-System interactive debugger, users can set breakpoints directly in the VHDL source code, single-step, and perform many other debug functions. In addition, any design created with V-System/Windows is written in IEEE-standard VHDL. Therefore, the code can be transferred to any IEEE-compliant workstation-based VHDL simulator. V-System/Windows runs on 286-, 386-, and 486-based PCs. It's shipping now for $1495.

Model Technology Inc., 15455 N.W. Greenbrier Pkwy., Suite 210, Beaverton, OR 97006; (508) 690-6838.

CIRCLE 320

ASIC, PCB TOOLS UNITE WITHIN FRAMEWORK

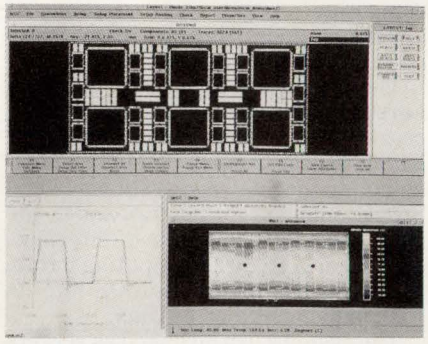
The first two elements of the Racal-Redac Visula Expert design system, ASIC Expert and System Expert, are now shipping. The tools run under the company's Vision framework, an inter-tool communication and project-management environment based on object-oriented programming. The third element of the system, Visula CAD Expert, is scheduled to ship this summer. Key product suites within the Expert series include an improved Cadat-2000 simulator and SilcSyn with VHDL synthesis. ASIC Expert handles complex ASICs through a top-down methodology. The System Expert handles pc-board design through logic, timing, and fault simulation; mixed analog-digital simulation; hardware modeling; schematic editing; and programmable-logic tools. The Visula Expert series runs on various Unix workstations. Pricing of the product suites start at $25,000.

Racal-Redac, 1000 Wyckoff Ave., Mahwah, N.J. 07430; (201) 848-8000. CIRCLE 321

TOOL SUITE TARGETS MCM DESIGN

A design system from Mentor Graphics called MCM Station is tailored to the creation of multichip modules (MCMs), electronic packages that combine bare multiple-chip die on one substrate. The system is integrated into the company's Falcon Framework for concurrent design.

MCM Station supports the entire



multichip-module design process, including rules-driven placement and routing, thermal and electrical analysis, and manufacturing interfaces. Mentor's AutoTherm software is used for thermal analysis. It's a finite-element-based tool for static and dynamic modeling of heat flow and dissipation. The system also incorporates the Quad Design Technology software to analyze high-speed signal delay, electrical crosstalk, and transmission-line effects. In addition, MCM Station provides full compliance with military documentation standards.

The system accepts chip and ASIC designs from various sources, including Mentor's Design Architect schematic-capture software. The design can then be simulated and analyzed. After that, MCM Station can transfer a completed multichip-module design to manufacturing in common file formats, such as GDSII and Gerber artwork outputs. It will also output designs in standard drill and milling formats.

MCM Station is available now. Pricing begins at $128,900 for the physical-layout, thermal-analysis, and signal-integrity-analysis tools.

Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 97070; (503) 626-7000. CIRCLE 322

■ *LISA MALINIAK*

HANDHELD METERS BOAST ADVANCED FEATURES

Three new handheld multimeters and enhanced versions of five existing models make up the 70 Series II family. Features that were once optional are now standard in the upgraded models.

Two new units, the 79 and 29, make up the high end of the series (the 29 version is designed for high-energy applications). These meters measure capacitance from 10 pF to 9999 μF, eliminating the need for a dedicated capacitance tester. In addition, they have a function called Smoothing, which displays the running average of eight readings so that stable readings are possible even with unstable signals. A proprietary Lo-ohms feature supplies 0.01-Ω resolution with high noise rejection to sense very small resistance changes.

The 79 and 29 also display frequency and voltage simultaneously. Frequency, from 1 Hz to 20 kHz, is shown on the digital display, while ac voltage registers on a new 63-segment analog bargraph. The bar-graph's rapid update rate simulates an analog needle for watching trends, peaking, and nulling.

The lowest-priced meter in the series is the new model 70, which measures ac

and dc voltage and ohms, and checks diodes and continuity. Although it has no current inputs, a 300-mV function allows a variety of current, temperature, and high-voltage accessories to be used.

All of the 70 Series II meters now include the patented Touch Hold feature, which captures and holds stable measurements. The feature enhances convenience and safety by letting the meters hold consecutive stable readings without manual resetting. Other features include autoranging, range hold, and optimal manual ranging.

The model 70 costs $69, and the models 79 and 29 are priced at $185.

***John Fluke Mfg. Co.** P.O. Box 9090, Everett, WA 98206-9090; (206) 347-6100.* CIRCLE 323

■ *JOHN NOVELLINO*

EMULATOR COVERS COP8 EMBEDDED CONTROLLERS

A 10-MHz PC-based emulator supports every unique feature of the National Semiconductor COP8 family of 8-bit embedded controllers. The iceMaster-COP8 includes a state-of-the-art windowed environment. Users can set up windows for code memory, source, RAM, watch, stack, system status, and registers. Multiple windows can be opened for RAM and code. Both simple and complex breakpoints and trace points can be set symbolically. Simple breakpoints are based on the program counter or its ranges. Complex breakpoints can depend on op-code values or class, reads or writes, registers, direct byte or bit, immediate operands, or logical AND/OR of any of these values. The iceMaster-COP8 base units costs $3099 and the probe cards for the particular COP8 devices start at $799.

Metalink Corp., P.O. Box 1329, Chandler, AZ 85244-1329; (602) 296-0797. CIRCLE 324

MICROWAVE COUNTERS ALSO MEASURE POWER

A pair of portable frequency counters make simultaneous frequency and power measurements on microwave signals, eliminating the need for a separate power meter. The Model 25B spans 950 MHz to 20 GHz; the 28B extends the upper limit to 26.5 GHz. Both units offer inputs to measure IF or baseband frequencies to as low as 10 Hz. Resolution is 1 Hz and 0.1 dB. With the standard timebase, frequency accuracy is better than 1 kHz for a 10-GHz signal. An optional ovenized timebase improves accuracy by 100 times. Power-measurement accuracy is typically ±0.5 dB. A 25-MHz YIG-preselector lets users limit measurements to a selected signal or channel. The EIP 25B costs $4650 and the EIP 28B goes for $5650. Delivery is in 2 weeks. GPIB programmability is optional.

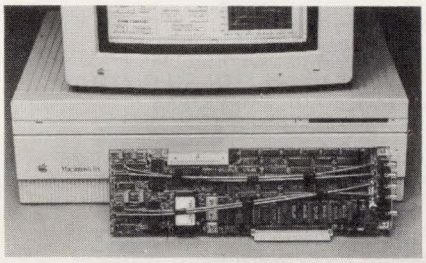
EIP Microwave Inc, 1589 Centre Point Dr., Milpitas, CA 95035; (800) 232-3471 or (408) 945-1477. CIRCLE 325

IC TESTER AIMS AT TTL AND CMOS DEVICES

In-circuit and out-of-circuit tests on digital ICs can be performed by the Pro-Line Model PL 5010. The tester's device library covers more than 90% of existing 14- to 28-pin ICs, including over 600 commonly used TTL and CMOS ICs. The library is updated as new devices become available. The microprocessor-based instrument can operate alone or connect to an IBM PC through an enhanced RS-232 port. With the PC and optional software, users can create custom-device libraries. A loop-test function helps the PL 5010 find intermittent failures by continuously testing a device until a failure is encountered. In addition, an auto-ID function identifies unknown devices by comparing their responses to those in the library. The PL 5010 is available immediately for $4500.

B&K-Precision, Maxtec International Corp., 6470 W. Cortland St., Chicago, IL 60635; (312) 889-1448. CIRCLE 326

MAC II BOARDS HANDLE AUDIO-ANALYSIS TASKS



A series of three 4-channel analog-input plug-in boards aim at specific audio-frequency applications on Macintosh II computers. The NB-A2150C samples at rates used for general audio-range analysis. The NB-A2150S is optimized for speech and voice-band measurements. The NB-A2150F is ideal for applications needing standard sampling rates for Fourier analysis. All of the units have analog and real-time digital antialiasing filters, 93-dB signal-to-noise ratio, and –95-dB total harmonic distortion. Amplitude flatness is within ±0.015 dB from dc to 20 kHz in the C and F models. That bandwidth is narrowed to dc to 4 kHz for the voice-band-oriented S model. The 16-bit analog inputs feature synchronized simultaneous sampling. All versions are available now at a price of $1995.

National Instruments, 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100. CIRCLE 327

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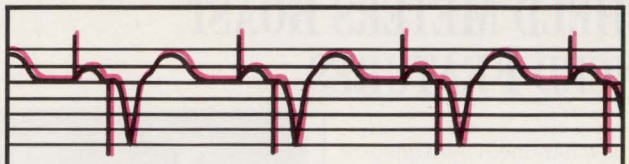

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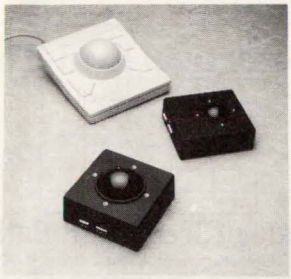

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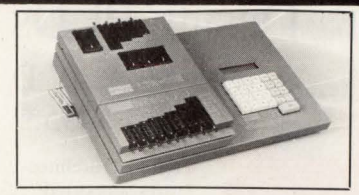

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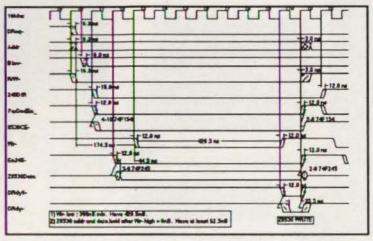

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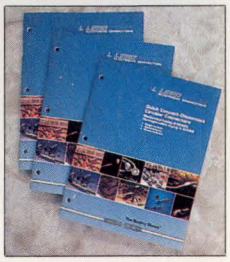

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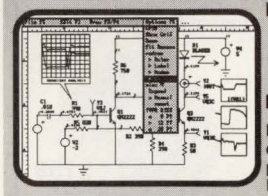

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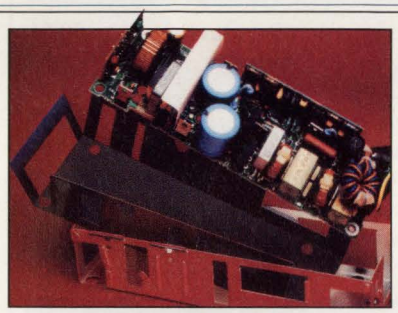

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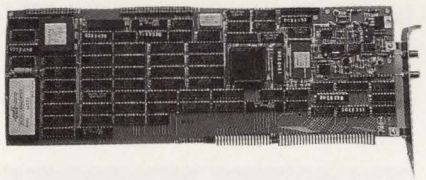

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- Programs **EE/EProms, Flash Eproms, ZPRams, Intel Micros, Memory Cards.**
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INTELLIGENT ROM EMULATOR $395
- Emulates **2716** through **27512** EProms with a single unit. **Access time 120ns.**
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- **Address Compare with Halt output, Address Snapshot, Trigger input.**
- **Fast data loading via parallel printer port (64k bytes in less than 10 sec).**
- **Cascadable up to 8 units.**Includes target cable with Trigger/Reset/Halt clips.
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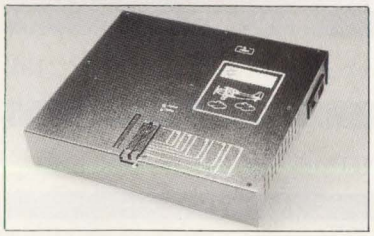

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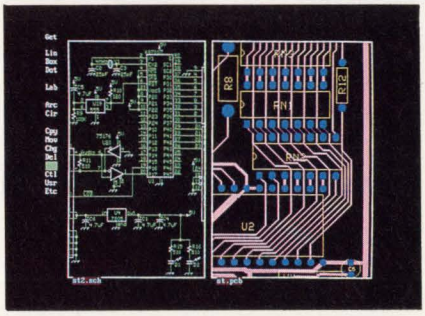

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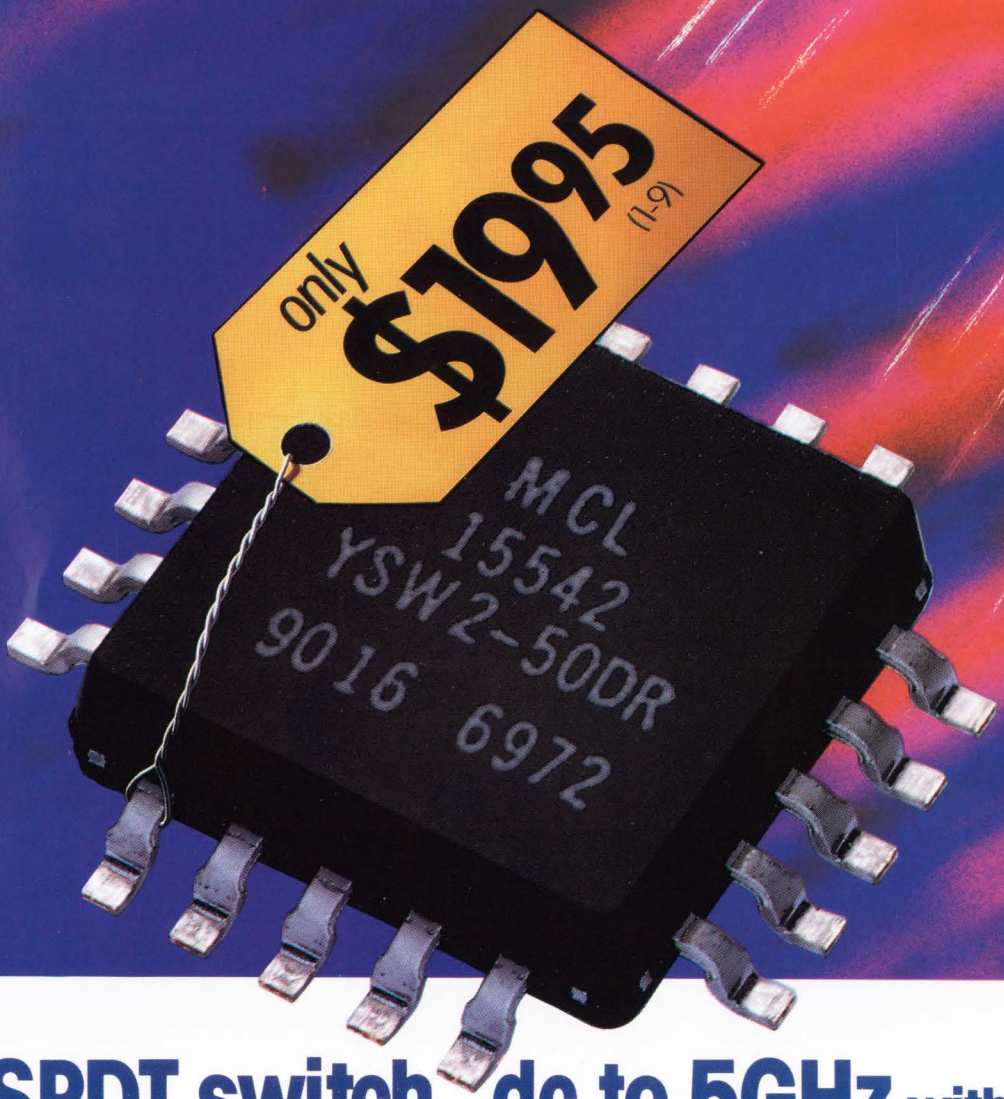

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isolation, typ(dB)*	50	40	28
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Rise/Fall time, max (nsec)		3.0	

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