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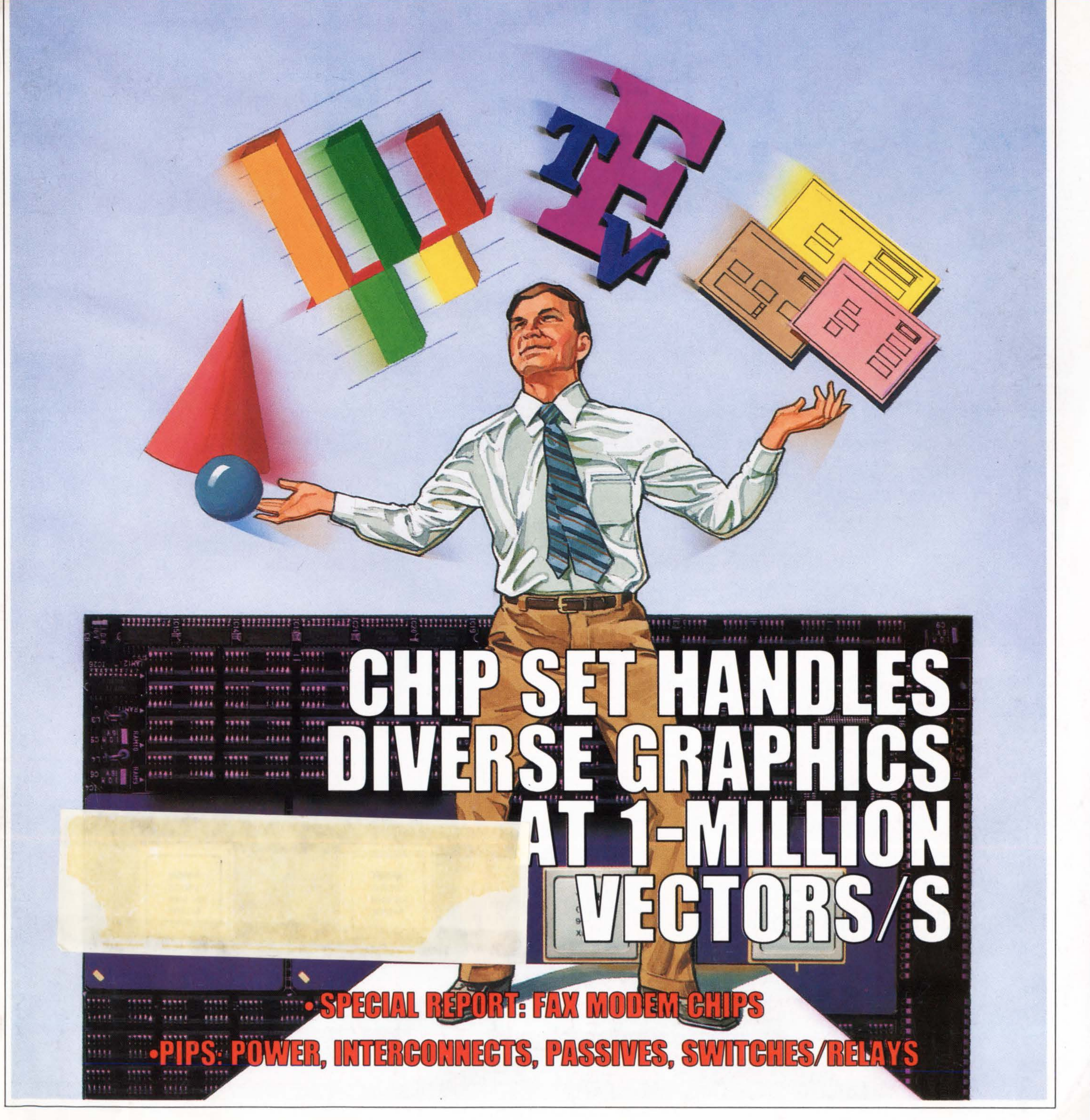

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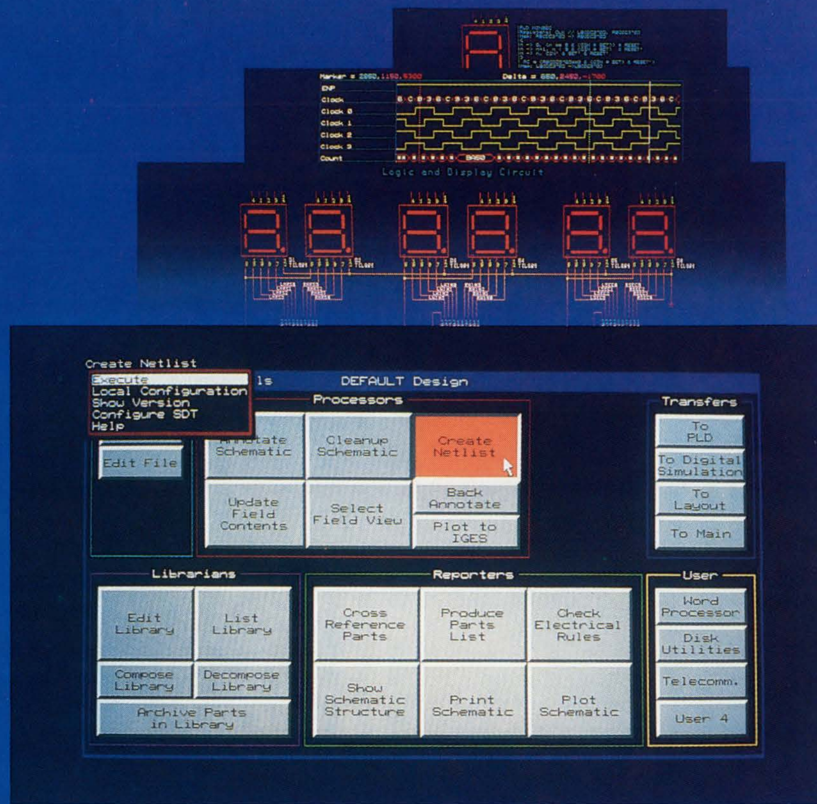

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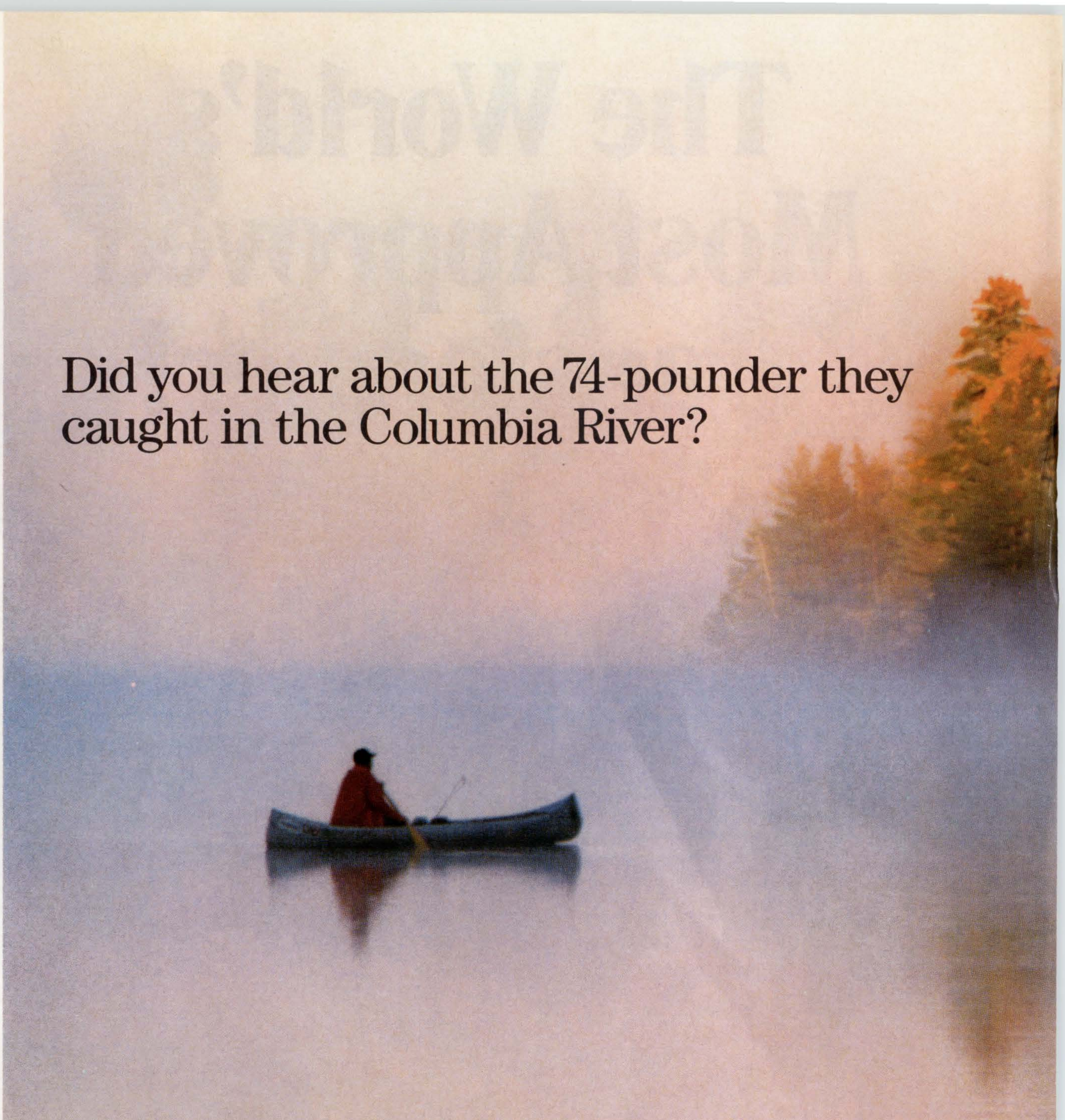
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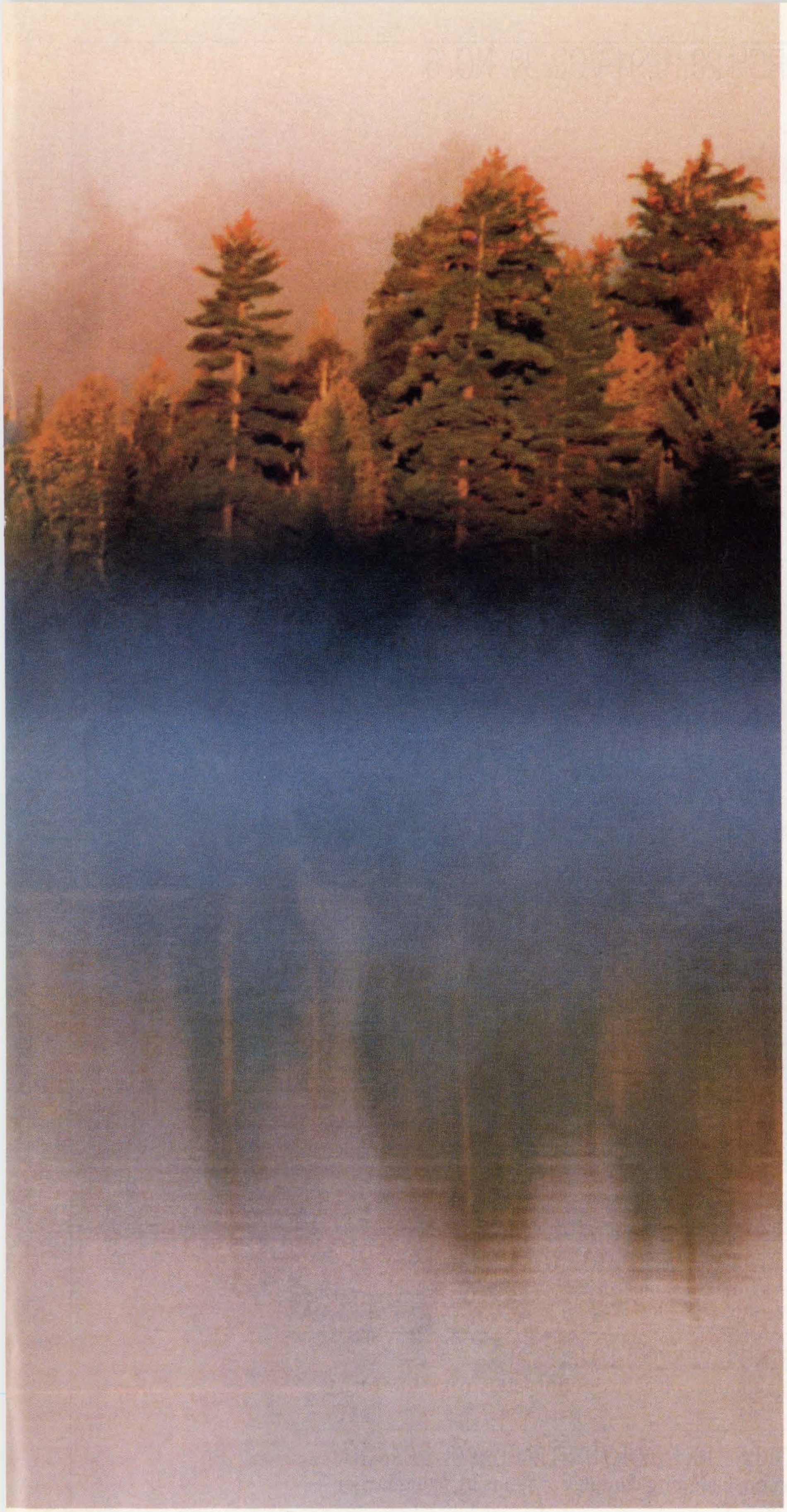

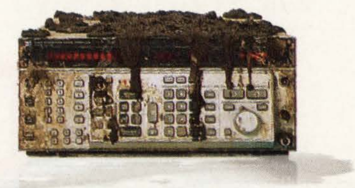

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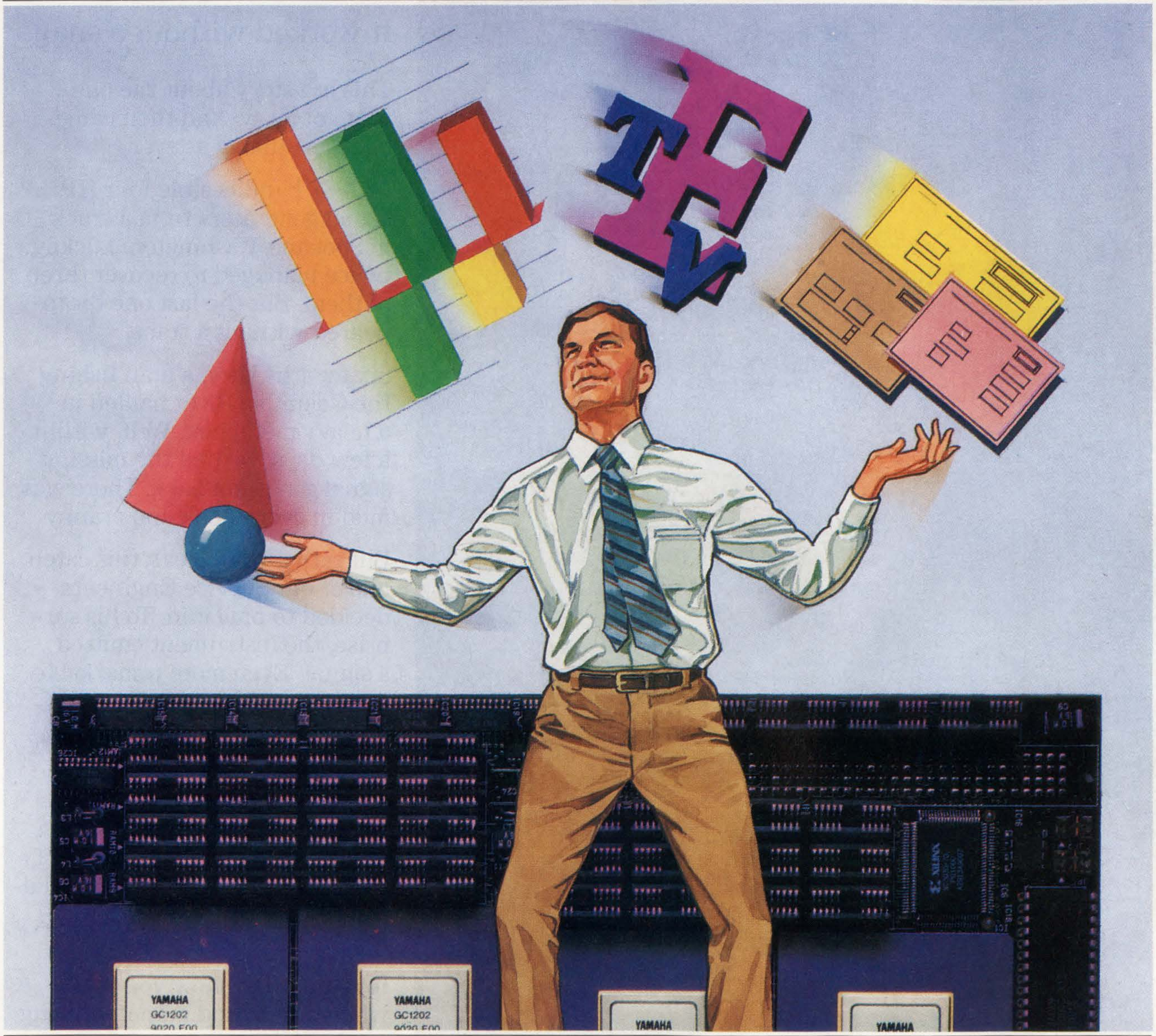

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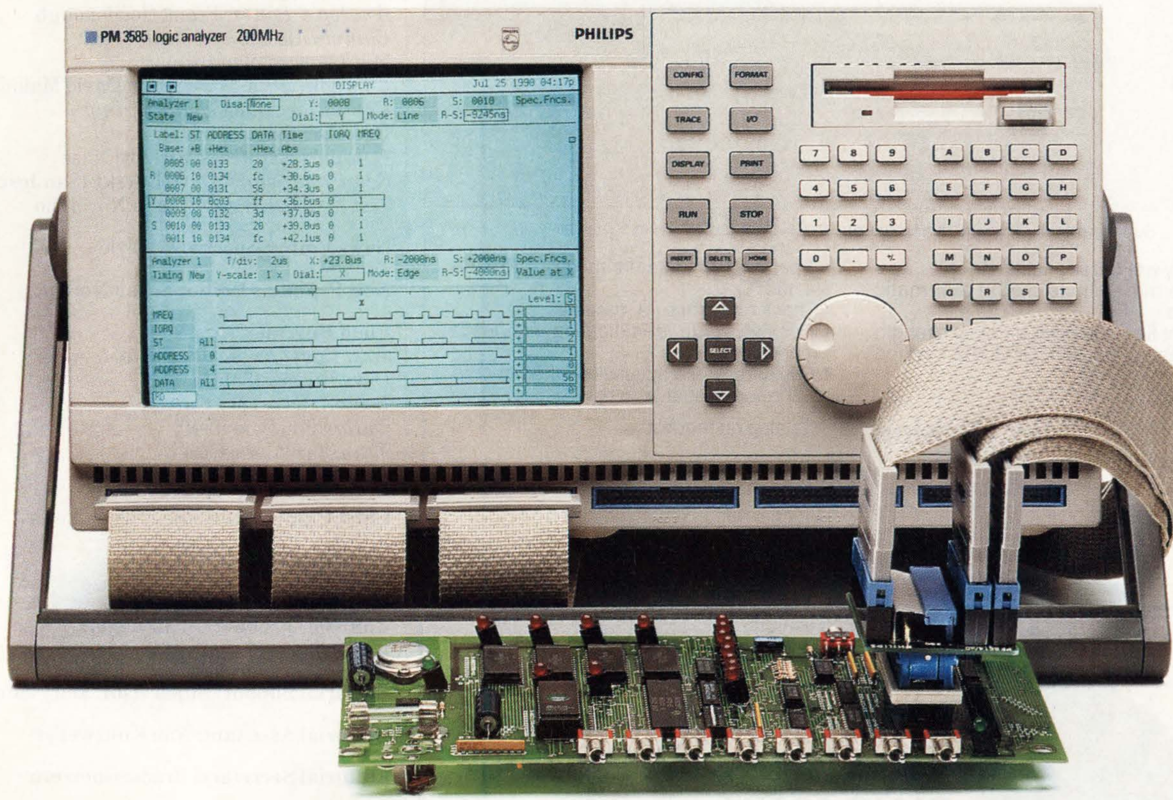

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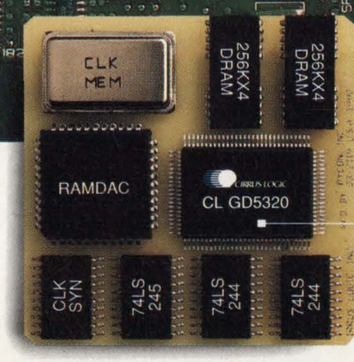

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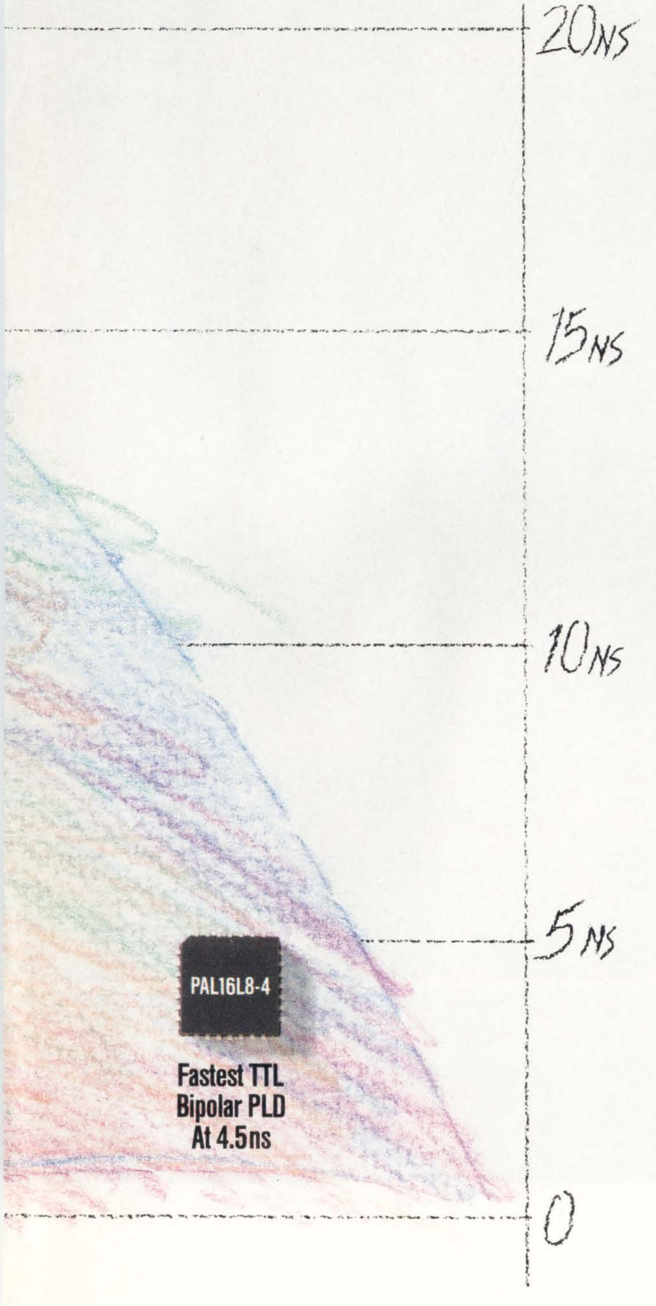

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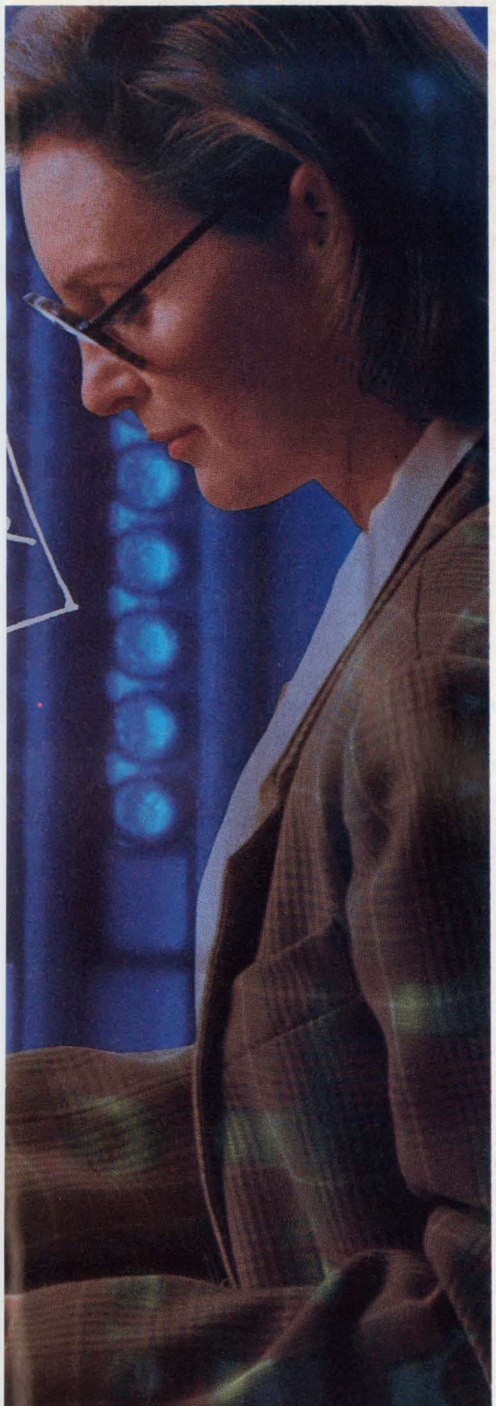

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THE INNOVATIONS LIVE ON

Creativity and drive are two of the most important attributes an engineer can have in electronic design or any other field. It's the impetus behind every development and facet of design. When Robert J. Widlar died on February 27, the electronic community lost an engineer who embodied these qualities.

Widlar, one of the industry's best known creative geniuses, never gave up in his pursuit for perfection. He carved the many paths the linear circuit industry has taken today. Nearly all of the devices he designed over 20 years ago are still as appropriate for today's designs as they were when first introduced. Some of Bob's notable devices most familiar to linear-IC engineers include the μA709, LM100, LM101, LM102, LM108, LM109, LM111, LM10, and LT1016, among many others.

Widlar's accomplishments are ground-breaking. He was the first to use the multicollector pnp transistor, which is used in virtually all linear ICs today. He invented super-gain transistors, now available in operational amplifiers industry-wide. Bob also developed the bandgap reference, which was first used in the LM109 power IC regulator and later in voltage references. His innovative circuit-design techniques formed the basis of many devices over the next 25 years and became part of school curriculums.

His linear-IC career began with Fairchild Semiconductor, and then he moved on to National Semiconductor, where he persevered for a number of years before retiring. Not one to sit still, though, Widlar soon came back onto the scene as an independent contractor. Later, he joined the start-up team at Linear Technology, helping in the company's initial stages and contributing to many of its products.

As one of the most renowned characters in Silicon Valley, many Bob Widlar stories are in circulation, and most of them are true. He was a person who lived life to the fullest and never did anything by halves. Known to use unconventional methods, he frequently held interviews in bars, with the press as well as with prospective employees. Bob Widlar was not one to have died bedridden. He led an active life and died in the same manner, running on the beach in Puerta Vallarta, Mexico.

Robert Dobkin
Vice President, Engineering
Linear Technology Corp.
Milpitas, Calif.

Editor's Note: Bob Dobkin, a close friend and associate of Bob Widlar, worked with Widlar at National Semiconductor for several years during his most creative period. Because of Dobkin's long association with Widlar, Electronic Design believes he is the most appropriate person in the electronics industry to reflect on Widlar's accomplishments.

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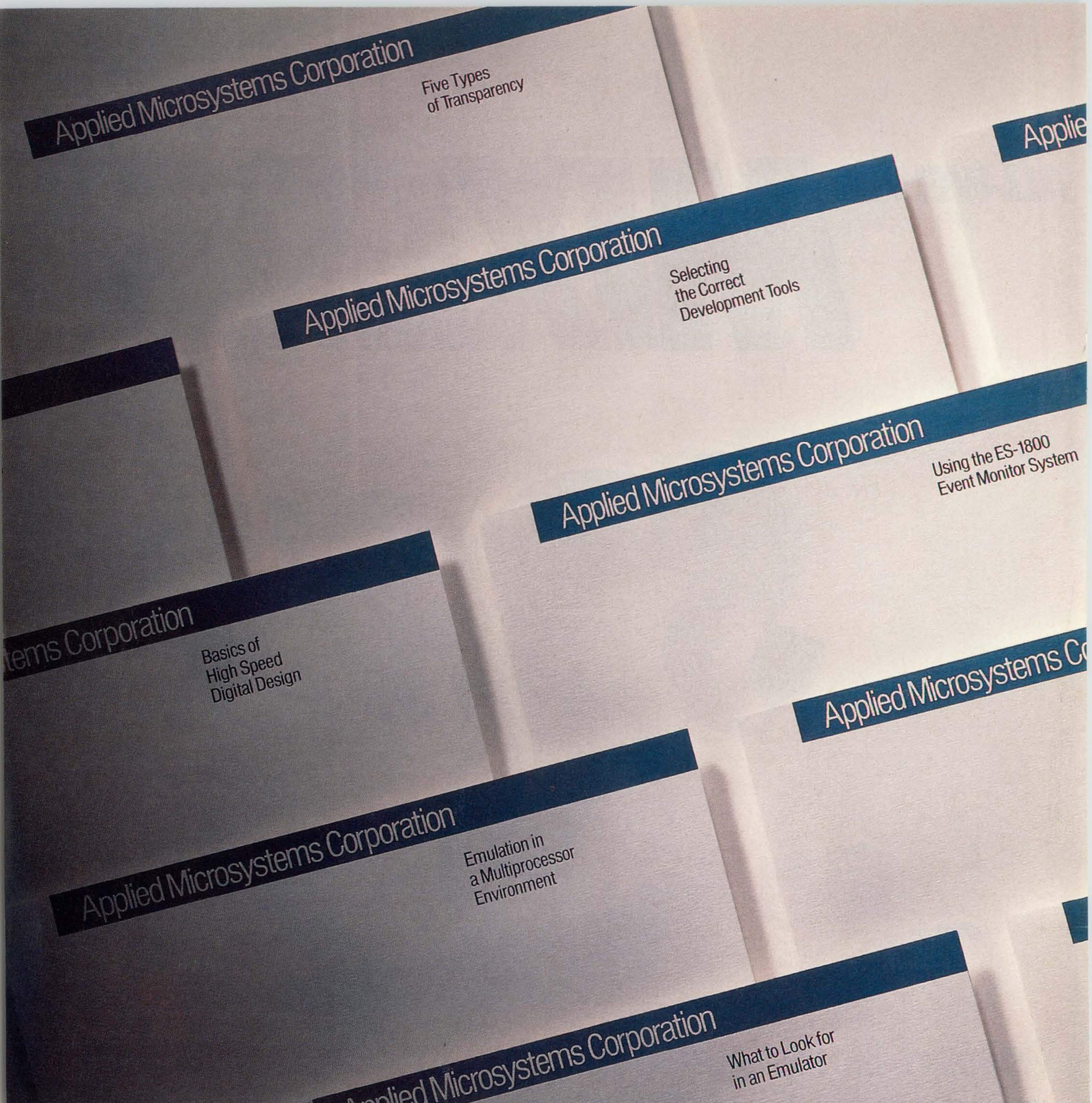
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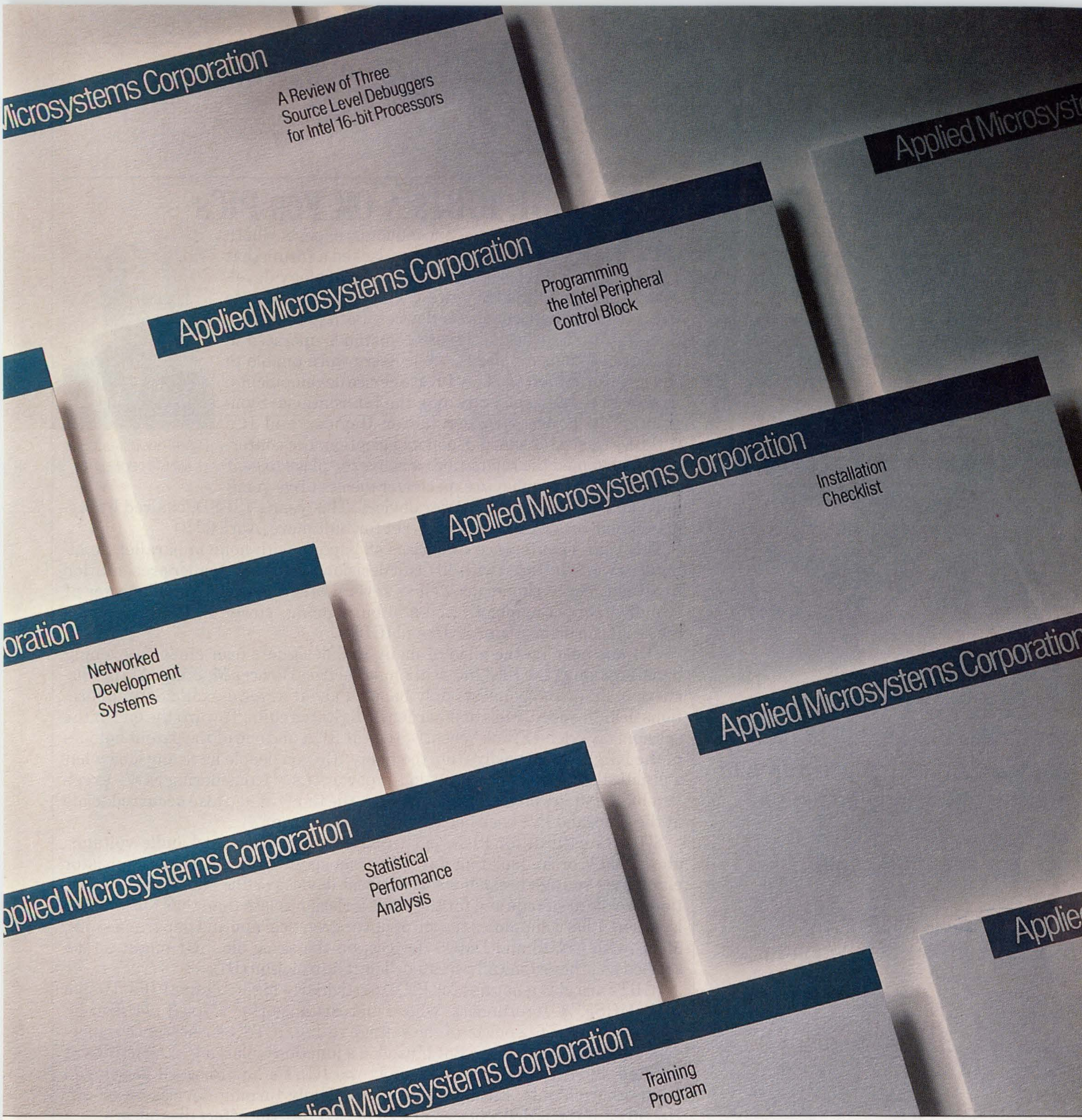

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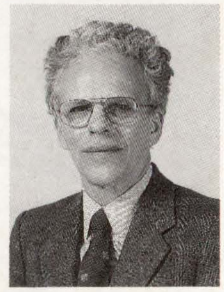
CIRCLE 147

ISPSD: SOI, IGBTs A-OK For PICs


FRANK GOODENOUGH
ANALOG & POWER

For years, power semiconductor experts—both device designers and users—lacked a forum that digs into problems and future technology developments in high-power, high-voltage discrete and integrated semiconductor devices. Both groups have thus suffered: device designers sometimes operated in the dark as to users' needs, while users were unable to collect information on likely future device developments. However, a couple of years ago, the International Symposium on Power Semiconductor Devices and ICs (ISPSD) was established. Upon its inception, the conference has gained the reputation as being *the* place to be if you want to learn what to expect over the next five years in IC and discrete silicon power devices. This year's ISPSD, chaired by Ayman Shibib of AT&T Bell Labs, is set for Baltimore, April 22-24.

This year's conference comprises 48 papers, with none in parallel, so attendees won't be faced with difficult decisions as to which paper presentation to attend. Three papers (as well as several others) highlight the merger of two diverse, yet symbiotic and still burgeoning, power IC (PIC) technologies—silicon on insulator (SOI) and IGBTs.

SOI has been on the mind of many PIC designers ever since an evening panel session at the 1983 International Electron Devices Meeting. At this discussion, all of the panelists only bandied about several exotic SOI applications in high-speed, radiation-hardened digital circuits. Toward the end of the session, my friend Frank Wheatly, then of RCA and one of the patent holders of the IGBT, asked boldly from the floor, "Do you people have any idea what a practical SOI technology can do for power ICs?" (considering SOI's excellent high-voltage insulating capabilities, the thought had also occurred to me at the time, and I've been hooked on SOI ever since).

SOI is a natural for PICs, particularly those that must handle voltages above 100 V or so. Isolating any given transistor from any other transistor eliminates voltage breakdown to adjacent devices or the substrate. In addition, the die area required for the oxide isolation is less than that for junction isolation. Plus it simplifies the job of putting vertical npn and pnp transistors, along with CMOS and DMOS devices, on the same die. SOI might be described as lithographically created dielectric isolation (DI).

IGBTs are also a natural for PICs, particularly high-voltage PICs. Unlike their MOSFET forerunners, whose on-resistance (for a fixed die size) increases with the 5/2 power of the voltage rating, IGBT on-resistance is independent of voltage rating. But if used in a junction-isolated IC, the hordes of injected minority carriers that supply the IGBT's low forward losses will flood other circuits, raising havoc by randomly turning devices on or off. However, if the IGBT is placed in a DI or SOI tub, the effect disappears.

Three upcoming ISPSD papers describe these technology mergers. The first, from device designers at Philips Laboratories, Briarcliff Manor, N.Y., describes a process for building 800-V devices on SOI for future 700-V lateral MOSFETs and IGBTs. The second paper, presented by researchers from Purdue University, West Lafayette, Ind., details an SOI process in which small-signal devices are built in an epitaxial layer. Power devices, such as IGBTs, are built in deep, oxide-lined trenches etched through the epi into the substrate. The third paper, from the Hitachi Research Laboratory, Ibaraki, Japan, describes a motor-control IC with a 600-V, 25-A, vertical IGBT output device that goes through the chip from top to bottom. Its upper portion, and the chip's small-signal devices, are in oxide-lined tubs embedded in polysilicon. The IGBT's lower portion is in direct contact with the polysilicon.

For conference details, contact Annmarie Pittman, Courtesy Associates, 655 15th St. N.W., Washington, D.C. 20005. Call (202) 639-4917.

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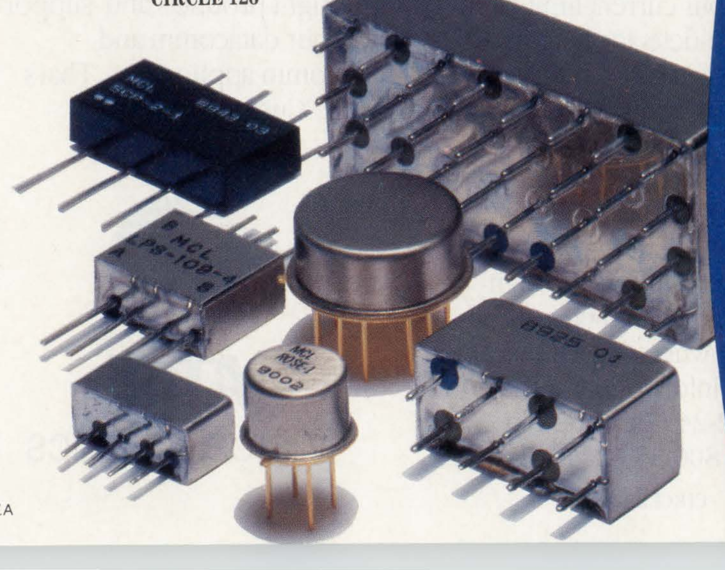

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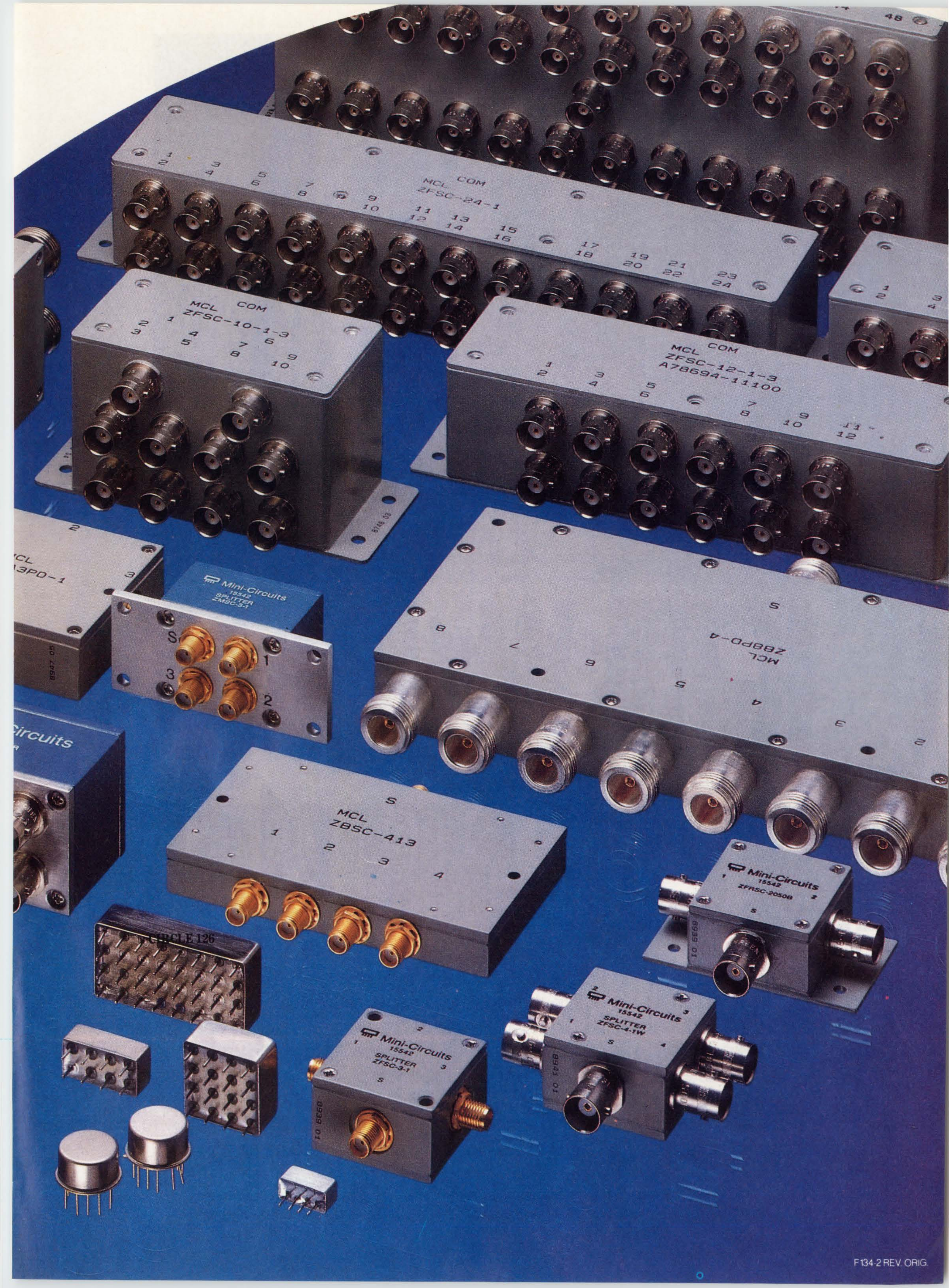

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HIGH-TEMP PROCESS MAKES SUPERCONDUCTORS

A reproducible process has been developed to manufacture Josephson junctions from a high-temperature ceramic superconductor. The process allows the fabrication of more than 50 double-junction superconducting quantum interference devices (Squids) that can operate at the relatively high temperature of liquid nitrogen, which is –196°C. The process, developed by Biomagnetic Technologies, San Diego, Calif., could lend itself to large-scale production and is the subject of a patent application submitted by the company. Tests to determine and optimize the process' characteristics will continue over the next several months. *DM*

EDAC STRESSES THE BENEFITS OF STANDARDS

Electronic Design Automation Companies (EDAC) will teach designers how to use standards to their advantage during a tutorial they're giving at the Idea Exposition, April 2-4 at the San Jose Convention Center. The tutorial, titled "Utilization of standards for wise development and selection of EDA tools," will cover why standards are important for users, tool developers, and workstation vendors, and will include discussion of specific standards. In addition, the speaker will supply a list of questions that EDA-tool buyers are recommended to ask of tool suppliers to make intelligent purchases. Mitch Weaver of Mentor Graphics, Beaverton, Ore., will be the primary speaker. *LM*

SBUS BACKED AS EXPANSION STANDARD

The 64-bit SBus has received an endorsement as the bus standard for expansion modules on pending Futurebus+ modules. Motorola Inc., Tempe, Ariz., announced that it will use the SBus—an open, high-performance modular I/O interconnect architecture developed by Sun Microsystems Inc., Mountain View, Calif. Motorola's Computer Group contends that SBus' growth and flexibility, combined with the large number of SBus products already in use, makes this bus the ideal choice for expansion modules. These expansion modules are used for high-performance I/O applications, such as system memory, peripheral controllers, coprocessors, networking, and graphics controllers. The modules offer specialized functionality that augments the CPU board. Because Futurebus+ is also an open standard, Motorola and Sun believe the expansion bus should be nonproprietary. Specifications for the SBus can be obtained by calling (408) 395-9522. *RN*

TINY 20-PIN PACKAGE SHRINKS CIRCUITRY

By occupying just one-third the board space of small-outline large (SOL) packages, the shrink small-outline package (SSOP) becomes the smallest commercially available 20-pin package for portable-communications devices. Used by Signetics Co., Sunnyvale, Calif., to house its NE/SA575 DK compandor and NE SA605DK/615DK FM IF mixer system, the package measures 1.5 by 4.5 by 6.75 mm. In addition to its small footprint, the package is thinner than the SOL package, which gives it an advantage in space-sensitive situations. Call Michael Sera at (408) 991-4544. *DM*

ANALOG PCB PACKAGE DOES FRONT-TO-BACK DESIGN

By leveraging a framework to mesh two analog-design packages, Valid Logic Inc., San Jose, Calif., created the first front-to-back environment for analog board design. The Analog Systems Lab (A/S Lab) consists of the company's Analog Workbench II analog-design system and release 5.0 of its Allegro pc-board system. Together, they furnish analog designers with in-process analysis, electrical design, and physical design. Valid claims that A/S Lab is the first package to account for the large amount of electrical and physical interdependencies in analog boards. In addition, recent enhancements to the Allegro product address unique needs of analog boards. For instance, the software supports the use of curved traces and intelligent shapes with curved boundaries to minimize signal discontinuity and maximize signal-to-noise ratios. A/S Lab will be shipping in May for $45,000. Call (508) 256-2300 for more details. *LM*

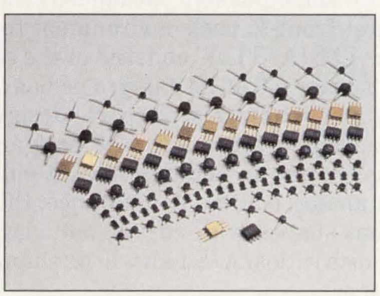
TEXAS INSTRUMENTS JOINS MULTICHIP TEAM

Texas Instruments, Dallas, has joined the Open Systems Project of the Microelectronics and Computer Technology Corp. (MCC), Austin, Texas. The project focuses its efforts on developing an industry infrastructure for multichip-module technology. TI becomes the twelfth participant in the project, which was launched in March, 1990. Its goal is to offer members a competitive advantage of one to two years by bringing low-cost, 40-MHz-plus systems to the market. *DM*

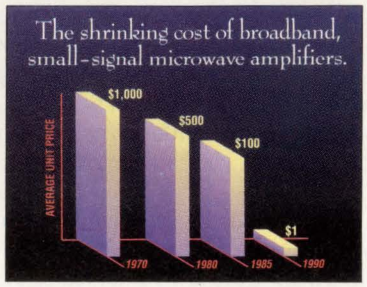
Why the cost of harnessing lofty technology is much less predatory these days.

Ancient falconers were the first to see the potential of harnessing high-flying technology. By the 1970's, microwave wizards had performed technical feats far beyond what ancient man could imagine. Yet, the most sweeping breakthroughs are emerging now, at Avantek.

Avantek is bringing the lofty cost of microwave technology down to earth, with a new generation of low-cost microwave components. In a word, our technology is going *plastic* —for high volume applications. Now, a wide range of high-performance MMICs and devices Avantek set the standards for are available in plastic and surface mount packages. This advanced microwave technology is also integrated into a variety of cost-effective components.



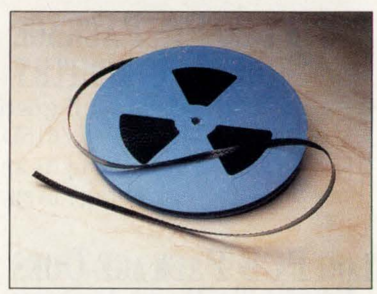
Avantek's broadband microwave amplifiers sell for as little as $1.00 each.



Avantek produces thousands of off-the-shelf products for the cellular telephone, sat com, fiber optics, data com, navigation, and telecom markets. We continue to break price/performance barriers with innovative products—silicon & GaAs semiconductors, LNAs, high power amplifiers, upconverters, downconverters, laser drivers and multiplexer/demultiplexers—for many high volume applications.

We also help customers hold down manufacturing costs in other ways. We offer the microwave industry's most extensive service and distribution network with twenty major stocking locations worldwide. So we can keep pace with the most demanding JIT programs. Or swiftly supply critical components for a single prototype. Or deliver a wide range of off-the-shelf components, often within 24 hours.

Making microwave history is part of Avantek's 25-year tradition. Today, we have an unsurpassed capability for RF and microwave products. As the world's leading manufacturer of commercial power amplifiers, GaAs & silicon transistors and MMICs for the cellular telephone, VSAT an DBS markets, we know how to meet demanding standards of cost, delivery and quality. Tomorrow this capability will enable us to meet the needs of new markets such as GPS and high frequency automotive electronics.



Avantek supplies microwave components in 7" and 13" tape and reel packaging for high-volume pick and place manufacturing.

For more information about how Avantek's new technologies can help your business thrive in the most predatory marketplace, call:

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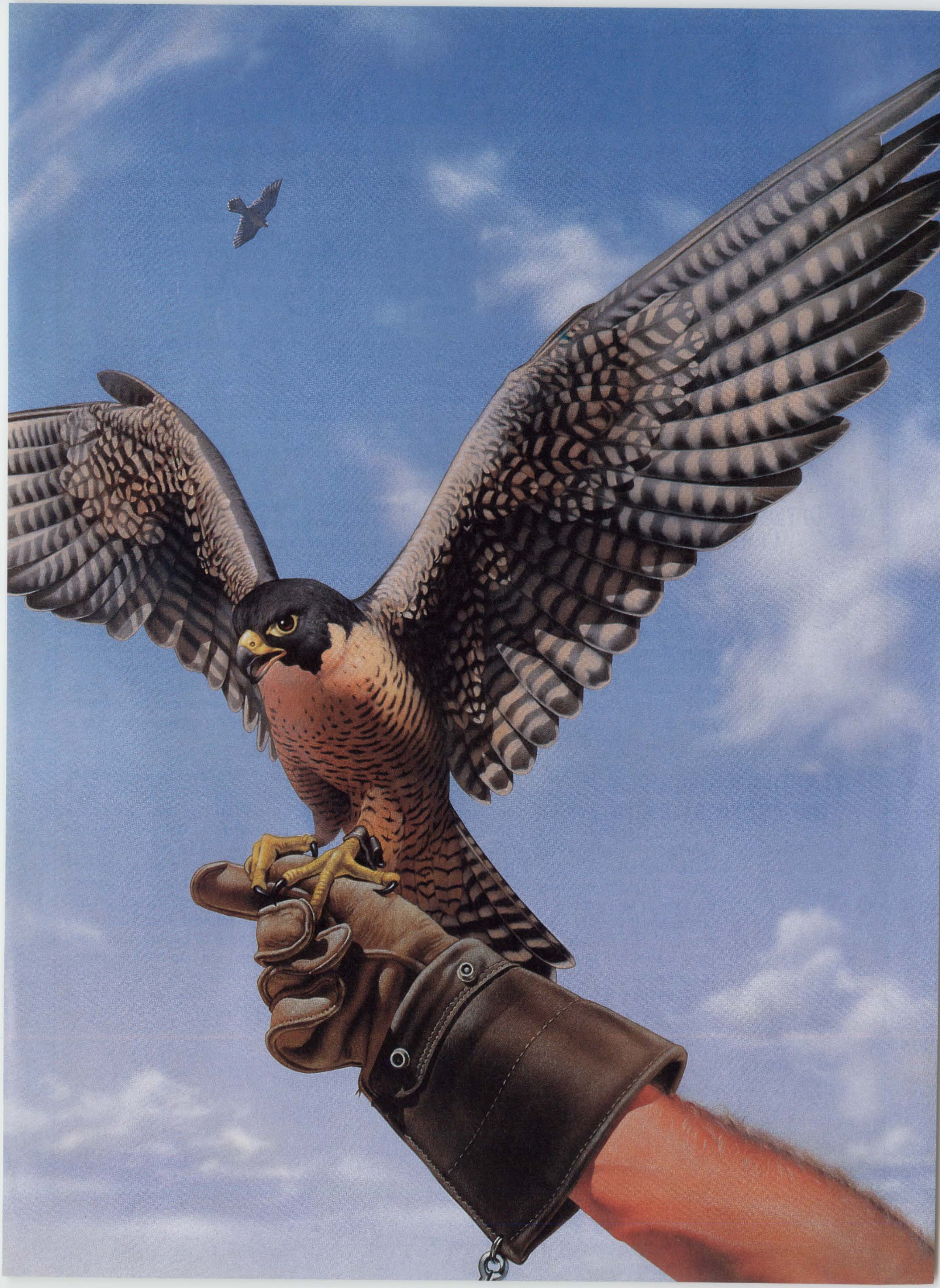
Putting microwave technology to work for you.

CIRCLE 154



HIGH-ENERGY SUPPRESSOR PROTECTS CIRCUITRY

A significant departure from conventional silicon transient-voltage suppressors is exemplified by the TransGuard voltage suppressor. The device, which is a true multilayer surface-mounted varistor, has a current capacity of 150 to 300 A. According to its developer, AVX Corp., Raleigh, N.C., that's five to ten times higher than silicon suppressors of similar size. The product dissipates energy in the total unit volume between its electrodes. This characteristic enables the device to take repeated surges without major parametric changes. In contrast, silicon-based devices dissipate transient power in their depletion regions only. Call Ron Demcko at (919) 878-6224. *DM*

BUILD STD 32 BOARDS FOR LESS

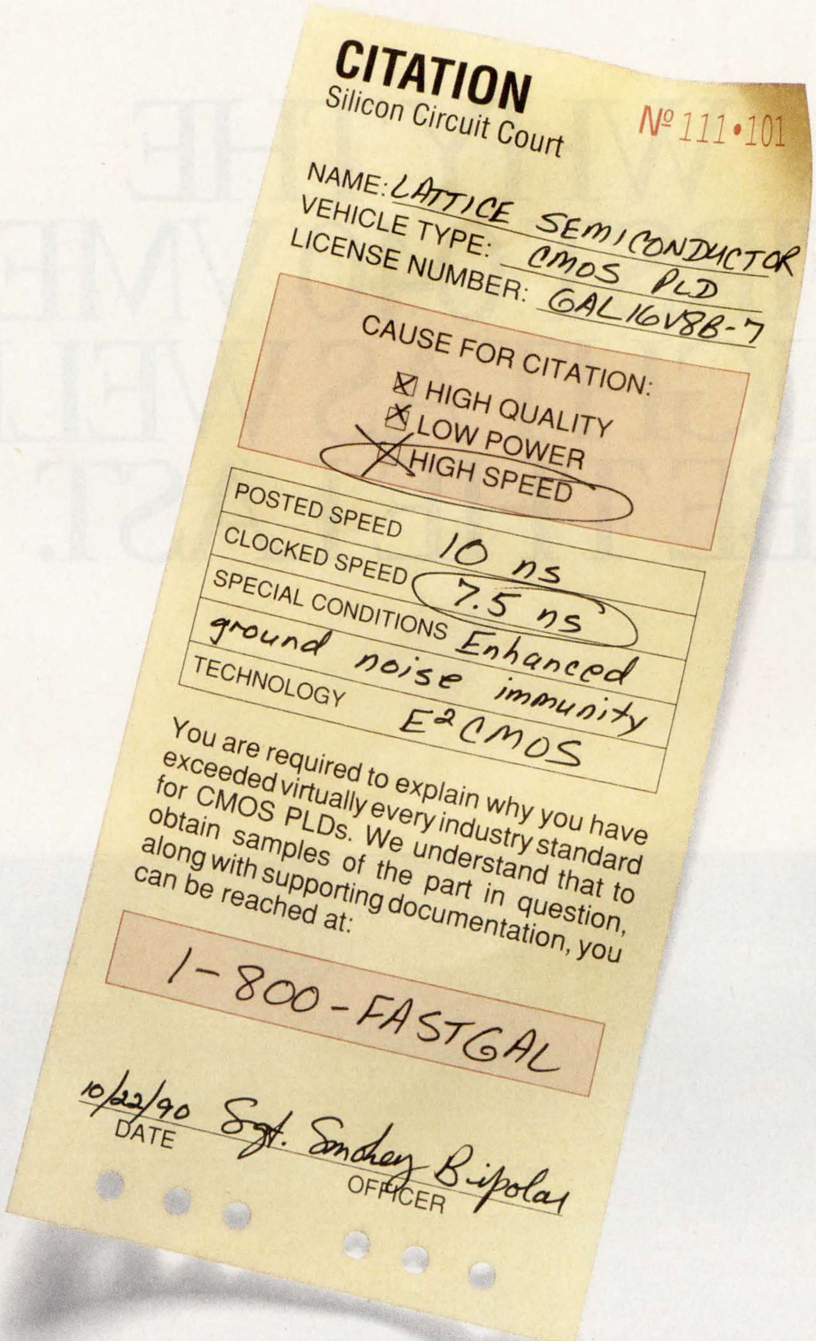
Using the STD 32 specification is now much more affordable for those employing it on a limited basis. Previously, users building boards to the 32-bit STD bus spec paid a $1000 licensing fee to Ziatech Corp., San Luis Obispo, Calif. To benefit smaller STD I/O manufacturers, Ziatech cut the fee to $150 for those companies that strictly build I/O boards, not CPUs or backplanes. This lower fee includes unlimited rights to manufacture and sell STD 32 I/O boards of any compliance level. STD 32's goal is to offer a compatible upgrade path to 16- and 32-bit computing for present 8-bit designs. For more information, contact Phil Nash of Ziatech at (800) 733-2111 or (805) 541-0488. *RN*

OPTICAL CLOCK PUSHES COMPUTER SPEEDS

Communications in systems ranging from supercomputers to telecommunications switches could become up to ten times faster using an optical clock created by researchers at Bellcore, Livingston, N.J. The prototype part uses lasers and other optical technology to hasten the ticks of a computer's clock. It takes advantage of the laser's ability to generate short, synchronous pulses. In addition, the optical fibers can carry light beams with virtually no loss or timing variation. Most high-speed computers are synchronous machines that must wait for a periodic pulse or signal from a clock to reach every circuit board before executing the next function. These computers are often slowed by conventional electronic timing devices and copper-wire connections. This results in less-accurate and more-costly computing. Consequently, designers must attach a "mode-locked" laser that acts as a master timing device to a strand of optical fiber. Then they attach a star coupler that splits the light into 1024 new beams. The beams, which are sent down separate pieces of fiber, are ultimately connected to circuit boards by a receiver. The timing signal's accuracy is within 12 ps over all 1024 boards. *RN*

VLSI DESIGN TOOLS SPUN OUT AS SEPARATE FIRM

In this era of megadeals in which one company swallows up another, its comforting to see a firm take a more conservative approach and spin out a company. That happened earlier this month when VLSI Technology Inc., San Jose, Calif., transferred its well-respected IC design tools to a newly formed and wholly owned subsidiary, Compass Design Automation, also of San Jose. Compass will be responsible for marketing all of VLSI's tools to the open market and developing new, more advanced programs. By spinning the software off to a separate entity, managers at VLSI hope to distance the design-tool groups from the intimate tie into VLSI's manufacturing facilities. That distancing will permit Compass to seek out relationships with other foundries and software suppliers. By broadening the reach of the VLSI Technology software to include macrocell libraries from a number of different semiconductor foundries, Compass hopes to become a foundry-independent software supplier. Other efforts by Compass include participation in a multicompany forum to define a standard for vendor-independent libraries for gate-array, cell-based, and other IC designs. Contact Taylor Scanlon, (408) 434-7648. *DB*



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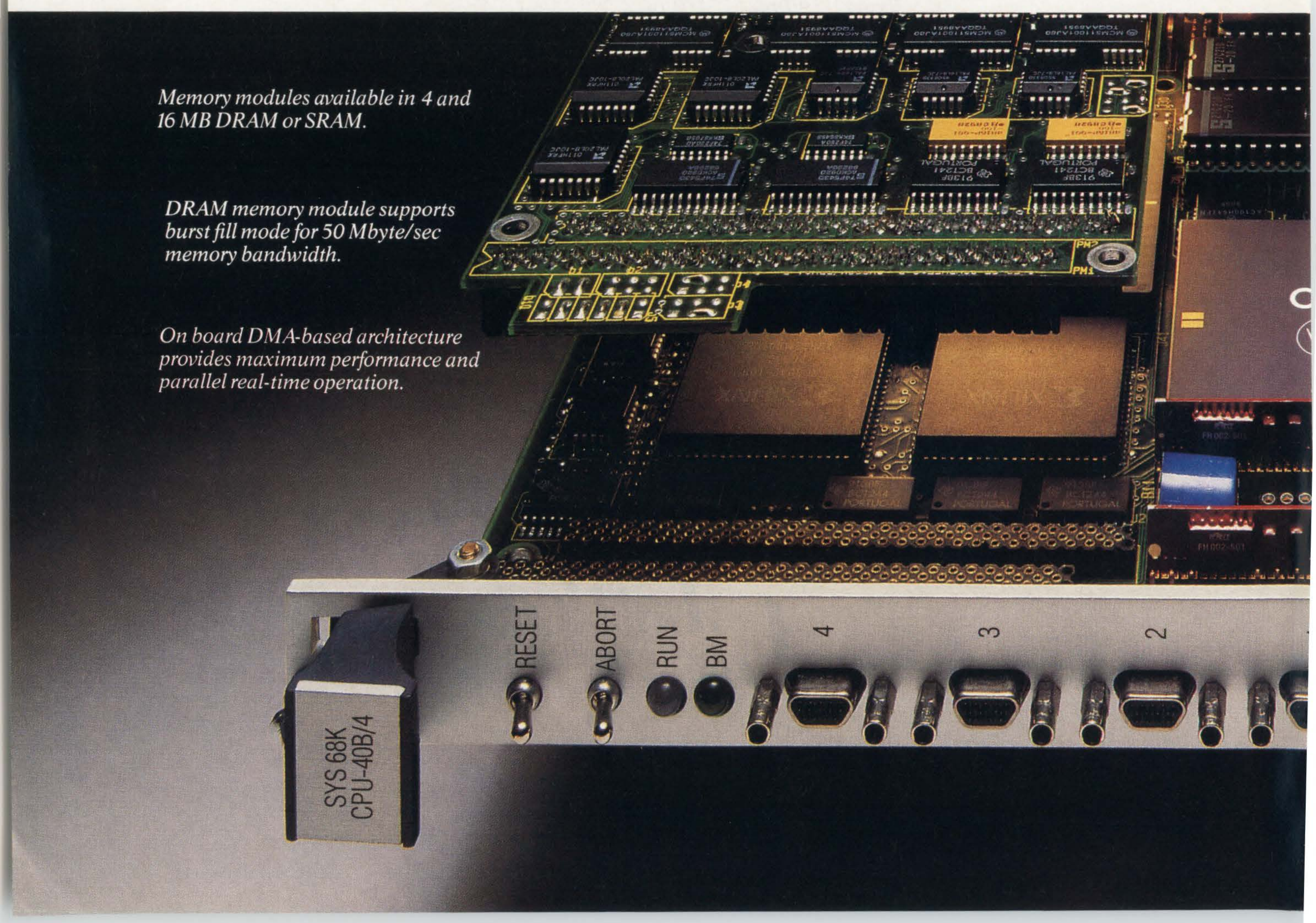
CIRCLE 158 FOR LITERATURE

WHY THE FIRST 040 VME MIGHT AS WELL BE THE LAST.



First, we're delivering 040 VME single board computers today. In quantity. So you can get started while the rest of the world waits for a delivery date from other suppliers.

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So it might just be the last 040 board you'll ever need.

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Of course, we provide comprehensive support with the industry's best-rated documentation,** complete systems integration support and technical assistance.

CPU-40 PERFORMANCE CHARACTERISTICS

Data from	CPU	CPU	CPU	CPU	VMEbus	SCSI*	Floppy Disk*	Ethernet*	Shared RAM*	VMEbus*
Transfer to	Shared RAM	EPROM	Serial I/O Timers	SCSI, Ethernet Controller, Floppy Disk	Shared RAM	Shared RAM	Buffer RAM	Dual-port RAM	VMEbus	VMEbus
Transfer Speed	53.7 MB/sec	16 MB/sec	2 MB/sec	2 MB/sec	5 MB/sec	4 MB/sec	500 KBit/sec	10 MBit/sec	15 MB/sec	15 MB/sec
Local 68040 CPU Operation	100%	100%	100%	100%	70%	80%	100%	100%	75%	100%

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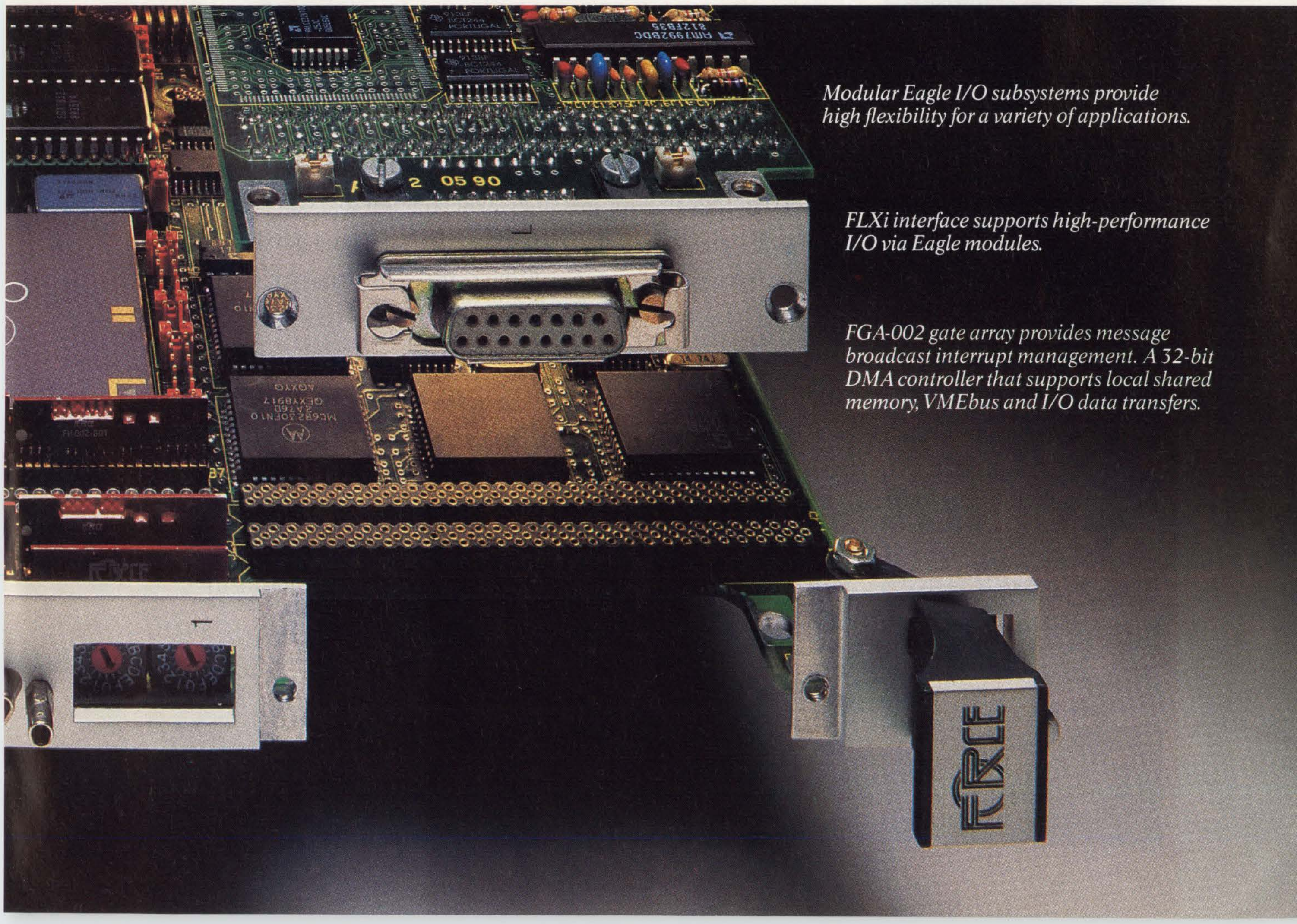
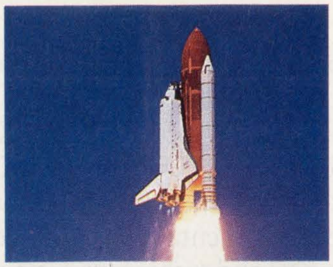
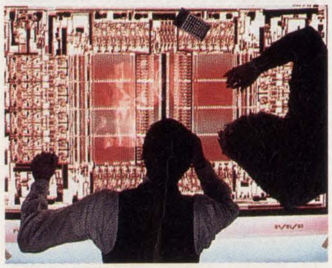
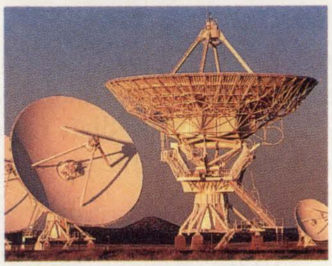
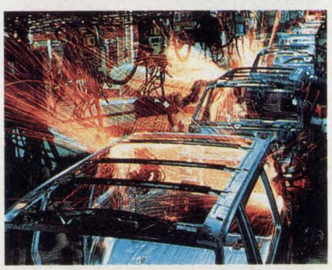
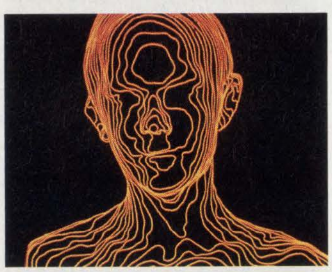
CIRCLE 80




PINLESS LAND-GRID-ARRAY SOCKET HOUSES INTEL'S 80386SL MICROPROCESSOR

Last fall's debut of Intel's high-integration version of the company's 80386SX microprocessor—the 80386SL—demanded a response from interconnection manufacturers. The chip is housed in a 227-pad land-grid-array (LGA) package, which is like a pin-grid array without its pins brazed on. As such, the package calls for a pinless interconnection scheme. Now, Rogers Corp. answers that call with a socket capable of handling the 80386SL. The technology can be extended to other LGA devices.

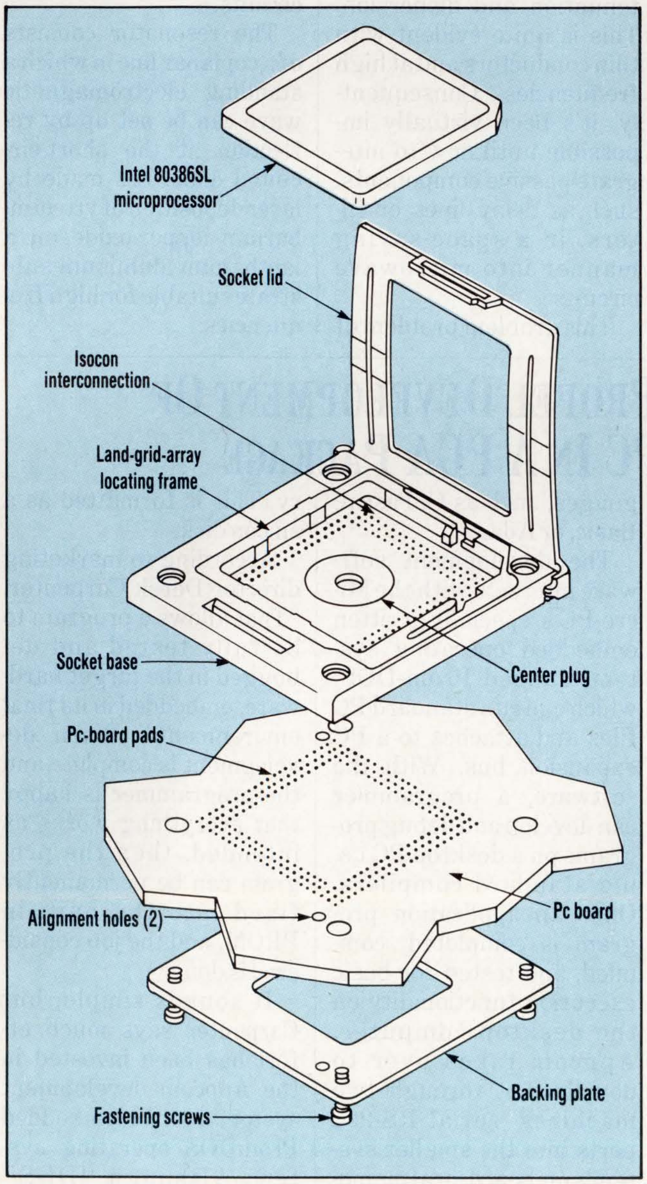
The Rogers socket is based on its Isocon technology *(see the drawing)*. The Isocon connector consists of an array of flat S-shaped beryllium-copper conductors suspended in high stress-retention microcellular silicone. As the connector is compressed, the conductors rotate around the center of their supporting medium to provide an aggressive 9-mil wipe at each conductor interface. Clamping hardware maintains the compressive load. In addition, a gas-tight contact is made over thousands of mating cycles.

Some of the system's key benefits include grid pitches between 0.100 in. (2.54 mm) and 0.050 in. (1.27 mm), as well as variable conductor location within a grid. Total contact resistance is less than 10 mΩ and total contact inductance is about 0.5 nH. A very low compressive force of about 15 lbs. is required to make a solid connection with the 80386SL chip's contacts.

Using a cellular material is essential because it preserves the accurate location of the conductors. The foam is only locally compressed by a reduction in size of the cells. As a result, it doesn't bulge in compression as solid elastomers do, which would change the location of the embedded conductors.

To place the conductors within the microcellular silicone matrix, slots are cut into the matrix with a laser. As a result, very little tooling is required to generate specific conductor-location patterns. The conductors themselves are built up using a beryllium copper core that's plated with 75 μin. of nickel, 50 μin. of hard gold, and 50 μin. of soft gold.

After long-term testing, which included high-temperature aging, temperature cycling with humidity, 10,000 mate-demate cycles, and various aggressive corrosion tests, the socket showed only very small increases in total interconnection resistance. In addition, there was a small and consistent standard deviation of the total resistance, indicating a reliable interconnection system.



Heat can be drawn away from the chip by two methods. In one method, a thermally conductive socket lid makes intimate contact with the ceramic on top of the LGA package. Here, it draws heat away from the package and functions as a heat spreader. Another technique involves an electrically insulated heat slug that's used under the LGA package and rests between the package and the pc board. Adding internal thermal pads and vias to the pc-board planes enables heat to be drawn from the bottom of the LGA package to the pc board's surface.

Machined-metal versions of the Isocon socket are available now, and molded parts will be available by the end of April. In prototype quantities, the molded socket will cost from \$0.60 to \$1.50 per pin. Tooling and non-recurring-engineering charges will run from \$5000 to \$10,000. In production volumes, the price run from \$0.15 to \$0.20 per pin. NRE charges for production runs can be as high as \$100,000, depending on volumes and complexity.

Contact the Rogers Corp., Circuit Components Div., 2400 S. Roosevelt St., Tempe, AZ 85282; (602) 967-0624.

DAVID MALINIAK

SUPERCONDUCTING THIN FILMS BOOST MICROWAVE RESONATOR QS UP TO 40 TIMES

Using zero-resistance high-temperature superconductors for planar thin-film structures, researchers at Siemens AG in Munich, Germany, have developed laboratory-type microwave resonators with a significantly improved quality factor Q over conventional resonators made from copper. The improved Q values were observed at different temperatures and different frequencies.

At 6.5 GHz and a temperature of 77K, a Q factor of 3840 was measured. Larger-area resonators, manufactured at the company's Erlangen laboratories together with Semiconductor Technologies in Santa Barbara, Calif., attained Qs as high as 12,000 at 10 GHz. That figure, Siemens says, is 40 times higher than the Q that's achievable with corresponding resonators from copper.

The quality of microwave resonators depends mostly on the conductivity of the material used. Another key factor involves the ohmic losses in metals due to the electrical resistance of the conducting lines, leading to signal attenuation and dispersion. This is quite evident with thin conductors and at high frequencies. Consequently, it's been virtually impossible until now to integrate passive components, such as delay lines or filters, in a space-saving manner into microwave circuits.

This problem problem of integrating passive components can be solved through the use of zero-resistance high-temperature superconductors that are cooled cheaply and efficiently with liquid nitrogen, which Siemens researchers verified with their demonstration device. The device they used was a line resonator, an important basic component of integrated microwave circuits.

The resonator consists of a coplanar line in which a standing electromagnetic wave can be set up by reflection at the short-circuited ends. It's made by laser deposition of yttrium-barium-copper-oxide on a lanthanum-aluminum substrate suitable for high frequencies.

This fabrication method allows the epitaxial deposition of thin monocrystalline superconducting films. The superconducting phase of the deposited material is formed during cooling in an oxygen atmosphere without subsequent treatment.

The resulting films can be structured by photolithographic and wet-chemical etching methods. The high-current capacity—about 1,000,000 A/cm^2—of the thin films made this way doesn't impair the resonator properties even under a high load.

Siemens foresees other high-frequency applications for high-temperature semiconductors. Such examples include high-efficiency antennas as well as dispersion-free signal transmission in high-performance computers.

JOHN GOSCH

SOFTWARE AIDS PROPEL DEVELOPMENT OF 8088/86-BASED PC IN A PGA PACKAGE

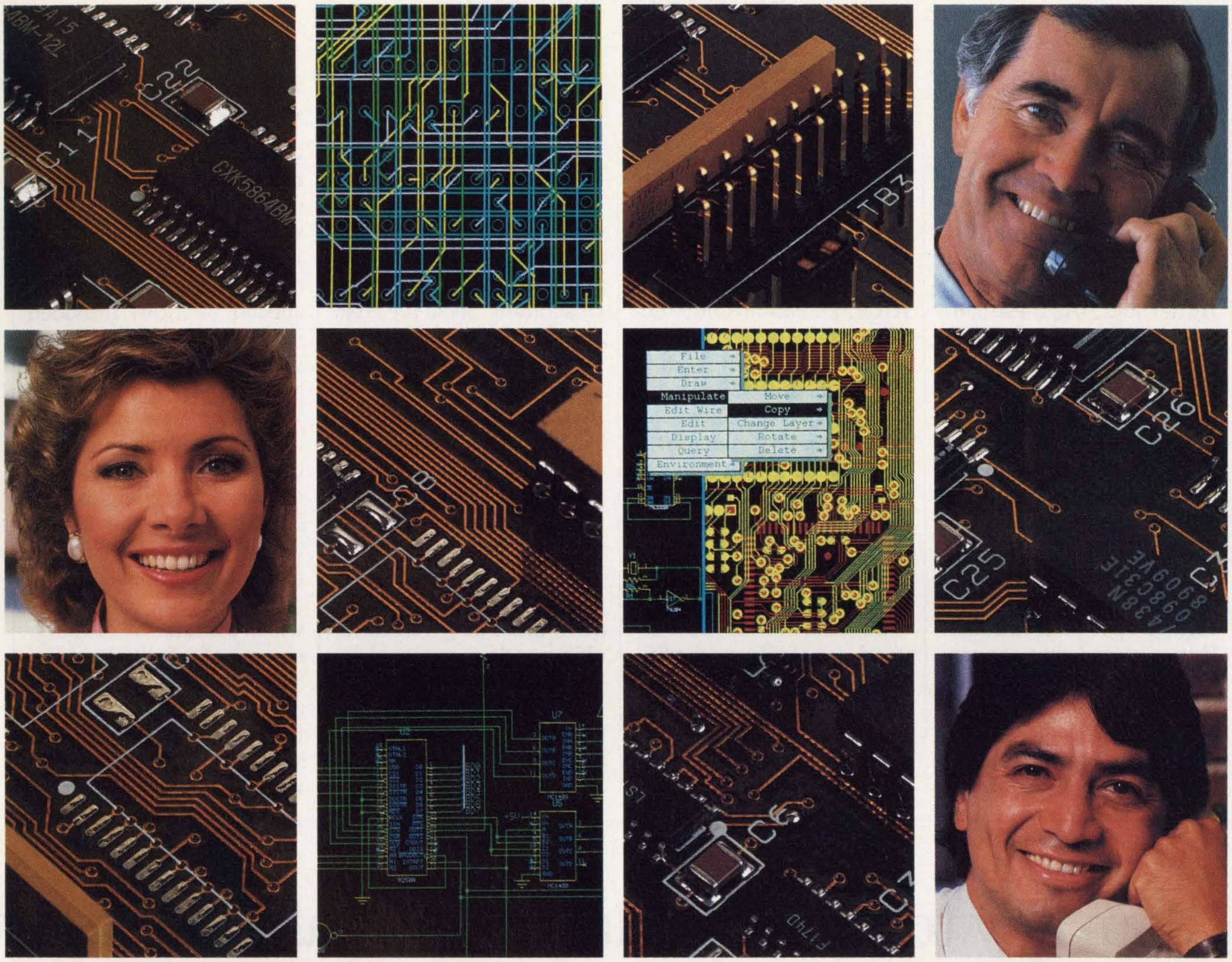
Reducing the size of an IBM-PC-compatible computer for use as an embedded controller is only half the battle in making it truly useful. What's just as important is to develop efficient software development aids that are compatible with the facilities of the computer. Designers at Hexatron Ltd., Letchworth, Hertfordshire, United Kingdom, have created an 8088/86-based PC-compatible computer that fits into a 60-by-55-mm (2.1-by-1.9-in.) 128-pin pin-grid-array package, and enhanced it with a software development kit called Appcom. The kit allows programming in high-level languages, such as C, Pascal, Basic, or Ada.

The development software interacts with the Micro-PC's specially written embedded operating system, dubbed Prom-DOS, which can run standard PC files and attaches to a PC expansion bus. With the software, a programmer can develop and debug programs on a desktop PC using standard compilers. Once an application program is completed, compiled, and tested for basic execution functionality on the desktop computer, Appcom takes over to download it through two machines' serial RS-232 ports into the smaller system's on-board local memory. This is formatted as a silicon disk.

According to marketing director Derek Carpenter, "That allows a program to be fully tested and debugged in the target hardware, embedded in its final environment." When development is complete and the programmer is happy that everything works as intended, then the program can be permanently fixed into the built-in PROM, and the job considered is done.

It sounds simple, but Carpenter says much effort has been invested in the Appcom development system and the embedded PromDOS operating system. Although "DOS" stands for disk operating system, the Micro PC is a diskless machine. This means both programs had to incorporate some special tricks so that the standard PC operating system, MS-DOS, could be emulated, and that it still occupied only a small portion of the computer's memory-storage space.

Hexatron technical director Andrew Butler explains that during the debugging process, Appcom puts two windows on the larger computer's screen, one for the target system and the other for command and control. A range of 15 special functions are thus made available, including file transfer, silicon-disk creation, and PROM programming. It also provides an interactive capability during the debug process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using a Basic interpreter built into the operating system.

"This has a full range of commands that give complete hardware control," Butler said. "As these commands are part of Basic, they can be used directly from the command line, or made into quick programs. This is much more powerful than normal batch commands and more flexible than a conventional debug program."

The resulting applications programs, too, are afforded special treatment. Butler stated that conventional MS-DOS programs are inefficient in their use of a machine's system memory—they must be relocated in memory each time they're run.

"They're not pure executable code," he said, "and that means the entire program file has to be copied from disk to working RAM, and all absolute addresses have to be changed, and that adds overhead time." Moreover, a standard compiler will allocate large portions of a PC's memory on the assumption that it has large amounts of memory to play with.

For embedded systems, both time and memory are commodities that must be used carefully and efficiently. In addition to running standard PC program files with the .EXE extension, Appcom can convert them into a special ".BIN" file. Butler explains: "These files are generated automatically from the original and are specially compacted to use very small amounts of memory. In addition, these files can run directly from the system's silicon disk without being copied into the system's operating memory." That also means programs can be fixed into PROM, protecting against corruption caused by power-supply glitches.

As an embedded computer, special consideration must be given to its ability to drive external devices. This is where the Prom-DOS/Appcom combination has its special capabilities.

"Unlike MS-DOS systems, Prom-DOS is fully re-entrant, so device drivers can use the operating system directly, and therefore be debugged in operation," Butler said. With special facilities provided in the development kit, programmers can write sophisticated driver software that can control a number of devices in real time "with just a few lines of code," according to Butler. Effectively, he claims, this gives the Micro-PC a multitasking ability.

Hexatron's Micro-PC, which contains all of the elements of a fully functional PC and needs no external components, uses a modified 10-MHz NEC processor that's fully compatible with the Intel 8088/86 family of processors. The package includes 512 kbytes of RAM, 512 kbytes of EPROM, and a 24-line dual serial input-output interface with three timers and an interrupt controller.

The main memory of 512 kbytes of RAM is housed in a thin small-outline package (TSOP) that's mounted under a 32-pin DIP socket in which the EPROM fits. Apart from the EPROM socket, all components are surface mounted.

The Micro-PC's I/O lines are compatible with TTL levels. The computer's output lines provide current-sinking capability.

Interfaces include two serial channels with Clear To Send and Request To Send signals. Both are capable of asynchronous communications with selectable data rates of up to 38 kbaud, including stop bits and parity. Interface levels are 5 V, making it possible to use RS232, RS423, RS422 and RS485 buffers. External buffers are required for obtaining full voltage and current levels when interfacing with RS232 lines.

The only power-supply requirement for the tiny computer is a single +5-V rail. Maximum current drain is 100 mA.

Physically, the Micro-PC is mounted in two parts. The actual circuit is mounted on a small pc board, which itself mounts onto a separate PGA carrier. This carrier is then fixed to a larger pc board by wave-soldering techniques, using automatic pick-and-place equipment. The larger board is then fixed in place with four screws, picking up electrical contacts automatically.

Carpenter says that pinouts of the Micro-PC have been specifically arranged to make it possible to link with external devices, including keyboards or pads and displays. Timing signals are given for external memory and I/O devices, and permit expansion to address 1 Mbyte of memory and 1 kbyte of I/O.

Specific signals are provided for linking the Micro-PC with an interrupt controller chip (an 8259), a real-time clock, graphics-display drivers, PC-type keyboards, and a watchdog and power-monitor device. Carpenter adds that the computer's standard digital I/O lines can connect directly with liquid-crystal displays and keypads.

Hexatron is also developing another version of the Micro-PC that will use an NEC-53 microprocessor. This processor is equivalent to the Intel i80286 microprocessor.

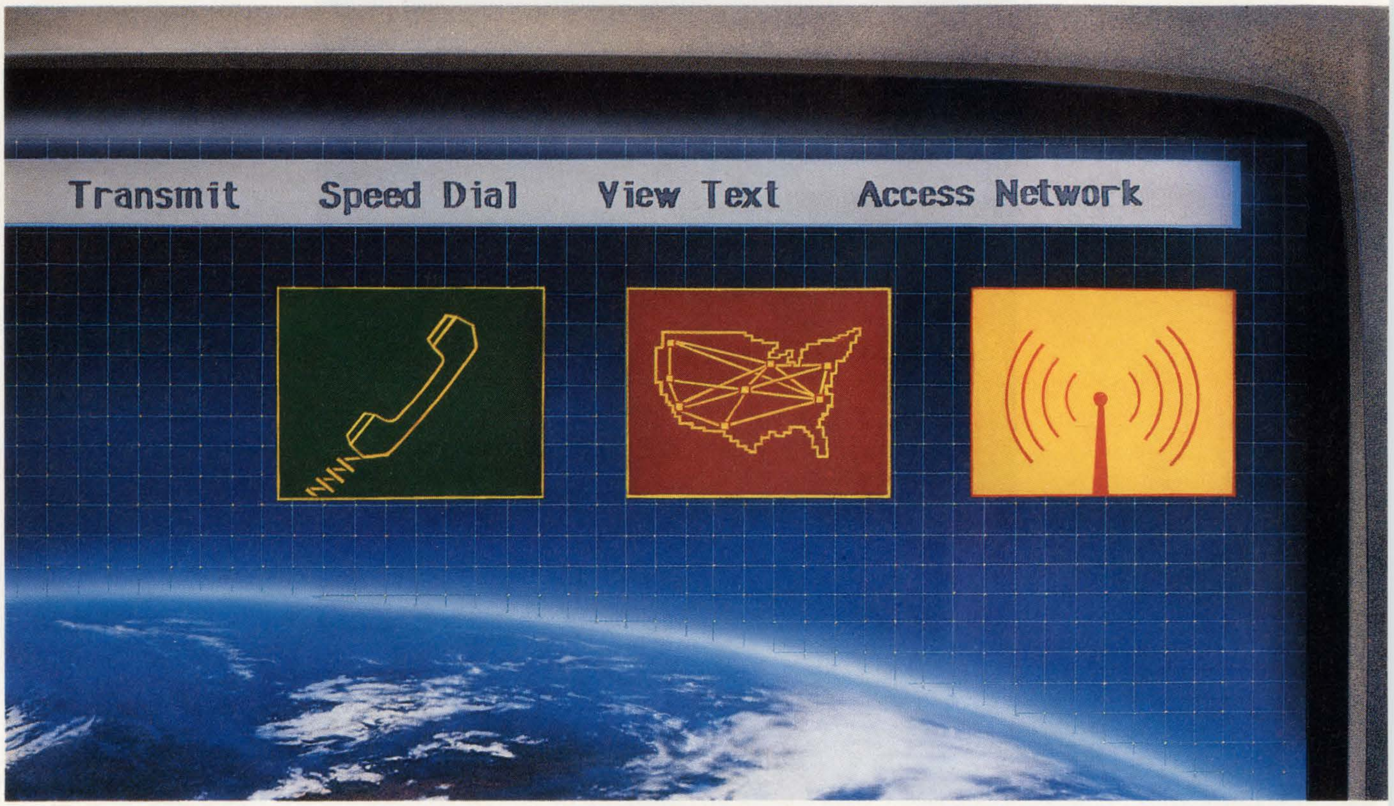
In the United Kingdom, the Micro-PC sells for £187 (dollar prices have yet to be set), and the Appcom design kit for £995.

For more information on the Micro-PC, contact Hexatron at 44(0)462 675530.

PETER FLETCHER

LITTLE FOOT.

SIEMENS



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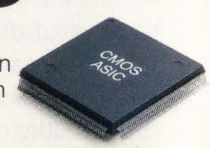

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CIRCLE 86

CHIPS RENDER WORKSTATION GRAPHICS INEXPENSIVELY

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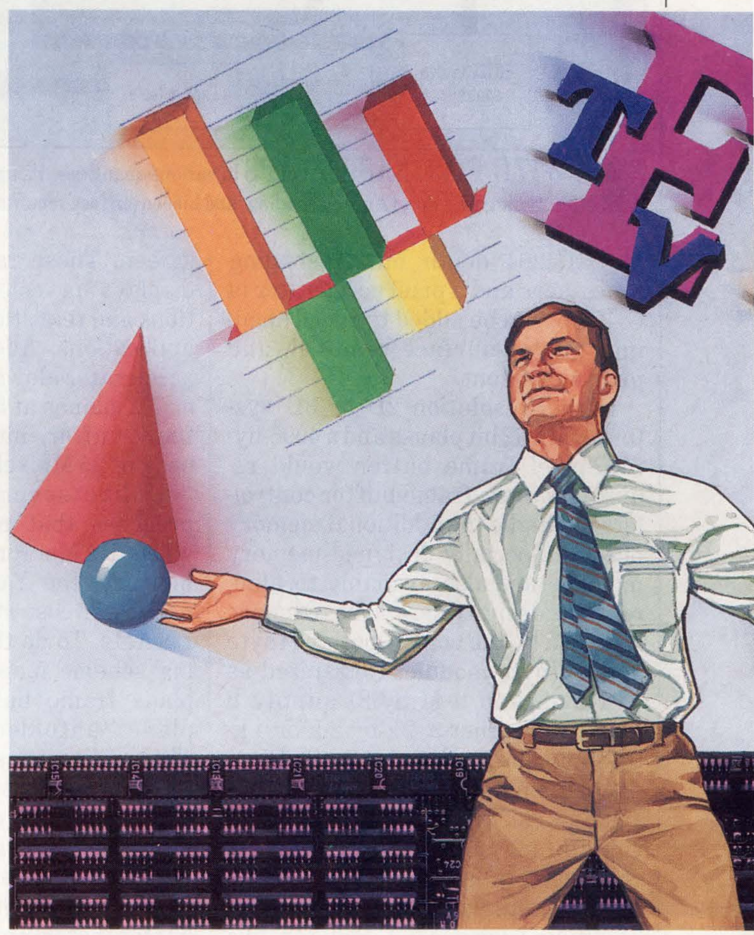
DAVE BURSKY

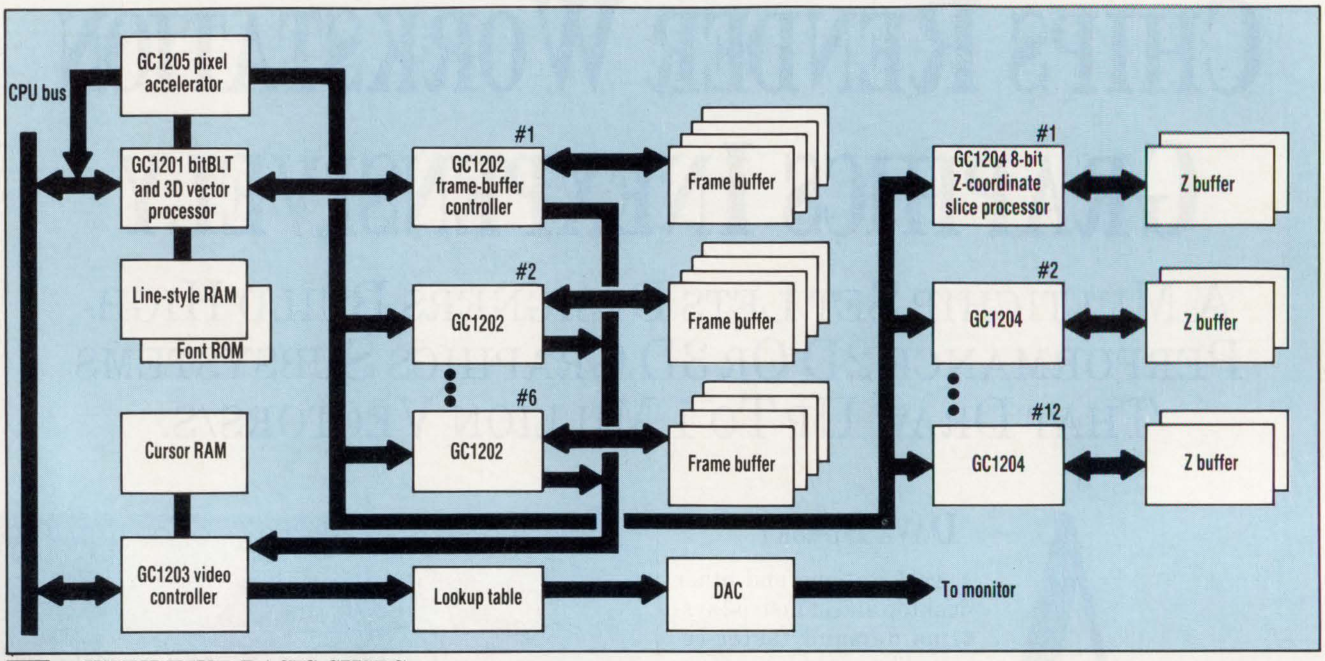
As workstations and other desktop and industrial systems demand faster-responding and higher-resolution graphics, system designers are running out of options. Unless they design their own custom graphics-control chips—an expensive process—they're limited as to what they can do. They can use dedicated chips for IBM-PC VGA or 8514A graphics. Or they can choose programmable processors that deliver VGA to mid-range graphics with acceptable performance. Or they can program RISC processors for high-performance graphics.



The need for an off-the-shelf graphics solution that performs like custom chips at a fraction of the price is critical. Such a solution could foster a new degree of standardization for graphics software, which until recently required custom drivers to be developed for each hardware platform. This gap in underlying graphics hardware hasn't gone unnoticed—Yamaha's Electronic Systems Div. has developed a multichip set that delivers high-end workstation graphics, at a component cost of $1000 to $3500 (evaluation-quantity pricing), not counting display memory. If quantity usage ramps up to thousands of units, the company estimates chip prices could drop by more than 60%.

There are five ICs in the initial chip set: the GC1201 bit-block-transfer unit and 3D vector processor, the CG1202 frame-buffer controller, the CG1203 video controller, the CG1204 depth buffer with shading processor, and the CG1205 pixel accelerator. The five 0.8-μm CMOS chips contain from 3500 to 13,000 gates each.

The chip architectures are crafted with system scaling in mind. A low-end system with eight bit planes and a 4096-by-2048-pixel frame buffer could be built with as few as three chips (not counting RAM): the GC1201, 02, and 03 *(Fig. 1)*. That system can draw 3D vectors at 35 ns/pixel, while bit-block transfers (bitBLT) go as fast as 18 ns/pixel. To upgrade the system, multi-



1. WITH FIVE BASIC CHIPS in various quantities, Yamaha's designers can craft high-performance color-graphics subsystems that offer 24-bit true color, Gouraud shading, and hidden-surface removal. The systems can draw short vectors at rates of over 1.2 million vectors/s.

ple GC1204 depth buffer/shading processors and a pixel accelerator (a GC1205) can be added to speed shading, hidden-surface removal, and pixel movement.

Higher-resolution 2D or 3D systems with 32 bit planes and a 4096-by-8192-pixel frame buffer would require six more frame-buffer controllers to handle the additional memory needed. Specially designed memory modules are also available to minimize the design time and board space required by the chips—both 1-Mbyte and 4-Mbyte modules (organized as 1-M-by-8 and 4-M-by-8) supply 8 planes for either a 4-k-by-2-k or 4-k-by-8-k frame buffer, respectively.

Assuming that the memory subsystems can keep pace with graphics circuits, 1.2 million 10-pixel 2D full-color vectors, or 0.7 million 3D full-color vectors with depth cueing, can be drawn each second. Polygon fills (100-pixel full-color polygons with shading and Z-buffers) can be done at 120,000/s for 2D and 70,000/s for 3D graphics. Both the vector and polygon numbers hold constant with any multichip combination used for the GC120X series. Up to 100,000 high-resolution (16-by-16-pixel) characters/s can also be drawn on the screen. Those rates offer dynamic displays in color-graphics simulations and realistic movement in CAD applications. Adding the 1205 pixel accelerator alows bitBLT operations on XY planes at 50 Mpixels/s. Using the Z-buffer, bitBLTs can reach a peak of 25 Mpixels/s.

Unlike several other chip approaches that require dual-ported video RAMs for the frame-buffer memory, the Yamaha chip set can use lower-cost standard single-port DRAMs. To do that, a novel unfolding scheme maps the entire multiplane frame buffer into a single-plane "unfolded" memory array. That makes it easier to use the memory, and enables users to zoom and pan around the entire buffer space as if it were all visible simultaneously. Furthermore, the frame-buffer controller chip has a double cache buffer that improves the access time to the frame buffer. And, to reduce the read/write access time of the single-port memory, the frame buffer is accessed in blocks by parallel read-modify-write operations. An image can thus be read from the frame buffer at up to 55 Mpixels/s.

The GC1201 contains the bitBLT and 3D vector processor, which together perform command analysis, vector generation, and data transfers. An asynchronous bus interface ties the 179-pin chip to the host-CPU interface. The vector generator contains a pipelined, three-axis digital differential analyzer (DDA) and can draw 3D vectors at 35 ns/pixel. Maximum resolution for X-, Y-, and Z-axis coordinates is 2^{16}, 2^{15}, and 2^{20}, respectively. The chip can pan over the entire unfolded memory plane as if the entire image was on the video screen. Zooming in ratios of 1 to 16 can also be done with no significant delay.

The chip has an overall drawing rate of 70 ns/pixel, which includes the write time to the pipeline circuit and the frame buffer. If the vectors are short (10 pixels), that can translate to a drawing rate of over 1 million vectors/s. Fat-line drawing, attribute-control functions, and a text-control circuit are also included in the 1201. If an external font memory is connected to the chip, any font can be drawn on an arbitrary bit boundary. Up to 32,000 different text styles and up to 256 line and interior styles can be used simultaneously.

The chip's bitBLT capability allows transfers to the frame buffer of plane, pixel, or array data formats, and supports bit-shift, auto wraparound, and transparency control. Command or memory I/O operations are supported for the host CPU and frame buffer. Frame-buffer read and write speeds are both 18 ns/pixel (24-bit true-color mode).

The 1201 has many powerful graphics commands. Besides basic line drawing and data-movement operations, it has a Set Character Font instruction. This command lets it switch from pixel data to a character memory, and thus quickly change from image to text, by using the character code following the command to control the access to the character memory. The Set Line Style command allows users to rapidly switch the line types among any of the potential 256 styles available.

Tying the 1201 into the frame-buffer memory array, the 256-lead GC1202 frame-buffer controller converts the frame-buffer image drawn by the 1201 into a digital video signal. Multiple 1202s can be connected together on a local high-speed graphics bus, with each chip supporting up to four frame-buffer planes. A system can use up to eight 1202s to create a 32-plane frame buffer. And because standard DRAMs are employed to implement the buffers, the buffer size can be easily upgraded by simply switching the RAMs when new-generation chips are available. As a result, such features as multibuffering, the display of large drawings, or direct copy transfers to a high-resolution laser printer are possible.

The XY plane or the Z direction of the frame buffer can also be reconfigured through software. For example, the 24 full-color planes typically ordered along the Z-axis can be rearranged in the XY plane as one monochrome plane, or as multiple frame buffers with different XY coordinates. The video image data is sent from the frame buffer to the GC1203 video controller, which generates all of the video timing signals. it also controls the image masks, panning, and the video cursors.

One 256-pin video controller chip processes the signals from up to 24 planes at a maximum video rate of 110 MHz. When running in a 60-Hz noninterlaced mode, the chip can supply display resolutions of up to 1280-by-1024 pixels. Since the frame buffer can be extended to almost any size, HDTV-compatible 1920-by-1035-pixel images can be created using an interlaced mode with a 74.25-MHz dot rate.

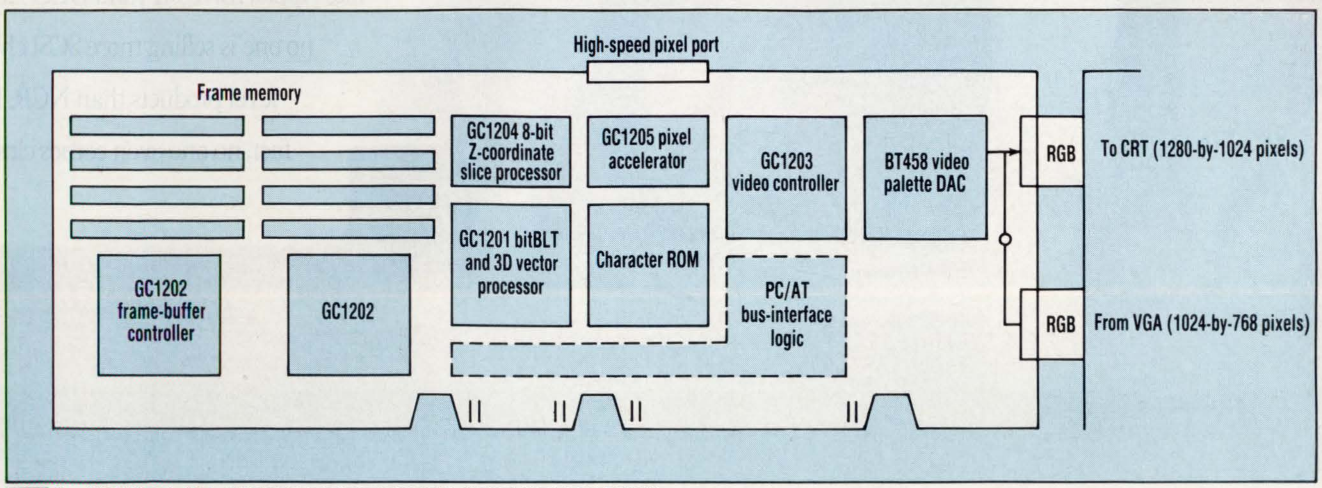
The chip's highly programmable aspects permit interlaced or noninterlaced operating modes, as well as user-definable video timing signals. With the maximum dot-clock rate of 110 MHz, the controller can handle most display resolutions. In the interlaced mode, screen refresh rates of over 80 Hz are possible; in the noninterlaced mode, the top refresh rate hits about 62 Hz. Masking operations are also possible—one for the entire plane-display control, and the other for arbitrary areas within a plane and arbitrary shapes. The chip also erases the screen in 4 ms.

Six different cursors, five of which can be displayed simultaneously (the four user-definable cursors and either the cross-hair or rectangular cursor), are handled by the controller. Address support for the four 64-by-64-pixel user-definable cursors is also on the chip. An off-chip 15-ns, 8-kbyte (8-k-by-8-bit) static RAM holds the cursor patterns.

Because cursor images are superimposed by video signals, the frame buffer's contents aren't disturbed. The combined digital video data and cursor signals are then fed to the lookup table memories associated with the video DAC, which delivers the video signal to the CRT.

The 100-lead GC1204 has an 8-bit processing slice to generate Z-coordinate values. It supports Z buffering, depth cueing, and shading operations thanks to a 24-bit integrator/divider, an 8-bit multiplier, and DDA circuitry. Up to three 1204s can be cascaded for Z-axis comparisons, which can be done at 35 ns/pixel. By arranging the chips in a matrix array, high-speed processing can be achieved by comparing 32 pixels simultaneously (four GC1204s for every Z-axis 8 bits). Ordinary DRAMs can be used to form the Z buffer.

Hidden surfaces are removed by



2. COMPACT, HIGH-PERFORMANCE GRAPHICS subsystems can be implemented on PC/AT-size add-in cards. Designing a system several notches above the simplest configuration requires six basic chips: one 1201 bitBLT and 3D vector processor, a pair of 1202 frame-buffer controllers, one 1203 video controller, one 1204 slice processor, and one 1205 pixel accelerator.

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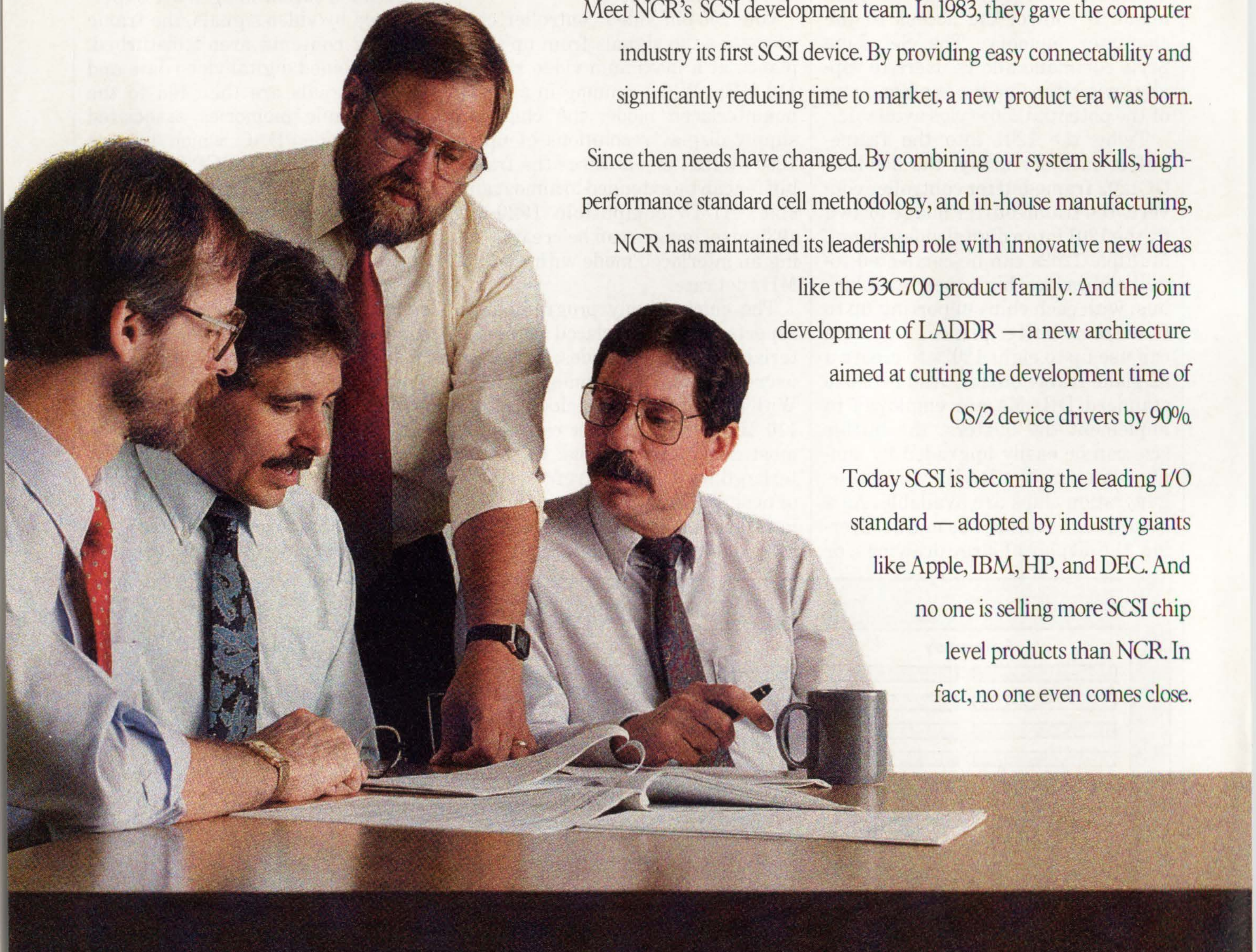

Part of the NCR SCSI Development Team: (left to right)
Jerry Armstrong, Sr.Software Engineer; **Harry Mason**, Strategic Marketing Manager; **John Lohmeyer**, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and **Dave Skinner**, SCSI ProductManager.

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having the 1204's Z-buffer control operate in parallel with the 1201's vector generator. The 1204 generates Z coordinates synchronized with the 1201's XY DDA interpolation at 36 ns/pixel. The coordinates are compared with the Z-buffer contents, and the result is transferred to a logical-operation selector circuit in the GC1202. The 1202, in turn, takes the results and determines whether or not the frame-buffer contents should be updated with the values in the data cache.

Gouraud-shading algorithms, which linearly interpolate the intensity between two points, are incorporated in the 1204 as well. The shading circuitry generates intensity in pixel units for each RGB color, synchronized with the XY DDA in the 1201 and the Z DDA in the 1204. The circuit operates independently of the cohabitating DDA; thus it can work in parallel. The shading data is RGB-coded with 8 bits per color. The GC1202's cache buffer is loaded with 24 bits/pixel through a 69-Mbyte/s graphics bus that connects the GC1202 and 1204.

To enhance the 3D images, depth-cueing logic on the 1204 generates up to 256 intensity levels that are inversely proportional to the Z-axis coordinate. It uses the coordinates of the front and back planes, the intensity scale, and the absolute intensity at two points to perform the calculation. The computations are done in accordance with the Phigs specification. Because depth cueing and shading are used separately, some of the circuitry is shared between both functions to save some chip area.

On-chip DMA controllers and FIFO buffers allow the 1205 pixel accelerator to give systems a four-fold improvement in the time required for bitBLTs. The accelerator chip is connected almost in parallel with the main GC1201 video controller. Instructions fed into the 1201 are also captured by the 1205, which "snoops" the bus, waiting for a command to interpret and execute. A large off-chip FIFO register (256 words by 24 bits) that buffers pixel data is controlled by a FIFO interface section and DMA logic that reside on the accelerator chip.

Because all of the chips were designed to operate together, a minimal amount of glue logic is needed to tie the chips into a host system. In fact, an AT-compatible add-in card can pack a complete video system, including the frame-buffer memory, to create a 1280-by-1024-pixel video display with a 4-k-by-2-k 8-plane frame buffer *(Fig. 2)*.

A more powerful VMEbus-based 6U evaluation card that has expansion connectors for a large daughtercard enables designers to maximize the system features. The base VME card has about the same features as the AT card. But the daughtercard includes the additional RAM to form an 8-k-by-4k-pixel frame buffer.

Within the next few months, Yamaha expects to have CGI and X-server drivers as well as an INS subset. Although no specially created software-development tools exist, standard VME hardware-development tools can be used to evaluate and develop software for systems using the chips.□

PRICE AND AVAILABILTY

Initial samples of every chip will be housed in pin-grid-array packages except for the GC1204, which will come in a 100-lead plastic quad-sided flat package. The GC1201, 1202, 1203, and 1205 come in 179-, 256-, 256-, and 135-lead PGAs, respectively. Samples of the chips will be sold in "kits." The $1000 basic kit has a 4-k-by-2-k-pixel frame buffer with one 1201, two 1202s, and one 1203. Extra 1204s can be added (up to five) at $100 each. The 1205 is also an extra $100. A larger kit for a 4-k-by-8-k-pixel frame buffer has six extra 1202s and sells for $3000. As with the other basic kit, extra 1204s and a 1205 can be included. Samples of all chips except the 1204 will be available next month; the 1204 will be ready in June. The custom memory modules—the 1-Mword by 8-bit and 4-Mword by 8-bit units—sell for $220 and $845, respectively. VMEbus evaluation boards, one with an 8-plane 4-k-by-2-k frame buffer and the other with a 32-plane 4-k-by-8-k buffer, sell for $6000 and $25,000, respectively.

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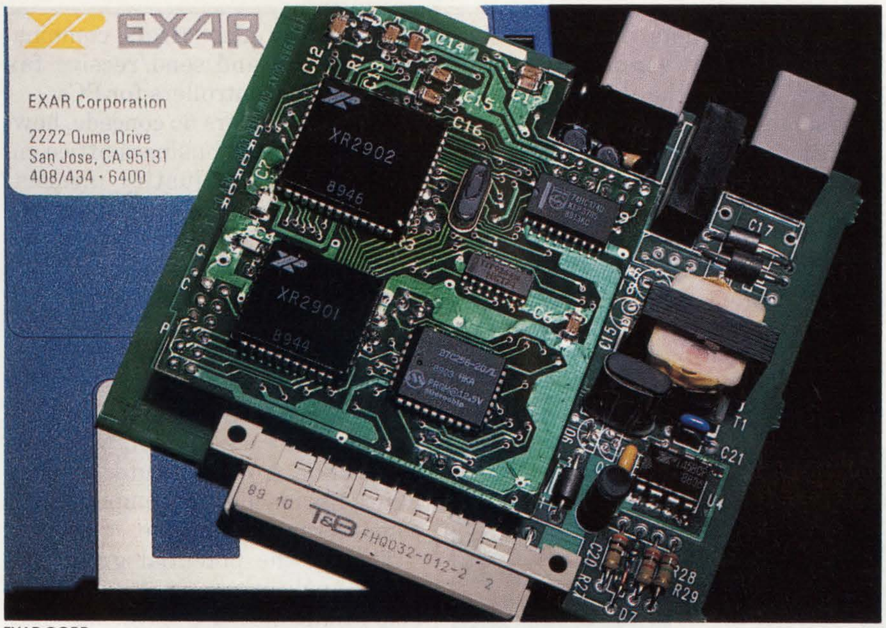

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WITH BUILT-IN FAXES BECOMING COMMONPLACE IN DESKTOPS, THE FOCUS NOW TURNS TO PORTABLE PCs.

FAX MODEM CHIPS BRING DATACOM TO LAPTOPS

Now that the last technical wrinkles for internal data/facsimile (fax) deployment in desktop personal computers are to be ironed out, the stage is set to attack the portable-computer market. With more portable personal computers, laptops, and notebook-size computers being used, an enormous opportunity exists to unite these document-producing machines with document-transmitting internal data and fax modems.

Before this can happen though, modem IC vendors must make some tough technical and marketing decisions. This is in view of the current uncertainty in changing fax-modem IC standards and unclear application requirements, even for desktops. For data modems, one decision is determining which compression and error-correction schemes to support. Another is whether to wait for the standards picture to clarify, or commit basic designs to silicon and depend on application software to track evolving standards *(see the figure)*. There are also the questions of what will be the biggest applications, what type of fax modems will be used, and in what type of computers and service will they be employed.

Some data-modem chip vendors say current industry technology-licensing practices can share the blame for any uncertainty about the market. The most recent flap concerns the V.42bis data-compression algorithm, for which IBM holds a patent. So does Unisys Corp. And British Telecom of the United Kingdom has applied for yet another. To obtain a license to incorporate the algorithm into their modems, OEMs must pay IBM a one-time \$20,000 charge or 1% of the price of each modem sold, \$20,000 to Unisys, and \$15,000 to British Telecom. The licensing cost is factored into the cost of the product.

Sierra Semiconductor Corp., San Jose, Calif., offers purchasers of its SC11091 modem controller the option of buying a PROM with the V.42bis code, only paying IBM \$20,000 directly. The PROM's price includes the cost of pass-through licensing for Unisys and British Telecom.

"We have no problem with the amount of the licensing fees," says Shyam Dujari, senior product marketing manager at Exar Corp., San Jose, Calif. "But IBM wants to license directly to systems manufacturers, which is a tedious approach that doesn't help the market." Exar believes licensing through chip vendors is more efficient and would promote faster product acceptance.

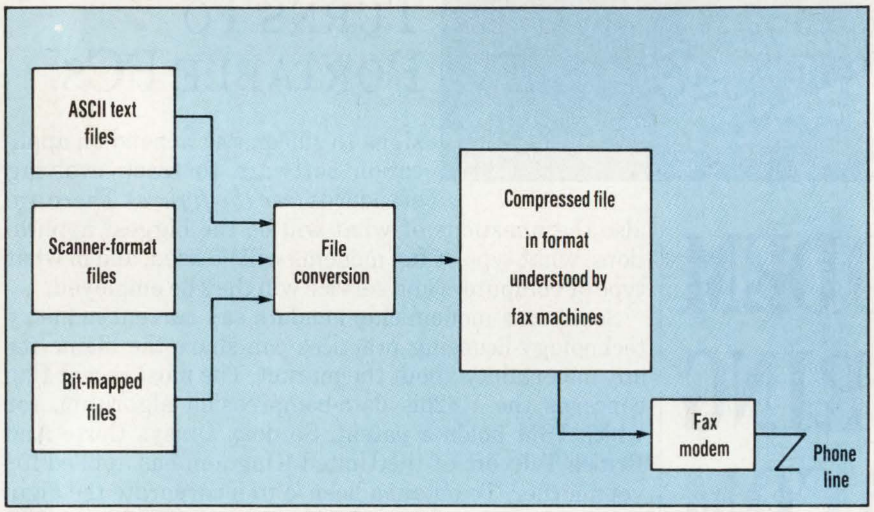
Rockwell International's Digital Communications Div., Newport Beach, Calif., feels that patent issues relating to the V.24bis standard have deterred many OEMs from implementing the protocol in their products. The company handles the situation by offering its "standard patent indemnification" to OEMs buying chips supporting the protocol. Details of this arrangement aren't yet available. However, the contractual agreement between Rockwell and its customers restricts application within Rockwell-stipulated guidelines.

Of more immediate concern is whether PC users really need both send and receive capability in their fax-equipped machines. Sierra Semiconductor argues that send-fax capability makes more sense than send-receive fax for most desktop and portable computer users. It argues that desktops are generally in an office environment that's equipped with a fax machine, and users might not want to tie up their machines with lengthy fax receptions.

Furthermore, because a received page of text is just a bit-mapped dot pattern representing characters of an ASCII code, the document can't be edited and rewritten. A computer may perform cut-and-paste operations on the image, but because all intelligence is stripped away from the document by scanning, it can only treat the document as a graphic element, not as an ASCII file. A data modem is much more efficient for transmitting alphanumerics.

Moreover, there's the issue of screen resolution. Most PCs have a 14-in. VGA monitor with a 640-by-480-pixel screen resolution, or 73-pixel/in. pixel density. If a received document has been scanned at 200 dots/in., the message is three times larger than the monitor. Consequently, reading it requires horizontal and vertical scrolling. A 14-in. Super VGA monitor with a 1024-by-768-pixel resolution (93 pixels/in.) displays about half of a document scanned at 200 dots/in., but readability still calls for scrolling. Unfortunately, scaling the document to fit the screen's dimensions isn't an ideal solution because it sacrifices both resolution and readability.

There's also the question of how faxed data will be received. Incoming faxes can't pass through a telephone switch at the receptionist's desk. An expensive front-end switch is needed to sense voice or fax and make the appropriate connection. The alternative is to use a separate line, which means paying an installation fee and a monthly charge. This also requires the sender to somehow alert the receiver to an impending fax transmission.



FAX APPLICATION SOFTWARE converts data files to a form that a fax machine can understand. Some file formats may need to convert to a bit-mapped format before the software can convert to a fax file format for transmission by the modem.

For these reasons, Sierra Semiconductor expects most of its business to come from its family of SendFax modem chips for PCs and laptops deployed in a departmental environment. This will allow a company to use simpler, less-expensive stand-alone fax machines, instead of more expensive ones intended for multiple users. The company first addressed this market about a year and a half ago with the SC11046 single-chip data/fax modem, a chip that combines 4800-bit/s fax-sending capability with a 2400-bit/s send-receive data modem. Since then, the company has introduced the SC11054 with 9600-bit/s fax-sending capability. The company also offers combinations of data and send/receive fax modems and controllers for PCs.

Fax-chip vendors do concede, however, that certain business-office environments may justify internal send-and-receive fax capability for PCs. For example, this is true for sophisticated setups that already have dedicated phone lines and high-end equipment, such as Super VGA monitors, laser printers, scanners, and PS/2 and Macintosh computers with ample memory capacity. The applications in this case are two-way communication from computer to computer, fax machine to computer, and computer to fax machine.

Though the potential growth of these applications isn't yet clear, chip companies are covering their bets by offering fax/data modem chips with send-and-receive capability. For example, Rockwell recently added another member to its True-FAX family of data/fax modems for use in PCs and portables. The RC9624AC integrates a 2400-bit/s data modem with send-and-receive 9600-bit/s fax capability for Group 3 fax operation. Send-and-receive functions at 9600-bits/s are also offered in Exar's XR-2900 FaxPlus chip set, and in Sierra Semiconductor's SK9698 chip set.

Chip and software vendors must also contend with the still-evolving fax-modem standards *(see "Fax protocols and standards," p. 49)*. The working document for Class-2 modems, called EIA 2388, is still undergoing changes, including command information content required for handshaking between modems. This information contains the modem manufacturer, type of software being used, the modem class, and revision number. The transmitting modem needs this information to determine what set of commands to use for the fax transmission.

Because of the changing standards environment, some fax-chip vendors are still introducing Class-1 modems that perform dial-up and connect functions, but no T.30 handshaking and T.4 error correction are done by DTE (data-terminal-equipment) application software. The

Class-1 standard was the first to extend the AT command set from Atlanta-based Hayes Microcomputer Products Inc. to control fax transmission. Although less flexible than Class-1 modems, Class-2 products have more features and require less involvement by the host CPU in fax operations. Already supported by at least two software houses, Class-2 modems combine T.30 handshaking with dial-up and connect functions. Although the standard is still evolving, most companies believe Class 2 is the way to go at this time.

More bothersome, however, may be the issue of data-flow control. Data rates above 19 kbits/s begin to present problems for fax transmission. In a typical send-fax modem, a buffer memory resides between the DTE bus and the modem functions *(see "Controlling data flow," p. 52)*. Before the buffer fills, an XOFF control signal is sent to the DTE. If the DTE doesn't respond quickly, the buffer can overflow and data will be lost. On the other hand, if the buffer is allowed to empty, the transmission is interrupted and the fax machine may disconnect.

What's needed is a buffer with large storage and the ability to issue flow-control signals to the DTE. With enough advance warning for worst-case latency under Microsoft Corp.'s Windows, this time period can be several hundred milliseconds.

As a result of these concerns, an expected major change in the PN (proposal number) 2388 recommendation is the addition of buffer-mem-

FAX PROTOCOLS AND STANDARDS

With some 600 different varieties of fax products offered by different vendors, a major challenge for modem hardware and software designers is to have their products communicate with as many existing products as possible. Fortunately, standards organizations simplify the job by classifying the various types of modems and by specifying how they communicate.

The International Consultative Committee for Telegraphy and Telephony (CCITT), which sets international communications standards, has classified four groups of facsimile service:

- Group-1 facsimile has analog transmission, no data compression, and transmits data over a public-switched telephone network (PSTN). A page of text is transmitted in about 10 min.
- With limited data-compression capability, Group-2 facsimile transmits a page of text over a PSTN in 3 min.
- Group-3 facsimile has digital transmission, complex data compression, and takes under 1 min. to transmit a page of text over a PSTN.
- Also containing digital transmission and complex data compression, Group-4 facsimile transmits data over a digital network (such as the Integrated Services Digital Network) with a page-transmission time of less than 1 second. This standard is subdivided into three classes of resolution. Class 1 and 2 have 200-bit/in. resolutions, and Class 3 has 300 bits/in. Optional resolutions are 300 and 400 bits/in. for Class 1, and 200, 240, and 400 bits/in. for Class 2 and 3.

Transmission rates for facsimile modems are under the same standards that govern data-modem transmission rates. Four of the latest CCITT data and fax modem standards track the escalating speeds of modem technology:

- V.29 defines 9600-bit/s fax modems for point-to-point, four-wire leased lines.
- V.32 defines two-wire, full-duplex data modems running at the same speed over dial-up and leased lines.
- V.32bis relates to 14.4-, 12-, 9.6-, 7.2-, and 4.8-kbit/s data modems for dial-up lines.
- V.33 defines 14.4-kbit/s fax modems for point-to-point, four-wire leased lines.

Other recent standards address error control, data compression, and connectivity for data modems:

- V.42 defines the LAPM (link-access protocol, modem) error-control procedure for transmission speeds of 1200 bits/s and higher.
- Levels 2, 3, and 4 of the Microcom Networking Protocol (MNP) are part of an error-control recommendation from Microcom Inc., which has become part of the CCITT V.42 standard.
- V.42bis is a 4:1 data-compression standard for modem speeds of 1200 bits/s and higher.
- Microcom's MNP Level 5 gives a 2:1 compression ratio for speed of 1200 bits/s and higher.
- MNP Level 7 offers a 3:1 compression ratio.
- T.4 is a compression scheme.
- T.30 is a handshaking protocol.

Meanwhile even more standards are emerging from the standards committees of various countries. In the U.S., the TR29 committees of the Telecommunications Industries Association (TIA), a subset of the Electronic Industries Association (EIA), recommend three modem classifications (not to be confused with those for resolution) that specify system elements for executing the handshaking protocol and performing data-compression:

- Class-1 (EIA 578) facsimile and data modems dial and connect to other modems. T.30 handshaking and T.4 data compression are performed in the DTE.
- Class-2 (EIA 592, also referred to as the 2388 proposal) modems handle the T.30 negotiation in the DCE (data-communications equipment, which can be a modem card or box), but not T.4 compression. This recommendation is still being amended.
- Class-3 modems perform both T.4 and T.30 functions.

ory definitions. Upon finalization, this proposal will be called EIA 592. As for buffer size, a 100-byte capacity suffices for standard DOS interfaces. But a Windows-enhanced or Macintosh environment needs anywhere from a 2-kbyte to 8-kbyte buffer to cover worst-case conditions. The PN 2388 committee is also determining at what unused capacity level the buffer should issue a wait command to the DTE's CPU to prevent overflow. A wait command can be a software instruction, such as XON/XOFF, or a hardware CTS (clear-to-send) signal.

Equally important, the DTE must service wait requests immediately, otherwise data is lost. For example, the priority level of an interrupt determines the wait time before the interrupt is serviced. The priority level for a DMA operation is higher than that for a communications port, and an I/O device interrupt priority level is somewhere between the two.

"This is especially critical for a PC running IBM's OS/2 operating system or Microsoft Corp.'s Windows on top of a high-speed communications program working in the background," says David Long, marketing manager for data communication products at Sierra Semiconductor. "Windows creates problems for a PC's communication ports by forcing the PC to wait for up to 300 ms before servicing an interrupt. At a 9600-bit/s fax rate, or 0.1 ms/bit, a lot of data is lost in that time."

Another potential error source are interrupt signals to the DTE. A PC treats a fax modem like any other modem. If an interrupt occurs while it's sending data to the fax modem, the computer may stop sending data and service the interrupt. Data modems are unaffected by such data stoppages because they have a built-in 60-second time-out feature. On the other hand, fax modems are designed to shut off when data flow is interrupted, thinking the transmission is finished.

Present error-control techniques for data modems also have room for improvement. "Available software algorithms for error correction and control do not provide a total solution," says David Long. "For example, the MNP error-correcting protocols of Microcom Inc. (Norwood, Mass.) perform modem-to-modem correction but don't deal with the PC-buffer interface where overflow errors can occur. On the other hand, a PC-resident protocol, such as XMODEM performs, PC-to-PC error correction by doing check sums on blocks of data. If a bad block is transmitted, XMODEM retransmits a corrected data block. But why not attack the problem at its source—the PC-buffer interface?"

Although existing modem hardware and software products can easily increase modem speed, a speed-limiting factor in the installed base of some personal computers has deterred the use of faster modems. The serial port in most MS-DOS devices in the IBM PC/XT and PC/AT models, along with some 80386-based machines, won't operate at data rates over 9600 bits/s. However, 80386-based machines using the 16C450 UART can operate at rates up to 19.4 kbits/s. Exar solves the problem by incorporating a speed-conversion/buffer feature in its products.

Another solution appears to be at hand in a new system of communications software developed by Hayes. Combined with a separate driver for data buffering and flow control, the enhanced serial-port (ESP) specification supposedly ensures data integrity for data rates up to 38.4 kbits/s. A version of this specification is implemented in Hayes' ESP card, which supports 19.2-kbit/s data rates on MS-DOS computers.

The quality of telephone transmission lines imposes another speed limitation. As transmission speed increases, data streams become more sensitive to adverse phone-line conditions. However, this problem appears to be solved by a Layer 2 link-level protocol from Microcom. Called MNP 10, the protocol supports CCITT's V.32, V.32bis, and V.22bis modulation standards, and AT&T's Bell 103A and 212A modulation standards. It also supports V.42 and MNP 1-4 error-control, and V.42bis and MNP 5 data-compression algorithms. The technology is designed specifically for communications in difficult transmission conditions, such as cellular, international, and poor-quality land-line connections.

MNP 10 handles adverse line conditions by constantly shifting transmission speed during the life of the connection. This upshifting and downshifting across the modulation schemes offers the highest possible speeds the transmission line will allow for maximum throughput. To ensure that both ends can deliver MNP services, modem handshaking begins at a low modulation rate selected by the user. Because call setup is the most vulnerable part of a MNP session, multiple attempts are made to establish a reliable link during noisy line conditions. After a connection is made, MNP shifts the modems to a higher modulation rate, line conditions permitting.

This past January, Microcom selected Rockwell as its first MNP 10 licensee. Rockwell will incorporate the technology into its V.22bis, V.32, and V.32bis modem chip sets. Until June of this year, customers can buy MNP 10 products from Microcom and MNP 10 chip sets from Rockwell. After that, an MNP 10 license for OEMs will be offered to the general public for a one-time fee ranging from $5000 to $20,000, depending on the annual revenue of the vendor requesting the license. Rockwell customers won't have to pay for a separate license. Key players in the portable-computer arena, such as Toshiba America information Systems, GRiD Systems, and Spectrum Cellular, will help promote MNP 10 as a de-facto standard and eventually a CCITT standard.

Other OEMs contend that the existing V.42 standard is flexible enough to handle cellular applications without resorting to yet another proprietary protocol with all its licensing complications. More important is to use an existing CCITT modulation standard that is least prone to making errors.

Once problems associated with putting basic internal data and fax modem capability into desktop and portable computers are more clearly defined, the solutions can't be far behind. In fact, the industry is already envisioning the capabilities of next-generation machines. "Basic PC fax will soon be history," says Dudley Westlake, product line manager for internal data/fax products at Rockwell. "Laptops and notebook computers are already beginning to rival desktop PCs in functionality, hard-disk capacity, and VGA resolution."

This trend is illustrated by the TravelMate family of notebook computers from Texas Instruments Inc, Dallas. The latest model, the 8.5-by-11-by-1.8-in. TM3000, weighs 5.6 lbs. and is powered by Intel Corp.'s 20-MHz 80386SX processor. Hard-disk memory capacity is either 20 Mbytes or 40 Mbytes, and the unit has a 1.44-Mbyte floppy diskette drive. Particularly impressive is the 10-in. diagonal VGA display, which is based on the triple-supertwist, side-lit LCD technology of Sharp Corp., Tokyo, Japan. The screen has 640-by-480-pixel resolution and 32 gray scales.

TravelMate options include a 2400-bit/s, V.22bis Hayes-compatible modem with send-fax capability and MNP 5 error correction. "We examined fax chips from several vendors, including our own digital-signal processors," says Vaughn Watts, TI's engineering manager for portable communication products at its Temple, Texas facility. "Our products consumed too much power and had too much horsepower for the application. Considering cost-performance ratios, we settled on a fax chip set from Sierra Semiconductor." TravelMate's fax hardware and software

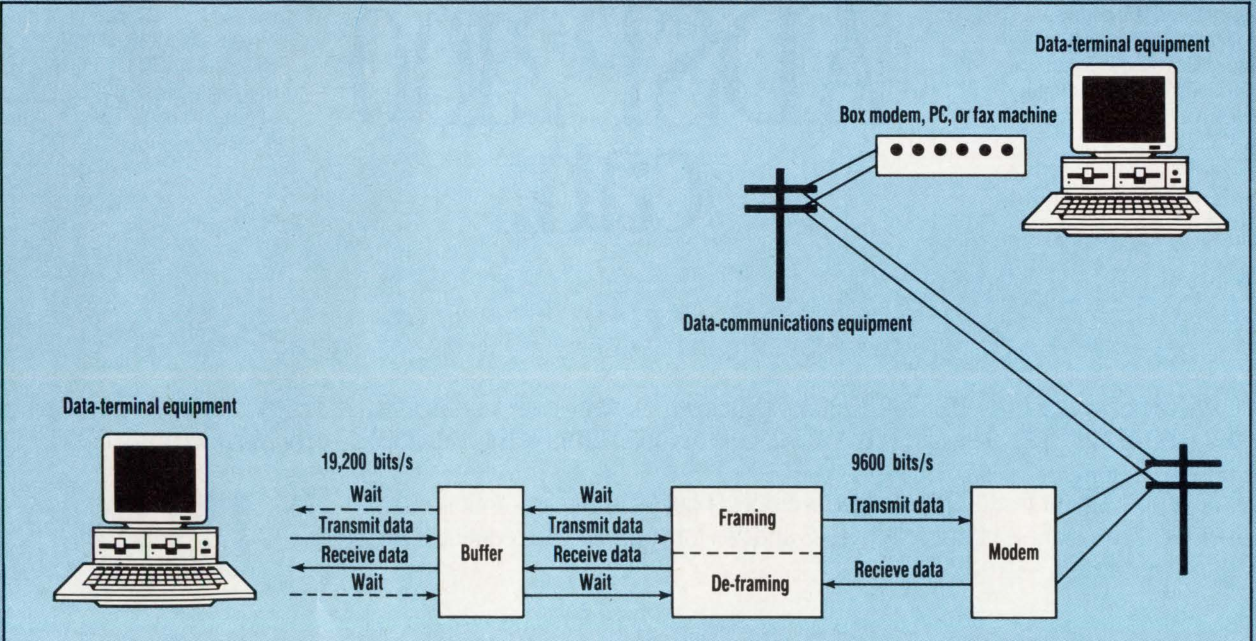
CONTROLLING DATA FLOW

A typical fax modem board has a data buffer for no data-flow interruption *(see the figure)*. For example, if the DTE is set for a 19.2-kbit/s rate and the modem connects at 9600 bits/s, data passes intact from the DTE to the modem as long as the buffer doesn't overflow or underflow. Maximum throughput is 9600 bits/s.

To avoid buffer overflow, both hardware and software flow-control methods are presently used to indicate to the DTE when it may or may not send data to the modem. With hardware flow control, the modem controls the CTS (clear-to-send) line and tells the DTE when it may or may not send data. Alternatively, the modem sends control characters (XON and XOFF) along the DTE's receive-data path to indicate when it may or may not send data. Conversely, the terminal can inform the modem, through hardware control, of its ability to receive data by controlling its request-to-send line, or by software control to send XON/XOFF characters on the transmit data path.

The modem can also provide error detection and correction using the Microcom Network Protocol (MNP) developed by Microcom Inc. Maximum modem-to-modem throughput depends on the class of connection used, and never exceeds the data rate of the slowest terminal. All classes of MNP support error detection and correction by using a 16-bit cyclic redundancy check sum (CRC) and retransmission. MNP 4 supports full-duplex operation, and MNP 5 adds run-length encoding and adaptive-frequency encoding (Huffman coding) for data compression.

Upon establishing a connection, two modems supporting MNP determine all mutually acceptable performance parameters. For example, if one modem is MNP 4 and the other is MNP 5, the resulting connection will be MNP 4.



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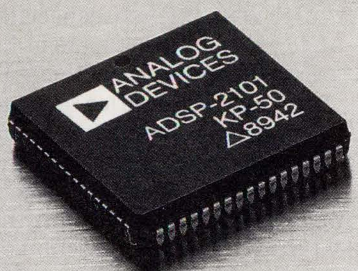

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offer dial-up scheduling, automatic retries, and alternate number dialing.

Future developments promised by fax-chip vendors include new devices with footprints under 3 in.^{2} and power dissipations well under the 0.5-W maximum now required for notebook PCs. "Next to come, especially from major fax manufacturers in Japan, is implementations of the V.17 standards, which specifies a 14.4-kbit/s data rate," says Exar's Dujari. "To meet this performance, the industry will use 2D compression, which compresses data in both the horizontal and vertical directions." Furthermore, V.17 specifies a forward-error-correction mode to ensure data integrity.

Dujari says the color fax standard, which is still being finalized, will require more complex hardware and software. It doesn't, however, pose terribly difficult technical problems—especially for a PC-to-PC application. Vendors also see no reason why future PCs can't have voice capability. Because a modem chip already has an analog-to-digital converter, a card could store digital voice messages as well as data. However, memory capacity might be a problem.

For instance, a telephone line has a 6-kHz bandwidth. Taking 8-bit samples of a 3-kHz voice spectrum at the Nyquist frequency of 6 kHz generates 48 kbits/s. Without compression, the computer would have to store 48 kbits for each second of speech. Applying 4:1 compression would enable four seconds of speech to be stored in the same space (comparatively, a page of faxed text now takes about 34 kbytes of memory space). Users could decide the sampling frequency necessary to get the desired speech quality within disk-capacity constraints. More advanced algorithms can deliver compression ratios much higher than 4:1 for voice applications.□

How Valuable?	**Circle**
Highly	541
Moderately	542
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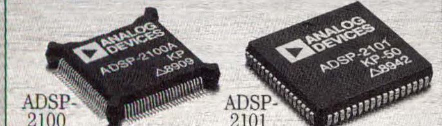

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ANALOG DEVICES

CIRCLE 142

ARCHITECTURAL MODELS ARE KEY TO SYSTEM-LEVEL DESIGN

USE THE TOP-DOWN METHOD WHEN DESIGNING COMPLEX SYSTEMS BY USING LARGER BEHAVIORAL BUILDING BLOCKS

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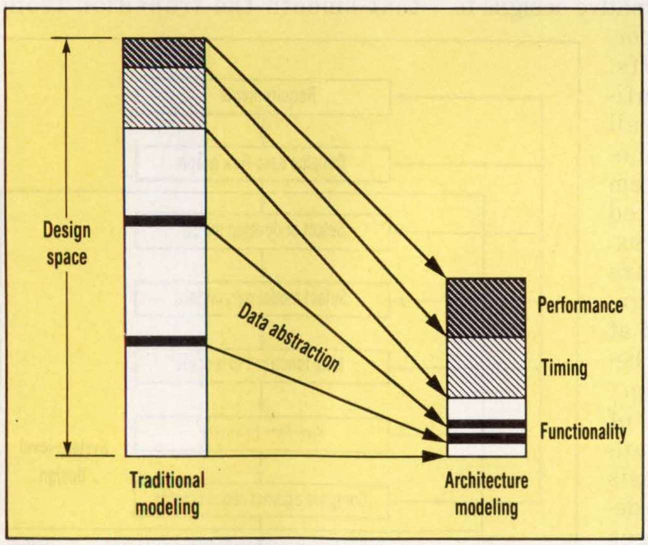
Mounting cost constraints and time-to-market pressures are forcing engineers to tackle increasingly complex electronic designs. And as designers strive to keep pace, their own methods are being reshaped by two ideas: concurrent engineering and a top-down approach to design.

The majority of electronic design engineers will use top-down methodology by 1995, predicts Dataquest, a San Jose, Calif., market researcher. Today, top-down methods are spreading to designing VLSI circuitry, board-level products, and other electronic systems that integrate hardware and software elements. In the future, electrical and computer-design engineers will become system engineers, spending most of their time working at the behavioral level.

But just what is a top-down design methodology? How does it relate to concurrent engineering and how can typical engineering organizations apply it to common design applications? What are the important ingredients to make this approach work? First, some problems hardware designers face today will be examined, followed by a methodology that uses behavioral models to implement a top-down approach to design. Also included is an example that shows how this approach works in designing a custom hardware architecture for an image-processing algorithm.

Architectural models are critical to evaluating designs before they're implemented. Similar to behavioral models, architectural models differ in that they support component sharing. These models can self-check the order and timing of input signals to identify functional problems, which may result in timing errors. Architectural models, an integral part of top-down design, have four important properties *(Fig. 1)*:

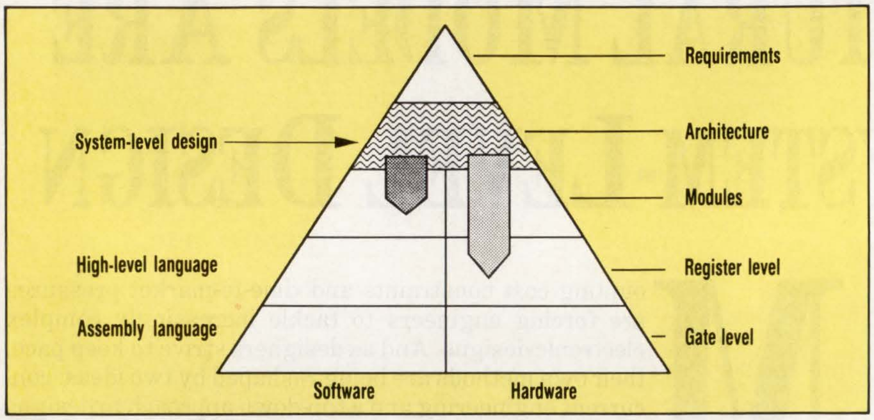
- They accurately capture the functionality of hardware and software components using a high level of data abstraction in data-flow form.
- Architectural models abstract implementation technology in the form of timing parameters. The ultimate values of these parameters determine a specific implementation technology.
- The models include arbitration schemes for sharing of components by multiple functions.
- These models should be parameterized, typed, and reusable.



1. ARCHITECTURAL MODELS, which are integral to top-down design, use data abstraction to accurately capture the functions of hardware and software components. The models abstract implementation technology in the form of timing parameters and include arbitration schemes so that multiple functions can share components.

The simulation models execute quickly, without sacrificing the accuracy required for cost and performance analysis. With system-level simulation employing architectural models, designers can evaluate alternative system designs for functionality, performance, and cost trade-offs.

By definition, concurrent engineering requires that design engineers, from the outset, consider all aspects of the product life-cycle. This encompasses conception



2. TOP-DOWN DESIGN methodology supports concurrent engineering by developing system architectures that are primarily driven by functional requirements. It's also maintained by emphasizing codesign of hardware and software subsystems.

through disposal, including manufacturability, quality control, cost, schedule, and user requirements. Historically, systems engineering used concurrent engineering to develop large-scale commercial and military systems, such as the space shuttle or B1B bomber. Unfortunately, systems engineering lacked integrated design-automation tools with simulation capabilities. The methods and engineering processes weren't formalized.

Basically, the primary goal of concurrent engineering is to execute various design tasks in parallel and to reduce design iterations (engineering change notices) resulting from manufacturing and reliability problems. The focus of concurrent engineering, therefore, must be expanded to address the issue of defining system architecture, perhaps the most critical factor in terms of cost and performance. In most hardware designs, architectural problems are usually discovered when the costs to correct the flaw are prohibitive. The problem is never corrected, reducing the product's lifespan.

If concurrent engineering is to support the product-definition phase, the system engineering effort must be anchored by formal design methods and appropriate design-automation tools. Top-down design supports this effort because it lets designers develop system architectures driven primarily by functional requirements. This approach also stresses codesigning hardware and software subsystems *(Fig. 2)*.

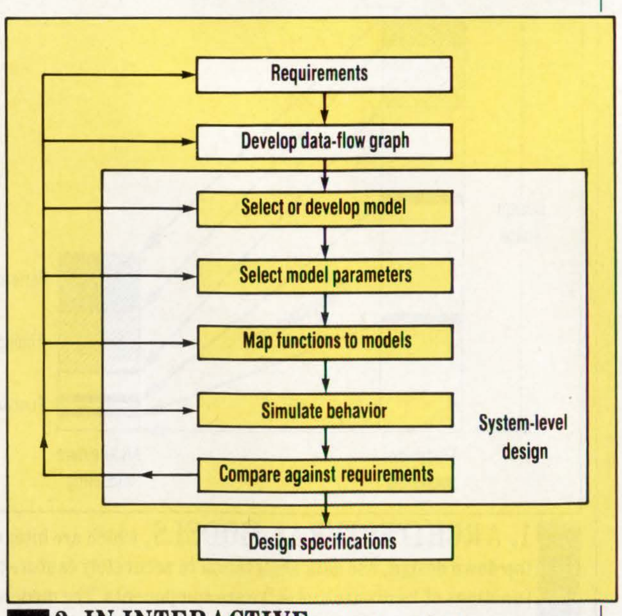
Because it incorporates evaluation and verification of designs at the system level, the top-down approach can produce optimal design specifications, which are correct by construction. The top-down paradigm aims to produce an optimal design specification, in block diagrams and state transition tables, for an electronic system that meets both functional and performance requirements.

Top-down design provides a focus not only on design validation but also on evaluating alternative designs to optimize cost and performance trade-offs. So designers' confidence and overall quality increase because the total system has been abstracted using the input of experienced software and hardware designers, and simulated at the system level before implementation.

The appearance of commercially available logic-synthesis tools and hardware description languages (HDLs) also helps focus attention on top-down design techniques. Logic synthesis supports the top-down approach by converting logic expressions into physically realizable gate-level descriptions. It also streamlines physical implementation. In addition, these descriptions efficiently use engineering time and layout patterns.

Logic synthesis supports a top-down design approach for generating gate-level design and provides local optimization of logic expressions within a few clock cycles. But complex designs of several hundred thousand gates can benefit from global optimization through system-level simulation and analysis. In these situations, top-down design requires behavioral models that represent both hardware and software components and use much higher abstraction levels than the gate- and cell-level models used in logic synthesis. These models are needed to perform system-level electronic design using commercially available system simulators.

Why is most hardware control logic usually implemented in a dozen or so states? And if the system becomes more complex, why is it typically partitioned so that each segment can be implemented in the predefined number of states? The reasons stem from the lack of a design methodology and supporting design-automation tools that smooth the transition from



3. IN INTERACTIVE system-level design, system-level functional specs are captured in data-flow form and component types are chosen to implement functions.

functional requirements to formal design specifications.

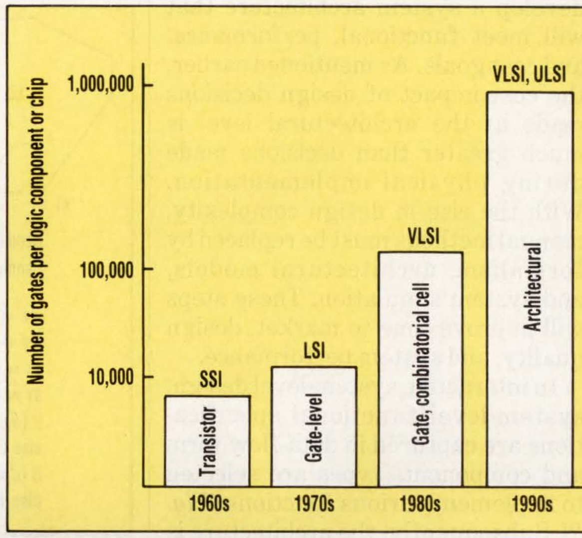
System-level design using architectural modeling helps make this transition by separating the concerns of functional requirements and design specifications. So the top-down approach offers a means for electronic-system designers to generate design specifications with hundreds of states that could be implemented using a hierarchical and concurrent finite-state machine (FSM).

Top-down design implies that design specifications are derived, preferably automatically, from functional specifications. Moreover, functional specifications are the primary source of guidance in designing complex systems. Consequently, this approach can reduce the typical ASIC system failure rate of 50%. Some of these failures are caused by inconsistencies between functional requirements and design specifications. Another potential benefit is the ability to develop efficient test waveforms to validate the design, and test vectors for manufactured parts.

The current bottom-up approach for electronic-system design typically begins with a schematic-capture system for design at the structural level. Once structure is determined, system behavior is captured with an HDL and simulated. With a top-down approach, the order of these two activities is reversed. Top-down design emphasizes a behavioral view of the application, not a physical or structural view. Of course, the top-down approach ultimately results in a structural or schematic representation of the design. The point is that system architecture models are necessary in top-down design, just as structural models are necessary for a bottom-up design approach.

To employ the top-down approach, designers must thoroughly understand the system's functional requirements, which are captured as executable behavior specifications. Top-down design also requires fast and accurate behavioral models, such as architecture models, that contain the functional and the timing properties of the components needed to implement these specifications.

The performance of these system-level models can be simulated by using system-level simulation software, such as the SES/workbench or Cadre's ADAS or with a hardware description language, like Verilog or VHDL. System-level simulation results offer a basis for quantitative design evaluation in a project's initial stages. In the later phases, gate-level simulation is appropriate for design validation. A uniform design environment throughout the design cycle enables designers to compare the results of simulations that are performed in the early and later stages of design.



4. THE 1990s will see a continuing upswing in the number of gates or components in a system, as the number of gates stretches to 1 million. With complex systems, designers can't rely on intuitively analyzing the designs and trade-offs using traditional gate or cell-level models. Instead, they must use behavioral models adapted to complex models.

With the top-down methodology, engineers can evaluate different design alternatives for a given set of requirements. This method also helps verify the correctness of a specific implementation at a high level of abstraction. To validate the design at a high level of abstraction, timing properties must be evaluated early in the design process, not just at the later stages.

In practice, a top-down approach establishes a parameterized system architecture and selects its optimal configuration parameters. Architectural models should also be parameterized to support this approach. These configuration parameters determine which functions are implemented in hardware versus software. In this way, top-down design supports concurrent engineering of both hardware and software designs. Some examples of hardware-configuration parameters are the number, size, and speed of buses in the system, memory-access time, cache-line size, number of ports on register files, and communication-buffer sizes. Software configuration parameters include scheduler parameters, such as task priority, garbage-collection interval, maximum allowed CPU time for a program; and memory-management parameters, such as page size, file allocation to disk sectors, and segment size. Communication-configuration parameters include time-out interval, fragment size, and protocol-related parameters for error handling.

System-Level Design

Electronic design of systems is traditionally ad hoc and manual—that is, without system-level design tools. The resulting architectures are thus derived mostly from the hardware engineer's experience. Most designers don't have a good feel for the quality and performance of system-design specifications due to the lack of a quantitative evaluation environment. System-level simulation using architectural models, the first step in top-down design, offers this type of design environment.

It's essential to identify the needs of complex-systems design and define properties of the behavioral models (architecture models) needed to support this task. The primary task in electronic-system design is to develop a system architecture that will meet functional, performance, and cost goals. As mentioned earlier, the cost impact of design decisions made at the architectural level is much greater than decisions made during physical implementation. With the rise in design complexity, manual methods must be replaced by formalism, architectural models, and system simulation. These steps will improve time to market, design quality, and system performance.

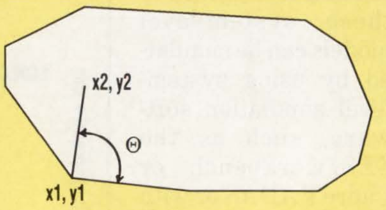
In interactive system-level design, system-level functional specifications are captured in data-flow form and components types are selected to implement various functions *(Fig. 3)*. Subsequently, the architecture is optimized to reduce the cost and to increase performance. This optimization process involves grouping functions that can share physical instances and designing controllers to arbitrate use of these instances by various groups of functions. In general, designing controllers means changing the component selection type and requires iteration among these tasks.

The component architectural models used in system-level design need to support component-sharing, represent functionality at a high level of data abstraction, and represent time accurately.

Complexity, measured by the number of gates or components in a system, will keep increasing in the 1990s. Electronic-system designs have grown more complex during the last four decades and the behavioral model has evolved accordingly *(Fig. 4)*. As these systems become more complex, designers are less able to intuitively analyze designs and make trade-offs using traditional gate- or cell-level models. Pressure to reduce time-to-market involves using larger building blocks, even at the expense of performance, to develop complex designs. Larger building blocks usually require the input and output ports to be shared, and include multistate behavior.

Modeling primitives that represent the design at the architectural level need to support sharing of I/O ports and multistate behavior.

Using architectural models is significant because they will reduce design space to a manageable level—very similar to the transition from transistor-level design in the 1960s to gate level in the 1970s *(Fig. 4, again)*. In addition, architectural models must be implemented in a computationally-efficient manner so that system-level simulation is completed in reasonable time. Architectural models with system simulation capability provide a computer-aided, top-down design environment, which helps to formalize the design process. Initially, the design in this environment can be represented concisely and then can be refined at higher levels of resolution as the project progresses.



Seed coordinates (x1, y1)
Candidate point coordinates (x2, y2)

$dx = x2 - x1$
$dy = y2 - y1$
$ax = abs(dx)$
$ay = abs(dy)$
if $(dx==0 \&\& dy==0)\ \Theta = 0$
else $\Theta = dy/(ax + ay)$
if $(dx < 0)\ \Theta = 2 - \Theta$
else if $(dy < 0)\ \Theta = 4 + \Theta$

5. A CONVEX-hull-algorithm design illustrates top-down design in a computationally intensive image-processing algorithm. The algorithm determines the image data's hull points. As shown in the algorithm, the angle of all image data to the point on the hull is computed repeatedly. The lowest angle point is selected to be the next hull point, and the process is repeated.

Most applications require flexibility, which is typically implemented in software. But implementing repetitive and well-defined functions in hardware often results in better performance. Specialized hardware can be developed for a custom application, usually in the form of ASICs. These designs require concurrent engineering of hardware and software modules.

Architectural models of electronic systems should represent the behavior of both hardware and software implementations of specific functions.

Convex-Hull Example

To illustrate the top-down approach, consider the design of a hardware system to implement a computationally-intensive, image-processing algorithm. The algorithm determines the image data's hull points *(Fig. 5)*. As shown in the algorithm, repetitive angle computation of all image data to the point on the hull is necessary. The lowest angle point is selected to be the next hull point and the process is repeated.

Angle computation is typically implemented in software, which provides satisfactory performance for interactive applications. However, this computation must be finished in 16.66 ms (frame speed) to support animation applications. This algorithm example describes a hardware implementation of the angle-computation portion of the algorithm and the performance characteristics of two alternative hardware design solutions. The rest of the algorithm, which downloads the image data in the RAM and uploads the hull points from the RAM, is still implemented in software.

The design objective is to evaluate

TABLE 1. COMPUTATION TIME

Condition	Architecture 1	Architecture 2
1. dx = 0, dy = 0	476 ns	965 ns
2. dx < 0	2805 ns	3765 ns
3. dy < 0	3045 ns	4005 ns
4. else	2885 ns	3845 ns

TABLE 2. COMPONENT UTILIZATION

% utilization	(dy < 0) Architecture 1	Architecture 2
BUS	17.07	25.9
ALU	19.21	33.33
RAM	29.37	47.47

alternative hardware architectures to compute the angle and to verify the design's functional and timing properties. Alternative architectures are evaluated through system-level simulation to determine the cost-performance trade-offs involved, such as number of buses, RAMs, and divide chips. This approach is based on behavioral modeling and simulation using an architectural library of component models. All component models were based on data-book specifications of components from major IC manufacturers.

A pipeline architecture using multiple buses was selected to maximize throughput. Two different architectures were simulated for performance and functional evaluation *(Fig. 6)*. The primary differences between the two designs are the number of buses and components dedicated to processing of angles in the the convex-hull algorithm. The number of components determines the number of angles computed per unit time. It's assumed that scheduling depends on data values.

The procedure to develop a hardware design for the convex-hull algorithm illustrates the top-down approach, as follows:

1. First, generate a data-flow graph.
2. Next, select required components from the component library.
3. Abstract timing properties.
4. Build architectural models of these components.
5. Map functions in the data-flow graphs to these component models.
6. Evaluate simulation results to determine system performance and component utilization.

Alternative architectures are evaluated through iteration in steps 5 and 6.

The top level of the SES/workbench simulation model for the angle computation illustrates the mapping of functions to components *(Fig. 7)*. Each component instance is contained in a submodel (the next level in the hierarchy), and can be referenced from the top level of the hierarchy. The algorithm that calculates the coordinates of the image is contained in the submodel hull_grf *(Fig. 8)*.

Simulating Behavior

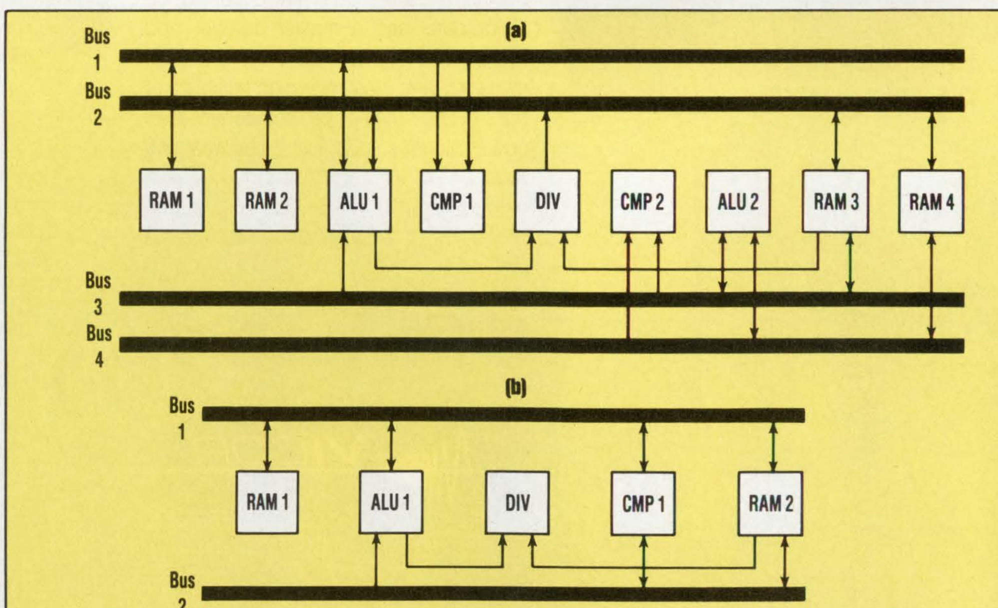
The hull_grf submodel captures functional behavior to represent angle computation. It includes logical references to the physical instance graph for the second architecture. Four concurrent RAM accesses are made for the X and Y coordinates for both the hull point and an image point (represented by the subgraphs ram_11, ram_21, ram_31, and ram_41). After RAM access, these data values are transferred on their respective buses: bus_11, bus_21, bus_31, and bus_41. These values then arrive at ALU_11 and ALU_21 for arithmetic computation. After computation, the values need to access the bus again.

All bus transfers refer to bus_1 and bus_2. However, bus conflict needs to be resolved. Because this is a pipeline design, new angle computation starts before the computation of the previous angle is completed, and can result in bus-allocation conflict for multiple angle computations. Similar conflict could arise in the sharing of ALUs and RAMs.

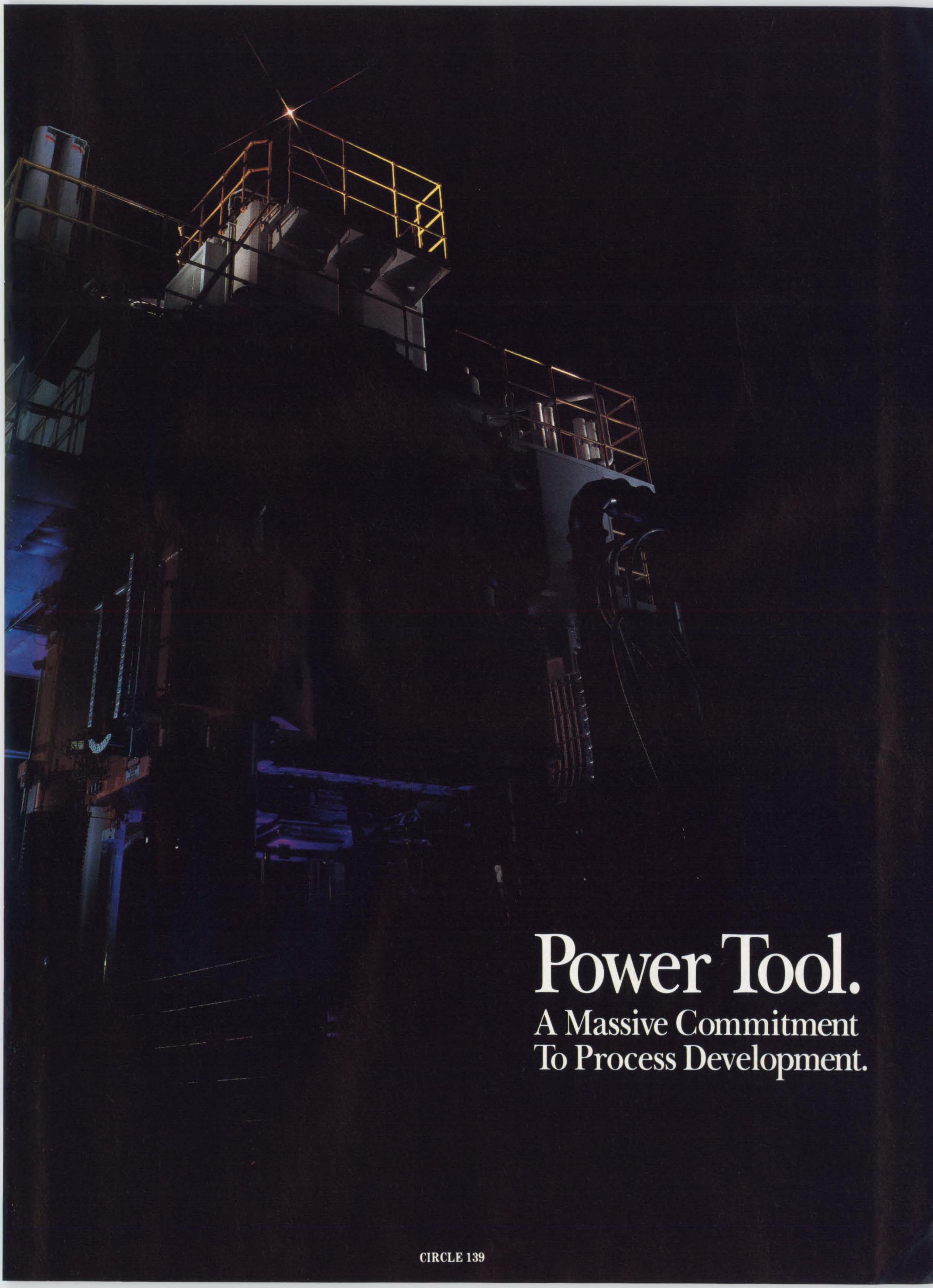
Different architectures are constructed merely by changing the referenced component graph name. Component mapping requires a designer's experience, intuition, and creativity. The resulting system architecture depends directly on component mapping and determines the final design's overall cost and performance. In general, an optimal mapping algorithm takes extensive computational time, which increases exponentially with design size.

The architectural model of the ALU is represented graphically in SES/workbench *(Fig. 9a)*, and textually in Verilog *(Fig. 9b)*. Both models are based on data for the SN74S381 from Monolithic Memories Inc., Santa Clara, Calif. They initially check availability of the input signals for the computation and then the availability of the ALU itself. Afterward, they compute the actual function.

The ALU model computes various arithmetic and logic functions. The Function-Select signal determines



6. TO IMPLEMENT **the algorithm, a pipeline architecture using multiple buses was chosen to maximize throughput. To evaluate performance, two architectures were simulated (a and b). The two designs differ in the number of buses and components to process the convex hull algorithm. These numbers change the amount of angles computed per unit time. Scheduling depends on data values.**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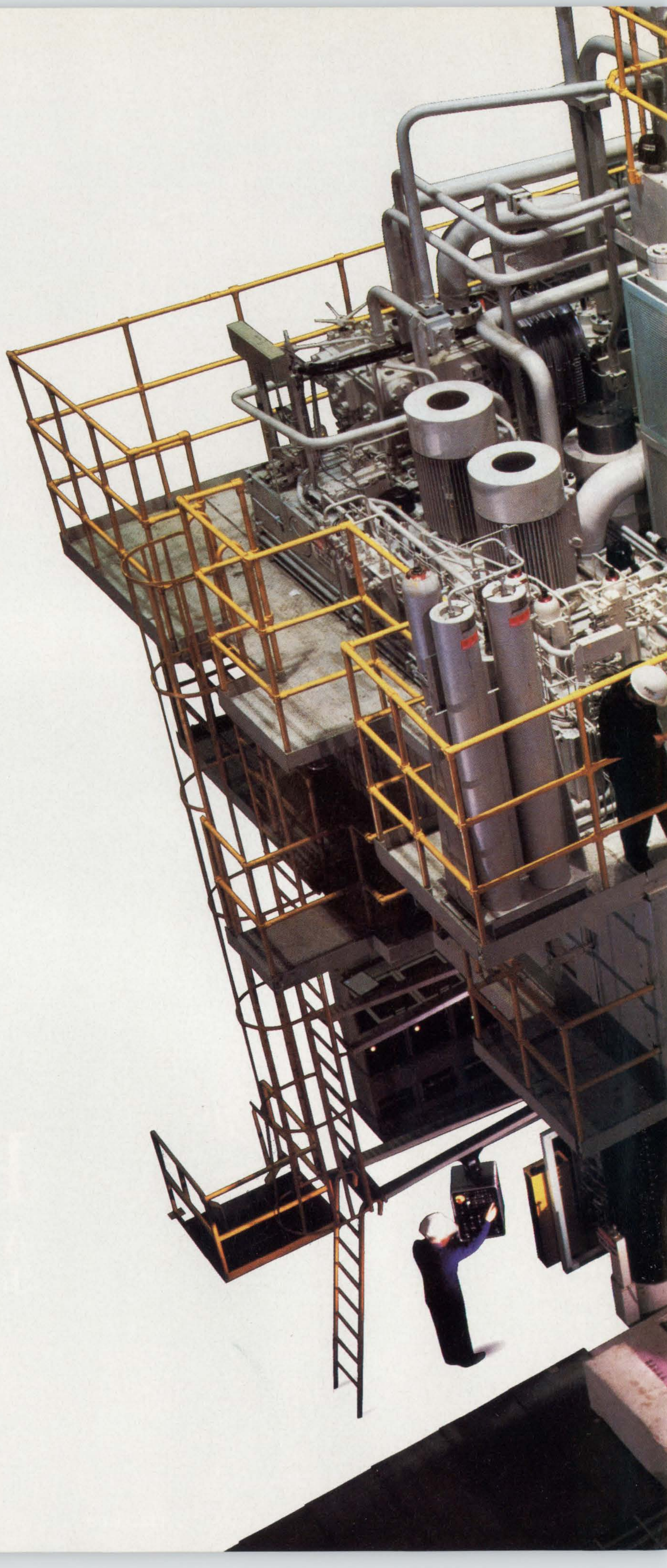
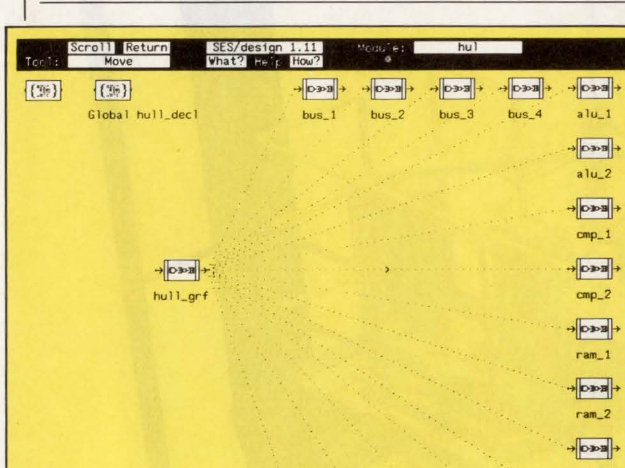



DIEFFENBACHER
ALPHA 1
KRAUSSMAFFEI



7. THE TOP LEVEL in the SES/workbench simulation model for angle computation illustrates function mapping to components. Each component instance, contained in a submodel (the next level in the hierarchy), can be referenced from the top level of the hierarchy.

which function will be executed. The model provides s_del and f_del as parameters to represent the execution times for these two operations. In general, different ALUs have different parameter values.

System-level simulation determines the computational time under the four scenarios described earlier in the algorithm for both architectural designs *(Tables 1 and 2)*.

These results bring out the cost/performance trade-offs for the two system architectures. The system design in Architecture 2 costs about 50% less than Architecture 1 because it has fewer components that are more highly utilized, as in dy < 0. But what about performance? In Table 1, angle computation time was used as a performance metric. The simulation results show that Architecture 2's overall performance was 70% of Architecture 1, with an even higher percentage under certain conditions. Conversely, Architecture 1 has 31.8% higher throughput (number of angles computed per unit of time) than Architecture 2.

In general, the convex-hull example shows how a computationally-intensive, signal-processing algorithm—traditionally implemented in software—can be implemented in hardware at the chip or board level to enhance performance to support animation applications. Specifically, this example describes an architectural model of an ALU, which represents functionality using "c" data structures in SES/workbench and behavioral language in Verilog. This model represents timing as parameters s_del and f_del, whose values determine a specific type of ALU. It also illustrates component sharing among multiple functions, which is implemented by wait statements in Verilog and use of the Block node in SES/workbench.

The hull example also illustrates the utility of the architectural models in the rapid construction and evaluation of alternative architectures for the application. These architectural models were constructed and evaluated in less than two weeks.

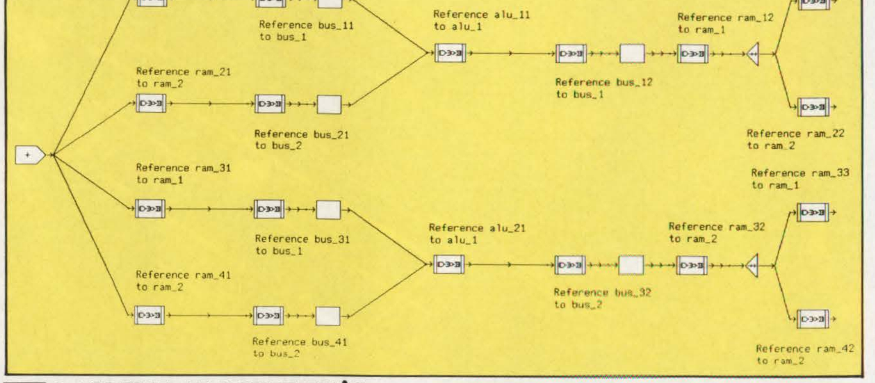
The representation of software and hardware behavior in data-flow form is reflected in this example. The algorithm requires downloading the image point in the RAM and uploading of the computed hull points from RAM, which are performed in software and represented using the same data-flow form.

This approach provides a basis to quantitatively evaluate a design implementation using custom hardware or software that executes on a system with or without a floating-point processor. The time to compute the hull coordinates for an image with 512 image points and 50 hull points took 15 ms for architecture 1. This same computation would take 90 ms in software running with a floating-point processor and 700 ms with software without a floating-point processor.

A WORKING APPROACH

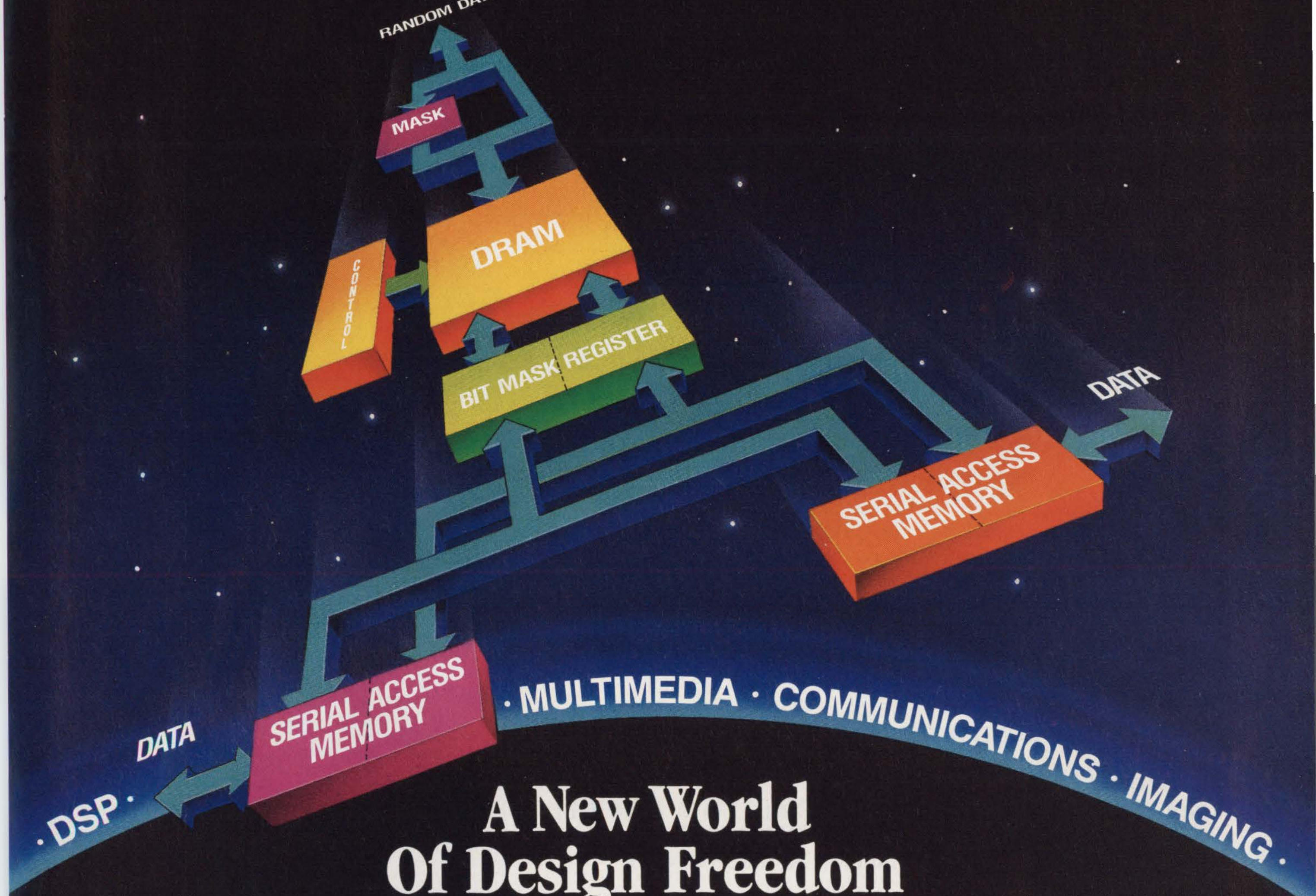
The design approach in the convex-hull example has been used by CAE Plus and other companies, such as AT&T, DEC, NCR, and Texas Instruments, for performance analysis of large-scale software and hardware systems. CAE Plus developed an architectural model library of software, hardware, and communication components, including the Network File System, Ethernet, Sparc, and MIPS RISC microprocessors, plus such buses as VME and MBUS. The company applied the top-down methodology by using these models in designing new systems and debugging existing designs of complex electronic systems.

Top-down design methods are



8. IN THE ALGORITHM'S SES/workbench model, the algorithm that calculates the image coordinates is contained in submodel hull_grf.

Triple Port DRAMs



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ARCHITECTURAL MODELS

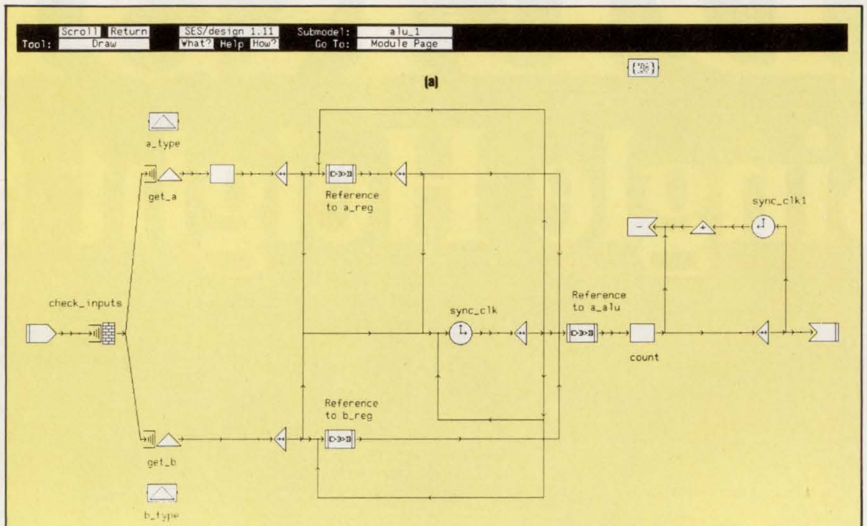
widely discussed but rarely implemented because the concept and organizational issues are somewhat unclear. Typically, architectural modeling saves money for an engineering organization, following an initial transition period or learning curve. The payoff is the reduced number of design flaws that could result in redesign, manufacturing iteration, or shorten product lifespan.

However, the top-down approach requires that electrical and computer engineers change their view of the design process. Because the top-down approach emphasizes behavior, designers will spend more time at this level rather than on physical implementation. Generating design specifications from functional requirements involves much creativity. Working with control and data flow among logical components is unfamiliar territory, underscoring the need for education and training. There is a lack of formal courses in top-down design.

The top-down approach supports codesign of hardware and software. It also offers an opportunity to reexamine the traditional and fictitious boundaries between hardware and software engineering disciplines.

Successfully implementing a top-down design approach also requires a set of CAE tools that communicate with each other. Specialized in-house and third-party software tools for electronic-system design are driving the need to integrate these tools within a unified framework. Tool integration is necessary for designers to traverse multiple levels in the design process from architectural modeling to layout. A common hardware-description language, such as Verilog or VHDL, enhances the capability to synthesize physical implementation of the design from design specification. This ability enables designers to work at the behavioral level of abstraction where leverage in the design cycle is greatest. It's also extremely beneficial in manufacturing general-purpose and custom integrated circuits.

The top-down approach takes a component-oriented view to designing complex electronic systems. Engineering organizations must develop a library of logical components, like those used in the example, so that they can be shared or reused in other design projects. The convex-hull architectural model required about two engineering weeks to develop using the component library.□



(b)

```
Jan  3 18:01 1991  new_shared_alu.v Page 1

module shared_alu;

// This module checks for the availability of select signal
// then for the availability of input data
// then for the availability of the alu
// and finally then computes the arthmatic operation.

reg[1:0] A1_token,A2_token,B1_token,B2_token, S1_token,S2_token,ALU_token;
reg[7:0] S1,A1,B1,S2,A2,B2, s,a,b,out;
parameter s_del =10, f_del = 40;

initial setup;
always  alu_control;

task alu_control;
begin
        wait (S1_token || S2_token);
        # s_del;
        if (S1_token == 1)
                begin
                        wait (A1_token && B1_token);
                        wait(ALU_token);
                        compute(S1,A1,B1);
                        A1_token = 0;
                        B1_token = 0;
                        S1_token = 0;
                end
                else
                begin
                        wait (A2_token && B2_token);
                        wait(ALU_token);
                        compute(S2,A2,B2);
                        A2_token = 0;
                        B2_token = 0;
                        S2_token = 0;
                end
end
endtask

task compute;
input[7:0] s,a,b;
begin
        shared_alu.ALU_token = 0;
        case (s)
                8'd0:   out =0;
                8'd1:   out = b-a;
                8'd2:   out = a-b;
                8'd3:   out = a+b;
                8'd4:   out = 0;
                8'd5:   out = a|b;
                8'd6:   out = a&b;
                8'd7:   out = 'bx;
        endcase
        # f_del;
        shared_alu.ALU_token = 1;
        $display ($time,"     out = ", shared_alu.out);
end
endtask


task setup;
begin
                ALU_token = 1;
```

9. THE ARCHITECTURAL MODEL of the ALU in SES/workbench and the same component model in Verilog are based on data for the SN74S381 from Monolithic Memories. Both models first check the availability of the input signals for the computation, then the ALU's availability. Next, they compute the actual function. This flow is represented graphically in SES/workbench (a), and textually in Verilog (b).

Prem P. Jain, president of CAE Plus, holds MS and PhD degrees in electrical engineering from Rensselaer Polytechnic Institute, Troy, N. Y.

Acknowledgment:
The convex-hull example is from research conducted by Nehal Desai. The author would like to thank John R. Mannix for his help in preparing this article.

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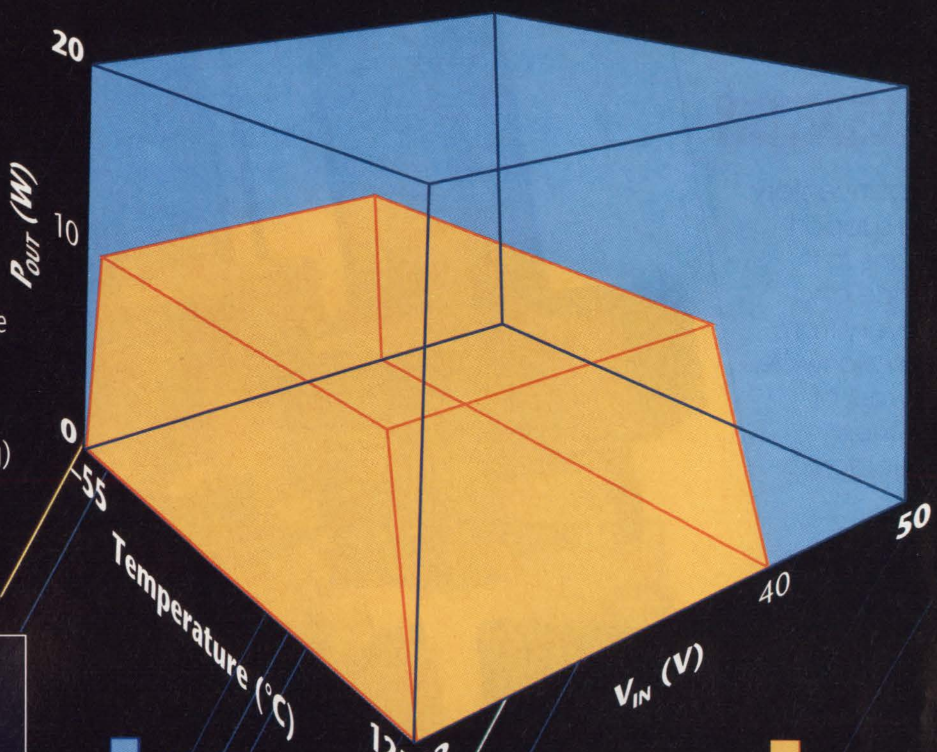

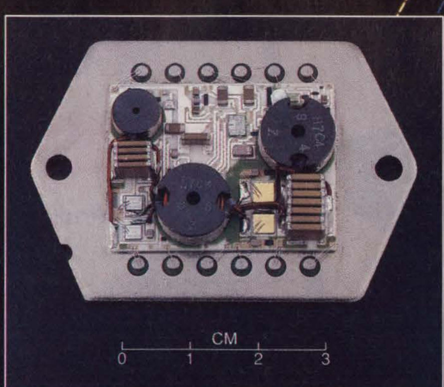

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A SPECIAL EDITORIAL FEATURE

PIPS

POWER • INTERCONNECTIONS • PASSIVES • SWITCHES • RELAYS

ELECTRONIC DESIGN

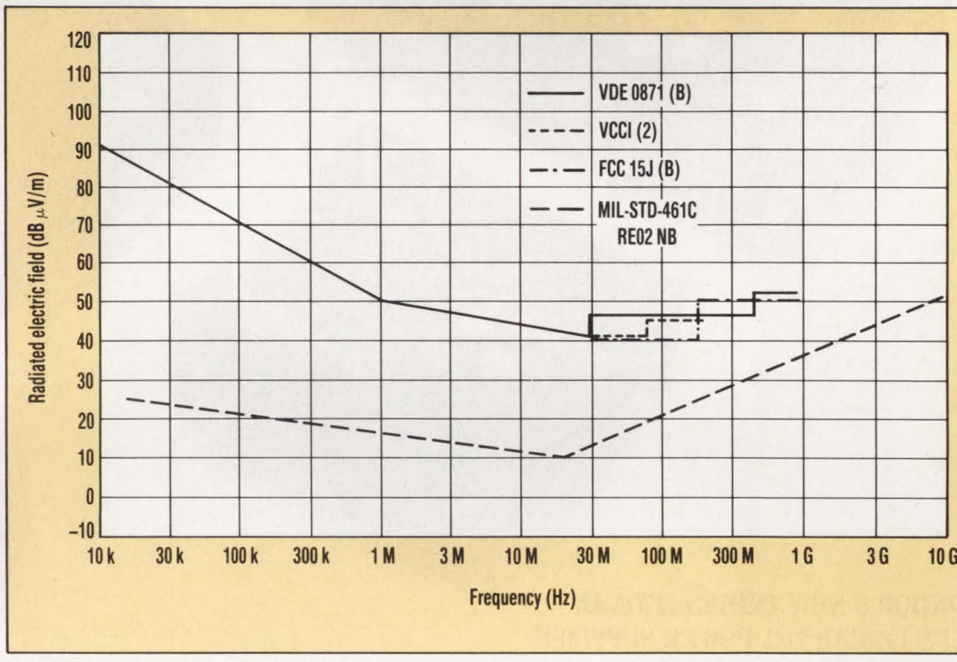
Suppress EMI/RFI From The Ground Up

Choice of logic speed, layout, and multilayer design help pc boards meet specifications.

BY RONALD W. BREWER
Instrument Specialties Co. Inc., Delaware Water Gap, PA 18327-0136; (717) 424-8510.

Suppression of high-frequency radiation, as it relates to computer design, reflects present government requirements as well as the industry's technological and commercial evolution. Also referred to as electromagnetic or radio-frequency interference (EMI/RFI), radiation from commercial equipment is governed by the FCC under Part 15, Subpart J, which applies to digital devices and systems that use timing signals with frequencies greater than 10 kHz.

Military equipment is subject to MIL-STD-461, which includes susceptibility requirements in addition to radiation limits. Forthcoming European CENELEC (Community European Normalization Electrotechnical) standards will also contain susceptibility requirements similar to the current VDE standards *(Fig. 1)*.



1. Radiated emission limits are shown for FCC Part 15 J(B), VDE0871(B), VCCI(2), and MIL-STD-461C. All limits have been normalized to a 3-meter measurement distance.

Commercial requirements limit the amount of RF noise that business- and home-computing devices may impart to electrical-power systems, as well as radiated energy that can interfere with other electronic equipment. If compliance with radiation requirements plagues manufacturers, it's typically because they haven't factored it into system design. Developmental testing is critical to meeting both regulatory standards and performance specifications.

Radiation emitted by electronic devices results from differential- and common-mode currents. In semiconductor devices, differential-mode currents flowing synchronously through two separate loops produce radiating electromagnetic fields. One type of loop is formed by the printed-circuit-board traces or rails that supply power to the semiconductor devices. Another type is created by the logic signals transferred from one device to another, which return by means of the power-distribution rails.

In contrast, common-mode radiation results from voltage drops in the system that create common-mode potential with respect to ground. Moreover, parasitic capacitive coupling, a difficult-to-control phenomenon occurring between conductive materials, makes external cables act as antennas.

Radiation from current loops in the far field may be calculated as follows:

$E = 1.316 (f^2 \times A \times I)(1/r)(1/SE) \sin \theta$

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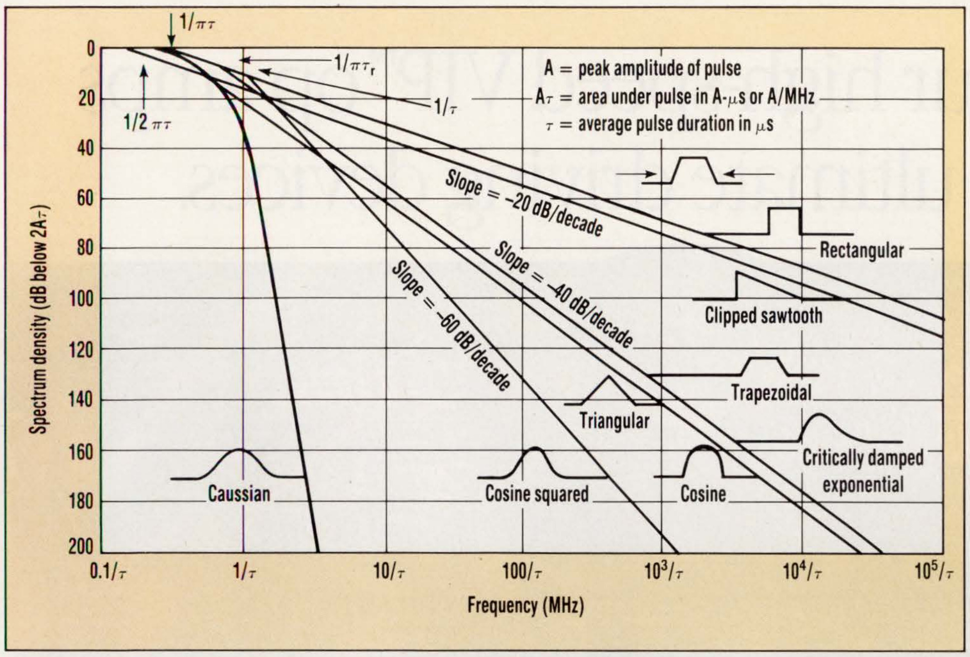


2. This chart compares the EMI characteristics of analog, low-speed digital, and high-speed digital logic.

where:

- E is volts/meter
- f is the frequency in MHz
- A is the radiating-loop area in cm^2
- I is the current in amps
- r is the measurement distance in meters
- SE is the shielding-effectiveness ratio
- Sin θ is the angle of the measuring device in relation to the plane of the radiating loop, which in the worst case equals one.

This equation must be modified to calculate emissions for regulatory agencies, most of which call for measurements to be performed over a ground plane rather than in free space. Because in-phase ground reflection can add as much as 6 dB to the measurement at higher frequencies, the equation should be multiplied by a factor of two.

Therefore, the radiation emitted by an unshielded 100-cm^2 loop carrying 8 mA of current at 30 MHz at a distance of 3 meters is 315.84 μV/meter, or 50 dBμV/meter. This result is more than three times the permitted FCC level of radiation for a Class B residential computing device *(Fig. 1, again)*. The 8-mA current is typical for a single logic device and associated wiring on a small printed-circuit board.

The calculation assumes a single-frequency sine wave, whereas most digital devices produce square or trapezoidal waves that contain an infinite number of sine-wave harmonics. Therefore, the Fourier series of the current must be determined to solve the equation for the various harmonic levels using:

$$I(n) = I\left[\frac{\sin(0.5n\pi)}{0.5n\pi}\right]\left[\frac{\sin(n\pi\, t(r)/T)}{n\pi\, t(r)/T}\right]$$

where

- I is the peak-to-peak amplitude of the wave
- T(r) is the rise time
- T is the period
- n is the harmonic number

This equation yields the harmonics amplitude envelope for a symmetrical trapezoidal wave. From $1/\pi T$ to $1/\pi Tr$, harmonics decrease at a rate of 20 dB/decade of frequency. Beyond that, they decrease at 40 dB/decade. Significantly, rise time determines energy in the latter range. The frequency factor in the equation must account for this increase.

The increases in EMI brought on by the evolution from analog to high-speed digital logic can be graphically depicted *(Fig. 2)*. The cosine-squared pulse with a slope of –60 dB/decade represents analog equipment, the trapezoidal shape with a slope of –40 represents low-speed digital, and the rectangular pulse with a slope of –20 represents high-speed digital logic.

Combining the first and second equations shows that because the radiating efficiency of the loop is increasing, the emission levels increase at 20 dB/decade with frequencies from $1/\pi T$ to $1/\pi Tr$ and plateau above this frequency. It also illustrates the direct correlation between rise times and radiated emissions and maintenance of increased amplitude in the higher frequency ranges.

The faster the logic speed, the more difficult it is to control radiated emissions. Generally speaking, the threshold to major interference problems lies at 50 MHz. The trend, however, continues to move toward higher frequencies. The fundamental frequency is 3 MHz for CMOS, 30 MHz for TTL, 150 MHz for ECL-10K, and 400 MHz for ECL-100K. But the harmonics of these devices can be 10 to 100 times greater in frequency than their fundamentals. And gallium arsenide devices now being used in sophisticated military applications operate at 4000 MHz—with some experimental applications running at more than 18,000 MHz.

Because the choice of logic family determines both operating current and frequency, board designers should select the lowest possible operating frequency and current consistent with the system's performance requirements. For example, TTL drivers use bipolar npn transistors that can create uneven current in the ground rail,

which results in EMI. Moreover, acute high-to-low transitions impart high-frequency energy to the negative supply rail, thereby producing emissions. Using CMOS instead of TTL means designs with much lower EMI levels. Earlier generations of CMOS, such as the 4000 series, generated much lower EMI levels because the MOSFET semiconductors used to switch voltage had higher impedance than bipolar devices. As a result, they lost drive capability as the output voltage approached the supply rails. This effectively rounded the waveform which, in turn, rolled off high-frequency harmonics.

But today's high-speed CMOS families, such as 74HC, incorporate lower-impedance output devices. Concurrently, higher operating speeds give rise to contention, a phenomenon that results from periodic, synchronous operation of P- and N-channel devices during logic transition. This condition can create a pulse in the supply-rail current, making HC logic even more of an EMI problem than equivalent TTL logic.

Contention also occurs when many devices access a bus at once. This can be controlled by careful design of the bus structure and timing elements.

A basic tenet of electromagnetic-compatibility (EMC) engineering is to suppress interference at its source. By dramatically reducing radiating-loop areas, large-scale ICs can offer as much as a 90-dB improvement in interference levels compared with discrete transistors. A typical pc board, however, contains numerous ICs, each of which may contain thousands of transistors. So a board with 20 DIPs may have as many as 20,000 individual sources of interference, each with its own associated loop that acts as one, coherent broadband emitter. As a result, interference levels reduced by using LSIs is lost.

To minimize these radiating loops, specific functional circuits should be confined to the smallest possible area, especially on multifunction boards that combine digital, analog, or mixed-logic devices. High-frequency devices and their associated circuits should be segregated and positioned so as to reduce the effects of capacitive and inductive coupling *(Fig. 3)*. This will help prevent contamination of low-frequency circuits by high-frequency currents.

The signal clock is generally the highest-frequency device in a system, and the logic devices are synchronized to it. As a result, clock-synchronous systems concentrate the energy of every logic device into narrow frequency-coherent components that combine to create radiation levels higher than any individual device can create.

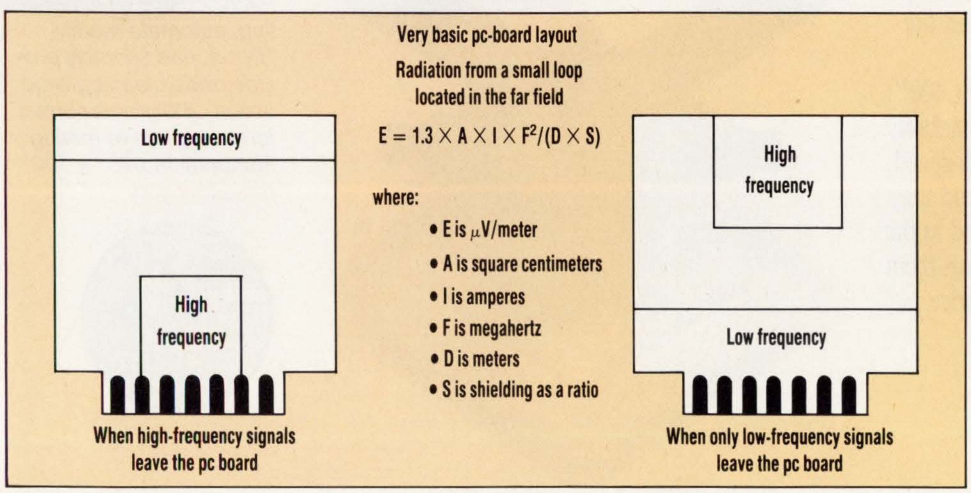
As the trend continues toward faster rise times and higher fan-out, system designers should make a concerted effort to use clocks that draw the least amount of current and still perform satisfactorily. Other criteria for suppression include slower rise times that yield weaker harmonics and operation over a narrow frequency range.

The negative connection to the power supply, or ground, is critical to clock design. Because wires and traces at RF act as inductors rather than short circuits, this connection should be a very low impedance. Although inductance varies with width and proximity to metal objects, 20 nH/in. is a good working estimate. At 100 MHz, the impedance of a 1-in. trace inductance would range from 10 to 20 Ω.

Inductive grounds, as in the case of a TTL inverter used to buffer a clock, can generate emissions. As it sinks more current than it sources, the inverter pulses current back through the ground rail. This creates a potential difference between the power supply and the gate ground pin, as well as RF voltage on the chip.

A 20-MHz TTL inverter at full fan-out produces some 200 mV of RF potential between the power-supply return and the clock-driver ground. When routed to other devices on the board, such as I/O drivers, the clock-driver ground can radiate emissions up to 20,000 μV/m at 3 meters, which is more than 200 times the FCC Class B limits. In addition, the circuit's outputs feed RF voltage to I/O cables, which also radiate noise.

The board designer not only must reduce the magnitude of the pulses fed back into the supply, but also must lower supply-rail impedance. Although convenient and economical, prepackaged clock oscillators exhibit fast rise times and high fan-out. Because of differences in design, some oscillators produce faster, higher-current signals than others, and the RF noise



3. High-frequency devices should be segregated from low-frequency units and positioned as close as possible to the backplane and connectors when their signals leave the board. Conversely, they should be positioned as far as possible from the backplane and connectors when high-frequency signals don't leave the board. This reduces the effects of capacitive and inductive coupling and helps prevent low-frequency circuits from being contaminated by high-frequency circuits.

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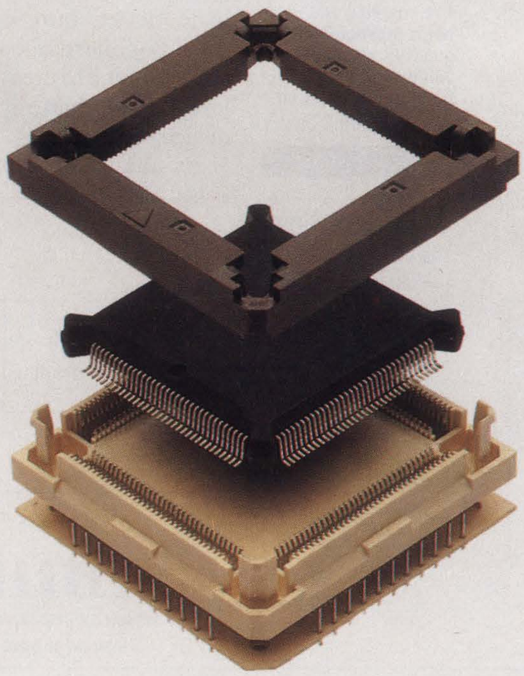

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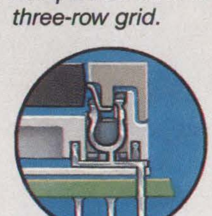
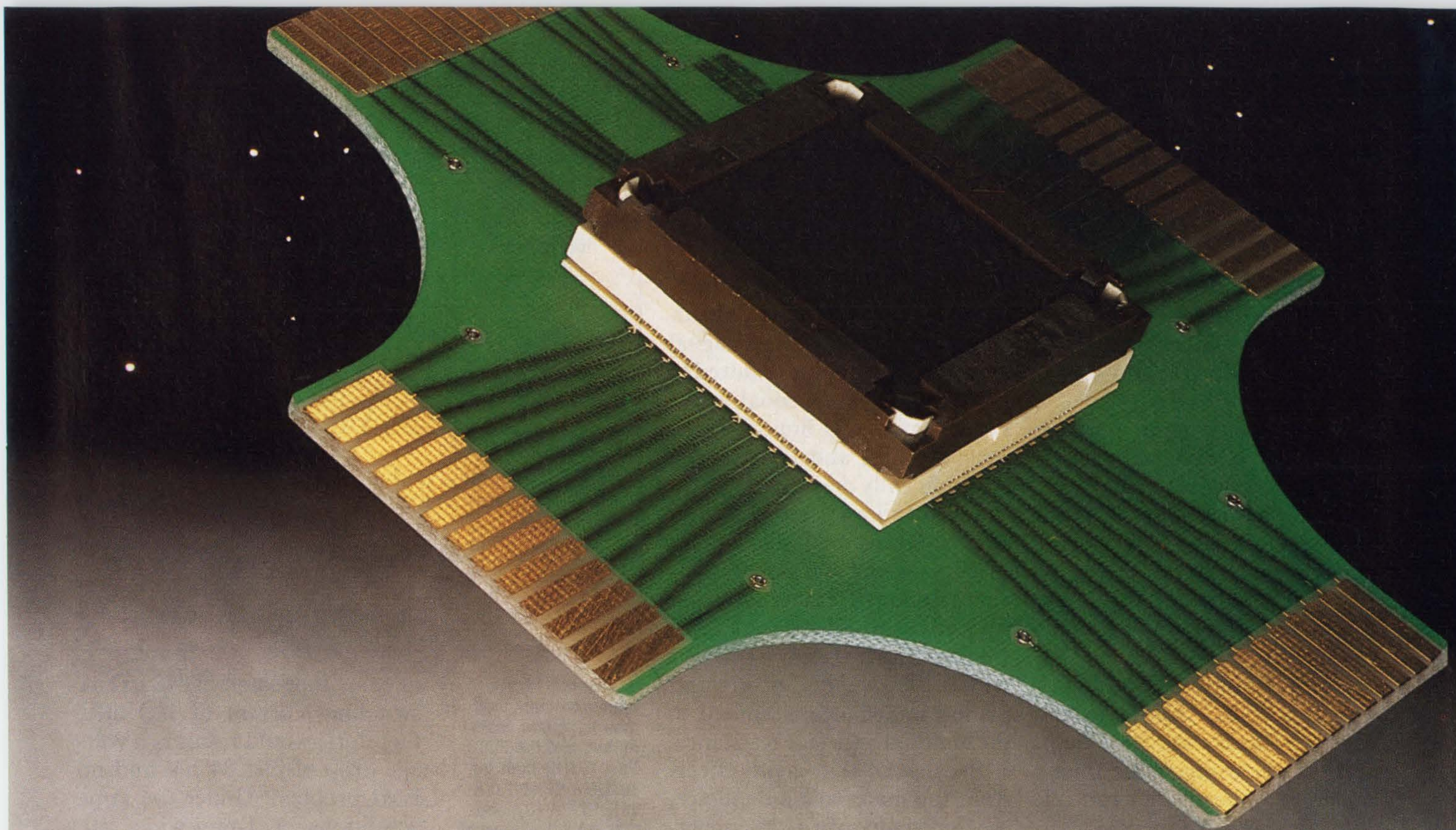




levels may vary by as much as 20 dB for equivalent clocks from different manufacturers. Investigating alternatives and matching clock capabilities to the application facilitates low-EMI designs.

CPUs with integral oscillators can help designers avoid overpowered clocks and save board space. Moreover, on-chip oscillators operate at lower power, and because they're segregated within the processor, they have significantly smaller radiating-loop areas.

Use of ferrite beads on high-frequency leads, such as external clock leads, can also help suppress electromagnetic interference. The beads can roll off offensive high-frequency harmonics without degrading data transmission. Typically rated at 5 to 10 μH, they produce higher impedances at RF than commonly used 22-to-47-Ω damping resistors. And unlike broadband damping resistors, they're frequency-selective.

A six-hole ferrite bead can accommodate a range of frequencies in 2-1/2-turn, 1-1/2-turn, and straight-through configurations. Clock frequencies from 500 kHz to 2 MHz call for the higher impedance afforded by 2-1/2-turn configurations with the bead located as close as possible to the output. Frequencies of 2 to 10 MHz require 1-1/2 turns. Above 10 MHz, the wires are run straight through the bead. Impedance increases with inductance—hence the number of windings—and should be limited at higher frequencies to prevent degradation of system performance.

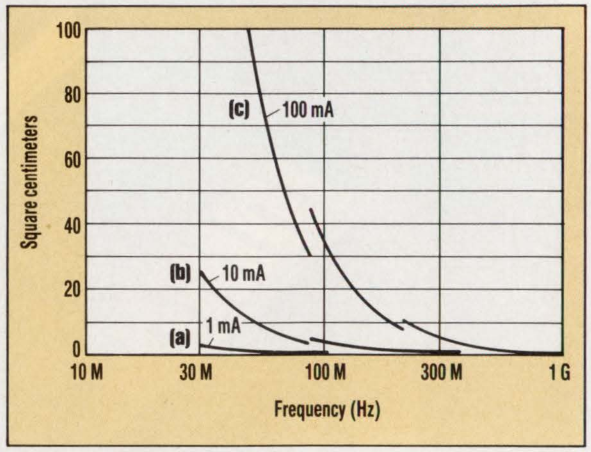
Ferrite beads tend to saturate under high current. This limitation can be remedied by using split configurations to lessen their permeability.

Using adjacent leads for clock signals and returns on pc boards can help reduce the area of clock-radiating loops, but requires larger boards. Because the interrelationship between the loop area and drive current results in a large RF signal, it's important that the designer minimize loop areas created by address, data, and other signal leads. The loop areas required to generate RF levels equal to the FCC Part 15J/B limit for currents of 1 mA and 100 mA can be graphically depicted *(Fig. 4)*.

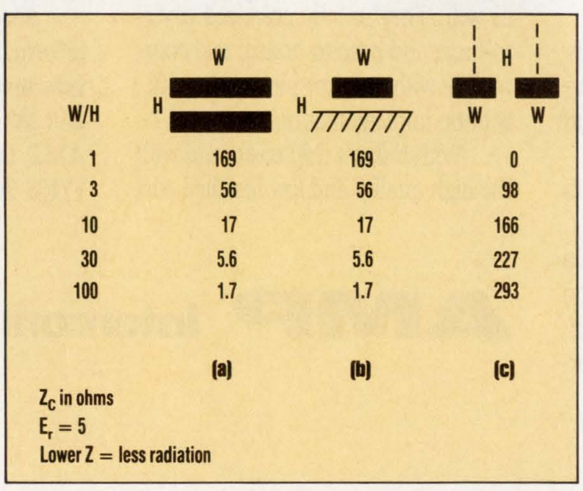
Another important factor in EMI-suppression design is power-supply and return impedance. As noted, traces have significant impedance at RF, which varies inversely with their width. However, a ground plane's impedance is limited to the material's surface resistance.

Because of skin-depth effects from the material's inductance, the impedance of a 1-oz. copper-foil ground plane at frequencies higher than 10 MHz increases proportionally with the square root of the frequency. Below 10 MHz, where it's largely resistive, changes in frequency have little effect on the overall impedance. In contrast, inductive reactance of a 1-mm-wide, 1-oz. foil trace, which increases in direct proportion to frequency, can yield impedances ranging from two to four orders of magnitude greater than those of a ground plane at higher frequencies.

Consider, for example, connecting two low-level devices with 1-mV sensitivities to a 1-oz. copper-foil power supply and return plane. Such a plane would have an impedance of 840 $\mu\Omega$. A switching current of 100 mA, therefore, would result in a voltage drop of just 84 μV and no EMI problem. Under the same conditions, a 1-mm-wide, 10-cm-long trace would have an impedance of 20 mΩ for a voltage drop of 6 mV, well above the sensitivity level of the devices.



4. This chart correlates maximum loop area in square centimeters and the FCC Part 15J(B) limit for radiated RF at 1 mA (a), 10 mA (b), and 100 mA (c) of current. The measurement distance is 3 meters.



W/H	(a)	(b)	(c)
1	169	169	0
3	56	56	98
10	17	17	166
30	5.6	5.6	227
100	1.7	1.7	293

Z_C in ohms
$E_r = 5$
Lower Z = less radiation

5. Power-rail impedance, which degrades logic performance, increases with frequency and separation distance. Three configurations are depicted: Two parallel planes in a multilayer board (a), a single trace over a ground plane in a multilayer board (b), and two parallel traces on a single-sided board (c).

The upshot is that using a ground plane on a single-sided board or sandwiching power and ground layers in a two-sided board can dramatically reduce emissions by supplying a low-impedance return. If it's impractical to incorporate a ground plane into the board, then positioning a metal plate or foil under it will serve the same purpose. That's because trace inductance varies with proximity to a ground plane as well as with its length and width. Mylar with foil on one side and adhesive on the other can simplify this procedure.

Another approach is to arrange grounds in a grid pattern. For example, the corner-to-corner impedance of a 10-by-10-in. board with a single edge-mounted ground trace equals 400 nH, or 250 Ω, at 100 MHz. Reconfiguring this 20-in. inductor into a matrix of 2-in. squares mathematically reduces impedance between opposite corners of the board by 10 times to a value of to 25 Ω. The grid can be constructed by laying out power and ground traces horizontally on one side of the board and verti-

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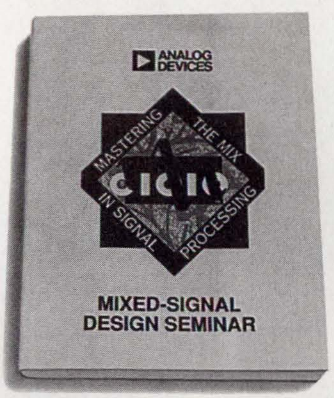

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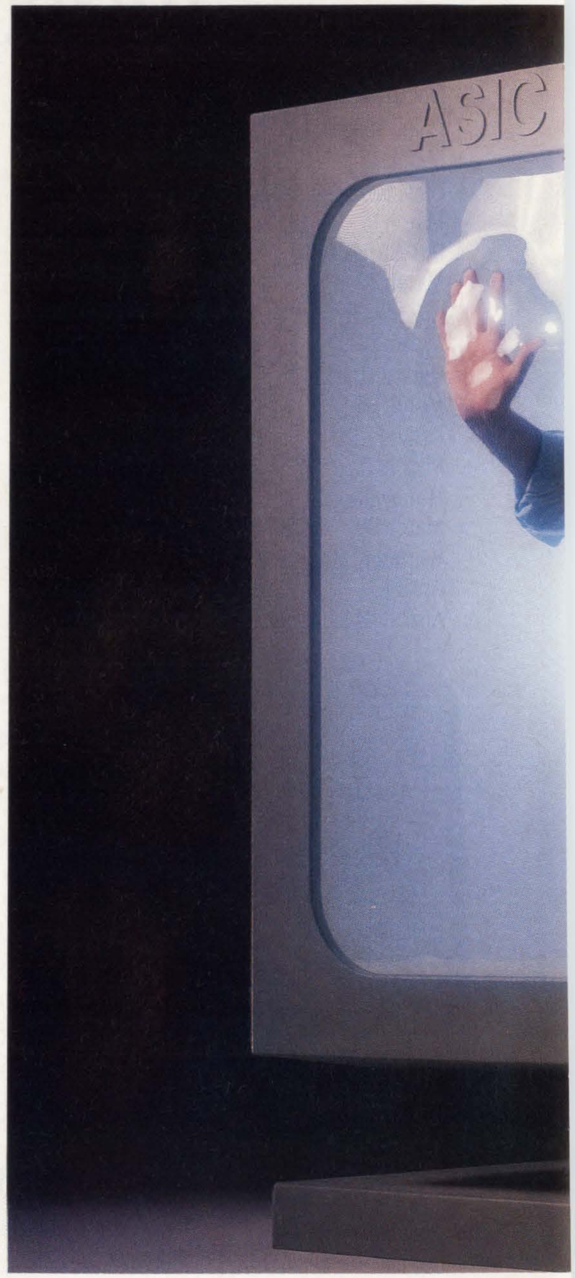

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cally on the other, and then tying the grid together with bypass capacitors.

As noted, power distribution on the board and data-transmission systems act synchronously to create separate but coherent radiating-loop areas. The power system's loop area is roughly equal to the separation of the rails multiplied by the distance from the nearest logic device to its decoupling capacitor. Data leads that use the power system for their return form dynamic-loop areas between sending and receiving devices.

Switching for transmission of logic signals creates transient-voltage drops throughout the power system, which impairs logic-device operation and creates interference. Installing decoupling or bypass capacitors near these devices reduces the size of radiating power loops and isolates the power dips from other logic devices. Decoupling capacitors act as storage elements from which associated logic devices draw instantaneous power as required.

The construction of capacitors gives them an inherent inductance, which is typically higher in electrolytic or Mylar designs than in ceramic ones. Trace inductance up to 20 nH combined with effective series resistance (ESR) can severely degrade their effectiveness.

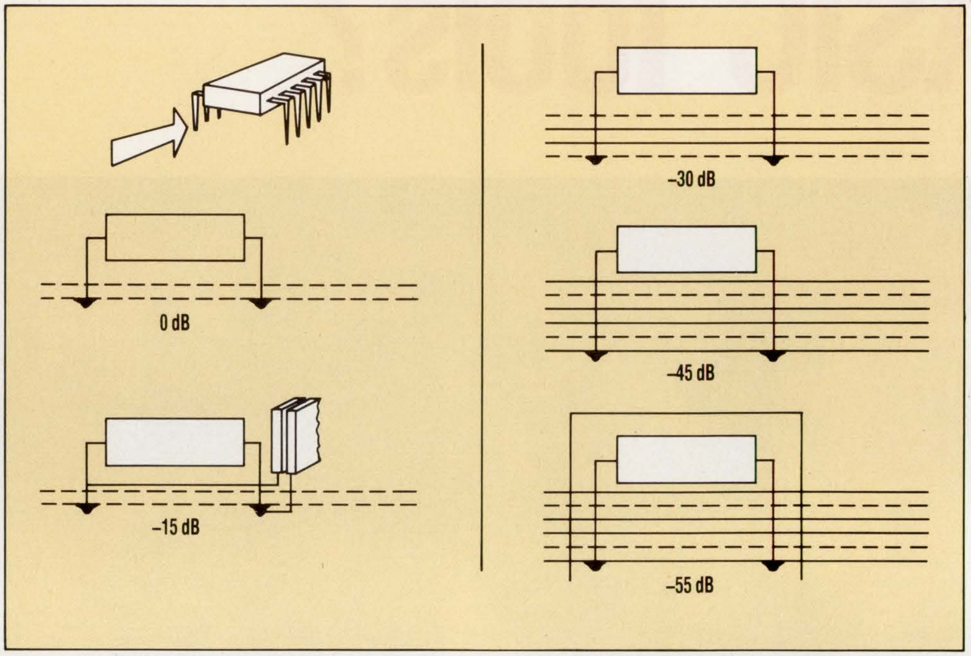
The following equation determines the bypass-capacitor values required to reduce effective impedance of the power-distribution system to control these voltage drops:

$$C = I/\,dV/dt$$

where:

- I is the current demand
- dV is the voltage drop
- dt is the switching time

Decoupling capacitors behave as capacitors at operating frequencies below their self-resonant frequencies and as inductors above these frequencies. This may mandate using several capacitors with different values to account for high and low self-resonant frequencies that result from lead inductance and capacitance.



6. Raised busing can reduce emissions of a single-layer board by up to 15 dB. Using a ground plane that acts as a separate, close-coupled parallel return can provide 30 dB of suppression. Shielding the data trace with another ground plane offers a 45-dB improvement compared with a typical two-layer board. Installing shielding canisters over board-mounted components yields a total reduction of 55 dB.

Because logic performance is degraded by power-rail impedance, which increases with frequency and separation distance, the rails should be as wide and as close together as possible. Three possible configurations include two parallel traces on a single-sided board *(Fig. 5a)*, one trace over a ground plane in a multilayer board *(Fig. 5b)*, and two parallel planes in a multilayer board, or the characteristic impedance of a raised-bus structure *(Fig. 5c)*.

These structures have much lower characteristic impedance and smaller loop areas than rail configurations, which can mean reduced board emissions by up to 15 dB *(Fig. 6)*. They also partially reduce the radiating area created by logic-signal transmission and return paths. Radiating-loop areas can be cut down significantly by designing the board with parallel data leads and separate returns rather than using the power system for return. But surface-area limitations make this approach impractical for single- or even double-trace-layer boards.

The most effective solution is a multilayer board with its inherent decoupling that's created by the power supply's capacitance and associated return layers *(Fig. 6, again)*. In a typical four-layer board design, the top and bottom layers are used for signal traces and the two middle layers for power distribution. For extremely high-speed applications, the configuration is changed to bury the signal leads between the ground planes, which precludes changes after the board is built.

With respect to the ground plane, the signal leads and returns take on the configuration of a microstrip or parallel-plate transmission line. This line's characteristic impedance is a function of the height-to-width ratio and the dielectric constant of the board material. It can be calculated as follows:

$$Z_o = (120\pi/\sqrt{E_r})\,(h/d)$$

where:

- h is the foil separation or board thickness
- d is the smaller dimension of the parallel plane
- E_r is the board's dielectric constant

Typically, Z_0 is less than 1 Ω for an h/d of less than 0.005 and E_r greater than 3. As a result, the potential drop at a logic chip with 20 mA of switching current is less than 20 mV. Because of the line's configuration, the low impedance does not couple RF energy to other chips supplied by the same plane, virtually eliminating electromagnetic interference.

Multilayer boards also have inherent capacitance, which may be calculated as follows:

$C = 0.0884E_r A/h$ pF

where:

- A is the board area (cm^2)
- h is the dielectric board thickness (cm)

For a typical h of 10 mils (0.0254 cm) and an er of 500, onboard capacitance is about 1740 pF/cm^2. A packing density of one chip per square inch will yield C greater than 10,000 pF/$in.^2$ (10,000 pF of decoupling per chip), which is more than enough to accommodate all logic-transition currents.

By inducing electromagnetic fields in the ground plane beneath them, high-frequency signal leads effectively create return paths for themselves. This phenomenon makes the current flowing in the ground plane behave as a separate, close-coupled parallel return. Provided the impedance is low, the ground plane can accommodate a virtually infinite number of data leads that will not interfere with one another even if they intersect. This approach can reduce emissions by up to 30 dB *(Fig. 6, again)*. Controlling the width of the data trace and the board's characteristics can help further lessen impedance and emissions.

Fringe radiation from the microstrip can be minimized by placing another ground plane over it to convert it into a strip line. This shields the data trace for a total reduction of about 45 dB compared with a typical two-layer board. Installing shielding canisters over board-mounted components yields a total reduction of 55 dB. *(Fig. 6, again)*.

Board designers should select the lowest possible operating frequency and current consistent with the system's performance needs.

For high-speed logic devices, meeting FCC requirements usually calls for measures beyond controlling radiating-loop areas. Emissions from components mounted on the board can be reduced by installing shielding enclosures for which the board's ground-plane layer serves as the bottom. These shields can be custom shaped and solder-mounted. By exhibiting measured attenuation of up to 62 dB at 1 GHz, they effectively control EMI emissions, susceptibility, and crosstalk at the board level.

In summary, cost-effective suppression of interference must be addressed in the pc board's initial design. As soon as hardware becomes available, diagnostic testing should be performed before the board goes into production. Hardening a board by good design typically adds 3% to 7% to its cost, depending on whether it's intended for commercial or military use. Hardening after development can cost five times as much.

The following is a checklist for low-EMI design:

1. Select the slowest, least powerful logic for the task. Avoid contention.
2. Consider clock alternatives and note variations in the noise levels among equivalent clocks from different manufacturers. Use integral oscillators instead of prepackaged units whenever possible.
3. Use ground planes or grids to reduce the impedance of return traces.
4. Segregate high-frequency devices and associated circuitry. Such devices and circuits should be positioned close to the backplane for signals leaving the board and away from the backplane for on-board signals. Leads should be filtered with split ferrite beads.
5. Minimize radiating-loop areas by using bypass capacitors on all sending and receiving devices and raised-bus power distribution on double-layer boards.
6. Design multilayer boards using the top and bottom layers for signal traces and the middle layers for power distribution.
7. Employ a ground plane over the top layer of the board to shield fringe radiation from data traces.
8. Install board-mountable shielding canisters over high-frequency devices.

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Ronald W. Brewer, director of EMC Technical Services at Instrument Specialties, holds a BSE from the University of Michigan and has over 25 years of experience in electromagnetic Tempest engineering and related disciplines.

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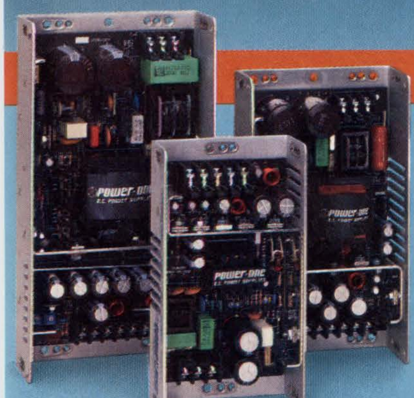

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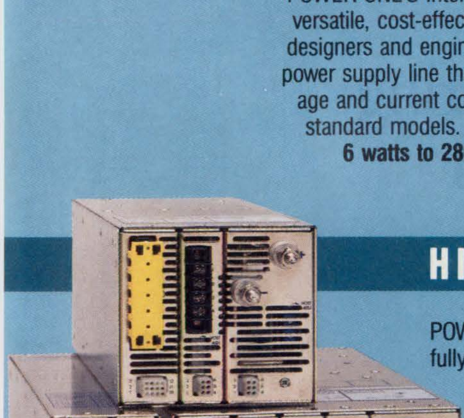

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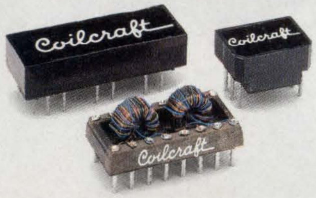

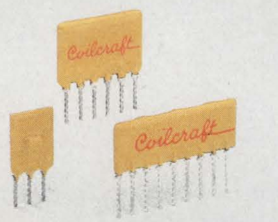

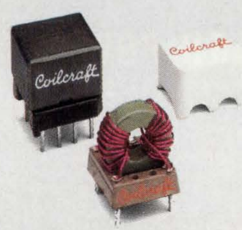

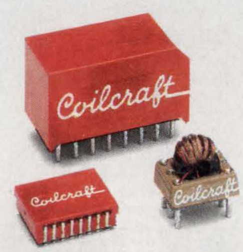

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CIRCLE 121

How To Recognize A Good Conductor Crimp

Attaining a solid terminal-to-wire bond involves many complexities.

BY RANDY J. KEMPF

Molex Inc., 2222 Wellington Ct., Lisle, IL 60532; (708) 969-4550.

How well a connector performs in an application depends on two main factors. The most important is choosing the right connector for the application. The second, and the subject of this article, is assuring the best possible crimp, or terminal-to-wire bond.

A good crimp has been defined in such terms as:

1. "The terminal didn't fall off."
2. "It had a specified crimp height."
3. "It met a specified pull test."
4. "All of the wire strands were deformed without fracturing."
5. "We smashed it down good."

Actually, only two are legitimate definitions of a good crimp termination. The correct ones will be discovered later, but if definitions #1 or #5 were included in your answer, do not skip to the end of this article. However, before the characteristics of a good crimp are defined, the components of a typical terminal must be more clearly understood.

A terminal can be divided into three main sections: the mating section, the conductor-crimp section, and the insulation-crimp section *(Fig. 1)*. The terminal's mating section makes the electrical junction with its male or female counterpart. It's this portion that determines the terminal's performance characteristics in terms of current-carrying capability, mating or engagement force, number of mating cycles, and the contact resistance of the interconnection.

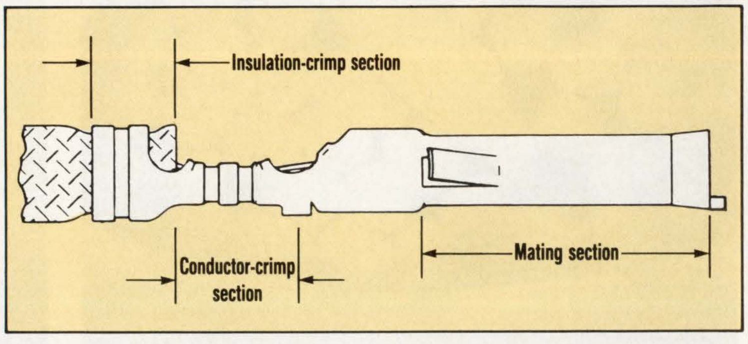
The terminal's current-carrying capability is the total current it can continuously carry to create a maximum temperature rise of 30°C above ambient. A terminal can usually carry somewhat more than that value without catastrophic failure. However, the 30°C value does offer a built-in safety factor that allows for a wide range of environmental and application conditions. Generally, the larger the terminal, the more current it can carry. That relationship, though, isn't necessarily direct. For example, a 0.062-in.-diameter terminal carries up to 5 A/circuit, a 0.093-in.-diameter terminal carries up to 12 A/circuit, and a 0.125-in.-diameter terminal carries up to 20 A/circuit.

Although the current rating is the most important criterion to use in selecting a connector, especially for a power application, other features of the terminal are also very important. These include the number of mating cycles, contact resistance, and engagement force.

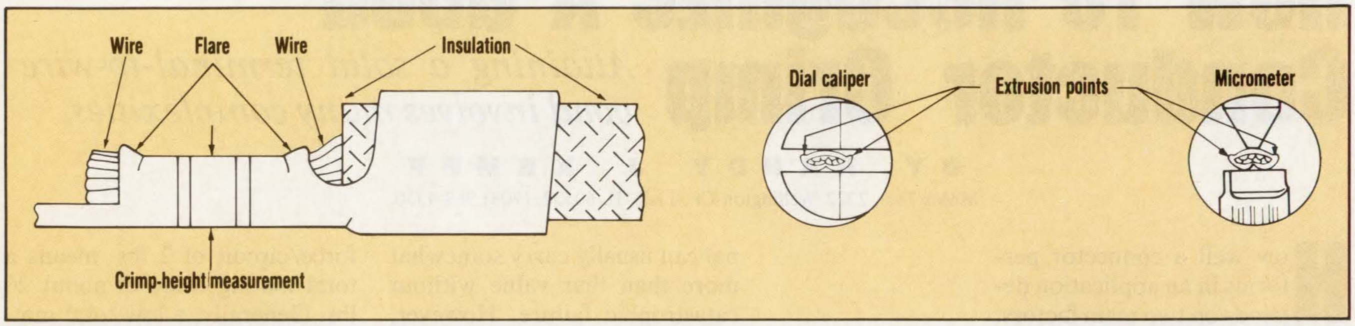
The engagement force is the effort required to mate or engage the male and female terminals. It's expressed in pounds/circuit, and can have values of 0.5 to 6 lbs. or more per circuit. The connector's total mating force can be easily determined by multiplying the terminal's mating force/circuit by the number of circuits or mated terminals in the housing. For example, a 10-circuit connector with a mating force/circuit of 2 lbs. means a total mating force of about 20 lbs. Generally, a low total mating force is desirable, especially when mating to a pc board where high mating forces could damage the board. This also holds true with high-circuit-count connectors, where a high force could make mating the connector difficult.

Another important feature of a terminal is the number of mating cycles, which is how many times the connection can be made and broken. That number is a complex combination of the terminal's configuration or geometry, its base metal (brass, phosphor bronze, or other high-performance alloy), and the plating on that base metal (tin, gold, or nickel). The terminal's geometry is designed to give the best combination of size and performance for the job.

As previously mentioned, the number of mating cycles a terminal can withstand depends in part on the terminal's base material. Brass is more than adequate for most applications. It offers an excellent combination of electrical conductivity and strength and can be formed into intricate shapes. In applications where many mating cycles are required (100 or more), a higher-performance base material,



1. The terminal's anatomy can be broken down into three main sections: the mating section, the conductor-crimp section, and the insulation-crimp section.



2. The conductor's crimp height can be measured with either a dial caliper or a blade-type micrometer. Care must be taken not to measure the extrusion points, which would be a misleading measurement.

such as phosphor bronze or beryllium copper, should be specified to maintain an acceptable normal force or terminal-to-terminal pressure.

The terminal's plating minimizes corrosion or tarnishing of the base material and the subsequent negative impact on contact resistance. Tin and tin-lead are the most frequently used cost-effective platings. In high-cycle (25 or more) or low-current (less than 0.5 A/circuit) applications, gold plating should be specified.

Contact resistance can be a very important design consideration in applications where a large voltage drop across the mated terminals would degrade system performance. If a large number of mating cycles reduces the normal force, or if the plating should wear away and permit corrosion to form, the contact resistance will increase. Because a mated terminal can be seen as a resistor with a typical value of 10 to 50 mΩ, a dramatic increase in resistance value could cause a loss of signal or an overheated terminal.

If the right connector system is matched with your application, and if the engineer who designed the terminal did a good job, the front third will work well. But let's look at the two-thirds of the terminal that's out of the design engineer's control.

The terminal is designed to operate within a certain range of wire-conductor and insulation diameters, usually expressed in AWG (American wire gauge). For each wire gauge within this range, the engineer specifies the dimension of the terminal-to-wire interface, or crimp height, that delivers the highest performance. It is defined as the highest pull force or strongest wire-to-terminal bond.

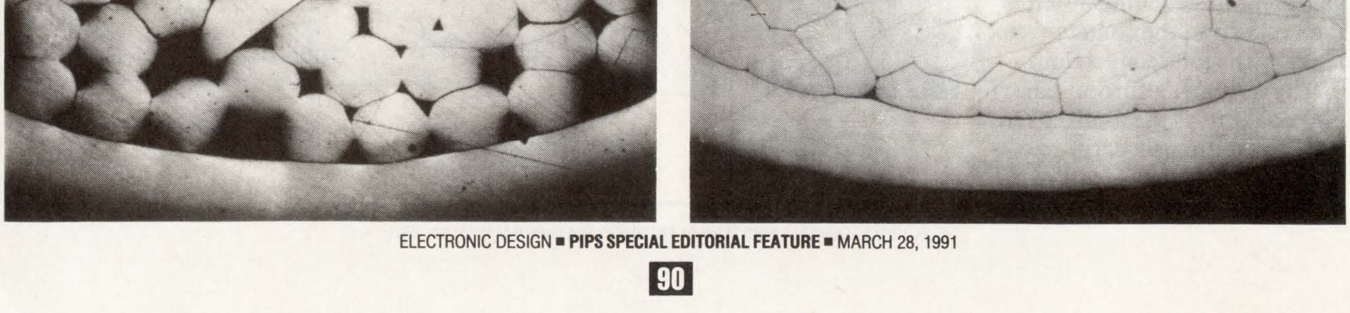
The pull force is the force, measured in pounds, that the wire-to-terminal interface will withstand when a straight axial load is applied to the terminated wire. This is, however, a destructive test and is therefore inappropriate as a 100% inspection method to assess termination quality. A better method is to measure crimp height. It's a non-destructive test that ensures the maximum bond.

The crimp height is measured, using a micrometer, at the conductor-crimp sections *(Fig. 2)*. If this dimension is too small, then the terminal is over-crimped and wire strands could be damaged, which results in a lower pull force. If the dimension is too large, then the terminal is under-crimped and the wire strands will not be deformed enough to assure that the crimp will pass the pull-force test *(Figs. 3a and 3b)*.

If the crimp height isn't within specification, the application tooling's crimp height should be adjusted. If the punch and anvil are so worn down that they can't make a good crimp, they should be replaced.

If a hand tool is used, its crimp heights can be adjusted by turn-

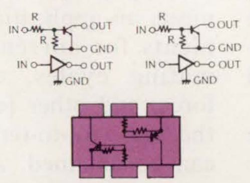
3. In the micro-section shown, the black areas (voids) indicate an under-crimp. If the crimp height is too large, then the wire strands will not be deformed enough to assure passage of a pull-force test (a). When the crimp height is correct, all wire strands are deformed and there are few, if any, voids present between them (b).



SMallTalk.

Let's talk savings.

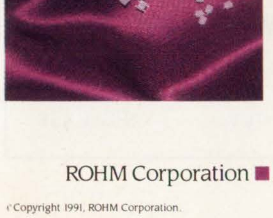
Surface mount transistors–or even T092s used with resistors in network pairing–can be replaced with a single digital transistor from ROHM. One small SOT-25 or -36 package can contain up to two transistors and four resistors. One component provides several functions, and that means lower placement cost, higher reliability, lower component count, less real estate, and reduced inventory. Standard V_{CE} ratings of 11V to 120V, and current ranges from 30mA to 100mA, are available.



Dual digital transistor circuit diagram. Dozens of layouts available.

Let's talk added value.

If you want maximum benefit from SMT, don't change to through-hole when it comes to LEDs. You can keep everything SMT by incorporating ROHM's surface mount LEDs as indicators on your board.



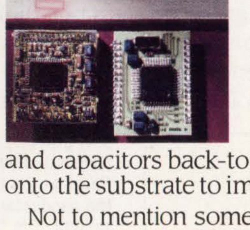
Our lineup includes single-chip LEDs in red, orange, yellow and green; and dual-chip types that give you combinations of colors. You can even get a three-color effect with red and green chips combined to make amber.

We offer standard brightness and high luminance, lensed LEDs packaged in SOT-23s, and lensed mini-molded styles. Brightness ranges from 555 to 700 angstrom units.

They can turn product designs into gems.

Let's talk component density.

You need density? How about 50 components per square centimeter?



That's what we've achieved in our newest hybrid circuits, thanks to TAB packaging, fine pitch lead spacing, and screening resistors and capacitors back-to-back–directly onto the substrate to improve shielding.

Not to mention some unbelievably small passive components.

Take our new MCR 01, the smallest resistor package in the world. A mere 1.0 x 0.5 mm, it's about the size of a grain of pepper. It occupies 60% less space and weighs 75% less than our MCR 03–formerly the world's smallest.

Resistance range is 5.6Ω to 1.5MΩ, and rated voltage is 0.032W with a 25W maximum.

We're now also offering a strong line of ceramic chip capacitors with package sizes as small as 0603 (1.6mm x 0.8mm). They're offered in NPO, X7R, Z5U, and Y5V dielectrics.

So when you're talking popcorn or jellybeans,

Remember that ROHM introduced SMT to this country, and was the first manufacturer to offer surface mount products in quantity.

And we continue to offer innovations like multiple-function transistors, unique diode packages, surface mountable networks, and industry-leading component densities.

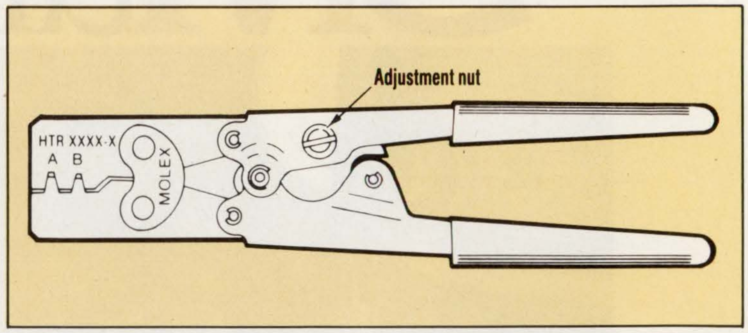
Call us and start a little SMallTalk of your own. We'll be happy to share some information.

ROHM

ROHM Corporation ■ ROHM Electronics Division ■ 8 Whatney ■ Irvine, CA 92718 ■ Telephone (714) 855-2131 ■ FAX (714) 855-1669

CIRCLE 177

ing the adjustment screw *(Fig. 4)*. On a hand tool, the conductor- and insulation-crimp heights are adjusted simultaneously. The crimp heights of terminations done with a hand tool should be checked often because a hand tool wears much faster than a bench press.



4. Crimp heights for hand tools can be adjusted by rotating the adjustment screw. Many poor crimps result from misadjustment of the crimp height.

A properly crimped terminal should have a slight flare at the rear of the conductor-crimp section *(Fig. 5)*. This flare prevents individual wire strands from being cut or damaged during the crimping process and provides a smooth transition between the conductor- and insulation-crimp sections. The application tooling has this flare built into the punch and anvil. However, as the tooling wears, this flare may shrink. When the flare reaches two times the terminal's material thickness, the punch and anvil should be replaced.

Another important indication of a properly crimped terminal is its straightness. For most terminals, the center lines of the mating end and the crimp sections should be the same or within 5° of each other. Otherwise, a bent terminal, often called a banana crimp, may be misaligned when inserted into a housing. The resultant condition, which is known as "butting," can prevent the connectors from mating. If the bent terminal is far enough off-center, the terminals could be damaged when mating or even cause the terminal to be pushed out the back of the housing. This is known as terminal backout.

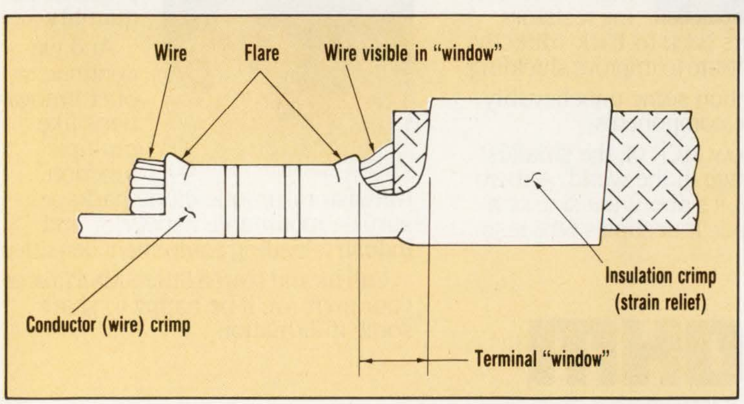
The banana shape can be either forward when it's bent in the same direction as the formed portion of the crimp section, or reverse when it's bent in the direction of the smooth side of the crimp section. If the bend is forward, the conductor-crimp height should be verified to see if it's correct and the insulation crimp should be reasonably symmetrical. If the crimps are acceptable, then the nose-hold-down device on the application tooling should be adjusted or replaced. This device may be a spring-loaded plunger or a plastic tube that comes in contact with the terminal's nose or mating end as it's being crimped and maintains its linearity.

A terminal bent in the reverse direction indicates a worn or damaged punch and/or anvil. As the crimp press completes its cycle and the punch or anvil moves away from the terminal, the worn or damaged tooling causes the terminal to become momentarily lodged, thus bending it. Replacing the punch and anvil will correct the reverse-bend problem.

The quality of the termination is directly related to the quality of the application tooling. Only the specific application tooling that's developed or recommended by the terminal's manufacturer for the wire gauge being used should be employed. The application tooling must also be kept in good working order. The tooling's perishable components, the punch and anvil, must be replaced as required to maintain a high-quality termination.

Now the correct definitions for a good crimp can easily be chosen. After selecting the terminal or connector system that meets an application's requirements for current handling, mating cycles, engagement force, and other features, then the best wire-to-terminal crimp can be obtained. Also, during setup and periodically within each production run, the conductor-crimp heights should be verified to meet the manufacturer's specifications (definition #2), so that the terminations will meet a specified pull force (definition #3) and have wire strands that are deformed without fracturing (definition #4).

Randy Kempf, director of product management at Molex, holds a BSEE from Purdue University, West Lafayette, Ind., and an MBA from the University of Iowa, Iowa City.

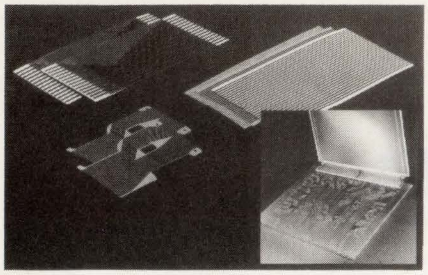


5. A properly crimped terminal should have flares at the end of the conductor-crimp section. The flares prevent individual wire strands from being cut or damaged during crimping.

CONNECTORS

▼ HEAT-SEAL CONNECTORS LINK LCDs TO BOARDS

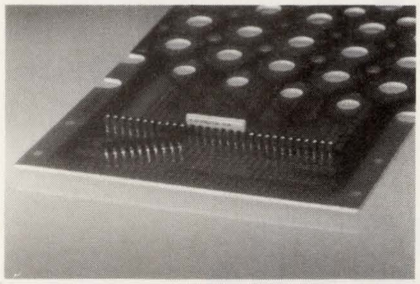
A low-cost line of high-density, flexible heat-seal connectors is available for pcb-to-LCD, pcb-to-pcb, and other similar applications. The J-Type series of solderless connectors consist of precision-screened traces of either carbon (JC type) or a carbon-silver blend (JS type) applied to a polyester substrate. A conductive



adhesive is applied over the bonding surface. Call for pricing.

Shin-Etsu Polymer America
34135 7th St.
Union City, CA 94587
(415) 475-9000
▶ CIRCLE 462

▼ PRESS-FIT RECEPTACLE SAVES THROUGH HOLES



A solderless press-fit receptacle eliminates damage to plated through holes in backplanes. The #8292-4 machined receptacle has a truly compliant tail that eliminates the risk of backplane damage when they're inserted. The tail is hollow and slotted, which permits it to close down and conform to the size of the hole. Pricing is $0.12 in lots of 10,000. Delivery is from stock.

Mill-Max Mfg. Corp.
P.O. Box 300
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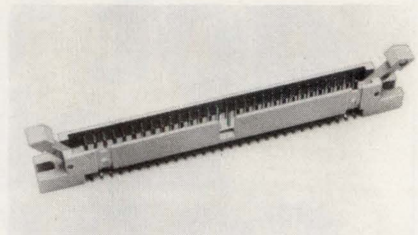
(506) 922-6000
▶ CIRCLE 463

▼ SURFACE-MOUNT HEADER FREES BOARD SPACE

Increased connector reliability and board real-estate savings are among the benefits of the 4600 Series surface-mounted shrouded headers. The devices have compliant gull-wing leads for a reliable surface-mount connection, which saves on re-



work. The leads are within the body shadow so the connector takes less space. Pricing is $5.90 in lots of 1000. Delivery is in six weeks from receipt of order.

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Austin, TX 78769-2963
(800) 225-5373
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Advanced Interconnections
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Bendix Connector Ops.
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(continued on p. 96)
(see p. 103 for key)

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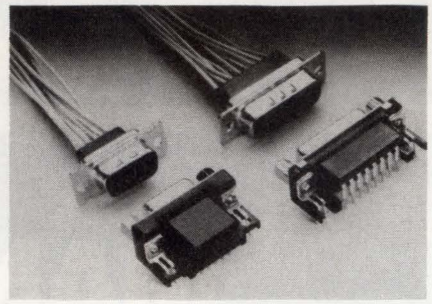
CIRCLE 355

(continued on p. 97)
(see p. 103 for key)

▼ D-SUBMINI CONNECTORS UP DENSITY, DROP COST

A line of high-density D-subminiature connectors is priced up to 40% lower than competitive offerings, claims its maker. The connectors' contacts are plated with 30 μin of gold for improved mating performance. Female contacts are protected with a closed funnel-entry design for reliable connections. Prices start



at $1.41 for a size-15 board-mounted receptacle in lots of 10,000. Delivery is from stock to six to eight weeks.

ITT Cannon
1851 E. Deere Ave.
Santa Ana, CA 92705
(714) 261-5300
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▼ DUAL-ROW SMT CONNECTORS MOUNT ON 0.100-IN. GRID

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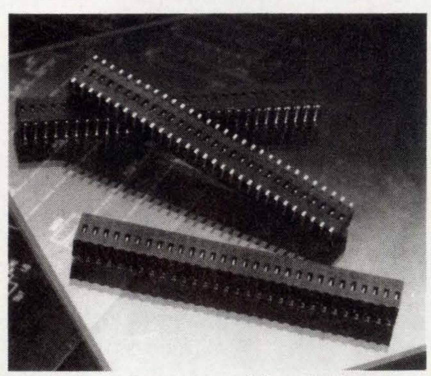

phosphor bronze with plating options of tin-lead or selective gold. Call for pricing and delivery.

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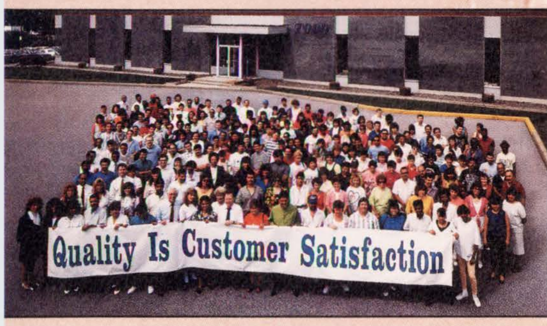

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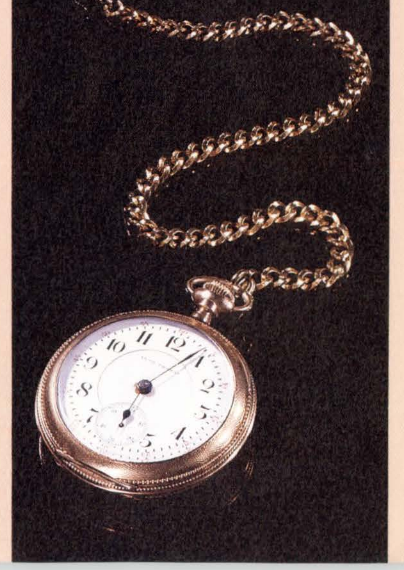

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- Cost/watt savings up to 30%

From standard voice and data networks to super micros and workstations, TODD's MAX series of switchers are increasingly become the #1 power choice of OEM system designers. Here's why:

Housed in a compact (2.5"x5"x9") package, the MAX 350's provide the outputs you need for ISDN, LAN and T1 applications – with yields of over three watts/in³ across four fully regulated outputs. Select a MAX 350 with auxiliary outputs and power common peripherals, ECL systems, RS232 outputs, and communications drivers.

The MAX 500 "bus driver" series pack 500 watts into a 2.5"x5"x11.5" package with power densities of almost 3.5 watts/inch. With VMEbus and Multibus II compatibility, up to 16 amps of peak current, and the ability to power up to 80 amps of logic and four hard disk drives, these switchers will meet all your peripheral start up needs.

Specify the MAX 700/750 series and you'll get an unprecedented design freedom for your high-end computer products. Replace a 5"x8"x11" shoe box switcher with a 2.5"x5"x13.6" MAX 700 or 750 switcher, and you'll get a space savings of 58%. Or build in redundancy with two MAX 700's in place of one shoe box. And while you'd expect to pay more for this kind of design flexibility, you'll actually realize cost savings of up to 30% per watt.

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MAX SERIES HIGHLIGHTS

Model	Output #1	Output #2	Output #3	Output #4
350 WATTS: 2.5"x5"x9"*				
MAX-353-0512	+5V @ 50A	+12V @ 8/12Apk	-12V @ 4.0A	—
MAX-354-1205	+5V @ 50A	+12V @ 8/12Apk	-12V @ 4.0A	-5.2 @ 2.0A
MAX-354-1212	+5V @ 50A	+12V @ 8/12Apk	-12V @ 4.0A	12V @ 2.0A
MAX-354-1224	+5V @ 50A	+12V @ 8/12Apk	-12V @ 4.0A	+24V @ 1.5A
400,500 WATTS: 2.5"x5"x11.5"*				
MSC-402-0512	+5V @ 20A	+12V @ 25/36Apk	—	—
MAX-503-0512	+5V @ 80A	+12V @ 10/16Apk	-12V @ 10.0A	—
MAX-504-1252	+5V @ 80A	+12V @ 10/16Apk	-5.2V @ 10.0A	12V @ 2.0A
MAX-504-1205	+5V @ 80A	+12V @ 10/16Apk	-12V @ 10.0A	5.2V @ 2.0A
MAX-504-1212	+5V @ 80A	+12V @ 10/16Apk	-12V @ 10.0A	12V @ 2.0A
MAX-504-1224	+5V @ 80A	+12V @ 10/16Apk	-12V @ 10.0A	+24V @ 2.0A
MAX-504-1552	+5V @ 80A	+15V @ 10/16Apk	-5V @ 10.0A	15V @ 2.0A
700,750 WATTS: 2.5"x5"x13.6"*				
MAX-704-1205	+5V @ 100A	+12V @ 12/20Apk	-12V @ 10.0A	5.2V @ 2.0A
MAX-704-1212	+5V @ 100A	+12V @ 12/20Apk	-12V @ 10.0A	12V @ 2.0A
MAX-753-0512	+5V @ 120A	+12V @ 12/20Apk	-12V @ 10.0A	—
MSC-753-0512	+5V @ 120A	+12V @ 20/27Apk	-12V @ 6.0A	—
MAX-754-1252	+5V @ 120A	+12V @ 12/20Apk	-5.2V @ 10.0A	12V @ 2.0A
MAX-754-1205	+5V @ 120A	+12V @ 12/20Apk	-12V @ 10.0A	5.2V @ 2.0A
MAX-754-1212	+5V @ 120A	+12V @ 12/20Apk	-12V @ 10.0A	12V @ 2.0A
MAX-754-1224	+5V @ 120A	+12V @ 12/20Apk	-12V @ 10.0A	+24V @ 2.0A

*Size for system air-cooled versions.

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Elma Electronic Inc.
41440 Christy St.
Fremont, CA 94538
(415) 656-3400
(DI) (DD) (ML) (WR) (BP) (VB) (MB) (IB) (BU) (GB) (PW) (GP) (IN) (VR) (PT) (EM) (CM) (ER) (GK)
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Emcor Products/Crenlo, Inc.
1600 N.W. Fourth Ave.
Rochester, MN 55901
(507) 289-3371
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Equipto Electronics Corp.
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Aurora, IL 60506-9988
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Fischer Connectors Inc.
28245 Crocker, Suite 210
Valencia, CA 91355
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Fujitsu Component of America Component Div.
3545 N. First St.
San Jose, CA 95054
(408) 922-9000
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GEM Inc.
109 State Place
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(619) 747-9177
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Garry Electronics
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Langhorne, PA 19047
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CIRCLE 362

General Devices Co. Inc.
1410 S. Post Rd.
Indianapolis, IN 46239
(317) 897-7000
(GP) (VR) (EM) (MI) (CM)
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Graphic Research Inc.
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Chatsworth, CA 91311
(818) 886-7340
(PC)
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Handy & Harman Tube Co.
Whitehall Rd. & Township Line
Norristown, PA 19403
(215) 539-3900
(TB)
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Harwin U.S.A.
4173 Main St., Suite 191
Bridgeport, CT 06606
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Hirose Electric USA Inc.
2685-C Park Center Dr.
Simi Valley, CA 93065
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Hoffman Engineering Co.
900 Ehlen Dr.
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Honda Connectors
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Vernon Hills, IL 60061
(708) 913-9566
(ID) (SM)
CIRCLE 369

Hughes Aircraft Co. Connecting Devices Div.
17150 Von Karman Ave.
Irvine, CA 92714
(714) 660-5769
CIRCLE 370

Hybricon Corp.
12 Willow Rd.
Ayer, MA 01432
(508) 772-5422
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Hypertronics Corp.
16 Brent Dr.
Hudson, MA 01749
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ITT Cannon Components Div.
1851 Deere Ave.
Santa Ana, CA 92705
(714) 261-5300
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CIRCLE 373

Instrument Specialties Co. Inc.
P.O. Box A, I-80 Exit
Delaware Water Gap, PA 18327
(717) 424-8510
(ES) (MG) (ER) (GK) (SE)
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Interconnect Devices Inc.
5101 Richland Ave.
Kansas City, KS 66106
(913) 342-5544
(CX) (ZI) (CD) (BI)
CIRCLE 375

Interlogic Industries
85 Marcus Dr.
Melville, NY 11747
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CIRCLE 376

JAE Electronics Inc.
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Irvine, CA 92718
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JST Corp.
1200 Business Ctr. Dr., Suite 400
Mt. Prospect, IL 60056
(708) 803-3300
(DS) (DI) (FC) (CE) (ID) (ZI) (SM)
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Keystone Electronics Corp.
31-07 20th Rd.
Astoria, NY 11105-2017
(718) 956-8900
(DS) (IN)
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Kycon Cable & Connector Inc.
1772 Little Orchard St.
San Jose, CA 95125
(800) 544-6941
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LEMO USA Inc.
335 Tesconi Cir.
Santa Rosa, CA 95401
(800) 444-LEMO
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Lumberg Inc.
420 Southlake Blvd.
Richmond, VA 23236
(804) 379-2010
(DI) (FC) (CE) (ID) (SM)
CIRCLE 382

MWS Wire Industries
31200 Cedar Valley Dr.
Westlake Village, CA 91362
(818) 991-8553
(CO) (FL) (TW) (SH) (WV) (PW) (MN) (HK)
CIRCLE 383

Manhattan Electric Cable Corp.
Station Plaza
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(914) 967-8000
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Mark Eyelet Inc. AMP Inc.
63 Wakelee Rd.
Wolcott, CT 06716
(203) 756-8847
(ZI) (SM) (DP) (PG) (CD) (MD)
CIRCLE 385

(continued on p. 98)

(see p. 103 for key)

▼ SIX-ROW CONNECTORS TEAM FOR 810 CONTACTS

The TBC Plus connectors, which come in 90- and 120-position versions, can be combined for high-pin-count interconnections of 810 positions or more. The connectors are on 0.100-by-0.100-in. contact centerline spacing. Pricing is about $0.12 per mated line. Delivery is in eight weeks from receipt of order.

AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
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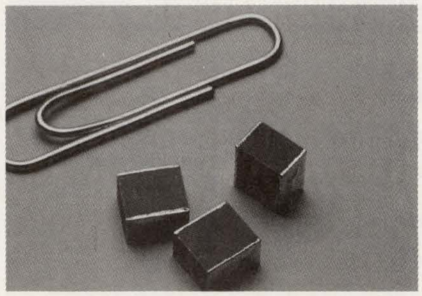
▼ CYLINDRICAL CONNECTOR OUTLASTS CORROSION

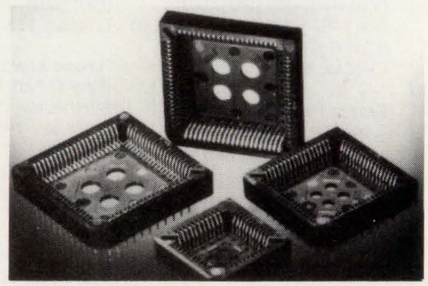
After successfully completing five years (44,000 hours) of testing, the DG123 composite cylindrical connector has proved impervious to salt-spray corrosion. The connector offers substantial weight reductions compared with comparable aluminum connectors. Call for pricing.



Deutsch Engineered Connecting Devices
Municipal Airport
Banning, CA 92220
(714) 849-7844
▶ CIRCLE 470

▼ SOCKETS FOR PLCCs TAKE JEDEC CARRIERS

A line of through-hole square sockets houses PLCC packages with 44, 68, and 84 leads. The sockets accept JEDEC Type A plastic leaded chip carriers with tin-plated leads on 0.050-in. centers. A high hold-down force prevents the chips from popping out. Raised inner platforms on the housing support the PLCC and prevent lead deformation. Call for pricing and delivery.



Molex Inc.
2222 Wellington Ct.
Lisle, IL 60532
(708) 969-4550
▶ CIRCLE 471

CONNECTOR AND PACKAGING MANUFACTURERS

Markel Corp.
P.O. Box 752, School Ln.
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Master Circuits Inc.
424 Apperson Way North
Kokomo, IN 46901
(317) 457-6605
(SS) (DD) (ML) (FX) (PC)
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Meritec div. of Associated Enterprises
1359 Jackson St.,
P.O. Box 8003
Painesville, OH 44077
(216) 354-3148
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Methode Electronics Inc.
7444 W. Wilson Ave.
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(708) 867-9600
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(818) 886-7340
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Micro Plastics Inc. Connector Div.
9180 Gazette Ave.
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(818) 882-0244
(CE)
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Mill-Max Mfg. Corp.
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(ZI) (SM) (CC) (DP) (PG) (CD)
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(708) 879-6262
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Morfor Products International
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Lowell, MA 01853-0657
(508) 453-5763
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10 Mupac Dr.
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(508) 588-6110
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NAS Electronics
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CIRCLE 399

Nemal Electronics Inc.
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N. Miami, FL 33161
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Newman, M.M. Corp. Heli-Tube Div.
P.O. Box 615, 24 Tioga Way
Marblehead, MA 01945
(617) 631-7100
(HN) (CA)
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Noble U.S.A.
5450 Meadowbrook Ind'l. Ct.
Rolling Meadows, IL 60008
(708) 364-6038
(FX)
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ODU U.S.A.
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Camarillo, CA 93012
(805) 484-0981
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CIRCLE 403

Omega Shielding Products Inc.
1394 Pompton Ave.
Cedar Grove, NJ 07009
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Optima Enclosures
2166 Mtn. Indl. Blvd.
Tucker, GA 30084-5088
(404) 496-4000
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CIRCLE 405

PCD Inc.
2 Technology Dr.
Peabody, MA 01960
(508) 532-8800
(CE) (ZI) (CD) (MD)
CIRCLE 406

PacTec Div. of LaFrance Corp.
Enterprise & Executive Aves.
Philadelphia, PA 19153
(215) 365-8400
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Panduit Corp.
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Tinley Park, IL 60477-0981
(800) 777-3300
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Penstock Inc.
520 Mercury Dr.
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(408) 730-0300
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Poly-Flex Circuits
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Cranston, RI 02920
(401) 463-3180
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Power Dynamics Inc.
59 Lakeside Ave.
West Orange, NJ 07052
(201) 736-5722
(ID) (CD) (PW)
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Powerbox Inc.
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Boulder, CO 80302
(303) 444-1461
(IN)
CIRCLE 412

Praegitzer Industries Inc.
1270 Monmouth Cut-off
Dallas, OR 97338-9532
(503) 623-9273
(SS) (DD) (ML) (PC)
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Precision Interconnect
16640 S.W. 72nd Ave.
Portland, OR 97224
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(continued on p. 101)
(see p. 103 for key)

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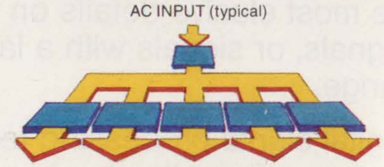

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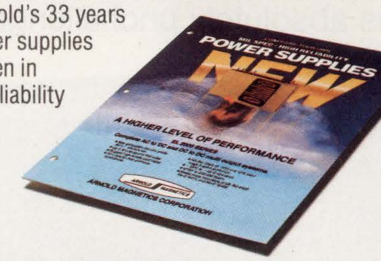

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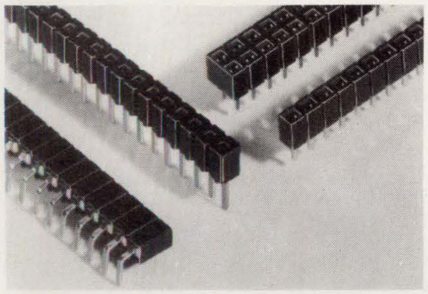
CIRCLE 119

▼ SOCKET STRIPS SPORT VERY LOW PROFILES

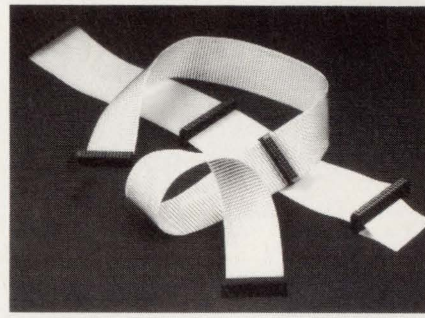
Two low-profile socket strips for 0.025-in. headers feature a very low profile of just 0.180 in. The SLW Series sockets offer a highly reliable tuning-fork-style contact and a choice of single- or double-row strips. They accept pins from 0.022 to 0.028 in. square. The CES Series features a folded dual-beam contact and a profile of 0.2 in. Both series start at $0.02 per pin. Delivery is from stock.

Samtec Inc.
P.O. Box 1147
New Albany, IN 47151
(800) SAMTEC9
▶ **CIRCLE 472**



▼ MULTISIGNAL CONNECTORS CAN BE DAISY-CHAINED

Meritec's Multi Signal Interconnects can be terminated in daisy-chain configurations to FEP, PTFE, or Filatex textile cables. The MSI connectors are offered in 10, 20, 26, 34, 40, 50, and 60 positions. They mate with 0.025-in. square or round pins on a 0.100-in. grid. In lots of 1000, a 40-position, 12-in. double-ended Filatex cable assembly with one daisy-chain connector would cost $33.58. Delivery is in four weeks.



Meritec
P.O. Box 8003
Painesville, OH 44077
(216) 354-3148
▶ **CIRCLE 473**

CONNECTOR AND PACKAGING MANUFACTURERS

Preh Electronic Inds. Inc.
470 E. Main St. (Rt. 22)
Lake Zurich, IL 60047-2578
(708) 438-4000
(DS) (DI)
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Pyle-National Inc.
1334 N. Kostner Ave.
Chicago, IL 60651
(312) 342-6300
(RF) (CX) (CD) (MD)
CIRCLE 416

Radstone Technology Corp.
20 Craig Rd.
Montvale, NJ 07645
(201) 393-2700
(VB) (MB) (BM) (EM) (MI)
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Revere Aerospace Inc.
845 North Colony Rd.
Wallingford, CT 06492
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(CD) (MD) (SH) (WV) (HN) (CA) (ER)
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Ribbon Cable Co.
8753 Lion St.
Rancho Cucamonga, CA 91730
(714) 987-0007
(FL) (TW) (SH) (WV) (HN) (ER)
CIRCLE 419

Richard Hirschmann of America
Industrial Row, P.O. Box 229
Riverdale, NJ 07457
(201) 835-5002
(AU) (DI)
CIRCLE 420

Rittal Corp.
3200 Upper Valley Pike
Springfield, OH 45505
(513) 399-0500
(GP) (IN) (VR)
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Robinson Nugent Inc.
800 E. 8th St.
New Albany, IN 47150
(812) 945-0211
(DS) (DI) (FC) (ID) (ZI) (SM) (CC) (DP) (PG) (CD) (BI)
CIRCLE 422

Rogers Corp.
Flexible Interconnections
2001 W. Chandler Blvd.
Chandler, AZ 85244
(602) 963-4584
(CE) (SM) (CD) (FX)
CIRCLE 423

Rogers Corp.
Composite Materials Div.
One Technology Dr.
Rogers, CT 06263
(203) 774-9605
(ZI) (SM) (CD) (BI) (CO)
CIRCLE 424

Rogers Corp.
Microwave/Circuit Materials
100 S. Roosevelt St.
Chandler, AZ 85226
(602) 961-1382
(CO)
CIRCLE 425

Rogers Corp.
Circuit Components Div.
2400 S. Roosevelt St.
Tempe, AZ 85282
(602) 967-0624
(PG)
CIRCLE 426

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Power Distribution
5750 E. McKellips Rd.
Mesa, AZ 85205
(602) 830-3370
(FX) (BP) (SB) (BU) (GB) (PW) (HN)
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Rosenberger/Micro-Coax div. of UTI
Box E, 245 W. 5th Ave.
Collegeville, PA 19426-0992
(215) 489-3700
(RF) (CX) (CD) (MD) (CO) (HN)
CIRCLE 428

Samtec Inc.
P.O. Box 1147
New Albany, IN 47151-1147
(812) 944-6733
(FC) (ID) (ZI) (SM) (CC) (DP) (PG) (CD) (FL)
CIRCLE 429

Schroff Inc.
170 Commerce Dr.
Warwick, RI 02886
(800) 451-8755
(DI) (ML) (WR) (BP) (PC) (VB) (MB) (BU) (HN) (GP) (BM) (CN) (IN) (VR) (PT) (EM)
CIRCLE 430

Shin-Etsu Polymer America Inc.
34135 7th St.
Union City, CA 94587
(415) 475-9000
(EL) (CD)
CIRCLE 431

Shogyo International Corp.
287 Northern Blvd.
Great Neck, NY 11021
(516) 466-0911
(AU) (CX) (DS) (DI) (SS) (DD) (WR) (PC) (CO) (FL) (TW) (SH) (PW) (HN) (PT)
CIRCLE 432

Shokai Far East Ltd.
9 Elena Ct.
Peekskill, NY 10566
(914) 736-3500
(AU) (RF) (CX) (DS) (DI) (FC)
CIRCLE 433

Stantron
Unit of Zero Corp.
6900 Beck Ave.
N. Hollywood, CA 91605
(818) 841-1825
(BM) (CN) (IN) (VR) (EM) (MI) (CM)

Strongbox
P.O. Box 2726
Culver City, CA 90231-2726
(213) 305-8288
(GP) (MI) (CM)
CIRCLE 434

Switchcraft Inc.
Components Div.
5555 N. Elston Ave.
Chicago, IL 60630
(312) 792-2700
(AU) (CX) (DI) (SM) (CD) (PW)
CIRCLE 435

Techmar Corp.
2232 S. Cotner Ave.
Los Angeles, CA 90064
(800) 832-4627
(MB) (GP) (BM) (IN)
CIRCLE 436

Technit Inc.
129 Dermody St.
Cranford, NJ 07016
(201) 272-5500
(ER) (GK) (VE)
CIRCLE 437

Technology 80 Inc.
658 Mendelssohn Ave. N.
Minneapolis, MN 55427
(612) 542-9545
(BP) (VB) (SB) (MB) (IB)
CIRCLE 438

Tecorp International
Interconnect Div.
19301 S. Santa Fe Ave.
Rancho Dominquez, CA 90220
(213) 764-0040
(CE)
CIRCLE 439

Teradyne Connection Systems Inc.
44 Simon St.
Nashua, NH 03060
(603) 889-5156
(DI) (ZI) (SM) (CD) (ML) (WR) (BP) (PC)
CIRCLE 440

Texas Instruments
Connector Systems
34 Forest St.
Attleboro, MA 02703
(508) 699-5213
(PG) (CD) (MD) (BI)
CIRCLE 441

Thomas & Betts Corp.
Electronics Div.
1001 Frontier Rd.
Bridgewater, NJ 08807
(201) 707-2456
(AU) (RF) (CX) (DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CC) (DP) (PG) (CD) (MD) (CO) (FL) (TW) (SH) (HN) (CA)
CIRCLE 442

Tricon Industries Inc.
Electromechanical Div.
2325 Wisconsin Ave.
Downers Grove, IL 60515
(708) 964-2330
(CD)
CIRCLE 443

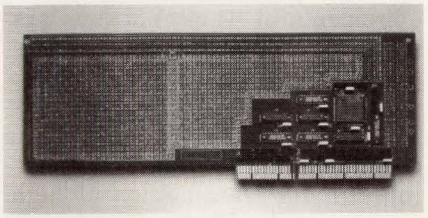
Underwater Kinetics
1020 Linda Vista Dr.
San Marcos, CA 92069
(619) 744-7560
(GP) (IN) (WT) (PT) (EM) (MI) (CM)
CIRCLE 444

Veam
100 New Wood Rd.
Watertown, CT 06795
(203) 274-9681
(AU) (CX) (CD) (MD)
CIRCLE 445

Vector Electronic Co.
12460 Gladstone Ave.
Sylmar, CA 91342
(818) 365-9661
(SS) (DD) (ML) (WR) (BP) (PC) (VB) (SB) (MB) (IB) (BU) (GB) (GP) (BM) (EM) (CM)
CIRCLE 446

(continued on p. 103)
(see p. 103 for key)

▼ PROTOTYPING BOARD CARRIES EISA LOGIC



Intel's EISA bus-master interface chip and glue logic are already installed and connected on the model 4619-8 pad-per-hole active-interface prototyping board. The board gives designers the convenience of solder mounting and the flexibility of bare-board design with the added benefit of having the EISA interface ready to go. The board accepts most component geometries including DIPs, PGAs, and PLCCs. In lots of one to nine, the board goes for $250. Delivery is from stock.

Vector Electronic Co.
12460 Gladstone Ave.
Sylmar, CA 91342
(818) 365-9661
▶ **CIRCLE 474**

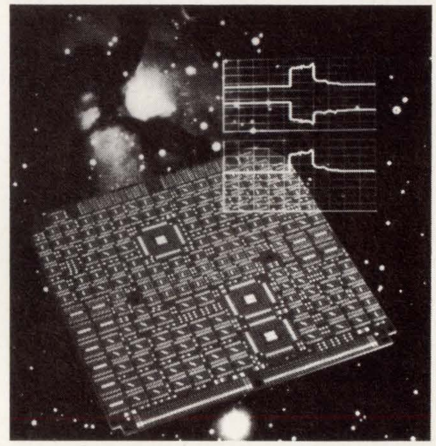
▼ WIRE-WRAP SYSTEM PACKS MORE BOARDS

Up to 20 of the LO-WRAP series of wire-wrap panels fit in an industry-standard 4HP (0.8-in.) pitch subrack, while other wire-wrap systems fit only 10 boards. The design is centered on a new socket design that reduces profile while permitting two full MIL-STD-1130B wraps with 30 Awg wire. The board is available in 26 configurations of board size and pin pattern. Pricing begins at $305 with delivery in four to six weeks from receipt of order.

Mupac Corp.
10 Mupac Dr.
Brockton, MA 02401
(508) 588-6110
▶ **CIRCLE 475**

▼ BOARDS KEEP TABS ON LINE IMPEDANCE

Printed-wiring boards with up to 16 layers are fabricated using advanced modeling techniques that keep line impedences to within ±10% of nominal. End results are modeled with statistical process control, empirical equations, and time-domain reflectometry. The model accurately predicts impedance values and avoids costly trial and error methods. Call for pricing and delivery.



Graphic Research Inc.
9334 Mason Ave.
Chatsworth, CA 91311
(818) 886-7340
▶ **CIRCLE 476**

▼ FAST DELIVERY FOR PRINTED-CIRCUIT BOARDS

A wide range of services are available including fast delivery of pc boards from Master Circuits. Prototypes are routinely produced in as little as 24 hours. All types of boards, from simple single-sided boards to complex multilayer boards with 4-mil lines and 12 layers, are available. Board materials include Teflon, FR-4, PC-75, Cem-1, polyimide, FR-370, and others. All boards are 100% inspected. Call for pricing and delivery.

Master Circuits Inc.
424 Apperson Way North
Kokomo, IN 46901
(317) 457-6605
▶ **CIRCLE 477**

CONNECTOR AND PACKAGING MANUFACTURERS

Vernitron Corp.
Beau Products Div.
P.O. Box 10
Laconia, NH 03247
(603) 524-5101
(AU) (DS) (CD)
CIRCLE 447

Viking Electronics Inc.
21001 Nordhoff St.
Chatsworth, CA 91311
(818) 341-4330
(DS) (DI) (FC) (CE) (SM) (CD) (MD) (BI)
CIRCLE 448

W. L. Gore & Associates Inc.
Electronic Prods. Div.
4755 E. Beautiful Ln.
Phoenix, AZ 85044
(602) 438-2017
(RF) (CX) (CO) (FL) (TW) (SH) (PW) (HK) (HN) (ER) (GK)
CIRCLE 449

WECO Electrical Connectors
Trimex Bldg., Rt. 11
Mooers, NY 12958
(518) 298-4810
(SM)
CIRCLE 450

Wieland Inc.
466 Main St.
New Rochelle, NY 10801
(914) 633-0222
(DS) (DI) (FC) (CE) (ID) (SM) (SS) (DD) (PW) (CA) (GP) (CM) (GK) (TB)
CIRCLE 451

Wilson Case Inc.
P.O. Box 1106
Hastings, NE 68901
(402) 463-5040
(IN)
CIRCLE 452

Zero Corp.
Zero Enclosures
777 Front St.
Burbank, CA 91502
(818) 841-1825
(GP) (BM) (CN) (IN) (VR) (WT) (PT) (EM) (MI) (CM) (ES) (MG) (ER) (GK) (VE)
CIRCLE 453

Zierick Manufacturing
Radio Circle
Mt. Kisco, NY 10549
(914) 666-2911
(ID) (SM) (PG) (CD)
CIRCLE 454

Zoltech Corp.
7023 Valjean Ave.
Van Nuys, CA 91406
(818) 780-1800
(GP) (EM) (CM)
CIRCLE 455

KEY

Connectors and Sockets

(AU)	Audio
(RF)	Radio-frequency
(CX)	Coaxial
(DS)	D-subminiature
(DI)	DIN design
(EL)	Elastomeric
(FC)	Flat cable
(CE)	Card edge
(ID)	Insulation displacement
(ZI)	Zero/low insertion force
(SM)	Surface mountable
(CC)	Chip carriers
(DP)	DIP/SIP
(PG)	Pin-grid array
(CD)	Custom design
(MD)	Military design
(BI)	Test and burn-in
(HV)	High-voltage

Boards and Panels

(SS)	One-sided
(DD)	Double-sided
(ML)	Multilayer
(WR)	Wire-wrap
(FX)	Flexible
(BP)	Backplane
(PC)	Printed circuit
(VB)	VME bus
(SB)	Standard bus
(MB)	Multibus
(IB)	IBM PC bus
(BU)	Futurebus
(GB)	Other bus

Wire and Cable

(CO)	Coaxial
(FL)	Flat
(TW)	Twisted-pair
(SH)	Shielded
(WV)	Woven
(PW)	Power cords/cables
(MN)	Magnet wire
(HK)	Hookup wire
(HN)	Harnesses
(CA)	Cabling materials

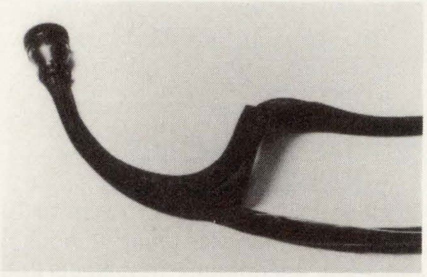
Enclosures

(GP)	General purpose
(BM)	Bench-mounted
(CN)	Consoles
(IN)	Instrument cases
(VR)	Vertical racks
(WT)	Water-tight
(PT)	Portable
(EM)	EMI/RFI design
(MI)	Military design
(CD)	Custom design

Shielding

(ES)	Electrostatic
(MG)	Magnetic
(ER)	EMI/RFI
(GK)	Gasket
(FR)	Ferrites
(SE)	Sheets/strips
(TB)	Tubing
(RC)	Rooms and chambers
(VE)	Vents
(WN)	Windows

▼ SELF-WRAP OVERSLEEVE PROTECTS WIRE HARNESSES

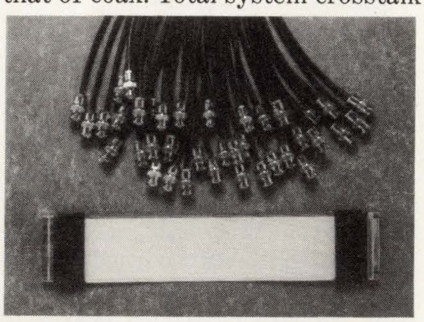


A self-wrapping oversleeve for wire harnesses requires no open ends for application, accommodates multiple breakouts, and is suited for long lengths. The Expando Flexwrap sleeving provides maximum coverage and mechanical protection. The sleeving is offered in two types. Expando DM is rated at 125°C and Expando 686 DM is rated at 200°C. Nominal diameters range from 1/2 to 1-1/4 in. Call for pricing.

Bentley Harris
241 Welsh Pool Rd.
Lionville, PA 19353
(215) 363-2600
▶ CIRCLE 570

▼ RIBBON CABLE NEARS COAXIAL STANDARDS

High speed and high signal fidelity are the hallmarks of the Ribbon-Ax II ribbon cable, which can replace up to 64 conventional coaxial cables. The Ribbon-Ax II cable's electrical performance closely approaches that of coax. Total system crosstalk

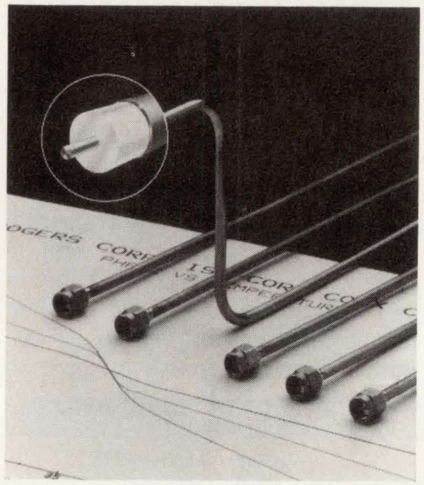


with two lines driven is less than 1% at a rise time of 600 ps. The cable's signal speed is 82% compared with 68% for RG-178 coax. Pricing starts at $0.80 per conductor foot and depends on quantity and cable construction. Call for delivery.

W.L. Gore & Associates Inc.
P.O. Box 51900
Phoenix, AZ 85076
(602) 438-2017
▶ CIRCLE 571

▼ COAXIAL CABLE STAYS STABLE OVER TEMP

Consistent electrical performance over a wide range of environmental conditions is provided by the Isocore Series 100 coaxial cable. The semirigid microwave cable is mechanically and electrically superior to MIL-C-17 cable, Rogers claims. The cable's



dielectric eliminates the expansion and contraction found in standard PTFE dielectrics. Attributes include a 70% propagation velocity and nominal impedance of 50 Ω. Call for pricing and delivery.

Rogers Corp.
One Technology Dr.
Rogers, CT 06263
(203) 774-9605
▶ CIRCLE 572

▼ POWER-SUPPLY CORDS GAIN JAPANESE APPROVAL

The Japanese "T" mark will be appearing on Belden's power-supply cords for appliances and electronic equipment. Products with that mark conform to the Dentori Law, which regulates appliance and materials control in Japan. Approvals are for two- and three-conductor cords rated for 125 V at up to 15 A. All Belden plugs made to Dentori standards use the company's PODSS design, which ensures that there will be no stray strands or shorts within the plug. The company will also offer OEM specials, and is ready to review OEMs' "T" mark requirements. Call for pricing and delivery.

Belden Wire and Cable
P.O. Box 1980
Richmond, IN 47375
(800) BELDEN-1
▶ CIRCLE 573

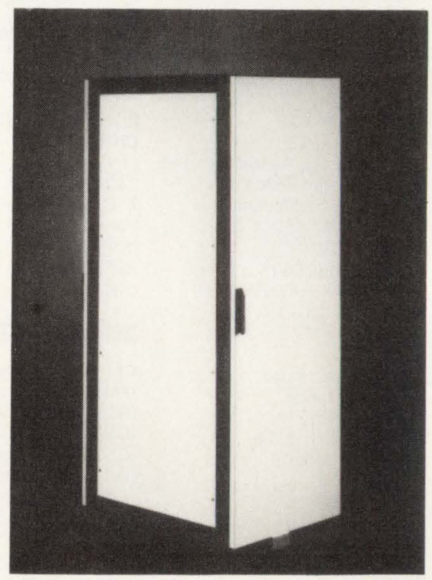
▼ BACKPLANES SERVE 64-BIT VME SYSTEMS

The high-speed and low-crosstalk requirements of 64-bit VMEbus systems using Motorola's 68040 processor are delivered by a line of backplanes from BICC-VERO. The backplanes use 11-layer strip-line construction to provide a good environment for transmission of high-speed signals. They offer full 80 Mbyte/s systems capability. Pricing is in the range of $1300, depending on type and quantity. Delivery is from stock.

BICC-VERO Electronics Inc.
1000 Sherman Ave.
Hamden, CT 06514
(800) 242-2863
▶ CIRCLE 574

▼ SHIELDED ENCLOSURES MEET TEMPEST NEEDS

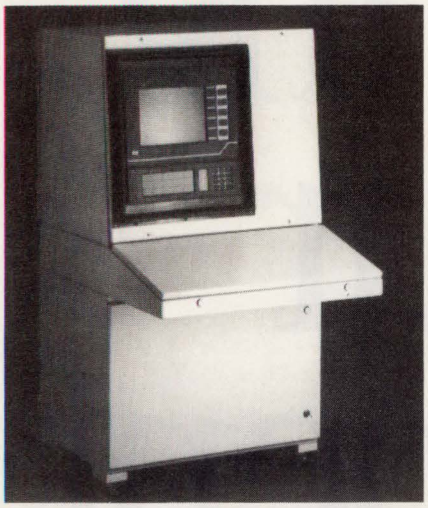
The E^3 Omega line of heávy-duty shielded enclosures protects against electromagnetic environmental effects. Engineered for ultra-high-level shielding in Tempest applications, the cabinets feature 12-gauge steel frame construction. The units' adjustable side struts and externally



removable side panels give maximum access to the cabinets' interior. Cable entry is possible from the top or bottom. In addition, the units are compatible with most AMCO accessories. Call for pricing and delivery.

AMCO Engineering Co.
3801 N. Rose St.
Schiller Park, IL 60176-2190
(708) 671-6670
▶ CIRCLE 575

▼ EQUIPMENT CONSOLE HOUSES WORKSTATIONS



Operator interfaces, workstations, industrial computers, or other CRT-based equipment find a home in the D-10 equipment console. The top module is available in widths of 24, 36, 48, and 60 in. All modules are 30-in. high and 21-1/2-in. deep. The instrument panels can be hinged or held with fasteners.

Hoffman Engineering Co.
900 Ehlen Dr.
Anoka, MN 55303-7504
(612) 421-2240
▶ **CIRCLE 576**

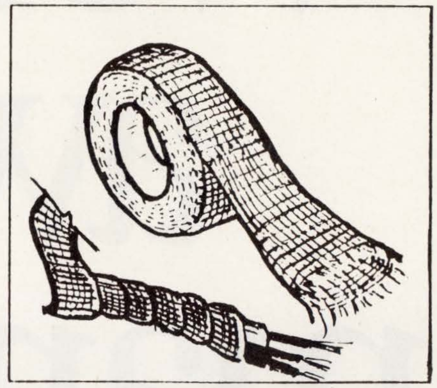
▼ HARDSHELL CASE PROTECTS LAPTOPS

Engineered specifically to protect portable computers, a hardshell laptop case is suited for those who demand durability. The cases are offered in a variety of interiors ranging from custom foam to padded dividers. A wide range of colors and sizes is available. All cases are made of engineering-grade plastic.

Underwater Kinetics
1020 Linda Vista Dr.
San Marcos, CA 92069
(619) 744-7560
▶ **CIRCLE 577**

▼ BRAIDED EMI SHIELDS CAN BE ADDED LATER

The growing EMI problem in cable assemblies is addressed by type XM400-1-100 shielding mesh/tape. The product can be added after the assembly is completed or to make shielding repairs. The two-ply tape, which is made of tinned copper, features a shielding effectiveness of 89 to 90% from 30 to 990 MHz. A 100-ft roll goes for $35. Delivery is from stock to four weeks.



Cole-Flex
91 Cabot St.
West Babylon, NY 11704
(516) 249-6150
▶ **CIRCLE 578**

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▼ VDT SHIELDING DEVICES KILL IMAGE GLITCHES

Effective elimination of disturbances to video images caused by magnetic interference is achieved by using a line of VDT shielding devices. The shields, which are custom fitted to any VDT, will restore color purity and minimize the shaking and flickering caused by magnetic fields emanating from other equipment or power lines. Call for pricing and delivery.

Amuneal Mfg. Corp.
4737 Darrah St.
Philadelphia, PA 19124
(215) 535-3000
▶ CIRCLE 579

▼ SNAG-FREE GASKET SHIELDS ENCLOSURES

A snag-free, track-mounted beryllium-copper shielding gasket is designed specifically for heavy-traffic enclosures. The Rite-Trak gasket incorporates a reverse foldover lip to protect the assembly when the door of an enclosure is opened. The design, which mounts simply and securely, facilitates replacement of damaged or worn gaskets, which can be removed with scissors. It can also be mounted for compression or wiping action simply by snapping it into a separate brass track that's permanently attached to the enclosure with rivets or screws. Call for pricing and delivery.

Instrument Specialties Co. Inc.
Delaware Water Gap, PA 18327-0136
(717) 424-8510
▶ CIRCLE 580

▼ LONG-TERM SHIELD TAPE EFFECTIVELY BLOCKS EMI

A tin-alloy-coated, copper-foil-backed tape features long-term electromagnetic shielding, excellent solderability, and corrosion resistance. Type 1183 tape suits applications calling for reliable point-to-point electrical contact, EMI-RFI shielding, grounding, and static-charge draining. The tape's tin-alloy coating give it good solderability, environmental stability, and corrosion resistance. It comes on a liner that permits easy handling and die-cutting. Call for pricing and delivery.

3M Electrical Specialties Div.
Building 130-3N-46
P.O. Box 2963
Austin, TX 78769-2963
(800) 233-3636
▶ CIRCLE 599

C&C Computers and Communications

The fast way to run RISC.

NEC cache SRAMs maximize RISC processor speed.

You've chosen a RISC processor to drive your speed-intensive system. Now you're looking for memories fast enough to match that high-performance engine.

NEC offers three cache SRAMs for high-speed applications. Two devices are tailored for 25/33MHz MIPS R3000 processors; the third is for any RISC application.

All feature an access time of 15 or 20ns, and all have address latches on-chip to drastically reduce component count in cache memory subsystems. Samples of our 12ns cache SRAM for 40MHz MIPS R3000 processors will be available soon.

If you're running RISC, run it full throttle. With the new cache SRAMs from NEC. For more information, contact NEC today.

Part Number	Organization	Access time	Package
μPD46741	8K x 20 x 2	15/20ns	68-pin PLCC
46710	16K x 10 x 2	15/20ns	52-pin PLCC
46730	16K x 18 or 8K x 18 x 2	15/20ns	52-pin PLCC

For fast answers, call us at:

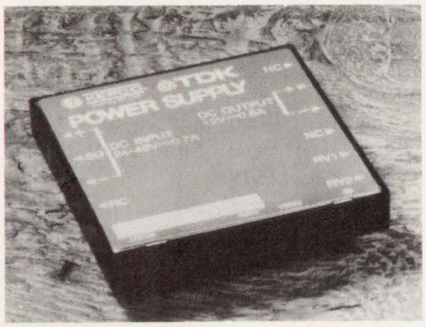
USA Tel:1-800-632-3531. Fax:1-800-729-9288. Germany Tel:0211-650302. Telex:8589960. The Netherlands Tel:040-445-845. Telex:51923. Sweden Tel:08-753-6020. Telex:13839. France Tel:1-3067-5800. Telex:699499. Spain Tel:1-419-4150. Telex:41316. Italy Tel:02-6709108. Telex:315355. UK Tel:0908-691133. Telex:826791. Ireland Tel:1-6794200. Telex:90847. Hong Kong Tel:755-9008. Telex:54561. Taiwan Tel:02-719-2377. Telex:22372. Korea Tel:02-551-0450. Fax:02-551-0451. Singapore Tel:4819881. Telex:39726. Australia Tel:03-267-6355. Telex:38343.

NEC

CIRCLE 132

▼ FORWARD CONVERTERS FIT IN FLAT PACKAGE

For distributed-power applications, 5- and 10-W models have been added to the FPD series of flatpack forward dc-dc converters. The converters require no added cooling for normal operation with inputs of 24 to 48 V dc and outputs of 5, 12, 15, and 24 V dc. Their construction features surface-mounted devices fastened to an aluminum base for efficient thermal coupling. Pricing in single quantities is $45 for the 5-W model and $70 for the 10-W version.



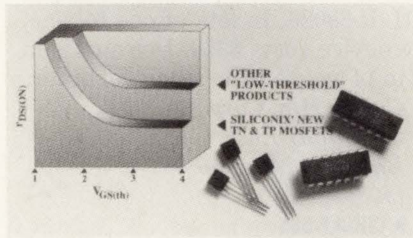
Kepco Inc.
131-38 Sanford Ave.
Flushing, NY 11352
(212) 461-7000
▶ CIRCLE 581

▼ DC-DC CONVERTER HAS ULTRA-HIGH DENSITY

A 0.50-by-2.4-by-3.6-in. dc-dc-converter module uses surface-mounted construction to produce a power density of up to 58 W/in.^{3}. Outputs from the μV 28 series of 200-to-250-W single-output MicroVerters are 5 V at 40 A, 12 V at 20 A, 15 V at 16 A, 24 V at 10 A, and 28 V at 9 A. Direct mounting of heat-dissipating components to the baseplate results in extremely low thermal resistance. Single-piece pricing is $225.

RO Associates Inc.
P.O. Box 61419
Sunnyvale, CA 94088
(408) 744-1450
▶ CIRCLE 582

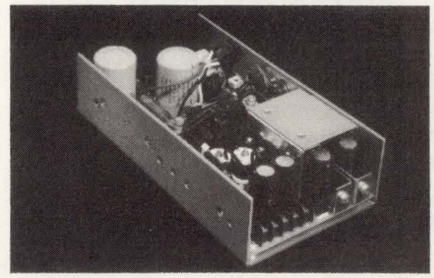
▼ LOW-THRESHOLD MOSFETs SUIT MANY TASKS



Low threshold voltages and low on-resistance values mark 15 power MOSFETs. The TN, TP, and TQ Series are general-purpose devices for use in a wide range of applications from level translation to motor control and power regulation. The $V_{GS(th)}$ of these devices makes them compatible with TTL and 5-V CMOS logic. At TTL levels, they exhibit lower $R_{DS(on)}$ than competitive products. Unit prices range from $0.56 to $4.64 in lots of 1000. Lead times for large lots are four to six weeks.

Siliconix Inc.
2201 Laurelwood Rd.
Santa Clara, CA 95054
(408) 988-8000
▶ CIRCLE 583

▼ 350-W SWITCHER PACKS FOUR OUTPUTS



A 350-W, quad-output switching power supply fills critical applications that call for parallel power sharing for expandable systems or redundant power supplies for reliability. The MPS-354-1224 supply uses Todd's "zero" wire power-sharing technique. The low-profile, open-frame supply has a main output of 5 V at 50 A. It also provides +12 V at 8 A with a 12-A peak capability and an auxiliary output of –12 V at 4 A. Delivery is from stock to six weeks.

Todd Products Corp.
50 Emjay Blvd.
Brentwood, NY 11717
(516) 231-3366
▶ CIRCLE 584

▼ MOTORIZED POT INCLUDES INDICATOR

An avionics-type dial and indicator helps measure or sense the levels or flow of liquids or gases when using the FS-758 motorized potentiometer. The precision device accepts up to 24-V dc inputs to its dc motor. Resistance range is from 1 kΩ to 100 kΩ. The function angle is 340° nominal with others available. The temperature coefficient of resistance is per MIL-R-39023. In lots of one to nine, the device costs $350. Delivery is in 12 to 14 weeks from receipt of order.

Carter Mfg. Corp.
237 Sugar Rd.
Bolton, MA 01740
(508) 779-5501
▶ **CIRCLE 585**

▼ SAW FILTER FOR CELLULAR PHONES

A surface-acoustic-wave, double-mode resonator filter is designed specifically for use in cellular telephones. The SWS-type filters are four-pole devices that feature a low profile as well as linear phase and excellent repeatability. Center-frequency range is from 82 to 95 MHz with a bandwidth of +15 or +12.5 MHz. Call for pricing and delivery.

Toko America Inc.
1250 Feehanville Dr.
Mount Prospect, IL 60056-6023
(708) 297-0070
▶ **CIRCLE 586**

▼ ROTATABLE LED ARRAY LIGHTS LARGE LENSES

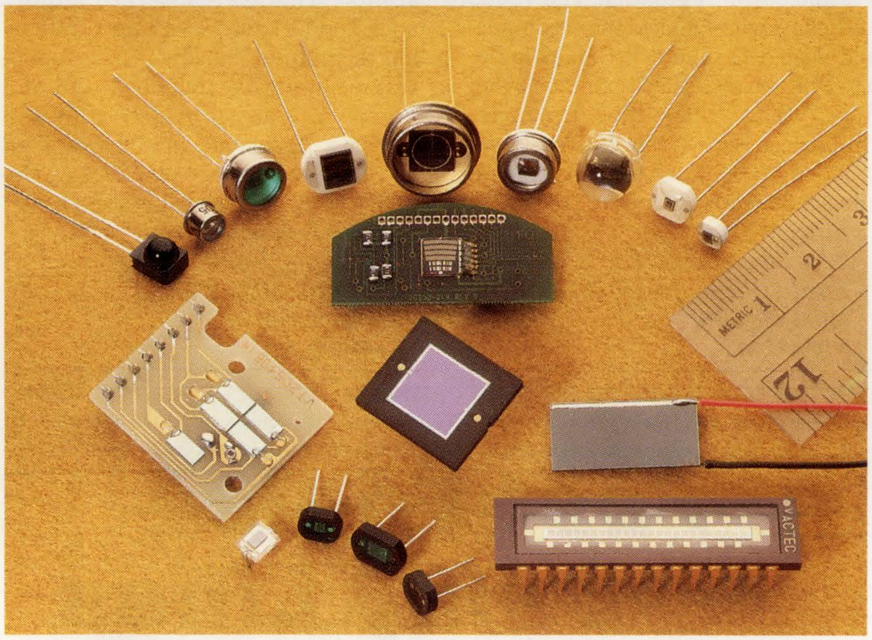
The quandary of replacing incandescent lamps in large illuminated panels has been solved by the MS500 variable LED array. The base rotates freely while maintaining contact with the pc board. Available in T-3-1/4 and T-4-1/2 screw and bayonet lamp bases and T-2 slide bases, the array is intended to light large square or rectangular lenses. Colors include red, amber, amber-yellow, yellow, and green. Pricing starts at $19.18 in lots of 1000. Delivery is in six to eight weeks.

Data Display Products
445 S. Douglas St.
El Segundo, CA 90245-4630
(213) 640-0442
▶ **CIRCLE 587**

▼ 1-mF CAPACITOR BOASTS LOW INDUCTANCE

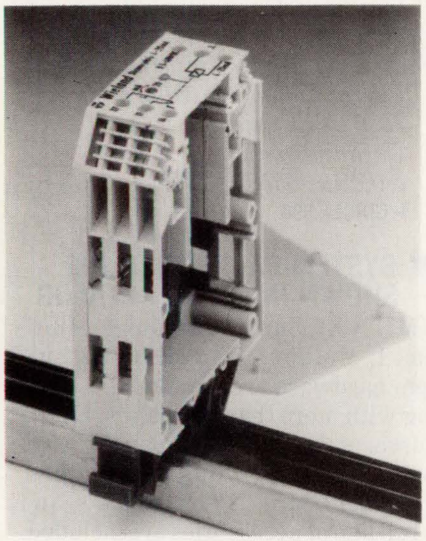
A surface-mountable 1-mF capacitor with low inductance is now available. The 900 C capacitor has an operating-frequency range of 100 kHz to 100 MHz and is rated at 100 V dc from −55 to +125°C. The high-current component replaces tantalum and aluminum electrolytic capacitors and is well suited for dc-bias applications. It also offers low ESR of less than 1/10 of an ohm from 0.1 to 100 MHz. Capacitance values are from 0.1 to 1 mF. Pricing is $3 in lots of 10,000 for 1-mF devices.

American Technical Ceramics Corp.
One Norden Lane
Huntington Station, NY 11746
(516) 547-5700
▶ **CIRCLE 588**



▼ USERS CAN ADJUST CURRENT-SENSING RELAY

A rail-mountable current-sensing relay module works with other Wieland analog modules that process, couple, and convert analog signals. The CSR module is protected against supply reversal and can operate over a range of 9.5 to 40 V dc. Using a po-



tentiometer on the unit, the current level that activates the relay can be adjusted by users between 4 and 20 mA. Delivery is from stock to six weeks. Call for pricing.

Wieland Inc.
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New Rochelle, NY 10801
(914) 633-0222
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▼ LIGHTED PUSHBUTTONS INSTALL WITH EASE

A snap-lock socket-mounting design permits the A3G lighted pushbutton switches to be easily connected to its base for quick installation, replacement, or maintenance. The switches feature oil-resistant service ratings for commercial and industrial applications. Options include SPDT or DPDT contacts with momentary, alternating, or indicator functions and a choice of screw terminals or #110 quick-connect terminals. In lots of 500, prices start at $5.90 for non-lighted versions and $7.80 for lighted types. Delivery is from stock to eight weeks.

Omron Electronics Inc.
1 E. Commerce Dr.
Schaumburg, IL 60173
(800) 62-OMRON
▶ **CIRCLE 590**

▼ LOW-PROFILE PCB RELAY SWITCHES UP TO 14 A

Only 110 mW of coil power is required to actuate the T75 Series pc-board relays. The devices, which stand just 0.591 in. tall, switch up to 14-A loads. Meshing walls separate the relay's motor structure from its contact cavity, ensuring 8-mm clearance and creepage distances as well as 4-kV dielectric strength. Standard coils are available for 3 through 60 V dc. Nominal coil-power needs are 230 mW, typically. Life is 20 million operations. A T75 relay with 1 Form C contacts and a 24-V dc coil goes for $2.29 in lots of 5000. Small quantities are delivered from stock.

Potter & Brumfield Inc.
200 S. Richland Creek Dr.
Princeton, IN 47671-0001
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▼ 16-A ROCKER SWITCH IS ATTRACTIVELY STYLED

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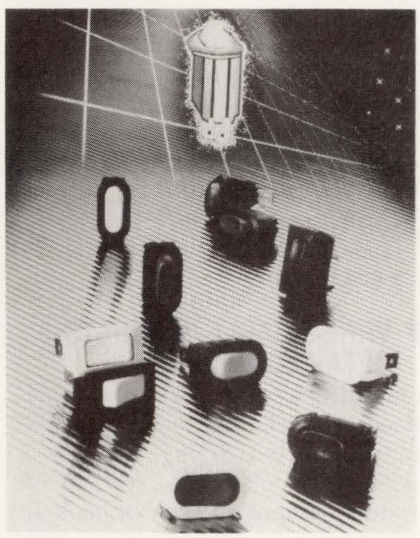

cessed channel extends along the full length of the rocker to promote positive finger positioning. Pricing is $0.57 in lots of 10,000. Delivery is in from eight to 10 weeks from receipt of order.

Micro Switch
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Freeport, IL 61032
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▼ MAGNETIC SHIELDING COVERED IN APP NOTE

A guide to magnetic shielding is contained within a 12-page application note. The booklet includes sections on theory and materials as well as a guide to Amuneal products such as CRT shields, transformer shields, special shields, and heat treatment. Several technical graphs and tables illustrate properties of shielding materials. A section details basic parameters that impact on the design of magnetic shielding.

Amuneal Mfg. Corp.
4737 Darrah St.
Philadelphia, PA 19124
(215) 535-3000
▶ **CIRCLE 593**

▼ OPTOELECTRONICS IN SHORT-FORM CATALOG

Products such as Intelligent Display devices, military high-reliability displays, numeric displays, optocouplers, LED lamps, IR emitters, and more are featured in a 48-page short-form optoelectronics catalog. The catalog includes information on Siemens product-quality programs.

Siemens Components Inc.
Optoelectronics Div.
19000 Homestead Rd.
Cupertino, CA 95014
(408) 725-3524
▶ **CIRCLE 594**

▼ WIRE & CABLE PRODUCTS DETAILED IN CATALOG

A broad spectrum of wire-and-cable-based products are shown in a 272-page illustrated catalog. The book is divided into color-coded sections on product categories such as hook-up wire, communication cable, computer cable, coaxial cable, plenum cable, general-purpose wire, electrical wire and cable, power-supply cords, and more. Full product specifications and ordering information are included.

Carol Cable Co. Inc.
249 Roosevelt Ave.
Pawtucket, RI 02862
(401) 728-7000
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▼ BROAD CONNECTOR LINE INCLUDES SOCKETS

A wide variety of interconnection products is detailed in a 28-page short-form catalog. Products include socket connectors and headers, pc-board transition headers, D-subminis, dual in-line products, card-edge connectors, and many more. Shown are dimensional diagrams, electrical and mechanical specifications, and ordering information.

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(805) 484-0540
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▼ SYSTEM-PACKAGING LINE SHOWN IN LARGE CATALOG

VME, VXI, Sun, Futurebus+, Multibus I, Multibus II, and PC/AT system hardware are detailed in a catalog with more than 250 pages. Enclosures, subracks, backplanes, wire-wrap boards, bus analyzers, extender boards, 19-in. cabinets, and a full line of accessories are included. Also included are backplane pinouts for each bus structure, backplane-design concepts, safety and emissions standards, and enclosure-cooling information.

Mupac Corp.
10 Mupac Dr.
Brockton, MA 02401
(800) 92-MUPAC
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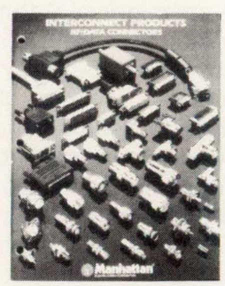
▼ RF/DATA INTERCONNECTS IN 96-PAGE CATALOG



A full line of BNC, TNC, twinaxial, mini-UHF, and F-type connectors are among the products featured in a 96-page catalog. Also included is a complete line of D-subminiature connectors in standard and pc-mounted versions. The catalog is geared toward the OEM, data-installer, and commercial markets.

Manhattan Electric Cable Corp.
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Rye, NY 10580
(800) 288-MECC
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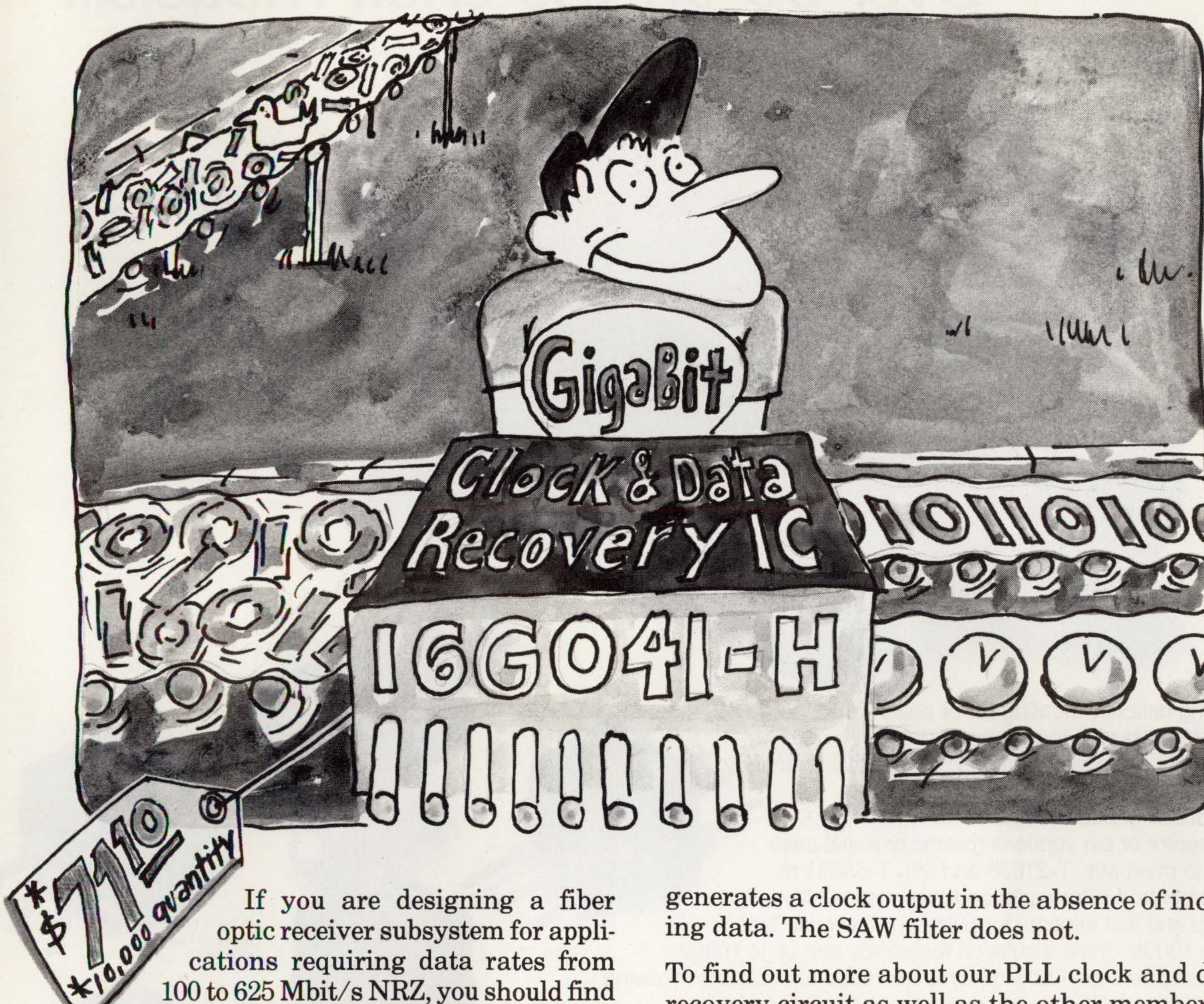

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CIRCLE 84

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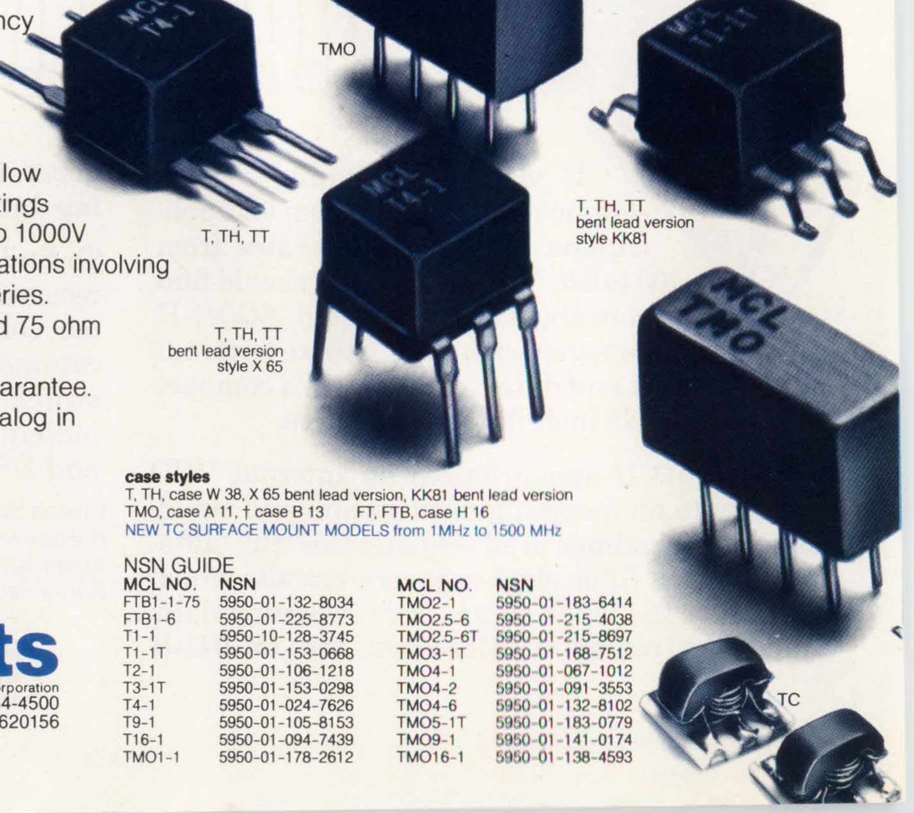

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case styles
T, TH, case W 38, X 65 bent lead version, KK81 bent lead version
TMO, case A 11, † case B 13 FT, FTB, case H 16
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NSN GUIDE

MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

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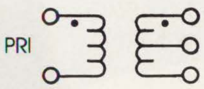
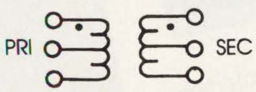
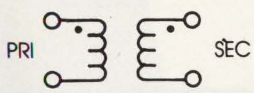
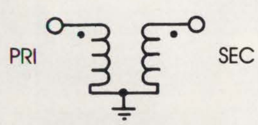
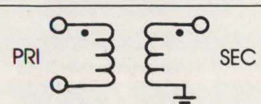
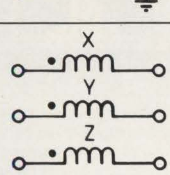
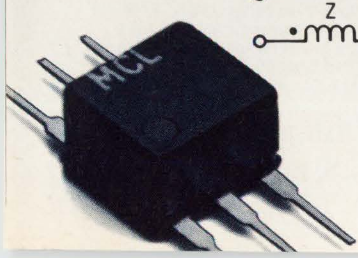
case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	.05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



■ Denotes 75 ohm models

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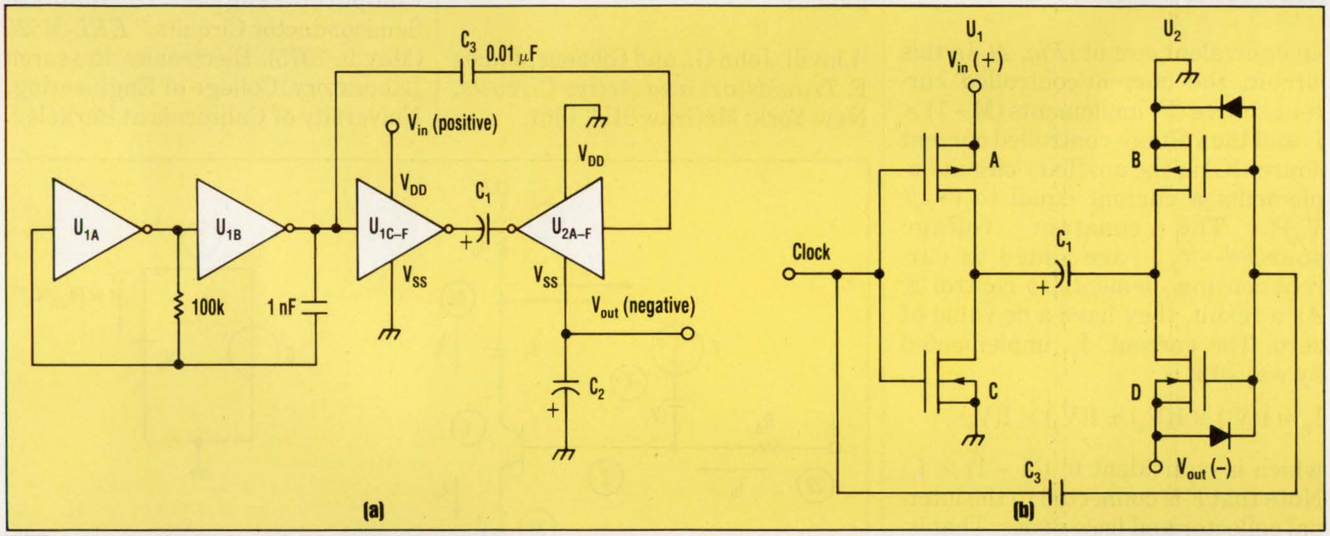
CIRCLE 521 GET NEGATIVE RAIL USING CMOS GATES

DAVID CUTHBERT
Tektronix Inc., TV Waveform Displays Div., M.S. W3 100, P.O. Box 500, Beaverton, OR 97077.

By implementing this inexpensive circuit built with CMOS gates, a negative rail can be obtained from a positive supply. The circuit's input range is 1.2 to 7.0 V, and the no-load loss is only 1 mV. The negative rail can be generated from one 1.5-V cell.

Two 74HC04 CMOS hex inverter chips are used in a charge-pump circuit *(see the figure, a)*. Two gates from U_1 form a 7-kHz clock oscillator. The four remaining gates are paralleled for the positive side of the pump. All six gates in U_2 are paralleled for the negative side of the pump *(see the figure, b)*. When the clock is low, FETs A and B are on and C_1 is charged to V_{in}. When the clock is high, C and D are on. C_1's positive end is grounded while its negative end is connected to the circuit's output. The clock signal is coupled to the input of U_2 through C_3. U_2's input-protection diodes clamp the signal to ground, creating a dc bias across C_3.

The converter output impedance is about 100 Ω and the maximum output current is 10 mA. With an input of 1.5 V, the no-load supply current is 20 μA. With $C = C_1 = C_2$, the peak-to-peak output ripple equals $V_{in}/2RFC$.□



A NEGATIVE RAIL IS OBTAINED from a positive supply by using two 74HC04 CMOS hex inverter chips in a charge-pump circuit (a). In the simplified circuit, C and D are configuraed so that when the clock is high, the positive end of C_1 is grounded while the negative end is connected to the output (b).

CIRCLE 522 SPICE2 MODELS BJT BREAKDOWN

DONALD B. HERBERT
26284 Via Desmonde, Lomita, CA 90717.

Avalanche-breakdown phenomena in bipolar junction transistors has been characterized in literature for a long time.[1,2] The multiplication factor (M) is commonly used to formulize the increase in collector current at or near avalanche breakdown, where:

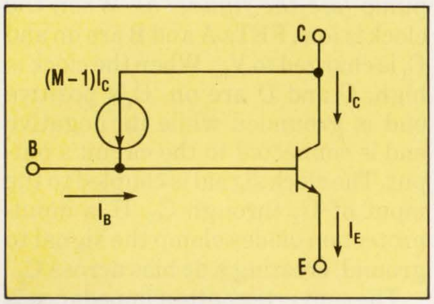
$M = 1/[1 - (V_{CB}/V_A)^N]$.

In this equation, V_{CB} represents the applied collector-base voltage, V_A is the avalanche-breakdown voltage, and N is the breakdown rate. N is an adjustable index depending on material constants and geometrical factors; for a silicon pn junction, N is about 3.

The application of the M factor can be extended with a Spice2 implementation. This is useful to study transistor operation in the vicinity of avalanche breakdown in various circuit configurations.

The multiplication factor can be added to a Spice2 bipolar transistor model in the form of a controlled current source connected from collector to base with a current equal to $(M - 1) \times I_C$ *(Fig. 1)*. This is similar to a previously pusblished approach.[1] Consequently, the added current source implements a total equivalent collector current equal to $M \times I_C$, which reduces to I_C at V_{CB} voltages well below avalanche breakdown.

In Spice2, the augmented transistor model can be implemented with



1. THIS CIRCUIT **serves as a model to implement the avalanche breakdown of a bipolar-junction transistor using Spice2. A multiplication factor (M) is included to control the increase in collector current at or near avalanche breakdown.**

an equivalent circuit *(Fig. 2)*. In this circuit, the current-controlled current source (F) implements $(M-1)\times I_C$ and the voltage-controlled current source (G) in the auxiliary circuit implements a current equal to $(V_{CB}/V_A)^N$. The constant voltage sources—V_{1-3}—are added as current-sensing elements to control F. As a result, they have a dc value of zero. The current, I_F, implemented by way of F is:

$$I_F = I(V_1) \times I(V_3) + I(V_2) \times I(V_3)$$

which is equivalent to $(M-1) \times I_C$. Note that F is connected to the internal collector and base nodes. That is, it's internal to the collector and base bulk resistances, R_C and R_B, respectively, which are added external to the Spice2 transistor model.

The Spice2 coding for the augmented transistor model is supplied in the form of a subcircuit model for a 2N2222A transistor using typical data *(see the table)*. Also, N is defined to be 3 and V_A is 200.

The augmented transistor model is also extended by Spice2 to supply a small-signal ac (frequency-domain) analysis using Spice2's standard approach. In other words, small-signal transconductance and conductance values for F and G are determined by Spice2 from a large-signal dc bias-point calculation. They're incorporated automatically into the small-signal equivalent circuit that includes standard hybrid-pi models of the built-in transistor elements.[3] The

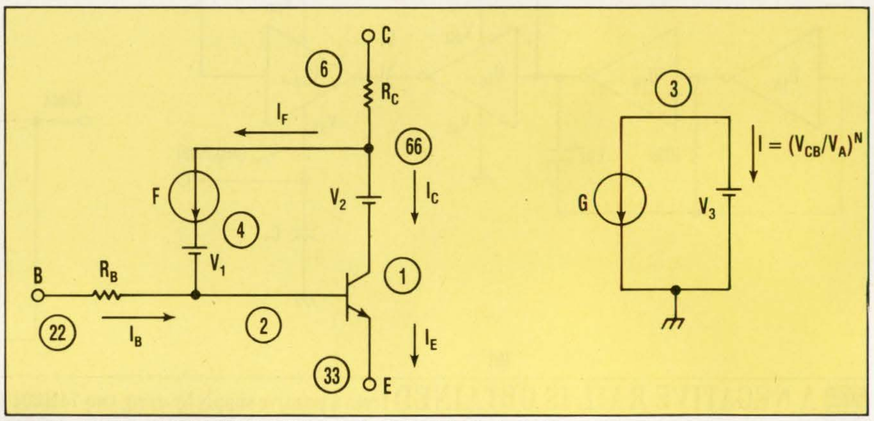
```
.SUBCKT  Q1   6        22        33
*             COLLECTOR  BASE  EMITTER
RB   22   2   7
Q1   1   2   33   G2N2222A
V1   4   2
RC   6   66   0.7
V2   66   1
F   66   4   POLY(3)   V1   V2   V3   0.0   0   0   0   0   0   1.0   0   1.0
*                                              Va=200,       N=3
G   0   3   POLY(1)   1   2   0.0   0.0   0.0   1.25E-7
*                                 P0    P1    P2    P3=(1/Va)**3
V3   3   0
.MODEL   G2N2222A   NPN   (BF=240   IK=.1923   C2=933   NE=2   BR=1   RE=0.007
+CJC=12PF   PC=0.75   MC=0.33   TR=176NS   IS=.0165PA   CJE=20PF   PE=0.75
+ME=0.5   TF=.265NS   VA=55)
.ENDS   Q1
```

small-signal circuit provided can be used to study frequency response and stability when a transistor operates in the avalanche-breakdown region.□

[1]Linvill, John G., and Gibbons, James F. *Transistors and Active Circuits.* New York: McGraw-Hill, 1961.

[2]Fitchen, Franklin C. *Transistor Circuit Analysis and Design.* New York: D. Van Nostrand Co. Inc., 1966.

[3]Nagel, Laurence W. "SPICE2: A Computer Program To Simulate Semiconductor Circuits." *ERL-M520* (May 9, 1975). Electronics Research Laboratory, College of Engineering, University of California at Berkeley.



2. THE ORIGINAL MODEL IS REPLACED **by an equivalent circuit with a current-controlled current source (F) and a voltage-controlled current source (G). Three voltage sources (V_{1-3}) are added to control F.**

CIRCLE

523 CAPACITOR PERMITS HIGHER SLEW RATES

JERALD GRAEME

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; (602) 746-7412.

The slew rate for the widely-used integrator circuit is limited by amplifier phase-compensation requirements. Typically, the op amp chosen for an integrator must be compensated for unity-gain stability, which in turn restricts slew rate. Much greater slew rates, however, are offered by op amps that are phase compensated for higher gains. By employing feedback-factor reduction (which reduces amplifier phase-compensation requirements), integrators can be built around these higher-slew-rate devices.

In this circuit, the OPA637 is compensated for gains of five or more

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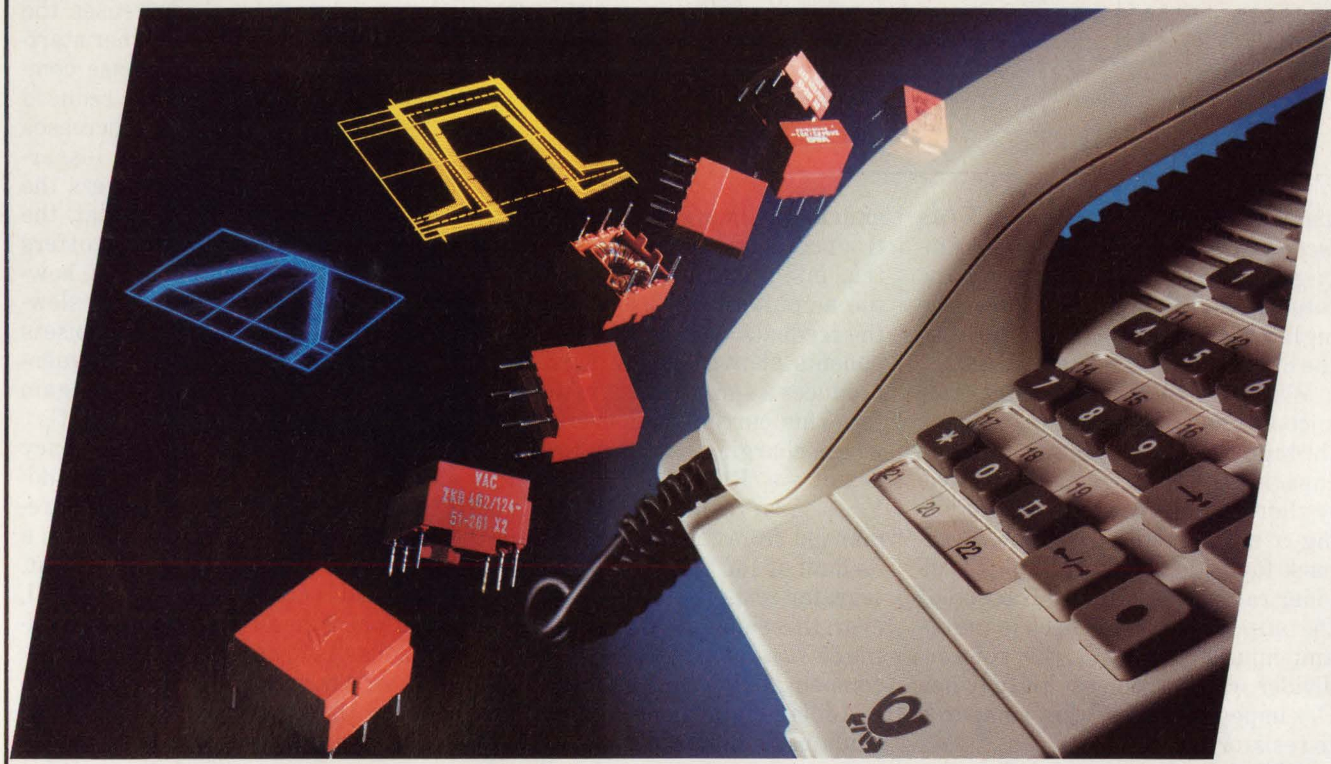

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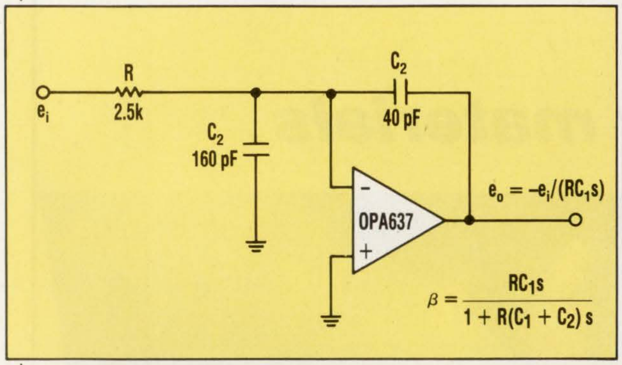
CIRCLE 156



BY ADDING a capacitor (C_2), the integrator feedback factor stays below unity. Thus, higher-slew-rate op amps which are phase compensated for gains greater than unity can be employed.

and supplies a slew rate of 135 V/μs *(see the figure)*. The equivalent unity-gain stable OPA627 has a slew rate of only 55 V/μs. To deliver the higher slew rate to the integrator, the circuit is modified by adding C_2.

Without C_2, the typical integrator encounters a short-circuit feedback through C_1. At high frequencies, the capacitor's low impedance effectively shorts the feedback path, producing a unity feedback factor. Feedback factor is simply the voltage divider ratio reflecting the fraction of the output voltage fed back to the op-amp input. Without C_2, this voltage-divider ratio becomes unity when C_1's impedance is very low compared to resistor R.

Adding C_2 alters the high-frequency feedback factor to reduce the op-amp phase-compensation requirement. With C_2, the voltage-divider ratio between op-amp output and input is reduced. At higher frequencies, C_1's low impedance no longer competes only with R's fixed impedance. Now, R is bypassed by C_2 to counteract the dominance otherwise produced by C_1's falling impedance. As frequency increases, R's significance is still removed, but C_2 retains the voltage-divider action. Ultimately, the high-frequency feedback factor becomes $C_1/(C_1 + C_2)$; this factor is easily made less than unity. Then, the op amp employed needn't be unity-gain stable. The higher slew rate version of the op amp is accommodated by the integrator circuit without concern for frequency stability.

The op amp shown supplies a 2.5:1 improvement in the slew rate available to the integrator. In practice, integrator slewing isn't pushed to the op amp's slew-rate limit. When an op amp is rate limited, the amplifier introduces large errors. To counteract this, integrator slewing is set below the amplifier limit by hand picking the feedback elements. For the components shown, a 10-V level for e_i produces a 4-mA current in the resistor. This current is delivered to C_1 where charging causes e_o to slew at $de_o/dt = e_i/RC_1 = 4\text{ mA}/40\text{ pF} = 100$ V/μs. As a result, the slew rate demanded from the amplifier is below its limit of 135 V/μs and accurate integrator response is retained. However, this slew rate demand is above the 55 V/μs available from the unity-compensated version of the amp.

Adding C_2 doesn't alter the circuit's basic integrator response. Input signal e_i is impressed on R to develop the feedback current e_i/R. This current reacts with C_1's impedance to produce an output voltage of $-e_i/(RC_1s)$. Consequently, the output voltage continues to reflect the input signal's integral. Because e_i isn't impressed on C_2, this capacitor doesn't affect the integrator circuit's basic input-to-output response.

Adding C_2, however, will incur bandwidth and noise consequences and excessive C_2 capacitance should be avoided. Closed-loop bandwidth decreases and noise gain increases as the feedback factor is reduced. The best choice for C_2 sets the maximum feedback factor for the minimum stable gain of the amplifier. Then, frequency stability is assured and the bandwidth and noise degradation is minimized. The maximum feedback factor, β_{max}, meets the optimum condition when:

$1/\beta_{max} = (C_1 + C_2)/C_1 = A_{min}$.

Here, A_{min} is the minimum gain for stable operation of the op amp. From the above expression, the optimum C_2 is defined as:

$C_2 = (A_{min} - 1)C_1$.

With this choice of C_2, only noise performance is compromised for the higher slew rate. C_2 decreases the bandwidth, but from a higher starting point. The reduced phase compensation that requires the reduced feedback factor actually increases amplifier bandwidth. The lesser-compensated amplifier delivers the same bandwidth at A_{min} that the greater compensated version offers at unity gain. Amplifier noise, however, increases with the higher slew-rate option. The op-amp input noise is amplified by $1/\beta$. At higher frequencies, adding C_2 increases noise gain from unity to $1/\beta_{max} = (C_1 + C_2)/C_1$.

At first, it seems that frequency stability is also compromised by adding C_2. This capacitor supplies a return to ground for C_1, resulting in a capacitive load on the op amp's input. The load is $C_L = C_1C_2/(C_1 + C_2)$. Still, this load is small due to practical limitations. As described above, an integrator's output slewing is also limited by the integrator feedback. In practice, any integrator that approaches the op-amp slew rate has a relatively small value for C_1.□

IFD WINNER

IFD Winners for November 22, 1990

Gary Kath and Sandy Hobbs, Sharp & Dohme Research Laboratories, P.O. Box 2000, R80-A18, Rahway, NJ 07065; (201) 594-5225. Their idea: *"Create Control-Panel Labels."*

VOTE!

Read all the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

OFFERS YOU CAN'T REFUSE

A free disk demonstrates the Schema Susie simulator for TTL, CMOS, PLDs, GaAs, microprocessor, and other ICs. With the simulator, designers can perform timing analysis to 10 ps. The disk is available from Omation, 801 Presidential Dr., Richardson, TX 75081; (800) 553-9119.

Intel Corp. will offer a free seminar on analog design to be held in several U. S. cities this spring. Design issues include static discharge, EMI/EMC, noise, and electrical transients. The seminars will be held April 8 in Phoenix; April 10 in Santa Clara, Calif.; April 15 in Boston; April 16 in Minneapolis; April 17 in Chicago; and April 18 in Dallas. For further information or to register, call (800) 548-4725.

The American Association of Concerned Engineers aims to carry on the goals of Irwin Feerst and the Committee of Concerned Engineers. Dues are $10 a year. Membership includes a subscription to the AACE's newsletter, which publishes articles, columns, along with readers' opinions on issues facing engineers. The AACE is concerned with layoffs among engineers and drops in salaries and benefits. In a recent issue, the organization urges reforms in IEEE election policies. Contact AACE Inc., P. O. Box 667, Trilby, FL 33593; fax (904) 567-0433.

A free videotape is available on VRTXdesigner, Ready Systems' simulator for VRTX32-based applications. The software eases development of VRTX32 embedded-systems software by simulating the workings of the VRTX32 kernel. VRTXdesigner is aimed at embedded-system designers building real-time applications with VRT32 and VRTXvelocity. Contact Ready Systems at 470 Potrero Ave., Sunnyvale, CA 94086; (800) 228-1249; (408) 736-2600.

MARKET FACTS

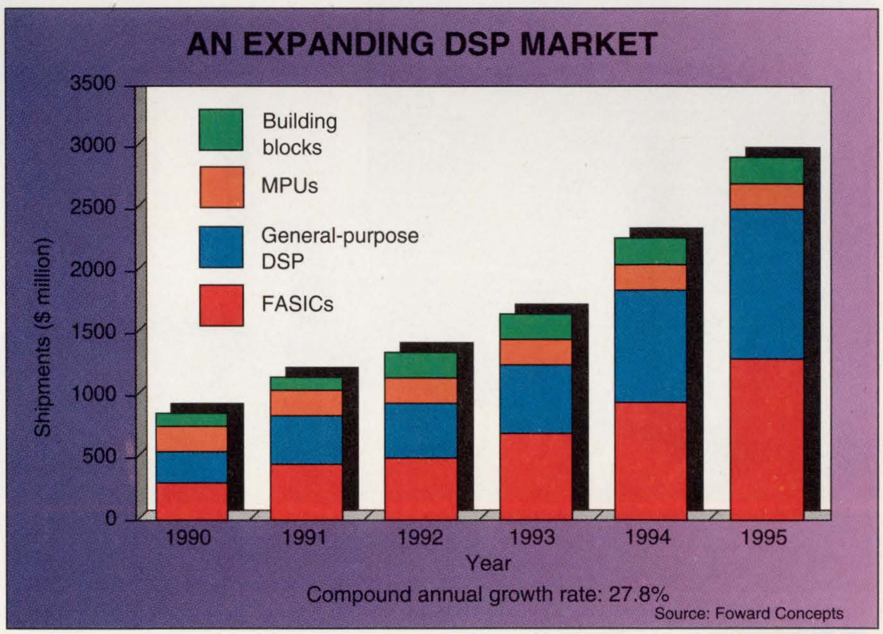
Vigorous best describes growth in digital signal processors. Against the tide of Japanese imports, the U. S. is shipping DSP chips to Japan. NEC, once the world leader in DSP chips, now trails several U. S. companies. Texas Instruments, for one, has captured about 60% of a worldwide market worth about $882 million last year, according to market researcher Forward Concepts. The Tempe, Ariz., market researcher predicts growth at a 28% annual rate to reach $3 billion by 1995.

Some market segments will grow as much as 100% during that time span vs. 14% growth for all ICs by 1995. Not only are DSP chips replacing analog ICs in current designs, but new application areas are opening up for these fast DSP chips.

The DSP IC market consists of DSP chips and function and alogorithm-specific (FASIC) chips. Sales of DSP chips are expected to grow from $285 million in 1990 to hit $1.3 billion in 1995. These chips are going into modems, disk drives, cellular phones, and consumer entertainment products.

Behind market leader TI are Motorola, with about 10.2% of the world market, NEC, with 9.1%, AT&T, with 8.4%, and Analog Devices, with 6.3%. Fujitsu and Oki are turning away from the general-purpose market to concentrate on modem and other non-programmable DSP chips.

In the FASIC arena, other hot areas are video compression, multimedia, high-definition TV sets, chips to augment CD/DAT stereo chips and speech chips for answering machines. This market sector is expected to grow from $392 million last year to $1.4 billion in 1995. Another growth area is that for alogrithm-specific devices in military and medical-imaging markets, which is expected to grow at a 12% compound rate.



DID YOU KNOW?

... that the U.S. share of the $814 billion world electronics market (including software and data processing) dropped from a 47% share in 1984 to 38% in 1989.

Electronic Industries Association

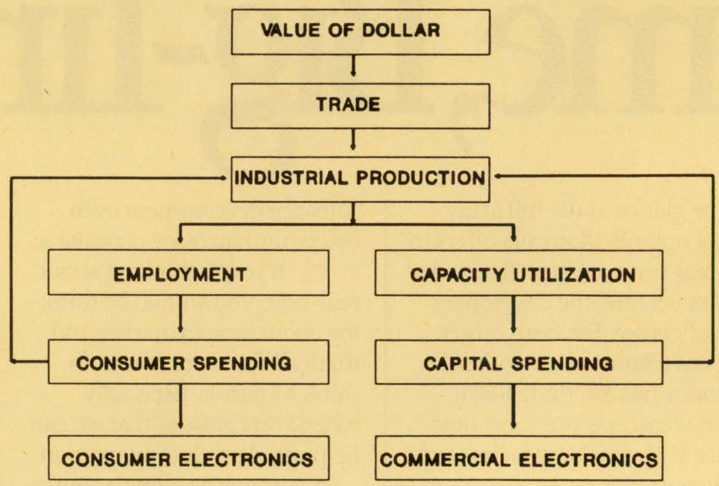
Motorola's In Real

QUICKLOOK

EYECATCHER

In a recession, as the value of the dollar drops, U. S. exports pick up and imports slow. So predicts Henderson's Electronic Market Forecast. Stepped-up exports give a boost to industrial production and use of manufacturing capacity. This in turn stimulates capital spending to increase production capacity and make it more efficient (right). Capital spending creates direct spending for commercial electronics such as communications, computers, and industrial electronics. A similiar pattern produces increased spending for consumer electronics (left), especially automotive products.

SHORT-TERM ELECTRONIC INDUSTRY FORCES



Source: Henderson Electronic Market Forecast

HOT PC PRODUCTS

Have you ever struggled to proofread a computer screen or wished that your electronic messages could be read aloud? From First Byte, Monologue 2.0 converts text or ASCII data into speech using phonetic translation and pronunciation rules. Examples include spreadsheets, word processors, databases, and e-mail.

Any pronounceable combination of letters and numbers can be spoken; pronunciations can be corrected. Monologue is a terminate-and-stay-resident program (TSR) that can be activated by a hot key. Programmers who'd like to add speech to an application can license the software. Monologue, which lists for $149, works with IBM PCs, XTs, ATs, PS/2s, or compatibles, with at least 384k. Look for a Windows 3.0 version in April. Contact First Byte, 3100 South Harbor Blvd., Suite 150, Santa Ana, CA 92704; (714) 432-1740.

Although it can use the speaker built-in to PCs, Monologue also works with speech accessories like Covox's Speech Thing. It is an 8-bit DAC that connects in line to a PC's parallel printer port. The unit converts digitized or synthesized speech from a software program's sound file. No speech card is needed. The software includes a talking calculator, blackjack game, music keyboard, and sound editor. The Speech Thing lists for $79.95, works with the foregoing PCs, and requires 256k, DOS 3.0, and GW Basic. Covox Inc., 675 Conger St., Eugene, OR 97402: (503) 342-1271.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458, fax (408) 253-6085

In the March 14 column, I shared with you one of my experiences in creating a project model. Getting people involved in modeling and planning was the only way I could get individuals and groups to set priorities, focus their energies, understand their roles, encourage collaboration, elicit creativity, and develop a spirit of shared responsibility. This effort must be a shared experience; a shared plan cannot be done with only a computer system. To do the planning exercise justice, one must create and manage information and communication among many people. Research and development, marketing, and manufacturing work in a highly interactive mode. Because of tight coupling between individuals and the complete removal of functional partitions, the product's developers must fully understand who needs what from whom and who will do what by when.

Producing the network model captures the dependencies as it describes the flow of work leading to the resultant new product. The database created from the modeling exercise becomes instrumental in reaching time to market goals. Also, the information produced from the data makes it possible to observe the process visually and graphically. You need the freedom to easily modify large network models, create new branches and networks, and see the entire picture while these changes are taking place. It's quite likely that the modeling of projects requires the visual manipulation of hundreds to thousands of elements to complete the development of a realistic hierarchical and network model.

Tools and techniques should be easy for people to learn and handle. People must be encouraged to produce models that are based on familiar techniques like writing entries on a calendar or generating a to-do list. The team developing the shared plan does not have the time to send everyone off to planning school to make their team members effective hierarchical and network thinkers. Training must be quick and accurate. Ideally, the tools and process should eliminate, or greatly reduce, the need for structured training by relying on information and skills that most people already have. Where possible, those skilled in understanding concepts and using tools should help develop the skills of their coworkers.

QUICKLOOK

TIPS ON INVESTING

A man on a British TV talk-show was asked, "To what do you attribute your exceptionally long life?" The man thought a moment and replied, "To bad luck, mostly." With a little luck and modern medicine, most engineers can expect to live into their 80s and beyond. Longevity, while a blessing, increases chances of needing long-term health care.

According to the U. S. Bipartisan Commission on Comprehensive Health Care, two million Americans over age 65 live in nursing homes. By the year 2030, that population will more than double. The average nursing home bed costs over $30,000 per year, with some running as high as $80,000. As a result, a serious illness could devastate your net worth—and your carefully laid retirement plans. One remedy is long-term health care insurance. A good policy makes it possible to protect your assets and your income from huge medical bills.

Look for a policy that includes all these features:

- **No prior hospitalization requirement.** You receive benefits whenever you need them, without having to prove a preexisting medical problem.
- **Lifetime coverage option.** Many people have purchased policies, only to have their coverage canceled when ill health strikes.
- **Inflation protection.** Your benefits should keep pace with health-care inflation, currently estimated at 12% per year.
- **Limited exclusions.** Make certain that Alzheimer's disease, senility, and related cognitive impairments are covered.

Most important, purchase your policy from a financially sound institution. Look for a top (A+) rating by A. M. Best, the insurance industry's most widely respected rating service.

While the cost of this protection varies, the constant is that the younger you are when you purchase a long-term health care plan, the lower the cost and the higher the daily benefits. A typical plan might cost a 55-year-old policyholder $850 per year. But if that policyholder waited until he was 75 to purchase the same plan, his premiums might be more than $3,500 a year. Daily benefits for the 55-year-old also might be up to 40% more than those for the 75-year-old. Each policy differs.

An engineer should weigh the purchase of a long-term health care policy according to his circumstances. Write for the Health Insurance Association's free pamphlet, "The Consumer's Guide to Long-Term Care Insurance," which lists companies offering these policies, from HIAA, P. O. Box 41455. Washington, D. C. 20018.

Finally, consider that the chances of having a fire are less than 5%, yet none of us would dare be without fire insurance to protect our homes. Unfortunately, our chances of needing long-term health care are many times greater than that. For a free copy of "The Changing American Dream: the Real Definition of Retirement," a Shearson Lehman Bros. publication, call or write to me at the address below.

Henry Wiesel is a financial consultant with Shearson Lehman Bros., 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221.

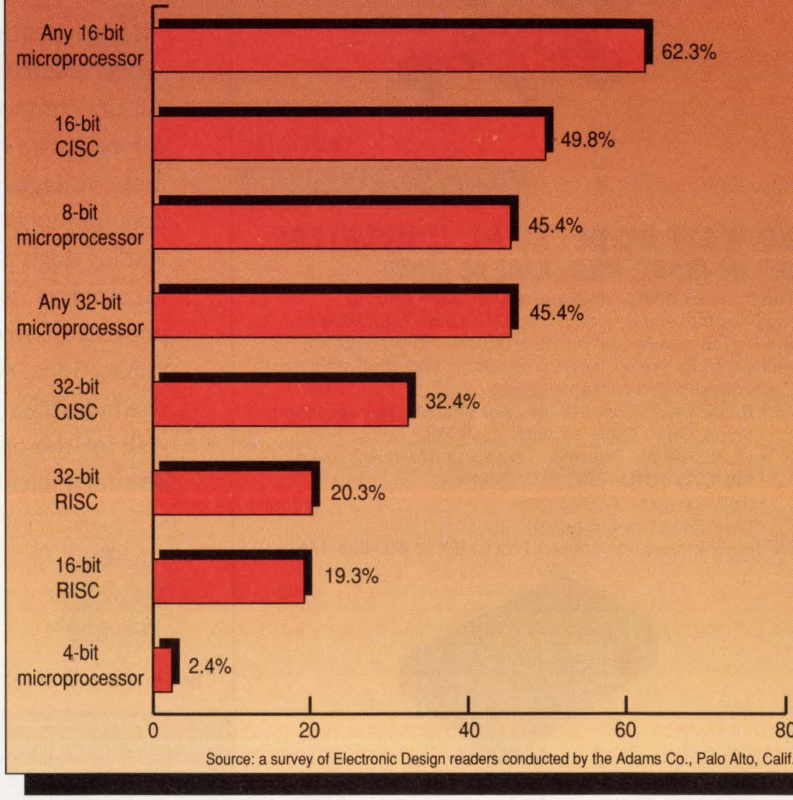
QUICK NEWS: THE PROFESSION

Engineering students receive a 50-year-old set of tools and a view of technology that is five years out of date by the time they reach the workplace, says Joel Orr, an expert on manufacturing automation. That's why Orr has started the League for Engineering Automation Productivity, or LEAP. His goal is to bring automation to engineering and bring engineers up to speed on automation. Orr hopes to sign up 5,000 engineers by the end of the year.

LEAP is assembing a demonstration center of workstations from the likes of HP, Silicon Graphics, and Sun. The center, in Virginia Beach, Va., has room for 18 workstations at a time, with vendors loaning them for about six months at a time. That way, the center stays current.

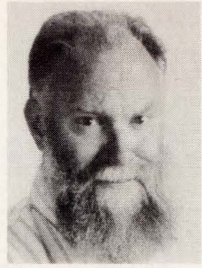
A $25 yearly membership buys a newsletter, use of the demo center, discounted attendance at the Congress on the Future of Engineering, to be held July 1–2, in the Washington, D. C area, publications that have case studies and how-tos, a series of product-recognition awards, based on the votes of members, sponsored research projects, and regional seminars. LEAP's first research project is a study comparing the quality of engineering graduates with industry expectations. It will also examine engineering educators' evaluations of their students, compared with the graduates' acceptability to industry. It will rank schools in terms of their graduates' computer literacy. Contact LEAP: (800) CADDCAM or (804) 495-8547.

WHICH MICROPROCESSORS WILL YOU USE IN DESIGNS IN THE NEXT 12 MONTHS?



Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

PEASE
PORRIDGE



BOB'S MAILBOX

Dear Bob:

Sure enjoyed your Spice article in Electronic Design. I've followed your musings for years, gosh, decades. Please don't ever stop. There is another aspect of the simulation thing. It is a matter of philosophy, I guess, and it has concerned me for a long time: The sense of accomplishment that comes from doing something the first time. Once you've done it, you've done it (how many endure the agony of climbing Mount Everest a SECOND time?). In the real world, this concept is intuitive, I think. But in the world of simulation, we confuse what we have accomplished with what we have imagined; worse yet, what the computer has imagined! Dreams and reality mingle, and we are led astray.

Case in point: Stirling engine development (one of my loves) has gone high tech. The talent and money is flowing toward the computer, not the lathe. We simulate, learn, simulate, etc. Each time we make an improvement it is rewarding, and provides the psychological boost needed to continue. Because it isn't so rewarding to do the same thing again, we don't bother to repeat in metal what we've already "built" on the screen. Soon the simulation errors compound until there is no way to distinguish dreams from reality.

I sometimes wonder if we could have experienced the industrial revolution at all, if somehow the computer had already existed. It is very tempting to simulate a thing rather than constructing it.

Simulation ain't the same as really doing it. Perhaps a close parallel? Or, to say it another way, is it possible that the boob tube in the office takes us on the same sort of journeys as the boob tube at home?

DARRYL PHILLIPS
President
The Airsport Corp.
Sallisaw, Okla.

I couldn't agree more. -RAP

Dear Bob:

I just finished reading your column "What's All This Spicey Stuff Anyhow? (Part 1)" in the Nov. 22 issue and I thought I'd share my own experiences with circuit simulation and EE education with you.

I am 33 years old, and was trained in math and computer science. Two years ago, I decided to pursue a Masters degree in EE at a well-known northeastern university. I told the boss that I was going to specialize in the mathy end of EE, like Control Theory, Signal Processing etc., but I had a hidden agenda. I wanted to learn electronics.

It's all worked out because I have learned electronics, but only sort of. You see, at this institution's outlying campuses, where they crank out BSEEs and MSEEs by the score, there are no labs. I repeat, no labs. No breadboards, no scopes, no components, no nothing. Any design that takes place is on the computer using a circuit simulation program. I have suggested to several professors that a real live lab would be very helpful, but they just "hurrumph" about the computer being just as good as a learning experience. So you see, it's not just lazy (young or otherwise) engineers copping out on the design process, it's the educational system taking the path of least resistance.

I have improved the situation for myself somewhat. I designed and built a dc power supply (you're probably saying "big deal," but that's pretty good for a mathematician!) I bought a breadboard, a selection of components, and a digital meter. With this setup, I can do quite a bit of experimenting on my own. My father, an "old tyme" electrical engineer, is so glad that his mathematician son has seen the light that he's salvaged an old scope from who knows where for me. I'm looking forward to its arrival.

As far as my experiences with the circuit simulation program are concerned, I concur with your opinion. We didn't use Spice, but some other Spice-like program. It was graphically oriented and very user-friendly, but it had the same crazy convergence problems that you describe. One project we had was to design an analog multiplier. Changing the quiescent current through the Gilbert cell ever so slightly made the difference between fast convergence for steady-state analysis and sitting for 15 minutes watching the cursor blink. Then, to add insult to injury, the case that converged for steady-state analysis didn't converge for Fourier analysis. I finally was forced to give it up. Interestingly enough, my professor accepted "Program Did Not Converge" as a correct answer.

CHRISTOPHER LENNON
Bedford, Mass.

Ouch! This guy's heading in the right direction, but the schools aren't. -RAP

Dear Bob:

I feel that your most recent column (Spice, Part II) needs some comment. You say, "I don't think you can beg or steal or borrow or buy a model of a transistor that's guaranteed." First, to what kind of transistor are you referring: bipolar, JFET, MOSFET, small signal, large signal, power, microwave, discrete, integrated devices?

Second, your statement implies that a single "transistor" model should be guaranteed to "run" under all conditions. Suppose I suggest that you should be able to design a single OP AMP that works equally well for all applications? I suspect that you would not only laugh in my face but that you would think to yourself that I am a fool for having made the suggestion in

PEASE PORRIDGE

the first place. Well, to suggest that a single transistor model should "run" under all conditions is equally laughable. Am I hitting below the belt?

Third, you seem to want to place the total responsibility for the success of the model upon that person who developed the model. However, I get the impression that you have no sympathy (or respect?) for a user of one of your op amps who misuses your op amp. Below the belt again?

Fourth, you seem to believe that those "transistor" models which have been built into the circuit simulation program Spice represent the complete set of models from which one can choose. The sad truth is that those "transistor" models built into Spice represent just about the worst set of models from which one can choose. Why is that the case? Because industry gets those models for free from the Univ. of Calif. at Berkeley as the result of student slave labor and typically is not willing to pay the price for truly physical and accurate models.

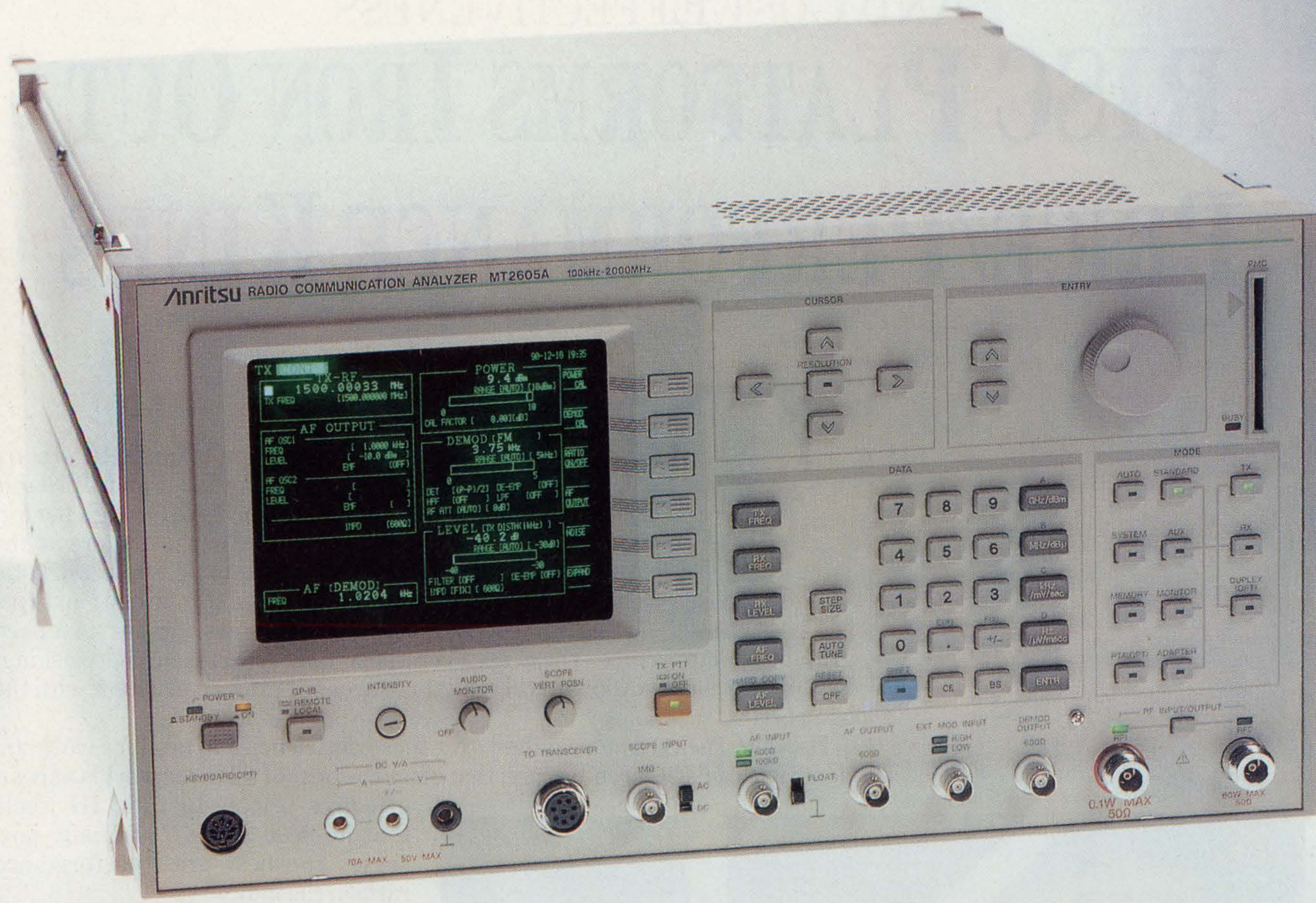
....You suggest that you may wish to BUY a guaranteed transistor model. Well, you can. My company has developed and markets Spite (SPI Transistor Emulator), the world's best CIS/SIS (MOS if you prefer) transistor model. The Spite model does employ physically meaningful parameters and parameter values. It also simulates, with unprecedented accuracy, a transistor which is properly used. Would you like to guarantee me that your op amp will always "run" for me no matter what I do to it? There just isn't any point in building a lot of unnecessary complications into the model to protect the unknowledgeable user from himself.

So what do you want your guarantee to say? Send me a reasonable specification and a purchase order and I will write your guarantee for you.

DR. JAMES E. SMITH
President
Semiconductor Physics, Inc.
Escondido, Calif.

I use mostly bipolars, but for CMOS this looks tempting! -RAP

Greater Range and Total Ability 100kHz to 2GHz



Anritsu's new MT2605A Radio Communication Analyzer is all you need for comprehensive radio testing. This single instrument can perform 14 separate tests in just 2 minutes. Plus, it covers the wide range from HF and VHF to UHF, and up to quasi-microwave spectra.

In fact, it's like 10 pieces of equipment in one.

The MT2605A is a signal generator, AF generator, frequency counter, power meter, modulation meter, AF level meter, distortion meter, oscilloscope, DC voltmeter and DC ammeter, all in one easy-to-use instrument.

Digital test capabilities include burst measurement.

In addition, the Personal Test Automation (PTA) software option even allows users to create custom test programs and store them on convenient Plug-in Memory Cards (PMC).

Features

- Frequency range: 100kHz to 2GHz
- Digital system testing:
  Burst measurement
  Bit error measurement (option)
  Digital modulation measurement (separate unit)
- Accurate, high-stability signal generator
  Setting resolution: 10Hz (available for narrow band systems)
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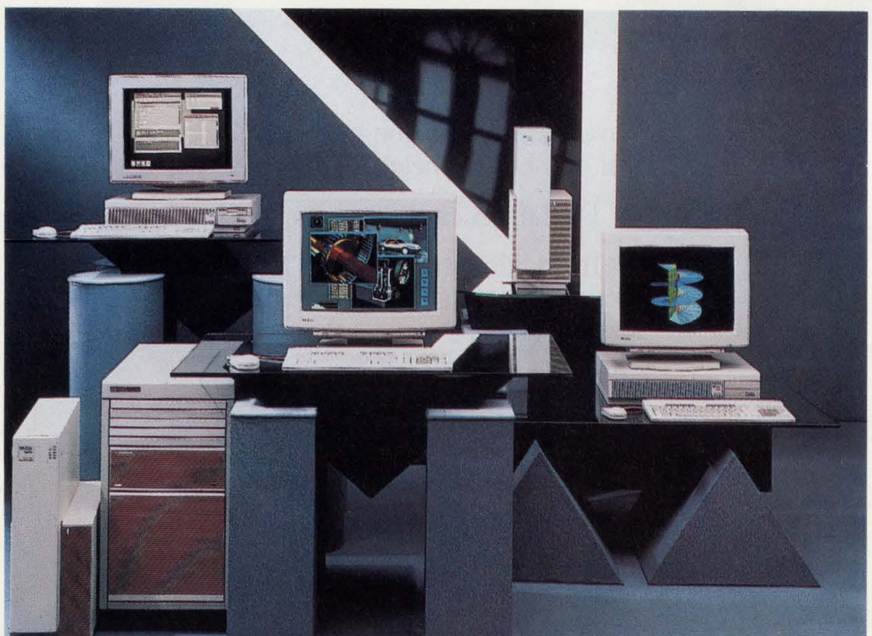
PRECISION-ARCHITECTURE WORKSTATIONS EXCEL AT COMPUTATIONAL POWER, GRAPHICS, NETWORKING, AND COST-EFFECTIVENESS.

RISC PLATFORMS IRON OUT PRICE/PERFORMANCE KINKS

RICHARD NASS

Through RISC technology, workstation manufacturers are able to build high-performance platforms at an affordable price. However, many of these platforms offer high performance in terms of one or more specific parameters at the expense of other parameters. For example, some workstations emphasize mainly computational throughput in terms of MIPS, MFLOPS, etc. Others stress mostly advanced graphics performance. There are even those that specialize in networking. Few, if any, workstations excel in all three areas at prices consistent with the use of RISC technology.

Hewlett-Packard pole-vaulted over these deficiencies to produce workstations, with a RISC architecture, that offer the best of all three worlds at cost-effective prices. In fact, HP feels that its 9000 Series 700 family possesses the best price/performance ratio in the industry.



1. HP'S 9000 SERIES 700 WORKSTATIONS consist of the models 720 (left), 730 (right), and 750 (center). The 720 and 730 are configured similarly, but the 730 contains a 66-MHz processor while the 720 contains a 50-MHz processor. The 750, which also has a 66-MHz processor, has four expansion slots and up to 192 Mbytes of RAM.

The RISC architecture in the Series 700 platforms is called PA-RISC, for precision architecture. HP has been using the highly-scalable PA-RISC processors since the mid 1980s. For this reason, over 2000 compatible applications exist throughout commercial and technical markets. These include scientific, design automation, mechanical CAD (MCAD), financial, CASE, artificial-intelligence, and data-transaction-processing applications.

The PA-RISC architecture delivers its high performance as a result of three factors: a sophisticated and scalable architecture, a state-of-the-art submicron CMOS manufacturing process, and a leading-edge compiler technology.

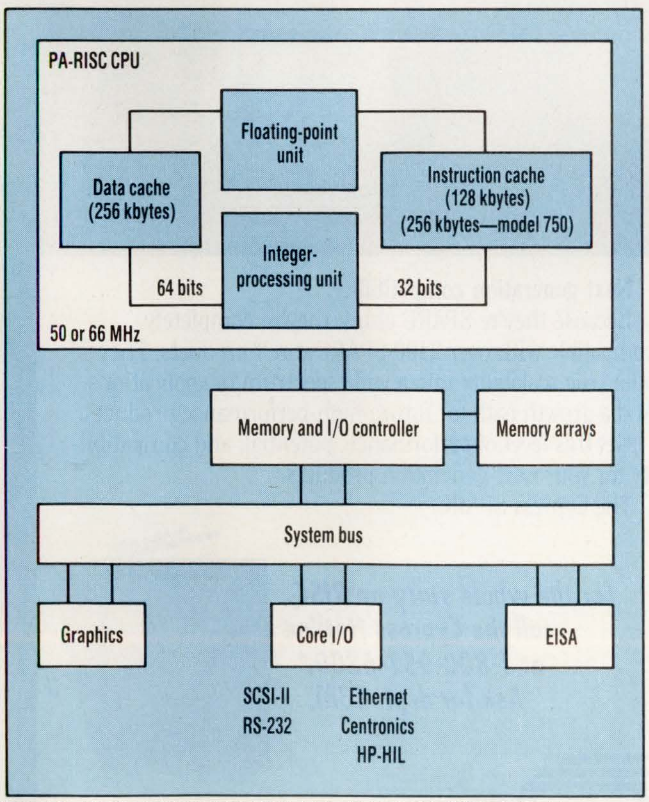
HP placed a large emphasis on the chips' manufacturing process. The way the gates are laid out on the chips allows the clock rate to be sped up without any degradation of performance. The company uses their internal manufacturing process to run the chips at a high clock rate with a fairly low power consumption and heat dissipation.

The workstation family consists of three members, Models 720, 730, and 750 *(Fig. 1)*. The low-end 720 delivers more than 57 MIPS, 17 MFLOPS, and 55 SPECmarks of performance for under $12,000. HP claims these specifications aren't available anywhere else at this price. "It's the best price/performance deal available anywhere in the workstation market," states Joe Raffa, HP's Product Marketing Manager for PA-RISC Workstations.

The high-end 750 imparts specifications of 76 MIPS, 22 MFLOPS, and 72.2 SPECmarks. It's expandability is evident with four available EISA slots. The Model 730 fills the void between the 720 and 750. It offers the same performance specifications as the 750 but contains less memory and isn't as expandable. It has just one EISA slot.

The 720 is based on a 50-MHz microprocessor, while the other two incorporate 66-MHz processors. The 720 and 730 come with 16 to 64 Mbytes of RAM and up to 840 Mbytes of internal storage capacity. The 750 can support up to 192 Mbytes of RAM and 2.6 Gbytes of internal storage. It also has 256 kbytes of cache memory, while the other two models contain 128 kbytes. Internal removable mass-storage devices are supported, including a CD-ROM, digital audio tape, and a 3.5-in. floppy-disk drive. External storage devices enable the 720 and 730 to store up to 10 Gbytes and push the 750 to 40 Gbytes.

All three of the Series 700 workstations are compatible with the fiber distributed data interface (FDDI) network. This stays in line with HP's belief that cooperative computing will be a major concern in the near future. Cooperative computing means distributive and network computing, or the ability to use computing resources around the network at the user's disposal in a sophisticated manner.



2. THE PRECISION-ARCHITECTURE (PA) RISC CPU runs at 50 or 66 MHz. The increased graphics performance results from coupling the CPU with the memory and I/O controller. The system bus connects to the graphics subsystem, the EISA bus, and SCSI-II, RS-232, and Ethernet ports.

All three of the Series 700 platforms share common user interfaces: X-Windows, HP-VUE, and the same release of the operating system, HP-UX. Because the OS has existed since the early 1980s, many applications are ported to it. The software comes preinstalled and preconfigured through a feature called Instant Ignition, which helps users get their systems up and running as quickly as possible. Users just unpack the computer and turn it on. This feature has been offered for about the last 18 months. HP also contends that the three systems will support OSF/1 when it becomes available, probably before the end of 1991. These are the first HP offerings to make that claim.

EISA Does It

HP designers also stringently adhere to hardware standards. They chose the EISA bus partly because of the 33-MHz performance level it's capable of attaining, and partly because of their goal to stick to standards. This is HP's second family to incorporate the EISA bus (the Series 400 was the first). HP previously used a proprietary backplane for its products and the ISA bus for the Apollo platforms, which the company later acquired. With the EISA bus, users can have access to an overwhelming amount of hardware and software.

The workstations' design focused heavily on improving floating-point and graphics performance and tightly integrated floating-point and integer-processing units. Some special instructions were added to increase parallelism, such as multiple execution of floating-point and integer instructions.

HP engineers custom-designed the memory and I/O controller to offer high-bandwidth access to the memory arrays and the system bus. The controller has built-in intelligence to help with certain elements of graphics performance, including the raw throughput needed to draw vectors as well as a number of preprogrammed graphics functions. Coupling the CPU and the memory-controller chips forms the basis of the graphics performance *(Fig. 2)*. This balances system performance, which means that the CPU's integer and floating-point operation are as fast as the graphics performance. As a result, overall application throughput is improved.

The system bus offers a high-

PRECISION-ARCHITECTURE RISC WORKSTATIONS

bandwidth connection to other graphics subsystems, many of which are integrated into the workstation package. Its ports offer access to the EISA bus as well as the SCSI-II, Ethernet, and RS-232 connections. This flexible core technology forms the backbone of the Series 700 family.

Three critical areas of graphics performance and functionality have been extended in the Series 700 family: speed, realism, and standards. The workstations deliver over 1 million 2D and 3D vectors/s. Because of the tight integration between the CPU and the graphic subsystem, the platforms pump out more than 30 frames/s. This is a necessary requirement in animation-type applications.

Flicker-free capabilities result from the systems' 72-Hz monitor, an important ergonomic requirement. Because HP is committed to graphics standards, it adopted OSF/Motif, X11 Windows, PHIGS, and GKS standards.

Four different graphics subsystems are available with each of the three workstations. The one exception is that the low-end graphics aren't available on the Model 750. The GRX subsystem offers 256 gray-scale planes. CRX supplies eight planes of color and is double-buffered. Here, the CPU can fill up an area of memory reserved for graphic images. While that image is being transferred to the display, a second image is sent to another reserved area of memory. While the second image is transferred, the first is updated, and so on. Many suppliers' implementations of double buffering offer four planes, rather than eight. HP's implementation improves graphics without compromising color.

The remaining two subsystems are the Personal VRX (PVRX) and the Turbo VRX (TVRX). PVRX offers solid-rendering 3D graphics with dynamic shading. This is a necessary feature in the MCAD and MCAE markets. The top-of-the-line TVRX is tuned toward specific graphics applications in mechanical engineering and scientific analysis. It also adds such features as antialiasing, alpha blending, and texture mapping.

Functional PC compatibility was also added to the Series 700 family. Through software emulation, the workstations can run an application that emulates an 80386-based PC with VGA capabilities running at 20 to 25 MHz. The application simulates the 80386 instruction set and the functionality that goes with the set. HP claims that all off-the-shelf DOS applications will run on the systems. The PC emulator is accessible through HP-VUE, HP's visual user environment. Users can simply open a window to run a DOS application. And it can run side-by-side with a Unix-based application.

The workstations can also be configured as servers for diskless workstations and X-terminals. A graphic subsystem wouldn't be required in this instance. Moreover, additional disk space and RAM would be included.

The systems are housed in highly integrated modular packages, making it easy to interchange subsystems. There's a separate handle attached to each subsystem so only that portion can be removed for replacement or upgrading. In addition, the systems' smart power supply is autoranging. It can be plugged in anywhere in the world, and will compute what the line voltage is and adjust to it accordingly.

PRICE AND AVAILABILTY

The 9000 Series Model 720 starts at $11,990; with PVRX graphics and a 400-Mbyte disk it goes for $34,490. The 730, which has a base configuration with a 200-Mbyte disk, costs $19,990. A fully loaded 730 sells for $103,990. The Model 750, with a 660-Mbyte disk is priced at $43,190. Configured as a server, it costs $39,690.

Hewlett-Packard Co. Inquiries, 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. **CIRCLE 512**

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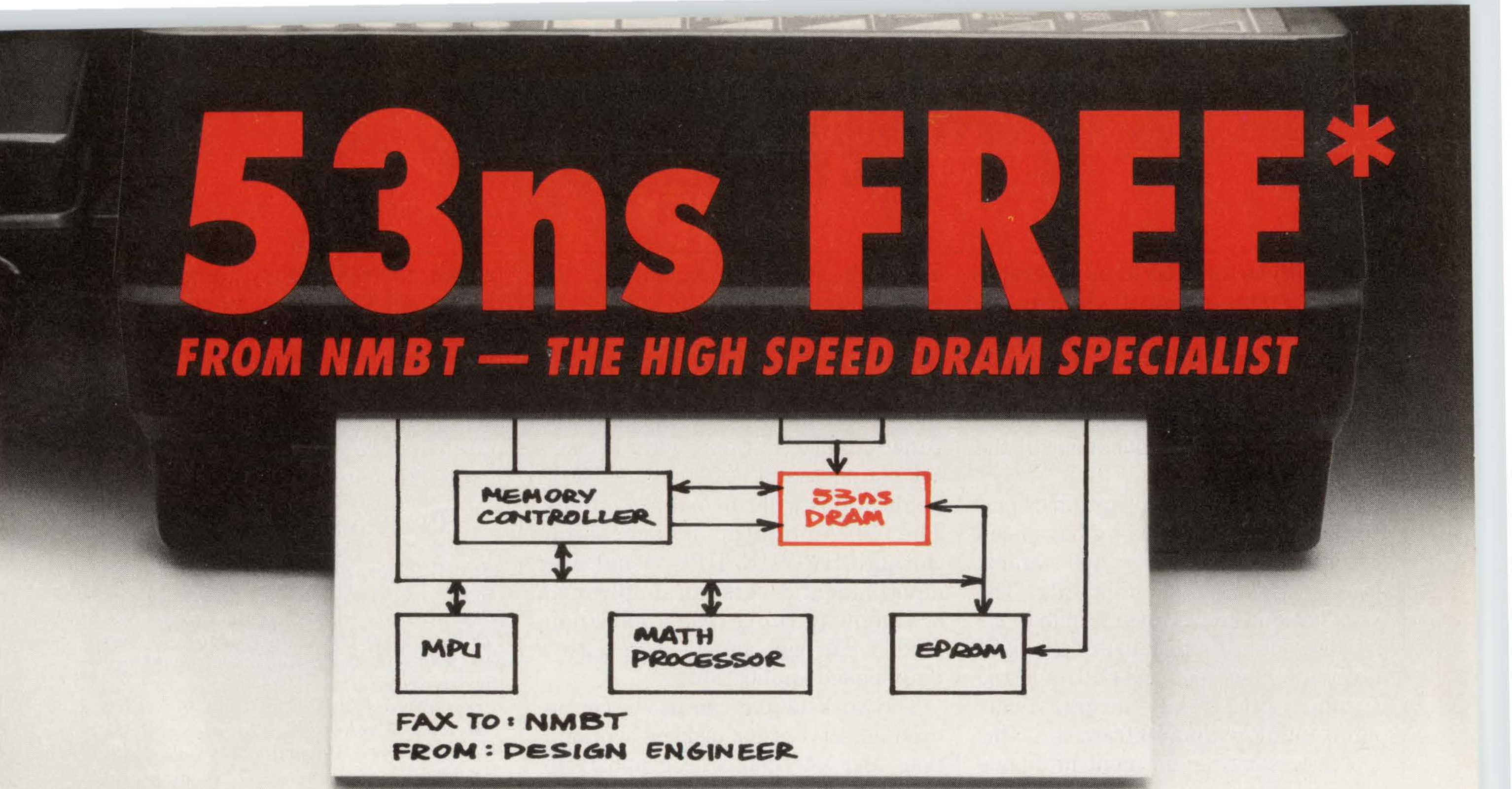

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CIRCLE 82

FRAMEWORK AIDS CONCURRENT ENGINEERING WITH CONFIGURATION MANAGEMENT

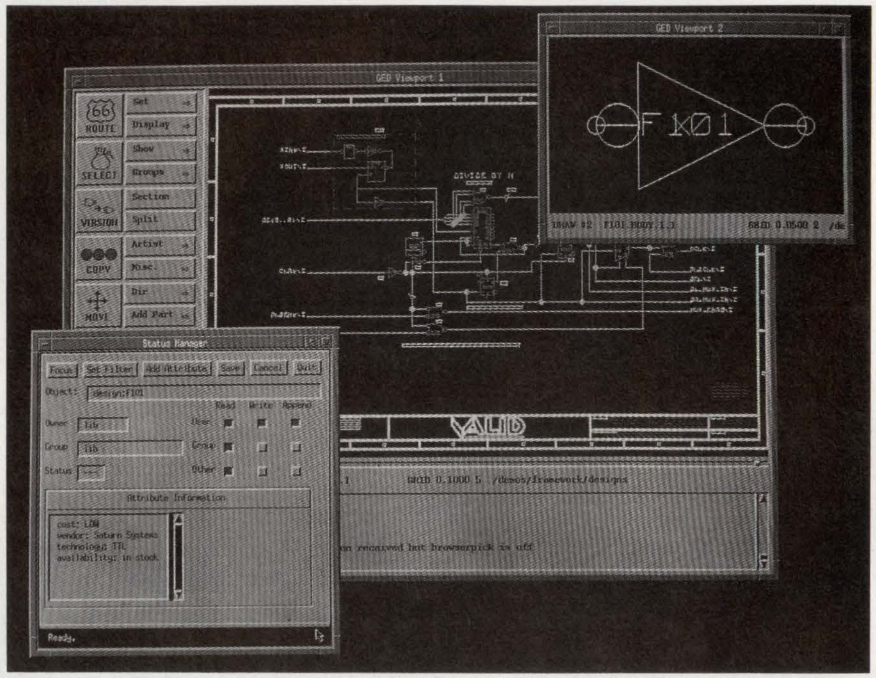
LISA MALINIAK

Design Manager, the third of four components that make up Valid Logic's ValidFrame framework, helps automate the administration of concurrent engineering in distributed-design environments. It manages data and furnishes administration capabilities for design-team members. The tool is based on the commercial object-oriented database-management system from Objectivity Inc., Mountain View, Calif.

Entire design departments, including engineers, project managers, and system and library administrators, benefit from Design Manager. In addition to handling the large amounts of data generated in electronic design, the software also brings administration to all design phases and manages the interrelationships between them. Major issues addressed by the Design Manager include: establishing organizational structure for personnel, synchronizing the activities of designers and departments, distributing the management of design data over a network, administering and controlling parts libraries, querying and reporting on data, and assembling and releasing correct data and documentation for accurate manufacturing.

Users can browse through design data and query the database. In addition, dynamic configuration management performs automatic version and release control, project tracking, work-group organization, and library maintenance. By separating application data from administrative data, Design Manager doesn't suffer severe speed tradeoffs that can result from single-database approaches.

A "workspace" concept administers the continual changes occurring in the design process. Workspaces define each user's environment in terms of the tools, libraries, and versions of data appropriate for their particular activities. Typically, each user has a private workspace and be-



longs to one or more shared workspaces. Workspaces can be created in a hierarchical fashion, possibly simplifying design partitioning. They control the flow of data between groups automatically, and coordinate the organized release of data as the design progresses.

For example, in a large engineering project that's been partitioned among three teams, a shared departmental workspace lets each team supply its stable module versions to the others to facilitate system-level simulation and analysis. When a team reaches a stable point in its work, the team leader promotes the module to the shared workspace. Meanwhile, engineers work in their own workspace without affecting the stable version.

Users access the dynamic configuration and distributed data-management capabilities through three main modules: the Browser, the System Administrator, and the Query Manager and Report Generator. All of the modules are invoked through an icon-based toolbox. The Browser functions as the users' window into design workspaces. The System Administrator furnishes menus and forms to define workspaces and establish the organization's workspace hierarchy. Finally, the Query Manager and Report Generator defines searches and makes reports.

Because the Design Manager operates transparently over heterogeneous networks, users can store and retrieve data to and from any platform in the environment. It manages data from Valid tools as well as commercial and customer-developed tools integrated into ValidFrame.

Library management, particularly controlled use of part libraries, is an important feature of the Design Manager. The library administrator can assign designers access to only certain approved libraries.

The Design Manager will be shipping by the end of the year on DEC, IBM, and Sun workstations. Standard Design Manager packages with configuration management cost $3500. Packages that include system administration and query and report capabilities go for $10,000.

Valid Logic Systems Inc., 2820 Orchard Pkwy., San Jose, CA 95134; (408) 432-9400. **CIRCLE 600**

PC SOFTWARE IS A HANDY ASSISTANT TO ENGINEERS

EEpal is a software package for engineers, designers, and technicians that merges many engineering activities into one easy-to-use program. These activities include on-line engineering formula reference, formula evaluation (including matrix evaluation), data look-up, simple and scientific calculator access, curve fitting, file editing, and the use of an appointment list with an alarm clock. Over 200 electronic engineering formulas are built into the program. In addition, users can add over 500 of their own formulas. They can also create and store vendor lists. An auto-dial feature allows the lists to be used with a modem to serve as a phone directory. The software, which costs $479, runs on most IBM PCs and compatibles as a standalone or memory-resident program. It requires 10 kbytes of RAM and a hard-disk drive.

Eagleware, 1750 Mountain Glen, Stone Mountain, GA 30087; (404) 923-9999. CIRCLE 601

DO TOP-DOWN, BOTTOM-UP PLD DESIGN

Both top-down and bottom-up design approaches are possible with the Amadeus PLD software from Cadence. Users can now create programmable-logic devices (PLDs) with schematics or hardware-description languages (HDLs). In addition, they can design with Boolean, truth-table, or state-machine descriptions in the Abel language. The tool is integrated into the Amadeus software. It's also linked with the company's design-synthesis software, which lets users explore design trade-offs early on. They can create designs in the Verilog HDL, and synthesize the designs for a PLD. Furthermore, PLDs that are described in Verilog or as schematics can be changed to ASICs without manual translations. Amadeus PLD, which will ship in May, runs on Unix workstations. Pricing begins at $12,000.

Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234. CIRCLE 602

SCHEMATIC TOOL NOW HAS XILINX 4000 LIBRARIES

Designers using the Schema III schematic-capture system now have the Xilinx 4000 series logic cell arrays (LCAs) at their disposal. The interface between Schema III and the Xilinx XACT design system includes library macros for 2000, 3000, and 4000 series LCAs. There are over 200 parts in the new series 4000 library, many being of a hierarchical design. Without leaving the drawing sheet, Schema users may browse through the Xilinx libraries and retrieve schematics of any part. LCA logic is graphically constructed using the schematic and user input. The completed schematics are then directly ported to the Xilinx design system for further checks and compilation. Schema III runs on PCs and costs $495. The XACT interface, which includes the series 4000 libraries, costs $250. Both tools are shipping now.

Omation Inc., 801 Presidential Dr., Richardson, TX 75081; (800) 553-9119. CIRCLE 603

MACINTOSH X-WINDOW OPTION EXTENDS REACH

An improved version of the X-window interface for the Macintosh computers—MacX 1.1—runs under the Macintosh operating system or A/UX, Apple's Unix implementation. It retains every function from the previous MacX 1.0 and adds three new features: 3X better performance; full support for cut and paste of text and graphics; and a version 11, release 4 code base to provide a complete, standard-conforming X-window system-server implementation for Macintosh computers. Additional features include full MultiFinder support for switching between X-client and Macintosh applications from the desktop; support for multiple monitors; and a window manager that allows X applications to appear in Macintosh-style windows on the desktop. To run MacX 1.1 and X11, the Macintosh must have 2 Mbytes of RAM, two floppy drives or a hard disk and one floppy drive, system software 6.0.4, and a network connection. X-window system 2.1 for A/UX requires 4 Mbytes of RAM, an 80-Mbyte hard disk, and A/UX 2.0 or later version. Prices start at $295 for the Macintosh operating-system version and $349 for A/UX version. Documentation and site licenses are also available.

Apple Computer Corp., 20525 Mariani Ave., Cupertino, CA 95014; (408) 996-1010. **CIRCLE 604**

SINGLE-BOARD COMPUTER RUNS REAL-TIME OS

A development tool package for Gespac's family of G-64/96-bus-based board-level products works with Wind River System's VxWorks real-time OS. This tool enables users to develop programs on powerful Unix workstations using Gespac boards. It supports high-speed downloading and debugging with the target system over an Ethernet connection. One of the first boards to be supported by the new environment is the GESSBS-6A 68000-based single-board computer. It features 2 serial ports, 256 kbytes of RAM, 2 Mbytes of EPROM, 20 parallel I/O lines, and a clock-calendar. The VxWorks tool package costs $2950 and is available now.

Gespac Inc., 50 W. Hoover Ave., Mesa, AZ 85210; (602) 962-5559. **CIRCLE 605**

OBJECT-ORIENTED TOOL CATERS TO X-WINDOWS

Xmath is an interactive, object-oriented, mathematical analysis and scripting environment designed specifically for X-Windows. It features a spreadsheet-style editor for matrices, point-and-click annotation, on-line help, and a built-in source-level debugger window for script-based programming. Xmath's object-oriented approach produces algorithms that are optimized for speed and accuracy.

Plots in many different styles can be generated automatically from data or computations, including 2D scanner plots, 3D surface plots, multiple X-Y plots, and multicurve strip charts. All plots can be annotated or altered interactively. Thr menu-driven OSF/Motif user interface makes numerical analysis easy. The tool incorporates application-specific engineering objects that improve computing speed and accuracy. Xmath is priced at $2495 for a single-user license and is available now. Discounts are available for multiple-copy purchases. Existing users of Matrix$_X$ can upgrade to Xmath for no charge.

Integrated Systems Inc., 2500 Mission College Blvd., Santa Clara, CA 95054; (408) 980-1500. **CIRCLE 606**

SOFTWARE CARRIES OUT DSP OPERATIONS

Designed for engineers and scientists using MS-DOS-based computers, Spawn is a complete signal-processing and data-analysis software environment. Its open architecture, flexibility, and built-in features quickly and easily produce complex custom applications. Spawn comes with built-in windows and graphical analysis tools for virtual-data management. It also offers object-oriented, open-architecture signal processing. The tool can be applied to simulation and analysis, as well as custom application development. The software is designed for such applications as data acquisition and display, post-collection data analysis, signal-processing simulation, algorithm testing, and application development on third-party DSP tools. Spawn is available now for $995. A demo disk is available from the company.

Jasco Systems Ltd., 9865 W. Saanich Rd., Sidney, British Columbia, Canada V8L 3S1; (604) 656-0234. **CIRCLE 607**

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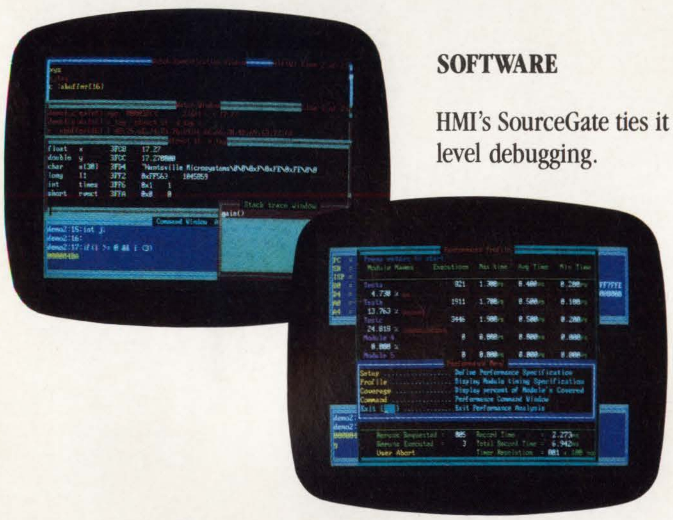

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68020	6809/6809E	8085
68030	68HC11 including F1 and D3	64180/Z180
	68HC001	Z80

HMI

CIRCLE 181

CROSS ASSEMBLER OPTIMIZES 8051 DESIGNS

Offering high-speed execution and code-size optimization, the C-8051 Version 4.0 cross compiler works with the Intel 8051 microcontroller family. The execution is coupled with the power of the full ANSI C language. The compiler allocates all global and local data statically. Function parameters and variables are put on a fixed location in memory. When the program no longer needs a certain location, memory is reused by other parameters or variables. This operation is performed by the linker and is transparent to the user.

With this variable-allocation model, C programs can be run without stack operations or consuming unnecessary RAM. Also, by using this static scheme to allocate variables, function calls are fast and require no extra overhead. Because each 8051 embedded design has its own unique requirements, C-8051 Version 4.0 offers six different memory models ranging from true single-chip designs to large bank-switched applications.

With 8051-specific extensions to the C language, such as data, idata, xdata, and code, users can put in variables and parameters wherever they're needed, regardless of which memory model is being employed. Built-in extensions for bit manipulation and direct access to 8051 registers enable efficient code generation. To maximize the 8051 processor, special keywords such as interrupt are added to make it easier to declare and write an interrupt function directly in C language without going through assembly code.

The cross-compiler is equipped with a DOS extender so that large programs can be compiled and linked, taking advantage of up to 16 Mbytes of extended RAM. The PC version of the kit, with the compiler, a macroassembler, a linker, a librarian, and manuals, costs \$1295. The C manual includes tutorial examples as well as reference information. Other versions of the software are available, including those for Sun, HP, and DEC platforms.

Archimedes Software Inc., *2159 Union St., San Francisco, CA 94123; (415) 567-4010.* **CIRCLE 608**

■ *RICHARD NASS*

POWERFUL SPREADSHEET EASES WHAT-IF ANALYSIS

When spreadsheets come to mind, financial planners are usually expected to be the users. However, the powerful features of Microsoft's Excel 3.0 suit it to a wide range of engineering what-if analyses. The program, which is a major upgrade over previous releases and incorporates over 100 new features, makes it easier to analyze data. An improved help capability also makes it easy for users of Lotus 1-2-3 to migrate to Excel 3.0.

An added button-oriented on-screen toolbar speeds the use of frequently employed functions, such as changing typefaces, auto summation of a row or column, and best-fit to change the size of a column border, among others. Outlining is another feature integrated into the spreadsheet. This feature allows large or complex worksheets to be collapsed or expanded so that users can view them at different levels of detail.

Data consolidation is also easier—users can combine and summarize worksheets in memory or on disk, regardless of the data's structure or format. Live links can also be established. Such links make it possible for data to be changed within the supporting worksheets. In addition, dynamic updating within the consolidated report is permited.

Also part of the package is Excel Solver, a program developed by Frontline Systems Inc., Palo Alto, Calif. Solver performs multivariable goal-seeking linear and nonlinear optimization with up to 200 variables (with bounds) and 100 constraint formulas. A single-variable goal-seek feature can also be invoked by dragging a pointer on a chart. In addition, Pioneer Software's Q+E program is included to allow the package to integrate data from other database programs. Object linking permits Excel 3.0 to embed objects, such as charts or worksheets, into other documents, or bring in objects from other documents.

Versions of Excel 3.0, which are available for Microsoft Windows or OS/2 or for the Apple Macintosh, sell for \$495. Purchasers of previous versions get a discount if they upgrade. Delivery of the Windows version is from stock.

Microsoft Corp. *One Microsoft Way, Redmond, WA 98052-6399; Pete Higgins, (206) 882-8080* **CIRCLE 609**

■ *DAVE BURSKY*

MEMORY ARRAY DRIVERS REDUCE ACCESS TIMES

By reducing the delays getting into and out of an array of memory chips, a GaAs-based memory driver trims the propagation delay to about 3.5 ns typical. That cuts the typical propagation delay by close to 2/3 over conventional bipolar or MOS drivers. The GigaBit Logic 10G014 memory driver handles arrays of dynamic or static RAMs. Its 90-mA output lets it handle large, distributed capacitive loads. It can also be used as a registered, ECL-to-TTL translator or bus-interface circuit.

The chip has eight latched address inputs. For each pair of inputs, there's a 2:1 multiplexer that converts the direct address signals into TTL-compatible row and column addresses for DRAMs. To minimize noise and the need to three-state the outputs, the four outputs of the 10G014 are differential and have open-drain structures. In addition, clocked control logic provides pipelining control with no additional logic. The chip is also designed for expansion—all of the necessary signals are present to permit multiple banks of memory chips to be addressed.

It runs from a +5 and –5.2 or –4.5 V, making it compatible with 10K and 100K ECL logic. It dissipates about 500 mW, and can thus be housed in either a 44-lead plastic leaded chip carrier or a 40-pin leaded or leadless ceramic chip carrier. It can also be delivered as an unpacked die. In lots of 10,000, the plastic-housed version goes for $13.90. Samples are from stock.

***GigaBit Logic Inc.**, 1908 Oak Terrace Lane, Newbury Park, CA 91320; Daniel Rodriguez, (805) 499-0610* **CIRCLE 608**

■ *DAVE BURSKY*

GATE ARRAY MERGES TEST LOGIC ON CHIP

FasTest arrays in the LFT150K series is the first gate-array family to use the CrossCheck Technology built-in test logic. Based on LSI Logic's LCA100K 1-μm compacted arrays, they offer 86,000 to 190,000 raw gates. With two levels of metal, they deliver 37,000 to about 80,000 usable gates and have 270 to 410 signal pins. The chips enable the designer to concentrate on functionality while transparently providing nearly total-fault coverage for high-quality testing. Embedded test structures defined by CrossCheck supply observation points at every node in the customer's design. Just four dedicated pins are required to use the embedded test logic, which can easily provide 98% fault coverage. The LFT150K arrays cost about 20 to 25% more than the LCA100K arrays, and employ a subset of the LCA100K cell library that has been recharacterized with the embedded test logic. Prototypes will be shipped in the late second quarter.

LSI Logic Corp., 1551 McCarthy Blvd., Milpitas, CA 95035; Dave Baillie, (408) 433-8000. **CIRCLE 609**

CHIP SET COMPRESSES, TRANSFERS VIDEO DATA

Transferring video data to computers often requires very-high-speed parallel or serial channels, due to the large quantity of data involved. However, with the release of a two-chip set from Brooktree, real-time video-data transfers over networks is now economical and practical. The Bt291 is the RGB-to-YCrCb compressor, while the Bt294 decompresses the YCrCb data back to RGB data. The video-net converters conform to CCIR 601 and SMPTE RP-125 standards.

The chips permit video sources and displays, such as cameras, tape decks, and monitors, to be connected to computers through real-time digital interfaces. The Bt291 combines 8-bits each of red, green, and blue information to form 8-bit Y and 8-bit CrCb components. The Y data is then optionally low-pass filtered and multiplexed with the CrCb information after the CrCb data is decimated to 1/2 the Y data rate. Video timing is then inserted and the entire multiplexed signal is delivered over an 8-bit bus. The chip also has a 16-bit YCrCb bus through which the signal can be mixed with digital audio or teletext, and three 256-word-by-8-bit color lookup-table-palette RAMs that aid gamma correction. An internal command register permits forced-blanking levels of Y and CrCb data and automatic line-count transmission.

The companion Bt294 converts the 8 bits of multiplexed video data back into the 24 bits of RGB color components and extracts timing to reconstruct the horizontal and vertical blanking and the field outputs. Both CMOS chips operate from 5 V and come in 100-lead PLCCs. Samples are available and sell for $133 in 100-unit lots.

***Brooktree Corp.** 9950 Barnes Canyon Rd., San Diego, CA 92121; Tom Kovanic, (619) 452-7580* **CIRCLE 610**

■ *DAVE BURSKY*

MASK OPTION FOR MACH TRIMS COST, UPS SPEED

AMD has just released a metal-mask option to its Mach family of PLDs, trimming manufacturing cost to as little as 0.3 cents/gate. The fixed metal mask improves internal propagation delays, ensuring that the hardwired chips deliver the same or better performance than the EEPROM-based field-programmable versions. The MASC option aims at users that consume at least 25,000 units of a specific pattern, which drops the cost to about 0.8 cents/gate vs. about 1 cent/gate for the programmable version. As volume increases to 250,000 or more units, the price drops to the 0.3-cents/gate level. Shipments of the mask-programmed units will start in May.

Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, CA 94088-3453; (408) 749-5703. **CIRCLE 611**

CHIP SET FOR MCA BUS SIMPLIFIES SYSTEMS

A chip set now squeezes all of the basic peripheral control and support functions into four different ICs by turning the design of an 80486-based Micro-Channel-bus-system motherboard into a simple task of connecting a half-dozen chips together. The TC85M9X1 four-chip set consists of a 184-lead bus-master DMA controller (TCM85M911); a 160-lead combination data and address buffer (85M921); a 160-lead memory and bus controller (85M931); and a 144-lead peripheral support chip with timers, parallel port, interrupt controller and other control functions (85M951).

All four chips plus an additional data and address buffer chip are used for a typical motherboard along with the CPU, secondary cache, BIOS ROMs, and the desired peripheral functions. To improve system performance and allow simple CPU upgrades, the chip set employs a proprietary internal architecture called the short-line interface kernel. SLIK defines a synchronous bus between the processor and memory subsystem, and an asynchronous bridge between the CPU block and the MCA bus and I/O subsystem.

The chips—developed by Micral, Minneapolis, Minn., an independent affiliate of Groupe Bull—are an offshoot of a chip set developed to implement a MIPS RISC-based motherboard.

Versions of the chip set are available for operation at either 25 or 33 MHz. In lots of 1000, the 25-MHz five-chip combination sells for $250. Delivery of engineering samples is from stock.

Toshiba America Electronic Components Inc., 9775 Toledo Way, Irvine, CA 92718; (714) 455-2000.

CIRCLE 612

■ *DAVE BURSKY*

PLD ENHANCEMENTS UP DRIVE, TRIM POWER

A trio of programmable-logic enhancements broadens the designer's choice of the ideal PLD. The first is a version of AMD's 16V8 with high-current (64-mA) output drivers, is ideal for buses. Next are zero-power versions of AMD's EEPROM-based 22V10 and 16V8. Both ZPALs consume 15 μA maximum during standby and come in 25- and 20-ns versions, respectively. The PALCE22V10Z-25 comes in 28-lead PLCCs and 24-pin skinny DIPs, while the 16V8Z-20 comes in 20-pin DIPs and PLCCs. Lastly, there's the Mach 210 with about 1800 gates, 64 programmable macrocells, and 44 pins. Military versions of the 210 will be ready in the third quarter. In 1000-unit lots, prices are $3.95 for the 24-pin DIP or 28-lead PLCC version of the 16V8HD-10; $5.90 and $2.75 for the PALCE22V10Z-25 and 16V8Z, respectively; and $36.90 for the 15-ns Mach210. A 20 ns version of the Mach210 sells for $24.60.

Advanced Micro Devices Inc., 901 Thompson Place, Sunnyvale, CA 94088-3453; (408) 749-5703. CIRCLE 613

WAFER-STEPPER FAMILY HITS 0.35-μM RESOLUTION

High resolution and precision overlay across the field of 30-mm-diameter I-line and deep-UV lenses makes the PAS 5500 family of wafer steppers suited for high-volume production of ultra-large-scale ICs. For the model PAS 5500/20 I-line stepper, production resolution is better than 0.7 μm. Moreover, the system can be upgraded with higher numerical-aperture lenses for sub-0.5-μm resolution. The PAS 5500/90 is the 0.35-μm, deep-UV family member. It uses a 248-nm excimer laser source to achieve its high resolution. The family's four systems are all built around an inherently stable, triangular lens base plate.

ASM Lithography Inc., 2315 W. Fairmont Dr., Tempe, AZ 85282; (602) 438-0559 **CIRCLE 614**

FUTUREBUS+ HARDWARE IS FULLY METRIC

The industry continues to move toward Futurebus+ as a mechanical packaging standard with the release of BICC-VERO's line of hard-metric Futurebus+ hardware. "Hard-metric" means that the products are designed to purely metric measurements as opposed to metric conversions of English measurements. The products include a card frame that conforms to IEE P1301.1 and a hard-metric backplane that conforms electrically to IEEE P896.2 and mechanically to IEEE P1301.1. Call for pricing and availability.

BICC-VERO Electronics, 1000 Sherman Ave., Hamden, CT 06514; (203) 288-8001. **CIRCLE 615**

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Shin-Etsu Polymer America, 34135 7th St., Union City, CA 94587; (415) 475-9000. **CIRCLE 616**

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Alpha Wire Corp., P.O. Box 711, Elizabeth, NJ 07207-0711; (908) 925-8000. **CIRCLE 617**

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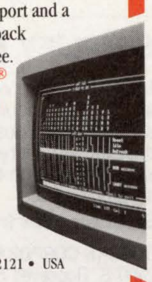

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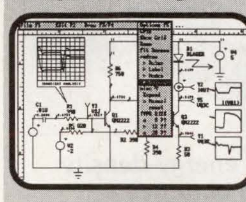

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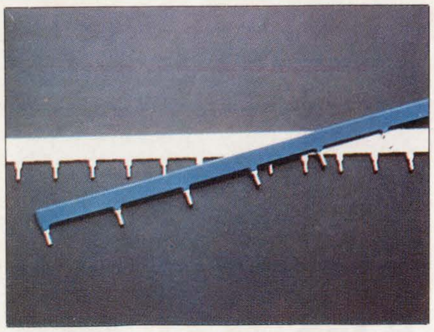

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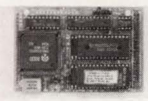

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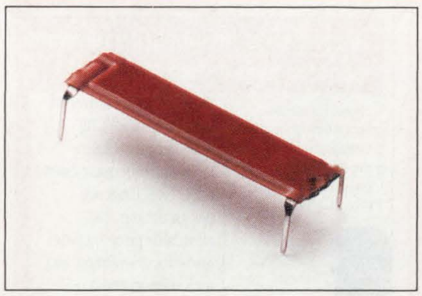

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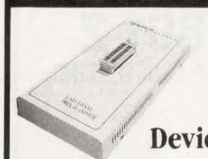

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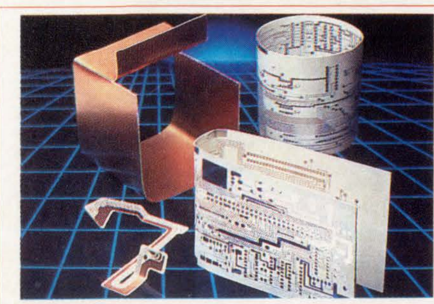

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TRACK I	**TRACK II**
Tuesday, 23rd -TUTORIALS-	
** Introduction to X-Motif ** Richard Lasslo, Hewlett Packard	** Introduction to FDDI ** Mark Wolter, National Semiconductor
Wednesday, 24th -OPENING KEYNOTE and TECHNICAL SESSIONS- **"Current and Future Trends in Network Management" - Keith McCloghrie, Hughes Lan Systems**	
NETWORK MANAGEMENT Open management architecture; Methodology for configuring large Networks; Security management for TCP/IP	PHYSICAL LAYER I & II Understanding twisted pair Ethernet; Non-buffered Ethernet controllers; Applying triple port DRAMs for increased performance; Advanced controllers
INTERNETWORKING Point to multipoint; Effects of high speed bridges on performance; IP routing over public switched networks; parallel networking	NETWORK TEST EQUIPMENT Trends & issues; Monitoring & managing; Conduit troubleshooting
X-WINDOWS I & II Font management; RISC controllers; GfW-Windows for PC platforms; advanced X-Terminal design; X-remote & terminal server solutions; Printing in X-Windows	HIGH SPEED NETWORKING - FDDI Traffic controller design; Network testing; Interoperability testing; FDDI tuning, Networking for real time applications
Thursday, 25th -OPENING KEYNOTE and TECHNICAL SESSIONS- **"The Invisible Network War" - Bruce Nelson, Auspex Systems**	
HIGH SPEED NETWORKING Protocol analysis for high speed; Impact of telecommunications & high speed systems; Traffic statistics for more effective window based mux; Frame Relay – overview of networking technology, concepts & implications; ISDN; Gigabit/s system issues	DISTRIBUTED SYSTEMS I & II Transactional remote procedure calls; client-agent-server model for distributed processing; Peer-peer computing; Protocol for interactive remote programming; Processing using local operating network;
	DISTRIBUTED SYSTEMS Panel Discussion
INTERNETWORKING II Ethernet-FDDI router design; Multicomputer interconnection; Routing protocol metrics; OSPF routing protocol	PHYSICAL LAYER III Parallel architecture; Bus mastering; FDDI concentrator design; Non-cable connectivity
NETWORK MANAGEMENT II Development & integration of MIB; SNMP experimental bridged MIB development; SNMP heterogeneous networking considerations; Object oriented agent architecture; Applying expert systems to planning & management	PROTOCOLS & NETWORK APPLICATIONS Fast, open systems interconnection protocol; E-mail integration; Hybrid image server; FAX outsourcing; Server allocation issues; DIR services & street talk

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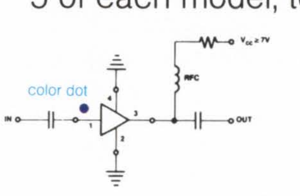

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8-CHAN MUX	YES	NO	NO
SINGLE +5V SUPPLY	YES	NO	NO
4-WIRE INTERFACE	YES	NO	NO
LOW POWER*	25mW/ 50μW	725mW	215mW
CONVERSION TIME	13μsec	35μsec	12.5μsec
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