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SPECIAL REPORT: PLDS AND FPGAS

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ELECTRONIC DESIGN

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MARCH 14, 1991

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CIRCLE 151 FOR LITERATURE

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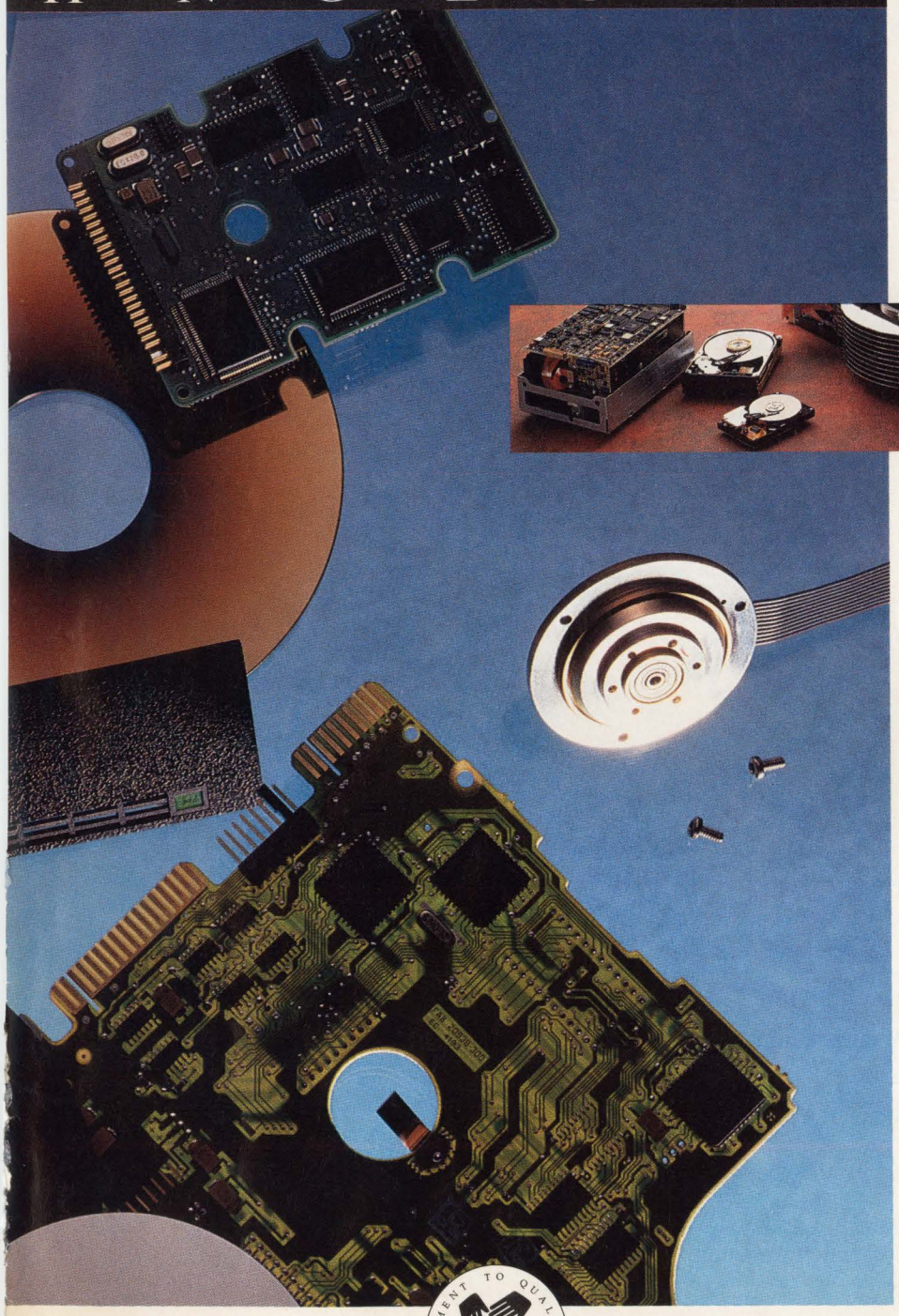
CIRCLE 84

Extraordinary disc drives require extraordinary parts.

H N O L O G Y



Today's disc drives are smaller in size and larger in capacity than ever before due to advances in component technology. By designing and manufacturing most of the components ourselves—a concept called vertical integration—we can control the technology, cost, availability and quality of these critical parts.

Technically speaking, no one builds more advanced thin-film discs and recording heads than Seagate. These core technologies help us put 3 gigabytes of storage in a box the size of a toaster. And because we design our own components, we can bring our new products to market faster.

Of course, a key consideration in building our own parts is the cost. By controlling the manufacturing process down to the component level, we can have a significant impact on the cost of our finished products. The end-result is a better value for the customer without sacrificing quality or performance.

In terms of availability, it's important to know that Seagate shipped over 7 million disc drives last year alone. With volumes like these, building our own components helps us avoid the parts shortages that often plague other disc drive manufacturers.

Most importantly, vertical integration allows us to maximize the quality of every component we produce. With the industry's most advanced equipment and testing techniques, we consistently turn out components and finished products that are beyond reproach.

Obviously, it takes an extraordinary capital investment to pursue this strategy. But the disc drive companies who control their critical component production will be better able to control their own destinies, as well as those of their customers.

For more information on our complete line of high-performance disc storage products, contact your authorized Seagate distributor. Or call Seagate at 800-468-DISC, or 408-438-6550.

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CIRCLE 146

MARCH 14, 1991 VOL. 39, NO. 5

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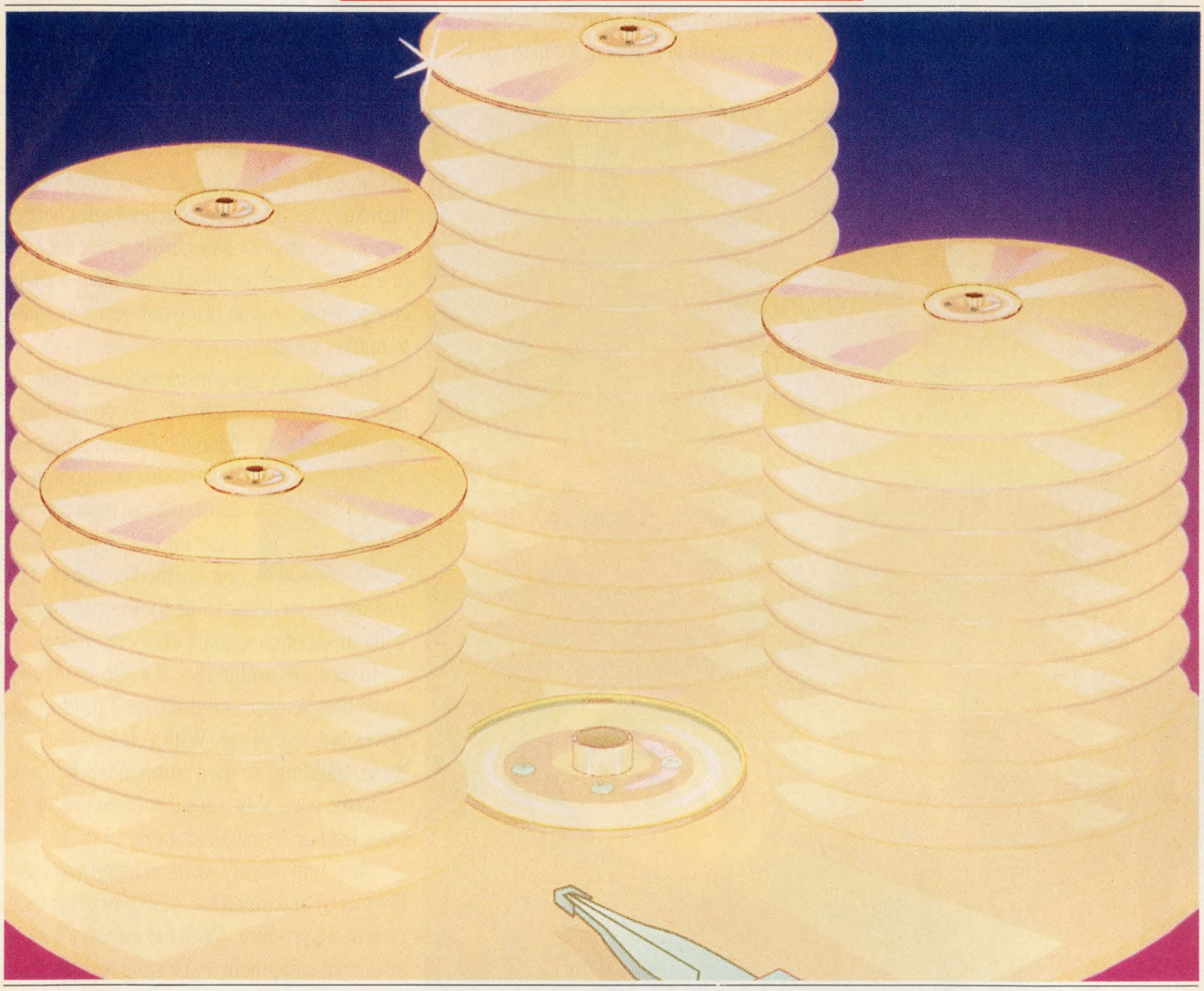

COMING NEXT ISSUE
- Special Report: Fax modem chips
- Design Team Issues: Architectural models are key to system-level design
- First details on new workstation graphics ICs
- PIPS: Power, Packaging, Interconnections, Switches & Relays
- Suppress EMI/RFI from the ground up
- How to recognize a good conductor crimp
- Manufacturer listing for interconnections
- Special products section
- PLUS:

Ideas for Design
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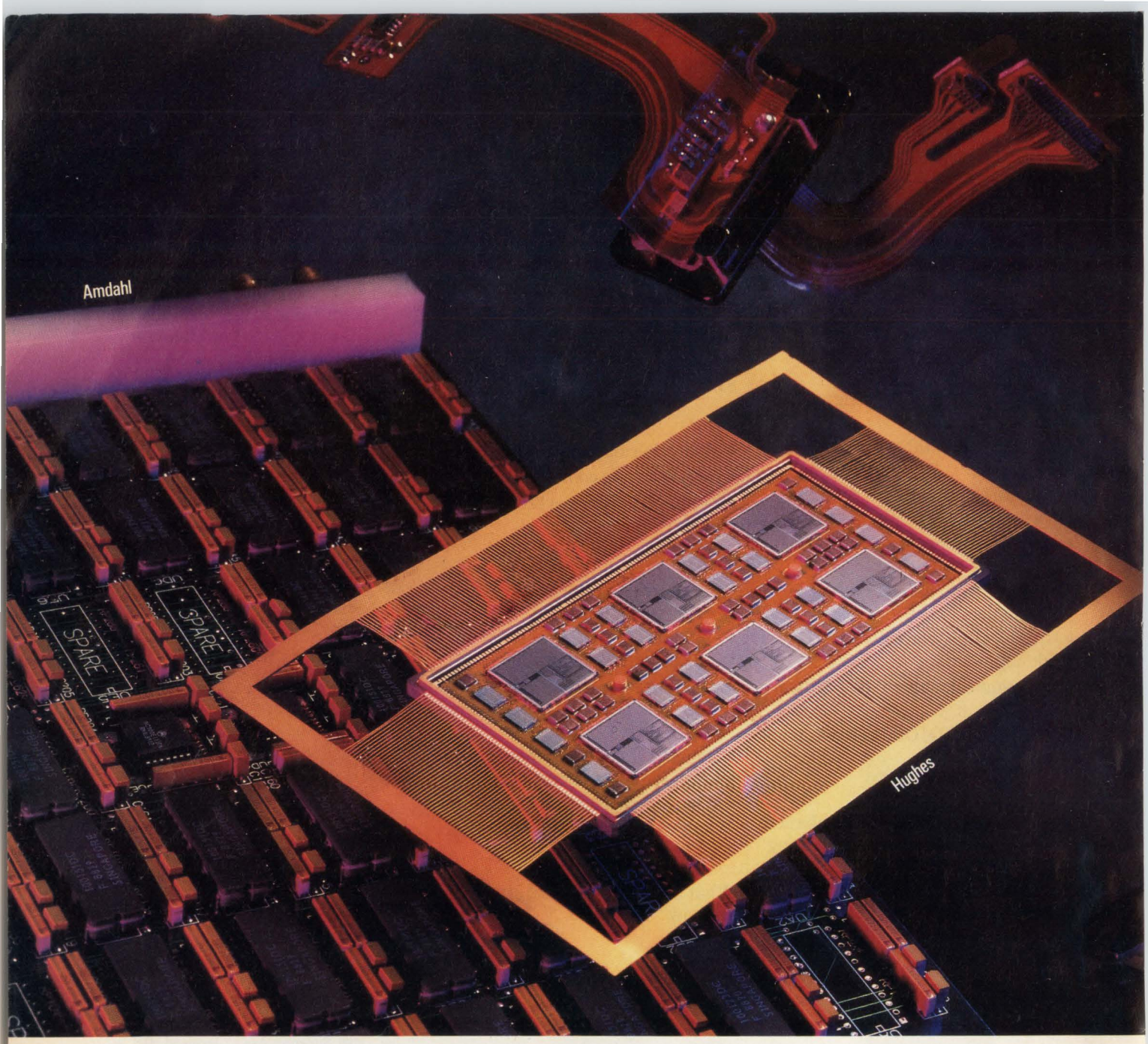

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In each case, Mentor Graphics design tools helped leverage these complex board technologies into successful products:

A ten-layer ECL board from Amdahl with 1257 components and 1659 nets, each with a length or impedance constraint.

A board from Tektronix combining very high-speed digital and low-noise analog circuitry.

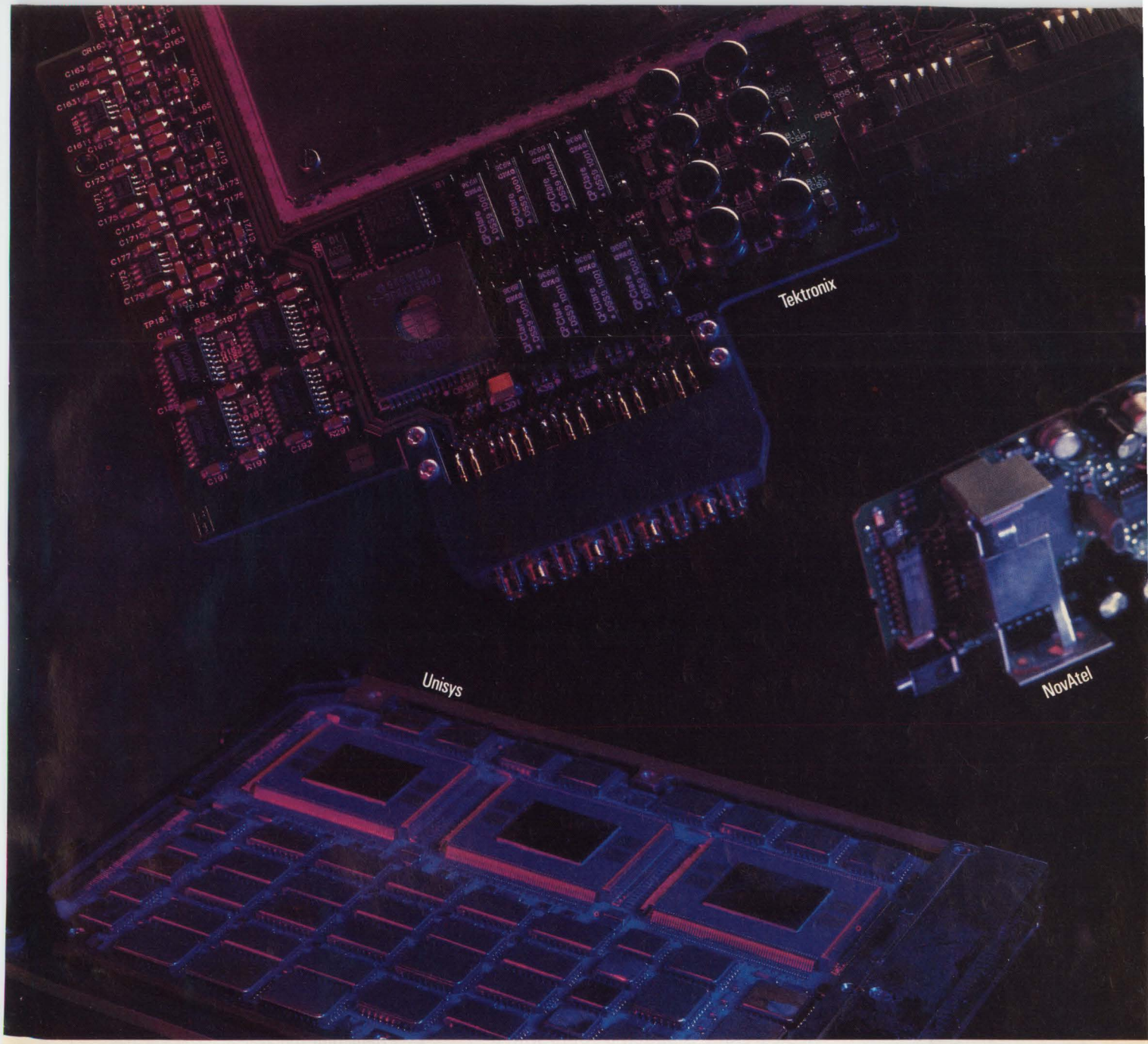
A PCB from NovAtel using chip-on-board (COB) technology for dramatic space savings.

A flexible circuit board from a major hard disk manufacturer with complex curved geometries.

A multi-chip module (MCM) from Hughes with 82 devices and 3300 interconnects on a 96x45 mm (3.8″ x1.8″) silicon substrate.

A Mil-Std multi-layer ceramic module from Unisys that packs 57 chips and 2834 pins into a 6″x6″ space less than .6″ thick.

Each of these designs required superior engineering combined with superb tool technology. Precisely the kind of partnership



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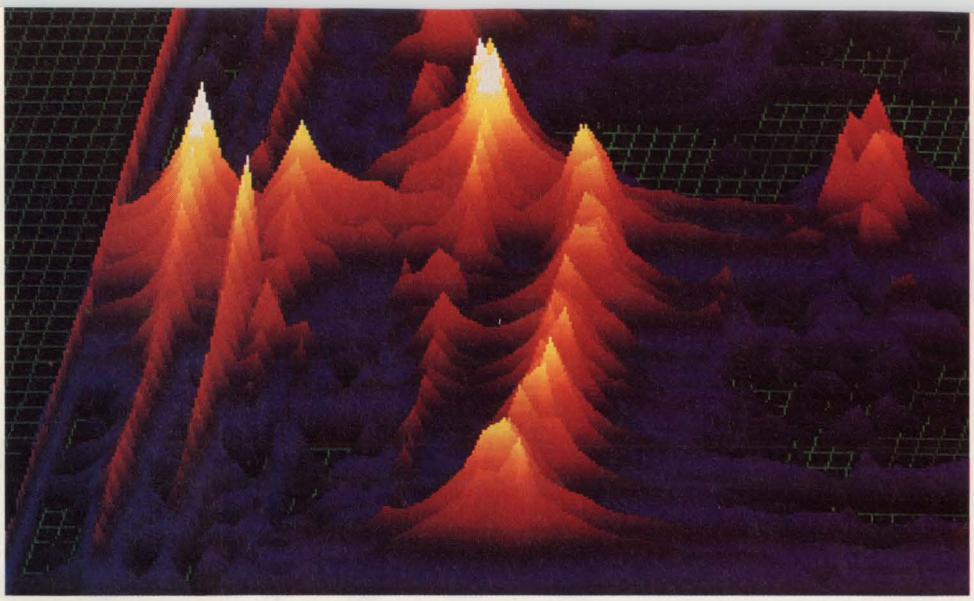

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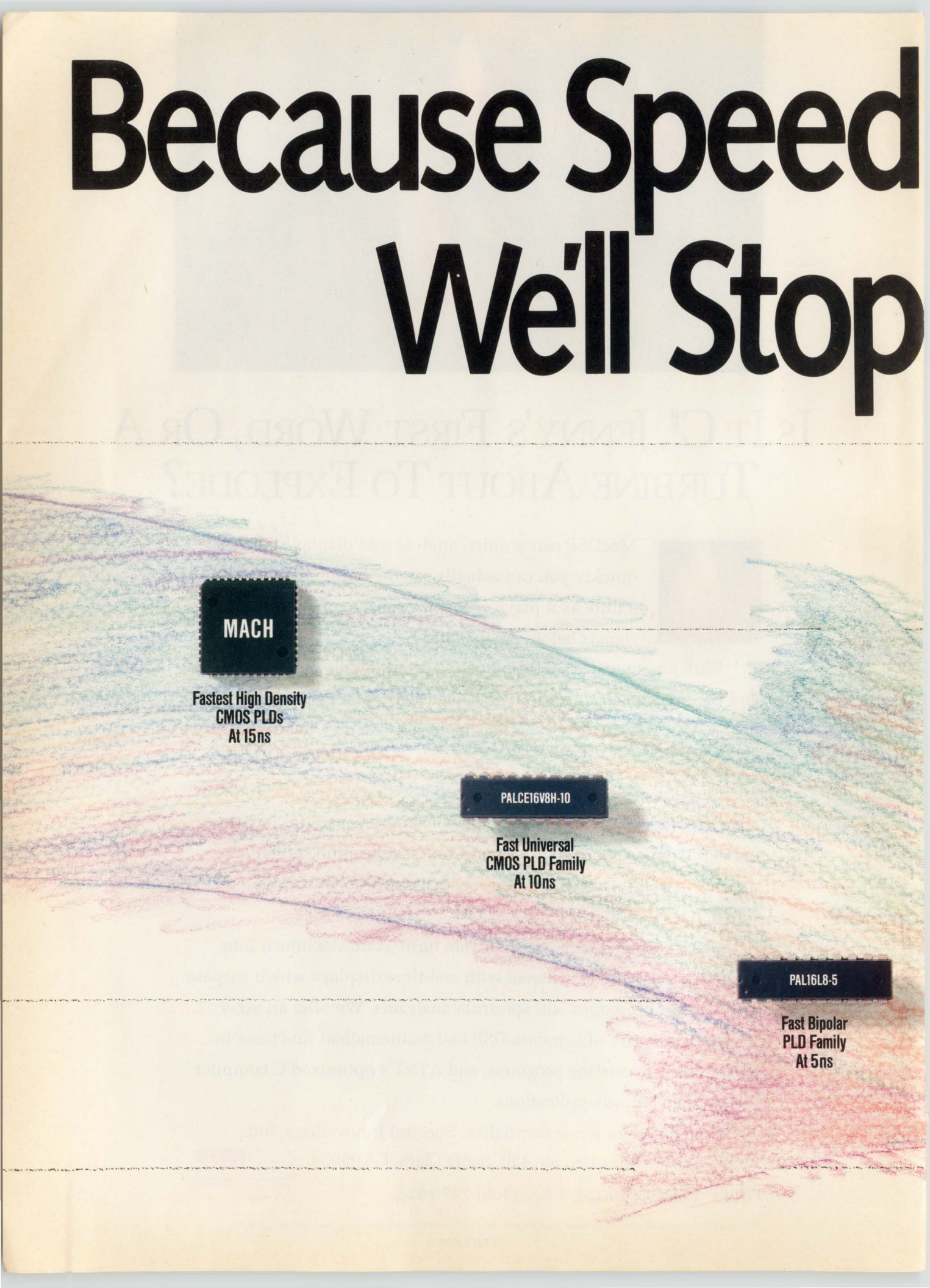
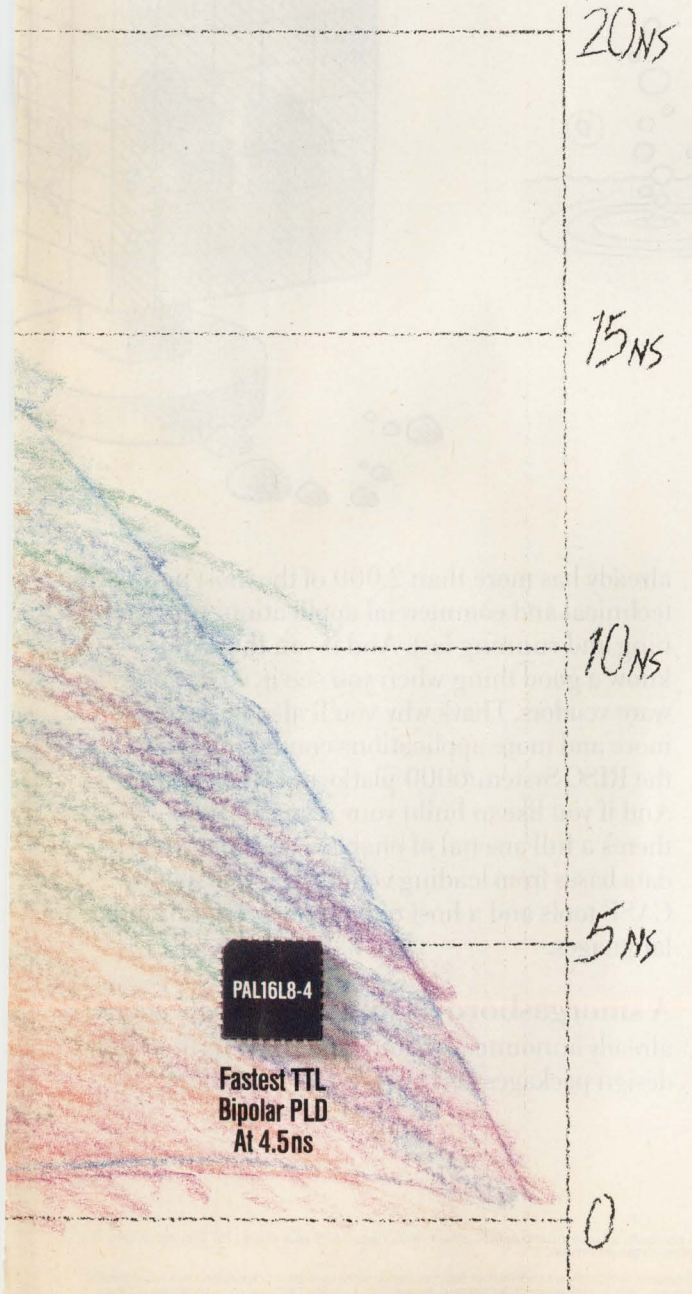
Contact us for a free demo disk. Spectral Innovations, Inc., 4633 Old Ironsides Dr., Ste.450, Santa Clara, CA 95054. Phone: (408) 727-1314. FAX: (408) 727-1423.

CIRCLE 99

Because Speed We'll Stop



Is Everything. At Nothing.



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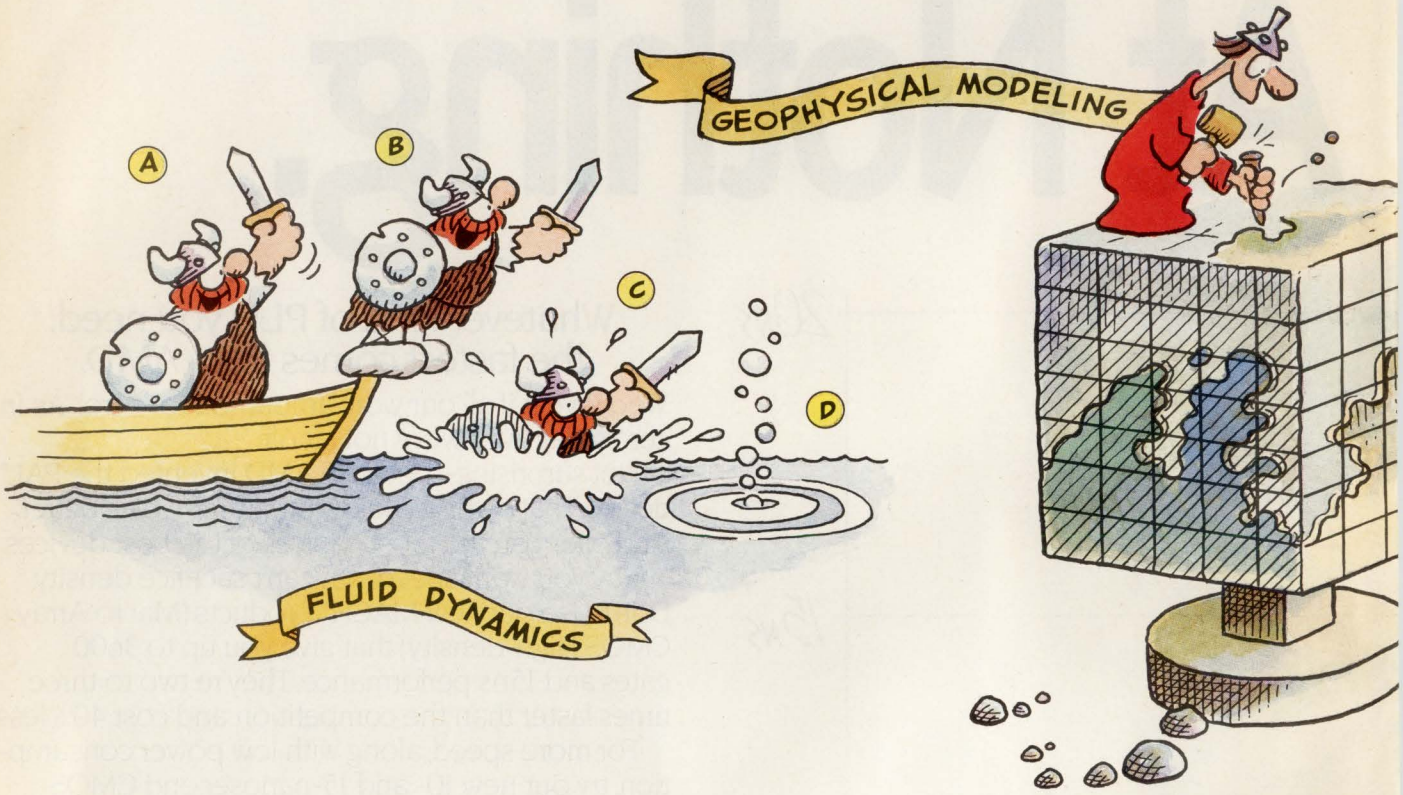
Advanced Micro Devices

CIRCLE 135

The IBM RISC System/ The power you've been seeking



It's a never-ending quest for power seekers. You're always looking for ways to run your favorite applications faster. Well, search no more. The RISC System/6000™ family of POWERstations and POWERservers gives you power that soars as high as 23 MFLOPS and 56 MIPS.

	MFLOPS	MIPS	SPECmark™
POWERstation 320	7.4	29.5	22.4
DECstation 5000-200	3.7	24.2	18.5

When it comes to porting, your ship has come in. Of course, all the speed in the world wouldn't mean much without the applications you need. So the RISC System/6000 family already has more than 2,000 of the most popular technical and commercial applications up, running and running fast. And if you think you know a good thing when you see it, so do software vendors. That's why you'll also be seeing more and more applications coming on board the RISC System/6000 platform all the time. And if you like to build your own solutions, there's a full arsenal of enablers and relational data bases from leading vendors, as well as CASE tools and a host of popular programming languages.

A smorgasbord of solutions. Applications already announced include the IBM engineering design packages CADAM,™ CAEDS,™ CBDS,™

MFLOPS are the results of the double-precision, all FORTRAN Linpack test 100x100 array suite. The Dhrystone Version 1.1 test results are used to compute RISC System/6000 Integer MIPS value where 1,757 Dhrystones/second is 1 MIPS (Vax 11/780). SPECmark is a geometric mean of ten benchmark tests. All performance data are based on published benchmark information.

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CIRCLE 94

THE ELECTRONIC ROLE IN WAR

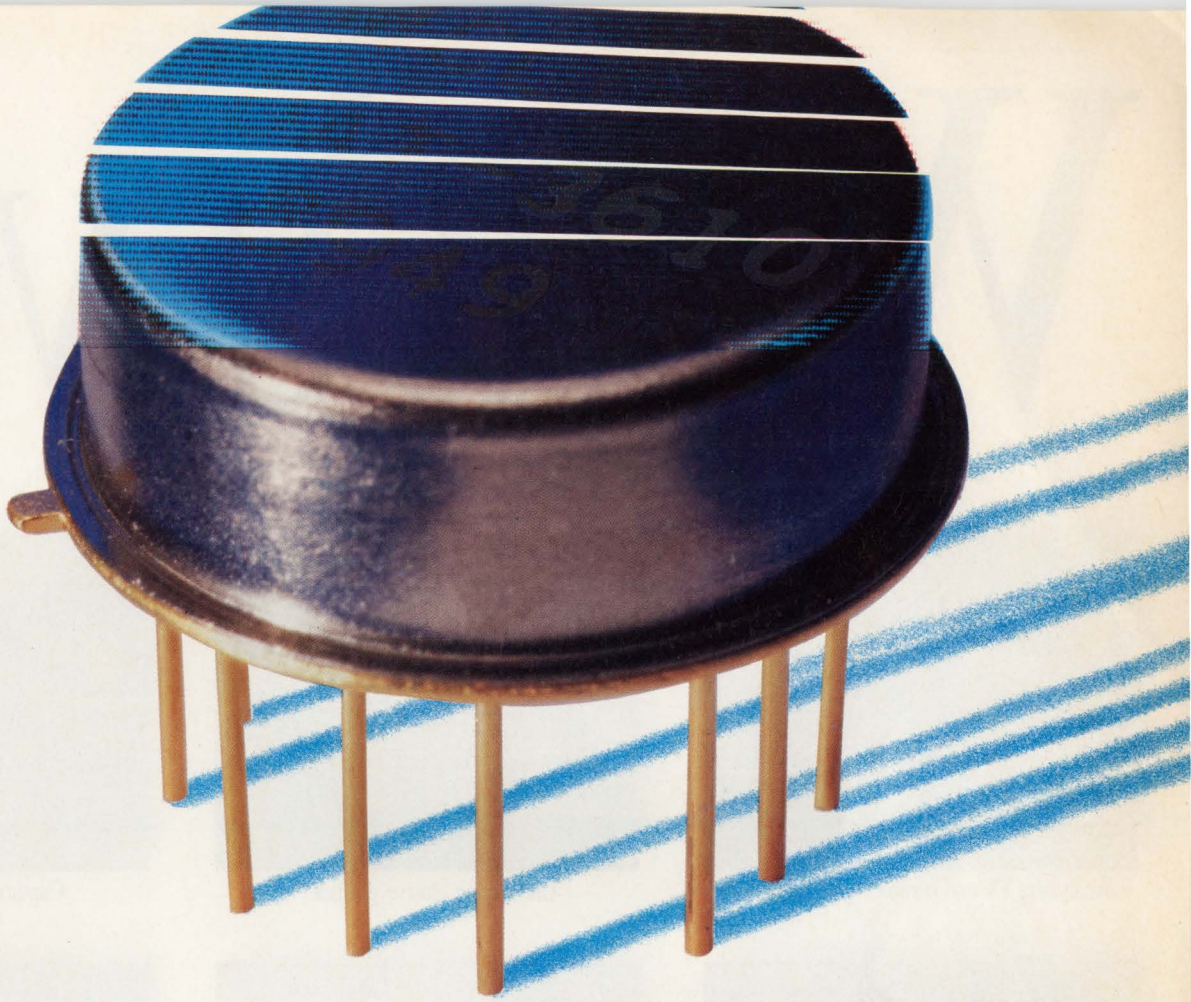
Up to now, we've hesitated to mention the Persian Gulf War in this column because of a time lag between the time this column must be written to meet our deadline and the time it appears on readers' desks. In this intervening period, rapidly changing events may render our comments, when they appear in print, inappropriate, or worse, insensitive to a negative turn of events in the war. However, while writing this column, the situation seems close to being resolved, with little doubt about the outcome. In the hope that peace will soon arrive, and within the bounds of the caveat cited above, we offer a comment on the technological aspects of the episode.

The prime-time TV showcase for the U.S. arsenal of sophisticated, electronically controlled weapons will be etched in our memories. For those who have built careers on designing electronic equipment to solve a customer's problem, there should be little surprise about their performance. After all, these devices, properly designed, simply follow the laws of physics, just as much as a bomb falling from a plane follows the basic physical law of gravity. But even knowing this, we still marvel at just how well those systems work, combining optics, radar, computer, and propulsion technologies.

Having proven the performance of this breed of intelligent weapons, what's next for the defense electronics industry? These weapons, with their demonstrated effectiveness, could undoubtedly be improved by incorporating the latest technology. We certainly hope that this is the last time they're used, but that should not stop us from improving the accuracy and reliability of the next generation, just in case we need them again.

While we're at it, let's also hope that the Department of Defense and defense-industry management will institute corresponding improvements in program administration to cut waste and inefficiency. This may not be easy to do, but it's as important as the swiftness and accuracy of the weapons themselves.

Stephen E. Scrupski
Editor-in-Chief



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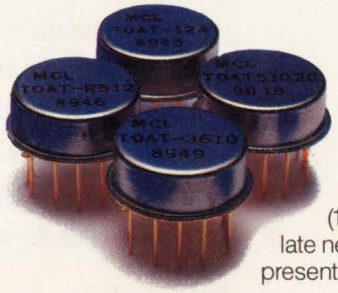
0.5	**0.12**	**1.0**	**0.2**	**3.0**	**0.3**	**5.0**	**0.3**
1.0	**0.2**	**2.0**	**0.2**	**6.0**	**0.3**	**10.0**	**0.3**
1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

bold faced values are individual elements in the units



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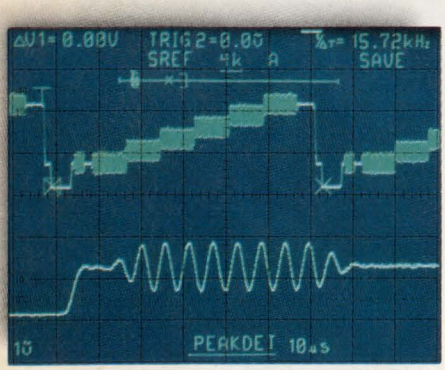
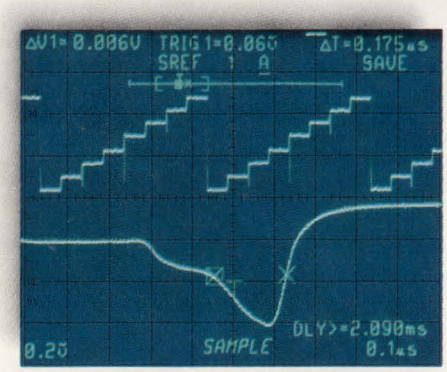
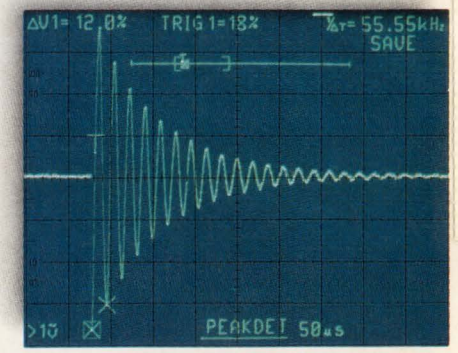


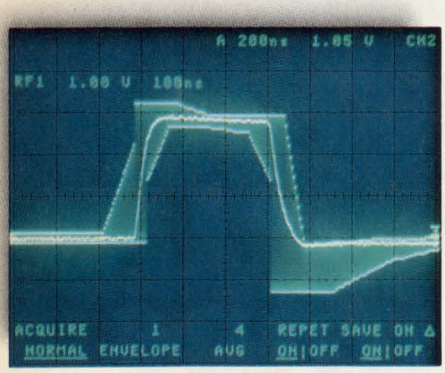
Analyzing TV and complex video signals?



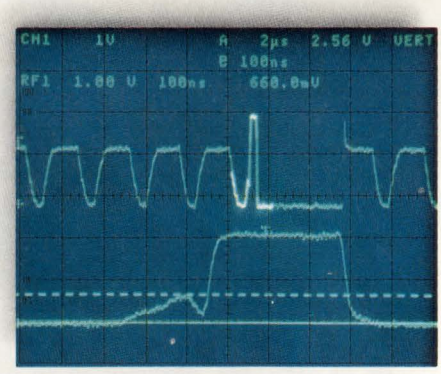
Uncovering elusive glitches?



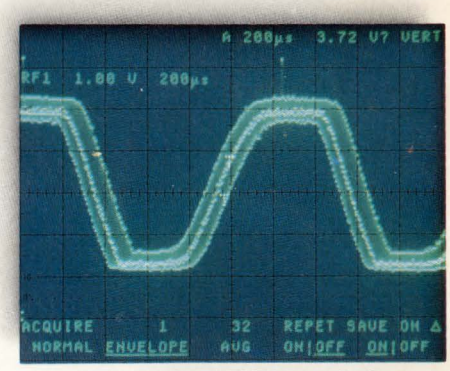
Capturing single-shot events?



Testing telecommunications signals?



Finding aberrations buried within a signal?



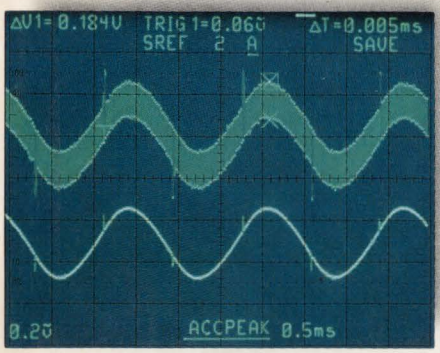
Automatic PASS/FAIL testing?

You can't depend on banner specs alone to solve problems like these. Whether you're trying to measure waveform parameters or analyze long data streams, identify infrequent events or track down glitches as narrow as 2 ns — there's all the difference between the depth of Tek troubleshooting and the trade-offs in other DSOs that compromise your results.

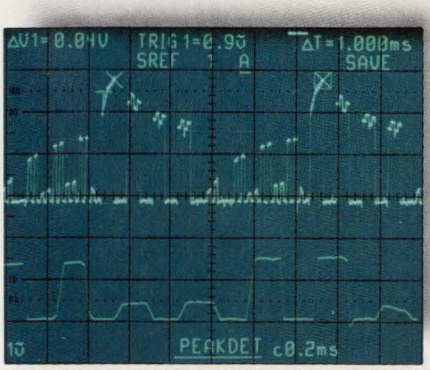
Spec for spec, feature for feature, no other company offers the credentials Tek does to effectively match DSO performance to your application needs. Whatever your criteria, you'll find a perfect solution in our line of problem-solving portable DSOs, from 10 to 500 MS/s.

Select the features to support your application. Tek DSOs offer a diverse set of capabilities including peak detect to uncover elusive glitches. Fast update rate for live signal display. Combined analog/digital operation for real-time verification of your

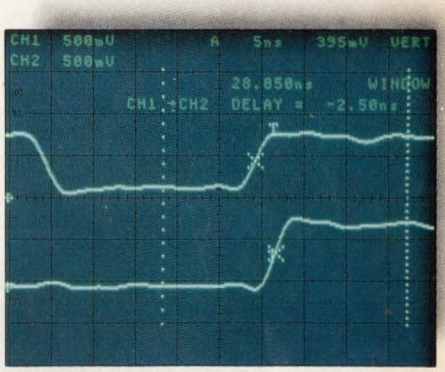
r problem?



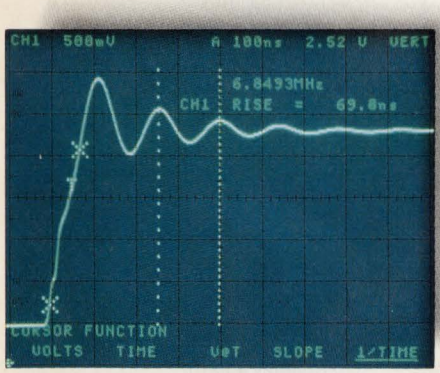
Characterizing signal noise?



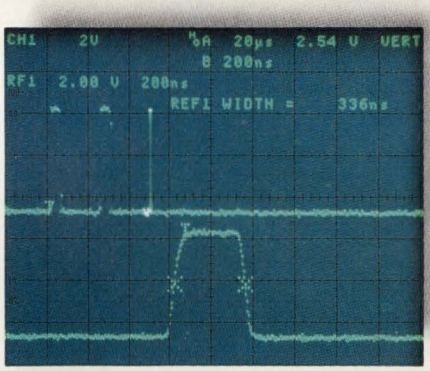
Capturing and analyzing long data streams?



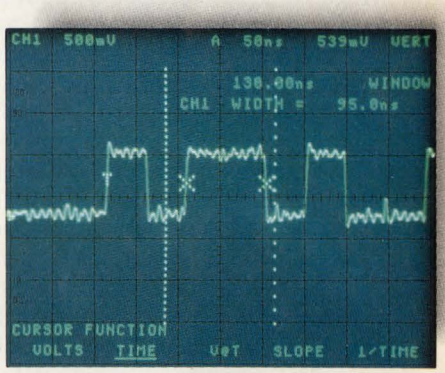
Measuring timing relationship between signals?



Performing complex measurements automatically?



Expanding glitches for close analysis?



Windowing in on signal details?

signal. Or Save on Delta to automatically verify that all parts of your signal fall within prescribed limits. Best of all, Tek's line of 100 MS/s digitizing scopes start at just $3995.

To find out which Tek scope is right for you, contact your Tek representative, return the card or call Tek direct. We can answer your questions and show you a scope that doesn't just look good on paper. It makes your toughest troubleshooting challenges routine.

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CIRCLE 113

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COMPONENTS & PACKAGING

Building power-factor correction into switching power supplies has become a fact of life for a number of reasons. For one, it alleviates the problems caused in electrical-distribution networks when the supplies' filter capacitors draw current in short pulses. It also keeps current out of the neutral line in balanced-load systems.

But for those who keep an eye on such things, as all power-supply manufacturers must (and as users should), power-factor correction can also keep products from running afoul of some prickly regulatory requirements. One requirement, which now exists only in an advisory capacity in Europe, may, upon its widespread adoption, fundamentally change the way power-supply makers and users look at the need for power-factor correction.

Though intended originally for household electronic equipment at power levels above 200 W, the requirement in question, IEC 555-2, allows a maximum third-harmonic current of 2.3 A with decreasing limits for higher-order harmonics. These limits will become even more stringent when a new revision (77A) is accepted. In this proposal, the standard applies to all equipment with line currents up to 16 A—there's no minimum. It also gives a relative as well as a reduced absolute limit for each current harmonic. The third-harmonic limit will now be set at 3.6 mA/W or 1.08 A absolute, with similarly decreasing limits for the higher orders.

The implications of the specification are already becoming clear. It's anticipated that these limits will be enforced extensively in Europe within the next year or two. Austria has begun invoking the standard and Germany is preparing to do so. Moreover, it's likely that the United States will soon begin to take these limits seriously. The effect of enforcement is to effectively ban the sale of any equipment that does not comply. Major systems manufacturers, who must be looking at least two years ahead in terms of their component specifications, should pay attention. If they want to get their products into the European marketplace, they'll be compelled to specify higher power factors and lower harmonic-current levels in their next-generation power supplies. The alternative, which is to specify a compliant and a non-compliant supply, is likely to be too costly for most OEMs.

There are some caveats to power-factor correction, though. For one, it makes the supply's design more complex. According to Lou Pechi, director of marketing at Power-One Inc., Camarillo, Calif., power-factor correction can increase design difficulty by up to a magnitude. When the power-supply business began emphasizing switching supplies instead of linear designs, much of the business went from captive to non-captive. Many power-supply consumers tried to design their own switchers in-house, but it required specialized design skills that were in short supply. Instead, many users bought switchers from OEM vendors. The same trend is likely to continue with the new generation of power-factor-corrected supplies.

On the one hand, Pechi agrees that enforcing the IEC 555-2 specification, on a virtual worldwide basis, is inevitable. But on the other, he noted, the IEC 555-2 specification doesn't demand a 0.99 power factor in all cases. For a 2000-W supply, in which harmonics will likely exceed the specification, the upper limits of correction are a necessity. As output levels decrease, however, the level of correction can fall as well. At 750 W, a 0.8 power factor is adequate. And at 500 W, users can probably live with a power factor of 0.6, which is the power factor of a regular power supply. Below 250 W, its not needed at all, because the harmonic content isn't there. The bottom line is that before specifying a power-factor-corrected supply for a given application, users have to dust off their Fourier textbooks and determine if it's needed at all.

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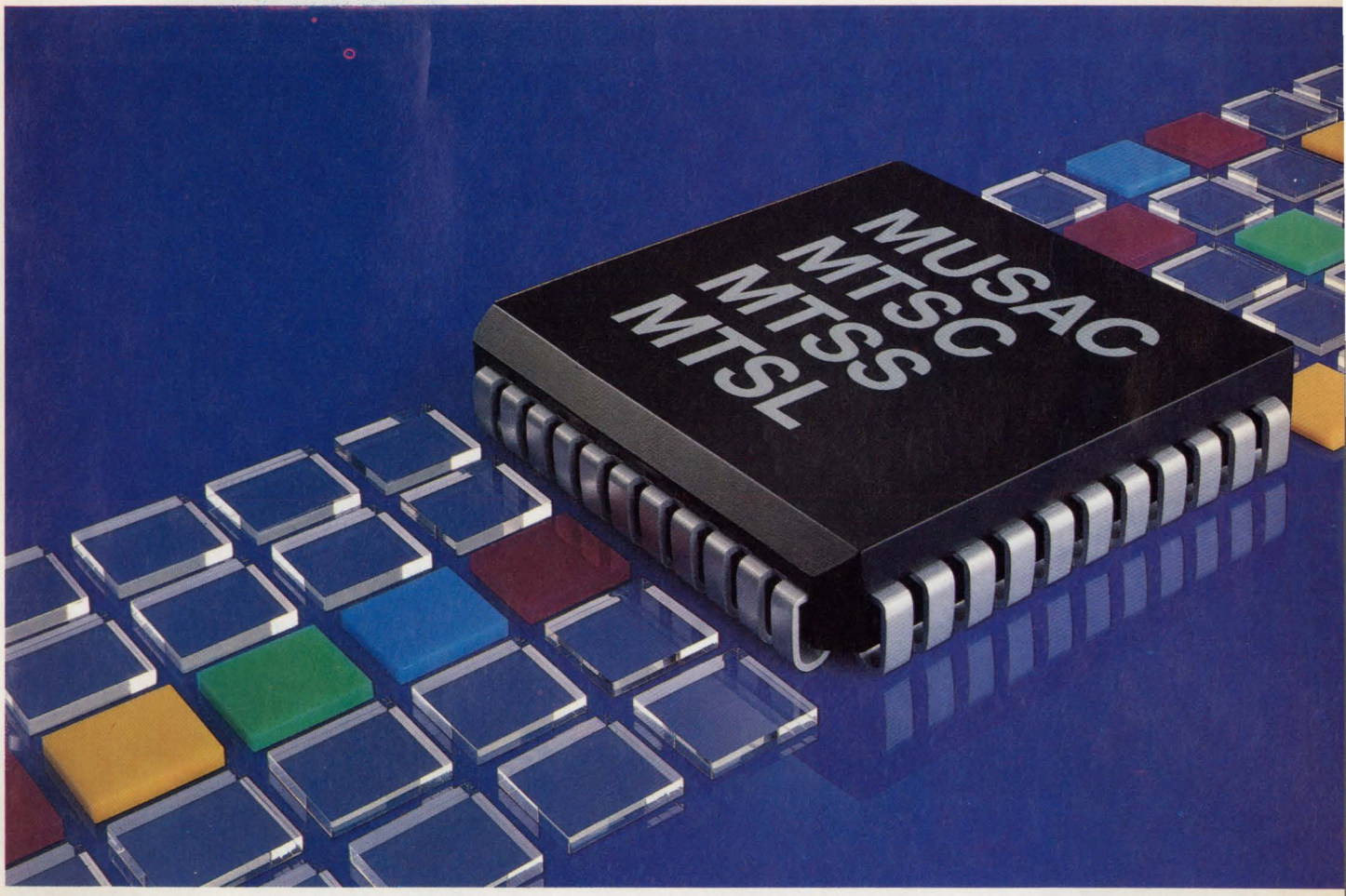

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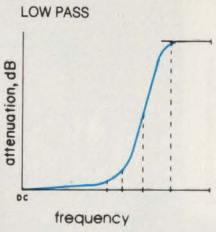

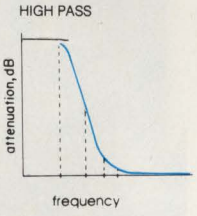

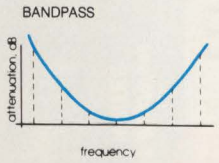

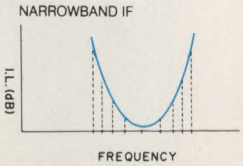

low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	PASS BAND, MHz (loss <1dB) Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	STOP BAND, MHz (loss > 10 dB) Max. F4	STOP BAND, MHz (loss > 20 dB) Min. F5	STOP BAND, MHz (loss > 20 dB) Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	STOP BAND, MHz I.L. > 20dB F6	STOP BAND, MHz I.L. > 35dB F7	STOP BAND, MHz I.L. > 35dB F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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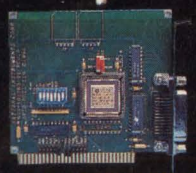

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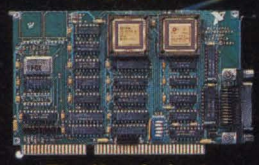

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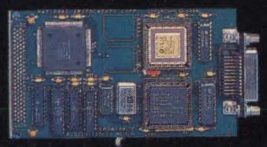

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DECstation TURBOchannel

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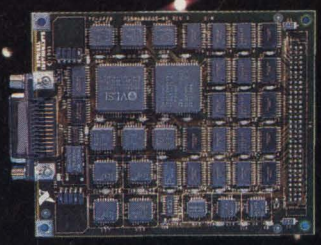
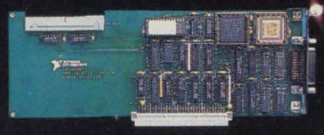


Macintosh NuBus



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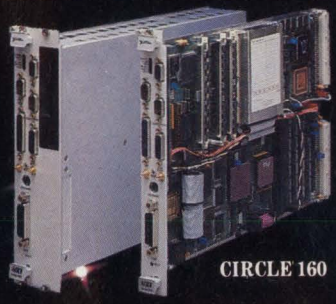

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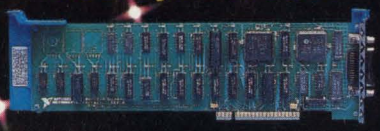
IBM PS/2 and RISC System/6000



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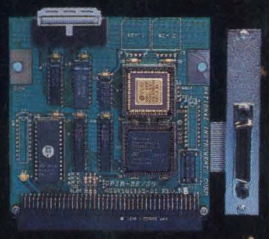
Macintosh SE/30



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By combining a harmonic-balance simulator and advanced graphics capabilities, a software package for RF engineers promises to drastically trim circuit development time. The simulator portion, from EEsof Inc., Westlake Village, Calif., lets designers analyze, tune, and optimize many linear and nonlinear RF circuits operating at frequencies of 3 GHz and below. As with lower-frequency software, such as Spice, the jOMEGA harmonic-balance program offers frequency- and time-domain simulation to analyze and optimize waveform characteristics. It also provides frequency response for such circuits as amplifiers, mixers, and oscillators, as well as for interface and signal-distribution networks. The harmonic-balance algorithms work with a full range of RF models (lossy and dispersive transmission lines, for example) developed for frequency-domain simulators. Nonlinear tuning and optimization capabilities quickly find the best conditions for amplifier outputs, mixer-conversion losses, and oscillator output-spectral purity. Other features include schematic entry, multi-window simulation controls, engineering documentation, and an optional module for RF board-design layout and floor planning. With that option, users can view circuit layout while simulating a design. Circuit parasitics and potential layout problems can thus be eliminated earlier in the design stage. The jOMEGA software runs on popular OS/2 and Unix platforms. It's starting price is $24,500. Contact Thomas Reeder, (818) 991-7530. *DB*

TECHNOLOGY DATABASE AIDS SYSTEM DESIGNERS

The first in a series of technology databases helps system designers approach their job from an international, market, and application-driven perspective. The Integrated Circuit Technology Database from Cypress Information Resources, Los Gatos, Calif., quickly gives designers about 100,000 IC offerings of over 350 IC companies for 500-plus applications. The application-structured database provides product selection and analysis with functional operation, electrical specifications, and product features for various VLSI chips. For example, a designer can enter in an application, such as data compression, and immediately retrieve a diverse selection of ICs. Or research and development, market, and vendor information, such as agreements, customer base, facilities, and sales could be examined. Addresses, fax numbers, and 800 numbers are listed for each company as well. The IC Technology Database, which costs $295, includes diskettes, a printed version of "The IC Product & Market Guide," and an instruction manual. For more information, call (408) 354-4887. *LM*

SOFTWARE DEAL AIMS FOR COMMON ENVIRONMENT

Hewlett-Packard Co., Palo Alto, Calif., and Sun Microsystems Inc., Mountain View, Calif., have inked a joint software development agreement to remove many application-interoperability barriers on different Unix workstation platforms. As a result, users will be able to seamlessly integrate data objects—text, graphics, and a spreadsheet block, for example—from systems made by different vendors on one or more networks. HP and Sun are targeting a common software environment to be made available through licensing. Initially, they've jointly defined an object-management specification—the object-management facility—and just proposed it as a common standard to the Object Management Group, a 108-member organization. The proposed standard employs object-management technology from HP and distributed computing technologies from both companies. In the next stage, both firms will work with standards bodies to promote interoperability of the HP network computing system and Sun's open network computing standards at the working protocol level. The ultimate objective is a common distributed application environment for Unix and other operating systems. Sunsoft Inc., Sun's new software subsidiary, will do the development work with HP. Contact Robert Frankenberg of HP at (408) 447-0905 and Edward Zander of SunSoft at (415) 336-6543. *DB*

IBM STRENGTHENS ITS SUPPORT FOR ISDN

Following up on its 7820 terminal adapter for the Integrated Services Digital Network (ISDN), IBM Corp., White Plains, N.Y., deepened its ISDN market involvement with several additional products and services for its PS/2 workstations. The company's new ISDN Interface Coprocessor/2 Model 2 adapter card attaches to the ISDN Basic Rate Interface. The card, teamed with supporting IBM software, transmits full-duplex data at 64 kbits/s over each of the two information (B) channels, controlled by the 16-kbit/s control (D) channel. This processing speed is over six times faster than 9600-bit/s modems currently used with PS/2s. Up to four cards can be installed in a PS/2 workstation for ISDN connection to similarly equipped IBM systems using either the 7820 terminal adapter or the new 3174 ISDN Basic Rate Interface adapter. Four ports on the 3174 support up to eight

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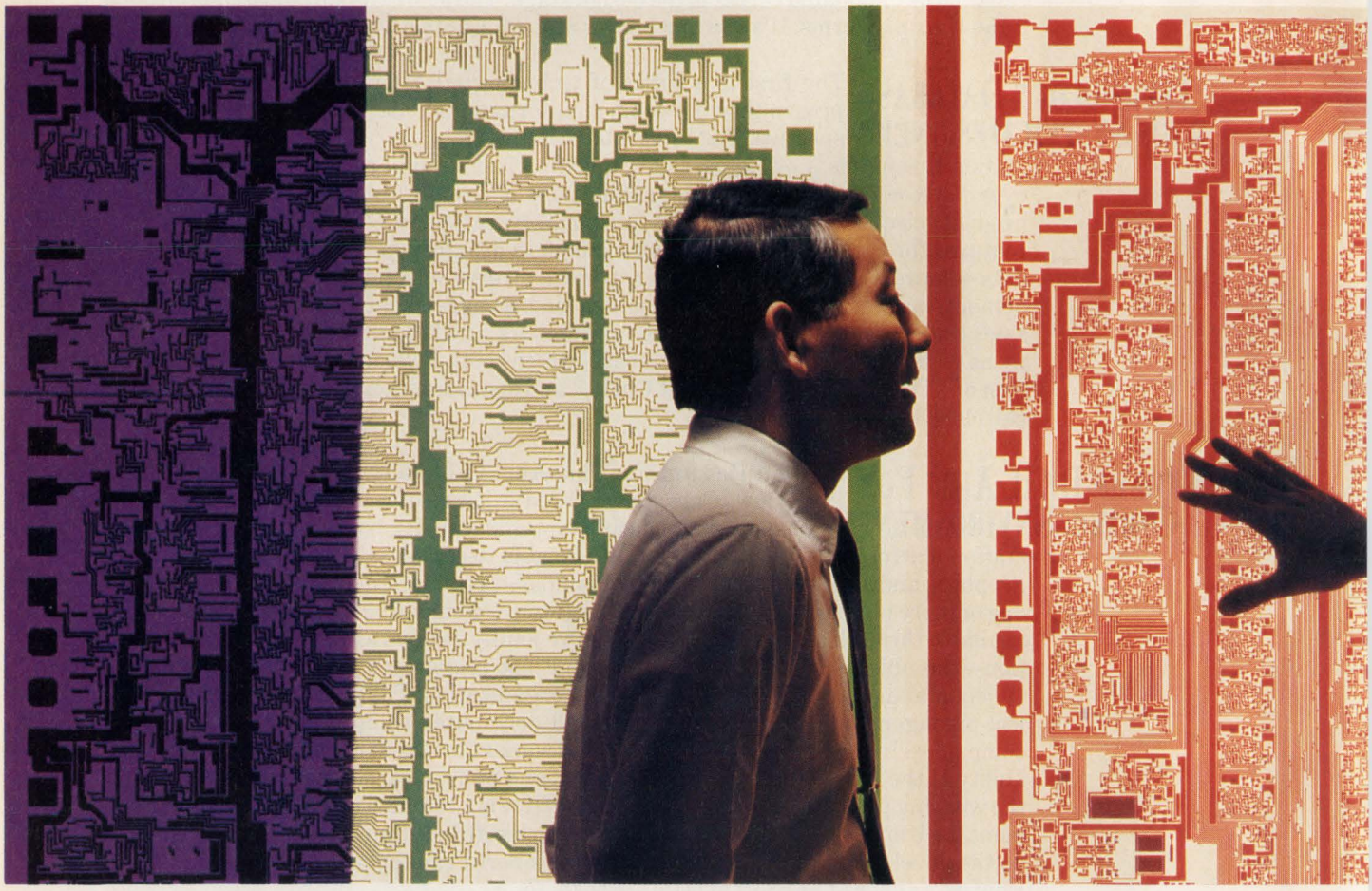

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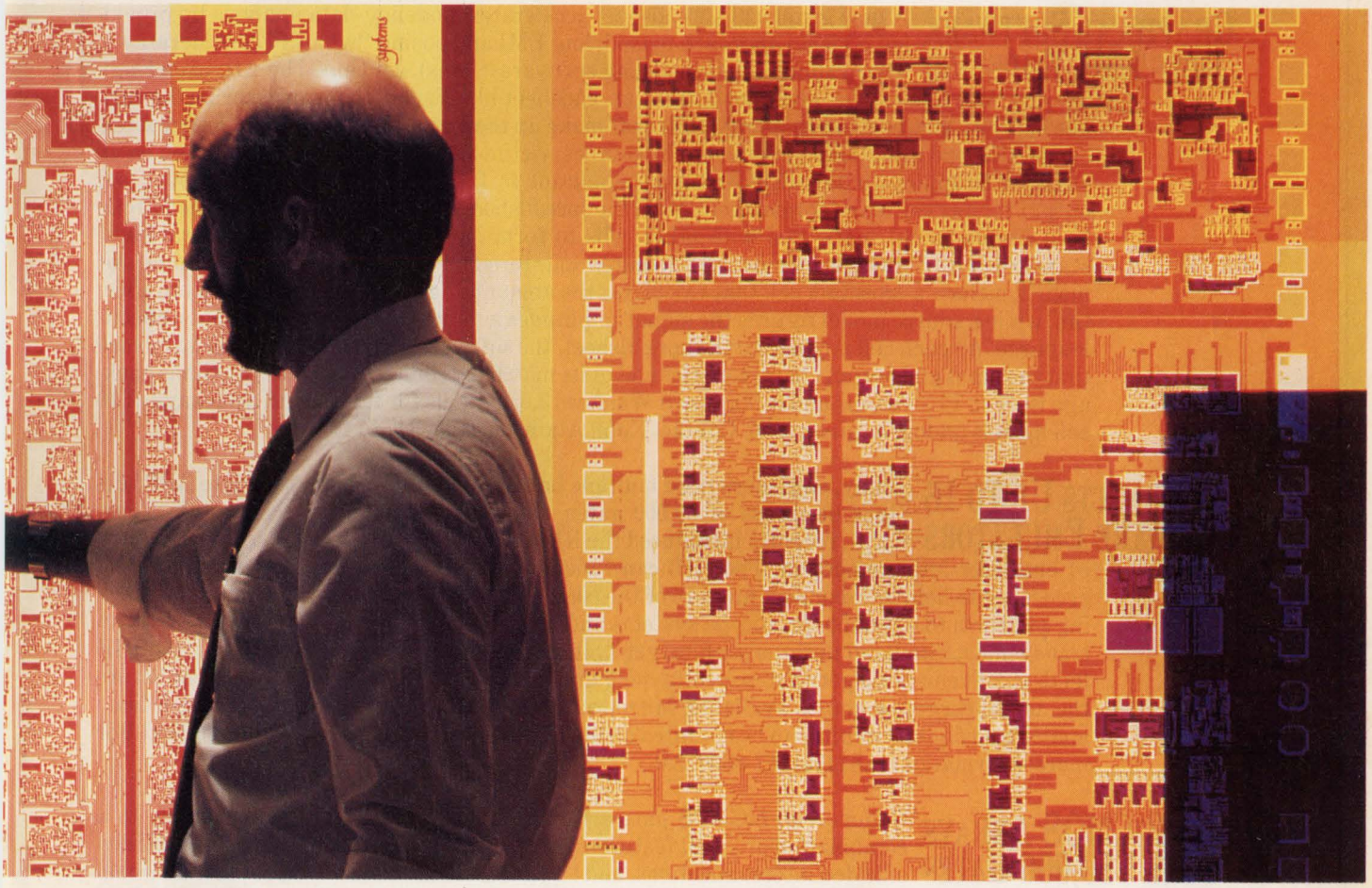

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SERVICE GROUP JUDGES SYSTEM PERFORMANCE

A service called Performance Design and Debug (PDD) is now available to designers of complex electronic and computer-based systems. Typical users of PDD, from CAE Plus Inc., Austin, Texas, are electrical and computer engineers who evaluate system performance prior to implementing a new design or debugging performance problems in existing systems. CAE Plus uses validated and parameterized architectural models along with client-supplied data to identify performance attributes and bottlenecks. PDD features customized architectural models, model validation, analysis of simulation results, and architecture design recommendations. For more information, call (512) 338-0165. *LM*

GRAPHICAL SOFTWARE DOES EMI MODELING

A new graphical spreadsheet accelerates modeling-data analysis by providing a visual approach to modeling EMI and posing "what-if" considerations. The graphical EMI modeling software (Gems), developed by Atkinson Engineering, Warrenton, Va., gives designers a spreadsheet-like display that can describe the various sources, victims, and coupling paths that make up the overall EMI situation. Every interconnection and interrelation between the sources, victims, and coupling paths can then be visualized. Graphics window displays supply amplitude vs. frequency plots for input, model, and output for any cell in the spreadsheet. With the spreadsheet concept, each cell (item model) can be a simple model that's tied with other cells to form more complex models. Libraries of standard or configurable models can be created and stored for future reuse. Some examples of models include a crosstalk cell that calculates the amount of crosstalk from a culprit to a victim, while a source model figures the signal amplitudes and frequencies generated at a specific source. As each cell is added to the spreadsheet, the software checks the cell type to ensure that the input and output characteristics and units match the connecting cells. The Gems package runs on PC systems under Microsoft Windows 3.0 and sells for $2950, with a package of 10 cell models adding another $950. Contact Kenn Atkinson, (703) 347-5716. *DB*

BOX CONNECTS UP TO 16 HARDWARE EMULATORS

Today, engineers need multiple hardware emulators that validate ASIC designs in excess of 50,000 gates. Quickturn Systems Inc., Mountain View, Calif., recently introduced the RPM Interconnect Box (RIB) to ease the task of emulator interconnection. The RIB can function either as a connector and breadboard accessory to help interconnect up to 16 of the company's RPM emulators or as a breadboarding platform to assemble prototype systems and to interconnect to an RPM emulator. It can also connect emulated designs with target systems. As a breadboarding platform, the RIB lends a convenient target-system prototyping area for connection to an RPM emulator before the actual target system is available. Microprocessors, peripherals, RAM, and user-defined analog and digital circuits can be mounted on the RIB. The RIB is available now for $2950. For more information, call (415) 967-3300. *LM*

LARGEST BiCMOS ARRAYS PACK 150,000 GATES

Commercial biCMOS gate arrays have now hit 150,000 gates thanks to a combination of small features, three levels of metal, a half level of localized silicided interconnections, and an epitaxial-based biCMOS process. This chip is the largest in a family of seven from Texas Instruments Inc., Dallas. The abundant levels of interconnection allow array utilization to approach 75% in most applications. The sea-of-gates architecture is akin to the one reported at several previous conferences, with just a few minor adjustments. Compilers are available to custom-define memory blocks, data paths, and other functions. Unloaded gate delays are typically about 150 ps, while on-chip RAM blocks achieve 3-ns access times. TI will allow large customers to define a user-specific version that has RAM, ROM, or data-path sections prediffused into base silicon. Core logic on the biCMOS arrays (without the I/O buffers) consumes only about 10% more power than logic on a pure-CMOS array. From 80 to 320 signal pins are available, depending on the array. Package pin counts range from 100 to 240 leads when housing an array in a metal quad-sided flat package, and up to 409 pins for a pin-grid-array package. Contact Tom Sprunger at (214) 997-3156. *DB*

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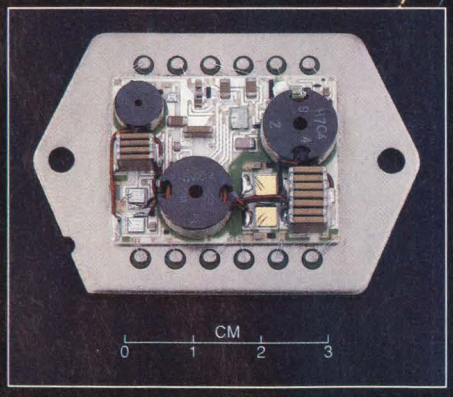
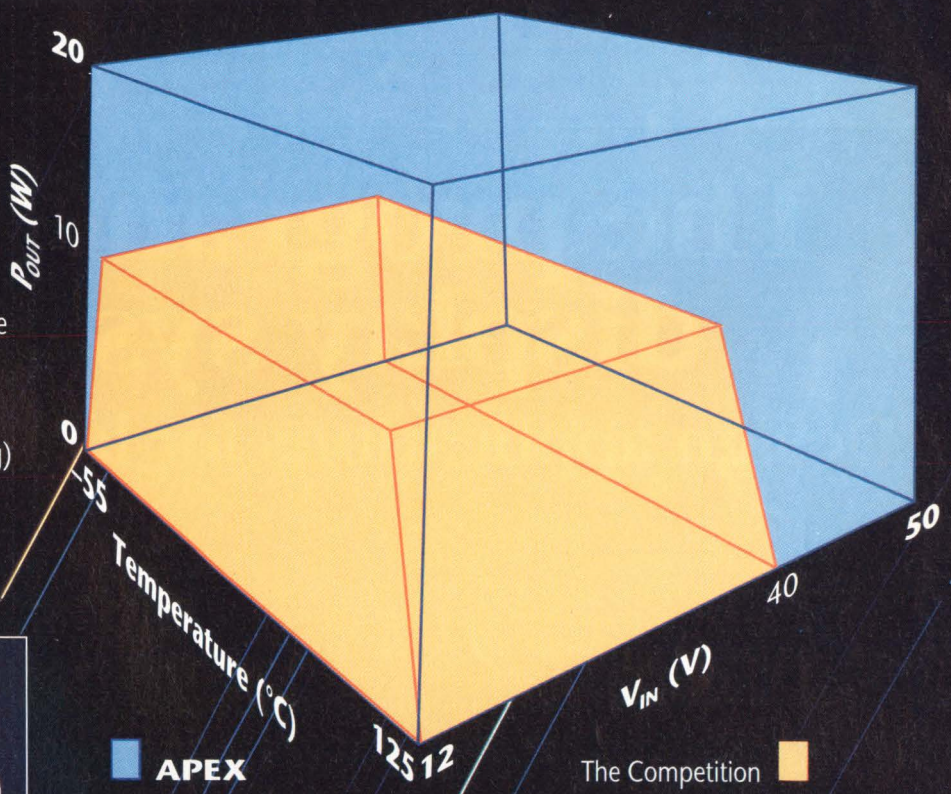


PATENT PENDING



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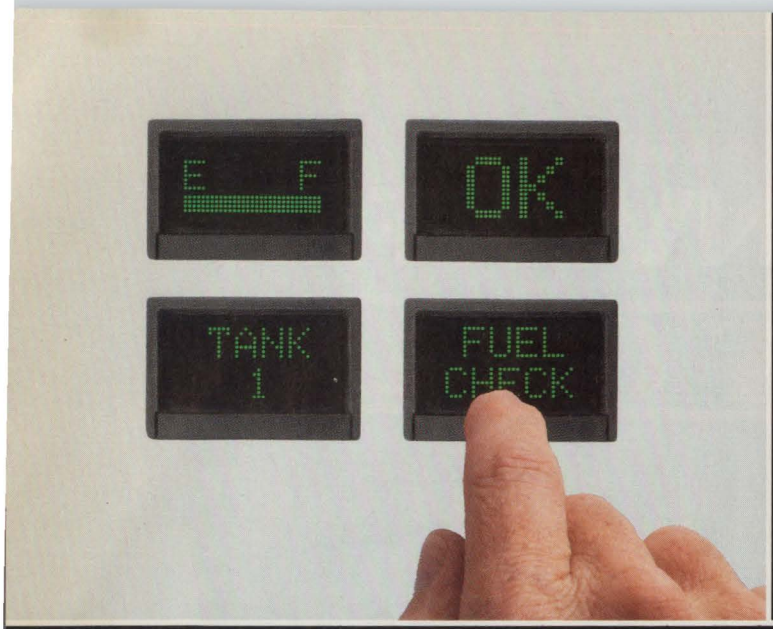
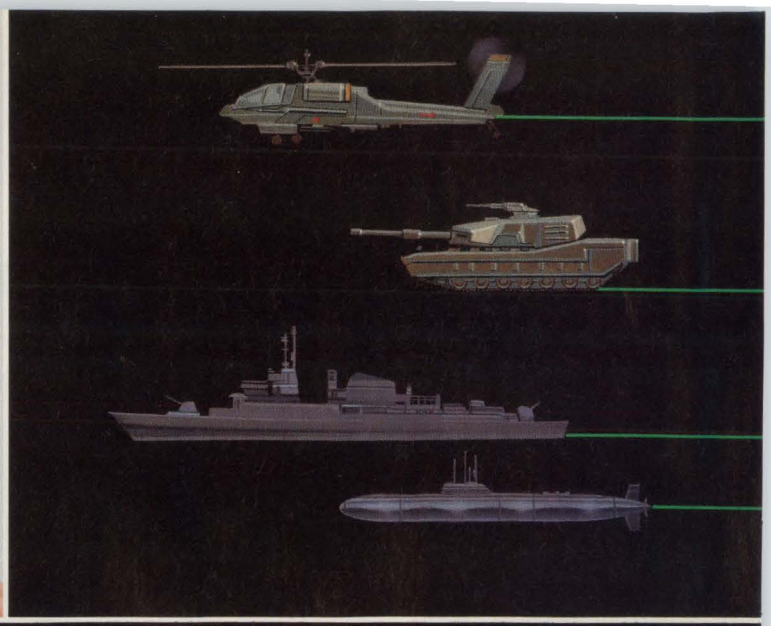
CIRCLE 85





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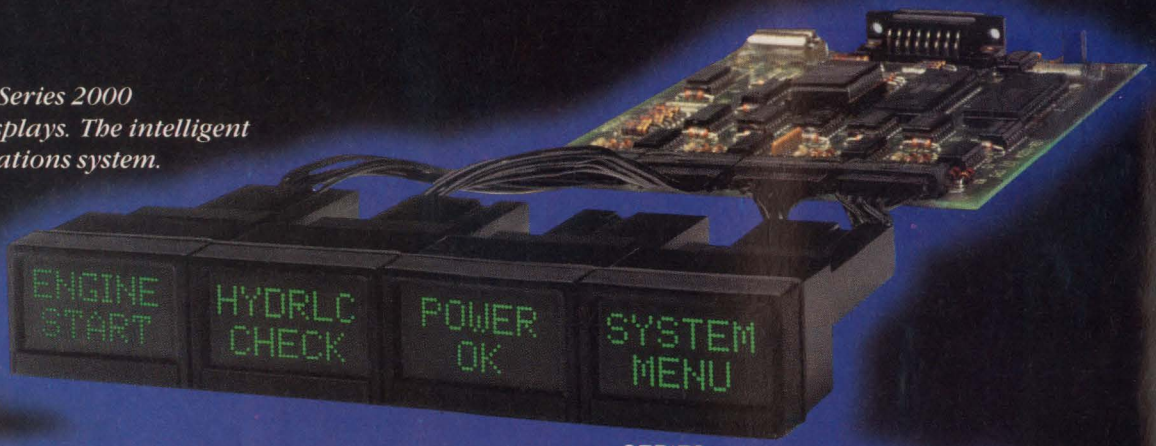


SERIES

VIVISUN 2000™

CIRCLE 106

U.S.-JAPAN DEVELOPMENTS ENHANCE DRAM PERFORMANCE AND PACKAGING

A pair of joint U.S. and Japanese developments promise to improve dynamic-RAM density and performance, as well as revolutionize the way chip design is approached. In one development, a new field-shield-capacitor cell structure improves the densities and speeds of DRAMs, and simplifies their structures. In another development, a packaging technique called lead-on-chip with center bond (LOCCB) allows DRAM designers to put more silicon in the same package size. It also minimizes on-chip noise and improves DRAM lead electrical uniformity.

As dynamic RAMs increase in density, fabricating their storage cells gets more and more complex, with designers being forced to either stack layers above the substrate or create trench structures in the substrate. A novel coaxial memory cell, created inside a trench, now promises to simplify the fabrication processes compared to other trench or stacked structures previously described by other companies. The cell was developed jointly by a small U.S.-based design consulting firm, United Memories Ltd., Colorado Springs, Colo., and NMB Semiconductor Ltd., Chiba, Japan.

Designers at United Memories in 1988 took a field-shield coaxial capacitor structure and implemented DRAM storage cells that provide sufficient capacitance for use in 4-, 16-, and possibly 64-Mbit-generation DRAMs. First prototypes of the structures for a 4-Mbit chip yield access times of 50 ns with a chip that fits in a 300-mil DIP.

The field-shield structure incorporates a polysilicon field-shield layer in the isolation or field-oxide region of the memory cell *(see the United Memories/NMB figure)*. By holding the field-shield region over the p-well implants in the substrate at ground potential, n-channel parasitic devices can be shut off. The field-shield sections over n-well regions are kept at the supply level to shut off p-channel parasitic field devices.

Because the gates of both parasitic transistor types are actively held off, the devices' threshold voltages can be set for about 2 V. Standard devices made with local-oxide-isolation schemes require a 10-V isolation capability, which means larger spacings between devices. The lower voltage enables the field-shield devices to be closer because isolation distances don't have to be as large. The field shield also precludes a field implant, simplifying the manufacturing flow.

Although the memory cell might be loosely classified as a "stacked-in-trench" type structure, the field shield goes into the trench before the cell electrode. That shields the cell electrode and reduces cell leakage. The combined structure is known as a buried-electrode shielded-trench (Best) cell.

Only two masking steps are required to build the Best capacitor, compared with the three to five masks typically needed for stacked capacitors. Moreover, only two etch steps are needed (one is a trench-formation etch). By comparison, a stacked-capacitor structure requires three to five etch steps (but no trench etch).

Because the field shield goes into the trench before the cell electrode and is separated from the substrate by a grown oxide, the trench's sidewalls and bottom serve as isolation areas. Consequently, there's no need to dope the sidewalls of the trench, as might be required in a typical trench process.

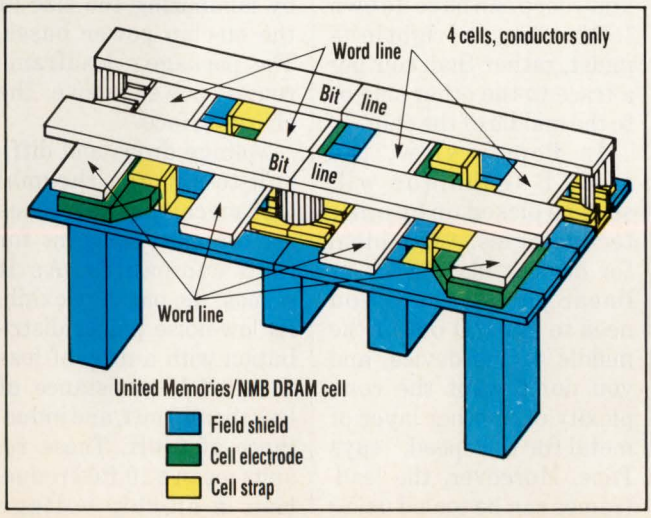
The counter-electrode of the DRAM cell capacitor serves as the field shield. This shield encloses the cell's capacitor electrode, preventing any cell-to-cell or cell-to-substrate coupling. That reduces any pattern sensitivity of the memory array. Furthermore, because the cell's capacitor electrode is shielded from the substrate by the field shield, trenches can be located adjacent to the wordline transistor without affecting the wordline-transistor characteristics.

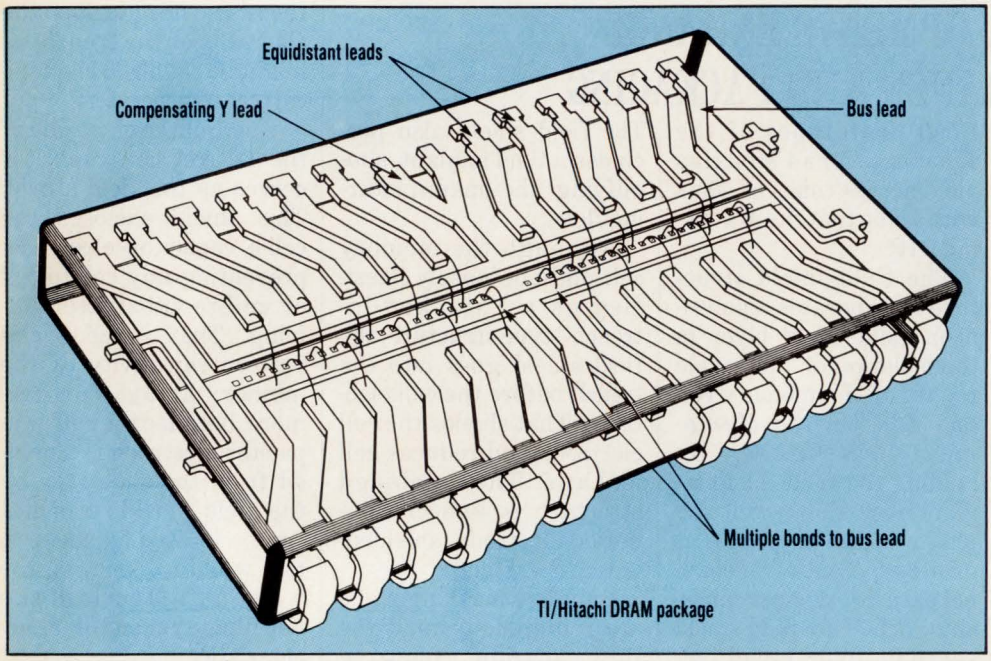
A high resistivity p-type substrate and shallow p well help fabricate n-channel transistors with low-body effects and low source/drain-to-substrate capacitance.

The low-body effect lets more of the charge reach the memory cell during a write operation. That eliminates the need to boost or bootstrap the wordline, simplifying memory circuit design and reducing chip operating power.

One key issue during coaxial-cell fabrication is the need for a highly selective polysilicon etching process, so that the polysilicon can be removed without affecting the oxide layer. An etch ratio of about 15:1 is needed, and that ratio can be achieved on a repeatable basis with today's processing equipment.

In a related area of DRAM development, wide-ranging implications can be seen with the recent packaging innovations from Texas Instruments, Dallas, and Hitachi America Ltd., Brisbane, Calif., in





their forthcoming 16-Mbit DRAM. The new package involves bond pads running in parallel rows down the chip's center rather than around its edges. The chip is then wire-bonded to a leadframe that extends over the top of the chip.

For a 16-Mbit DRAM, the effect is to create a very stable ground with multiple bonds to the chip. But the leadframe technique carries great promise for future memories, plus other technologies involving large die and high speeds, such as ASICs and linear ICs. It also may change the way designers approach chip design and layout: Traditional approaches, with bond pads around the chip's perimeter and a third layer of metal for grounds, may be passe.

According to Ken Pope, manager of product marketing for Hitachi America, the LOCCB packaging technology will shine brightest when it's applied to memory devices handling such wide words as by-16 and by-18 parts. The multiple outputs required by such chips can benefit greatly from the stable ground offered by the LOCCB technique.

In addition, the technique allows bond pads to be placed where it's most convenient for the design's sake and not for bonding machines. It also saves the complexity and expense of a third or fourth layer of metal to achieve the highest possible speed. In a high-speed static RAM, for example, a block of memory cells that's perhaps 512-kbits deep can have its own I/O bonding pad right in its midst, rather than routing a trace to the other side or to the middle of the chip.

In Pope's view, the LOCCB technique will soon be picked up by other technologies. "It's ideal for devices like ASICs or linear parts, where you need to get I/O out of the middle of the device, and you don't want the complexity of another layer of metal for the speed," says Pope. Moreover, the leadframes can be tooled using standard CAD tools for ICs with irregular structures.

The packaging technique is the first result to be disclosed from the total 16-Mbit DRAM development project the two companies launched in December, 1988. The memory's plastic SOJ package houses chips as large as 330 by 660 mils, conforms to JEDEC standards of 400 by 725 mils, and has dual-power (V_{CC}) and ground (V_{SS}) pins. The lead-on-chip package also offers a very area-efficient chip design by minimizing the size of the on-chip power buses. The package's leadframe routes power above the chip's surface.

Voltage drops and difficult-to-manage thermal and mechanical stresses are foremost concerns for both companies. As it stands, the package exhibits low-noise power distribution with a drop of less than 0.2 V, resistance of less than 10 mΩ, and inductance of 6 nH. These results mean a 10-fold reduction in on-chip voltage spikes compared with conventional plastic SOJ packages, which have 20-mΩ resistances and 10-to-20-nH inductances in the on-chip power buses.

At the heart of the LOCCB design is its balanced-capacitance leadframe that maintains uniform input-pin capacitance. All internal leads are equidistant from each other. A passive Y lead in the middle of the leadframe, and on either side, minimizes differences in pin-to-pin capacitance *(see the TI/Hitachi figure)*.

Two metal bus lines run parallel above the full length of the chip. One links the dual V_{SS} pins located at the ends of the package, while the other links the corner dual V_{CC} pins on the other side of the chip. As a result, multiple bonds exist from the power and ground pins to the circuit. With dual pins for each bus, resistance is slashed to under 10 mΩ, effective inductance to about 6 nH, and electrical noise to less than 0.2 V.

Later iterations of the 16-Mbit DRAM will involve smaller die, and the leadframe will shrink accordingly. But rather than going to fewer pins, which would take the part out of JEDEC standards, the developers may widen some traces to improve speed as they work toward wide-word memories. Another advantage of the LOCCB technique is that because the bond pads aren't on the chip's periphery, designers gain some space on the die for circuitry. That means more than one generation of die could be squeezed into a same-size package.

DAVE BURSKY and DAVID MALINIAK

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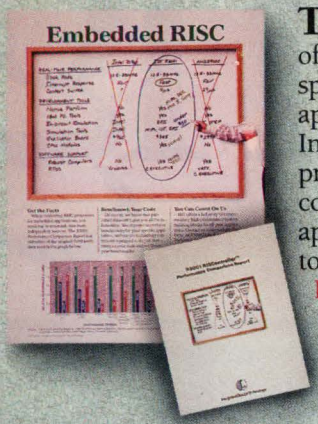

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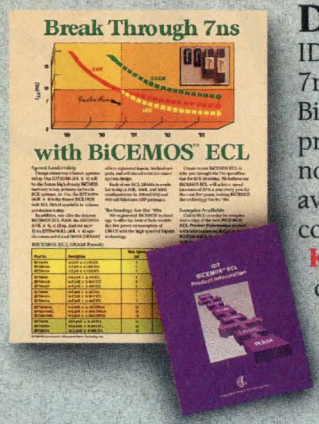

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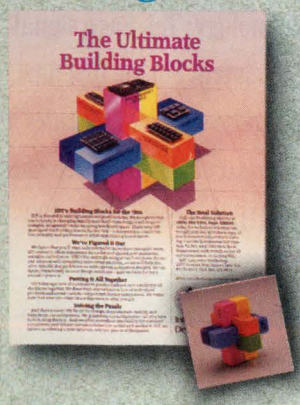

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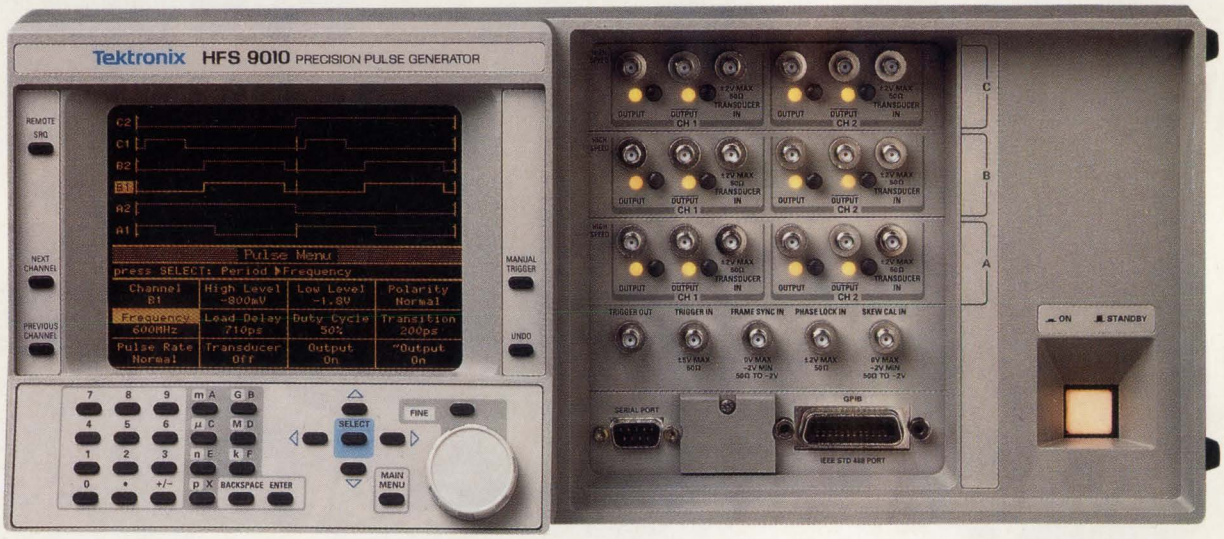

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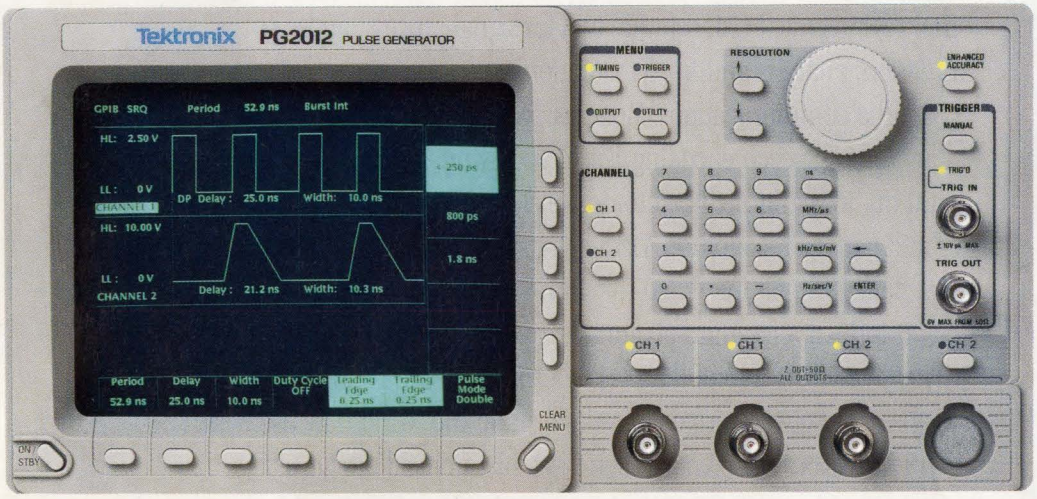

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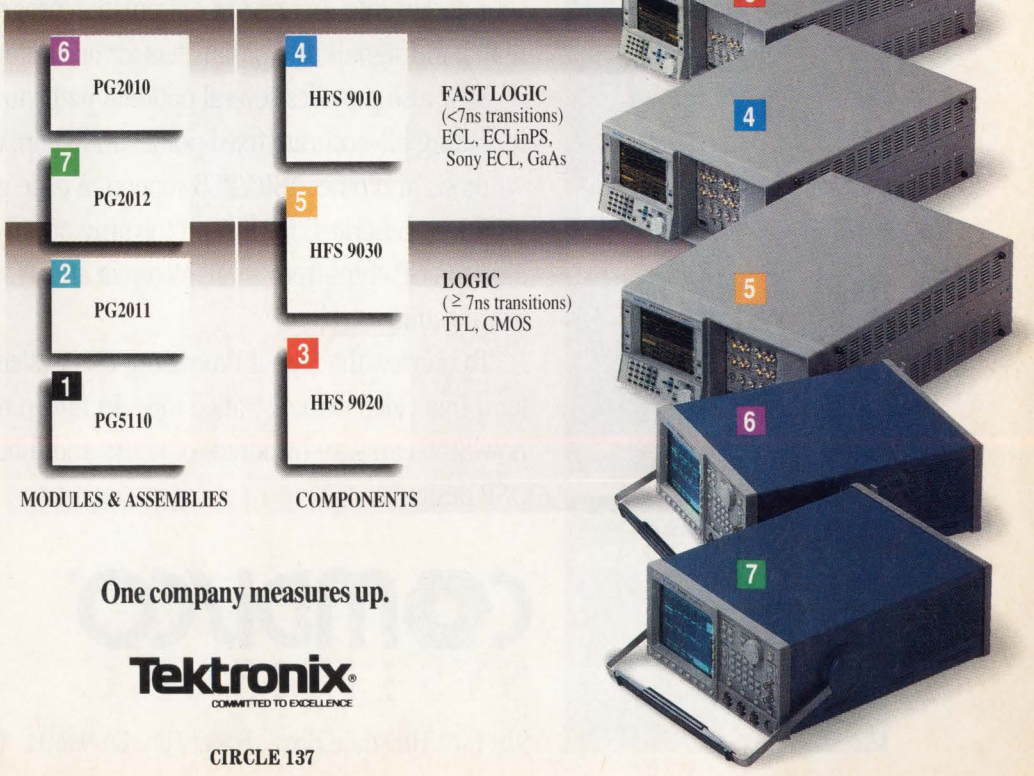

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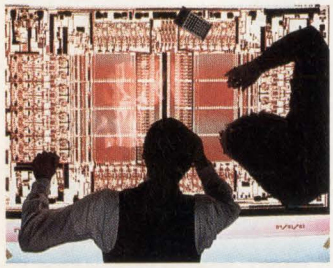

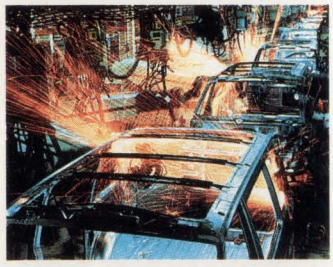

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CIRCLE 133

TWO CHIP-SET OPTIONS LET DESIGNERS READILY IMPLEMENT SMALL OR LARGE STORAGE USING REDUNDANT ARRAYS OF INEXPENSIVE DISKS.

BUILD SCSI RAID SYSTEMS TO BOOST DATA AVAILABILITY

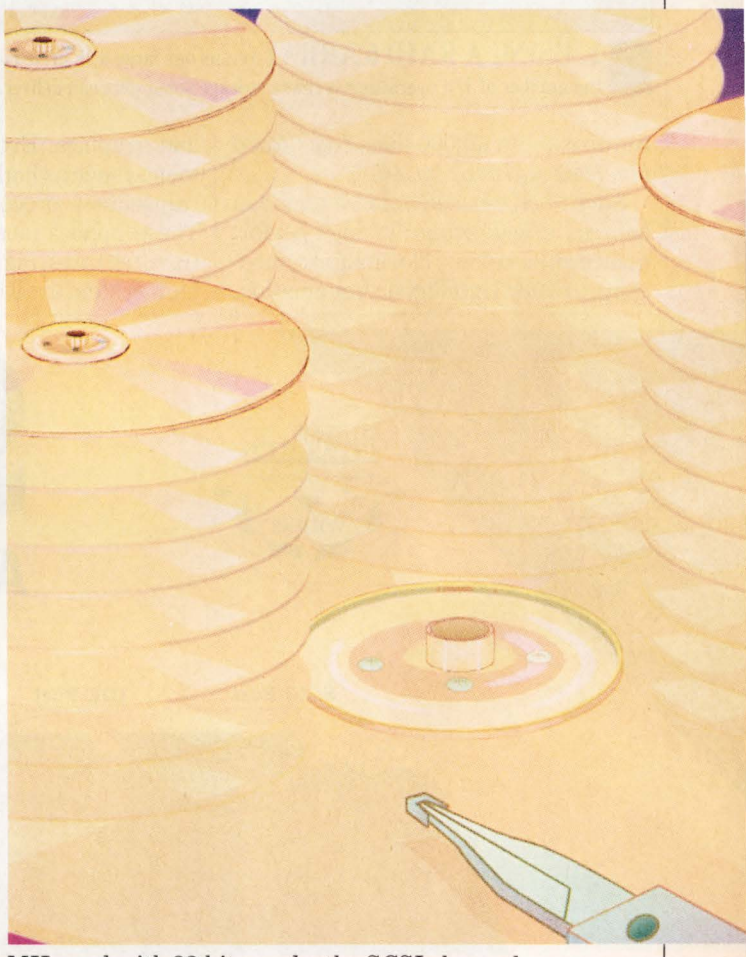
DAVE BURSKY

Now that CPU throughput rates and new system buses (the extended ISA, IBM's Micro Channel) have faster data-transfer rates than standard mass-storage subsystems, designers are being forced to reexamine the subsystems to eliminate I/O bottlenecks. Implementing fast and wide options of the ANSI SCSI-2 standard can push data rates to 40 Mbytes/s. But single disk drives can't sustain such data rates.

One solution, an offshoot of research at many universities, is using redundant arrays of inexpensive disks, better known as Raid architectures, for the storage subsystem. When combined with fast- and wide-SCSI controllers, Raid systems offer higher I/O throughputs to keep up with fast processors. Data is also better protected against drive failures, large "virtual" disk drives can effectively be created, and the redundant drive array's cost more than offsets the potential cost of losing mission-critical data.

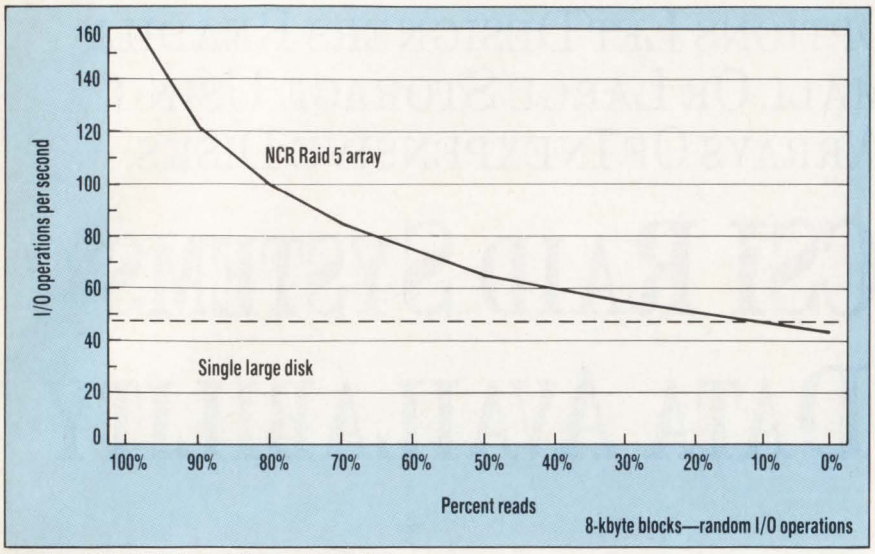
The biggest problem with implementing a Raid subsystem is the design and programming of the storage controller that manages the array of drives. Seizing both sides of that design challenge, NCR has come up with a two-pronged solution. The first is the industry's first commercial chip sets for building small and large Raid systems that can be configured for Raid levels 0, 1, 3, and 5. Except for a few rare cases, those four levels will satisfy any system design requirement.

As part of those chip sets, the first 16-bit wide and fast-SCSI 2 controller (the 53C916) and a bus extender (the 53C932) allow building 32-bit wide- and fast-SCSI channels. At 10 MHz and with 32-bit words, the SCSI channel has four times the throughput of the fiber-optic I/O channels used on mainframes. And it runs ten times the speed of desktop system I/O transfers.



The second half of the solution is a control program that runs on an Intel 68020 controller that implements Raid levels 0, 1, 3, and 5. Such a program has well over 125,000 lines of code. A program for just one Raid level might

RAID STORAGE CONTROLLER



1. USING A RAID 5 ARRAY versus one large disk drive could more than double the number of I/O operations/s that a storage subsystem can deliver.

require about 40,000 lines *(see "Raid levels explained," p. 40).*

Such SCSI-2-based Raid systems can address a wide range of high-performance applications, like imaging, modeling, artificial intelligence, simulation, and graphics. Even business requirements, such as high-throughput on-line transaction processing, can benefit. These applications require very high transfer rates, high data integrity, and high system availability—at low cost.

The number of I/O operations per second is a good measure of drive subsystem performance, says Al Loftus, NCR's director of logic products. For a single drive, a system might typically achieve close to 50 I/O operations/s (assuming 8 kbytes per I/O transfer). With a Raid subsystem, however, more than twice that can easily be achieved with a SCSI-2-based Raid system due to the various parallel operations that take place inside the array *(Fig. 1).* Furthermore, he continues, depending on such factors as hardware cost, its performance, and data availability, a different level of Raid architecture might be appropriate to better match the system applications. Other more detailed factors include the logical-block size used by the system, and the read to write ratios for data in the files. Different factors may influence the choice of Raid level *(see the table).*

There are two separate chip approaches that NCR offers. The first, for small arrays, consists of two new chips: the 53C916 wide-SCSI-2 controller with a 16-bit interface and 20-

RAID STORAGE CONTROLLER

Mbyte/s data-transfer capability, and the 53C920 SCSI data-path manager. Several standard SCSI controllers (such as the 53C96) and other readily available components are also included. The combination will enable designers to build single-board controllers that can control a small array of five SCSI devices and transfer data to the host system *(Fig. 2)*. Data transfers can be done either over another SCSI port, or through a system bus connector for an IBM PC or compatible. The PC or compatible can have an AT bus (also referred to as ISA or industry-standard adapter bus), or a Micro Channel Adapter (MCA) bus. Also possible are an extended ISA bus or an Apple-compatible NuBus interface.

RAID SELECTION CRITERIA PRIORITIZATION

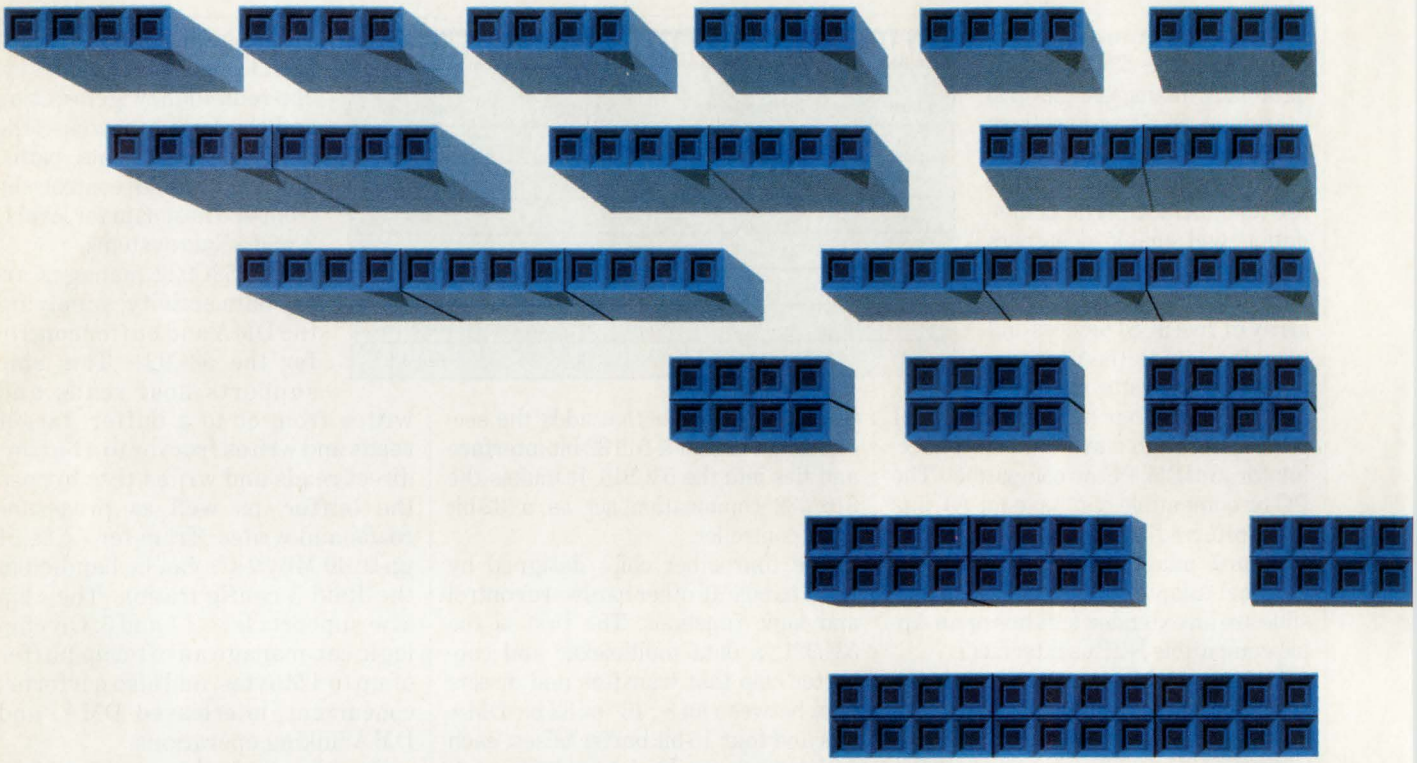
Cost	Performance	Data availability	Optimum raid level
—	—	X	Raid 1
—	X	—	Raid 0
—	X	—	Raid 1
X	—	—	Raid 0
X	—	X	Raid 3/5
X	X	—	Raid 0
X	X	X	Raid 3/5

For larger drive-array systems, the second approach employs five more custom-developed chips that supplement the 53C916. The expanded configuration handles arrays up to 90 drives. One of the extra chips is the 53C932, a SCSI bus extender that adds the second 16-bit half of a full 32-bit interface and ties into the 53C916. It makes the 916/932 combination act as a 32-bit SCSI controller.

The four other chips designed by NCR handle all other hardware control and logic functions. The first is the 53C921, a data multiplexer and converter chip that transfers and directs data between an 8-, 16-, or 32-bit DMA bus and four 16-bit buffer buses, each with byte parity. Each bus also has a 4-word FIFO register to buffer the data transfers and lessen rate dependence during asynchronous transfers. The chip also includes cyclic-redundancy generation and checking to increase the integrity of the data paths. The chip would control the front-end host data for level 1, 3, and 5 Raid systems.

The 53C922 manages array data activity, supplying the DMA and buffer control for the 53C921. This chip supports host reads and writes from or to a buffer, target reads and writes from or to a buffer, direct reads and writes that bypass the buffer, as well as processor reads and writes. Transfer rates of up to 40 Mbytes/s can be handled in the Raid 3 configuration. The chip also supports levels 1 and 5. On-chip logic can manage an off-chip buffer of up to 4 Mbytes, and also performs concurrent, interleaved DMA, and DMA linking operations.

Providing the basic control functions to implement the Raid subsystem, the 53C923 is designed to supply the bus



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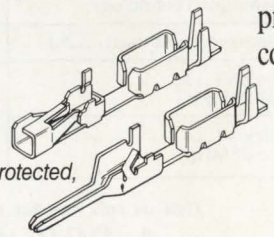
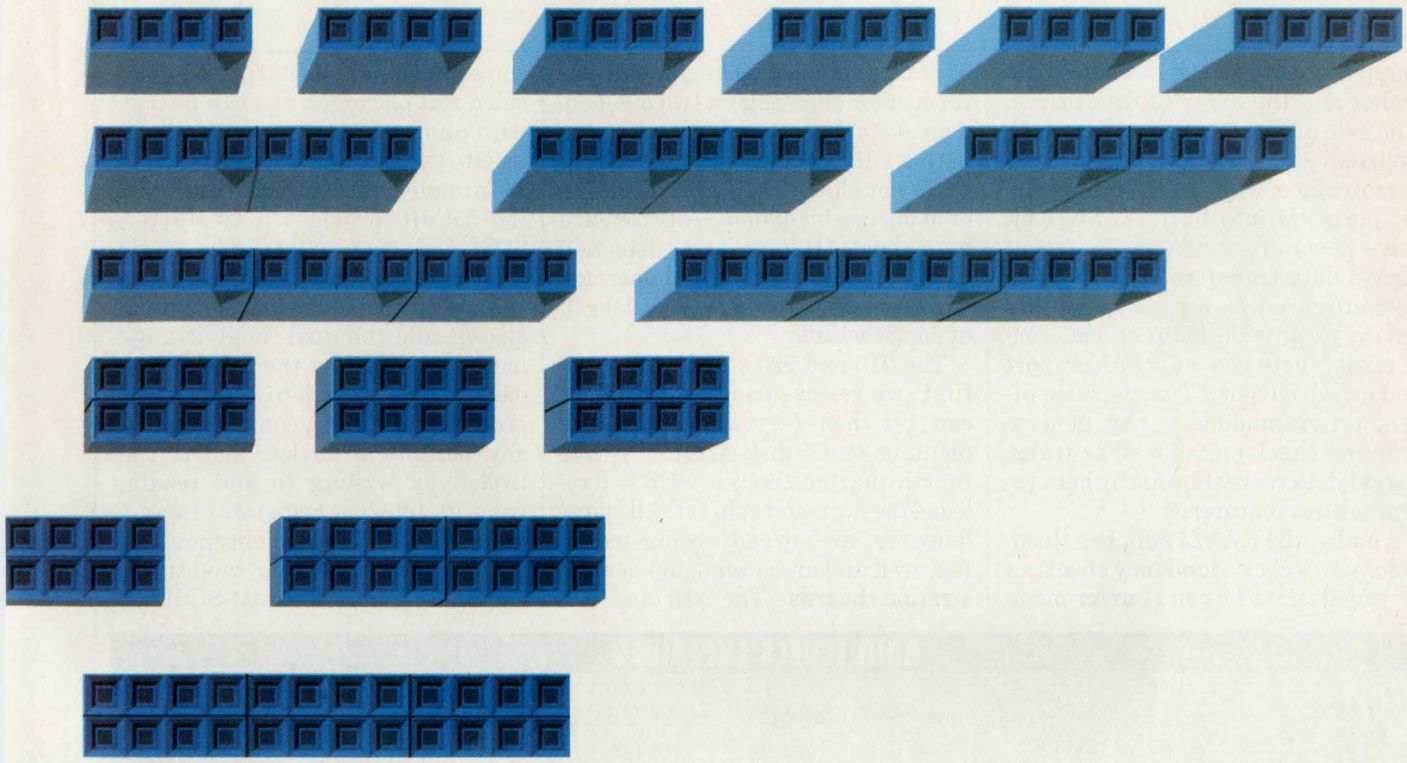


Dual-beam contacts are over-stress-protected, and feature post stops to protect wire on wrap type posts.



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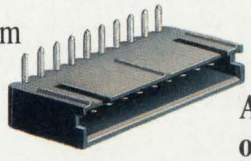

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mapping between the interface controller and the array of disk drives. One side of the chip has a 16-bit multiplexed address/data host-processor interface, while four additional 9-bit ports tie into buffers. Six 9-bit drive ports are available for target (drive) data transfers. The chip can be configured as a passive routing device to provide bidirectional connectivity between any buffer port and any drive port. The chip also offers programmable parity generation and checking, as well as transparent data recreation and other system control features.

Finally, the 53C924 supplies Reed-Solomon cyclic redundancy checking to provide data-bus and buffer-memory error detection. The chip can perform error checking on two independent data paths and functions as both a CRC checker with two check bytes per block and as a parity checker using one bit of odd parity for each byte of data. It guarantees detection of any one-word error and operates with a maximum data-block length of 65,534 words.

The 916 and 920 chips will be the first two released so that designers can get their feet wet with implementing small disk arrays. By the fourth quarter, though, NCR will release the high-end chip set. All chips, however, are already being manufactured and are running on demonstration boards. The 916 and 920 come in 84- and 160-lead plastic quad-sided flat packages and can be used with almost any SCSI controller to tie into the five SCSI drives.

To implement the small disk array, the 53C916 provides a 20-Mbyte/s SCSI-2 interface with a 16-bit single-cable data path to maximize the data-transfer rate. However, the chip can also handle the dual-cable arrangements specified by the SCSI-2 standard. The chip ties into a local microprocessor and DMA control logic like any peripheral device, and is controlled by writing to and reading from its internal registers. In addition to supporting asynchronous and synchronous operating modes, the chip also supports the fast-SCSI syn-

RAID LEVELS EXPLAINED

The concept of Raid—redundant arrays of inexpensive disks—evolved from university research into schemes to improve disk-drive data I/O transfer rates, storage capacity, and drive-subsystem reliability (uptime). Raid basically refers to an architecture that safeguards data. If a disk fails, data can be reconstructed, because data is striped across several disks. An extra disk drive is typically used in the Raid approaches, either to serve as a dedicated parity drive or to hold part of the striped data.

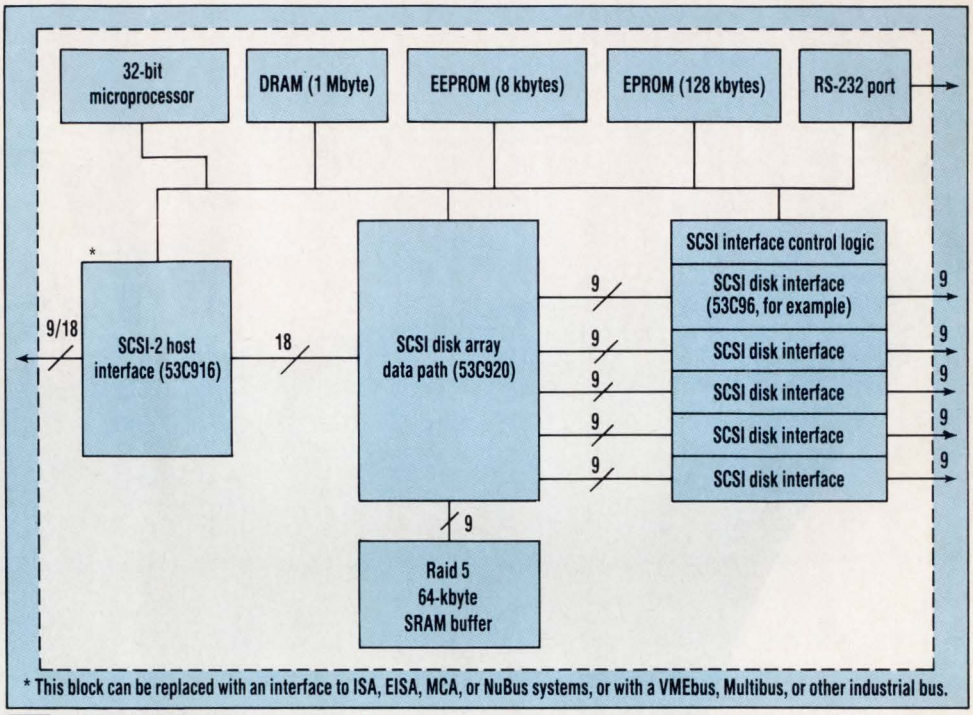
Redundant arrays offer very high data-availability ratings, because even if one drive fails, data can be accessed transparently to that failure. The arrays are also high in performance since multiple spindles can access data concurrently. And, the arrays can be very cost effective because multiple low-cost drives are used rather than the highest-density single-spindle drive. There are six basic Raid architectures, referred to as levels 0 through 5, that designers can use. Each aims at different performance and cost requirements.

Raid levels 2 and 4 are rarely implemented because the other schemes either perform better or are more cost effective. NCR has a simple primer on Raid concepts, "What Are Disk Arrays?," publication number ST-2116-73, that's available at no cost. For a copy, **CIRCLE 514**

Raid level	Title	Description
0	Data striping without parity (DSA)	Data is striped by system block size. • Drive spindles may be synchronized, but it's not required. • Independent data paths go to the drives. • The number of drives is scalable. • The number of drive groups is scalable.
1	Mirrored disk array (MDA)	Each block of data is duplicated on the mirror drive. • Drive spindles may be synchronized, but aren't required. • Independent data paths go to the drives. • The number of drives isn't scalable. • The number of groups is scalable.
2	Hamming code for error correction	Bit-interleaved data is transferred across a group of disks, and then enough check disks are added to supply single-error correction and double-error detection. (similar to DRAM ECC approaches). • Drive spindles may be synchronized, but aren't required. • Independent data paths go to the drives. • The number of drives isn't scalable. • The number of groups is scalable.
3	Parallel disk array (PDA)	An array of disk drives transferring data in parallel with one redundant drive that functions as a parity check disk. Together they work as one large virtual drive. • Parity is the Exclusive-OR of data on drives 1, 2, 3, and 4. • Drive spindles are synchronized. • Parallel data paths are supplied to each drive. • The number of data drives is expandable.
4	Independent disk array (IDA)	An array with the ability to read and write in individual drives within the array, but all data drives use a common parity drive. • Data is striped by system block size. • Parity is the Exclusive-OR of data across all drives. • Drive spindles may be synchronized, but it's not required. • Independent data paths go to each disk drive. • Both the number of drives and the number of drive groups are scalable.
5	Independent disk array (IDA)	An array of drives with the ability to read and write data and parity across all disks. No dedicated parity drive exists. • Data is striped by system block size. • Parity is the Exclusive-OR of data across all drives. • Drive spindles may be synchronized, but it's not required. • Independent data paths go to each drive. • Both the number of drives and the number of drive groups are scalable.

chronous option of SCSI-2, as well as both 8- and 16-bit cabling schemes. In addition, the 916 responds to the advanced commands included in the SCSI-2 standard, such as the multiple-byte command queuing and extended-message transfers.

On-chip logic also ties directly into the 932, the bus extender chip used in the large array configuration that expands the bus interface to 32 bits. Two data buses on the SCSI-2 chip—an 8-bit microprocessor interface and a 16-bit DMA channel bus—enable the chip to keep both ports simultaneously active to maximize data throughput. The dual ports also eliminate the need for off-chip bus-steering logic to route data between the microprocessor, the DMA channel, and the SCSI chip.



2. TWO CHIPS, the NCR 53C916 and 920, make building small Raid subsystems a more manageable task. With a CPU, RAM, control memory, SCSI ports, and a temporary data buffer, the chips reduce the additional logic needed. The controller can then reside on a board of less than 80 in.^{2}.

Complete with its own 1-kword by 32-bit ROM and 256-byte RAM, the on-chip controller that performs the command interpretation is a powerful state machine that the rest of the chip puts to work. An on-chip 24-bit transfer counter and the appropriate SCSI and DMA handshake signals handle large DMA transfers with minimal microprocessor intervention. The processor is only interrupted either when it detects a bus condition that requires servicing or when a programmable sequence or command sequence is completed. The chip has two degrees of user programmability—the command level and the instruction-sequence level.

At the command level, single commands are handled after they're written to the internal command register. The more-complex sequence level has the chip executing a sequence of commands that were previously downloaded. Downloading can be done by writing to the chip's sequence-execution-instruction-address register. This level of programming reduces bus overhead and protocol interrupt handling.

To handle all of the data movement between the multiple disk drives that make up the small Raid subsystem, the 53C920 does all data routing, data multiplexing/demultiplexing, and parity generation/checking. The chip also contains all of the logic required to handle data transfers between the DMA data bus of the host-side SCSI chip, the DMA data buses of the five other SCSI chips that connect to the disk drives, and an external buffer memory used for temporary storage. Each operation of the 920 is supervised and controlled by a local microprocessor that executes the control programs that instruct it how to implement any of the Raid levels.

One application that spurred the 920's and the 916's development was a 68020-based single-board array controller—the ADP-92. The board manages one rank of up to five disk drives and has an RS-232 serial port for local communication and diagnostics. Each drive is controlled by one of five 53C96 byte-wide SCSI controllers.

The board implements Raid 0, 1, 3, or 5 levels and provides a SCSI-2 10-Mbyte/s 8-bit interface, or a 20-Mbyte/s 16-bit interface, to the host system. Furthermore, an expanded version of the board can control multiple ranks of drives, each operating at a different Raid level. The ADP-92 disk-array controller board is sold by the company's Wichita, Kans.-based division for about $2500. That's about the same price as the previously introduced EISA-based integrated-drive-array controllers.□

PRICE AND AVAILABILTY

The first two chips to be released, the 16-bit 53C916 SCSI-2 controller and the 53C920 data-path manager, will sell for $93 and $89, respectively, both in 1000-unit quantities. Samples of both chips are available immediately. The five additional chips for the large Raid arrays won't have set prices until late second quarter when samples are to be released.

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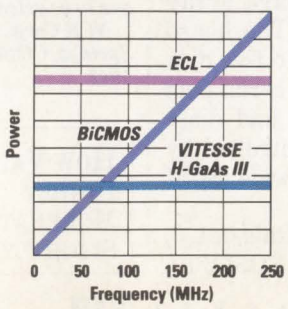

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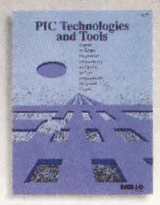

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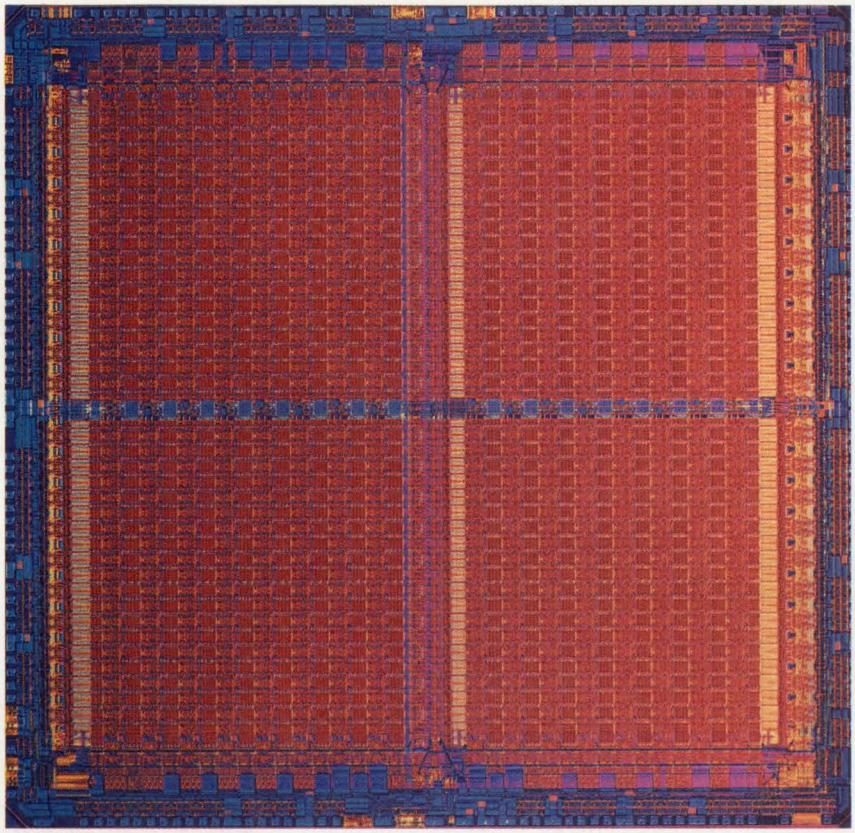


ACTEL CORP.

HIGH-DENSITY PROGRAMMABLE LOGIC TAKES ON GATE ARRAYS

DAVE BURSKY

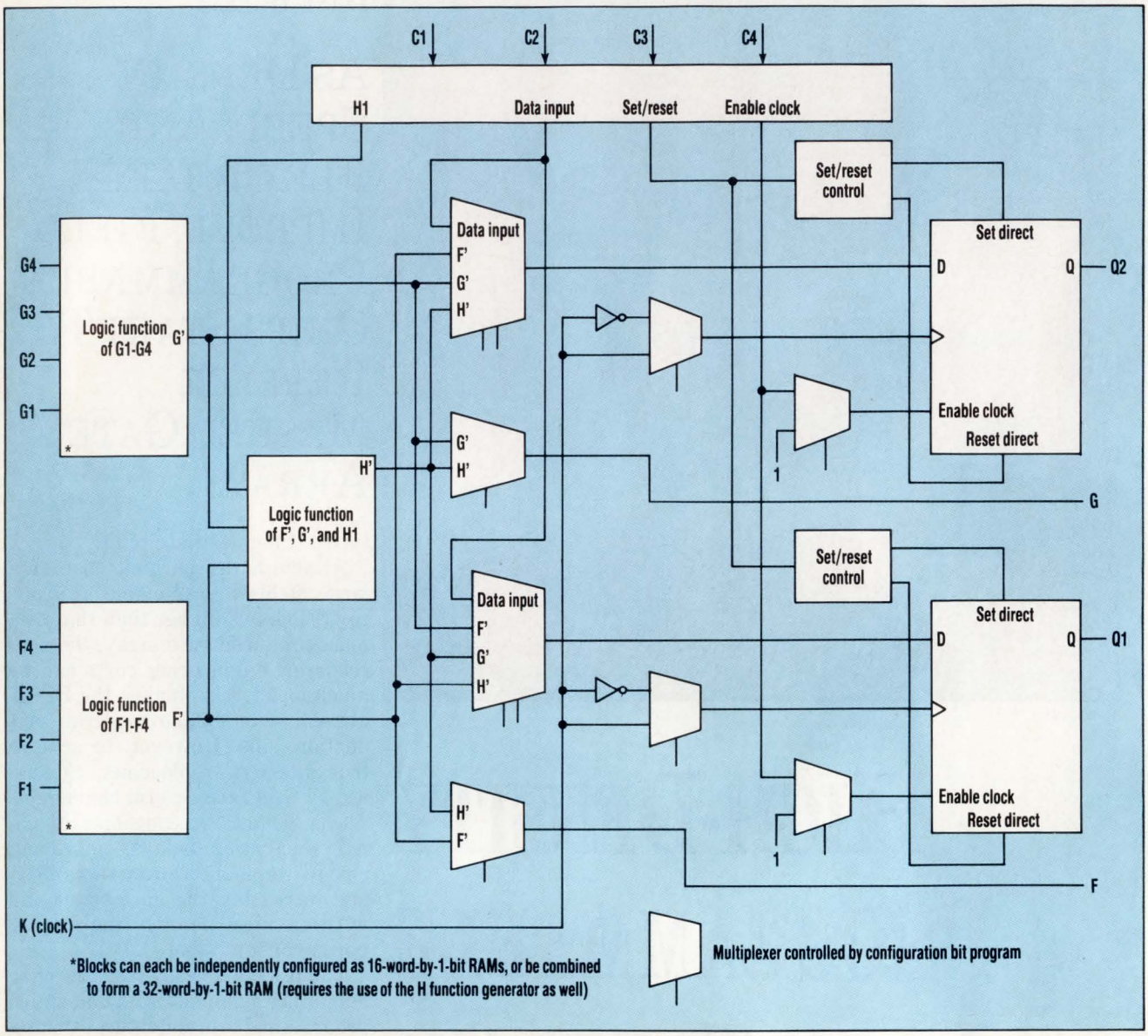
AS DENSITY, SPEED, AND FLEXIBILITY IMPROVE, FIELD-PROGRAMMABLE CHIPS START TO REPLACE MASKED GATE ARRAYS.

In the 15-plus years since the first field-programmable logic devices (PLDs) were introduced, densities have crept up from tens of gates to several thousand per chip. The flexibility of programmable logic chips has also increased. Today's large field-programmable chips now vie with low-end (sub-10,000-gate) mask-programmable gate arrays by offering designers the ability to almost instantly create a functional prototype of their desired circuit.

Although the per-unit cost of a large field-programmable gate array (FPGA) is higher than that of a mass-produced gate array, the nonrecurring-engineering costs can be much lower. This makes the FPGA attractive for small to moderate production runs. However, to achieve true gate-array replacement capability, FPGAs face several challenges. These include reducing on-chip signal-propagation delays, improving circuit implementation flexibility, and increasing the gate count—all without significantly increasing power consumption.

Though not an easy task, the challenges are being met with innovative programmable architectures that reduce the delays while offering more flexible interconnections. Help also comes from finer-line processes—smaller device features reduce the gate delays. That increases the maximum operating speed and allows more gates per chip. Reduced device sizes also enables transistors to be positioned closer together. As a result, losses caused by parasitic elements are cut down, translating into lower power consumption.

One particularly difficult issue involves defining exactly what an FPGA is. No standard definition exists, but several points can be used as guidelines. First, the circuit should allow multiple levels of logic to be interconnected through programmable-interconnection elements without using an I/O pin. Second, it should have a defined propagation delay through each level. And third, it



1. MORE INPUTS ARE AVAILABLE on the enhanced configurable logic block of Xilinx's XC4000 series of programmable arrays than on the CLBs of Xilinx's previous family. The series includes dedicated carry logic to improve arithmetic operations.

should have a reasonably large number of available equivalent gates (over 1500 gates is a well-accepted rating that moves a chip's classification from a PAL device or a simple PLD to an FPGA).

A noticeable FPGA trend is the virtual complete shift away from bipolar technology as densities increase. Advanced CMOS processes with submicron features now dominate the high-density programmable-device arena. The FPGA field is also dominated by California-based startup companies—firms less than six years old, with most not even owning their own processing facilities. But that won't stop engineers from adopting FPGAs. Presently, only about 8% of engineers using programmable logic currently employ FPGA-complexity devices. However, a recently released ASIC study by Electronic Trend Publications, Saratoga, Calif., projects that FPGAs will account for 25% of all programmable-logic sales by 1993.

The more programmable devices resemble a gate array, the more designers must depend on good software tools. These tools must hide chip architectures from system designers and allow them to work at the macrocell level. Only the desired functions from the cell library would need to be chosen. In addition, as more of the system is built from FPGAs, simulation models and delay-extraction tools will be increasingly counted on to verify system operation and performance prior to hardware implementation *(see "Software tools are crucial," p. 48).*

None of the early large PLD manufacturers could develop the innovative circuits needed to stay at the

forefront of density. Texas Instruments, for example, licensed both the Altera and Actel field-programmable logic structures to gain a foothold in the complex PLD market. TI also has rights to use the Actel technology in other product areas not yet disclosed. Intel also licensed some of the Altera devices, but has recently focused attention on more application-focused programmable devices aimed at specific system problems.

To some extent, Advanced Micro Devices also bought its way into the market by first acquiring Monolithic Memories Inc. MMI, the original patent holder for PAL devices, had also invested in and licensed the Xilinx RAM-based logic-cell-array (LCA) programmable architecture. Although AMD is still an investor in Xilinx, it has refocused its strategy by phasing out sales of the LCA devices while developing proprietary mid-range-complexity chips based on EEPROM elements—the Mach family.

Until this month, National Semiconductor has been a player only in low-complexity and high-speed PLDs. However, this week, National unveiled a mid-range family based on a multiple-array programmable logic (MAPL) architecture. The family is also based on EEPROM configuration cells and will compete with the Mach family as well as PLDs from Cypress Semiconductor, Exel, Philips-Signetics, and Plus Logic. It will also vie with the lower-complexity family members from Actel, Altera, and Xilinx.

The fuse-programming technique for PLDs has moved from the metal-link-style fuse to RAM, EPROM, EEPROM, and even antifuse-type control cells for all of the CMOS logic chips. In the case of RAM, EPROM, and EEPROM cells, chips using them can be erased and rewritten to reconfigure the chip in the prototype system or even once the end equipment is fielded (RAM and EEPROM-based units predominantly).

So far, Xilinx and Plessey, a newcomer to the market, are the only companies using configurable logic based on static-RAM storage cells that hold array configuration data. Xilinx, though, has lined up AT&T Microelectronics and Seiko-Epson as alternate sources for its XC2000, XC3000, and recently released XC4000 families. The arrays find many applications, whether as a prototyping aid due to their in-system reprogrammability and internal observability, or as a production device for low-to-medium-volume end products (several hundred to tens-of-thousands of units per year).

The Xilinx families are popular because they can implement significant blocks of logic, and because their in-system reconfigurability enables one chip to perform multiple functions or have its logic updated. An informal survey of computer-board makers at this year's Buscon revealed that many manufacturers use one or more Xilinx arrays on their production-version boards. The chips are used to implement secondary bus controllers and specialized interface logic.

Xilinx recently released its third generation, the XC4000 series, which will offer better flexibility, more features, and higher performance. Improved flexibility comes from additional routing resources and an enhanced logic-cell architecture that allows more functions in each cell. Also, the RAM configuration cells can be used as standard memory cells. The inefficient implementation of registers and small blocks of RAM was a major complaint with the XC2000 and XC3000 families. Members in the 3000 family offer complexities from 2000 up to 9000 gates and 64 to 82 I/O lines, depending on the package.

With improvements in array connectivity and the use of a submicron process (instead of the 1.2-μm process that manufactured the previous families), the XC4000 series can offer higher operating speeds—as much as 33% over the XC3000 family. The smaller features also enable designers to pack more equivalent gates on a chip; XC4000 devices range in complexity from 2000 to 20,000 gates per chip. The first XC4000 devices to be sampled range from 5000 to 10,000 gates.

External system clock speeds with the 4000 series can run as high as 60 to 70 MHz. Internal logic functions also operate faster. For some simple functions, such as a 16-bit multiplexer, a 16-bit synchronous counter, and an 8- or 9-bit parity generator/checker, the XC4000 family requires 20 ns with 8 configurable logic blocks (CLBs), 20 ns and 5 CLBs, and 5 ns with one CLB, respectively. In comparison, the XC3000 arrays require 35 ns and 14 CLBs, 28 ns and 7 CLBs, and 14 ns and 2 CLBs, respectively.

The basic CLB on the chip has been restructured to add more inputs (9 vs. 5 in the XC3000 series), as well as to include carry logic to improve circuit performance for adders and other ALU operations *(Fig. 1)*. With the enhanced block, wide and fast decoders can also be created thanks to some dedicated decoding logic added to the matrix. Furthermore, the 4000-series architecture permits the 16 configuration-bit storage locations in each CLB to be used as RAM. At the same time, the combinatorial function generators can perform a different, perhaps unrelated job. Depending on the total array size, blocks of RAM ranging in size from 2 to 28 kbytes can be formed.

Unlike the CLB programming level of the Xilinx arrays, Plessey's electrically reconfigurable array (ERA) offers a much finer level of granularity. In the ERA, the basic programmable element is a NAND gate, similar to the basic element in a mask-programmed gate array. Such a fine level of granularity is both a blessing and a curse to the designer. It's great if custom logic down to that level must be implemented. But for more standard logic, it depends heavily on a comprehensive macrocell library of more complex logic functions to eliminate repetitive design tasks.

The gate-level granularity is also somewhat slow. Because each level of gating incurs a fixed propagation delay, designers must minimize the number of levels. With more complex logic cells, some of the gate levels are already precombined in the macrofunction to improve circuit performance. Thus, the longer propagation delays in finer-granularity circuits may limit the frequency to a level below that of some of the ma-

SOFTWARE TOOLS ARE CRUCIAL

For the complex field-programmable gate array to be on a par with the masked gate array when designing, then the tools that capture and verify the design must be as good as those tools used for masked arrays. Such tool improvements are starting to emerge as programmable chip makers feel they must hide the actual array architecture.

Submerging chip architectures is actually a result of increased chip complexity. Increased internal logic, which gives programmable arrays their flexibility, makes it harder and harder for system designers to really understand the intimate details of every array family. Consequently, by submerging the architecture's details into the tools, the software supplier lets users concentrate on their design rather than the low-level implementation. However, that puts a strong onus on the tools to offer the most advanced features and capabilities to maximize the use of the unique architectures of each array.

Most silicon suppliers first offered their tools on PC-type platforms, because initial architectures weren't very complex and the horsepower of 80286- and 80386-based PCs could handle the placement and routing. However, as complexities increased, the PC no longer had processing overhead to spare. As a result, the more powerful desktop workstations have become a prime target for the new FPGA design tools.

For the designer to verify system operation, the tools will have to analyze how best to fit a design into the available logic, and perhaps perform logic reduction and optimization, post-placement delay extraction, and back-annotation of the propagation delay figures. Some of the tools are even starting to link into logic-synthesis software, so that portions of the desired circuit can be derived from a logic description, rather than from a schematic.

In addition to software tools offered by the FPGA vendors, simulation models for many chips are available from Logic Automation Inc., Beaverton, Ore. Full design suites of tools, such as the Amadeus PLD package, are available from Cadence Design Systems Inc., San Jose, Calif.; other tools come from Mentor Corp., Beaverton, Ore. With the Cadence Amadeus PLD package, engineers can create a design with schematics, or hardware-description languages. They can also use Boolean, truth-table, or state-machine syntax descriptions in Abel 4.0, the popular PLD design language from Data I/O Corp., Redmond, Wash. The design-entry portion of the software is linked with Cadence's Improvisor, a design-synthesis tool that allows designers to explore implementation alternatives early in the design cycle.

With simulation models available, designers not only evaluate the operation of a chip, but of an entire board or system. The cost of an FGPA—$20 to $30 on the low end and close to $200 on the high end—is much lower than that of the engineering and mask charges for a gate array. But no one wants to go through several iterations of a design, throwing away a few hundred dollars each time. Simulation can avoid the iterations, as well as possibly catch design inconsistencies in the rest of the system.

One unique option that Logic Automation has for its models is a windowing capability that allows designers to "look" inside the registers of an FPGA during simulation. Breakpoints can be set on particular data patterns, execution can be single-stepped, and register values altered—all to quickly identify and correct design problems. The windows feature is especially helpful with ICs that have many buried registers.

crocell-based chips. Depending on the number of speed-critical paths within the chip, the finer-grained circuits may not be fast enough.

The Actel ACT-1 and ACT-2 families of one-time programmable arrays, which compete for some of the same applications, may offer an even higher degree of configurability than the Xilinx products. However, configurability comes at the expense of reprogrammability. The reason is they employ one-time programmable antifuse elements that form small, short-circuit paths to configure the chip. One major benefit of the antifuse technology is its "hardness" to radiation, which makes the arrays promising candidates for many military and satellite systems.

Initially fabricated with a 2-μm process, the ACT-1 arrays offer the equivalent of 1200 and 2000 gates (for the A1010 and A1020, respectively). However, designers at Actel feel that the technology is on the early edges of the scaling curve, with plenty of room for feature reduction. The newly released ACT-2 family illustrates that point by trimming the features to 1.2 μm and upping the gate count to 2500, 4000, or 8000 on the A1225, 1240, and 1280, respectively. The largest chip, the A1280, comes in a 176-lead pin-grid array. In small quantities, it sells for $440 each. Such a high pin count is essential for the chips to be used in many of the latest digital systems.

The gate-array-like architecture of the ACT-2 series makes it possible for the chips to implement large macros easily and achieve moderate performance levels. A 16-bit loadable binary counter can run at 40 MHz, a 16-bit binary adder requires 20 ns, and a 32-bit version needs 30 ns. Those numbers are worst-case specifications over temperature and voltage variations. The chips still use rather large feature sizes, compared with the submicron-process features of some EEPROM- and EPROM-based programmable logic devices. Actel, though, is confident that chips performing 50 to 150% faster than today's will be possible, as feature sizes drop to 0.8 μm.

Competing with the RAM and anti-

fuse arrays are the UV EPROM-based programmable logic chips that are part of the Altera Max and EP families and in part, alternate-sourced by Cypress, Intel, and TI.

The Max 5000 series architecture consists of multiple programmable logic blocks on one chip that can be tied to each other through both local and global programmable connections. Each logic-array block (LAB) consists of a macrocell array containing 16 macrocells, an expander product-term array, and an I/O control block *(Fig. 2)*. Each macrocell, in turn, consists of a programmable logic array and an independently configurable register that can be set as a D, T, J-K, or S-R flip-flop, a flow-through latch, or bypassed for purely combinatorial operation. Each LAB has one system clock input.

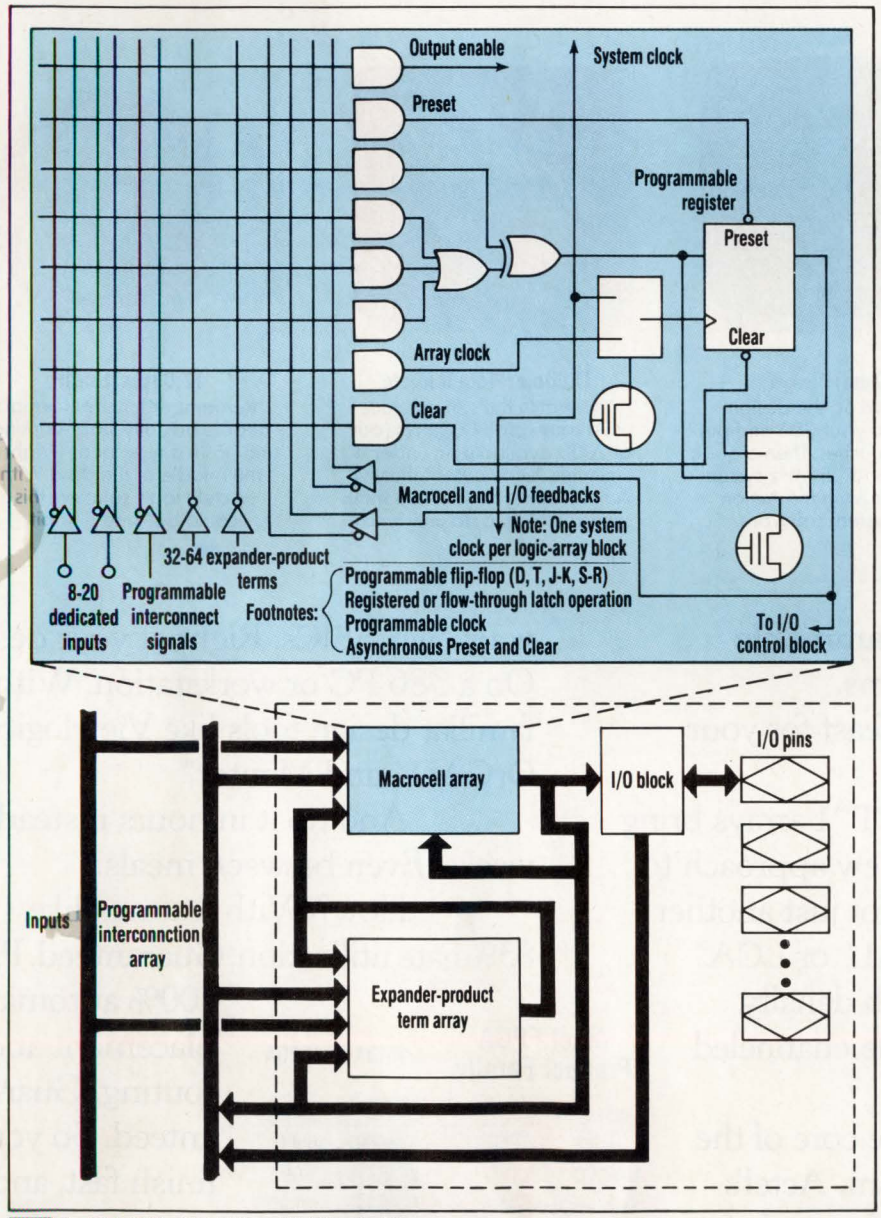
That architecture differs markedly from the Actel and Xilinx approaches, and somewhat resembles a chip built from multiple, independent PAL devices. The largest Max-family member is the recently released EPM5192, which packs 12 LABs and comes in either a 100- or 84-lead package. However, designers at Altera also noted the need for a high-pin-count chip without as much logic. Along came the EPM5130, which packs only 8 LABs but comes in a 128-lead package. The 5192 has about 7500 gates, while the smallest member, the 5016, contains the equivalent of about 600 gates. Counters formed on the arrays have a top speed of about 40 MHz on the 5192, and 100 MHz on the 5016.

Of course, one problem when evaluating the chips in real systems is that loading conditions are rarely perfect, and direct signal paths don't justify employing a complex device. If other elements, such as using the expander terms, are considered, system performance will degrade by as much as 50%. These performance changes might be avoided if designers are totally familiar with an architecture, or have some software tools that can avoid such situations automatically *(see "Sidestepping architectural curves," p. 53)*.

Designers at Altera are working on a second-generation Max family that will offer complexities of up to about 20,000 gates and pin counts of up to 208 pins. Although full details won't be available for a while, some preliminary data is included in the company's 1991 product catalog.

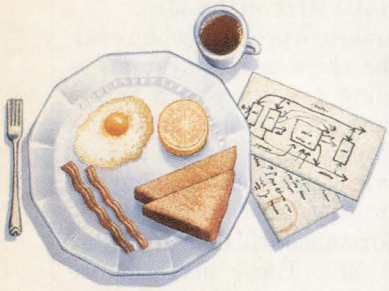
Licensed alternate sources for both the Max and older EP logic families—Cypress, Intel and Texas Instruments—offer exact replacement devices. Both Cypress and Intel, however, also developed proprietary programmable chips based on UV-EPROM technology. The CY7C3xx family from Cypress focuses on various aspects of bus interfacing and is architecturally more like PAL-type devices than FPGAs. Intel's most recent devices are also relatively low-complexity chips, but they run fast and aim at applications in which power is a key issue: They consume about one-tenth the power of most equivalent-complexity devices.

One relative newcomer to the EPROM-based logic market, Plus

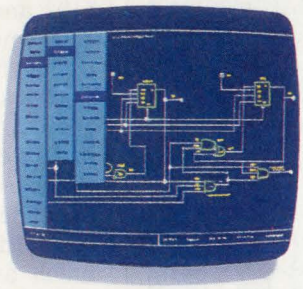


2. EACH OF THE MAX 5000 series chips from Altera has 1 to 12 logic-array blocks. Each block in turn contains 16 programmable macrocells. Altera connects the LABs with both local and global routing. The local routing makes it possible for the localized functions to be routed without going through the main interconnection matrix.

Be Brilliant At In Productio

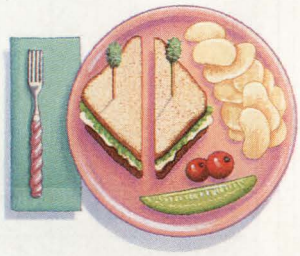


7:05 am : Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am : Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am : Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm : Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

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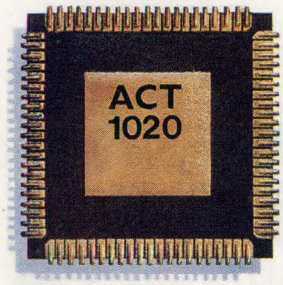
And do it in hours instead of weeks. Even between meals.

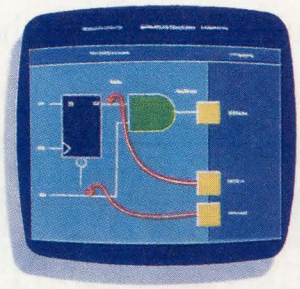
How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most

Actel FPGA Product Family		1010A	1020A
Equivalent Gates	Gate Array	1200	2000
	PLD/LCA	3000	6000
User I/O		57	69
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

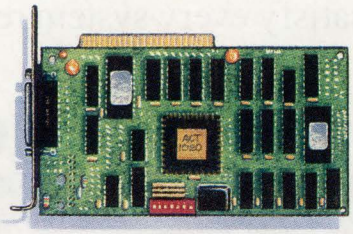
Breakfast And n By Dinner.



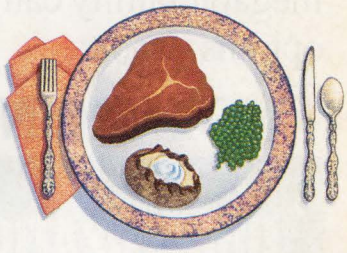
1:15 pm: Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a very quick coffee break while your design becomes a reality.



1:25 pm: Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



4:00 pm: Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished way ahead of schedule! Better think of something to do until 5:00.



6:00 pm: Dinner
Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

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Design verification is quick and easy with our Actionprobe™ diagnostic tools, for 100% observability of internal logic signals. Guaranteed. So you don't have to give up testability for convenience.

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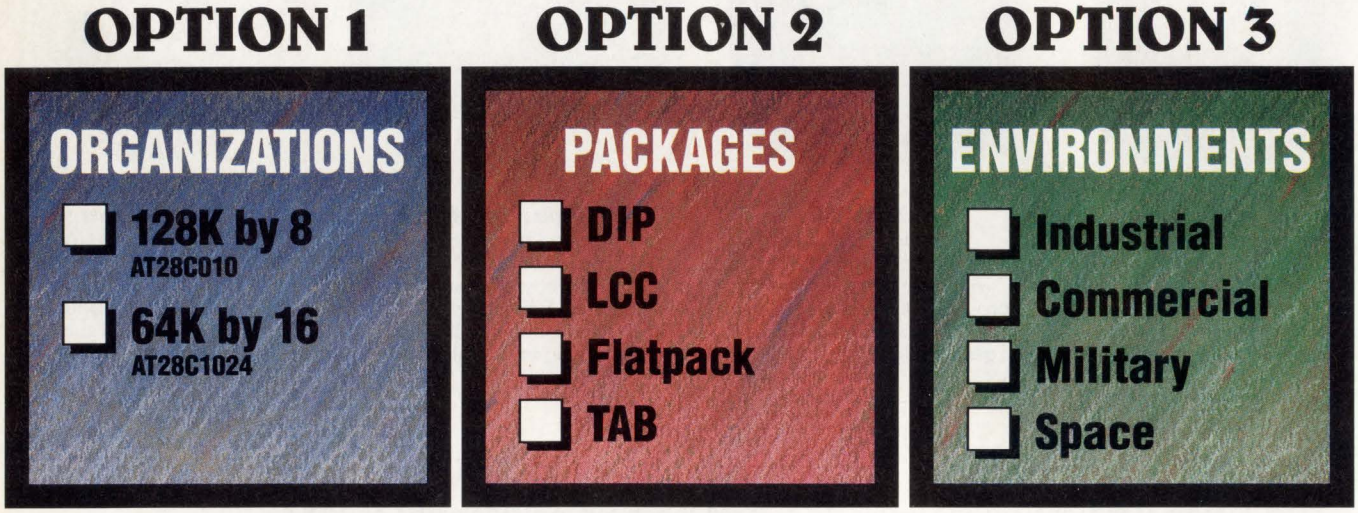

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SIDESTEPPING ARCHITECTURAL CURVES

The once simple architecture of programmable-logic devices has been radically transformed over the past few years into a wide range of complex-architecture variations. Such complex-device families as Altera Corp.'s Max family or similar chips increase the logic capacity to gate-array proportions. But always tagging along are numerous unusual traits or peculiarities that designers must know about to unleash a device's full performance.

Unfortunately, with such a proliferation of devices on the market, it's become more difficult for designers to understand the details of device architectures—especially those with obscure but important features. As a result, advanced fitter software is emerging as an aid designers can use to take advantage of obscure or little-exploited features.

The more common peculiarities found in the three broad device-architecture categories relate to partitioning, expansion of terms, and product-term steering. A number of available and popular devices can personify these traits.

One of those three device categories, a partitioned architecture, consists of one large logic array that's divided into multiple programmable sub-arrays. Those sub-arrays resemble smaller PLDs, and are interconnected through local and global buses. Altera's EP1800, for instance, has four quadrants, and each quadrant has eight local and four global macrocells. Local macrocells feed back only into their own quadrant. Global macrocells, though, have feedback paths onto a global bus, and thus into other quadrants. However, their pin feedback is global while their register feedback is local.

Global feedback, in a limited amount, forces the designer or the fitter software to partition logic between quadrants wisely to maximize the utility of the global paths. If a design is incorrectly partitioned and has too much communication between quadrants, the global feedback will be exhausted and the logic won't fit.

Another aspect to watch carefully with the EP1800 is the source of global feedback—it's not the macrocell's registered output, but rather its pin output. Because the pin is fed by a three-statable buffer, the feedback won't work as expected unless the buffer's three-state control is permanently enabled.

A third peculiarity of the EP1800 is its clocking. Usually, a macrocell's flip-flop can be clocked by either a synchronous, quadrant-wide clock, or if necessary, by a gated product term. However, if a product term is needed to control the macrocell's output enable, only the synchronous clock is available; term clocking is no longer an option.

Macrocells in Altera's MAX devices, such as the EPM5128, are a good example of using expander terms. Each macrocell has a limited number of product terms available. If they're inadequate in a particular instance, the expander capabilities can increase the number of available terms. But the expansion bus is effectively fed by NAND gates, which implies that the incoming terms must be transformed to maintain their functionality before being used. This may involve more than complementing the logic. An entire, second reduction pass may be necessary to best utilize the expansion capability.

In addition, the EPM5128's expansion bus is shared between macrocells, which means that shared product terms are the best candidates for expansion. Placing singly used terms on the bus is a waste of silicon resources.

Product-term steering, the last of the three categories, shows up in devices like Atmel's 2500 and Intel's 5AC312. There are two versions of steering: term joining and term sharing. The AT2500 exemplifies joining. Each macrocell has 12 product terms available to it. In the simplest configuration, four feed the combinatorial output, four feed one buried register, and four feed a second buried register. However, if required, the combinatorial output can "grab" some or all of the 12 terms to extend its capabilities.

The peculiarity is that the buried registers can still be used, even if the combinatorial output has accessed extra terms, as long as the register's equation is a subset of the combinatorial equation. If not, the register is wasted.

Product term sharing is similar to joining. In this case, however, increasing the number of product term inputs to a macrocell is done by having the macrocell borrow logic from its neighbors. An example is Intel's 5AC312, which packs three adjacent macrocells, each containing two groups of four product terms.

The uniqueness or peculiarity is that each macrocell (A, B, or C) can either give up a group of four product terms or borrow a group from each adjacent macrocell. For example, say A and C each needs 12 product terms for their equations. Each then takes a set of four terms from B, leaving B unusable because it has no more product terms.

One thread runs through all of these peculiarities: If not properly understood and accounted for, the devices that employ them can't be utilized efficiently. The penalties are wasted effort, wasted silicon, and wasted board space. The onus is on the designer, or a smart piece of software, to understand the oddities and make the proper trade-offs that result in efficient utilization.

This information is provided by Steve Kaufer, project engineering manager at Data I/O Corp., Redmond, Wash.

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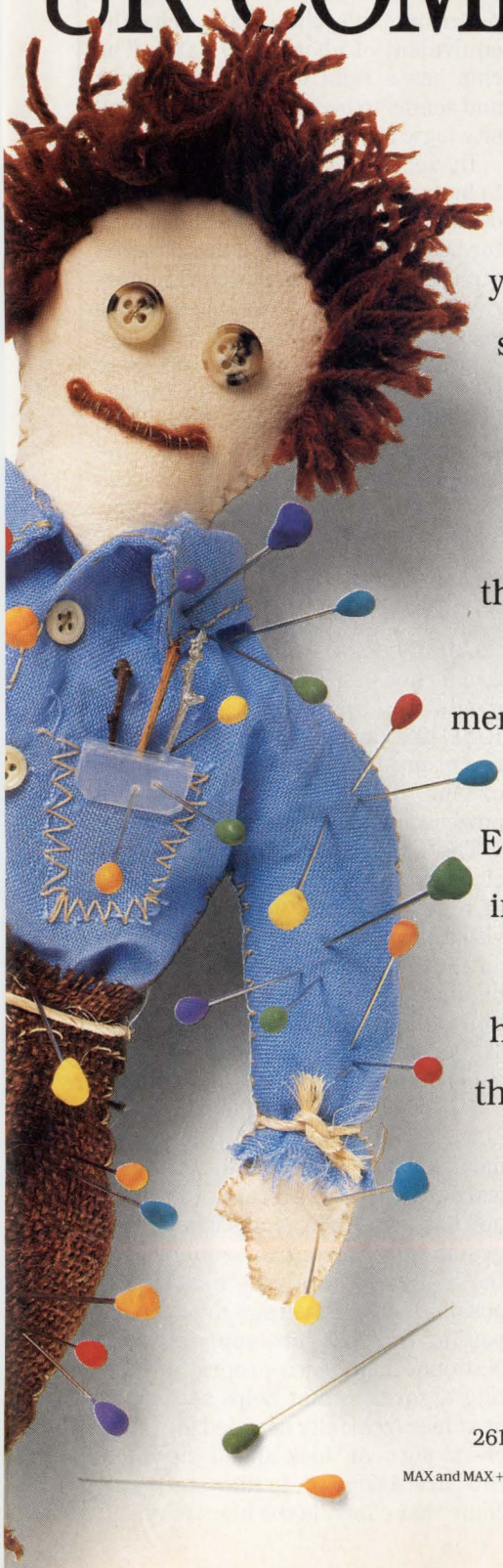

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CIRCLE 88

Logic, has developed a family of three programmable arrays in its FPGA2000 series with equivalent complexities of 2000, 4000, and 8000 gates in packages with 40 to 144 leads. Based on a 1.5-μm CMOS process, the chips' architecture is very similar to that employed by Altera—function blocks containing the programmable logic cells surround a universal interconnection matrix. However, unlike the Altera parts, the I/O cells come in two parts—the first section is associated with each function block, and the second portion is part of a common I/O pool on either side of the interconnection matrix that the function blocks tie into. Currently, only the mid-density chip is in production, but the smaller family member will be available next quarter and the largest should be sampled near the end of the year.

In addition to the general-purpose logic chips, Plus Logic has come up with a special array version with an on-board 1152-bit configurable register, the FPSL5110. The company plans to officially release the chip next quarter. The register contains 32 words of storage, each word 36-bits wide. The configuration logic allows the register to be set up as either a dual-port RAM or a FIFO register (uni- or bidirectional).

Unique among the programmable logic chips, this data buffer chip will contain the equivalent of the 2000-gate FPGA2000 in addition to the register. It's about the same complexity as the forthcoming RAM-based Xilinx XC4005, but occupies about 1/4 the chip area. Operating at 40 MHz, the chip can be set to work as a rate buffer between systems operating at dissimilar speeds, or as a mailbox conveying control information between two systems.

Moving its bipolar programmable macro logic architecture into CMOS EPROM technology, Philips-Signetics will soon release the PML2552, a 68-lead chip with 29 dedicated inputs and 24 I/O lines. Internal flip-flops can toggle at 50 MHz while the internal NAND logic paths have a propagation delay of 12 ns/level.

Employing a folded-NAND structure, the array permits 100% connectivity, eliminating routing restrictions. In addition, the chip contains 52 dedicated flip-flops—16 input D-types, 20 internal J-Ks, and 16 output D-types. Multiple, dedicated clock inputs enable the circuit to be partitioned into multiple subcircuits that can operate independent of each other. To improve the multilevel logic capability, 96 NAND foldback gates are included on the chip.

Atmel is also pushing up the density of its EPROM-based logic with a programmable chip that packs the equivalent of about 2500 gates. The chip has a relatively low pin count and seems to be targeted at mid-density logic replacement.

By applying EEPROM technology to high-density programmable logic, designers at National Semiconductor have come up with a novel paged architecture that allows the logic array to maintain its best speed across a wide range of densities. Chips range from the first 28-pin 1000-gate ICs released this month, to the 68-lead, 4000-gate chips slated for 1992. The paged architecture allows the arrays to run at system speeds of 45 to 50 MHz (with feedback) without submicron processing. The first arrays employ 1.4-μm design rules.

The MAPL architecture is optimized for state-machine applications. It banks on the fact that the circuit doesn't require all logic elements at the same time. That allows RISC-like design approaches to the use of product terms. Only a subset of the product terms must be powered on at any one time.

The 128 product terms in the first chips are broken down into 8 pages of 16 terms each. Full interconnectivity allows any input to be routed to any output through any programmable array—with the same propagation delay, regardless of the path. The consistent delay makes overall chip performance more predictable.

The hierarchical scheme creates a new critical path. Unlike a logic signal delay path in other chips, the critical path is the time it takes to power-on and power-off various levels. Programming the control sequence for the hierarchy would be next to impossible for the average user. So, as part of the software support tools, National included a proprietary fitting algorithm that helps set up the next hierarchically decoded logic level—a sort of look-ahead decoder. Bits are assigned to the state machine that controls the hierarchy and

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This is intended to be a guide rather than a definitive list.

act as decoding tags to determine the level that's activated.

The first series of chips in the MAPL family—the MAPL128 and 144—will be targeted at synchronous state-machine applications. They come in 28- and 44-lead packages, respectively. Both D and J-K flip-flops are included as part of the hardware resources, minimizing the need for software transformations or additional product terms to implement such flip-flops.

Going head-to-head with National's new family, the Mach series from Advanced Micro Devices claims to merge the best of PLDs with the best of FPGAs. The first family of Mach chips, the Mach 110 series, aims at general-purpose logic-replacement applications; the 210 series, which packs embedded flip-flops, is more suitable for state-machine applications (ELECTRONIC DESIGN, *March 8, 1990, p. 105)*. The chips have internal 15-ns propagation delays and can handle system clocks at rates of up to 50 MHz.

The first members of each series are now available. The larger 84-pin Mach 130 and 230 are slated for release next quarter; the mid-size 68-pin Mach 120 and 220 are scheduled for third-quarter release. AMD has also developed a mask-programmable replacement for the Mach chips that allows a customer to move to a lower cost for production. The company estimates that quantities of as few as 15,000 units would permit them to use a masked version.

Both Lattice Semiconductor and International CMOS Technology also have EEPROM-based programmable logic chips with the GAL6001 and the PEEL family, respectively. But their largest available chips only marginally fall into the large PLD area, and are equivalent to about 1200 gates. New things are afoot at Lattice that push densities up into the FPGA area, but the company is keeping mum until later this year.□

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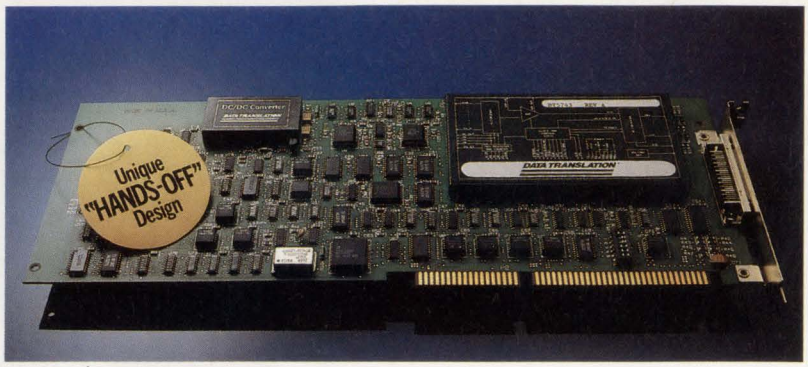

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EASILY UPGRADE A 68030-BASED SYSTEM WITH A CLEVER CACHE DESIGN

BUILD A CACHE DAUGHTERBOARD THAT PLUGS INTO THE EXISTING PROCESSOR SOCKET TO EXPLOIT THE PROCESSOR'S SYNCHRONOUS MODE.

Companies spend lots of time and resources creating a microprocessor-based product. By the time the product is ready for the market, however, the industry has already introduced a faster or more advanced processor. Selling yesterday's technology is difficult, yet it's not profitable to sacrifice the existing system and develop another product that uses the updated technology. The ideal solution is to bring the updated technology to the existing system without major changes.

For instance, a 68030-based system that uses dynamic RAM (DRAM) runs at 3 clock cycles/access in the asynchronous mode. The system doesn't take advantage of the processor's synchronous operation, which runs at 2 clock cycles/access at 33 MHz. Adding cache memory to the existing system would convert a large number of the slow DRAM accesses to fast accesses in the cache static RAM (SRAM). A high ratio of SRAM accesses to DRAM accesses indicates better performance.

A cache can be built on a daughterboard that plugs into the system's existing processor socket. That way, designers can upgrade an outdated microprocessor-based system without changing its architecture. The cache system is a small subsystem that uses fast SRAM and cache technology. With that technology, the processor can run at it's maximum speed. The cost of developing this small, add-in daughterboard is minimal compared to the cost and the time it takes to rebuild another system. This cache system can upgrade an application's speed up to 30%.

The operation of cache is based on the principle of program locality. Programs usually access the same memory blocks repeatedly. In addition, they spend much time executing instructions in a loop. DRAM is used for main memory and SRAM for the cache. Accesses to SRAM are fast and don't need wait states. When the program reads data or instructions from the slower DRAM memory, the processor writes the surrounding block of data into the cache. Subsequently, the next access to the same information comes from the cache memory with no wait states.

There are drawbacks, however. The data that the microprocessor needs may not always be in the cache memory. When the program attempts to find data in the cache, the system will indicate if the desired data is stored there. This is done with

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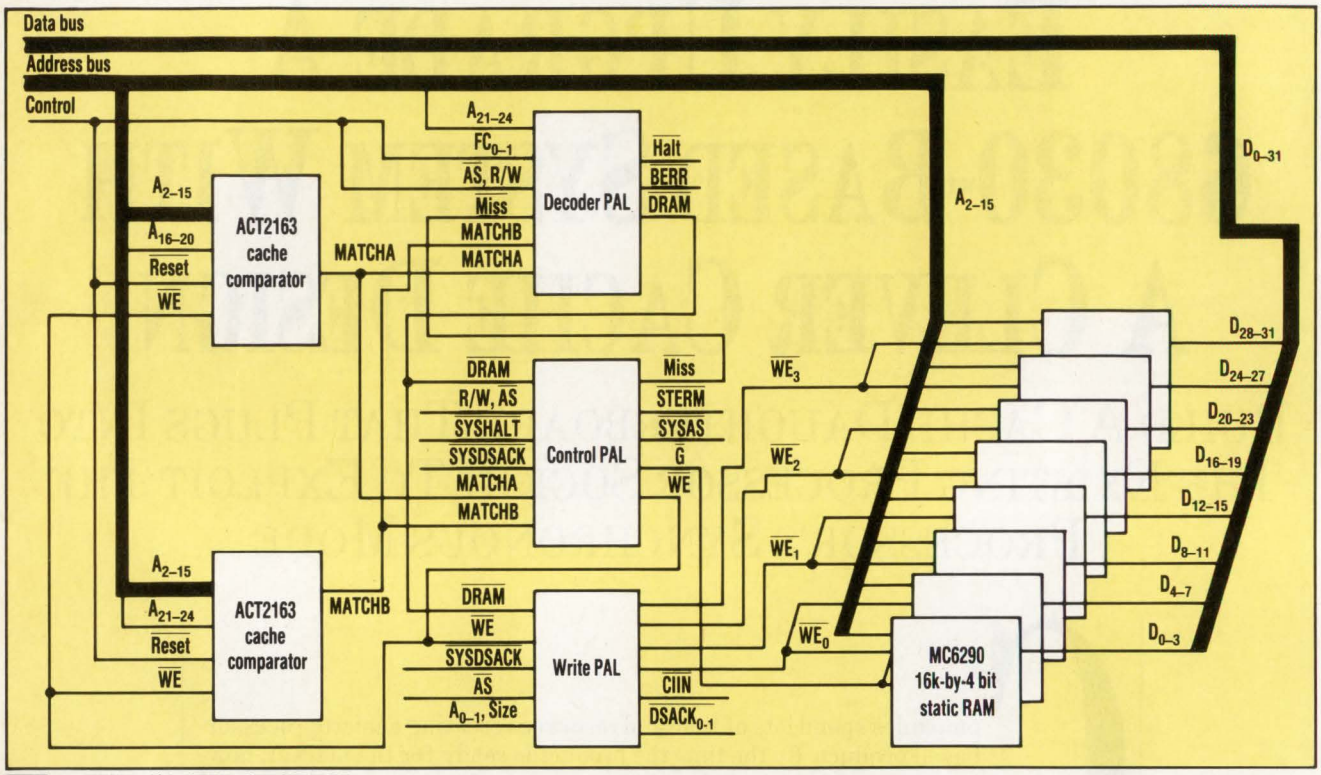


1. THE CACHE SYSTEM is made up of eight Motorola SRAM chips, three PAL devices, and two Texas Instruments tag comparators.

the cache tag comparator, which compares the current address being accessed by the processor to the addresses of data stored in SRAM and determines if they match.

A cache hit occurs when a match is found. In that case, the memory location needed by the program is already in the cache (SRAM), so the cache can give the required information to the processor without delay. A cache miss occurs when there's no match, and the processor has to fetch data from the main memory (DRAM) and update the cache.

A Tricky Task

Designing the add-in cache system is tricky because it can't alter the existing system, but instead must work around it. This cache has unique features that optimize the overall system performance. For example, the design interleaves DRAM and SRAM accesses. Interleaving memory accesses reduces the penalty of a cache miss. In addition, the cache controller hides the dynamic RAM refresh in static RAM and peripheral accesses.

The daughterboard uses a simple direct-mapped cache that's made from 64 kbytes of fast static memory. Direct-mapped design offers simplicity and uses the least amount of tag memory. The main memory (DRAM on the system board) is divided into logical pages. Each page of DRAM is the same size as the cache.

The total number of the DRAM pages is calculated by dividing the DRAM size by the size of the SRAM. In this 68030-based system, 8 Mbytes of DRAM and 64 kbytes of SRAM exist. The number of pages is $8000 \div 64 = 128$ pages.

Each page is directly mapped to the 64-kbyte SRAM space. A page consists of 16k 4-byte lines. The address space A_{2-15} covers the 16k lines needed for each page.

Tag memory, which is the fast SRAM part of the tag comparator, stores the tag of each line. The tag is the page number that's unique for each line. In this system, the tag takes a value of 0 to 127 for the total of 128 pages. When the processor stores any information into the SRAM, the cache controller stores the line tag into the tag memory. The tag memory is 16k by 7 bits, and is mapped directly into the SRAM space A_{2-15}. Seven bits are needed to store 128 tags.

When the processor starts an access, the tag comparator reads the stored tag data for this location. It compares the tag data with the current accessed address (A_{16-22}) and indicates a hit if they match. Address lines A_{16-22} select one page of the 128 pages.

The cache is made up of eight 15-ns, 16k-by-4-bit Motorola MC6290 SRAM chips *(Fig. 1)*. Each page is organized as 16k 32-bit words. Address signals A_{0-1} are used to decode 4 bytes of the cache line, while A_{2-15} create the 16k words of address space.

This design uses two Texas Instruments ACT2163 16k-by-5-bit, 20-ns tag comparators. Address lines A_{2-15} are connected to both of the tag comparators and the SRAM address bus. Also, A_{16-20} and A_{21-24} are connected to the data inputs of the two cache tag comparators to store the page

number.

MATCHA and MATCHB are the output signals of the tag comparators. These signals go high on a compare cycle if the current processor address A_{2-24} matches a previously stored tag. Address tags are stored each time the processor writes to the cache.

The DRAM controller used in the existing system supports three modes. A standard DRAM page-mode access requires a precharge time delay before the controller accesses a new row and column. This access takes 7 clock cycles at 33 MHz and is the slowest mode. Fast page mode is used if the controller accesses a new column in the same row. This is the fastest access, taking only 3 clock cycles. Interleaving mode is used when the controller finds an access in a different row and that row is precharged. It takes only 5 clock cycles/access in this mode.

Different Modes

The old non-cache system runs at an average speed of about 5 cycles/access with the DRAM memory. The three different modes that the controller uses with the DRAM in the old system will average 5 clock cycles/access. This average access time is calculated as $(3 + 5 + 7) \div 3 = 5$, assuming that each mode has an equal chance to occur.

In the new system, when the cache controller misses, the processor has to get the information from the DRAM main memory. On a cache miss, the cache controller adds two more clock cycles to the DRAM access because it enters the retry mode of the 68030. The retry mode is used because the 68030 samples the Synchronous Termination signal $\overline{\text{STERM}}$ before a valid result of the miss or hit signal. The total average access time in a miss is $5 + 2 = 7$ clock cycles/access.

With a cache hit, the system can run at 2 clock cycles/access. This design gives an average hit/miss ratio of about 85%. The average read access time becomes $(2 \times 0.85) + (7 \times 0.15) = 2.75$ clock cycles/access assuming 85% SRAM accesses and 15% DRAM accesses.

The cache controller uses the write-through method in which the controller writes every time to the DRAM and to SRAM. This technique minimizes the memory write time. The average write time, 5 clock cycles/access, is the same as for the DRAM access because the retry operation isn't needed.

Overall read and write speed for the new system can be calculated from the read accesses and the write accesses. It averages about $(2.75 + 5) \div 2 = 3.875$ clock cycles/access. The percentage performance increase over the non-cache system is $5 \div 3.875 = 29\%$.

The upgraded system board is the old system with the 68030 unplugged from its socket *(Fig. 2)*. The cache daughterboard includes the static RAM, a control block containing the cache controller that arbitrates between the old system resources and the cache system memory, and the 68030 microprocessor. A 169-pin connector links the old system to the daughterboard through the existing processor socket.

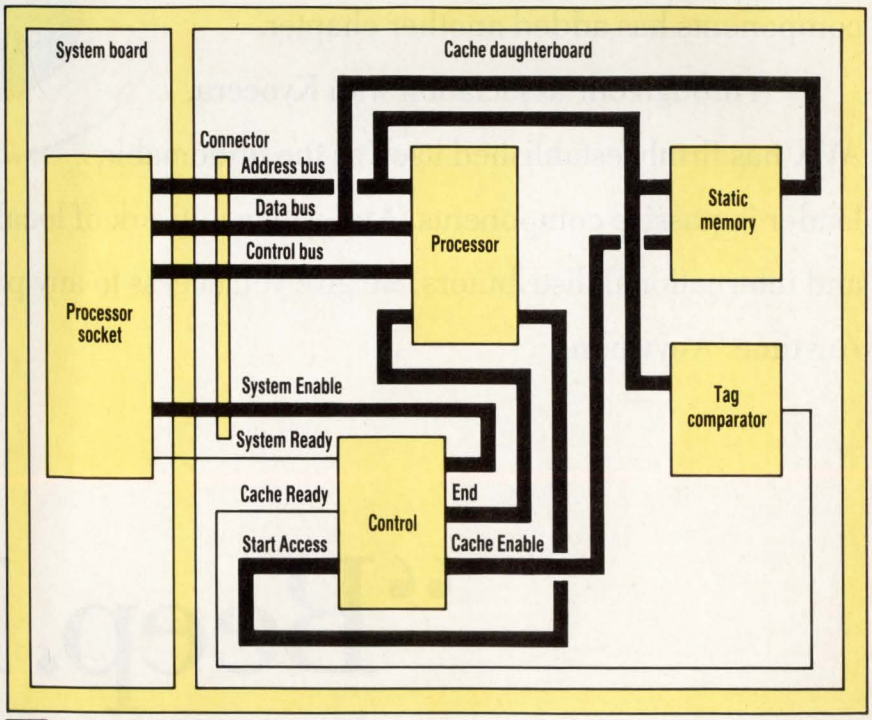
The address bus, which is the 68030 address bus (A_{0-24}), is shared by the processor, the cache system, and the old system. The data bus is the 68030 data bus (D_{0-31}) and is also shared by the processor, cache system, and the old system. The control bus consists of 68030 control signals that are shared by both the cache board and the system board. Those signals are Clock, Reset, Read/Write (R/W), and the dynamic bus-sizing signals.

The Start Access signal is the Address Strobe ($\overline{\text{AS}}$) signal from the 68030 microprocessor that indicates a valid access. $\overline{\text{AS}}$ indicates a valid address on the bus, and is connected to the cache controller to indicate a start of an access.

A Cache Hit

Cache Ready is an output of the tag comparator that indicates a cache hit if the information can be retrieved from the SRAM. The Cache Enable signal is an output of the cache controller to enables the SRAM so that the processor can get the information from it.

The cache controller drives the System Enable signal active if the processor needs information from the old system that has the DRAM and the peripherals. System Enable



2. AN EXISTING SYSTEM is upgraded by plugging a cache daughterboard into the system's microprocessor socket. The processor is relocated to the daughterboard.

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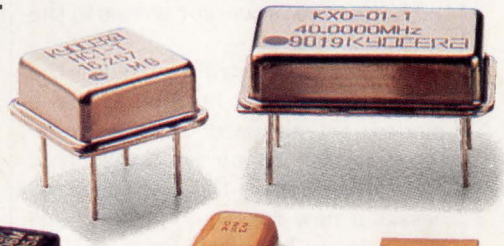

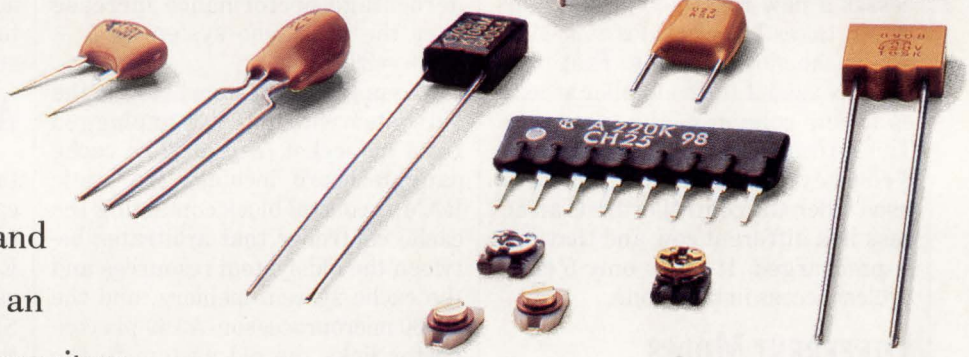

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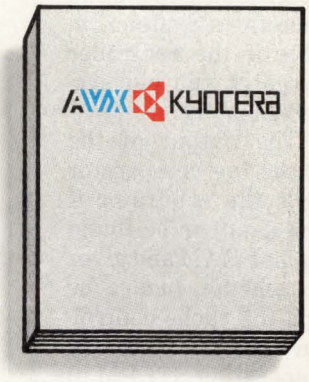

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CIRCLE 116

ng. Tick. Hum."

is the Address Strobe signal to the old system. Called $\overline{SYSAS}$, it starts accesses on the old board.

System Ready is used on the old system board for the bus cycle termination signal $\overline{DSACK}_{0-1}$. On the cache board, it's called $\overline{SYSDSACK}$ and tells the controller that the information is ready from the system board. The controller generates $\overline{STERM}$ and $\overline{DSACK}_{0-1}$ synchronous and asynchronous termination signals to end the processor access.

The cache controller has a special arbitrator that allows the 68030 to choose between the added system's SRAM memory and the old system's DRAM or peripherals. The arbitrator monitors the processor's Start Access signal ($\overline{AS}$), Clock, and the address. It then generates a Cache Enable signal if the controller accesses the cache and generates System Enable if the controller accesses the old system memory.

The output of the cache tag comparator tells the arbitrator if the data can be found in the SRAM and gives a cache hit. In a cache hit, the cache controller ends the access by generating $\overline{STERM}$ to the 68030.

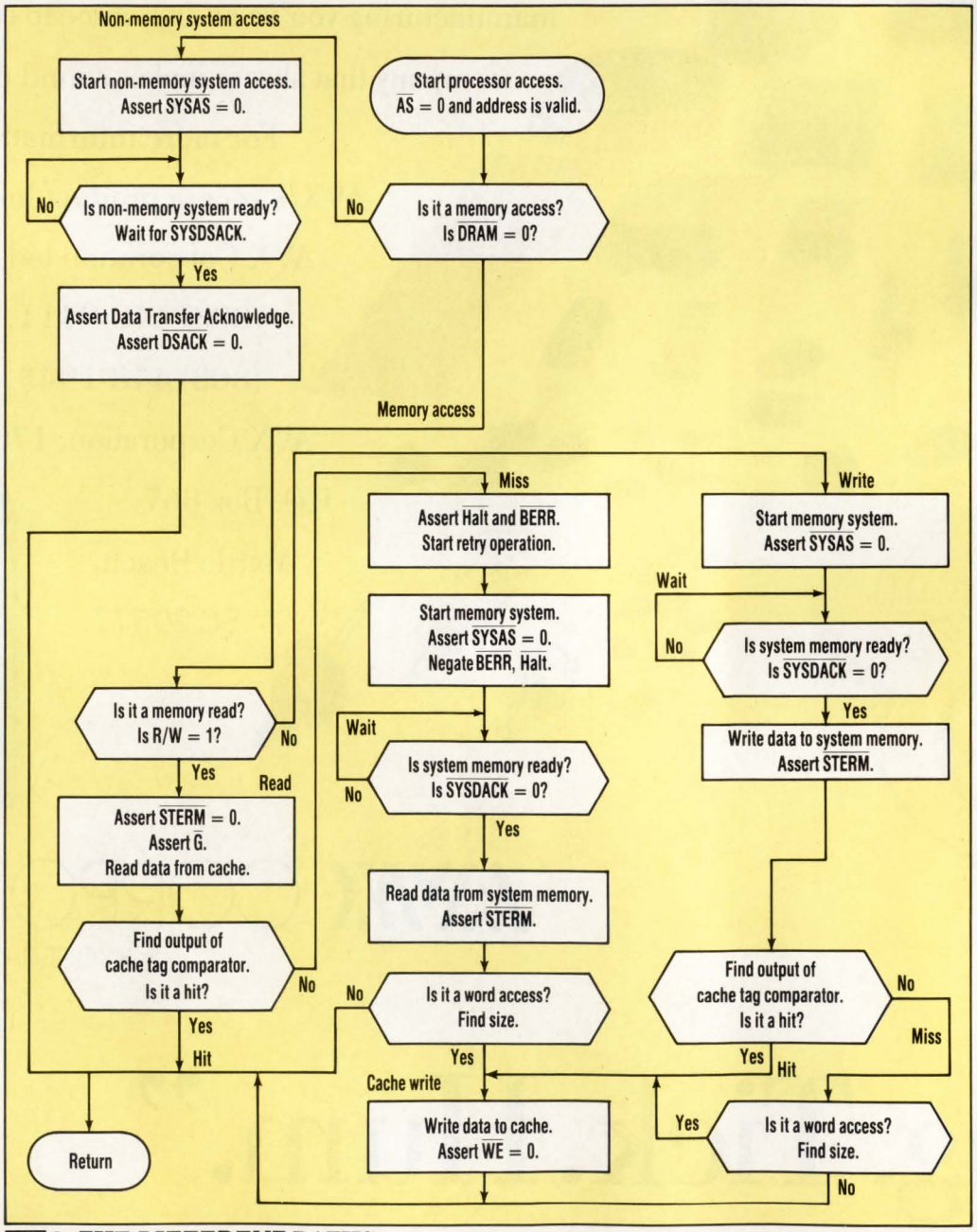
In a cache miss or a peripheral access, the arbitrator generates another start signal for the system board called $\overline{SYSAS}$. This signal is connected to the system board's $\overline{AS}$ signal in the interface socket. The system board sees $\overline{SYSAS}$ as a Start Address strobe from the processor, and responds to it with the asynchronous termination signal $\overline{SYSDSACK}$ when data is ready from the DRAM or a peripheral device.

The cache controller regenerates $\overline{STERM}$ after receiving $\overline{SYSDSACK}$ on a DRAM access. It passes the $\overline{SYSDSACK}$ signal directly to the processor as the $\overline{DSACK}$ signal on a peripheral access.

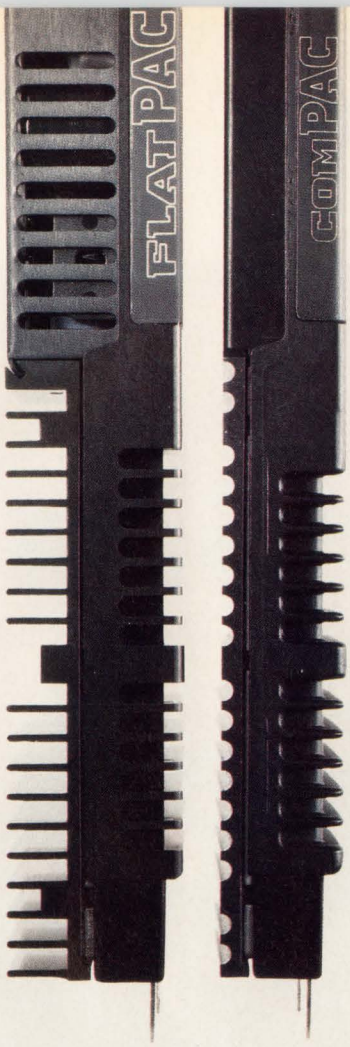
The 68030 processor supports synchronous bus cycles that are terminated with the Synchronous Termination signal $\overline{STERM}$. These cycles are for 32-bit ports and take a minimum of two clock cycles. The bus cycle is synchronous if:

- Data Transfer Acknowledge ($\overline{DSACK}$) is not asserted.
- The port size is 32 bits.
- Synchronous-input setup and hold time for $\overline{STERM}$ is met.

Synchronous mode is used to run



3. THE DIFFERENT PATHS taken by the cache-based system for memory and non-memory accesses are shown in a flow chart.



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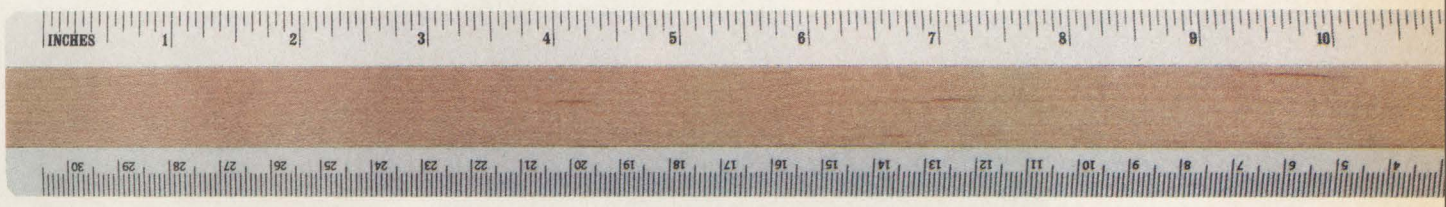

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Up to 600 Watts	**Output Power**	Up to 600 Watts
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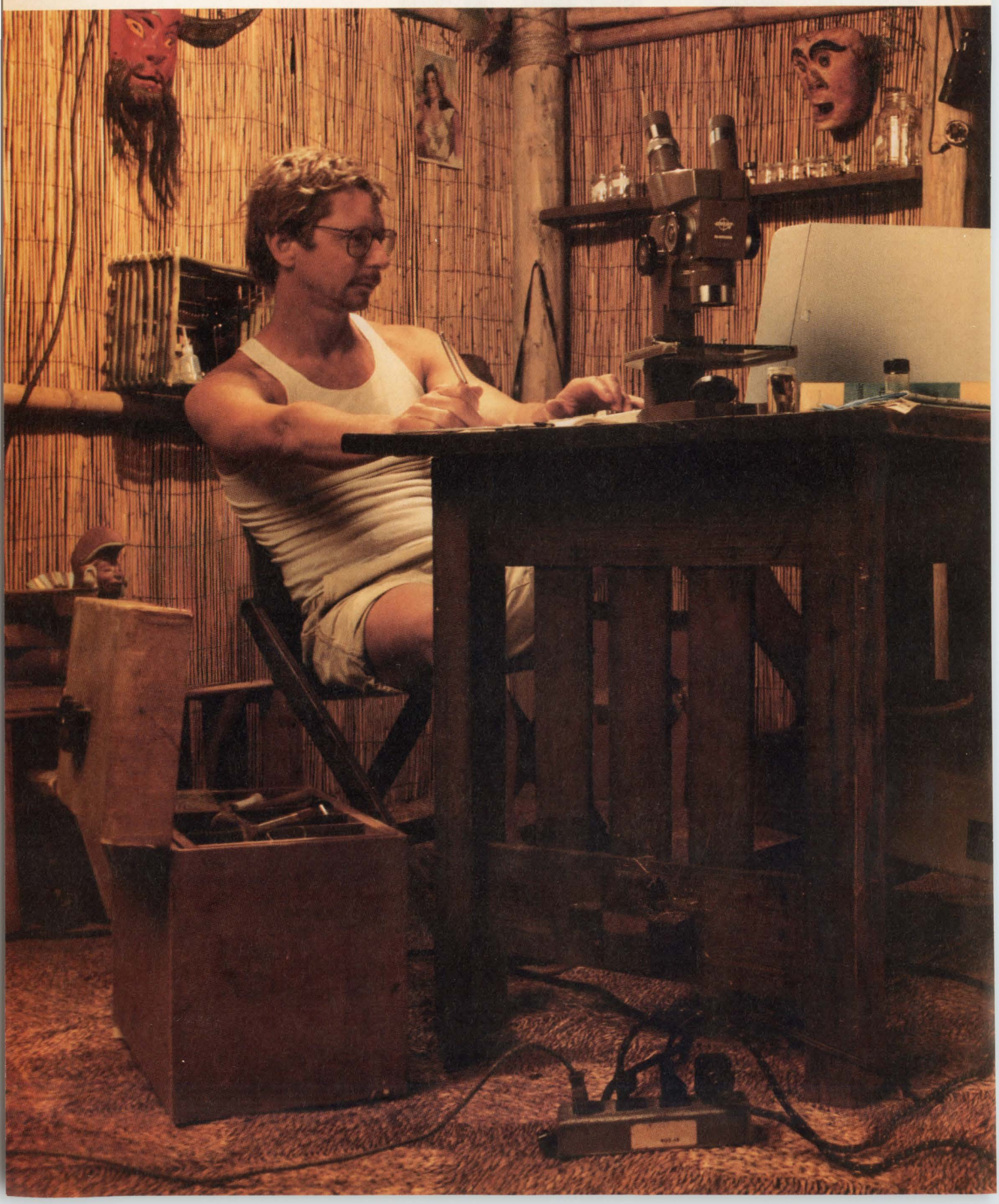

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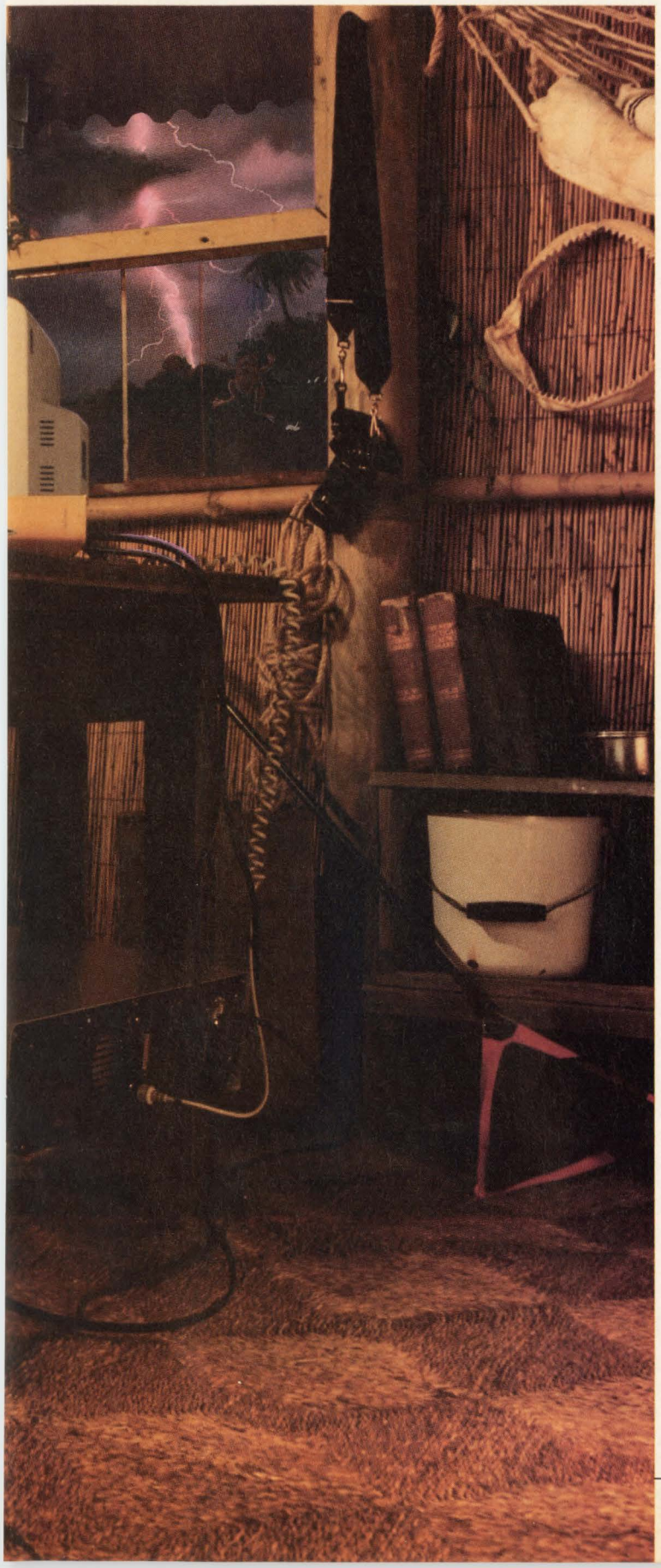

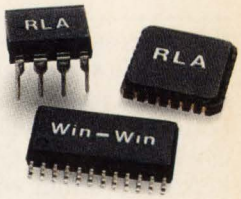

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Where quality starts with fundamentals

the processor at two cycles in the SRAM. To avoid wait states, the system must assert the $\overline{\text{STERM}}$ signal before the rising edge of the second clock cycle. Data must be valid 0 ns before the falling edge of the second clock so that the processor latches valid data. The cache controller asserts the Synchronous Termination ($\overline{\text{STERM}}$) signal early and doesn't wait for Address Strobe ($\overline{\text{AS}}$).

Asynchronous operation is used for data transfer to peripherals on the main system board. The system uses $\overline{\text{AS}}$, $\overline{\text{DS}}$, and $\overline{\text{DSACK}}$ to control data transfers.

$\overline{\text{AS}}$ signals the start of a bus cycle, and $\overline{\text{DS}}$ is used as a condition for valid data on a write operation. Decoding the 68030 size output signals and A_{0-1} provides strobes that select the active portion of data bus. The peripheral then responds by placing the requested data on the correct portion of the data bus and asserting the $\overline{\text{DSACK}}$ signals to terminate the cycle.

Retry Operation

On a cache miss, the cache controller forces a retry operation to prevent the processor from latching bad data. The system asserts $\overline{\text{STERM}}$ and doesn't wait for the output of the tag comparator to become valid, avoiding a wait state.

The cache controller asserts $\overline{\text{BERR}}$ and $\overline{\text{Halt}}$ during a bus cycle so that the processor enters the retry sequence. The processor samples the $\overline{\text{BERR}}$ and $\overline{\text{Halt}}$ signals on the falling edge of the second clock cycle. It also terminates the bus cycle and places the control signals in their inactive states. The processor retries the previous access when $\overline{\text{BERR}}$ and $\overline{\text{Halt}}$ are negated.

The decoder PAL device asserts $\overline{\text{DRAM}}$ if the accesses are to the memory *(Fig. 3)*. The PAL equation to generate the memory decode signal is:

$$\text{DRAM} = \overline{A_{24}} * \overline{A_{23}}$$

If $\overline{\text{DRAM}}$ is false, the access is to non-memory devices. On the start of processor access, the control PAL device monitors $\overline{\text{AS}}$ and $\overline{\text{DRAM}}$. It asserts $\overline{\text{SYSAS}}$ if the access is to the non-memory devices. The PAL equation is:

$$\text{SYSAS} = \overline{\text{DRAM}} * \text{AS}$$

$\overline{\text{SYSAS}}$ is the Start Access signal, previously $\overline{\text{AS}}$ in the old system. Assertion of $\overline{\text{SYSAS}}$ causes the system to start the non-memory access.

The write PAL device then waits for $\overline{\text{SYSDSACK}}$, which comes from the old system when it has valid data. The PAL device asserts the $\overline{\text{DSACK}}$ signals to end the processor cycle. The PAL equation is:

$$\text{DSACK} = \overline{\text{DRAM}} * \text{SYSDSACK}$$

The control PAL device asserts $\overline{\text{STERM}}$ when the processor starts a memory read. $\overline{\text{STERM}}$ comes early enough to be sampled by the processor's second clock rising edge for a synchronous access with zero wait states. The PAL device examines the results of the tag comparator's output and generates $\overline{\text{Miss}}$ if it's false. It also asserts a read enable signal called $\overline{\text{G}}$ to the SRAM. The PAL equations are:

$$\text{STERM} = \text{DRAM} * \text{R/W} * \overline{\text{Miss}}$$

$$\text{G} = \text{DRAM} * \text{AS} * \overline{\text{Miss}}$$

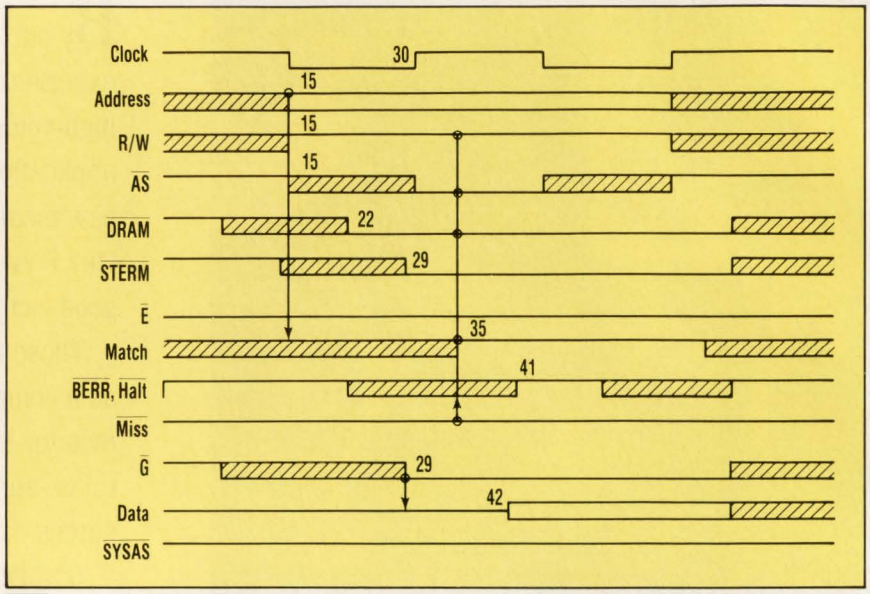
$\overline{\text{DRAM}}$ is generated by the address, and is valid at: time = address valid time + PAL delay = 15 + 7 = 22 ns *(Fig. 4)*. $\overline{\text{DRAM}}$ and R/W generate the $\overline{\text{STERM}}$ signal, which is valid at: time = $\overline{\text{DRAM}}$ valid time + PAL delay = 22 + 7 = 29 ns. The microprocessor samples $\overline{\text{STERM}}$ at the rising edge of S_2 at 30 ns for zero-wait-state access.

During an SRAM or DRAM read cycle, the cache controller asserts $\overline{\text{STERM}}$ and $\overline{\text{G}}$. It then generates a $\overline{\text{Miss}}$ state signal if MATCHA, $\overline{\text{MATCHB}}$, or both are false. The $\overline{\text{Miss}}$ state is generated from a PAL register clocked by the falling edge of the clock.

The decoder PAL device examines MATCHA and $\overline{\text{MATCHB}}$, and asserts $\overline{\text{BERR}}$ and $\overline{\text{Halt}}$ if a miss occurs. The processor samples $\overline{\text{BERR}}$, $\overline{\text{Halt}}$ on the falling edge of the second clock, and enters the retry operation. It stays idle for two cycles. $\overline{\text{Miss}}$ becomes active and negates $\overline{\text{BERR}}$ and $\overline{\text{Halt}}$, therefore the retry time is minimum.

$\overline{\text{SYSAS}}$ is asserted by the control PAL device as soon as $\overline{\text{Miss}}$ is generated. It doesn't wait for the processor to finish the retry mode. $\overline{\text{SYSAS}}$ starts the DRAM access from the system memory, thereby interleaving it with the cache accesses. The PAL equations are:

$$\text{Miss} = \text{DRAM} * \text{AS} * \text{R/W} *$$



4. A CACHE HIT occurs when the $\overline{\text{Miss}}$ signal is false. The processor can read data located in the SRAM when the $\overline{\text{G}}$ signal is asserted.

MEGA MEMORY.

SONY HIGH-DENSITY SRAMS

MODEL	CONFIG.	SPEED (ns)	PACKAGING	DATA RETENTION
CXK581000P*	128K x 8	100/120	DIP 600 mil	L, LL
CXK581000M*	128K x 8	100/120	SOP 525 mil	L, LL
CXK581100TM*	128K x 8	100/120	TSOP	L, LL
CXK581100YM*	128K x 8	100/120	TSOP (reverse)	L, LL
CXK581001P	128K x 8	70/85	DIP 600 mil	L
CXK581001M	128K x 8	70/85	SOP 525 mil	L
CXK581020SP	128K x 8	35/45/55	SDIP 400 mil	
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CIRCLE 125

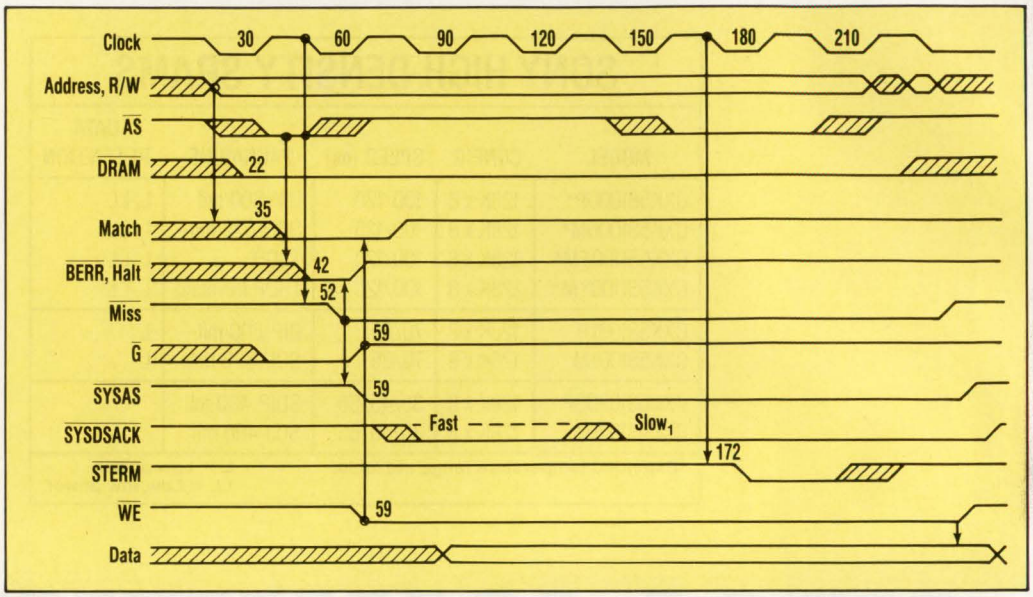
$\overline{(MATCHA * MATCHB)}$

$Halt = BERR = DRAM * \overline{AS} * R/W * \overline{(MATCHA * MATCHB)} * \overline{Miss}$

$SYSAS = DRAM * Miss$

The old system asserts $\overline{SYSDSACK}$ when it completes the DRAM access. The control PAL device waits until $\overline{SYSDSACK}$ comes before asserting $\overline{STERM}$ to end the access. The PAL equation is:

$STERM = DRAM * Miss * SYSDSACK$



5. IF THE TAG COMPARATORS don't find a match, a cache miss occurs; $\overline{BERR}$, $\overline{Halt}$ is asserted; and the processor reads data from the main memory.

Byte read or write from the SRAM is possible because the cache controller writes the data that comes from the system DRAM to the SRAM if it's a word. The PAL equation is:

$WE = Miss * (\overline{A_0} * \overline{A_1} * \overline{Size_0} * \overline{Size_1})$

The rising edge of $\overline{Miss}$ makes $\overline{WE}$ go from low to high and writes the data into the SRAM.

MATCHA, MATCHB comes from the address tag comparators, and is valid at: time = address valid + access time = 15 + 20 = 35 ns *(Fig. 5)*. $\overline{BERR}$, $\overline{Halt}$ comes from MATCHA, MATCHB, $\overline{DRAM}$, R/W, and $\overline{AS}$ at: time = match valid + PAL delay = 35 + 7 = 42 ns. The processor samples $\overline{BERR}$, $\overline{Halt}$ at the falling edge of S_2, which occurs at 45 ns.

$\overline{Miss}$ is generated from the clock's falling edge and $\overline{AS}$ at: time = falling edge of S_2 + PAL delay = 45 + 7 = 52. $\overline{BERR}$, $\overline{Halt}$ becomes false from $\overline{Miss}$ at: time = $\overline{Miss}$ valid + PAL delay = 52 + 7 = 59. The processor samples $\overline{BERR}$, $\overline{Halt}$ by the falling edge of the clock at 75 ns. In addition, $\overline{SYSAS}$ is generated by $\overline{Miss}$ at: time = $\overline{Miss}$ valid + PAL delay = 52 + 7 = 59 ns. $\overline{SYSDSACK}$ comes from the system DRAM controller before the clock's falling edge.

The cache system supports byte access from the SRAM to increase system performance. To support the byte read from the cache memory, the controller uses byte writes to the static RAM in a write access with a hit. In a memory write with a miss, the cache controller writes the data to the SRAM if it's a word access. The PAL equations for a write operation are:

$SYSAS = DRAM * \overline{(R/W)} * AS * \overline{SYSHALT}$

$STERM = DRAM * \overline{(R/W)} * AS * SYSDSACK$

$WE = DRAM * \overline{(R/W)} * AS * (MATCHA * MATCHB) + DRAM * \overline{(R/W)} * AS * (\overline{A_0} * \overline{A_1} * \overline{Size_0} * \overline{Size_1})$

On a write to memory, the control PAL asserts $\overline{SYSAS}$ to start the DRAM access. Control PAL waits for the $\overline{SYSDSACK}$ (DRAM is ready) signal, then it asserts $\overline{STERM}$ to finish the cycle. The control PAL generates the $\overline{WE}$ signal to do byte write to the SRAM if the accesses are a write with a hit. In a write with a miss, the controller asserts $\overline{WE}$ to do only word write if $(\overline{A_0} * \overline{A_1} * \overline{Size_0} * \overline{Size_1})$ is true.

$\overline{SYSDSACK}$ generates $\overline{STERM}$ on DRAM accesses and when $\overline{STERM}$ = $\overline{SYSDSACK}$ valid + PAL delay = 45 + 7 = 52 ns. The processor samples $\overline{STERM}$ at the clock's rising edge at 60 ns.

The cache controller improves the system refresh time by hiding the refresh in memory or peripheral accesses. The old system uses the $\overline{Halt}$ signal to refresh the DRAM. With the new design, the cache controller can monitor $\overline{SYSHALT}$ (the old $\overline{Halt}$ that goes to the processor socket in the old system board) and doesn't assert a $\overline{Halt}$ signal to the processor. The controller, instead of halting SRAM or peripheral accesses, allows them to continue.

The cache controller uses the $\overline{SYSAS}$ and $\overline{SYSHALT}$ signals to stretch a system DRAM access if the refresh is occurring during a memory access. If a refresh has already started, the controller delays the start of a system DRAM access until the refresh is finished.□

Nagi Mekhiel, a professor in the Electrical Engineering Dept. at Ryerson Polytechnical Institute in Toronto, has a BSEE from the University of Assiut, Egypt, and an MSEE from the University of Toronto.

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MODERATELY	542
SLIGHTLY	543

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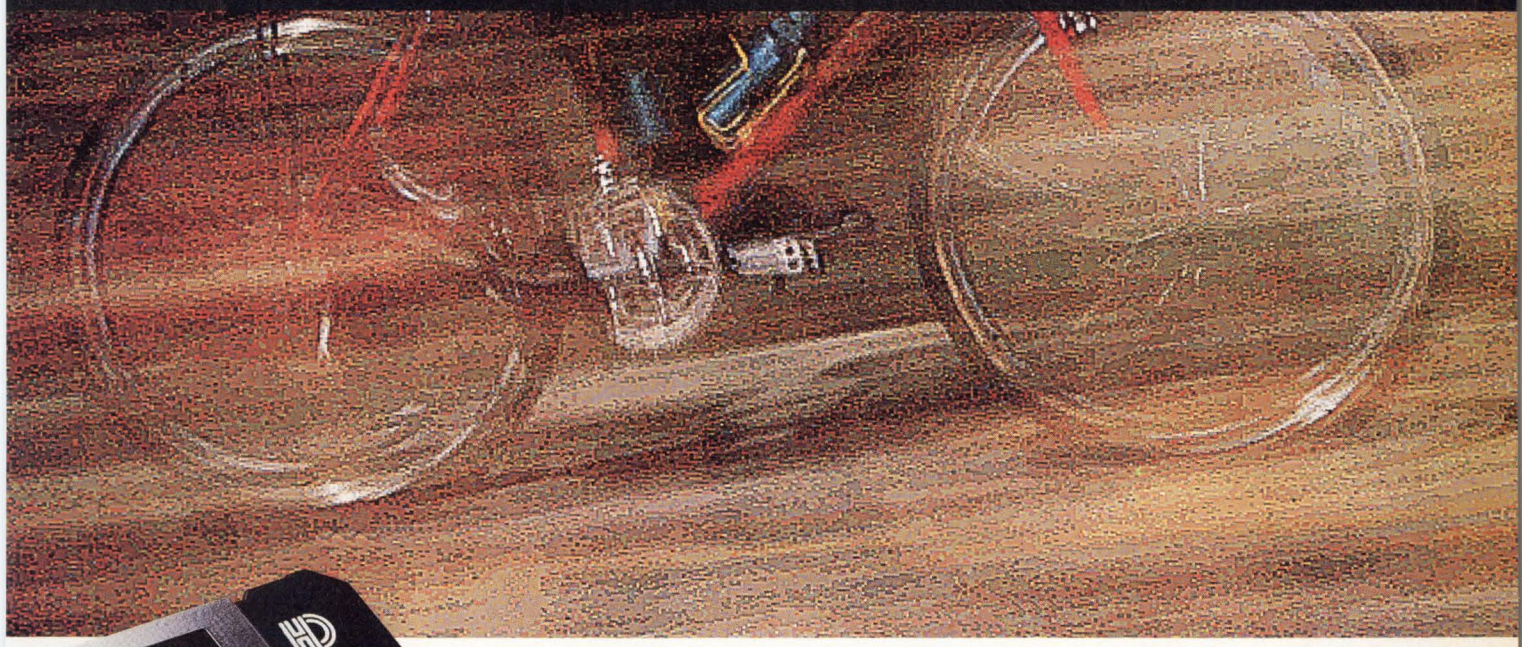

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CIRCLE 2

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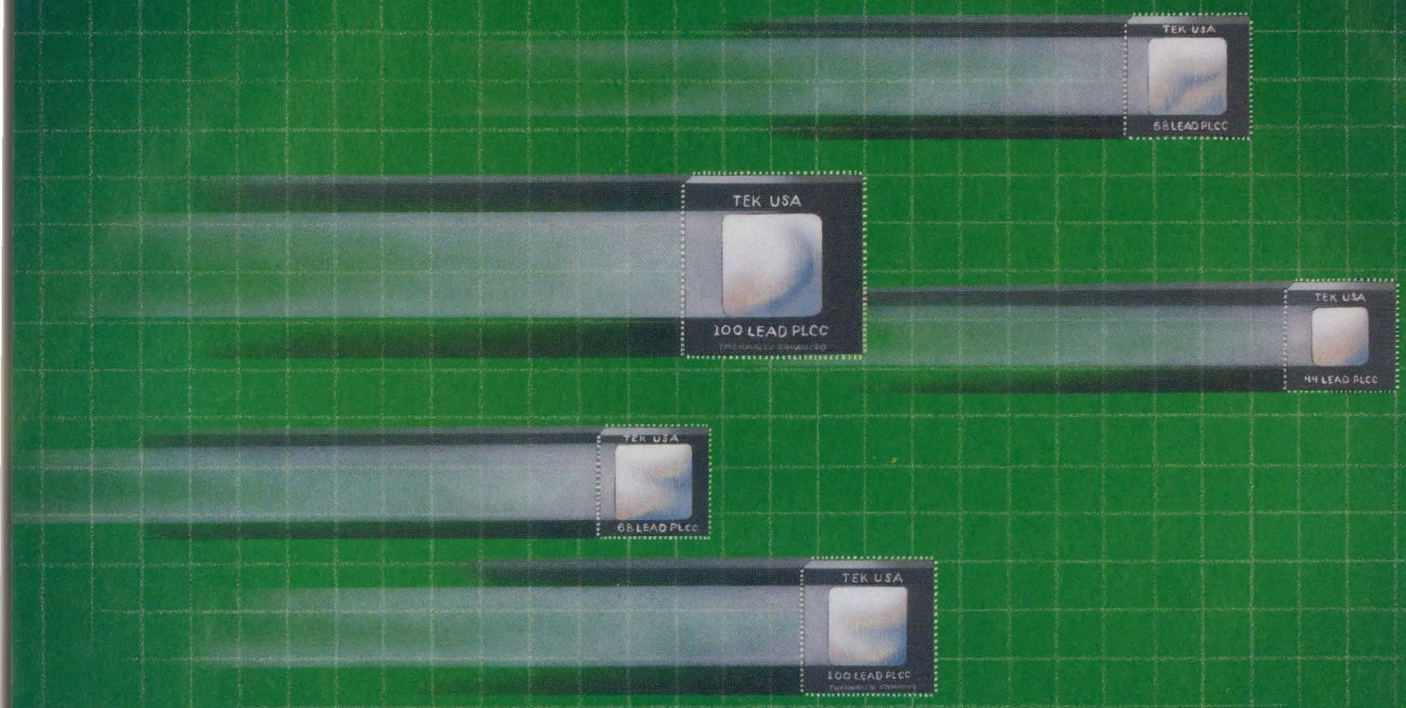

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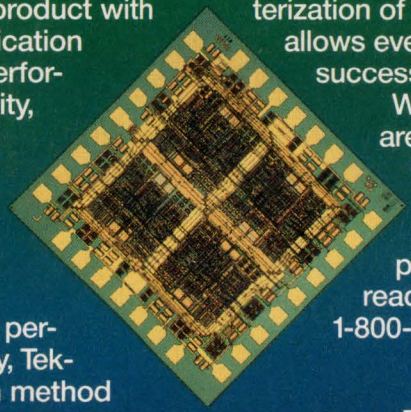

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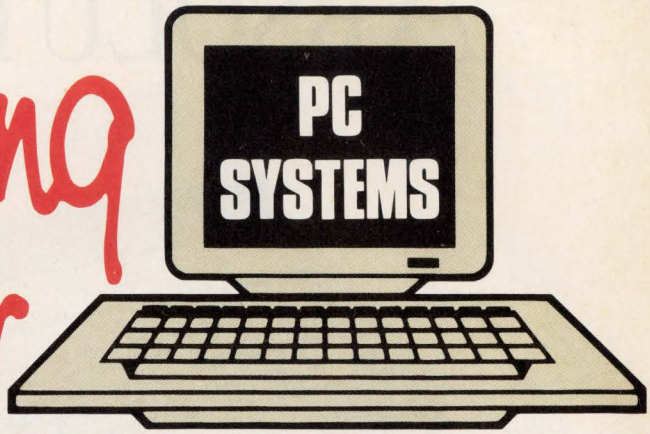
CIRCLE 119

Designing For PC SYSTEMS



This is the second installment of a new section in Electronic Design focusing on the design of PC systems. The section will appear regularly throughout 1991.

Chip Set Runs 486 CPUs From 20 To 50 MHz

OPTI INC., SANTA CLARA, Calif. has started sampling a motherboard chip set for AT-based systems that can support 80486 personal-computer architectures running at clock speeds from 20 to 50 MHz. The 486WB chip set also incorporates write-back cache-control logic to improve the processor efficiency over standard write-through cache implementations. By placing all of the speed-critical memory data paths in the 82C491 (the first of the two chips in the chip set), designers at the company could simplify the memory subsystem on the motherboard. DRAMs with access times from 80 to 120 ns could be used without impacting cache performance. Caches from 64 to 512 kbytes can be implemented, and cache burst cycles of 2-1-1-1 and 3-1-1-1 are supported for 33- and 50-MHz system clocks, respectively. Thesubsystem enables the CPU to achieve about a 10% performance improvement over write-through approaches. The second chip, the 82C492, handles the bus interface and CPU control and clocking. It requires just a single-phase 50-MHz input, which should also satisfy FCC certification requirements. The 33- and 50-MHz versions are immediately available for $80 and $110, respectively, in 10,000-set lots. Contact Raj Jaswa (408) 980-6511. CIRCLE 532

Innovative Designs Debuted At MAC Expo

A PLETHORA OF APPLE Macintosh support and expansion products could be seen in almost every aisle at the recently held Mac Expo in San Francisco, Calif. A six-processor Macintosh-based system developed by Pacific Data Systems, Arieta, Calif., delivers the power of six Macintosh systems in one desk-side cabinet. The system employs a proprietary CPU-sharing multiplexed design that gives the power user multiprocessing capabilities that permit multiple complex tasks to execute concurrently. Integrating six processors in one system improves system efficiency because all six share the same peripherals. Contact Alex Nury, (818) 899-6077.

.....For Macintosh users that need the utmost in data-transfer rates from their mass-storage systems, a disk array storage subsystem developed by MicroNet Technology Inc., Irvine, Calif. pushes the sustained transfer rate to 4.4 Mbytes/s. The array uses a 16-bit SCSI-2 interface and proprietary control software that takes advantage of the SCSI-2 commands to deal with small- and large-block accesses. An overlapping seek algorithm is also used to achieve effective seek times as fast as 5.7 ms. The $19,995 Raven SBT-2500NPR contains a pair of 1.25-Gbyte drives and dual, SCSI-2 host adapters. Contact Suzanne Kimball, (714) 837-6033.

.....Using an offshoot of the solid-state still-image camera developed by several Japanese companies, Dycam Inc., Chatsworth, Calif., has created a still-image "point-and-shoot" camera that feeds data directly to the Macintosh or a PC. The Dycam model 1 captures and stores up to 32 gray-scale photographs with a resolution of 376-by-240 pixels and 256 shades of gray. Like electronic cameras, just one button needs to be pressed to capture an image—exposure setting, flash, and focus are all controlled automatically. Captured images are transferred to the computer over the serial communications port. Contact Mark Vonarx, (818) 988-7951.

.....A 68040-based NuBus card extends the useful life of older Macintosh II systems by accelerating computations on Macintosh II computers. The card, from Radius Inc., San Jose, Calif., will come in 25- and 33-MHz versions and operates transparently to all Macintosh programs. The card will speed integer and floating-point operations, and will also be integral component to Radius' high-performance color display subsystems. Contact Steve Holtzman, (408) 434-1010.

.....For Macintosh, PC, or workstation users that really need data in a hurry, Atto Technology Inc., Amherst, N.Y., unveiled a solid-state disk subsystem that trims the access time to just 50 μs, potentially improving system performance by up to 10-fold over mechanical disk drives. The SiliconDisk Plus employs an 8-bit SCSI interface to the host system and can sustain a 5-Mbyte/s data-transfer rate. The base system has 32 memory slots—each can hold 1- or 4-Mbyte SIMMs for a total capacity of 128 Mbytes. Contact Tim Klein at (716) 688-4259. A slightly slower solid-sate drive with the same capacity was also released by Newer Technology, Wichita, Kans. Its access time is just 0.5 ms, about 10 times that of the Atto drive. Contact Newer at (316) 685-4904.

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CIRCLE 107

Simple upgrade lets 80386 systems use i486

Adding a few PLDs and some simple logic enables an i486 CPU to boost system throughput.

BY BRIAN DELLACROCE

VLSI Technology Inc., 8375 South River Pkwy., M/S 260, Tempe, AZ 85284; (602) 752-6394, FAX 602-752-6000.

A performance boost of up to 290% for systems currently using the full 32-bit 80386DX microprocessor from Intel Corp. is now possible by substituting the more powerful i486 processor. However, rather than redesign the entire system motherboard to use a new chip set and go through the component requalification process, existing i386-based systems can be modified with the addition of about seven active components to accept the i486 processor and run in the non-burst mode. The cost of the modification is about $30, not counting the cost of the new CPU.

Benchmark performance comparisons between a 33-MHz 80386DX-based system using an 80387 coprocessor and a converted i486-based system are shown in Table 1. The performance increases come from several architectural improvements that were incorporated in the i486: specifically, the internal, high-speed cache memory and the on-board floating-point unit (FPU). The processor's instruction set was also optimized for speed. However, the built-in 8-kbyte cache has the most impact on performance.

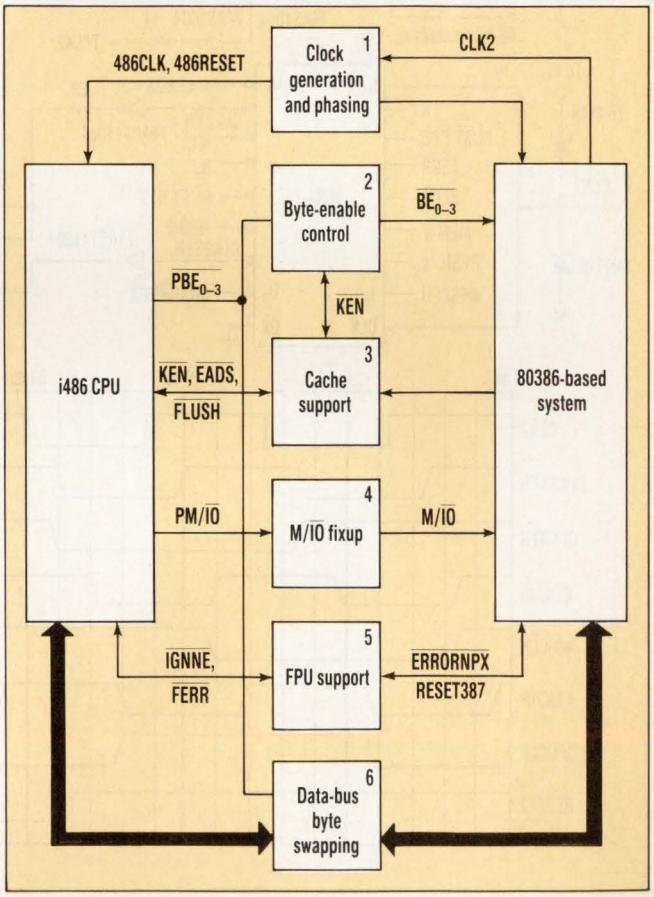
The one feature that the i386 system modification can't incorporate—burst-mode transfers—enables the i486 to achieve significantly higher bus throughput rates than the 80386DX's pipelined method. However, using the burst mode would require significant changes to the memory subsystem. When substituting an i486 for an 80386DX in a system originally designed for an 80386DX, there are a number of hardware issues and incompatibilities that the processor interface must resolve *(Fig. 1)*.

The first area, clock generation and phasing, is fairly straightforward. The i486 requires a clock that's half the frequency of the clock supplied to the 80386DX. Many systems already have an internal clock with that frequency. However, in these systems (e.g. chip sets), this lower frequency (internal) clock signal may not be available to drive the i486's clock input. The clock also may be disabled when the system is in reset. However, the i486 must be supplied with an active clock during reset. Consequently, the interface circuitry may have to divide the master 80386DX clock frequency in half to generate the i486's clock.

In addition, the logic must ensure that the i486's clock is generated in phase with the system's (internal) clock. There are two approaches that can be used. First, the system's clock can be synchronized to be in phase with the clock supplied to the i486. Second, the clock supplied to the i486 can be synchronized to the system's clock.

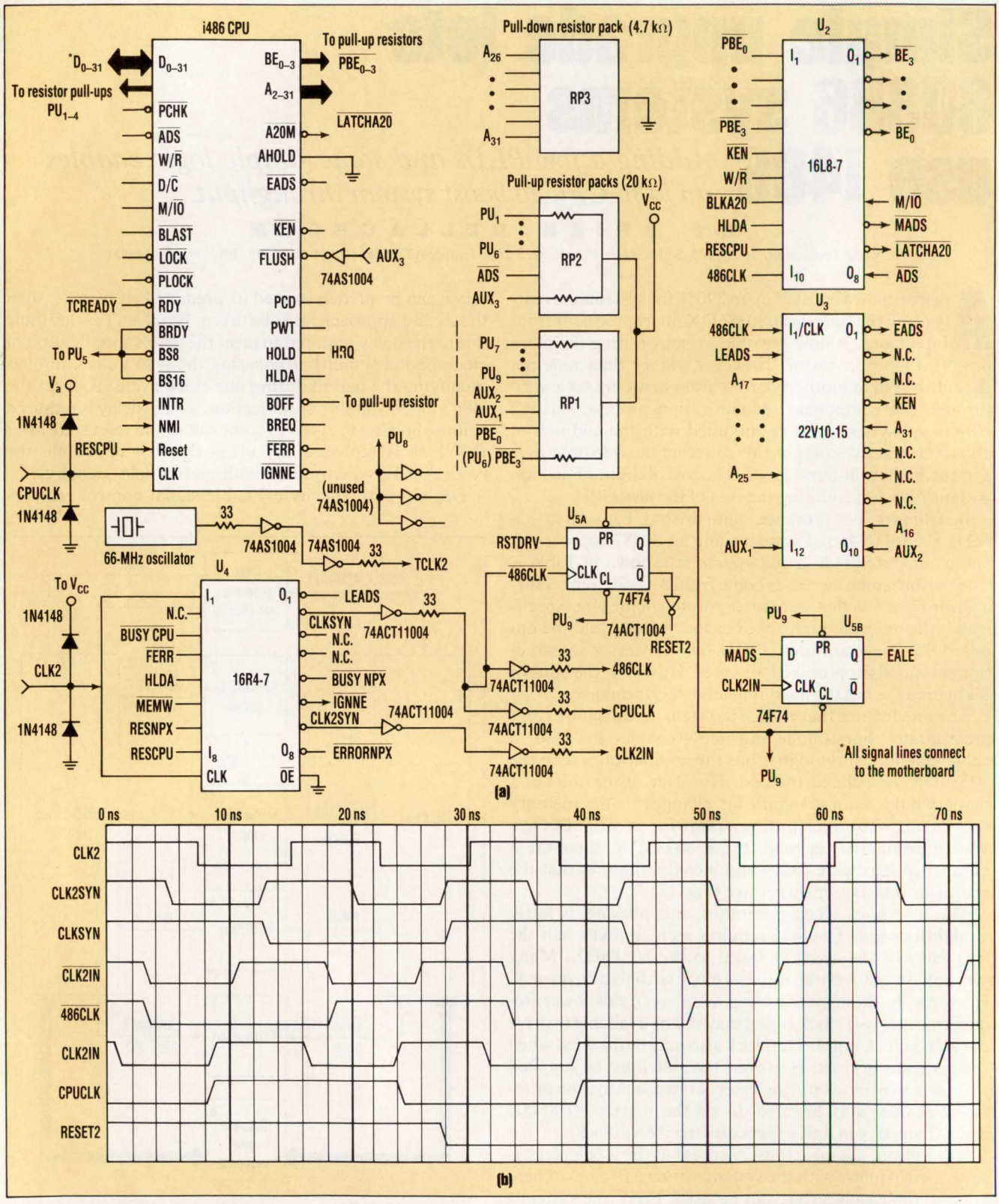
The first approach is recommended if the system clock's phase can be predetermined or predicted. If it can't, then the second approach must be taken. But it isn't as desirable due to the delay required to meet the i486's specification of clock-period stability. Rephasing the i486's clock implies modifying the period during one clock cycle. To meet the i486's clock-stability specification, a 1-ms delay is required before allowing the i486 to come out of the reset state after the clock is rephased. By using the first approach, the clocks can be synchronized without this delay penalty.

Dealing with the Byte Enable signal control requires



1. To replace an 80386DX processor with an 80486 without redesigning the entire system, an adapter can be built to handle the six areas in which the two CPUs are incompatible.

RUN 80486 WITH 80386 CHIP SET



2. The logic needed to build an adapter that converts an 80386DX system to work with an 80486 microprocessor consists of seven small logic chips plus the CPU and a few discrete components (a). The adapter must deal with such issues as synchronizing the CPU to the system clock (U_4, U_{5A}, U_{7A-B}, and U_8), ensuring correct operation of the cache (U_3), and controlling the byte-enable lines (U_2). The typical clock waveforms and reset input to the Topcat VL82C330 controller illustrates that timing is critical in the path that generates RESET2 (b).

monitoring the internal state execution of the processor. When an i486 issues the first address of a cache line fill, it may not assert all four Byte Enable signals. This occurs when the internal execution unit requests only 8 or 16 bits of information. Byte enables are asserted at the same time the address is driven, but the cache unit can only determine if an address is cacheable after it samples the Cache Enable input (KEN).

Because the cache line is four 32-bit (double) words, the i486 expects valid data on all 32 data lines for cacheable regions, even though it didn't drive all four Byte Enable lines active. The system must supply 32 bits of valid data so that invalid data isn't cached. If the address is cacheable, the interface must ensure that all four Byte Enable lines are asserted to the system.

The modified interface must define non-cacheable memory areas (for example, video, expanded memory, etc.) and drive the i486's KEN input accordingly. In addition, cacheability information should be supplied to the part of the interface that must overcome the byte-enable issue. Cacheability mapping can be accommodated by using either of two possible methods to decode the address lines and generate the KEN signal. In the first scheme, a programmable logic chip can be used, or alternatively, a fast static RAM can be added. The PLD has the advantage of simplicity and low cost, while the SRAM offers more flexibility for programmers to define the cacheability map. However, the implementation is more complex and costs more as well.

Cache support also requires that the cache invalidation signal be generated (EADS). During non-CPU (e.g. DMA) transfers to main memory, the i486 must snoop the address bus and invalidate cache lines. Therefore, addresses must be driven to the i486 during non-CPU transfers. Some 80386DX-based systems may not have this ability because the address bus for an 80386DX is defined as output only. Furthermore, all 32 address lines must be driven during non-CPU cycles. Because very few systems use the full available 32-bit address space, some of the upper address lines may not be driven during non-CPU cycles. The cache-flush mechanism can also prevent a stale cache condition caused by non-CPU writes. The snooping method will perform better because the entire cache need not be invalidated during DMA cycles.

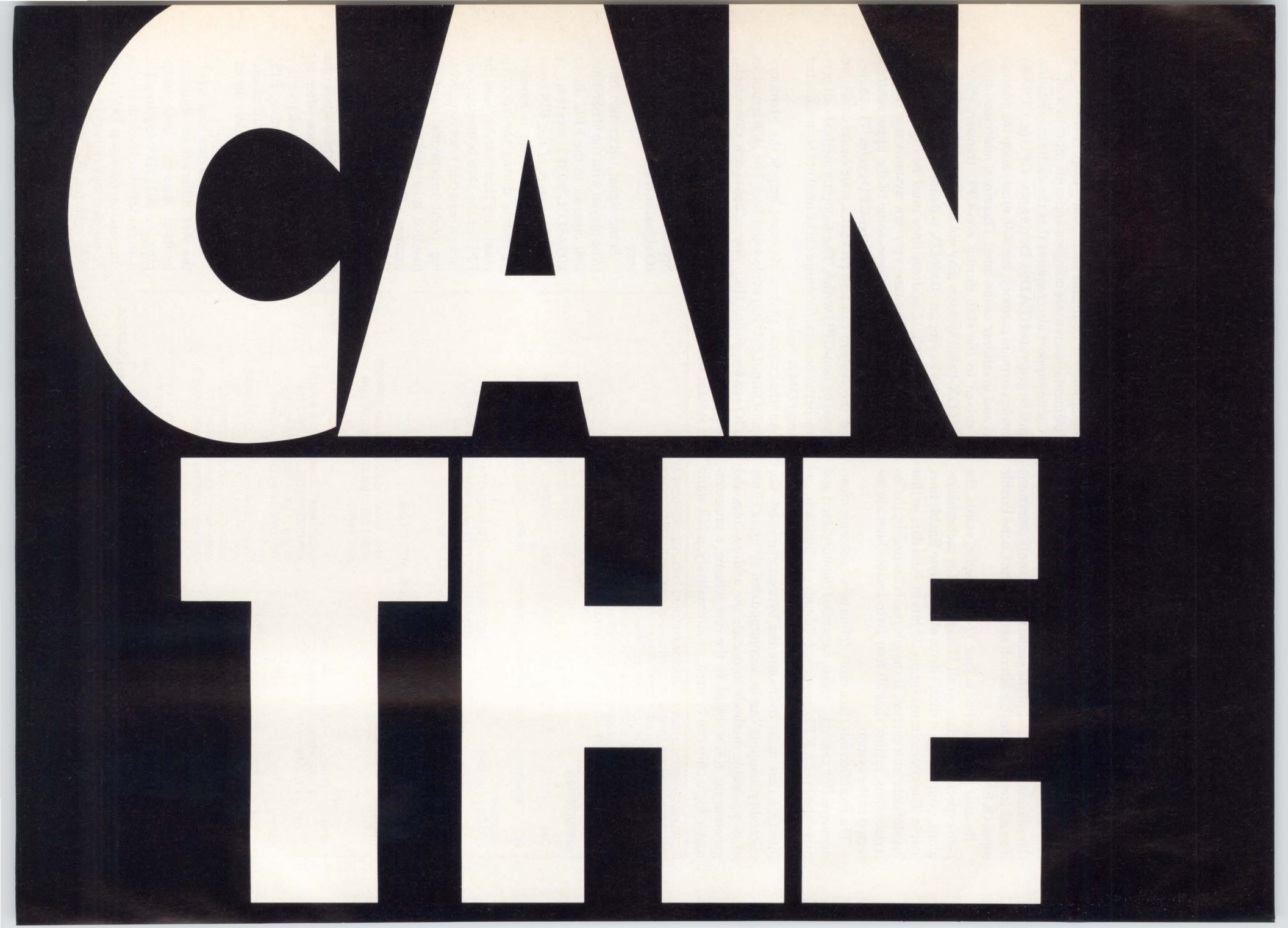
Another signal that needs some help is the Memory/Input-Output (M/IO) cycle select line. The i486 issues an M/IO as a low during Halt/Special bus cycles. Conversely, the 80386DX issues M/IO as a high during these cycles. If the system uses M/IO to decode Halt/Special cycles, the interface must detect the Halt/Special cycle and invert the M/IO signal as it appears to the system.

```
;THIS PLD GENERATES CLKSYN AND CLK2SYN FROM CLK2. CLKSYN IS CLK2 DIVIDED BY
;TWO AND DE-SKEWED TO MATCH CLK2SYN WHICH IS A BUFFERED VERSION OF CLK2.
;SKEW BETWEEN CLKSYN AND CLK2SYN IS LESS THAN 1NS AND IS SIMPLY THE INTERNAL
;SKEW BETWEEN SIMILIAR NON-REGISTERED PATHS. NOTE, PHASE SYNCRONIZATION OF
;CLKSYN TO CLK2SYN IS NOT NECESSARY SINCE SYNCHRONIZING THE CHIPSET
;TO THE PROCESSOR IS ACCOMPLISHED BY CONTROLLING RESET TO THE '330.
;THIS PLD ALSO GENERATES IGNNE _ TO THE 486 AND ERRORNPX _ TO THE CHIPSET.

CHIP U4 PAL16R4
;1       2        3          4       5        6        7        8        9        10
CLK2     CLK2A    BUSYCPU _  NC      FERR _   HLDA     MEMW _   RESNPX   RESCPU   GND
;11      12       13         14      15       16       17       18       19       20
OE _     ERRORNPX _ CLK2SYN  IGNNE _ BUSYNPX _ FERR1 _  CLK2BY2 CLKSYN  /LEADS _  VCC

EQUATIONS
CLK2BY2 := /CLK2BY2                    ; EQUALIZE INTERNAL DELAY BETWEEN
                                       ; CLK2SYN AND CLKSYN FOR MINIUM POSSIBLE SKEW.
/CLKSYN = /CLK2A    * /CLK2BY2         ; LATCH ON NOT CLK2A FOR VERY LITTLE SKEW IN
        +  CLK2A    * /CLKSYN          ; RELATION TO CLK2SYN.
        + /CLK2BY2  * /CLKSYN

CLK2SYN = /CLK2A                       ; ONE PROP DELAY TO DESKEW.

ERRORNPX _ = BUSYNPX _                 ;WHEN A NUMERIC ERROR OCCURS -FERR GOES
                                       ;ACTIVE THIS CAUSES U3 TO ACTIVATE THE
                                       ;ERRORNPX _.

IGNNE _ := FERR1 _ + FERR _ + /BUSYNPX _
         + /ERRORNPX _ + /BUSYCPU _    ;THE INTERRUPT SERVICE ROUTINE IS THEN
         + RESNPX                      ;EXPECTED TO CLEAR THE INTERRUPT BY
                                       ;WRITING TO PORT F0h. AT THIS POINT
FERR1 _ := FERR _                      ;THE -IGNNE SIGNAL IS DRIVEN LOW BY
                                       ;THIS PAL
                                       ;THUS CAUSING THE PROCESSOR TO IGNORE
BUSYNPX _ := FERR _ + /FERR1 _ + RESNPX ;NON-CONTROL FLOATING POINT
                                       ;INSTRUCTIONS. -IGNNE IS DEACTIVATED
                                       ;WHEN -FERR GOES HI IN RESPONSE TO
                                       ;SOFTWARE CLEARING THE NUMERIC ERROR.

LEADS _ = /MEMW _ * HLDA               ;FORM LONG INVALIDATION SIGNAL ON ANY
                                       ;MEMORY WRITE WHEN IN HOLD. THEN GO
                                       ;ELSEWHERE AND SHORTEN TO 1 CLOCK LONG
```

3. The logic equations to configure U_4 are relatively simple. The PLD generates the CLKSYN and CLK2SYN signals from the CLK2 signal.

Some signal tricks also have to be played with the 80386 lines that connect to the FPU. In an 80386DX/80387 system, a hardware reset of the FPU can be performed when it handles exceptions during various computations. However, because the FPU of the i486 is internal and lacks a separate reset line, floating point exceptions must be handled in a slightly different manner. The Ignore Numeric Error (IGNNE) input to the i486 is designed to allow its FPU to recover from an exception. The FPU will freeze upon the next FPU instruction after an error if IGNNE is inactive. By driving this input active, FPU control instructions can be executed to handle and clear the exception.

One other signal area where the i486 differs is its ability to perform data-bus byte swapping. An 80386DX requires that data read from a 16-bit device be supplied on the lower half of the 32-bit data bus (bits 0-15). The i486 requires that the data ap-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CIRCLE 123

pear on the data lines as indicated by the Byte Enable lines. For example, consider a 16-bit (word) read cycle of byte addresses 2 and 3 from a 16-bit device. Either processor will assert Byte Enables 2 and 3 (making them true) when issuing the address. However, the 80386DX will expect the data to appear on data lines 0-15 while ignoring data on lines 16-31. The i486 expects the data to appear on data lines 16-31 and will ignore data lines 0-15. A similar mechanism applies for accesses to 8-bit devices. This can present difficulties in systems that don't "mirror" the data on the unused lines of the processor data bus.

In most systems, timing constraints on the M/$\overline{IO}$ and the Byte Enable signals are the critical factors in obtaining the highest performance from an i486 conversion. Because of delays imposed in manipulating these signals, a one-clock-cycle delay may have to be injected at the beginning of each bus cycle. In other words, the Address Strobe ($\overline{ADS}$) signal may have to be delayed by one full processor clock to have more time available. In this manner, the bus cycles can be pipelined to the system, starting the system cycle one clock after the i486 cycle. This is undesirable because it adds one wait state to all bus cycles. But, since the i486 operates from its internal cache most of the time (which doesn't require bus cycles), the overall system performance reduction isn't as severe as might first be expected.

A more detailed view of the actual circuitry required to implement the i486 upgrade to an 80386DX system can be captured by examining a system implementation using VLSI Technology Inc.'s VL82C386SET "Topcat" PC/AT-compatible chip set. This chip set compresses most of the logic on a system motherboard to just three chips: the VL82C330 System Controller, the VL82C331 ISA Bus Controller, and the VL82C332 Data Buffer.

For systems that already employ the Topcat chip set, two of the six interfacing issues—the byte swapping and M/$\overline{IO}$ issues—are eliminated. Byte swapping is eliminated because the chip set never asserts $\overline{BS8}$ (bus size equals 8 bits) or $\overline{BS16}$ (bus size equals 16 bits) to the processor. Device support for 8- and 16-bit I/O transfers is hidden from the processor and the data is automatically mirrored onto the "unused" portions of the processor data bus. In addition, the chip set doesn't use M/$\overline{IO}$ to recognize Halt/$\overline{Special}$ cycles. This makes M/$\overline{IO}$ manipulation unnecessary.

As mentioned, the best method for handling the clock synchronization issue is phasing the chip set to the processor's clock. This eliminates any need to wait for the i486's clock to stabilize after rephasing. Also, it's important when running an operating system, such as OS/2, or other applications that reset the processor to switch from native to protected mode.

Rephasing the chip set requires one flip-flop that delays the reset line to the system controller chip. The system controller chip generates an internal clock signal that's the same frequency as the i486's clock. Because the system controller generates the reset signal to the i486, by controlling the point at which reset is released, the internal clock is guaranteed to be in phase with the i486 clock.

Timing is critical when synchronizing the reset signal, so timing should be examined carefully. The VL82C330 samples its reset input on every rising edge of CLK2IN. Because CLK2IN is a 66-MHz signal (for 33-MHz 80386 operation), high-speed logic must be used *(Fig. 2a)*. The typical waveforms of the clock signals required by

```
; THIS PLD GENERATES THE FOLLOWING SIGNALS
;  KEN __ - CACHE ENABLE IS DECODED FROM ADDRESS A16-A31
;           CURRENTLY THE FOLLOWING AREAS OF MEMORY WILL NOT BE CACHED.
;           000A 0000 - 000B FFFF ; VIDEO RAM
;           000C 0000 - 000C FFFF ; VIDEO BIOS (OPTIONAL VIA THE 330 CHIP'S EXT CTRL 1 OUTPUT)
;                                   EXT CTRL1 = 1 , VIDEO BIOS CACHEING ON
;                                   EXT CTRL1 = 0 , VIDEO BIOS CACHEING OFF
;           000D 0000 - 000D FFFF ; EMS
;           000E 0000 - 000F FFFF ; BIOS -(OPTIONAL VIA THE 330 CHIP'S EXT CTRL 2 OUTPUT)
;                                   EXT CTRL2 = 1 , BIOS CACHEING ON
;                                   EXT CTRL2 = 0 , BIOS CACHEING OFF
;           8000 0000 - FFFF FFFF ; POWER ON RESET
;
; EADS __ - A SHORTENED (1 CLK WIDE) ADDRESS INVALIDATION SIGNAL GENERATED DURING MEMORY
;           WRITES DURING HOLD.
;
CHIP U3 PAL22V10
;PIN1      2        3    4    5    6    7    8    9    10    11     12
 CLK    LEADS __   A17  A18  A19  A20  A21  A22  A23   A24   A25    GND
; 13     14       15    16    17    18    19    20     21           22          23        24
AUX1   AUX2     A16    NC    NC    NC    A31   KEN __ SLEADS __  DSLEADS __  /EADS __  VCC

EQUATIONS
KEN __ = /A16 * /A17 * A18 * A19 * /A20                    ; CXXXX VIDEO BIOS
       * /A21 * /A22 * /A23 * /A24 * /A25 * /AUX1          ; bios

       + A16 * /A17 * A18 * A19 * /A20                     ; DXXXX EMS
       * /A21 * /A22 * /A23 * /A24 * /A25

       + /A16 * A17 * /A18 * A19 * /A20                    ; AXXXX VIDEO
       * /A21 * /A22 * /A23 * /A24 * /A25                  ; buffers

       + A16 * A17 * /A18 * A19 * /A20                     ; BXXXX VIDEO
       * /A21 * /A22 * /A23 * /A24 * /A25                  ; buffers

       + /A16 * A17 * A18 * A19 * /A20                     ; EXXXX BIOS
       * /A21 * /A22 * /A23 * /A24 * /A25 * /AUX2

       + A16 * A17 * A18 * A19 * /A20                      ; FXXXX BIOS
       * /A21 * /A22 * /A23 * /A24 * /A25 * /AUX2

       + A31                                               ; POWER ON RESET

SLEADS __ := LEADS __                          ; SYNC IT
DSLEADS __ := SLEADS __                        ; DELAY IT
EADS __ = /SLEADS __ * DSLEADS __              ; OUTPUT SHORT (1 CLK LONG) EADS __
```

4. To control the cache, the configuration equations for PLD U_3 allow up to 16 non-cacheable areas of 32 kbytes each to be mapped in the cache.

the i486 adapter show that the in-phase operation of the chip set depends on the recognition of RESET2 as low at the third rising edge of CLK2IN *(Fig. 2b)*. Care must be taken to avoid the possible race condition that can arise between the second rising edge of CLK2IN and RESET2.

When the 486CLK is used as the clock input to U_{5A} (half of a 74F74 dual flip-flop), it imposes a minimum propagation delay requirement on the combination of U_{5A} and U_{6A} (a 74ACT11004 inverter). The RSTDRV signal must not propagate through the combination of U_{5A} and U_{6A} in less than 6 ns.

If it does, RESET2 might appear low at the VL82C330 on the wrong edge of CLK2IN. Proper operation is guaranteed by the circuits as shown. There is a temptation, however, to replace the U_{5A}-U_{6A} combination with one ACT74 flip-flop. An ACT74 will, however, violate the 6-ns minimum propagation delay requirement, and the VL82C330 may then sample its reset line as low on the wrong edge of CLK2IN.

```
; THIS PLD GENERATES THE SYSTEM BYTE ENABLES, IT ALSO LATCHES
; BLKA20 DURING HOLD.
; ALL BYTE ENABLES ARE FORCED ACTIVE ON MEMORY READ CYCLES FROM A CACHEABLE
; AREA. THIS IS TO PREVENT CACHING INVALID DATA.

CHIP U2 PAL16L8
;1      2       3       4       5       6       7       8       9       10
PBE0 _  PBE1 _  PBE2 _  PBE3 _  KEN _   WR      BLKA20 _ HLDA   RESCPU  GND
;11     12      13      14      15      16      17      18      19      20
486CLK  ADS _   LATCHA20 _ MADS _ PMIO  BE0 _ BE1 _ BE2 _ BE3 _ VCC

EQUATIONS
/BE0 _ = /PBE0 _                          ; FORCE BYTE ENABLES LOW IF
       + PMIO * /WR * /KEN _              ; MEMORY READ.
                                          ; DO NOT FORCE FOR UNCACHEABLE
                                          ; AREA.

/BE1 _ = /PBE1 _
       + PMIO * /WR * /KEN _

/BE2 _ = /PBE2 _
       + PMIO * /WR * /KEN _

/BE3 _ = /PBE3 _
       + PMIO * /WR * /KEN _

BE0 _.TRST = /HLDA * /RESCPU              ; GET OFF THE LINE DURING HOLD
BE1 _.TRST = /HLDA * /RESCPU              ; OR RESET.
BE2 _.TRST = /HLDA * /RESCPU
BE3 _.TRST = /HLDA * /RESCPU

LATCHA20 _ = /HLDA      * BLKA20 _        ; LATCH BLKA20 SIGNAL ON HLDA SINCE
           +  HLDA      * LATCHA20 _      ; CHIPSET WILL DEASSERT IT DURING HOLD.
           +  BLKA20 _  * LATCHA20 _

MADS _ = ADS _ + 486CLK
```

5. The set-up equations for PLD U_2 (which handles the byte-enable control) let the chip generate the proper system Byte Enable signals and latch the BLKA20 line during Hold.

If, for other reasons, the ACT74 flip-flop must be used, it must be clocked with CLKSYN instead of 486CLK. Out-of-phase operation between the CPU and chip set can be easily identified by observing the CPU's READY input and Address Strobe (ADS) output. There will be no significant (< 10 ns) overlap time when both signals are low if the CPU and chip set are operating in phase. Critical timing exists in virtually every path found in this interface, therefore device substitutions should not be made without careful timing analysis.

Because the i486 and the chip set operate off different clock signals (the i486 clock is half the frequency of the chip set clock), the skew between these two signals must be minimized—that's the job of PLD U_4. A number of equations are used to configure the PLD, a 16R4-7 *(Fig. 3)*. The 16R4 generates CLKSYN and CLK2SYN with typically less than 1 ns of skew. The clocks are buffered, inverted twice by four inverters from U_6 to avoid duty cycle distortion, and converted to CMOS levels for the chip set.

The clock stability requirement precludes using the turbo-mode clock switching function that's supported by the chip set. Switching between turbo and non-turbo modes dynamically switches the clock frequency and will cause the i486 to crash. In most applications, however, the slower, non-turbo mode isn't used. As a result, little is lost by not having the option of slowing down the CPU.

Floating-point error handling is also controlled by U_4. When a numeric error occurs, the i486 asserts FERR. That signal causes U_3 to activate the signal ERRORNPX, which in turn causes an interrupt number 13 to be generated by the VL82C330. The interrupt service routine clears the interrupt by writing to port F0 (h). This causes U_4 to drive the IGNNE signal active (low). Now the processor ignores non-control floating-point instructions until FERR goes high in response to software clearing the numeric error (for example, executing a FINIT instruction).

To support the cache, the simpler implementation employing a PLD will be used. A 22V10 (U_3) was selected and it monitors the address bus and generates the KEN signal. The 22V10 proved to be the best choice because it has the necessary input width and speed. With the accompanying configuration equations, the circuit can create up to 16 non-cacheable areas of 32-kbytes each *(Fig. 4)*.

The address invalidation signal (EADS) is generated when a memory write occurs during a processor hold state, such as a DMA write. Fortunately, this method works because the chip set drives the address back to the processor. Since the processor suspends internal operation during invalidation cycles, the EADS signal is shortened to one clock cycle, improving CPU performance. Address lines A_{26-31} are pulled down during non-CPU cycles because they're not driven by the chip set. Passive or active pull-down can be used on these lines. Passive pull-downs are adequate for most applications because the i486 will only drive these address lines high when it's fetching its reset

TABLE 1: COMPARISON OF 80386DX VS. 80486 THROUGHPUT

Benchmark	80386	80486	Increase
Landmark 1.14	38	149	292%
Norton S1	33.2	50.7	53%
QAplus Dhrystones	6500	22,700	249%

Note: Comparison is based on i486 and 80386 33-MHz systems using Topcat chip set. Norton SI is heavily biased toward write operations and therefore shows the lowest performance improvement.

vector. After vectoring to the BIOS boot code, the i486 will drive these lines low.

In addition, resetting the processor causes the cache to be flushed and disabled. Therefore, active pull-downs should be used if the processor drives any of these upper address lines when the cache is enabled. If the system uses a Weitek coprocessor, the i486 will drive A_{31} high when performing coprocessor cycles. If the next cycle is a DMA write cycle, the passive pull-downs may not be able to bleed off the voltage stored in board capacitance quickly enough. Active pull-downs that are enabled during DMA write cycles would ensure that the correct address is invalidated.

Lastly, a 16L8 PLD (U_2) can be used to resolve the byte-enable control problem. This PLD forces all Byte Enable lines low during memory read cycles that are to cacheable areas. Performance would be degraded if all memory reads, including those to noncacheable areas, were forced to be 32-bit reads. The Byte Enable outputs of this PLD are three-stated during hold and reset cycles to prevent bus contention. A number of equations are required *(Fig. 5)*.

A timing analysis of the critical path for byte-enable timing shows that the byte-enable timing specifications are satisfied for the VL82C330. Byte Enables are sampled by the VL82C330 halfway through the T2 phase, and a 4-ns setup time is required. The setup time permits 1.5 cycles (T1 plus half of T2) or a total of 45 ns for the decoding. Allowing 16 ns for the i486's delay for address and Byte Enables, 15 ns for $\overline{KEN}$ generation, 7.5 ns for the byte-enable PLD propagation delay, 4 ns for VL82C330 setup time, and 2 ns of CPUCLK to CLK2IN skew leaves a byte-enable timing margin of 0.5 ns, worst case.

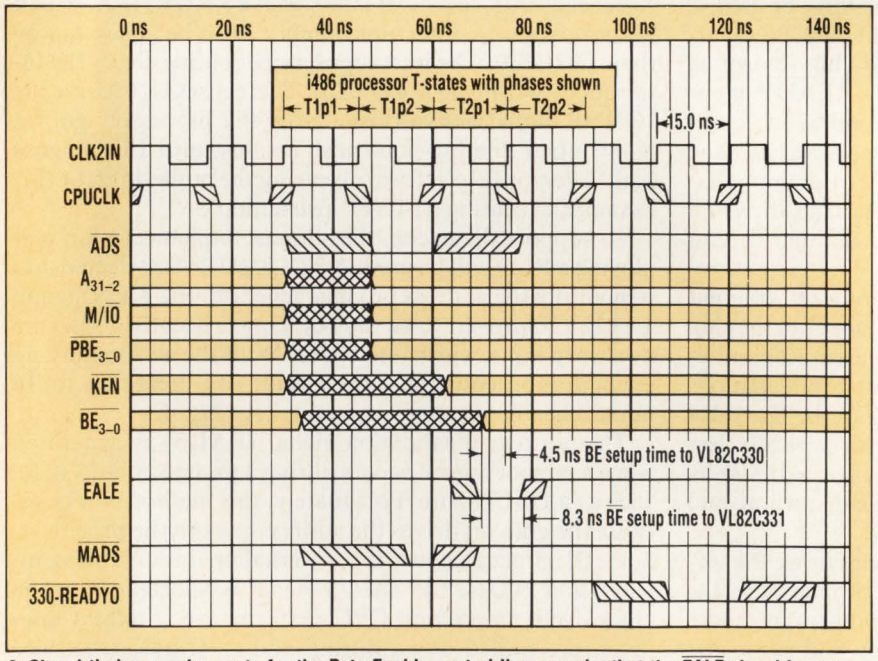
However, worst-case byte-enable timing to the VL82C331 results in a negative timing margin if the i486's $\overline{ADS}$ signal drives the VL82C331's $\overline{EALE}$ pin. The delay information can be derived from the following calculations:

+30.0 ns ADS falling edge to ADS rising edge
−13.0 ns worst case address and Byte Enable lines valid (16-3)
−15.0 ns $\overline{KEN}$ generation/PLD propagation delay
− 7.5 ns Byte-enable fixup PLD propagation delay
− 4.0 ns VL82C331 setup time
− 2.0 ns CPUCLK to CLK2IN skew

= −11.5 ns Byte-enable timing margin to VL82C331.

The difficulty with this initial proposal is that $\overline{ADS}$ may return to the high state as soon as 3 ns after the start of the T2 state. In the worst case, the address and Byte Enable lines may not be valid until 16 ns after the start of T1.

So, instead of a worst-case analysis, a "common parts" analysis should be used. One useful assumption is that the maximum time difference between $\overline{ADS}$ low and address valid is 6.5 ns (1/2 the maximum difference of 16 ns − 3 ns). However, even with this method, the adapter is still 5 ns shy of meeting specification.



6. Signal timing requirements for the Byte Enable control lines require that the $\overline{EALE}$ signal be synthesized from the ADS and 486CLK signals. The $\overline{EALE}$ signal delays the point at which the VL82C331 samples the Byte Enable signals, ensuring that the setup time specification is satisfied.

The solution is to generate an $\overline{EALE}$ signal whose rising edge is guaranteed to occur near the middle of the T2 state *(Fig. 6)*. That can be done by clocking "ORed" $\overline{ADS}$ and 486CLK through a flip-flop. The clock for the flip-flop is the CLK2IN signal. Stepping through the worst-case timing numbers for the generated $\overline{EALE}$ signal appears as:

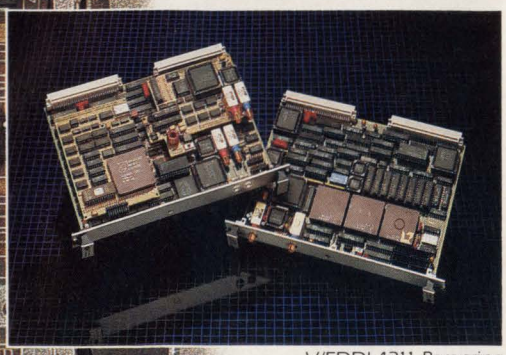
+30.0 ns T1 state, width
+15.0 ns 1/2 of T2 state
+ 3.8 ns Minimum low-to-high propagation delay of 74F74
−16.0 ns Maximum i486 address-valid delay
−15.0 ns $\overline{KEN}$ generation PLD propagation delay
− 7.5 ns Byte-enable fixup-PLD delay
− 2.0 ns CPUCLK to CLK2IN skew

=+8.3 ns available $\overline{BE}$ setup time

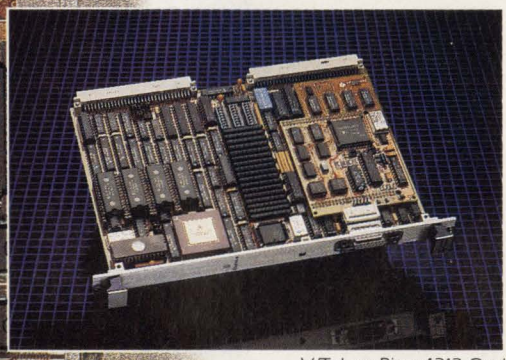
− 4.0 ns VL82C331 setup time

=+4.3 ns Byte-enable timing margin

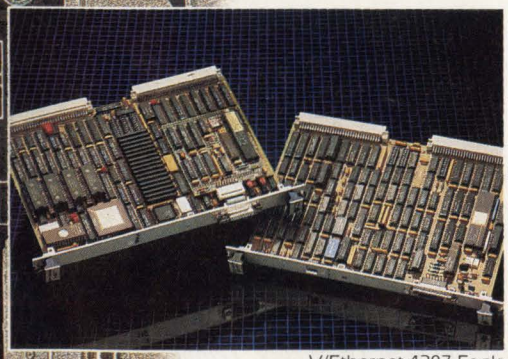
NETWORKING SOLUTIONS



V/FDDI 4211 Peregrine
V/FDDI 3211 Falcon



V/Token-Ring 4212 Owl



V/Ethernet 4207 Eagle
V/Ethernet 3207 Hawk

FDDI, TOKEN-RING AND ETHERNET COMMUNICATIONS

The need to network has never been greater. Diverse processing platforms, distributed architectures, client-server, departmental and workgroup environments all contribute to increased demands on the network. System and network designers need a proven source of technology solutions for the wide range of networking and communication application problems they face.
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Interphase's FDDI 100 Mb/s offerings are a logical choice for the industry. The V/FDDI 3211 Falcon received *UnixWorld* magazine's Product of the Year designation and was the industry's first 6U VMEbus FDDI solution. Interphase's newest FDDI product is the V/FDDI 4211 Peregrine, a RISC-based high-performance node controller capable of link level operation or on-board protocol processing. The Peregrine provides single or dual attach configurations, with SMT (Station Management Software) running on-board, all in one 6U VME slot.

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The V/Token-Ring 4212 Owl is an ultrafast Token-Ring node controller based on the partitioned architecture of Interphase's proven Eagle class of controllers. The Owl facilitates connectivity of UNIX® systems, workstations, supercomputers or any other VMEbus system into an IBM® environment using IEEE 802.5 Token-Ring. This multiple processor design provides an elegant queued interface to the system supporting IEEE 802.2 LLC, and a flexible 4 or 16 Mbit interface to the Token-Ring network.

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Interphase also offers two Ethernet design options. The V/Ethernet 4207 Eagle 32-bit protocol platform is the high-performance standard for the industry, and offers on-board TCP/IP support. The V/Ethernet 3207 Hawk is designed specifically for cost-sensitive VMEbus applications.

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CIRCLE 115

■ RUN 80486 WITH 80386 CHIP SET ■

TABLE 2: SIGNAL CONNECTIONS FROM ADAPTER TO 80386 HOST

Adapter side	Host system side
A_{2-31}	VL82C330 A_{2-26}, A_{29}, A_{31}
	VL82C331 A_{2-25}
D_{0-31}	VL82C332 D_{0-31}
$\overline{ADS}$	VL82C330 pin 27
$W/\overline{R}$	VL82C330 pin 24
$D/\overline{C}$	VL82C330 pin 25
$M/\overline{IO}$	VL82C330 pin 26
$\overline{BE_3}$	VL82C330 pin 20
	VL82C331 pin 69
$\overline{BE_2}$	VL82C330 pin 21
	VL82C331 pin 70
$\overline{BE_2}$	VL82C330 pin 22
	VL82C331 pin 71
$\overline{BE_0}$	VL82C330 pin 23
	VL82C331 pin 72
$\overline{EALE}$	VL82C331 pin 83
TCLK2	VL82C330 pin 44
CLK2	VL82C330 pin 32
CLK2IN	VL82C330 pin 30
RSTDRV	VL82C331 pin 122
RESET2	VL82C330 pin 111
RESCPU	VL82C330 pin 36
RESNPX	VL82C330 pin 41
$\overline{TCReady}$	VL82C330 pin 34
INTR	VL82C331 pin 75
NMI	VL82C331 pin 76
$\overline{MEMW}$	VL82C331 pin 35
$\overline{ERRORNPX}$	VL82C330 pin 43
HRQ	VL82C330 pin 40
HLDA	VL82C330 pin 28
AUX_1	VL82C330 pin 41
AUX_2	VL82C330 pin 50
AUX_3	VL82C330 pin 49
$\overline{BLKA20}$	VL82C330 pin 94
$\overline{BUSYNPX}$	VL82C330 pin 42
$\overline{BUSYCPU}$	VL82C330 pin 38

to VL82C331

In an actual 80386DX system, there will be more connections between the i486 adapter than those discussed. Of course, all of the address and data lines must be connected, as well as many other signal lines to tie all of the logic together. Table 2 shows the mapping of signals from the Topcat chip set to the i486 adapter. Signals on the system side may have many connections to devices within the system, and aren't necessarily connected only to the adapter.

Brian Dellacroce, systems engineer for the Personal Computer Products Division of VLSI Technology Inc., holds a BSEE from Arizona State University, Tempe.

HOW VALUABLE?

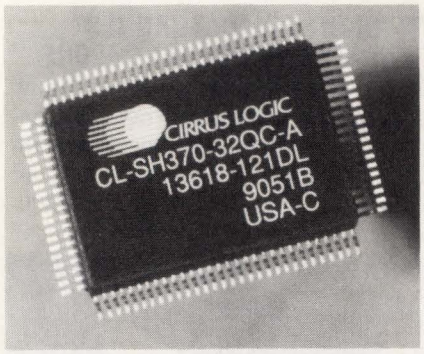
HIGHLY	CIRCLE 523
MODERATELY	CIRCLE 524
SLIGHTLY	CIRCLE 525

▼ RAISE DISK PERFORMANCE USING FEWER CHIPS

As hard disk drives become smaller and more intelligent, designers look for ways to reduce space and power demand while increasing performance. Two SCSI (Small Computer Systems Interface) disk controllers from Cirrus Logic Inc., the CL-SH370 and the CL-SH351, do just that.

In one chip, the SH370 contains most of the hardware that's needed to build a complete SCSI Winchester disk-drive controller subsystem. It's suitable for the 3-1/2- and 2-1/2-in. drives incorporated into the smaller footprint workstations and laptop and notebook PCs.

The SH370 automates many functions that would usually require a local microprocessor. For this reason, designers can eliminate one of the two local embedded processors that typically were needed to control a disk drive, as well as the circuitry needed to execute the functions. In addition, the chip supports zone-recording formats and a proprietary split data-field capability that increases the areal density of data on the drive's media. This nearly doubles the drive's capacity without changing the media or head technology. To compensate for the inherently higher error rates created by higher densities, the IC incorporates the company's proprietary Reed-Solomon on-the-fly error-correction technology.



The SH351 controller is a socket- and firmware-compatible upgrade of the company's SH350 controller. With a 10-Mbyte/s synchronous SCSI-2 transfer rate and a 32-MHz disk-transfer rate, the SH351 implements the "fast" data transfer of the SCSI-2 standard. It's intended for such applications as workstations and minicomputers.

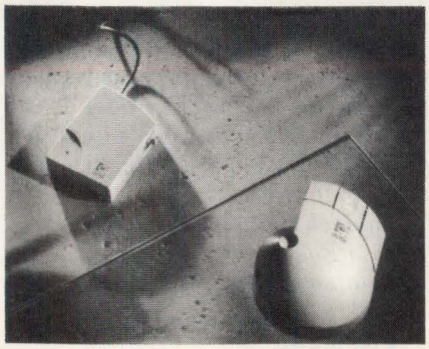
The SH351 includes support for embedded servo designs and zone-recording formats. It's speed-matching capabilities permit up to 15-byte synchronous transfer offsets and 13 programmable transfer periods.

Both disk controllers are housed in 100-lead quad flat packs. Both are available now in sample quantities, with production starting in the second quarter. The SH370 goes for $22 in quantities of 100. The SH351 costs $20 in similar quantities.

Cirrus Logic Inc.
1463 Centre Pointe Dr.
Milpitas, CA 95035
(408) 945-8300
▶ **CIRCLE 336**

▼ MOUSE LOSES ITS CORD

With the introduction of Logitech's cordless mouse, the MouseMan Cordless Radio Mouse, users are no longer restricted by the constraints of corded input devices. Eight adjustable channel settings on the receiver enable the mouse to be operated simultaneously by multiple users working within the device's 6-ft. range, with no interference from other units. The MouseMan doesn't require direct line-of-sight communication with its receiver, which can be positioned anywhere within the transmission range. It also features standby and sleep modes to prolong the one-year (or so) battery life. The mouse's resolution is 400 dots/in. The cordless MouseMan, which is fully compatible with Microsoft Windows 3.0, costs $199.

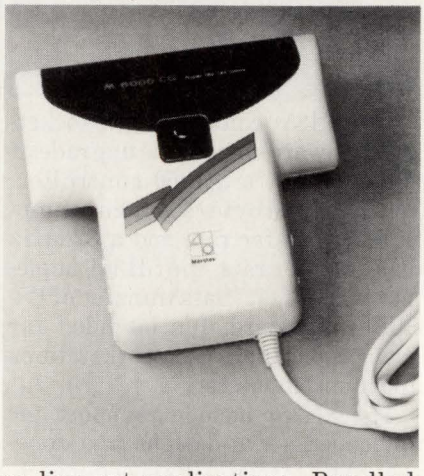


Logitech Inc.
6505 Kaiser Dr.
Fremont, CA 94555
(415) 795-8500
▶ **CIRCLE 337**

PC DESIGN PRODUCTS

▼ 18-BIT COLOR SCANNER DISPLAYS 262,144 COLORS

PC and Macintosh users can now scan in 18-bit-color or gray-scale images. The M-6000CG boasts an 18-bit/pixel display resulting in 262,144 colors. The scanner also supplies 400-dot/in. gray-scale resolution for text



or line-art applications. Bundled software includes a high-end color paint-imaging package as well as optical-character recognition. Available now, the PC version costs $695, while the Macintosh version sells for $795.

Marstek Inc.
17795-F Skypark Cir.
Irvine, CA 92714
(714) 833-7740
▶ **CIRCLE 338**

▼ PRINTER FITS UNDER NOTEBOOK PC

As more and more laptops are being sold, users need printers with a similar footprint. Enter the LT-20 dot-matrix printer. It's designed to fit under a notebook-style laptop with its flat-sheet feed design. The low-profile printer measures 14.6 by 11.3 by 2 in. and weighs 5.9 lbs. It comes with a 50-sheet cassette tray. Powered by a rechargeable NiCd battery, the LT-20 printer can print 100 pages on one 10-hour charge. A car-battery adapter and a font ROM with eight fonts are also available. The printer's MTBF is rated at 4000 hours, excluding the printhead, which is rated at 50 million characters. The LT-20 sells for $499.

Seikosha
10 Industrial Ave.
Mahwah, NJ 07430
(201) 327-7227
▶ **CIRCLE 339**

▼ INPUT DEVICE MIGRATES TO KEYBOARD

With all of the new Windows 3.0 applications being developed, users find that an input device, such as a mouse or a trackball, is a necessity. The MouseBoard puts an alternate input device right on the keyboard, so an external pointer isn't needed. Positioned where the directional keys would sit on typical AT-style keyboards, the MousePanel does the job of a mouse and directional keys. Hitting a "mouse" key switches between the mouse and the directional keys. Cursor movements are controlled by gliding movements on the panel. The keyboard also comes with a software driver and a paint application. It works with IBM PC/XT/AT, PS/2, and compatible computers. It's also compatible with all Microsoft protocols. Click-type keys are available on request.

Cherry Electrical Products Corp.
3600 Sunset Ave.
Waukegan, IL 60087
(708) 662-9200
▶ **CIRCLE 340**

▼ CONNECT MIL HARDWARE TO PCs

Designed to connect Navy tactical data systems to personal computers, the Eagle interface board fits right into a vacant slot in a PC. With the board, military-systems integrators can develop, monitor, simulate, and test military software systems without the lengthy lead times and high prices of military hardware. The board can even be installed in a laptop computer for field applications. The Eagle is fully compliant with MIL-STD-1397, types B and C. It features full-duplex 32-bit I/O support. The board features MS-DOS resident drivers and it interfaces to high-level languages. Eight software-selectable data rates range from 1.2 to 25.6 μs per transfer. The board contains a built-in test feature for self-diagnosis. Up to 32 Eagle boards can reside in a system. The Eagle board is priced at $4050 with large-quantity discounts available. Delivery is from stock to four weeks.

Sabtech Industries Inc.,
5411 East La Palma Ave.
Anaheim, CA 92807
(714) 970-5311
▶ **CIRCLE 341**

▼ 3.5-IN. DAT DRIVE HOLDS 5 GBYTES

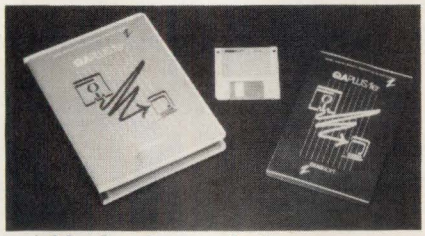
The Model 3600 DAT (digital-audio-tape) drive holds 5 Gbytes of data in a 3.5-in. form factor. The drive features a sustained transfer rate of 520 kbytes/s. The high capacity is achieved by combining hardware-based data compression with long-

length tapes. Another feature of the drive is its high reliability—60,000 hours. This is done by reducing the chip count and using just one board. The 3600 uses a vertical hub assembly that assures a reliable cassette engagement and disengagement. The drive costs under $1400 in OEM quantities and is available now.

WangDAT Inc.,
151 Kalmus Dr., K-3
Costa Mesa, CA 92626
(714) 241-9613
▶ CIRCLE 342

▼ LOCATE AND DIAGNOSE A PC'S HARDWARE PROBLEMS

By using QAPlus/fe-tech, advanced PC end users or field technicians can test all of their major hardware components, including floppy and fixed disks and I/O ports. The software



quickly locates and diagnoses any problems. QAPlus/fe-tech can be used with IBM PC/XT/AT, PS/2, and compatible computers. It contains interactive testing capabilities that let users evaluate a computer's keyboard, mouse, joystick, or audio speaker. The software can also diagnose faulty RAM chips. QAPlus/fe-tech is priced at $499.95.

DiagSoft Inc.
5615 Scotts Valley Dr., Suite 140
Scotts Valley, CA 95066
(408) 438-8247
▶ CIRCLE 343

TINY SPDT SWITCHES
ABSORPTIVE... REFLECTIVE

dc to 4.6GHz from $32.95 (10-24)

Tough enough to pass stringent MIL-STD-883 vibration, shock, thermal shock, fine and gross leak tests... useable to 6GHz... smaller than most RF switches... Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

Switch fast... to Mini-Circuits' GaAs switches.

SPECIFICATIONS

Pin Model / Connector Version	KSW-2-46 / ZFSW-2-46		KSWA-2-46 / ZFSWA-2-46	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	**$32.95**		**$48.95**	
	$69.95		**$79.95**	

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CIRCLE 521 MODEL THERMISTOR WITH SPICE

JIM HAGERMAN
5137 Camino Playa Malago,
San Diego, CA 92124; (619) 931-5012.

With this Spice subcircuit, a typical resistive component can be replaced by a two-terminal thermistor in Spice simulations *(Fig. 1)*. Most Spice-based simulators permit a temperature-dependent model of a resistor. However, the model is limited to a second-order polynomial that may not result in an accurate model of the actual component's characteristic, especially over a wide temperature range.

To overcome this problem, the subcircuit uses the high-order polynomial description of the nonlinear voltage-controlled current source. In this way, any polynomial (of nth degree) that describes the thermistor's resistance as a function of temperature can be applied directly in Spice. There are several known methods for generating these polynomials, and numerous easy-to-use software packages can simplify this task.

The model's accuracy is mostly limited by the accuracy of the polynomial. Using TableCurve 2.0 from AISN Software, Grants Pass, Ore., two polynomials were generated to model the data listed for a Dale Electronics negative-temperature coefficient (NTC) curve #1 from 0 to 100°C. The results for the two polynomials indicate good correlation with the expected data *(Figs. 2a and 2b)*.□

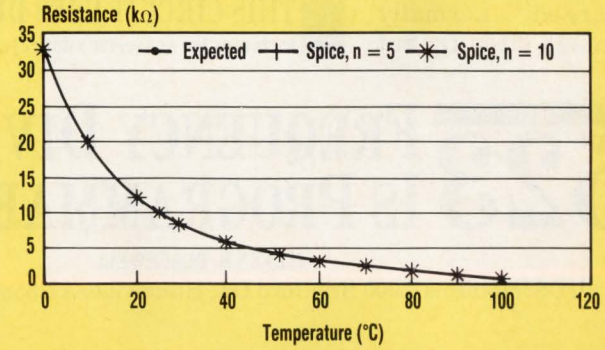
```
*  NTC.SUB     Jim Hagerman 7/5/90
*
*  This is a model of a 10k Ohm thermistor with characteristics of a Dale Electronics NTC
   curve #1.
*
*  The nominal value of resistance at 25C is Rref.
*
*  The characteristics R(T) is used for Gout. Note that if Celsius is used TNOM is set to
   zero.

.options tnom=0
.subckt ntc 1 2
   Eout 1 3 poly(2) (5,0) (4,0) 0 0 0 0 1.0
   Vsense 3 2 dc 0.0
   Fout 0 4 Vsense 1.0
   Rref 4 0 10k
   Gout 0 5 poly(1) 6 0 3.266
   +                -0.16633619
   +                 0.0046450693
   +                -8.6856965e-5
   +                 1.017213e-6
   +                -3.8668603e-9
   +                -8.8615615e-11
   +                 1.678045e-12
   +                -1.3013017e-14
   +                 4.8617031e-17
   +                -6.8866237e-20
   Ro 5 0 1.0
   Itemp 0 6 dc 1.0
   Rt 6 0 Rtemp 0.001
   .model Rtemp res(r=1 tc1=1000)
.ends ntc
```

1. THIS SPICE SUBCIRCUIT serves as a model of a 10-kΩ thermistor. When simulating with Spice, the model can be used in place of a normal resistive component.

T	Resistance (kΩ)		
	Expected	Spice	
		n = 5	n = 10
0	32.66	32.63	32.66
10	19.90	19.98	19.90
20	12.49	12.45	12.49
25	10.00	9.949	10.00
30	8.058	8.025	8.058
40	5.326	5.360	5.326
50	3.602	3.652	3.602
60	2.488	2.488	2.488
70	1.751	1.701	1.751
80	1.256	1.229	1.256
90	0.9164	0.9751	0.9164
100	0.6792	0.6597	0.6793

(a)



(b)

2. ACTUAL SPICE SIMULATION results for two different values of n are compared with the expected values (a). A plot of the same data illustrates the model's resistance-temperature curve (b).

VOTE!

Read all the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

CIRCLE 522 INCREASE DC-DC CONVERTER POWER

CARL SPEAROW
Sundstrand Corp., 4747 Harrison Ave., Rockford, IL 61125; (815) 394-3263.

The MAX630 dc-dc converter, which has a fixed 50% duty cycle, achieves regulation by skipping cycles as necessary. This is fine for voltage-doubling applications, but for large step-up ratios, the inductor dumps its energy very quickly and the converter idles for the remainder of the cycle. As a result of this action, output power becomes less than optimal.

This 3- to 15-V converter circuit sidesteps that problem *(see the figure)*. The oscillator circuitry has been modified to increase the duty cycle to 80%.

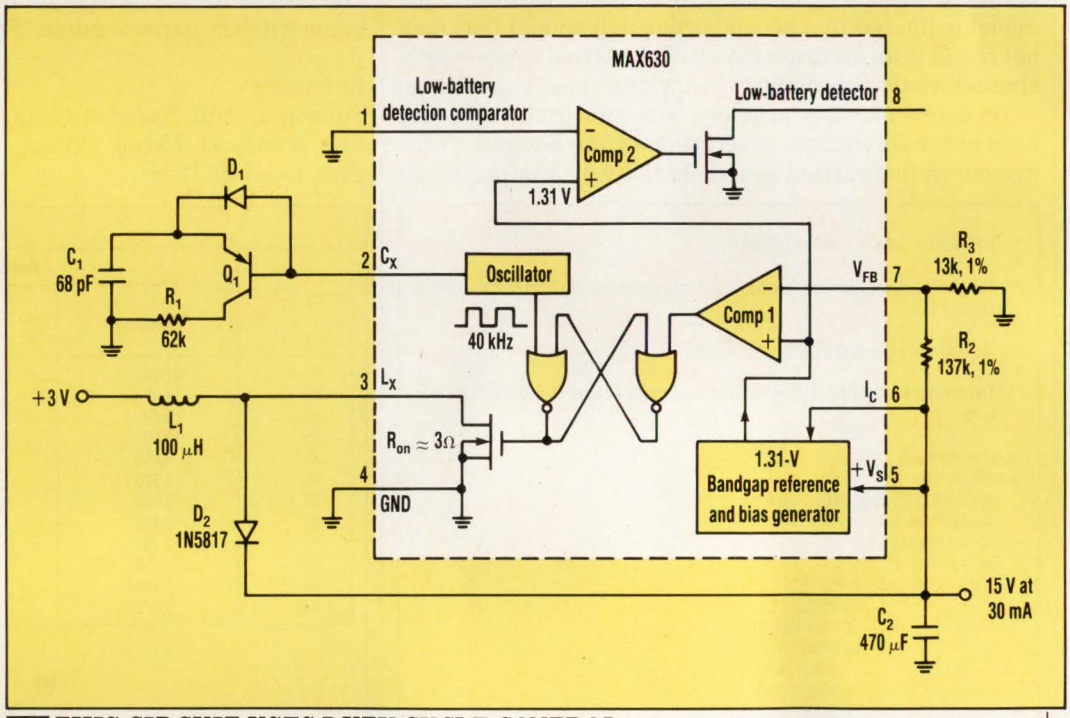
The C_X pin on the MAX630 is a bidirectional current source that's intended to charge and discharge a capacitor to produce a 50% duty cycle. Here, capacitor C_1 is charged normally through diode D_1, but the capacitor is discharged in one-fourth the time through transistor Q_1 and resistor R_1.

The resulting output power rating depends on the tolerances of the component chosen and the input voltage range. But in any case, it's about 1.6 times that of the standard circuit.□

IFD WINNER

IFD Winner for November 8, 1990

James Wong, Analog Devices, Precision Monolithic Div., 1500 Space Park Dr., P.O. Box 58020, Santa Clara, CA 95052; (408) 727-9222. His idea: *"Add Programmable Gain, Attenuation."*



THIS CIRCUIT USES DUTY-CYCLE CONTROL to increase the dc-dc converter power. Q_1 increases the converter's duty cycle by speeding up C_1's discharge by a factor of four.

CIRCLE 523 FREQUENCY DIVIDER IS PROGRAMMABLE

STEVEN R. BLACKWELL
UDS/Motorola, 5000 Bradford Dr., Huntsville, AL 35805; (205) 430-8112.

Frequency-divider circuits are used in a wide variety of devices, and programmable frequency dividers are often required so that these devices can operate in multiple modes. This circuit offers a simple, inexpensive divider that can be programmed to divide by any integer from 2 to 65 *(Fig. 1)*. It employs a variable-length shift register (4557), a D-type flip-flop (1/2 74HC74), and an inverter (1/6 74HC14). The circuit is self-starting, so it doesn't need an external reset and doesn't have any undefined "hang-up" states, unlike many other divider circuits. This is critical in the design of timers that can't be easily monitored and controlled from a processor.

The circuit's operation is illustrated by its timing diagram. The flip-flop's input is connected to the output of the 4557, so the flip-flop simply latches the output of the shift register. The clock phase is inverted between the two devices, enabling their outputs to change on opposite clock edges. The flip-flop's output is fed back into the 4557's reset input. The 4557's serial input is tied high, so each clock pulse shifts another "1"

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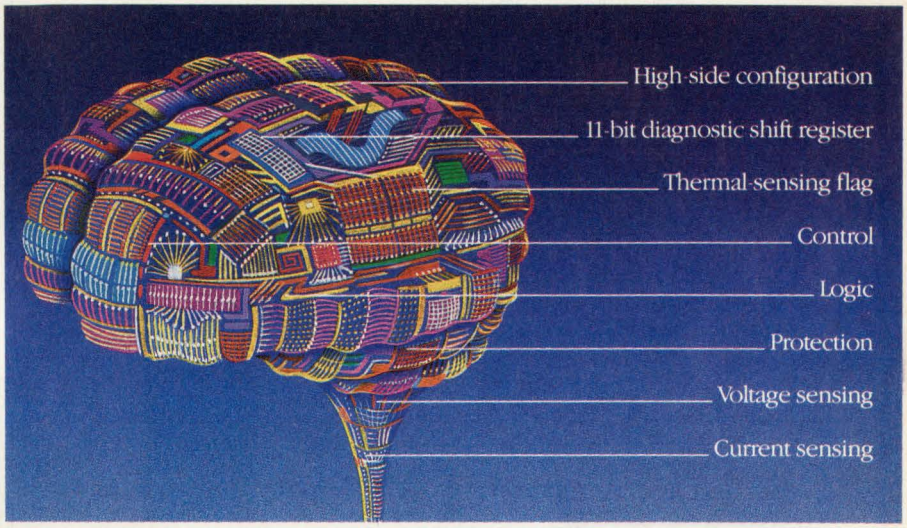

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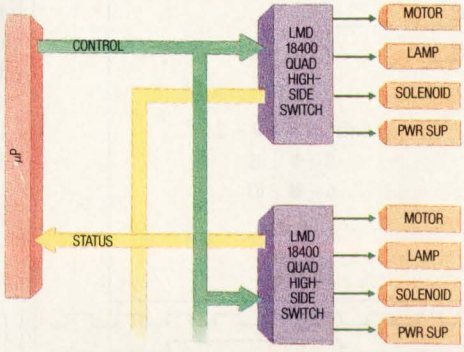

Parallel operation of LMD18400s

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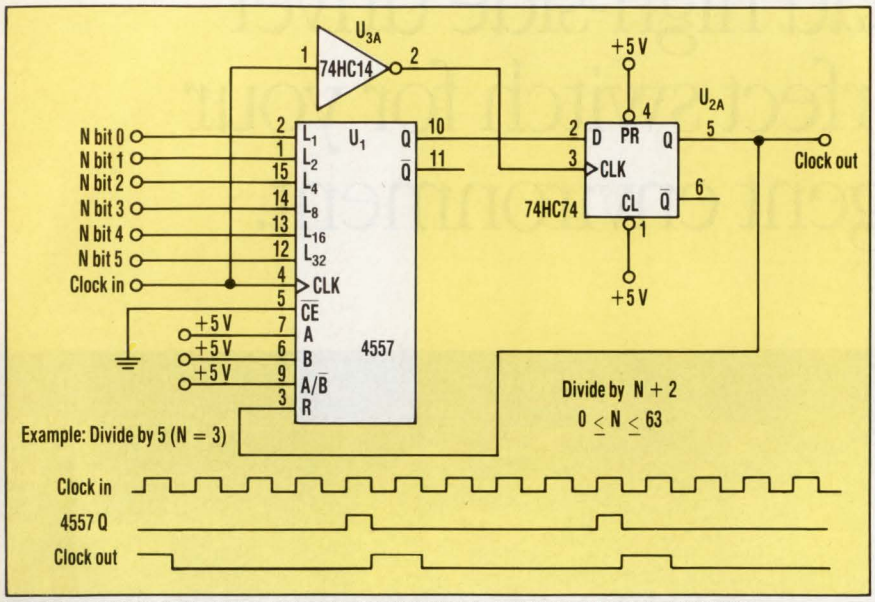
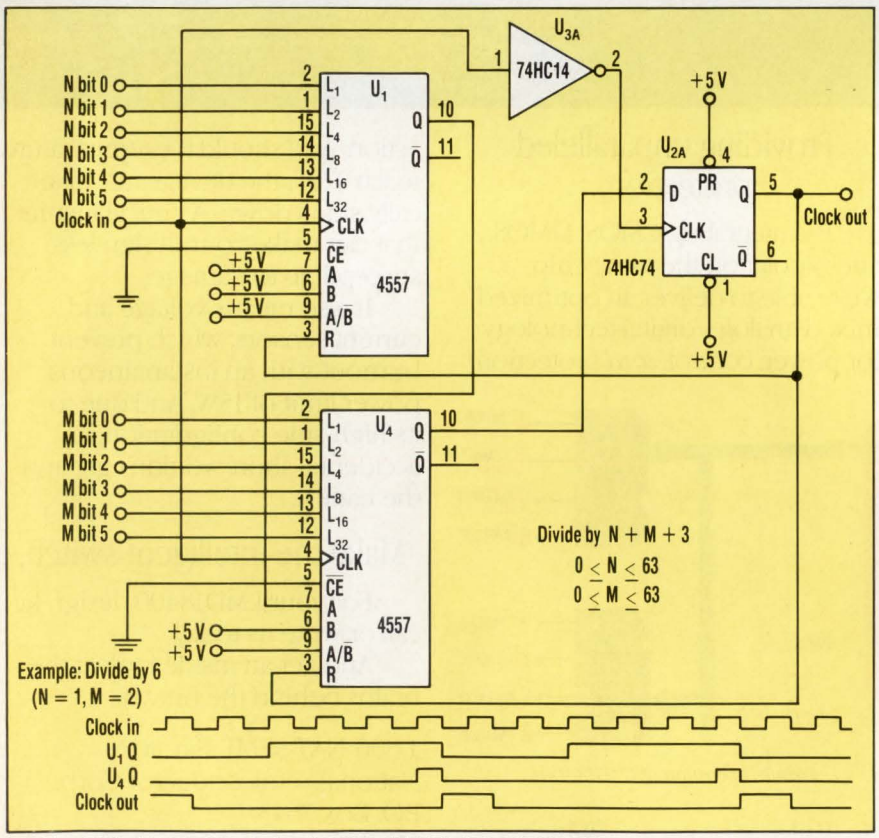


1. THIS SIMPLE, INEXPENSIVE FREQUENCY DIVIDER circuit can be programmed to divide by any integer from 2 to 65. The actual frequency division equals N + 2, where N is from 0 to 63. When N = 3, as shown in the timing diagram, the circuit divides by 5.



2. BY ADDING A SECOND SHIFT REGISTER, the range of programmability can be extended. The first shift register's output is fed into the input of the second. In essence, the two parts act as a single shift register with a length of (N + 1) + (M + 1). The timing diagram shows a division by 6.

into the 4557. N + 1 cycles after the reset pulse is removed, the first 1 will propagate to the shift register's output. The 1 is latched into the flip-flop on the clock's next falling edge and then fed back to the 4557 reset pin, causing the shift register's contents to be set to 0.

The reset is removed when a 0 is clocked into the flip-flop on the next falling clock edge, restarting the process. No external reset is required to start the divider. This is because a 1 will propagate to the shift register's output within the first N + 1 clock cycles to supply the first reset pulse, regardless of the 4557's power-up state.

The length-control inputs (N) of the 4557 set the divide ratio. The shift register will have a length of N + 1, where N can be set to any integer from 0 to 63. One clock cycle is taken for the reset pulse, so the total divide count is N + 2.

Some applications require a symmetrical output clock. An extra flip-flop can be added at the output to perform a divide by 2, producing a symmetric output.

The divider circuit's range of programmability can be easily extended by increasing the shift register's effective length. This is done by adding one or more 4557s *(Fig. 2)*. The output of the first shift register (U_1) is fed into the serial input of the second shift register (U_4), whose output drives the flip-flop. The 4557s' clock inputs are tied together, as are the reset inputs. As a result, the two chips act as one shift register of length (N + 1) + (M + 1). The circuit's divide count is now (N + 1) + (M + 1) + 1, or simply N + M + 3, offering a divide range of 3 to 129. This technique can be extended to any number of shift registers, with each register adding N + 1 to the divide count.□

Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

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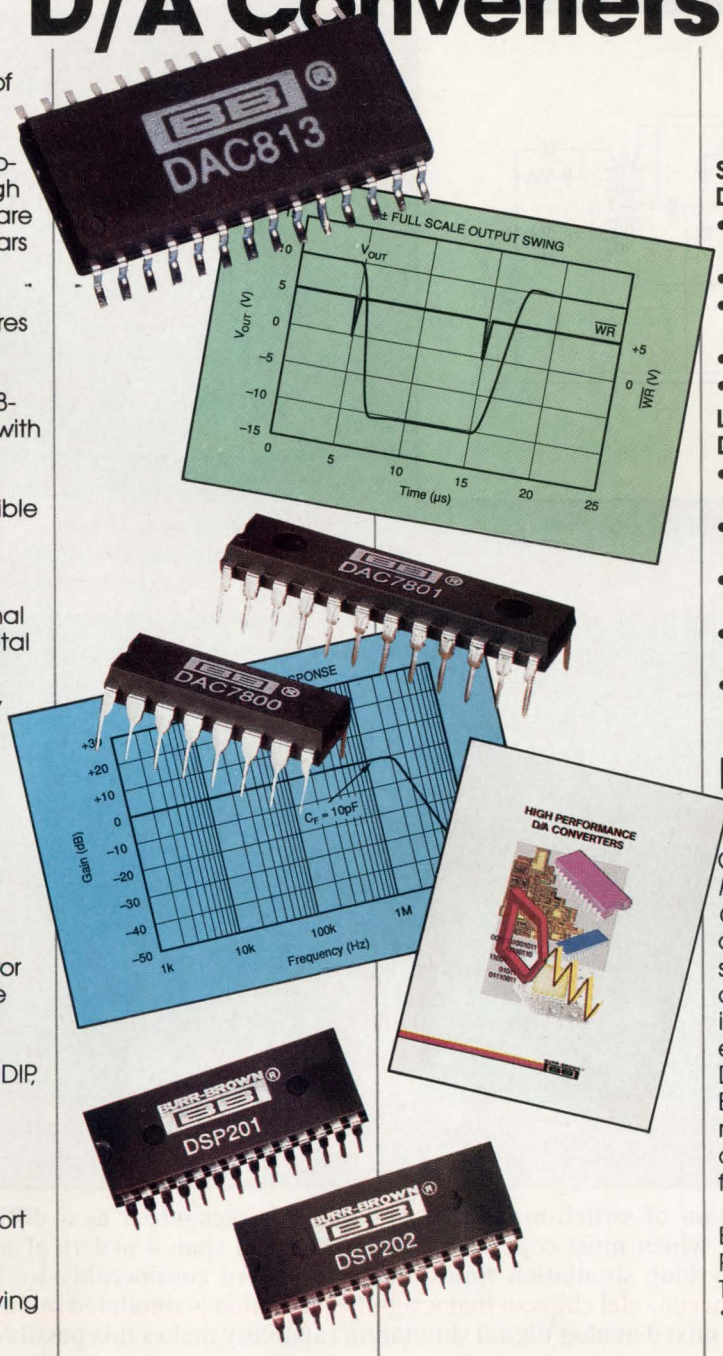

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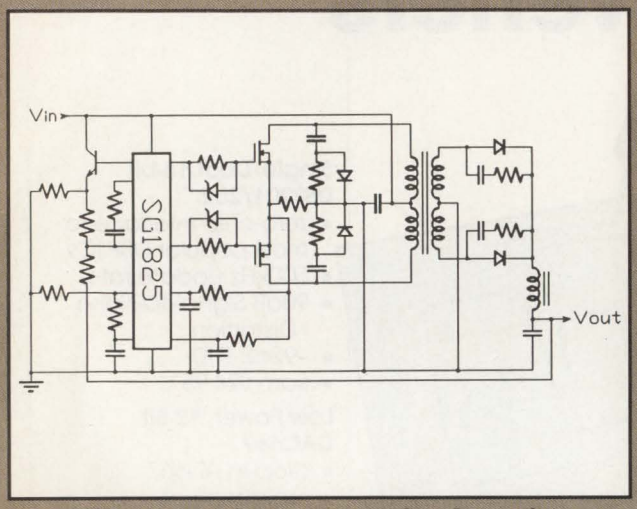
CIRCLE 91

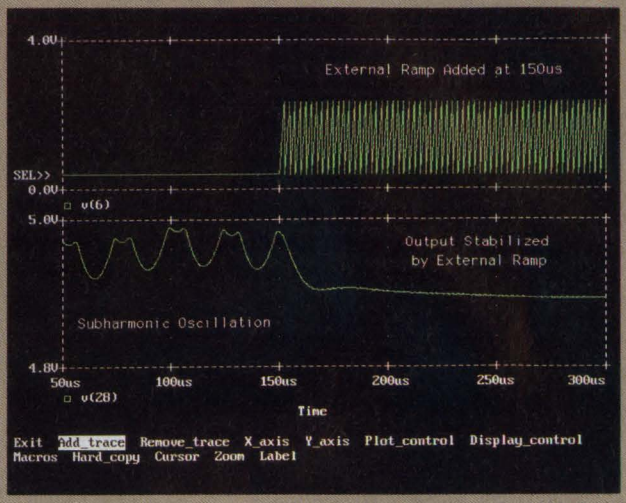
PSpice

MicroSim Corporation

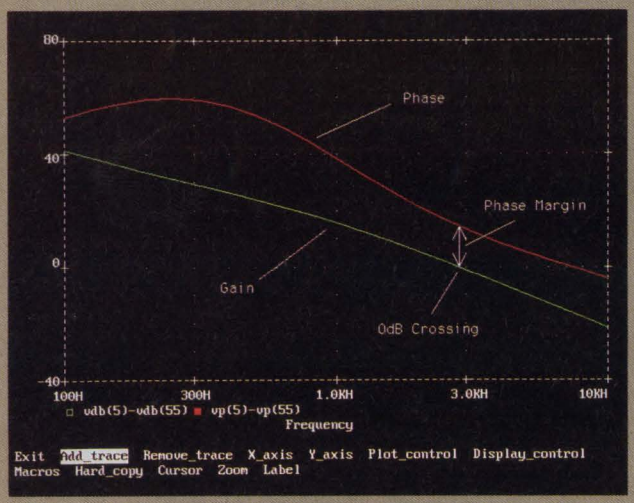
The Standard for Circuit Simulation Switch-Mode Power Supply Design



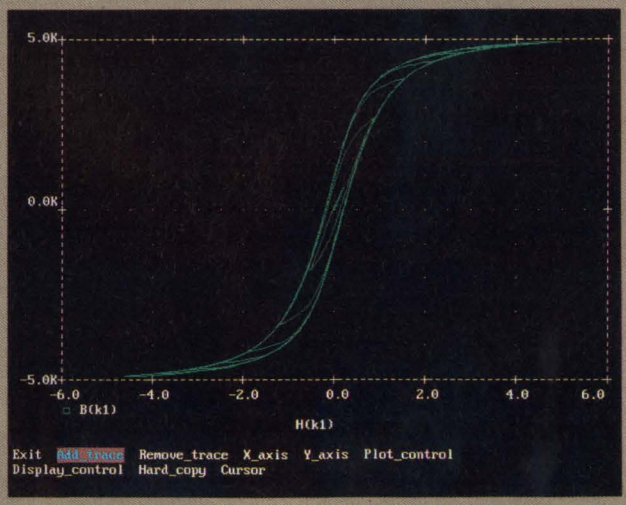
Current mode power supply schematic.



Power supply simulated using mixed analog/digital simulation. Plot shows subharmonic oscillation being suppressed by external ramp.



Simulation using the Vorperian switch model to examine the stability of a power supply.



Hysteresis curve of transformer.

A cycle by cycle simulation of switch-mode power supplies is recognized as a difficult simulation task for SPICE-based simulators, which must cope with timings that can span 4 orders of magnitude. This problem invariably results in very long simulation times, but is improved considerably by MicroSim's approach of building the controller macromodel chips so that a significant section is simulated in the digital domain. PSpice's behavioral modeling and mixed analog/digital simulation capability makes this possible.

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CIRCLE 87

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

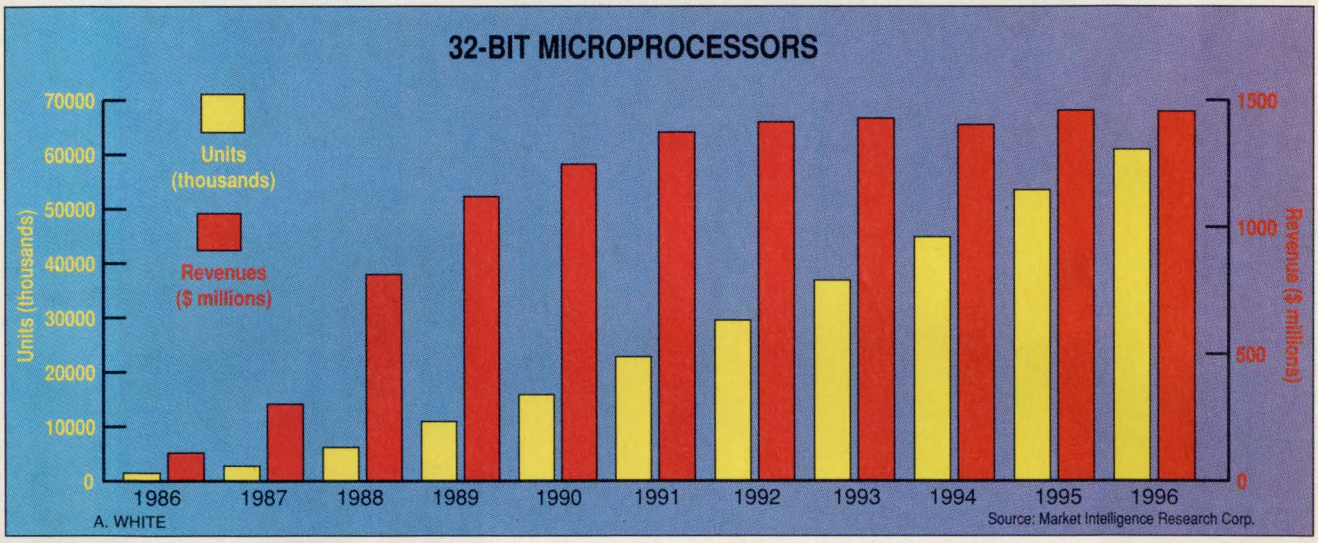
Fueled by brisk demand for RISC chips in workstations, sales of 32-bit microprocessors should amount to $1.37 billion this year, a 10% increase over last year's revenues. This prediction comes from Market Intelligence Research Corp.

Nonetheless, the overall growth rate for 32-bit processors is tapering off, according to the Mountain View, Calif., market researcher. Next year should see just a 3% increase over 1991. Compare that with 1988's revenue increase of 169% over 1987. The compound annual growth rate from 1989 to 1996 is expected to be 3.8%.

The 32-bit processor market is made up of CISC and RISC processors, with the latter showing faster growth. In 1989, revenues for CISC microprocessors amounted to $1.06 billion compared with $60.3 million for 32-bit RISC processors. By 1993, sales in the 32-bit CISC arena will inch up to $1.07 billion vs. $349.5 million for 32-bit RISC processors.

From the performance standpoint, the speed of RISC processors is increasing sharply, from today's 12 MIPS standard to at least 100 MIPS by 1995. Another trend is merging CISC and RISC architectures. Multiprocessing also is enabling vendors to pack more system punch while still relying on standard microprocessors.

As for software, the Unix operating system holds the lead for 32-bit processors, with C as a programming language. Underlying this trend is a growing emphasis on portability and compatibility among systems.



OFFERS YOU CAN'T REFUSE

Entrepreneurs take note: Free software can help you find out if you qualify for a business loan. First Step Review, developed by the National Business Association and the U. S. Small Business Administration, gives an orientation to the SBA guaranteed-loan program. The program asks for information about the applicant seeking the loan, which it evaluates and scores. A score of 70 or above suggests that the applicant has a good chance to receive a loan. With the program, an applicant can do "what-if" analyses to see how the application can be improved. Results include an approximate monthly payment at various interest rates.

Contact the National Business Association, First Step Review Program, P. O. Box 870728, Dallas, TX 75287; (800) 456-0440.

Personal computers drop in value—by up to one-third—the moment they're plugged in. One way around this is to buy used PCs. A brochure, "How to Buy or Sell in the Used Computer Marketplace," is free from the National Computer Exchange, New York, N. Y. The brochure describes the quickest, most convenient way to buy or sell Macintoshes, 386s, 286s, XTs, PS/2s, portables, laptops, Apple II, and laser printers.

For more information, contact NACOMEX, 118 East 25th St., New York, NY 10010; (212) 614-0700; fax (212) 777-1290.

The Cosmic Software Catalog lists abstracts of 1200 scientific programs made available under NASA's Technical Utilization Program. The abstracts explain the program's capabilities and note the programming language, machine requirements, size, and price of the source code and supporting documentation. The printed and microfiche catalogs contain a keyword index; the disk versions have a search menu. Source code is usually included, and educational discounts may apply. The catalog sells for $25 in print or in microfiche; a DOS disk is $30; the international version costs $60. For further information, contact the Cosmic catalog order department at (404) 542-3265; fax (404) 542-4807.

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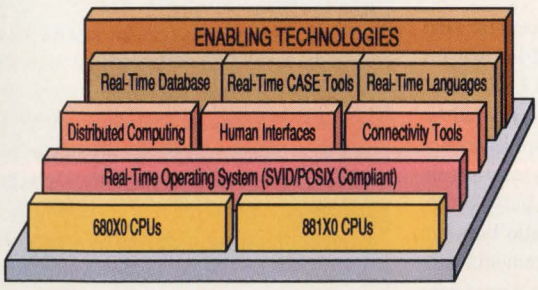

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CIRCLE 95

QUICKLOOK

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *Noise Reduction Techniques in Electronic Systems*, 2nd ed. by Henry W. Ott. Wiley, 1988. ***$47.95.***
2. *Microchip Fabrication*, 2nd ed. by Peter Van Zant. McGraw-Hill, 1990. ***$49.50.***
3. *Art of Electronics*, 2nd ed. by Paul Horowitz and Winfield Hill. Cambridge University Press, 1989. ***$49.50.***
4. *C Language Algorithms for Digital Signal Processing*. Paul M. Embree and Bruce Kimble. Prentice-Hall, 1991. ***$50.***
5. *Principles of Electronic Packaging*. Donald P. Seraphim, Ronald Lasky, and Che-Yu Li. McGraw-Hill, 1989. ***$56.95.***

COMPUTER SCIENCE:

1. *Object-oriented Design with Applications* by Grady Booch. Addison Wesley, 1990. ***$37.25.***
2. *Programming Windows*, 2nd ed. by Charles Petzold. Microsoft Press, 1990. ***$29.95.***
3. *Postscript Language Reference Manual*, 2nd ed. Adobe Systems Inc. Addison-Wesley, 1990. ***$28.95.***
4. *Computer Architecture: A Quantitative Approach* by John Hennessy and David Patterson. Morgan Kaufman, 1990. ***$54.95.***
5. *Introduction to Algorithms* by Thomas H. Corman, Charles E. Leiserson, and Ronald L. Rivest. McGraw-Hill, 1990. ***$49.95.***

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HOT PC PRODUCTS

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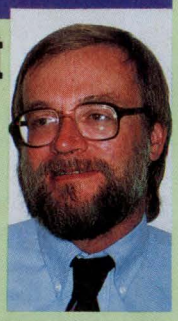
DID YOU KNOW?

. . . that high-tech products that come to market six months late but on budget will earn 33% less profit over five years. In contrast, products that come out on time yet 50% over budget diminish profits by a scant 4%.

McKinsey & Co.

KMET'S KORNER

...Perspectives on Time-to-Market



BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

I struggled with the creation of project models over about 10 years. I tried an assortment of techniques based on a variety of project-management software tools. A major advance, which had nothing to do with the tools I used, materialized in 1985. At that time, I was managing Hewlett-Packard's program to develop the 8770A Arbitrary Waveform Synthesizer. It was a development effort that was taking place in locations scattered across the western United States.

I knew that a model of the entire development effort was absolutely essential for us to achieve our development goals within this distributed, concurrent engineering environment. Armed with an Apple Macintosh 512k loaded with MacProject, I set out singlehandedly to create the model. It took me about two weeks to build an activity network that contained 200 elements. I was working in a paperless environment, going from brain to MacProject. Placing the first 30 or so tasks was easy and fun.

After that, the creation, placement, arrangement, and connection of the remaining 170 elements became quite a chore. With the creation of each task, I had to estimate its duration, assign resources, and establish predecessor and successor relationships. I gave my best effort at doing this for all 200 elements. With data entry complete, I ran a printout from the Imagewriter. A few hours and a few rolls of Scotch tape later, a new layer of wallpaper was decorating my office wall. Of course, seeing the network model in this form for the first time made it necessary to go back and make a few adjustments. When I felt that I had reached the point of diminishing returns, I stopped creating the model and took it out for a reality test.

The model was given to every individual that I had in the resource listing for critical analysis, comment, and revision. I explained to each person why the network looked the way it did. These people explained to me why I was wrong and what I should do about it. It was either get humble or disappear—I chose humility. Then I methodically updated the entire model in about a week, based on the feedback supplied by the project participants. Where things did not look right, I asked responsible people to help me or I called them on the phone to make them a part of the decision process. Trace elements of a shared planning process began to appear.

This revision went out for review by all participants. I took this baseline version of the plan to functional and general management, which fully committed all the resources identified in the plan to execute the project. I now had a model of reality for myself and the entire 8770A new product-development team.

For me, doing the 8770A project with a network model completely eliminated the possibility of ever doing another project without one. It's an essential element in the characterization of the new product development process. However, creating this model taught me a number of valuable lessons for improvement when building a model for my next project/program. And I began to form a clear idea of how to help others model and plan their work.

Ron Kmetovicz will lead a Time to Market seminar entitled "Speeding New Ideas to the Marketplace" at Santa Clara University's Executive Development Center, to be held April 25, 1991. For more information call Elmer Luthman, center director, (408) 554-4521; fax (408) 554-4571.

QUICKLOOK

TIPS ON INVESTING

Futures funds offer engineering investors a way to diversify their portfolios and participate in the world market. Consider typical questions investors might ask:

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A futures fund is a way to participate in a wide variety of financial commodity markets. Such funds offer potential for substantial gain without taking on many of the significant risks often associated with speculative commodity trading.

Q. How are futures funds structured and what do they invest in?

They are structured as limited partnerships where your losses and liability are limited to the amount you actually invest. The funds often invest in traditional commodity markets such as agricultural products and precious metals and energy (for example, crude oil, gasoline, and heating oil). Trading in these markets often allows you to participate in trends that can run counter-cyclical to a declining stock market. This diversification can be beneficial for the traditional portfolio.

Futures funds also invest in the worldwide financial markets such as foreign currencies (the yen and the deutsche mark, for example), international interest-rate instruments, and stock-market indexes.

Q. Who should invest?

Futures transactions often involve substantial risk and aren't suitable for every engineering investor. If you've built a solid portfolio of investments to meet your basic financial needs and can put some risk capital to work, you might consider the futures markets and the limited partnership structure of a futures fund.

Q. Who manages the trading in a futures fund?

As the limited partnership structure of a futures fund limits the risk of trading in commodities, the use of a professional commodity trading adviser (CTA) to manage the money may enhance the potential for returns.

Successful commodity trading requires a full-time commitment to these fast-moving markets. The CTA analyzes markets, develops sophisticated trading strategies, invests the funds assets, monitors positions, and determines when to take a profit or limit a loss.

Q. What is the minimum investment?

For most funds, you may invest as little as $5,000. For retirement plan accounts—IRA and Keogh plans—you may invest as little as $2,000. A portion of the assets also earn interest, an important source of income that helps defray management fees, which are generally 3% to 4% of net assets. In addition, incentive fees are paid to the CTA when the fund makes money. These fees generally range from 10% to 20% of profits for most public funds. Commissions range from 8 to 10% of the fund's trading assets. When considering a futures investment, note that rate of return is usually quoted after these fees and expenses are deducted.

To see if a futures fund is appropriate for your overall portfolio, talk it over with your financial consultant.

Henry Wiesel is a financial consultant with Shearson Lehman Bros, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221, (800) 221-0073 in N.J. Wiesel invites questions and comments from readers.

MICROPROCESSOR SURVEY

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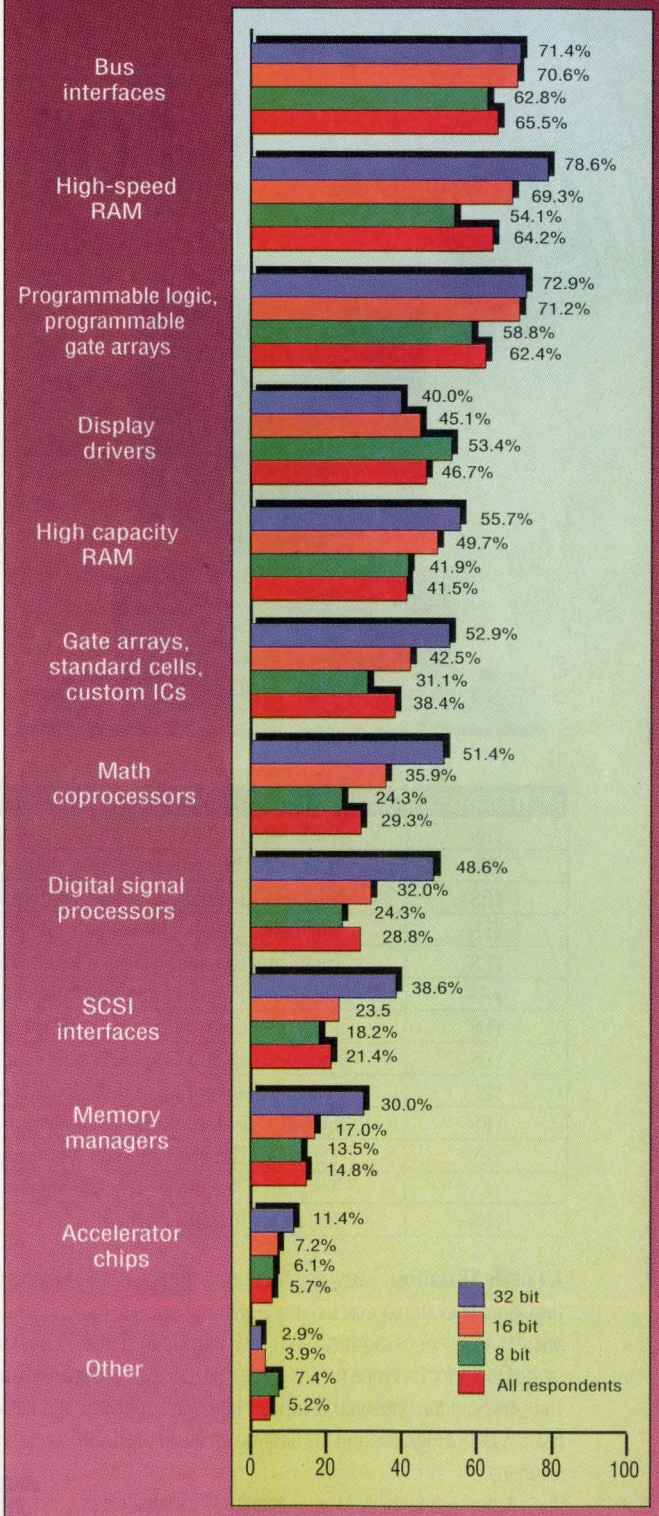

Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

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YES	Integrated Environment: Mouse, Editor, Debugger, Calculator	YES
YES	Supports 16 Megabytes of Memory (breaks DOS 640K barrier)	YES
YES	Engineering Math: Matrix Math, Complex Numbers	YES
YES	High Level Graphics: Screen, Plotter, Printer	YES
YES	Structured Programming with Independent Subprograms	YES
YES	Runs on Industry Standard Personal Computers	NO*
YES	Industry Standard Graphic Printer Support: Epson, IBM, lasers, etc.	NO
YES	Industry Standard Network Support: Novell, IBM, Microsoft, NFS, etc.	NO
YES	Industry Standard IEEE-488 Support: National Instruments, IOtech, etc.	NO
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CIRCLE 98

WHAT'S ALL THIS STATISTICAL STUFF, ANYHOW?

I've always been a fan of Mark Twain and his writing. He had a rather good perception of the American people, and many topics that he wrote about are fascinating to this day. One of my favorite quotes of Twain is: "There are three kinds of lies: there are "lies," there are *damned lies*, and there are STATISTICS...."

One thing that doesn't help me a darned bit is "statistics," at least in the sense that most mathematicians and engineers use them. I find most statistical analyses worse than useless. But I *do* like to use charts and graphs. I took some data of diodes' V_F versus I_F recently. The data was a little suspicious when I wrote down the numbers, but after I plotted the data, I *knew* there was something wrong. Then I just went back and took more data until I understood what the error was, ac current noise that was being pumped out of the inputs of the digital voltmeter, crashing into the diode, and causing rectification. If data arises from a well-behaved phenomenon and conforms to a nice Gaussian distribution, then I don't care if people use their statistical analyses—it may not do a *lot* of harm. (Personally I think it does harm, because when you use the computer and rely on it like a crutch, you get used to believing it and trusting it without thinking....) However, when the data gets screwy, classical statistical analysis is worse than useless.

BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

For example, one time a test engineer came to me with a big formal report. Of course, it didn't help that it arrived at 1:04 P.M. for a Production Release Meeting that was supposed to start at 1:00 P.M. But this was not just any hand-scrawled report. It was handsome, neat, and computerized; it looked professional and compelling. The test engineer quoted many statistical items to show that his test system and statistical software were great (even if the ICs weren't). Finally he turned to the last page and explained that, according to the statistics, the ICs' outputs were completely incompetent and way out of spec. Thus, the part could not be released.

In fact, he observed, the median output of the output was 9 V, which was pretty absurd for the logical output of an LM1525-type switching regulator, which could only go to the Low level of 0.2 V or the High level of 18.4 V. How could the outputs have a median level of 9 V?

How do you get an R-S flip-flop to hang up at an output level half-way between the rails? Unlikely.... Then he pointed out some other statistics—the 3 sigma values of the output were +30 V and –8 V. Now, that's pretty bizarre for a circuit that only has a +20-V supply and ground, (and it isn't running as a switching regulator, it's just sitting there at dc). The meeting broke up before I could find the facts and protest, so that product wasn't released on schedule.

It turns out, of course, that the tester was running falsely. So while the outputs were all supposed to be *set* to +18.4 V, they were actually in a random state. Half of the time the outputs might be at 18.4 V and half of the time at 0.2 V. If you feed this data into a statistical program, it might indeed tell you that a lot of the outputs would be at +9 V, and some of the outputs might be at –8 V, assuming that the data came from a Gaussian distribution. But if you *look* at the data and *think*, it's obvious that the data came from a ridiculous situation. Rather than ramming the data into a statistical format, the engineer should have checked his tester.

Unfortunately, this engineer had so much confidence in his statistical program that he spent a whole week preparing the Beautiful Report. Did he inform the design engineer that there were some problems? No. Did he check his data, check the tester? No. He just kept his computer cranking along, because he knew the computer analysis was the most important thing.

We finally fixed the tester and got the product out a little late, but obviously I wasn't a fan of that test engineer (nor his statistics) as long as he was at our company. And that's just one of a number of examples I trot out when anybody tries to use statistics that are inappropriate.

I do like to use scatter plots in two dimensions to help me look for trends, and to look for "sports" that run against the trend. I don't look at lots of data on good parts or good runs, but I study the *heck* out of bad parts and bad runs. And when I work with other test engineers who have computer programs that facilitate these plots, I support and encourage those guys to use those programs, and to *look at* their data, and to *think* about those data. I support anything that facilitates thinking.

A couple years ago, I was approached by an engineer who was trying to use one of our good voltage references with a typical characteristic of about 20 ppm per 1000 hours long-term stability at +125°C. He

was using it around room temperature, and was furious because he expected it to drift about 0.1 ppm per 1000 hours at room temp, and it was a *lot* worse than that. He asked why our reference was no good. I pointed out that amplifiers' drifts and references' drifts do *not* keep improving by a factor of 2 every time you cool them off another 11 degrees more.

I'm not sure who led him to believe that, but in general, modern electronic components aren't greatly improved by cooling or the absence of heating. In fact, those of us who remember the old vacuum-tube days remember that a good scope or voltmeter usually worked better if you kept it running nice and warm all the time, because all of the resistors and components stayed dry and never got moist under humid conditions. I won't say that the electrolytic capacitors might not have liked being a little cooler. But the mindless effort to improve the reliability by keeping components as cool as possible has been overdone. I'm sure you can blame much of that foolishness on MIL-HBDK-217 and all its versions. In some businesses, you have to conform to -217, no matter how silly it is, but in the industrial and instrument business, we don't really have to follow its every silly quirk and whim.

One guy who argues strenuously about -217 is Charles Leonard of Boeing, and you may well enjoy his writing (Leonard, Charles, "Is reliability prediction methodology for the birds?," *PowerConversion and Intelligent Motion,*" November 1988, p. 4). So if something is drifting a little and you think you can make a big improvement by adding a fan and knocking its temperature down from +75 to +55°C, I caution you that you'll probably be disappointed because there usually isn't a lot of improvement to be had. It's conceivable that if you have a bad thermal pattern causing lots of gradients and convection, you can cut down that kind of thermal problem. In general, though, there's not much to be gained unless parts are getting up near their maximum rated temperature or above +100°C. Even plastic parts can be pretty reliable at +100°C. I know the ones I'm familiar with are.

(This column is an excerpt from the soon-to-be-published book I have written entitled "Troubleshooting Analog Circuits." This endeavor will be published by Butterworths in April 1991.)

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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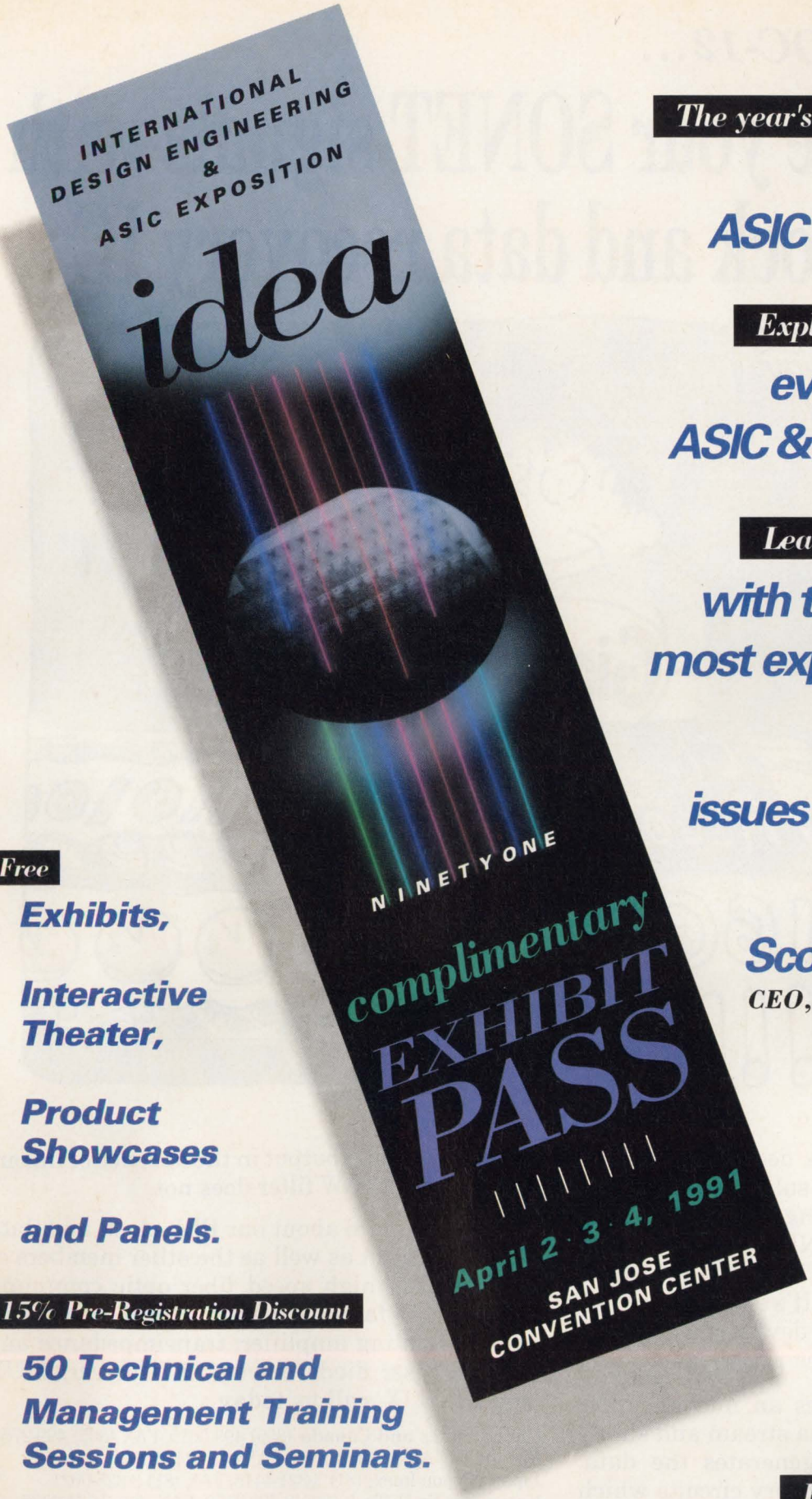

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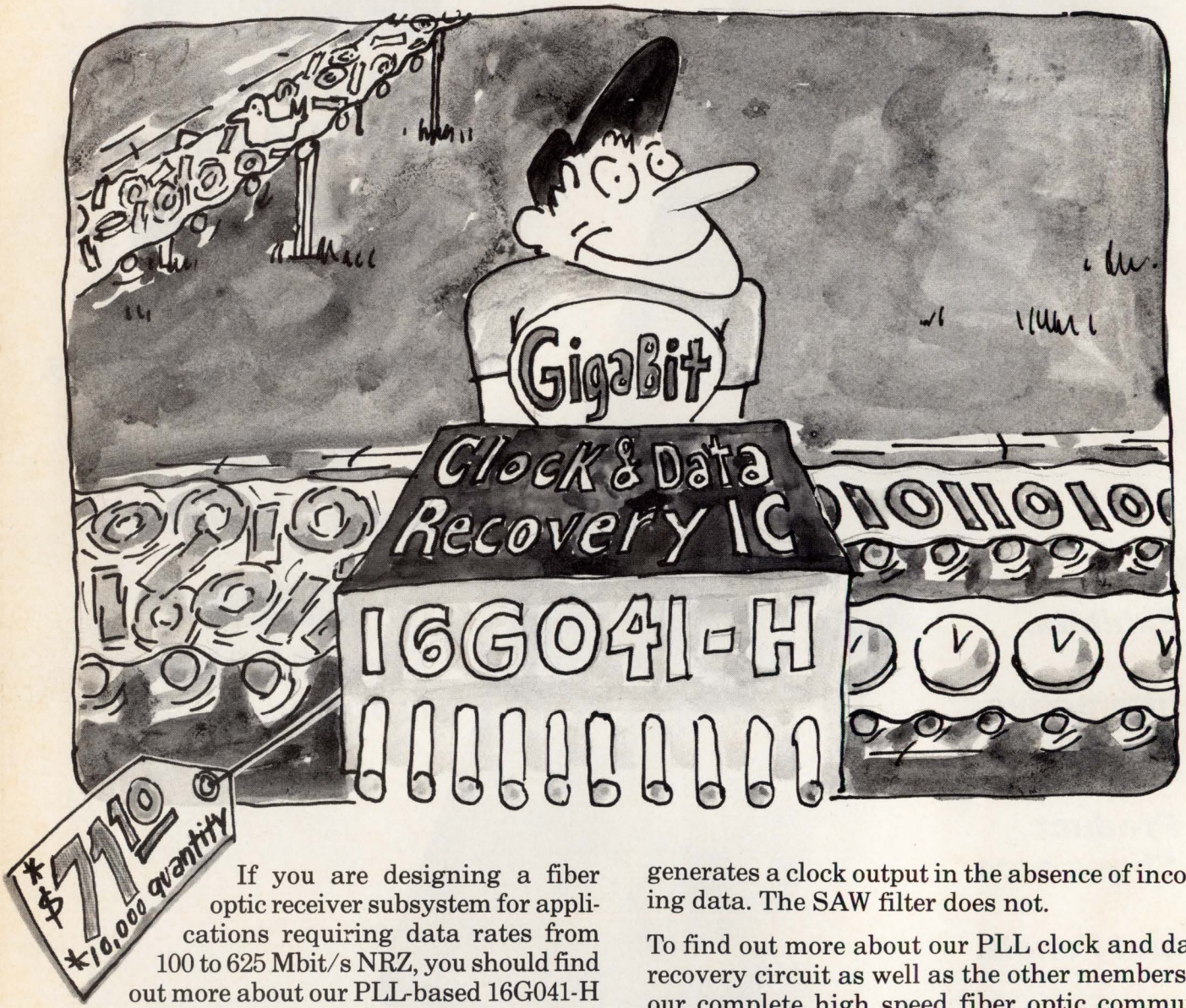

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CIRCLE 82

REPEATER INTERFACE IC TAKES ON ETHERNET MEDIA

ROBUST EXECUTIVE AND CONTROL FUNCTIONS SIMPLIFY NETWORK-MANAGEMENT TASKS FOR FUTURE ETHERNET LANS.

MILT LEONARD

With proven adaptability to changing user needs, the IEEE 802.3 Ethernet topology is positioned to become the local-area network (LAN) of choice for larger and more complex networks of the future. Adding to Ethernet's popularity is the various data-carrying media it can support, a trend that will stretch into the 1990s. Anticipating such a trend, National Semiconductor Corp. has developed a repeater interface designed for multimedia Ethernet LANs.

The DP83950 repeater interface controller (RIC) is designed to totally manage multimedia Ethernet LANs with diversified equipment and lengthy cable runs, and to detect and correct error transmissions. These LANs, which will require repeaters, hubs, bridges, and gateways, will link PCs, workstations, and specialized servers over a wide range of Ethernet configurations.

One configuration may be an older thick Ethernet cable interconnected with a thin Ethernet type to support a cluster of computers and peripherals. Another could be a low-cost, unshielded twisted-pair cable with a 10-Mbit/s data rate, running from the thick coaxial cable to a cluster of similar machines. Future networks that will be interconnected to the Fiber Distributed Data Interface (FDDI) can also exploit the DP83950's capabilities. The FDDI is a 100-Mbit/s fiber-optic data highway for next-generation computers working in a distributed processing environment.

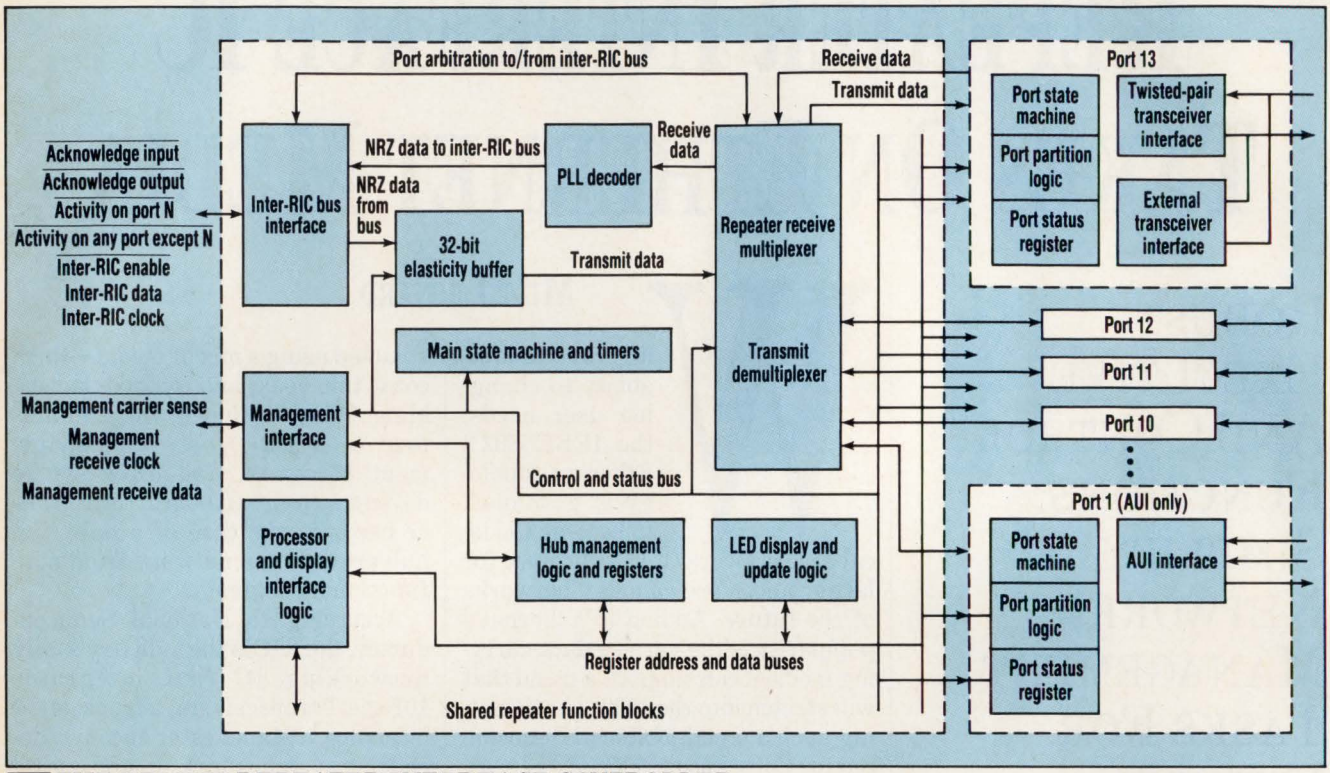
The RIC, a multiport repeater, regenerates incoming signals. A repeater permits a network to be constructed using a mix of media—thick coax, thin coax, and twisted-pair cabling. When equipped with an interface to a CPU, network-management hardware, and error-display devices on a circuit board, the repeater becomes the core of a hub. The hub protects the network from malfunctioning segments.

According to National Semiconductor, the RIC is the industry's only networking IC that integrates 10Base-T transceivers, a transceiver interface, a Manchester encoder/decoder, a system interface, and digital logic on one mixed-signal chip *(see the figure)*. The device has 13 ports that connect to network segments. Functions replicated in all ports include a port-status register, port-partitioning logic, and a port-state machine. Automatic signal-polarity detection and correction capabilities are also incorporated.

A port-state machine controls the transmission of repeated data and jam signals over the attached segment. It also decides whether or not a port will be the source of data or collision information to be repeated over the network. Twelve ports (2 through 13) also have a user-configurable transceiver interface that connects an on-chip 10Base-T transceiver to twisted-pair cabling, or bypasses the transceiver for an external transceiver. The Port-1 interface is dedicated to connecting to transceiver boxes and cables that are attached-unit-interface (AUI) compatible. These AUI interfaces consist of four-pair shielded wires.

The repeater core logic, which holds 30% of the chip's logic circuitry, contains a main state machine. This control-center oversees operations shared by all ports: a phase-

MULTIPORT REPEATER CONTROLLER



THE DP83950 REPEATER INTERFACE CONTROLLER contains all functions to support the IEEE 802.3 10Base-T standard for managed and non-managed Ethernet hubs. The chip includes interfaces for a system microprocessor, as well as the company's Sonic network interface controller for advanced network-management functions. This combination supplies the managed objects for the simple network-management protocol (SNMP), as well as the Open Systems Interconnection (OSI) network-management protocols.

locked loop for decoding, a 32-bit elasticity buffer for temporary storage of data-field bits, and receive and transmit multiplexers.

Many network applications are expected to be in "dumb" or standalone repeater modules. Here, the RIC serves only as a signal regenerator for point-to-point connections between nodes on the star topology of 10Base-T. For more complex connections, the device can be combined with a microprocessor and logic circuits to perform network-management and control functions. Data transfer between the RIC and processor occurs over an octal bidirectional bus. A number of RIC registers contain information that indicates the status of the hub-management functions, chip configuration, and port status. An arbiter schedules and controls processor accesses and ensures that correct information is written into display latches.

A repeater module can contain from three to eight RICs and support up to 256 external ports. When multiple RICs are cascaded in a hub, they communicate through an inter-RIC bus to share data packets and collision status while still operating as individual logical repeaters. One RIC failure won't affect the rest of the network. Repeater systems usually include visual displays that indicate network activity and the status of specific repeater operations. The RIC's display-update function block accommodates various indicators and merely requires external SSI devices to drive the indicators—usually LEDs. Over 60 LEDs associated with 12 ports can be used to indicate general repeater status and individual port status.

Future network controllers will not only supply basic management and control functions, but will also be used in hubs that collect, analyze, and display status and error conditions of the network segments to which they're attached. Ideally, the system would store the combined data-packet and status field of specific ports in system memory to be examined by hub-management software. The RIC does this with a dedicated hub-management interface, which is similar to the inter-RIC bus. That bus enables data packets to be recovered from the receiving RIC. The target recipient in this case is a network interface controller, such as National's DP83932 Sonic IC.

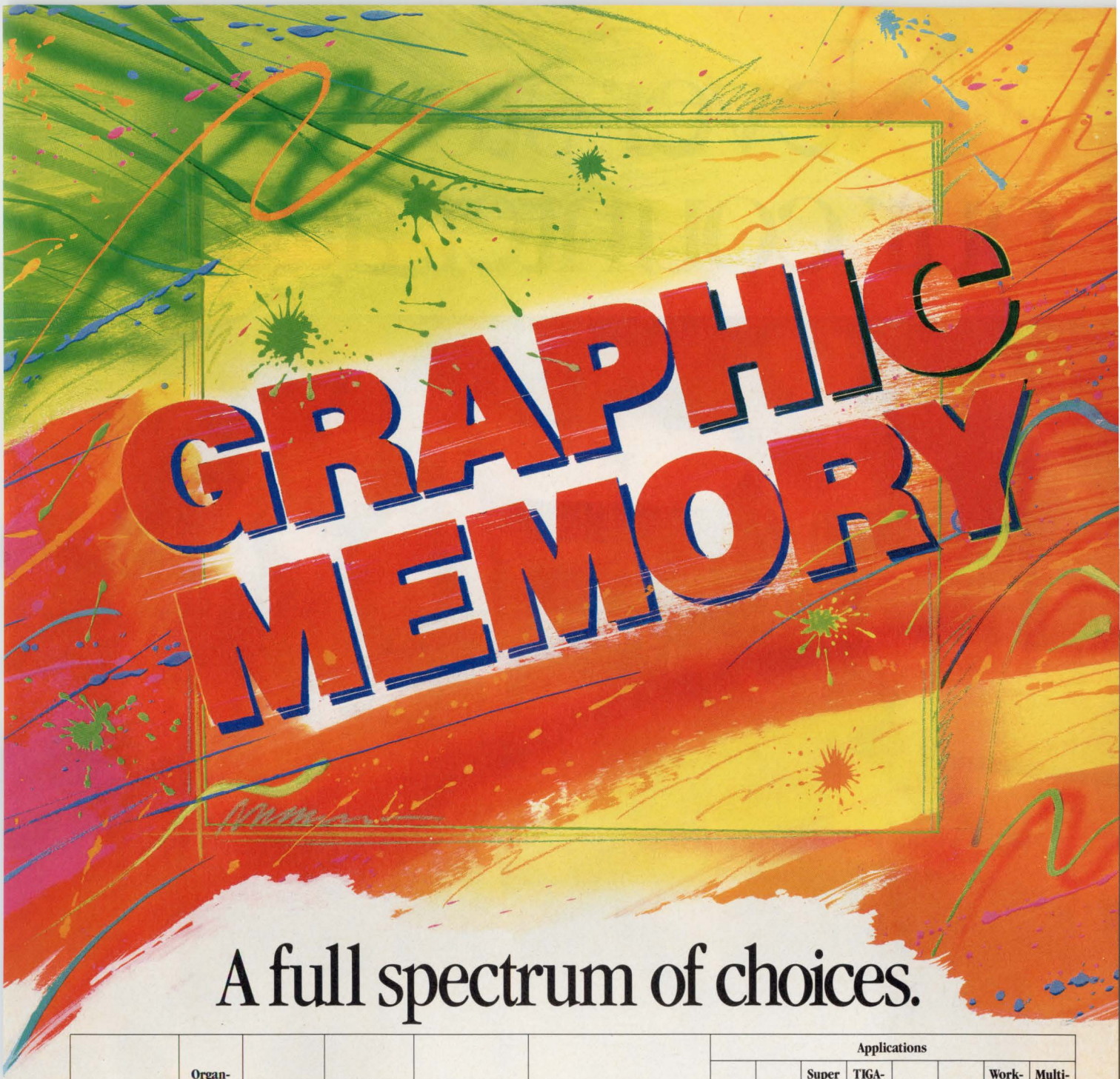
The DP83950 RIC is fabricated with a 1.5-μm CMOS process. The repeater IC dissipates 1.5 W.□

PRICE AND AVAILABILTY

Packaged in a 160-lead pin grid array, the DP83950 RIC is available now for $145 each in sample quantities of up to 100 units.

National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052-8090; Tushar Kothari, (408) 721-7020. **CIRCLE 513**

HOW VALUABLE?	CIRCLE
HIGHLY	535
MODERATELY	536
SLIGHTLY	537



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	x16*	80 – 100	ZIP, SOJ	MT4C1664/65/70	Now	●	●	●		●			
4 Meg DRAM	x16*	60 – 100	SOJ, TSOP	MT4C16256/7	Samp. Q4 '91; Prod. 1H '92		●	●		●			
256K VRAM	x4	100 – 120	DIP, ZIP	MT42C4064	Now	●	●	●	●		●	●	
1 Meg VRAM	x4	80 – 120	ZIP, SOJ	MT42C4255/6	4255 Now; 4256 Q4 '91		●	●	●	●	●	●	●
	x8	80 – 120	ZIP, SOJ	MT42C8127/8	8127 Now; 8128 Q4 '91		●	●	●	●	●	●	●
2 Meg VRAM	x8	70 – 100	SOJ	MT42C8256	Samp. Q4 '91; Prod. 1H '92			●	●	●	●	●	●
1 Meg Triple-Port DRAM	x4	80 – 120	SOJ	MT43C4257/8	Now							●	●
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CIRCLE 129

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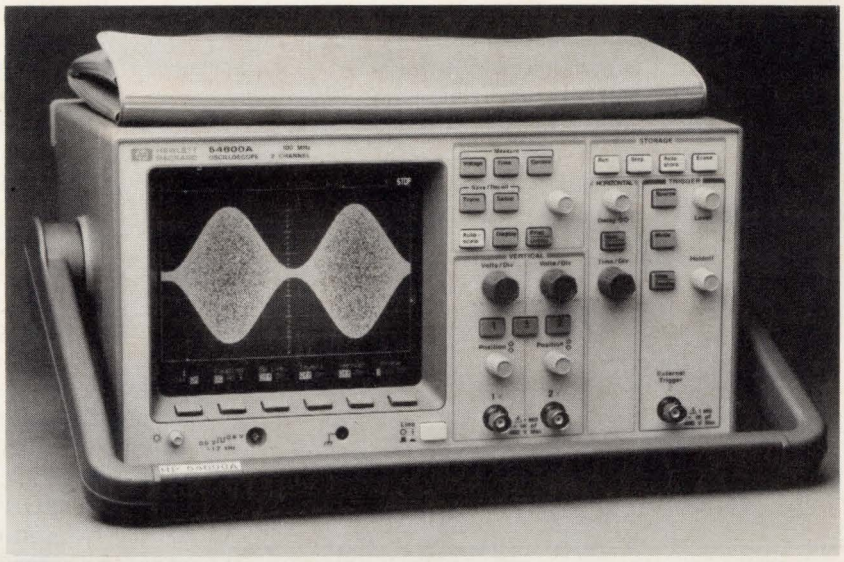

1. THE HP 54600A USER INTERFACE is designed to look and feel like that of an analog oscilloscope in order to appeal to engineers reluctant to make the move to a digital scope.

A Pair Of Digital Storage Oscilloscopes Try To Make Designers Forsake The Comfort Of Their Familiar Analog Instruments.

Scopes Offer Digital Power In A Cozy Setting

John Novellino

As popular as digital oscilloscopes have become, many engineers are still leery about making the switch from their trusted analog instruments. Some don't like the menu-driven interfaces usually found on digital scopes. Another complaint is that some digital scope displays lack a "live" feel—that is, they have a slow update rate. Price can also be an inhibiting factor.

Two portable digital scopes from Hewlett-Packard, the HP 54600A and HP 54601A, take direct aim at the analog holdouts. The goal is to convince analog-scope users that they can exploit the numerous features offered by digital instruments without losing the analog look and feel. The scopes fit into the heart of the general-purpose market, with 100-MHz bandwidths in 2-channel (54600A) and 4-channel (54601A) versions. Furthermore, prices are quite attractive. For a few hundred dollars more than comparable analog scopes, users can enjoy the automated features of digital storage instruments.

HP heavily emphasized user feedback in the design of the two scopes, espe-

cially the interface and display update rate. "In extensive focus group testing," says Dennis Weller, R&D section manager at HP's Colorado Springs Div. "we asked users why people don't buy digital scopes." Some users disliked the interface on earlier HP digital scopes, which included one knob whose function was controlled by keystrokes. So the 54600-series front panel looks very similar to that of an analog scope *(see the figure)*. Dedicated knobs adjust primary control functions: vertical sensitivity and position, time base, horizontal delay, trigger level, and hold-off. Buttons control storage, measurement, and utility functions.

A weakness of early HP digital scopes was the display update rate. Previous units could process and display 20,000 to 100,000 data points/s. But because the 54600-series breaks up the processing tasks among three processors, the new scopes improve that by an order of magnitude, reaching 1 million points/s.

The acquisition and display processing are done by custom devices, leaving the system CPU free to perform its own tasks. The acquisition processor, which is built in HP's proprietary CMOS process, contains 200,000 transistors. The IC creates waveform records from the digitizer data. The display processor, a gate array that uses a commercially available process, transforms the waveform records into the pixel display.

The scopes have a 20-Msample/s sampling rate with an 8-bit vertical resolution and peak-detection capability. The vertical sensitivity range is 2 mV to 5 V/div. Edge, line, and TV triggering are offered.

The advantages of digital technology are evident in the scopes' ability to perform 12 automatic measurements on frequency, time, and voltage. In addition, dual cursors help users make manual time and voltage measurements. An autoscale function sets up the scope with one keystroke. Two trace memories hold a total of 2 ksamples. The units are fully programmable through optional GPIB or RS-232 interfaces. These interfaces, as well as an optional parallel interface, can also be used to supply a plotter or printer.□

Price And Availabilty

The 2-channel HP 54600A costs $2395, and the 4-channel HP 54601A goes for $2895. The GPIB and RS-232 interface modules are $425 each, and the parallel interface costs $275. All are available 4 weeks from receipt of an order.

Hewlett-Packard Co., Colorado Springs Div., P.O. Box 2197, Colorado Springs, CO 80901-2197; (800) 752-0900. CIRCLE 512

How Valuable?	Circle
Highly	538
Moderately	539
Slightly	540

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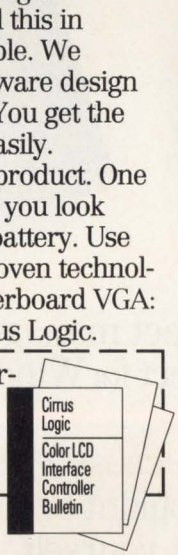

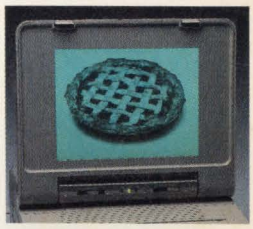

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SPREADSHEET-LIKE VHDL TOOL ALLEVIATES PROGRAMMING HASSLES

LISA MALINIAK

Engineers who want to design with VHDL but don't want to tangle with the programming process can find relief with the Hum design system from Lewis Systems Inc. The Hum design system is constructed from modules that are invoked from the initial menu. Users can switch back and forth between modules during the design process.

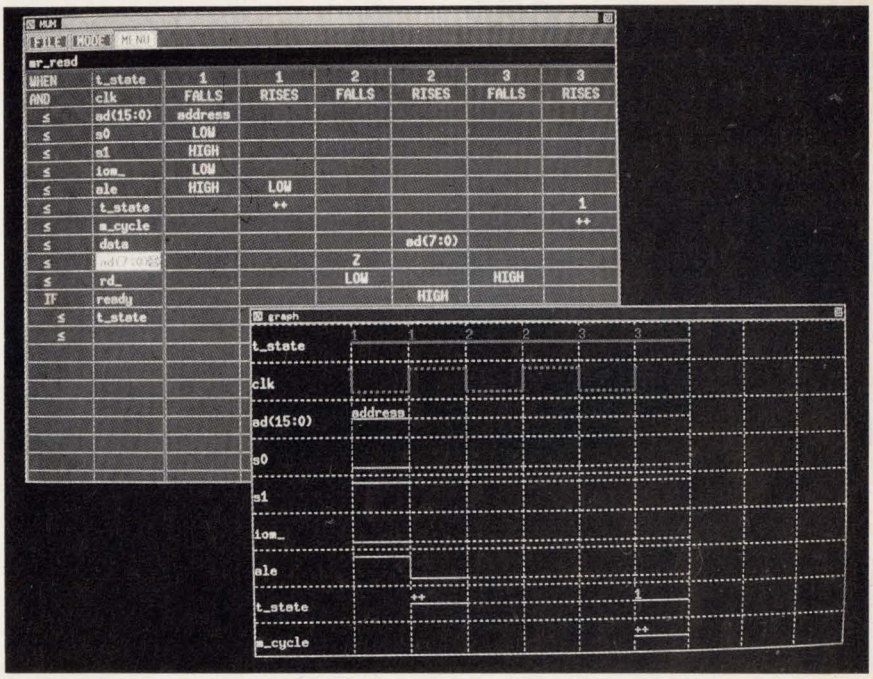
The Humtable is a spreadsheet-like table used to create VHDL models. The first and second columns in the Humtable are the control and object columns. Words in the control column (such as when, and, if) determine whether or not the identifiers in the object column (such as clk, S0) are control objects or assignment objects. Identifiers or operators in the remainder of the columns define conditions that produce a result assigned to the identifier in the object column. Events are "read" down each column. For example, when the clock falls, set S0 low.

Humtables are created almost the same way and in the same sequence in which they're conceived in the engineer's mind. Two different engineers often develop different Humtables for the same process, yet the resulting VHDL models are compatible. Also, Humtables are well-suited to segmenting the design into individual logical processes, such as memory read, reset, and instruction execution functions.

A nice feature of the system is that once an identifier is used, it's placed in a pop-up table and never has be typed in again. Users move the mouse to the desired box in the table and select proper identifiers.

Users may enter logic equations in the Humtable. These equations may be of any complexity and may overrun the width of the entry space. In addition, other Humtables can be called from the one in use. This is equivalent to invoking a procedure or function in VHDL.

A new design begins in the Humpins module—a table that designers use to identify the I/O pins of the design. Once entered in the table, they're placed in the pop-up menu and are available for use in Humtable development.



The Humsym and Humgraph modules furnish visual feedback of the design process occurring in the Humtable. Humgraphs are symbolic representations of the process, close to those shown in data books. Each time an event is entered into a Humtable, it's immediately reflected in a corresponding Humgraph *(see the photo)*.

Humtables are expanded into a native Hum language called Humbase. Humbase is less elegant than VHDL, and doesn't require much more programming ability than the Humtable. It's made available to users in case they want to add to or modify the design at this level.

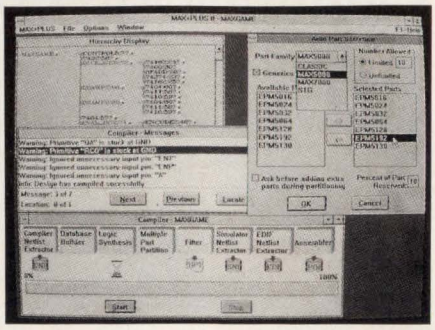
Engineers can generate large numbers of vectors for their design with the Humstim module (it will not be available with the first release of the product). Engineers use the Humtime module (also not available with the first release) to supply complex input-pin-to-output-pin timing values for the design. Timing can be implemented in the first-release Hum product by selecting the timing option while a Humtable is active. Timing values are then entered in the active space in the table, which in turn are entered directly into the VHDL code.

A Humcode module, to be available in the second quarter, will enable users to define the format modes for an instruction set. Users will be able to define instructions in a shorthand form that will expand into the Humtables automatically.

Additional Hum modules include a debug module, a color-selector module, a symbolic simulator, and a user-setup module. All Hum modules except the Humtime, Humcode, and Humstim modules are available now. The other three modules will ship in the second quarter of this year. The software, which costs $24,000, runs on Sun workstations. It will eventually run on HP/Apollo and Vax workstations.

Lewis Systems Inc., 1915 Peters Rd., Suite 113, Irving, TX 75061; (214) 438-3189. **CIRCLE 319**

PROGRAMMABLE-LOGIC TOOLS RUN UNDER WINDOWS 3.0



Altera's Max+Plus II software is the first logic design system operating under Microsoft Windows 3.0. Max+Plus II is a CAE system offering hierarchical schematic capture and HDL logic entry, logic synthesis, and timing simulation for the company's Classic and Max erasable programmable-logic devices (EPLDs). A 5000-gate design is typically compiled in 10 minutes or less.

By using the enhanced memory-management capabilities of Windows 3.0, Max+Plus II can automatically partition very large logic designs into a set of EPLDs. Designers can identify critical timing paths in the source design. Then the software automatically synthesizes the design and fits it into multiple EPLDs. The software also performs multichip simulation to verify the total design. And because Max+Plus II supports EDIF net lists, workstation-based designers can use their existing design-entry and verification tools with the tool's EPLD logic synthesis.

Max+Plus II, which will ship in April, costs $9995. The software supports all Altera general-purpose EPLDs, including the recently announced Max 7000 family that extends to 20,000 gates.

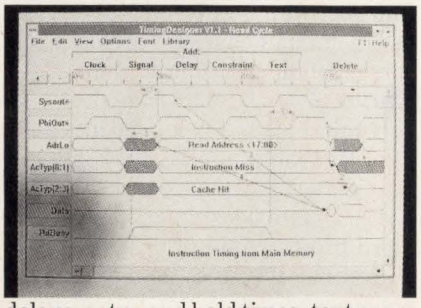
***Altera Corp.**, 2610 Orchard Pkwy., San Jose, CA 95134-2020; (408) 984-2800.* **CIRCLE 320**

■ *LISA MALINIAK*

PC SOFTWARE CHECKS TIMING FOR DIGITAL CIRCUITS

Electronic engineers can use the TimingDesigner software to specify, modify, and check timing requirements for digital circuits. TimingDesigner is a front-end design tool that automates the creation and analysis of timing diagrams.

Waveforms, clocks, gate and path



delays, setup and hold times, text annotations, and timing-parameter tables are entered with point and click mouse operations. To draw timing diagrams, designers use a mouse to place edges on the diagram model and to select between high and low signal states or valid or invalid bus states. Clock signals are generated automatically by entering period, duty cycle, duration, phase, and jitter into a dialog box.

Designers select delays from a separate library window. Each part has a minimum and maximum delay. The minimum and maximum values can be entered directly or computed from formulas based on user-defined variables such as temperature or voltage. Text can be placed anywhere on the diagram in several sizes and fonts.

As a timing diagram is modified, TimingDesigner automatically maintains the timing relationships specified between waveform edges. The software then performs timing analysis that gets updated dynamically as the diagram is modified. It displays the earliest and latest time that every edge can occur, computes the available margins for all timing limits, and highlights timing-limit violations in red and valid conditions in green.

TimingDesigner, which is shipping now, costs $1495. It runs under Windows 3.0, and requires an IBM PC or compatible with 1 Mbyte of memory, an EGA monitor, a hard disk, and a mouse.

***Chronology Corp.**, 2849 152nd Ave. NE, Redmond, WA 98052-5516; (206) 869-4227.* **CIRCLE 321**

■ *LISA MALINIAK*

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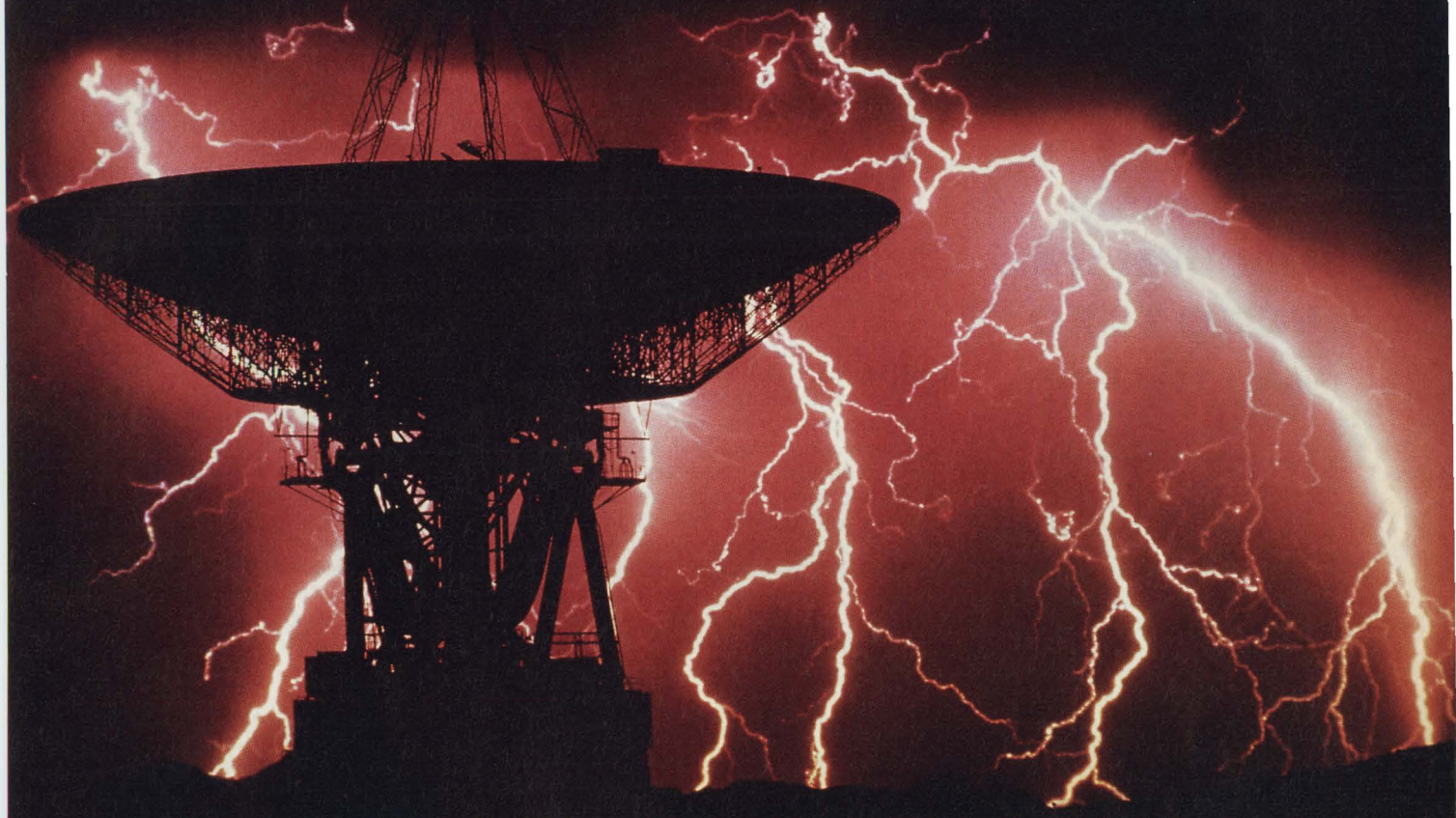

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(25°C @ 1MHz Samping Rate)
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CIRCLE 81

REVAMPED PC-BOARD DESIGN SYSTEM RUNS ON SUN WORKSTATIONS

Version 2.1 of the Crystal pc-board design system features an engineering change system, a 3D spacing checker, and a Gerber data viewer and editor. In addition, users can now run the tool set on Sun Microsystems' Sparcstation as well as Apollo workstations. The Crystal software is for the design and routing of high-speed, high-density pc boards.

The engineering-change system incorporates wiring and component changes automatically in a completely routed design without rerouting unmodified wires. Changes are added using the transmission-line, coupling, and length rules from the original design.

With the 3D spacing checker, users can verify routed Gerber data against spacing and clearance rules to ensure there aren't any violations. Spacing checks can be performed an all pc-board layers at one time.

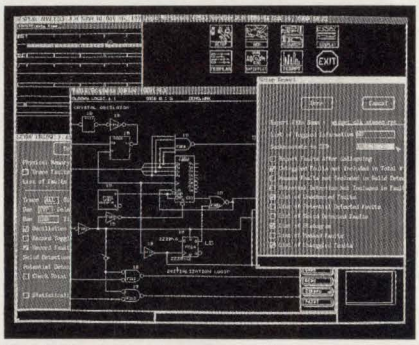
Users can view any combination of Gerber layers on a color display with the Gerber viewer and editor. The Gerber viewer can pan and zoom any area of the printed-circuit-board surface, and also measures feature sizes and clearance with a built-in ruler. With the editor, users can move and change the size of Gerber segments to solve clearance problems.

The Crystal Version 2.1 pc-board design system is available now on Apollo and Sun workstations. Pricing starts at $50,000, depending on configuration and platform. Delivery is four weeks after receipt of order.

***Shared Resources Inc.**, 3047 Orchard Pkwy., San Jose, CA 95134; (408) 434-0444.* **CIRCLE 322**

■ *LISA MALINIAK*

FAULT SIMULATOR NOW HAS TEST PLANNING



Test planning is among the many new features Valid Logic has added to the newest version of the RapidTest fault simulator. Specific test-planning features include: hierarchical fault selection for partitioning designs into blocks for test-vector creation; an automatic fault-collapsing algorithm to eliminate redundant faults; and a test-plan control function to define and automate the sequencing of multiple, hierarchical simulation runs. RapidTest 3.0 also offers schematic back-annotation, board-level simulation, and full integration with the company's Logic Workbench digital simulation environment. Operating under Logic Workbench, RapidTest 3.0 shares the same user interface, libraries, analysis tools, and database as Valid's RapidSim logic simulator. Pricing for RapidTest 3.0 with the Logic Workbench starts at $24,000. The starting price when sold separately is $17,000. RapidTest runs on DEC, IBM, and Sun workstations.

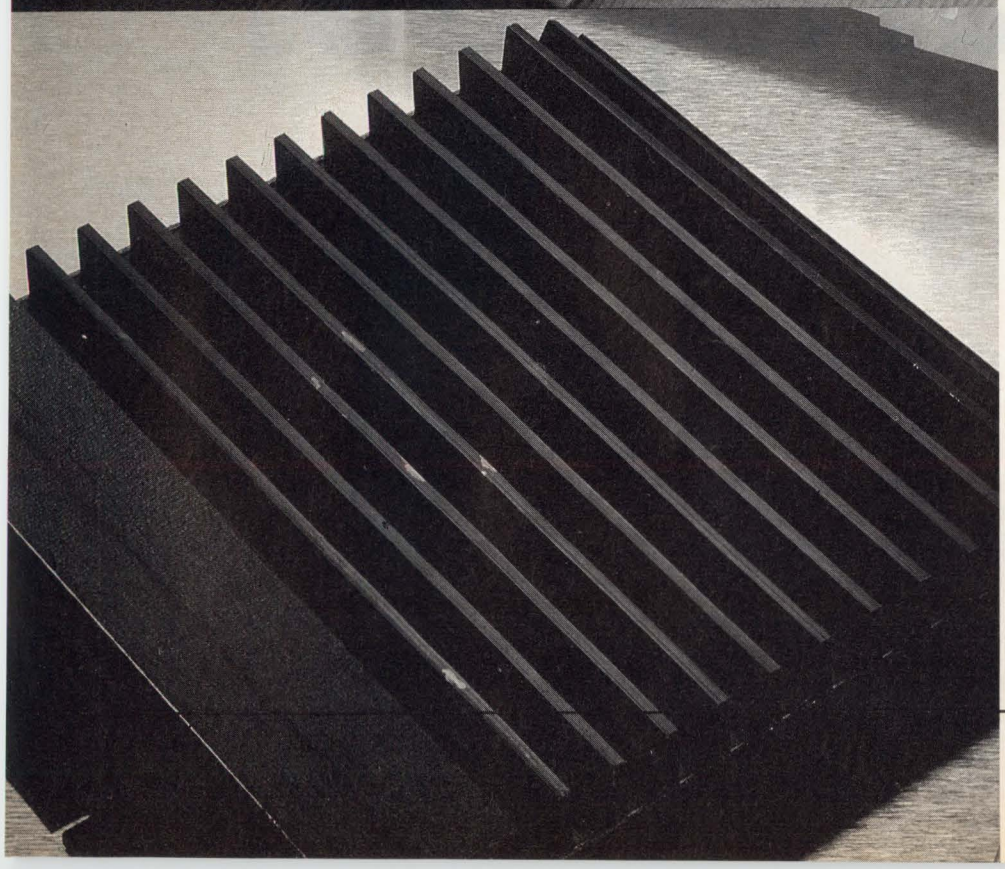
Valid Logic Systems Inc., 2820 Orchard Pkwy., San Jose, CA 95134; (408) 432-9400. **CIRCLE 323**

CAE TOOL CATERS TO SEQUENTIAL LOGIC

State/view is a graphical editor tailored for designing sequential circuits. It combines the advantages of graphical editing with the flexibility of high-level languages, closing the gap between hand-drawn diagrams and the sometimes complex syntax of logic compilers. Designers use State/view to draw diagrams interactively on the screen and then convert them to input files for various logic compilers. These design files can be used to synthesize PLDs, FPGAs, or gate arrays. Both Mealy and Moore machines can be defined at either circuit level or in flexible abstract terms. State/view creates concise documentation of the design and also ensures that flow diagrams and the compiler's input file are always congruent. The first release of the tool will produce design files for LOG/ic from Isdata and Data I/O's Abel. VHDL files will be supported in the future. State/view runs on all PCs with EGA or VGA graphics. It will be available in the first quarter for $945.

Isdata Inc., 800 Airport Rd., Monterey, CA 93940; (408) 373-7359. **CIRCLE 324**

MAGNESIUM. THE LIGHTWEIGHT SOLUTION FOR TOUGH DESIGN PROBLEMS.



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CIRCLE 114

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CIRCLE 80

LOGIC-DESIGN SOFTWARE USES EXTENDED MEMORY

The second version of the Bool logic-synthesis tool uses up to 16 Mbytes of extended memory in AT-class PCs. Bool is a general tool for synthesizing two-level logic from a behavioral description, and is aimed at ASIC and PLD designs. A compiler reads a behavioral description of a digital circuit written in a C-like language, then minimizes, simulates, and prints it out in various formats. Version 2 includes improvements in the syntax, minimizer, simulator, and output formatting. Among the new features are: support for multistage logic by including such variable types as flip-flops and nodes, an improved behavioral model, an event-driven simulator, and an enhanced built-in library. The Bool software runs on PCs and Sun workstations. Bool Version 2 is shipping now for $1100. A scaled-down version that can't use extended memory is available for $590.

Cornell Design Tools, 761 Cornell Dr., Santa Clara, CA 95051; (408) 984-0777. CIRCLE 325

LOGIC COMPILER MIXES FOUR ALGORITHMS

A Macintosh-based logic compiler for programmable devices uses four different reduction algorithms, depending on the circuit's complexity and desired compilation speed. The MacCUPL compiler uses the Quine-McCluskey reduction algorithm to guarantee minimum logic gates; Expresso, Presto, and Quick algorithms are used for faster compilation times. It runs under the Mac operating system and complies with all Apple user-interface guidelines. Device simulations are displayed in either waveform or tabular form. With assertion-level tracking, users can define arbitrary logic levels according to the levels they want to come out of the target devices. After inputting a design, users declare pins active high or active low, and MacCUPL automatically changes signal definitions throughout the design. The compiler supports PLDs, PALs, PROMs, EPROMs, EEPROMs, FPLAs, and other programmable devices. MacCUPL is shipping now for $1895.

Logical Devices Inc., 1201 N.W. 65th Pl., Ft. Lauderdale, FL 33309; (305) 974-0967. CIRCLE 326

ANALOG LIBRARY GROWS BY MORE THAN 40%

By adding 1025 new analog components models and symbols, the size of Mentor Graphics' AccuParts library has increased by more than 40%. The library now has 3454 models. Parts categories range from transistors and diodes to complex analog ICs. Also included in the new library are over 500 macromodels for such complex components as operational amplifiers. In addition, many model templates now incorporate more dc, ac, and transient effects. AccuParts models and symbols are qualified by Mentor and are integrated with the company's schematic-capture tools and AccuSim analog simulator. AccuSim can interactively simulate thousands of analog circuit elements. The updated AccuParts library, which is available now, is useful for simulating analog systems in the aerospace, communications, automotive, and other industries. Pricing ranges from $6000 to $22,000 for a one-year subscription.

Mentor Graphics Corp., 8500 S.W. Creekside Pl., Beaverton, OR 97005-7191; (503) 626-7000. CIRCLE 327

ANALOG EDITOR LINKS SCHEMATICS AND LAYOUT

The Analog Artist Layout Editor is an interactive editor from Cadence Design Systems for the physical layout of analog and mixed-signal ICs. Because the tool tightly links schematic design and physical layout, users needn't learn two separate sets of commands for schematic and layout representation. The editor has both layout-editing and layout-checking functions. It has polygon editing capabilities that allow users to cut polygon shapes, merge two or more polygons into one, and convert paths to polygons. In addition, users can interactively select one device in the schematic and place a corresponding layout device in the layout. The editor is available as an option to the company's Analog Artist Design System. It can also be purchased as an upgrade to existing Cadence layout editor installations. Analog Artist Layout Editor runs on most Unix platforms, and is shipping now for $25,000 per seat.

Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234. CIRCLE 328

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CADSTAR's revolutionary new user interface almost reads your mind, anticipating your next move and intelligently defaulting to the most likely action. For example, if you pick a part, CADSTAR lets you move it without selecting an action from a menu. If you pick a connection, you can manually route it instantly.

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RACAL

CIRCLE 120

CHIP SET MIXES VIDEO AND GRAPHICS ON MONITORS

Two chips from Philips Components-Signetics enable video and computer-painted images to be combined on computer monitor screens. The SAA7191 digital decoder converts digitized NTSC, PAL, or SECAM signals into the square-pixel luminance and chrominance (Y,U,V) signals required for desktop video. The conversion to square pixels allows image manipulation without distortion, and produces hard-copy prints that precisely match the on-screen video and graphics.

The SAA7191 accepts either composite or S-VHS inputs. Its output chroma and luminance values are compatible with CCIR 601 specifications, also known as D1 in the U.S. The SAA7192 color-space converter accepts YUV signals from the SAA7191, interpolates samples, and digitally converts the YUV signals to the 24-bit RGB data format required for driving desktop color displays. The chip also performs inverse gamma correction using an on-chip lookup table. The RGB output can be manipulated as computer graphics, or converted into analog red, green, and blue.

Both devices operate on 5 V and are packaged in 68-pin plastic leaded chip carriers. Prices for quantities of 100 to 1000 pieces are $34.30 for the SAA7191 and $22.81 for the SAA71192. Production volumes are scheduled for the first quarter of 1991.

***Philips Components-Signetics,** 811 E. Arques Ave., Sunnyvale, CA 94088-3409; Steve Solari, (408) 991-4577* CIRCLE 329

■ *MILT LEONARD*

32-BIT DSP CORE FEATURES SMALL SIZE

The ST18932 32-bit DSP core has the industry's smallest core die size. Designed for cellular telephones, it's based on SGS's ST18 DSP architecture. Built in 1.2-μm CMOS, it's compatible with SGS's CMOS standard cells. A combination of the DSP core, the digital cell library and the module generators for RAM, ROM and PLAs allows complete DSP systems to be implemented in customer-specific form. The chip's 32-bit ALU operates on real or complex numbers. Its parallel architecture allows it to read two independent operands, perform a multiplication and an ALU operation, write a result back to memory, modify three address pointers, and perform an I/O operation, all within one machine cycle of 77 ns. The ST18932 is supported by a complete set of hardware and software tools for system development. Available now, a customer-specific chip, including the 32-bit DSP core, will cost around $20 in large quantities.

SGS-Thomson Microelectronics Inc., I-20014 Agrate Brianza, Italy; (0039) 39-6555-597. CIRCLE 330

GROUP LISTENING-IN IC COMBINES NEW FEATURES

A "group listening-in" IC for analog telephone sets now incorporates supply circuits. Unlike other ICs, the TEA1805 maintains its high audio quality even at low line currents.

The bipolar IC works in line-powered telephone sets that have a loudspeaker in the base as well as the handset, enabling a group of people to listen to a telephone conversation at the same time. It offers excellent acoustical performance by suppressing feedback, or howling, and by ensuring that the received speech signal isn't influenced by outgoing speech.

The 1085 also provides call-progress monitoring of pulse or dual-tone mutliple-frequency (DTMF) tones. It incorporates a loudspeaker amplifier with fixed 35-dB gain, a dynamic limiter, and mute circuitry. It can develop more than 40 mW into a 50-Ω speaker in a bridge-tied-load configuration.

The IC draws up to 120 mA of current and provides a stabilized 3.6-V supply for peripheral ICs. Its minimum input current is 4 mA. The TEA1805 device is available in a 24-lead plastic SOT-101B DIL package or surface-mount SO-24 minipack. Samples are now available. Price is about $4 each in 100-unit lots.

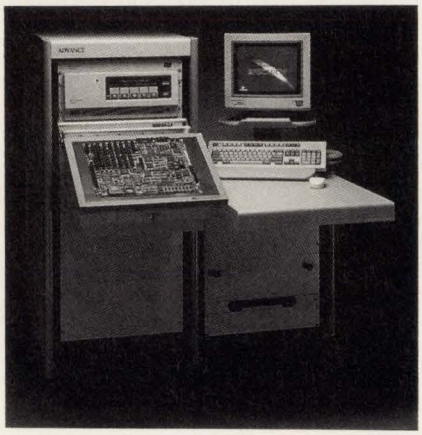
Philips Components, P.O. Box 218, NL-5600 MD Eindhoven, the Nether lands; (0031) 40-724173. CIRCLE 331

TESTER, DEVELOPMENT SOFTWARE HANDLE TOUGHEST PC BOARDS

The Advance, a functional ATE workstation, combines with the Spectrum functional test and diagnostics software system to tackle test and diagnostic problems on high-performance pc boards.

The Advance aims specifically at boards with one or more microprocessors, mixed-signal technology, custom devices, and fine-pitch surface-mounted components. The system employs a workstation form-factor ideally suited to the distributed test needs of a parallel or cell-level manufacturing process. This architecture makes it possible for quick and economical distribution, and addition, of tester resources to handle rapidly changing market and product needs.

The Spectrum software offers a development environment that speeds test programming, from simple pass-fail functional tests to complete fault-isolation packages. A built-in test executive, called the Spectrum TestExec, provides a sophisticated framework for organizing test programs and eliminates large segments of application programming. Furthermore, with Spectrum, the functional test and diagnostics program are the same. Spectrum's primary diagnostic tool, its fault dictionary, goes beyond the conventional driver/sensor-based dictionary to include a wide range of data, including microprocessor emulation, high-speed measurement, and analog results.



Prices for the Advance depend on configuration and start at approximately $100,000. First shipments are scheduled for March. The Spectrum software costs $9500 for a complete development version and $1500 for a runtime version. Shipments are scheduled for April.

***Summation Inc.**, 11335 NE 122nd Way, Kirkland, WA 98034; (206) 823-8688.* **CIRCLE 332**

■ *JOHN NOVELLINO*

ACQUISITION SYSTEM DISPLAYS IN REAL TIME

Version 5.3 of the AT/MCA CODAS (computer-based oscillograph and data-acquisition system) software-hardware package has been enhanced with a third real-time display mode, a variety of frequency-domain analysis tools, and a built-in statistics program. In addition, version 3.1 of the Advanced CODAS waveform analysis program has been upgraded with an arithmetic operations module and other analysis features. The AT/MCA package is a real-time waveform-acquisition, display, and analysis system for IBM PC/AT or MicroChannel computers. The Advanced CODAS software speeds analysis and reduction of waveform data acquired with the AT/MCA CODAS system. AT/MCA CODAS 5.3 costs $2790, and Advanced CODAS 3.1 goes for $595. Upgrades to current owners are free. Delivery of both is within 2 weeks.

***Dataq Instruments Inc.**, 825 Sweitzer Ave., Akron, OH 44311; (216) 434-4284.* **CIRCLE 345**

ASSEMBLY CONVERTS 28-PIN DIP PLUG TO PLCC

Emulators designed for 28-pin DIP devices can be converted to work with PROMs in 28-pin PLCC packages using the SOCON 28DIP6/PLCC converter. The assembly consists of a pc board with a female production-style DIP socket on top. The board is mounted on a PLCC plug with 50-mil-space, gold-plated round contact pins. The pins are wired one-to-one. The 28DIP6/PLCC costs $165 each; quantity discounts are available. Delivery is stock to 5 days after receipt of an order.

EDI Corp., P.O. Box 366, Patterson, CA 95363; (209) 892-3270. **CIRCLE 333**

DEBUG TOOLS FOR 4-BIT CPUS RUN WITH WINDOWS

One major complaint from designers working with 4-bit microcontrollers are primitive and unwieldy development tools. The Simplehost software debugging tool for NEC Electronic's 17000 family of 4-bit controllers will change that thanks to its ability to run under the Microsoft Windows shell. The Simplehost software deals only with source code, automatically assembling the code for the designer. This eliminates a tedious step in the design process.

A novel patch feature of the Simplehost software debugging tool allows the debugger to transfer only changed lines of code to a target system when the designer makes a change in the program. As a result, the time required to test program fixes is reduced drastically because the entire program needn't be recompiled.

Also part of the Simplehost software package is a programmable pulse generator that acts as a pattern generator, permitting the designer to create signal patterns graphically. With the ability to call multiple windows onto the PC-hosted screen, a designer can execute a software program while viewing the trace file. The designer can then highlight a particular instruction in the code file and see the same instruction highlighted automatically in the trace file.

Another feature is Simplehost's ability to let the engineer set up break conditions up to four levels deep. A RAM coverage feature enables the programmer to identify whether he has written to or read from any RAM location at any given time.

A ROM coverage function of the Simplehost software debugging tool helps identify how many times each instruction is executed.

The Simplehost software runs on any PC platform using Windows 3.0 and is employed with the IE-17K hardware emulator. Prices for the emulator and software combination start at $4000. Users already owning an IE-17K emulator can get the Simplehost software at no charge.

***NEC Electronics Inc.**, 401 Ellis St., Mountain View, CA 94039; Mahmoud Etemadi, (415) 960-6000.* **CIRCLE 335**

■ *DAVE BURSKY*

CAE Technology Report

March 1991
Vol. 3, No. 3

Silicon Breadboards Arrive

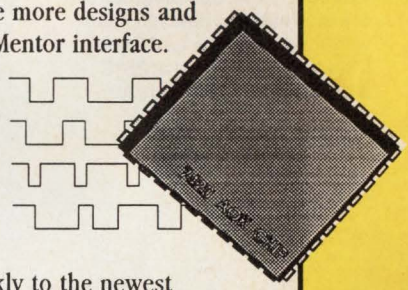
Silicon vendors got together with a leading CAE house and scored in a big way. They created silicon breadboarding that allows interactive simulation of multiple field programmable gate arrays (FPGAs), as if they were one piece of silicon. The user can display, next to each other, cells from different FPGAs and observe in real-time how a change in one cell affects operations of cells in other FPGA packages. This new technological advancement allows the user to break any design into multiple FPGAs and test them as one entity. This way, designers don't have to wait for the newest and biggest FPGAs; instead, they can design with the most economical and well established FPGA parts. Contact Actel at (800-227-1817) and XILINX at (408-879-5199) about FPGAs. For Silicon Breadboarding (SUSIE 6.0), contact ALDEC (805-499-6867). **CIRCLE 102**

OrCAD™ Users Benefit Again

Users of the popular OrCAD schematic capture program got a major support from SUSIE 6.0 which simulates their designs with 10 picosecond accuracy. OrCAD users can now directly interact with their designs as if they were real hardware breadboards. For example, they can toggle switches, move jumpers, replace ICs, change JEDEC fuse maps and hex files, modify layout delays, etc., all in real-time. The designers can also modify their designs and test vectors while they simulate. Since there are no compilations and the simulator behaves like a real hardware breadboard, it is easy to learn and use. The SUSIE simulator is finding broad applications, primarily among PLD and FPGA designers who urgently need such an interactive tool. SUSIE 6.0 sells from stock. **CIRCLE 103.**

Mentor™ Designs - Run In Real-Time!

Mentor users can now verify their designs in real-time thanks to a new EDIF interface to SUSIE which is the industry's most popular logic simulator. SUSIE runs on 386/486 PC platforms and simulates designs in excess of 200,000 gates, with 10 picosecond accuracy. SUSIE comes equipped with a software accelerator, milestones, and an automatic design errors locator. The user can modify design and test vectors while he or she simulates, and working with SUSIE is much like working with real hardware. SUSIE frees Mentor workstations to handle more designs and costs only $9,995, including Mentor interface. **CIRCLE 104.**



Free Upgrade to VHDL Libraries

To help customers move quickly to the newest industry standard, SUSIE 6.0, ALDEC is upgrading all SUSIE installations at a straight price differential. The libraries are upgraded to the new VHDL standard at no cost. The new SUSIE has many improvements like a DOS extender, milestones, graphical test vector editor, software accelerator, powerful breakpoint editor and many other features that make it the most popular engineering tool.

SUSIE is resold or recommended by over 15 OEMs worldwide, including CADAM™, Racal-Redac™, Accel™, Omation™ CAD Software™, etc. It looks like everybody's betting on SUSIE these days. **CIRCLE 105.**

How To Shop For A Good Simulator

There are many benchmarks and comparison sheets that pit one simulator against another. However, newest benchmarks stress speed, real-time operation and test automation. Clearly, the most important trend is interactive, real-time simulation that allows the user to interact with the design and test vectors while simulating. This allows for the kind of interaction that designers used to have with a real hardware breadboard. The latest enhancements in speed is selective simulation which allows instant manual selection of design sections for simulation. This may speed simulation over 100 times. The latest in automation is "milestones" which allows instant resimulation of past cycles with new design and test vector changes. Simulators have considerably progressed during the last year, and if you're looking for a good buy, make sure that your simulator operates in **real-time** and comes equiped with **selective simulation** and **milestone functions**. Don't waste today's budget on yesterday's batch-style technology.

* **SUSIE** is a trademark of ALDEC Co., Inc. Newbury Park, California, USA . **TEL: (805) 499-6867 FAX: (805) 498-7945**

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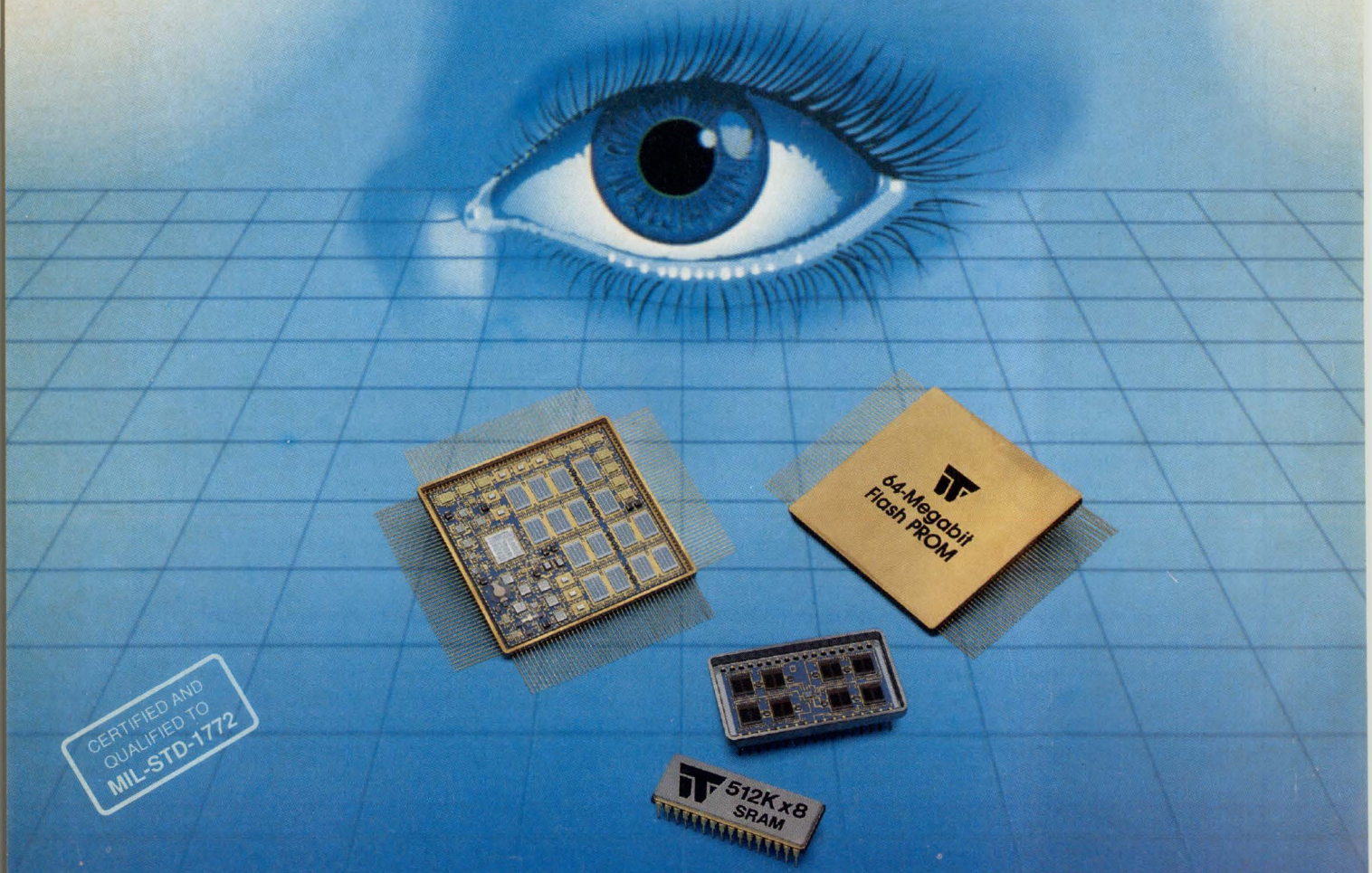

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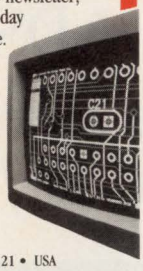

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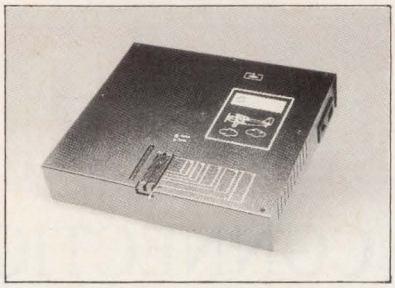

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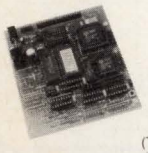

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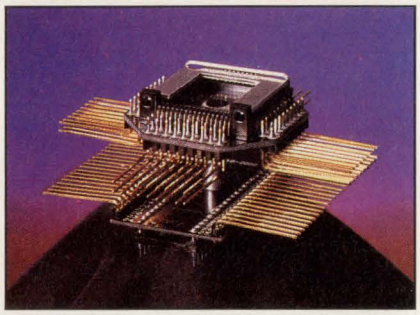

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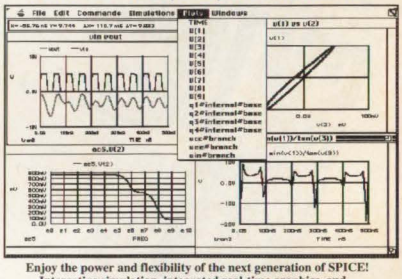

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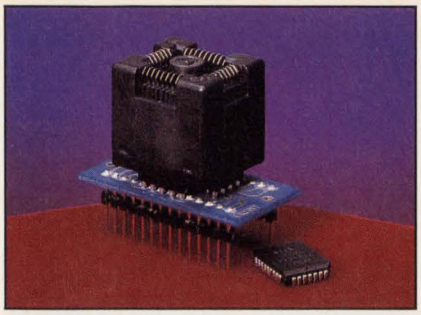

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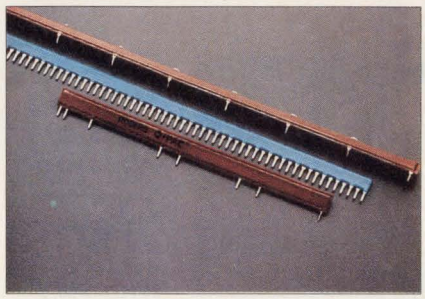

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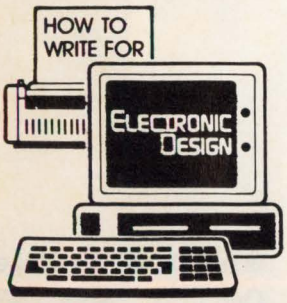

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Jan. 10	Dec. 14	April 11	March 15	July 11	June 14	Oct. 10	Sept. 13
Jan. 31	Jan. 4	April 25	March 29	July 25	June 28	Oct. 24	Sept. 27
Feb. 14	Jan. 18	May 9	April 12	August 8	July 12	Nov. 7	Oct. 11
Feb. 28	Feb. 1	May 23	April 26	August 22	July 26	Nov. 21	Oct. 25
March 14	Feb. 15	June 13	May 17	Sept. 12	Aug. 16	Dec. 5	Nov. 8
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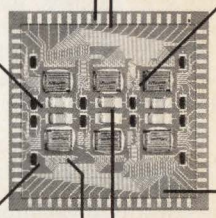

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CIRCLE 86

NEW!...THE MOST POWERFUL...MOST ACCURATE CLUB IN GOLF!

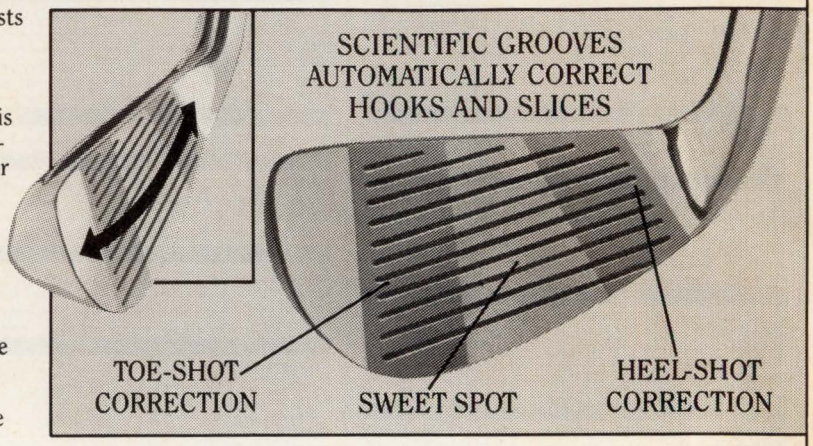
The CONTROLLER® HITS 30-50 YARDS LONGER, AUTOMATICALLY CORRECTS HOOKS AND SLICES ...MUST CUT STROKES — OR MONEY BACK!

Put your #3, #4 and #5 woods in the cellar. Tests show our new Controller driving iron can outhit all three by 30 to 50 yards.

And that's only half the story. The Controller automatically corrects hooks and slices! The club is so powerful, so accurate, we unconditionally guarantee it will cut 5 to 10 strokes off your score — or you owe us nothing! In fact, to prove it we'll send you one risk-free.

Test it against your #3 wood. If it doesn't give you 30 more yards (if you are a fairly good golfer), send the club back for a refund.

But it will give you 30 more yards! In fact, the Controller is so powerful many golfers use it off the tee, especially on narrow fairways.



Here is the Controller's exact distance advantage as compiled by some low-80's golfers.

CONTROLLER®	220 yards
#3 Wood	190 yards
#4 Wood	180 yards
#5 Wood	170 yards

Now test the Controller's accuracy against your 3-iron. Purposely hit a shot off the *toe* of each club and watch what happens. Your 3-iron will *hook* the ball violently—the Controller will keep it down the middle! The same is true with *heel* shots. Your 3-iron will *slice* the ball violently—the Controller will automatically keep it on course!

THE GREATEST STROKE-CUTTER IN GOLF

These scientific breakthroughs make the Controller driving iron the most powerful strokecutter in golf. We believe the club will transform the game. First of all, it obsoletes fairway woods! The Controller not only hits 30 to 50 yards farther than fairway woods, it automatically corrects hooks and slices! Here's how it works.

AUTOMATIC ACCURACY

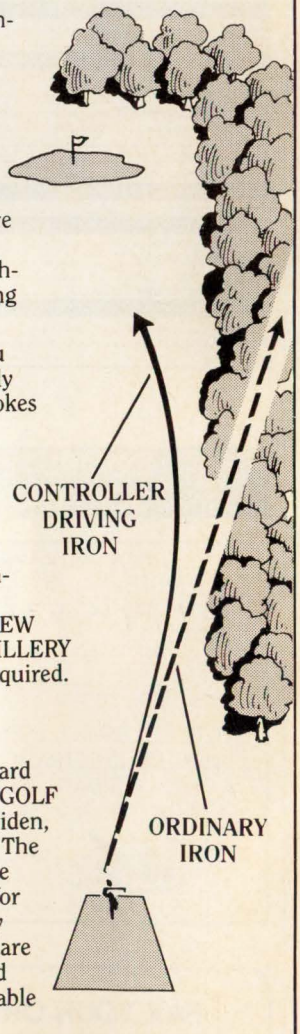
The Controller has an *invisible curve* across its hitting surface—a curve that's going to revolutionize your game. *No other iron has it!* Hit a shot off the Controller's sweet spot and it will go straight, as it would with an ordinary iron. But even pros hit off the heel and toe.

Now, here is the Controller's genius...here is why you could cut as many as 10 strokes off your score. Hit the ball off the Controller's heel or toe and its invisible curve will automatically impart a corrective spin to what would otherwise be a disastrous hook or slice. The ball will actually fade or draw back on course! It's an incredible sight and you can prove it to yourself with only a few test shots. **THIS IS THE MOST IMPORTANT GOLFING BREAKTHROUGH IN GENERATIONS.** ALONG WITH THE CONTROLLER'S EXTRA 30-50 YARDS, YOU SHOULD EASILY CUT 5-10 STROKES OFF YOUR GAME!

Here are more reasons why the Controller driving iron is going to give you the best golf of your life...

- it gives you the power of a driver with the control of an iron...
- its sleek, smooth head swoops through grass more cleanly than a wood...
- its 17° loft gets your shot up faster than a #3 wood...
- its smaller head size (versus a wood) boosts clubhead speed...
- its boron-graphite shaft model adds even more clubhead speed...
- it lets you carry more wedges and putters without exceeding the 14-club limit (by eliminating your #3, #4 and #5 wood)...

The Controller is new and supply is limited. You must act now and remember, you are completely protected. If the Controller doesn't cut 5-10 strokes off your score, you may return it (undamaged, of course) for a prompt refund of its price.



FREE!

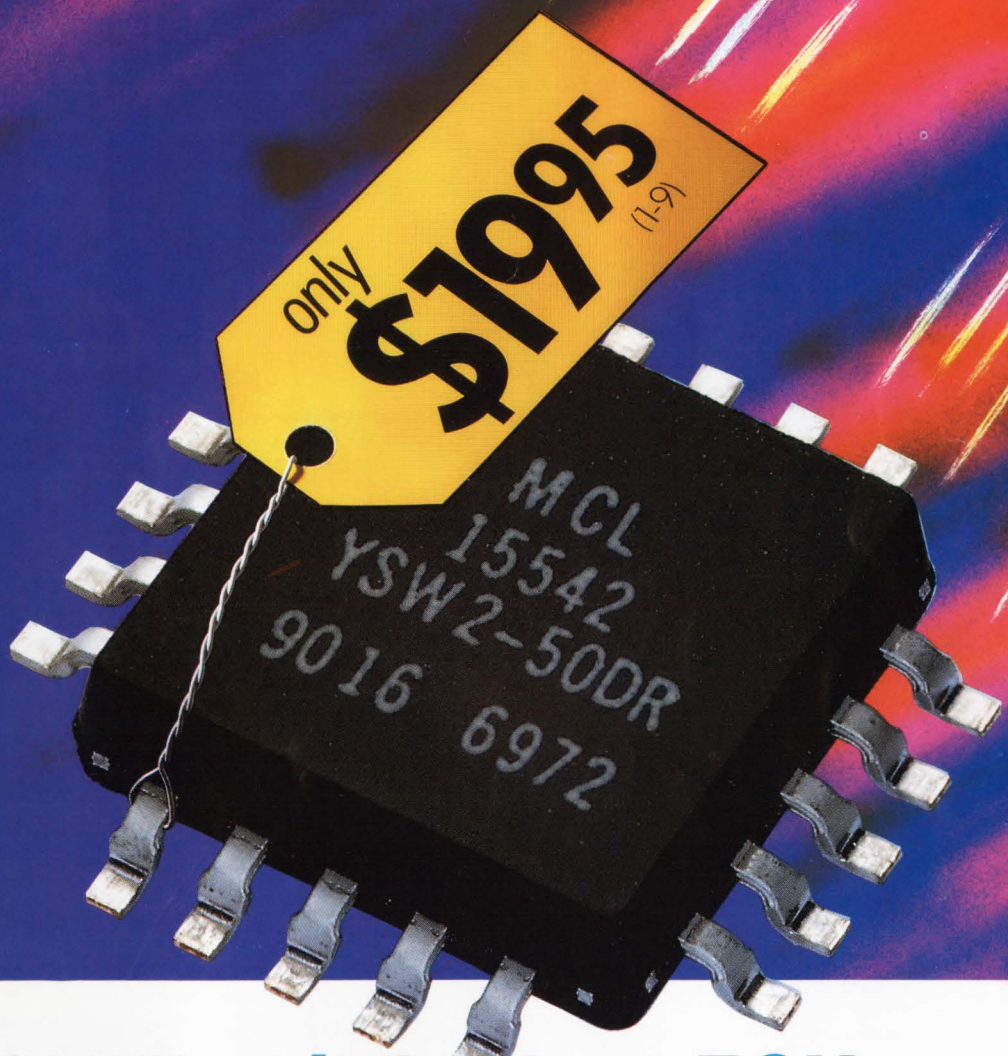
...just for trying the Controller! Keep your new power pin-high with a $15.00 Rangefinder! It's yours to keep FREE! even if you return the Controller for a refund. NOW YOU CAN RANGE YOUR NEW DISTANCE LIKE AN ARTILLERY OFFICER. No batteries required. Clips to belt.

HOW TO ORDER

Send your name, address and check (or credit card number and expiration date) to the NATIONAL GOLF CENTER (Dept. DR-50), 500 So. Broad St., Meriden, CT 06450. Or call 203-238-2712 (8-8 PM, M-F). The steel-shaft CONTROLLER costs only $59.00; the boron-graphite model costs $89.00. Add $4.00 for shipping. CT and NY must add sales tax. Specify regular or stiff flex, no P.O. boxes, all deliveries are UPS. A refund is guaranteed if a club is returned undamaged within 30 days. Clubs are also available in ladies size, steel or graphite, same prices.

THE CONTROLLER HITS LONGER AND STRAIGHTER THAN ANY OTHER CLUB IN GOLF. IF IT DOESN'T CUT 5-10 STROKES, YOU OWE US NOTHING! ACT NOW!

incredible!



SPDT switch dc to 5GHz with built-in driver

Truly incredible...a superfast 3nsec GaAs SPDT reflective switch with a built-in driver for only $19.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' YSW-2-50DR?

Check the outstanding performance specs of the rugged device, housed in a tiny plastic case, over a -55° to +85° C span. Unit-to-unit repeatability for insertion loss is 3-sigma guaranteed, which means less than 15 of a 10,000-unit production run will come close to the spec limit. Available for immediate delivery in tape-and-reel format for automatic placement equipment.

SPECIFICATIONS
YSW-2-50DR

	dc-500MHz	500-2000MHz	2000-5000MHz
Insertion loss, typ (dB)	0.9	1.3	1.4
Isolation, typ(dB)*	50	40	28
1dB compression, typ (dBm @ in port)	20	20	24
RF input, max dBm (no damage)	22	22	26
VSWR (on), typ	_____	1.4	_____
Video breakthrough to RF, typ (mV p-p)	_____	30	_____
Rise/Fall time, typ (nsec)	_____	3.0	_____

*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

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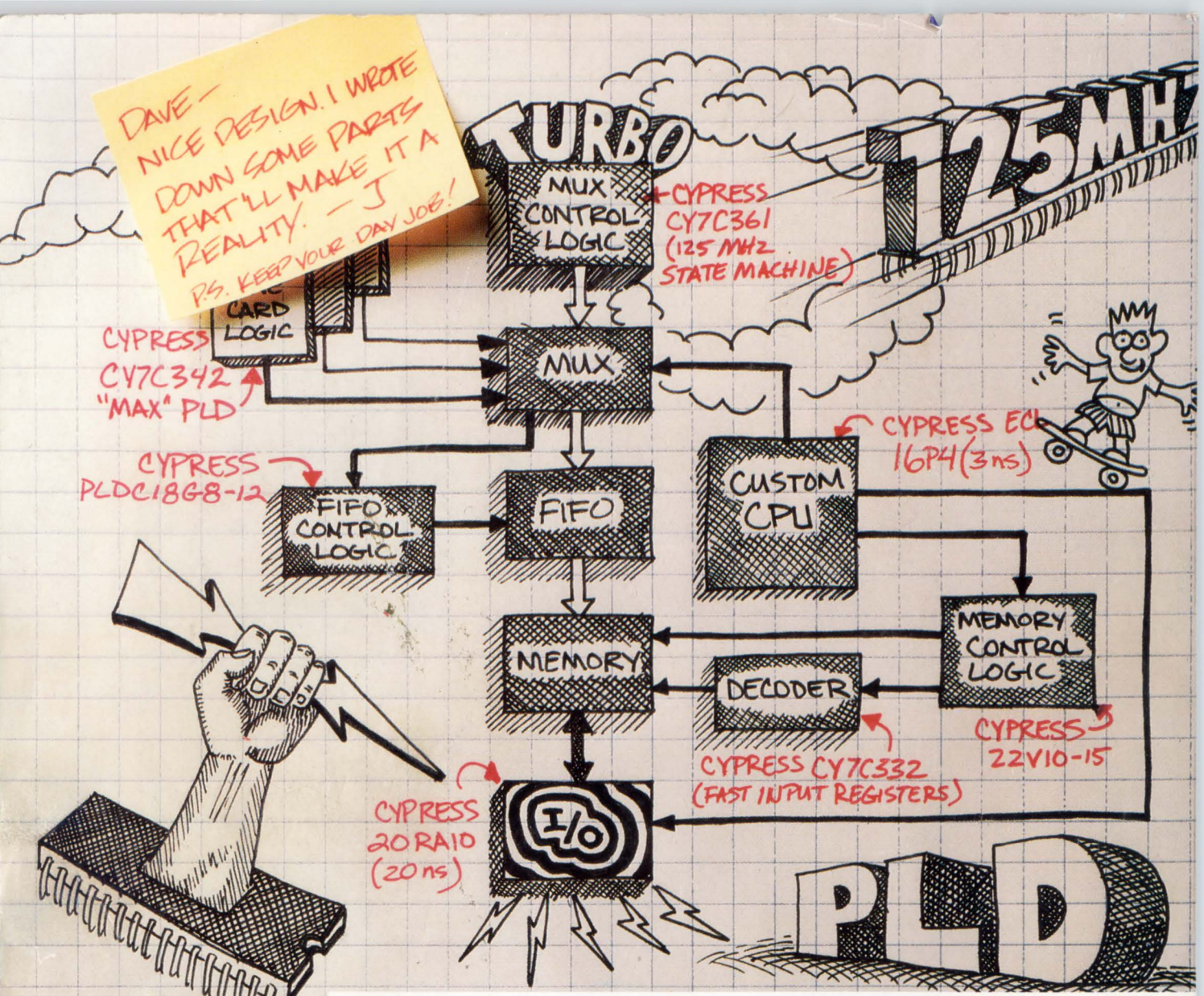
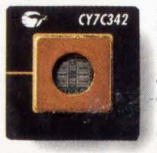
CIRCLE 153



No matter where you're going, or how fast, we have the right PLD.



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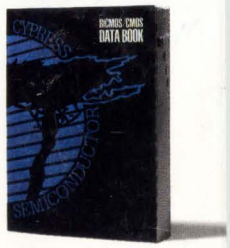

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