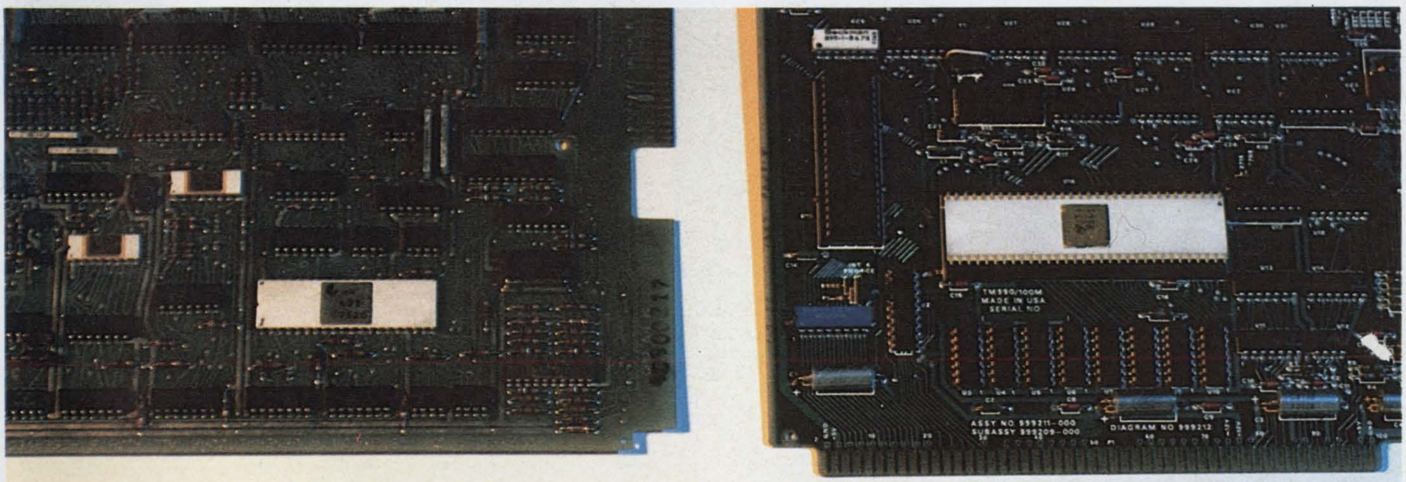
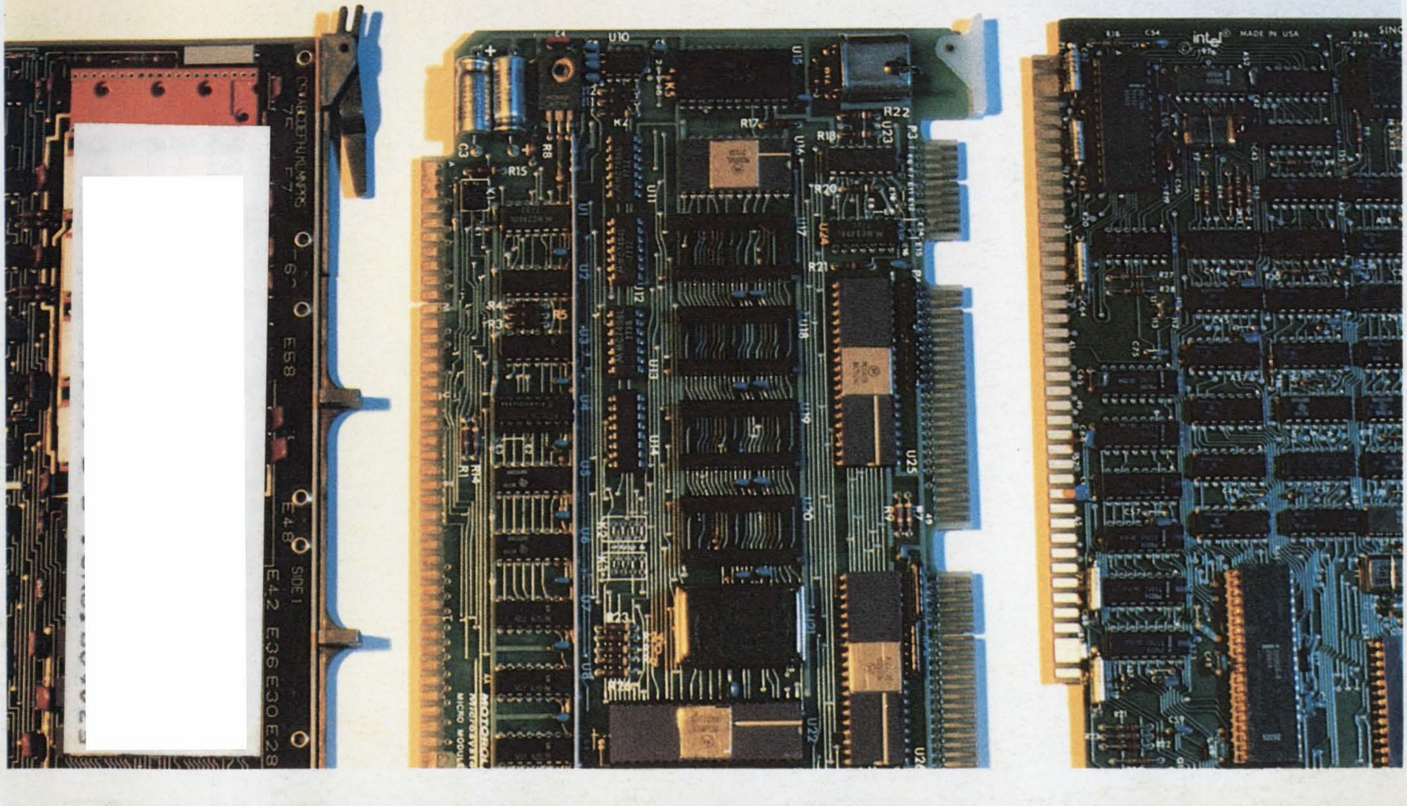
Electronic Design® VOL. 26 NO. 11
FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE
MAY 24, 1978

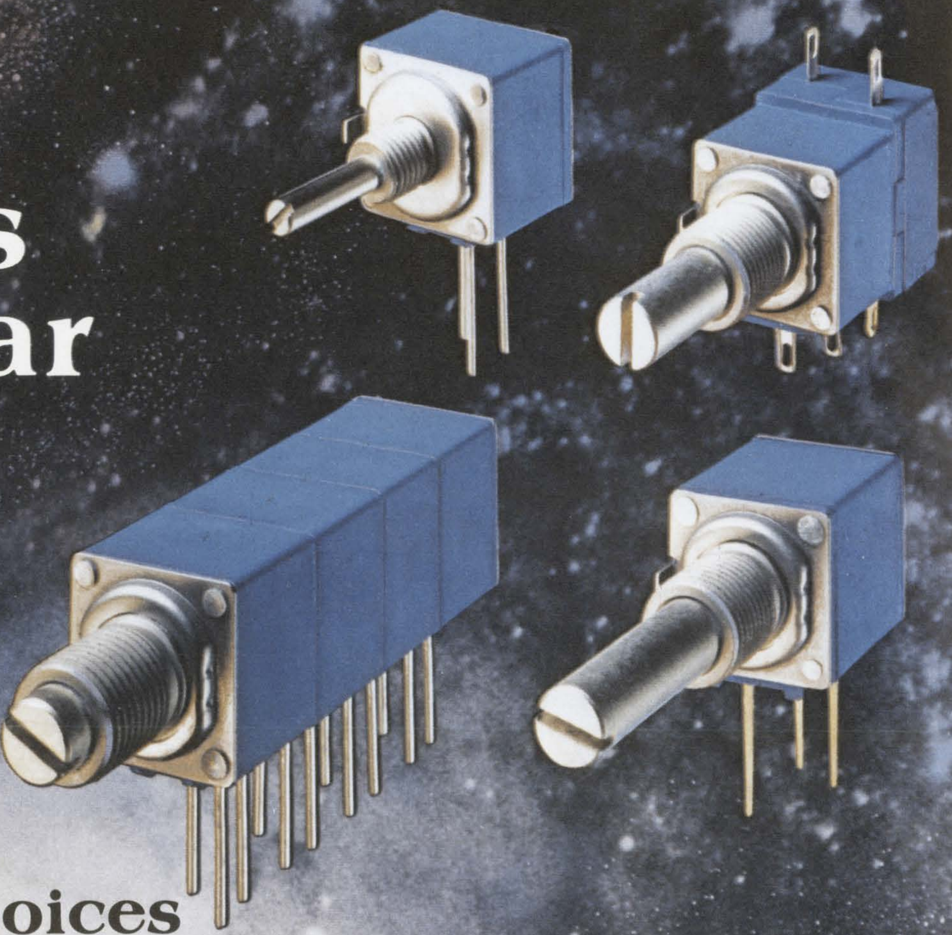
Selecting a microcomputer no longer means studying dozens of manuals. Electronic Design's μC Data Manual summarizes each board's performance and all the available hardware and software support. The Manual includes guidance on performance limits, spec pitfalls and software basics in articles starting on Pg. 65.



Microcomputer Data Manual



Bourns Modular Pots...



A Galaxy of Design Choices

A BILLION DESIGN CHOICES:
(1) Precision potentiometers, semi-precisions, panel controls or switch modules, (2) Cermet, conductive plastic or wirewound elements, (3) Linear tapers, CW or CCW audio tapers at various tolerances, (4) A wide selection of bushings and single or dual concentric machined shaft options, (5) Gangable up to four cups, (6) PC pins or solder lugs, and (7) A wide range of resistance values. We offer the broadest line of modular pots and switches available anywhere.

PRECISIONS — Model 83/84 10-turn wirewounds with modular construction and PC pins. A Bourns exclusive.

SEMI-PRECISIONS — ±1% to ±2.5% zero-based linearity range achieved by laser tailoring. The Model 87/88 fills the gap between low-performance controls and high-cost precisions. Another Bourns exclusive.

PANEL CONTROLS — Economical Model 81/82 single turn pots with independent linearity of ±5% and low 1% CRV.

SWITCHES — Click them. There's a touch of class. The Model 85/86 combines Bourns modular pots with optional rotary switches. Modular switches have low contact resistance and a positive action detent at CW or CCW end.

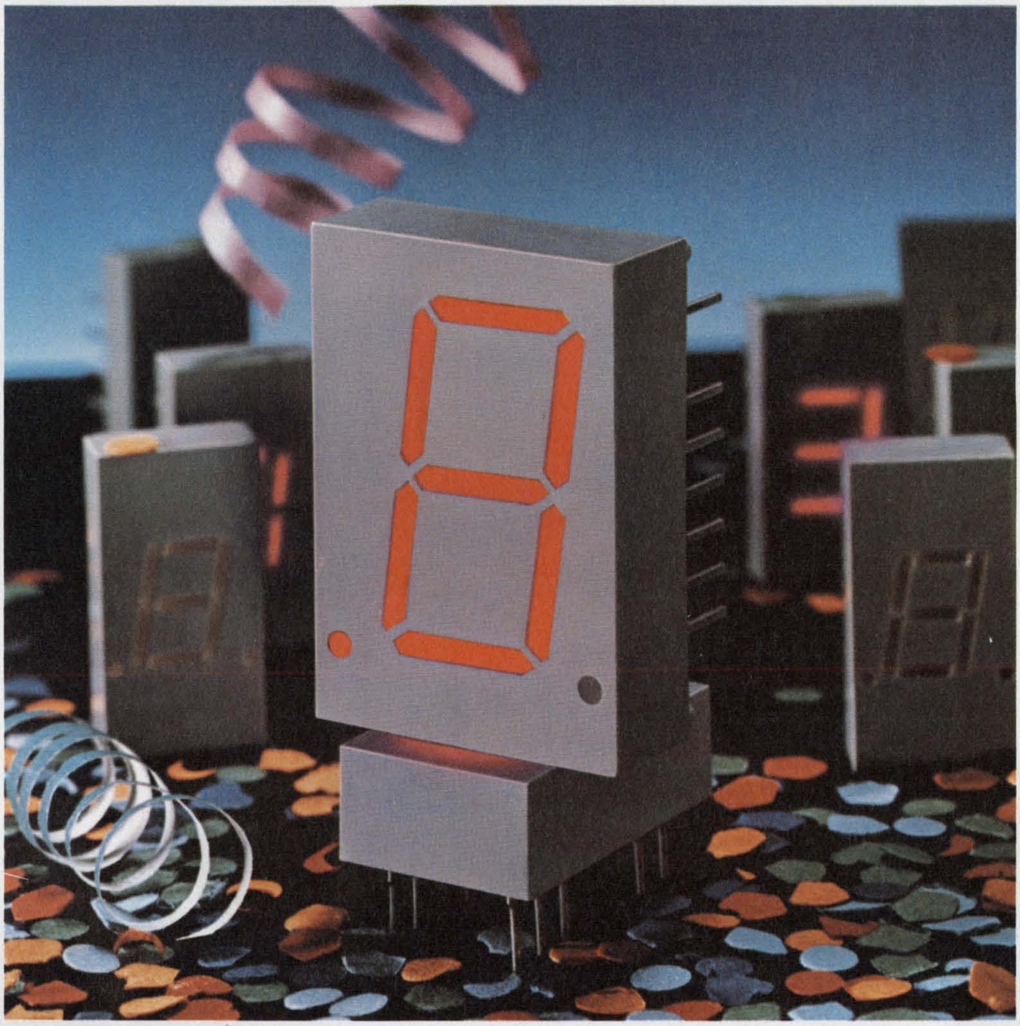
And, there's more: Consistently smooth, quality feel, regardless of model or modular configuration (torque range of only .3 to 2.0 oz.-in.); Bourns quality; competitive pricing; and universal flexibility. Send today for your new catalogs on the Model 80 family of modular pots and switches . . . Reach for a star from the Bourns Galaxy.

TRIMPOT PRODUCTS DIVISION, BOURNS, INC., 1200 Columbia Avenue, Riverside, CA 92507. Phone: 714 781-5122 — TWX 910 332-1252.

BOURNS®

For Immediate Application — Circle 130 • For Future Application — Circle 230

SURPRISE!



HP's New Display is a Big Show Off.

Big, because they're a full 20mm (0.8″) high with bright, clear viewing as far as 10 metres. They show off well too, with excellent readability in bright ambient conditions because of a gray body color and untinted segments. This is HP's new family of HDSP-3400 Series of seven-segment red displays.

IC compatible, they're ideal for electronic instrumentation, point-of-sale terminals, TV's, weighing scales and digital clocks, and other applications where you need a big, easy-to-read display. And power requirements are low since they utilize a single GaAsP chip per segment.

Units are priced at $1.80* in quantities of 1000. For immediate delivery, call any franchised HP distributor. In the U.S. contact Hall-Mark, Hamilton/Avnet, Pioneer-Standard, Schweber, Wilshire or the Wyle Distribution Group (Liberty/Elmar). In Canada, call Hamilton/Avnet or Zentronics, Ltd. *U.S. Domestic Price Only.

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1507 Page Mill Road, Palo Alto, California 94304

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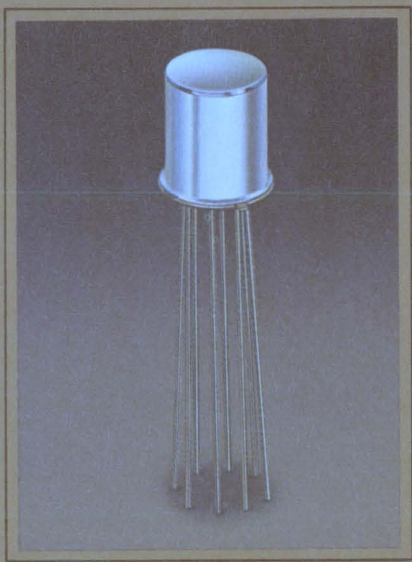
01804

CIRCLE NUMBER 2

TO-5 RELAY UPDATE

Still the world's smallest RF relay ...and the stingiest



When we first told you about the inherently low inter-contact capacitance and low contact circuit losses of our TO-5 relays, you agreed that they were ideal for RF switching. And you began designing them in immediately. They provided high isolation and low I.L. up through UHF (typical performance 45 db isolation and 0.1 db I.L. at 100 MHz).

Then you discovered another benefit – particularly for hand-held transceivers where battery drain is critical. The TO-5 is very stingy on coil power; the sensitive versions draw only 210mV at rated voltage.

So if you're looking for a subminiature RF switch, don't settle for anything less than TO-5 technology. It's available in commercial/industrial as well as MIL qualified types. Write or call us today for full technical information.

TELEDYNE RELAYS

3155 W. El Segundo Blvd., Hawthorne, Calif. 90250 • (213) 973-4545

CIRCLE NUMBER 3

Electronic Design®

VOL. 26 NO. **11**

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

MAY 24, 1978

NEWS

TECHNOLOGY

PRODUCTS

DEPARTMENTS

Cover: Photo by Art Director, Bill Kelly, boards courtesy of Data General, Digital Equipment, Intel, Motorola, and Texas Instruments.

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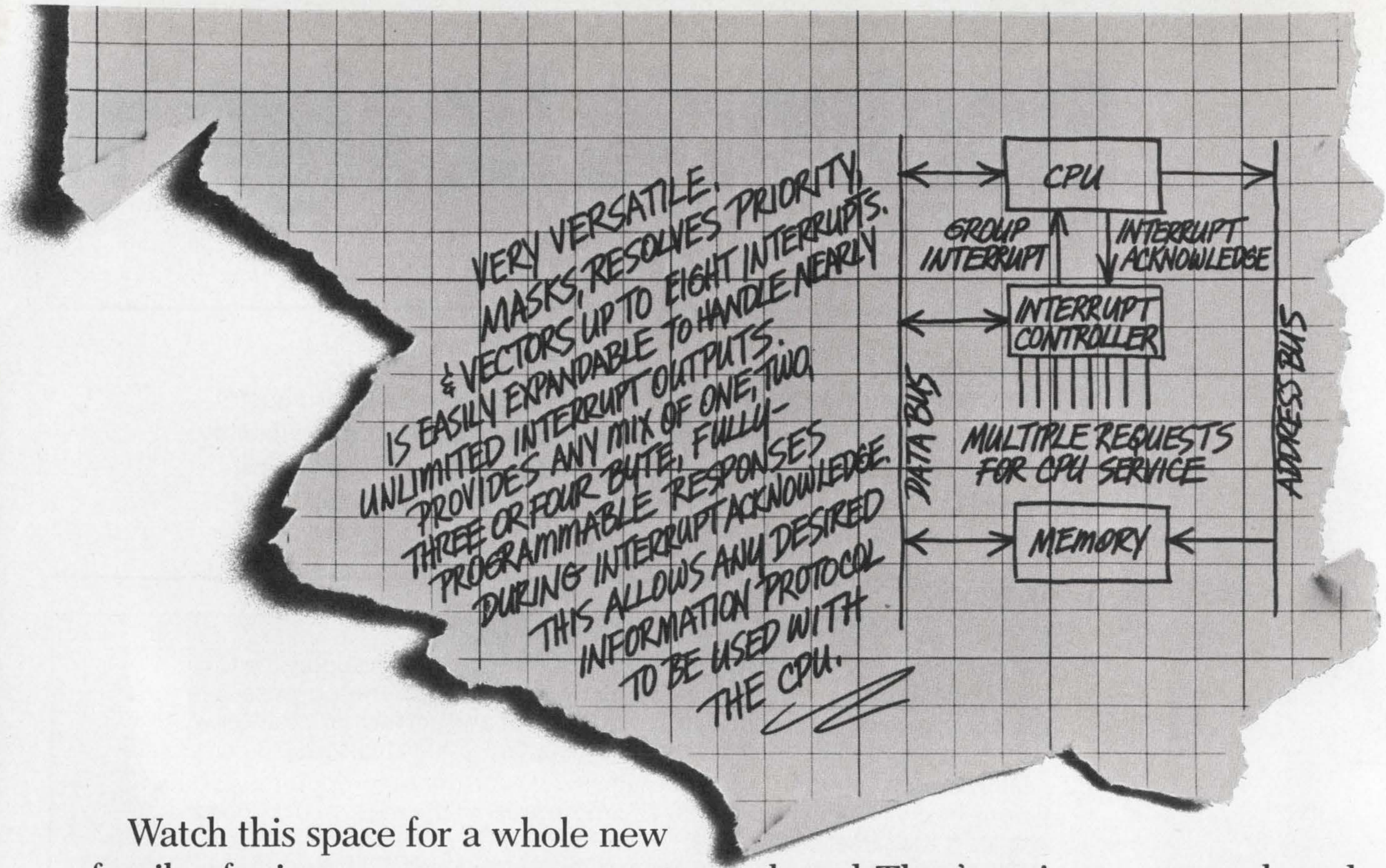


Watch this space for a whole new family of microprocessor components designed by Advanced Micro Devices. They're built from your side of the board. They're microprocessor-based solutions from a system viewpoint.

For example:

MOS MICROPROCESSING: WE'RE ON YOUR SIDE.

Across the desk

Standardized text editor is in committee

The lament of Mike Duncan for a standardized text editor (ED No. 3, Feb. 1, 1978, p. 120) has been answered. Honeywell Information Systems has produced a powerful and integrated text-processing *language* (TEX), which is the main starting point for X3J6, a new ANSI standardizing committee. TEX combines editing, computing, and resource management. It may be executed either from a terminal or as a program stored in a file.

If Mr. Duncan wishes to contribute to X3J6, he may inquire by writing to the ANSI Secretariat c/o Robert M. Brown, Secretary, X3, CBEMA—Suite 1200, 1828 L Street, N.W., Washington, DC 20036.

Robert L. Brandt
Consultant, Software Systems
Honeywell Information Systems
P.O. Box 6000
Phoenix, AZ 85005

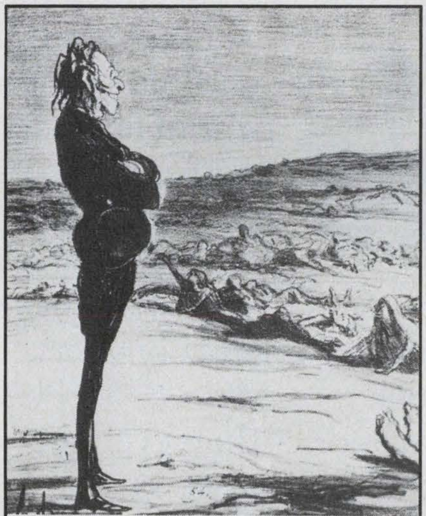
While you were away...

I enjoy your editorials about "Charlie's Company." Let me tell you my little encounter with his outfit.

I wanted to order some parts for a project I'm working on and needed price/availability information. So I called Charlie's company, a well-known semiconductor-chip house, and asked to speak to someone in sales/marketing. I was politely informed that "We're sorry, but everybody is in a meeting, and won't be available for a couple of hours." This was somewhat upsetting to me, a potential customer. Not all of the parts were sole-source, so I called Joe's company where a salesperson was available. I trust that Charlie's sales staff had a "profitable" meeting.

Roger E. Wiegel
Rockwell International
Collins Radio Group
Cedar Rapids, IA 52406

Misplaced Caption Dept.



And if we get this contract, there'll be a bonus for everybody—and not quite so much mandatory overtime.

Sorry. That's Honoré Daumier's "The Dream of the Inventor of the Needle Gun," which is in Le Charivari (A satyrical journal founded in 1832).

Focusing on drivel

It's unfortunate that your otherwise excellent Focus on Scientific Calculators (ED No. 5, March 1, 1978, p. 40) had to be muddied up by the arcane

(continued on page 16)

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Managing Editor, Electronic Design, 50 Essex St., Rochelle Park, NJ 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.

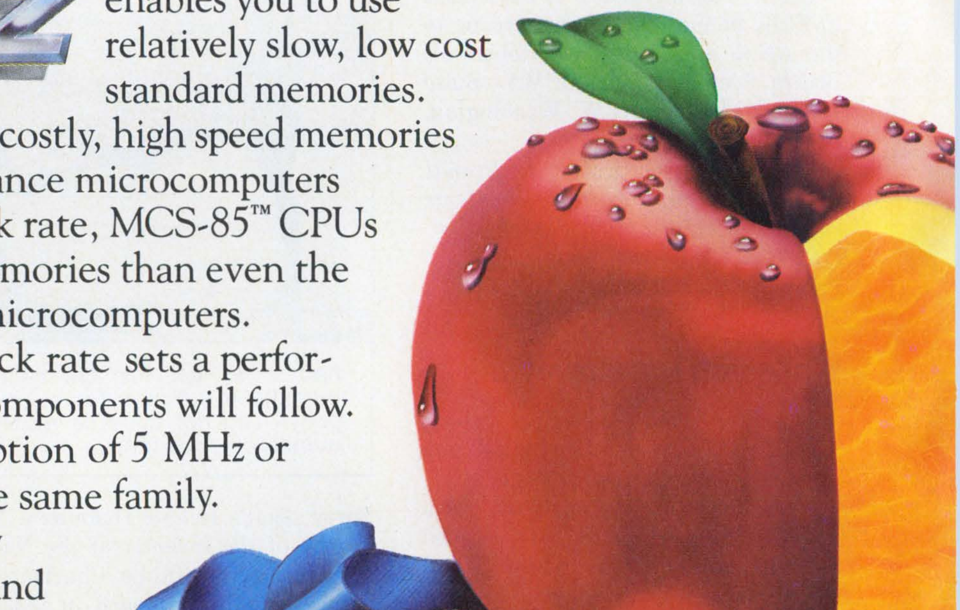
Intel delivers the 8-bit microcomputer,

Our newest 8085A selection is, quite simply, the world's fastest 8-bit microcomputer. It's the 8085A-2, with a 5 MHz clock rate—66% faster than a standard 3 MHz 8085A. Now you can achieve a new level of system performance using the world's best selling and best supported microcomputer family.

There's a surprising measure of economy that goes along with the 8085A-2's startling performance. Its superior bus architecture enables you to use relatively slow, low cost standard memories.

You don't need the costly, high speed memories that other high performance microcomputers demand. In fact, at any clock rate, MCS-85™ CPUs operate with 25% slower memories than even the most efficient competitive microcomputers.

The 8085A-2's faster clock rate sets a performance trend all MCS-85 components will follow. That gives you the design option of 5 MHz or 3 MHz operation within the same family. Of course the 8085A is fully compatible with the 8085, and offers the same growing selection of memories, programmable peripheral interfaces and support circuitry.



world's fastest the newest 8085A.

Join the Majority. Since its introduction, more major companies have chosen the 8085A than all other microcomputers combined. Almost overnight, the 8085A became the new industry standard.

Full software and bus compatibility with the familiar 8080 is one reason why. Designers have found they have a head start in implementing new MCS-85-based designs. And, the 8085A is your bridge to compatibility with upcoming Intel microcomputer advances.

#1 in Support. Choosing the right microcomputer means more than evaluating CPU performance. When you choose MCS-85, you get the highest performance CPU, plus a full family of compatible memories and peripherals, and access to our fast growing software library. Making Intel your microcomputer supplier unlocks the door to the industry's most comprehensive development support, too.

Our Intellec,® and new Intellec® Series II, Microcomputer Development System speeds your product to market. It's the only development system with two high level languages, PL/M and FORTRAN. It's the only development system that gives you symbolic debugging, using ICE-85™ in-circuit emulation. And it's the only development system you'll need for today's leading microcomputers, and tomorrow's, too.

Intel further supports our microcomputers worldwide with on-site FAE applications assistance, training classes and design seminars.

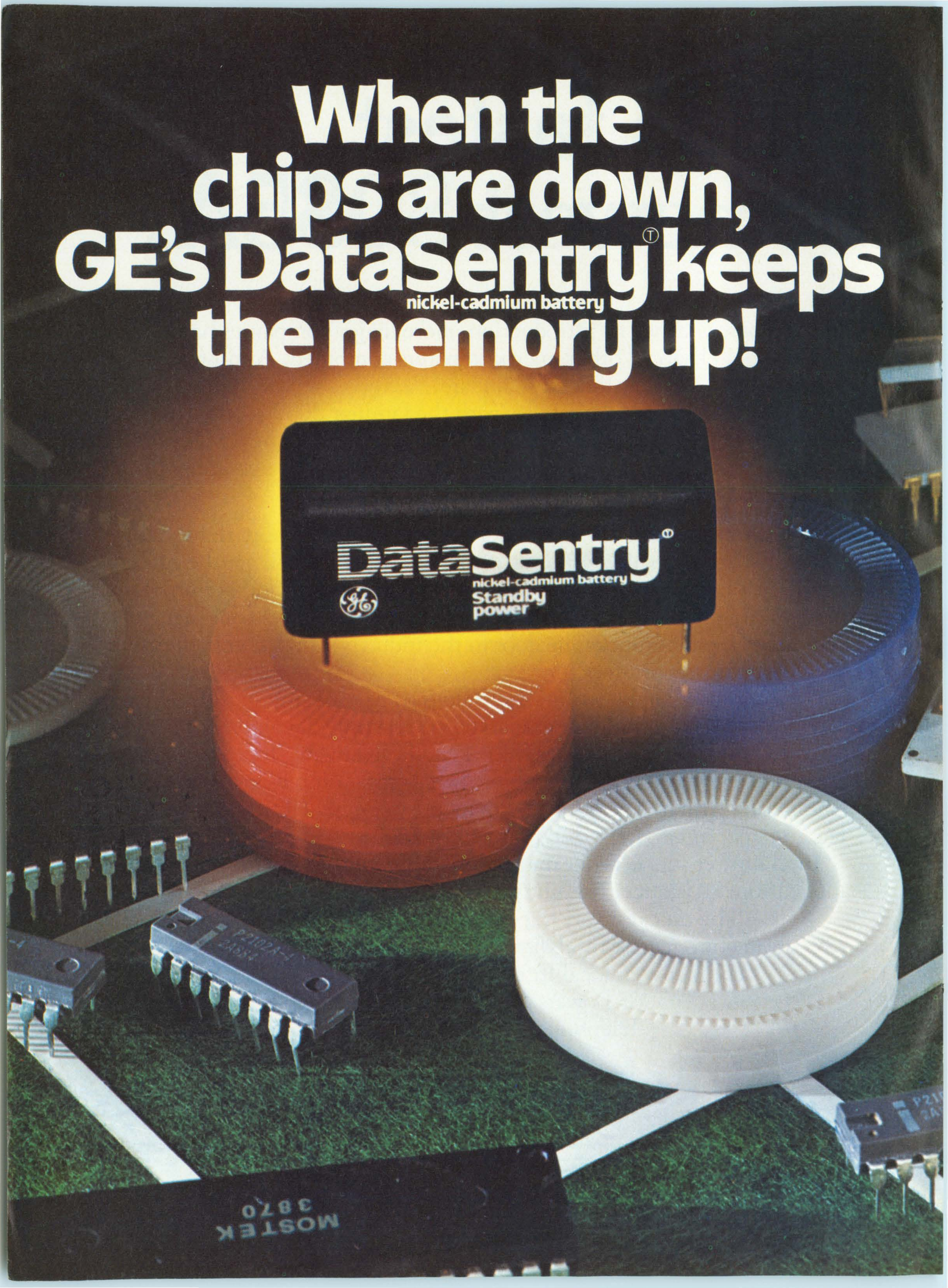
The quickest way to get started is to order MCS-85 components from your nearest Intel distributor. Or, for a new 8085A-2 data sheet, contact your local Intel sales office or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone: (408) 987-8080.

intel® delivers.

Europe: Intel International, Rue du Moulin a Pàpier, 51-Boite 1, B-1160, Brussels, Belgium. Telex 24814.
Japan: Intel Japan, K.K., Flower Hill-Shinmachi East Bldg. 1-23-9, Shinmachi, Setagaya-ku, Tokyo 154. Telex 781-28426.

Distributors: Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Sheridan, Wyle/Elmar, Wyle/Liberty, L.A. Varah or Zentronics.

CIRCLE NUMBER 7


When the
chips are down,
GE's DataSentry keeps
nickel-cadmium battery
the memory up!
DataSentry
nickel-cadmium battery
Standby
power

☐ **Consider the useful companion instruments that add to your measurement capabilities.**

You'll see why so many engineers around the world not only considered the HP 140 series but are now using them and appreciating their value.

Select either normal or variable persistence display, choose economy or high-resolution IF module. Then pick or change your frequency range by simply plugging in the appropriate tuning module.

No matter what range you're working in, you need reliable unambiguous answers. HP's spectrum analyzers give you accurate measurements over wide, distortion-free dynamic ranges, time after time.

MODEL #	DESCRIPTION	DOMESTIC US PRICE
140T 141T	Normal Persistence Display Variable Persistence/Storage Display	\$1600 \$2500
8552A 8552B	Economy IF Section High Resolution IF Section	\$3175 \$3875
8556A	20 Hz-300 KHz RF Section	\$2525
8553B 8443A	1 kHz-110 MHz RF Section Companion Tracking Generator/Counter	\$3250 \$4775
8554B 8444A	100 kHz-1250 MHz RF Section Companion Tracking Generator	\$4300 \$3500
8555A 8445B	10 MHz-40 GHz RF Section 10 MHz-18GHz Automatic Preselector	\$7900 \$3050

Call your nearby HP field engineer or write for the full story on value in spectrum analyzers.

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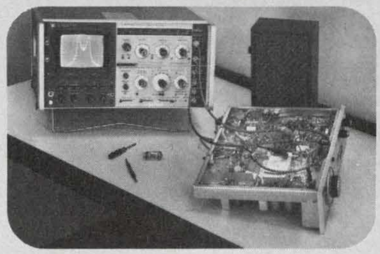
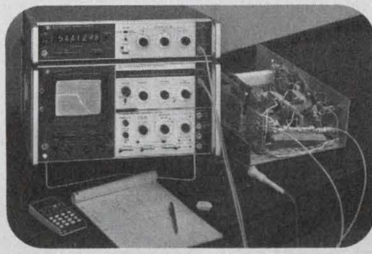
20 Hz to 300 kHz



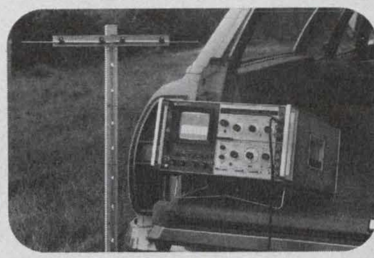
The 8556A tuner covers 20 Hz to 300 kHz and comes with a built-in tracking generator. It's calibrated for measurements in both 50 and 600 ohm systems, with accuracies better than ±1 dB. Highest resolution is 10 Hz.

1 kHz to 110 MHz



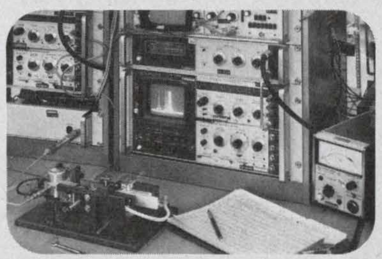
The 8553B takes you from 1 kHz to 110 MHz with −140 dBm sensitivity and resolution as high as 10 Hz. Signals can be measured with ±1¼ dB accuracy. Choose the companion HP 8443A Tracking Generator/Counter for wide dynamic range swept frequency measurements and precise frequency counting.

100 kHz to 1250 MHz



Use the 8554B tuning section to cover the 100 kHz to 1250 MHz range. Maximum resolution is 100 Hz. Measure with ±1¾ dB accuracy. Its companion HP 8444A Tracking Generator (500 kHz to 1300 MHz) also works with the 8555A tuning section.

10 MHz to 40 GHz



For 10 MHz to 40 GHz, choose the 8555A. Its internal mixer covers to 18 GHz, accessory mixer for 18-40 GHz. Maximum resolution is 100 Hz. Measure with ±1¾ dB accuracy to 6 GHz, ±2¾ dB to 18 GHz. For wide scans free from unwanted response between 10 MHz and 18 GHz, add the HP 8445B Automatic Preselector.

45803

CIRCLE NUMBER 9

So Ours Let You Change Applications. . .Without Changing Your Logic Analyzer

The logic analyzer . . . it's become *the* essential measurement tool for digital designers like you. But just a logic analyzer isn't enough. Because your logic analyzer should be as versatile as you are.

Our dictionary calls versatile "capable of turning with ease from one to another of various tasks." And versatile is exactly what you have to be in your day to day digital design work. Versatile in the tasks you perform, and versatile in your role as part of the design team.

And so you need a logic analyzer every bit as versatile as you are. One that lets you "turn with ease." From hardware to software analysis. Or from microprocessor to non-microprocessor design.

TEKTRONIX LOGIC ANALYZERS: THE VERSATILE ONES

VERSATILE CONFIGURATIONS:

Concentrate on new applications — not on learning a new logic analyzer. Modules that plug in to *any* Tektronix 7000 Series oscilloscope let you "build" the logic analyzer *you* need.

VERSATILE FEATURES:

You — not the logic analyzer — decide how you'll look at logic. Go from state tables to mapping to timing — without going to another logic analyzer. Touch a button and select binary, hex, octal, mapping, timing, GPIB, or ASCII.

You need confidence in your measurements. So you want the best possible resolution. And that means you need to sample faster than the system under test — the faster the better. So Tek Logic Analyzers let you sample asynchronously up to 100 MHz at a resolution of 15 ns.

You're looking at a lot of information in digital systems — yet you want to find your problem in one pass. Our large, formattable 4K memory can deliver up to 1024 bits per channel.

You need to see what's on — and off — the bus. Synchronous and asynchronous operation in the *same* logic analyzer lets you perform software and hardware analysis.

Your design has to work right every time. Automatic Data Comparison will verify it for you. Or identify any fault. While you're busy elsewhere.

VERSATILE APPLICATIONS:

Tektronix Logic Analyzers stay with you. For design; debugging; and troubleshooting. For hardware and software analysis. For timing and state applications. For *whatever* job is at hand.

Versatile — so you can do today's job and tomorrow's. So you can change applications without changing your logic analyzer.

Contact Tektronix Inc., P.O. Box 500, Beaverton, OR 97077. In Europe, Tektronix Ltd., P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

Tektronix
COMMITTED TO EXCELLENCE

1 Look at logic in your language: choose binary, hex, octal, mapping, timing, GPIB, or ASCII

2 The faster your measurements, the better the resolution. Sample up to 100 MHz at 15 ns resolution

3 See all the information you need to see with our large 4K formattable memory

4 Get the whole picture: verify logic on the bus synchronously; verify timing sequences asynchronously

5 Concentrate on other work while Automatic Data Comparison verifies operation — or identifies faults

TECHNICAL DATA CIRCLE 10 ON READER SERVICE CARD

DEMONSTRATION CIRCLE 11 ON READER SERVICE CARD

TEKTRONIX LOGIC ANALYZERS THE VERSATILE ONES

Across the desk

(continued from page 7)

drivel of "What is the answer: 2 + 3 × 4 = 20 or 14?"

Infants learning their math tables can handle numbers with no intrinsic value because they're only concerned with one mathematical function (i.e., multiplication). But engineers and scientists almost invariably assign values to their numbers: apples or oranges, degrees or dollars, milliamps or mugwumps. The problem, then, is not $2 + 3 \times 4 = ?$, but either $(2 + 3) \times 4 = ?$, or $2 + (3 \times 4) = ?$ The parentheses inherently exist. "Which arithmetic?" indeed! I can't imagine difficulties with the Algebraic Operation System unless one doesn't understand the problem supposedly being solved.

Tom MacLaren, MTS

Teledyne Controls
200 N. Aviation Blvd.
El Segundo, CA 90245

Licensing means little

Congratulations, George. You finally got out of those mythology editorials and made a mighty stroke with your pen—"Protecting the Members" (ED No. 2, Jan. 18, 1978, p. 55).

Every time I hear ramblings for more engineer licensing and stronger engineering societies I cringe at the social stupidity of great engineering minds. We have licensed TV and auto repair and have instituted so many other so-called social-protection laws that Henry Ford, if he'd been faced with the current situation, would have given up and gone to Europe before inventing the Model T.

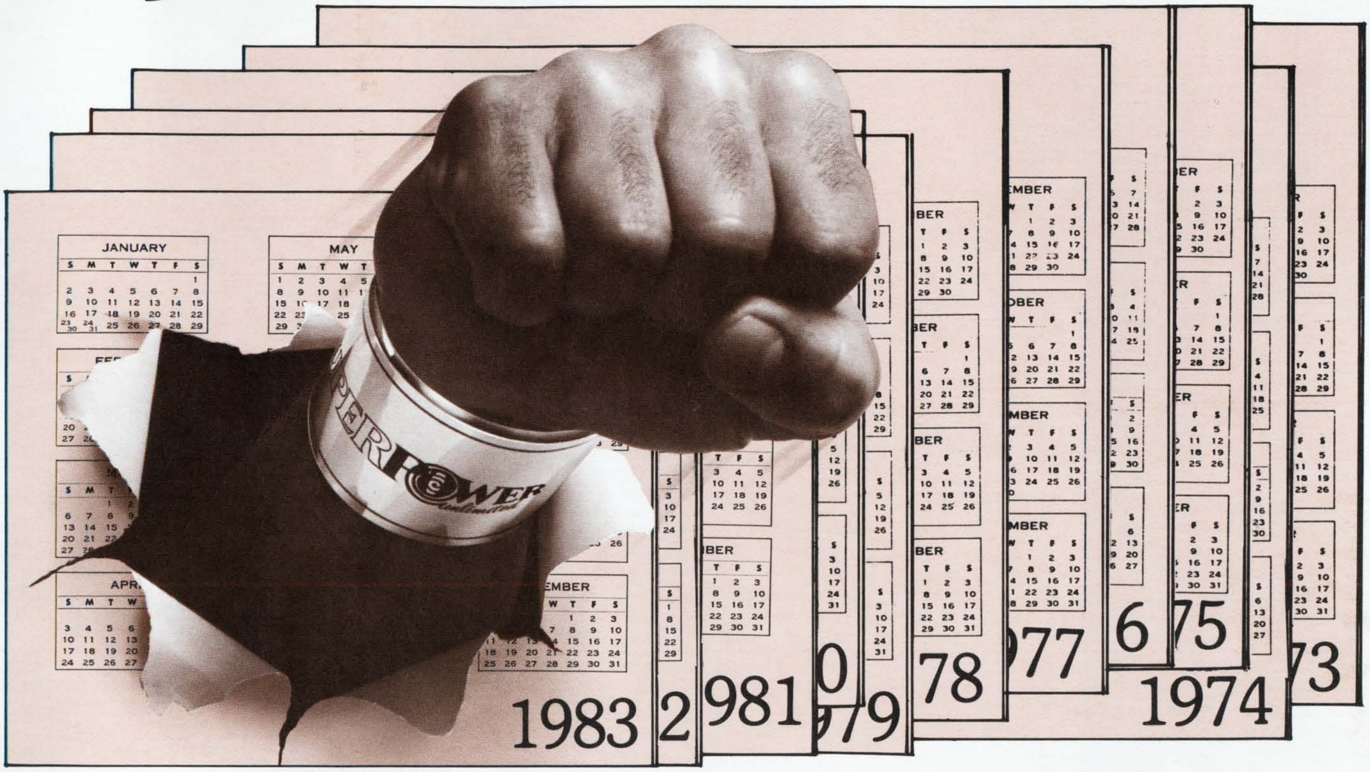
I bought an RCA TV set for Christmas. At 60 days (end of warranty), it refused to run more than 10 minutes. This can happen with any manufacturer, so that's not the point. I took it into the shop with full agreement that I would pay for the repair. After two months I asked if I could sit down at the bench and work on it. I would not tackle it at home for lack of generators and circuit diagrams. In 30 minutes I had it working and paid the shop for its parts.

I'm about to celebrate my 60th birthday. At 55 I did not know any more about what was in a computer than a licensed doctor or lawyer. Since then

(continued on page 26)

TEAR ALONG PERFORATION FOR SELECTOR GUIDE . . . USE IT AS POCKET GUIDE, TACK IT UP, OR FILE IT.

Switchmode power can move you years ahead of your competition.



Just like it's done for us.

State-of-the-art in silicon power transistors has long been one of Motorola's strengths. Our introduction of the Switchmode* concept three years ago with the 2N6542 through 2N6547 proved it to be the overwhelming choice of designers everywhere for switching power supplies and similar high voltage applications.

Because each and every Switchmode device is specifically *designed* and *characterized* for those applications.

Nobody else goes to the lengths we do to completely define all necessary performance data of this state-of-the-power art. No unknowns, no empiricals, no vague or non-existent specs but solid, practical data from a pragmatic source . . . the Designers* Data Sheet. You're way ahead from the start.

There are imitators, but nobody offers anywhere near the broad selection of unique device-tools we do to make your design job even easier—nearly 70 individual Switchmode discrete and Darlington parts for applications from 0.5 to 50 A, 200 to 750 V. We cover all the bases—and at the right price, naturally.

There are now 16 economical Darlington devices available from 8 to 50 A, 450 to 750 V. The new MJ10008/9 Darlingtons offer 20 A, 500 V capability with max hot inductive crossover time of 1.6 μs and min gain of 30 at 10 A. 100-ups are just $6.25 and $7.65. And our MJ10004-5, 20 A, 450 V series offering 1.5 μs max crossover and min gain of 40 at 10 A is value-priced at $6.25 and $7.65. The MJ13014/15 10 A, 400 V discrete units provide 1.5 μs max crossover time and min gain of 8 at 5 A. Prices are only $3.45 and $4.05. And the new high current MJ10015/16 50 A, 500 V Darlingtons provide 1.0 μs time and gain of 25 at 20 A with price tags of $13.80 and $16.85. Plus we've got TO-220s including the new discrete MJE13006/7 with 8 A, 400 V performance and low cost of $1.95 and $2.60.

These or any of the industry-leading Switchmode units on the next page are available now from factory or your authorized distributor for your years-ahead designs.

Stay with us. There's a lot more from a SuperPower.

*Trademark Motorola Inc.

MOTOROLA

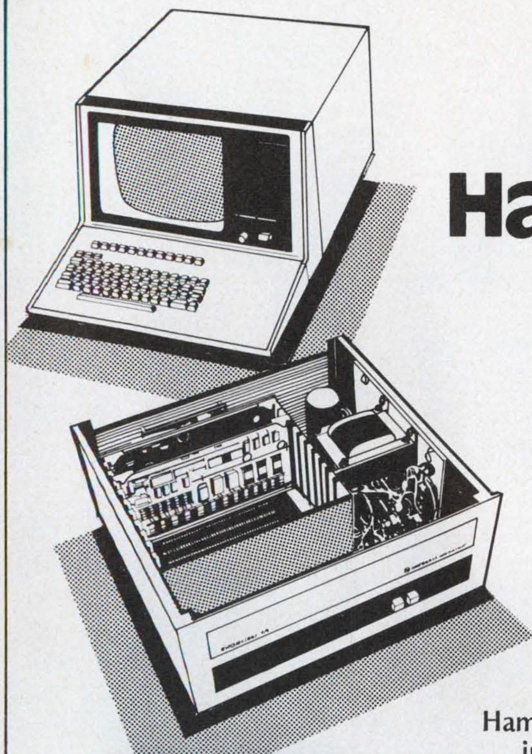
Semiconductor Group

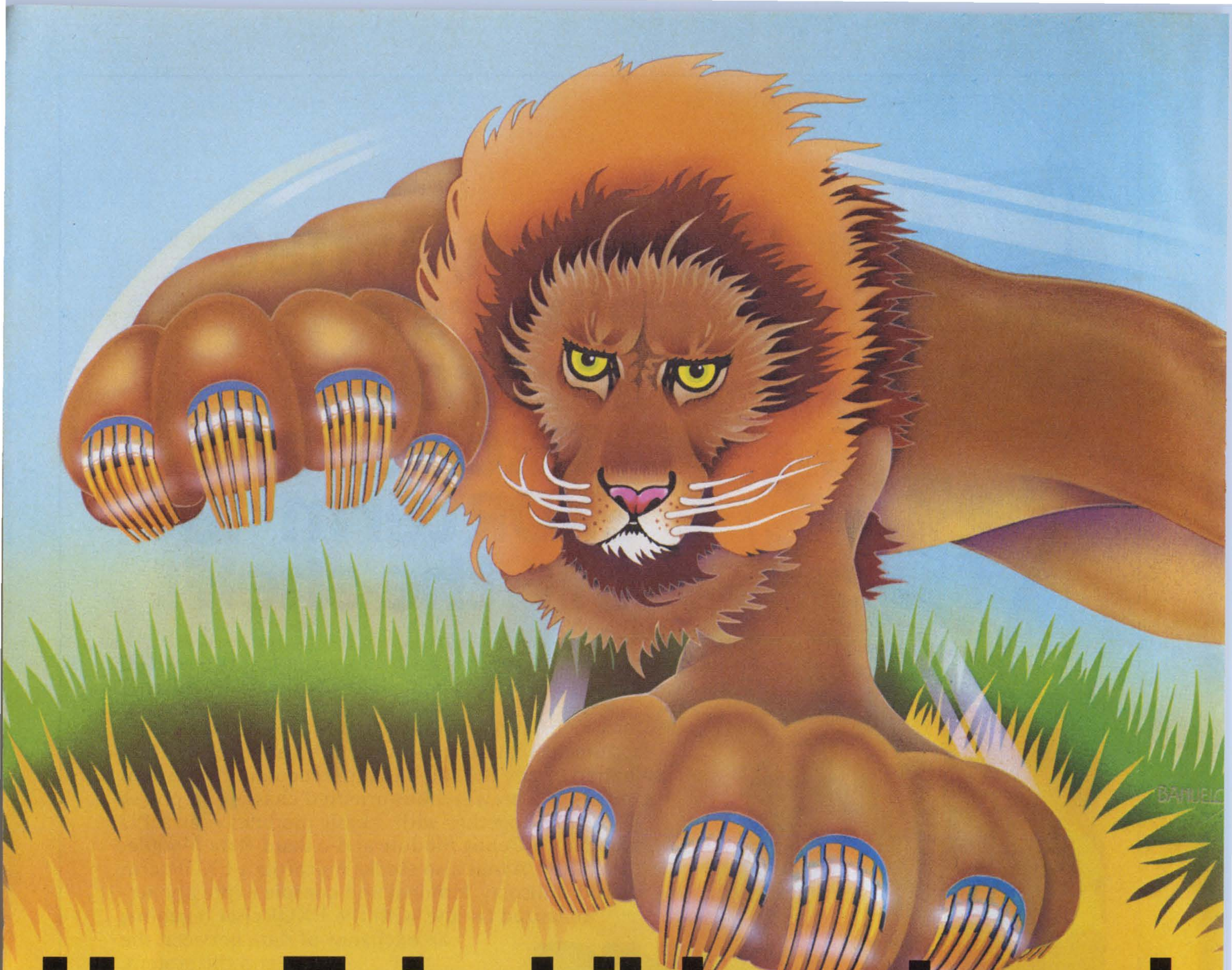
Motorola Switchmode* Power Transistors

V_{CEO} (sus) Volts Min	I_C Cont Amps Max	V_{CEX} Volts Min	Device Type NPN unless otherwise noted	h_{FE} @ Min/Max	I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	Case JEDEC/Motorola
750	8	1500	MJ12005	5 min	5		1	5	4 typ	TO-3/11
	5	1500	**MJ12004**	2.5 min	4.5		1	4.5	4 typ	TO-3/11
	2.5	1500	**MJ12002**	1.11	2		1	2	4 typ	TO-3/11
700	8	1400	MJ10011#	20 min	4		1	4		TO-3/11
600	15	700	• **MJ10014**##	10/70	10	2.5	0.8	10		TO-3/11
550	15	650	• **MJ10013**##	10/70	10	2.5	0.8	10		TO-3/11
500	50	750	• **MJ10016**##	10 min	40	2.5	0.5	20		TO-3 Mod/197
	20	750	• **MJ10009**##	30/300	10	2	0.6	10	8**	TO-3/11
		600	• **MJ13335**	10/60	5	4	0.7	10		TO-3/11
450	20	650	• **MJ10008**##	30/300	10	2	0.6	10	8**	TO-3/11
	20	550	• **MJ13334**	10/60	5	4	0.7	10		TO-3/11
400	50	600	• **MJ10015**##	10 min	40	2.5	0.5	20		TO-3 Mod/197
	20	500	**MJ10001**#	40/400	10	3	1.8	10	10**	TO-3/11
			MJ10005##	40/400	10	1.5	0.5	10	10**	TO-3/11
			• **MJ13333**	10/60	5	4	0.7	10		TO-3/11
	15	850	**2N6547**	6/30	10	4	0.7	10	6	TO-3/11
	12	700	**MJE13009**	6/30	8	3	0.7	8	4**	TO-220/221A
	10	550	MJ10012#	100/2K	6	15	15	6		TO-3/11
		500	**MJ10003**#	30/300	5	2.5	1	5	10**	TO-3/11
			MJ10007##	30/300	5	1.1	0.25	5	10**	TO-3/11
	10	450	• **MJ13015**	8/20	5	2	0.5	5		TO-3/11
	8	850	**2N6545**	7/35	5	4	1	5	6	TO-3/11
		700	**MJE13007**	6/30	5	3	0.7	5	4	TO-220/221A
	5	850	**2N6543**	7/35	3	4	0.8	3	6	TO-3/11
	4	700	• **MJE13005**	6/30	3	3	0.7	3	4	TO-220/221A
	1.5	700	**MJE13003**	5/25	1	4	0.7	1	5	TO-126/77R
	0.5	400	**MJ4647**	20 min	0.5	0.72†		0.05	40	TO-39/79
350	20	450	**MJ10000**#	40/400	10	3	1.8	10	10**	TO-3/11
			MJ10004##	40/400	10	1.5	0.5	10	10**	TO-3/11
		450	• **MJ13332**	10/60	5	4	0.7	10		TO-3/11
	15	375	2N6251	6/50	10	3.5	1	10	2.5	TO-3/11
	10	400	• **MJ13014**	8/20	5	2	0.5	5		TO-3/11
	8	700	2N6308	12/60	3	1.6	0.4	5	5	TO-3/11
		450	**MJ10002**#	30/300	5	2.5	1	5	10**	TO-3/11
			• **MJ10006**##	30/300	5	1.1	0.25	5	10**	TO-3/11
	5	450	2N6499	10/75	2.5	1.8	0.8	2.5	5	TO-220/221A
	2	400	2N6213-PNP	10/100	1	2.5	0.6	1	4	TO-66/80
325	8	700	MJ9000	3.75 min	6		1.1	6		TO-3/11
	5	700	MJ3030	3.75 min	3		1	3		TO-3/11
		350	2N6235	25/125	1	3.5	0.5	1	20	TO-66/80
300	15	650	**2N6546**	6/30	10	4	0.7	10	6 to 24	TO-3/11
	12	600	**MJE13008**	6/30	8	3	0.7	8	4**	TO-220/221A
	8	650	**2N6544**	7/35	5	4	1	5	6	TO-3/11
		600	2N6307	15/75	3	1.6	0.4	3	5	TO-3/11
			MJE13006	6/30	5	3	0.7	5	4	TO-220/221A
	5	650	**2N6542**	7/35	3	4	0.8	3	6	TO-3/11
		400	2N6498	10/75	2.5	1.8	0.8	2.5	5	TO-220/221A
	4	600	• **MJE13004**	6/30	3	3	0.7	3	4	TO-220/221A
	2	500	2N3585	25/100	1	4	3	1	10	TO-66/80
			2N6422-PNP	25/100	1	4	3	1	10	TO-66/80
		350	2N6212-PNP	10/100	1	2.5	0.6	1	4	TO-66/80
	1.5	600	**MJE13002**	5/25	1	4	0.7	1	5	TO-126/77R
	1	300	2N5345	25/100	0.5	0.6	0.1	0.5	60	TO-66/80
	0.5	300	MJ4646	20 min	0.5	0.72†		0.05	40	TO-39/79
275	15	300	2N6250	8/50	10	3.5	1	10	2.5	TO-3/11
	8	500	2N6306	15/75	3	1.6	0.4	3	5	TO-3/11
	7	300	2N6077	12/70	1.2	2.8	0.3	1.2	7	TO-66/80
	5	500	MJE3029	30 min	0.4		1	3		TO-3/11
		275	2N6234	25/125	1	3.5	0.5	1	20	TO-66/80
	2	375	2N3584	25/100	1	4	3	1	10	TO-66/80
			2N6421-PNP	25/100	1	4	3	1	10	TO-66/80
	1	250	2N5344	25/100	0.5	0.6	0.1	0.5	60	TO-66/80
250	20	350	• **MJ13331**	8/40	10	3.5	0.7	10	5	TO-3/11
	7	275	2N6078	12/70	1.2	2.8	0.3	1.2	7	TO-66/80
	5	350	2N6497	10/75	2.5	1.8	0.8	2.5	5	TO-220/221A
225	5	250	2N6233	25/125	1	3.5	0.5	1	20	TO-66/80
	2	275	2N6211-PNP	10/100	1	2.5	0.6	0.1	4	TO-66/80
200	20	300	• **MJ13330**	8/40	10	3.5	0.7	10	5	TO-3/11
	15	225	2N6249	10/50	10	3.5	1	10	2.5	TO-3/11
	2	200	2N5052	25/100	0.75	3.5	1.2	0.75	10	TO-66/80
	0.5	200	MJ4645	20 min	0.5	0.72†		0.05	40	TO-39/79

•New Device #Darlington ##Darlington with speed-up diode. †t_{off} ** h_{fe} @ 1 MHz. **Heavy black type** denotes Designers Data Sheet characterization.
*Trademark Motorola Inc.

11614 PRINTED IN USA 3-78 IMPERIAL LITHO B70290





How Fairchild captured the lion's share of the LSI test market.

We were with you in the beginning. When you were pioneering new LSI devices, we were creating the technology to test them.

Today we're the leader. There are over 2000 Fairchild test systems installed throughout the world. Last year alone we shipped more LSI, VLSI and memory test systems than all the competition combined.

What's it mean to you? If you're a maker or user of LSI, Fairchild can provide the system and the service to solve almost any testing problem.

A system for every application.
Whether your needs are for high-volume production testing, incoming inspection, development engineering or circuit evaluation, there's a Fairchild system that's right for you. Our testers are modular,

easily tailored and they're efficient–they'll provide 50 to 100 percent greater throughput than competing systems.

Sentry V for economical LSI testing. It's the most advanced LSI test system in its price class. Sentry 5 delivers high throughput, exceptional accuracy and the flexibility to handle all modern technologies.

Sentry VII for LSI engineering and characterization. It's the industry standard. Sentry 7's multitasking software and distributed processing cuts device characterization to a fraction of the time required by other systems.

Sentry VIII for VLSI. When it comes to testing VLSI, Sentry 8 is the only game in town. It's the only commercial 120-pin test system with data pattern handling, multiple clocking, real-time error analysis and high speed memory on every pin. Its test programs are also software-compatible with Sentry 5 and 7.

Xincom III for efficient memory testing. Xincom 3 is Fairchild's computer controlled memory test system for production testing, circuit characterization and incoming inspection. It has a host computer and up to four test satellites, each with two heads for testing RAMs, ROMs or PROMs in wafer form or packages. Its distributed architecture lets you test several devices simultaneously in real time with true foreground/background processing. Without slowing the testing function in the foreground, the background allows program development, data analysis and logging, printer/CRT interaction and more.

World-wide service for every system. Our products made us number one. Our service keeps us there. Training centers in the U.S., Europe and Asia have taught over 5000 engineers and technicians the latest in LSI testing techniques and equipment. Our worldwide applications staff will help you develop test programs to suit your requirements, so your Fairchild system is productive from the moment it's installed. And our field service group will be close by to keep your system running. Whether you're in Singapore or San Francisco.

Watch us roar. With the lion's share of the market, you have made Fairchild king of the testing jungle. We're constantly improving our technology to keep pace with yours. We intend to stay on top.

Find out more about Fairchild's LSI test systems. Mail the coupon today, or contact: **Fairchild Systems Technology,** 1725 Technology Drive, San Jose, California 95110 (408) 998-0123.

Fairchild: First in LSI testing

Please send data on the following: Sentry V ☐ VII ☐ VIII ☐
Xincom III ☐ I'd like to talk with a Fairchild engineer. ☐
My testing needs include:____________

Name____________
Title____________
Company____________
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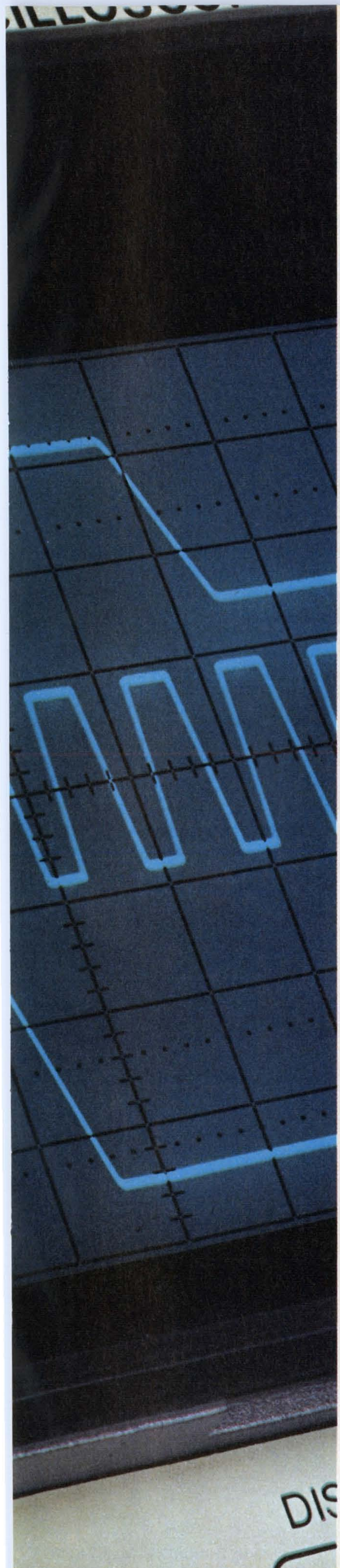
City______ State____ Zip____
Area Code____ Phone______

FAIRCHILD

CIRCLE NUMBER 13


1741A STORAGE OSC
STORE
ERASE
OR
VIEW
TIME
ERASE
(PUSH)
MAX
MAX
WRITE
STORE
DISPLAY



For one easy-to-use scope that: Captures single-shot events... Displays low-duty-cycle signals clearly... Provides three channels for the price of two...

HP's the Answer.

And the new 1741A is your scope. It gives you a unique combination of features for a moderately priced 100 MHz storage scope: Variable persistence for clear viewing of glitches and low-duty-cycle traces; storage for studying single-shot events; and third-channel trigger view for convenience in making simultaneous three-channel timing measurements.

Excellent variable persistence means a bright, sharp trace you'd expect only on a nonstorage scope. The result is an easy-to-read display of fast, low-duty-cycle repetitive signals. And the ability to see leading edges and glitches you'd otherwise miss.

Auto erase/Auto store. In Auto erase you adjust the display rate up to 2.5 per second. After that, it's all automatic, which means you simplify set-ups and eliminate smeared displays of digital data. It's a powerful tool for capturing those elusive glitches in data streams. In Auto store, your 1741A is armed, and as long as the instrument is fully operational and powered, will wait indefinitely, ready to store a random, single-shot event when it occurs.

Third-channel trigger view, selected at the push-of-a-button, lets you observe an external trigger signal along with channel A and B—three traces in all—so you can easily make timing measurements between all three channels. In most applications, that means three-channel capability for the cost of a two-channel variable persistence/storage scope.

For measurement convenience, the 1741A has a selectable 50 ohm input in addition to the standard 1 megohm input. A 5X magnifier permits two-channel measurements as low as 1 mV/div to 30 MHz, without cascading. You can even select a special modification (TV Sync) to tailor this scope for TV broadcast and R&D applications. Priced at \$4250*, the 1741A is an exceptional storage scope value.

Call your local HP field engineer today for all details. And for low-cost variable persistence/storage in a 15 MHz scope, ask him about HP's new 1223A.

And here's something NEW for scopes. HP's EASY-IC PROBES. A new idea for probing high-density IC circuits that eliminates shorting hazards, simplifies probe connection to DIP's and generally speeds IC trouble-shooting. Ask your HP field engineer about them.

*Domestic U.S.A. price only.

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CIRCLE NUMBER 14

The EMR is dead... Long live Motorola

The SPST electromechanical relay (EMR) is dead – killed by contact arcing, mechanical wearout and incompatibility with modern circuitry.

We know – and you know – where multiple-pole, higher current contactor applications are required, it'll still be around.

But for the bulk of logic level designs where you need the advantages of solid-state reliability, convenience, versatility, standard packages, multiple sourcing and low cost... solid-state relays are the *only* way to go!

Now Motorola presents a new, broad line of SSRs and I/O modules vastly superior to the century-old EMR and affording significant advances even over similar contemporaries. Advances that spell quality throughout.

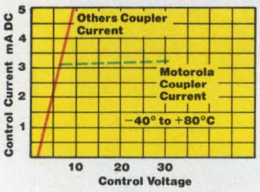
• Like better input characteristics for optimized opto coupler life. The more current, the shorter the coupler's life expectancy. Our SSRs limit coupler current and hold it to a minimum. The result is a longer-lasting SSR with constant performance over time.

• Like use of the finest, in-house manufactured semiconductors from the world's technology-in-volume producer. Nobody can beat that kind of QC.

• Like extended design goals with design performance verified by Mil-type testing. Quality and care in manufacture mean a better product from us now and a better one for you down the road.

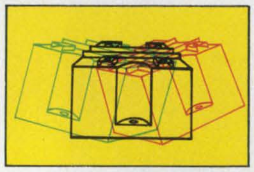
• Like complete, void-free, vibration-resistant potting that's withstood millions of hours of under-the-hood environments.

For Power Designs



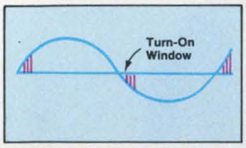
Positive control over temperature

We guarantee the control points of the output switch over the full spec'd temp range. You can count on it from 3-32 V over a −40° to +80°C range. And the highest voltage doesn't shorten life of the optical isolator. Our design goal is reliable operation for 10 years.



Shock & vibration-resistance

Completely potted units have shown ability to withstand MIL-spec type testing for accelerated impact, vibration, salt spray, thermal cycling life, etc. We make 'em rugged for rugged environments.

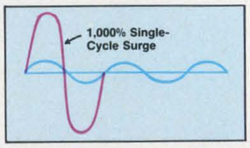


Zero voltage switching

Closures can occur only near the zero-crossing point of line voltage, minimizing noise generation which could interfere with other electronics. The electrical environment therefore remains clean.

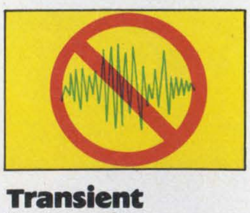
Reverse polarity protection

Additional features like reverse polarity protection obviate damage from error in installation and subsequent equipment malfunction.



High peak surge ratings

1000% single cycle surge ratings protect against current abuse. Conservatively-rated components and thermal design contribute to longer service life.



Transient immunity

Motorola SSR components are 100% overrated for high voltage conditions. Each is internally protected against high line, random noise, spikes and conditions typically found in harsh industrial environments.

solid-state relays!

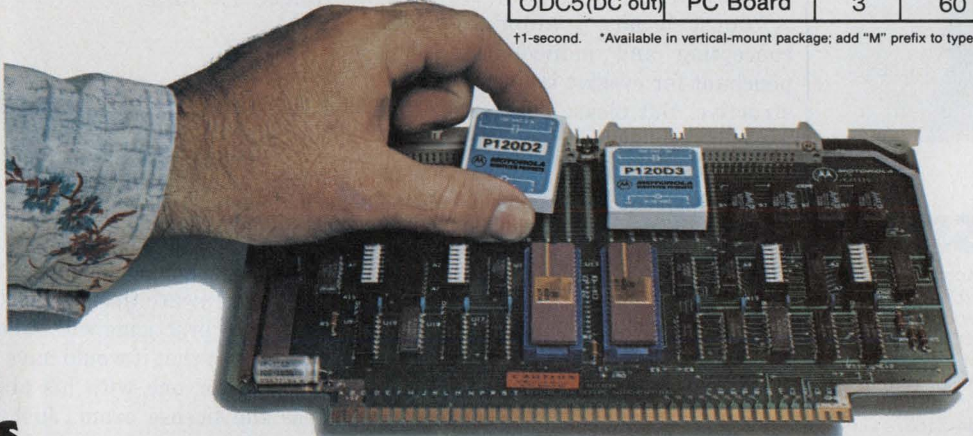
• Like compatibility with microprocessors, integrated circuits and other solid-state relay control circuits.
• Like standardized packaging and footprints available from multiple industry sources.
• Like technical field assistance from our nationwide applications engineers and reps and stocking from authorized distributors.

That's why our relays and modules are so good. And that's why they'll last a long time.

For more information on any of these new Motorola solid-state units, contact Motorola Subsystem Products, P.O. Box 20912, Phoenix, AZ 85036 (602) 244-3103. Viva Motorola Solid-State Relays!

Switch	Type Mounting	Output Current A	Line Voltage V	Peak Surge# A
M120D05A	Chassis	5	120	50
M120D10A	Chassis	10	120	100
M240D05A	Chassis	5	240	50
M240D10A	Chassis	10	240	100
P120D2*	PC Board	2	120	20
P120D3*	PC Board	3	120	55
P240D2*	PC Board	2	240	20
P240D3*	PC Board	3	240	55
IAC5 (AC in)	PC Board	—	95-130	—
IDC5 (DC in)	PC Board	—	10-32	—
OAC5 (AC out)	PC Board	3	12-140	55
ODC5 (DC out)	PC Board	3	60	5†

†1-second. *Available in vertical-mount package; add "M" prefix to type number. #Single-Cycle.

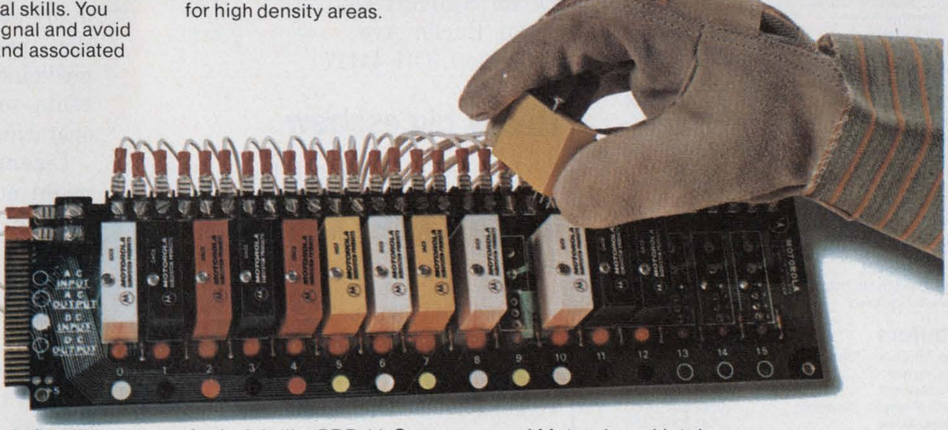


For PC Boards

Fit-anywhere, go-anywhere horizontal- or vertical-mounted convenience and economy are yours with the P/MP-series 2 & 3A, 120 & 240 V relays.

Measuring only ⅜" thick, P-series offers the lowest profile solid-state unit of its kind for card rack mounting on ½" centers. No wire terminations. No mechanical skills. You treat system loads like any other electrical signal and avoid connector-wire, board-mounting problems and associated labor costs.

1,500 V photo isolation, zero-voltage turn on, built-in snubber network, 100% testing at rated load, I/C compatibility and a −40° to +100°C operating range are standard. The family's also available in a compact, vertical-mounted MP-series package for high density areas.



For I/O Systems

In a costly electronic control system, it's easy to invest two-thirds to three-fourths of total cost in just interface and wiring. We've now solved that and given you the convenience and versatility to revolutionize your I/O control system.

Because each Motorola I/O module contains signal conditioning, isolation, logic interface, power handling and status indication drive in one compact, compatible package that interfaces with all 5 V logic families and standard MPU I/O requirements. At a *fraction* of the cost of other systems.

The color-codable board's standard, too... with or without the modules. You can interface the entire system with standard minis like PDP-11, Supernova and Motorola and Intel micros... install them in standard NEMA enclosures... and remove or replace modules without disturbing field wiring. The package is rapidly becoming the industry standard, too... and that makes it comfortable.

Motorola I/O Modules. Easy. Quick. Reliable.

MOTOROLA INC.

CIRCLE NUMBER 15

Across the desk

(continued from page 16)

I have built two computers at home. The second one was a 16-bit version of the PDP-8. I have gotten our company into microprocessor control of our high-power transmitters.

So when I hear a mature engineer with many years of experience sing the blues about how technology is passing him by and how there ought to be a law or club to protect him, I understand why. He's ossifying and no longer needed by society.

Homer A. Ray Jr.
1406 San Rafael
Dallas, TX 75218

Concepting clear ideas

Your February 1 editorial on idea concepting and individuals with a penchant for evasive language was instructive. But please also realize that loose in the world are a number of advanced-concepts people who really do work at the frontiers of advanced technology, and who can succinctly express their notions in brief, unconfusing language (not always English).

Your point was well taken, and I'll bear your admonition in mind. In the future when I need to be confusing and evasive I'll use a different title—like Editor-in-Chief.

Ernie Guerri
Director
Advanced Concepts
Gould Inc.
Ocean Systems Div.
18901 Euclid Ave.
Cleveland, OH 44117

Really big eschew

Great editorial in the Feb. 1 issue. Eschew obfuscation? I would, George; but obfuses get caught between my teeth.

Jim Rose
Communications Management Co.
20944 Sherman Way
Suite 108
Canoga Park, CA 91303

More noise

"Predict Noise in Digital Systems" in ED No. 5, March 1, 1978, p. 64, contained a printing error on p. 66 in Fig. 3, Location 042-045 of the SR-52 program: The entry under "Keys" should read 02+ RCL, not 02 − RCL. Otherwise the article was very good.

The program can be used also on a TI-59 calculator by coding directly from the "Keys" column and making the following conversions

SR-52	TI-59
HLT	R/S
*rset	RST
*if flg 1 143	*if flg 1 116
*if flg 2 168	*if flg 2 135
*if flg 3 202	*if flg 3 161

On the TI-59, the program takes 173 keystrokes.

James Spackman
Project Engineer
Texas Instruments Inc.
P.O. Box 5621
Dallas, TX 75222

Licensing and the public

So they finally got Irwin Landes ("Protecting the Members," Jan. 18) after 25 years or so. Maybe he had that coming. As an Honors graduate of Harvard Law School, he certainly must have been aware that he was breaking the law by practicing without a license, and I doubt that it would have been too difficult for one with his abilities to pass the license exam. Just too lazy probably—or, perhaps, he considered himself above ordinary people who must conform to the law. Something of the same nature may be said for Mr. D'Adamo, who probably helped a good many people with his efforts. The law that prevents him from practicing medicine without a license also prevents some back-alley butcher from operating on 10 or 20 people per day.

Licensing electronics engineers might not be a bad idea. Even though it might result in "union-like" advantages for some, one cannot avoid the fact that more and more electronics engineering will be classified as entering the public domain. Therefore, it seems sensible to license engineers to protect the public, just as doctors and lawyers are licensed. No capable person would be barred from working in his chosen field, since he would have the opportunity to pass the license exam. Even the independent inventor wouldn't be affected since he could still patent his inventions and have them

(continued on page 30)

One dynamic reason to buy Mostek's 4K static.

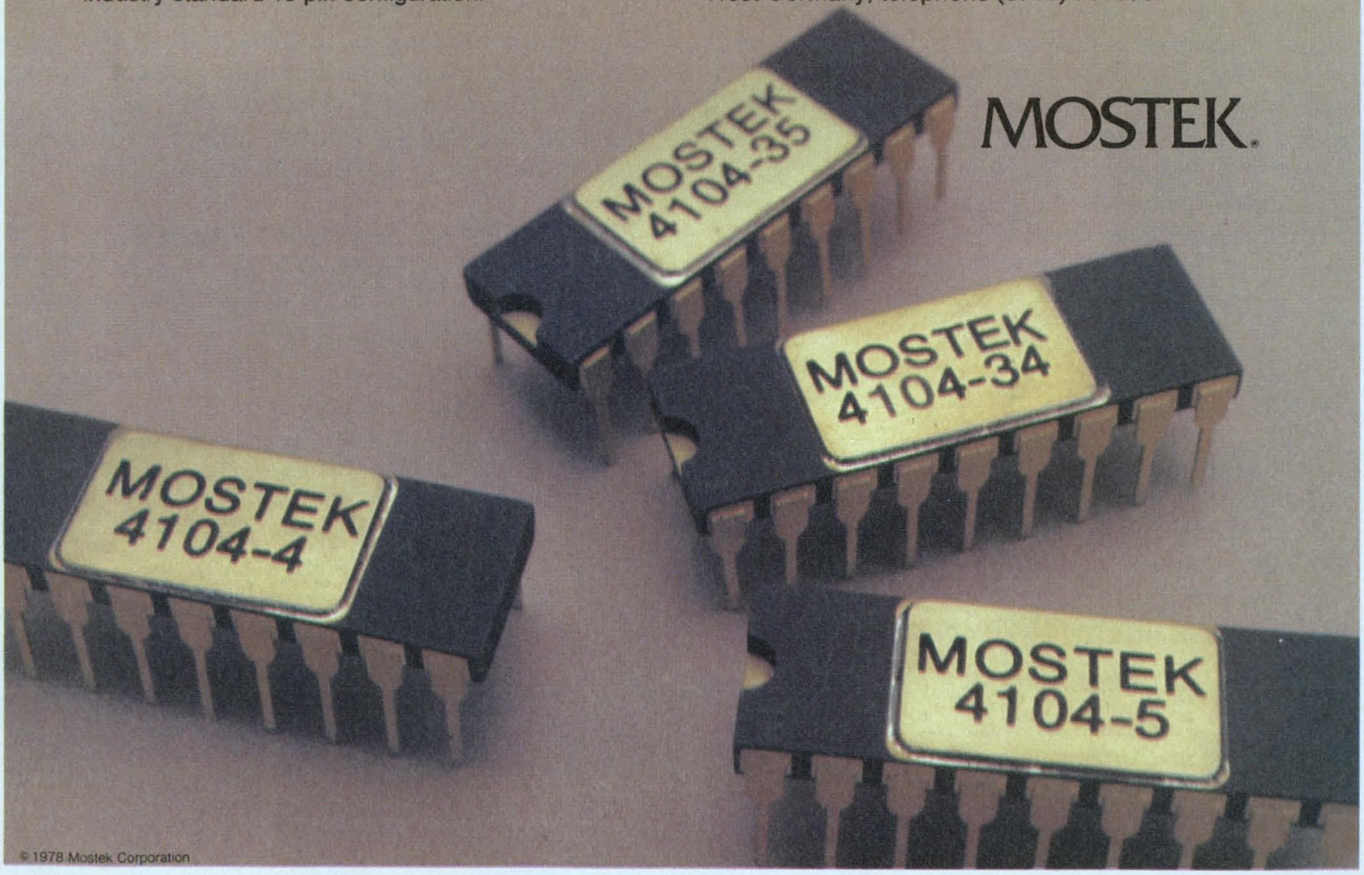
Delivery.

Delivery's fast and that's good news, but there are more dynamic reasons to buy the Mostek 4104 4K X 1 static RAM. For one, it offers the industry's best speed/power product. Using our own widely-copied Edge-Activated™ design concept, Mostek engineers developed the 4104 offering the best features of static and dynamic RAMs. Power is extremely low— just 150mW active and 28mW standby. It's directly compatible with TTL. It operates on a single +5 Volt power supply with a tolerance of ±10%. And you can get it in the industry-standard 18-pin configuration.

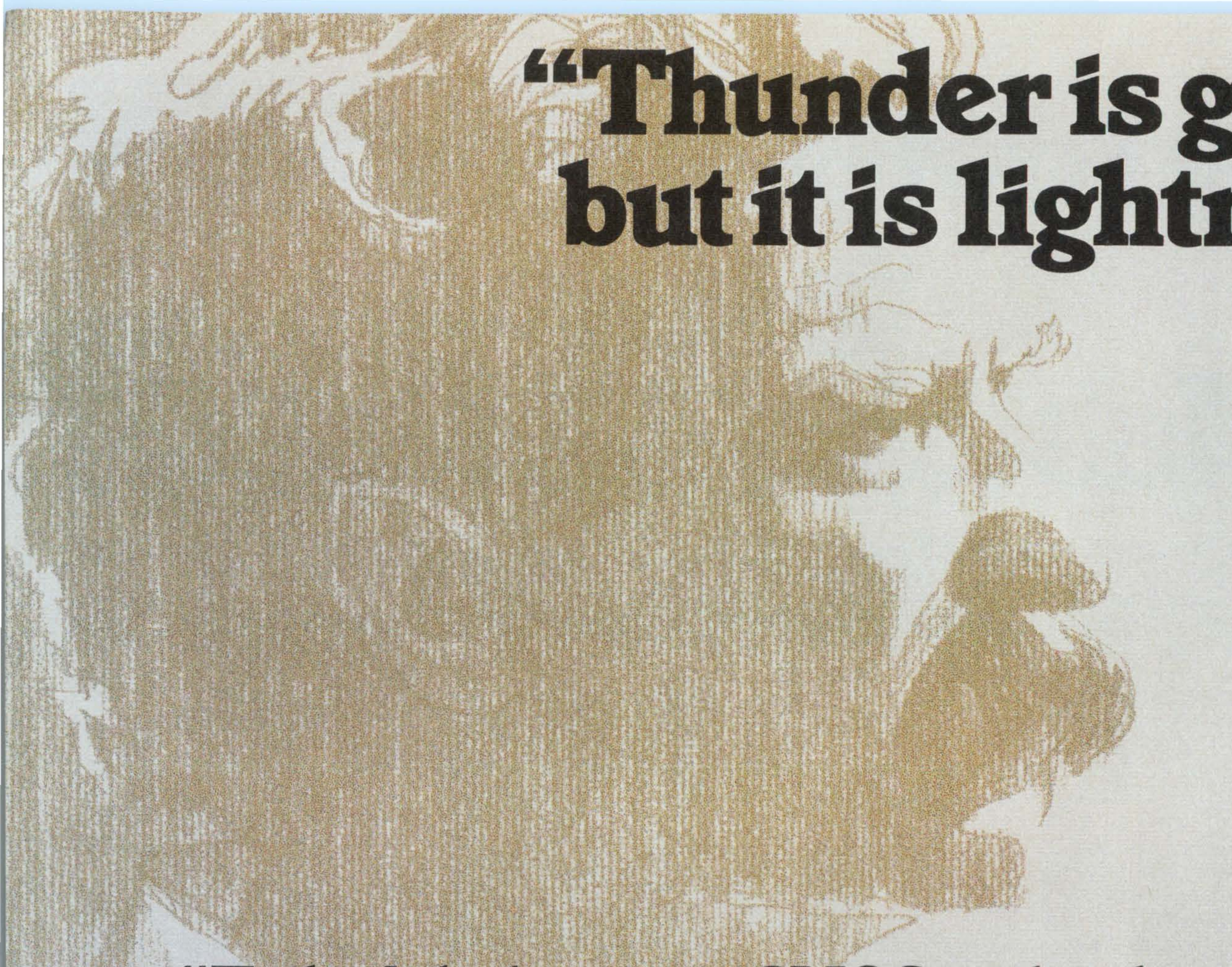
	ACCESS TIME	CYCLE TIME	ACTIVE POWER (MAX)	STANDBY POWER (MAX)	BATTERY BACKUP POWER (-3X Series)
MK4104-4/-34	250ns	385ns			
MK4104-5/-35	300ns	460ns	150mW	28mW	10mW
MK4104-6	350ns	535ns			

The new 4104-3X series offers the capability of retaining data in a reduced power mode. When Vcc is lowered to 3V, maximum power dissipation is only 10mW. This allows complete data retention during battery operation.

There's a lot of dynamic reasons for Mostek's 4104 static RAM. To get the complete story, call a Mostek distributor or sales representative now. Or contact Mostek at 1215 W. Crosby Road, Carrollton, Texas 75006; telephone (214) 242-0444. In Europe, contact Mostek GmbH, West Germany; telephone (0711) 701096.



CIRCLE NUMBER 16



"Thunder is good, but it is lightning

"Today's lightning is CMOS technology."

You probably think of CMOS technology in terms of low power applications. You ought to think of it in terms of system performance. High speed. Higher noise immunity. Better drive capability... even analog and digital on a single chip. And of course, CMOS lower chip temperatures and, therefore, greater VLSI chip density. That adds up to system performance and reliability. At a competitive price.

TOMORROW'S TECHNOLOGY TODAY.

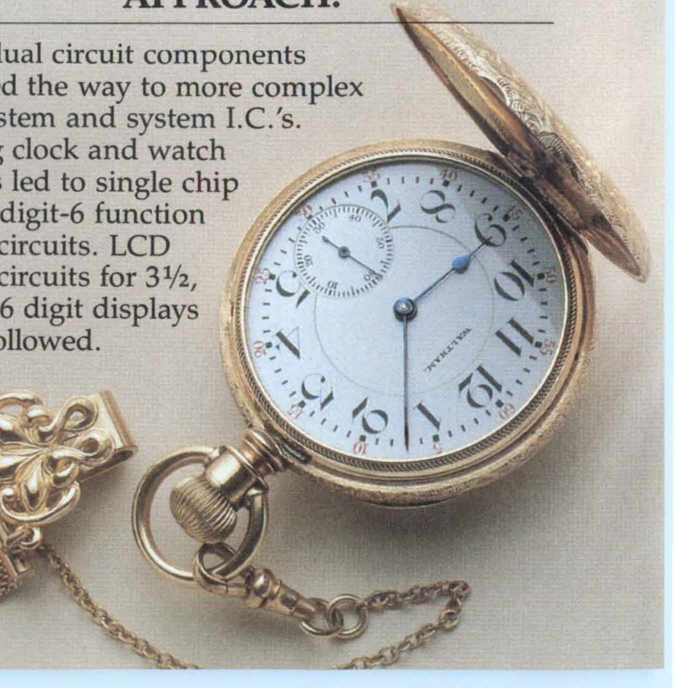
Intersil is the source. One chip system and subsystem circuits. Frequency counters. Up-down counters/timers. LED and LCD display drivers. 3 1/2 digit and 16 bit data converters. Touchtone® encoders. Ultra-high reliability circuits for heart pacers. Dedicated controllers. And more.

CMOS THINKING.

We've used each phase of CMOS development to boot-strap the next. Each new circuit grows from a tried and proven success. For instance, our original low power watch and clock circuits were the basis for exceptionally low current drain frequency oscillators. Static and dynamic divider concepts allowed us to push the technology to 10MHz for direct scaling. Output transistors now allow direct driving of LED displays and synchronous or stepper motors. And most recently, digital and analog circuits have been married on a single chip.

THE BUILDING BLOCK APPROACH.

Individual circuit components have led the way to more complex sub-system and system I.C.'s. Analog clock and watch circuits led to single chip LED 4 digit-6 function watch circuits. LCD watch circuits for 3½, 4, and 6 digit displays soon followed.



Across the desk

(continued from page 26)

approved for public use by a licensed engineer.

Howard D. Peck
Research and Development Engineer

GTE Sylvania
Johnston St.
Seneca Falls, NY 13148

Right on target

Beautiful, George! Your editorial, "Protecting the Members" (Jan. 18) says it all on professional and occupational licensing laws. Your previous efforts on this subject were good, but open to misunderstanding. For instance, many readers thought you were boosting laetrile itself, rather than the freedom to choose it on an open market—hence the laetrile controversy that still rages in your letters column.

Now, however, you've gone right to the key issue: the right of the individual to offer his services to anyone who finds them useful enough to pay for them. The only way anyone can misunderstand this time is to take your ironic statements literally.

I have a dream: Thousands of engineers, led by your magazine, mount a campaign to repeal every licensing law that enriches others at our expense. When I wake up, though, I realize that if engineers ever did mobilize to that extent, it would probably be to pass a licensing law of their own.

I must admit one thing: The pro-licensing engineers are refreshingly honest about why they want licensing—to protect their jobs and salaries. There is practically none of the blather about "protecting the public" that we routinely get from the other special interests.

Steve Klein

Ocean Technology, Inc.
2835 N. Naomi St.
Burbank, CA 91504

Who's we?

I do not wish to enter the laetrile controversy, but I would like to ask Nathaniel Cunningwell, whose letter appeared in the January 18 issue, who the "we" is in "We found it necessary to make bureaus."

My own observation is that "we" have had nothing to say about the formation of the numerous government bureaus, and even less to say about their activities—or about "deglitching" them.

If Mr. Cunningwell believes that reducing everyone to the same level is progress, then he certainly must be happy. Instead of some people being screwed by a few organizations, everyone is being screwed by one supercorporation, wrongly called "government."

Perhaps Mr. Cunningwell would be willing to tell us how to deglitch the bureaucracies before the present ratio of one bureaucrat to five workers becomes five to one.

W. F. Cox

The Comark Co.
P.O. Box 2086
2310 Fourth St.
Santa Rosa, CA 95405

Government protection doesn't solve anything

Your January 18 editorial, "Protecting the Members," is another good one. I cannot understand why everyone wants the government to solve all our problems when it is obvious that all government has done is make existing problems worse while creating new ones. Licensing electronics engineers will produce the same type of results.

D. J. Morroni

Electric Equipment and
Engineering Co.
40 W. 49th Ave.
P.O. Box 16383
Denver, CO 80216

It's good—and ours

The circuit in "Try a Wien-bridge Network" by Glenn Darilek and Oren Tranbarger (ED No. 3, Feb. 1, 1978, p. 80) is indeed an excellent circuit. We thought so much of it when we developed it that we obtained a patent on it, No. 3,838,351, dated Sept. 24, 1974, and filed on July 13, 1973. This circuit has been—and is—used in some equipment we manufacture.

Dr. Norris C. Hekimian
President

Hekimian Laboratories, Inc.
15825 Shady Grove Rd.
Rockville, MD 20850

New Books

Angle Modulation, The Theory of System Assessment—J.H. Roberts, Peter Peregrinus, Ltd., Southgate House, Stevenage, Herts, SG1 1HQ, England, 278 p. $27.50.

CIRCLE NO. 440

Logic Designer's Manual—J.D. Lenk, Prentice-Hall, Englewood Cliffs, NJ 07632, 504 p. $18.95.

CIRCLE NO. 441

Rotating Electric Machinery and Transformer Technology—D.V. Richardson, Reston Publishing Co., Reston, VA 22090, 615 p.

CIRCLE NO. 442

The Directory of Defense Electronic Products and Services, U.S. suppliers 1978—Information Clearing House, 500 Fifth Ave., New York, NY 10036, 173 p. $20.

CIRCLE NO. 443

Directory of Electronic Circuits with a Glossary of Terms—M. Mandl, Prentice-Hall, Englewood Cliffs, NJ 07632, 321 p. $16.95

CIRCLE NO. 444

Microwave Homodyne Systems—R.J. King, Peter Peregrinus Ltd., England, distributed by ISBS Inc., P.O. Box 555, Forest Grove, OR 97116, 368 p.

CIRCLE NO. 445

An Introduction to Microcomputers, Volume O The Beginner's Book—Adam Osborne & Associates, P.O. Box 2036, Berkeley, CA 94702, 221 p.

CIRCLE NO. 446

Nonlinear Systems Analysis—M. Vidyasagar, Prentice-Hall, Englewood Cliffs, NJ 07632, 302 p. $21.95.

CIRCLE NO. 447

Switching and Linear Power Supply, Power Converter Design—A.I. Pressman, Hayden Book Co., 50 Essex St., Rochelle Park, NJ 07662, 384 p. $19.95.

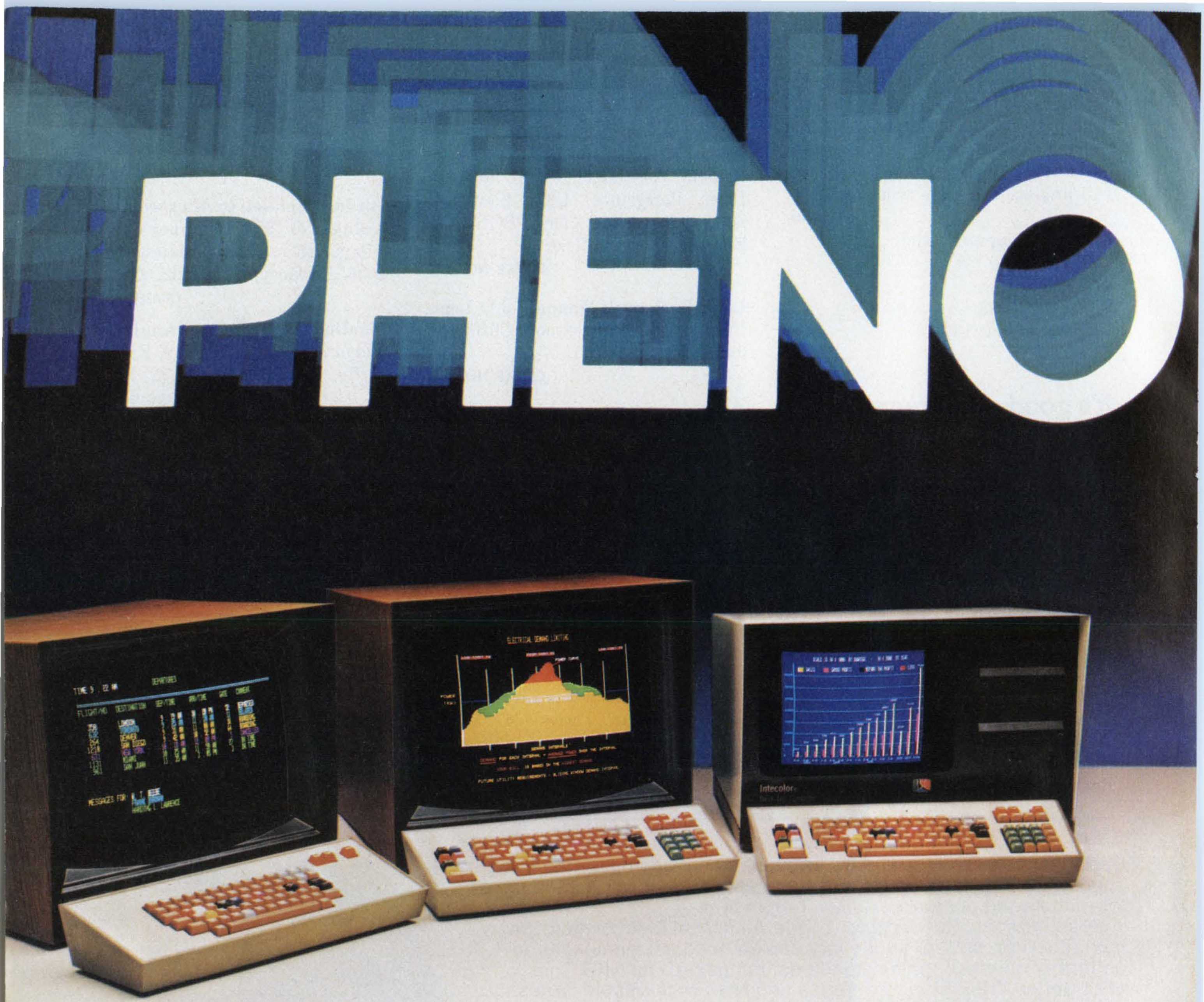
CIRCLE NO. 448

A Step by Step Introduction to 8080 Microprocessor Systems—D.L. Cohen and J.L. Melsa, Dilithium Press, P.O. Box 92, Forest Grove, OR 97116, 169 p.

CIRCLE NO. 449

Microprocessor Interfacing Techniques—A. Lesea and R. Zaks, Sybex, Inc., 2161 Shattuck Ave., Berkeley, CA 94704, 348 p.

CIRCLE NO. 450



Intecolor 8001 Color Data Terminal—$995*

Color Graphics 8001G—$1,925*

Intecolor 8032 Microcomputer System—$3,495* with dual built-in mini disk drive (Display of ISC financial data shows how you can present yours in graphic form.)

For a relatively young company we've got a phenomenal success story.

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*Prices for the 8001 and 8001G are based on orders of one evaluation unit, cash-with-order, guaranteed 30-day delivery or your money back. Prices for the 8032, 8051 and 8070 are 100 unit prices, net 20 days.

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Unretouched photographs of screens

Intecolor 8051 Microcomputer System with mini-disk drive—$3,150* (Shown with special ARABIC/FARSI configuration. Optionally available at extra cost.)

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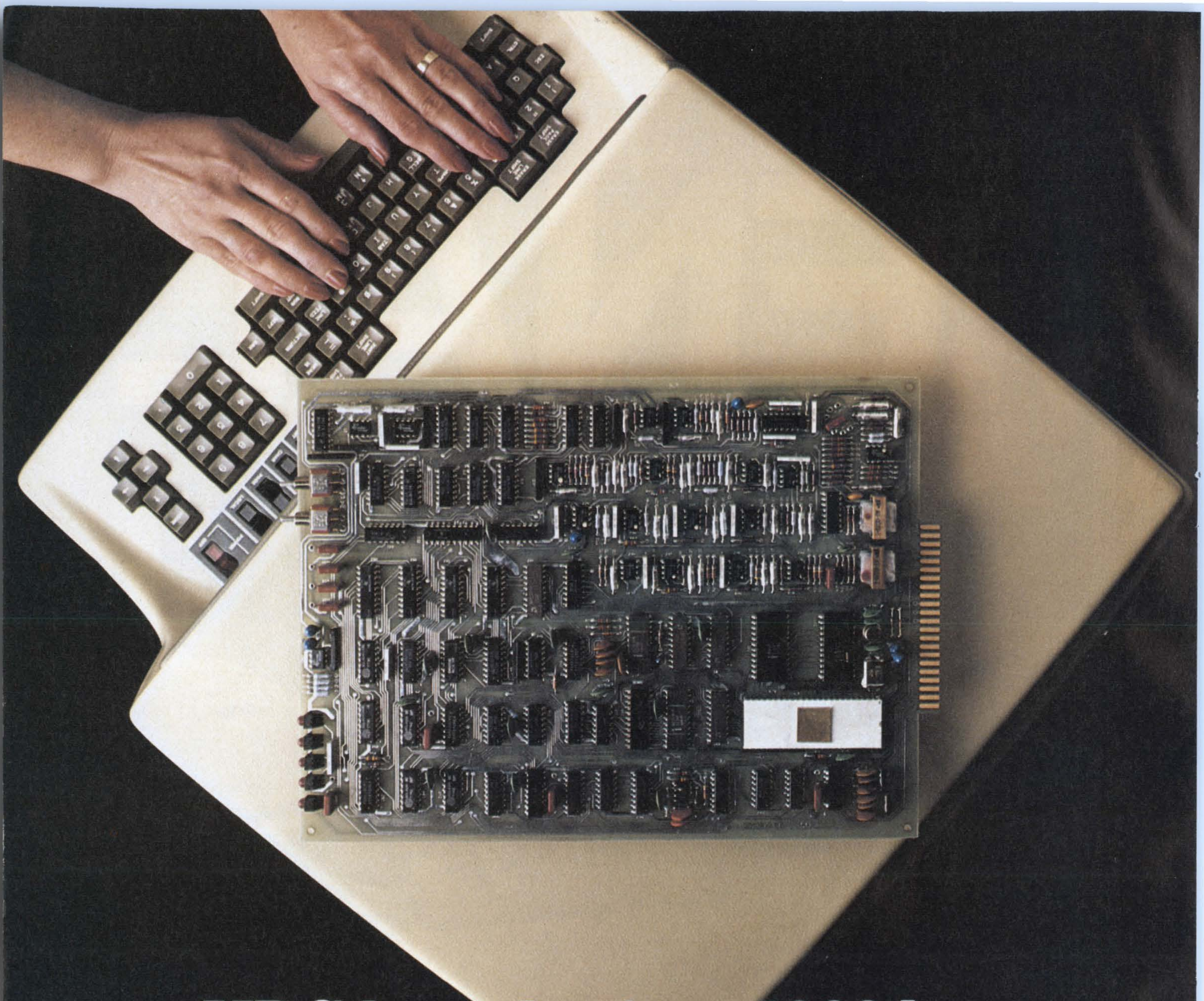
CIRCLE NUMBER 18



UDS has the first 4800 bps Bell-compatible OEM modem- <100 square inches

UDS has leapfrogged current LSI technology with nanosecond microprocessor performance! All components are industry standards — no custom or single source parts are used.

- **First chance to build-in.** Radically reduced space requirement (including .5″ maximum component height) and low power consumption ease design constraints.
- **Design flexibility.** Most parameter changes require firmware alterations only. Physical layout can be adapted to your specifications.
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UDS announces a 4800 bps Bell-compatible microprocessor modem.

UDS has leapfrogged current LSI technology with nanosecond microprocessor performance! All components are industry standards — no custom or single-source parts are used.

- **Bell compatibility.** Available in 208A (four-wire) and 208B (two-wire) configurations, one-third Bell's size.
- **Reliability.** A drastic reduction in total number of components results in a longer MTBF.
- **Multi-channel opportunity.** A 7" x 19" rack-mountable enclosure accommodates up to eight single-channel cards.
- **Cost/effectiveness.** Microprocessor power and innovative design make the UDS 208 your best buy for data communications at 4800 bps.

For further details, contact us at Universal Data Systems, 4900 Bradford Dr., Huntsville, AL 35805. Phone 205/837-8100; TWX 810-726-2100.

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Created by Hall & McKenzie, Inc., Winter Park, Florida

CIRCLE NUMBER 20

Alpha particles may be cause of soft errors in memory

As semiconductor memory chips have increased in density, more and more soft errors have been cropping up. For example, a ONE suddenly changes to a ZERO for no reason. If unchecked, such soft errors, prevalent in very dense 16-k RAMs, could really proliferate in 64-k devices, and ultimately limit the density of semiconductor dynamic RAMs.

But the cause may have been discovered—alpha particles—as well as a solution, at the IEEE's Reliability Physics Symposium in San Diego.

Timothy May and Murray Woods, device specialists at Intel Corp. (Santa Clara, CA), have found alpha particles —helium nuclei—emanating from the small amounts of uranium or thorium in a semiconductor package. Penetrating the semiconductor material, the particles form hole-electron pairs that drift to lightly charged diffusion areas and fill them up.

As memory structures have shrunk, so have the charge densities; thus, the effects of the alpha particles have become more harmful.

Glass used in semiconductor packages, because of their zirconia and quartz-filler materials, can contain between two and 30 parts per million of uranium and thorium, according to May and Woods. Typical epoxies show as much as 1.5 ppm, and alumina typically between 0.1 and 1 ppm.

But there are ways to minimize the particle effects, says Thomas Kline, a memory-device specialist at National Semiconductor, Santa Clara, CA:

- Increase the relative charge densities in the storage cells.
- Shield the die from the packaging materials.
- Encourage the systems designer to include error correction provisions in his designs.

While all scaled-down versions of 16-k RAMs would suffer, Kline feels that the National parts may be less vunerable than most to the alpha particles. They have been designed and have an extra p-n junction, which tends to increase the charge density in the storage areas. With the storage cells spread further apart, an alpha particle will be less likely to strike a charge area. And the extra p-n junction helps increase the stored charge densities, which reduces the harmful effects of the extra charges induced by the alpha particles.

Powerful minicomputer thinks it's a mainframe

Big computers, beware. Here comes a minicomputer that has more computing power than an IBM 370/138—the System/400 from National Semiconductor. Not only does the system offer better performance than the 370/138, it can also run IBM's DOS/VS and VM/370 software packages, which are the most widely used IBM operating systems. These packages provide access to more system and applications software than all minicomputer operating systems combined. And the IBM software can run on the System/400 without any modifications.

The arsenal of the System/400, from the Santa Clara-based firm, includes two processors: a bipolar-bit slice based 32-bit processor for normal instruction execution, and a single-board microcomputer for what the Santa Clara-based company calls a service processor. This processor performs the microprogram loading, system console control and permits remote diagnostics.

Built from the high-speed 2901A-1 bit-slice processor fabricated by National, the System/400 is structured around a 32-bit synchronous central logic bus that is capable of up to 20 Mbytes/s. The basic System/400 configuration also includes a CRT-based system console, 256 kbytes of dynamic memory, a 200-Mbyte disc drive, a printer and diskette drive. All this comes for \$165,000—about half that of the IBM 370/138.

The Super-mini is expandable, too. Memory can grow to 16 Mbytes (built from 16-k dynamic RAMs) and I/O processors can increase from two to 12. Each I/O processor is microprogrammable and can execute the various channel programs that handle 3330-Type discs, tape drives and other peripherals. Line printers, disc drives, tape drives, card reader/punches and other peripherals can be added as needed.

A prototype of the System/400 will be shown at the NCC show, to be held in Anaheim, CA, June 6, 7 and 8. Production units will not be available until the first quarter of 1979.

First CCD tester handles every semi memory

The first memory tester designed for charge-coupled devices reportedly can test and characterize every type of CCD on the market or known to be in development.

Not only can the 5580-9 general-purpose memory tester handle CCDs of any length and loop, it can test all RAMs and ROMs up to 65-k × 10 bits.

Introduced this week at the Semicon show in San Mateo, CA, by Fairchild's Xincom Div. (Chatsworth, CA), the 5580-9 includes a special enhanced timing module (ETM) that generates CCD drive signals.

The key to testing and characterizing CCDs is to use a large number of different timing sets as stimuli, says Xincom's Jim Mulady. "These are combinations of clock and data streams with differing phase relationships. As you feed clocks and data to the serial CCD memory, you must switch from one phase relationship to another in real time."

The 5580-9 holds information specifying 12 such combinations in its RAM memory, and the ETM generates the signals and does the real-time switching.

Priced around \$120,000, the new tester is already in production.

CIRCLE NO. 316

Fast 1-k RAM's access time cut in half

Advances in ECL process technology are slashing the access time of 1-kbit RAMs from 20 ns to 10 ns. The 10-ns access time of the Fairchild 256 × 4 RAM, the 10422, is guaranteed, says Bill Carrico, marketing manager for

LSI memories at Fairchild's Mountain View, CA, facility.

The 10422, to be introduced in the fall, will be the second memory chip made with Fairchild's Isoplanar II process. The first, a 256 × 1 RAM designated the 10414/100414, also has fast access times—10 ns maximum and 7 ns typical.

The greater speed stems more from shallow elements than from reduced mask area, according to Carrico. Starting with the same cell size and mask layout used with Isoplanar I, Isoplanar II produces 5-GHz transistors, whereas the older Isoplanar I walled-emitter process can produce only 1-GHz transistors.

Like the previously fastest 1-k, the 1-k × 1 10415A (with access times of 20 ns maximum, 12 ns typical), the 10422 will be a fully-decoded random access memory chip, with on-chip voltage compensation. Designed for cache, scratchpad, and writable-control-store uses, the 22-pin, 5-V device will be compatible with all 10-k and 100-k ECL logic families.

Connector joins PCs—without pins or sockets

No more pins and no more sockets—not, at least, with a Conmet stacking connector. To interconnect PC boards or couple baby boards to motherboards, merely interpose the connector between the boards and provide a means to securely fasten the two together.

The novel, simple connecting approach, manufactured by Tecknit (Cranford, NJ), consists of a plastic holder with the connecting element, a rubber-like strip, inserted into it. This element, a strip of silicone rubber 0.030 in. thick, contains one or two layers (or rows) of parallel copper-alloy wires with a diameter of 0.003 to 0.005 in. Each wire, surrounded by silicone rubber, is thoroughly insulated from every other wire, but the wire ends are slightly exposed. And the wire ends contact terminal pads on the mating boards.

Pinless and socketless, the Conmet stacking connector provides high contact density, as close as 0.025 in., and low resistance, less than 25 mΩ.

Not only is the initial contact resistance low, but the connector automatically forms an environmental seal for its contacting wire ends to maintain this low resistance. And, of course, the silicone-enclosed connecting wires are fully protected against corrosion.

Three standard Conmet connecting-element strips are identified by a color code: red, for 0.025-to-0.05 in. PC-board contact spacing; green, for 0.05-to-0.1-in. spacing; and blue, for 0.1 to 0.02 in. The red and green elements contain double layers of wires, the blue, a single layer.

Connector costs range from $2.61 to $4.78 each in quantities of 10 to 24.

CIRCLE NO. 317

Scientific calculator fits your wallet

CMOS chips and field-effect liquid-crystal displays combine to cut the power dissipation of two new scientific calculators enough that their batteries needn't be changed more often than once a year. And the units are small enough to fit comfortably inside a wallet or pocket.

For example, the "Minicard" FX-48 from Casio Inc. (Fairfield, NJ), the U.S. marketing arm of Japan's Casio Computer Co. Ltd., is about the size of a credit card and about 1/8 in. thick, and weighs only 1.6 ounces. It performs 32 scientific functions, including factorials, logs, summations, and trigonometric calculations, in addition to the four basic math functions. It operates for up to 1000 hours—a year's normal use—and is priced at $39.95.

The slightly larger Casio FX-8000 adds stopwatch, timer, and clock features to its 42 scientific functions. For $49.95, the FX-8000 measures to hundredths of a second, and has a multistep timer that allows five intervals to be programmed so that a beeper goes off at five preset intervals. Housed in its own notebook case, the FX-8000 runs for 2000 hours between battery changes. That's still a year's average use because the timer functions are used more often.

News Briefs

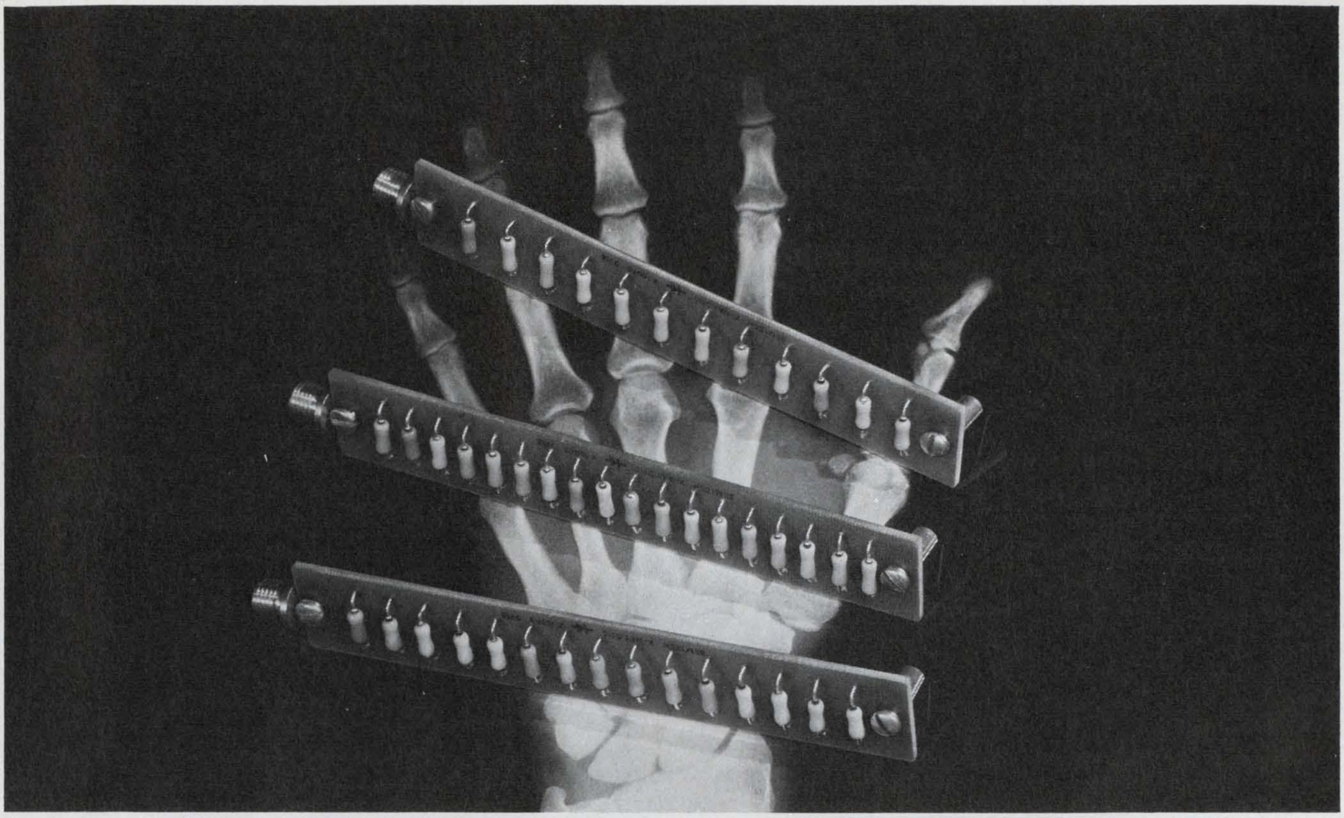
A new class of static RAMs is coming—byte-wide (8-bit output) static RAMs in both MOS and bipolar forms.

Mostek (Carrollton, TX) and SEMI (Phoenix, AZ) have 1-k by 8 MOS devices. While SEMI's has an access time of 200 to 300 ns, Mostek says it can select devices with access times down to 90 ns. Meanwhile, Signetics Corp. (Sunnyvale, CA) is planning a series of byte-wide bipolar RAMs. The company already has a 64 × 9-bit unit, where the extra bit is used for error correction. Coming are 256 × 8 and 256 × 9 devices with latches that ease direct connections to microprocessors. They also have the same devices without latches. Access time is in the 45 to 60-ns range. Look for the devices within the next few months.

The largest byte-wide RAM in the industry, a 4-k × 8 (32 kbits) MOS RAM will be available from Zilog (Cupertino, CA) for year-end sampling. Actually a pseudostatic RAM, the device has internal refresh circuitry that makes the refresh operation transparent to the user. Typical access time is 250 ns, and cycle time typically 500 ns. Signetics also is developing a byte-wide PROM, a 4-k × 8 unit, using an advanced bipolar Schottky process with under 100-ns access time. This device will lead to a 64-k bipolar PROM. Samples are expected by the end of the year.

The lowest-power precision operational amplifier chip is coming from Precision Monolithics (Santa Clara, CA). Operating from a single power supply (3 to 30 V) with supply current of 45 μA maximum, it has excellent offset voltage, 200 μV, and a common-mode rejection of 110 dB. Tradeoff is in speed—slew rate is 0.04 V per μs.

A family of 8048-type devices built in CMOS is in the works at Intersil (Santa Clara, CA). The first chip will be the C-8748, which is pin-compatible with the Intel 8748 NMOS devices. This chip includes an 8-k EPROM and 64 bytes of RAM. It is expected in the fourth quarter. The chip, incidentally, may be the industry's largest chip in standard production—it will measure 290 mils square. An 8049 and an 8741 will follow. Intersil is also planning CMOS memories with a 512 × 8 EPROM and is developing a 2-k × 8 clocked ROM, an 8-k × 8 clocked ROM, and 1-k × 4-k × 1 static RAMs.



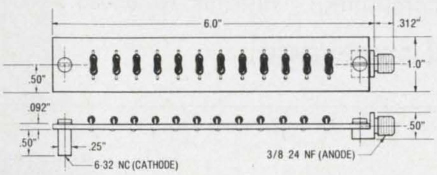
"X-WAY STIC"

High Quality - Low Cost Rectifiers for X-ray Power Supplies.

Semtech Corporation introduces "X-WAY STIC" a new series of open rectifier sticks specifically designed for X-ray power supplies.

Each X-WAY STIC utilizes hermetically sealed Metoxilite multi-chip "avalanche" rectifiers mounted on a PCB. These Metoxilite multi-chip rectifiers (technology initially developed for high reliability aerospace programs), are now available *at reduced prices.*

In addition to X-ray power supplies, these rectifiers can be effectively used in most standard, single and polyphase circuits. Designed for use in oil environment.



Types: X100KS, X125KS & X150KS

PIV (operating): 100, 125 & 150kV

PRV (test): 125, 150 & 175kV

Average Rectified Current @ 55°C Oil: 150mA

Reverse Current @ PRV: 1.0μA

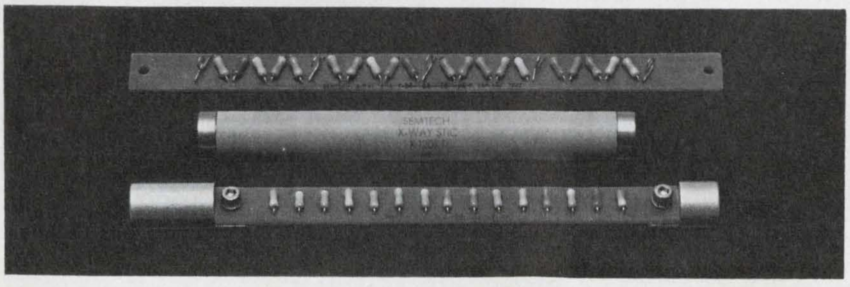
Recurrent Surge (10 cycles @ 60 Hz rate): 7.5A

Single Cycle Surge @ 8.3ms: 25A

Forward Voltage @ 50mA: 160, 190 & 220V

RELIABILITY COSTS LESS!

OTHER X-WAY STIC TYPES AVAILABLE:



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CIRCLE NUMBER 21

Systems on Silicon.

The embodiment of this systems-on-silicon concept is our fully compatible M6800 Family.

With 1.0, 1.5 and 2.0 MHz speed options of the MC6800 microprocessor at the center of the multi-chip approach, all necessary I/O, memory, and peripheral family functions complete the system. Later this year, introduction of the MC6809 advances multi-chip systems to a new performance dimension, and provides the bridge from 8-bit to 16-bit applications.

Reducing the basic seven parts of the multi-chip system to two, with little or no sacrifice in processing power or design flexibility, is the mission of our MC6802-6846 combination. It's the low-cost way to get more of the system on less of the silicon.

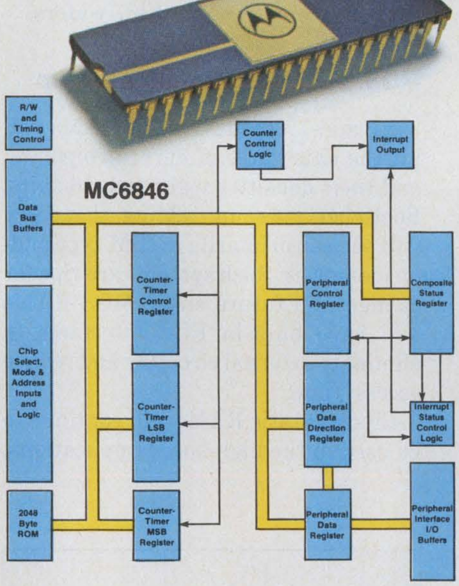
That idea followed to its conclusion arrives at the single-chip microcomputer. The third generation MC6801 will put an entire minimum system onto one chip of silicon, yet enhances MC6800 performance. The MC6805 single-chip microcontroller will complement the '6801 for low-end, low-cost applications.

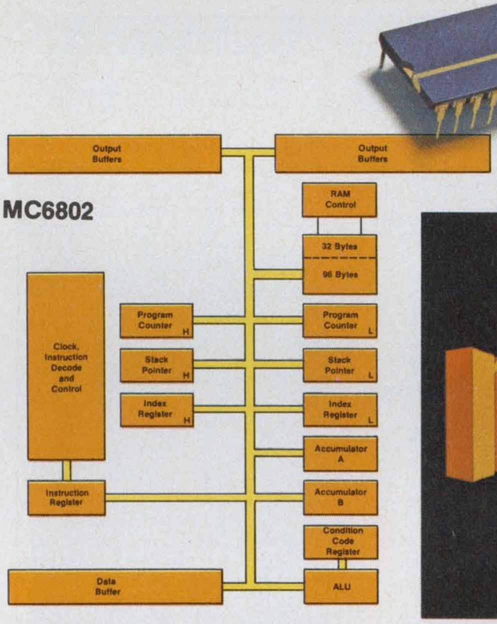
Every one of Motorola's microprocessor-microcomputer products uses the EXORciser* and/or its compatible system development tools for system development. All M6800 software, including FORTRAN, COBOL, BASIC, and MPL high-level languages, is fully compatible.

No one puts systems on silicon like Motorola. Motorola: first in compatibility, technological diversity, training, and commitment.

*Trademark of Motorola Inc.

Build systems with the MC6802 & MC6846...and save.





The pair is priced under $15.00 in 10K quantities, and there's no extra cost for software or system development tools since all M6800 Family processors are totally compatible. They are available in quantity, now.

Together, these two chips supply all the power of the MC6800 MPU, plus 128 bytes of scratchpad RAM, 2,048 bytes of ROM program storage, and on-chip clock circuitry. Ten parallel I/O lines for controlling system peripherals and equipment, and a 16-bit programmable timer with three control lines for synchronous control of external circuits also are provided.

M6800 Family functions like the Asynchronous Communications Interface Adapter, MODEMs, Peripheral Controllers, and General Purpose Interface Adapter work with the '6802 just like it was a '6800. Indeed, they can't tell that it isn't a '6800. External multiplexed interfacing or buffering is never required between the MC6802 and any peripherals or memory.

In addition to the standard MC6800 features of the MC6802, it has a couple of unique advantages. The first 32 bytes of RAM can be held in a low-power mode during power down situations, permitting retention of critical data when power is lost.

For enhancement of MC6802 system cost-effectiveness, you can replace the normal 1-MHz crystal with a 4-MHz crystal.

This low-cost, two-chip system is a winner. So you can familiarize yourself with it, Motorola authorized distributors are offering, for a limited time, a special information package with the MC6802 and MC6846, all for the price of the units, themselves.

MOTOROLA INC.

CIRCLE NUMBER 22

NCC: Memories are growing fast, and so is Japanese semi industry

Static MOS random-access-memory will have 16-kbit capacities by mid-1980, and will be as fast as today's bipolar static RAMs.

Dynamic MOS RAMs with 64-kbit capacities, now being sampled, will be readily available by 1980.

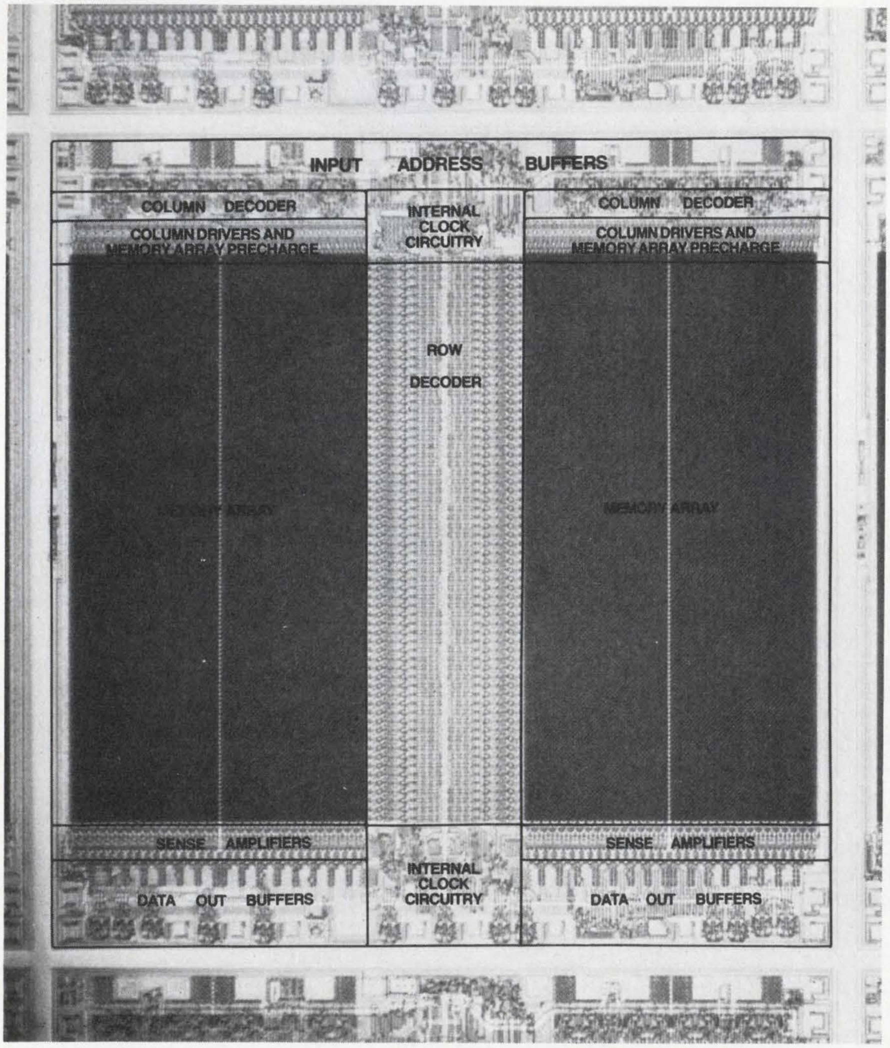
Magnetic-bubble and charge-coupled-device memory chips will have 1-Mbit capacities by 1980, but they will probably not be competing with one another for use in the same applications.

Standards, which are desperately needed in constructing and even in describing memory chips and microprocessors, are being worked on in earnest.

Stephen E. Scrupski
Senior Editor

These predictions and conclusions will come out of the technical sessions at next month's National Computer Conference in Anaheim, CA. Not only that, but a worldwide perspective will be added by a team of Japanese engineers reporting on advances in Japanese semiconductor technology.

The main production part for the next two years should be 16-k MOS dynamic RAMs, predicts Charles Boettcher of National Semiconductor (Santa Clara, CA). After that, 64-k RAMs will be available, built with about 4-micron geometries on 4-in. wafers.

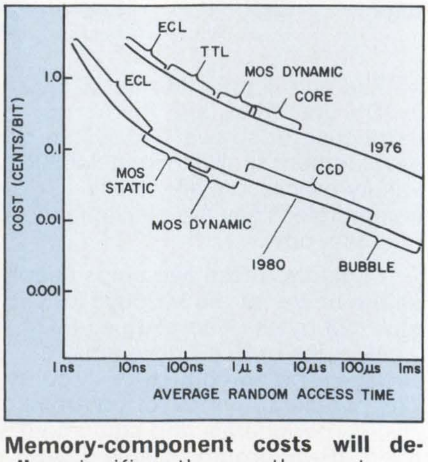


High-density ROMs are now being produced, such as this 64-kbit unit from Mostek, which requires only 200-mW active power and 25-mW standby.

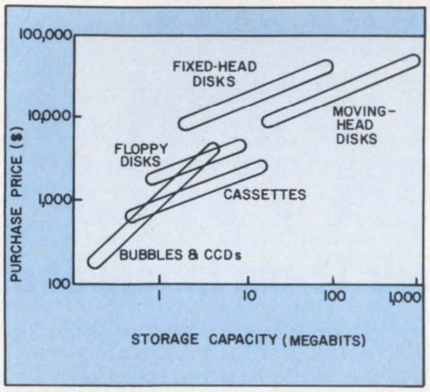
MOS static RAMs catching up

By mid-1980, MOS static RAMs will hit the data rates of current bipolars, and their densities will reach 16 kbits, Boettcher goes on, adding that they will be used primarily in IBM-type add-on memories. Such systems are ripe for changes, so future static MOS RAMs will have built-in ECL interfaces to eliminate external circuitry and reduce access time.

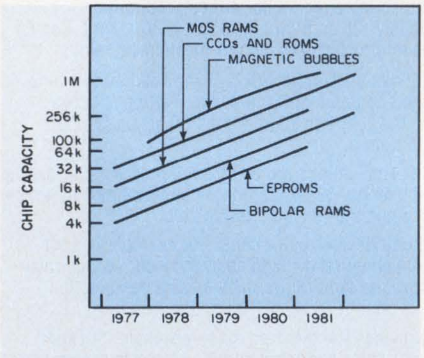
Bipolar static RAMs will continue to be used in the high-speed applications,



Memory-component costs will decline significantly over the next couple of years, and hit the levels shown here. Note the potentially low costs of CCDs and bubbles.



Mass-storage costs in today's market cover three orders of magnitude, with magnetic bubbles and CCDs going for the lowest costs. Prices shown include interface circuits.



Densities will keep increasing in solid-state memories. Today's 16-k MOS RAMs will soon be replaced by 64-k devices, with 256-k RAMs likely by 1980, according to TI's Juliessen.

says Boettcher. Built in ECL form, 128-bit RAMs will have access times of less than 5 ns, while 4-kbit ECL chips will offer access times less than 25-ns.

The lowest cost per bit of all semiconductor-memory technologies will continue to be offered by charge-coupled devices—about one-third to one-fourth the cost per bit of other types. However, Boettcher warns, there's little to be expected in CCD access-time improvements because of the basic serial-memory scheme.

Boettcher bases all his predictions on four basic factors that determine practical device densities: storage-cell complexity, feature size, wafer size, and defect density. Taken together, these four factors have increased batch density about 120 times.

The most significant changes, he says, have been in the decrease in storage cell complexity. Expressing cell area in units of f^2, where f is the minimum feature size allowed by pattern-definition technology, Boettcher states that cell sizes in the past eight years have decreased from 200 f^2 to the range of 16 f^2 to 20 f^2. But he doesn't stop there. It's theoretically possible, he says, to reach 4 f^2, which means simply two features in both the x and y directions—one to store information and the other to isolate it from adjacent cells. Not only that, but if other means can be found to isolate adjacent cells in less than a feature size, even f^2 is possible.

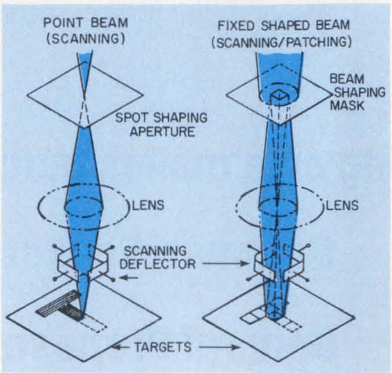
Another big help to improving RAM capacities is increased wafer size. Four-inch wafers give four times more wafer area than conventional 2-in. wafers.

Two less significant factors are improved feature size and decreased defect density, which haven't contributed as much to increasing the number of good bits per batch. For that matter, says Boettcher, electron-beam exposure systems are five to eight years away from practical use in direct wafer

Electron-beam lithography advances in Japan

Optical lithography methods used to produce LSI devices will eventually be replaced by electron-beam lithography. The best possible resolution with light is about 1 micron. But electron beams (or X rays), with their much shorter wavelengths, can reduce this to less than 0.1 micron, and greatly increase LSI density.

Japanese contributions to electron-beam lithography will be revealed by a team of engineers from the University of Tokyo and the Institute of Physical and Chemical Research in Wakoshi. The latest figures, over a target area 7 × 7 mm, are a 0.1-μm resolution with a 1-μA beam whose size varies from 0.1 μm to 2.5 μm. With 1-μA beam current, a 2-in. wafer can be scanned in 20 seconds.



As with the raster scan used in television, an electron point beam is deflected electrically and scanned across a target area (see sketch). A fixed-shaped beam (also shown) is typically a square about 2.5 by 2.5 μm. A variable-shaped beam may also be formed in a similar manner by using two overlapping masks. Spot scanning uses simpler electron optics, but the variable-shaped beam offers higher exposure speeds.

Actually, there are three basic exposure methods: electron-beam, optical and X-ray (see table). And there are several ways to generate patterns, including contact-masking, image projection and direct pattern generation.

All three exposure methods can be used for contact-masking. But contact-masking is the least desirable, since mask life is limited by its being in contact with the target silicon area.

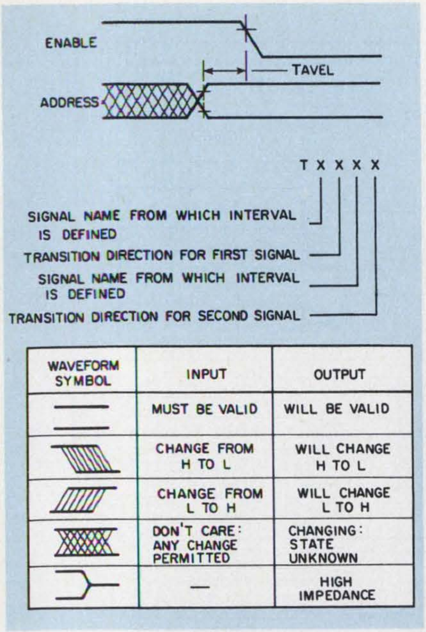
With an image-projection scheme, the mask need not be in contact with the target, but then the need for a lens makes it hard to project images with X rays.

Patterns can be generated directly only with electron beams, which can be scanned across the target, so a mask isn't needed. Instead, the features of the circuit to be formed are programmed into the scanning-system controls.

Scanned electron beams have been used as an intermediate stage to produce masks to be used in contact masking with conventional optical lithography.

	Contact mask	Mask projection	Direct pattern generation	Ulitmate resolution
Optical	√	√	X	≥ 1 μm
X-Ray	√	X	X	≤ 0.1 μm
Electron beam	√	√	√	≤ 0.1 μm

√ — Practical X — Impractical



Memory standards being developed by an IEEE committee include definitions of abbreviations for timing parameters as well as graphic representations of waveforms.

Table 1. Features of the DSA MOS masterslice chip

Number of Circuits	800 internal gate cells 116 output gate cells	
Power Supplies	V_{ee} 5V single power supply	
Propagation Delay	basic cell (minimum interconnection) basic cell (average interconnection of ALU)	1.0 ns at 3.6 mW 3.0 ns at 3.6 mW
Output buffer	TTL-compatible t_r=7 ns at 1 TTL load t_r=5 ns at 1 TTL load	
Total power Dissipation	internal gate cells output buffer circuits	2.5 W 0.5 W
Chip size	7.68 x 7.88 mm^2	
Number of pins	maximum 120 pins	

Table 2. Properties of W²L bipolar circuits

	T²L	W²L	I²L
Delay time ns/gate	3-30	3-30	10-100
Power consumption mW/gate	2-20	1-10	0.01-1
Threshold voltage V	1.4	0.7-1.4	0.7
Power supply V	5	1.6-5	0.8-5
Load drive	good	good	poor
Masks	6	6	4
Transistor mode	normal	normal	inverse
Active area ratio /gate /ALU	1 1	0.4 0.3	0.1 0.2

manufacture of devices.

Nevertheless, batch density will continue to improve. Boettcher foresees about a 100-times increase over the next eight years, but cautions that this will require large investments in both capital equipment and design talent. At the same time, fewer manufacturers will be able to afford such investments. And meanwhile, the market for memory products will have to continue expanding at a rate to make such investments pay off.

Meanwhile, a 256-k bubble chip can be expected in a year, and a 256-kbit CCD a year later, predicts J. Egil Juliussen of Texas Instruments in Dallas. By 1980, he says, look for a 1-Mbit bubble-chip. A 1-Mbit CCD chip will follow in 1981.

Watch out magnetic discs

Bubbles and CCDs will steadily encroach on magnetic-disc applications, and by 1980 or 1981, one bubble or CCD chip will store more than today's minifloppy disc. The single-unit OEM price of a minifloppy, about $350, may decrease $100 over the next couple of years. However, Juliussen points out, such a price decrease will be no match for the progressively lower prices inherent in bubble and CCD manufacturing technologies.

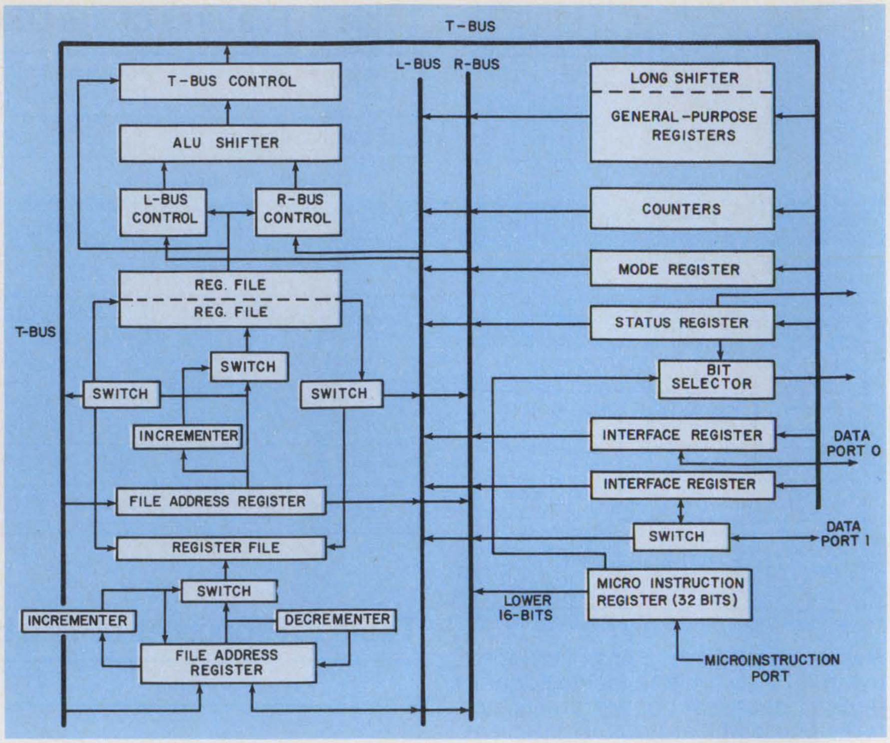
"Magnetic bubbles and CCDs will have little direct application competition," Juliussen goes on. Bubbles will fit better in small systems, whereas CCDs, with their inherently higher performance, are more likely to turn up in large computers, as fillers of the memory heirarchy gap. And the nonvolatility of bubbles and the availability of support circuits suit them to mass storage for microprocessor-based systems.

Bubbles cannot match CCDs for access times. Juliussen reports that 64-k CCD chips from TI and Fairchild have average access times of 410 μs and can transfer data at 1 to 5 Mbits per second. Intel's 64-kbit takes 130-μs because it has more shift registers. But the Intel chip's transfer rate is about half that of the other chips.

Bubbles don't even come close. TI's 92-kbit bubble chip has a 4-ms access time and can transfer data at only 50 kilobits per second. But bubble chips do have many available support chips, which enhance their usefulness to μP-based systems.

"The bottom line is price," states Juliussen. CCDs will probably stay ahead of bubbles over the next few years, he says, because of the manufacturing experience gained with MOS and because there are currently three manufacturers producing CCD chips. However, bubble chips require fewer manufacturing steps. And, as more manufacturers crop up, bubbles should close the price gap. In fact, says Juliussen, bubbles "have an excellent chance of gaining an advantage over CCDs."

Right now, three products are using TI's 92-k bubble chip. The TI 763/765 portable keyboard-printer terminals, part of the company's Silent 700 series, use at least 20 kbytes of bubble memory and can be expanded to 80 kbytes. A microcomputer system with 80



This universal computing element, called Pulce, uses three 16-bit buses to interconnect various specialized registers. Developed in Japan, it's built in an n-channel MOS-on-sapphire substrate, and holds about 20,000 transistors.

kbytes of bubble memory has been introduced by Q1 Corp., while Data Systems has a floppy-disc replacement unit that is compatible with DEC's PDP-8 and PDP-11 systems and uses between 86 and 519 kbytes of bubble memory.

In the past year, both Intel and National Semiconductor have mounted efforts to supply bubble-memory chips. Juliussen also notes that AT & T is field-testing its 13A announcement system, which plays back prerecorded messages, and uses 68-kbit bubble chips developed at Bell Labs and manufactured by Western Electric.

Currently, three systems use Intel's 16-k CCD chips: Intel's own OEM memory board, Technical Analysis Corp.'s replacement for a fixed-head disc unit for use with its Nova-based small business computer, and Alpha Data's fixed-head-disc replacement unit, which is compatible with its other fixed-head-disc units.

Slowing down for standards

In general, then, memories are moving fast. Still, memories have settled down to the point where it's now sensible to consider at least standardizing the way their parameters are specified.

A new IEEE subcommittee is now studying proposed standards for preparing memory-chip data sheets, for test patterns and for thermal resistance. The data-sheet standard will cover such aspects as symbology and presentation of data, says committee member J. Reese Brown, Jr. of Burroughs Corp. (Piscataway, NJ). Timing specifications, in particular, have exhibited the largest differences among the vendors. Brown, a leading authority on semiconductor memories, notes that the timing specs of current MOS dynamic memories are extremely complex, typically covering seven different signals or groups of signals—each having up to four critical timing events. Moreover, each event must be specified with respect to at least one other signal and often with respect to three or four others.

As a result, a scheme is being introduced for describing time intervals with abbreviations. The initial character, T, is followed by four descriptives that specify two signal points, and the name and the transition direction for the signals. For example, the symbol TAVEL would describe the address set-up time as the time between address-valid and enable-low time.

As for test patterns, Brown notes that the committee originally tried to base its recommendations on one of the more widely understood programming languages, such as APL or Basic. But the language used has now evolved into one that tends to be closer to the language of some actual testers, and is undergoing further refinements.

Thermal-resistance standards are still being studied and will be ready for presentation to the subcommittee by late 1978.

Memory devices are being studied by a second JEDEC committee, Brown adds. Committee JC-42, though made up solely of representatives of device manufacturers, is working closely with Brown's committee.

Microprocessors are also coming in for standards work. A microprocessor standards committee has been formed by the IEEE Computer Society, report Tom Pittman of Itty Bitty Computers (San Jose, CA) and Robert G. Stewart of Stewart Research Enterprises (Los Altos, CA). In particular, they note that work is needed on standardizing microcomputer bus structures and controls.

Right now, there are at least three widely used bus systems: the MITS S-100, the Intel MDS bus, and the National Semiconductor Microbus. The S-100 has been widely used since its introduction in the Altair 8800 computer, but it still has problems, such as the use of positive true rather than negative true. It also uses too many bus-control signals, according to Pittman and Stewart, and it assigns separate buses for data inputs and data outputs.

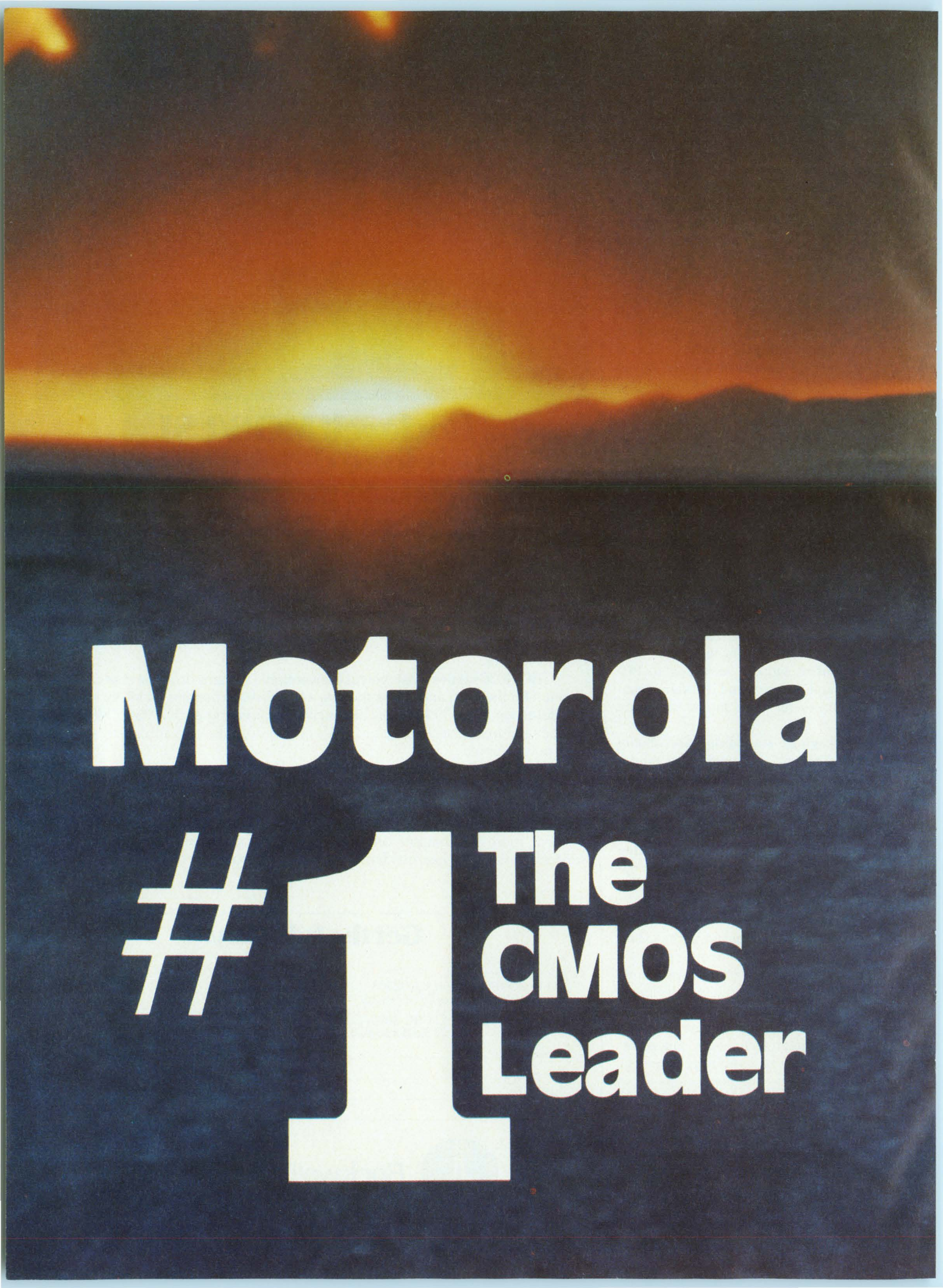
Packaging standards are badly needed as well. Although most microprocessors come in 40-pin packages, Pittman and Stewart observe that the locations of such basic terminals as ground and power supply aren't fixed. Such variations are, of course, related to the chip designers' problems in optimizing chip operation by minimizing conductor trace lengths.

Meanwhile, Japanese semiconductor technology has advanced to the extent that a special Japanese contingent will present several papers on topics ranging from new semiconductor devices to remote processing. The primary focus, however, will be on Japanese computer semiconductor technology and recent developments in computing elements.

Several new memory chips from Japanese producers will be cited by Takuo Sugano of the University of Tokyo:

- A low-power, 4-k static bipolar RAM with 25-ns access time and 350-mW dissipation from Hitachi.
- A 4-k bipolar static RAM with 40-

(continued on page 50)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Leader

Motorola announces 12 UB types to complement the #1 CMOS B-Series

Nine gates, two buffers, and an array are now available from Motorola in conformance with the JEDEC CMOS B-Series standard for UB devices. The six major gates (see table) are now available both ways, as B or UB. That's buffered or unbuffered. Although construction of these devices differs, pinouts are the same.

The UB listings are included with all the recent updating in our new revision of the CMOS Pocket/Wall Selector Guide, just off the press. And, when we talk about reliability, we back it up. The details are now compiled for 1977 and spelled out in our new report on CMOS IC Reliability, 1978.

Copies of both these new pieces, plus new UB data sheets are yours for the asking. Send your letter or the coupon from this ad to Motorola Semiconductor Group, P.O. Box 20912, Phoenix, AZ 85036. Please specify which items you want.

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Responding to demand, Motorola shipped industry record quantities of CMOS units in 1976 and 1977 from our ultra-modern, high-capacity facilities. In doing so, we earned that big number 1.

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Motorola UB CMOS

Part No. MC1xxxx	Function	UB Data Sheet Available	B-Series Available
4000UB	Gate		
4001UB	Gate	✓	✓
4002UB	Gate	✓	✓
4007UB	Array	✓	
4011UB	Gate	✓	✓
4012UB	Gate	✓	✓
4023UB	Gate	✓	✓
4025UB	Gate	✓	✓
4049UB	Buffer	✓	
4069UB	Buffer	✓	
4501UB	Gate		
4572UB	Gate		

TO: CMOS
Motorola Semiconductor Group
P.O. Box 20912, Phoenix, AZ 85036

Please send me:

☐ CMOS Pocket/Wall Selector Guide, Spring, 1978
☐ CMOS IC Reliability, 1978
☐ UB Data Sheets

Name ____________ Title ____________

Company ____________ Dept. ____________

Address ____________ Phone ____________

City ________ State ________ Zip ________

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(continued from page 47)

ns access time and 500-mW dissipation from NEC.

- A 64-k MOS RAM with 200-ns access and 150-mW dissipation on a 6.1 × 5.8-mm chip from the Electrical Communication Laboratories of the National Telegraph and Telephone Public Corp. The silicon-gate device uses 2-μm pattern widths.
- A CMOS 4-k static RAM with 5-μm geometries with an access time of 200 ns, operational power dissipation of 50 mW, and standby power of 0.5 μW. This Toshiba device is 4.7 mm square.
- A 2-k electrically alterable ROM from Toshiba with 20-μs writing time for a single cell and less than 5 s for a fully decoded 2048-bit memory. Erasure is with ultraviolet light or by electric injection of electrons from a floating gate.
- A 16-k erasable ROM from NEC with 300-ns access time and 450-mW power consumption on a 3.6 × 4.90-mm chip.

High-speed logic devices are also being turned out with new structures, Sugano goes on.

A master-slice type MOS LSI being worked on by Mitsubishi uses a diffusion self-aligned (DSA) process. The latest chip is a 920-gate array (see Table 1). The chip, which measures 7.68 × 7.88 mm, is TTL-compatible and uses a single 5-V supply. Propagation delay per cell is 1 ns at 3.6 mW dissipation.

Meanwhile, a new logic configuration called wired-OR, wired-AND logic (W^2L) has been developed by OKI. The performance level falls roughly between TTL and I^2L (see Table 2). With such a configuration, a circuit has much better load-driving ability and is faster than I^2L, but also dissipates more power per gate and requires more mask steps.

An elevating improvement

Another new structure, this one for bipolar-transistors, is called an elevated electrode integrated circuit (E^2IC). Circuit speed goes up because the transistors don't enter the saturation region. Delay time per gate is about 85 ps and the delay-time-power product is about 0.075 picojoules. Such devices, produced by NTT's Electrical Communication Labs, have also been built into an 8-bit arithmetic logic unit with 180 gates on a 1.6 × 1.0-mm chip.

A new type of 16-bit single-chip universal computing element called Pulce

Table 3. Pulce characteristics

Device type	n MOS/SOS
Chip size	8.85 x 6.66mm
Gates in a chip	7000
Transistors in a chip	20000
Package	80-pin flat package with cooling fins.
Power supply	5V
Machine cycle	200ns
Power dissipation	1.5W
Operating temperature	0°C-50°C
Data width	16 bits 32 bits
Registers	44
(General purpose)	29
(Mask)	7
(Dedicated)	(16 bits) 6 (4 bits) 2
Shifter	
(Single word)	0-15 bits
(2,3,4 words)	1 bit
Decimal operation	add/sub (1 digit)
Stack	Hardware support

will be described by Toshiba and the Electrotechnical Laboratory of the Agency of Industrial Science and Technology. The chip is built as n-channel MOS on sapphire with 4-μm design rules. This silicon-on-sapphire technique produces a speed that is about 1.6 times the speed produced with a bulk-silicon substrate. The chip, measuring 8.85 × 6.66 mm, has 7000 logic gates using about 20,000 transistors. It's housed in an 80-pin package to avoid multiplexing, which would slow down operation.

The basic architecture uses three 16-bit internal buses and 16 registers directly accessible from the buses. Microinstruction-cycle time is 200 ns with a single-phase clock. The delay through a lookahead-carry path of 10 gates for a 16-bit arithmetic operation is 35 ns while the binary addition time, including decoder delay, is between 80 ns and 115 ns.

The Pulce is microprogrammed with 32-bit words to give the user flexible control over its operations. The I/O operations, however, are externally controlled rather than by microinstructions. Input-output communications are handled through two registers with bidirectional buffers.

The 80-pin package comes equipped with five aluminum cooling fins. And when operating at rated speed, Pulce chip dissipates 1.5 W.

VLSI in Japan

Meanwhile, on a "larger" scale, Japanese computer makers are investing heavily in a joint project sponsored by the country's Ministry of International Trade and Industry. The goal is to develop process techniques for submicron pattern geometries required for very-large-scale-integration devices. Electron-beam and X-ray techniques, as well as improved optical-lithography equipment are being developed (see box on p. 44).

The current LSI devices in Japanese computers are no slouch, either, according to Osamu Ishii of the Electro Technical Laboratory. In the ACOS series computers produced by NEC and Toshiba, a typical logic chip uses current-mode logic with 200 gates per chip and 7 picojoules per gate. Up to 110 such chips are housed in a 240-pin ceramic package measuring 80 mm by 80 mm and 12 of these packages can be held on a 15-layer printed-circuit-board. All told, that means as many as 40,000 gates per board. The ACOS series computers generally span the same performance range as the IBM System/370 computers.

One special requirement facing Japanese computer systems is the need to handle a mixture of Kanji (ideographic) and Kana (phonetic) characters. While there are only 48 phonetic characters, there can be as many as 10,000 different ideographic characters. As a result, character generators and printers are quite complex, and a large amount of memory is required.

For example, with a 4000-Kanji-character set, memory capacity for a 24-by-24-dot-matrix representation would require as many as two-million bits. With the LSI advances, decreasing memory costs may one day solve this problem, says Ishii. Further, the input typewriter is very complex—it uses several shift keys. This reduces typical input speed to about 45 characters per minute—a far cry from a conventional alphabet-input speed of about 50 words per minute, or about 250 characters per minute. ■■

Designing μP software in 'modules' speeds development, ups reliability

Not only will microprocessor programs be more flexible, they will be written more quickly and easily if formed from functional program modules. In addition, these modules should help cut the high cost of μP software.

The latest microprocessor-development systems are making it easier to write programs in modular style. For example, with module-oriented "structured programming," the Intellec Series II development system from Intel (Santa Clara, CA) can work in PL/M, Fortran and assembly language, and can link program segments written in any of those languages into a single, final program.

"One could write critical time-dependent functions in assembler, special math functions in Fortran, and other code elements in PL/M," according to Intel's Joseph Harakal, software product manager in the Microcomputer Division. "After compilation, they can be linked to form the application-load modules," Harakal went on, speaking at the Mini/Micro Computer Conference in Philadelphia.

Andy Santoni
Associate Editor

With structured programming, a complex microprocessor program is broken down into simpler blocks of program code, just as a complex circuit design is broken down into simple segments on a block diagram. The program segments can be used again in other projects, and they can be altered without changing other parts of the program.

Structured programming would be a big help to a system that may have to be expanded—for example, a process controller built around a single-board computer, notes Harakal. After the analog and digital needs of the unit have been identified and programmed, the system may have to be expanded to include a hard-copy terminal for alarm and control-function changes. Then, after the product goes to market, a competitor may introduce a similar product, so a decision may be made to add an inventory package.

If the process-control unit's original software were in modular form, Harakal suggests new software could be added without rewriting the entire system.

Software is expensive

But the eventual aim of structured programming is to reduce the cost of

Typical Development Systems

Development system	Chip support	Real-time in circuit emulation	Symbolic de-bugging	Text editor	Assembler	Basic	Fortran	PL/M	Other languages	Relocation and linkage: Full	Relocation and linkage: Load time
Data General	Micro NOVA	N	N	Y	Y	Y	Y	N	N	Y	Y
DEC	LSI-11	N	N	Y	Y	Y	Y	N	Focal	Y	Y
Fairchild Formulator	F8	Y	Y	Y	Y	N	N	N	N	Y	Y
Intel Intellec Series II	8021, 8041, 8048, 8049, 8080, 8085, 3000	Y	Y	Y	Y	N	Y	Y	N	Y	N
Mostek AID-80F	Z-80	Y	N	Y	Y	N	N	N	N	N	Y
Motorola Exorciser	6800	Y	N	Y	Y	Y	Y	N	N	Y	Y
Mupro-80ED	8080	Y	N	Y	BSAL 80/85	N	N	N	N	N	Y
Tektronix 8002	8080, 6800 Z-80	Y	N	Y	Y	N	N	N	N	N	N
TI 990/10	9900	Y	Y	Y	Y	Y	Y	N	Cobol	Y	Y
Zilog MCZ-1	Z-80	Y	N	Y	Y	Y	Y	PL/Z	Cobol	Y	N

Microprocessor software is easier to write with development systems like these. The choice is wide and getting wider, but Joseph Harakal of Intel Corp. (Santa Clara, CA) could list only a few of the systems available, and not all their features. He warns: "One should consult current vendor data sheets and manuals for details."

software, which is holding back the application of microprocessors.

Improvements are needed

"Clearly, radical improvement is required in the effectiveness of software if full advantage is to be taken of the benefits offered by the microcomputer," says Andrew A. Allison, a consultant from Los Altos Hills, CA. Unfortunately, however, while semiconductor technology has been quick to make low-cost computers available, software-development techniques haven't kept up.

With the rapid fall in the cost of microcomputer hardware, Allison goes on, μP development systems can be built more flexibly and at lower prices, which helps cut software costs. But the cost of software still has not kept pace with the cost of hardware.

There are complete microcomputer systems available for $500 to $5000 that can handle many applications by themselves, Allison points out. But for something like a small-business application, where a program might have between 5000 and 10,000 steps, each step would have to be designed, written, tested, and documented for $5 to $7. The software cost is much higher than the hardware cost.

Microprocessors are unique

While mini and mainframe computers suffer from many of the same problems, there are some difficulties that μPs can call their own, says Burt Masnick, senior technical specialist at Hazeltine Corp. (Greenlawn, NY).

Frequently, for example, the microprocessor programmer must understand the external activity and signal levels that occur as instructions are executed. Unfortunately, says Masnick, "while instruction manuals usually describe the logical effect of the instruction set in detail, they are occasionally obscure or vague on important details."

Write, edit, and debug a microprocessor program, then transfer it to PROM, with a development system like this one, from Tektronix.

Programs need space

In addition, microprocessor hardware and software are often developed simultaneously, and debug includes both hardware and application-software testing. And most microprocessor programs are stored in ROM, so designers are faced with rigid size constraints. "In some cases there is literally no way to expand program memory size, and in others cost sensitivity to added componentry that supports added program size can be large."■■

New single-board 16-bit μCs may soon be challenged by 16-bit chips

Dave Bursky
Associate Editor

The 16-bit single-board microcomputer still involves more talk than action. There's only one complete single-board system available—and it's the TM 990/100M from Texas Instruments. All others lack either memory space or input-output capability, or both.

But, more complete single-boards are on the way promised the speakers at the 16-bit Microcomputer panel session of the Mini/Microcomputer Conference in Philadelphia.

Not only that, but Jim Huffhines, the director of MOS microprocessor marketing at Texas Instruments (Houston, TX), predicts that increases in IC density will lead to complex single-chip microcomputers that will, in some cases, make the single-board μC obsolete. By 1983, predicts Huffhines, ROM-dominant chips will be able to store 32 kwords of memory in addition to a full 16-bit processor and some I/O capability (see table).

Density boosts speed

And, as density increases, clock speed increases—whether the circuit is an all-in-one microcomputer chip or a general-purpose microprocessor. Devices in a chip will be both smaller and closer together, which will reduce both propagation delays and capacitance. The result? Processing speed should increase fivefold by 1985.

One process that should help boost density is Intel's HMOS, according to Michael Lania, an Intel applications engineer. With HMOS, Lania points out, the new 8086 16-bit microprocessor has about the same die size as the original 8080 but double the word size and complexity. Actually, the 8086 is two processors in one—a bus controller and a logic processor, both operating asynchronously.

The 8086 will also have many minicomputer-like features, including an extended addressing capability of 1 Mbyte and high-level instructions such as multiply and divide. Operating speed will also be that of a minicomputer—many instructions will execute in less than a microsecond. The operating speed of the processor is partially attributed to the pipelined architecture that holds five instructions in a queue to speed the fetch operation for sequentially accessed instructions.

Two other prime contenders for 16-bit applications are the LSI-11 from Digital Equipment Corp. (Marlborough, MA) and the microNova from Data General (Southboro, MA). But neither is really a true, stand-alone computer since either the memory space or I/O capability of the boards is quite limited.

Indeed, with what may seem like backtracking, says Rolando Esterverena, LSI-11 product manager for DEC, the company recently announced the LSI-11/2—a half-sized LSI-11 card with the LSI-11 processor and just enough bus drive and control circuitry to function. For many applications, the physical board size is a limiting factor, DEC's reasoning goes. And since additional cards have to be used in most cases anyway, reducing card size will make systems easier to configure.

But changes in the LSI-11 won't stop there, hints Esterverena, DEC is hard at work evaluating IC technologies and performance capabilities to enhance the operating characteristics of the processor.

On a general note: 16-bit microprocessors currently being introduced by several manufacturers will perform an order-of-magnitude better than available devices, according to Howard Raphael, manager of microprocessor marketing and applications engineering at National Semiconductor (Santa Clara, CA).

The memory-addressing capacity of the larger processors will offer the user more I/O flexibility and addressing ranges of greater than a million bytes. This, in turn, means that larger system programs can be written and that high-level languages will be available.

To produce the 16-bit processors, Raphael continues, National Semiconductor is committed to its XMOS short-channel MOS process. This process permits subnanosecond on-chip gate delays that will, in turn, lead to submicrosecond instruction-cycle times.

Another trend in the high-end microprocessor market is the growing use of peripherals and dedicated memory systems (RAM, ROM and I/O on a chip). And as memories get denser, more solid-state software will be available—an 8-kbyte ROM-based Basic is already available from National Semiconductor and other companies.

Basic is not the only language being put into silicon. Pascal will shortly be available in ROM form, as well as APL and Fortran.

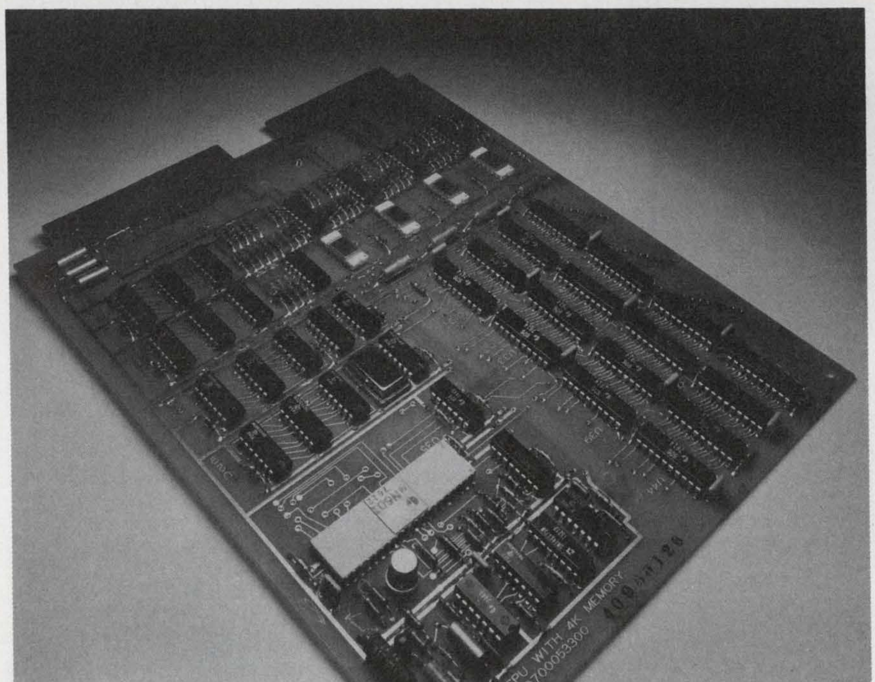
One key area of microcomputer use still in its infancy, states Raphael, is multitasking and multiprocessing. What's more, the troubleshooting techniques for such interwoven systems must still be developed. ■■

Projection of microcomputer capabilities

Current 16-bit all-in-one microcomputers:
TMS9940: 2 kbytes ROM, 128 bytes RAM — Address space & program counter are 16 bits wide

As circuit density increases the following products can be fabricated:

Microprocessors		1979	1981	1983	1985
ROM dominant	ROM	4 kbytes	16 kbytes	60 kbytes	—
	RAM	256 bytes	1 kbyte	4 kbytes	—
RAM dominant	ROM	128 bytes	128 bytes	128 bytes	128 bytes
	RAM	512 bytes	2 kbytes	8 kbytes	32 kbytes
Relative system speed		1.5×	2×	4×	5×



The 16-bit microNova computer board developed by Data General provides minicomputer power at microcomputer prices. Moreover, much of the Nova minicomputer software can be used.

As ATE software gets simpler, cheaper, tester features increase

Automatic-test-equipment makers are making it simpler and faster to program their systems. That should help cut the cost of the most expensive part of their system—software. What's more, new hardware and software features help ATE systems locate more faults.

A software package developed by GenRad Inc. (Concord, MA) cuts the time taken to model a complex chip to a fraction of what used to be necessary, says Brian Childs, a GenRad applications engineer, speaking at Nepcon in New York. Before, a chip had to be modeled as a collection of gates and flip-flops. For a complex IC like a microprocessor, the model "would be so horrendously large you probably wouldn't attempt it," says Childs.

With GenRad's Simulation Command Language, by contrast, the test system programmer writes a flow chart based on the device's block diagram—showing register-to-register movements, for example. The language converts this input to a model that takes up 1/3 the memory space of a gate-level model—in some cases, even 1/10 the size of the gate-level equivalent, says Childs.

The resulting model is added to the user's library in the same code as other models, so the use of SCL is transparent to the operator testing boards with the system.

Editing is easier

Making changes in an SCL model is simpler, too, says Childs. A change in one model function does not change all the other functions, he explains. And there's no need to change all the gates and flip-flops that perform a function, as is necessary in gate-level models.

The cost for all this? It's free—if you already have a GenRad test system. GenRad supplies the program to any of its users that need it to model proprietary LSI circuits, but charges for the required two-week training course. Stock programs for common microprocessor parts, like 8080 and 6800 family members, are available from GenRad at a price comparable with that of gate-level programs.

Cost, of course, is the main reason for using device models in automatic testing, explains Keith Wolski, vice-president of marketing and sales at Digitest Corp., Dallas. Moreover, since device models form the basis for automatic test generation any improvements would be welcome.

Digitest's ATG algorithm, Lasar, (logic automatic stimulus and response), has been improved with Alec, an automatic Laser executive control program that simplifies use and increases efficiency, says Wolski.

An Alec user feeds a computer circuit information, the percentage of fault coverage required, and whether faults should be detected to the failed IC or only to the failed node. Alec calls up the parts of the Lasar program necessary to generate the test, which can be in formats acceptable to many different ATE systems, including ones from Teradyne, Computer Automation and Tektronix.

With Lasar alone, the user has to call up a dozen or more program modules —stimulus generation, stimulus reduction, fault detection, and utilities among others—to generate a single test. To guarantee fault coverage, the test might take three or four times longer than with Alec, says Wolski.

But the greatest advantage of Alec lies in the ability to change a test program without rendering the program useless, which is what normally happens, says Wolski. Changing a program usually requires a new fault dictionary to trace faults, and cuts down the number of faults that the test can catch.

With Alec, a change in the test pro-

Automatic-test systems cut the cost of making PC boards. Now suppliers are looking to cut the cost of ATE's remaining bottleneck—software.

gram automatically changes the signals generated to stimulate the board under test so that the fault-detection percentage is maintained.

Computers find faults

Once a failure has been noted by a test system, the cause of the failure must be located. A number of features have been added to ATE system hardware and software to simplify this task, says Shelly Schneider, systems analyst at Instrumentation Engineering (Franklin Lakes, NJ).

Diagnostic clips allow an operator to read all pins of an IC at once, instead of probing one pin at a time. Not only does this save time, it also enables the test system to track down the first pin that fails—not the first pin probed that fails.

In addition, tracking optimization routines make diagnosis, especially in wired-OR and feedback circuits, faster and more accurate. "For bus-oriented components," Schneider explains, "the circuit description can describe the input conditions under which the outputs of a device are enabled. Reference data will then tell the algorithm which of the elements on a bus should be driving, and data read by the probe will tell which elements are actually driving."

In feedback loops, a technician might be able to locate the fault when the diagnostic probe can't, Schneider goes on: "On-line simulation during probing could detect, for instance, if a node is shorted and the corresponding pin's inputs and output are inconsistent."

But for boards that may contain analog as well as LSI digital circuitry, automatic test generation may not be useful, says Fred Macdonald, product manager for board test systems at Teradyne Inc., Boston, MA. ATG is sufficient for small and medium-scale-integration boards, he says, but the newest boards are more complex, bus-structured, and have more functions per chip. The solution, says Macdonald, is to combine "in-circuit' testing, static testing and fuctional testing.

But most in-circuit test systems can't handle the long test patterns needed with LSI parts, Macdonald warns, nor can they drive heavily loaded buses. After-in-circuit testing, Macdonald suggests static stuck-faults testing of all parts except the CPU. These segments can then run at speed to uncover timing problems. Then, for greater reassurance that all is well, the entire board can be functionally tested at speed.■■

CIRCLE NUMBER 26 ▶

News

Minis and μCs—a hit in class

Both minicomputer and microcomputer systems are being used more and more to provide remedial and educational services to students in grade school, junior-high school, high school and even colleges. That's what speakers revealed at a Symposium for Computers in the School and for Education in the Home, held at the Trenton (NJ) Computer Fest at Trenton State University.

With the cost of minicomputers dropping due to pressure from the high-end microprocessor and microcomputer market, educators are fast taking advantage of the available computing power. A typical educational system for a school without much funding consists of a PDP-11 minicomputer with 10 terminals, according to Marilyn Spencer, Coordinator of Instructional Computing for the Ridgewood, NJ, public schools. With the Digital Equipment Corp. users' library available and instructors writing programs, students have a wide range of remedial math, reading and spelling programs as well as self-pacing educational programs in science, history and English, and even games.

μCs for work and play

Many schools use microcomputers too, says Spencer. For instance, some Berkeley, CA, schools have over 20 microcomputer systems that students can use for learning or playing. Students work at their own pace and can select the program they want.

Still, computers are not benefiting all students. According to Spencer, studies have shown that pupils in grades lower than the fourth cannot make effective use of computerized learning systems due to poor physical coordination.

Meanwhile, large education computer systems are being reduced in size without reducing their usefulness, according to Dr. Carl Scholz of Advanced Interactive Systems (Philadelphia, PA). For example, the PLATO system developed by the University of Illinois and used in its medical school by students for updating and reference, was originally designed to operate on a large computer like an IBM 370. But now the system is being reduced to run on a large minicomputer in the PDP-11 family.

PLATO permits an English-like conversation with the computer, with almost no syntax or program format. The computer does a complete syntax analysis of every phrase typed in on a terminal and determines the key word or reference item in the phrase.

There are even computer systems available for the instructors. One such system, ERIC (Educational Resources Information Center), provides a worldwide computer network that can be accessed by educators and researchers. The data base consists of educational, education-related and social-science information. For a nominal fee, educators can access ERIC and receive bibliographic citations and abstracts of documents. Over 650 libraries worldwide support ERIC and provide microfiche copies of the referenced documents. (For more information about ERIC, contact Charles Hoover, National Institute of Education, 1200 19th Street, NW, Rm 709, Washington, DC 20208.)

To find out what various schools across the country are doing with computers, contact the Human Resources Research Organization, which has published a guide called the Academic Computing Directory (300 N. Washington Street, Alexandria, VA 22314, $3.95). This directory provides a list of all the schools that have some computing equipment or active computer-use programs, and the names of those in charge of the programs at each school.■■

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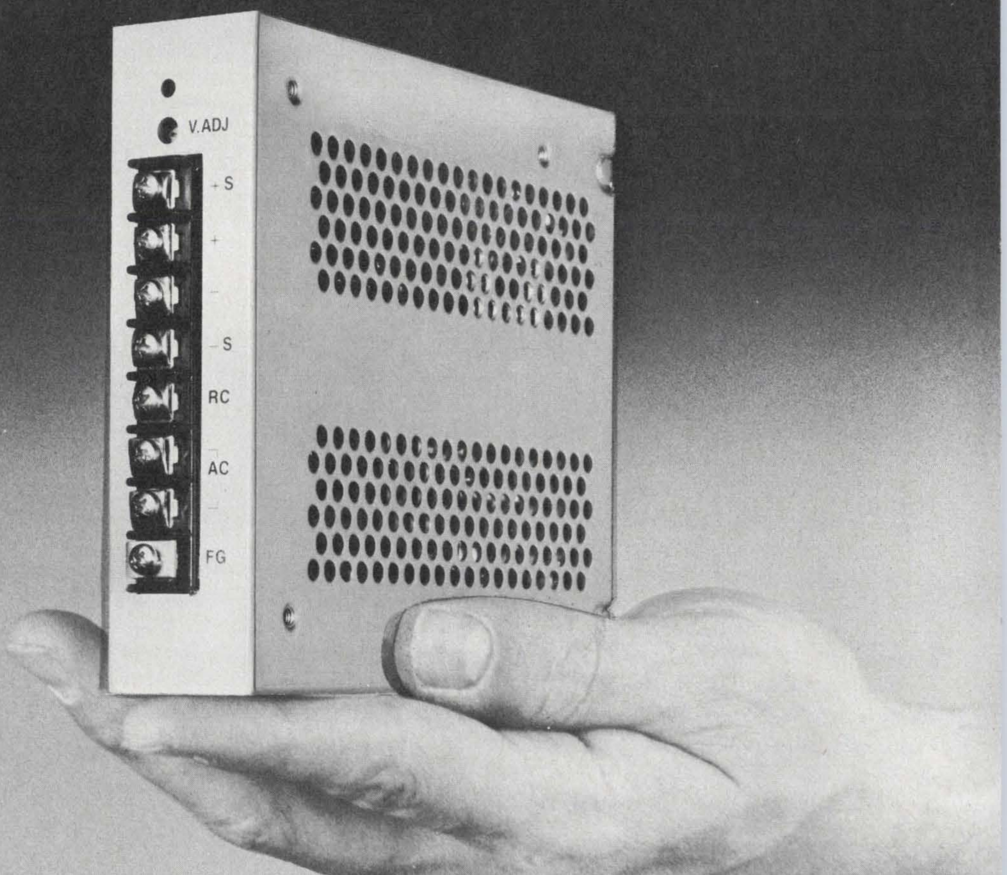

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Washington report

John Rhea, Washington Bureau

Pentagon spending on flight simulators to soar

By 1980, the Defense Department plans to be buying more than half a billion dollars' worth of flight simulators a year—nearly two and a half times as much as will be spent this year.

The major driving force is the uncertainty still clouding both the price and availability of jet fuel. The Arab oil boycott of 1973 triggered a crash program in the Pentagon to replace much of the combat training traditionally done in the air with on-the-ground simulation.

As oil prices have continued to soar, so has the price of air time. Defense officials now estimate that an hour in the air costs an average of eight times as much as an hour of simulator training. And while price ranges for hourly operating costs are put at $9 to $275 for simulators, they're put at $63 to $3610 for aircraft.

Lower cost isn't the only good thing about simulators. "An extremely important attribute of flight simulators is that they allow maneuvers that are dangerous or even forbidden in operating aircraft," says Dr. Ruth M. Davis, deputy undersecretary of defense for research and engineering. "A pilot can experience malfunctions and learn how to recover from catastrophes that cannot be reconstructed in aircraft in flight."

Commercial airlines, faced with razor-thin profit margins, have not only relied on flight simulators for years but have pioneered the technology. The military services are beginning to follow their lead. The Army, for example, which is spending nothing at all this year for simulators, wants $29.8-million in the fiscal 1979 budget. The long-range plan calls for more than double that, to $62.2-million, by fiscal 1980.

Navy and Marine Corps procurement of simulators is expected to decline somewhat—from $129.9 million this year to $128.2-million in fiscal 1979 to $120.8-million in 1980. But the Air Force will more than compensate for this drop. From $87.1-million this year, its simulator procurement is due to rise to $137.6-million in 1979, then more than double to $330.4-million in 1980.

At the same time, limited funds are being put into research and development of new simulators so that the services won't have to rely heavily on systems originally developed for the airlines. This budget item, almost all of which is spent by the Air Force, is projected at $45.6-million this year, $36.4-million in 1979 and $50.5-million in 1980.

GAO, in switch, praises sole-source procurement

The General Accounting Office has taken the unusual step of defending a sole-source procurement by the Navy of a new communications system on the grounds that the equipment was needed quickly and the contractor met or exceeded all government requirements.

Sole-source procurements are usually frowned upon. The GAO, acting as the Congressional watchdog for contracting irregularities, has criticized them in the past.

However, the watchdog office praised both the Navy and contractor Spectral Dynamics Corp. of San Diego for bringing in the WQC-5 acoustic communications system, which is used by submarines to contact surface ships and aircraft.

The original system, known as the SQT-2/WQR-2, had been purchased in 1972 from Sanders Associates (Nashua, NH) at a unit price of $73,000. But in 1974, Spectral Dynamics proposed a better system that could be put together from off-the-shelf commercial components for $54,280 apiece, and won the production contract from the Naval Sea Systems Command.

"The AN/WQC-5 has proven to be a very reliable and useful communication system," the GAO wrote to Sen. William Proxmire (D-WI) in defending the sole-source procurement. "It has exceeded its required mean time between failure by 150%. The contractor has met or exceeded delivery dates and has been cooperative in correcting any problems, generally without cost to the government."

Marines seek own battlefield laser target spotter

The Marine Corps, dissatisfied with the Army's battlefield ground-laser spotting systems for locating enemy forces, has decided to make its own.

Usually, the Marines depend on the Army to develop their battlefield equipment. The Army has two laser target designators and locators available, but one is too inaccurate at long ranges, while the other is too heavy (55 lb) to be man-portable, according to Brig. Gen. William H. Fitch, Marine Corps deputy chief of staff for research and development.

The Marines' MULE (modular universal laser equipment) is intended to weigh 38 lb including a 4-lb detachable north-finding module, and to be carried by two combat-equipped Marines. Accuracies are classified, but are said to be good enough to enable the Marines to hit both moving and stationary targets with the first round of artillery fire.

Capital capsules:

An "umbrella committee" to bring together government and industry struggles against the problems of electromagnetic interference has been formed under the aegis of the National Bureau of Standards. Members to date include the Electronic Industries Assn., IEEE, the Society of Automotive Engineers and the Motor Vehicle Manufacturers Assn. Chairman Myron L. Crawford of the NBS's Electromagnetic Fields Div. (Boulder, CO), says the group will enable the automotive, aerospace, defense and consumer-electronics industries to reach a consensus on EMI standards rather than try to tackle them separately. . . .**The Export-Import Bank, which helps to finance the purchase of American high-technology products abroad, is due to go out of business Sept. 30** unless Congress extends its charter for another five years. Industry groups are marshaling support for the bank at hearings now being conducted before the Senate Banking Committee. The bank is particularly important now that the U.S. balance-of-trade deficit has exceeded $30-billion, says Karl Harr, president of the Aerospace Industries Assn., adding that Eximbank finances 60% of American commercial aircraft sold abroad. . . .American electronics firms will be heavily represented at the **International Naval Technology Expo-78, scheduled for June 6-8 in Rotterdam, the Netherlands.** Americans will present more than half the technical papers at the sessions on communications, command and control, sensors and weapon-control systems. They are expected to dominate the adjoining technical display as well.

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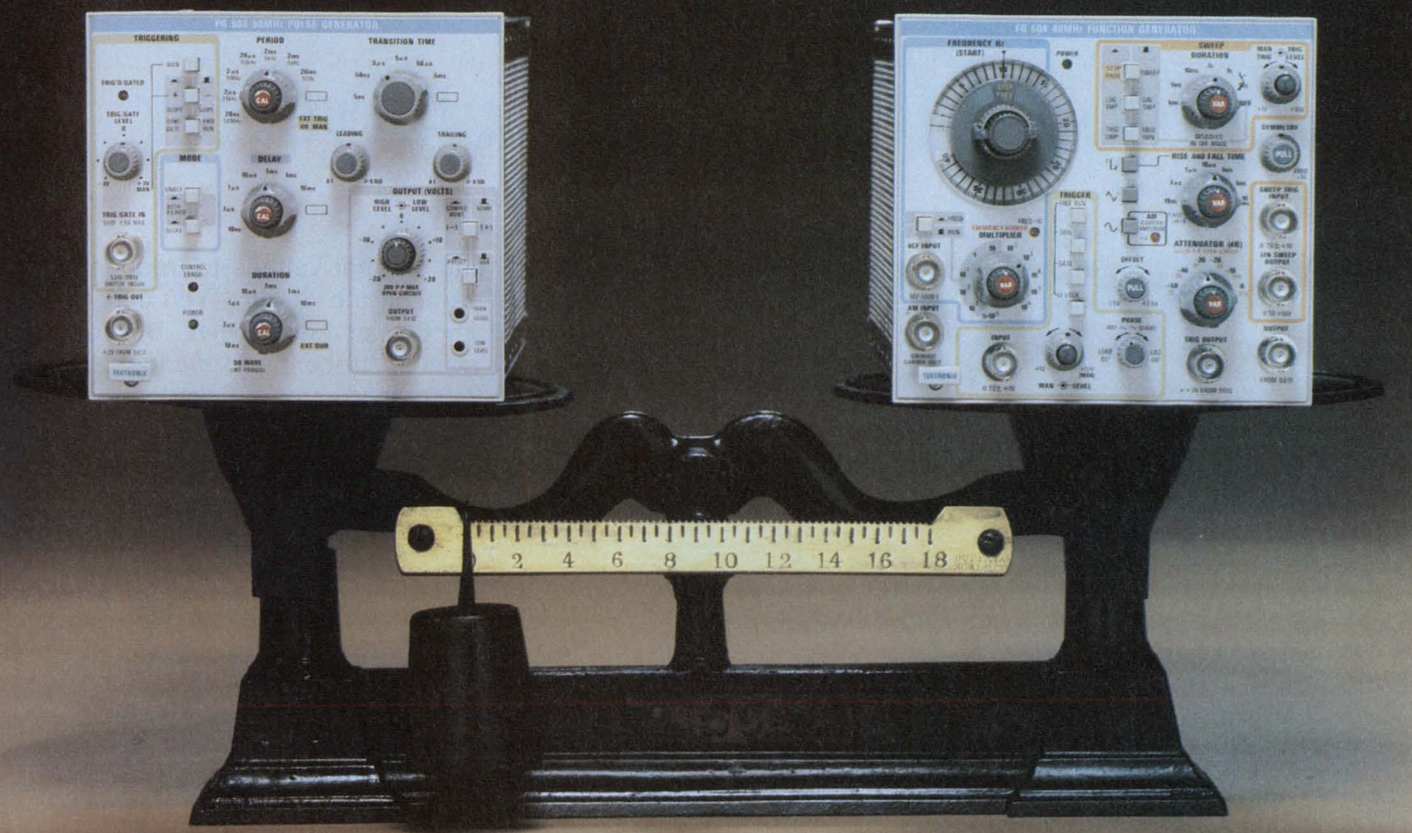

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PG 508	**FG 504**
Similar Features	
50 MHz	40 MHz
20 V p-p from 50 Ω ± 20 V window	30 V p-p from 50 Ω ± 20 V window
20 V max unipolar output	15 V max unipolar output
Unique Features	
Constant pulse width w/changes in frequency	Constant duty cycle w/changes in frequency
Delay and double pulses	Phase lock to an external signal
High/Low voltage controls	Voltage and offset controls

And, there's more. We've prepared an in-depth evaluation of the capabilities of these two instruments, and we'd like to give you a copy. (Just circle reader service number below.)

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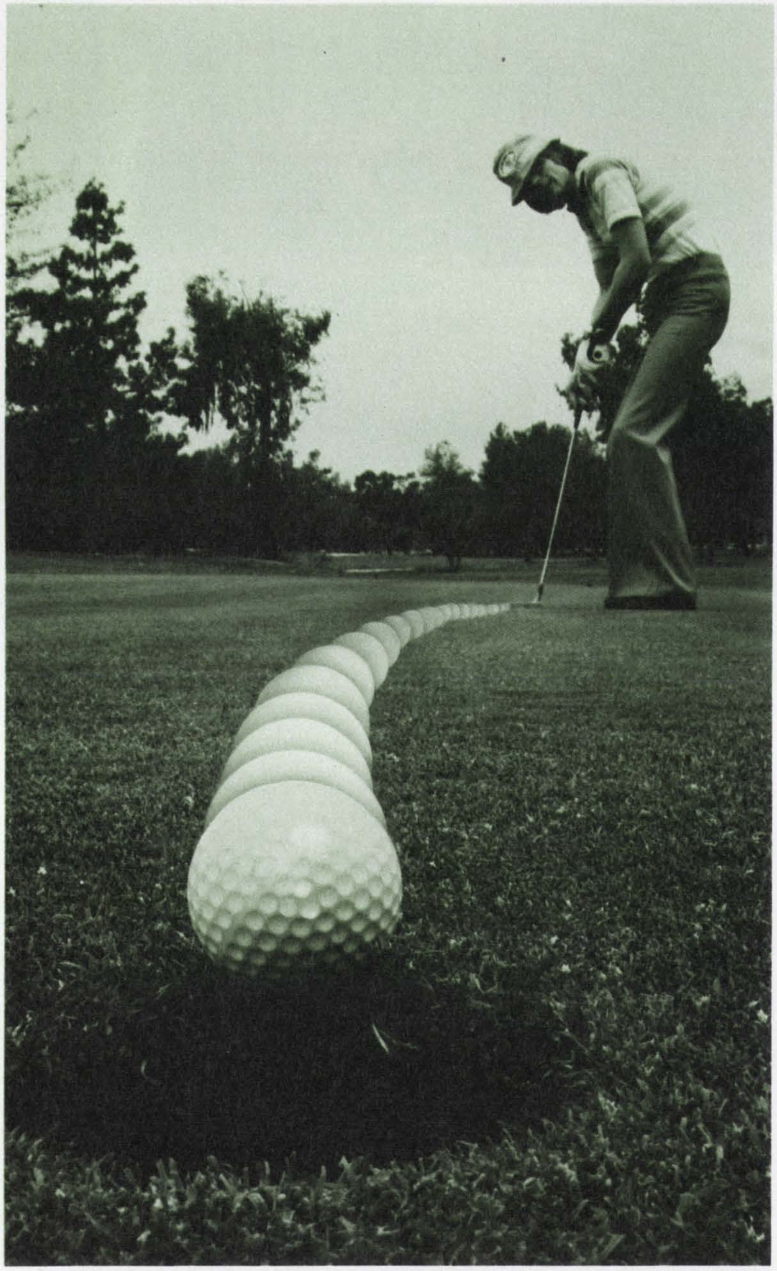

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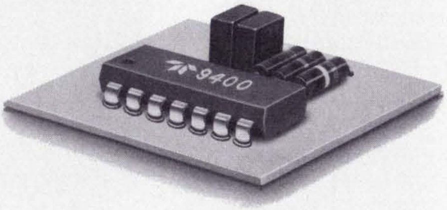

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CIRCLE NUMBER 31

Editorial

The way I see it

I've worked in this industry for 17 years, first as a designer and then as an editor. And one thing has remained constant through it all. The game keeps changing for the electronic design engineer.

New technologies and techniques continue to threaten the old ways of designing systems, equipment and circuits. To keep your competitive edge today, you've got to learn disciplines that were not evident yesterday.

Yet the new is bound to the old. New component technology must be compatible with existing techniques. Ever cheaper and more powerful digital and linear semiconductor components are linked to established analog and passive components; new magnetic and optic components must be related to existing interconnection, packaging and production techniques —and all require a design know-how unprecedented in 40 years of designing.

Today's design engineer must be a specialist in hardware and a generalist in software. He must know the nitty gritty of specifying catalog components without ignoring the implications of broad technological changes. He must know how to use what's here and how to prepare for what's coming.

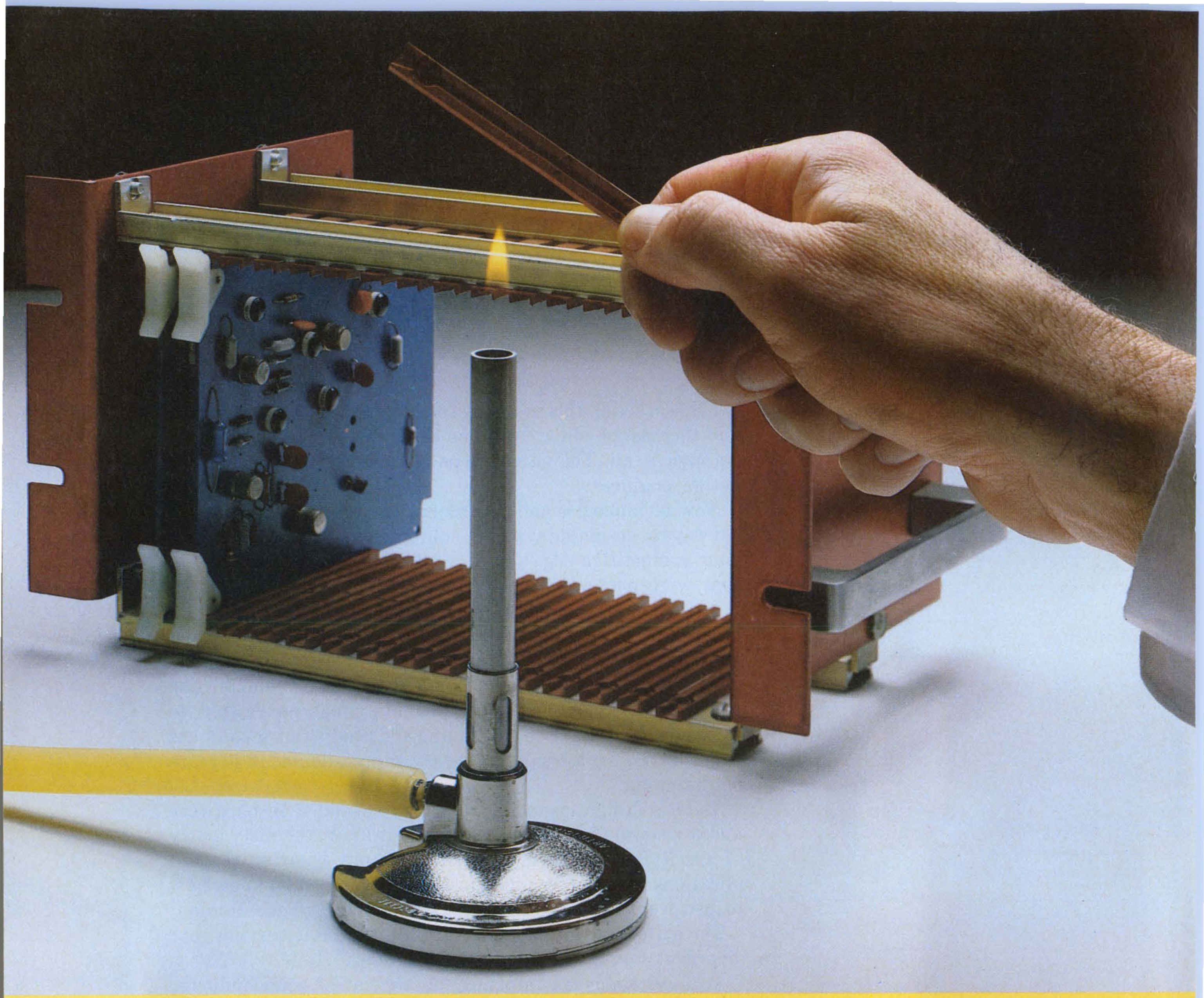
The editors of this magazine are committed to serving your divergent but interrelated design needs.

We will keep you informed on the latest semiconductor devices, as well as on the latest passive components. We will tell you how to implement software in mini and microcomputer systems, and how to design and build active and passive filter circuits. We will show you how to put together memory systems with the newest RAMs, and how to wire up a backplane with the newest flat cables.

In short, we will make ELECTRONIC DESIGN the sole wellspring of all relevant design information. Because we know that the designer who survives in this game needs the sharpest weapons.

Larry Altman

LAURENCE ALTMAN
Editor



MICROCOMPUTER DATA MANUAL

This manual contains three sections to help you evaluate the various microcomputer boards offered by over 30 manufacturers.

The first section deals with microcomputer specifications and some of the problems you will encounter when trying to make a selection. The tables included summarize the specifications of general-purpose microprocessors as well as all single-board microcomputers. Devices and boards are listed alphabetically by company.

The second section contains at least a page-long summary of data for each microcomputer board or family of boards. In some cases, a board's architecture is so complex, it warrants a page by itself. In other cases, the support hardware is so diverse, it can't fit on one page along with everything else. At any rate, each data-summary contains a complete capsule description of the processor board, its family of support products, software, and prices for all the boards as of April 1, 1978.

The third section is an appendix that summarizes the architecture and instruction sets of six popular microprocessors: the 8080/8085, the Z80, the 6800, the CDP1802, the 6100 and the TMS9900. This information will give you a good idea of processor capabilities and instruction flexibility.

Contents

The microcomputer card—a microprocessor or custom LSI-based computer system on a PC board—gives you a packaged solution to many processing problems. However, with the wide array of processors available and the many different features possible on a card, selecting the right microcomputer has become very difficult. Indeed, very little detailed information is readily available, since just three years ago there existed no off-the-shelf microcomputer card.

To find the best card, you now have to pore over dozens of technical manuals. And once you've selected the card for your system, you face an even tougher challenge—testing it. Since the boards are fairly general-purpose computer systems, they have an almost unlimited number of code combinations and I/O configurations. Thoroughly testing them, could require more than 10 years, even when they operate at top speed.

To help you understand the capabilities of each microcomputer board and simplify your selection, ELECTRONIC DESIGN presents the following Microcomputer Data Manual. The manual provides not only page-long performance summaries of each microcomputer board, but also comparison charts of microprocessors and microcomputers as well as a discussion of various specifications to help you narrow the field of choices.

A full card

A microcomputer card is a complete computer system, except for power supply and switches, on a single printed-circuit board. That means the card contains the central processor (usually a microprocessor, but it can be a custom LSI chip set or a bit-slice based processor), some read/write random-access memory, some permanent read-only program memory (ROM, PROM or EPROM), and some type of input/output interface (usually, a serial interface and some parallel I/O lines).

Typical cards include all the computer circuits except for the memories that hold the programs for your applications—you develop the program and plug in your own ROMs. Cards are intended to solve many of the small manufacturer's development problems: For applications requiring less than a few thousand boards, they offer an economical alternative to the company that designs a board from the ground up.

Many types of microcomputer cards are available, of course, but not all provide a complete solution. Most of the personal-computer central processor cards, for example, contain the processor, clock and buffers, but no program or data-memory space and no input/output lines except for the data and address buses. Systems built from these cards, then, need a large array of support just to satisfy minimum requirements.

There are a few manufacturers that make μC boards that meet the definition set forth, and they will be covered. However, cards containing only the processor and no memory or I/O aside from normal address and data buses will be left to a future report.

Many microprocessor development and prototyping systems offer most microcomputer features—CPU, RAM, ROM, and very limited I/O. But they aren't intended for expansion and in many cases have a built-in keypad and display for simple program development. Some of the boards also have an area where designers can create their own interface or auxiliary circuit. However, this means that each board must be customized by you for each final piece of equipment shipped—not an ideal situation for the high-volume user.

Some of the more flexible development and learning systems will find their way into limited production applications. Single-board systems that include a keyboard and display, such as the MMD-1 from E & L Instruments, the SDK-85 from Intel, the MEK6800D2 from Motorola, the KIM-1 from MOS Technology, the COSMAC VIP from RCA, and the VIM-1 from Synertek, permit you to develop programs in machine code, and usually include monitor programs in ROM that handle the keyboard, display control and peripheral interfacing.

More μC pretenders

Meanwhile, some of the recent microprocessor circuits—microcomputer chips—are actually edging into very low-cost applications formerly performed by simple boards. These chips meet almost all the requirements that define a microcomputer board. They have the CPU, RAM, ROM and some I/O capability all on a single chip. However, they do need other components to function—a crystal or R-C timing network and some I/O drivers or buffers, for starters. By the time these components are added, you have a microcomputer board, albeit a minimal system.

This system usually can't be expanded—often, the ROM and RAM space is built into the chip and can't grow as the application grows. Moreover, a chip is supplied with the application program already in it, so changes in the programming are almost impossible.

Now to business. To select a microcomputer card, start with examining the word size, the I/O capability, the instruction set and the memory capacity. The most commonly available word size for microcomputer boards is eight bits, although some 4 and 16-bit boards are available.

Start with word size

Indeed, most microcomputer and microprocessor specifications are very similar, if not identical. And for any single product, many are interrelated—for instance, I/O capability, speed, and word size can't be dealt with separately. You must work with all of them hand-in-hand. Somewhere, though, you must pick a starting point for your selection, and the processor word size and instruction set are probably the best places to begin.

Off-the-shelf boards have data-word lengths of 8, 12 or 16 bits and are available with bipolar, CMOS or NMOS processors on the board.

By far, the most popular microprocessor used by board manufacturers is the 8080A, although the 6800, Z80 and now the 8085A are closing fast. Not all microprocessors, though, are available on off-the-shelf boards, as you see by comparing the list of available microcomputer boards (Table 1) and the list of general-purpose microprocessors (Table 2).

The word size you pick depends heavily on the application and how fast and accurate the data processing and manipulating must be. If your system, for example, requires computational accuracies and resolution of 0.1% and looser, an 8-bit processor is most economical. Why? Simply because a system using, say, 8-bit a/d or d/a converters for analog signal processing, has a converter accuracy limited to about 0.1%; thus, tighter accuracies would be wasted.

An 8-bit processor can be used for systems that have more accurate converters, but each data word would require two memory words. A 12 or 16-bit processor can more easily handle the data for processing. Using the larger word size also keeps the number of memory accesses down, since only one access per data word would be needed.

Word size also depends very heavily on your instruction set. Some of the small-word-size processors have powerful instructions for manipulating data, while some 16-bit processors have limited bit or word-manipulation commands. Of course, the instruction set you need hinges on the application.

Applications that are very input/output-intensive should mate with processors that have a good mix of I/O commands in their repertoire. Commands such as bit or byte setting, incrementing or decrementing of data at the port should be sought. Other applications require a different mix of instructions.

For instance, data processing probably requires good arithmetic and logic-manipulative capability as well as efficient memory-reference instructions. Examine instruction sets, and you'll be able to estimate how useful the processor will be for your application.

But when examining the instruction set, don't get overly excited about a super-fast clock speed—the frequency of the clock is, in most cases, two to ten times faster than it takes to execute an instruction. Often, a manufacturer uses a basic cycle time or period—sometimes referred to as a microcycle—to define the instruction-execution time. The microcycle is not always the inverse of the clock frequency—it's often a multiple, possibly double or triple the clock.

Since each instruction, then, requires several microcycles to be executed, a three-microcycle command may require three, six or nine clock cycles. What's more, very complex instructions like divide and multiply can require hundreds of microcycles.

A test program helps

The internal processor architecture also determines how fast an instruction is executed—similar instructions from different processors will execute at different speeds, and thus give differences in performance. So, to really compare two processors, you should develop a complete test program to test all the instructions you're concerned with. Such a benchmarking program can help determine the power of a processor's instruction set, and also clarify another often abused specification—the number of instructions.

Comparisons abound based on the number of instructions available from a processor—but don't base your choice on such numbers. Make sure all the commands available are commands you can use—no sense getting variety if you need only a few.

Break down the instruction set into the different categories of commands to get a better picture of what is available. You'll find that, depending on the processor used on the board, the number of instructions for one particular category could range from one or two to over a dozen. Instructions you want but which aren't included in the regular instruction set can be provided by programmed subroutines, athough you'll sacrifice some processing speed for each subroutine you create to perform the desired task.

Examine each processor's programming manual carefully—the number of instructions available can shrink or grow from page to page. This is because many instructions operate on various registers within the processor or can be used in different ways. While some manuals just list a basic instruction and its dozen or so variations, others call each variation a different instruction. Up goes the number of commands.

Take a look at the instruction set for the Z80, for example. There are 158 commands, but after you've taken into account all the possible addressing modes and variations, you end up with 696 instruction codes.

The most flexible instruction sets often come with 16-bit processors since they are, in most cases, reduced versions of available minicomputers. Some 16-bit processors offer multiply and divide instructions that execute in microseconds. Eight-bit processors require milliseconds to perform the same calculation, because they must be programmed by the user.

As a matter of fact, some true minicomputers are actually offered as single-board computers, including Computer Automation's LSI-4/10 Naked Mini and Digital Equipment Corp.'s LSI-11. These "stripped down" minicomputers provide a subset of the instruction set of the larger machines—CA's 4/90 from CA and DEC's PDP-11—and have just enough hardware. In fact, unless your application is pretty minimal, you'll have to add additional support cards for memory and I/O capability.

The complete basic instruction sets for many of the processor boards as well as basic microprocessor architectures are included in the appendix to this report. Additional information about the processors themselves is available in our Microprocessor Data Manual (ED No. 21, Oct. 11, 1977, p. 54).

Everything may be too much

Since the microcomputer board is intended to be a complete system, it should contain everything you need except the program. But how much of "everything" will you really need? Most designers cannot answer this question before they design their systems. And even afterwards they may not be sure since new options can come along at any time.

To select a board, then, not only will you have to decide on the word size and the instruction set, but you'll have to figure how much on-board RAM, ROM and I/O you'll need, and what sort of expansion capabilities you'll want.

An old programmer's saying is that given a fixed amount of memory space, the program under development will grow to fill that space and 10% more. This isn't always the case, of course, but in this day of pin-compatible RAMs and ROMs, memory size can often be changed just by pulling out one chip and plugging in another.

However, microcomputer boards come with all manner of varying amounts of RAM and ROM. Available RAM space typically ranges from 256 bytes to well over 16 kbytes. For ROM space, most boards offer empty sockets that can hold as few as 256 bytes or as many as 8 kbytes.

Some of boards are not expandable—there are no address buses leaving the board, or the amount of on-board memory is already at the processor's addressing limits. As an alternative, companies offer families of boards so that if one version doesn't have enough memory or I/O capability, the next step up might.

If the board you've selected lets you add your own expansion memory, make sure you get the right speed memory chips—some processors require very-high-speed memory chips even though the cycle times seem slow.

In addition, find out how many ways the memory on the board can be accessed. Most microcomputer boards prohibit the on-board memory from being accessed from external sources—all memory accesses go through the processor, so data transfers to the memory are fairly slow. Boards that permit access to the memory from other sources offer many advantages for multiprocessing and applications where transfers from bulk-memory devices would occur.

Just as you can configure the memory the way you need it on the board, you can set up the input and output lines. Most boards provide the means to control external peripheral equipment via specialized and general-purpose I/O circuits. Some I/O circuits are programmable and must be set up with software whenever the board is initialized or the peripheral is changed. Other circuits are just simple line drivers and receivers that can be pin-strapped to set up their function.

The interface capability of the board's I/O lines can often be determined by selecting the proper line driver or receiver. However, the control and data buses have fixed interface requirements, some of which may be TTL, some CMOS and some three-state. Still, check the line buffering included on the board. Some lines may only be able to drive a single TTL normalized load while others might be able to handle 10 to 100 normalized loads per line.

The number of parallel I/O lines you can use is critical for many applications. Up to about 48 lines are available on most boards. These lines are often programmable as input or output, but they may be dedicated, depending on the applications envisioned by the board vendor. Some boards, though, have lines that can be programmed to be bidirectional—and can be software-controlled. These lines are handy for signaling applications and for simple serial-communications links.

Serial I/O capability is also available on most boards—either via RS-232 interfaces or via TTY 20-mA current-loop interfaces. The choice is sometimes user selectable via jumpers, and sometimes selectable at time of purchase by the board selection or components inserted. The maximum data rate on the serial line depends on whether the operating mode is synchronous or asynchronous. Many boards can handle asynchronous rates from 110 to 19,200 baud and synchronous rates up to about 56,000 baud. Baud rates are often switch or jumper-selectable, although some boards use communications chips controlled completely by software and permit the communication rates to be adjusted "on the fly" to communicate at whatever rate the peripheral is operating.

We interrupt this program...

If an application involves unpredictable or asynchronous events, an interrupt capability on the board is essential. Most boards have at least one level of interrupt, but only a few of the newer units can handle several levels of prioritized interrupt.

Interrupts are often used when a peripheral must transmit large amounts of data to the processor very rapidly. If the board can do direct-memory access, the processor can withdraw from the communications loop after an interrupt and permit data to transfer synchronously at high speeds between the peripheral and the memory. DMA transfers through the processor.

One thing you'll have a hard time checking is noise immunity—an important spec if your application includes an industrial environment as one of the factors. You won't find the spec on most microcomputer data sheets. But you should know that not

Table 1. General-purpose microprocessors

Manufacturer	Processor	Process technology	Word size (data/instruction)	Direct addressing range (words)	Number of basic instructions	Maximum clock frequency (MHz)/phases	Instruction time shortest/longest[2] (µs)	TTL compatible	BCD arithmetic	On-chip interrupts/levels	Number of internal general-purpose registers	Number of stack registers	On-chip clock	DMA capability	Specialized memory & I/O circuits avail.	Prototyping system avail.	Package size (pins)	Voltages required (V)	Assembly language development system	High-level languages	Time-sharing cross software	Comments	Circle number
Motorola	MC14500	CMOS	1/4	0	16	1/1	1/1	Yes	No	Yes/1	1	0	Yes	No	No[4]	No	16	3 to 18	No	No	No	Needs external program counter	451
Intel	4004	PMOS	4/8	4k	46	0.74/2	10.8/21.6	No	Yes	Yes/1	16	3x12	No	No	Yes	No	16	15	Yes	Yes	Yes	Superseded by 4040	452
Intel	4040	PMOS	4/8	8k	60	0.74/2	10.8/21.6	No	Yes	Yes/1	24	7x12	No	No	Yes	Yes	24	15	Yes	Yes	Yes	General-purpose 4-bit µP	453
NEC Microcomputers	µPD541	PMOS	4/8	4k	69	0.5/2	6.4/38.4	Yes	Yes	Yes/8	4	8x12	No	Yes	Yes	Yes	42	5,−5	Yes	No	No	Intended for electronic cash registers, etc.	454
Fairchild	2 chip F8	NMOS	8/8	64k	69	2/1	2/13	Yes	Yes	Yes/1	64	RAM	Yes	Yes	Yes	Yes	40	5,12	Yes	Yes	Yes	Usually used with program storage unit	455
General Instrument	8000	PMOS	8/8	1k	48	0.8/2	1.25/3.75	No	Yes	Yes/1	48	0	No	No	Yes	Yes	40	5,−12	No	Yes	Yes	Predecessor of F8	457
Intel	8008	PMOS	8/8	16k	48	0.8/2	12.5/37.5	No	Yes	Yes/1	6	7x14	No	No	Yes	Yes	18	5,−9	Yes	Yes	Yes	Predecessor of 8080, still in wide use	458
Intel	8080A	NMOS	8/8	64k	78	2.6/2	1.5/3.75	Yes[3]	Yes	Yes/1	8	RAM	No	Yes	Yes	Yes	40	5,12,−5	Yes	Yes	Yes	By and large, still the most popular	459
Intel	8085	NMOS	8/8	64k	80	3/1	1.3/5.85	Yes	Yes	Yes/4	8	RAM	Yes	Yes	Yes	Yes	40	5	Yes	Yes	Yes	8080 code compatible, has built-in clock	460
MOS Technology	MCS-650X	NMOS	8/8	64k	56	4/1	0.5/3.5	Yes	Yes	Yes/1	0	RAM	Yes	No	Yes	Yes	40	5	Yes	Yes	Yes	Provides 13 addressing modes	461
MOS Technology	MCS-651X	NMOS	8/8	64k	56	4/2	0.5/3.5	Yes	Yes	Yes/1	0	RAM	No	No	Yes	Yes	40	5	Yes	Yes	Yes	Similar to 650X but needs 2ϕ clock	462
Motorola	M6800	NMOS	8/8	64k	89	2/2	1/2.5	Yes	Yes	Yes/1	0	RAM	No	Yes	Yes	Yes	40	5	Yes	Yes	Yes	Available in new depletion-load version	463
Motorola	M6809	NMOS	8/8	64k	100+	2/1	2/5	Yes	Yes	Yes/1	0	RAM	Yes	Yes	Yes	Yes	40	5	Yes	Yes	Yes	Enhanced 6800 command set	464
Motorola	M6802	NMOS	8/8	64k	89	2/1	2/5	Yes	Yes	Yes/1	0	RAM	Yes	Yes	Yes	Yes	40	5	Yes	Yes	Yes	Has 128 x 8 on-chip RAM	465
National Semiconductor	SC/MP	PMOS NMOS	8/8	64k	46	4/1	5/10	NMOS only	Yes	Yes/1	0	RAM	Yes	Yes	No[4]	Yes	40	5,−7	Yes	Yes	Yes	Has handy daisy-chain capability	466
NEC Microcomputers	µPD 8080A	NMOS	8/8	64k	78	2/2	1.92/8.16	Yes[3]	Yes	Yes/1	8	RAM	No	Yes	Yes	Yes	40	5,12,−5	Yes	Yes	Yes	Pin compatible but does BCD subtraction	467
RCA	1802	CMOS	8/8	64k	91	6.4/1	2.5/3.75	Yes	Yes	Yes/1	16	RAM	Yes	Yes	Yes	Yes	40	3 to 12	Yes	Yes	Yes	Superseded two-chip version	468
RCA	1803	CMOS	8/8	64k	91	6.4/1	2.5/3.75	Yes	Yes	Yes/1	16	RAM	Yes	Yes	Yes	Yes	28	3 to 12	Yes	Yes	Yes	Trimmed down version of 1802	469
Scientific Microsystems	SMS-300	Bi-polar	8/8	8k+	8	10/1		Yes	No	No		0	No		Yes		50		No	Yes	Yes	Very specialized instruction set	470
Signetics	2650	NMOS	8/8	32k	75	1.2/1	4.8/9.6	Yes	Yes	Yes/1	7	8x15	No	Yes	Yes	Yes	40	5	Yes	Yes	Yes	Has two higher speed versions	471
Zilog	Z80	NMOS	8/8	64k	150+	4/1	1/5.75	Yes	Yes	Yes/1	14	RAM	No	Yes	Yes	Yes	40	5	Yes	Yes	Yes	8080 instructions are a subset	472
Intersil	6100	CMOS	12/12	4k	81	4/1	2.5/5.5	Yes	No	Yes/1	0	RAM	Yes	Yes	Yes	Yes	40	4 to 11	Yes	Yes	Yes	Emulates PDP-8 instruction set	473
Toshiba	T3190	PMOS NMOS	12/12	4k	108	2.5/1	10/30	Yes	No	Yes/8	8	RAM	Yes	Yes	Yes	Yes	36	5, −5	Yes	Yes	Yes	Has multiply and divide inst.	474
Data General	mN601	NMOS	16/16	32k	42	8.33/2	1.2/29.5	Yes	No	Yes/1	4	RAM	Yes	Yes	Yes	No	40	5,10,14,−4.25	Yes	Yes	Yes	Emulates NOVA instruction set	475
Fairchild	9440	I^2L	16/16	64k	42	10/1		Yes	No	Yes/1	4	RAM	Yes	Yes	No[4]	No	40		No	No	No	Emulates NOVA instruction set	476
Ferranti	F100L	Bi-polar	16/16	32k	28	20/1	1.19/5.75	Yes	No	Yes/1	0	RAM	No	Yes	Yes	Yes	40	5	Yes	Yes	Yes	Can do double word operations	456
General Instrument	CP1600	NMOS	16/16	64k	87	4/2	1.6/4.8	Yes	No	Yes/1	8	RAM	No	Yes	Yes	Yes	40	5,12,−3	Yes	Yes	Yes	All internal registers can be accumulators	477
National Semiconductor	INS8900/PACE	NMOS/PMOS	16/16	64k	45	2/2	2.5/5	No	Yes	Yes/6	4	10x16	No	Yes	Yes	Yes	40	5,8,−12	Yes	Yes	Yes	Architecture intended for data handling	478
Panafacom	MN1610	NMOS	16/16	64k	33	2/2	2/6	Yes[3]	No	Yes/3	5	RAM	No	Yes	Yes	No	40	5,12,−3	Yes	No	No		479
Texas Instruments	TMS9980	NMOS	16/16[1]	16k	69	4/4	3.2/49.6	Yes[3]	No	Yes/4	16	RAM	Yes	Yes	Yes	No	40	5,12,−5	Yes	Yes	Yes	Small version of TMS 9900	480
Texas Instruments	TMS/SBP9900	NMOS I^2L	16/16	64k	69	4/4	2/31	Yes[3]	No	Yes/16	16	RAM	No	Yes	Yes	No	64	5,12,−5	Yes	Yes	Yes	Emulates 990 mini instructions	481
Western Digital	WD-16	NMOS	16/16	64k	116	3.3/4	2.1/780	Yes	Yes	Yes/16	6	RAM	No	Yes	Yes	Yes	40	5,12,−5	Yes	Yes	No	Very similar to DEC LSI-11	529

1. Has 8-bit external buses and 16-bit internal buses 2. With maximum clock 3. Except clock lines 4. Standard TTL or MOS circuits will suffice

Table 2. Single-board microcomputer systems

Manufacturer	Model	Word size in bits (data/address)	CPU type	Clock freq. (MHz) Min./Max.	Memory Kbytes (K=1024): Total addressable	Amount of RAM on card (b=bytes)	Amount of ROM on card*	DMA capability	Bus type (P=proprietary, blank= no bus)	Parallel I/O lines	Serial I/O: Number of ports	Baud rate (max.) (kbaud)	Interrupt provisions	Multiprocessing capability	Counter-timers: No. of timers/bits per timer
Advanced Micro Computer	SKC 85	8/15	8085 A	0.5/3	32	0.75	0/4		P	44	2		●		2/14
American Microsystems	EVK 300	8/16	6800	0.3/1	16	1	6	●		48	1	9.6			
Analog Precision	TPM 200	8/16	8080 A	1.1/2	16	0.25	1.2		P						
Apple Computer	A2B0004X	8/16	6502	1.023	64	4/48	0/12		P		1	9.6			
Applied Systems	ASC/80	8/16	8085	0.5/5	64	0.25/1	4		P		1			●	
Bedford Computer Systems	MCS	8/16	8080 A	1/2	52	1	0/7		P	24					
Computer Automation	LSI 4/10	16/	Custom	16	128	1/4 kwds		●	P		32 lines	19.2	●	●	
Control Logic	CSS-1143	8/16	Z-80	2	64	1	0/16		P		1	110b			
	MM1-MSC	8/16	Z-80	1.8432	64	1280b	0/2				4	50	●	●	
Cromemco	SCC-W	8/16	Z-80 A	4	0.512	1	0/8	●	S-100	24	1	76.8			5/16
Data General	microNova	16/15	mN601	8.3	32	2/4	0.5/4		P		1	16.6M			
Digital Eqpt. Corp.	KD11	16/15	LSI-11	2.6	32	4/4	0	●	P		1				
Dynabyte	BC 1-1	8/16	Z-80	2.5	64	4/16	0/12	●	P	88	4	9.6	●		
Ferranti	F 100	16/16	F-100 L	0/12	64	8/32	0/32		P	16	3			●	
Hawker-Siddeley	SM-CPU 80	8/16	8080 A	2	64	0	0		P			9.6	●	●	3/16
Henize Interactive Control	M-5002	8/16	MC 6802	0.9216/2	see comments		1/4	●	P	20	1	9.6	●	●	
Heurikon	MLZ-80	8/16	Z-80	2 or 4	64	4	0/8	●	Multibus	32	2	19.2	●	●	4/16
	MLP-8080	8/16	8080	2	64	2	2	●	P		2	9.6	●		

*provided/max. possible

Software A Assembler AP Applications package DB Debugging aids, monitor, etc. H High-level language(s) OS Operating system	Supply voltages (U=unregulated inputs; on-card regulators)	Board size (in.)	Comments	Circle number
DB	+5	3.9×6.3	256 bytes CMOS RAM with battery backup. Eurocard.	482
A, DB, H, OS	+5	10.5×12	Maximum addressable ROM 6 k. EPROM programming for S6834. Disassembler available.EVK-100, EVK-200 also available.	483
N/A	±5, ±12	6×8	8-bit a/d converter. I/O port enables only. Power-on reset.	484
A, DB, H,	±5, ±12	8.5×14	TTL serial interface, composite video output, cassette I/O port, ASCII keyboard input, audio output for loudspeaker, two joystick inputs. Parallel I/O is by bus accessory cards.	571
H	+5	4.5×6	Software includes executive and emulation programs in PROMs; also communications software. Optional: Z-80 CPU, multiprocessing capability, board size.	485
AP	+5,±15	5.25×9	No card rack required. Custom test firmware.	486
A, DB, H, OS	+5	7.5×16.9	Power fail shutdown and auto restart. Real-time clock. Pascal available. Multiply and divide instructions standard.	487
A, AP, DB, H, OS,	±5, ±12	16×8	User's program library available for both types.	572
A, AP, DB; H, OS	±5, +12	10×7	Serial ports TTL, to 9.6 kbaud asynch., 50 kbaud synch. Three interrupt inputs.	573
A, DB, H, OS	+8,±18 U	5×10	Mates with all S-100 compatible computers.	488
A, AP, SB, H, OS	+5, +15, -5	9.5×7.5	I/O is bit-serial at 16.6 MHz. Software includes most Nova and Eclipse programs.	574
A, AP, DB, H, OS	+5, +12	10.5×8.9	Jumper-selected restart mode. Double-precision fixed and floating-point arithmetic and multiply/divide options. Software-compatible with PDP-11.	575
A, H	±5,±12,+28	14.8×12.4	For control applications. 8 relay outputs, 16 LEDS, on-board EPROM programmer. Cassette port and video output.	489
N/A	+5	9.1×6.6	Other supply voltages may be needed.	490
N/A	+5,±12	9.74×6.81	Power fail detection and restart. Real-time clock. Watchdog timers. Double Eurocard.	491
A, AP, OS	+5,±12	9.75×5.98	Maximum addressable memory 61,440 bytes. RAM on card: 128 bytes provided, 1152 maximum. Power fail detection and restart. Optional battery backup for RAM. Accessory boards are Motorola-compatible.	492
A, HL, OS	+5,±12	6.75×12	On-card floppy-disc controller. Power-on jump to selectable start address. Bus watchdog timer. 16 Mbyte address capability possible. SDLC compatible, with hardware CRC. System bus not required for on-card operations.	493
A	+5,-9,-12	8.5×10.5	Addressing in 4K switch-selectable increments through 64K memory space.	494

N/A: not available

Manufacturer	Model	Word size in bits (data/address)	CPU type	Clock freq. (MHz) Min./Max.	Memory Kbytes (K=1024)				Bus type (P=proprietary)	Parallel I/O lines	Serial I/O		Interrupt provisions	Multiprocessing capability	Counter-timers: No. of timers/bits per timer
					Total addressable	Amount of RAM on card (b=bytes)	Amount of ROM on card*	DMA capability			Number of ports	Baud rate (max.) (kbaud)			
Hewlett-Packard	2108 K	16/16	Custom	28.5	2 M	see comments		●	21MX	16	0		●	●	
Hodge, Taylor	HTA 6800	8/16	6800	1	50	128 b	0/8	●	S-100	0	1	9.6	●	●	
Iasis	SBC 80/80 C	8/16	Z-80	2.048	64	16	0/16	●	SBC	64	1	38.4	●	●	2/16
	SBC 80/14 C	8/16	8080 A	2.048	64	4	0/8	●	SBC	48	1	38.4	●	●	2/16
Imsai	MPU-B	8/16	8085	3	64/1M	0.25	2/4	●	S-100	16	2	56	●	●	3/16
Intel	iSBC 80/04	8/16	8085 A	1.966	see comments	0.25	2/4		none	22	1	4.8	●		1/14
	iSBC 80/05	8/16	8085 A	1.966	64	0.5	2/4	●	Multibus	22	1	4.8	●	●	1/14
	iSBC 80/10 A	8/16	8080 A	2.048	64	1	0/8	●	Multibus	48	1	38.4	●	●	
	iSBC 80/20	8/16	8080 A	2.15	64	2	0/8	●	Multibus	48	1	38.4	●	●	2/16
MDS	MD-690	8/	MC 6802	1/2	56	1152 b	2		S-100	16	1	2.4		●	
Milertronics	PDC-102	8/16	8085	3.579	64	0.25			P	5	1	9.6		●	
Monolithic Systems	MSC-8001	8/16	Z-80 A	1/4	64	4/8	0/16	●	Multibus	48	1		●	●	2/16
Mostek	OEM-80	8/16	MK 3880	0.005/2.5	64	4/64	0/25	●	P	40	1	9.6		●	4/16
Motorola	M68 MM 01	8/16	MC 6800	1	41	1	0/4	●	EXORciser	60			●	●	
	M 68 MM 01 A	8/16	MC 6800	1	64	1	0/8	●	EXORciser	40	1	9.6	●	●	
	M 68 MM 01 B	8/16	MC 6802	1	42	128 b	0/8	●	EXORciser	26	1	9.6	●	●	3/16
	M 68 MM 01 B 1	8/16	MC 6802	1	64	128 b/ 384 b	0/8	●	EXORciser	26	1	9.6	●	●	2/16
Mupro	MBC-80 CRT	8/16	8080 A	2/3.125	64	4/16	0/8	●	SBC-80	32	1	9.6	●	●	

*provided/max. possible

Software A Assembler AP Applications package DB Debugging aids, monitor, etc. H High-level language(s) OS Operating system	Supply voltages (U=unregulated inputs; on-card regulators)	Board size (in.)	Comments	Circle number
A, AP, DB, H, OS	+5,-2	18.13×13	Maximum addressable RAM 1 Mwords. User-microcodable. ROM on card is for microcode. Can address 16 Kwds of microcode off-card. DMA transfer to 1.14 Mwds/s. 16 words of RAM on card. Member of 21MX family.	495
A, AP, DB, H, OS	+5,±12	5×10	Hardware and software accessories to support Calcomp Trident disc storage modules. Some IBM software support.	496
A	±5,±12	6.75×12	Hardware single step. Jump to any address on reset. Separate RAM power bus and memory protect line.	497
A	±5,±12	6.75×12	SB80/10C: 1K of RAM on card, otherwise same as /14C.	498
DB	+8,±18 U	5.25×10	One Mbyte of RAM addressable thru auxiliary controller. Power-on jump.	499
DB	+5	6.75×7.85	Total addressable RAM 256 bytes; total addressable ROM 4K bytes. For stand-alone applications. Serial I/O via CPU's SID, SOD lines.	500
DB	+5	6.75×12	Same features as 04 but plugs into Multibus.	501
DB	±5,±12	6.75×12	Second-sourced by National Semiconductor and other companies.	502
DB	±5,±12	6.75×12	iSBC 80/20-4: 4 Kbytes of RAM on card. Up to 16 CPU's on bus.	503
DB	+8,±16 U	5.38×10	MC68B02 CPU also available. MIKBUG - compatible monitor designed to interface with most fast memory-mapped video and graphics boards.	504
DB	+5	4.38×4.86	PDC-100, which uses SC/MP II, also available; similar.	505
DB, OS	+5,±12	6.75×12	Z-80 based, Multibus compatible microcomputer.	506
A, DB, H, OS	+5,±12	12×8.5	Same as Z-80 CPU. ROM and RAM address mapping. OEM-80: No ROM supplied. Available is a complete ROM-based prototype package. European card: 233×250 mm.	507
A, DB.H	+5,-12	9.75×5.98	Has 3 PIAs. 120 I/O lines total. Suitable for control applications. Power-on reset. EXbug can be used.	508
A, DB, H	+5,±12	9.75×5.98	Has 2 PIAs. Power-on reset. EXbug can be used.	509
A, DB, H	+5	9.75×5.98	Battery can back up lower 32 bytes of RAM in low-power mode. Power on reset. EXbug can be used.	510
A, DB, H	+5	9.75×5 98	Battery can back up lower 32 bytes of RAM in low-power mode. Power-on reset. EXbug can be used. Built-in dymanic RAM refresh circuits. Power-on reset. Exbug can be used.	511
A, DB, HL, OS	+5,±12	6.75×12	16 of the 32 I/O lines dedicated to 8×8 key matrix. Built-in CRT interface for 80×24 CRT display.	512

Manufacturer	Model	Word size in bits (data/address)	CPU type	Clock freq. (MHz) Min./Max.	Memory Kbytes (K=1024): Total addressable	Memory: Amount of RAM on card (b=bytes)	Memory: Amount of ROM on card*	Memory: DMA capability	Bus type (P=proprietary)	Parallel I/O lines	Serial I/O: Number of ports	Serial I/O: Baud rate (max.) (kbaud)	Interrupt provisions	Multiprocessing capability	Counter-timers: No. of timers/bits per timer
National Semiconductor	IMP-16 C, L	16/16	IMP-16	5.7143	64	1	0/1	●	P	16	1		●	●	
	ISP-8 C/100 N	8/16	ISP-8 A/600	4	64	0.25	0/0.5		P	5	1	9.6	●	●	
	BLC-80 series	8/16	8080 A	2.048	64	see comments		●	SBC-80	48	1	38.4	●	●	
Ollituote Div. of Kone Oy	CPS-81	8/16	8080 A	2	32	1	0/2	●	P	16	1	9.6	●		5/16
Omnibyte	OB 8001	8/16	6800	1	64	1152b	0/4		P		1	19.2			
Pertec Computer	680 b	8/16	6800	0.5	64	1	0.24/1		P		1	9.6	●		
Pro-log	PLS-401	4/12	4004/4040	0.75	4	see comments			P	see comments					
	PLS-800	8/		1/3	8	1/2	0/8		P	40	1	9.6			
Process Computer Systems	PCS 1806	8/16	8080 A	2	64	1	0/7	●	Flexibus II	16	1	9.6	●		5/8
	PCS 1810	8/16	8080 A	2	64	1	0/3	●	Flexibus II	32	1	9.6	●		5/8
	PCS 1880	8/16	Z-80	4	64	1	0/6	●	Flexibus II	8	1	9.6	●		1/16
Processor Technology	Sol-PC	8/16	8080 A	2/3.57	64	2	2	●	S-100	16	1	9.6	●		
Quay	90/94 MPS	8/16	Z-80 A	2.5/4	64	5/65	1/7	●	P	64	1	9.6		●	4/16
Realistic Controls	MPPS-100	8/16	1802	2.4576	64	2	0/4	●	P	32	1	2.4	●	●	1/16
Space Byte	8085 CPU	8/16	8085	3	64	0.25	0/6	●	S-100	32	2	38.4	●	●	1/14
Synertek	CP 110	8/16	6502	1	64	1	1/5	●	P	28	3	9.6	●		1/16
Texas Instruments	TM 990/180 M	8/14	TMS 9980	2.5/3	16	0.5/1	2/4	●	P	24	1	38.4	●		2/16
	TM 990/100 M	16/15	TMS 9900	3	32	0.5/1	2/4	●	P	16	1	38.4	●		2/16
Wintek	WINCE CMM	8/16	6800	0.1/1	64	0.5	4	●	P	32	1	9.6		●	
Zilog	Z 80-MCB	8/16	Z-80	2.47	64	4/16	0/4	●	P	16	1	38.4	●	●	4/16

*provided/max. possible

Software A Assembler AP Applications package DB Debugging aids, monitor, etc. H High-level language(s) OS Operating system	Supply voltages (U=unregulated inputs; on-card regulators)	Board size (in.)	Comments	Circle number
OS	+5,-12	11×8.5	Multiprocessing, and 4 DMA ports (to 1Mwds) on -16L only. Battery backup line. External clock possible. ROMs extend instruction set. Hi-speed (97 Kwds/s) block transfer instructions.	513
DB, HL	+5	4.38×4.86	SC/MP II. Delay instruction (132 ms maximum). Suffix NE: Eurocard.	514
DB	±5,±12	6.75×12	BLC-80/10 is Intel SBC-80/10 equivalent. BLC-80/11 is Intel -10A equivalent. BLC-80/14 is same as BLC-80/12, except has 4K of RAM.	515
DB, OS	±5,±12	6.75×12	Four strobe pulses for multiplexed output. Eurocard.	516
A, DB, H, OS	±5, ±12	4.5×6.5	Parallel I/O: 16 programmable lines.	576
A, DB, H, OS	see comments	10×11	Parallel I/O thru bus and universal I/O card. Power supply on card except for transformer; low-voltage ac input.	517
	+5, -10	4.5×6.5	Eight models. On-board RAM to 640 4-bit nibbles. ROM up to 2048 4-bit words. I/O is 16 TTL input lines, 16 TTL output lines, several MOS-compatible lines.	577
A, AP, DB, H	±5, +12	4.5×6.5	Five models available—two with 8080A CPU, one with 8085, one with 6800 and one with Z-80 CPU. Serial I/O available only on 8085-based card.	578
A, DB, H, OS	±5,±12	10.5×8.5	Power fail interrupt.	518
A, DB, H, OS	±5,+5 to +30	10.5×8.5	Power fail interrupt.	519
A, DB, H, OS	±5,±12	10.5×8.5	Optional AMD 9511 hardware math chip with fixed, float, and conversions; logs, trig, etc.	520
A, DB, H, OS	±5,±12	16×10	Six configurations. All have 1024-character video out, 2K OS in ROM, audio cassette interface, keyboard interface.	521
DB, H	±5,+12,+28	16.18×7.88	CPU: Z-80 or Z-80A. PROM programmer. Single-step circuits. Hardware breakpoints. Total board memory to 72K. Backplane-independent.	522
A, AP, DB, H, OS	+5	9.87×7	10 mA total supply drain. Real-time clock. On-board ac supply and battery charger. Timesharing network development programs.	523
A, AP, DB, H	+8,±16 U	5×10	Parallel I/O port is intended for floppy disk interface.	524
A, DB, H	+5,+12,-10	4.25×7	Also called Super Jolt. 64 bytes of interrupt vector RAM on board. Microcomputer with keyboard, called VIM-1, also available.	525
A, DB, H	+5,±12	11×7.5	Serial data can be thru differential line driver/receiver. Prototyping area on board	526
A, DB, H	+5,±12	11×7.5	Multiply, divide, bit I/O instructions. Prototyping area on board. Another board also available, TM 990/101 M.	527
A, DB, H	+5,±12	4.5×6.5	44-pin/0.156 in. connectors. Some unusual accessory cards.	528
A, AP, DB, H, OS	+5,	7.7×7.5	Board has a 126 pin interface bus.	530

one available board is equipped with high-noise-immunity logic. You'll have to put in the shielding or signal protection yourself. Only a handful of μC boards use CMOS and so are more immune to noise than most NMOS or bipolar-based boards. Of course, some noise problems will still exist—high-speed operations always generate noise. And short spikes and transients could easily be mistaken for signals.

The boards that provide very-high-speed operations—less than 1 μs per instruction—use bipolar bit slices to form the heart of the processing section. These boards are microprogrammable in that a special memory holds the sequence of operations that define each of the computer's operations. And, by modifying the stored instructions in the microprogram memory, the way in which the computer instruction is performed can be altered.

Faster than the MOS

Typically, a bit-slice-based processsor is two to five times faster than a MOS-based machine. And it may require anywhere from 100 to over 1024 words of microprogram memory to control all instruction operations. However, each microprogram word is not the ordinary 8 to 16-bit data word size most processors use—the word can be from 20 to 60 bits long. This length is needed since the word controls more than just the processor—it manipulates the processor subfunctions, memory and peripherals.

Microprogrammed systems offer advantages over the predefined microprocessor-based machines since you can define your own instruction set and thus customize the processor for your application. And with microprogramming, you won't need as much peripheral control hardware since software can do much of the peripheral control.

Microprogramming also presents a good alternative for system emulation or when critical routines must be executed quickly.

There are, though, some drawbacks to a microprogrammed system. Because the programmer must work quickly to develop the final applications program, developing the microprogrammed instructions first will delay the introduction of the final system. And the over-all system must be defined before the software since the program has a great deal of control over the final hardware.

The single-board microcomputer business started out as a custom manufacturing business, and as a result, most of the boards are still not alternate-sourced. With few exceptions, no manufacturers make a pin-for-pin replacement, or even additional support, for another company's processor board.

The few exceptions include the Intel SBC-80 family of boards and the Motorola family of Micromodules. The Intel CPU boards are alternate-sourced by Iasis, Mupro and National Semiconductor and have a following of about 15 other companies that offer support peripheral boards. The Motorola boards don't have as wide an alternate sourcing, but the choice is rapidly growing.

One big reason that second-sourcing isn't commonplace is that each board manufacturer continually tries to out do the others with "innovative" features included on each board. Some CPU boards, for example, include counter/timers, DMA capabilities, a/d or d/a converters, specialized interfaces for specific peripherals, or even a second "slave"' processor. Your application will, of course, determine which of the features you're willing to pay for.

Processing power: ever on the increase

However, the most powerful boards are yet to come—in a few months, souped up CPU boards will be available from two companies. The SBC-80/30, being developed by Intel, will contain the 8085 μP as a CPU, operate at 3 MHz, handle eight levels of prioritized interrupt, offer fully programmable parallel and serial I/O lines, contain 16 kbytes of dynamic RAM and up to 4 kbytes of ROM/EPROM, and carry a socket for peripheral control by an auxiliary processor. The memory on the board will have dual-port access—in addition to the 8085 CPU on the board, CPUs connected to the Multibus will be able to access the memory.

The other board is under development by Advanced Micro Computers, a company founded by Advanced Micro Devices and Siemens. The Monoboard, as it is called, operates with a 4-MHz maximum clock and performs complex mathematical operations such as 16 and 32-bit signed two's complement arithmetic and 32-bit floating-point addition, subtraction, multiplication and division, as well as complex trigonometric and logarithmic functions.

The Monoboard contains eight levels of prioritized interrupt and four independent DMA channels. Optional ROM-based software includes monitors, text editors and macroassemblers. Up to two kbytes of additional EPROM can be stuffed on the board and four kbytes of static RAM will come as standard. A current-loop interface is also included on the board.

Other companies are rapidly introducing new boards. However, they are not really "standard" bus structures. The only buses, aside from the Intel Multibus, that are somewhat duplicated are the S-100 bus originated by MITS for the Altair microcomputer, and the EXORciser bus developed by Motorola for its development system. Every other board manufacturer offers a different bus for its own board.

The 100-pin S-100 bus is an intriguing phenomenon: Many designers claim it is a poor design, yet it has become enormously popular—it was there when nothing else existed. And now, it is so common that over 50 companies supply various peripheral products that plug into the bus. However, relatively few microcomputers plug into it—most of the CPU boards made for the S-100 bus are just that, CPUs. They contain no memory or I/O circuits and must communicate over the bus to auxiliary support boards.

For that matter, few of the boards that are compatible with the S-100 have all the features necessary to call themselves a complete microcomputer. One board that does, though, is an 8085-based board from Space Byte Inc. It contains two RS-232 ports, 22 parallel I/O lines, 256 bytes of RAM, up to 3 kbytes of ROM or EPROM (jumper-alterable to 6 kbytes using 2716s), a programmable 14-bit timer/counter and four levels of vectored interrupts.

Imsai Manufacturing also offers an 8085-based board, which has five levels of priority interrupts, 256 bytes of RAM, up to 2 kbytes of EPROM (jumper selectable for up to 4 kbytes of ROM), two serial ports, 22 parallel I/O lines, three counter/timers (16 bits each), and a power-on-jump initialization.

Although the S-100 bus was originally designed around an 8080-based CPU, several other bus-compatible processor boards are available. For instance, Analog Precision makes an 8080A-based board with an a/d converter on it.

All aboard the bus

Of course, designing with a standard bus eases some of the system definition problems, but which bus should you select? There are about six well known bus structures: the S-100, the SBC-80, EXORciser, LSI-11, Nova, and the SS-50 (a personal computing bus used with some 6800-based systems). The number of pins on the bus has little bearing on the flexibility of the bus—Wintek, for example, uses a 44-pin bus on its family of Wince cards. Zilog, on the other hand, uses a 126-pin bus for its Z80-MCB CPU card.

Differences in the complexity of the various bus structures may determine the complexity of the support hardware and the speed of input and output operations. And the layout of the bus—the way the power, signal and ground lines are interspersed—must also be examined when high data-transfer rates are expected. Some buses are bandwidth-limited to less than 1 MHz, while other buses, such as the SBC-80, can handle data transfers at rates up to 5 MHz.

Power requirements for the various microcomputers range all over the spectrum, from less than 100 mW for an all-CMOS board to several watts for the speedy bipolar boards. Your application will, of course, determine how much power you can spare for the computing function.

Support for microcomputer systems comes from more sources than just the original board manufacturers. For example, the SBC-80 family of microcomputer boards can count on close to 20 manufacturers of bus-compatible products. Similarly, DEC, Data General and Motorola have alternate suppliers of many peripheral support boards, although none of their suppliers offers a pin-compatible μC.

Available products range from simple digital I/O cards that add additional parallel or serial ports to the microcomputer, to large memory arrays of 64 kbytes and more, to specialized analog input/output boards or floppy-disc controllers. Intel even offers a high-speed mathematics processor that works in conjunction with the CPU board.

Developing programs for the microcomputers is very similar to the program-development cycle for any microprocessor-based product. But deciding on which development tool to use is just as complicated as trying to select the processor board. Features vary considerably from one manufacturer's system to another. Depending on the features offered, be prepared to spend anywhere from \$6000 to \$20,000 for a system that lets you program only one type of processor.

Variety, the spice of life

A few systems do permit you to work with more than one type of microprocessor, so that you can develop several projects concurrently without extensive overhead. You'll pay a little more for the base system—probably about \$25,000. What you're actually buying is a full-feature microcomputer system. Such a system typically includes 64 kbytes of RAM, a CRT terminal, a high-speed printer, a PROM programmer, a dual floppy-disc operating system, in-circuit emulation capability, and a tremendous amount of software capability, including a high-level language such as PL/M or even Fortran.

If you don't have the capital to invest in a development system, you can always use a larger computer to develop the software. Time-sharing software houses such as The Boston Systems Office (Boston, MA), National CSS (Norwalk, CT), General Electric Information Services (Bethesda, MD), First Data (Waltham, MA), United Computer Systems (Kansas City, MO), and Tymshare (Cupertino, CA) offer many cross-software packages that run on large minicomputers and mainframes. Each company's original programs offer different features, so compare before you get on-line or you'll be paying for something you're not getting or not using.

During a typical development cycle, you will use programs such as an assembler, editor, linker, loader and possibly a compiler. Large programs can be used to develop applications software, these are written in Basic, variations of PL/1, Fortran, Cobol and even other languages such as APL and Pascal. All the high-level languages, though, generate more code than would have been necessary had the program been developed in machine language from the start. That's the penalty you'll pay for the convenience of working in high-level languages.

Besides the basic development aids, simulators, emulators and debuggers are available to ensure that the error-free program gets to the end user as soon as possible. Even the time-sharing vendors offer some debug programs and simulators on the large computers that can be down-loaded to your system.

Time-sharing services, though, are no panacea. Computer time is expensive, so keep a careful watch over the on-line time, and even the storage space in the larger computer for your programs. Storage space, output time for listings, communication links and manpower will cost you dearly.

Costs, though, vary widely, depending on the service used and the approach taken by the programmer. Some programmers can keep program costs down by transferring some of the task to dedicated hardware. Or, if hardware has to be minimized, programmers can do that by transferring as many tasks as possible to software. However, there comes a point where the secondary jobs done by the processor may burden the circuit to such an extent that it can't perform its original task. When this happens, you may have to use a secondary processor or use dedicated support circuits to perform the jobs.

When you start a development project, don't forget to consider some of the peripheral equipment used in the development system. Keeping the overhead low by using, say, an ASR-33 teletypewriter instead of a high-speed printer for listing outputs is false economy. If you've spent the day correcting a 2000-line program and you want to get a correct listing with all the comments to double-check, you'll spend the night at the plant if you use an ASR-33.

Assuming that the printer does 10 characters per second and that each line has about 60 characters, you'll have to wait 12,000 seconds for a full listing (over three hours). With a faster printer—say, a 100 character-per-second unit—the print time would drop to just 20 minutes.

Does the system use a cassette, cartridge or disc-file system? Floppy-disc operating systems are the most popular and the most expensive, but they offer the fastest performance and the easiest storage capability.

Dual-disc systems offer the fastest response times since one disc typically holds the operating system program while the other holds the user files. This permits the RAM in the system to be used for developing programs instead of holding the operating system program.■■

Need more information?

Listed below are all the original-source microcomputer-board manufacturers and most alternate-source vendors. For additional companies and other types of processor boards, consult ELECTRONIC DESIGN's GOLD BOOK under Computers, Digital, General-Purpose; Computers, Digital, Industrial and Process Control; Computers, Digital, Instrument and Test-System Control; Computers, Digital, Micro; and Computers, Digital, Mini.

Advanced Micro Computers, 3330 Scott Blvd., Santa Clara, CA 95051. (408) 732-2400. **Circle No. 531**

American Microsystems Inc., 3800 Homestead Rd., Santa Clara, CA 95051. (408) 246-0330. **Circle No. 532**

Analog Precision Inc., 1620 N. Park Ave., Tucson, AZ 85719. (602) 622-1344. **Circle No. 533**

Apple Computer, 10260 Bandley Drive, Cupertino, CA 95014. (408) 996-1010. **Circle No. 534**

Applied Systems Corp., 26401 Harper Ave., St. Clair Shores, MI 48081. (313) 779-8700. **Circle No. 535**

Bedford Computer Systems Inc., 3 Preston Ct., Bedford, MA 01730. (617) 275-0870. **Circle No. 536**

Computer Automation Inc., 18651 Von Karman, Irvine, CA 92664. (714) 833-8830. **Circle No. 537**

Control Logic, Nine Tech Circle, Natick, MA 01760. (617) 655-1170. **Circle No. 538**

Cromemco, 2432 Charleston Rd., Mountain View, CA 94043. (415) 964-7400. **Circle No. 539**

Data General Corp., Rt. 9, 15 Turnpike Rd., Westboro, MA 01581. (617) 485-9100. **Circle No. 540**

Digital Equipment Corp., One Iron Way, Marlborough, MA 01752. (617) 481-7400. **Circle No. 541**

Dynabyte, 4020 Fabian, Palo Alto, CA 94303. (415) 494-7817. **Circle No. 542**

Henize Interactive Control Inc., 401A Astor Ave., Dayton, OH 45449. (513) 859-8118. **Circle No. 544**

Heurikon Corp., 700 W. Badger Rd., Madison, WI 53713. (608) 255-9075. **Circle No. 545**

Hewlett-Packard, 11000 Wolfe Rd., Cupertino, CA 95014. (408) 257-7000. **Circle No. 546**

Iasis Inc., 815 W. Maude Ave., Sunnyvale, CA 94086. (408) 732-5700. **Circle No. 547**

Imsai Mfg. Corp., 14860 Wicks Blvd., San Leandro, CA 94577. (415) 483-2093. **Circle No. 548**

Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051. (408) 246-7501. **Circle No. 549**

Kone Oy, Ruukintie 18, Espoo 32 SF-02320. Finland. 90-801-7011. **Circle No. 557**

MDS, P.O. Box 36051, Los Angeles, CA 90036. (213) 479-8761. **Circle No. 550**

Milertronics, 303 Airport Rd., Greenville, SC 29607. (803) 242-9232. **Circle No. 551**

Monolithic Systems Corp., 14 Inverness Dr. East, Englewood, CO 80110. (303) 770-7400. **Circle No. 552**

Mostek Corp., 1215 W. Crosby Rd., Carrollton, TX 75006. (214) 242-0444. **Circle No. 553**

Motorola, 2200 W. Broadway, Mesa, AZ 85201. (602) 962-3561. **Circle No. 554**

Mupro Inc., 424 Oakmead Pkwy., Sunnyvale, CA 94086. (408) 737-0500. **Circle No. 555**

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051. (408) 737-5000. **Circle No. 556**

Omnibyte Corp. 2711 B Curtiss Street, Downers Grove, IL 60515. (312) 852-8320. **Circle No. 558**

PCS Inc., 750 N. Maple Rd., Saline, MI 48176. (313) 429-4971. **Circle No. 559**

Pertec Computer Corp., 20630 Nordhoff Ave., Chatsworth, CA 91311. (213) 998-1800. **Circle No. 560**

Processor Technology Corp., 6200 Hollis St., Emeryville, CA 94608. (415) 652-8080. **Circle No. 561**

Pro-Log Corp., 2411 Garden Road, Monterey, CA 93940. (408) 372-4593. **Circle No. 562**

Quay Corp., P.O. Box 386, Freehold, NJ 07728. (201) 681-8700. **Circle No. 563**

Realistic Controls Corp., 3530 Warrensville Center Rd., Cleveland, OH 44122. (216) 751-3158. **Circle No. 564**

Space Byte, 1720 Pontius Ave., Suite 201, Los Angeles, CA 90025. (213) 468-8080. **Circle No. 565**

Synertek Systems, 2589 Scott Blvd., Santa Clara, CA 95051. (408) 247-8940. **Circle No. 566**

Texas Instruments, Digital Systems Div., P.O. Box 1444, MS 784, Houston, TX 77001. (713) 494-5115. **Circle No. 567**

Wintek Corp., 902 N. Ninth St., Lafayette, IN 47904. (317) 742-6802. **Circle No. 568**

Zilog, 10460 Bubb Rd., Cupertino, CA 95014. (408) 446-4666. **Circle No. 569**

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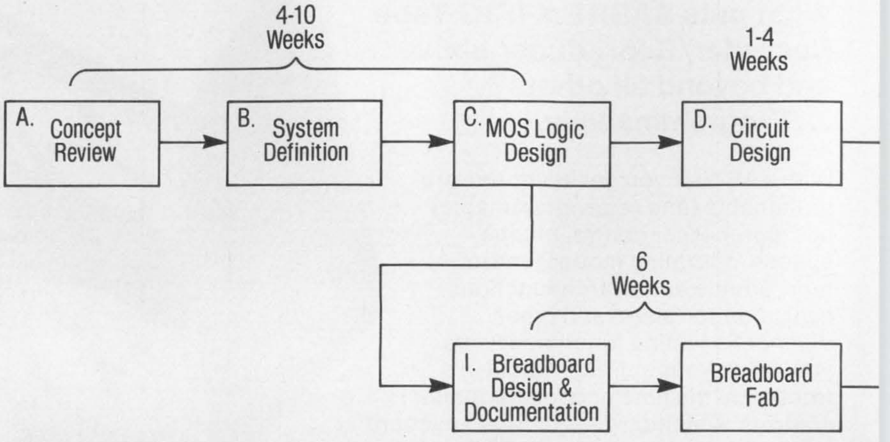

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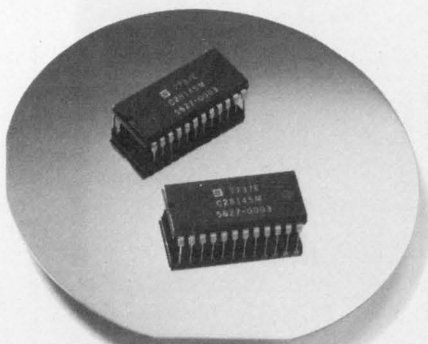

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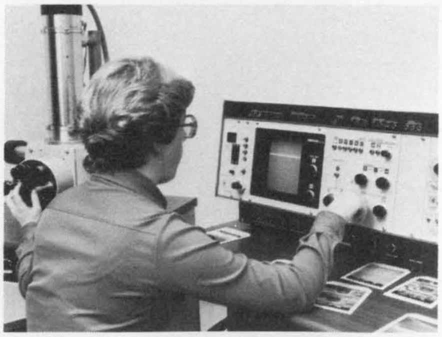

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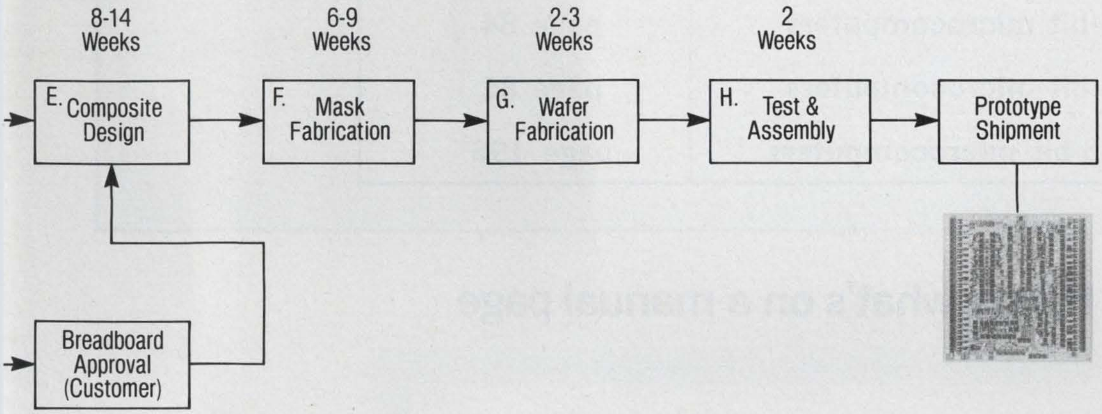

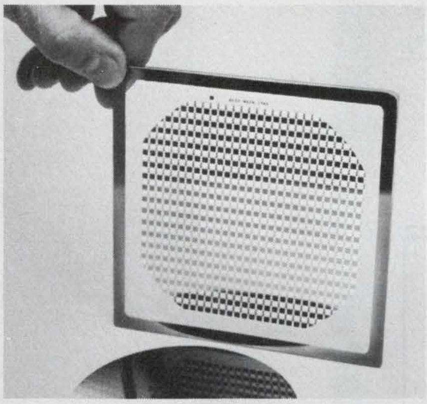

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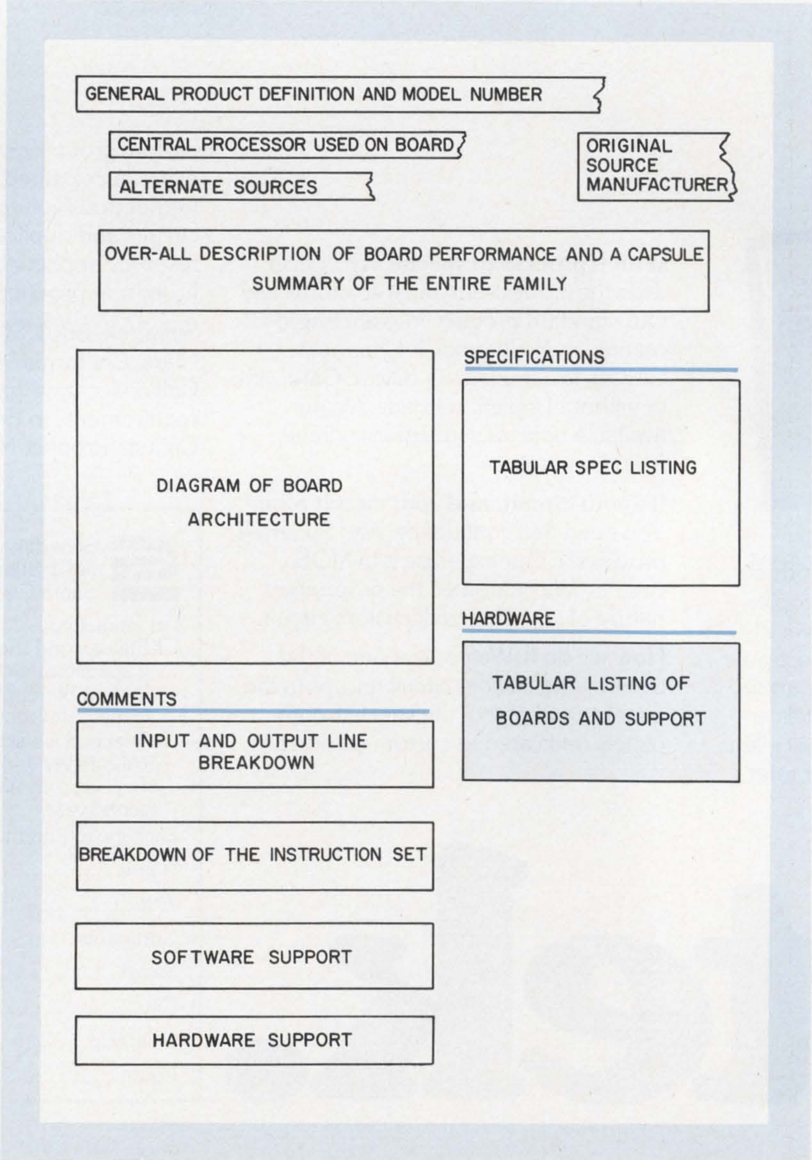
CIRCLE NUMBER 67

Using the Microcomputer Data Manual

The Data Manual's microcomputer data pages are organized first by processor-word size, then by processor type number (the most popular first), and then alphabetically by original-source manufacturer. The breakdown of generic families for this manual includes only three basic classes of processor boards:

Generic type	Page number
4-bit microcomputers	page 84
8-bit microcomputers	page 86
16-bit microcomputers	page 196

Here's what's on a manual page



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CIRCLE NUMBER 34

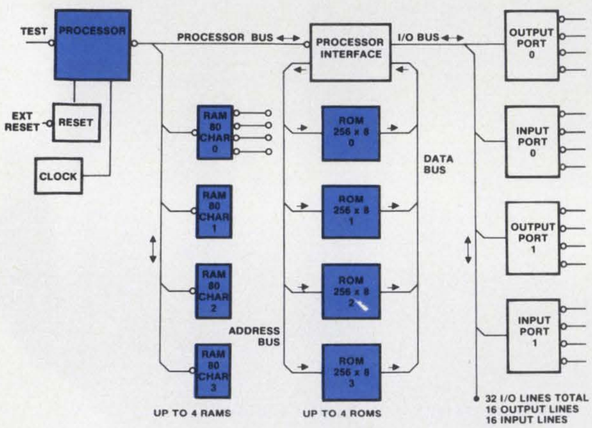
4-bit single-board microcomputers, PLS-401

μP used: 4004 or 4040

Alternate sources: None

Pro-Log
2411 Garden Road
Monterey, CA 93940
(408) 372-4593

The Pro-Log family of 4-bit microcomputer cards includes eight different models, the PLS-401, 411, 441, and the 4111, 4115, 4415, 4416 and 4417. The 401, 411, 4111 and 4115 are all based on the 4004 and the others are 4040 based. The 4004 based boards have RAM space for up to 640 4-bit characters and PROM space for up to 2048 words of instructions. Input and output lines are available as TTL latches or as MOS level RAM data lines on the boards. The 401, 411 and 441 are not expandable for memory or I/O, while the other five boards offer some expansion capability.



Specifications

Word size (data/address)	4/12 bits
On-board RAM (min/max)	up to 640 nibbles
On-board ROM (min/max)	2048 4-bit words
Addressable memory	4 kwords
Clock frequency	0.75 MHz
I/O ports, parallel	16 in/16 out TTL, up to 24 MOS
I/O ports, serial	0
Board size	114.3 × 165.1 mm
	4.5 × 6.5 in.
Power required (V/I)	5 V/550 mA
	−10 V/350 mA

Comments

The input and output lines of the 4-bit microcomputer cards are typically set up as 16 TTL level inputs, 16 TTL level outputs and then several MOS-compatible lines (usually there is at least 1 four-bit MOS port).

The instruction set is that of the 4004 or 4040 microprocessor. There are 60 commands for the 4040 and 46 for the 4004. Instructions are broken into three major groups—basic operations, machine-only instructions, and I/O and RAM commands.

Software support is available only in the form of some "starter sets" of boards and documentation.

Hardware support consists of the available memory and I/O boards as well as PROM programmers and an upgrade to 8-bit microcomputer cards.

Hardware

Model	Description	Price (unit qty)
PLS-401	Microcomputer (4004)	$ 195
PLS-411	Microcomputer (4004)	235
PLS-441	Microcomputer (4040)	215
4111	Microcomputer (4004)	140
4115	Microcomputer (4004)	205
4415	Microcomputer (4040)	240
4416	Microcomputer (4040)	250
4417	Microcomputer (4040)	205
4111-2	Memory card for 4111	60
4112	PROM card	115
4112-2	PROM expander	80
4125	PROM simulator for PLS-411	110

There is also a wide array of I/O cards and interconnect cables available.

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ANOTHER PRODUCT OF A COMPANY CALLED TRW

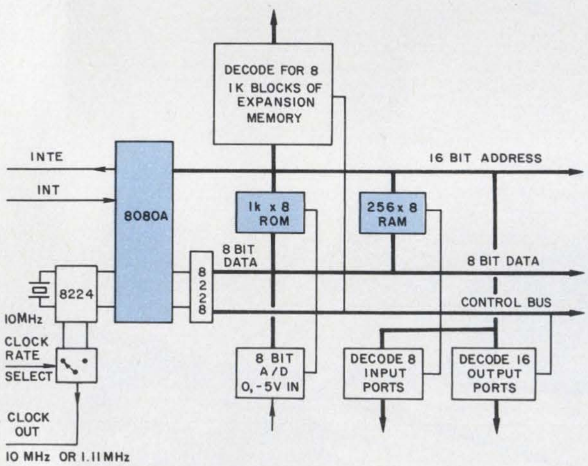
8-bit single-board microcomputer, TPM2

μP used: 8080A

Alternate sources: None

Analog Precision
1620 North Park Avenue
Tucson, AZ 85719
(602) 622-1344

An 8080A-based board, the TPM2 general-purpose microcomputer card includes 1 kbyte of ROM, 256 bytes of RAM, an 8-bit a/d converter, eight input lines, 16 output enable lines and power-on reset capability. For system interface, the microcomputer card uses an 80 pin bus. Intended for use in the company's line of process control instrumentation, off board ROM and RAM can be added to the processor.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	256 kbytes
On-board ROM (min/max)	1.25 kbytes
Addressable memory	32 kbytes
Clock frequency	18 MHz*
I/O ports, parallel	16 enable lines
I/O ports, serial	0
Board size	15.24 × 20.32 mm
	6 × 8 in.
Power required (V/I)	5 V/1000 mA
	−5 V/100 mA
	12 V/0.1 mA
	−12 V/0.1 mA

*divided down by clock generator to 2 MHz

Comments

The input and output lines consist of enable signal lines, eight as input and 16 as output. The actual ports are implemented off the card via support boards. One unique feature of the CPU card is that it contains an 8 bit analog-to-digital converter that can handle a single channel analog input of 0 to −5 V and digitize it for subsequent processing.

The instruction set consists of the 8080A's 78 basic commands. The commands break down into five basic groups: data transfer, arithmetic, logic, branch and stack, and I/O and machine control. There are also four addressing modes—direct, indirect, register and immediate. The move, load and store instructions can transfer either 8 or 16-bit data words between memory, the six working registers and the accumulator.

Hardware support for the TPM2 microcomputer card consists of specialized interface cards and signal conditioning circuits.

Software support for the microcomputer includes special purpose process control programs developed by the company and most commercially available 8080A programs.

Hardware

Model	Description	Price (100 qty)
TPM2	Microcomputer card	$ 105
INT 1	Interrupt controller card	90
TP 1	Teleprocessing port	80
TPM 2-11	Isolated analog input	N/A
LDF 2-1	Teleprocessing communications card	N/A

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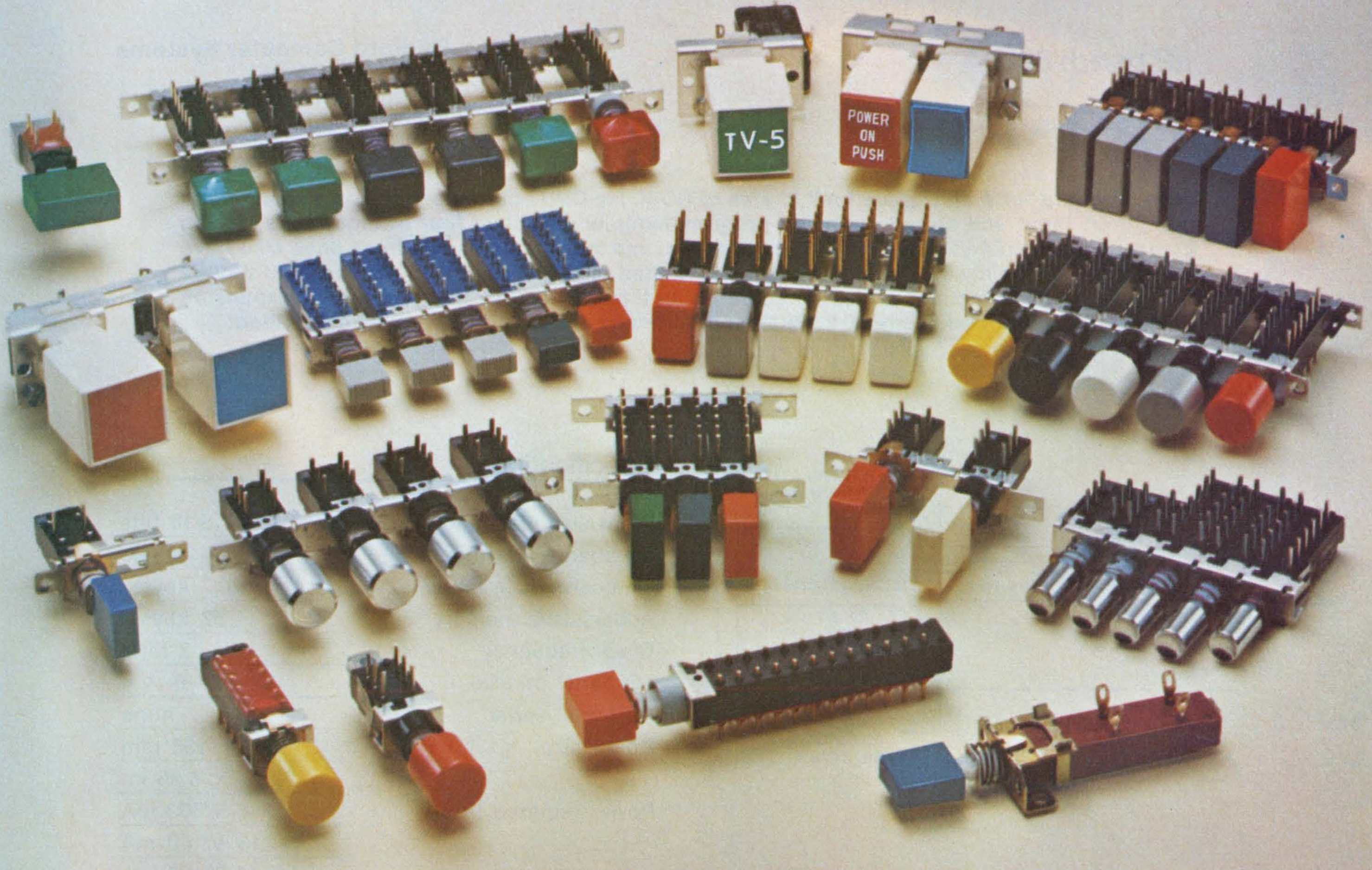

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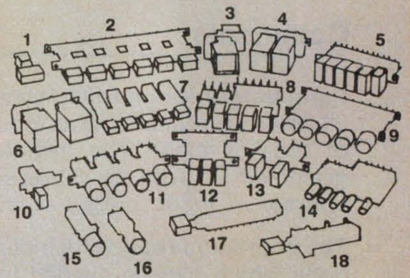
Key to Picture Above



1. Dust seal cover.
2. Interlocking lockout.
3. Lighted TV-5 line switch.
4. 17.5 mm lighted switch with flat and concave lenses.
5. Panel offset bracket.
6. 20 mm lighted switch with recessed lenses.
7. Diallyl phthalate insulation.
8. 10 mm gold terminals.
9. Master-on lockout.
10. Selective pin cutting.
11. Momentary actuation.
12. Momentary lockout.
13. Push-push and momentary assembly.
14. Override cam release function.
15. Epoxy seal.
16. Rear coupler.
17. Terminals with built-in standoff.
18. 2 amp. line switch.

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CIRCLE NUMBER 36

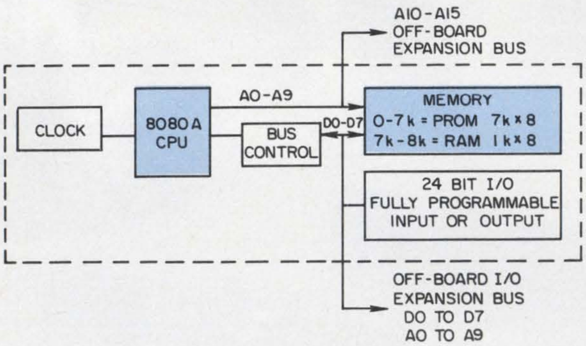
8-bit single-board microcomputer, MCS

μP used: 8080A

Alternate sources: None

Bedford Computer Systems
3 Preston Court
Bedford, MA 01730
(617) 275-0870

With on-board RAM and space for 7 kbytes of ROM, the CPU board functions as a stand-alone computer. Input and output ports are programmable in groups of four or eight lines. Seven control lines and 24 I/O lines are TTL-compatible, and the 24 data and address lines also have three-state capability. Expansion boards are bolted to a 5.25-in. frame and no card rack is required. Interconnections are either soldered, or through plug-in ribbon cables. All expansion I/O is memory mapped above 60 k. Custom boards and custom software can be provided.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1 kbyte
On-board ROM (min/max)	0/7 kbytes
Addressable memory	52 kbytes
Clock frequency	2 MHz
I/O ports, parallel	6 × 4
I/O ports, serial	none
Board size	229 × 136 mm
	9 × 5.25 in.
Power required (V/I)	5 V/600 mA
	15 V/100 mA
	−15 V/100 mA

Comments

Input/output is controlled by an 8255, which offers 24 lines, programmable as input or output in groups of four or eight. The device is defined as programmed I/O with bit set/reset capability, and can operate in input, output or bidirectional mode.

The command repertoire includes 78 basic instructions which can be divided into five groups: data transfer, arithmetic, logic, branch and stack, I/O and machine control. There are four addressing modes —direct, indirect, register and immediate.

Software support consists primarily of custom firmware, both for testing and applications.

Firmware includes parallel and serial I/O boards, a/d and d/a converters, printer and display controls and a power supply. The MCS is capable of addressing 52 kbytes of off-board RAM.

Hardware

Model	Description	Price (100 qty)
80-0013	MCS CPU board	$ 300
80-0014	24-bit prog'ble I/O	60
80-0015	12-bit a/d converter	120
80-0055	USART with EIA I/O	60
80-0056	same, but 2 ports	85
50-0001	Power bus PC board	12
50-0002	Data bus PC board	18
82-0050	40-col. printer control	175
82-0051	Display/control panel	300
82-0052	Power supply (5, ±15 V)	250

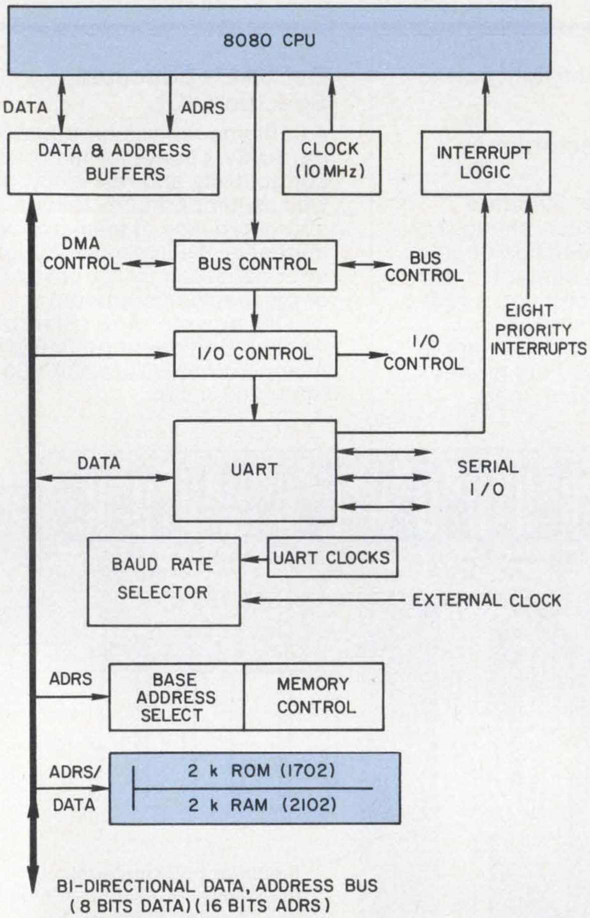
8-bit single-board microcomputer, MLP-8080

μP used: 8080A

Alternate sources: None

Heurikon
700 West Badger Road
Madison, WI 53713
(608) 255-9075

On a single circuit board, the MLP-8080 microcomputer packs the processor, 2 kbytes of RAM, up to 2 kbytes of EPROM, two serial interfaces (20 mA current loop and RS-232) eight levels of priority interrupt, and appropriate bus drivers. The board has no parallel I/O lines except for the bidirectional data bus and the 16-line address bus.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	2048 bytes
On-board ROM (min/max)	0/2048 bytes
Addressable memory	64 kbytes
Clock frequency	2 MHz
I/O ports, parallel	0
I/O ports, serial	3 (110 to 9600 baud)
Board size	216 × 266 mm
	8.5 × 10.5 in.
Power required (V/I)	5 V/3000 mA
	−9 V/250 mA
	−12 V/20 mA

Comments

There are only serial I/O lines on the MLP-8080 microcomputer board—an RS-232 and a 20 mA current loop. Both interfaces can operate at rates from 110 to 9600 baud, and are optically isolated to prevent transient damage.

The instruction set is that of the board's 8080A processor. There are 78 instructions that are grouped into data transfer operation, arithmetic commands, logic functions, branch and stack operations, and I/O and machine control instructions. There are also four addressing modes—direct, indirect, register and immediate.

Software support includes a monitor program for use with either a TTY or CRT terminal. When used with the board, it permits simple program development and execution. Also available are a Basic interpreter and a disc file management system.

Hardware

Model	Description	Price
MLP-8080	Microcomputer board	$ *
MLP-8010	4 k RAM/4 k ROM	
MLP-8016	16 k RAM & floppy-disc I/E	
MLP-8020	32 char × 16 line video card	
MLP-8022	80 char × 25 line video card	
MLP-8026-9	9 in. CRT display	
MLP-8026-12	12 in. CRT display	
MLP-8030	64 line I/O board (32 ea)	
MLP-8032	8 8-bit ports (4 in, 4 out)	
MLP-8035	Time base option	
MLP-8061	Floppy-disc drive	
MLP-8062	Dual floppy drive	
MLP-8064	Quad floppy drive	
MLP-8016F	controller w/16 k RAM	

There is also a wide array of system hardware such as front panels, chassis, breadboard cards, and terminals available.
* Prices are currently under revision; contact company for latest prices.

Hardware support consists of a wide array of boards and accessories. Also available is an intelligent terminal, the HIT-5000, that can be set up with a dual floppy-disc system and custom interface logic.

If you're looking for a low profile...

You need something other than the typical radial leaded capacitor. And that means that AVX's new dual-in-line DIPGuard® ceramic capacitor is exactly what you've been looking for.

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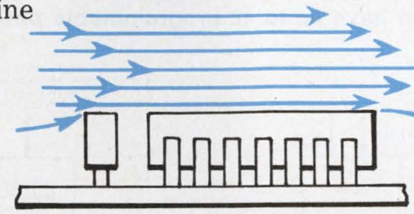
DIPGuard, on the other hand, has the same seated height as the IC package, a mere 0.175 inches. There's far less blocking of air circulation and, therefore, far more efficient cooling throughout the system.



DIPGuards offer another significant advantage. Because they have the same height and same lead spacing as the IC packages that you insert automatically, you can expect lower circuit board assembly cost.

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CIRCLE NUMBER 38

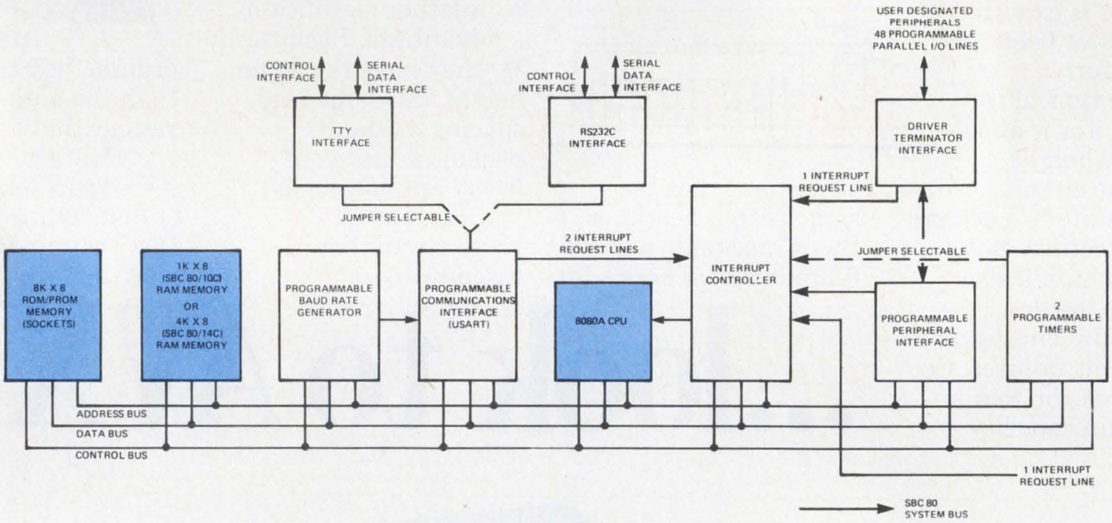
8-bit single-board microcomputer, 80/10C, 14C

Iasis
257 Humboldt Ct.
Sunnyvale, CA 94087
(408) 734-9600

μP used: 8080A

Alternate sources: Intel, Mupro, and National Semiconductor have pin compatible but not 100% function compatible boards.

The SBC-80/10C and 14C single-board microcomputers are compatible with the Intel Multibus and are pin replacements for the SBC-80/10A from Intel and the BLC-80/11 and 14 from National Semiconductor. There are some differences in the Iasis boards, though. Each of the boards have two real-time clocks, a DMA capability, and built in hardware single-step logic. The 10C can hold 1 kbyte of RAM (the 14C holds 4 kbytes) and up to 8 kbytes of ROM/EPROM. Both boards also handle one level of interrupt and have up to 48 programmable parallel I/O lines and a serial interface on the same board.



Comments

The input and output lines of the SBC-80/10C and 14C are formed by two 8255 PIOs. There are 48 parallel I/O lines that can be programmed as inputs, outputs or bidirectional. One serial I/O port is available and it can be configured as either an RS-232 or TTY interface capable of asynchronous operation over 75 to 9600 baud or synchronous operation up to 38,400 baud. Two counter/timers are also available, each with a resolution of 16 bits and capable of interrupting the processor.

The instruction set of the board is that of its 8080A CPU. There are 78 basic instructions that can be broken into data transfer operations, arithmetic commands, logic instructions, branch and stack functions, and I/O and machine control operations. There are also four addressing modes—direct, indirect, register and immediate.

Software support includes a monitor program in an optional PROM and, of course, most 8080A programs from various user libraries can also be used. Cross-software for program development is also available from many time-sharing vendors.

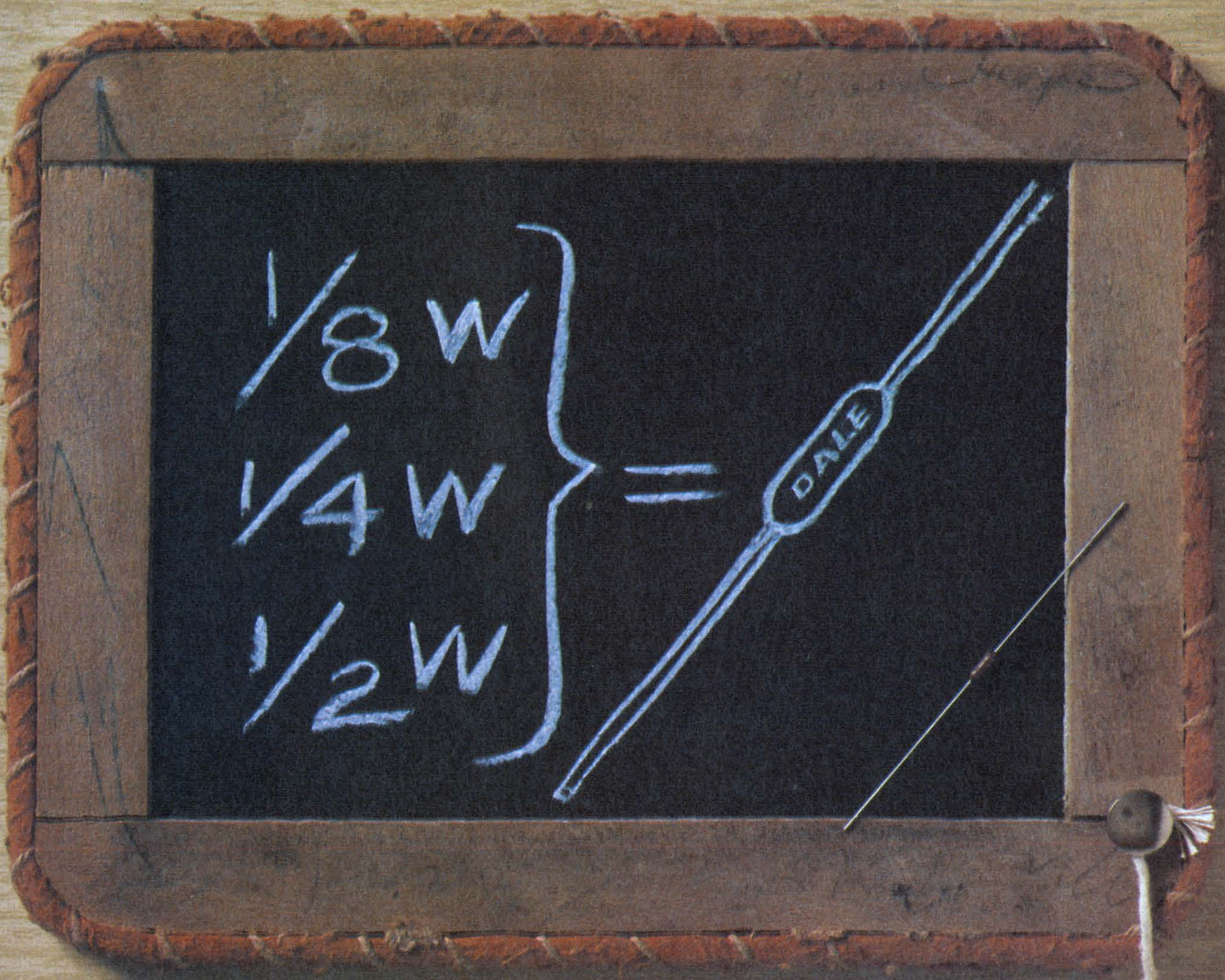
Hardware support from Iasis consists of the SBC-80/80C, a Z80-based processor board. There will be some applications support boards in the near future and users can currently select support from over a dozen manufacturers of SBC-80 boards.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	256 bytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	64 kbytes
Clock frequency	2.048 MHz
I/O ports, parallel	48 programmable
I/O ports, serial	1 (75 to 38,400 baud)
Board size	171.5 × 304.8 mm
	6.75 × 12 in.
Power required (V/I)	5 V/2500 mA
	12 V/140 mA
	−5 V/2 mA
	−12 V/100 mA

Hardware

Model	Description	Price (100 qty)
SBC-80/10C	Microcomputer board (1 k RAM)	$ 365
SBC-80/14C	Microcomputer board (4 k RAM)	435
SBC-80/80C	Microcomputer board (Z80 CPU)	500



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CIRCLE NUMBER 39

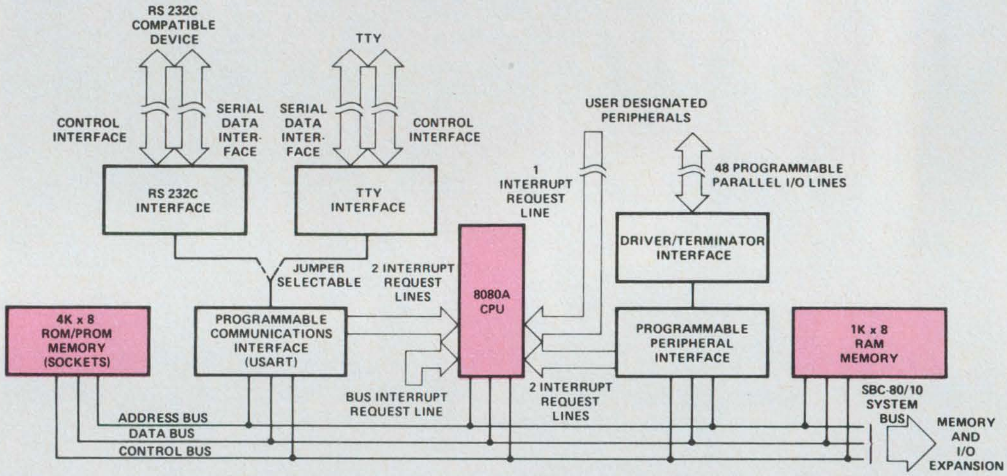
8-bit single-board microcomputer, 80/10A

μP used: 8080A

Alternate sources: Iasis, Mupro, National Semiconductor

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
(408) 987-8080

The SBC-80/10A microcomputer card is part of the SBC-80 family of five CPU cards. Features of the 80/10A include 48 programmable parallel I/O lines, a TTY and an RS-232 serial I/O port (jumper selectable) capable of synchronous or asynchronous operation, 1 kbyte of RAM, sockets for up to 8 kbytes of EPROM/ROM, and a baud-rate generator, jumper strappable from 75 to 38,400 baud. The board includes the interface logic for Intel's Multibus, operates in a multimaster mode, has six interrupt lines, and sockets for line and bus drivers.



Comments

Input and output lines of the SBC-80/10A consist of 48 programmable parallel lines and one serial port that can act as either an RS-232 or 20 mA current loop I/O line. The serial port can be asynchronous at data rates from 75 to 19,200 baud, or synchronous up to 38,400 baud. Sockets are used for the line drivers and receivers, so they can be user selected for optimum performance.

The instruction set of the board is that of the 8080A processor, which contains 78 basic instructions. The commands are divided into five groups: data transfer, arithmetic, logic, branch and stack, and I/O and machine control. There are also four addressing modes—direct, indirect, register, and immediate.

Software support for the SBC-80 family of boards includes a large library of user routines and, depending on the complexity of the system, the RMX-80 Real-time Multitasking Executive software package or the ISIS operating system in the MDS development systems. Cross software is also available from a large number of time-sharing software vendors.

Hardware support includes complete development systems such as the MDS and the Series II. These systems provide dual-disc operating systems and high-level language capability along with in-circuit emulation options to speed hardware and software. Also available are breadboard kits of the 8080 and 8085.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1024 bytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	64 kbytes
Clock frequency	2.048 MHz
I/O ports, parallel	6 × 8
I/O ports, serial	1 (75 to 38,400 baud)
Board size	171.5 × 304.8 mm
	6.75 × 12 in.
Power required (V/I)	5 V/2900 mA
	12 V/140 mA
	−5 V/2 mA
	−12 V/175 mA

Hardware

See page 95 for a complete listing of all boards.

Hardware for SBC-80 systems

Model	Description	Price (unit qty)	Model	Description	Price (unit qty)
SBC-80/04	Microcomputer board	$ 195	519	72 line digital I/O	$ 395
80/05	Microcomputer board	350	530	Teletypewriter adapter	150
80/10A	Microcomputer board	495	534	Quad serial I/O card	650
80/20	Microcomputer board	735	556	Optically isolated I/O	395
80/20-4	Microcomputer board	825	711	12-bit analog input card	895
310	High-speed math board	595	724	Quad 12-bit analog outputs	750
104	Combo memory & I/O	715			
108	Larger version of 104	815	732	Combination analog & digital I/O board	1125
116	Larger version of 108	985			
201	Diskette controller	995	604	Cardcage and backplane	170
202	Dual-density controller	1290	614	Expansion cardcage	170
212	Dual-drive system	4350	660	7-in high system crate with power supply	1350
016	16 k dynamic RAM board	825			
032	32 kbyte dynamic RAM	1360	630	Quad output power supply	270
048	48 kbyte dynamic RAM	1860			
064	64 kbyte dynamic RAM	2200	635	Larger version of 630	460
094	4 kbyte RAM/battery	795	RMX/80	Multitasking executive software package	1950
416	16 kbyte PROM/ROM card	295			
501	DMA controller	450			
508	64 line digital I/O	350			
517	Programmable parallel & serial I/O	400			

Also available are a wide range of cables and small hardware assemblies, as well as various diagnostic software packages and prototyping systems.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digital

OEM PRODUCTS GROUP

CIRCLE NUMBER 41

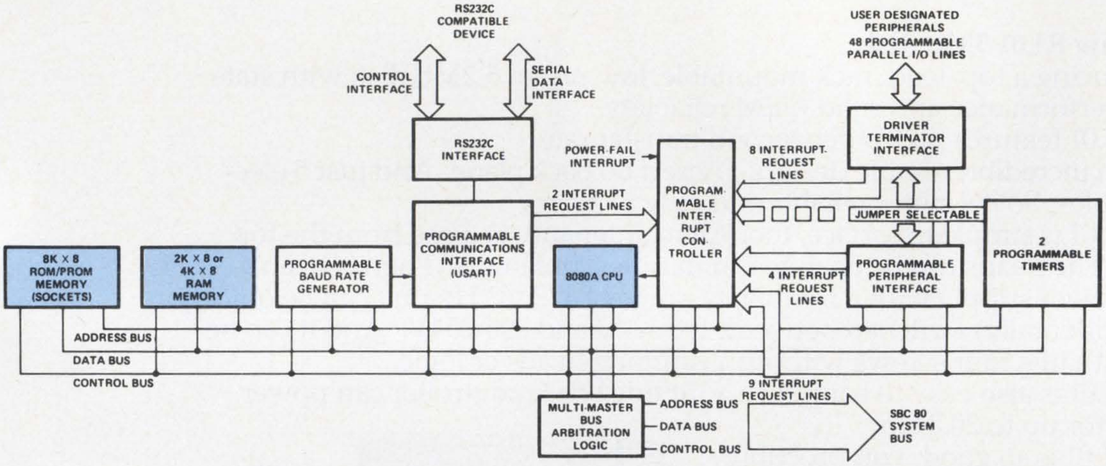
8-bit single-board microcomputer, 80/20, -4

μP used: 8080A

Alternate sources: None

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
(408) 987-8080

The high end of the SBC-80 family, the SBC-80/20 and 20-4 offer all the features of the 80/10A plus quite a few more. For example, the 80/10A has a strappable USART, while the 80/20s have a programmable one, where the 10A has 1 kbyte of RAM, the 20 has 2 kbytes and the 20-4 has 4 kbytes, and, where the 10A has a 2.048 MHz clock, the 20s have a 2.150 MHz, thus speeding up the processing even more. The 80/20 and 20-4 also have special bus arbitration logic so that they can be used in multiple bus-master systems, allowing up to 16 master CPUs to share the bus. There are also two programmable 16-bit binary or BCD timers and full eight-level priority interrupt logic on the boards.



Comments

The input and output lines of the SBC-80/20 and 20-4 consist of 48 programmable parallel lines and one serial port. The serial port is dedicated as an RS-232 compatible interface and has a fully software-programmable data rate and synchronous/asynchronous capability. Data rates range from 75 to 19,200 baud in the async mode and up to 38,400 in the sync mode. The parallel lines are set up as six groups of eight, but software can configure the lines in any combination of input, output and bidirectional lines. Sockets are provided for interchangeable I/O line drivers and terminators.

The instruction set of the board is that of the 8080A processor, which contains 78 basic instructions. The commands are divided into five groups: data transfer, arithmetic, logic, branch and stack, and I/O and machine control. There are also four addressing modes—direct, indirect, register, and immediate.

Software support for the SBC-80 family of boards includes a large library of user routines and, depending on the complexity of the system, the RMX-80 Real-time Multitasking Executive software package or the ISIS operating system in the MDS development systems. Cross software is also available from many time-sharing software vendors.

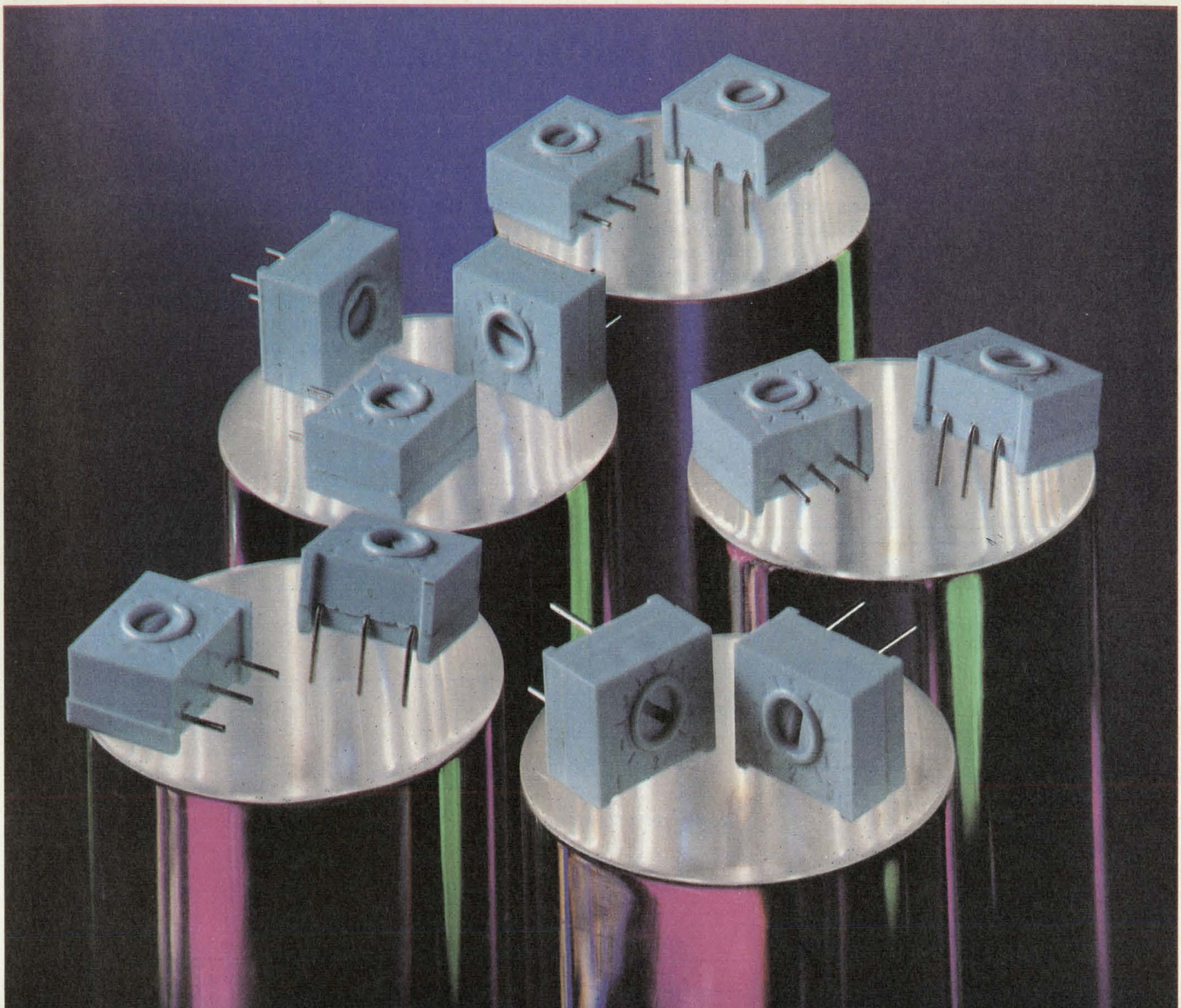
Hardware support includes complete development systems such as the MDS and the Series II. These systems provide dual-disc operating systems and high-level language capability along with in-circuit emulation options to speed hardware and software. Also available are 8080 and 8085 breadboard kits.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	2/4 kbytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	64 kbytes
Clock frequency	2.15 MHz
I/O ports, parallel	6 × 8
I/O ports, serial	1 (up to 38,400 baud)
Board size	171.5 × 304.8 mm
	6.75 × 12 in.
Power required (V/I)	5 V/4000 mA
	12 V/90 mA
	−5 V/2 mA
	−12 V/20 mA

Hardware

See page 95 for a complete listing of all boards.



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CIRCLE NUMBER 42

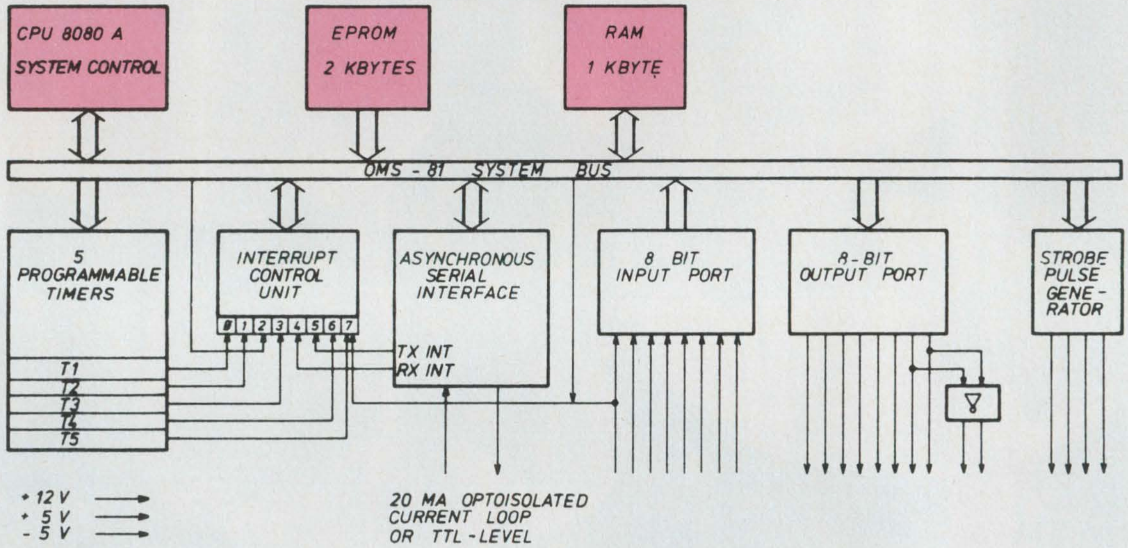
8-bit single-board microcomputer, CPU-81

μP used: 8080A

Alternate sources: None

Kone Oy, Instrument Div.
Ruukintie 18
SF-02320 Espoo 32, Finland
Helsinki 801-7011

The CPU-81 board can either be used by itself, or expanded into a full-sized rack, using standard Europa connectors: A 64-pin connector for the system bus, a 20-pin Elco connector or flat cable for serial, and a 16-pin flat cable for parallel I/O ports. All cards are of single-Eurocard size (100 × 160 mm), and test programs for each are available. Memory includes 1 kbyte of RAM on-board, and sockets for 2 kbytes of EPROM. I/O includes two parallel 8-bit ports and one serial port, five programmable timers and four strobe lines for multiplexed output. Unusual features include an expandable hardware test program and stand-alone minimonitor.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1 kbyte
On-board ROM (min/max)	0/2 kbytes
Addressable memory	32 kbytes
Clock frequency	2 MHz
I/O ports, parallel	1 × 8 in, 1 × 8 out
I/O ports, serial	1 (9600 baud max)
Board size	160 × 100 mm
	6.3 × 3.94 in.
Power required (V/I)	5 V/1000 mA
	12 V/300 mA
	−5 V/100 mA

Comments

I/O includes one 8-bit parallel input port and one 8-bit output port, and an optoisolated serial port with 20-mA current loop, operating at 9600 baud max.

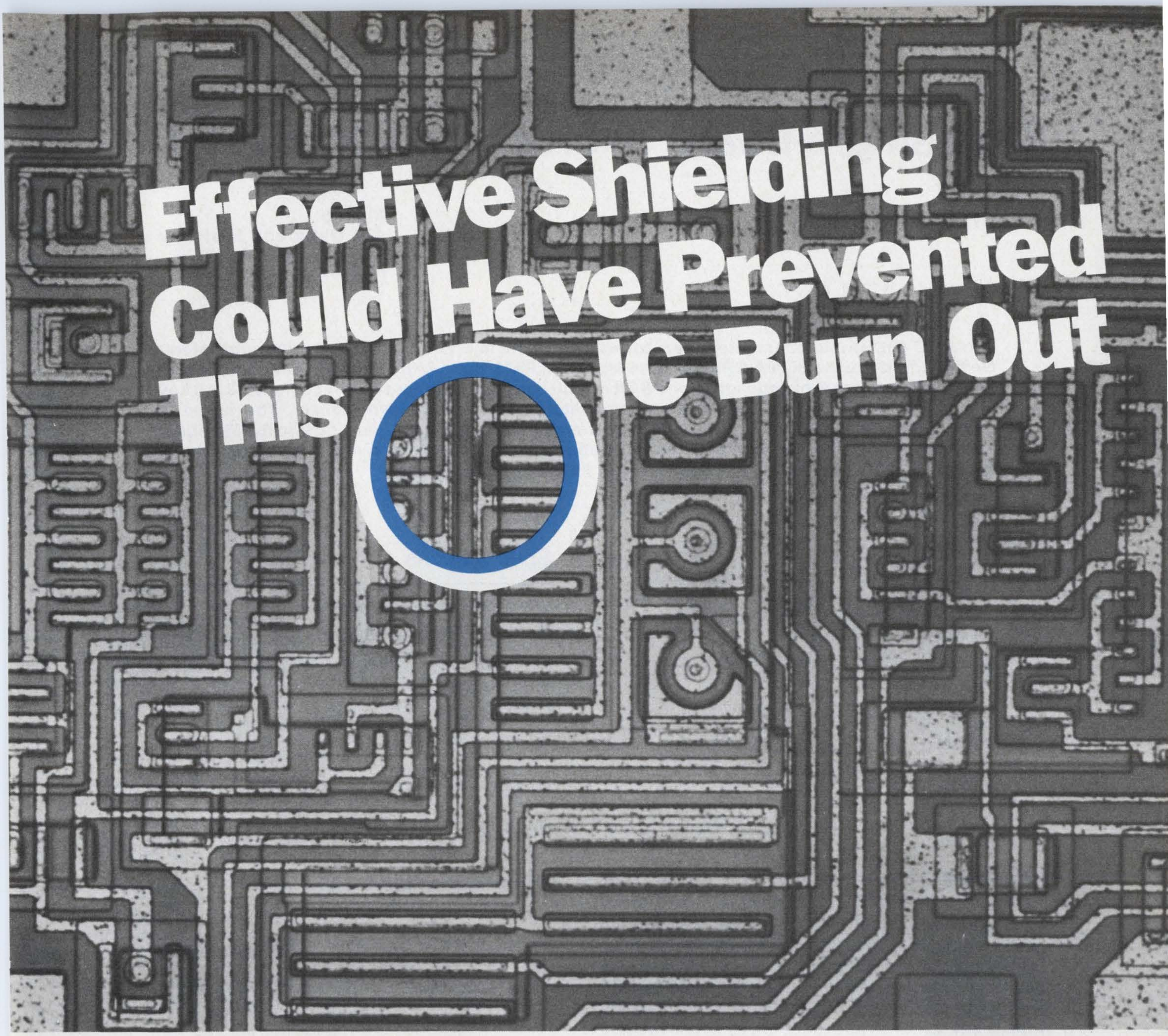
Basic instructions include Data transfer, Arithmetic, Logic, Branch and stack, and I/O and Machine control. Four addressing modes (direct, indirect, register and immediate) are available. Move, Load, and Store instructions operate either on 8 or 16-bit data words. The number of basic instructions totals 78.

Hardware

Model	Description	Price (100-qty)
CPU-81	Basic module	$ 380
MEM-81	Socket board for 8-k EPROM, 2-k RAM	190
SER-81	RS-232C or 20 mA interf.	280
DIO-81	48 prog'ble I/O lines	230
OPTO-01	8-bit isol. output bd.	150
OPTO-02	8+1-bit isol. input bd.	150
RELE-01	8-bit relay output bd.	180
EXIN-01	8-bit isol. interrupts	150
DAC-01	8-bit isol. d/a board	330
ADC-01	8-bit a/d adapter	330
SPI-81	Strip printer interf.	230
CAS-81	C-cassette adapter	290

Hardware support includes, in addition to the listed boards, power supplies, regulators, a keyboard/display unit ($990), and a control panel ($1700) for hardware and software testing.

Software support includes the real-time operating system OMOS-81 (2 kbyte EPROM, 0.5 kbyte RAM) which is shipped free with the system. It accommodates assembly language and PL/M.



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CIRCLE NUMBER 43

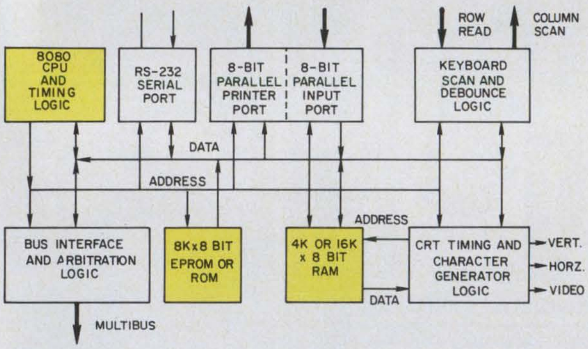
8-bit single-board microcomputer, 80CRT

μP used: 8080A

Alternate sources: None

Mupro
424 Oakmead Parkway
Sunnyvale, CA 94086
(408) 737-0500

The MBC-80CRT microcomputer board forms a complete interactive control/display subsystem. On the board are the 8080A CPU, up to 16 kbytes of RAM, up to 8 kbytes of EPROM, one RS-232 serial I/O port, one 8-bit input port, one 8-bit output port, one keyboard interface (for an 8 × 8 key array) and a CRT interface providing horizontal, vertical and video signals. The board is compatible with the Intel SBC-80 family of microcomputer boards and can plug into the Multibus. The keyboard scanning ports perform key debouncing and N-key rollover. The video terminal section provides an alphanumeric display of 24 lines of 80 characters.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	4/16 kbytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	64 kbytes
Clock frequency (min/max)	2/3.125 MHz
I/O ports, parallel	2 × 8 (one in, one out), dual 8-bit for keyboard
I/O ports, serial	2 (one RS-232 and one video)
Board size	171.5 × 304.8 mm
	6.75 × 12 in.
Power required (V/I)	5 V/2750 mA
	12 V/350 mA
	−12 V/50 mA

Comments

The input and output lines of the MBC-80CRT microcomputer are configured to provide one serial RS-232 port with modem control and programmable baud rate, one parallel 8-bit output port, one parallel 8-bit input port, one 8 × 8 line keyboard interface with N-key rollover and debounce, and one CRT interface with vertical, horizontal and video outputs.

The instruction set is that of the board's 8080A microprocessor. There are 78 basic instructions that are divided into data transfer operations, arithmetic instructions, logic commands, branch and stack operations, and I/O and machine control instructions. There are also four addressing modes—direct, indirect, immediate and register.

Software support for the microcomputer includes a multi-user, multitask disc-based operating system, a high-level text editor, mnemonic and block structured assembly languages, Basic, and an interactive debugger.

Hardware support consists of a complete disc-based development system and a real-time in-circuit emulator in addition to the memory boards listed in the table. Also, since the board is SBC-80 compatible, all Multibus support boards are available to the designer.

Hardware

Model	Description	Price (100 qty)
MBC-80CRT	Micro-computer board	$ 595
MBC-016/P/C	16 k RAM with parity & EC	667/700/956
MBC-032/P/C	32 k RAM with parity & EC	1095/1180/1496
MBC-048/P/C	48 k RAM with parity & EC	1360/1475/1912
MBC-064/P/C	64 k RAM with parity & EC	1695/1870/2337

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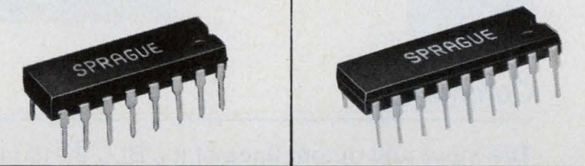
For Engineering Bulletin 29313A and a 'Quick Guide to Interface Circuits', write to: Technical Literature Service, Sprague Electric Company, 347 Marshall Street, North Adams, Mass. 01247.

For the name of your nearest Sprague Semiconductor Distributor, write or call Roger Lemere, Sprague Products Company, North Adams, Mass. 01247. Tel. 413/664-4481.



Type No.	UDN-6116A	UDN-6126A	UDN-6118A	UDN-6128A
No. of Pins	16	16	18	18
Sustaining Voltage	85V	85V	85V	85V
Source Current	40mA	40mA	40mA	40mA
No. of Drivers	6	6	8	8
Input	5V	6-15V	5V	6-15V
Compatible with:	TTL, Schottky TTL, DTL, and CMOS	MOS (PMOS or CMOS)	TTL, Schottky TTL, DTL, and CMOS	MOS (PMOS or CMOS)

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CIRCLE NUMBER 44

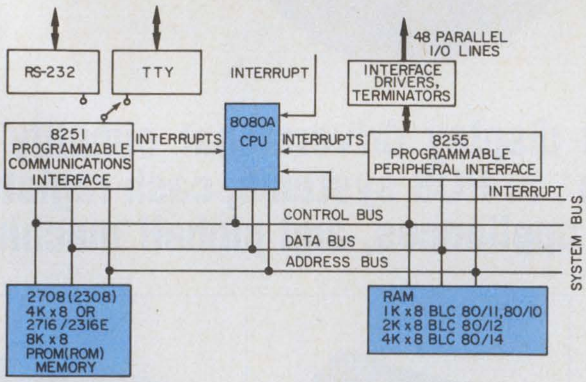
8-bit single-board microcomputer, BLC-80/10

μP used: 8080A

Alternate sources: Iasis, Intel, Monolithic Systems, Mupro

National Semiconductor
2900 Semiconductor Drive
Santa Clara, CA 95051
(408) 737-5000

Although the BLC-80 family of microcomputer boards are basically duplicates of the Intel SBC-80/10 and 10A, they offer the user an alternate source to the family, and thus a little relief in terms of supply. There are four boards in the National family—the BLC-80/10, 11, 12 and 14. The 10 is identical to the Intel 80/10 and can hold only 1 kbyte of RAM and up to 4 kbytes of EPROM (2708 type). The other boards accept either 2708 or 2716 EPROMs, with the 80/11 being the equivalent of the Intel 80/10A. The other boards, though, offer increased RAM capacity over the Intel boards—2 or 4 kbytes of RAM, respectively. Otherwise, they are identical to the 80/10 and 80/11.



Comments

The input and output lines of the BLC-80/10 family consist of 48 programmable parallel lines and one serial port that can act as either an RS-232 or 20 mA current-loop interface. The serial port operates asynchronously at data rates from 75 to 19,200 baud and synchronously at rates up to 38,400 baud. Sockets are available for the software programmable parallel lines so they can be set as inputs, outputs or bidirectional.

The instruction set of the board is that of the 8080A, which contains 78 basic instructions. The commands are divided into five groups: data transfer, arithmetic, logic, branch and stack, and I/O and machine control. There are also four addressing modes—direct, indirect, register and immediate.

Software support for the BLC-80 family of boards includes a 2 kbyte monitor program that permits hardware breakpoints and memory move operations. Also available are user libraries and any 8080A compatible program, as well as all cross software available from time-sharing vendors.

Hardware support includes a wide array of support boards and prototyping packages. Also, since these boards are alternate sources, complete development systems are also available.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1/4 kbytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	64 kbytes
Clock frequency	2.048 MHz
I/O ports, parallel	6 × 8
I/O ports, serial	1 (75 to 38,400 baud)
Board size	171.5 × 304.8 mm
	6.75 × 12 in.
Power required (V/I)	5 V/2900 mA
	12 V/150 mA
	−5 V/2 mA
	−12 V/150 mA

Hardware

See page 105 for a listing of all boards.

Hardware for the BLC-80 family

Model	Description	Price (unit qty)
BLC-80/10	Microcomputer board	$ 445
80/11	Microcomputer board	470
80/12	Microcomputer board	495
80/14	Microcomputer board	570
016	16-kbyte RAM board	784
406	6-kbyte ROM/PROM	315
416	16-kbyte ROM/PROM	266
8432	32 kbyte ROM/PROM & on board programmer	266
104	RAM, ROM, & I/O	679
116	RAM, ROM & I/O	936
501	DMA controller	405
508	Digital I/O expander	315
517	Combo digital & serial I/O	380
711	Analog input	850
724	Analog output	712
732	Combo analog I/O	1069

Model	Description	Price (unit qty)
80P	Prototyping package	878
80P14	Same but includes 80/14	1003
RMC-80/10	Rack-mount computer system	1345
80/14	Same but with CPU	1495
BLC-604	Card cage with backplane	153
614	Expansion card cage	153
635	System power supply	460
660	8-slot cage and supply	1250
665	Heavy-duty supply	700
910	Prototyping system monitor	200

Also available is a wide range of cables and small hardware assemblies, as well as various diagnostic tools and manuals.

Free 1978 Engineering

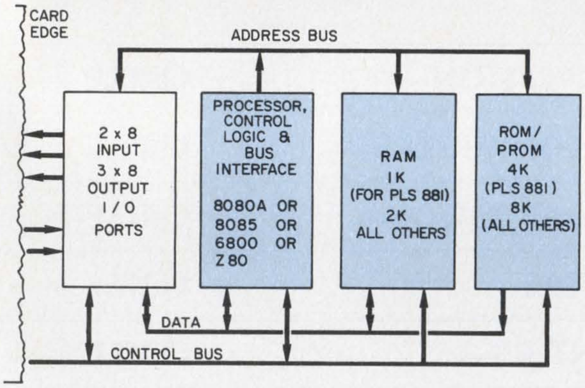
8-bit single-board microcomputers, PLS 800

μP used: 8080A, 8085, Z80 or 6800

Alternate sources: None

Pro-Log
2411 Garden Road
Monterey, CA 93940
(408) 372-4593

The Pro-Log family of 8-bit microcomputer cards consists of five models—the PLS-881, 888, 858, 868 and the 898. Both the 881 and 888 are basically identical, except that the 888 uses the Texas Instruments three supply version of the 2716 PROM instead of the 2708 used on the 881. The 858 is an 8085 based board and is the only one in the family to offer a serial I/O port via the SID and SOD lines of the 8085. The 868 is based on the 6800 μP and the 898 offers the 158 commands of the Z80. None of the boards is intended for expandable systems, although with a few modifications they can be expanded beyond the memory limits of 2 kbytes of RAM and 8 kbytes of ROM/EPROM.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1/2 kbytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	8 kbytes
Clock frequency (min/max)	1/3 MHz
I/O ports, parallel	16 lines in, 24 out
I/O ports, serial	1 (8085 card only)
Board size	114.3 × 165.1 mm
	4.5 × 6.5 in.
Power required (V/I)	5 V/1600 mA*
*Worst case PLS-881	12 V/260 mA*
	−5 V/160 mA*

Comments

The input and output lines of the 8-bit microcomputer cards consist of 16 dedicated input lines, 24 dedicated output lines, all TTL compatible, and on the 858 card a single serial port made from the 8085's SID and SOD I/O lines.

The instruction set of the cards depends on the processors used. The 881 and 888 have the instruction set of the 8080A, the 858 has the 8085 instruction set, the 868 has the 6800's instruction set and the 898 has the Z80 instruction set.

Software support is available from outside sources. There are many vendors of 8080, 8085, 6800 and Z80 software, and programs include assemblers, editors, monitors, debuggers, high-level languages and applications programs.

Hardware support consists of the wide variety of memory and I/O boards as well as the PROM programmers offered by the company. Other vendors also have pin compatible support cards available for many applications. There are also combination equipment packages available to minimize start-up costs.

Hardware

Model	Description	Price (unit qty)
PLS-881	Microcomputer (8080A)	$ 260
PLS-888	Microcomputer (8080A)	295
PLS-858	Microcomputer (8085)	295
PLS-868	Microcomputer (6800)	295
PLS-898	Microcomputer (Z80)	295

There is also a wide family of CPU and support boards that can be used if the system grows beyond the single-board limit. The 8000 family of cards includes 8080 and 8008 CPU cards, RAM and ROM/PROM cards, and I/O and support cards as well as card cages.

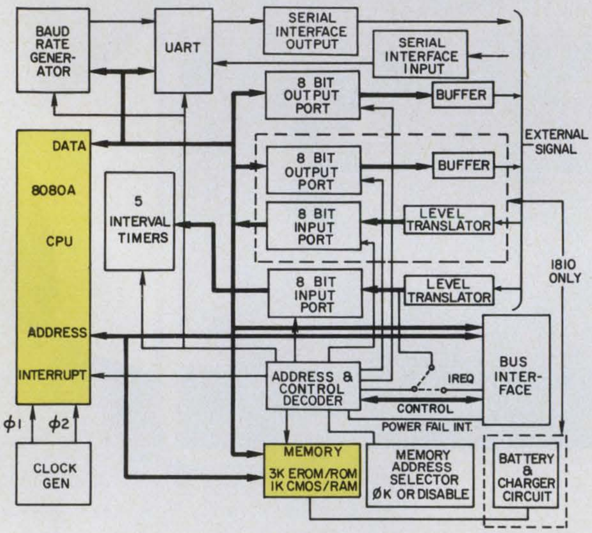
8-bit single-board microcomputers, 1806, 1810

μP used: 8080A

Alternate sources: None

Process Computer Systems
750 North Maple Road
Saline, MI 48176
(313) 429-4971

The PCS 1806 and 1810 are stand-alone microcomputer systems that can also be plugged into a range of chassis (4 to 20 slots) using the Flexibus II backplane. This bus architecture allows memory, I/O, and interface modules to be addressed as memory locations. The starting address for memory on the CPU is selectable. Eight vectored interrupts are controlled by the I/O controller chip. A special CPU reset circuit senses power failures and permits data transfer to battery-backed RAM (on board for the 1810). Parallel I/O consists of eight lines in and eight out for the 1806 and double that for the 1810, serial I/O has 20-mA current loop (or RS-232 for the 1810) with full-duplex operation, optically isolated.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1 k/1 kbytes
On-board ROM (min/max)	0/3 kbytes
1810:	0/7 kbytes
Addressable memory	64 kbytes
Clock frequency	2 MHz
I/O ports, parallel	8 lines in, 8 out
1810:	2 × 8 each in, out
I/O ports, serial	1 (110 to 9600 baud)
Board size	267 × 216 mm
	10.5 × 8.5 in.
Power required (V/I)	5 V/1480 mA
(1810 currents are	12 V/435 mA
approx 100 mA lower)	−5 V/210 mA

Hardware

Model	Description	Price (unit qty)*
1806	μC module	$ 295
1810	μC module w. battery	595
1804	Ac-dc I/O module	335
1805	Gen. purpose I/O	395
1812	CRT/keyboard interface	325
1813	ROM/RAM module	300
1814	CMOS RAM module	495
1820	Multifunction I/O	375
1821	Optically isolated digital input module	265
1823	TTL I/O	285
1825	Optically isolated ac output module	375
1830	Relay output module	295
1850	High-level CMOS a/d (single-ended, d/a)	795
1851	Low level CMOS a/d (single-ended differ.)	750
1860	Quad serial port	595
1890/91	Breadboard kit	125/175
1893	Power fail module	115
	* in 100 qty 30% discount	

Comments

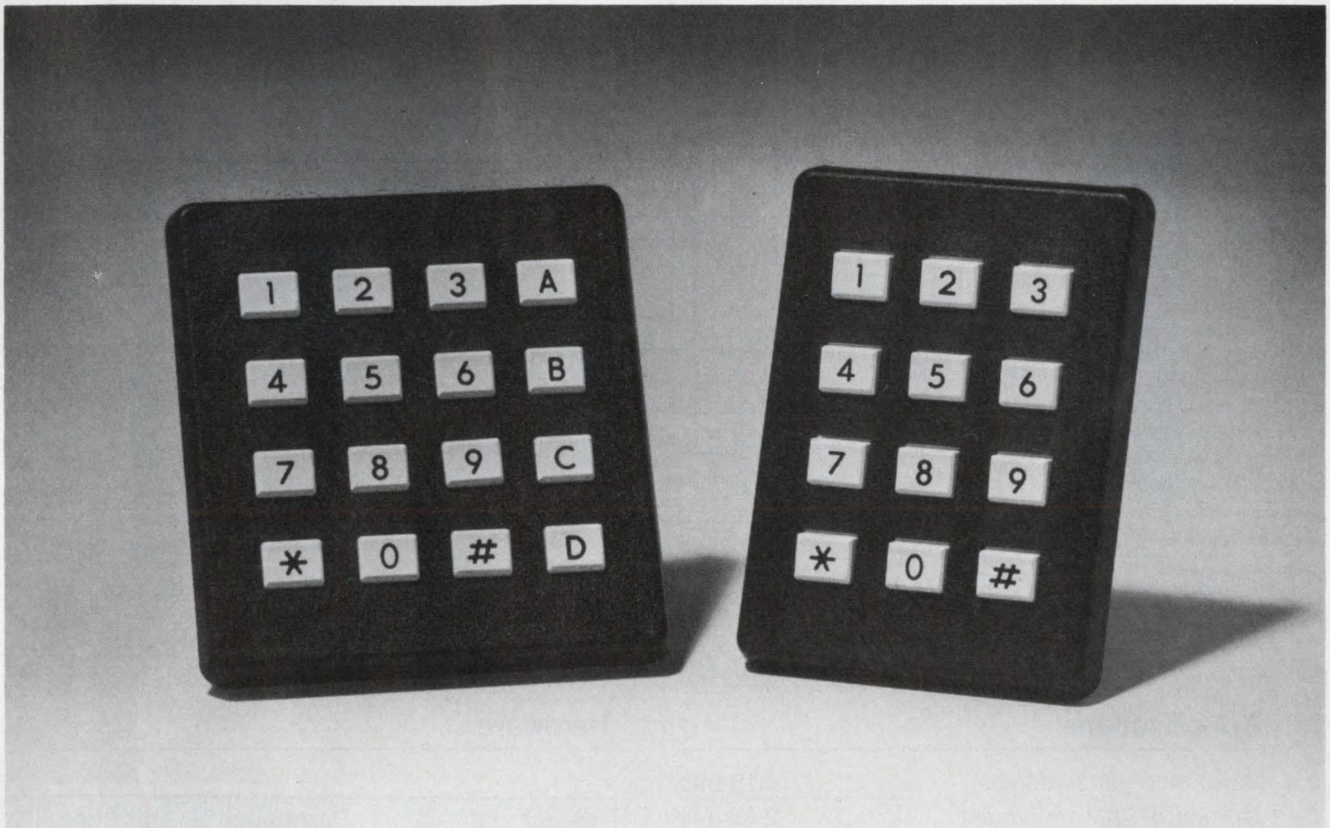
Parallel ports for the 1806 include one input and one output of 8 lines each while the 1810 offers two each. The extra ports of the 1810 are addressed directly as I/O by the CPU, while the first set of ports is under control of the multifunction I/O controller chip. The optically isolated serial transmitter-receiver ports, controlled by the I/O chip, provide communication with a TTY and other peripherals at seven software-controlled baud rates from 110 to 9600. The 8 lines of the data bus are bidirectional (three-state).

The instruction set is divided into five groups: Data transfer, Arithmetic, Logic, Branch and Stack, and I/O and Machine control. The four addressing modes are direct, indirect, register and immediate. The move, load, and store instructions can transfer either 8 or 16-bit data words between memory, the working registers, and the accumulator.

Hardware support includes a wide selection of modules, as well as several chassis (4, 8, 7 and 20 slots) and power supplies. The Superpac 180 microcomputer combines several of the listed boards with a keyboard and display. Two development systems (SPDS and SPDSB) are also available.

Software support includes Protopac (Basic and RTX), SPDS disc-based development system with relocatable macro assembler with Fortran, RTX and Basic as options, and various utility routines (Spur-0,1,2,A,X) as well as an integer and floating-point math library.

Great Tactile Feel



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CIRCLE NUMBER 47

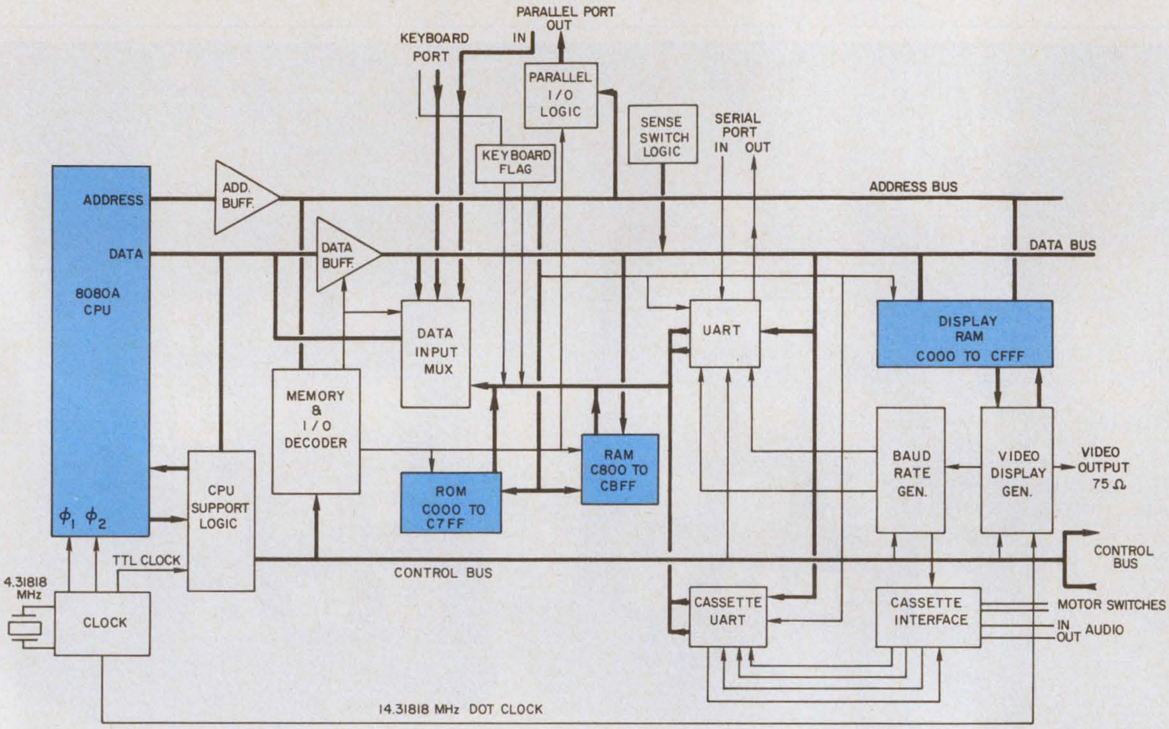
8-bit single-board microcomputer, Sol-PC

μP used: 8080A

Alternate sources: None

Processor Technology Corp.
7100 Johnson Industrial Drive
Pleasanton, CA 94566
(415) 829-2600

The board is offered as the SOL-PC single-board computer, or as the Sol-20 stand-alone computer, in six system configurations. All configurations include the 8080A microprocessor, 1024-character video circuitry, a 2048-byte operating system on preprogrammed ROM chips, audio cassette interface, parallel and serial interfaces, and keyboard interface. The Sol-20 systems also include keyboard, cabinet, power supply and cooling fan.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	2 kbytes
On-board ROM (min/max)	2 kbytes
Addressable memory	60 kbytes
Clock frequency	3.57 MHz
I/O ports, parallel	8 input, 8 output lines
I/O ports, serial	1 (75 to 9600 baud)
Board size	406 × 254 mm
	16 × 10 in.
Power required (V/I)	5 V/2500 mA
	12 V/150 mA
	−12 V/200 mA

Hardware

Model	Description	Price (unit qty)
Sol-PC	Single-board comp.	$ 745
2KRO	Erasable PROM module	89
4KRA	Low-power stat. RAM	150
BOOTLOAD	Personality module	100
GPM	1 k RAM, 1 k (P)ROM	169
8KRA	8-k static RAM	250
16KRA	16-k dynamic RAM	399
3P+S	Par./ser. I/O module	199

Comments

The input and output lines can be tied for bidirectional operation. Seven lines are available for control and handshake. The serial interface can be configured as RS-232C or 20-mA current loop.

The instruction set contains five groups: data transfer, arithmetic, logic, branch and stack, I/O, and machine control for a total of 78 basic commands. Addressing modes are direct, indirect, register and immediate.

Available hardware includes, in addition to the listed items, an upgrade kit (cabinet, keyboard, fan, power supply and backplane extension) that converts the Sol-PC to a Sol-20 ($675), as well as a wrapped-wire module, extender board, video display module ($295), and peripherals.

Software support includes Basic/5 (cassette), Extended Basic, Focal, Mathpack, a resident assembler, simulator, and text editor cassette, disc operating systems, and disc Basic.

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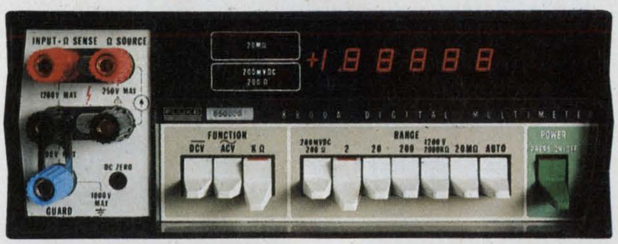

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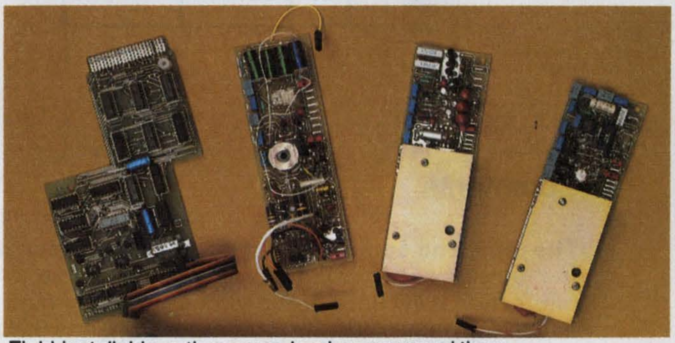

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CIRCLE NUMBER 49

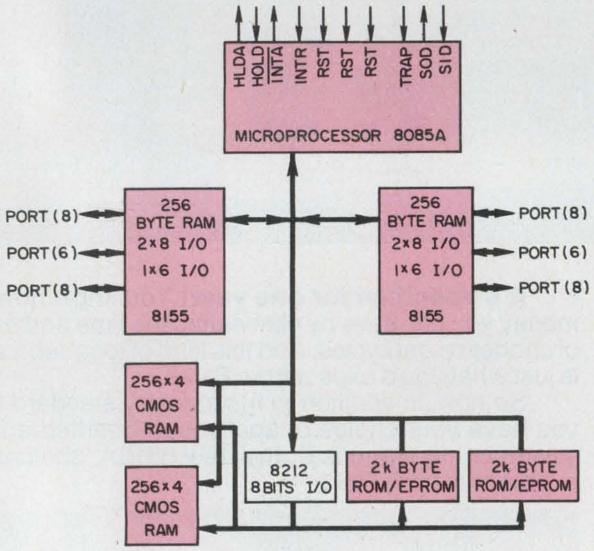
8-bit single-board microcomputer, SKC 85

μP used: 8085A

Alternate sources: None

Advanced Micro Computer
3330 Scott Blvd.
Santa Clara, CA 95051
(408) 732-2400

A complete single-board computer system, the SKC 85 holds up to 4 kbytes of EPROM and up to 1.25 kbytes of static RAM, of which 256 bytes are CMOS and have a battery back up. The board has four interrupts with fixed restart addresses, two 14-bit timers, a serial I/O interface, 44 bidirectional I/O lines, and can operate from a 5 V supply. The board has a 96-pin interface bus, with no unused pins.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	512/1280 bytes
On-board ROM (min/max)	0/4 kbytes
Addressable memory	64 kbytes
Clock frequency	3 MHz
I/O ports, parallel	4 × 8 & 2 × 6
I/O ports, serial	1 (uses SID/SOD lines)
Board size	100 × 160 mm
	3.9 × 6.3 in.
Power required (V/I)	5 V/600 mA

Hardware

Model	Description	Price (100 qty)
SKC 85	Single-board computer	$ 408
—	Operators panel	N/A

Comments

The input and output lines of the SKC 85 consist of the ports on two 8155 I/O chips. There are 44 bidirectional I/O lines grouped in four sets of eight and two groups of six. The processor's SID and SOD lines are used for a serial communications port. All parallel and serial lines are software programmable. The serial interface can be configured for either RS-232 or TTY compatibility.

The instruction set of the 8085A based board contains five basic groups of commands: Data transfer, arithmetic, logic, branch and stack, I/O and Machine control. There are a total of 80 commands, two more than those of the 8080A. All 8080A software can run on the 8085A. Addressing modes include direct, indirect, register and immediate.

Available hardware includes an 8080A-based CPU only card, the SMP 80. All standard peripherals can be interfaced to the SKC 85 via the I/O ports or the control bus.

Software support for the board includes the MON 1, a monitor program. Since the board is 8080A and 8085A software compatible, any program written for either processor can be used.

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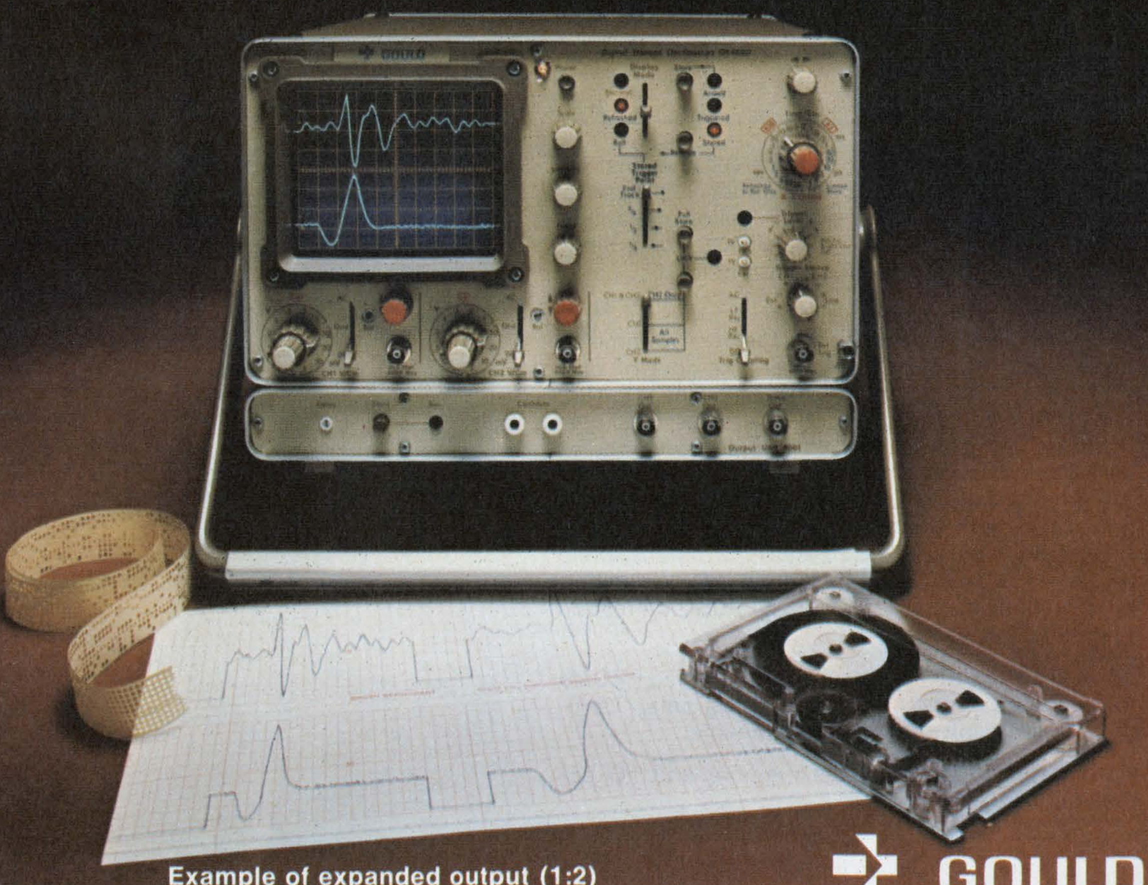
For brochure call toll free (800) 325-6400. Ext. 77. In Missouri: (800) 324-6600.



Example of expanded output (1:2)

GOULD

CIRCLE NUMBER 50

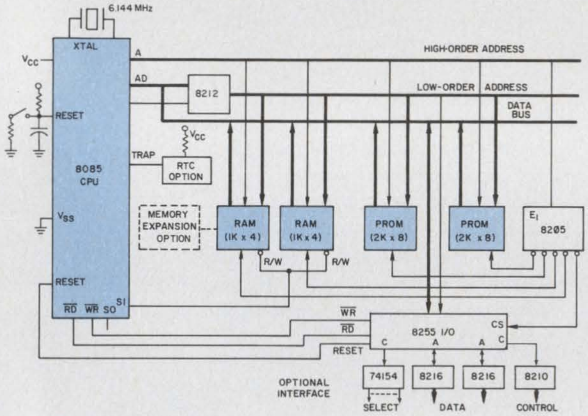
8-bit single-board microcomputer, ASC/80

μP used: 8085 (Z80 optional)

Alternate sources: None

Applied Systems Corp.
26401 Harper
St. Clair Shores, MI 48081
(313) 779-8700

With both RAM and ROM on board, the ASC/80 can function as a stand-alone computer, but also offers optional expansion capability to add external memory, more I/O, and peripheral interfaces. Sixteen (32 optional) parallel I/O lines are programmable (in groups of four) as inputs or outputs. All have three-state capability, and are optionally either MOS or TTL compatible. A serial I/O line works at speeds from 110 to 9600 baud. On-board RAM is 256 bytes, expandable to 1 k, and sockets for up to 4 k of RAM are provided. Preprogrammed PROMs for executive and emulation software as well as communications programs and custom software are offered.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	256/1024 bytes
On-board ROM (min/max)	0/4 kbytes
Addressable memory	64 kbytes
Clock frequency	5 MHz
I/O ports, parallel	4 × 4 (32 opt.)
I/O ports, serial	1 (110 to 9600 baud)
Board size	168 × 114 mm
	6 × 4.5 in.
Power required (V/I)	5 V/500 mA

Comments

Parallel I/O includes 16 (optionally 32) lines that are programmable as inputs or outputs in groups of four. All parallel I/O lines have three-state capability, and can be provided either TTL or MOS-compatible. The serial I/O port operates from 110 to 9600 baud.

The instruction set of the 8085 includes all 78 of the 8080 instructions (data transfer, arithmetic, logic, branch/stack, I/O, and machine control) plus RIM (read interrupt mask) and SIM (set interrupt mask). RIM and SIM are used to provide maskable vectored interrupts. The Z-80 version also includes all 8080 op codes, plus 80 more. Twelve of these are general-purpose arithmetic commands, and 28 arithmetic-logic commands (17 for 8-bit, 11 for 16-bit operations). There are 20 load instructions, while 12 serve I/O operations. Exchange, block transfer, bit-set, shift/rotate, jump, and call/return commands complete the set.

Software support includes preprogrammed PROMs for executive and emulation programs. Communications software is also available.

Hardware support includes memory and I/O extension boards.

Hardware

Model	Description	Price (100 qty)
ASC/80	8085 CPU board	$ 199
ASC/Z80	Z-80 CPU board	199
4RM	4-k static RAM	99
4PM	4-k PROM	99
2410	Parallel I/O board	85
8SI	Serial I/O (1 port)	85

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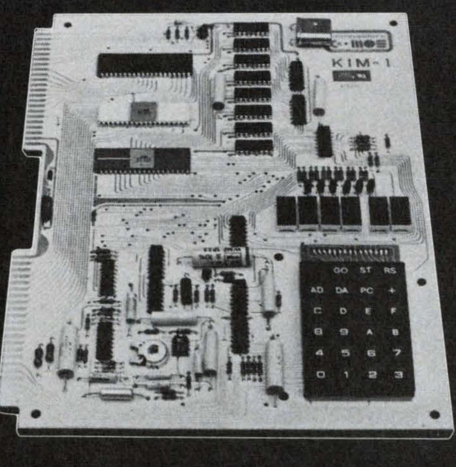

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901 California Avenue
Palo Alto, CA 94304
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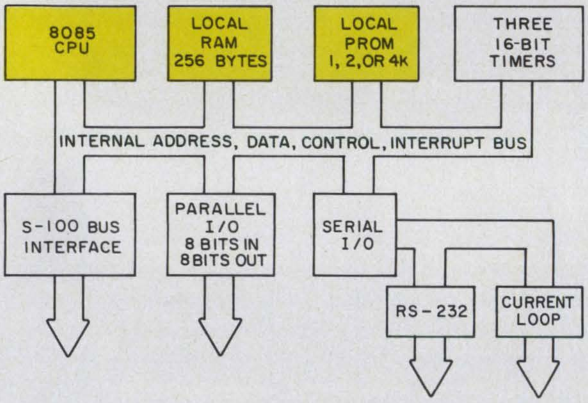
8-bit single-board microcomputer, MPU-B

μP used: 8085A

Alternate sources: None

Imsai Manufacturing
14860 Wicks Blvd.
San Leandro, CA 94577
(415) 483-2093

The MPU-B single-board microcomputer system is an S-100 bus compatible board that can operate as a stand-alone computer. On the board are 256 bytes of RAM, space for up to 4 kbytes of ROM or EPROM, three 16-bit timers, 16 bits of parallel I/O and a serial port capable of either RS-232 or 20 mA current-loop operation. The serial port is software controllable and is capable of asynchronous, synchronous and Bisync operation.



Comments

The input and output lines of the MPU-B are set up as eight dedicated input lines, eight dedicated output lines, and a software programmable serial port, jumper strappable as either an RS-232 or 20 mA current-loop interface. The serial port operates in synchronous, asynchronous or Bisync modes at data rates from 500 to 56,000 baud. Word size, parity, and stop bits are programmable.

The instruction set of the board follows that of its 8085 processor. There are 80 basic commands, 78 of which duplicate 8080A instructions. The new commands include RIM (read interrupt mask) and SIM (set interrupt mask), and provide the 8085 with four levels of vectored interrupt.

Software support consists of a wide range of programs including a disc-operating system (IMDOS) that supports 18 drives and is a superset of Intel's CP/M. There are also many utility routines, assemblers, eight versions of Basic, a version of Fortran IV, and a language called ISAM, soon to be delivered by Imsai.

Hardware support for the MPU-B includes the boards listed on the table and many more S-100 bus compatible products including cabinets, motherboards, front panels, and over 50 other vendors of S-100 support boards.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	256 bytes
On-board ROM (min/max)	2/4 kbytes
Addressable memory	64 kbytes
Clock frequency	3 MHz
I/O ports, parallel	2 × 8 (one input, one output)
I/O ports, serial	1 (0.5 to 56,000 baud)
Board size	133.4 × 254 mm
	5.25 × 10 in.
Power required (V/I)	8 V/1400 mA *
	−16 V/100 mA *

* on-board regulators are used.

Hardware

Model	Description	Price (unit qty)
MPU-B	Microcomputer board	$ 325
RAM-16	16 kbyte RAM	499
RAM-32	32 kbyte RAM	799
RAM-65	64 kbyte RAM	2649
SIO-2-2	Dual serial I/O board	299
PIO-4-4	Quad PIO board (64 lines)	299
MIO	Combo parallel, serial, cassette	350
DIO	Floppy-disc controller	799
Model 40	Teletype 300 lpm printer	3656
PCS80/15	Card cage with supply & CPU	799

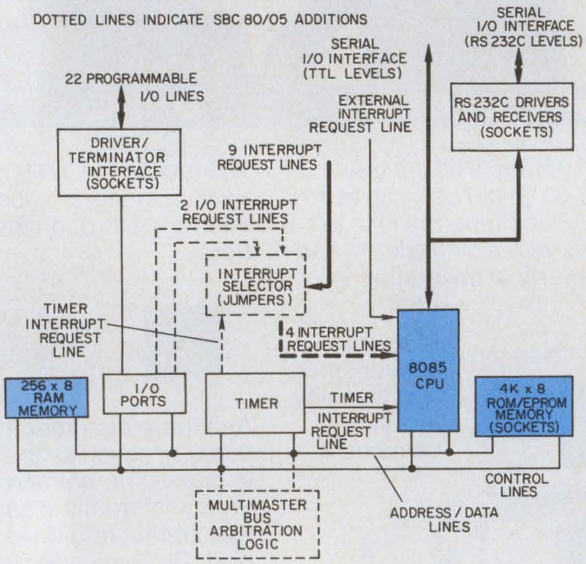
8-bit single-board microcomputer, 80/04, 05

μP used: 8085A

Alternate sources: None

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
(408) 987-8080

The SBC-80/04 and 05 single-board microcomputers are complete systems. The 04 is intended for stand-alone applications and does not have an interface to the Intel Multibus. The 05 has the interface and some additional interrupt control logic. Both boards use the 8085A processor and have 256 and 512 bytes of static RAM, respectively. Both boards are limited to 22 programmable parallel I/O lines and a TTL-compatible serial interface created by the SID and SOD lines of the processor. Able to operate from just a 5 V supply, both boards have a programmable 14-bit timer and can hold up to 4 kbytes of ROM/EPROM.



Specifications

Word size (data/address)	8/16 bits
On-board RAM	256/512 bytes (04 & 05, resp.)
On-board ROM (min/max)	2/4 kbytes
Addressable memory	4.25 kbytes (04)
	64 kbytes (05)
Clock frequency	1.966 MHz
I/O ports, parallel	2 × 8 and 1 × 6
I/O ports, serial	1 (up to 4800 baud)
Board size	171.5 × 199.4 mm (04)
	171.5 × 304.8 mm (05)
	6.75 × 7.85 in. (04)
	6.75 × 12 in. (05)
Power required	5 V/600 mA (04) 5 V/1800 mA (05)

Comments

Input and output lines of the SBC-80/04 and 05 are divided as follows: 22 parallel lines from an 8155 that are software programmable and arranged in two groups of eight and one group of six, and one serial port formed by the processors' SID and SOD lines. Also included is the programmable 14-bit timer.

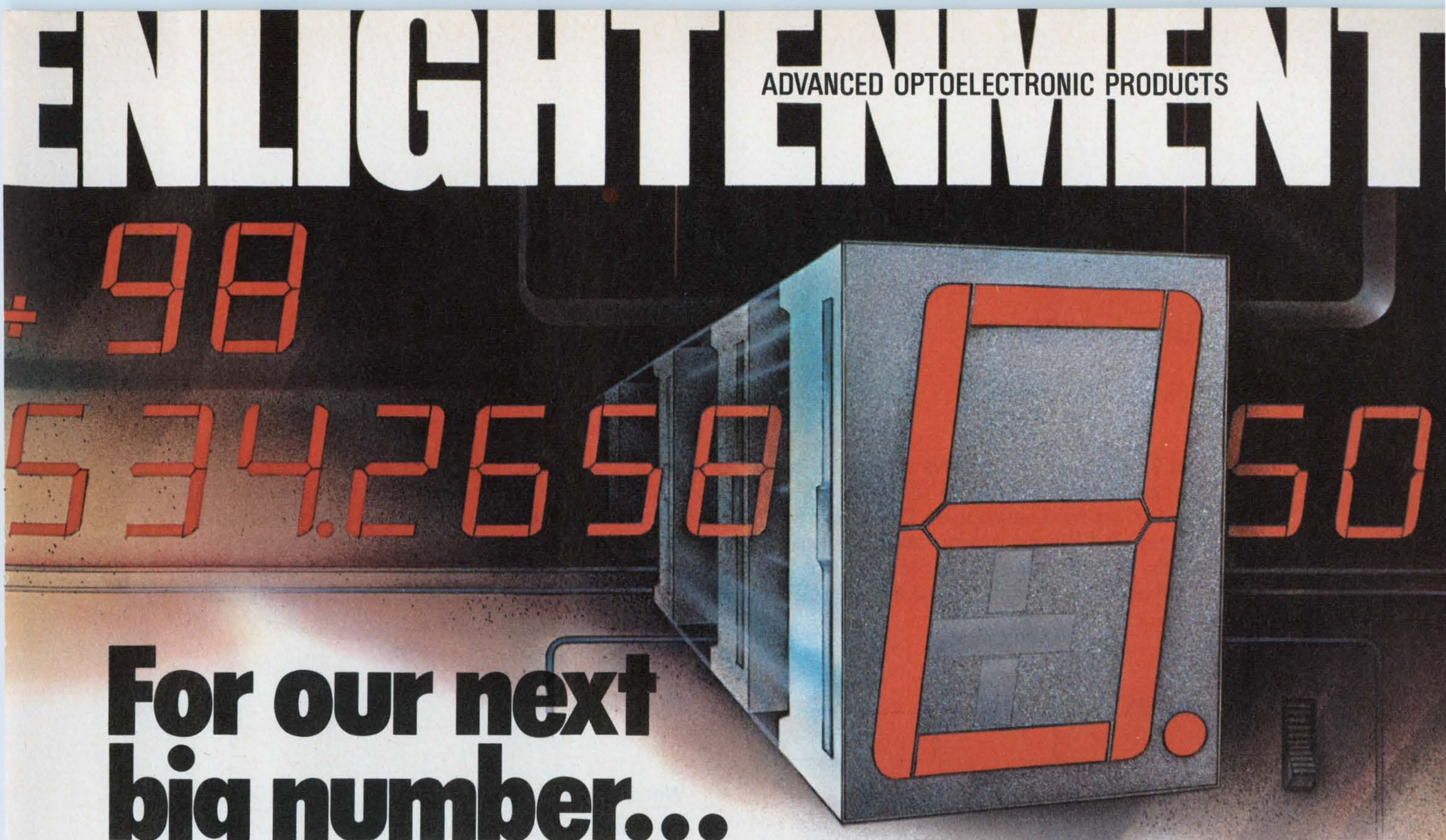
The instruction set of the 8085 based boards consists of the 78 instructions for the 8080A and the two new commands for setting and reading the interrupt mask, RIM and SIM. The 78 basic commands are divided into five groups: data transfer, arithmetic, logic, branch and stack, and I/O and machine control. There are also four addressing modes—direct, indirect, register and immediate.

Software support for the SBC-80 family of boards includes a wide library of user routines and, depending on the complexity of the system, the RMX-80 Real-time Multitasking Executive package ($1950) or the ISIS operating systems in the MDS development systems. Much cross-software is also available from many of the time-sharing vendors.

Hardware

See page 95 for a complete listing of all boards.

Hardware support includes complete development systems such as the MDS and the Series II. These systems provide dual disc operating systems and high-level language capability along with in-circuit emulation options to speed hardware and software design. Also available are card cages, power supplies, complete packaged systems, and cables.



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CIRCLE NUMBER 53

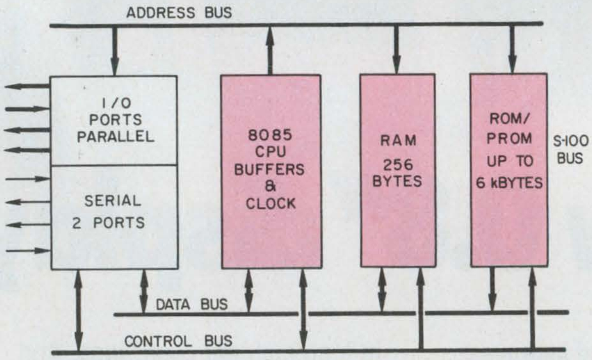
8-bit single-board microcomputer, 8085 CPU

μP used: 8085

Alternate sources: None

Space Byte
1720 Pontius Avenue, Suite 201
West Los Angeles, CA 90025
(213) 468-8080

The 8085 CPU single board computer system contains an 8085 microprocessor and all the I/O necessary to support a disc-based computer system. On the card are 256 bytes of RAM, space for up to 6 kbytes of EPROM, two RS-232 serial ports with software selectable baud rates, one 14-bit programmable counter/timer, four levels of vectored interrupt, 24 parallel I/O lines with handshake logic and the interface logic for the S-100 microcomputer bus. The EPROM sockets on the board are jumper selectable for use with either 2708 or 2716 EPROMs.



Comments

The input and output lines of the CPU card are set up as eight parallel input lines, 16 parallel output lines, six handshake signal lines, and two serial RS-232 ports. There are also the S-100 bus interface lines for system expansion and control. Both RS-232 serial ports are software programmable for baud rate and asynchronous or synchronous operation.

The instruction set is that of the boards' 8085 processor and contains 80 basic commands, 78 of which are those of the 8080A. The new instructions —set interrupt mask (SIM) and read interrupt mask (RIM) are used to implement the five levels of interrupt capability built into the 8085.

Software support for the microcomputer card includes a monitor program in 3 kbytes of PROM. On the PROMs are the disc bootstrap, I/O routines and utilities. Disc operating systems include FDOS-III and CP/M. Also available is a disc version of extended Basic (DEBBI) from ICOM along with its floppy-disc system, and from Microsoft a version of Fortran IV that operates in conjunction the CP/M package.

Hardware support consists of a floppy-disc operating system as well as all commonly available S-100 bus-compatible products.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	256 bytes
On-board ROM (min/max)	0/6 kbytes
Addressable memory	64 kbytes
Clock frequency	3 MHz
I/O ports, parallel	24 lines and handshake logic
I/O ports, serial	2 (programmable)
Board size	135 × 254 mm
	5.375 × 10 in.
Power required (V/I)	8 V/430 mA
	16 V/110 mA
	−16 V/120 mA

Hardware

Model	Description	Price (unit qty)
8085 CPU	Microcomputer board	$ 499
16 k RAM	16 kbyte static RAM card	599
N/A	EPROM programmer	399

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CIRCLE NUMBER 54

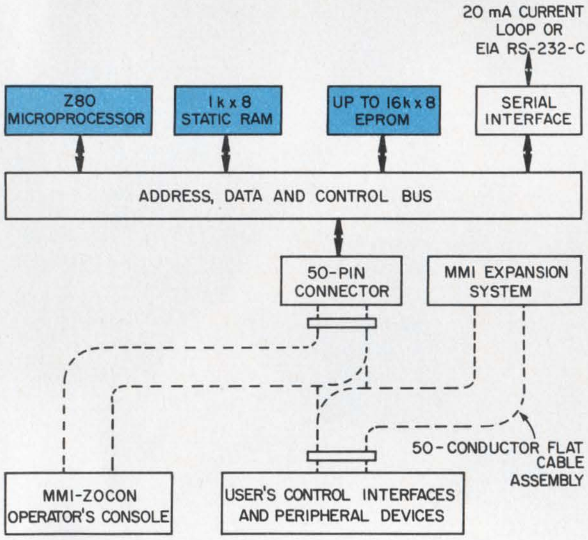
8-bit single-board microcomputer, CSS-1143

μP used: Z80

Control Logic
Nine Tech Circle
Natick, MA 01760
(617) 655-1170

Alternate sources: None

The CSS-1143 single-board computer provides a stand-alone solution to many applications. On the board are a Z80 CPU, 1 kbyte of static RAM, up to 16 kbytes of EPROM, an asynchronous serial interface capable of RS-232 or 20 mA current loop operation and an interface compatible with the company's Poly-bus used in the MM1 family of microcomputers.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1 kbyte
On-board ROM (min/max)	0/16 kbytes
Addressable memory	64 kbytes
Clock frequency	2 MHz
I/O ports, parallel	0
I/O ports, serial	1 (110 baud)
Board size	406.4 × 203.2 mm
	16 × 8 in.
Power required (V/I)	5 V/1700 mA
	+12 V/525 mA
	−12 V/450 mA

Comments

Input and output lines of the CSS-1143 microcomputer consist of an RS-232 or 20 mA current-loop interface factory set for 110 baud and a 50-pin port with a subset of the company's Poly-bus interface. A board with selectable baud rates will be available shortly.

The instruction set is that of the board's Z80 microprocessor and contains 158 commands, 78 of which are those of the 8080A. In all, there are 41 8 and 16-bit load commands, 14 exchange, block transfer, and search instructions, 40 arithmetic and logic operations, 16 shift and rotate commands, nine bit set, reset, and test operations, 11 jump instructions, seven call and return directions, and 12 I/O commands.

Hardware

Model	Description	Price (unit qty)
CSC-1143	Microcomputer board	$ 500
MM1-ZOCON	Operators console	650
	All boards in the MM1 family	See p. 126

Hardware support consists of an operator's console for programming, and most of the modules in the company's MM1 microcomputer family.

Software support includes utility programs, assemblers, editors, debuggers, loaders and operating system. Also available is a disc operating system and a Fortran compiler. For users, the CLUB (Control Logic Users Brigade) program library contains mathematical and conversion routines, cross assemblers, and other utility programs.

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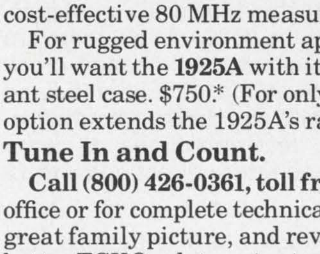

1925A

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CIRCLE NUMBER 55 FOR LITERATURE

CIRCLE NUMBER 56 FOR DEMONSTRATION

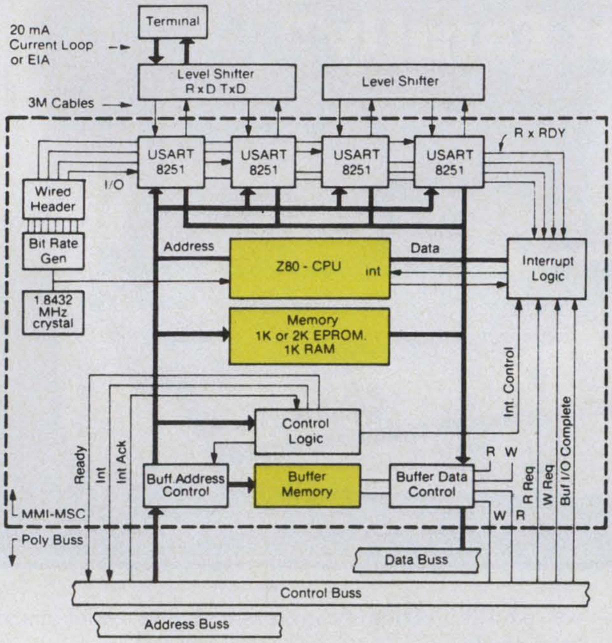
8-bit single-board microcomputer, MM1-MSC

μP used: Z80

Alternate sources: None

Control Logic
Nine Tech Circle
Natick, MA 01760
(617) 655-1170

The MM1-MSC single-board microcomputer contains a Z80 CPU along with up to 2 kbytes of EPROM and 1280 bytes of RAM. There are four serial I/O ports, each of which can operate synchronously at rates to 50 kbaud or asynchronously at data rates of 110 to 9600 baud. A priority-interrupt controller provides interrupts from all four ports as well as from three external interrupt inputs. The on-board RAM consists of a 1 kbyte CPU scratchpad/data storage area and a 256 byte buffer memory used for data and command transfer between the MM1-MSC and another CPU.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1280 bytes
On-board ROM (min/max)	0/2 kbytes
Addressable memory	64 kbytes
Clock frequency	1.8432 MHz
I/O ports, parallel	0
I/O ports, serial	4 (110 to 50,000 baud)
Board size	254 × 177.8 mm
	10 × 7 in.
Power required (V/I)	5 V/2275 mA
	12 V/50 mA
	–5 V/75 mA

Hardware

Model	Description	Price (unit qty)
MM1-MSC	Microcomputer board (Z80)	$ 950
MM1-ACPU	Microcomputer board (8080A)	300
MM1-ZCPU	Microcomputer board (Z80A)	350
MM1-RAM	4 kbyte static RAM (1 k inc.)	200
MML-R/VRAM	4 kbyte nonvolatile RAM (inc. 1 k)	660
MML-DRAM	16 kbyte dynamic RAM (inc. 4 k)	430
MM1-PROM	16 k PROM board (no PROMs)	190
MM1-DIO	Digital I/O board	235
MM1-DAS	12-bit a/d converter	1295
MML-AOS	12-bit d/a (four outputs)	1075
MM1-OPT	Clock, serial I/O & digital I/O	250
MM1-MONS	Monitor Start (Z80 or 8080A)	150
MM1-OCON	Operator console (Z80 or 8080A)	650
MM1-PCON	Programmer console (8080A)	1500
MML-BTE	Bus Terminator	125
PFD	Power fail detect	130
MM1-ENC-DT	Desk top enclosure	725
MM1-ENC-RM	Card cage with supply (rack)	625

Comments

Input and output lines of the MM1-MSC consist of just four serial ports. Each port accepts and delivers TTL level signals in either asynchronous or synchronous modes, operating at 110 to 9600 baud and up to 50 kbaud, respectively. There are three interrupt inputs in addition to the four serial I/O interrupts.

The instruction set is that of the board's Z80 microprocessor and contains 158 basic commands, 78 of which are those of the 8080A. In all, there are 41 8 and 16-bit load commands, 14 exchange, block transfer and search instructions, 40 arithmetic and logic operations, 16 shift and rotate commands, nine bit set, reset and test operations, 11 jump operations, seven call and return directions and 12 I/O operations.

Software support includes utility programs, assemblers, editors, debuggers, loaders and operating systems. Also available is a disc operating system and a Fortran compiler. For users, the CLUB (Control Logic User Brigade) program library contains mathematical and conversion routines, cross assemblers, and other utility programs.

Hardware support consists of the various boards listed in the table and a family of 12 development systems, providing various levels of design support. Terminals, printers, paper tape reader/punches, PROM programmers and disc systems are available.

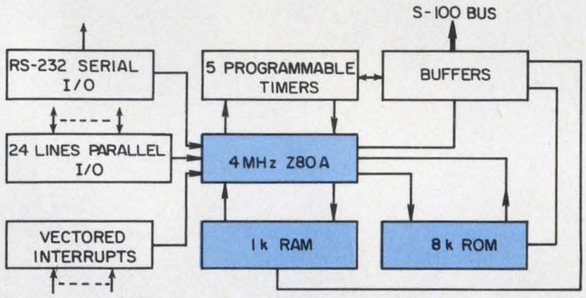
8-bit single-board microcomputer, SCC-W

μP used: Z80A

Alternate sources: None

Cromemco
2400 Charleston Rd.
Mountain View, CA 94043
(415) 964-7400

The SCC-W single-card computer system, based on the Z80A microprocessor, operates at a 4 MHz clock rate and is compatible with the S-100 bus. On the card are 1024 bytes of RAM, space for up to 8 kbytes of ROM or EPROM, 24 bidirectional parallel I/O lines, and an RS-232 or 20 mA current loop serial I/O port. The serial channel can be software controlled for baud rates from 110 to 76,800 baud.



Comments

The input and output lines of the microcomputer are structured such that there are 24 bidirectional parallel lines and one serial port that can be configured for either an RS-232 or 20 mA current-loop interface capable of operation at software-programmable data rates from 110 to 76,800 baud. Parallel I/O lines can drive 20 TTL loads.

The instruction set is that of the board's Z80A microprocessor. There are 158 basic instructions, of which 78 are those of the 8080A. Of the 158 commands, there are 41 8 and 16-bit load instructions, 14 exchange, block transfer and search operations, 40 arithmetic and logic commands, 16 shift and rotate instructions, 21 bit and I/O operations, and 11 jump commands.

Software support consists of ROM-based monitors and assemblers, a 3 kbyte Basic and a 16 kbyte Basic. Available on disc are a macro-assembler, a disc operating system, extended disc Basic and Fortran IV. Of course, most available 8080A and Z80 programs can run on the board and many time-sharing vendors offer various cross software programs for program development and debugging.

Hardware support consists of a wide array of S-100 compatible boards offered by the company as well as a cabinet and full disc-based system. Also, many of the over 50 companies that have S-100 boards offer compatible products for the microcomputer.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1024 bytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	64 kbytes
Clock frequency	4 MHz
I/O ports, parallel	24 lines (programmable)
I/O ports, serial	1 (110 to 76,800 baud)
Board size	135 × 254 mm
	5.375 × 10 in.
Power required (V/I)	8 V/1000 mA*
	18 V/100 mA*
	−18 V/100 mA*

*Unregulated supply voltages

Hardware

Model	Description	Price (100 qty)
SCC-W	Microcomputer board	$ 450
4KZ-W	4 kbyte RAM card	295
16KZ-W	16 kbyte RAM card	795
8KBS-W	8 k ROM/2708 programmer	245
32KBS-W	32 k ROM/2716 programmer	295
4FDC-W	Floppy-disc controller	595
D+7A-W	7 channel a/d & d/a card	245
16KPR-W	16 k ROM card	245
CGI-W	Color graphics interface	350
MCB-216	Monitor and Basic in ROM	90

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Cost-effective

design, manufacturing, and implementation makes the PCS 1880 and other PCS products possible.

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8-bit single-board microcomputer, BC1-1

μP used: Z80A

Dynabyte
4020 Fabian
Palo Alto, CA 94303
(415) 494-7817

Alternate sources: None

The BC1-1, otherwise known as the Basic Controller, not only provides the user with a complete microcomputer system, but some output relays as well. On the board is a Z80-based microcomputer with a minimum of 4 kbytes of dynamic RAM (expandable to 16 k), two slots for 2 kbyte EPROMs, a PROM programmer, four slots for an additional 8 kbytes of ROM, 32 TTL-level output lines, 32 TTL-level input lines, a cassette recorder interface, four 0.75-A reed relays, four 5-A, 115-V general-purpose relays, a composite video output for a 64 character × 16 line video display, and two more parallel I/O ports (8 bits in and 8 bits out).

Comments

The input and output lines of the Basic Controller consist of 32 TTL-level input lines, 32 TTL level output lines, a cassette interface with motor control capability, two serial I/O ports (one is RS-232 only and the other is jumper settable as TTY or RS-232), a composite video output delivering a 64 character × 16 line display, eight relay outputs and two byte-oriented ports, one as an input and one as an output. Also included on the board are eight user-definable indicator LEDs and another eight LEDs usable as a port data display.

The instruction set of the Z80 microprocessor is available to users. There are 158 basic commands in the instruction set, and 78 of them are code compatible with the 8080A instruction set. The commands include 21 8-bit load directives, 20 16-bit load instructions, 14 exchange, block transfer and search operations, 40 arithmetic and logic operations, 16 shift and rotate commands, 21 bit and I/O operations, and 11 jump instructions.

Software support for the board is available in ROM form as ZIBL, an industrial version of Basic developed by Dynabyte. The software is designed for control applications and can perform single bit control of the input and output lines. Also, since the board uses a Z80, most 8080A or Z80 software can be used.

Hardware support for the board consists of just the power supply, cover panel and expansion chip sets. Additional support boards are in design and should be available in the near future. Cable sets will also be available shortly.

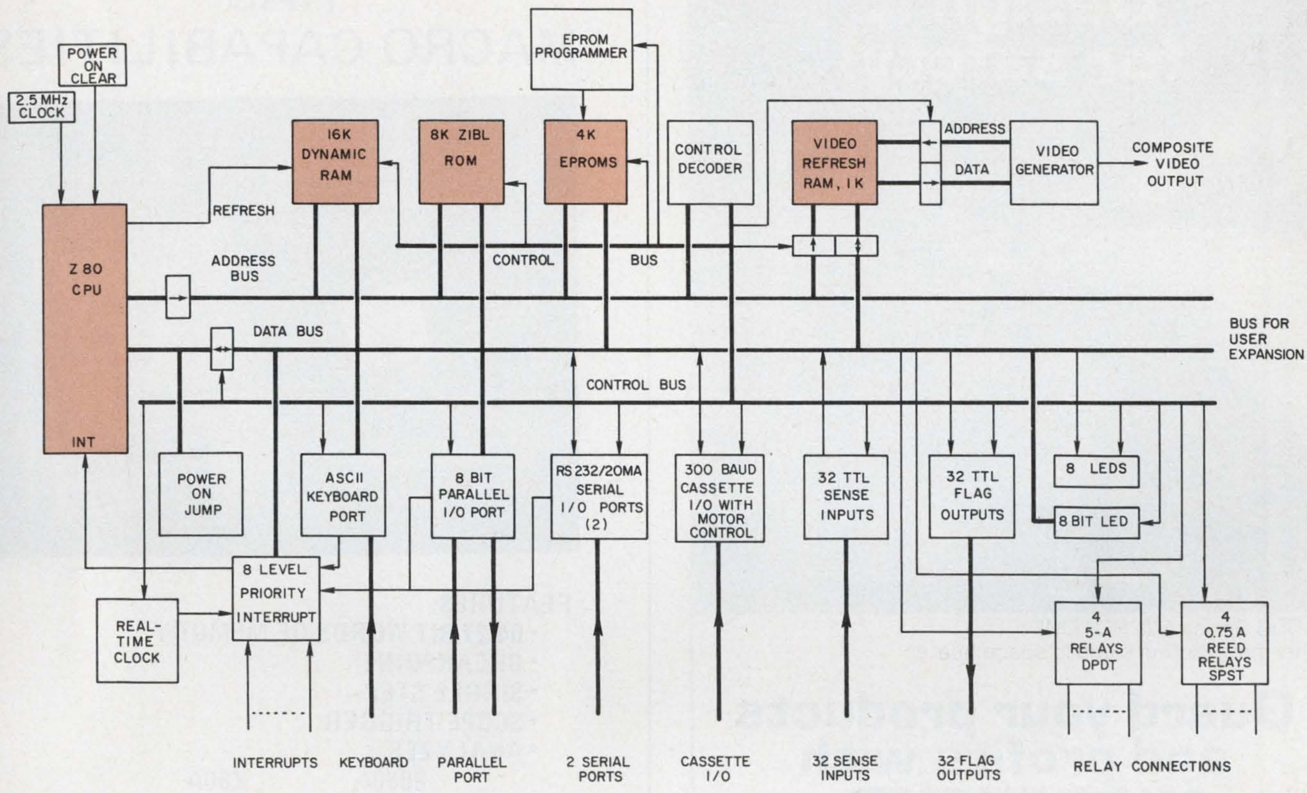
Note: For board architecture, see page 131.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	4/16 kbytes
On-board ROM (min/max)	0/12 kbytes
Addressable memory	64 kbytes
Clock frequency	2.5 MHz
I/O ports, parallel	1 × 8 plus 32 lines and eight relay outputs
I/O ports, serial	2 (RS-232, TTY) plus a video output
Board size	375.9 × 315 mm
	14.8 × 12.4 in.
Power required (V/I)	5 V/3000 mA
	+12 V/100 mA
	−5 V/2 mA
	28 V/60 mA

Hardware

Model	Description	Price (unit qty)
BC1-1	Microcomputer board	$ 750
BC1-X1	Power supply	50
BC1-X2	Translucent cover	15
BC1-X3	4 kbyte expansion RAM	110
BC1-X4	2 kbyte EPROM	55



POWER ON CLEAR
2.5 MHz CLOCK
EPROM PROGRAMMER
16K DYNAMIC RAM
8K ZIBL ROM
4K EPROMS
CONTROL DECODER
VIDEO REFRESH RAM, 1K
ADDRESS
DATA
VIDEO GENERATOR
COMPOSITE VIDEO OUTPUT
REFRESH
Z 80 CPU
ADDRESS BUS
CONTROL
BUS
DATA BUS
BUS FOR USER EXPANSION
CONTROL BUS
INT
POWER ON JUMP
ASCII KEYBOARD PORT
8 BIT PARALLEL I/O PORT
RS 232/20MA SERIAL I/O PORTS (2)
300 BAUD CASSETTE I/O WITH MOTOR CONTROL
32 TTL SENSE INPUTS
32 TTL FLAG OUTPUTS
8 LEDS
8 BIT LED
8 LEVEL PRIORITY INTERRUPT
REAL-TIME CLOCK
4 5-A RELAYS DPDT
4 0.75 A REED RELAYS SPST
INTERRUPTS
KEYBOARD
PARALLEL PORT
2 SERIAL PORTS
CASSETTE I/O
32 SENSE INPUTS
32 FLAG OUTPUTS
RELAY CONNECTIONS

Dynabyte

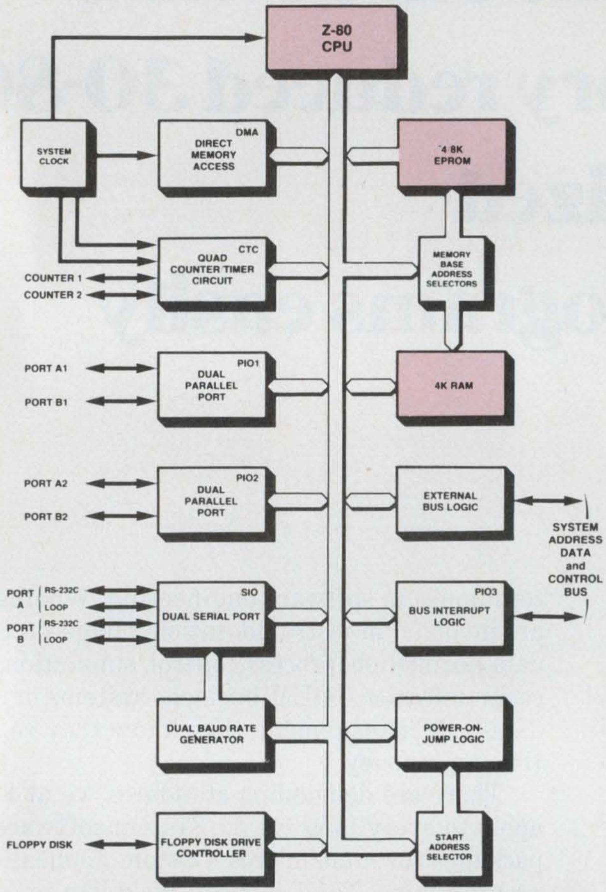
8-bit single-board microcomputer, MLZ-80

μP used: Z80

Alternate sources: Iasis and Monolithic Systems offer Z80-based SBC-80 compatible boards

Heurikon
700 West Badger Road
Madison, WI 53713
(608) 255-9075

The MLZ-80 microcomputer is a Z80-based system that is compatible with the Intel SBC-80 Multibus. On the card are four eight-bit ports (two of which can be bidirectional), two serial I/O ports (RS-232 or 20 mA current loop), 4096 bytes of RAM, sockets for up to 8 kbytes of EPROM, a floppy-disc interface, four counter/timers, a DMA interface, and power-on-jump logic. Either a 2.5 or 4 MHz version of the CPU is available. There are also eight levels of priority interrupt on the card.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	4096 bytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	64 kbytes
Clock frequency	2.5/4 MHz
I/O ports, parallel	4 × 8 & floppy-disc
I/O ports, serial	2 (50 to 19,200 baud)
Board size	171.5 × 304.8 mm
	6.75 × 12 in.
Power required (V/I)	5 V/1500 mA
	12 V/180 mA
	−12 V/120 mA

Hardware

Model	Description	Price (100 qty)
MLZ-80	Microcomputer board	$ 995
MLZ-80D	Processor board less chips	390
MLZ-8/32	32 k RAM card with 8 k EPROM	1200
MLZ-8/32D	Same but with just basic logic and sockets for RAM	350
MLZ-000	Breadboard card	190
MLZ-8022B	80 char × 25 line CRT card	390

Comments

Input and output lines of the MLZ-80 consist of four 8-bit ports, two of which can be set as bidirectional. All data and control lines are brought to a 50 pin edge connector. There are also two independent serial ports, each of which can be set for RS-232 or 20 mA current-loop operation. Both serial ports are software programmable for data rates from 50 to 19,200 baud. The last port is a floppy-disc interface for a formatter/controller.

The instruction set is that of the board's Z80 processor, and consists of 158 basic commands, 78 of which are those of the 8080A. The Z80 commands include 41 8 and 16-bit load instructions, 14 exchange, block transfer and search operations, 40 arithmetic and logic commands, 16 shift and rotate functions, 21 bit and I/O operations, 11 jump instructions and seven call/return commands.

Software support for the MLZ-80 starts with the ZRAID monitor program included on the floppy-disc software package. Soon to be available software will include an assembler, editor, debugger, and a disc-operating system. Currently available is a 16 k Basic interpreter and disc operating system on paper-tape, EPROM or floppy disc.

Hardware support consists of a single or dual floppy-disc-based development system. Peripherals such as printers, terminals, a paper tape punch/reader, and others are also available. And, since the board is SBC-80 compatible, support boards from over a dozen suppliers provide analog or digital interfaces for the MLZ-80.

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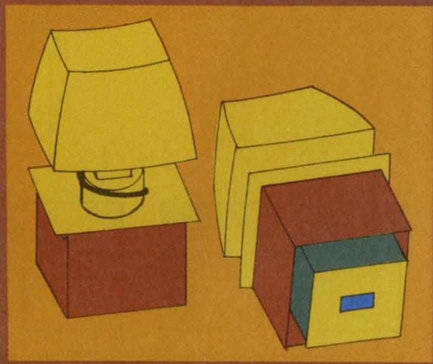


Square pad increases reliability. Height with keytop: $1\frac{5}{16}$".

C. P. CLARE & COMPANY
GENERAL INSTRUMENT CORPORATION

CIRCLE NUMBER 62

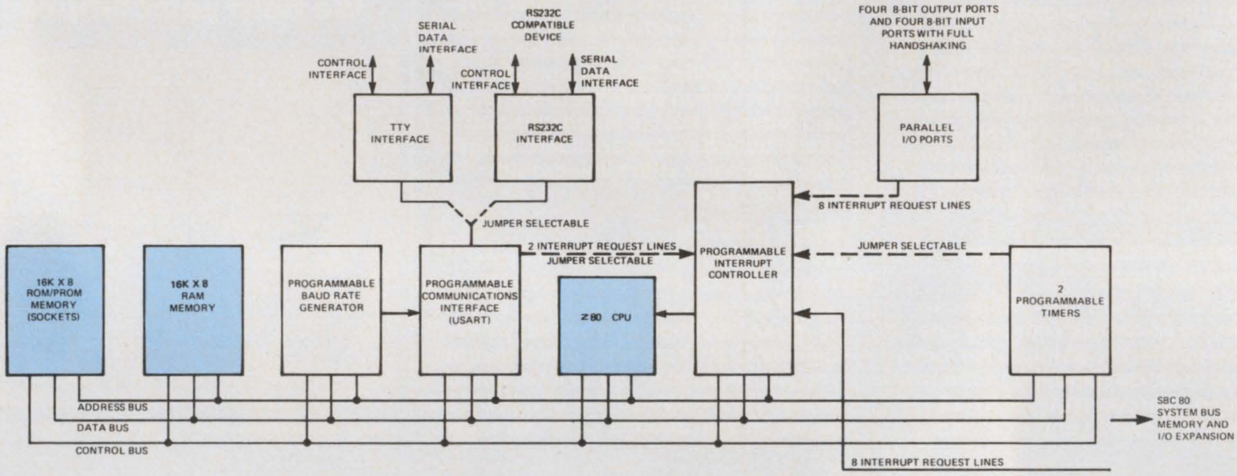
8-bit single-board microcomputer, 80/80C

μP used: Z80

Alternate sources: None

Iasis
257 Humboldt Street
Sunnyvale, CA 94087
(408) 734-9600

The SBC-80/80C is a Z80-based microcomputer board that is pin compatible with SBC-80 Multibus boards from Intel. On the board are up to 16 kbytes of RAM, up to 16 kbytes of EPROM, eight parallel I/O ports with full handshaking, one serial I/O port with RS-232 or TTY interface capability, two programmable counter/timers, eight levels of prioritized interrupt, hardware single-step logic, two real-time clocks and a DMA channel capability. There is also an auxiliary power bus on the board for battery back up of the RAM.



Comments

The input and output lines of the SBC-80/80C consist of eight parallel 8-bit ports made from 8212 latches that can be set up as inputs or outputs. There is also one serial port that can be programmed for baud rate and asynchronous or synchronous operation. The port can function as either an RS-232 or 20 mA current-loop interface. Baud rates range from 75 to 9600 baud for the asynchronous mode and up to 38,400 baud for the synchronous mode.

The instruction set is that of the board's Z80 microprocessor. There are 158 basic commands, including all 78 commands of the 8080A. Of the 158 commands, there are 41 8 and 16-bit load instructions, 14 exchange, transfer and search commands, 40 arithmetic and logic directives, 16 shift and rotate operations, 21 bit and I/O operations, and 11 jump instructions.

Software support consists of an optional ROM-based monitor program. Most 8080A programs and Z80 programs will run on the board, and time-sharing vendors offer a wide variety of cross-software for program development.

Hardware support for the SBC-80/80C consists of just the boards listed in the table. Additional support will come in the near future from Iasis, but there are currently over a dozen vendors of SBC-80 compatible support boards.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	4/16 kbytes
On-board ROM (min/max)	0/16 kbytes
Addressable memory	64 kbytes
Clock frequency	2.048 MHz
I/O ports, parallel	8 × 8 nonprogrammable
I/O ports, serial	1 (75 to 38,400 baud)
Board size	171.5 × 304.8 mm
	6.75 × 12 in.
Power required (V/I)	5 V/1800 mA
	12 V/400 mA
	−5 V/2 mA
	−12 V/100 mA

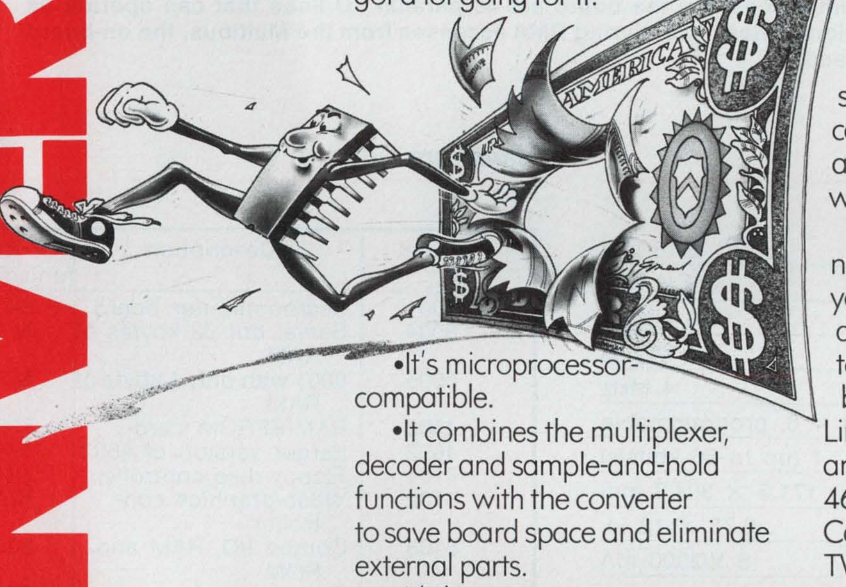
Hardware

Model	Description	Price (100 qty)
SBC-80/80C	Microcomputer board	$ 500
SBC-80/10C	Microcomputer board	365
SBC-80/14C	Microcomputer board	435

A/D CONVERTER

Announcing a cost breakthrough in multi-channel, μP compatible converters.

Fairchild just made a 6-channel analog-to-digital converter that's got a lot going for it.



•It's microprocessor-compatible.

•It combines the multiplexer, decoder and sample-and-hold functions with the converter to save board space and eliminate external parts.

•It's low cost.

Not just low, real low.

For only \$3.50 (100-piece price) you get a complete 8-bit, A/D linear subsystem. And the whole subsystem comes in either a plastic or ceramic 16-pin DIP so you don't have to play expensive design games to make it fit.

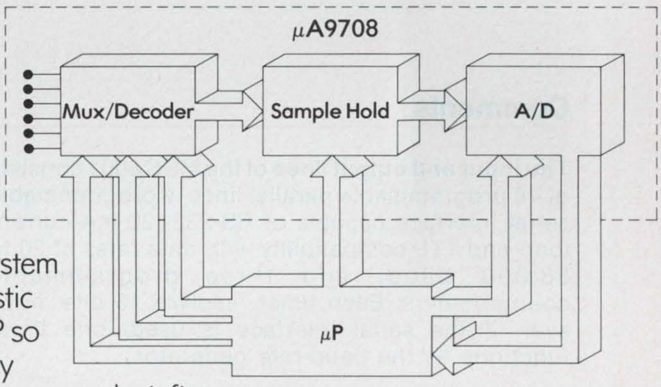
Technical wizardry.

Fairchild technology makes it all possible. The μA9708 is a monolithic 6-channel, 8-bit converter, designed for use with microprocessor systems like the F3870 and the F6800.

It provides 8-bit, $\pm\frac{1}{2}$-LSB conversion in 300μs featuring auto-zero and full-scale correction capabilities, ratiometric conversion and a wide input dynamic range which includes ground.

The key to the μA9708 is a simple analog-to-pulse width conversion technique used to achieve high-accuracy conversions with no critical external components.

For more details about our new A/D converter, just contact your Fairchild sales office, distributor or representative today. Or use the direct line at the bottom of this ad to reach our Linear Division. Fairchild Camera and Instrument Corporation, 464 Ellis Street, Mountain View, Calif. 94042. Tel: (415) 962-4903. TWX: 910-379-6435.



Typical μP Data Acquisition System Utilizing μA9708

FAIRCHILD

Call us on it. (415) 962-4903

CIRCLE NUMBER 63

8-bit single-board microcomputer, MSC 8001

μP used: Z80A

Alternate sources: None

Monolithic Systems
14 Inverness Drive East
Englewood, CO 80110
(303) 770-7400

Built around the Z80 microprocessor, the MSC 8001 operates at a 4 MHz clock and is fully hardware and software compatible with the Intel SBC-80 Multibus. The board holds up to 8 kbytes of EPROM and up to 8 kbytes of static RAM. Completely programmable interfaces connect the board to asynchronous or synchronous peripherals with TTL-compatible RS-232, or 20-mA current-loop interfaces. On the board are 48 parallel I/O lines that can operate as input, output or bidirectional lines. And, during DMA accesses from the Multibus, the on-board memory can be accessed.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	4/8 kbytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	64 kbytes
Clock frequency	4 MHz
I/O ports, parallel	6 × 8, programmable
I/O ports, serial	1 (up to 56 kbits/s)
Board size	171.5 × 304.8 mm
	6.75 × 12 in.
Power required (V/I)	5 V/2000 mA

Hardware

Model	Description	Price (unit qty)
MSC 8001	Microcomputer board	$ 845
8004	Same, but 32 kbytes of RAM	N/A
8005	8001 with only 1 kbyte of RAM	N/A
4502	RAM/EPROM card	795
4602	Larger version of 4502	2175
8101	Floppy-disc controller	N/A
8102	Video/graphics controller	N/A
8103	Combo I/O, RAM and ROM	820
8201	7-slot card chassis	375
8202	Quad output power supply	400

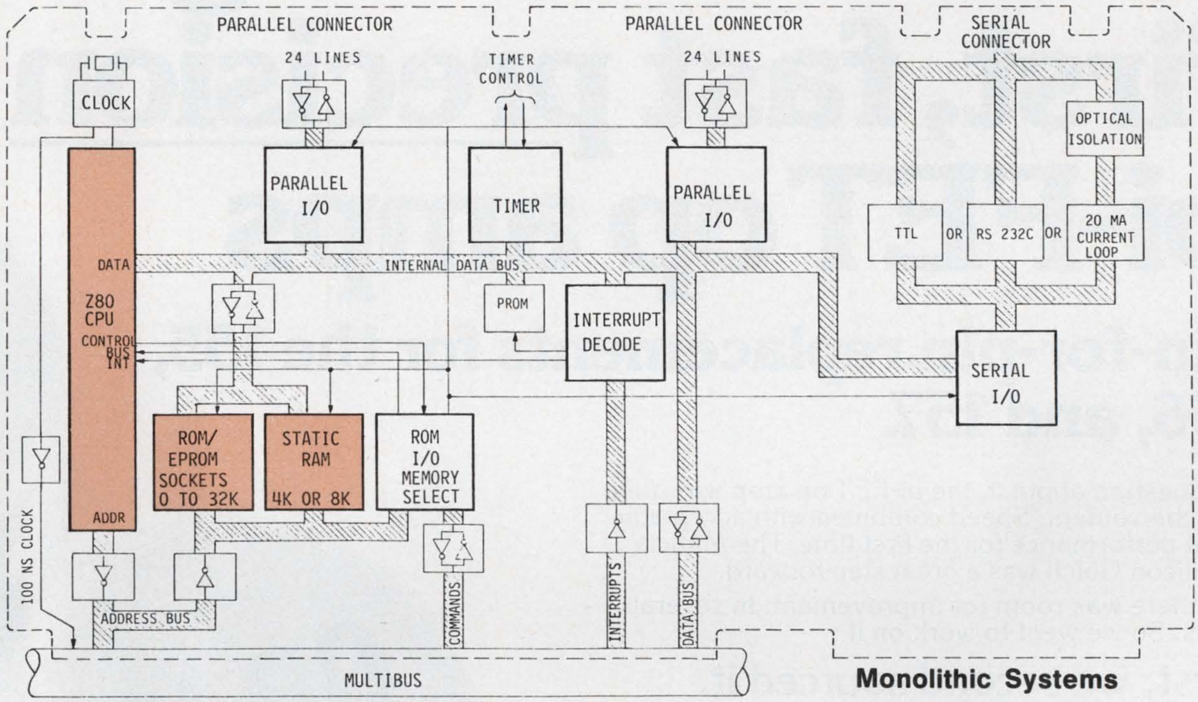
Comments

The input and output lines of the MSC 8001 consists of 48 programmable parallel lines, a programmable serial interface capable of RS-232, 20 mA current loop and TTL compatibility with data rates of 20 to 56,000 baud, and three programmable counter/timers. Each timer resolves 16 bits; however, if the serial interface is used, one timer functions as the baud-rate generator.

The instruction set is that of the Z80, which contains 158 basic commands, 78 of which are those of the 8080A. Of the 158 commands, there are 21 8-bit load commands, 20 16-bit load commands, 14 exchange, block transfer and search instructions, 17 arithmetic and logic commands for 8-bit operations and 11 for 16-bit functions, 12 general-purpose arithmetic commands, 16 shift and rotate operations, nine bit set, reset and test instructions, 11 jump directions, seven call/return commands, and 12 I/O operations.

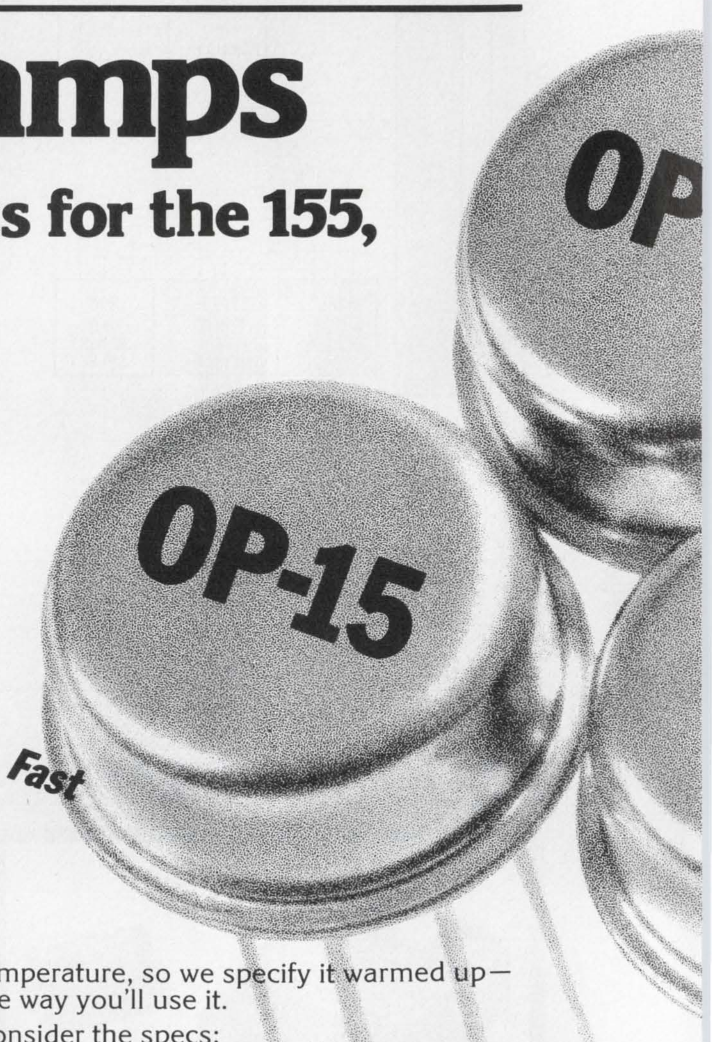
Software support consists of EPROM-based monitor editor, assembler and loader programs as well as a floppy-disc-based operating system. Also, since the processor can accept almost all 8080A code, most existing 8080A programs can be used. Time-sharing software vendors also have a variety of cross software available to the designer.

Hardware support consists of a floppy-disc-based development system as well as many peripheral boards. Also, since the board is SBC-80 compatible, most existing peripherals for the Intel SBC-80 family can be mated to the MSC 8001 family.


PARALLEL CONNECTOR
24 LINES
TIMER CONTROL
PARALLEL CONNECTOR
24 LINES
SERIAL CONNECTOR
CLOCK
PARALLEL I/O
TIMER
PARALLEL I/O
OPTICAL ISOLATION
TTL
OR
RS 232C
OR
20 MA CURRENT LOOP
DATA
INTERNAL DATA BUS
Z80 CPU
CONTROL BUS
INT
PROM
INTERRUPT DECODE
SERIAL I/O
ROM/ EPROM SOCKETS 0 TO 32K
STATIC RAM 4K OR 8K
ROM I/O MEMORY SELECT
ADDR
100 NS CLOCK
ADDRESS BUS
COMMANDS
INTERRUPTS
DATA BUS
MULTIBUS

PMI is delivering the first, fast precision bi-FET op amps

pin-for-pin replacements for the 155, 156, and 157.



No question about it, the bi-FET op amp was quite an achievement. Speed combined with acceptable input performance for the first time. The Miracle of Silicon Gulch was a great step forward.

But there **was** room for improvement. In several areas. So we went to work on it.

First, we second sourced it. And made it better.

We set about to improve idling current control, reduce second-stage TCV_{os} and improve the first stage balance. The results were PMI's PM155A, 156A, and 157A, with specs, yields, and delivery far superior to the Miracle's maker. But we didn't stop there.

We were convinced that the basic design could be improved. It could be made faster. And more precise. So we designed a completely new proprietary series of op amps that would perform the way bi-FET op amps should.

And now, meet the Miracle of Miracles!

PMI's OP-15, OP-16, and OP-17 are the first **precision** pin-compatible versions of the 155A, 156A, and 157A, respectively. They give you three **major** improvements in performance:

1. Higher speed—by a factor of two.

2. Reduced offset voltage, thanks to our production-proven zener zap trimming technique. TCV_{os} is well-behaved.

3. High-temperature bias current drastically reduced—by an order of magnitude—by means of a FET leakage current cancellation circuit. **U.S. Patent 4068254.**

Let's look at that last point for just a moment. Although FET input current is picoamperes at room temperature, it doubles with every ten-degree rise. It can be several nanoamperes at 70°C ambient and **hundreds** of nanoamps at 125°C—worse than many bipolar op amps. The fact that the chip temperature is 20° to 30° higher than the ambient doesn't help. FET bias current is important. We think it's misleading to specify it at junction temperature, so we specify it warmed up—the way you'll use it.

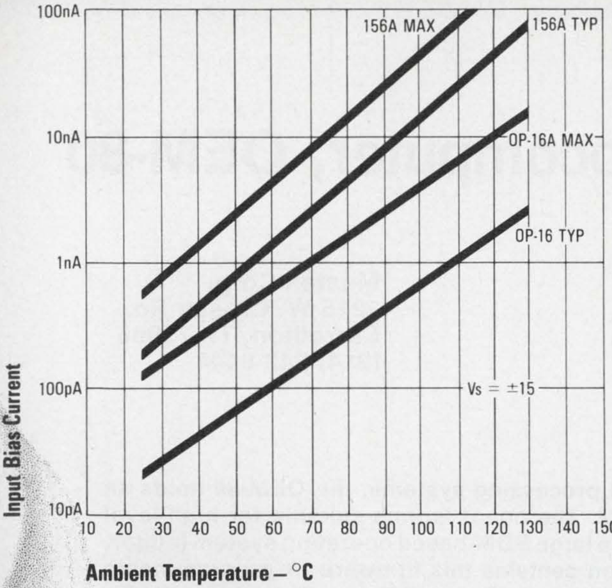
Consider the specs:

OP-15/LF155, OP-16/LF156 and OP-17/LF157 Comparison Chart

Parameter*	LF155A LF355A	OP-15A OP-15E	LF156A LF356A	OP-16A OP-16E	LF157A LF357A	OP-17A OP-17E	Units
Offset Voltage, Max.	2.0	0.5	2.0	0.5	2.0	0.5	mV
Bias Current, Max. (warmed-up) 0 to 70°C	8.0	0.75	9.0	0.9	9.0	0.9	nA
−55 to 125°C	100	9	180	11	180	11	nA
Slew Rate, Min.	3	10	10	18	40	45	V/μsec.
Gain-Bandwidth Product Typ.	2.5	6.0	4.5	8.0	20	30	MHz
Supply Current, Max.	4	4	7 156A 10 356A	7	7 157A 10 357A	7	mA
Voltage Gain, Min.	50	100	50	100	50	100	V/mV

*All other parameters are more or less equivalent; in the case of TCV_{os}, however, the OP-15/16/17's **really do** meet the spec—and our typicals **are** typical of what you get.

A quick look tells us that the OP-15 has the speed of the 356A, but not the **power dissipation,** which is the same as the 355A. The OP-16 is twice as fast as the 356A.



Input Bias Current vs. Ambient Temperature
(Units are warmed-up in free air)

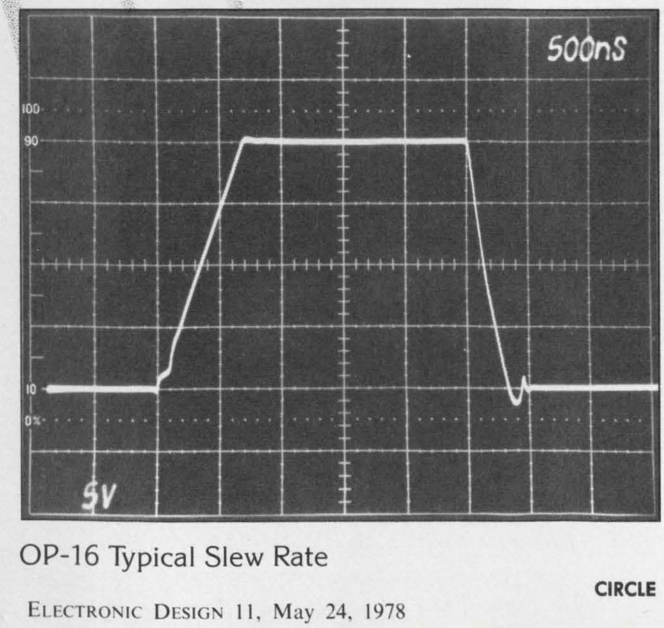
So what's the bottom line?

Offset voltage improved fourfold. Circuit balanced for low TCV_{OS}. Bias current over temperature reduced ten times. And the OP-15/16/17 fits all 155/156/157 sockets. Plus:

The **OP-15**'s supply current is low like the 155's, yet it gives you the speed of the 156.

The **OP-16** gives you the best power/speed compromise you can find—twice as fast as the 156, but with the same moderate power dissipation.

The **OP-17** gives you ultra-high speed (70v/μsec. typical in a gain of five)—high enough to challenge costly dielectrically-isolated devices.



OP-16 Typical Slew Rate

And cost. What about cost?

There's no basis for comparisons, since nobody else is delivering "A" grade bi-FETs anyway. For sure nobody is delivering anything that comes close to the OP-15/16/17 specifications. But we would like to make something clear:

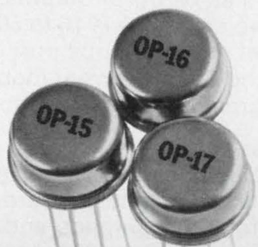
We do not consider a bi-FET op amp to be a substitute for a 741. With its larger chip area and extra ion-implant step, the bi-FET will always cost more; and the OP-15, 16, and 17 are **precision,** high-speed, low-bias-current op amps designed to give you high performance and high speed over the full operating temperature range. They cost more than 741's.

On the other hand, they cost **less** than LF-155/6/7A's—even though they outperform them.

Model	Temp. Range	Price (100–999)
OP-15/16/17A	−55°C/+125°C	$18.00
OP-15/16/17B	−55°C/+125°C	$ 9.00
OP-15/16/17C	−55°C/+125°C	$ 6.00
OP-15/16/17E	0°C/+70°C	$10.00
OP-15/16/17F	0°C/+70°C	$ 3.50
OP-15/16/17G	0°C/+70°C	$ 2.50

Lower price. Better performance. And we actually deliver them.

When you get right down to it, our miracle is a lot more dazzling than their miracle.



PMI's OP-15, OP-16, and OP-17. The next industry standard.

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Telephone: (408) 246-9222
TWX: 910-338-0528
Cable: MONO

Mail to:
Precision Monolithics, Inc., 1500 Space Park Drive
Santa Clara, CA 95050
I'm interested in the following:
☐ OP 15/16/17 data sheets ☐ Full Product Catalog
☐ Have a Sales Engineer call ( ) ____-______
Name________________
Title________________
Company________________
Address________________
City________ State________ Zip________

CIRCLE NUMBER 66

8-bit single-board microcomputer, OEM-80

μP used: Z80

Alternate sources: None

Mostek Corp.
1215 W. Crosby Rd.
Carrollton, TX 75006
(214) 242-0444

Developed primarily for small business and word processing systems, the OEM-80 holds as much as 16 kbytes of RAM and 20 kbytes of ROM. The board is thus suitable for high-level languages or substantial data, and accommodates a large ROM-based operating system (editor, assembler, loader, debugger). The SDB-80 version contains this firmware. A programmable serial interface (110 to 9600 baud) and 40 lines of buffered I/O are available. Bus expansion for an optional disc controller and a variety of other boards is provided. The OEM-80 also contains four programmable timers, dynamic-memory refresh, and vectored interrupts. A Fortran cross assembler and simulator for 16-bit minis is available.

Comments

Parallel I/O consists of 40 lines that are buffered and can be configured as inputs or outputs, 20 of them bidirectional. Drive capability is 16 to 50 mA of sink current. The serial asynchronous port can accommodate RS-232 and 20-mA current loop interfaces. The speed is programmable from 110 to 9600 baud.

The instruction set of the board's Z80 includes all 8080 op codes, plus 80 more. Twelve are general-purpose arithmetic commands, 17 are arithmetic-logic commands for 8-bit operands, and 11 more are for 16-bit operations. There are 20 load instructions, and 14 exchange, block transfer, and search instructions. Nine bit set, reset and test commands, 16 shift/rotate functions, 11 jump commands, seven call/return functions and 12 I/O operations complete the set of 158.

Software support includes an operating system with debugger ($75) and text editor/assembler ($300) in ROM, a Fortran IV cross assembler and simulator ($250 each) and floppy-disc development software and operating system.

Hardware support includes OEM-80 versions with system firmware (from $1195), the AIM-80 in-circuit emulation module ($1195), breadboard and extender cards ($55), and the disc-based development system AID-80F ($5995).

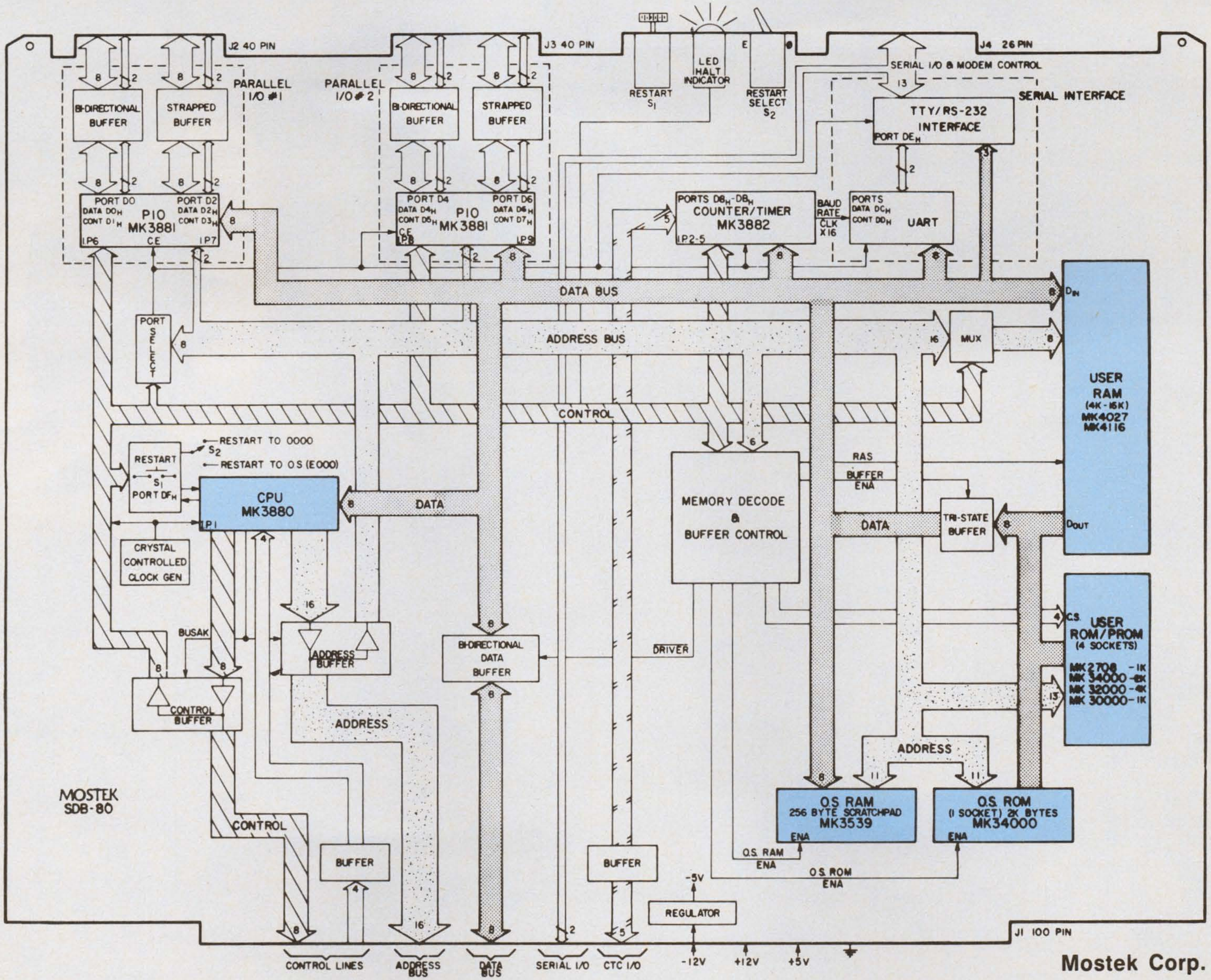
Note: For board architecture see p. 143.

Specifications

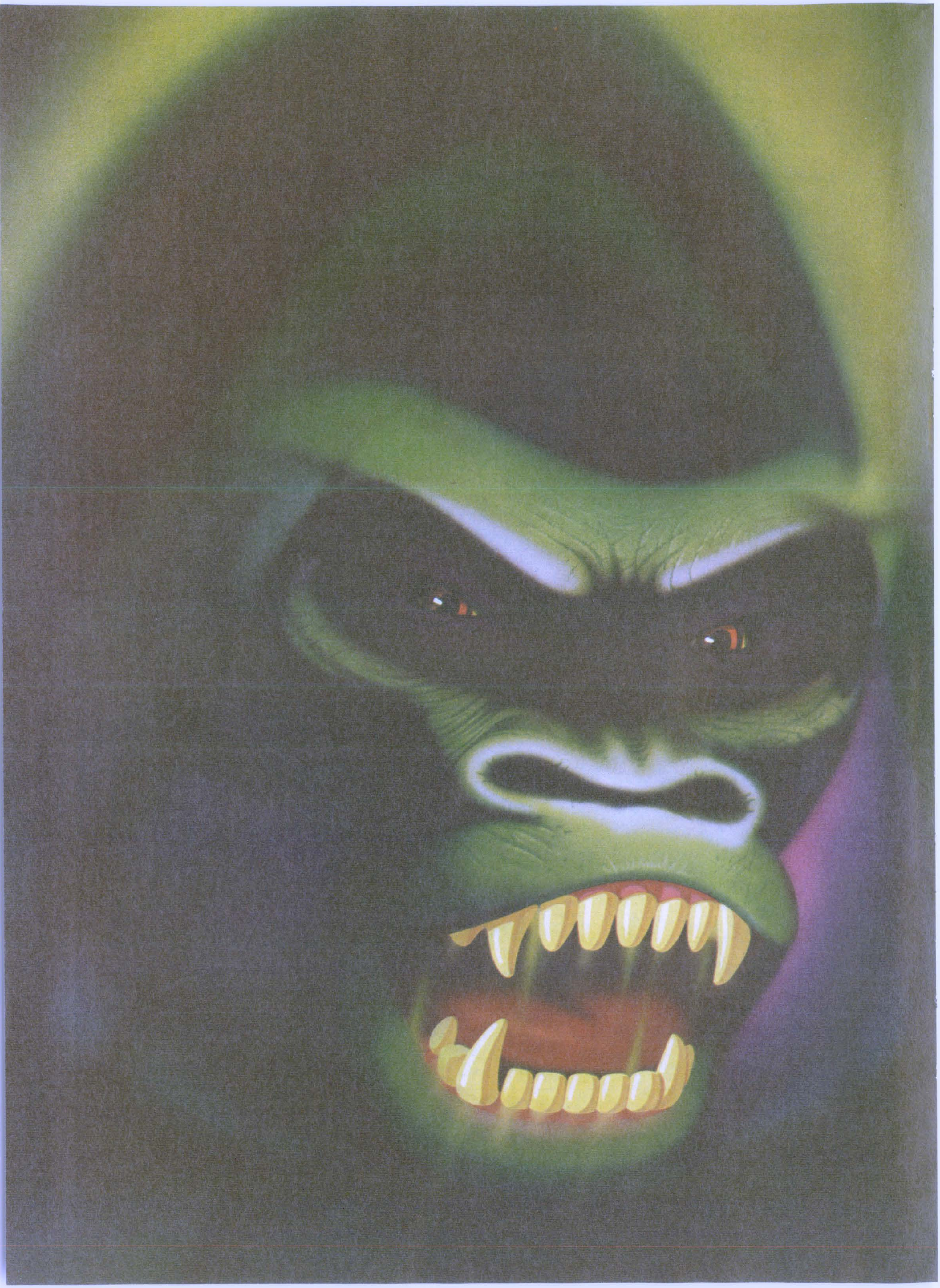
Word size (data/address)	8/16 bits
On-board RAM (min/max)	4/16 kbytes
On-board ROM (min/max)	2/20 kbytes
Addressable memory	64 kbytes
Clock frequency	2.5 MHz
I/O ports, parallel	4 × (8+2)
I/O ports, serial	1 (110 to 9600 baud)
Board size	305 × 216 mm
	12 × 8.5 in.
Power required (V/I)	5 V/2600 mA
	12 V/480 mA
	−12 V/180 mA

Hardware

Model	Description	Price (100 qty)
OEM-80/4	μC with 4 k RAM	$ 430
OEM-80/16	same w. 16 kbytes RAM	539
RAM-80A	16 kbyte RAM board	364
RAM-80B	same, expand. to 64 k w. 4 par. I/O ports	573
FLP-80	Floppy-disc interface	543
PPG-08	PROM programmer	210
VAB-2	CRT interface module	132
XAID-102	3-slot card cage	100


J2 40 PIN
J3 40 PIN
J4 26 PIN
J1 100 PIN
PARALLEL I/O #1
PARALLEL I/O #2
BI-DIRECTIONAL BUFFER
STRAPPED BUFFER
PORT D0
PORT D2
PIO MK3881
PORT D4
PORT D6
LED HALT INDICATOR
RESTART S_1
RESTART SELECT S_2
SERIAL I/O & MODEM CONTROL
SERIAL INTERFACE
TTY/RS-232 INTERFACE
COUNTER/TIMER MK3882
UART
DATA BUS
ADDRESS BUS
CONTROL
MUX
USER RAM (4K-16K) MK4027 MK4116
PORT SELECT
RESTART TO 0000
RESTART TO O.S (E000)
CPU MK3880
CRYSTAL CONTROLLED CLOCK GEN
MEMORY DECODE & BUFFER CONTROL
RAS
BUFFER ENA
DATA
TRI-STATE BUFFER
USER ROM/PROM (4 SOCKETS)
MK2708 - 1K
MK 34000 - 8K
MK 32000 - 4K
MK 30000 - 1K
BUSAK
ADDRESS BUFFER
BI-DIRECTIONAL DATA BUFFER
DRIVER
CONTROL BUFFER
ADDRESS
O.S RAM 256 BYTE SCRATCHPAD MK3539
O.S ROM (1 SOCKET) 2K BYTES MK34000
O.S RAM ENA
O.S ROM ENA
MOSTEK SDB-80
BUFFER
REGULATOR
-5V
CONTROL LINES
ADDRESS BUS
DATA BUS
SERIAL I/O
CTC I/O
-12V
+12V
+5V

Mostek Corp.



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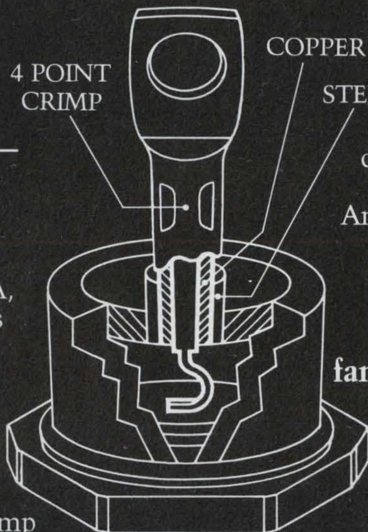

Introducing Unitrode's SD51 – the first significant increase in reliability for a power Schottky. At 18% less cost.

We didn't want to introduce a 60A, 45V power Schottky that was just as good as the competition's. We wanted to give you one you could actually use. Without all the traditional SD51 reliability problems.

So we made some changes.

We gave our SD51 family a copper terminal and a four-point crimp to make it rugged and minimize contact resistance. (A steel terminal with a two-point crimp may be good enough for the other guys. But it's not good enough for Unitrode.)

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But if you know Unitrode, you know we didn't stop there.

Introducing Unitrode's USD545 family of power Schottky rectifiers.

Our new USD545 family shares the same rugged mechanical package as our SD51 series. And offers increased current ratings– 75A average and 1000A surge. Yet it's even more reliable thanks to its lower junction temperature. This is a result of lower leakage at elevated temperatures (50mA at 45V at 125°C case temperature) and better thermal resistance (0.8°C/W). And you can have this added reliability for just $5.85 in 100's.

As you can see, we set some pretty tough standards.

For more information, just circle the reader service number or call or write: Unitrode Corporation, 580 Pleasant Street, Watertown, MA 02172. Tel. 617-926-0404.

UNITRODE

IN SEMICONDUCTORS, UNITRODE MEANS POWER.

CIRCLE NUMBER 33

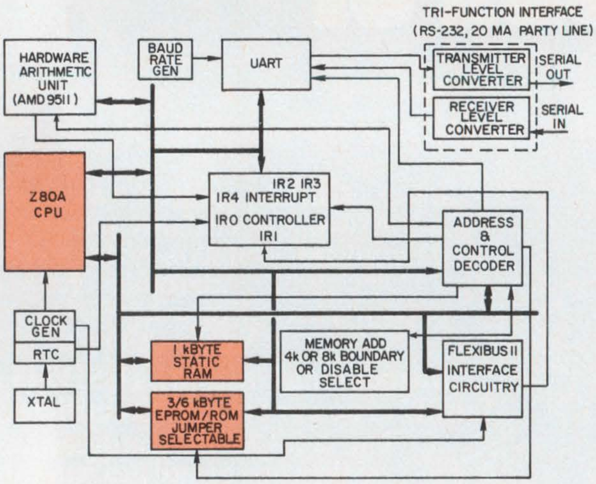
8-bit single-board microcomputer, PCS 1880

μP used: Z80A

Alternate sources: None

Process Computer Systems
750 North Maple Road
Saline, MI 48176
(313) 429-4971

The PCS 1880 is a stand-alone μC board, which can be plugged into a Flexibus II system whose architecture allows memory, I/O, or interface modules to be addressed as memory locations (memory-mapped I/O). The Z80's duplicate set of general-purpose registers permits fast storage when interrupts or subroutines are serviced. An external last-in, first-out stack is provided to store the program counter, flags, all six general-purpose registers, and the auxiliary register set. Board option A includes the AMD 9511 math chip which provides the four basic math functions in fixed and floating point notation (up to 32-bit accuracy), plus square root, trigonometry, exponentiation and common as well as natural logarithms.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1/6 kbytes
On-board ROM (min/max)	0/6 kbytes
Addressable memory	64 kbytes
Clock frequency	4 MHz
I/O ports, parallel	8 three-state lines
I/O ports, serial	1 (50 to 9600 baud)
Board size	267 × 216 mm
	10.5 × 8.5 in.
Power required (V/I)	5 V/1700 mA
	12 V/200 mA
	−5 V/100 mA

Comments

I/O ports include eight parallel lines for memory-mapped I/O (up to 256 addresses), and an optically isolated serial port which can operate as RS-232, 20-mA current loop, or party line. Nine switch-selectable baud rates range from 50 to 9600 baud. The UART receiver and transmitter is controlled by the interrupt controller, which handles five vectored interrupts. One nonmaskable interrupt is handled directly by the CPU.

The instruction set of the Z80A contains all 78 op codes of the 8080A's instruction set, plus 80 more. Of the 158 total instructions, 12 are general-purpose arithmetic commands, 17 arithmetic/logic commands for 8-bit and 11 for 16-bit operations, 21 are 8-bit and 20 are 16-bit load commands, and 14 exchange, block transfer and search instructions. Nine bit set, reset and test commands, 16 shift and rotate functions, 11 jump instructions, seven call/return directives and 12 I/O operations complete the set.

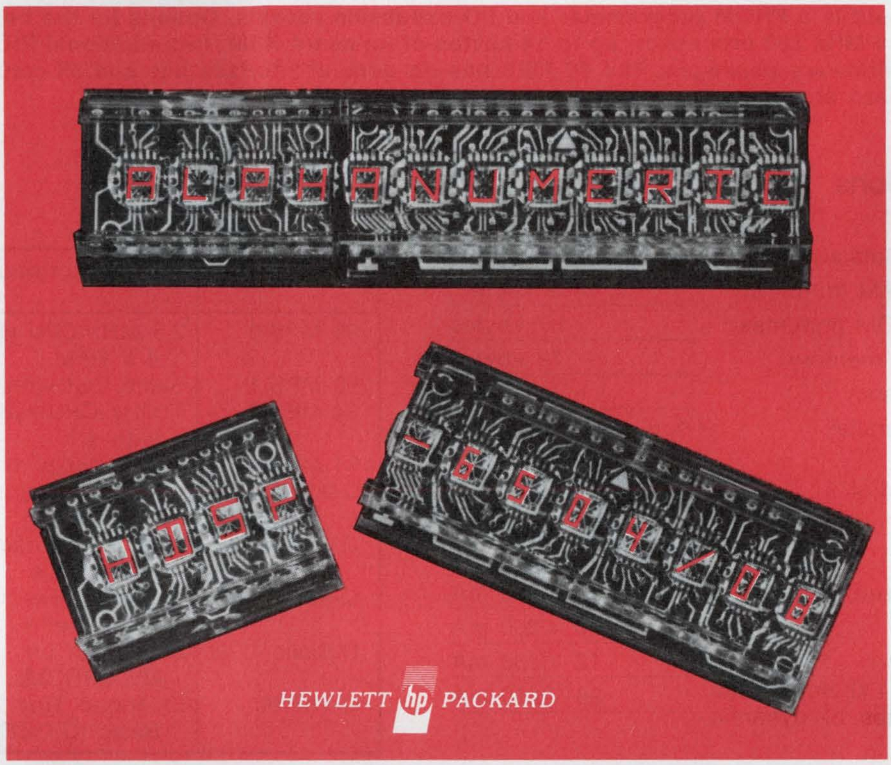
Hardware

Model	Description	Price (100-qty)
1880	μC module	$ 447
Option A	Contains arithm. chip	557

Hardware support includes a range of modules, listed under the PCS 1806/1810 systems, and the SPDS disc-based Z80 development system.

Because the board is software-compatible with the 8080A instruction set, all PCS 1806/SuperPac software is supported by the 1880. This includes utility and math libraries.

Get high efficiency and crystal clarity in the new HP 16-segment alphanumeric displays.



From Schweber.

Hewlett-Packard has done it again. An all new 16-segment alphanumeric display with low power consumption, high on/off contrast and perfect readability.

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With their compact size and double-end-stackable design, HP 16-segment displays are ideal for computer terminals and other peripherals, desk-top calculators, in-plant control equipment and small, hand-held instruments. They also interface with MPU and LSI circuitry.

In addition, when you order your high efficiency HP 16-segment alphanumerics from Schweber, you get efficient, off-the-shelf deliveries too. Instantly!

4 Digit	250-999	100-249	25-99	1-24
HDSP-6504	17.00	19.00	21.60	24.00
HDSP-6505 (2nd Lens)	.70	.75	.80	.85

8 Digit	125-499	50-124	13-49	1-12
HDSP-6508	34.00	38.00	43.20	48.00
HDSP-6509 (2nd Lens)	.70	.75	.80	.85

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Eden Prairie, Minn: 612/941-5280 ■ Dallas, Texas: 214/661-5010 ■ Detroit, Michigan: 313/525-8100 ■ Irvine, Ca.: 213/537-4321
714/556-3880

SCHWEBER ELECTRONICS

CIRCLE NUMBER 68

8-bit single-board microcomputer, 90 MPS

μP used: Z80A

Quay Corporation
P.O. Box 386
Freehold, NJ 07728
(201) 681-8700

Alternate sources: None

The 90 MPS is a complete microcomputer system on a board and includes 4 kbytes of dynamic RAM, 1 kbyte of static RAM, 1 kbyte of EPROM, a 2.5 MHz Z80 CPU, two Z80-PIO chips, a counter/timer, and a UART with RS-232 or 20 mA current loop compatibility. Also included on the board is a PROM programmer and I/O expansion sockets. Options for the board consist of the 4 MHz Z80 processor, up to 64 kbytes of on-board RAM, two additional PIO chips and many firmware packages. The 90 MPS has no general interface bus and all connections to the board are made via the three 60-pin I/O connectors.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	5/65 kbytes*
On-board ROM (min/max)	1/7 kbytes
Addressable memory	72 kbytes
Clock frequency	4 MHz
I/O ports, parallel	4 × 8, expandable to 8 × 8
I/O ports, serial	1 (up to 9600 baud)
Board size	40.4 × 19.6 mm
	16.175 × 7.875 in.
Power required (V/I)	5 V/1000 mA
	−5 V/200 mA
	12 V/250 mA
	28 V/250 mA

* Combines 1 kbyte of static and 64 kbytes of dynamic RAM.

Hardware

Model	Description	Price (100 qty)
90 MPS-Ø	2.5 MHz CPU with 4 k RAM	$ 500
90 MPS-1	Same, but with 16 k	775
94 MPS-Ø	4 MHz CPU system with 4 k	570
94 MPS-1	Same, but with 16 k	845
Q4k×8DRM	4 k × 8 dynamic RAM chips	75
Q16k×8DRM	16 k × 8 dynamic RAM chips	305
Q-Basic 1/90	LLL/Quay Basic (8 k) on cassette	50
Q-Basic 1/90P	Same, but on UV EPROMs	195
Q-TBE/90	Extended Tiny Basic (UV EPROM)	115

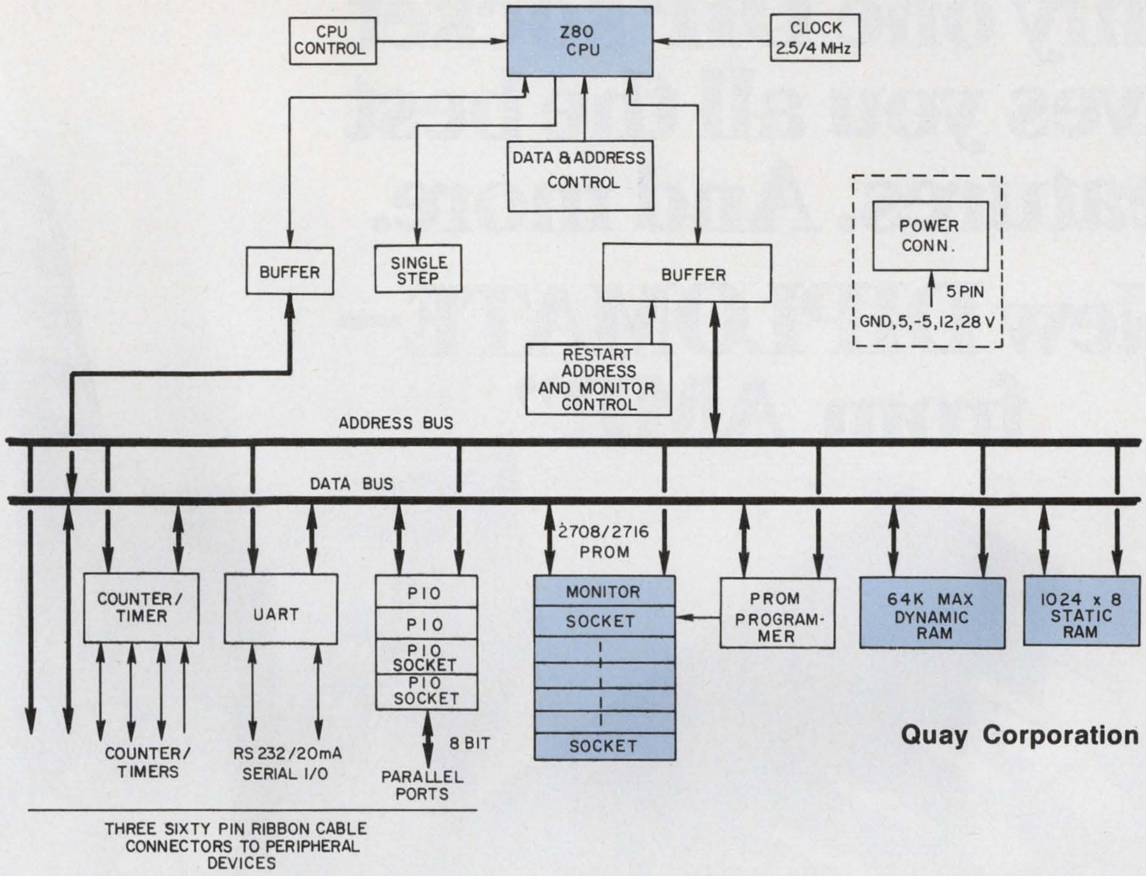
Comments

The input and output lines of Quay 90 MPS are provided by the Z80-PIO chips used. Each PIO chip has two 8-bit ports and several handshake lines as well as the ability to handle vectored interrupts. The computer board can hold up to four PIO chips, thus providing up to 64 I/O lines and 16 handshake lines. The serial port consists of a UART and RS-232/TTY interfaces and can operate at up to 9600 baud.

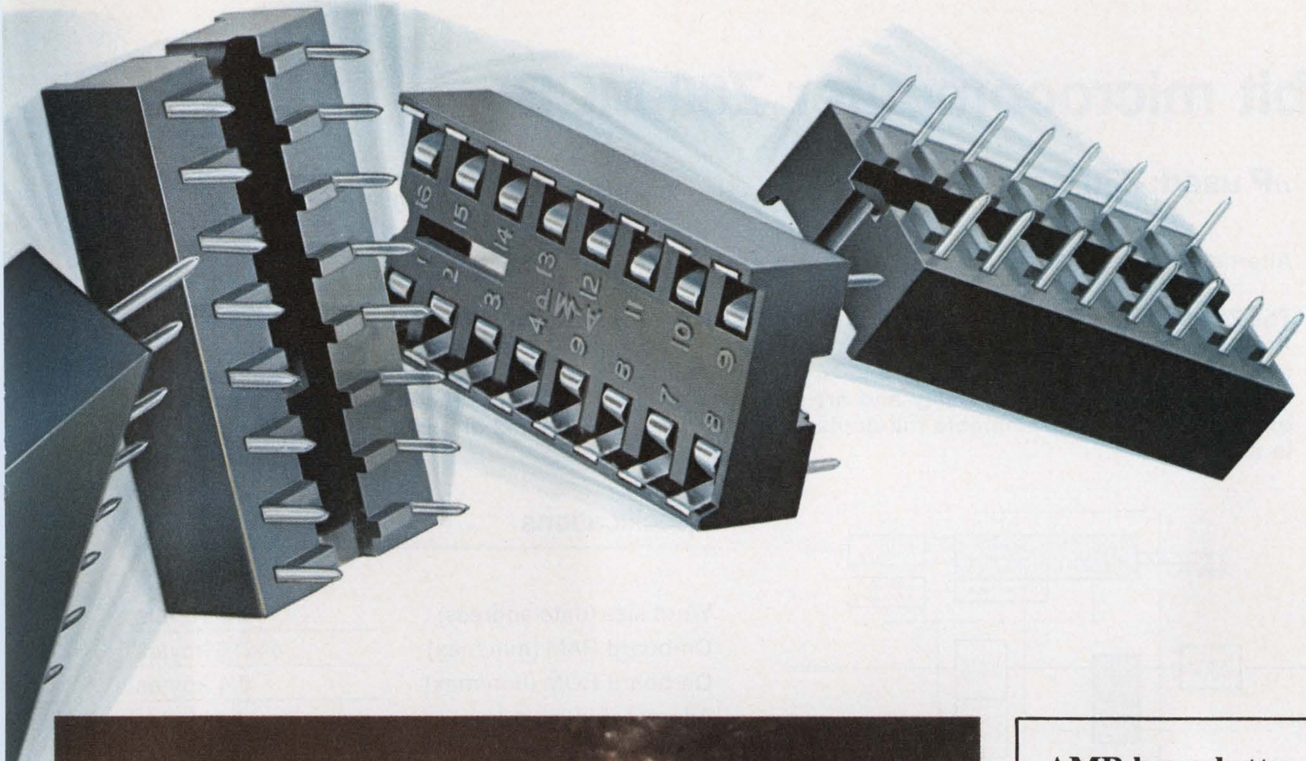
The instruction set of the board is that of the Z80 processor and contains 158 basic commands, 78 of which are the 8080A's instructions. There are 21 8-bit load commands, 20 16-bit load commands, 14 exchange, block transfer and search operations, 11 16-bit arithmetic and logic instructions, 12 general-purpose arithmetic commands, 16 shift and rotate functions, nine bit set, reset and test operations, 11 jump directives, seven call/return instructions, and 12 I/O commands.

Hardware support for the 90/94 MPS consists of the items in the table and any Z80-compatible hardware from other vendors.

Software support consists of the ROM and cassette based Basic and Tiny Basic, as well as single-step capability of the CPU. There are also three hardware breakpoints and a snap/trace (PC) capability. Paging is used on the upper 16 k of memory to bring the total addressable memory to 64 kbytes of dynamic RAM, 7 kbytes of PROM and 1 kbyte of static RAM.



Quay Corporation



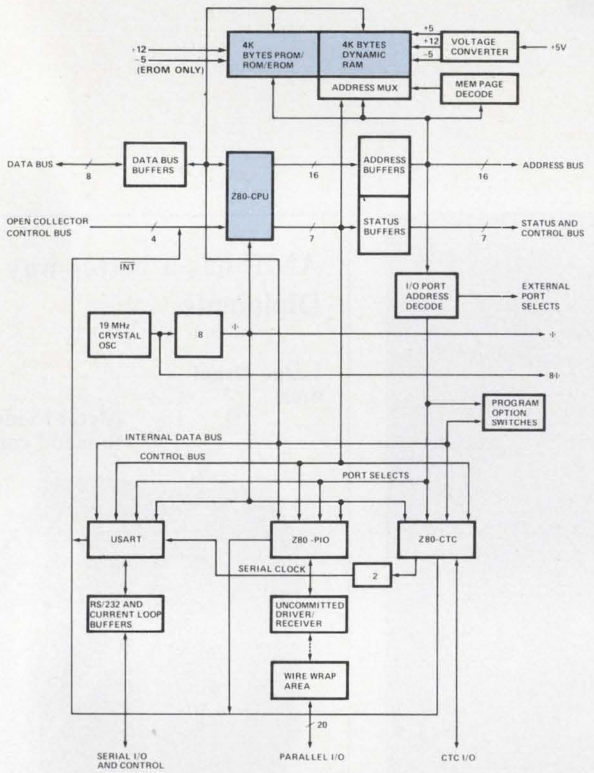
8-bit microcomputer Z80-MCB

μP used: Z80

Alternate Sources: None

Zilog Inc.
10460 Bubb Road
Cupertino, CA 95014
(408) 446-4666

The Z80-MCB is a self-contained microcomputer that needs only a 5-V power supply to operate. It also serves as the CPU board for a modular microcomputer system because the 122-pin interface bus is compatible with the MCZ microcomputer system. All data, address and control lines have three-state capability and are TTL-compatible. The 158 instructions include those of the 8080A. A programmable full-duplex serial I/O port with RS-232 or current-loop interface is included.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	4 k/16 kbytes
On-board ROM (min/max)	0/4 kbytes
Addressable memory	64 kbytes
Clock frequency	2.47 MHz
I/O ports, parallel	2 × 8
I/O ports, serial	1 (50 to 38,400 baud)
Board size	196 × 190 mm
	7.7 × 7.5 in.
Power required (V/I)	5 V/2000 mA

Hardware

Model	Description	Price (25 qty)
Z80-MCB	Microcomputer board	$ 415
Z80-MDC	Memory/disc controller	695
Z80-RMB	RAM memory board	650
Z80-IOB	Parallel I/O board	315
Z80-PMB	PROM memory board	345
Z80-SIB	Serial I/O board	335
Z80-VDB	Video display board	400
Z80-PPB	PROM/EPROM programmer	525
Z80-AIO	Analog board	875

Comments

Two 8-bit parallel ports with handshakes and sockets for drivers and receivers, 4 counter-timer channels, and full-duplex USART are provided. Bus request and acknowledge signals on the backplane simplify use in multiprocessing applications.

The set of 158 instructions not only includes those of the 8080A, but also commands for 4, 8, and 16-bit operations with indexed, relative, and bit addressing modes. Block memory, I/O, and 16-bit arithmetic instructions are provided.

Available hardware, in addition to the listed boards, includes a wire wrap board ($250), extender board ($125) and card cage ($225), as well as a program development station and the MCZ-1 series microcomputer system. A Z80-MCB option contains a 1-kbyte monitor in resident PROM.

Software support includes a macro-assembler, file maintenance system, editor, debug and utility routines, basic interpreters, PL/Z, Cobol, and Fortran. A software library and users' group provide applications programs.

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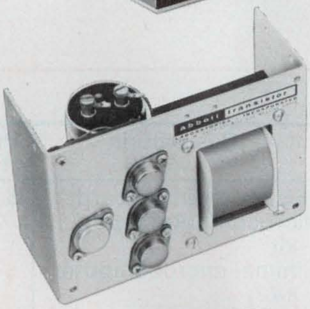

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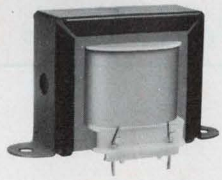

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See Power Supply Section 4000, and Transformer Section 5600, Vol. 2, of your EEM catalog; or Power Supply Section 4500, and Transformer Section 0400, Vol. 2, of your GOLD BOOK for complete information on Abbott products.

abbott transistor

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Eastern Office
1224 Anderson Ave., Fort Lee, N.J. 07024
(201) 224-6900 Telex: 13-5332

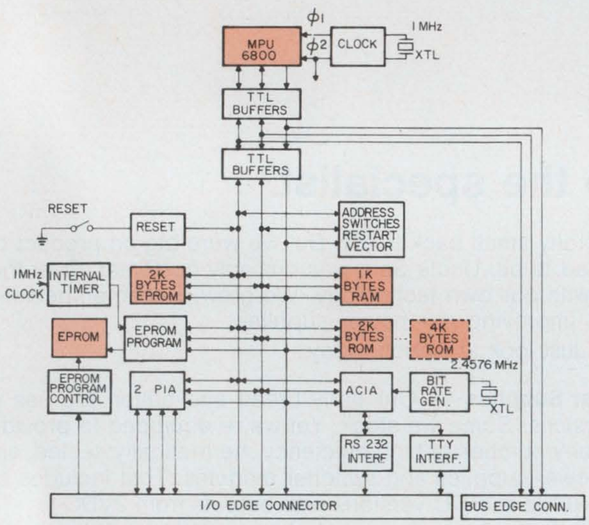
8-bit single-board microcomputer, EVK 300

μP used: 6800

Alternate sources: None

American Microsystems
3800 Homestead Rd.
Santa Clara, CA 95051
(408) 246-0330

There are three boards in the family, the EVK 100, 200 and 300, of which only the EVK 300 comes completely assembled. On the board are up to 4 kbytes of ROM, 2 kbytes of EPROM, 1 kbyte of static RAM, 58 I/O lines and a TTY current loop or RS-232 interface as well as the 6800 central processor. The board has totally buffered interface lines, the ability to select the restart address, a selectable DMA mode, an interval timer, and an on-board programmer for the S6834 EPROM.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1 kbyte
On-board ROM (min/max)	2/6 kbytes
Addressable memory	16 kbytes
Clock frequency	1 MHz
I/O ports, parallel	6 × 8 lines, 4 × 2 lines
I/O ports, serial	1 (110 to 9600 baud)
Board size	259 × 305 mm
	10.2 × 12 in.
Power required (V/I)	5 V/4000 mA

Comments

The input and output lines of the EVK 300 are formed from three 6820 PIAs. Each PIA offers two 8-bit ports and two handshake lines for each port, for a total of 58 parallel I/O lines. There is also a serial port on the board capable of operating from 110 to 9600 baud in either an RS-232 or TTY interface.

The basic instruction set consists of 72 commands that include binary and decimal arithmetic operations, logic instructions, shift and rotate functions, branch and stack manipulation commands and memory transfer operations. I/O commands are stored in the memory address space. Most instructions operate on both the ALU and memory.

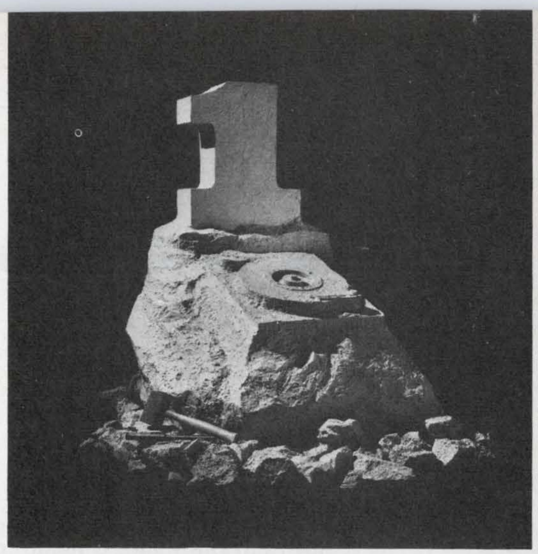
Hardware support for the EVK family consists of the various levels of EVK boards and a large development system for in-circuit emulation and hardware testing.

Software support for the boards includes a microassembler, a disassembler, a ROM-based subroutine library, ROM-based Tiny Basic and a full operating system. All 6800 compatible software can also be used with the board.

Hardware

Model	Description	Price (100 qty)
EVK 300	Microcomputer board	$ 615
EVK 200	Microcomputer board kit	475
EVK 100	Minimal microcomputer kit	295
EVK 99	Evaluation kit	133
EVK 98	Prototyping board	75

An evolution of the third kind.



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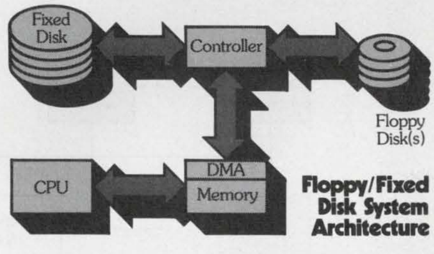

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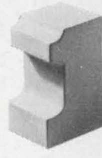

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CIRCLE NUMBER 72

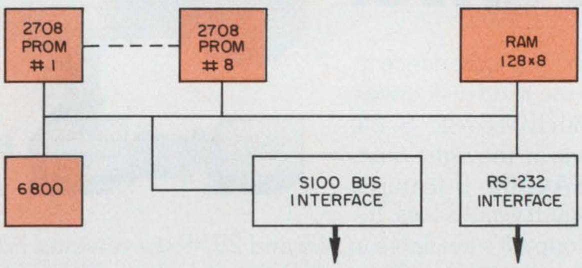
8-bit single-board microcomputer, HTA 6800

μP used: 6800

Alternate sources: None

Hodge, Taylor & Assoc.
1161 North Tustin Ave.
Orange, CA 92667
(714) 998-0607

The HTA-6800 microcomputer board offers the user an S-100 bus interface for expandability but operation with a 6800 μP. On the board are 128 bytes of RAM up to 8 kbytes of EPROM and an RS-232 interface in addition to the CPU and bus logic. For program development an EPROM containing a superset of Motorola's EX-BUG and AMI's DEBUG is included. Much high level software is included in the HTA6800 package—IBM scientific subroutines, Fortran IV, Basic, a macroassembler, linking loader and even a word processing package.



Comments

Input and output lines of the HTA-6800 consist of an RS-232 interface and the S-100 bus interface, which has a 16-bit address bus and an 8-bit data bus in addition to a wide variety of control and signal lines.

The instruction set is that of the board's 6800 microprocessor. There are 72 commands that include binary and decimal arithmetic operations, logic instructions, shift and rotate functions, branch and stack manipulation commands, and memory transfer operations.

Software support includes a machine-level package that supports EXBUG, MCBUG and DEBUG routines from Motorola and AMI. Also available is software complete with an IBM Scientific subroutine package, Fortran IV, Basic, a macro assembler and a linking loader. Software is designed to support some of the IBM applications software.

Hardware support includes hard and floppy disc controllers from the company as well as most S-100 compatible boards from various manufacturers.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	128 bytes
On-board ROM (min/max)	0 to 8 kbytes
Addressable memory	64 kbytes
Clock frequency	1 MHz
I/O ports, parallel	0
I/O ports, serial	1 (RS-232)
Board size	254 × 127 mm
	10 × 5 in.
Power required (V/I)	5 V/1500 mA
	12 V/60 mA
	−12 V/60 mA

Hardware

Model	Description	Price (100 qty)
HTA6800	CPU with no software	under $200
	With full software pkg for hard or floppy disc	4895
HTA-SM1	Calcomp Trident hard-disc controller	1895

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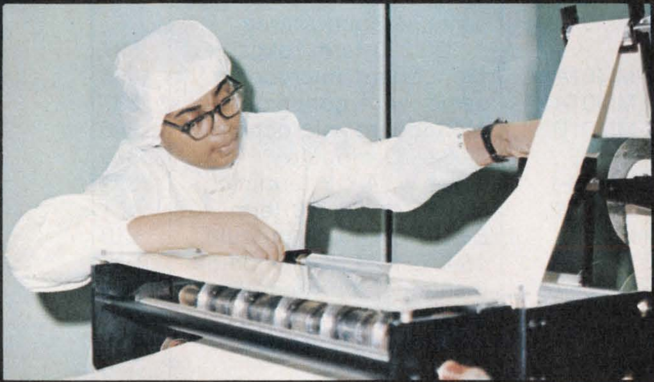

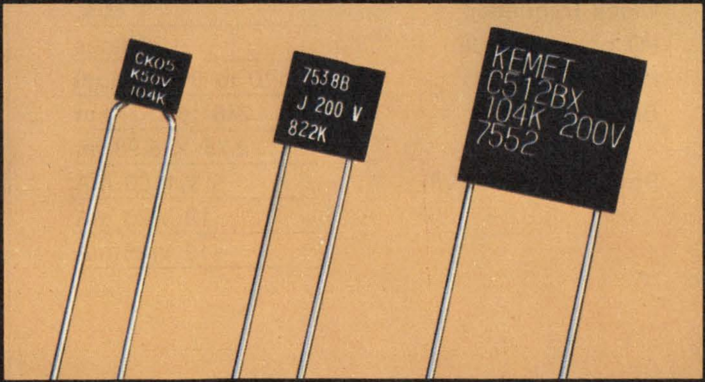

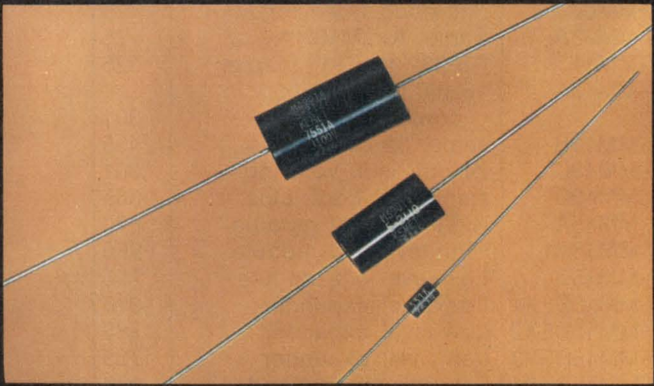

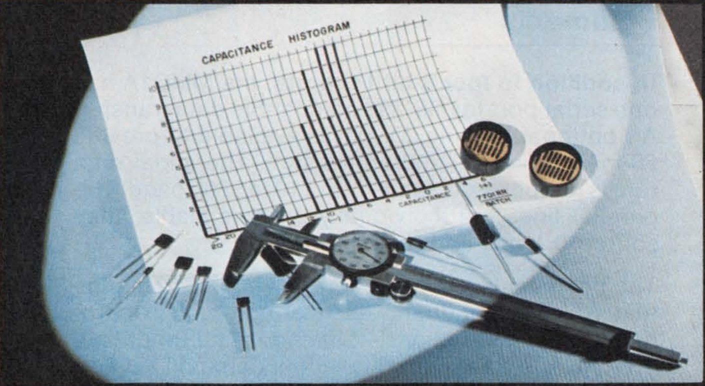

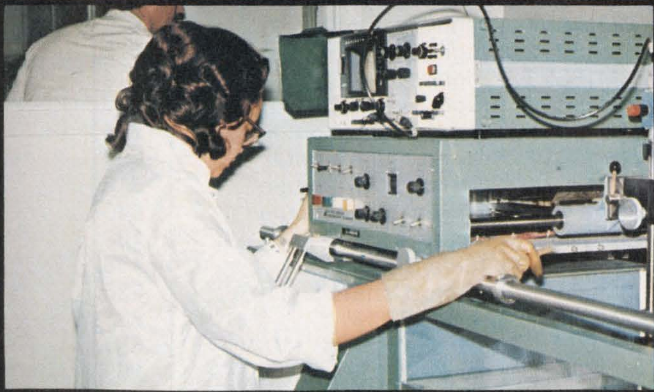

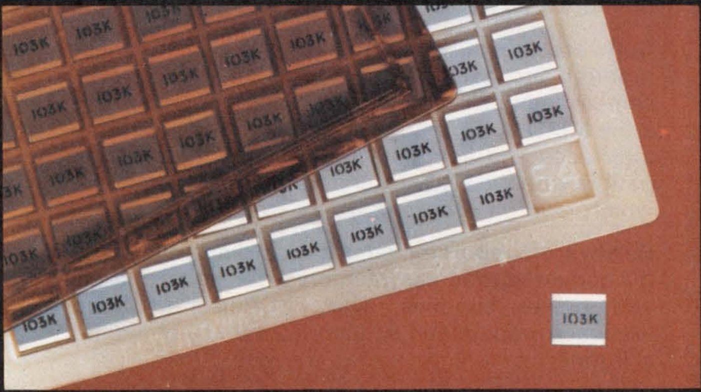

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8-bit single-board microcomputers, 01A, A2

μP used: MC6800

Alternate sources: None

Motorola Microsystems
2200 West Broadway
Mesa, AZ 85201
(602) 962-3561

The Monoboard microcomputer (or micromodule) 1A provides 1 kbyte of RAM, up to 4 kbytes of EPROM (2k for MM01A2), or 4 to 8 kbytes of ROM, two programmable peripheral interface adapters (PIAs) for parallel I/O, and an asynchronous RS-232C communications interface with four jumper-selectable baud rates (110, 300, 1200 and 9600 baud). The board can also be interfaced with other Micromodules and the EXORciser development system over its 86-pin bus. This feature permits the user to debug both software and hardware, and to troubleshoot a Monoboard-based product. Most of the interface lines are TTL compatible (40), while 16 have three-state capability.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1024 bytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	64 kbytes
Clock frequency	1 MHz
I/O ports, parallel	32 lines
I/O ports, serial	1 (110 to 9600 baud)
Board size	248 × 152 mm
	9.75 × 5.98 in.
Power required (V/I)	5 V/1100 mA
	12 V/20 mA
	−12 V/25 mA

Comments

In addition to four 8-bit I/O ports, the MMO1A has one serial port for RS-232 compatible data transfer. An optional module (MM11) is available to provide 20-mA TTY to RS-232 conversion. The serial data rate is jumper-selectable from 110 to 9600 baud. The parallel lines are individually programmable; they source 0.1 mA and sink 1.6 mA.

The basic instruction set consists of 72 commands that contain binary and decimal arithmetic operations, logic instructions, shift and rotate functions, branch and stack manipulation commands, and memory transfer operations.

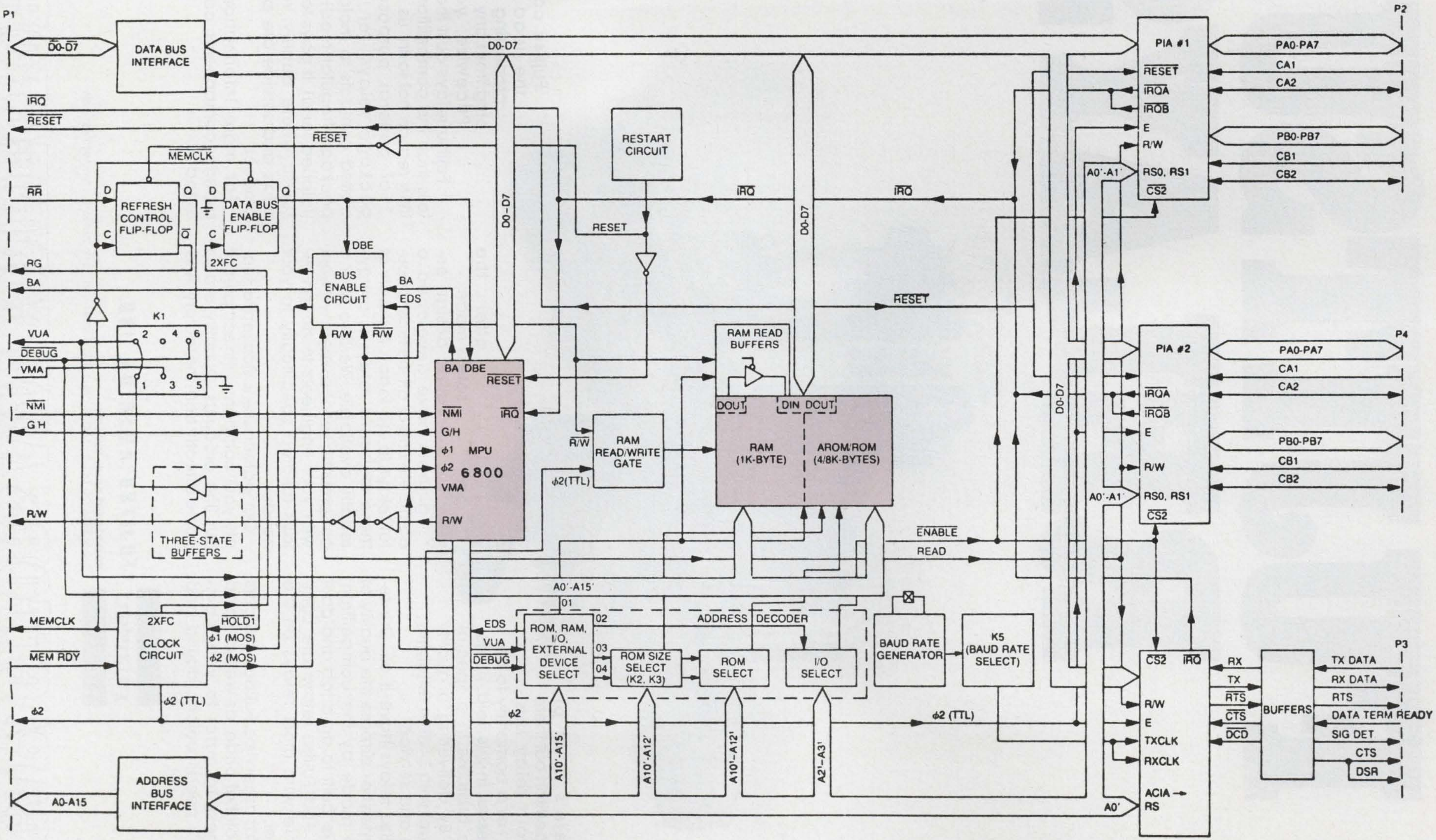
Software is available either as the ROM-resident monitor and debugger Microbug, or an editor/assembler can be read in from cassette or paper tape if the MMO1A is part of a system with the necessary interfaces and adequate RAM. The board is compatible with the EXORciser development system, for which a large program library exists.

Hardware support includes a wide range of a/d and d/a converter modules, memory extensions, chassis and power supplies. The EXORciser's EXbug firmware module can be incorporated by changing a jumper.

Note: For board architecture see p. 159.

Hardware

Model	Description	Price (unit qty)
M68MM01	Monoboard microcomp.	$ 495
-MM01-1	MM01 w. 3 connect. and 4.7 k termin. pkgs.	534
-MM01-2	same, 4 conn., three 330/220 term. pkgs	537
-MM01A	Monoboard microcomp.	495
-MM01A1	same, w. 4 connectors	537
-MM01B	Monoboard microcomp.	286
-MM03	32/32 I/O module	375
-MM03-1	same w. 4.7 k termin.	391
-MM03-2	same w. 330/220 term.	401
-MM04	8-k EROM/ROM module	210
-MM04-1	16-k EROM/ROM module	230
-MM05A	8-channel a/d module	725
-MM05B	16-channel a/d module	725
-MM05C	4-channel d/a module	725
-MM06	2 k static RAM	280
-MM08	Microbug ROM for MM01	425
-MM08A	Same, for MM01A	75
-MM11	RS-232 to TTY adapter	125
-MM13A	16 digital outputs, contact closure	301
-MM13B	same, 32 outputs	485
-MM13C	24 opt. isol. volt. inp.	301
-MM13D	same, but cont. clos.	365
-MM15A	High-level a/d module	870
-MM15A1	High-level a/d module	960
-MM15B	Low-level a/d module	755
-MM15BEX1	Low-level expander	375
-MM15BEX2	Low-level expander	580
-MM15BEX3	Low-level expander	785
-MM15BEX4	Low-channel expander	990
-MM15CV1	High-level volt. d/a	650
-MM15CV2	High-level volt. d/a	675
-MM15CV3	High-level volt. d/a	714
-MM15CV4	High-level volt. d/a	800
-MM15C11	Current d/a module	765
-MM15C12	Current d/a module	790
-MM15C13	Current d/a module	815
-MM15C14	Current d/a module	840
-MMCC05	5-card cage	168
-MMCC10	10-card cage	198
-MMLC1	10-card chassis, 110 V	635
-MMLC2	same, 220 V	635
-MMSC1	5-card chassis, 110 V	585
-MMSC2	same, 220 V	585
-MMPS1-1	Power supply, 110 V	345
-MMSP1-2	same, 220 V	345



Motorola Microsystems

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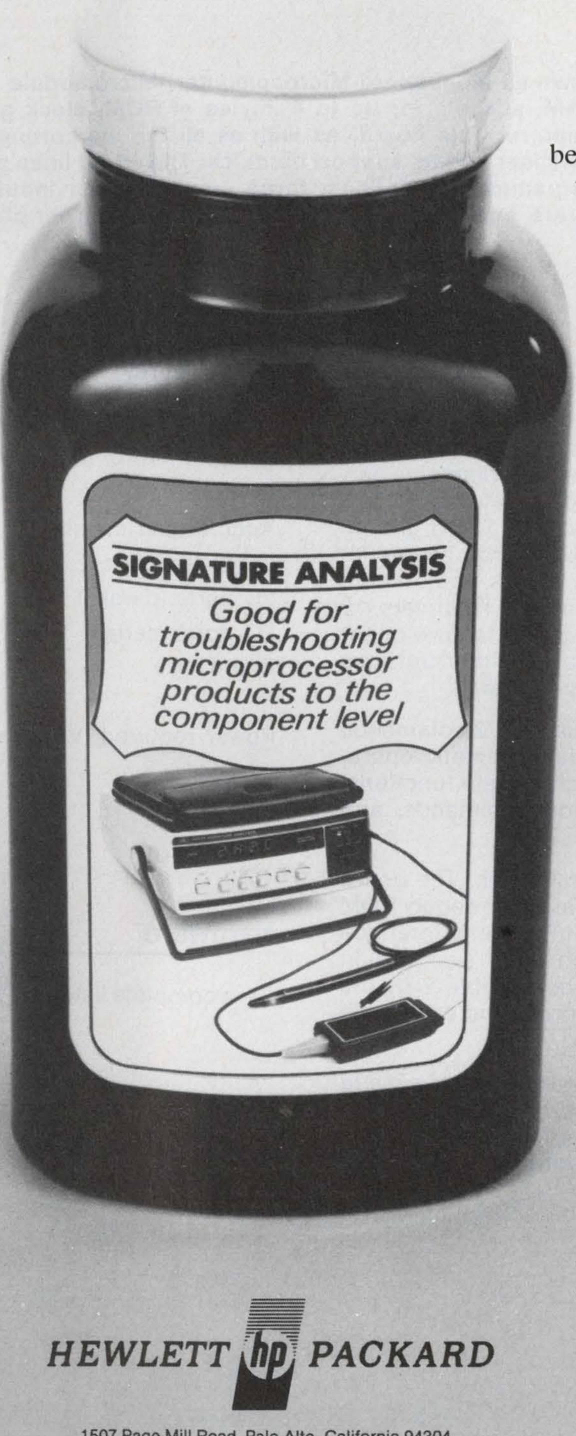

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It's a fascinating—and very workable--concept. Amazingly the price of the HP 5004A Signature Analyzer that makes all this possible is a low $990.*

To help you take advantage of this breakthrough we've prepared Application Note 222 —"A Designer's Guide to Signature Analysis." It's yours for the asking. Just contact your nearest HP field sales office or write.

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CIRCLE NUMBER 75

8-bit single-board microcomputer, MM01

μP used: MC6800

Motorola Microsystems
2200 West Broadway
Mesa, AZ 85201
(602) 962-3561

Alternate sources: None

The M68MM01, also known as Monoboard Microcomputer, Micromodule 1, contains the 6800 μP, 1 kbyte of static RAM, sockets for up to 4 kbytes of ROM, clock generator, and three peripheral interface adapters. This board, as well as all the supporting hardware are bus-compatible with the EXORciser and its support modules. The 60 I/O lines provide three groups of eight individually programmable I/O lines, three groups of four input or output lines, 12 output lines with TTL drivers, and 12 interrupt input lines, busable as peripheral control outputs.

Comments

With 120 I/O pins, the MM01 micromodule is easy to incorporate in large systems. Three peripheral interface adapters (PIA) provide programmable parallel I/O lines for transferring data between Micromodule 1 and the rest of a system. Three groups of eight lines each are individually programmable; they source 0.1 mA and sink 1.6 mA. In addition, 12 output lines have open-collector TTL drivers, 12 I/O lines work in groups of four and feature open-collector TTL outputs, and 12 busable interrupt lines can also be used to control peripherals.

The basic instruction set consists of 72 commands that contain binary and decimal arithmetic operations, logic instructions, shift and rotate functions, branch and stack manipulation commands, and memory transfer operations.

Software is available in several forms. The board can be used with a resident monitor/debug ROM (Microbug), or for a system with cassette interface an editor/assembler is offered (also available in paper tape). As the board is compatible with the EXORciser, a large library of programs developed for that system can be tapped.

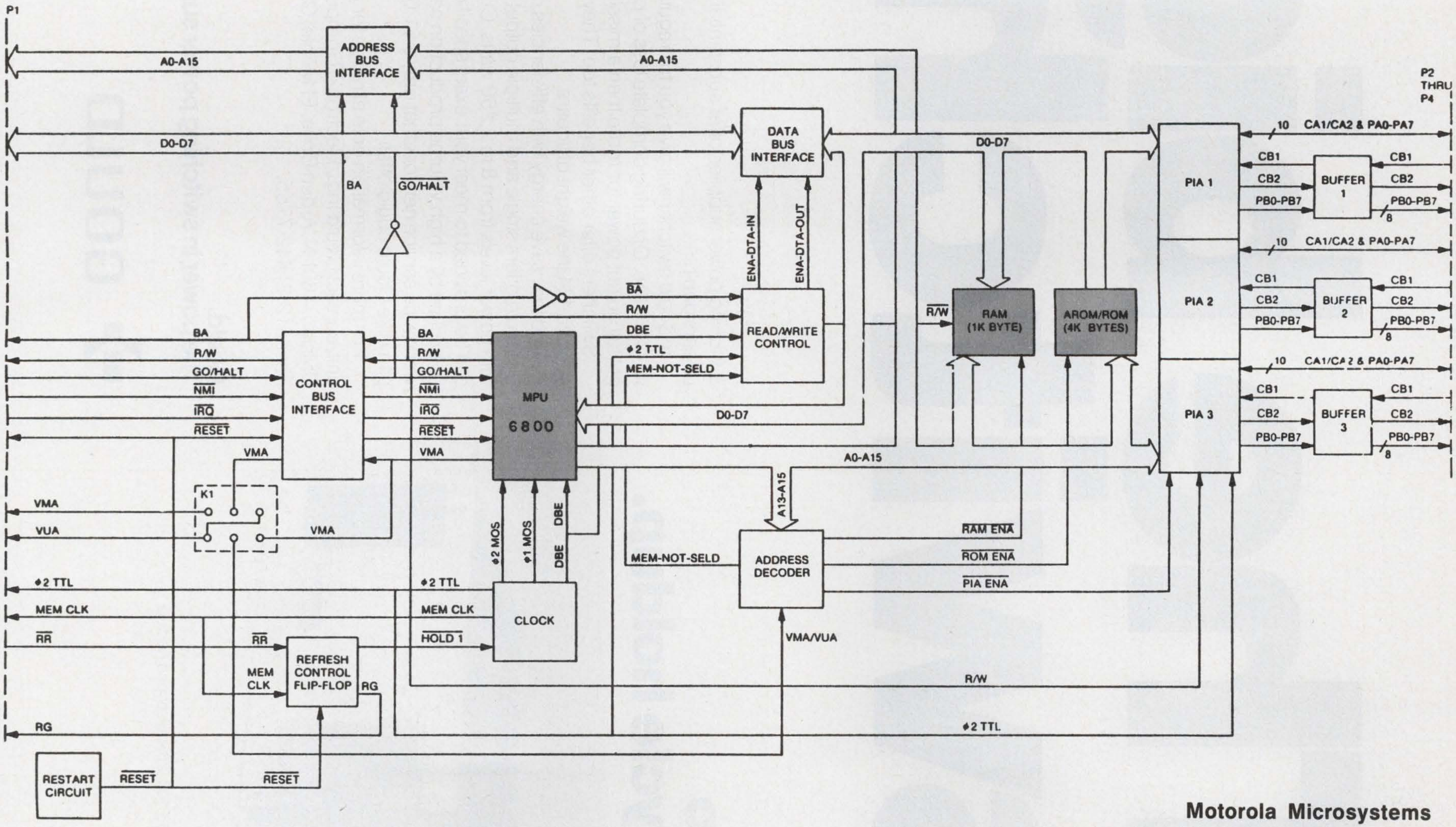
Hardware support includes a wide range of a/d and d/a boards, memory extensions, chassis and power supplies. The EXORciser's EXbug firmware module can be incorporated by changing a jumper.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1024 bytes
On-board ROM (min/max)	0/4 kbytes
Addressable memory	41 kbytes
Clock frequency	1 MHz
I/O ports, parallel	60 (see notes)
I/O ports, serial	None
Board size	248 × 152 mm
	9.75 × 5.98 in.
Power required (V/I)	5 V/1100 mA
	−12 V/500 mA

Hardware

For a complete listing of all boards see page 158.



Motorola Microsystems

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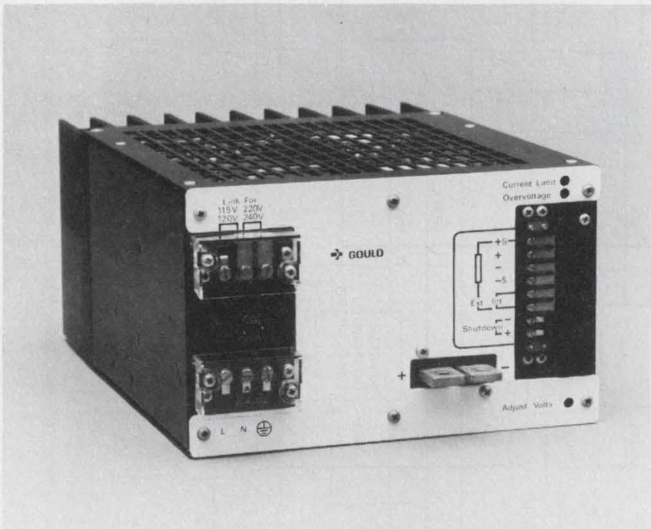

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CIRCLE NUMBER 215

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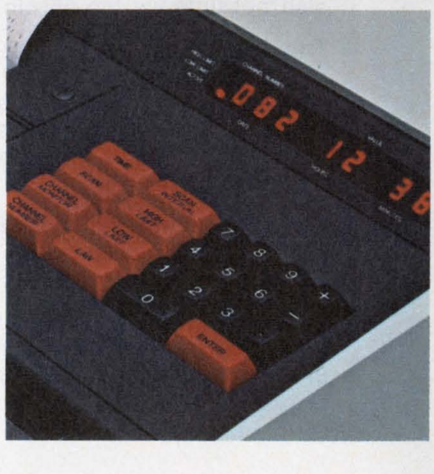

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EMR Telemetry
P.O. Box 3041, Sarasota, FL 33578
813-371-0811

CIRCLE NUMBER 77

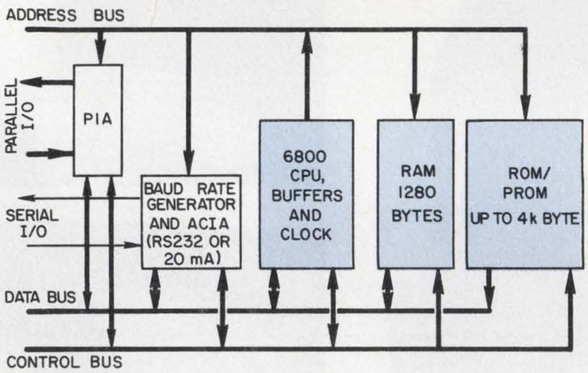
8-bit single-board microcomputer, OB8001

μP used: 6800

Alternate sources: None

**Omnibyte Corp.
2711 Curtiss Street
Downers Grove, IL 60515
(312) 852-8320**

The OB8001 microcomputer board is designed around the 6800 microprocessor and comes with 1152 bytes of static RAM, sockets for up to 4 kbytes of EPROM, 16 programmable parallel I/O lines, and a programmable serial interface. For applications requiring system capabilities, the board can address an additional 60 kbytes of memory space. Available for use with the board are monitor, assembler and editor programs as well as a disc operating system and Basic.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1152 bytes
On-board ROM (min/max)	0/4 kbytes
Addressable memory	64 kbytes
Clock frequency	1 MHz
I/O ports, parallel	16 programmable lines
I/O ports, serial	1 (50 to 19,200 baud)
Board size	114 × 165 mm
	4.5 × 6.5 in.
Power required (V/I)	5 V/2000 mA
	12 V/200 mA
	−5 V/100 mA
	−12 V/200 mA

Comments

The input and output lines of the OB8001 consist of 16 programmable parallel lines plus handshake signals from the on-board PIA, and one serial port capable of providing either an RS-232 or 20 mA current loop interface at asynchronous data rates from 50 to 19,200 baud. Interfaces to the board are also possible via the 56 pin general-purpose bus.

The instruction set is that of the board's 6800 microprocessor and consists of 72 basic instructions including binary and decimal arithmetic operations, logic instructions, shift and rotate commands, branch and stack operations, and memory transfer instructions.

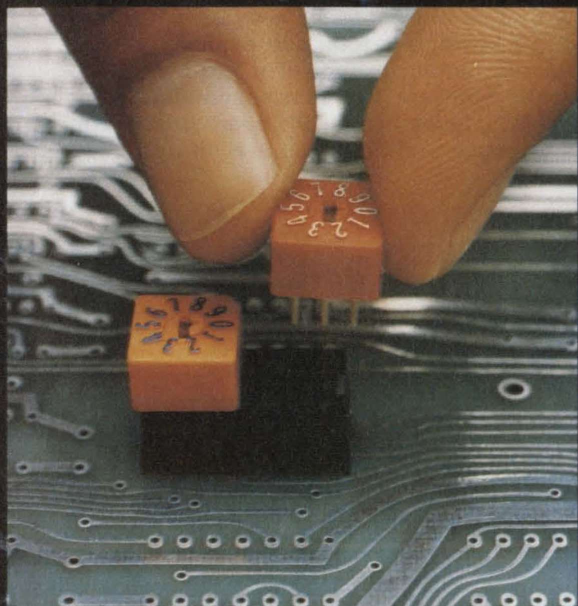
Software support includes a ROM-resident monitor, a disc operating system, an assembler and editor, and Basic.

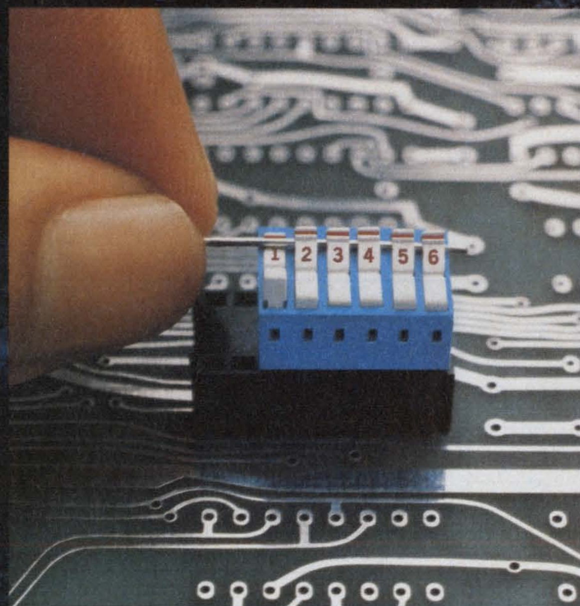
Hardware support includes the wide array of support boards listed in the table and a complete development system ($5500).

Hardware

Model	Description	Price (unit qty)
OB8001	Microcomputer board	$ 395
OB8010	4 k ROM/2 k RAM	275
OB8015	Quad PIA board	240
OB8020	Breadboard card	80
OB8025	Serial interface board	240
OB8030	Extender board	35
OB8035	8 k RAM board	595
OB8040	16 channel a/d board (12 bit)	595
OB8045	4 channel d/a board (8 bit)	295
OB8050	PROM programmer	395
OB8055	FIFO register board	295
OMNIBUG	ROM resident monitor	100
FDOS II	Disc operating system	300

Also available are system crates and peripheral devices such as terminals, floppy-disc systems and printers.




1 2 3 4 5 6

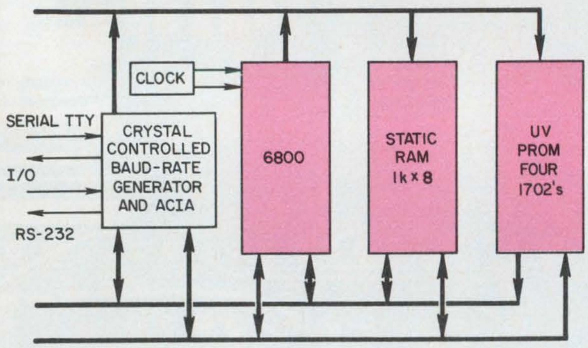
8-bit single-board microcomputer, 6806

μP used: 6800

Alternate sources: None

Pertec Computer Corp.
20630 Nordhoff Ave.
Chatsworth, CA 91311
(213) 998-1800

The 6806 is the "mainframe" board of the Altair 680 microcomputer, and needs only an external transformer to be operational. The board contains 1 kbyte of RAM and 256 bytes of ROM for the resident monitor. The ROM can be expanded to 1 kbyte, and total addressable memory is 64 kbytes. The board only provides serial input and output, except over the bus. Either TTY or RS-232 can be selected by strapping. All essential software (two-pass assembler, editor, linker, Basic) on Microfloppy, cassette or paper tape is included in the CPU board price. Front panels (turnkey or toggle/indicator) as well as card cages and housings are offered.



Comments

Input/output of the CPU board is limited to one serial port, jumper-selectable from 110 to 9600 baud; software-selectable speed is, however, available as an option.

The basic instruction set of the 6800 consists of 72 commands that contain binary and decimal arithmetic operations, logic instructions, shift and rotate functions, branch and stack manipulation commands, and memory operations.

Software suport in the form of cassette, Microfloppy, or paper tape is offered with the CPU board at no extra charge. This includes two forms of Basic with CSAVE and CLOAD commands, assembler, editor and linker. The two-pass assembler provides a cross-referenced symbol table. A bootstrap loader is contained in ROM.

Hardware support includes a range of extension boards, front panels, card cage and housing. The card cage accommodates up to three additional boards.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1 kbyte
On-board ROM (min/max)	256/1024 bytes
Addressable memory	64 kbytes
Clock frequency	0.5 MHz
I/O ports, parallel	none
I/O ports, serial	1 (110 to 9600 baud)
Board size	279 × 279 mm
	11 × 11 in.
Power required (V/I)	8 V*/2500 mA
	16 V*/500 mA
	−16 V*/500 mA

*unregulated voltages

Hardware

Model	Description	Price (unit qty)
68mb	CPU card w. PROM	Under $ 500
680b	−mb w.front panel, cage	625
680bT	Turnkey system	610
680b KACR	ACR board (Ks.City Std)	250
680b PCI	Process control board	235
680b UIO	Universal I/O board	160
680b BSU	16-k static RAM	785
680b MCD	16-k dynamic RAM	395
680 AD/DA	A/d-d/a converter	375
680 MDS	Minidisc controller	1150

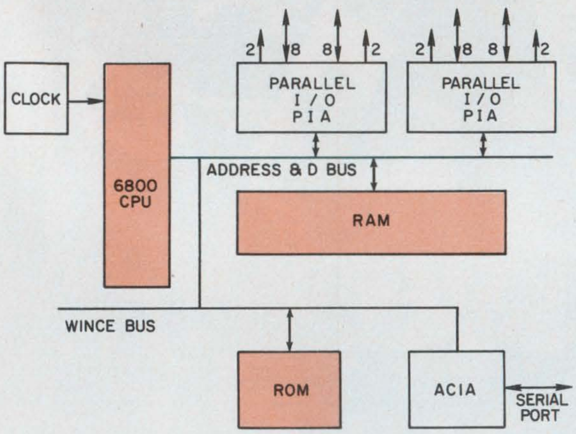
8-bit single-board microcomputer, CMM

μP-used: 6800

Wintek Corp.
902 N. 9th Street
Lafayette, IN 47904
(317) 742-6800

Alternate sources: None

The Micro Modules in Wintek's system are designed for industrial control and laboratory applications, and are among the smallest offered. A pluggable EROM programmer and keyboard/display card simplify system configuration. All interface lines are MOS and TTL compatible, and have three-state capability. The clock rate is adjustable from 0.1 to 1 MHz. Some uncommon cards are offered, including a modem. Four cards (eight optional) can be combined in the System 68 cabinet and power supply.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	512/512 bytes
On-board ROM (min/max)	1/4 kbytes
Addressable memory	64 kbytes
Clock frequency	1 MHz
I/O ports, parallel	4 × 8, bidirectional
I/O ports, serial	1 (9600 baud max)
Board size	114 × 165 mm
	4.5 × 6.5 in.
Power required (V/I)	5 V/600 mA
	12 V/50 mA
	−12 V/50 mA

Comments

I/O ports include an asynchronous serial, programmable port capable of operating to 9600 baud. Programmability includes stop bit(s), parity and data word size (7 or 8 bits). There are 32 parallel I/O lines that can be programmed as input or output, and eight more lines that serve as handshake and control lines.

The basic instruction set consists of 72 commands that contain binary and decimal arithmetic operations, logic instructions, shift and rotation commands, branch and stack manipulation functions and memory transfer operations. I/O commands are stored in the memory address space.

Hardware support consists of 11 Micromodules, including a counter/timer for frequency, event and elapsed time measurement ($99), a CMOS RAM/with battery backup and holding 2 kbytes of data ($244), card racks, backplanes, breadboard and extender cards.

Software support includes a resident 1-kbyte monitor/loader/debugger (Fantom II), an editor/assembler, 4-k Basic, cross software (assembler, PL/W compiler, linking loader), and a 16-bit Fortran simulator. A multiprocessing operating system facilitates distributed processing applications.

Hardware

Model	Description	Price (100 qty)
N/A	μP, RAM, ROM, I/O	$ 139.30
N/A	16 k dynamic RAM	279.30
N/A	16 k for 2708s	88.90
N/A	Programs 2704, 2708, 2716	139.30
N/A	Relay driver sensors	81.90
N/A	8-bit d/a, 12-bit a/d	137.90
N/A	Floppy disc interface	199.00
N/A	Cassette/CRT interface	97.30
N/A	16 keys, 15 displ. dig.	139.30

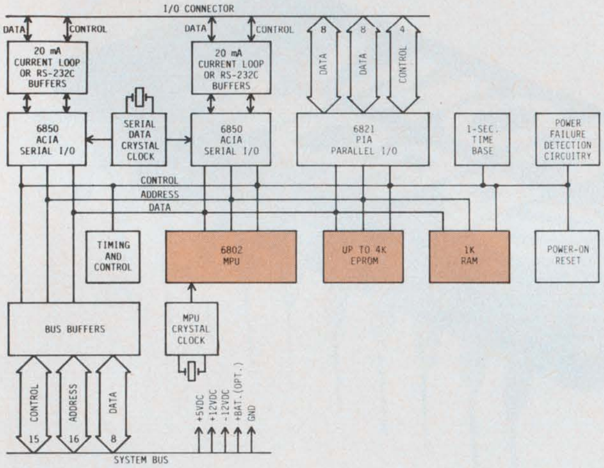
8-bit single-board microcomputer, M-5002

μP used: 6802

Henize Interactive Control
401 Astor Avenue
Dayton, OH 45449
(513) 859-8118

Alternate sources: Motorola's Micromodules are bus compatible

Designed specifically for hostile industrial environments, the M-5000 microcomputer boards provide fully-buffered buses along with power-fail detect and auto restart circuitry. The CPU board comes with 128 bytes of RAM (expandable to 1152 bytes), space for up to 4096 bytes of ROM, 20 parallel I/O lines and two serial ports, each able to handle RS-232 or 20 mA current-loop operation at programmable rates from 75 to 9600 baud. The boards are bus compatible with the Motorola family of EXORciser Micromodules.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	128/1152 bytes
On-board ROM (min/max)	0/4 kbytes
Addressable memory	61,440 bytes
Clock frequency	0.9216/2 MHz
I/O ports, parallel	2 × 8 & 4 handshake
I/O ports, serial	2 (75 to 9600 baud)
Board size	151.8 × 247.7 mm
	5.98 × 9.75 in.
Power required (V/I)	5 V/1200 mA
	12 V/180 mA
	−12 V/120 mA

Comments

The input and output lines of the M-5002 microcomputer are organized as two programmable 8-bit ports with two handshake lines per port available for control. There are also two photo-isolated serial ports on the board, and each can be set as either an RS-232 or 20 mA current loop interface. Both ports are software programmable for 7 or 8 data bits, 1 or 2 stop bits, and odd, even or no parity.

The instruction set is that of the board's 6802 processor, which, in turn has the instruction set of the 6800. There are 72 basic instructions for the 6800, including binary and decimal arithmetic operations, logic commands, shift and rotate functions, branch and stack manipulation operations, and memory transfer instructions.

Software support includes ROM/EPROM-based routines such as a disc operating system and specialized application routines—plant security monitor, real-time attendance system, hospital doctor's register and more. Custom software development services are also available.

Hardware support consists of individual modules with device driver subroutines through complete turn-key systems. And, since the boards are compatible with the EXORciser bus, all Motorola support boards will function with the M-5002 microcomputer.

Hardware

Model	Description	Price (100 qty)
M-5002	Microcomputer board	$ 420
M-5014	DMA control module	750
M-5026	8 channel ACIA/modem	420
M-5030	16 k RAM/2 k EPROM	485
M-5028	Calendar/time of day	360
FD-500	Floppy-disc interface	550
R-6000	Optical badge reader	375
T-300	Remote data transmitter	705
R-200	Remote receiver/ controller	640
R-6005	Remote badge reader	1200

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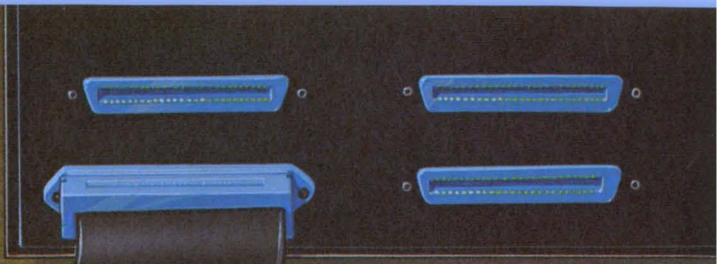

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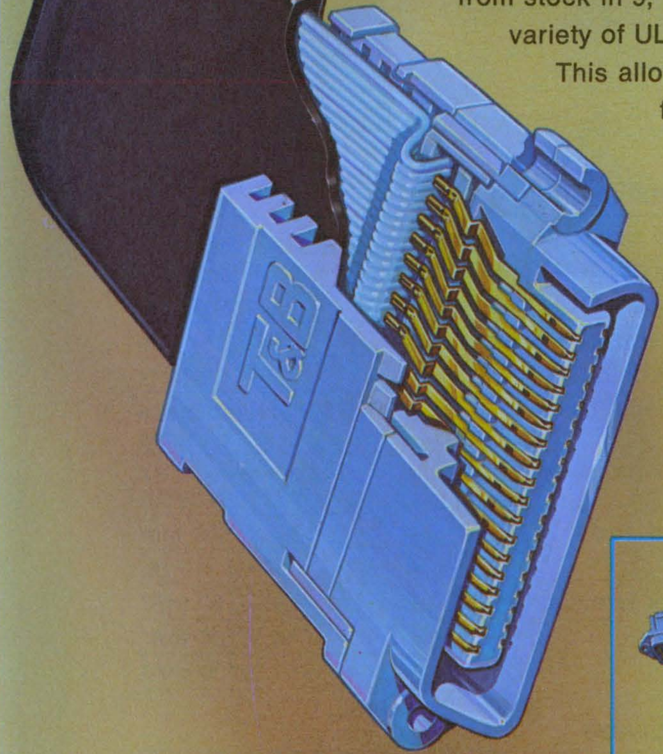

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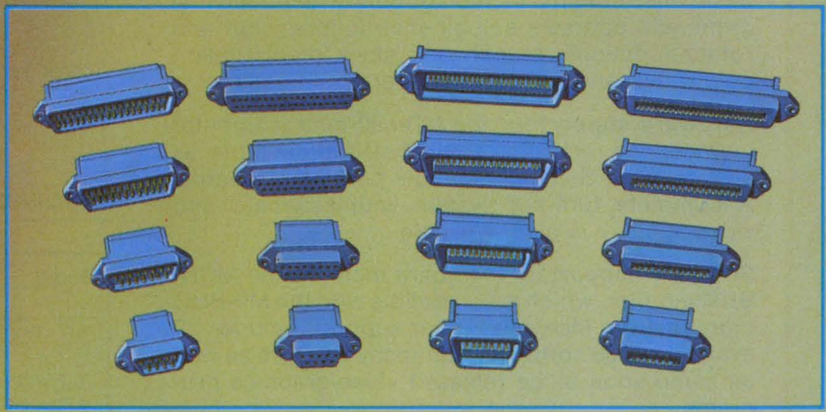
CIRCLE NUMBER 81



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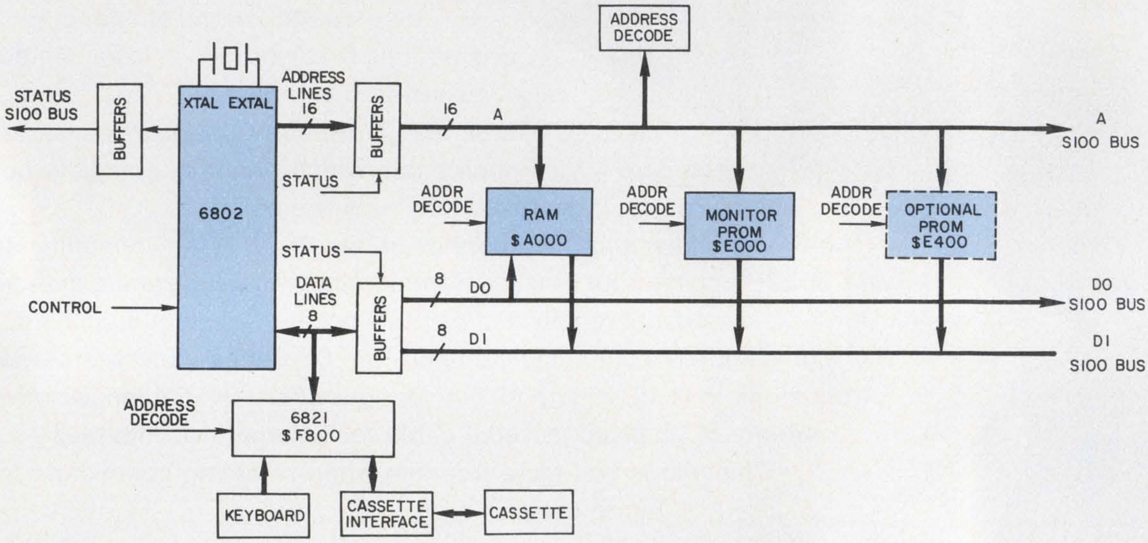
8-bit single-board microcomputer, MD-690

μP used: 6802 or 68B02

Alternate sources: None

MDS
P.O. Box 36051
Los Angeles, CA 90036
(213) 479-8761

The MD-690 is an S-100 bus compatible single-board microcomputer based on the 6802 microprocessor. It is compatible with all 6800 software and comes with a 1 kbyte PROM-based monitor program called MONBUG. On the card are an interrupt driven keyboard input and a 2400 baud Manchester cassette interface. Up to 1152 bytes of user available RAM can be put on the card as well as a second 1 k × 8 PROM. Both a 1 and 2 MHz version of the card are available.



Comments

The input and output lines of the microcomputer board consist of two 8-bit ports and the four handshake lines of a 6821 PIA. Eight lines are dedicated for a keyboard input and four more are dedicated for a 2400 baud cassette interface. However, the lines are fully programmable and can be restructured by reprogramming the memory. All I/O functions are performed via memory-mapping.

The instruction set of the 6802-based board is the same as for a 6800 microprocessor. There are 72 basic instructions including binary and decimal arithmetic operations, logic instructions, shift and rotate functions, branch and stack manipulation operations and memory transfer commands.

Hardware support for the MD-690 microcomputer includes the rack and cabinet listed in the table, as well as most S-100 compatible peripheral boards. A complete turn-key system with keyboard and video display is also available.

Software support for the board includes the MONBUG monitor, which is compatible with the MIKBUG monitor from Motorola. Other support includes all available 6800 software from many vendors as well as some soon to be released video/graphics programs.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1152 bytes
On-board ROM (min/max)	1/2 kbytes
Addressable memory	64 kbytes
Clock frequency	2 MHz
I/O ports, parallel	2 × 8 & four handshake lines
I/O ports, serial	1 (Manchester cassette)
Board size	135 × 254 mm
	5.375 × 10 in.
Power required (V/I)	8 V/750 mA*
	16 V/100 mA*
	−16 V/100 mA*

* unregulated

Hardware

Model	Description	Price (100 qty)
MD-690	6802-based microcomputer kit	$ 139
MD-691	Microcomputer crate kit	98
MD-692	Keyboard and case kit	98
MD-693	Video terminal and graphics interface kit	125
MD-695	8 kbyte low power RAM, 450 ns access	139

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42802HPT6

CIRCLE NUMBER 82

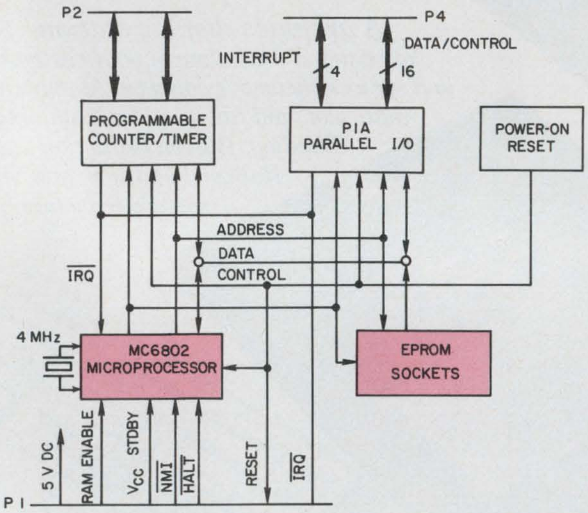
8-bit single-board microcomputer, 01B

μP used: MC6802

Alternate sources: None

Motorola Microsystems
2200 West Broadway
Mesa, AZ 85201
(602) 962-3561

Micromodule MM01B uses the MC6802 μP which contains all the registers and accumulators of the 6800, plus a clock oscillator, a driver, and 128 bytes of static RAM. The lower 32 bytes of the RAM may be retained in a low-power mode if a standby battery is provided. The MM01B supplies 16 parallel I/O lines and four interrupt lines. The I/O ports can be configured by software. A programmable timer can be used to generate system interrupts or output signals under software control. Two sockets accommodate up to 4 kbytes of EPROM storage.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	128 bytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	42 kbytes
Clock frequency	1 MHz
I/O ports, parallel	16 I/O lines
for timer:	6 I/O lines
I/O ports, serial	None
Board size	248 × 152 mm
	9.75 × 5.98 in.
Power required (V/I)	5 V/350 mA

Comments

The input/output ports of the MM01B include 16 programmable parallel lines and four interrupt lines. Under software control, the I/O ports can provide polarity, sink current and terminations for custom peripherals. Six additional I/O lines are used for the built-in programmable timer (MC6840) which can generate system interrupts or output signals.

The basic instruction set consists of 72 commands that contain binary and decimal arithmetic operations, logic instructions, shift and rotate functions, branch and stack manipulation commands, and memory transfer operations.

Software is available either as a ROM-resident monitor and debugger (Microbug), or in the form of a cassette or paper tape containing an editor/assembler, if the MM01B is part of a suitable system. The board is compatible with the EXORciser development system and can therefore use programs from the EXORciser library.

Hardware includes a wide range of memory, a/d and d/a converter boards, chassis and power supplies. The EXORciser's firmware module EXbug can be incorporated in the MM01B by changing a jumper.

Hardware

For a complete listing of boards see page 158.

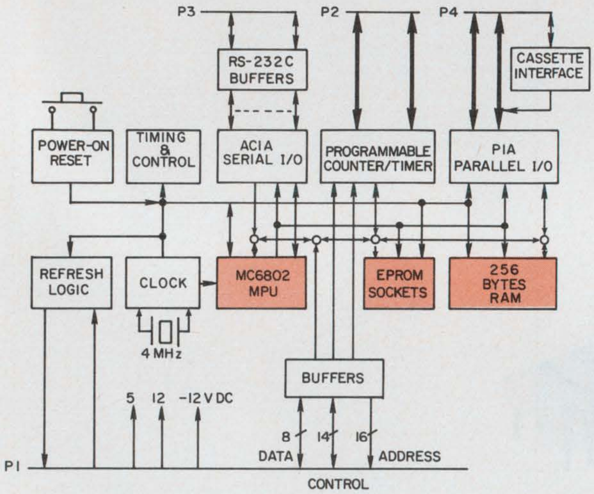
8-bit single-board microcomputer, 01B1

μP used: MC6802

Alternate sources: None

Motorola Microsystems
2200 West Broadway
Mesa, AZ 85201
(602) 962-3561

Micromodule MM01B1 uses the MC6802 μP which contains all the registers and accumulators of the 6800, plus a clock oscillator, a driver, and 128 bytes of static RAM. The lower 32 bytes of RAM can be saved during power failures if a standby battery is provided. The I/O complement of the MM01B1 includes 16 programmable parallel I/O lines, an RS-232C port with software programmable baud rate, and a cassette interface. The MM01B1 is the only board in the MM01 family that directly accepts programs from the EXORciser library, provided enough RAM is available. Refresh circuits for dynamic RAM are built in. The on-board timers can be programmed to count, measure time or generate pulses.



Comments

The I/O ports of the MM01B1 include two parallel 8-bit ports with four interrupt lines, an RS-232C serial port with program-controlled baud rate, and a cassette interface. Also available are two timers that can be programmed to count events, measure frequencies and time intervals, or generate interrupts, pulses or square waves. The output of the third timer is used internally to control the serial I/O baud rate.

The basic instruction set consists of 72 commands that contain binary and decimal arithmetic operations, logic instructions, shift and rotate functions, branch and stack manipulation commands, and memory transfer operations.

Software support includes an editor/assembler on cassette (or paper tape), and in the form of a ROM-resident monitor and debugger (Microbug). Because the board is compatible with the EXORciser, the development system's software can be used, including a large program library.

Hardware includes a wide range of a/d and d/a converter boards, memory boards, as well as chassis and power supplies. The EXORciser's firmware module EXbug can be incorporated in the MM01 modules by changing a jumper.

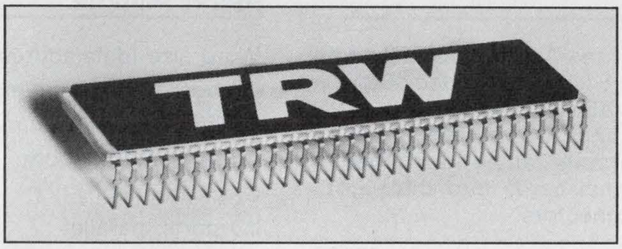
Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	128/384 bytes
On-board ROM (min/max)	0/8 kbytes
Addressable memory	42 kbytes
Clock frequency	1 MHz
I/O ports, parallel	16 I/O lines
for timer:	2 lines
I/O ports, serial	2 (RS-232, cass.)
Board size	248 × 152 mm
	9.75 × 5.98 in.
Power required (V/I)	5 V/350 mA

Hardware

For a complete listing of boards see page 158.

Finally - a cheap
(or rather inexpensive)
Video A/D Converter



Now you can afford to go digital

We've done today what everyone thought was years away. We've developed a Monolithic Video A/D Converter to sell for less than $500—it works just great—and best of all, it's ready for delivery now.

TRW's new 8 bit TDC 1007J costs only $485 (in 100's), features up to a 10 to 1 power reduction over existing converters, is less than ⅓ the size, and converts with unmatched accuracy up to 30MHz (33 ns conversion time).

The TDC 1007J exceeds the standards that networks require for studio equipment, yet is economical enough for field and/or industrial use. If you have a product that is now using one of those expensive Video A/D Converters you can mount the TDC 1007J (and about $30 worth of other components) on a card and start saving a bundle immediately. (Incidentally—we are making available, in small quantities, an evaluation board. It's a fully tested drop-in unit containing everything you need to go digital—just ask for TDC 1007 PCB.)

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An Electronic Components Division of TRW Inc.,
P.O. Box 1125
Redondo Beach, CA 90278

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CIRCLE NUMBER 84

8-bit single-board microcomputer, Apple II

μP used: 6502

Alternate sources: None

Apple Computer
10260 Bandley Dr.
Cupertino, CA 95014
(408) 996-1010

The Apple II microcomputer provides the user with a complete single-board computer system. On the board are a 6502 microprocessor, space for up to 48 kbytes of RAM and up to 12 kbytes of ROM/PROM, interfaces for a TTL serial output, video component monitor, cassette recorder, ASCII keyboard, games, and a speaker. No parallel I/O ports are on the board, however there are eight bused I/O connects with 50 pins to provide peripheral interfaces. Each interface plugged into the bus has its own software included and than saves the user the task of developing driver routines. On board memory can be either 4 or 16 k dynamic RAMs, installable by the user in 4 or 16 kbyte blocks. ROM spaces can be filled in 2 kbyte blocks.

Comments

Input and output lines of the Apple II consist of a TTL-level serial interface, a composite video output, a cassette I/O port, an ASCII keyboard input, a speaker (audio) output and two joystick inputs. Parallel I/O and control circuits can be added to the board by inserting optional cards into the eight parallel-bused 50-pin connectors.

The instruction set is that of the board's 6502 microprocessor and is very memory oriented. There are 56 basic instructions and the following addressing modes: accumulator, immediate and absolute addressing; zero page, and indexed absolute addressing; implied, and relative addressing; and indexed in direct, indirect indexed, and absolute indirect addressing.

Software support for the Apple II consists of multiple levels depending on the system purchased. Various cassette-based programs are available as well as ROM-based integer Basic or cassette-based floating-point Basic. There is also an assembly-level monitor program included with the ROM-based software.

Hardware support consists of the items listed in the table and most microprocessor-compatible peripheral devices. Soon to be announced is a mini floppy-disc system (about $700).

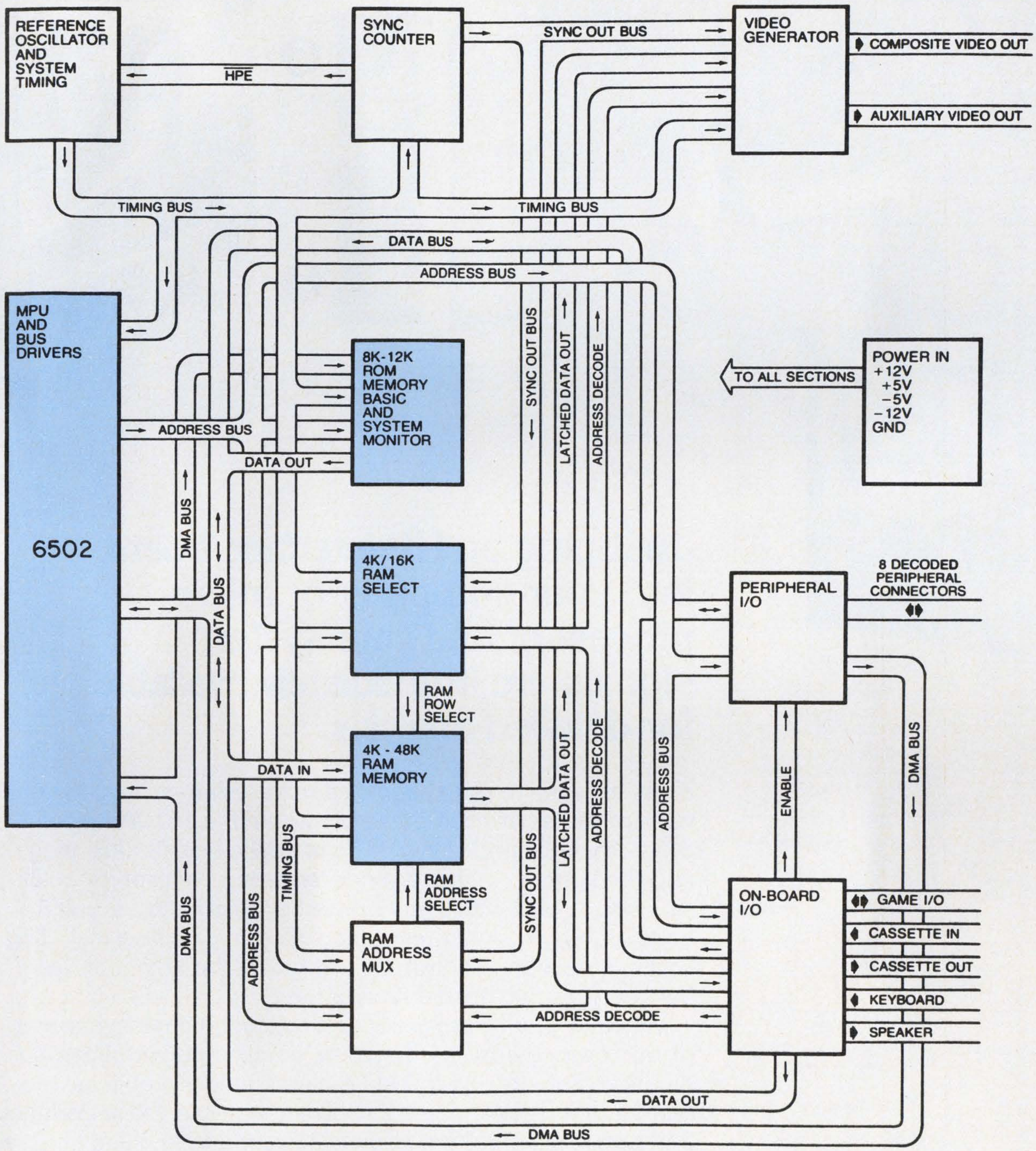
Note: For board architecture, see p. 181.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	4/48 kbytes
On-board ROM (min/max)	0/12 kbytes
Addressable memory	64 kbytes
Clock frequency	1.023 MHz
I/O ports, parallel	0
I/O ports, serial	1 (110 to 9600 baud)
	1 (cassette I/O)
Board size	215 × 345.6 mm
	8.5 × 14 in.
Power required (V/I)	5 V/1600 mA
	12 V/350 mA
	−5 V/10 mA
	−12 V/50 mA

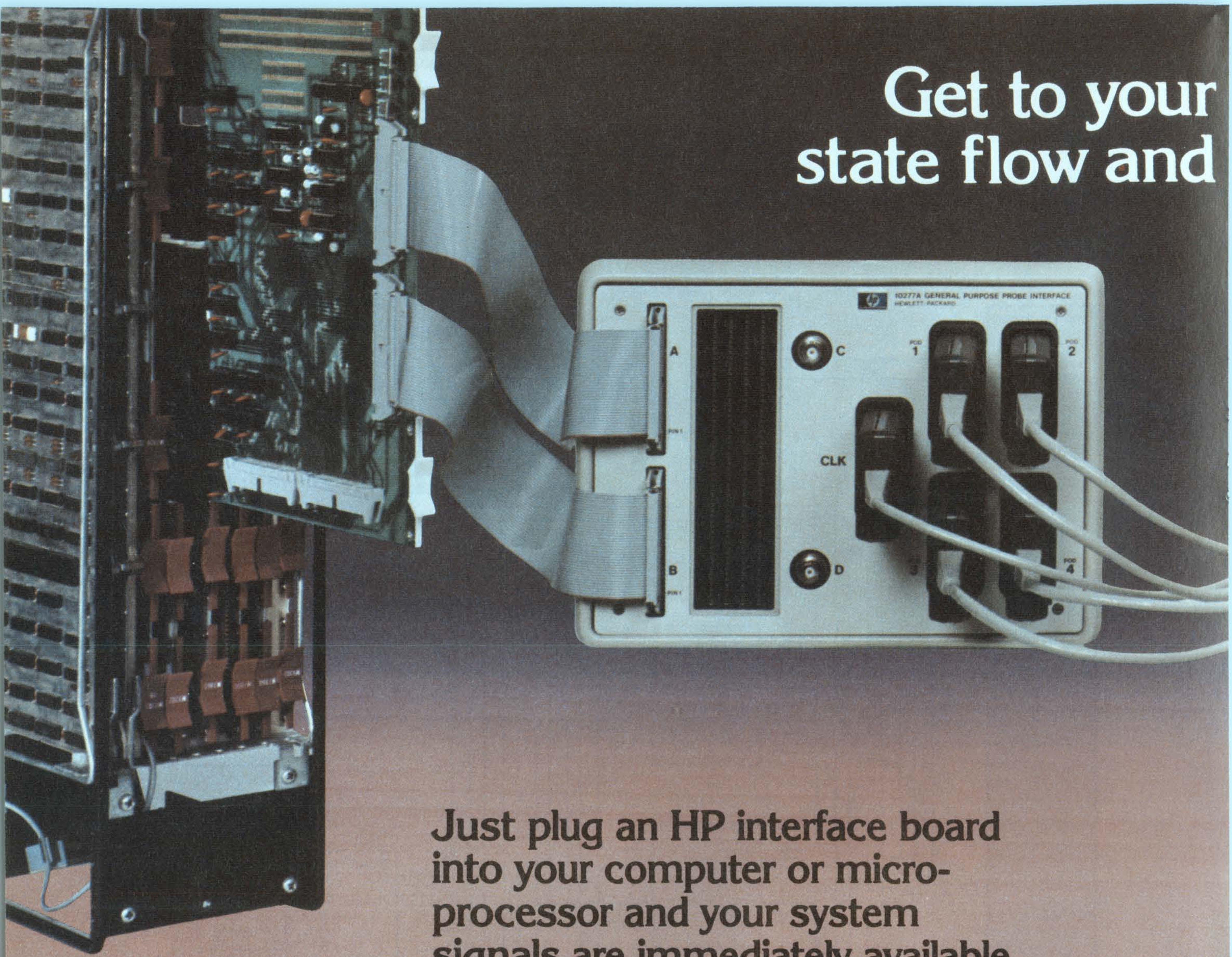
Hardware

Model	Description	Price (unit qty)
A2B0004X	(Microcomputer with 4 k RAM, 8 k ROM)	$645.00
	(4 k increment of RAM)	75.00
	(16 k increment)	300.00
A2M0002X	Keyboard	149.50
A2M0001X	Power supply	279.50
A2S004X	Packaged computer (4 k) (Apple II)	995.00
A2B0002X	Printer interface	180.00
A2B0004X	Serial interface	225.00
A2B0003X	Communication interface	180.00
N/A	Disc interface (soon to be announced)	
A2M0007	Joysticks	25.00



Apple Computer

Get to your state flow and



Just plug an HP interface board into your computer or microprocessor and your system signals are immediately available for detailed analysis.

Now, it's easy to get a clear picture of system activity in your minicomputer or microprocessor with HP's 1610A Logic State Analyzer and one of HP's interface boards. Just plug into the system . . . use a simplified menu concept for quick set-ups . . . and with a few simple keyboard entries, you'll have an easy-to-interpret display of your state flow including address, data and control line activity, or the time interval between specific bus-arbitration steps.

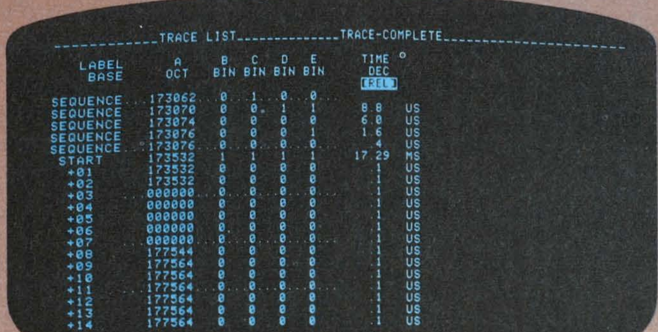
Whether you're designing or maintaining a minicomputer or microprocessor-based system, here's a powerful combination that lets you quickly solve state flow problems and analyze handshake operations. Now, you can easily evaluate and optimize your programming, lowering testing and trouble-shooting costs.

Find out how this versatile combination of HP's 1610A (priced at $9500*), minicomputer interface boards ($300*) and the 10277A general purpose interface board ($400*) can help you get at your system problems quickly. See the listing for available boards dedicated to various minicomputers. For complete details, contact your local HP field engineer today.

* Domestic U.S.A. price only.

minicomputer/microprocessor bus problems quickly.

Easy set-up.
Simple keystrokes let you define sequence requirements for a specific bus-arbitration process. And by selecting the count time, you can measure the elapsed time intervals between all of the specified sequences. Now you can accurately troubleshoot timeout problems or optimize time-dependent code.



Quick analysis of state flow or bus arbitration.
Trace-list menu lets you observe the results of the specified handshake. The time interval adjacent to each event can be either relative (between each event) or absolute (referenced to the trace start). And by defining another trace specification, you can easily monitor program flow in the numerical bases of your choice.

Boards now available include:

Model Number	**Minicomputer**
10275A	DEC PDP/11 (UNIBUS)
10276A	DEC LSI/11 (Q-BUS)
10277A	General purpose probe interface

HEWLETT PACKARD

1507 Page Mill Road, Palo Alto, California 94304

For assistance call: Washington (301) 948-6370, Chicago (312) 255-9800, Atlanta (404) 955-1500, Los Angeles (213) 877-1282

088/5

CIRCLE NUMBER 85

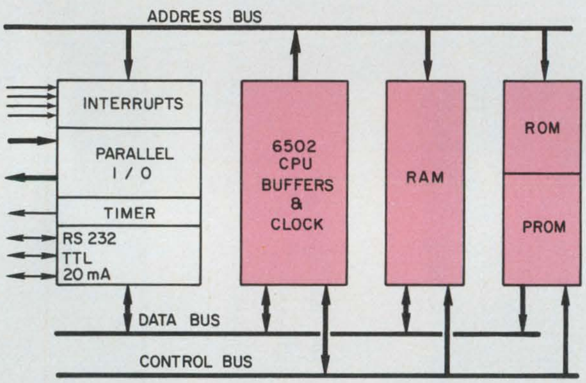
8-bit single-board microcomputer, CP110

μP used: 6502

Alternate sources: None

Synertek Systems
P.O. Box 552, 2589 Scott Blvd.
Santa Clara, CA 95051
(408) 247-8940

The CP110 microcomputer card is built around the 6502 microprocessor. It offers 1 kbyte of static RAM, 28 bidirectional and programmable I/O lines, three serial interfaces, a 1 kbyte resident ROM monitor program, space for up to 2 kbytes of EPROM or 4 kbytes of ROM and a 1 MHz crystal clock. The board can be expanded via a memory interface bus and the I/O connector. In addition to the general-purpose RAM on the board there are an additional 64 bytes of RAM for interrupt vectors and an interval timer capable of generating a system interrupt.



Comments

The input and output lines of the CP110 microcomputer are configured around one 6520 peripheral interface adapter and a 6530 I/O chip. The PIA has two 8-bit ports, with two control lines each, while the I/O chip provides an additional 10 I/O lines. All lines are completely software programmable. The serial interface consists of parallel TTL, RS-232 and 20 mA current-loop ports that can operate at data rates from dc to 9600 baud.

The instruction set of the 6502 microprocessor is available to the user. There are 56 basic instructions that are very memory oriented, with much emphasis placed on the variety of addressing modes—all 13 of them.

Software support for the CP110 consists of a 1024-byte ROM-based program, DEMON, that is a combination debug and monitor routine. Optional ROMs are available with a single-pass resident assembler, and a Tiny Basic interpreter. Cross-software for the 6502 is available from many time-sharing vendors.

Hardware support consists of several compatible boards listed in the table, including the VIM-1, a single board computer with keyboard, video interface and 32 kbytes of on-board memory capability. The System 65 development center provides a dual mini-floppy operating system and two-pass assembler, an editor and debugger. In-circuit emulation capability is a option.

Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	1024 bytes
On-board ROM (min/max)	1/5 kbytes
Addressable memory	64 kbytes
Clock frequency	1 MHz
I/O ports, parallel	3 × 8 & 1 × 4
I/O ports, serial	3 (TTL, RS-232, TTY)
Board size	108 × 177.8 mm
	4.25 × 7 in.
Power required (V/I)	5 V/800 mA
	−10 V/30 mA*+
	12 V/30 mA+

* TTY only
\+ for RS-232

Hardware

Model	Description	Price (unit qty)
CP110	Microcomputer board	$ 375
MM100	4-k static RAM card	247
MM200	2-k PROM board (1702A)	149
PD100	I/O board (digital)	149
PS100	Power supply	149
PS101	Power supply	169
VIM-1	Microcomputer with keyboard and display	269

Programmable Direct Synthesizer: 0.1 to 160 MHz

THE VALUE

Rockland Series 5600 Programmable Frequency Synthesizers employ the *direct* synthesis technique – no slow and noisy phase-locked loops – yet cost less than many PLL designs in this range! Resolution is *constant*: 1 Hz across the entire 0.1 to 160 MHz range. That's a *single* range, too; no range switching, no multipliers. Spectral purity is outstanding: –70 dB phase noise: –35dB harmonics; –70 dB spurious. Stability is exceptionally high: 1×10^{-9}/day, with a very low T.C. (1×10^{-8} from 0°C to 50°C). Or inject your own external reference. Output levelling is exceptionally tight: ±0.5 dB throughout the frequency range.

Digitally programmable at much higher speed than conventional PLL designs: 20μsec switching time, negligible switching transient. All functions are remotely programmable (*including* level).

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The greatest value: Rockland engineering and manufacturing experience. Superb quality. Maximum applications support.

THE WAYS

Model 5600 has manual front-panel controls plus full remote digital programmability.

Model 5610A has blank front panel, no manual controls, but the same full digital programmability. Considerably lower in price than Model 5600, Ideal for OEM Systems.

Model 5620 is a stripped-down chassis version for OEM build-in, and retains all electrical features. Even lower in price than Model 5610A.

THE DATA

Complete engineering specifications, price and delivery quotations. Use the reader-service card, or call or write

Rockland Systems Corporation,
230 West Nyack Road,
West Nyack, NY 10994.
(914) 623-6666.

ROCKLAND

CIRCLE NUMBER 86

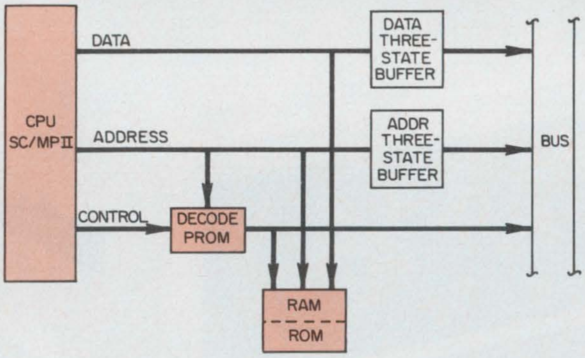
8-bit single-board microcomputers, 100, 102

μP used: 8085A, SC/MP II

Milertronics
303 Airport Road
Greenville, SC 29607
(803) 242-9232

Alternate sources: −100: National Semiconductor; −102: None

The PDC family of cards is designed to match system complexity to the actual need, with minimum "overkill." CPU card I/O is therefore limited to 1 bit serial in and out, 2 bits parallel in, and 3 bits parallel out, all MOS and TTL-compatible. On-board memory includes 256 bytes of RAM and 512 bytes of ROM, expandable to 1 kbyte. Interface and memory cards can be added as required, with a maximum of 64 k of memory. RAM-decoding is done on the CPU card with user-programmable PROM. Bus request logic simplifies use of the CPU boards in multi-processing operations. All interface lines have three-state capability except for the flag output. Custom software design is available.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	256 bytes
On-board ROM (min/max)	0.5/1 kbyte
Addressable memory	64 kbytes
Clock frequency	3.579 MHz
I/O ports, parallel	2 bits in, 3 out
I/O ports, serial	1 in, 1 out
Board size	123 × 111 mm
	4.862 × 4.375 in.
Power required (V/I)	5 V/760 mA

Comments

I/O for the CPU board is limited to one serial input and one output line, plus three bits parallel out and two bits parallel in. All are TTL compatible and, with the exception of the flag output, have three-state capability. Additional cards, connected over a 62-line bus, provide the normal parallel and serial interfaces.

The instruction set for the PDC-100 includes 24 single-byte and 22 double-byte instructions. Single-byte instructions include those for extension and pointer registers, shift, rotate, and serial I/O. All memory operations require two bytes. For the PDC-102, the instruction set includes all 78 8080A commands, plus interrupt mask read and set. They are used with the four vectored interrupts, three of which are maskable.

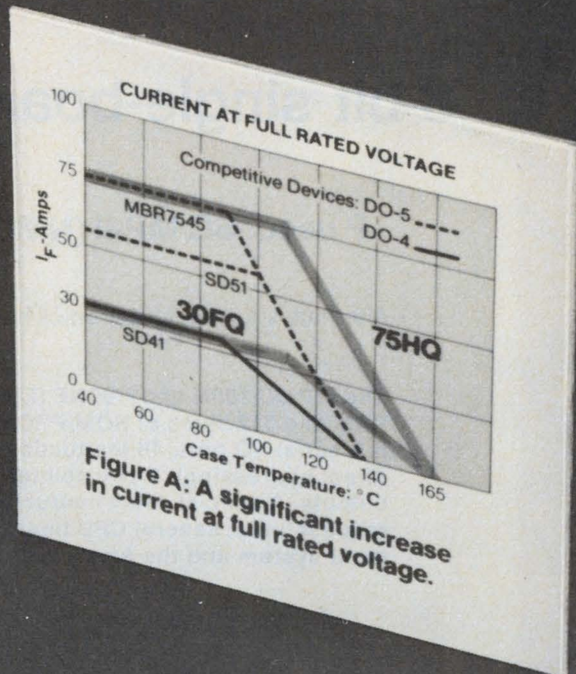
Software support for the PDC family includes a PROM loader and editor. In addition, custom software development is available.

Hardware support includes interface and memory cards. Since the PDC-100 is plug-compatible with National Semiconductor's ISP card, additional hardware support is available from that source.

Hardware

Model	Description	Price (100 qty)
PDC-100	SC/MP II CPU card	$ 206.25
PDC-102	8085A CPU card	225.00
PDC-311	Bipolar PROM card	86.25
PDC-440	Parallel interface	146.25
PDC-502	Serial interface card	176.25
ISP-8C-002	2 k RAM card (unit qty)	238.00

Now! 175°C Power Schottkys.



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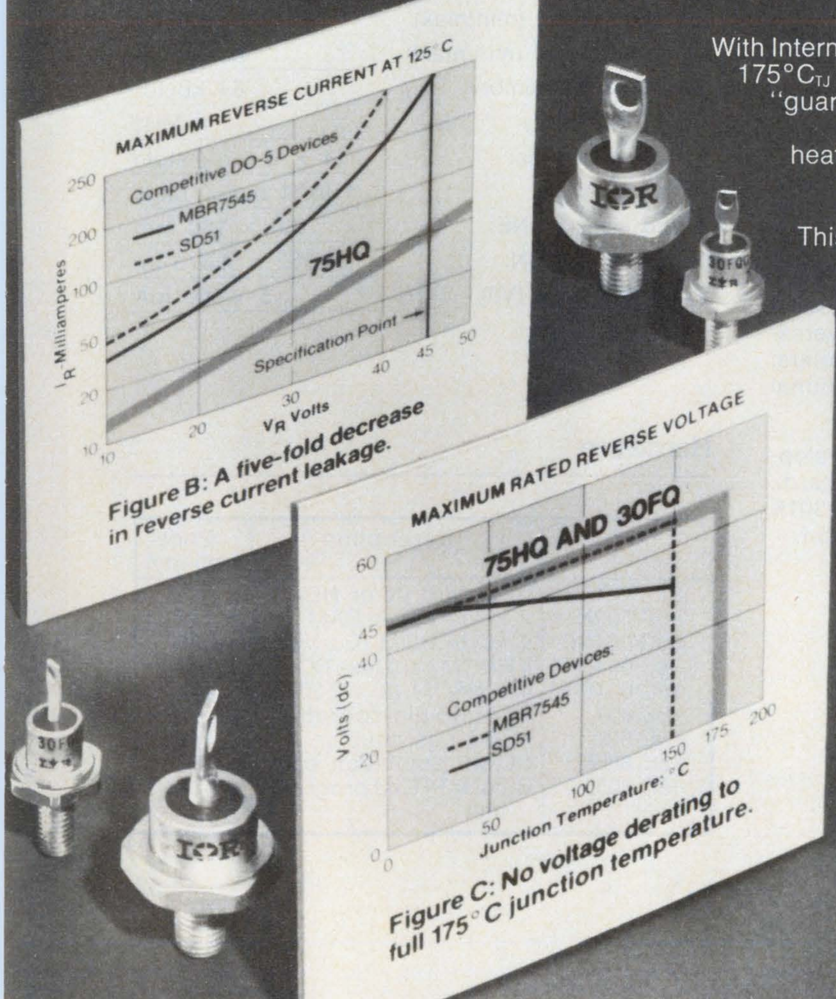

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233 KANSAS STREET, EL SEGUNDO, CA 90245 • (213) 322-3331 • TWX 9190-348-6291 • TELEX 66-4464

CIRCLE NUMBER 87

8-bit single-board microcomputer, ISP-8C/100

μP used: SC/MP-II (NMOS)

Alternate sources: Milertronics has pin-compatible board.

National Semiconductor Corp.
2900 Semiconductor Drive
Santa Clara, CA 95051
(408) 737-5000

The ISP-8C/100N and /100NE (Eurocard) are 8-bit microcomputer cards with 256 bytes of static RAM and 512 bytes of ROM/PROM on board. They have buffered data and address buses, a 20-mA serial I/O port, 46 instructions, 16-bit addressing for up to 64 kbytes of memory (4 kbytes direct addressing), three pointer registers, two sense inputs, external interrupt and three flag outputs. A special delay instruction permits delays up to 131.593 ms. By daisy chaining the bus request lines, several CPU boards can be configured for multiprocessing. A low-cost development system and the small card size (4.375 × 4.862 in., or Eurocard) are also available.

Comments

Eight parallel I/O lines are buffered three-state compatible, each sinking 2 mA and sourcing 14 mA. Serial lines include In, Out, and external flags F2, F1, F0 (all programmable up to 9600 baud).

The instruction set of 46 commands contains 24 single and 22 double-byte instructions (all memory operations). Single-byte commands include those for an extension register, the pointer register, and for shift, rotate and serial I/O.

Software support includes a high-level interpretive language (NIBL) using eight MM5204 PROMs ($260) or two MM2316A ROMs ($85), and the SC/MP utility package Supak ($300). Also available are conversational cross-assemblers that run on minicomputers, and a Fortran cross-assembler on GE and National CSS time-sharing networks.

Hardware support includes the low-cost development system ISP-8P/301N (301NE for Eurocard), each $350, a SC/MP LCDS retrofit kit (ISP-8P/301K or KE, $175), and a Seiko printer interface set.

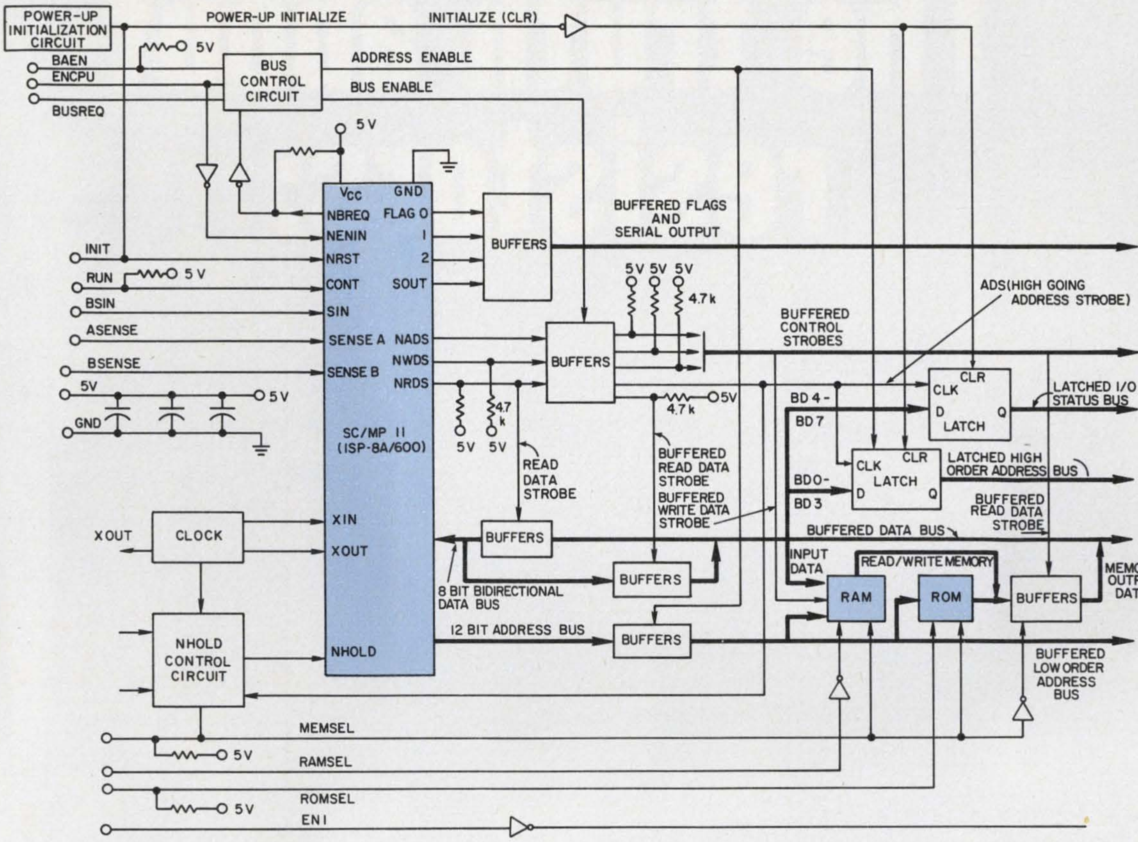
For board architecture, see page 189.

Specifications

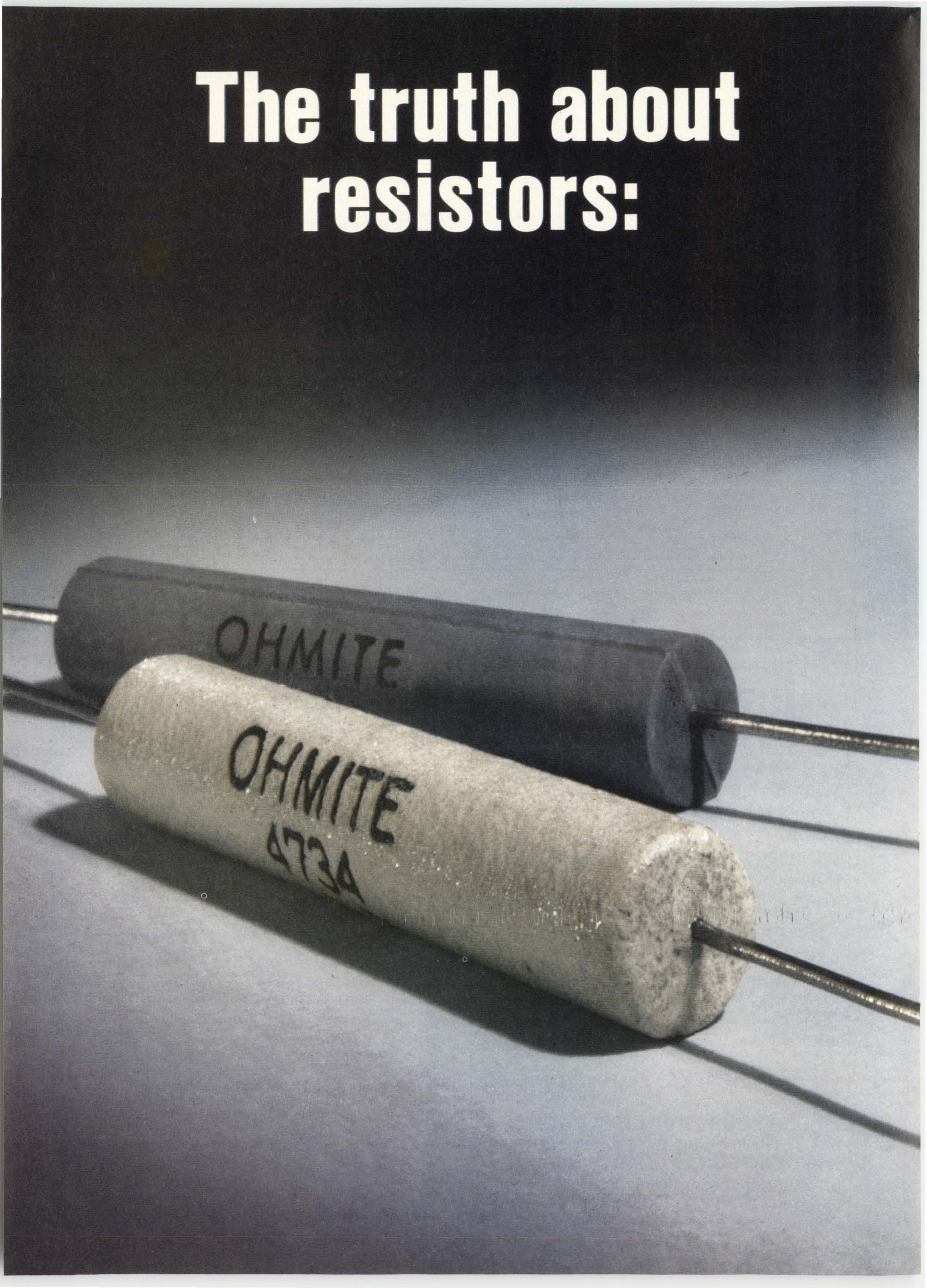
Word size (data/address)	8/16 bits
On-board RAM (min/max)	256 bytes
On-board ROM (min/max)	512 bytes
Addressable memory	64 kbytes
Clock frequency	4 MHz
I/O ports, parallel	1 × 8 three-state
I/O ports, serial	1 in, 1 out, 2 flags
Board size, 100NE:	160 × 100 mm
100N:	4.862 × 4.375 in.
Power required (V/I)	5 V/600 mA

Hardware

Model	Description	Price (100-qty)
ISP-8C/100	CPU card (N or NE)	$ 147
–8C/002N	2 kbyte static RAM	112
–8C/004NE	4 kbyte ROM (Euro)	186
–8C/004B(E)	4 k ROM card less ROM	112
–8C/004P(E)	4 k PROM (8 × 5204Q)	161
–8C/801	32 × 16-pin sockets	21
–8C/802	LCDS bus coupler	42
–8C/806(E)	SC/MP emulation card	98
–8C/805(E)	Bipolar PROM programmer	133



National Semiconductor Corp.


The truth about resistors:
OHMITE
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THERE IS A DIFFERENCE.

If you use wirewound resistors, you probably specify either silicone or vitreous enamel coatings. Before you buy either coating, make sure you talk to someone who knows both. Because some companies that offer only one type of coating would have you believe that silicone and vitreous enamel work equally well in <u>all</u> applications and are therefore interchangeable.

Don't believe it.

The truth is this: many significant differences—in aging characteristics, resistance to heat, puncture, overloads and mechanical shock—not only can make a critical difference in your product's performance, but in your company's reputation, as well.

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Many telephone equipment manufacturers have found, for example, that silicone deposits can foul relay contact surfaces, causing expensive maintenance and trouble-shooting headaches. So these manufacturers demand vitreous enamel-coated resistors for critical switching equipment.

Now, we're not saying that vitreous enamel is always the answer. Some applications call for vitreous. Some call for silicone. That's why Ohmite offers both. We can show you where one resistor works better and why; explain the options, costs and trade-offs involved. In fact, we can tailor a complete package to your overall resistive product requirements.

Before choosing one coated resistor over another, talk to the people who know resistors best: Ohmite.*

Ohmite Manufacturing Company, 3601 Howard Street, Skokie, IL 60076; 312-675-2600.

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Get a copy of our free brochure, "The truth about resistors:" It contains a wealth of performance characteristics and application experience covering silicone and vitreous enamel-coated resistors. Circle the reader service number for your copy today.

CIRCLE NUMBER 89

OHMITE®

makes the difference

**After all, who are you going to believe? A company that offers only silicone? Or vitreous enamel? Or a company that offers both?*

0-77-1

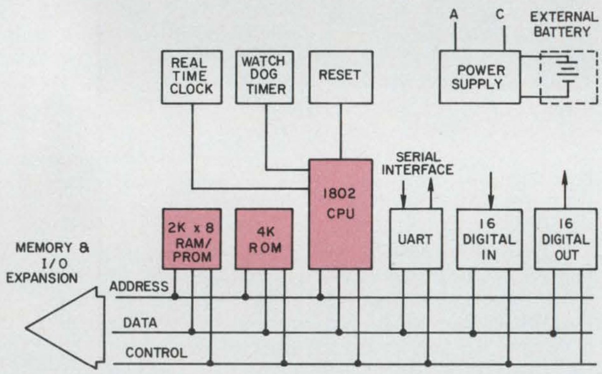
8-bit single-board microcomputer, MPPS 100

μP used: 1802 (CMOS)

Alternate sources: None

Realistic Controls Corp.
404 W. 35th Street
Davenport, IA 51806
(319) 386-4400

The single-card OEM microcomputer belongs to the Micropower system line, with extremely low power consumption (50 mW max). The card includes the CPU, clock, RAM, nonvolatile ROM, I/O ports and drivers, and serial interface. The ac power supply and battery charger (for back-up) are on the board. Any of the processor's 16 scratchpad registers can be used as program counters, permitting 64-kbyte direct addressing. Multidrop communication permits multiprocessing.



Specifications

Word size (data/address)	8/16 bits
On-board RAM (min/max)	2 kbytes
On-board ROM (min/max)	0/4 kbytes
Addressable memory	64 kbytes
Clock frequency	2.4576 MHz
I/O ports, parallel	16 lines in, 16 out
Board size	251 × 178 mm
	9.87 × 7 in.
Power required (V/I)	115 V ac, 60 Hz
	or 5 V/10 mA

Comments

All 16 input and 16 output lines are MOS and TTL compatible. Interface lines on the 60-conductor main bus have three-state capability. The CMOS UART has a jumper-selectable baud-rate generator and provides full-duplex double-buffered transmission.

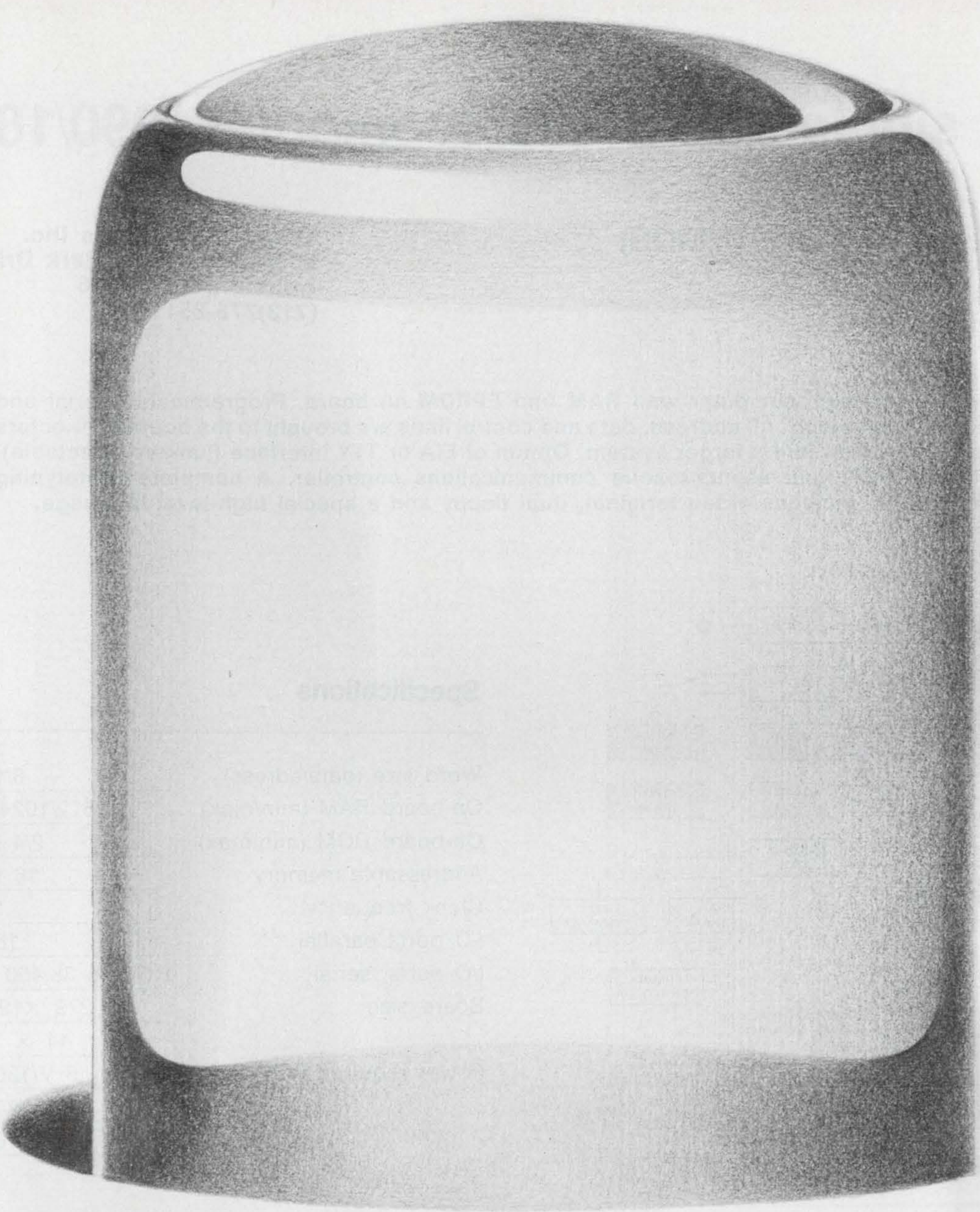
The 91 basic instructions include 10 for control, seven each for memory reference and register operation, 12 each for logic and arithmetic, as well as 28 branch, nine skip, and 14 I/O instructions.

Most hardware needed is on-board, including up to 2 kbytes of RAM/ROM combinations, and up to 4 kbytes of nonvolatile ROM, in 512-byte increments (RCA 1821 masked ROMs). Memory and I/O expansion boards are available, and are supported to a total of 64 kbytes. The operator interface board has a 32-key keyboard and 24 character 16-segment display.

Software support includes extensive development programs available on several nationwide time-sharing networks.

Hardware

Model	Description	Price (unit qty)
MPPS	Processor system	$ 895
MPM-101	4 kbyte RAM	595
MPPI	Operator interface	525
MPA	32-input analog board	495



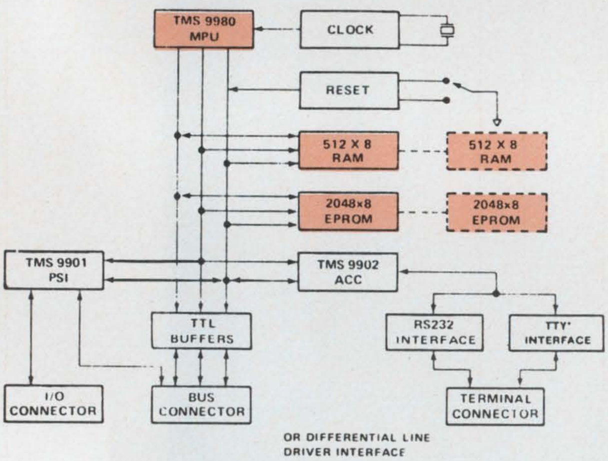
8-bit single-board microcomputer, 990/180M

μP used: TMS9980 (NMOS)

Alternate sources: None

Texas Instruments Inc.
8600 Commerce Park Drive
Houston, TX 77036
(713)776-6511

A single-board microcomputer with RAM and EPROM on board. Programmable serial and parallel I/O is provided. All address, data and control lines are brought to the board connectors for easy expansion into a larger system. Option of EIA or TTY interface (jumper-selectable), prototyping area; and asynchronous communications controller. A complete prototyping system, AMPL, includes video terminal, dual floppy and a special high-level language.



Specifications

Word size (data/adress)	8/14 bits
On-board RAM (min/max)	512/1024 bytes
On-board ROM (min/max)	2/4 kbytes
Addressable memory	16 kbytes
Clock frequency	3 MHz
I/O ports parallel	16 lines
I/O ports, serial	1 (75 to 38,400 baud)
Board size	279 ×190 mm
	11 × 7.5 in.
Power required (V/I)	5 V/1300 mA
	12 V/200 mA
	−12 V/100 mA

Comments

Serial and parallel I/O are programmable. The interface chip handles 16 parallel I/O lines (TTL compat.) while serial I/O is RS-232 or 20-mA current loop on the −1, or differential line driver on the −3.

The instruction set includes 16 arithmetic (multiply/divide), 20 program control, 14 data control, six logical, four shift, five bit I/O, six external instructions totaling 69 commands.

Software support for the board includes a line-by-line assembler ($100), interactive debug monitor TIBUG ($100), and transportable cross support software (assembler, simulator, ROM utility).

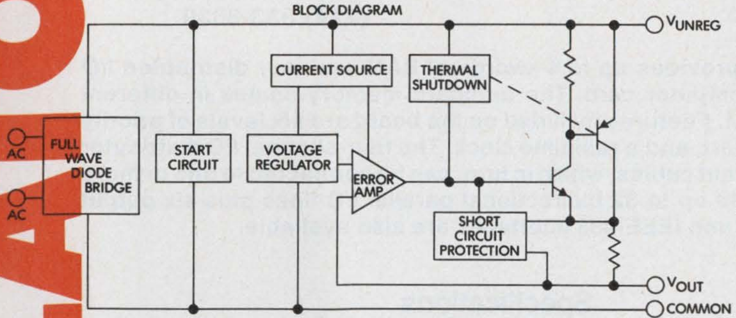
Supporting hardware includes an I/O expansion board, a microterminal for data entry and editing, and 4-slot chassis, extender board, prototyping card and connector kit.

Hardware

Model	Description	Price (unit qty)
TM990/180M-1	μC board w. TIBUG monitor (2 EPROMs)	$ 435
TM990/180M-3	μC board w. 4 unprogrammed EPROMs, 8 RAMs	495
TM990/310	48 I/O points, progr'ble	295
TM990/301	Microterminal to enter & edit programs	125
TM990/510	OEM chassis, 4 slots	190
TM990/511	Extender board	130
TM990/512	Prototyping card	80

AC INPUT REGULATOR

Now there's one less bridge to cross to get to your power supply.



Fairchild's new SH1705 makes it a whole lot easier to arrive at power supply designs. It's a 5 V, 5 A positive voltage regulator with a twist. There's a full wave diode bridge built-in.

So now, you can design in about half the time, using fewer parts, less board space and at least one less assembly step.

The SH1705 is in a hermetically sealed TO-3 package so it can fit into even the tightest squeezes on your pc board. It features low dropout voltage across the regulator section. Internal current and thermal limiting. And 50 W power dissipation.

Bridging the gap between build or buy.

Until the SH1705, you had two choices. Build-up from discretes which is time-consuming and costly. Or buy a complete open frame power supply which is bulky. And costly, no matter what your quantities are.

Designing with the SH1705 gives you the best of both worlds without the disadvantages. And it's easy. All you need is the transformer, capacitors, heat sink and the SH1705.

Bridge over troubled power supplies.

If you're having trouble with power supply designs, or just interested in saving time, space and money, we'll send you one of our new positive voltage regulators with a bridge inside. Contact your Fairchild sales office, distributor or representative today. Or use the direct line at the bottom of this ad to reach our Hybrid Division. Fairchild Camera and Instrument Corporation, 464 Ellis St., Mountain View, Calif. 94042. Tel: (415) 962-3771. TWX: 910-379-6435.

FAIRCHILD

Call us on it. (415) 962-3771

CIRCLE NUMBER 94

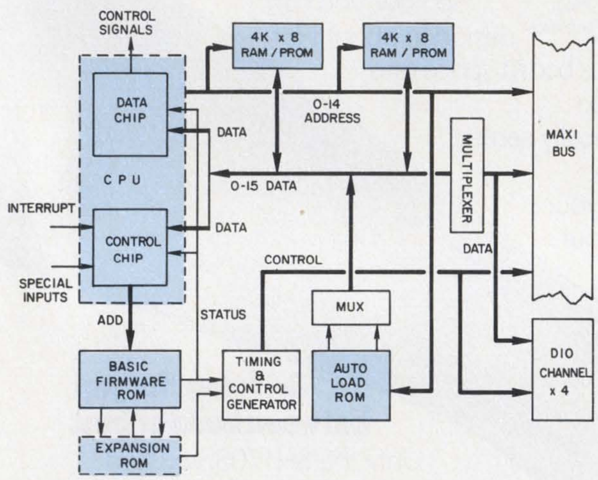
16-bit minicomputer, LSI 4/10

Custom LSI based processor

Computer Automation
18651 Von Karman
Irvine, CA 92713
(714) 833-8830

Alternate sources: None

The LSI 4/10 single-board computer provides up to 4 kwords of RAM and four distributed I/O channels, all on a single half-size computer card. The on-board memory comes in different configurations of RAM and RAM/PROM. Features included on the board are six levels of priority interrupt, power-fail protect, auto-restart, and a real-time clock. The four-channel I/O distributor on the board accepts up to four intelligent cables, which in turn, can be connected to one or more peripherals. Board capabilities include up to 32 bidirectional parallel I/O lines plus six output control and five input control. RS-232 and IEEE-488 interfaces are also available.



Specifications

Word size (data/address)	16/16 bits
On-board RAM (min/max)	1/4 kwords
On-board ROM (min/max)	0/4 kwords
Addressable memory	64 kwords
Clock frequency	16 MHz
I/O ports, parallel	32 lines and handshakes
I/O ports, serial	0
Board size	190.5 × 429 mm
	7.5 × 16.9 in.
Power required (V/I)	5 V/5400 mA

Comments

The input and output lines of the LSI 4/10 board provide up to 64 distributed I/O channels, each with a bandwidth of 31,350 bytes/s. The channels operate in simplex, half-duplex or full duplex modes. Software enables functions such as parity check, character detection and CR detection. All boards interconnect via the Maxi-bus, an 86 pin interface.

The instruction set of the board consists of 76 basic commands grouped as follows: 34 arithmetic, logic and memory or register-reference commands, four bit manipulation operations, 16 jump instructions, two stack commands, eight I/O functions, six machine control instructions, four status control operations, and two trap commands. Additional instructions are available on the larger, but software compatible, 4/30 and 4/90 processors, as well as some extensions that can run on the 4/10 itself.

Software support for the LSI 4 family of CPUs includes both assembly-level and high-level language capability. Assemblers, editors, Basic, Fortran IV and Pascal are available. There are also operating systems and executive programs as well as system utilities and diagnostics available for the user purchasing a complete system.

Hardware support consists of a wide array of memory and I/O boards as well as disc operating systems, card cages, power supplies, and the peripheral themselves. There are also independent vendors that offer pin-compatible support boards.

Hardware

Model	Description	Price (unit qty)
LSI 4/10	Stand-alone computer card	$ 645
LSI 4/30	MSI version of CPU only	1395
LSI 4/90	Highest performance CPU	2090
IOD-4	4 channel I/O distributor	250
IOD-8	8 channel distributor	290
MEM-4/32	4 to 32 k RAM board	550/3170
MEM-4/16	4 to 16 k of core storage	985/3050
DOS4	Disc operating system	2000
RTX4	Real-time executive	500
S/W	Fortran, Basic, Pascal	1500/400/900

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ADDRESS: ______________________

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Viking CONNECTORS

Viking Industries, Inc., 21001 Nordhoff Street, Chatsworth, CA, U.S.A.

CIRCLE NUMBER 95

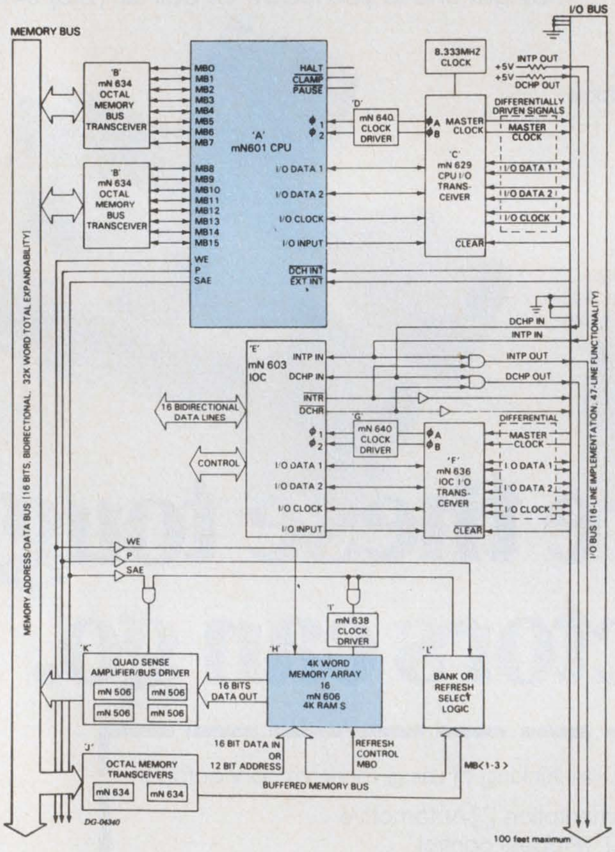
16-bit minicomputer, μNova

μP used: mN601

Alternate sources: None

Data General Corp.
15 Turnpike Rd., Rte. 9
Southboro, MA 01581
(617) 485-9100

The microNova single-board minicomputer uses two independent buses to communicate with memory and I/O devices. The 20-line bidirectional memory bus accesses and refreshes the memory, while the I/O bus drives devices up to a distance of 100 ft. The I/O bus contains a 2-bit bidirectional differential data line, timing lines and control lines. Because the microNova is software compatible with the Nova computer line, it can draw on a huge pool of programs written in assembly language, Basic or Fortran. Peripherals range from a handheld calculator-like "console" (20 keys, 6-digit display) to one and two-drive diskettes. System configurations range from single boards to whole racks.



Specifications

Word size (data/address)	16/15 bits
On-board RAM (min/max)	2/4 kwords
On-board ROM (min/max)	512/4096 words
Addressable memory	32 kwords
Clock frequency	8.3 MHz
I/O ports, parallel	none
I/O ports, serial	1 (16.6 Mbit/s)
Board size	214 × 190 mm
	9.5 × 7.5 in.
Power required (V/I)	5 V/1900 mA
	15 V/500 mA
	−5 V/250 mA

Hardware

Model	Description	Price (100 qty)
8562	CPU with 4-kword RAM	$ 496
8563	CPU with 8 kword RAM	589
8573	8 kword dynamic RAM	589
8570	4 kword PROM	465
4207	Asynchr. interf. (1 port)	155
4210	Par. I/O (48 each)	155
4222	Digital I/O (16 each)	248
4223	12-bit a/d (16 SE)	713
4224	12-bit d/a (2 chan.)	496
4226	Synchron. line ctrlr.	248
4227	Multi-line communic.	310

Comments

Input/output within the microNova system is bit-serial at a 16.6 MHz rate. Parallel I/O is available by adding the appropriate board.

There are 72 basic instructions that fall into six groups: Arithmetic and logic (10 instructions), memory reference (six instructions), I/O (11 instructions), stack manipulation (12 instructions), and central processor control (nine instructions). Addressing can be absolute, PC-relative, indexed, conventional indirect (eight levels), and indirect through auto-incrementing (five levels).

Software support is extensive, because it includes most Nova and Eclipse programs. Two operating systems are available with two assemblers, editors, library files, debugger, and relocatable loader. Both a single and a multitasking Fortran IV, as well as extended Basic are offered.

Hardware support includes a wide range of cards, as well as mounting hardware from single boards to whole racks. The microNova can be operated with a hand-held keyboard/display.

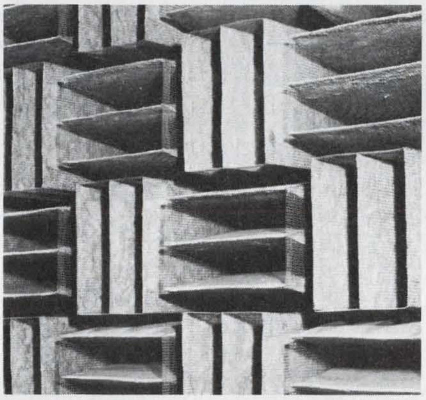
Torinmoves

The smaller 3" fan

Yes. It takes less space. TA300 stands for Torin three inch tube axial — but it's 1½ inch thick all over and that's thin. The improved aerodynamics of the impeller demands less power, permitting the design of a superbly compact motor. The motor compactness in turn adds to the impeller efficiency by creating an optimum ratio of impeller hub to tip size. A good worker for mini-computers, business machines, and the other space demanding electronic devices. The TA300 is very efficient, provides a good flow of air, and is quiet about it. *Circle 120*

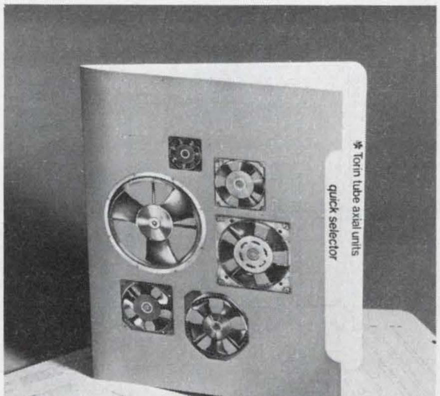
Sound advice

Since testing methods for sound characteristics vary from one manufacturer to another, it is difficult to compare results. Henceforth all our descriptive literature on blowers will carry comprehensive test results on four vital factors: NPEL, PSIL, Sound Power Level and Sound Pressure Level . . . with the latter two in chart form, plotted against Octave Band Center Frequency Herz. Our test methodology simulates in-service operating conditions as realistically as possible, and the process is fully explained.



Quick pick

To make it easy as possible for you to scan our tube axial blower line, we've come up with what we call our "Quick Selector Folder." It shows our complete selection of tube axials from 3 to 10 inches in diameter. Ask us to send you the folder. *Circle 121*



All muscle, no fat

Our TA600 is the thinnest blower of its type produced in this country . . . only 1½ inches thick. It will slip into spaces in computer equipment and business machines that won't accommodate fat 6 inch units. Its strength is in producing an extremely high CFM per watt ratio. And the one-piece die-cast zinc housing adds rigidity and acts as a heat sink. *Circle 122*

Torin Corporation Kennedy Drive Torrington, Connecticut 06790 (203) 482-4422

Facilities United States: Torrington, Connecticut, Van Nuys, California
Australia: Sydney; **Belgium:** Nivelles; **Brazil:** São José dos Campos; **Canada:** Oakville, Ontario; **Spain:** Alcalá de Henares; **United Kingdom:** Wiltshire

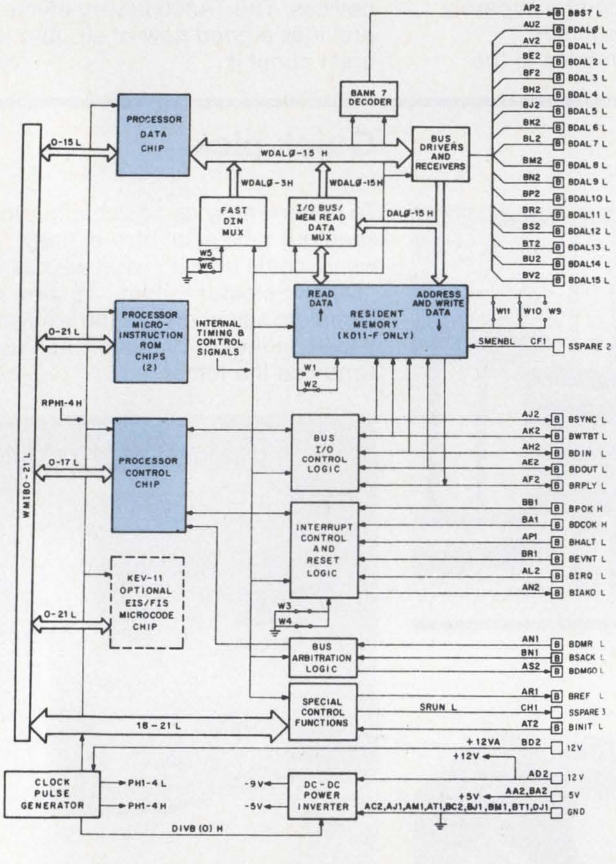
16-bit minicomputer, KD11-F

Based on LSI-11 chip set

Alternate sources: None

Digital Equipment Corp.
1 Iron Way
Marlborough, MA 01752
(617) 481-7400

The LSI-11 microcomputer system is based on an asynchronous bus that permits system components to operate at their maximum speed. Direct addressing extends to 32 kwords, or 64 kbytes. A hardware memory stack handles structured data, subroutines and interrupts. DMA capability enhances distributed processing. The restart mode (power up vector, microcode subset, bootstrap) is jumper selected. A microprogram controls all manual entry and display functions. Double-precision fixed and floating-point arithmetic and multiply/divide are available as options. Because the LSI-11 system is software compatible with the larger PDP-11s, a wide range of programs is available. Over 100 boards and accessories provide hardware support.



Specifications

Word size (data/address)	16/15 bits
On-board RAM (min/max)	4 kwords
On-board ROM (min/max)	0/0 words
Addressable memory	32 kwords
Clock frequency	2.6 MHz
I/O ports, parallel	16-bit bus
I/O ports, serial	none
Board size	228 × 266 mm
	10.5 × 8.9 in.
Power required (V/I)	5 V/1800 mA
	12 V/800 mA

Hardware

Model	Description	Price (100 qty)
KD11-F	CPU with 4 kword RAM	$ 634
MRV11-AA	ROM board, 32 sockets	112
MSV11-B	4 kwords dynamic RAM	400
MSV11-DD	32 kwords dyn. RAM	1536
DLV11	Ser. I/O 20 mA/EIA	160
DLV11-J	4-pt. ser. I/O, RS-422	298
DZV11-B	4-line MUX, max 9600 bd.	544
AAV11-A	12-bit 4-channel d/a	576
ADV11-A	12-bit 16-chan SE a/d	640
DRV11	Parall. interf. I/O	134
IBV11-A	IEEE-488 intrum. interf.	480

Comments

Input/output is over a 33-line bus. Address and data are multiplexed on 16 lines, eight lines are vacant, and the balance serves control functions.

The basic op code of the LSI-11 uses both single and double operand address instructions. The 66 basic instructions can be supplemented with those of the Extended Arithmetic chip. By utilizing the general-purpose registers, the instruction repertoire can be extended to over 400. Addressing modes include single and double operand, four modes of direct addressing, and three modes of indirect (deferred) addressing.

Software support includes paper tape software (editor, assembler, linker, debugger, loader) for $110 and the floppy-disc based RT-11 operating system (includes foreground/background and macros), from $1105, as well as Basic, Fortran, APL and Focal versions. Thanks to the LSI-11's compatibility with the PDP-11 family, a large library of applications programs is available.

Hardware support includes 10 variants of the CPU, 13 memory boards, seven communications boards, nine interfaces and over 50 accessories. Packaged development systems range from $1995 to $5495.

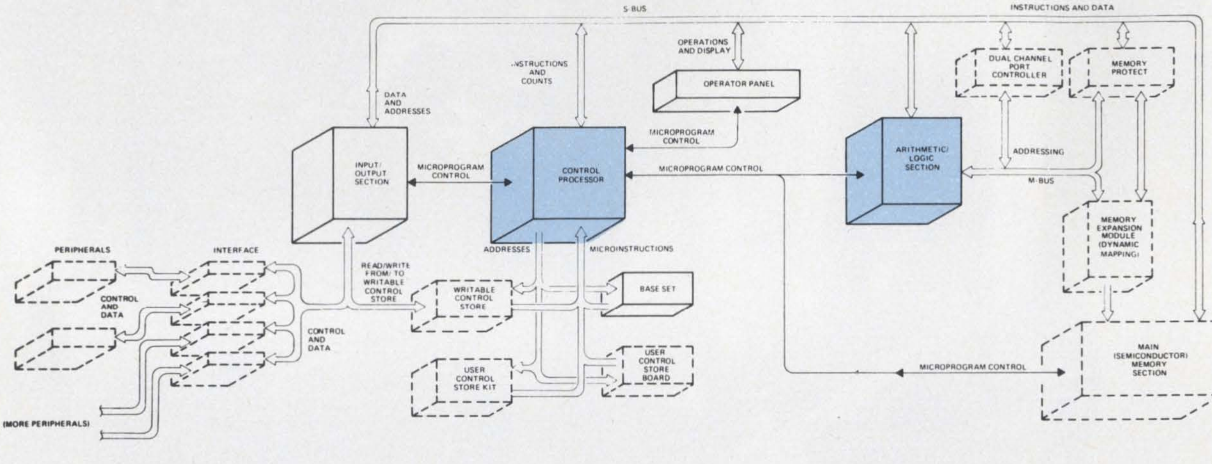
16-bit single-board computer, 2108K

MSI logic based

Hewlett-Packard
11000 Wolfe Road
Cupertino, CA 95014
(408) 257-7000

Alternate sources: None

The K-series single-board computer is a compatible member of the HP-1000 minicomputer family. It is a user-microcodable processor with a 325 ns pipelined instruction execution. On the board are two DMA channels, with a maximum block transfer of 32 kwords/channel at data rates of up to 1.14 Mwords/s. Up to 55 word-serial bidirectional I/O ports are available and multilevel priority interrupt capability is included on the board. A scratchpad RAM of just 32 16-bit words and a control ROM space of up to 1024 24-bit words are available to the user. An external addressing range of 2 Mbytes can be handled with dynamic mapping.



NOTE: DASHED OUTLINES (— — —) INDICATE EQUIPMENT NOT SUPPLIED WITH THE STANDARD COMPUTER

Specifications

Word size (data/address)	16/15 bits*
On-board RAM (min/max)	16 words
On-board ROM (min/max)	0/1024 24-bit words
Addressable memory	2 Mbytes
Clock frequency	28.5 MHz
I/O ports, parallel	55 16-bit ports
I/O ports, serial	0
Board size	460 × 330 mm
	18.125 × 13 in.
Power required (V/I)	5 V/9500 mA
	−2 V/250 nA

*Optional dynamic mapping to 20 bits

Hardware

Model	Description	Price (unit qty)
2108K	Processor board	$ 1475*
17278A, B	Card cages	475/625
12728C	Front panel control	325
12728E	ROM-based instructions	350
2108MK	Processor & 32 k RAM (2 boards)	2950

*There is also a wide array of HP-1000 series boards and software available for use with the processor.

Comments

The input and output lines of the 2108K processor are set up as addressable I/O ports. Up to 55 16-bit word-serial ports can be accessed by the processor. There are no serial ports on the board, but there are two DMA channels available, each capable of transferring blocks of 32 kwords at 1.14 Mwords/s.

The instruction set of the board is user definable by microprogramming, however a set of control ROMs is available to provide the HP-1000 instruction set which consists of 128 basic operations, 53 of which are memory and register reference commands, 17 are I/O operations, 16 are arithmetic (including floating point arithmetic), 32 are index operations, and 10 more are bit, byte and word manipulation instructions. For the microprogrammer there are 211 operations possible.

Software support includes the ROM-based HP-1000 instruction set and microprogramming support—an assembler, drivers and a development system. There is a software subscription service available.

Hardware support includes all the HP-1000 support boards and development boards for the microprogram code. There are also some independent vendors that offer HP-1000 compatible boards.

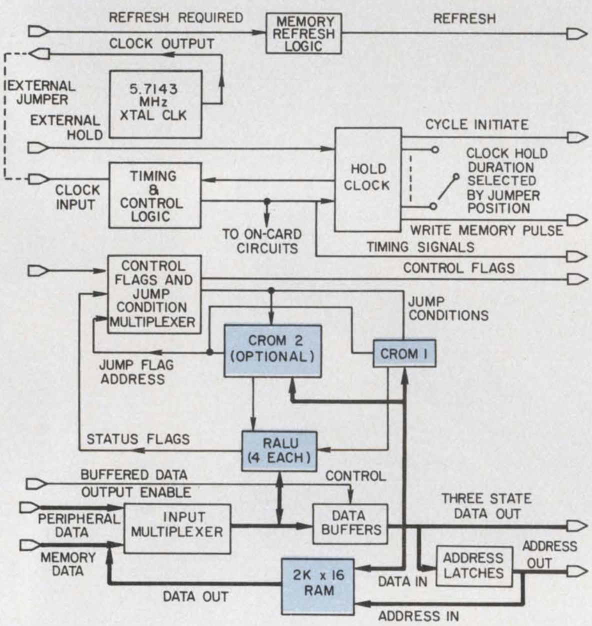
16-bit minicomputer, IMP-16C, L

Based on IMP-16 chip set

Alternate sources: None

National Semiconductor Corp.
2900 Semiconductor Drive
Santa Clara, CA 95051
(408) 737-5000

A stand-alone 16-bit minicomputer, the IMP-16 is based on the multiple-chip IMP-16 set which contains 4-bit PMOS processor slices. The IMP-16C/400 includes 1 kword of static RAM, sockets for 1 kword of ROM/PROM and a set of 43 instructions. The IMP-16C/500 adds 17 instructions for double-word memory, reference and arithmetic. The IMP-16L/300 offers the combined 60-instruction set and adds four DMA ports with transfer rates up to 1 million words/s. With the Extended CROM-II installed, 17 more instructions are available. A Power I/O CROM provides 11 additional I/O data transfer instructions. The 16L architecture facilitates multiprocessing.



Specifications

Word size (data/address)	16/16 bits
On-board RAM (min/max)	1 kword
On-board ROM (min/max)	0/1 kword
Addressable memory	64 kwords
Clock frequency	5.7143 MHz
I/O ports, parallel	2 × 16 in, 1 × 16 out
I/O ports, serial	1 (using CPU flag)
Board size	279 × 216 mm
	11 × 8.5 in.
Power required (V/I)	5 V/2250 mA
	−12 V/500 mA

Comments

I/O is structured with 16 three-state buffered output lines, 16 three-state address lines and two selectable 16-bit input buses. Serial I/O is accomplished with one of the CPU's control flag lines.

The instruction set consists of 17 memory reference, 15 register reference instructions, and seven I/O, flag and halt instructions. The control ROM CROM II adds to this set 17 more instructions, including multiply, divide, double precision add and subtract, and a number of bit, byte, and flag instructions. DMA, stack and string instructions are available on the Power I/O CROM.

Software support includes the IMP-16F/400 Floating Point Firmware package with single and double-precision arithmetic and trigonometry functions, and an Arithmetic CROM that offers double operations (two's complement, shift, load) and fractional operations. Also available are a cross assembler ($495) and DOS software on paper tape or cards ($200).

Hardware

Model	Description	Price (100 qty)
IPC−16C/400	Microcomputer	$ 557
−16C/500	Microcomputer	592
−16L/300	Microcomputer	595
−16P/004A	4 kword static RAM	473
−16P/008P	8 kword ROM card	767
−16P/008B	008P card less ROM	280
−16L/006P	2 & 4 k ROM card	630
−16L/006B	006P card less ROM	385

Hardware support consists of the IMP-16P development system ($5075), dual-floppy disc system with I/F and software ($2660), and a range of prototype cards and card cages.

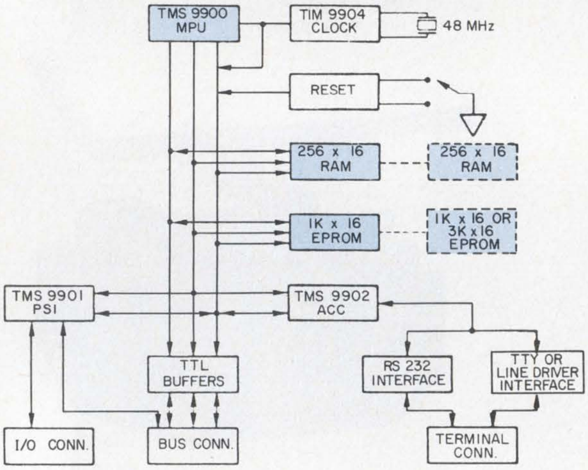
16-bit minicomputer, TM990/100M

μP used: TMS9900 (NMOS)

Texas Instruments Inc.,
8600 Commerce Park Drive
Houston, TX 77036
(713) 776-6511

Alternate sources: None

A single-board microcomputer with RAM and EPROM on board. Programmable serial and parallel I/O is provided. All address, data and control lines are brought to the board connectors for easy expansion into a larger system. Option of EIA or TTY interface (jumper-selectable), prototyping area, and asynchronous communications controller. A complete prototyping system, AMPL, includes video terminal, dual floppy and a special high-level language. An upgraded version, the 101M, offers a second serial port and double the RAM capacity.



Specifications

Word size (data/address)	16/15 bits
On-board RAM (min/max)	256/2048 words
On-board ROM (min/max)	1 k/4 kwords
Addressable memory	32 kwords
Clock frequency	3 MHz
I/O ports (par./ser.)	1 × 16/75 to 38,400 bd
Board size	279 × 190 mm
	11 × 7.5 in.
Power required (V/I)	5 V/1300 mA
	12 V/200 mA
	−12 V/100 mA

Comments

Serial and parallel I/O are programmable. The interface chip handles 16 parallel I/O lines (TTL compat.), while serial I/O is RS-232 or 20-mA current loop on the −1, or differential line driver on the −2 and −3.

The instruction set includes 16 arithmetic (multiply/divide), 20 program control, 14 data control, 6 logical, 4 shift, 5 bit I/O, 6 external instructions totaling 69 commands.

Software support for the board includes a line-by-line assembler ($100), interactive debug monitor TIBUG ($100), and transportable cross support software (assembler, simulator, ROM utility).

Supporting hardware includes memory and I/O expansion boards, a microterminal for data entry and editing, and 4-slot chassis, extender board, prototyping card and connector kit.

Hardware

Model	Description	Price (unit qty)
TM990/100M-1	μC board w. monitor	$ 450
TM990/100M-2	Unprogrammed μC bd.	450
TM990/100M-3	μC Board w. max. memory	572
TM990/101M	μC board	625
TM990/201-41	4k EPROM, 2k RAM	595
TM990/201-42	8k EPROM, 4k RAM	928
TM990/201-43	16k EPROM, 8k RAM	1430
TM990/206-41	4-k RAM expansion	585
TM990/206-42	8-k RAM expansion	790
TM990/310	48 I/O points, progr'ble	295
TM990/301	Microterminal	125

Appendix

The following 19 pages contain summaries of the architectures and instruction sets for six popular microprocessors: the 8080A/8085, the 6800, the Z80, the CDP1802, the 6100 and the TMS9900. These processors were selected to give you a sample of the various instructions and modes of operation that are possible.

Instruction set and programming for the 8080 and 8085

The basic instruction set for the 8080 contains 78 commands that can be grouped into four major categories: data-transfer instructions, branch instructions, arithmetic and logic instructions, and I/O and machine-control instructions. The 8085 adds two more instructions to the 8080 set, and both fall into the last category. (See table for a full listing of the instruction mnemonics and their definitions.)

The first byte of an instruction is an operation code. The op code is supplemented in many cases by one or two address or data bytes. Data stored in memory or registers may be addressed in one of four modes:

- Direct—a memory address of the data is contained in bytes 2 and 3 of the instruction;
- Register—the register or register pair containing the data is specified by the instruction;
- Register indirect—a register pair containing the data's memory address is specified by the instruction;
- Immediate—the instruction contains the data, rather than the data address.

Branch instructions specify the next instruction by containing the next instruction address (direct) or by indicating a register pair containing the next instruction address (register indirect).

Two complete sets of software packages are available to the programmer: those resident in the Intellec MDS system, and cross products (available on both computer tape and time-shared computer networks) written in ANSI-standard Fortran IV.

The cross products and resident software generate completely compatible code. Routines written with either method can be linked, emulated and debugged in the microcomputer environment with the Intellec MDS system, which can also be used to combine the debugging of program and hardware design.

Programs can be written with a macro assembler or PL/M compiler (PL/M is Intel's high-level programming language). The macro assemblers translate mnemonics into machine code. PL/M allows programs to be written in a natural algorithmic language and eliminates the need to allocate memory or manage register usage.

An example of a sorting routine written with PL/M appears in the figure. The free-form input shown is translated into 8080 object code by the compiler; the programmer can concentrate on the software design structure and system-logic requirements.

```
                    /*   BUBBLE SORT DECLARATION   */
SORT  PROCEDURE (N) ADDRESS.
    /*   N = LENGTH OF A
         COUNT = NR. OF SWITCHES PERFORMED TO-DATE
         SWITCHED = (BOOLEAN) HAVE WE DONE ANY SWITCHING YET ON THIS SCAN?   */
    DECLARE (N, I, SWITCHED) BYTE.
         (TEMP, COUNT) ADDRESS.
    SWITCHED = 1.            /*   SWITCHED = TRUE MEANS NOT DONE YET   */
    COUNT = 0.
    DO WHILE SWITCHED.
         SWITCHED = 0.       /*   BEGIN NEXT SCAN OF A   */
         DO I = 0 TO N-2.
              IF A(I) > A(I+1) THEN
                   DO.               /*   FOUND A PAIR OUT OF ORDER   */
                   COUNT = COUNT + 1.
                   SWITCHED = 1.     /*   SET SWITCHED = TRUE   */
                   TEMP = A(I).      /*   SWITCH THEM INTO ORDER   */
                   A(I) = A(I+1).
                   A(I+1) = TEMP
                   END.
         END.
         /*   HAVE NOW COMPLETED A SCAN   */
    END  /*   WHILE   */.
    /*   HAVE NOW COMPLETED A SCAN WITH NO SWITCHING   */
    RETURN COUNT;
END SORT
```

A. **"Bubble sort" routine written in PL/M** arranges data pertaining to events according to the frequency with which individual events occur. Events occurring most frequently move to the top.

Mnemonic	Definition
Data transfer instructions	
MOVr1,r2	Move register to register
MOV M, r	Move register to memory
MOV r, M	Move memory to register
MVI r	Move immediate register
MVI M	Move immediate memory
LXI B	Load immediate register Pair B & C
LXI D	Load immediate register Pair D & E
LXI H	Load immediate register Pair H & L
LXI SP	Load immediate stack pointer
STAX B	Store A indirect

Mnemonic	Definition
Data transfer instructions	
STAX D	Store A indirect
LDAX B	Load A indirect
LDAX D	Load A indirect
STA	Store A direct
LDA	Load A direct
SHLD	Store H & L direct
LHLD	Load H & L direct
XCHG	Exchange D & E H & L Registers
PUSH B	Push register Pair B & C on stack
PUSH D	Push register Pair D & E on stack

Mnemonic	Definition
PUSH H	Push register Pair H & L on stack
PUSH PSW	Push A and Flags on stack
POP B	Pop register Pair B & C off stack
POP D	Pop register Pair D & E off stack
POP H	Pop register Pair H & L off stack
POP PSW	Pop A and Flags off stack
XTHL	Exchange top of stack, H & L
SPHL	H & L to stack pointer

Jump, call and return instructions

JMP	Jump unconditional
JC	Jump on carry
JNC	Jump on no carry
JZ	Jump on zero
JNZ	Jump on no zero
JP	Jump on positive
JM	Jump on minus
JPE	Jump on parity even
JPO	Jump on parity odd
PCHL	H & L to program counter
CALL	Call unconditional
CC	Call on carry
CNC	Call on no carry
CZ	Call on zero
CNZ	Call on no zero
CP	Call on positive
CM	Call on minus
CPE	Call on parity even
CPO	Call on parity odd
RET	Return
RC	Return on carry
RNC	Return on no carry
RZ	Return on zero
RNZ	Return on no zero
RP	Return on positive
RM	Return on minus
RPE	Return on parity even
RPO	Return on parity odd
RST	Restart
IN	Input
OUT	Output

Arithmetic and logic instructions

INR r	Increment register
DCR r	Decrement register
INR M	Increment memory
DCR M	Decrement memory
INX B	Increment B & C registers
INX D	Increment D & E registers
INX H	Increment H & L registers
INX SP	Increment stack pointer
DCX B	Decrement B & C
DCX D	Decrement D & E
DCX H	Decrement H & L

Mnemonic	Definition
DCX SP	Decrement stack pointer
ADD r	Add register to A
ADC r	Add register to A with carry
ADD M	Add memory to A
ADC M	Add memory to A with carry
ADI	Add immediate to A
ACI	Add immediate to A with carry
DAD B	Add B & C to H & L
DAD D	Add D & E to H & L
DAD H	Add H & L to H & L
DAD SP	Add stack pointer to H & L
SUB r	Subtract register from A
SBB r	Subtract register from A with borrow
SUB M	Subtract memory from A
SBB M	Subtract memory from A with borrow
SUI	Subtract immediate from A
SBI	Subtract immediate from A with borrow
ANA r	AND register with A
XRA r	Exclusive OR register with A
ORA r	OR register with A
CMP r	Compare register with A
ANA M	AND memory with A
XRA M	Exclusive OR memory with A
ORA M	OR memory with A
CMP M	Compare memory with A
ANI	AND immediate with A
XRI	Exclusive OR immediate with A
ORI	OR immediate with A
CPI	Compare immediate with A
RLC	Rotate A left
RRC	Rotate A right
RAL	Rotate A left through carry
RAR	Rotate A right through carry
CMA	Complement A
STC	Set carry
CMC	Complement carry
DAA	Decimal adjust A

I/O and machine control instructions

EI	Enable interrupts
DI	Disable interrupt
NOP	No-operation
HLT	Halt

New 8085A instructions

RIM	Read interrupt mask
SIM	Set interrupt mask

Architecture of 8080 and 8085 microprocessors

Both the 8080A (top) and the 8085A (bottom) share the same basic architecture and instruction set. Both processors have an internal array of six 16-bit registers, three of which can be addressed in byte or double-byte formats. The other three registers form the stack pointer, program counter and the incrementer/decrementer and address latch.

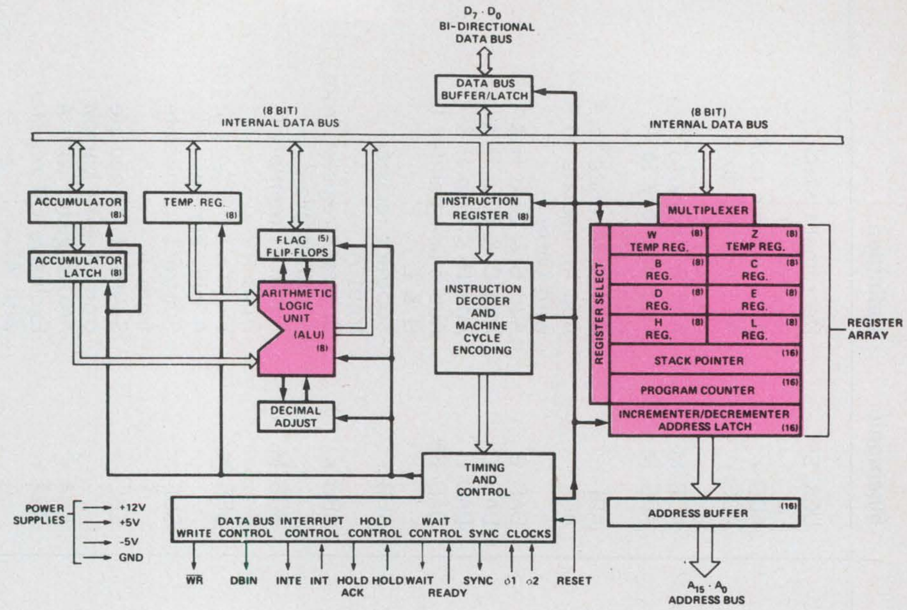
Up to 64 kbytes of memory can be directly addressed by either processor. And since the stack pointer permits any portion of the RAM to be used as an external stack, subroutine nesting is limited only by the memory size. The stack can be used to store the contents of the program counter, flag register, accumulator and all the general-purpose processor registers.

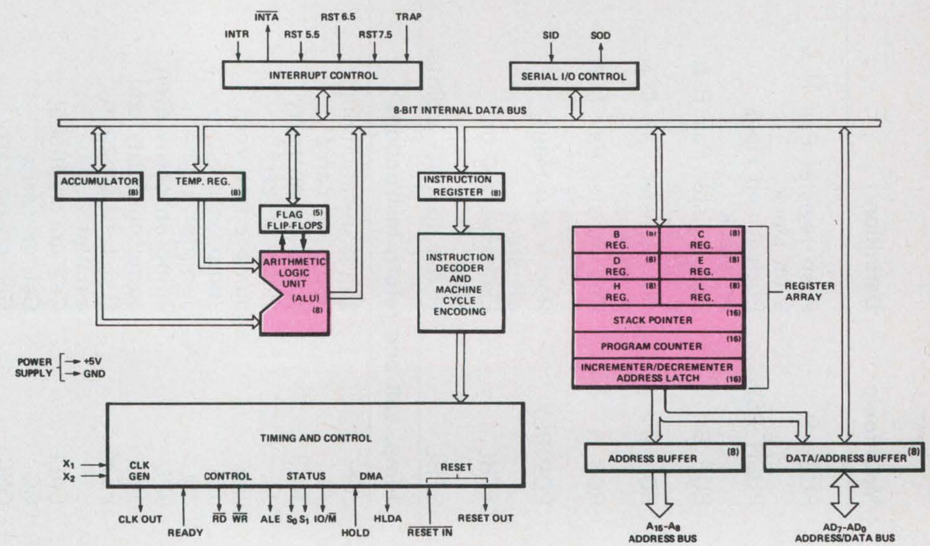
The arithmetic and logic section (ALU) performs arithmetic, logic and shift/rotate operations. Associated with it are an 8-bit accumulator, a temporary register, and a 5-bit flat register (zero, carry, sign, parity, and auxiliary carry). Testing the auxiliary carry for decimal correction permits decimal arithmetic to be performed.

It's in the control section that the 8080 and 8085 begin to differ. Both the 8080 and 8085 are fed by internal 8-bit data bus and controlled by the timing and control subsection. But the 8085 has an internal clock generator and more control lines. In addition, the 8085 uses a partially multiplexed address bus—only eight address lines are directly available for address information; the other eight address lines are time-multiplexed with the data bus. The on-chip latches of the newer support chips (8155/8355/8755) permit a direct interface with the 8085 and 16-bit addressing.

Furthermore, the 8085 can now have four levels of vectored interrupts via the interrupt control section. And because its number of address lines has been reduced, two pins can function as a serial I/O port.

The 8080 and 8085 also diverge on clock speeds and power requirements. While the 8080A requires three supplies and a two-phase clock, the 8085 needs just a single 5-V supply and an external crystal or R-C network.





MC6800 programming methods and mnemonic definitions

To get a good look at the basic instruction set of the MC6800, you can divide it into accumulator and memory, index register and stack, jump-and-branch and condition-code instructions (see table). Each instruction requires one byte and is followed by either one or two additional bytes—of an address location, data or even another instruction.

The MC6800 offers seven different ways to address data:

(1.) Inherent. This mode lets you use the operand as the address for the data to be manipulated. The operand may be either one or two bytes long.

(2.) Accumulator. Although similar to inherent addressing, in this mode the operator defines the location being addressed.

(3.) Immediate. In this mode, the byte following the instruction is used as the operand of the instruction. No reference to the memory need be made.

(4.) Direct. For direct addressing, the µP can only reach locations 0 to 255 because only a single-byte operand is used. After an instruction is encountered in this mode, the µP looks at the program counter's contents, adds one and uses that number as the location of the data word.

(5.) Extended. This mode is similar to the Direct mode except that a 2-byte operand is used, thus permitting the µP to reach the remaining memory locations, 256 to 65,535. After an instruction is encountered, the µP looks at the contents of the program counter, adds one and uses that number as the first half of the memory address. This repeats and the original value of the program counter plus two becomes the second half of the memory address.

(6.) Relative. You can specify a memory location whose address, relative to the value in the program counter, can be up to 125 locations below that value or up to 129 locations above the value. To go further than the 129 locations requires an unconditional jump, jump to subroutine or return from subroutine.

(7.) Indexed. The numerical address is not fixed, but depends on the contents of the index register.

Addressing-mode selection is made when the

Nomenclature

ACCA	Accumulator A	IXL	IX, lower order 8 bits
ACCB	Accumulator B	PC	Program counter, 16 bits
ACCX	Accumulator ACCA or ACCB	PCH	PC, higher order 8 bits
CC	Condition code register	PCL	PC, lower order 8 bits
C	Carry bit of CC	SP	Stack pointer, 16 bits
V	Two's complement overflow indicator bit of CC	SPH	SP, higher order 8 bits
Z	Zero indicator bit of CC	SPL	SP, lower order, 8 bits
N	Negative indicator bit of CC	M	A memory location (one byte)
I	Interrupt mask bit of CC	M+1	The byte of memory at location 0001 plus the address of the location indicated by M
H	Half carry bit of CC	REL	Relative address
IX	Index register, 16 bits		
IXH	IX, higher order 8 bits		

Accumulator and memory instructions

Operation	Mnemonic	Description
Add	ADDA ADDB	Adds contents of ACCX and contents of M; places results in ACCX.
Add accumulators	ABA	Adds contents of ACCB to contents of ACCA; places results in ACCA.
Add with carry	ADCA ADCB	Adds contents of C bit to the sum of the contents of ACCX and M; places results in ACCX.
Logical AND	ANDA ANDB	Performs logical AND between the contents of ACCX and contents of M; places results in ACCX.
Bit test	BITA BITB	Performs logical AND comparison of contents of ACCX and M and modifies N, Z and V bits of CC. Contents of ACCX and M are not changed.
Clear	CLR CLRA CLRB	The contents of M or the contents of ACCX are replaced with zeros.
Compare	CMPA CMPB	Compares the contents of ACCX and M and modifies the N, Z, V and C bits of CC. Contents of ACCX and M are not changed.
Complement, 1s	COM COMA COMB	Replaces each bit of the contents of ACCX or M with its one's complement

(continued on next page)

(continued from page 211)

programs are written. If you manually translate the program into machine code, the addressing mode is inherent in the operation code.

Several different methods of generating the machine-level codes are available to the programmer. For in-house development you can use an assembly program available either from timesharing services or from the EXORciser development system. Timesharing services also offer a high-level language called MPL (a subset of PL/1) that is especially handy for applications that involve mathematical computations of data.

The compiler program of MPL translates source statements into M6800 assembly-level programs. Already written assembly-level instructions can be embedded in the compiled program to permit optimization when programs are already available. An assembler program then takes the assembly-level program and makes two passes in the first, it assigns numerical values to source-statement labels, then checks syntax and lists errors. On the second pass, undefined symbols from pass one are defined and an assembled listing is provided. The assembler has 12 directives, which can be used to assign data values, allocate memory and control the sequencing and formatting of programs.

Also available are an interactive simulator program that duplicates, on a host computer, the exact execution of the assembled machine-language program. Another useful program is the Build Virtual Machine, which permits you to reorganize the software you have under development. This program helps to determine and minimize memory requirements.

For development systems such as the EXORciser, a macroassembler is available. Macroinstructions represent a sequence of assembly-level instructions. The macros simplify program development, when instruction sequences must be repeated, by providing the programmer with a shorthand notation of the sequences.

In the EXORciser, the Evaluation Module II and in the Design Evaluation Kit, available firmware includes EXbug, MINIbug and MIKbug, respectively. These programs contain routines for loading user programs, for debugging them and for providing interactive control of the prototype system.

Complement, 2s (negate)	NEG NEGA NEGB	Replaces each bit of the contents of ACCX or M with its two's complement.
Decimal adjust, A	DAA	Adjusts contents of ACCA and C bit to represent correct BCD sum and carry after an ABA, ADD or ADC operation on a BCD operand.
Decrement	DEC DECA DECB	Subtracts one from the contents of M or ACCX.
Exclusive OR	EORA EORB	Performs logical Exclusive OR between contents of ACCX and M; places results in ACCX.
Increment	INC INCA INCB	Adds one to the contents of M or ACCX.
Load Accumulator	LDAA LDAB	Loads contents of M into ACCX.
OR, Inclusive	ORAA ORAB	Performs logical OR between contents of ACCX and M; places results in ACCX.
Push data	PSHA PSHB	Contents of ACCX stored on stack at the address contained in SP; SP then decremented by one.
Pull data	PULA PULB	SP incremented by one; ACCX loaded from stack, from the address contained in SP.
Rotate left	ROL ROLA ROLB	All bits of ACCX or M shifted left by one bit. Bit 0 of the byte loaded with the initial C bit. C bit loaded with the initial MSB of ACCX or M.
Rotate, right	ROR RORA RORB	All bits of ACCX or M shifted right by one bit. Bit 7 of the byte loaded with the initial C bit. C bit loaded with the initial LSB of ACCX or M.
Shift left, arithmetic	ASL ASLA ASLB	All bits of ACCX or M shifted left by one bit. Bit 0 of the byte loaded with zero. C bit loaded with the initial MSB of ACCX or M.
Shift right, arithmetic	ASR ASRA ASRB	All bits of ACX or M shifted right by one bit. Bit 7 of the byte loaded with a zero. C bit loaded with the initial LSB of ACCX or M.

Operation	Mnemonic	Description
Shift right, logic	LSR LSRA LSRB	All bits of ACCX or M shifted right by one bit. Bit 7 of the byte held constant. C bit loaded with the initial LSB or ACCX or M.
Store accumulator	STAA STAB	Store the contents of ACCX at M; the contents of ACCX remains unchanged.
Subtract	SUBA SUBB	Subtract the contents of M from ACCX; place the results in ACCX.
Subtract accumulators	SBA	Subtracts the contents of ACCB from ACCA; places results in ACCA. Contents of ACCB not affected.
Subtract with carry	SBCA SBCB	Subtracts the contents of M and C from ACCX; places results in ACCX.
Transfer accumulators	TAB TBA	Moves contents of ACCA to ACCB (TAB) or vice versa (TBA). The contents of the transferred accumulator are not changed; the contents of the receiving accumulator are changed.
Test, zero or minus	TST TSTA TSTB	If MSB of ACCX or M is one, then the N bit of CC is set to one. If the contents of ACCX or M are all zeroes, then the Z bit is set to one.
Index register and stack manipulation instructions		
Compare index register	CPX	The contents of IXH and IXL are compared to M and M+1, respectively. The N,Z and V bits of CC are affected.
Decrement index register	DEX	Subtracts one from the index register. Z bit of CC is affected.
Decrement stack pointer	DES	Subtracts one from the stack pointer. CC not affected.
Increment index register	INX	Adds one to the index register. Z bit of CC is affected.
Increment stack pointer	INS	Adds one to the stack pointer. CC not affected.
Load index register	LDX	Loads IXH and IXL with contents of M and M+1, respectively. The N,Z and V bits of CC are affected.
Load stack pointer	LDS	Loads SPH and SPL with the contents of M and M+1, respectively. The N,Z and V bits of CC are affected.
Store index register	STX	Stores IXH and IXL at locations M and M+1, respectively. The N,Z and V bits of CC are affected.
Store stack pointer	STS	Stores SPH and SPL at locations M and M+1, respectively. The N,Z and V bits of CC are affected.
Transfer from IX to SP	TXS	Loads SP with contents of IX minus one. Contents of IX unchanged.
Transfer from SP to IX	TSX	Loads IX with contents of SP, plus one. Contents of SP unchanged.
Jump and branch instructions		
Branch always	BRA	Branch to the address equal to PC+0002+REL.
Branch if carry clear	BCC	Branch to the address equal to PC+0002+REL, if the C bit = 0.
Branch if carry set	BCS	Branch to the address equal to PC+0002+REL, if the C bit = 1.
Branch if equal to zero	BEQ	Branch to the address equal to PC+0002+REL, if the Z bit = 1.
Branch if ≥ zero	BGE	Branch to the address equal to PC+0002+REL, if the logical Exclusive OR of N and V bits = 0.
Branch if > zero	BGT	Branch to the address equal to PC+0002+REL,if the contents of Z+[N + V] = 0.
Branch if higher	BHI	Branch to the address equal to PC+0002+REL, if the logical AND of C and Z bits = 0.
Branch if ≤ zero	BLE	Branch to the address equal to PC+0002+REL, if the contents of Z+ N + V =1.
Branch if lower or same	BLS	Branch to the address equal to PC+0002+REL, if the contents of C+Z = 1.

Branch if < zero	BLT	Branch to the address equal to PC+0002+REL, if the contents of N + V = 1.
Branch if minus	BMI	Branch to the addrress equal to PC+0002+REL, if the contents of N = 1.
Branch if ≠ zero	BNE	Branch to the address equal to PC+0002+REL, if the contents of Z = 0.
Branch if overflow clear	BVC	Branch to the address equal to PC+0002+REL, if the contents of V = 0.
Branch if overflow set	BVS	Branch to the address equal to PC+0002+REL, if the contents of V = 1.
Branch if plus	BPL	Branch to the address equal to PC+0002+REL, if the contents of N = 0.
Branch of subroutine	BSR	Branch to the address equal to PC+0002+REL. PC+0002 stored in the stack.
Jump	JMP	PC loaded with a numerical address; a jump to that location occurs.
Jump to subroutine	JSR	PC incremented by 0002 (indexed address mode) or 0003 (extended address mode), then stored in the stack. PC loaded with a numerical address; a jump to that location then occurs.
No operation	NOP	Advances PC; no other registers affected.
Return from interrupt	RTI	CC, ACCX, IX and PC stored in the states that were saved in the stack.
Return from subroutine	RTS	SP incremented by one; PCH loaded with the contents of the location specified by SP. Again, SP is incremented by one; PCL loaded with the contents of the location specified by SP.
Software interrupt	SWI	PC incremented by one; then PC, IX, ACCX, and CC stored in the stack. SP decremented by one after each byte is stored. I bit then set and PC then loaded with the address specified by the software.
Wait for interrupt	WAI	Registers operated on and saved as in SWI instruction, except I bit is not set. Program execution suspended until interrupt occurs on IRQ line. When IRQ goes low, and provided that the I bit is clear, program execution proceeds as in SWI.
	Condition code register manipulation instructions.	
Clear carry	CLC	Carry bit reset to zero.
Clear interrupt mask	CLI	Interrupt bit reset to zero.
Clear overflow	CLV	Overflow bit reset to zero
Set carry	SEC	Carry bit set to one.
Set interrupt mask	SEI	Interrupt bit set to one.
Set overflow	SEV	Overflow bit set to one.
Transfer from ACCA to CC	TAP	Transfers the contents of 0 through 5 of ACCA to the corresponding bit positions of CC. Contents of ACCA not changed.
Transfer from CC to ACCA	TPA	Transfers the contents of bit 0 through 5 of CC to the corresponding bit positions of ACCA. Bits 6 and 7 of ACCA are set to one. Contents of CC not changed.

Architecture of the MC6800 microprocessor

The MC6800 microprocessor is a single-chip, 8-bit parallel processor housed in a 40-pin dual in-line package. The μP has a variable-length stack, maskable interrupt vectoring, direct memory addressing capability and six internal registers, as well as 72 variable-length instructions and seven addressing modes.

Inside the μP are three 16-bit registers, which form the Stack Pointer, Program Counter and Index Register. There are also three 8-bit registers that are known as the condition-code register and accumulators A and B. Since the address register is 16 bits wide, up to 64-k words can be directly addressed.

The stack pointer contains a 2-byte register that holds the address of the next available location in an external push-down/pop-up stack (usually part of the external RAM). The stack is usually used to store the contents of the program counter, accumulators, index register, and other information necessary for the μP to resume operation after an interrupt is serviced.

The arithmetic and logic section of the μP (the ALU) does all the bit manipulation under instruction-set control. In conjunction with the ALU, the two accumulators hold the data that go into and come out of the logic array.

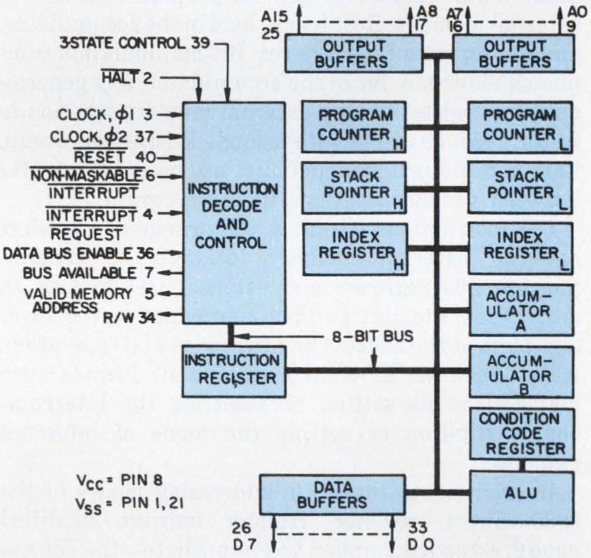
The instruction register, along with the on-chip decoder and control-logic array, manage the internal operations of the μP. Combinations of commands and addressing modes produce a total of 197 executable instructions that are assembled in one, two or three bytes of machine code.

A two-phase clock controls all the timing of the μP. On the first phase the contents of the program counter are transferred to the address bus. The Valid-Memory-Address line then goes high to indicate a valid address is on the bus. On the negative transition of the clock, the program counter gets incremented.

When phase 2 of the clock goes HIGH, data are put on the data bus. (The direction of data flow—to or from the μP—is determined by the Read/Write control line.) Then, when phase 2 goes LOW, data are latched into either the μP or the memory. This sequence occurs every time the μP addresses a location and transfers a data word.

Incoming commands go into the instruction register and are then decoded by the Instruction Decode and Control array, which in turn controls the ALU. All the registers and input and output buffers are interconnected on an 8-bit-wide data bus.

The nine control lines available on the MC6800 package permit various machine operations or provide special control functions. The Go/Halt line permits you to stop all μP operation when put into the Halt position (LOW). The Three-State Control line permits you to cause the Read/Write line and all the address lines to go into the OFF (high impedance) state. You can then use the address bus for DMA applications.



The Read/Write line tells the peripheral devices whether the μP is in the read (HIGH) or write (LOW) state. When the Three-State Control line goes HIGH, it forces the R/W line OFF (high impedance). A Valid Memory Address line tells the memory and peripheral devices that the information on the address bus is a valid address.

For control of the data bus, two lines are available—the Data Bus Enable, which enables the bus drivers when it is placed in the HIGH state, and the Bus Available which, when brought HIGH, indicates that the μP has stopped and that the address bus is available.

Software capabilities of the Z80

Able to execute over 150 different instructions, including all 78 of the 8080A command set, the Z80 features seven basic families of instructions: load-and-exchange, block-transfer-and-search, arithmetic and logic, bit-manipulation (set, reset and test), jump, call-and-return, input/output, and basic μP-control commands. In all, the Z80 can recognize 696 op codes —244 are the codes of the 8080A.

Load instructions move data internally between μP registers or between the registers and external memory. All these instructions must specify a source location, from which data are to be moved, and a destination location. Block-transfer instructions permit any block of memory to be moved to any other location. Search commands let any block of external memory be examined for any 8-bit character. Once the character is found, the instruction is terminated.

The ALU instructions operate on data held in the accumulator and other general-purpose registers or external memory. Results are held in the accumulator, and appropriate flags are set. Bit-manipulation commands allow any bit in the accumulator, any general-purpose register or any external memory location to be set, reset or tested with a single instruction. Jump, Call and Return instructions are used to transfer between various locations in the program.

I/O instructions permit a wide range of transfers between external memory locations or general-purpose Z80 registers and external I/O devices. In either case, the port number is provided on the lower eight bits of the address bus during any I/O operation. Also, the basic μP-control commands include such instructions as setting or resetting the interrupt-enable flip-flop or setting the mode of interrupt response.

In addition to the seven addressing modes of the 8080—direct, register, register indirect, modified page Ø, extended, implied and immediate—the Z80 has three more addressing modes: relative, indexed, and bit addressing—that can be used.

A special byte-call instruction lets the Z80 program proceed to any of eight locations in page Ø of the memory. This modified page Ø addressing allows a single byte to specify a complete 16-bit address, which saves memory space.

Relative addressing lets the Z80 use the byte following the op code to specify a displacement from the current program-counter value. The displacement value is in 2's-complement form, which permits up to a +127 or −128 byte displacement. Extended addressing includes two bytes of address in the instruction.

Index registers can also be used as part of the address. In the indexed addressing mode, a byte of data following the op code is a displacement value that must be added to the specified index register (the op code indicates which register) to form a memory pointer. Also available is an implied addressing mode in which the op code uses the contents of one Z80 register or more as the operands. The last addressing mode lets the Z80 access any memory location or μP register and permits any bit to be set, reset or tested.

Mnemonic	**Description**
8-bit load instructions	
LD r, r'	Load register r with r'
LD r, n	Load register r with n
LD r, (HL)	Load r with location (HL)
LD r, (IX+d)	Load r with location (IX+d)
LD r, (IY+d)	Load r with location (IY+d)
LD (HL), r	Load location HL with r
LD (IX+d), r	Load location IX+d from register r
LD (IY+d), r	Load location IY+d from register r
LD (HL), n	Load location HL with value n
LD (IX+d), n	Load location IX+d with n
LD (IY+d), n	Load location IY+d with n
LD A, (BC)	Load AC with location BC
LD A, (DE)	Load AC with location DE
LD A, (nn)	Load AC with location nn
LD (BC), A	Load location BC with AC
LD (DE), A	Load location DE with AC
LD (nn), A	Load location nn with AC
LD A, I	Load register A from I
LD A, R	Load AC with register R
LD I, A	Load register I with AC
LD R, A	Load register R with AC
16-bit load instructions	
LD dd, nn	Load registers dd with nn
LD IX, nn	Load register IX with nn
LD IY, nn	Load register IY with nn
LD HL, (nn)	Load L with contents of location nn and H with (nn+1)
LD dd, (nn)	Load registers dd with location nn
LD IX, (nn)	Load IX with location nn
LD IY, (nn)	Same but for IY
LD (nn), HL	Load location nn with HL
LD (nn), dd	Load location (nn) with register pair dd
LD (nn), IX	Same but for IX
LD (nn), IY	Same but for IY
LD SP, HL	Load stack pointer from HL
LD SP, IX	Load stack pointer from IX
LD SP, IY	Load stack pointer from IY
PUSH qq	Load register pair qq onto stack
PUSH IX	Load IX onto stack
PUSH IY	Load IY onto stack
POP qq	Load register pair qq with top of stack
POP IX	Load IX with top of stack
POP IY	Load IY with top of stack
Exchange, transfer and search instructions	
EX DE, HL	Exchange contents of DE & HL
EX AF, A' F'	Exchange contents of AF & A' F'
EXX	Exchange all six general purpose registers with alternates
EX (SP), HL	Exchange stack pointer contents with HL contents
EX (SP), IX	Same but use IX register
EX (SP), IY	Same but use IY register
LDI	Load (HL) into DE, increment DE and HL, decrement BC
LDIR	Same but loop until (BC) = O
LDD	Load location (PE) with location (HL) and decrement DE, HL and BC
LDDR	Same but loop until (BC) = O
CPI	Compare contents of AC with (HL), set Z flat if =, increment HL and decrement BC
CPIR	Same but repeat until BC = O
CP s	Compare operand s with AC
CPD	Same as CPI but decrement HL
CPDR	Same as CPIR but decrement HL
8-bit arithmetic and logic instructions	
ADD A, r	Add contents of r to AC
ADD A, n	Add byte n to AC
ADD A, (HL)	Add contents of HL to AC

ADD A, (IX+d)	Add location (IX+d) to AC
ADD A, (IY+d)	Same but (IY+d)
ADC A, s	Add with carry operand s to AC
SUB s	Subtract contents of r, n, HL, IX+d or IY+d from AC
SBC s	Same but also subtract carry flag
AND s	Logic AND of operand s and AC
OR s	Same but OR with AC
XOR s	Same but EX-OR with AC
INC r	Increment register r
INC (HL)	Increment location (HL)
INC (IX+d)	Same but use (IX+d)
INC (IY+d)	Same but use (IY+d)
DEC m	Decrement operand m

16-bit Arithmetic instructions

ADD HL, ss	Add register pair ss to HL
ADC HL, ss	Same but include carry flag
SBC HL, ss	From HL subtract contents of ss and carry flag
ADD IX, pp	Add register pair pp to IX
ADD IY, rr	Same but use rr and IY
INC ss	Increment register pair ss
INC IX	Increment IX register
INC IY	Same but IY register
DEC ss	Decrement register pair ss
DEC IX	Same but IX register
DEC IY	Same but IY register

General purpose arithmetic & control instructions

DAA	Decimal adjust accumulator
CPL	Complement (AC)
NEG	Complement (AC) and add 1
CCF	Complement carry flag
SCF	Set carry flag = 1
NOP	No operation
HALT	Halt, wait for interrupt or reset
DI	Disable interrupts
EI	Enable interrupts
IMØ	Set μP to interrupt mode Ø
IM1	Set μP to interrupt mode 1
IM2	Set μP to interrupt mode 2

Rotate and shift instructions

RLCA	Rotate AC left
RLA	Same but include carry flag
RRCA	Rotate AC right
RRA	Same but include carry flag
RLC r	Rotate register r left
RLC (HL)	Rotate location (HL) left
RLC (IX+d)	Same but location (IX+d)
RLC (IY+d)	Same but location (IY+d)
RL m	Same as any RLC but include carry flag
RRC m	Same as RLC but shift right
RR m	Same as RL m but shift right
SLA s	Shift left (any RLC register)
SRA s	Same but shift right and keep MSB
SRL s	Same as SLA but shift right
RLD	Simultaneous 4-bit rotate from AC_L to L, L to H and H to AC_L
RRD	Simultaneous 4-bit rotate from AC_L to H, H to L and L to AC_L

Bit set, reset and test instructions

BIT b, r	Test bit b of register r
BIT b, (HL)	Test bit b of location (HL)
BIT b, (IX+d)	Test bit b of location (IX+d)
BIT b, (IY+d)	Test bit b of location (IY+d)
SET b, r	Set bit b in register r to 1
SET b, (HL)	Same but use contents of location HL
SET b, (IX+d)	Same but use contents of location IX+d
SET b, (IY+d)	Same but use contents of location IY+d
RES b, s	Reset bit b of operand m

Jump, c all and return instructions

JP nn	Unconditional jump to location nn
JP cc, nn	If condition cc True, do a JP nn otherwise continue
JR e	Unconditional jump to PC+e
JR C,' e	If C = 0 continue. If C = 1 do JR e
JR NC, e	Reverse of JR c, e
JR Z, e	If Z = 0 continue. If Z = 1 do JR e
JR NZ, e	Reverse of JR Z, e
JP (HL)	Load PC from (HL)
JP (IX)	Load PC from (IX)
JP (IY)	Load PC from (IY)
DJNZ, e	Decrement register B and jump relative if B = 0
CALL nn	Unconditional call subroutine at location nn
CALL cc, nn	Call subroutine at location nn if condition cc is True
RET	Return from subroutine
RET cc	If cc false continue, otherwise do RET
RETI	Return from interrupt
RETN	Return from nonmaskable interrupt
RST p	Store PC in stack, load 0 in PC_H and restart vector in PC_L

Input/output instructions

IN A, n	Load AC with input from device n
IN r, (C)	Load r with input from device C
INI	Store contents of location specified by C in address specified by HL, decrement B and increment HL
INIR	Same but repeat until B = 0
IND	Same as INI but decrement HL too
INDR	Same as INIR but decrement HL too
OUT n, A	Load output port (n) with AC
OUT (C), r	Load output port (C) with register r
OUTI	Load output port (C) with location (HL) and increment HL and decrement B
OTIR	Same but repeat until B = 0
OUTD	Same as OUTI but decrement HL
OTDR	Same as OTIR but decrement HL

Notes

b represents a 3-bit code that indicates position of the bit to be modified

cc represents a 3-bit code that indicates which of eight condition codes are to be used

d is an 8-bit offset value

dd refers to register pairs BC, DC, HL or the stack pointer

e represents a signed two's complement number between −126 and +129

m is an 8-bit number

n is an 8-bit number

nn refers to two 8-bit bytes

p represents one of eight restart vector locations on page Ø

pp refers to register pairs BC, DE, the IX register or the stack pointer.

qq refers to register pairs AF, BC, DE or HL

r or r' refers to registers A, B, C, D, E, H or L or their alternates

rr refers to register pairs BC, DE, the IY register or the stack pointer

s refers to either the r registers, the n data word or the contents of locations specified by the contents of the HL, IX+d or IY+d registers

ss refers to register pairs BC, DE, HL or the stack pointer

Z80 microprocessor architecture

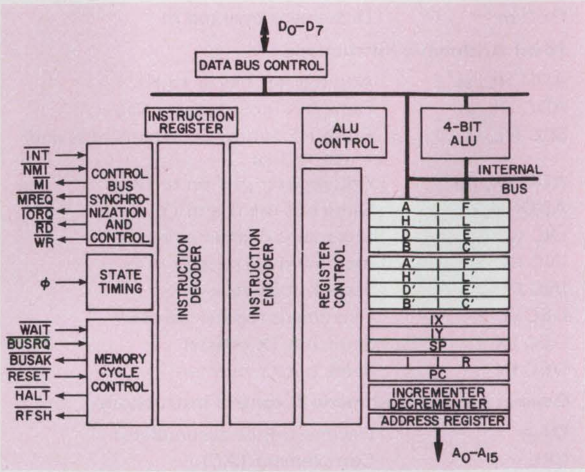
Built into the Z80 microprocessor are all bus-control, memory-control, and timing signals in addition to eight general-purpose 16-bit registers and an arithmetic-and-logic unit (ALU). The Z80 is upward-compatible with the Intel 8080A and 8085 μPs.

All the 8080 registers are duplicated within the Z80 and, in addition to the eight 8-bit registers (A, F, B, C, D, E, H and L) of the 8080, there is an alternate set (A′, F′, B′, C′, D′, E′, H′ and L′) and several other special-purpose registers. The additional registers include two 16-bit index registers (IX and IY), an 8-bit interrupt-vector register (I) and an 8-bit memory-refresh register (R). Also carried forward from the 8080 register set are the 16-bit stack pointer and the 16-bit program counter (PC).

Normally, all instructions reference the main register set, and alternate registers are accessed via two exchange commands that swap register contents in the banks. One command, exchanges the accumulator and register flags, while another instruction, exchanges the other six general-purpose registers. Since both instructions are single-byte, minimum-execution-time instructions, a complete swap can be done in four clock cycles (1 μs for a 4-MHz clock). These commands and registers are very handy for rapid single-level interrupt handling.

The Z80's two index registers have no direct corollary in the 8080 architecture, but in operation they resemble the single index register in the 6800 μP. Instructions using this mode such as the accumulator-load command [LD A, (IX + 7)] contain a single-byte offset field (+7, in this case). The effective address of the operand is the sum of the offset and the IX-register contents. This addressing mode is particularly convenient for table references, multibyte entries or for passing a pointer to a group of subroutine parameters. The offset byte is interpreted by the Z80 as a 2's complement number, so both positive and negative indexing is possible.

A special feature of the Z80 is its ability to refresh dynamic memory automatically. Its memory-refresh register acts as a 7-bit counter that is incremented after every op-code fetch. After the fetch, the R-



register contents are loaded onto the low-order seven bits of the address bus, and a status line on the processor goes low to indicate the presence of a valid refresh count. Because this entire process takes place while the op code is decoded internally, it never interferes with any other μP activity on the bus.

The I register forms the high-order eight bits of an address. When an interrupt occurs and the Z80 is in the vectored mode, the lower order eight bits are supplied by an interrupting peripheral. In response to the interrupt, the μP does an Indirect Call instruction with the composite address. All the support chips have corresponding registers that store the low-order eight bits and supply them to the Z80 when the interrupt is acknowledged.

Able to perform 12 basic operations—add, subtract, AND, OR, Ex-OR, compare, test-bit, reset-bit, set-bit, increment, decrement, and left or right-shift and rotate (arithmetic or logic)—the ALU communicates with the registers and external-data bus by means of a buffered internal bus. As each instruction is fetched from memory, it is loaded into the instruction register and decoded by the control section, which supplies all the control signals for the Z80's subsystems.

CDP1802 programming methods and mnemonic definitions

The instruction set of the CDP1802 consists of 91 single-byte commands grouped into five basic types: register, memory and logic; arithmetic; branch, skip and control; and I/O byte transfer instructions.

Most instructions require two machine cycles (1 instruction period). The only exceptions are the long-branch and long-skip instructions, which require three cycles. Each machine cycle is internally divided into eight equal time intervals, T, so the instruction time is 16 T for two machine cycles and 24 T for three cycles.

There are four basic addressing modes of the Cosmac:

- Register. The operand's address is contained in the four lower-order bits of the instruction byte. This mode permits you to directly address any of the 16 scratch-pad registers so that you can count or move data in or out. Typical instructions might be Decrement (2N) and Get Low (8N).
- Register-Indirect. The address of the operand is stored in one of the 16-bit scratch pad registers. When you access one of the 16 registers it points to the location in memory where the operand is stored.
- Immediate. The operand is in the byte following the instruction. This mode permits you to extract data from the program stream without setting up special memory locations and pointers to them. Typical instructions include Add Immediate (FC) and Load Immediate (F8).
- Stack. One specific CPU register is implied as the pointer to memory. The stack is used as a last-in, first-out working area to store intermediate calculations and keep track of control transfers between parts of a program.

Each CPU instruction is fetched on the first machine cycle and executed during the second cycle, except for long-branch and long-skip instructions that require the first machine cycle to fetch the instruction on the second and third cycle to fetch the address (execute).

Each instruction is broken into two 4-bit hex digits, designated as I (the higher-order digit) and N (the lower-order digit). The I word specifies the instruction type, and the N word either designates the scratch-pad register to be used or acts as a special code.

Register operations include instructions that count or move data between internal 1802 registers. Memory reference commands provide directions to load or store a memory byte. Branching operations provide conditional and unconditional branch instructions that can either work in the current memory page or go to any location.

Arithmetic and Logic instructions provide many of the common operations: add, subtract, AND, OR, EX-OR and shift, while control and I/O commands take care of all the timing and data-transfer operations. The control functions facilitate program interrupt, operand selection, branch and link operations and control the Q flip-flop. The I/O functions handle memory loading and all data transfer operations into and out of the 1802.

Memory and logic instructions**

Instruction	Mnemonic	Op code
Increment reg N	INC	1N
Decrement reg N	DEC	2N
Increment reg X	IRX	60
Get low reg N	GLO	8N
Put low reg N	PLO	AN
Get high reg N	GHI	9N
Put high reg N	PHI	BN
Load via N	LDN	0N
Load advance	LDA	4N
Load via X	LDX	F0
Load via X and advance	LDXA	72
Load immediate	LDI	F8
Store via N	STR	5N
Store via X and decrement	STXD	73
OR	OR	F1
OR immediate	ORI	F9
Exclusive OR	XOR	F3
Exclusive OR immediate	XR	FB
AND	AND	F2
AND immediate	ANI	FA
Shift right	SHR	F6
Shift right with carry Ring shift right	SHRC RSHR	76*
Shift left	SHL	FE
Shift left with carry Ring shift left	SHLC RSHL	7E*

Arithmetic instructions**

Instruction	Mnemonic	Op code
Add	ADD	F4
Add immediate	ADI	FC
Add with carry	ADC	74
Add with carry immediate	ADCI	7C
Subtract D	SD	F5
Subtract D immediate	SDI	FD
Subtract D with borrow	SDB	75
Subtract D with borrow, immediate	SDBI	7D
Subtract memory	SM	F7
Subtract memory immediate	SMI	FF
Subtract memory with borrow	SMB	77
Subtract memory with borrow, immediate	SMBI	7F

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(continued from page 219)

Branch instructions		
Short branch	BR	30
No short branch (see SKP)	NBR	38*
Short branch if D = O	BZ	32
Short branch if D not O	BNZ	3A
Short branch if DF = 1	BDF	33*
Short branch if pos or zero	BPZ	
Short branch if equal or greater	BGE	
Short branch if DF = O	BNF	3B*
Short branch if minus	BM	
Short branch if less	BL	
Short branch if Q = 1	BQ	31
Short branch if Q = 0	BNQ	39
Short branch if EF1 = 1	B1	34
Short branch if EF1 = 0	BN1	3C
Short branch if EF2 = 1	B2	35
Short branch if EF2 = 0	BN2	3D
Short branch if EF3 = 1	B3	36
Short branch if EF3 = 0	BN3	3E
Short branch if EF4 = 1	B4	37
Short branch if EF4 = 0	BN4	3F
Long branch	LBR	C0
No long branch (see LSKP)	NLBR	C8*
Long branch if D = 0	LBZ	C2
Long branch if D not 0	LBNZ	CA
Long branch if DF = 1	LBDF	C3
Long branch if DF = 0	LBNF	CB
Long branch if Q = 1	LBQ	C1
Long branch if Q = 0	LBNQ	C9

*Note: This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

**Note: The arithmetic and logic instructions are the only instructions that can alter the DF.

Skip and control instructions		
Short skip (see NBR)	SKP	38*
Long skip (see NLBR)	LSKP	C8*
Long skip if D = 0	LSZ	CE
Long skip if D not 0	LSNZ	C6
Long skip if DF = 1	LSDF	CF
Long skip if DF = 0	LSNF	C7
Long skip if Q = 1	LSQ	CD
Long skip if Q = 0	LSNQ	C5
Long skip if IE = 1	LSIE	CC
Idle	IDL	00
No operation	NOP	C4
Set P	SEP	DN
Set X	SEX	EN
Set Q	SEQ	7B
Reset Q	REQ	7A
Save	SAV	78
Push X,P to stack	MARK	79
Return	RET	70
Disable	DIS	71

Input/output byte transfer instructions		
Output 1	OUT 1	61
Output 2	OUT 2	62
Output 3	OUT 3	63
Output 4	OUT 4	64
Output 5	OUT 5	65
Output 6	OUT 6	66
Output 7	OUT 7	67
Input 1	INP 1	69
Input 2	INP 2	6A
Input 3	INP 3	6B
Input 4	INP 4	6C
Input 5	INP 5	6D
Input 6	INP 6	6E
Input 7	INP 7	6F

Internal architecture of the Cosmac microprocessor

The RCA Cosmac microprocessor is a single-chip circuit handling 8-bit data. The CMOS μP comes in a 40-pin package and has an architecture based on an array of 16 general-purpose scratch-pad registers, each of which holds a 16-bit word (R registers). These registers can be used to point to data in memory, to point to programs, or to store data (two bytes per register).

Any of the 16 general-purpose registers can be designated to function as a program counter, memory-address register, data source, or data destination just by setting one of the three available 4-bit pointers, the N, P and X registers.

The D register, which holds 8 bits, buffers data transfers between the scratch-pad registers and the data bus and functions as an accumulator.

By changing the contents of the P register, you can point to a different R register (thus changing the program counter). The N register stores a variable pointer that is directed by the instruction. The other 4-bit register, X, stores a pointer that designates an address register during I/O and some ALU instructions. Like the P register, it can be loaded by a single instruction.

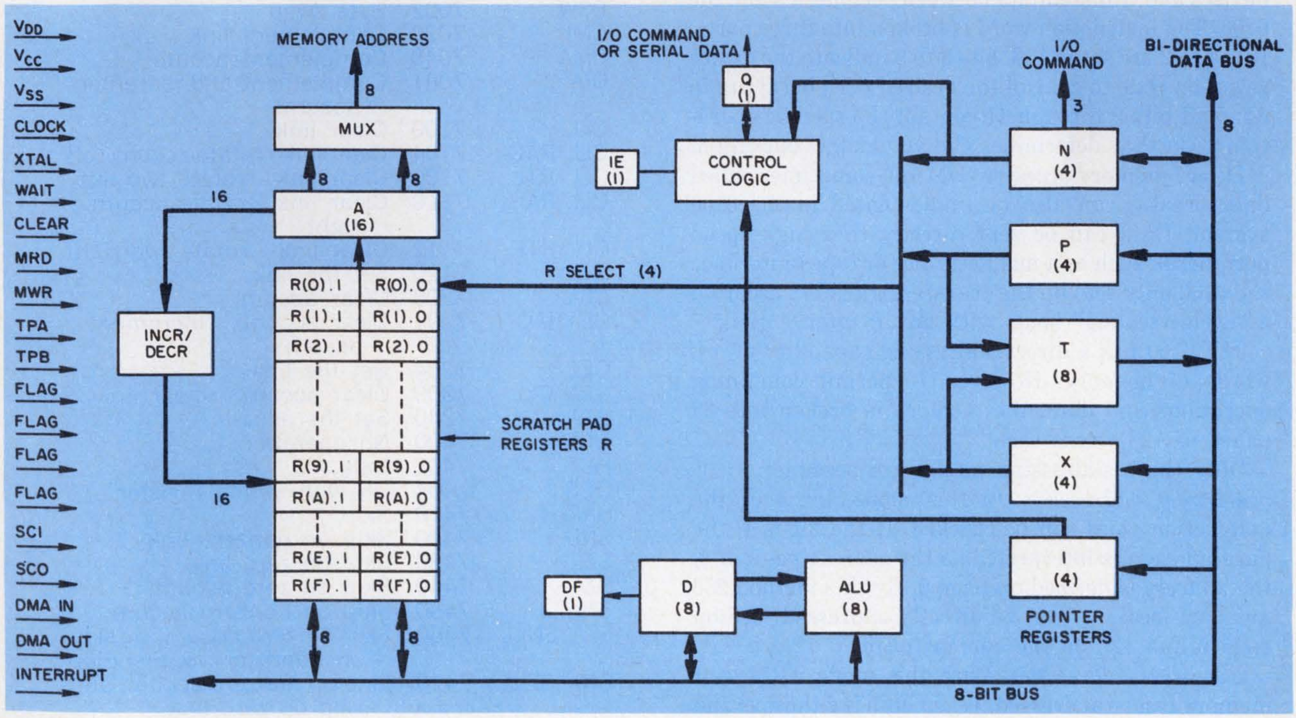
The use of the N, P and X registers to indirectly specify a 16-bit address is a key feature of the 1802 μP. In addition to the register arrays, the 1802 contains a conventional arithmetic and logic unit that performs operations between data stored in the D register and in memory, with the result stored in D. An overflow bit, DF, is also available and can be used for conditional branching.

Instruction cycles are divided into fetch and execute halves often referred to as machine cycles. During the fetch cycle, instructions are brought from the program memory, the four most-significant bits are placed in the I register, and the four least-significant bits are funneled into the N register. The I register designates a class of instructions, and the N register defines the specific processor operation.

The 15 lines of I/O interface offer some unique features:

- Four input flags, which can be tested by condition branch instructions.
- A serial output, which can be set and reset under program control and tested by conditional branch instructions.
- Programmed I/O data transfer, which uses the data in the N register as a device-select code, then transfers data between the device and memory.
- A maskable interrupt, which is activated by a single input. When an interrrupt occurs, the old values of the P and X registers are automatically saved in a temporary register, T, and new values are jammed into the P and X registers.
- A DMA channel, which can be activated by either of two control lines, uses the R(Ø) register as a pointer. Each DMA request causes one machine cycle to be stolen, generates appropriate memory address and control signals, and increments the pointer.
- Timing signals, which provide synchronization to assist in data transfers and general system timing functions.

The 8-bit ALU performs all the arithmetic and logic operations. Operand bytes are pulled from the D register and from the memory (on the data bus).



Instruction set and addressing schemes of the 6100

Instructions of the 6100 are 12 bits long and can be broken into three major groups: memory reference instructions (MRI), operate instructions (OI) and input/output transfer instructions (IOT). All of the over 70 instructions are software compatible with the PDP-8/E command set. The basic PDP-8/E papertape software are supplied by Digital Equipment Corp. can operate with the 6100.

The MRI instructions either operate on the contents of a memory location or use the contents to operate on the AC or PC. Each MRI is broken into two parts: Bits 0 to 2 represent the operation code, the other nine bits the operand address.

Operate instructions are broken into three groups of microinstructions. Group 1 commands perform logic operations on the contents of the accumulator and link registers and are identified by a ∅ in the bit-3 position. Group 2 microinstructions primarily test the contents of the accumulator or link and then conditionally skip the next sequential instruction. They require a 1 in the bit-3 position and a ∅ in the bit-11 position. The Group 3 microinstructions perform logic operations on the contents of the AC and MQ registers and have a 1 in the bit-3 and bit-11 positions.

Operate microinstructions from a certain group can be microprogrammed with other microinstructions from that same group, thus reducing the number of lines of code. The actual code for a microprogrammed combination of two or more microinstructions is a logic OR of the octal codes for the individual commands.

IOT instructions initiate the operation of peripheral devices and transfer data between peripherals and the 6100. The instruction word is broken into three parts: Bits ∅ to 2 are set to 11∅, bits 3 to 8 indicate the device selection code to control the desired peripheral (up to 64), and bits 9 through 11 contain the specific operation code that determines the actual I/O operation.

Direct memory accesses (DMAs), sometimes called data breaks, can also be implemented in the 6100 system. Data can be sent directly to a high speed peripheral, such as a magnetic disc or tape unit. Since the 6100 only sets up the transfer, transfers occur on a "cycle stealing" basis with no μP intervention.

The 6100 has a direct addressing capability of 4 k words of memory. However, to permit combining operations and data, the memory is broken into 32 pages of 128 words each.

Only three addressing modes are possible:

■ *Direct addressing.* In this mode, bit 4 of the instruction word can be checked. If the bit is 1, the page address is interpreted as the current page; if ∅, the address is defined on page ∅. By this method 256 memory locations can be directly addressed (128 on page ∅ and 128 on the current page.

■ *Indirect addressing.* With this mode, all 4 k of memory can be addressed. When bit 3 is ∅ the operand address is obtained by first referencing a "pointer" address that is located either on the current page or page ∅ of the memory. The address of the data or instruction to be handled is in the location specified by the pointer.

■ *Auto-indexed addressing.* Within the 6100, provisions have been made for an external stack of eight registers (memory locations ∅∅1∅ to ∅∅17, octal) that can be used for indexing applications. Whenever these locations are indexed indirectly, the contents are incremented by 1 and restored before they are used as an operand address.

Memory reference instructions

Mnemonic	Octal code	Operation
AND	0000	Logic AND
TAD	1000	Binary ADD
ISZ	2000	Increment, and skip if zero
DCA	3000	Deposit and clear AC
JMS	4000	Jump to subroutine
JMP	5000	Jump
IOT	6000	In/out transfer
OPR	7000	Operate

Operate instructions

NOP	7000	No operation
IAC	7001	Increment accum.
RAL	7004	Rotate accum. left
RTL	7006	Rotate two left
RAR	7010	Rotate accum. right
RTR	7012	Rotate two right
BSW	7002	Byte swap
CML	7020	Complement link
CMA	7040	Complement accum.
CIA	7041	Complement and increment accum.
CLL	7100	Clear link
CLL RAL	7104	Clear link - rotate accum. left
CLL RTL	7106	Clear link - rotate two left
CLL RAR	7110	Clear link - rotate accum. right
CLL RTR	7112	Clear link - rotate two right
STL	7120	Set the link
CLA	7200	Clear accum.
CLA IAC	7201	Clear accum. - Increment accum.
GLT	7204	Get the link
GLA CLL	7300	Clear accum. - clear link
STA	7240	Set the accum.
NOP	7400	No operation
HLT	7402	Halt
OSR	7404	OR with switch register
SKP	7410	Skip
SNL	7420	Skip on nonzero link
SZL	7430	Skip on zero link
SZA	7440	Skip on zero accum.
SNA	7450	Skip on nonzero accum.
SZA SNL	7460	Skip on zero accum. or skip on nonzero link or both
SNA SZL	7470	Skip on nonzero accum. and skip on zero link

SMA	7500	Skip on minus accum.
SPA	7510	Skip on positive accum.
SMA SNL	7520	Skip on minus accum. or skip on nonzero link or both
SPA SZL	7530	Skip on positive accum. and skip on zero link
SMA SZA	7540	Skip on minus accum. or skip on zero accum. or both
SPA SNA	7550	Skip on positive accum. and skip on nonzero accum.
SMA SZA SNL	7560	Skip on minus accum. or skip on zero accum. or skip on nonzero link or all
SPA SNA SZL	7570	Skip on positive accum. and skip on nonzero accum. skip on zero link
CLA	7600	Clear accum.
LAS	7604	Load accum. with switch register
SZA CLA	7640	Skip on zero accum. then clear accum.
SNA CLA	7650	Skip on nonzero accum. then clear accum.
SMA CLA	7700	Skip on minus accum. then clear accum.
SPA CLA	7710	Skip on positive accum. then clear accum.
NOP	7401	No operation
MQL	7421	MQ register load
MQA	7501	MQ register into accum.
SWP	7521	Swap accum. and MQ register
CLA	7601	Clear accum.
CAM	7621	Clear accum. and MQ register
ACL	7701	Clear accum. and load MQ register into accum.
CLA SWP	7721	Clear accum. and swap accum. and MQ register
SKON	6000	Skip if interruption on
ION	6001	Interrupt turn on
IOF	6002	Interrupt turn off
SRQ	6003	Skip if INT request
GTF	6004	Get flags
RTF	6005	Return flags
SGT	6006	Operation is determined by external devices, if any
CAF	6007	Clear all flags

Input/output instructions

Teletypewriter keyboard/reader

KCF	6030	Clear keyboard/reader flag, do not start reader
KSF	6031	Skip if keyboard/reader flag = 1
KCC	6032	Clear AC and keyboard/reader flag, set reader run
KRS	6034	Read keyboard/reader buffer static
KIE	6035	AC 11 to keyboard/reader interrupt enable FF
KRB	6036	Clear AC, read keyboard buffer, clear keyboard flags

Teletypewriter teleprinter/punch

SPF	6040	Set teleprinter/punch flag
TSF	6041	Skip if teleprinter/punch flag = 1
TCF	6042	Clear teleprinter/punch flag
TPC	6044	Load teleprinter/punch buffer select and print
SPI	6045	Skip if teletypewriter interrupt
TLS	6046	Load teleprinter/punch buffer, select and print and clear teleprinter/punch flag

A look inside the 6100 microprocessor

Since the 6100 microprocessor was designed to emulate the PDP-8/E minicomputer made by Digital Equipment Corp., it should come as no surprise that the μP is also architecturally identical. The 6100 has six 12-bit registers, an arithmetic-and-logic unit (ALU), all the gating and timing logic, and the instruction-decode and control ROM.

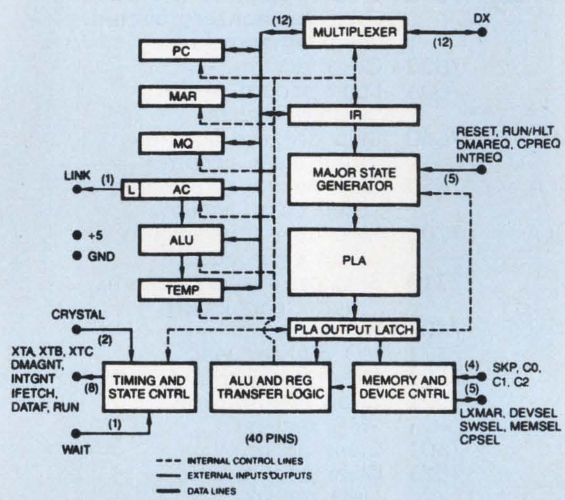
The accumulator register (one of the six just mentioned) is the central focus point of the 6100. All the arithmetic and logic operations are performed in it. For any ALU operation, the data held in the accumulator and the data fetched from memory are combined and stored (temporarily) back in the accumulator. Under software control, the accumulator can be cleared, set, complemented, tested, incremented or rotated. The accumulator also serves as an input/output register since all I/O transfers must pass through it.

A one-bit extension called the link is built into the accumulator. It can be complemented with a carry out of the ALU or cleared, set, complemented, tested and rotated along with the rest of the accumulator—all under program control. The link also serves as the carry output for two's complement arithmetic.

The other 12-bit registers include the MQ, a programmable register that can be used as a temporary storage location. The TEMP register can be used for microprogram control and helps to avoid race conditions. The MAR register holds the current address of the memory location selected for reading or writing. And, of course, both arithmetic and logic operations are done in the 12-bit ALU, as well as shifting left or right.

The PC (program counter) register holds the address of the memory location from which the next instruction will be fetched. During normal operation (an instruction fetch), the contents of the PC are transferred to the MAR, and the PC gets incremented by one. Of course, a jump or skip instruction modifies the procedure. Also included on the chip is a 12-bit instruction register (IR) that holds the instruction to be executed.

Data and addresses share a common 12-line bus that feeds directly into a 12-bit multiplexer. The multiplexer, in turn, is controlled by the major-state generator and control ROM. All timing and state signals needed by the 6100 are generated by an on-chip clock (only a 4-MHz crystal is required). An internal dividing circuit reduces the clock so that the internal states are 500 ns long.



Programmed data transfers, the easiest means of controlling data I/O, require the least hardware support. However, to use this form of I/O, the 6100 must remain in an idle state (wait loop), while the I/O device completes its last transfer and prepares for the next. Interrupts can reduce or totally eliminate the time waiting for device status signals.

Whenever the INTREQ input is driven LOW, the interrupt system permits external signals to divert the program to a preselected subroutine. If no higher priority requests for an interrupt exist, the current request is granted when the 6100 completes its current instruction. After reacting to an interrupt request, the Interrupt-Enable flip-flop in the 6100 gets reset so that no other interrupts can be acknowledged until the current interrupt is serviced and the system goes back to program control.

Instruction set for the TMS9900

The TMS9900 16-bit microprocessor's instruction set consists of 69 basic commands that are loosely grouped into four classes: control; data transfer; internal-register operations; and arithmetic, logic and data manipulation commands. Various modes are also contained to address data held in RAM.

Eight basic addressing modes are available: workspace-register addressing, workspace-register indirect addressing, workspace-register indirect auto-increment addressing, symbolic (direct) addressing, indexed addressing, immediate addressing, program-counter relative addressing, and communications-register unit addressing.

Instruction-execution times are a function of the clock speed, addressing mode and the number of wait states required for each memory access. Two of the most powerful instructions include the binary 16-bit multiply and divide commands (MPY and DIV), which typically execute in a maximum of 52 and 124 clock cycles, respectively. (Assuming a 300-ns clock period, this translates into 15.6 and 37.2 μs, about 10 to 100 times faster than processors that must be programmed for the instructions.)

The instruction set also contains five external commands that allow user-defined external functions to be initiated under program control. When any of the commands (CKON, CKOF, RSET, IDLE, and LREX) are executed, a unique 3-bit code appears on the most significant three bits of the address bus, along with a CRUCLK pulse. When the processor is in the idle state, the code and pulse occur repeatedly until the state is terminated. By decoding the code, special instructions can be implemented.

The instruction set breaks down as follows: 26 arithmetic, logic and data manipulation commands; 14 internal-register-to-memory operations; five data-transfer commands; and 24 control functions. All instructions are software-compatible with the 990 family of minis made by Texas Instruments.

Dual operand instructions	
Mnemonic	**Definition**
A	Add
AB	Add bytes
C	Compare
CB	Compare bytes
S	Subtract
SB	Subtract bytes
SOC	Set ones corresponding
SOCB	Set ones corresponding bytes
SZC	Set zeros corresponding
SZCB	Set zeros corresponding bytes
MOV	Move
MOVB	Move bytes
COC	Compare ones corresponding
CZC	Compare zeros corresponding
XOR	Exclusive OR
MPY	Multiply
DIV	Divide
XOP	Extended operation

Single operand instructions	
B	Branch
BL	Branch and link
BLWP	Branch and load workspace pointer
CLR	Clear operand
SETO	Set to ones
INV	Invert
NEG	Negate
ABS	Absolute value*
SWPB	Swap bytes
INC	Increment
INCT	Increment by two
DEC	Decrement
DECT	Decrement by two
X**	Execute
CRU instructions	
LDCR	Load communication register
STCR	Store communication register
SBO	Set bit to one
SBZ	Set bit to zero
TB	Test bit
Jump instructions	
JEQ	Jump equal
JGT	Jump greater than
JH	Jump high
JHE	Jump high or equal
JL	Jump low
JLE	Jump low or equal
JLT	Jump less than
JMP	Jump unconditional
JNC	Jump no carry
JNE	Jump not equal
JNO	Jump no overflow
JOC	Jump on carry
JOP	Jump odd parity
Shift instructions	
SLA	Shift left arithmetic
SRA	Shift right arithmetic
SRC	Shift right circular
SRL	Shift right logical
Immediate register instructions	
AI	Add immediate
ANDI	AND immediate
CI	Compare immediate
LI	Load immediate
ORI	OR immediate
LWPI	Load workspace pointer immediate
LIMI	Load interrupt mask
STST	Store status register
STWP	Store workspace pointer
RTWP	Return workspace pointer
External instructions	
IDLE	Idle
RSET	Reset
CKOF	User defined
CKON	User defined
LREX	User defined

Operand is compared to zero for status bit.
If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the TMS 9900 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

Internal architecture of the TMS9900

The TMS9900 is a 16-bit microprocessor that uses a memory-to-memory architecture for multiple-register files. As a result, it responds quickly to interrupts and has a high degree of programming flexibility. Inside, three 16-bit registers serve as the program counter, workspace pointer and status register.

Blocks of memory are designated as workspace to replace internal hardware registers. The first 32 words of memory are allocated for interrupt trap vectors. The next 32 words are used by the extended-operation instruction for trap vectors. The last two memory words in the memory space serve as the trap vector of the load signal.

If needed, the allocated areas can be used as general memory. The remaining memory space is available for program storage.

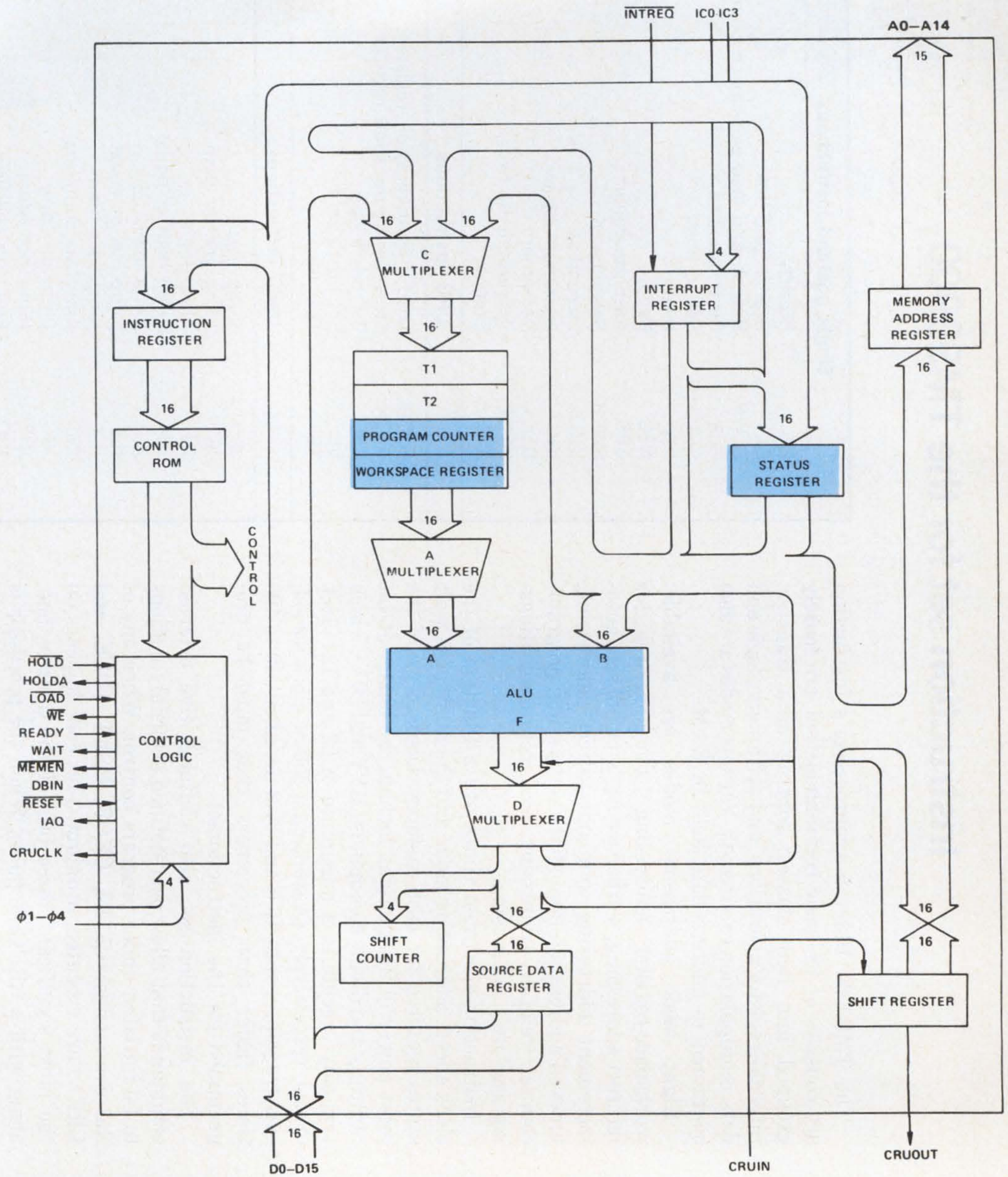
The TMS9900 has a full 16-bit arithmetic and logic unit capable of multiplication and division in addition to 67 other basic instructions.

Sixteen levels of prioritized interrupt are built-in. The processor continuously compares the interrupt code with the interrupt mask stored in the status register. When the processor recognizes an interrupt, it initiates a register-swap operation to exchange the contents of the program counter, workspace pointer and other registers with the interrupt vectored data.

Input/output operations are performed via a direct, command-driven interface support circuit that can provide up to 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields of 1 to 16 bits. Three dedicated processor pins and 12 address lines are used to interface to the I/O.

A typical minimum system using the TMS9900 would consist of the processor, the clock generator, some latches for I/O and some RAM and ROM for program control and storage.

The processor has an addressing range of 32,768 16-bit words and comes in a 64-pin dual-in-line package. To operate, the processor requires a four-phase clock input along with three power supplies. An I²L version, the SBP9900, that uses a single supply and single-phase clock is also available.



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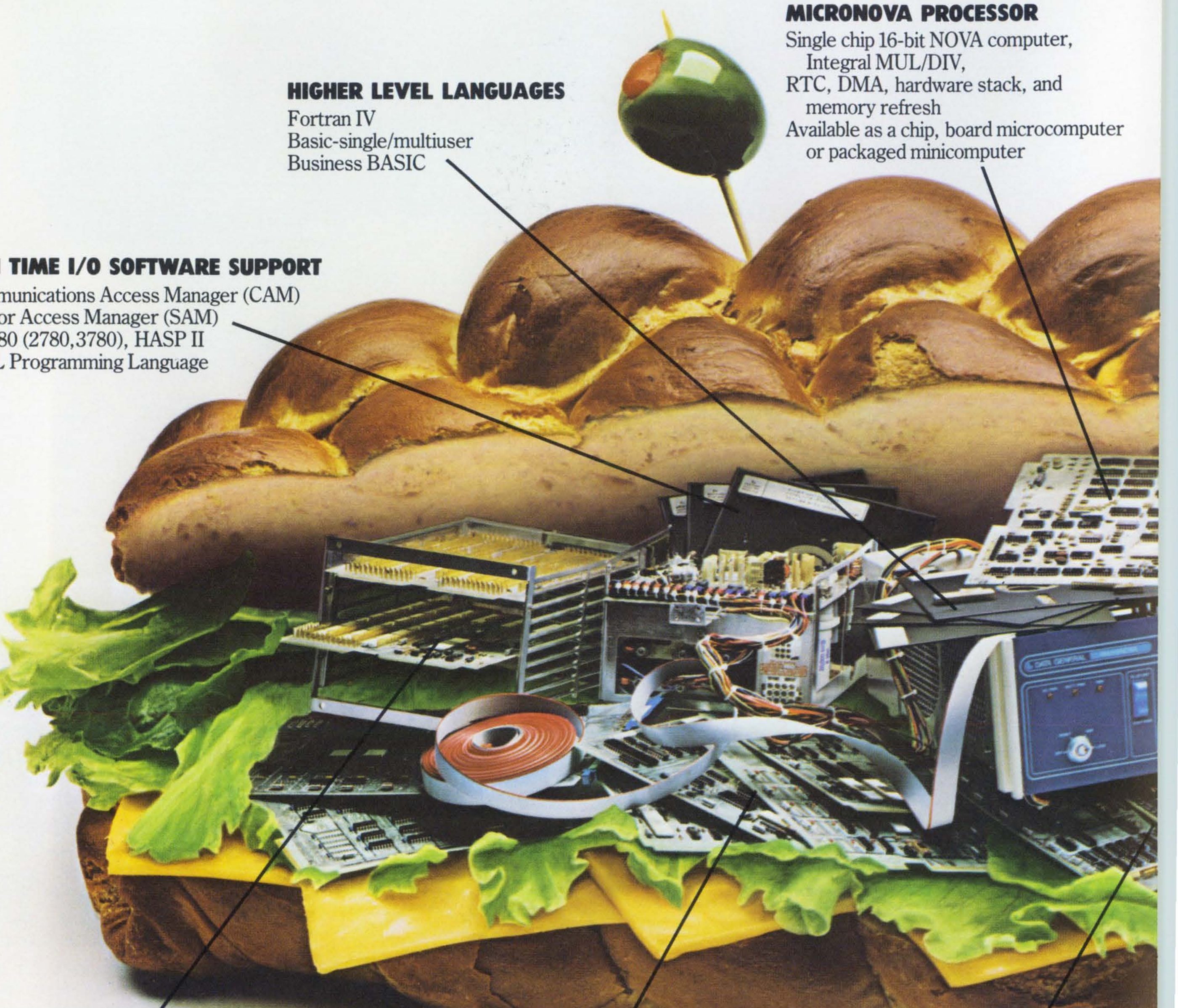

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CIRCLE NUMBER 175

Developing microcomputer software requires a thorough knowledge of μP operation. Internal registers and addressing modes are just two important aspects to examine.

Designing with microprocessors and microcomputers has become more of a programmer's job than a circuit designer's. Circuits fit together like building blocks, but software holds the blocks together. Consequently, to design with micros, you not only have to use your design expertise, but you have to know programming as well.

When the discussion turns to software, don't get discouraged—you don't have to feel as though you've walked into a four hour discussion during the third hour. Review some of the fundamentals of micros and programming, and you'll be able to lead the discussion instead of listening.

This article is aimed at the programming novice. While no knowledge of microprocessors is required, a little background of computer and digital terminology will help. What's more, those of you who do microprocessor programming will find some new ideas and a good review of some fundamental programming concepts.

A microcomputer is a collection of circuits, including a microprocessor or custom LSI processing element, and needs just a power supply and program to perform. Included in a microcomputer are input/output control lines with the necessary buffering, communications channels, and enough RAM and ROM space to hold the programs.

The core of most microcomputer systems is a microprocessor. On a single chip, it has arithmetic processing circuits, control memory for its basic instruction set, and, depending on the model, such features as a clock oscillator, random-access read/write memory or read-only memory.

Both a simple microcomputer system and a microprocessor require software (programs) to perform the control of input/output operations and communications operations (Fig. 1).

A microprocessor may be the focal point in most microcomputer systems, but it's not alone. Memories are used to hold programs and any data that must be manipulated by the instructions. Programs are stored in the memory as a series of binary words, each word containing from four to 16 bits depending on the type of processor used. Each word or series of words represents an instruction or data that the microprocessor will decode or act upon when that information is presented to the processor input.

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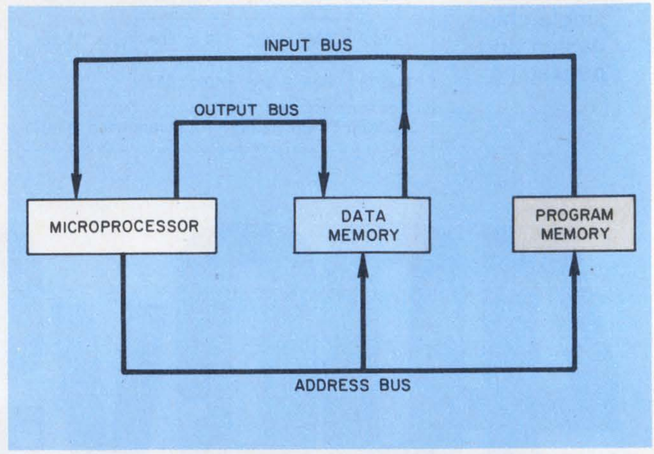
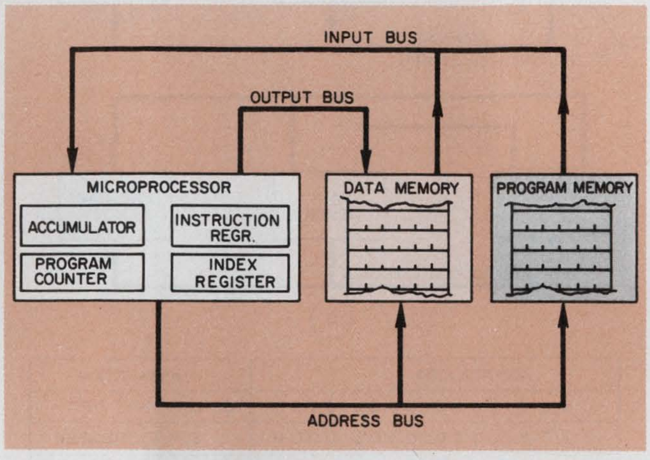


1. **Programs and data** stored in a microcomputer's memory provide all the control for a simple μP-based system.

Like a microprocessor, a microcomputer can be treated as a sort of "black box" for software. Either "box" communicates with the outside world via three paths—the data bus, the address bus and the control bus. The data bus is a set of parallel-line signals that permits bidirectional digital-data transfer. It can have 4, 8, 12, or 16 lines, depending on the processor used. The digital words transmitted over the data bus are either instructions for the processor, the data to be manipulated or the processed results of the data.

The address bus, typically 16 lines, sends its address request to the computer's memory. The binary number represented by the logic state of all 16 lines is the memory-address location that the processor wants to access.

The processor is controlled by several lines called the control bus. These lines, some of which are outputs and some inputs, perform basic operations typically required, such as halt, start, reset, wait, and interrupt. Some lines serve also to control other parts of the computer system. For example, a Read/Write line can be used to control the system memory for read and write operations.



2. **Four basic registers inside the microprocessor** help the μC keep track of the program, data and I/O operations.

A microprocessor has all three buses just discussed, but may not have any specialized input/output lines. A microcomputer, on the other hand, may not have the address bus available to the outside, although one may be on the board for internal use. A microcomputer, though, will have a control bus and many I/O lines for transmitting data or control signals back and forth.

Internal registers control operations

Inside a microcomputer's microprocessor, registers help to control and keep track of various operations (Fig. 2). Every microprocessor has the following four registers:

- Accumulator (AC), which is the focal point for all data manipulation operations. Numbers are added to or subtracted from the AC. Shift operations and complementing can also be done, as well as many Boolean operations. Some processors have more than one register to perform these functions.
- Index register (IR), which is used to hold the addresses of important memory locations. This register can usually be incremented and loaded by various instructions. It functions as a pointer to direct the processor to an area of memory containing the necessary information.
- Instruction register (INR), which holds the instruction during the instruction decode and execute phase of microprocessor operation. This register receives the instructions from the program memory.
- Program counter (PC), which keeps track of the processor's progress through the program. Often, the processor has instructions that can modify the way the counter behaves (decrementing instead of incrementing, skipping a count, branching to a completely new number, etc.).

To transfer data back and forth, microcomputer or microprocessor systems commonly use 8-bit words (often referred to as bytes). The sequence that accomplishes the transfer or performs an operation is called an instruction cycle. A basic instruction cycle is actually three instructions (Fig. 3a):

1. Fetch the next instruction (access the memory and pull the word stored in the specified location into the processor).
2. Increment the PC.
3. Execute the instruction.

Look at a simple three-step program that first sets an AC to zero, increments it, and shifts the it up one bit (Fig. 3b). To follow the sequence of events, you must first assume that the processor's PC has been set to a predetermined value—say, zero—by a previous instruction.

The program starts when the processor sends out the contents of the PC on the address bus (memory-address zero is being accessed). Some control signals are used to tell the memory whether a read or write operation is taking place. When the memory is accessed, the instruction or data held in the memory gets placed on the data bus; in this case, the instruction is "Set AC to zero." The processor then pulls the instruction in from the data bus and loads it into the INR. Next, the contents of the PC are incremented.

Finally, the instruction is executed and the AC is set to all zeros. With instruction 1 completed, the process repeats with address 0001_H sent out to the memory. Unless there is an instruction to tell the processor to stop sending out addresses at the beginning of each cycle, the computer will just go on to the next address once the program has finished and access that instruction.

If each instruction is limited to one byte, processors that have 8-bit-wide buses will be limited to no more than 256 instructions. To overcome this, many processors use multiple-byte instructions where the actual instruction is broken down into two or three sequential bytes and automatically executed in sequence.

Instructions that reference the memory—"Read data from location XXXX" or "Write data into location XXXX"—are good examples of three-byte operations. The first byte is the command, and the next two bytes contain the address location. Depending on the processor, you will either get the lower or higher byte first; what's important is that you know which one you're getting.

For the processor to handle multiple-byte instructions, it must be modified so that the instruction cycle treats all but the last byte of a multiple-byte instruction as instructions requiring no action. When a multiple-byte instruction is transmitted from the program memory to the processor, the code of the first byte is recognized as a three-byte instruction and the processor waits until the third byte before executing the full instruction. During the first two cycles it rebuilds the 24-bit instruction from the separate bytes. Generally, the first byte of the instruction is known as the operation, or op code, and the other bytes are known, quite naturally, as the address.

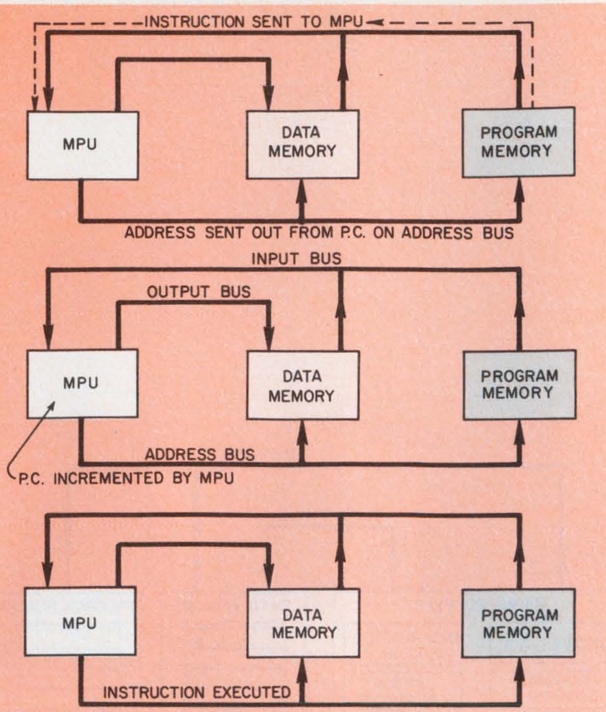
Instructions fall into four groups

There are basically four types of commands used by all computer systems, and micros are no exception:

1. *Arithmetic and logic instructions*, which perform all the number and data manipulation.
2. *Memory-reference instructions*, which tell the computer where in the memory to load or access the instructions or data.
3. *Jump and branch instructions*, which modify the contents of the PC so that the processor can alter the flow of the program.
4. *Input and output instructions*, which let the processor communicate with the outside world and control things.

The arithmetic and logic section within the microprocessor—the ALU—performs all the manipulation for the instructions that deal with mathematical and Boolean operations: addition, subtraction, shifting, ANDing, ORing, etc. How many different operations are available depends on the built-in capabilities of the processor. For operations that require two operands—addition, for example—the accumulator often can be the source for one, while the other is usually brought in from some other source such as a memory location or register.

Several flip-flops are often used in addition to the AC to store special indicator bits, or flags, of certain operations. A flag register usually has bits to indicate the results of operations such as overflow, zero AC, carry, and other possibilities. Flag bits usually operate as follows: If an addition taking place in the AC produces a result larger than the eight bits of the AC can represent, the overflow flag is set (the flip-flop's output is set to ONE).



(a)

ACCUMULATOR	INSTRUCTION
d d d d d d d d d d d d d d d d	BEFORE FIRST INST.
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SET AC TO ZERO
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	INCREMENT AC
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	SHIFT AC 1 PLACE

(b)

3. **The basic instruction cycle for a microprocessor** can be broken into three stages (a). All operations on data are performed in the processor's accumulator (b).

During operations such as a shift, the bit representing the most significant bit of the AC can be shifted into the flag so that the flag bit is treated as an extension bit to the AC. Some processors leave it up to you to include the bit or not.

A carry-link flag, available in many microprocessors, can be considered a one-bit extension to the AC. By rotating the AC through the flag bit, you can access and modify any bit within the AC. This can turn out to be slow when, for example, bit 4 of an 8-bit accumulator must be complemented (Fig. 4). Such a program will require four shifts to the left, a complement carry-link flag, and four shifts to the right—nine instructions all told.

Alternatives depend on the processor's instruction set. If the CPU has an Exclusive-OR instruction, just Ex-OR the AC with 10_H. The same results will be achieved, but with only two bytes of program memory. Some processors even have instructions that permit them to manipulate individual bits in their AC, thus reducing the job to one instruction.

A typical list of possible flag indicators is given in Table 1, and a list of some arithmetic and logic instructions in Table 2.

Table 1. Typical flag-register bits

Flag	Indicator
Carry	Indicates a carry from an arithmetic operation
Overflow	Indicates an overflow from an arithmetic operation
Link	Indicates when a shift operation has reached a certain point
Sign	Indicates the sign of the number in the AC
Parity	Indicates odd or even parity of the AC contents
Auxiliary	Indicates a carry from the lower half byte to the upper half byte of the AC (this flag is used when the processor performs decimal operations)

Table 2. Common ALU instructions

Mathematic	Logic
Add	Exclusive-OR
Subtract	Complement
Shift left (multiply by 2)	Clear AC
Shift right (divide by 2)	AND
Increment	OR
Decrement	Compare
Various instructions that permit manipulation of the ALU flags and I/O port bits.	

A memory-reference instruction performs operations on the data or program memory. Very often, the instruction can contain an arithmetic or logic function along with the memory reference.

Realistically, the memory is a larger part of the over-all system than the processor, so when you select a processor, you should check the efficiency of all memory-reference instructions.

Memory-reference instructions usually fall into two broad categories—those addressing data, and those addressing the program memory. Generally, once a program is in a microcomputer system it doesn't modify itself—which means that information is not normally written into the program memory during operation. Therefore, most program-memory-reference instructions are similar to "Read contents of program memory location ABCD."

There are two reasons for this programming philosophy: First, it makes system "crashes" less likely; second, program memory is usually a read-only type, so writes are impossible unless the ROM is a phantom. In that case, at system start-up, the contents are transferred into overlapping RAM.

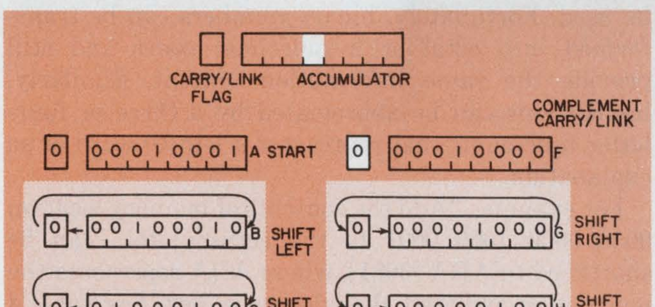
Memory references are typically required by Add and Subtract instructions and more advanced commands such as Multiply and Divide. All four commands require two operands, which must be pulled into the AC from the memory. As a result, the instructions have an extended instruction cycle. After the first operand is loaded into the AC, the index register is commonly used to specify one of the memory locations. However, there are many ways to specify a memory location, as the rest of this article will show.

Some typical memory-reference commands are shown in Table 3. The first five instructions have two operands; while one is held in the AC, the other is combined with the contents of the AC in the manner specified. The result remains in the AC.

The last four typical commands start with a single operand in a specified memory address. The operand is brought to the ALU, and after the command performs the specified operation, it places the result back into the location. The original contents of the AC are not affected by most of these operations.

Hop around with jump commands

Jump and branch instructions permit the processor to hop about nonsequentially within a program. For instance, if a program contains three jobs, A, B, and C, and each is a complete program section in itself, or subroutine, the processor can be directed to perform them in any order. It simply has to be told where to go to in the program flow. This is done by loading



4. **To alter the state of accumulator bit 4,** the entire contents of the accumulator must be shifted through the carry-link bit of the μP. Once changed, they must be shifted back again to their original position.

the PC with the address of the first instruction of the desired subroutine (Fig. 5).

Such a jump or branch instruction is referred to as an unconditional jump since the jump will occur no matter what the external or internal conditions are. But a more powerful jump command, the conditional jump, checks certain internal register conditions or external conditions.

Upon meeting one of the specified conditions, the program will change its flow. For example, an instruction might be "If condition X is true, then jump to instruction XXXX, otherwise perform the next sequential instruction." Flag bits often serve as the check points for conditional jumps, although processors with I/O lines can often test the status of individual lines.

Input/output instructions permit the processor to communicate with other types of equipment. The channels of communication are referred to as ports, and eight parallel I/O lines are called a parallel port. If just one line is used, it can be referred to as a serial port. However, communication usually occurs on both directions, and a port that can handle the data flow both ways—in and out—is called a bidirectional port.

Inevitably, a fifth category of "special instructions" will become part of the instruction-set groupings. But with the groupings as loosely defined as they are, you'll have a hard time deciding where to fit them in. Typical special instructions include such operations as stop, delay for n seconds, do nothing, etc.

Now that you know the various kinds of instructions you'll use in a microcomputer, you can write them. Work with binary numbers, however, and you'll soon be looking for a better way.

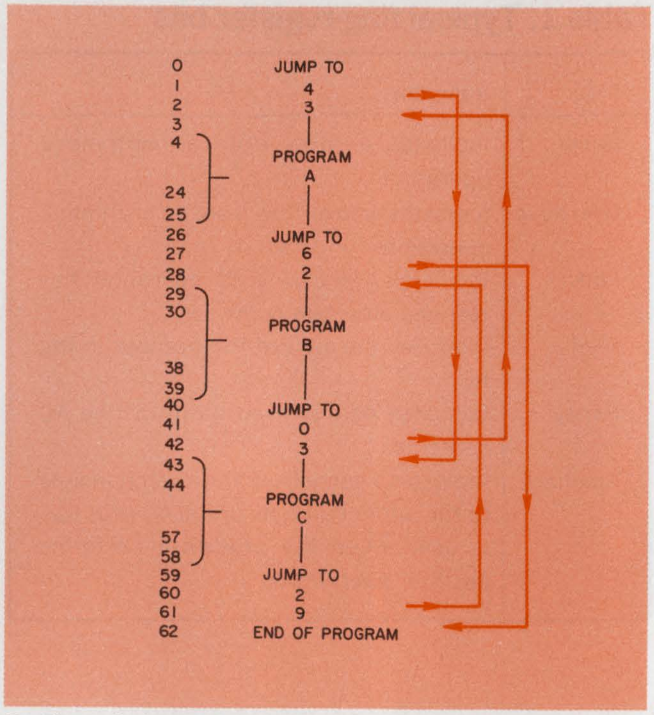
Recode binary to simplify programming

Binary numbers can make instruction writing very cumbersome, very soon. For every address, 16 bits must be written; for every instruction, eight bits must be used. Fortunately, binary numbers can be transformed into octal or hexadecimal codes and still provide the same information content. Similarly, instructions can be abbreviated by a three or four-letter mnemonic that represents a 1-to-10 word or so explanation.

For example, "Add the contents of memory location 0000 0000 1000 0001 to the accumulator" can be shortened to ADA [0081], where ADA represents the instruction and 0081 the address in hex. See Table 4 for a binary/octal/decimal/hex conversion chart for 0 to 15.

Unfortunately, however, each microprocessor has its own set of mnemonics and its own instructions, albeit similar. There is no standardization, and thus, for each microprocessor, the learning process starts all over again.

Only the sequence of events in developing the program remains constant. Programs written in binary, octal or hex codes are machine-language



5. **Three independent subprograms,** A, B and C, can be set to run in any order by a larger supervisory program. All the program must do is initiate each of the smaller programs and wait for that routine to finish.

Table 3. Memory-reference commands

Add contents of specified memory location to AC
Subtract contents of specified memory location from AC
AND contents of specified memory location with AC
OR contents of specified memory location with AC
Exclusive-OR contents of specified memory location with AC
Shift contents of specified location one place to the left
Shift contents of specified location one place to the right
Increment the contents of the specified location
Decrement the contents of the specified location

programs, while programs written using mnemonics are assembly-language programs.

In any computer system, the processor manipulates binary information stored in the program and data memory. How easily and quickly the processor can access the information will determine the computer's maximum operating speed, and, to some extent, the length of the program.

The ability to operate with numbers formatted in binary-coded decimal (BCD) is an important feature available in most microcomputers and microprocessors. These devices are often used in a

```
 0010 1000
 0011 1001
 ---------
 0110 0001
```

6. **Unless a processor works completely in BCD** when performing BCD operations, results of any calculation must be adjusted by a Decimal Adjust Accumulator command included after the calculation.

Clear AC	1 byte
Add [ABCA]	3 bytes
Add [ABCB]	3 bytes
Add [ABCC]	3 bytes
Add [ABCD]	3 bytes
Shift right	1 byte
Shift right	1 byte
Total memory requirement = 15 bytes	

7. **Using direct addressing** to average the sum of four numbers, a typical microcomputer program might require seven instructions and 15 bytes of memory.

Clear AC	1 byte
Add @ [ABCE]	3 bytes
Increment [ABCE]	1 byte
Add @ [ABCE]	3 bytes
Increment [ABCE]	1 byte
Add @ [ABCE]	3 bytes
Increment [ABCE]	1 byte
Add @ [ABCE]	3 bytes
Shift right	1 byte
Shift right	1 byte
Total memory requirement = 18 bytes	

8. **By converting the program in Fig. 7 into an indirectly addressed version,** more memory space and time are required for execution. However, for examples more complex than this simple averaging problem, indirect addressing can save many memory locations.

Table 4. Binary/octal/decimal/ hex conversion chart

Binary	Octal	Decimal	Hexa-decimal
0000 0000 0000 0000	000 000	00000	0000
0000 0000 0000 0001	000 001	00001	0001
0000 0000 0000 0010	000 002	00002	0002
0000 0000 0000 0011	000 003	00003	0003
0000 0000 0000 0100	000 004	00004	0004
0000 0000 0000 0101	000 005	00005	0005
0000 0000 0000 0110	000 006	00006	0006
0000 0000 0000 0111	000 007	00007	0007
0000 0000 0000 1000	000 010	00008	0008
0000 0000 0000 1001	000 011	00009	0009
0000 0000 0000 1010	000 012	00010	000A
0000 0000 0000 1011	000 013	00011	000B
0000 0000 0000 1100	000 014	00012	000C
0000 0000 0000 1101	000 015	00013	000D
0000 0000 0000 1110	000 016	00014	000E
0000 0000 0000 1111	000 017	00015	000F

man/machine interface and direct operation on BCD data provides a faster response. Several levels of BCD operations are possible—from simple instructions that convert the result of a BCD addition back into BCD right up to the processors that can operate throughout in either BCD or two's-complement binary mode.

Suppose 28 is added to 39, and both numbers are represented in an 8-bit BCD format (Fig. 6). The result is not a BCD representation of the result, but a binary sum of the two BCD numbers. To obtain the true BCD result, the processor must execute a special instruction to convert the number in the processor's AC back into BCD. The instruction, usually referred to as a decimal adjust accumulator (DAA), uses the information that a carry has occurred from the low-order BCD character to the high-order character to restore the least-significant digit to its correct value, 0111. So for each BCD operation, the program must contain an extra instruction. Some processors have separate binary and BCD math instructions and will thus not require the DAA operation. Table 5 shows the complete algorithm for the DAA instruction.

As with many math operations, each time the processor performs an operation, certain flags get set or reset. These flags are often grouped together and referred to as the program-status word, and can be considered an additional register in the processor.

Two flags that appear redundant at first are the overflow and carry. The carry flag is set only when an arithmetic operation results in a carry; the overflow flag only when an arithmetic operation produces a true arithmetic overflow. For example, +5 minus +3 in two's-complement math produces a carry-out of the high-order bits. However, the +2 result is still within the number range of the processor, so the overflow flag is not set.

If −100 were added to −64, though, you would not only get the carry-out, but an overflow indication as well, since the result is a positive 8-bit number even though the result should be negative. (An 8-bit word has a negative number range of −127.)

Addressing techniques move data

To get data or instructions into and out of the processor, the information held in memory must be addressed and then pulled into the processor, or vice-versa. The three most popular techniques used to address the memory include direct, indirect and immediate addressing.

Direct addressing includes the address of the relevant data within the instruction. However, this mode has severe limitations for the programmer since every time a data address is used, it must be included in the instruction. For example, if you need to find the average of four numbers stored at addresses ABCA, ABCB, ABCC and $ABCD_H$, then the program using direct addressing would be as shown in Fig. 7. This program leaves the result in the accumulator.

You already know that a program can be simplified by having the index register act as a pointer to the memory locations. This type of memory addressing is called indirect. In its most general form, the pointer register can be an internal processor register or any memory location. Thus, for the averaging in Fig. 7, memory location ABCE could serve as the pointer if you used an indirect add instruction (the @ indicates indirect mode). If, when the program starts, location ABCE contains the address for ABCA, the program will look like the one in Fig. 8.

This revised program uses more memory space than if it used direct addressing. However, for long lists of numbers to be added, the indirect addressing technique combined with an increment and compare loop would drastically shorten the number of instructions needed. But there is a penalty: the instruction cycle for an indirect-addressing command is longer than for a direct-addressing instruction.

The third address mode is immediate addressing. The operand is included in the instruction itself. A typical instruction would be "Add the constant ABCE to the AC," and its mnemonic could be ADD # ABCE. The # symbol denotes immediate addressing. This addressing method is useful when known constants must be included in a program.

You can make these three basic memory-address instructions more powerful. Auto-incrementing, auto-decrementing and indexed addressing are refinements that advanced processors have to shorten programs and make more efficient use of both the programmer's time and available memory space.

Combined commands simplify programming

The program shown in Fig. 8 using indirect addressing can be considerably shortened if the processor has an add and increment instruction. Just five instructions would be needed to perform the four-number addition.

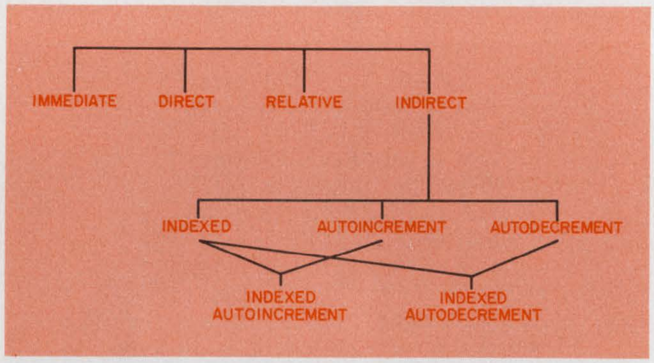
Another refinement, particularly useful in complex programs, is indexed addressing. Here, the correct data address is calculated by adding an offset value to a specified address. Usually, the offset is stored in the index register and the specific address can be obtained by direct or indirect addressing.

For example, if the IR contains 0005 and the instruction "Add [0A00] indexed" is used, the correct data address is obtained by adding the contents of the IR to 0A00 to give the correct address, 0A05. Some processors even have an indexed auto-increment indirect-addressing mode, where the correct address is obtained by adding the IR to the indirectly specified address, and then the IR is automatically incremented. Some processors can manipulate the indirect address rather than the IR.

Another popular form of addressing used by some processors is relative addressing. This mode is similar to indexed addressing since the correct address is calculated by adding an offset to some base address. The instruction usually contains the offset and the PC has the base value. Relative addressing is usually used for jump and branch type commands since the final location depends on the value in the PC.

To make microprocessor-based systems more memory-efficient, vendors are trying to reduce the number of bytes needed for each instruction. Usually, this requires that the addressing capability of the memory-reference instructions be reduced while retaining the essential characteristics of the conventional instruction. Reducing the number of instruction bytes reduces cycle time, which speeds up the overall program.

The three-byte indirect addressing technique described can use any memory location as a pointer to the appropriate data address. However, this complete flexibility is not usually required, and in most cases only one or two address pointers are really needed. Thus, you can reduce the three-byte instruction to a single byte where the actual address pointer is specified within the instruction op code. In many processors, the index register can be used for this purpose, and some microprocessors have several other internal registers that can be used similarly.



9. **Various addressing techniques are available to the knowledgeable programmer.** However, not all processors have all possible programming modes. In fact, most processors offer only a small percentage of available addressing modes.

Speed addressing by paging

Although register addressing is better than indirect addressing, it's slower than direct addressing, which can be accelerated even more. With paging, the high-order address byte can be stored within the processor while only the low-order address byte is specified by the direct-addressing instruction. This approach works when most of the addresses that a processor must access are located near each other and, therefore, have the same high-order address byte.

For efficient paging, one extra register in the processor must be available to hold the page address, and the processor should have some special instructions to manipulate the register contents, such as an increment or decrement command. The programmer, though, must take care that page boundaries aren't crossed.

An alternative to the extra register is to restrict direct addressing to a single page, say page 0, so that when a direct-addressing instruction is received by the processor, it knows all the high-order bits are zeros.

Some processors contain multiple on-chip registers than can be used for many operations to quicken program execution. Most on-chip registers are designed so that just a single-byte instruction can access them. These registers can be used by the programmer for either data storage or address pointers.

Usually, however, a microprocessor does not have all the addressing modes described, and when you evaluate various units, one worthwhile check is to check how many bytes of program are required to perform all the classic memory-reference instructions.

For instance, some processors don't come with direct addressing. So you'll have to build such an instruction: Load the index register with the required address (three bytes) and then add the contents of the address specified by the index register to the AC (one byte). Do the same for other types of addressing-mode commands. All the modes are summarized in Fig. 9.

Divert programs by jumps and branches

Just as for memory-reference instructions, jump instructions should be kept short to minimize program-execution time. Paging and indirect-register-addressing techniques can be used with jump instructions to speed program flow. Several forms of paging can be used, but with the simplest form, the high-order address byte doesn't change and only the low-order byte is loaded for the jump. This method is restricted to jumps within the current page, but in many cases that's enough.

Another approach is to add a number to the program counter, a number that can be specified either in the jump instruction (immediate addressing) or in a register. Do this, and you can reduce a three-byte instruction to two bytes. Conditional jump commands enable the program to make decisions based on the status of certain flags. An example of this is "Jump to specified address if AC is zero (check the zero flag), otherwise continue with the normal program flow."

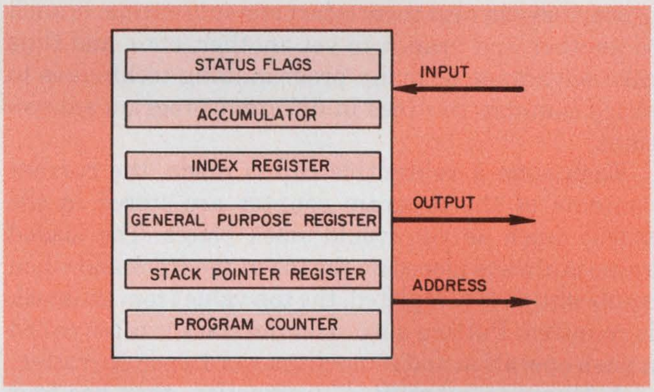
Using this instruction in an example, take up the four-number averaging problem again. The program must find the average of four numbers stored in locations ABCA, ABCB, ABCC, and ABCD. Assuming the processor has the internal-register architecture shown in Fig. 10, use the general-purpose register for counting how many times the program executes the add instruction.

The averaging program can then be structured as outlined in Fig. 11a. The conditional jump instruction, "If GPR does not equal zero, jump back to add instruction," enables the program to make an elementary decision on whether to go around the loop once more or do the averaging. The final program pattern, as set up for the memory, is shown in Fig. 11b. Here, the jump instruction specifies that the loop will return to address 0007_H each time the GPR is tested and isn't zero.

If your processor doesn't have the general-purpose register, the results of the addition and the contents of the loop counter will have to be exchanged continually to perform the necessary updates and checks. The address to which the program jumps does not have to be explicit in the program, though. You can use direct and indirect addressing to specify the value that must be loaded into the PC.

In some processors, the PC, IR, GPR, and AC all become general-purpose registers for some operations. Therefore, an instruction such as "Load immediate ABCD to register A" may produce quite different results depending on how you use register A.

One instruction that can perform a conditional jump with only a single instruction byte is a skip command, which translates into "If condition XYZ is satisfied



10. **Processors more advanced** than the version modeled in Fig. 2 offer many more registers to the programmer to permit subroutine nesting, on-chip variable or data storage, and special pointers for fast memory access.

then skip the next n instructions." However, this instruction assumes you know how many instructions are in between it and the next command—which you may not know during program development.

Two very specialized jump instructions, "Jump to subroutine" and "Return from subroutine," are used in much the same way as the unconditional jump commands, except that when the jump takes place, the original contents of the PC aren't lost but stored temporarily in a special location often referred to as a "stack." There, they can be recovered by a return instruction. Subroutine jumps can be conditional or unconditional operations, depending on what the processor can do.

Reduce repetition with subroutines

Sometimes a specific operation must be repeated many times, much like the addition process in Fig. 7. Writing the same program each time it is needed

Table 5. 8-bit DAA algorithm

Carry flag before DAA	Upper half-byte	Half carry before DAA	Lower half-byte	Number added to AC	Carry flag after DAA
0	0 to 9	0	0 to 9	00	0
0	0 to 8	0	A to F	06	0
0	0 to 9	1	0 to 3	06	0
0	A to F	0	0 to 9	60	1
0	9 to F	0	A to F	66	1
0	A to F	1	0 to 3	66	1
1	0 to 2	0	0 to 9	60	1
1	0 to 2	0	A to F	66	1
1	0 to 3	1	0 to 3	66	1

would be a great waste of space, especially if the program is complex. The answer is subroutines. Some processors can nest them (start one subroutine, branch to another and branch to yet another, etc.), and thus take advantage of many programming techniques to share common routines in different program subsections.

Each time a subroutine call is made, the current contents of the program counter are stored in the stack, much as you would stack plates. The loaded value is always placed on the top of the stack and when a subroutine is completed, the top value from the stack is removed. Putting a word on the stack is often called a push operation and removing a word a pop operation.

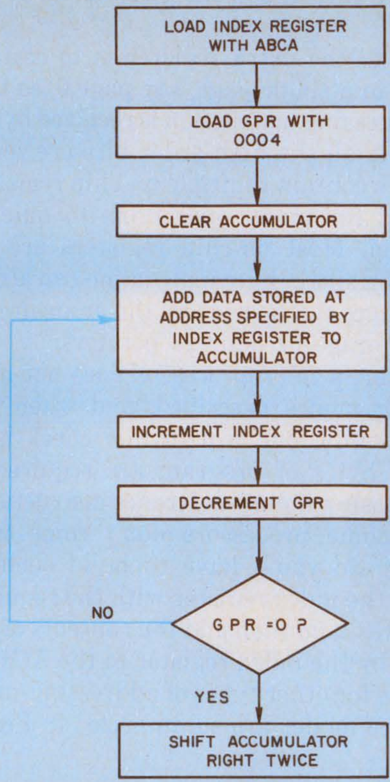
A "Jump to subroutine" instruction, then has four parts:

1. Send out the contents of the PC and fetch instruction.
2. Increment PC.
3. Store contents of PC in stack.
4. Load PC with address of subroutine specified in instruction.

Stacks can be implemented two ways: with a shift register, where a push corresponds to a shift in one direction and a pop refers to a shift in the other, or with a RAM and a stack-pointer register. The register is a special register or memory location put aside specifically for keeping track of the next memory location available for the stack.

The shift-register approach is chiefly used where the stack is part of the processor chip, and although faster than an off-chip register, it is restricted by the number of possible stages (addresses) it can hold. With the stack pointer approach, the stack can grow to any size needed since external memory is used and more can be added as necessary.

Push and pop instructions are quite powerful in their own right, particularly if they can operate on registers other than the program counter. In many cases, in fact, when the processor jumps to a sub-



(a)

Instruction No.	Program memory contents	Program memory address (hex.)
	Load IR immediate	0000
1	A B	0001
	C A	0002
	Load GPR immediate	0003
2	0 0	0004
	0 4	0005
3	Clear accumulator	0006
4	Add @ IR	0007
5	Increment IR	0008
6	Decrement GPR	0009
	If GPR ≠ 0 Jump	000A
7	0 0	000B
	0 7	000C
8	Shift right	000D
9	Shift right	000E

(b)

11. **Performing the multiple-number averaging using subroutines,** this flow chart (a) shows how the processor monitors the value of the general-purpose register. Nine instructions are needed to perform the averaging as well as 15 memory locations (b).

routine, not only should the contents of the PC be stored, but also the contents of other internal registers. This is very important if the processor is interrupted from its normal operation by something like a power problem or an interrupt signal from another piece of equipment.

Besides stack architectures, multiple PCs and register banks can also be used in subroutine calls. Some processors have enough internal registers so that two or even three sets of registers can be switched back and forth for subroutine handling.■■

This article was adapted, with the permission of the publisher, from the "Microprocessor Systems Handbook," a recently published book from Analog Devices, Norwood, MA.

Multiprocessing adds muscle to μPs.

Linking several small processors often gives you more computing power than one heavyweight working alone.

Organize microprocessors into a multiprocessing system and you'll enjoy three advantages that one big processor can't duplicate:

- System throughput can be increased.
- Processor tasks can be segmented thanks to simplified hardware and software.
- Your system can be expanded for more flexibility simply by adding modules.

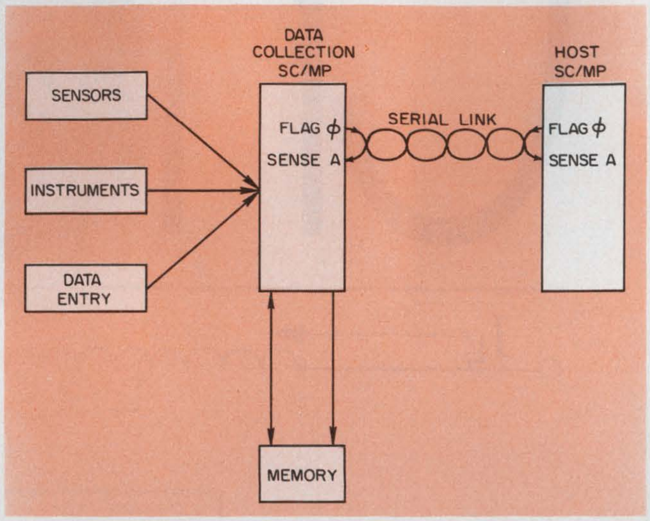
Not only do multiprocessing architectures increase your computing power, they allow communications between processors as well. And in many cases, multiprocessing gives you a system solution that's faster and cheaper than using a single processor. Here are some typical applications for putting several interconnected processors to work:

1. Remote, microprocessor-controlled data terminals linked to a central or host processor.
2. Situations where a single processor offers too little computing power, but a more powerful unit offers too much.
3. Multiple, related tasks that cannot be handled efficiently by one processor.

But don't jump into multiprocessing without first understanding the architectures you can use and the options you get with each one. Of the three basic architectures, "serial-link" applies when the volume of system data is small, while "common-bus" and "private-bus" handle more information, as well as allowing interprocessor communication.

Serial links are long links

To pass a limited amount of information between two processors located a considerable distance apart, form the communications link with serial-link architecture. A remote data-collection system using SC/MP processors (Fig. 1) exemplifies this architecture. The remote processor collects, stores and analyzes data from its input devices, and later transmits the information to the host. Both the remote and host units are self-contained systems, with their own RAMs, program ROMs, and I/O units. And they operate independently of one another, passing data or control signals over the link.



1. **Serial-link architecture** allows long-distance communications between processors. The host can receive data over the link from a number of data-collection units, but only one unit communicates at a time.

If more than one remote unit is used, and a remote, not the host, fails, the system can be kept operating. On the other hand, any processor failure in a serial link cannot be corrected or overcome by the other units. For this reason, don't use this architecture in a system whose operation is critical and must be maintained at all times.

Serial-link is not limited to hardwired operation between processors; a modem hookup or even a radio link is possible. An example of a weather-recording system is shown in Fig. 2. Here, μP-1 collects data on rainfall, wind speed, temperature and time of day. It also analyzes and compacts the data.

At a predetermined time, the information is passed to the host processor via the modem. The host can collect and analyze data from several remote processors. But μP-1 and all remotes are responsible for their own instrument control, data analysis and storage, and communication with the host processor.

Where serial-link is essentially a system of self-contained units operating one-to-one—with one remote talking to the host at one time—common-bus architecture lets processors talk to each other on shared lines, use a common system memory, and

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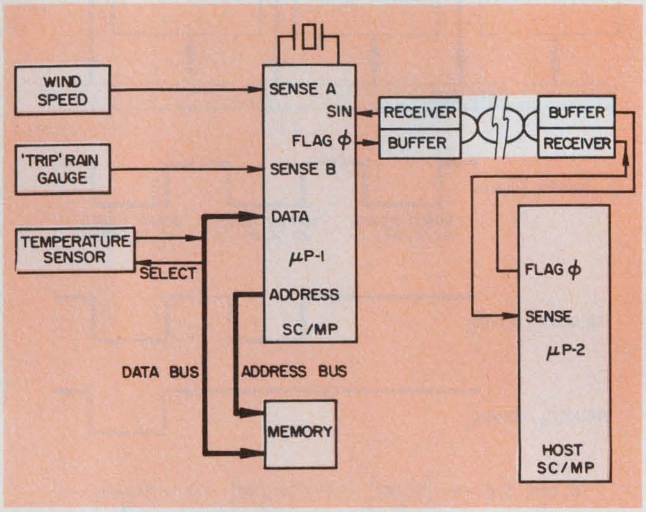
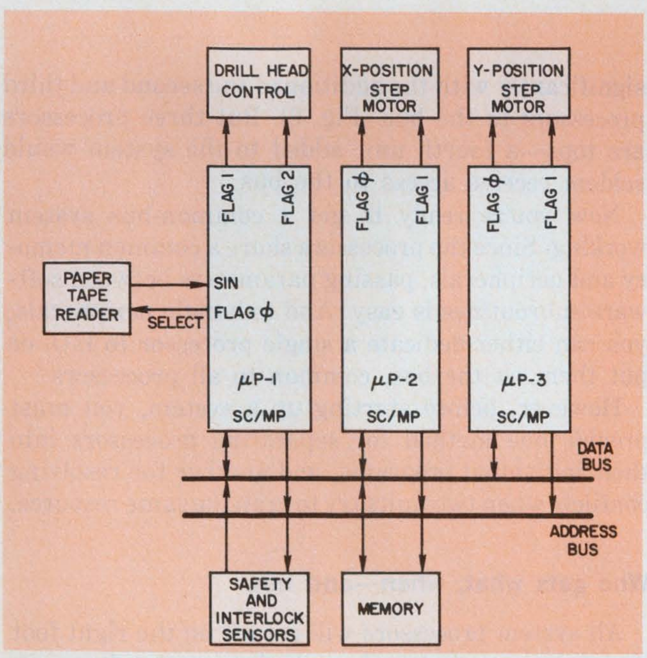


2. **A weather station illustrates serial-link architecture** in operation. Processors don't have to be hardwired; a modem or radio link can pass data and commands between host and remote units.



3. **Common-bus architecture can handle distinct but interrelated tasks,** as shown by this drill-press controller. Information and safety checks passed between the three processors are coordinated to move the drill head and the work in the proper manner.

process a larger volume of information. This scheme takes advantage of the fact that several processors can share a single memory and system buses because one processor needs the bus for only a fraction of the instruction-execution time.

Common bus—where one μP won't do

When a single microprocessor doesn't have the computing power you need, or when several distinct but interrelated tasks must be performed simultaneously, common-bus architecture is the answer. Since the bus is available to other units during unused portions of execution time, system throughput improves.

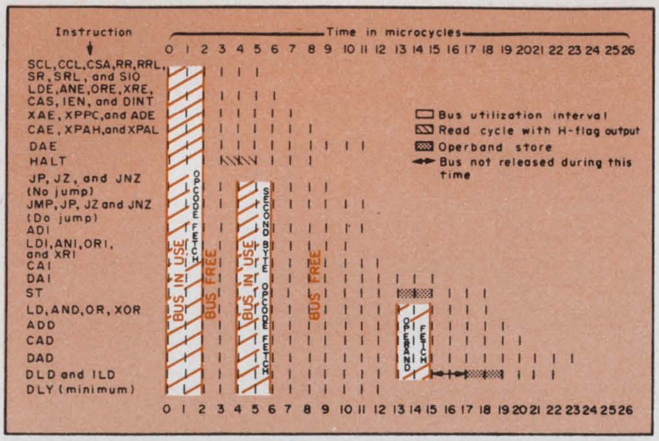
Common-bus architecture fits the bill when your application can be partitioned among the microprocessors. You can allow one processor to perform only keyboard, display and I/O functions, while a second unit collects and interprets data. Moreover, your software development is simplified because you can write partitioned subprograms, each to be run on a separate processor. Subprograms can be made fairly independent of one another, so they can be debugged and tested separately.

Common-bus does have two drawbacks: Interprocessor interference limits the number of units that can be connected together, and the processors themselves must be physically close to each other.

To see how common-bus architecture allows tasks to be partitioned, look at the numerically-controlled drill press system in Fig. 3. This multiprocessed system allows the X and Y position functions to be performed simultaneously, and without additional expensive hardware. It's also an example of how three relatively low-cost microprocessors can replace one expensive minicomputer.

The system tasks, though closely related, cannot be carried out by a single processor. The three SC/MP processors are required to read the control paper tape, control the X and Y position motors, raise and lower the drill head and make safety checks. μP-1 controls the paper tape reader and receives X and Y position information from it. Absolute-position data are then transferred to μP-2 (X position) and μP-3 (Y position).

Now μP-2 and 3 must compute a relative-position-change number and move the stepping motors accordingly. After the motors are correctly positioned, μP-1



4. **A bus-utilization schedule** shows that portion of total execution time that a processor needs the bus. SC/MPs release the bus when they aren't using it, so other units can execute their instructions.

receives signals from the other two microprocessors to lower the drill head. μP-1 first performs some safety checks, then lowers and raises the head. The entire cycle is then repeated.

For a multiple processor system to increase throughput rates, you need to allocate the system bus efficiently. Not only must the bus-allocation scheme be automatic, but the decision time to grant access to any processor must be minimized.

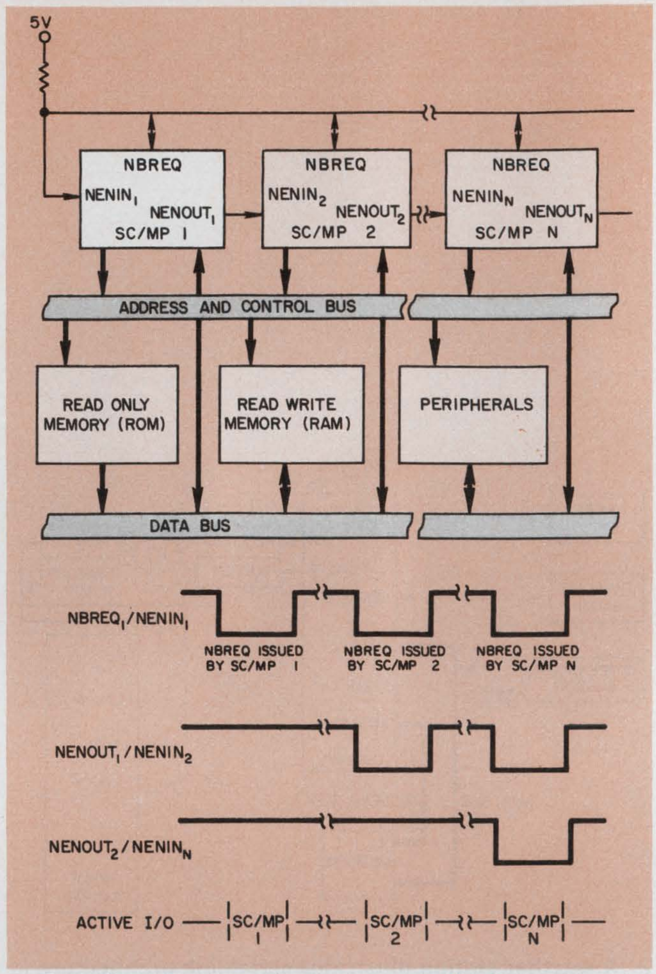
μPs don't waste much time

Since a common-bus microprocessor needs access to the system bus for only short periods of the instruction-execution time, it can spend the remaining time in its own internal timing states. During these states the bus can be allocated to another microprocessor, which then fetches its op codes or memory data-reference instructions.

In Fig. 4, a bus-utilization schedule shows how much time must be allocated to a SC/MP. Note that it uses the bus for 2-μs intervals, then releases it for another μP to execute its own instructions.

Bus allocation for SC/MPs is done automatically, on chip. Signal lines NBREQ, NENIN and NENOUT in Fig. 5 select which processor can have access to the bus at any time. If a processor's NBREQ and NENIN inputs are both high, it can take the bus. It then forces NBREQ and NENOUT to go low to prevent another unit from taking the bus before access is finished. In the figure, unit-1 has the highest priority and unit-N the lowest.

But the total number of units that can be connected to the bus is limited by something called the bus-utilization factor—the average ratio of a processor's required bus-access time to total instruction-execution time. For an SC/MP common-bus scheme, the factor is 1/3 meaning that the maximum number of units that can be connected is three, and each needs the bus a third of the time. System throughput improves



5. **Bus allocation is performed automatically** by SC/MPs. Signals NBREQ, NENIN and NENOUT select which unit has access at any time. SC/MP-1 has the highest priority and SC/MP-N the lowest.

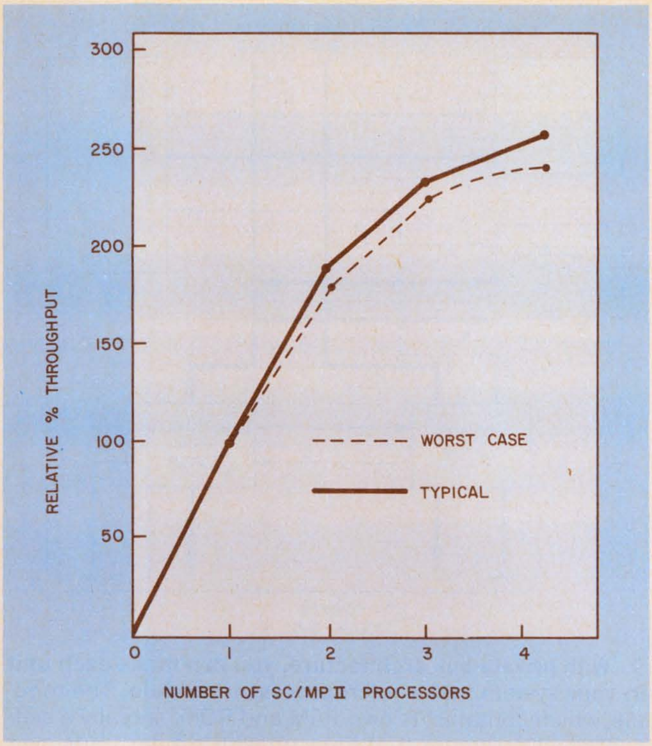
significantly with the addition of the second and third processors to the bus (Fig. 6). But three processors are tops—a fourth unit added to the system would seldom receive access to the bus.

Now you're ready to get a common-bus system working. Since the processors share a common memory and peripherals, passing parameters between software subroutines is easy. And to handle peripherals, you can either dedicate a single processor to I/O, or put them on the bus, common to all processors.

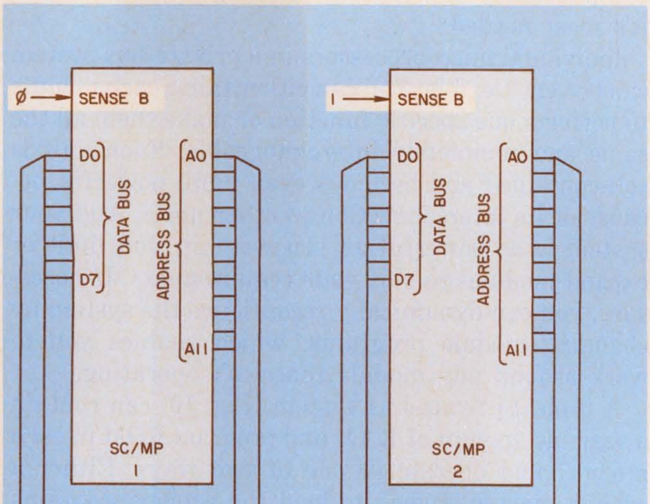
However, before starting up a system, you must provide one method for separating processors into their individual programs, and another for resolving conflicts when two units try to grab the same resource.

Who gets what, when—and how

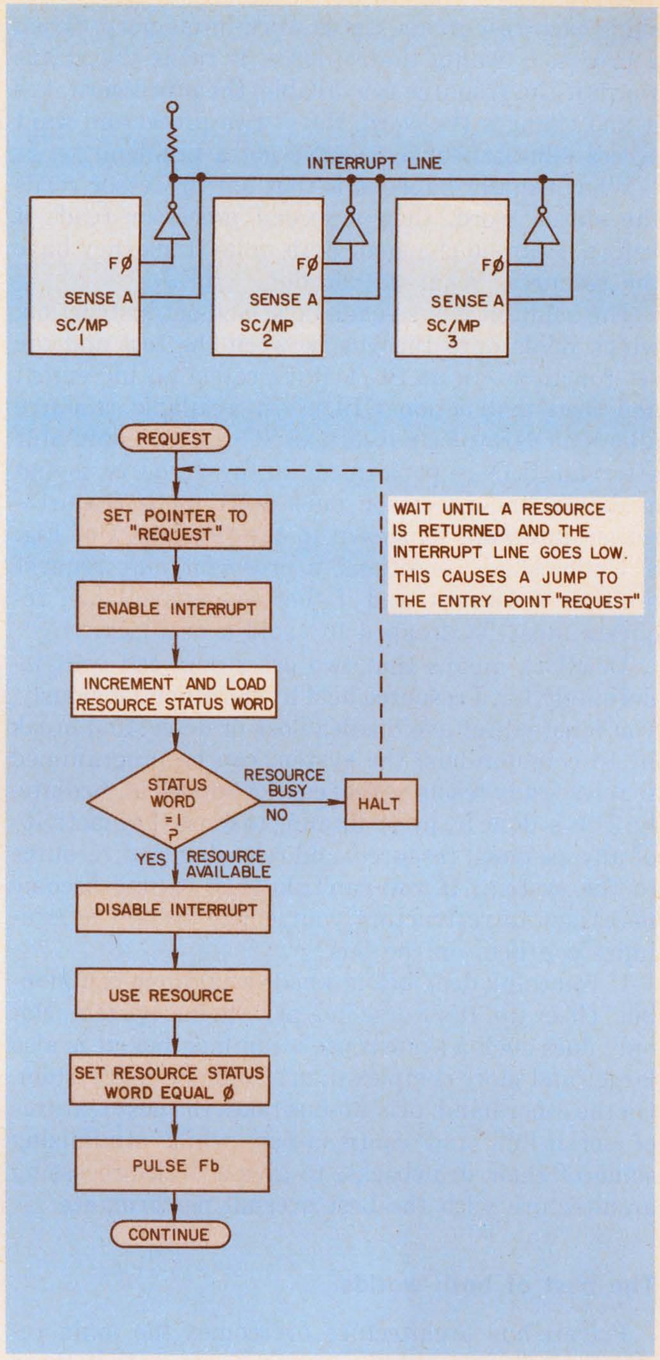
All system processors will get off on the right foot if each knows what to do and where to go after your system is reset. Use a start-up scheme like the one in Fig. 7 with SC/MPs. A unique code is hardwired into the sense inputs of each unit. Immediately after reset, at program location 0001, which is common to



6. **System throughput increases** when three processors share a common bus. But adding a fourth unit doesn't do any good; it will seldom receive access to the bus.



7. **Common-bus microprocessors must be separated** into their proper starting routines after the system is reset. For SC/MPs, a unique code on the sense inputs gets each unit into its own program.



8. **It's important to allocate system resources properly,** if you want to avoid deadlocks. This flow chart shows how SC/MPs use an ILD instruction to determine if a system resource is available to a processor.

all units, each processor gets instructions to read its own code. And the code contains information to allow a processor to jump to its correct starting address.

Now you're underway, but before long a conflict may arise when more than one processor wants access to a system resource. It would be nice to use a separate bus-allocation processor, but that's a luxury you can't afford because of the limitations imposed by the bus-utilization factor. Since you can't use more than three units, resource allocation must be handled by individual processors.

The most straightforward allocation technique assigns each resource a status word in memory. When a processor wants the resource, it reads the status word; if the resource is available, the processor takes it and changes the word. But if two processors want access simultaneously, you've got a problem.

What usually happens is that one processor reads the status word, then a second processor reads it before it can be changed. Both units think they have the resource. What do you do?

The solution is a so-called test-and-set instruction, which holds onto the bus between the test and the set functions. In an SC/MP it's called an increment and load instruction (ILD). An available resource allows a ONE to be put into an SC/MP's accumulator after an ILD is performed. If the resource is not available, the processor must wait for a resource-return interrupt as shown in the flow chart of Fig. 8. Under some conditions, a processor may request multiple resources, and if they are unavailable, requests must be dropped to avoid a deadlock.

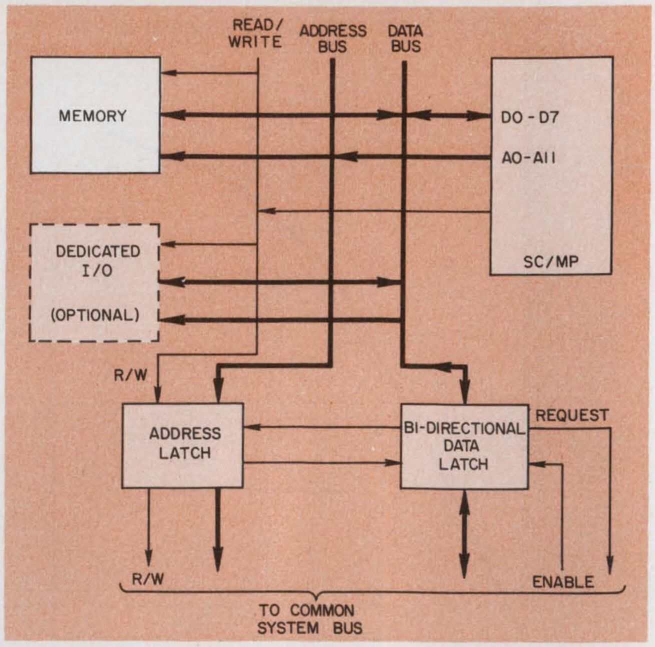
Deadlock means that two processors can wait indefinitely for a resource held by the other. Obviously, you must either avoid a deadlock or detect and break it. In common-bus, the system can be programmed to release any resource that cannot be used immediately. This is done by programming to sense the inactivity of any assigned resource, and releasing that resource to the system. If you can't do this, it may become necessary to restructure your entire system to minimize conflicts on the bus.

If you think deadlock is a bad situation in common-bus, cheer up. It's worse in a private-bus system. Not only does such a system use a common bus, it is also larger and more complex than a common-bus system. On the other hand, private-bus takes the best features of serial-link and common-bus, while minimizing some of their drawbacks, to give a multiprocessing architecture with the best over-all performance.

The best of both worlds

Private-bus architecture overcomes the main restriction of common-bus systems—no more than three microprocessors at a time. Each private-bus processor (Fig. 9) contains its own local RAM and program ROM—like serial-link. But it also has access to the system memory and I/O devices—like common-bus. In fact, the processor, RAM, ROM and system-bus link can be packaged together into a single microprocessor module. And with this modular concept you have the flexibility to expand and maintain your system easily.

With private-bus architecture each processor can access its own local memory at full speed, without being limited by the other units. And since you avoid the common-bus problem of interprocessor interference, you can hook up more than three SC/MP processors at a time. System throughput naturally increases but, even better, it increases directly with the number of processor modules in your system. And the hardware and software overhead associated with



9. **With private-bus architecture, you can make each unit in your system into a microprocessor module.** The module, which contains its own RAM and ROM, is really a self-contained computer that links up with similar units over a common-bus system.

increased throughput is minimal. What's more, you can physically distribute processing power to where it's most needed.

Individual microprocessors in a private-bus system can be very flexible: You can either tailor each module to perform one specific function or make them all the same and completely interchangeable. Each unit is self-contained and becomes even more powerful because of its interconnection to other units. And your system is as powerful as you want it; you limit or expand modules to suit your requirements. If necessary, you can dynamically reconfigure the system by changing module programs, which enables you to work around any module that isn't operating.

A typical private-bus system (Fig. 10) can contain a variable amount of RAM and program ROM in each module, and operate in one of two ways. Either a system master is used to load the proper programs into the module RAM, or the operating programs are stored in the module ROMs. All modules can be placed in a single package or distributed to where processing power is needed. An application for this type of system is a production line where each module is responsible for a different task.

The system bus provides for high-speed communication between modules, and the system master monitors conditions and issues instruction changes as required. Another job for the master is to perform diagnostics on modules and report malfunctions and their causes to a human operator. If your operation requires high reliability, put in redundant processor modules to take over in case a primary module fails.

Because the computing demands placed on a private-bus system are much more complex than those in common-bus, allocating system resources can't be left to the processors themselves. You need an independent unit to resolve conflicts on how memory, I/O and communications channels are to be shared.

Here comes the judge

The unit that passes judgement on which processor gets what resources in private-bus architecture is called the system-bus arbiter. Among other things, it must handle multiple-resource requests, independent requests and returns. And most importantly, it must detect and prevent deadlocks.

The arbiter can be a microprocessor, or it can be specialized hardware, depending on your system tasks. A microprocessor arbiter probably does a better job since you can tailor it to your system to ensure maximum throughput and avoid deadlock. A hardware arbiter is used mainly for granting high-speed, single-byte access to the common memory. Of course, in a large multiprocessing system, you may need both hardwired and microprocessor types.

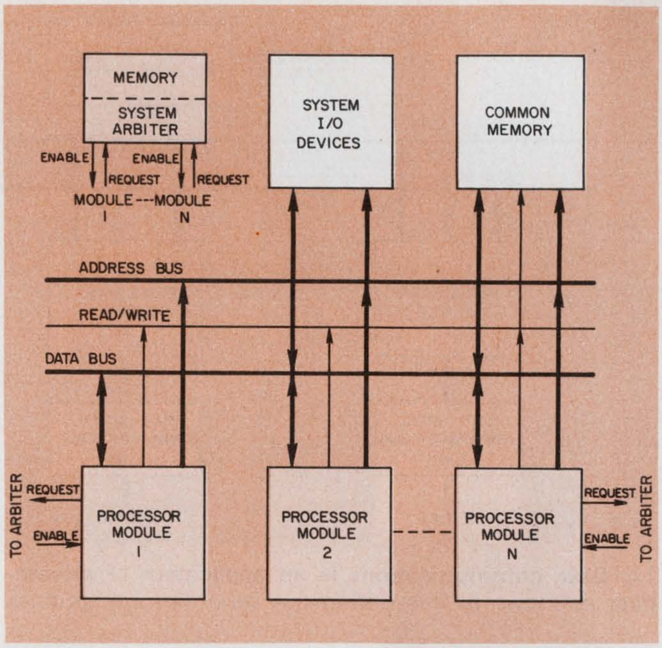
The easiest allocation scheme that a microprocessor arbiter can perform is to match requests with available resources on a pseudorandom basis. In other words, any resource is assigned to the first request encountered in a linear search of the request list. More difficult schemes include round-robin or first-in-first-out queuing. But a system arbiter can be designed to allocate resources based on priorities you assign to resource requests.

Both types of arbiters must allocate resources fairly. When a block of common memory is accessed, the hardware arbiter must grant one request while holding all others for execution in a speedy and automatic way. The hardware arbiter can sometimes be adapted from a priority-interrupt control unit. Or it can be custom-designed to fit your application.

Sometimes both types of arbiter are needed in one system. A good example of this dual arbiter is found in a data-communications network made of four intelligent data receiver-transmitter processors (Fig. 11). Each processor communicates both with a high-speed serial data link and with others over the system bus. But for this network to operate at high speeds, the system arbiter incorporates both a microprocessor and a hardwired unit.

As a processor receives and verifies a message, the starting and ending address of that message in central memory is passed to the destination processor. This processor then encodes and retransmits the message to the next higher point in the communications network. A supervisory processor maintains network information and data-link assignments based on equipment conditions, message load and the most direct route to the final destination.

Because the receiver-transmitter modules are intelligent terminals, protocols can be handled by the processors themselves, without typing up the entire



10. **Several processors can be connected to the bus** in a private-bus scheme. Individual processors are independent of each other, yet have access to memory and system I/O devices.

system. And the units can be expanded to accommodate any future needs.

Although private-bus is the most powerful individual configuration of the three multiprocessing architectures, many system problems are so complex that you may have to combine the features of two or more schemes to find a solution. And with multiprocessing you can do just that.

One system, three architectures

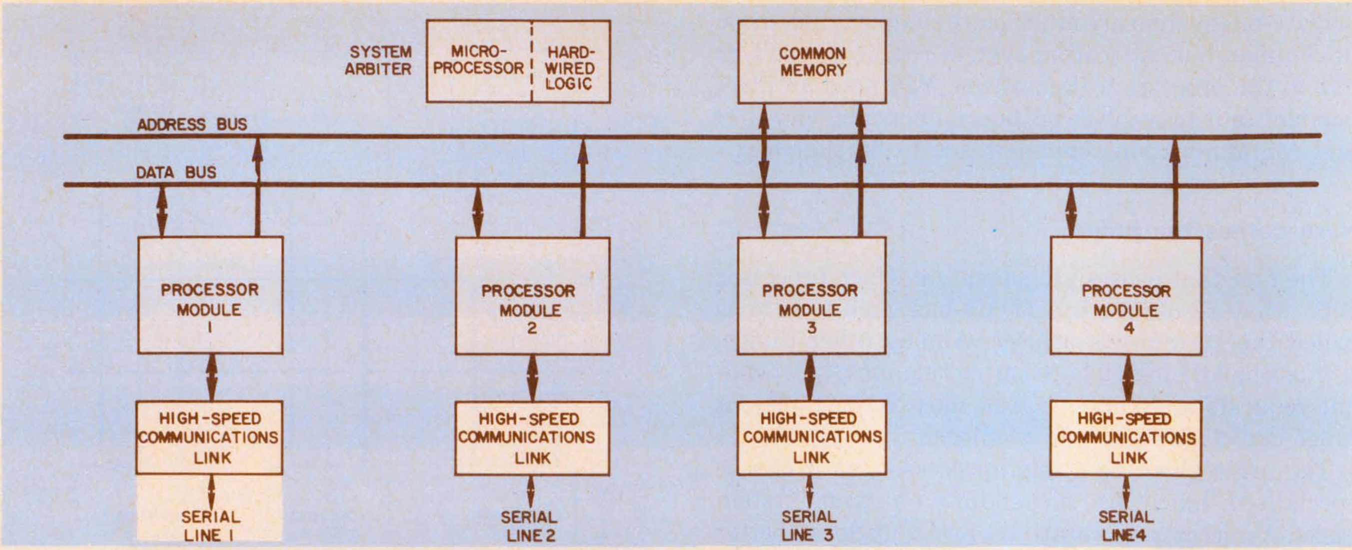
All three architectures are used to improve the response time, data-handling capability and reliability of the security system in Fig. 12. Each remote station consists of two SC/MPs on a common bus, connected via a serial link to a communications SC/MP at the host processor. Communications units are interconnected by a private bus within the host system.

In each remote unit, the μP-1 supports the keyboard and display, and keeps time, while the μP-2 takes care of communications, the badge reader and control latches.

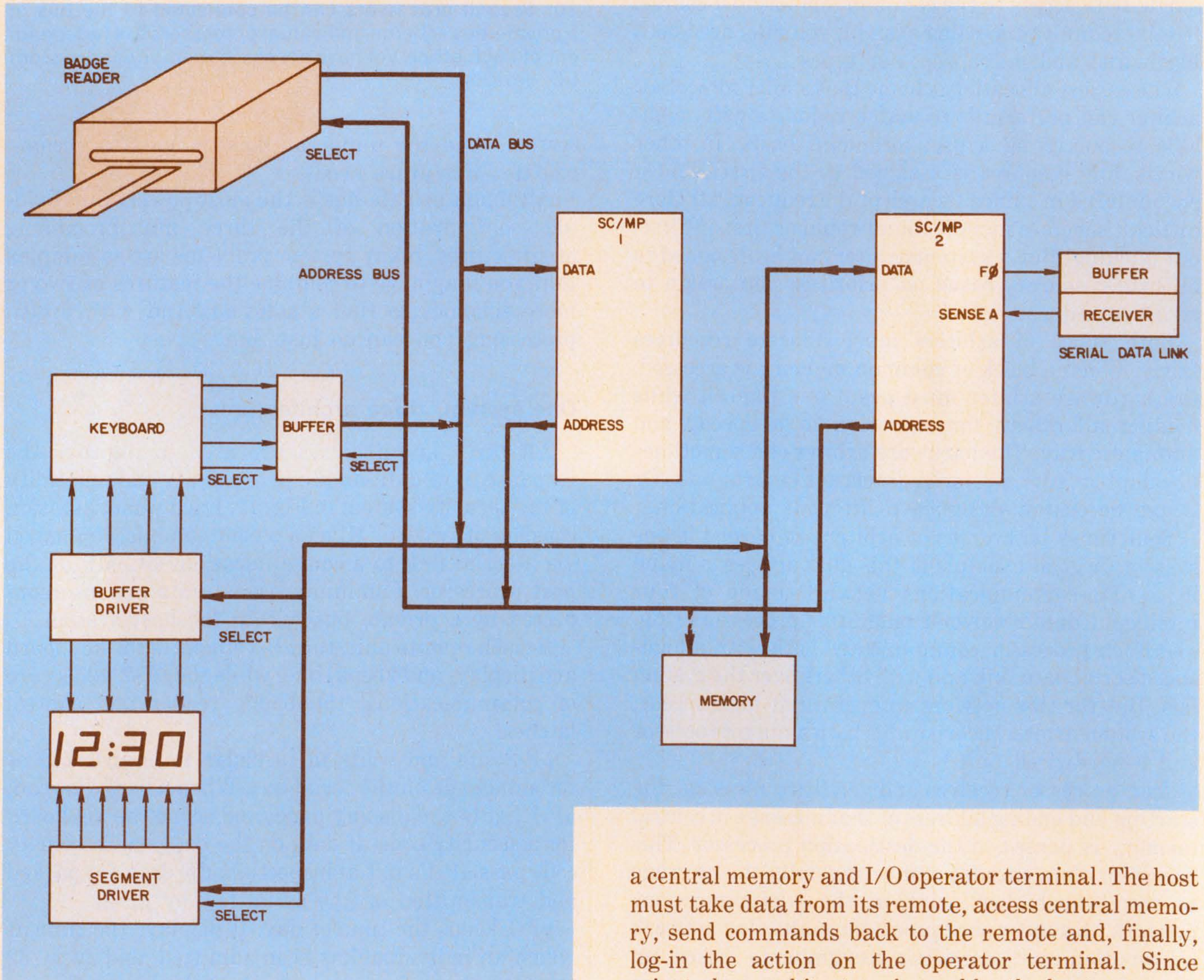
μP-2 sits and waits for a badge to be inserted or for a message on the serial bus. When a badge is read, μP-1 lights the display panel and scans the keyboard for a security code. If data on the badge and security code pass μP-1's initial inspection, the data are packed and transmitted on the serial bus by μP-2.

μP-1 keeps the time of day. It displays the time at which an individual has been admitted, and every 30 minutes thereafter, as a check with the host.

A large security system can have a number of remote stations, with each reporting to the central controller via its own serial bus. The controller uses one host processor for every remote, and also contains



11. **Data communications is an application of private-bus,** as shown in this network. A serial link brings data into each processor, but processors communicate with each other on a common bus.



12. **Multiprocessing lets you combine three different architectures** in one application as in this remote security station. Common-bus is used within the station, which is connected to a central processor via a serial link. A central processor uses private-bus architecture.

a central memory and I/O operator terminal. The host must take data from its remote, access central memory, send commands back to the remote and, finally, log-in the action on the operator terminal. Since private-bus architecture is used by the hosts, you can increase or decrease the number of remotes easily, and work around a failed host. A hardware arbiter is used to give the processors high-speed access to a common memory and the operator terminal. ■■

Stop display jitter with software.

Improve the machine-to-human interface in analog-input μP systems with a little software and no extra hardware.

Imagine a supermarket customer watching the display digits on an analog-to-digital-based electronic scale bouncing around as his purchases are weighed and priced. As an engineer, you wouldn't be bothered by an instrument having display jitter in its least-significant digit. But it's enough to make a customer doubt the scale's accuracy.

The solution? Stop display jitter with software—and without extra hardware. A/d-based electronic weighing systems usually include a microprocessor for handling arithmetic computations and control. With the processor, you can usually add more software. Fortunately, jitter elimination requires very little software compared to the total ROM/RAM program of your system.

Weigh it for yourself

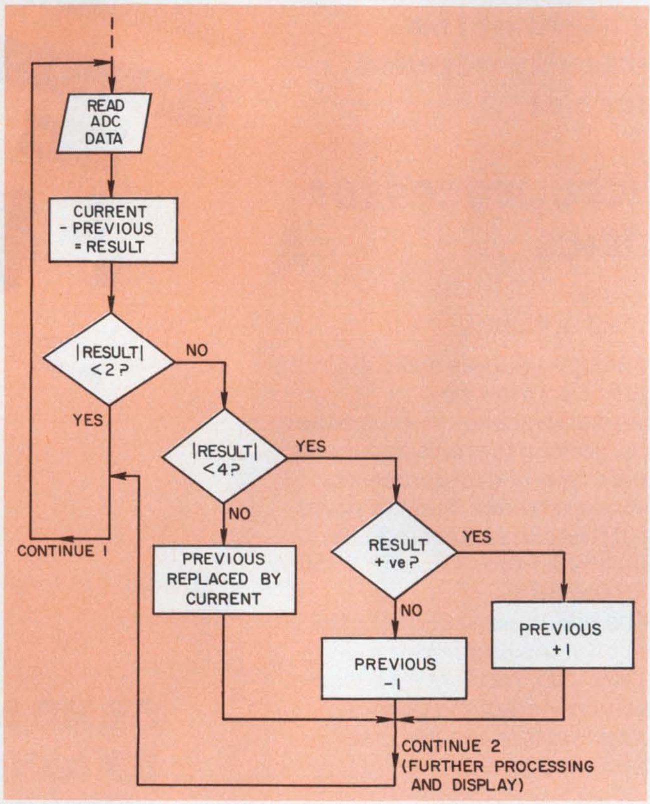
Just as hysteresis in the form of a Schmitt-trigger is used in analog circuits to clean up noisy signals, it can be used in the digital form of processor software to stop display jitter.

The scheme is very simple. An 8080A microprocessor compares the present output of an a/d converter (a Siliconix LD 120/121) with a previously stored value. If the difference between the two values exceeds a preassigned amount, a new value is computed to replace the one previously stored. Eventually, the displayed value for a particular input settles within a band bounded by the upper and lower limits of the a/d converter's output.

A flow chart for the jitter-elimination routine is shown in Fig. 1. The scale's display is controlled by a small RAM, which is updated only under the condition CONTINUE 2 in the flow chart. Fig. 2 gives you the complete jitter-elimination program for an 8080A, while memory assignments for the routine are shown in the ROM table (Fig. 3).

Note that the data originate as five BCD digits stored in three bytes of RAM. The least-significant digit is stored in CRNT, the most significant in CRNT + 2. Bytes representing BCD-digit pairs have their less significant digits in bits 0 through 3, their more significant ones in bits 4 through 7.

Gregory Yuen, Design Engineer, General Instrument Microelectronics, Ltd., Newark Road North, Glenrothes, Fife, KY7 4NL Scotland.



1. **Display jitter is eliminated** when this flow chart is converted into an 8080A microprocessor program. The display is controlled by a small RAM, which is updated only on condition CONTINUE 2.

Now, how does the program affect the electronic scale's operation? The a/d converter has a resolution of one part in 19999 (LSD/full scale), but the weighing function requires only one part in 1279, or 1/8 oz in 9 lb, 15 7/8 oz. The extra resolution is used to satisfy accuracy-related legal regulations and to provide auto-balancing and other functions. Further, jitter of ±1 count can be expected from the converter in its most sensitive full-scale range, which is 200 mV.

Down at the supermarket, the food goes on the scale, the display is solid as a rock, but...

What the customer doesn't see...

...is that the a/d converter starts with an output of 03679 in period 1, while the scale's display shows 03680 (see period 1, Fig. 4). This value stays on the

Line	Label	Code	Operand	Comment
1		LXI	D,RSLT	;D and E address result
2		LXI	H,CRNT	;H and L address current data
3		MVI	C,03H	;Set number of bytes to be moved=3
4	LOOP1:	MOV	A,M	;Move byte in memory to accumulator
5		XCHG		;Switch D and E with H and L
6		MOV	M,A	;Store in memory
7		DCR	C	;Done if C=0
8		JZ	DIFF	
9		XCHG		;Reswitch D and E with H and L
10		INX	D	;Address next result byte
11		INX	H	;Address next current data byte
12		JMP	LOOP1	
13	DIFF:	LXI	D,RSLT	;D and E address result
14		LXI	H,PRVS	;H and L address previous ADC data
15		LXI	SP,PTR	;Pointer for return address from subroutine
16		MVI	C,03H	;Set number of bytes for subtraction
17		CALL	DSUB	;Call decimal subtract subroutine
18		JC	IDPOS	
19		LXI	H,RSLT	;H and L address result
20		MVI	C,03H	;Set number of bytes
21		STC		;Set carry
22	LOOP2:	MVI	A,99H	;Load accumulator with 99H
23		ACI	00H	;Add zero with carry
24		SUB	M	;Produce complement of subtrahend
25		MOV	M,A	;Store result
26		DCR	C	;Done if C=0
27		JZ	IDNEG	
28		INX	H	;Address next byte
29		JMP	LOOP2	
30	IDNEG:	MVI	B,00H	;B=00H identifies negative number
31		JMP	CKMSZ	
32	IDPOS:	MVI	B,FFH	;B=FFH identifies positive number
33	CKMSZ:	LXI	H,RSLT+1	;H and L address byte RSLT+1
34		MVI	A,FFH	;Load accumulator with FFH
35		ANA	M	;AND accumulator with byte in memory
36		JNZ	UPDTE	
37		INX	H	;H and L address byte RSLT+2
38		MVI	A,0FH	;Load accumulator with 0FH
39		ANA	M	;AND accumulator with byte in memory
40		JNZ	UPDTE	

continued on next page

```
41          LDA    RSLT     ;Load accumulator with byte in RSLT
42          CPI    02H      ;Carry=1 if byte in RSLT less than 2 (Note 1)
43          JC     CONT1    ;(Note 2)
44          LDA    RSLT     ;Load accumulator with byte in RSLT
45          CPI    04H      ;Carry=1 if byte in RSLT less than 4 (Note 3)
46          JC     CKSGN
47  UPDTE:  LXI    D,PRVS   ;D and E address previous ADC data
48          LXI    H,CRNT   ;H and L address current ADC data
49          MVI    C,03H    ;Set number of bytes
50  LOOP3:  MOV    A,M      ;Move byte in memory to accumulator
51          XCHG            ;Switch D and E with H and L
52          MOV    M,A      ;Store in memory
53          DCR    C        ;Done if C=0
54          JZ     CONT2
55          XCHG            ;Reswitch D and E with H and L
56          INX    D        ;Address next byte of previous ADC data
57          INX    H        ;Address next byte of current ADC data
58          JMP    LOOP3
59  CKSGN:  LXI    H,CNST   ;H and L address constant
60          LXI    D,PRVS   ;D and E address previous ADC data
61          MVI    C,03H    ;Set number of bytes
62          MOV    A,B      ;Move contents of B to A
63          ANI    01H      ;If zero, result is negative
64          JZ     DECP
65  INCP:   CALL   DADD     ;Increment previous ADC data
66          JMP    CONT2    ;(Note 2)
67  DECP:   CALL   DSUB     ;Decrement previous ADC data
68          JMP    CONT2    ;(Note 2)
```

Notes

1. Operand 02H suitable for jitter of ±1 count (see text).
2. Program continuations 1 and 2 (see Fig. 2).
3. This operand should be greater than that in Note 1.

Lines 1-12: Temporary storage of current data in RSLT.

Lines 13-17: Calculate difference between current and previous ADC data (result is in 10's complement).

Lines 19-26: Calculate magnitude of negative difference.

Lines 33-40: Check most significant bytes=0.

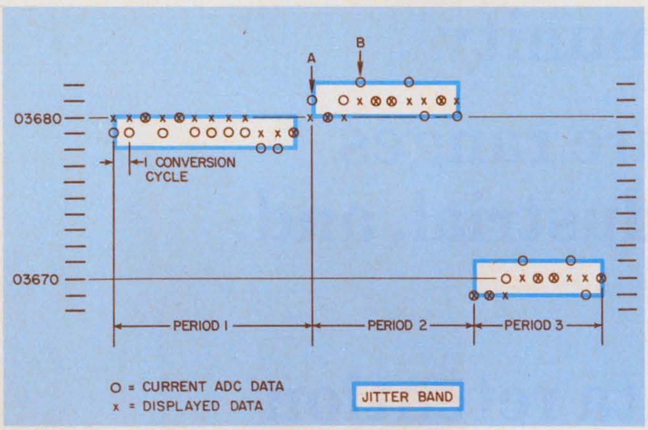
Lines 47-58: Update previous ADC data.

Lines 59-64: Check sign of result.

2. **The 8080A program for the electronic weighing system** uses only 68 lines of code, a pretty small amount compared to the over-all system program. This routine contains the entire jitter elimination scheme.

```
ROM:

Address                 Contents

CNST          01   }Constant to be added to{Least significant
CNST+1        00   }or subtracted from      {        .
CNST+2        00   }value in PRVS           {Most significant


RAM:

CRNT          Least significant 2 digits of current ADC data
CRNT+1        Next 2 digits
CRNT+2        Most significant digit (bits 0-3)
PRVS          Least significant 2 digits of previous ADC data
PRVS+1        Next 2 digits
PRVS+2        Most significant digit (bits 0-3)
RSLT          Least significant 2 digits of result of current minus previous
                                                                 ADC data
RSLT+1        Next 2 digits
RSLT+2        Most significant digit (bits 0-3)
PTR           Pointer for return address from subroutines
```

3. **Three bytes of RAM** hold the weighing system's BCD data, as shown in this memory map.



4. **Data eventually settle** in the middle of the jitter band, but not in one conversion cycle. It can take up to three cycles for the data to finally settle.

display until the difference between the current a/d converter output and the displayed value is larger than 1. When that happens, the display is updated to read 03679. But as long as the converter input is constant, the display remains steady—jitter of ±1 digit in the converter output is ignored.

In period 2, assume that the converter output is incremented to 03681. When a change larger than 1 occurs at A in Fig. 4, the displayed data are also incremented by one. This doesn't bring the data into the middle of the error band yet. But if the next change, at B, exceeds 1, the display is increased by one. Now the data settle.

Say a big change takes place in period 3. The converter output goes down to 03670, which represents a change of more than four. So the increment/decrement-by-one routine in the flow chart (Fig. 1) is bypassed to allow current-converter data to be transferred directly to PRVS. The display is updated and will eventually settle to the middle of the error band, but for large changes, this direct type of transfer speeds up settling time.

The number of digits that the system handles can be as large as you want, but you must allow for the converter's jitter characteristics. The 8080A program is for a five (actually 4 1/2)-digit converter, whose jitter is ±1 count. But if jitter were ±2 counts, you would have to change operand 02H in the program to 03H. Operand 04H could then either remain the same or be incremented—the only requirement is that it be greater than 02H.

Note that the program is written to handle unsigned converter data. However, if your system uses both positive and negative information, you can retain the principles of the program with some additional programming modifications.

Finally, the technique is not limited to a/d converters and scales—you can also cure jitter problems in frequency counters and other digital applications.■■

Acknowledgment

The material for this article originated from work done by the author while he was employed by Siliconix Ltd., Swansea, UK.

Check your memory system design requirements.

- Low power drain in both active and standby conditions
- Fast access times
- TTL compatibility in/out
- High noise immunity
- Full temperature ranges for military, industrial, and commercial
- Guaranteed data retention

ECL triple-line receiver makes a stable harmonic oscillator

Use all three sections of a 10116 ECL triple-line receiver (Motorola) to build a harmonic crystal oscillator (Fig. 1) with less frequency shift than standard oscillator designs. When you tune the LC tank circuit of a standard oscillator (Fig. 2) for a desired harmonic, output frequency can shift because of the changing load seen by the crystal.

The first section of the line receiver in Fig. 1 is connected as a fundamental-frequency crystal oscillator in the normal way. Pin 11 (V_{BB}) biases the inputs, and crystal Y_2, connected in a positive-feedback loop, creates the oscillation. Capacitor C_2 allows you to fine-tune the frequency.

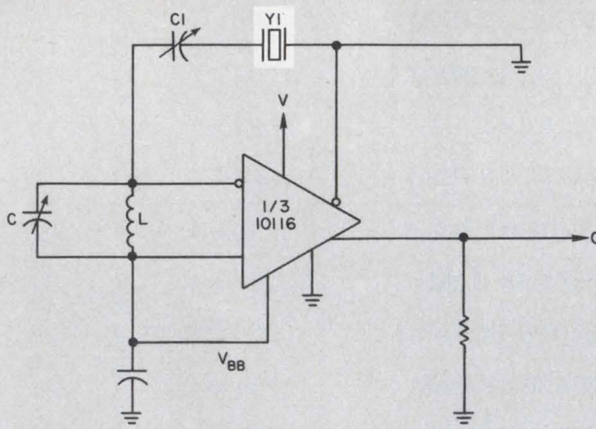
The second section is a harmonic amplifier that common-mode-rejects the fundamental frequency, while the desired harmonic, tuned by the L_1C_1 tank, is amplified. To tune for the harmonic, put your scope probe on pin 14 while adjusting inductor L_1 for a peak.

The last section of the line receiver, designed as a Schmitt trigger, is used to buffer and square-up the output waveform. And transistor Q_1, at the output, serves as a TTL interface.

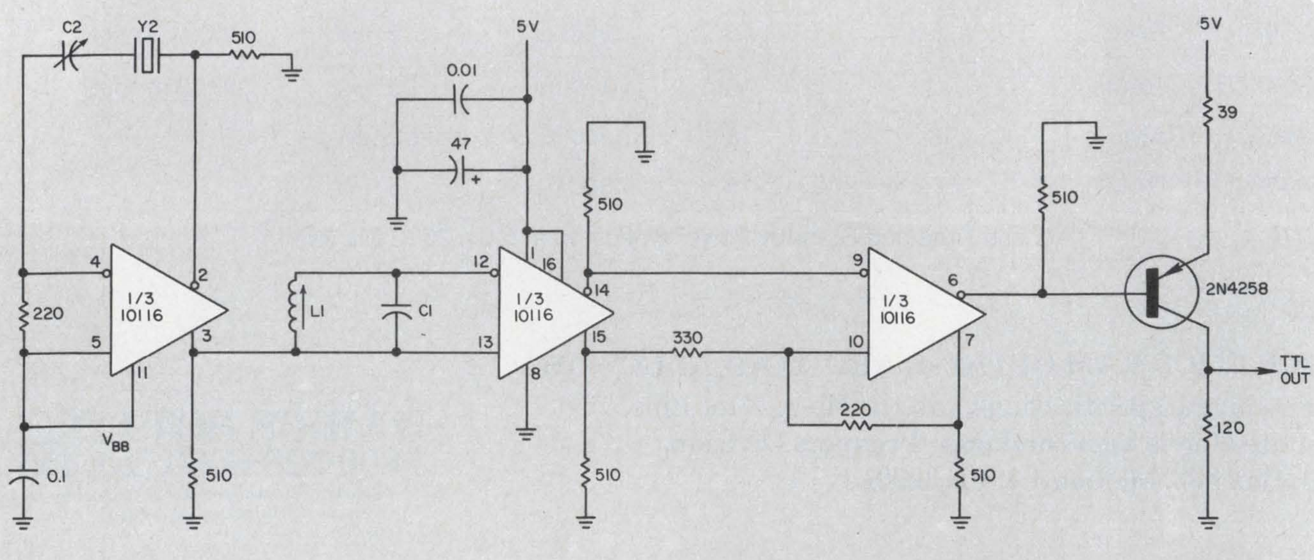
This circuit uses an 8.5-MHz crystal—the harmonic oscillator passes the third harmonic—to give an output frequency of 25.5 mHz. With a 10116 line receiver, you can operate at frequencies greater than 60 MHz. But for very-high-frequency work, you'll have to use the faster 10216 version.

Robert A. Cervas, Project Engineer, The Hickok Electrical Instrument Co., 10514 Dupont Ave., Cleveland, OH 44108.

CIRCLE NO. 311



2. **Single-stage oscillators** suffer from frequency shift because the load seen by crystal Y_1 changes.



1. **A stable harmonic oscillator has three stages:** Stage 1 generates the fundamental; Stage 2 is a filter and harmonic amplifier; and Stage 3 buffers and squares-up the output.

Pseudorandom tone generator produces 16 tones over its frequency range

With a 555 timer wired as an astable multivibrator, and a 7-bit binary counter connected to make the timer work as a pseudorandom generator, the circuit in Fig. 1 generates 16 different tones randomly over a 6 kHz range. Not only is the frequency range surprisingly large, but you can use the technique to divide a frequency range into even finer increments by adding a few more resistors.

When the Control line (Fig. 1) is held low, U_1, a 7-bit binary counter (MC14024, Motorola), counts the clock pulses coming through NOR gate U_4. But the timer, U_3, is disabled because a low on the Control line holds its V_{cc} and reset inputs (pins 4 and 8) low. A high on the Control line disables the clock input to U_1, which effectively captures a bit pattern on its output pins, Q_1 through Q_4. Simultaneously, the high on pins 4 and 8 of U_3 enables the oscillator.

The bit pattern at U_1 determines which combination of resistors R_1 through R_4 is connected in parallel with R_5. This parallel resistor combination then determines the oscillation frequency of U_3. If you use a clock source of about 1 kHz, the Control line can be operated simply by closing a switch.

The circuit breaks a frequency range of 1 to 7 kHz into 16 equally spaced frequency divisions (Fig. 2). Binary weights must be assigned to resistors R_1 through R_4, and all component values can be determined from

$$f_L = 0.72/R_5C_1, \quad (1)$$

$$f_H = f_L + 1.35/R_4C_1. \quad (2)$$

Resistors R_1 through R_3 are weighted as follows:

$$R_1 = 8R_4$$

$$R_2 = 4R_4$$

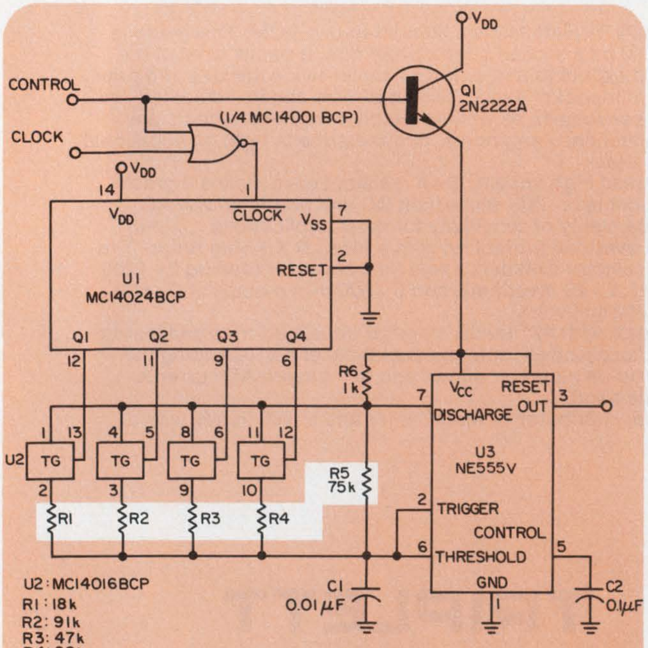
$$R_3 = 2R_4.$$

Eqs. 1 and 2 are fairly accurate as long as the parallel combination of R_1 through R_5 is at least ten times greater than R_6. But the frequency precision depends on the tolerances of the resistors. For this circuit, ±5% carbon composition resistors are used, so the difference between any two frequencies is not exactly constant (see Fig. 2).

If you need a precision generator, add a trimmer capacitor in parallel with C_1 to reach the low-frequency limit, and use ±1% metal-film resistors for R_1 through R_6.

Michael F. Gard, Senior Biomedical Engineer, Veterans Administration Hospital, 915 North Grand, St. Louis, MO 63106.

CIRCLE NO. 312



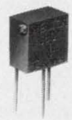
1. **The parallel combination of resistors R_1 through R_5** determines the output frequency of this pseudorandom tone generator. The frequency is randomized by the count stored in U_1.

Counter outputs				Frequency (Hz)
Q_4	Q_3	Q_2	Q_1	
0	0	0	0	890
0	0	0	1	1260
0	0	1	0	1573
0	0	1	1	1937
0	1	0	0	2353
0	1	0	1	2715
0	1	1	0	3021
0	1	1	1	3378
1	0	0	0	3747
1	0	0	1	4101
1	0	1	0	4400
1	0	1	1	4748
1	1	0	0	5144
1	1	0	1	5491
1	1	1	0	5783
1	1	1	1	6124

mean frequency difference between steps = 349 Hz

2. **The difference between any two frequencies is not constant,** but that's because ±5% resistors are used in the design. Your design can be more precise if you use tighter tolerance components.

actual size



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The 860 features 16 turns of adjustability in either top or side adjust models. Its power rating is ¼ watt at 85° C, with an operating temperature range of -55°C to +150° C. The 860 is completely sealed against contaminants. Military (RJ26) and Established Reliability (RJR26) models are also available. Write or phone today for evaluation samples, specifications and pricing.

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CIRCLE NUMBER 107

Divide input events with a low-cost, voltage-programmed pulse sequencer

A pulse train of digital data can be divided by a variable integer number with a CMOS pulse sequencer. The divisor is a ratio set with a low-cost multiturn potentiometer, connected to the noninverting input of a general purpose op amp. Conventional divide-by-N sequencers use programmable counters or binary-rate multipliers, which work well with a fixed integer divisor. But when divisors must be variable, expensive coded switches are usually required.

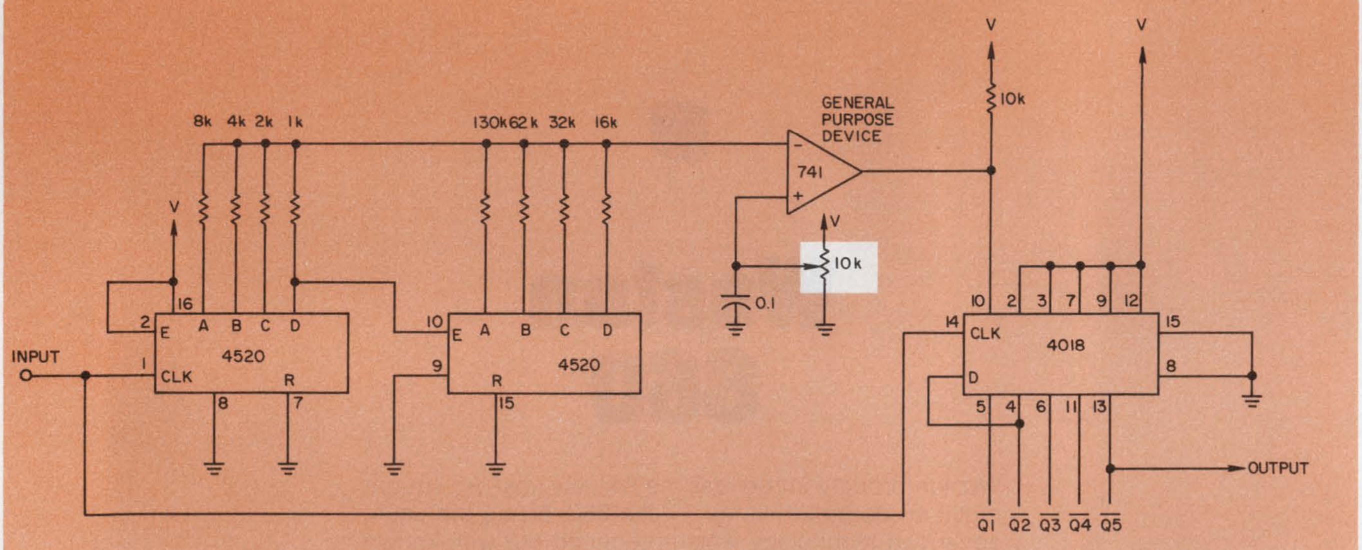
Event inputs to the circuit produce a positive-going ramp voltage at the output of both halves of the MC14520 binary counter. The binary-weighted resistor network on the counter-output lines is summed into the inverting input of the op amp, which is connected as a voltage comparator. When the ramp voltage exceeds the comparator's threshold (set by the 10-kΩ pot), the output voltage switches from high to low, and enables the 4018 to begin counting.

The preset input of the 4018, rather than the reset input, is used to inhibit the count—presetting with all ONEs forces the outputs low, and inhibits counting at the same time. To minimize counting errors and provide additional scaling, establish a fixed predivision ratio by feeding counter outputs back to the input. For the 4018 shown, the ratio is four, but you can change it to suit your application.

A regulated power supply will give you the best accuracy, but the circuit is reasonably accurate and adjustable over a 256-step range. The output signal is a pulse train whose length corresponds to the comparator trip points established by the ramp, and the potentiometer position. For low-speed applications, a general-purpose op amp works fine.

Wayne Kirkwood, Engineer, Micmix Audio Products, 2995 Ladybird Lane, Dallas, TX 75220.

CIRCLE NO. 313



Divide input events by a variable number with this pulse sequencer. The 10-kΩ potentiometer lets you set the division ratio at the comparator input. Additional scaling is provided by the 4018.

IFD Winner of January 18, 1978

Jerald Graeme, Manager, Monolithic Engineering, Burr-Brown Research Corp., International Airport Industrial Park, Tucson, AZ 85734. His idea "Twin-tee Filter Rejects more than 70 dB with Capacitance-Multiplier Circuit" has been voted the most valuable of Issue Award.

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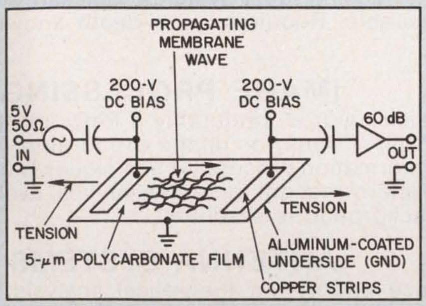
Delay-time losses dive with waves on membrane

A low-cost delay line that makes use of the properties of waves propagating on a thin, stretched membrane has low propagation losses and delays up to several milliseconds. These waves are theoretically free of dispersion effects that limit the performance of other types of delay lines. The propagation velocity of the waves is determined solely by the tension applied to the membrane.



The membrane line, electrostatic in operation, has been developed at Finland's University of Helsinki. The line is made of a polycarbonate film 5-μm thick and about 2.5 cm wide. One side of the film is coated with a thin aluminum layer, which serves as the ground electrode. The input and output are applied and taken from two 0.5-mm-wide copper strips etched on a printed-circuit board and suspended close to the uncoated side of the film.

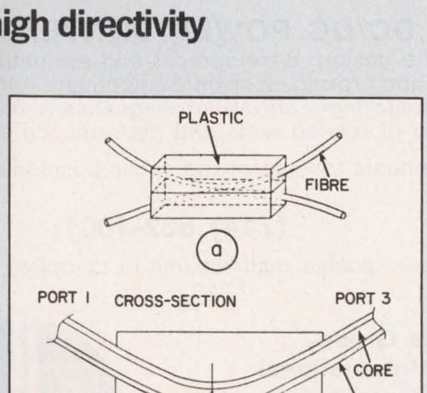
Prototype lines operate with a 200-V-dc bias on the copper input and output transducer strips. Inputs of 5 V from a 50-Ω line have been demonstrated to launch 400 to 500-kHz waves with a velocity of 200 meters per second.

Delays of several milliseconds have been obtained with a tension of 5 Newtons/cm. Propagation losses are small—about 0.15 dB/cm at 100 kHz. Time-bandwidth products of 500 have been achieved.

When operating in a vacuum, line performance improves: Dispersion effects below 50 kHz disappear and propagation losses decrease even further. University researchers predict that the frequency response can be extended into the low-MHz regions.

Low-loss optical coupler has high directivity

A fiber-optic coupler not only gives 50-50 power division between two output fibers with very low loss, but also has high directivity which makes it suitable for duplex transmission links. The fibers of the coupler, developed by Matsushita Electric, in Japan, are multicomponent, multimode step-index glass. Both fibers have a 100-μm core diameter, a 25-μm cladding thickness and a numerical aperture of 0.29. The refractive indices of the core and cladding are 1.543 and 1.515, respectively.



The two fibers are first mounted in separate plastic blocks as shown in the figure. The blocks are then ground and polished on the convex side of the fiber curve until a few microns of the core glass are removed. The exposed cores are then brought into contact and clamped together with a matching oil (refractive index, 1.475) applied to the mating surfaces.

When either input port is illuminated with 830-nm infrared light from a LED, the outputs from ports 3 and 4 measure between 45 and 47% of the input, which means an insertion loss of 0.36 dB. Measuring the output from port 2 and comparing it with that from 4 gives a directivity of 47.0 dB.

Loudspeaker distortion damped out by fluid

Magnetic fluid in the air-gap of a loudspeaker cone's driving unit cuts down on distortion by eliminating the mechanical resonances of loudspeaker-cone driving elements.

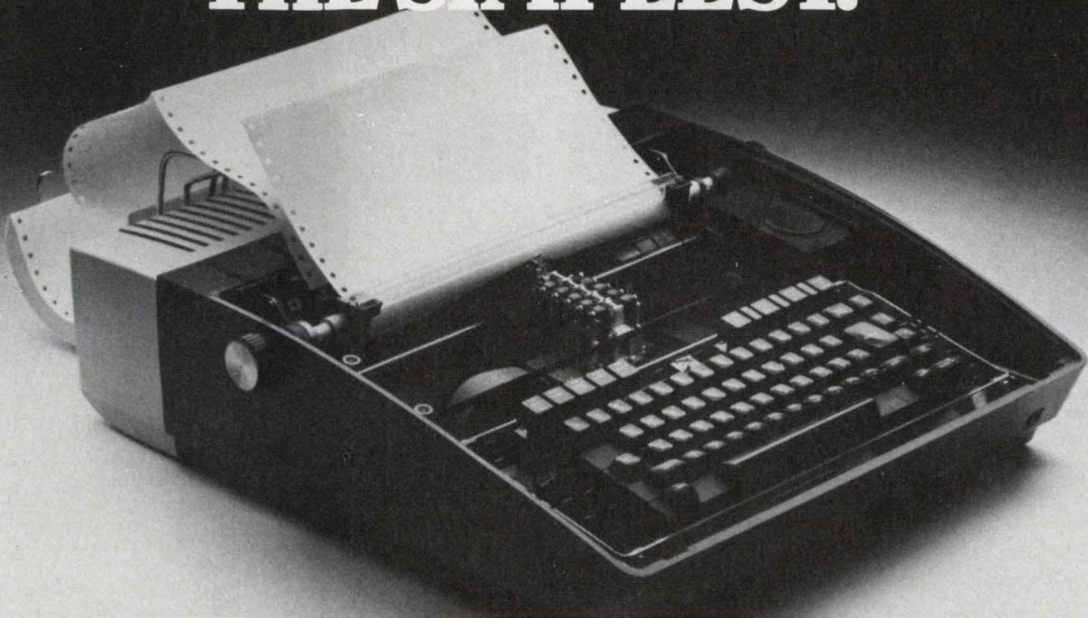
Distortion is particularly undesirable in high-fidelity loudspeakers. In a three-speaker unit, for example, the resonance of the midrange driver may fall within the audio range.

One common solution is to tailor the cut-off slopes of the crossover networks, which separate the bands of frequencies being fed each of the three speakers. This tailoring takes the distortion frequency out of the audio range being handled by the unit, but the steep slopes needed in these filters are themselves a source of distortion, and cause high-frequency ringing.

The new approach, used by the French loudspeaker firm, Auditor France, damps out the midrange resonances with Ferrofluid, which consists of magnetic particles suspended in a viscous oil. Ferrofluid, which is made in the U.S. by Ferrofluidics Corp. (Burlington, MA), has been used by American loudspeaker manufacturers but only to aid heat dissipation.

In the French application, a little bit of Ferrofluid is injected into the gap in which the voice coil moves, and is held there by the loudspeaker-magnet field. Tests show that injecting the fluid damps out a troublesome 900-Hz resonance, and gives the loudspeaker system a smooth response up to 20 kHz.

IT'S NO COINCIDENCE THAT THE MOST RELIABLE 30 CPS TELEPRINTER IS ALSO THE SIMPLEST.



Lift the cover on the Teletype* model 43 teleprinter and you'll be surprised at how little there is inside. Just five pluggable major components.

Now if it's this simple on the inside, imagine how reliably it'll perform on-line.

Because the less there is, the less there is that can go wrong. In fact, there's so little that can go wrong that the recommended preventative maintenance schedule is only twice a year.

Naturally, there are other features about the model 43 that are impressive. The first is the $800 OEM price. And that includes a TTL interface. It's also available with EIA/current loop interfaces in both dual port—so you can add another device—and single port versions. Then there's the high degree of legibility from the 9-wire impact printhead—with a service life that averages 300 million characters; low operating and maintenance costs; and built-in test capabilities.

The model 43 will also impress your customers. It's compact, attractive, and quiet. Plus it helps save paper and duplicating costs by printing 132 characters per line on 12″ wide by 8½″ long fanfold paper. Plus an 80-column friction feed version is also available.

The way we see it, a printer has to be simple in order to be reliable. And the way you see it, a printer has to be reliable in order to be efficient.

No wonder we're getting a reputation as the OEM printer people.

THE OEM PRINTER PEOPLE

*Teletype is a trademark and service mark of the Teletype Corporation.

CIRCLE NUMBER 211

CERMET TRIMMERS

Type A: ¼" dia., single turn, 10 ohms to 2.5 megs ±10%, 0.5W at 85°C, immersion sealed, 6 terminal options. TCR ±35 PPM/°C typical. Pub. 5238. **$0.96***

Type S: ⅜" dia., single turn, 50 ohms to 1 meg ±10%, 0.5W at 85°C, immersion sealed, top or side adjust. TCR ±35 PPM/°C typical. Pub. 5208. **$1.15 or 1.40***

Type E: ⅜" square, single turn, 10 ohms to 2.5 megs ±10%, 0.5W at 70°C, immersion sealed, 14 terminal options. TCR ±35 PPM/°C typical. Pub. 5219A. **$0.49***

Type D: ⅜" dia., single turn, 10 ohms to 2.5 megs ±20%, 0.5W at 70°C, dust cover, 8 terminal options. TCR ±35 PPM/°C typical. Pub. 5240. **$0.37***

Type 90: 7/16" square, single turn, 100 ohms to 2 megs ±20%, 0.5W at 70°C, 1.0W at 40°C, open frame, 2 terminal options. TCR ±100 PPM/°C typical. Pub. 5242. **$0.41***

Type MT: ⅜" square, 20 turn, 10 ohms to 2.5 megs ±10%, 0.5W at 70°C, immersion sealed, 7 terminal options. TCR ±35 PPM/°C typical. Pub. 5241. **$1.13***

Type RT: ¾" long, 20 turn, 10 ohms to 2.5 megs ±10%, 1.0W at 40°C, immersion sealed, 4 terminal options. TCR ±35 PPM/°C typical. Pub. 5237. **$0.65 or 0.93***

HOT-MOLDED COMPOSITION TRIMMERS

Type Y: ½" dia., single turn, 100 ohms to 5 megs ±10% or ±20%, 0.25W at 50°C, dust/splash resistant, 5 styles, non-linear tapers. Pub. 5209. **$0.90 to 1.59***

Type F: ½" dia., single turn, 100 ohms to 5 megs ±10% or ±20%, 0.25W at 70°C, immersion sealed, 6 styles, non-linear tapers. Pub. 5234. **$1.00 to 1.62***

Type O: ½" dia., single turn, 100 ohms to 5 megs ±10% or ±20%, 0.40W at 70°C, immersion sealed, 4 styles, non-linear tapers. Pub. 5235. **$1.20 to 1.58***

Type FD: ½" dia., 2 section, 1 turn, 100 ohms to 5 megs ±10% or ±20%, 0.25W at 70°C, immersion sealed, 4 styles, 5 tapers, 2 attenuators. Pub. 5231. **$2.65 to 4.10***

Type BT: ½" dia., 2 section, 1 turn, for 75 ohm Bridged-T pad applications, dust/splash resistant, side and top adjust versions. Pub. 5236. **$2.49***

Type N: 1¼" long, 25 turn, 100 ohms to 2.5 megs ±10% or ±20%, 0.33W maximum at 50°C, immersion sealed. Pub. 5206. **$2.50 or 2.65***

Type R: 1¼" long, 25 turn, 100 ohms to 2.5 megs ±10% or ±20%, 0.25W at 70°C, immersion sealed, bushing mount option. Pub. 5205. **$2.87 to 3.73***

*1000 piece price.

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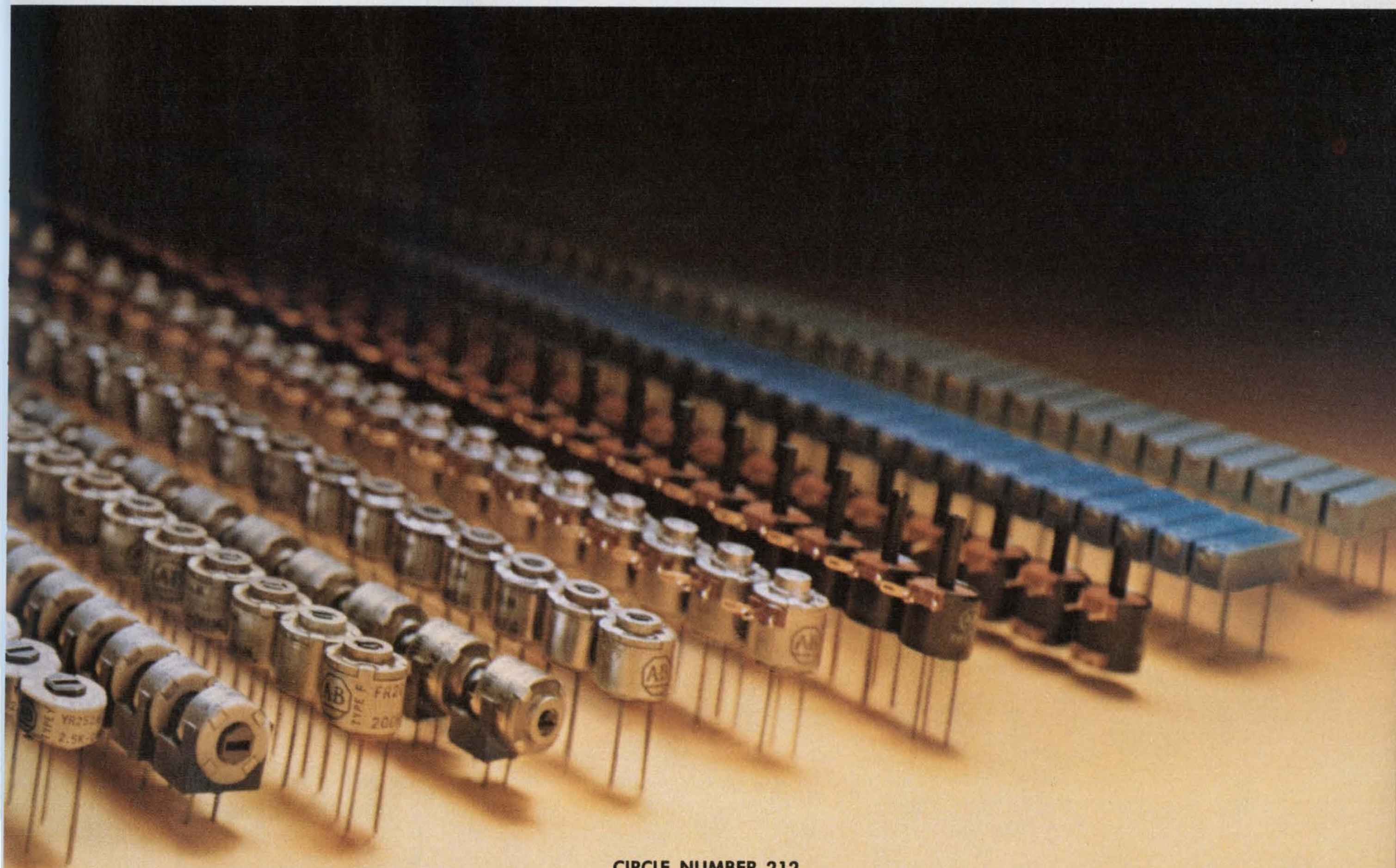
EC172A



CIRCLE NUMBER 212

FOR RENT

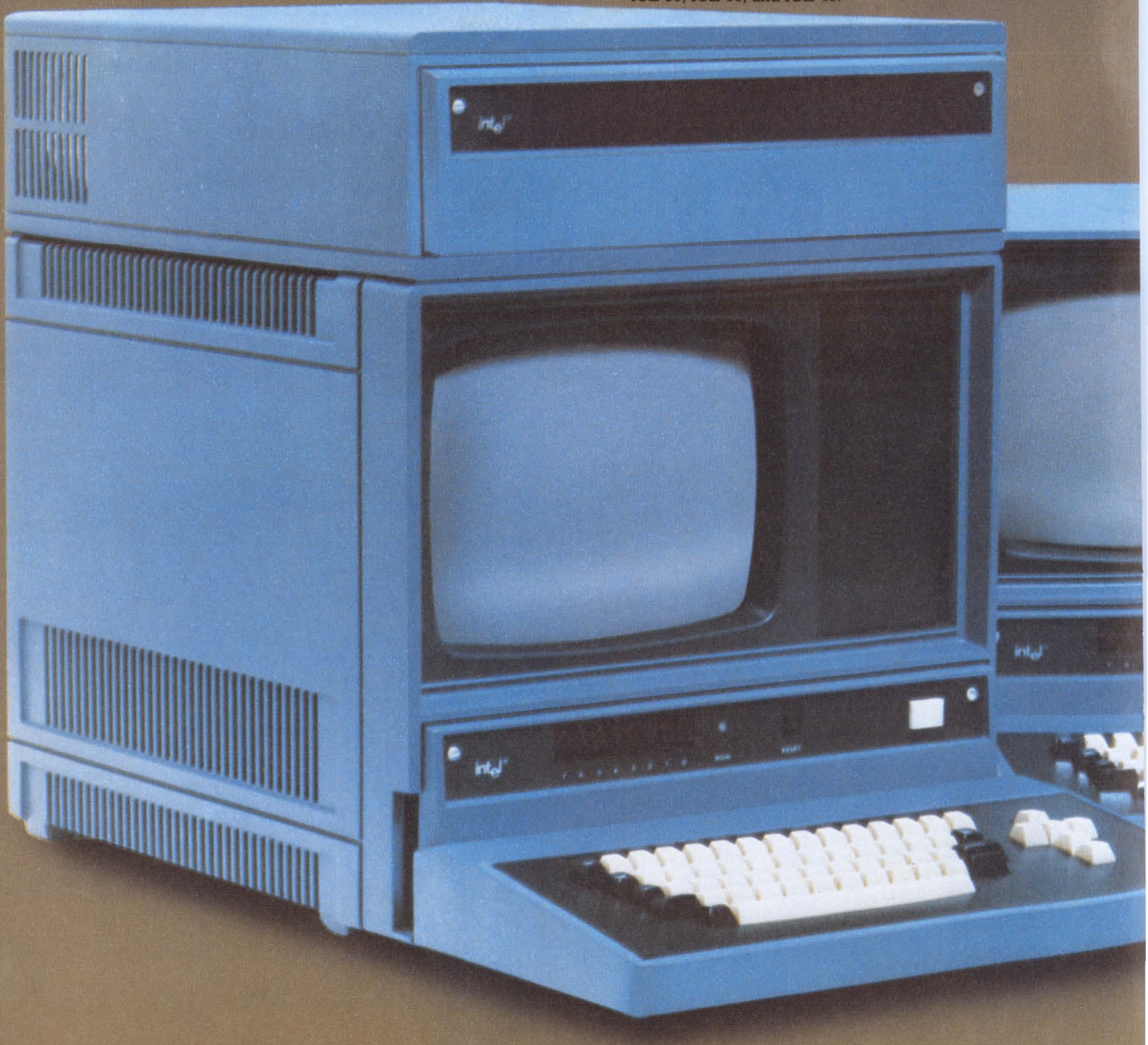
Intel's amazing new generation Intellec® Series II Microcomputer Development Systems . . . everything you'll ever need to develop a microcomputer-based product.

The Intellec Models 210, 220 and 230 are the first fully integrated, packaged tools for developing and testing your microcomputer-based products. They'll each fit easily on your lab bench to help cut months from your design cycle.

You can rent the newest generation microcomputer development systems today from REI and start taking advantage immediately of the fast, flexible and cost-efficient Intellec systems. Each can help you build a more reliable product. And because these new Intellec systems are so compact, they use less of your valuable laboratory bench space than any other microcomputer development aid on the market.

Model 230 is the most powerful member of the Intellec Series II family, providing you two double-density floppy diskettes with over 1-million bytes of on-line data storage, 64K bytes of RAM and an integral CRT.

The compact Model 230 also gives you a detachable, typewriter-style keyboard with upper and lower case characters and cursor controls. Its powerful ISIS-II Diskette Operating System has relocatable and linkable software and allows the use of two high-level programming languages, PL/M-80 and FORTRAN 80, plus the microcomputer industry's most comprehensive line of macro assemblers. The system has over 1-million bytes of on-line diskette storage and will support up to 2½-million total bytes. The System Monitor (in ROM memory) provides a Self-Test system diagnostic, and interfaces for a printer, paper tape reader/punch and universal PROM programmer are also provided. Model 230 gives you access to all the tools needed for your development work, including software editors, assemblers, compilers and debuggers, plus Intel's famous In-Circuit Emulators—ICE-80, ICE-85, and ICE-48.



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Take a look at some of Dow Corning's electrical/electronic design problem solvers.

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Durable, flexible conformal coating. For a tough, clear, shock-insulating conformal coating on circuit boards, you can't beat Dow Corning® 3140 RTV silicone coating. This flowable, one-part silicone coating is the only conformal coating that has UL component recognition to 180 C and also meets the requirements of Mil Spec MIL-I-46058-C and MIL-A-46146.

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CIRCLE NUMBER 214

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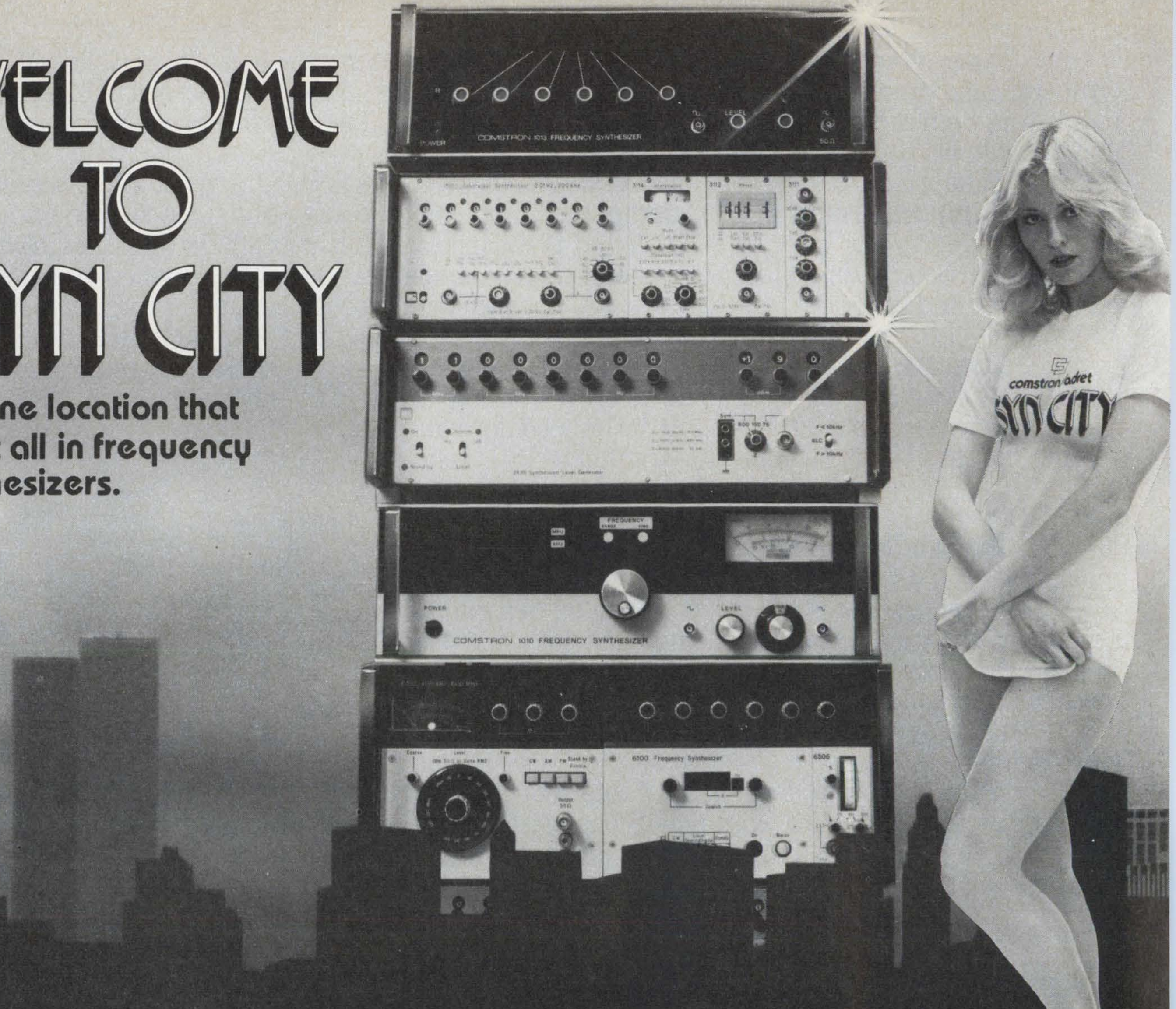

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- **Model 1010**—Spin-wheel tuned frequency synthesizer, 1.0 Hz - 10 MHz in 2 ranges
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- **Model 2400**—Level generator/Frequency synthesizer, 300 Hz - 14 MHz
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CIRCLE NUMBER 76

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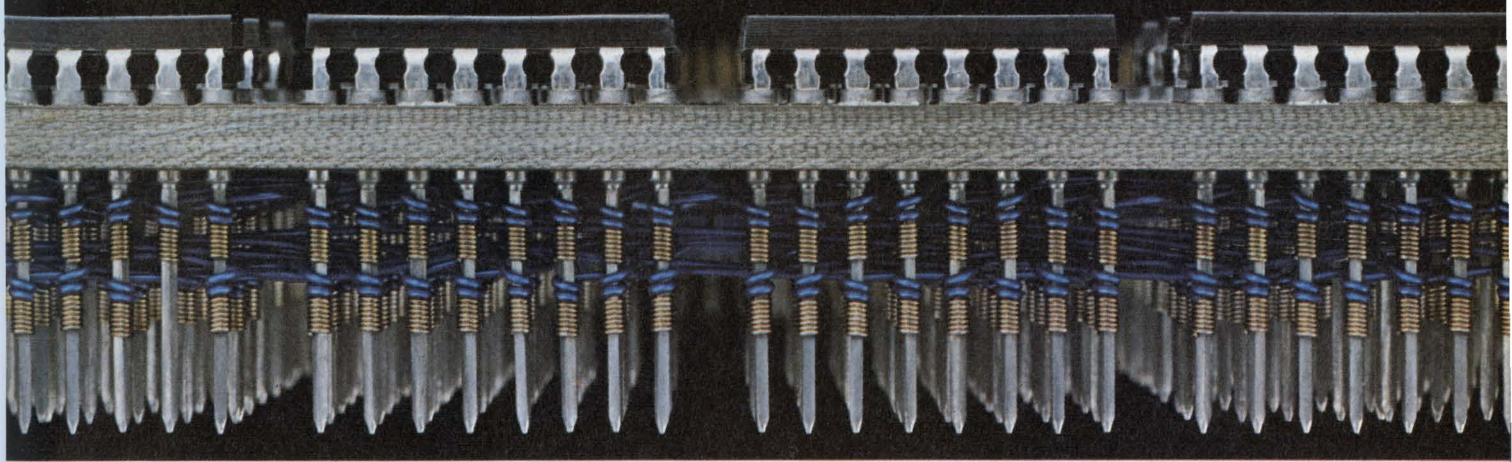

Today more than ever before, the substantial time and money savings made possible by Wire-Wrap* packaging panels are making this interconnection method the logical choice of countless project engineers.

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Large scale ECL wire-wrap panel with 660 SIP/DIP patterns.

Give us a chance to demonstrate exactly how Wire-Wrap panels can improve your system's electrical and heat transfer characteristics, planar density, and reliability. Also, we'll show you how wire wrapping's unmatched flexibility can always help get your products to market faster, often at less total cost than with any other method.

Take our ECL and Schottky panels. Thousands of Augat boards are already at work in high speed logic applications, bringing our customers reduced costs, better high speed transmission, and lower noise levels.

One Augat customer is using ECL panels in the CPU of a major new computer because, in addition to density and flexibility considerations, it got them to market months ahead of timetables required by other interconnection techniques.

Our new hi-density I/O V-series has become popular because it features a two-piece connector that crams up to 96 I/O connections into each group of 35 IC positions.

As for microprocessors, we offer an extensive new series specifically dedicated to μP based systems. The concept is modular, with panels and complete accessory hardware for CPU, I/O, memory, and peripheral control and processing.

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Hi-density I/O μP packaging system.

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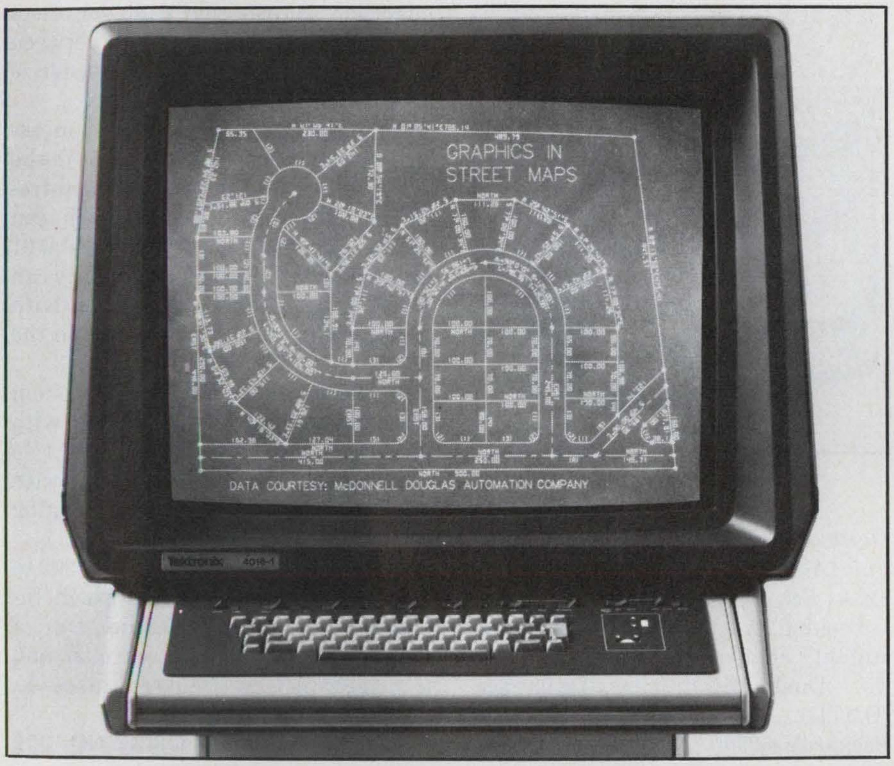
GENERAL ELECTRIC

CIRCLE NUMBER 111

New products

Computer terminal displays more information by almost half



Tektronix, P.O. Box 500, Beaverton, OR 97077. (503) 644-0161. P&A: See text.

The largest computer display terminal—the Tektronix 4016-1—lets you plot 47% more graphics information than previously possible. The terminal's 25-inch screen can hold over 100,000 0.1-in.-long vectors, and can draw the vectors at 20,000 cm/s. Tek's largest unit up 'til now, the 19-in. 4014-1, draws at 15,000 cm/s.

Moreover, the 4016-1's larger screen means better resolution. And its faster speed means that larger plots take no longer than on the smaller 4014-1. Consequently, software timing requirements don't have to be changed if you switch from the 4014-1.

The 4016-1 is compatible with the Tektronix Plot 10 software and all bus interfaces, including those for communications, peripherals—like hard copy printing—and the company's intelligent graphics-enhancement options.

The 4016's keyboard connects to the display via cable, so you can detach the two, if you want. In the alphanumeric mode, the 4016 provides a full ASCII character set and four standard formats, ranging from 74 characters per line by 35 lines, to 133 characters per line by 64 lines. An optional format stretches the numbers to 179 and 86—15,394 on-screen characters.

In the graphics mode, the 4016-1's specs include 4 k by 4 k (12 bits) addressable points (4096 × 3120 viewable points) and five formats, including straight, dotted and dashed lines. A special point-plotting mode addresses points absolutely, with program control of plotted point size.

The written image on the unit's direct-view storage tube is bright green on a green background. An optional filter enhances contrast with green images on a blue field.

First deliveries of the 4016-1 display terminal are expected to take place in December at an approximate cost of $20,000, which includes the Enhanced Graphics Module.

Booth No. 2309 **CIRCLE NO. 301**

13-MHz signal source programs via GPIB

Wavetek, P.O. Box 651, San Diego, CA 92112. John Roth (714) 279-2200. $4300; 4 wks.

The Model 172A programmable signal source is GPIB compatible and features full 13-MHz synthesizer performance. It has an interactive front panel with a 40-character display and storage for up to 100 generator settings. A microprocessor with its numeric capability relieves the system controller from formatting responsibility. Full function-generator versatility is provided in addition to 5-1/2-digit synthesizer resolution.

CIRCLE NO. 303

Frequency synthesizer takes many plug-ins

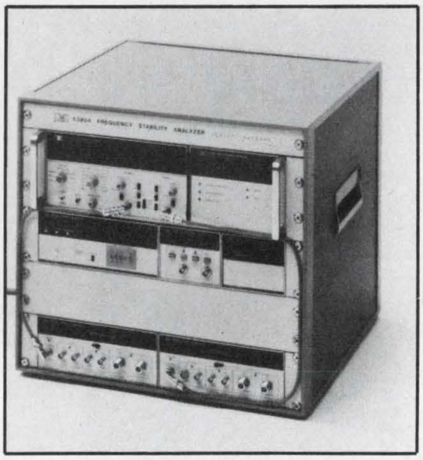
Comstron/Adret, 200 E. Sunrise Hwy., Freeport, NY 11520. Dr. Ron Juels (516) 546-9700.

The Series 6000 is a versatile, high-performance, synthesized signal generator. The series consists of two mainframes and numerous plug-ins. By interchanging plug-ins, the system functions as a frequency synthesizer, a signal generator or a spectrum analyzer. The frequency ranges, chosen by rf plug-ins, are 300 Hz to 110 MHz, 400 kHz to 600 MHz, 400 kHz to 1.28 GHz. Salient specs include resolution of 1 Hz, stability of $\pm 5 \times 10^{-9}$ per day and a noise floor of -140 dB/Hz. Modulation is AM, FM or PM, search and sweep. All functions are fully programmable, BCD or IEEE 488.

CIRCLE NO. 304

INSTRUMENTATION

Analyzer's got the tool for best stability measurement



Hewlett-Packard, 1507 Page Mill Rd., Palo Alto, CA 94304. (415) 856-4234. P&A: See text.

Looking for a standard in frequency-stability analysis? Stop here, for now. The Dual Mixer Time Difference (DMTD), an option to Hewlett-Packard's 5390A Analyzer, measures precision sources that can't be offset and eliminates dead time between measurements when you characterize fractional-frequency deviation.

With the 5390A, then, you can measure close-in phase noise or work in the time domain to get the fractional-frequency deviation. In-phase, you can work really close to the carrier—0.01 Hz to 10 kHz. The source frequency can range from 500 kHz to 18 GHz, with a sensitivity of 150 dB relative to the carrier, at 1-Hz offset.

In the time domain, the HP system uses two-sample Allan variance, with averaging times varying from 10^{-5} to 10^6 seconds. There's no dead time with the DMTD configuration for averaging periods greater than 20 μs.

The DMTD option (01) adds $5900 to the 5390A's $27,000 price, which includes, among other equipment, a desktop programmable controller and a printer-plotter. Delivery takes 12 weeks.

CIRCLE NO. 302

Data-link analyzer monitors communications

Halcyon, 2121 Zanker Rd., San Jose, CA 95131. Chuck Volkland (408) 293-9970.

The 803A uFox data-link analyzer is a diagnostic tool for data-communication systems. For on-line testing, the instrument monitors the data stream in a variety of codes and checks text, control and protocol characters. Used off-line, it simulates a CPU, a terminal or a modem to isolate any problem. Microprocessor control and a conversational language make operation easy for nonprogramming personnel. Additional features include software updating by PROM replacement, self-check routine, indicators to show the status of RS-232 leads and test points for all important leads.

CIRCLE NO. 305

Frequency counter takes 1.75-in. panel space

Systron-Donner, 10 Systron Dr., Concord, CA 94518. Rudy Wagner (415) 675-5000. $1395; 4 wks.

A "thin-line" 1.25-GHz frequency counter for IEEE-488 bus applications, Model 6043A, measures only 1.75 in. high. The instrument measures frequencies from 20 Hz to 1.25 GHz. Operation is automatic, and measurements are displayed on an 8-digit LED readout. LED indicators on the front panel show the programmable mode of the counter. Front-panel pushbuttons select resolution from 0.1 Hz to 1000 Hz in decade steps, select attenuation for inputs to 100 MHz and provide reset and hold controls. All controls except the power switch are programmable.

CIRCLE NO. 306

Suppose someone with no axe to grind designed practical one-card microprocessor systems.

Pro-Log sifts through manufacturer's claims, selects the best parts, and designs them into simple, reliable systems...
...systems flexible enough to use in a wide variety of applications. Systems easy to build, easy to service. Systems in which every part—the microprocessor, every semiconductor, every connector, every miscellaneous component—is or soon will be a second-sourced industry standard.

Card	PLS 881	PLS 888	PLS 858	PLS 868	PLS 898
Processor	8080A	8080A	8085	6800	Z-80
PROM* Capacity	4K (2708)	8K (TMS2716)	8K (2716)	8K (2716)	8K (2716)
RAM** Capacity	1K	2K	2K	2K	2K
Input Ports (8 lines)	2	2	2	2	2
Output Ports (8 lines)	3	3	3	3	3
100 Piece Price	$165	$185	$185	$185	$185

*PROM not included. **1K of RAM included.

Our comparison guide helps you avoid the pitfalls of microprocessor design.
Send for your copy today. Pro-Log Corporation, 2411 Garden Road, Monterey, CA 93940. Phone (408) 372-4593.

Pro-Log builds 8080A, 8085, Z-80, and 6800 microprocessors into one-card systems.
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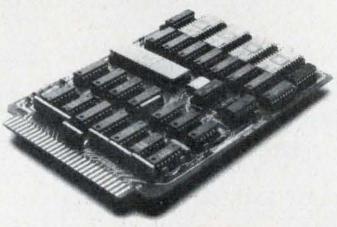
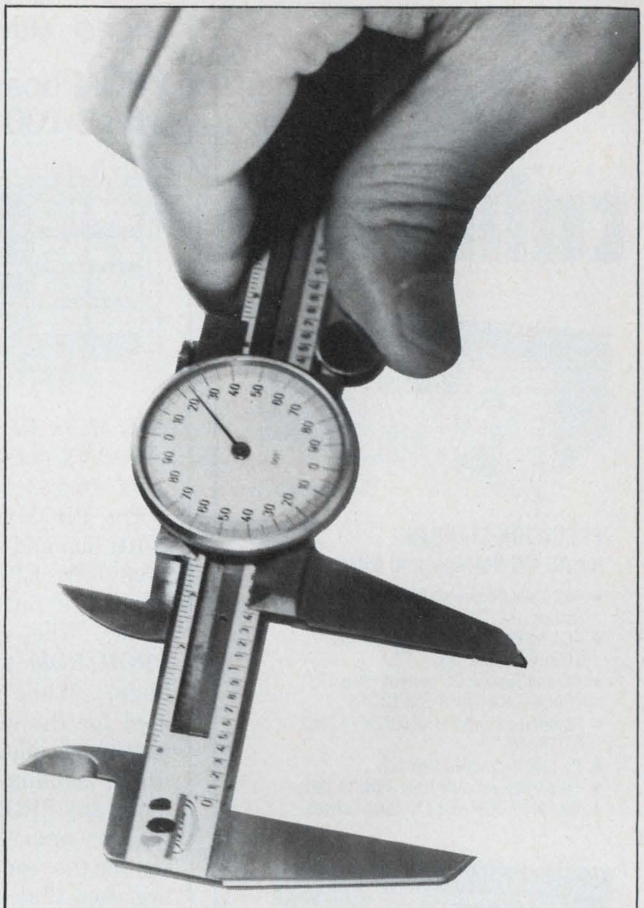


PRO-LOG CORPORATION

Microprocessors at your fingertips.

CIRCLE NUMBER 113



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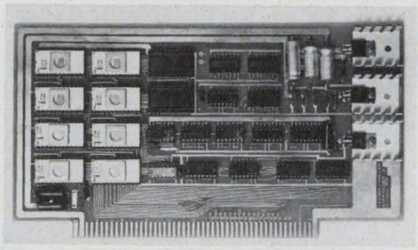
◀ CIRCLE NUMBER 114

PROM board mates with S-100 bus

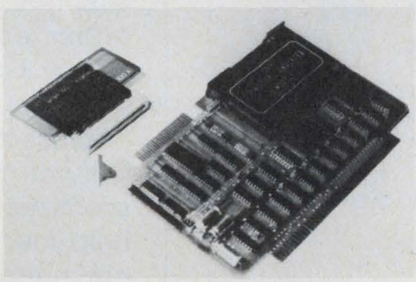


Mini Micro Mart, 1618 James St., Syracuse, NY 13203. (315) 422-4467. $59.95 (kit), $109.95 (assembled).

The PROM Board mates with the S-100 bus and can be used with eight 2708 type EPROMs with additional provisions for two other PROMs or ROMs. This provides for a total PROM/ROM storage capacity of 12 kbytes. While the board is prejumpered for the use of the PROMs as a continuous block of memory, the address decoding scheme provides for using any PROM anywhere within the memory map. Circuitry is provided for pulling the ready line low when PROMs are used that are not fast enough to run at full CPU speed.

CIRCLE NO. 307

Digital analyzers verify correct digital patterns



Phoenix Digital, P.O. Box 11628, Phoenix, AZ 85017. Bill Johnson (602) 996-8262. From $295; 4 wks.

The LS-100 series of digital signature analyzers provides the foundation for troubleshooting and repair of discrete, LSI and microprocessor circuits. Verification of correct digital patterns provides go/no-go testing as well as diagnostics. The error detection accuracy is 99.99% and identification of bad components, PC boards and entire systems is possible. Options include remote LED signature display, 32-line multiplexer, logic probes, enhanced software package and stand-alone test ability.

CIRCLE NO. 308

Rack-mounted μC conserves panel space

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. John Jones (408) 737-6593. $1345; stock.

A low-profile, completely packaged 8-bit microcomputer, the RMC80/10 requires only 3.5 in. of panel space in a standard 19-in. rack. Based on the BLC80/10 CPU board, which uses the 8080A μP, the unit includes programmable serial and parallel I/O, complete busing, power supply, fans and three expansion-board slots. The CPU has 1 kbyte of RAM and four sockets for up to 4 kbytes of PROM.

CIRCLE NO. 309

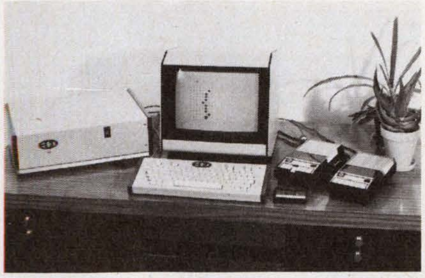
Desktop computer system is based on LSI-11

General Robotics, 57 N. Main St., Hartford, WI 53027. Don Woelz (414) 673-6800. $12,000 (single), $7155 (100 qty).

A self-contained desktop computer system, the MVT/X3 is based on the DEC LSI-11. The system includes an LSI-11, 62 kbytes of RAM, a line printer, a keyboard, three mini-floppy discs, an operating system and a 12-line by 40-character display. The total unit is packaged in a single 41 × 53 × 61-cm tabletop enclosure and weighs less than 45 kg. Floating-point arithmetic hardware is a standard feature. Nine additional dual-height QBUS slots are provided for expansion. The RAM provides 62 kbytes of self-refreshing memory with an access time of 450 ns. The line printer prints 60 char/s of a 64-character ASCII set. The mini-floppy discs store over 1 Mbyte. The display is a flat plasma panel with 12 lines of 40 characters.

CIRCLE NO. 310

μC features variable format display

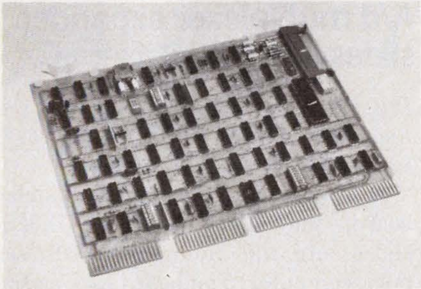


ECD, 196 Broadway, Cambridge, MA 02139. Dave Hendrickson (617) 661-4400. $3900; 4 wks.

The display processor in the Seven-X microcomputer handles formats of up to 132 columns, permitting direct display of line-printer oriented data. Software modifies, in real time, almost every display parameter. Dense text, very bold messages and bit-map graphics can be displayed in different windows of the same display. Each system has an external I/O bus driver that daisy-chains up to ten peripheral devices. Every system operates through a powerful central-system bus that supports up to 12 displays and 16 independent processors. A single stack holds up to 1 Mbyte of RAM. The basic system consists of one 16-k central processor, one display and one general I/O and system-support board.

CIRCLE NO. 320

Async serial interface mates with PDP-11



Computer Interface Technology, 2080 S. Grand Ave., Santa Ana, CA 92705. Jerry Washburn (714) 979-9920. $450; stock.

The CDL-11 module is a universal link between the PDP-11 Unibus and any asynchronous serial interface. Only one jumper is used to select a version compatible with a required DL-11 type. Register addresses, vectored interrupts and the 16 available baud rates are selected with DIP switches.

CIRCLE NO. 321

Assembler microprograms bit-slice μPs

Signetics, P.O. Box 9052, 811 E. Arques Ave., Sunnyvale, CA 94086. Rick Eklund (408) 739-7700. $775.

A microassembler that microprograms all popular bipolar (bit-slice) microprocessors is provided in a software package. The software can be used for the complete microprogramming cycle including defining microinstructions, writing and assembling programs, and generating paper tape output for ROM programming. The assembler also permits flexible editing and program alterations through iterated loops, updates and replacements, and it has a built-in test program to check system accuracy. The package is written in ANSI FORTRAN IV and can be run on any 16 or 32-bit computer with FORTRAN compatibility.

CIRCLE NO. 322

MICRO/MINI COMPUTING

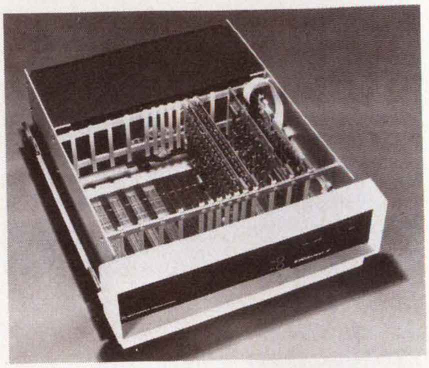
32-k add-in memory mates with PDP-11s

Fabri-Tek, 5901 S. County Rd. 18, Minneapolis, MN 55436. Orval Larson (612) 935-8811. $2450; 4 wks.

The 32-k Add-In-11, a semiconductor add-in memory system for the DEC PDP-11/04 and 11/34 minicomputers provides 32 k by 18 bits of dynamic MOS memory on a single card. It allows memory expansion in 32-kword increments to the maximum limits of the computer. The memory is hardware and software compatible with the PDP-11/04 and 11/34 modified Unibus. The unit has an on-board parity generator, checking circuits and control status register, which holds any detected parity error.

CIRCLE NO. 323

μC development tool operates at 2 MHz



Motorola Semiconductor Products, P.O. Box 20912, Phoenix, AZ 85036. Gary Hughes (602) 244-6815. $7300 to $7850; stock.

The capabilities needed to design and develop μC systems based on the M68BXX series of 2-MHz chips are offered in the EXORciser II development system. The basic system consists of the MEX6800-2 MPU II and MEX68DB2 Debug II modules, power supply and a 14-slot chassis to take PC boards with which the user emulates his μC system hardware. A motherboard provides power and signals to the μP control, data and address buses and an RS-232C port communicates with peripherals. Also supplied are 32 kbytes of memory, a macro assembler, a linking loader and a text editor program.

CIRCLE NO. 324

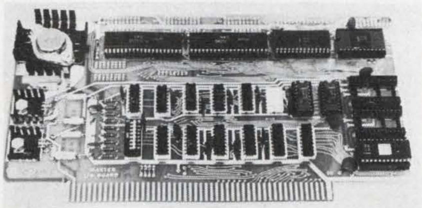
A/d multiplexer expander slides into EXORciser μC

Datel Systems, 1020 Turnpike St., Canton, MA 02021. Ron Petrelli (617) 828-8000. $295; 6 to 8 wks.

A 32-channel multiplexer expander board, the Model ST-6800ADX32S, slides into the Motorola EXORciser microcomputer. The board acts as the slave of a master a/d converter board, Model ST-6800A2B. The system, consisting of the master and slave, digitizes analog inputs to 12-bit binary resolution with 0.025% accuracy. The 64-channel system accepts +5, +10, ±5 or ±10-V input ranges. Eight inputs on the master board also accept a choice of process-transmitter current-loop resistors with ranges of 4 to 20, 1 to 5 and 10 to 50 mA. Settling time is 1 μs for the multiplexers and the channel-to-channel throughput time is 20 μs.

CIRCLE NO. 325

I/O board has memories and peripheral chips



Space Time Productions, 2053 N. Sheffield, Chicago, IL 60614. M.L. Simon (312) 348-3916. $369.

The Master I/O board contains enough ROM, RAM and I/O to allow a two-board S-100 system with choice of processors. The board can be used to emulate the Intel SBC I/O functions. Besides 1-kbyte of RAM and 3-kbytes of ROM, the board has two 8255s that can be programmed to be inputs, outputs, bidirectional, or handshake lines. One of the ports on each chip can use bit/reset commands. Each 8255 has a total of 24 I/O lines. One 8253 has three 16-bit counter/timers. The 8251 USART can be programmed for various clock division ratios, and operate at data rates up to 56 kbaud.

CIRCLE NO. 326

μC system employs dual disc drives

Gnat Computers, 7895 Convoy Ct., San Diego, CA 92111. Frank Adams (714) 560-0433. $5500; stock to 4 wks.

The Gnat-Pac System 9 combines a microcomputer with dual standard floppy-disc drives. The computer hardware includes an 8080A CPU, 32-k of RAM, 16-k of ROM space for up to 2-k PROM, four RS-232 serial I/O ports and floppy-disc controller. Dual disc drives provide 500-kbytes of storage and are optionally expandable to 1 Mbyte. The System 9 is packaged in a 10.5-in. high cabinet and includes card rack, fan, 11-slot motherboard, RFI line filter, wiring and power supply. Software includes a monitor, loader, disc operating system with assembler, editor and dynamic debugger including trace, test and debug.

CIRCLE NO. 327

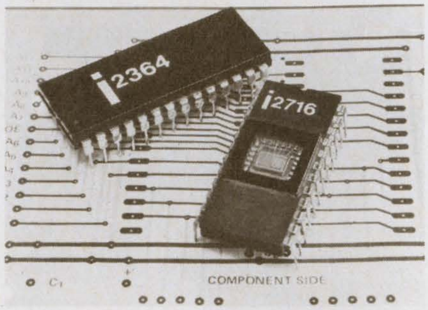
4-bit counters program synchronously

RCA Solid State, P.O. Box 3200, Somerville, NJ 08876. (201) 685-6423. $1.18 to $4.72 (100 qty); stock.

Four CMOS synchronous programmable 4-bit counters, CD40160B through CD40163B, are functionally equivalent to and pin-compatible with the industry TTL counter series 74160 through 74163. These devices are for high-speed counting use where their internal carry look-ahead capability can be used. The four counters also provide full parallel programming of states synchronously with the clock. The CD40162B decade counter and CD40163B binary counter are cleared synchronously. The CD40160B decade counter and CD40161B binary counter are asynchronously cleared. The chips are in 16-lead ceramic or plastic DIPs.

CIRCLE NO. 328

High-density ROMs operate in 300 ns

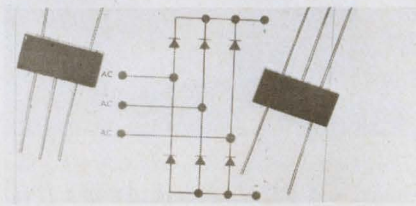


Intel, 3065 Bowers Ave., Santa Clara, CA 95051. Rob Walker (408) 249-8027. See text.

The 2332 high-density ROM stores 32 kbits and the 2364 stores 64 kbits. They are organized as 4096 × 8 and 8192 × 8 bits, respectively. Both operate at a 300-ns maximum access time, use a single +5-V supply and are directly TTL-compatible. The ROMs also provide a separate output enable function to eliminate bus contention and assure compatibility with the multiplexed bus structures of new microprocessors. Interchangeability with the new generation of 5-V EPROMs and upward compatibility to future high-density devices storing more than 64 kbits is provided. In quantities of 250, the 2332 costs $27 in plastic and $32.25 in cerdip; the 2364 costs $53.50 in plastic and $67.25 in cerdip.

CIRCLE NO. 329

Submini 3-phase bridges block up to 4 kV



Solid State Devices, 14830 Valley View Ave., La Mirada, CA 90638. Dee Peden (213) 921-9660. $10 to $25 (100 qty); stock to 8 wks.

A line of fast-recovery 3-phase full-wave bridge assemblies measures 1 × 0.19 × 0.42 in. and has reverse blocking voltages from 200 to 4000 V per leg. The SDA 240 bridges type A through E are rated at 200, 400, 600, 800 and 1000 V at 2 A. The F, G and H units have voltages of 2, 3 and 4 kV at 0.5 A. The standard units have maximum reverse-recovery times of 2 ms, while the fast-recovery units have 200-ns times. Forward voltage drops range from 1.2 to 3.5 V per leg and reverse leakage is 30 μA per leg.

CIRCLE NO. 330

IC has two independent precision timer circuits

Texas Instruments, P.O. Box 5012, M/S 308 (Attn: NE556), Dallas, TX 75222. Dale Pippenger (214) 238-5908. $0.52 to $4.32 (100 qty); stock.

A dual precision monolithic timing circuit, the NE556/SE556, is a highly stable controller that produces accurate time delays or oscillation. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other. The circuits may be triggered and reset on falling waveforms and the outputs may sink or source 150 mA.

CIRCLE NO. 331

V/f converter offers guaranteed tempco

Raytheon Semiconductor, 350 Ellis St., Mountain View, CA 94040. (415) 968-9211. $0.95 (plastic, 100 qty); stock.

A voltage to frequency converter, the RC4152, offers guaranteed temperature drift. Both the current source and voltage reference have guaranteed tempco of ±100 ppm/°C max with the one-shot stability rated at ±50 ppm/°C max. The bandwidth is greater than 100 kHz, linearity is ±0.05% max and the device is compatible with all logic forms. The RC4152 consists of a comparator, a one-shot, a precise gated current source output, an internal voltage reference and an open-collector output. The devices are available in plastic or ceramic DIPs and metal cans.

CIRCLE NO. 332

Diodes yield wideband white noise to 300 MHz

Standard Reference Lab, Pollitt Dr. S., Fair Lawn, NJ 07410. John Halgren (201) 797-3907. $11.50 to $168 (25 qty); stock to 8 wks.

A series of white-noise diodes provide broadband noise over the range of 10 Hz to 300 MHz. Each diode is in a hermetically sealed DO7 glass package and has a minimum noise output ranging from 100 to 500 μV over the specific frequency band. Other characteristics include operation from −55 to 125 C, frequency response within 2 dB, typical zener current ranges from 0.01 to 2 mA to 1 to 10 mA and load resistance of 600 Ω.

CIRCLE NO. 333

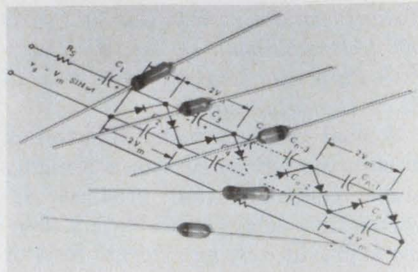
8-A triacs mount directly on heat sink

RCA Solid State, P.O. Box 3200, Somerville, NJ 08876. (201) 685-6423. $1.06 to $1.33 (100 qty); stock.

Four 8-A isolated-tab silicon triacs in the T2851 series are in the Isowatt package. That package is similar to the TO-220AB except for having a mounting flange electrically isolated from all elements of the device. These triacs can be mounted directly on the heat sink without insulating hardware, improving heat transfer. The series has an rms on-state current rating of 8 A, a full-cycle surge current rating of 100 A pk and repetitive off-state voltage ratings of 200, 300, 400 and 500 V.

CIRCLE NO. 334

Multijunction diodes rectify high voltage

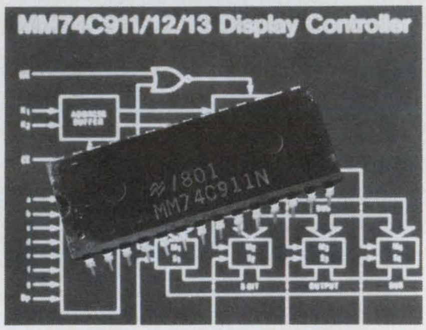


Semtech, 652 Mitchell Rd., Newbury Park, CA 91320. Bill Krause (213) 628-5392. $0.62 to $1.32 (100 qty); stock.

Mini-Stic rectifiers, Type FM50, 75, 100 and 150, have PIV ratings from 5 to 15 kV. The stacked junction rectifiers handle average currents of 25 and 10 mA at 25 C. The static forward voltages at 10 mA and 25 C are from 10 to 20 V, depending on the PIV rating. The reverse recovery time is 300 ns max. The FM50 and 75 are 0.3 × 0.12 in. The FM 100 and 150 are 0.5 × 0.12 in.

CIRCLE NO. 335

Display controller IC replaces discretes



National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. Bob Bennett (408) 737-5720. $7.40 (100 qty); stock.

The pair of CMOS intelligent display controller ICs, MM74C911/12, replaces as many as 5 to 10 discrete transistors and medium-scale ICs. The chips serve as the interface elements between a machine controller (microprocessor) and a LED or gas-discharge display. The MM74C911 multiplexes four digits with 8 bits of input information. In many cases, it is capable of both digit and segment expansion. The MM74C912 multiplexes six digits with on-chip ROM (16 × 7 bits), with the ROM addressed by four data bits. It is capable of digit expansion with the decimal point input going directly to the output. The chips are in 28-pin DIPs.

CIRCLE NO. 336

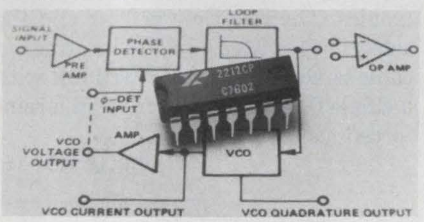
10-A transistor switches in 250 ns

TRW, 14520 Aviation Blvd., Lawndale, CA 90260. John Power (213) 679-4561. $4.30 to $7.70 (100 qty); 4 to 8 wks.

The 2N6579-84 transistors switch up to 450 V in 250 ns. With a junction and storage temperature range of −65 to +200 C, the transistors dissipate 71.4 W at 100 C. At 7 A and a collector-emitter voltage of 3 V, the units have a dc current gain ranging from 7 to 35. The devices are packaged in TO-3 metal cans.

CIRCLE NO. 337

Phase-locked loop IC improves tempco



Exar Integrated Systems, P.O. Box 62229, Sunnyvale, CA 94088. Brooks Hamilton (408) 732-7970. $3.00 (100 qty); stock.

A precision phase-locked loop circuit, the XR-2212, has a temperature stability five times better than that of previous PPLs. In addition to its improved tempco of 20 ppm/°C, the circuit has quadrature VCO outputs, frequency of 0.01 Hz to 300 kHz, supply voltage range of 4.5 to 20 V, a dynamic range of 2 mV to 3 V rms and it handles analog or digital signals from 2 mV to 6 V pk-pk. The 16-pin unit is compatible with all logic families and microprocessor peripheral systems.

CIRCLE NO. 338

8-bit latch is addressable

Solid State Scientific, Montgomeryville, PA 18936. (215) 855-8400.

The SCL 4099B is an 8-bit addressable latch with a parallel-output storage register. Data is stored in a particular bit when the bit is addressed with the Write Disable line at a low level. When Write Disable is at a high level, data entry is inhibited. All eight outputs can be used continuously, independent of the inputs. A Master Reset input resets all latches to a low level. Supplied in a 16-lead package, the circuit is available with standard or MIL-STD-883B processing.

CIRCLE NO. 339

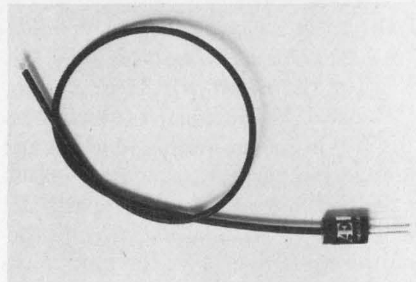
Dc-to-synchro converter has no moving parts

General Magnetics, 211 Grove St., Bloomfield, NJ 07003. (201) 743-2700. From $435; 6 wks.

Having no moving parts, the MAC 1562-1 dc-to-synchro converter develops a fully-isolated 400-kHz, 11.8-V line-to-line, 3-wire, ac output with an angle linearly proportional to a dc signal. It provides a 0.5-VA power output, requiring ±15 V dc at 100 mA for full load, together with a 26-V, 400-Hz reference voltage. Specs include an accuracy of 15 min of arc, full-range dc inputs of ±10 V for a transfer function of ±18°/V and a tracking accuracy of 720°/s. The size is 3.925 × 2.9 × 0.7 in.

CIRCLE NO. 340

High-speed light sensor mates with fiber optics

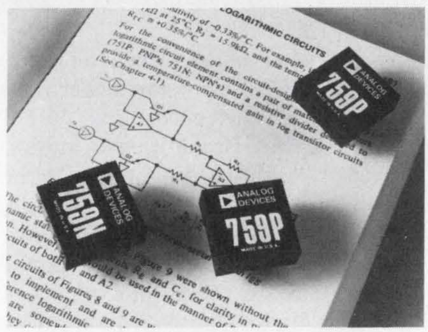


Aborn Electronics, 1928C Old Middlefield Rd., Mountain View, CA 94043. (415) 967-6350. $35 (100 qty).

The APX-200 high-speed p-i-n silicon photodiode has an integral 25-cm fiber-optic pigtail for high optical efficiency and easy interface to cables and electronics. The rise time is 1 ns and the sensitivity is 0.3 μA/μW. The attached cable is DuPont type PFX-P140R with a single 0.4-mm plastic fiber in a reinforced jacket.

CIRCLE NO. 341

Log amps provide 1% conformance



Analog Devices, P.O. Box 280, Norwood, MA 02062. Alan Haun (617) 329-4700. $22 (100 qty); stock.

A pair of log/antilog amplifiers that provide conformance accuracy of 1% to ideal-log operation over four decades of current logging have a 200-kHz bandwidth. The Models 759N and 759P are housed in a 1.125 × 1.125 × 0.4-in. package that includes a complete dc logarithmic amplifier with internal-reference current of 10 μA and pin-selectable scale factors of K = 2, 1, or 2/3 V per decade. The amplifiers offer six decades of current logging from 1 nA to 1 mA and four decades of voltage logging from 1 mV to 10 V. The accuracy of 1% is provided from 20 nA to 200 μA. A 2% accuracy is obtained from 10 nA to 1 mA. The 759N computes the log of positive signals while the 759P computes the log of negative signals.

CIRCLE NO. 342

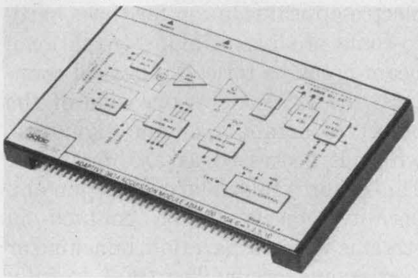
Crystal osc drives TTL from 32 to 65 kHz

Conner-Winfield, West Chicago, IL 60185. (312) 231-5270. $55; 5 wks.

The low-profile hermetically sealed DIP crystal oscillator Model S14R4H4 drives CMOS or one TTL load at any fixed frequency from 32 to 65 kHz. Frequency stability is ±0.02% from −25 to 71 C. Frequency accuracy is ±0.005% at 25 C. The pins plug into a 14-pin IC socket and the size is 0.2 × 0.49 × 0.875 in.

CIRCLE NO. 343

Data-acquisition module employs 12-bit a/d



ADAC, 15 Cummings Park, Woburn, MA 01801. (617) 935-6668. $595; 4 wks.

The Adam 100 data-acquisition module is a 12-bit a/d with 100-kHz throughput rate and an accuracy of ±0.025% of full scale. The module is contained in a 3 × 4 × 0.375-in. metal can that provides electrostatic and electromagnetic shielding on six sides. The unit contains a high-speed sample and hold plus 16 channels of multiplexer inputs that are jumper selectable at the pin-outs for single-ended, pseudo-differential or eight fully-differential inputs. Jumper selections of full-scale ranges are available at the connector pin-outs. Also included are three-state outputs for data transfer to bus-oriented systems.

CIRCLE NO. 344

Amplifier provides 3-kV rms isolation

Intronics, 57 Chapel St., Newton, MA 02158. (617) 332-7350. $89 (100 qty); 4 to 6 wks.

The Model IA175 isolation amplifier is optimized for 12-bit data-acquisition systems that require up to 3-kV rms of isolation. The linearity is ±0.005%. The amplifier has common-mode rejection of at least 120 dB with 5-kΩ source imbalance, input noise of 1 μV from 10 Hz to 1 kHz and a drift of ±0.01%/°C maximum.

CIRCLE NO. 345

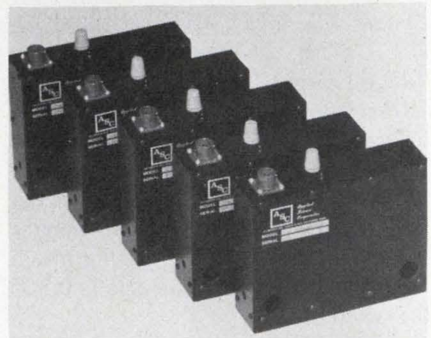
A/d converts in 2 μs with 12-bit accuracy

Dynamic Measurements, 6 Lowell Ave., Winchester, MA 01890. (617) 729-7870. $230 to $300.

The 2813 family of analog to digital converters permits throughput rates of 1.33 MHz (8-bit models), 1 MHz (10-bit models) and 0.5 MHz (12-bit models). Twelve-bit models with 0.4 and 0.25-MHz rates are also available. Maximum linearity is ±1/2 LSB and the nonlinearity tempco is below ±10 ppm/°C. Noise is limited to under 0.2 LSB at the major transitions. The units are RFI/EMI shielded on five sides and measure 2 × 4 × 0.4 in.

CIRCLE NO. 346

Optical counter handles hard-to-count items

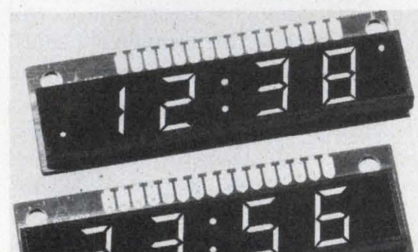


Applied Science, 412 Martin Ave., Santa Clara, CA 95050. (408) 243-3833. From $1200.

The OC-1 optical counter offers an electro-optical solution for those hard-to-count products. Unlike conventional beam-break or reflective optical counters, the OC-1 views one side of the object to obtain a unique signature, which is processed as a count pulse. This ensures false-alarm rejection and permits objects to be counted in streams where separation, bunching or overlapping occur. The OC-1 is fully self-contained and may be located out of immediate proximity to the stream.

CIRCLE NO. 347

Digital-clock displays indicate other variables



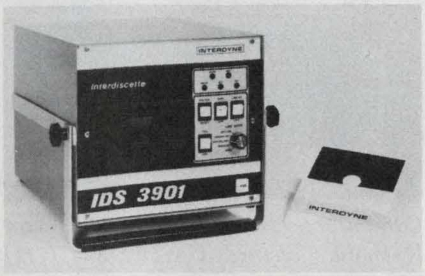
Litronix, 19000 Homestead Rd., Cupertino, CA 95014. Jim Futer (408) 257-7910. $3.05 to $4.45; stock to 12 wks.

The DL-4507 LED clock display may be used as a 24-h display, or as a 12-h display with AM/PM indicator and as a general-purpose digital display. With suitable switching, it may indicate several variables such as time, temperature or rpm as commanded. Functioning as a clock, the unit displays a colon and an alarm-on indication. The display, with 0.5-in. high digits, mounts on a PC board with edge connectors. The standard module has red or green digits. On special order, yellow or high-brightness red digits are available.

CIRCLE NO. 348

DATA PROCESSING

Serial mini floppy buffers data terminal

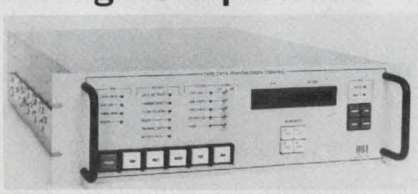


Interdyne, 14761 Califa St., Van Nuys, CA 91411. Bill Geist (213) 787-6800. $2050; 4 wks.

A fast-access intelligent buffered data terminal, the Model IDS 3901, uses a 5.25-in. standard diskette drive and is RS-232C compatible. Average access time is 0.6 s. The terminal has an editable data buffer holding up to 128 characters, and allows insertion of blocks or entire paragraphs. The unit is controlled by 30 ASCII commands and outputs 13 plain-English messages. Other features include storage of 143 kbytes (formatted) per diskette, switch-selectable asynchronous rates from 110 to 19,200 baud as well as transparent binary modes and auto error check.

CIRCLE NO. 349

Taped-data transmitters use high-level protocols

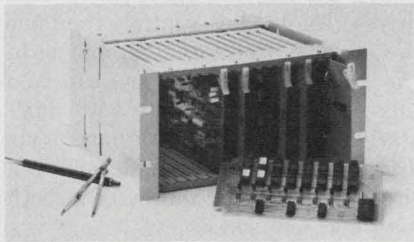


Quad Systems, 11900 Parklawn Dr., Rockville, MD 20852. (301) 770-6788.

The Model 7300, for transmission of IBM-format digital magnetic-tape data, has adopted high-level line protocols. The use of error-protected Bi-Sync or SDLC formats enable increased throughput efficiencies at rates to 56.2 kbits/s. Several levels of data-base protection are available from simple character parity to selected repeat ARQ. Error checking is provided on either a character or block basis. Error protection methods and line protocols are selected to match terminal and transmission characteristics. A built-in self-test function is provided.

CIRCLE NO. 350

Voice readout system is solid-state



Master Specialties, 1640 Monrovia, Costa Mesa, CA 92627. Ken Renaud (714) 642-2427.

At the heart of the modular voice-readout system, Model 1650, is the word storage base made up of ICs. PROMs allow custom programming of specified words into the system which outputs a distinct male voice. The system accommodates 10 plug-in circuit boards for a vocabulary of 160 words in a standard ATR rack. Each circuit board expands the vocabulary.

CIRCLE NO. 356

DATA PROCESSING

Tape-drive formatter links four transports

Tandberg Data, 4060 Morena Blvd., San Diego, CA 92117. Pete Gilbody (714) 270-3990.

With the TDF 4050 tape formatter, users may daisy-chain up to four transports simultaneously. The formatter enables the generation and reading of ANSI, IBM and ECMA-compatible tapes. It works with 9-track 1600-bit/in. PE and 800-bit/in. NRZI tape drives. The module controls from one to four tape transports that may be of the same or half speed and can be a mix of different formats with dual-stack heads. The TDF 4050 handles six different tape-drive speeds and can read and write PE and NRZI at both high and low speeds.

CIRCLE NO. 357

Minicomputer system has versatile software

Computer Automation, 18651 Von Karman, Irvine, CA 92713. (714) 833-8830. $9750 to $11,000 (100 qty).

Basic Desk is a packaged hardware/software system tailored to OEM customers or the high-volume buyer who adds specific application software and resells to end-users. The system is configurable from a minimum single-terminal, dual floppy-disc system to a four-terminal version supporting multiple-floppy and 10-Mbyte discs, line printer and other peripherals. System software, developed around BASIC, is oriented to multi-user environments. Hardware includes a 16-bit minicomputer with 32 kwords of memory, two floppy-diskette drives, a CRT terminal and additional support through a distributed I/O system.

CIRCLE NO. 358

Unit allows 4 terminals to share a modem

Tele-Dynamics, 525 Virginia Dr., Fort Washington, PA 19034. (215) 643-3900.

Model 7251, a modem sharing device, permits four separate data terminals to communicate through a single modem on a shared basis. The four terminals and the single modem connect to the 7251 through RS-232C interfaces and the selector sequentially monitors the request-to-send lines. When a request-to-send signal is received from any terminal, the 7251 automatically selects the appropriate port to connect that terminal to the modem. A front-panel switch is provided to unconditionally connect one of the terminals to the modem by selecting port number 1 and bypassing the other three ports.

CIRCLE NO. 359

Cassette recorder stores 6 hours of analog data

Paradigm, Baxter Springs, KS 66713. (316) 856-2133. $500 to $865; 4 to 6 wks.

The Model 248 LTR provides 6 hours continuous recording on a C-90 Philips-type cassette tape. The tape speed of 15/16 in/s allows electronic switching of one channel sequentially through tracks 1 to 4. A visual indication of track status and record ready is provided. An audible alarm signals at the end of track 4 when the tape needs to be changed. A high-level input operates from phone lines, two-way radio or preamp output. Three operating modes include VOX, offhook or continuous recording.

CIRCLE NO. 360

Paper-tape terminal runs at 300 baud

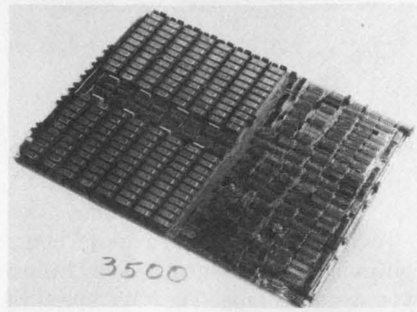
Drillick LaManna, 280 Midland Ave., Saddle Brook, NJ 07662. (201) 791-1414.

The Model DLC 3000 paper-tape punch reader operates with 300-baud printers and visual display units. The unit connects to other equipment via an RS-232C interface to provide an automatic send-receive (ASR) capability. The terminal also stands alone to send and receive data and to punch and duplicate tape. Standard switch settings include half or full duplex, 110 or 300 baud and remote control of reader and punch.

CIRCLE NO. 361

DATA PROCESSING

128-k memory card offers multiple options

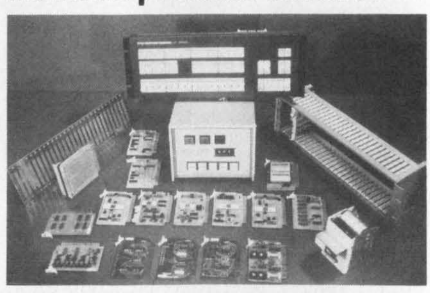


EMM Commercial Memory Products, 12621 Chadron Ave., Hawthorne, CA 91250. (213) 644-9881. $4995; 13 wks.

The variety of options offered on the Microram 3500 single-card 128 k × 22 semiconductor memory system includes ECC (single-bit error correction and multiple-bit error detection) and word or byte parity generation and checking. The card is also available with page mode, byte mode, error stop and a fault location LED display which operates in conjunction with the ECC option. Provisions have been made for battery backup. When operated in the page mode, the system automatically detects page boundaries. In page mode with a match condition, a cycle time of 270 ns is achievable. A no-match condition yields a 450-ns cycle time. Non-page-mode cycles are completed within 400 ns.

CIRCLE NO. 362

Output module handles process control



Wyle Lab, 3200 Magruder Blvd., Hampton, VA 23666. (804) 838-0122. $345.

The PCO-1A process control output module provides two complete 4 to 20-mA or 10 to 50-mA output circuits in one module. The current range is independently selectable for each circuit, and both outputs are short-circuit protected.

CIRCLE NO. 363

Acoustic coupler has crystal control

Datec, P.O. Box 839, Chapel Hill, NC 27514. Ida Plymale (919) 549-8945. $395; 4 to 8 wks.

Both transmitter and receiver of the Model 32 acoustic coupler use crystal-controlled CMOS digital ICs for accurate and stable FSK frequency generation and discrimination. Interfering transmitter harmonics are notched out by linear-phase active filters. A signal-quality carrier detector eliminates false carrier indication and permits channel establishment with signals as low as −55 dBm. Both RS-232 and 20-mA TTY interfaces are provided. Simultaneous operation of two data terminals is possible with a terminal splitter attachment.

CIRCLE NO. 364

Limited-distance modem has thorough diagnostics

Tele-Dynamics, 525 Virginia Dr., Fort Washington, PA 19034. (215) 543-3900. $695.

A limited-distance modem, the Model 7300, features comprehensive diagnostic capabilities for both system and self-test. The modem provides full or half-duplex operation over 4-wire lines or simplex operation over 2-wire lines at data rates from 1800 to 19,200 bits/s. The diagnostic features include analog and digitial loopback, command loopback and a built-in test-pattern generator. Over-all performance is monitored by six LEDs. A typical range is 17 m at 2400 bits/s using No. 22 wire. At 19,200 bits/s, the range is 7 m.

CIRCLE NO. 365

Optical character reader handles typewriter font

Dest Data, 1285 Forgewood Ave., Sunnyvale, CA 94086. Derek Jones (408) 734-1234. $55,000; 12 to 14 wks.

An addition to the OCR/WORD line of optical character readers (OCR) handles the Prestige Elite typewriter font, including underlined words and phrases and provides an output signal denoting the location of the underlines. A basic unit with this capability accepts input from the normal 12-pitch typewriter. Without re-keying, the typewritten material may be entered into most word processing systems for editing, storage and processing.

CIRCLE NO. 366

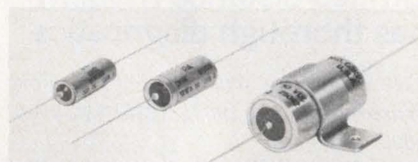
Thick-film resistors formed as chips

Assembly Specialists, P.O. Box 965, Acton, MA 01720. (617) 263-9100. Stock to 2 wks.

A line of thick-film resistor chips with leads have values from 10 Ω to 25 MΩ with specified tolerances of 1 to 25%. The chip size is 0.2 × 0.2 × 0.025 or 0.3 × 0.3 × 0.025 in. with lead spacings on 0.1, 0.125 or 0.15-in. centers. The chips have less than 5 μV/V noise and a controlled tempco of less than 50 ppm, if required.

CIRCLE NO. 367

Capacitors retain charge for 150 hours



Industrial Condenser, 3243 N. California Ave., Chicago, IL 60618. (312) 463-2200.

The miniaturized and metallized Synthar Type TSZ long-time-constant capacitors retain 99% of their charge for 150 hours. The capacitors have ratings from 0.005 to 50 μF, operating temperatures from −55 to 125 C, voltage ratings of 50 to 600 V and insulation resistance of 2.8 × 10^5 MΩ-μF.

CIRCLE NO. 368

Rotary switch sports high dielectric strength

Janco, 3111 Winona Ave., Burbank, CA 91504. (213) 845-7473.

The Type 1900 HD rotary switch has high dielectric strength and a diameter of 1 in. Special treatment is given to all ground metal parts, metal parts are substituted with nylon and normally low-strength creepage-path areas are safeguarded. The result is a switch with a 3.5-kV rms dielectric strength between current-carrying members and ground. The switch is available in 2 to 12 positions with detent angles of 30, 36 and 45 degrees and a maximum number of 12 poles. The environmental requirements of MIL-S-3786 are met.

CIRCLE NO. 369

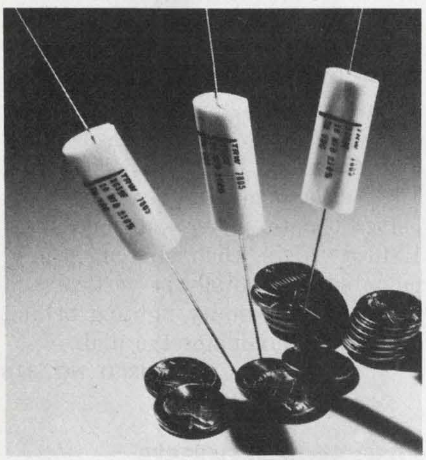
Mini power transformer mounts on PC boards

Abbott Transistor Labs, 639 S. Glenwood Pl., Burbank, CA 91506. Wayne Lovett (213) 841-3630. $5.90; stock.

A miniature low-profile power transformer, the 6LP8-3, mounts on PC boards and supplies 8 V ac at 0.4 A or 16 V ac center-tapped at 0.2 A for 3.25 W. Output voltage tolerance is within 5% when measured at full load and 115 V ac input. Voltage regulation is 20% no-load to full-load and insulation test voltage is 1000 V ac. The height of the transformer is 1.17 in.

CIRCLE NO. 370

Metallized capacitors boast small size

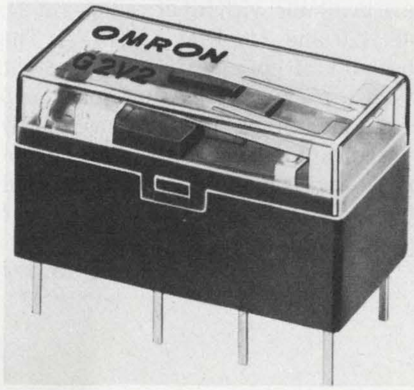


TRW Capacitors, 301 West O St., Ogallala, NE 69153. (308) 284-3611. See text; 12 wks.

Described as the smallest possible size in a metallized-polyester capacitor, the Type X659F ranges in size from 0.125 × 0.23 × 0.438 for 0.47 μF to 0.43 × 0.79 × 1.5 in. for 20 μF at 50 V. Capacitance values from 0.01 to 20 μF are available at from 50 to 500 V dc. The capacitors have axial leads and the dissipation factor is less than 1% when measured at 1000 Hz. The operating temperature range is −55 to 100 C or to 125 C with 50% derating. Price is $0.40 for a 0.1 μF, 100 V dc device in production quantities.

CIRCLE NO. 371

Mini relays packed in DIP mounts



Omron Electronics, 233 S. Wacker Dr., Chicago, IL 60606. Don Nelson (312) 876-0800. $1.78 (1000 qty).

Series G2V relays feature low-profile packaging with above-board dimensions of 0.433 high × 0.413 × 0.827 in. A DIP-terminal layout is compatible with standard 0.1-in. grid PC-board mounting. The case construction is resistant to flux wicking and allows for automatic dip or wave soldering. Bifurcated cross-bar contacts provide switching from signal level (1 mA) up to 2 A, with 6-ms operate and 3-ms release. Five models offer coil ratings of 3 to 24 V dc and provide 2-pole Form C contacts.

CIRCLE NO. 372

Solid-state keyboard has no contacts

Cherry Electrical Products, 3600 Sunset Ave., Waukegan, IL 60085. Frank Amendola (312) 689-7600.

The Cherry solid-state capacitive keyboard has low-profile keys with no contacts. The integrated keyboard encoder requires only a +5-V supply. It encodes up to 10 bits for 110 keys and four modes per key. Codes are designed in and via a low-cost mask option any code can be selected. Scan time is adjustable from 10 to 80 μs per key. A noise-immunity circuit is included to distinguish good keys from noise and a key recognition circuit eliminates teasing of keys. Burst-rate capability is 1000 char/s.

CIRCLE NO. 373

Memory relay holds during power failure

Master Electronic Controls, P.O. Box 25662, Los Angeles, CA 90025. Bill Tooker (213) 393-3177.

The MR memory relay maintains circuit integrity under normal or abnormal conditions such as fluctuating voltage, complete power outage or other control system failure. The relays are available with input voltages of 24, 48, 120 and 240 V ac at 1.2 VA. The output is an optically isolated triac that turns an external load on or off at 5 A ac maximum. The unit has a LED to indicate reset condition. The memory feature is maintained by an internal battery that is activated only in event of power failure.

CIRCLE NO. 374

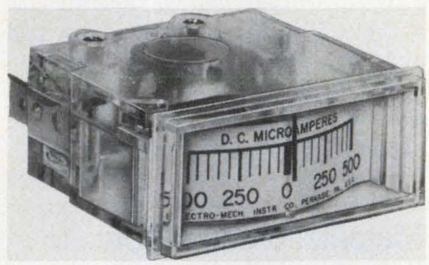
Electrolytic capacitors boast of low leakage

Nichicon, 6435 N. Proesel Ave., Chicago, IL 60645. (312) 679-6530.

These radial-lead low-leakage capacitors can replace expensive tantalum and Mylar-film capacitors without sacrificing performance characteristics. The LL series of miniature aluminum electrolytics has reduced leakage levels to a maximum of 0.002 CV or 0.4 μA, whichever is greater. Units are available in a range of 0.1 through 100 μF. The operating temperature range is −40 to 85 C.

CIRCLE NO. 375

Edge-reading meters have flat faces



EMICO, P.O. Box 368, Dublin, PA 18917. (215) 249-9330.

The flat-face edge-reading meter, Model 13-F, is available as a dc or ac ammeter, voltmeter or milliammeter in a wide variety of ranges. Depending upon the range, its accuracy is 3 or 5%. The clear molded-polystyrene or polycarbonate meter case measures 1.813 × 0.75 in. The meter can be clip-mounted horizontally or vertically in the panel. Proximity lighting behind the panel illuminates the dial.

CIRCLE NO. 376

Disc switch boasts 10-million operations

ITT Schadow, 8081 Wallace Rd., Eden Prairie, MN 55344. (612) 944-1820.

Totally sealed disc switches can be operated more than 10-million times without failure. Pressure on the switch's upper dome collapses! it momentarily, making instant positive three-point contact with the lower diaphragm. Features include self-cleaning, a broad range of switching power from a few milliwatts to 30 W with low bounce (less than 10 μs) and an option to mount the disc element on a PC board, either alone or associated with pushbuttons.

CIRCLE NO. 377

Luminescent panel backlights LCD

Liquid Xtal Displays, 24500 Highpoint Rd., Cleveland, OH 44122. Hugh Mailer (216) 831-8100.

Electroluminescent panels provide illumination for night-time viewing of an LCD. With an inverter, the panels provide 100-h continuous operation when powered with two AA alkaline batteries. The panel adds less than 0.03 in. to the thickness of the LCD.

CIRCLE NO. 378

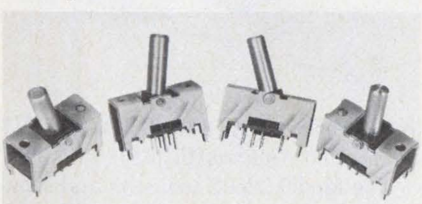
Air capacitors mount vertically on PC boards

Johanson Mfg., 400 Rockaway Valley Rd., Boonton, NJ 07005. Eric Fogerlund (201) 334-2676. $1.80 to $4.00; stock to 3 wks.

Vertical-mount trimmer capacitors can be adjusted after the PC board has been assembled. These air-dielectric types offer space-saving advantages over horizontally mounted units and still allow boards to be mounted on 0.5-in. centers. The trimmers are available in capacitance ranges from 1 to 8 pF to 1.5 to 30 pF with a variety of Q values, as high as 5000.

CIRCLE NO. 379

Mini toggle switch has polished look



UID Electronics, 4105 Pembroke Rd., Hollywood, FL 33021. (305) 981-1211. From $0.35.

For that polished look, try this PC-mounting mini toggle switch with a brushed-aluminum actuator. The switch is rated at 0.5 A, 120 V ac, 10,000 cycles. Dual-wipe contacts increase contacting area to provide reliability.

CIRCLE NO. 380

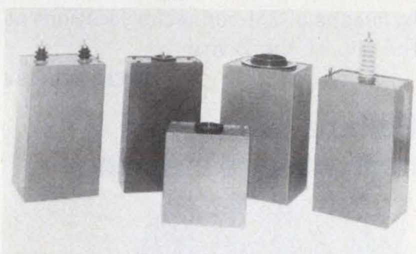
Relay accepts immersion in PC-board cleaners

Potter & Brumfield, 200 Richland Creek Dr., Princeton, IN 47671. Roy Stuart (812) 386-1000. From $2.43; stock.

A UL-recognized, immersion-cleanable PC-board relay, T10, is rated to 3 A. The relay accepts full immersion in PC-board cleaning solvents for up to two minutes. The part is available in 1 and 2-A, 28-V dc or 120-V ac, DPDT, 4PDT and 6PDT models. The 1-A models have bifurcated contacts for low-level switching. Standard coil voltage ratings of all models are 5, 6, 12, 24 and 48 V dc. The relays seat 0.425 in. high, allowing PC boards to be mounted on centers of 0.6 in.

CIRCLE NO. 381

High-voltage capacitors store energy



Capacitor Specialists, P.O. Box 2052, Escondido, CA 92025. (714) 747-4000. $0.08 to $0.11/joule.

Using a dielectric system of film, paper and nonflammable, non-PCB oil, the Series ES energy-storage capacitors offer 127 models in five bushing styles. Voltage ratings from 3 to 125 kV are available with current ratings to 250 kA. The operating temperature range is −35 to 70 C. Low losses allow operation at up to 100 pulses/s.

CIRCLE NO. 382

Film-dielectric cap has zero tempco

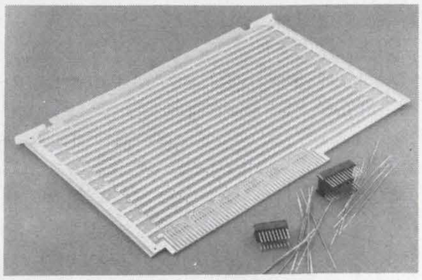
American Radionic, 51 Austin St., Danbury, CT 06810. Dick Stockman (203) 743-6308.

Zerocap film-dielectric capacitors offer the special characteristics of low dielectric absorption, high insulation resistance and a zero tempco from 0 to 70 C. The capacitors are available in a wide range of tolerances in values from 0.01 to 1 μF. A typical capacitor such as a 0.1 μF at 100 V is 0.9 in. long by 0.425-in. diameter.

CIRCLE NO. 383

PACKAGING & MATERIALS

Wrapped-wire board goes into TI μCs

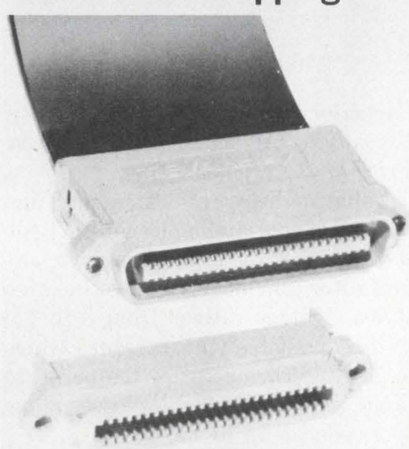


Technical Micro Systems, 17935 Sky Park Circle, Irvine, CA 92714. Paul Cloud (714) 549-3991. $65; stock.

A wrapped-wire board, Model WWB, holds 63, 14-to-20-pin ICs and mates with TI's TM 990/100M microcomputer. Dedicated power, ground and decoupling are provided for the 20-pin ICs. Connections to the 100-pin card-edge fingers are made at wrapped-wire sockets. Additional I/Os are provided by means of 3M-connector locations at the top of the board.

CIRCLE NO. 384

Ribbon connectors need no wire stripping

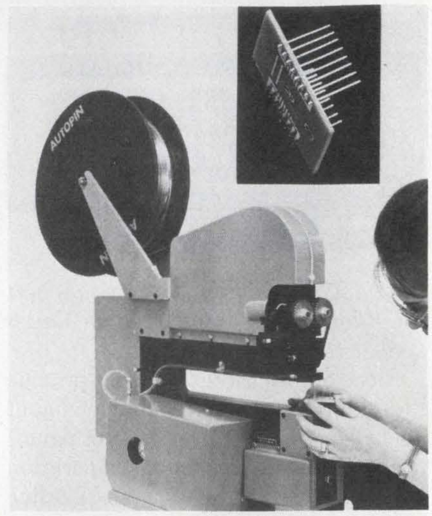


T&B/Ansley, 3208 Humbolt St., Los Angeles, CA 90031. (213) 223-2331. $0.06/contact.

Blue Macs ribbon connectors can be mass-terminated in seconds to standard 50-mil-pitch flat cable without wire stripping or soldering. The one-piece design features self-aligning cable grooves that automatically position each conductor over the contacts. To install, the cable is positioned in the connector opening and crimped with hand or bench installation tools. Up to 50 conductors can be simultaneously mass-terminated. The series includes male and female connectors in 14, 24, 36 and 50-contact versions.

CIRCLE NO. 385

Machine inserts pins at rate of 2500/h



Autosplice, 220 E. 23 St., New York, NY 10010. (212) 674-4369.

With the Autopin pin-terminal insertion system an operator can insert from 1500 to 2500 pins/h. The system includes an applicator machine and a coil of round or square wire. In a typical operation, the operator positions a PC board, coil or bobbin and trips the machine. The equipment feeds a length of wire, cuts it and inserts it in one operation. The pin length is adjustable to 1.125 in. and the machine can be set for different board thicknesses. The end of the pin terminal can be square cut, tapered or concave.

CIRCLE NO. 386

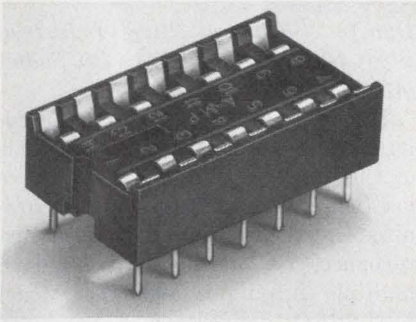
Tool slits and separates flat cable

K-G Devices, P.O. Box 81, Dewitt, NY 13214. Art Goldsmith (315) 683-5666.

The Model 2250S tool slits and separates all types of flat ribbon cable with all types of plastic film. The tool jaws cut through the film between the wires in one operation for up to 3 in. Wires as small as AWG 30, and even mixed wire sizes in the same cable, can be slit in widths up to 2.5 in. Custom variations are available for unlimited slitting lengths. The tool may be bench mounted or hand held.

CIRCLE NO. 387

DIP sockets are machine insertable

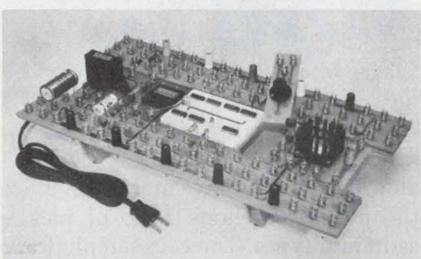


AMP, Harrisburg, PA 17105. Jim Pletcher (717) 564-0100.

Designed for socket-to-board and DIP-to-socket automatic machine insertion, Diplomate low-profile DIP sockets have a large target area and wide-contact side ramps for easier insertion. During insertion, the DIP leads do not scrape the plastic housing. The polyester housings have a closed bottom to prevent solder wicking and flux contamination of the contact area. An anti-overstress wall protects contacts from damage by oversize or bent DIP leads.

CIRCLE NO. 388

Breadboard allows solderless wiring



Multi-Tronix, 3210 Terry Dr., Toledo, OH 43613. (419) 472-0723. See text; stock to 4 wks.

Series 2000 Hybridboards are solderless mediums for circuit hook-ups. PC modules provide the sockets, switches and potentiometers to be used together with standard off-the-shelf components. The modules are locked in place between the panels of the board by means of spring-loaded sliding fingers. The resulting assembly connects to external equipment through 10 color-keyed binding posts. High-density socket modules accommodate ICs and allow interfacing with discrete components and power devices. Replaceable coil-spring solderless connectors, having a current rating of 15 A and accepting up to 16-AWG wire, are provided. The board is priced at $75 and modules sell for $2 to $90.

CIRCLE NO. 389

Work station handles static-sensitive parts

Static, P.O. Box 414, Lee, MA 01238. (413) 243-0455.

The Microautostat grounding and ionizing work station consists of a copperclad, nickel-plated, laminated work surface, connected to a power unit by a shielded cable. The station provides reliable protection from static charges for sensitive devices such as MOSFETs during assembly, without the use of conductive plastic bench tops, aprons and ionizing blowers. The work surface is a PC board into which are imbedded 18 shockproof ionizing points. Air ionized by the points neutralizes static electricity in the work zone, and the grounded nickel-plated surface ensures a path to ground.

CIRCLE NO. 390

Solder extraction unit converts air to vacuum

Pace, 9329 Fraser St., Silver Spring, MD 20910. Al Rosenthal (301) 587-1696. $325.

The Model SX-214 Ped-A-Vac II solder-extraction system turns any work station into a power desoldering/soldering center. All that is required is an air supply of from 60 to 80 psi. The system quickly removes components from any circuit board and doesn't generate electrical spikes. It can be used safely with all MOS devices. Using a foot-controlled, floor-mounted vacuum generator, the system converts shop air into a high-flow-rate vacuum for desoldering use. The handpiece uses a heat control that automatically reduces tip temperature during vacuuming operations to protect the pad area. A temperature controlled soldering iron also is provided.

CIRCLE NO. 391

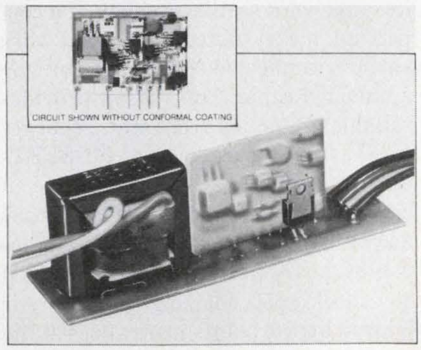
Lead cutter and former feature adjustable head

Wybar Electronics, P.O. Box 109, Syracuse, NY 13201. (315) 454-3237.

An automatic lead cutter and former, Model BE-100, includes a fully adjustable head. The machine adjusts with a single control to take components up to 2 W in size. It produces up to 18,000 components per hour. The BE-100 cuts and forms right angles from taped components. It is also available with a rapid-feed manual-load method for loose components.

CIRCLE NO. 392

Charger operates in emergency power systems

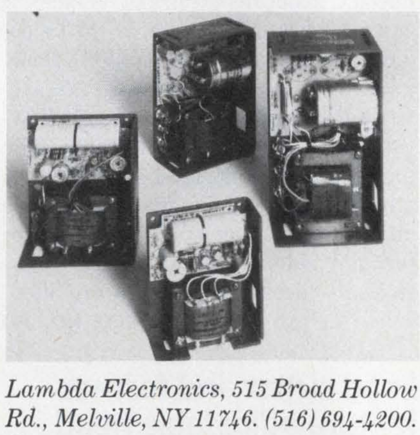


Centralab Electronics, 5757 N. Green Bay Ave., Milwaukee, WI 53201. (414) 228-2874. $9.00 (1000 qty).

The Emergency Power Battery Charger maintains a full charge on standby 6 or 12-V batteries. The charge is maintained by the float-voltage method. The thick-film circuit module senses power-line failures and switches the battery output on when power line fails. On restoration of power the charger switches back to the charging mode and regulates the charging current. The charging current is 250 mA.

CIRCLE NO. 393

Open frame supplies come in 56 models



Lambda Electronics, 515 Broad Hollow Rd., Melville, NY 11746. (516) 694-4200. From $27.

The LO series of open-frame power supplies for OEM users contains 56 models in six package sizes with single, dual and triple outputs up to 28 V dc and currents up to 25 A. Line and load regulation is 0.15% with a ripple of 1.5 mV rms. Features of the series include fold-back current limiting and no overshoot on turn-on, turn-off or power failure. All models are convection cooled and have a tempco of 0.03%. Ambient operating range is 0 to 60 C.

CIRCLE NO. 394

Switcher supply powers CRT terminals

Dynetic Systems, 19128 Industrial Blvd., Elk River, MN 55330. Bill Sadler (612) 441-4300.

The SPU series of switching-regulated power supplies matches the needs of CRT terminals. The supplies have low field leakage and optional synchronized input for minimal video disturbance. A wide range of voltages in multiple outputs is available. Model SPU-5-15/15 delivers +5, +15 and −15 V dc at 200 W. Remote sensing on all outputs provides 0.1% regulation from no load to full load with ripple and noise less than 50 mV pk-pk on all outputs. Electrical and thermal protection is provided for short, overload and overvoltage conditions.

CIRCLE NO. 395

Silver-zinc rechargeable cells pack more power

Saljac Enterprises, P.O. Box 5337, Beverly Hills, CA 90210. (213) 278-8714.

Medicharge silver-zinc, rechargeable, button cells have more than twice the power-to-volume ratio of nickel-cadmium types. The cells supply 1.5 V against the NiCd's 1.2 V and offer 25% better voltage stability throughout the discharge cycle. Batteries can be charged and discharged many times and they operate at 95% efficiency, thereby also providing a longer-charged shelf life.

CIRCLE NO. 396

UPS comes in ratings up to 83 kVA

Cyberex, 7171 Industrial Park Blvd., Mentor, OH 44060. (216) 946-1783.

Uninterruptible power systems (UPS) now have single-phase ratings up to 83 kVA. Typical output characteristics are ±10% transient-voltage response for 100% load change, ±1% voltage stability, ±0.5% frequency stability and less than 5% harmonic distortion with no low-order harmonics.

CIRCLE NO. 397

Application notes

Custom ICs

"How Cost Effective are Custom ICs?" looks at the relative economies of discrete-circuit designs versus semicustom IC designs at various volume levels. Interdesign, Sunnyvale, CA

CIRCLE NO. 398

Temp-resistance applications

The temperature-resistance characteristics of the TSP102 PTC silicon thermistor is explained in a 22-page report. Texas Instruments, Dallas, TX

CIRCLE NO. 399

Solder creams

An eight-page handbook on solder creams covers the use of these metal-joining materials for electrical, electronic, and mechanical assemblies. Tables, curves, photographs and drawings are included. Alpha Metals, Jersey City, NJ

CIRCLE NO. 403

Digital clocks

How to interface digital clocks directly to the communications port of a computer, CRT terminal, teleprinter, or other recording device is described in a new data sheet. Chrono-Log, Havertown, PA

CIRCLE NO. 404

Ac-line noise suppression

The protection of sensitive electronic equipment from the problems created by ac-line noise, transients and spikes is covered in a manual. Topaz Electronics, San Diego, CA

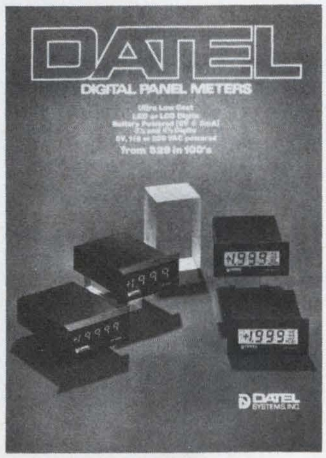
CIRCLE NO. 405

Spectrum analyzers

How the peak memory capability of today's spectrum analyzers can simplify the procedures for calibrating impulse generators used in RFI measuring equipment is covered in a six-page brochure. Marconi Instruments, Northvale, NJ

CIRCLE NO. 406

New literature



Digital panel meters

A 20-page brochure features low-cost 3 1/2 and 4 1/2 digit DPMs, Models DM3100 and 4100. The brochure details electrical and physical parameters, applications, block diagrams and ordering information. Datel Systems, Canton, MA

CIRCLE NO. 407

16,384-bit dynamic RAM

A 14-page catalog includes a description, features, waveforms and electrical characteristics of the 4116 16,384-bit dynamic RAM. ITT Semiconductors, Dallas, TX

CIRCLE NO. 408

μC system

An 8-page TRS-80 microcomputer-system-products catalog provides information on upgraded systems, peripherals and ready-to-use software developed specifically for the system. Radio Shack, Fort Worth, TX

CIRCLE NO. 409

Plug, socket connectors

A 24-page catalog on plug and socket connectors includes complete specifications, connector dimensions and suggested panel-mounting dimensions, supported with photographs and dimension drawings of all connector types. A variety of cable-mounting hardware is described and illustrated. Beau Products Div., Vernitron Corp., Laconia, NH

CIRCLE NO. 410

Transmitters, converters

Pressure transmitters, P-I/P-E converters are covered in an eight-page catalog. Photos, block diagrams, electrical and mechanical specifications are included. Kulite Semiconductors, Ridgefield, NJ

CIRCLE NO. 411

Switchers

Switching power supplies are highlighted in an eight-page brochure. Construction details and circuit descriptions are provided. Kepco, Inc., Flushing NY

CIRCLE NO. 412

Frequency counters

Multifunction counters to 520 MHz are featured in a six-page foldout. A counter-selection guide gives information on all of the company's counters. John Fluke Manufacturing, Mountlake Terrace, WA

CIRCLE NO. 413

Rf attenuators

A 112-page catalog features rf attenuators and other coaxial components. Specifications and outline drawings are given. Also included are decibel-conversion tables, a glossary of transmission-line terms and a list of reference literature. Weinschel Engineering, Gaithersburg, MD

CIRCLE NO. 414

Test instruments

Specifications and technical information on more than 55 products, including oscilloscopes; digital VOMs; frequency counters, rf, audio, pulse, function, and color-bar generators; power supplies; probes; testers; and test-instrument accessories are provided in a 44-page catalog. VIZ Test Instruments, Philadelphia, PA

CIRCLE NO. 415

Wrapped-wire panels

Photos, descriptions, specifications, outline drawings and prices of pin-in-board type ALA wrapped-wire panels, cords, drawers and frames are shown in a 28-page brochure. EECO, Santa Ana, CA

CIRCLE NO. 416

Crystals

Performance specifications of cold-weld, general-purpose and high-stability crystals are included in a 12-page booklet. Outline drawings are included. Bliley Electric, Erie, PA

CIRCLE NO. 417

Semiconductor products

Specifications and technical data on current-regulator diodes, varactor diodes, FETs, switching and chopping transistors, grown-junction replacement transistors, hybrid analog gates and d/a-ladder switches are given in a short-form catalog. Teledyne Crystalonics, Cambridge, MA

CIRCLE NO. 418

Reed relays

Mechanical and electrical characteristics, dimensional drawings and schematics for reed relays are given in a 16-page catalog. Hamlin, Lake Mills, WI

CIRCLE NO. 419

Relays, actuators

Included in a 20-page catalog is a description, ratings, and dimension information for general-purpose, telephone-type relays, actuators and buzzers. Omega Co., div. of Magnecraft, Chicago, IL

CIRCLE NO. 420

Oiltight pushbuttons

A 12-page brochure features oiltight pushbutton controls. Descriptions include an octagonal mounting-ring system, sealed switch-contact blocks, pilot lights and illuminated devices and accessories. Allen-Bradley, Milwaukee, WI

CIRCLE NO. 421

Signal processor

A high-speed, programmable, signal processor (PSP-100), designed for real-time electronic-support and countermeasures systems that deal with dense signal environments, is described in a brochure. The brochure includes a technical description, functional block diagram, I/O capabilities and designs, programming opinions. GTE Sylvania, Mountain View, CA

CIRCLE NO. 422

Bulletin board

Intel's Microcomputer Components Div. has reduced prices 33% on components in the **MCS-80 product** family, most notably the industry-standard 8080A microprocessor.

CIRCLE NO. 423

Chicago Miniature Lamp Works has reduced prices by as much as 40% on popular types of **LEDs.**

CIRCLE NO. 424

Raytheon's Semiconductor Div. has reduced prices 20 to 40% on **standard PROMs and PROMs with built-in power-down capabilities.**

CIRCLE NO. 425

Prices have been reduced 50% on **Signetics adaptable board computer (ABC 1500) kit**—a complete 8-bit microcomputer.

CIRCLE NO. 426

EMM SEMI has announced a price cut on its **3539 2-k static RAMs.** In quantities of 500, the price was cut from $7.80 to $4.05.

CIRCLE NO. 427

Hewlett-Packard has announced an across-the-board reduction of $11,000 in the U.S. price of every model in the **HP 3000 Series of business-computer systems.**

CIRCLE NO. 428

Prices for **EECO's D300 and D400 video display terminals** were reduced approximately 15%.

CIRCLE NO. 429

Honeywell has introduced a family of **30-cps and 120-cps teleprinters** for use with its Series 60 computers. Initial models include the 1001, 1002, 1003 and 1005.

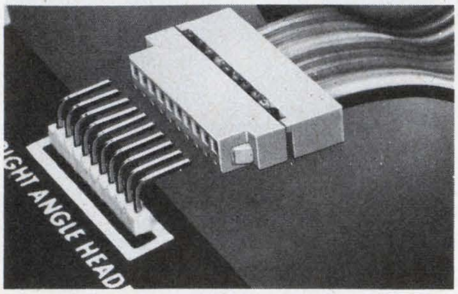
CIRCLE NO. 430

Azurdata slashes **Scorepad-terminal** prices by as much as 35%.

CIRCLE NO. 431

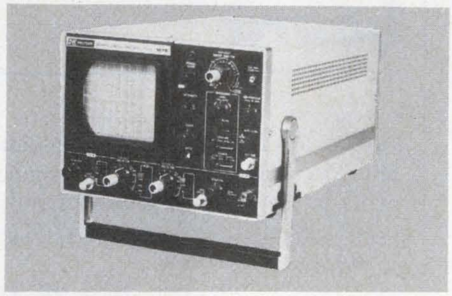
quick ads

New and current products for the electronic designer presented by their manufacturers.



METHODE MASS TERMINATION CONNECTORS FOR CABLE-TO-BOARD RIBBON CABLE ON .100" CENTERS. An industry first, "Jaguar 100" connectors eliminate rejections caused by shorts to adjacent conductors, a major cause for rejects when terminating on .050" centers. 1300-200 Series available in straight-on and right angle versions. 10 to 28 contact positions (22-26 AWG). Tin plated brass contacts. 94V-0 housings. Methode Electronics Inc., 1700 Hicks, Rolling Meadows, IL. 60008 (312) 392-3500.

.100" CENTERS CONNECTORS 181

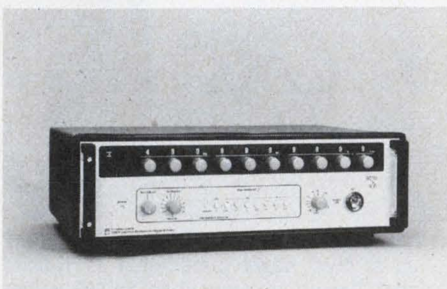


30MHz DUAL TRACE SCOPE with delay line, 5". 30MHz 5" DUAL TRACE TRIGGERED scope, with delay line, only $999 with probes. Rise time under 11.7nS. Triggers up to 50MHz, 5mV/cm vertical sensitivity. 20 calibrated sweeps, internal calibration source, many other features. Immediate delivery from distributor stock. B&K-PRECISION, Dynascan Corp., 6460 Cortland, Chicago IL 60635, 312/889-9087.

DUAL TRACE SCOPE 184

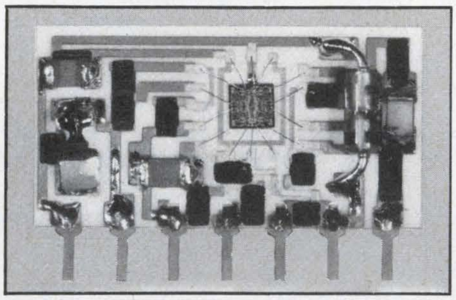
MICROPROCESSOR dc POWER SUPPLY (SMP SERIES). Directly compatible with wide selection of micros, minis, CPUs and peripherals (AMD, Intel, NEC, TI, GI, Fairchild, Harris, Motorola, RCA, Signetics, National, Mostek, Intersil, etc.). Well Regulated. Low Ripple. OV Protection. Over 12 models, 5 Vdc to 18 Vdc. From $27.50. Immediate delivery from over 70 distributors nationwide. Send for specfilled catalog. Standard Power, Incorporated, 1400 South Village Way, Santa Ana, CA 92705. 714/558-8512.

POWER SUPPLY 187



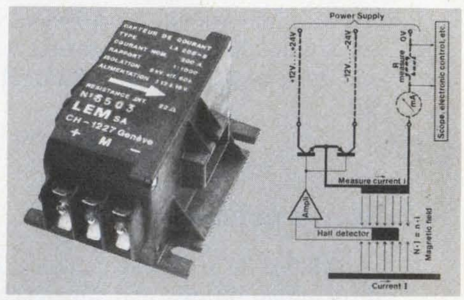
FREQUENCY SYNTHESIZERS. GenRad offers the best combination of low-phase noise, fast switching speed and price. Frequency range is dc to 500 MHz. Important features: non-harmonic spurs > 80 dB down; a-m, fm and pm capabilites; built-in search sweep; programmable (BCD parallel) frequency control; and optional resolution to 0.1 Hz. GenRad, 300 Baker Ave., Concord, MA 01742, (617) 369-8770.

FREQUENCY SYNTHESIZERS 182



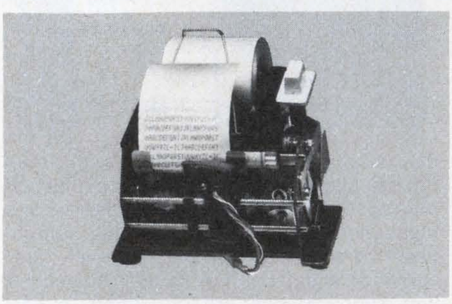
ULTRA SMALL ACTIVE BAND PASS FILTER fabricated using OP Amp incorporated Hybrids Circuit. Operating Voltage 1-2.5V/ 4-15V, Frequency Range 288.5-2800Hz, Q 180+20, 35+5 and etc. .788" × .138" × .433". By adding Feed Back Circuit of extra Diode and Capacitor, it does the job of small but reliable Oscillator. Active Filters can be tailor-made to customer's specifications. IWATA ELECTRIC CO., LTD. Mansei Bldg., 1-1-16 Sotokanda, Chiyoda-ku, Tokyo, Japan.

ACTIVE FILTER 185



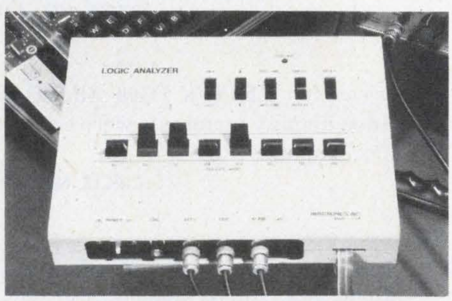
Revolutionary transfoSHUNT LEM can solve your current measure problems. It gives an accurate reproduction of any current DC and AC with a 5 kV insulation and a very convenient ratio 1:1000 i.e.Amps=>mA Model LA200S for instance measures up to 200 A with 1% accuracy. Price 95 $. Worth trying in chopper, inverter, power supply etc. A good accessory for scope and multimeter. L E M SA 14E Rte St-Julien CH 1227, GENEVA SWITZERLAND Tx 28 94 22, Phone (022) 42 29 00

LEM CURRENT MEASURE 188



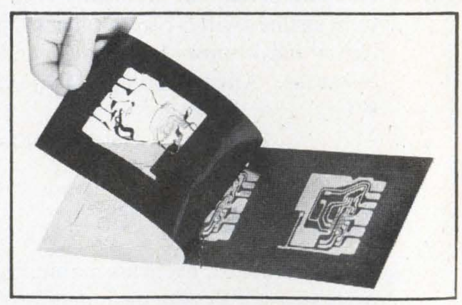
FAST, LOW COST DISCHARGE PRINTER DC-4004A prints 48 columns at 144ccps. Printing alphanumerics in 5 x 7 matrix format on 4.72" paper, its MTBF is 144 million characters. Just 2.6" H x 6.7" W x 5.9"D. it's only $127 in 100 quantity. Interface electronics, other printers available. HYCOM 16841 Armstrong Ave., Irvine, CA 92714 (714) 557-5252.

DISCHARGE PRINTER 183



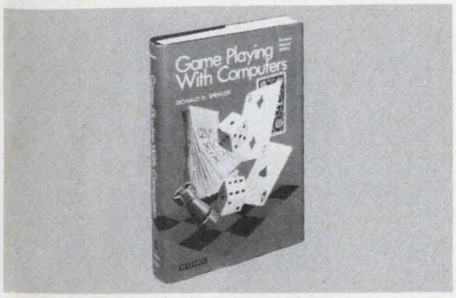
LOW COST LOGIC STATE ANALYZER. For $295, the 8-channel Model 100A features: 16-word truth table display • Pre- & post-trigger data capture • Single/Repeat display modes • HEX or OCTAL formats • Operates with virtually any oscilloscope. Need 24 bits? Qualifiers? Program paging and loop analysis? Add the Model 10 Expander for another $295. Both stocked in U.S. and overseas. Also kits. Paratronics, Inc., 800 Charcot Ave., San Jose, CA 95131. Tel: 408-263-2252.

PARATRONICS 186



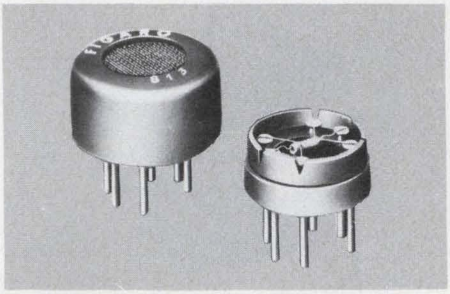
STAMPED CIRCUITS look like etched circuits, but they're not. They're stamped —and cost less. One oz., 2 oz., and up to 4 oz. copper available on all conventional PC board materials. Rogers Corporation, 5259 Minola Drive, Lithonia, Georgia 30058 (404) 981-9830

MEKTRON 189



GAME PLAYING WITH COMPUTERS, Revised Second Edition, by Donald D. Spencer. This volume presents over 70 games, puzzles, and mathematical recreations for a digital computer. The reader will also find brand-new "how to" information for applying mathematical concepts to game playing with a computer. #5103-4, 320 pp., $16.95. Circle the Info Retrieval Number to order your 15-day exam copy. When billed, remit or return book with no obligation. **Hayden Book Co., 50 Essex St., Rochelle Park, N.J. 07662.**

GAMES-PLAYING GUIDE

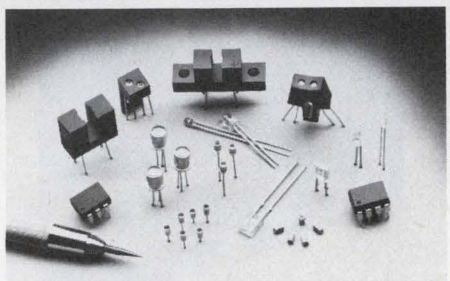


FIGARO GAS SENSOR TGS is a gas sensitive semiconductor. When combustible gas is absorbed on the sensor surface, a marked decrease of electrical resistance occurs. Major features of the sensor include high sensitivity, long term reliability and low cost. The applications are: GAS-LEAK ALARM, AUTOMATIC FAN CONTROL, FIRE ALARM, ALCOHOL DETECTOR, etc. Figaro Engineering Inc., North America Office-3303 Habor Boulevard, Suite D-8, Costa Mesa, Calif. 92626 Tel: (714) 751-4103 Telex: 678396

GAS SENSOR 193

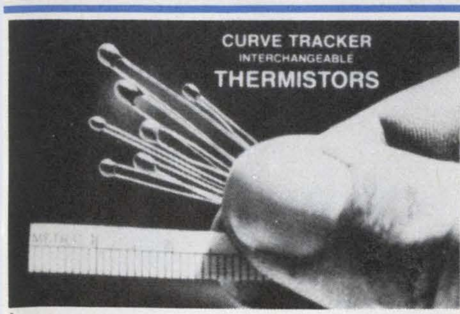
EXTREMELY SHOCK-ABSORBENT CASES. These polyethylene cases protect your delicate product better than metal or fiberglass cases (and far cheaper). Shock-damping outer shell first absorbs some impact energy, then foam absorbs even more. Result: your product suffers fewer g's. Airtight and waterproof. Meet military/airline/ASTM specs. Unbelieveable prices. 64 sizes. Also custom — send dwgs. Thermodyne International Ltd, 12600 Yukon Ave, Hawthorne, CA 90250 (213) 679-0411.

SHOCK-ABSORBENT CASES 191



FREE SPECTRONICS CATALOG describes infrared LEDs, PHOTOTRANSISTORS, OPTO SWITCHES and OPTO ISOLATORS. Microprocessor compatible isolators are U. L. recognized to 3500VAC. Outputs include SCR, transistor and high speed darlington (6N138). Industry standard LEDs and phototransistors are ideal for sensor applications to replace mechanical switches. Call or write for assistance with your state of the art design. SPECTRONICS, 830 E. Arapaho Rd., Richardson, Tx. 75081, (214) 234-4271.

OPTOELECTRONICS 194



CHIP THERMISTORS combine small size with reliability and low cost. R @ 25°C 50KΩ to 500KΩ ± 10% to ±1%. INTERCHANGEABLE tolerances ±1°C, ±.5°C or ±2°C. Point matched interchangeables to ±1%. HYBRID CHIPS and PROBES to your specs. WESTERN THERMISTOR CORP., 354 Via Del Monte, Oceanside, CA 92054. TWX 910-322-1983. (714) 433-4484.

THERMISTORS 192

The MICROPORT 8 digital panel display was designed to make interfacing to an 8 bit microprocessor port as simple as possible. The display contains all circuitry required to do its own timing, memory and multiplexing. With proper address decoding for the strobe, the MICROPORT 8 can even be connected to the processor data buss and accessed as a memory location. One year warranty. $109 (1-4). Jim Eley, Telesis Laboratory, P.O. Box 1843, Chillicothe, Ohio 45601 (614) 773-1414

8 Digit Panel Display 195

Electronic Design

ELECTRONIC DESIGN's function is:

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- To give the electronic design engineer concepts and ideas that make his job easier and more productive.
- To provide a central source of timely electronics information.
- To promote communication among members of the electronics engineering community.

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Individual article reprints and microfilm copies of complete annual volumes are available. Reprints cost $6.00 each, prepaid ($.50 for each additional copy of the same article), no matter how long the article. Microfilmed volumes cost $23 for 1976 (Vol. 24); $30 for 1973-75 (Vols. 21-23), varied prices for 1952-72 (Vols. 1-20). Prices may change. For further details and to place orders, contact Customer Services Dept. University Microfilms, 300 N. Zeeb Rd., Ann Arbor, MI 48106. (313) 761-4700.

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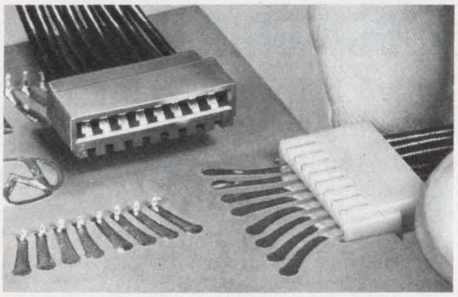
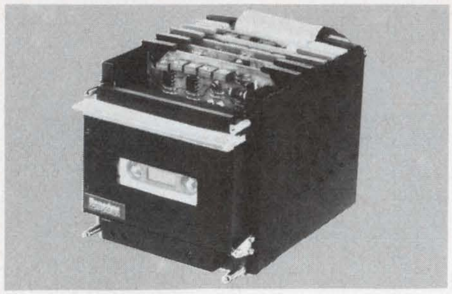
quick ads

New and current products for the electronic designer presented by their manufacturers.



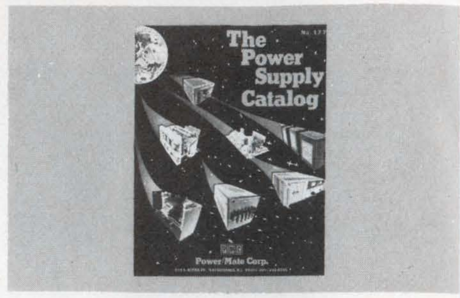
New Miniature Series 1500 Card Edge Connectors On .100" Centers For 1/16" PC Boards—Permit High-Density Wire-To-Board Interconnects plus in-the-field contact removal or replacement. Designed to mate with .062" thick single side PCB's. Permit independent wire harness assembly for 2/25 conductor cable. Methode 1400 Series crimp contacts used are rated at 3.5 amps. Contacts plated tin or gold. 94V-0 material housings. Methode Electronics, Inc., 1700 Hicks Rd., Rolling Meadows, IL 60008. (312) 392-3500.

MINIATURE CONNECTORS **196**



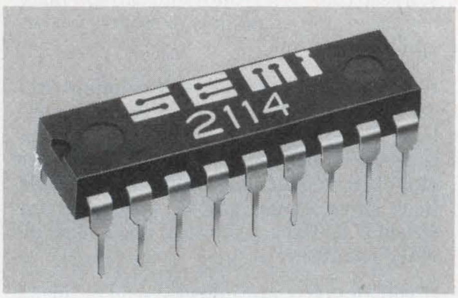
ANSI COMPATIBLE HIGH SPEED RECORDER Models 764-8 and 765-8 record and playback tapes directly compatible with Texas Instruments Inc. Silent 700 ASR data terminals. Units contain all circuits for accepting parallel data, formatting the data and adding the preamble and postamble. Easily interfaced to microprocessors, both recorders are TTL compatible and can store over 2 megabits of data. Recording speed is 20 ips. Weight only 4 lb. Delivery is 2 weeks. Memodyne Corporation, 385 Elliot Street, Newton Upper Falls, MA 02164. (617) 527-6600

HIGH SPEED RECORDER **199**



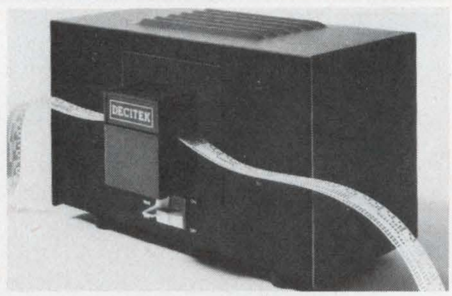
Free New catalog contains over 34,500 quality power supplies from the world's largest manufacturer, Power/Mate Corp. Power Supplies for every application including submodulars, open frame, varirated, encapsulated, laboratory & system. All units UL approved and meet most military and commercial specs for industrial and computer uses. Power/Mate Corp., 514 S. River St., Hackensack, NJ 07601 (201) 343-6294

POWER SUPPLIES **202**



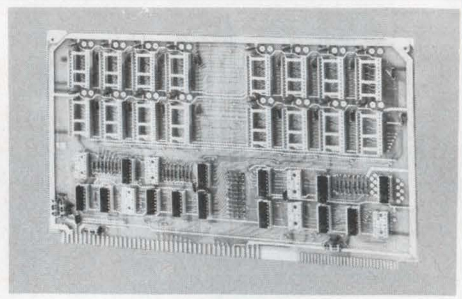
The experienced 2114 4K static RAM. From EMM — the industry's largest supplier of 4K static RAMs — a 2114 with a year and a half of delivery behind it. Not a new part. Just a new pin-out of a proven part. 1K x 4 organization. 5V only. Standard 18-pin DIP. It draws only 300 mw, has all the speed you need for microprocessor applications. EMM/SEMI, Inc., 3883 N. 28th Ave., Phoenix, AZ 85017. (602) 263-0202.

4K STATIC RAMS **197**



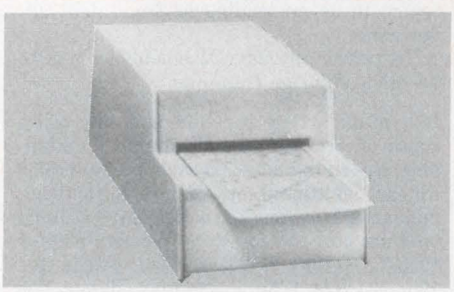
NEW DESKTOP TAPE READER—all you do is plug this Smart Box in. Up to 300 cps—RS232C, Current loop, parallel I/O—and quality built. State-of-the-art fiber optics, photo transistor read head, dual-sprocket drive. Outstanding for flexibility and simplicity. Low cost. Decitek, 250 Chandler Street, Worcester, MA 01602 (617) 798-8731.

NEW DESKTOP TAPE READER **200**



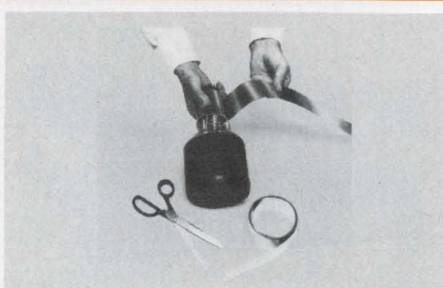
SBC 80/10 COMPATIBLE RAM AND PROM MEMORIES: $195, 32K PROM board except 2716 E-PROMs. $195, 16K PROM board except 2708 E-PROMs. $186, 8K PROM board except 2708 E-PROMs. $395, 8K RAM board includes low-power static RAMs. $295, 4K RAM board includes low power static RAMs. Battery backup RAM boards are also available. . .We ship from stock in three days. . .Electronic Solutions, Inc., 7969 Engineer Road, San Diego, CA 92111 (714) 292-0242

RAM and PROM BOARDS **203**



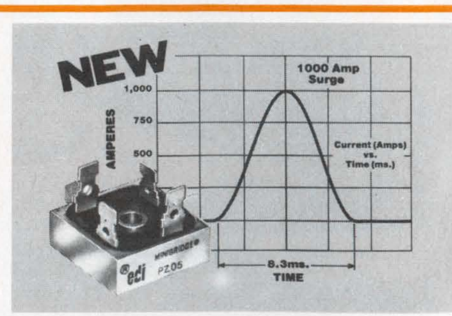
NEW SERIAL CARD READER The Model 417, from AMP. Reads punched hole or mark sense data on standard 80-column cards. Provides character serial, bit parallel data plus special interface options. Automatically returns or captures cards. Available with stand-alone housing, or with convenient panel-mounting provisions. Write AMP Incorporated, Capitron Division, Elizabethtown, PA 17022.

AMP CAPITRON DIVISION **198**



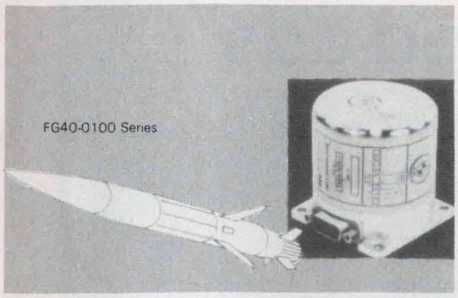
FORM YOUR OWN MAGNETIC SHIELDS When you need only one or two magnetic shields, save time and money by shaping your own. All it takes is a scissors and our improved Eagle alloys for magnetic shielding. We'll gladly help. Check the card in this publication and we'll send full details on Eagle foil and sheet stock. Eagle Magnetic Co., Inc., Box 24283, Indianapolis, IN 46224 317/297-1030.

MAGNETIC SHIELDING **201**



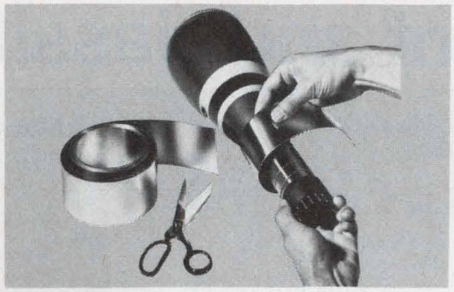
KILO-AMP SURGE CURRENT BRIDGE RECTIFIER CREATED BY ELECTRONIC DEVICES, INC... New Minibridge® rectifier can withstand a 1,000 ampere surge current. The "PZ" has a PRV to 400V, a 30 Amp. Current Rating, 0.250 Quick Connect Terminals, and a small 1 ⅛" x 1 ⅛" (2.84 mm) size. For trial samples, complete information, write: Sales Manager, Electronic Devices, Inc., 21 Gray Oaks Ave., New York, N.Y. 10710.

SAMPLE RECTIFIER **204**



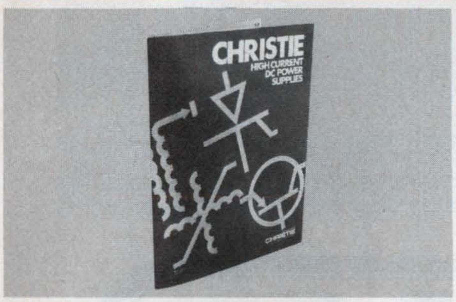
SPRING DRIVEN GYRO FOR MISSILE GUIDANCE SYSTEMS Rugged, 2¼" diameter, eight-ounce gyro fully qualified to MIL specs and GSA scheduled, contract No. GS-OOS. Solenoid activated, potentiometer on outer gimbal, manual caging, remote electrical uncaging, 100 MS runup time, full rotation, electrical range 357°, resolution 0.25°. Commonality of critical parts ensures low cost and fast delivery. Humphrey, Inc., 9212 Balboa Ave., San Diego, California 92123. Phone (714) 565-6631.

GYRO **205**



AD-MU CUT-OUT MAGNETIC SHIELDS Easily, quickly cut with scissors and shaped by you from AD-MU foil alloys. Available in various widths, lengths, shielding strengths. Time-saving, cost-saving, convenient. No waiting. No designing, tooling or fabricating costs. Ideal for R/D, hard-to-get-at places, or for small quantity or extremely compact applications. One formula (ask us) determines thickness and number of layers. Fully annealed, ready to use. AD-VANCE MAGNETICS, INC., 226 E. Seventh St., Rochester, Indiana 46975 (219) 223-3158

MAGNETIC SHIELDING **208**



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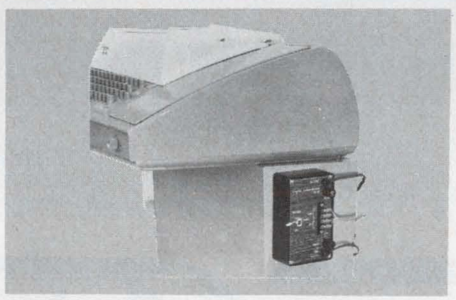
POWER SUPPLY CATALOG **206**



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ED5000 ROM/RAM SIMULATOR **207**

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POWER SUPPLY CATALOG **210**

Electronic Design

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June 7	**May 12**	May 26
June 21	**May 26**	June 9
July 5	**June 9**	June 23
July 19	**June 23**	July 7
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Aug. 16	**July 21**	Aug. 4
Sept. 1	**Aug. 4**	Aug. 18

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CALL THE RECRUITMENT HOT LINE 201-843-0550

Camera-ready film (right reading negatives, emulsion side down) or camera-ready mechanicals must be received by deadline. Or, if you wish us to set your ad (typesetting is free) simply pick up the phone and call our RECRUITMENT HOT LINE — (201) 843-0550. Ask for:

Constance McKinley
RECRUITMENT ADVERTISING MANAGER
ELECTRONIC DESIGN
50 Essex Street, Rochelle Park, New Jersey 07662

Engineers

WE ARE SEEKING ENGINEERS WHO ARE SPECIAL

HUTCHINSON INDUSTRIAL CORP., a well established manufacturer of peripheral equipment components, located in a clean air setting just an hour from Minneapolis, is currently seeking to build for the future with:

MECHANICAL DESIGN ENGINEER: This highly visable position offers an excellent opportunity for advancement. The successful candidate will hold responsibilities for the development and improvement of mechanisms and light machinery. In addition, must be able to work as an independent project engineer. An appropriate education includes a MSME degree.

ELECTRICAL ENGINEER: BSEE with educational background or experience in electromechanical interfacing instrumentation, control systems and automatic test equipment. Wide variety of challenging project responsibilities.

For immediate consideration submit comprehensive resume including salary history in confidence to:

Verne Meyer
HUTCHINSON INDUSTRIAL CORP.
40 West Highland Park
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Hutchinson Industrial Corporation

Project Engineers Electrical

Engineers with varying experience and length of service backgrounds sought to expand Project Engineering - Electrical Group. BSEE required.

Projects include process control, high-speed packaging automation, relay, programmable controller, mini-computer application, industrial power supply and distribution, building services.

Scope includes preliminary through final designs, oversight of consultants, contractors, equipment supplies, supervision of equipment installation and start-up.

Experienced Engineers must be capable of executing complete projects from conceptual stage through efficient production operation.

Outstanding potential for personal growth with industry leader during growth and expansion program.

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Anheuser-Busch, Inc.

Manager, Salaried Employment
Department J-4
721 Pestalozzi
St. Louis, Missouri 63188

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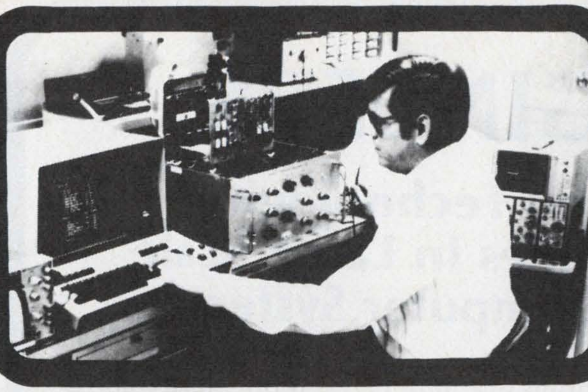

Systems/Design ENGINEERS

A Halliburton Company -Welex Division

Welex, the wireline service division of Halliburton Company, is assisting the energy industry in its search for and development of oil and gas resources. Welex designs and manufactures the electronic surface and subsurface equipment used in its field operations. Research is the backbone of Welex growth and is why we consider our Engineers to be so vital to the success of our operations.

We are initiating a major expansion of our technical staff and many challenging opportunities exist for Engineering Programmers and Electrical or Mechanical Engineers with recent creative experience in some of the following areas:

- Real Time Software
- Digital Circuits Assembly
- Assembly Language
- Analog Circuits
- Data Acquisition
- Microprocessors
- Graphics Displays
- Microcomputer

These permanent positions require minimum BS degree with graduate degree preferred.

Welex is headquartered in Houston, Texas, the 5th largest city in the U.S. The climate is mild and sunny on the Texas Gulf Coast, where cultural events, sports and recreational activities at nearby beaches and lakes are available year round. Houston's lower cost of living and no local or state income taxes make it more than comfortable to pursue your profession.

JOIN our team of professionals in helping this vital industry to keep AMERICA moving. If you are interested in the career opportunities we have to offer, please send resume in confidence to Employment Supervisor, Dept. ED, P.O. Box 42800, Houston, Texas 77042.

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Microprocessor Applications Engineer. Our advanced product design group is now offering an exciting and challenging opportunity to pioneer new product applications for the controls industry. BSCIS/BSEE (MS preferred) with three plus years experience in microprocessor systems design required. Prefer background in the controls or related industry with intimate knowledge of semi-conductor manufacturers.

Project Engineer-Electronics. BSEE/BSME with five to seven years experience in monolithic power semiconductor packaging and high volume hybrid micro-applications. Knowledge of current state-of-the-art and technology trends required.

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Mr. R. E. Goolsby
Ranco Controls Division
601 West Fifth Avenue
Columbus, OH 43201

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RANCO

Electronic Engineers

Down-to-earth product development openings for space-age engineers

General Electric specializes in producing high-quality appliances for the home. And our continuing leadership in this competitive business is a tribute to our engineering people. Last year alone, for example, many of the new products introduced featured highly innovative applications of space-age technology. The near future will bring more breakthroughs—and that's where you can help.

We have several openings for professionals with a BSEE and 3 to 5 years product development experience. Background must include applying the latest circuit design and micro-electronic design techniques. Join us and we'll provide you with a fully commensurate salary, famous GE benefits and stimulating assignments in an environment where individual contributions are seen and recognized. Apply now. Send your resume, including a description of your achievements and salary history to: C. C. St. Mark, Ref. 74-C,

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POWER SUPPLY AND FREQUENCY CHANGERS

Circuit Design Engineers
Application Engineers

Key positions are now available in a multi-million dollar division of this expanding operation. Varo, Inc. is a progressive NYSE company and a leader in the electronics industry. The Power Systems Division specializes in the development of power supply systems for both military and commercial markets. Our needs are:

ELECTRONIC CIRCUIT DESIGN ENGINEERS — with a BSEE required and an MSEE preferred. Must have 8 to 10 years experience in HIGH VOLTAGE circuit design or LOGIC and POWER circuit design.

HIGH VOLTAGE experience will include the design of low voltage oscillators, voltage multiplying techniques and low current sensing circuits.

LOGIC AND POWER experience would include the utilization of SCRs and power circuit design and logic circuit design utilizing TTL, CMOS, and/or microprocessors.

APPLICATION ENGINEERS — for power convertors and frequency changers. The qualified individual will possess a BSEE with 5 years of progressive selling experience. Previous power systems design experience a plus. Must be able to develop marketing tactics, sales techniques, strategic plans, and product forecasts. Experience working with Department of Defense/Energy agencies a plus.

The company offers an excellent fringe benefit program. Salaries are commensurate with experience and are complemented by a salary incentive program. If you are ready for a real challenge, send your resume with salary history in strict confidence to:

Bob Williams

VARO, INC.

P.O. Box 401426, Garland, TX 75040

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Constance McKinley

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Engineers

Boston Interviews with Technical Management May 23, 24 and 25

Our Hunt Valley complex, located in the northern suburb of Baltimore, has immediate openings in two engineering departments.

The Nuclear Instrumentation Control Department has requirements for engineers with experience in analog and digital circuit design. Responsibilities include the development and design of instrumentation and control equipment and systems for commercial and naval nuclear programs.

Requirements:

—BSEE with minimum of 5 years design experience.

—Ability to analyze designs and present results.

—Desire to apply innovative solutions to complex engineering problems.

The Integrated Logistics Support Engineering Department is involved in a variety of long-term automated test projects and has needs in the following areas:

Software

Applicants should have BSEE and major specialization in computers or with BS in Computer Science and a knowledge of digital and analog circuit design and at least 2 years experience in one or more of the following areas:

Design and generation of analog/digital test application software

Design and generation of ATE executive and support software.

Logistics and Maintenance

Applicants should have BSEE with advanced statistics and/or numerical analysis courses with a minimum of 2 years experience in one or more of the following: logistics models, simulation models, logistic support analysis, support equipment requirements, maintenance planning.

Digital Hardware Design

Responsibilities include systems specifications and design utilizing advanced microprocessors and microcomputers as applied to sophisticated electronic test problems. Minimum of 2 years experience and BSEE degree.

Electronic Design

Requires capability in solid state electronic design. Should have at least 2 years experience in analog and digital testing of military avionics subassemblies. BSEE required.

IF or RF Electronic Design

At least 2 years design experience involving very stable oscillators and other RF circuitry operating at X-band. BSEE degree.

Also, professionals with electronics background are needed in the following areas:

Field Engineering
Engineering Writers
Industrial Engineering
Product Evaluation
Test Engineering
Electromagnetic Compatability
Product Reliability/Maintainability
Quality Assurance
Manufacturing Processes

Attractive foreign assignments are also available for your consideration.

Boston Interviews

To arrange a Boston interview with technical management, call:

T. K. Brown
at 617/536-5700

Tues., May 23, 10 A.M. to 8 P.M.

Wed., May 24, 10 A.M. to 8 P.M.

Thurs., May 25, 10 A.M. to 5 P.M.

If unable to arrange an interview at this time, please send resume, stating present salary, and indicating department of interest, to:

R.A. Richmond, Dept. 425
Westinghouse
P.O. Box 1693
Baltimore, MD 21203

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Westinghouse

Advertiser's index

**Advertisers in International Edition*

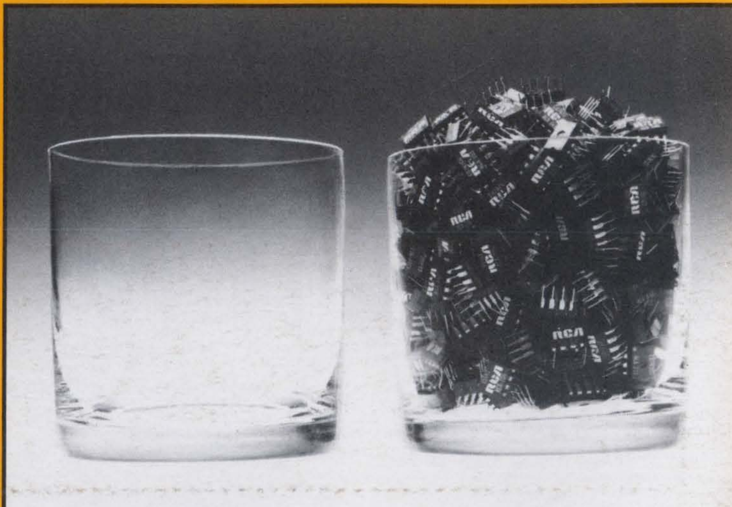
RCA. Newsmaker in Linear.

The 3240 Dual. New proof BiMOS is the answer in op amps.

First RCA introduced the BiMOS 3140, most useful op amp since the 741. Now, in volume, the 3240 – dual version of the 3140. It brings BiMOS benefits to users of the 747, Bifet TL082, and the often hard-to-get 1458.

Better than 1458 on performance. The 3240, like the 3140, delivers the benefits of MOS/FET input. Such as ultra-high input impedance and very low input current. It also gives you bipolar speed and high supply voltage operating capability: 4 to 44 V, dual or single supply. And much more.

Available now. In volume. Just a few months after its introduction, we're making the 3240 in volume...more proof of BiMOS ease of manufacture. So you can get as many as you want. Now.



When they're out of 1458's... Order the CA3240.

Duel of the Duals

Type (with single supply)	Input Common-Mode Voltage Range	V_{OM}^+	I_I	Slew Rate	Gate Input Protection Diode
BiMOS CA3240E	0 to (V^+–3V)	1 to (V^+–3V)	50 pA	9 V/μsec	Yes
Bifet TL082CP	5 to (V^+–5V)	5 to (V^+–5V)	400 pA	12 V/μsec	No
CA1458E	3 to (V^+–3V	5 to (V^+–5V)	500K pA	0.5 V/μsec	—
MC1458SP	3 to (V^+–3V)	5 to (V^+–5V)	500K pA	16 V/μsec	—

For more information, contact your local RCA Solid State distributor. Or contact RCA Solid State headquarters in Somerville, NJ; 1130 Brussels, Belgium; Sunbury-on-Thames, Middlesex, England; Quickborn 2085, W. Germany; Ste.-Anne-de-Bellevue, Quebec, Canada; Sao Paulo, Brazil; Tokyo, Japan.

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RCA

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