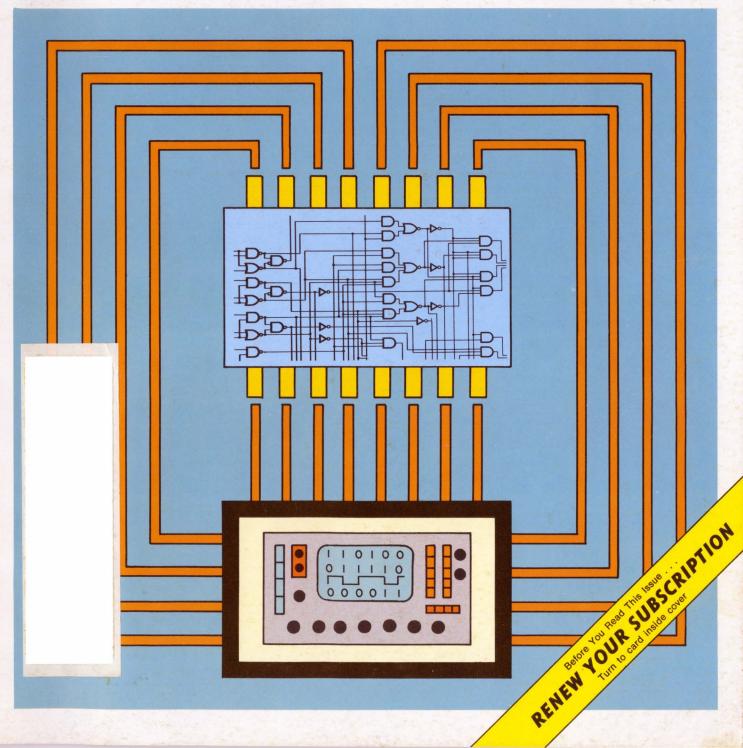
### ELECTRONIC DESIGN FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

Logic analyzers dig out faults in digital circuits more easily and quickly than other means. The latest can be used in the field as well as in the lab, and

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### Look inside our new Precision Pot...

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Since our new potentiometer looks like others on the outside, here's the inside story . . . that's where Bourns makes the difference:

The total construction of this new 1% linearity, conductive plastic, single-turn pot is ingeniously simple. Our one-piece precious metal contact delivers tens-of-thousands more trouble-free revolutions than the typical failure-prone two-piece type. Then, our exclusive silver deposition between the molded-in terminals and the element guarantees a connection that won't migrate or weaken during installation and operation. And, proven techniques like low temperature firing and thermal swaging replace unreliable solder, conductive epoxy and silver cement throughout the potentiometer. No one matches our performance, and our price is just as eye opening — less than \$6.00 in production quantities.

With fewer parts, unique packaging and solid connections, the result is obvious — the most reliable precision potentiometer you can specify for the price.

The  $7_8$ " diameter model is available in either bushing (Model 6637) or servo mount (Model 6537) styles. The larger 1%" diameter bushing mount (Model 6657) also offers a full line of non-linear functions . . . all with the same outstanding design and price advantages.

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ONE-PIECE CONTACT







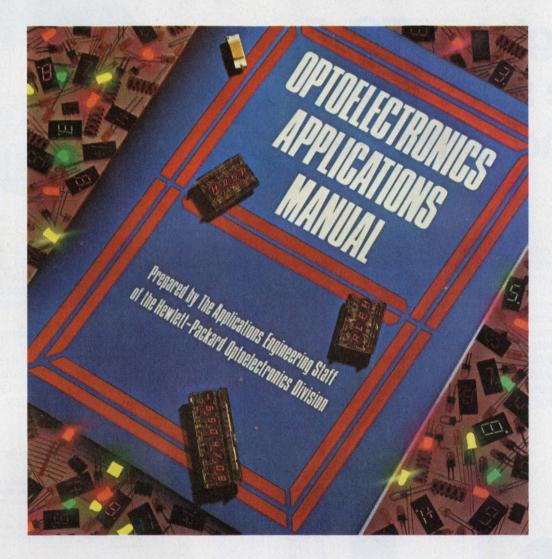




For Immediate Application-Circle 130
For Future Application-Circle 230

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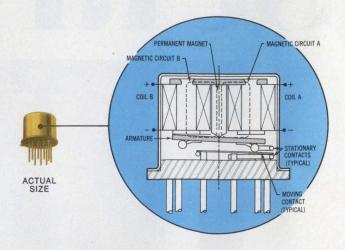
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### **TO-5 RELAY UPDATE**

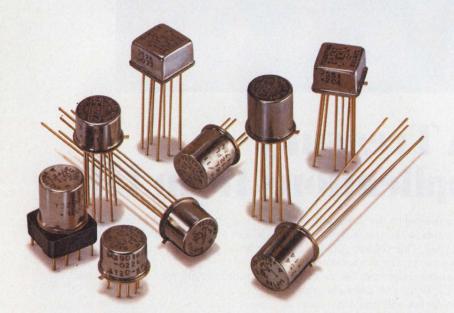
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Whenever critical switching circuits call for reprogrammable non-destructible memory, choose Teledyne's magnetic latching TO-5 — the relay that remembers. Once set with a short pulse of coil voltage, it will retain its state until reset or reprogrammed — even if system power fails or is shut off. And you get the added advantage of reduced system power demands, since conventional relay holding power is not required. But reprogrammable memory capability and low power consumption are not the only advantages of our TO-5 maglatch relays. Their subminiature

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Our magnetic latching as well as our complete line of TO-5 relays includes military and commercial/industrial types with MIL versions qualified to "L" and "M" levels of established reliability specs. For complete data, contact Teledyne Relays — the people who originated the TO-5 relay.



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   Hi-vibration types.

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VOL. 26 NO.

### **NEWS**

- 21 News Scope
- The latest logic analyzers offer more functions in a smaller package and at less cost—A special report.
- Forget the bugs in 4-k and 16-k RAMs—the big news is at 64-k.
- 38 The new GaAs FETs—less noise, higher power and broader bandwidth.
- 47 Washington Report

### **TECHNOLOGY**

- Microcomputer Basics: Part 1. Reduce your μC-based system design time by using single-board microcomputers. Assembled boards in the SBC-80 series offer stock answers to custom demands.
- **Logic analyzers aren't all alike.** Learn the differences between state and timing instruments, and you'll end up with the right troubleshooting tool.
- Try a Wien-bridge network instead of a twin-T in your next analog filter design. The advantages begin with a filter you can design in five fast steps.
- 84 Ideas for Design:

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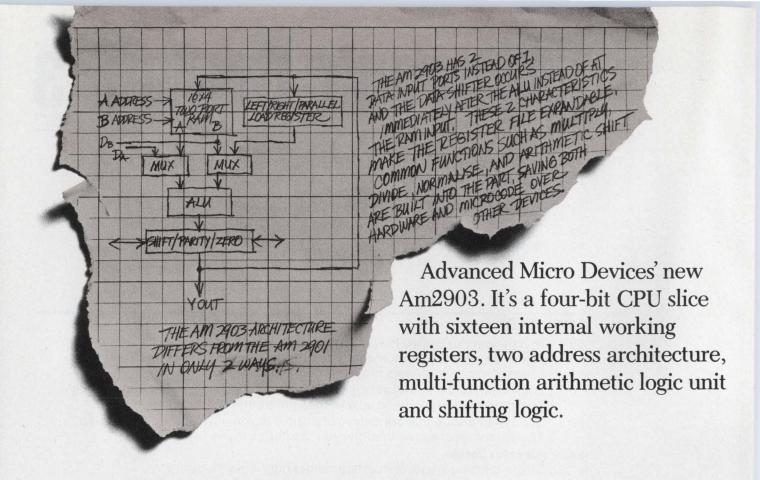
### **PRODUCTS**

99 ICs & Semiconductors 110 Packaging & Materials 102 Components 114 Data Processing 104 Modules & Subassemblies

### **DEPARTMENTS**

53 Editorial: Concepting an idea
7 Across the Desk 124 Employment Opportunities
118 New Literature 128 Advertisers' Index
119 Design Aids 128 Information Retrieval Card
119 Vendors Report
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ELECTRONIC DESIGN 3, February 1, 1978

### Across the desk

### Not that cheap

I wish to correct a few errors in "Software Distribution Is a Problem in Personal Computing-with Solutions" (ED No. 21, Oct. 11, 1977, p. 34). The correct name of our company is Micro-Scan Corporation, and our bar-code scanner is the "Data-Scan" Model BCS-1. Also, a statement inaccurately attributed to me might lead to some confusion-namely, that the price of our bar-code scanner (\$97.50) "is an order of magnitude cheaper than any available optical scanners." In fact, there are a few bar-code scanners that, when coupled with a signal conditioner, may cost as little as two and one-half to five times the price of our bar-code scanner, with its integral signal conditioner.

Frederick L. Merkowitz Micro-Scan Corp. P.O. Box 705 Natick, MA 01760

### You're a rug lifter

Most pieces on stepper motors are usually a rehash of manufacturers' published data, but your Focus (ED No. 22, Oct. 25, 1977, p. 48) pointed out many of the hidden problems that are usually swept under the rug.

Thanks for telling your readers that for some applications dc servos are a better design choice than steppers. We've seen enough cases where a stepper was used in an application better suited for a dc servo to know that many engineers follow the "easy" openloop path without thoroughly evaluating total-system parameters.

Allison C. Danzig Marketing Manager

PMI Motors 5 Aerial Way Syosset, NY 11791

### A forceful objection

In the Focus on Stepping Motors (ED No. 22, Oct. 25, 1977, p. 48), we find that

the established way of specifying torque is with force-unit lengths. The examples given are ounce-inches and gram-millimeters. But as I recall, the gram is a unit of mass, not a unit of force. Perhaps we should specify torque in dyne-centimeters, or newton-meters. As we make the transition to metric, let's try to get it right!

Harold Hallikainen President

Hallikainen & Friends 340 Higuera San Luis Obispo, CA 93401

### **Misplaced Caption Dept.**



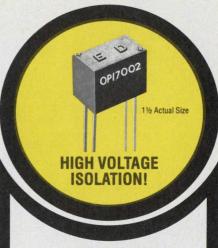
High-yield production requires true clean rooms and suitable attire for personnel.

Sorry. That's Jean Antoine Watteau's "Gilles," which hangs in the Louvre in Paris.

### Don't pass us by

The instruments described in "Precise Signal Sources..." (ED No. 24, Nov. 22, 1977, p. 76), with one exception, by no means represent the latest in technology or flexibility. Indeed, some of (continued on page 120)

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Managing Editor, Electronic Design, 50 Essex St., Rochelle Park, NJ 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.



### OPTRON OPTICALLY COUPLED ISOLATORS

NEW OPI 7000 SERIES OFFERS LOW COST, HIGH VOLTAGE ISOLATION

OPTRON's new OPI 7000 series optically coupled isolators meet the designer's requirements for high voltage isolaton, yet at a low cost.

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OPTRON	GE
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OPI 7010	H15A1
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OPI 7340	H15B1

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 $\mu$ Scope 820 is really the first test instrument of its kind. It's built around its own microprocessor, to provide a "smart" solution that's highly sophisticated, yet easy to use. Because it's user programmable with interchangeable plug-in ROMs or PROMs, it's like taking a design engineer along on every service call. And because it's fully portable, the  $\mu$ Scope 820 console goes wherever the action is—to the design lab, the production line or into the field.

Unlike logic analyzers, the  $\mu$ Scope 820 console provides a genuine solution for test and service personnel. It provides the same inside look at system operation that you get with a logic analyzer. But the  $\mu$ Scope 820

goes far beyond the mere collection of data. Its internal microprocessor system can actually analyze the data it collects. It does that with diagnostic programs you design specifically for your end product.

Rather than passively watching system operation, the  $\mu$ Scope 820 console lets you execute application programs or diagnostics you develop, in real time or single steps. And it provides full breakpoint capability



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Until now the only way to get this kind of diagnostic capability was to use your Intellec® Microcomputer Development System. Now we've taken the Intellec features that have proven most useful for field service and production-level system checkout and have packaged them in this

packaged them in this self-contained 20-lb attache case. That's portability.

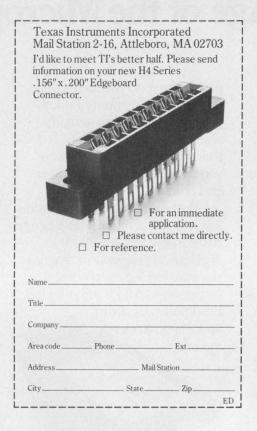
And we've enhanced that portability with a µScope 820 price of just \$2000,\* complete with personality probe and all accessories. So you can afford to put a μScope 820 console wherever you need one, and free your development lab instruments to concentrate on development. No longer must you invest in in-house-designed custom test instruments for each of your end products. And the µScope 820 console will be available with a selection of front panel overlays, "personality" cards and system probes to support a variety of microprocessors.

To get your copy of our μScope 820 brochure and to arrange for a demonstration right in your lab, contact your local Intel distributor or sales representative. Or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051. Telephone (408) 987-8080. In Europe contact: Intel International, Rue de Moulin a Pàpier, 51-Boite 1, B-1160, Brussels, Belgium. Telex 24814. In Japan contact: Intel Japan, K.K., Flower Hill-Shinmacki East Bldg. 1-23-9, Shinmachi, Setagaya-Ku, Tokyo 154. Telex 781-2846.

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On each 11" X 17" panel you can custom-design individual boards to meet your front panel needs. The illustration

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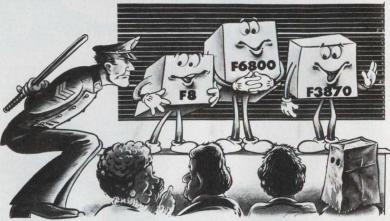
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F3856	2K ROM/TIMER/161/O			
F3857	2K ROM/TIMER/SMI			
F3852	MEMORY INTERFACE-DYNAMIC/TIMER			
F3853	MEMORY INTERFACE-STATIC/TIMER			
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	Co	ming Soo	n			
F6843 F6844 F6845	CRT CONTROLLER DIRECT MEMORY ACCESS FLOPPY DISK CONTROLLER	F3846 µA9706	BISYNC/SDLC COMMUNICATIONS CONTROLLER 8-CHANNEL, D/A CONVERTER			

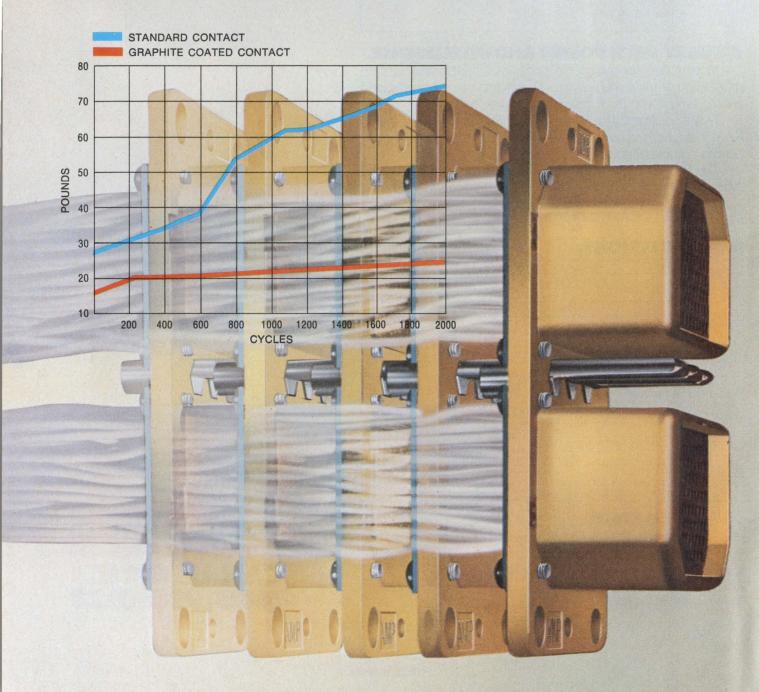
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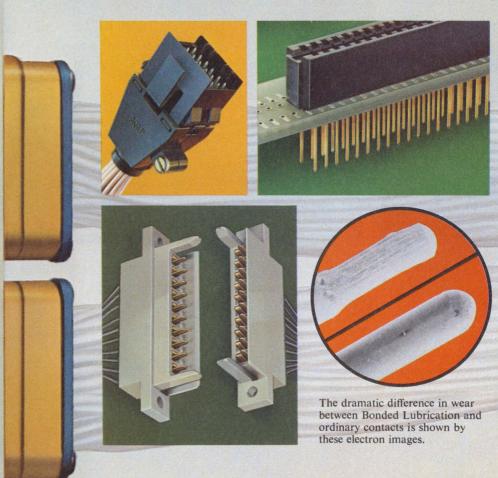
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### AMP has a better way.

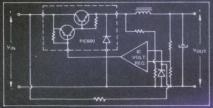






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Typical Schematic for Positive Voltage Switching Regulator:

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Full disc compatibility with Zilog's larger Development Systems makes the Z80-PDS an excellent lowcost work station for adding program development power to microcomputer design teams.

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available in 1 week from factory or from distributor stock. 6, 8 or 10 pin models(-01 circuit) in 49 standard values. Consult factory for fast delivery times on other configurations and schematics. APPLICATIONS: Standard circuit (-01) has 5, 7 or 9 resistors with 1 pin common.

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**CIRCLE NUMBER 351** 



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Remember, good connections run in our family.



CIRCLE NUMBER 14

### News scope

**FEBRUARY 1, 1978** 

### Now μPs help cut heat bills and sync filmstrip sound

How'd you like to cut your fuel bill in half by designing a microprocessor-based heating system that uses solar heat—and your swimming pool for a heat sink? Or perhaps you would like to add a microprocessor control system to an educational film-strip projector so that the narrative sound, on cassette tape, automatically follows any selected sequence of film frames—for less than \$10.

If you're interested, go to the Consumer Systems Session at the Industrial Applications of Microprocessors Conference in Philadelphia, March 20 through 22, where the designers of both systems will give you a nuts and bolts description of how you can.

The solar residential heating system, which is controlled by an Intel 8035 CPU with a 2-k × 8-type 2716 PROM, comes from S.C. Peek, senior engineering specialist for GTE Sylvania, Salem, MA. He is operating the system in his home and pool.

The microprocessor is used not only for control, but was also used to simulate system operation, Peek explains in "A Solar Heating System Simulated, Controlled and Instrumented by a Microcomputer."

According to simulation based on the weather of 1958, a standard year used by solar-system designers, the fuel bill using the solar system will be only \$314 against \$666 using oil heat.

To provide low-cost control, the  $\mu P$  system, using Sylvania's Modular Electronic Control Assemblies, takes inputs from glass-bottle thermistors strategically placed in the system and applies their analog signals to simple, ramp-generating a/d converters. Algorithms controlling the system can be readily modified because the program is designed in Basic language. A Z-80 programmer is being used at the Peek home.

The microprocessor controls the exchange of energy from solar panels to the swimming pool, and from the swimming pool to a heat pump that

extracts heat from the water and circulates hot air. The bank of five solar panels (Peek will have 10 next year) captures the heat in 300 ft of common black neoprene garden hose. As the water heats above a preset temperature, the system starts circulating it, while transferring heat to the pool. The collection panels have proven to be 68% efficient, with 25 F outside temperature. This contrasts with the more usual high temperature solar panels which have 40 to 50% efficiency.

Another way to get solar heat is via the pool itself, which is covered with a few hundred blank, transparent fluorescent-lamp tubes acting like thermos bottles floating on top of the water. The sun's radiation goes through them and is trapped in the pool. A pump circulates the pool water through a radiator that extracts heat to warm up air to 130 F. The air is then circulated through the house.

This solar system is more efficient than solar systems that circulate 140-F hot water, according to Peek.

Jack V. Landau, staff engineer at the Singer Corporate R&D Laboratory in Fairfield, NJ, was given an objective of producing a control system for \$10 that would keep the narrative sound on a tape cassette in step with a random choice of the frames of a film-strip projector. He started with a PPS-4/1 microcomputer from Rockwell.

But because the chip doesn't have an accurate timing system, software was used to solve several timing problems, according to Landau in "A Microcomputer Controlled Filmstrip Projector." One major challenge, providing the timing to keep the cassette tape in sync with either regular or random frame changes, was met with a 50-Hz cueing signal 450 ms long to advance the frames.

Software also provides delayed signals from the various switches in the projector to eliminate extraneous transients and a debounce function to prevent erroneous operation. Software also keeps track of whether or not the tape has broken or run out, by checking the status of signals produced by a switch that is actuated by the tapeplayer spindle.

The processor provides the operator with a "book-mark" key to identify and recall automatically any frames the operator selects.

It also monitors the pulse widths of the cueing signals to reject noise or other transients that might accidentally advance the film strip.

According to Landau, he brought in the design for less than the \$10 goal.

### Programs don't disappear in thumbwheel calculator

Programmable calculators have an annoying tendency to lose their programs when turned off. One way to solve this problem is found in a unique hybrid programmable, the EL 5001, which permanently stores six engineering programs as well as 26 other preprogrammed scientific functions. This 39-key machine from Sharp in Paramus, NJ, was introduced at the recent Winter Consumer Electronics Show in Las Vegas.

The programs are selected not by keystroke but by a six-position thumb-



wheel switch. Answers in the \$49.95 calculator appear in a 10-digit fluorescent display with a two-digit exponent in a scientific-notation mode.

Programs cannot be keyed into the EL 5001, but those designed-in were judged to be solutions to the most common engineering problems. Electronic designers will be particularly interested in four programs that have simple keystroke routines for solving complex number, impedance, vector, and stability problems.

For complex numbers, impedance and vector problems, add, subtract, multiply and divide operations are programmed-in. Answers to complex-number arithmetic appear for both real and imaginary components. And transformation to polar coordinates is provided.

For impedance and vector calculations, answers can be obtained in polar form with a magnitude and an angle, or in rectangular coordinates. For stability analysis of simple systems, one program solves for the real and imaginary roots of quadratic functions. Another program used integrates polynomial functions simply. And a statistical program permits the standard deviation of experimental samples and their populations to be calculated.

One unusual program makes it easy to plot monomial and polynomial functions of  $X^2$ ,  $X^{1/2}$ ,  $Y^x$ , and  $Y^{1/x}$ .

If a wrong number is entered at any program step, it can be corrected simply by keying in the proper number and repeating that step. The error is simply overwritten.

CIRCLE NO. 317

### $\mu$ P-controlled tester cuts mini-based cost by half

A printed-circuit board tester designed at RCA Laboratories in Princeton, NJ, uses a microprocessor development system as a controller to cut hardware costs to about \$5000—a far cry from the \$10,000 or more for commercial minicomputer-based testers.

"Microprocessors offer the opportunity to apply computer control to testing problems that do not justify a more powerful and costly processor," says Angelo Marcantonio, a member of RCA Labs' technical staff. In this case, an RCA 1802 CMOS microprocessor, housed in a COSMAC development system, was chosen for its I/O architecture and because the project members knew it well.

The board tester, used for high-volume production line testing at RCA, can perform 100 measurements per second on a board populated by diodes, capacitors, inductors and resistors. One board can be tested in about one second; inserting and removing the PC card raises the handling time to about nine seconds.

The tester makes both dc and ac twoterminal impedance measurements on the boards. Resistance measurements are made with a stable dc source by calculating the voltage drop across a precision resistor in series with the unknown. The magnitude and polarity of the potential across diodes is checked by applying a low amplitude direct current and measuring the response with an a/d converter. Reactive components are tested either by a fast-pulse technique or by calculating the phase shift on a 5-kHz sine wave.

All measurements are referenced to readings obtained from a known-good PC board. Test programs and limits are stored in EPROM that is separate from the EPROM that stores the tester's control program. The test program can therefore be modified simply by updating the directive EPROM without changing the test system's control program.

The tester consists of the micro-computer, interfaces, a control panel, a printer, and an air-actuated contact assembly mounted in a standard rack. Interfaces include a 12-bit a/d, software-controlled relay matrix, signal multiplexer, 20-column printer interface, and a signal package with a dc source, pulse generator, ac generator, and phase-measurement circuitry.

The control program occupies less than 1.5 kbytes of memory, and test directives occupy 2 kbytes. That means there are 128 tests at 16 bytes per test in the program.

Since boards to be tested consist of passive components, signal and detection circuits are relatively simple and inexpensive.

### Listen carefully: Your car's calling you

Ever return home from a business trip only to wander aimlessly around the airport parking lot, trying to find your car? Well, take heart: An electronic auto-security system that responds to a pocket transmitter will locate it for you in a flash—of the lights, that is—and with a blast of the horn.

Press the button on your lightersized uhf transmitter, and if your car is parked within 100 ft the Pulsafe Auto Security System from TMX, Inc. (Los Angeles, CA) will recognize your custom-coded transmission, turn the car's parking lights on, deactivate the alarm system, remove the ground from the ignition wires, and honk the horn.

Five pulses are transmitted in sequence during a 400-ms time window.

Each pulse duration is resistor-programmed to one of 25 particular val-

ues, and the same resistor programming takes place in the receiver. Five pulses combined with 25 steps and 10 different channel frequencies yield over 140-million code combinations.

"No station license is required," notes TMX General Manager Nate Sassover. "Because the unit's radiated power is so low, it complies with FCC rule number 15."

After parking your car, lock it, then push the transmitter button—the intrusion system is armed, the ignition ground is activated and the horn beeps twice to verify.

To guard against intruders, Pulsafe isn't wired to the auto's door switches, but uses an audio detection system with an adjustable threshold. Should an unauthorized person enter the car or tamper with the engine compartment, he will have to contend with the horn sounding and the headlights flashing alternately for one minute.

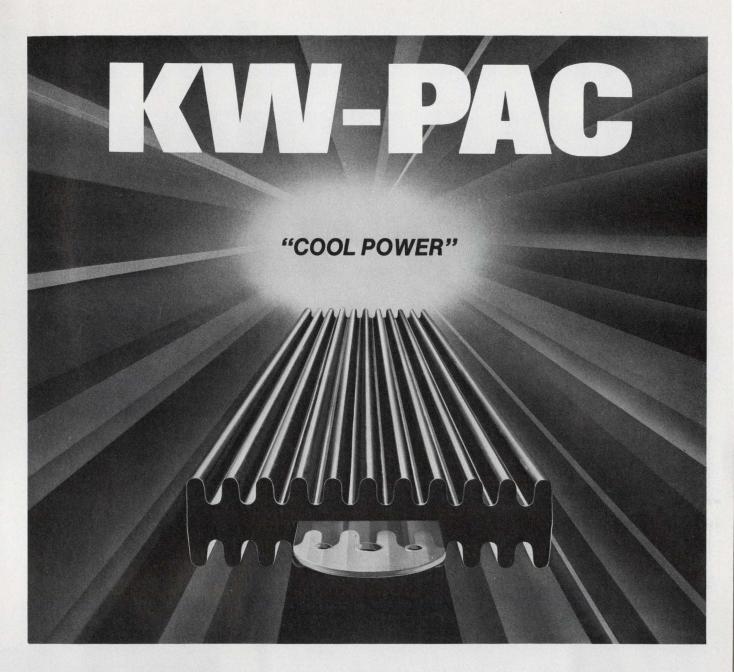
### Paramedics' load lightened by new voice/ECG radio

Paramedics looking for a lightweight coronary observation transceiver to help them take care of heart attack victims will welcome a unit weighing less than 19 lb including battery and handset. This transceiver from Motorola's Communications Division in Ft. Lauderdale is much lighter and more compact than available "portable" units, which weigh as much as 50 lb.

The weight of the APCOR Duplex/Multiplex Coronary Observation Radio is kept down by putting much of the circuitry into hybrid modules, and by replacing steel and fiberglass with lighter alloys and high-impactresistance plastic.

The Motorola unit consists of a uhf-FM voice transmitter and receiver, and signal-processing circuits for the electrocardiogram (ECG). With this transceiver, a paramedic can talk to a doctor at a hospital while sending him an ECG over the same channel. The ECG signal is multiplexed into the voice-transmit channel by modulating a 1.4 kHz subcarrier. Voice is passed through a notch filter at the subcarrier frequency, and then mixed with the subcarrier for transmission.

With 12 W, the range can extend to as much as 20 miles, under ideal conditions. For a bit more range, transmit power can be increased to 15 W. Operation is full duplex in the 450 to 470-MHz band, with a transmit frequency 5 MHz above receive.

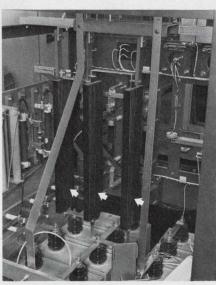


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- 750 V to 72,000 Volts
- 3.8 to 20 Amperes (55°C oil)

A 72KW driver power supply, built by Continental Electronics Manufacturing Co., Dallas, Texas, featuring three KW-PAC rectifiers.



CIRCLE NUMBER 15

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and versatile hardware for microcomputer applications or Z80 program development. As a complete disk-based computer it provides all the tools required for hardware/software development and debug.

The efficient, straightforward hardware organization of AID-80F includes the powerful Z80 Software Development Board, OEM-80; a memory and I/O expansion board, RAM-80; and the floppy-disk controller board, FLP-80. Optional in-circuit emulation capability is provided by Mostek's Application Interface Module, AIM-80™. AID-80F Software.

Mostek software is state-of-theart: efficient, comprehensive, and easy-to-use. It's designed to

AID-80F offers powerful software accelerate your own programming rate, allowing you to concentrate on the application problem, which greatly reduces the overall development cycle.

> The power of Mostek software is found in programs like Monitor, Text Editor, Assembler, Relocating Linking Loader, and Debugger. In addition, the Peripheral Interchange Program (PIP) offers the most complete peripheral management system in the industry



AID-80F Hardware.

OEM-80. It's the heart of Mostek's new AID-80F, providing the power of the Z80 microcomputer plus 16K bytes of on-board RAM.

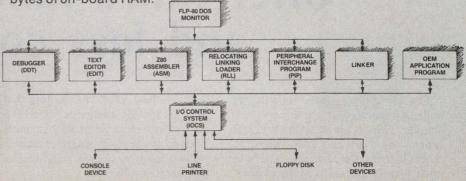
RAM-80. This memory and I/O expansion board includes 16K bytes of RAM (expandable to 64K bytes) and four eight-bit I/O ports.

FLP-80. Mostek's flexible diskdrive controller board interfaces OEM-80 with up to four drives with soft sector format.

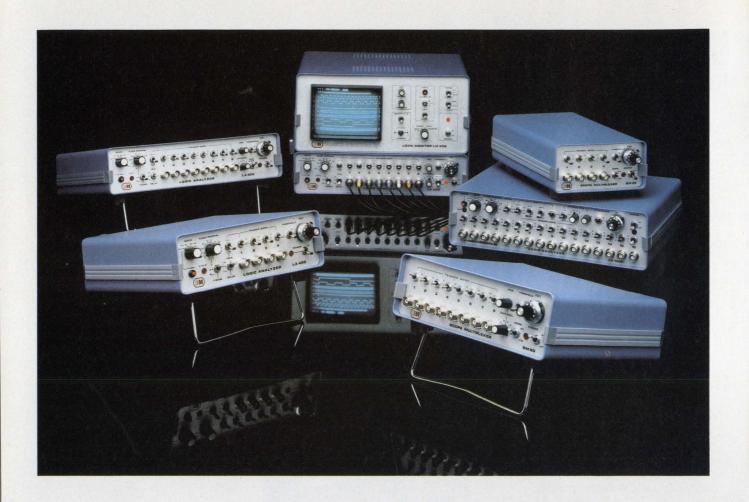
AIM-80. This optional board allows real-time, in-circuit emulation with extensive debug, trace and diagnostic capabilities.

AID-80F is priced at just \$5995 and each board is also available separately. To get a complete descriptive package on the AID-80F Microcomputer, contact your sales representative or write Mostek Corporation; 1215 W. Crosby Road; Carrollton, Texas 75006; (214) 242-0444, Mostek GmbH: West Germany; Telephone: (0711) 701096

### MOSTEK







### The latest logic analyzers offer more functions and less cost

The latest logic-state, logic-timing and microprocessor analyzers are smaller, lighter, easier to use, and less expensive to buy and to operate than their older counterparts. The aim is to make logic analyzers as useful in field-service testing as in the design lab.

While most older logic analyzers are designed specifically for engineers to test and debug new digital circuits and systems, many new ones are being optimized for the field-service technician trying to get a once-working system back on the air. But this doesn't mean that design engineers have to make do with their older instruments while all the new gear goes elsewhere.

Over the past year, the changes that have made logic analyzers more valuable to the technician make them more valuable to the design engineer as well, while adding to a growing choice of logic-testing aids.

### **Testing logic**

Not too long ago, logic-analyzer suppliers could be counted on the fingers of one hand—now more than two dozen are in the game. And each one makes an instrument—or a line of instruments—that's a little bit different.

While the most popular logic-timing analyzers sample digital signals at 10 or 20 MHz, some units can't even exceed 2 MHz. But at least one (Biomation's Model 8200) can sample up to 200 MHz.

Then there's the logic-state analyzer, a slightly different breed that samples at the clock frequency of the unit under test. Recently, Hewlett-Packard introduced its Model 1615A, which combines logic-state and logic-timing analysis.

Yet another variation, the microprocessor analyzer, is aimed at microprocessor-based systems. Some, like American Microsystems Inc.'s MDC-140, are so dedicated to microprocessor testing that they are nearly useless for testing random logic. And some only test specific device types.

Suppliers are placing more emphasis on field-service applications for all analyzers because field-service departments buy hundreds of one model at a time, to give all technicians the same kit of aids.

Andy Santoni Associate Editor There's plenty to choose from now in logic analyzers, as can be seen from just one manufacturer's offerings. E-H International offers analyzers, scope multiplexers, and monitors from about \$450 to \$2700.

Moreover, field-service departments are ready for logic analyzers, says Bruce Farly, product manager at Hewlett-Packard Co.'s Colorado Springs Division. Since this relatively new breed of instruments is already accepted and understood by most design engineers, he explains, suppliers are now ready to take in a new group of potential users.

### **Cutting** costs

A good example is the Model 920-D from Biomation Corp., Cupertino, CA. At less than \$1300, the 920-D is Biomation's least expensive analyzer, yet it retains most of the features of the firm's older models, and even adds a few. It has nine input channels, and its operation is triggered on any userselected combination of these nine channels. The ninth channel can operate just like any of the other eight, or it can be used as a trigger marker and qualifier. It can also be used to gate the clock of the system under test when this signal doubles as the recording clock of the analyzer.

Like all Biomation logic analyzers, the 920-D has a latch input mode for capturing narrow pulses or glitches—in this case, as narrow as 10 ns. Input impedance is 1 M $\Omega$ , and either  $\times$  1 or  $\times$  10 scope probes can be used. Threshold levels can be fixed to TTL or ECL levels, or adjusted by a front-panel slotted control.

Unlike Biomation's older eight-channel Model 810-D, which operates to only 10 MHz, the 920-D boasts 20 MHz. And neither combinatorial triggering nor digital trigger delay is covered by the older unit's \$1500 price.

Why is the new model less expensive, yet more powerful? The tried-and-true methods for cutting the cost of electronic equipment apply as well to logic analyzers as to any other product. With field-service needs in mind, Biomation can expect higher volume for its new instrument. This expected volume justifies using a molded plastic box that is lighter and more durable, yet less expensive, than the 810-D's metal cabinet. And large-scale integrated circuits replace many of the small and medium-scale and discrete devices in the 810-D.

"Because of its compact size and light weight, the instrument is a willing companion for the field service technician," says Roy Tottingham, applications engineer at Biomation. Designers gain, too—"Because of the operating features and modest cost, the instrument is also quite suitable as a design aid for the engineer."

### Keyboard control helps

Similar accolades can be given to Hewlett-Packard's Model 1602A logic-state analyzer. Its keyboard control panel and quick connect and disconnect edge-connector probe simplify service and production-line applications, as does it programmability. With Option 001, the Model 1602A becomes compatible with the HPIB—HP's version of the IEEE-488 standard instrument interface bus—so it's easy to tie into an automatic functional test system.

For example, working with a computing controller, the 1602A can test a computer system that has failed. Enough tests can be performed in a short enough time for the failure to be tracked down to the errant board.

Swapping boards at random to find the one bad board is avoided—and money saved—if the bad board is discovered quickly. Otherwise, bad boards going back to the factory for rework and good boards going out to field-repair depots create what is called a "float" of assemblies that represents a costly inventory.

Even though a calculator-controller and logic-state analyzer combination may seem rather large and cumbersome for the field, faster and more accurate field repairs may make such a combination seem lighter. In fact, HP believes that solving service and production problems will occupy most of the 1602A's time. However, the company also believes that the analyzer will make a superb companion to laboratory equipment.

The primary reason that the 1602A is useful for both laboratory and field applications is that it's very easy to use, says HP's Farly. At turn-on, the unit performs a self-test that, if all is well, ends with the display lighted up in alleights so that even the display is tested. If a failure occurs, the instrument can be commanded to single-step through



**Timing or state analysis, or both at the same time,** is a feature of Hewlett-Packard's Model 1615A. It can also catch glitches as short as 5 ns, and display them on a built-in CRT. Price is \$6800.



**Keeping costs down** is the aim of HP's Model 1602A. IEEE-bus compatibility and testing are special features of the instrument, which sells for only \$1800.



**Testing the S-100 bus** standard for small-computers is simplified with the Paratronics Model 150. And it costs only \$449 (\$369 in kit form).

the test program and tell an operator where the failure is.

A signal-source card that plugs into the 1602A's probe pod makes it possible to test even the probe, so that both the design engineer and service technician can be sure there are no instrument problems to contend with while making measurements.

### Checking out the bus

The probe pod can also be connected, via two optional modules, to an IEEE-488 bus system. The logic analyzer then becomes a bus-system analyzer and can check that the instruments are communicating with each other in the proper sequence and with the proper handshake signals.

As a matter of fact, adding the ability to check the 488 bus to a logic analyzer's bag of tricks is becoming more common, as illustrated by the DF2 bus-analyzer plug-in for Tektronix Inc.'s Model 7D01 logic analyzer. The DF2, like the basic 7D01 logic analyzer from the Beaverton, OR, firm, plugs into the company's 7000 Series of oscilloscopes. Another Tektronix logic analyzer, the LA 501, plugs into the firm's TM-500 Series of modular-instrument mainframes.

### **Catching glitches**

Often, new modules for one set of logic-analyzer plug-ins become avail-

able in a different format for the other module series. Last fall, for example, Tektronix added the DL2 digital latch, which mates with 7000-Series scope mainframes, and the DL 502, which mates with TM-500-Series mainframes. Either unit can latch glitches as narrow as 5 ns and with amplitudes as small as 500 mV centered on a threshold set by the user.

The DL 502 is part of a convenient, though expensive, package for fieldservice logic testing. Also included are a WR 501 word-recognizer and digital



More features, less cost is the hallmark of Biomation's 20-MHz, 9-channel Model 920-D, shown here with optional CRT display.

delay, an LA 501 logic analyzer, and an SC 502 dual-trace, 15-MHz oscilloscope—all in a six-hole TM-500 mainframe. More likely, this \$7400 combo (\$5990 without the scope and in a four-hole frame) will be found in the lab where the mainframe and scope plug-in can work with a different set of plug-ins for other applications, and the flexibility of the modular system can be put to good use.

A less-expensive logic analyzer plugin package is the LC-320 from Scanoptik Inc., Rockville, MD. Tektronix' SC 502 is combined with Scanoptik's LC-32 logic analyzer in a three-hole mainframe for \$4390.

The \$1595 LC-32 has 32 channels and a 4-MHz maximum clock rate. It can store in its memory then feed up to 64 words of data, typically from a microprocessor's address and data buses, to an external CRT display unit.

### Checking out microprocessors

Another logic analyzer aimed at testing microprocessor systems—and only \$1020—is the MPA-1 from E-H International Inc. located in Oakland, CA. Designed by Yucca International Inc. (Scottsdale, AZ), the MPA-1 comes with a probe for one microprocessor type, and can be configured for other microprocessors by changing probes. So far, 6800 and 8080 probes are available, and probes for the Z-80, F-8, and SC/MP are in the works.

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\*Complete Kit (No. 698-OK-002): \$190. Kit less driver and pre-amp (No. 698-OK-001): \$99.50. elements feature gold-plated brass construction to ensure the integrity of shielded enclosures.

The temperature referenced pre-amp operates from dc to



†Dupont trademark

All components of the kit are available separately. Standard accessories include butt splices, o-ring seals, and cables of other lengths. For more details and a list of Augat distributors, write Augat, Inc., 33 Perry Avenue, P.O. Box 779, Attleboro, Mass. 02703.Tel. (617) 222-2202

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Most of the other logic analyzers in E-H's product line were also designed by another firm—Dolch Logic Instruments in Germany. Like the MPA-1, they are marketed in the U.S. by E-H, which expects soon to be manufacturing the instruments, too.

All the new logic analyzers from E-H have clock rates up to 20 MHz. Memory depths are 256, 512, or 1024 words of 4 to 16 bits, and prices range from under \$1000 to about \$2300.

Besides its logic analyzers, E-H has a pair of logic monitors that, when connected to any logic analyzer, add comparison-mode testing to that analyzer's roster of features. Data are stored in one register, then more data are stored in a second register and compared with the first set. Since differences are flagged, spotting faults is simplified. The eight-channel LM 208 is priced at \$2295 and the 16-channel LM 216 is \$2695.

Meanwhile, some of the lowest-cost logic analyzers are coming from Paratronics Inc. of San Jose, CA. For example, the Model 100A, an eight-channel unit that stores 16 words, is \$295—or \$229 in kit form. For the same prices, the Model 10 expander adds 16 bits of triggering and display.

The Paratronics analyzer is a logicstate instrument that displays onezero truth tables on an external CRT. The Model 100A/10 package also provides a user-programmable digital delay for paging through programs up to 1000 steps long, and a pass counter that



**Grab the bus and check it out** with a logic analyzer that has an IEEE-488 adapter, like this Tektronix combination of analyzer, adapter, and latch in a 7000-Series scope mainframe.

permits a microprocessor's state to be monitored after a set number of passes through a loop.

Another Paratronics analyzer, the Model 150 Bus Grabber, is designed to test computers that conform to the S-100 bus standard. For \$449 (\$369 in kit form), the 150 plugs into a computer slot and monitors 56 bus signals. Eight more signals can be picked up by an optional plug-in flat-ribbon probe assembly.

The latest Paratronics analyzer, the Model 532, goes for \$1500. This 32-channel  $\mu$ P-based instrument captures and displays up to 250 words either in alphanumeric hexadecimal notation or in binary ones and zeros. It also fea-



Different strokes—timing diagram, state diagram, or map—are available in a few logic analyzers like this BP Instruments 50D with optional 50D011 display formatter.

tures a wide range of triggering modes, including the ability to trigger on the nonoccurrence of an event.

### Variations on triggering

Extensive triggering facilities are also featured in HP's Model 1615A. This unit combines logic-timing and logic-state analysis so that time-domain problems like glitches or state-domain problems like program errors can be traced. In fact, the state-domain display can be triggered by a time-domain occurrence, and vice versa.

The \$6800 Model 1615A can trace events on as many as 24 channels at up to 20 MHz, with a 256-word memory. And with a 6-bit clock qualifier, the user can select specific data such as read or write instructions or I/O instructions.

The analyzer can be configured by keyboard entry into 24 bits for state analysis, 8 bits for timing analysis, or a combination of 16 bits of state and 8 bits of timing information. Glitches greater than 5 ns wide can be captured and made part of the unit's trigger specification.

Unlike most analyzers, which use a pulse-stretching circuit to catch and display transients, the 1615 uses a second memory to store transient data. With pulse stretching, a transient is stored, then displayed on the analyzer's next clock edge. If the signal line goes through a normal transition between the glitch and the clock edge, the transient may be lost. In the 1615A, the glitch would be shown as a brightened edge on the transition.

The ability to display both time and data-domain problems helps a design engineer debug both hardware and



Testing microprocessor systems is easier with an analyzer that's dedicated to the task. The AQ8080 can handle 8080 and 8085 types by changing probes.

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software problems, notes Ken Pine, marketing vice-president of BP Instruments Inc. The Cupertino, CA, firm's Model 50D or Model 50D16 can be attached to the Model 50D011 display formatter to allow an operator to examine stored digital information in timing-diagram, binary, hex or octal, or map modes. The map-mode format generates an XY plot of the 510 words stored in memory, arranging them in  $4\times 4$  (Model 50D) or  $8\times 8$  (Model 50D16) patterns—which is also done in some HP and Tektronix analyzers.

Even more information is available in the display generated by the logic-analyzer option to the MDC microprocessor development system from American Microsystems Inc., Santa Clara, CA. A very flexible and high-powered logic analyzer for 6800-Series microprocessor systems, the MDC-140 is also an expensive choice—about \$4000, in addition to \$9600 for the  $\mu$ P development system.

For the additional \$4000, a buyer gets 40 data channels with 1024 traced steps, delay from 0 to 64-k clocks, four clock types with speeds to 10 MHz, and four qualifiers—two to start the delay, one to define clock cycles, and one to trigger external equipment such as an oscilloscope. The display can be in almost any format—binary, octal, hexadecimal, or symbolic.

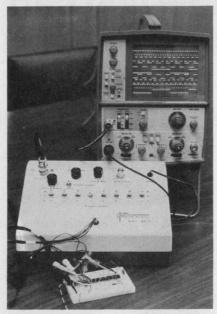
Since the logic analyzer is tied to the microprocessor-development system and its floppy-disc drive, it can even display disassembled instructions—the mnemonics used to program the system—instead of numeric equivalents. That simplifies program tracing.

### Using different microprocessors

Another analyzer, the µscope 820 from Intel Corp., Santa Clara, CA, can not only monitor the activity in a microprocessor-based system but can also modify system parameters and program flow. Housed in an attache case, the 820 is low enough in cost—about \$2000—to be useful in the field.

Preprogrammed maintenance and troubleshooting programs can be executed directly from the instrument's front panel. High-level command keys and operator prompting simplify operation, minimize operator errors, and ease operator training.

The 820 interfaces to the system under test via the microprocessor socket, and the microprocessor itself is plugged into the 820's probe pod. Probe pods and control-panel overlays for 8080 and 8085-type microprocessors



**Eight lines in timing-diagram format** can be displayed on a scope screen with the Kenmark Model RK778—which goes for just \$225.

are available.

One problem with this type of interface is that the  $\mu P$  of the unit under test has to be socketed. Unsoldering the  $\mu P$  will most likely destroy it. Even pulling the microprocessor out of a socket will at least bend pins and at worst destroy the chip through static discharge. A better way to interface with a unit under test is to clip onto

the microprocessor itself without disturbing it mechanically.

That's the usual way with the microprocessor analyzers from AQ Systems Inc., Yorktown Heights, NY. The firm's 6800-type analyzer can be configured to test 6502-type devices by changing the probe. In the same way, the company's 8080-type analyzer can be configured to test 8085s.

The newer of the two analyzers is the AQ8080, priced at \$2550 with an 8080 probe and \$2390 with an 8085 probe. An extra 8080 probe is \$355 and an extra 8085 probe \$495.

The AQ8080 has bidirectional access to a microprocessor's internal registers as well to its memory and I/O ports. It also has a conditional hardware breakpoint and monitor, and can trace up to 128 program steps, with cycle and instruction step modes. Absolutely no memory from the unit under test has to be allocated to the AQ8080's functions. As a result, system design does not have to take the tester into account.

The latest supplier to enter the logic analyzer field is Kenmark Development Group Inc., East Northport, NY. Its Model RK778, an eight-channel real-time analyzer, displays timing diagrams on an external CRT. A glitch catcher can detect positive or negativegoing glitches less than 13 ns long, and the analyzer can operate at up to 20 MHz. Price is \$225.

### **Need more information?**

Not every manufacturer of logic analyzers has been cited in this report, nor has every analyzer made by each of these suppliers been described in detail. For additional details, circle the appropriate number on the Reader Service Card and consult the GOLD BOOK.

American Microsystems Inc., 3800 Homestead Rd., Santa Clara, CA 95051. (408)246-0330. (Ed Barnett) Circle No. 501 Applied Microsystems, P.O. Box 245, Bothell, WA 98011. (206)827-9111. (R. Knoke)

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Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077, (503)644-0161. (Dave Parmley) Circle No. 520 Vector Associates Inc., 685 Station Rd., Bellport, NY 11713. (516)286-9000. (Sheldon Bienstock) Circle No. 521

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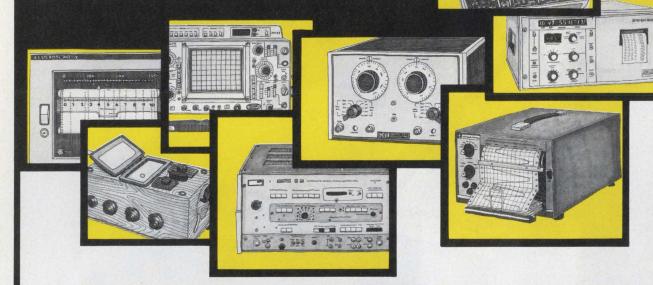
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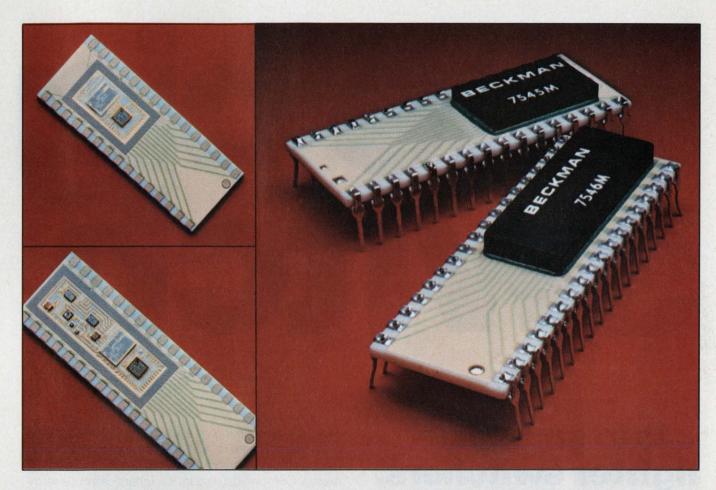
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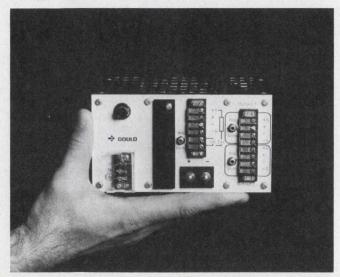
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—102 dBm on the Reference Level. The instrument also provides excellent frequency response on all input circuitry (RF attenuator, preselector and mixer) as well as frequency band gain variations. You can make a choice of scale factors, make amplitude measurement over a 140 dB range +30 dBm to −110 dBm, while benefitting from internal preselection (measuring distortion products as small as 100 dB down and identifying all applied signals) with low distortion. You can also recover modulation waveforms in the time domain, with calibrated sweep times ranging from 10 sec/Div to 2 microsec/Div.

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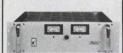


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## A Preview of the Solid-State Circuits Conference

## Forget the bugs in 4-k and 16-k RAMs—the big news is at 64-k

The problems with 4-k RAMs haven't been sorted out, and 16-k RAMs haven't been around long enough for all the problems to surface. Yet the top question at the memory sessions of this year's International Solid-State Circuits Conference (San Francisco, Feb. 15 to 17) will be: Which technology will bring home a 64-k RAM first?

"That level of density is now in active development," says Vir Dhaka, director of Xerox Corp.'s Microelectronics Center in El Segundo, CA. Dhaka is chairman of an ISSCC session designed to "provide a forum for all the approaches to fabricating a 64-k RAM," he says.

Three technologies that could yield

Andy Santoni Associate Editor 64-k RAM devices (which actually store 2<sup>17</sup>, or 65,536, bits) will be described:

- NMOS, the most mature technology, is being used in a device under development at Nippon Telephone and Telegraph Public Corp. in Tokyo.
- I<sup>2</sup>L, a bipolar process, is already yielding 16-k devices at Fairchild Camera and Instrument Corp.'s research and development laboratories in Palo Alto, CA, and may be extended to 64 k.
- VMOS, which researchers have pushed from 1-k to 64-k just in the last year, is actively being developed by both Siemens AG of Munich and American Microsystems Inc., Santa Clara, CA.

Another technology, charge-coupled devices, has also reached the 64-k level, but only in serial memories. Like shift registers, CCDs continuously circulate data and have first-in/first-out access

to stored information, not totally random input and output. Fairchild will describe a buried-channel CCD memory that operates at clock rates from 1 to 5 MHz and uses an eight-phase ripple clock within an interlaced seriesparallel-series structure.

### A straightforward problem

The most straightforward way to achieve 64-k densities in RAMs is NMOS technology, says Dhaka. Many manufacturers with NMOS processing expertise could simply extend this expertise to making 64-k devices, he explains.

But pushing NMOS technology to 64 k, while straightforward, is far from easy. Simply scaling devices down would increase density enough to quadruple bits on a chip from 16 k, but would also have to shrink signal lines to a couple of microns, less than half that of present lines. Otherwise, chips would be so large that defects on any given chip would be inevitable.

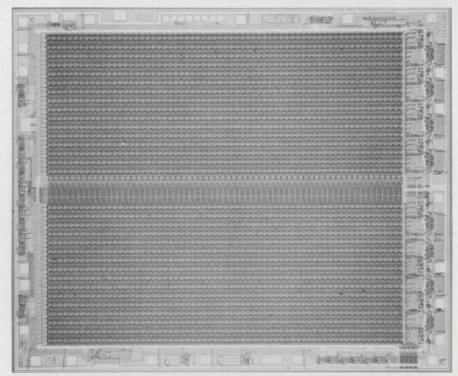
Most researchers are looking to electron-beam or X-ray lithography to gain so great an improvement in line widths.

The Nippon Tel & Tel approach to increasing NMOS RAM density is to make a single-transistor cell and a single-level polysilicon gate with improved photolithography. Prototypes access in 200 ns and dissipate 150 mW.

## Going bipolar

But lower power dissipation at shorter access times may come with I<sup>2</sup>L (integrated-injection logic). Using this technology, Fairchild researchers have already developed a 16-k RAM, organized in a 16,384 × 1-bit array. The device's outputs are compatible with TTL circuits.

Fairchild's' dynamic memory can challenge MOS devices with its 130-ns



The densest static RAM yet is an 8192-bit device from EMM-SEMI. Operating from a single 5-V supply, the device is aimed at microprocessor applications.

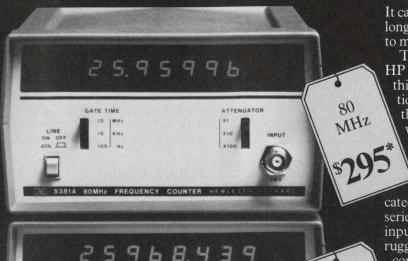
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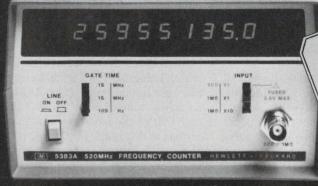
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## Memories at ISSCC

Memory Devices							
Developer	Storage (bits)	Access time (ns)	Power dissipation (mW)	Technology			
Dynamic RAMs Nippon T-T Siemens Fairchild Static RAMs EMM-SEMI Hitachi Nippon Elec. Hughes ROMs Mostek PROMs Intersil	64k 64k 16k 8k 4k 4k 256 64k	200 — 130 300 25 40 — 80	150 — 350 80 350 50 — 150	NMOS VMOS 12L  NMOS TTL TTL Nonvolatile  NMOS CMOS			
Memory Cells							
Developer	Application	Area	Te	Technology			
IBM Signetics Philips Catholic Univ. Leuven SGS-ATES/ Telefunken	16k RAMs Static RAMs ROMs Digital filter ROMS TV tuner PROMS		Bipolar	Josephson junction I <sup>2</sup> L Bipolar punch-through NMOS  Nonvolatile			
CCDs							
Developer	Storage (bits)	Clock rate Package (MHz)		Package			
Fairchild	64k	1-5 16-pin		16-pin			

access time and operation from a single  $5 \pm 0.25$ -V supply. And the device is said to operate over a temperature range of 25 to 75 C.

#### In the groove

However, a 64-k RAM is being brought along with V-groove technology by Siemens AG and American Microsystems. Using existing photolithography, Siemens has fabricated one-transistor memory cells small enough to build a chip that can fit into a standard 16-pin package.

So the technology race for a 64-k RAM is on. Xerox's Dhaka notes that the ISSCC papers indicate that commercial availability is no longer considered pie-in-the-sky or even several years away. But which technology will be first?

"The 64-k RAM, in a shrunk version of NMOS, will most definitely be available," Dhaka believes—"even though users will still come back and say they really can't get good 4-k devices, and that 16-k memories are hard to get at

all." Dhaka predicts sample quantities of 64-k devices trickling out of vendors the second half of this year, with production quantities starting to flow in 1979.

So far the 64-k RAMs closest to production are all dynamic, with all the problems and additional refresh circuitry dynamic operation implies. But density is increasing, albeit more slowly, in static RAMs, too.

#### Larger statics are here, too

The highest-density static RAM now available is an 8-k device from EMM-SEMI Inc., Phoenix. Its aim at microprocessor-based systems is obvious from its organization—1024 eight-bit words.

Chip timing matches the 2-MHz microprocessor requirement, and the chip matches the common I/O and three-state requirements of data-bus systems.

EMM-SEMI applied three concepts to increase performance and density:

Clocked peripheral chip circuitry,

which reduces power consumption, increases speed, and prevents race problems.

- High-value polysilicon resistors, which decrease memory cell size and power.
- A high-performance silicon-gate process, which increases density and performance.

In bipolar static RAMs, the two densest devices are 4-k static circuits from Hitachi Ltd. in Tokyo and Nippon Electric Co. Ltd. in Kawasaki. The Hitachi part has an access time of only 25 ns, yet dissipates a meager 350 mW. Nippon's answer is a 40-ns, 50-mW RAM that improves performance by combining polysilicon self-alignment with diffused-collector, non-epi technology and a local-oxidation step.

### ROMs get bigger

Read-only memories haven't been left behind. A 64-k ROM is being developed at Mostek Corp., Carrollton, TX. Organized as 8192 eight-bit words, it operates from a single 5-V power supply, with a typical access time of 80 ns and power dissipation of 150 mW.

The Mostek part, too, is perfect for microprocessor and minicomputer storage with its 8-bit layout. And its access time is as low as many bipolar parts with less than half the storage capacity.

But no matter how dense a memory gets, it remains basically an array of cells, one per bit. That's why the development of a smaller or faster cell, which by itself has no practical use, is important.

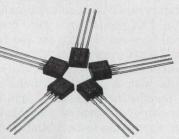
A RAM cell developed at IBM's Research Laboratory in Zurich, for example, uses Josephson junctions to attain an access time of about 15 ns—about half that of the next-fastest RAM described at this year's ISSCC (see table). The cell is intended as a feasibility model for a 16-kbit memory that, with its very high speed and fairly high density, should find a home in interimstorage computer memories.

For high-density static memories, a bipolar cell has been developed at Signetics Corp., Sunnyvale, CA. It measures only about 1 mil (25.4 microns) on a side, and uses I<sup>2</sup>L technology, with four transistors in a single isolated region.

An even smaller cell, for dense bipolar ROMs, has been developed at the research laboratories of Signetics' parent, Philips (Eindhoven, The Netherlands). These cells have areas as small as 100 square microns.

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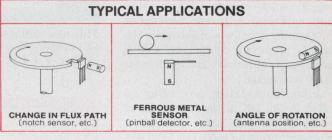


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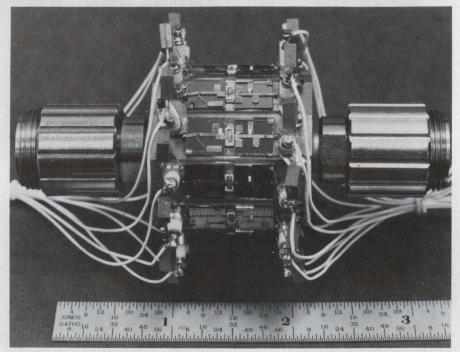


## The new GaAs FETS—less noise, higher power and broader bandwidth

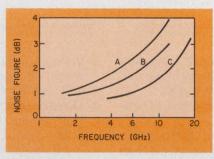
Broader bandwidth, lower noise and higher power are being attained in laboratory versions of gallium arsenide (GaAs) FET amplifiers, with commercial versions trailing not too far behind. What's more, new techniques, like combining a dozen FET amplifier outputs with a radial transmission line, promise to reach new highs in power-output efficiencies. And thanks to new approaches to monolithic GaAs FET IC technology, broadband amplifiers are emerging with direct coupling that requires no matching network. All these FET developments and more will be reported at the ISSCC:

- GaAs FET noise figures range from less than 1 dB at 4 GHz and to 3 dB at 18 GHz in the lab. And theoretically, they may go as low as 0.7 dB for 9.5-W output at 4 GHz. These figures will be achieved with such technological improvements as new active and buffer-layer growth techniques, more uniform batches of substrate material, improved contact reliability, and the use of ternary and quaternary III-V materials.
- Ion implantation, now being applied in the lab to the fabrication of GaAs FETs, may prove superior to current processing methods. At 4 GHz, packaged GaAs FETs prepared by ion implantation have demonstrated 1.1 dB with gains of 12 dB. At 15 GHz, the noise figure rises to only 2.5 dB with a power gain of 7 dB.
- A new kind of dc-coupled device, a monolithic microwave IC for use in instrumentation, has an unusually broad bandwidth from 0 to 4 GHz. Unlike other GaAs microwave FET amplifiers, this device operates without coupling or matching networks. It will be described by R.L. Van Tuyl, project manager for GaAs IC Development at Hewlett-Packard's Santa Rosa, CA, division.

Jim McDermott Eastern Editor



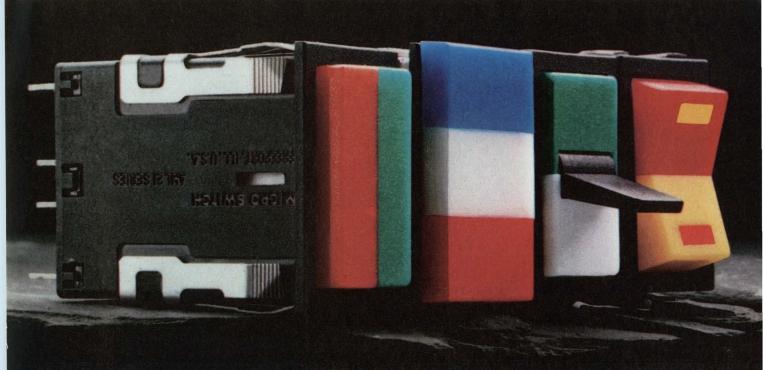
This new radial transmission line combines the outputs of 12 gallium-arsenide FET amplifiers with a combined efficiency of 90%. The device, by Westinghouse, produces 4.4 W and has a bandwidth of 30% at 8.5 GHz.



Performance of commercial  $0.5-\mu$ m-gate devices (B) exceeds that of  $1-\mu$ m units (A). (C) shows laboratory-device figures.

The IC is too tiny to permit inductors and capacitors on the chip. While attempts have been made using bipolar monolithic technology to achieve the same kind of broadband performance, the best previously reported obtained a unity-gain frequency somewhat in excess of 1 GHz. The HP device, on the other hand, has a unity gain of 6 GHz.

- A GaAs multistage amplifier with the broadest bandwidth to date of its kind—7 to 18 GHz—will be reported by S.R. Hennies, engineer at Avantek, Inc., Santa Clara, CA. The device, which has the lowest noise figure of any 18-GHz amplifier at present, uses Avantek's M107 gold metalized GaAs FET chips for a six-stage gain module with an amplification of 28 dB. Power output is over 10 dBm. The FET structures have a 0.5-µm gate length and a 300-µm gate width. A limiter is included in the first stage of the amplifier.
- High-power GaAs MESFETs from Nippon Electric in Japan have an output of 7 W at 5.6 GHz. This unusually high output stems from a simplified recess structure to reduce the drain breakdown, details of which will be



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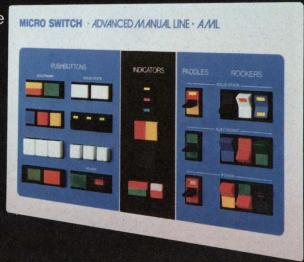
AML has it all -pushbuttons. indicators, and now, paddles and

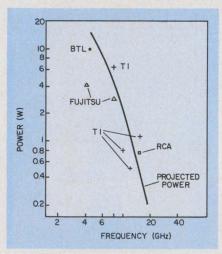
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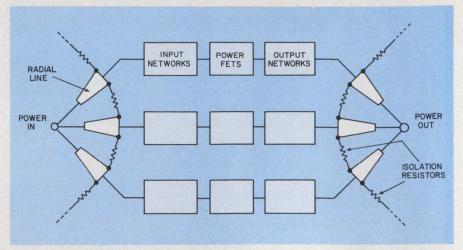


**GaAs-FET power**, projected from devices measured by researchers, will reach 10 to 15 W at 4 GHz and between 6 to 7 W from 8 to 10 GHz.

reported by the Japanese researchers who developed it. An internal matching network is incorporated to improve device efficiency.

■ A 1-W, 2 to 6-GHz amplifier using a discretely packaged MSC8004 GaAs power FET demonstrates that broad bandwidths can be obtained from state-of-the-art packaged commercial devices. The amplifier, which will be described by P.C. Wade, project leader for GaAs FET applications at Microwave Semiconductor Corp. (Somerset, NJ), has 100% (4 GHz) bandwidth and compares with those using chips or chip carriers. The discrete GaAs FET is incorporated in a hermetic stripline package called the MSC Flipac. It is the first commercially available power amplifier to cover such a broad bandwidth in this kind of package.

The MSC Flipac is also one of the



The key advantage of this radial power combiner is that failure of one FET power stage drops power output only 0.8 dB. This feature is achieved through the isolation provided by resistors between sectors. The technique could result in a 100-W amplifier one day.

first power amplifiers to be characterized in terms of large-signal impedance rather than small-signal parameters. And its 15% efficiency is good for broadband amplifiers.

- The design and fabrication of a GaAs amplifier that simultaneously provides relatively high power, bandwidth and efficiency will be described by Texas Instruments researchers. The device, an X-band amplifier operating in the 9 to 10-GHz region is a three-stage microwave IC power FET with 1.6-W output, 20-dB gain and 28% efficiency.
- An idea dating back to the MIT Radiation Laboratory days of the 1940s has been resurrected by the race for GaAs FET amplifier designs with ever higher outputs. The idea is the radial transmission line, the resurrectors are researchers at Westinghouse's Ad-

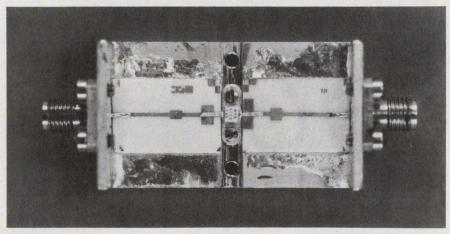
vanced Technology Laboratory in Baltimore. The result is a distributed type of amplifier that combines the power output of twelve 340-mW GaAs FET amplifiers with an output efficiency of close to 90% over a bandwidth of more than 30% at 8.5 GHz.

The radial combining circuitry will be described by James Schellenberg, senior engineer at the Advanced Technology Laboratory and Marvin Cohn, manager of microwave physics at the ATL's Systems Development Division. The circuitry provides both a broader bandwidth and lower loss than other kinds of coupler-type schemes. The radial coupler, designed by Schellenberg, has obtained a loss slightly over 11 dB, which is about 0.25 dB above the theoretical 10.8-dB loss associated with the 12-way power division, and only about 0.05 dB higher than that of a typical single-stage, two-way combiner circuit.

A radial line is used to form the two microstrip power driver/combiners that cap each end of the cylindrical amplifier. The amplifier circuits are arranged around the circumference of these radial circuits and connected to the radial lines by coaxial feed-throughs.

The combiner circuits are built in thin-film form on fused-silica substrates. For a given frequency, the electrical size of the elements is about 50% greater than alumina or sapphire because of the low dielectric constant of the silica material. This increase in effective electrical size provides the proper aspect ratio for the radial combining circuit.

Ideally, the combiner should be a plain disc, fed from  $50-\Omega$  lines. But to



This hermetically sealed stripline package with a GaAs FET amplifier has 100% bandwidth and uses commercial devices by Microwave Semiconductor. The amplifier covers a 2 to 6-GHz band and operates with 15% efficiency.



## -30 dBm sensitivity, FM tolerance standard

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<u>Speed:</u> Fast acquisition and 1 Hz resolution in one second are provided over the entire frequency range.

<u>Discriminator output:</u> Gives the operator a visual picture of any modulation characteristics on the carrier.

Other models: If you don't need 24 GHz coverage, S-D offers four counters starting at \$4,600. (U.S. price only).

To find out more about the performance leaders in microwave counters, call Scientific Devices or contact S-D at 10 Systron Drive, Concord, CA 94518. Phone (415) 676-5000. Overseas, contact Systron-Donner in Munich; Leamington Spa, U.K.; Paris (Le Port Marly); Melbourne.



compensate for differences in amplifier characteristics, the disc has been slotted and  $100-\Omega$  resistors have been connected across the open ends of the slots. Isolation achieved with the radial combiner ranges from 14 to 22 dB, port to port, depending on whether

the two ports are adjacent or opposite.

Although the operating characteristics of the FET devices in the combiner differed substantially, the Westinghouse design was able to match amplifier modules to within 1.2 dB in amplitude and 13° in phase. One de-

sirable feature of this combiner system is that it is "fail safe." Failure of a single FET reduces the net output power by only 0.8 dB. Three device failures reduce it by only 2.5 dB.

This technique is expected to bring a 100-W amplifier one day.

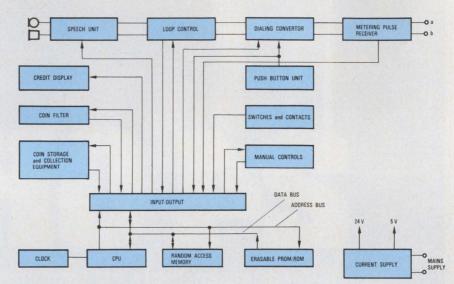
## μP controls pay-phone calls—and collections

A microprocessor enables a new pay telephone to meet the special requirements of different countries—coin denominations, coin materials, rates, signal levels required by switching centers and methods for requesting additional payments. The NT2000 telephone comes from Standard Elektrik Lorenz AG, an International Telephone & Telegraph subsidiary in Stuttgart, Germany.

A microprocessor in the pay telephone controls such elements as the hook switch, additional call button, and keyboard, as well as the coin-handling process, which is signaled by electronic coin filters and detectors in the coin channels.

#### Money tallied, too

The microprocessor also counts tolls paid, determines refunds when necessary, and compares numbers dialed with numbers stored in ROM to determine if the number should be accepted by the coin telephone. In response to the results obtained from its supervisory and computing functions, the  $\mu P$  carries out such control func-



**Coin slots and keypads** in a new telephone from ITT's Standard Elektrik Lorenz AG are under the control of a microprocessor CPU.

tions as controlling deflector and collection magnets in the coin channels.

The microprocessor system includes a CPU, RAM, EPROM, input/output interfaces, and a clock generator. EPROM was selected to shorten program generation time as well as the time it takes to try out prototypes supplied to telephone administrations, according to D. Adolphs, who is in charge of coin-telephone projects at Standard Elektrik Lorenz.

A version of the NT2000 was built with standard CMOS integrated circuits, and a second with custom MOS LSI circuits, Adolphs adds. But the microprocessor simplifies adaptation to customer requirements.

## Dual-laser system improves welding accuracy

A dual-laser system that uses one laser to direct another precisely to its target is being used to weld terminals very accurately and very quickly in telephone switching equipment.

This so-called "edge-detection" system is an optical package that enables the beam from a low-power (1 mW) HeNe laser to scan targets continuously while remaining concentric with the beam of a pulsed high-power Nd:YAG laser. This creates reflections off the targets and these are detected by a photodiode in the optical package.

The system is being used at Western

Electric's Omaha, NE, plant to weld common-bus terminals on a multicontact crossbar switch. Differences in reflectivity between the terminals to be welded and their backgrounds trigger the Nd:YAG laser at exactly the right instant for welding—accuracy is within 0.002 in.

More than 200 welds per second can be achieved with the system, a far cry from the maximum 20 welds per second with current computer-controlled welding systems.

Before edge detection was developed, variations in the size of switches and

in the number of terminals created severe problems for the resistance welding system that was being used. Each variety of switch required a separate indexing installation and elaborate fixturing. Also, resistance welding electrodes had to be replaced and complex part handling mechanisms made for excessive downtime.

Western's edge-detection system, on the other hand, can handle multipart devices that have large cumulative tolerance buildups. It can also handle large variations in component dimensions.

# Tired of selecting 741's and 747's to get premium performance? Specify our OP-02, OP-04, OP-14!

If your design requires premium 741 performance that right now can be met only by a costly and time consuming "selection game," the PMI OP-02 is for you.

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Prices run higher than standard 741's, of course, but well below standard 725's. For a little bit extra you get **guaranteed** better performance across the board, low noise, low drift, low TCV<sub>OS</sub>, low TCl<sub>OS</sub>, and insensitivity to output load conditions. Check the specs

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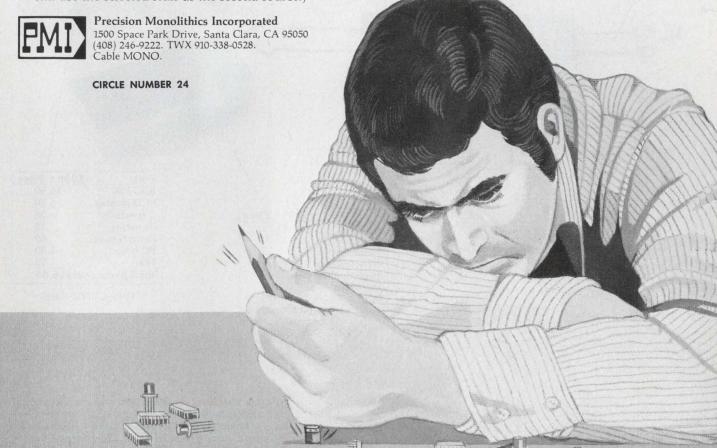
2. Call your PMI distributor for a few OP-02's to convince yourself that PMI's specs are for real.

3. Specify the OP-02 as the **preferred** source. (You can still use the selected stuff as the second source.)

	Input Offset Voltage mV MAX		Input Offset Current nA MAX		Input Bias Current nA MAX	
esta di kata	MIL	Comm.	MIL	Comm.	MIL	Comm.
Industry Standard 741	6.0	7.5	500	300	1500	800
PMI SSS741	3.0	7.5	10	50	100	200
PMI OP-02	1.0	3.0	5	10	50	100
Industry Standard 725	1.5	3.5	40	50	200	250
PMI SSS725	0.18	1.6	4	25	120	180

## **DUALS** also available!

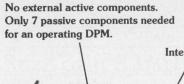
Standard	Superior Second Source	Premium Performance
747	SSS747	OP-04
1458/	SSS1458/	
1558	1558	OP-14

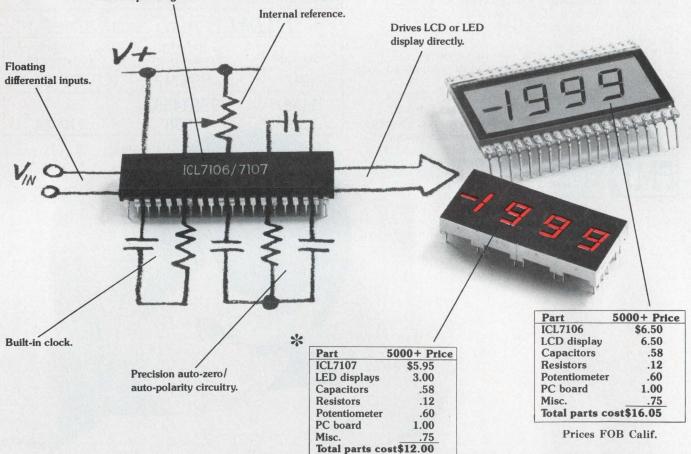


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## U.S. to keep patent rights to government-funded R&D

The Carter Administration has informed Congress that it will continue the policy of retaining title to patents stemming from federally financed research and development, and will not assign title to the inventors, who would then license the government to use the results.

A controversy has raged for 30 years over these two approaches to patent rights for government-sponsored inventions, according to John H. Shenefield, assistant attorney general in charge of the Justice Department's Antitrust Division, in testimony before the Senate monopoly subcommittee. Under the "title" policy, favored by the Justice Department, the government takes title to the patents involved, and private interests may use the inventions by obtaining a government license. Under the "license" policy, which is backed by some government contractors, the contractor gets title to the invention, with the government retaining a royalty-free license. But the contractor doesn't have to license its use by any third parties.

Shenefield argued that the "title" policy best ensures that when the government underwrites R&D, the public receives the benefits. Under the "license" policy, he claimed, "the public would pay the contractor twice—first through the governmental research support and then again through the patent-monopoly surcharge in the marketplace, which is reflected in the price the public pays for goods subject to that surcharge."

## Ten firms vie to integrate MX missile guidance

Ten companies are competing for a development contract to integrate the guidance and control system in the new MX mobile intercontinental ballistic missile, and the Air Force expects to select at least two companies for parallel efforts by May.

The highly accurate guidance system, known as the Advanced Inertial Reference Sphere (AIRS), has been developed by the Charles Stark Draper Laboratory, and prototypes have been built by Northrop Corp. The two winning contractors will study linking the AIRS system with an inertial measurement unit developed by Honeywell's Aerospace Division and mission-oriented software.

In the running for the guidance-integration contract are Litton Industries, General Motors' Delco Electronics Division, Northrop, Rockwell International's Autonetics Group, Raytheon, General Electric, Boeing, Texas Instruments, Bendix, and Hughes Aircraft.

After an initial system definition phase, which is expected to run through December, the Air Force can exercise a contract option for one firm to continue with engineering development of the system through September, 1983. However, this will depend on the availability of funds in this year's defense budget. Although Defense Secretary Harold Brown has not yet approved the MX concept for engineering development, the Air Force is trying to define all the missile subsystems during this calendar year in anticipation of development funds in next year's budget. Brown has been reluctant to push ahead with MX until the SALT negotiations with the Soviet Union over strategic weapons are concluded.

Another key MX contract to be awarded in May will cover missile assembly, test and system support. It will also run through December, with an option to extend it through September, 1983. Competitors are Boeing, Rockwell, GTE Sylvania and Martin Marietta's Denver Division.

## Five aircraft land automatically in Atlanta

The first fully automatic multiple landings under zero-visibility weather conditions have been conducted at Atlanta's Hartsfield Airport. According to the Federal Aviation Administration, five Lockheed L-1011s, four from Delta Airlines and one from Eastern Airlines, performed full Category III instrument landing operations, which means that the landings were automatic right down to the application of brakes after touchdown.

The weather conditions during the landings satisfied the minimum requirements for full CAT III operations: clouds on the ground, recorded as zero ceiling, and a visual range on the runway between 700 and 1200 feet.

## Weather satellite needed for global project

Western European and American space scientists are trying to come up with a synchronous-orbit weather satellite to replace the Soviet satellite that was supposed to be part of the 1979 Global Atmospheric Research Program.

GARP is scheduled to begin next Jan. 1 to collect weather data for a year from a variety of sources, including five satellites in synchronous orbit 22,300 miles above the earth. Four of the weather satellites are already orbiting, but last month the Soviets informed World Meteorological Organization (GARP sponsor) that they wouldn't be able to launch their satellite until late 1979, almost a year behind schedule.

All four orbiting satellites were launched by the National Aeronautics and Space Administration—two for the National Oceanic and Atmospheric Administration (NOAA), one for Japan and one for the European Space Agency (ESA). One possible fifth is another NOAA weather satellite, due to be launched in May this year.

## Capital capsules: The National Science Foundation will replace its Directorate for Research Applications on Feb. 6 with a Directorate for Applied Science and Research

Applications in an attempt to strengthen the links between the Foundation's basic research activities and applied research needs. Dr. Jack T. Sanderson, assistant NSF director for research applications, will head the new organization....The National Bureau of Standards will sponsor a conference on microcomputer-based instrumentation at its Gaithersburg, MD, head-quarters June 12 and 13. Co-sponsors are the IEEE Computer Society and the Group on Instrumentation and Measurement....NASA is turning its launching of satellites into a profitable business. Of the agency's 25 launches scheduled for 1978, 15 will be "paying customers," including the European Space Agency, Comsat Corp., Japan, the United Kingdom, Canada and other U.S. government agencies.

## Now...LOOK at GPIB Activity:

ASCII decoded device dependent message transmitted over data bus

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7DO1 TRIG +133 GP IB \$30 REN 0 0 ø 0 CR 000 #0 A #3 F EOI. ATH UNL REN 0000 LAG CR 9999 ATN SRQ 00000 TRIG 3710

Service request when asserted

End or identify when asserted

4 user definable lines

Remote enable when asserted

Announcing visible GPIB communications at the touch of a button: the new TEKTRONIX DF2 Display Formatter. The DF2 monitors and displays activity on the GPIB bus as disassembled instructions in familiar IEEE 488 mnemonics.

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## Designing A Controller? Use The DF2!

It's plug-to-plug compatible with GPIB controllers so you monitor commands at a glance.

## Designing Talkers/Listeners? Use The DF2!

Now it's simple to make sure talkers are responding properly to the controller and listeners are receiving correct data.

## Integrating GPIB Systems? Use The DF2!

You know monitoring and displaying bus events and their sequence are essential for effective integration of multi-vendor GPIB products. Now you have the essential tool: use the DF2 to analyze any specific data transaction you wish.

You'll also find the DF2 a powerful service tool. Observe GPIB bus activity to simplify troubleshooting and keep your system up and running properly.

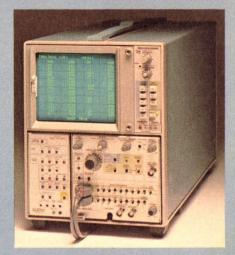
The DF2 Display Formatter also provides displays in timing and mapping modes as well as state tables in binary, hexadecimal, or octal notation. Combined with the DF2, our 7D01 Logic Analyzer is the most comprehensive and versatile logic analysis tool available today. And because the 7D01 Logic Analyzer System is compatible with any TEKTRONIX 7000 Series oscilloscope, you may already own part of a Logic Analyzer package.

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Before you design-in a Z-80, 6800 or 8085, compare it with the high performance R6500.

Rockwell's R6500 delivers boosted performance and economics through its third-generation pipelined architecture with 13 powerful addressing modes, true indexing capability, complete decimal/binary arithmetic mode selection, on-chip clock and proven 2MHz performance. Prove it to yourself - Benchmark it!

## R6500 offers innovative architecture and technology.

The 8-bit R6500 is produced with N-channel, silicon gate, depletion load technology and innovative architecture. The result is smaller, faster chips to keep your system costs down and performance up.

A family of ten software compatible CPUs in 28- and 40-pin DIP packages give you the most cost-effective fit for your application. Prove it to

yourself-Price it!

## R6500 is designed for greater memory and I/O efficiency.

Of the leading NMOS microprocessors, only the R6500 has 13 addressing modes and true indexing capability. More addressing modes coupled with an advanced instruction set makes programming the R6500 easy and efficient. Fewer program steps means lower memory cost and faster program execution.

R6500 memory-managed I/O eliminates performance bottlenecks associated with the separate I/O buses, I/O commands and register over-

head required by other microprocessors.

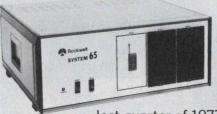
A broad selection of memory, I/O and combination memory-I/O-timer circuits are available. And Rockwell is presently delivering the industry's first fully static 32K ROM – the R 2332 – and the industry's fastest 32K ROM—the R2332-3.

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SYSTEM 65 Microcomputer Development System is efficient and easy-to-use and is equipped with dual mini-floppies. It's priced at only \$4800.

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Industry researchers say the multiplesourced 6500 outshipped the Z-80, 6800 and 8085 during the last quarter of 1977. Benchmark it!

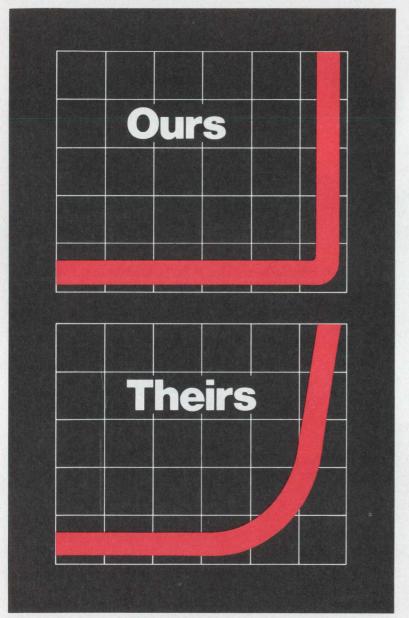
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## **Editorial**

## Concepting an idea

A fellow telephoned for help the other day. He was trying to find new applications for his company's product and—I swear he said this—he was "concepting an idea."

Well, I wanted to help, but I stumbled on his "concepting an idea," so I asked him to explain. I shouldn't have. His explanation befuddled me even further. As far as I could determine, he was doing market research. But on his company's Table of Organization he no doubt shows up as the man who concepts ideas, which is more "scientific." And the club of idea conceptors is certainly more exclusive than the club of market researchers.



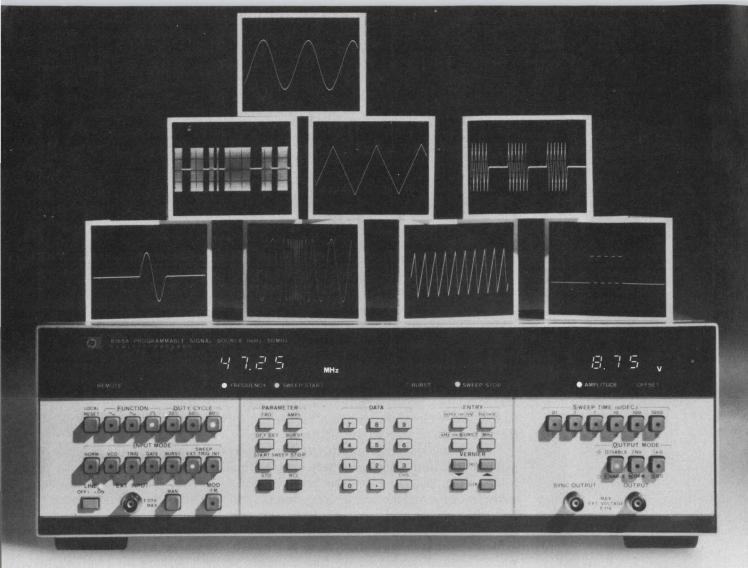
Though any specialty certainly requires specialized language, the practice of using obfuscating language where simple English would do has been with us a long time. Doctors code their prescriptions in Latin to keep understanding away from you and me, and lawyers write in gobble-de-gook for the same reason.

Nowhere is the practice spoofed more effectively than in the chapter-heading quotations in Max Shulman's delightful Barefoot Boy with Cheek. In French—for French is more "literary" than English—Shulman quotes some of the world's great Frenchmen. We find Rabelais saying "Le livre est brun" ("The book is brown"), Voltaire saying "Le crayon est sur le table" ("The pencil is on the table"), and Anatole France asking "Ou est mon chapeau?" ("Where is my hat?") Had Shulman thought of it, I'm sure he could have done something with "concepting an idea" or some of the language we engineers use to befuddle and intimidate our neighbors.

Let's eschew obfuscation.

hour Kouthey

GEORGE ROSTKY Editor-in-Chief



Instrument shown with optional sweep mode

## Now, quickly program these waveforms...

# Using HP's new 8165A, the first programmable signal source with a 0.001 Hz to 50 MHz range.

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The 8165A, priced at \$6000\*\*, also gives you high accuracy, eliminating the need for time-consuming setup verification with expensive counters and volt meters. Contact your local HP field engineer for complete details.

\*HP's implementation of IEEE Standard 488-1975

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## **Reduce your** $\mu$ **C-based system** design time by using single-board microcomputers. Assembled boards in the SBC-80 series offer stock answers to custom demands.

System designers eager to take advantage of the dramatically increased capabilities of microcomputers have been hindered two ways: Their production volumes have been too low to amortize software and hardware development costs effectively, or hardware subtleties and test requirements have confined them to fully assembled and tested computer subsystems. But now those obstacles are overcome with families of fully assembled and tested microcomputers and system-expansion boards like the Intel SBC-80 series. They are ready-to-use, flexible and inexpensive—prices range from just \$195 to \$825 in unit quantities.

The main members of the SBC-80 family are the 80/04, 80/05, 80/10A, 80/20 and 80/20-4 central-processor boards, with either an 8080A or 8085 microprocessor acting as the master CPU (Table 1). Most of the boards measure  $6.75 \times 12$  in. and contain the CPU, clock, read/write memory, control ROM, I/O ports, serial communications interface and bus-control logic.

I/O interfacing is an area where design flexibility is essential to meet changing requirements efficiently. The programmable parallel and serial I/O structures of the boards make them versatile enough to do just that. What's more, upgrading system performance is easy thanks to the SBC-80 system bus, the Multibus, which permits modular performance expansion.

The Multibus provides a defined, standard interface between the SBC-80 single-board computers and expansion boards. As many as 16 SBC-80 family boards can simultaneously share the bus.

### All in the SBC-80 family

As exemplified by the block diagram of the SBC-80/10A (Fig. 1), the SBC-80 microcomputer system has all that's needed for many applications. The SBC-80/10A is the oldest board in the family and has been widely imitated since it was one of the first "standardized" microcomputers commercially available.

The CPU section of the 80/10A board consists of

the 8080A CPU, the 8224 clock generator and the 8238 system controller. Capable of fetching and executing any of the 8080A's 78 instructions, the CPU section can respond to interrupt requests originating on and off the board. (For more about the 8080A, see "Microprocessor Basics, Part 2," ED No. 10, May 10, 1976, p. 84).

The system-bus interface section includes an assortment of circuits to gate the interrupt and hold requests, the ready signals, and a system-reset signal. Other circuits drive the various control lines. Two 8216s help drive the bidirectional data bus, and six 8226s drive the external system-data and address buses as part of the SBC-80/10A's Multibus interface.

The RAM section of the 80/10A consists of 1024 bytes of static MOS memory. For program storage, up to 8192 bytes of ROM can be mounted on the board in 1024-byte increments by means of a 2708 or 8708 EPROM, an 8308 mask-programmed ROM, or in 2048 byte increments via the 2716 EPROM or 2316 ROM.

A serial interface on the board uses an 8251 programmable universal synchronous/asynchronous receiver/transmitter to provide a serial-data channel. The serial port operates at programmable rates up to 38,400 baud (synchronously) or 19,200 baud (asynchronously) with a choice of character length, number of stop bits, and even, odd or no parity. On-board interfaces provide direct EIA RS-232 or teletypewriter current-loop compatibility.

Two 8255 programmable peripheral interface circuits provide 48 I/O lines for transferring data to or from peripheral devices. Eight already-committed lines have bidirectional drivers and termination networks permanently installed, so that they can be inputs, outputs or bidirectional (jumper-selectable). The other 40 lines are uncommitted. On-board sockets permit drivers and termination networks to be installed, as needed. Since software configures the I/O lines, I/O can be customized for every application.

The 80/10A also responds to a single-level interrupt that can originate from one of many sources, the USART, programmable I/O and two user-designated interrupt-request lines. When an interrupt is recognized, a Restart-7 instruction is generated, and the processor accesses location  $38_{\rm H}$  to get the starting address of the service routine.

System expansion and support are possible with a

George Adams, Product Line Manager, Single-Chip Micro-computers, Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051.

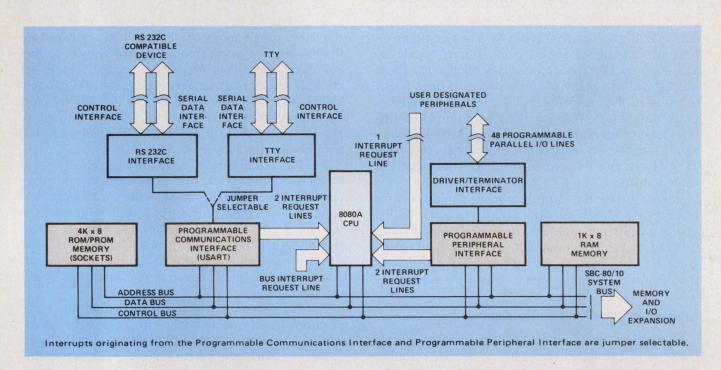
wide variety of alternate-source CPU, memory, and I/O boards (Tables 2 and 3). Up to 65,536 bytes of ROM, PROM or RAM can be accessed by one 80/10A. Expandable backplanes and card cages are also available to support multiboard systems.

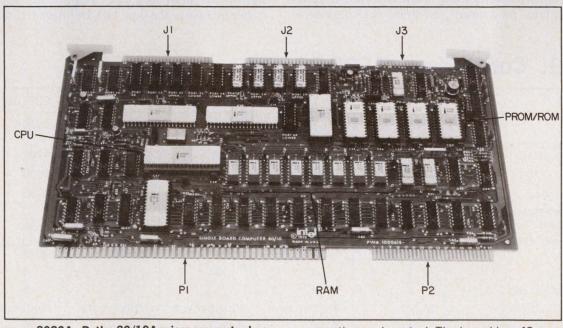
### Interfacing starts with the bus

Although the SBC-80/10A is a complete microcomputer system, it can be expanded readily or it can serve as a primary master controller for other microcomputer cards. The 80/10A has five edge connectors, three on the top of the board and two on the backplane, or bottom, side. Two of the "top" connectors,  $J_1$  and  $J_2$ , serve as parallel I/O ports, while  $J_3$  is a serial I/O port. All parallel I/O lines on the 50-contact  $J_1$  and  $J_2$  connector areas are paired with an independent signal/ground pin to permit alternate signal/ground wiring when using flat-cable interconnects. Serial port  $J_3$  uses a 26-contact PC-edge connector to provide interfaces for both RS-232 and current-loop devices.

To communicate with other system-compatible boards, the 80/10A uses the 86-pin Multibus ( $P_1$ ). To provide accessible test points, the 80/10A has a 60-pin edge connector ( $P_2$ ). The control signals on the Multibus provide the real power and capability in control applications.

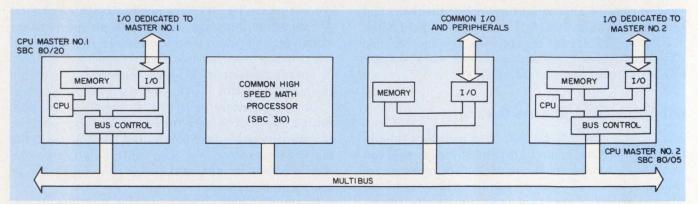
Of the 86 pins that make up the Multibus, 24 are assigned to power and ground, 16 to addressing, eight to bidirectional data, and 12 to signal and control





1. Based on an 8080A µP, the 80/10A microcomputer has a straightforward design suitable for general-purpose

computing and control. The board has 48 programmable I/O lines and serial interfaces.



2. The Multibus interface for the SBC-80 CPU boards not only permits simultaneous multiprocessing, but also enables several processors to share the same bus and

peripheral devices. Arbitration logic on the CPU boards decides which board gets on the bus first if several units simultaneously access the bus.

(these 12 are defined in Table 4). The remaining 26 pins are unassigned at this point. Higher capability SBC-80 products, though, are in development. These boards will use many of the unassigned lines (eight unassigned pins are allocated for additional bidirectional data lines). The remaining lines provide multilevel (eight) interrupt lines, various control lines and a multimaster, bus-arbitration control structure (Fig. 2). Address and data lines are three-state, and the interrupt and control lines are open-collector.

Boards using the Multibus have a master-slave relationship: A bus master—such as an SBC 80 CPU board, a DMA controller or a diskette controller—can control the command and address lines. Conversely, slave boards—such as a memory, I/O-expansion or mathematics boards—cannot control the bus.

#### Arbitration resolves priority disputes

In multimaster systems, the bus-arbitration logic uses the  $\overline{\text{CCLK}}$  signal of the bus to provide a timing reference to help satisfy many simultaneous requests for bus control. As a result, different speed masters

can share resources on one bus. Actual transfers on the bus proceed asynchronously with respect to the bus clock. Once bus access is granted, single or multiple read/write transfers can proceed at up to 150 kbytes/s for CPU operations and up to 1 Mbyte/s for DMA operations. The bus has a bandwidth of 5 Mbytes/s so that future performance enhancements may be directly supported.

Both serial and parallel modes of bus-priority resolution are available. In the serial mode, up to three masters can share the system bus, with requests ordered on the basis of bus location. Each master on the bus notifies the next one down in priority when it needs to use the bus, and monitors the bus-request status of the closest higher-priority master. With an external priority network, up to 16 masters can share the bus.

The dual-bus nature of the Multibus permits each processor-based master within the system to retain its own local memory and I/O, which it uses for most operations. Such local operations occur entirely on the individual board and don't require the system bus.

In contrast to the dual bus architecture, all masters

Table 1. Comparison of SBC-80 CPUs

	SBC 80/04	SBC 80/05	SBC 80/10A	SBC 80/20	SBC 80/20-4
CPU	8085	8085	8080A	8080A	8080A
EPROM capacity (bytes) (with 2716)	4096	4096	8192	8192	8192
(with 2708)	2048	2048	4096	4096	4096
RAM (bytes)	256	512	1024	2048	4096
Programmable parallel I/O lines	22	22	48	48	48
Serial I/O capability	RS232C SID/SOD <sup>1, 2</sup>	RS232C SID/SOD <sup>1, 2</sup>	RS232C/TTY USART	RS232C <sup>2</sup> USART	RS232C <sup>2</sup> USART
Timers	1	1	0	2	2
Interrupt levels	4	4	1	8	8
Multibus interface	None	Multi-master	Single-master	Multi-master	Multi-master
Price (unit quantity)	\$195	\$350	\$495	\$735	\$825

Notes: <sup>1</sup>Provided by 8085 CPU SID and SOD serial I/O lines. <sup>2</sup>Optional SBC 530 TTY interface is available.

Table 2. Additional SBC support boards

		ar obo support be	
Function	Model	Description	Price (unit qty)
RAM	SBC 016 SBC 032 SBC 048 SBC 064 SBC 094*	16 kbyte dynamic RAM 32 kbyte dynamic RAM 48 kbyte dynamic RAM 64 kbyte dynamic RAM 4 kbyte CMOS static RAM with 96 hour battery backup.	\$ 825 \$1360 \$1860 \$2200 \$ 795
EPROM	SBC 416	16 kbytes using 2708 type (1024 x 8) EPROM	\$ 295
Digital I/O	SBC 508*	32 input lines/32 out- put lines, all buf- fered/terminated	\$ 350
	SBC 517	48 programmable par- allel lines with full buffering/termination options, full RS232C port, 1 ms real-time clock, and 8-line inter- rupt control	\$ 400
	SBC 519*	72 programmable parallel lines with full buffering/termination options, real-time clock (interval is jumper selectable to 0.5, 1, 2, or 4 ms), and 8-level programmable interrupt control.	\$ 395
Communications	SBC 534	Four programmable synchronous/asynchronous serial ports, each with: programmable baud rates, programmable data formats, programmable interrupt control, 16 RS232C buffered programmable parallel I/O lines configured as a Bell Model 801 automatic calling unit interface. Two programmable 16-bit interval timers (usable as real-time clocks), and software selectable loopback of serial ports for diagnostic use.	\$ 650
	SBC 556*	48 optically isolated lines; 24 input 16 output, and 8 programmable (in/out), 8-level programmable interrupt control, and 1 ms real-time clock.	\$ 395
Analog I/O	SBC 711*	16/8 (single-ended/differential) 12-bit a/d channels; user expandable on-board to 32/16 channels	\$ 895
	SBC 724*	Four 12-bit d/a chan- nels	\$ 750
	SBC 732*	Combination analog I/O; same a/d capability as SBC 711 plus 2 d/a channels	\$1125
Combination memory and I/O	SBC 104	8 kbytes capacity (sockets) using 2716 (2 k x 8) EPROM or 4 k using 2708, 4 kbytes dynamic RAM, 48 programmable parallel I/O lines, with full buffering/termination, as options. RS-232C port, a 1 ms real-time clock, and an eight-line interrupt control	\$ 715

in multimaster/single-bus systems use the common bus for all instruction or data fetches or whenever data must be written to output devices or memory. Rapidly, then, the system bus becomes the bottleneck for over-all system throughput. Masters in SBC-80 systems only use the Multibus when data or instructions are resident in common, or global, memory or I/O. Since masters can request the Multibus simultaneously, on-board arbritration logic resolves any multiple contention.

### **Examine board performance**

A look at the entire family of SBC-80 micro-computers reveals varied levels of performance. All five boards are inexpensive, but the most inexpensive is the 80/04, which costs \$99 in 100-unit quantities, and is intended for stand-alone applications. To get the cost down, the board was designed to use the 8085 CPU and the 8155 RAM, timer and I/O circuit.

The 80/04 contains an 8085 CPU, 256 bytes of RAM, space for up to 4 kbytes of EPROM (two 2716 EPROMs, or four 2708 EPROMs), 22 programmable parallel I/O lines with sockets for buffer and termination options, a 14-bit programmable timer/event counter, and provision for an RS-232-C serial port using the 8085 SID/SOD serial interface. The board can also house an on-board +5-V regulator, so an unregulated voltage can be connected.

The next step up, the 80/05, has the same architecture and connector types and pinouts as the 80/04. Direct software compatibility is achieved with the same CPU along with the same RAM, ROM, I/O, and timer addressing. However, the 80/05 contains twice as much RAM as the 80/04. And since the 80/05 has the full Multibus multimaster interface, 80/05-based systems can be expanded with any of the Multibus-compatible boards from Intel or other suppliers.

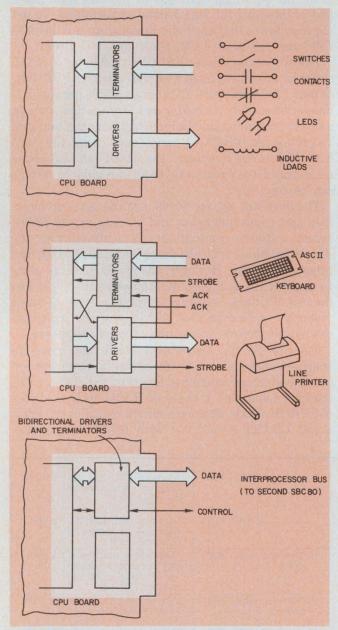
The SBC-80/10A comes next. It provides more onboard memory and I/O for systems requiring expanded on-board resources. Based on the 8080A CPU, the board contains 1 kbyte of RAM, up to 8 kbytes of EPROM/ROM, 48 programmable parallel I/O lines, a full USART serial port with RS-232-C and tele-

ST. S. Mar. C.			
	SBC 108	Same as SBC 104, except has 8 kbytes of dynamic RAM	\$ 815
	SBC 116	Same as SBC 104, except has 16 kbytes of dynamic RAM	\$ 985
High-speed math	SBC 310*	High speed mathematics processor including floating-point capability (32 bit).	\$ 595
Peripheral control	SBC 201	Dual single-density dis- kette controller	\$ 995
Silver the	SBC 202	Quad double-density diskette controller	\$1290
DMA control	SBC 501	DMA controller, up to 1 MHz transfer rates	\$ 450
	Peripheral control	SBC 116  High-speed SBC 310* math  Peripheral SBC 201 control SBC 202  DMA SBC 501	cept has 8 kbytes of dynamic RAM  SBC 116  Same as SBC 104, except has 16 kbytes of dynamic RAM  High-speed math math  BBC 310*  High speed mathematics processor including floating-point capability (32 bit).  Peripheral control  SBC 201  Dual single-density diskette controller  SBC 202  Quad double-density diskette controller  DMA  SBC 501  DMA controller, up to

\*Requires +5 V only.

typewriter interfaces, and a full Multibus interface (but only single-master capability; the board has no multimaster capability). Intended for single-CPU systems with only one other Multibus peripheral controller, the 80/10A can interface with such as the SBC-201 or SBC-202 single and double-density diskette controllers, or the SBC-501 DMA controller.

System designers requiring the same on-board I/O capability as the SBC-80/10A but with more RAM, more efficient real-time capability, and full multimaster Multibus control can go further up the ladder to the SBC-80/20 or SBC-80/20-4. These boards differ only in that the 80/20 contains 2 kbytes of RAM and the 80/20-4 contains 4 kbytes. Both boards can hold up to 8192 bytes of ROM (21)or EPROM, handle up



3. Programmable I/O lines from the SBC-80 parallel interfaces can be set so that they are individually programmable as inputs or outputs (a), byte-programmable as inputs or outputs with handshaking (b), or bidirectional on a byte-programmable basis (c).

to eight levels of prioritized interrupt, and share the Multibus in the multimaster mode. Either board has two programmable interval timers/event counters. Auxiliary power buses and memory-protect control logic on the board permit battery backup of the RAM.

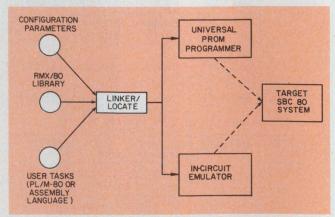
### Take advantage of interrupts and timers

Real-time applications frequently require that high-priority programs operate on the basis of external events, time-of-day, or elapsed time without impacting current background processing. These multi-programming requirements are supported in the 80/20 and 80/20-4 by an eight-level programmable interrupt controller (PIC) and two programmable interval timer/event counters. The priority level of any event generating an interrupt request is assigned through jumper selection and the priority algorithm chosen by system software.

Any combination of interrupt levels may be masked by storing a single byte in the interrupt-mask register contained by the PIC, whose four software-selectable priority algorithms are described in Table 5. The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 bytes (software-selectable). The resulting 32 or 64-byte block may begin at any 32 or 64-byte boundary in the 65,536-byte memory space. A single 8080A jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory.

The two programmable timers may be used to generate real-time clocks by requesting periodic interrupts through the PIC, so that the CPU is free to handle numerous other system-timing and control functions. The outputs and gate/trigger inputs of the timer/counters can be routed via jumpers to the PIC, the I/O driver/terminators, or the programmable parallel I/O.

Seven software-selectable timing/counting functions are available. Either timer may be set to act as a rate generator (divide-by-N counter), a square-wave



4. **By using the RMX-80 executive** and the library of oftenused subroutines, program development can be simplified since the subroutines are modular and can be linked together, then checked out in a system prototype.

Table 3. Non-Intel SBC-compatible boards

Manufacturer	Multibus CPU boards	RAM boards	Core memory boards	PROM/ROM boards	Analog boards	AC power control boards	IEEE-488 bus	Tape interface	Floppy-disc controller	Communications interface	Video boards	Math processors	Breadboards	Circle no.
ADAC Corp., 118 Cummings Park,			1	. See	•		100				1000	1100		451
Woburn, MA 01801.(617) 935-6668  Ampex, Memory Products Div., 200 N. Nash St., El Segundo, CA 90245.(213) 640-0150			•											451
Analog Devices, Route 1 Industrial Park, P.O. Box 280, Norwood, MA 02062.(617) 329-4700			70		•									453
Augat Inc., 33 Perry Ave., P.O. Box 779, Attleboro, MA 02703.(617) 222-2202		Lagar E	-12 7			170		No.			i i		•	454
Burr-Brown, International Airport Industrial Park, P.O. Box 11400, Tucson, AZ 85734. (602) 294-1431		The same			•		6.0					2 4 4		455
Cybernetic Microsystems, 2460 Embarcadero Way, Palo Alto, CA 94303. (415) 321-0410		EAR	Sug		•					N.		•		456
Data Translation Inc., 23 Strathmore Road, Natick, MA 01760-(617) 655-5300			in	9=10	•	7134	party.	57%	10 9	100	722			457
Datacube Corp., 25 Industrial Park, Chelmsford, MA 01824. (617) 256-2555											•			458
Datel Systems Inc., 1020 Turnpike St., Building S., Canton, MA 02021.(617) 828-8000			Ma	le file	•	Pag.			27128	2	h			459
Digidata Corp., 8580 Dorsey Run Road, Jessup, MD 20794. (301) 498-0200				Is.			•		1					460
EDAC Corp., 1417 San Antonio Ave., Alameda, CA 94501.(415) 521-6600		2113 2									•			461
Electronic Engineering & Prod. Services, TE. #2, Louisville, TN 37777. (615) 984-9640						•								462
Electronic Solutions, 7969 Engineer Rd., San Diego, CA 92111.(714) 292-0242	•	•		•		out.			LAST.	b like		Halife		463
Garry Mfg. Co., 1010 Jersey Ave., New Brunswick, NJ 08902.(201) 545-2424													•	464
Hal Communications Corp., Box 365B, 807 E. Green St., Urbana, IL 61801.(217) 367-7373		lynd.					7			MA	•			465
lasis, 815 W. Maude Ave., Sunnyvale, CA 94086. (408) 732-5700	•									MIL			J.F.	466
ICOM, 6741 Variel Ave., Canoga Park, CA 91303.(213) 348-1391			P. I				1000		•					467
Megalogic Corp., 9650 National Road, Brookville, OH 45309.(513) 833-5222					18			•		1				468
Micro Memories Inc., 9438 Irondale Ave., Chatsworth, CA 91311.(213) 998-0700			•			214					N. A.			469
Microtec, P.O. Box 60337, Sunnyvale, CA 94088.(408) 733-2919				•										470
Monolithic Systems Inc., 14 Inverness Drive, East, Englewood, CA 80110 (303) 770-7400	•	•												471
National Semiconductor, 2900 Semiconductor Drive, Santa Clara, CA 95051.(408) 737-5000	•						7 19							472
North Star Computers Inc., 2465 Fourth St., Berkeley, CA 94710 (415) 549-0858												•		473
The Thomas Engineering Co., 1201 Park Ave., Emeryville, CA 94608.(415) 547-5860										•				474
Vector Electronic Products, 12460 Gladstone Ave., Sylmar, CA 91342.(213) 365-9661			Je!										•	475
Zia Tech., 10762 La Roda Drive, Cupertino, CA 95015. (408) 996 -7082			100											476

generator, a programmable retriggerable one-shot, or software or hardware-triggered strobe. One of the timers can be jumper-selected as an event counter, and either can generate an interrupt after a specified interval or after a specified number of events.

The programmability of each on-board timer allows timing intervals from approximately 2  $\mu$ s to over 60 ms. But the two timers may be cascaded to provide intervals greater than 1.1 hour, in 1.86  $\mu$ s increments. In the event counter mode, external event rates up to 1.1 MHz may be counted.

# Flexible I/O, a must for any system

All SBC-80 microcomputers provide 22 or 48 programmable parallel I/O lines that, grouped as 8-bit ports, are fully programmable to allow enough flexibility to handle any changes in system interfacing. Programmability is permitted through data direction, control mode, interrupt handling, and buffer/termination. The I/O configuration for a specific application is selected through software initialization of the parallel I/O control logic, jumper selection of control/interrupt line routing, and the particular buffer and termination devices chosen.

Fig. 3 illustrates the basic modes of operation that may be selected by software to meet application requirements. Mode 0 is used for slow-to-medium-speed interfacing where immediate handshake response or interrupt generation is not needed. This mode is extremely useful for interfacing to inputs such as switches or outputs such as LED indicators or numeric displays.

Mode 1 provides handshaking lines required for many medium to high-speed peripherals. A typical output function could be a line printer; an input device could be an encoded keyboard or paper tape reader.

In addition, the 80/10A and 80/20 have Mode 2, a bidirectional data/control structure. This interface may provide, for example, a communication link between parallel processors.

The SBC-80 I/O structure also permits multiple options for output buffering and input termination. TTL drivers with 16 to 48 mA of drive can be used, and input lines may be terminated to minimize the impact of noise and cable disconnects. Any of the TTL drivers (four outputs) or input terminators (for inputs) listed in Table 6 may be inserted into sockets to provide proper buffering or termination.

Like the design flexibility of the SBC-80 parallel I/O structure, the serial I/O structure allows interface characteristics to be revised rapidly through software, jumper, and buffer changes. Besides the SBC-80/10A, the 80/20 and 80/20-4 contain the USART serial channel. These boards provide RS-232 interfaces, but the SBC-80/10A also has a teletypewriter current-loop interface. Synchronous/asynchronous mode, data format, control-character format, and parity are all under program control. So is baud rate on the 80/20 and 80/20-4. Baud rate is jumper-selectable on the

# Table 4. Multibus control signals

	Ti marabas corra or signals
ĀĀĊĶ	Advance-acknowledge signal, used in 8080A-based systems. It is sent to the SBC-80 board by a memory bank in response to a memory-read command, allowing the memory to complete the access without requiring the CPU to wait.
BCLK	Bus clock, used to synchronize bus-control circuits on all master boards. It has a period of 101.725 ns (9.8304 MHz) and a 30 to 70% duty cycle. The signal may be slowed, stopped or single-stepped.
BPRN	Bus-priority-input signal, used to indicate to the master that a higher-priority master board wants to use the system bus. When brought high, the signal suspends processing activity and places line drivers of the master in a standby mode.
BUSY	Bus-busy signal, a bidirectional control line that allows control and monitoring of the Multibus in multimaster systems. As an output from a bus master, BUSY indicates the bus is being used by the board. It prevents all other master boards from gaining control of the bus. Each master monitors BUSY as an input to determine current Multibus usage status.
CCLK	Constant clock, used to provide a 9.8304-MHz clock signal for optional memory and I/O expansion boards. CCLK coincides with BCLK and has a period of 101.725 ns and a 30 to 70% duty cycle.
INIT	Initialize signal, used to reset the entire system to a known internal state.
ĪNTR1	Interrupt input, used to interrupt the processor via an externally generated interrupt request.
IORC	I/O-read command, a signal generated by the master to indicate that the address of an input port has been placed on the system-address bus and that the data at that input port are to be read and placed on the system-data bus.
IOWC	I/O-write command, a signal generated by the master to indicate that the address of an output port has been placed on the system-address bus and that the contents of the system-data bus are to be output to the addressed port.
MRDC	Memory-read command, a signal generated by the master that indicates that the address of a memory location has been placed on the system-address bus. It specifies that the contents of the addressed location are to be read and placed on the system-data bus.
MWTC	Memory-write command, a signal generated by the master to indicate that the address of a memory location has been placed on the system-address bus. It causes information on the data bus to be written into the addressed memory location.
XACK	Transfer-acknowledge signal, an input signal to the master board from an external memory location or I/O port to indicate that a specified read or write operation has been completed.

80/10A CPU board.

The synchronous and asynchronous nature of the serial interface makes it compatible with virtually every standard serial data-transmission technique used today (including IBM's Bi-Sync). This allows multiple SBC-80 boards to be interconnected as a distributed-processing network. The resulting task segregation or redundancy (or both) significantly improves both system performance and reliability.

Two jumper-selectable interrupt requests may be generated automatically by the serial interface. One occurs when a newly received character is ready to be loaded into the CPU (receive-channel buffer is full). The other occurs when new data are ready to be transmitted to the remote device (transmit-data buffer is empty).

Both the SBC-80/04 and 80/05 provide serial I/O capability through the serial input data (SID) and serial output data (SOD) functions of the 8085 CPU. These functions are controlled by software executing the 8085 read-interrupt mask (RIM) and set-interrupt mask (SIM) instructions.

For systems requiring many serial channels, the SBC-534 communications-expansion board provides four USART channels with RS-232-C and optically isolated current-loop interfaces, programmable interrupt, timing, baud-rate control, and a Bell 801 Auto-Call unit interface.

# Expand the system via the Multibus

The SBC-80 family is gaining not only in popularity but in support for its Multibus as more and more companies offer SBC-compatible boards. Intel now provides high-speed mathematics, RAM, EPROM, mass storage, digital I/O, combination memory and I/O, serial communications, and analog-I/O expansion boards.

For applications requiring fast, high-precision number crunching, the SBC-310 math unit acts as an intelligent slave to perform floating-point and fixed-point mathematics. A processor uses the 310 by passing parameters to it along with a command byte to select the desired operation from the SBC-310's 14 instructions. The repertoire includes 32-bit floating-point (single-precision) addition, subtraction, multiplication, division, squaring, square root, comparisons, and tests; 16-bit fixed-point multiply, subtract, extended divide, and extended compare; and conversion from fixed to floating point or vice versa.

A completed operation may be signaled either by the math unit via an interrupt or by the host processor's polling the "operation complete" flag in the unit's status register. The result may be retrieved at this point or left in the 310's accumulator for further use.

In addition, the 310 provides control circuitry so that it may be treated as a "shared resource" among several CPU boards.

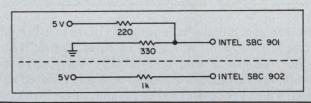
Two diskette options are available for mass storage.

Table 5. Programmable interrupt modes, SBC-80/20-4

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Autorotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns low- est priority level. Priority of all other levels based in se- quence on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Table 6. Line drivers and terminators

Driver	Characteristic	Sink current (mA)
7438	I,OC	48
7437	1	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	1	16



The SBC-201 diskette controller provides full control for one or two single-density diskette drives and acts as a programmable slave to masters on the Multibus. All diskette information is stored in the IBM soft-sectored format. For systems requiring greater storage capacity, the SBC-202 provides full control for up to four double-density diskette drives. Thus, 2 Mbytes of mass storage may be added to SBC-80-based systems for each SBC-202 plugged into the bus.

Digital I/O may be expanded using any of three Intel boards. The SBC-519 provides 72 programmable parallel I/O lines as well as interrupt handling and a real-time clock.

The 519's clock can interrupt the appropriate CPU periodically so that the CPU can monitor system-I/O status. High-speed I/O events can gain the CPU's attention via interrupts. The SBC-517 combination I/O board and the SBC-104, 108 and 116 combination memory and I/O boards offer 48 programmable parallel lines, a full RS-232 USART serial channel, interrupt handling and a 16-ms real-time clock. The

# Table 7. RMX-80 routine library

RMX/80 module	Function
Nucleus (executive)	Provides basic capabilities (concurrence, priority, and synchronization/communication) found in all real-time systems.
Terminal handler	Provides real-time asynchronous I/O between an operator's terminal and tasks running under the RMX/80 executive, includes a line-edit feature similar to that of ISIS-II (supervisory system on the Intellec development system) and type-ahead facility.
Diskette file systems	Diskette driver and file management capabilities, allows user to load tasks into the system and to create, access, and delete files in a real-time environment without disrupting normal processing. File formats compatible with ISIS-II for both single and double-density systems.
Free space manager	Maintains a pool of free RAM and allocates memory out of the pool upon request from a task; reclaims memory areas when no longer needed.
Debugger	Specifically designed for debugging software running under the RMX/80 executive; used by linking it to an application program or task. Thus, it can be run directly from the single-board computer's memory.
Math handler	Provides full control and communication for SBC 310 math board for high-speed fixed and floating-point math functions.
Analog interface handler	Provides real-time control for SBC 711, 724, and 732 analog I/O expansion boards.

104, 108 and 116 also hold up to 8 kbytes of EPROM, along with 4, 8 or 16 kbytes of RAM, respectively.

For systems geared to especially noisy environments, the SBC-556 provides 48 optically isolated I/O lines, which are configured as 24 input lines, 16 output lines, and eight programmable-I/O lines. The user fixes the optical-isolation characteristics according to his exact system requirements by installing the opto-isolators and current-limiting resistors of his choice into the board sockets. Input voltages up to 48 V, output lines up to 30 V and currents up to 60 mA may be interfaced.

Of course, many more RAM, ROM, communications and interface options are available. But for systems to come together quickly during development, there must be some standardized operating software to provide some of the most fundamental system routines.

#### System software: the glue that binds

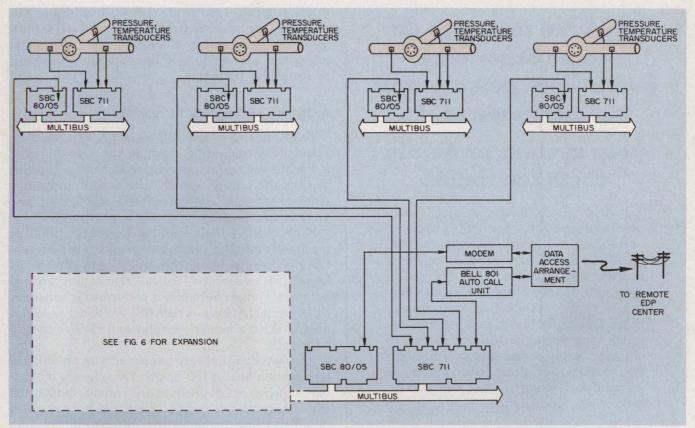
Where the Multibus provides a standard hardware structure, RMX-80, a real-time multitasking executive supplies a modular software framework. With RMX-80, routines don't have to be developed for task synchronization, priority resolution and peripheral control (printers, terminals, diskettes, etc.). Versions

are available for the SBC-80/20, 80/20-4 and 80/10A CPU boards.

Critical projects can be completed rapidly because RMX-80 provides major portions of the software requirements for many real-time systems. For example, the diskette file-extension software of the RMX-80 program may be linked into the system software. Thus, users can immediately have a diskette file structure with facilities to open and close files, create and delete files, read or write files sequentially or randomly (read function may be used for initial program load, if desired), or allocate file storage dynamically on single or double-density diskettes.

The compactness of RMX-80—the entire executive resides in 2 kbytes of ROM—reduces memory requirements and eliminates the need for bootstrap-program loading. All RMX-80 operations are based on individual tasks. A task is a program with unique data and stack that operates asynchronously with other such programs in the system.

Basically, the RMX-80 is a library of "standard" routines (Table 7), such as an analog-interface handler and a terminal handler. Fig. 4 illustrates how to develop software by selecting appropriate RMX-80 modules, then locating and linking them with particular software tasks on an Intellec microcomputer development system. In addition, a debugger module



5. This possible SBC-80 system configuration uses four SBC-80/05s to monitor and control pipeline parameters

and feed data back to a master controller, an SBC-80/20-4. The master controller sends data back to a host system.

in the RMX-80 speeds real-time system development.

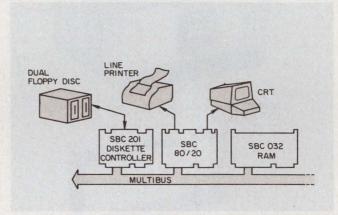
The executive accesses system resources according to task priority, intertask communication, interrupt-driven control for standard devices, real-time clock control, interrupt handling, and other optional functions. In all, there are 255 separate task-priority levels, and since multiple tasks may share the same level, the actual number of tasks is limited only by memory size.

### Develop programs with the Intellec

The Intellec and its ICE-80 and ICE-85 in-circuit emulators help minimize the time required to develop software and hardware. Standard Intellec stand-alone software includes resident macroassemblers for the 8080A and 8085 CPUs, a text editor, and a system monitor/debugger. As a result, programs can be assembled, loaded, edited, executed, and debugged.

ICE diagnostics can significantly reduce program development and debug time. Break points may be set on user-specified memory-read or write operations, I/O read or write operations, or user-defined extension parameters. Programs can be single-stepped to check operating conditions and performance.

PL/M-80 is the high-level systems-programming language. The optional Intellec-resident PL/M compiler provides the ability to program in this natural, algorithmic language, so there is no need to manage register usage or to allocate memory. PL/M programs



6. Expanding the pipeline monitor/controller system is as simple as plugging more cards into the Multibus and altering the software. By adding another SBC-80/20 to the master controller, some local processing can be done and a local CRT and high-speed printer can be added as well as RAM and diskette-memory space.

may be linked to assembly-language programs to hasten product development further.

A relocatable macroassembler residing on the Intellectranslates symbolic assembly language into 8080 or 8085 machine code and permits the use of relocatable and linkable object code. With full macro capability, similar sections of code needn't be written over and over.

Intellec options include a diskette operating system, ISIS-II, with diskette controller, single or dual diskette

# some other way – what these power amps are designed to do, your system probably costs too much.

If you're trying to do

In the DC to 30KHz range, Crown power amps are practically unbeatable. They're rugged, reliable, and can handle almost any load — right or wrong. Their performance has been proven in many different kinds of systems, under wildly different conditions. Designed for 19" rack mount and quick, simple hook-up. And they are almost always cheaper than whatever you think is an alternative. For more information, write or call the Crown Industrial department.

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drives and ISIS-II software. ISIS-II provides all the facilities for producing and handling relocatable code, including a relocating macroassembler, relocating loader and a linker to help link separately compiled or assembled programs.

# Apply the SBC boards to real use

To get an idea of the SBC 80 family's capabilities, examine the application shown in Fig. 5. In this case, a remote control/monitoring section of a pipeline supervisory control system grows with increasing requirements for additional local throughput and processing capability.

Four SBC-80/05s act as remote pipeline monitors/controllers. Each unit monitors various contact closures (limit switches, relays, etc.) and a hex keypad, with a subset of its own I/O lines programmed as inputs. Contact debounce is performed in software. Other digital I/O lines on each SBC-80/05 act as output lines to drive a numeric display and various control relay coils.

Analog-control lines are interfaced with an SBC-732 combination analog-I/O board. Transducers indicating temperature and pressure drive analog inputs, and analog outputs drive valves. Flow rate is determined in software by manipulating differential pressure data available from pressure transducers.

The four 80/05s are linked serially to a remote SBC-80/20-4-based data concentrator. An SBC-534 communications expansion board provides four RS-232-C serial channels, each interfacing directly with one of the four 80/05-based pipeline monitor/controllers. The 80/20-4 periodically queries each monitor to determine its current status. The concentrator also relays control commands from a host computer controlling the entire pipeline. The 80/20-4's own RS-232-C serial channel provides the interface for this high-speed synchronous link to the host CPU.

The 80/20-4 can contact the host CPU with the Bell 801 automatic calling-unit interface on the SBC-534. The synchronization and control of communication between the four 80/05s and the host are handled by RMX-80 on the 80/20-4.

The 80/20-4 system can be expanded to provide local processing capability, as shown in Fig. 6. Here, another 80/20-4 is added as a second master on the Multibus to provide control for a local CRT and high-speed printer, and to provide local processing capability.

An additional 32 kbytes of RAM are furnished by an SBC-032 RAM-expansion board. A third master, an SBC-202 dual-density diskette controller, can also be added to the Multibus, along with two double-density diskette drives. Communication between the two 80/20s is handled via user-written intermaster message tasks.

Note: Multibus, RMX-80 and Intellec are registered trademarks of Intel Corp.

# Introducing

# HP's first general-purpose Logic State Analyzer designed for both controllable production testing and field service...and it's low cost.

Until now, production line testing of digital equipment has meant complex test gear, large sums for computerized equipment or time-consuming manual checks . . . perhaps all three. In the field, it's been traditional test gear without the measurement capabilities of logic state analyzers.

Now, with the low-cost 1602A, HP offers a general-purpose, Logic State Analyzer that's easy to use in a number of plant or field applications. Manufacturing can use it in automatic functional test systems or in board-level and incoming inspection testing. And its ease of use, light weight and portability makes it a natural for field service applications, too. The 1602A, priced at \$1800\*, is compatible with many logic systems having data rates to 10 MHz. It monitors, stores and displays activity on system buses or control lines (up to 64, 16-bit words on a single instrument) to verify proper system function.

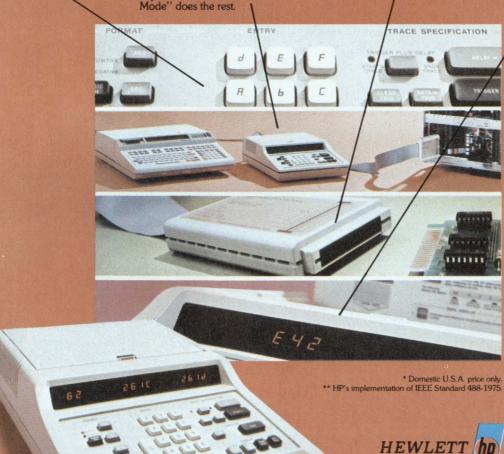
It's portable, adaptable to automatic control, low cost and so easy to operate it's almost self teaching. It can boost your production-line testing throughput and field-service trouble-shooting efficiency. Get all the details from your HP field engineer.

For manual production line testing and for field service troubleshooting, the 1602A keyboard lets you define testing and display parameters with just a few keystrokes. The LED display then lets you compare line or bus activity with test specifications.

For automatic systems, an HP-IB\*\* option lets you do setups and evaluation using a computing controller. When used with HP's 9830A or 9825A controllers, programming is simple. An operator just presses a few special-function keys, and the HP-IB's "Learn Mode" does the rest.

Edge-connector probes speed setup. When test points are built into your system's boards or board extenders, the probes are simply plugged in. Time-consuming and error-prone probe connections can be eliminated.

This instrument minimizes chances of error two ways: Extensive messages tell the operator that the 1602A is being used properly. And internal diagnostics verify proper operation.

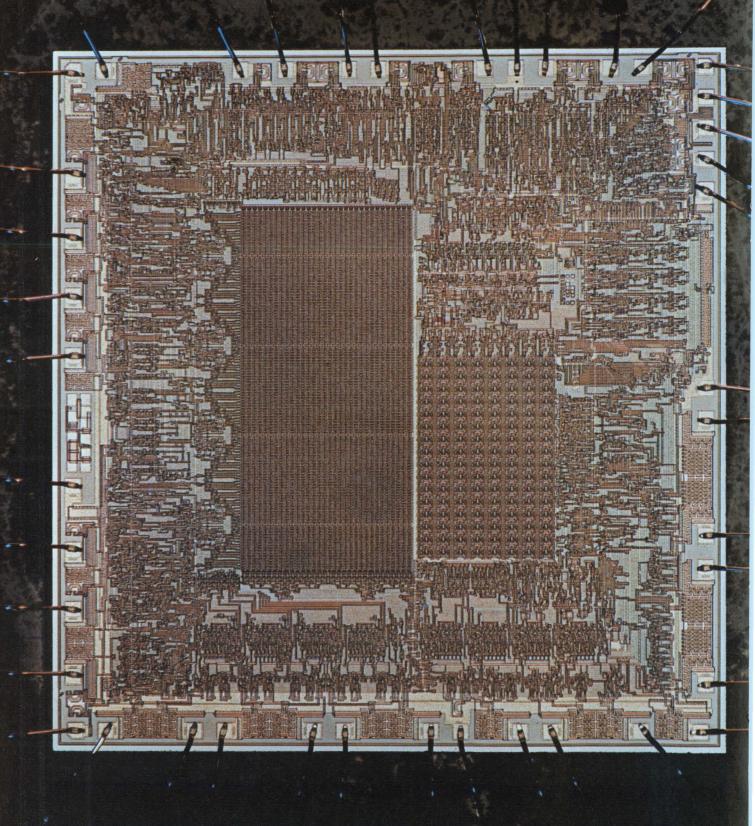


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# Dense, it is.



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The S2000 is an entire microcomputer on a single chip, with expandable program ROM and versatile I/O. So you can implement or enhance your control schemes quickly and easily.

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For less than \$5 each in quantity, each \$2000 contains:

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Soon, other S2000 family microcomputers will have vacuum fluorescent display drivers and on-chip 2K ROMs. In addition, AMI welcomes modifications to the S2000 to meet your particular I/O requirements, making your system even more cost effective.

Our Microcomputer Development Center (MDC) contains a powerful array of hardware and software tools to get your product to the market fast. Its intelligent 6800 microprocessor system controls a CRT with a flexible text editor, a smart macro-assembler, and a built-in PROM burner.

The DEV-2000 Development Board lets you do hardware emulation and software debug at the same time. The SES-2000 Static Emulator Module plugs right into your prototype. Our Logic Analyzer gives you computer power to create your own diagnostic display layouts and formats. And we even have software that simulates the S2000 within the MDC.

What more could you ask, except for some Application Engineers to help you do a fast turnaround. We have those, too. Specialists in the S2000 are ready and waiting for your call at (408) 246-0330. Or simply write to AMI Marketing, 3800 Homestead Road, Santa Clara CA 95051. You'll be amazed how smart one dense little chip can be.



# Technology

# Logic analyzers aren't all alike. Learn the differences between state and timing instruments, and you'll end up with the right troubleshooting tool.

Don't choose a logic analyzer until you can determine if your application calls for a logic-timing or logic-state instrument. A timing analyzer primarily depicts multichannel, low-repetition-rate or single-shot timing events. A state analyzer is meant to record state sequences, which are often complex and require fairly sophisticated recognition techniques.

Don't assume right off that the state analyzer is by default a software instrument just because the timing type—in its quest to uncover glitches and race conditions—is generally considered a hardware tool. It's true that the state analyzer can depict software in execution. But calling it a software analyzer ignores the countless hardware phenomena that lead to the creation of false states. And a hardware designer may be misled into thinking that a state analyzer can't handle his problem, when quite often it can.

#### Take a microcosmic view

With that in mind, look at how a timing analyzer works. Immediately, you see a variable-rate, internal reference clock generating a sampling sequence to read all channels simultaneously. The recorded data are the outputs of comparators that indicate whether the input lines are high or low relative to a threshold voltage at the clock edge.

The data are subsequently displayed on a CRT so that changes from low to high states appear as ideal waveform transitions (Fig. 1). Obviously, the more rapid the sampling rate, the better the resolution in time. Right now, the fastest available sampling rate is 200 MHz, which gives a resolution of ±5 ns.

Another important feature of most logic-timing analyzers is the ability to catch glitches, so that they can detect a pulse or a double transition between samples. A glitch is two or more transitions through the threshold, separated by a minimum duration that depends on the capability of the particular logic analyzer. The minimum detectable width on glitch detectors is about 2 ns.

Consider the output of a one-shot multivibrator, which should be a clean, single pulse of predetermined width. With the analyzer looking at the one-shot's output at a slow sample rate, the pulses do seem uniform. However, the glitch detector indicates an

occasional second pulse, or glitch, on the pulse-trailing edge (Fig. 2a).

By specifying the glitch as the trigger condition, you can get a stable display. Expand the trailing edge of the pulse with higher sweep speeds, and you see the real problem—a double pulse (Fig. 2b). Connect probes to all of the monostable's inputs, and you'll see which of the inputs makes the monostable double-pulse.

#### Rethinking resolution

Still, a timing analyzer has its critics, who point out that unless you are willing to spend a lot, the obtainable resolution doesn't begin to approach that of an average-priced scope. That's true for measuring two or four-channel repetitive events, but not for multichannel, single-shot events above chop frequencies; negative-time events (those prior to the trigger); and very narrow pulses relative to long periods—all of which a scope can't check nearly as easily, and some not at all.

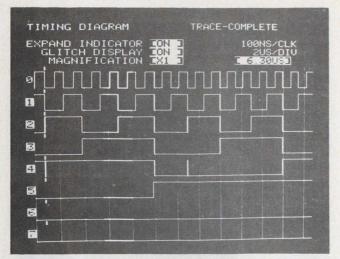
Actually, a timing analyzer's strength is not fine-tuned timing resolution, but functional timing measurements. Suppose you'd like to display handshake sequences for memory or I/O data transfer. Or you'd like to examine a handshake sequence on the IEEE standard interface (Fig. 3). You'll be interested in the sequence in which lines toggle—not resolution to the nearest nanosecond on precise edges. The distinction may be subtle, but it can change your outlook toward the features needed in a timing analyzer.

Take a microprocessor-based, real-time controller, which can have some fairly tricky timing sequences. A 20-MHz timing analyzer, with its 50-ns resolution, may be more than adequate for showing the functional timing relationships needed to troubleshoot the problems. But a scope won't be. Generally, if the sampling rate is at least five times greater than the data rate, then resolution is probably adequate for functional timing measurements.

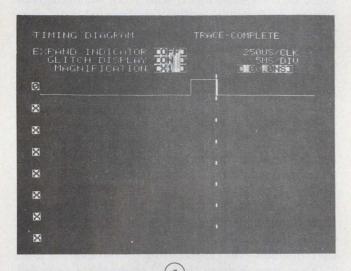
But more crucial than sampling rate in many applications is triggering capability. If data recognition (or nonrecognition) is sufficiently definitive, it often provides answers directly, so you don't have to study the recorded timing diagrams. There are several ways to trigger logic-timing analyzers:

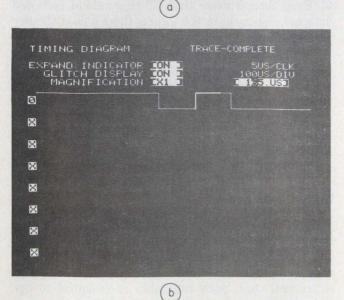
■ Asynchronously, with any Boolean expression of up to three ORed terms, including the NOT condition for an expression existing for a minimum selectable time (e.g.,  $A \cdot B \cdot \overline{C} \cdot D$ ;  $\overline{A \cdot \overline{B} \cdot C} + D + E$ ;  $A \cdot \overline{B} + \overline{A} \cdot B$ ).

**Bruce Farly,** Product Manager, Logic Analyzers, Hewlett-Packard, Garden of the Gods Rd., Colorado Springs, CO 80907.



1. This timing-diagram display shows functional timing relationships. Double transitions of sufficient energy between samples, called glitches, are highlighted by brightened video. The recorded trigger point is indicated by a brightened vertical dashed line.





2. A 6-ms-wide output pulse of a one-shot multivibrator appears to have an occasional glitch on the trailing edge (a). Expanding the appropriate edge with faster sampling rates shows that the glitch is actually a double pulse (b).

■ Synchronously, with an ANDed condition on the inputs of highs, lows and "don't cares," but only when the data are sampled. (This can be troublesome when the sample period is increased because the probability of sampling the desired trigger condition is reduced.)

• *On a glitch*, with a glitch on a given channel, between successive samples, and simultaneously with

any allowed Boolean expression.

(Some analyzers can trigger on a latched, or pulsestretched glitch, which obviously cannot be combined with a specified high or low condition on the same channel. Latched glitches, if adjacent to a normal data transition, may go undetected.)

Externally, with an additional nondisplayed input that permits triggering from either an edge or

level, depending on the instrument.

■ *Delayed*, with a triggering hold-off until a digital delay is counted down or a specified time interval passes.

• Armed, with a two-condition sequential trigger in which any of the outlined triggering methods are possible once the arming signal is received.

Not all triggering methods are available on one logic analyzer. Let your application dictate triggering flexibility. The more precisely the instrument can home in on a problem, the less dependent it will be on large memories or high sample rates.

The most crucial features of a timing analyzer, therefore, are the maximum sample rate, hence, best resolution; the largest memory depth needed to record the longest time interval for a given sample rate; a glitch detector; and triggering capability. How does the logic-state analyzer differ? A look at a typical design cycle may clear things up (Fig. 4).

#### How state analysis works

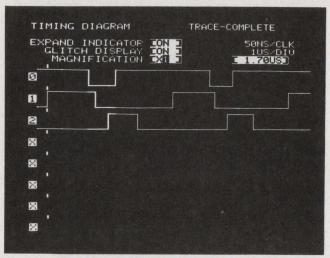
The graphic algorithmic process in the figure could represent the design cycle for a microprocessor or a minicomputer-based system, or even a ROM-based controller with no CPU, but with a simple automatic sequencer. "Algorithm," in fact, means a sequence of steps designed to perform a given task, for which hardware is to be designed and software written.

Quite often software and hardware are developed by separate design teams. They are distinctly different tasks. At any rate, the output of the hardware team, circuit boards of some kind, and the software output, object code, must come together sooner or later.

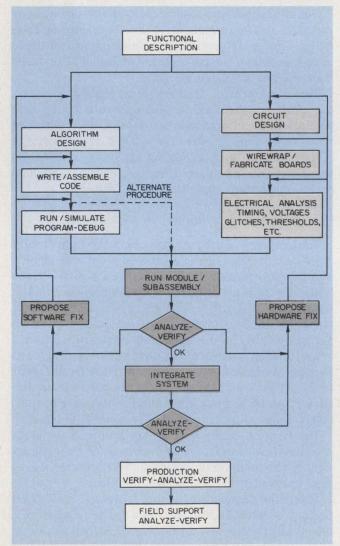
The final objective is to create a unique sequence of states resulting from the marriage, or the interaction, or the melding of software and hardware. However combined, they must act together.

When the sequence of states is wrong, be it from timing, glitches, noise, or software or algorithmic mistakes, there is a state-flow error, which shows up as an erroneous-state sequence. But how do you detect it? With an instrument that records logic states in the same way hardware responds to those states.

Often, the bulk of algorithmic-based hardware operates synchronously with a strobe signal—a master



3. **The IEEE 488 interface handshake** sequence is grist for a timing analyzer. Channel 0 = DAV, channel 1 = NRFD, and channel 2 = NDAC.



4. This generalized flow diagram depicts a typical design cycle. Note the separate tasks of writing software and building hardware, and the crucial junctions where the two jobs are systemized. Logic-state analysis is aimed at the resulting real-time hardware/software interaction.

clock, a subset of that master, or a handshake occurring only when data are valid. Whatever the strobe, when it toggles, the hardware responds.

# Synchronous? Asynchronous?

Obviously, then, a state analyzer must operate on the strobe—not on an internal clock signal as a timing analyzer does. This difference might lead you to believe that the timing analyzer is asynchronous and that the state analyzer is synchronous. That belief is an oversimplification. However, to read the same data as the hardware does, a state analyzer must operate synchronously with the system under test. In other words, it must read word parameters or state parameters, not timing parameters.

What's more, because a state analyzer reads data the way the hardware does, it should not require any hold time—that is, a period in which the data must remain stable after a strobe edge. That's because nearly all synchronous systems operate with D flipflops, or their equivalent, which are edge-triggered devices. Furthermore, unlike a timing analyzer's maximum clock rate, a state analyzer's needn't be any faster than the data rate.

A typical problem for a state analyzer involves an 8-bit microprocessor with a 16-bit address field. The state sequences of address values are essential, as are the values on the data bus and the activity on the I/O ports. Obviously, then, a state analyzer requires a large number of channels. A timing unit wouldn't because to examine more than eight simultaneous waveforms would confuse rather than help the problem

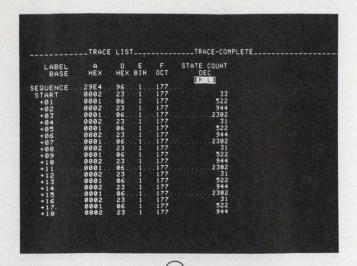
With state parameters, the multiple-channel information is boiled down into an appropriately coded display like hexadecimal, or even a reconstruction of the mnemonic code representing the data values (Fig. 5). Even though more than 32 channels of recorded data are displayed in the figure, there's no difficulty reading them.

To understand real-time tracing of state flow, consider the problem of monitoring microprocessor stack operations (Fig. 6). Here a state analyzer in its "trace-triggers" mode records successive stack pushes (writes) and pops (reads) as they occur in an 8080 system. Such measurements are easy to make with a state analyzer, and can help track down lost programs caused by stack overflows.

# What is selective trace?

A state analyzer can selectively trace data two ways. In a clock-qualification scheme, data are strobed in only if certain external qualifiers are true at the clock edge (valid memory address flag is true, a write pulse is present, etc.). Such capability is essential to deciphering data on a multiplexed bus. The other way is to qualify recorded data within the analyzer itself. A state analyzer should be able to do both.

Note that the "trace-triggers" mode records data



5. A state-analyzer listing of trace data boils down information on 6800-series microprocessor RAM addresses (a). The A-label is the 16-bit RAM address, the D label is

ADDRESS ENABLE Ø8FE TRIGGER <= Ø8FE >= Ø8DØ	DATA EXTERNAL
TRACE TRIGGERS ADRS	9999 9999 9999 9999 9999 9999 9999 9999 E 9999 9999 E 9999 9999 E 9999 9999 E 9999 9999 9999 9999 9999 9999 9999 9999

6. When recording real-time stack transactions on an operating 8080A-based system, selective tracing allows pushes (writes) and pops (reads) to be examined easily to help track down stack overflows.

ENABLE TRIGGER	ADDRESS 8000 XXXX	DATA EXTERNA	ЯL
DISABLE	8000		
ADRS O	PCODE/DAT	A EXTERNA	
TIME =	79	1 MICROSECOND	5
MAX =	79		S
MIN =	75	9 MICROSECOND	S

7. **Direct measurement of time intervals** between two states is very desirable in a logic-state analyzer. One unit, the HP 1611A, actually keeps track of the measured minimum and maximum values.

	ADDRESS	DATA	EXTER	RNAL
TRIGGE	ER <= 0100	СЗ		
TO 1 CD	OSCUP-E	DDE TO	1CD-C	
TRIGR	OCCUR=5	PRE-TR	NE 6 IGK=0	
	OPCODE/DAT		NE EXTERM	
ADRS 013A	POP PSW			100
013H 08F5	56 READ		Control of the last of	100
08F6	3E READ		Complete Complete	300
Ø13B	RET		THE RESERVE TO SERVE THE PARTY OF THE PARTY	300
98F7	FE READ		And the second second	900
98F8	AA READ		Section 19 Section 19	300
ØØEE	JMP 00F1	0	the Continue of the Line of the	900
'99F1	CALL 011B	0	1999 9	999
Ø8F8	00 WRITE		1999 90	900
Ø8F7	F4 WRITE		1999 91	200
Ø11B	PUSH PSW	2	1999 91	900
08F6	3E WRITE		1000 01	900
08F5	56 WRITE			999
Ø11C	MUI A,03			9 <b>9</b> 9
Ø11E	STA 0800			000,
0899	03 WRITE	6	1000 0	000

(b)

the 8-bit data bus, both coded in hex. Another listing, of 8080A data captured in real time, is displayed in the microprocessor's assembly language (b).

only within a given address range—the second kind of selective-trace recording. Selectiveness is important because quite often the state sequence of interest is more significant than that which occurs on every strobe signal. In fact, by prior analysis of the problem, most data transactions can be discarded. Without selective tracing, no practical memory would be deep enough to solve all possible state-analysis problems. A timing analyzer, on the other hand, would not be able to use selective tracing because the display created would be unintelligible.

So selective tracing reduces data and enables reasonable measurements of events that are widely separated in state time. Which points to another quite useful feature—the ability to measure either the time between events or the number of states occurring between events (Fig. 7).

Quite often, such information alone can ferret out a functional problem. The number of lower-order states occurring between successive high-order states is quite often a clue to an anomaly. By actually depicting the path length, a state count can be a tremendous help in spotting problems or optimizing operations.

When state sequences get extremely complex, finding a unique sequence may call for sophisticated tracing. The spotlight here falls on trigger power.

### Triggering and formatting

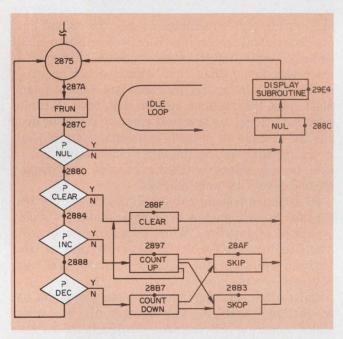
Actually, "trigger" is a misnomer for a logic-state analyzer. Selecting unique states from a sequence to begin or end recording certainly can involve more than recognizing a single event. Quite often a state analyzer is required to recognize and record a sequence of events, so that a particular path can be traversed through the sequence to arrive at a state of interest (Fig. 8).

Suppose the state sequence beginning at address

 $29E4_{16}$  is to be recorded, having come in one pass from state  $2875_{16}$  and having gone through states  $2884_{16}$  and  $2897_{16}$ . To avoid multiple passes if all four states are not found in order in a single pass (Fig. 9), a sequence restart term,  $29E4_{16}$ , resumes the search for the sequence. The state count in the right-hand column of Fig. 10b shows that another much longer path could run from  $2875_{16}$  to  $2884_{16}$  without the restart term to confine the search to a single pass.

But when state boundaries are crossed in an unknown fashion, relational operator triggering ( $\geq$ , $\leq$ ) can be extremely useful. Here, a state analyzer bounds a range of state values—inclusively or exclusively—and selects as the trigger the first excursion into or out of the range.

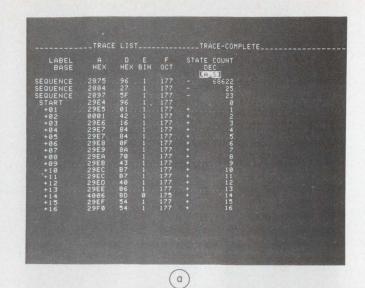
Unfortunately, all state-analysis problems aren't confined to neat 16-bit or 8-bit hex or octal fields. Someone working with an 8-bit microprocessor wants a data format unlike the ones for bit-slice architecture



8. Often, a sequence of states is needed to define a path of execution. One such case: a portion of the flow chart for a 6800  $\mu$ P-based demonstration system.

	TRACE SPE	ECIFICA	TION	1/ 10	TR	RACE-COMPLETE
	LABEL BASE	A HEX	D HEX	EBIN	F OCT	OCCUR DEC
FIND IN	THEN	2875 2884 2897 29E4	**	× × × × × ×		00001 00001 00001 00001
SEQ RES	TART COND	9E4	***	8	2000	
TRACE EALL S	STATESD					
COUNT [	SIAIE	200000	200	•		

9. **Up to seven sequential events can be specified** by a state analyzer, with an occurrence count for each event to indicate when a trace should begin. A sequence-restart term ensures that the sequence is satisfied in a single pass.



TRACE LIST TRACE-COMPLETE

LABEL A D E F STATE COUNT

BASE HEX HEX BIN OCT

SEQUENCE 2895 96 1 177 - 43

SEQUENCE 2894 27 1 177 - 25

SEQUENCE 2897 55 1 177 - 23

START 29E4 96 1 177 - 0

91 29E5 01 177 - 1

91 29E5 01 177 + 1

92 29E6 16 177 + 2

93 29E7 94 177 + 4

94 29E7 94 177 + 5

95 29E7 94 177 + 5

96 29E8 0F 177 + 5

97 29E9 9A 177 + 6

97 29E9 9A 177 + 6

97 29E9 9A 177 + 9

98 29EA 79 177 + 9

99 29EB 43 177 + 9

99 29EB 43 177 + 9

99 29EB 43 177 + 9

99 29EB 67 177 + 10

11 29EC 67 177 + 11

11 29EC 67 177 + 11

12 29ED 40 177 + 12

13 29EE 66 177 + 13

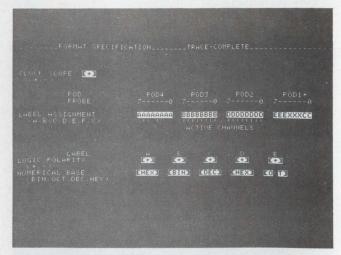
14 4066 89 0 175 + 14

15 29EF 54 1 177 + 15

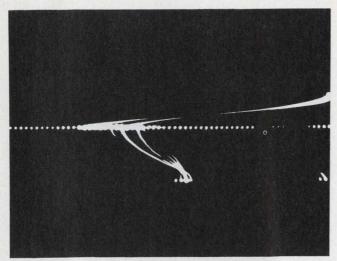
15 29EF 54 1 177 + 15

10. **Two ways to a single goal:** A sequence can be satisfied either by multiple passes (a) or by a single pass through sequential terms (b). Note the difference in path length as indicated by the state count.

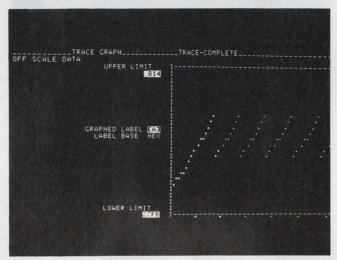
(b)



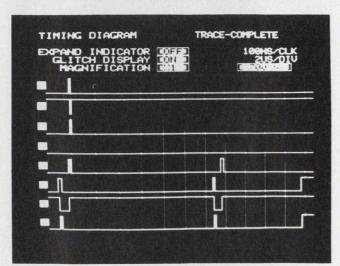
11. A logic-state analyzer should offer flexible data formatting. Shown here is an arbitrary grouping of 32 inputs, with a label assigned to each group. Thereafter, each label can be coded independently in hex, octal, decimal or binary, in either positive or negative logic.



12. **One "map" display mode** provides a dynamic overview of state activity to identify errant behavior, recognizable repeated patterns or response to a stimulus.



13. A data-domain graph also presents state activity. The axes are state magnitude (vertical) vs state sequence (horizontal). Label A—address, in this case—is graphed showing a looping operation (sawtooth waveform) in the  $28XX_{16}$  range of addresses.



14. **Sometimes, both logic states and timing** information must be recorded simultaneously. This combo is the forte of one unit, the HP 1615A.

TRACI	E LIST	TRACE-COMPLETE
C16	BITI	
LINE NO.	C BIN	
	DIN	
241	00000100	
242	00001000	
243	00010000	
244	00100000	
245	01000000	
246	10000000	
247	10000000	
248	01000000	
249	00100000	
250	00010000	
251	00001000	
252	00000100	
253	00000010	
254	00000001	
255	00100000	

15. State measurement of data transacted during an IEEE-488 bus transaction shows the absence of the last data byte (00000001) before the control character (inverse video). Here, the time recording of Fig. 16 triggered the state recording.

or a 16-bit minicomputer. A state analyzer should accommodate every need (Fig. 11).

# Mapping the big picture

One way to format data is to reduce the information to a graphic overview. Two types are available: the map in Fig. 12 and the data-domain graph in Fig. 13. But not all maps are alike. While all manufacturers have adopted axes similar to those introduced by the HP 1600A, some offer only a static plot of the data recorded in memory, with or without lines connecting the dots to show state sequence. Lines connecting the state values help you recognize patterns. Others offer a rapid display/record cycle that presents a dynamic view of state activity.

To see how mapping can help your measurements, ask yourself: In pattern recognition, does the sequence always occur the same way? Does my system respond to a stimulus? Does state XXXX ever occur? Does my system ever make excursions outside or inside certain bounds? The last question especially can be addressed effectively only with a dynamic map.

A data-domain graph, on the other hand, plots state magnitude as a function of state sequence. Note in Fig. 13 that when the p counter is graphed, program looping always takes the shape of a sawtooth waveform. The graph is another way to make complex operations more comprehensible, which quickens analysis.

The most crucial features of a state analyzer, therefore are sufficient word width to read all data of interest, simultaneously, with as flexible a data format as possible; a speed only as fast as the data rate, but with zero positive hold time; selective data strobing, both on a clock and data-selection basis, if possible; and as flexible triggering as possible. A state analyzer can also be a big help if it can map, graph,



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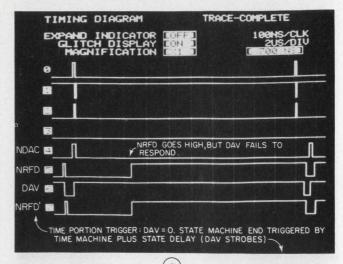
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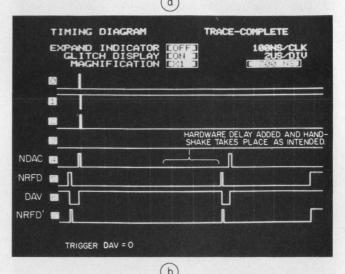
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16. Referencing timing-diagram displays by combining the capabilities of trigger and digital (state) delay: An incorrect handshake sequence causes the data byte to be dropped (a). The sender shuts down early-NRFD goes high but no DAV is received. The handshake is corrected by adding some delay (b).

or count states, and measure elapsed time between states.

So the differences between a timing analyzer and a state analyzer are considerable. Given the functions of each analyzer, they have to be.

But when all is said and done, you may still have to record state sequences while triggering a timing analyzer so that you can view timing related to the same functional events. The combination instrument in Fig. 14 does both simultaneously, not alternately.

Suppose a DMA error on an HP-IB interface shows up as a missing data transaction (Fig. 15). You must examine the HP-IB handshake sequence just before the control character—while recording the state data.

The tricky part is to place the timing display on the appropriate data transaction. Success depends on a combined asynchronous-pattern trigger and digital delay (by the external state clock). Fig. 16a shows a sender shut down prematurely, and 16b shows the problem corrected by adding some delay.

# Intel delivers the only 16-pin 4K RAM that's sure to keep you smiling.

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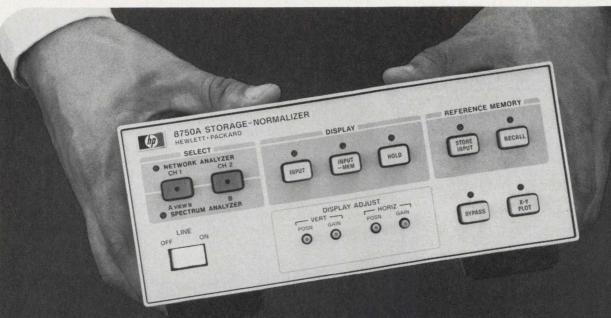
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	2104A-2	200 ns	320 ns	32 mA
,	2104A-3	250 ns	375 ns	30 mA
	2104A-4	300 ns	425 ns	30 mA
	2104A	350 ns	500 ns	30 mA

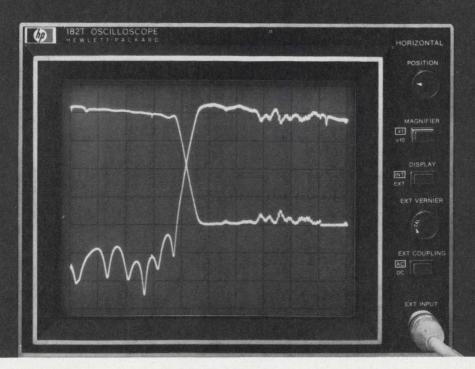
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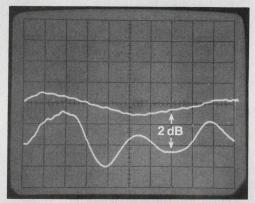


# The HP8750A Storage-Normalizer: It brings additional accuracy and simplicity to swept frequency measurements.

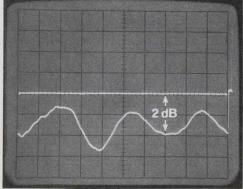
Here's an extremely useful and versatile accessory for most HP Network and Spectrum Analyzers. The 8750A Storage-Normalizer employs memory techniques to "normalize"—that is, remove system response from measured data. And its digital storage, constantly updated, provides a continuous flicker-free display regardless of sweep speed.

Here are some examples of the improvements it can bring to your swept frequency measurements:

# High Accuracy Measurements.



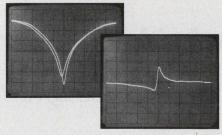
Before Normalization



Normalized

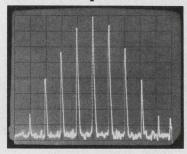
Frequency response or tracking errors in transmission or reflection measurements are eliminated with normalization. You can calibrate the test system's response and store it, then subtract it from the measured data. The resultant difference represents the corrected measurement that's displayed directly in dB.

# **Comparison Measurements.**



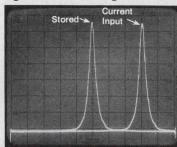
No longer is it necessary to visually scale deviations between two traces. With the HP 8750A, you can now display the *difference* between the two. Deviation between test devices is displayed directly in dB with a single trace.

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Use it for high resolution measurements when slow scan times are needed and get a bright, flicker-free display. Measurement data are displayed from memory with continuous refresh, independent of scan time and scope adjustments.

# **Spectral Comparisons.**



Using the 8750A in spectrum analysis applications, a signal spectrum can be frozen on the CRT and then compared directly with the current input signal.

Because the HP 8750A can "freeze" the display, photography is simplified and hard copies such as X-Y recordings can automatically be plotted, even while new measurements are being made.

Domestic U.S. price of the Storage-Normalizer is \$1450.

Call your HP field engineer for more information on how the 8750A enhances measurements made with HP 8755, 8410, 8407 and 8505 Network Analyzers, HP 8557, 8558 and 8565 Spectrum Analyzers, plus other instruments. Or write.



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# **Try a Wien-bridge network** instead of a twin-T in your next analog filter design. The advantages begin with a filter you can design in five fast steps.

Put a Wien-bridge network, instead of a more popular twin-T network, into your analog filter and you'll get deeper notches and higher Qs. An added bonus is the simple design equations. With a five-step procedure that contains only three linear equations, you can build a Wien-bridge notch filter that has fewer frequency-determining components than a twin-T.

With fewer components to adjust, it's easier to trim a Wien-bridge filter to a desired notch frequency. You'll get higher Qs because the need for critical balance required between the two parallel branch networks of a twin-T is eliminated. Tuning for the best null is simple, because there's no interaction between null-determining and frequency-determining components. And a Wien-bridge can be designed for any practical bandwidth, with notch depths limited only by stray leakage capacitance.

You can apply a Wien-bridge filter to the same signal-filtering jobs usually assigned a twin-T. Depending on your design, it will reject unwanted frequency components, let you measure harmonic distortion, or serve as a building block to synthesize bandpass filters.

To find the component values of a Wien bridge, start by examining its transfer function to see how the design equations are developed.

# Equations are in the transfer function

You can find the transfer function of a Wiencapacitance-bridge notch filter from the schematic diagram of Fig. 1. In Laplace notation, the general form of the transfer function is:

$$H(s) = \frac{E_{out}}{E_{in}}$$

$$= \frac{k_2}{1-k_f} \left[ \begin{array}{c} s^2 + \left( \frac{3k_2-1}{k_2} \right) \omega_0 s + \omega_0^2 \\ s^2 + \left( \frac{2-3k_f}{1-k_f} \right) \omega_0 s + \omega_0^2 \end{array} \right], (1)$$

where  $k_2$ ,  $k_{\rm f}$  and  $\omega_0$  can be defined in terms of the

**Glenn Darilek**, and **Oren Tranbarger**, Senior Research Engineers, Southwest Research Institute, 6220 Culebra Rd., San Antonio, TX 78284.

circuit components as

$$k_{2} = \frac{\frac{1}{R_{2}}}{\frac{1}{R_{1}} + \frac{1}{R_{2}} + \frac{1}{R_{f}}},$$
 (2)

$$k_{f} = \frac{\frac{1}{R_{f}}}{\frac{1}{R_{f}} + \frac{1}{R_{f}} + \frac{1}{R_{f}}},$$
(3)

and  $\omega_0 = 1/RC$ . (4)

But if the circuit of Fig. 1 is to act as a notch filter, the transfer function must take the following form:

$$H(s) = \frac{s^2 + \omega_0^2}{s^2 + b\omega_0 s + \omega_0^2},$$
 (5)

where b is defined as the notch bandwidth, 1/Q. Comparing like terms in Eqs. 1 and 5, you can see that the "s" term in the numerator of Eq. 1 does not appear in Eq. 5. Therefore, the coefficient of s must equal zero:

$$3k_2 - 1 = 0 (6)$$

Solving for k2:

$$k_2 = 1/3.$$
 (7)

Examine Eqs. 1 and 5 again. The notch bandwidth, b, in the denominator of Eq. 5 must equal the coefficient of the  $\omega_0$ s term in the denominator of Eq. 1. Bandwidth is then expressed as:

$$b = \frac{2 - 3k_f}{1 - k_f}.$$
 (8)

When Eq. 7 and Eq. 8 are substituted into the expressions for  $k_2$  and  $k_f$  (Eqs. 2 and 3), you get design equations for two of the network's five resistive components:

$$R_2 = \frac{b (R_1)}{3 - b}$$
 (9)

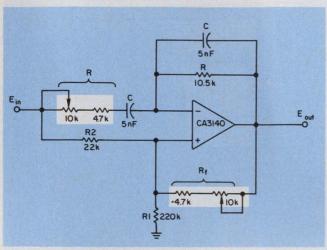
$$R_{f} = \frac{b (R_{1})}{3 - (2-b)}$$
 (10)

The frequency determining resistors are calculated from Eq. 4:

$$R = \frac{1}{2\pi f_0 C} \tag{11}$$

Comparing Eqs. 1 and 5, the gain coefficient can be written as,

$$H_0 = \frac{k_2}{1 - k_f} \tag{12}$$



1. This Wien-bridge notch filter can replace a twin-T filter in analog signal-processing applications. The  $10\text{-}k\Omega$  potentiometers are provided for easy nulling of the signal at the notch frequency.

By substituting Eqs. 2 and 3 into Eq. 12, the gain coefficient reduces to:

$$H_0 = \frac{1}{1 + \frac{R_2}{R_1}} \tag{13}$$

But from Eq. 9,

$$R_2/R_1 = b/(3-b),$$
 (14)

and after substituting Eq. 14 into Eq. 13,

$$H_0 = 3-b/3.$$
 (15)

Eq. 15 shows that the out-of-notch gain of the filter is related to its bandwidth. And in some cases, particularly a high-Q filter where b is relatively small (b = 1/Q), the circuit has essentially unity gain.

Now you're ready to apply the equations in a procedure that determines a filter's component values.

# Five steps to a Wien-bridge filter

When using the Wien-bridge design procedure, you must calculate some component values and select others:

1. Select a value for  $R_1$ . For most applications, a value between 100 k $\Omega$  and 1 M $\Omega$  can be used. You can

calculate the fractional bandwidth, that is, the ratio of the filter bandwidth in Hz, to the rejection frequency, also in Hz. If the ratio is 0.1 or less, choose an R<sub>1</sub> value that is closer to the high end of the resistance range.

2. Calculate R<sub>2</sub> from Eq. 9.

3. Calculate Rf from Eq. 10.

4. Select a value for C. It can be any stock value capacitor whose impedance at the notch frequency is within an order of magnitude larger or smaller than  $10~\mathrm{k}\Omega$ .

5. Calculate the frequency-determining resistor, R from Eq. 11.

Notice, from Eqs. 4, 9 and 10 that frequencydetermining components are independent of bandwidth-determining components. Therefore, frequency can be changed without affecting bandwidth and vice versa.

In putting the 5-step procedure to work, assume that a notch filter is required to reject a signal at 3 kHz and have a bandwidth of 800 Hz. Now, find the component values of the filter.

The fractional bandwidth, b, is  $\frac{800}{3000}$  or 0.267. Select a value of 220 k $\Omega$  for R<sub>1</sub>. Calculate R<sub>2</sub> from Step 2 (Eq. 9):

$$R_2 = \frac{(0.267) (220 \times 10^3)}{(3.0 - 0.267)}$$

= 21.5 k $\Omega$ .

Calculate Rf from Step 3 (Eq. 10):

$$R_{\rm f} = \frac{(0.267) (220 \times 10^3)}{3(2 - 0.267)}$$

=11.3 k
$$\Omega$$
.

For C, select 5 nF. From Step 4,  $X_c$  will be 10.6  $k\Omega$  which is close enough to 10  $k\Omega$ .

Calculate R from Step 5 (Eq. 11):

$$R = \frac{1}{2\pi \ (3 \times 10^3) \ (5 \times 10^{-9})}$$

$$= 10.6 \text{ k}\Omega.$$

The component values for this example are part of the schematic in Fig. 1, but to make adjustments easier,  $10\text{-k}\Omega$  potentiometers have been inserted in series with both R and R<sub>f</sub>. Tuning the circuit is easy. Alternately adjust the pots until the signal at the required notch frequency is nulled out. For proper adjustment, use a very pure test signal or you'll find it difficult to determine when you're at null. That's because some signal generators generate test-signal harmonics that can interfere with tuning. If you need more than 50 dB of rejection, you'll have to be careful about circuit layout and shielding. And your op amp must have high gain and high input impedance at the notch frequency, in addition to being able to pass all signals of interest.

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# Single-shot multi uses few parts, provides high noise immunity

A single-shot multivibrator built with an LM 3900 current-differencing amplifier uses only one capacitor and three resistors and needs no diodes for clamping or pulse steering (see figure). Its nonregenerative circuit has greater noise immunity than conventional single-shots. The circuit generates an output pulse for each input positive-going transition.

In the quiescent state,  $4.5 \mu A$  supplied to the 3900's inverting input through  $R_1$  holds the output at ground. The drop across the noninverting input terminal is 0.5 V, because of the amplifier's input diode. A positive-going edge at the circuit's input, differentiated by  $CR_3$ , causes a larger current to flow through  $R_2$  than  $R_1$ , so the amplifier output switches high (+5 V). The switching time is limited only by the 3900's slew rate. As the differentiator voltage,  $V_{R3}$ , decays, current flow in  $R_2$  falls until it equals the flow through  $R_1$ , and produces a 1.35-V drop across  $R_2$ . This voltage

together with the 0.5-V diode drop at the noninverting input results in 1.85 V at  $V_{\rm R3}$ , where the amplifier output returns to the ground state.

The positive-going output pulse width t, is, obtained by solving

$$1.85 = 5 e^{-t/CR_3}$$

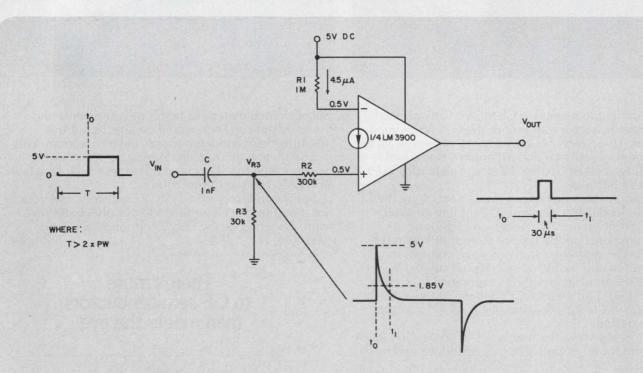
where

t = 
$$(10^{-9})(3 \times 10^4)$$
 ln  $(5/1.85)$   
  $\approx 30 \mu s$ 

A negative-going output pulse can be generated simply by interchanging the inputs to the noninverting and inverting terminals of the amplifier. Note that the pulse width can be controlled by a variable-voltage to R<sub>1</sub>; a higher voltage than 5 V would widen the pulse.

Tom Frederiksen, Applications Engineer, National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051

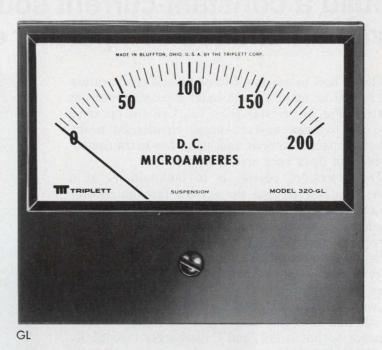
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# Build a constant-current source or sink with an unused comparator of a quad package

Here's how to use one of those unused comparators of a dual or quad chip to build a constant-current source (Fig. 1a) or sink (Fig. 1b). Usually, op amps are used to make constant-current circuits. But a left-over comparator circuit and just a few extra components can do a very creditable job.

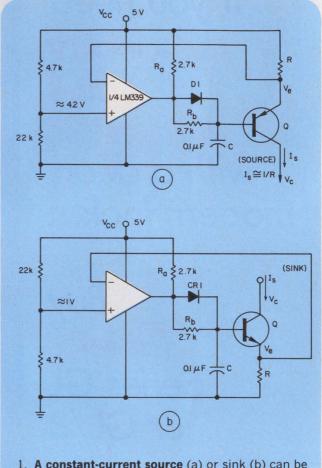
The object, of course, is to maintain  $V_e$  at a constant level, so that the current through resistor R and hence transistor Q, is constant regardless of changes in  $V_c$ . However, the voltage difference between  $V_c$  and  $V_e$  must exceed the emitter-collector drops of Q—about 0.5 V. Voltage  $V_e$  is compared with a reference voltage of about 4.2 V. If  $V_e$  is too low, the comparator output is open, and capacitor C charges via  $R_a$  and  $D_1$ , which reduces the base current in Q—and thus increases  $V_e$ ; if too high, the comparator output is low, and C discharges through  $R_b$  to lower  $V_e$ . Thus, capacitor C acts as a filter to smooth, or average, the voltage of this "bang-bang" type of output from the comparator.

However, the LM339 comparator isn't truly stable in either the high or low output state, but always overshoots the switching point and oscillates. With the values shown, oscillations at the LM339 output are less than 1 V pk-pk, and the comparator output never

goes completely on or off.

In Fig. 1a, the voltage difference,  $V_{cc}-V_e$  is about 1 V, so the current  $I_s$  can be approximated by 1/R. For example, 100 k $\Omega$  provides 10  $\mu A$ .

Mark R. Gardner, Plato V Consultant, Carroll Manufacturing Co., 1212 Hagan St. Champaign, IL 61820. CIRCLE NO. 312



1. A constant-current source (a) or sink (b) can be built with a comparator operated in an oscillating state. Capacitor C smooths the output.

# Gated programmable delay-line oscillator's repetition rate changeable every period

Need a clock-pulse generator, whose repetition rate can be changed on a period-to-period basis without settling time before changing the period length? The programmable delay-line oscillator in Fig. 1 does it, and provides 10-ns incremental changes of the time between pulses from 100 to 990 ns.

Even the first period is accurate. Moreover, the circuit can be restarted after a return to its quiescent state with a delay of only 1/2 its least period. And oscillations can be stopped any time without gener-

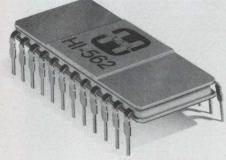
ation of extraneous pulses.

The generator's output consists of pulses about 25 ns wide. For a 50% duty-cycle, you can use the output from a flip-flop driven by the generator running at twice the output frequency. The circuit shown has worked at frequencies as high as 20 MHz. Low frequencies car be obtained by dividing the output with decade counters. Or, different base periods can be achieved with delay lines having time constants different from those in Fig. 1.

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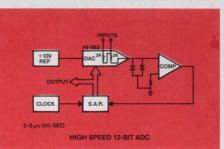
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CIRCLE NUMBER 47

The least-significant-digit (LSD) input in BCD is presented to latch  $IC_1$ , and the most-significant-digit (MSD), to down counter  $IC_5$ . Multiplexers  $IC_2$  and  $IC_3$  select the desired tap on delay lines  $DL_1$  and  $DL_2$ , which determine the oscillating frequency. Gate  $IC_4$  synchronously controls starting and stopping of the oscillator. Note: You need two eight-input multiplexers for the 10 steps of the LSD; the unused inputs are grounded. Multiplexer  $IC_3$  selects the 80 and 90-ns steps, when  $IC_1$ 's  $\overline{Q_3}$  output is low. And the circuit's logic requires the use of the noninverting outputs of the multiplexers.

When the enable signal is high for at least half a period, the circuit is in its quiescent state. Also, the output of IC<sub>4</sub> is low; therefore, all inputs to the multiplexers are low. A high pulse to the Reset line with the Enable line high initializes the circuit. Down counter IC<sub>5</sub> resets and its Borrow output, B<sub>0</sub>, goes low, since its clock line is low. NOR gate IC<sub>6</sub> and D flipflop IC<sub>7</sub> differentiate IC<sub>7</sub>'s clock input to provide a negative-going pulse at IC<sub>6</sub>'s output when IC<sub>7</sub>'s D input is high. Similarly, IC<sub>8</sub> and IC<sub>9</sub> provide a negative and a positive-going pulse, respectively, but only when IC<sub>8</sub>'s D input is low. The IC<sub>9</sub> output pulse acts as a loading signal for IC<sub>5</sub>, and the IC<sub>8</sub> output pulse as a load/clocking signal for IC<sub>1</sub>.

A period starts when the Enable line goes low. The output of IC<sub>4</sub> then goes high, and the initial positive clock edge from IC<sub>4</sub> passes through the delay lines to the multiplexer inputs. After the delayed signal ar-

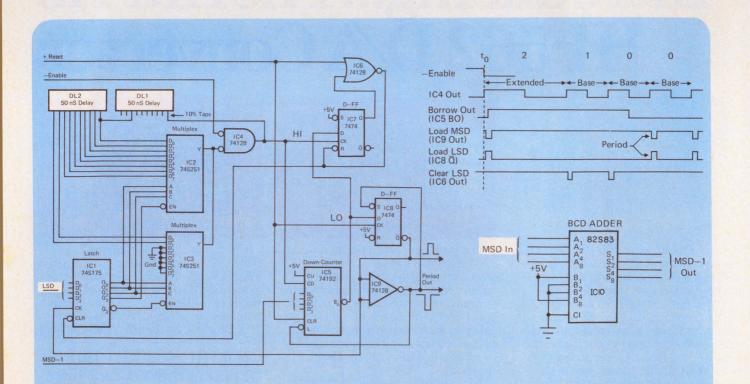
rives at the input selected by the stored LSD, it is sent back to IC<sub>4</sub>, inverted, and sent through the delay line again. After this second pass, a positive transition appears at the IC<sub>4</sub>'s output, which completes the first cycle and resets the LSD latch to zero. The first clocking cycle may be the base period determined by DL<sub>1</sub> (in this case 100 ns) or an extended period of 100 ns plus the incremental delay provided by DL<sub>2</sub>. Subsequent cycles occur at the base period until the down counter reaches zero, when an output signal can load digits available at the circuit's inputs.

Note that DL<sub>1</sub> is tapped. Select a tap that produces a 50-ns half-cycle delay when added to the multiplexer and IC<sub>4</sub> gate delay. No further tuning should be necessary. A continuously variable untapped DL<sub>1</sub> line could, of course, provide more precise initial calibration.

The data input to the down counter must be the MSD value minus one (MSD-1), since the base—or minimum—delay period is in the circuit when the loaded MSD digit is a zero. Therefore, the BCD adder, IC<sub>10</sub> must be inserted in the circuit. The adder's A inputs receive the desired MS digit, its B inputs are hardwired to the value 9 and its carry-input is held low to produce a subtraction of one.

A. M. Patlach, E-beams Device Fabrication, San Jose Research Lab, IBM, Monterey & Cottle Rds., San Jose, CA 95193.

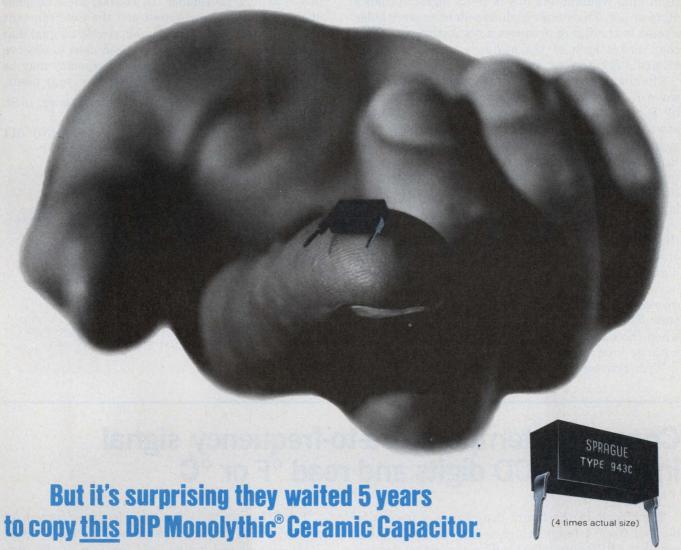
CIRCLE No. 313



A programmable delay-line oscillator with the components shown provides output pulses approximate-

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# Pulser generator determines states of three-state bus drives

When testing party-line bus systems employing three-state logic, you often experience difficulty determining whether the bus is in its high-impedance state or not. The simple high-impedance-source pulse circuit in the figure produces a distinctive waveform that makes each of the system's three bus states immediately obvious on a scope display.

The circuit employs a 555 timer to generate a square wave of approximately 1500 Hz. The network formed by R<sub>2</sub> and C<sub>1</sub> shapes the waveform to a distinctive sawtooth that is unlikely to be mistaken for a valid signal on a three-state digital bus. Variable resistor, R<sub>1</sub>, determines the signal strength and should be set to limit the drive to about half the LOW current of the logic family under test. A center setting of  $10 \text{ k}\Omega$ is suitable for common TTL.

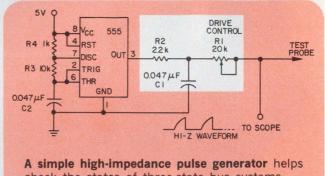
With the scope input in parallel with the test probe, the ramp waveform from the pulse generator will be observed on the scope when the bus signal is in its high-impedance state. However, if the bus has a normal signal on it, the signal will dominate the display, because the bus drive is in a low-impedance state. For this same reason the scope also will indicate when the bus is set to either a ONE or ZERO state, without interference from the ramp waveform.

With resistor R<sub>1</sub> properly adjusted, drive current

from the pulser is limited so that logic circuits connected to the bus aren't falsely triggered, while the bus is at high impedance. Of course, the frequency of the pulse-generator output and the time constant of the C1R2 low-pass filter should provide a signal that best corresponds to the sweep speed used to observe the bus. Thus, C<sub>1</sub>R<sub>2</sub> and the 555's frequency may be changed from the values shown to meet your needs.

John Walker, Consultant, Marinchip Systems, 16 St. Jude Rd., Mill Valley, CA 94941.

CIRCLE No. 314



check the states of three-state bus systems.

# Convert a temperature-to-frequency signal into four BCD digits and read °F or °C

The circuit in the figure can change a frequency derived from a temperature-to-frequency (T/f) converter to a BCD output for the display of either degrees Cor F, without switching anything in the analog input. Also, the circuit can handle temperature both above and below zero without switching ranges.

Temperature-to-voltage and voltage-to-frequency converter circuits, which have been published in the Ideas for Design columns, can be combined to form a T/f converter. None, however, provide a digital output.

The heart of the frequency-to-BCD circuit consists of five-decades of 74192 up/down counters. The leastsignficant decade is undisplayed to avoid a bobbling last digit. A temperature-converson cycle begins when the up/down counters are preset by the Load signal to a number larger than the largest negative temperature to be displayed. Simultaneously, the Minus flip-flop (7474) is cleared, which sets the decade counters to count down.

The T/f-converter pulse train is then counted for a fixed period of time determined by a 555 timer, 74161 counter and gating 7474 flip-flop. If the temperature is positive, the decade counters pass through zero. This event is detected by the 74260 zero-detector gate, which sets the Minus flip-flop and causes the decade counters to count up. At the end of the counting period the contents of the four most-significant counters are loaded into 74174 latches.

If the transfer function of the T/f converter is  $f_{out} = cT + \theta,$ 

then the circuit's master-clock period, ts, must be 10<sup>2</sup>/c, and the decade counters must be preset to a number equal to that of  $\theta \times t_s$  to read the temperature, T, in degrees C. The offset constant, O, and input frequency, fout, are in hertz and the constant, c, is in  $(degrees \times seconds)^{-1}$ . The 10<sup>2</sup> factor allows the circuit to resolve tenths of a degree. To read the temperature in degrees F, you merely preset the counter to

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CIRCLE NUMBER 49

 $[(9 \times \theta \times t_s)/5 - (32 \times 10^2)]$ 

and set the master-clock period to (9/5) × t<sub>s</sub>.

Changing the preset value of the counter is easily and directly done in the circuit with the SPST C/F switch. However, to generate the period of (9/5)  $t_s$ , the circuit starts with a primary clock period of  $t_s/5$ , and then multiplies  $t_s$  by five for reading in degrees C and by nine for degrees F. To multiply the period, the circuit simply divides the clock as required.

As an example, suppose the T/f transducer has an offset, Θ, of 20 kHz at 0 C and a temperature coefficient, c, of 400 Hz/°C. Then

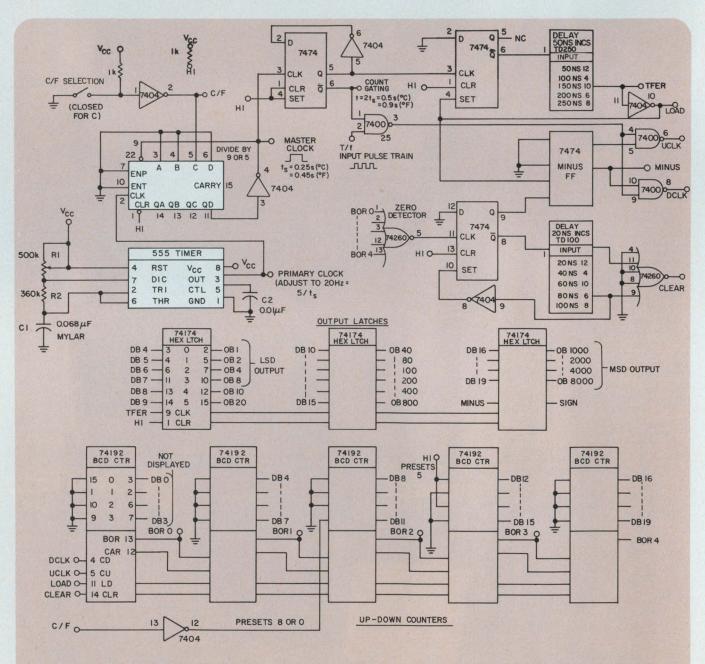
 $f_{out} = 400T + 20,000,$ 

and  $t_s = 10^2/400$ . Therefore the primary clock period is  $t_s/5 = 0.25/5$ , or 0.05 s, and the counters are preset to  $t_s \times 20,000 = 5000$  for degrees C, and 9000 - 3200

= 5800 for degrees F. To assure a square wave for the Count-Gating signal, the master-clock frequency is divided by two. Thus, the period of the Count-Gating signal becomes  $0.25 \times 2 = 0.5$ s.

Best results are attained when the T/f converter's offset count is set at a value well below the temperature range you desire to measure accurately. High offset values present little difficulty to the digital processor. A high offset has the advantage of eliminating the extreme low end of a T/f converter's output, where a large portion of its nonlinearity lies.

Glen Miranker, Research Assistant, Laboratory for Computer Science, Massachusetts Institute of Technology, 545 Technology Square, Cambridge, MA 02139. CIRCLE No. 315



A counter circuit provides a four-digit BCD output to resolve 0.1 of a degree of fahrenheit or centigrade temperature, and does it over the whole range, both below and above zero, without range switching.

# The 8080 A/D & D/A Advantage

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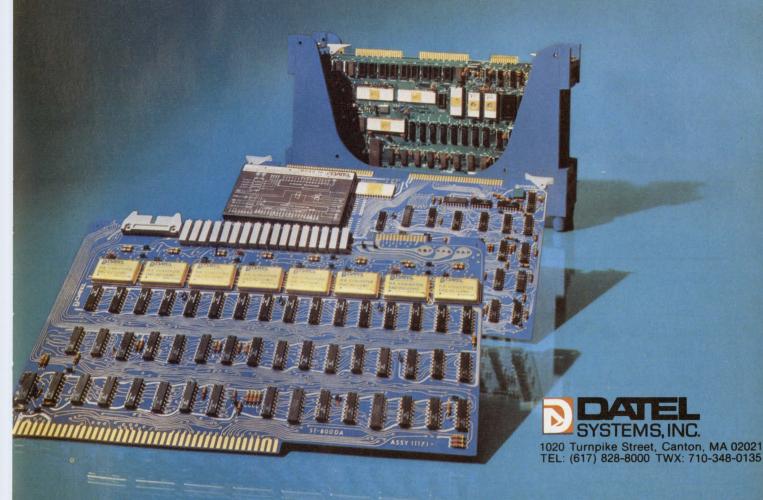
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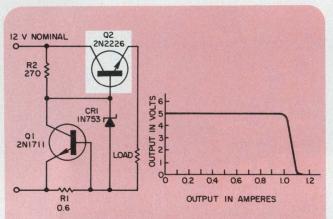
# Add foldback protection to your supply and stop pass-transistor failures

You can save your power supply's series pass transistor under shorted-output conditions by adding two resistors that provide voltage feedback. Otherwise, a sustained short circuit in a current-limiting power supply, like the one in Fig. 1, can cause a damaging temperature rise in power Darlington pass transistor, Q<sub>2</sub>.

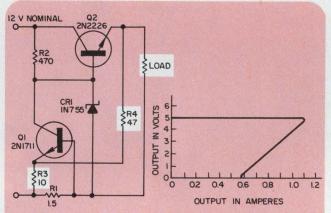
The circuit of Fig. 1 is modified by adding two voltage-feedback resistors,  $R_3$  and  $R_4$  (see Fig. 2a). Control transistor  $Q_1$ 's emitter voltage depends on the power-supply output voltage as sampled by the  $R_3$ ,

 $R_4$  voltage divider. If  $R_1$  senses a current overload, the drop across it decreases the output voltage and lowers the emitter voltage of  $Q_1$ . Then  $Q_1$  turns on at reduced current through  $R_1$ , which limits current flow through  $Q_2$  as shown in the current-foldback characteristic of Fig. 2b. You can adjust the foldback ratio by changing  $R_3$  and  $R_4$ , or  $R_1$ , or all three.

Floyd S. Griffin, Vice President, Ordnance Research Inc., P.O. Box 1426, Fort Walton Beach, FL 32548. CIRCLE No. 316



1. A conventional current-limiting power supply is protected from instantaneous short-circuits, but long-duration shorts can overheat pass transistor  $Q_2$ , leading to its eventual failure.



2. Two resistors added to Fig. 1 provide voltage feedback (a) and generate a current-foldback output characteristic (b).

#### IFD winner of September 27, 1977

Joe Orender, General Manufacturing Co., P.O. Box 5123, Wichita Falls, TX 76307. His idea "Transformer Completely Isolates Contact without a Floating Power Source" has been voted the Most Valuable of Issue Award.

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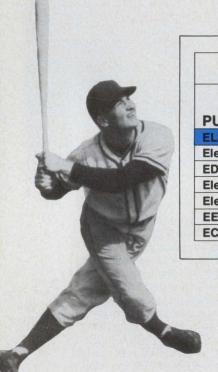
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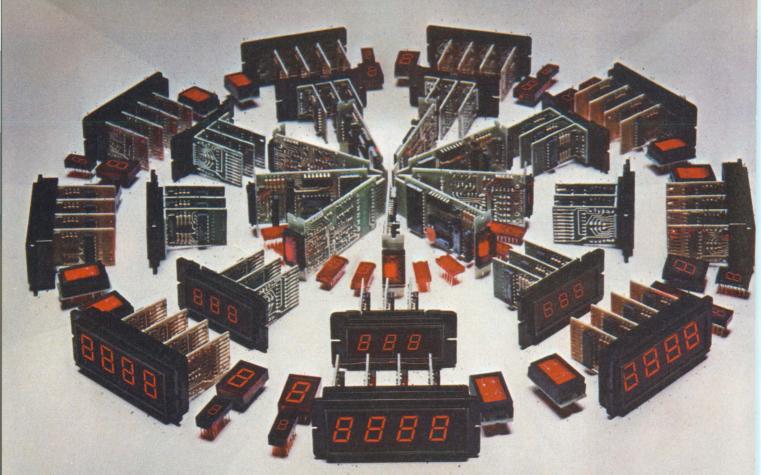
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CIRCLE NO. 301

# Make your own ICs with design kit

Interdesign, 1255 Reamwood Dr., Sunnyvale, CA 94086. (415) 734-8666. \$59; stock.

The MO-K monochip design kit contains all the ingredients you need to convert your discrete linear or digital circuits to custom ICs. Divided into linear and digital subsections, the design manual explains bipolar and n-channel MOS technologies in detail. Breadboard components are included to enable you to verify your linear circuits.

CIRCLE NO. 302

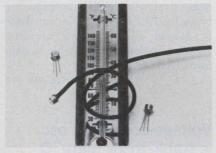
# CMOS quartz clocks drive sync motors

RCA, Box 3200, Somerville, NJ 08876. (201) 685-6423. \$1.30 to \$1.75 (100 qty); stock.

Five timing ICs, types CD22011E through CD22015E, use CMOS technology to drive synchronous or stepping motors. Each circuit consists of an input inverter for use as a crystal oscillator, a frequency divider, one or more zener diodes for transient protection and one or two output drivers. They differ primarily in quartz-crystal frequency, output-pulse width and duty cycle. With oscillator frequencies from 1.9666 to 4.194 MHz, output-pulse frequencies from 1 to 64 Hz can be obtained. The devices are in 8-lead mini-DIP packages.

CIRCLE NO. 303

# Temperature sensor spans -55 to 150 C

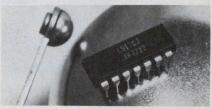


Analog Devices, 829 Woburn St., Wilmington, MA 01887. Jeff Riskin (617) 935-5565. \$1.95 to \$7.95 (100 qty).

An IC temperature sensor, AD590, is capable of 1-C absolute accuracy over -55 to +150-C range. The device is a two-terminal unit that produces an output current proportional to absolute temperature when driven by a dc supply voltage between 4 and 30 V. The sensor is laser trimmed to produce an output of 298.2 µA at 25 C. The output changes  $1 \mu A/^{\circ}C$  from that point. Three models are available. The "L" version has a calibration accuracy of ±1-C and ±1-C linearity from -55 to 150 C; the "K" version has 2-C accuracy with -1-C linearity; and the "J" version has 5-C accuracy and ±2-C linearity. Packaging is in a TO-52 metal can.

CIRCLE NO. 304

# Micropower IC drives alarm circuits



Siliconix, 2201 Laurelwood Rd., Santa Clara, CA 95054. Jim Graham (408) 246-8000. \$2.18 (100 qty); stock.

The L911 detector IC is for micropower systems requiring a high-inputimpedance comparator and alarm driving capability. The use of the circuit only requires a few resistors that control the set current of the IC and the threshold setting of the input comparator. The output can be used for logic triggering or in conjunction with higher current driver SCRs or transistors. The L911 interfaces with a variety of detector on/off control systems and monitor alarms. Input impedance is greater than 109 \Omega and current consumption is less than 10 µA at 9 V. The output current sourcing is adjustable from 0.5 to 30 mA. Housed in a 14-pin plastic DIP the L911 operates from 6 to 16-V supplies.

CIRCLE NO. 305

# Detector converts light to pulse signals

Integrated Photomatrix, 1101 Bristol Rd., Mountainside, NJ 07092. Marie Rozar (201) 233-6010.

The IPL-13 device combines a planar light sensor with amplification and triggering to provide an output frequency that is a function of incidentlight level. The trigger converts light intensity to a variable pulse rate with 2% linearity. Response peaks in the infrared at 0.8 microns, but is between 50 and 70% of the peak across most of the visible spectrum. Output rate of the 1-µs pulses varies from 10 pulses/s in the dark to 100,000 pulses/s when exposed to 30 mW/cm<sup>2</sup>. The 0.0075-in. square diode, on a 0.040-in. square silicon chip is packaged under glass in a four-lead TO-18 case.

# HV rectifier goes into magnetron supplies

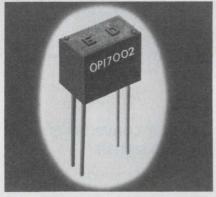


Semtech, 652 Mitchell Rd., Newbury Park, CA 91320. Bill Krause (805) 498-2111, \$1.50; stock.

The type SCMW-1 and SCMW-2 (isolated) high-voltage rectifiers are designed for magnetron power supplies. These multichip silicon rectifiers are mounted on metal flanges and encapsulated for better heat dissipation. The voltage breakdown at  $100~\mu\text{A}$  is 12 kV min and reverse operating voltage is 5 kV. The average rectified current at 55 C is 350 mA.

CIRCLE NO. 307

# HV isolator is optically coupled



Optron, 1201 Tappan Circle, Carrollton, TX 75006. (910) 860-5958. \$1.00 to \$1.15 (1000 qty); stock.

The OPI 7000 series of optically coupled isolators has an input-to-output isolation voltage of 6000 V in free air and 10,000 V when encapsulated. An isolator consists of an infrared LED coupled with either a silicon phototransistor or photo-Darlington in a molded plastic package. Standard pin spacing of 0.3 × 0.1 in. fits DIP sockets. Current transfer ratios range from 20 to 100% for the phototransistor versions (OPI 7002 and 7010), and from 200 to 400% for the photo-Darlington models (OPI 7320 and 7340).

CIRCLE NO. 308

# 3-digit chip forms low-cost DPM

Analog Devices, P.O. Box 280, Norwood, MA 02062. Joe Codispoti (617) 329-4700. \$5.50 (1000 qtu); stock.

A three-digit I²L LSI requires only 10 additional components to become a complete digital panel meter. The AD2020 chip includes an input amplifier, a comparator band-gap reference, counters, clock, control logic, multiplexer and all drivers needed to implement a dual-slope conversion DPM. Only a capacitor, three transistors, one decoder/driver, two potentiometers and three displays are needed to complete the DPM. The device is housed in a 16-pin plastic DIP.

CIRCLE NO. 309

# Bipolar transistor has low noise up to 4 GHz

Aertech, 825 Stewart Dr., Sunnyvale, CA 94086. (408) 732-0880. \$20/\$50; stock.

The ABT7701 is an npn, silicon, bipolar transistor designed for low-noise, small-signal amplifier use to 4 GHz. The transistor has typical noise figures of 1.7 and 2.7 dB at 2 and 4 GHz, respectively. Corresponding gains are typically 12 and 8 dB. The transistor is housed in a 100-mil hermetic stripline package or available in chip form (ABT7700).

CIRCLE NO. 310

# Voltage-controlled osc is stable to 20 ppm/°C

Exar Integrated Systems, P.O. Box 62229, Sunnyvale, CA 94088. (408) 732-7970. \$0.97 (100 qty); stock.

The ultra-stable voltage-controlled oscillator IC, SR-2209, has 20 ppm/°C temperature stability and 1000:1 sweep range. It comes in an 8-pin DIP and produces independent symmetrical triangle and square-wave outputs. The oscillator operates over eight decades of frequency, from 0.01 Hz to 1 MHz. The frequency is set by an external R-C combination, and it can be linearly swept over a 1000 to 1 control range. The output waveforms are unaffected by frequency sweep. An internal regulator makes the device insensitive to supply voltage changes; it can operate with a supply voltage of 8 to 26 V or  $\pm 4$  to  $\pm 13$  V.

CIRCLE NO. 320

# Voltage reference diodes have low noise

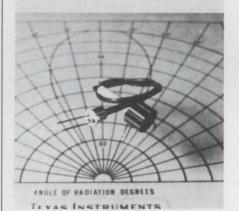


CODI, Pollitt Dr. S., Fair Lawn, NJ 07410. John Halgren (201) 797-3900. \$35 (100 qty); stock to 6 wks.

A family of low noise, ultrastable, precision reference diodes (PRD) includes an equivalent to the Motorola MZ605, the PRD 7530. This diode has a nominal operating current of 7.5 mA and time stability of 30  $\mu$ V or 5 ppm/1000 h. Noise is 1 ppm of output, and the TC is 1 ppm (at the zero TC operating current) from 25 to 45 C.

CIRCLE NO. 321

# GaAlAs diodes are sources for fiber optics



Texas Instruments, P.O. Box 5012, MS 308 (Attn: TXES475/476), Dallas, TX 75222. Jim Walyus (214) 238-4422. \$50/\$75 (100 qty).

Two gallium-aluminum-arsenide infrared emitting diodes, the TXES475 and the TXES476, have a peak emission wavelength of 790 nm to match an optical window in DuPont's new PFX-PIR infrared transmitting plastic fiber-optic cable. Two times higher output powers are achieved at this wavelength than are available with shorter wavelength emitters. The emitters are mounted in a modified TO-18 package and have an integral PFX-PIR140 fiber-optic cable for coupling the optical power from the emitter chip. Optical rise time is typically 25 ns. Output power at 50-mA diode current for a 25-cm cable length is 50 µW for the TXES475 and 75 µW for the TXES476.



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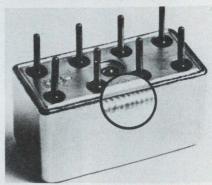




CIRCLE NUMBER 55

### COMPONENTS

### Relays packaged in welded hermetic cases



Hi G, 580 Spring St., Windsor Locks, CT 06096, John Parsons (203) 623-2481.

The Flagship series of relays is impervious to environments encountered in manufacturing and on the job, because of an all-welded metal case. The use of laser-welding techniques makes possible a degree of environmental protection hitherto available only in more costly relays. The relays are completely impervious to the strong solvents used in the cleaning of PC boards. Each relay is filled with inert gas.

CIRCLE NO. 323

### Thin wafer fan yields low noise



Rotron, Woodstock, NY 12498. Pete Rakov (914) 679-2401.

The wafer, a thin tube-axial fan with an acoustical rating as low as NC-41. measures only 1 × 3.63 in. The fan can provide up to 37-cfm free-air delivery. Motor voltage of 115 or 220 V can be supplied for nominal speeds of 2730 rpm at 50 Hz or 3300 rpm at 60 Hz. The fan is UL-recognized and CSA certified.

# **Green LEDs provide** guaranteed brightness

Litronix, 19000 Homestead Rd., Cupertino, CA 95014. Terry Snowdon (408) 257-7910. See text; stock.

Green GaP LED lamps, with guaranteed brightness, come in T-1-3/4 and T-1 sizes. The GL-4950, a T-1-3/4 size, has a large, full-flood radiating surface. At 20 mA, its guaranteed minimum brightness is 1 mcd, typical brightness is 1.8 mcd. The GL-211, a T-1 size, at 20 mA has a guaranteed minimum brightness of 0.8 mcd; typical brightness of 1.5 mcd. Both lamp types can be powered directly by standard TTL and MOS IC circuitry. Snapin mounting clips for panel mounting are available. Prices in quantities of 1000 are 30¢ for GL-4950 and 19¢ for GL-211.

CIRCLE NO. 325

# Stepper motor converts pulses to angular steps

Haydon Switch & Instrument, 1500 Meriden Rd., Westbury, CT 06705. (203) 756-7441.

A two-wire stepper motor, Type 31300, directly converts electrical impulses into discrete angular steps of an output shaft. Operating from simple "on/off" pulses, no control logic is required. The rotor turns 180° when power is applied and an additional 180° when power is removed; no power is consumed between pulses. Motors for 12 or 24-V-dc operation are available. Rotation is unidirectional, cw or ccw, and standard available step angles are 36, 30, 6 and 0.36°. Output torque at 0.36° step angle is 2.5 oz-in. at pulse rates up to 40 pulses/s. Size is 1-1/6 in. dia. by 1-1/16 in. long.

CIRCLE NO. 326

# 10-A time-delay relay spans 5-to-300-s range

Zenith Controls, 830 W. 40th St., Chicago, IL 60609. (312) 247-6400.

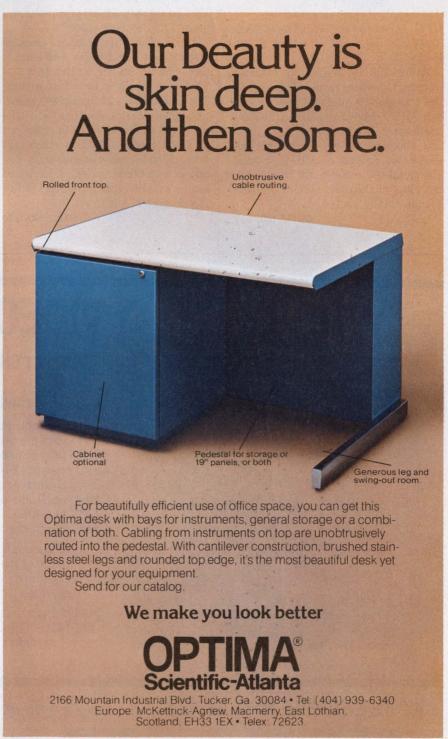
Solid-state time-delay relays, Series SS, are for electronic timing use in the range of 5 to 300 s. They feature a heavy-duty output relay with gold-flashed contacts, UL recognition, a 10-A-DPDT, 120-V-ac resistive rating and minimum life of 10 million cycles. Repeatability is  $\pm 1\%$  of full range, and its 95-to-130-V-ac input-voltage range has no effect on timing. Operating ambient temperature is -40 to 80 C.

CIRCLE NO. 327

# Rotary switches have coded outputs

Oak Industries, Crystal Lake, IL 60014. J.C. Vodnansky (814) 549-5000. See text.

Seven standard communicatorseries rotary switches are available. They include one and two-section models offering 16, 24 and 40 positions with various coded outputs. The 24 and 40-position models include a cam that acts as a precision, internal detent that eliminates both backlash from loose rotors and stack-up tolerance problems. Coded outputs available include binary 01 through 40, two-digit, sevenbar displays and 1 through 24 and hexadecimal. Price for a single-section switch is \$9.10 (1-24), \$5.46 (100); two section, \$13.78 (1-24), \$8.27 (100).



### **MODULES & SUBASSEMBLIES**

# Digital-tape transport works in hostile areas



MFE, Keewaydin Dr., Salem, NH 03079. Jim Saret (603) 893-1921. \$1150; 4 wks.

Model 250BH-1 digital tape-cassette transport operates from -30 to +55 C. The transport is qualified mechanically to MIL-E-5400R and MIL-STD-810C "Helicopter Environment" for vibration, shock and 30-g crash safety. The electronics consist of MIL-type 5400 ICs, metal-to-hermetic seal transistors and glass diodes. The unit's PC board is conformally coated.

CIRCLE NO. 329

### Smart monitor shows upper/lower case



Ann Arbor Terminals, 6107 Jackson Rd., Ann Arbor, MI 48103. Sarah Freeman (313) 769-0926. \$900; 8 wks.

Model 400W Smart Monitor modules display upper and lower case characters. Characters are written in a  $7 \times 10$  dot matrix in a  $10 \times 12$  dot field. The unit displays 20 lines of 80-character alphanumerics, with five additional lines that can be accessed in either roll or scroll modes. Blinking characters are available and the cursor is displayed as a blinking field. A keyboard can be supplied that generates the full 128-character ASCII set.

CIRCLE NO. 330

# DPM draws trickles from the battery

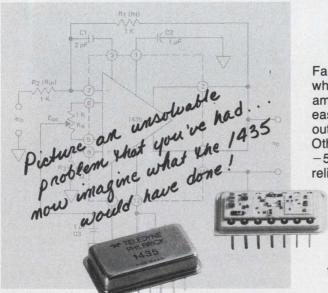


Datel Systems, 1020 Turnpike St., Canton, MA 02021. Eugene Murphy (617) 828-8000. \$49 (100 qty); stock to 4 wks.

Digital panel meter, DM-310001, draws only 3 mA from a 9-V battery. The device's liquid-crystal display includes a volt, ohm or amp descriptor label that operates under logic control. Display resolution is 31/2 digits and the input configuration is balanced differential. Automatic-zero correction eliminates the temperature drift of zero. The device measures a slowly varying or dc voltage between -2 V and +2 V and displays this voltage 3 times per second as black decimal digits against a light background. The instrument comes in a  $2.53 \times 3.25 \times 0.94$ in. plastic case.

CIRCLE NO. 331

# WHO NEEDS A VIDEO OP AMP



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You'd like to have a known, stable signal to input to your circuit, so you can tell whether its output is on target. But the multiple pulse or wave generators, flip flops, logic gates or other gear you've been using to generate your word and timing patterns just aren't enough. You can't program them easily or with any guarantee they're accurate.

You'd rather have a single instrument that has multiple channels and is easily programmed. So you can input *exact* duplicates of the real programs your circuit will be handling. So you can tell at a glance whether your output is right.

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We'll show you a self-contained, low-cost, small digital debugging tool for \$2,500 and up. A multichannel, microprocessor-controlled data and timing generator that's programmable with only 16 instructions. A general purpose tester that can generate large amounts of digital data, that's interactive, can respond to external stimuli and make decisions. A benchtop instrument that can be used rack-mounted as part of a computer-driven system, or as the core of a low-cost, stand-alone digital test system.

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CIRCLE NUMBER 58 FOR LITERATURE

### **MODULES & SUBASSEMBLIES**

# μprinter selects baud rates

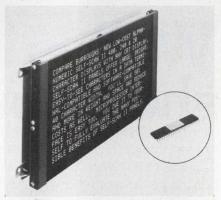


Centronics, Hudson, NH 03051. Tom Eifler (710) 228-6505. \$695.

The user can select baud rates, parity and the number of stop bits on the Microprinter-S1. The printer provides a 7-bit serial RS-232 interface, standard ASCII 96-character set and operates from 50 to 9600 baud. Copy is produced on aluminum-coated paper by an electric-arc discharge. 80 columns can be printed on 4¾-in. roll paper.

CIRCLE NO. 334

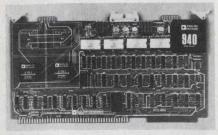
# Flat-panel display is μP controlled



Burroughs, P.O. Box 1226, Plainfield, NJ 07061. (201) 757-5000. See text; stock.

To operate the microprocessor-controlled flat-display panel, Self-Scan II. feed it 8-bit signals. The displays include editing and control routines for insertion, deletion or blinking of letters, words or lines, increasing or decreasing brightness and right-to-left data entry. The display subsystem operates off an 8-bit bidirectional bus or a TTL bus. In DMA mode, data can be entered at a rate up to 1 MHz. With the addition of a keyboard and communication interface, the combination serves as a compact data terminal. Prices in 100 quantity are: \$225, 40char; \$500, 240-char; \$750, 480-char.

# Output subsystem gives simple 8080 conversion



Analog Devices, P.O. Box 280, Norwood, MA 02062. Russ Ver Nooy (617) 329-4700. \$298/\$379.

A d/a converter board, RTI-1201, provides simplified 8080 data conversion, with hardware and software to interface the Intel SBC-80 computers to the outside world. The board is a complete 2 or 4-channel analogoutput subsystem that includes four digital outputs and is compatible with the RTI-1200 I/O interface board, the Intel System-80 microcomputers, the Intel MDS development system and the National Semiconductor BLC-80/10 board-level computer.

CIRCLE NO. 336

# Cartridge transport works on low power

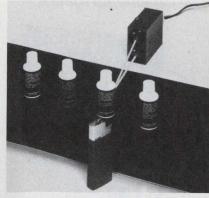


Kennedy Co., 540 W. Woodbury Rd., Altadena, CA 91001. Russ Bartholomew (213) 798-0953. \$500 to \$795; 8 wks.

A 3M-type cartridge transport, Model 631, requires only a dual-voltage power supply from which it takes only 22.6 W max during start, dropping to 8.2 W when running. The transport is bidirectional and can be equipped with one, two or four read/write and erase heads, giving a maximum unformatted storage capacity of 720 kbytes/track or 2.88 Mbytes/cartridge. Normal operating speed is 30 in/s. Using a phase-encoded format at a recording density of 1600 bits/in., the transport has a data transfer rate of 48 kbits/s.

CIRCLE NO. 337

# Scanner eliminates false triggering

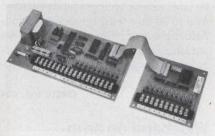


Banner Engineering, 9714 10th Ave. N., Minneapolis, MN 55441. Floyd Schneider (612) 544-3164. \$80; stock.

The SP-1000V scanner uses a narrow, modulated, converging beam to sense at approximately 4 in. and not beyond. This eliminates false triggering from background objects. The beam converges to a 0.12-in. diameter spot and is useful for sensing through narrow gaps. The beam can easily differentiate white objects an inch thick on a white background or very dark objects not easily sensed with conventional diffuse scanners.

CIRCLE NO. 338

# Electronic stepper goes forward and reverse



Vorne Industries, 5023 W. Belmont Ave., Chicago, IL 60641. Tom Canene (312) 725-3077. See text; stock to 4 wks.

A bidirectional sequencing stepping switch, Model 301, is expandable to 60 steps. The stepper consists of a master board that controls the first 10 steps and up to five slave boards of 10 steps each may be added to expand the switch. A preset switch on the master board sets the maximum number of steps in a sequence and a 0.4-in. LED display indicates each step in the sequence. The unit will switch up to 1 A at 24 V dc. Power requirement is 35 VA at 120 V, 60 Hz. Price of the master board is \$120 in 25 to 990 quantity and each slave board is \$40.

CIRCLE NO. 339

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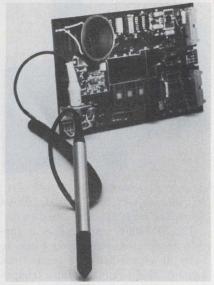
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### **MODULES & SUBASSEMBLIES**

### Bar-code reader goes into existing terminals



Interface Mechanisms, 5503-232nd St. S.W., Mountlake Terrace, WA 98043. Alison Grey (206) 774-3511. \$420 (100 qty); 4 to 8 wks.

Single-card mounting eases inclusion of the Model 9200 bar-code reader into existing terminals. The unit is a complete reader except for an enclosure and power supply. All the needed programming for normal operation is on the card and the device reads all popular bar codes including UPC, Codabar and Code 39. A bar-code tag or label can be bidirectionally scanned at 3 to 50 in/s with the device's handheld light pen. The reader processes variable-length messages up to 32 characters (standard) or 64 characters (optional).

CIRCLE NO. 404

### Wideband op amp comes in 16-pin DIP

Optical Electronics, P.O. Box 11140, Tucson, AZ 85734. Mrs. Mac (602) 624-8358. \$55; stock.

The 9932 wideband FET-input op amp is electrically similar to the National Model LH0032 and is available in a standard 16-pin DIP. The device has a differential input, which exhibits common-mode rejection at higher frequencies. Slewing rate is ±600-V/µs min at unity gain. Unity-gain frequency is 150 MHz. Output is ±10 V at 50 mA and input-bias current is 100 pA. Max settling time to 0.1% error is 100 ns. The device operates from -65 to +85 C.

CIRCLE NO. 405

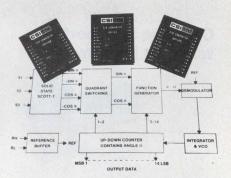
### Two-module system cuts data-acquisition cost

Micro Networks, 324 Clark St., Worcester, MA 01606. John Munn (617) 852-5400. \$137.50 (100 qty).

A two-package system, the MN 7130 multiplexed sample/hold amplifier and ADC80 12-bit a/d converter, combine to form a 12-bit 16-channel dataacquisition system costing less than \$140. The combination provides 12-bit resolution, 16 single ended or eight fulldifferential input channels, and better than a 30,000 sample/s throughput rate. The sample/hold provides input channels addressable with a single digital word and a fast, 8-us, acquisition time. An internal instrumentation amplifier is included that provides 250-MΩ input impedance and over 80 dB of common-mode rejection in the differential-input configuration.

CIRCLE NO. 406

### Synchro converters yield 10, 12 or 14 bits

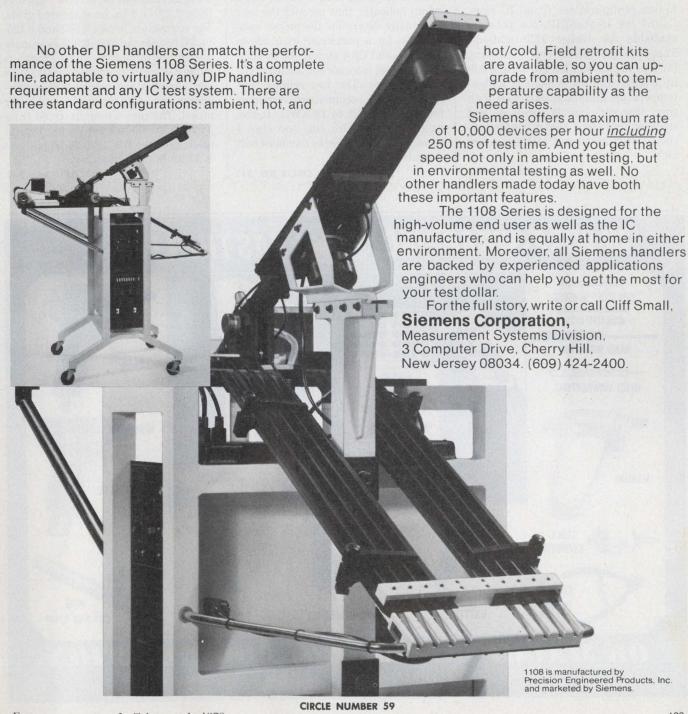


Control Sciences, 8399 Topanga Canyon Blvd., Canoga Park, CA 91304. Hal Ericsson (213) 887-7344. See text; stock.

A family of miniature synchro (or resolver) to digital converters (s/d), Type 168F, has 10, 12 and 14-bit outputs. Price for the 14-bit Model 168F100 is \$395, 10-bit Model 168F200 is \$195 and the 12-bit Model 168F300 is \$245. The devices measure 2.62 ×  $3.12 \times 0.42$  in. and operate from 50 to 1200 Hz. The 10-bit models operate at up to 65 rps with  $K_a = 30,000$ , while the 12-bit and 14-bit models track at up to 30 rps and 10 rps, respectively. Higher acceleration constants and tracking rates can be supplied when units are operated at 400 Hz or higher excitation frequencies. The 14-bit model provides ±4 min ±0.9 LSB. while the 12 and 10-bit units are  $\pm 8.5$ and ±30 min, respectively.

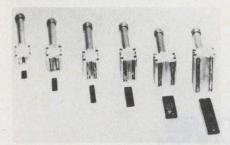
### SIEMENS

# No matter which IC test system you have, we've got your DIP handler.



### PACKAGING & MATERIALS

# Rework head solders and desolders ICs

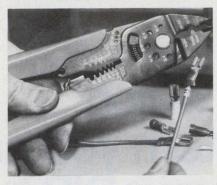


Micro Electronic Systems, 8 Kevin Dr., Danbury, CT 06810. (203) 746-2525. \$35 to \$40.

Two miniature solder pots in dualin-line configurations fit all IC sizes. Called the Heat-a-DIP, the pots are available for Weller TCP stations. There are six tips for every DIP size, for 6 to 40 pins and for 0.3, 0.5 and 0.6in. widths. The pot is made of a hightemperature aluminum extrusion with tiny iron-pot inserts pressed and soldered into slots. Solder contamination is eliminated and MIL specs are met

CIRCLE NO. 340

# Crimping tool measures compression force

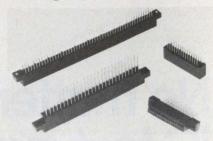


Thomas & Betts, 36 Butler St., Elizabeth, NJ 07207. (201) 354-4321.

Hand-crimping tool, WT2000, has a crimp indicator that permits the user to visually determine the proper compression for a particular wire size to meet UL and CSA standards. In addition, the tool incorporates a shear-type wire stripper. The tool crimps both insulated and noninsulated terminals for sizes from 22 to 10 AWG. It also cuts and strips wire, cuts bolt sizes 4 through 10 and reshapes damaged bolt threads.

CIRCLE NO. 341

### Solderless wrap used on edgeboard connectors

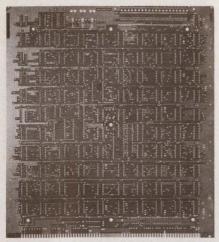


Elfab, P.O. Box 34555, Dallas, TX 75234. John Garcia (214) 233-3033. See text.

A line of solderless-wrap edgeboard connectors has 0.1, 0.125, 0.15 and 0.156-in. centers with row spacings from 0.2 to 0.3 in. on staggered grids. The connectors accept 0.062 and 0.125-in. PC boards and have 0.025-in.-square wiring terminations. The body is molded of black phenolic per MIL-M-14 and contacts are made of phosphorbronze alloy 510, finished in gold over nickel. The connectors are rated from 3 to 5 A at 600 to 1800 V rms. Typical pricing for the BW 1020 25/50 position is \$2.29 in 1000 quantity.



# Additive PC boards have solder mask



Photocircuits, 31 Sea Cliff Ave., Glen Cove, NY 11542. (516) 448-1301.

Solder-coated CC-4 additive PC boards are made by first applying a permanent solder mask to one, or more commonly to two sides of a standard bare-copper board. The entire board is then coated with hot solder and hotair leveled. This results in a uniform solder coating, 0.0003-in. thick, on the nonmasked pad areas and also through the plated holes.

CIRCLE NO. 343

# Guillotine screw allows quicker terminal wiring



Kulka Electric, 520 S. Fulton Ave., Mount Vernon, NY 10551. (914) 664-4024.

The Guillotine Screw, which gets its name from its insulating-piercing mechanism, is available on a wide variety of terminal boards and blocks. Hook-up wire can be inserted under the screw head without stripping the insulation. When the screw terminal is tightened, effective electrical contact is made right through the insulation. The terminal is made with a sharp-toothed captive washer mounted under the screw head. The terminal can be used with either stranded or solid wire of #22 through #16 AWG at 12 to 125 V up to 20 A.

CIRCLE NO. 344

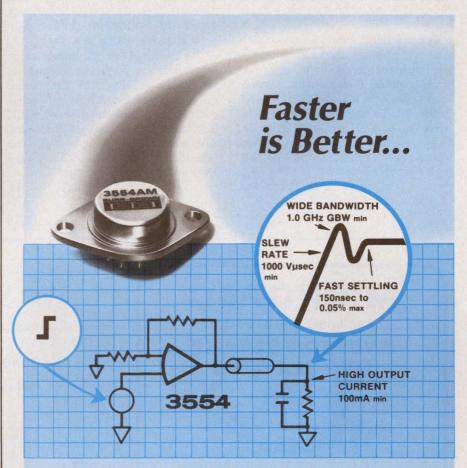
# Automatic device aids PC board assembly

Universal Instruments, P.O. Box 825, Binghamton, NY 13902. (607) 772-7522. \$13,200; 12 to 14 wks.

The Model 6232 Man-U-Sert performs all the functions of PC-board assembly except the actual component insertion. Guided by a stored program, an 80-compartment rotary bin pres-

ents the proper component, while the workholder moves the board, so that the component is always inserted in the same work area. A programmable image of 24 different characters is projected on the board to show the set of holes and the proper way a component is to be inserted. Programming can be manual with a keyboard terminal or with an off-line coordinate-measuring system.

CIRCLE NO. 345



### ...When There Are No Performance Surprises!

Designing wideband or high speed equipment? Here's an op amp that puts it all together:

Fast slewing, fast settling, large gainbandwidth product, excellent DC performance (drift of 15µV/°C) and one that produces a full 100mA output!

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means better system accuracy with transient signal conditions. High output current lets you drive heavy loads with good total frequency response.

This FET differential input op amp, priced from \$39.60 in hundreds, is fully specified in an 8-page data sheet that includes 26 performance curves, typical application information and circuits.

Contact Burr-Brown, P.O. Box 11400, International Airport Industrial Park, Tucson, AZ 85734, U.S.A. Phone: (602) 746-1111

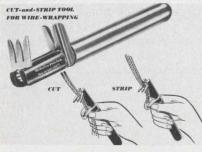


Putting Technology To Work For You

CIRCLE NUMBER 61

### PACKAGING & MATERIALS

### Tool cuts and strips wire for wrapping

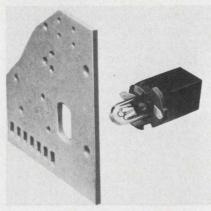


OK Machine & Tool, 3455 Conner St., Bronx, NY 10475. Judy Camen (212) 994-6600.

The ST-100 hand tool strips wire without nicking and automatically generates the proper strip length for wire-wrapping. A slim design makes it easy to store in a pocket, belt holster or tool kit. To operate, you first place wires (up to 4) in stripping slot with ends extended beyond the cutter blades. Then, you press the tool and pull. The tool handles #20 to #30 AWG.

CIRCLE NO. 346

### PC lampholder is submini size

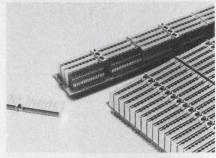


Leecraft Mfg., 21-16 44th Rd., Long Island City, NY 11101. J. Rattinger (212) 392-8800. \$0.20; 3 to 4 wks.

The Series 69-07 PC-board lampholder takes a T-1-34 size wedge-base subminiature lamp. The lampholder connects board circuitry via leaf-spring contacts and prelocated board pads. The lamp projects through the board to present a low profile, allowing the board to be positioned as close as 1/4 in. from a translucent covering panel.

CIRCLE NO. 347

### Backpanels are PDP compatible



Elfab, P.O. Box 34555, Dallas, TX 75234. (214) 333-3033.

PDP-compatible backpanels use solid-pin contacts that are press-fitted into the PC board to form a gas-tight interface with its plated-through holes. The contacts are located on a 0.125 × 0.125-in. staggered grid and housed in a thermoplastic-polyester molded insulator. The PC board is made from FR-4 per MIL-P-13949 and the contacts from phosphor bronze with 50-uin. gold over 30-to-150-µin. of nickel in the engagement area. The backpanels come in all popular slot configurations.

CIRCLE NO. 348

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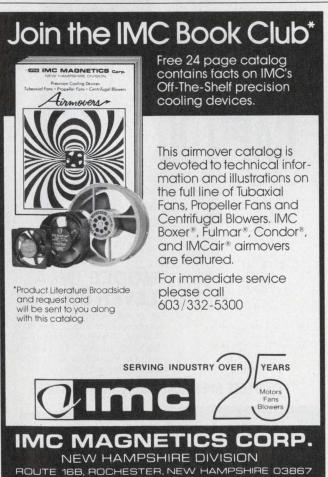
CIRCLE NUMBER 81 ELECTRONIC DESIGN 3, February 1, 1978



CIRCLE NUMBER 62



**CIRCLE NUMBER 64** 



**CIRCLE NUMBER 63** 



 No soldering required to make contact assembly by simply clamping mating surfaces together . Eliminates lead straightening and positioning . Minimum space required . Good contact without marring contact pads.

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113

### DATA PROCESSING

# Medium-distance modem operates at 4800 bits/s



Gandalf Data, 1019 S. Noel St., Wheeling, IL 60090. (312) 541-6060.

The LDM 404B medium-distance modem is for use in a metropolitan area where unloaded cable pairs are unavailable. The modem operates at 4800 bits/s synchronously with an option for a dual-channel 2400 bits/s configuration. Operation can be over standard-tariff 3002 voice-grade leased lines with most carrier systems including T carrier. No special tools or test equipment are required for installation. A built-in tuning meter simplifies alignment.

CIRCLE NO. 356

# Data recorder contains baud-rate converter



Columbia Data Products, 6655 Amberton Dr., Baltimore, MD 21227. Don Knight (301) 796-2300. Stock to 4 wks.

A data cartridge recorder with a built-in baud rate converter, the Model 300 C connects between a modem or CPU and a terminal with an online/off-line storage capacity of 1.5 × 106 char. The unit is equipped with dual RS-232 ports, dual UARTs and a 512-char buffer to get the baud-rate conversion. Speeds are selectable from 110 through 19,200 baud with current-loop capability in the terminal port. In the on-line mode, characters received on one port will be immediately retransmitted on the other port at the pre-selected baud rate.

CIRCLE NO. 357

# Terminal displays dual languages



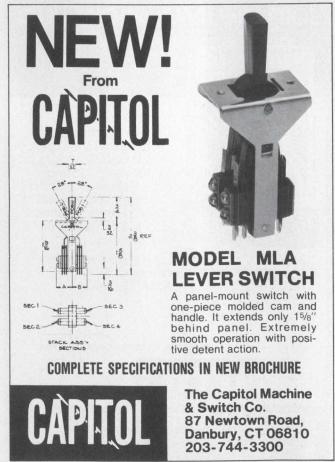
Megadata, 30 Orville Dr., Bohemia, NY 11716. (516) 589-6800. \$5800 to \$6850; 8 to 12 wks.

The dual-language terminal, Model 700/DL, operates in English plus any other language. When required, the operator can enter data from right to left. Characters are represented by a 10 × 15 matrix. The terminal includes insert, delete and text editing features. The device has a memory of up to 73 kbytes, a 126-station keyboard, a 15-in. diagonal display and rates from 50 baud to 38.4 kbaud serial, or 10,000 char parallel. The terminal is available with interfaces and protocols for most popular mainframes.

CIRCLE NO. 358



CIRCLE NUMBER 65



CIRCLE NUMBER 66

ELECTRONIC DESIGN 3, February 1, 1978





The Model 100A has the major features of more costly logic state analyzers. Operates with virtually any scope and logic family; captures and displays sixteen 8-bit words before or after a pre-defined trigger word; formats data in HEX or OCTAL groupings; offers single or repeating truth tables; provides trigger output for waveform analysis.

For more advanced applications, add the mating Model 10 Trigger Expander to the Model 100A. This integrated package offers 24 bits, qualifiers, program paging and loop analysis capabilities. Model 10 prices: KIT-\$229.00; ASSEMBLED-\$295.00; Model 100A/10 mounting baseplate-\$9.95.

Each unit includes a 100-page User's Manual.



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CIRCLE NUMBER 68

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### **DATA PROCESSING**

# IBM-compatible display has 12 lines of 40 char

Trivex, 3180 Red Hill Ave., Costa Mesa, CA 92626. R.J. Martin (714) 546-7781. \$2950.

A 480-char display, Model 0771, is compatible with IBM 3271-2 and 3272-2 controllers, and arranges text into 12 lines of 40 char each. The display is plug-compatible with IBM units; enhancements include local display-to-print, 10-key numeric pad, light pen, OCR wand, operator prompting line, cursor position display, cluster diagnostics and response time indicator. The latter displays average and maximum response time, number of transactions, and number of responses above a pre-set (0 to 30 s) response-time threshold.

CIRCLE NO. 359

# Acoustic coupler is compatible with Ma Bell

Anderson Jacobson, 521 Charcot Ave., San Jose, CA 95131. Bob Miller (408) 263-8520. \$795.

The AJ 1245 is a Bell-compatible 103 and 202-mode acoustic coupler including a modem. It interfaces with any EIA terminal and communicates acoustically at 0 to 450 baud in 103 mode and 0 to 1200 baud in 202 mode. The user switch-selects the mode and the coupler automatically adjusts baud rate and interface protocol. The unit also functions automatically, as a slave to a remote 202 modem, and simultaneously provides a 103 full-duplex interface to the terminal at speeds up to 1200 baud.

CIRCLE NO. 360

# Data digitizing stylus has one moving part

RAD, 346 Summer St., Duxbury, MA 02332. Dick Diozzi (617) 585-9440. \$105.

The RAD II digital input stylus has a removable tip and only one moving part—the Fisher #14 ink refill which activates a switch when pressure is applied. The stylus' pick-up coil is compatible with most graphic display systems, sensing the 300 mA tablet current and providing a resolution of 100 lines/in.

CIRCLE NO. 361

# Terminal combines video with daisy printer



DTC, 1190 Dell Ave., Campbell, CA 95008. Ron Lampe (408) 378-1112. From \$5000; 4 wks.

The DTC-382 Data Communications Terminal combines a video display unit with a daisy-wheel printer and provides the advantages of high-speed CRT operation with hard-copy printout. The video portion has four pages of data, each 80 columns by 24 lines, which can be scrolled over the screen. Eight different field attributes can be used. Insertion and deletion of characters and lines is standard as well as sending from screen memory to either printer and/or an RS232 line. Shadow printing, automatic underline, and plotting are included. The unit prints forwards and backwards without the need for host-computer programming.

CIRCLE NO. 362

# Modem handles data at two distinct rates

General DataComm, 131 Danbury Rd., Wilton, CT 06897. Ed Tworkowski (203) 762-0711.

The Model 212A modem handles serial data at two distinct rates over switched networks: The low-speed mode is asynchronous with a rate of 300 bits/s, while the high-speed mode is either synchronous or asynchronous at 1200 bits/s. The protocol is the same for high and low speeds. Speed selection is determined by the calling modem (by a switch or an EIA interface lead) and the answering modem automatically operates at the proper speed. Standard features include local and remote signal-loopback diagnostics, manual or automatic call origination and answering, and DTR control.

CIRCLE NO. 363

# Software package Mac is a macro assembler

Digital Research, P.O. Box 579, Pacific Grove, CA 93950. (408) 373-3403. \$70.

A macro assembler called Mac operates with a Diskette Operating System and implements the revised Intel standard macro facility. Repetition of source statements is provided with indefinite repeat on characters, text and numerics. Parameterized macros can be called out from previously defined macro libraries.

CIRCLE NO. 364

# Portable data logger operates at 32 samples/s



Sea Data, 153 California St., Newton, MA 02158. Lon Hocker (617) 244-3216. \$4195; stock.

The Model 1250 data logger is a compact unit that provides operating speeds up to 32 samples/s and storage capabilities in excess of 10 Mbits on a standard 300-ft Philips-type cassette. A high-resolution stepping motor provides an 8-channel scan interval of 250 ms with 12-bit accuracy on a single 5-Ah battery charge. The scan interval is 0.25 to 512 s and the channel scan conversion rate is 15 ms/channel. The recorder circuitry is CMOS and uses power only during scans.

CIRCLE NO. 365

# Acoustic coupler mates with Bell 212A

Omnitec Data, 2405 S. 20th St., Phoenix, AZ 85034. Paul Shatusky (602) 258-8244. \$341; stock.

The Model 701R acoustic coupler is fully compatible with the Bell System Model 212A at 300 baud. The device can be supplied to operate at data rates up to 600 baud. TTY and RS232 interfacing, acoustic or hardware coupling and half or full duplex operation are available.

# Line-voltage regulators are solid state

Superior Electric, 383 Middle St., Bristol, CT 06010. Joe McMahon (203) 582-9561. \$275 to \$695; stock.

Four solid-state Stabiline automatic voltage regulators in the SVR series are rated from 0.75 to 4 kVA. The regulators have an efficiency of 95% at 60 Hz and a correction rate of 1/2 cycle per 7-V step without overshoot or undershoot. Accuracy is  $\pm 3.5\%$  for line, load and power factor variations. All four types can be operated over an ambient temperature range of 0 to 50 C. The regulators have virtually zero waveform distortion and are insensitive to load power factor.

CIRCLE NO. 367

# Lab supply has three outputs

Amber Electronics, 17752 Sky Park Blvd., Irvine, CA 92714. Dejan Cvetkovich (714) 754-0272. \$195.

Tri-Power-Mate is a laboratory power supply with four separate outputs. The output voltages are 5,  $\pm 15$  and variable 0 to 30 V dc with current limiting at 10, 50, 100, 500 mA and 1, 2 A. Max ripple at 1 A is 0.1% (5 V), 0.3% ( $\pm 15$  V), 4 mV pk-pk (0 to 30 V). Load regulation is 0.3% ( $\pm 15$  V), 0.03% (0 to 30 V) and line regulation is 0.01% (0 to 30 V). The variable output is monitored by an ammeter and a voltmeter.

CIRCLE NO. 368

# Switchers spread 200 W over five outputs

Power/Mate, 514 S. River St., Hackensack, NJ 07601. Joe Geronimo (201) 343-6294. \$290 up.

Type ES open-frame, multiple-output, switching-regulated power supplies deliver a total of 200 W to five outputs. The dc supplies are available in a wide variety of voltage and current combinations. The supplies have efficiencies of 78% and operate to 50 C without derating. Hold-up time is 30 ms after loss of input power. Weight is 4.5 lb, size is  $11.5 \times 5.5 \times 4$  in.





## New literature



### Semi test sockets

Test sockets and carriers for integrated and hybrid circuits, MSI and LSI, rectifiers, and other semiconductor devices are highlighted in a 12-page catalog. Textool Products, Irving, TX

CIRCLE NO. 370

### **Transistors**

Specifications for 2000 transistors are contained in a 16-page catalog. Products included are high-power switching, high voltage, small signal, and rf devices. Semicoa, Costa Mesa, CA

CIRCLE NO. 371

### **Processors**

Two publications describe the HP 2240A Measurement and Control Processor. A six-page brochure describes the processor's features and its advantages in manufacturing and engineering. The second, a 22-pager, is an application note containing measuring and control examples using the 2240A. Hewlett-Packard, Palo Alto, CA

CIRCLE NO. 372

### 1978 calendar

A 1978 calendar shows the San Francisco skyline, Alcatraz Island and the Golden Gate Bridge, as seen from the bay. This four-color calendar measures 46-1/2 in. long, 10-1/2 in. wide and is suitable for framing. California Microwave, Sunnyvale, CA

CIRCLE NO. 373

### **Drafting aids**

A 132-page PC-drafting-aids technical manual and catalog is divided into two separate sections, a product catalog and a technical manual. The product-catalog portion features illustrations and data (expressed in both standard inch and metric measure) on over 15,000 printed-circuit drafting aids. Bishop Graphics, Westlake Village, CA

CIRCLE NO. 374

### Flexible keyboards

The flexible PRO keyboard for personal computer, hobbyist and OEM users is described in an eight-page catalog. Cherry Electrical Products, Waukegan, IL

CIRCLE NO. 375

### Portable oscilloscopes

Selection considerations, applications, and basic specifications of portable oscilloscopes are included in a 24-page brochure. Tektronix, Beaverton, OR

CIRCLE NO. 376

### **Bug hound**

The 2220 Bug Hound is described in a four-page brochure. GenRad, Concord, MA

CIRCLE NO. 377

### **MOS** circuits

More than 80 standard MOS large-scale-integrated circuits are detailed in a 36-page catalog. The catalog includes descriptions and functional diagrams of the AMI S2000 4-bit computer-on-a-chip  $\mu P$  and the S6800 and S9900 microprocessors and products. American Microsystems, Santa Clara, CA

CIRCLE NO. 378

### One-chip microcomputer

A 64-page reliability report covers 21-million hours of device testing of the TMS 1000 Series one-chip microcomputers. Included are a review of how MOS devices function, various failure mechanisms and a discussion of the terminology and methodology used by TI in the TMS 1000 quality-assurance and reliability program. Texas Instruments, Houston, TX

CIRCLE NO. 379

### Single-board computer

The MSC 8001, Z80 multibus single-board computer, is described in a 16-page brochure. Colored block diagrams superimposed over the board illustrate functions and interactions among the computer's various elements and buses. Monolithic Systems Corp., Englewood, CO

CIRCLE NO. 380

### Rectifiers and zeners

Electrical characteristics for semiconductor rectifiers and zener diodes are given in tabular form in a 50-page catalog. Line diagrams of the various component configurations with full dimensional data are shown. Semicon, Burlington, MA

CIRCLE NO. 381

### **Analog ICs**

A 343-page analog integrated-circuit data book provides specifications, performance curves, and circuit diagrams. Also included are a 118-page application section covering 21 topics, sections on chip geometries, quality and reliability programs, and packaging. The book costs \$2.95. Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901

### Programmable keyboards

Standard features, specifications, and diagrams of programmable keyboards are shown in a bulletin. Cortron Div., Illinois Tool Works, Chicago, IL

### Selector guide

An OEM pricing product information selector guide combines product summary specifications, industrywide cross-reference, and OEM pricing on all Siliconix products into one catalog. Siliconix, Santa Clara, CA

CIRCLE NO. 384

### **Knobs and accessories**

Over three dozen basic styles of machined-aluminum and molded-plastic control knobs are described in a 36-page catalog. Dimensional drawings detail each style; color choices are described; and prices for knobs and accessories are shown. Alco Electronic Products, North Andover, MA

# Design aids

### Wall chart/calendar

A data-converter wall chart/1978 calendar contains data-acquisition design aids such as charts, graphs and nomograms. Teledyne Philbrick.

CIRCLE NO. 386

### **Electroplating processes**

"Comprehensive Guide to Precious Metal Plating Processes For Engineering Applications" lists and describes over 60 precious-metal processes specifically designed for electronics and general industrial use. Sel-Rex.

CIRCLE NO. 387

### **Bipolar circuits**

Key specifications of high-speed LSI bipolar signal-processing circuits are presented in a chart. TRW LSI Products Div.

CIRCLE NO. 388

### **Industrial plastics**

Complete property data, application information and standard mill-shape availabilities of industrial plastics are included in a 26-page guide. The Polymer Corp., Reading, PA

CIRCLE NO. 389

### Data-comm, code charts

Two wall mountable charts are available—the RS-232C and current-loop data communication chart and an ASCII code chart. Termiflex.

CIRCLE NO. 390

### Time scheduler

With the turn of a dial on a calculator, you can find the number of business days between any two calendar days for a five or six-day workweek, the number of calendar days between any two dates and the number of seven-day weeks between two dates. The calculator costs \$3.95. Ergo Enterprises, 1241 Welsh Rd., Huntington Valley, PA 19006

CIRCLE NO. 391

# Vendors report

Annual and interim reports can provide much more than financial position information. They often include the first public disclosure of new products, new techniques and new directions of our vendors and customers. Further, they often contain superb analyses of segments of industry that a company serves.

Selected companies with recent reports are listed here with their main electronic products or services. For a copy, circle the indicated number.

Management Assistance. Data processing.

CIRCLE NO. 392

Paprican. R&D laboratory.

CIRCLE NO. 393

**Datapoint Corp.** General-purpose processors and compatible software, programs and peripherals.

CIRCLE NO. 394

General Instrument. Data products, cable-TV products, components and semiconductors.

CIRCLE NO. 395

The Plessey Co. Telecommunications and telegraphic equipment, electronic equipment including radio and radar, aerospace equipment and industrial hydraulic products, electronic and mechanical components.

CIRCLE NO. 396

Tocom. Bidirectional cable systems.

CIRCLE NO. 397

Computer Automation. Minicomputers, data-processing systems and automatic test equipment.

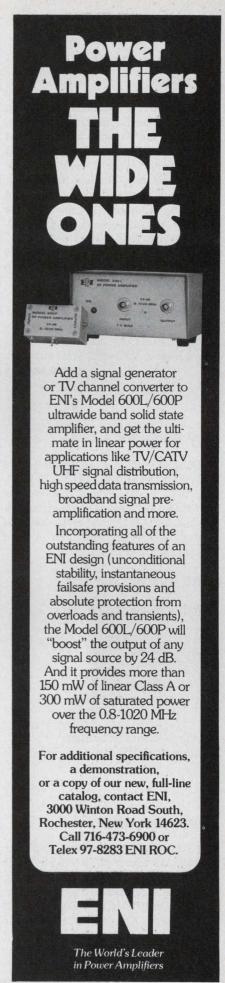
CIRCLE NO. 398

Network Systems. Adapters to interconnect computers and peripherals.

CIRCLE NO. 399

**Inco Ltd.** Metals, batteries and related products.

CIRCLE NO. 403



**CIRCLE NUMBER 74** 

### Across the desk

(continued from page 7)

the instruments mentioned have been on the market for nearly eight years. It struck me as odd, however, that Rockland System Corp.'s name was not mentioned in your "Need More Information?" box. We have been manufacturing frequency synthesizers—and indeed have dominated a portion of the frequency synthesizer market, according to Frost & Sullivan—since 1971.

David Kohn Vice President, Marketing

Rockland Systems Corp.

Ed. Note: Sorry about the oversight. For more information contact: Rockland Systems Corp., 230 W. Nyack Rd., West Nyack, NY 10994. (914) 623-6666.

CIRCLE NO. 318

### Try these for size

Douglas Varney's "Determine Wire Size with Equations" (ED No. 20, Sept. 27, 1977, p. 20) brings to mind the following well-seasoned equations for estimating AWG sizes; cross-sectional areas, in circular mils  $(A_{\rm cm})$ ; and diameters, in mils  $(D_{\rm m})$ :

 $AWG = 10 \log (325^2/A_{cm}).$ 

 $AWG = 20 \log (325/D_m).$ 

 $A_{cm} = 325^2/10^{\frac{AWG}{10}}$ 

 $D_m \ = \ 325/10^{\frac{AWG}{20}}.$ 

David Michael Myers Chief Engineer

Autocybernism Unlimited Hughesville, MD 20637

### Ten years after

I was rather disappointed with your "new" instruction set (see "Late WOM Tester," ED No. 21, Oct. 11, 1977, p. 7). With the exception of one instruction (IDC: Initiate Destruct Command, in place of EM: Emulate 407), this set is at least 10 years old. I first obtained a copy of this set, then entitled "Proposed 360 Instructions," from my college roommate, who in turn had ob-

tained it from his older brother, who at the time was a student at Reed College in Oregon.

Steven P. Northrup

Monroe The American Road Morris Plains, NJ 07950

### Get the picture?

Our apologies to everyone—especially PolyMorphic Systems, Santa Barbara, CA—for a pix mix on p. 219 of ED No. 21, October 11, 1977. The photo is of asynchronous line drivers by Micon Systems, Chatsworth, CA. Here's what the PolyMorphic System 8813 compact, complete disc-based microcomputer really looks like:



### **00FF!**

Say, processor manufacturers. How about having future processor instruction sets include both 0016 and FF16 as NOP codes? Users could then include both unprogrammed "little gaps" in their PROM programs into which jumps could be inserted for program changes or field updates. Fusible-link PROMs and EPROMs could then be modified quickly without redoing the entire program. One could also eradicate incorrect code statements by overwriting up to the next "little gap." Many systems won't find the NOP time objectionable but rather a fair tradeoff for easier development and field updating.

> John Robertson President

Telesis Laboratory P.O. Box 387 Chillicothe, OH 45601

# Give me a standard text editor anytime

Add me to the list of those who want a standardized interactive text editor. Now that I'm using brand XXX editor in the morning, brand XX in the afternoon and cheapo brand X at night at

home, I've begun to kick my dog. And all because 1A in XXX = 1L in XX = A1 in X. And 1L = 1T = V1 and Gstring 1\$-1C2\$ = Cstring1\$string 2\$ = C/string1/string2/ and 1K = 1K = D1. "Insert," in XXX and XX, inserts before the current line, but after the current line in X. And so on, ad nauseum.

Why not a standard text editor just as there is a standard FORTRAN? As with FORTRAN, it would be difficult to define I/O commands, i.e., those that read into or write from the text buffer. But it's easy enough to define a standard set of buffer-manipulation commands. How does one go about getting the ANSI, IEEE, or EIA interested in writing a draft proposal? And how does one find out if there is enough popular support for such a standard?

Mike Duncan Engineer

Atmospheric Technology Div.

National Center for Atmospheric
Research
P.O. Box 3000
Boulder, CO 80303.

### Clearly invisible display

The caption under Fig. 2 of a recent article on EMI control (ED No. 25, Dec. 6, 1977, p. 76) insists that the display "clearly shows the grid coordinates where the picture was taken." Because the printer failed to separate the red color of the original photo, the display clearly shows nothing. The real reading should have been:

115 MG 6930 6589

# Right product, wrong company

Somehow, Barber-Colman got listed as a vendor of stepping motors in our article on the subject in ED No. 22, Oct. 25, 1977, p. 48. The company makes fractional horsepower motors, but not the stepping kind. If you're interested.

CIRCLE NO. 319

### Me an editor?

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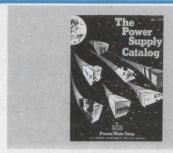
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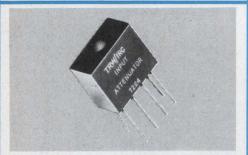
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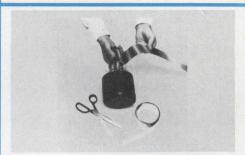
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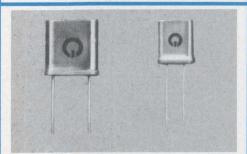
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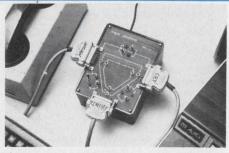
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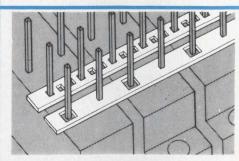
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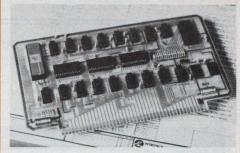
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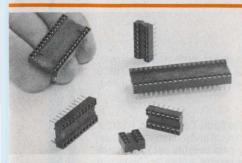
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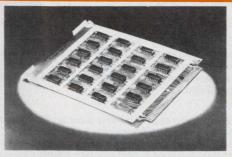
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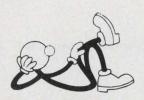
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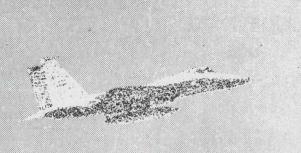
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## Advertiser's index

Advertiser	Page
AMP, Incorporated	32H 82 4, 5 68, 69 128
B & K Products of Dynascan Corporation Beckman/Helipot Division Bourns, Inc., Trimpot Products Division C Burr-Brown Research Corporation	over II
Capitol Machine & Switch Co., Inc., The	11 113 122 123 123 123 66 123
Dale Electronics, Inc	93, 95
Eagle Magnetics, Inc	122 119 121
Fairchild Semiconductor	12, 13 123 106
GTE Sylvania GenRad General Electric Company, Instrument Rentals General Electric Company, Semicon- Products Department Gould, Inc., Electronic Components	123 32D ductor 83
Hamilton/Avnet Electronics Harris Semiconductor, A Division of Harris Corporation Hayden Book Company, Inc*105, 108	87
Inc	8, *109 7, 78-79 115
IMC Magnetics Corporation Intel Corporation Intel Memory Systems Interface	8, 9 77 05, 107 115
Johanson Manufacturing Corp	
Kepco, Inc	46
Memodyne Corporation	123

Advertiser	Page
Micro Devices Corp  Micro Switch, A Division of Honeywell  Micropac Industries, Inc  Miller-Stephenson Chemical Co., T	112 he 6
Mostek Corporation  Norplex Division, UOP, Inc	. 24, 25
OK Machine & Tool Corporation. Optron, Inc	110
Panduit Corporation Paratronics, Inc* Philips Electronic Components	114
and Materials	105
Q-Matic Corp	122
RCA Solid State Division. C Rental Electronics, Inc. 32 Rockwell International. Rogers Corporation.	2A, 32G 50, 51
SMK Electronics Corporation of America. Scientific Atlanta Inc./Optima Div. Semtech Corporation. Siemens Corporation. Sierracin/Sylmar. Slaughter Company. Sprague Electric Company. Statek Corp. Systron-Donner.	23 109 17 112 37, 89 122
TDK Electronics. TRW Capacitors, an Electronic Com Division of TRW, Inc TRW/IRC Resistors, an operation Electronic Components. Tecknit. Tektronix, Inc Teledyne Philbrick. Teledyne Relays,	nponents 32B of TRW 122 113, 115 49
A Teledyne Company. Teledyne Semiconductor. Texas Instruments, Incorporated. Thermalloy Company. Triplett Corporation.	52
Union Carbide, Components Department United Systems Corporation Unitrode Corporation	82
Woodtron Ltd	
Zilog	16A
RECRUITMENT	
Cadre Corporation. Hewlett-Packard. National Personnel. Northrop. Sencore. Steve Sons. Vought Corporation.	127 125 125 127
	7)

# 74.95 JL SOURCE.

It's CSC's DP-1: the automatic signal source that cuts hours from trouble-shooting TTL/DTL, CMOS and other popular logic circuits. SPECIFICATIONS

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This compact, circuit-powered unit lets you inject signals at key points to test digital circuits with fast stimulus-response troubleshooting techniques. Just set a switch to the proper logic family; connect two clipleads to the circuit's supply, and touch the DP-1 probe to a node. It automatically senses the circuit's condition (high or low state) and produces an opposite-polarity pulse of the proper level. That's all there is to it!

Versatility-flexibility. Select single-pulse or 100 pulse-per-second operation with the handy pushbutton control. A LED indicator signals single-shot or continuous mode. DP-1 can also be connected indefinitely, presenting a 300K impedance to the circuit under test. Short circuits can't harm it, even over prolonged periods. It's also protected against overvoltage up to 25V and reverse-polarity up to 50V.

For all its versatility, portability, operating ease and compact size, DP-1 is priced at only \$74.95—a fraction of what you'd expect to pay for a precision digital pulse source. Order today. Call 203-624-3103 (East

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Logic family switch—Sets proper pulse level for TTL/DTL or CMOS families

Rugged, high-impact plastic case-Built to take it lab or in the field.

Protected - Features built-in short-circuit, overvoltage and reverse-polarity protection

Operating mode pushbutton-Selects single-shot or 100 pps operation

LED Pulse indicator — Monitors operating mode

Interchangeable ground leads connection - provide ground-side input connection, where desired, via optional cables.

Interchangeable probe tips-For greater versatility. Straight tip supplied: optional alligator clip and insulated quick-connecting clip available

Plug-in leads - 24" supplied, with nor alligator clips.

Tri-state-output—DP-1 is isolated from circuit under test: Z≥300K Auto-polarity pulse sensing - DP-1 automatically produces proper polarity pulse for circuit under test: logic "0" level produces a "1" pulse; logic "1" level produces a "0" pulse

LED indicator - flashes once for single pulse, stays lit to indicate pulse train

Short-circuit protection - can pulse into short circuit continuously

Power - overvoltage protected to 25V, reverse-voltage protected to 50V; voltage range 4-18V, 30mA max.

Pulse modes - Single pulse; press pushbutton for one sec. or less. Pulse train (100pps): hold pushbutton down

Pulse specs TTL CMOS

Pulse width 1.5usec + 30%

Fan out 60 loads Sink and

Source 100nsec T,

T,\* one TTL load, 500nsec

10usec + 30%

100mA source 50mA source to logic to 3.5V; sink to 6V 1; sink to logic 0 100 nsec 100K load. 8nsec

\*T<sub>r</sub> is directly proportional to load resistance

Dimensions (I x w x d) 5.8 x 1.0 x 0.7' (147 x 25.4 x 17.8mm) Weight 3 oz. (.085kg)

Power Leads plug-in 24" (610mm), color coded insulated clips; others available

ACTION	MOMENTARY PRESS OF PUSH- BUTTON	RELEASE PUSH- BUTTON	CONTINUOUS PRESS OF PUSHBUTTON (OVER 1 SEC.)
LED	* FLASHES	O	ON
	DP-1 SENSES LOGIC "1" (HIGH) PRODUCES "0" PULSE OR 100 PPS PULSE TRAIN		
PUT	LOGIC 1 LOGIC 0		$\mathbf{m}$
OUTPUT	DP-1 SENSES LOGIC "D (LOW) PRODUCES "1" PULSE or 100 PPS PULSE TRAIN LOGIC 1 LOGIC 0		

NOTE SEE SPECIFICATIONS FOR DUTY CYCLE

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