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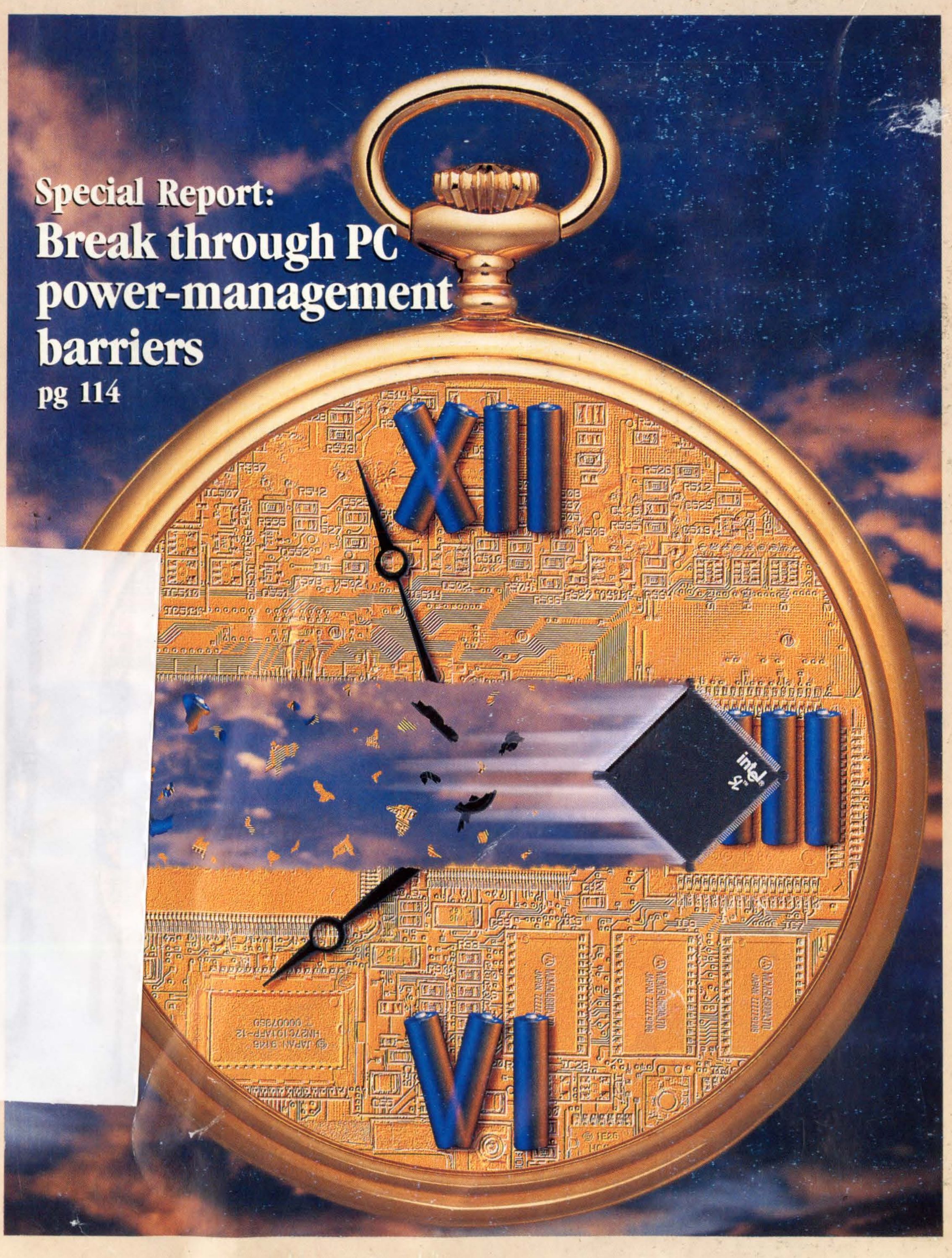
A CAHNERS PUBLICATION
October 15, 1992

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

PROCESSOR UPDATES PG 79



Special Report:
Break through PC power-management barriers
pg 114

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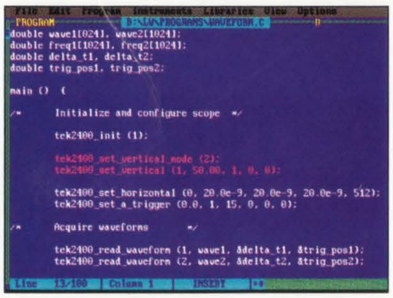

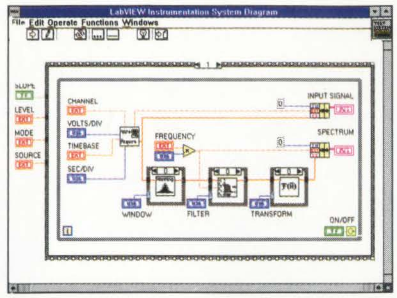

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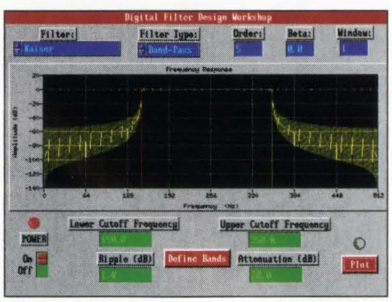

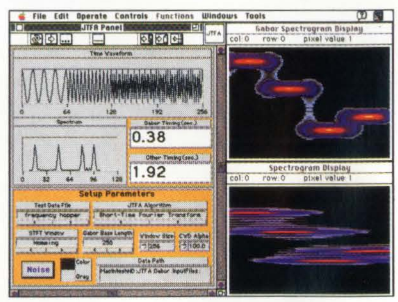

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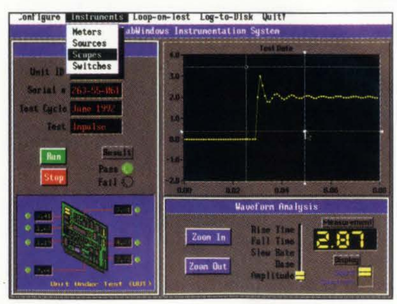

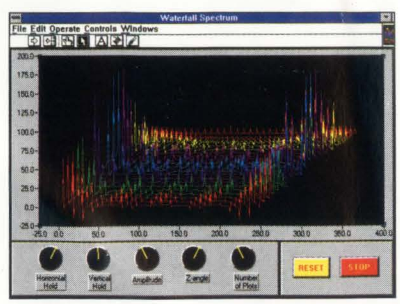

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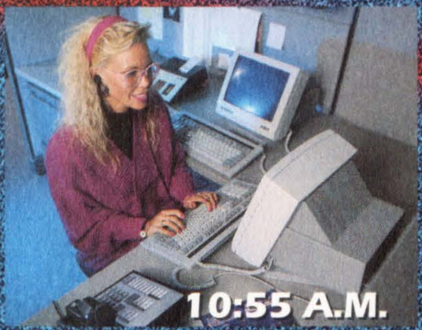

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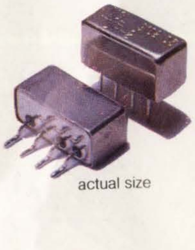

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SPECIFICATIONS

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TUF-3	7	0.15-400	4.98	0.34	46	5.95
TUF-3LH	10		4.8	0.37	51	7.95
TUF-3MH	13		5.0	0.33	46	8.95
TUF-3H	17		5.0	0.33	50	10.95
TUF-1	7	2-600	5.82	0.19	42	3.95
TUF-1LH	10		6.0	0.17	50	5.95
TUF-1MH	13		6.3	0.12	50	6.95
TUF-1H	17		5.9	0.18	50	8.95
TUF-2	7	50-1000	5.73	0.30	47	4.95
TUF-2LH	10		5.2	0.3	44	6.95
TUF-2MH	13		6.0	0.25	47	7.95
TUF-2H	17		6.2	0.22	47	9.95
TUF-5	7	20-1500	6.58	0.40	42	8.95
TUF-5LH	10		6.9	0.27	42	10.95
TUF-5MH	13		7.0	0.25	41	11.95
TUF-5H	17		7.5	0.17	50	13.95
TUF-860	7	860-1050	6.2	0.37	35	8.95
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TUF-860MH	13		6.8	0.32	35	11.95
TUF-860H	17		6.8	0.31	38	13.95
TUF-11A	7	1400-1900	6.83	0.30	33	14.95
TUF-11ALH	10		7.0	0.20	36	16.95
TUF-11AMH	13		7.4	0.20	33	17.95
TUF-11AH	17		7.3	0.28	35	19.95

*To specify surface-mount models, add SM after P/N shown.

■ $\overline{X}$ = Average conversion loss at upper end of midband ($f_U/2$)

δ = Sigma or standard deviation

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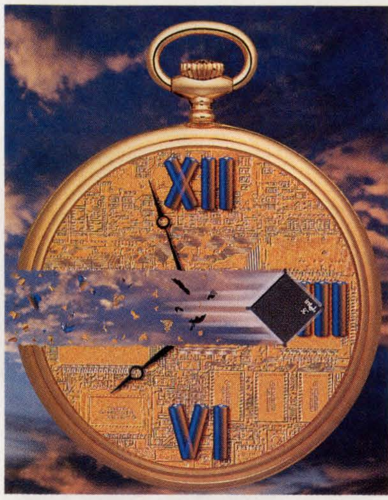
CIRCLE NO. 3

F 145 REV. F

EDN
MAGAZINE EDITION

October 15, 1992 VOLUME 37, NUMBER 21

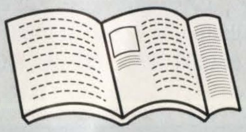


On the cover: The time is right for you to check out the power-saving features that are revolutionizing the design of portable computers, from laptops and notebooks to check-book-sized palmtops. The Special Report on page 114 describes the technology that provides the key to improving power management. (Photo courtesy Intel Corp)

Continued on page 7

Foldout Contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.



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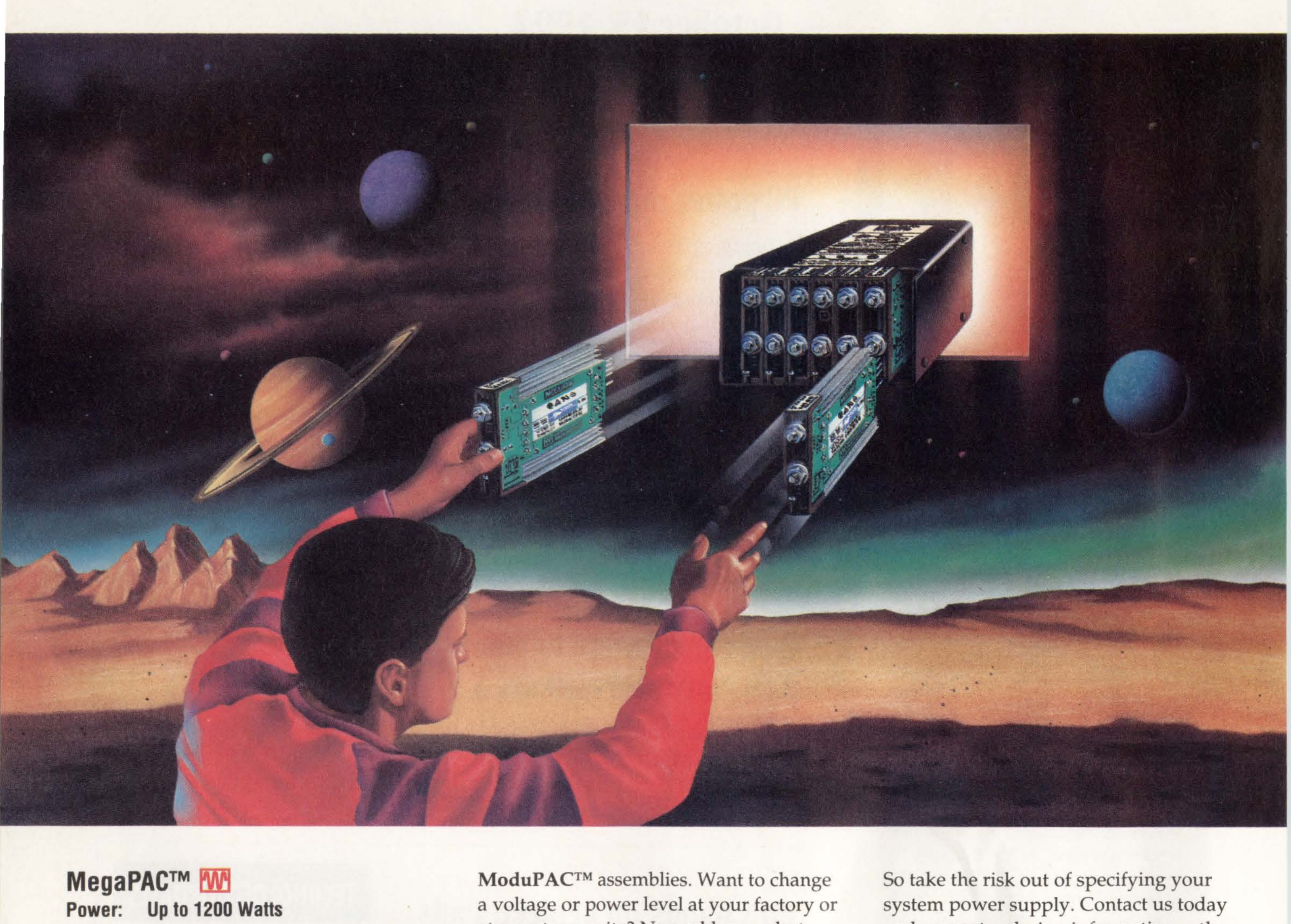
POWER To Configure



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Component Solutions For Your Power System

CIRCLE NO. 5

EDN
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October 15, 1992

Continued from page 5

TECHNOLOGY UPDATES

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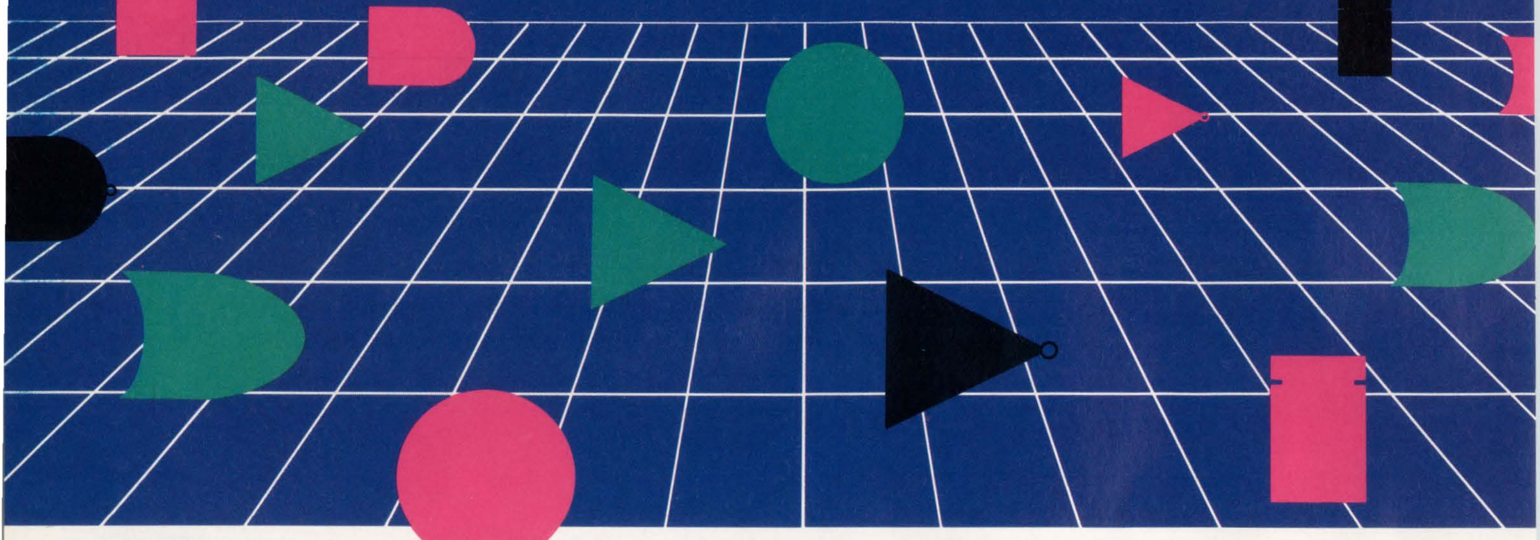

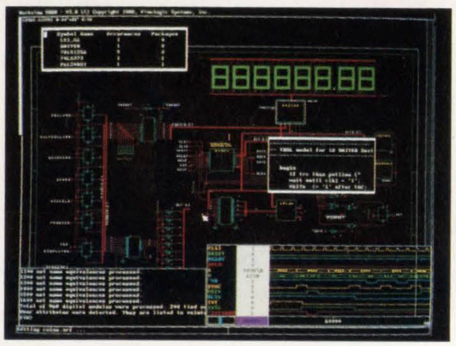

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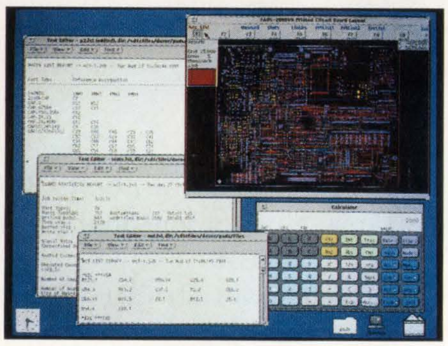

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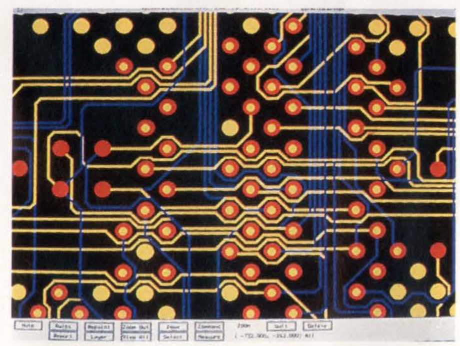

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CIRCLE NO. 6

A summary and analysis of articles in this issue

John Gallant foresaw a strategic writing problem soon after he began investigating **power management for personal computers** for this issue's Special Report. "I found that the topic was enormous. Anybody that has anything to do with making portable computers is putting power-management features into their products, almost down to the nuts and bolts. Certainly anything electrical has a 'power hook' in it these days."

John's problem was figuring out a way to limit the potentially enormous scope of the article. He decided to concentrate primarily on the power-management modes of the most widely used microprocessors for today's portable computers, opting to include a synopsis of how the modes operate.

"Low-power management is one of the big revolutions of the 1990s, and the motivation is, of course, portable computers," says John. But it's not just hardware that's being modified. Because of all these extra power hooks, BIOS vendors have had to come up with innovative power-management firmware. In his Special Report, John covers the developments in both hardware and software power management and also takes a look at what designers have to deal with before the complete changeover to 3V devices occurs.

Continuing his hands-on reports on design software, Doug Conner lets you know what it's like to work with **Pads Logic for schematic entry and Pads 2000 for pc-board design.** (His hands-on review of Accel's Tango products appears in the May 21, 1992, issue.) "I spent two solid weeks learning the software, and took a couple of days to design a board on it." Overall, he was impressed and found only a few nits to pick.

By taking the time to learn this and other design-software packages, Doug says his future articles that cover the CAE software area can only benefit from his user perspective. He's looking forward to evaluating more products during the coming year.

In Part 2 of Dan Strassberg's Design It Right Series, you're in for a behind-the-scenes design story of three computer products from Force, Tusk, and Quantum. Take a look at the lessons each company learned in the do's and don'ts boxes—maybe there's something you can use to further a pet project.

In Dan's 4-part **Design It Right** series, only Part 2 covers products that fall outside the test and measurement area. Why? Dan polled all of EDN's technical editors and sent letters to over 80 companies, asking everyone to nominate products that had good design stories associated with them. Out of about three dozen nominations, he selected the 12 products that he believed had the most educational design stories to tell. Except for the three computer products you'll read about in this issue's article, the rest are test related, which is not surprising (but also not intentional): Dan is our resident test expert.

After talking to Force, Quantum, and Tusk for Part 2, Dan found that the breakneck pace of the computer-and-peripheral business allows little time to correct errors of any type. The technology is evolving so swiftly that design teams have to be more efficient in that area than in just about any other segment of electronic equipment manufacture. Getting in and out with clean designs is the name of the game.

Joan Morrow Lynch
Managing Editor

Soon, Eight Ho
Computing Will

(actual size)

AMD Introduces The World's First 386 Microprocessor With 3-Volt Technology.

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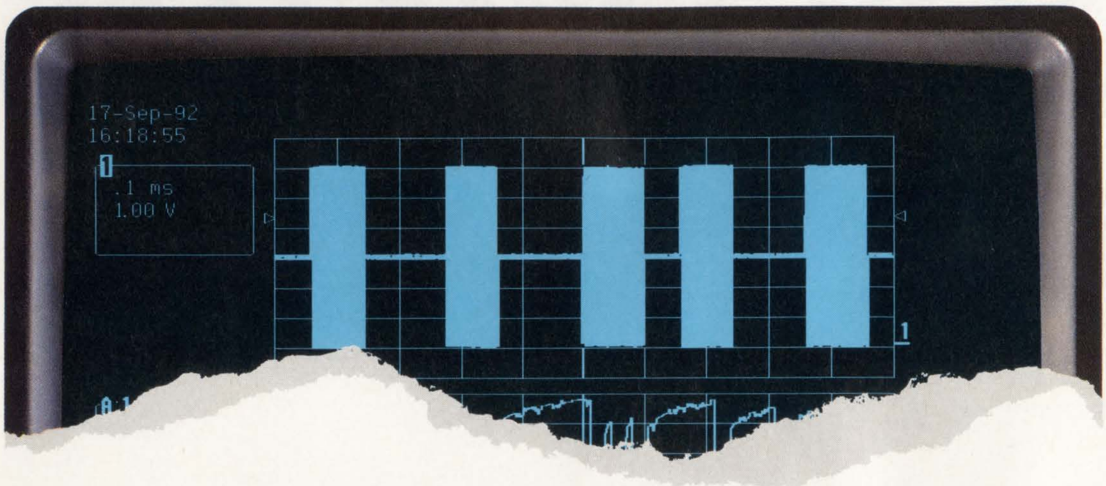
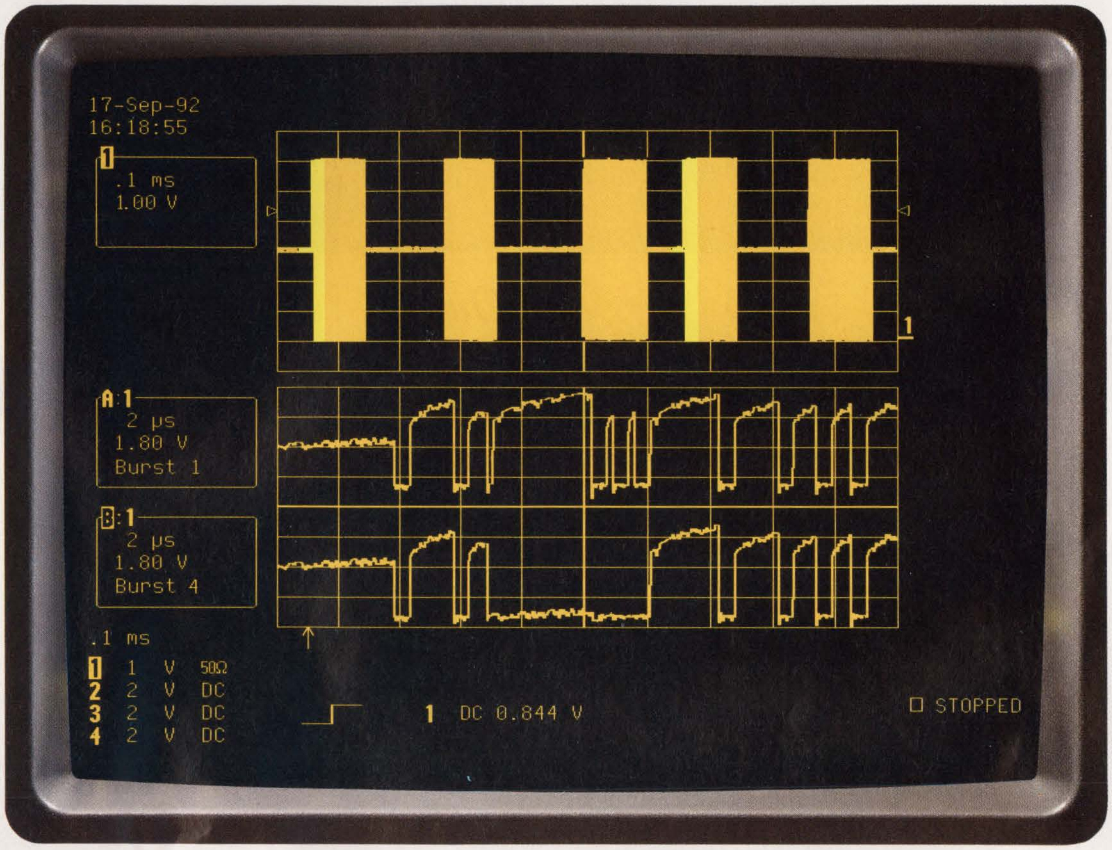
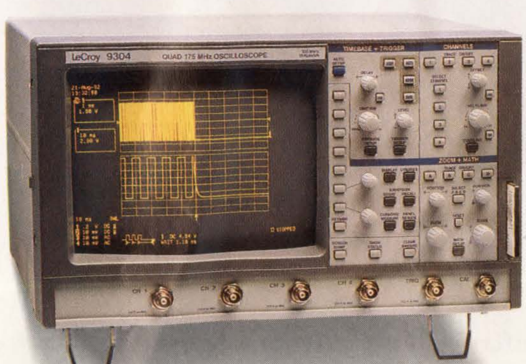
If you're only getting half the picture...



...talk to LeCroy.



Your analog oscilloscope gave you the whole picture. You'd set the trigger and the timebase, then use delayed sweep to examine the details. Measure precise timing. Or compare pulses in a stream.



But when you cross over to digital, will you still get the whole picture? Most digital scopes can't show you a live waveform and an expanded portion **simultaneously**. And if you can't see both together, how can you tell where the expansion really is?

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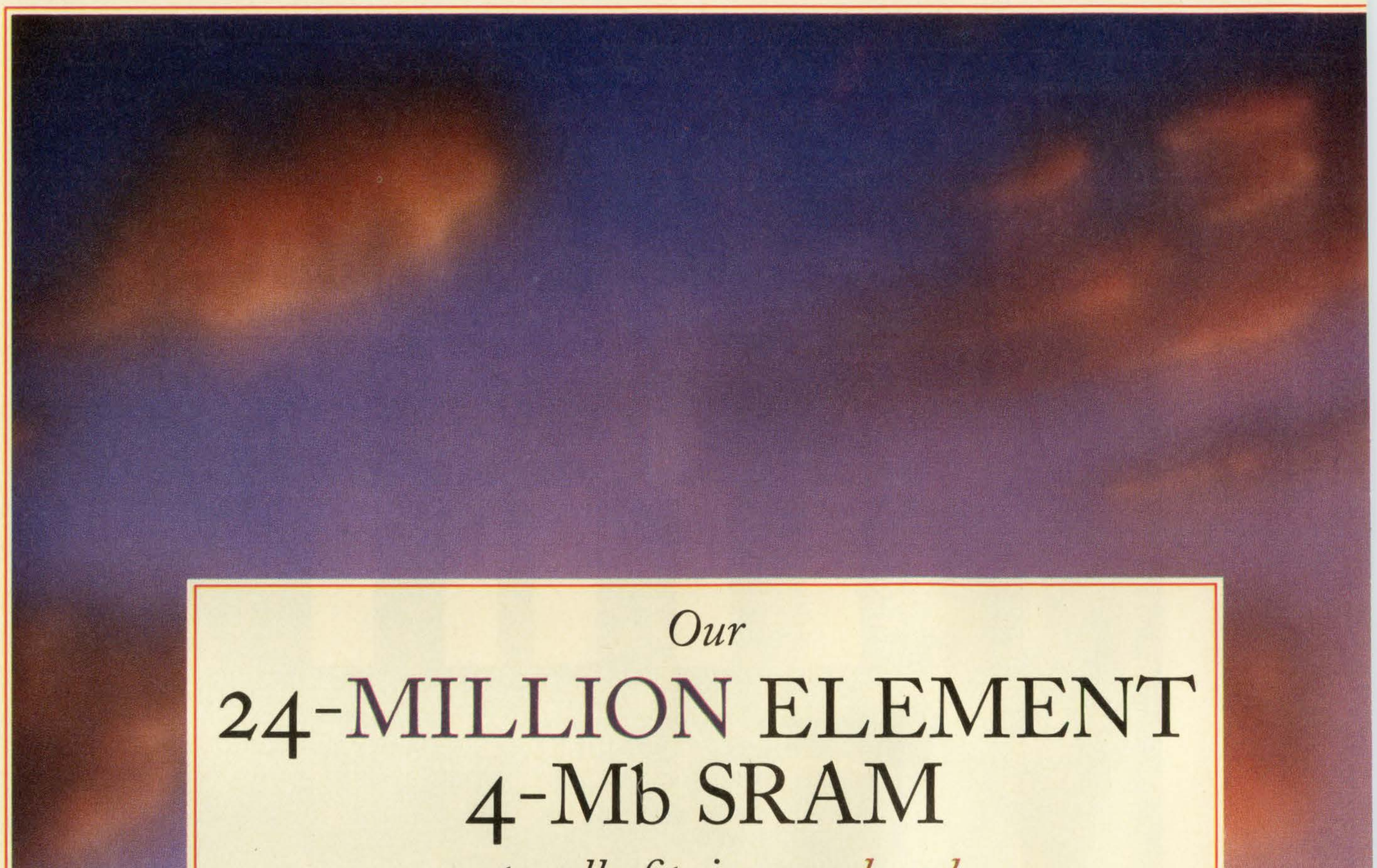

With 18 million transistors and a total of 24 million elements, the 4-meg SRAM is the most complex memory device ever made.

But the products that will be built with it are even more extraordinary. Personal Digital Assistants, handheld notebook and pen-based computers—all with power only available in mainframes a few years ago. And complex telecommunications switches, video phones, robotics, and interactive cable systems will use the 4-meg SRAM too.

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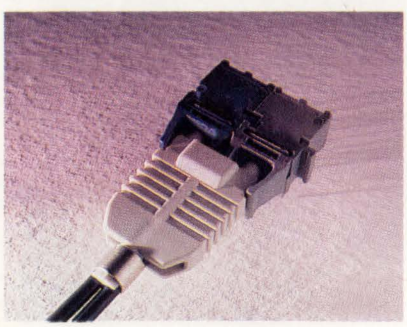
HP's 50 MBd Plastic Fiber-Optic Data Links. Anything else would be twisted.



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CIRCLE NO. 17

EDITED BY SUSAN ROSE

68300 ICEs with trace ability cost $4995

Huntsville Microsystems' $4995 Lite in-circuit emulators (ICEs) for 68300-series processors (including the 68340 and HC16 family) cost less than half as much as other comparably powerful hardware-based debugging tools for these processors. There are other 68300-series debugging tools in the same price range, but they lack some of the Lite units' key features, such as a 4k×63-bit trace buffer. The 4.8×4.5×1.5-in. emulators, which are no larger than the pods of many other ICEs, clip directly onto the target processor's pins or plug directly into its socket. Emulation RAM is 256 kbytes. The emulators handle dynamic bus sizing and mapping of all chip-select signals. The vendor's Sourcegate debugger accompanies each unit. The debugger, available in MS-DOS and Unix versions, provides source-level debugging of code generated by all major C and Ada compilers. Huntsville Microsystems Inc, Huntsville, AL, (205) 881-6005.—by Dan Strassberg

PC/104 consortium gains momentum

The PC/104 Consortium, a group of companies that manufactures small, stack-together modules for embedded-computer applications, shows evidence of gaining momentum. At the recent Buscon exhibit in Boston, MA, 14 companies announced new PC/104 modules, and 13 other companies announced that they have recently joined the consortium. The consortium was formed in January 1992, and now has 46 member companies.

PC/104 modules conform to a standard, which is published by the consortium, that defines a compact, modular form-factor for adding PC and PC/AT functions to embedded applications. PC/104 modules measure 3.6×3.8 in. and provide a stacking bus connector that eliminates the need for backplanes and card cages.

New PC/104 modules announced at Buscon perform a range of functions for embedded control that include data acquisition, processing, text-to-speech conversion, and touch-screen control. One company, WinSystems, introduced an 80386SX-based module that connects either to other PC/104 modules or to an STD bus. PC/104 Consortium, Sunnyvale, CA, (408) 245-9348, FAX (408) 720-1322; WinSystems, Arlington, TX, (817) 274-7553, FAX (817) 548-1358.—by Gary Legg

Specify FPGA timing needs up front

A key concerns for FPGA-(field-programmable gate array) designers is whether the circuit will run fast enough to meet system timing requirements. XACT-Performance from Xilinx lets designers using the company's FPGAs specify the timing performance they need up front during schematic design. When you later run the automatic partitioning, place, and route tools, they will attempt to deliver a circuit that meets performance requirements.

The software lets you specify timing requirements in a straightforward format during schematic design. You enter the register transfer requirements for clock-to-setup, the I/O transfer requirements for pad-to-setup and clock-to-output, and pad-to-pad requirements. Unachievable performance requirements are typically flagged before you've spent much time on the design.

Older methods used network criticality assignments to provide short delays on selected nets. You don't know if your criticality assignments have had the desired effect until you evaluate the resulting delays of the placed and routed device. Thus the network-criticality-assignment method often leads to an iterative design approach. The software eliminates or reduces these design iterations. The software is a free upgrade to registered users of XACT 4000. Others can upgrade for $2000. Xilinx Inc, San Jose, CA, (408) 559-7778.
—by Doug Conner

Futurebus+ products emerge at Buscon

New Futurebus+ chips and boards made their debut at the recent Buscon exhibit in Boston, MA. They joined a host of other products for the embedded-systems market, many of which are boards that have been upgraded with an 80486 or compatible processor.

The CA91C899 Logical Interface Futurebus+ Engine (LIFE) chip from Newbridge Microsystems is the first 1-chip controller that fully complies with Futurebus+ Profile B. New Futurebus+ products from Myriad Logic include a High-Performance Parallel Interface (HIPPI) board, a 512-Mbyte memory board, and a carrier board for connecting Transputer networks. Among the 486-based boards announced at Buscon were Multibus I and II boards from Intel, STD 32 boards from Ziatech, STEbus and VME boards from Arcom, and a PC/104 module from Ampro. Radstone Technology introduced a module that connects between a VME board and the VME backplane and allows live (power-on) insertion of boards.

Ampro, Sunnyvale, CA, (408) 522-2100, FAX (408) 720-1305; Arcom, Kansas City, MO, (816) 941-7025, FAX (816) 941-0343; Intel, Santa Clara, CA, (800) 438-4769; Myriad Logic, Silver Spring, MD, (301) 588-0604; Newbridge Microsystems, Kanata, ON, Canada, (800) 267-7231 or (613) 592-0714, FAX (613) 592-1320; Radstone Technology, Montvale, NJ, (800) 368-2738 or (201) 391-2700, FAX (201) 391-2899; Ziatech, San Luis Obispo, CA, (805) 541-0488.—by Gary Legg

FDDI chip set handles fiber or twisted pair

National Semiconductor has created a 2-chip set that lets designers create a compact FDDI (Fiber Distributed-Data Interface) adapter card for desktop computer systems. One chip (DP83256VF) handles the physical-layer interface, clock-recovery, and clock-distribution needs for the card. The other chip (DP83266VF) handles system interface, memory control, and the media-access-control (MAC) protocol. National is also offering software drivers to facilitate the chip set's use with network operating systems such as NetWare, LAN Manager, and the TCP/IP interface protocol.

The physical-layer chip (Player+) incorporates all of the necessary filter and timing components for data transmission and recovery on chip. It connects directly to fiber-optic transmitter and receiver modules for FDDI networks. The device, together with a twisted-pair transceiver, will also handle networks that substitute unshielded twisted-pair wire for optical fiber (SDDI).

The system interface chip (MACSI) has a system interface for direct connection to the Sbus used in Sun SPARCstations. The interface is also adaptable to EISA and Micro Channel buses. The chip incorporates 4608-byte FIFO transmit and receive buffers to reduce latency when used with slow system buses.

The 2-chip set costs $165 (100) and is available as two 160-pin PQFPs (plastic quad flatpacks) or as a 160-pin MACSI and a 100-pin Player+ device. The larger-pin-count Player+ (DV83257VF) makes available additional signals needed for scrambled-data applications. Evaluation boards (DP83200MK) for both fiber and twisted-pair networks are available for $3995. National Semiconductor, Santa Clara, CA, (408) 721-5000.

—by Richard Quinnell

Cadence offers design-for-manufacture software

Cadence Design Systems' DFA (design for assembly) and DFM (design for manufacture) software is part of the company's Allegro tool set for system design and is available as an option to the company's System Workbench. The software includes default checking rules that the user can override with custom ones.

The DFA software identifies components that do not match automatic assembly rules and verifies that the clearances between components are adequate for automatic assembly equipment, as well as for inspection and repair. The tool also identifies areas that might produce solder shorts and opens during wave soldering. The software verifies that the selected hole sizes are large enough for component insertion and small enough for proper soldering; that the specified drill sizes are appropriate for efficient shop handling; that there is sufficient annular ring for soldering; and that one-pass drilling can be done.

The DFM software automatically generates factory-fabrication data such as soldermask, solder-paste, and registration coupons. The tools allow users extensive control over the generated results through both default and user-defined design rules. Tools for the Sun-4 platform will be available in the fourth quarter of 1992 for $14,900, each with a floating license. Cadence Design Systems, San Jose, CA, (408) 943-1234.—by John Napier

Mixed A/D simulator offers speed and capacity

The Shado mixed analog-digital simulator from GenRad integrates the company's HISIM logic simulator from HILO 4 and Anacad's ELDO analog simulator. The analog simulator uses multiple algorithms to achieve fast simulation. The company claims simulation time grows linearly with analog circuit size instead of exponentially as is often the case for analog simulators. The analog simulator accepts Spice 2G6 models and has its own proprietary high-level description language, which can accommodate equations to describe nonelectrical subsystems. A lock-step algorithm synchronizes the two simulators and makes efficient use of system memory. The $30,000 software runs on Sun SPARCstations and HP 700 workstations. GenRad Inc, Concord, MA, (508) 779-6271.—by Doug Conner and John Napier

Arrays displace high-speed discrete transistors

Discrete transistors are no longer the only high-speed analog design option. You can now also use four fixed-geometry transistor arrays from Harris Semiconductor to create high-speed functions, such as 3-GHz amplifiers and mixers. The arrays solve some of the temperature-drift problems of discrete designs because they are on the same die, have matched electrical performance, and will track identically with temperature.

The arrays contain various combinations of five 8-GHz npn and 5.5-GHz pnp transistors in SOICs. The HFA3046, '3127, '3096, and '3128 contain transistors in the following combinations, respectively: 5 npns, with two configured as a differential pair; 5 npns, 3 npns, and 2 pnps; and 5 pnps. Prices range from $3.10 to $3.80 (100). Harris Semiconductor, Melbourne, FL, (800) 442-7747, ext 7041.

—by Anne Watson Swager

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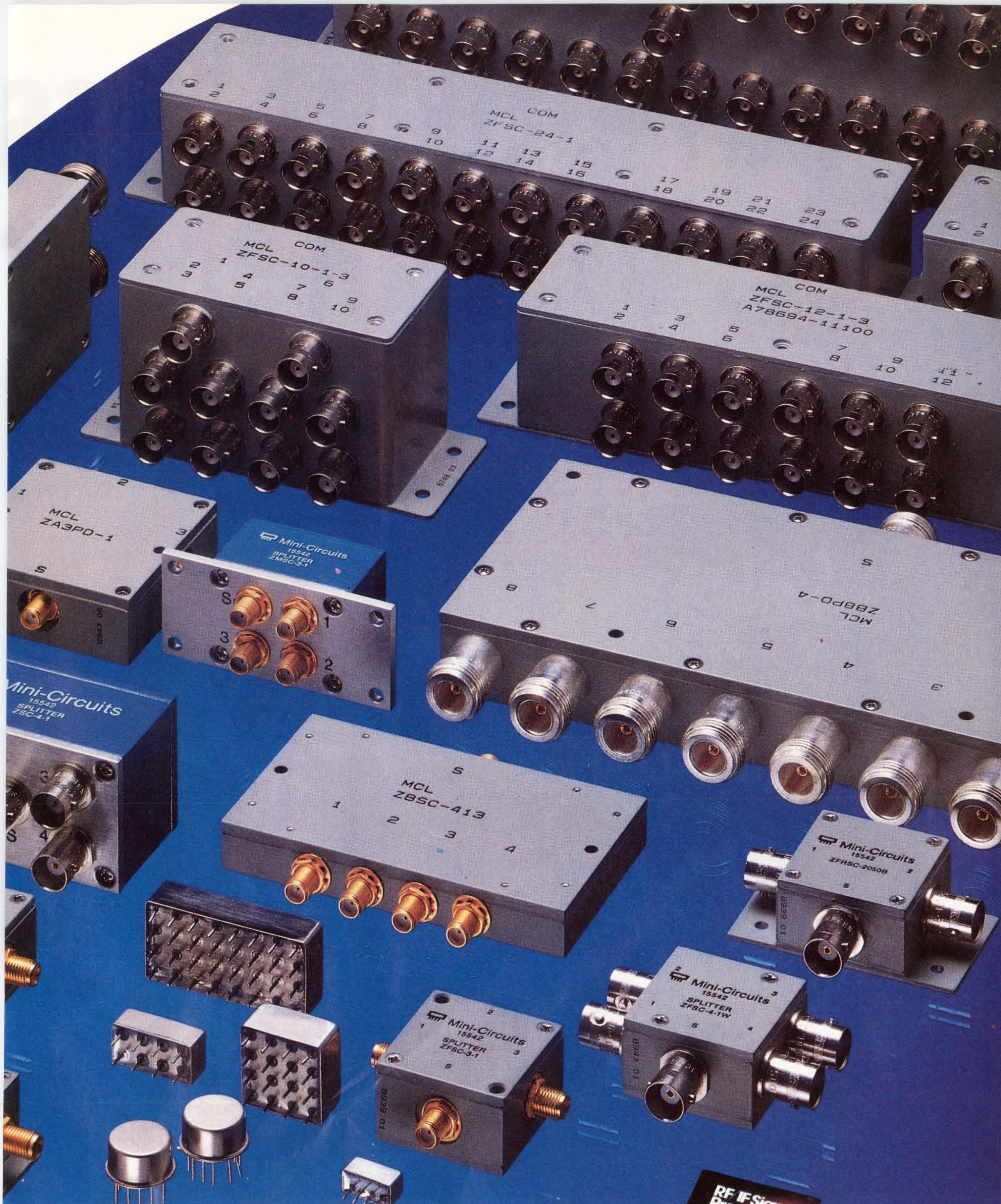
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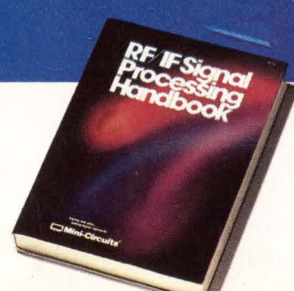
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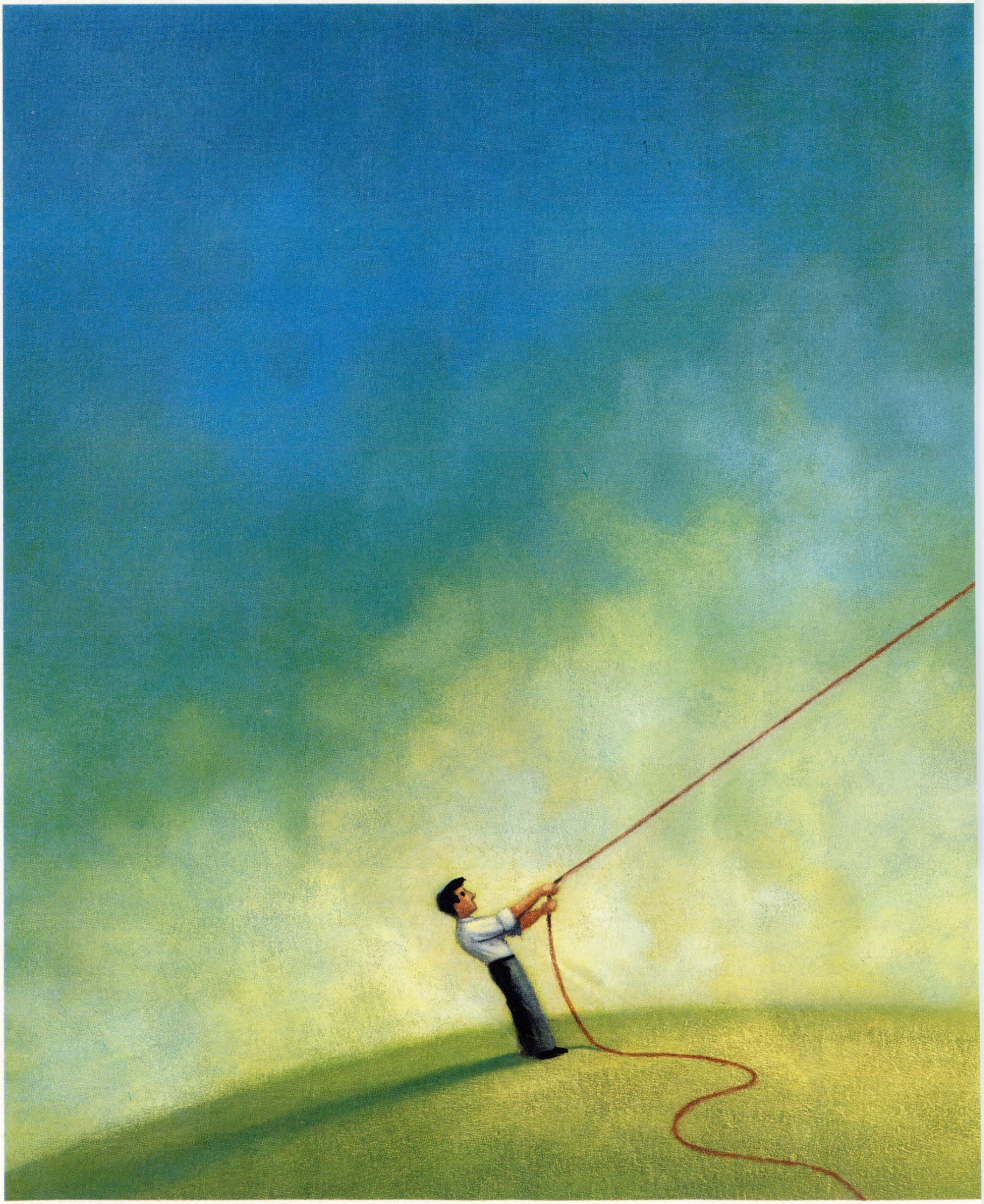

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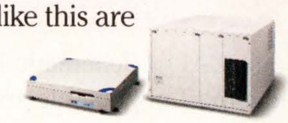

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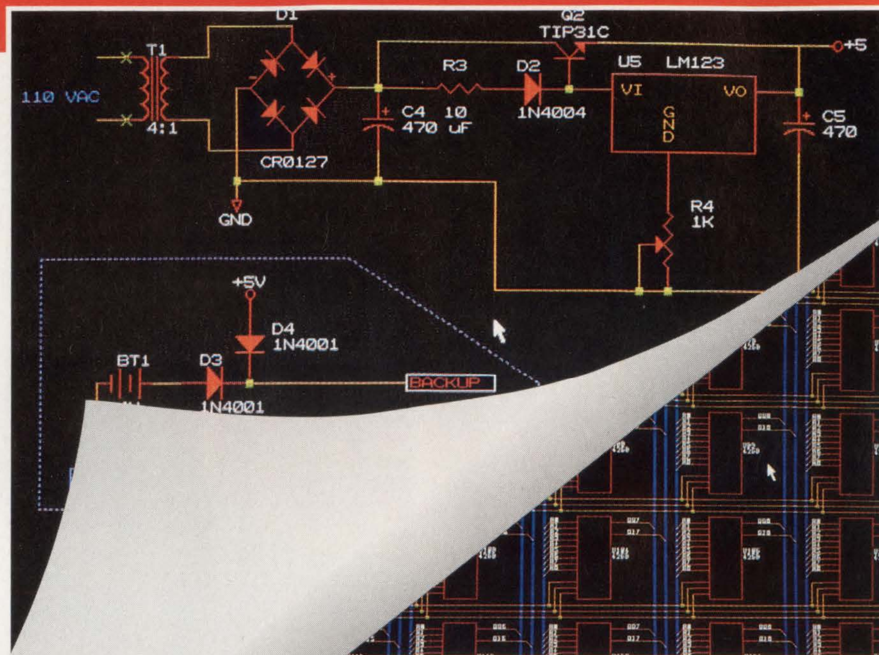

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CIRCLE NO. 21

Taking responsibility for education

The editorial by Joan Morrow Lynch entitled "Everyone wins" (EDN, June 4, 1992) is gratifying because it gives examples of interest in science and engineering. I am a volunteer liaison between Hewlett-Packard (HP) and our local school district's high schools, specializing in math and science education.

The editorial makes an interesting point: Lack of a demand from the students will defeat every program, every time. I see this every time I'm called upon to advise on the acquisition of another computer for the classroom. Schools think they need a Macintosh with a MIDI interface and a CD-ROM to teach the students. In fact, what schools need are students who believe their own future success in life depends on the education they receive from the school and in which they actively participate.

In a microprocessor-programming class I taught to some high-school students as part of their applied-technology course, I could give homework and exams. The students complained that I shouldn't be giving them homework. One student was on the swimming team and had to practice three hours a day; my homework was cutting into his practice. I pointed out that homework is practice for the mind. Why, I asked him, is it okay to practice for a sport, but not for an intellectual activity.

Until we raise our expectations of what constitutes a good preparatory education, we will be in this crisis. It's not the facts that you learn in school that are important, it's the process of learning and training your mind to think.

I'm currently involved in a project with Liberty High School. Scat Hovercraft in Florida has donated one of their Hovercraft as a vehicle for applying physical principles to solving real-world problems. We are trying to assist Scat in lowering the noise generated by their products. The students are learning about how engineering and team activities actually occur. HP and other companies have also donated equipment and provided mentors. We've completed one year so far, and I'm impressed with this year's results.

Looking back on this project, however, I wonder why all of this is necessary. It's expensive and very time-consuming. The answer is simple. If we were to teach traditional physics in a traditional classroom environment, we wouldn't have any students to teach. The Project Engineering class is "sexy," and it captures their imagination. This isn't bad, and it's similar to the thrust of Lynch's editorial, but why is it necessary?

Until the students and their parents take responsibility for their own education, programs such as these will be necessary, and they will be insufficient. For every 50 students who participate, 250 will breeze through at the lowest common denominator. They will feel good about themselves, but they will be uneducated.

Arnold S Berger, PhD
R&D Project Manager
Hewlett-Packard Co
Colorado Springs, CO

Reciprocal apologies are in order

Please accept my apologies for writing unclearly and for using unexplained acronyms. My letter to Signals & Noise in the June 18, 1992, issue (pg 31) was about programmable logic devices (PLDs), not PIDs.

Also, Little Rock (unlike our governor, Bill Clinton) is in Arkansas—abbreviated AR. AK [which also appeared in the June 18, 1992, issue] stands for Alaska.

Jim Honea
Electronic Design Engineer
Aerospace Controls Corp
Little Rock, AR

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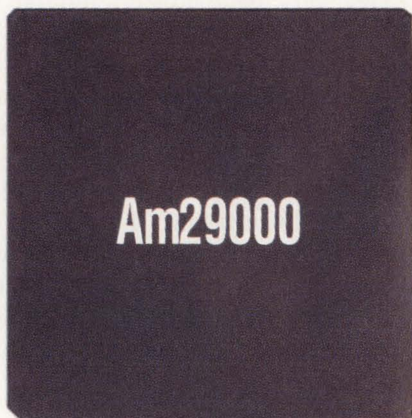

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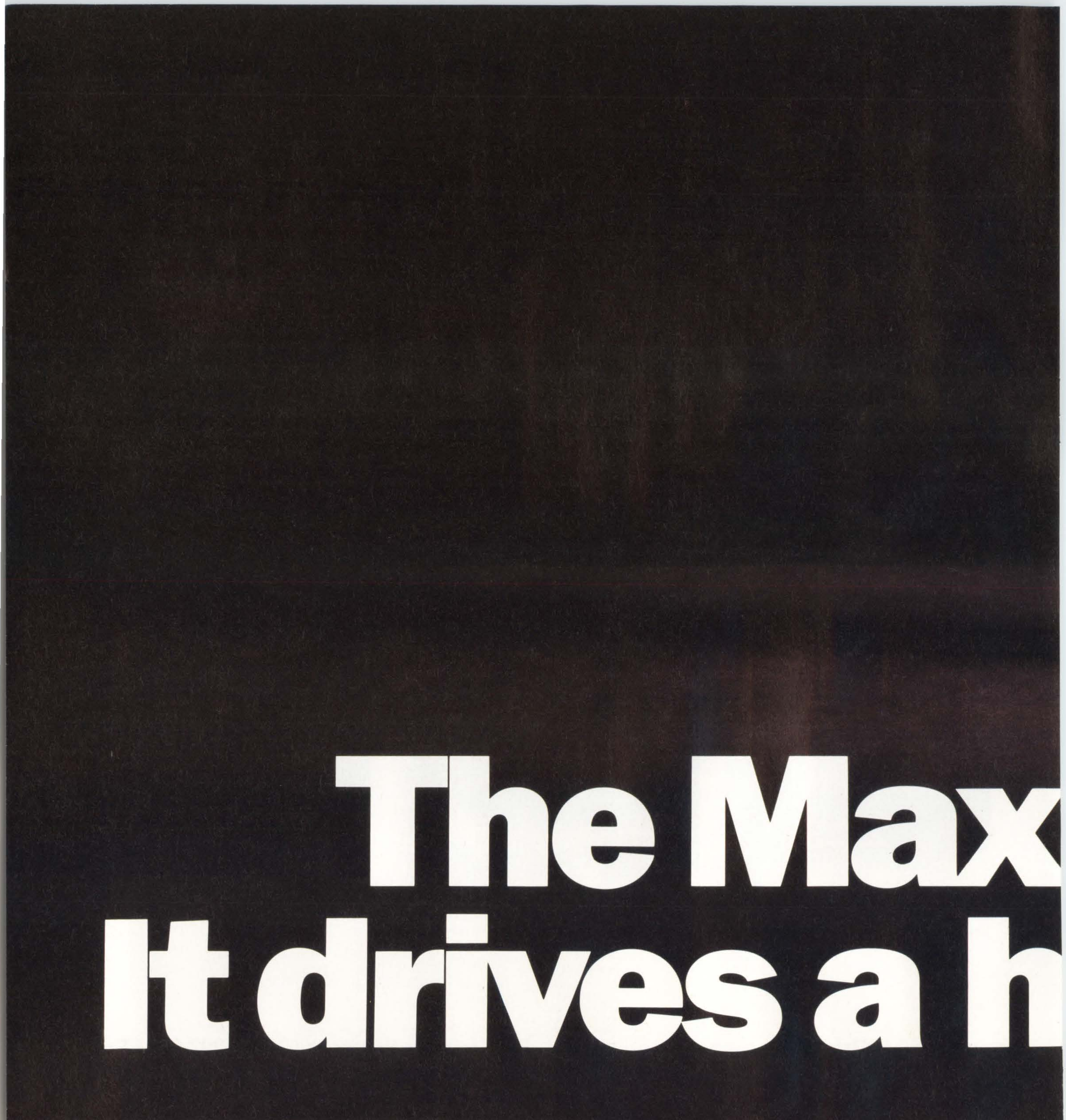

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CIRCLE NO. 24

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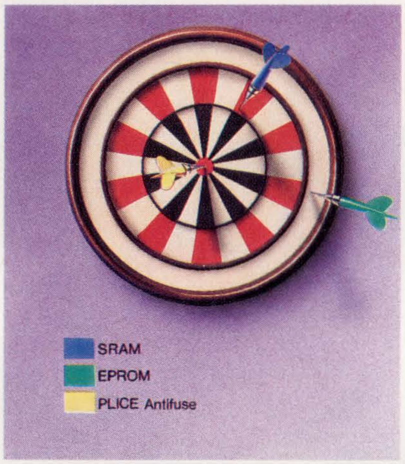

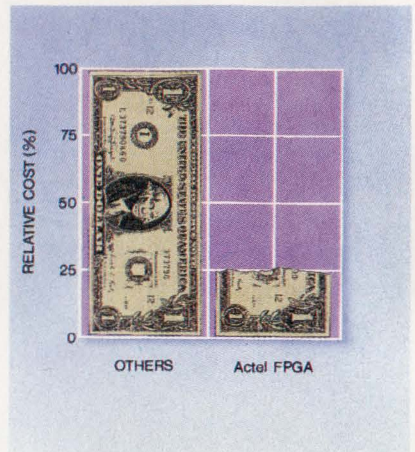

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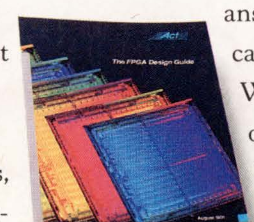

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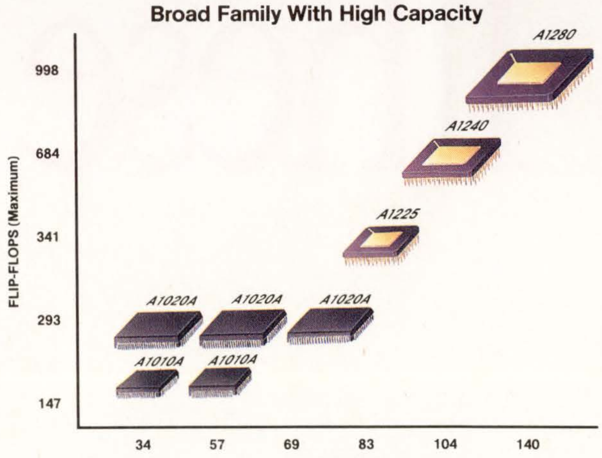

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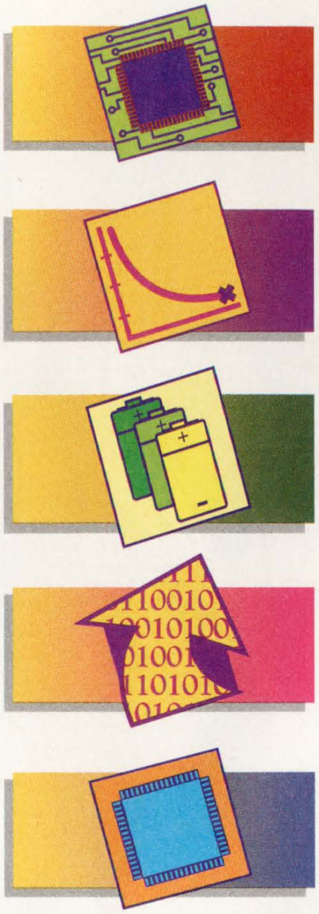

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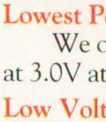

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EPOCH

CIRCLE NO. 27

Washington: off frequency

Today, more and more communication companies and groups want to claim portions of the radio-frequency (RF) spectrum. Unfortunately, the RF spectrum is already crowded, and its bounds are limited. We can't create extra frequencies for new applications. However, we can carefully apportion the frequencies to meet the needs of new technologies. But that's not always done. The US Senate has decided to join the battle for frequencies by preventing the US Federal Communications Commission (FCC) from reallocating a small set of frequencies. That's a bad approach to a complex problem.

A few months ago, the FCC proposed moving users in the 1.85- to 2.2-GHz band to other frequencies. The newly available spectrum would be opened to personal communication services and new services now only in experimental stages. The present users of the band are mainly railroads and utility companies that communicate between fixed points. With its usual wisdom, the Senate blocked the FCC from reallocating the frequencies around 2 GHz to new services. The ban is an amendment to a bill that several electronics-industry groups seek to kill. Likewise, President Bush has said that he will veto any bill that blocks frequency changes.

The National Telecommunications and Information Administration (NTIA) also looked into the problems of relocating the 1.85- to 2.2-GHz-band users to frequencies between 1.7 and 1.85 GHz. Government communications now use that band. However, by carefully planning the frequencies of new stations, the paths of communication links—and considering other factors, all but 2% of the existing stations—could coexist with present operations. Making radio-communication facilities change frequencies can be expensive, but it can be done. No one should assume they have proprietary rights to parts of the RF spectrum. I've stated several times that frequencies should be put to the highest and best use, and that's still my opinion.

Nicholas Negroponte, head of the MIT Media Laboratory, thinks that if both points in a communication path are fixed, communications should go by wire or fiber optics. On the other hand, if either of the points moves, it should communicate by wireless. We agree. Communicators with fixed bases should plan to relinquish valuable spectrum space to mobile users. FCC Commissioner Alfred Sikes estimates that such a blocking of the 1.85- to 2.2-GHz band could postpone new communication services by 15 years. If Congress succeeds in blocking the reallocation of frequencies to innovative forms of communication, consumers—and the electronics industry—will suffer. Let's get moving.

Jon Titus
Editor

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1990 Certificate, Best Series
1987, 1981 (2), 1978 (2),
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American Society of
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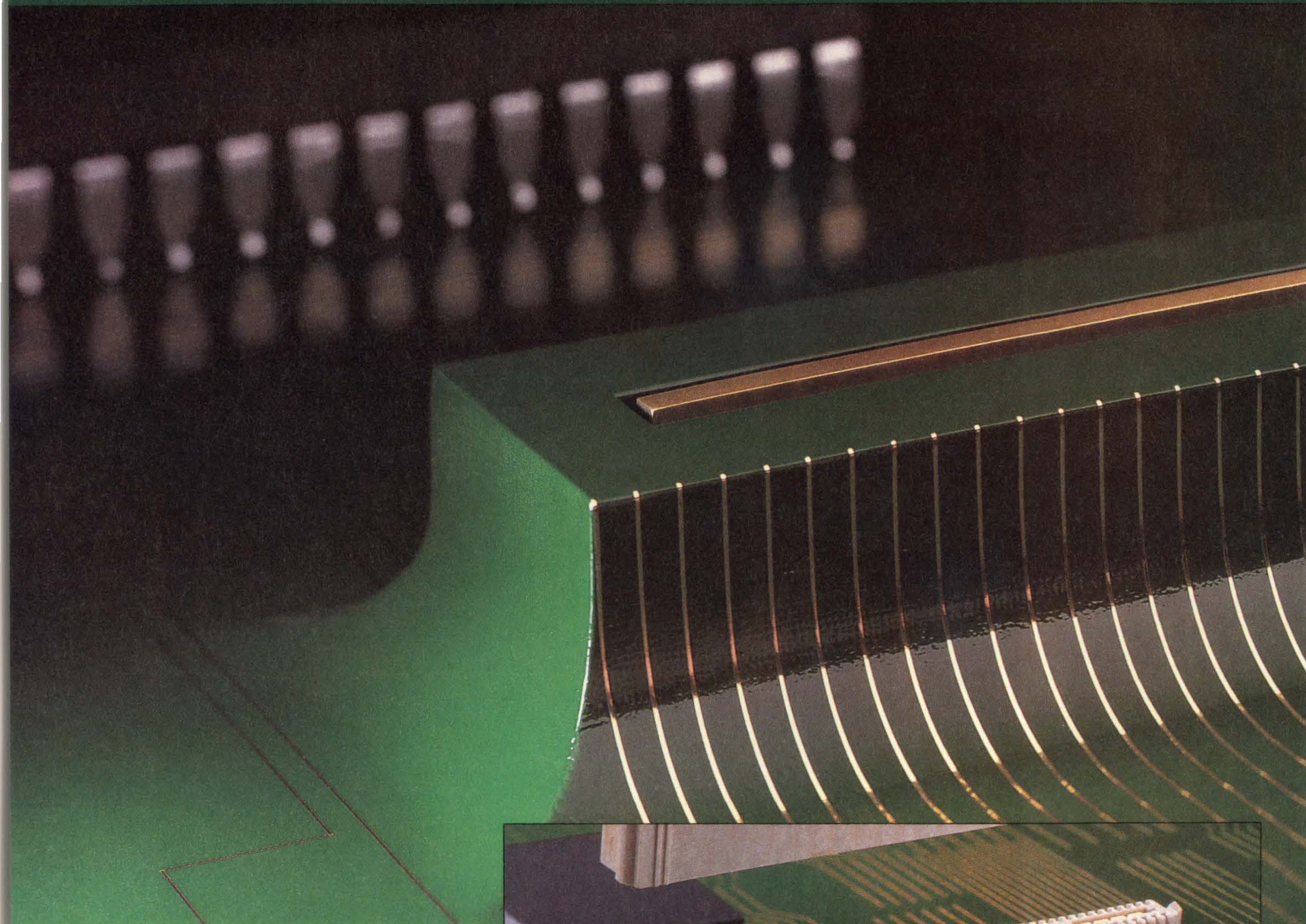

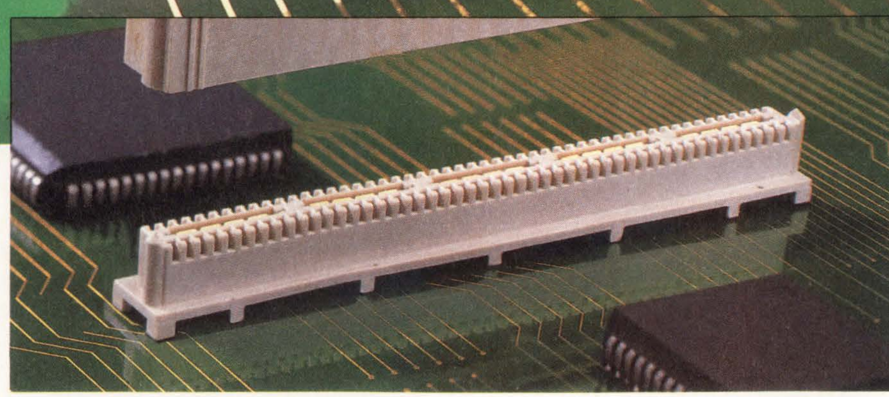

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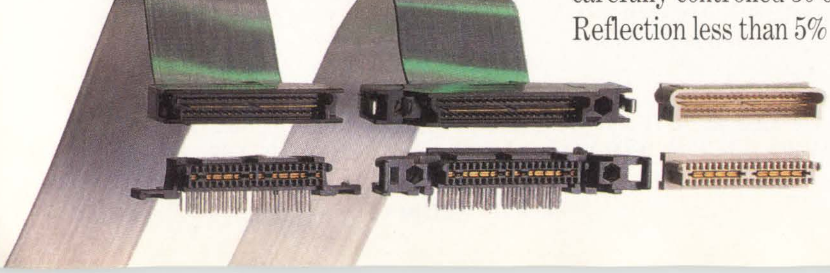

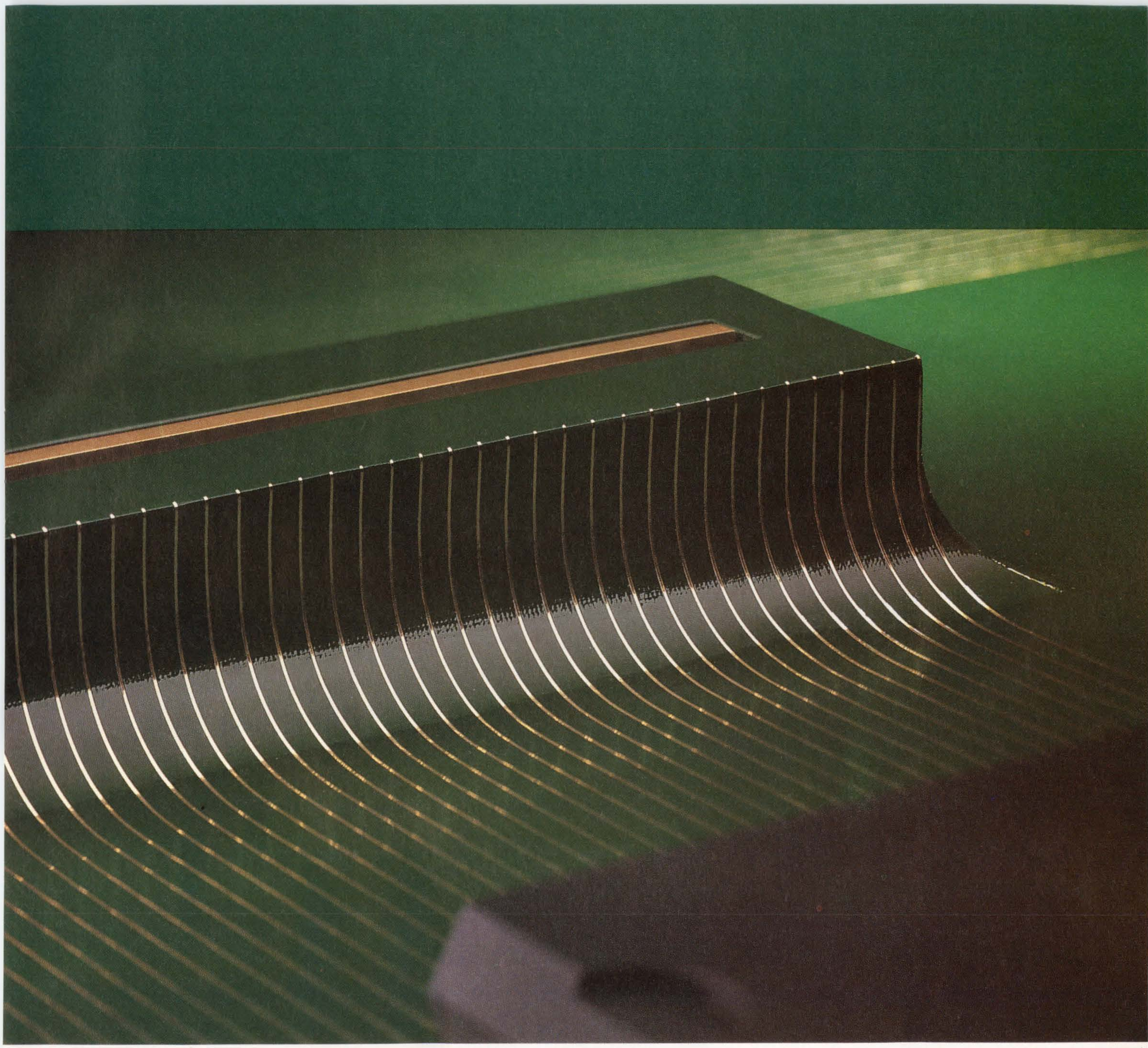

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CIRCLE NO. 29

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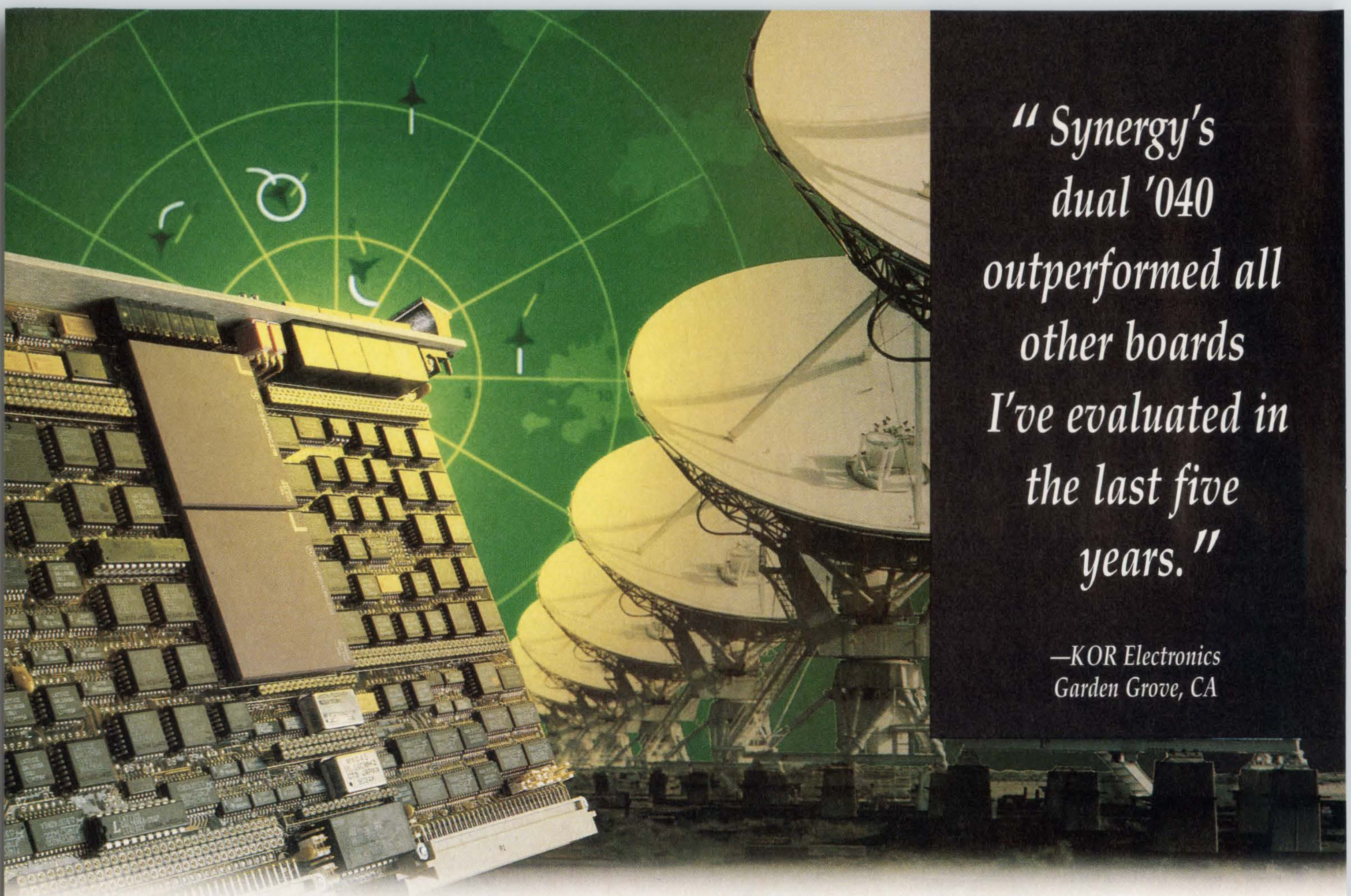

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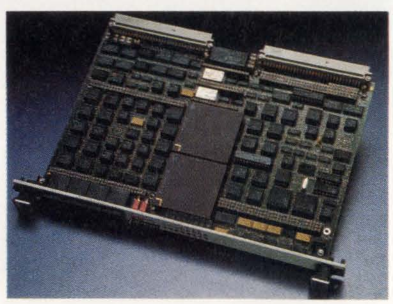

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CIRCLE NO. 31

EDN hands-on project: Pads software performs complex designs for less

DOUG CONNER, Technical Editor

Although Pads high-performance design software is priced near the top for PC systems, it's priced near the bottom when running on a workstation. The software can accommodate complex pc-board design without the limitations found in low-cost software.

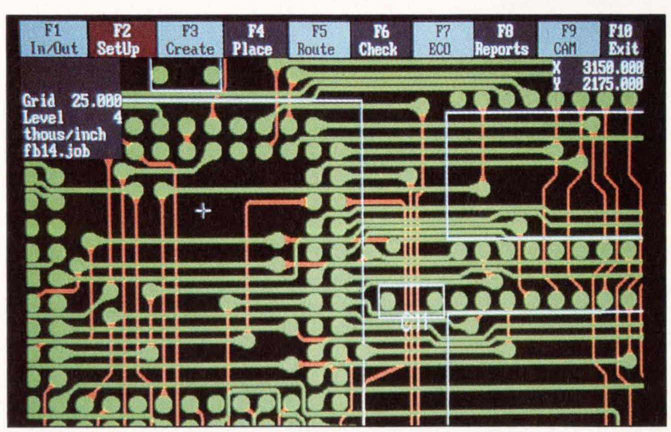
When considering schematic entry and pc-board layout tools for PCs, you can find a lot of software offering various price-performance tradeoffs. Pads Software offers several packages ranging from low-cost to high-performance. I tried the company's high-performance software, Pads Logic for schematic entry and Pads 2000 for pc-board design, to see how they perform. The software runs on DOS-based PCs and Unix workstations.

The capability of these software tools becomes apparent when you look at the tutorials. The 145-pg tutorial on schematic capture and 182-pg tutorial on pc-board layout are thorough. These tutorials don't just take you through the basics. They walk you through every advanced feature. I spent the better part of two weeks going through most of the tutorials. It's a lot of time, but when you're done, you'll know how to use the software on real work, not just how to get started. The schematic-entry tutorials take you through the hierarchical design. The pc-board design tutorials cover using the software for simple 2-layer designs and for multilayer through-hole and surface-mount designs. Designing a small, 4-layer pc-board after completing the tutorials was easy.

In just a few pages I can't go through the software in detail, but I'll try to give you a feeling for what the software can do and cover some of the features that I feel are worthy of note.

The ten choices in the basic menu structure appear across the top of the screen and match the ten function keys. You can also select the functions with a pointing device such as a mouse. I didn't make a specific count to see how many menu levels there are. The count differs with the path you are following, but my impression is about five. Initially I was not impressed with the menus; I felt a little lost trying to navigate through them. As I worked through the tutorials, the lost feeling left and I felt the menu system was Spartan but efficient.

The menu groups are well thought out. I seldom found myself wasting a lot of keystrokes on menu changes. For example, in schematic capture one menu covers all the component and connection additions. When you add a component, a new menu automatically pops up, letting you rotate, mirror, call up an alternate symbol, or complete the



The menu structure is similar for both the schematic entry and pc-board layout software. Although it's perhaps a little slow to learn at first, it's very efficient once you become accustomed to it.

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 CIRCLE NO. 32

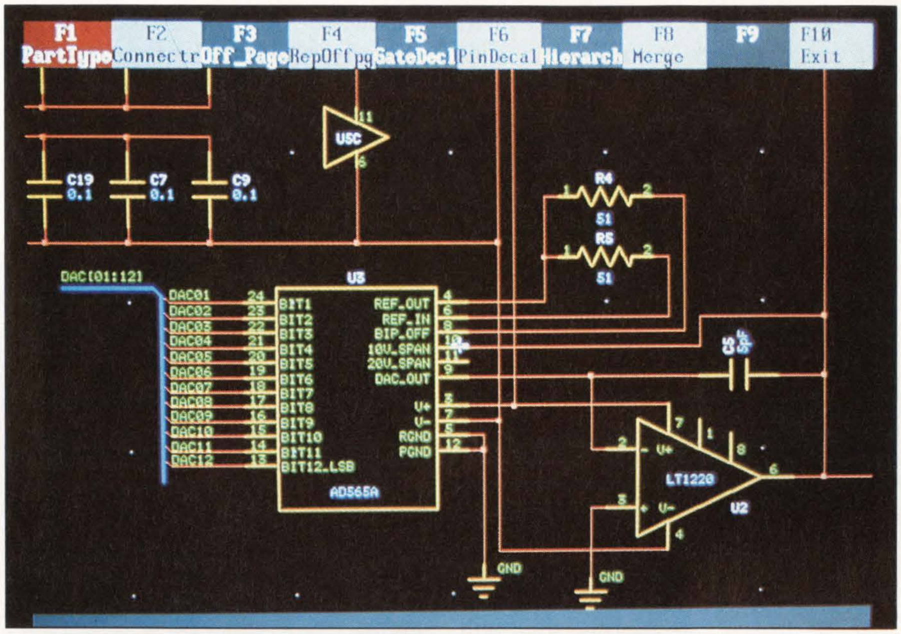
SCHEMATIC ENTRY AND PC-BOARD LAYOUT

placement. Similarly, in pc-board design work, one menu covers most of the functions you need when placing parts, while another menu covers routing.

In addition to the menus, there are some modeless commands for operations such as changing the grid. You type g25 and a carriage return to change to a 25-mil grid, regardless of where you are in the menu system. In schematic entry you can change sheets instantly using a modeless command (sh3 for sheet 3). A modeless search command lets you jump instantly to a specified grid point or a part and pin number. Modeless commands let you set and change the layer pair for pc-board routing, the current layer, and some other functions.

You can create keyboard macros for combining groups of commands to speed up any keyboard-intensive operations that you repeat often. The software also includes a timed automatic backup feature that helps you avoid losing work due to an unexpected power outage.

Schematic-entry software has been around for quite a few years now and many features are common across the industry. I'll just mention a few of the features to give a feeling for the level of detail in the software.



The schematic-capture software is straightforward and easy to use. The library editor made it simple to create parts that aren't in the standard library.

Group functions

One of the immediately apparent features of schematic entry that I appreciated was the design-oriented database. The entire design is in RAM at once, so sheet changes are fast.

Group functions for moves, copies, and deletes are an important productivity aid, especially if they are well thought out to cover most of the problems associated with this powerful command. The group function in Pads Logic lets you select the part of a design with a rectangular window and then highlights what has been selected for the move. If there are lines that go outside the window, you can select whether to maintain the connections during the move or disconnect them. You can also select whether to add or delete items from the group, a useful feature when you've captured parts you didn't want in the group or missed a few. The group menu also lets you select the origin point for the group move or copy. When you want to accurately place a group for a move or a copy, you set the origin on a convenient reference point and then the cursor attaches to that point during the move.

The schematic-entry software also includes true busing. The bus lines are named and automatically increment through the range of signals you specify. The auto incrementing of the names, such as bus DATA[00:31], provides the signal names, DATA00 through DATA31, without you typing each one in.

Creating parts

Libraries for schematic entry are the ordinary 7400 series, some microprocessors and peripheral ICs, a few analog ICs, and discrete components. As always, you'll have to add parts to the library to accomplish most designs. The tutorial has you add several different parts to the library for experience, giving you an easy template to follow for creating other parts.

In my sample design, I had to add a few parts. The 84-pin field-programmable gate array (FPGA) was quick to add because I could use the semiautomatic part generator. You enter the number of signals on the left and right sides of the symbol, and it automatically adds them to a properly sized rectangular symbol. You specify pin names, pin numbers, pin properties, and complete a short table for the database. The database for the part lets you add ten lines of your own information, which might include such things as a part description, the manufacturer, a price, or whatever you'd find useful.

If you need to create a new symbol, you just use the 2-D drawing menu. I created an op-amp symbol, although I could have copied it from one of the existing parts.

SCHEMATIC ENTRY AND PC-BOARD LAYOUT

The software provides several different reports including the ordinary netlist and a bill of materials. You can use the options to output the netlist in about a dozen different formats to make it suitable for use with simulators and other software tools.

Transferring data between the schematic-entry software and the pc-board layout software is an important step. If the transfer is automatic, then it will save time and virtually eliminate inconsistencies that result in errors between the schematic and the pc-board layout. Although the usual direction at the start of a design is from schematic to pc-board layout, after design of the pc board has begun, you will need to back annotate the part identifiers and sometimes swap pins or gates from pc-board layout to schematic.

In addition, depending on the flexibility of the particular design project, the person laying out the pc board may be able to change connector pin numbers on cables, data or address lines on RAM, and make other changes that may simplify the layout. These changes must all be back annotated to the schematic.

Changes that require forward annotation from schematic to pc-board layout are common too. Design engineers sometimes find mistakes (usually known as improvements) after pc-board layout has begun. After a design is finished, correcting errors or adding desirable improvements requires the dreaded engineering change order, better known as an ECO.

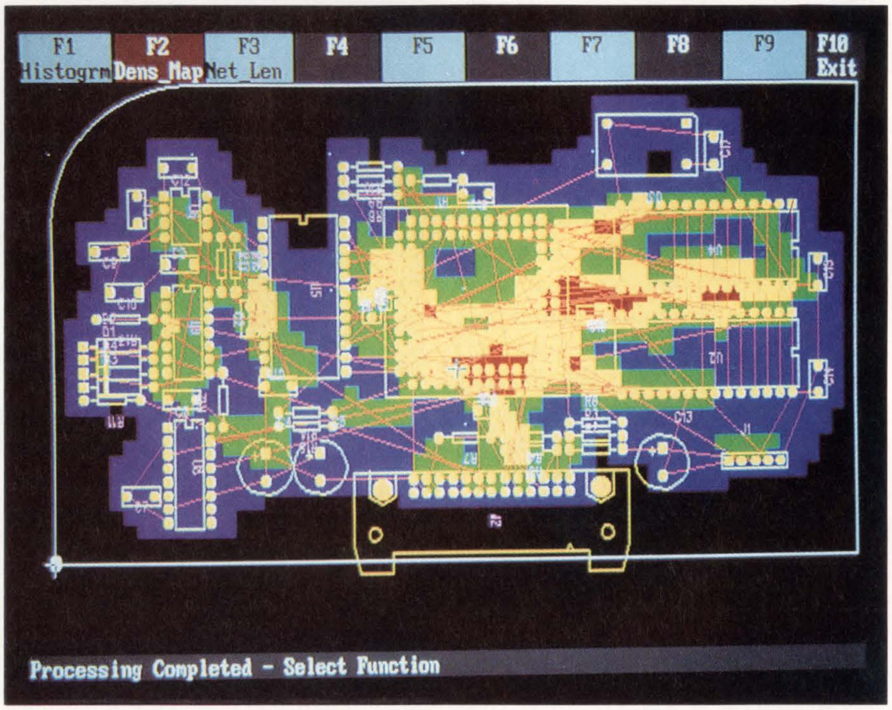
In the process of evaluating the software, I had an opportunity to try forward and back annotations and ECO changes several times. The process is easy and gives you confidence that the automatic transfer of data is keeping an accurate match between schematic and pc-board design data.

Here is how the forward and backward transfer of data works. Initially you transfer the schematic for pc-board layout with a netlist transfer. As part of the netlist transfer, the pc-board layout software accepts pc-board layout decals for the parts used. If the package-type decal exists in the library (or you've added it to the library), then the design will be immediately ready for placement when you start pc-board layout.

Once you've transferred your initial design, then the software tools handle subsequent schematic changes as additions or deletions of parts and connections. If you alter the schematic, you specify the new and old schematic using the ECO menu, and the software automatically creates a file containing the additions and deletions. You read the file into the pc-board layout software to make the changes.

If you've made changes to the layout that need to be back annotated to the schematic, the process works in reverse. You enter an ECO mode and make the needed changes to the layout, and Pads 2000 creates an ECO file. You enter the schematic ECO mode and read in the file to update the schematic.

The end result is that Pads Logic makes it relatively quick and painless to keep the pc-board layout and schematic matched throughout the design process.



A density-map placement-evaluation aid shows the relative concentration of networks. The yellows and reds indicate where you will have the most congestions.

When you first transfer the netlist to the pc-board design, it dumps all the part decals at the board's origin. You can place the part decals using manual placement or autoplacement.

The autoplacement software requires a placement matrix. You set up the placement matrix by specifying the number of rows and columns and the spacing between the rows and columns. The software creates the matrix and then you can place it visually on the pc-board outline. You need at least enough matrix vertices for all the components you wish to place. Delete specific matrix points where you don't want to

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CIRCLE NO. 33

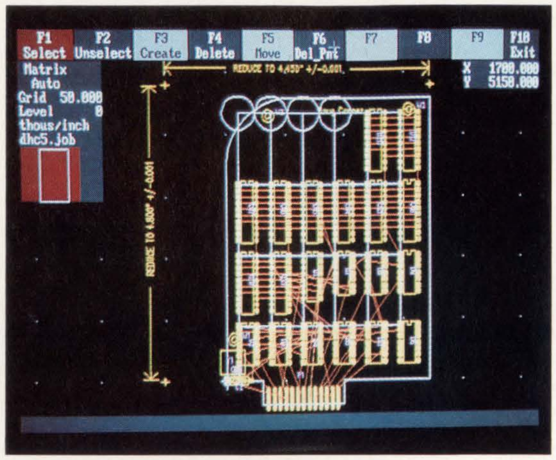
SCHEMATIC ENTRY AND PC-BOARD LAYOUT

place parts. You can preplace any special ICs and glue them down. After that's done, you can run autoplace and the software attempts to minimize the connection length of all networks as it places the parts.

You can exercise a certain amount of control over autoplacement by manually placing some parts. For example, by placing a memory IC in one location, you can force other memories to be placed close to it. The tutorial discusses how to help autoplacement come up with the placement you want, especially on those nonideal designs that are frequent in the real world.

I spent some time working with autoplacement both in the tutorial and in designing another pc board, and I'm convinced this is a useful tool. It's not a gimmick that just works on some ideal TTL design. The software automates what it can and gives you the flexibility to correct or preplace what it can't.

After the initial placement you can make modifications manually or automatically to move parts, or swap parts and pins. You can maintain the original placement matrix or move parts off the matrix. Once you have the ICs in place, you can change the matrix or make a new one for placing decoupling capacitors and any other components suitable for autoplacement.



Here is one of the tutorial boards just after autoplacement of the ICs. The white matrix that intersects pin 1 on the ICs is the placement matrix I set up. The circles in the upper left matrix are points that I've deleted. I preplaced one memory IC in the upper right corner, which pulled the other memory ICs to the top of the board during autoplacement. Unplaced components are stacked on top of each other in the lower left corner.

Evaluating your parts placement is aided by several different tools. A ratsnest display lets you see the networks and connections to them. An interesting feature of the ratsnest display is that the connections dynamically change to show the shortest connection between all pins in a network. As you move parts around during placement, you'll see the order of networks change to minimize the length of the new connections.

A quantitative aid for placement is the total connection length, which measures the total orthogonal-connections length of all the networks, commonly referred to as the Manhattan length. Minimizing the connection length generally leads to a good placement, provided the placement leaves enough space between components to route the signals.

Two qualitative placement aides help you evaluate the relative difficulty of routing the design. One is a histogram that shows the density of signals in the routing channels. The other is a color-coded density map that shows the relative density of signals over the pc board.

Occasionally special component-placement requirements dictate angular placement of parts, especially radial placements around a central point or simply fitting components onto an irregularly shaped pc

Software specifications

Pads Logic, $750. 2 Mbytes of extended memory, 4 Mbytes preferred.

Pads 2000 on DOS Systems, $12,500, including Pads-PowerRouter. $7000 without autorouter. On Sun SPARC and HP9000/700 workstations, $20,000, including Pads-PowerRouter.

The suggested memory for running Pads 2000 on DOS systems is 6 Mbytes of RAM for a 500-IC design, and as much as 16 Mbytes for designs with more than 2000 ICs.

The 32-bit database offers 1-μm resolution or 0.00001 in. and a maximum-dimension working area of 143 cm or 56.3 in. The database uses much finer resolution but limits the number to provide exact translation between metric and English units.

The software provides 30 layers for routing and documentation.

Both the schematic-entry and pc-board-layout software provide the outputs for dot-matrix printers, laser printers, plotters, and photoplotters.

I tested the software on a 33-MHz 486 system with 12 Mbytes of RAM.

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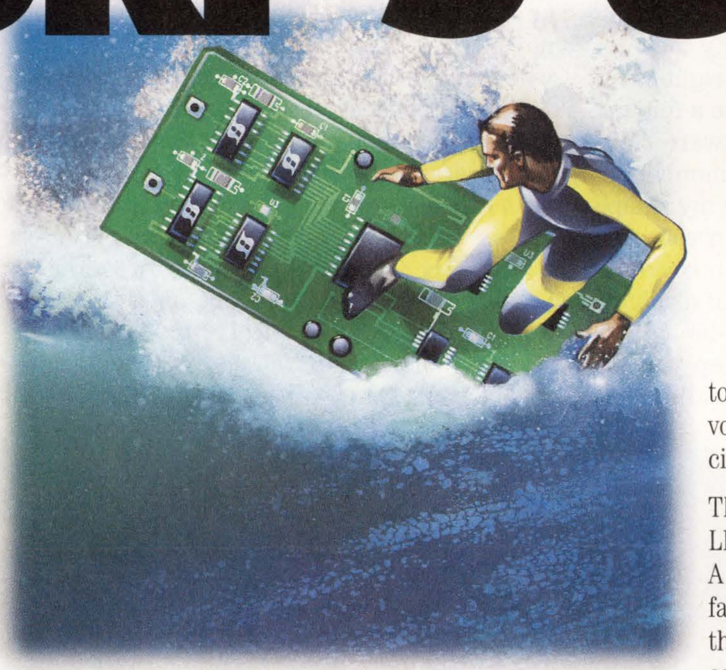

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board. The layout software lets you rotate and place parts to 0.1° resolution.

You can place components automatically or manually on both sides of the board, a necessity for some surface-mount designs.

One last operation when placing parts is renumbering them on the pc-board to follow some logical sequence. The pc-board layout software can accomplish the renumbering operation automatically and provide the file for back annotating the schematic. You specify the numbering sequence such as right to left and top to bottom, create a fine matrix grid, and the software automatically does the renumbering. The software worked on my sample board, which did not have components neatly arranged in rows and columns—another step of drudgery removed from the pc-board designer's life. The one step you will need to perform manually is to move the part identifiers where you want them on the silkscreen.

Before you route a complex board, you need to setup the pad stacks. Much of the capability required for complex pc-board design centers around the pad-stack feature. Pad stacks essentially let you create different pads at the same x,y location on different layers of a multilayer design. Although many low-cost software packages allow you some flexibility in multilayer and surface-mount designs, you need to recognize the limitations when certain features are missing.

Without pad stacks, you usually have the same pad size and shape on all circuit layers. Furthermore, without pad stacks, pads and vias appear on every layer of a circuit board (**Fig 1**). The importance of these limitations is apparent on a 6-layer design. A typical 6-layer through-hole design will have two inner layers for power and ground. The other two inner layers are for routing signals. Although pads are needed around the through holes on the two outer routing layers for soldering components, pads are only necessary on inner layers when a signal connects to the hole, whether for a component pin or a via. When pads are placed on every layer even though they are not needed, the space for routes is unnecessarily restricted.

You don't need to be designing a 6-layer board to benefit from pad stacks. Even a 2-layer board may benefit if the design uses surface-mount components. Because surface-mount components don't require a through-hole, you can use the location of a pad on one side for a track or independent pad on the other side.

Complex pc-board designs may also use blind and buried vias. **Fig 1** shows these two types of vias. The motivation for using blind

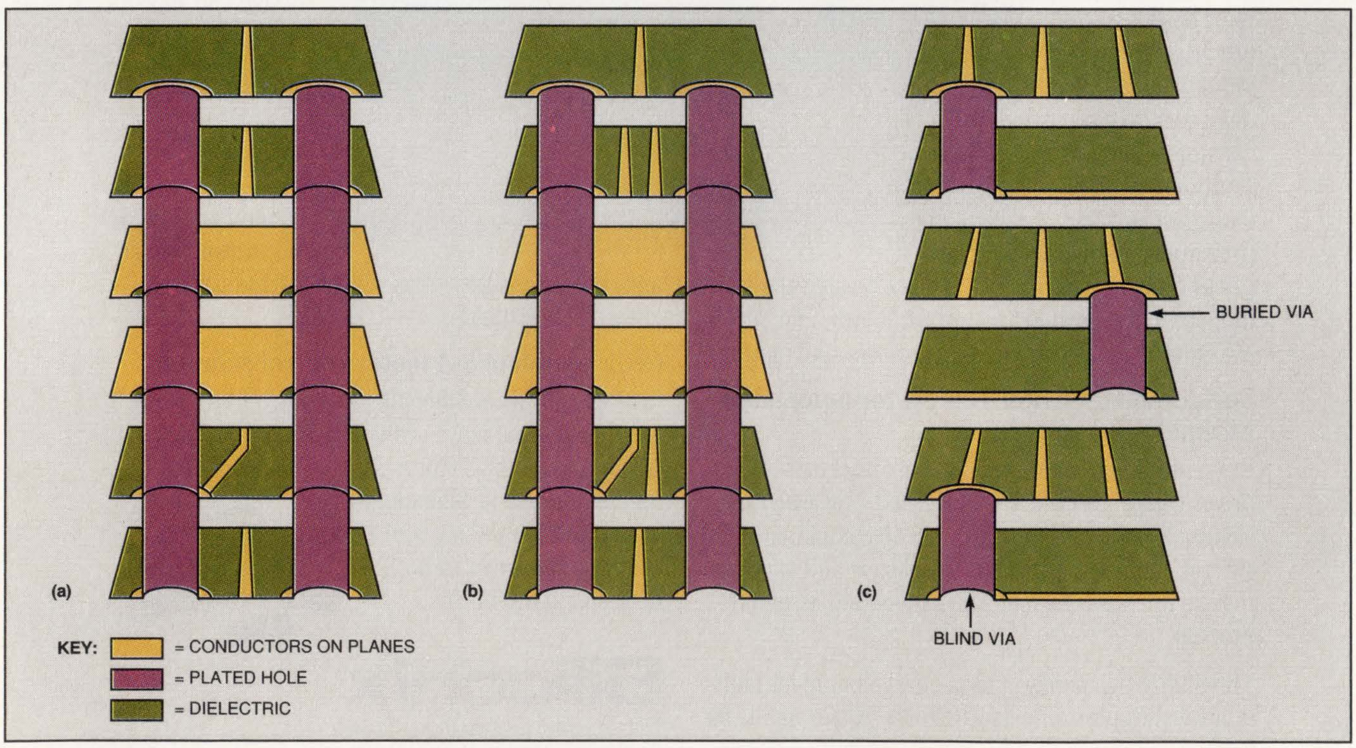

Fig 1—Without using pad stacks, through-hole pads and vias take up space on every board layer whether the pad is necessary or not (a). Pad stacks let you eliminate pads on inner layers when they are not necessary (b). Using the same manufacturing technology, you should be able to route more signals between IC pins by eliminating unnecessary pads on inner layers. Pad stacks also let you create blind and buried vias (c), which requires more manufacturing steps, but is useful when routing very dense pc-boards.

and buried vias is the same—to preserve space on other layers for routing.

You usually don't need the capability to create pad stacks for 2- or 4-layer through-hole design. You may be able to perform some surface-mount designs without pad stacks. If you need to do 6-layer design or multilayer surface-mount boards, especially with components on both sides, you need flexible pad stacks. If you don't have them, you're unnecessarily limiting your design.

However, you need to remember that designing with pad stacks is more complex. Without pad stacks, pc-board design is essentially a 2-D design process. All pads and vias appear on every layer. With pad stacks, the design process becomes 3-D. Independent pads, vias, and tracks can exist at the same x,y location.

Another concern with pad stacks is the difficulty of modifying a manufactured pc board. Cuts and jumpers on pc boards designed with internal routing layers are painful enough when the vias go all the way through the board. Signals routed completely on internal layers with buried vias are difficult to alter. If your design process usually calls for a lot of changes to the pc board after it's built, you'd better tighten up your design before advancing to internal routing layers with buried vias.

If pad stacks sound like a lot of complexity you don't need, you can essentially ignore them for 2- or 4-layer designs with power and ground planes. If and when you need to use pad stacks, the tutorial material will bring you up to speed quickly on how to set them up and use them.

Manual routing tools

I found the manual routing tools easy to use from the start. Routes were easy to modify too. When routing boards, I generally spend a significant amount of time modifying tracks I've already put down, so I appreciate flexibility to modify the tracks easily; moving segments, corners, deleting corners, changing layers, and such. With Pads 2000, I often found that the ability of the software to add an improved redundant track to an existing one was an easy way to modify the tracks. When you complete the redundant track, the software can automatically remove the part of the old track that is no longer needed.

Pads 2000 also lets you make T routes. You aren't required to route from pin to pin. If a network contains three or more pins, you can route from anywhere along one of the tracks.

When you are routing a track and you come to a roadblock or something you wish to modify before you go on, you can select an end track with no via command. The track stops at the current cursor location and the network connection line proceeds from that point to the destination. You can fix the roadblock and continue routing. You might create several partial tracks while you work on signals in a congested area. The network connections assure you won't forget them and no work is lost, as might be the case if the software didn't let you keep the partial route.

The software lets you route using miters with 45° chamfers or with rounded corners. You can select the size of the chamfer or radius of the curve as a ratio of the track width. It's easy to add or change miters on existing tracks.

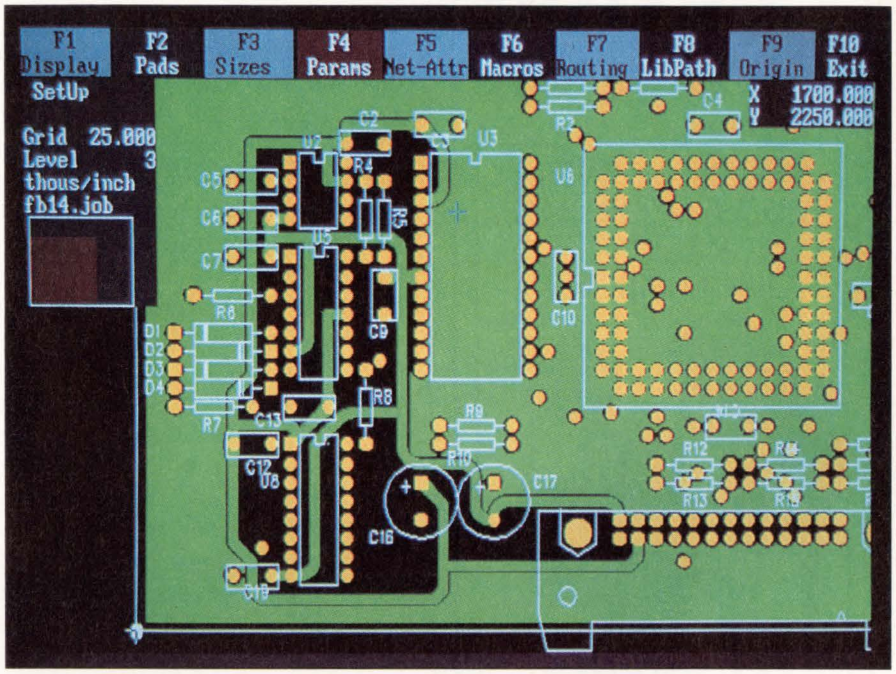

Fig 2—Embedded in the +5V plane are the +12V and −12V power distribution networks. The voltage plane was automatically generated around the +12V and −12V networks using a copper pour without any manual modifications. The tracks also show some experiments with different mitering options.

Pouring on the copper

The software has a copper-pour feature that I think is extremely useful. A good way to see what you can do with copper pour is to look at **Fig 2**, which I created using the capability. What the figure shows is a +5V plane with embedded +12V and −12V power distribution. In this case I used 50-mil traces, but the embedded tracks could be any size. To design this layer, I connected the +12V and −12V signals, set up the copper-pour area, and then performed a copper pour with parameters set to the desired, clearance, radius, allowable copper island size, and a few other parameters. The copper pour was specified to connect with the +5V network. The copper flood to create the plane and clearance was totally automatic. I made no manual edits or modifications to what you see.

The copper-pour feature is invaluable for squeezing a few difficult-to-route signals onto a plane. You must be careful not to break up the plane excessively. I avoid breaking up ground planes except to isolate analog and digital ground planes for sensitive circuits. You can use the copper-pour feature for grounding and shielding and other applications where an isolated copper plane is needed in an area containing signals.

Checking for space violations

During ordinary manual routing, the software does not warn or prevent you from making spacing errors. Any errors are clearly marked when you run a space check. Unless you are confident you know what you are doing, it's a good idea to run them occasionally before you lay down too many tracks with a chronic spacing error.

If you want to have on-line checking, you can use one of the manual modes, provided you are using the complete Pads 2000 package with autorouter. The autorouter lets you operate in a variety of modes from manual to fully automatic. Another 58-pg user's manual takes you through tutorials on using the autorouter. The manual covers strategies you can use to fine tune the router to do what you want. I didn't have time to run through the autorouter tutorials and learn to use it. The company also sells other autorouters.

My overall impression of the Pads software is that it can efficiently handle virtually any type of pc-board design work with the exception of high-speed, matched-line-length designs. The company plans shortly to introduce an electrodynamic checking module to better address the needs of high-speed pc-board design.

I felt the software had a good combination of automatic features and plenty of flexibility for efficient manual work. The only weak area I noticed was in the parts library for the schematic entry software.

While using the libraries I discovered two small problems. The LM319H part in the library is a dual comparator that should use a 10-pin TO-5 metal-can package. Although the pin numbering was correct for the metal can in the schematic, the pc-board decal called out was a 14-pin DIP. The other problem was more of an omission than an error. The 74LS32 part did not have a Demorgan equivalent, as was the case for other standard 7400-series gates.

My suspicious nature leads me to believe the library might have a few more problems. Although the problems I mentioned are small, they are a departure from the high quality I experienced with the rest of the software. Mark Pavitt, VP of marketing for Pads Software, said that the company is aware of a few problems in the libraries and is planning to license outside libraries for use with Pads Logic. EDN

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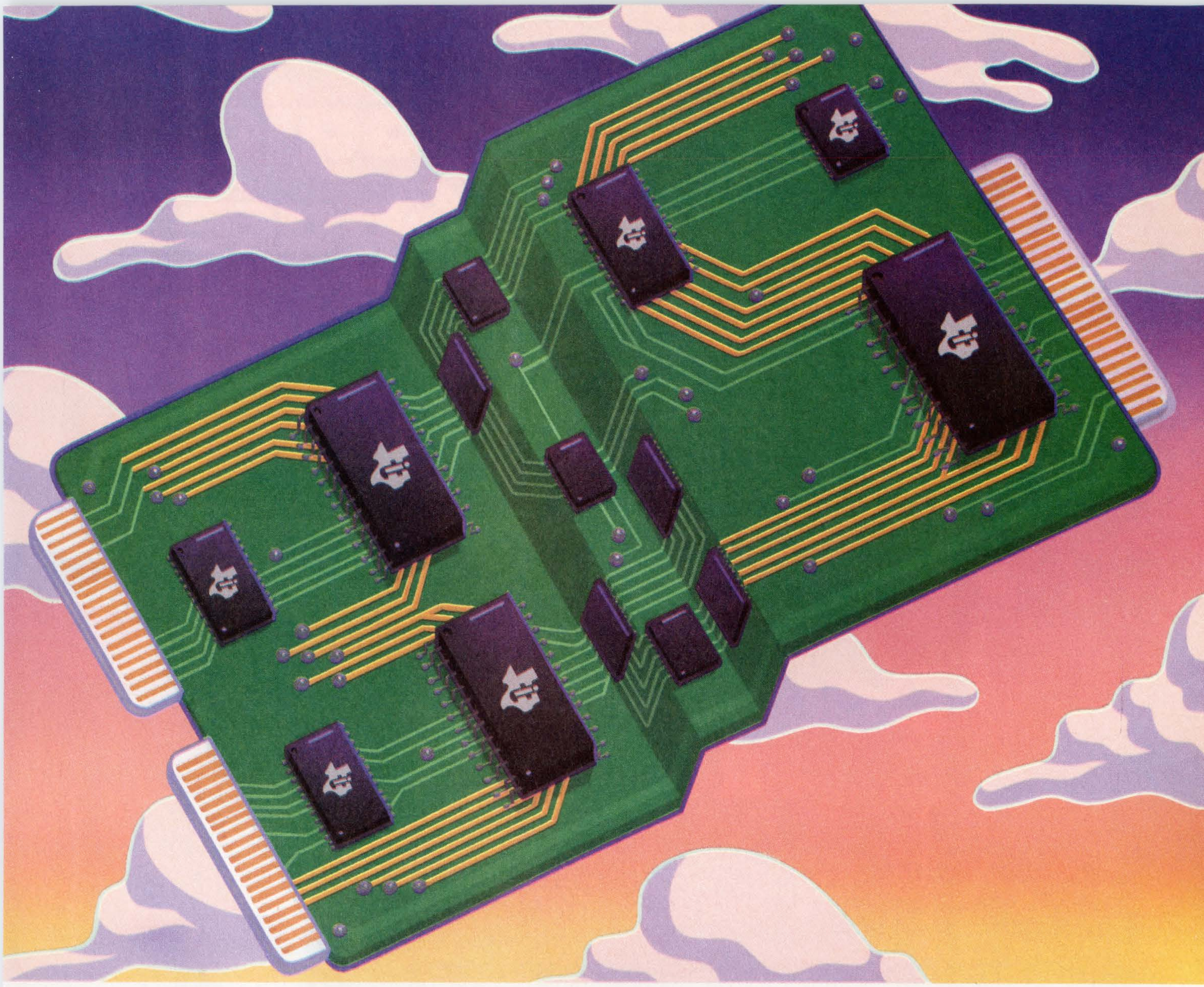

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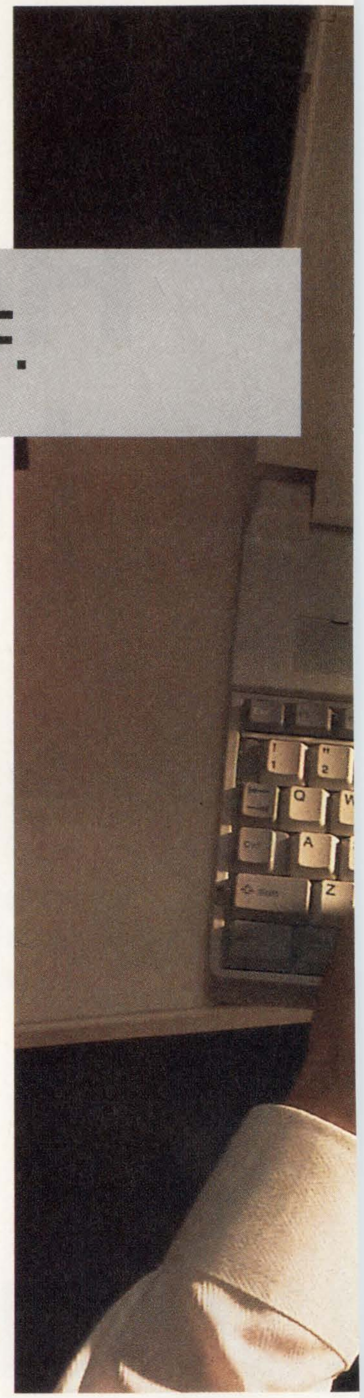

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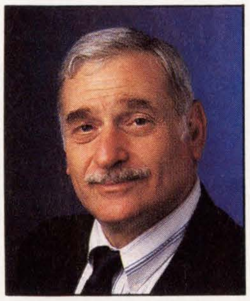
32-bit PCs take on embedded applications

RAY WEISS, Technical Editor



Instead of using a µC, you can now drop in a complete 386/486 PC to provide a user interface or to control hardware.

Plummeting 386/486 prices are making the embedded 32-bit PC a viable option for control and monitoring applications. The embedded PC has increasingly become a drop-in alternative to less expensive but more design-intensive microcontrollers (µCs) and microprocessors. The idea behind an embedded PC is simple: Instead of designing in a µC or µP from scratch, why not just drop in a complete PC and treat the subsystem like an embedded controller? There are clear-cut advantages to using an embedded PC:

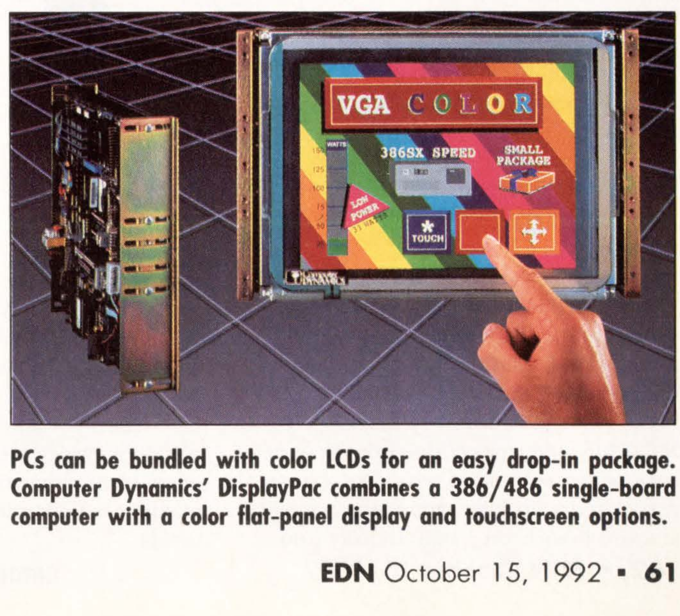
- Minimal system design because a PC is a complete subsystem
- Simpler cross development because embedded target matches PC host
- Low-cost, highly interactive, effective development tools
- Access to a huge base of PC applications
- Usable hardware from handheld and portable PCs
- Large PC engineering and programming talent pool
- User familiarity with DOS and Windows interfaces.

Many embedded systems engineers and managers are learning new design lessons. "I was a believer in the old way of doing your own complete system design," says Bill Richardson, director of engineering at LeCroy Corp (Chestnut Ridge, NY), an instruments and oscilloscope vendor. "Luckily, some of my staff saw a new way—using an embedded PC—and pressed for it. And I finally listened to them. The result was that we got 2 to 3 times performance increases with an 386/486 at 60 to 70% less cost." LeCroy used a PC mother board as the mainframe controller for its Model 7200A, an advanced, modular digital oscilloscope.

Embedded PCs aren't for everybody. If you need highly deterministic, real-time operation, an embedded controller is a much better bet. Embedded PCs, however, make sense for fast turnaround, not-quite-hard real-time systems with product-manufacturing run rates under 5000 units. Lots of applications let you drop in an embedded PC as a box, a mother board, a single-board computer, or a PC on a bus card.

Embedding PCs

Embedded PCs are busily at work in applications that range from controlling military systems to running amusement parks. Ruggedized PCs supported the Patriot Missile systems used in Operation Desert Storm and VME-based PCs (Radisys) act as controllers in Disney's new EuroDisney theme park in France. Also, take a look close to home. If your company is using new board or chip production equipment, you're apt to find



PCs can be bundled with color LCDs for an easy drop-in package. Computer Dynamics' DisplayPac combines a 386/486 single-board computer with a color flat-panel display and touchscreen options.

EMBEDDED PCs

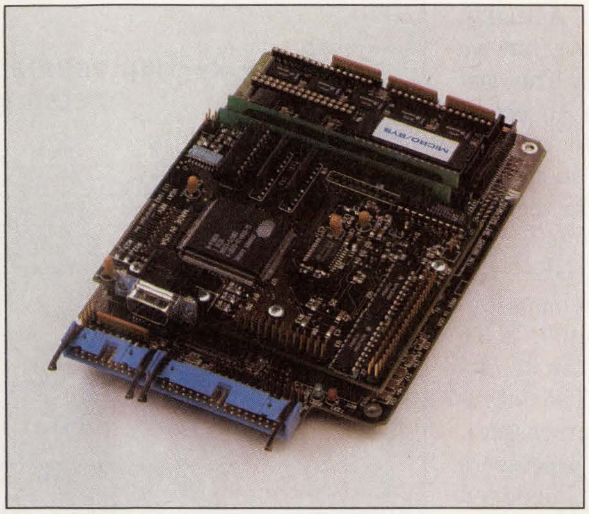
one or more embedded PCs.

Embedded PCs range from off-the-shelf PC systems to roll-your-own mother boards. Many low-level control applications can be run directly with a PC under DOS. "For a couple of contracts I worked on for large industrial controllers," says Alvin Schneider, an engineering consultant in Minneapolis, MN, "PCs were just put into rugged boxes. One industrial application was to control molten metal flow. The PC had no problem handling it. However, you do have to be careful with DOS because it's not preemptive. DOS services, such as graphics, can block critical interrupt processing."

In addition, PCs serve as networked remote controllers, linking into industrial and commercial controllers. And for more complex applications, many engineers use PCs to front-end real-time embedded µCs or rack-mounted controllers. These PCs provide monitoring stations and user interfaces. Other designers simply take the PC hardware, drop DOS, and substitute deterministic, real-time operating software.

Low-power 386/486s open up embedded PCs to handheld and portable applications. Portable PC chips and boards are being designed into handheld instruments. "We couldn't use PC technology before," says the chief engineer at a handheld instrument company. "Now we're developing our next-generation products using 386SLs and low-power 486s. We couldn't use the CPUs before, but now they have the low-power operation to go along with their 32-bit processor power and ease of design." (This engineer viewed using embedded 32-bit PCs as a competitive advantage and didn't want to use his company's name for fear of tipping off the competition.)

Bison Instruments (Minneapolis, MN) is now using the 486 single-board computer as the core for its new portable, 124-channel seismograph. "We used an Ampro LB/486 board piggybacked on a larger I/O board," says John Nelson, vice president of engineering. "We saved in design time, starting off with a board ready to go, complete with peripherals. We needed the 32-bit processing power; we store the program in flash and the explo-



Micro/sys integrated Windows 3.0 onto its Windowcard 486, enabling you to build-in a Windows interface with a minimum of hardware and software design effort. Windows is embedded in 4 Mbytes of flash memory.

Table 1—Representative 386/486 CPUs

Vendor	CPU	Clock (MHz)	Price (1000)	Comments
Advanced Micro Devices	386DX	25, 33, 40	$63	Standard 386. PQFP.
	386SX	33 20, 25	$47 $42	386 with 16-bit external bus. PQFP.
	386SXLV	20, 25, 33	$54	3V 386SX with 16-bit external bus. PQFP.
	386DXLV	25	$72	3V standard 386. PQFP.
Chips & Technology	38600DX	25 33, 40	$152 $180	Redesigned standard 386; same pinout; 10% faster.
	38605DX	25 40	$167 $198	Redesigned 386; extended pinout; 512-byte cache, faster. Superstate power management.
Cyrix	486DLC	25 40	$99 ($119)[1] $159 ($199)[1]	486 instruction set, in 386DX pinout; 1-kbyte cache.
	486SLC	25	$99	3V, QFP. 16-bit bus, 486 instruction set in 386SLC pinout, comes with 1-kbyte cache.
Intel	386DX	16, 20, 25 33	$96 $116	Standard 386, 32-bit external bus. PQFP.
	386SX	16 25	$49 $78.50	386 with 16-bit external bus. System management mode (SMM). PQFP.
	386SL	16 20 25	$48 (3.3W) $67 (3.3V) $96	Redesigned 386SX for low-power applications. 3.3V operation with SMM, cache.
	486SX	16 25	$99 ($174)[2] $119 ($243)[2]	486 with 16-bit external bus, no FPU.
	486DX	25, 30 50	$367 $536	Standard 486 with FPU. PQFP.
	486DX2	50	$487	
Texas Instruments	486SLC	25	$99	Same as Cyrix.
	486DLC	40	$119	Same as Cyrix.

Notes:
1. Price when bundled with 87DLC FPU.
2. Price when unit comes with 3.3V part.

ration data on hard disk. Actually, we used to be a 68K house, but we switched over to the 486. The cost of PC software relative to cross-development tools made the 486 very attractive and hard to resist."

Many engineers get the best of both worlds, mixing PCs with real-time μCs. For example, GEC Express Lift Company (Northamptonshire, UK) uses PCs and PCs on standard bus Eurocards for its elevator control systems. The elevators have 8-bit onboard processors, and each group of eight processors is controlled by a 68020. Embedded PCs act as the maintenance console for each elevator group. Full PCs are used as remote management stations that link to elevator groups.

"Initially we couldn't use PCs for control because they were too expensive," says J. Michael Gallagher, senior design engineer at GEC. "Now it's different. We've got a 386 card that plugs right into our main group single-height Eurocard industrial bus. We're considering doing more with PCs. A major factor is low-cost, specialized software that is easily available, such as expert system tools."

PCs have also invaded military turf. Ruggedized PCs offer a relatively low-cost, standard platform for upgrading and replacing existing equipment. For example, the US Navy's MAUDE (Multiple Auxiliary Device Emulator) program uses ruggedized PCs to emulate NTDS (Navy Tactical Data System) peripherals and, in some cases, CPUs for tactical systems. The software emulates the older equipment and links to the Navy NTDS systems via the NTDS bus. Special interface boards, such as the Sabtech Navigator II Serial NTDS, turn the PC into an NTDS node. Today's 32-bit PCs deliver a lot more processing power than much older equipment and can emulate obsolete peripherals or can be used

Table 2—Representative embedded 386/486 operating software

Vendor	Software	Price	Comments
Annabooks	AT BIOS Kit	$199	C source BIOS. Comes with 10 licenses.
	MOS-DOS	$595 (3.xx)	
	Developers Kit	$695 (5.0)	
	MS FLASH File Developers Kit	$95	High-level drivers to create flash file system. Over 10 licenses, $5 to $7 royalty.
Datalight	ROM-DOS	$495	ROM version of DOS comes with Mini-BIOS.
	C-thru-ROM	$495	Kernel and DOS-like I/O services link to C object DOS 3.31 compatible OS.
Digital Research	DR DOS 6.0	OEM[1]	Full DOS 5.0 and Windows compatibility.
	FLEX OS	OEM[1]	Real-time, multiuser OS. DOS application environment for 386 protected mode.
	PalmDOS	OEM[1]	DOS for palmtops. Works with PCMCIA, power management.
(Micro/sys) Drumlin	Divvy	$229	Multitasking kernel sits on top of DOS. Single and multiprocessing versions.
	Divvy/MPX	$429	
General Software	Embedded DOS	$995, $495 starter	Multitasking, re-entrant DOS. Runs in RAM. Comes with source. 32 kbytes minimum.
	Boot Tool Kit	$149	Builds bootable object with DOS services. No royalty.
JMI Software Consultants	C Executive	$2300	Multitasking kernel follows C I/O standards. Easy for C programmers to use.
Kadak	AMX 86	$3000	Multitasking kernel. Supports DOS command-task application. Runs in 386/486 real mode.
	AMX 386	$4000	Protected-mode multitasking kernel. Uses extended memory with Phar Lap extender.
Integrated Systems	pSOS	From $4000	Popular multitasking OS. Supports DOS as a task.
Intel	iRMX for Windows	$5595	Multitasking kernel runs DOS or Windows as task. Supports Windows DDE (dynamic data exchange).
MCSI	ExeCite	$99 $198	Runs .exe files without DOS. Comes with file system. 16-kbyte RAM.
Microsoft	DOS 3.3	OEM[1]	DOS 3.3, 5.0 are available for ROM. DOS 5.0 supports flash memory, power management.
	DOS 5.0	OEM[1]	
	Windows 3.1	OEM	ROMable version for embedded systems; windowed; cooperative; multitasking.
Microware	OS-9000	$995	Full OS. Supports DOS and Windows as a task. Emulates DOS BIOS. Runs major DOS applications.
Ready Systems	VRTX-32/386	$12,500	Development environment; real-time kernel for 386 protected mode; source-level debugger; runs VRTX-32/386 kernel.
US Software	MultiTask! 80×86	$24.95	Multitasking OS kernel. Runs DOS as a task.
	MultiTask! 386/486	$34.95	Protected-mode multitasking OS kernel.
	ProtoTask!	$14.95	Multitasking OS runs on PC for testing MultiTask! code on host PC.
	GoFast 387	$24.95	ROMable 387 emulator for 386SX, 486SX. Fast-floating point. Used by Intel.
Ziatech	STAR System STARWindows	$295	Runs on Ziatech STDbus board and provides multiprocessing with CPUs communicating, using the STDbus as a LAN medium. STARWindows lets CPUs running DOS pass info to CPU running Windows via DDE.

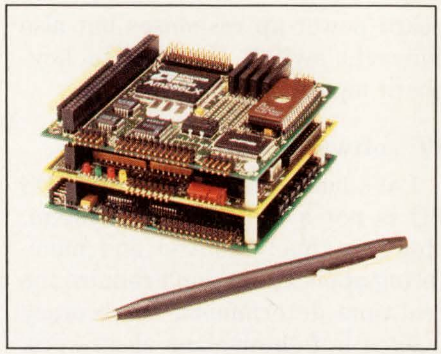
Notes:

1. OEM pricing to be negotiated.
2. Annabooks sells small volumes of these Microsoft products.

in lieu of more expensive NTDS test sets.

According to Bill Travin, the US Navy's FSG-7 program maintenance officer, NTDS emulators have saved the Navy well over $1 billion. "Not only are the PCs cheaper," he says, "but they are state of the art, and all kinds of engineers and programmers can work with them. These PCs saved us both money and time."

Of course, drawbacks exist to getting on the fast-moving PC technology train. For one thing, when you buy into PCs, you also buy into the accelerated PC design cycles, with large technology shifts in products, chip sets, and CPUs. "PC's are a different case," says LeCroy's Richardson. "The evolution of products is unbelievable—try nine months or less. Components don't stay still. You have to be able to move with it. You can buy off-the-shelf components and mother boards because of PC standards, but you have to qualify your vendors and test for compatibility. With PCs, you're basically trading NRE and design time for quality control, test, and manufacturing flexibility. In general, we've found PC quality to be very high."



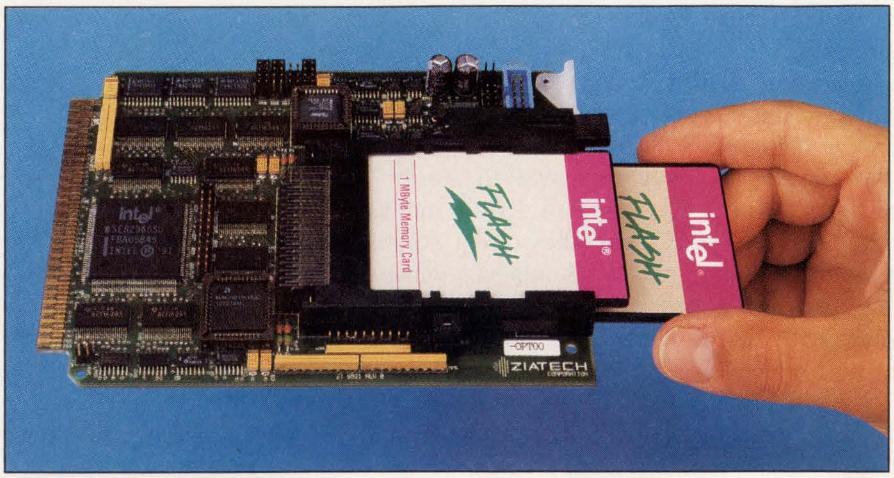
PC/104 defines stackable modules with an internal ISA-like bus that replaces the standard card with two high-reliability connectors (64-pin P1, 40-pin P2 connectors).

Table 3—Representative 386/486 embedded PC boards

Vendor	Board	Price	Comments
Arcom	SCIM386SX	£627 (100)	16/20/25-MHz 386SX to 4-Mbyte DRAM. STEbus board and local expansion bus.
Ampro	CoreModule 386SX	$571 (100)	PC/104 compatible; 25 MHz; 3.6×3.8 in.; 4-Mbyte RAM; 1-Mbyte solid-state disk.
Computer Dynamics	SBC-SXE	$815 (OEM)	25-MHz 386SX; 1.5-Mbyte ROM/RAM; 16-Mbyte DRAM; to 765-kbyte flash ROM.
Diversified	CAT975	$755	Passive backplane 386SX; to 16-Mbyte DRAM; 1-Mbyte PROM disk; watchdog timer; VGA-IDE interface.
Dolch	486 Apache	$2500	Passive backplane board; 50 MHz; to 32-Mbyte DRAM.
Dyna Five Corp	Baby Bullet 386SX-25	$1095	1-board computer; 25-MHz 386SX; IDE; ATbus; solid-state disk; watchdog timer.
Dynatem	V486	$2564	VMEbus 3U height; 20, 33 MHz.
I-Bus	I486/50	$1710	Passive backplane 486DX; 50 MHz; to 32-Mbyte DRAM; watchdog timer; IDE. Optional 256-kbyte secondary cache daughter board.
Industrial Computer Source	SB486T/33	$2195	Passive backplane CPU card; to 32-Mbyte DRAM. Comes with 0 DRAM. IDE and floppy controllers.
MCSI	IND-386SX	$895	Diskless 386SX; ISA bus; 4-Mbyte PROM-disk; watchdog timer; 25 MHz; 16-Mbyte RAM.
Micro/sys	WindowCard/486	$3655	1-board computer with 20/25 MHz 486. Embedded Windows 3.1 in flash EPROM.
Octagon Systems	5025	$745 (1 Mbyte) $895 (4 Mbytes)	25-MHz 386SX XT/AT card. Comes with DOS 3.31. Watchdog timer. Two 512-kbyte solid-state disks.
Prolog	7874	$2495 $3195 (33)	STD-32 bus card; 25/33-MHz 486. 4-Mbyte DRAM (to 16 Mbytes). Flash memory with DOS 5.0. DMA controllers.
Radisys	EMC-2100	$1195	System has box, CPU card, VGA controller, disk, 8-slot chassis. 386SL, 16 MHz, 1-Mbyte DRAM. Private bus. 25-MHz 386SL available ($625).
Winsystems	MCM-SBC486DX	$995	486DX 25 MHz, to 8-Mbyte DRAM STD Bus. Watchdog timer, power/fail reset.
Ziatech	ZT 8902	$1850	STD-32 bus. 25 MHz 486. Up 4-Mbyte RAM, 1-Mbyte flash memory. Watchdog timer. On-board DMA controllers.

A PC running with DOS isn't highly deterministic. "There are a number of undocumented features that can limit performance," says John Foster, the author of Annabooks' BIOS- and PROM-Kits. "But," he notes, "the saving grace is that there is the range of CPU performance available. In many cases, for moderate control applications, you can solve a performance problem by simply dropping in a faster PC. The 386 CPU rates are up to 40 MHz now and moving. And the hardware reliability is very good."

DOS's reliance on rotating memory is a problem for many applications that need more reliable storage. Alternatives include Microsoft's flash memory file system (also sold by Annabooks) for Intel flash memory, as well as disk emulators based on flash, EPROM/PROM, and battery-backed SRAM. Another problem is, believe it or not, running an embedded PC without a keyboard (DOS requires a keyboard for the power-up sequence). Embedded DOS usually takes care of the problem. However, if you're just dropping in a standard PC, you can buy specialized keyboard encoders or eliminators from Vetra that plug into the keyboard socket. The encoder not only generates the key-



The PCMCIA standard defines plug-in cards that can easily add memory or peripheral functions. This Ziatech ZT 8921 card uses PCMCIA memory cards for dynamic storage on the STDbus.

board power-up responses but also converts switch closures to keyboard inputs.

PC software

Let's face it, the classic MS-DOS PC is not a full real-time system. However, many control and monitoring applications don't require the real-time determinism or accuracy needed in fighter-plane electronics. PCs are limited in I/Os, number of interrupts (16), and interrupt response. Moreover, PC software, such as DOS, is single threaded, running only a single task at a time.

The good news it that there are still ways to take advantage of the huge PC hardware and software base. These include using a

- Standard PC with a disk or ROMable DOS. Disks can be replaced with silicon disks such as DOS 3.3/5.0, DR DOS 6.0, ROM-DOS, and C-thru-ROM, or ROMable Windows,
- Multitasking operating system that sits on top of DOS and schedules tasks on a cooperative, priority basis, such as Divvy,
- Real-time multitasking kernel that includes DOS as a task, such as Multi-Task!, OS-9000, iRMX for Windows, pSOS, and OS-9000
- Real-time kernel that provides DOS file and Int 21 (interrupt 21) services. The kernel may support multiple DOS task treads, reentrant services. These include embedded DOS and AMX,
- Real-time kernel that is not DOS compatible but runs on PC hardware. Some also execute on a PC host for debugging. These include C Executive, VRTX, MTOS, VxWorks, and OS-9.

Microsoft fields a ROMable DOS (3.3 and 5.0), as does Digital Research (now part of Novell) with DR DOS 6.0. Digital Research just released its PalmDOS, a special ROMable DOS for low-power, portable palmtop applications. This is a stripped-down DOS with provisions for PCMCIA cards, flash memory, and power management. It takes a minimum of 58 kbytes of ROM.

MS-DOS 5.0 also has a power-management driver that takes advantage of the new Intel/Microsoft Advanced Power Management system (Power.Exe BIOS API) that supports four power states—ready, standby, suspend, and off. ROMed MS-DOS 5.0 takes as little as 57 kbytes of ROM. Both DR DOS 6.0 and MS-DOS 5.0 have PCMCIA card drivers and ROM disk emulators. DR DOS has provisions for linking into a network, including security passwords and hidden partitions.

If you are willing to spend a few megabytes for OS storage, you can even get embedded Windows 3.1. Microsoft is fielding ROMable Windows, complete with PCMCIA drivers, power management, and disk emulator. In Windows, power management comes as an installable driver and a virtual device. Developers can add options using DLLs (Dynamic Link Libraries).

One way to put multitasking into embedded PCs is to run a multitasking kernel above DOS. That is what Micro/sys' Divvy does. This kernel delivers a cooperative scheduling layer above DOS with multiple tasks. This technique is effective for many industrial control applications that don't have hard real-time requirements. Divvy is compatible with standard DOS development languages and tools.

Many control applications combine DOS software with specialized real-time application code. A real-time kernel that runs DOS or Windows as a task with other real-time tasks works well for this class of application. Users get a well-known interface and a PC application if needed, while the real-time work is handled by the multitasking kernel. For example, Intel's iRMX real-time OS for Windows runs Windows or DOS as an iRMX task with other tasks.

DOS, with all its warts, is an extremely well-documented and well-known application-program interface (API). An army of PC programmers knows the inner workings of Int 21 requests for DOS services, as well as the DOS file system innards. One way to tap into that expertise is to provide DOS-like services on a real-time kernel. Some systems, such as AMX, provide a real-time kernel with multiple tasks and a single DOS thread. Others, such as embedded DOS, deliver a real-time kernel that handles multiple DOS threads.

A different tack is to use low-cost PC hardware but run a standard real-time operating-system kernel such as VRTX, C Executive, MTOS, and VxWorks. Some of these kernels, such as C Executive, can run on both the host and the target system. Other kernels, such as VRTX, MTOS, VxWorks, OS-9, and pSOS, are part of sophisticated cross-development environments that support interactive PC-host to embedded-PC target debugging.

You can take your PC in a lot of hardware flavors. Just what form

For more information . . .

For more information on the 32-bit embedded PC products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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EMBEDDED PCs

it takes is dependent on a number of factors, including price, portability, power and size requirements, and processing needs. Outside of just bolting a PC onto your equipment, you can use a

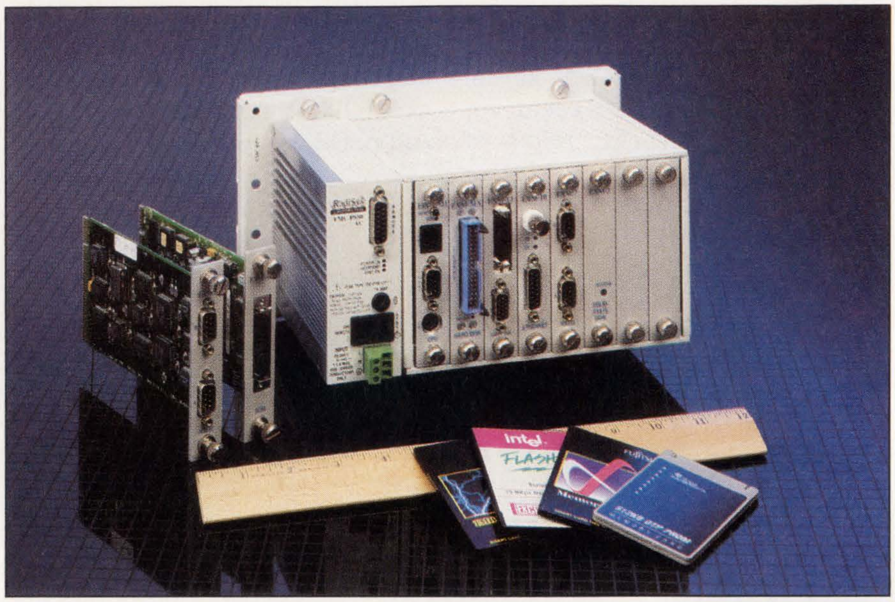
- Standard-form-factor mother board
- ISA passive backplane with a CPU card
- Single-board PC
- Single-board PC interfacing to STD, VME, or STE buses
- PC chip set to roll your own PC.

If you have the room and power, you can simply bolt-in a PC or drop-in a standard-form-factor PC mother board. This approach becomes less attractive in harsh environments or tight spaces. Mother boards are the cheapest way to go, but they may not be optimal for cooling, with the base generating heat that rises among the plug-in cards. Also, CPU replacement is much harder and the PC ISA bus is not a high reliability connector/backplane combination.

Many engineers simply drop-in PCs and link them to single-board computers for control. "If you need a keyboard, a floppy disk, and an interface, a PC is a good choice," says Robert Coomer, president of R.L.C (Atascadero, CA), a single-board computer vendor of 186-based systems. "A lot of our customers actually use a PC for the interfaces and then turn to μC-based SBCs for real-time control."

One popular PC industrial-automation alternative relies on passive ISA backplanes, which are used to seat AT card PCs and peripheral cards. Cooling characteristics are much better, and CPU cards are easily swapped. With this structure, the CPU cards are more reliable, but systems still provide the advantage of using standard PC I/O cards and a range of specialized engineering and peripheral cards.

Self-contained single-board computers are one way to build and embed a PC. A single-board computer holds a complete PC and has I/O interfaces. It can have bus interfaces as well. These computers are more expensive than other options but have small form factors and high board densities, making them ideal for embedded in-size critical applications. Some single-board computers have connectors for adding daughter cards to increase expandability.



Embedded PCs run in industrial environments. Radisys EMC packages small cards into an industrial enclosure. PCs plug right into the private bus.

An attractive alternative that combines single-board computers and the ISA bus is the PC/104 standard. Pioneered by Ampro, it has been accepted by more than 25 board vendors, including CPU board vendors such as Dyna Five. Instead of relying on a bus to interconnect boards, PC/104 proposes stacking the single-board computer modules and linking them with a PC bus that uses higher reliability, on-board stack connectors. PC/104 is a proposed extension to the IEEE PC bus standard. The modules can also be combined on a carrier card.

Module stacks save space; there is no need for a separate bus backplane. (National Semiconductor tried a such a busless stack years ago with its MA2300, based on an 8-bit NSC800 μC.) A 3-module, PC/104 stack is only 2 in. high. The modules, based on the Ampro "MiniModule" form, are 3.6 ×3.8 in. Stacking also minimizes bus drive requirements, due to smaller bus signal runs, dropping to 6 mA for PC/104.

PCs are also now an option for most standard bus systems, including STD, STE, and VME buses. For example, you can buy a STDbus or VMEbus PC card, drop it into your system, and take advantage of low-cost PC technology. PCs are increasingly used in these bus systems for control and user interfacing. Thus, engineers can take advantage of the wide base of PC development software for specialized bus systems.

For the classic board designer, rolling your own PC can be a piece of cake if the design is straightforward; it can also be complex, depending on system interfacing and processing. Most PC chip-set vendors have ready-to-go board designs. However, small production-run projects may have difficulties getting access to chips and services, for PC

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EMBEDDED PCs

chip-set vendors are used to dealing in large sales volumes. A production run of 100 to 1000 systems may not be large enough to attract necessary vendor support services. This vendor attitude may change as Intel and Microsoft put increasing emphasis on embedded PCs.

Finally, pay careful attention to the emerging PCMCIA standard, originally aimed at defining laptop memory cards. The standard defines a series of credit-card-size cards, 3.3, 5.0, and 10.5 mm in thickness. The first form, the 3.3-mm cards, is now the de facto mechanism for adding memory to laptops, as well as peripherals such as modems and Ethernet connections. Coming are a raft of PC peripherals, including hard disks for the larger card forms.

PCMCIA cards have a good chance of becoming the add-on peripheral standard of the '90s. More than just a memory-card form, PCMCIA can be viewed as the add-on bus or the peripheral bus for PCs. For embedded systems, PCMCIA cards offer a cheap, rugged, compact removable mechanism to add memory, peripherals, connectivity, or functionality to a controller. EDN

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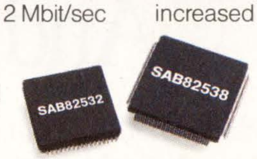

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Fault-tolerant 8.4-Gbyte disk array moves 20 Mbytes/sec over SCSI-2 bus

The $31,650 Rimfire 6710 disk-array subsystem provides 8.4 Gbytes of high-speed data storage in a fault-tolerant package by ganging nine 3.5-in. hard-disk drives in a RAID-3 configuration. RAID stands for redundant array of independent (formerly "inexpensive") disks. The RAID-3 configuration stores user data on eight of the nine hard drives; the ninth drive stores parity information. If one drive fails, the subsystem continues operating by regenerating the missing bit on the fly.

Operating the eight data drives in parallel also allows the disk array to deliver a 20-Mbyte/sec burst transfer rate and a sustained rate of more than 19 Mbytes/sec over a 16-bit SCSI-2 port. If you use the subsystem as an 8-bit peripheral, you halve the transfer rate. The subsystem's SCSI-2 port operates as an 8- or 16-bit port, synchronously or asynchronously, using either the fast or slow SCSI protocol.

Each drive in the array resides on its own carrier. You can swap out a drive while the array is operating (hot swap), and the array can then automatically regenerate data on the replacement drive. You select whether regeneration occurs as a background task during inactive time periods, in an interleaved mode that partitions the disk accesses between the data-rebuilding and normal data-access operations, or in a dedicated mode that locks out user data requests.

Replacement disks need not be the same size or even from the same manufacturer. They only need have at least as much capacity as the drive you're replacing. This feature protects you from the inevitable obsolescence of a particular hard-disk drive or even an entire disk format. (Have you attempted to buy any 12-in. hard-disk drives recently?)

An RS-232C port allows you an alternative to the SCSI-2 port for maintenance operations. The vendor supplies DOS-based maintenance software that lets you configure the subsystem, monitor its performance, and run diagnostic tests. You can also conduct remote diagnostics by connecting a modem to the serial port. A keypad and LCD provide local control of the unit.

The array measures 7×17×22 in. You can mount it in a rack or operate it as a desktop unit. The subsystem's power supply automatically switches between 90-130V and 180-264V settings and accepts 50- or 60-Hz power. The unit weighs approximately 60 lbs, including the disk drives.—**Steven H Leibson**

Ciprico Inc, 2800 Campus Dr, Plymouth, MN 55441. Phone (612) 551-4000. FAX (612) 551-4002.

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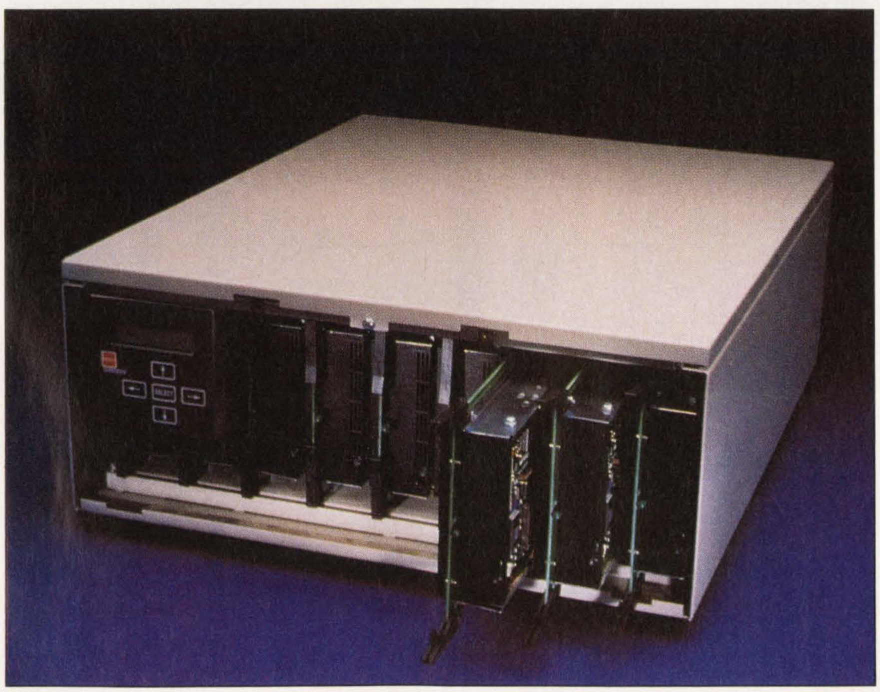


Nine 3.5-in. hard-disk drives mounted on independent carriers in a RAID-3 (redundant array of independent disks) configuration provide fault-tolerant storage of 8.4 Gbytes.

Accelerator chips speed Windows graphics

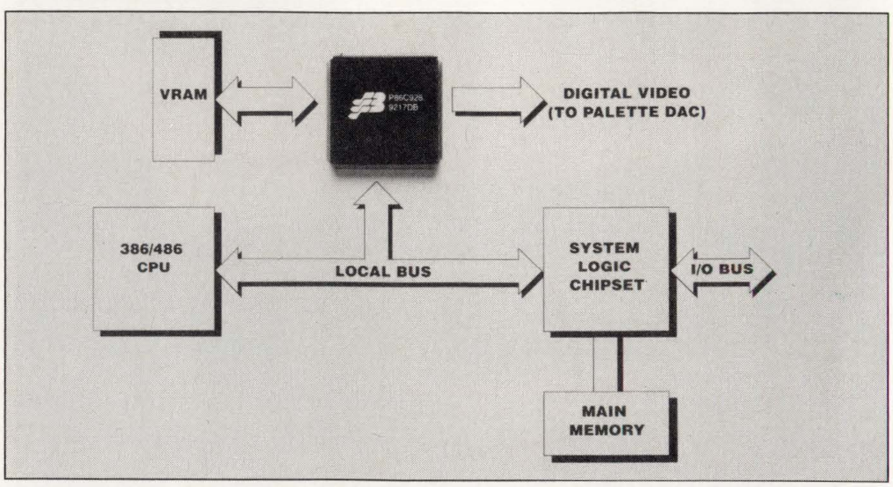
Three single-chip graphical-user-interface (GUI) accelerator chips speed up applications running under Windows 3.0 and 3.1, X-Window Systems, and AutoCAD. The 86C801 and 86C805 utilize dynamic RAM (DRAM) for the display memory, and the 86C928 utilizes video RAM (VRAM). The 86C801 connects to a 16-bit ISA bus, the 86C05 connects to a 32-bit 386DX/486 local bus or a 32-bit EISA bus, and the 86C928 connects to any one of the three buses.

These GUI accelerators implement functions on-chip that Microsoft has defined as critical to running Windows. These functions include line drawing, hardware cursor, bitblt, and clipping. Because the devices accelerate these functions, common GUI operations, such as opening and resizing windows, pulling down menus, painting menu backgrounds, and dragging and scrolling, appear instantaneous to the user.

In addition, the chips accelerate 24-bit true-color graphics for Windows 3.1 applications. Unlike SVGA controllers, where the CPU performs all 24-bit operations, these accelerator chips offload 24-bit-color operations from the CPU and implement these tasks themselves. For multimedia applications, the chips have a Genlock function to synchronize the accelerator's video output with an external NTSC or PAL video signal. In addition, via a shared memory architecture, an 86C928-based Windows accelerator board can handle real-time video signals via a video-coprocessor attachment.

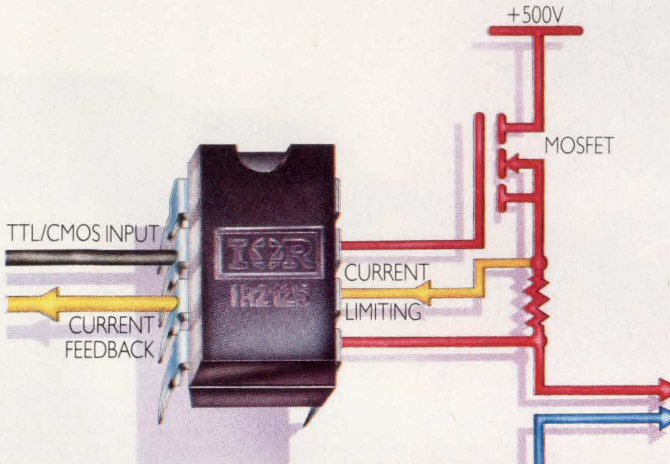
The 86C801 and 86C805 accelerators both operate with as much as 2 Mbytes of DRAM. The 86C928 operates with as much as 4 Mbytes of VRAM. All three of the accelerators are compatible with existing drivers for the company's 86C911 accelerator. The 86C801 comes in a 160-pin plastic quad flatpack (PQFP) and costs $29 (1000). The 86C805 comes in a 184-pin PQFP and costs $35 (1000). The 86C928 comes in a 208-pin PQFP and costs $65 (1000).—**John Gallant**

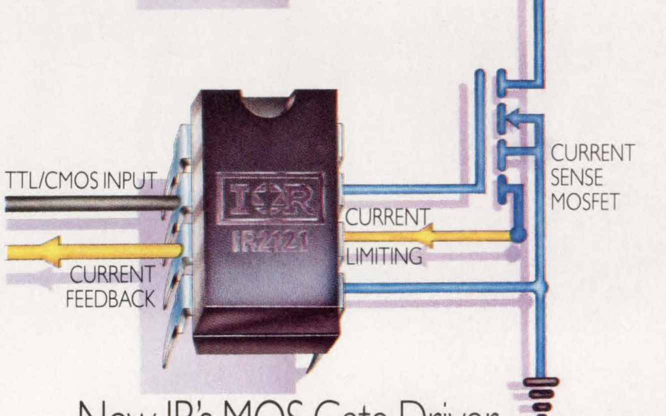
S3 Inc, 2880 San Tomas Expressway, Santa Clara, CA 95051. Phone (408) 980-5400. FAX (408) 980-5444. **Circle No. 382**



The 86C928 GUI accelerator can attach to a local bus and 4 Mbytes of VRAM to accelerate graphics from 18× to 30× over SVGA modes.

Designated Drivers.





Now IR's MOS Gate Driver family includes high-voltage devices designated for applications where protection is paramount: Introducing the IR2125 and IR2121, designed to drive and protect motor controls and other circuits up to 30 kHz.

These MGDs outperform costly multi-component drive circuits. They simplify design, provide protection, and can eliminate the transformer and associated components in many applications.

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The 500V IR2110 with 2A source/sink capability is setting the industry standard for a half-bridge driver. It's driving pairs of FETs or IGBTs in motor control, UPS, solid state ballast, and switching power supply applications all the way up to 500 kHz.

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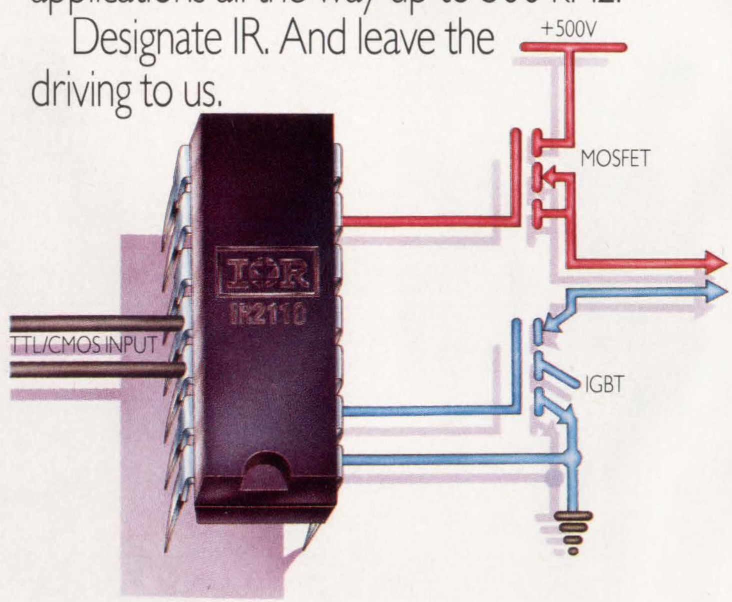

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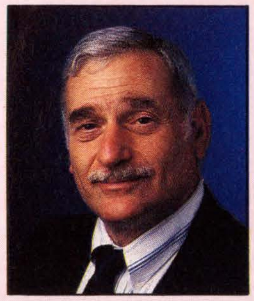
RISC/2: Half RISC, half CISC μPs break traditions



There's an old saying, "Whenever anything becomes common knowledge, it's probably wrong." Take RISC technology: these days, RISC processors have fallen into a kind of ho-hum, lockstep, taken-for-granted technology. Many developers believe RISC μPs have now settled down to a long and hard, but stable and well-defined development path, a path leading to hefty RISC CPUs.

That's a far cry from when stripped-down, hungry RISC μPs first barged into the desktop arena—things started with a bang. First-generation commercial RISC came barreling out of its corner at the bell, swinging away at its CISC opponent. Faster, smaller, cheaper was its battle cry. And RISC performance won the day. Today, RISC dominates the workstation/server ring.

Now commercial RISC is shifting to accelerated RISCs such as TI's SuperSPARC, Cypress' HyperSPARC, Mips' R4000, and DEC's Alpha. Using superpipelining or superscalar techniques, they crank CPU performance by kicking up clock rates and issuing more instructions per clock cycle; in super pipelining by shaving the clock and starting an instruction every half cycle; and in superscalar by decoding and starting multiple instructions every clock cycle.

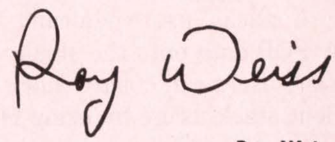
RISC technology has congealed into a nice set of common definitions: load/store execution, pipelining, simple instruction sets, hard-wired minimal logic (compared with microprogrammed CISC), relying on software for most exception processing, simple addressing, fixed-length instructions, a large register set, and fast single-cycle execution (dependent on a tight ALU cycle and a mechanism feeding instructions every cycle). Implicitly associated with these definitions are general-purpose register machines having on-chip or tightly coupled caches, on-chip FPUs, and instruction sets that increasingly look alike.

And so here we are, all nice and safe and cozy, comfortable in commonly accepted definitions of desktop RISC. No more surprises, we say; nice going. Wrong. A new RISC perturbation has been seeping from the woodwork: embedded, minimal RISC. These are stripped down μPs combining 32-bit RISC throughput with low power and penny-pinching cost. "RISC/2" (RISC-over-two) is probably as good a tag as any for this deviant branch of the RISC tribe that harbors latent CISC traits.

RISC/2 μPs target embedded or portable applications and so lack many of the amenities and wide buses of their desktop cousins. Whereas RISC stripped down hardware to the bare metal for speed, RISC/2 aims at mixing RISC and CISC flavors, seeking an optimal triad of speed, low power, and low cost. Two such 32-bit RISC/2 CPUs are the ARM family (formerly Acorn and now made by VLSI Technology and Plessey) and the Hyperstone (from Hyperstone Electronics, GmbH, and soon to be a Zilog core). Both are minimal CPUs with significant RISC sins. Apple, by the way, has selected ARM to power its Personal Communicator, supposedly the next killer information appliance after PCs.

RISC/2 competition is growing. Entering the ring is a new contender: Hobbit, a 32-bit RISC/2 μP from AT&T, targets personal communications. A RISC μP by many standards, Hobbit, a resurrection of AT&T's C-machine research, violates RISC canons with a stack-oriented architecture (no user-accessible registers) that—horror of horrors—operates directly on memory. The low-power Hobbit comes complete with a support chip set and runs the Penpoint OS for portables.

RISC (and CISC) μP vendors that waited for portable applications to fall gently into their laps now have a fight on their hands. There's a moral here: don't drop your dukes and assume that current technology is forever. Technology tends to defeat the status quo, making fixed definitions obsolete and spawning new contenders as it mutates. Watch yourself in the technology clinches and don't take any wooden definitions.



Ray Weiss
Technical Editor

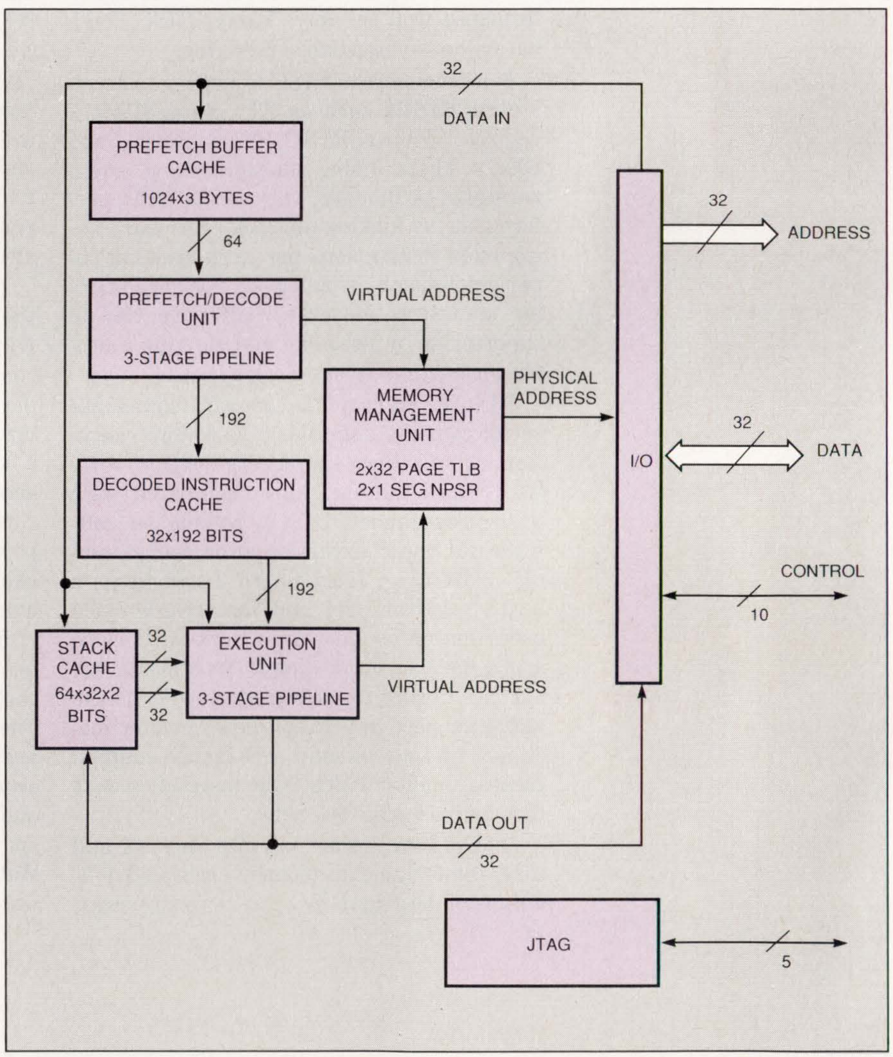
AT&T C-machine targets personal communicators

Many engineers believe that the next killer hardware after the PC will be personal communicators. These are small handheld devices with high processing power, graphical interfaces, and communications capability. AT&T has tailored a RISC processor and chip set for personal communications: the Hobbit, or ATT92010 μP, accompanied by a 4-chip set. The chips include a system management device, a display controller, a PC-MCIA interface device, and a P-ISA (private bus) interface device.

Hobbit and its support chips are low-power devices, with performance that matches first-generation commercial RISC. Although Hobbit's performance is roughly comparable to that of a 25-MHz 80486, its architecture is optimized to execute C programs. It is a stack-based machine that has no user-addressable registers. Instead, the CPU caches the application stack—the stack that a C compiler creates for each function's activation environment (which holds the function's local variables). The top of the stack is cached on chip but is addressed as memory, not as registers.

Instead of moving the stack into registers for fast code access, as most RISC processors do, Hobbit provides direct access to the actual function stack. The CPU caches the top of the user stack in a 256-byte cache. When a function is called, the hardware fills the stack with the function's activation environment. Similarly, the hardware pops the environment when control returns to the calling function. Unlike classical stacks, user code can't PUSH or POP data onto the stack. However, users can ensure more efficient stack usage by using Hobbit instructions that prepare the stack and ensure that there is enough room on the stack for a function. Additionally, the top of the stack cache serves as a fast accumulator—interim results of operations can be put on the stack for local storage. The 256-byte stack has a 87% hit ratio according to AT&T studies.

Hobbit also takes an innovative approach toward the classic RISC problem of keeping the instruction flow going. To do this, Hobbit essentially works as two separate machines: a fetch/decode machine and an execution unit. The fetch/decode machine is made up of a prefetch buffer, or instruction cache, of 3 kbytes, and a 3-stage, pipelined prefetch/decode unit. The fetch/decode machine fetches instructions, caches them, and decodes them before they are needed for execution. The decoded instructions are converted into a 110-bit control word that is held in a 32-entry decoded instruction cache, which then feeds instructions to the execution unit as needed.



AT&T's Hobbit combines RISC performance with C-machine stack architecture. Variable-length instructions are fetched, decoded, and stored as fixed-length codewords for execution.

This 2-step tactic is very clever. Hobbit uses variable-length instructions, which it fetches, decodes early, and converts into fixed-length control words for fast execution. Thus, this μP has the benefits of variable-length instructions (compact code), as well as fixed-length instructions (faster execution).

If an instruction is followed by a branch, the branch is included in the leading instruction's decoded control word. In effect, branches are folded into the preceding instruction, compacting execution code. Each instruction control word has two address fields and a branch-prediction bit (set by the compiler) to preselect which path to take. Successfully predicted branches take only one pipeline cycle in the execution unit, whereas unsuccessful branches cost three cycles.

AT&T Hobbit 32-bit μP

- 25-MHz clock
- Stack-oriented RISC architecture
- 15.6 VAX MIPS at 25 MHz
- 34 variable-length instructions
- 512-byte stack cache
- 3-kbyte instruction cache, MMU
- 32-bit external address and data buses
- 250 mW at 3.3V; 900 mW at 5V
- 132-pin PQFP, JTAG compatible
- $35 for CPU (10,000); $100 for CPU and chip set (less P-ISA bus interface chip). Sampling now, production 4Q92.

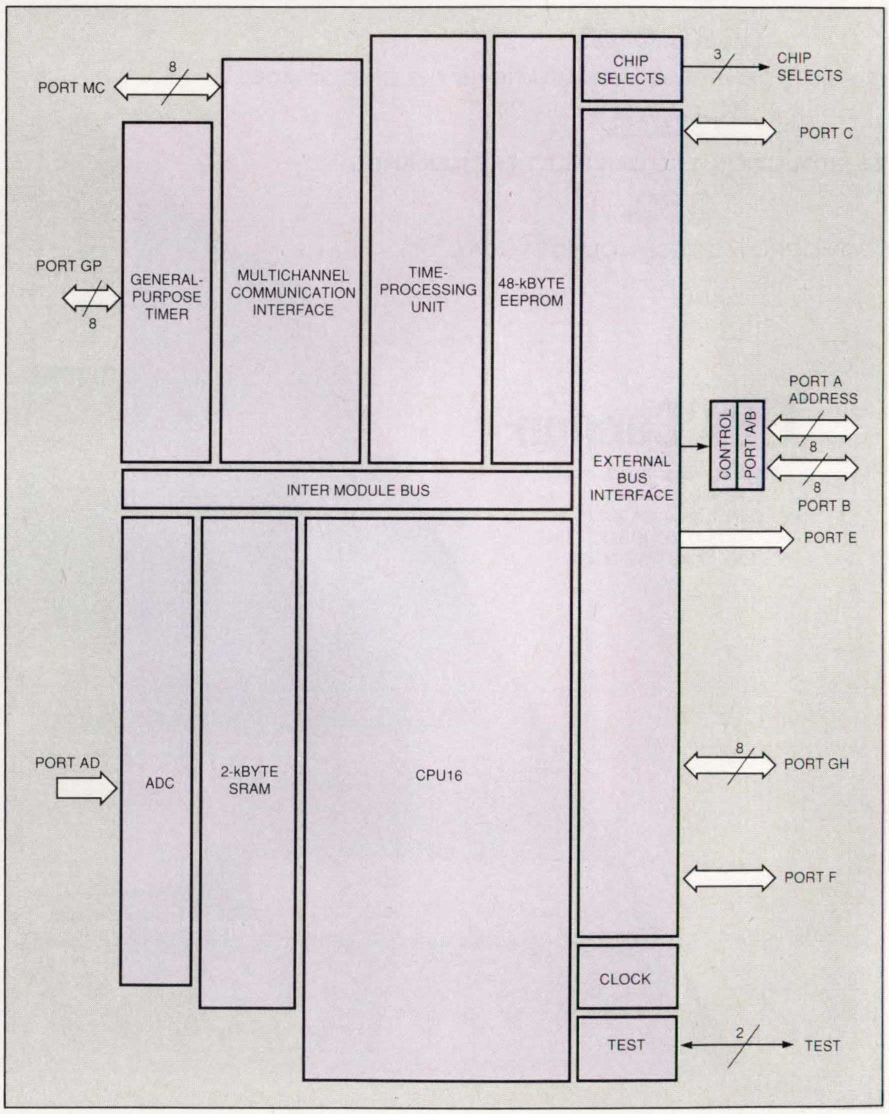
The CPU has a shallow, 3-stage pipelined execution unit and an MMU (memory-management unit) with two 32-entry translation look-aside buffers (TLBs), one each for data and instructions. The shallow pipeline and interruptible major instructions (MPY, DIV, and others) give Hobbit a relatively fast interrupt latency of 800 nsec.—**Ray Weiss**

AT&T Microelectronics, 1090 E Duane Ave, Sunnyvale, CA 94086. Phone (408) 522-5555. FAX (408) 522-4401. **Circle No. 395**

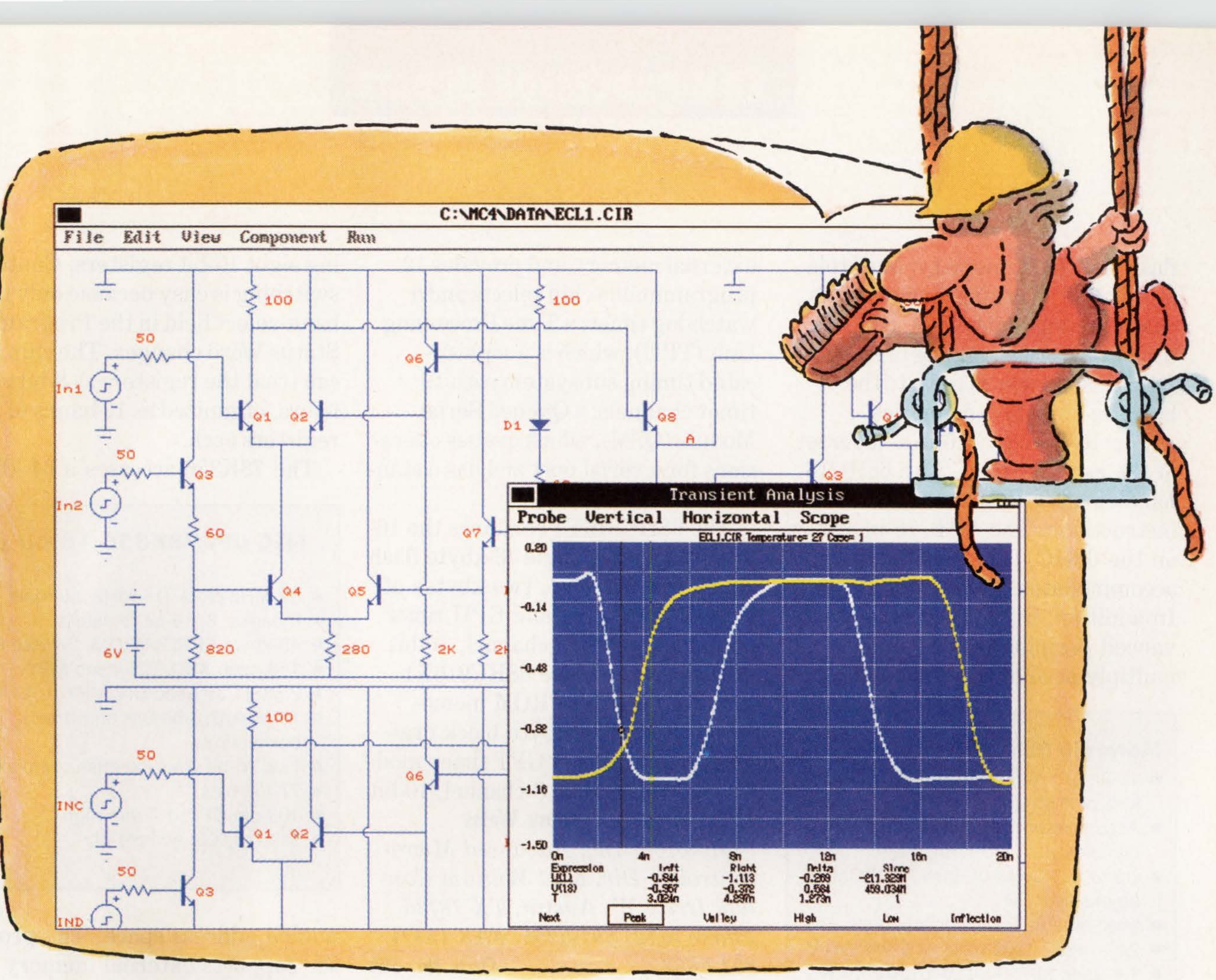
16-bit 68HC16 includes 48-kbyte flash EEPROM

Flash EEPROM is on its way to being a mainstream memory option for embedded control. Flash has the advantage of being electrically reprogrammable; it will eventually be onboard programmable with standard logic voltages. Motorola has moved flash EEPROM onto its 16-bit microcontrollers (μCs). The 68HC16 μC uses changeable flash for program memory.

Two configurations of 48-kbyte flash EEPROM for the 68HC16 include a single 48-kbyte flash memory, the 68HC916Y1, or 48-kbyte flash divided into a 32- and a 16-kbyte memory (the 68HC916X1). The smaller, 16-kbyte memory is block erasable: It's divided into eight blocks of two kbytes each. These blocks can be addressed individually for erasing, which minimizes overall erasure. The other flash blocks must be fully erased before recording new data. Data is written by byte or word; 12V dc is required to erase and write the



The 68HC916Y1 combines 48 kbytes of flash EEPROM memory with a 16-bit CPU and a full set of peripherals. Flash memory makes it easy to reprogram.



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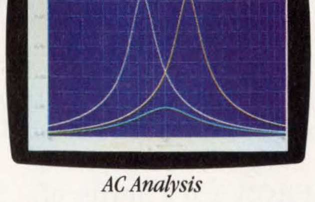

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CIRCLE NO. 54

flash EEPROM memory. Motorola is, however, working on moving its charge-pump technology, which is used in 5V programming of small EEPROM blocks in µCs, to the large on-chip flash memories.

The 16-bit 68HC16 is a superset of the 8-bit 68HC11. The 68HC16 handles all 68HC11 resources and instructions. The 68HC16 improves on the 68HC11 in that it routinely accommodates 1-Mbyte addressing. In addition, it incorporates advanced peripherals that include a multiply-accumulate unit (MAC).

Motorola 68HC916Y1 16-bit µC

- 16-bit µC, 16.78-MHz clock (from 32 kHz or 4 MHz)
- Accumulator-based design, with 2 accumulators; 2 index registers
- Up to 48 kbytes of flash EEPROM, 2 kbytes of RAM
- Inter Module Bus connects units
- 240-, 480-, 1300-nsec ADD/MPY/DIV
- 1.4-µsec MPY/ACCUMULATE cycle
- 8/16-bit external, multiplexed bus
- Choice of advanced timer modules with capture, compare, pulses
- ADC, serial communication channels, memory interfaces, watchdog timer
- 100 I/O pins
- Sample qty, first quarter 1993; in 160-pin PQFP, $75.

The µC has an accumulator-based architecture. Processing centers around two 8-bit accumulators (like the 68HC11) and a 16-bit accumulator. The two 8-bit accumulators can be treated as a single, 16-bit accumulator register.

The µC has a modular structure that is built on the Inter Module Bus (IMB), an on-chip support bus, which is the same bus that serves as a base for the 683xx specialized µC. This bus makes it easy for you to add peripherals in the future. The IMB modules include a General Purpose Timer (GPT) with free running timer/counters, compare/capture registers, and two PWM channels; a System Control Interface Module (SCIM), which interfaces external memory and provides 12 programmable chip selects and a watchdog timer; a Time Processing Unit (TPU), which is a sophisticated timing subsystem with 16 timer channels; a Queued Serial Module (QSM), which queues operations for a serial port and has a standard UART.

The 68HC916Y1 combines the 16-bit CPU with a single 48-kbyte flash EEPROM memory, two kbytes of static RAM, TPU and GPU timer modules, and an 8-channel, 10-bit A/D converter. The 68HC916X1 has two flash EEPROM memories—32- and 16-kbyte block erasable—along with a GPT timer module, a QSM, and an 8-channel, 10-bit A/D converter.—**Ray Weiss**

Motorola Inc, Advanced Microcontroller Div, 6501 William Cannon Drive W, Austin, TX 78735. Phone (512) 891-3255. FAX (512) 891-2652. **Circle No. 396**

16-bit µC beefs up peripherals and adds 48-kbyte ROM

Sixteen-bit processors are attracting designers who've run out of 8-bit processing power but can't afford to step up to 32 bits. Sixteen-bit processors offer better addressing, higher processing power, larger peripheral sets, and more on-chip memory. NEC's 16-bit K3 family's top-of-the-line µPD-78K356 integrates 48 kbytes of ROM/EPROM and 2 kbytes of RAM with a set of timing and signal-conversion peripherals, including a 2-µsec, 10-bit A/D converter.

With a 32-MHz external clock, the 78K356 has a basic instruction cycle of 125 nsec (NOP) with a 188-nsec ADD, which places it in the faster, 16-bit category. Register-based, the processor operates on eight register banks, each comprising eight 16-bit registers. Context switching is easy because only the bank-select field in the Program Status Word changes. The chip also can treat the registers as 8-bit registers, organized as 16 banks of 16 registers each.

The 78K356 accesses a 64-kbyte unified address space. The processor supports external memory with a multiplexed external bus, 16-bit address, and 16-bit data. A 16-bit stack pointer references a LIFO memory stack. The processor maintains user and supervisor modes to separate the system from application processing.

NEC µPD78K356 16-bit µC

- 32-MHz clock (16-MHz internal)
- 8 banks; 8, 16-bit registers
- 48-kbyte EPROM/ROM; 2-kbyte RAM
- 188-nsec ADD, 875-nsec MPY
- 2.688/1.31-µsec DIV/MPY-ACCUM
- 10-bit A/D, 8-bit D/A converter; 2-µsec conversions
- Five 16-bit timer/counter complex
- 77 I/O pins
- 100-pin QFP; 1.7-mm high
- $14 (10,000) sample qty

Processor throughput is upped via features that include a multiply-accumulate function, which will do single or multiple MAC cycles using a sequencer to run the ALU; a Macro Service Function, which processes interrupt events on a cycle-stealing basis, offloading the CPU; and DMA, which efficiently transfers data blocks. In addition, A/D conversion can be directly triggered from timer events, saving code.

The 8-channel, 10-bit A/D converter has three operating modes: under-input control, software control, or timing-triggered control. Four external signals can trigger conversion. One option allows pulses on one line to walk the conversion down the channels, converting the next channel at each suc-

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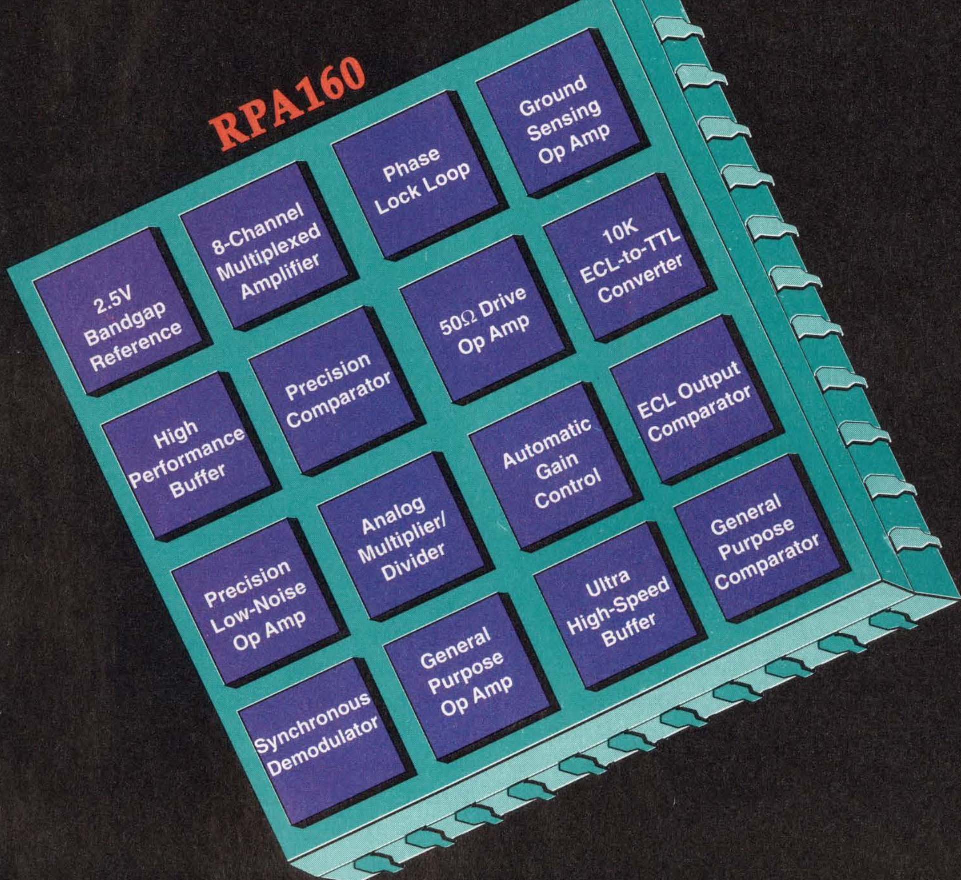

RPA 160
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Offset Voltage — 4 mV
Bandwidth — 160 MHz
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Supply Sensitivity — 0.2%/V

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Input Bias Current — 500 nA
Gain Bandwidth — 25 MHz
Noise Voltage — 2.5 nV/√Hz

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ceeding pulse. Conversion can also trigger from timing events (up to four timing-event signals). Conversion results are stored in eight conversion result registers.

Other peripherals include five 16-bit free-running timer/counters with 15 capture-compare registers, two PWMs (with 8-, 10-, or 12-bit resolution), an 8-bit watchdog timer, a UART, and a 3-input, 2-channel synchronous serial I/O port.—**Ray Weiss**

NEC Electronics Inc, Box 7241, Mountain View, CA 94039. Phone (415) 960-6000. **Circle No. 397**

8-bit COP8 µC gets smart C compiler

Using the National COP8 8-bit µC, embedded-system designers no longer have to stick to assembly language; the COP8C Code Development System C compiler generates highly optimized C code.

COP8C C COMPILER

- Compiler for 8-bit COP8 µC (to 8-kbyte ROM, 256-byte RAM)
- Expert system optimizers
- Generates ROMable code
- Integrates with existing ICE for source-code debugging
- $895 (C compiler only)

Developed by ByteCraft Ltd for National Semiconductor, the C compiler relies on multiple expert systems for efficiency. The systems select the right assembly-language instruction sequences and addressing for optimal operation. A profile of the target hardware is built and used as a database for the expert systems. Intermediate code passes through rule-based expert systems at different optimization stages. Code is optimized for local centers of reference, for minimal temporary storage or size, and to minimize register references (it actually scoreboards register references to eliminate redundancies).

ByteCraft uses these techniques for other C compilers, notably one for the 68HC05 (another minimal µC), which comes close to achieving hand-coded assembler efficiencies.

The compiler includes a C preprocessor. The compiler supports standard C constructs such as break, case, continue, do...while, for, goto, if, if..else, return, return expr, switch, and the following data types: char and int (8 bits), long (16 bits), pointer (8/16 bits), and short (8 bits). COP8C extensions are binary constants, interrupt functions, direct I/O port access, bit arrays, in-line assembly language, and direct register access. Variable modifiers include auto, const, extern, register, signed, static, unsigned, and volatile.

National's COP8 is a low-cost, minimal-architecture 8-bit µC with a 1-µsec ADD. Accumulator-based, the CPU has two index registers, up to 8 kbytes of program memory, and up to 256 bytes of RAM. Using C for the COP8 helps to eliminate register references, moving programming to a higher level. Because of the COP8's restricted RAM, you must minimize function-call depth and the number of local variables.—**Ray Weiss**

ByteCraft Ltd, 421 King St N, Waterloo, Ont, N2J 4E4, Canada. Phone (519) 888-6911. FAX (519) 746-6751. **Circle No. 398**

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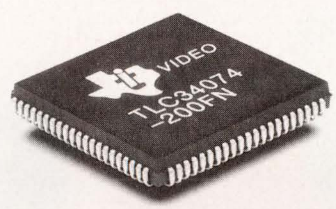

It's the first 200-MHz video interface optimized for X terminals, enabling 1600 x 1280 resolution at a 72-Hz refresh rate. And it's in distributor stocks now.

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TLC34074 — Designed specifically for B&W/grey-scale applications

Resolution	Refresh Rate	Price (1,000s)	Speed
1600 x 1280	@ 72 Hz	$34	200 MHz
1600 x 1280	@ 60 Hz	22	170 MHz
1280 x 1024	@ 72 Hz	12	135 MHz

TLC34076 — True color for X terminals, high-end PCs and workstations

Resolution	Refresh Rate	Price (1,000s)	Speed
1280 x 1024	@ 72 Hz	$45	135 MHz
1280 x 1024	@ 60 Hz	30	110 MHz
1024 x 768	@ 72 Hz	18	85 MHz

More advantages

- Both devices are compatible with virtually any video controller architecture: CISC and RISC microcontrollers, including TI's TMS340 graphics coprocessors, as well as hard-wired controllers.
- Handles Big- or Little-Endian formats with no hardware modifications.
- Direct interface to VRAM and controller.

For more information

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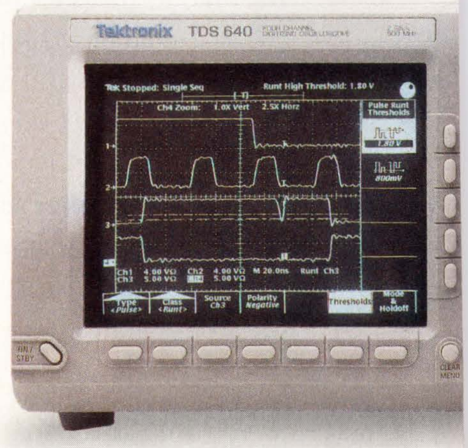
but also a perfect companion. The TDS 640 digitizing oscilloscope.



To get you started, the GPX provides more channels than cable TV. Up to 160, for instance, of 80 MHz state analysis, and 32 channels of 1 GHz timing or 160 channels of 200 MHz transitional timing.

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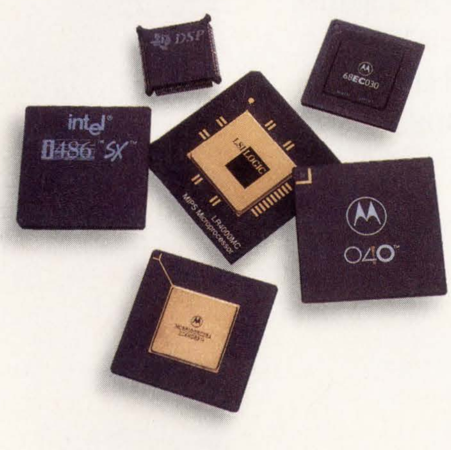

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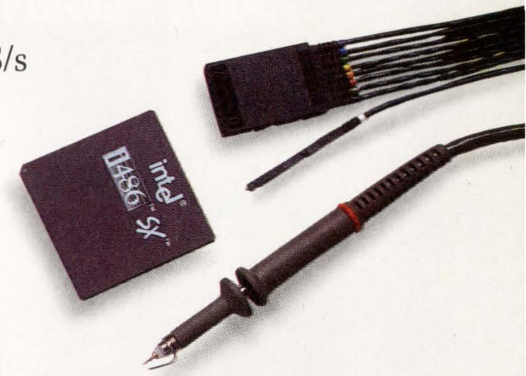

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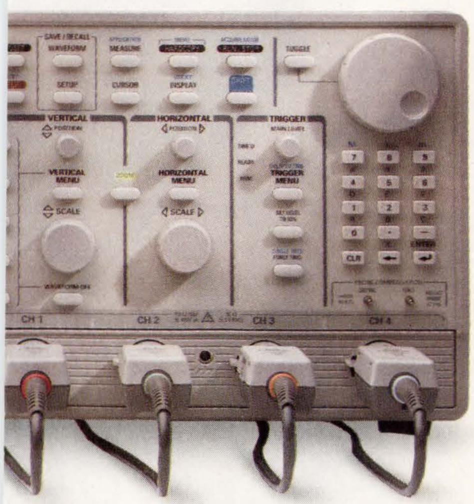

Cost effective, too. In fact, the GPX and TDS together sell for less than competing scope/logic analyzer combinations. And if you buy the pair between now and February 28, 1993, we'll take an additional 10% off the retail price.

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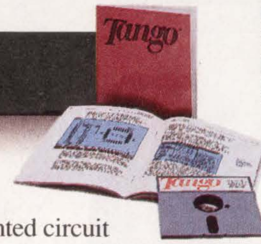

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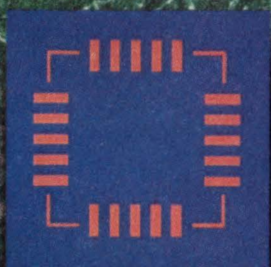

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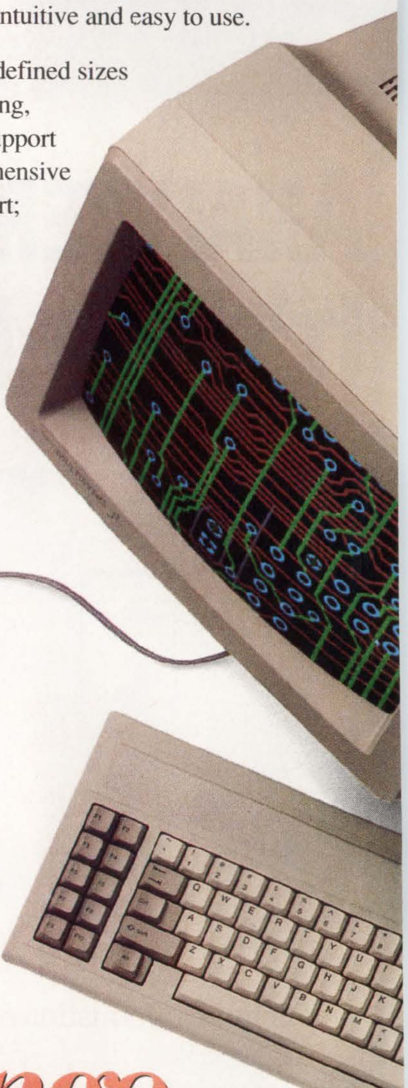

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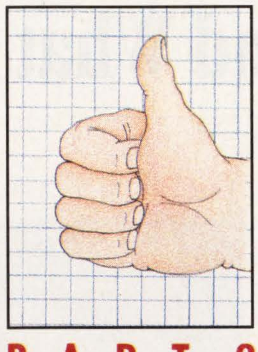


PART 2

A story of three computer products

Dan Strassberg, Senior Technical Editor

This second installment of EDN's Design It Right series on developing electronic products tells the stories of three computer-and-peripheral products. The Force CPU-2S is the first in a family of VMEbus boards, each of which provides the capabilities of a Sun Microsystems SPARCstation in a single-board plug-in format. The Quantum Go*Drive 2½-in. (diameter) hard-disk drives have helped to make notebook PCs a reality. The Tusk Supertablet is in the vanguard of what many observers think is a revolution—pen-based computing. In one of its many embodiments, this chameleon-like product is a pen PC.

Of these products, the CPU-2S and the Go*Drives come from established companies that have refined their methods of developing products over the course of several years. One reason that Force is noteworthy is the very strong influence of its quality organization. Quantum is worth learning about because it is in a business that lives or dies by time to volume deliveries. The firm has developed a successful 8-year relationship with a manufacturing partner in Japan. When Quantum needed to cut new-product development time drastically, the company recognized that it had to transform both its own culture and that of its partner. The transformation worked.

On the other hand, Tusk is a new company that has designed an unconventional product—perhaps a revolutionary one. The firm is concentrating on market research, product definition, design, and marketing. It won't be building the product itself, but will rely on contract assembly. Don't be fooled, though: Tusk isn't taking this approach out of naivete or a lack of manufacturing expertise. The firm's management team includes a seasoned operations executive with heavy experience in desktop-PC manufacturing. Like Quantum, Tusk is simply being pragmatic. By using contract assembly, the firm is delegating a task to those who can perform it best and is focusing its own resources where they can make a unique contribution.

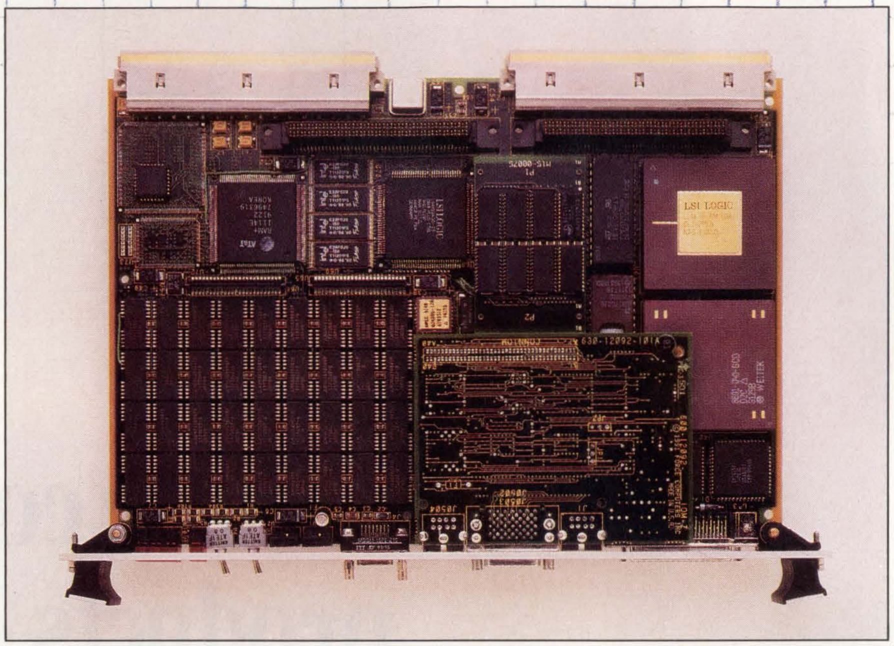
Illustrations by Daniel J Collins

Force Computers Inc—CPU-2S

How You Know And What You Know

At Force Computers, on almost any day, the burning question of the day is "How do you know?" The Quality Department asks that question relentlessly to promote a disciplined thinking style whose purpose is resolving problems while they are still minor . . . before they have a chance to grow into crises.

Force didn't invent the idea of repeatedly asking people how they know. The registrars who visit a company's facilities to provide certification of compliance to international quality standards such as ISO 9001 use the same technique. During certification, the registrars interview employees who perform a variety of jobs. Whenever an employee asserts that something is true, a registrar is likely to ask "How do you know?" Having achieved the correct mindset, Force is well on its way to obtaining certification under ISO 9001; the firm's German subsidiary has received it already.



You would expect a 6U VMEbus board that is the functional equivalent of a Sun SPARCstation to be dense. Force's CPU-2S is. However, the identically sized CPU-2E, which debuted a few months later, added still more capabilities and placed functions previously performed by a mezzanine board (at the left, just below the center) on the main board.

In the case of the CPU-2S, the technique worked—by minimizing the number of schedule slips caused by unplanned events. The entire project took just 15 months from inception to shipment. The $7995 (US base price) CPU-2S is in effect a Sun SPARCstation on a remarkably complex 14-layer 6U-size VMEbus pc board that contains a RISC µP, a high-performance numeric coprocessor, several custom VLSI ICs, and as much as 64M bytes of RAM. It is the first member of a family of three boards whose total sales are expected to exceed 10,000 units over four to five years.

Despite its complexity, and even though there had been neither a full breadboard nor a full simulation, the very first CPU-2S board came up and ran without any modifications. (Although the board didn't run at first, it would have, had it not been for a defective crystal. After two days of fruitless troubleshooting, a frustrated engineer bounced his screwdriver off the crystal can. *Then* the board began to work.)

Even though the prototype was a success, Force did make changes to improve manufacturability before putting the design into production. These changes were relatively minor, however, and from the time engineering finalized them, only 45 days elapsed until manufacturing declared the first lot complete. The 45-day interval represented a nearly ⅔ reduction from the time required on earlier Force products.

If you have inferred that Force's design process is organized and disciplined, you're right. Unlike many companies of its size (about 85 people work at the US headquarters; the German subsidiary employs perhaps half again as many), Force adheres to a formal product-development protocol. Of course, the existence of a script can't guarantee that everything always happens as planned. (The crystal problem is an example of something that didn't.) But when things go wrong, a disciplined, methodical problem-solving approach stands the best chance of producing a solution in a reasonable time.

One of the disciplines Force has developed—if not perfected—is sharing resources among projects. Sharing resources isn't something Force particularly likes to do; in an ideal world, a company could commit people to work exclusively on

Force's lessons cover issues from microscopic to global

In designing a complex pc board, pay attention to component placement. If you do, the rest will fall in place. Careful placement is the key to routing, manufacturability, and reliability.

Don't assume that, when you have selected a set of design tools, they will magically become useful right away.

Encourage the people who will use new tools to receive training, and allow time for them to train and come up to speed. Tools affect the way people do their jobs and the way an organization operates. If your expectations about how fast you will be able to integrate a new tool into your operation are set too high, the results may be chaos and missed deadlines.

Don't be satisfied with "good" results in manufacturing. Even when the results meet your expectations, strive for continued improvements. Chances are, if you ask "How do you know that you can't do better?" you won't get a good answer. At Force, this approach—the opposite of "If it ain't broke, don't fix it"—results in a continuous stream of process improvements that reduce rework and raise both quality and profitability. An example is an improved method of soldering through-hole mounted components on boards containing surface-mounted components on both sides. Such boards now go through the solder wave in a carrier that covers all of the solder-side surface-mounted parts.

Plan and execute a concurrent-engineering program. Concurrent engineering works! Not only will working simultaneously on design, manufacturing, and sales issues reduce the time from concept to delivery, the cross-pollination of ideas that naturally follows will improve the product. Because of contact with people from various disciplines, designers in a concurrent-engineering program get a better picture of what is required for the product to succeed. As a result, they incorporate features that improve the product's chances of success.

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a single project. In the real world, though, few companies can afford that luxury; some members of a project team will have responsibilities on more than one project.

Force recognizes that people don't multitask very well; someone working on a project 30% really works on the project 100% for some part of the time and 0% the rest of the time. For people, task switching takes time, and schedules must allow for such inefficiencies. When a team member works on several projects, a crisis on one will inevitably disrupt the schedules of the others. Effective resource sharing is another reason for companies to do their utmost to avoid crises, but even Force's disciplined approach can't guarantee that emergencies will never occur.

When you schedule a project that uses shared resources, you must assume that crises will arise on each project on which a shared person is working. Allow slack time in your schedule to cover temporary losses of shared people. If you get ahead of your schedule, don't relax or congratulate yourself; a crisis on one of the other projects could still set you back.

When you must share resources, communication becomes the key to setting and keeping realistic schedules. For this purpose, Force runs weekly concurrent-engineering meetings. At first, each project had its own meeting. Then the company tried a single meeting for all projects. The single meeting became too unwieldy, however, so project-oriented meetings resumed. These meetings have a rigid 1-hour time limit. A representative of the Quality Department attends; when a project is running smoothly, it is likely that team members' only contact with the quality group will occur at these weekly meetings.

A project's initial meeting establishes the input and output requirements for each contributing group. Each group determines what items or information it will need as inputs to produce a particular output. A group's input requirements become some other group's output requirements and give rise, in turn, to more input requirements. When all groups have established their input and output requirements, they can determine how much time they will need for each task. At this point, there is enough information to construct a schedule. Of course, constructing the schedule would be easier if no resources were shared, and staying on schedule would be a snap if crises never arose.

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Quantum Corp—The Go*Drive Series

Speeding R&D By Changing Corporate Cultures On Two Continents

This 2-platter, 160-Mbyte, 2½-in. hard-disk drive has twice the storage capacity of a 2-platter drive of the same size that the vendor, Quantum Corp, introduced just 10 months earlier.

Throughout the electronics industry in the '90s, reducing time to market is probably the single most important objective of R&D managers. And if there is one part of the industry that lives and dies by time to market, it's hard-disk drives. But as Larry Willson, Director of Development for Quantum Corp's 2½-in. products points out, in hard drives, although the time from the inception of a development project to the product announcement is very important (this is the period that most people think of as "time to market"), what is *really* crucial is the time to volume deliveries.

In the disk business, competition is so keen that missteps often prove fatal. The field is littered with the corpses of companies that announced products they hadn't learned to produce in volume and couldn't deliver reliably in quantity before competitors could. Naturally, an industry that emphasizes time to volume requires unusually close cooperation between design and manufacturing.

Quantum designs all of its drives at its Milpitas, CA headquarters and manufactures its high-capacity, high-performance workstation drives in the US. However, high-volume personal-computer products, including 2½-in. drives, are built by a Japanese partner, Matsushita Kotubuki Electronics Industries (MKE) in Ipponmatsu. The two firms have been working together for more than eight years.

Quantum long ago established an enviable reputation for product quality. When the company said it was ready to ship a product in volume, it really was able to do so, and the product performed as advertised. Quantum's problem had been that it usually wasn't ready to accept volume orders until its competitors had locked in the juiciest OEM contracts. To survive, the firm had to change its culture; it had to learn how to shorten development cycles without sacrificing its vaunted quality. But because of Quantum's reliance on a Japanese manufacturing partner, changing Quantum's culture involved changing the culture of *two* corporations operating in two very different societies six thousand miles apart.

The solution was an approach that Quantum calls fast cycle time or FCT. One element of FCT is what Quantum calls the "bump" environment. The company locates all team members close enough to each other that in doing their jobs they almost literally bump into one another. These informal contacts lead to exchanges of information that otherwise might remain privy to only a few team members. For products that will be produced in Japan, MKE representatives are part of the bump groups.

Another element of FCT that began as an experiment and has since become a way of life is called the "messy" meeting. These meetings, which occur early in a program, give every affected group an opportunity to challenge the program's rationale and fundamental approaches. (See the editor's analysis box on pg 664 of the October 1, 1992 issue of EDN.) The meetings last about three hours; as many as 35 people attend, and anybody can speak. Nowadays, a somewhat shorter follow-up meeting often occurs two to three weeks later. Here, team members answer questions that they couldn't answer adequately at the initial meeting.

The first product on which Quantum tried FCT was the Go*Drive 40/80 duo, the first members of what is now a 6-member family of 2½-in. drives for laptop and notebook PCs. Besides the original pair, the family now includes the Go*Drive 60/120 and the Go*Drive GRS 80/160. As you've probably discerned, the numbers at the end of the model designation are the drives' approximate formatted capacities in Mbytes. In each model pair, the first unit has a single platter and the second has two. Thanks to technology improvements during the 10 months between the introduction of the first and third drive pairs, the latest 1-platter unit boasts almost the same capacity as did the original 2-platter model.

Over the production life of the family, the firm expects to ship approximately 1.5 million units. Current estimated street prices (single-piece quantity) with a 16-bit ISA bus integrated-drive-electronics (IDE) interface are around $220 for 40 Mbytes, $260 for 60 Mbytes, and $300 to $330 for 80 Mbytes. Units with a SCSI interface sell for about $10 more.

According to Quantum, the Go*Drive family was the industry's first series of 2½-in. drives. Developing the first two drives took 17

Keep goals clear but leave room for trial and error

Get all groups that have a stake in your product to buy off on, or agree to, the spec; then freeze the spec. Some of the biggest delays in R&D programs occur when companies fail to make decisions. Delays also result from specs that are not well thought out or are too flexible. If you can get the affected groups to really consider your spec's implications and voice their concerns early (as Quantum does at its "messy" meetings), you will reduce the likelihood of falling into these traps.

Integrate design and manufacturing activities. Not only should the work go on concurrently, the people must feel like a team. One of Quantum's devices for achieving teamwork is the "bump" environment (see story).

Don't forget that key customers and vendors are part of your team. Two groups from outside your company must become part of your team: key customers and key vendors. Maintain open relations with these groups. An open atmosphere is your best defense against unpleasant surprises.

Keep the invention of new technology off the critical path. Quantum achieves this objective by maintaining advanced development groups for recording technology and process engineering.

Transfer learning from project to project. Establish a formal process for assuring that key lessons—both technological and procedural—are transferred from one project to the next. At Quantum, a product steering committee is responsible for communicating these lessons.

Use a "try-it, fix-it" approach. Do lots of simulations; build lots of prototypes; don't be afraid to make lots of mistakes. Mistakes that occur at the prototype stage, although disappointing, are much less costly than ones that you find out about only when you're in production.

Don't scrimp on development costs. A few dollars spent on keeping the program on schedule are minuscule compared with the costs of missing the market. For example, Quantum found it worthwhile to buy a large-format copier to duplicate the large PERT charts the Go*Drive team produced each week. Without it, team members had to tape multiple sheets together. They found it easier not to bother, but without charts they could read, they also missed deadlines.

Don't try to do what others can do better. Quantum's experience with attempting to design tooling for MKE (see story) is a good example of what happens when you waste effort on activities that others are better qualified for. You fall into similar traps when you fail to take advantage of vendors' expertise.

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months. These products included so many novel elements that the company classified them as revolutionary, even though no advance, by itself, represented a revolutionary improvement over existing practices. Whereas the 17-month cycle marked a dramatic reduction from earlier programs that Quantum had classified as revolutionary, the less extensive program to develop the 60 and 120-Mbyte models, also conducted using FCT, took just six months. Bringing out the single-platter 80-Mbyte unit and its 2-platter 160-Mbyte counterpart required a mere four months.

Six thousand miles from home

The MKE engineers who become part of bump groups are not the only ones who cross the Pacific during Quantum development programs; engineers from Milpitas spend many weeks at MKE. To prepare for trans-Pacific assignments, people from each company receive training in the other country's language and customs. During the away-from-home assignments, the guests develop lasting friendships with their hosts. As the two companies continue to work together, these friendships are certain to improve cooperation even further.

In the area of manufacturability, Quantum personnel have learned not to second guess their MKE counterparts. Early attempts in Milpitas to develop production tooling for the Go*Drive family yielded fixtures that MKE couldn't use; MKE had to replace the fixtures with units of its own design.

MKE's interest in optimizing the production process extends beyond tooling. MKE engineers aren't shy about telling Quantum when elements of a design should be altered to simplify manufacturing. Quantum has found that the MKE people research the suggested changes meticulously and propose most of them before volume production begins, avoiding the cost of making running changes. The modifications are nearly always practical and usually improve quality as they reduce cost. The result is that everybody wins: MKE and Quantum share in the savings; Quantum's customers benefit from improved reliability.

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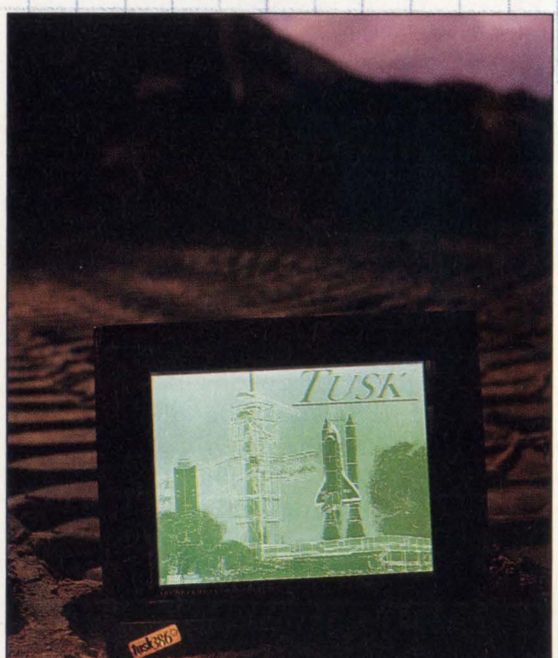
Tusk Inc—Supertablet PC

Don't try to be all things to all people

Reading about its features and specs may make you lust after the Tusk Supertablet PC. But at a price of over $5000, the machine costs considerably more than laptop or notebook PCs. So, despite its dazzling list of features, it isn't a computer for all seasons, and Tusk is taking great care not to represent it or sell it as such. The company doesn't even plan to release the unit to the retail channel through which most general-purpose PCs are sold. Rather, the firm is targeting the Supertablet at a host of special applications where, despite its price, it will be an economical solution or the *only* practical solution.

Defining what the Supertablet is—and isn't—is a challenge, because the machine can be so many



What looks straightforward enough often is anything but. The Supertablet's chameleon-like ability to adapt to the needs of specific applications might make you think that its designers wanted to please everyone. But at over $5000, the unit is not priced like a general-purpose PC, and Tusk has no intention of trying to sell it to a mass market.

things. It can be a pen-based PC—but it doesn't have to be. It can be a portable high-resolution monochrome-graphics workstation with a 1280×1024-pixel, 11-in.-diagonal, 64-shade, paper-white display—but it doesn't have to be; it will also be available with a monochrome LCD having the standard 640×480-pixel VGA resolution. (The 1280×1024-pixel version provides a built-in double-scan VGA capability, so applications that don't support 1280×1024 pixels can provide near-full-screen displays.) The computer can also be very light—but it isn't always. There really is no standard model.

The heart of the Supertablet is a <6-lb (with VGA-resolution LCD) pen-based PC that has a 25-MHz i386SL μP, fast local-bus video, support for simultaneous displays on the LCD and an external CRT, a math-coprocessor socket, an internal 2400-bps data/9600-bps FAX modem (9600-bps data/FAX modem optional), 8 Mbytes of RAM (expandable to 20 Mbytes), an 85-, or 190-Mbyte hard disk, and batteries that provide 4 hours of operation without invoking any of the power-conserving features. The tablet includes standard connectors, for example for the RS-232C and printer ports and the modem's telephone connection. For protection from the environment, these connectors are covered.

Oil wells to PCs

Bill Hart, one of Tusk's two founders and the person behind the technical aspects of the Supertablet, is an ME, not an EE. His background is in instruments for oil-well surveying. Oil fields are far from the most hospitable environment for electronic equipment, and Hart carried the lessons he learned in packaging well-survey equipment into the Supertablet design. The tablet is extremely rugged. According to Hart, a 200-lb man can stand on it without damaging it. The hard disk is cushioned in material that, on impact, absorbs energy by changing from solid to liquid form and then reverting to the solid state. The tablet, though sealed against moisture, is totally convection cooled.

As were so many other decisions in the tablet's design, the choice of a pen technology was governed by environmental factors. According to Hart, the electromagnetic technology that Tusk chose is the only one that allows an operator to wipe off a glob of mud that might fall onto the screen and go right on using the pen and PC as if nothing had happened. The pen requires no tether (no cable to connect it to the PC), though Tusk will provide passive tethers to keep pens from getting lost.

A key feature that the firm in-

Changing markets require PC designers to react fast

Involve the mechanical and electrical architects in the market research. Through focus groups and in-depth interviews with representatives of targeted groups of users, Tusk conducted extensive market research. However, the firm was half way through the definition process before the design team conducted its first concept review. Although the team members were never confused about the fact that they were developing a rugged computer, users' specific ruggedness requirements caused some rethinking of approaches the team had already decided on. In retrospect, had the team known about the customer requirements sooner, the tablet's development costs would have been somewhat lower.

Don't attempt to use outside vendors for leading-edge technologies. Tusk had little success with such attempts. In one case, Tusk engaged a BIOS house to extend the firmware to handle the pen and i386SL power-management functions. However, the BIOS firm was so involved in support for core i386SL functions, that to stay on schedule, Tusk had to bring the BIOS development in house.

Once you have defined the product's feature set, limit changes to those necessary to meet manufacturing requirements.

But don't be inflexible in applying the preceding rule. Tusk based the Supertablet's original release date on the projected availability of pen-based operating systems. When the operating-system release dates slipped—not altogether unexpectedly—the computer's release date slipped too. When the release date slipped, Tusk had to revisit the feature set, because the hardware technology continued to evolve. Holding the feature set constant would have resulted in a design that had less than the 18 months of sales life the firm had been counting on to recoup its investment.

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cluded to enhance serviceability is a provision for remote fault diagnosis via modem. The machine need only function minimally to permit use of this feature. The computer also allows for multiple versions of the BIOS (basic input/output system). One version is in read-only memory (ROM), as is customary in PCs, but the unit also incorporates flash electrically programmable memory chips that can contain alternate versions. This feature will permit BIOS changes that are sometimes necessary for compatibility with new or upgraded operating systems.

The multiple-BIOS capability is just one of many features that are both elegant and utilitarian. Included in the tablet is an unusual, environmentally protected, 200-contact, zero-insertion-force (ZIF) connector whose expected life exceeds 10,000 insertion/withdrawal cycles. The connector, which carries the complete ISA (industry-standard architecture) bus as well as other signals, can link the unit to a docking station. One such station includes a full PC keyboard (not just a keyboard port) and a floppy-disk drive, but little else. Docking the tablet requires merely dropping it into a slot and tilting it back a few degrees. Alignment between the connector's mating halves is automatic.

No clamshell

When you place the tablet in the docking station, you have a lightweight (roughly 10-lb) desktop or laptop PC. To carry this unit around, you don't fold it up clamshell style as you would most laptops; you remove the tablet and place it face down atop the keyboard. Then you place the two stacked objects in a portfolio that also accommodates the battery's quick charger. The complete package with the portfolio weighs roughly 12 or 13 lbs. Although that weight sounds high for a laptop PC in 1992, it is not high for a portable high-resolution graphics workstation.

The docking station replicates all of the tablet's standard I/O connectors, so you can connect external peripherals to the tablet via the station. You can also remove the tablet from the station without disconnecting the peripherals. But because the connectors on the tablet and on the station are identical, you can reconnect the peripherals directly to the tablet.

Many Supertablet users will never see the docking station or the portfolio, however. Thanks to features designed into the tablet, users with no keyboard will easily be able to run applications that depend on text entry. Several other pen computers require software that uses part of the screen to emulate a QWERTY keyboard; such software can conflict with the applications. On the Supertablet, around the periphery of the screen, etched into the protective glass are alphanumeric "keys" that you "press" by tapping the pen against them. The PC's special BIOS recognizes such "key presses" just as if they came from the docking station's keyboard.

By making the use of the docking

EDITOR'S ANALYSIS

A cynical view of early manufacturing involvement

A very high percentage of the companies mentioned in this series suggested among their do's and dont's that you should get manufacturing involved early in the design process; most suggest manufacturing involvement from the very beginning. As one who has worked in both design and manufacturing, I have a slightly jaundiced view of involving manufacturing in design.

I spent over 20 years in design and three years in manufacturing and test engineering, and it seems to me that design engineers' interest in having manufacturing participate in design often has little to do with hearing another group's ideas. Rather, designers espouse manufacturing involvement for defensive reasons: When production or test problems crop up, the designers can say "Well, the problems aren't my fault; there was a manufacturing person on the project team and he (she) endorsed the design."

Too many design engineers are used to treating manufacturing people as if they were second-class citizens, and too many manufacturing people stand in awe of designers. Too many design engineers are convinced that if only manufacturing people were a little smarter . . . if they had just one tenth of the brain power of designers, all of manufacturing's problems would go away.

I suggest that these designers walk a mile or two in a manufacturing engineer's shoes. And I suggest to managers that they examine their company's culture. Companies that send a message that design engineers are first class but manufacturing engineers aren't encourage the design of products that will be troublesome to manufacture. You can send messages about the value of different jobs in a variety of ways—through pay scales, through stock options, through perks such as office size . . . even through things like which department has a rug on the floor and which doesn't.

I submit that the problem begins long before most engineers collect a paycheck. Veneration of design and denigration of manufacturing begin in college. Most EE faculty members have never held jobs outside of academia.

station optional for text entry, the tablet's designers have freed up the ZIF connector for attaching accessories. In most cases, accessory units will come not from Tusk but from vendors who will resell the Supertablet into specialized markets.

This is a hard-hat job

One attachment is a receiver that picks up signals from GPS (Global Positioning System) satellites orbiting the earth. Envision this: A worker for a utility—a telephone or electric company—carries a receiver-equipped tablet. The tablet's screen displays a map of the worker's surroundings; the area shown changes as the worker moves about. Overlaid on the map are the locations and identifying codes of facilities (poles, transformers, and conduits, for example). The tablet's hard disk stores the maps.

The worker drives to a job site in a truck, alights from the truck to perform repairs or tests, and, while out of the truck, uses the pen and tablet to enter data about the operations performed. Upon returning to the truck, the worker detaches the receiver from the tablet and slips the tablet into a specialized docking station on the truck's dashboard. (Like the receiver, this station is not a Tusk product.) The docking station is linked to a transmitter in the truck, which sends the newly entered data to a central computer containing the master facilities database. The computer then automatically broadcasts database updates to the tablets carried by the utility's other workers.

Although this example might sound fanciful, it's real. The technology will be available by the time you read this; Tusk expects to ship its first Supertablets to customers in early October. All manufacturing will be done by an independent contract-assembly firm, hence the design will either be producible at the outset or it will very quickly become so. When a product's designers and manufacturer have this kind of arms'-length relationship, design problems that might otherwise linger beneath the surface tend to receive quick attention. Moreover, Tusk doesn't lack for in-house manufacturing expertise. Its operations group is headed by an executive who directed desktop-PC manufacturing at IBM Corp's Boca Raton (FL) facility.

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They pass on to their students a disdain for "industry." But they pass on far less disdain for design than for manufacturing. One possible solution is offering EE faculty summer jobs in manufacturing companies—not in design departments but in manufacturing.

If America is to regain the status of a world leader in high technology, it *must* put its manufacturing house in order. It *must* find ways of competing with low-cost producers, even ones in third-world countries. Only through adding value can you create real wealth. Manufacturing—mass production—is how you add value on a massive scale. When a society holds the activity that creates its wealth in low esteem, it has little chance of becoming wealthier; in fact, it has a good chance of becoming a lot poorer.

Now, return from this global view of the problem to a facet that you can control: Making *your* product more manufacturable requires more than paying lip service to manufacturing involvement in the design process. Create an atmosphere in which manufacturing people are not afraid to express their ideas. Listen when they talk. Incorporate manufacturing suggestions into your designs. These steps may seem like small ones, but their potential impact is profound; you can even view them as the beginning of a new American industrial revolution.

Next in Design It Right . . .

Part III of Design It Right, which will appear in the October 29, 1992 issue of *EDN*, will cover leverage, or how to get the biggest bang for your R&D bucks. In it, you'll discover how one company replaced a proprietary μP board in a high-performance instrument with an 80X86 mother board and standard PC peripherals. The approach brought with it some unexpected responsibilities for the designers. You'll also read how a new company found that its suppliers were as interested in its success as its own employees. As a result, the suppliers became, in effect, members of the design team. Finally, you'll learn about a company's experiences in designing a product around the VXI modular-instrument standard.

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DPS MODEL TABLE

	d-c OUTPUT HIGH RANGE		d-c OUTPUT LOW RANGE		RESOLUTION	
MODEL	VOLTS	AMPERES	VOLTS	AMPERES	VOLTAGE	CURRENT
DPS 12.5-6M	0-12.5	0-6	0-6	0-8	0.05V	0.04A
DPS 25-3M	0-25	0-3	0-9	0-5	0.1V	0.02A
DPS 40-2M	0-40	0-2	0-15	0-3	0.2V	0.02A
DPS 125-0.5M	0-125	0-0.5	0-60	0-1	0.5V	0.004A

DPS GENERAL SPECIFICATIONS

SPECIFICATION	CONDITION	RATING DESCRIPTION
INPUT		
a-c Voltage	User selectable	115/230 Va-c ± 10%
Current	Max load 115Va-c	1.4A
Fuse	115Va-c	3A
	230Va-c	2A
Frequency	Range	50-60Hz
OUTPUT		
d-c output	Microprocessor controlled	Linear, series-pass
Type of stabilizer	—	Voltage
Voltage	0 to 40°C	0-100% rating in two ranges
Current	CCP	Current limit mode
	OCP	Over current protection disables output
	Short circuit protect	Disables output after 10 seconds
Error sense	Drop	0.25V per lead
Isolation voltage	Output to ground	400 Vd-c or peak
Leakage current	rms at 110Va-c	50 microamperes
Output to ground	p-p at 110 Va-c	0.5 milliamperes
Series connection	Max voltage off gnd	400V
Parallel connection	—	NA
OVP	Control limit	Voltage stop
CONTROL		
Type	Local	Keypad
	Remote	RS232C
Dynamics (Resistive load)	Rise time	<16 msec
	Fall time	<75 msec
Isolation	Control-output	Optical
Range	Current capacity	Automatic
Memory	Store settings	3 volatile locations
MECHANICAL		
Input connection	Detachable line cord	IEC type
Output connections	Front	Binding posts
Meters	Two LED	Three digit
Indicators	LED	Remote
		Talk
		Listen
		OPE (output enable)
		OCP CCP
Mounting	19" rack	RA 56
Cooling	—	Convection
Dimensions	Outside HxWxD	4.5"x13.1"x8.5"
Panel finish	Fed Std 595	Color 26440, Gray
Weight	Packed for shipment	14.5lb/6.6Kg
	NET	13lb/5.9Kg

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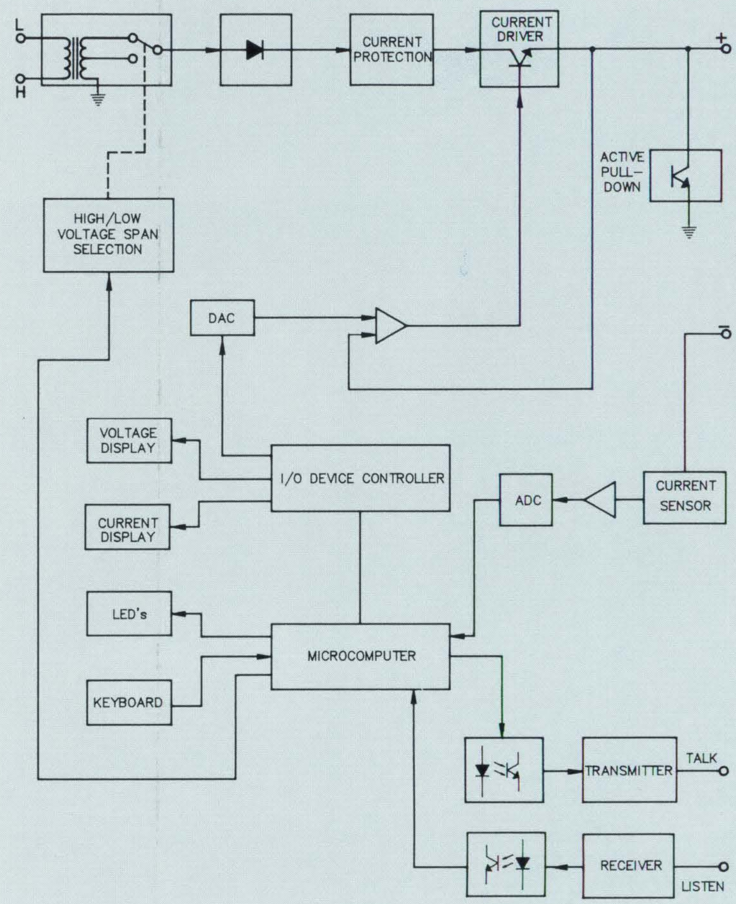
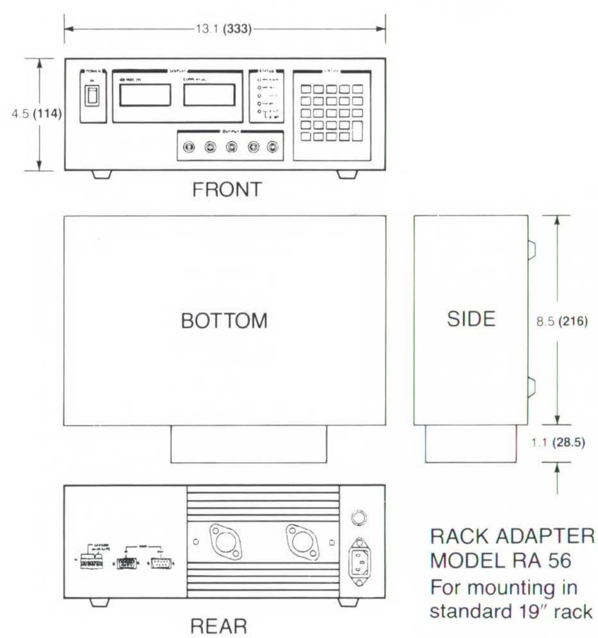


DIMENSIONS

Dimensions in light face type are in inches,
dimensions in bold face type are in millimeters.



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Power-management ICs secure your portable application between battery charges, letting you keep a firm grip on your data. (Photo courtesy Cirrus Logic Inc)

POWER MANAGEMENT

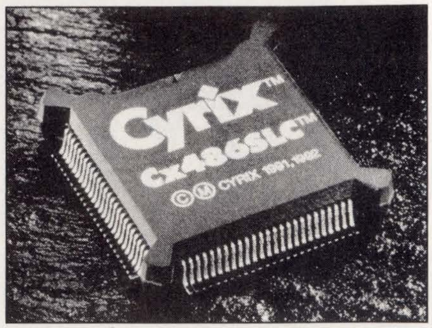
Today, no respectable business traveler leaves home without a portable computer. This boom has spurred the development of power-management products that ensure these computers have enough juice between battery charges.

John Gallant, Technical Editor

In recent years, the portable computer has spawned an outbreak of innovations to conserve battery power. When portable computers were in their infancy in the late 1980s, computer vendors generally used an all-CMOS design surrounding a 16-MHz 386SX µP to extend battery life. Although an all-CMOS design can conserve power in low-frequency applications, higher-performance CPUs warrant more power-saving features to achieve useful battery life between charges. These power-saving features are revolutionizing the design of mobile computers ranging from laptops and notebooks to check-book-sized palm tops. The obvious way to conserve power in a CMOS design is to use a low clock rate whenever possible. Because CMOS drivers consume power only during clock transitions,

fewer transitions are less power consuming than many transitions. In fact, CMOS drivers display linear power dissipation vs the clock frequency. However, to achieve the maximum performance of the computer, you need to run the clock at the maximum CPU speed. Therefore, to manage the power consumption in high-performance portable computers, vendors use techniques to lower the frequency or even shut off the clock to portions of the computer that aren't currently in use. In essence, vendors manage power consumption by minimizing the duty cycle of the system clock rate relative to the maximum CPU clock rate. An effective power-management policy also removes the power to any device not in use.

To achieve effective power management, CPU vendors and third-party IC and software vendors have worked closely to integrate specific power-management features in products intended for mobile use. One of the innovations in CPUs is Intel's i386SL Superset. In 1990, Intel introduced the SL Superset,



The Cyrix Cx486SLC µP runs i486 object code, features a CPU suspend mode, and has the same package size and pin assignments as the i386SX µP.

which consists of an i386SL CPU ($122 (1000) for a 25-MHz version) and an 82360SL ($32 (1000)) peripheral controller. The i386SL CPU contains a 16-, 20-, or 25-MHz 386 µP core that has the same page-management memory system as a standard i386 µP. In addition, on-chip hardware implements an expanded memory system that is compatible with the LIM 4.0 standard.

A super chip manages all

The 82360SL contains many of the I/O peripheral features found in core logic. These features include serial ports, parallel ports, timers, interrupt handlers, and DMA controllers. The chip also has keyboard, floppy-disk drive, and IDE-disk drive control features. The chip generates dynamic RAM (DRAM) refresh signals and has a low-power timer to refresh low-power DRAMs. A system-management mode (SMM) is the main feature of the SL Superset to conserve power. The SMM lets you write software to monitor and control system power transparent to normal operations. The ingredients that let you implement SMM are a system-management interrupt (SMI), a system-management RAM (SM-RAM), and an I/O port called Ideaport.

The 82360SL generates the SMI in response to system interrupts that monitor system activity and battery status. The SMI connects directly to the CPU and is similar to a nonmaskable interrupt (NMI), which is unaffected by the interrupt-enable bit in the CPU's flag register. The SMI has a higher priority than the NMI, however. The SM-RAM consists of a separate 64 kbytes of memory space that the CPU switches into locations 030000H through 03FFFFH when the CPU recognizes an SMI. The CPU hides the main memory normally located in this space. The CPU saves its contents to the SM-RAM area and switches to real mode for execution of the SMI handler code at the absolute 038000H address. You can implement handler code to independently control the speed or stop the CPU, math coprocessor, DMA, or keyboard clocks.

The SL Superset has 13 power-management timers to keep track of external-device idle times. The Ideaport can control power to as many as six external devices. The SMI handler, resident in the 82360SL, monitors and interprets system events to provide three different power-management states—

Maximizer (tm) 386SL—Power Management
Copyright (c) SystemSoft Corporation 1990-1992. Version x.x

Power Management:	[On]	CPU Standby:	[12 Secs]
Warning Beeps:	[Enable]	Global Standby:	[2 Mins]
Battery Low Suspend:	[Enable]	Auto Suspend:	[4 Mins]
Any Key Resume:	[Disable]	On/Off Button:	[On/Off]
Modem Ring Resume:	[Disable]	Alarm Resume:	[Disable]
0-Volt Disk Suspend:	[0-Volt]	To 0-Volt Suspend:	[120 Mins]

Device Controls		Device Status
Panel Backlight:	[1 Mins]	On
Fixed Disk:	<Disabled>	
Diskette Drive:	[Automatic]	On
Parallel Port:	[6 Mins]	On
Com A Device:	[2 Mins]	On
Com B Device:	[4 Mins]	On

Arrows—Move	F2 Standby Now	F5 Previous	F8 Suspend Now
F1 Help	F3 Power Switch	F6-Next	F9 Auto Config
Esc Exit			F10 Save & Exit

This simulated screen presentation of Systemsoft's Maximizer software demonstrates its flexibility. The menu lets you interactively establish the time-outs for system power-management modes, control individual components, and select hot keys.

local standby, global standby, and suspend. In local standby, when a device is idle for a programmed count, the handler shuts off power to the device. Power turns back on when something accesses the device. A global-standby mode stops the CPU clock. In addition, in global standby you might typically power-down all six external devices, slow the keyboard and math-coprocessor clocks, and stop the DMA clock. In a suspend mode, the handler powers-down the system and all SL Superset parts except a resume-state machine and a slow refresh clock to refresh the DRAMs. In suspend mode, the resume-state machine can recognize an external event to resume operations from where an application left off.

The key to implementing Intel's power-management mode is the addition of the SMI line to the chip set, which lets a protected memory space (SM-RAM) save the CPU's status-register contents. However, in Intel's product, you must use the 82360 SL peripheral controller to generate the SMI signal. For notebook designers that committed early to the i386SX μP, switching to the SL Superset means creating a new mother-board layout. But Intel has competition from Advanced Micro Devices (AMD) and Cyrix these days for x86-type μPs.

In March 1992, Cyrix announced the Cx486SLC ($119 (1000)) μP, which contains a static CMOS core that runs i486 object code. The chip operates from 3.3V and runs at 25 MHz (see **box**, "The 3V revolution"). Because the chip maintains the same package size and pin assignment as the i386SX μP you don't have to make major changes to the mother board to upgrade. A 1-kbyte on-chip cache RAM conserves power by reducing the number of reads and writes to system memory. Fewer accesses increases the time the system memory is in standby. You can suspend operations of the μP via a suspend-request pin. A suspend-acknowledge pin indicates the μP is inactive and in suspended mode.

AMD's static CMOS Am386-SXLV ($43 (1000)) μP offers an SMI line similar to Intel's SL Superset that is accessible to any external core-logic device. The Am386SXLV also maintains the same package size and pin configuration as the i386SX μP. In addition, the Am386SXLV, which was announced in October 1991, operates as fast as 25 MHz from a 3.3V power supply. In contrast, the 3.3V version of Intel's 386SL ($78 (1000))

The 3V revolution

A quiet revolution is going on. In the 1960s, when TTL became the logic family of choice, a 5V supply was chosen to provide adequate noise immunity. TTL's totem-pole output configuration produces a typical 3V-logic high-output level, which provides a 0.6V margin above the typical V_{OH} threshold of 2.4V. However, the advent of CMOS in the 1970s created a logic configuration having an output swing to the supply rail. Although the supply rail has remained at 5V for many years to maintain TTL-to-CMOS logic compatibility, a 5V rail is unnecessary and in many respects remains as 1960s hangover.

Because the CMOS output can swing to the rail, a 3V supply in an all-CMOS design provides the same noise margin as TTL. A change to a 3V rail provides a couple of benefits. One benefit is power savings. Joule's law ($P=V^2/R$) states that the power consumption is proportional to V^2. Therefore, a simple change from a 5V supply to a 3V supply reaps a power savings of $3^2/5^2=0.36$, or 36% less current drain from the power supply.

In addition, a lower supply rail permits device designs using smaller geometries. The relentless drive to integrate more performance and higher speed into CPUs is forcing vendors to use component geometries less than 0.8 μm. However, geometries of 0.5 and 0.6 μm exhibit reliability problems due to gate-oxide breakdown and hot electron effects when using a 5V supply rail. A 3V supply rail reduces the failure mechanisms to acceptable reliability figures.

Although JEDEC defined a low-voltage 3.3V standard for TTL devices in 1984, the emphasis on low-power portable-computer design in the 1990s is providing the impetus to change from a 5 to a 3.3V standard. The current JEDEC standard has a ±10% tolerance, which permits operation from 3 to 3.6V.

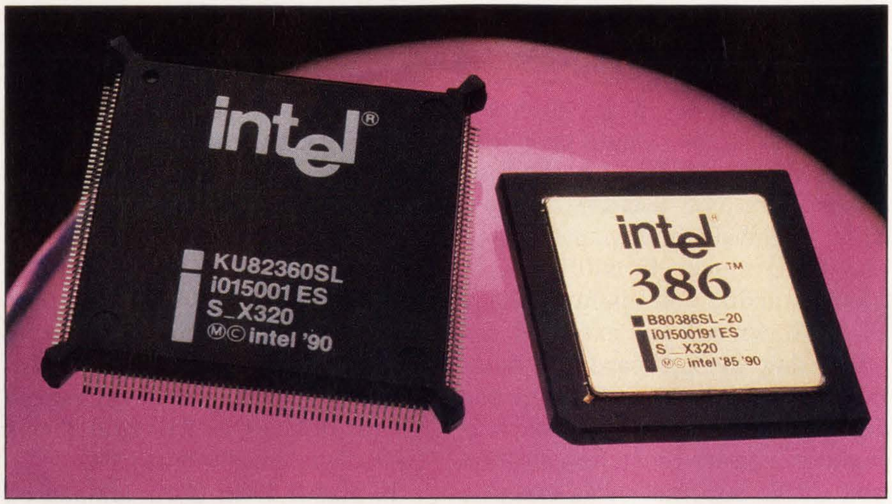
Pundits predict that by 1995 there will be a complete switch over to 3V devices. But in the interim, portable-computer designers must deal with systems that have a mixture of 5 and 3V components. Currently 3V CPUs, memory, core logic, and video controllers are available. But other portable peripherals, such as PCMCIA controllers, ISAbus expansion slots, and floppy- and hard-disk-drive controllers still require a 5V supply.

To prevent a 5V output from overdriving a 3V input system, designers may opt for both a 3V and a 5V local bus on the mother board. The buses communicate via 3-to-5V translators. Some vendors provide the level translators on chip so that the core runs at 3.3V and the peripheral I/O drivers run at either 3.3 or 5V selectable by the system designer.

chip, which was announced in June 1992, operates at 20 MHz. AMD also offers a 25-MHz Am386DXLV ($61 (1000)) low-power μP that operates from 3.3V and has an SMI interface.

AMD has formed an alliance, called FusionPC, with a number of core logic and BIOS vendors to guarantee that their low-power μPs interoperate with peripheral components. As a consequence, you can choose how to implement the power-management features. For example, Headland Technology's HT25 ($37.55 (1000)) core-logic chip connects directly to the SMI line on the Am386SXLV and Am386-DXLV μPs. The HT25 performs the peripheral-support functions on a single chip and operates at 25 MHz from a 3V supply. The HT25 generates the SMI when one of its 44 activity monitors detects device-idle time. The chip can control or stop the CPU and math-coprocessor clock speeds and supports slow-refresh and self-refresh DRAMs during suspend mode.

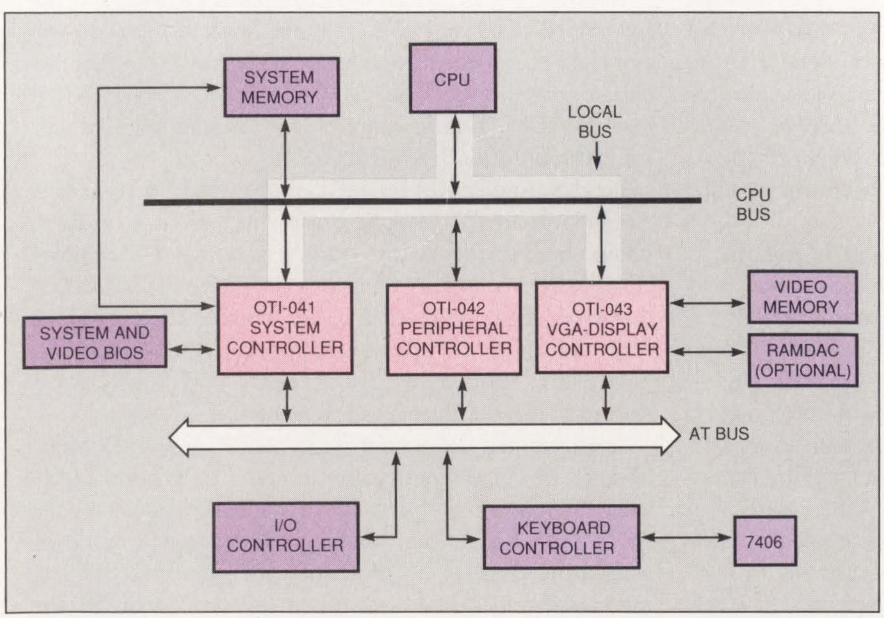
To effectively manage the system power, all of the computer subsystems must have power-management capabilities. For example, a system might use a Motorola 68HC05G8 ($16 (1000)) or a Signetics 87C752 ($7.50 (10,000)) μC that contains A/D converters to monitor battery conditions via an external resistor divider. When the battery weakens, the μC generates a battery-low or a battery-dead indication for an activity monitor. In addition, these μCs have timers and counters that can monitor device activity on chip. The biggest current drain in portable computers is the video subsystem, primarily the backlight for the LCD screen. To ensure maximum battery life, an LCD controller must provide flexible options to minimize power consumption when the LCD is not in use.



Intel's 2-chip implements the company's system-management mode. The 82360SL I/O subsystem chip generates the system-management interrupt for the i386SL μP.

Cirrus Logic's CL-GD6412 ($65) LCD VGA-controller chip features standby, suspend, and shutdown modes. Cirrus defines its standby and suspend modes differently from Intel. In standby mode, the chip suspends power to the LCD, but all other functions continue. In suspend mode, the chip suspends all video-subsystem operations except maintenance of the operating state and video-RAM contents. In shutdown mode, the chip stores the operating state and video-RAM contents to the hard disk before removing power from the entire video subsystem. In addition, when driving a dual-scan panel, the CL-GD6412 achieves the required panel-refresh rate using one half the normal-dot clock rate. The lower-dot clock rate proportionally reduces the video-subsystem power. The chip operates from either 3 or 5V supplies.

SMOS Systems's SPC8107 ($18 (1000)) LCD VGA controller operates from 3V and features four soft-



Headland's HT25 core-logic chip generates a system-interrupt signal to manage the power consumption of AMD's AM386SXLV and Cyrix Cx486SLC μPs. The chip operates only from 3V and requires external translators to drive 5V devices.

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ware- and one hardware-controlled power-saving modes. In all of the power-saving modes, the controller disables the LCD screen. In software mode 1, the CPU can read and write to the video RAM. Software mode 2 prevents CPU access to the video RAM. Modes 1 and 2 refresh video memory at 64 or 8 kHz. Software mode 3 is similar to software mode 2 but also disables memory refresh and optionally disables the clock oscillator. Software mode 4 is similar to software mode 2 but uses self-refresh DRAMs to maintain the video-RAM contents. In the hardware mode, called suspend mode, the CPU can't access the video RAM, and the controller provides the control for self-refresh DRAMs, disables the clock oscillator, and deactivates all CPU interface signals.

The power-saving modes of LCD VGA controllers represent typical subsystem options designers have for conserving power in portable computers. With so many options available, it isn't surprising that portable-computer designers rely on BIOS vendors to supply power-management firmware in ROM that coordinates the system's power-down modes. One such BIOS vendor is Phoenix Technologies Ltd. Phoenix offers the Phoenixmiser, which operates with the PhoenixBIOS 386SL to administer all of the power-management features of Intel's SL Superset under Microsoft's Windows. Because Phoenixmiser and the PhoenixBIOS 386SL offer numerous custom options, the product cost is negotiable for OEM vendors.

The Phoenixmiser manages five system states. The on state runs the system at the specified setup speed with all devices at full power. A component power-management control state controls power to individual devices, such as the LCD panel, backlight, hard-disk drive, and parallel and serial ports. An idle state turns off the power between individual keystrokes and the CPU, floating-point unit, and keyboard controller. A standby state turns off the display and the hard- and floppy-disk drives, and saves the status in system memory. The standby state places the system memory into slow-refresh mode and cuts the keyboard clock in half. The suspend state stores all system status to the hard disk and removes power from the system. Upon resume, the system reads the status from disk to return to the same point in the application.

Systemsoft is another software vendor that offers power-management firmware along with a system BIOS in ROM for Intel's SL Superset. The Maximizer's ($5.35) configuration utility provides user-adjustable settings to provide flexible power management. When using the utility, the screen displays a number of system-level power-management fields. The fields include turning the power management on and off and programmable timeouts for four different power-down modes. A CPU standby mode halts the CPU clock after a programmed system-inactivity period. A global standby mode reduces the power further by removing power to controllable peripherals. A 5V suspend mode conserves 99% of battery drain and saves system information in DRAM. A zero-volt suspend mode shuts off all system power and saves system information to disk. The bottom of the screen's menu lets you select hot keys to turn on the standby and suspend modes.

An optional APM Interface module ($2) for the Maximizer lets you take advantage of the Advanced

For more information . . .

For more information on power-management products such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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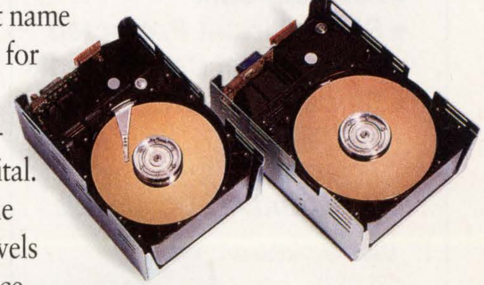

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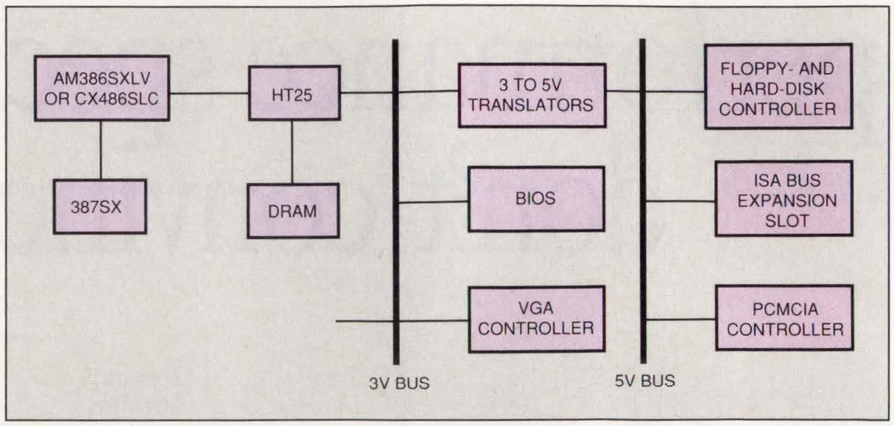

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Power Management (APM) feature in Windows 3.1. Microsoft and Intel jointly defined the application program interface, which lets an application running in Windows 3.1 send a command to the BIOS layer to manage the system power. Until APM, all power-down modes relied on timers to determine device inactivity. Because the timeouts are arbitrary, a system can be on much longer than necessary. APM sends a direct command from the application layer to the BIOS layer whenever an application doesn't require full system power. The APM interface module allows control of peripheral devices via Maximizer's global standby mode, whenever the module recognizes the APM command.

Chip set is BIOS independent

One disadvantage of managing system power at the BIOS level is the dependence on a specific operating system. To eliminate this dependence, Oak Technology offers a 3-chip set, called the Oaknote subsystem, to provide all of the core logic and display control for 386SX- or Cx486SLC-based systems. The chip set operates at 8 to 33 MHz and consists of the OTI-041 ($56 (1000)) system controller, OTI-042 ($56 (1000)) peripheral controller, and OTI-043 ($43 (1000)) VGA-display controller. The chip set has power-management features that include activity monitors, programmable I/O pins, and automatic wake-up modes. The activity monitor circuits track system interrupts, keyboard, networking, modem, and peripheral activities. Based on this activity, the chip set can enter power-saving modes independent of the BIOS firmware. Because the power management resides in on-chip hardware, it is transparent to the operating system.

The portable-computer designer is confronted with many possible avenues when considering power management. Besides choosing an appropriate CPU, the designer must use peripheral ICs that compliment the CPU's power-management mode. The designer must also select a BIOS vendor that supports both the mode and a specified operating system or chose a hardware implementation that is independent of the software. In any case, ROM-resident power-management firmware that is tuned to the chosen system configuration makes power management more tractable. EDN

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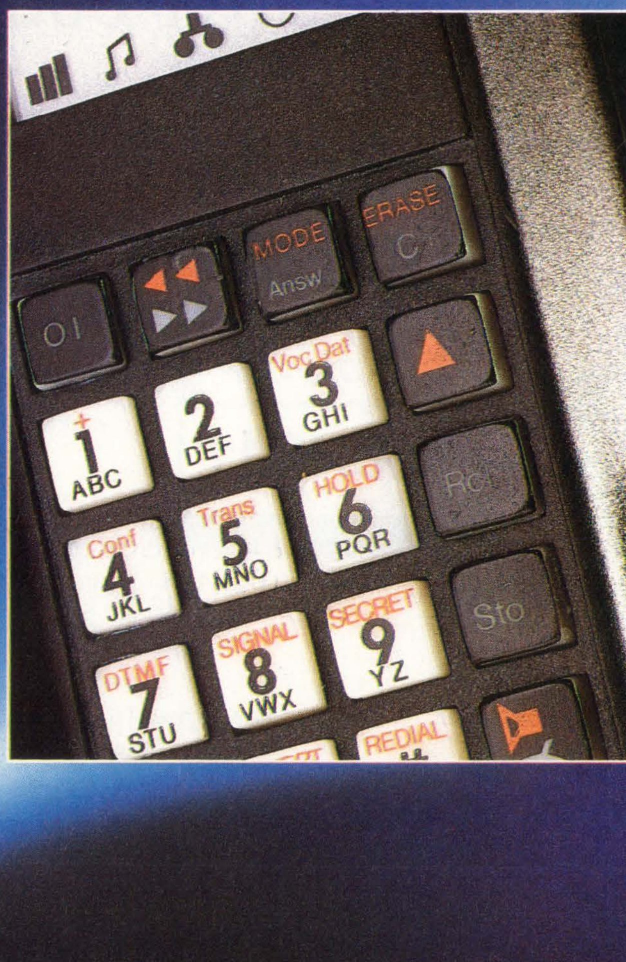

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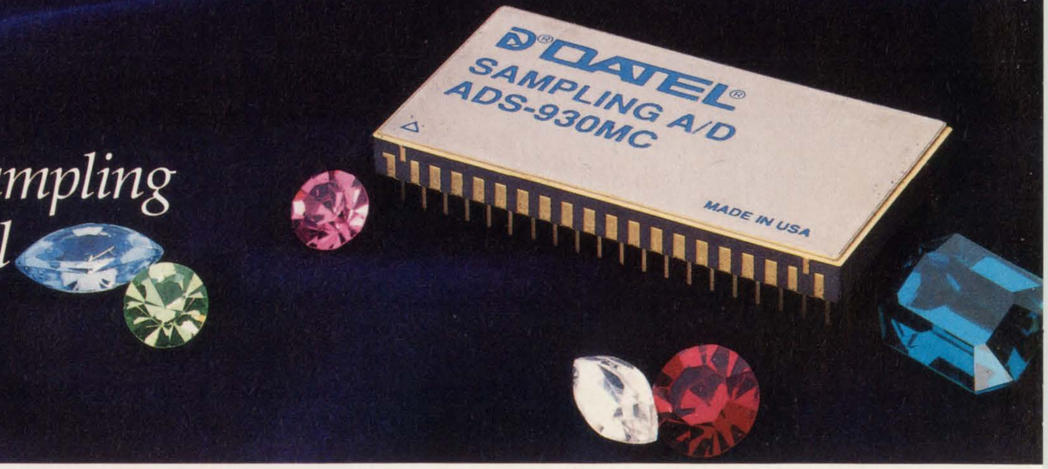

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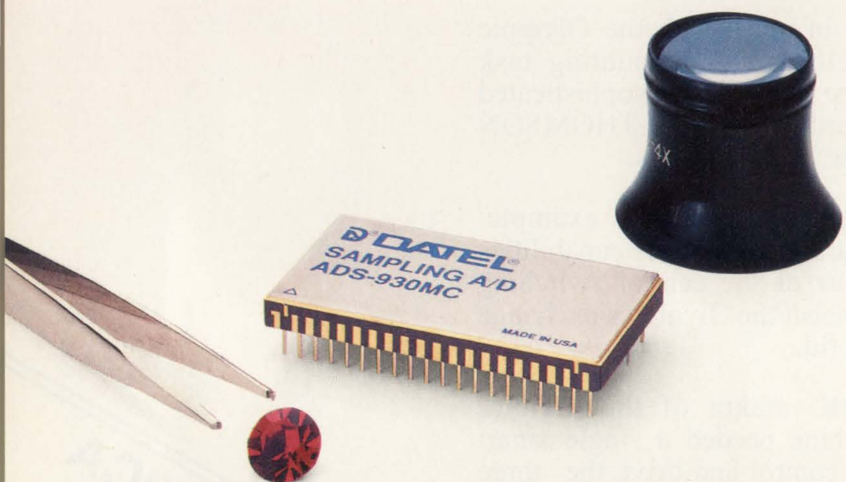

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Designer's guide to
sampling A/D converters
Part 3

Layout, grounding, and filtering complete sampling ADC system

Walt Kester, Analog Devices

Part 1 covered sampling ADCs' static and dynamic characteristics and how to protect the analog input. Part 2 discussed four key peripheral circuits. Part 3 concludes the series by examining the problems of interfacing the ADC to the rest of the system and the critical issues of grounding, layout, and filtering.

After you've selected an ADC based on its performance characteristics and considered the requirements of the peripheral circuits, you'll need to interface the ADC to the rest of the system. Then you'll have to address pc-board layout, grounding, and filtering the power-supply output, all of which can present challenges to the sampling-ADC-system designer.

To enhance performance and simplify the external circuitry, many sampling-ADC systems include digital-signal-processing (DSP) chips. The following guidelines for determining ADC interface requirements assume the presence of a DSP μP. One of the key factors to consider when interfacing an ADC to a system is the data-output configuration. Sampling ADCs have either parallel data outputs (one pin per bit) or a single serial-output data line. First, consider the parallel case.

Many parallel-output sampling ADCs have 3-state outputs that the IC's output-enable pin enables or disables. Connecting these 3-state outputs directly to a backplane data bus may be tempting, but severe noise problems may result for several reasons. All ADCs have a small amount of internal stray capacitance (typically 0.1 to 0.5 pF) between the digital outputs and the analog input. Although ADC manufacturers make every attempt during the design and layout phase to keep this capacitance to a minimum, noise on the external digital connections can couple back to the analog input. Connecting the digital output lines directly to a backplane bus often causes excessive overshoot and ringing and possibly other high-frequency noise on the digital-output lines. The effect of the noise is to decrease the ADC's overall S/N ratio and effective number of bits. Code-dependent noise also tends to increase the harmonic distortion of the ADC.

The best approach for preventing this potential problem is to provide an intermediate buffer latch close to the ADC's parallel data outputs. This latch will isolate the noisy signals on the data bus from the ADC's data outputs, thus minimizing any coupling into the ADC's analog input. Consult the data sheet regarding exactly how you should clock the data from the ADC into the buffer latch. Sampling ADCs usually have a conversion-complete or busy signal for this purpose. To further reduce the possibility of noise corrupting the ADC's analog input, don't access the data in the intermediate latch during the ADC's conversion time. The data-sheet timing information should indicate the best time to access the output data.

Fig 1 shows a simplified parallel interface between the AD676 16-bit, 100k-sample/sec ADC and the ADSP-2101 DSP μP. (The device pins have been relabeled to simplify the following discussion.) In a real-time DSP application such as digital filtering, the processor must complete its series of instructions within the ADC's sampling interval. Note that the clock edge from the sampling-clock generator initiates the conversion cycle. Although some DSP μPs can generate lower-frequency clocks from the DSP master clock, using these signals as precision sampling-clock sources may cause excess timing jitter. Generating the ADC sampling clock from a low-noise crystal-oscillator circuit is a better idea.

After the ADC completes the conversion, it asserts the conversion-complete line, which interrupts the DSP processor. The processor places the ADC's address on the data-memory address bus and asserts the data-memory select line. The circuit then asserts the DSP processor's read line, and the trailing edge of the read pulse latches the ADC data into the processor's internal registers. At this point, the processor is free to address other peripherals that share the common data bus.

Because of the high-speed internal DSP clock (50 MHz for the ADSP-2101), the read pulse's width may be too narrow for the pulse to properly access the data in the buffer latch. If this is the case, adding the appropriate number of programmable software wait states to the DSP processor will both increase the width of the read pulse and cause the data-memory select and address lines to remain asserted for a correspondingly longer period of time. In the case of the ADSP-2101, one wait state is one instruction cycle, or 80 nsec.

Interfacing serial outputs

Sampling ADCs that have a serial output usually interface to a DSP μP's serial port as **Fig 2** shows. The sampling-clock generator is a low-noise oscillator. The ADC presents its output data on the serial data line one bit at a time. The serial-clock signal from the ADC latches the individual bits into the serial-input shift register of the μP's serial-clock port. After the serial data transfers into the serial-input register, the ADC's serial-port logic generates the processor-interrupt signal.

Compared with parallel-output ADCs, the advantages of using serial-output ADCs include fewer interface connections and reduced noise because of fewer digital runs. However, the number of serial ports available on the DSP μP limits the number of peripheral serial devices you can use.

Note that until recently, manufacturers usually classified data-conversion devices in one of two groups: high resolution or high speed. As a result, two sets of techniques for applying the converters evolved. Today's high-performance sampling ADCs, however, have blurred the boundary between high resolution and high speed. For example, an ADC having an effective sampling rate of 100k samples/sec may require an internal clock running at several megahertz. This internal-clock requirement is especially true of sigma-delta converters. An 18-bit sigma-delta ADC may have a throughput rate of 50k samples/sec, but the oversampling frequency may be 64 times as high (3.2 MHz). Moreover, the ADC may interface to a DSP μP having an instruction-cycle time of less than 100 nsec and an internal clock running at 50 MHz. This combination of high resolution and high speed may present problems for design engineers whose primary experience has been with ADCs having one characteristic or the other, but not both.

To achieve optimal performance from both parallel- and serial-output sampling ADCs, mount the converter on a pc board that has a low-impedance ground plane. The ground plane (or planes) serves as a low-impedance return path for high-frequency transient currents. If you use a double-sided pc board, dedicate one side of

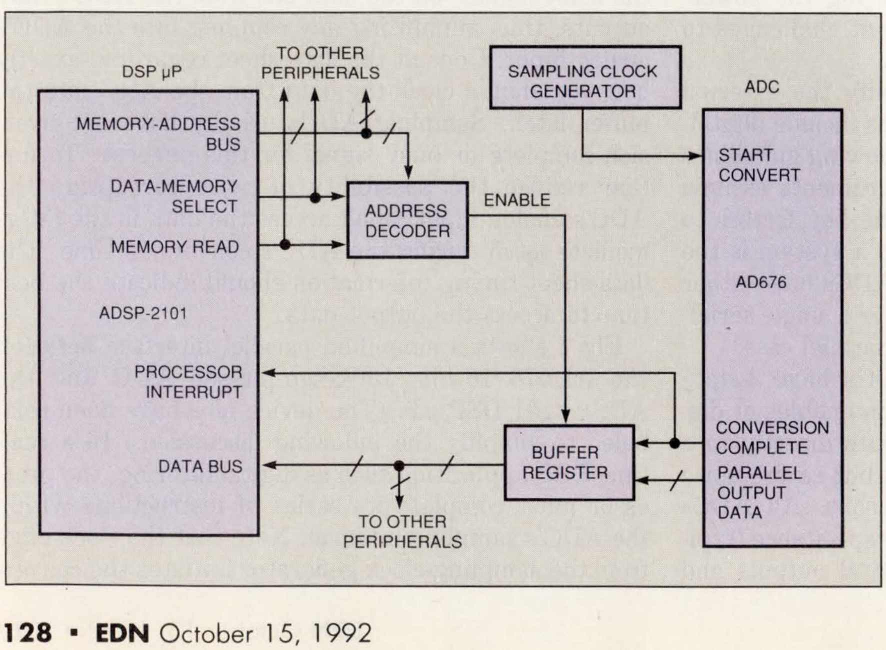

Fig 1—This parallel interface between the AD676 16-bit ADC and the ADSP-2101 DSP μP includes an intermediate buffer latch close to the ADC's parallel data outputs. The latch isolates the noisy signals on the data bus from the ADC's data outputs, thus minimizing any coupling into the ADC's analog input.

the board to the ground plane. As you lay out the board, you will inevitably lose portions of the ground plane to feedthrough holes and crossover runs. If you lose more than 25% of the original area, consider using a multilayer board. A multilayer pc board allows for much greater component density without sacrificing the ground-plane area. The layers that are not grounded handle the crossovers.

In multiple-board systems containing both analog and digital components, the common practice is to maintain separate analog and digital ground planes on each pc board. Analog components are grounded and bypassed to the analog ground plane; digital components are grounded and bypassed to the digital ground plane. The analog and digital ground planes of each pc board connect to separate ground planes on the backplane. Ultimately, the analog and digital grounds connect at a single point (sometimes called the star ground) in the system. This point is usually at the power supplies.

These guidelines can be confusing when you're dealing with ADCs that have both analog and digital ground pins. **Fig 3** is a simplified diagram of an ADC containing both analog and digital circuits. Because of the inductance and resistance of the wire bond, the analog and digital grounds do not connect within the package. If a connection were made from point A to point B in **Fig 3**, the noisy digital current would modulate the relatively constant low-noise analog current. Thus, the connection would create digital noise within the analog circuits and degrade the ADC's performance. Most manufacturers recommend connecting the analog- and digital-ground pins externally and using short connections to connect the pins directly to the ground plane.

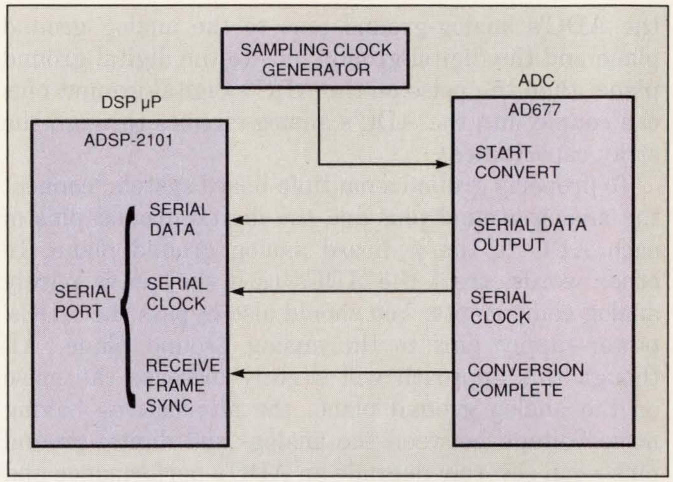

Fig 2—Sampling ADCs that have a serial output usually interface to the serial port of a DSP processor. Compared with parallel-output devices, the advantages of using serial-output ADCs are fewer interface connections and reduced noise because of fewer digital runs.

If you need to maintain separate analog and digital grounds, try connecting the analog- and digital-ground pins at the ADC. This procedure may work on a pc board having one ADC, but problems can arise in systems that have multiple pc boards and ADCs. In such systems, joining the analog and digital grounds at each ADC can create ground loops between the analog and digital ground planes. On the other hand, if you connect

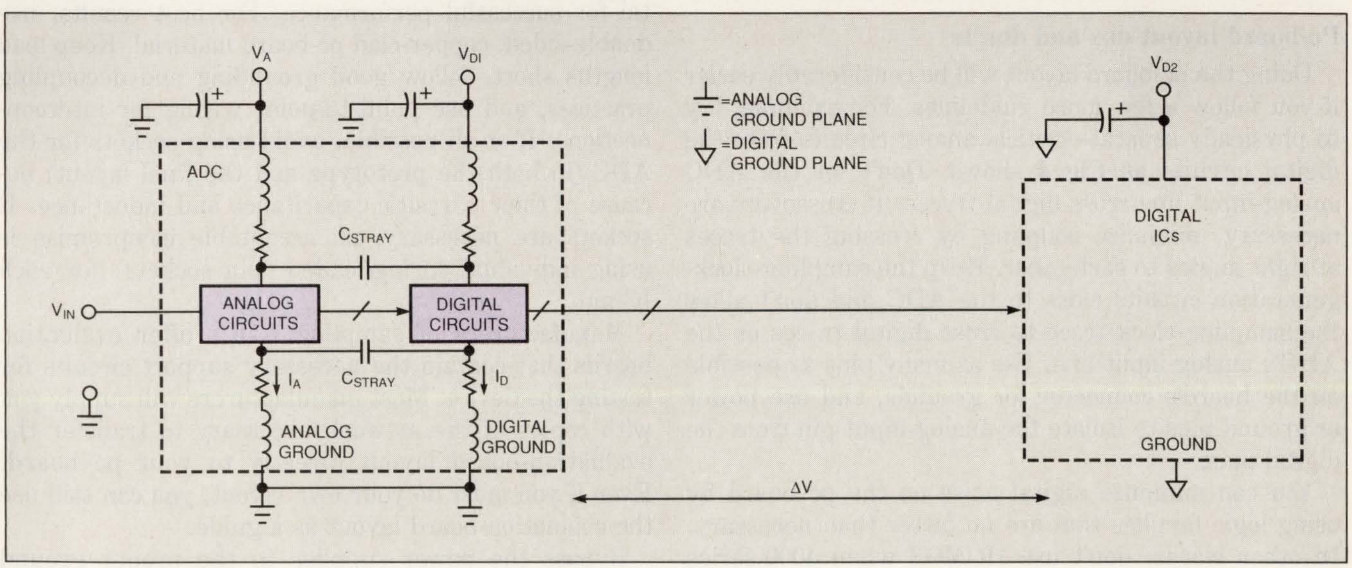

Fig 3—This simplified diagram of an ADC containing both analog and digital circuits illustrates proper grounding. Because of the inductance and resistance of the wire bond, the analog and digital grounds do not connect within the ADC package. If a connection were made from point A to point B, the noisy digital current would modulate the low-noise analog current, which would degrade the ADC's performance.

the ADC's analog-ground pins to the analog ground plane and the digital-ground pins to the digital ground plane, then the noise on the ADC's digital-ground pins can couple into the ADC's analog circuits through the stray capacitance.

To properly ground a multiple-board system, connect the analog-ground pins and the digital-ground pins of each ADC to the pc-board analog ground plane. In other words, treat the ADCs as if they were purely analog components. You should also bypass the ADCs' power-supply pins to the analog ground plane. Although this approach will slightly increase the noise on the analog ground plane, the alternative—having noise voltage between the analog- and digital-ground pins—can severely degrade an ADC's performance and is a worse choice. You should connect the ground pins of the digital circuits that connect to an ADC's digital outputs to the digital ground plane. The noise voltage between the two ground planes will slightly lower the noise margins at the digital-logic interface, but this reduction is usually acceptable.

If an ADC requires +5V, −5V, or both, use dedicated power supplies rather than supplies that also supply TTL, CMOS, or ECL circuits. If an ADC's power dissipation is low enough, consider deriving the voltages from the 15V analog supplies using 3-terminal regulators. If you can't avoid using the digital supplies for an ADC, be sure to include plenty of decoupling RC or LC filtering circuits on the pc board. You should treat the sampling-clock-generation circuits as analog components and do all grounding and decoupling with respect to the pc-board analog ground plane.

Pc-board layout dos and don'ts

Doing the pc-board layout will be considerably easier if you follow a few more guidelines. For example, try to physically separate critical analog circuits from the digital circuits as **Fig 4** shows. Don't let the ADC analog-input line cross digital traces. If crossovers are necessary, minimize coupling by crossing the traces at right angles to each other. Keep the sampling-clock-generation circuits close to the ADC and don't allow the sampling-clock trace to cross digital traces or the ADC's analog-input line. Use as many pins as possible on the board's connector for grounds, and use power or ground pins to isolate the analog-input pin from the digital pins.

You can minimize digital noise on the pc board by using logic families that are no faster than necessary. In other words, don't use HCMOS when 4000-series CMOS is fast enough. Also, use differential drivers and receivers to transfer analog signals across noisy interfaces. These components have high common-mode rejection ratios at audio frequencies as well as low

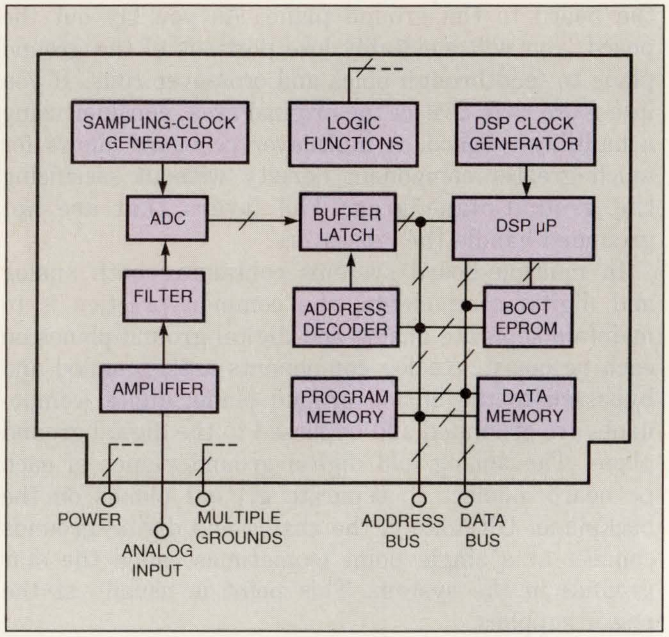

Fig 4—When routing a mixed analog and digital pc board that includes a sampling ADC, try to physically separate critical analog circuits from the digital circuits.

THD specifications. For high-frequency applications in which you must use single-ended techniques, transferring the signal across a noisy interface and maintaining acceptable dynamic range may be impossible. In this case, your only alternative may be repartitioning the system so that critical analog circuits are on the same pc board as the ADC or ADCs.

Building prototypes of precision-ADC systems is vital for successful performance. For best results, use double-sided, copper-clad pc-board material. Keep lead lengths short, follow good grounding and decoupling practices, and use point-to-point wiring for interconnections. If at all possible, avoid using sockets for the ADC (in both the prototype and the final layout) because of their parasitic capacitance and inductance. If sockets are necessary, an acceptable compromise is using individual spring-loaded "pin sockets" for each IC pin.

Manufacturers of sampling ADCs offer evaluation boards that contain the necessary support circuits for testing the device. Most manufacturers will supply you with copies of the artwork necessary to transfer the evaluation-board layout directly to your pc board. Even if you must do your own layout, you can still use the evaluation-board layout as a guide.

Bypass the power supplies to the proper ground plane at the ADC power pins with quality ceramic capacitors. Keep the bypass-capacitor lead lengths to an absolute minimum. In some applications, you may need to use surface-mounted chip capacitors for mini-

mal inductance. Values of 0.01 to 0.1 μF work well for high-frequency decoupling.

To bypass low-frequency power-supply noise, use high-quality tantalum or aluminum electrolytic capacitors of 5 to 10 μF. Place these capacitors near the point where the power supplies enter the pc board. If your system uses switching power supplies, you may need pi-network filters, which are available as single-bulkhead, feedthrough-mounting components. One caveat you should be aware of is that manufacturers of sampling ADCs commonly include on their data sheets disclaimers regarding the performance of the ADC in systems using switching power supplies. Although linear supplies are your safest bet, the extra power dissipation they require is not acceptable in many systems. If you must use switching supplies, use them with caution. The following general guidelines will help you avoid some of the most common pitfalls.

Switching supplies generate conducted noise, capacitively coupled noise, and magnetically coupled noise. The noise transients on the output lines of switching supplies are short-duration voltage spikes. Although the actual switching frequencies may range from 10 to 100 kHz, these spikes can contain frequency components that extend into the hundreds of megahertz.

Because of the wide variations in the noise characteristics of commercially available switching supplies, you should always purchase these supplies in accordance with your specification-control drawing. Although specifying switching supplies in terms of rms noise is common practice, you must also specify the peak amplitudes of the switching spikes under the output loading conditions you expect in your system. You should also insist that the switching-supply manufacturer inform you of any internal supply changes that may alter the spike amplitudes or durations or the switching frequency. These changes may require corresponding changes in your external power-supply filtering networks.

Filtering switching-supply outputs that provide several amperes and generate voltage spikes having high-frequency components is a challenge. For this reason, you should place the initial filtering burden on the switching-supply manufacturer. Even so, you may need to add further external filtering. **Fig 5** shows a general circuit for external filtering. Note that series inductors isolate both the output and common lines from the external circuits. Because the load currents may be several amperes, make sure that the inductors you choose don't saturate. Split-core inductors are a good choice. Two large electrolytic capacitors follow the split-core inductors in **Fig 5**. You may have to do some system-level experimentation to determine the optimal point at which to locate the junction of these capacitors. Chassis ground, system star ground, and floating ground are all candidates.

Place a large solid-tantalum or aluminum electrolytic capacitor of 1 to 10 μF on the pc board near the point where the power enters the board. A high-frequency, pi-network filter built from ceramic capacitors and ferrite beads should follow the electrolytic capacitor. Pi networks are available as components that you can mount directly on the pc board. Bypass the power pin of each IC on the board using a high-quality ceramic capacitor; use minimum lead lengths between the supply pin and ground. In some cases, you may need sur-

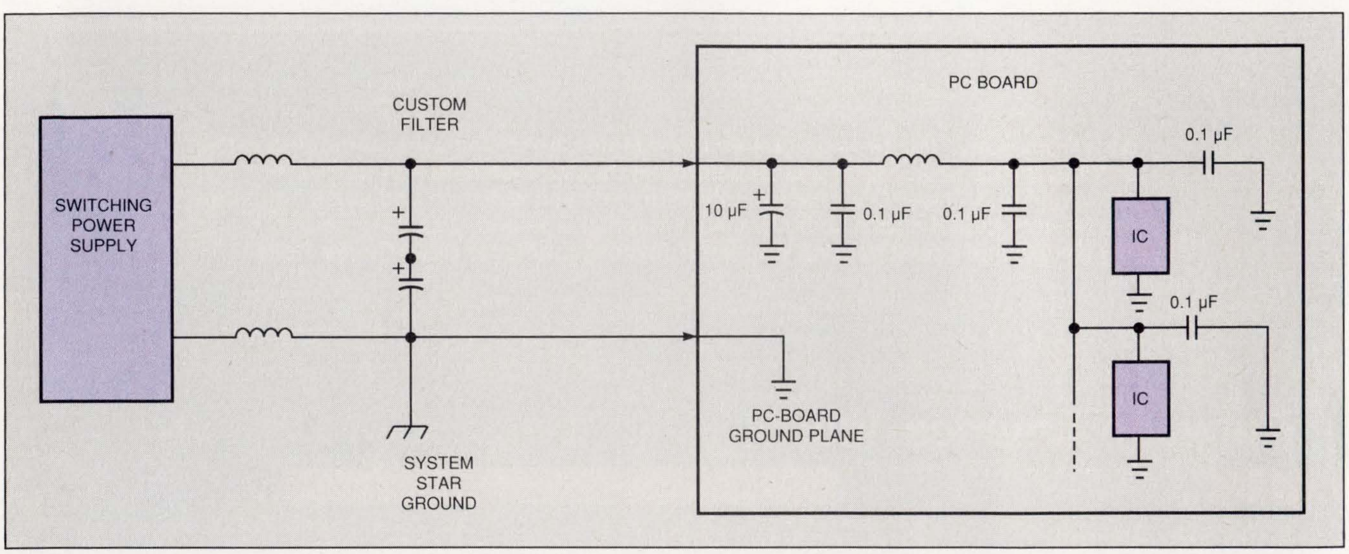

Fig 5—Filtering switching-power-supply outputs is a challenge. In this filter, series split-core inductors isolate both the output and common lines from the external circuits. Two large electrolytic capacitors follow the inductors. You may have to do some system-level experimentation to determine the optimal point at which to locate the junction of these capacitors.

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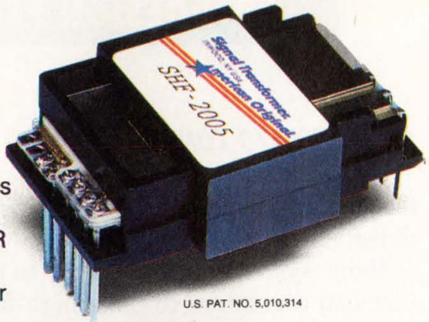

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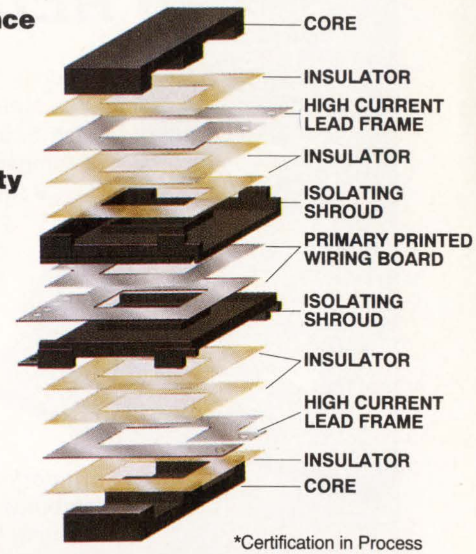

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Always check the performance of the switching supply in your system by temporarily replacing it with a low-noise linear supply. You can then compare system performance and observe the effects of the switcher on the S/N ratio and other system criteria. In some high-resolution applications—such as professional audio applications using ADCs that have an 18-bit dynamic range—linear supplies are almost always required. EDN

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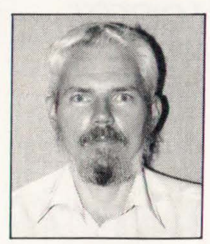
Author's biography



Walt Kester is a corporate staff applications engineer at Analog Devices (Greensboro, NC) and has been with the company for 23 years. His principal responsibility is applications support for linear and converter products. A member of IEEE, Walt has a BSEE from North Carolina State University (Raleigh, NC) and a MSEE from Duke University (Durham, NC). In his leisure time, Walt enjoys travel and carpentry.

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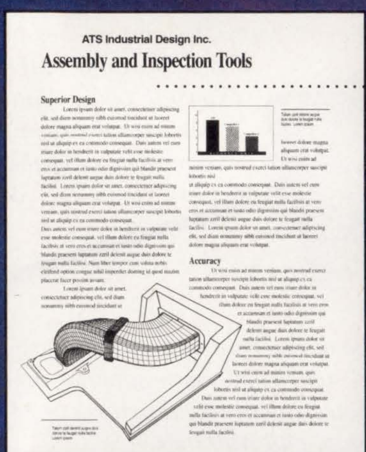

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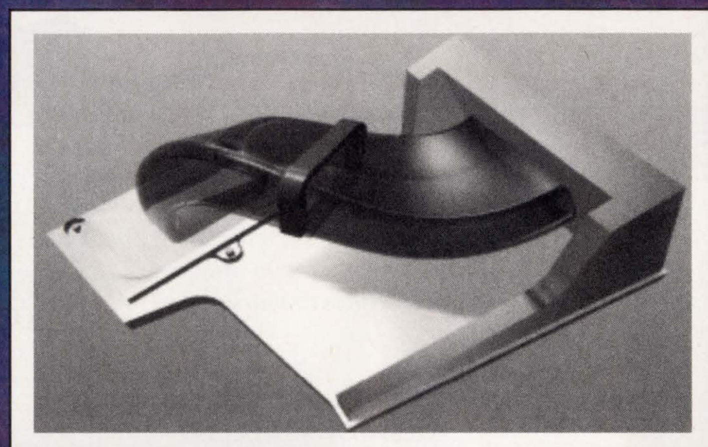

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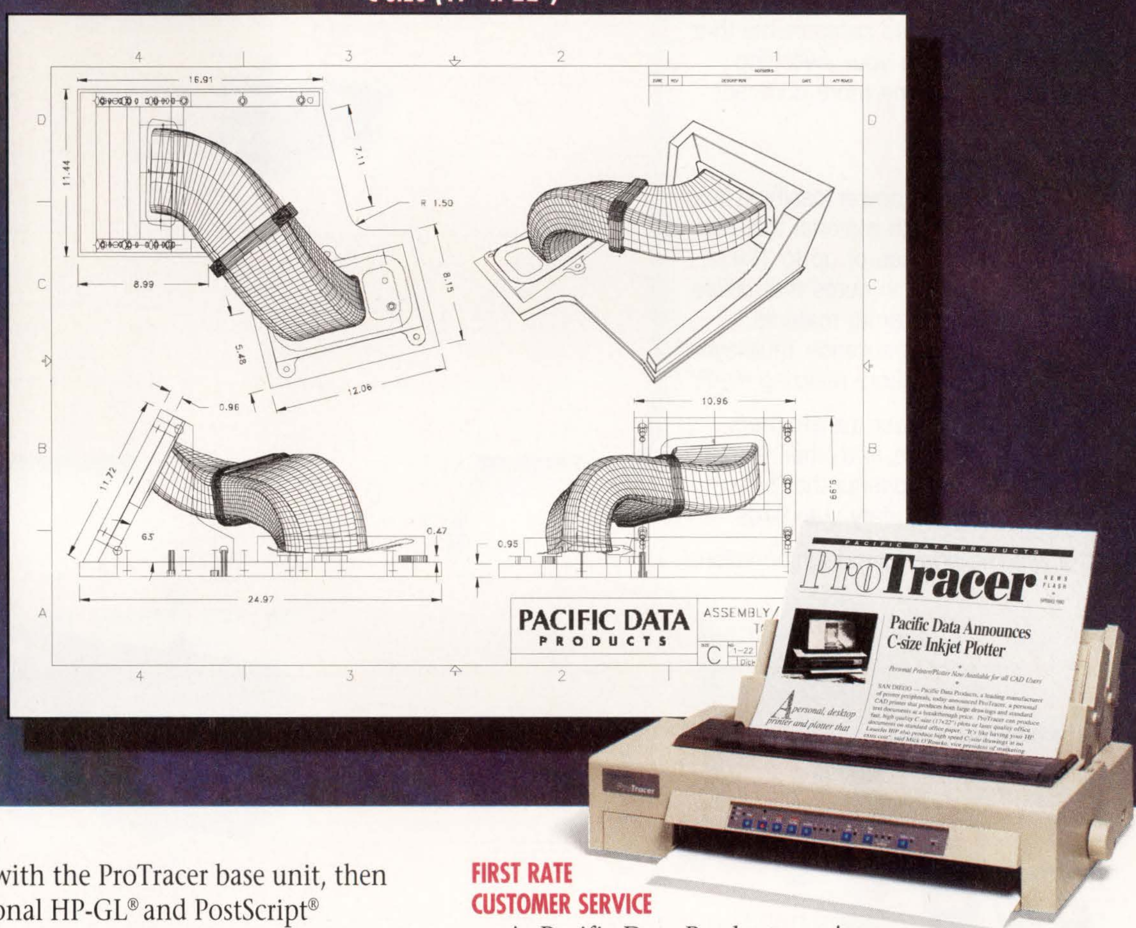

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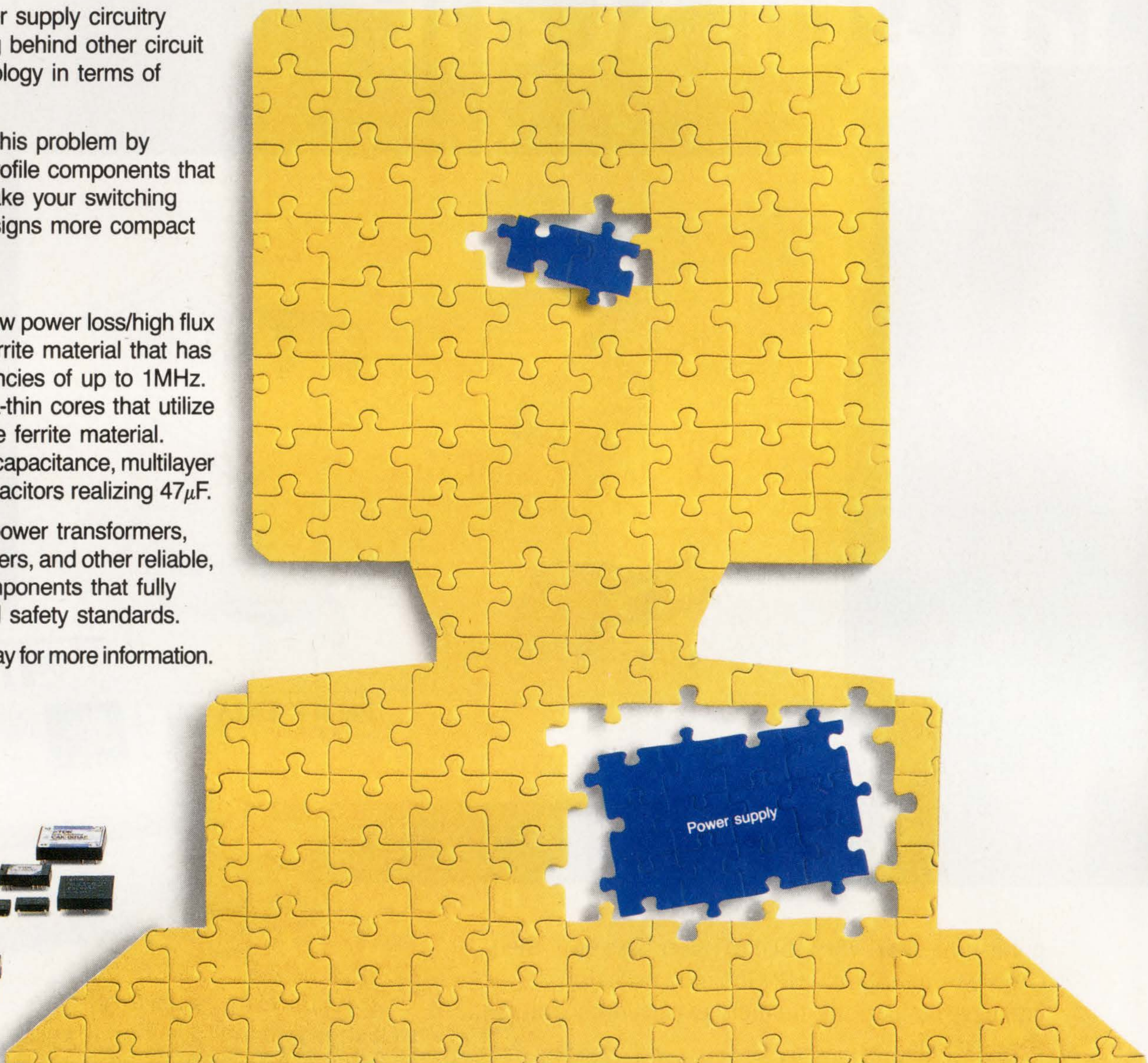

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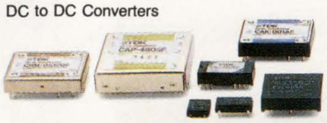

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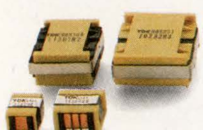

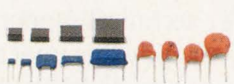

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CIRCLE NO. 98

EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

1.5 to 5V converter supplies 200 mA

Jim Williams, Linear Technology Corp, Milpitas, CA

Some 1.5V-powered systems, such as survival 2-way radios and remote, transducer-fed data-acquisition systems, require much more power than stand-alone IC regulators can provide. The converter in **Fig 1** supplies 200 mA at 5V from a 1.5V input.

The circuit is essentially a flyback regulator. The LT1170 (IC_1) switching regulator's low saturation losses and ease of use permit high-power operation and design simplicity. Unfortunately, the device has a 3V minimum supply requirement. Bootstrapping its supply pin from the 5V output is possible but requires some form of start-up mechanism. The 1.5V-powered LT1073 switching regulator (IC_2) provides a start-up loop. When power is applied, IC_2 runs and its SW_1 pin periodically pulls current through L_1. L_1 responds with high-voltage flyback events. The circuit rectifies these events, and the 470-μF capacitor stores the rectified voltage, thus producing the circuit's dc output. The output divider-string values cause IC_2 to turn off when the circuit output crosses approximately 4.5V.

Once IC_2 turns off, it obviously can no longer drive L_1, but IC_1 can. There is some overlap between the time the start-up loop turns off and IC_1 turns on, but it has no detrimental effect. The start-up loop functions over a range of loads and battery voltages. Start-up currents approach 1A, so you must pay attention to IC_2's saturation and drive characteristics. The worst case for the start-up loop is a nearly depleted battery and heavy output loading.

Fig 2a is a plot of the input and output characteristics for the circuit. Note that the circuit will start into

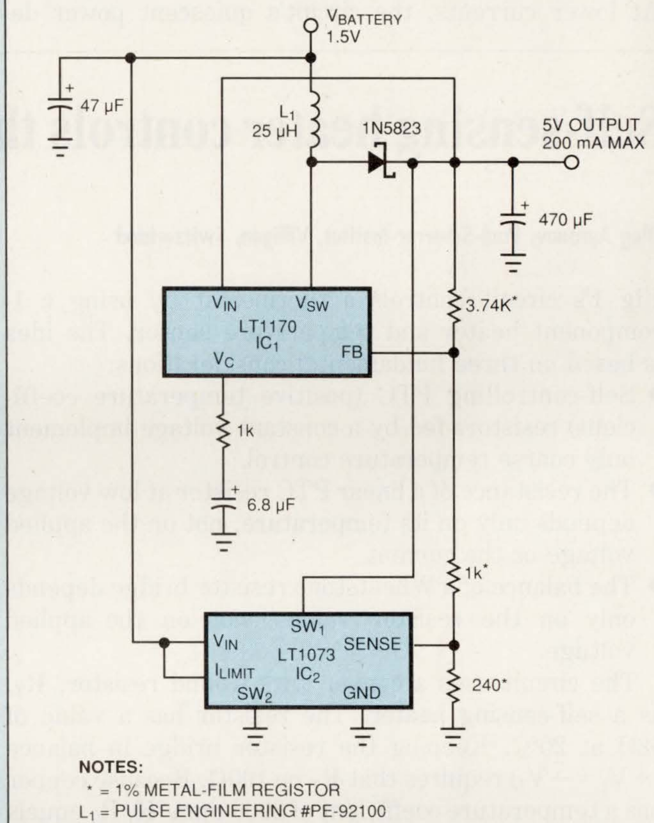

Fig 1—Using two switching regulators—one for low-voltage start up—this converter provides 200 mA at 5V from a 1.5V source.

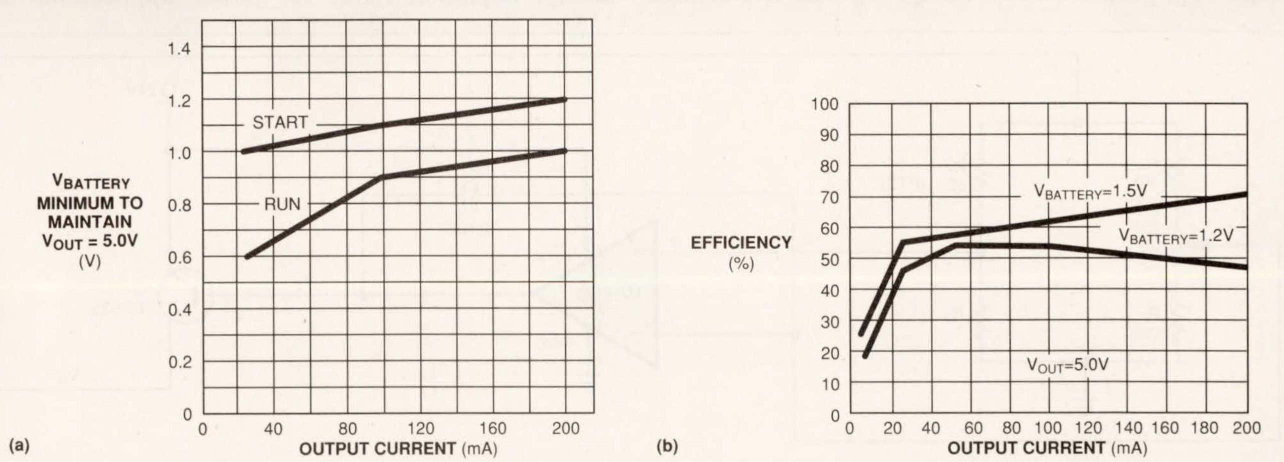

Fig 2—Performance curves of input vs output (a) and efficiency vs output (b) show this converter's start-up voltage of 1.2V and its high efficiency at higher output currents.

all loads with $V_{BATTERY}=1.2V$. Start-up is possible down to 1.0V at reduced loads. Once the circuit has started, the plot shows it will drive 200-mA loads down to $V_{BATTERY}=0.6V$. **Fig 2b** shows the circuit's efficiency at two supply voltages over a range of output currents. At lower currents, the circuit's quiescent power degrades efficiency. At lower supply voltages, fixed junction-saturation losses are responsible for the lower overall efficiency. **EDN BBS /DI_SIG #1186** EDN

To Vote For This Design, Circle No. 396

Self-sensing heater controls thermostat

Oleg Ayranov, Paul-Scherrer-Institut, Villigen, Switzerland

Fig 1's circuit controls a thermostat by using a 1-component heater and temperature sensor. The idea is based on three fundamental considerations:

- Self-controlling PTC (positive temperature coefficient) resistors fed by a constant voltage implement only coarse temperature control.
- The resistance of a linear PTC resistor at low voltage depends only on its temperature, not on the applied voltage or the current.
- The balance of a Wheatstone resistor bridge depends only on the resistor values, not on the applied voltage.

The circuit uses a copper wire-wound resistor, R_T, as a self-sensing heater. The resistor has a value of 82Ω at 20°C. Keeping the resistor bridge in balance $(+V_I=-V_I)$ requires that R_T be 100Ω. Because copper has a temperature coefficient of 3900 ppm/°K, R_T equals 100Ω when the temperature is approximately 76°C. If the temperature of R_T changes in any direction, a deviant voltage (V_I) arises between the two arms of the bridge. The op amp amplifies this deviant voltage up to the value V_O and changes the drive voltage of the bridge (V_D) proportionally via Q_1. V_D does not change the ratios of the resistors (R_1/R_2 and R_T/R_3) in a direct way, but changes the power dissipation of R_T. Consequently, the temperature of R_T closes the control loop. R_4 provides fine adjustment of the bridge.

Choosing the op amp for this circuit is critical. Because the op amp operates with a single supply $(+V_{CC}=24V,\ -V_{CC}=0V)$, its input-voltage range must include 0V. At the same time, the op amp's common-mode rejection ratio in this range must not degrade. In the data books, the common-mode rejection of an op amp is declared only as an unsigned quantity in decibels, which doesn't allow a unique conclusion about the amplifier's behavior with a common-mode input signal. In this case, the behavior of V_O with the op-amp inputs close to 0V is important. If when the inputs are close to 0V, V_O also approaches 0V, the bridge remains without current. So without additional measures, the control loop could have an unwelcome second stable state.

The most simple way to prevent this unwelcome state would be to use an N-channel depletion FET for Q_1. The bridge would not remain without current even if $V_O=0V$, which means the unwelcome case could never occur because $V_D>0V$ with $V_O=0V$. Unfortunately, depletion FETs for power applications have

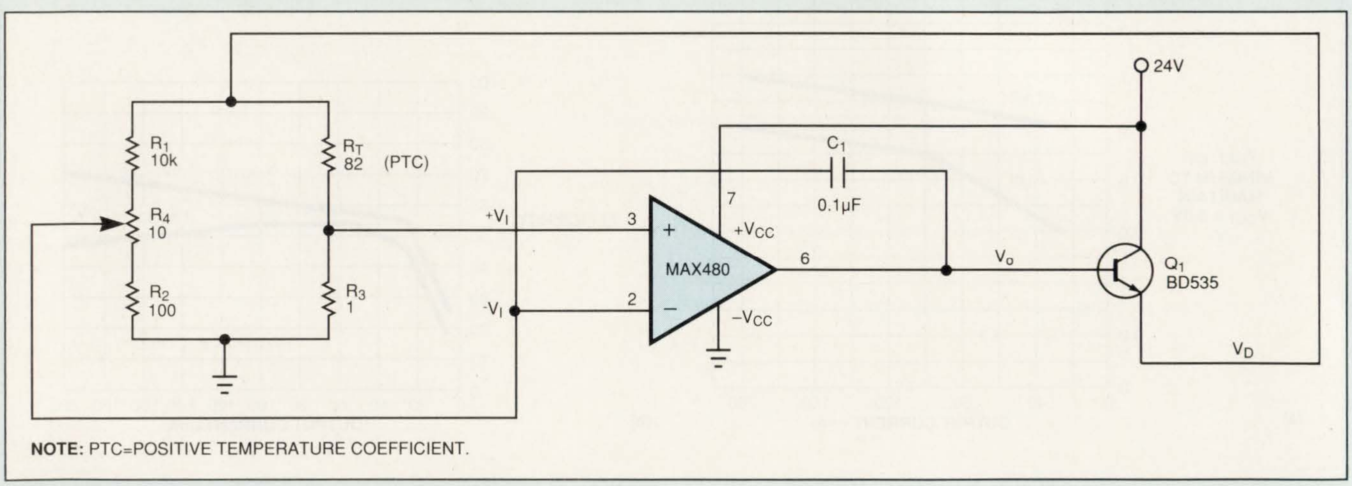

Fig 1—Choosing the op amp is critical to the design of this self-sensing heater. The op amp's input-voltage range must include ground because the op amp operates from a single supply.

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Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	—	20	—	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
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CIRCLE NO. 77

disappeared from the market in the last few years. The other preventative measure is using a zener diode or a constant current source, which the circuit could switch in parallel with the collector-emitter route of Q_1. This addition would guarantee a permanent minimal current through the bridge.

In **Fig 1**, the op amp is a MAX480. At $+V_I = -V_I = -V_{CC} = 0V$, the op amp's output voltage approaches the maximum possible value of $+V_{CC} - 1V$). Thus, this op amp is ideal for this application. Neither a zener diode nor a constant current source was necessary. The well-known CA3140 op amp showed similar behavior, but its open-loop gain was much smaller than the MAX480's.

Other criteria for the choice of the op amp are high open-loop gain, low input-offset-voltage drift, and low input current. In principle, the circuit would work without Q_1 if the op amp could provide enough output current. But power op amps that satisfy the output-current requirement don't satisfy all the other op-amp requirements.

C_1 determines the integral part of the control loop and must be big enough to sufficiently suppress all noise interfering with V_I. You can freely choose the values of R_1, R_2, R_T, and R_3. The only consideration is the power through R_1, R_2, and R_3. If the power grows too large, the resistors could heat up in different ways, which would falsify the whole control loop.

Finally, a few words about the operating point of the thermostat. Because deviant voltage V_I is also a linear function of drive voltage V_D, the total gain of the control loop strongly depends on the average value of V_D. If the circuit permits only small deviations from the rated temperature, the operating point of V_D should be high. The voltage difference between the operating point and the maximum value of V_D should be only big enough to guarantee a sufficient margin of power for the minimal ambient temperature. **EDN BBS /DI_SIG #1188**

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Text continued on pg 146

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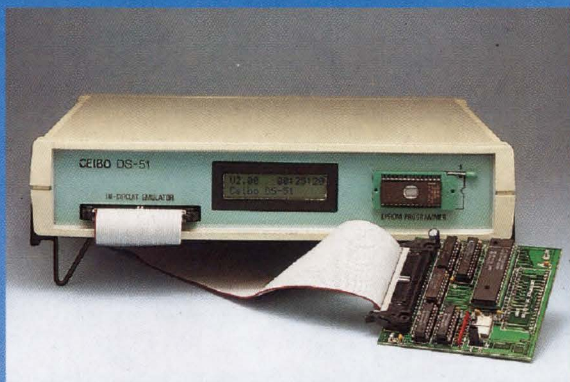
DS-51 Microprocessor Development System



Ceibo DS-51 is a real-time in-circuit emulator dedicated to the 8051 family of microcontrollers. It is serially linked to a PC/XT/AT or compatible systems. The software includes Source Level Debugger for PLM and C, a unique Source Level Assembler Debugger, Performance Analyzer, On-line Assembler and Disassembler, and many other features.

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MP-51 allows to enable or disable the PLD or Microcontroller security capabilities.

MP-51 loads different file formats: Intel Hex, Intel OMF, Binary, Motorola S-records, JEDEC, etc.

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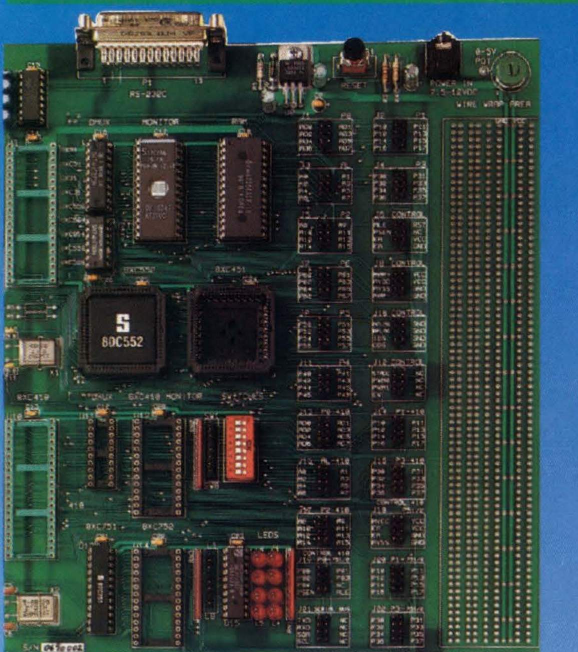
DB-51 Development Board



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CIRCLE NO. 30

Linear regulator suppresses surges

Brian Houghton, Colorado State University, Ft Collins, CO

The linear regulator in **Fig 1** functions as a surge suppressor, protecting a downstream switching regulator from transients. The circuit can protect 24V circuitry from long, 10J surges that reach as high as 150V dc.

In operation, the input voltage is normally less than the desired clamp voltage (zener diode D_1 sets the clamp voltage). Here, the base of transistor Q_2 will be at ground, cutting off emitter current. Because Q_2 is off, transistor Q_3 will also be off. Thus the pass transistor, Q_1, sees a gate-to-source voltage approximately equal to zener diode D_3's rating, saturating Q_1 on.

If the input voltage rises above the breakdown voltage of zener diode D_1, the resulting bias voltage across R_1 will turn Q_2 on, putting Q_3 into the linear mode. Q_3's increasing collector current will raise Q_1's gate voltage, tending to turn Q_1 off. The circuit will reset itself when the input voltage drops to normal levels.

Capacitor C_1 sets the dominant pole of the feedback loop when the circuit regulates. D_2 reduces R_1's power dissipation during low input-voltage conditions. R_1's power-handling capability plays a dominant role in the circuit's ability to handle repeated surges. With the components shown, the circuit withstood 130V surges lasting 0.1 sec at a 1-Hz repetition rate.

EDN BBS /DI_SIG #1134 EDN

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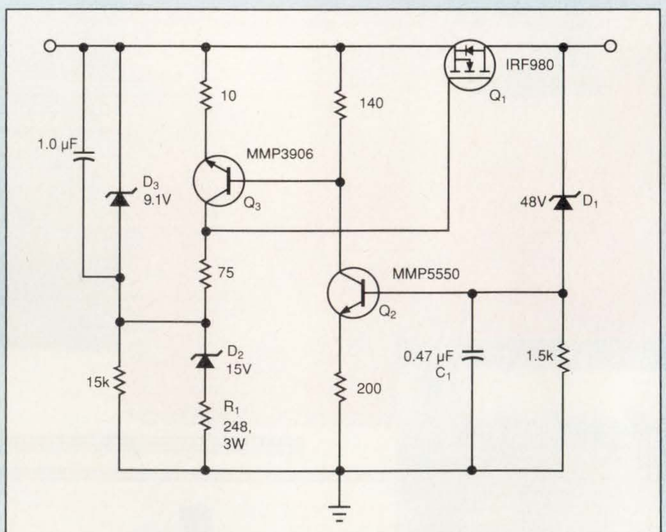

Fig 1—This linear regulator sits upstream of a switching regulator. The linear regulator operates only during power surges, protecting the switching circuitry.

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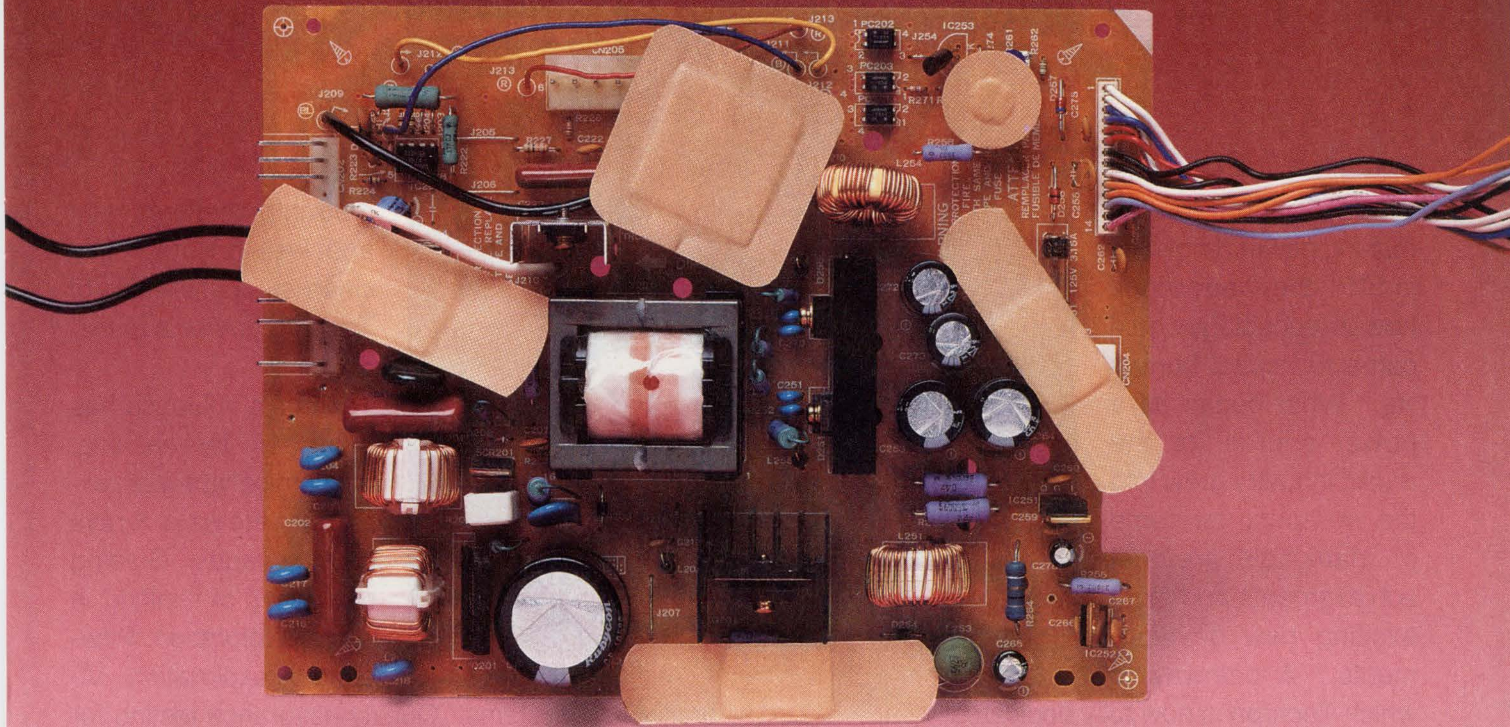

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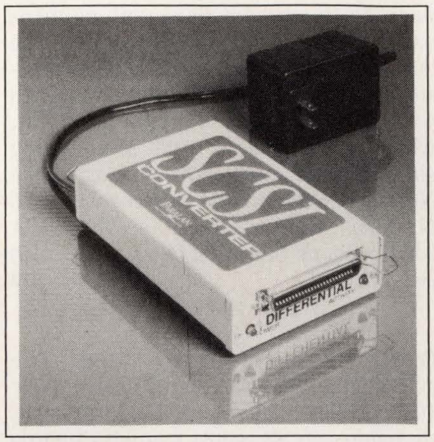
CIRCLE NO. 97

Computers & Peripherals



Converters. Series SD10 single-ended to differential converters manage the arbitration and disconnect/connect features of the SCSI bus. The converters accommodate cable lengths of 102 ft when converting to or from the differential type of SCSI. You can extend the bus to 200 ft by connecting two converters back-to-back. The units maintain full compliance with the ANSI X3T9.2 specification. The SD10 is a stand-alone external box, the SD11 is a board version. $475 and $284, respectively. **Paralan Corp,** 7171 Ronson Rd, San Diego, CA 92111. Phone (619) 560-7266. FAX (619) 560-8929. **Circle No. 301**

Color monitor. The Diamond Pro 17 for PCs, Macs, and Unix-based systems offers the Diamond Match Color Calibration System for matching on-screen colors with hardcopy or Pantone colors. The 17-in. CRT has an aperture grille pitch of 0.26 mm and is compatible with resolution-graphics standards from 640×480 pixels through 1280×1024 pixels at 60 Hz noninterlaced. $1599. **Mitsubishi Electronics America Inc,** Information Systems Div, 5665 Plaza Dr, Cypress, CA 90630. Phone (800) 843-2515; (714) 220-2500. **Circle No. 302**

Monitor. The TruePoint-AT20 combines a capacitive touch screen with a 20-in. color monitor. The unit has an active display area of 14.9×10.9 in. and features a resolution of 1280×1024 pixels. The unit is available in rack-mount and open-frame versions. The monitor provides 1024×1024 touch points. Drivers are available for all Windows 3.0 or OS/2-based authoring tools, thus minimizing development times for systems integrators. $3245. **MicroTouch Systems Inc,** 55 Jonspin Rd, Wilmington, MA 01887. Phone (508) 694-9900. FAX (508) 694-9980 **Circle No. 303**

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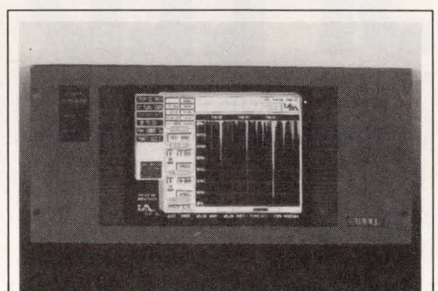
Development board. The Fast 8 Forth development board is a multipurpose board. You can use it for rapid prototyping in specific applications or as an embedded controller. A separate dual-serial-port chip allows debugging of stand-alone systems that use the Super 8 chip serial port in single-chip configurations. RS-485 LAN compatibility eases design in distributed-control systems. $329. **Space-Time Productions,** 3124 Meriday, Suite 103, Rockford, IL 61109. Phone (815) 874-2296. **Circle No. 305**

Single-board computer. The MVME197 uses the full power of the 50-MHz 88110 µP. Key computer features include high-density ASICs; SCSI, Ethernet, and parallel interfaces; a serial port; Unix system V support; and VME D64 protocol compliance. The computer comes with VMEexec development tools. $9995. **Motorola Inc,** 2900 S Diablo Way, Tempe, AZ 85282. Phone (602) 438-3576. **Circle No. 306**

Frame grabber. The LG-3 is a gray-scale NuBus frame grabber that can capture 8-bit 640×480-pixel images in $1/30$ of a second. On-board frame storage may be expanded from the minimum 1 Mbyte to 64 Mbytes. You can connect the unit to four video sources simultaneously. You can use any of the eight lookup tables to modify the digitized video. Software controls the digitization range. $895. **Scion Corp,** 152 W Patrick St, Frederick, MD 21701. Phone (301) 695-7870. FAX (301) 695-0035. **Circle No. 307**

Compression board. The Super Motion Compression card is compatible with Microsoft's DV-MCI development environment and uses a JPEG chip set to allow the compression and decompression of video at 30 frames per second. This design lets the card function across a range of ISA-based platforms. In addition to Microsoft Windows 3.0 or higher, card requirements include a 16-bit, full-size slot; a hard disk or mass-storage device with a 400-kbps continuous transfer rate; MS-DOS or PC-DOS version 3.3 or greater; and New Media Graphics' Super VideoWindows ISA board with a bidirectional NMG-VideoBus. Power requirements are 3.8A at 5V and 10 mA at ± 12V. $1995. **New Media Graphics Corp,** 780 Boston Rd, Billerica, MA 01821. Phone (508) 663-0666. FAX (508) 663-6678. **Circle No. 308**

VMEbus board. The HKMIPS/V3500 board uses the R3500 RISC processor and provides a sustained performance of 32 VAX MIPS and 11 MFLOPS. It features 64 kbytes each of direct-mapped data and instruction cache, on-board Ethernet and SCSI interfaces, as much as 32 Mbytes of local dynamic RAM (DRAM), and as much as 1 Mbyte of EPROM. The board also features two programmable counter/timers, a real-time clock with 32 kbytes of nonvolatile RAM, and four serial ports compatible with the RS-232C and RS-422A protocols. $9995 with 32 Mbytes of DRAM. **Heurikon Corp,** 8310 Excelsior Dr, Madison, WI 53717. Phone (608) 831-0900. FAX (608) 831-4249. **Circle No. 309**



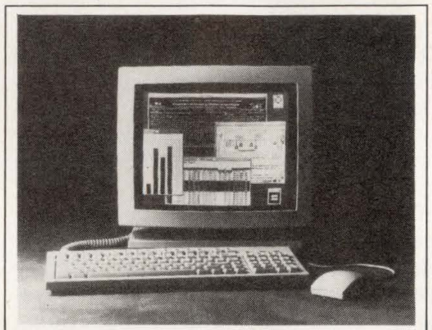
Industrial displays. Rackview is a flat-panel-display monitor. It is available in high-contrast, 16-level monochrome-electroluminescent or 185,000-color active-matrix TFT versions. An optional 128×128-point-resolution infrared touch screen is available for a direct user/screen interface. $4400. **Dolch Computer Systems,** 372 Turquoise St, Milpitas, CA 95035. Phone (408) 957-6575. FAX (408) 263-6305. **Circle No. 310**

Optical storage systems. The OpStar 6613 is based on the 12-in. Worm technology and provides end users with storage from 6.55 Gbits in a single drive

to 327.5 Gbits in a jukebox. OpStar jukeboxes range from desktop models to desk-side units. Media removability lets you secure data while also providing data transportability between systems. From $5695 for drive that accepts 650-Mbit optical disks. **Data General Corp,** 4400 Computer Dr, Westboro, MA 01580. Phone (508) 366-8911.
Circle No. 311

Accelerator. The TokaMac II FX is a 33-MHz 68040-based accelerator for the Macintosh IIfx. In addition to the 33-MHz processor, the unit uses a 128-kbyte zero-wait-state second-level cache. The unit requires a combined processor direct slot (PDS) and NuBus design to provide the speed of the PDS and to bypass the I/O performance bottlenecks of the NuBus. The unit, with a built-in math coprocessor and large on-board caches, increases performance of the Macintosh IIfx by as much as 200%. The cache produces data-miss rates of 3%. $3995. **Fusion Data Systems,** 8920 Business Park Dr, Suite 350, Austin, TX 78759. Phone (512) 338-5326. FAX (512) 794-9997. **Circle No. 312**

Trackball. Spaceball 2003 provides the visual feedback critical for effective 3-D design. It features a VCR mode that lets users instantly record and playback 3-D sequences as they generate them with the device. You can use the device in conjunction with a mouse or a digitizing tablet. The design consists of a sphere fixed on a partially concave stand. $1595. **CalComp Inc,** 14555 N 82nd St, Scottsdale, AZ 85260. Phone (602) 948-6540. **Circle No. 313**

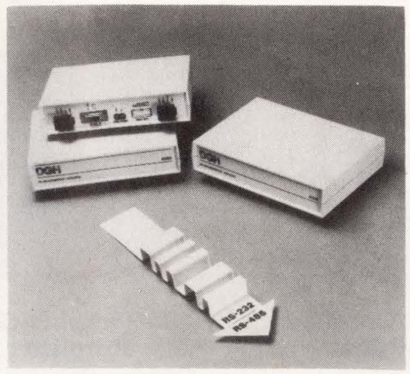


Monochrome terminal. The NCD15r combines high-performance MIPS R3000 RISC electronics with the compact 15-in. 1024 × 800-pixel monitor used in the company's CISC units. The base electronics uses a 33-MHz processor plus an ASIC. The unit comes with 4 Mbits of standard dynamic RAM, which is expandable to 20 Mbits using single in-line memory modules. $1895. **Network Computing Devices Inc,** 350 N Bernardo Ave, Mountain View, CA 94043. Phone (415) 694-0650. FAX (415) 961-7711. **Circle No. 314**

Graphics accelerator card. The AT600 Plus gives the end user 1280 × 1024 pixels in 16 colors, noninterlaced, by using the S3 86924 graphics engine from S3 Inc. With a refresh rate of 72 Hz at 1280 × 768 pixels, the unit prevents annoying flicker. The board uses a 64 × 64 × -pixel 2 hardware cursor compatible with Windows 3.0. The card is compatible with the VGA standard, so all DOS and Windows software applications will perform as expected. The unit comes loaded with software drivers for most popular applications. $395. **National Design Inc,** 1515 Capital of Texas Hwy S, Austin, TX 78746. Phone (512) 329-5055. **Circle No. 315**

Computer. The 5025 Micro PC is the smallest 386SX card available for passive-backplane PC operation. A keyboard and monitor are not required for operation. The CMOS card requires less than 1.5W. Three solid-state disks are included. The first contains DOS 3.31. The second is a flash memory for programs; the flash programmer and software are built in. The third disk can hold 1.5 Mbits of battery-backed RAM for logging process variables and data. The solid-state disks complement a standard 4-Mbit dynamic RAM. From $595 for a 16-MHz version. **Octagon Systems Corp,** 6510 W 91st Ave, Westminster, CO 80030. Phone (303) 430-1500. FAX (303) 426-8126. **Circle No. 316**

Graphics terminal. The IC-20 is compatible with the entire command set of the DEC VT340 terminal. It is also compatible with ANSI 3.64 graphics primitives and local macros. The unit uses a back-lit LCD with a resolution of 320×240 pixels in graphics mode or 16 lines of 40 characters in text mode. Data entry is via a 51-key membrane keypad mounted on the enclosure's front panel. The terminal communicates with host and auxiliary devices over two RS-232C/422/485 ports. The ports can accommodate data rates of 300 baud to 38.4 kbaud. From $1250. **Emerald Computers Inc,** 16100 SW 72nd Ave, Portland, OR 97224. Phone (503) 620-6094. FAX (503) 639-7932. **Circle No. 317**



Converter. The A2000 converts the RS-232C communications standard to the electrical signals required by RS-485. The unit is also an RS-485 repeater. It provides automatic control of bus direction without any hand-shaking signals from the host. Bus control is completely transparent to the user. The unit amplifies the RS-485 signal to drive as many as 32 additional drivers. Optical isolation equals 1500V ac. Surge protection is provided on the RS-485 output connections. $200. **DGH Corp,** Box 5638, Manchester, NH 03108. Phone (603) 622-0452. FAX (603) 622-0487. **Circle No. 318**

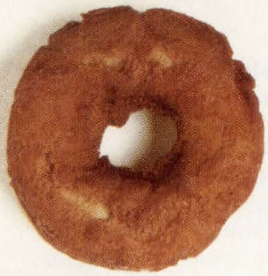
Fiber-optic multiplexer. The FMX900 simultaneously transmits and receives data channels with full handshake. Both RTS/CTS and DSR/DTR handshakes are provided. A single chassis lets you extend as many as 16 asynchronous 19.2-kbaud ports through a single pair of glass fibers. The enclosure contains a power supply and a mother board that accepts plug-in cards. The unit transmits at 3 Mbaud in serial format. $2900 for a version that connects eight RS-232C ports to eight terminals located 300 meters apart. **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132. FAX (602) 889-1510. **Circle No. 319**

2. Electronic Load

3. Voltage Source

4. Power-Pulse Generator

5. Current Source



6. Power-Function Generator

7. Direct-Coupled Amplifier

8. Variable-Gain Amplifier

9. Fast-Slewing Power Supply

10. DC Amplifier

11. AC Power Supply

12. Differential Amplifier

13. Signal-Inverting Amplifier

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CIRCLE NO. 86

Energy analyzer. The 21-lb, battery- or ac-powered 8000-2 is an 8-channel instrument that combines features of a 3-phase true-rms voltmeter, a clamp-on ammeter, a wattmeter, a DSO, a phase-angle meter, a harmonic-distortion analyzer, a neutral-to-ground monitor, a transducer monitor, an energy-demand analyzer, and an out-of-limits event monitor. Among the unit's capabilities are motor inrush-current measurement, rate-structure analysis, and harmonic analysis to IEEE-519 and IEC-555. From $6320. **Dranetz Technologies Inc,** Box 4019, Edison, NJ 08818. Phone (908) 287-3680. FAX (908) 248-9240. **Circle No. 467**

Pattern-matching software. Genmatch DSP32C software now works with the DT2878 and DT2841 ISA bus DSP and data-acquisition series. It allows real-time comparison of waveforms having data rates to 100 ksamples/sec. In determining whether patterns match, the software lets you apply tolerances to waveform segments. It lets you divide waveforms into as many as 2000 segments, and it lets you specify that a match has been achieved if m of n segments lie inside the tolerance band. Developer's edition, including one year of updates, $3500. **Genias Corp,** 2006 Woodrun SE, Lowell, MI 49331. Phone (800) 443-6427; (616) 897-5252. FAX (616) 897-0306. **Circle No. 468**

Cable-TV/TV-signal-level meter. The 8.375×4.75×7.875-in., 10.5-lb, battery-powered 951 meter can automatically search, measure, and store signal levels on 32 channels. There are two display modes: a bar-graph display of eight channels on an LCD screen and an LED display in dBmV or other engineering units. To conserve its batteries, the unit powers down automatically after a period of disuse. $1695. **Leader Instruments Corp,** 380 Oser Ave, Hauppauge, NY 11788. Phone (800) 645-5104; (516) 231-6900. **Circle No. 469**

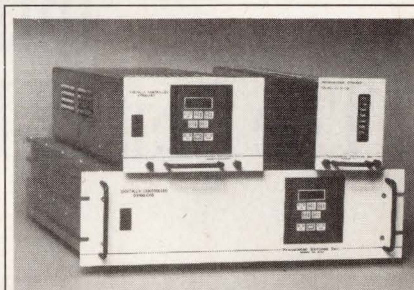
Frame-relay testers. The PC-based Sherlock LT, 5400, and 5410 wide-area-network protocol analyzers and monitors now include a local-management interface. The interface permits frame-relay decoding and supports 7-level system network architecture (SNA) decoding, X.25 decoding, and synchronous testing to 72 kbps. Asynchronous testing is supported to 38.4 kbps, as are bit- and block-error-rate testing. The vendor offers a variety of plug-in interfaces that conform to various standards. Frame-relay option, $895. **International Data Sciences Inc,** 501 Jefferson Ave, Warwick, RI 02886. Phone (800) 437-3282; (401) 737-9900. FAX (401) 737-9911. **Circle No. 470**

10-MHz-to-20-GHz synthesized signal generator. At $32,500, the 83732A costs 40% less than the vendor's most nearly comparable previous product. The generator provides output power of 10 dBm with harmonics below −55 dBc and spurious amplitude, frequency, and pulse modulation below −60 dBc. A digital pulse generator produces 25-nsec-width pulses whose rise and fall times are less than 10 nsec and whose on/off ratios exceed 80 dB. An option that improves the frequency resolution to 1 Hz adds $2000. Delivery, 12 weeks ARO. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 471**

Mixed-signal and digital IC testers. The 82000M and 82000P are test systems for mixed-signal ASIC evaluation and IC production testing, respectively. The 82000 model D100X offers improved pulse performance (relative to that of the vendor's 82000 model D100) for testing of digital ICs at speeds to 100 MHz. Fully-equipped 128-channel D100X system, approximately $325,000. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 472**

Spread-spectrum generator and demodulator for ISA bus. The $2250 ST-101 is a direct-sequence generator; the $3800 ST-102 is a programmable demodulator. Both boards let you program binary- and quadrature-phase-shift-keyed spreading sequences that include as many as 256k chirps. Chirp rates can range from 0.5 to 10 MHz. You can order the boards for intermediate frequencies of 10.7 or 21.4 MHz. The software provided with each board supports the simultaneous operation of four boards of each type. **Sigtek Inc,** 4618 Dower Dr, Ellicott City, MD 21043. Phone (410) 465-9192. FAX (410) 750-3350. **Circle No. 473**

Board-test system. The GR179X platinum test system is actually a version of GenRad's GR275X system that accommodates customer-developed fixtures and test programs that originally ran on GR179X systems two decades ago. Conversion and verification of GR179X programs takes 2 to 8 hours. Upgrades of the system provide access to the GR275X's full capabilities, including digital testing at a 20-MHz data rate. The 128-channel system, from $425,000. **GenRad Inc,** 300 Baker Ave, Concord, MA 01742. Phone (508) 369-4400, ext 2970. **Circle No. 474**



250W to 4-kW dynamic loads. The IEEE-488-programmable DCL series of electronic loads includes models with power ratings of 250W, 750W, 1.5 kW, and 4 kW; voltage ratings to 400V; and current ratings to 600A. The units can impose square-wave loading to 12 kHz (sine-wave bandwidth is 34 kHz). When operating in the constant-current mode, the units can impose arbitrary-waveform loading. $2400 to $12,000. **Transistor Devices Inc,** 274 S Salem St, Randolph, NJ 07869. Phone (201) 361-6622. FAX (201) 361-7665. **Circle No. 475**

Calibration-automation software. Met/Cal V3.0 for MS-DOS PCs generates, checks, and documents calibration procedures; executes those procedures in computer-aided or closed-loop modes; records the results; and produces calibration certificates and reports. The software's record-keeping procedures comply with standards such as ISO 9000 and MIL-STD-45662A. V3.0 adds support for the vendors' 5700A calibrator, 5790A measurement standard, PM 6680 counter/timer, 90-series Scopemeters and handheld DMMs, and Hydra series

CIRCLE NO. 88

data-acquisition instruments. Also included is support for the Tektronix SG5030 leveled sine-wave source. $5750; upgrade for current users, $600. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 443-5853.
Circle No. 476

Philips Test and Measurement, Bldg TQIII-4, 5600MD Eindhoven, The Netherlands. Phone local office.
Circle No. 477

Optical reference receivers. The ORS series of reference receivers lets you verify network compliance with the SONET (synchronous optical network) and SDH (synchronous digital hierarchy) standards. The ORS52 works with the OC-1 51.84-Mbps standard; the ORS156 works with the OC-3/STM-1 155.52-Mbps standard; and the ORS622 works with the OC-12/STM-4 622.08-Mbps standard. You can select optical-to-electrical converters with several different sensitivities. From $3995. **Tektronix Inc,** Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200.
Circle No. 478

2-channel analog scopes with menued user interface. The $1540 60-MHz TAS 455 and the $2195 100-MHz TAS 465 include such convenience features as a ground trace that appears on the screen for a few seconds any time you touch a channel's position control, and a trigger-level trace that appears superimposed on the trigger waveform whenever you adjust the trigger level. Moreover, the scopes' menu structure is identical to that of the DSOs in the vendor's TDS series for all functions the two series have in common. The scopes come with an unusual 3-year warranty: If, because of defects in materials or workmanship, a TAS scope fails within three years of purchase, the vendor will replace it. **Tektronix Inc,** Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200.
Circle No. 479

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EL2444 quad	120 MHz	4.95
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NEW EL2245 dual	100 MHz	2.95
NEW EL2073	200 MHz	4.95
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EL2041	90 MHz	250	3.75
EL2006	60 MHz	450	22.59
EL2171	3 GHz	1200	4.95
EL2038	1 GHz	1000	3.90
EL2039	600 MHz	550	2.75

*V/µs **BW

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*V/µs

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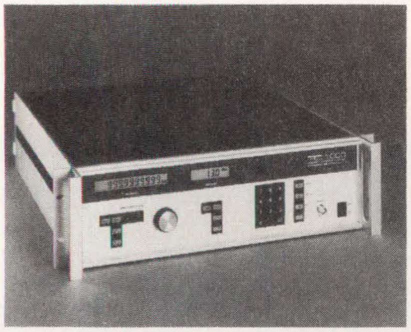
CIRCLE NO. 89



Frequency synthesizers that change frequency in 5 μsec. You can set the frequency of the 500D (1 to 500 MHz), 620D (1 to 620 MHz), and 1000D (0.1 to 1000 MHz) from the units' front panels or remotely via TTL BCD inputs. An IEEE-488 interface is optional. You can order the units with resolution as fine as 0.1 Hz. The synthesizers switch to within 0.1 radian of a new frequency in 5 μsec, if the old and new frequencies are above 10 MHz. A table look-up option provides phase-continuous switching and even faster transient response. Single-sideband phase noise (1-Hz bandwidth) is below −100 dBc 100 Hz from the carrier and below −120 dBc 10 kHz from the carrier. An optional oven-controlled crystal oscillator is stable to within 3 ppb/day and ±10 ppb from 0 to 50°C. From $6610 to $12,145 (for a model 1000D with 0.1-Hz resolution and oven-controlled oscillator). Delivery, six weeks ARO. **Programmed Test Sources Inc,** Box 517, Littleton, MA 01460. Phone (508) 486-3008. FAX (508) 486-4495. **Circle No. 480**

IEEE-488 interface for HP Series 700 workstations. The SCSI488/H connects to the SCSI port of a Hewlett-Packard Series 700 Model 705 or 710 and enables the workstation to control IEEE-488 instruments and peripherals. The unit, which conforms to HP's standard-instrument-control-library (SICL) applications-programming interface, transfers data at 1 Mbyte/sec. You can daisy chain the interfaces to control as many as 98 devices. $1495 including SICL software. **IOtech Inc,** 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093. TWX 6502820864. **Circle No. 481**

Generator of 65-psec-rise-time 7.5V pulses. The 10,070A produces positive or negative pulses that have a 125-psec fall time and 1.5-psec jitter. You can adjust the pulse width from

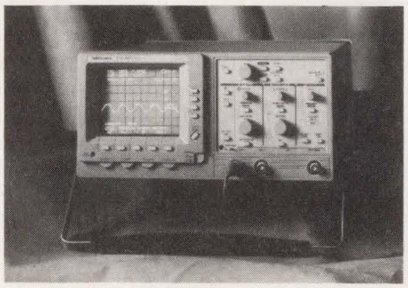
100 psec to 10 nsec in 2.5-psec steps. You can adjust the amplitude over an 81-dB range in 1-dB steps. The repetition rate, trigger delay, and baseline offset are also adjustable. The front panel includes a key pad and an LCD. Suggested list price, $13,400. Delivery, 12 weeks ARO. **Picosecond Pulse Labs Inc,** Box 44, Boulder, CO 80306. Phone (303) 443-1249. FAX (303) 447-2236.
Circle No. 482

5½-digit, 0.1-Hz to 16-MHz frequency synthesizer. The 6.5×4.5×0.75-in. SM-102 provides a TTL square wave for a 50Ω load. The unit has 8-decade frequency ranges. Frequencies are accurate to ±10 ppm from 0 to 50°C. Frequency stability of ±1 ppm over this range is optional. Following a command to change frequency, the unit's output settles within 10% of the new frequency in 10 msec. $528 (1); OEM qty available. Delivery, 30 to 45 days. **Syntest Corp,** 40 Locke Dr, Marlborough, MA 01752. Phone (508) 481-7827. FAX (508) 481-5769. **Circle No. 483**

AC/DC dielectric analyzer. The 1870 performs tests specified by agencies such as the International Electrotechnical Commission and Underwriters' Laboratories. The unit measures insulation resistance to $>10^{12}\Omega$ at test voltages to 500V dc. The basic inaccuracy is <1%, and the unit offers automatic range selection and pass/fail detection. All functions are accessible from the front panel and from an IEEE-488 interface. $8450. **QuadTech Inc,** 45 Main St, Bolton, MA 01740. Phone (800) 253-1230; (508) 779-8300. FAX (508) 779-0247. **Circle No. 484**

High-speed PS/2 interface for benchtop IC test systems. The PS/2 HSI board lets you interface the vendor's ETS series testers to PCs that use the Micro Channel Architecture bus—for example, the IBM PS/2 series. The interface, which costs less than

$5000, lets the test systems run under IBM's OS/2, a true 32-bit operating system. The vendor claims that using the 32-bit OS provides enhanced throughput in comparison with operation under a 16-bit OS. System prices, less than $300 per pin. **Hilevel Technology Inc,** 2991 Dow Ave, Tustin, CA 92680. Phone (800) 445-3835; (714) 573-1888. FAX (714) 573-1899. **Circle No. 485**



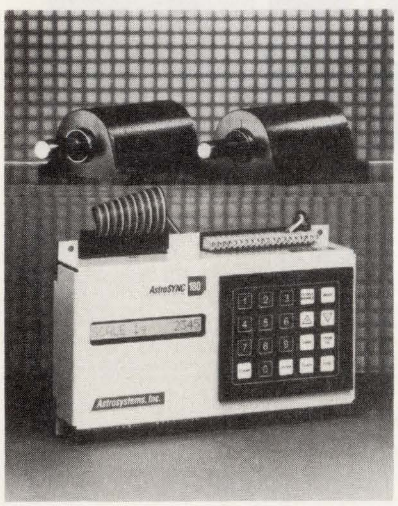
Portable spectrum analyzers. The HP 8560 E series includes a $26,000 unit that operates from 2.9 GHz to 30 Hz, a $31,000 unit that covers 6.5 GHz to 30 Hz, and a $36,000 unit that covers 26.5 GHz to 9 kHz (30 Hz optional). Below 1 GHz, phase noise is −113 dBc/Hz at a 10-kHz offset from the carrier. The units' frequency references are accurate to ±270 Hz after a 5-minute warmup and to ±180 Hz after a 10-minute warmup. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 486**

Tunable laser sources. The 8167A operates at wavelengths near 1300 nm; the 8168A operates in the vicinity of 1550 nm. Each unit permits a ±50-nm wavelength adjustment. Accuracy is ±0.1 nm; repeatability is better than ±0.05 nm. Resolution is 0.015 nm at 1300 nm and 0.02 nm at 1550 nm. Each unit, approximately $60,000. **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 452-4844. **Circle No. 487**

Spacer for microwave wafer probing. The Microwave Wafer Spacer enhances the accuracy of probing-system calibration and on-wafer measurements by reducing errors from nonuniform, multimode propagation. The quartz substrate accommodates wafers to 4-in. D. A plenum with laser-drilled vacuum vias permits securing the DUT-spacer ensemble to the wafer chuck. $850. **Tektronix Inc,** Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 488**

Components & Power Supplies

Blue LEDs. The L200CWGB6 aqua-blue LED is housed in a T-1-¾ package and has a 150-mcd output intensity. The unit is available in a clear narrow-beam style and operates at a 20-mA forward current. Operating wavelength equals 482 nm. From $12.50 (1000). Delivery, stock to six weeks ARO. **Ledtronics Inc,** 4009 Pacific Coast Hwy, Torrance, CA 90505. Phone (310) 549-9995. FAX (310) 549-4820. **Circle No. 423**

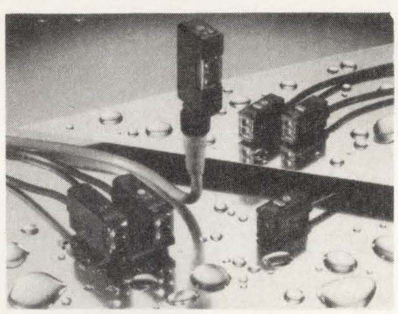


Synchronizer. AstroSYNC/180 keeps two shafts running at any desired speed ratio without mechanical coupling. Users program a gear ratio A/B by simply entering the numbers A and B on the keypad or by using a remote command via RS-422 or -485 communication. The unit continuously monitors position and computes the optimum dc control signal, keeping the shaft speed synchronized and the position matched. Multiple units can be slaved together for multiaxis synchronization. From $700 (OEM qty). **Astrosystems Inc,** 6 Nevada Dr, Lake Success, NY 11042. Phone (516) 328-1600. TWX 510-223-0411. **Circle No. 424**

Power module. MHW9002 Series power modules are for use in telecommunications equipment. They operate from a 5.8V supply and require only 5 mW of RF input power. The modules are available in versions that cover four frequency bands—the -1 version covers 824 to 849 MHz and outputs 31.5 dBm min; the -2 version has an 870- to 905-MHz operating range and a 31.5-dBm output; the -3 version spans 890 to 915 MHz and outputs 32 dBm; and the -4 version operates at 898 to 925 MHz and outputs 31.5 dBm. $18 to $21.20 (OEM qty). Delivery, 12 to 16 weeks ARO. **Motorola Inc,** E114, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-3818. FAX (602) 244-4597. **Circle No. 425**

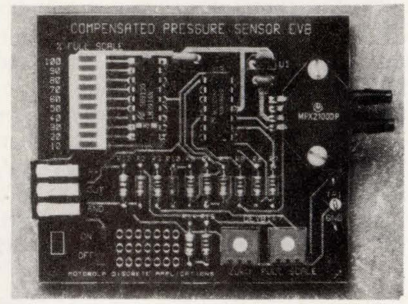
Mounting board. The PB-16M8 16-channel mounting board accepts two Mini-8 series I/O modules. The board features industry-standard logic connections through a 50-pin header connector, 2A line fuses, LED status indicators, and barrier strips for field-wiring terminations. $58 (25). **Gordos,** 1000 N Second St, Rogers, AR 72756. Phone (800) 726-0300; (501) 636-5000. FAX (501) 636-2305. **Circle No. 426**

Terminal blocks. Series 88 and 89 terminal blocks accept wire sizes of #12 through #30 AWG. Terminal spacing is 0.2 in. and 5 mm for the 88 and 89 units, respectively. Both lines are available in vertical and right-angle versions in lengths of 2 to 12 positions. The blocks conform to VDE specifications. $0.20 per position (250). **Beau Interconnect Systems,** Box 10, Laconia, NH 03247. Phone (603) 524-5243. FAX (603) 524-1627. **Circle No. 427**



Photoelectric sensors. The E3S sensor features NEMA 4X and 6 ratings. They are available in standard (-A) and miniature (-B) versions in through-beam, retroreflective, and diffuse reflective models. Response time equals 0.5 msec. From $80. **Omron Electronics Inc,** 1 E Commerce Dr, Schaumburg, IL 60173. Phone (708) 843-7900. FAX (708) 843-7787. **Circle No. 428**

Pressure gauge kit. This kit contains interface circuitry that converts the output of an MPX2100 pressure sensor to a 0.5 to 4.5V output that is then translated by a bar-graph display driver to interface with a 10-segment LED bar-graph display. The boards are de-



signed to provide a 15 psi, full-scale pressure measurement. The kit contains a completely assembled evaluation board, application note, MPX2100 data sheet, MC33274 data sheet, and a sensor brochure. $75. **Motorola Inc,** 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-5395. FAX (602) 244-5680. **Circle No. 429**

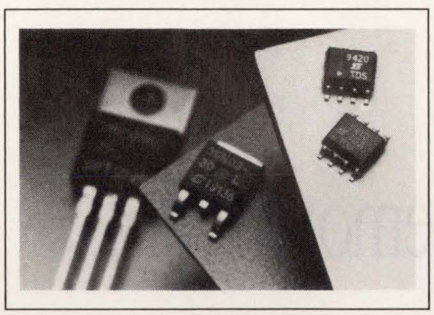
Flex circuit connectors. FPC connectors allow vertical or right-angle connection of flexible etched cable, flat flex cable, and flexible printed circuits to a pc board. The right-angle versions mate with either side of the cable. The vertical unit has a detent that holds the actuator in the open position to provide a zero-force insertion. The connectors are available with 4 to 30 positions. $0.38 to $0.80 (250,000). Delivery, six weeks ARO. **AMP Inc,** Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752. **Circle No. 430**

Grommet edging. Spring-Fast composites are clad with a polymer that ensures abrasion resistance and provides electrical insulation. The product is recognized by all certification groups and meets all Bellcore flammability requirements. The edging easily snaps into place to cushion cable pathways through metal wall slots and along cabinet edges. $2.72 per grommet ft. **Device Technologies Inc,** Box 968, Framingham, MA 01701. Phone (508) 877-4233. FAX (508) 877-8179. **Circle No. 431**

Crystals. These crystals operate over a range of 6 to 30 MHz and have a ±150-ppm pulling range from nominal load capacitance. Room-temperature frequency tolerance equals ±10 ppm. The units are housed in a leaded package measuring 0.53×0.434×0.18 in. $4.80 (100). Delivery, six weeks ARO. **Standard Crystal Corp** 9940 E Baldwin Pl, El Monte, CA 91731. Phone (800) 423-4578. FAX (818) 443-9049. **Circle No. 432**

Enclosures. Ratiopac cases can be used as desktop units or as 19-in. rack-mounted enclosures. All dimensions are identical to a 19-in. subrack for mounting bus-structured backplanes and plug-in units from the front or rear. The cases will accommodate a 3U unit in a 3U case or a 6U unit in a 6U case. The line includes a variety of widths in 3 and 6U heights. From $124 for a 3U unit. **Schroff Inc,** 170 Commerce Dr, Warwick, RI 02886. Phone (800) 451-8755; (401) 732-3770. FAX (401) 738-2904. **Circle No. 433**

Power transistor. The MRF10031 is designed for common base-amplifier applications in military and commercial transmitters. The unit will provide a 9.5-dB gain operating from 36V and will handle 10-μsec pulses at a 50% duty cycle for a period of 3.5 msec. The transistor will output a minimum of 50W pk over its operating range of 960 to 1215 MHz. $95.50. Delivery, stock to 12 weeks ARO. **Motorola Inc,** MD 56-102, Box 52073, Phoenix, AZ 85072. Phone (602) 244-3818. FAX (602) 244-4597. **Circle No. 434**



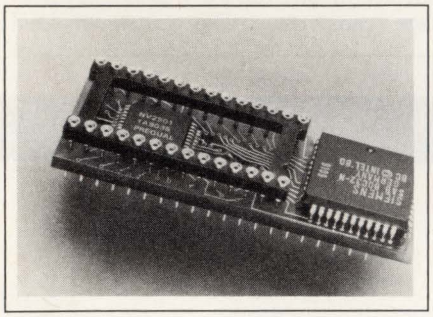
MOSFETs. The Si9420DY and Si9410DY are rated for 200 and 30V, respectively. The units are housed in 8-pin surface-mount packages and are mounted on low thermal-impedance copper lead frames, which allow the units to dissipate 2.5W. The Si9410DY features a 4.5V gate drive. Si9410DY, $0.77; Si9420DY, $0.46 (OEM qty). **Siliconix Inc,** 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000. **Circle No. 435**

Adapter. Model ANC-9232P adapter accepts 14×14 pin-grid-array devices with as many as 132 pins and converts the layout to wire-wrap pins. The unit is available with 3-level wire-wrap pins or 0.18-in. gold-plated machine pins. The units feature labeled test points for each of the 132 pins and two LED status circuits that provide a visual indication for user-selected signals. $115. **Antona Corp,** 1643½ Westwood Blvd, West Los Angeles, CA 90024. Phone (310) 473-8995. FAX (310) 473-7112. **Circle No. 436**

Power transformers. SPW-2300 Series units are rated for 12 VA and have outputs ranging from 5 to 230V ac. In addition to shrouded primaries, each transformer has insulating anchor and crossover tapes. Each unit is totally immersed in 100% solid epoxy to withstand aqueous and solvent pc-board cleaning processes. $5 (OEM qty). **Prem Magnetics Inc,** 3521 N Chapel Hill Rd, McHenry, IL 60050. Phone (815) 385-2700. **Circle No. 437**

Interface module. The PE-65745 is a surface-mount 10Base-T isolation interface transformer. The transfer-molded

part operates with Level One's LXT901 and Fujitsu's MB86961 transceiver chips. The unit withstands infrared and vapor-phase reflow soldering. The unit meets the IEEE-802.3 standards and FCC/VDE emissions requirements. $2.25 (1000). **Pulse Engineering Inc,** Box 12235, San Diego, CA 92112. Phone (619) 674-8100. FAX (619) 674-8262.
Circle No. 438



Socket. The Correct-A-Chip programmed socket lets you incorporate additional circuitry within the socket envelope to create a semihybrid daughter board. The socket lets you lay out function sites on mother boards, and various plug-in functions can then be socketed into the sites. To upgrade designs, you replace the original ICs with newer devices that have better performance; the socket easily converts from one package style to another. $15 (500). Delivery, four to six weeks ARO. **Aries Electronics Inc,** Box 130, Frenchtown, NJ 08825. Phone (908) 996-6841. FAX (908) 996-3891.
Circle No. 439

Capacitors. These polypropylene devices have 1 and 2% tolerances and are available in values ranging from 0.001 to 10 μF. The devices come with working voltage ratings of 67, 135, 270, and 660V ac and 100, 200, 400, and 1000V dc. Operating range spans −55 to +105°C. $1 (1000) for 1% units. Delivery, 8 to 10 weeks ARO. **Electrocube,** 1307 S Myrtle Ave, Monrovia, CA 91016. Phone (818) 301-0122.
Circle No. 440

Board connectors. Model 301B-48TRU connectors are designed to connect pc-memory-upgrade boards for HP Laserjet printers. Contacts are rated for 1A at 500V ac. Contact and insulation resistance equal 30 mΩ and $10^9\Omega$, respectively. The insulators carry a 94V-0 UL rating. Operating range spans −55 to +105°C. **Oupiin America,** 26821 Reuther, Unit D, Santa Clarita, CA 91361. Phone (805) 252-4760. FAX (805) 252-9214. **Circle No. 441**

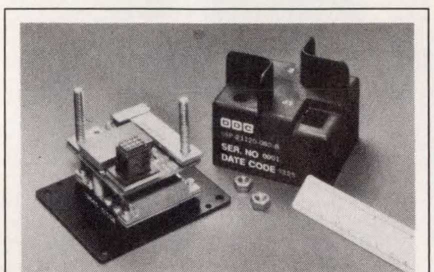
Solid-state relays. The HSSR-8060 and -8400 operate as single-pole, normally open switches. The 8060 can switch loads of 28V dc, 24V ac, or 48V dc. They have a 1.5A rating and a 0.4Ω on resistance. The 8400 will switch 110 or 220V ac loads. It has a 6Ω on resistance and a 300-mA current rating. HSSR-8060, $3.65; HSSR-8400, $3.47. **Hewlett-Packard Co,** Box 58059, Santa Clara, CA 95052. Contact local sales office.
Circle No. 442

Rechargeable battery. These nickel hydride batteries have 40% more capacity than similar-sized NiCd units. The batteries can be charged in 1 hour and have a wide discharge range, −20 to +60°C. Life is specified as 500 charge-discharge cycles. The units are available in cadmium-free standard cells and high-capacity versions that contain

0.4% cadmium. AA cells, \$6.50 (1000). **Varta Batteries Inc**, 300 Executive Blvd, Elmsford, NY 10523. Phone (914) 592-2500. **Circle No. 443**

Transistors. The high-speed GF IGBTs have BV_{CES} ratings of 600 to 1000V and have a fall time of 0.5 to 0.8 μsec. Low-conduction-loss GL models also have a 600 to 1000V BV_{CES} rating and a fall time of 1 to 1.5 μsec. Current ratings range from 25 to 55A for GF units and 30 to 75A for the GL devices. From \$9 to \$28 (100). **Advanced Power Technology**, 405 SW Columbia St, Bend, OR 97702. Phone (503) 382-8028. **Circle No. 444**

Resistor networks. These gull-wing resistors come in narrow (Series 4K00T), medium (Series 4800T), and wide (Series 4400T) types. The narrow-body units are available with 8, 14, and 16 pins with a resistance range of 10 to 100 kΩ. The medium-body units are available with five tolerances and come in 14-, 16-, 18-, and 20-pin versions. The wide-body units are housed in 16- and 20-pin packages. From \$1.76 (OEM qty). **Bourns Networks Inc**, 1400 N 1000 W, Logan, UT 84321. Phone (801) 750-7333. **Circle No. 445**



Circuit breaker. The SSP-21120 solid-state power controllers replace circuit breakers. The line includes versions rated for 40, 60, and 80A at voltages as high as 28V dc. Fault and I^2t trip characteristics can be factory set. The controllers have a 6.3-mΩ on-resistance and dissipate only 12W. A built-in test monitors the status of both the internal and external circuitry in real time. Operating range spans −55 to +85°C. From \$1295. **ILC Data Device Corp**, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600, ext 7419. FAX (516) 567-7358. **Circle No. 446**

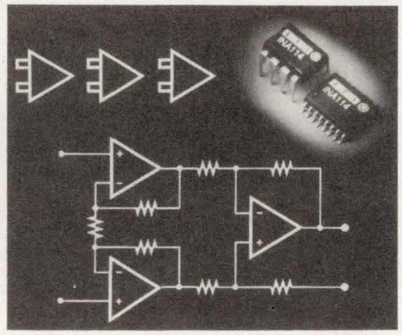
Ribbon connector. The metal-shell, right-angle ribbon connectors in the Lyte Series have a 0.085-in. pitch and are available with 14, 24, 36, and 50 contact positions. The connectors have sturdy bail latches for secure locking. Operating range spans −55 to +105°C. \$1 to \$3. Delivery, stock to six weeks ARO. **Cinch Connectors**, 1500 Morse Ave, Elk Grove Village, IL 60007. Phone (708) 981-6000. **Circle No. 447**

Optical data link. This optical data link comprises the FTM-8500 transmitter, the FRM-8500 receiver, and the FCC-2000 link controller. The link will accommodate data transmission speeds of 100 Mbps to 1.5 Gbps over distances of 500m. Bit error rates are $<10^{-12}$, and laser-light source life is specified at 200,000 hours. The transmitter and receiver modules consume <1W of power and operate from 5 and 12V supplies. The modules work with standard multimode fiber. FTM-8500, \$310; FRM-8500, \$300; FCC-2000, \$60. **Finisar Corp**, 3515 Edison Way, Menlo Park, CA 94025. Phone (415) 364-2722. **Circle No. 448**

Integrated Circuits

True-color PC RAMDAC. The Bt485 provides 75-, 85-, 100-, and 135-MHz video bandwidth to work with 1280× 1024-pixel graphics. It offers 16.7 million colors in 24-bit true-color mode and is compatible with VGA, superVGA, Windows-based systems, Targa, and Macintosh standards. The chip connects directly to the video-RAM frame buffer, and it provides the serialization and timing logic. A TTL on-chip clock doubler eliminates the need for ECL logic. The 75-MHz version, $22.65 (100). **Brooktree Corp,** 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. FAX (619) 452-1249. TLX 383596. **Circle No. 401**

Dual comparator. The SPT9691 features a common-mode input-voltage range of −4 to +8V and a maximum propagation delay of 3 nsec. The dual comparators use JFET input stages, which have typical input bias currents of ±0.1 nA. The 3-dB bandwidths of each device track each other and are typically 300 MHz. The open-loop gain is 60 dB, and the input capacitance is 1 pF. The 20-pin plastic leaded chip carrier, which operates from 0 to 70°C, $16.40 (1000). Delivery, four to six weeks ARO. **Signal Processing Technologies,** 1510 Quail Lake Loop, Colorado Springs, CO 80906. Phone (800) 643-3778, ext 778; (719) 540-3914. FAX (719) 540-3970. **Circle No. 402**

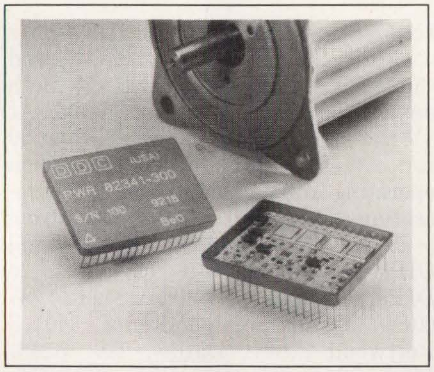


Instrumentation amplifier. The INA114 instrumentation amplifier provides 50-μV offset voltage; 0.25-μV/°C offset voltage drift; 2-nA input bias current; 115-dB CMRR; 3-mA quiescent current; and ±40V input overvoltage protection. A 3-op-amp design fits into an 8-pin DIP that operates from ±2.25 to ±18V. $3.25 (1000). **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. **Circle No. 403**

Computer chip set. The EF8290WB chip set consists of two 160-pin plastic quad flatpacks--the 82EC392 bus controller and the 82EC495 system controller. The chip set works with 386DX, 486SX, and 486DX μPs running at 20 to 50 MHz. You switch to a 386 μP mode by connecting a pin to V_{SS}. The chip set has 64-, 128-, 256-, and 512-kbyte cache-memory sizes. The chip set also works with the Weitek 3167 and 4167 coprocessors. $24 (100). **Efar Microsystems Inc,** 800 Charcot Ave, #110, San Jose, CA 95131. Phone (408) 943-1688. FAX (408) 943-1689. **Circle No. 404**

Low-voltage 80C51 μC. The 80CL51 is pin-for-pin compatible with the 80C51 microcontroller (μC). It operates from 1.8 to 6V dc and oscillator frequencies from dc to 3.58 MHz. The CMOS chip draws 50 μA when operating at 1.8V and 32 kHz; when operating at 3V and 3.58 MHz, the chip draws 2.5 mA. Power-down current draw is 10 μA when operating at 1.8V. The 80CL51 has eight more external interrupts than an 80C51 μC and can wake the controller from power-down mode. DIP version, $3.20 (10,000). **Signetics Co,** Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000. **Circle No. 405**

FPGA family. The ATT1C05 and ATT1C11 are the first members of the Optimized Reconfigurable Cell Array (ORCA) FPGA family; they have densities of 5000 and 11,000 gates, respectively. The ORCA family has densities ranging from 3000 to 20,000 gates and clock rates as fast as 80 MHz. Configurable look-up tables in each logic block optimizes logic utilization. ATT1C05, $240; ATT1C11, $710 (100). **AT&T Microelectronics,** 52AL040420, 555 Union Blvd, Allentown, PA 18103. Phone (908) 771-2788. **Circle No. 406**

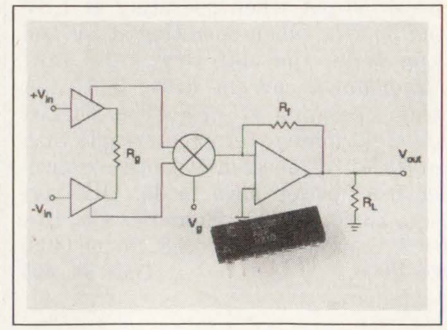


H-bridge motor driver. The PWR-82341 has two MOSFET H-bridge output stages that deliver 10A peak and 5A continuous current. The output stages can switch at 50 kHz and operate from a 100V dc supply voltage. A hermetically sealed metal package occupies 2.5 in.^{2} of board space. Internal logic for the two output phases prevent simultaneous turn-on of upper and lower transistors. The device operates from −55 to +125°C. $510. Delivery, from stock to 90 days ARO. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716. Phone (800) 332-1772; (516) 567-5600, ext 7419. FAX (516) 567-7358. **Circle No. 407**

Ferroelectric RAM. The FM 1208 is a 4-kbit nonvolatile ferroelectric RAM organized as 512×8 bits. It uses 1.5-μm silicon-gate CMOS technology. The chip operates from a 5V supply and consumes a maximum power of 44 mW. The I/O ports are TTL compatible, and the operation is synchronous on the high-to-low transition of $\overline{CE}$ signal. The read and write cycles are symmetrical and have a read-access time of 250 nsec. $2.95 (1000). **Ramtron International Corp,** 1850 Ramtron Dr, Colorado Springs, CO 80921. Phone (800) 545-3726; (719) 481-7000. FAX (719) 481-9170. **Circle No. 408**

FPLA and PLD. The GAL6002B-15L PLD (programmable logic device) is an upgrade to the company's GAL6001 field-programmable logic array (FPLA). The chip operates at a maximum frequency of 75 MHz and has a propagation delay of 15 nsec. The architecture features individually configurable macrocells and provides more registers. The GAL26V12B-10L is an upgrade to the GALCV12-15L. The chip operates as fast as 105 MHz and has a propagation delay of 10 nsec. In DIPs, GAL6002B-15, $9; GAL26CV12B-10, $8 (1000). **Lattice Semiconductor Corp,** 5555 NE Moore Ct, Hillsboro, OR 97124. Phone (503) 681-0118. FAX (503) 681-3037. TLX 277338. **Circle No. 409**

3.3V DRAMs. This set of four 4-Mbyte dynamic RAMs operate from 3.3V. The devices come in versions having 70- or 80-nsec access time and typically consume 190 mW for a 70-nsec access time. The devices feature page and early write access modes. They consume 1.8 mW in standby mode, and they have a self-refresh mode. The M5M4V4160, M5M4V4170, and M5M4V4260 have a 256k × 16-bit organization. The M5M-4V4800 has a 512k × 8-bit organization. $28 (100). **Mitsubishi Electronics America Inc,** 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900. **Circle No. 410**



Variable-gain amplifier. The CLC522 amplifier integrates a 2-quadrant multiplier, two input buffers, and an output current-feedback op amp to implement a variable-gain amplifier in a 14-pin DIP. You need two external resistors to set the maximum gain from 2V/V to 100V/V. The gain-control range is 40 dB from the maximum setting. At 10V/V gain setting, the bandwidth is 165 MHz. $9.26 (1000). **Comlinear Corp,** 4800 Wheaton Dr, Fort Collins, CO 80525. Phone (303) 226-0500. FAX (303) 226-0564. TLX 450881. **Circle No. 411**

Low-voltage SRAMs. The DS2016 is a 2k × 8-bit static RAM (SRAM), and the DS2064 is an 8k × 8-bit SRAM. Both devices operate from 2.7 to 5.5V. At 3V the standby current is less than 50 nA. Access times are 300 nsec when operating at 3V and 150 nsec when operating at 5V. The devices operate from −40 to +85°C and come in 600-mil DIPs or 300-mil SOIC packages. In DIPs, DS2016, $3.30; DS2064, $7 (1000). **Dallas Semiconductor,** 4401 S Beltwood Pkwy, Dallas, TX 75244. Phone (214) 450-0448. FAX (214) 450-0470. **Circle No. 412**

Flash PLD. The Flash PALC22V10D is an electrically erasable and reprogrammable 22V10 PLD. The chip has a 10-nsec propagation delay and draws 90 mA from a 5V supply. You can program the part using standard PLD programmers such as ABEL, PLDesigner, LOG/iC, and CUPL. You can erase and program the part with the Cypress QuickPro II programmer running version 2.078 or higher. The 24-pin DIP, $15.55 (100). **Cypress Semiconductor,** 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600. **Circle No. 413**

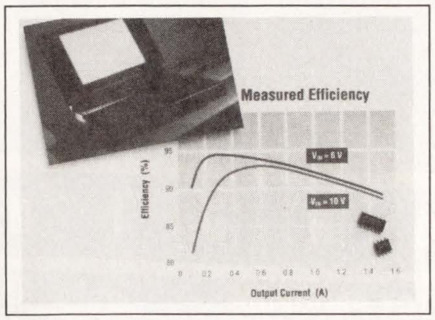
Sampling A/D converters. The ADS-188 and ADS-188A are 12-bit sampling A/D converters in 24-pin DIPs. The hybrids operate as fast as 5 MHz and consume 1.8W operating from ±15 and 5V supplies. Typical harmonic distortion is −73 dB, and the signal-to-noise ratio is 66 dB. The ADS-118 has 3-state outputs, and the ADS-118A features direct adjustment of offset and gain errors. The operating temperature ranges from 0 to 70°C. $203. Delivery, stock to six weeks ARO. **Datel Inc,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356. **Circle No. 414**

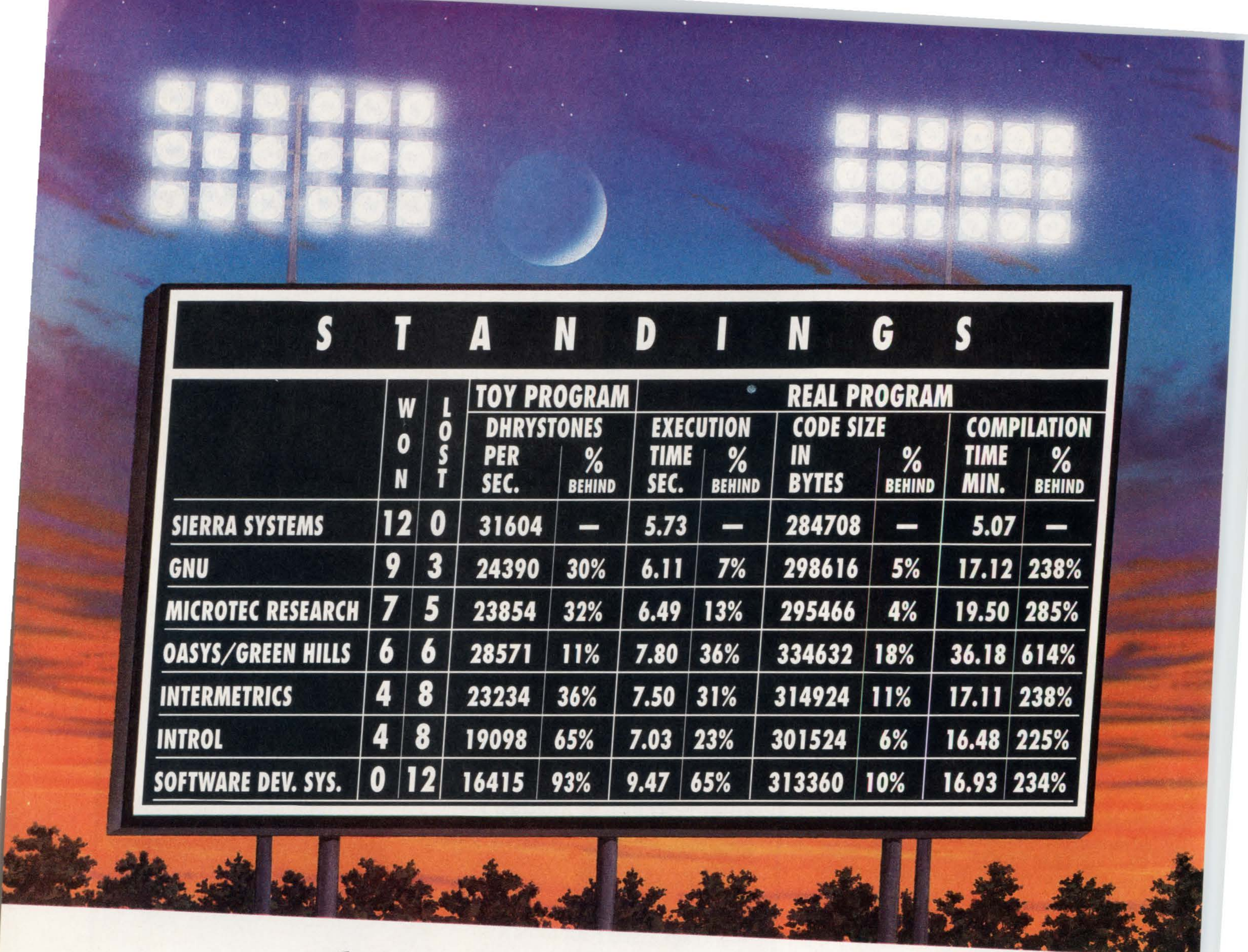
Communications chip sets. The PHY1001 and PHY1002 2-chip sets provide fax, modem, voice, and caller-ID functions. They operate at 14,400 bps, which conforms to V.32bis data and V.17 fax standards. Both chip sets include voice compression as standard. The PHY1002 is a reduced-part version of the PHY1001 for low-power applications. The PHY1002 consumes 450 mW operating and 80 mW in sleep mode. PHY1001, $40; PHY1002, $50 (1000). **Phylon Inc,** 4027 Clipper Ct, Fremont, CA 94538. Phone (510) 656-2606. FAX (510) 656-0902. **Circle No. 415**

Clocked FIFO memories. This series of memories operates as fast as 67 MHz. The SN74ACT7813, SN74ACT7805, and SN74ACT7803 have 64×18-bit, 256×18-bit, and 512×18-bit organizations, respectively. The architecture synchronizes the output- and input-ready flags to the read and write clocks, respectively. SN74ACT7813-40DL, $15.60; SN74ACT7805-40DL, $18.10; SN74ACT7803-40DL, $20.50. **Texas Instruments Inc,** Semiconductor Group (SC-92047), Box 809066, Dallas, TX 75380. Phone (214) 995-6611, ext 3990. **Circle No. 416**

1-GHz frequency synthesizer. The UMA1016xT integrates a 1-GHz prescaler to synthesize frequencies in the 500-MHz to 1-GHz range. The device can change frequencies within 100 μsec. Two separate divider-ratio registers permit the IC to switch from transmit to receive frequencies without reloading data. A 5-Mbps, 3-wire serial interface passes channel information to the chip. $3.60. **Philips Semiconductors,** Box 218, Bldg BAF-1, 5600 MD Eindhoven, The Netherlands. Phone 40 722091. FAX 40 724825. **Circle No. 417**

Synchronous buck regulator. You can combine the Si9150CY synchronous buck regulator controller with a MOSFET half-bridge to implement a 7.5W, 3.3V, or 5V power supply. The chip operates from a 6 to 16.5V dc input voltage and features dual 100-mA output drivers. You can use a switching frequency as fast as 300 kHz. The chip has overcurrent protection and a low-current standby mode. $2 (OEM qty). **Siliconix Power MOSFET,** 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (800) 554-5565, ext 1400. **Circle No. 418**





	WON	LOST	TOY PROGRAM DHRYSTONES PER SEC.	% BEHIND	REAL PROGRAM EXECUTION TIME SEC.	% BEHIND	CODE SIZE IN BYTES	% BEHIND	COMPILATION TIME MIN.	% BEHIND
SIERRA SYSTEMS	12	0	31604	—	5.73	—	284708	—	5.07	—
GNU	9	3	24390	30%	6.11	7%	298616	5%	17.12	238%
MICROTEC RESEARCH	7	5	23854	32%	6.49	13%	295466	4%	19.50	285%
OASYS/GREEN HILLS	6	6	28571	11%	7.80	36%	334632	18%	36.18	614%
INTERMETRICS	4	8	23234	36%	7.50	31%	314924	11%	17.11	238%
INTROL	4	8	19098	65%	7.03	23%	301524	6%	16.48	225%
SOFTWARE DEV. SYS.	0	12	16415	93%	9.47	65%	313360	10%	16.93	234%

68000 Compiler Benchmark Results.

Sierra Systems undefeated on the 68040. Two benchmarks were selected, Dhrystone 2.1 (the Toy program) and the Sierra Systems production C compiler (the Real program). The compiler was selected because both its size and complexity are representative of real-world applications.

The Sierra C™ compiler delivers unchallenged compilation times with industry leading run-time performance on all applications. Add our equally fast QuickFix™ source-level debugger, and you have a package with all the quality, speed, and ease-of-use demanded by today's design teams.

68332 and 68010 standings also available. For more detailed results, additional information, and a competitive edge for your products, call **800-776-4888.**

Won/Lost Record: For each benchmark, the compilers' run-time performances were compared to each other with wins and losses totalled in round-robin fashion. (See Dhrystones and Execution Time columns on scoreboard.)

Compilers: GNU 2.0, Intermetrics 8.0, Introl 3.06, Microtec Research 4.2d, Oasys/Green Hills 1.8.5Rc, Sierra Systems 3.0, Software Development Systems 5.1.

Hosts: 33 MHz 386 Zeos PC and Sun SPARCstation IPC. All compilers were run on the PC, except for GNU and Oasys/Green Hills, which were run on the Sun. Running the Sierra Systems compiler on both host systems allowed the Sun times to be scaled to PC time for the scoreboard.

Target: Motorola VME167, 25 MHz 68040 with caches enabled.

SierraSystems

6728 Evergreen Avenue, Oakland, California 94611
Tel (510) 339-8200 Fax (510) 339-3844

CIRCLE NO. 84

CAE & Software Development Tools

Synthesis tools. For designing programmable logic, the PLDesigner-XL family works with VHDL (VHSIC-Hardware-Description-Language) language entry or an extended version of Minc's Design Synthesis Language. The software is available in three configurations. The Prodigy Series includes the Minc language input and offers single-device software from $2995. The Professional Series offers multiple-device partitioning and schematic interfaces from $4995. The Virtuoso Series has VHDL input and the choice of any two CPLD-(complex PLD) or FPGA-(field-programmable-gate-array) device libraries from $8995. **Minc Inc,** 6755 Earl Dr, Colorado Springs, CO 80918. Phone (719) 590-1155. **Circle No. 449**

Thermal analysis software. The Circuit Board Thermometer version 2.0 has translators for P-CAD, PADS-PCB, Tango, and Orcad circuit-board-layout programs. The Windows software performs conduction, conduction with natural convection, forced convection, and transient thermal analyses. The software interpolates temperature and heat-flow contour plots. $2475. **Lakeview Software Corp,** Laurel Lakes Executive Park, 8377 Cherry Lane, Laurel, MD 20707. Phone (301) 317-0726. FAX (301) 317-0587. **Circle No. 450**

C compiler and development tools. C Transition Pack consists of a compiler and development tools for migrating C applications from version 1.0 to 2.0 of Solaris. Transition packs for C++, Pascal, and Fortran are available. C version, $995; others, from $1995. **Sunpro,** 2550 Garcia Ave, Mountain View, CA 94043. Phone (415) 960-1300. FAX (415) 969-9131. **Circle No. 451**

MMIC element library. Generic Smart Library is a user-definable MMIC (monolithic microwave integrated circuit) element library that can be customized for virtually any analog GaAs-IC foundry. You can fit the parameters for each library model to match the characteristics of the foundry. The library exactly synchronizes electrical element models with physical MMIC element layout representations. From $12,000. **Eesof Inc,** 5601 Lindero Canyon Rd, Westlake Village, CA 91362. Phone (800) 343-3763; (818) 991-7530. FAX (818) 991-7109. TLX 384809. **Circle No. 452**

Model-development software. The Modeltools software package provides on-demand models for development of fully functional hardware simulation for board and system designers. The software features easier data entry, automatic generation of model software, and model verification. It requires the LM-family hardware-modeling system on the network. $9000. **Logic Modeling Corp,** 1520 McCandless Dr, Milpitas, CA 95035. Phone (408) 957-5200. FAX (408) 945-9181. **Circle No. 453**

Software development tools for R3000. The cross-software development tool kit for the Mips R3000 family of RISC (reduced-instruction-set-computer) processors runs on PC-DOS and Unix. It includes an ANSI C compiler, libraries in source code, an assembler, a linker, a locator and a debugger. The compiler works with both hardware and software floating-point operations. Processor-specific optimizations include register allocation, peep-hole optimization, leaf-function handling, and function inlining. Complete tool kit, from $6990; individual components, from $1750. **Boston Systems Office/Tasking,** Norfolk Pl, 333 Elm St, Dedham, MA 02026. Phone (617) 320-9400. FAX (617) 320-9212. **Circle No. 454**

Object-oriented design on Mac CASE. Macanalyst and Macdesigner 3.3 let you apply object-oriented-design methods to development projects in computer-aided software engineering (CASE). Other features include real-time extensions, data modeling, screen prototyping, requirement database, and global data dictionary. The software requires at least 4 Mbytes of RAM and system 6.0, 7.0, A/UX 2.0, or later. Macanalyst/Combo, $995; Macanalyst/Expert, $1595; Macdesigner, $995. Educational pricing available. **Excel Software,** Box 1414, Marshalltown, IA 50158. Phone (515) 752-5359. FAX (515) 752-2435. **Circle No. 455**

Digital-signal-processing software. The Monarch series of DSP software comprises four packages. Digital Filters provides finite-impulse-response (FIR) and infinite-impulse-response (IIR) filter-design methods. Adaptive Filters offers adaptive algorithms for single and multidimensional signals. Siglab is a signals and systems laboratory for DSP to simulate and test designs. Code Generators implement digital filters on DSP μPs. Adaptive Filters, $399; Digital Filters, Siglab, and Code Generator, $99 each. **The Athena Group Inc,** 3424 NW 31st St, Gainesville, FL 32605. Phone (800) 741-7440; (904) 371-2567. FAX (904) 373-5182. **Circle No. 456**

Speech-synthesis-integration tool kit. The Sound Bytes Developer's Kit is a library of subroutines. You use it with the company's Sound Bytes software, which allows you to incorporate speech synthesis into new and existing applications. The software, written in C, converts text into speech and is available for the Macintosh with 2 Mbytes of RAM and system 6.0.x or higher. From $3750. **Emerson and Stern Associates Inc,** 10150 Sorrento Valley Rd, Suite 210, San Diego, CA 92121. Phone (619) 457-2526. **Circle No. 457**

Modem evaluation software. For most industry-standard modems, Taskit provides ready-to-run evaluation scripts for the latest requirement from EIA and CCITT; new test procedures can be added to the package. Modem types covered include V.Fast, V.32bis, V.32, V.22, V.22bis, and Bell 212A. Software with sample test documentation and results, $2450. **Telecom Analysis Systems Inc,** 34 Industrial Way E, Eatontown, NJ 07724. Phone (201) 544-8700. FAX (201) 544-8347. TWX 510-601-5535. **Circle No. 458**

Microprocessor development tools. A set of development tools for Motorola's 16-bit 68000 and 68302 microprocessors include Validate/XEL integrated debugger, an optional optimizing C compiler, an instruction-set simulator, and EL 1600 emulator. The tools are based on the company's emulation-link architecture, which provides network accessibility and a high-level-debugging capability. Each tool, priced separately, $2000 to $15,050. **Applied Microsystems Inc,** Box 97002, Redmond, WA 98073. Phone (800) 426-3925; (206) 882-2000. FAX (206) 883-3049. **Circle No. 459**

CAE tool for MS-Windows. Previously known as Simulab, Simulink is a computer-aided engineering tool for simulating nonlinear dynamic systems. This version uses the Simulink/Matlab open architecture, simulation, modeling, analysis, and design. The software can be "linked" or integrated with other products in windowing systems such as Windows, OSF/Motif, X Windows, and Macintosh. $3995. **The Math Works Inc,** Cochituate Pl, 24 Prime Park Way, Natick, MA 01760. Phone (508) 653-1415. FAX (508) 653-2997. TWX 910-240-5521. **Circle No. 460**

Scientific graphing package. Plotit 2.0 converts data into charts and graphs for analysis. It accepts data from dBase database files, Excel or Lotus 1-2-3 spreadsheet files, or ASCII files. Fastfont technology provides outline fonts and access to third-party fonts. You can choose from more than 60 2-or 3-D or SPQC (Statistical Process Quality Control) graphs including pie graphs, pareto charts, bubble graphs, and fence plots. $495. **Scientific Programming Enterprises,** Box 669, Haslett, MI 48840. Phone (517) 339-9859. FAX (517) 339-4376. **Circle No. 461**

Table-driven cross-disassembler. The XDASM table-driven cross-disassembler for more than 20 common processor families allows you to add tables for future processors. The software automatically assigns label names, deblocks subroutines, inserts assembler directives, and provides multiple cross-reference tables. It also allows full control of the disassembly using a separate TAG file. $249. **Data Sync Engineering,** Box 146, East Stroudsburg, PA 18301. Phone (717) 421-1977. **Circle No. 462**

PLD design software. MacAbel 4.1 provides PLD design on the Macintosh. Based on Data I/O's Abel package, the software reads in a high-level-language description of a circuit. It then automatically optimizes the logic and converts it to a programmer load file that can be used by any JEDEC-compatible programmer. $1995. **Capilano Computing Systems Ltd,** 960 Quayside Dr, Suite 406, New Westminster, BC V3M 6G2, Canada. Phone (800) 444-9064; in Canada, (604) 522-6200. **Circle No. 463**

Logic-synthesis software. The Benchkit utility aids users in determining the capabilities of PLD and FPGA synthesis software. The utility generates random Boolean equations in the format required as input for most universal programmable-logic tools. You specify parameters to control the generation of the random equations. Free. **Minc Inc,** 6755 Earl Dr, Colorado Springs, CO 80918. Phone (719) 590-1155. **Circle No. 464**

Recovery software for Unix. Bart, backup and recovery software for Unix networks, provides file recovery, backup capability, multiple-volume backups, and multiple backups per tape. Licensing fees, $399 to $49,995. **Raxco,** 2440 Research Blvd, Suite 200, Rockville, MD 20850. Phone (301) 258-2620. FAX (301) 330-5756. **Circle No. 465**

ICE for NEC V40 and V50. The UEM in-circuit emulator for NEC's V40/50 microprocessors consists of a full-featured emulator and a source-level debugger for C. The debugger works with many compilers and assemblers, including those from Microsoft, Borland, and Intel. The software works with both 8 and 16-bit versions of the processors. $7000. **Softaid Inc,** 8300 Guilford Rd, Columbia, MD 21046. Phone (800) 433-8812; (410) 290-7760. **Circle No. 466**

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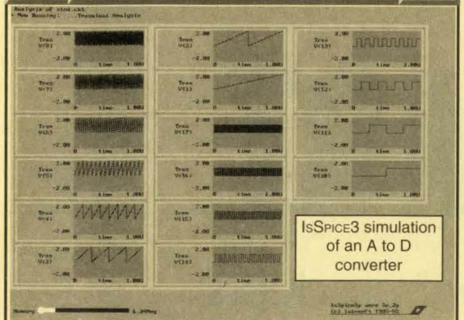

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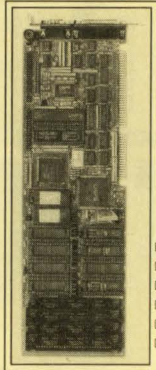

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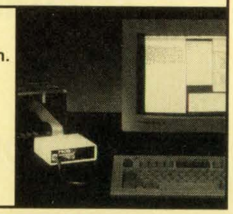

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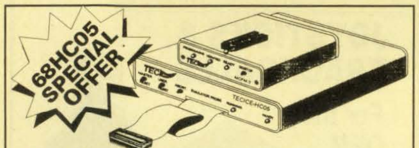

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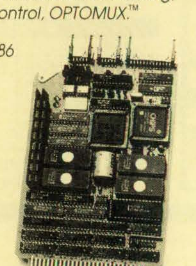

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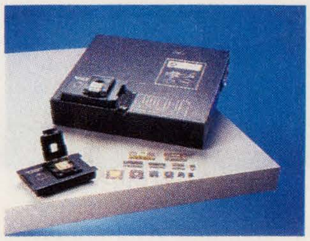

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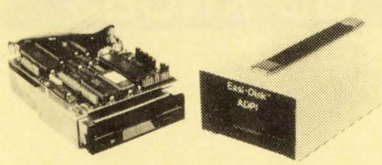

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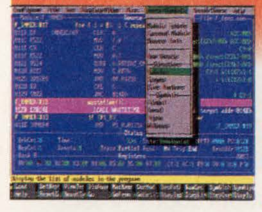

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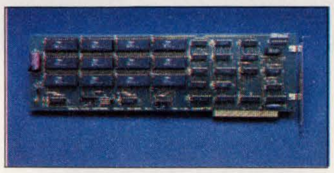

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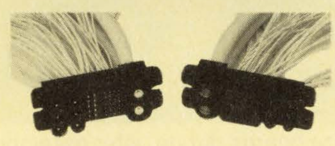

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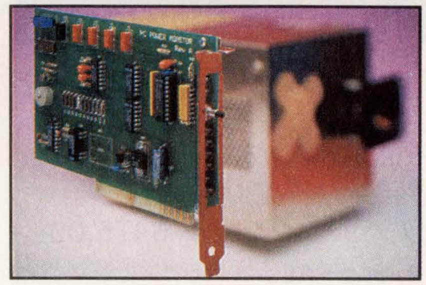

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EDN Magazine	Nov. 12	Oct. 22	COMDEX/WESCON SPECIAL ISSUE • Integrated Circuits • Test & Measurement • Design it Right Series—Part IV
WESCON '92 SHOWGUIDE & PRODUCT SPOTLIGHT		Oct. 9	A free page available to all advertisers running a full page in 2 out of 3 Wescon issues.
EDN Products & Careers	Nov. 19	Nov. 5	CAE Software • EDN's "Innovation Crusade"—Winners Coverage • Communications Technology • Regional Profile: So. California, Nevada
EDN Magazine	Nov. 26	Nov. 5	19th Annual Microprocessor Directory • ASICs • Sensors • EDN's "Innovation Crusade"—Winners Coverage
EDN Products & Careers	Dec. 3	Nov. 19	ICs & Portable Computers • Power Sources • Laptops/Portables • Low-power Design • Regional Profile: Massachusetts, New Hampshire
EDN Magazine	Dec. 10	Nov. 19	INTERNATIONAL PRODUCT SHOWCASE—Vol. 1 • Power Sources • ICs & Semiconductors • Software • Hardware & Interconnect
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Systems Development Engineer

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EDN Magazine Edition

ATLANTA

Loral Information Display Systems, a division of Loral Corporation (NYSE), designer of digital electronic information systems and graphic displays for military applications, has the following immediate opportunities:

DIGITAL DESIGN ENGINEER - BSEE with 8-10 years experience in high speed microprocessor based computer graphics design. Experience in military displays and display processor design preferred. Knowledge of CAE simulation technologies helpful.

MECHANICAL ENGINEER - BSME with 5-10 years experience in military electronic packaging design, analysis and quality testing. Strong background in chassis design, PWBs, CCAs, harness and thermal analysis. Prefer finite element experience with ANSYS.

PROJECT ENGINEER - BSEE with 5 years experience in project engineering or project management in a military electronics development engineering environment. Must have extensive scheduling, budgeting, and customer interface experience. Systems engineering background helpful.

RELIABILITY ENGINEER - BSEE with 5-10 years experience in reliability analysis and predictions, creating reliability test plans and performing stress analysis. Knowledge of Mil Std 217, 781, 785, and 1629 necessary. Background in failure analysis and maintainability a plus.

INTEGRATION ENGINEER - BSEE with 8-10 years experience in hardware/software design experience plus proven experience in Engineering Lab Integration and Testing.

MARKETING ENGINEER - BSEE with minimum 7-10 years experience in technical marketing of military electronic or avionics systems to prime contractors, Air Force and Navy. Prefer specific background in airborne and ground display systems. Responsibilities include generating new business opportunities with prime DOD contractors and Air Force and Navy customers.

Loral Information Display Systems is a progressive company offering unusual growth opportunities in our own office park in NE Atlanta. We provide top industry pay and benefits. If interested, please send or fax resume with salary history to: **Robert C. Hall, Loral Information Display Systems, Dept. EDN015, 6765 Peachtree Industrial Blvd., Atlanta, GA 30360. FAX (404) 448-9163.** EOE, M/F/H/V. U.S. Citizenship required.

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Information Display Systems

EDN-INTERNATIONAL ADVERTISERS INDEX

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CIRCLE NO. 103

CIRCLE NO. 104

EDN-ACRONYMS & ABBREVIATIONS

ADC—analog-to-digital converter
BIOS—basic input-output system
CMOS—complementary metal-oxide semiconductor
CPU—central processing unit
CRT—cathode-ray tube
DMA—direct memory access
DRAM—dynamic RAM
DSP—digital signal processing
ECL—emitter-coupled logic
ECO—engineering change order
EPROM—erasable PROM
FCT—fast cycle time, Quantum Corp's name for its approach to reducing time to volume deliveries
FPGA—field-programmable gate array
HCMOS—high-speed complementary metal-oxide semiconductor
IDE—integrated drive electronics
IEEE—Institute of Electronic and Electrical Engineers
I/O—input-output
ISA—the industry-standard architecture bus used for personal-computer input-output cards
ISO 9001—an International Standards Organization standard covering the methods by which companies ensure quality in all aspects of their operations
JEDEC—Joint Electron Device Engineering Council
LC—inductance-capacitance
LCD—liquid-crystal display
MS-DOS—Microsoft disk operating system
NMI—nonmaskable interrupt
pc board—printed-circuit board
PC—personal computer
PCMCIA—Personal Computer Memory Card International Association
PROM—programmable read-only memory
RAM—random-access memory
RC—resistance-capacitance
RISC—reduced-instruction-set computer
ROM—read-only memory
RS-232C—an Electronic Industries Association standard for serial communication; the most common serial-communication standard in personal computers
SAR—successive-approximation register
SBC—single-board computer
SCSI—small computer systems interface, a high-speed bus used to interface external peripherals to PCs and workstations
6U—a physical size designation for VMEbus boards; a 6U board measures 6.29×9.18 in.
SM-RAM—system-management RAM
SMM—system-management mode
S/N—signal-to-noise (ratio)
SRAM—static RAM
THD—total harmonic distortion
TTL—transistor-transistor logic
VGA—a display or display adapter conforming to IBM Corp's video-graphics-array standard; the lowest common denominator of VGA displays is 640×480-pixel resolution
VLSI—very-large-scale integration
VME—Versa Module Eurocard
ZIF—zero insertion force

Pressure-sensor demo boards offer display choices

Sensors and transducers often seem difficult to use. Many require special bridge and conditioning circuits before they can supply a usable signal. Many of today's sensors incorporate signal-conditioning circuits. Interest in sensors runs high because most of us have to measure the conditions of real things. After temperature, pressure is perhaps the most widely measured physical variable.

Two demonstration kits let you experiment with modern pressure sensors from Motorola. (Although called kits, the two units are sold assembled and tested.) The kits give you a choice of a bar-graph or a digital pressure display. If you have put off investigating pressure sensors, these kits can ease your first experiences.

The bar-graph kit, KITDEV-B129/D, measures pressure in 10 levels of 10 kilopascals (kPa) each, from 10 to 100 kPa. (For reference, 100 kPa is about equal to atmospheric pressure at sea level.) Because the pressure sensor in this kit has two openings, you measure pressure against local atmospheric pressure. By switching your hose connection on the sensor, you can measure vacuum. Two potentiometers let you adjust the sensor's zero and its full-scale range.

The KITDEVB114/D supplies the digital display and is more complex. It provides a microcontroller that drives the liquid-crystal display and auto-zeros the sensor's output. The display shows pressure in 0.1 lb/in.^{2} increments from 0 to 15 lb/in.^{2} Although this sensor also measures pressure relative to local atmospheric pressure, it has only one connection, so you can't measure vacuum. The KITDEVB114/D provides a software listing for the measuring and displaying program, so you can learn what the microcontroller does and how it does it.

Both kits provide a test point that lets you measure the sensor's output voltage, so you can acquire data with a computer or data logger. The kits also supply schematic diagrams, information about the pressure sensor, and an overview of the manufacturer's other pressure-sensor devices. You furnish power sources and plastic tubing with an inside diameter of 0.125 in. to connect your pressure or vacuum source to the sensors. The bar-graph unit requires a power supply between 6.8 and 13.2V dc. The bar-graph kit operates from a 5V dc power supply.

—**Jon Titus**

Cost for the bar-graph kit, KITDEVB129/D, is $50. The price for the LCD kit, KITDEVB114/D, is $95. Motorola Inc, Literature Distribution Center, Box 20924, Phoenix, AZ 85063. Phone (602) 994-6561.

Demo board eases data-acquisition-system design tasks

Designing a complex data-acquisition system doesn't have to be a daunting task. Today's data-converter chips offer capabilities that let you design a data-acquisition system on a small circuit board. Typical of the all-in-one data-acquisition chips is the LM12458, which has been available for some time from National Semiconductor. However, engineers faced with the chip's data sheet may be taken aback by all of its programmable features.

To help ease the job of designing your own data-acquisition system, National Semiconductor also supplies a demonstration board and demonstration software to control it. The LM12458EVAL board occupies a short 8-bit slot in ISA-bus computers, and it lets you acquire data from as many as eight analog signals. You make connections through a 37-pin D-type female connector. You supply the male connector. The board's DIP switches and jumpers lets you choose specific I/O addresses and the proper interrupt for operation, but the board comes preset for an address range (120H) and an interrupt (IRQ2) that won't cause conflicts in most personal computers.

Keep in mind that the board is meant to demonstrate how the chip operates and to let you experiment with its various operating modes. Don't use the board as an add-in card for routine data-acquisition tasks. There is no signal buffering, filtering, or other signal-conditioning circuitry on the board. If after using the demonstration board you choose to specify the LM12458 chip in a design, you'll want to provide your own analog and digital support circuits. The documentation provides an example of the minimum circuitry you'll need.

Because the chip furnishes so many programmable options, the demonstration software is the key. Before you try to use the board, run through the demonstration routine. By doing so, you'll find out more about how you can control the data-acquisition operations and the timing functions on the chip. For example, an on-chip RAM lets you set up an 8-step sampling program that acquires information at specific intervals. You'll be able to program an on-chip 16-bit timer that controls the sampling sequence. The software also lets you examine your data and adjust the program steps, timing intervals, voltage references, and other parameters. You can also save your data-acquisition setups, as well as any data you acquire, in disk files.

The software requires a hard disk, at least 400 kbytes of memory, and MS-DOS, version 3.3 or higher. The demonstration software provides pull-down menus, and you can point to menu items with a mouse. Extensive help screens give you information on a myriad of topics involving timing, setting up the board, and the chip's pinouts. Unfortunately, if you need help, you have to leave the part of the software you're working on and go to the help menu. There is no context-sensitive help available. However, because the help information is complete and in concert with the demonstration routines, you'll be able to figure out how to use the board.

After you become familiar with the operations of the converter board and the chip, you can access the chip's internal registers and memory locations on your own. I suggest using C, Basic, or another language that lets you transfer and command words to and from the device with relative ease. Although the chip can operate in either 16- or 8-bit parallel modes, the board supplies the chip in the 8-bit configuration. If you're not willing to face dozens of status and control bits, internal registers, and an internal FIFO memory, the demonstration board may not help in your design. Instead, consider an off-the-shelf board that supplies its own driver software.

However, if you feel comfortable programming control bytes and bits, both the chip and the board provide a powerful way to get the data-acquisition system you require with a lot of flexibility built in. The board provides an inexpensive introduction to designing your own data-acquisition system from the chip level on up. You can purchase the board from any National Semiconductor distributor, worldwide.

—Jon Titus

LM12458EVAL board, National Semiconductor. Phone (800) 272-9959, (408) 721-4902. FAX (408) 721-6346. $225.