

EDN[®]

Europe's Electromagnetic
Compatibility Law pg 57

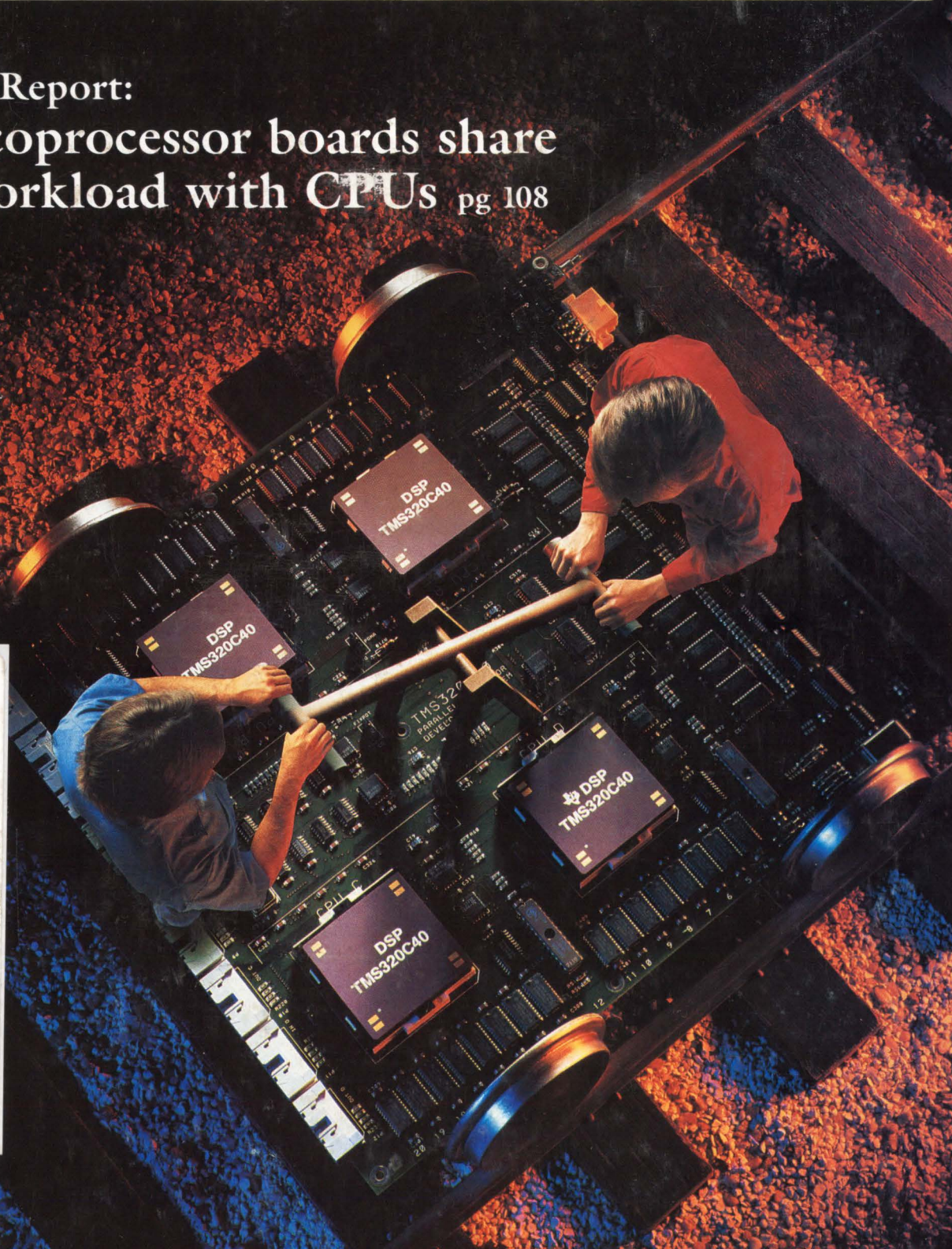
High-density PLD
architectures pg 75

Windows-based engineering
software pg 130

Writing Spice models pg 149

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report: DSP coprocessor boards share the workload with CPUs pg 108



Real-Time Software Performance Analysis and Test Coverage



HMI's Performance Analysis Card (PAC) provides real-time software performance analysis and real-time software test coverage for all HMI-200 series in-circuit emulators. This option operates completely transparent to the system under test and collects its data in real-time to establish a true profile of the software execution.

Features:

- Hardware implemented
- Up to eight modules can be defined
- Histograms for each module are displayed
- Minimum, Maximum and Average time duration for each module displayed
- Coverage mode displays which pieces of the code did and did not execute
- Trace data has a time stamp

Benefits:

- More efficient code produces higher performance products for your company
- Better tested code eliminates bugs generated from untested code and creates higher quality software for your company
- The Emulator and Performance Analysis together shorten the design cycle time allowing your company to have its window of opportunity in the marketplace

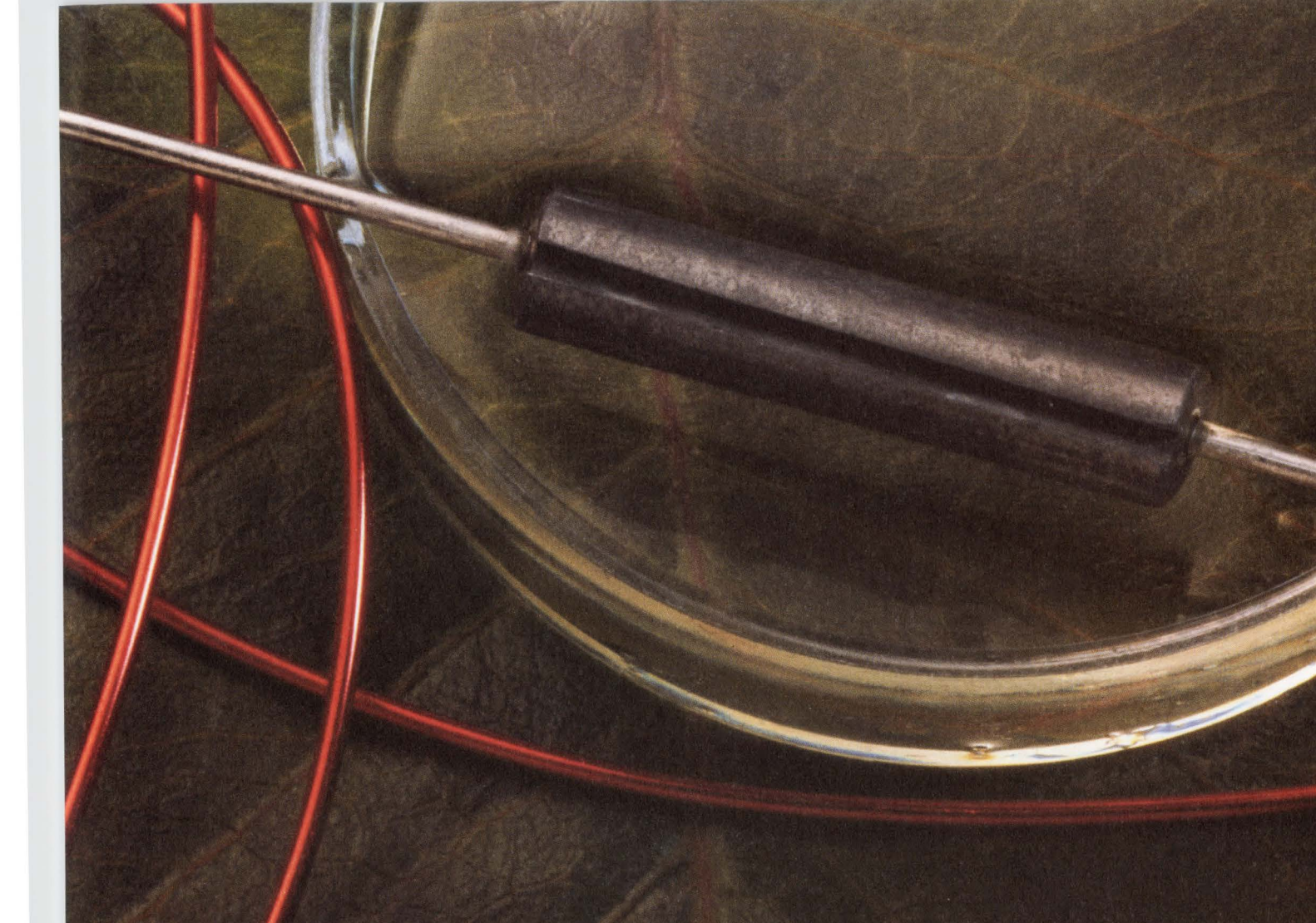
Available Emulators:

68000	68030	68340	68HC11 Family	8085
68008	68302	6809/6809E	includes D1 & F3	64180/Z180
68010	68331	68HC001	DS5000	Z80
68020	68332	8051 Family	8096/80196 Family	



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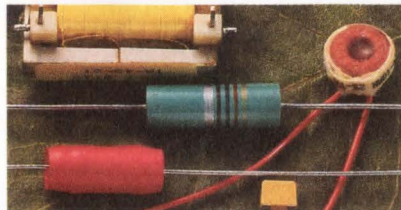
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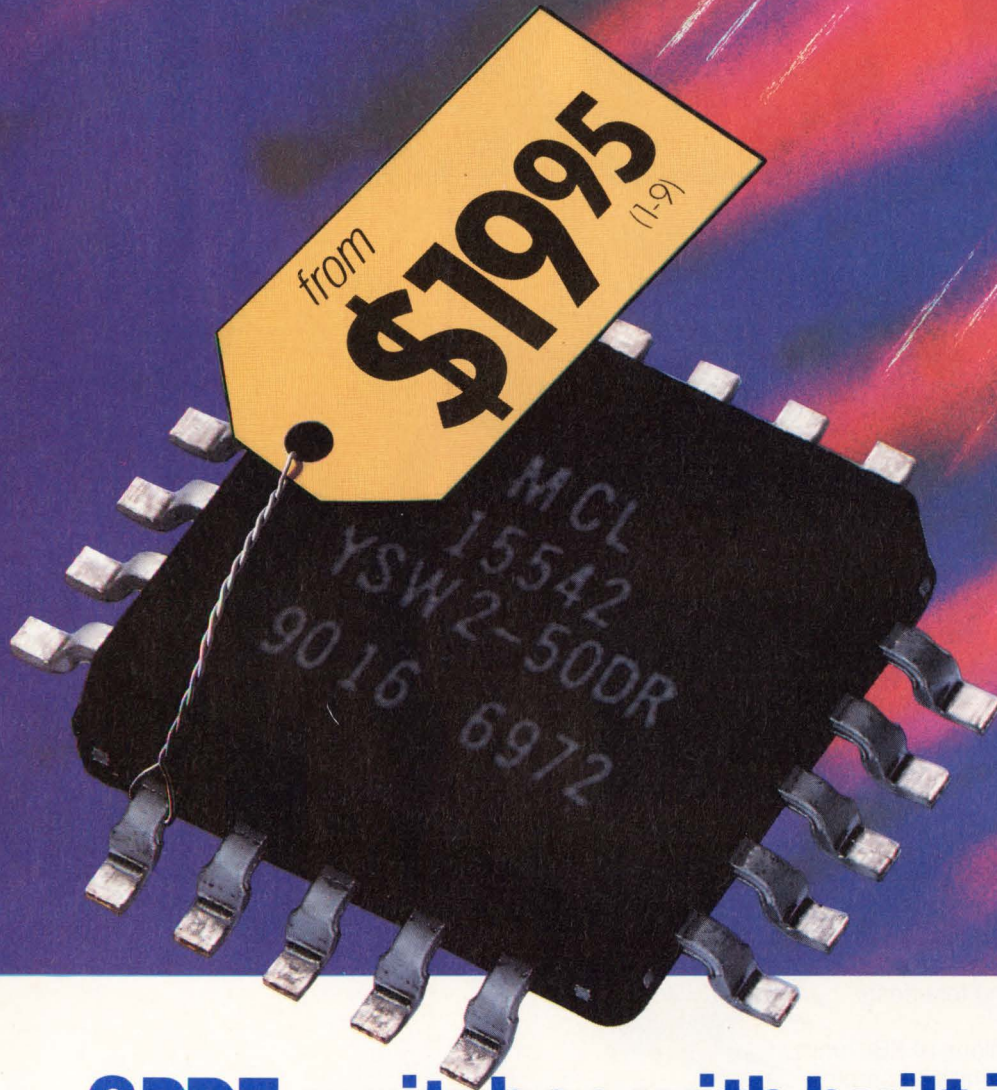


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SPECIFICATIONS

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	ZYSW-2-50DR (connector)		\$59.95
	YSWA-2-50DR (pin)	Absorptive	\$23.95
	ZYSWA-2-50DR (connector)		\$69.95

Frequency, (MHz)	50	100	dc-500	1000	500-2000	2000-5000
Insertion loss, typ(dB)	0.9	1.1	0.9	1.1	1.3	1.4
Isolation, typ (dB)	65	54	50	37	40	28
1dB compression, typ (dBm @ in port)	20	18	20	18	20	24
RF input, max dBm (no damage)	22	20	22	20	22	26
VSWR (on), typ	1.4	1.25	1.4	1.35	1.4	1.5
Video breakthrough to RF, typ(mV p-p)	30	30	30	30	30	30
Switching speed, typ (nsec)	3.0	3.0	3.0	3.0	3.0	3.0

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SBL SPECIFICATIONS (typ).

Model	Frequency (MHz)	Conv. Loss (dB)	Isolation (dB)		LO Level (dBm)	Price, \$ ea. (10 qty)
			L-R	L-I		
SBL-1	1-500	5.5	45	40	+7	4.50
• SBL-1X	10-1000	6.0	40	40	+7	6.25
SBL-1Z	10-1000	6.5	35	25	+7	7.25
SBL-1-1	0.1-400	5.5	35	40	+7	7.25
SBL-3	0.025-200	5.5	45	40	+7	7.25
• SBL-11	5-2000	7.0	35	30	+7	18.75
SBL-1LH	2-500	5.8	68	45	+10	5.50
SBL-1-1LH	0.2-400	5.2	64	52	+10	8.25
• SBL-1XLH	10-1000	6.0	40	55	+10	7.25
SBL-2LH	5-1000	5.9	61	54	+10	8.25
SBL-3LH	0.07-250	4.9	60	53	+10	8.25
• SBL-11LH	5-2000	7.0	45	30	+10	19.75
SBL-1MH	1-500	5.5	45	40	+13	9.80
SBL-1ZMH	2-1100	6.5	40	25	+13	11.70

• IF not DC coupled

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with extra long life due to unique HP monolithic diode construction, 300°C high temp. storage, 1000 cycles thermal shock, vibration, acceleration, and mechanical shock exceeding MIL requirements.



On the cover: Faster coprocessor boards accelerate your computer's speed by keeping DSP (digital signal processing) functions on track while the main processor performs low-speed chores. EDN examines 38 DSP coprocessor boards and the technological trends they represent. See our Special Report on pg 108. (Photo courtesy Texas Instruments Inc; photography, Rusty Hill; art direction, Ken Martin)

SPECIAL REPORTS

DSP coprocessor boards 108

The technology in these number crunchers is developing so fast that about the only things moving faster are the instructions and data they handle. Besides faster μ Ps, architectural innovations—especially parallel and pipelined processors—are adding to the boards' speed. But as is so often the case, software is struggling to keep pace.—*Dan Strassberg, Associate Editor*

Windows-based engineering software 130

The PC is the most popular computer for engineering development work, but lack of graphics-display and printing standards has blocked developing appropriate workstation-class engineering software. Windows 3.0 opens the flood gates.—*Steven H Leibson, Executive Editor*

DESIGN FEATURES

Techniques let you write general-purpose Spice models 149



By incorporating flexibility into your Spice models, you'll develop a library of accurate models that you can adapt for many applications, rather than reinventing the wheel every time. An example of such a model is a universal power converter.—*David Caldwell, Consultant*

Phase compensation extends op amp stability and speed 181

Because most op amps lack provision for altering internal phase compensation, circuit designers often add external compensation to counter the effects of capacitance loading and parasitic capacitance and inductance.—*Jerald Graeme, Burr-Brown Corp*

Continued on page 7

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TECHNOLOGY UPDATES

European EMC regulations: Europe lays down EMC Law 57

A law regulating the electromagnetic compatibility of many products takes effect in Europe on January 1, 1992. Deciding how to make the products conform will be up to the design engineer.
—*Brian Kerridge, European Editor*

High-density PLD architectures: Family tree sorts out high-density PLDs 75

Bringing order to the welter of high-density programmable-logic devices is no easy task. After conferring with experts, EDN bravely offers this hopefully comprehensive and extensible overview.—*Charles H Small, Senior Editor*

EDITORS' CHOICES

CMOS monolithic 5-tap, delay-line IC 93

Surface-micromachined acceleration sensor 95

PRODUCT UPDATE

Low-power, 1.8-in. hard-disk drive 99

NEW PRODUCTS

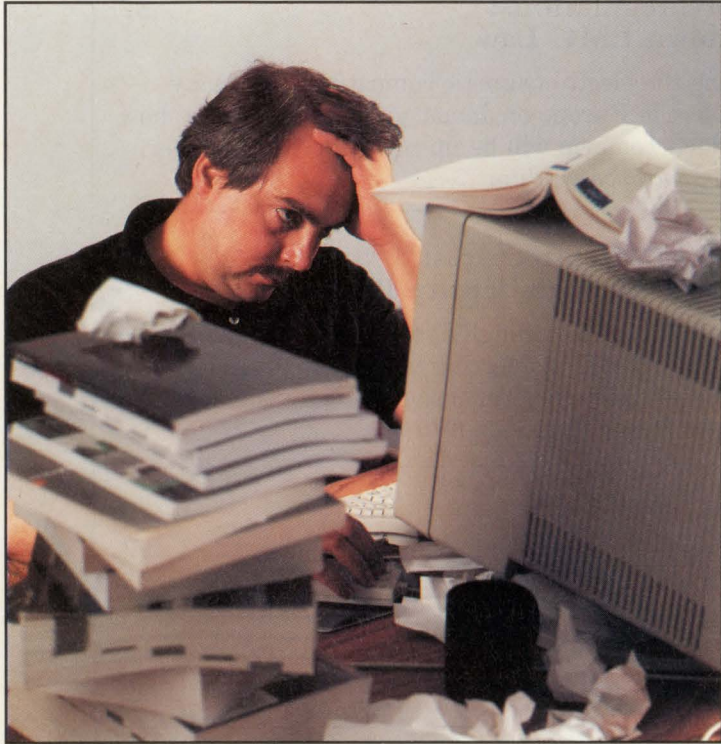
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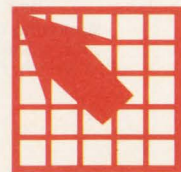


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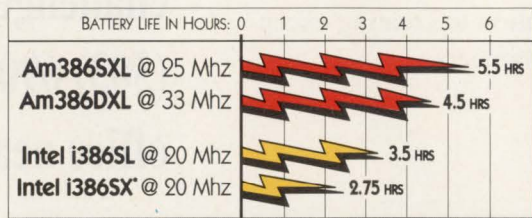
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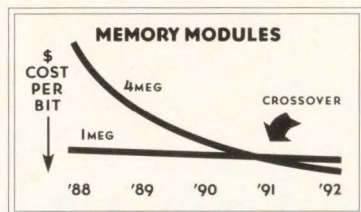
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IN MEMORY MOD CROSSOVER HAS J

You've heard the old saying, "we'll cross that bridge when we come to it." Well, we have.

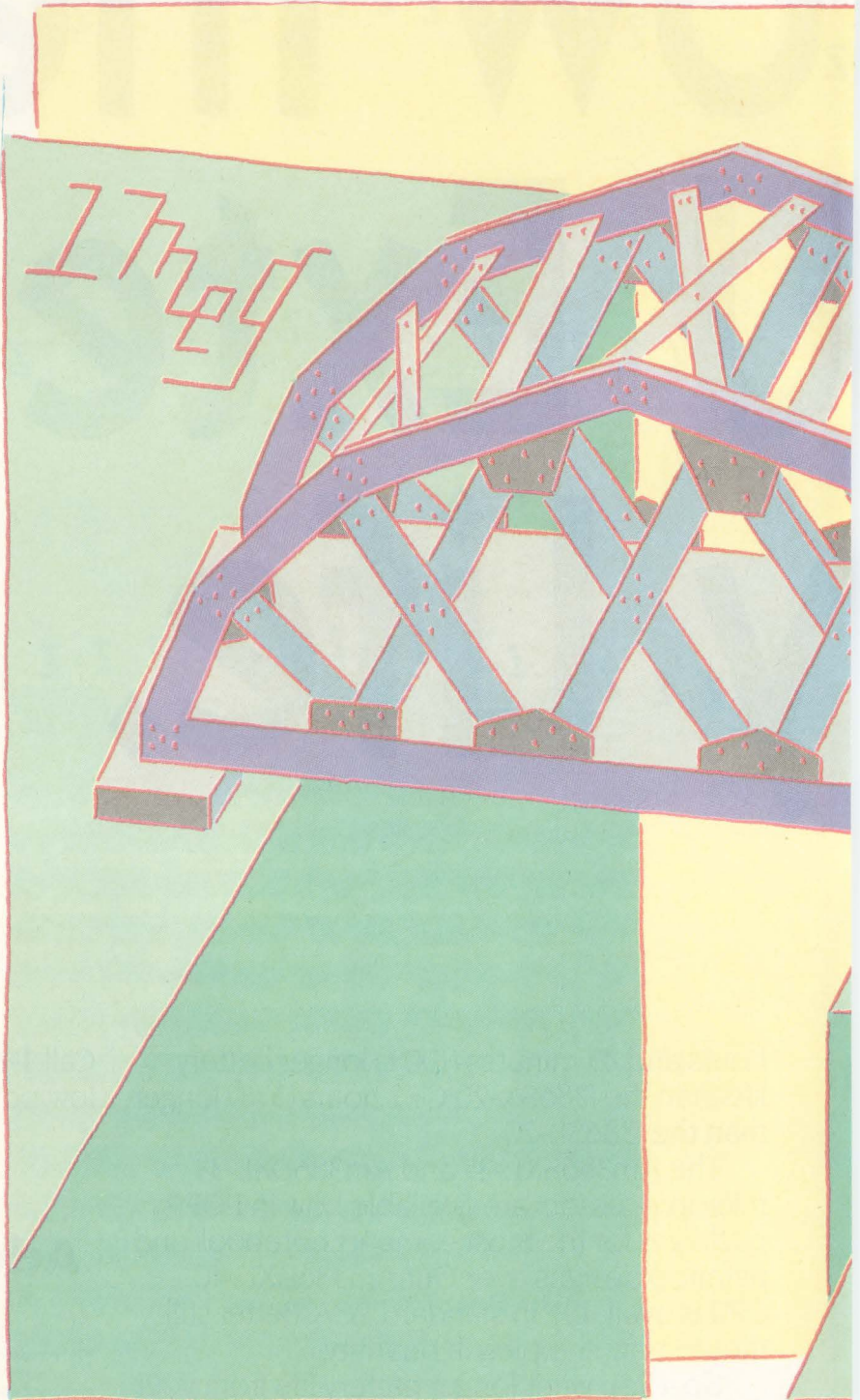
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1	KMM591000AN	1M x 9
4	KMM584000A	4M x 8
4	KMM594000A	4M x 9
4	KMM5321000A	1M x 32
4	KMM5331000A	1M x 33
4	KMM5361000A	1M x 36
8	KMM5322000A	2M x 32
8	KMM5332000A	2M x 33
8	KMM5362000A	2M x 36

Samsung is one of the world's leading manufacturers of both DRAMs and memory modules. Our outstanding quality, reliability, and availability have helped us gain this leading position.

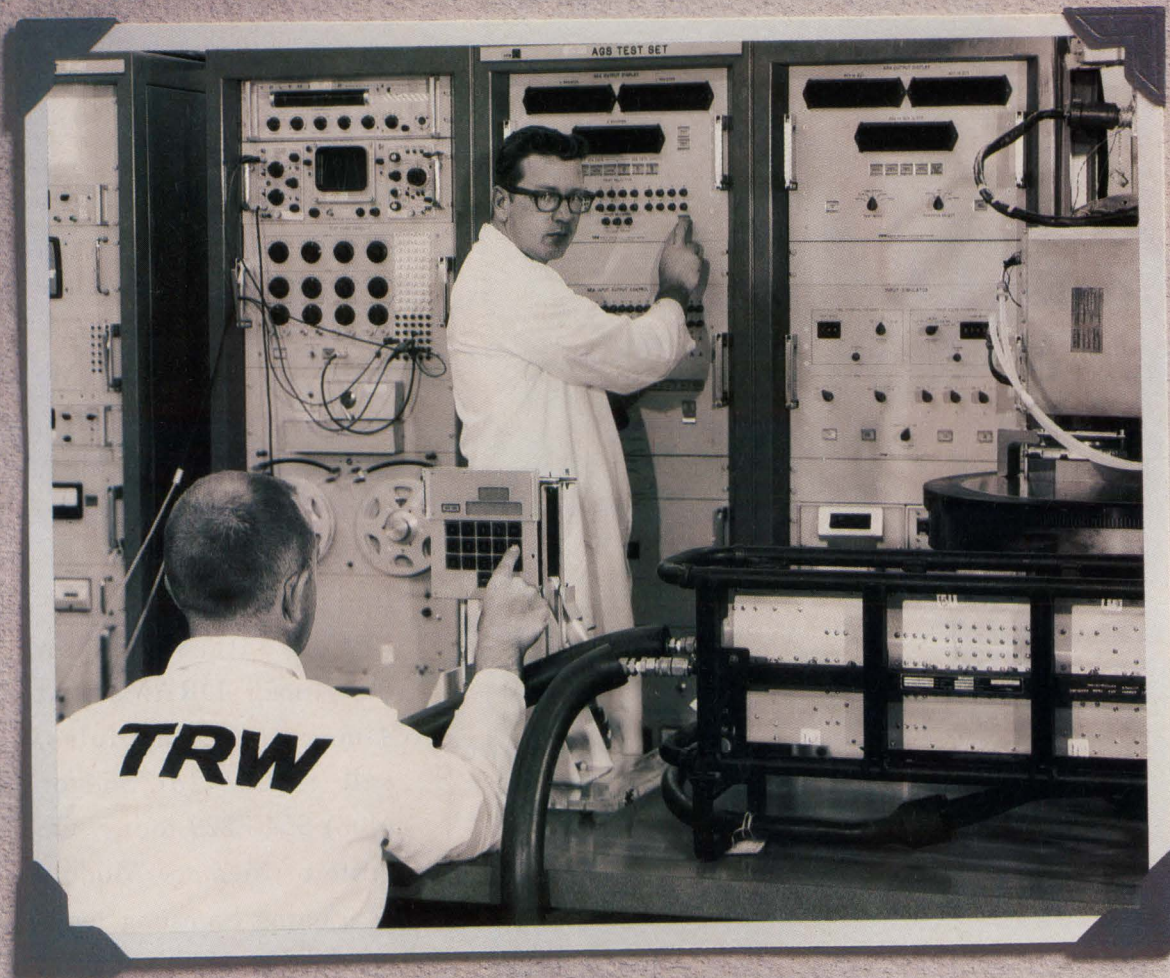
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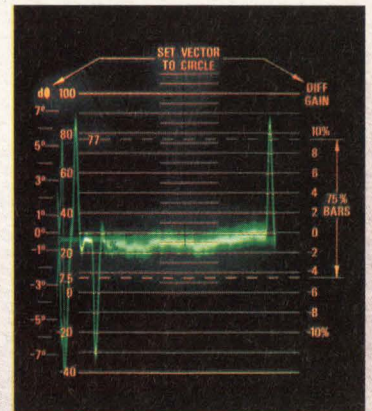
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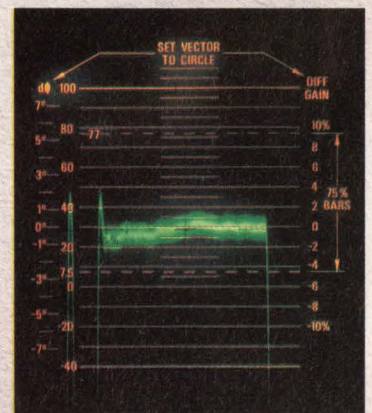
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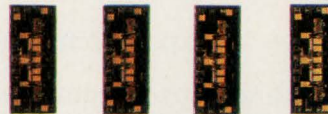
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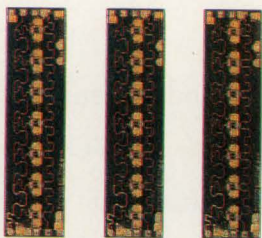
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EDITED BY SUSAN ROSE

VARIABLE-GAIN AMPLIFIER KEEPS BANDWIDTH CONSTANT

You can vary the gain of Analog Devices' AD600 and AD602 dual amplifiers from 0 to 40 dB and -10 to 30 dB, respectively, without affecting the 35-MHz, 3-dB bandwidth of the device. The amplifiers comprise a fixed-gain amplifier preceded by a variable attenuator. The attenuator is made up of a 7-section R-2R ladder network, which continuously interpolates between the tap points. The result is very accurate gain; the gain error is ± 0.5 dB max at the extremes of the voltage-control range and ± 0.2 dB max in the center. The attenuator also prevents large input voltages from reaching the fixed-gain stage, letting its design be optimized for low noise. This fact combined with the linearity of both the attenuator and fixed-gain stages leads to low noise and THD specifications of $1.4 \text{ nV}/\sqrt{\text{Hz}}$ and -60 dBc, for $\pm 1\text{V}$ outputs, respectively.

The amplifiers implement, in terms of dB, a linear gain law. For example, applying a gain-control voltage of -0.625 to +0.625V, the gain of the AD600 increases linearly from 0 to 40 dB. Group delay is stable and typically ± 2 nsec. The amplifiers are optimized for driving flash ADCs in ultrasound applications, but also apply to those circuits that require a combination of precise gain, low noise and distortion, and wide bandwidth. Each amplifier dissipates a maximum of 125 mW. The \$15 (100) amplifiers are available in either 16-pin DIPs or SOICs, and operate over a 0 to 70°C temperature range. Analog Devices Inc, Wilmington, MA, (617) 937-1428, FAX (617) 821-4273.—Anne Watson Swager

COMBINATION OPTICAL DRIVE FITS 3½-IN. FORM FACTOR

The 3½-in. OD-3000 multifunction optical drive stores 128M bytes using MO (magneto-optical) technology and can read optical ROM (O-ROM) disks. The MO media can withstand 10 million write cycles and still record data reliably, where other rewritable optical technologies typically limit media to 10,000 write cycles. The drive features a 3000-rpm rotational speed that results in an average rotational-latency spec of 10 msec. The drive requires an average of 42 msec to seek to data. Other key specs include 11W power dissipation during read/write operations and 2.6W when the drive is inactive. The drive can read data continuously from disk at 640k bytes/sec and write data continuously at 203k bytes/sec. The drive costs \$1050 (1000) and the rewritable media costs \$60 per disk. Teac America Inc, Montebello, CA, (213) 726-0303, FAX, (213) 727-7621.—Maury Wright

SCSI BUS MONITOR PROVIDES MENU-DRIVEN DEBUGGING

For \$895, you can buy Workstation Products Inc's Pathfinder 1000 SCSI bus monitor, which analyzes the activity on your bus- or debug-driver software. Plug this device between your SCSI bus and an ASCII terminal to achieve nonintrusive synchronous or asynchronous monitoring. The device does not use an address on the SCSI bus. In its run mode, the monitor captures commands and data until its event buffers are full. In continuous mode, the monitor continues to capture data until you stop it. In trigger mode, you can specify the condition under which the device begins or stops capturing data. The monitor comes with 2 kbytes of memory, a power supply, manual, and a 6-in. SCSI cable with a 50-pin connector. A monitor with 8 kbytes of memory costs \$995. Workstation Products Inc, Richardson, TX, (214) 669-9587.—J D Mosley

NEWS BREAKS

LOGIC-ANALYZER FAMILY BETTERS PRICE/PERFORMANCE RATIO

The TA4000 series of logic analyzers from Thurlby-Thandar embodies a range of advanced features at a bundled price substantially below competitor's products. Three models offer a choice of 32, 48, or 80 channels. Asynchronous sampling is at 100 MHz max across all channels, or at 400 MHz max across 8 or 16 channels. Memory depth at 100- and 400-MHz sampling is 2 and 8 kwords, respectively. A 5-nsec glitch capture operates on eight channels without loss of memory depth. Synchronous sampling is at 50 MHz max across all channels, and includes an 8-level branching-trigger facility that steps at up to 20 nsec. Optional disassemblers cover a range of 8-, 16-, and 32-bit μ Ps. In addition to internal nonvolatile memory, you can store 512 kbytes of data on a front-panel plug-in memory card. Included as standard in the price are interfaces for IEEE-488, Centronics, RS-232C, and composite video. The 32-, 48-, and 80-channel logic analyzers cost £2495, £2995, and £3995, respectively. Disassemblers cost £195. Thurlby-Thandar Ltd, Huntingdon, UK, (480) 412451, FAX (480) 450409.—Brian Kerridge

ENGINEERING SPREADSHEET WORKS WITH PICTURES

If you've adapted Lotus 1-2-3 to help you analyze data and complex functions, you've sacrificed the visual impact of looking at plots, graphs, and curves. DSP Development Corp's Dadisp (Data analysis and display) provides the spreadsheet's utility while maintaining the visual effect of your data. The data analysis software, which runs on PCs and under the X-Window system on most common workstations, accepts data from numerous sources, including ASCII and binary file formats and many data-measurement and -acquisition devices. Additionally, you can manually enter data sets into a spreadsheet-like table. Once entered, you view and manipulate the data either graphically or in tables. The software includes a range of mathematical, statistical, and engineering functions and lets you create and add custom functions as needed. Special functions include contour plotting, density plots, spectral 3-D plots, and 4-D plots. The user interface provides as many as 100 windows that operate as cells in the X-Y dimension of a 3-D spreadsheet; changing data in the Z-dimension of a cell causes the software to recalculate all dependent data in other cells. You can overlay data and zoom in and out of windows as needed. The software starts at \$895. The PC version costs \$1695. DSP Development Corp, Cambridge, MA, (617) 577-1133, FAX (617) 577-8211.—Michael C Markowitz

DRIVERS LET YOU COMPARE DRAWINGS IN AUTOCAD

Nth Graphics's Nth Drive display-list processing software and Nth Engine display-controller drivers now include a drawing management and viewing module called Nth View/AC, which lets you open an unlimited number of AutoCAD .DWG files for viewing and plotting without leaving your active drawing. This module produces display-list zooms and real-time pans. An icon-based interface and a command window called the Top N provide pop-up control of your screen. Each drawing you add to the screen appears in a window that you can size, move, and overlap onto other windows. In addition, a garbage-collection scheme works continuously in the background to purge the display list of each vector you erase or move during an edit session. The display controller with a suite of drivers starts at \$995. The processing software sells for \$595. Both products include the drawing management module. Nth Graphics Ltd, Austin, TX, (800) 624-7552 or (512) 832-1944, FAX (512) 832-5954.—J D Mosley

A REVOLUTIONARY ADVANCE IN SPARC MULTIPROCESSING.

The industry's first integrated SPARC® multiprocessing solution — the CY7C605 Multiprocessing Cache Controller/MMU.

High-performance systems designers have migrated to RISC in a race for performance. Just as rapidly, there is a movement to multiprocessing, which represents the most cost-effective way to load more power into a single system.

Multiprocessing RISC design is not simple. There are substantial technological challenges, particularly in the area of multi-level memory systems.

Now we offer a breakthrough to help you implement multiprocessing systems rapidly.

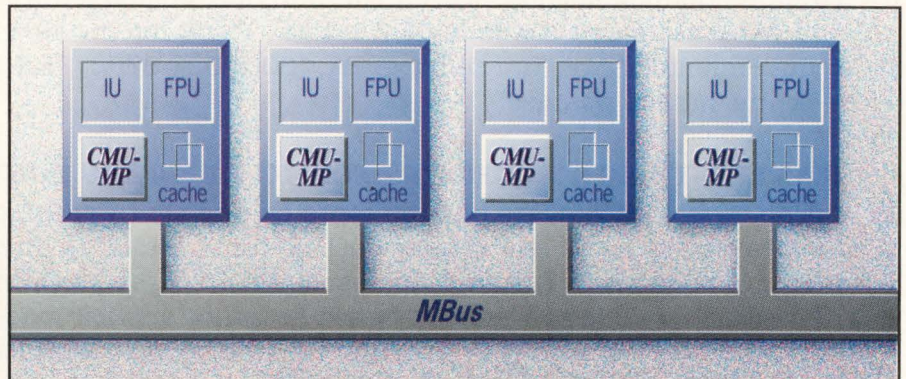
Cache coherency without stealing processor cycles — a leap in performance.

Maintaining cache coherency is one of the biggest problems to solve in shared memory multiprocessing systems.

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NEWS BREAKS

DESIGN SERVICE VALIDATES HIGH-SPEED INTERCONNECTS

AMP is now offering design analysis and support through AMP Interconnection Systems to provide performance prediction and validation of critical high-speed digital and analog systems. This service can benefit any design that includes fast-edge-rate logic requiring transmission-line performance through the interconnects. The analysis capabilities include critical net simulation, crosstalk and noise margin prediction, timing verification, and EMI/EMC, thermal, and power-distribution analysis. Services include connector and subassembly characterization and active-device modeling; connector, cable, net-topography, system-impedance, and layout-rules recommendations; waveform analysis; components placement optimization; and backplane and board layout design. Price for the service varies with customer requirements. AMP, Harrisburg, PA, (800) 522-6752, FAX (717) 986-7575.

—Anne Watson Swager

RASTER-IMAGE ACCELERATOR IC RENDERS FONTS IN REAL TIME

The D7001 IC renders outline fonts on the fly in graphics-display and page-printer applications. The IC can render outline fonts scaled to any size fast enough for laser printers to print at full engine speeds of 17 pages per minute and slower. A single IC can also be used in mother-board graphics applications to directly drive WYSIWYG (what you see is what you get) display and printer engines. You can use the IC in applications with fonts based on Bezier curves, B-spline curves, and vectors. The chip includes multiple filling algorithms to handle both Roman characters and Kanji glyphs. For 12-point type at 300-dpi-resolution fonts, the IC can render more than 7500 cps. Available now for \$35 samples, the IC comes in a 144-pin quad flatpack. Destiny Technology Corp, Milpitas, CA, (408) 262-9400, FAX (408) 262-0221.

—Maury Wright

GATE-ARRAY FAMILY OFFERS HIGH I/O-TO-GATE RATIO

The HG62S gate-array family from Hitachi offers as many as two I/O pins for each 100 used gates. Family members come in sizes from 14,451 to 34,797 raw gates, with 160 to 240 I/O pads. The array uses 0.8- μ m, 2-layer metal CMOS technology, has input buffers with 0.8-nsec propagation delay and output buffers with 1.8-nsec delay and 24-mA drive. Internal gate delays are 0.3 nsec for a 2-input power NAND with a fanout of two. The devices are available in EIAJ plastic quad flatpacks in 64- to 208-pin sizes at a cost of \$0.07 to \$0.10 per pin (10,000). Hitachi America Ltd, Brisbane, CA (415) 589-8300, FAX (415) 583-4207.—Richard A Quinnell

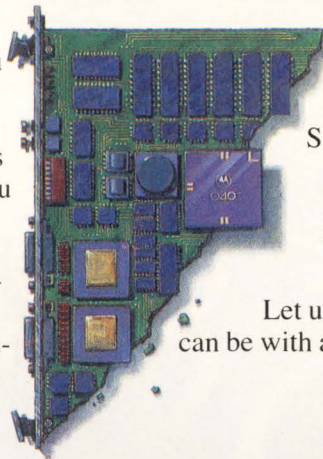
DEVICE CONVERTS CMOS SRAM INTO NONVOLATILE MEMORY

More than just a power source for static RAMs (SRAMs), the bq2502 Integrated Backup Unit from Benchmarq provides power monitoring and switching for one or two banks of RAM. This encapsulated DIP module contains a nonvolatile-SRAM controller chip and a 3V lithium battery. To avoid accidental discharge and simplify handling procedures, the manufacturer ships each module with its battery-output pin electrically isolated. After installation, the module monitors V_{CC} to detect an out-of-tolerance power supply, switches to the internal battery supply if V_{CC} decays, write-protects the memory during power failures and during system power-up, then switches back to the V_{CC} supply when reliable operation resumes. Priced at \$6 (1000), these modules come in 12-pin DIPs that are less than 0.375-in. tall. Benchmarq Microelectronics, Carrollton, TX, (214) 407-0011, FAX (214) 407-9845, contact John Landau.—J D Mosley

Why Settle for 1/2 an '040 Board?

You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPS, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the

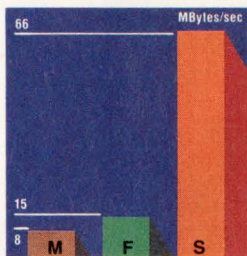


SV430 outperforms every other SBC on the market by as much as 150%.

Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

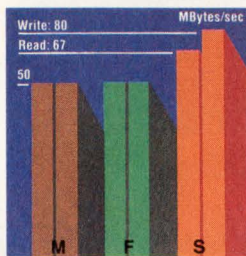
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!

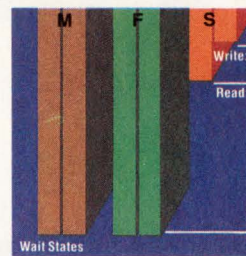


VME Transfers
VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison.

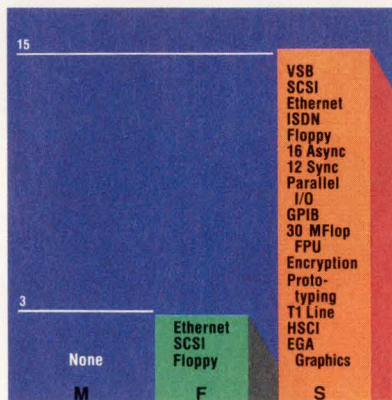
Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



DRAM Burst Rates
A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



DRAM Random Accesses
Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.

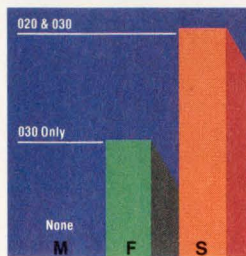


I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.

Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

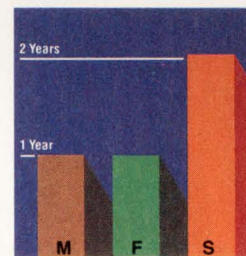
VME64 is a trademark of Performance Technologies, Inc.



'020/'030 Compatibility

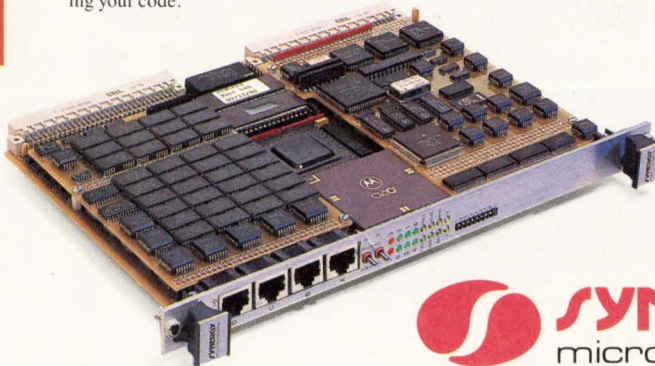
Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and

'030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Synergy Microsystems, Inc., 179 Calle Magdalena, Encinitas, CA 92024 (619) 753-2191 FAX: 619-753-0903

FILTERS



dc to 3GHz from \$1145

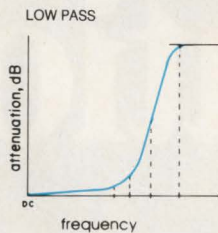
lowpass, highpass, bandpass, narrowband IF

- less than 1dB insertion loss • greater than 40dB stopband rejection
- 5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • meets MIL-STD-202 tests
- rugged hermetically-sealed pin models • BNC, Type N; SMA available
- surface-mount • over 100 off-the-shelf models • immediate delivery



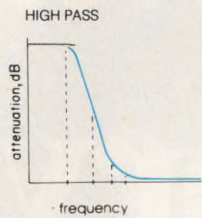
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB)		fco, MHz (loss 3db)	STOP BAND, MHz (loss >20dB) (loss >40dB)		VSWR pass-band typ.	VSWR stop-band typ.	PRICE \$ Qty. (1-9)
	Min.	Nom.		Max.	Min.			
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



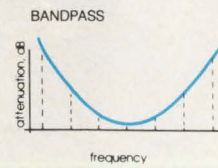
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB)		fco, MHz (loss 3db)	STOP BAND, MHz (loss >20dB) (loss >40dB)		VSWR pass-band typ.	VSWR stop-band typ.	PRICE \$ Qty. (1-9)
	Min.	Min.		Min.	Min.			
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



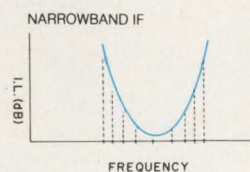
bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB)		STOP BAND, MHz (loss > 10 dB) (loss > 20 dB)				VSWR 1.3:1 typ. total band MHz	PRICE \$ Qty. (1-9)
		Max. F1	Min. F2	Min. F3	Max. F4	Min. F5	Max. F6		
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB		STOP BAND, MHz I.L. > 35dB		PASS-BAND VSWR Max.	PRICE \$ Qty. (1-9)
			F5	F6	F7	F8-F9		
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95



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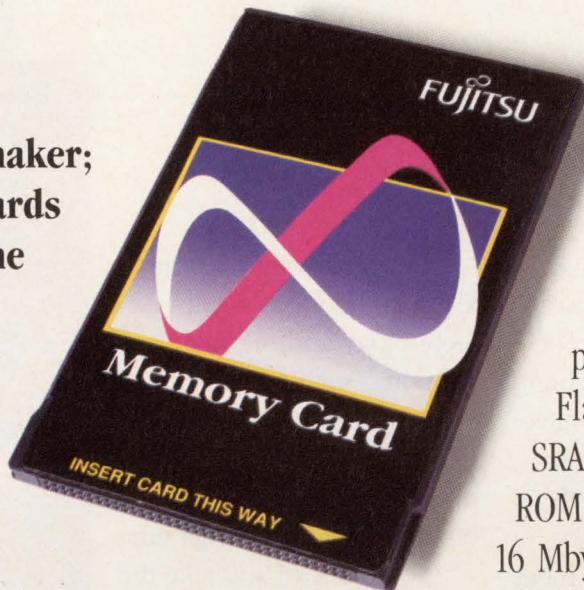
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Cadence	Sun/SPARC Solbourne	Sun OS 4.1.1 Verilog 1.5C	Simulation Fault grading Design verification
IKOS		4.0 up	Simulation Fault grading
Mentor Graphics	HP/Apollo DNx Series	DNIX 5.03, Sun OS 4.1.1 Digital application 6.1 Digital application 6.3	Capture Simulation Design check
	HP9000 Sun/SPARC Solbourne	Digital application 8.0 (in qualification) Parade	Layout Clock Structures
Synopsys	Sun/SPARC	Sun OS 4.1.1 Interface to Mentor, Valid, Viewlogic	Design synthesis Test synthesis
Valid	Sun/SPARC Sun-3	Sun OS 4.1.1 GED, ValidSIM, RapidSIM	Design capture Simulation Design check
	DECstation 3100 IBM RS6000	ULTRIX, ValidSIM, GED GED, ValidSIM, RapidSIM	
Viewlogic	Sun/SPARC	Sun OS 4.1.1 Workview 4.0	Design capture Simulation
	PC386	DOS 3.3, Workview 4.0	

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CIRCLE NO. 18

Introducing the New Generation 574 A/D



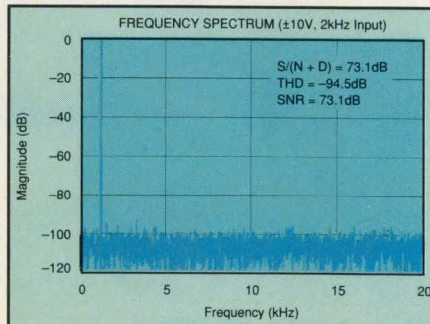
A New Classic

We designed our new 12-bit CMOS A/D converter with you in mind...by adding several innovative features to the standard ADC574 pinout. ADS574 and ADS774 drop into most applications without any system modifications, use minimal power, and operate from a single +5V supply. Complete with on-chip sample/hold, clock, reference, μ P interface, three-state outputs, and internal scaling resistors, ADS574 and ADS774 set a new standard for your design.

A New Standard in Savings

Replace your old standard with our new classic and save...design time, power, board space and money. Designed to operate from a single power supply while still supporting all of the

ADC574 input ranges, ADS574 and ADS774 use only one-fourth the power of that old standard. On-chip sampling combined with our new skinny-DIP package (0.3" wide) or SOIC gives you a lot more board space. And, our pricing sets a new standard—starting at \$14.15*



ADS574

Innovative Features

- Throughput time (acquire & convert)
25 μ s max.....ADS574
8.5 μ s max.....ADS774
- Power consumption
100mW max...ADS574
120mW max...ADS774
- Single +5V supply
- Guaranteed AC, DC performance
- Industry standard input ranges
- Industry standard digital interface
- Compact 0.3" or 0.6" wide 28-pin plastic or ceramic DIP, 28-pin SOIC, die
- From \$14.15*



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We're so convinced that our new parts are the next industry standard—we'll give you the first one free! Just call **1-800-548-6132** for samples and detailed data sheets or contact your local Burr-Brown sales office for assistance.

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SIGNALS & NOISE

Questionable values appear in table

In J D Mosley's article, "Improvements unleash new application areas" (EDN, October 11, 1990, pg 97), there is a mistake in Table 1. The data corresponding to Optical Output Power are in fact the data corresponding to Total Power Dissipation. Values of about 100 mW of optical output power for the IREDS (infrared emitters) are far off the values of commercial products.

I have verified the values of the Motorola IREDS in the manufacturers' data book:

MLED71

Total power dissipation . . . 90 mW
Power output 5 mW

MLED930

Total power dissipation . . . 250 mW
Power output 4 mW

It's impossible to check the other IREDS, but I think they are also wrong.

One of the most important applications for these devices is in optical communications; for a good comparison, an additional column should indicate the speed, such as rise and fall times.

*Francisco J Gabiola Ondarra
Profesor Titular de EU
Dpto-Ingenieria Electronica
ETSI Telecomunicacion
Ciudad Universitaria S/N
Madrid, Spain*

(Ed Note: In Table 1, I used the Motorola Semiconductor values listed in the Motorola data book.)

How discontinued parts affect engineering design

We have had the experience of designing a part (Allegro Microsystems UCN5825B) into a product, and then, just as we introduced the product, found out that the company was discontinuing the part. The part is advertised in the 1991

IC Master, and our distributor [at the time of this writing] had not been informed that the part was discontinued. We found out by accident when calling an applications engineer at the company about another problem.

This part is a BiMOS combination of a shift-register and high-voltage driver. It has four outputs, each of which can handle a 2A drive. Not only is there *not* a second source for the part, no other part even comes close—at least none that we can find. We not only have to redesign the board, but we also have to either change specifications or squeeze in two packages where one served before.

Perhaps we were foolish in using a single-sourced part, even if it has been available for several years, but most of the company's parts in this category are single sourced. Why would anyone ever use any of them if he or she seriously suspected that the parts would be abruptly discontinued?

I understand that the company has been bought by a foreign company. Do the new owners think that this method of operation is going to protect their investment?

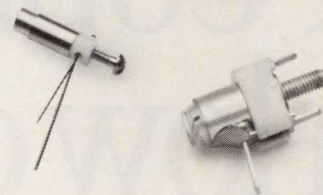
*Norman L Rogers
President
Z-World Engineering
Davis, CA*

HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158, or leave a note via MCI mail at EDNBOS. Or use EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/SOAPBOX, then W to write us a letter. You'll need a 2400-bps or less modem and a communications program set for 8,N,1.

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- Cap ranges: 0.25-1.5 pF;
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- Multiturn resolution at low cost
- Q typically > 2000 to VHF
- Temp coefficient of capacitance:
-50 ± 50 ppm/°C;
0 ± 200 ppm/°C
- Operating temp: -55° to 125°C;
-40° to 100°C

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CIRCLE NO. 20

Sprague-Goodman



Ceramic Dielectric Trimmer Capacitors

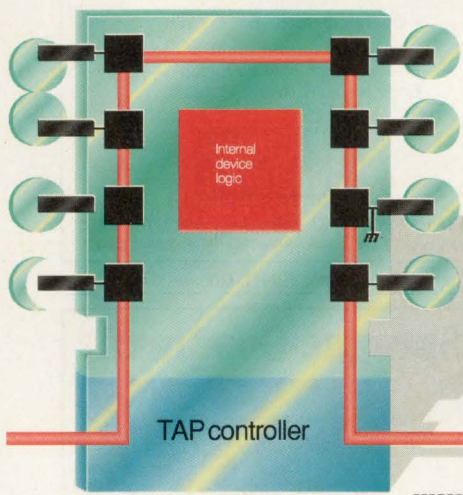
- Rugged 5 & 7 mm types**
Operating temp: -55° to +125°C
Cap ranges: 1.3-2.0 pF to 12-160 pF
- Miniature types suitable for hybrids**
Operating temp: -25° to +85°C
3 series: 2.0 x 1.2 mm; 3.0 x 1.5 mm;
5.0 x 2.0 mm
Cap ranges: 2.5-10 pF to 5.5-40 pF
- Microwave types**
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Designed for volume applications
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CIRCLE NO. 21

People say boundary in low cost, high quality Now you can test that



Find common manufacturing faults without test pattern libraries or physical test access with boundary-scan design and VICTORY software.

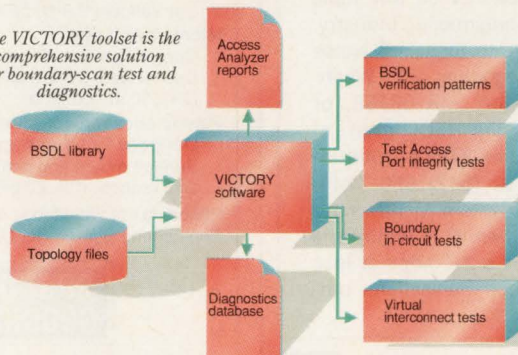
Increasing device complexity. Rising pattern development costs. High density packaging. Disappearing nodal access. These are the board test problems boundary scan was created to solve. Which is fine in theory. Only problem is there hasn't been any way to put boundary scan to the test. Until now.

VICTORY - the first software to automate boundary-scan testing.

Introducing VICTORY™ from Teradyne: the only software toolset ready to help you turn boundary-scan theory into a practical advantage. From the moment your first boundary-scan device is designed in, VICTORY starts

to simplify the testing of complex digital boards. And the more boundary-scan parts you have, the more time and money you save.

The VICTORY toolset is the comprehensive solution for boundary-scan test and diagnostics.

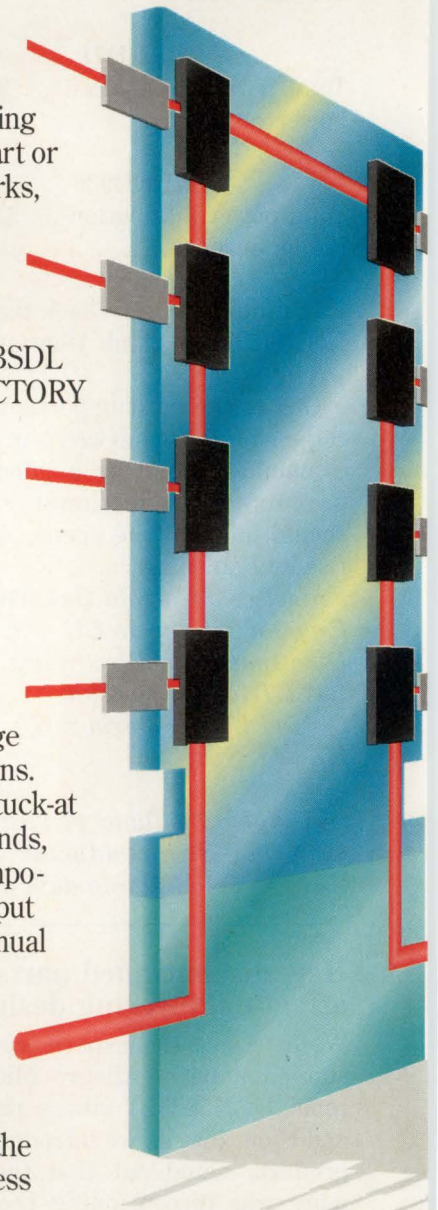


Delivers high fault-coverage.

Whether you're testing one boundary-scan part or boundary-scan networks, VICTORY software automatically gives you 100% pin-level fault coverage. Using the IEEE 1149.1 and BSDL standards, it takes VICTORY only a minute or two to generate test patterns. It would take a programmer days, even weeks to deliver the same fault coverage for conventional designs.

Now you can find stuck-at faults, broken wire bonds, wrong or missing components—even open input pins—all without manual diagnostic probing. VICTORY's fault diagnostics clearly spell out both fault type and fault location. And that's just the manufacturing process

Concurrent engineering takes on new meaning when you use VICTORY's Access Analyzer to optimize board layout for testability and cost-efficiency.

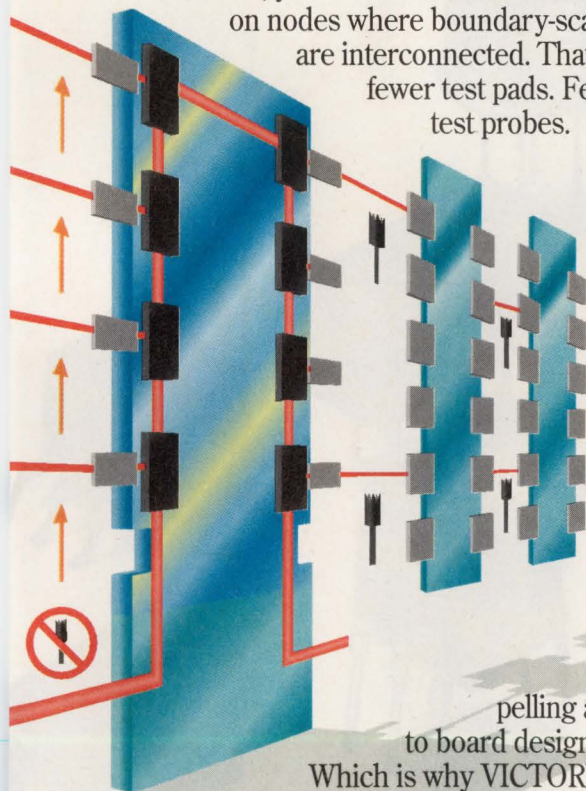


scan is a breakthrough board testing theory.

feedback you need to eliminate defects where it's most cost-effective—at the source.

Helps solve the test access problem.

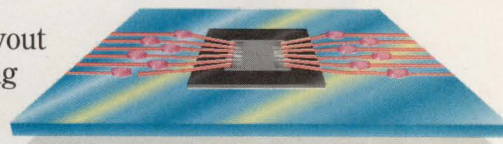
With boundary-scan design and VICTORY software, you won't need bed-of-nails access on nodes where boundary-scan parts are interconnected. That means fewer test pads. Fewer test probes.



That's a compelling advantage to board designers.

Which is why VICTORY's Access Analyzer was developed. With this concurrent engineering tool, designers get testability information early in the design process. They can easily see where test points are required for visibility and where they can be dropped, for opti-

mized board layout without lowering fault coverage.



Boundary-Scan Intelligent Diagnostics identify faults by type and location without physical probing—even on high-density SMT assemblies

Good for the bottom line.

Shorter test programming time. Higher fault coverage. Lower PC board and test fixture costs. The bottom line on VICTORY is how positively it will affect your bottom line. And because VICTORY works with all Teradyne board testers, you're free to tailor a test process that's cost-effective for both your boundary-scan and non-scan boards. No matter what your test objectives. For example, with our new Z1800VP-series testers, a complete solution for in-circuit and boundary-scan testing starts at well under \$100,000.

Make the next logical move. Call today.

Boundary scan is the design-for-test breakthrough that promises lower cost, higher quality board testing. But don't take our word for it. Call Daryl Layzer at (800) 225-2699, ext. 3808. We'll show you how, with VICTORY software and Teradyne board testers, you can test this theory for yourself.



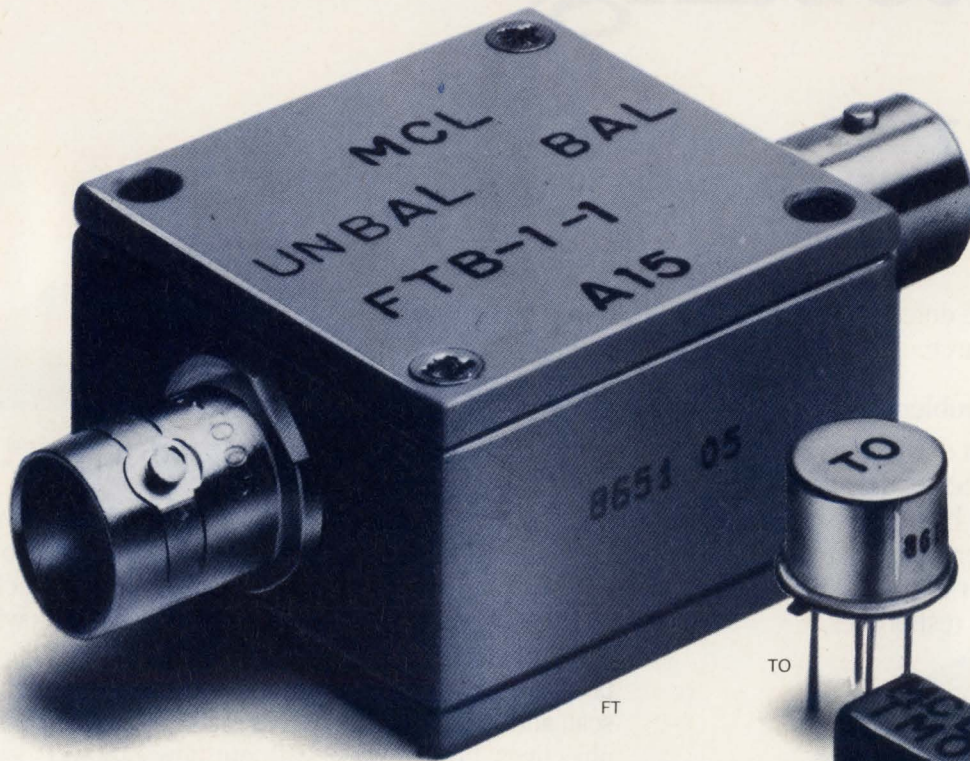
Get high fault coverage at low cost when you test boundary-scan boards with our new Z1800VP system and VICTORY software.

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RF TRANSFORMERS

Over 50 off-the-shelf models...

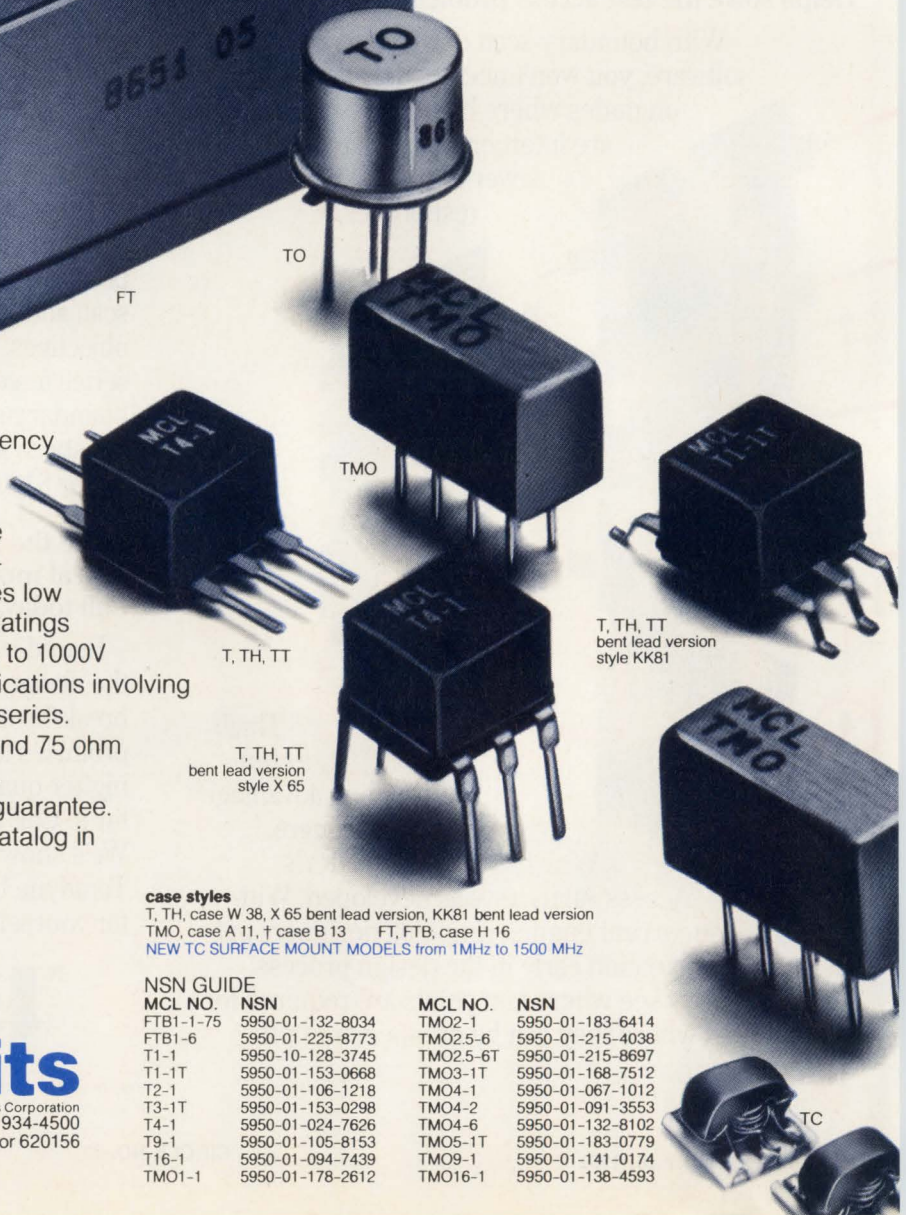


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*units are not QPL listed



case styles

T, TH, case W 38, X 65 bent lead version, KK81 bent lead version
 TMO, case A 11, † case B 13 FT, FTB, case H 16
 NEW TC SURFACE MOUNT MODELS from 1MHz to 1500 MHz

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MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

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 setting higher standards

Mini-Circuits

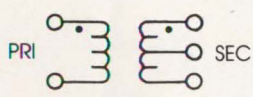
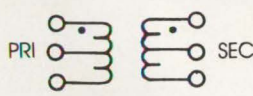
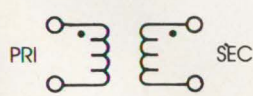
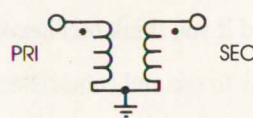
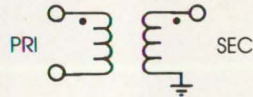
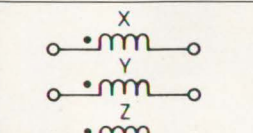
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				3dB MHz	2dB MHz	1dB MHz				
A* 	T	T1-1T	1	05-200	05-200	08-150	.2-80	4.45		
		T1-6T	1	003-300	003-300	01-150	.02-50	6.95		
		T2-1T	2	07-200	07-200	1-100	.5-50	4.95		
		T2.5-6T	2.5	01-100	01-100	02-50	.50-20	4.95		
		T3-1T	3	05-250	05-200	1-200	.5-70	4.95		
		T4-1	4	2-350	2-350	35-300	2-100	3.25		
		T4-6T	4	02-250	02-250	05-150	0.1-100	4.45		
		T5-1T	5	3-300	3-300	6-200	.5-100	4.95		
		T8-1T	8	03-140	03-140	10-90	1-60	7.95		
		T13-1T	13	3-120	3-120	7-80	5-20	4.95		
		T16-6T	16	03-75	03-75	06-30	1-20	5.65		
		T4-1H	4	10-350	10-350	15-300	25-200	5.95		
		TH	TMO1-1T	1	05-200	05-200	08-150	2-80	7.95	
			TMO2-1T	2	07-200	07-200	1-100	5-50	8.45	
			†TMO2.5-6T	2.5	01-100	01-100	02-50	.05-20	8.45	
			†TMO3-1T	3	05-250	05-250	1-200	5-70	7.95	
TMO4-1	4		2-350	2-350	35-300	2-100	6.25			
TMO5-1T	5		3-300	3-300	6-200	5-100	8.45			
TMO13-1T	13	3-120	3-120	7-80	5-20	8.45				
B* 	TT	TT1-6	1	004-500	004-500	02-200	1-50	6.95		
		TT1.5-1	1.5	075-500	075-500	2-100	1-50	5.95		
		TT2.5-6	2.5	01-50	01-50	025-25	.05-10	6.45		
		TT4-1	3	05-200	2-50	2-50	1-30	5.95		
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95		
		TT25-1	25	02-30	02-30	05-20	1-10	9.95		
	TTMO	TTMO25-1	25	02-30	02-30	05-20	1-10	11.95		
		TTMO1-1	1	005-100	005-100	01-75	.05-40	11.45		
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95		
C 	T	T1-1	1	15-400	15-400	35-200	2-50	3.25		
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65		
		T1-6	1	01-150	01-150	02-100	.05-50	5.65		
		T1.5-1	1.5	1-300	1-300	2-150	.5-80	4.45		
		T1.5-6	1.5	02-100	02-100	05-50	0.1-25	5.65		
		T2.5-6	2.5	01-100	01-100	02-50	.05-20	4.45		
		T4-6	4	02-200	02-200	05-150	1-100	4.45		
		T9-1	9	15-200	15-200	3-150	2-40	3.95		
		T16-1	16	3-120	3-120	7-80	5-20	4.45		
		T36-1	36	03-20	03-20	05-10	1-5	6.95		
		TO	TO-75	1	10-500	—	10-500	40-250	6.95	
			TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
				T9-1H	9	2-90	2-90	3-75	6-50	6.45
				T16-1H	16	7-85	7-85	10-65	15-40	6.45
		TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45	
			TMO1-1	1	15-400	15-400	35-200	2-50	6.25	
	TMO1.5-1		1.5	1-300	1-300	2-150	5-8	8.45		
	†TMO2.5-6		2.5	01-100	01-100	02-50	.05-20	7.95		
	†TMO4-6		4	02-200	02-200	05-150	1-100	7.95		
	TMO6-1	6	3-200	3-200	5-150	5-50	7.95			
TMO9-1	9	15-200	15-200	3-150	2-40	7.95				
TMO16-1	16	3-120	3-120	7-80	5-20	7.95				
D 	T	T2-1	2	050-600	050-600	1-400	5-200	3.95		
		T3-1	3	5-800	5-800	2-400	—	4.45		
		T4-2	4	2-600	2-600	5-500	2-250	3.95		
		T8-1	8	15-250	15-250	25-200	2-100	3.95		
		T14-1	14	2-150	2-150	5-100	2-50	4.95		
		TMO	TMO2-1	2	050-600	050-600	1-400	5-200	7.95	
	TMO3-1		3	5-800	5-800	2-400	—	8.45		
	TMO4-2		4	2-600	2-600	5-500	2-250	7.95		
	TMO8-1		8	15-250	15-250	25-200	2-100	7.95		
	TMO14-1		14	2-150	2-150	5-100	2-50	8.45		
	FT		FT1.22-1	1.22	005-100	005-100	01-50	.05-25	35.95	
		FT1.5-1	1.5	1-400	1-400	5-200	1-100	35.95		
E 	FTB	FTB-1	1	2-500	2-500	5-300	1-100	36.95		
		FTB1-6	1	01-125	01-125	05-50	1-25	36.95		
		■FTB-1-75	1	5-500	5-500	5-300	10-100	36.95		
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25		
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95		

■ Denotes 75 ohm models

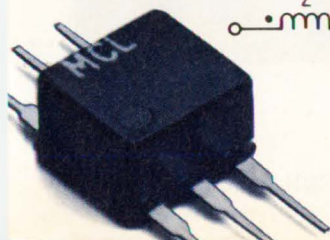
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0.1 dB over 1 dB frequency range
0.5 dB over entire frequency range

Maximum Phase Unbalance
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5.0° over entire frequency range

CIRCLE NO. 23

C72-2 REV. B



You have to build a to build just

The new Tek TDS Series

More than a million Tektronix oscilloscopes have all been leading up to this: the most powerful, versatile, and intuitive instruments ever developed for the mainstream of test and measurement.

The new TDS 500 Series is the culmination of everything Tek has learned in the design, manufacture and use of digitizing oscilloscopes. It's an achievement made possible only by the unique integration of acquisition functions and combinational trigger logic onto a single board.

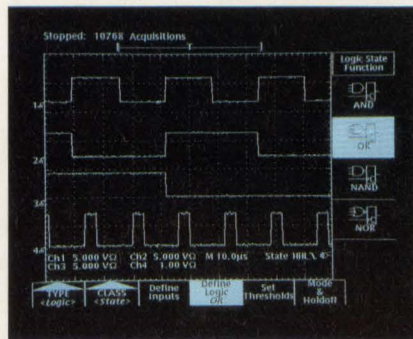
Only by the development of a milestone multiprocessor architecture.

Only by the addition of Tek's TriStar™ Digital Signal Processor (DSP).

Only by Tek's capacity for taking the hard work out of high performance.

The TDS Series performs, *live, up-*

dates and measurements that inhibit most other digitizing scopes. Its real-



time DSP lets you perform single-shot averaging and extend resolution to 12 bits. The TDS Series arms you with up to

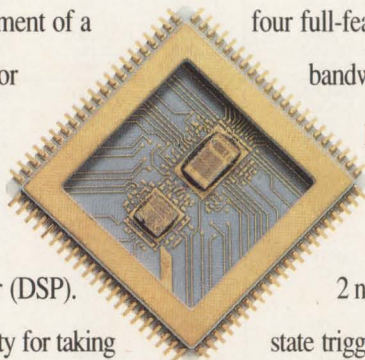
four full-featured channels. 500 MHz bandwidth. Up to 1 GS/s sam-

pling and 4 ns peak detect.

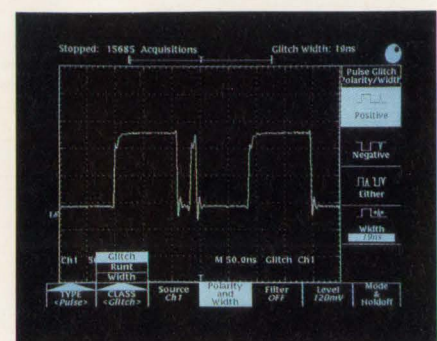
Up to 50K record lengths. Time interval,

2 ns glitch, runt, pattern and

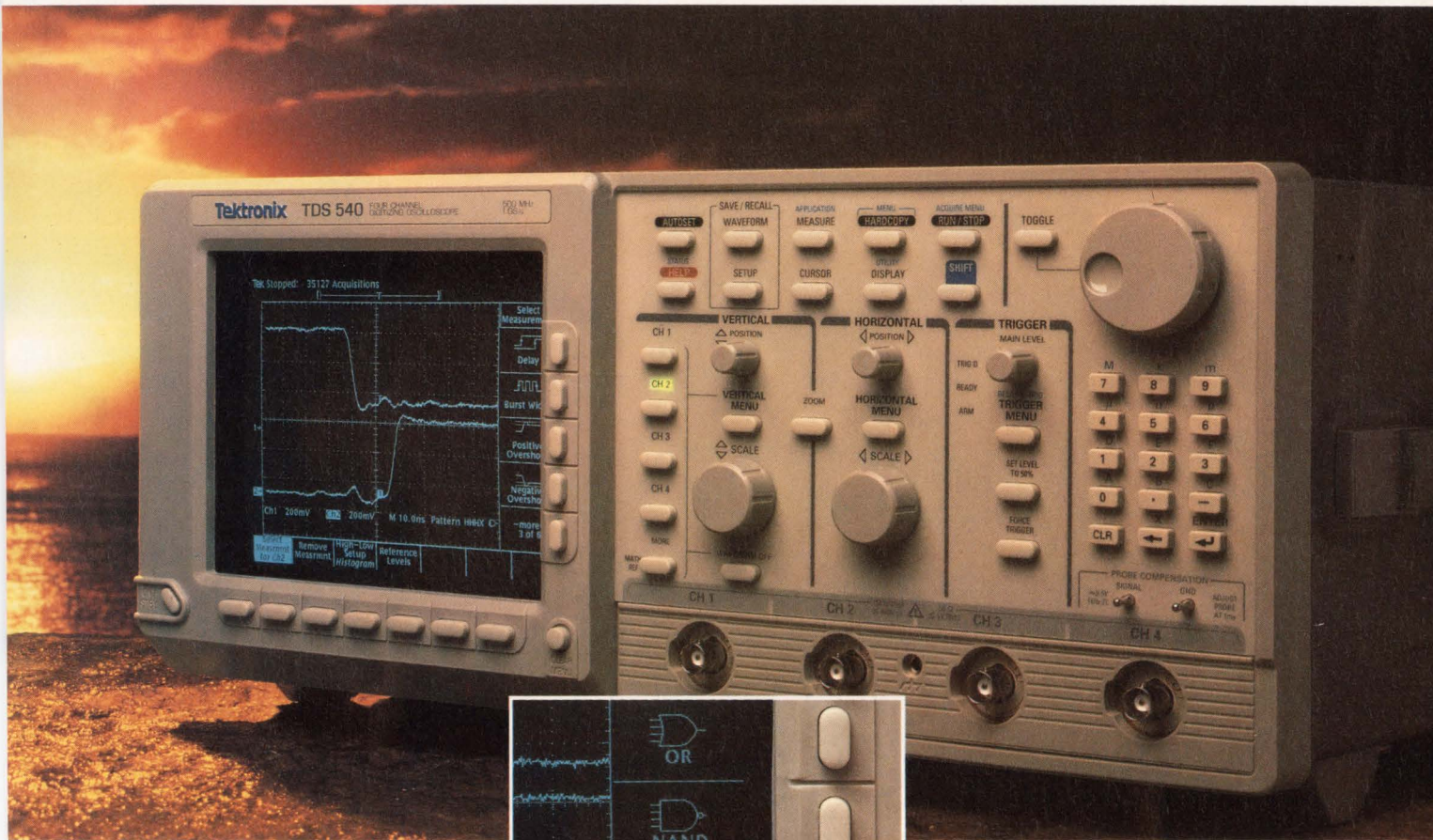
state triggers. With acquisition sensitivity and fast overdrive recovery bringing greater waveform detail within your grasp.



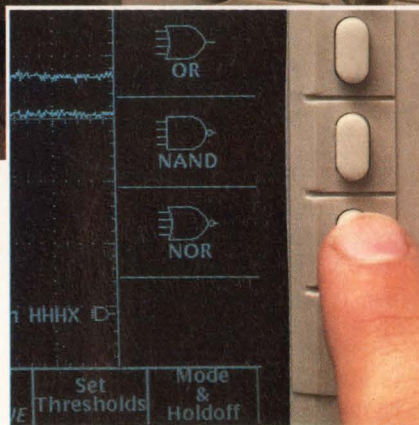
And if you think oscilloscopes aren't as easy to use and comprehend as they



million oscilloscopes one like this.



could be, you owe yourself a demo of the TDS. Its simplified front panel, VGA-quality display resolution, on-line help text, innovative icons that instantly differentiate menu functions — all add up to a scope that makes the user's manual more a formality than a necessity.



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ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

Reader wants to send real-time video via phone lines

I am looking for videophone boards or modules that will accept/deliver NTSC video and that will send "still" or maybe even near-real-time video signals over standard phone lines.

Tom Hill

**Sammons Communications
Duncanville, TX**

Unfortunately, off-the-shelf technology hasn't yet advanced to the stage where you can plug a television broadcasting station into your PC. However, sending individual video images via modem is a piece of cake—as long as you don't mind tying up your computer for hours and running up your phone bill.

The simplest and least expensive way to do what you propose is to make sure that both the sending and receiving computers are equipped with VGA boards that also output recordable NTSC images. (Refer to J D Mosley's article on image-processing hardware in the August 19, 1991, issue of EDN for a representative sample of such boards.) These boards produce interlaced NTSC images in a 512 × 400-pixel, 60-Hz recordable format, but typically display a maximum of only 256 colors. As long as you aren't concerned with photographic-quality images, you can buy such cards for your application for \$1000 or less. Note, however, that VGA images are noninterlaced, whereas NTSC images are interlaced. Accordingly, this method actually lets you transmit a normal VGA image via modem, but the sending and receiving VGA boards will automatically convert that image to the NTSC format.

For photographic-quality images, use a Targa board or other compat-

ible video graphics board to create a recordable NTSC image that contains 32,768 to as many as 16 million colors. You'll pay \$1500 or more for these boards, but if realistic image quality is important, you'll need the broad color palette of these boards.

The principal stumbling block is your requirement for using "standard phone lines," which seems to indicate that you also want to use a standard 2400-bps phone-line modem. You can do that. You can even use your favorite communications package—just have your communications software send the image as a binary file, rather than ASCII.

However, you have to consider the practical aspects of the task. It isn't unusual for a full-color computer image to encompass half a megabyte of data. To pump this much data through a 2400-bps modem would theoretically take about 56 minutes per image—and that doesn't include pauses for handshaking or error correction. Even if you beefed up your equipment to include a 9600-bps modem, each image would require 14 minutes for transmission. Such requirements preclude the 30-frame/sec display rate required for real-time video.

One alternative, suggested by Videotex Systems (Dallas, TX), is to equip both the sending and receiving computers with image-compression boards. Although such boards can reduce your transmission time, they also degrade the image: The greater the compression, the greater the degradation. But even if you bought boards that could provide 100 × compression, you still wouldn't reach real-time video rates. And even if you could transmit 15M bytes every second, where would you store all that data?

Our advice is to videotape whatever it is you want to record in "real

time" and let an overnight delivery service hand the tape to the person you're trying to reach. You'll both save a lot of time, money, and hassle. And if the objective is to have the recipient alter your images in some way, this delivery method lets that person use the video-input port of a video graphics card to download your recorded images into his or her computer for subsequent manipulation.

Wants to access EDN BBS

I am interested in obtaining a program from your bulletin board system (BBS). I do not have a modem attached to my computer, but the computer is linked to the Janet network, which can access the American Internet system. I am writing to inquire if your bulletin board has an Internet address and if so the method of accessing the program from this connection.

Paul Drummond

**The New Medical School
Newcastle-upon-Tyne, UK**

The United States National Science Foundation runs Internet, which is a noncommercial service, so we can't get an address on it. EDN has investigated links to commercial services and X.25 networks, but we found that the fees were too high for us to continue to offer a free BBS. However, we're getting some high-speed modems soon and are considering putting another EDN BBS computer in the United Kingdom. This computer would be updated every week via streaming tape. **EDN**

Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241; leave a letter in the ask_edn Special Interest Group.

NEW PRODUCTS – NICOLET'S PRO OSCILLOSCOPES

"Measurement Experts" get more choices from Nicolet

Nicolet Pro Oscilloscopes offer advanced trigger options in a waveform-analyzer-class scope

Nicolet invented the first digital oscilloscope to help engineers make better measurements. And for almost twenty years, they continued to focus on producing and improving top-end instruments for their "measurement expert" customers. Nicolet's new line of "Pro" digital oscilloscopes offers advanced trigger, display and programming features, while maintaining Nicolet's insistence on the highest standards of data integrity.

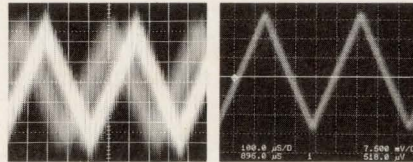
Nicolet Pro Oscilloscopes

The seven Nicolet Pro Oscilloscopes range from 8-bit units running at 200 Megasamples per second to differential-input 12-bit high-accuracy models. The Nicolet Pro 90 is a unique configuration of both, with independent timebases for *simultaneous* recordings at different accuracy levels and speeds.

Advanced Triggering in an Analog World

But the real innovation is that Nicolet has found a way to apply logic-analyzer style "advanced" triggering to the analog world. Many scopes have logic-analyzer style trigger modes. But logic-analyzer

implementations of glitch and dropout triggers assume the input signals are square-waves. With most *scope* applications, baseline noise and variations of input slew rate can mimic the intended trigger events. The results are false triggers, spurious "jitter" on repetitive signals, and incorrect timing on single-shot events – in short, false data.



Conventional scope

Nicolet scope

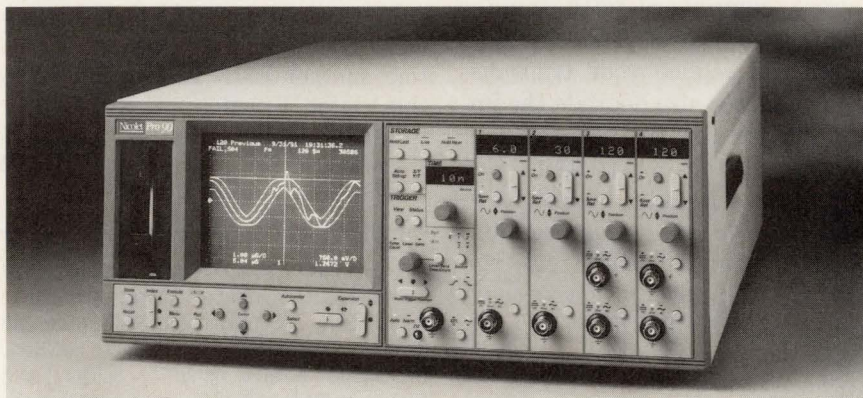
Nicolet's new scopes are different, with a unique variable-sensitivity control to prevent false triggers. Only Nicolet Pro Oscilloscopes arm or trigger when the input passes sequentially through *two* operator-selected voltages, eliminating triggers due to noise or baseline instability. And using the advanced modes is easier than you'd think – Nicolet displays the trigger level and sensitivity right on the waveform, and provides an on-screen icon of the chosen trigger type, source and key parameters.

Quality Measurement for Electronics

Of course, every Nicolet Pro model offers the familiar "quality measurement" features characteristic of Nicolet products, including ultra-long 256K memory, built-in MS-DOS floppy plus optional hard drive, and Nicolet's on-board programming language, TACT, for custom solutions to most measurement problems without an external PC. And even with four records of 256K each on the screen, Nicolet's crisp vector display instantly shows you a one-in-a-million transient.

Nicolet is entering its third decade of designing digital oscilloscopes still "on target" with instruments for today's measurement expert.

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(800) 356-8088**



Nicolet Pro Digital Oscilloscopes offer advanced triggering with sensitivity control for the analog world of noisy signals.

CALENDAR

Transmission and Distribution Conference & Exposition, Dallas, TX. IEEE/PES Registration, 2368 Eastman Ave, Suite 11, Ventura, CA 93003. (805) 654-0171. September 22 to 27.

Electronics Design Show, Birmingham, W Midlands, UK. MGB Exhibitions Ltd, Marlowe House, 109 Station Rd, Sidcup, Kent DA15 7ET, UK. (81) 302-8585. FAX (81) 302-7205. TLX 918389. September 24 to 25.

Electrical Overstress/Electrostatic Discharge Symposium, Las Vegas, NV. EOS/ESD Association, Box 913, Rome, NY 13440. (315) 339-6726. FAX (315) 339-6793. September 24 to 26.

Failure Mode and Effect Analysis (seminar), Boston, MA. Quality Alert Institute, 1475 S Colorado Blvd, Suite 206, Denver, CO 80222. (800) 221-2114; in CO, (212) 353-4420. FAX (800) 473-8348. September 27.

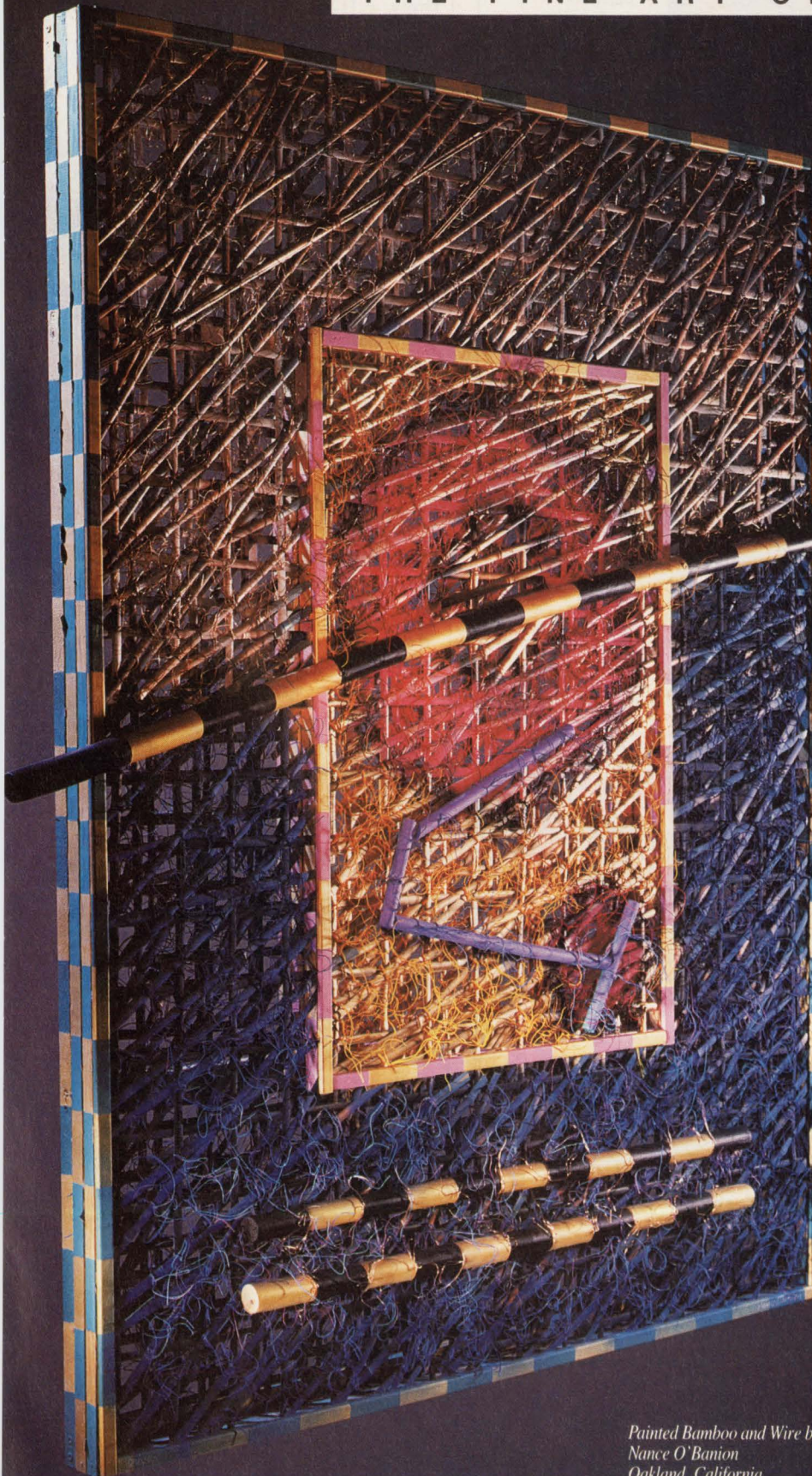
Information Security 91, Vienna, Austria. Diebold GesmbH, Graf Starhemberg-Gasse 25, A-1040, Wien (Vienna), Austria. (504) 13000. FAX (504) 1309. September 30 to October 1.

Electronic Imaging East, Boston, MA. Miller Freeman Expositions, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. FAX (617) 232-0854. September 30 to October 3.

IEEE-Holm Conference on Electrical Contacts, Chicago, IL. IEEE, Holm Conference Registrar, Box 1331, Piscataway, NJ 08855. (201) 562-3863. FAX (201) 562-1571. TLX 833233. October 6 to 9.

Telecom '91: World Telecommunications Exhibition, Geneva, Switzerland. International Telecom-

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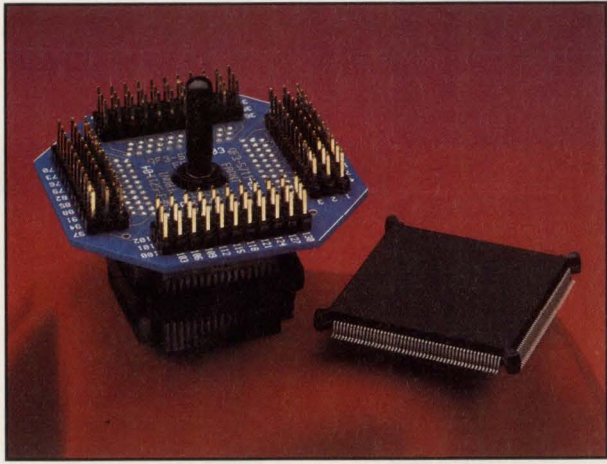
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CALENDAR

munication Union, Place des Nations, CH-1211 Genève 20, Switzerland. (22) 730-5236. (22) 733-7256. October 7 to 15.

DOD-STD 2167A/2168 Seminar, San Diego, CA. David Maibor Associates Inc, Box 846, Needham Heights, MA 02194. (617) 449-6554. FAX (617) 455-8928. October 8 to 10.

Modern Electronic Packaging Seminar, Burlington, MA. Technology Seminars Inc, Box 487, Lutherville, MD 21093. (301) 252-3425. FAX (301) 761-7942. October 9 to 11.

Symposium on High Density Integration in Communications and Computer Systems, Waltham, MA. Harry Lockwood, GTE Laboratories Inc, 40 Sylvan Rd, Waltham, MA 02254. (617) 466-2786. FAX (617) 890-9320. October 17 to 18.

Paris Cité: International Forum for Creative Technologies, Paris, France. ADAC/Paris Cité, 27 Quai de la Tournelle, 75005, Paris, France. (43) 26-29-99. FAX (43) 29-38-01. October 18 to 21.

IEEE GaAs IC Symposium '91, Monterey, CA. Jo Ann McDonald, The Legacy Co, Box 151, King City, CA 93930. (408) 385-5321. Registration: (202) 347-5900. FAX (202) 347-6109. October 20 to 23.

ISHM '91: International Symposium on Microelectronics, Orlando, FL. ISHM, Box 2698, Reston, VA 22090. (800) 535-4746; in VA, (703) 471-0066. FAX (703) 471-1937. October 21 to 23.

Object-Oriented Analysis and Design Seminar, Washington, DC. Technology Transfer Institute, 741 10th St, Santa Monica, CA 90402. (213) 394-8305. FAX (213) 451-2104. October 21 to 23.

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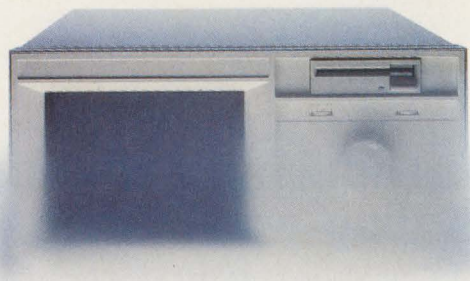


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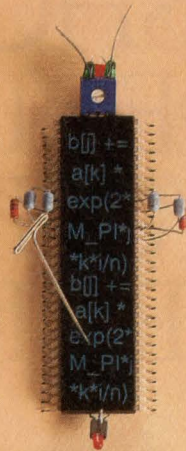


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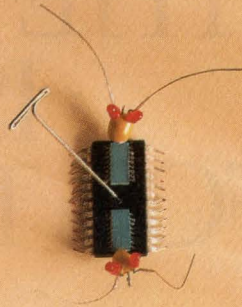
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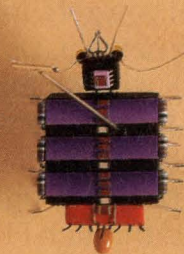
LOCK UP



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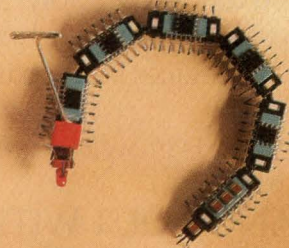
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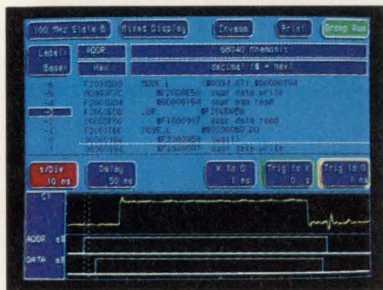
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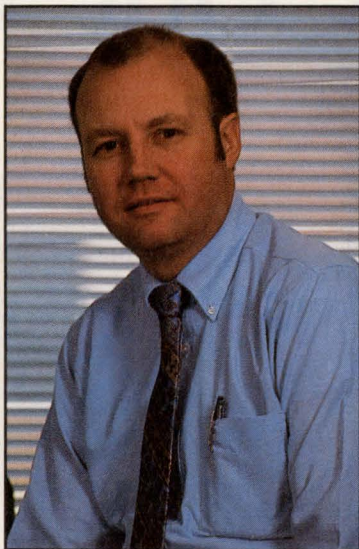
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EDITORIAL

The IEEE gets it wrong



In June, I received an announcement from the IEEE (Institute of Electrical and Electronics Engineers) that the group was presenting an award to Apple Computer Inc for creating the personal computer. The award singles out Apple "for the creation and establishment of the broadly successful personal computer." The Apple II computer was very successful and it—along with the Visicalc spreadsheet program—pushed desktop computers into commercial use. However, Apple neither created nor established the personal computer.

The award committee's chairman told me that the IEEE chose its words carefully so that it would not appear that Apple had invented the first personal computer. However, my thesaurus says that both create and establish can also mean originate and start.

The chairman also told me that the committee used only published resources and that it didn't interview people who developed small computers in the 70s. By not talking with those people, the IEEE was led astray. If nothing else, I'm disappointed in the IEEE for its misinformed role in helping to further solidify myth into historical fact. There are many people and many computers that deserve recognition for their roles in advancing us toward today, when PCs are a part of daily life for almost everyone.

History proves that Apple was not the first to create a PC. Back in the late 60s and early 70s Digital Equipment Corporation shrank its 12-bit PDP-8 into a desktop computer, the PDP-8/L, which became popular in controller applications. A group calling itself the Amateur Computer Society was founded by hard-core hackers in 1970, and many members spent considerable time and money trying to clone DEC's PDP-8/L. As I recall, coming up with the proper core memory was a nightmare.

Once Intel's 8-bit 8008 microprocessor arrived in 1973, designing your own computer became easier. Hobbyist computers such as the Mark-8 and Scelbi-8 became available. Intel's more sophisticated 8080 made possible computers such as the MITS Altair and the IMSAI. Later processors from Zilog and MOS Technology formed the heart of the Apple II, Radio Shack's TRS-80, and Commodore's PET. Let's not forget IBM's 5100, a portable computer from 1975 that you could program in APL. Other mid-70s computer developments from the Digital Group, Southwest Technical Products, Processor Technology, Sphere, and others are just too numerous to relate.

In the early days of the microprocessor revolution, there were many parallel and sequential efforts—often somewhat blurred even in the minds of those of us who were present. Apple came in on the tail end of that first burst of innovation. One thing is for sure; Apple neither created nor established the personal computer. The IEEE should withdraw its award as graciously and as quickly as possible.



Jesse H. Neal
Editorial Achievement Awards
1990 Certificate, Best Editorial
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1987, 1981 (2), 1978 (2),
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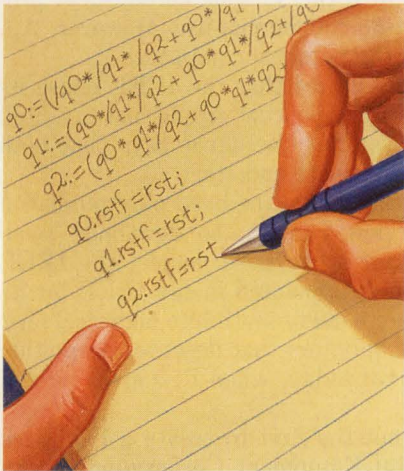
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1988, 1983, 1981

A handwritten signature in black ink that reads "Jon Titus".

Jon Titus
Editor

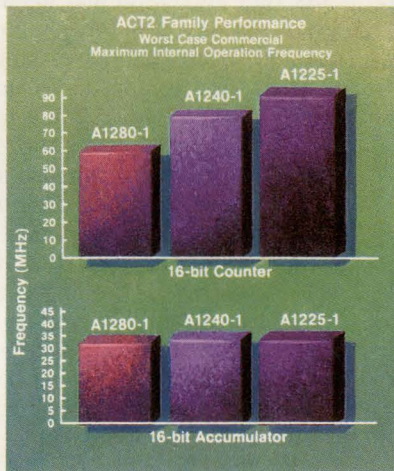
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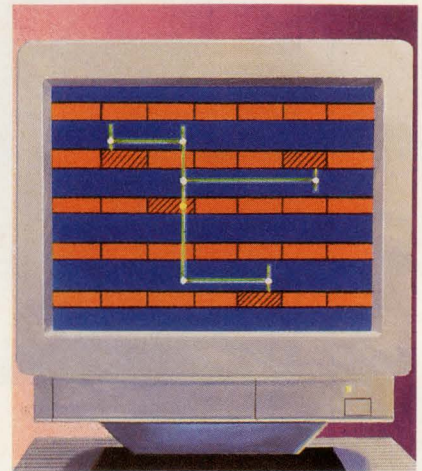
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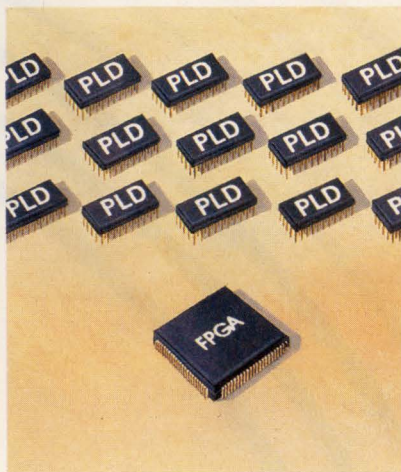
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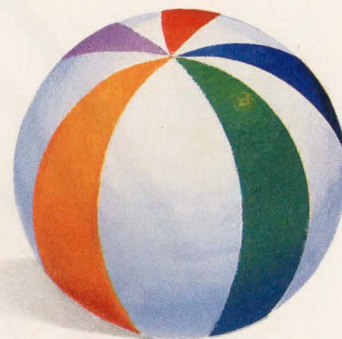
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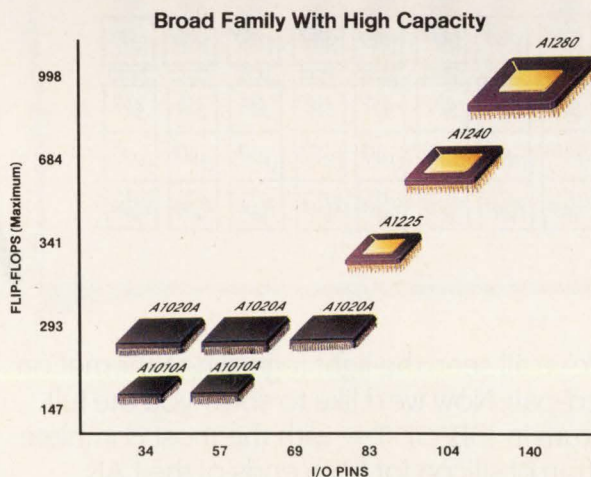
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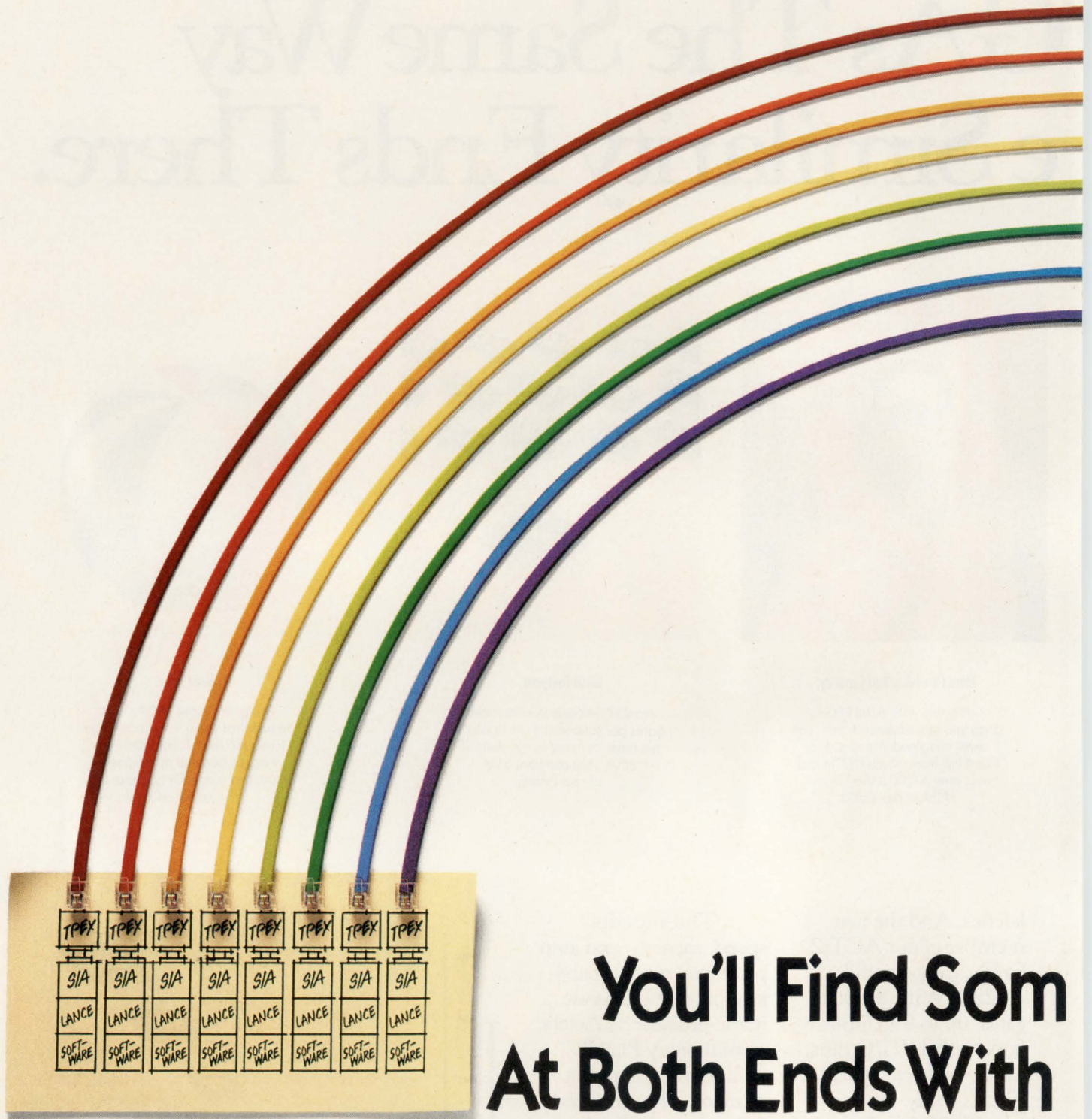
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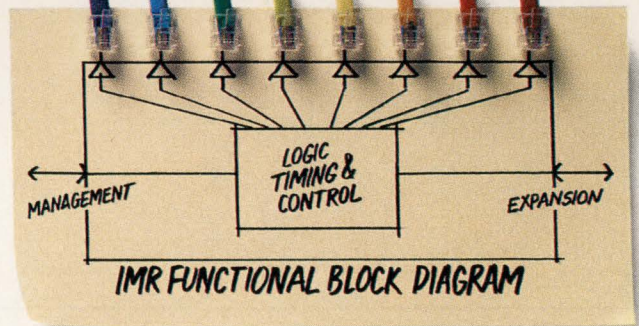
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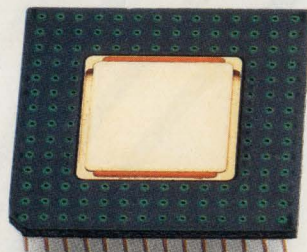
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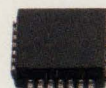
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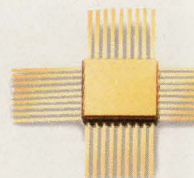
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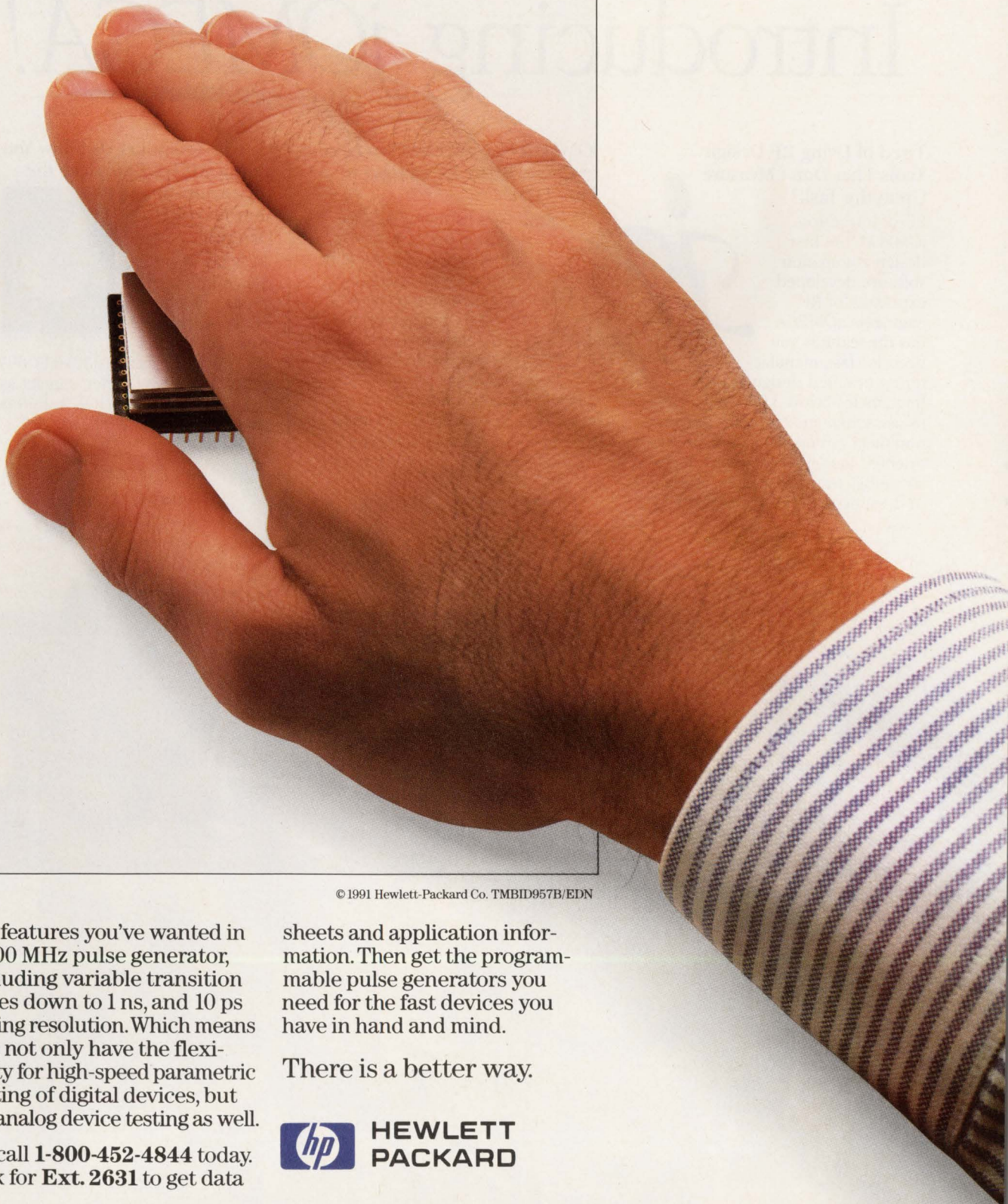


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TECHNOLOGY UPDATE

EUROPEAN EMC REGULATIONS

Europe lays down EMC Law

A law regulating the electromagnetic compatibility of many products takes effect in Europe on January 1, 1992. Deciding how to make the products conform will be up to the design engineer.

Some specifications have yet to appear, but enough technical information is available to make a start.

*Brian Kerridge,
European Editor*

Ohm's Law, Kirchoff's Laws, and now Europe's EMC Law. All electronic circuits produce electromagnetic emissions (EMI) at some level. Equally, all circuits become susceptible to EMI at some level. Europe's Electromagnetic Compatibility (EMC) Law sets out exactly what levels are acceptable in both cases for your product. In the future, when designing products for Europe, you will have to consider the EMC Law alongside other circuit constraints.

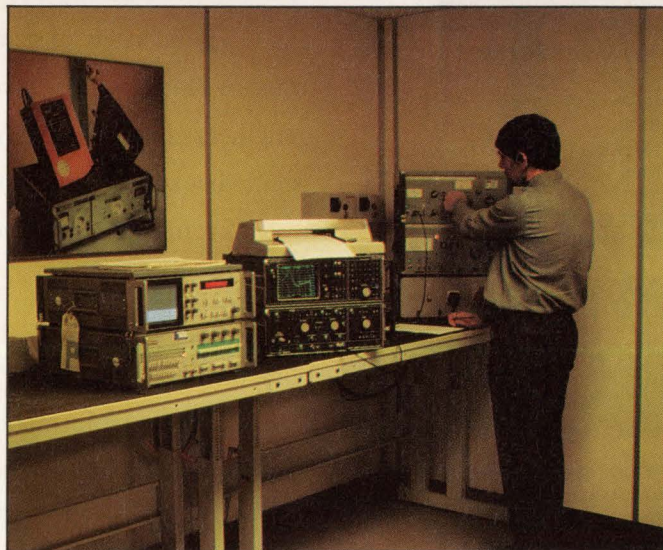
As part of Europe's move toward a single market structure, politicians and technocrats decided to formalize and harmonize EMC regulations. The result is European Directive 89/336/EEC (European Economic Community), entitled *Approximation of the Laws of the Member States relating to Electromagnetic Compatibility* issued by the Council of European Communities. Products will require a "CE" mark, as well as other documentary evidence, as proof of conformance.

In principle, as from January 1, 1992, it becomes a criminal offense to contravene the regulations. In practice, you still have a breathing space of two or three years in which to prepare.

If you declare compliance and your product fails to conform, ultimately it must be re-

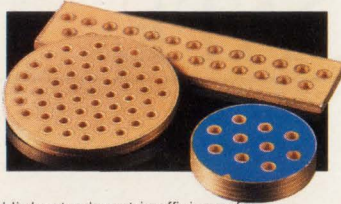
moved from sale and your stock impounded. If you fabricate documentation in order to imply compliance, then your company will face legal action against its European signatory.

The range of products affected by the new ruling is vast. According to an interpretation of the Directive by Chris Grimes, Chief Consultant on EMC with Siemens Plessey Assessment Services, "If an electron flows in your product, then the Directive is applicable to it." The EMC Directive encompasses regulations on emissions and immunity for conducted and radiated electromagnetic sources, line distortion, and electrostatic discharge (ESD). CENELEC (European Committee for Electrotechnical Standardization) is the European authority producing the new series of technical documents (distinguished by



Setting up a lab for EMC-emission and -immunity testing is expensive. Test equipment alone costs about £200,000, and you'll need a shielded and damped room to put it in.

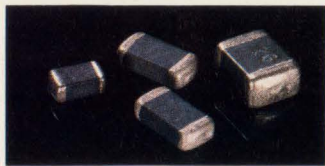
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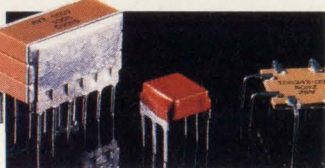
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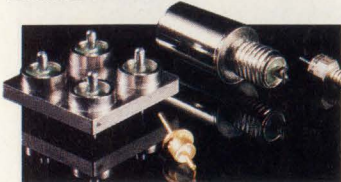
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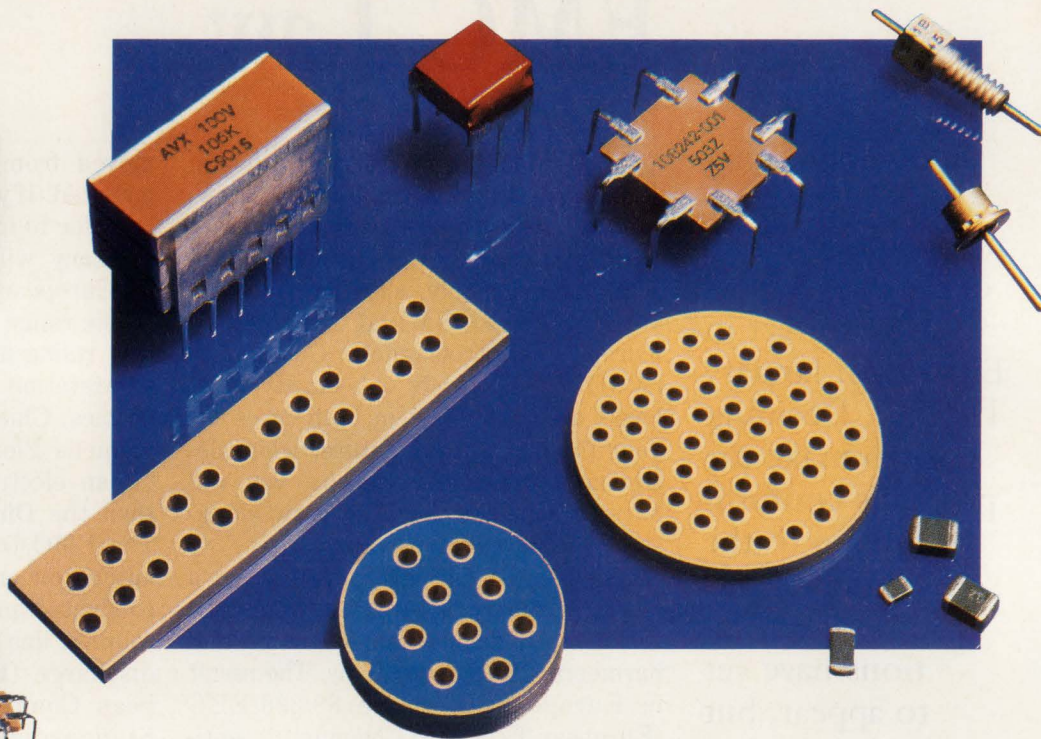
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TECHNOLOGY UPDATE

European EMC regulations

European Standard prefix "EN" (from its title in German)). Generally, the new documents specify harmonizations of existing specifications from CISPR (International Special Committee on Radio Interference), or the national standards of the European countries. **Table 1** identifies the EN documents produced so far and the provisional EN documents (prENs) under development, cross-referenced to established specifications. When deciding which specifications apply to your product, look for product-specific versions first, such as in the case of information technology equipment. If more than one specification applies, adopt the toughest. In the case where no specification exists for your product, the Directive still requires your product to conform to the EMC law. (How to deal with that situation appears later.)

Transition period eases pain

But don't think all issues are cut and dried. Although legislation will be in place from day one, some of the technical specifications will come later. Partly because of this delay, a transition period will enable a smoother switch from National to harmonized European specifications. The end date of the transition period is under consideration, but may extend to 1995. In the transition period, you can either wait, or attain compliance from day one using a mixture of whatever new specifications exist together with prevailing national specifications. Naturally, there is some confusion, and even experts in the same European countries cannot entirely agree on what you need to do to conform. Differences also exist between the EEC's member states over what technical specifications should apply. Even wording of the Directive itself

proves troublesome. The Council intends to publish a further document by the end of this year to clarify some issues, such as what "taken into service" and "placed on the market" mean.

Make no mistake, though—despite these discordant notes, the EMC Directive exists and will soon apply throughout the EEC's 12 member states and the four EFTA (European Free Trade Association) countries. By the end of the transition period at the latest, all electronic products must conform; and only harmonized EN specifications will count. Compliance will be mandatory for products in current production, regardless of country of origin.

When politicians, specmakers, and marketeers have had their say, it will be up to you, the design engineer, to decide how to make the product conform.

That your product must ulti-

mately conform is certain. How you reach conformance is less certain. The issues are complex, and subject to various interpretations. At the very least, your company will need to assign one person the responsibility of studying, interpreting, and tracking the developing situation.

Fig 1 shows EDN's interpretation of the various routes to compliance. Several organizations are already offering specialist help and advice. (See **box**, "Who can help?")

Three ways lead to compliance

In overall terms, the route to placing a compliant product on the European market is straightforward. First, you adopt one of three possible methods to convince yourself that the product conforms technically. Then, you apply a "CE" mark to the product and ship it with a declaration-of-compliance certificate.

The certificate must name a com-

Table 1—European standards relating to EMC

	European standard ¹	Subject	Equivalent standard
Emission	prEN 50081-1	Generic domestic, commercial, and light industrial equipment	None
	prEN 50081-2	Generic industrial equipment	None
	EN 55011	Industrial, scientific, and medical equipment	CISPR 11
	EN 55013	Radio and TV receivers	CISPR 13
	EN 55014	Household appliances	CISPR 14
	EN 55015	Lighting equipment	CISPR 15
	EN 55022	Information technology equipment	CISPR 22
Immunity	EN 60555	Line disturbances	IEC 555
	prEN 50082-1	Generic domestic, commercial, and light industrial equipment	None
	prEN 50082-2	Generic industrial equipment	None
	EN 55020	Radio and TV receivers	CISPR 20
	prEN 55101-2	Information technology equipment—ESD	None
	prEN 55101-3	Information technology equipment—RF radiation	None
	prEN 55101-4	Information technology equipment—RF disturbances	None
	HD 481 ²	Industrial process, measurement and control equipment	IEC 801

Notes:

1. European standard designation is EN; provisional status is prEN.
2. No EN number yet, still at harmonization status.

TECHNOLOGY UPDATE

European EMC regulations

pany signatory. Ideally, that person should be a resident European native. In the case of manufacturers outside the EEC, that person would normally be in the employ of your representative or distributor.

The three methods of reaching a level of confidence that your product complies are:

- self-certification
- third-party certification
- technical-construction file.

Self-certification appears to be the most direct route, as it is informal and involves minimal interactions outside your company. As the Directive stands, this route allows you freedom to do whatever convinces you that your product complies. When you feel certain of compliance, then your path is clear to apply the CE mark and get on with the selling.

The danger with this route is if someone officially challenges your product's conformance. How able will you be to support your belief that the product does indeed conform? If you are unable to convince the EEC trade authorities, then your product must be withdrawn and your company stands the risk of being blacklisted. In extreme cases, your European signatory could end up explaining things in court.

Nonetheless, companies outside Europe will favor this route, especially where the convenience of local EMC test facilities exist. In the case of a challenge, when test results from a reputable source are available, the danger of a product ban diminishes.

Third-party certification is the route that offers optimal assurance that your product conforms. Essentially, you subcontract the work to an accredited laboratory. The laboratory tests, reports, and certifies product compliance. A third-party test house must be accredited, oth-

erwise the laboratory is not authorized to issue certificates. In the UK, NAMAS, a department of NPL, accredits such laboratories. DAE is the accrediting authority in Germany.

At present, accredited labs exist only in Europe. By the end of 1991, NAMAS expects there will be around 30 accredited labs for EMC testing in the UK. Germany will have around 15. Ideas to allow third-party testing in laboratories outside Europe are in the early

stages. In the case of self-certification, it is not essential for your laboratory to be accredited.

Paperwork proves powerless

The technical-construction-file route is the most uncertain way to have your product declared compliant. In the first place, there is no clear idea yet of what should be in a technical-construction file. The attraction of this route is that the need for testing is not mandatory. The general intention is that the file

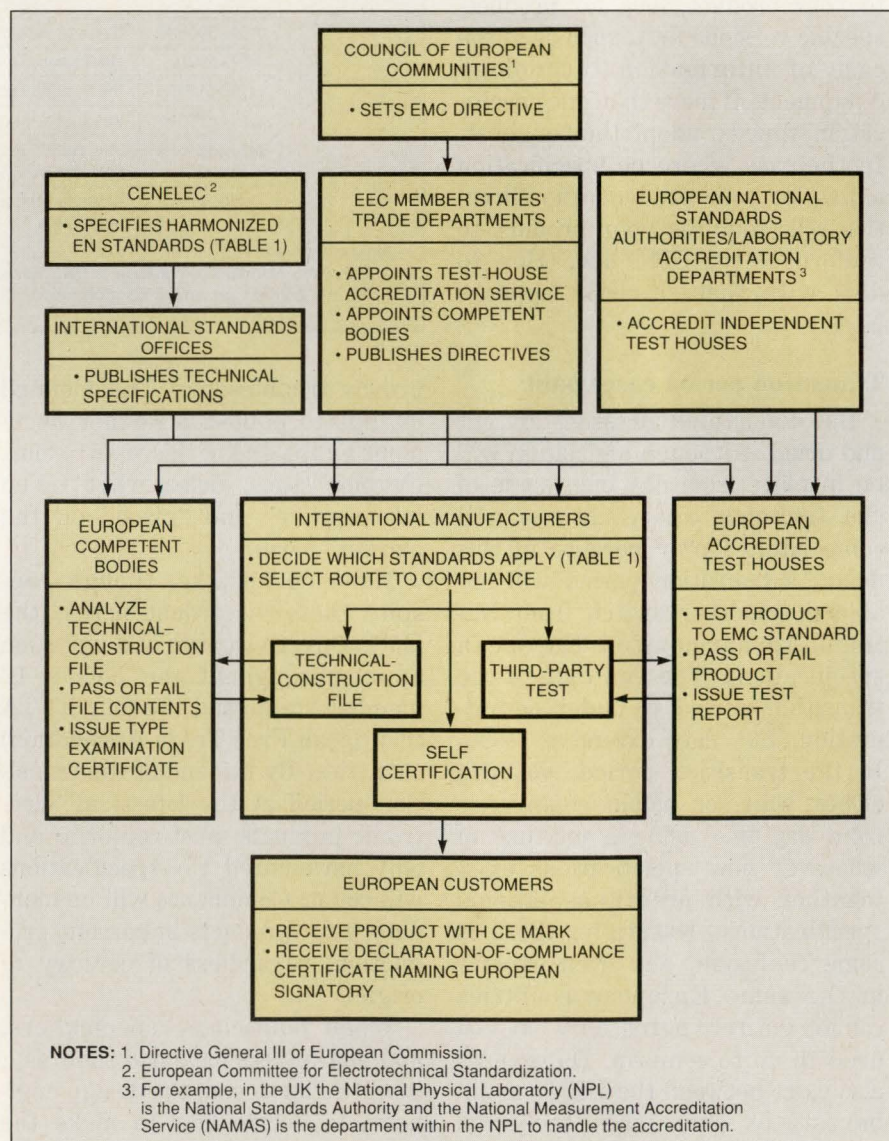
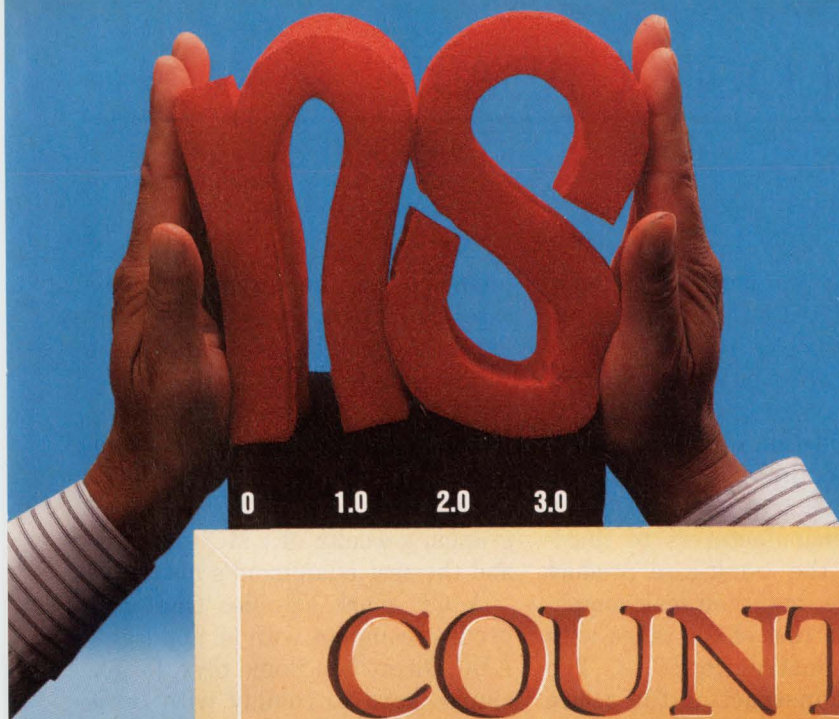


Fig 1—EDN's guide to compliance with Europe's EMC Directive.



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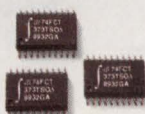
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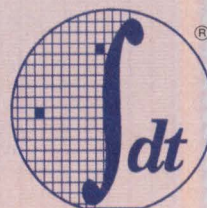
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European EMC regulations

contains sufficient information to convince a "competent body" that your product complies. A competent body is another independent agency, authorized by governments to vet technical-construction files and issue approval certificates. By the end of 1991, each EEC member state's trade department will issue a list of accredited test houses and competent bodies.

Geoff Orford, at NAMAS, believes the technical-construction-file route, as the directive has outlined it, has little merit. He says that

most EMC Standards are simply recipes for testing, and therefore you cannot hope to demonstrate compliance without some tests.

Grimes says the value of the technical-construction-file route shows up when manufacturers have a range of similar products. He recommends manufacturers to third-party test the worst-case product in the range, and then seek compliance for the rest of the range with technical-construction files. The technical-construction-file route also theoretically allows early com-

pliance with the directive in the case of temporary absence of standards. Although, on what basis a competent body will make a judgment remains uncertain.

Grimes says he expects a technical file to include a technical report, a detailed block diagram, photographs, a wealth of EMC test data, and the test equipment's history.

A CE mark signifies that your product complies with all applicable EEC Directives. Some toys, for example, have to comply with three earlier Directives, and are among

Who can help?

For more information on Europe's EMC Law, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following companies or organizations directly, please let them know you read about them in EDN. When you contact them directly from outside Europe, faxing is the best option. For example, the UK Government's Department of Trade and Industry EMC office operates a system of taking phone calls by answering machine. The office answers routine overseas queries by fax.

For a copy of Directive 89/336/EEC:

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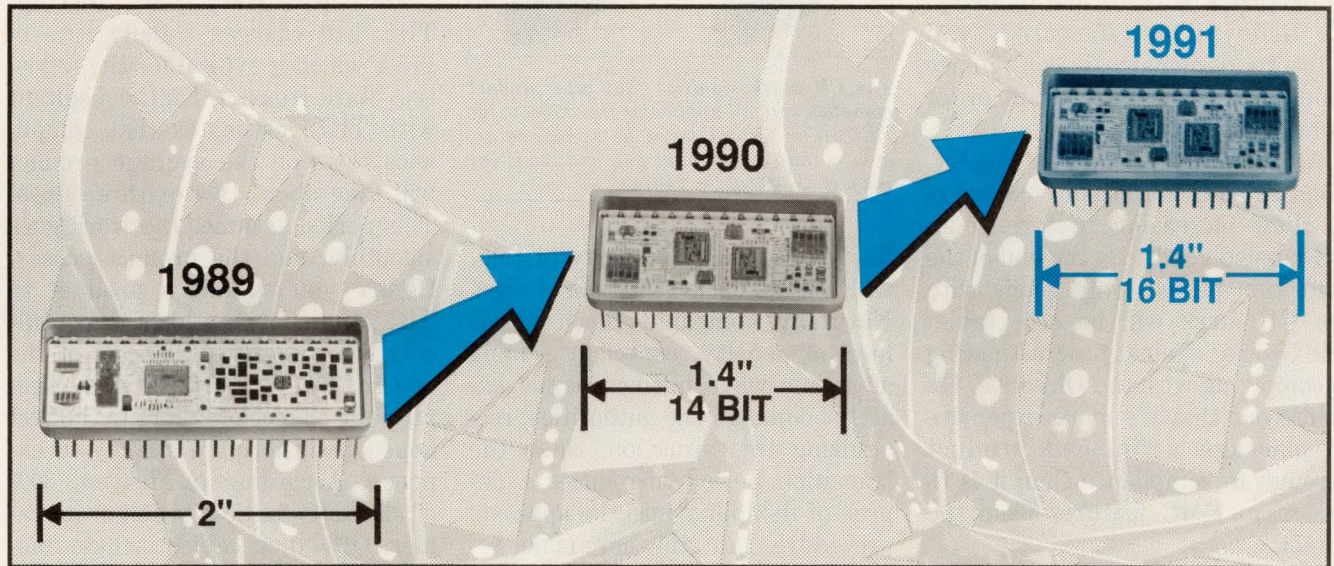
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Our present line of multichannel Synchro- or Resolver-to-Digital converters has been expanded to include additional features such as 16 bit resolution. Assigned model numbers SDC-14575, SDC-14605, and SDC-14615 series, these products offer the smallest size, and lowest cost per channel of any hybrid product available.

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The SDC-14605 and SDC-14615 series, are two- and three-channel versions of the SDC-14575. All channels are independent, except for the reference inputs and digital output pins, which are shared. Output angle data is enabled onto the tri-state data bus in two or three bytes. Enable MSB (EM) is used for the most significant 8 bits and Enable LSB (EL) is used for the least significant 8 bits.

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For additional information please contact Bill Cullum at (516) 567-5600, extension 389. □

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TECHNOLOGY UPDATE

European EMC regulations

the first products already displaying CE marks. The first CE marks showing adherence to the EMC Directive should appear by the end of 1991, according to Tony Bond, head of the EMC office of the UK's Department of Trade and Industry. He believes manufacturers will want to demonstrate compliance sooner rather than later in order to beat competitors.

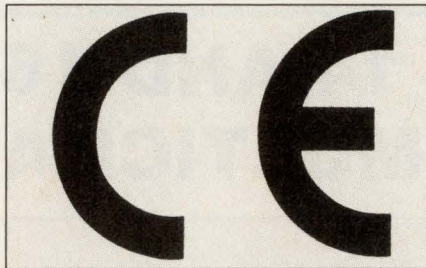
As the transition period passes, Bond expects purchasing managers to show increasing preference to CE-labeled goods. By the end of the transition period, only goods with the CE mark will be acceptable. Bond warns against procrastinating in complying with the Directive. He points out that it's more expensive to massage a finished product through to compliance than it is to design in EMC features from the outset.

He also thinks manufacturers in the UK will provide a natural watchdog service over other suppliers. He says the system will be "complaints driven"—competitors will step forward to expose one another.

In Germany, the Ministry of Telecoms has 50 offices spread throughout the country to police contraventions of EMC and other Directives. These offices routinely purchase and test products. If your product is found lacking, you will have to pay heavily for the test work, and be given a fixed period in which to conform. You may also be punished for importing the goods in the first place. Essentially, if you get to this stage in Germany, you're in big trouble.

All routes demand heavy toll

Attaining compliance will be expensive. Even discounting your additional design effort and manufacturing costs, the extra work in assembling documentation, and the



The CE mark signifies that your product complies with all applicable Directives of the EEC. The letters must be semicircular, greater than 3 mm in height, and the E-bar must be >80% of the radius.

likely need for third-party testing, will cost at least \$2500 per design. Naturally, companies flinch at this level of penalty, especially coming at a time when business is not exactly booming. The authorities, recognizing this situation, claim the transition period introduces a degree of flexibility into the approval procedure. But still there is not really a low-cost route.

At a recent forum of EMC-Directive experts in the UK, a delegate from a small company producing custom designs asked how he could afford to meet the Directive and survive. The experts had no satisfactory answer. The only advice from the panel (a test house representative), was to discuss the problem with a test house. It seems that companies in this predicament have a difficult decision to make: They can either dodge the directive and risk getting caught, or go out of business.

If you consider self-certification using your own set-up, the cost is exorbitant. Tom Leahy, technical manager with Schaffner EMC Ltd, estimates a minimum of £280,000 is necessary in order to do emission and immunity testing. Of that figure, £100,000 buys you an electromagnetically shielded and damped room of around 25m², which he says is essential to obtain repeatable test results. Leahy sees that the main

problem with setting up your own facility is in locating experienced engineers to make the measurements. He reports mainly multinationals following this route, and only a few of the smaller companies.

For third-party EMC testing, TRL Ltd charges a daily rate of £750, which is typical for the industry. Mark Heaven, EMC consultant with TRL, estimates that compliance tests on the average product will take about two or three days. This period assumes the work goes smoothly, and the product passes. Before you submit a product to TRL, the company likes to consult with you on critical aspects of the design. These consultations minimize the chance of failure in the test house, and therefore limits your expense. According to Heaven, 80% of all EMC failures result from cables. Offending cables include line-cords, data-links (such as RS-232C and IEEE-488), and signal leads. Apertures in the product's enclosure have the second largest effect on a product's failure.

Heaven says fixing EMC problems in a finished product is often a losing battle, and costly. Unless you carry out substantial redesign, involving changes to the pc-board layout, all you can do is install more shielding or filtering. The best way is to be conscious of EMC requirements throughout the design process. In that way, you can minimize, or even eliminate, additional product and manufacturing cost. Also, you optimize your chance of passing the test routine the first time. Some products cannot avoid cost penalties, however—notably, enclosures for information-technology products. Additional shielding using electroless plating on plastic surrounds increases component cost as much as three to ten times.

Wolfgang Sammet, EMC specialist with Siemens, also emphasizes

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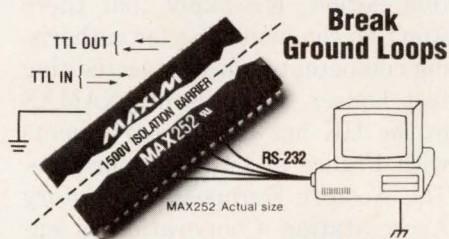
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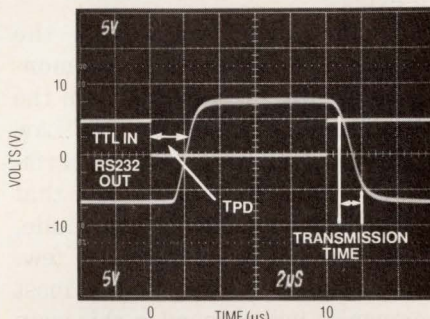
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Isolated RS-232 in One Package!



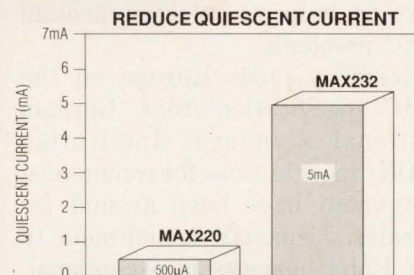
The **MAX252** provides a complete isolated interface in one +5V-powered standard 40-pin DIP package by delivering voltage isolation up to UL levels (1500V for 1 sec).

New +5V RS-232 Transceiver Doubles Speed of Existing +5V RS-232 Devices!



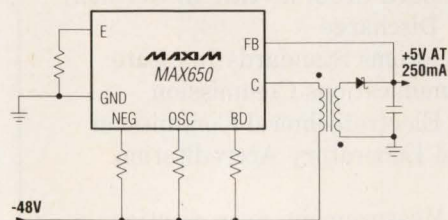
The **MAX232A** +5V dual RS-232 transceiver is guaranteed to operate at data rates up to 116kb/s, while driving real loads – 2500pF and 3kΩ. And, the **MAX232A** uses space-saving 0.1µF caps.

RS-232 Transceivers at 1/10th the Power!



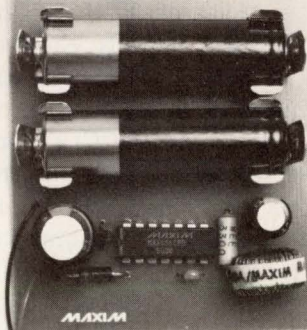
The **MAX220** dual +5V transceiver is designed specifically for low-power operation. Quiescent operating supply current is a mere 500µA unloaded. And, the **MAX220** is guaranteed to operate at data rates up to 20kb/s.

-48V to +5V Output Switching DC-DC Converter



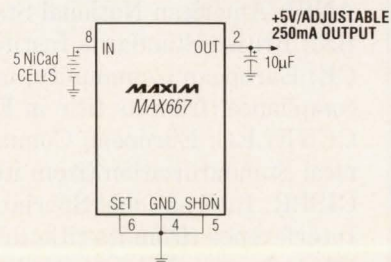
The **MAX650** contains all control functions and a 140V, 250mA PNP transistor, reducing external components. The converter has a selectable soft-start function, a shutdown pin for output on-off control, and peak-current limiting on the PNP output.

Evaluation Kit for Simple +3V to +5V Step-Up Converter



The **MAX655** Evaluation Kit includes everything needed to build and test a circuit that converts 2 AA cells to +5V. The kit includes an evaluation board with low-noise layout, a **MAX655**, and all components necessary for prototyping with the **MAX655**.

+5V Linear Voltage Regulator Has 150mV Dropout at 200mA



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TECHNOLOGY UPDATE

European EMC regulations

the importance of good design practice from the beginning. He says particular attention to grounding and short signal paths on your pc-board layout pays dividends. He also meets many problems at a system level. It is quite common for a collection of modules that pass an EMC test as individual units to fail when connected together. This situation highlights the problem of "configuration control," which Sammet sees as the major obstacle in the future. Several EMC specialists suggest Henry W. Ott's *Noise Reduction Techniques in Electronic Systems* (Wiley-Interscience, 1988) as a comprehensive and readable text to help you design around EMC problems.

Germany leads Europe on the EMC specification front. German National Standards Institution (VDE) specifications for commercial equipment have been around for decades. Siemens's commitment to the EMC business is exceptional. The company has extensive test facilities in Munich and markets a va-

riety of EMC components for products and installations. Siemens has run EMC training seminars for design engineers for the last 20 years. Currently, the program takes place six times a year at international venues. Despite these advances, it is Sammet's view that a lot more needs to be done. In particular, he thinks electricians and technicians, as well as design engineers, need to be aware of, and understand how their work affects EMC.

The impact and complexity of the new EMC legislation is likely to influence all involved to move cautiously through the early months of 1992. Nobody knows exactly what to expect.

So far, every sign from the authorities suggests a common-sense approach, particularly in the UK. The objective of the EMC Law is to be protective more than pernicious. If you can demonstrate that you've taken a responsible attitude, then your problems should be few. The authorities anticipate that most companies will respond in this way,

just as they have with safety regulations.

Some anomalous and difficult areas persist, however. It's not likely that they will disappear until the new regulations have passed a burn-in period.

Lack of commonality throughout the EEC is one such problem. In the transition period, for example, it will be possible for different specifications to apply in different countries, but all these specifications will lead to qualifying for the same CE mark. For example, as German VDE specifications are the toughest, it will be attractive to qualify elsewhere. Even after the transition period, it's likely that there won't be common rules for authorizing competent bodies or accrediting test houses. At present, NAMAS in the UK has mutual agreements with France and the Netherlands. The Western European Laboratory Accreditation Cooperation is engaged in providing common rules, but progress is at snail's pace.

Looking further afield, there is

What does it all mean?

The following list of acronyms are in common usage in the Standards and EMC world:

ANSI: American National Standards Institute
BSI: British Standards Institution
CE: European Community, used for CE mark of compliance (from its title in French)
CENELEC: European Committee for Electrotechnical Standardization (from its title in French)
CISPR: International Special Committee on Radio Interference (from its title in French)
DAE: German Laboratory Accreditation Service (from its title in German)
EEC: European Economic Community (Belgium, Denmark, France, Germany, Greece, Ireland, Italy, Luxembourg, The Netherlands, Portugal, Spain, and the United Kingdom)
EFTA: European Free Trade Association (Austria, Finland, Sweden, and Switzerland)

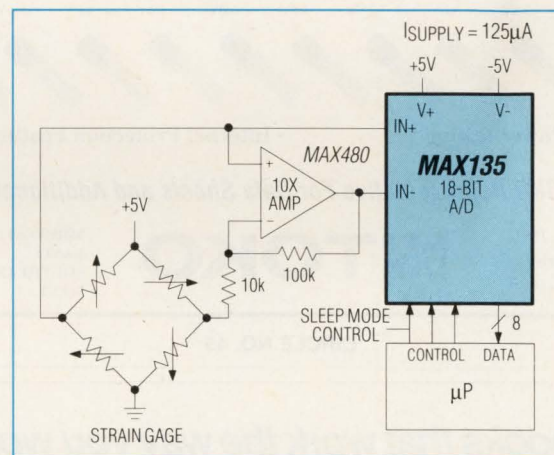
EMC: Electromagnetic Compatibility
EMI: Electromagnetic Interference
EN: European Standard (from its title in German)
ESD: Electrostatic Discharge
ETSI: European Telecoms Standards Institute
FCC: Federal Communications Commission
IEC: International Electrotechnical Commission
ILAC: International Laboratory Accreditation Cooperation
NAMAS: National Measurement Accreditation Service (Department of NPL)
NPL: National Physical Laboratory (in UK)
prEN: Provisional EN, not fully ratified
RFI: Radio Frequency Interference
VDE: German National Standards Institution (from its title in German)
WELAC: Western European Laboratory Accreditation Cooperation

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- ◆ **$\pm 10pA$ Input Current**



Maxim's MAX135 and MAX480 team up with a bridge and a μ P for high-accuracy measurements over temp.

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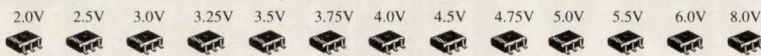
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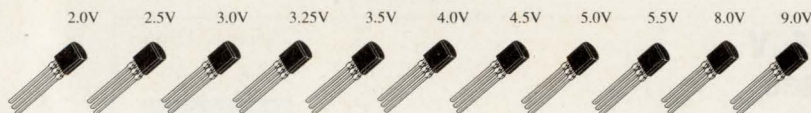
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UPDATE

European EMC regulations

a strong case for establishing equivalent competent bodies and accredited test houses outside Europe. This move would make it much more straightforward for international manufacturers to use the third-party test route to comply. However, the likelihood of this happening in the next five years seems remote. Yet another organization, the International Laboratory Accreditation Cooperation, supports the idea, but implementing any program is way off.

The most persistent headaches will result from difficulties of configuration control. For example, if a PC plug-in card complies in PC type A, but fails in PC type B, you will have to decide how many other PC types you should try it in. If you are a systems integrator, your headaches multiply. All your systems may have a different configuration, and the system may pass at one site, but fail at another. If you're a small company making custom designs, it's unlikely you can pass the cost of testing to your customer for every single product.

Europe's EMC Law is here to stay and is certain to disturb the tranquility of your R&D lab. In design-cycle terms, the 1995 drop-dead date is not so far away. Tune in to Europe's EMC emissions, before Europe designs in immunity to your products. **EDN**

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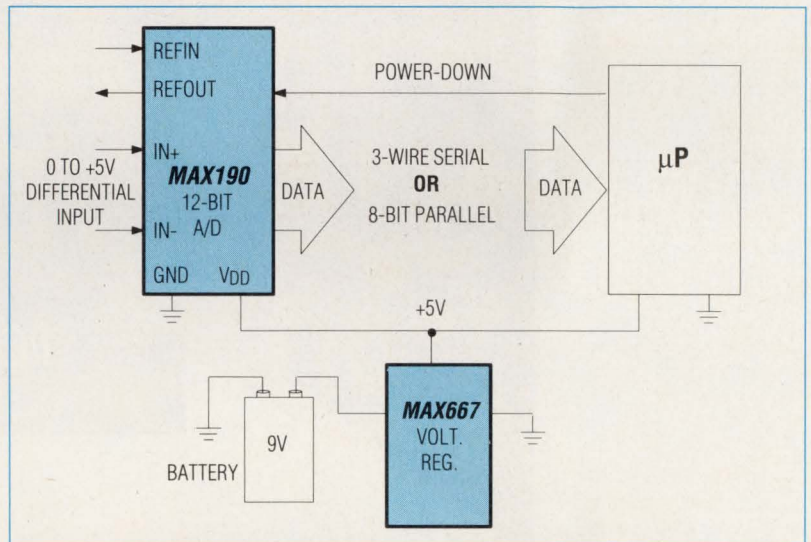
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4. 150 μ W Power-Down

5. 35 μ s Start-Up

6. 1/2LSB Linearity

7. 100kbit (10bit Channel to μ P Configuration)

8. 100kbit (10bit Channel to μ P Configuration)

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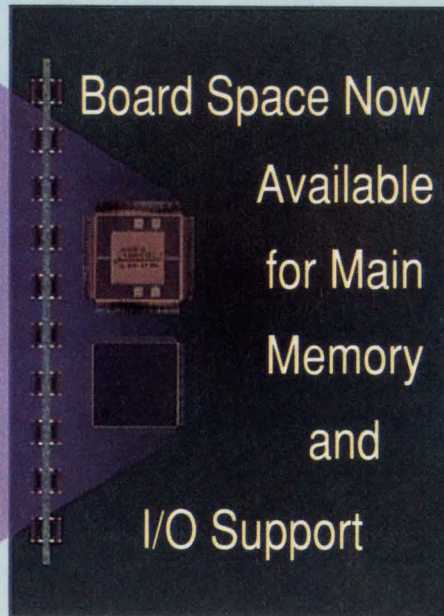
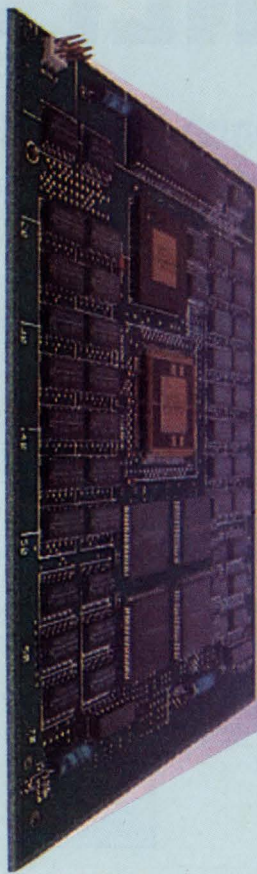


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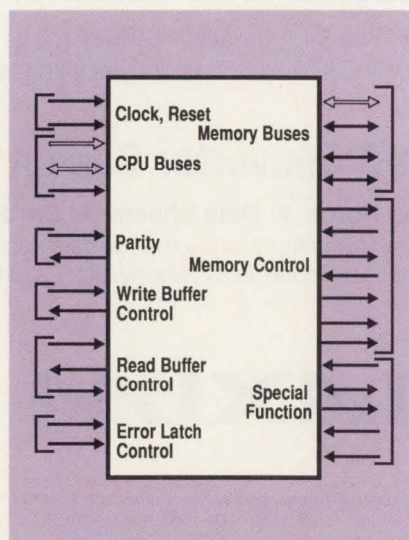
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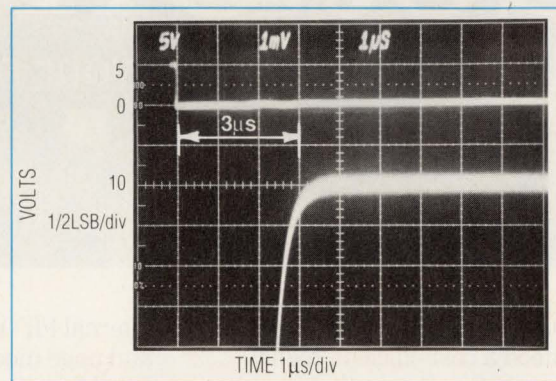


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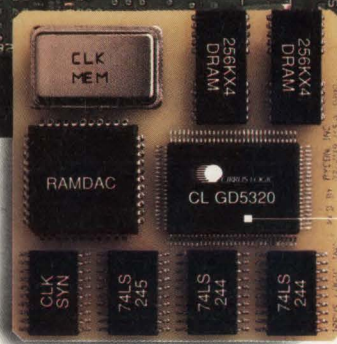
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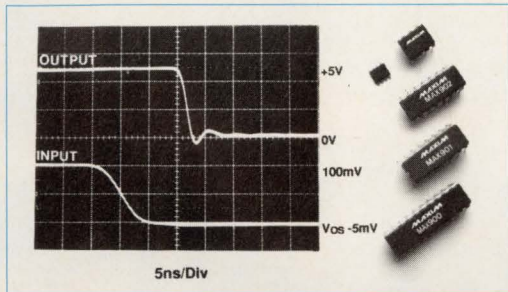
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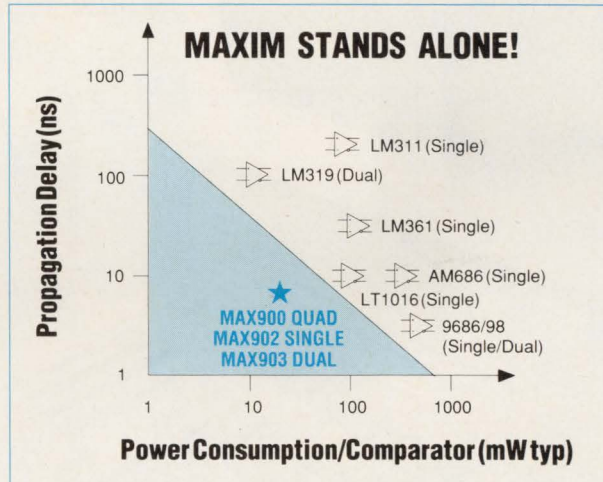
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MAX902	2	8	10	35	YES	-100mV to +2.5V	Single Ended	\$4.01
MAX903	1	8	10	18	YES	-100mV to +2.5V	Single Ended	\$3.15
MAX912 ¹	2	8	10	40	YES	-100mV to +2.5V	Complementary	\$4.00
MAX913 ¹	1	8	10	25	YES	-100mV to +2.5V	Complementary	\$3.13
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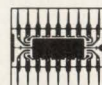
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HIGH-DENSITY PLD ARCHITECTURES

Family tree sorts out high-density PLDs

Bringing order to the welter of high-density programmable-logic devices is no easy task. After confer-
ring with numerous experts, EDN bravely offers this hopefully comprehensive and exten-
sible overview.

*Charles H Small,
Senior Editor*

A mind-numbing variety of high-density PLDs (those having more than 2000 "equivalent gates") is already available. And hardly a month passes without yet another new or enhanced high-density PLD or two becoming available. Further, unconfirmed sightings of "stealth chips" (publicized, but not announced) suggest that soon even more devices may appear.

EDN interviewed experienced users and high-density-PLD makers, asking each to take a stab at categorizing these devices. No two replies were even remotely similar. However, we synthesized some very general categories, and we submit the family-tree chart in **Fig 1** and a supplementary chart (**Table 1**) for your approval. Though comprehen-

sive, the charts need to be extensible, because when the stealth chips bolt from their secret black projects into the market, they will have to fit in somewhere.

The companies listed offer PLDs having significantly higher capacity than standard PLDs such as the 22V10. Yet notice that neither chart mentions just how much larger. The only metric available for comparing high-density PLDs' capacities is "equivalent gates." However, the high-density-PLD industry has not converged on a unified method of calculating equivalent gates. The industry is even further away from coming up with a metric that designers will accept and can use.

This lack of a useful capacity specifica-
tion for high-density PLDs is unfortu-

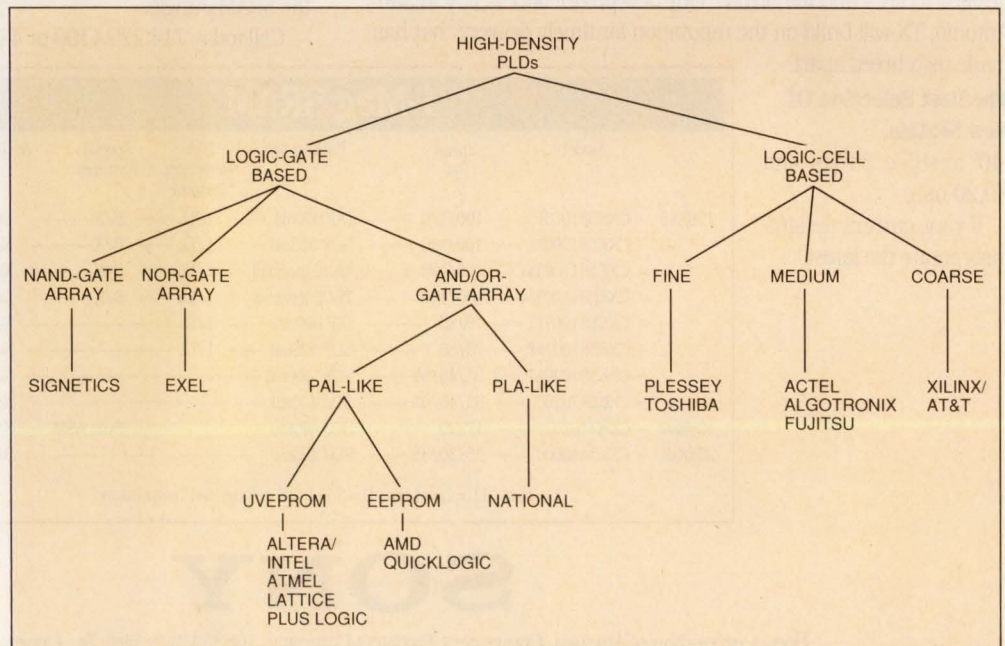
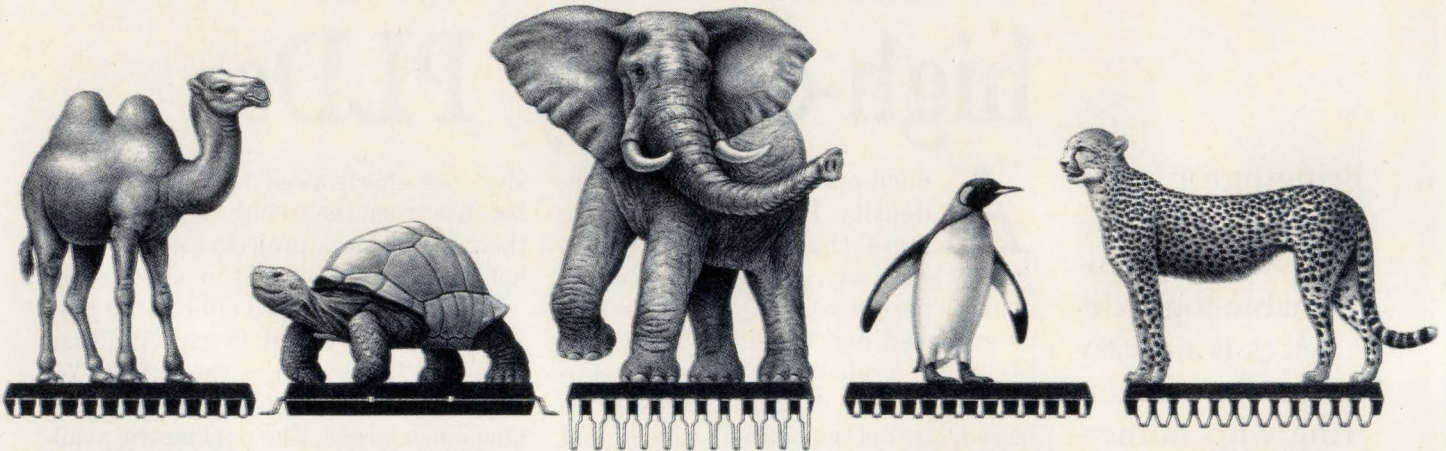


Fig 1—This family tree attempts to break down available high-density PLDs down into useful categories. Hopefully, as new devices appear, they will hang from branches that fit organically into this tree.

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Model	Speed (ns)	Packaging	Data Retention Current	Special Features	Availability	
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-- CXK581000M	100/120	SOP 525mil	L/LL	B/X	Now	
-- CXK581100TM	100/120	TSOP (normal)	L/LL	B/X	Now	
-- CXK581100YM	100/120	TSOP (reverse)	L/LL	B/X	Now	
-- CXK581001P	70/85	DIP 600mil	L/LL		Now	
-- CXK581001M	70/85	SOP 525mil	L/LL		Now	
-- CXK581020SP	35/45/55	SDIP 400mil			Now	
-- CXK581020J	35/45/55	SOJ 400mil			Now	
128Kx9 -- CXK77910J	17/20	SOJ 400mil		Sync ASM	3/Q '91	
256Kx4 -- CXK541000J	25/30/35	SOJ 400mil			3/Q '91	

L = Low LL = Low,Low B = 3 Volt X = Extended Temperature

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TECHNOLOGY UPDATE

High-density PLD architectures

nate. Experienced users agree that the three most important specs for a high-density PLD are capacity, speed, and price. Incidentally, users are not thrilled with the specs for speed either, finding that using such specs requires careful study of the fine print and considerable experimentation. And while they can get firm specs for price, most think the prices are too high.

Returning to **Fig 1**, the first and most definite cut of the analytical scalpel divides field-programmable gate arrays (FPGAs) from devices that realize canonical, sum-of-products, Boolean equations. FPGAs have largely uncommitted interconnections. That is, both ends of each possible internal connection are user programmable; the connections between logic elements on-chip are not deterministic. FPGAs compose the logic-based-cell branch of the tree.

The sum-of-products devices, in a fashion very similar to their PAL-device and PLA-device forbears, have at least one end of every internal connection fixed, leaving only one end for you to connect. Their internal connections are deterministic. Sum-of-products devices compose the logic-gate-based branch.

A couple of comments are in order. First, you must realize that FPGA is a misnomer. FPGAs do not resemble conventional mask-programmed gate arrays at all. Unfortunately, the much more apt term "logic-cell array," LCA, is a trademark of Xilinx. If you could see the die of an FPGA, you would find a rectangular array of logic cells surrounded by a phalanx of I/O cells. Running between (and, in some cases, over) the cells are uncommitted connecting lines of different length and current-carrying

capacity. The logic cells of the various FPGAs contain different amounts of logic, and you can program each device's logic cell into a unique—and sometimes quirky—set of Boolean functions.

The fewer logic elements in an FPGA's logic cell, the more fine is its "granularity"; conversely, the more logic elements in an FPGA's

Actel's Act devices were simple combinatorial-logic blocks; the company's second-generation devices have combinatorial cells and cells containing registers. Compared to Plessey's Era logic cell, Xilinx's LCA logic cell is complex, containing both combinatorial logic and registers.

Quicklogic's devices defy classification. Conceptually, they are AND/OR SOP devices. Physically, they resemble logic-cell arrays, having core macrocells surrounded by interconnection channels. Algotronix's logic-cell devices easily connect into rectangular arrays so that you can assemble large blocks of tiled, programmable logic. At press time, information on the Fujitsu devices was sketchy.

Designing with these logic-cell-based devices hearkens back to the days when engineers used discrete logic or small-scale integration (SSI). Breaking up a logic design into bits that will fit into individual cells and then connecting those cells is usually too complex a task to be done manually. Hence, designers rely on software for these tasks. The software they use has much in common with place-and-route software for printed-circuit boards.

Boolean equation realized

The logic-gate devices on the left of **Fig 1** have the same theoretical underpinning as earlier PAL devices and PLA devices: the fundamental theorem that says you can realize any logic function with a sum-of-products Boolean equation. You can sum ORed, NANDed, or NORed products leading to AND-OR, NAND-NAND, or NOR-NOR sum-of-products equations. The elegance and simplicity of these equa-

Table 1—FPGA granularity

	Granularity			Programming technology	
	Fine	Medium	Coarse	RAM	Antifuse
Actel		✓			✓
Algotronix		✓		✓	
Fujitsu		✓		✓	
GEC Plessey	✓			✓	
Toshiba	✓			✓	
Xilinx			✓	✓	

logic cell, the more coarse is its granularity. The divisions between fine, medium, and coarse granularity in **Table 1** are rough estimations made only for comparison.

An FPGA's granularity is a compromise between complexity and fan-in. If the granularity is fine, then the FPGA's simple logic cells will each need few inputs. Hence, fan-in will not be a problem. However, the device will obviously need many logic cells to perform a given function. If, on the other hand, an FPGA's granularity is coarse, then its more-complex logic cells will be relatively powerful, and you will need fewer of them for a given task. But a complex logic cell will, perforce, need more inputs than a simple cell would, perhaps leading to fan-in problems that may strain the internal-connection resources of the device.

GEC Plessey's logic cell is little more than a simple gate. Toshiba's cell is similar because both FPGAs stem from Pilkington designs. The logic cells in initial offerings of

TECHNOLOGY UPDATE

High-density PLD architectures

tions translates into a simple, regular structure for a programmable-logic device.

Their simplicity and regularity also beget simpler and faster-compiling software than the software for FPGAs. Designing with the logic-gate-based devices has much in common with designing for PAL devices. However, their prewired structure suffers from the same bugaboo that haunts PAL devices: low gate-utilization rates.

The designers of logic-gate-based, high-density PLDs have enhanced earlier PAL-device and

PLA-device architectures in several ingenious ways, striving to make their devices' layouts more flexible. Altera, for example, hard wires only three AND terms to each OR gate in its Max devices. To set up product terms having more than three ANDed inputs, you wire in some floating, uncommitted AND gates. Thus, the device does not have the rigid 8-AND-gates/OR-gate structure of many PAL devices. Note that this flexibility costs you some extra delay when you wire in floating gates.

Similarly, Advanced Micro De-

vices' Mach devices allow you to assign blocks of ANDed terms, in groups of four, among OR gates. Actel's Act devices also share product terms. Lattice's pLSI devices permit you to allocate groups' connections at several levels. National's MAPL devices contain "pages" of PLAs. Just like the MAPL devices' PLA-device ancestors, the connections between ANDed terms and OR gates are completely programmable.

Signetics' and Exel's novel devices actually come closest to meeting the literal definition of an

For more information . . .

For more information on the high-density PLDs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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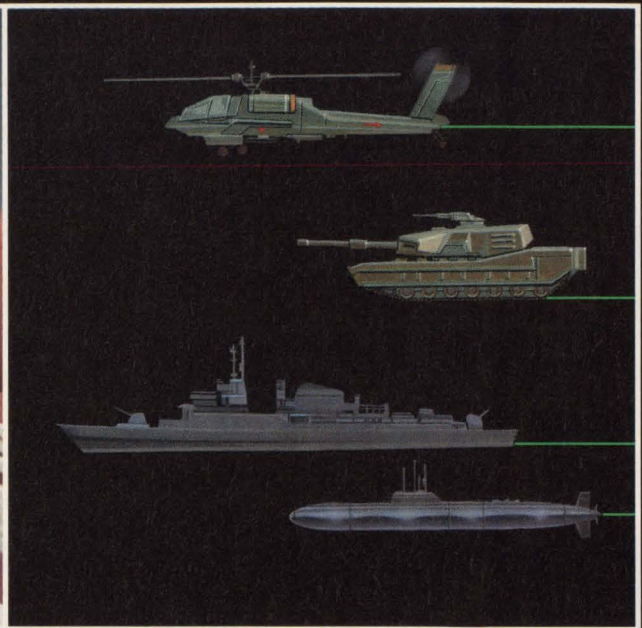
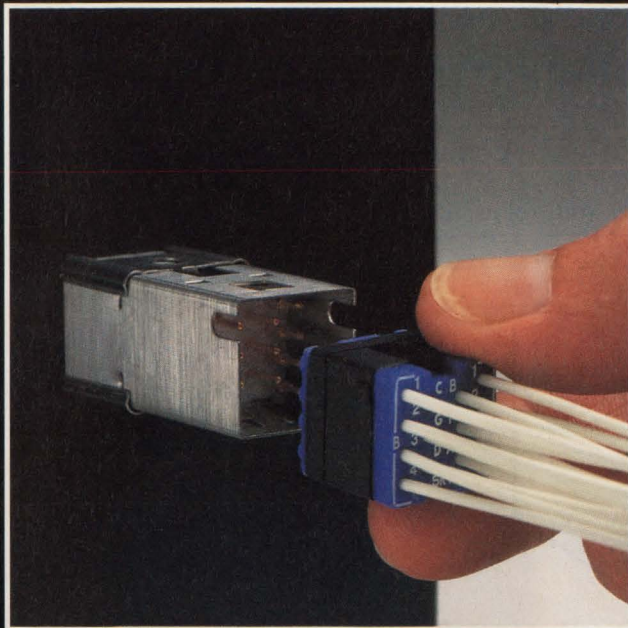
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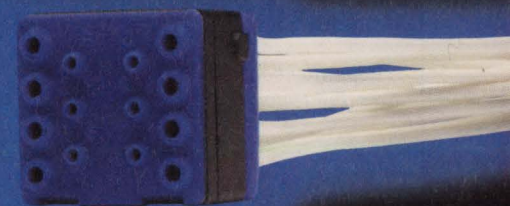
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TECHNOLOGY UPDATE

High-density PLD architectures

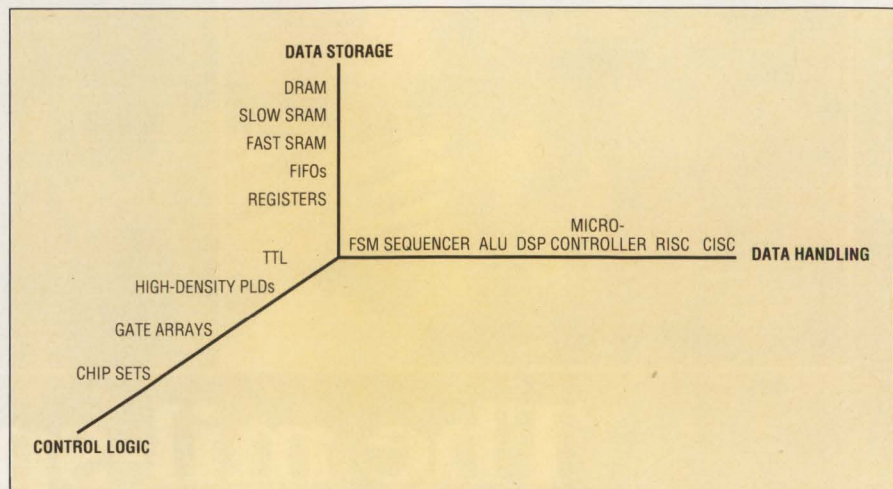
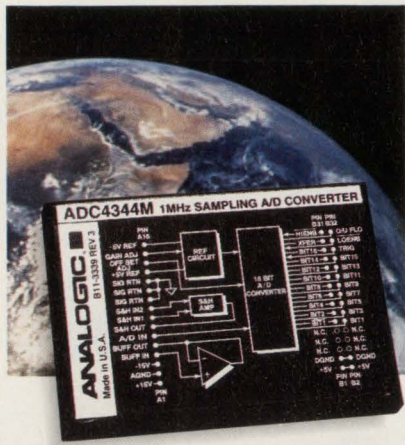


Fig 2—Right now, programmable-logic devices perform control functions. Future devices may incorporate functions from the data-storage and data-handling axes. (Courtesy Plus Logic)



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FPGA. These devices are indeed arrays of a single type of gate—NAND gates and NOR gates, respectively. However, these arrays of gates still do not even remotely resemble a conventional mask-programmed gate array. In Signetics' and Exel's devices, a programmable crosspoint matrix potentially connects any gate's output to any gate's input. Thus, these devices' so-called "folded" architecture permits chaining NAND or NOR gates to realize the sum-of-products form.

But these are no ordinary gates. Even the most brilliant logic designer will have to spend some time thinking through the possibilities inherent in, for example, Signetics' array of 256-input NAND gates. Obviously, fan-in will never be a problem.

Future high-density PLDs will add more leaves and branches to the family tree in Fig 1. Fig 2 provides a conceptual model for other areas high-density PLDs may move into. This figure ranges digital devices along three axes. Note that, except for finite-state-machine sequencers, programmable logic falls on the control-logic axis. Future

high-density PLDs could move in new directions, combining control logic with data storage or data handling.

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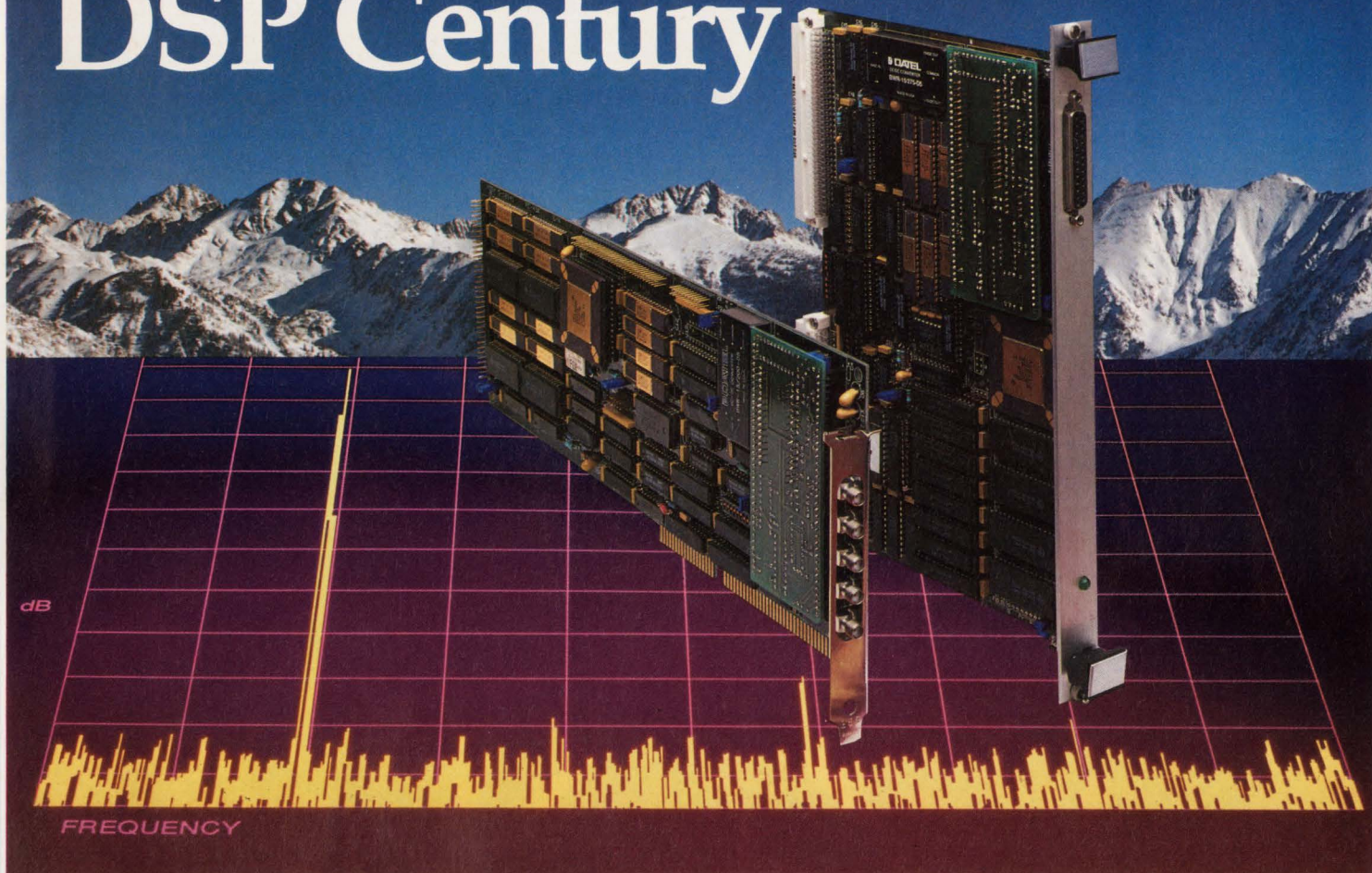
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WHAT'S COMING IN EDN

The Magazine Edition's October 1, 1991, issue will include EDN's DSP-chip directory. This annual feature updates the latest developments in the rapidly evolving technology of digital signal processing (DSP). In addition to updating the chips' many parts and features, this year's directory addresses how the choices of operating systems and interfaces to host operating systems are making DSP available to more applications.

Also coming in EDN in October and November is more from the mind of Jim Williams. We'll devote 50 pages to his study of high-speed analog design.

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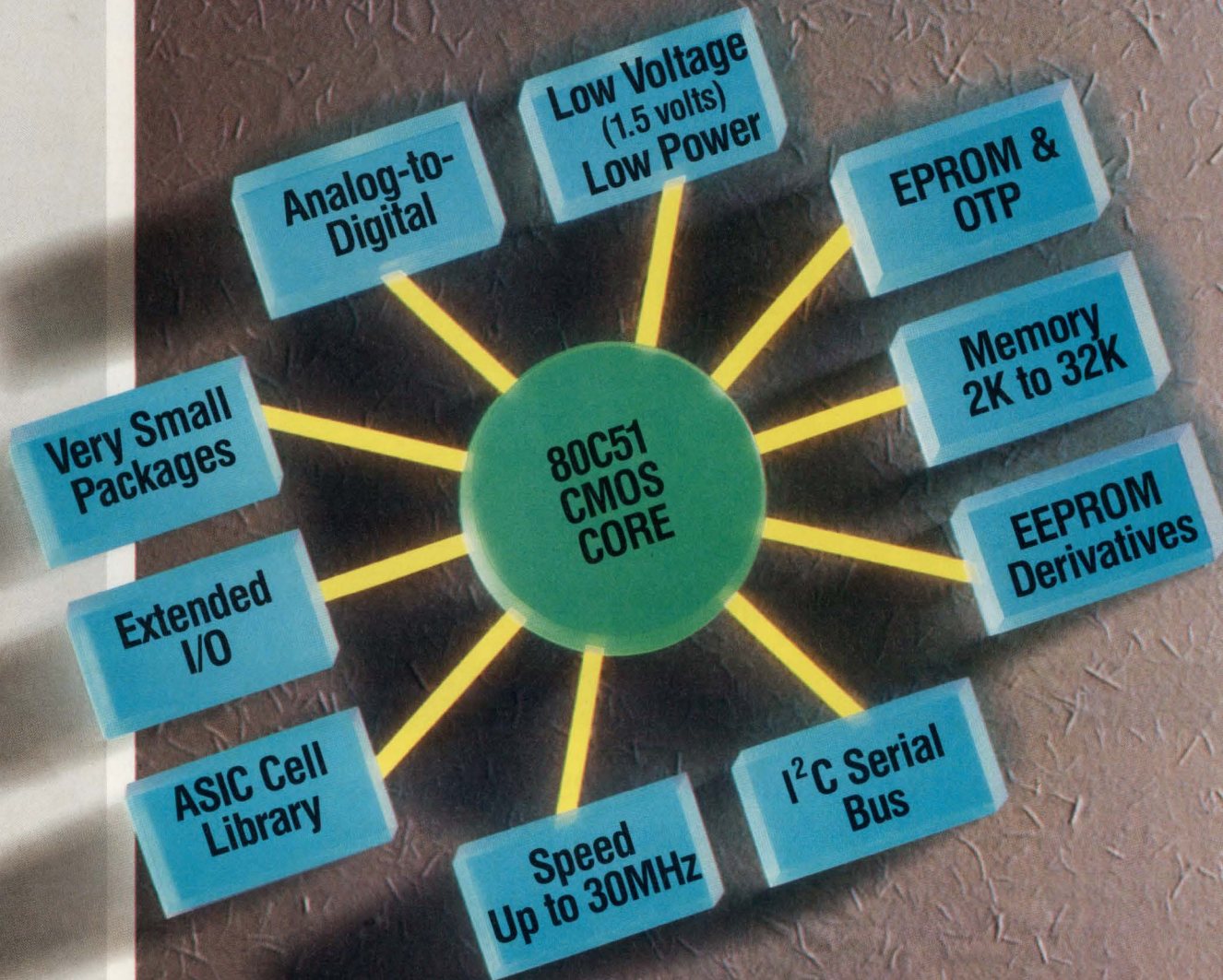
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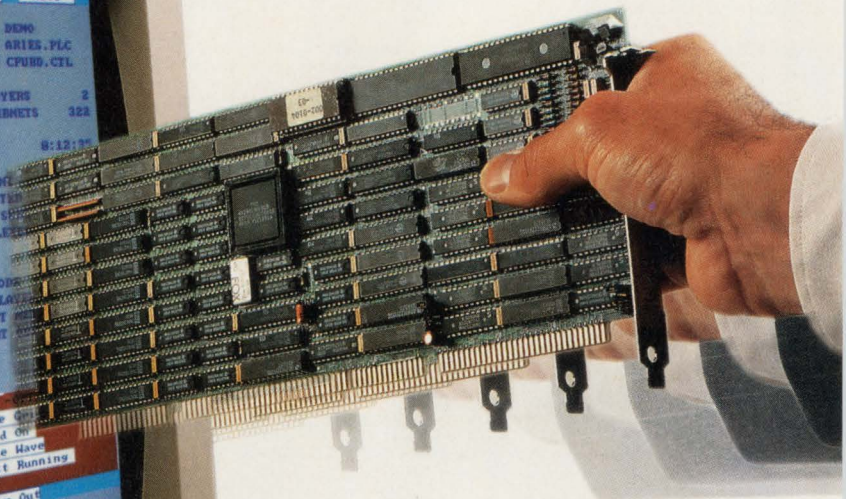
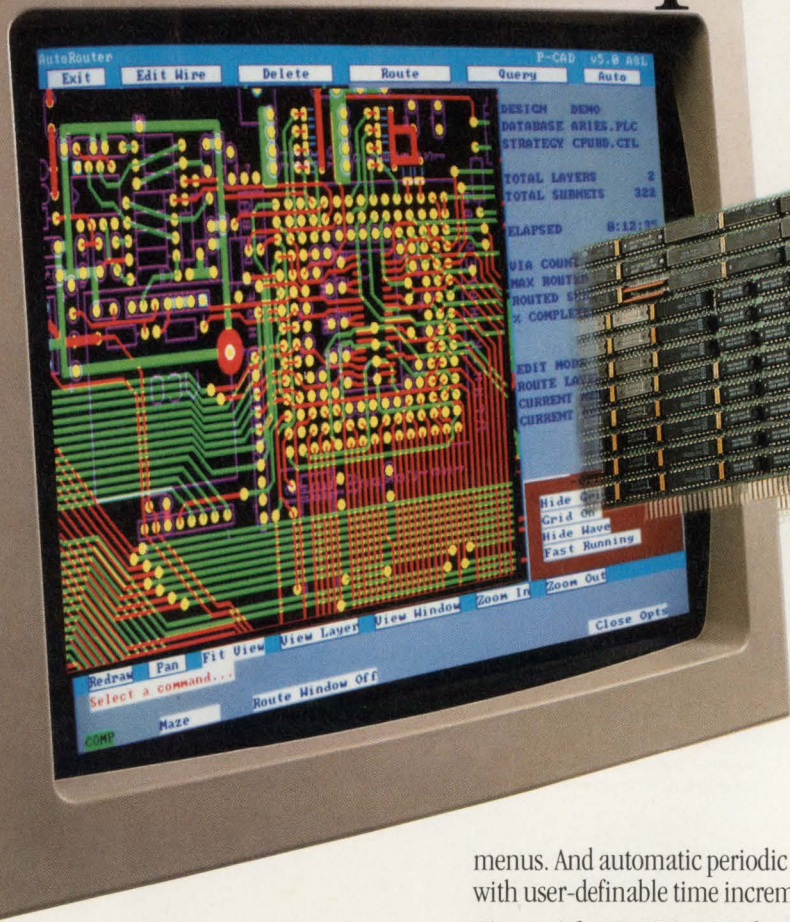
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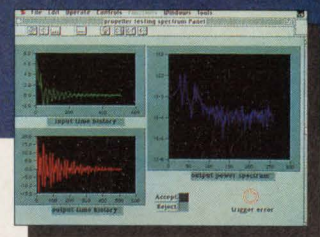
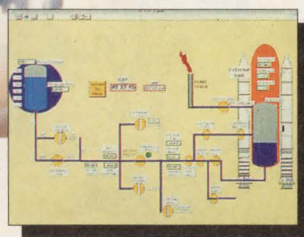
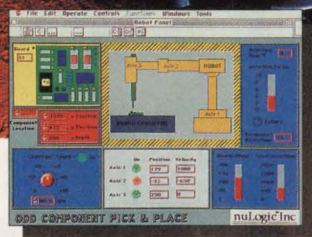
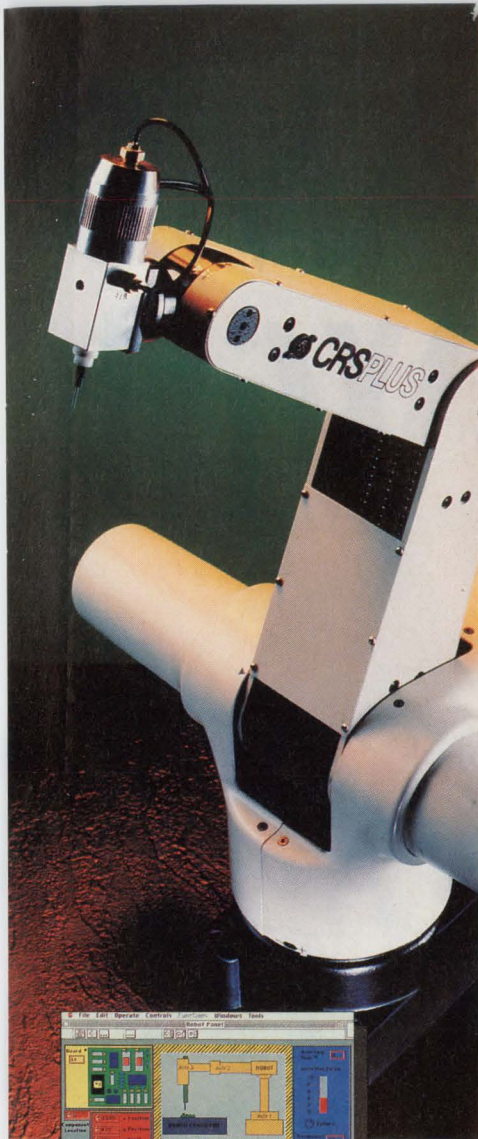
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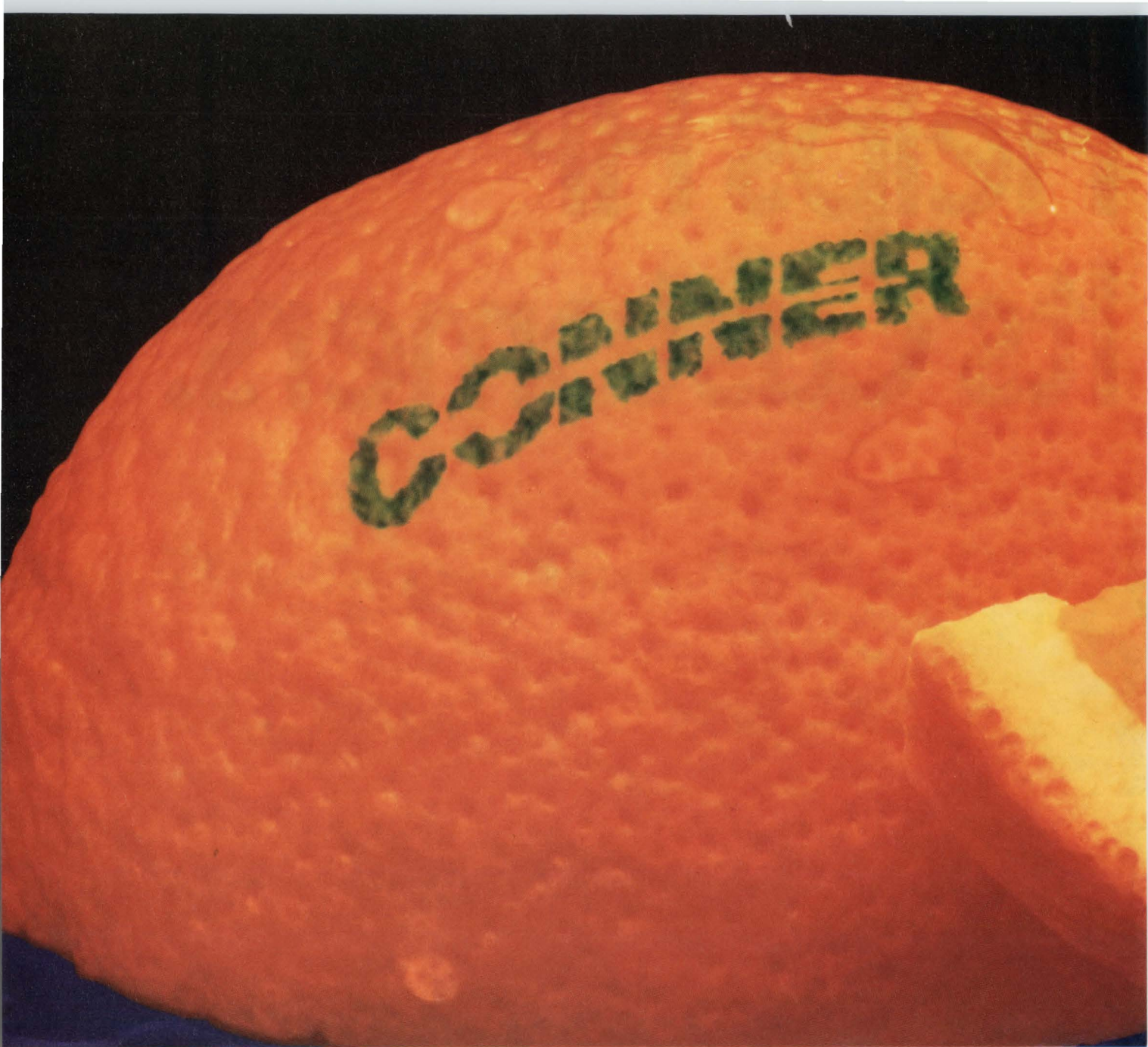
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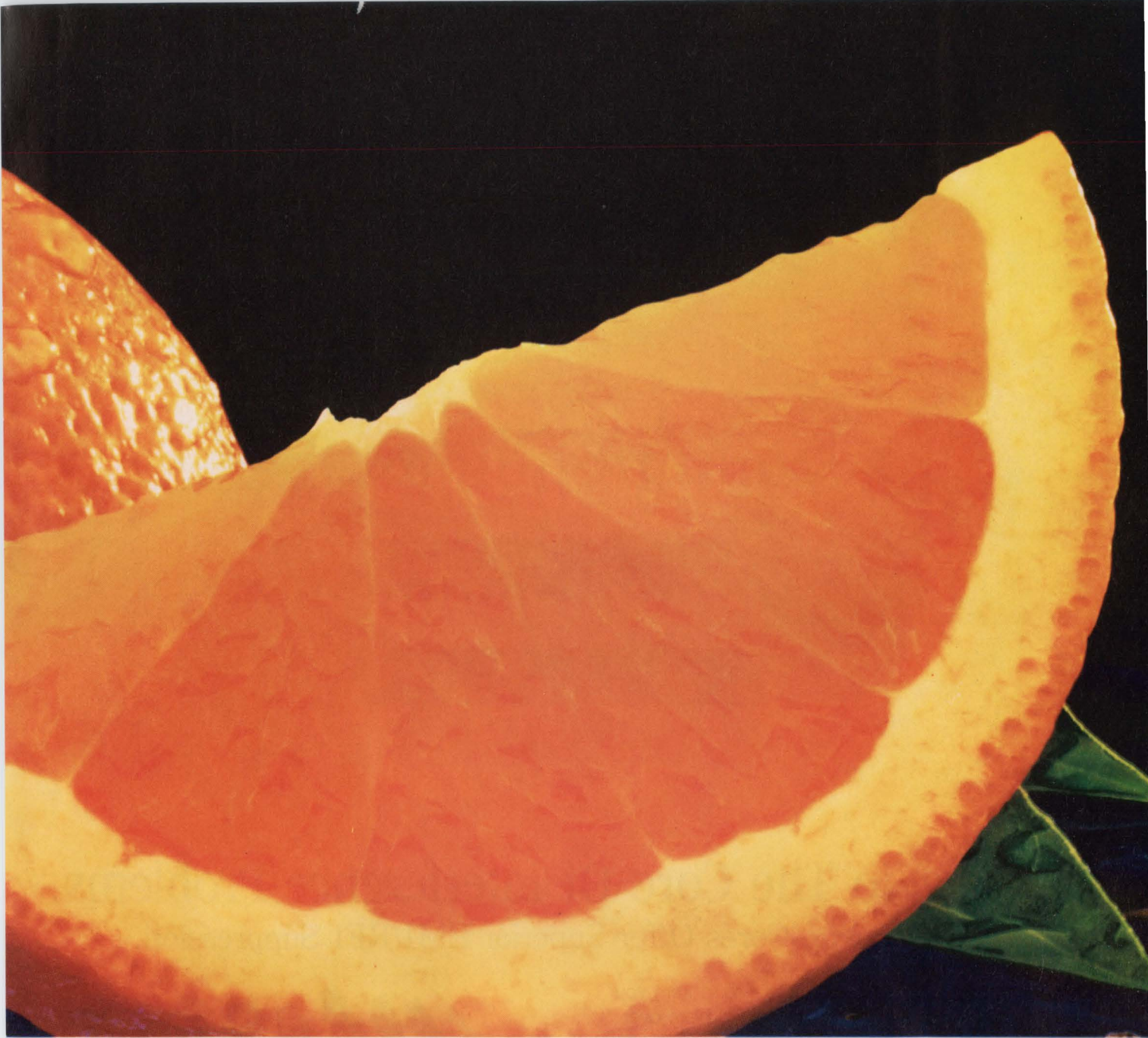


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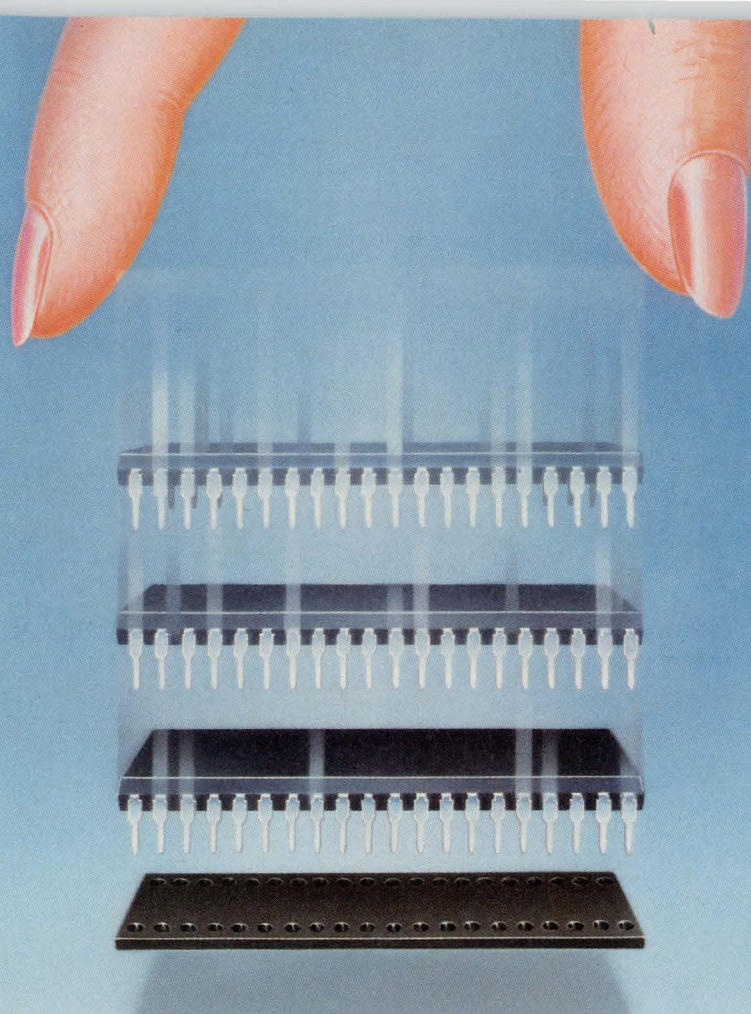
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Fig 1 depicts the IC and a simple control circuit. The D_0 and D_1 digital inputs select a delay range from a choice of four for operation. The ranges are 25 to 50, 50 to 100, 100 to 200, and 200 to 400 nsec. You set the exact delay using the RC input. The frequency-based

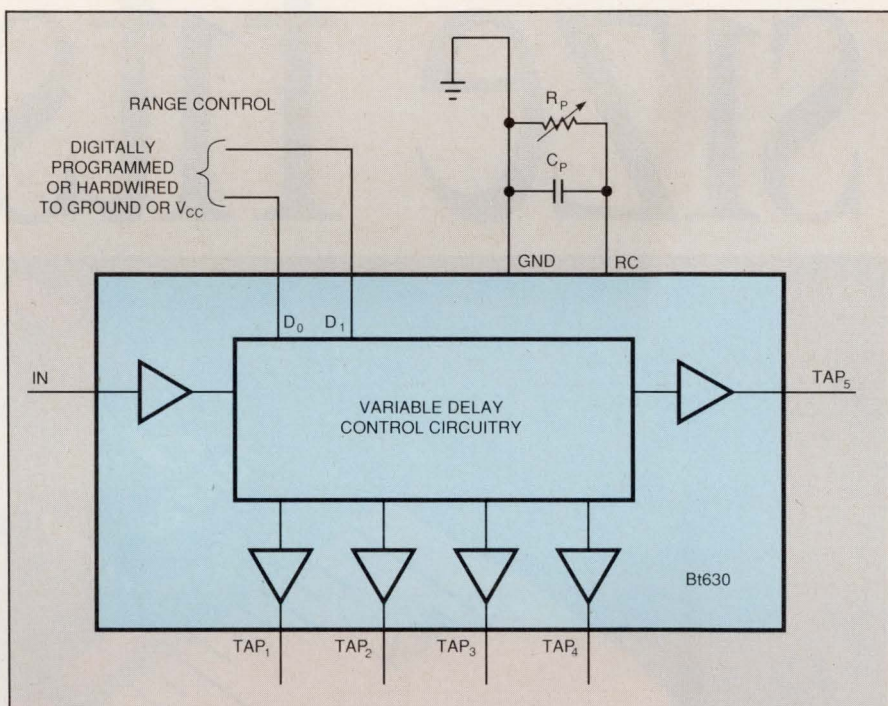


Fig 1—A simple RC control circuit and two digital inputs vary the output delay of the Bt630 delay line from 25 to 400 nsec.

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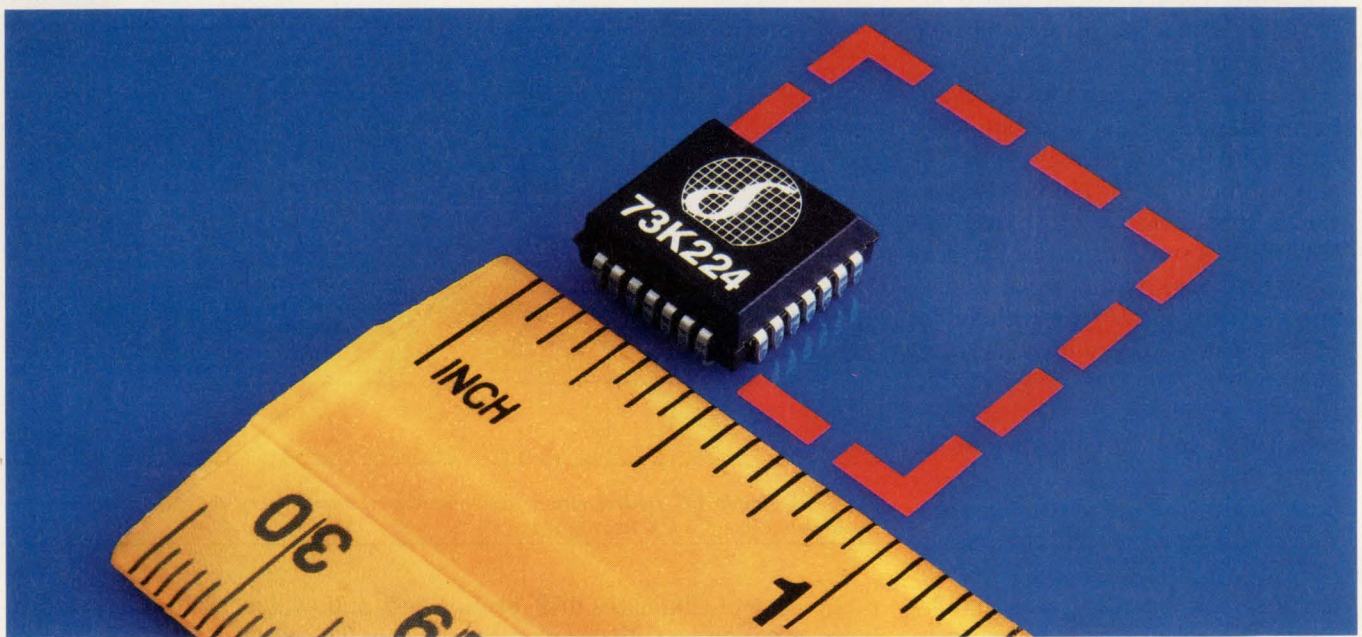
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Surface-micromachined acceleration sensor includes on-chip signal conditioning

The ADXL-50, a surface-micromachined acceleration sensor and signal conditioner is targeted for multiple automotive applications, such as air-bag devices and antiskid braking systems.

Although the science-fiction concept of a micromachined motor of pin-head size has yet to materialize, this accelerometer actually improves upon today's state-of-the-art silicon-processing capabilities. The device uses current technology in a unique way: Although accelerometers using bulk-micromachining methods to fabricate a silicon membrane have existed for several years, the ADXL-50 uses surface micromachining, a more difficult and sophisticated method.

Bulk-micromachined accelerometers combine a silicon membrane—formed by chemical etching—with thin-film piezo resistors connected in a bridge circuit. In operation, acceleration exerted on the device deforms the membrane, resulting in a change in the resistance of the piezo resistors and producing a small output from the bridge circuit. But bulk-micromachined accelerometers are usually sensitive to temperature variations—not a desirable attribute in automotive applications—and require complex external signal-conditioning circuitry to amplify and linearize the output signal. The size of bulk-micromachined devices also makes them relatively expensive.

By contrast, surface-micromachined devices are typically only 10 to 20% as large as bulk-type devices, thereby providing more efficient use of silicon real-estate. Of even greater importance, surface micromachining uses conventional IC fabrication techniques, which allow

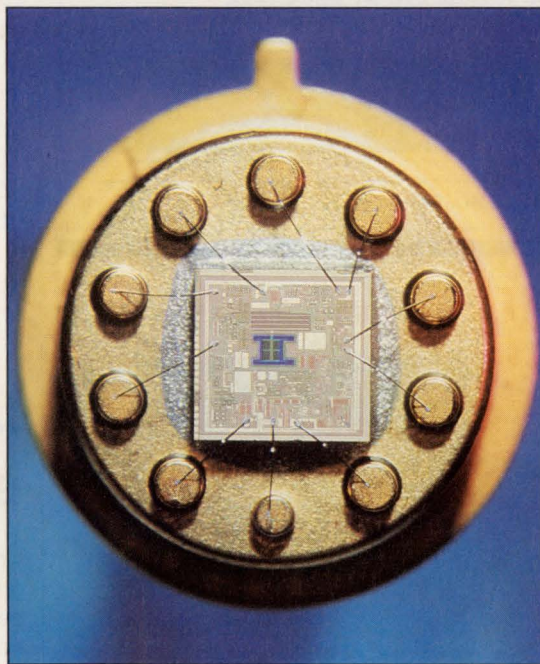
long, thin arms of the "H" act as tethers to secure the floating micromachined element to the substrate. The thicker central mass is free to move in a plane perpendicular to the tethers. Projecting from the central mass is a series of filaments that look like the fingers of

a comb. Each of these filaments is one plate of a series of parallel-plate variable capacitors; the other plates are secured to the substrate and interleave with the moving-mass plates. Acceleration or deceleration in the axis of sensitivity exerts a force on the central mass that displaces the interdigitized capacitor plates, causing a fractional change in capacitance.

The device operates within a force/balance electronic control loop. Basically, this circuitry splits a carrier signal into two phases, 180° apart. These signals then are transferred to electrodes on opposite sides of the movable center member. There is no signal on the center member if the structure is perfectly centered. Under acceleration, one capacitor increases in value while the other one decreases,

causing the phase of the carrier on the higher side to appear on the center member. Other circuitry then amplifies, demodulates, and filters this signal to produce a 0.25 to 4.74V output that is proportional to acceleration.

Compared with a membrane and piezo-resistor sensor, the capacitive sensing used in the accelerometer

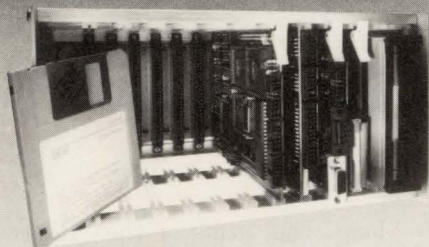


Featuring a surface-micromachined sensor, the monolithic ADXL-50 device includes signal-conditioning circuitry and a self-test capability. Designed for automotive air-bag applications, this accelerometer is also useful in antiskid braking systems.

the manufacturer to include the signal-processing circuitry on the same chip as the micromachined structure. The specific nature of its surface-micromachined structure and signal-processing circuitry distinguishes this accelerometer.

The structure forms a capacitive sensor that, when viewed from above, looks like a letter H. The

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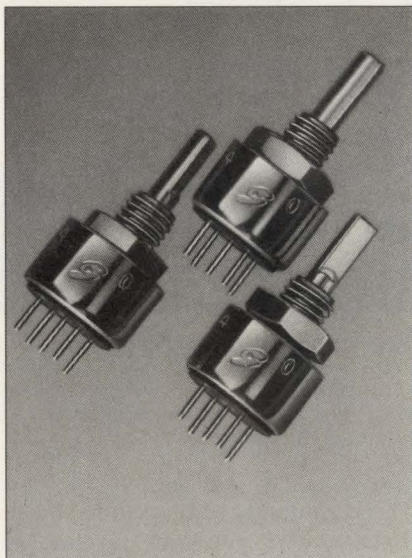
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EDN EDITORS' CHOICE

is essentially immune to temperature variations. Capacitive sensing also allows operation over a frequency range from dc to 1 kHz. In addition, the monolithic device has a guaranteed accuracy of 5% over its full $\pm 50g$ range. Of particular importance in automotive air-bag applications is the device's self-test feature that assures the user that the accelerometer is functional. Present systems use multiple switch modules that either work when needed or they don't; you can't test them beforehand. And, at about \$15 each, these modules are expensive.

The ADXL-50, which operates over the -55°C to $+125^{\circ}\text{C}$ temperature range, comes in a 10-pin, TO-100 metal can. The device costs \$23 (100); in automotive OEM quantities, it costs \$5.—*Dave Pryce*

Analog Devices, 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428.

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EDN's Editors' Choice

On occasion, a new product will show a great deal of innovation and thus appear as an EDN Editors' Choice selection. To qualify for special coverage by our editors, an innovative product must:

- Offer significantly higher levels of performance in ways not previously available
- Solve a continuing problem much more effectively than its predecessor
- Exhibit a marked degree of cleverness, which differentiates it from earlier products
- Embody new technology that advances the state of the art or use older technology in a unique and innovative way.

EDN September 16, 1991

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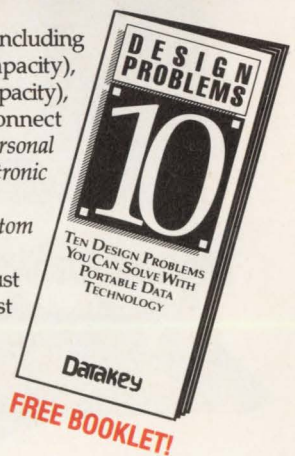
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PRODUCT UPDATE

Low-power, 1.8-in. hard-disk drive holds 21.4 Mbytes, withstands 200g shocks

Discard your notions of the appropriate applications for hard-disk drives. The 1.8-in. Model 1820 drive stores 21.4M bytes in a head-disk assembly measuring $0.394 \times 2.01 \times 2.76$ in. The drive employs a separate controller card measuring $0.276 \times 2.01 \times 3.03$ in. Together, the two components weigh 95 g. You can mount the drive and controller card independently or piggyback the controller on the head-disk assembly. The controller card has an IDE (integrated drive electronics) interface, which is the interface PCs commonly use. Engineering samples of the product cost \$485.

The disk drive runs on 5V and can run from batteries. It draws 2W while reading or writing information, 1W when idle, 35 mW in standby mode, and 15 mW in sleep mode. The drive spins up in 1.5 sec typ, so you can keep it in the sleep mode most of the time for many applications. Its automatic power management lets you realize large power savings using the drive's sleep mode while still servicing data-transfer requests.

During the first second of activation after receiving a data-transfer request, the drive consumes 3.5W. In the next second, the drive consumes 2W while performing the requested data transfer. For the next five seconds, the drive is in its 1W idle mode. While in the idle mode, the drive keeps the platter spinning in case another data-transfer request appears. If no requests are made during the 5-sec idle time, the drive drops into its 35-mW standby mode. After another five seconds

of inactivity, the drive goes into its 15-mW sleep mode. The company claims the hard-disk drive consumes much less power than competing products because of this power-management scheme.

The 1.8-in. hard drive employs a loading ramp that keeps the heads off the disks while the drive is switched off. The loading ramp gives the drive its 200g shock immunity. The ramp also pushes the number of start/stop cycles the drive can endure to 1,000,000 because the heads never touch the storage media. Because no reliability penalty is incurred for stopping the platter's rotation, the 1.8-in. hard drive can save power by frequently entering its idle and sleep modes. Consequently, the automatic time delays for activating these modes are much shorter than

for disk drives that land their heads on the media when the platters stop rotating.

The drive's electronics are on a separate controller card, so you can fit the device into thin spaces. The controller and head-disk assembly communicate via a flat cable. The controller circuitry includes a 32-kbyte data buffer, and the IDE disk interface can transfer data in bursts at 4 Mbytes/sec. The drive's average seek time is 20 msec, and the heads can move from track to track in 8 msec. A 40-Mbyte version will be available in the second quarter of 1992. —**Steven H Leibson**

Integral Peripherals Inc, 5775 Flatiron Pkwy, Suite 100, Boulder, CO, 80301. Phone (303) 449-8009. FAX (303) 449-8089.

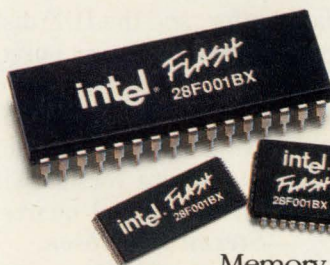
Circle No. 730



About the size of a small matchbox, this 1.8-in. hard-disk drive can store 21.4 Mbytes and operate from batteries.



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Updating your system code, to say the least, has been a pain. Well, erase those painful memories.

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CIRCLE NO. 104

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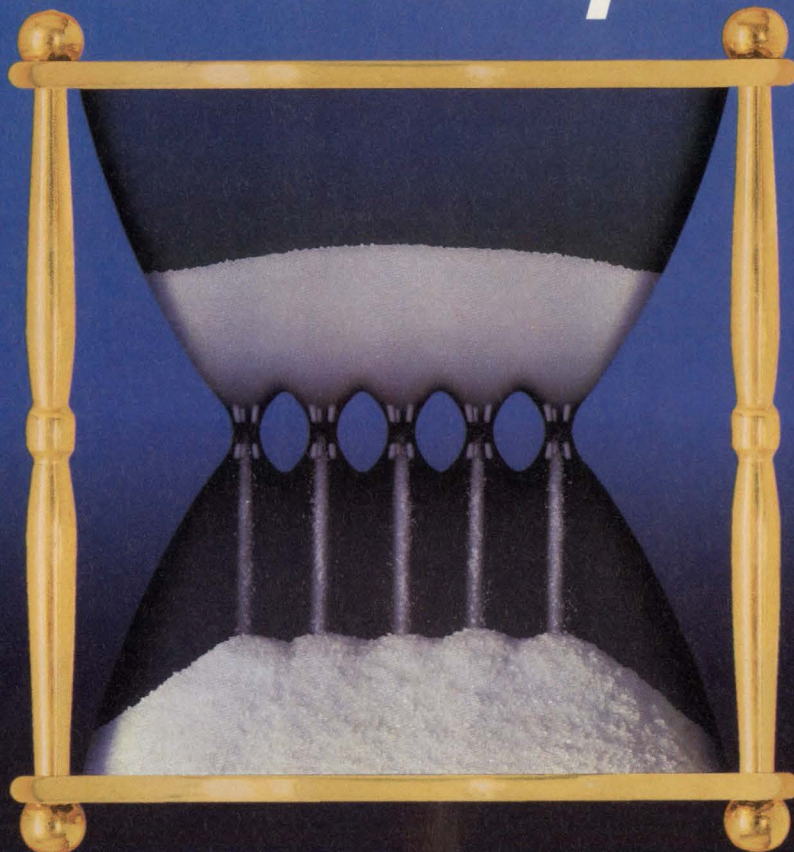
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The K-Series' unique architecture includes a revolutionary Peripheral Management Unit™ macro service for nonstop instruction execution while processing up to 16 I/O requests at the same time. By designing in the K-Series microcomputer, you can improve your system throughput by as much as 5X.

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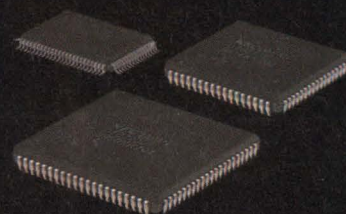
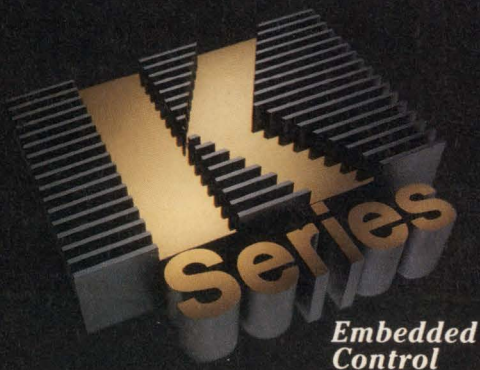
The K-Series provides you a worry-free upgrade path from the 8-bit K2 microcontroller family to the 16-bit K3 devices. And your future designs will exploit the power of the lightning-fast 125-ns K6, with real-time operating system in

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TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Breaking the analog barriers to optimum system design

IN THE ERA OF

MegaChip

TECHNOLOGIES



Advanced Linear extends the boundaries of system performance.

Innovative analog circuits from Texas Instruments add a new edge to Digital Equipment's proven market winners. They can do the same for you.



The goal Digital Equipment Corporation set was clear: Strengthen its position as the leading supplier of Ethernet-based local area network products. Achieving the goal has been spurred by the use of Advanced Linear circuits from Texas Instruments.

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Expertise and teamwork carry the day

For many years, Digital has used a wide variety of TI linear circuits — from op amps to mixed-signal devices — and values our analog viewpoint toward system design.

As Digital defined the requirements to meet its market goal, the decades-long relationship entered a new era of even more intense cooperation. With Digital handling system-level design and TI applying its linear expertise, the two teams fully utilized our LinASIC™ design methodology to create a series of mixed-signal Ethercell™ functions. They are the basis for the advanced linear devices Digital requires.

The design flow was aided by our

Boston-area Regional Technology Center that provides access to LinASIC development tools and by the extensive use of EDIF to exchange information.

Enhancing Digital's competitive edge

To date, close teamwork has produced components that can enhance Digital's ability to respond quickly to market demands for feature-rich but lower cost Ethernet and communications products:

- A dual driver and dual receiver IC that minimizes the number of components required for the Attachment Unit Interface (AUI) function in an Ethernet network.

“Utilizing TI’s LinASIC mixed-signal design methodology allows us to design cost-effective solutions with aggressive time-to-market goals.”

— Nick Ilyadis, Product Engineer
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As Digital recognizes, few in the industry can match our experience in analog design and digital design. This expertise enables us to effectively combine high-performance

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Let us help you meet your challenge

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Our service circles the globe, and our worldwide manufacturing capability can support your production schedules wherever you are.

TI's analog viewpoint: From process technologies come Advanced Linear ICs.

TI's LinASIC mixed-signal methodology —

A cell-based design methodology allowing the combination of high-performance analog and digital functions on the same chip. This mixed-signal capability is used for many of our catalog products and for custom/semicustom solutions. It is supported by large cell libraries, design-automation tools and these TI Advanced Linear wafer process technologies:

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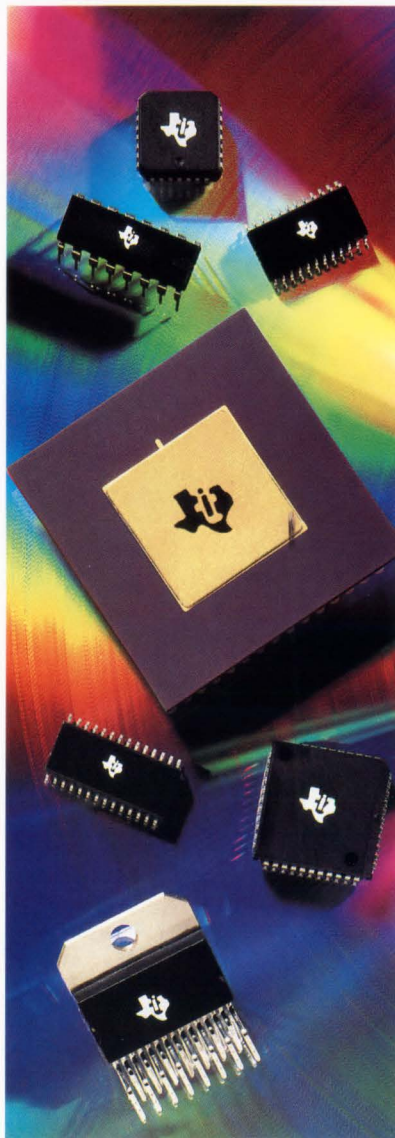
Advanced LinCMOS — An N-well, silicon-gate, double-level polysilicon process featuring improved resistor and capacitor structures and having three-micron minimum feature sizes.

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For more information on our Advanced Linear process technologies and the products they are producing, call 1-800-336-5236, ext. 3425.



TI's LinASIC methodology and Advanced Linear process technologies are enhancing these product families

Data Transmission — This family meets the needs of most industry-standard interfaces (EIA, IEEE, ANSI) and ranges from drivers/receivers/transceivers to fully integrated controller/transceivers.

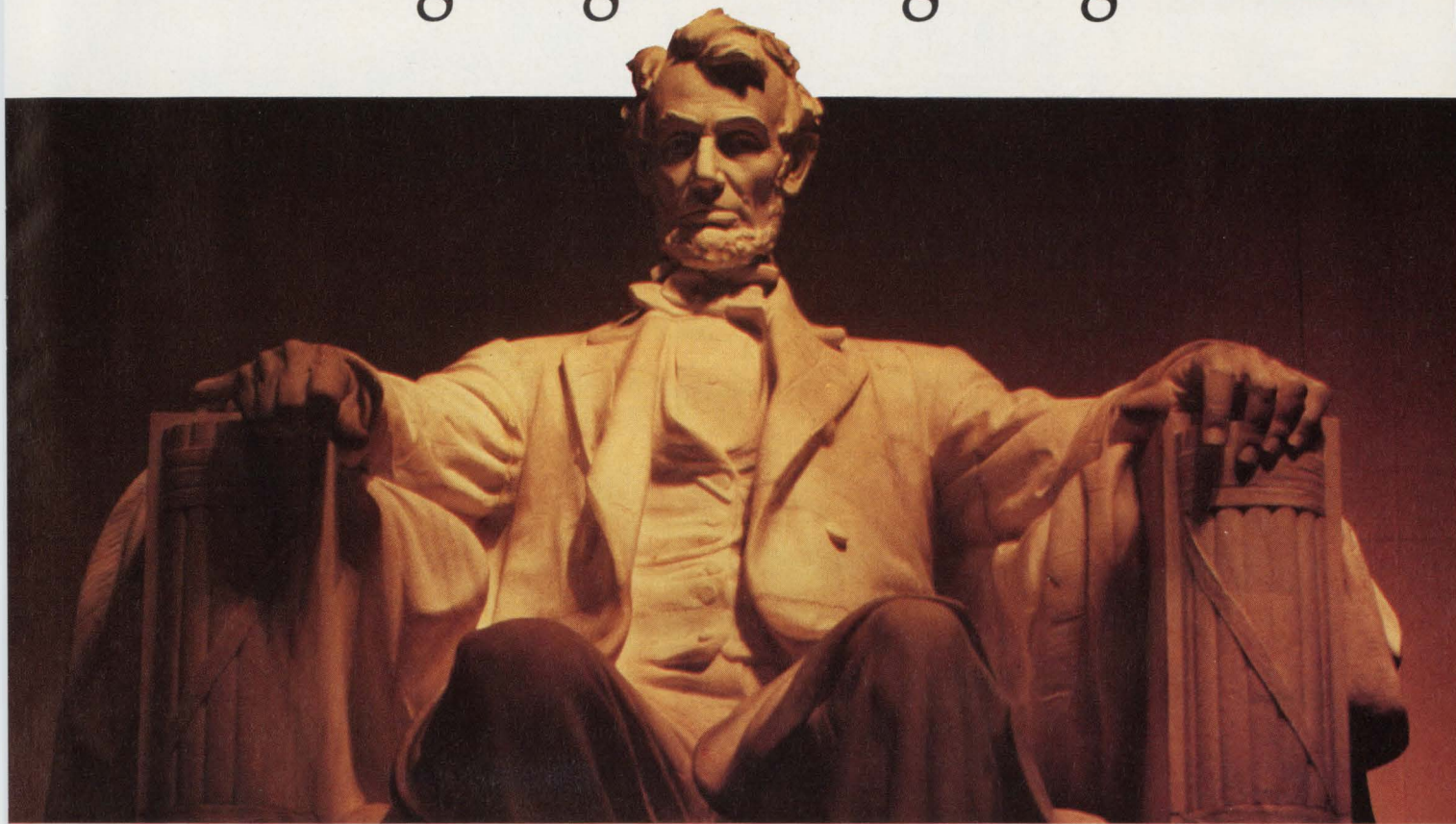
Data Acquisition — The family ranges from stand-alone A/Ds and D/As to complete data conversion subsystems on a chip; from general-purpose functions to highly integrated digital signal processor and graphics signal processor analog interface circuits. Other specialized family members include telecom and speech synthesis functions.

Intelligent Power — These devices combine high-voltage and/or high-current switches with the analog and digital circuitry required to perform interface, control, protection and diagnostic functions in microcontroller-based systems.

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Custom/semicustom Functions — In modifying existing products to fit your needs or in defining your own unique functions, our LinASIC methodology allows access to existing analog cells used in the development of our catalog products and compatibility with our digital cell libraries.

Announcing a night to recognize greatness



EDN's Innovation and Innovator of the Year Awards Ceremony

On the night of November 19 during Wescon, EDN will present the 1991 Innovation and Innovator of the Year awards at the Mark Hopkins Hotel in San Francisco. You are invited to show the finalists that you support greatness in innovation by attending the awards ceremony that is the culmination of their hard work. Through its Innovation Crusade, EDN hopes to inspire

engineering professionals within the electronics field to reach for higher plateaus of inspiration and creativity.

The dedication and involvement of EDN readers, like yourself, have made the Innovation Crusade and awards ceremony a reality. By taking the time to nominate your peers and, in

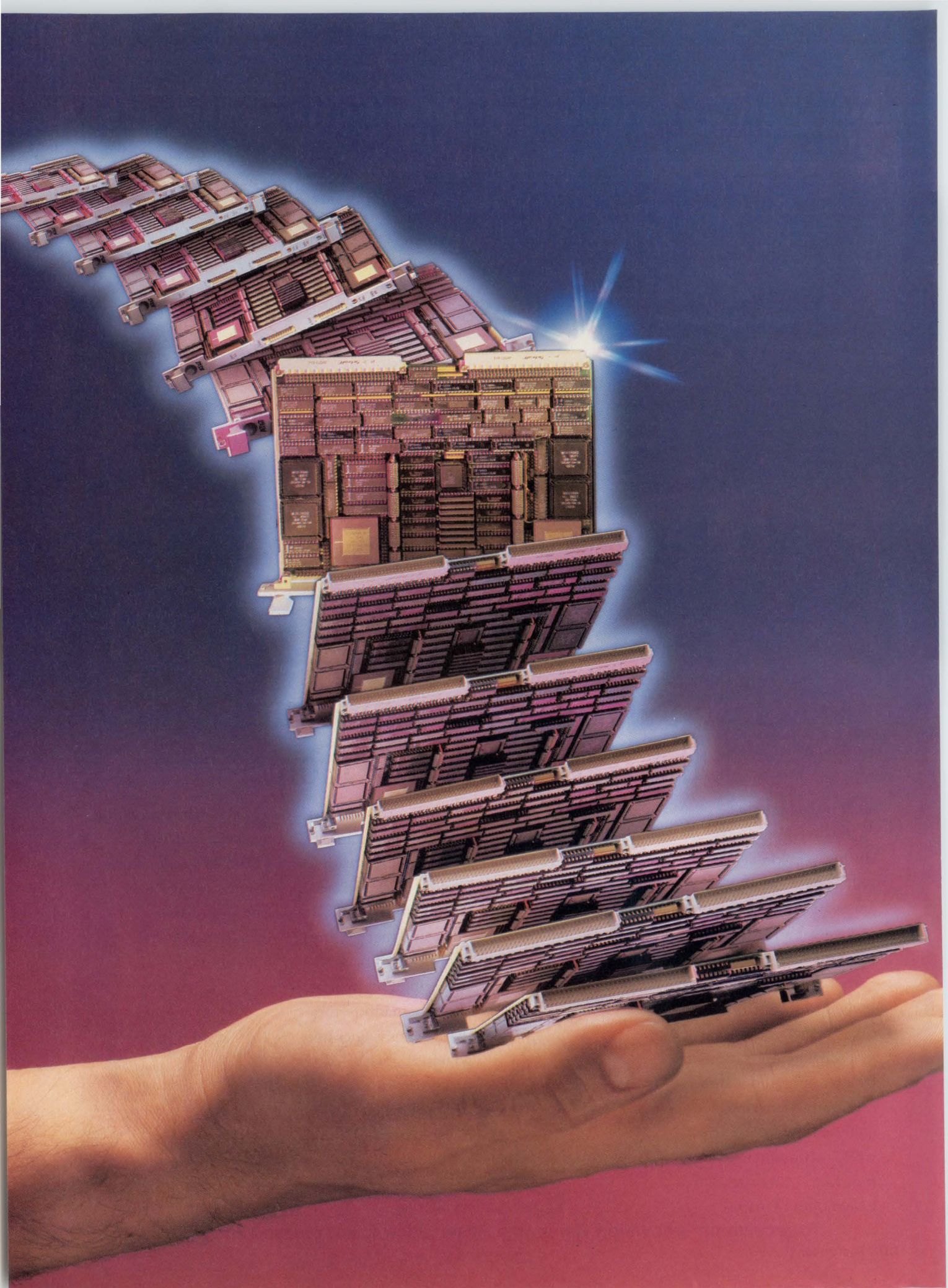
fact, select the winners, you show commitment to quality and creativity in electronics and are driving this crusade. But don't stop there ... order your ticket to the industry event of the year and show these innovators that greatness does not go unrecognized. All proceeds of the dinner will be donated to the EDN Scholarship Fund.

To receive a reservation order form to the EDN 1991 Innovation Dinner and Awards Ceremony, fax Pam Winch at (617) 558-4470.



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DSP coprocessor boards

The technology in these number crunchers is developing so fast that about the only things moving faster are the instructions and data they handle. Besides faster μ Ps, architectural innovations—especially parallel and pipelined processors—are adding to the boards' speed. But as is so often the case, software is struggling to keep pace.

Dan Strassberg, Associate Editor

Digital signal processing (DSP) is one of the most rapidly evolving areas of electronics. And within the DSP field, coprocessor boards are quite possibly the fastest-changing product category. Most of these boards plug into a computer's I/O bus and increase the computer's speed by performing DSP functions while the main processor handles housekeeping chores and other low-speed tasks. In April 1990, when EDN last took a comprehensive look at these boards (**Ref 1**), they were just beginning to employ parallel and pipelined processors. Today, the use of multiple DSP chips is rapidly becoming commonplace. However, system developers who use the boards have few software options to simplify allocating tasks among the multiple μ Ps.

Table 1 (pg 112) lists 38 DSP coprocessor boards from 26 firms. We se-

lected these products from a field of more than 70 boards, most of which had not yet been introduced at the time of our April 1990 story. In choosing units for the **table**, we picked products that, by and large, did not appear in our earlier listing and which, in our opinion, indicate trends. As noted above, one trend is the use of multiple processors. Twenty of the boards in the **table** contain more than one μ P. And the product information that vendors sent us covered even more multiprocessor boards. Another clear trend is the use of floating-point DSP chips. Two dozen of the boards in the **table** include them.

Despite its throughput limitations, the ISA bus—represented by 20 boards—remains the most popular bus for DSP coprocessor boards. All but one of the ISA bus boards are for the 16-bit, IBM PC/AT version. The VMEbus is well represented too; 11

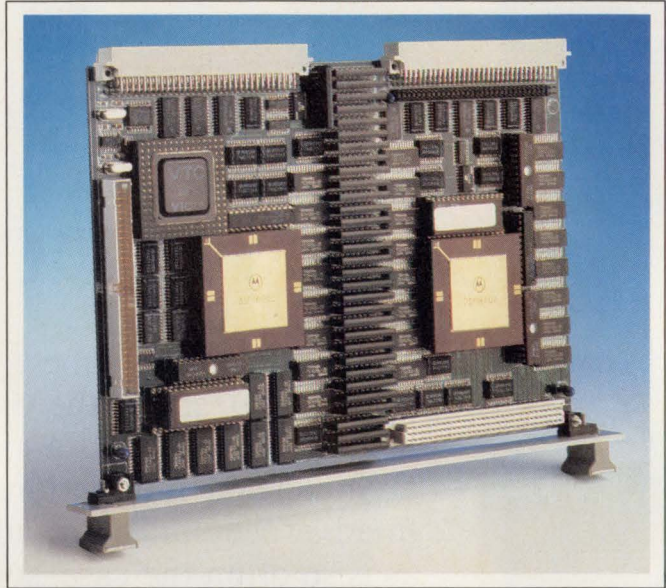
DSP coprocessor boards incorporate multiple μ Ps, high-speed I/O, and extensive memory capacity to broaden the field of applications within your computer's grasp. (Photo courtesy AT&T Microelectronics and Heurikon Corp)

Processors from Texas Instruments, Motorola, and AT&T are the most prevalent, with a smattering of boards using parts from other semiconductor companies.

boards plug into the VMEbus. The **table** also shows three Nubus boards for Apple Computer's Macintosh II family, one Micro Channel Architecture board for IBM's PS/2 series, one board for the STD Bus, and one board in the diminutive Sbus format of Sun Microsystems' SPARCstations. Bear in mind that, despite its length, the **table** lists no more than half of the boards introduced in the past 18 months. For example, although the only Sbus board shown comes from Sonitech International, at least one other firm, Ariel Corp, makes Sbus DSP boards. Moreover, nearly all of the boards in EDN's April 1990 listing are still available.

As you might expect, processors from Texas Instruments, Motorola, and AT&T are the most prevalent, with a smattering of boards using parts from other semiconductor companies. Intel's i860 makes an appearance on a VMEbus board from CSPI. CSPI chose the Intel RISC chip because of the μ P's extremely powerful floating-point processor. CSPI's competitors don't question the chip's floating-point capability; they do ask whether the i860's performance justifies its price. Some doubt whether the i860, which has the I/O structure of a general-purpose processor, can keep pace with the I/O data rates DSP chips must usually handle. CSPI is not alone in liking the i860 for DSP, though; you should look for the IC in board-level DSP products scheduled to appear within the next six months from at least one other manufacturer.

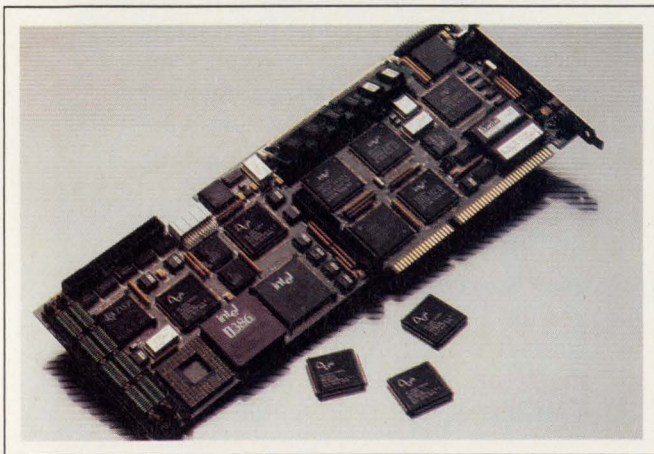
The i860 is not the only unusual DSP μ P to appear on a DSP board. Array Microsystems' boards use the



The board size, the bus's high performance, and the capabilities of workstations that use the bus are some of the reasons for the growing popularity of VMEbus DSP coprocessor boards. Without appearing particularly crowded, Ariel Corp's V96 contains two DSP96002s and a massive amount of memory.

firm's own frequency-domain processor and controller chips. Array's literature boasts that its boards let you "plug in the world's fastest DSP." Impact Technologies' Viper 8704/30-30 sports four vector processors from Zoran Corp. Multisignal Technology's MTAP-90 also uses four processors, three of which come from United Technologies. Two of the listed boards use processors from Analog Devices Inc. One comes from the transoceanic partnership of Spectrum Signal Processing in British Columbia, Canada and Loughborough Sound Images in England. The other is the lowest-priced board in the **table**, Street Electronics' \$175 Echo DSP, scheduled for introduction next month. Analog indicates that several other firms offer coprocessor boards based on its DSP chips, but these board vendors failed to respond to our information requests.

Most DSP operations are I/O intensive. Consequently, many DSP boards have extensive I/O capabilities. As standard features, at least six of the listed boards provide analog I/O facilities (A/D and D/A converters). Many other boards have high-speed parallel or serial digital I/O ports. Some of the parallel ports, especially the wide ones, are extraordinarily fast. Two vendors specify their boards' parallel-port transfer rates at 20M bytes/sec. One claims its port operates at 40M bytes/sec, and another says its port runs



A complete 25-MHz i386DX-based PC and a 33-MHz TMS320C31 DSP μ P work together on Spectrum Signal Processing and Loughborough Sound Image's Media-Link DSP/PC, a full-length board for the 16-bit ISA bus in passive-backplane systems.

at 64M bytes/sec. (That's more than 0.5G bits/sec!)

Despite many engineers' perceptions that DSP techniques are mainly for speech and audio work, the use of DSP has expanded into motion control and many other fields. As DSP applications diversify, users' I/O requirements are changing. Board vendors are responding to the changing requirements in several ways. One way is the inclusion of mezzanine buses. Mezzanine buses turn plug-in boards into small systems. A mezzanine bus is a connector with defined pinout and timing standards that accepts daughter cards. The daughter cards usually perform I/O functions, but some provide other facilities. For example, they can add extra memory for a processor, and sometimes they contain additional (parallel) processors.

Mezzanine-bus daughter cards often fit within the confines of the board they plug into, but not always. Sometimes, the daughter cards occupy additional slots in the bus that accept the main board. In such cases, the daughter cards may connect with the main bus only to receive power and ground. Daughter cards that occupy main-bus slots receive mezzanine-bus signals from the main board via a short cable or "frontplane." A frontplane is a printed board or semirigid set of conductors that plugs onto a connector at the edge of a board opposite its main-bus connector.

A mezzanine bus by another name . . .

Apparently, some vendors use definitions of a mezzanine bus that are broader than the one given above, whereas other firms use more restrictive definitions. For example, Datel Inc sells its DSP boards only with plug-on daughter cards that perform I/O. Even though Datel has a family of pin-compatible daughter cards, the company refuses to categorize these cards' interface as a mezzanine bus. When you review the **table**, be mindful that different vendors have different understandings of the meaning of a mezzanine bus.

Although bus-board manufacturers have defined several mezzanine buses, each of which is vying for acceptance as a de facto industry standard, only a few of these buses appear on the listed boards. One mezzanine bus that is compatible with products from at least three DSP-board vendors is Data Translation's DT-Connect. The **table** shows a large number of proprietary buses. In general, if you select a board that uses a widely supported mezzanine bus, you will have a greater choice of compatible devices than if you select a board whose mezzanine bus is proprietary.

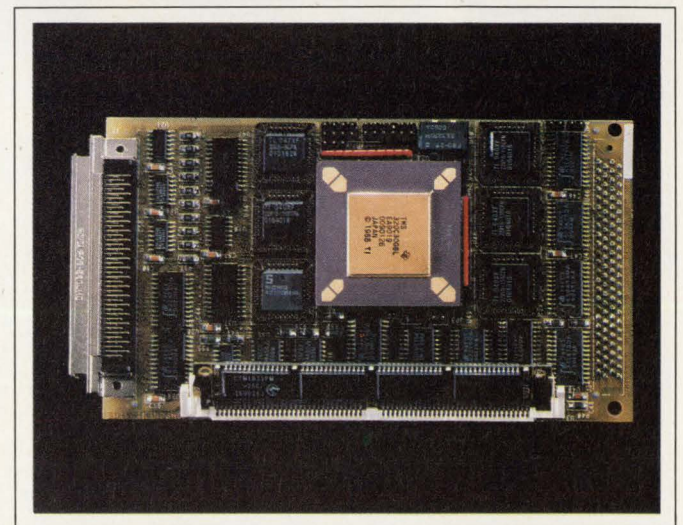
Not only is DSP I/O intensive, it is memory inten-

sive. Some of the listed boards have provisions for accommodating prodigious amounts of memory. DSP μ Ps need fast memory, and the boards almost always implement their fastest memory with static random-access memory (SRAM) chips. Often, the boards configure the SRAM as cache, but the maximum size of the cache is frequently larger than the tens of kilobytes common with most CISC (complex-instruction-set-computer) μ Ps.

For economy (and to hold pc-board area within practical limits), when DSP boards accommodate many megabytes of memory, most of the memory usually consists of dynamic RAM (DRAM). DRAM, though slower than SRAM, is less costly and more dense. Approximately one-third of the listed boards accommodate 8M bytes or more of DRAM without need of mezzanine-bus memory cards. The **table** lists six DSP boards that accommodate 64M bytes of DRAM. The six boards come from three vendors. Note that 64M bytes is more storage than you'll find on the much slower but nonvolatile hard disks of most personal computers in use today!

DSP work demands EEs' skills

As has happened time and again during the last decade, hardware developments have outpaced software advances. Many of the key players in DSP applications development have had no formal training in software engineering. Instead they are EEs who have acquired software skills on the job. But DSP work cries out for



Packing DSP onto the tiny format of Sun Microsystems' Sbus presents a difficult challenge to board designers. But several firms have met the challenge. One of them is Sonitech International.

Table 1—Representative DSP coprocessor boards

Vendor	Model; when introduced; price	Processor/clock speed (MHz)/ number of processors	Bus/DMA?/ mapping	Mezzanine bus/width (bits)/speed (bytes per sec)	Memory (bytes) for program and data		I/O functions	
					Min	Max	On base board	With mezzanine card(s)
Analogic/CDA	MSP-8C30; 5/91; \$7050 to \$18,500	TMS320C30/33/2	ISA-16/yes/ NS	SCSI/8/1.5M; Pixel/16/NS	0-D ² 64k-S ³	32M-D	SCSI, \$500 Pixel bus connects to separate VCA ⁵ card.	
Array Microsystems	a66550; NS ¹ ; \$11,900	a66111/25/1/ a66211/25/1 ⁶	ISA-16/no memory	NA	768k	768k	I/O port—15-MHz burst-rate I/O; magnitude and phase	NA
Ariel Corp	DSP-C40; 6/91; \$4995	TMS320C40/NS/1	ISA-16/yes/ I/O and memory	DT-Connect/ 16/20M ⁷ Proprietary/ 32-bit/40M	1M-D 32k-S	64M-D 6M-S	2-channel, 16-bit over-sampling ADC and DAC	Industry-standard digital-audio interface, Next computer DSP port
	MP3210; 5/91; \$4995	DSP3210/33/2	ISA-16/yes/ I/O and memory	DT-Connect/ 16/20M Proprietary/ 32-bit/40M	1M-D 16k-S	64M-D 2M-S	See unit above	See unit above
	MM-96; 6/90; \$3995 to \$5995 (dual processors)	DSP96002/33/1 or 2	ISA-16/yes/ I/O and memory	DT-Connect/ 16/20M Proprietary/ 32-bit/30M	1M-D 192k-S	64M-D 768k-S	All I/O functions are on external cards	NA
	Quad-processor; 11/91; \$8995 to \$13,995	DSP56001/NS/2 or 4	VME 6U ⁹ / yes/NS	Proprietary/ 24/NS	144k-S	576k-S	Next computer DSP port	NA
Atlanta Signal Processors Inc	Vortex; 5/91; \$4995 to \$13,995	TMS320C40/50/1 TMS320C31/33.33/1	ISA-16/yes/ I/O and memory	'C31/32/ 22.2M Memory/ 32/33.3M	2M-D 256k-S	64M-D 2M-S	6 8-bit, 20M-byte per sec communication ports; 2 1-way, 16-bit ports; 1 serial	Industry-standard digital audio interface, \$1195; 16-bit dual ADC DAC, \$795
	Banshee \ VMD; 1/91; \$4995 to \$14,295	TMS320C30/33/1	VME 6U/ depends on host/memory and I/O	'C30/32/ 22.2M	256k-S	16M-D 2M-S	1 TTL serial; 2 RS-422	See unit above
	Cheetah; 6/90; \$3995 to \$12,795	DSP96002/33/1 DSP56001/NS	ISA-16/yes/ I/O and memory	96002 I/O/ 32/22.2M Memory/ 32/22.2M	64k-S	64M-D 2M-S	2 TTL serial	See above Multiprocessor interface, \$995
AT&T Microelectronics	WE-DSP32C-BD-VME; Q4/90; \$9995	DSP32C-5E/25/4 DSP32C/25/2	VME 6U/ yes (serial and parallel ports)/ memory	Serial bus/ 2 wire/100k (Phillips IICbus)	1M-D 512k-S	4M-D 512k-S	2 25M bit per sec serial; 20M byte per sec parallel	NA
Burr-Brown	ZPB3400; 6/91; \$4495	DSP32C/50/1 or 2	VME 6U/ yes/ memory	Proprietary/ 18/20M	1M-D 256k-S	4M-D 512k-S	NA	Several analog I/O cards
Communications Automation and Control Inc	XC4-A0; 3/91; \$995 to \$1295	DSP-32C/40/1	ISA-8/no/ I/O	NA	64k	256k	Serial communication with ADCs, DACs, DSP boards	NA
	MC5-C0; 6/91; \$1495 to \$3495	DSP-32C/50/1	Micro-channel/ NS/NS	Proprietary/ serial/16M bps	256k	1M	Serial communication with DSP boards	Serial communication with mezzanine boards

Notes:

1. NS=Not specified.
2. '-D' after number of bytes denotes dynamic random-access memory (DRAM).
3. '-S' after number of bytes denotes static random-access memory (SRAM).
4. NA=Not applicable.
5. VGA=IBM Video Graphics Array display standard.
6. Also performs block floating-point operations.
7. The DT-Connect standard originated with Data Translation Inc.
8. 'OS'=operating system.
9. The so-called '6U' VME board is the most common VMEbus board size.
10. Although the boards are available only with daughter cards, the vendor does not describe the interface between the main card and the daughter cards as a mezzanine bus.
11. I/O daughter cards mount to Tiger 40 board but cause the board to use two bus slots.
12. '-E' after number of bytes denotes electrically programmable read-only memory (EPROM).
13. In the \$5995 version, the UT69532 operates at 15 MHz and performs 75M floating-point operations per sec (FLOPS).
14. MOPS=millions of operations per sec.
15. SRAM is divided equally between processors. Each processor's memory is half local and half global.
16. '-N' after number of bytes denotes nonvolatile memory.
17. '-R' after number of bytes denotes read-only memory.

DSP coprocessor boards

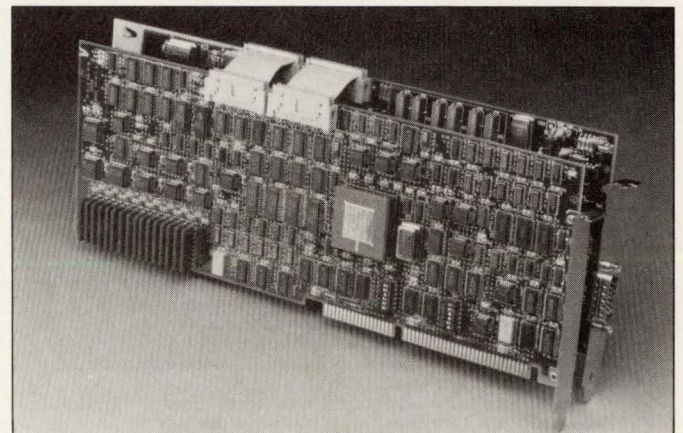
Supporting software (and price, if not included with board)	Comments
Drivers for Interactive Unix; image libraries; MSPrtx OS ^a	Dual-banked memory lets both processors access 32M bytes of RAM simultaneously with no wait states.
IBM PC- and VAX-based system simulators	Vendor says board does FFT-based frequency-domain functions faster than any competitor. Vendor also sells VME boards using same μ Ps.
Assembler/linker, optimizing C compiler, C drivers, DT-Connect drivers applications libraries	Has oversampling inputs and outputs with tracking filters.
C compiler/assembler; C drivers; DT-connect drivers; VCOS OS; applications libraries	Same as unit above. In addition, dual processors perform 50M FLOPS peak.
Optimizing C compiler and OS, \$2425; C and hardware drivers; monitor; applications libraries	Proprietary Hyperbus has two ports per board, allowing daisy chains of indefinite length. Dual processors perform 100M FLOPS peak.
C drivers; Assembler/linker, \$495; Symbolic debugger, \$495	Operates at 54 MIPS. Lower indicated price includes two processors; higher price includes four.
Assembler/linker/C compiler; source debugger; Spox OS; signal generation and analysis, \$3000	The 'C31 can process I/O for the 'C40 or can function independently. Uses dual-port memory for communicating with host PC. The Ashell program provides an integrated development interface.
Assembler/linker/optimizing C compiler/source debugger, \$1595	Listed software tools run on IBM PCs. Data communication uses true dual-ported memory.
See Vortex board	Works with same Ashell program as Vortex board. 56001 processors can control I/O or function independently.
C compiler assembler, simulator, applications library, \$3800	175M floating-point operations per sec; 75M instructions per sec. All three I/O ports (2 serial; 1 parallel) have DMA.
Driver, monitor; applications developer (DisplayXL), \$1495	
Assembler/linker/simulator, \$495; C compiler, \$1000; application library, \$95; debugger, \$395	A similar board for the 16-bit ISA bus (Model AC5-A0) costs \$200 more and has a 50-MHz DSP32C. This board also has the serial mezzanine bus of the board below.
See board above; also spectral display/digital scope (no charge)	

Table continued

EEs' background in the underlying theory relating the time- and frequency-domain descriptions of signals; the work does not place a premium on the discipline that a software-engineering curriculum instills. DSP work also demands the resourcefulness that many EEs have developed through working on projects without having sufficient tools.

EEs are pragmatic as well as resourceful, though. When they have the option of creating their own tools (because few exist) or taking advantage of existing ones, they will usually try to use what's available. For example, EEs no longer write much DSP code in assembly language. The advent of complex floating-point DSP chips with rich instruction sets and tools such as high-level-language compilers and source-level debuggers has made coding DSP routines in assembly language unattractive in comparison with writing high-level code. Of the high-level languages, C is by far the most popular. Assembly still often gets the nod for fixed-point DSP chips and for coding routines whose operating speed is critical. Usually though, system software developers don't write such routines themselves; they take the routines from libraries developed by others.

Multiprocessing has added a new dimension to developing DSP applications software. The most straightforward multiprocessing case occurs in a real-time system that has many similar input channels, each of which produces data requiring identical or nearly identical processing. If a single DSP μ P can't handle all the processing chores quickly enough, several processors can. You can assign groups of channels to each μ P, but you have to make sure not to assign more tasks to a processor than it can complete before it must work on the next set of data.



Mezzanine buses make for flexible expansion of a DSP board's I/O, memory, or processing capabilities. Here, Data Translation's DT-Connect bus (on the ribbon cables at the top) links a frame grabber board to the firm's DT2878, which contains a DSP32C.

Table 1—Representative DSP coprocessor boards (continued)

Vendor	Model; when introduced; price	Processor/clock speed (MHz)/ number of processors	Bus/DMA?/ mapping	Mezzanine bus/width (bits)/speed (bytes per sec)	Memory (bytes) for program and data		I/O functions	
					Min	Max	On base board	With mezzanine card(s)
Communications Automation and Control Inc	SC5-A0 12/90; \$1495 to \$1795	DSP-32C/50/1	STD (8 or 16 bit)/no/ I/O	Proprietary/ serial/16M bps	64k	256k	See board above	See board above
CSPI	Supercard SC-2XL/ VME; 6/91; From \$8500	i860/40/2	VME and VSB/yes/ memory	CSPI (publicly available)/ 64/160	2M	16M	VSB interface is operation	NA
Dalanco Spry	250; 12/90; \$1095 to \$1395	TMS320C25 or TMS320E25/40/1	ISA-16/no/ I/O	Proprietary/ 16/20	72k	384k	DSP serial port; 8-channel 12-bit ADC (250k samples/sec) timer; 2 12-bit DACs	None
Data Translation	DT2878 Series; 10/90; \$4495 to \$7995	DSP32C/50/1	ISA-16/no/ I/O	DT-Connect/8 or 16/10 MHz	2M	8M	NS	Frame grabbers; image processors; data-acquisition boards
Datel Inc	PC-430 Series; 5/91; \$3995 to \$4595	TMS320C30/32/1	ISA-16/yes/ I/O and memory	NS ¹⁰	512k-D 32k-S	512k-D 32k-S	All configurations include daughter cards	Variety of ADCs to 4M samples/sec; serial ports
DSP Research	Tiger 40; 8/91; \$4995 to \$6995	TMS320C40/50/1	ISA-16/yes/ NS	2 (I/O and memory)/32/ 100M DT-Connect/ 16/40M	64k-S	66M-D 2M-S	Six communication ports	¹¹ Digital sound I/O; telephony interface 12-bit analog I/O
Eighteen Eight Laboratories	PL2500 Series; 1/91; \$2495 to \$5995	DSP32C/50/1	ISA-16/yes (3 channel)/ I/O	Span 32/32 (data) 24 (address)/20	256k-E ¹² 256k-S	4.25M-S	NS	Boards interface to DT-Connect, Univision bus, and memory
Heurikon	Surfboard; 8/91; \$8495 to \$9695	DSP32C-5E/25/4 DSP32C/25/2	VME 6U/ yes (serial and parallel ports)/ memory	Serial bus/2 wire/100k (Philips IICbus)	1M-D 512k-S	4M-D 512k-S	2 25M bit per sec serial; 1 20M byte per sec parallel	NA
Impact Technologies	Viper8704/ 30-30; 1990; \$15,990 to \$33,990	Zoran ZR34161/30/4	This board was described more fully in EDN's April '90 directory but is included here because of its unusual use of four vector processors.					
Multisignal Technology Corp	MTAP-90; 8/91; \$5995 to \$6995	One UT69532IQMAC Two 74ACT8832As One 74ACT8818/ all 20 MHz ¹³	ISA-16/no/ through address and data registers	Proprietary/ 32/80M	768k-S	4M with mezzanine board	Data transfer via 6 local buses	NA
National Instruments Corp	NB-DSP2301; 5/91; \$3495	TMS320C30/27/1	NuBus/yes/ memory	RTS/serial bus/8.33M bits per sec	256k	1.28M	NA	Vendor supplies 9 boards for RTSI bus
Pacific Cyber/ Metrix Inc	DSP-3A; 6/91; \$17,779	TMS320C30/40/3	VME 6U/ yes/ memory	Yes (not named)/32/ 100M	2M	3.5M	VSBbus; 3 40M-byte per sec parallel ports	NA
Pentek Inc	4823; 6/90; \$6995 to \$7995	TMS320C30/32/1	VME 6U/ NS/memory and I/O	Intel Mix bus/ 32/10M	128k-E 256k-S	8M-D	2 serial (synchronous); 2 timer/counters; 2 general I/O	10 types include ADCs, DACs, and additional μ P

Notes:

1. NS=Not specified.
2. '-D' after number of bytes denotes dynamic random-access memory (DRAM).
3. '-S' after number of bytes denotes static random-access memory (SRAM).
4. NA=Not applicable.
5. VGA=IBM Video Graphics Array display standard.
6. Also performs block floating-point operations.
7. The DT-Connect standard originated with Data Translation Inc.
8. 'OS'=operating system.
9. The so-called '6U' VME board is the most common VMEbus board size.
10. Although the boards are available only with daughter cards, the vendor does not describe the interface between the main card and the daughter cards as a mezzanine bus.
11. I/O daughter cards mount to Tiger 40 board but cause the board to use two bus slots.
12. '-E' after number of bytes denotes electrically programmable read-only memory (EPROM).
13. In the \$5995 version, the UT69532 operates at 15 MHz and performs 75M floating-point operations per sec (FLOPS).

DSP coprocessor boards

Supporting software (and price, if not included with board)	Comments
See board above	
pSOS + Unix-compatible OS, C and Fortran compilers for SPARC CPUs	
Assembler, debugger, hardware interface routines, waveform editor, sample code (included)	Includes FIR filter code generator and data-acquisition software. Block move commands transfer data to PC memory at 3M bytes per sec without DMA.
C compiler, \$1500; support library, \$500; advanced image-processing library, \$1495	
Driver, DSP library, scheduler, boot code, \$495	Total harmonic distortion more than 68 dB below full scale to fifth harmonic. Can transfer 4M samples per sec without pauses (1 channel).
C source debugger, libraries for all on-board devices and communicating to host	Development package with optimizing C compiler, \$1495. As many as 16 boards connect together. PC- and workstation-based tools support multiple μ Ps.
598 microcoded routines in PROM; support for C, Fortran, and Pascal included	You can call the microcoded routines from high-level programs in languages from seven vendors. Runtime software supports 8 boards simultaneously.
C compiler, assembler, simulator, applications library, \$3800	175M floating-point operations per sec, 75M instructions per sec. All three I/O ports (2 serial, 1 parallel) have DMA.
Microprogram routines, monitor, debugger included	Meta-assembler, \$2000. Sustained operation at 100M FLOPS and 40 MOPS. ¹⁴ Slave unit adds 2 ALUs and a floating point unit.
Analysis library, \$695; interface kit, \$295; Labview 2, \$1995; developer tool kit, \$2500	Board has master and slave NuBus interfaces. When board is slave, bus master can write to memory on board. As master, board transfers to host memory.
Support function library and development utilities included	Performs block DMA at 80M bytes per sec. Cross-compiler kit and Spox OS, \$5100. FIFO buffers between μ Ps and to external ports.
Debugger, Spox OS with ADC and DAC drivers; run on Sun-4 and IBM PC/AT	Board vendor has ported Comdisco Systems Signal-Processing Workstation software to this board.

14. MOPS=millions of operations per sec.

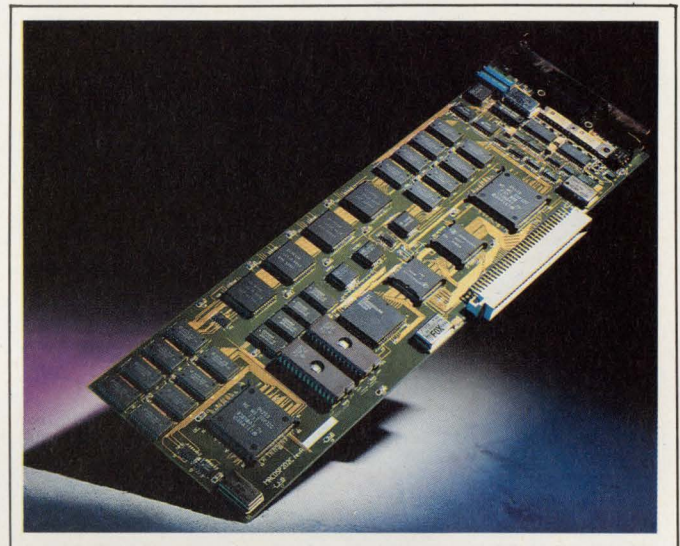
15. SRAM is divided equally between processors.

Each processor's memory is half local and half global.

16. '-N' after number of bytes denotes nonvolatile memory.

17. '-R' after number of bytes denotes read-only memory.

Table continued



Using the Macintosh II family to develop and run DSP applications is simpler if you have a powerful coprocessor board. This unit from Spectral Innovations includes two DSP32Cs and runs Apple's Real-time Operating System Executive (A/Rose).

Another approach—exemplified by boards from AT&T and Heurikon—uses both parallelism and pipelining. In these boards, there are two groups of three pipelined processors. The three processors in each group work in sequence on the same data: The first processor places its output data in a buffer; the second processor takes data from the buffer, processes it further and deposits it into a second buffer; the third processor receives its input from the second buffer and does still more processing. The processors run algorithms that divide the tasks so the buffers don't overflow and the processors don't have to wait for new data. The pipelined processors are fast enough to keep up with new data as it appears in real time.

Designing the algorithms so that the pipelined processors get along harmoniously and keep up with real time is not a trivial job. So far, there doesn't appear to be any commercial software that automatically optimizes the sharing of tasks among the processors. However, Comdisco's (Foster City, CA) Signal-Processing Worksystem (SPW), a \$25,000 (approximately) workstation-based development package, optionally includes a graphical tool called Multiprox (MPX) that assists you in dividing the work. Once you've made a cut at assigning the tasks to processors, SPW will generate the code and simulate the results. If you are unsatisfied, you can try dividing the work differently.

As happens early in the life of most technologies that exhibit great potential, DSP is in ferment. The processor chips' capabilities are increasing rapidly. The cost of a given amount of computational power is declin-

Table 1—Representative DSP coprocessor boards (continued)

Vendor	Model; when introduced; price	Processor/clock speed (MHz)/ number of processors	Bus/DMA?/ mapping	Mezzanine bus/width (bits)/speed (bytes per sec)	Memory (bytes) for program and data		I/O functions	
					Min	Max	On base board	With mezzanine card(s)
Sonitech International Inc	Spirit-30 SBus; 5/91; \$3995 to \$8995	TMS320C30/33/1	Sbus (1 slot)/NS memory	Parallel I/O expansion/32 data, 4 address/32M	256k-S	2M-S	2 μ P serial ports, 1 μ P parallel port	NA
	Spirit-30 VME; 5/91; \$4995 to \$9995	Same as board above	VME 6U master or slave/NS/NS	Same as board above	256k-S	16M-D 1M-S	Same as board above	NA
	Spirit-40 AT; 5/91; \$8995	TMS320C40/40/2	ISA-16/yes/ I/O	NA	1M-S ¹⁵	4M-S	5 8-bit 2-way communication ports. See comments	NA
Spectral Innovations	MacDSP II; 4/91; \$7995	DSP32C/50/2 68000/10/1	NuBus/yes/ 68000; memory; DSP320 I/O	NA	2M-D 2M-S 8k bytes dual-ported SRAM	2M-D 2M-D	2 16-bit ADCs and DACs, 250k samples per sec	NA
Spectrum Signal Processing Inc and Loughborough Sound Images	VASP; 3-board set; Q2/91; \$45,285 to \$110,515	DSP96002/27/5	VME/yes/ memory	Signal Bus/ 64/100M	640k-N ¹⁶ 1.485M-S	160M-D (dual-ported) on 5 memory expansion boards	Can use data-acquisition boards in other VME slots	NA
	Media-Link Series; 5/91; From \$3500	TMS320C31/33/1 i386/DX/25/1; 80387 or Weitek coprocessor (optional)	ISA-16/ NS/NS	DSP-Link/ 16/10M Media-Link/ 26/66M	For DSP: 256k For i386: 2M	2M 8M	Accesses standard IBM PC peripherals	NA
	TMS320C50 System Board; 2/91; \$2495 to \$3495	TMS320C50/40/1	ISA-16/NS memory and I/O	DSP-Link/16/ 13.32M	8k-S	256k-S	2 16-bit 200k samples per sec ADCs, DACs 2 7.2M bps serial ports	2 16-bit 50k samples per sec sigma-delta ADCs
	ADSP-21020 Board; 5/91; \$5995	ADSP-21020/20/1	ISA-16/NS I/O	DSP-Link/16/ 10M	0	3.84M-S	2 16-bit 200k-samples per sec ADCs, DACs	See board above
Star Technologies	AP-120; 11/89; \$20,000	TMS320C30/32/4	VME 9U by 400 mm/ master/ slave VME interface	NA	1.25M-S	1.5M-S	Synchronous interface 64M bytes per sec	NA
Street Electronics	Echo DSP; 10/91; \$175	ADSP-2105/40/1	ISA-16/no/ I/O	NA	16k	64k	1 8-bit ADC (48k samples per sec), 2 16-bit DACs (48k samples per sec)	NA
Texas Instruments	TMS320C40 PPDS; 8/91; \$19,000	TMS320C40/50/4	Uses ISA-bus half-card controller or SCSI port	Global bus/32/ 100M 8 communication ports/serial/20M	18k-R ¹⁷ 512 (cache)	1.5M with mezzanine board	Global bus and ports described at left at left	NA
Zola Technologies	Dual DSP Audio Card; Q3/91; \$2500 to \$5995	DSP56001/32/2	NuBus/NS/ all data memory mapped to bus	NA	120k	120k	NA	NA

Notes:

1. NS=Not specified.
2. '-D' after number of bytes denotes dynamic random-access memory (DRAM).
3. '-S' after number of bytes denotes static random-access memory (SRAM).
4. NA=Not applicable.
5. VGA=IBM Video Graphics Array display standard.
6. Also performs block floating-point operations.
7. The DT-Connect standard originated with Data Translation Inc.
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9. The so-called '6U' VME board is the most common VMEbus board size.
10. Although the boards are available only with daughter cards, the vendor does not describe the interface between the main card and the daughter cards as a mezzanine bus.
11. I/O daughter cards mount to Tiger 40 board but cause the board to use two bus slots.
12. '-E' after number of bytes denotes electrically programmable read-only memory (EPROM).
13. In the \$5995 version, the UT69532 operates at 15 MHz and performs 75M floating-point operations per sec (FLOPS).

DSP coprocessor boards

Supporting software (and price, if not included with board)	Comments
Runtime and DSP libraries included, development systems	Architecture is same as those of vendor's VME, ISA-16, and Micro-channel boards.
Same as board above	VMEbus master operation lets board transfer data from frame grabbers without host intervention.
Runtime library included, development systems	80M FLOPS. Communication ports, each with its own DMA control, let you set up μ P arrays of your choice (tree, ring, cube, etc).
Signal analysis, \$495; array processor library, \$495; assembler/simulator, \$500; DSP library, \$100; C compiler, \$1500	Supports Apple Real-time Operating System Executive (A/ROSE), which provides pre-emptive multitasking and round-robin task scheduling with 110- μ sec context switching. DSP- μ Ps communicate via dual-ported SRAM.
Assembler/linkers, C compilers for IBM PCs and Sun stations, \$495 to \$3900	Three board types: general signal processing, I/O, and 2-port memory. Maximum price includes 5 fully loaded memory boards. Typical configuration processes 2.2G FLOPS peak.
Symbolic monitor/debugger, assembler/linker, C compiler, simulator, Spox OS	Unit is both a DSP board and a complete i386-based PC system board for passive-backplane systems.
Monitor/debuggers, high-level language interface library, assembler, \$500; C compiler, \$2500; simulator, \$2000	Board has 55-square-cm prototype area.
See board above, Spox OS (Price NS)	Has 2 memory expansion connectors. Allows 80M bytes of program and 24G bytes of data storage.
Assembler, linker, debugger, signal-processing library, Spox OS	
Low-bit-rate speech coding and music recording/playback software	Very low-cost board with a programmable DSP μ P, ADC, and DACs. Development software comes from the chip vendor, Analog Devices. Microphone and speakers included.
Optimizing ANSI C compiler, assembler, linker, debugger, runtime library, Spox OS drivers, simulator	Parallel debugger uses JTAG scan interface to permit development of software that runs simultaneously on a virtually unlimited number of TMS320C40s.
Assembler, linker, librarian, \$495; algorithm design and modelling package, \$895; sound recording, editing playback, \$995	Base price is for board alone. Maximum price is for board, external data-acquisition unit and software

14. MOPS=millions of operations per sec.

15. SRAM is divided equally between processors. Each processor's memory is half local and half global.

16. '-N' after number of bytes denotes nonvolatile memory.

17. '-R' after number of bytes denotes read-only memory.

ing just as quickly. As costs decline, the number of applications that become candidates for DSP techniques multiplies. You can safely say that, at present, the number of DSP applications that engineers are investigating exceeds by several orders of magnitude the number of applications with designs in commercial production.

When you expect to sell a DSP-based product in low or moderate quantities, using an OEM DSP board as a component of your product cuts hardware-development costs and lets you bring the product to market sooner than would developing unique hardware. When you are buying large quantities of boards for volume production of a DSP-based product you've already developed, the availability of development tools is no longer important. However, as long as most of the DSP boards sold go into developing new applications—the current situation—having development tools available will be a key factor in a board's success.

The abundance of tools that run on IBM PCs is a major reason for the dominance of the PCs' ISA bus as a format for DSP boards (Ref 2). As long as a significant amount of DSP work relates to audio, DSP-board vendors will continue to develop new ISA bus products. But applications that demand higher performance strain the bus's capabilities—not just its data-transfer rate but also its ability to deliver the dc power that high-performance boards use. Interestingly, among the vendors' submissions, we found little evidence of strong interest in the most obvious alternatives to the ISA bus. There were no boards for the EISA bus and only one for the IBM PS/2 Micro Channel Architecture bus.

Spectrum Signal Processing and Loughborough Sound Images have an interesting answer to many of the limitations of the ISA bus. The Medialink is a complete 25-MHz 80386DX CPU on a full-size, 16-bit ISA bus plug-in board for passive-backplane systems. Besides a '386 with as much as 8M bytes of RAM and facilities for an 80387 or Weitek numeric coprocessor, the board contains a TI TMS320C31 DSP μ P with as much as 2M bytes of its own RAM. It also contains an interface that can communicate with off-board DSP μ Ps at speeds as great as 66M bytes/sec.

Placing the DSP chip and the '386 on the same board considerably speeds up interprocessor communication. This architecture is very likely a precursor of things to come. Workstations from Next Computers Inc already include a DSP chip on their system boards. That chip performs a variety of functions, among them most of those of a modem. Spectrum and Loughborough are not alone in envisioning the not-too-far-distant day

Manufacturers of DSP coprocessor boards

For more information on DSP coprocessor boards such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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DSP coprocessor boards

when the system boards of all PCs and workstations include at least one DSP μ P. The firms are hoping that Medialink will establish the standard for communicating with DSP μ Ps in computers based on 80x86 CPUs.

A move to workstations and to the VMEbus

But DSP-board vendors' interest in the VMEbus—a bus that has long been a mainstay of the workstation world—provides evidence of a different sort of change: The increasing power of DSP chips and the growing popularity of multiprocessor architectures are causing engineers to look closely at developing new DSP products on VMEbus-based workstations rather than on PCs. Not only do workstations perform important development tasks, such as compilation, faster than most PCs do, the VMEbus can accommodate larger boards that use more dc power than those that fit PCs. Also encouraging the use of workstations for DSP development is the growing availability of workstation-based DSP development tools.

But from a DSP-board standpoint, not all is rosy on the workstation front. Although several vendors have introduced boards for the Sbus of Sun Microsystems' SPARCstations, the small board format limits the units' capabilities.

All the evidence points to a continuation—even an acceleration—of the breakneck pace of change in the world of DSP boards. Fueled by increases in the power of DSP chips and reductions in the chips' cost, potential new applications will mushroom. With the explosion in applications will come the need for new and different boards—flexible ones for development work and low-cost ones for use in some of the DSP-based products the development work will produce. **EDN**

References

1. Gallant, John, "Plug-in DSP boards," *EDN*, April 26, 1990, pg 142.
2. Leibson, Steven H, "DSP development software," *EDN*, November 8, 1990, pg 156.

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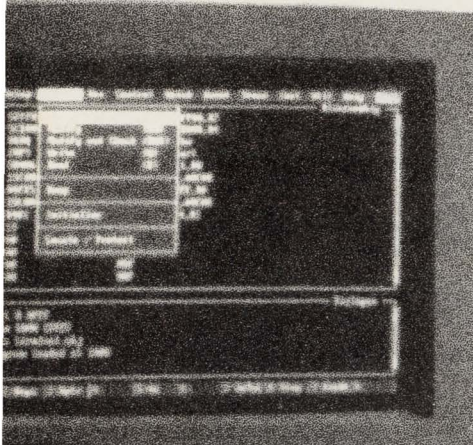
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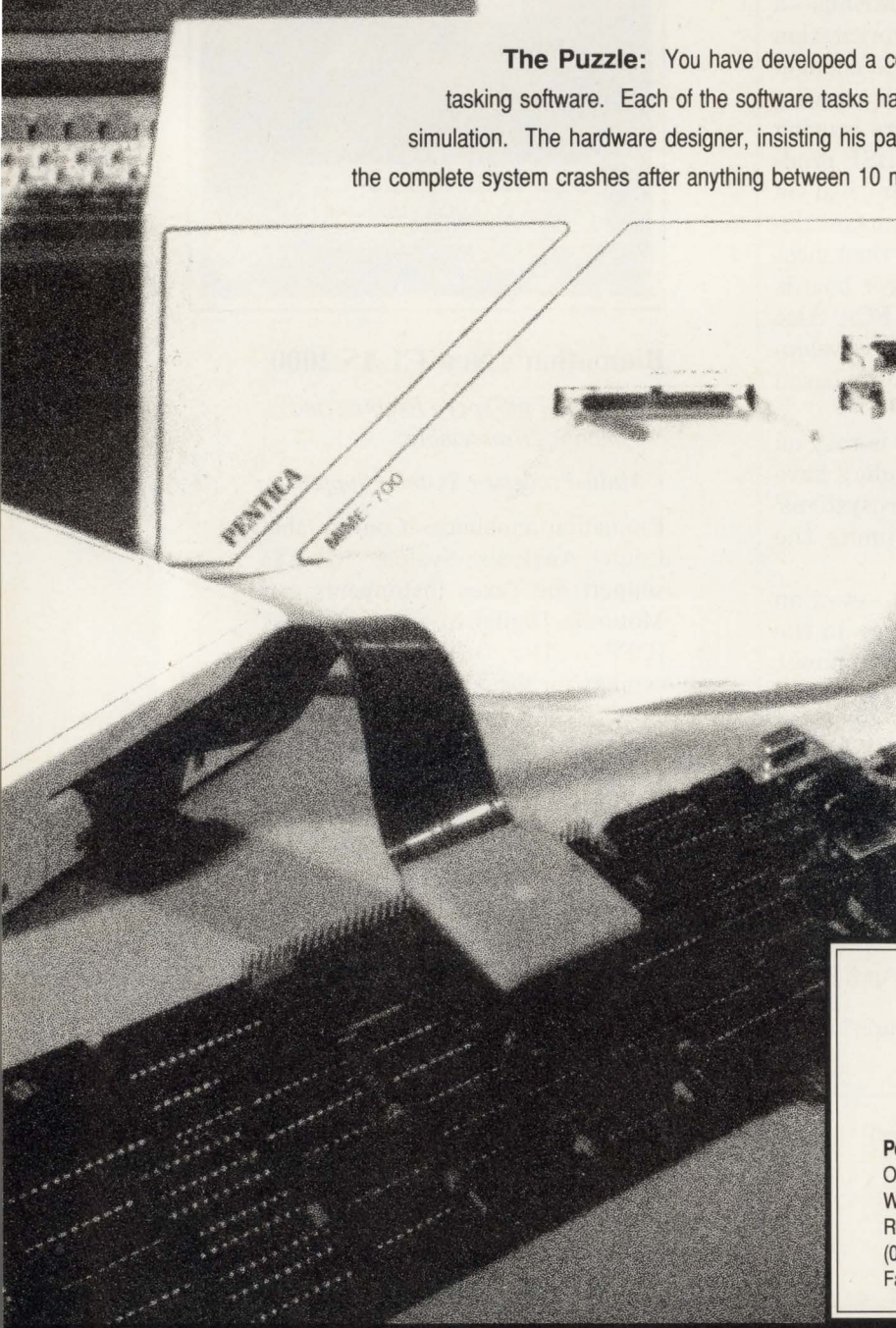


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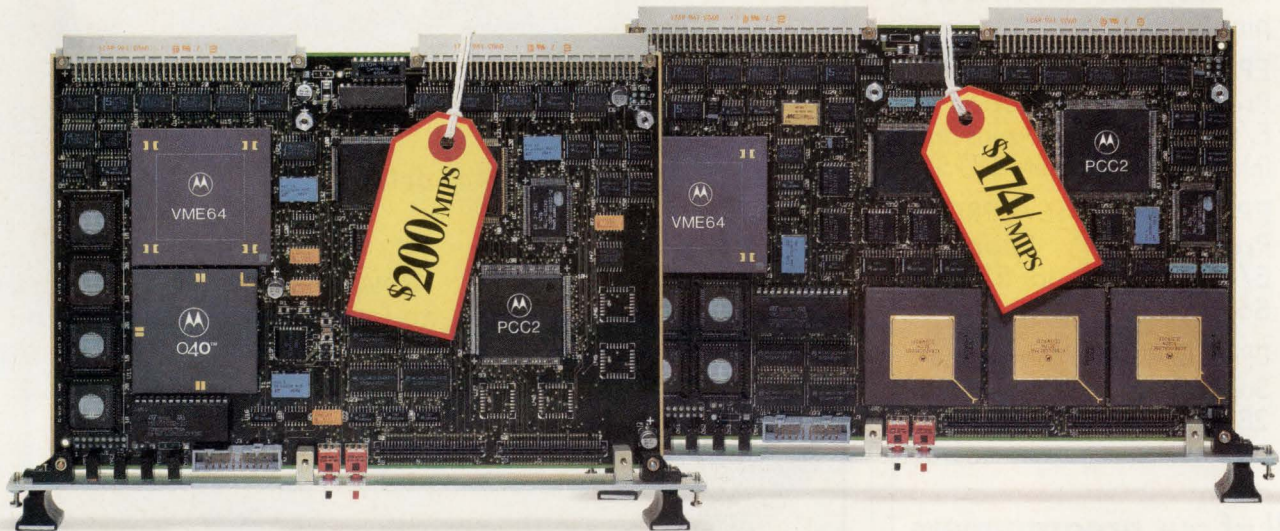
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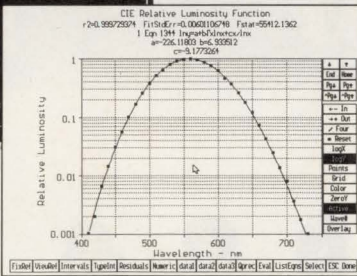
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4	54878.649683	1256	26	ln(a+b*x^c)/ln(x)
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6	54588.717658	1237	25	ln(a+b*x^c)/ln(x)
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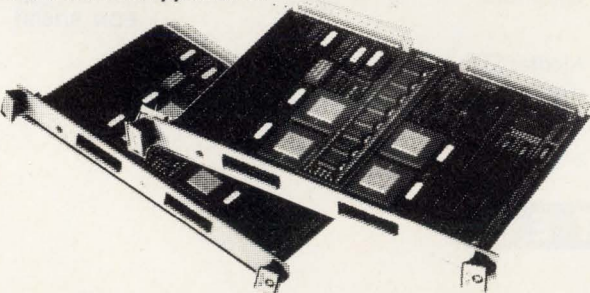
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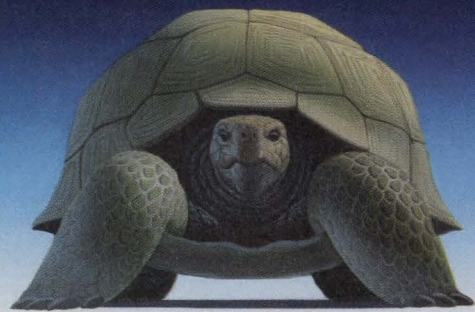
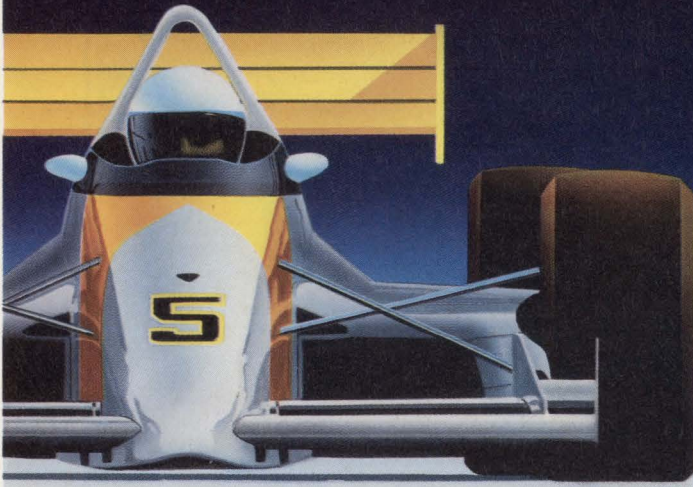
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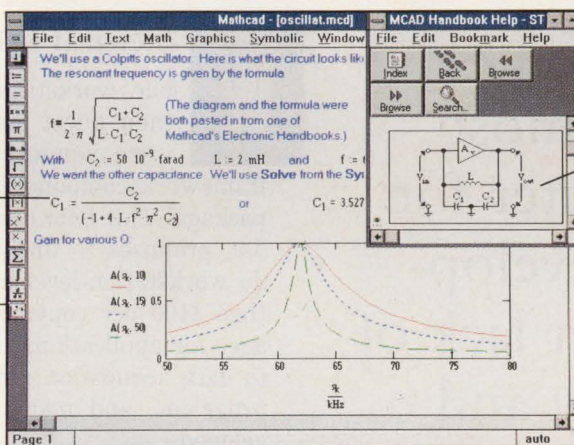
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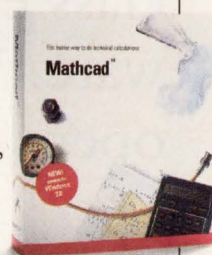
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Windows-based engineering software

■ The PC is the most popular computer for engineering development work, but lack of graphics-display and printing standards has blocked developing appropriate workstation-class engineering software. Windows 3.0 opens the flood gates.

Steven H Leibson, Executive Editor

While workstation vendors and users continue their quest for the framework grail, PC software vendors have had most of the major framework components dropped in their laps in one package. This boon, in the form of Microsoft Windows 3.0, promises to unshackle the PC's latent ability to do workstation-level engineering work and costs less than \$100 per copy. Many vendors of software packages for applications ranging from engineering design to data acquisition already offer Windows-compatible programs, and many more programs are being developed.

According to the EDN News Edition's 1991 EDA survey, the PC holds a solid lead over all other computers as an engineering development platform (Ref 1). Of the top four computer types used for electronic design automation, 80386-, 80286-, and 80486-based PCs hold positions 1, 2, and 4, respectively. The 80486 μ P is relatively new, so you can expect PCs to hold the top three positions next year.

PCs dominate engineering

Taken as a group, PCs dominate engineering work. Even so, several factors prevent engineering-software vendors from fully exploiting the advanced PC hardware available today. One of the chief culprits has been DOS. Even version 5, the latest DOS incarnation, offers little support for graphics and suffers from a relative lack of memory. Programs running under DOS 5 are still limited to 640 kbytes of RAM. Consequently, PCs with many megabytes of RAM and high-performance, high-resolution displays need individual treatment from engineering-software vendors. Each machine is a special case.

DOS program developers either ignore high-performance PCs by writing code for the lowest common denominator or create and support numerous device drivers for the various PC displays, printers, and mice. These hardware-support activities can divert software

vendors' resources away from making improvements to the engineering aspects of their products. For example, a vendor of pc-board layout tools may have to choose between adding yet another display driver or improving its automatic router.

Microsoft's Windows 3.0 solves DOS's display-driver and memory-scarcity problems, so application developers can work on the application instead of wasting time and effort on the PC's hardware needs. Windows manages the PC's display—no matter what display-adaptor card you have—and presents a unified display interface to the application software. It does the same for printers and mice. Further, Windows frees application programs from DOS's 640-kbyte barrier. In fact, engineering-software vendors cite these features as the main reasons for adopting Windows 3.0. **Table 1** lists a healthy sample of Windows-based engineering software already on the market. Many more such products are on the way.

Some stalwart hold-outs (both users and vendors) have put off the switch to Windows claiming that graphical user interfaces (GUIs) are for sissies and that DOS-based applications run faster. In truth, Windows does ask more from the PC, and lower-performance machines will bog down to the point where they're unusable.

However, PCs based on 80386 and 80486 μ Ps—the type most often used for scientific and engineering applications—have little trouble running Windows. PC hardware advances, which seem to occur on a daily basis, make Windows' performance less of a problem as time passes.

In effect, Windows 3.0 uncouples PC hardware and software. If a PC-hardware vendor develops a faster display adapter or builds a higher-resolution display,

Windows can adapt without requiring changes in the application software. The only new software you'll need is a Windows display driver, and the display vendor—the appropriate party—becomes responsible for developing that code. The same fortuitous situation exists for printer manufacturers. Software vendors cite this

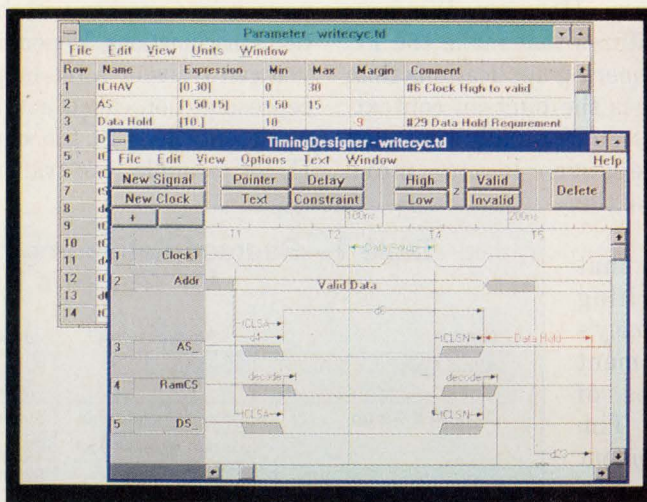
feature, above all others, as the main reason for switching to writing Windows applications.

The second most popular reason for switching is Windows' ability to make more than 640 kbytes of memory available to an application program. Some programs, such as Deutsch Research's Spicewindows Professional, simply cannot run in 640 kbytes. Prior to Windows, the only remedy for this lack of memory was third-party DOS extenders, which have several drawbacks: They're not standardized, they cost the vendor and the user extra money for each application program, and they can cause compatibility problems for other DOS programs.

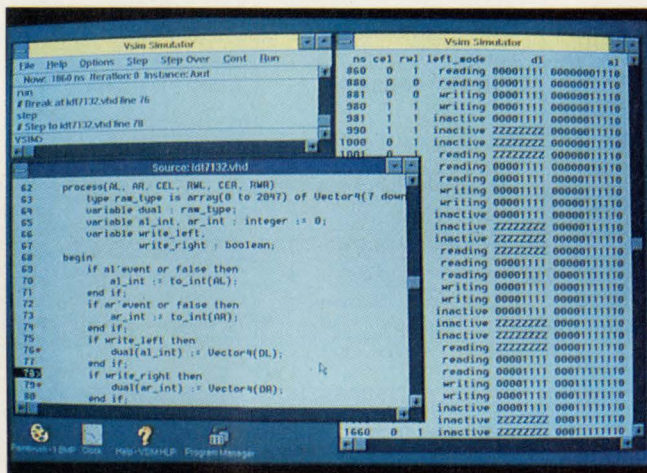
Windows lets application programs use more memory than the PC has RAM by implementing a simulated form of virtual memory that spools parts of programs to disk when the PC runs out of RAM. But unlike true virtual-memory systems such as Unix, Windows requires the software developer's cooperation to pull this trick off successfully.

Similarly, Windows provides a form of multitasking called "cooperative multitasking" that also works only if the application code cooperates. (For more information about developing Windows-based applications, see **box**, "Hints from veteran Windows application developers.")

Even if graphics standards and memory management were all that Windows offered, many engineering-software vendors would still adopt the GUI because



Many engineering tasks formerly done by hand, such as creating and analyzing timing diagrams, translate quite well to the Windows graphics environment. Timing Designer from Chronology not only lets you draw timing diagrams, it calculates timing margins from the data you enter to ensure that your design meets setup- and hold-time requirements.



Even text-oriented applications benefit from the Windows environment. Model Technology's V-System/Windows creates a total development environment by displaying your VHDL source code in one window, simulation control in a second window, and the VHDL simulator's results in a third window.

“Windows has got to be the future of ECAD on the PC.”—*Jeff Deutsch, president, Deutsch Research*

of its popularity with PC users. However, Windows now has several additional features that make the PC a far better candidate for engineering applications than ever before. One such feature is the built-in, context-sensitive help system. This system is rapidly replacing paper user manuals because it is more convenient to use and serves the user better than a book.

Altera is one vendor that cites this advantage to writing Windows programs. The company's Max+Plus II PLD development system includes 3 Mbytes of on-line help information. Tim Southgate, software development manager at Altera, says that context-sensitive help isn't a radical idea for Windows applications, but it is radical for CAD tools. Altera's help system lets you click on a displayed object and immediately find out what it does and how to use it.

Mathsoft used Windows' help system in its Mathcad technical computation package and was even able to extend the concept. Using the Windows help system, the company created electronic handbooks that let you cut standard formulas from the handbook and paste them into your Mathcad document. These formulas are not just text representations, they're "live." You can feed constants and variables to them, and they'll compute results.

Mathsoft's use of the help system demonstrates Windows' ability to link the operation of different applications. Software developers can use these intertask communications channels to pass information between applications programs. In addition to the help system, Windows provides for intertask communications through three other means: the Windows clipboard, a facility called dynamic data exchange (DDE), and shared memory in dynamic link libraries (DLLs).

The Windows clipboard lets you cut an object from one window and

paste it into another with blissful disregard of the operation's machinations. Depending on the application program, you can transfer a bit map, a block of text, a scalable representation called a Windows metafile, or all three representations to the clipboard. Altera's Max+Plus II, for example, can transfer all three object types.

Table 1—Representative engineering software for Windows 3.0

Vendor	Product name	Product description or use	Price
Altera Corp	Max+Plus II	PLD development system	\$9995
CAD/CAM Group	Design Capture Tool	Schematic entry	\$995 to \$2495
	Design Analysis Tool	Design verification	\$495 to \$995
	Waveform Tool	Simulation interface	\$695 to \$1995
Chronology Corp	Timing Designer	Timing-diagram entry	\$995 ¹
Data Translation	Global Lab Image	Image analysis	\$2495
Dazix	Ace+ PC Entry	Schematic entry	\$3500
Design Systems sA	DS-Carte	Pc-board layout	Fr 6000
	DS-Logic	Schematic entry	Fr 8000
	Start-CAD	Schematic entry and pc-board layout	Fr 4900
Deutsch Research	Spicewindows Professional	Analog simulation	\$2295
Dolphin Integration	Smash	Mixed analog and digital simulation	\$3950 to \$4950
	Interactive Curve Display	Visual analysis of Spice output files	\$295
Foresight Resources Corp	Drafix Windows CAD	Mechanical CAD	\$695
Geotest Inc	ATEasy	Autoamted testing	\$2995
Hewlett-Packard Co	HP 4990A Probeview	LAN-protocol analysis	\$5000
Hyperception Inc	Hypersignal-Windows	DSP design	\$795 to \$2995
Laboratory Technologies Corp	Labtech Notebook for Windows	Laboratory data acquisition	\$1495
Mark V Systems Ltd	Objectmaker	CASE for Ada, C, and C++	\$8000
MathSoft Inc	Mathcad	Mathematical analysis	\$495
Microsim Corp	Schematics	Schematic entry	\$1250 ²
Microsoft Corp	Microsoft Project for Windows	Project Management	\$695
Model Technology Inc	V-System/Windows	VHDL development system	\$1495
NCI	PA480/485	25/50-MHz, 48-channel logic analyzer	\$1200 to \$1400
Popkin Software & Systems Inc	System Architect	CASE	\$1395 to \$1595
Quicklogic	pASIC Toolkit	FPGA development system	\$3995
Scientific Software Tools Inc	Driverlinx	Data-acquisition software drivers	\$400
Simucad Inc	Silos III	Logic and fault simulation	\$1200
Symantec Corp	On Target	Project management	\$399

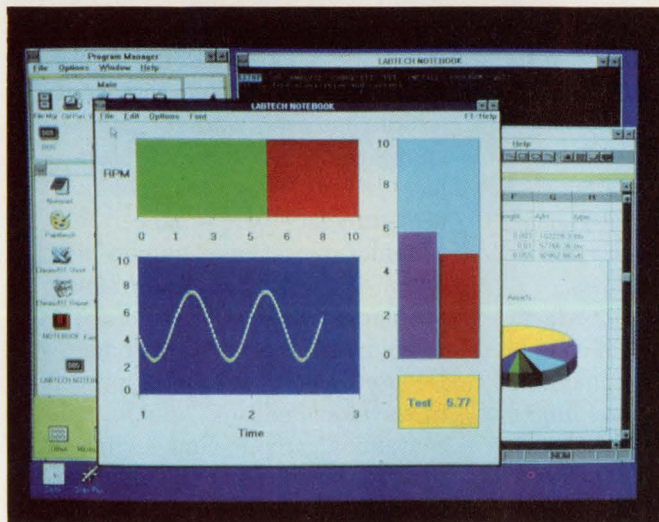
Notes:

1. The price of Chronology's Timing Designer software changes to \$1495 on October 1, 1991.
2. The price of Microsim's Schematics software package changes to \$1750 on October 1, 1991.

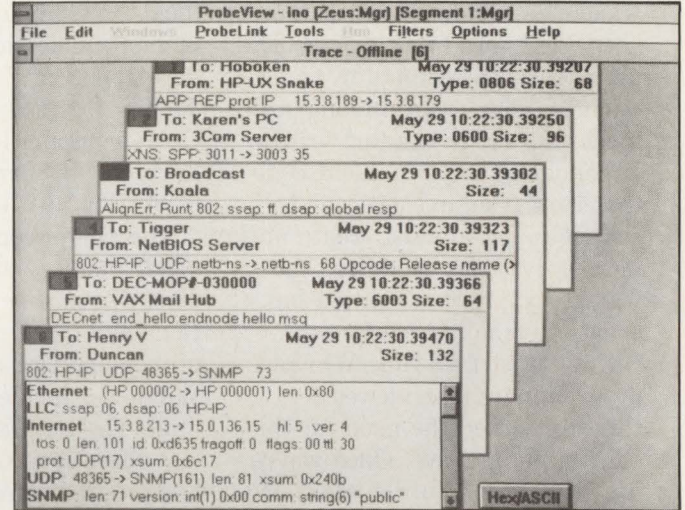
At times, you may want information to move from one application to another without manual intervention. Hyperception's Hypersignal-Windows package illustrates the advantages of this transfer mode. You can set up a simulated system in the product's block-diagram editor and, through DDE, send signals generated by the simulation to a graphical-analysis package for scrutiny. There are other ways to send data from one program to another, but the DDE facility provides a standardized method for performing this function. Jim Zachman, Hyperception's president, says that DDE will enable software developers and engineers to solve new types of problems.

Quicklogic also uses DDE to carry information between concurrently running programs in its pASIC Toolkit. The PLD compiler and the schematic editor are independent programs that run concurrently, and the two programs need to communicate. The editor sends netlists to the compiler, and the compiler sends back-annotation information to the editor. If an error occurs during compilation, you can click on the error message in the compilation window, and the offending node will be highlighted in the schematic window. Messages to perform these feats flow through the Windows DDE pipeline.

However, DDE doesn't solve all intertask communications problems. DDE creates a conduit between concurrently running application programs, but it doesn't define the format of the information that flows through that conduit. Application-program developers must agree on the data format before DDE can become use-



You can perform data acquisition and analysis simultaneously under Windows. Laboratory Technologies' Labtech Notebook for Windows can capture data while a spreadsheet analyzes and presents results.



Instruments can also exploit multiple windows to present information more logically. Hewlett-Packard's Probeview puts each network information packet in its own window for easier analysis.

ful. For programs written by the same vendor, the data-format problem doesn't present much of an obstacle. But until engineering-software vendors band together to create some DDE communications standards, you should not expect Windows programs "with DDE support" to work together unless the vendors explicitly state that the programs can communicate with each other.

Microsoft set a de facto DDE standard for business software with its \$495 Excel spreadsheet. Most business applications that "support DDE" actually conform to the Excel protocol. That standard doesn't serve the engineering community's needs well because it concerns itself with only business-type information. Microsoft is in the early stages of developing a higher-level messaging specification called object linking and embedding (OLE), which may move the industry towards a more comprehensive communications protocol.

Bridging the communications gap

Like DDE, Windows DLLs can also ease the burden of communications between different programs. Quicklogic employs DLLs to translate information passed between the program components of its pASIC Toolkit. Rather than reinvent schematic entry, Quicklogic's tool employs the CAD/CAM Group's Schematic Capture Tool for the graphic design of PLDs. Quicklogic's Toolkit generates a netlist from the completed schematic. CAD/CAM's product didn't use the netlist format Quicklogic wanted to use, so Quicklogic linked a

Text continued on pg 136

Hints from veteran Windows application developers

If you haven't written code for a graphical user interface (GUI) before, Windows will probably throw you a few curves. Unlike conventional programming, in which the computer drives the user, GUIs are event driven: The user drives the computer. Consequently, your programming style must change. Instead of writing a monolithic piece of linear code that runs from initialization to completion, you must create numerous program modules that wait for appropriate activating events to transpire before executing. Most first-time Windows programmers interviewed for this story cited the need for this shift in perspective. Once you're over this initial hurdle, most programmers say that writing code for Windows is no different from writing other types of programs.

You will have to learn about Windows' idiosyncrasies, however. For example, C programmers are accustomed to using C's *malloc* function to allocate memory and to obtain a pointer to that memory from the operating system. They then use *free* to dispose of that memory. Under Windows, you cannot use *malloc* and *free* because Windows simulates a virtual memory system. Thus, Windows doesn't hand out absolute memory addresses unless you really need to use that memory.

Name that memory block

To allocate a block of memory, you must first use a Windows function call to get a memory-block "handle," or name. When you want to use that memory, you use a second call to lock the block of memory and obtain a pointer to the locked memory block. Your program should keep the memory pointer only for as long as it plans to actively use the memory. When the program no longer needs that memory, you should free the memory block

for other applications' use.

Alternatives to Windows memory-allocation techniques can make programming a lot easier. Chronology found one way to reduce the complexity of Windows memory allocation. The company developed its Windows product, Timing Designer, using a \$400 C++ compiler for Windows from Zortech (Woburn, MA, (617) 937-0696, FAX (617) 937-0793).

The C++ compiler's *new* and *delete* memory-allocation calls replace C's *malloc* and *free* functions and mask the complexities of memory management under Windows. Incidentally, Windows limits the total number of memory allocations to 8000 for all active programs. Windows programmers soon learn to independently suballocate 32-kbyte memory blocks within their programs.

Several veteran developers note that C compilers for Windows have a tough time with large programs. Altera's Tim Southgate and Deutsch Research's Jeff Deutsch both say they used compilers running under OS/2 because Windows compilers simply could not accommodate the multimegabyte size of their programs. Deutsch cites the 32-bit addressing capabilities of OS/2 compilers as a real benefit for developing large Windows applications. As an alternative to running compilers under OS/2, Model Technology employed Oxygen, a \$99 package from Rational Systems Inc (Natick, MA, (508) 653-6006, FAX (508) 655-2753). Oxygen lets you run OS/2 compilers under Windows.

The Windows user interface also adds a great deal of complexity to your code. "You may need as many as 300 Windows function calls to open a dialog box," says Bill Falk, Quicklogic's interface specialist. Falk overcame the complexity of the Windows user-interface model by adopting XVT

(Extensible Virtual Toolkit), a \$795 Windows-development product from XVT Software Inc (Boulder, CO, (303) 443-4223, FAX (303) 443-0969). XVT lets you create a dialog box with one call. The package handles both display and printing functions.

Writing code for XVT instead of Windows not only reduces complexity, it makes your program portable. XVT Software offers compatible versions of the product for the Apple Macintosh operating system, OS/2 on the PC, and Unix systems running the X Window system. In fact, the IEEE's P1201.1 standards committee has selected the XVT product specification as the base document from which it will draft a standard application programming interface for portable GUI applications. (This move neatly sidesteps the Motif-vs-Open Look GUI debate that has been raging in the Unix community for almost two years.) Falk says XVT lets you make 90% of your code portable across the four operating environments. According to Falk's tests, you pay a 2% performance penalty for this flexibility.

Windows' display performance is an issue you must deal with. Chronology experimented with rubber-band animation for waveform editing in Timing Designer but found Windows' display performance sluggish in that mode. (Note that even workstations running the X Window system have trouble providing speedy user-interface performance. Fast graphics operation seems to be one of the toughest performance problems for any GUI to crack.) The current version of Timing Designer uses a simpler approach to waveform editing, but the code contains a compile-time switch to restore the rubber-band visual effect when PC display performance improves.

Snappy performance is merely

nice for user responsiveness, but real-time products that run under Windows must execute with dispatch to perform their assignments. Because Windows employs "cooperative multitasking" instead of preemptive multitasking, any Windows application program can completely take over the PC. Should this situation arise, a real-time application program could easily find itself without enough CPU cycles to complete its tasks. A real-time application can also monopolize the PC. This situation ensures that the real-time program completes its duties, but it diminishes Windows' usefulness.

A real-time crash

Even if an application program does take over the PC, Windows doesn't allow "bare-metal programming." You cannot interact directly with the PC's hardware under Windows without crashing the system. For example, you cannot write directly to the PC's screen, and you cannot manipulate the PC's interrupt controller for your own purposes.

Real-time programs often try such maneuvers to meet hard-deadline requirements. Consequently, real-time Windows application programs may simply not be able to meet hard deadlines. Fred Putnam, president of Laboratory Technologies, notes that the initial version of his company's Labtech Notebook for Windows, a real-time data-acquisition package, can't always meet hard deadlines, although the DOS version can.

Putnam also has direct experience creating international versions of Labtech Notebook for Windows. Microsoft offers international versions of Windows 3.0 with appropriate character sets for various countries. Good Windows programming practice places all program text into re-

source files instead of embedding the text in the program modules. This technique greatly eases converting programs to other languages, says Putnam, because almost all the internationalization effort focuses on translating text in the resource file.

Even if you plan to offer only English versions of your product, you must work carefully on the program's look and feel when writing Windows application programs. Users expect Windows programs to be consistent from one application to the next. Chronology employed a graphics designer to help create Timing Designer's user interface because, as Chronology's president Lawrence E. Lewis says, most engineers and programmers lack training in contemporary visual styles or color matching.

Chronology also put together a Windows style guide for its program developers by combining published style guides for OS/2's Presentation Manager, Windows, and Apple's Macintosh. "Existing business packages set the expected operating style for all Windows programs," says Lewis. "Even if you can think of a better way to do things, you should stick with existing de facto standards because that's what Windows users expect," he adds. Lewis says that Microsoft's Excel spreadsheet for Windows sets a lot of those standards. Chronology wasn't afraid to violate this rule, however. Timing Designer's prototype trials indicated that users preferred text information in the product's tool bar instead of the icons Excel uses. Consequently, Timing Designer's tool bar contains no icons.

For early product trials, you may want to use a software prototyping tool to build a mock-up version of your product. Prototype programs incorporating just the user interface can help devel-

opers and users alike get a feel for how your product will work in the early development stages. Simucad used this approach to create a user interface for its Silos III simulator. The company employed the \$495 CASE:W package from CASEworks (Atlanta, GA, (404) 399-6236, FAX (404) 399-9516) to create the prototype interface. Simucad selected this package because it generates compilable interface code once you are satisfied with your design. You finish your program by adding the code that does the application's real computational work.

Once your application is up and running under Windows, you'll find debugging the program more difficult than debugging programs under DOS. The event-driven nature of Windows applications splits your code into relatively independent modules that you must test individually. The Windows user interface complicates testing because you can't use simple keyboard-macro programs for regression testing as you can with DOS programs. You need a program that records both mouse movements and keystrokes for Windows. None of the developers interviewed could recommend such a program.

Symantec's Dave Richards says debugging Windows applications is difficult because you can't isolate concurrently running programs. Consequently, a runaway application can kill the Windows kernel or step on some other memory location and crash the operating system. That's a tough debugging environment, indeed. In general, most of the Windows programmers interviewed for this article thought that Windows debugging tools are still somewhat immature. "Event-driven debugging is a nightmare," summarizes Quicklogic's Falk.

translation DLL it wrote to CAD/CAM's tool. One added line to the schematic-capture tool's initialization file creates this link. The DLL converts netlists in CAD/CAM's format to Quicklogic's format.

Translation is a popular use for Windows DLLs among many application developers. Symantec uses more than 30 DLLs to translate text files among word-processor file formats in its \$199 Justwrite word-processing pack-

age for Windows. The word processor loads only the DLLs it needs to satisfy a user request. Thus, using DLLs minimizes the amount of RAM the translation code consumes while retaining a broad ability to handle many file formats. Conversely, Symantec's On Target project-management package doesn't employ DLLs because Dave Richards, the engineering manager for the product, saw no inherent advantages to using DLLs.

Manufacturers of Windows-based engineering software

For more information on Windows-based engineering software packages such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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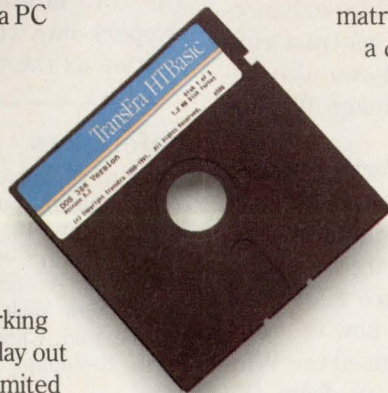
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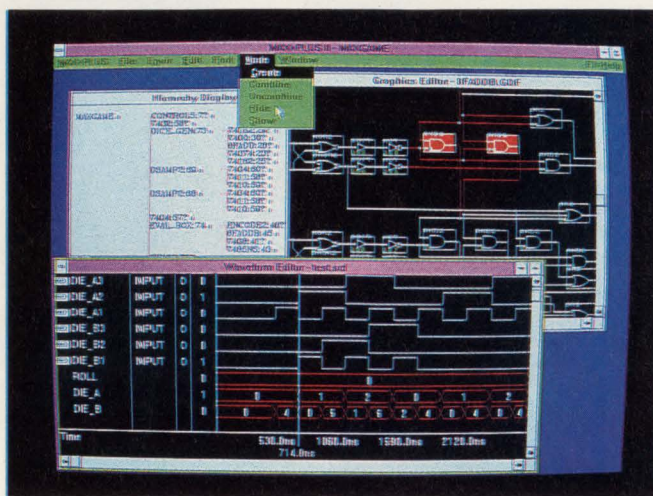
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Jeff Deutsch, president of Deutsch Research, points out that DLLs help keep the source code of his company's Spicewindows Professional analog simulation package private. Earlier versions of Spice from a variety of vendors embedded the simulation models in the program code, which made adding models quite difficult. By specifying a DLL-based model interface for its simulator, Deutsch Research permits outside model development while still keeping its proprietary application code secure.

Altera's Tim Southgate also finds DLLs useful. He says they're efficient because different programs can share one image of a DLL loaded into memory. Programs that use C runtime libraries, for example, can use this feature to greatly reduce the memory the programs consume. Also, DLLs make a program modular, which reduces the time required to link a program together during development. (Southgate notes that linking a 1.8-Mbyte program using static linking can take an hour. One-hour cycle times can really impede software development.) Altera's Max + Plus II uses more than 50 DLLs. Further, DLLs make field upgrades easy. A vendor need send out only the new or revised DLL instead of an entirely new program. This ability can significantly reduce media-distribution costs for large programs.

One aspect of Windows software engineering—software vendors don't often mention is the wealth of Windows-based business software that can cross over to serve engineers. Word processors, spreadsheets, and data-base managers all work as well in the engineering domain as they do in business. You might be surprised at the engineering abilities of some business packages. For example, Winrix is a \$495 image-creation and -editing package from Rix Softworks Inc (Irvine, CA, (714) 476-8266, FAX (714) 476-8486). The product performs several 24-bit color image-enhancement operations such as brightness and contrast control, color correction, and sharpening. It can also import and export a wide variety of PC image file formats.

You can easily move data back and forth between engineering packages and business packages through Windows' various forms of intertask communications. Quicklogic employed this Windows feature to create user manuals for its pASIC Toolkit. Bruce Kleinman, then Quicklogic's CAE tools architect and now the company's manager of customer engineering, used the Windows clipboard to transfer display screens from the company's PLD development tools directly into the document files that became the product's user manuals. Kleinman points out that engineering is far more than just design entry. "Engineers also must write docu-



Communications links between windows provide a standard way to improve a product's interactivity. When you select waveforms in the simulation window of Altera's Max + Plus II PLD development package, the corresponding nodes in the schematic representation of your design will change color to highlight the circuitry you're studying.

mentation, do analysis, and perform tests," he says. Engineering and business applications for Windows support all these tasks.

Major vendors of PC business software have either introduced Windows versions of their flagship packages or are currently developing such products. Vendors of PC-based engineering software products are following suit. Now that Windows has severed the hobbling linkage between advances in PC hardware and software, developers of both product types can devote their full energy to getting every last bit of application performance from their products. Moreover, they can survey the field and find new application problems to overcome instead of worrying about recently introduced graphics cards that now need device drivers. This turn of events will draw even more software developers into the fray and further solidify the PC's position as the top engineering computer. **EDN**

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1. Russell, John, "1991 EDA Survey: Your tools haven't changed much, but designs are more complex," *EDN News Edition*, June 13, 1991, pg S48.
2. LeBlond, Geoffrey T, William B LeBlond, and Jennifer L Palonus, *Windows 3 Power Tools*, Bantam Computer Books, New York, NY, 1991.
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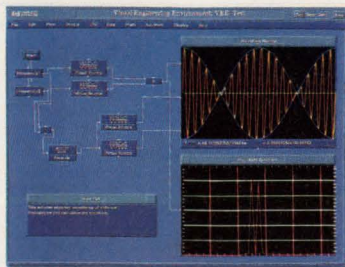
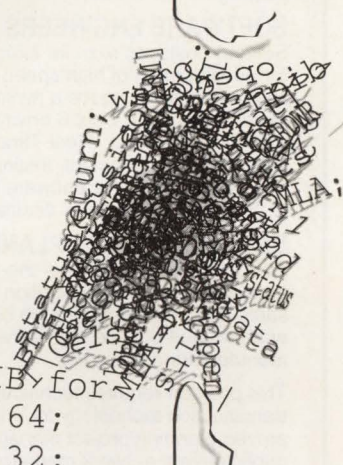
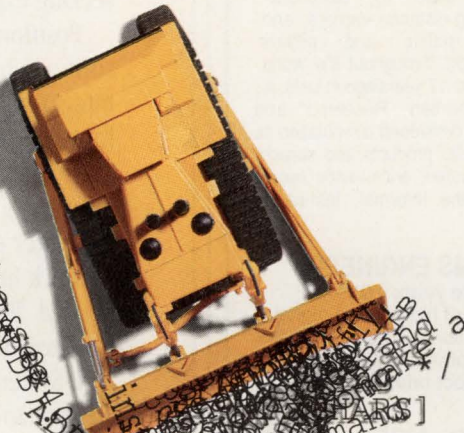
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```

void service(eid)
int eid;
{ int stat, byte;
/*serial pollinst
byte=hpib_spoll(ex
if ( (byte<0)||! (b
    printf("SRQ Probl
    return; }
stat=my_read(eid, DVM_
if (stat>0) {
    buffy[stat] = '\0';
    printf("Data from instrumen
else printf("I/O read error\n");
return; }
main() {
int busid, stat, MTA, MLA;
char command[MAXCHARS];

busid=open("/dev/hpib7", O_RDWR); /* open raw HP-IB
MTA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
MLA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
stat = BUTTON_BIT ;
sprintf(command, "KM%02o", stat); /* 2 octal digits */

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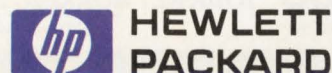
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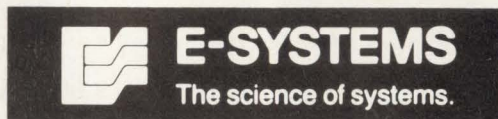
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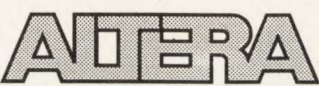
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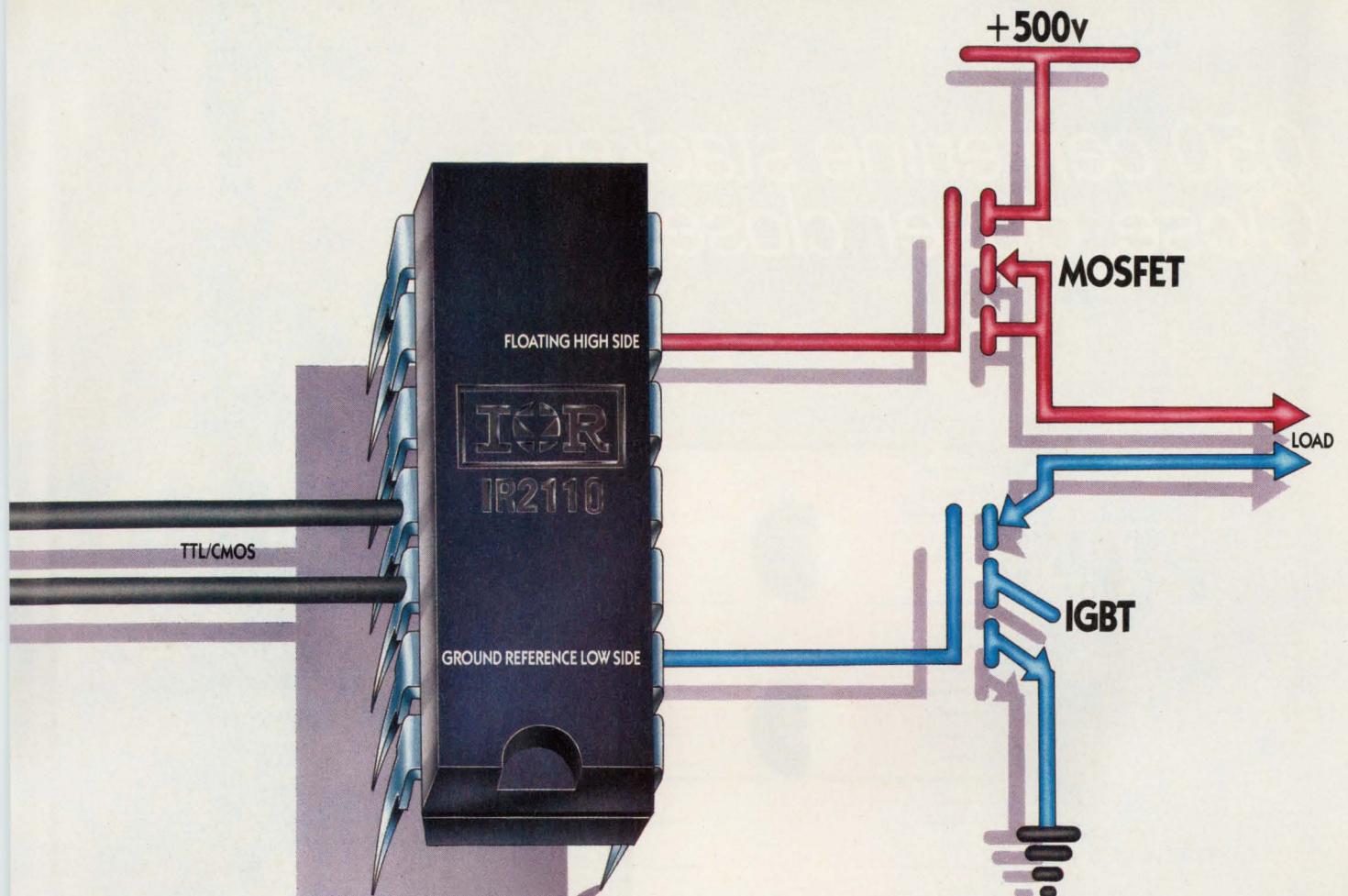
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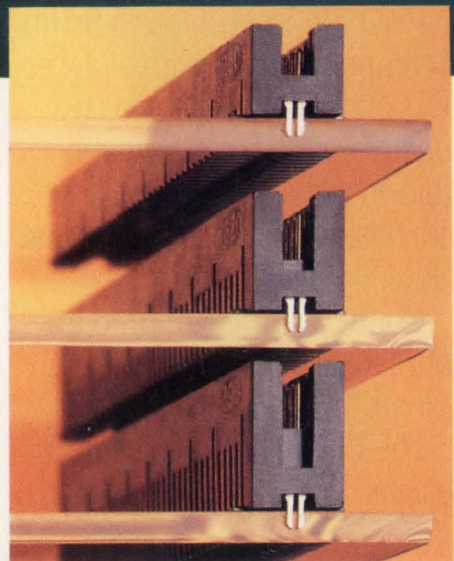
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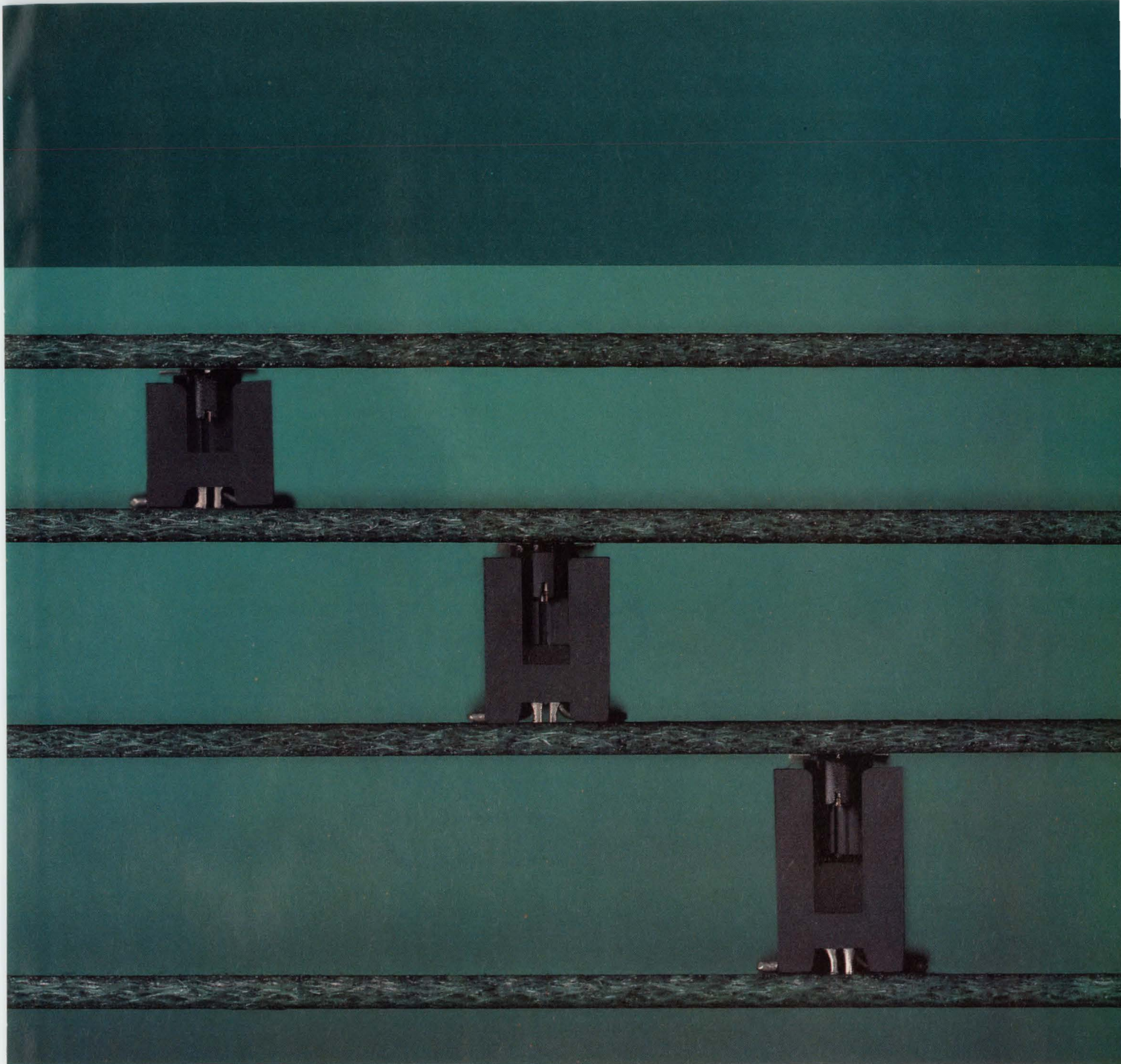
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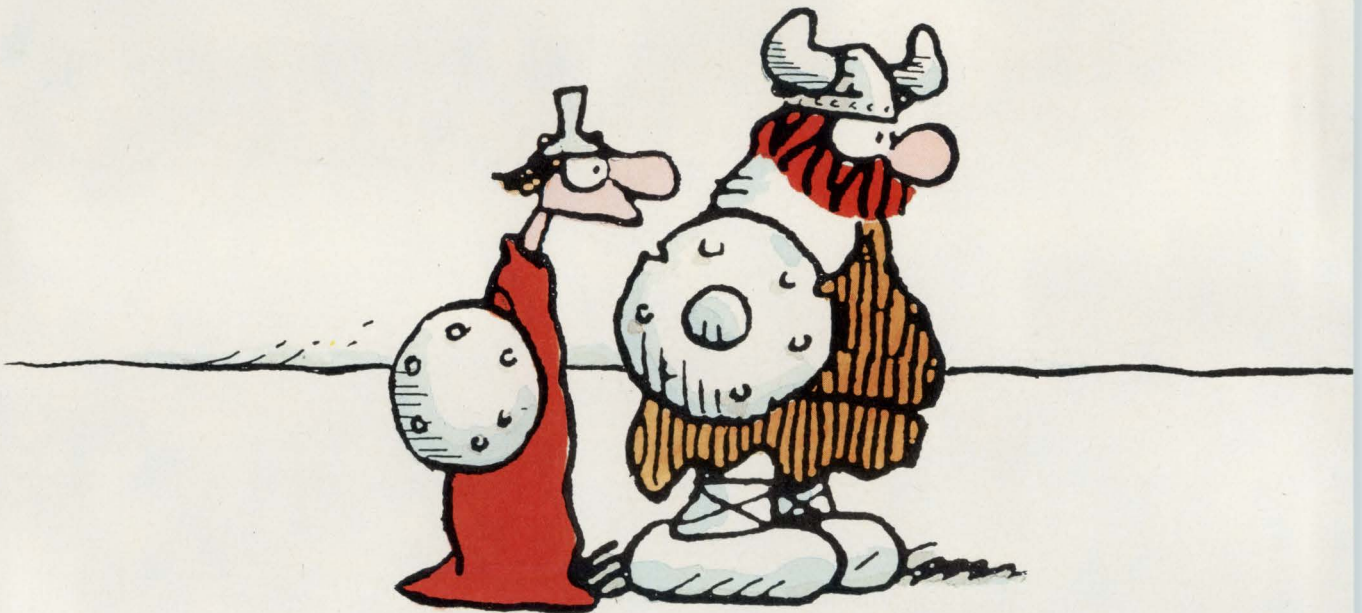
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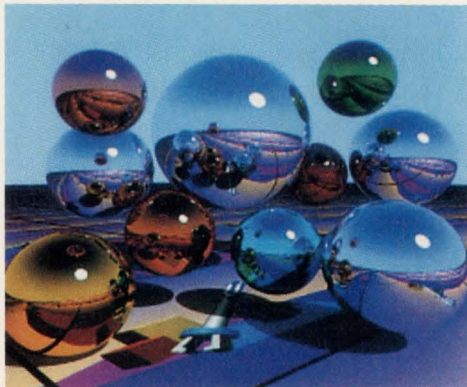
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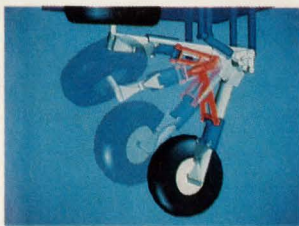
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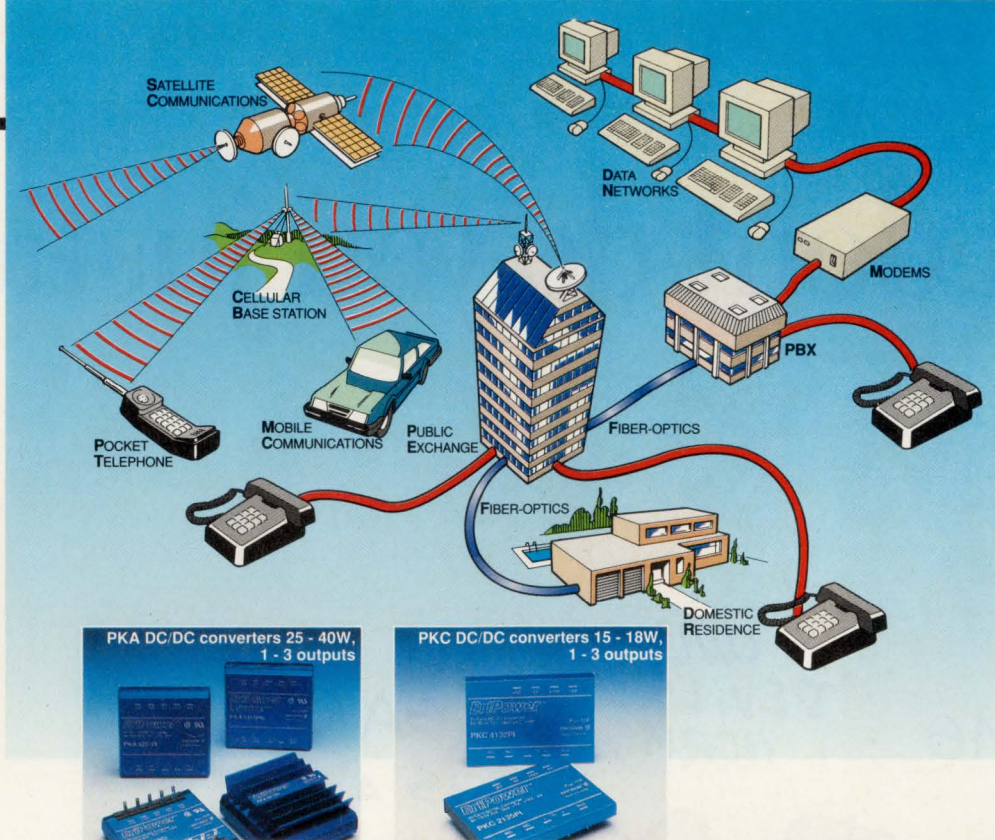
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Techniques let you write general-purpose Spice models

By incorporating flexibility into your Spice models, you'll develop a library of accurate models that you can adapt for many applications, rather than reinventing the wheel every time. An example of such a model is a universal power converter.

David Caldwell, *Consultant*

Computer simulations can save you valuable time by letting you work out the major bugs in a circuit design before building it in hardware. Unfortunately, if the device models you need aren't readily available, you may not be able to make substantial design improvements before committing to hardware. One way to increase your model library is to build models general enough so you can adapt them to a variety of applications. Such models will save you time in future simulations by eliminating the need to develop new models. Also, over time these reusable models reduce the likelihood of encountering errors.

Creating a universal power-converter model illustrates several techniques for adding flexibility to Spice models. This model simulates the buck, boost, and

buck-boost pulse-width-modulated (PWM) topologies; continuous and discontinuous conduction modes; dc operating-point, large-signal transient, and small-signal frequency-domain analyses; and positive and negative polarities. The model's versatility lets you simulate a wide variety of converters quickly and easily.

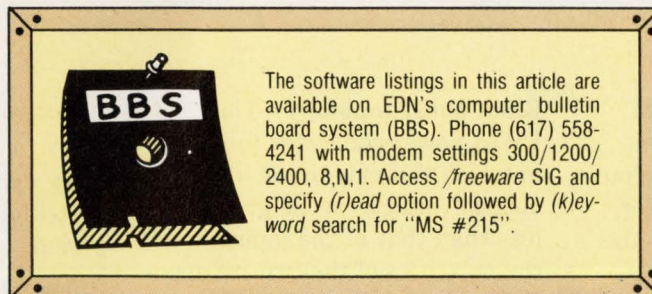
You can simulate capabilities with a flexible model that you cannot simulate with specific-case models. For example, the universal power-converter model can simulate multiquadrant converters, such as uninterruptible power supplies and power-factor-correction units. These subsystems require a versatile model because each cycle of processed power (usually 60-Hz line voltage) forces the converters to operate under a variety

of conditions. To perform a complete transient simulation, the model must automatically adjust its transfer function to handle all combinations of conduction modes and polarities.

The converter model is a simple power-transfer subcircuit with several

enhancements. You can add flexibility to other Spice models by using the same enhancement techniques. These techniques let you transform a specific subcircuit into a versatile analysis tool for a broad spectrum of applications. The techniques include

- Using time averaging to simplify switching networks
- Taking advantage of application similarities



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Writing general-purpose Spice models lets you reuse existing models rather than creating new models for every application.

- Generating external control ports
- Using diode networks to simulate if-then-else conditions
- Performing calculations via dependent sources
- Using internal feedback to realize difficult expressions.

Fig 1 shows a functional power-converter subcircuit. A dc transformer, an ideal device linear down to dc, represents the power transfer between the reference (R) and diode (D) ports and the inductor (L) and diode (D) ports. It transfers energy by translating voltage levels without power losses. By arranging the R, L, and D nodes, you can simulate the various converter topologies, so that the input current satisfies the derived equations.

The transformer has a variable turns ratio, N , which lets the simulator change the transformer's gain as a function of the external voltage at node C1. The simulator adjust the turns ratio through a high-gain feedback network until the resultant current flow from node R to node D is equal to the value the simulator calculates. The simulator performs the math using dependent sources and diode networks.

Spice has difficulty simulating switching networks directly, and calculating transient solutions is time consuming. In power converters, the corner frequency of the LC output filter is much lower than the switching frequency to minimize output-voltage ripple. To observe the response to a sudden load change, you must look at a time frame that is very long compared with the switching period, and Spice's algorithms do not handle the disparity in time constants very well.

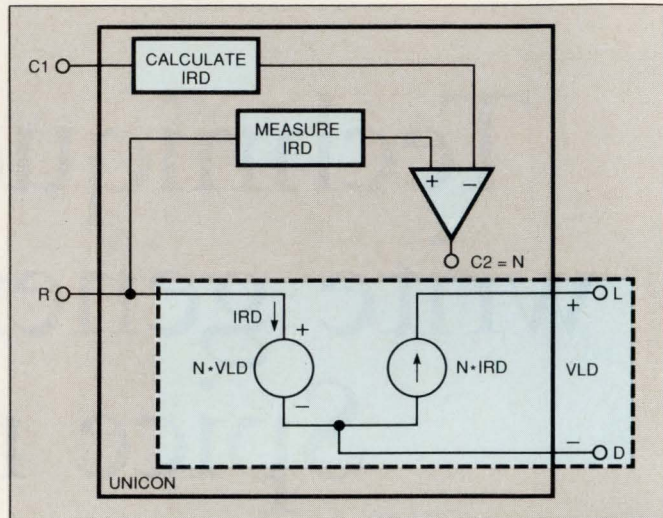


Fig 1—This functional model of a power converter includes an ideal dc transformer; four user-accessible nodes—reference (R), diode (D), inductor (L), and control (C1); and an internal control node, C2, that Spice uses to adjust the model's gain.

You can't perform ac analyses of the subcircuit because Spice generates a linear network based on a single operating point. Switches are either closed or open in the discrete-time model, and neither condition is representative of a switch's average state. You must replace the switching components with a time-averaged model to obtain meaningful results.

The time average is the peak amplitude of the switching waveform multiplied by the duty cycle. Replacing the switching waveform with the time-averaged waveform in Spice costs you the ability to

Glossary of terms

Boost topology—The PWM power-converter topology in which the magnitude of the output voltage is always greater than that of the input, and the polarities of the two are the same.

Buck topology—The PWM power-converter topology in which the magnitude of the output voltage is always less than that of the input, and the polarities of the two are the same.

Buck-boost topology—The PWM power-converter topology in which the magnitude of the output voltage can be greater or less than that of the input, and the polarities of the two are opposite, unless an isolation transformer is used.

Continuous conduction mode—The mode in which the inductor current never reaches zero.

Discontinuous conduction mode—The mode in which the in-

ductor current reaches zero every cycle.

Duty cycle—The ratio of the switch on time to the switching period.

Pulse-width modulation (PWM)—Duty-cycle variation of a fixed-frequency switching waveform.

Switch-mode power converter—A high-efficiency circuit that utilizes pulsating switches and magnetics to transform voltage levels.

see period-to-period transient responses. In return, time-averaging waveforms simplify the circuit, eliminate problems associated with simulating vastly different time constants, and provide accurate results in both the time and frequency domains. Sampling theory states that time averaging waveforms is valid at frequencies as great as half the switching frequency.

To create a time-averaged model in Spice, derive the transfer function for the switching device and generate the Spice-equivalent network to realize the equation. For an explanation of time averaging for the input current of a buck converter in both continuous and discontinuous modes, see **box**, "Determining the conduction mode."

The dashed box in **Fig 1** shows the Spice implementation of a converter power section. The subcircuit is a time-averaged model of a switch-mode power converter. **Fig 2** shows models of the three basic PWM power-converter topologies: buck, boost, and buck-boost. Note that all three models contain the same elements but in different configurations. You can derive most power-converter models from this primary set.

All three topologies operate under the same basic

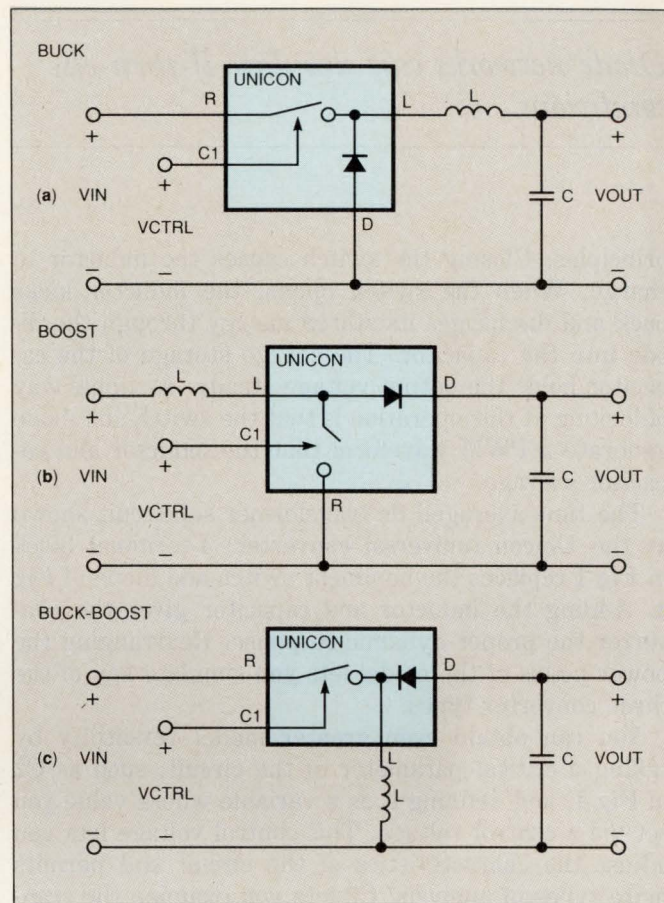


Fig 2—You can derive most power-converter models from three basic PWM power-converter topologies: buck (a), boost (b), and buck-boost (c).

Determining the conduction mode

The time-averaged value of the input current for both the discontinuous and continuous operational modes is a control parameter for the Spice power-converter model. The three topologies use the same model with rearranged nodes, so the buck-converter subcircuit (**Fig 2a** in the main text) can illustrate the analysis for all three.

In discontinuous-mode operation, the inductor discharges completely during every cycle. During each cycle the inductor current is zero at some point, and neither the switch nor the diode conducts. The switch pulse width causes the magnitude of the average inductor current to vary and is unaffected by previous cycles. You can characterize discontinuous-mode converters as PWM-

controlled current sources because their output voltage is load-dependent.

In continuous-mode operation, the inductor discharges partially every cycle, so either the switch or the diode is always conducting. The output voltage must adjust to balance the volt-second product across the inductor at any given duty cycle. The average inductor current will automatically vary over a number of cycles until it satisfies the load at the resultant output voltage. Because the output voltage of continuous-mode converters is not load-dependent, these converters are modeled as PWM-controlled voltage sources.

A converter regulated to a constant output voltage operates in discontinuous mode at light loads

and approaches continuous mode as the load draws more output current. If a simulator solves the current equations for both modes of operation, the value of greater magnitude is the correct one. When the calculated discontinuous current is greater than the calculated continuous current, the load is not heavy enough to push the converter to continuous-mode operation. Therefore, the discontinuous-current value is correct, and you can ignore the continuous-current value.

You can confirm the validity of the conduction-mode equations you derive by comparing these equations to the equations in well-established and proven references, such as **Refs 1 and 2**.

Diode networks can simulate if-then-else conditions.

principles. Closing the switch causes the inductor to charge. When the switch opens, the inductor kicks back and discharges its stored energy through the diode into the capacitor. The charge storage of the capacitor holds the output voltage steady. A simple way of looking at this operation is that the switch and diode generate a PWM waveform that the inductor and capacitor average.

The time-averaged dc transformer subcircuit shown as the Unicon (universal converter) 4-terminal block in **Fig 1** replaces the nonlinear switch and diode of **Fig 2**. Adding the inductor and capacitor gives the converter the proper dynamic response. Rearranging the power nodes of the model lets you simulate any of the three converter types.

You can obtain even greater model versatility by taking a critical parameter of the circuit, such as C2 in **Fig 1**, and defining it as a variable whose value you set via a control voltage. This control voltage lets you adjust the characteristics of the circuit and permits more types of analysis. C2 lets you examine the transient response to a control-voltage step in the time domain and measure gain and phase as a function of the control voltage in the frequency domain.

The power-converter model has two control nodes. C1 is a user-accessible node that selects the duty cycle

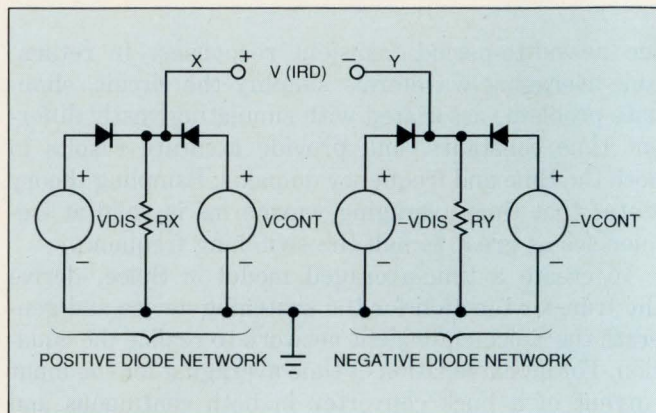


Fig 3—This Spice model contains both a positive and a negative diode network, which together accurately model continuous and discontinuous conduction.

of the simulated switch. Internal control node C2 selects the turns ratio of the dc transformer, which simulates the average voltage across the switch and diode. The internal control node is necessary because the selected duty cycle cannot directly set the transformer's turns ratio. The relationship between the duty cycle and the turns ratio is different for the discontinuous and continuous conduction modes, so the simulator must mathematically manipulate the model to deter-

Spice convergence

The biggest drawback of flexible Spice models is that they tend to be more complicated than single-application models. Therefore, you may encounter more difficulties in the convergence of the computer algorithms. The universal converter model used with Intusoft's (San Pedro, CA, (213) 833-0710) IsSpice PC simulation package has successfully analyzed many power supplies. But expecting to never encounter convergence problems is unrealistic.

If convergence problems do arise, the .NODESET command lets you estimate any node voltage and allow the Spice algorithm to use that voltage for the first iteration of its computation. Setting the expected output voltage and duty cycle of the power con-

verter increases the probability of convergence if your initial simulations fail to converge.

You can also aid convergence by using the .OPTIONS command to modify parameters. You can instruct the simulator to increase the number of iterations it can take to find a solution by changing the values of ITL1 and ITL2. You can increase the error tolerance of the program by altering RELTOL (relative tolerance) and ABSTOL (absolute tolerance).

A less sophisticated approach to obtaining convergence is to alter the topology of the circuit without changing the circuit's function. The power-converter subcircuit of **Fig 4** and **Listing 1** of the main text is the result of

some experimentation. There are several other ways to realize the same transfer function, but the one shown has the best convergence.

One alternate way to arrange the circuit is to switch the voltage and current sources of the dc transformer. Another way to realize the circuit is by setting the input current of the converter with a current source and varying the output voltage until the output power is equal to the input power. Because altering the circuit may be time consuming, you should only attempt such modifications after trying the .NODESET and .OPTIONS commands. **Ref 3** discusses more methods to aid Spice convergence.

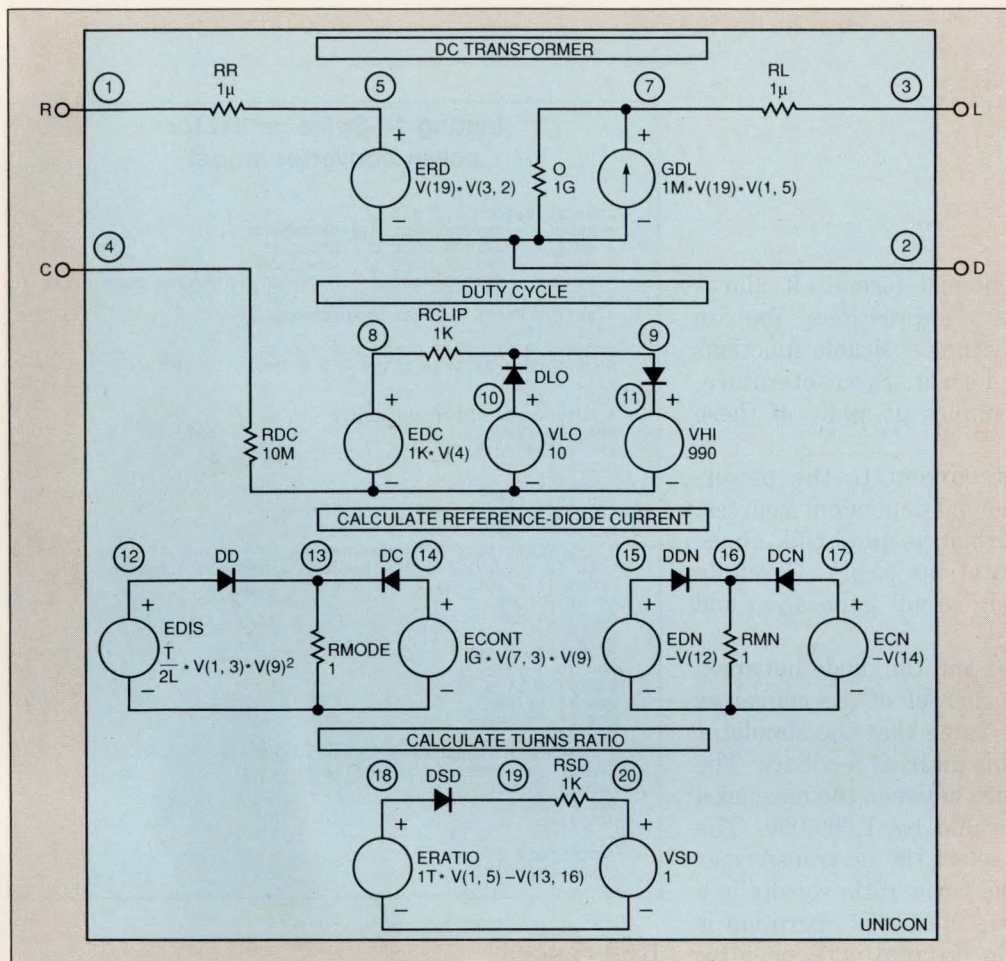


Fig 4—The complete Spice universal power-converter model contains four subcircuits, which perform lossless energy transfer, generate the duty cycle, and calculate the reference-diode current and the turns ratio.

mine the proper turns ratio given the operating conditions of the converter.

In addition to rectifying circuits, diodes are useful for controlling Spice's mathematical operations. This diode action is similar to the flow of a software program in which an executed expression is a function of the response to an if-then-else statement.

Diode networks in the power-converter subcircuit determine if the model is operating in the discontinuous or continuous conduction mode. If the simulator calculates the current for both modes of operation, the value of greater magnitude is the correct one. The diode network in **Fig 3** models this effect. The left half shows the diode ORing scheme for positive polarity currents; the right half shows the scheme for negative currents. Either of the networks would work alone if you knew the polarity of the current, but both networks are necessary to make a flexible model that can handle currents of either polarity.

By taking the voltage across the load resistor in the positive network (node X) and subtracting the load-resistor voltage of the negative network (node Y), you can find the correct magnitude and polarity of the converter's input current. If the current is positive, the voltage at node X will be the greater of the calculated currents for both conduction modes, and the simulator sets the voltage at node Y to zero. Conversely, if the polarity of the current changes, then the simulator

sets the voltage at node X to zero, and the voltage at node Y represents the absolute value of the current. The simulator negates the voltage at node Y when it again calculates the difference between the voltages at nodes X and Y.

The diode network determines the greater of the two voltage magnitudes while retaining the original polarity of the signals. This characteristic means that you can change conduction modes or polarities during a simulation, and the model will automatically modify its transfer function to fit the new operating conditions. Thus, you can use the Spice subcircuit to model and simulate multiquadrant converters such as uninterruptible power supplies and power-factor-correction units.

Note that using diodes to select which expression executes is an approximation that includes the error of the forward voltage drop of the diode. Fortunately, you can minimize this error. Multiplying the signals by a scale factor can ensure that the result is very large compared with the diode drop. You might also reduce the forward voltage of the diode by changing its default parameters. Increasing the value of the saturation current or reducing the emission coefficient will also minimize the approximation error.

Polynomial-equation-based dependent sources enable you to realize mathematical functions in Spice. These equations have the form of $A + Bx + Cx^2 + \dots$ and may contain several variables. Despite the restric-

tive appearance of the polynomial format, it allows Spice to execute many types of expressions. You can even implement division and other desirable functions that don't appear to fit this format. Spice literature, such as Ref 3, provides examples of many of these functions.

Spice calculates the input current to the power-converter model using polynomial-dependent sources. Although the polynomial format is powerful, Spice doesn't perform some computations easily. Carefully selecting parameters may help circuit generation and simulation run more smoothly.

By using dependent sources and the diode network, the op amp forces the input current of the converter model to equal the reference value that the simulator calculates. Fig 1 illustrates this internal feedback. The op amp multiplies the difference between the measured current and the calculated value by 1,000,000. The simulator uses the result to select the dc-transformer turns ratio. An increase in the turns ratio results in a decrease in the input current; thus, this operation is similar to that of a high-gain op amp with negative feedback.

You can use internal feedback when an expression is difficult to derive or realize in Spice. In the converter model, deriving the turns ratio of the dc transformer as a function of the duty cycle for the discontinuous mode is not trivial. Deriving the input current for both conduction modes is easier. You can use high-gain negative feedback to satisfy the derived equations.

Fig 4 is the complete Spice schematic of the universal power-converter model; Listing 1 is its associated netlist. The model limits the duty cycle to between 1 and 99%, which corresponds to voltage values of 0.01 to 0.99V at control node C. The model also limits the turns ratio of the dc transformer to values greater than 1, which is the value that represents the operational limits of the converter topologies. Scale factors convert the voltage across the sense resistors to current and amplify voltage signals so that the relative voltage drops across the diodes are negligible.

You can further generalize the model to simulate additional converters by altering one value. Inserting the variable T/2L in the discontinuous-current calculation (EDIS in Listing 1 and Fig 4) tells the subcircuit the switching period and the output inductance value of the converter. Substitute T/2L for 0.02273 in the Spice listing as follows:

```
EDIS 12 0 POLY(2) 1 3 9 0 0 0 0 0 0 0 0 T/2L
EDN
```

Listing 1—Spice netlist for power converter model

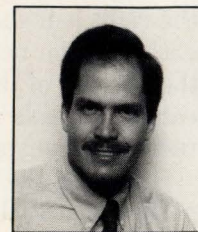
```
.SUBCKT UNICON 1 2 3 4
* NODE 1 = SWITCH NODE R ( REFERENCE )
* NODE 2 = SWITCH NODE D ( DIODE )
* NODE 3 = SWITCH NODE L ( INDUCTOR )
* NODE 4 = SWITCH NODE C ( CONTROL, 1V = 100% DUTY CYCLE )
*
* SWITCH MODEL ( IDEAL TRANSFORMER )
RR 1 5 1U
ERD 5 2 POLY(2) 19 0 3 2 0 0 0 0 1
GL 2 7 POLY(2) 19 0 1 5 0 0 0 0 1MEG
RL 3 7 1U
RO 7 2 1G
* DUTY CYCLE INPUT AND LIMIT
RDC 4 0 10MEG
EDC 8 0 4 0 1K
RCLIP 8 9 1K
VLO 10 0 10
DLO 10 9 DEF
VHI 11 0 990
DHI 9 11 DEF
* CALCULATE PORT R-D CURRENT
EDIS 12 0 POLY(2) 1 3 9 0 0 0 0 0 0 0 0 0.02273
ECONT 14 0 POLY(2) 7 3 9 0 0 0 0 0 1G
DD 12 13 DEF
DC 14 13 DEF
RMODE 13 0 1
* DUAL POLARITY
EDN 15 0 12 0 -1
ECN 17 0 14 0 -1
DDN 15 16 DEF
DCN 17 16 DEF
RMN 16 0 1
* CALCULATE TRANSFORMER TURNS RATIO
ERATIO 18 0 POLY(2) 1 5 13 16 0 1T -1
DSD 18 19 DEF
RSD 19 20 1K
VSD 20 0 1
*
.MODEL DEF D
.ENDS UNICON
```

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2. Cuk, S and R D Middlebrook, "A General Unified Approach to Modeling Switching Dc-to-Dc Converters in Discontinuous Conduction Mode," IEEE PESC Conference Proceedings, 1977.
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4. Vorperian, V, "Simplified Analysis of PWM Converters Using the Model of the PWM Switch, Part I: Continuous Conduction Mode," IEEE Transactions on AES, Vol 26, No. 2, March 1990.

Author's biography

David J Caldwell works as a consultant in the field of analog-circuit design and analysis in Hermosa Beach, CA. He has worked on power and control systems and has been responsible for developing custom hardware in a variety of applications. David has a BSEE from the University of Michigan and an MSEE from the University of Southern California and is a member of the IEEE.



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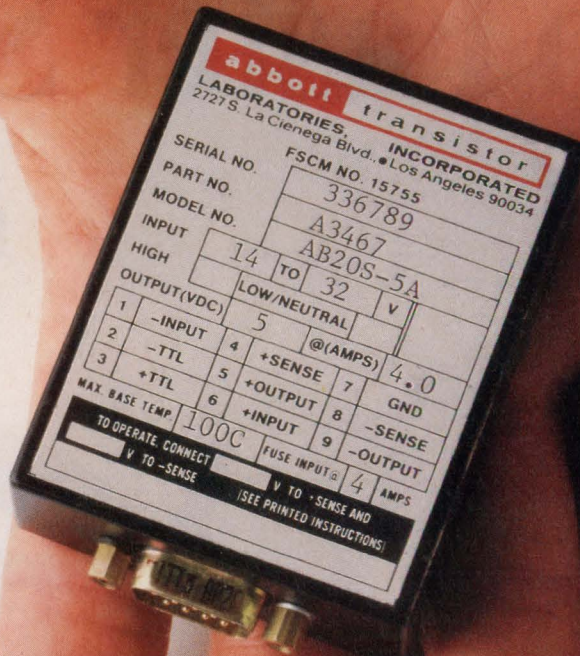
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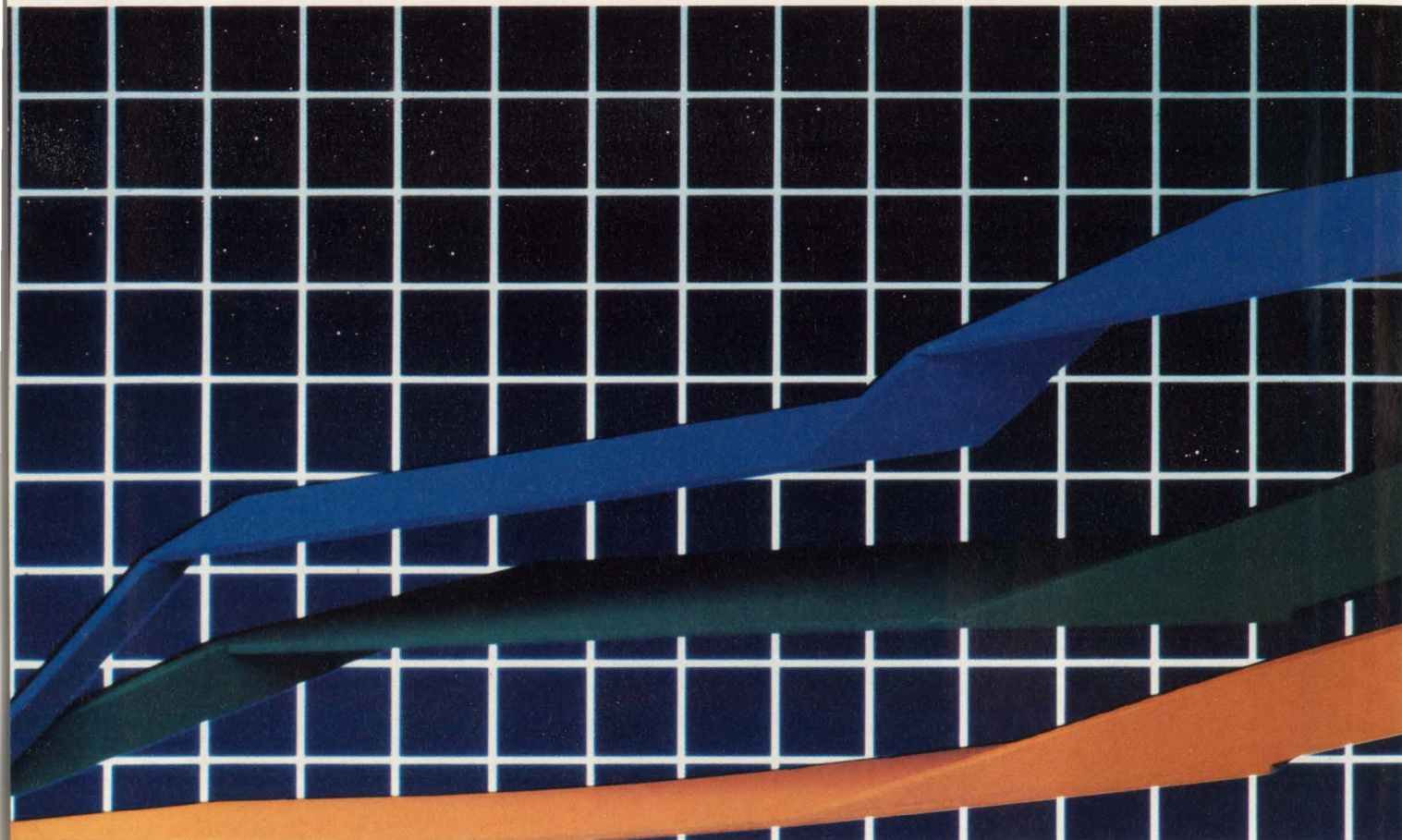
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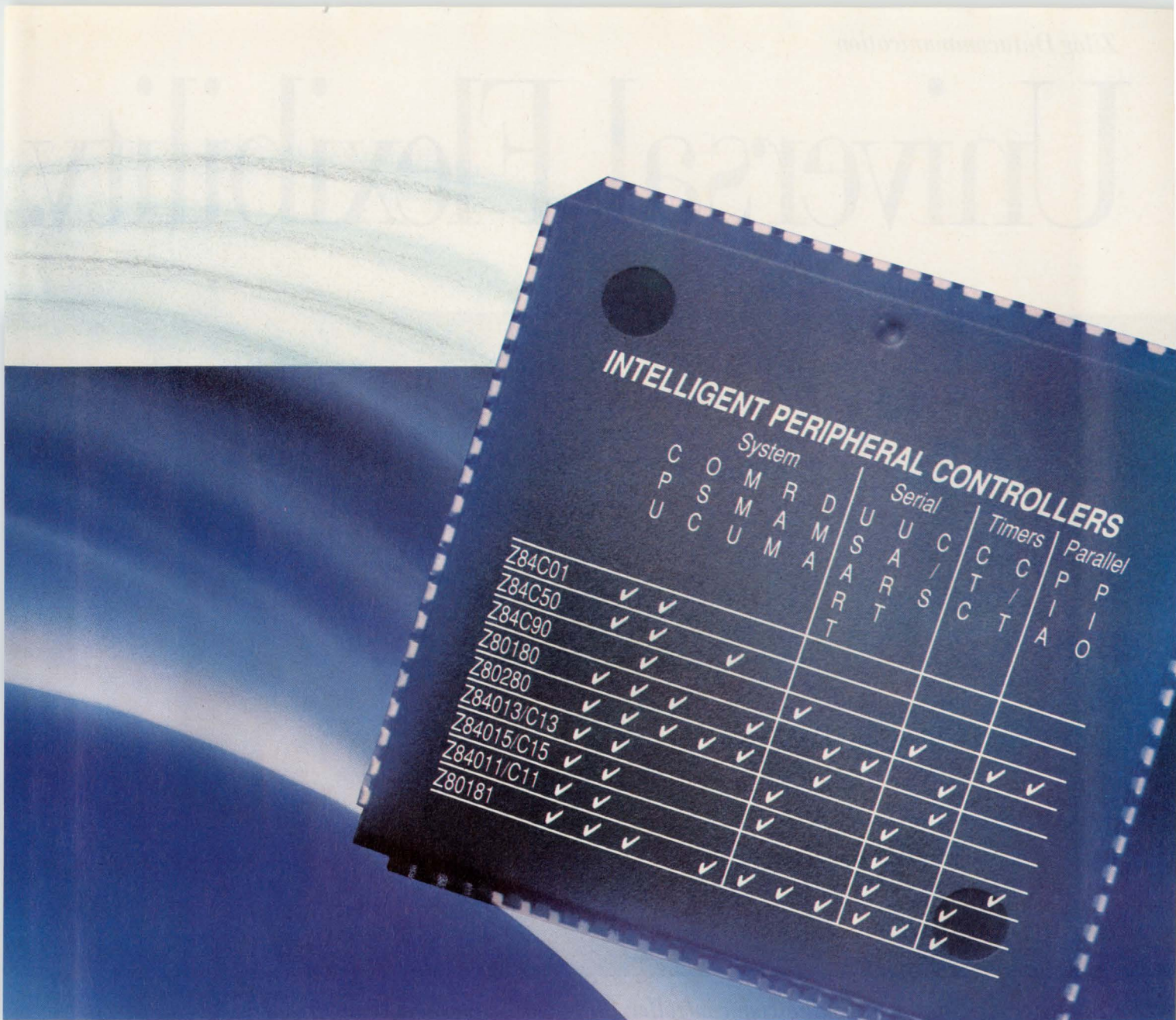
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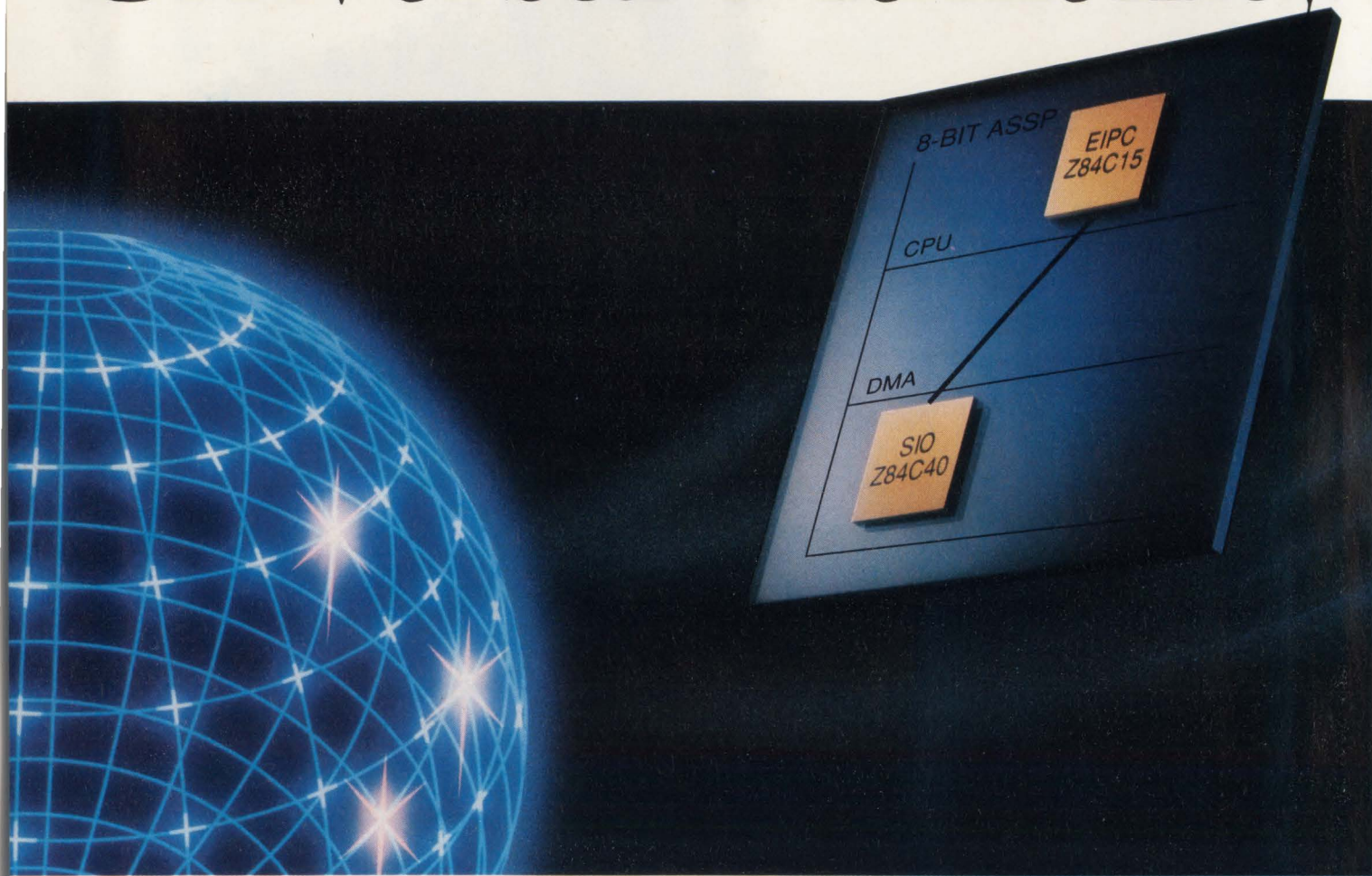


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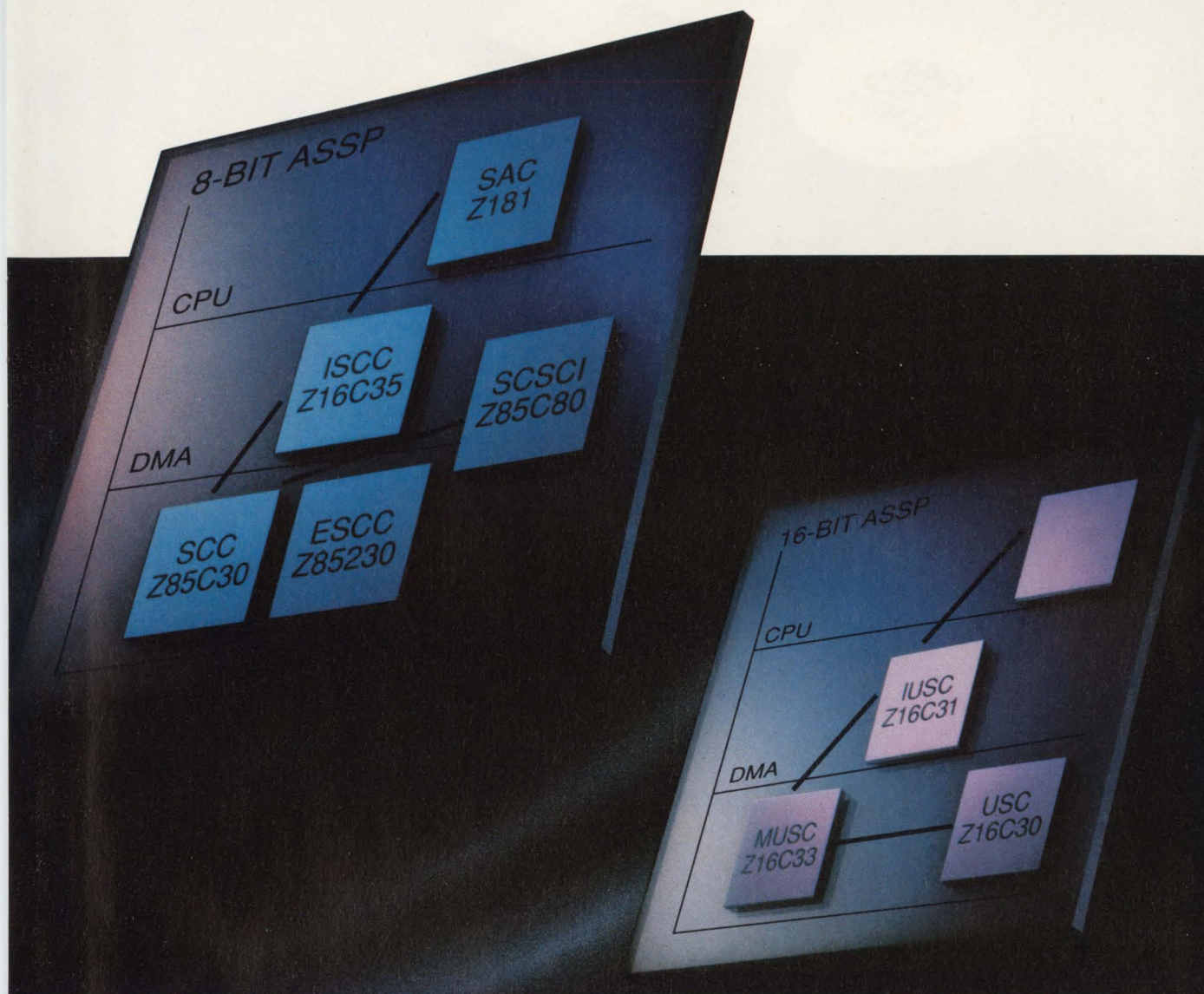
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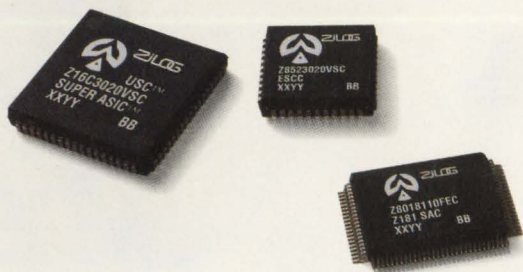
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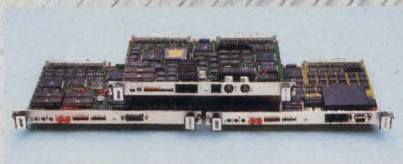
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Phase compensation extends op amp stability and speed

Because most op amps lack provision for altering internal phase compensation, circuit designers often add external compensation to counter the effects of capacitance loading and parasitic capacitance and inductance. External phase compensation also permits the use of lightly compensated, higher-speed amplifiers in low-gain circuits.

Jerald Graeme, *Burr-Brown Corp*

To counter the effects of capacitance loading and parasitic capacitance and inductance, circuit designers can use one of four external phase-compensation methods that suit almost any application. Two of the methods specifically address capacitance loading requirements by controlling the amplifier's open-loop response. The first method requires empirical component selection, but also offers a unique filtering action. The second method removes much of the empirical selection, but can restrict output voltage range.

The other two methods address any phase compensation requirement by controlling the $1/\beta$ curve of the amplifier feedback. These two methods also offer an opportunity for increased slew rate. The second $1/\beta$ method is especially useful for the voltage-follower configuration. An analysis of differential-input configurations defines which method out of the four is best for your design.

All four methods satisfy the external-phase compensation that a capacitive-load drive commonly requires. As **Fig 1** illustrates, capacitive loading degrades frequency stability. Load C_L reacts with the op amp's open-loop output resistance (R_o) to produce an added pole in the feedback path. This pole transforms the amplifier's open-loop response as illustrated by the unloaded and loaded curves of the plot. Phase shift from the added pole introduces response ringing and can even cause oscillation.

Adding the inverse feedback-factor curve, $1/\beta$, to the open-loop response quantifies this response degradation. The nature of the intercept of this curve with the amplifier's open-loop gain predicts stability conditions. The difference in the slopes of the two curves relates to the net phase shift in the feedback loop. At the intercept, internal phase compensation limits this slope difference, or rate-of-closure, to preserve stability (**Ref 1**). For **Fig 1**, the $1/\beta$ curve has zero slope, and the loop phase-shift depends only on the slope of the amplifier's open-loop response. In the unloaded case, this response has a single-pole roll off at the intercept for a slope difference of 20 dB/decade at the intercept. This rate-of-closure predicts a stable 90° phase shift in the loop.

In the loaded case, a second pole at $f_p = 1/2\pi R_o C_L$ alters the amplifier's open-loop response. The resulting 2-pole, or 40-dB/decade, response slope signals a phase shift that eventually reaches 180°. If the phase shift reaches 180° at or before the intercept with the $1/\beta$ curve, oscillation results. Even if oscillation does not occur, this second pole increases response overshoot and ringing, gain peaking, and bandwidth limiting. The

When driving a capacitive load, you commonly need to add external phase-compensation to the op amp.

phase margin (the amount of phase shift $<180^\circ$) predicts the actual response degradation (Ref 2). Typically, a phase margin between 45 and 60° is desired to limit overshoot to 30% and peaking to 3 dB.

For the capacitive-load case of Fig 1, the net phase shift at the intercept is $\phi_i = 90^\circ + \tan^{-1}(f_i/f_p)$. Here, the 90° shift results from the first amplifier pole, and f_i is the frequency of intercept with the $1/\beta$ curve. This intercept frequency is also the bandwidth limit of the circuit. At the intercept, the feedback demand for gain and the available amplifier gain cross. Beyond this frequency, there is insufficient amplifier gain for continuance of the full-circuit response.

Graphical analysis provides insight

You can obtain a design equation for f_i by a graphical analysis of Fig 1's curves. In the unloaded case, the response has a maximum bandwidth defined by the unity-gain crossover frequency f_c . For gains higher than unity, the β factor reduces the maximum bandwidth to the frequency βf_c . With capacitance loading, the intercept retreats along the $1/\beta$ curve to an intercept frequency, f_i , as shown. You can define this frequency in terms of βf_c and f_p through a geometric evaluation of the curves. Note that the dashed line indicating f_p forms right triangles bounded by the $1/\beta$ curve and the two open-loop responses. The hypotenuse of the loaded triangle has a 2-pole slope, or twice the slope of the hypotenuse of the unloaded triangle. Thus, the base of the loaded triangle is one-half the length of the base of the unloaded triangle.

Given the logarithmic nature of the frequency axis, this relationship between triangle bases is expressed as $\text{Log}(f_i) - \text{Log}(f_p) = 0.5\text{Log}(\beta f_c) - \text{Log}(f_p)$. Solving this expression for f_i defines this new bandwidth limit at the geometric mean of f_p and βf_c . And, for Fig 1,

$$BW = f_i = \sqrt{f_p \beta f_c}$$

For the specific components of Fig 1, $R_o \approx 30\Omega$, making $f_p = 530$ kHz. Also, $f_c = 6$ MHz, $\beta = 0.5$ and the resulting intercept frequency and bandwidth limit is $f_i \approx 1.26$ MHz. Then, from before, $\phi_i = 90^\circ + \tan^{-1}(f_i/f_p) = 157^\circ$. The resulting phase margin is $\phi_m = 180^\circ - \phi_i = 23^\circ$, which predicts marginal stability.

Little can be done to restore bandwidth under capacitive loading, although the technique in Fig 3, described later, offers some improvement. More important is the restoration of stable performance, which requires added phase compensation. The most fre-

quently used external-phase compensation permits stable drive of large capacitive loads through the addition of a decoupling resistor and a feedback capacitor. Fig 2 shows this configuration, with R_C and C_C providing the phase compensation. In this circuit, R_2 is part of the total gain-setting network and is also integral to the overall phase compensation. For a voltage-follower circuit, you also need R_2 for phase compensation. The circuit shown is a noninverting amplifier, but you can apply the compensation technique to any configuration. However, using this technique with differential-input connections degrades common-mode rejection, as discussed later with Fig 6.

The Fig 2 phase compensation provides a bypass-feedback loop that takes control of the op-amp feedback at higher frequencies. With this compensation, the response of the primary feedback loop still develops a 2-pole roll off, but this response does not reflect op-amp-feedback conditions. Instead, the bypass-feedback loop retains stable feedback conditions and the response curve is largely unaffected by the capacitive

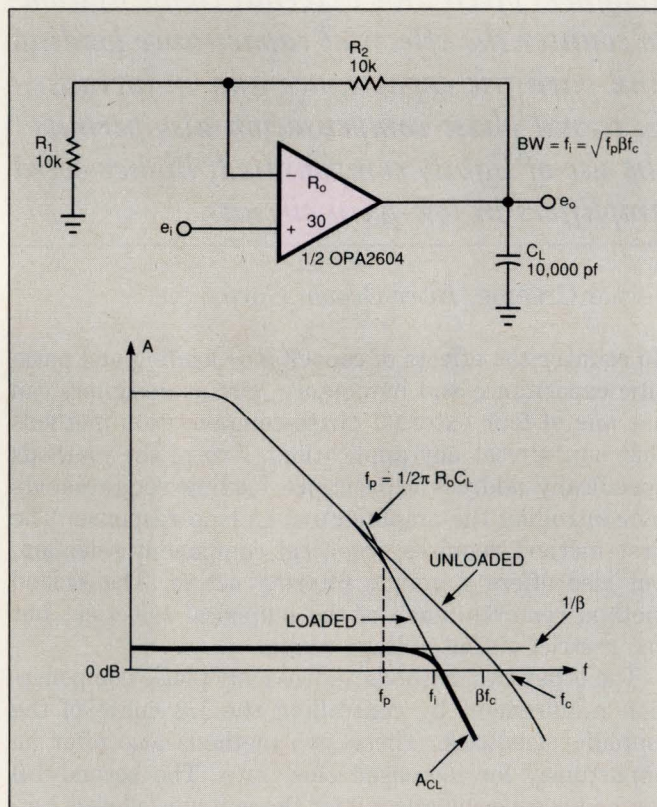


Fig 1—Capacitive loading of an op amp's output resistance introduces a second pole in the open-loop gain response for a -40 dB/decade slope at the $1/\beta$ intercept.

load. Compensation resistor R_C first isolates the op amp from the effect of C_L and then compensation capacitor C_C bypasses the primary feedback loop.

At first, the addition of R_C would seem to aggravate the problem because it moves the pole created by C_L to an even lower frequency, f_p' . Similarly, the addition of C_C causes the $1/\beta$ curve to drop to the unity-gain axis for the maximum possible demand on stability. As shown, the response curve of the primary loop has a well-developed 2-pole response at this curve's intercept with the $1/\beta$ curve. This action suggests poor frequency stability.

However, this response curve only represents the open-loop gain from the op-amp inputs to the circuit output. This curve does not represent the feedback conditions controlling the amplifier at higher frequencies. With two feedback paths, the op amp is controlled by whichever path supplies the feedback current to resistor R_1 . At low frequencies, the impedance of C_C is large, and the feedback path through R_C and R_2 dominates. At high frequencies, C_C prevails and the response curve of the bypass loop is in control at the $1/\beta$ intercept. As a result, the bypass response curve represents the open-loop gain from the op-amp inputs to the op-amp output and not to the overall circuit output.

The amplifier input-to-output response normally provides stable conditions for gain or $1/\beta$ all the way down to unity gain. As shown, the resulting bypass response is almost unaffected by C_L because of the decoupling provided by R_C . This response intercepts the $1/\beta$ curve before fully developing a 2-pole roll off and predicts good stability characteristics. In practice, Fig 2's OPA2604 drives the 10,000-pF load with only 12% overshoot and 0.3-dB gain peaking. For audio amplifiers like the OPA2604, this phase compensation permits stable drive of the capacitance of long shielded cables.

Component selection remains empirical

The actual choice of R_C and C_C in Fig 2 is complicated by the nature of the op amp's open-loop output impedance. This impedance is not simply resistor R_o as modeled in Fig 2. A typical op amp has an open-loop output resistance in the range of 100 Ω to 1 k Ω at dc, but the output impedance drops dramatically to about 10 to 50 Ω as frequency increases. At very high frequencies, this impedance may rise again. Also, the output impedance is sensitive to the instantaneous level of the amplifier's output current.

Numerous factors contribute to these effects, making

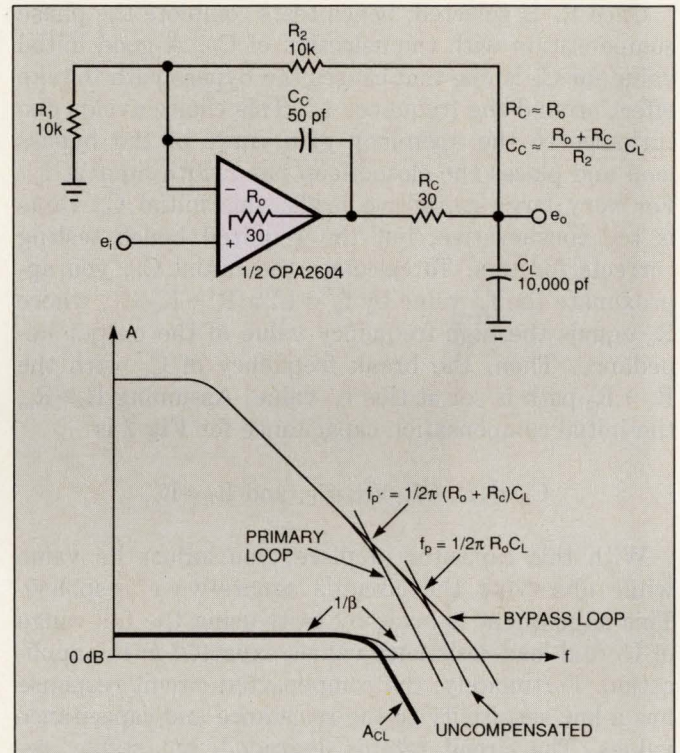


Fig 2—A decoupling resistor, R_C , and bypass capacitor, C_C , isolate an op amp from the effects of the capacitance load, C_L .

complete modeling of output impedance not generally worthwhile. As a result, circuit analysis only offers a basic guide to selection of R_C and C_C , and the final choice is empirical. Note that circuit simulation with op-amp models is limited by this same constraint. Spice op-amp models typically include high- and low-frequency output impedances that are modeled by resistors.

Despite these limitations, guidelines can expedite the initial selection of R_C and C_C . First, you choose a value for R_C that is in the range of the op amp's high-frequency output resistance, typically 10 to 50 Ω . To determine the high-frequency value of R_o , you find frequency f_p from a measured response plot and then $R_o = 1/2\pi C_L f_p$. You should not make R_C arbitrarily large, because the voltage drop across R_C detracts from the output-voltage range. This voltage drop does not introduce a gain error because R_C is enclosed in the primary feedback loop. Larger values of R_C also restrict the bandwidth, which is now limited to $f_p' = 1/2\pi(R_o + R_C)C_C$. Fortunately, even small values of R_C dramatically reduce the phase shift developed across R_o by C_L .

Phase-compensation methods involve the control of the amplifier's open-loop response or the control of the $1/\beta$ curve of the amplifier's feedback loop.

Once R_C is selected, bench tests complete the phase compensation with the selection of C_C . A good initial value for C_C is one that causes the bypass path to take effect around the frequency f_p' . This choice avoids disturbance to the open-loop gain curve of the bypass loop and places the closed-loop bandwidth limit at f_p' . For very large capacitive loads, this initial C_C value is too conservative, but the required bench testing corrects for this. To calculate the initial C_C , you approximate the f_p' value by $f_p' = 1/2\pi(R_o + R_C)C_L$, where R_o equals the high-frequency value of the output impedance. Then, the break frequency of C_C with the $R_C + R_2$ path is set at this f_p' value. Assuming $R_2 \gg R_o$, the initial compensation capacitance for **Fig 2** is

$$C_C \approx [(R_o + R_C)/R_2]C_L, \text{ and } R_C \approx R_o.$$

With this capacitor in place, you adjust its value while observing the circuit's square-wave response. This adjustment is made by tests using the full range of C_L and load-resistance values expected in the application. Fortunately, the compensated circuit response has a low sensitivity to the resistance and capacitance values. The circuit retains degraded, but stable, response over a 100:1 range around the design center. Thus, 2:1 variations in R_o , due to manufacturing tolerances, do not greatly affect circuit stability. However, you still need bench testing to define the design center.

Compensation also filters noise

The phase compensation of **Fig 2** also provides unique filtering that rejects amplifier noise better than most op-amp filter circuits (**Ref 3**). The op amp amplifies the input-voltage noise by a gain of $1/\beta = 1 + (R_2/R_1)$ in **Fig 2** and in the analogous inverting configuration. To filter out high-frequency noise, it's common practice to bypass R_2 with a capacitor. However, this only removes the R_2/R_1 portion of the op amp's noise gain. Without R_C and C_C , the amplifier's high-frequency noise continues to receive a gain of $1/\beta = 1$ up to the open-loop roll-off of the op amp's gain. This same condition is true for almost any op-amp connection, including active filters. For low-frequency applications, the inadvertently included op-amp noise can dominate noise performance.

In the **Fig 2** configuration, the filter formed by R_C and C_L interrupts the continuation of a unity noise gain. At higher frequencies, the op amp is still under the control of a unity feedback factor as provided by the C_C feedback. Thus, amplifier input noise continues

to receive a corresponding unity gain at high frequencies. However, this unity gain extends only to the op-amp output. Between this output and the actual circuit output is the lowpass filter of R_C and C_L . This filter shunts the high-frequency amplifier noise to ground. For filter applications, C_L is not incidental and you must add it as an element in the circuit design.

Pole and zero compensate for C_L

A second external-phase-compensation method removes most of the empirical component selection. However, this method does reduce the output voltage range when significant output currents are supplied. This second method (**Fig 3**) introduces a paralleled resistor and capacitor in series with the amplifier output, but inside the feedback loop. The result is a pole and zero compensation of a capacitive-loaded amplifier. As illustrated, the circuit is a voltage follower, but this compensation method applies to all op-amp configurations.

With the circuit in **Fig 3's** compensation, the capacitive load that creates the problem becomes part of the phase compensation solution. As before, load C_L reacts with the circuit's open-loop output resistance, creating a second response pole. In the uncompensated case, C_L reacts with R_o to produce a pole at f_p , which compromises frequency stability as described with **Fig 1**. To restore stability, this pole is first moved back to f_p' by adding resistor R_C . The resulting response is free to be redirected anywhere within the bounds of the uncompensated response. Bypassing R_C with C_C gradually removes the effect of the lower frequency f_p' by restoring a 20-dB/decade response slope. This is the response slope at the new f_i' intercept with the $1/\beta$ curve, and stability is improved.

To quantify the improvement and select the compensation components, you need to examine the frequencies of the compensated poles and zeros relative to f_i' . You can use many pole and zero combinations. Different combinations produce optimum conditions for different op-amp configurations. However, it is desirable to use a systematic approach to select compensating components. Fortunately, circuit stability is rather insensitive to the chosen pole-zero combination, and a single selection method adequately restores phase margin for all configurations.

Phase shift at the compensated intercept is interpreted from the duration of the new 20-dB/decade region. For about 90° of phase margin, you would set this region to span one decade of frequency both before and after f_i' . Experience shows that the decade after

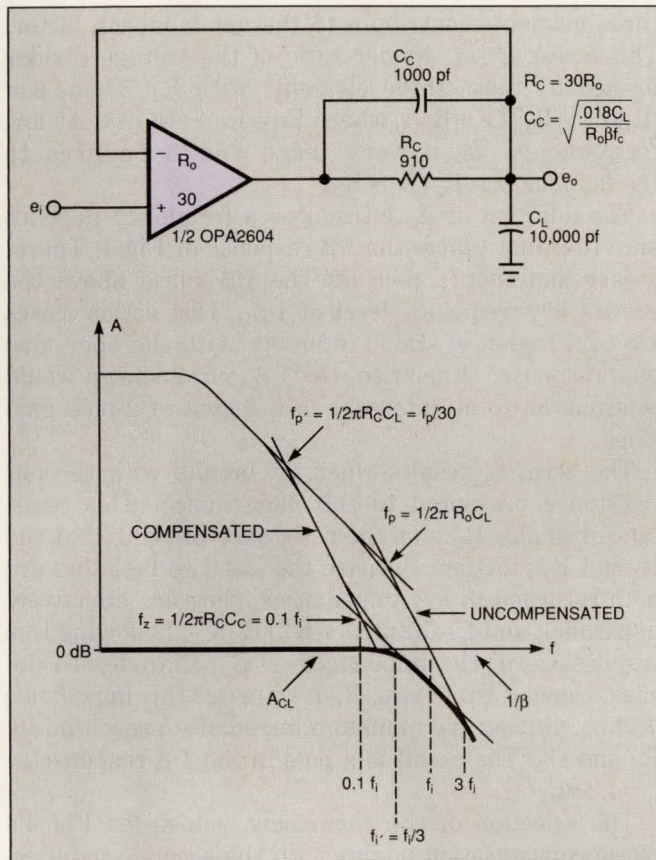


Fig 3—A parallel-connected resistor and capacitor provide pole-zero phase compensation for a capacitive-loaded op amp.

f_i' is important because secondary poles in this region add even more phase shift. However, the decade before the intercept is unnecessarily restrictive of bandwidth. In practice, the 20-dB/decade span before intercept is reduced to about one-half of a decade of frequency. Given the logarithmic nature of the frequency axis, the one-half decade equates to about a factor of three in frequency.

Fig 3 shows a compensated response that approximates the above conditions. The compensated intercept frequency is set at $f_i' = f_i/3$, which results in a 20-dB/decade response span up to $3f_i$. Thus, above f_i' , the reduced response slope covers a frequency range of 9:1 or almost a decade. Before the intercept, this span continues as set by the choice of f_z . For one-half decade in this region, you should place the compensation zero at $f_z \approx f_i'/3$, which is approximately equal to $0.1f_i$. The result is a 20-dB/decade span covering a frequency range of about 30:1.

The component selection for the **Fig 3** circuit follows

from the previously stated conditions and the measurement of f_p . Resistor R_C is chosen first through a relationship between frequencies f_p and f_p' . These two frequencies are also separated by a 30:1 range as seen from the geometry of the responses. The straight-line extensions of the compensated and uncompensated responses form a parallelogram. Thus, the distance between f_p and f_p' equals that between $3f_i$ and $0.1f_i$ —a 30:1 span. To make $f_p' = f_p/30$, the compensation resistor is set at $R_C \approx 30R_o$. Note that this setting makes $R_C \gg R_o$, and the resulting phase compensation is insensitive to the actual impedance of R_o . Thus, empirical fine tuning of the compensation is no longer necessary.

A drawback of the higher R_C value is reduced output voltage range due to the large voltage drop across this resistor. The high-frequency value of R_o is still approximated by empirical measurement of frequency, f_p . Op-amp data sheets do not always reflect this R_o value, which is determined from the relationship $R_o = 1/2\pi f_p C_L$.

Using the selected value of R_C , capacitor C_C is defined by the response conditions established for **Fig 3**. For $f_z = 0.1f_i = 1/2\pi R_C C_C$, the compensation capacitance is defined by $C_C = 5/\pi R_C f_i$. Frequency f_i is known from the previous expression of $f_i = \sqrt{f_p \beta f_c}$, where $f_p = 1/2\pi R_o C_L$, and f_c is the unity-gain crossover frequency of the op amp. For **Fig 3** with $R_C = 30R_o$,

$$C_C = \sqrt{0.018 C_L / R_o \beta f_c}$$

With the resulting phase compensation, the OPA2604 again drives a 10,000-pF load. The resulting overshoot is 18% and gain peaking is 1.3 dB. As with **Fig 2**, **Fig 3**'s phase compensation retains a degraded but stable response for a 10:1 increase or decrease in the value of the load capacitance, C_L . Bandwidth is again set by the intercept of the open-loop gain and the $1/\beta$ curve. As described, this intercept is set at $f_i' = f_i/3$. As with **Fig 1**, $f_i = \sqrt{f_p \beta f_c}$, where $f_p = 1/2\pi R_o C_L$, and the **Fig 3** bandwidth is

$$BW = \sqrt{0.18 \beta f_c / R_o C_L}$$

With the specific components shown, the capacitance loading reduces bandwidth to 600 kHz from the 6 MHz of the unloaded case.

For the voltage-follower example, $1/\beta$ follows the 0 dB or unity-gain axis in **Fig 3**, but this axis does not generally define the critical intercept. In other op-amp configurations, the $1/\beta$ curve is shifted upward and the

Depending on the circuit, you can use either empirical or analytical component-selection methods.

intercept with this curve defines f_i for the component selection. The β factor in the previous equation for C_C automatically adjusts the component selection for this difference in intercept. A second caution with **Fig 3** is that the pole-zero compensation results in poor settling time (**Ref 4**). Where settling time is important, you should use the circuit of **Fig 4** or **Fig 5** without capacitor C_C .

Compensation tailors $1/\beta$

In the previous two circuits, phase compensation is directed toward control of the amplifier's open-loop response at the $1/\beta$ intercept. The circuits that follow control the $1/\beta$ response itself. Instead of reshaping the open-loop response, these circuits tailor the $1/\beta$ curve to intercept the open-loop response at the point where this response offers good stability, which is accomplished with either negative or positive feedback. The $1/\beta$ phase compensation permits the same capacitive load drive as the previous circuits. In addition, the $1/\beta$ method offers an opportunity for a higher slew rate.

The circuit in **Fig 4** alters the feedback factor using negative feedback provided by R_C and C_C . This method, shown in **Fig 4** as a noninverting-amplifier configuration, also applies to all other op-amp configurations. For the voltage-follower case, resistor R_2 is again added as part of the phase compensation. In addition, the **Fig 4** phase compensation applies to a 2-pole amplifier response of any origin. The second pole can be the result of capacitive loading, a lightly phase-compensated amplifier, or parasitic effects in a high-frequency amplifier. This versatility is not available for the circuits in **Figs 2** and **3**. **Fig 2** depends on a unity-gain-stable op amp, and **Fig 3** requires the load capacitance as part of the phase compensation.

Fig 4's circuit connects the phase-compensation elements between the op-amp inputs to alter the feedback factor without altering the circuit's closed-loop gain. Elements R_C and C_C are bootstrapped on the input signal e_i and they produce no feedback current in direct response to e_i . This signal is impressed only upon R_1 , where the signal creates a feedback current to produce a corresponding voltage on R_2 . Thus, R_1 and R_2 continue to control the closed-loop gain experienced by e_i .

The circuit does, however, impress the feedback error signal between the op-amp inputs on R_C and C_C . This error signal produces a current in these elements, as well as in R_1 . All three elements contribute to the gain received by the feedback error signal. Thus, the

three elements contribute to the net feedback factor. This factor is the divider ratio of the voltage divider formed by these three elements with R_2 . Then, $\beta = (R_1 \| Z_C) / (R_1 \| Z_C + R_2)$, where $Z_C = R_C + (1/C_C s)$. At low frequencies, Z_C is very large and β reduces to the familiar $\beta_0 = R_1 / (R_1 + R_2)$.

The addition of Z_C introduces a frequency dependence to β that tailors the $1/\beta$ response of **Fig 4**. There, a zero and then a pole lift the $1/\beta$ curve above the curve's low-frequency level of $1/\beta_0$. This action raises $1/\beta$ to a region of stable intercept with the open-loop gain response. Otherwise, the $1/\beta_0$ curve shown would continue on to an intercept in a region of 2-pole gain slope.

The zero, f_z , results when C_C breaks with the net resistance presented to this capacitance. This resistance includes R_C plus the resistance presented at the R_1 and R_2 junction. Because the last two resistors are both returned to low impedances, they are effectively in parallel, and $f_z = 1/2\pi(R_C + R_1 \| R_2)C_C$. Following this response-zero, the impedance of C_C continues to decline, causing $1/\beta$ to rise. R_C terminates this impedance decline, setting the minimum impedance presented by R_C and C_C . The result is a pole in the $1/\beta$ response at $f_p = 1/2\pi R_C C_C$.

The selection of the component values for **Fig 4**'s phase compensation begins with the second amplifier-response pole. Whatever the cause of the pole, its position defines a minimum amplifier gain, A_{\min} , for which the amplifier displays good stability. Placing the $1/\beta$ intercept at this pole assures about 45° of phase margin; less phase margin is undesirable. An intercept prior to the second pole increases phase margin but also increases noise gain and reduces bandwidth. An earlier intercept requires raising the $1/\beta$ curve further at high frequencies. This increases the gain for high-frequency noise. Similarly, an earlier intercept reduces bandwidth, since f_i defines the circuit bandwidth.

To place the intercept at the second pole, select R_C to set the high-frequency $1/\beta$ equal to A_{\min} . In the case of a lightly compensated amplifier, A_{\min} is a specified value. For other cases, you determine A_{\min} empirically as the open-loop gain level at the second amplifier pole. For **Fig 4**, the high-frequency $1/\beta$ is $1/\beta_0 + R_2/R_C = A_{\min}$. Solving for R_C yields

$$R_C = R_2 / (A_{\min} - 1/\beta_0),$$

where $1/\beta_0 = 1 + R_2/R_1$.

To phase compensate the circuit in **Fig 4** for capaci-

tive loading, you first approximate A_{\min} from the specified amplifier output resistance. Resistance R_o forms a pole with C_L at $1/2\pi R_o C_L$, and you choose the compensation to align the $1/\beta$ curve with this pole. The pole nearly always occurs in a region of the amplifier response where the amplifier gain (A) is approximately equal to f_c/f . Here, f_c is the unity-gain crossover frequency of the op amp. At the intercept frequency $f = f_i$, making $A_{\min} = f_c/f_i = 2\pi R_o C_L f_c$.

Next, you choose C_C to ensure that f_p and f_z do not disturb the phase conditions at the intercept chosen above. Making $f_p = 0.1f_i$ sufficiently removes f_p and f_z from the intercept. Then, the phase contributions of f_p and f_z are both fully developed and cancel when the intercept is reached. For $f_p = 0.1f_i$, $C_C = 5/\pi R_C f_i$. In this case, f_i is the frequency of the intercept and also the frequency at which A_{\min} occurs. For lightly compensated amplifiers, you can read this frequency from the open-loop response of the data sheet. In other cases, you determine the value of f_i by measurement.

Phase compensation has side effects

The phase compensation for Fig 4's circuit offers access to an increased slew rate but reduces input impedance. A higher slew rate results when you use lightly compensated op amps in low gain applications. Several op amps are available with two phase-compensation options to offer higher slew rate and bandwidth to high-gain applications. One option phase-compensates the amplifier for unity-gain stability and serves all applications. The other option uses lighter phase compensation to avoid restriction of slew rate and bandwidth for gains at or above some value of A_{\min} . The circuit in Fig 4's external phase compensation bridges the difference. The higher slew rate normally available to higher gain applications becomes available to lower gains as well.

The key to this speed benefit is the altered $1/\beta$ curve. The Fig 4 circuit applies the faster, lightly compensated version of the amplifier to low-gain applications, with frequency stability restored by the external phase compensation. For the OPA37 shown, the compensation extends the slew rate to $12V/\mu\text{sec}$ from the $2V/\mu\text{sec}$ of the unity-gain-stable OPA27 companion product.

Bandwidth, however, does not similarly enjoy this increase because the elevated $1/\beta$ curve moves the f_i intercept back in frequency. As a result, bandwidth is essentially unchanged from that of the unity-gain-stable version. Settling time is improved with this op-

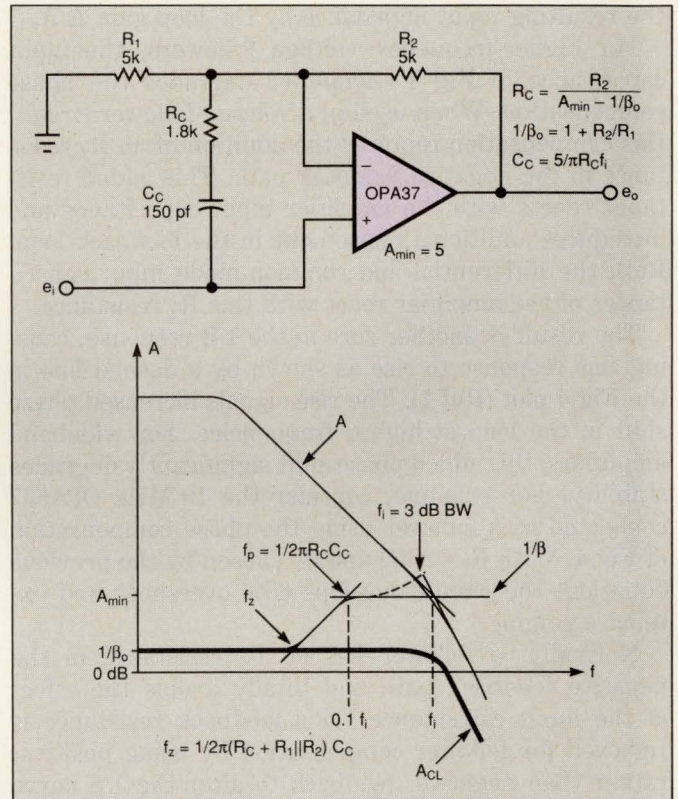


Fig 4—The addition of a zero and pole to $1/\beta$ phase-compensates any 2-pole op-amp response, regardless of the cause of the second pole.

tion because of the increased slew rate. However, this improvement is counteracted by a long settling tail introduced by f_z and f_p . To avoid this tail, caused by the added pole and zero, you can replace C_C by a short circuit. However, removing C_C increases the gain available to the amplifier's input offset voltage and low-frequency noise.

The circuit's (Fig 4) phase compensation also alters input impedance for noninverting applications. At first, you might expect a very low impedance because the compensation elements connect directly to the circuit input. However, as described earlier, these elements are bootstrapped on the input signal, and no input current flows from them in direct response to e_i . Indirectly, e_i creates a signal on R_C and C_C through the gain-error signal between the op-amp inputs. This signal is $e_o/A = A_{CL}e_i/A$, where A_{CL} is the closed-loop gain of the circuit and A is the open-loop gain of the amplifier. The resulting current supplied to the circuit input defines an input impedance of $Z_I = AZ_C/A_{CL}$, where $Z_C = R_C + (1/C_C s)$. Thus, the bootstrapping of Z_C boosts

One method of phase compensation adds the benefit of a filtering action that can significantly reduce amplifier noise.

the resulting input impedance by the loop gain A/A_{CL} .

For higher-frequency voltage followers, the input capacitance of Fig 4's amplifier degrades the phase compensation. When used in a voltage-follower circuit, this compensation requires the addition of an R_2 resistance in the negative feedback path. This added resistance reacts with the amplifier input capacitance and introduces additional phase shift in the feedback loop. Both the differential and common-mode input capacitances of the amplifier react with this R_2 resistance.

The result is another zero in the $1/\beta$ response, causing this response to rise as shown by a dashed line in the Fig 4 plot (Ref 1). The rise signals increased phase shift in the loop at higher frequencies. For wideband amplifiers, this added phase shift significantly degrades stability. For example, consider the 16-MHz OPA637 connected as a follower using the phase compensation of Fig 4. With $R_2 = 2$ k Ω and C_C chosen by the previous equation, the circuit develops 65% overshoot and extensive ringing.

Normally, a follower has no R_2 resistance in the negative feedback path and totally avoids the effect of the input capacitance. This feedback resistance is removed for follower compensation by using positive, rather than negative, feedback to alter the $1/\beta$ curve (Ref 5). The resulting configuration actually benefits from amplifier input capacitance. Moreover, positive feedback is the only external phase-compensation method available to committed, voltage-follower op amps. The positive-feedback method also works for phase compensation of other noninverting configurations. However, these configurations require an R_2 resistance and little advantage remains over Fig 4's method. Also, you should not use the positive feedback approach for differential-input configurations, as explained by Fig 6.

The Fig 5 voltage-follower case illustrates positive-feedback phase compensation. In this circuit, compensation elements R_C and C_C again form a feedback voltage divider with R_2 . However, R_2 is no longer in the negative feedback path where it could react adversely with amplifier input capacitance. Instead, the circuit adds a positive feedback path to the normal follower connection. With both negative and positive feedback factors, β_- and β_+ , the net feedback of an op amp is the difference between the two feedback factors (Ref 6). For Fig 5, $\beta_- = 1$ and $\beta_+ = R_2/(R_2 + Z_C)$, where $Z_C = R_C + (1/C_C s)$. The result is a net feedback factor of

$$\beta = (1 + R_C C_C s) / [1 + (R_C + R_2) C_C s].$$

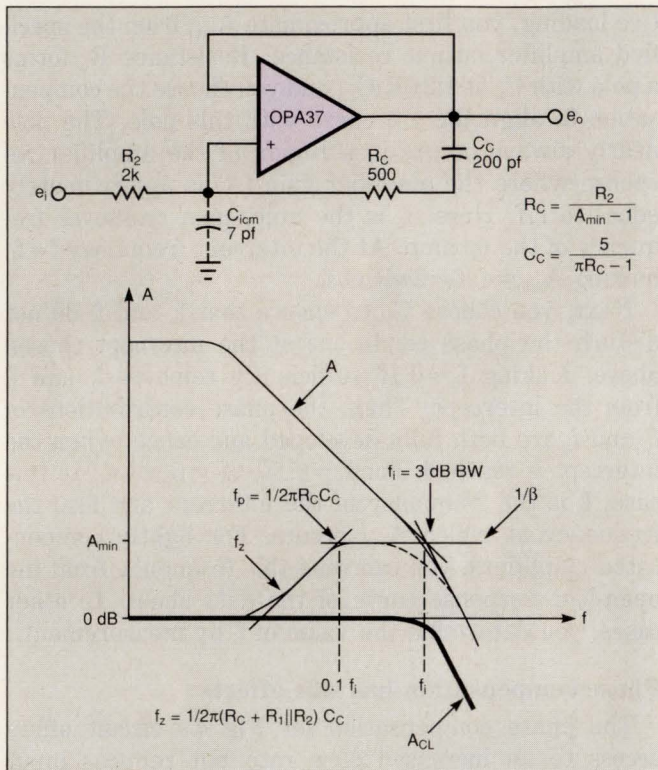


Fig 5—For a high-frequency voltage follower, positive feedback provides phase compensation with less sensitivity to amplifier-input capacitance.

The resulting $1/\beta$ curve, which is much like that of Fig 4, has a pole and zero to lift the $1/\beta$ curve before the intercept. For Fig 5, the zero occurs at $1/2\pi(R_C + R_2)C_C$ and the pole occurs at $1/2\pi R_C C_C$. The bootstrapped phase-compensation elements limit disturbance to closed-loop gain and input impedance. The compensation elements ride on signal e_i because of bootstrap feedback from the amplifier output. Because e_i does not directly develop a signal on these elements, the circuit remains a voltage follower with $e_o = e_i$. The only signal on these elements results from the gain-error signal between the op-amp inputs. This signal, $e_e/A = e_i/A$, appears across $Z_C = R_C + (1/C_C s)$, resulting in a circuit input current of e_i/AZ_C . Thus, the input impedance of Fig 5 is $Z_i = AZ_C$.

Component selection favors Z_i or noise

The choice of the Fig 5 components follows the Fig 4 approach but with an added degree of freedom. The high-frequency value of $1/\beta$, $1 + (R_2/R_C)$, is again chosen for an intercept at the amplifier's minimum stable gain A_{min} . Typically, A_{min} occurs at the second amplifier re-

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Phase compensation often involves tradeoffs in performance parameters such as slew rate, input impedance, and bandwidth.

sponse pole as shown. Again, A_{\min} is a specified value for the op amp or often set by capacitance loading at $A_{\min} = 2\pi R_0 C_L f_c$. For Fig 5, $R_C = R_2 / (A_{\min} - 1)$. Next, the pole of the $1/\beta$ response is set a decade below the intercept or $f_p = 1/2\pi R_C C_C = 0.1f_i$. This setting assures that the f_p and f_z shown have canceling phase effects when the intercept is reached. Then, $C_C = 5/\pi R_C f_i$.

The above equations for R_C and C_C define the relative values of the compensation elements. However, the absolute values depend upon first choosing a value for R_2 . In Fig 4, this resistor is part of the normal feedback network and the resistor value is chosen with other criteria. In Fig 5, however, R_2 only serves as a phase compensation element, and you are free to set its resistance value.

The factors now guiding the R_2 choice are input impedance and noise. With $Z_i = AZ_C$, input impedance increases with higher values of R_C and lower values of C_C . The previous equations for R_C and C_C show that input impedance increases with increasing R_2 values. However, noise also increases because R_2 generates a

voltage noise of $\sqrt{4KTR_2}$ at the amplifier input. Thus, the choice of the R_2 value is a compromise.

With the specific components shown in Fig 5, a compromise $R_2 = 2 \text{ k}\Omega$ results in $R_C = 500\Omega$ and $C_C = 200 \text{ pF}$. The OPA637 then delivers a slew rate of $135\text{V}/\mu\text{sec}$, as compared with the $55\text{V}/\mu\text{sec}$ available with the unity-gain-compensated OPA627. Resulting overshoot is 16%, as compared with 65% in an equivalent solution from Fig 4. This latter improvement is the result of the difference in effects of amplifier input capacitance. As described with Fig 4, this input capacitance causes the circuit's $1/\beta$ curve to rise at high frequencies, which increases the loop phase shift. In Fig 5, the opposite effect occurs, and the $1/\beta$ curve declines as a result of amplifier-input capacitance. The amplifier's common-mode input capacitance bypasses R_2 , which rolls off the positive feedback and the $1/\beta$ curve. As indicated by a dashed line, this action reduces, rather than increases, the rate-of-closure of the $1/\beta$ and gain curves.

Where noise is more important than input impedance, you choose R_2 so that its noise voltage is only about one-third that of the amplifier input. This one-third factor turns into a one-ninth contribution to overall rms noise. The rms addition of the resistor and amplifier noises first raises each term to the second power. As a result, the resistor noise is essentially negligible. For a resistor noise $\sqrt{4KTR_2}$ equal to one-third the amplifier noise (e_n), R_2 is set to

$$R_2 = e_n^2 / 36KT,$$

where K is Boltzman's constant, or 1.38×10^{-23} , and T is the temperature in degrees Kelvin, or $^{\circ}\text{C} + 273$. Under these conditions, the $e_n = 5 \text{ nV}/\sqrt{\text{Hz}}$ of the OPA637 calls for $R_2 = 500\Omega$. Then, $R_C = 125\Omega$ and $C_C = 820 \text{ pF}$.

Differential input connections of op amps impose a special restriction on external phase compensation. The benefit realized with differential inputs is common-mode rejection, and phase compensation added to the circuit can degrade this rejection. To retain high common-mode rejection, you must place any added phase-compensation where there is no common-mode swing across the compensation elements.

Fig 6 illustrates this technique with the differential-amplifier connection. Consider a common-mode signal connected to the e_1 and e_2 inputs. Under balanced conditions, the circuit rejects this signal and produces no signal at the e_o output terminal. However, a common-

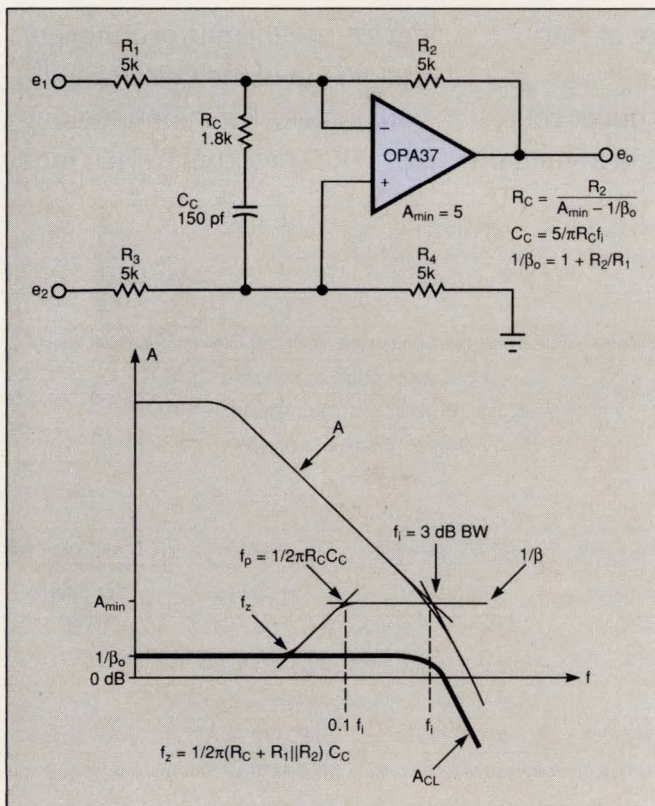
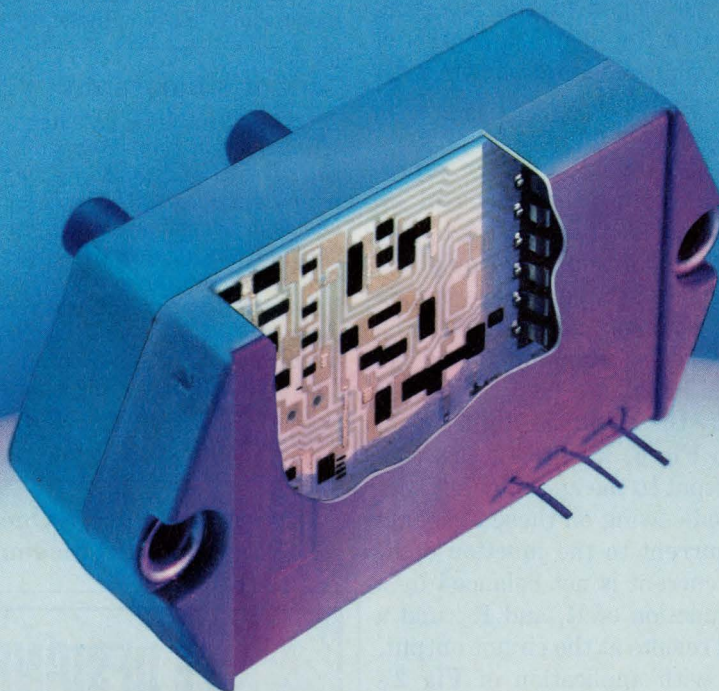


Fig 6—External phase compensation for differential-input connections is placed where no common-mode signal appears across the compensation elements.

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Differential-input connections of op amps impose special restrictions on external phase compensation.

mode signal is present at the op-amp input terminals. The voltage divider formed by R_3 and R_4 transmits a portion of the e_2 signal to the op amp's noninverting input. This signal is also developed at the inverting input of the amplifier through the feedback control of this input. For the equal-value resistors shown, one-half of any common-mode signal connected to the e_2 terminal appears at both amplifier inputs.

These input and output signal conditions are representative of all differential-input connections of op amps. A common-mode signal is transmitted to the op-amp inputs but not to the op-amp output. Any phase compensation elements added between these inputs and the output contain a common-mode signal. The resulting signal current degrades common-mode rejection by introducing a signal imbalance.

For example, if you apply the circuit in Fig 5's compensation to the circuit in Fig 6, R_C and C_C are connected from the op-amp output to the amplifier's noninverting input. Common-mode swing on these elements then introduces a signal current to the junction of R_3 and R_4 . The effect of this current is not balanced by a matching current at the junction of R_1 and R_2 , and a common-mode error signal results at the circuit output. A similar error develops with application of Fig 2's external phase compensation.

For differential-input op-amp connections, any external phase compensation added should be of the type illustrated in Fig 3 or Fig 4. With Fig 3's method, the compensation elements are in series with the amplifier output and do not support a common-mode swing. With Fig 4's method, demonstrated by the circuit in Fig 6, the only signal across R_C and C_C is the differential error signal between the op-amp inputs. This error signal contains a component of common-mode error but is small compared to the actual common-mode signal.

The resulting signal current in R_C and C_C degrades common-mode rejection, but far less than the compensation methods in Figs 2 and 5. Selection of the R_C and C_C values in Fig 6 follows directly from the discussion of Fig 4. Fig 6 also includes R_3 and R_4 , which are not present in Fig 4, but these resistors do not alter the feedback factor. The phase-compensation effects are the same for the two circuits.

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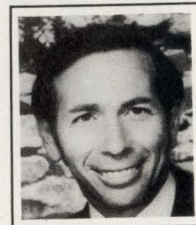
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Author's biography

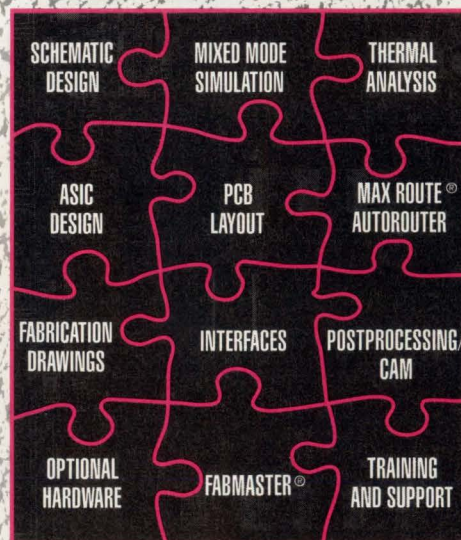
Jerald Graeme is the manager of instrumentation components design at Burr-Brown and has been with the company for 25 years. During that time, he has developed numerous linear circuits, including op amps, instrumentation amplifiers, analog multiplexers, V/F converters, and D/A converters.

Jerry has a BSEE from the University of Arizona and a MSEE from Stanford University. Leisure-time activities include scuba diving, photography, and woodworking.

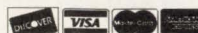


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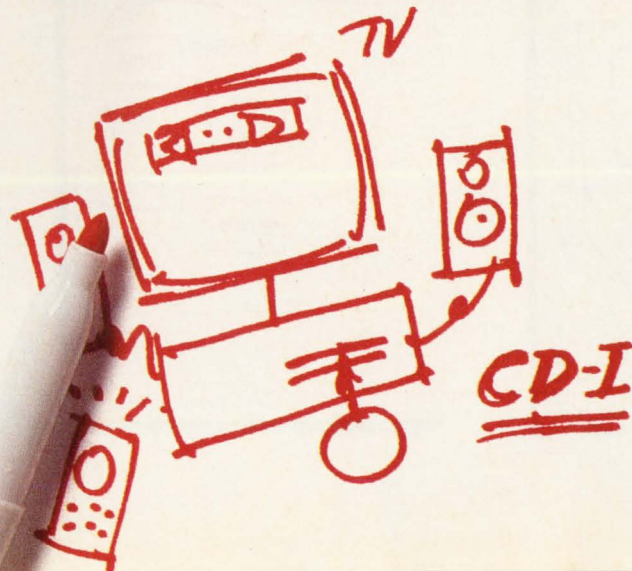
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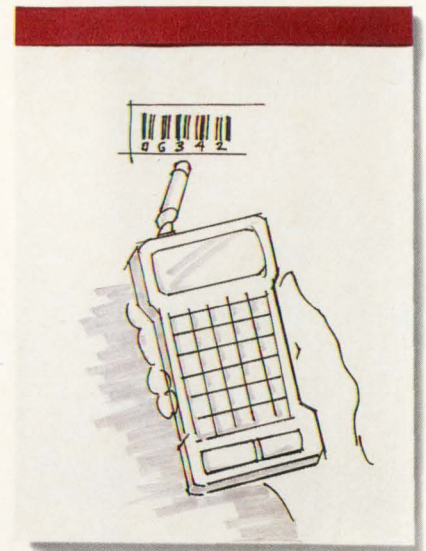
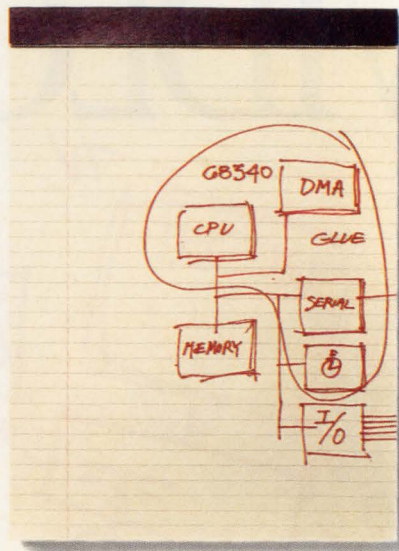
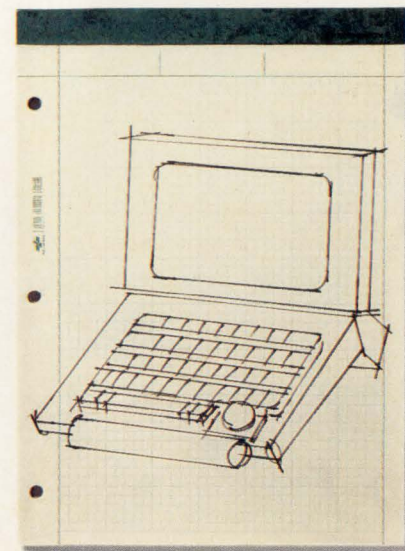
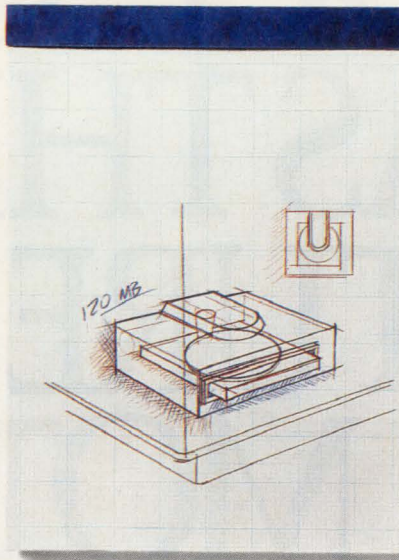
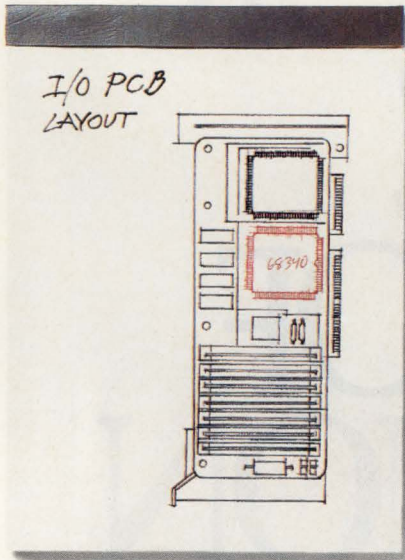
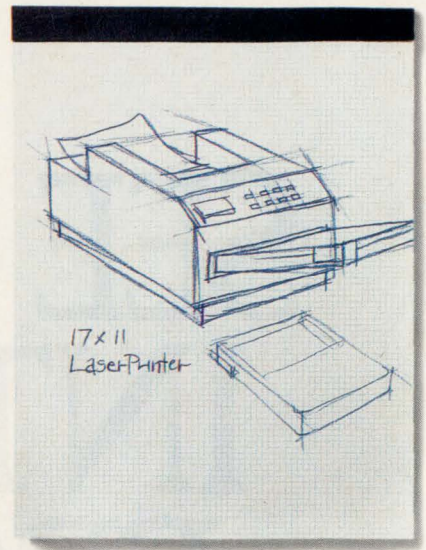
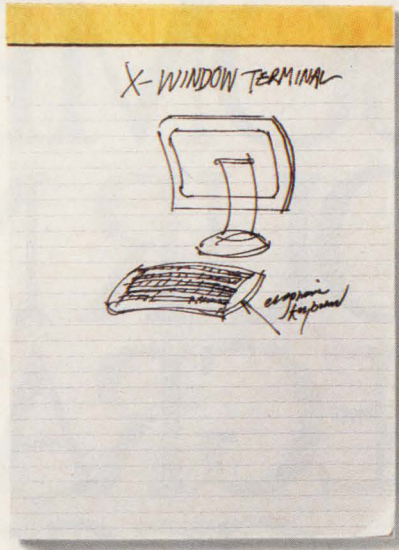
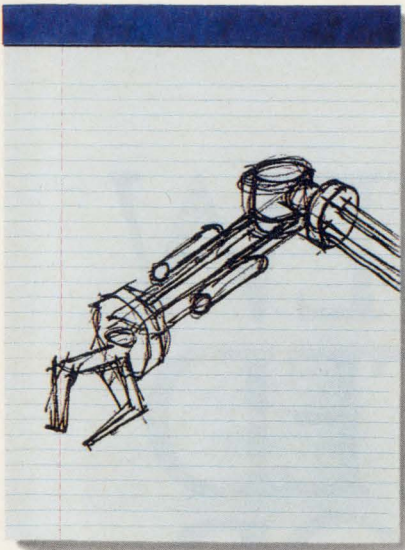


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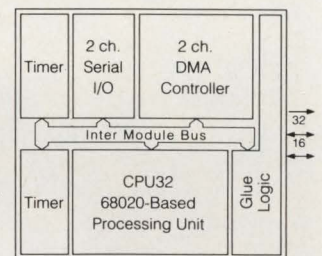
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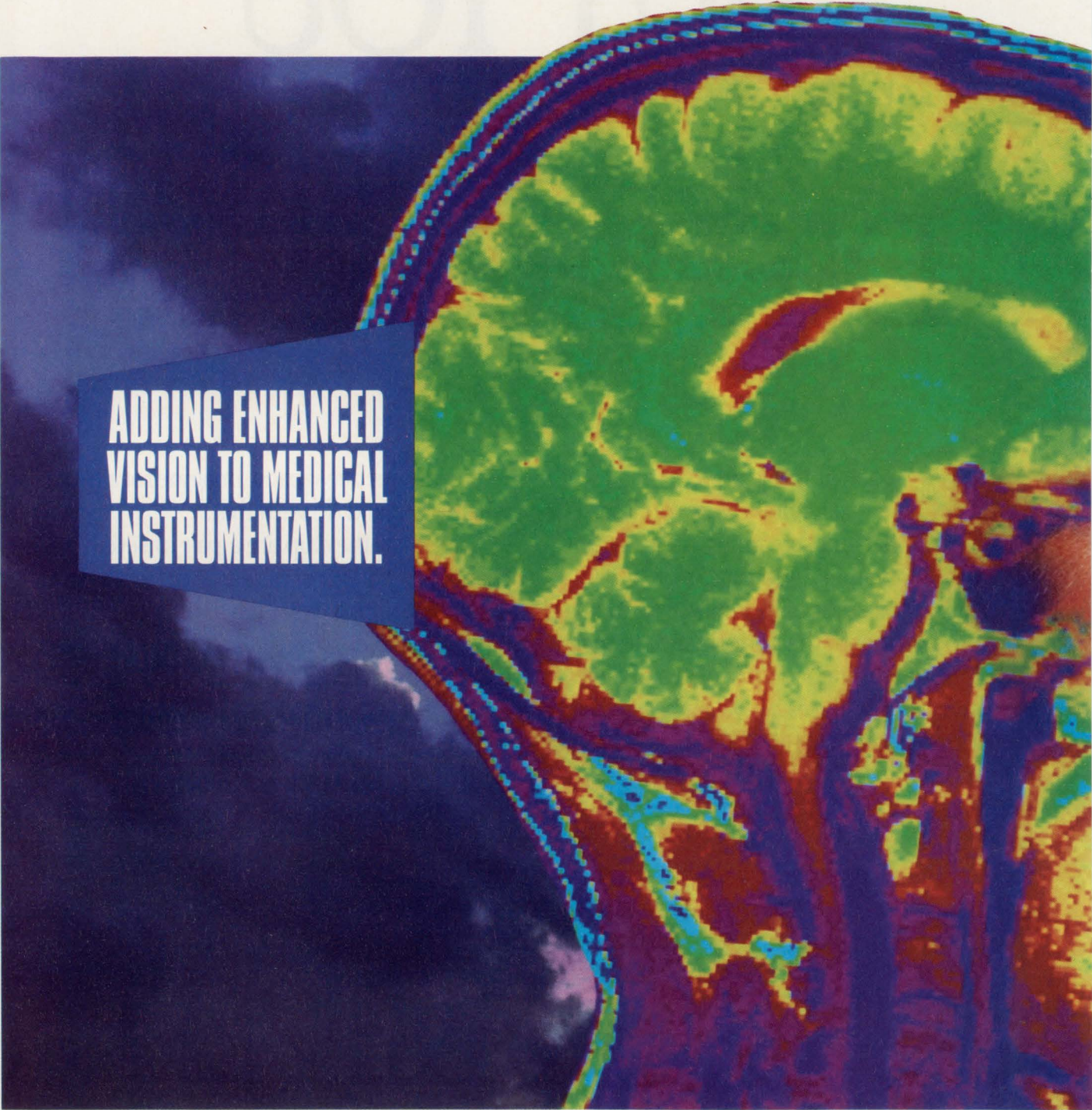


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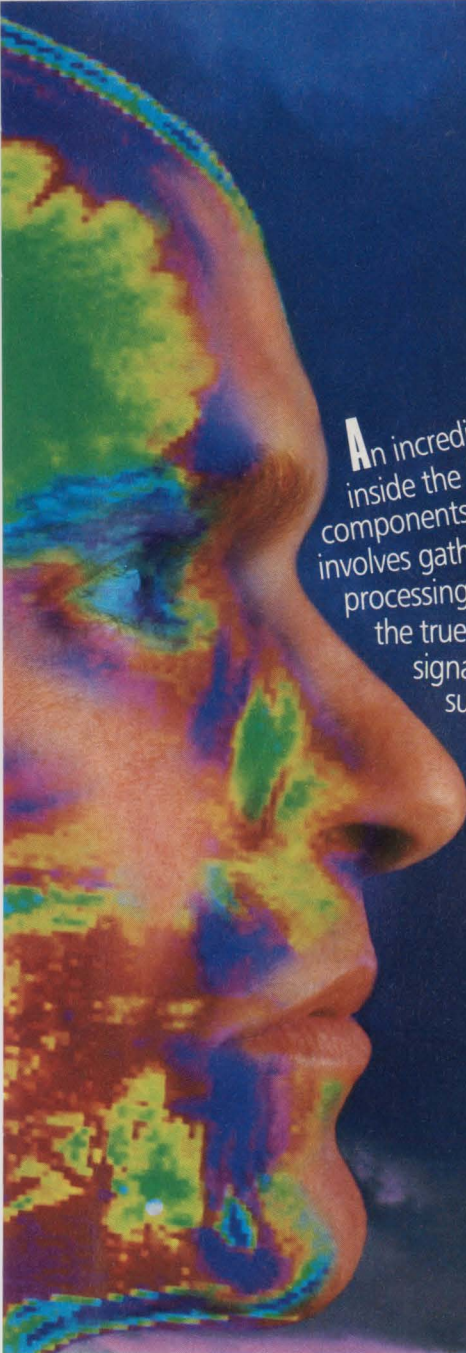
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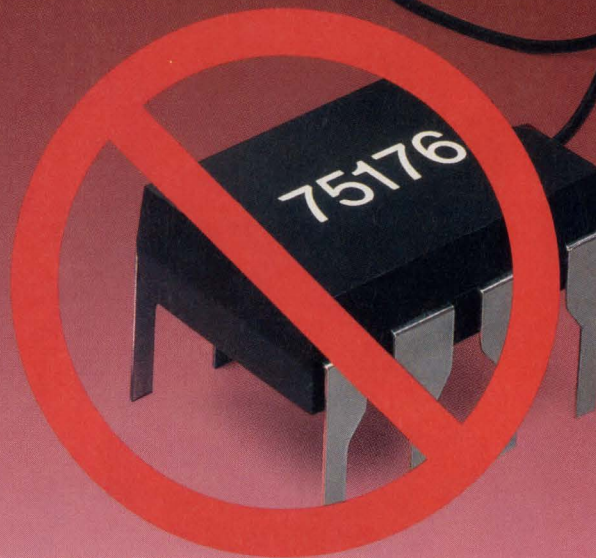
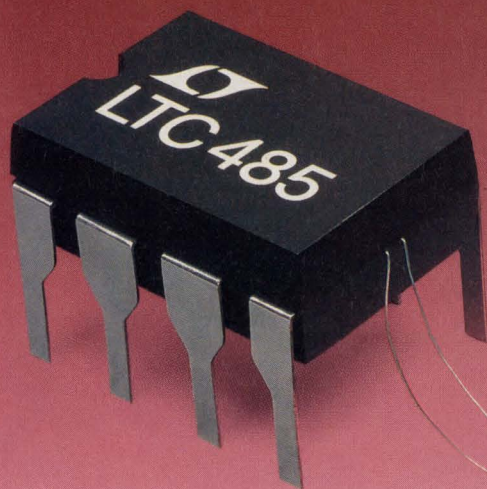
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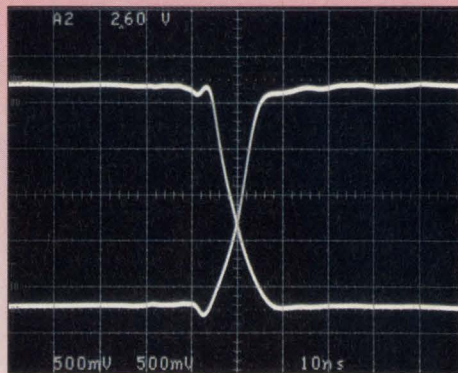
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EDITED BY CHARLES H SMALL

Programmable oscillator runs without μP

Jon Klein
Micro Linear, San Jose, CA

The circuit in Fig 1, using a clever scheme adaptable to other programmable devices, allows you to operate the ML2035 programmable sine-wave generator, IC₃, without a controlling μP . IC₁, a 74HC4060 counter, provides both the sine-wave generator's clock as well as a gating pulse to shift register IC₂. When IC₁'s pin 5, Q₅, goes high, IC₂ begins shifting eight hard-wired bits into the sine-wave generator to program it. After IC₂ shifts the 8 bits, Q₅ goes low, enabling normal operation. The circuit can produce both 50- and 60-Hz outputs from a NTSC color-burst crystal (3.579545 MHz). Table 1 lists binary codes for other crystal frequencies. The sine-wave generator's output exhibits a maximum of 0.5% THD. EDN BBS /DL_SIG #1019

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Table 1—Shift register values and frequency errors for standard crystal values

f _{CRYSTAL} (MHz)	f _{OUT}	D ₁₀	D _{HEX}	74HC165 Code		Error
				ABCD	EFGH	
4.00	50	105	69	1001	0110	0.14%
4.00	60	126	7E	1000	0001	0.14%
4.194304	50	100	64	1001	1011	0.00%
4.194304	60	120	78	1000	0111	0.00%
6.00	50	70	46	1011	1001	0.14%
6.00	60	84	54	1010	1011	0.14%
8.00	50	52	34	1100	1011	-0.82%
8.00	60	63	3F	1100	0000	0.14%

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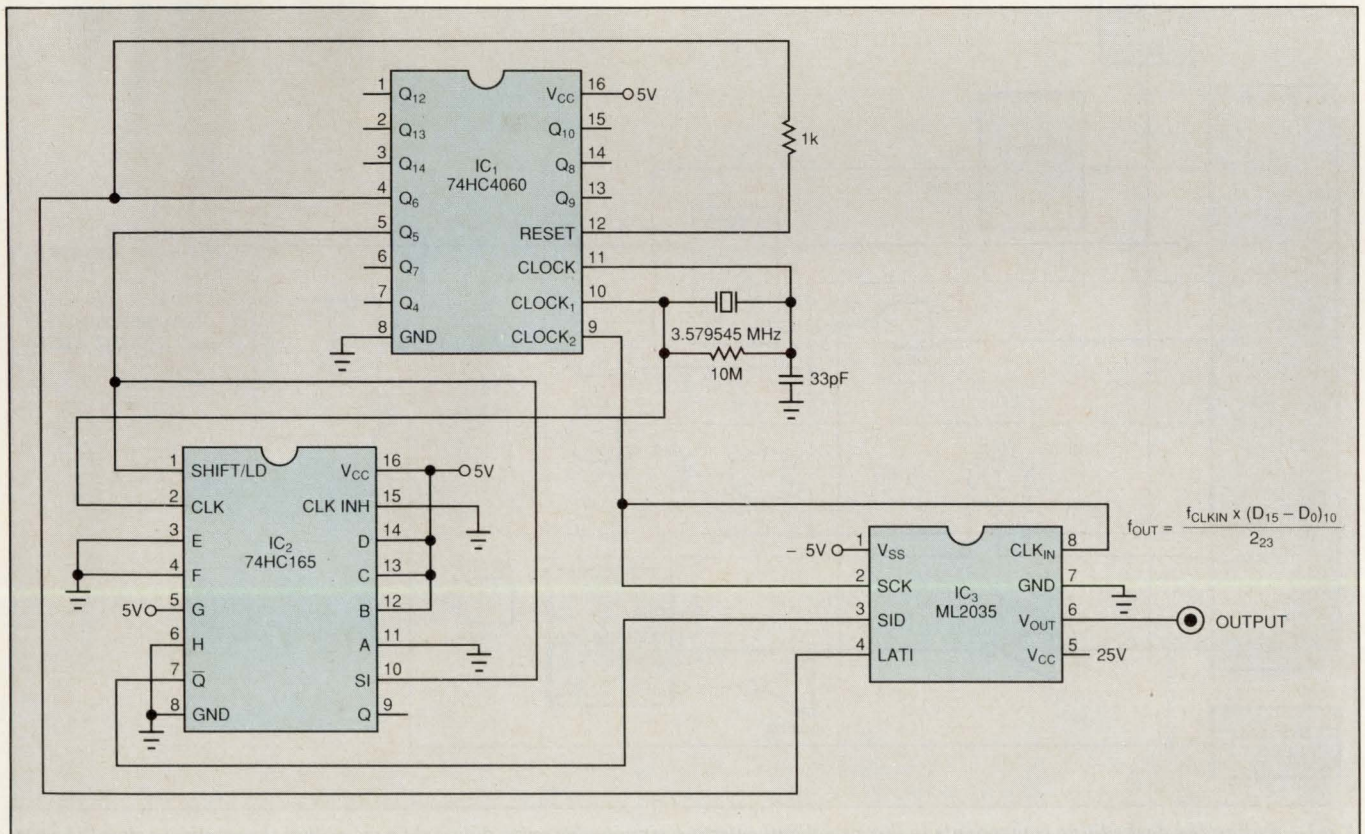


Fig 1—Counter IC₁ first clocks in an 8-bit programming code via shift register IC₂, subsequently clocking sine-wave generator IC₃.

Slow peripherals interface to fast 68000s

Don Atkins
Motorola, Austin, TX

If you plan to interface slow peripherals to 68000-family μ Ps, you may have to lengthen the μ P's data-hold time during write operations. At faster frequencies, the M68000 family shortens the Address Strobe-Data Strobe (AS-DS) to data-invalid time (ie, the data-hold time) because the clock cycle is shorter. If data from the μ P is buffered and the DS signal qualifies the chip-select signal to the peripheral, then worst-case propagation delays may violate the data-hold-time specification of the peripheral. Even fast peripheral devices may be at risk if the propagation-delay skews through the data buffer and the chip-select qualifier is large enough.

Fig 1 shows a sample circuit where the μ P interfaces to a write-only hardware register (IC₃), a 74LS273 octal D-type flip-flop. Decoded address lines generate

a chip-select (\overline{CS}) signal for IC₃, qualified by both the read/write (R/W) and data strobe (\overline{DS}) signals.

The \overline{AS} signal qualifies the \overline{IOSEL} signal from the address-decode block, connecting to both the 74F245 (IC₁) and the 74F164 (IC₂). The 74F245 bidirectional data buffer allows the μ P to read and write 8-bit peripheral devices. The 74F164 shift register generate the $\overline{DSACK0}$ signal, which terminates the bus cycle.

During write operations, the μ P transmits data and clocks them into IC₃ on the negative edge of the \overline{DS} signal. The problem with this circuit is that without the components shown connected by dashed lines (and \overline{DS} hooked directly to the third 74F32), the design violates IC₃'s 5-nsec data-hold time. Calculations show that the hardware provides 0.9 nsec of data-hold time, whereas the 74LS273 requires 5 nsec. An easy fix to this problem would be to substitute a faster D-type flip-flop that requires 0 nsec of data-hold time. This quick fix only provides 0.9 nsec of safety for data-hold

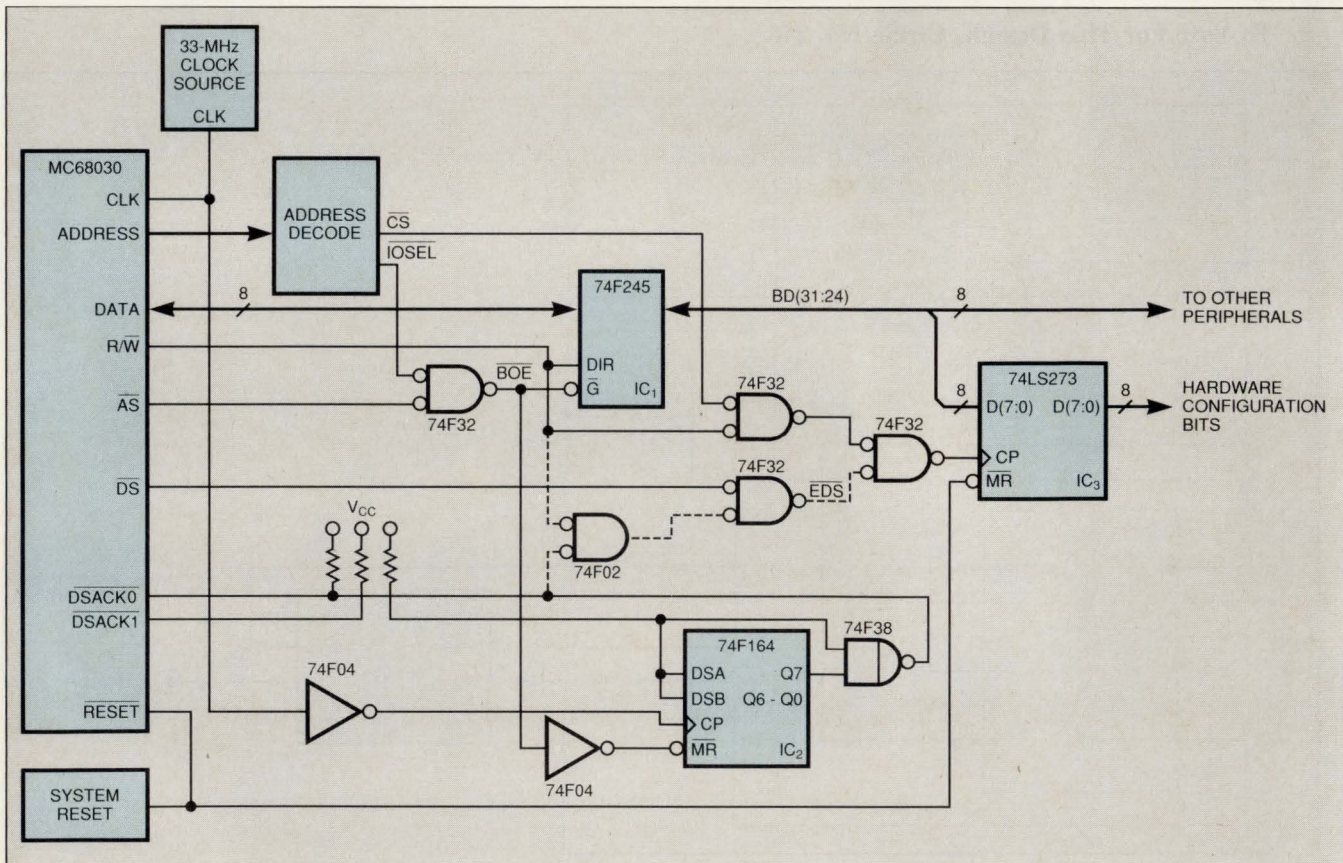
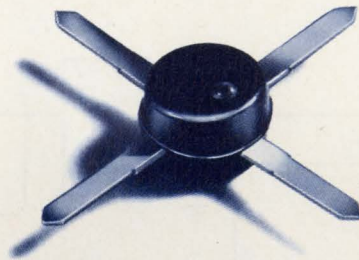


Fig 1—Adding the dashed-line components to this peripheral-interface circuit adds extra data-hold time so that the relatively slow 74LS273 (IC₃) can work with the fast μ P.

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SPECIFICATIONS

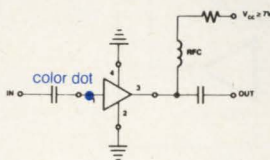
MODEL	FREQ. MHz	GAIN, dB			Min. MHz	• MAX. PWR. dBm	NF dB	PRICE \$ Ea.	Qty.
		100 MHz	1000 MHz	2000 MHz					
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.

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80 x 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 x 60	10%	X7R	.022, .047, .068, .1µf

† Minimum Order 50 per Value
• Designers kit, kcap-150 pieces of each capacitor value, only \$99.95

DESIGN IDEAS

time and limits the design to a maximum of 33 MHz.

The components connected by dashed lines generate an early data-strobe signal (EDS) to provide longer data-hold times. The $\overline{\text{EDS}}$ signal asserts when $\overline{\text{DS}}$ asserts. The $\overline{\text{EDS}}$ signal then negates during write cycles when the $\overline{\text{DSACKx}}$ signal asserts. This action creates an extra clock cycle of data-hold time. At 33 MHz, the data-hold time increases to 35 nsec.

If you need longer data-hold times, you can use IC_2 to negate the $\overline{\text{EDS}}$ signal sooner. Each successively lower-numbered output pin you choose to connect on IC_2 retards the $\overline{\text{EDS}}$ signal and increases the data-hold time by one clock period.

Peripherals like the MC68681 Dual Asynchronous Receiver/Transmitter (DUART) and the MC68901 Multi Function Peripheral generate their own data-acknowledge ($\overline{\text{DTACK}}$) signal. Fig 2 shows how to interface an MC68681 DUART (IC_3) to increase the data-hold time from the μP . In this case, an Early-Address Strobe (EAS) qualifies the memory-mapped chip select ($\overline{\text{CS}}$) signal through a 74F32 2-input OR gate. The output of the 74F32, $\overline{\text{DUARTCS}}$, then connects to the $\overline{\text{CS}}$ input of IC_3 . Like the $\overline{\text{EDS}}$ signal, the

$\overline{\text{EAS}}$ signal asserts with the μP 's $\overline{\text{AS}}$ and negates during write cycles based on one of the outputs of the 74F164 shift register (IC_2). The $\overline{\text{AS}}$ signal qualifies the memory-mapped $\overline{\text{IOSEL}}$ signal from the address decode block to generate the Buffered-Output Enable ($\overline{\text{BOE}}$) signal used to enable the 74F245 data transmitter (IC_1) and to release IC_2 .

The final major difference between Fig 1's circuit and Fig 2's is a third memory-mapped signal $\overline{\text{DTACKEN}}$ from the address-decode block. The $\overline{\text{DTACKEN}}$ signal asserts whenever a peripheral that generates its own acknowledge signal is selected. This action prevents IC_2 from terminating the access until IC_3 asserts the $\overline{\text{DTACK}}$ signal. If the μP selects a peripheral that does not generate its own $\overline{\text{DTACK}}$ signal, then the $\overline{\text{DTACKEN}}$ signal does not assert. This sequence allows IC_2 to start shifting data immediately and terminate the access by asserting the $\overline{\text{DSACK0}}$ signal. EDN BBS /DL_SIG #1021 **EDN**

To Vote For This Design, Circle No. 747

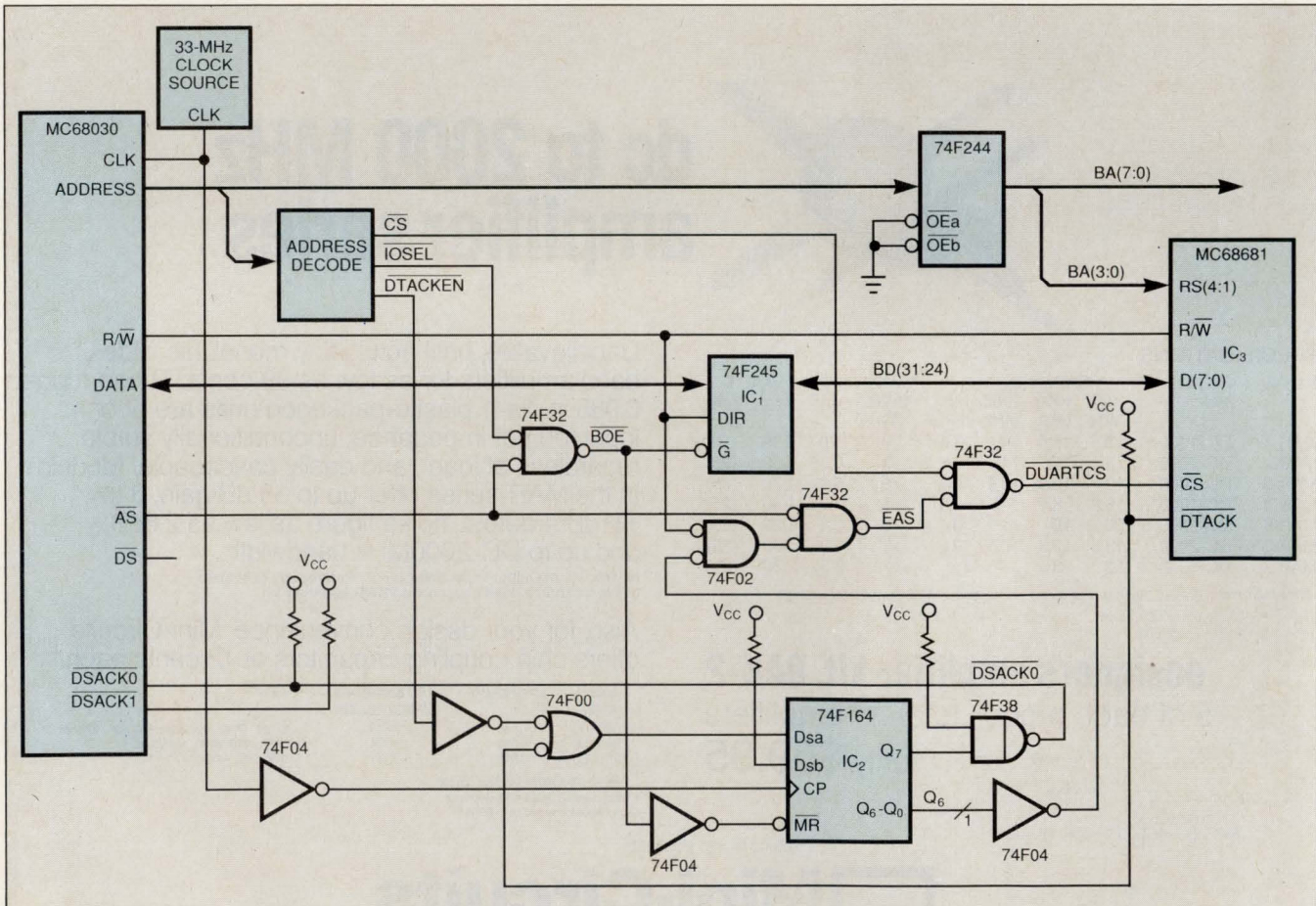
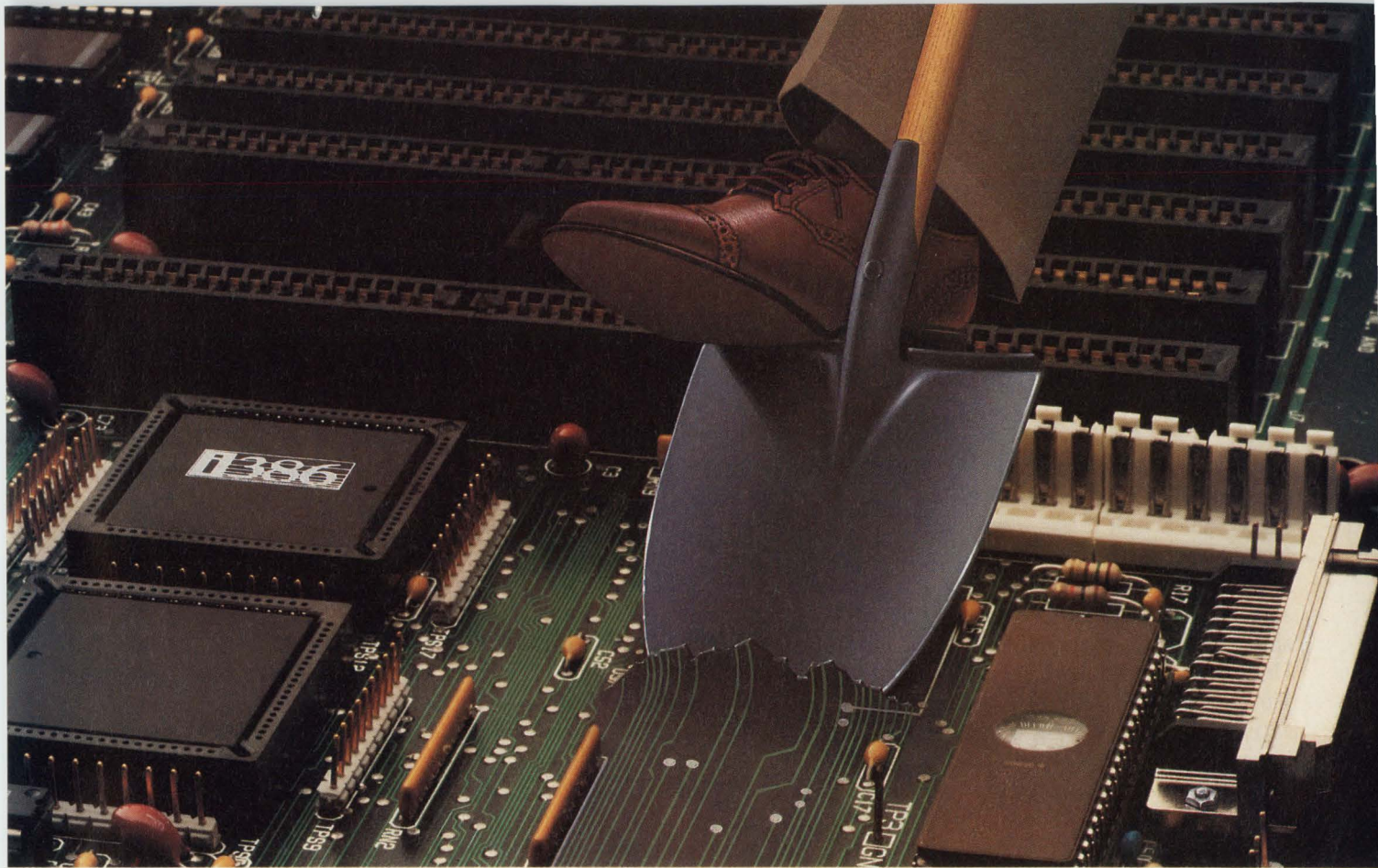


Fig 2—Similarly to Fig 1, this peripheral-interface circuit allows slower peripherals that develop their own acknowledge signal to interface to fast μP s.



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Relay has electrically resettable fuse

Sam Ochi
IXYS Corp, San Jose, CA

Fig 1 shows an intelligent, fully isolated, solid-state ac relay, having a resettable 10A electronic fuse. The relay can switch 6 kW (600V ac at 10A). A 5V signal from either a system controller or a manual switch applied to V_{IN} turns the relay on. Within 1 μ sec of sensing a short circuit or an overload, the relay will shut itself off, turn on LED D_1 , and set flag FLT. Under system control, this solid-state relay can complete an on/off cycle in less than 1 μ sec at repetition rates as high as 50 kHz. Such cycling proves useful for starting highly inductive loads.

A 5V signal applied to V_{IN} enables IC_1 , a PWM single-phase, dc-motor controller, to turn on the relay. Pushing switch S_1 or energizing the \overline{RST} line resets the relay. IC_1 drives terminals 3 and 4 of the primary

of transformer T_2 , a communications transformer, through C_1 and R_1 . T_2 's secondary, terminals 5 and 6, energizes motor controller IC_2 . C_2 , C_3 , and R_2 serve to filter any high dV/dt common-mode noise present between the ac power line and IC_1 's ground.

IC_2 converts its received differential signal to a full V_{EE} -to- V_{DD} swing (pin 15). The pin-15 signal drives the series-connected NMOS power transistors, Q_1 and Q_2 , via gate resistors R_3 and R_4 . V_{DD} , which is typically 15V with respect to the sources of Q_1 and Q_2 , is more than enough to turn them on. Conversely, V_{EE} , which is typically -5V, provides a noise margin of 5V to hold the power NMOS devices off in very-high-noise environments.

Once Q_1 and Q_2 are on, IC_2 uses R_5 and R_6 to sense the currents flowing through Q_1 and Q_2 . During the positive half cycle of the input-ac waveform, Q_2 acts as the main switching device, and Q_1 's internal drain-to-

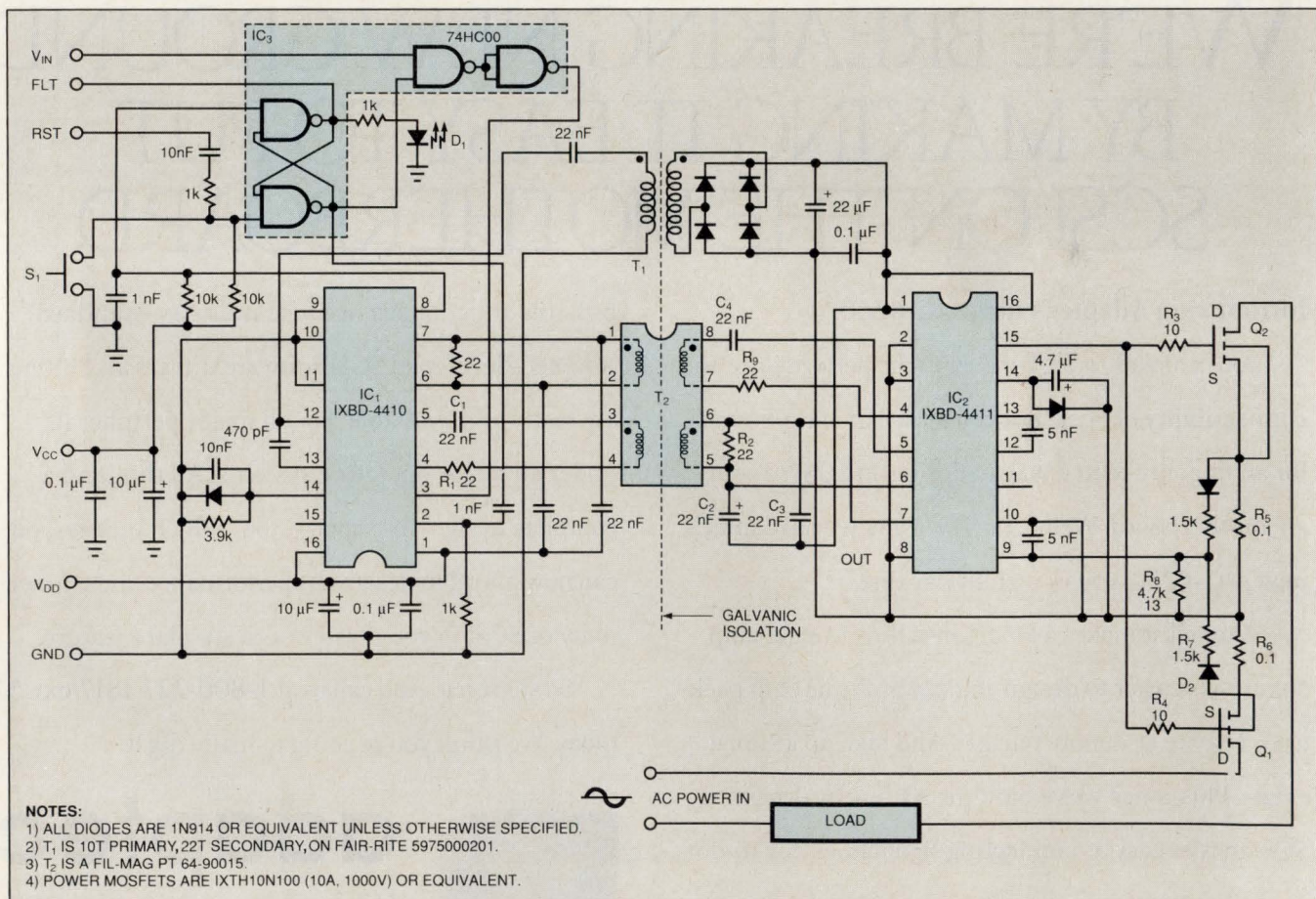
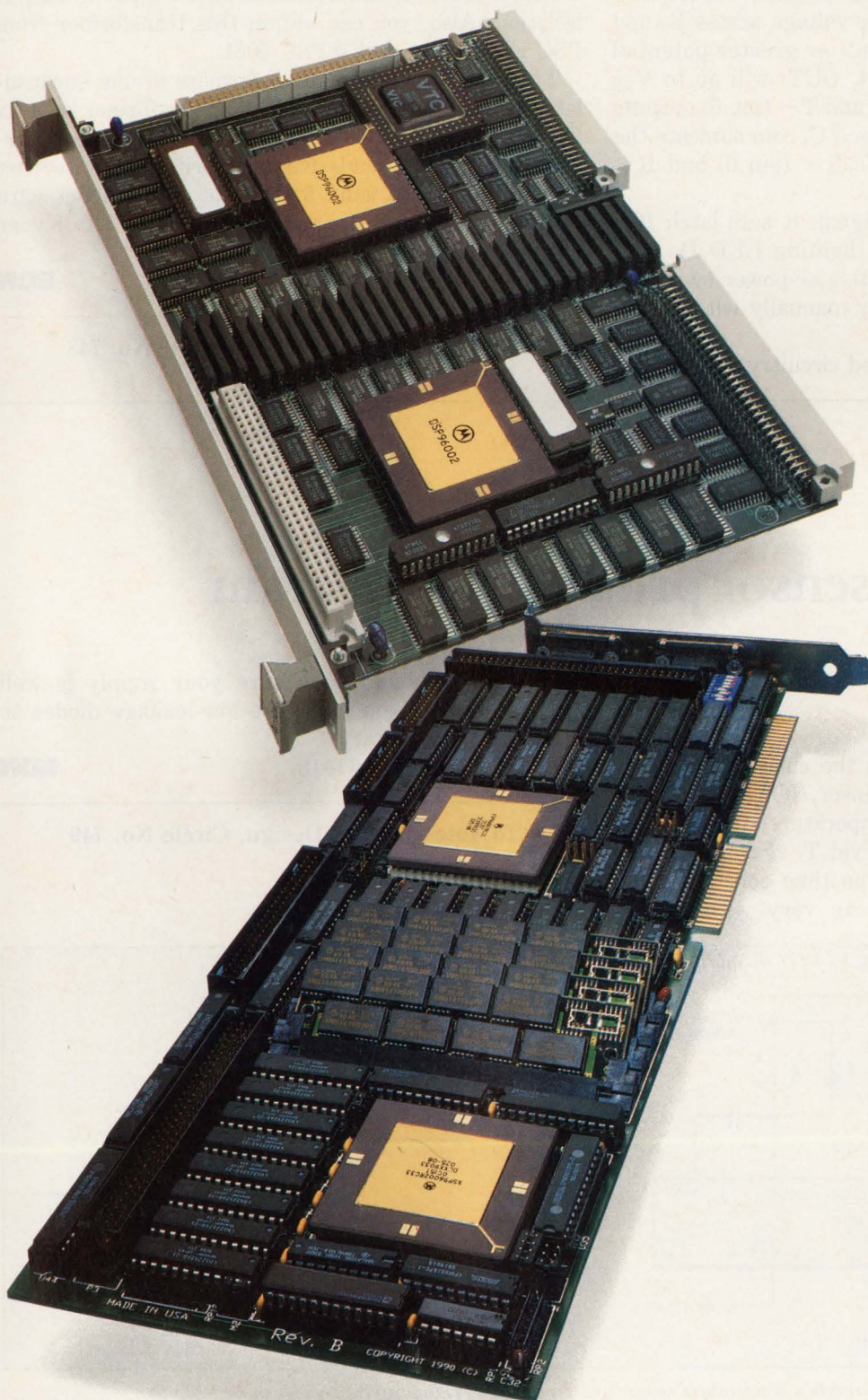


Fig 1— This intelligent, fully isolated, solid-state ac relay has a resettable 10A electronic fuse and can switch 6 kW.

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DESIGN IDEAS

source diode conducts. The voltage across the current-sense resistor (R_6) is positive with respect to the floating common ground point, FGND, the intersection of R_5 and R_6 .

When more than 10A flows through Q_1 and Q_2 , a positive 1V or more appears across R_6 that will forward bias D_2 and drop the remaining voltage across R_7 and R_8 . About 200 nsec after 300 mV or greater potential appears across R_8 , IC_2 's output, OUT, will go to V_{EE} from V_{DD} , and IC_2 's T+ (pin 5) and T- (pin 6) outputs will transmit a fault signal. R_9 and C_4 communicate the fault signal through T_2 to IC_1 's R- (pin 6) and R+ (pin 7).

When IC_1 receives a fault signal, it sets latch IC_3 , disabling the relay's input and lighting LED D_1 . The circuit's operation during negative ac-power swings is similar. You can reset the relay manually with switch S_1 or via input \overline{RST} .

Transformer T_1 and associated circuitry provide the

fully floating V_{DD} power for IC_2 . IC_1 's charge-pump clock drives power-transfer transformer T_1 . T_1 is a ferrite toroid (Fair-rite part #5975000201) transformer that is segment wound using 10 turns of #30 Kynar for the primary and 22 turns of #30 Kynar for the secondary. This transformer has 2500V input-to-output isolation. Also, you can obtain this transformer from PSC Electronics part #PSC-5061.

T_2 is two ferrite-bead transformers in one encapsulated 8-pin DIP. One source of this transformer is Delta Electronics part #BD4414/15. Of course, you can purchase the ferrite beads from Fair-rite (Fair-rite part #2664000101) and wind 6 turns of #36 magnet wire for the primary and two turns of #30 wire with Kynar insulation for the secondary.

EDN BBS /DL_SIG #1020

EDN

To Vote For This Design, Circle No. 748

Temperature sensor produces pulse train

Jhoti Vandana

SEMP, Kalpakkam, India

The circuit in Fig 1a converts the current output of the AD590/592 temperature sensor, IC_1 , into a pulse train. The sensor measures temperatures from -55°C to $+150^\circ\text{C}$. The width of interval T_1 (Fig 1b) varies inversely with temperature. The time constant R_1C_1 sets interval T_2 . Because T_2 can vary with power-

supply fluctuations, make sure your supply is well regulated. Also, you must use low-leakage diodes to preserve IC_2 's accuracy.

EDN BBS /DL_SIG #1018

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To Vote For This Design, Circle No. 749

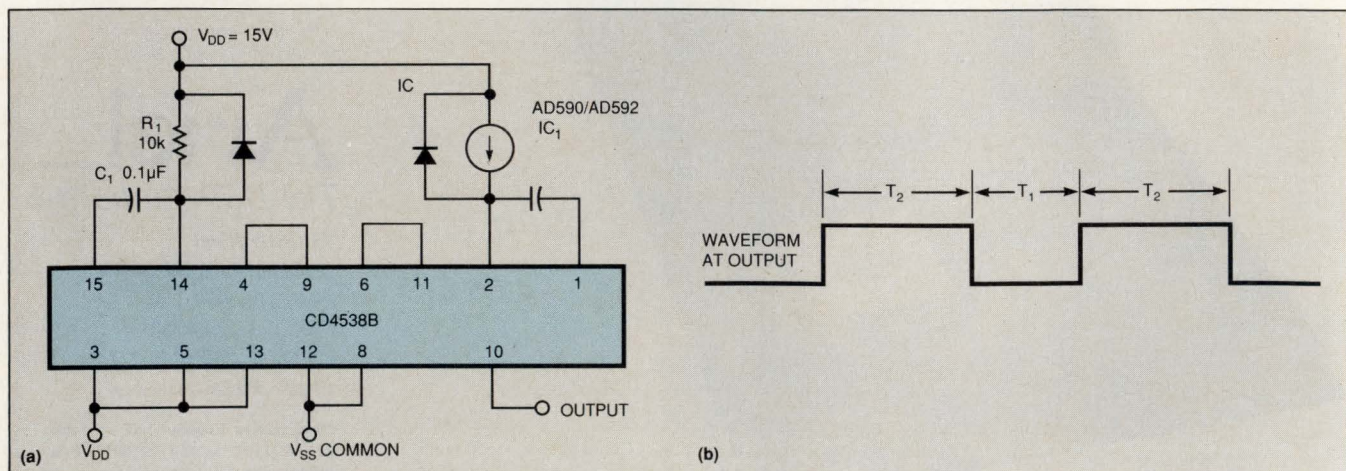
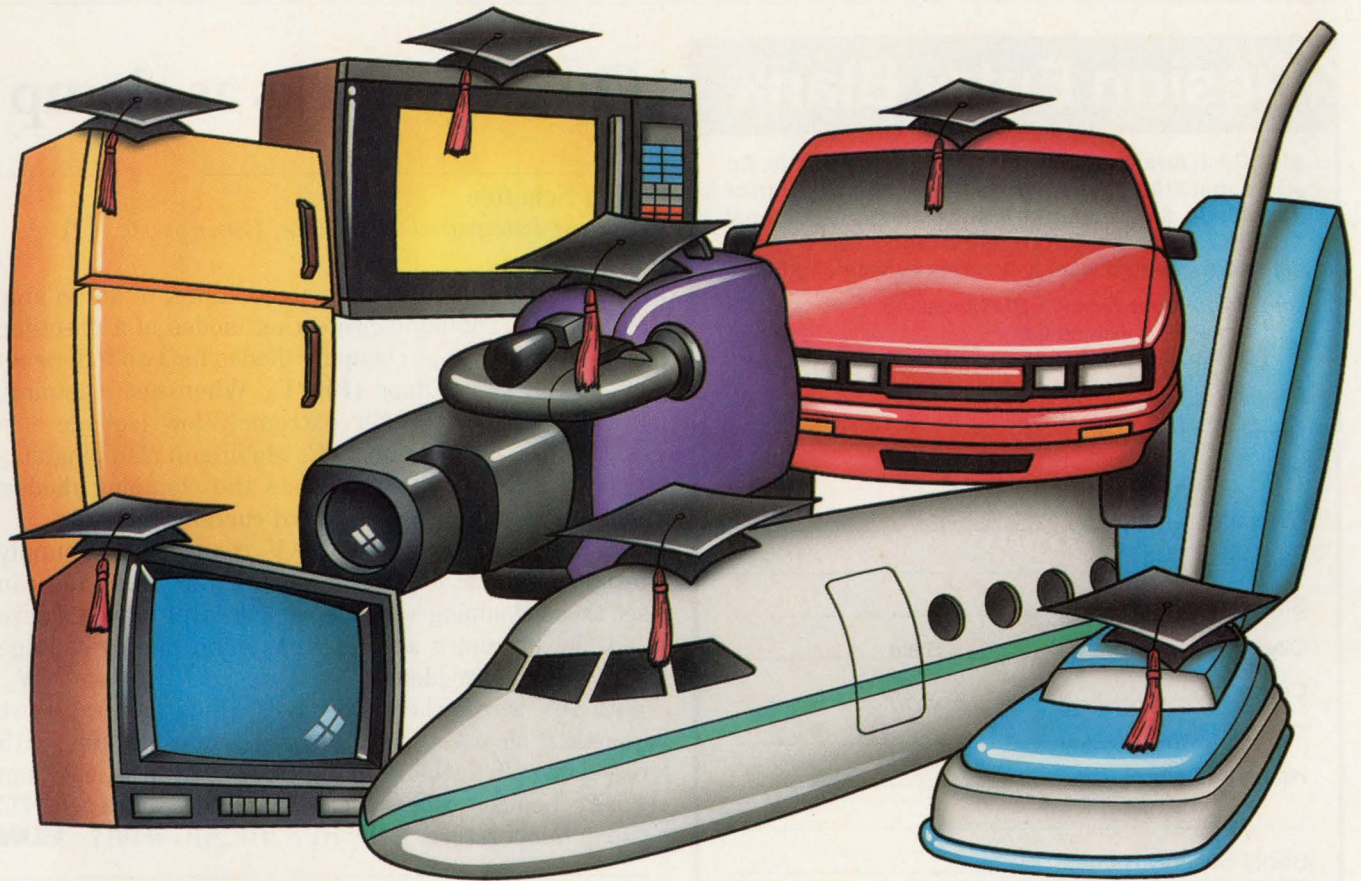


Fig 1—A simple dual multivibrator converts a temperature sensor's current output (a) to a variable-width pulse train (b).



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Op amp works as clamp

Greg Schaffer

Maxim Integrated Products, Sunnyvale, CA

Forget about amplifying. Instead, think of an op amp as a clamp. The input-protection diodes of a precision op amp can serve as clamping diodes for two independent analog-signal lines (Fig 1). When not clamping, the device's diodes offer extremely low leakage currents of 50 to 100 fA at 20°C. Maximum clamping current is ± 10 mA. Table 1 lists the clamping diodes' forward voltage versus forward current.

Clamping voltages V_1 and $-V_2$ connect to the supply terminals of the low-voltage CMOS op amp. You can set these clamping voltages at any level between zero and the op amp's absolute-maximum supply voltage (12V total), provided V_1 is more positive than $-V_2$. With 10V across the supply pins, the amplifier draws less than 50 μ A typ. If pin 3 remains positive with respect to pin 2, the typical supply current is less than 1 μ A. Leakage approximately doubles for each 8°C rise in temperature. EDN BBS/DL_SIG #1017 **EDN**

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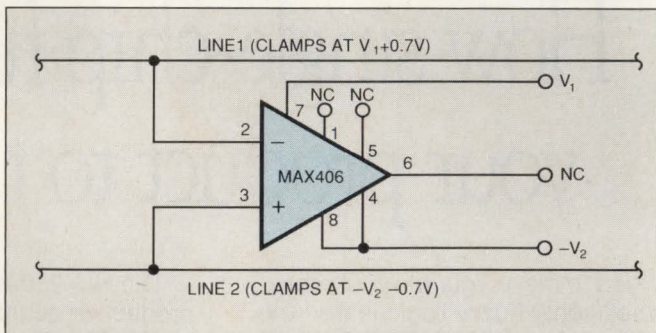


Fig 1—This circuit takes advantage of the low-leakage input diodes of a precision CMOS op amp, using them to clamp two analog-signal lines.

Table 1—Diode forward voltage vs current

Positive (V_1)		Negative ($-V_2$)	
Diode current (mA)	Diode voltage (V)	Diode current (mA)	Diode voltage (V)
0.01	0.635	-0.01	-0.608
0.10	0.714	-0.10	-0.670
1.00	0.822	-1.00	-0.751
2.00	0.861	-2.00	-0.787
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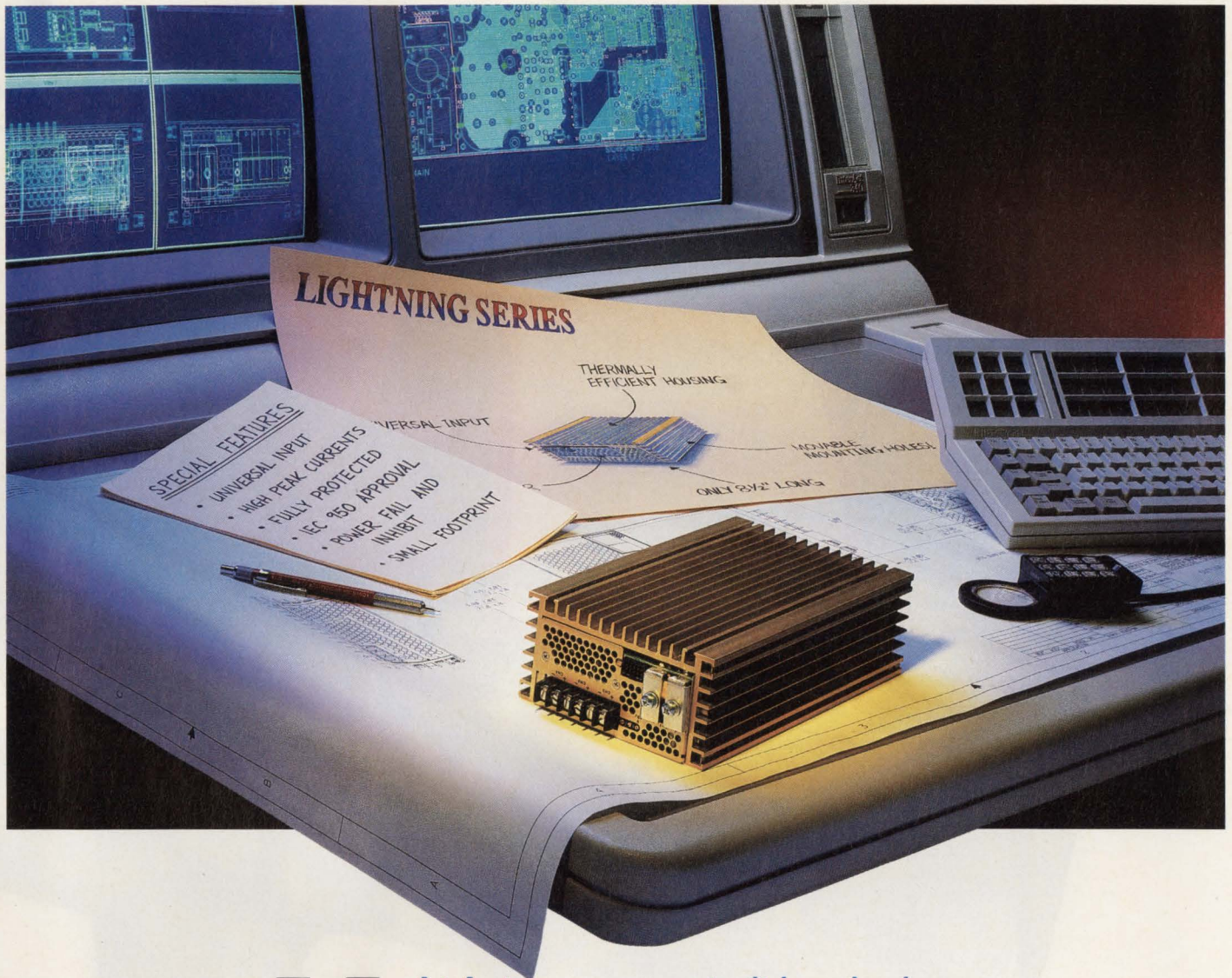
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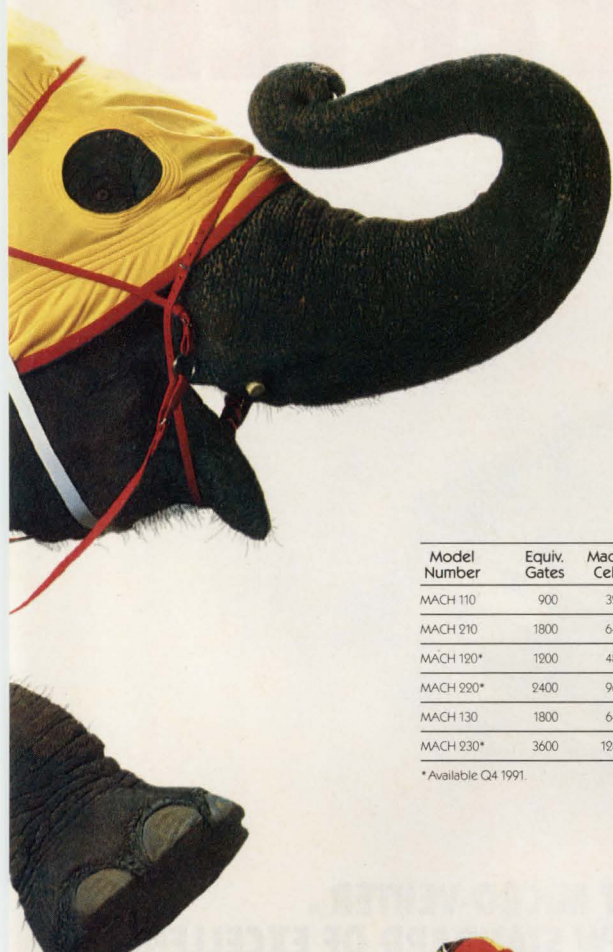
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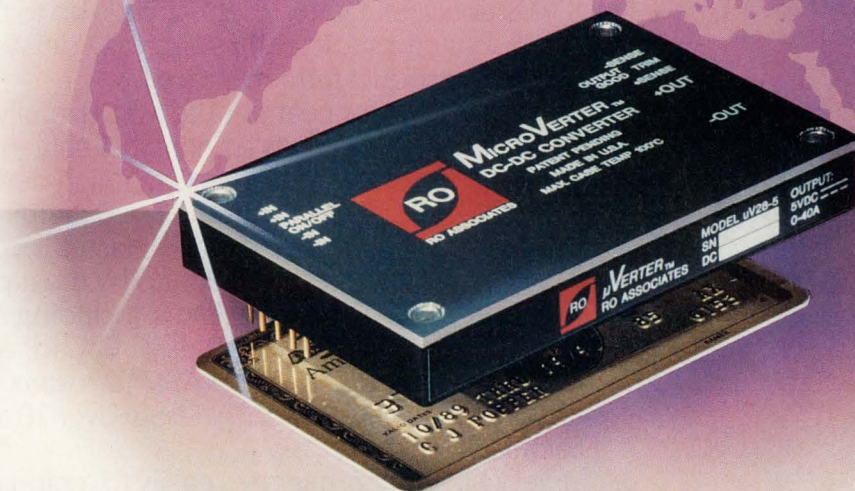


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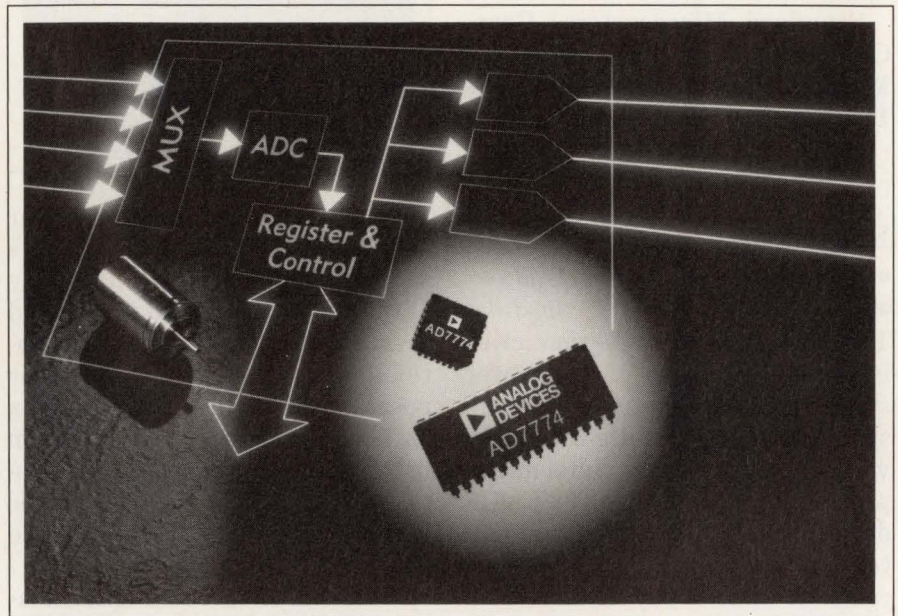
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- Combines A/D and D/A conversion
- Has adjustable operating parameters

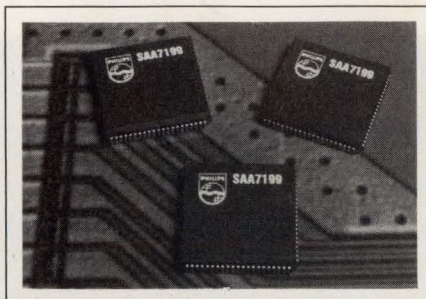
The AD7774 multichannel I/O device is specifically designed for closed-loop motion control and servo systems. The device includes a 4-channel, 8-bit A/D converter (sharing two track/hold amplifiers), two 8-bit and one 11-bit D/A converters, analog output amplifiers, an internal reference, and a microprocessor interface. The I/O device allows either independent or simultaneous sampling of inputs. Three key operating parameters are independently adjustable: the mid-point of the ADC's transfer function (bias), the input voltage swing of the ADC (span), and the mid-point output voltage of the DAC (bias). By adjusting these biases and the span, you can optimize the perform-



ance of the converters—especially in applications where only a positive supply rail is available—by referencing the input and output voltages to a point other than analog ground. The AD7774 operates from

5 and 12V supplies. In 28-pin DIP and plastic-leaded-chip-carrier packages, from \$18 (1000).

Analog Devices, 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. **Circle No. 380**



Encoder For TV And VCR Computer Graphics

- Accepts seven digital formats
- Generates NTSC or PAL analog signals

The SAA7199 digital video encoder enables high-quality computer graphics and digital video to be displayed on TV monitors or stored on video tape. The encoder allows personal computers and workstations to perform the same display, editing, titling, and special-effects functions that normally require ex-

pensive analog editing boards and systems. The encoder accepts seven different digital formats including CCIR601 (a common digital data structure for NTSC, PAL and SECAM) or computer graphics such as 24-bit RGB or 8-bit VGA. The encoder generates analog output signals in both NTSC and PAL formats. Three user-selectable modes are available. In the master mode, the SAA7199 accepts timing information from the graphics system; in the stand-alone mode, it generates graphics timing signals based on a provided video clock; in the genlock mode, it locks to an analog video signal and generates all graphics timing signals. The genlock mode allows graphics overlay on any video source. \$47 (100).

Signetics Co., Box 3409, Sunnyvale, CA 94088. Phone (408) 991-4577. **Circle No. 381**

Floppy-Disk Controller

- Supports 4-Mbyte drives
- Pin-compatible with standard devices

The FDC37C65C+ floppy-disk controller supports all drive formats including 360-kbyte, 1.2-Mbyte, and the new 4-Mbyte format used in "super-floppy" drives. The C+ controller offers the same features as the industry-standard FDC37C65C floppy-disk controller, with additional support for 4-Mbyte floppy disks. The + designation represents the addition of a 16-byte FIFO and a vertical recording format. The pinout remains the same, which significantly reduces development time and expense when replacing the earlier device. The support for vertical-format drives is enabled by addressing the mode-control register. The FDC37C65C+ controller operates from a

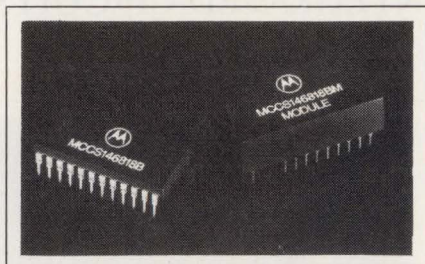
single 5V supply and is 100% compatible with IBM software. \$6.31 (50,000).

Standard Microsystems Corp,
Component Products Div, 35
Marcus Blvd, Hauppauge, NY
11788. Phone (516) 273-3100.

Circle No. 382

Real-Time Clock

- *Includes on-chip static RAM*
 - *Available as a complete module*
- The MCCS146818B real-time clock includes 128 bytes of low-power static RAM and features a timing system that lets you use the device with either Motorola or Intel microprocessor timing cycles. The CMOS device includes all the common battery-backup functions, such as a complete time-of-day clock with a 12- or 24-hour mode, a daylight-savings-time option, an alarm with a programmable interrupt, and a



100-year calendar with leap-year compensation. The device counts seconds, minutes, hours, days, day of the week, date of the month, and year. A module version, which interfaces with 1-MHz processor buses, includes the CMOS clock, a 32.768-kHz crystal, and a lithium battery. Clock chip, in a 24-pin plastic DIP, \$4.65; in a 28-pin plastic leaded chip carrier, \$5.03; complete 24-pin module, \$8.08.

Motorola Inc, MOS Digital-Analog IC Div, Box 6000, Austin, TX 78762. Phone (800) 521-6274.

Circle No. 383

64-Bit Microprocessor

- *Operates at 50 MHz*
- *Features 100-Mflops performance*

Designed for use in high-end computing systems, the 64-bit i860-XP microprocessor provides a peak performance rate of 100 Mflops at 50 MHz. Available in both 40- and 50-MHz versions, the CPU maintains full binary compatibility with the first-generation i860-XR. At 50 MHz, the i860-XP offers performance of 20 double-precision Linpack Mflops and can exceed 40 SPECmarks to meet the number-crunching computing needs of scientific and engineering applications. The CPU includes a RISC (reduced-instruction-set computer) integer unit, two pipelined floating-point units, a graphics unit, 16-kbyte instruction and data caches, and a memory-management unit. An on-chip bus unit supports pipelined

When considering DSP, take



burst transfers of 400 Mbps. Other features include bus-snooping hardware and a cache protocol that maintains cache consistency between multiple XP processors. The i860-XP comes in a 262-pin ceramic pin-grid array. 50- and 40-MHz versions, \$699 and \$560 (1000), respectively.

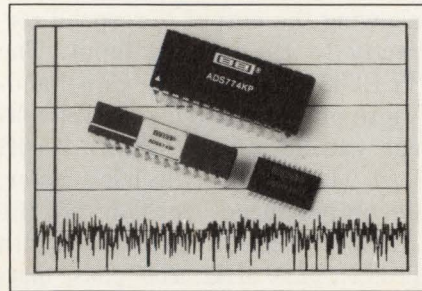
Intel Corp., Box 7641, Mount Prospect, IL 60056. Phone (800) 548-4725, or local office.

Circle No. 384

12-Bit A/D Converters

- Include S/H circuit
- Have 8.5- and 25- μ sec conversion times

Designed to plug into most ADC574 sockets without system modification, the ADS574 and ADS774 are 12-bit successive approximation A/D converters. Both devices feature an internal sample/hold circuit,



a 2.5V reference, a clock, a digital interface for microprocessor control, 3-state output drivers, and internal scaling resistors for input ranges of 0 to 10V, 0 to 20V, ± 5 V, or ± 10 V. For 12-bit conversion, the ADS574 and ADS774 have a maximum acquisition-and-conversion time of 25 and 8.5 μ sec, respectively. Both parts operate from a single 5V supply. Depending on the operating mode, a -12 or -15 V supply is optional, but a $+12$ or $+15$ V supply is not used. Other key specifications are $\pm 1/2$ -LSB integral

nonlinearity, $\pm 3/4$ -LSB differential nonlinearity, -77 -dB THD and 78-dB SFDR (spurious-free dynamic range). The ADS574 and ADS774 are available in 0.3- or 0.6-in.-wide, 28-pin plastic or side-brazed hermetic DIPs, and in 28-pin SOIC packages. From \$14.15 (100).

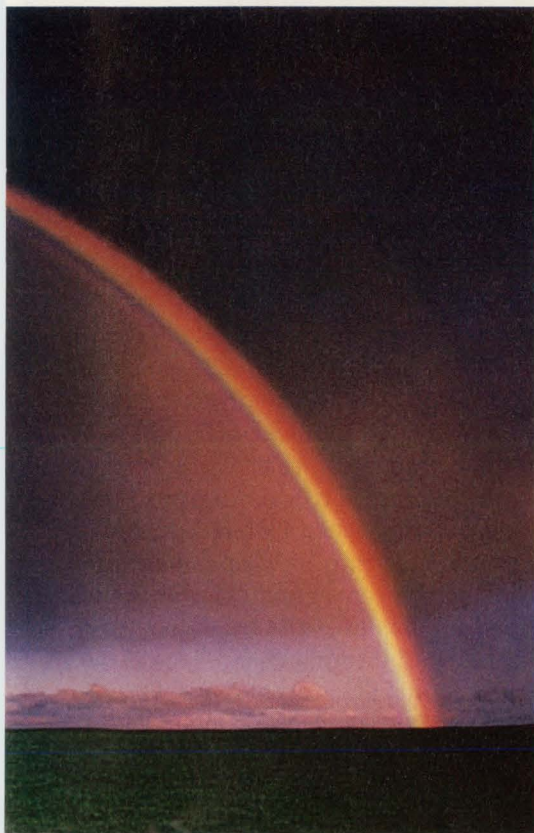
Burr-Brown Corp., Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111. Circle No. 385

Audio/Video Op Amps

- Have nonsaturating outputs
- Have gain-bandwidth products to 80 MHz

Designed for use in active filters, audio preamplifiers and baseband video applications, TLE2027 and TLE2037 op amps feature an output-saturation recovery circuit. This circuit prevents output saturation, eliminating recovery time and

a look at the full Spectrum.



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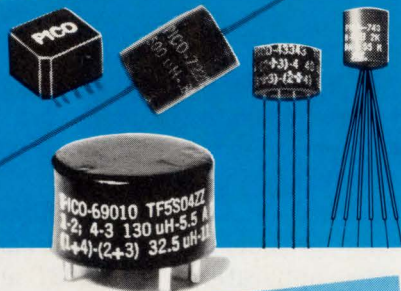
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INTEGRATED CIRCUITS

allowing the output to respond correctly to the applied input. The TLE2027 has a unity-gain bandwidth of 15 MHz and a typical voltage gain of 45V/ μ V with a 2000 Ω load. The TL2037, which is a faster, decompensated version of the TLE2027, has a gain-bandwidth product of 80 MHz, a 50° phase margin, and is stable at gains of five or greater. Package options include DIP, SO and metal can. In commercial plastic DIPs, \$1.19 (1000).

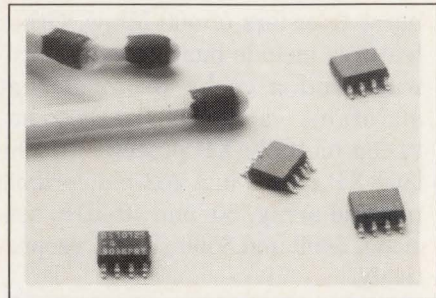
Texas Instruments Inc, Semiconductor Group (SC-91047), Box 809066, Dallas, TX 75380. Phone (800) 336-5236, ext 700; (214) 995-6611, ext 700. **Circle No. 386**

Power Converter/Regulator

- Generates \pm voltages locally
 - Operates over a 3.5 to 15V range
- For components such as op amps and comparators that need voltages unavailable from the system power supply, you can use the UC1054 to generate the required voltage locally. A charge-pump device, the UC1054 can generate or regulate positive and negative voltages between 3.5 and 15V, using any supply voltage in that range. The chip provides as much as 100 mA of output with a typical voltage loss of 1.1V over the full range. Typical circuit configurations include a voltage inverter, voltage regulator, and negative or positive voltage doubler. You can configure the device as a voltage regulator by placing a voltage divider between the output and the on-chip 2.5V reference pin. An oscillator pin lets you adjust the 25-kHz frequency of the internal oscillator or to synchronize it with another device. A shutdown feature reduces the quiescent supply current to 100 μ A. In 8-pin plastic and ceramic DIPs, from \$2.10 (1000).

Unitrode Integrated Circuits, 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410.

Circle No. 387



Silicon Delay Line

- Includes logic functions
- 6000 permutations are possible

Integrating logic and delay lines into a single chip, the DS1012 lets the designer choose from a variety of timing values and logic functions. More than 6000 permutations are possible. The device provides two inputs, each of which provides independent delays to a pair of outputs. Logic output options include AND, NAND, OR, NOR, XOR, XNOR, HALF-XOR and HALF-XNOR. The manufacturer can independently invert any of the four outputs, thereby saving the designer a logic gate in his or her application. When not cycling, the DS1012 draws only 10 μ A of supply current, making it suitable for battery-operated applications such as laptop and notebook computers. In 8-pin DIP and SOIC packages, from \$2.40 (10,000).

Dallas Semiconductor, 4401 S Beltwood Pkwy, Dallas, TX 75244. Phone (214) 450-0448.

Circle No. 388

14-Bit A/D Converter

- Includes S/H amplifier
- Converts at rates to 2 MHz

The ADS-942 14-bit A/D converter uses a subranging architecture to provide high speed and precision. The converter, which features a fast S/H amplifier, can digitize sinusoidal signals to 1 MHz at a 2-MHz sampling rate or step inputs at a 1.3-MHz conversion rate. Functionally complete, the ADC also contains an internal clock, 3-state outputs, and an internal 10V reference. The reference can supply 5 mA to

INTEGRATED CIRCUITS

external circuitry. Other key specifications include total harmonic distortion of -85 dB and a S/N ratio of -77 dB. A pin-selectable feature provides analog input signals of 0 to 10V or ± 5 V. The digital inputs and the 3-state outputs are TTL and CMOS compatible. The ADS-942, which comes in a small, 32-pin DIP, operates from 5V and ± 15 V supplies and consumes 2.9W. From \$374 (OEM qty).

Datel, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356. TLX 174388.

Circle No. 389

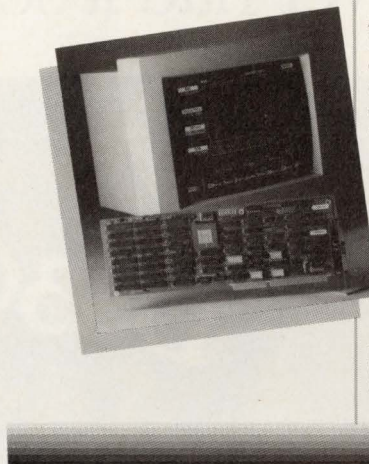
Analog Interface Chip

- Has 25-kHz sampling rate
- Extends voice band to 7600 Hz

For processing signals beyond the 300 to 3000-Hz voice band, the TLC32046 features a user-programmable, analog-input bandpass/low-pass filter having a nominal bandwidth of 300 to 7600 Hz. The maximum sampling rate is 25 kHz. The chip is a complete analog-to-digital and digital-to-analog input/output system that interfaces directly with the TMS320 DSP family. The chip integrates several functions, including 14-bit A/D and D/A converters, a bandpass antialiasing filter, a low-pass output-reconstruction filter, signal conditioning, control, and timing. The device offers three operating modes—telephone, word, and byte—and a selectable (sin X)/X correction for D/A conversion. For flexibility, the device offers programmable sampling rates, filter bandwidths, A/D path gain, and multiplexed analog inputs. The analog input can be single-ended or differential. TLC32046, in a 28-pin DIP or 28-pin quad flatpack, \$14.63 (1000).

Texas Instruments Inc, Semiconductor Group (SC-91045), Box 809066, Dallas, TX 75380. Phone (800) 336-5236, ext 700; (214) 995-6611, ext 700. Circle No. 390

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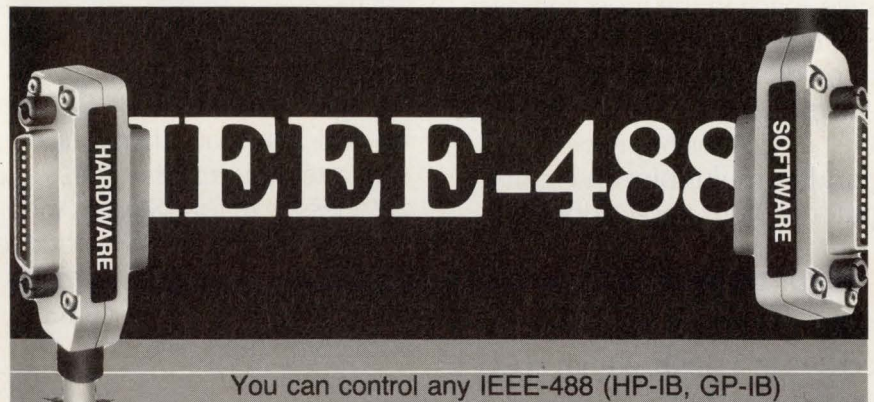
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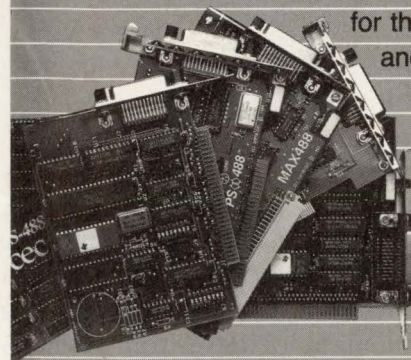
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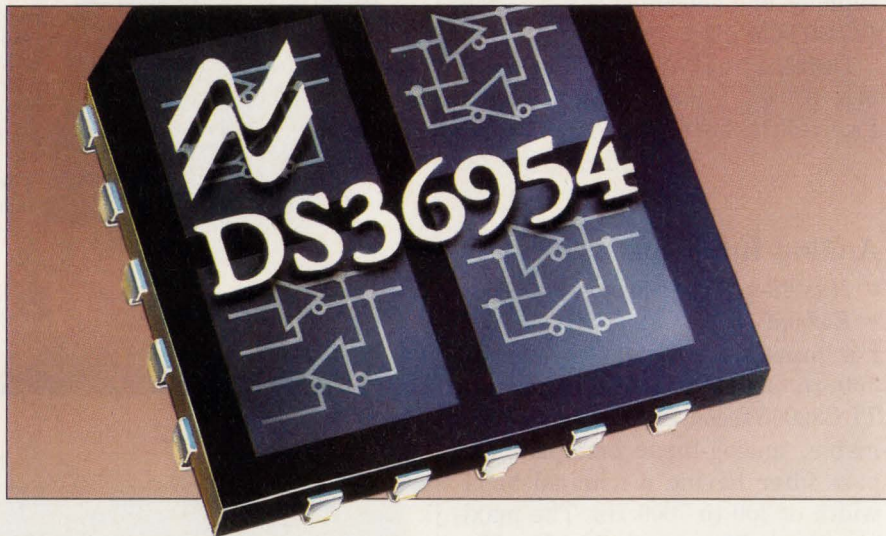
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t _{PHLD}	9	12	19
t _{SKD}		3	6
RECEIVER			
t _{PLH}	9	14	19
t _{PHLD}	9	13	19
t _{SKD}		1	3

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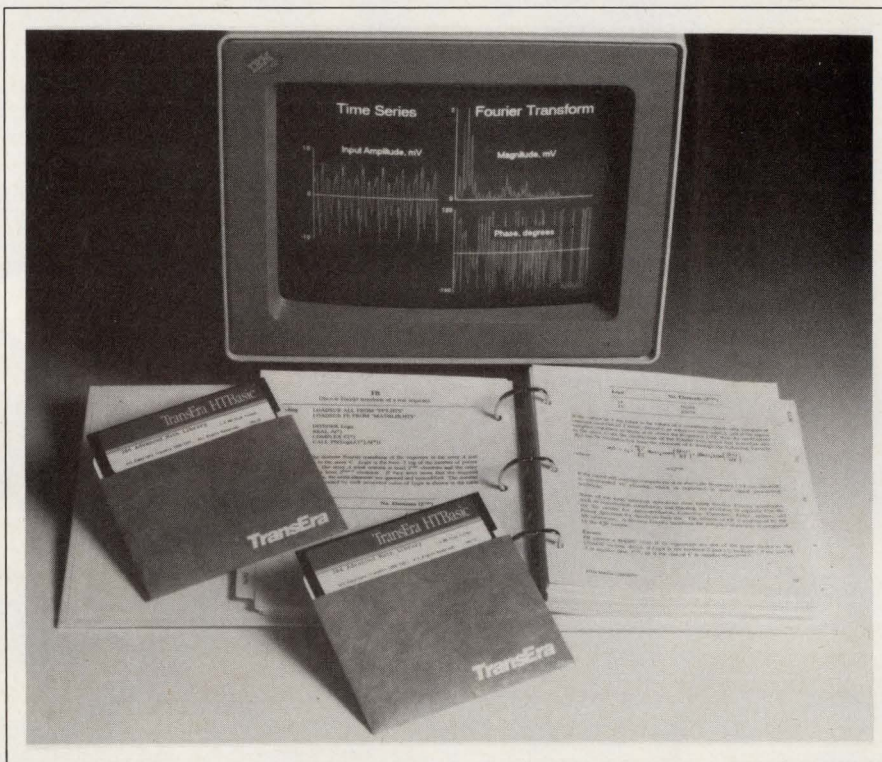
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quires use of the DOS 386 version of HTBasic. Library, \$400; DOS 386 HTBasic, \$925.

TransEra, 3707 N Canyon Rd, Provo, UT 84604. Phone (801) 224-6550
Circle No. 360

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files. The software, which requires use of HP Basic release 6.2, runs on HP Basic workstations such as the HP 9000 Series 300 controllers. It also runs on PCs with either an HP 82300C or HP 82324A measurement coprocessor. HP Basic Plus, \$450; HP Basic 6.2, \$1050; upgrade, \$250. Delivery, eight weeks ARO.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014.
Circle No. 361

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Teamone Systems Inc, 710 Lakeway Dr, Sunnyvale, CA 94086. Phone (408) 730-3500.

Circle No. 362

Text continued on pg 227

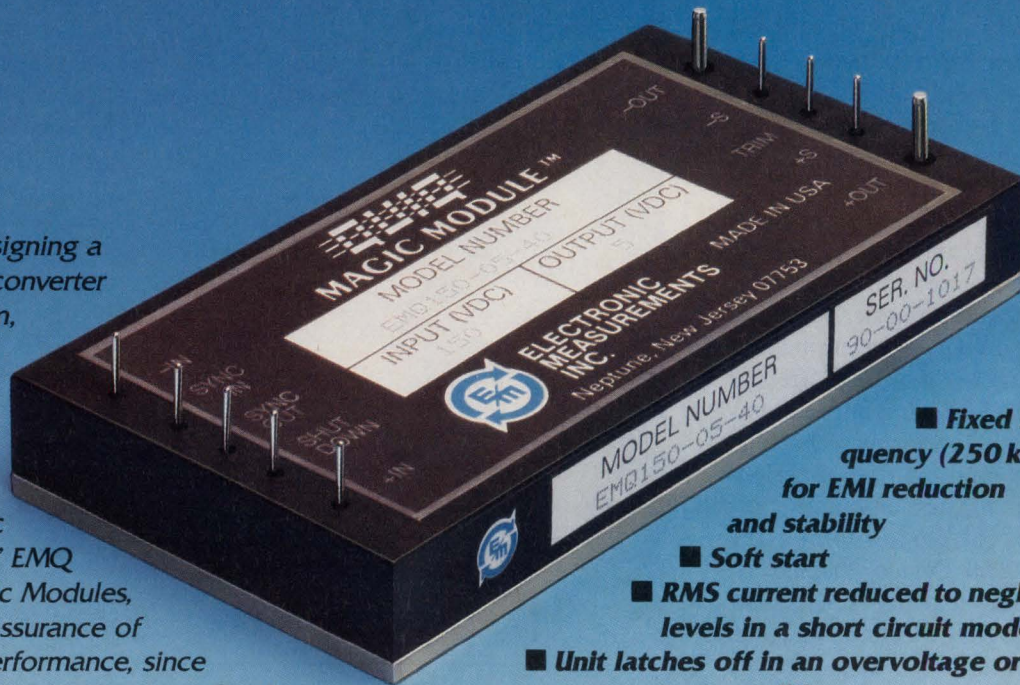
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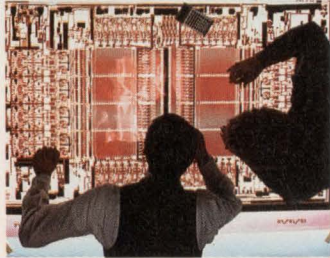
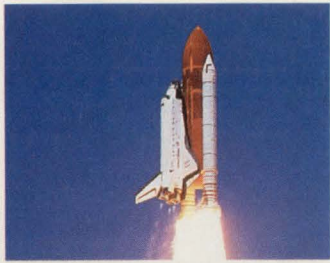
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Integrated Tool Set For Layout And Analysis

- Provides layout for high-speed, high-density modules
- Includes tools for thermal and transmission-line simulation

The CAD Expert suite of tools, part of the supplier's Visula EDA Expert series, provides rules-driven physical-layout tools for high-speed, high-density modules (including pc boards, hybrids, multiple-chip modules, and high-density interconnects). The layout tools are integrated with physical-analysis tools for thermal and transmission-line simulation. The tools allow users to define engineering and manufacturing rules and parameters in the design process and later use those definitions in processes such as component placing and signal routing. By bringing manufacturing constraints into the design and layout phases, they ensure that designers adhere not only to engineering rules in the design process, but also to manufacturing rules. To guarantee design integrity, signal analysis is possible at any phase of the design cycle. Key features of the tool set are a grid-free system architecture that applies to a mixture of fine-line geometries, an object-oriented structure that represents components and data as objects, and an expandable relational database that holds the design and manufacturing rules. From \$32,000.

Racal-Redac, 1000 Wyckoff Ave, Mahwah, NJ 07430. Phone (201) 848-8000. FAX (201) 848-8189.

Circle No. 363

Reverse-Engineering Tool For Fortran Programs

- Shows structure of existing programs written in Fortran
 - Helps create documentation for previously undocumented code
- Teamwork/Fortran Rev graphically reveals the structure of existing Fortran programs, helping engi-

neers understand undocumented code and create new documentation. It automatically generates structured-design charts from Fortran source files; Teamwork/SD, another tool in the supplier's line of CASE products, can display the charts. Users can use a mouse to browse or edit the source code un-

derlying displayed modules, and they can suppress the display of individual modules or entire groups of modules. For example, a user can choose to suppress the display of specific subroutine calls or eliminate all common-block data modules. The product works with many dia-

Text continued on pg 230



8051 & 68HC11

PC-Based In-Circuit Emulators

Nohau Covers All Your Development Needs for the 8051 and 68HC11 Families!

Free Demo

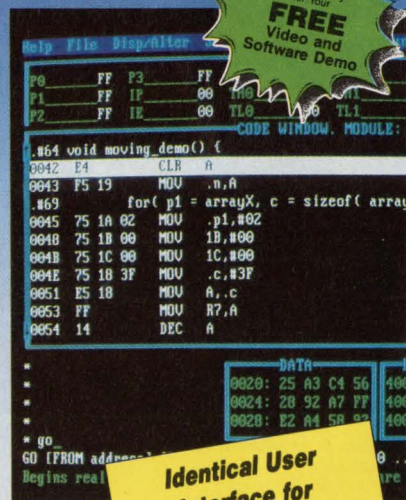
You can start your debugging with this **FREE** demo simulator. You can load up to 512 bytes of code, assembler, C, or PL/M and do full debugging/simulation in assembly and source level. A great way to get started for **FREE**. Fantastic for schools! Just call and we'll send it!

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The full-blown simulator is an extension of the DEMO. You can load up to 64K of code and use 64K of XDATA space. You can program an "external environment" to interact with your code to simulate your target system. The emulator is the hardware extension of the simulator!

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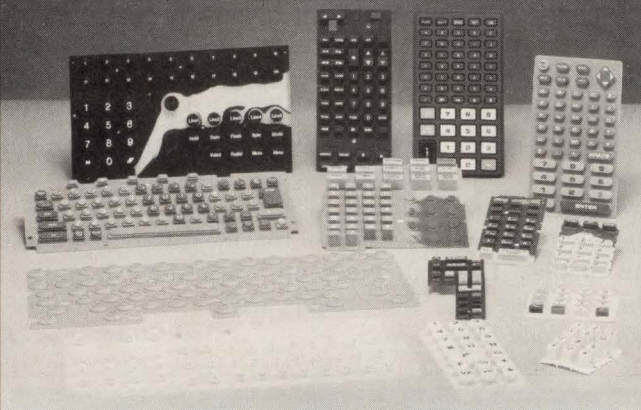
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CIRCLE NO. 156

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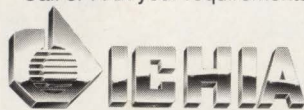


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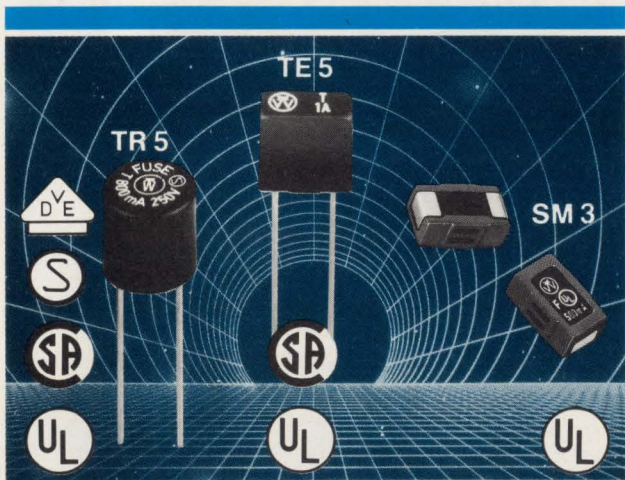
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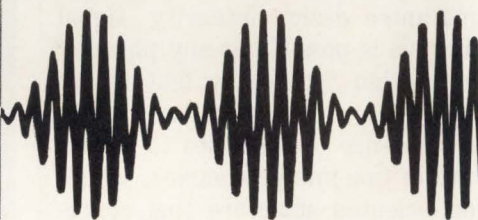
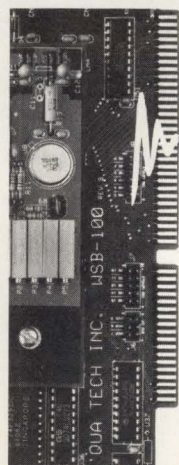


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CIRCLE NO. 193

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lects of Fortran, such as ANSI Fortran-77, MIL-STD 1753, and several language extensions. The language extensions that are covered include those used on workstations from Sun, DEC, HP Apollo, and IBM as well as for several IBM and Cray mainframes. The tool also features preprocessing to assist with

uncommon dialects, plus an open interface between its Fortran parser and its structure-chart generator for customers who need to reverse-engineer custom or proprietary languages. The product is available on Sun systems now; versions for DEC VAX VMS, DEC Ultrix, HP-UX, Apollo Domain, and IBM AIX will

be available in the future. \$9700/seat.

Cadre Technologies Inc, 222 Richmond St, Providence, RI 02903. Phone (401) 351-2273. FAX (401) 351-7380. **Circle No. 364**

DSP Software-Design Tools

- Increase user productivity in programming and debugging
- For fixed- and floating-point DSP families

Two software-design tool sets aid software development and debugging for the supplier's DSP processors. Tool set ADDS-210xx-SW is for floating-point chips, including the recently announced ADSP-21020; tool set ADDS-21xx-SW is for fixed-point devices, including the ADSP-2100A, ADSP-2101, ADSP-2105, ADSP-2111, and ADSP-21msp50. The floating-point set comprises an assembler, linker, assembly library, librarian, simulator, and PROM splitter. The assembler creates object files in industry-standard Common Object File Format (COFF). The simulator, which has context-sensitive help, windowing interface with mouse support, and reconfigurable windows, features full symbolic disassembly and multiple breakpoints. The fixed-point tool set includes an assembler, linker, simulators, and PROM splitter; an optional C compiler package (standard in tool set for VAX) includes a runtime library with more than 100 mathematical and DSP functions. (A C compiler and runtime library for the floating-point set are in beta test.) The floating-point set runs on PCs; the fixed-point set is available for PCs, Sun-3 and Sun-4 workstations, and DEC VAX (VMS 5.3-1) systems. Floating-point set, \$995; fixed-point set, \$795 (PC version); \$1295 (Sun version); and \$5995 (VAX version); C compiler and runtime library, \$1995 (PC); \$2995 (Sun).

Analog Devices Inc, Box 9106, Norwood, MA 02062. Phone (617) 461-3911. **Circle No. 365**

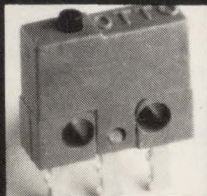
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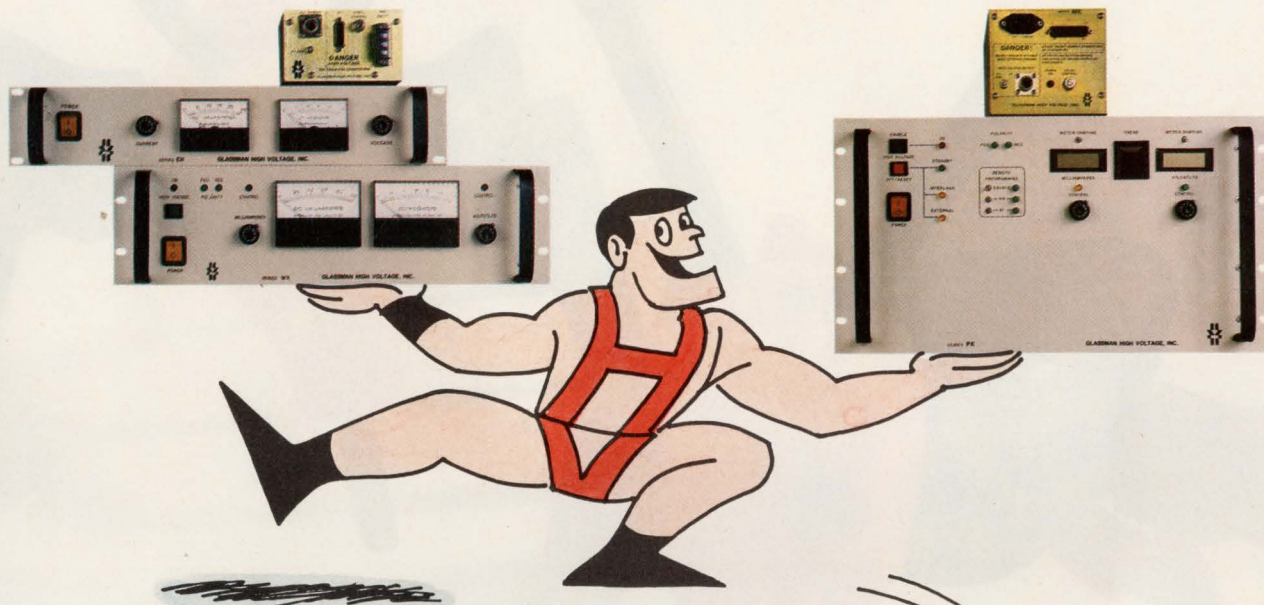
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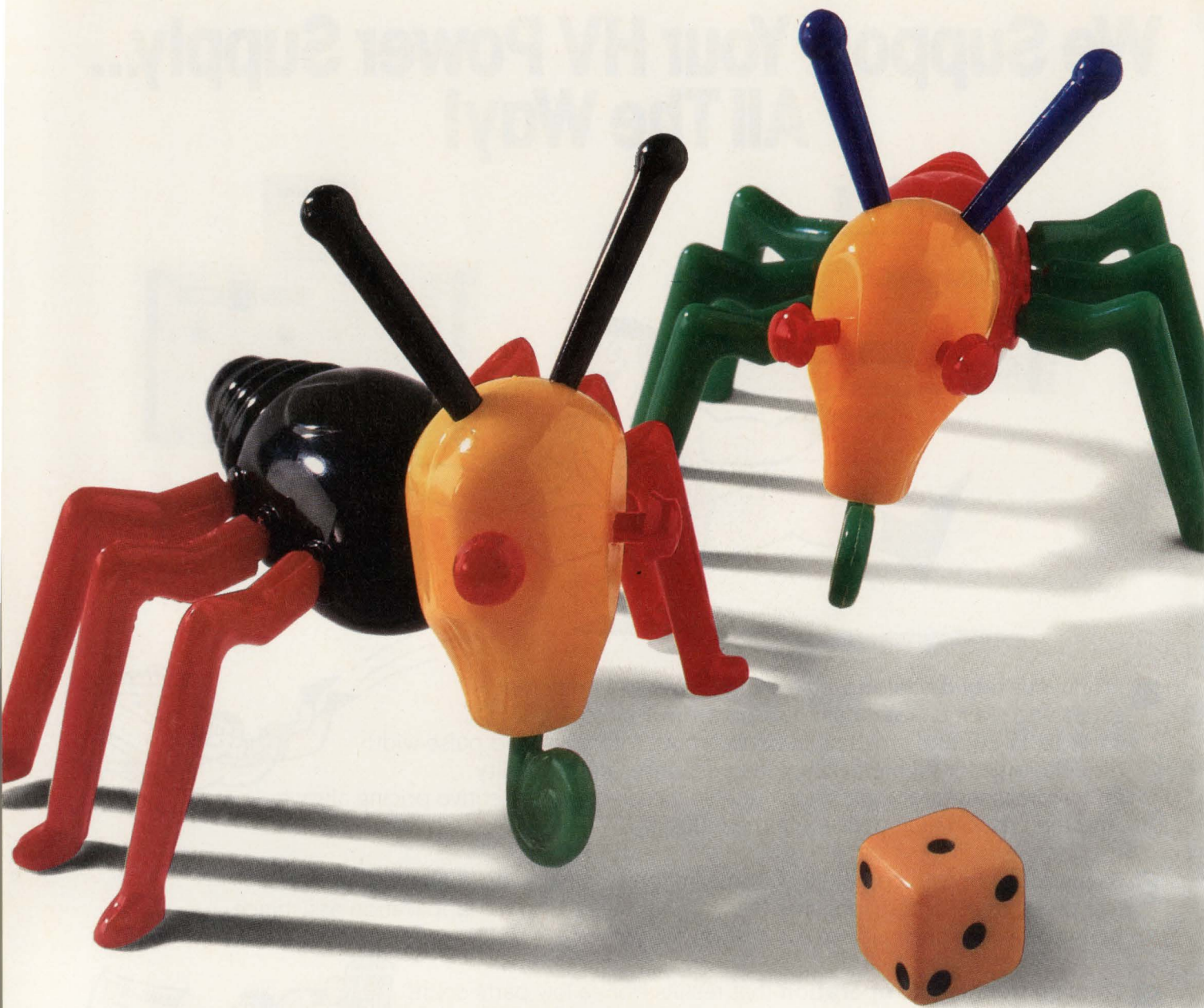
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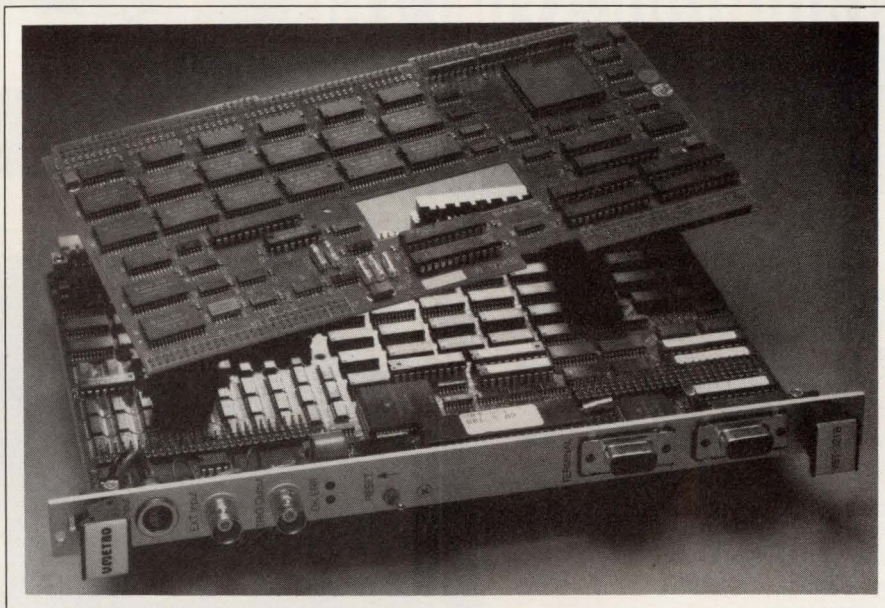
NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

VMEbus Tracer With SCSI Port And Deep Memory

- Records 64k or 256k frames of bus activity
- Sends records to mass-storage device via SCSI port

The XMEM-PB/SCSI board plugs onto the vendor's VBT-321B VMEbus tracer, which is, itself, a VMEbus board. The daughter card stores a 64k-frame (optionally 256k-frame) trace and sends it through an onboard SCSI port to a mass-storage device as a Unix-compatible file. Firmware on the main board is compatible with Sun Microsystems' SunOS version of Unix. The vendor can also furnish a version of the board that incorporates a 2-bank interleaved trace memory. This arrangement allows you to capture SCSI traces continuously and to transfer them to mass storage without gaps. From \$2850.



Vmetro Inc, 2500 Wilcrest Dr, Suite 550, Houston, TX 77042. Phone (713) 266-6430. FAX (713) 266-6919. **Circle No. 351**

Vmetro A/S, Box 213, Leirdal, 1101 Oslo 10, Norway. Phone (472) 322580. FAX (472) 322880.

Circle No. 352

IEEE-488 DACs

- Can have two or four 16-bit DACs
- Each DAC is ohmically isolated from chassis to 500V

The DAC488/HR2 and DAC488/HR4 D/A converters are 1³/₄-in.-high, ac-powered units that you can mount in an equipment rack. They connect to the IEEE-488 bus and contain either two or four plug-in boards, respectively, which hold a 16-bit DAC. Each DAC is optically isolated from the chassis and the bus, and can continuously transfer data from the bus to its output at 100 kwords/sec. Each DAC includes an 8-kword buffer. Two options are available: One option increases a buffer to 128 kwords; the other option increases a buffer to 480 kwords. Because the unit is μ P controlled, you can increase the size of any buffer by looping—repeatedly routing a range of stored values to a DAC. Linking buffer segments lets you create still longer

waveforms. To create a function generator, you can synchronize the unit to an external clock or use one of its several built-in clocks and trigger sources. DAC488/HR2, \$2495; DAC488/HR4, \$3495; 128-kword-buffer option, \$195; 400-kword-buffer option, \$395.

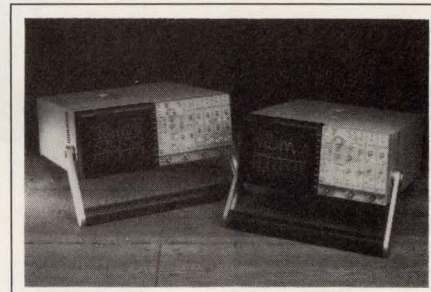
Iotech Inc, 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 431-4093. TWX 650-282-0864.

Circle No. 353

2- and 4-Channel, 150-MHz Digital Scopes

- Take 400 Msamples/sec
- Have 16 nonvolatile waveform memories

The 4060 family of DSOs includes the model 4062, a 2-channel unit and the 4064, a 4-channel unit. Both DSOs offer 150-MHz bandwidth and, in single-shot mode, take 400 Msamples/sec on each channel.



Each unit includes 16 nonvolatile waveform memories. You can position cursors to obtain an on-screen numeric display of voltage or time. In addition, the scopes display pulse parameters measured according to IEEE-194 (1977). Pretriggering to 100% of the sweep time and post-triggering to 999 sec let you acquire only the portion of a waveform you want to view. A limit-comparison function lets the scopes check every sample against a range of allowable values. If any sample falls outside the range, the scopes capture the

Text continued on pg 237

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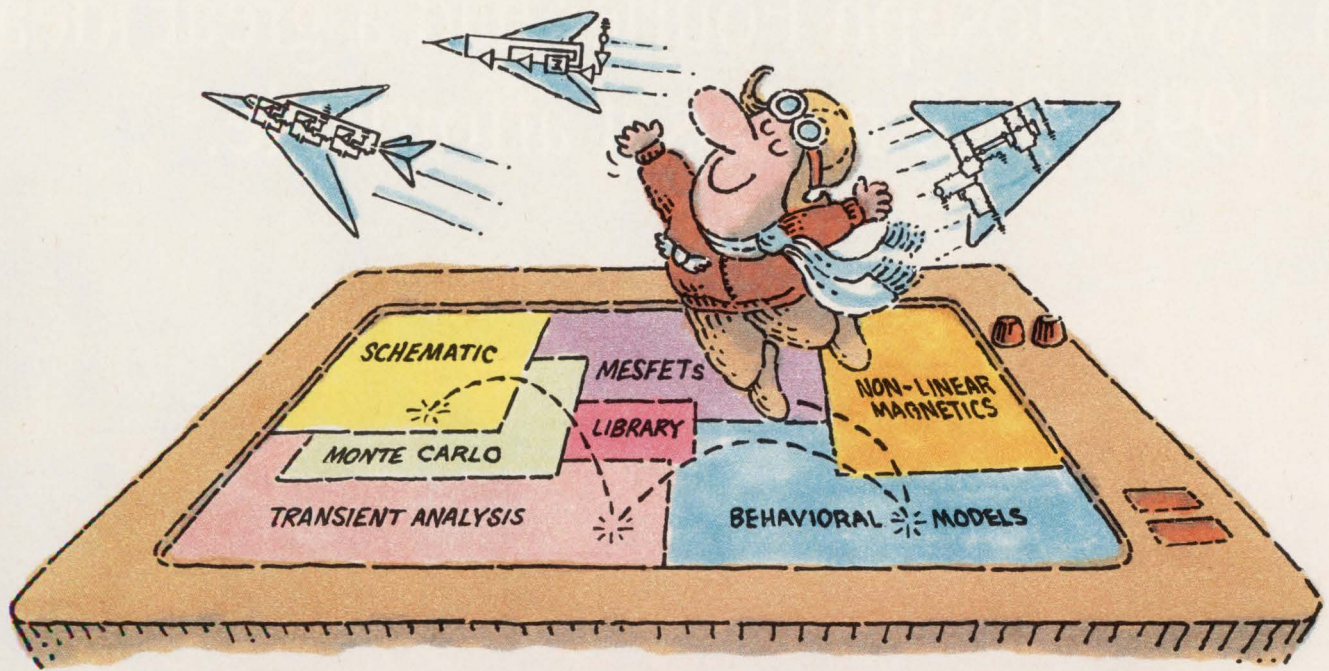
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CIRCLE NO. 162



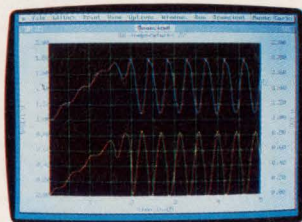
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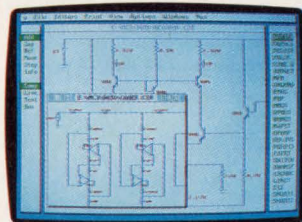
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Analysis and simulation is faster, too. Because the program's now in "C" and assembly language. That also means more capacity — for simulating even larger circuits.

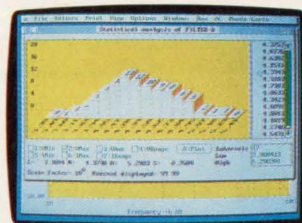
As always, count on fast circuit creation, thanks to window-based operation and a schematic editor. Rapid, right-from-schematics analysis — AC, DC, fourier and transient — via SPICE-like routines. The ability to combine digital/analog circuit simulations using integrated switch



Transient analysis



Schematic editor



Monte Carlo analysis

models and parameterized macros. And stepped component values that streamline multiple-plot generation.

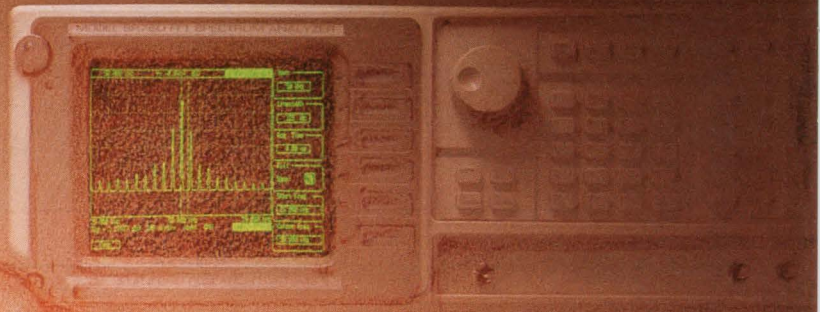
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Circle No. 354



Benchtop PC-Board Diagnostic Tester

- Tests analog and digital ICs in circuit
- Uses test history to optimize test routines

The Pro-Line PL 5000 pc-board diagnostic system is an in-circuit tester for analog and digital ICs. It can test TTL, CMOS, and ECL devices. The basic unit has 48 channels including six guard lines. You can expand it to 64 channels. Menu-based software helps you create programs for specific boards. You tell the tester the component designations and IC types and indicate their X-Y locations on the board. You then move a test clip from IC to IC, and the unit "learns" the board. During testing, the tester prompts you to enter the board's serial number and fault symptoms. The tester uses this information to optimize the test routines and to help it determine probable causes of the symptoms. From \$14,950.

Maxtec International Corp, 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-1448.

Circle No. 355

Sbus and VMEbus-Based Timebase Generators

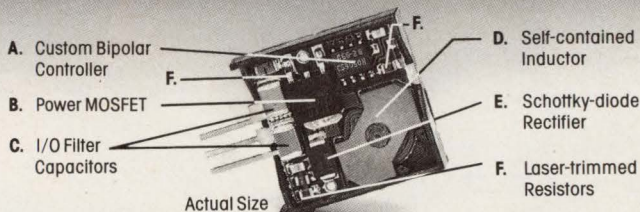
- Synchronize computer systems to an external time code
- Maintain 1- μ sec accuracy

The AITG timebase generator boards use an externally supplied time code to synchronize the time kept by Sun Microsystems worksta-

tions. The boards also generate time codes for use elsewhere. A board that synchronizes other equipment need not receive a time code from a separate source. The boards accept codes in such formats as Interrange Instrumentation Group (IRIG) -A and -B and Na-

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INNOVATION OF THE YEAR AWARD WINNER



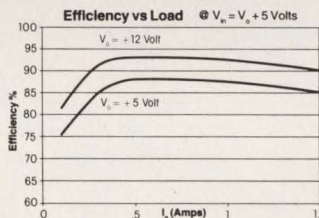
- A. Custom Bipolar Controller
- B. Power MOSFET
- C. I/O Filter Capacitors
- D. Self-contained Inductor
- E. Schottky-diode Rectifier
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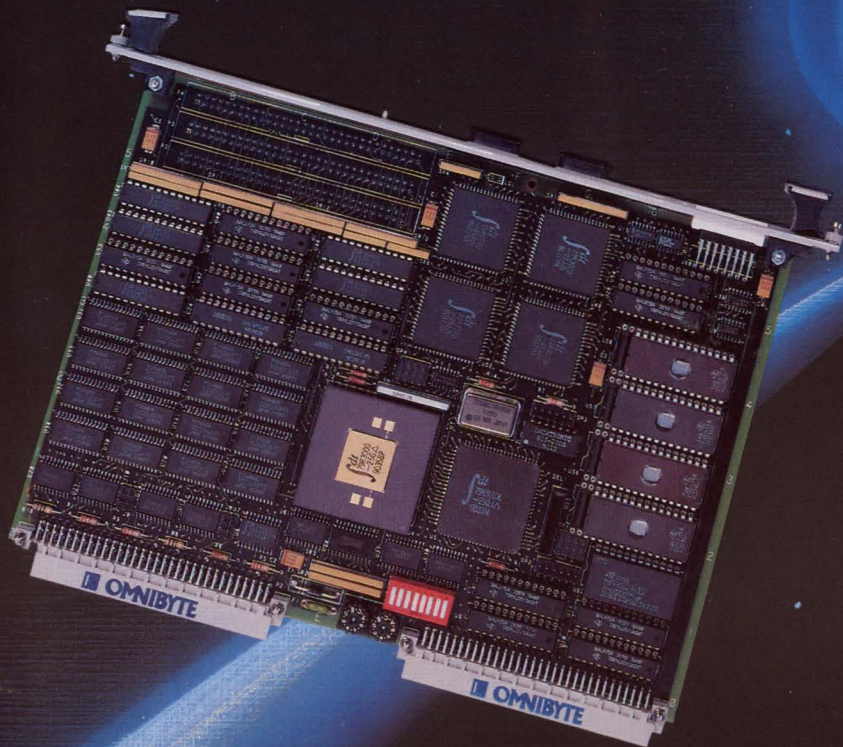
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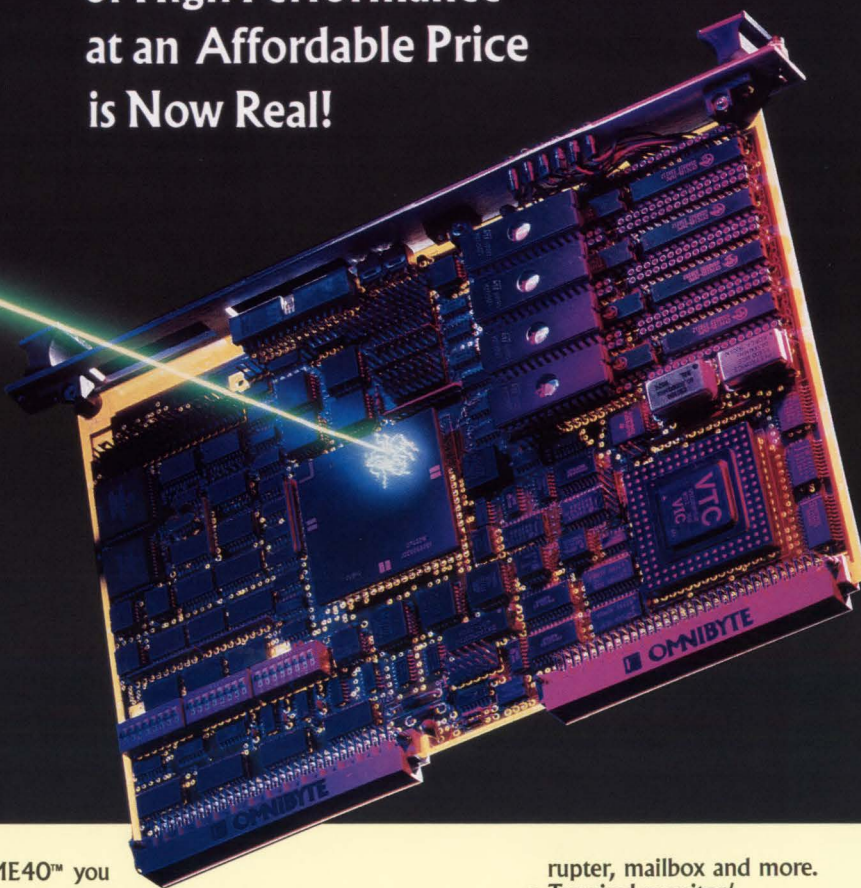
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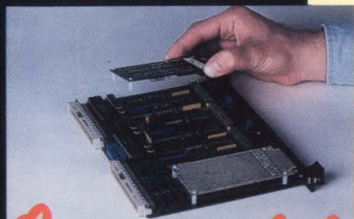
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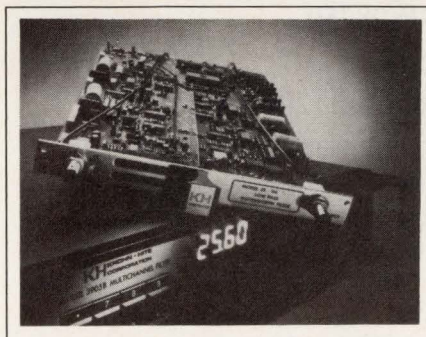
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tional Aeronautics and Space Administration (NASA) 36 and 2137. The boards keep time with an accuracy of 1 μ sec. The AITG-VME-9U is for Sun workstations that use VMEbus I/O boards in the so-called 9U format. The AITG-S is a single-width Sbus card for Sun's SPARCstations. VME device, \$2250. Delivery, 30 to 45 days ARO. Sbus device, \$2350. Delivery, November 1991.

Odetics Inc., 1515 S Manchester Ave, Anaheim, CA 92802. Phone (714) 774-5000. **Circle No. 356**



Programmable Lowpass Filter

- Has 4-pole Butterworth response
- Corner frequency is settable from 170 Hz to 25.6 MHz

The Model 35 is a plug-in board for the vendor's IEEE-488-programmable modular-instrument chassis. The board contains a 4-pole Butterworth active lowpass filter with cut-off frequencies that you can program from 170 Hz to 25.6 MHz with 2½-digit resolution. Below 2.56 MHz, the cutoff frequencies are accurate to $\pm 2\%$; from 2.56 to 25.6 MHz, accuracy is $\pm 5\%$. The board offers both dc and ac coupling and has an input amplifier with selectable gains of 1, 10, and 100 $\pm 1\%$. You can bypass the filter and use the board as an amplifier with 50-MHz bandwidth. The maximum input is ± 1.5 V pk divided by the gain. \$1800. Delivery, six to eight weeks ARO.

Kron-Hite Corp., 255 Bodwell St, Avon, MA 02322. Phone (508) 580-1660. **Circle No. 357**

Network Analyzer For RF-Component Testing

- Has 300-kHz to 1.3-GHz, 1-Hz resolution synthesized source
- Provides dynamic range of 90 dB

The HP 8711A RF network analyzer helps you characterize circuit components at high frequencies. The instrument contains a 1-Hz

resolution, 300-kHz to 1.3-GHz, swept, synthesized signal source that completes a full-band sweep in 50 msec. The analyzer has a 9-in. CRT display and a dynamic range of 90 dB. The unit has a 3½-in. floppy-disk drive. With an optional interpreter but without a host com-

Text continued on pg 245

VORTEX™ Concentrates I/O for top 'C40 performance



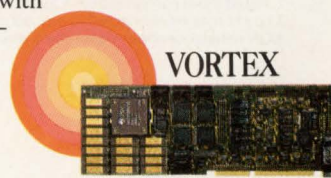
Harness the awesome power of TI's TMS320C40 digital signal processor to your AT or compatible computer—the Vortex system board from ASPI is all you need!

The Vortex is particularly well-suited for prototyping and implementing multiprocessor configurations. The six 'C40 communication ports allow direct processor-to-processor communication; almost any number of Vortex Boards can be linked quickly and easily by just plugging them together.

Besides the main TMS320C40 processor, a Vortex Board has a TI TMS320C31 floating-point processor. The 'C31 can be used with the 'C40 for I/O processing or filtering, or for entirely separate functions. This gives the Vortex a total floating-point capacity of 83 MFLOPS.

The Vortex will accommodate up to 2 Mbytes of SRAM, and works with ASPI's daughter boards—including a 64 Mbyte DRAM board, digital audio interface and general A-D/D-A systems.

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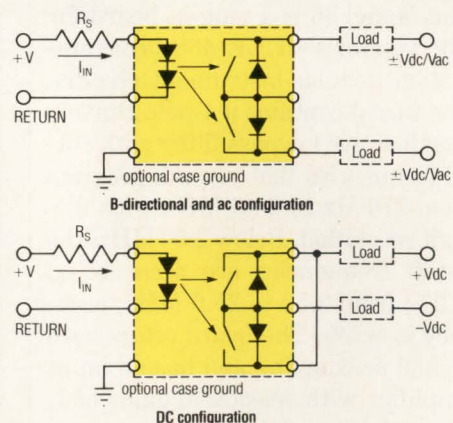
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- Very-low leakage current (200 nA)
- DC or bi-directional power FET output (see wiring diagrams)
- Ideal for ATE applications
- Optical isolation
- Fast switching speed
- Adjustable turn-on times
- Low profile 6-pin mini-DIP
- Cost efficiency

Review the electrical characteristics below and call us for immediate application assistance.*

INPUT ELECTRICAL CHARACTERISTICS (-55° to +105° unless otherwise noted)				
	Min	Max	Units	
Continuous Input Current (I_{IN})	10	50	mA_{DC}	
Input Current (Guaranteed On)	10		mA_{DC}	
Input Current (Guaranteed Off)		100	μA_{DC}	
Input Voltage Drop at (I_{IN}) = 25mA		3.25	V _{DC}	
OUTPUT ELECTRICAL CHARACTERISTICS (-55° to +105° unless otherwise noted)				
Part Number	FB00CD	FB00FC	FB00KB	Units
Bidirectional Load Current (I_{LOAD})	±1.0	±0.50	±0.25	$\text{A}_{DC}/\text{A}_{PK}$
DC Load Current (I_{LOAD})	2.0	1.0	0.5	A_{DC}
Bidirectional Load Voltage (V_{LOAD})	±80	±180	±350	$\text{V}_{DC}/\text{V}_{PK}$
DC Load Voltage (V_{LOAD})	80	180	350	V_{DC}
ON-Resistance (R_{ON}) at (I_{LOAD}) max.	0.72	1.8	12.9	Ohms
Turn-On Time (T_{ON})	800	800	500	μs
Turn-Off Time (T_{OFF})	300	600	500	μs

Notes: 1. A series resistor is required to limit continuous input current to 50mA (peak current can be higher).
 2. Rated input current is 25mA for all tests.
 3. Loads may be connected to any output terminal.
 4. ON resistance shown is for the bidirectional configuration. The DC ON resistance is 1/4 of these values.



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TOKIN was able to accomplish all this by firing two special materials with different temperature characteristics at a low temperature (less than 1,000°C), thereby

increasing capacitance while cutting costs. A dramatic breakthrough in capacitor technology.

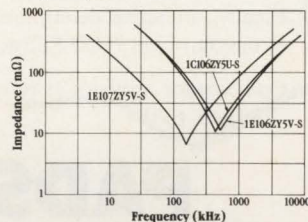
What's more, you can put these devices to work in a wide range of application including EMI/EMC filters

and bypass capacitors.

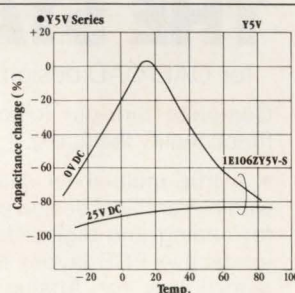
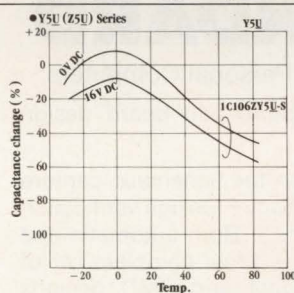
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Stability at Low and High Temperatures



New Multilayer Ceramic Capacitor

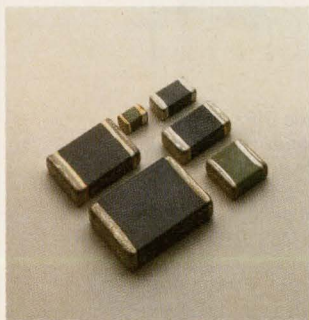
		25V10 μ F		25V22 μ F	
		Dimensions (mm)	Case Code	Dimensions (mm)	Case Code
NEW	Y5U (Z5U)	2.7x5.7x2.5	C205M ^{*1} C205F	5.0x5.7x2.5	C505F
	CONVENTIONAL	Y5U	6.3x10.0x3.0	C610F	—
	Y5V	4.0x8.0x2.5	C408F	6.3x10.0x3.0	C610F

*New product C205M: Nickel/Tin Plate Termination

Ceramic Capacitor End Termination

Nickel/Tin Plate Termination ^{*1}	IE106ZY5U-SD
Fired-on End Termination	All Case Code

^{*1}The product is the experimental stage



Characteristics

	Temp. Characteristics Y5U (Z5U)			Temp. Characteristics Y5V		
	25V	50V	75V	25V	50V	75V
10 μ F	IE106ZY5U-C205M IE106ZY5U-C205F	IH106ZY5U-C505F	IN106ZY5U-C610F	10 μ F	IE106ZY5V-C408F	IH106ZY5V-C610F IN106ZY5V-C812F
22 μ F	IE226ZY5U-C505F	IH226ZY5U-610F	—	22 μ F	IE226ZY5V-C610F	IH226ZY5V-C812F
33 μ F	IE336ZY5U-C610F	IH335ZY5U-C812F ^{*1}	—	33 μ F	IE336ZY5V-C610F	—
47 μ F	IE476ZY5U-C812F ^{*1}	—	—	100 μ F	IE107ZY5V-C812F	—

^{*1}C812F (8x12.5x3mm): The product is in the experimental stage.

TOKIN

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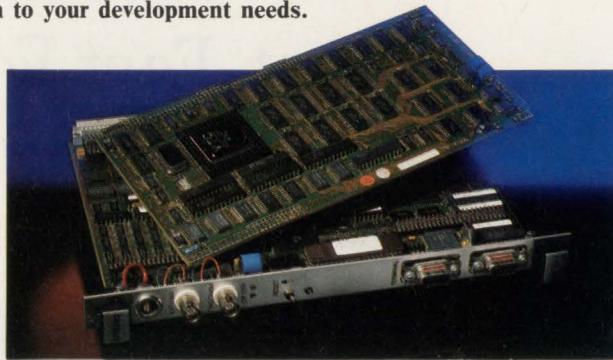
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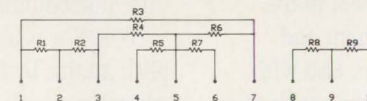
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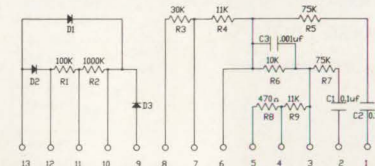
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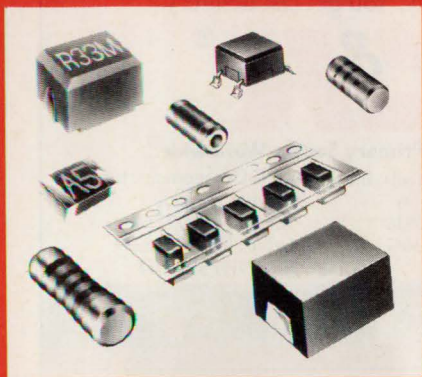
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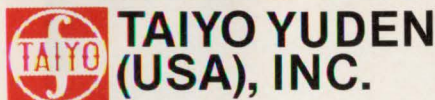
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CIRCLE NO. 173

TEST & MEASUREMENT

puter, it can run programs written in the Instrument Basic language. This capability lets you use the analyzer by itself to automate procedures. You can write programs on an external computer, but you can do so without a computer by recording keystrokes or by using a plug-in keyboard. \$13,500; Basic, \$1350; keyboard, \$210. Delivery, 16 weeks ARO.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 358



Logic Analyzer

- Captures data at 200 MHz
- Can have up to 384 channels

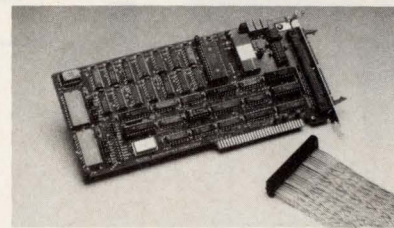
The Clas 2000 logic-analysis system captures data at speeds to 200 MHz and can have 384 channels. The system includes a 40-Mbyte hard drive, a floppy-disk drive, a keyboard, and a mouse. The graphic operator interface uses a windowed, icon-based display. You can configure all channels as a single analyzer or split them into two independent, synchronized, cross-triggered logic analyzers that have 5-nsec timing resolution. Microprocessor analysis packages include disassembly software and interface hardware for popular processors including the 68020, 68030, 68040, and 88000; the 80286, i386, i486, and i960; the T800 family, and the TMS320C25 and TMS320C30. \$15,950 to \$45,950.

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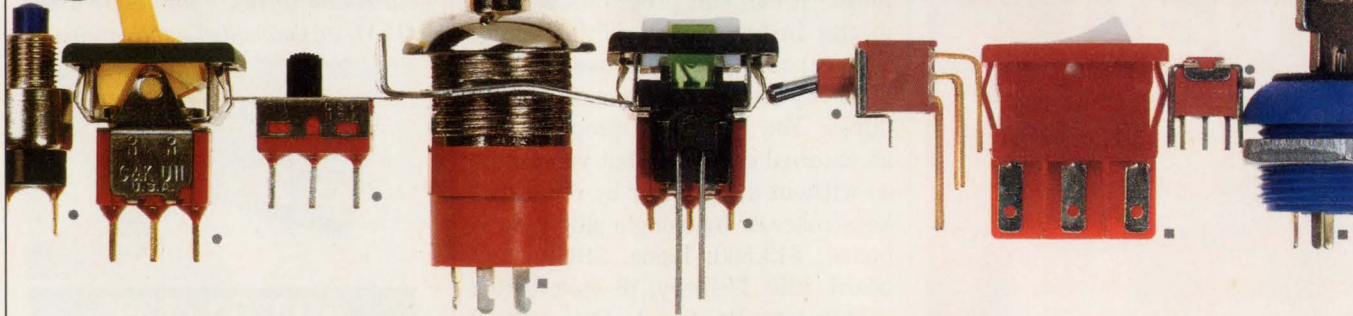
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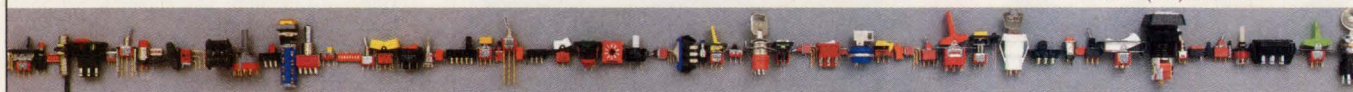


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CIRCLE NO. 175

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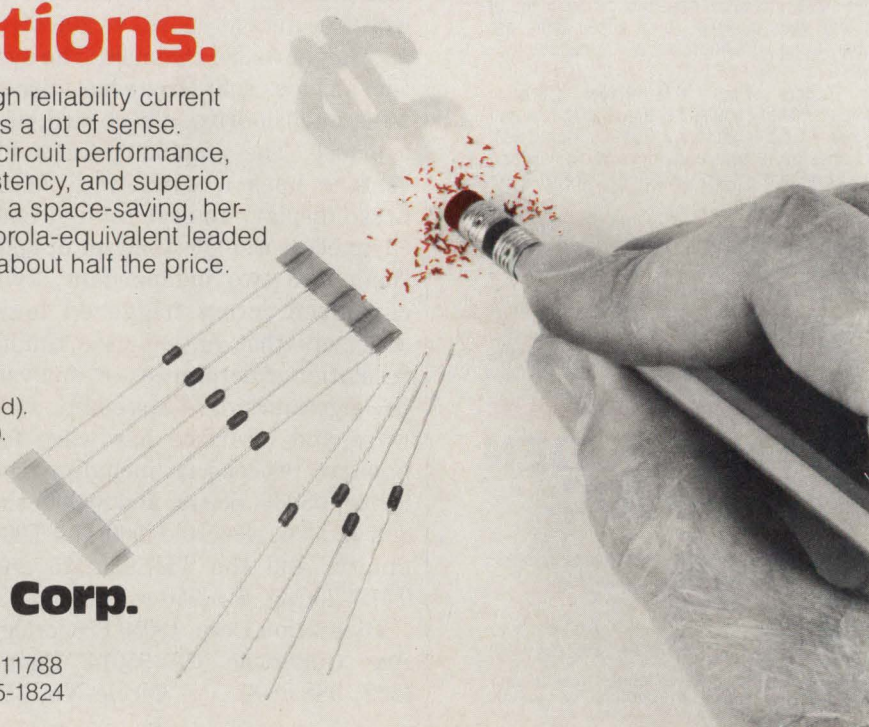
Available Types:

1N5283 THRU 1N5314 (leaded).
CCL0035 THRU CCL5750 (leaded).
CMCL1300 THRU CMCL 1304 (leaded).
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NEW PRODUCTS

COMPUTERS & PERIPHERALS

40-MHz 386 Computer

- Uses AMD's Am386DX μ P and a 64-kbyte cache
- Has 4 Mbytes of dynamic RAM and a 220W power supply

The ME 386-40 ISA bus computer uses AMD's 40-MHz Am386DX μ P. The base configuration has a 64-kbyte cache, 4 Mbytes of dynamic RAM, a 1.2-Mbyte, 5-1/4-in. floppy-disk drive, a parallel port, two serial ports, a keyboard, and a 220W power supply. The cache is expandable to 256 kbytes, and you can expand the mother board's memory to 64 Mbytes. The mother board has a socket for either an Intel 80387 or a Weitek 3167 coprocessor. The computer delivers 9.71 MIPS. The mother board has six 16-bit and two 8-bit ISA bus expansion slots. You can opt for a hard-disk drive with capacities ranging as high as 750 Mbytes, and you have a choice of a 101-key keyboard or a keyboard with a trackball mouse. Base configuration, \$1949; base configuration with an 80-Mbyte, hard-disk



drive, 1.44-Mbyte, 3-1/2-in. floppy-disk drive, super VGA color card and monitor, and either DOS 3.3 or 4.01, \$2899.

Micro Express, 1801 Carnegie Ave, Santa Ana, CA 92705. Phone (800) 642-7621; (714) 852-1400. FAX (714) 852-1225. **Circle No. 374**

Facsimile Relay

- Digitizes and compresses Group III fax data
- Connects a PBX trunk to a modem's data input port

The FR-100/EM4W facsimile (fax) relay lets you transmit Group III fax data over a data network. The unit digitizes and compresses the analog output signal from a Group III fax machine and produces 9600- or 4800-bps digital data. The unit connects a fax machine or a PBX trunk to the data port of a modem or a multiplexer. To transfer fax data over a data network, you need a fax relay at each end of the link. The relay supports both DTMF and pulse dialing and handles PBX signals type I through V. The relay operates from 110 to 220V ac and consumes 15W max. The unit meas-

ures 5.5×9.0×8.5 in. and weighs 7 lbs. \$3640.

Entropic Speech Inc, 10011 N Foothill Blvd, Cupertino, CA 95014. Phone (408) 973-9800. FAX (408) 973-0336. TLX 1561464.

Circle No. 375

Pen Recorders

- Display 24 input signals in four colors
- Sequentially scan each channel for 0.1, 0.2, or 0.5 secs

The HR Series of pen recorders measure and record as many as 24 input signals. The recorders display the data in three modes—analogue trends, analogue trend with digital printout, and data logger. The units scan each input channel for 0.1, 0.2, and 0.5 sec/channel. They display

analog data in four different colors, permitting six channels/color. You can program the units to record the following parameters using LCD displays—year, month, day, minute, recording mode, chart speed, data size, print interval, type of input signal, and measuring range. The recorders can also print a message of as many as 79 characters/line at any location on the chart. A clock and a timer for starting and stopping measurements are also included. The recorders have IEEE-488 or RS-232C ports for computer communications. From \$3495.

Soltec Corp, Sol Vista Park, 12977 Arroyo St, San Fernando, CA 91340. Phone (800) 423-2344; (818) 365-0800. FAX (818) 365-7839.

Circle No. 376

Killer Specs.



Panther[®] SCSI

Stalking system performance is your goal. That's why Maxtor's 1.2GB SCSI Panther was designed to perform a data seek in just 13ms. No other drive in its class features such lightning speed.

Panther's hunting prowess of 2ms track-to-track seek time stands out compared to Seagate's Wren 7 seek time of 2.5ms. And Panther outruns the competition with a 30Mb/sec. internal transfer rate.

Experience counts. Panther uses the reliable head disk assembly used in the Maxtor XT-8000, which boasts more than 300,000 units in the field. Panther shreds the competition with the widest range of available controllers, an MTBF of 150,000 hours, Novell certification and a highly competitive price.

Call about the full line of Panther drives that range from 1.2GB to more than 1.7GB capacity. If you're stalking performance, check out Panther's killer specs. *Call your nearest Authorized Maxtor Distributor.*

1GB-plus Disk Drive Comparison Criteria	Maxtor Panther P0-12S	Seagate Wren 7
Capacity (unformatted)	1.2GB	1.2GB
Seek Time	13ms	15ms
Track-to-Track	2ms	2.5ms
Internal Transfer	17.4 to 29.7Mb/s	15-23Mb/s
Maximum Seek	26ms	34ms



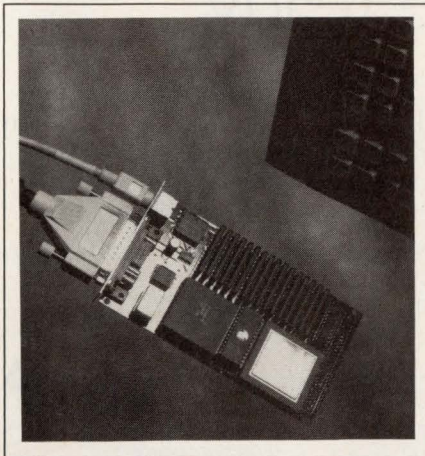
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We Drive Harder.

Maxtor[®]

CIRCLE NO. 177



Sbus Graphics Board

- Drives 1280 x 1024-pixel displays
- Runs on Sun's Open Windows 2.0 software

The GXTRA 1280 single-slot graphics card works with the Sbus in Sun SPARCstations. It drives 1280 x 1024-pixel displays and has a Sun-4 keyboard and mouse port. The board contains an 8-bit-color frame buffer, and it runs on Sun's Open Windows 2.0 software. Windows executes partially on the board and partially on the host CPU. You can install multiple Sbus boards to service additional users on a single SPARCstation. The board uses a proprietary gate array, which accelerates low-level graphics primitives such as drawing 2-D vectors, solid and stipple fills, and characters. \$2250.

Tech-Source Inc, 442 S North Lake Blvd, Suite 1008, Altamonte Springs, FL 32701. Phone (407) 830-8301. FAX (407) 339-2554.

Circle No. 377

80286 Single-Board Computer

- Contains 4 Mbytes of PROM disk emulation
- ISA bus board contains 4 Mbytes of DRAM and two RS-232C ports

The IND-286 single-board-computer (SBC) works with a passive 8-bit ISA bus. The SBC contains a 16-MHz 80C286 μ P and features ROM-DOS, an MS-DOS 3.3-com-

patible, ROM-based, disk-operating system. The board also includes a battery-backed, 4-Mbyte, PROM disk emulator and a watchdog timer. The emulator boots the system and lets you place application software in EPROM or battery-backed static RAM. The board's flash EPROM programmer permits field upgrades. The SBC features as much as 4 Mbytes of dynamic RAM. It has five kinds of ports: two RS-232C; one parallel printer; one keyboard; one floppy disk; and one IDE hard disk. A clock/calendar and a socket for an optional 80C287 coprocessor also comes with the board. Using an embedded BIOS setup utility, you can configure a system and set the clock/calendar. The board consumes 4W. \$795.

Micro Computer Specialists Inc, 2598-G Fortune Way, Vista, CA 92083. Phone (619) 598-2177. FAX (619) 598-2450. Circle No. 378

Ethernet Board

- Installs in Macintosh IIsi and SE/30 computers
- Comes in coax or 10BaseT twisted-pair versions

The Ether DS Ethernet adapter board installs in the direct slot of a Macintosh IIsi or SE/30 computer. A coax version supports thick or thin Ethernet and a twisted-pair version supports 10BaseT Ethernet networks. The board's drivers for Apple's Ethertalk Phase I and Phase II protocols free you from using high-level protocols. Macintosh computers can communicate via Appletalk, TCP/IP, DECnet, or other high-level protocols. Network management software, which comes with each board, provides statistics on Ethernet performance and lets you run loop-back diagnostic tests. \$395.

Compatible Systems Corp, Box 17220, Boulder, CO 80308. Phone (800) 356-0283; (303) 444-9532. FAX (303) 444-9595. Circle No. 379

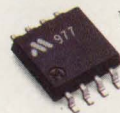


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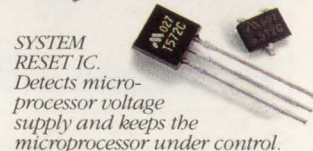
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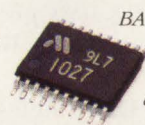
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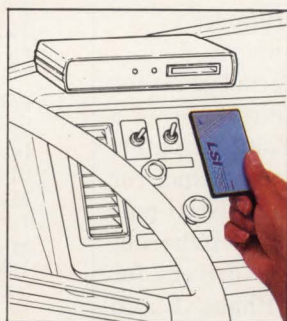
CIRCLE NO. 179

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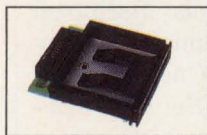
LSI CARD is the most reliable memory card applying contactless access system (CCL Technology) and solves all the problems for other memory cards such as water, oil, dust, stain, contact wear, static electricity etc.

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LSI CARD provides a variety of card drive from CPU BUS Direct connection to PC bus drive to complete your system design.



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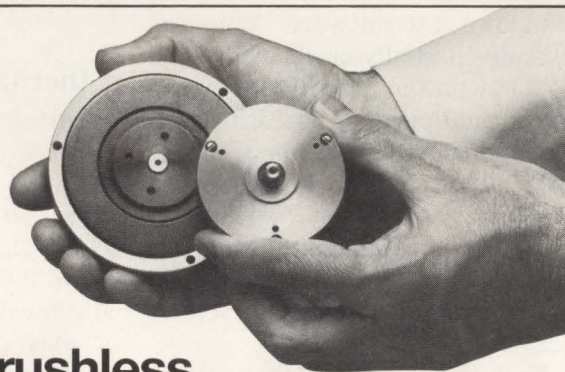


DRIVE UNIT

You may call now the following contact for further information.

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c/o. ADVANCED TECHNOLOGY DEVELOPMENT, INC.
3301 El Camino Real, Atherton, CA 94027
TEL: 415-367-0522/FAX: 415-368-7717



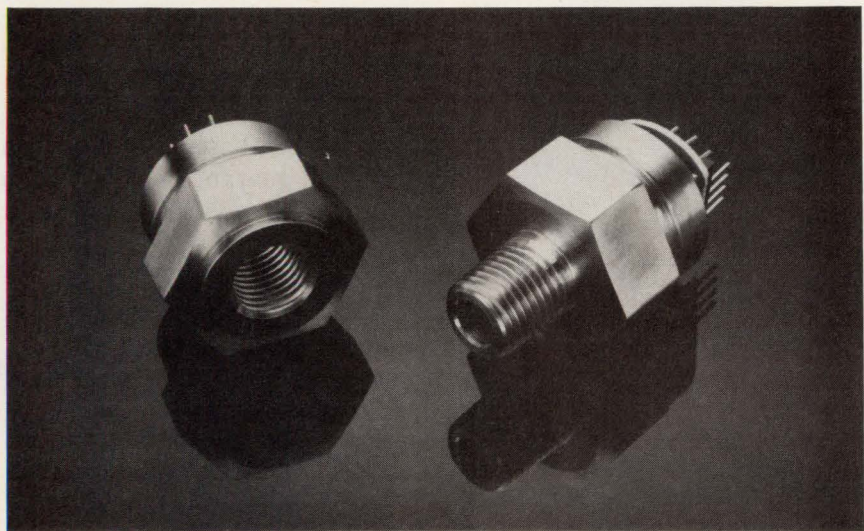
Brushless DC motors provide extended life in demanding applications

These compact 12-24 VDC motors are designed for tape cartridge drives, business machines, medical equipment, pumps/compressors and similar applications. Available in 2.0" and 3.2" diameters with stall torque from 10 to 84 oz-in. Custom shaft and housing and configurations to match your requirements. AMETEK, Lamb Electric Division, 627 Lake Street, Kent, OH 44240. Tel: 216-673-3451. Fax: 216-673-8994. In Europe, Friedrichstrasse 24, 6200 Wiesbaden, Germany. Tel: 611-370031. Fax: 611-370033.

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NEW PRODUCTS

COMPONENTS & POWER SUPPLIES



Pressure Transducers

- *Designed to handle rugged environments*
- *Provide gauge or absolute-pressure measurements*

The Model 1230 and 1231 pressure transducers feature all 316L stainless construction and employ a proprietary technology that isolates the semiconductor sensor from harsh media and environments. Both are available in gauge and absolute-measurement versions in pressure ranges of 5 to 5000 psi. Static pressure-measurement accuracy for standard B grade units

equals 0.25%; 0.125% accuracy is available in A grade units. Respective thermal errors from -28 to +82°C are ± 2.5 and $\pm 1.25\%$. Standard versions are available with a choice of constant current or voltage excitation. Output span is a normalized 100 ± 2 mV dc, and long-term measurement repeatability equals $\pm 0.02\%$. A 4-pin, in-line connector provides electrical connections. Model 1230, \$75 to \$80; Model 1231, \$90 to \$115.

Foxboro/ICT Inc, 199 Riveroaks Pkwy, San Jose, CA 95134. Phone (408) 946-1010. **Circle No. 391**

Current Source

- *Develops a 4- to 20-mA output*
- *Has a $\pm 1\%$ accuracy*

Model 930 in combination with the MK298 mounting kit can convert a 0 to 10V input into a 4- to 20-mA output. With a different mounting kit, the unit develops a constant output of 0.5 to 500 mA. Converter accuracy equals ± 15 of full scale. The response time to a step change in the load of 10 to 100 Ω in 100 msec is 10 μ sec max. Typical frequency response with a 100 Ω load equals 10 kHz. The converter operates with any supply voltage in the

12 to 32V range and draws 60 mA max at full load. \$108. Delivery, stock to six weeks ARO.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (800) 542-3355; (415) 932-3911. FAX (415) 932-6017. **Circle No. 392**

Crystal Oscillator

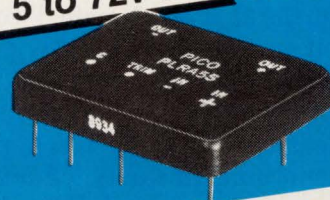
- *Features ± 55 -ppm/V sensitivity*
- *Has 25-ppm stability*

The Model VC-7025 voltage-controlled crystal oscillator (VCXO) features a specified control sensitivity of ± 55 ppm/V. Sensitivity val-

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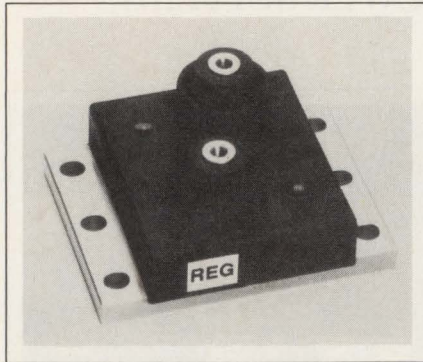
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COMPONENTS & POWER SUPPLIES

ues as high as ± 70 ppm/V are attainable. Housed in a 14-pin DIP measuring only $0.31 \times 0.52 \times 0.82$ in., the oscillator has a 25-ppm frequency stability over a 0 to 70°C range and features 5-nsec rise and fall times. Output frequency range for the oscillator spans 2 to 35 MHz. The unit can drive a 10-gate load (TTL or CMOS) and operates from a single 5V supply. Current drain equals 35 mA. Nominal control-voltage level equals 2.5V dc, and control-voltage range spans 0.5 to 4.5V dc. Deviation sensitivity measures ± 50 ppm/V typ, and monotonic linearity equals 20% max. Aging characteristic for the oscillator is specified at ± 1 ppm/year. \$14.50 (1000). Delivery, 8 to 10 weeks ARO.

Raltron Electronics Corp., 2315 NW 107th Ave, Miami, FL 33182. Phone (305) 593-6033. FAX (305) 594-3973. **Circle No. 393**



High-Power Resistors

- Handle 250W
- Available in 0.1% tolerances

Designed specifically for snubber protection circuits, REG resistors can handle continuous loads of 250W and withstand 2-kW instantaneous pulses. Resistance values range from 1 to 1500Ω, and resistance tolerances of 0.1 to 5% are available. Over a 20 to 60°C range, temperature coefficient of resistance equals 20 ppm/°C max. Isola-

tion and inductance values equal 5000V ac min and 400 nH max, respectively. Resistor construction provides an efficient thermal interface. The Manganin resistive element mounts on a ceramic plate, which then mounts directly to a large copper baseplate. This construction guarantees an internal heat resistance of 0.1° K/W max. From \$150.

Isotek Corp., 566 Wilbur Ave, Swansea, MA 02777. Phone (508) 673-2900. FAX (508) 676-0885.

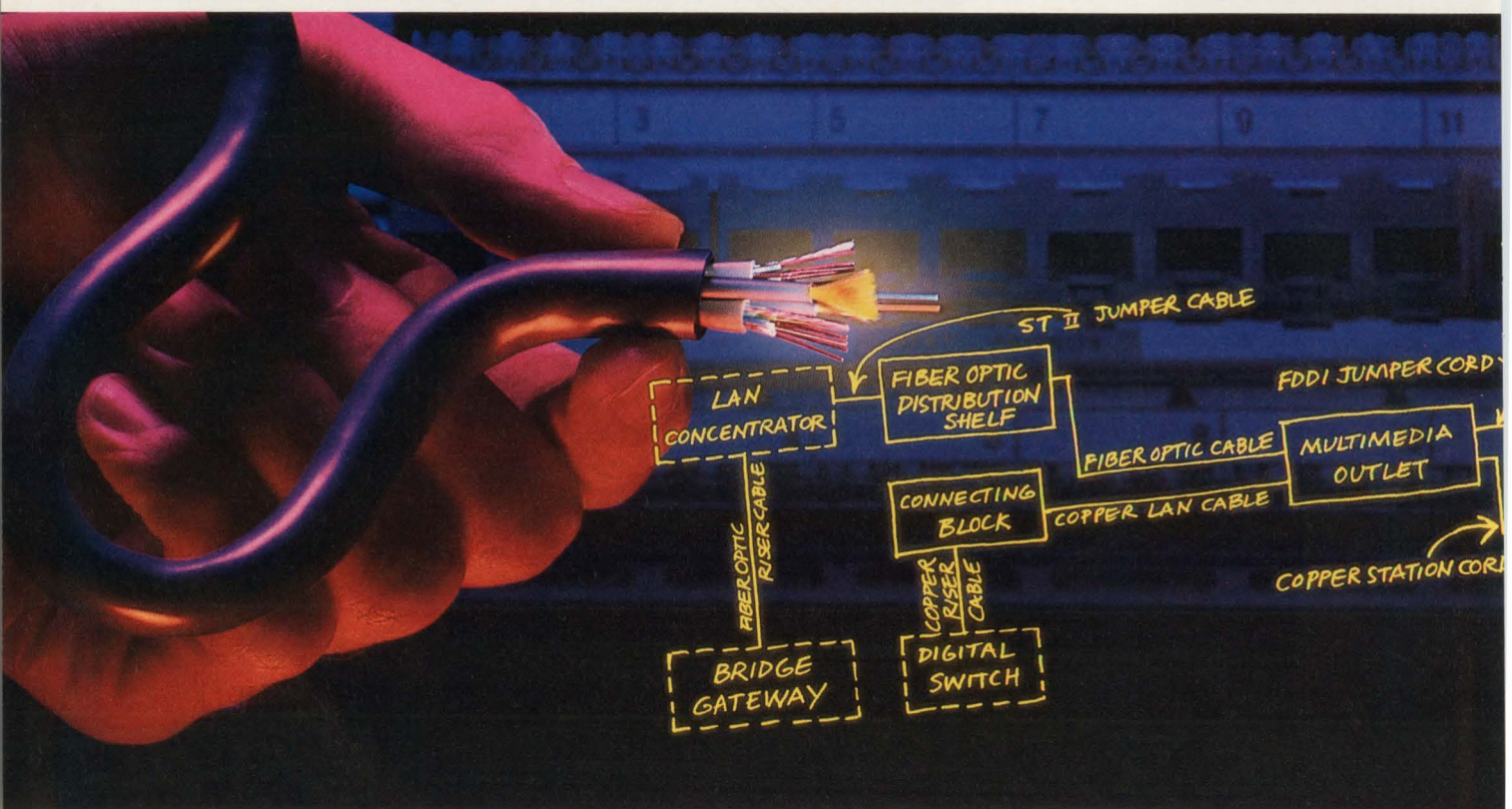
Circle No. 394

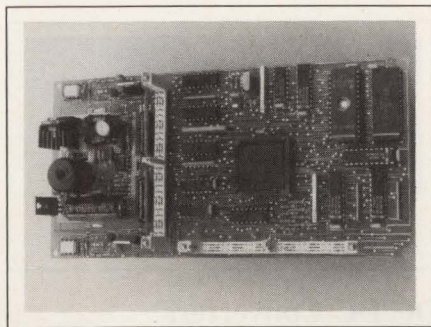
Cooling Module

- Controls fans or blowers
- Is RS-232C compatible

The CMM cooling management module is a smart control system that accepts temperature, air flow, or other sensor data as inputs. The unit provides failure prediction and

Every connecting product for every kind





overall system management such as speed control and on/off functions. The module features an embedded microcontroller with PID (peripheral-integral-differential) loops to control fans or blowers. The unit is RS-232C compatible and allows you to perform system upgrades using software. The modules are available with custom I/Os in 5 to 48V versions, and they can control from 6 to 20 fans or blowers. The module can synchronize all fans to avoid "beat" phenomenon, and it

can compensate for filter blockages and other user-defined temperature variations. From \$150 (100).

Cambridge Aeroflo Inc, 900 Mount Laurel Circle, Shirley, MA 01464. Phone (508) 425-2346. FAX (508) 425-2338. **Circle No. 395**

Power MOSFETs

- Feature on-chip current limiting
- Protected from shorted load conditions

The MLP1N06CL and MLA1N06CL TMOS power MOSFETs have integrated on-chip current limiting, gate-to-source voltage clamping, and gate-voltage protection. The voltage-clamping capability protects the device against unclamped inductive switching transients and overvoltage stress conditions. This feature provides high immunity to ESD. The devices also self-protect against shorted load

conditions by limiting current flow when the gate is fully enhanced. Both units can be driven directly with CMOS or TTL drivers. MLP1N06CL, in a standard TO-220 package, \$1.48; MLA1N06CL, in a fully isolated TO-220 package, \$1.73 (1000). Delivery, stock to eight weeks ARO.

Motorola Inc, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-3370. FAX (602) 244-4015.

Circle No. 396

Futurebus + Backplane

- Conforms to the hard metric specification
- Features 13 slot positions

This 128-bit Futurebus + backplane conforms fully to the P1301 hard metric specifications as well as the P896.2 specification from revision 5.4. The unit has 13 slots positioned on a 30-mm spacing and accepts

of connection.

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CIRCLE NO. 182

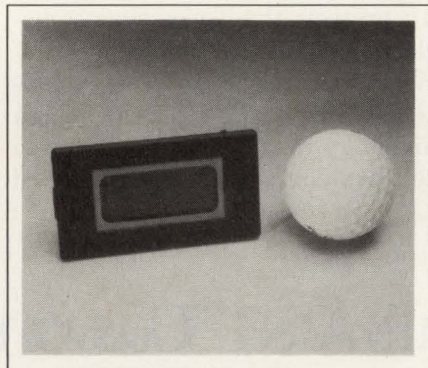
Stalking the field for an interconnect solution specialist?



12SU daughter boards. Each slot has 80 pins available for user-specified I/O via a rear connector. Arbitration is implemented as an optional 48-pin connector located at the center of each slot of the backplane. Power distribution is implemented via press-fit connectors rated for 45A. Multiple power and ground planes are provided on the 5 and 2.1V lines to alleviate the problem of ground bounce. \$1920. Delivery, four to six weeks ARO.

Bicc-Vero Inc, 1000 Sherman Ave, Hamden, CT 06514. Phone (203) 288-8001. FAX (203) 287-0062.

Circle No. 397



Digital Panel Meter

- Has an LCD readout
- Features 0.1% accuracy

The Model DPM5035L 3½-digit voltmeter features snap-in installation and a built-in bezel. It has a basic measurement range of ± 199.9 mV dc with an accuracy of $0.1\% \pm 1$ digit. Power consumption is 2 mW at 9V dc and 1 mW max at 5V dc. A 0.5-in.-high LCD provides the readout. The unit operates from a 5 to 15V power supply and has an input impedance of $10^{10}\Omega$ min. Decimal-point position is user selectable. The meter operates over a 0 to 50°C range, measures 3.1 × 1.7 × 0.95 in., and weighs approximately 1.6 oz. \$22.55 (100). Delivery, stock to six weeks ARO.

DI International Inc, 95 E Main St, Huntington, NY 11743. Phone (516) 673-6866. Circle No. 398



DC/DC Converters

- Only 0.27 in. high
- Operate to 125°C

MSA Series 5W dc/dc converters are only 0.27 in. high and are rated for full-power operation from -55 to +125°C. The units operate over the full MIL-STD-704 input range of 16 to 40V. Single- and dual-output models are available with 5, 12, 15, ± 12 , and ± 15 V options. Dual-output models support unbalanced loading with as much as 90% of the total rated load available from either output. The converters are fully isolated and offer typical line and load regulation as low as 15 mV. Typical output-ripple voltage is 50 mV, input-ripple current is 40 mA p-p, audio-rejection specifications are 50 dB. From \$225 (100).

Interpoint Corp, Box 97005, Redmond, WA 98073. Phone (206) 882-3100. Circle No. 399

Optical Switch

- Has no contact mechanism
- Activates with a 15g force

The EE-SA105 optical switch operates without a contact mechanism, using an infrared LED and phototransistor combination to indicate activation. It activates with a 15g operating force and has a 0.059-in. pretravel. The infrared LED accommodates 50-mA forward current levels and has an output of 0.5 mA min at V_{CE} equals 5V. The switch has a high output when in the rest position; fully activated, the switch has a 200-mA-max dark-current output. LED output intensity degrades only 7.5% after 500 hours of continuous operating time. \$0.99 (5000).

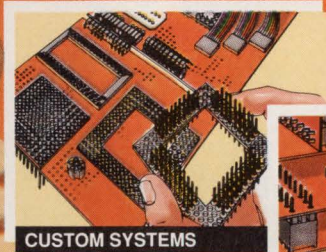
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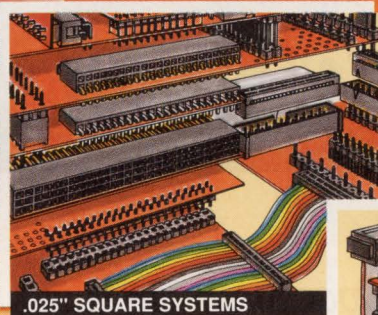
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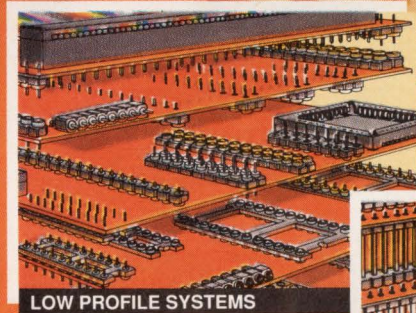
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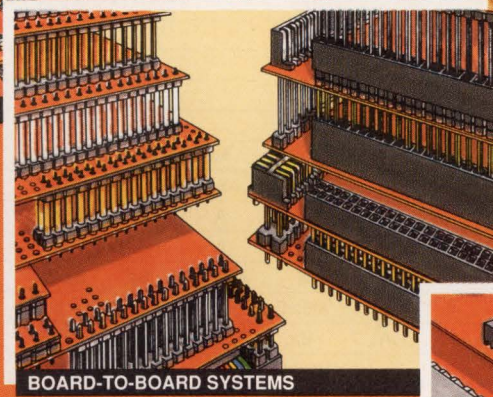
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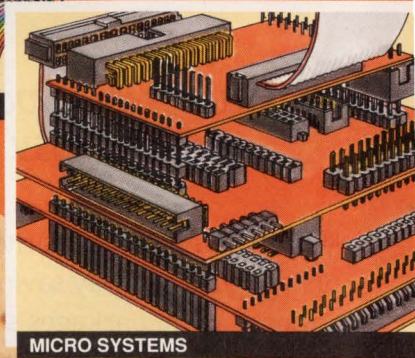
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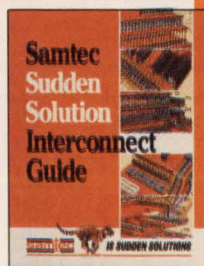
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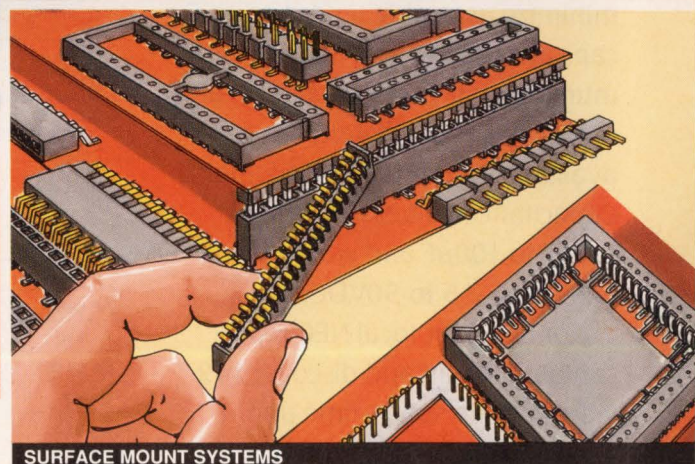
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0.33							A ₂		A	B ₂
0.47							A ₂	A	A•B ₂ •B	B ₂
0.68						A ₂	A ₂ •A		A•B ₂ •B	C
1.0					A ₂	A ₂ •A		A	B ₂ •B	C
1.5			A ₂	A ₂ •A	A	A		B ₂ •B	B ₂ •B•C	D
2.2			A ₂	A ₂ •A	A	A	B ₂ •B	B ₂	B ₂ •B•C	D
3.3			A ₂ •A	A	A	A•B ₂ •B	B ₂	B ₂ •B•C	C•D	
4.7	A ₂	A	A	A	A•B ₂ •B	B ₂	B ₂ •B•C	C	D ₂ •D	
6.8		A	A•B ₂ •B	B ₂	B ₂ •B•C	C	D ₂ •D	D ₂ •D		
10		A•B ₂ •B	B ₂	B ₂ •B•C	C	C•D ₂	D ₂ •D			
15	A	B ₂	B ₂ •B•C	C	C•D ₂	D ₂ •D				
22		B ₂ •B•C	C	C•D ₂ •D	D ₂ •D	D ₂ •D				
33		C	C•D ₂ •D	D ₂ •D	D ₂ •D					
47		C•D ₂ •D	D ₂ •D	D ₂ •D						
68		D ₂ •D	D ₂ •D							
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	W	L	H
A ₂ case	1.6 (.063)	3.2 (.126)	1.2 (.039)
A case	1.6 (.063)	3.2 (.126)	1.6 (.063)
B ₂ case	2.8 (.110)	3.5 (.138)	1.9 (.075)
B case	2.6 (.102)	4.7 (.185)	2.1 (.083)
C case	3.2 (.126)	6.0 (.236)	2.5 (.098)
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mm (inch)

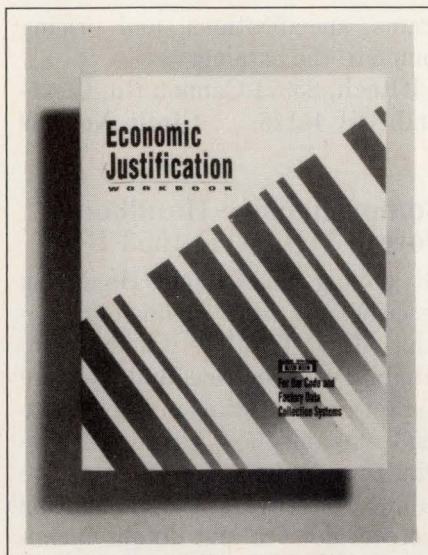
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EDN September 16, 1991

LITERATURE



Justifying Bar-Code Data-Collection Systems

This workbook, *Economic Justification*, details investing in a bar-code data-collection system, using one of three economic-analysis techniques: payback, present value, or rate of return. The 28-pg booklet also presents examples such as time and attendance, labor tracking, work-in-process tracking, shipping and receiving, and warehouse management. Worksheets and formulas round out the publication.

Burr-Brown Corp., Box 11400, Tucson, AZ 11400.

Circle No. 366

Catalog Documents Add-On Products For CAD/CAM

The 1991 Third Party Catalog features the vendor's software. It discusses approximately 200 hardware and software products that complement or extend the uses of the Personal Designer CAD package and the Personal Machinist CAM package. More than 80 third parties—including hardware and software vendors, CAD/CAM users, and CAD/CAM resellers—developed and now offer the products described in the catalog. Included are *Application Software* for augmenting the company's two software packages in areas such as solid de-

sign, parametrics, sheet-metal folding and unfolding, and kinematics; *Symbol Libraries* for applications ranging from mold design and steel detailing to tool design and welding; *Data Management Software* for tracking, revision control, and controlling access to engineering documents; *Translators* for exchanging

the software packages' databases with Chrysler, Ford, GM, and other databases; *Networking Products*, which links more than one of the two software-package systems; *Macros and Utilities* for time saving and convenience in areas such as text editing, plot spooling, and redefining keyboard and menu lay-

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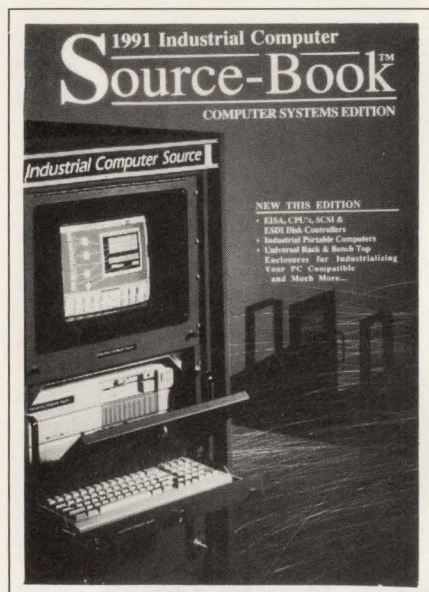
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outs; *Training Manuals and Teaching Aids* to augment the standard documentation and tutorials; and *PC Hardware*, which provides graphics boards, plotters, digitizers, and other peripherals.

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Source Book Covers IBM PC-Related Products

Computer Systems Edition II features more than 800 IBM PC-related products. It describes applica-

tions in telecommunications, industrial and education laboratories, factory automation, and process measurement and control industries. The 96-pg publication notes the addition of 20-, 15-, and 10-slot rack and benchtop chassis, 8- and 15-slot chassis with electroluminescent displays, 6-, 10-, and 15-slot OEM card cages, industrial portable and transportable computers, and a universal rack-mount kit. Other additions include an 80486 25-MHz, EISA plug-in CPU card, 19-in. rack accessories, A/D and communications cards, and Labtech Notebook with Iconview.

Industrial Computer Source, 4837 Mercury St, San Diego, CA 92111.

Circle No. 368

Support Products For Peripherals And Computers

This catalog offers an array of support products for the company's peripherals and computers. Divided into seven sections, the publication covers serial HP-IB (IEEE-488) converters; IBM PC/AT, PS/2, and 386 interfaces; HP 900 file-transfer packages; HP-IB bus extenders; the Macintosh/HP-IB converter; the parallel/HP-IB converter; and cables and accessories. Block dia-

grams, specifications, and pricing complete the catalog.

Iotech, 25971 Cannon Rd, Cleveland, OH 44146. **Circle No. 369**

Comprehensive Handbook Covers MIL-STD-1553 ICs

The 608-pg 1553 Product Handbook describes the vendor's line of monolithic MIL-STD-1553 ICs for high-reliability aerospace and defense markets. A tutorial on MIL-STD-1553 explains how to design systems to meet its requirements. The publication covers the monolithic protocol devices and details monolithic transceivers with block diagrams, features, characteristics, and package pinouts for each product. Application notes, discussions of quality and reliability, ordering information, and the complete text of MIL-STD-1553B round out the handbook.

United Technologies Microelectronics Center, 1575 Garden of the Gods Rd, Colorado Springs, CO 80907.

Circle No. 370

DMA, Data-Acquisition Fundamentals, And Interrupts

Three application notes examine fundamentals of DMA and data ac-



IEEE 488.2 for PCs

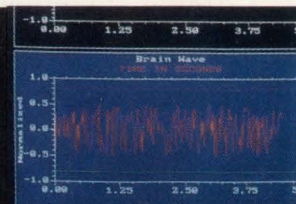
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LITERATURE

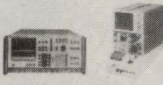
quisition, and programming interrupts. *Data Acquisition Fundamentals* (Part No. 340019-01) explains the use of PCs such as the IBM PC/XT, PC/AT, PS/2, or Macintosh for laboratory research, industrial control, and test and measurement. It illustrates such elements of data acquisition as transducers, signal conditioning, data acquisition, and analysis hardware and software. *Programming Interrupts for Data Acquisition on 80x86-Based Computers* (Part No. 340022-01) deals with interrupt programming on computers based on the 80x86 family of μ Ps that are used on IBM PC/XT, PC/AT, PS/2, and EISA computers. *DMA Fundamentals on Various PC Platforms* (Part No. 340023-01) shows how DMA is implemented in a typical PC architecture and compares several PC DMA applications.

National Instruments, 6504 Bridge Point Pkwy, Austin, TX 78730. **Circle No. 371**


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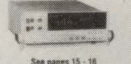
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This catalog of new and used electronic test equipment provides listings of oscilloscopes, spectrum analyzers, DMMs, power supplies, signal sources, and environmental chambers from manufacturers such as

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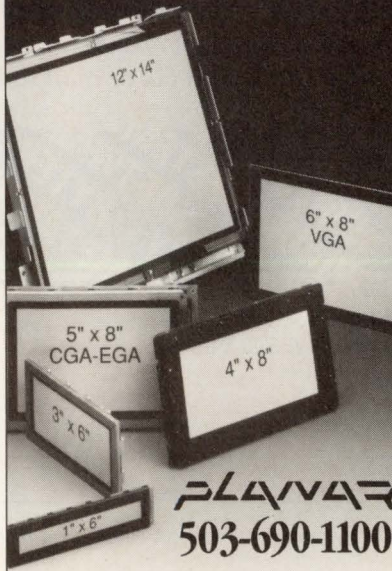
RAG Electronics Inc, 21418 Parthenia St, Canoga Park, CA 91304. **Circle No. 372**

Listing Of Nanosecond Waveform Generators

This 113-pg catalog mentions more than 300 models of nanosecond waveform generators, including ultrahigh-speed pulse generators, impulse generators, monocycle generators, samplers, delay generators, and accessories. Approximately 40% of the models presented are new, and the book provides an enlarged applications-information section.

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section

1 * 50 300

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EDN

Professional Issues

Your local schools want YOU

Volunteers are needed to improve math and science education.

Jay Fraser, Associate Editor

Remember when you were in high school and those people came in to talk about careers? You probably saw an airline pilot and a nurse and maybe even an engineer. The engineer spoke briefly about what he did, and you didn't understand very much of it. Then he left, and you never saw him again. Years ago, that was considered volunteering in the schools.

Today volunteer programs are much more sophisticated and much more important. The problems besetting the American educational system are well known—falling test scores, American students ranking far behind foreign students in science and math, and fewer American students going into engineering every year. American schools need to be revitalized, and engineers are being called upon to help.

On February 19th of this year, the two honorary cochairmen of the National Coalition of Engineering Societies for Precollege Mathematics and Science Education met with President George Bush in the Oval Office of the White House. They presented him with a nine-foot scroll that included the signatures of the presidents and executive directors of the 41 national engineering societies that make up the Coali-

tion. At the meeting they announced their goal of recruiting 100,000 volunteer engineers to help in improving math and science edu-

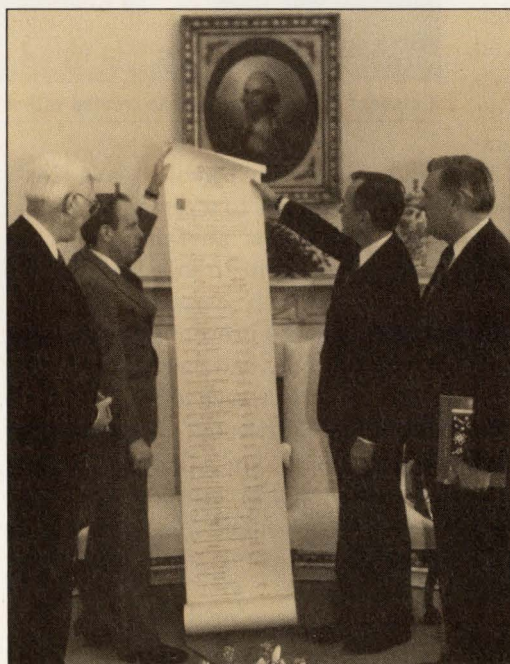
No one has attempted a volunteer program on this scale before, and it will require some real effort from the engineers who choose to join it.

"We're not interested in having someone come into a school one time and do a Mr. Wizard or a Mr. Math," says Lee DeLorme, the acting executive director of Engineers for Education. "We're asking our volunteers to make a long-term commitment. Commitment is the key to the program."

One of the nagging problems with volunteer programs in the past was that engineers and teachers sometimes didn't coordinate their efforts. The engineers would give demonstrations that had little to do with the course, or, worse yet, try to take on the role of teacher.

"I think the focus shouldn't be on teaching," says DeLorme. "Rather, the volunteer should be an added resource for the

teacher and the school. The role that the volunteer assumes in the school—tutor or adviser or whatever—should be done, not in a vacuum, but in consultation and agree-



President Bush and Dr. Lawrence P. Grayson, chairman of Engineers for Education, hold up a scroll listing the 41 engineering societies pledged to improving math and science education.

cation. The Coalition, better known as Engineers for Education, wants to make an engineer available to every elementary and secondary school in the United States.

Professional Issues

ment with the individual teacher. Once they determine what the school needs and what the engineer can contribute, then they can develop an effective program."

DeLorme says the response to Engineers for Education has been surprisingly quick and very gratifying. During the first three months following the formal announcement of the program at the White House, more than 500 engineers have called the hot line and volunteered.

As Engineers for Education has expanded its working relationship with industry, it has found that many high-tech companies already support various volunteer programs, and many engineers already donate their time to local schools. Hewlett-Packard, for example, is involved in dozens of volunteer programs around the country.

Russ Herrell is an electrical engineer who works in the research and development laboratory at Hewlett-Packard's facility in Fort Collins, CO. He's also the chairman of the steering committee of the Visiting Scientists program, which pairs up a company scientist or engineer with a teacher in one of the local schools. The program was founded in 1983 and has been very popular with both students and teachers.

Herrell says that the program benefits teachers because they see demonstrations that give insights into applications of some of the things they're teaching. "At the high-school level, teachers are aware they're teaching skills—computer skills or engineering skills—but they don't know how they're applied. A little hands-on demonstration of the fruit of the labor usually goes over very well with the students, too. Students are always awed by some of the fancier technologies that we can bring into the classroom to show them," he says.

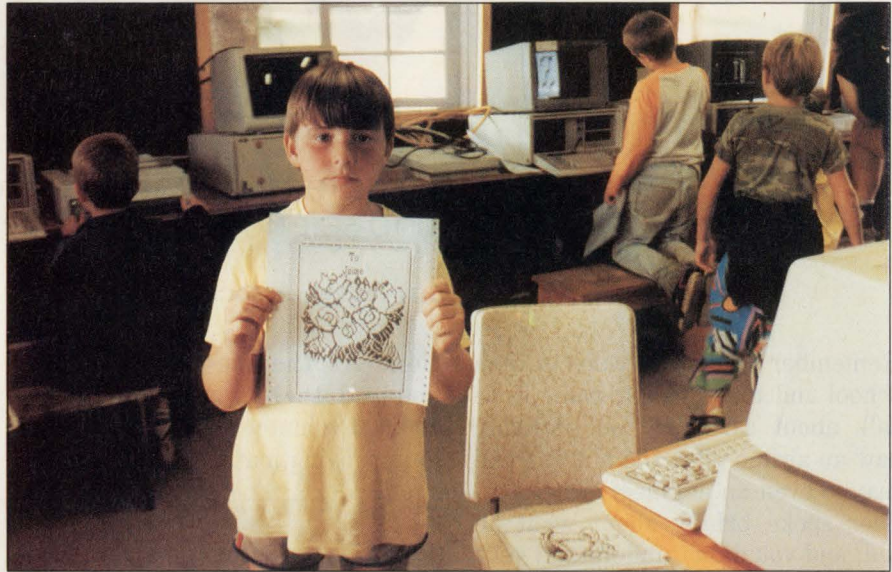
Engineers who volunteer in

schools have an important function that goes beyond giving demonstrations or even teaching. They are also role models for the students.

"When I was growing up, an engineer was someone like Steven Douglas on 'My Three Sons.' What

be improved if a company has flex time or if it simply gives its engineers the time off they need.

Another problem is the lack of a comprehensive, national plan for improving the schools. Volunteering helps bring industry and educa-



A student displays a picture he created with a computer after only a few hours of instruction.

did he do? I didn't know," says Herrell. "If you get to a certain age and you don't know anything about a topic, you begin to lose interest in it. You mentally close the door on it. We want to prevent that.

"We actually had one female engineer go into a second-grade class, and a little girl came up to her and said, 'Gee, I don't think I can be an engineer. I'm a girl.' Where did she get that idea? We do a lot of good just by being role models."

Volunteers face problems

There are problems involved in volunteering beyond making sure the engineer is working closely with the teacher and is contributing something meaningful to the class. First among the complaints is that there's never enough time. Business hours aren't the same as school hours, and it's sometimes difficult for engineers to get away in the middle of the day. The situation can

tion closer together, but the local, state, and federal government also have a role to play.

One of the most persistent problems is the difficulty in measuring results. Students' test scores don't give an accurate picture of the effectiveness of a volunteer program because so many other factors are involved. The people who run the programs usually don't attempt a strict quantitative analysis of the students' progress. They have other ways of measuring success.

"We get many letters from teachers expressing their appreciation, and we've had several incidents of students who have decided to go into engineering because of our activities," says Herrell. "One of the things we feel is a measure of success is the number of pairings (between an engineer and a teacher) that have continued the next year. We figure that if the teachers feel they're getting something out of it

and the engineers feel they're getting something out of it, then they must be doing something successfully."

Like Hewlett-Packard, IBM supports many volunteer programs around the country. An unusual one took place at a summer camp in Fairlee, VT, and was funded by the state. Last year three IBM employees taught children eight to thirteen years old how to use a computer. Many of them were the sons and daughters of migrant farm workers and had never seen a computer before. Penny Swank, a systems analyst, was one of the volunteer instructors.

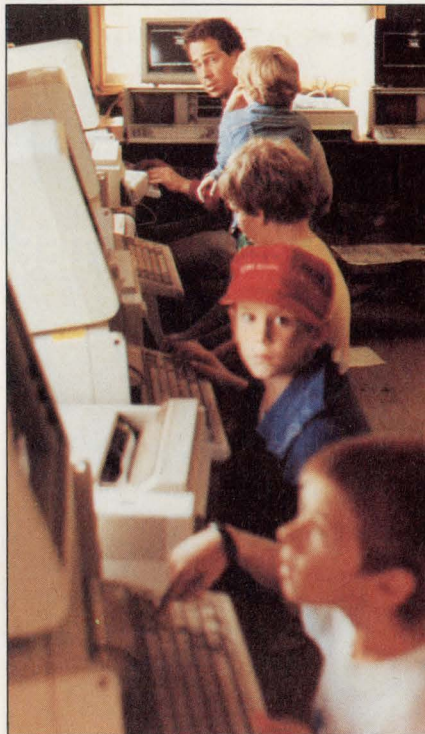
A feeling of accomplishment

"We tried to give the students some confidence with computers," she says. "We provided programs so they could walk out of that room having produced something, whether it was a greeting card or a picture or a banner. The idea was to give them the feeling they could accomplish something using a computer."

The camp took in 80 to 90 children and had a network of 10 computers. Students were given at least one hour of instruction each week, and they could also work with the computers in their spare time. The computer room quickly became one of the most popular places in the camp.

"We had to schedule hours for it to be closed so we wouldn't be totally inundated with kids," says Swank. "There was a lot of work that had to be done to prepare the curriculum from day to day, and we just had to close the room to do that work. In fact, after we put the kids to bed at 10 o'clock, we worked until one or two in the morning getting ready for the next day.

"There's no way to give a child a computer-science education when you only have a few hours. Our goal was to give the children some sort



A volunteer instructor works with children in the computer room at a summer camp in Fairlee, VT.

of confidence level with the computer, particularly those who were afraid when they came in. The idea was to give them an opportunity to

achieve some sort of success, and I think we did that. It was an excellent program."

Not all stories about volunteer programs have happy endings. Last year the state of Vermont withdrew its funding for the camp. Unless the director can raise money from another source, it will close permanently.

Some professional organizations sponsor volunteer programs. The National Society of Professional Engineers (NSPE), for example, runs MathCounts, a series of competitions between teams of seventh and eighth graders from around the country that culminates in a national championship each May in Washington, DC. The purpose of MathCounts is to build mathematics skills and promote strategic problem solving among students. More than 8000 volunteers from the NSPE donate their time to the program each year as organizers, coaches, and administrators.

The Junior Engineering Technical Society (JETS) sponsors academic competitions among high-school students, engineering design

You can help

The organizations listed sponsor nationwide programs aimed at improving precollege science and math education. Write or phone them to find out about the activities near you and how you can help.

Engineers for Education
American Association of
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1111 19th St NW, Suite 608
Washington, DC 20036
(800) 489-0348

Science Olympiad
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American Chemical Society
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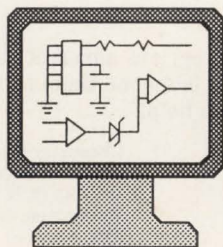


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Professional Issues

contests, and a national engineering aptitude search. The aptitude search is a guidance test that helps students evaluate their chances of success if they choose to go to engineering school. JETS has been running these programs for 40 years. Other professional organizations also support precollege educational activities (see **box**, "You can help").

You don't have to work for a large high tech firm or belong to a professional organization to help improve our schools, however. You can make a contribution by doing something as simple as attending a meeting of your local school board. You understand what kind of preparation a student needs to succeed in engineering school or in a technical profession. Talk to your school administrators and teachers and make sure that your schools are providing sufficient instruction in science and math. You can help, but first you have to become involved.

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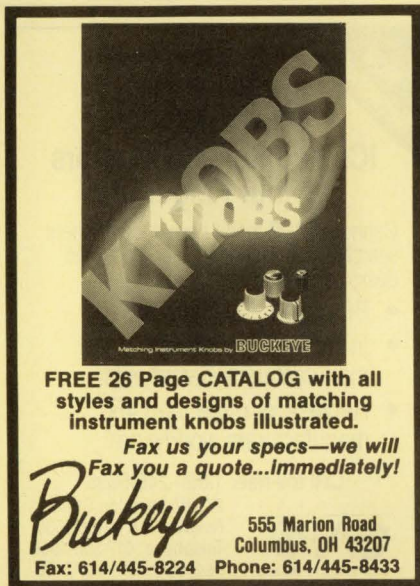
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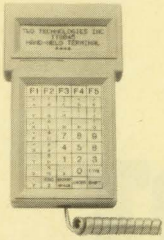
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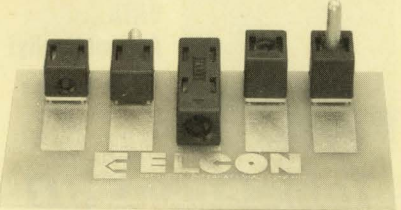
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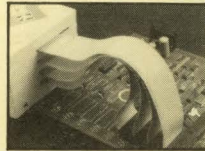
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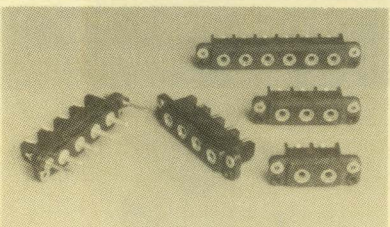
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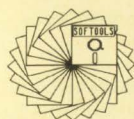
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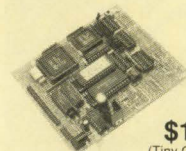


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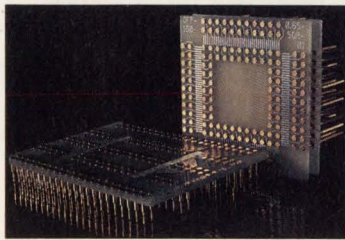
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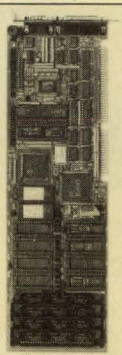
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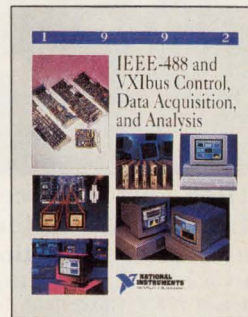
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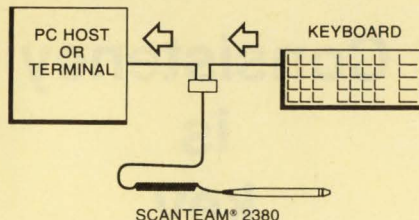
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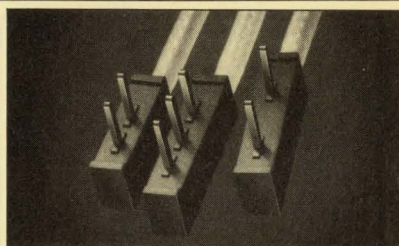
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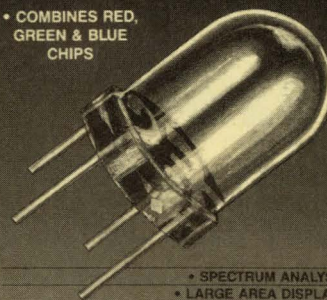


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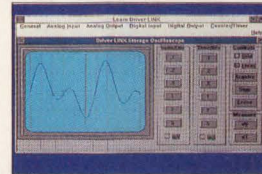
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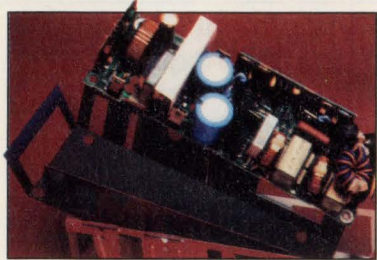
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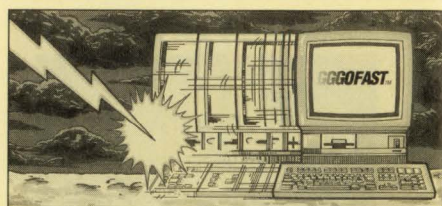
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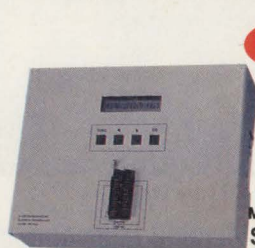
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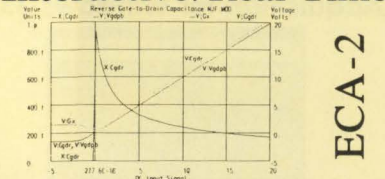
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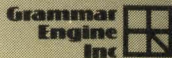
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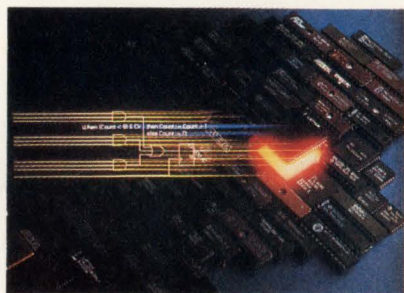
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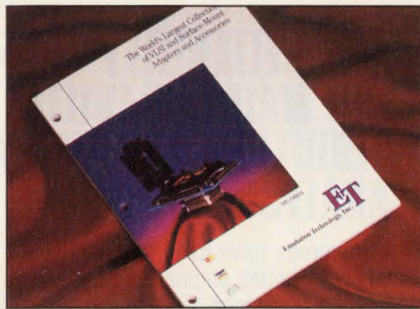
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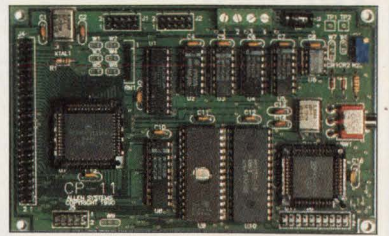


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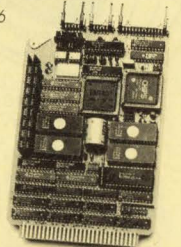
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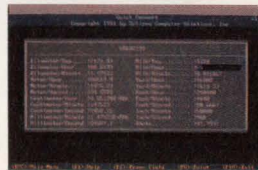
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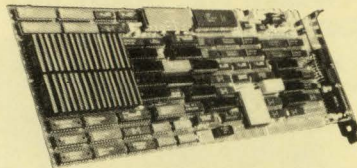
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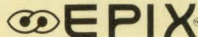
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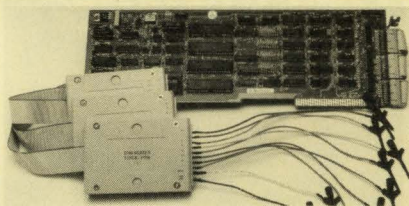
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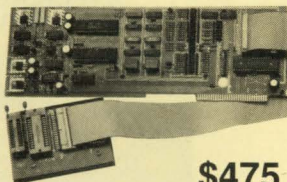
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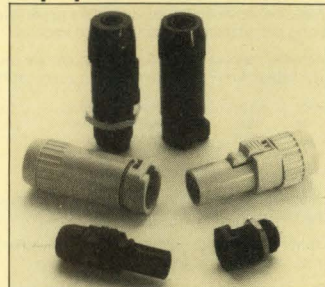
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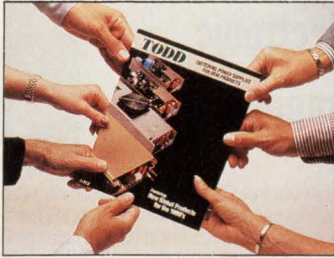
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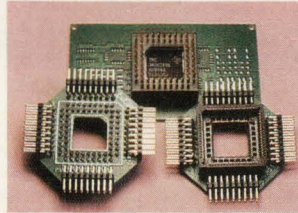
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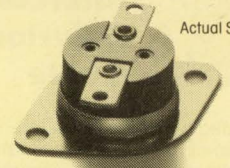
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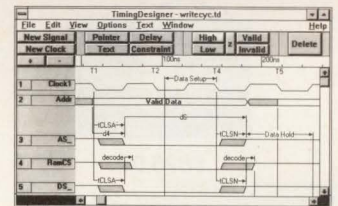
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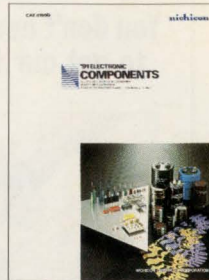


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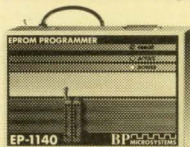
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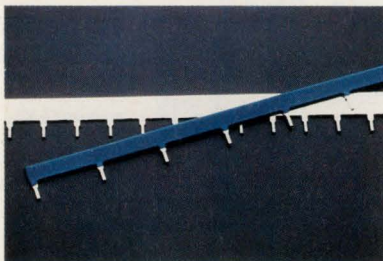
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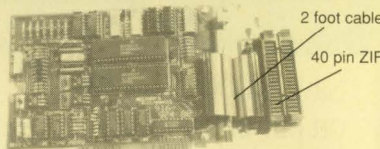
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Magazine Edition	Oct. 24	Oct. 3	Telecommunications ICs, Graphics & Video Circuits, Computers & Peripherals, Software, Wescon Preview Issue
Magazine Edition	Nov. 7	Oct. 17	High Performance DSPs • CAE/ASICs, Computers & Peripherals/Communications, Software, Wescon Show Issue
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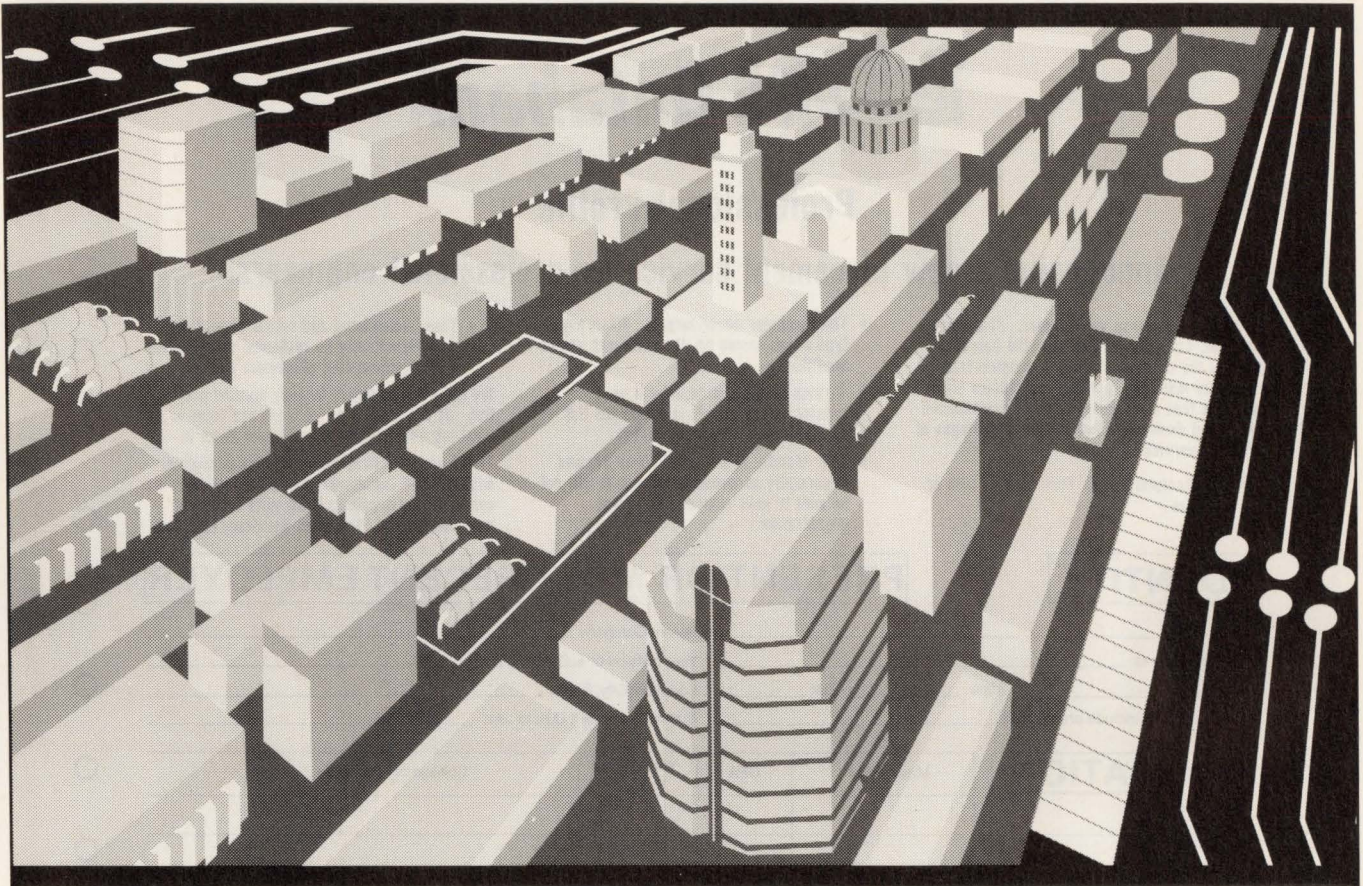
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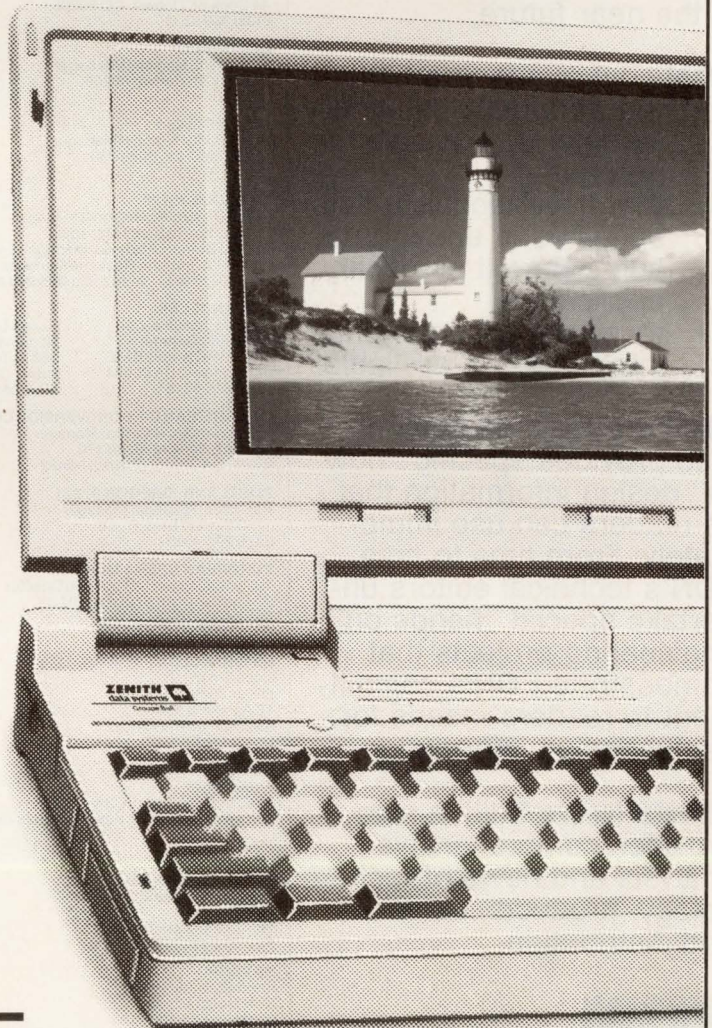
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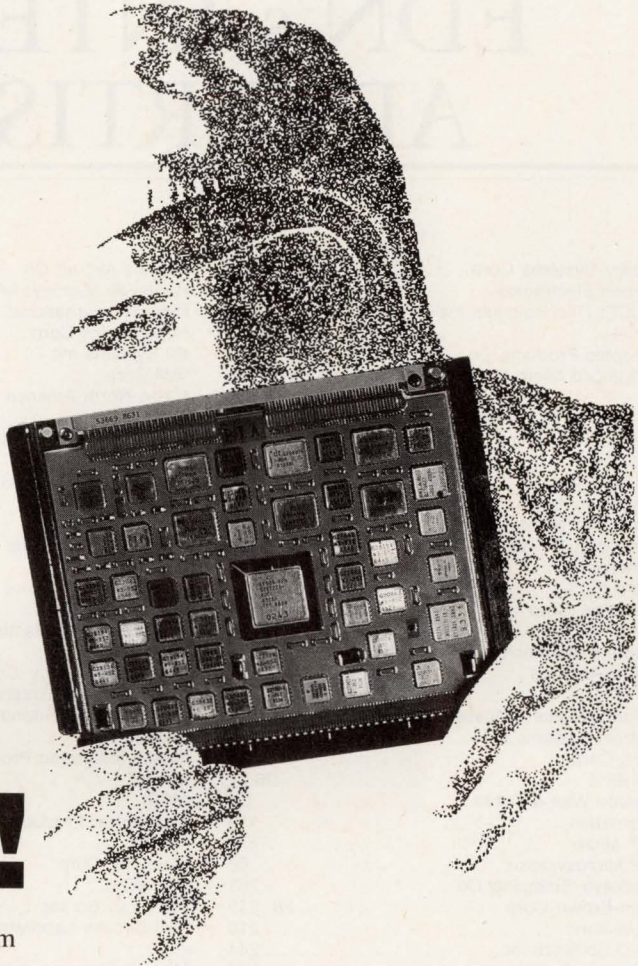
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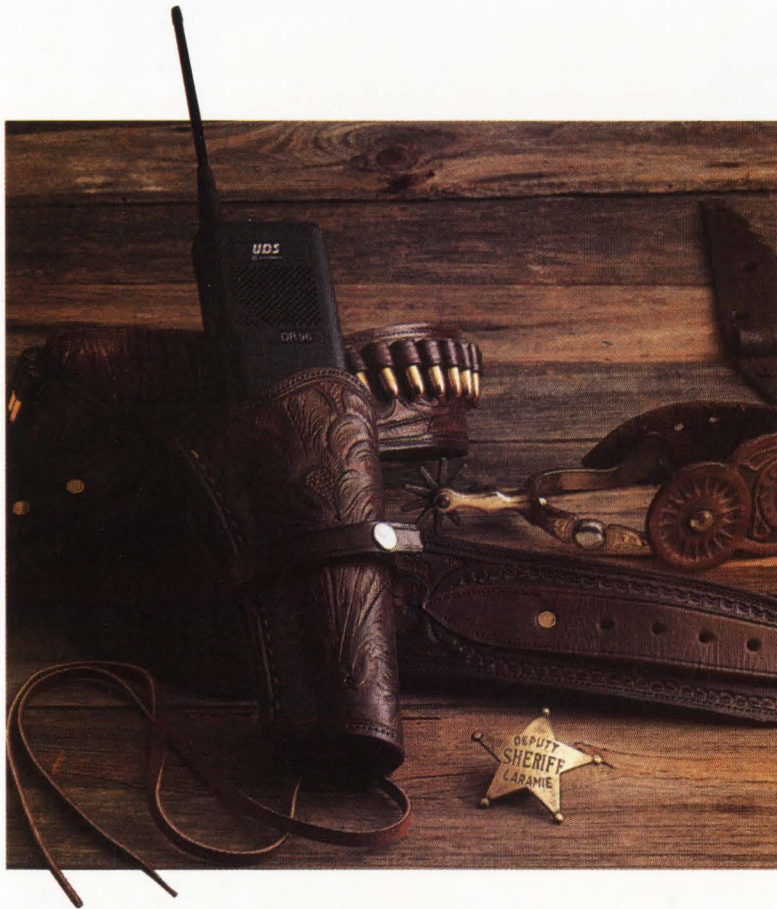
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