A CAHNERS PUBLICATION

FEBRUARY 4, 1991

EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report:

Competitive 3½-in. hard-disk drives erode demand for larger units

pg 72

Complete Family Of High Performance D/A Converters

Burr-Brown offers one of the industry's most complete line of high performance digital-to-analog converters. High quality and reliability are assured by our 35+ years of microcircuit design and manufacturing experience. Key features include:

- wide selection of 12-bit, 16-bit, and 18-bit resolution DACs with many performance options
- μprocessor-compatible DACs with double-buffered latches
- zero-chip interface DACs for digital signal processing and digital audio applications
- low cost, low power, CMOS DACs
- variety of package options

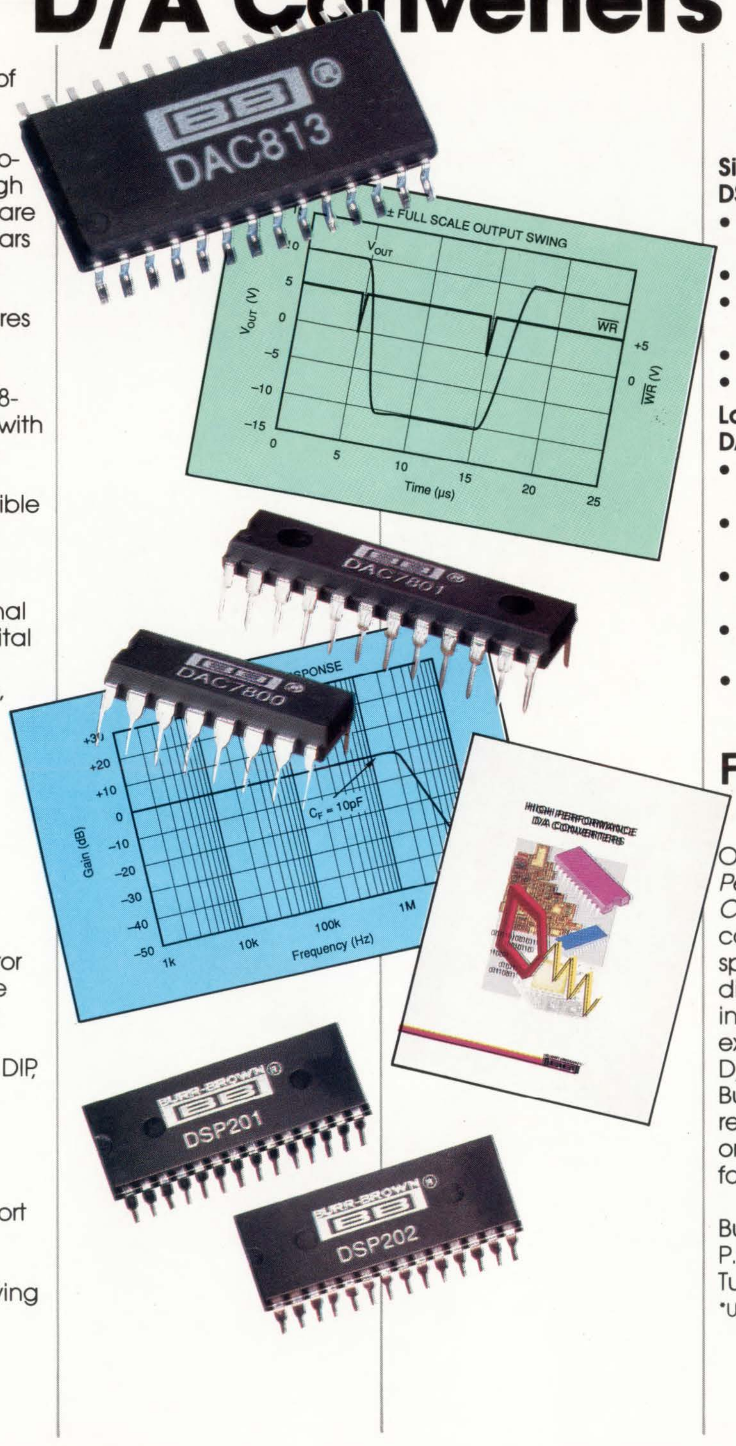
New Family Members

Complete 12-Bit DAC813

- ±1/2LSB linearity error
- μprocessor interface
- 270mW max power dissipation
- compact 0.3″ wide DIP, SOIC
- from $11.90*

Dual 12-Bit CMOS DAC7800/01/02

- 8-bit, 12-bit, serial port interface
- single +5V supply
- 4 quadrant multiplying
- 0.3″ wide DIP, SOIC
- From $12.35*



Single/Dual 18-bit DSP201/202

- zero-chip interface to most popular DSP ICs
- 500kHz update rate
- 90dB Signal-to-Noise +Distortion
- -92dB THD
- from $24.95*

Low Power, 12-Bit DAC667

- drop-in AD667 replacement
- 390mW max power dissipation
- fast 60ns digital interface
- ±10V $_{out}$ on ±12V to ±15V supplies
- From $11.90*

Free Selection Guide

Our new *High Performance D/A Converters* guide contains key product specs, performance diagrams, applications information and examples of our newest D/A converters. Ask your Burr-Brown sales representative for a copy, or call **1-800-548-6132** for immediate assistance.

Burr-Brown Corp.
P.O. Box 11400
Tucson, Az 85734

*U.S. OEM prices, in 100s.

BURR-BROWN®

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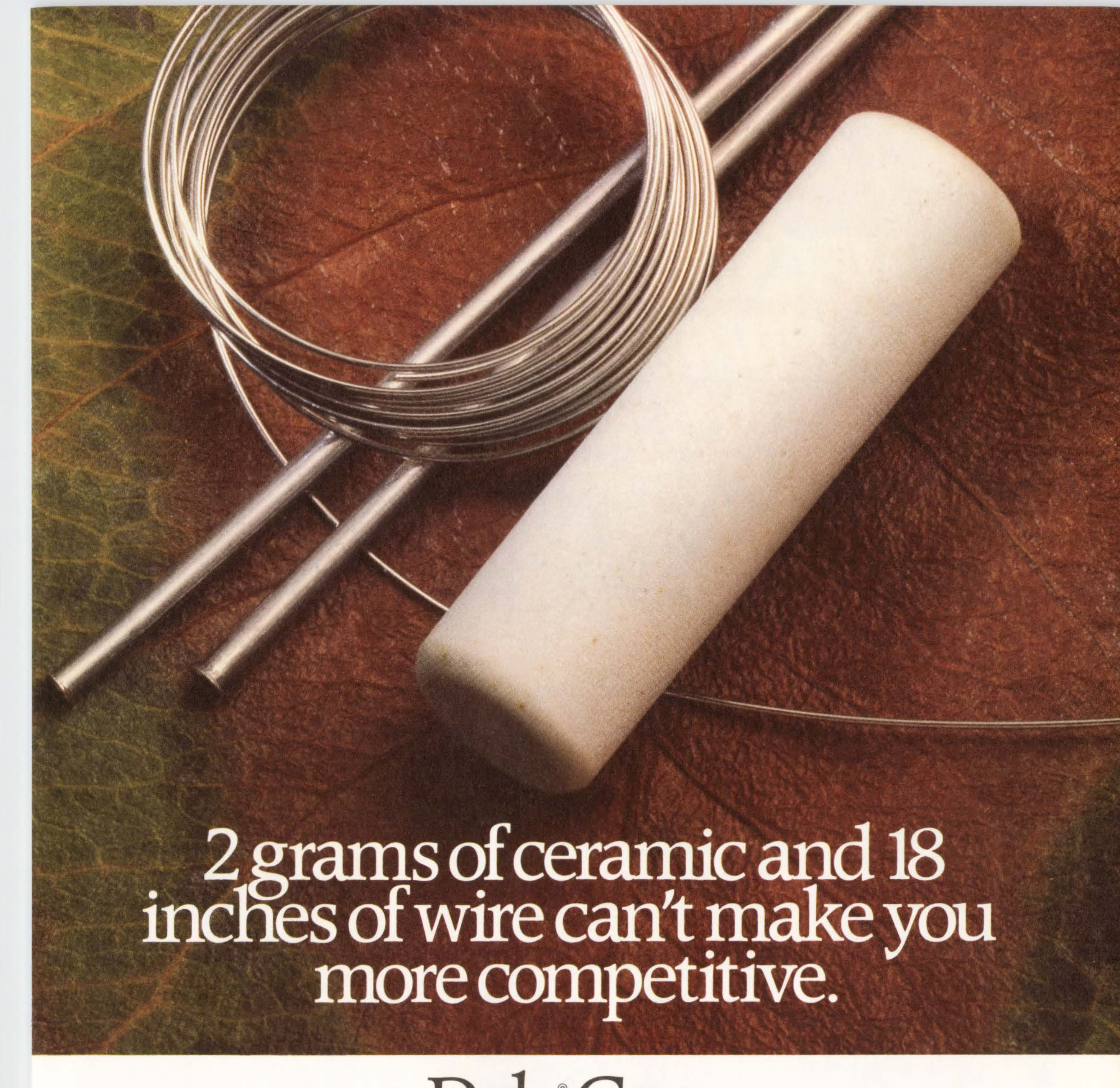

Dale® Can.

There's only one real reason to specify Dale® wirewound resistors: We'll work harder turning something common into something uncommonly valuable. Up front, that means saving you selection time by producing every standard shape and size in the book. Plus, we give you immediate access to design assistance and a wide range of proven special products.

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And, it means making reliability

the least of your worries with well-established Statistical Process Control and Quality Assurance systems to give you ship-to-stock capability.

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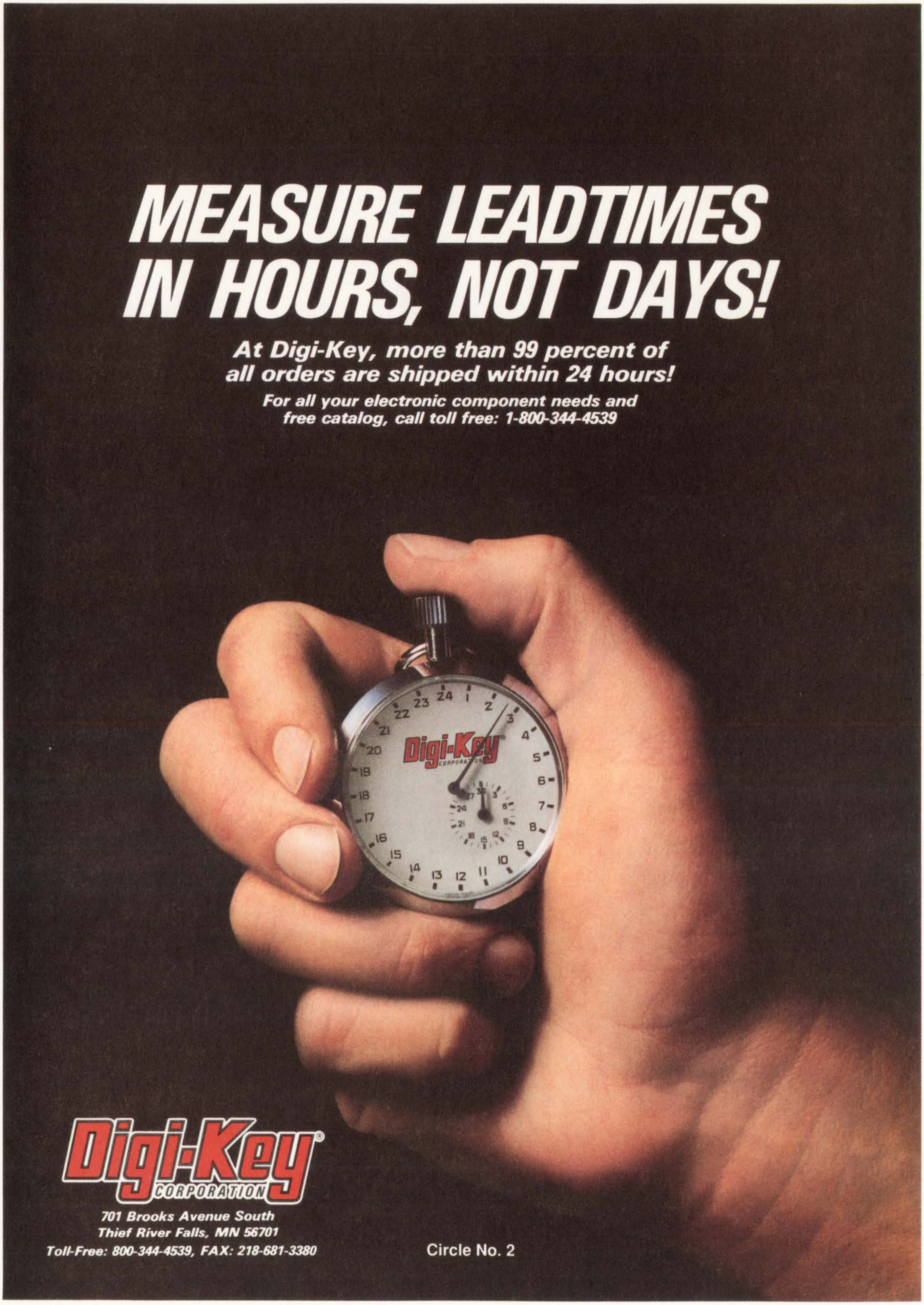
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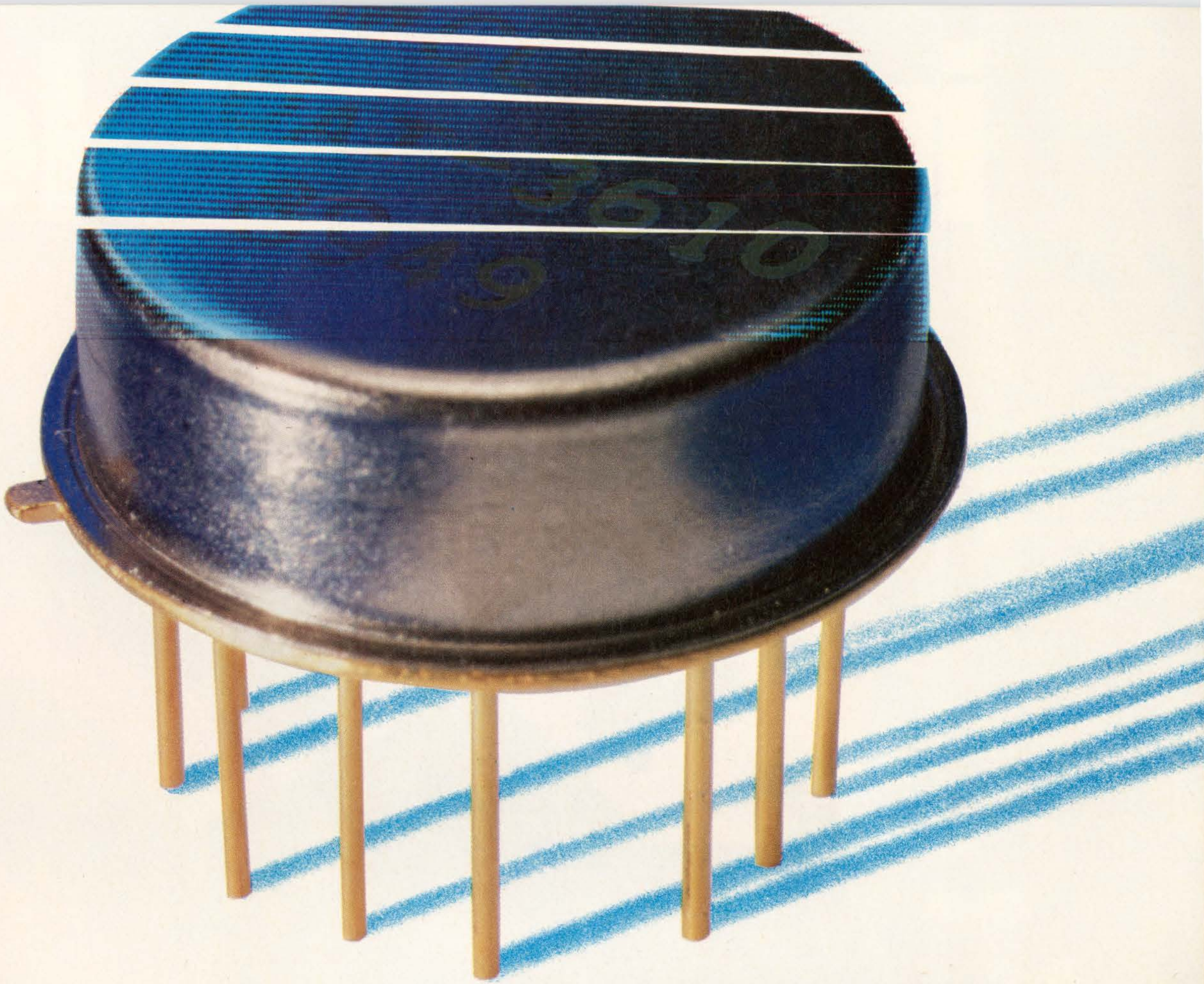
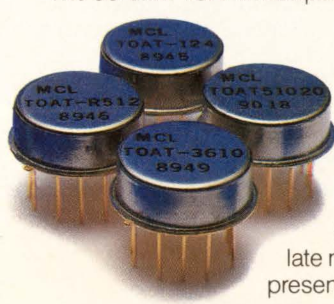


PRECISION TTL-CONTROLLED ATTENUATORS

up to 35dB
10 to 1000MHz
only **$59⁹⁵**

Now...precision TTL-controlled attenuators accurate over 10 to 1000MHz and −55 to +100°C. Four models are available in the new TOAT-series, each with 3 discrete attenuators switchable to provide 7 discrete and accurate attenuation levels (see chart). Cascade all four models for up to 64.5dB control in 0.5dB steps. Custom values available on request. The 50-ohm TOAT-series performs with 6μsec switching speed and can handle power levels up to 0dBm. Units are housed in a rugged hermetically-sealed TO-8 package to withstand the shock, vibration, and temperature stresses of MIL-STD-883. Connector versions are available. Take advantage of the $59.95 (1-9 qty) price breakthrough to stimulate new applications as you implement present designs and plan future systems.



TOAT-R512 Accuracy		TOAT-124 Accuracy		TOAT-3610 Accuracy		TOAT-51020 Accuracy	
(dB)	(+/−dB)	(dB)	(+/−dB)	(dB)	(+/−dB)	(dB)	(+/−dB)
0.5	**0.12**	**1.0**	**0.2**	**3.0**	**0.3**	**5.0**	**0.3**
1.0	**0.2**	**2.0**	**0.2**	**6.0**	**0.3**	**10.0**	**0.3**
1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

bold faced values are individual elements in the units

finding new ways...
setting higher standards

CIRCLE NO. 110

Mini-Circuits

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P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156

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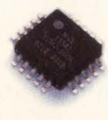
SPDT switch dc to 5GHz with built-in driver

Truly incredible…a superfast 3nsec GaAs SPDT reflective switch with a built-in driver for only $19.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' YSW-2-50DR?

Check the outstanding performance specs of the rugged device, housed in a tiny plastic case, over a -55° to +85° C span. Unit-to-unit repeatability for insertion loss is 3-sigma guaranteed, which means less than 15 of a 10,000-unit production run will come close to the spec limit. Available for immediate delivery in tape-and-reel format for automatic placement equipment.

SPECIFICATIONS YSW-2-50DR	dc-500MHz	500-2000MHz	2000-5000MHz
Insertion loss, typ (dB)	0.9	1.3	1.4
Isolation, typ(dB)*	50	40	28
1dB compression, typ (dBm @ in port)	20	20	24
RF input, max dBm (no damage)	22	22	26
VSWR (on), typ		1.4	
Video breakthrough to RF, typ (mV p-p)		30	
Rise/Fall time, typ (nsec)		3.0	



*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

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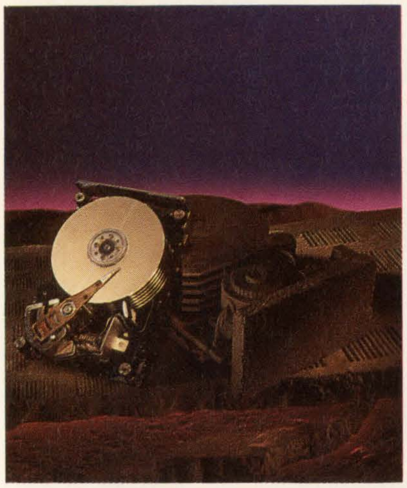
Volume 36, Number 3

EDN® Magazine Edition

February 4, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *The trends that are sculpting the hard-disk-drive market—higher capacities, faster operation, lower prices—are embodied in the latest round of 3½-in. devices. See our Special Report beginning on pg 72. (Photo courtesy Conner Peripherals Inc; design by Greg Meadows and Ken Camozzi, Meadows Graphic Arts Inc; models by Steve Pombo, Pombo Enterprises; photography by Tim Tabke, Phoenix Productions)*

Continued on page 7

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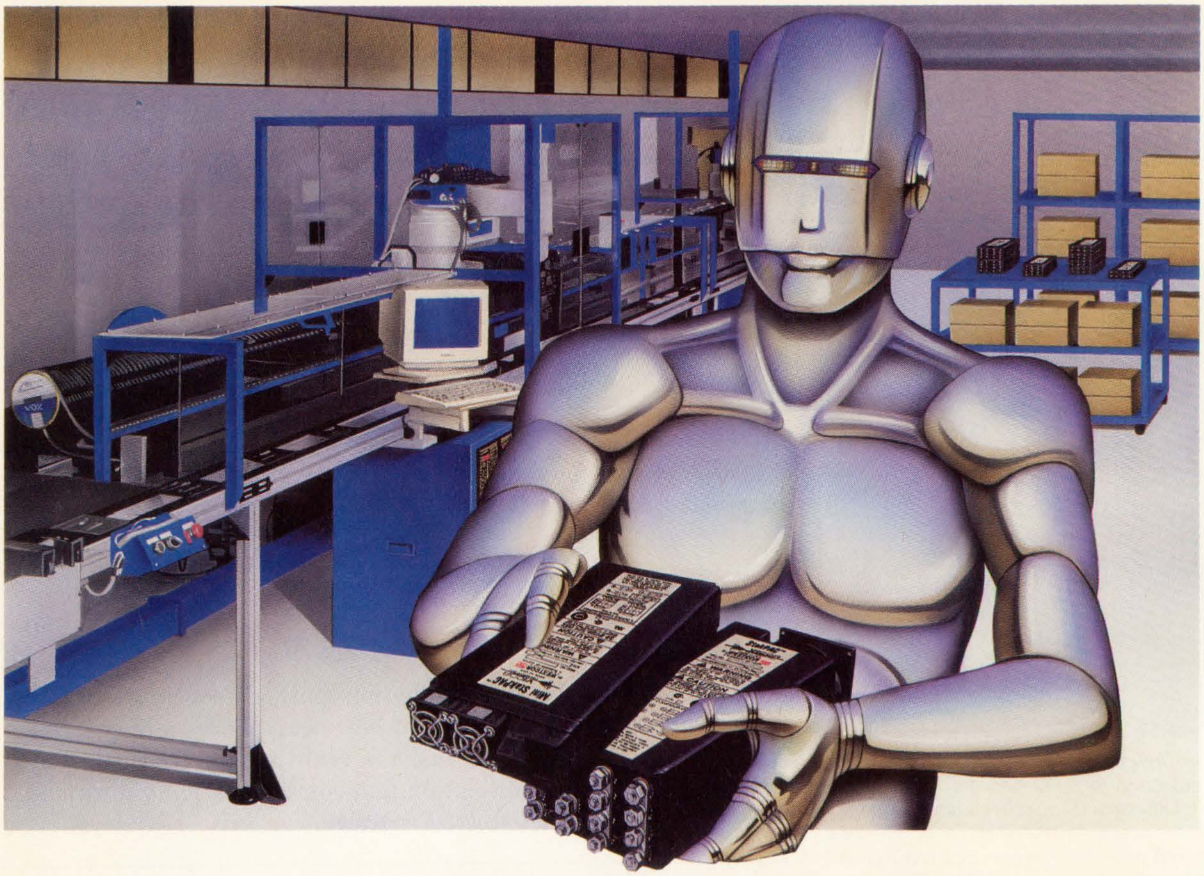

RoboPower

STAKPAC™		MINI STAKPAC™
1200 Watts	**Power**	600 Watts
110/220 VAC	**Input**	110/220 VAC
Up to 8	**Outputs**	Up to 5
3.2"x5.5"x11.5	**Dimensions**	1.9"x5.5"x12"
Fan-Cooled	**Cooling**	Twin Fans

Each StakPAC output is factory configured utilizing Vicor's robotically manufactured power converters...VI-200 series modules. Consider the advantages of a StakPAC customized for your system needs with automized power modules:

USER DEFINABLE OUTPUTS— The use of proven standard catalog modules offers the features of a custom without the associated risk or investment.

STANDARD MODELS—Many preconfigured standards available.

QUICK DELIVERY—Typical delivery 1 week or less for custom or standard evaluation units.

COMPACTNESS—Low profile packages provide up to 6 watts/cubic inch, twice the industry norm.

UL, CSA, TUV SAFETY AGENCY APPROVAL— All StakPAC configurations are approved, standard or custom.

EMI—FCC/VDE Level A, conducted.

StakPACs are designed and built by Westcor Corporation, Los Gatos, CA, a Vicor subsidiary. StakPACs are sold world-wide through Vicor Corporation, Andover, MA.

STAKPAC STANDARDS
1200 WATT MODELS

Total output power may not exceed 1200* watts for any model, single or multiple output. Lower power StakPAC models and many other configurations are available. *Standard models supply 1100 watts; high-powered version 1200 watts. Please contact the factory.

Model	Output Voltage (VDC) and Maximum Current (amperes) per Channel #1	#2	#3	#4	#5
Single Output					
SP1-1801	2 @ 240				
SP1-1802	5 @ 240				
SP1-1603	12 @ 100				
SP1-1604	15 @ 80				
SP1-1605	24 @ 50				
SP1-1606	28 @ 42				
SP1-1607	48 @ 25				
Dual Output					
SP2-1801	2 @ 120	5 @ 120			
SP2-1802	5 @ 120	5 @ 120			
SP2-1803	5 @ 120	12 @ 66			
SP2-1804	12 @ 66	12 @ 66			
SP2-1805	15 @ 53	15 @ 53			
Triple Output					
SP3-1801	5 @ 180	12 @ 16	12 @ 16		
SP3-1802	5 @ 150	12 @ 33	12 @ 16		
SP3-1803	5 @ 180	15 @ 13	15 @ 13		
SP3-1804	5 @ 150	15 @ 26	15 @ 13		
Quad Output					
SP4-1801	5 @ 150	12 @ 16	12 @ 16	5 @ 30	
SP4-1802	5 @ 150	15 @ 13	15 @ 13	5 @ 30	
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24 @ 8	
SP4-1804	5 @ 150	15 @ 13	15 @ 13	24 @ 8	
Five Output					
SP5-1801	5 @ 120	12 @ 16	12 @ 16	5 @ 30	24 @ 8
SP5-1802	5 @ 120	15 @ 13	15 @ 13	5 @ 30	24 @ 8
Seven Output					
SP7-1801	5 @ 60	12 @ 16	12 @ 16	24 @ 8	24 @ 8
	#6	#7			
	5.2 @ 28	2 @ 30			

MINI STAKPAC STANDARDS
600 WATT MODELS

Total output power may not exceed 600 watts for any model, single or multiple output. Lower power Mini StakPAC models and many other configurations are available. Please contact the factory.

Model	Output Voltage (VDC) and Maximum Current (amperes) per Channel #1	#2	#3	#4	#5
Single Output					
ST1-1401	2 @ 120				
ST1-1402	5 @ 120				
ST1-1301	12 @ 50				
ST1-1302	15 @ 40				
ST1-1303	24 @ 25				
ST1-1304	28 @ 21				
ST1-1305	48 @ 13				
Dual Output					
ST2-1401	2 @ 60	5 @ 60			
ST2-1402	5 @ 60	5 @ 60			
ST2-1403	5 @ 60	12 @ 33			
ST2-1404	12 @ 33	12 @ 33			
ST2-1405	15 @ 26	15 @ 26			
Triple Output					
ST3-1401	5 @ 60	12 @ 16	12 @ 16		
ST3-1402	5 @ 60	15 @ 13	15 @ 13		
ST3-1501	5 @ 90	12 @ 8	12 @ 8		
Quad Output					
ST4-1401	5 @ 30	12 @ 16	12 @ 16	5 @ 30	
ST4-1402	5 @ 30	15 @ 13	15 @ 13	5 @ 30	
ST4-1403	5 @ 30	12 @ 16	12 @ 16	24 @ 8	
ST4-1501	5 @ 30	15 @ 13	15 @ 13	24 @ 8	
ST4-1502	5 @ 60	12 @ 16	12 @ 8	5 @ 15	
ST4-1503	5 @ 60	15 @ 13	15 @ 7	5 @ 15	
ST4-1504	5 @ 60	12 @ 16	12 @ 8	24 @ 4	
ST4-1505	5 @ 60	15 @ 13	15 @ 7	24 @ 4	
Five Output					
ST5-1501	5 @ 30	12 @ 16	12 @ 16	5 @ 15	24 @ 4
ST5-1502	5 @ 30	15 @ 13	15 @ 13	5 @ 15	24 @ 4

For ordering information call Vicor Express at 1-800-735-6200 or (508) 470-2900 at ext. 265.

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CIRCLE NO. 98

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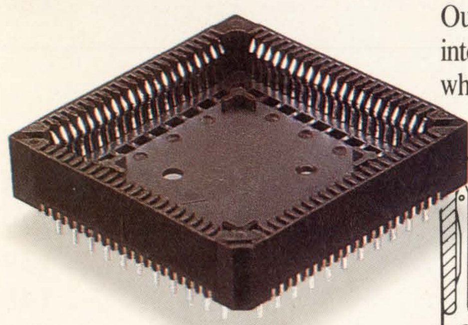
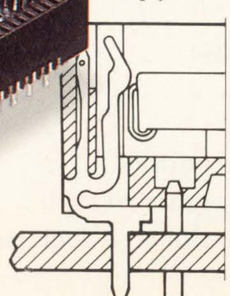
A chip carrier socket that won't play "pop goes the circuit."



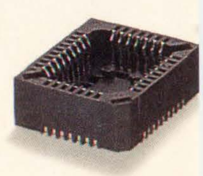
Our sockets are designed to get solidly into contact and stay in contact. No matter what the outside influences. Pop-out is simply not a problem.



Controlled contact interface angle in AMP HPT sockets ensures positive chip carrier retention. Our exclusive removable housing allows direct inspection of solder joints, and fast repair/replacement of contacts.

The contacts are High Pressure Tin, an AMP proprietary design which creates very high normal forces—a minimum of 200 grams per contact—for maximum retention and reliable interconnection. Short-signal-path contacts float in the housing to accommodate thermal expansion.

Two basic styles of sockets are available: square or 32-position rectangular EPROM and SO-J. Both come in solder



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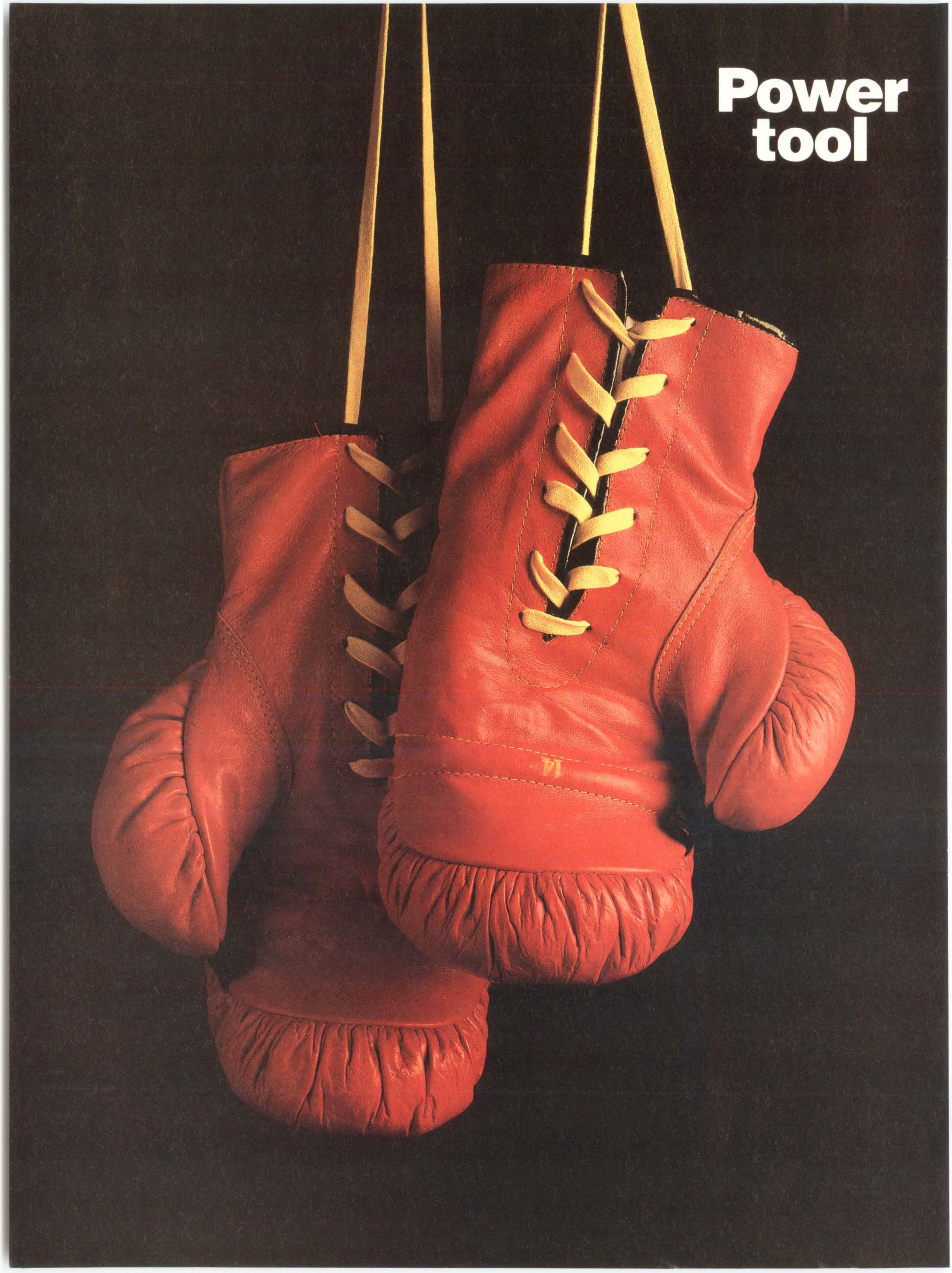
tail or surface mount versions and feature all the important details. Tin-over-nickel plating is applied after the contacts are formed, to assure full plating. We've built in visual indicators for locating pin 1, and polarizing to aid correct insertion.

Orientation holes in the 94V-0 housing floor make registration to the pc board both fast and simple, ideal for hand or tube-loaded robotic insertion. And the high pin counts make very effective use of real estate.

Call the AMP Information Center at 1-800-522-6752 for literature on HPT PLCC Sockets. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas

Seven socket sizes are available, with carrier extraction tools provided for each size.


Power
tool

Power tools

KEPCO TEST/BENCHTOP POWER SUPPLIES

The correct tool makes any job easier. Kepco's Power Supplies for workbench, for burn-in, and float-charging batteries are just some of the tools at your disposal.

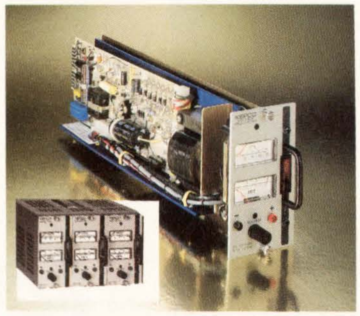
For your workbench choose a multi-out array that you configure for the application by plugging-in modules with adjustable outputs. You can combine one, two or three modules in convenient bench-top housings or put six of them together in a rack. Other experimentalist power includes a nice selection of 100W single output instruments (MSK), a triple output logic-analog model (MPS), and burn-in/float chargers (TBC) that range from 300 to 3000 Watts in all the popular voltages.

Custom power assemblies allow you to create your own toolkit with just the selection of voltage and power to fit your need.

Other power tools from Kepco include: *ac power* to 18KVA, precision *programmable dc* for test applications, *high voltage* models and four-quadrant *bipolar power.* For these, and our broad selection of *switching power* models, including *d-c to d-c converters,* please ask for one of the three catalogs illustrated below.

Instrumentation and Bench | a-c power and d-c bipolar | Switching a-c to d-c and d-c to d-c

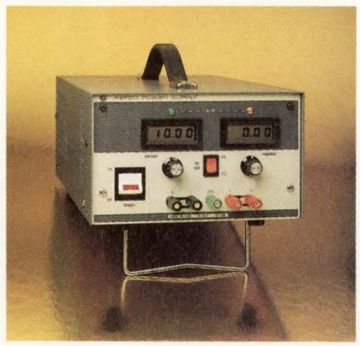
146-1716 | 146-1704 | 146-1692



Plug-in power

- ☐ 20 Watt modules, either voltage stabilizers (series PCX-MAT) or current stabilizers (series CC).
- ☐ Sized to plug-in six abreast in a 19″ rack or in bench-top housings for 1, 2 or 3 units.
- ☐ Mix or match.
- ☐ Select from six voltage ranges up to 100V.

Kepco Group PCX-MAT and CC Power Supplies



100 Watts of precision benchtop power.

- ☐ LCD meters to set the level accurately, a preview feature to check your setting before applying power to your load.
- ☐ Linear design for low-noise high stability.
- ☐ Ten-turn controls for good resolution.
- ☐ Five models offer outputs up to 125 Volts.

Kepco Group MSK Power Supplies

A triple output design for maximum convenience.

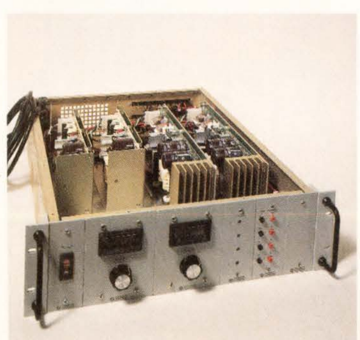
- ☐ 0-6V at 5A for logic and a tracked ± 0-20V, 1A for analog.
- ☐ Each output current limited, the 0-6V output has an overvoltage protector.

Kepco Group MPS Power Supply

Battery/float-chargers.

- ☐ For telecommunications: maintain 12V, 24V and 48V batteries, built-in equalize timer.
- ☐ For burn-in: power up to 3000 Watts, current limited, over-voltage protected. Two output settings, remotely selectable for margining.

Kepco Group TBC Float Chargers/Power Supplies



Kepco Custom System Power Assemblies

We will stuff a 19″ rack (5¼ or 7″) full of switchers to your requirement. With modules from 3 Watts to 3000 Watts, in a wide selection of voltage ranges, we can accommodate most needs.

- ☐ LCD output meters.
- ☐ Test points.
- ☐ Pilots, trimmers, circuit breakers. Convenient ⅛ rack panel format allows multiple control and monitoring.

Kepco Power Assemblies.

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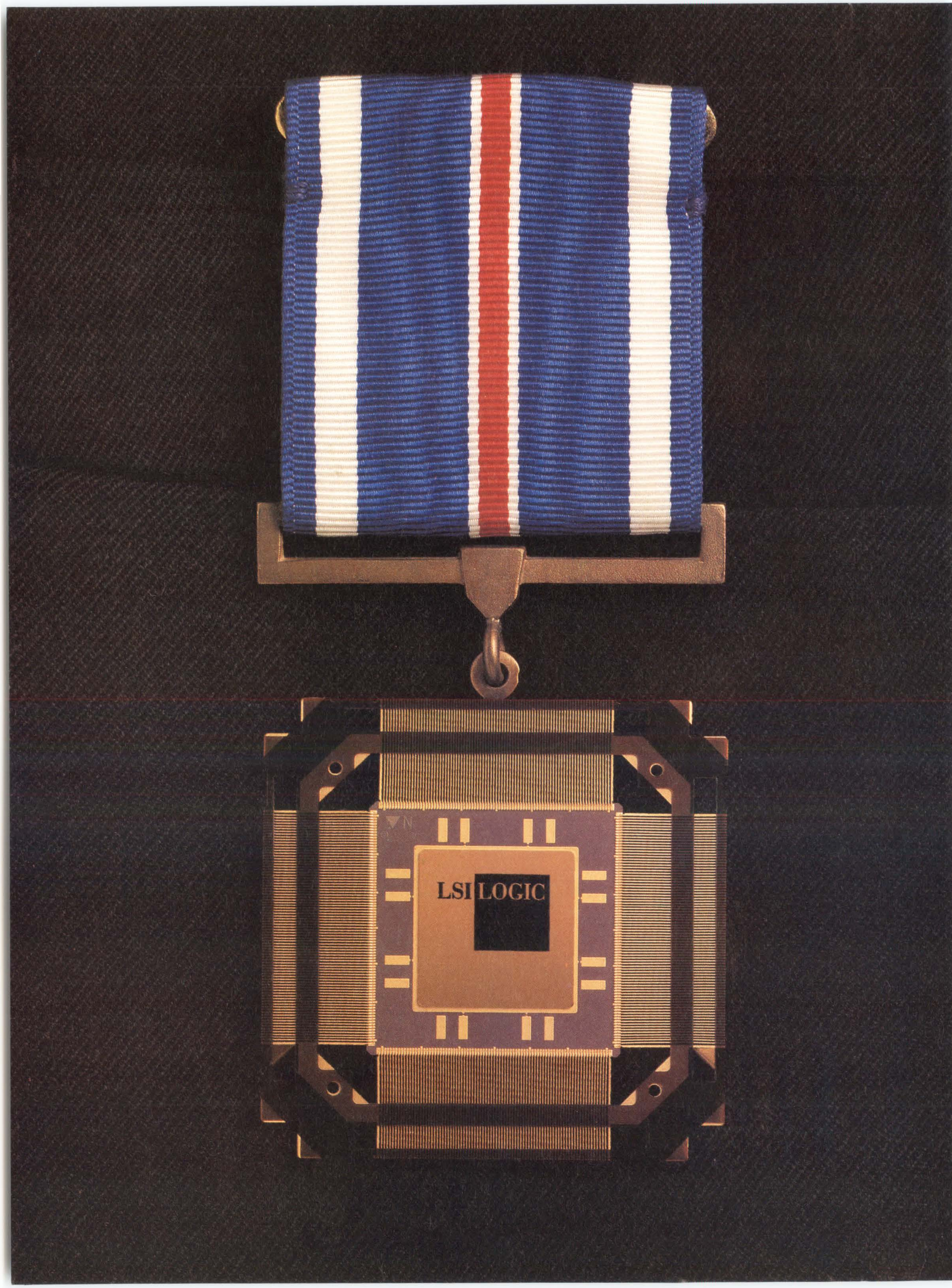
LSI LOGIC

WE'RE STILL ON ACTIVE DUTY.

While many companies have deserted the military ASIC business, our commitment hasn't changed.

So if you're looking for a long term strategic partner, stand at ease.

LSI Logic has earned its stripes by successfully completing more military gate array designs than all other ASIC manufacturers combined. Led by a dedicated Military Aerospace group, we're ready when you are to make those designs a production reality.

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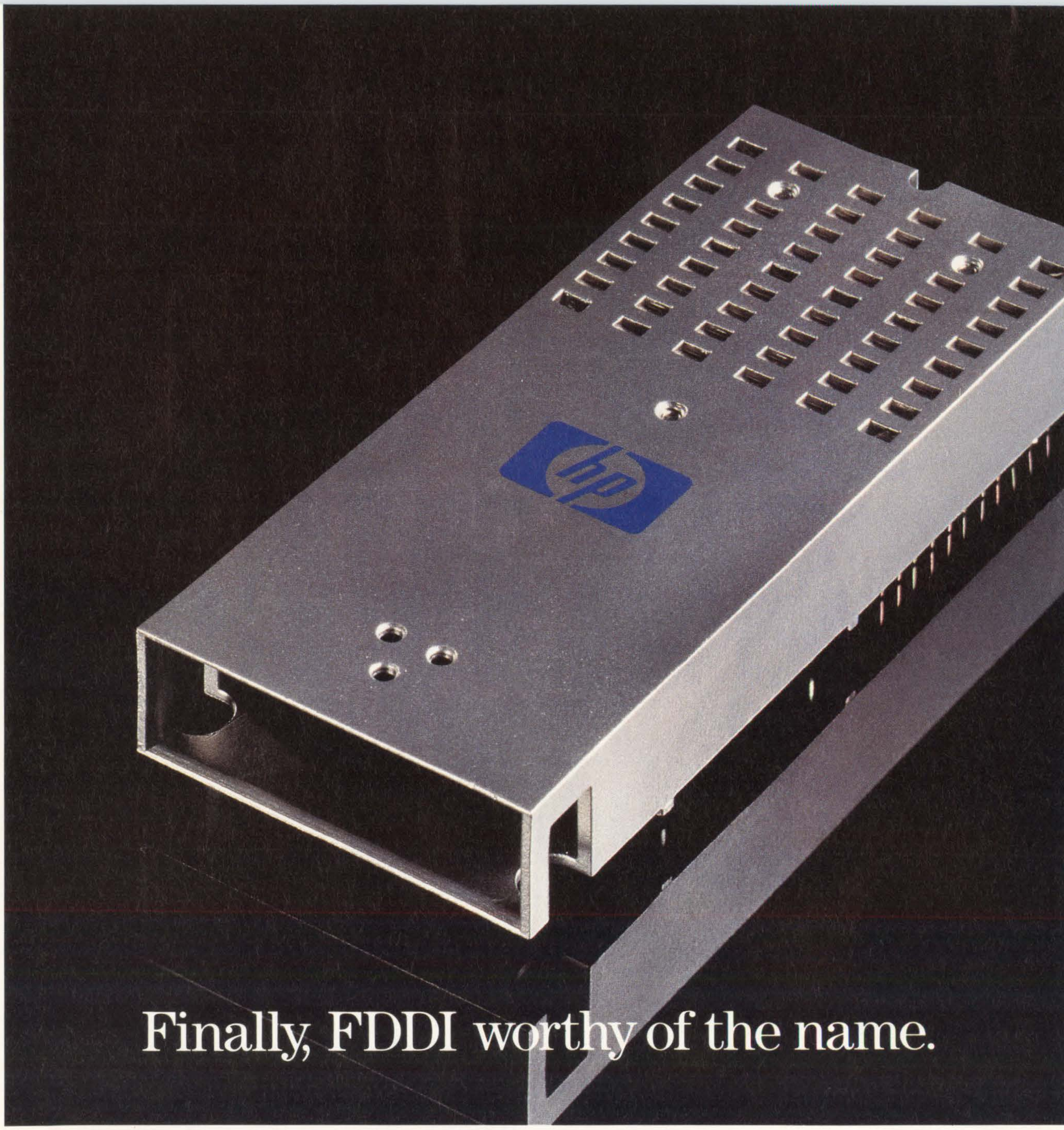

It's one thing to set the standard for an entire industry, as HP helped to do with FDDI. But it's quite another to follow it up with products that set the standard for performance and quality. Of course, that's just the HP way.

Case in point, our new integrated FDDI transceiver with integral MIC receptacle makes the most of its HP heritage. Engineered to meet and beat FDDI standards, this single-piece solution provides consistent performance over a wide range of operating temperatures and voltages. The bottom line is a 14.5dB power budget that exceeds the 11dB FDDI PMD standard, resulting in a comfortable 3.5dB design margin.

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CIRCLE NO. 78

NEWS BREAKS

EDITED BY SUSAN ROSE

COMPANY BREATHES NEW LIFE INTO SILICON CARBIDE

Cree Research has developed proprietary processes for large-diameter, low-defect-density silicon carbide (SiC) wafers. SiC has four basic material properties: wide energy bandgap, high-breakdown electric field, high thermal conductivity, and high saturated-electron-drift velocity. The wide bandgap lets the material emit high-energy wavelength light—blue light—when fabricated into a light-emitting-diode. LED dice cost $0.96 (quantity) and final-packaged blue LEDs cost $1 to $2.

The company will also use the SiC wafers to make high-power, high-temperature, radiation-resistant microwave devices, such as its already tested SiC MOSFET that can withstand temperatures of 650°C, and devices with more complex circuitry than LEDs. Cree Research Inc, Durham, NC, (919) 361-5709, FAX (919) 361-4630.
—Anne Watson Swager

CAHNERS 1991 ECONOMIC FORECAST AVAILABLE TO READERS

Every year, Cahners Economics, the research and forecasting group at Cahners Publishing, compiles a list of trends and predictions for the coming year. The *Cahners 1991 Economic Outlook* reviews the economy in general, demographics, financial markets, and international markets. In addition, it has analyses of industries covered by Cahners publications, including electronics (semiconductors and components, computers and telecommunications, instruments and controls, military, and consumer). For EDN readers, the 57-pg book costs $11 (list price is $75). Cahners Economics, attn: Wendy Chambers, 275 Washington St, Newton, MA, (617) 630-2124, FAX (617) 630-2100.—Susan Rose

CMOS μP INCREASES SPEED

Zilog's Z280 16-bit μP now comes in a 12.5-MHz version that is 25% faster than the company's 10-MHz version. The μP has a 3-stage pipelined architecture, and an optional 8- or 16-bit data bus; it is code compatible with the company's 8-bit Z80 CPU. The μP's on-chip memory-management unit can address 16M bytes of memory and a 256-byte instruction and data cache. Other on-chip functions include three 16-bit counter/timers and a full-duplex UART. The $28 (1000) μP comes in a 68-pin plastic leaded chip carrier. Zilog, Campbell, CA, (408) 370-8000, FAX (408) 370-8056.—Dave Pryce

FUTUREBUS+ CHIPSET COMPLIES WITH IEEE STANDARDS

National Semiconductor Corp recently announced a Futurebus+ chip set that complies with the IEEE P896.1 and P896.2 specifications. The set consists of five ICs that use the company's backplane transceiver logic (BTL). The devices come in either plastic quad flatpacks or plastic leaded chip carriers. (Prices listed are for the flatpacks.)

The $7.70 (100) bipolar DS3883 is a 9-bit data transceiver that transmits and receives address, data, parity, command, and status signals. A 64-bit system requires 10 of these ICs. The IC has filters that eliminate glitches due to wire-ORed connections. The $28.75 (100) CMOS DS3875 arbitration controller supports the Futurebus+ distributed protocol and message passing in the central arbitration scheme. The

$13.90 (100) BiCMOS DS3885 is a 9-bit arbitration transceiver that communicates with the bus and the arbitration controller. The transceiver implements the arbitration-competition logic and performs parity checks. The $9.90 (100) BiCMOS DS3886 is a 9-bit latched-data transceiver, and the $13.90 (100) BiCMOS DS3884 is a handshake transceiver. National Semiconductor Corp, Santa Clara, CA, (408) 721-5000, FAX (408) 749-9071.—John Gallant

QUADRUPLE CMOS COMM DEVICE SAVES BOARD SPACE

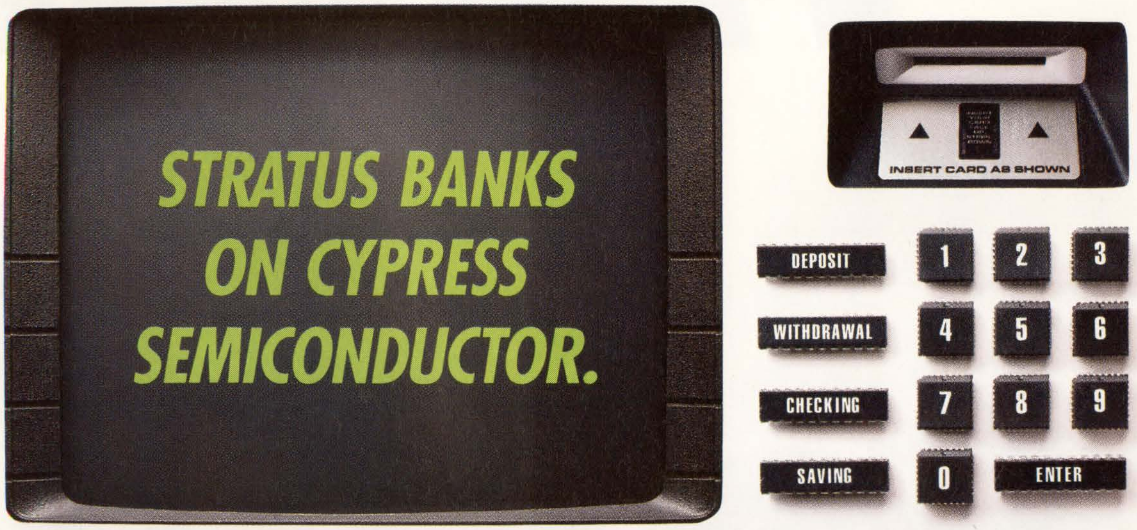
VLSI Technology Inc's VL16C554 combines the abilities of four ICs in a single chip. The chip has four VL16C550 UARTs, each with its own 16-byte data FIFO circuit, and suits applications that involve intensive data communication in PCs, terminal cluster controllers, or statistical multiplexers. The chip's four CMOS asynchronous communications elements act as serial data I/O interfaces that perform serial-to-parallel conversion on data characters received from peripheral devices, such as modems. The VL16C554 comes in an 84-lead plastic leaded chip carrier and costs $63 (1) or $32 (1000). VLSI Technology Inc, Tempe, AZ, (602) 752-8574, FAX (602) 752-6000.—J D Mosley

WINDOWS-BASED DSP DEVELOPMENT SOFTWARE SUPPORTS OOP

Signal Technology Inc's N!Power 1.0 is an object-oriented Windows-based development framework for digital-signal-processing applications. It lets you prototype your application rapidly because it treats individual data files and software modules as objects. You string together the data, algorithms, and hardware control functions drawn from both the framework library and third-party software using a Lisp-based symbolic language to define the procedures. The framework runs on a Sun SPARC or VAX workstation and costs $6000. The framework package supplies the X-Window interface, an object-oriented high-level application language, 2- and 3-D graphics capability, and a library of signal- and data-analysis functions. You can add modules to the framework, including a library of DSP algorithms, DSP-chip code generators, and control for selected A/D and D/A devices. You can also acquire a module that lets you add third-party software to the framework. Modules cost from $250 to $3750. Signal Technology Inc, Goleta, CA, (805) 968-3000, FAX (805) 968-2620. —Richard A Quinnell

MEMORY-CELL STRUCTURE LIMITS LEAKAGE IN DRAMs

Toshiba America Electronic Components is researching a memory cell that provides 0.6 μm of separation between the crucial regions of trench cells in dynamic RAMs (DRAMs), even with 0.4-μm design rules. The company is developing the cell because conventional methods of building trench cells for DRAMs won't scale to 64M-bit densities. Because of their proximity to each other, leakage between adjacent trench cells, and from active areas to the storage capacitors within cells, results when IC geometries shrink. The memory cell uses a thin insulating layer of oxide on the surface of each trench capacitor to prevent leakage. In addition, the memory cell uses an asymmetric and offset trench, rather than the parallel alignment of conventional trenches. Toshiba America Electronic Components, Irvine, CA, (714) 455-2000, FAX (714) 859-3963.—Michael C Markowitz



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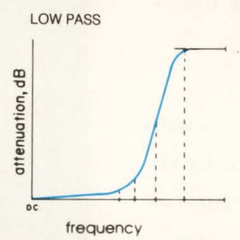
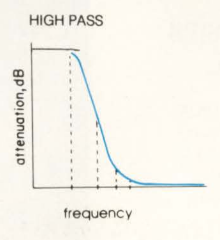


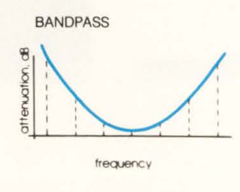
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	(loss>40dB) Max.	(loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



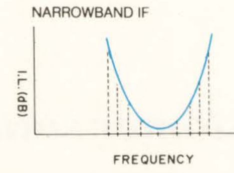
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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Mentor Graphics	HP/Apollo DN3XXX DN4XXX	DOMAIN/OS 10.1 IDEA Series 7.0	GA: 1.2μm SOG: 1.0μm, 0.8μm SC:1.5μm, 1.2μm
Synopsys	Sun-4	Sun OS 4.03 *Interface to Mentor, Valid, Viewlogic	SOG: 1.0μm, 0.8μm
Valid	Sun-4 Sun-3	Sun OS 4.0.1 GED, ValidSIM, RapidSIM	GA: 1.2μm SOG: 1.0μm, 0.8μm SC: 1.5μm, 1.2μm
	DEC Station 3100	ULTRIX ValidSIM GED	GA: 1.2μm SOG: 1.0μm, 0.8μm SC: 1.5μm, 1.2μm
Viewlogic	Sun-4	Sun OS 4.0.3 Workview 4.0	GA: 1.2μm SOG: 1.0μm, 0.8μm SC: 1.2μm
	PC386	DOS 3.3 Workview 4.0	GA: 1.2μm SOG: 1.0μm, 0.8μm SC: 1.2μm

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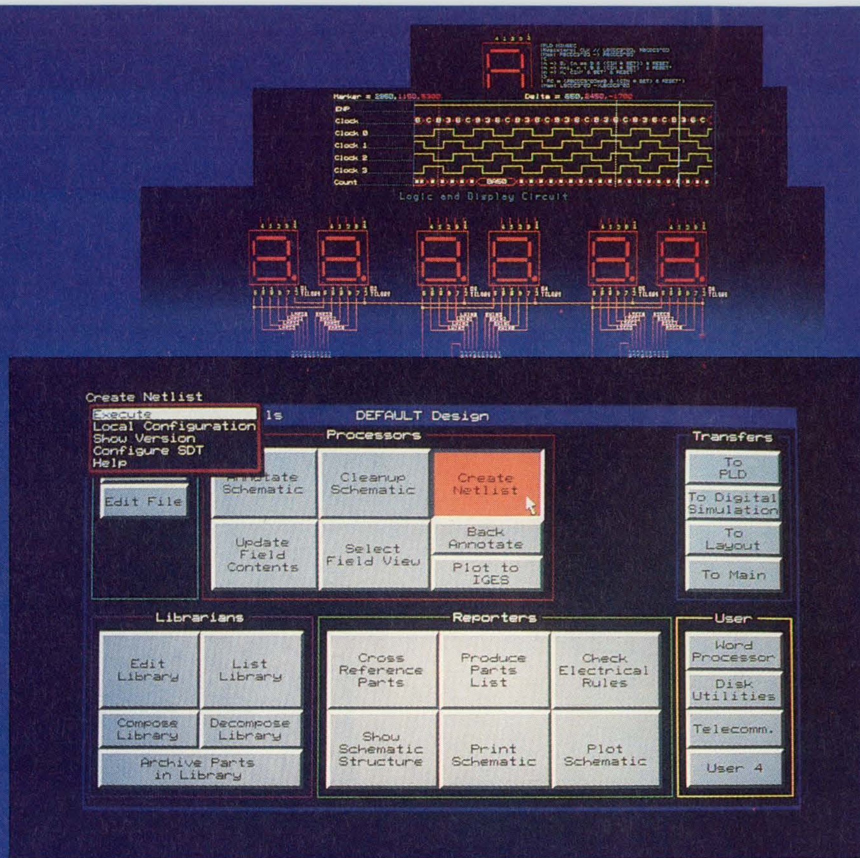

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SIGNALS & NOISE

Reader notes competent reporting on neural networks

Maury Wright's article, "Neural networks tackle real-world problems" (EDN, November 8, 1990, pg 79), is the sort of in-depth reporting that should stimulate more designers to investigate the benefits of neural networks. Many companies are using this technology to reduce costs and improve quality.

Maury referred to our C25 accelerator board as having a price range of $2500 to $4150. The company now offers only the high-end zero-wait-state board at $1995.

Mark Lawrence
President
California Scientific Software
Grass Valley, CA

Price of optical-disk drive

The price of the RMD-5100-S 3½-in. rewritable optical-disk drive from Most Inc did not appear in the New Product write-up (EDN, December 20, 1990, pg 118) because it was not available when this issue went to press. The RMD-5100-S drive costs $2450; the price of $120 is for the cartridges only.

Phone-number correction

Two digits in the phone number for Xitron Technologies Corp (EDN, December 20, 1990, pg 149) were inadvertently transposed. The correct number is (619) 458-9852.

Software correction file available on EDN BBS

The correction file for the software in Fred Salvatti's article, MS152 (EDN, August 20, 1990, pg 141) is available on EDN's Bulletin Board Service (BBS), /freeware SIG, (617) 558-4241 (2400,8,N,1).

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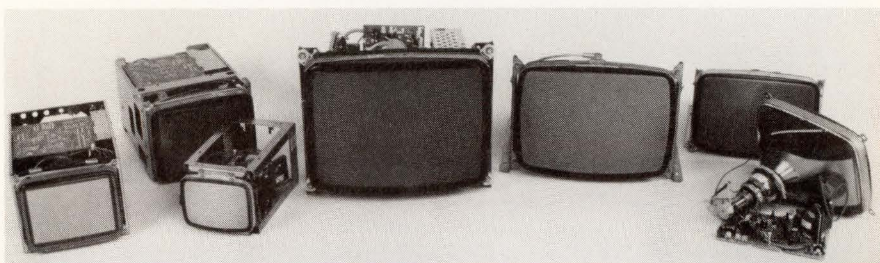

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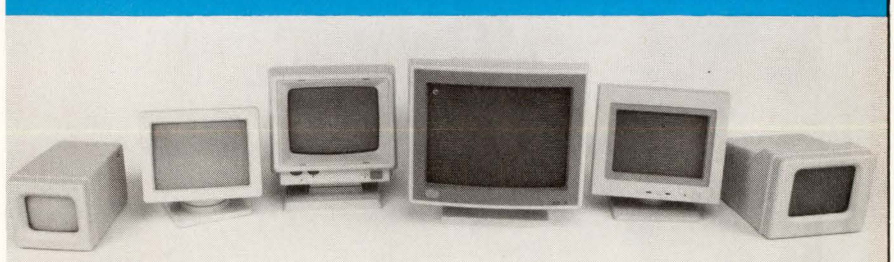

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Apart from our nameplate, a Seagate disc drive looks much like any other when viewed from the outside. But it's the tangible and intangible elements we put inside that make a Seagate drive really shine.

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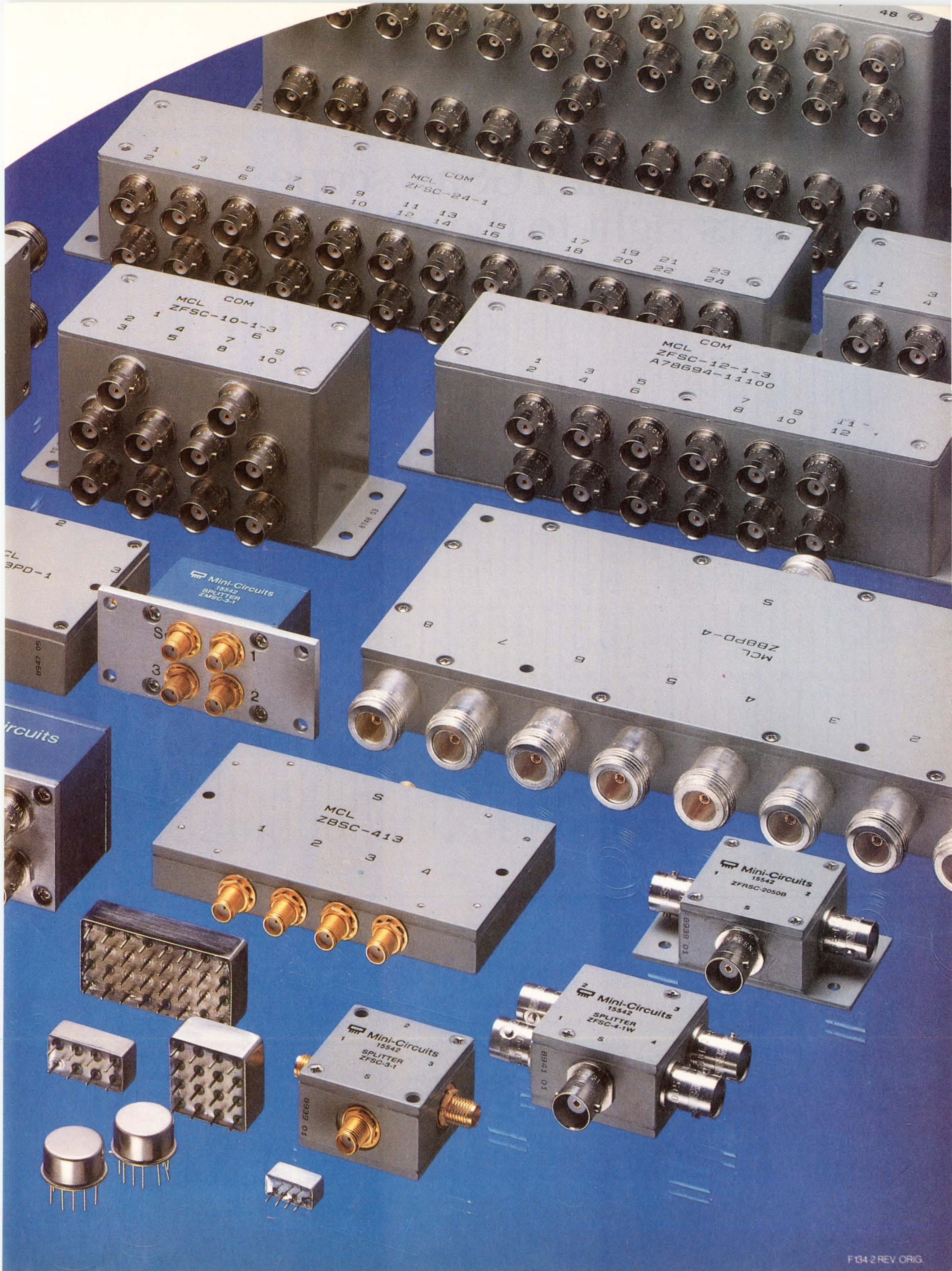

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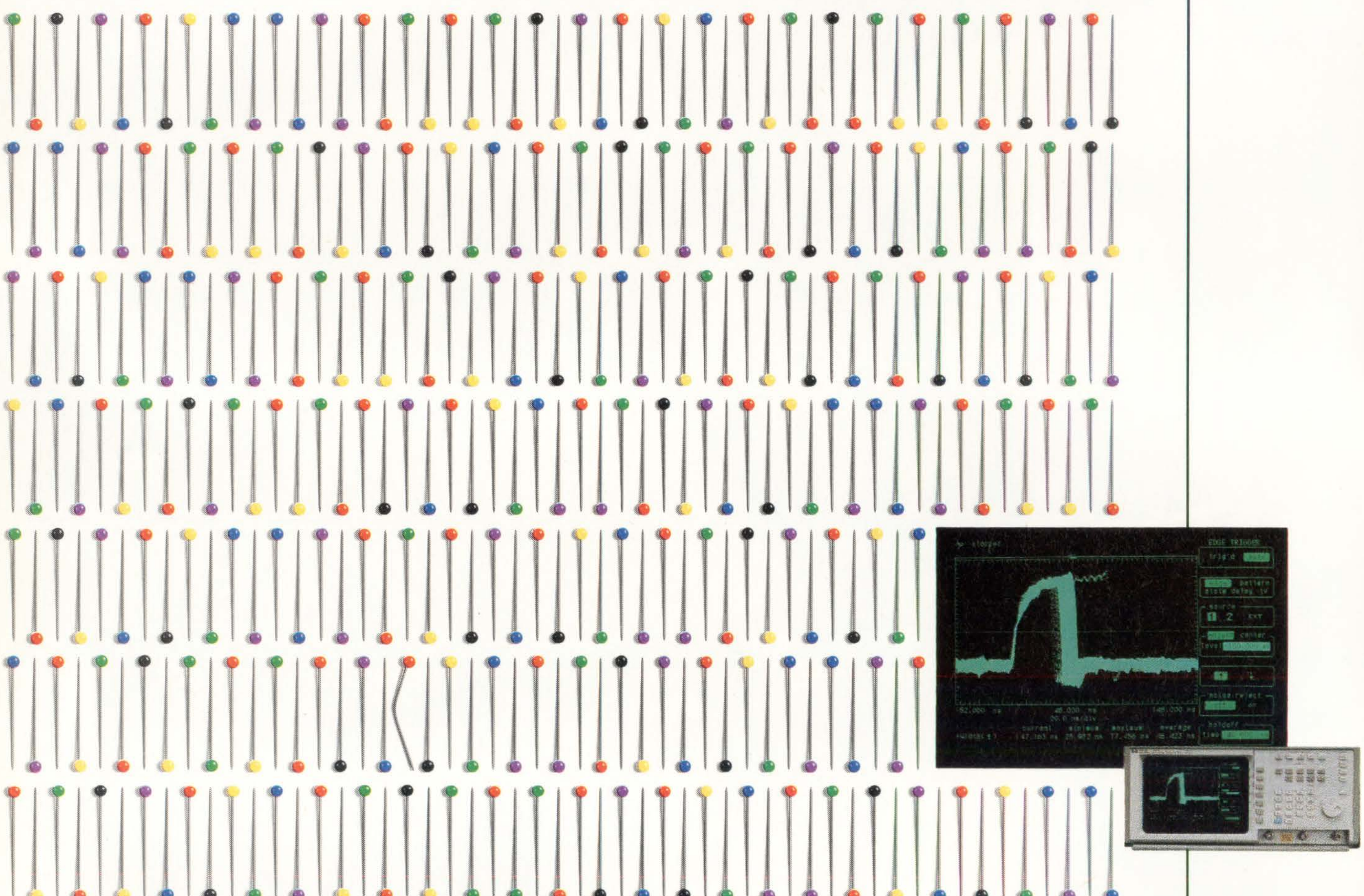

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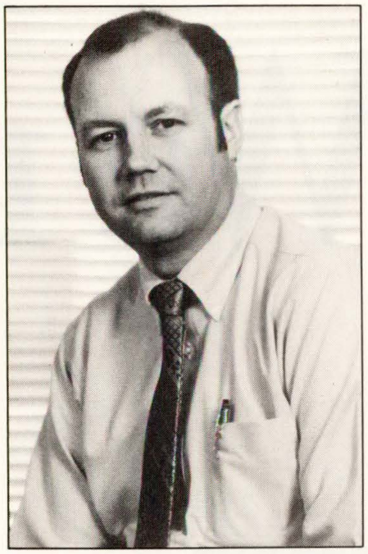
EDITORIAL

Where are the experimenters?



Electronics used to be a fun hobby. I remember my first experiments with electricity. My grandfather, an electrician, wired up a selection of switches, bulbs, buzzers, and bells on small wooden blocks so I could connect them and try out various circuits. Those first circuits led me to explore crystal radios, a 1-tube receiver, plug-board experimenter kits, and, later, kits from Heathkit, Lafayette Radio, and Allied Radio. I tried out a lot of ideas and circuits—even though I didn't always know what I was doing. I recall a particularly neat breadboard that supplied components on yellow plastic mounts that fit into a large sheet of perforated wooden board. Special jumper clips connected the components. The explanations in the accompanying manual told me how the circuit worked and what each component did.

New York City held a special lure for teenagers like me growing up on Long Island. Many of us wanted to "go to the city" to sample night life, see a play, or visit a museum or library. Instead, at 15, my first solo trip to New York took me to Canal Street, an experimenter's paradise where electronic-surplus stores lined a quarter-mile stretch of this downtown street. The stores offered relays, switches, surplus computer boards, military radios, and even old teletypewriters. When you needed a part, you found it on Canal Street.

Much of Canal Street is now history, and I'm afraid that much of the hobby of electronics is, too. I'm always surprised at this time of year by the lack of "101-electronic experiment" kits, chemistry sets, and microscopes in the toy stores. It seemed not long ago that kids enjoyed technical toys. These days, many toys and games use electronic components, but the kids don't know it and don't appreciate what electronics does for them. (Maybe they just haven't had the chance—safety concerns with some of these sets seem to have cleared the shelves of nearly all experimenting toys.)

Most of the hard-core electronics hobbyists and experimenters I knew in high school went on to become talented engineers or scientists. I'm convinced that their early hands-on experience with electronics further advanced their learning and their careers. Perhaps they succeeded because they had developed a feel for things electronic, a love for the technology, and a deep enthusiasm for new possibilities.

The engineering profession is poorer for not giving youngsters the opportunities to experience electronics firsthand, particularly when they're open-minded and awed by technical things. Yet, it's difficult to give them that opportunity. For example, few of the young people I know are interested in amateur radio. With cellular phones, fax machines, and computers and modems, who's thrilled by 2-way Morse-code communication with a person in New Zealand? Likewise, small, inexpensive radios and stereos are easy to buy on most kids' allowances. That makes it completely unattractive to build a short-wave receiver. Why bother?

On the other hand, we don't have legal or medical hobbyists, yet our colleges and universities turn out many fine lawyers and physicians who get almost all of their experience in formal surroundings. Maybe the lack of electronics as a hobby or avocation doesn't harm the engineering profession after all. It's possible, though, that we might have *even better* doctors, lawyers, and engineers if they got some realistic exposure to medicine, legal matters, and electronics before they chose a profession.

Jon Titus

Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

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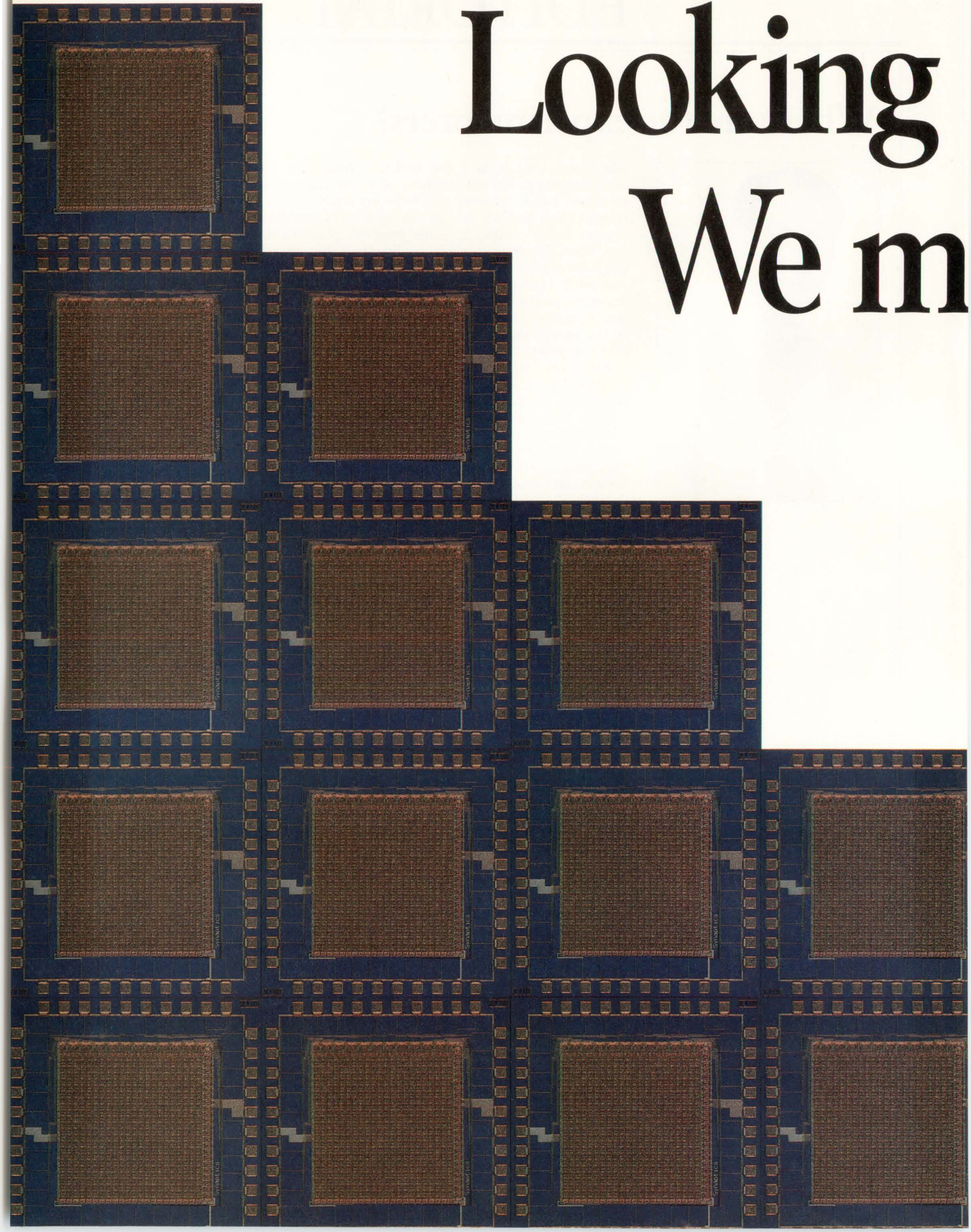

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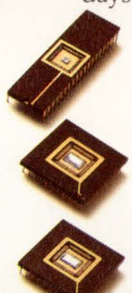

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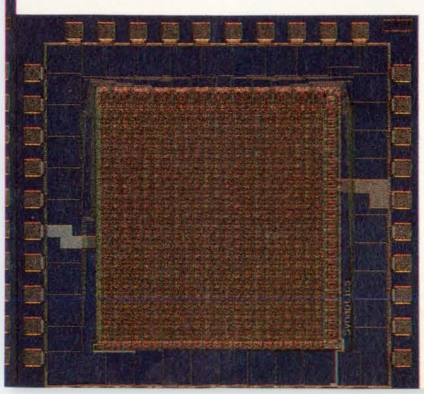

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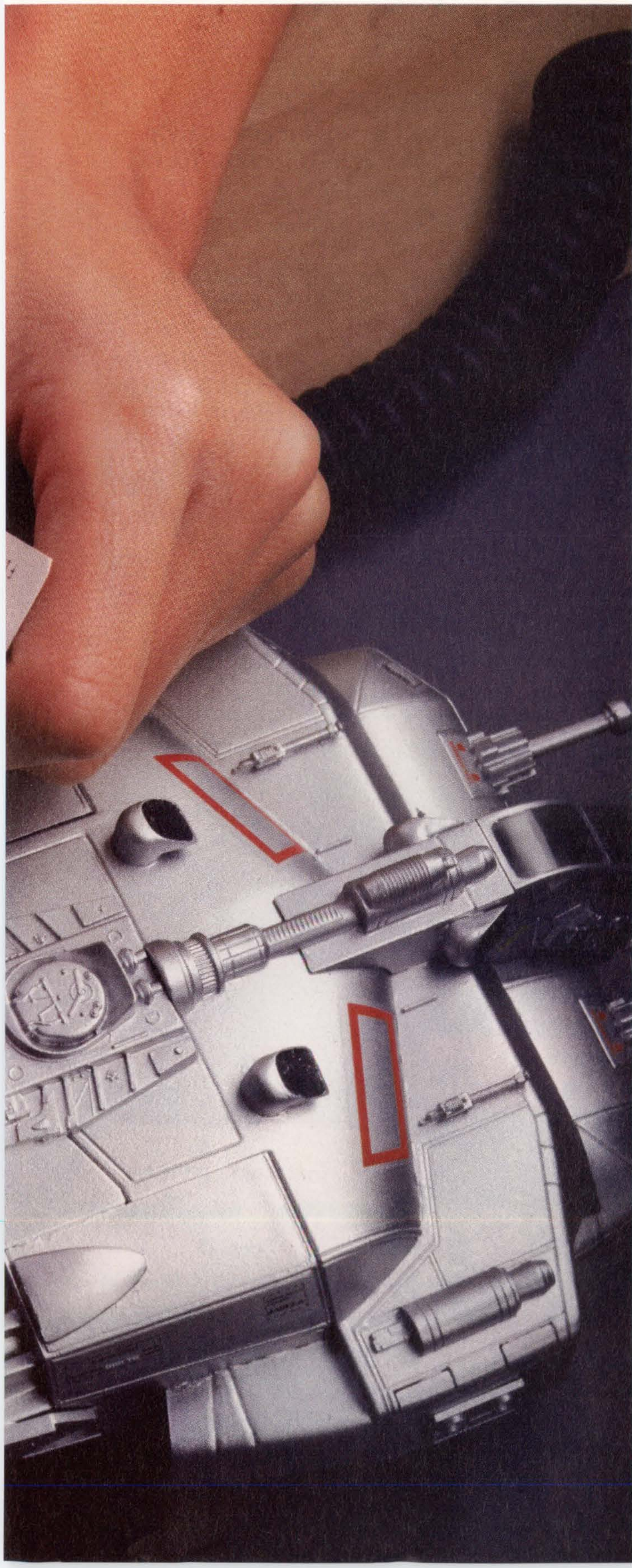

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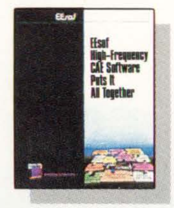

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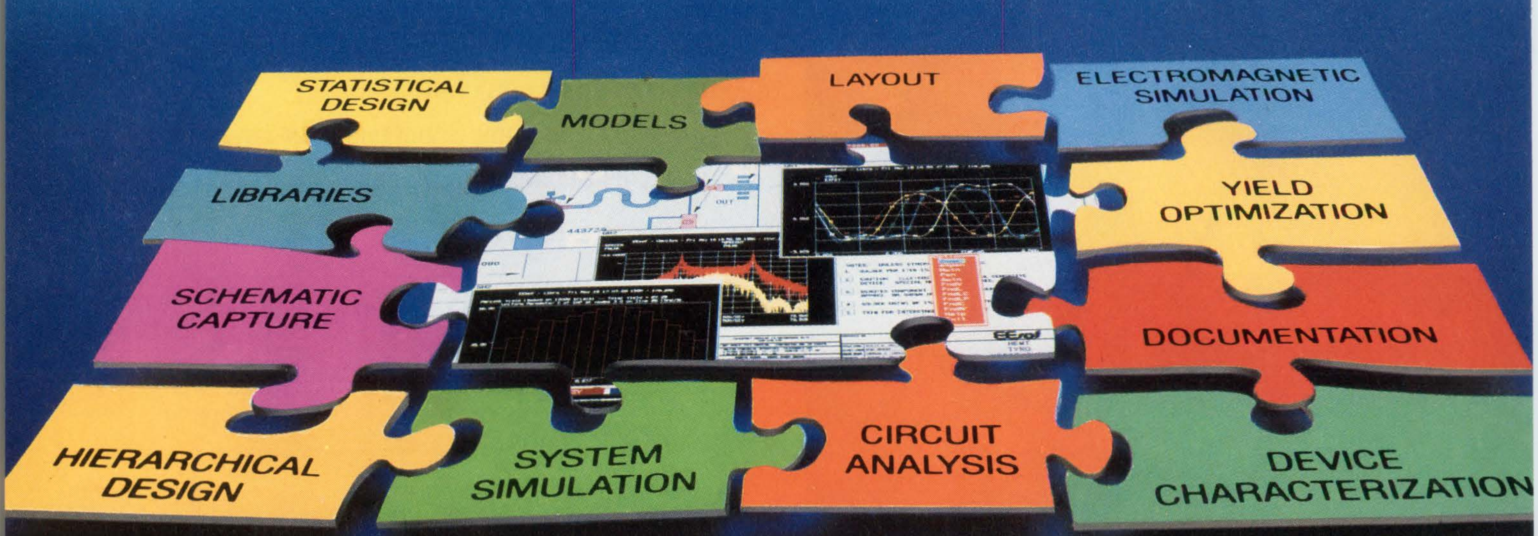

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CIRCLE NO. 71

SEMICUSTOM ANALOG ASICs

Design methods resist generalization

Designing an analog ASIC requires a tremendous amount of communication between system and IC designers.

Anne Watson Swager,
Regional Editor

Choosing the appropriate design method for your analog ASIC can reduce much of the design risk currently associated with these ICs (see **box,** "Recognize risks to reap rewards"). Making this choice is not trivial because many variations of each basic method exist. Regardless of whether you, the vendor, or an independent designer or fabless design house do the majority of the designing, a close working relationship among all concerned parties is the only way to ensure design success.

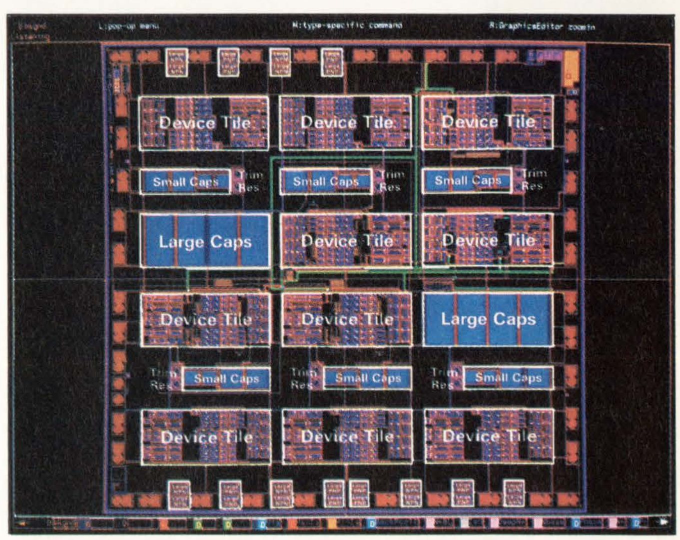
Analog-ASIC design methods fall into two general categories: full custom and semicustom. Full-custom ASICs are completely handcrafted from bare silicon, generally by an experienced IC designer.

Semicustom analog ASICs split into array-based and standard-cell designs. Traditional component arrays consist of a slate of transistors, resistors, and capacitors on a piece of prefabricated silicon. Tile arrays comprise fixed circuit blocks. Each block contains a fixed number and type of active and passive components. For both types of arrays, the designer's job is to connect the elements by defining one or sometimes two final metallization layers.

Standard-cell designs start out as a blank slate. By defining the functions you want from the vendor's library—or by specifying some new cells of your own—you create the entire mask set for the chip. The vendor has already designed and characterized the cells' corresponding mask sets. Most vendors of cells and arrays have some capacity to place digital gates on their ICs. These vendors still consider themselves analog vendors, despite the mixing of analog and digital circuitry.

Full-custom ICs clearly make the best use of their die area, but they incur the longest design times and highest NRE costs. Standard cells place second on the silicon-efficiency scale. You choose only the exact circuit elements you need. However, standard-cell designs are only half a step from full custom. Rarely does a vendor's library contain all the cells you need; the vendor must often create new "custom" cells.

Arrays trade a standard-cell design's



Tile arrays use silicon less efficiently *than standard-cell designs do, but they generally have faster turnaround times. Many tile arrays, such as the HTA2000 from Harris Semiconductor, also have cell functions.*

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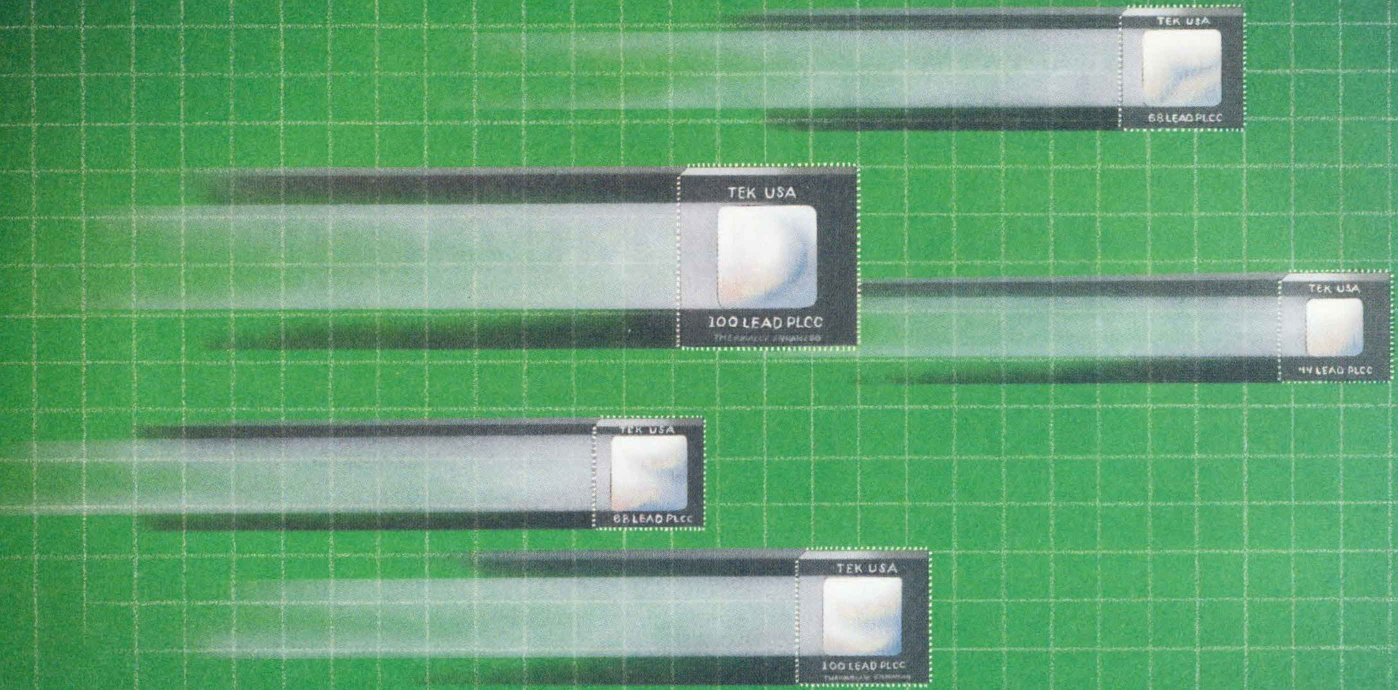

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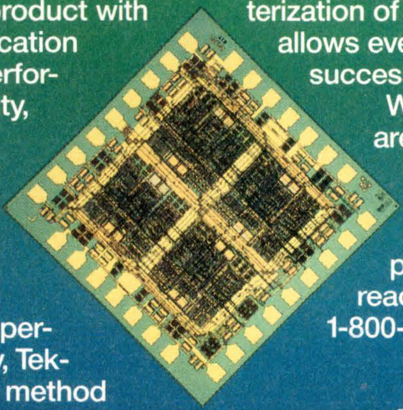

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Copyright © 1990, Tektronix, Inc. All rights reserved. ICO-100 efficient use of silicon for lower NRE costs and faster turnaround times. Tile arrays constrain a design if that design calls for an element or number of elements not on the array. Also, tile arrays may waste silicon by leaving some passive or active components unused.

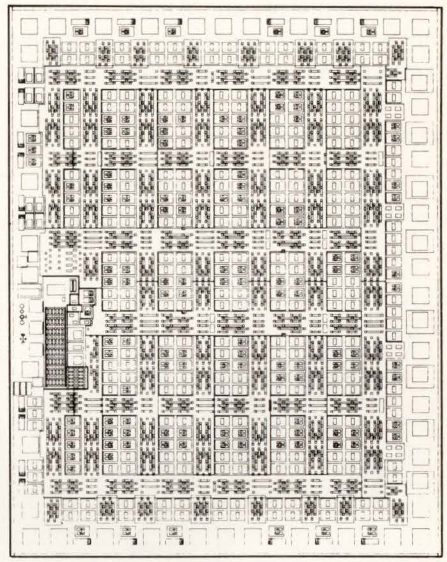
Volume will also influence your design-method choice. For example, if you're planning to build a small number of ICs, a tile array will get you started with less NRE costs. Also, many vendor's fabrication processes and design methods may only be viable for high-volume customers (many vendors define high volume as 100,000 to 250,000 units per year). Unless a vendor has a substantial business interest in your particular application area, you may not be able to find a company to build your chip in small volumes.

Now, the exceptions

Unfortunately, these generalizations about design methodologies make choosing a design approach sound cut and dried. It's not. For one thing, analog-ASIC design capabilities are changing fast. **Table 1** can serve as a guide, but tables tend to oversimplify the design choices. The equivalent of the digital gate array does not exist in the analog world: There's no consensus or well-accepted standard approach to designing analog ASICs.

For example, making assumptions about the process technology you need may be risky. Analog ASICs can be CMOS, bipolar, or BiCMOS. You might assume that you have to use a bipolar process to build a function with a particular performance level, but even the vendors themselves are surprised at what they can accomplish with CMOS processes. Don Bartlett, an analog-design project leader at NCR Microelectronics, says his company now has a 10-bit ADC as a standard cell—a goal engineers didn't think they could achieve a year ago.

Both standard cells and arrays are changing in ways that either minimize or remove their previous limitations. Tools continue to become available to system designers. Large and well-established semiconductor companies such as Texas Instruments, Motorola, National



Bandgap references are a permanent fixture *of some tile arrays. The Genesis 5200 semicustom IC from Cherry Semiconductor has a reference on the lower left-hand side of the array.*

Recognize risks to reap rewards

Analog ASICs are laden with many design risks and tool shortcomings that digital ASICs have long since overcome. Common design problems include isolating noise, isolating the substrate, interfacing the chip with external electronics, and keeping NRE costs low and all schedules short. Designers measure the "first-time silicon success" of analog ASICs functionally. Many analog ICs work on the first pass, but they often require some form of tweaking to perform exactly as you want.

Inadequate tools and the lack of test methods are the two big stumbling blocks for analog and mixed-mode ASICs. Spice and its derivatives serve many pure analog designs well, but capable mixed-mode simulation tools are just beginning to become available. Worst-case modeling is difficult, and vendors don't guarantee a part will work based on simulation results alone.

No systematic or widely accepted test method for analog ASICs exists. Vendors don't have much to say about test except that they're working on it. They do say that testing a highly embedded function requires early planning on how the testing equipment will access the chip.

The good news is that you don't necessarily need expensive tools to design analog ASICs. Many vendors have made IBM PCs and compatibles their hardware of choice. Other design methods don't even require that you simulate the ASIC because you're combining proven building blocks. Micro Linear's semistandard ICs let you specify a combination of proven circuits. Advanced Linear Devices provides building blocks identical to those of the final IC. You can connect these blocks and troubleshoot them on a pc board.

Semiconductor, and Analog Devices have much experience designing analog and mixed-signal ASICs. These companies will design semicustom ICs for you, as will other companies listed in **Table 1,** using their proprietary tools and standard cells. They generally work with very-high-volume customers and only make their tools available to special customers. However, these companies envision a time when tools will be available to all their customers. Within the next couple of years, TI will make parts of its

Table 1—Representative semicustom analog ASIC design methods

Manufacturer	Product	Design method	Vendor/customer relationship	Process	Typical NRE costs
Advanced Linear Devices	Function specific linear ICs	Cell based with standard products	Customer designs	CMOS	\$20,000 to \$50,000
Analog Devices	Mixed-signal ASICs	Cell based	Turnkey supplier only	BiCMOS	\$50,000 to \$100,000
AT&T Microelectronics	CBIC process	Array based	Customer/vendor designs	Bipolar	\$30,000 to \$50,000
Cherry Semiconductor	Genesis	Array based	Customer designs	Bipolar	\$10,000
Custom Arrays Corp	MM/MV	Array based	Customer designs	Bipolar	\$5000 to \$15,000
Exar	Flexar	Array based	Customer designs	Bipolar	\$2500 to \$9500
Gould AMI	Mixed-signal design solution	Cell based	Customer designs	CMOS	\$50,000 to \$70,000
Harris Semiconductor	Mixed-signal, analog and power ASICs	Cell based	Customer deisgns	Bipolar, CMOS, BiCMOS	From \$40,000
ICS	Mixed-signal ASICs	Cell based	Turnkey supplier only	CMOS	\$30,000 to \$70,000
International Microelectronic Products	Mixed-signal ASICs	Cell based	Turnkey or joint designs	CMOS, NMOS	\$90,000
Micro Linear Corp	Semistandard ICs	Array and cell based	Turnkey supplier only	Bipolar, CMOS	\$5000 to \$50,000
Motorola	Mixed-signal ASICs	Cell based	Turnkey or joint designs	CMOS bipolar	\$30,000 to \$55,000
National Semiconductor	Clasic	Cell based	Turnkey or joint designs	Bipolar, CMOS, BiCMOS	\$45,000 to \$65,000
NCR Microelectronics	Mixed-signal ASICs	Cell based	Turnkey or joint designs	CMOS	\$40,000 to \$50,000
Plessey Semiconductor Corp	ULA mixed-signal ICs	Array based	Turnkey or joint designs	Bipolar	\$5000 to \$6500 (customer designs) from \$18,500 (turnkey designs)
Raytheon Semiconductor	RLA, RFA	Array based	Customer designs	Bipolar	From \$21,000
SGS-Thomson Microelectronics	ANACA mixed-signal and linear ASICs	Array and cell based	From turnkey to customer designs	Bipolar, CMOS, BiCMOS	\$30,000 to \$75,000 (standard cell) \$25,000 to \$40,000 (arrays)
Sierra Semiconductor	Mixed-signal ASICs	Cell based	Turnkey or joint designs	CMOS	\$20,000 to \$120,000
Tektronix	QuickTile	Array based	Customer designs	Bipolar	\$85,000 to \$91,000
Texas Instruments	LinASIC	Cell based	Primarily turnkey	Bipolar, CMOS, BiCMOS	\$50,000 to \$150,000

Note: The mixed analog/digital methods included in this table have the ability to integrate large amounts of analog circuitry. Vendors that offer primarily digital ASICs with only a small analog portion are not included here.

tools compatible with Mentor Graphics' Falcon framework. Gould AMI is announcing the final version of its Mixed-Signal Design Solution system this quarter. The system will include model-building software that lets you create cells in house.

Categorizing array-based methods is difficult. Array-based methods range from AT&T's high-speed, high-performance CBIC process to Advanced Linear Devices' standard IC building-block approach. Many arrays now have features that minimize their previous limitations, too.

Typical turnaround times (weeks)	Comments
12 to 16	User designs and breadboards the ASIC with completely specified, standard ICs provided by the vendor. Specializes in low-power designs.
24 to 52 from signed specification	NRE charge includes all design and fabrication to deliver final packaged and tested silicon. Specializes in high-performance (12-bit accuracy) circuits.
6 to 8	High-speed and high-performance process. Some arrays are laser trimmable. Building block kits are available. Vertical pnp and npn transistors.
8 to 12	Company maintains BBS for users to transfer design information (1-800-272-2447).
4 to 8 from layout	Macrocell library contains amplifiers, comparators, timers, regulators, buffers, flip-flops, S/H amplifiers, and Schmitt triggers. Kit parts available. Company sells design software for 386-based IBM PC.
3 to 6	Designer can move tiles to different locations and can create either an npn or a pnp transistor in a given location. Macro library of proven circuits.
From 20	Model-building software lets designers create models in house.
6 from final design	Tile arrays and standard cells part of FastTrack design system. Runs on Unix workstations.
16 to 20 from first specification	Design services include "free-look" prototyping. Vendor can make changes at this stage without scrapping masks and prototype wafers. Specializes in low-power designs, not locked into 5V process.
22 to 24	Also offers manufacturing services for customer designs.
6 to 14 (bipolar) 12 to 24 (BiCMOS) after design verification	You create a semistandard IC by modifying an existing standard product.
6 from simulation	Company provides engineering design assistance for $3000/week. NRE and lead times are quoted for company's MOS products.
12 to 16 (conception to first prototype)	1-week training course is free to customers and $1000 for others. Dense bipolar process yields high integration.
10.5 from design review	Accurate cell models have timing information from silicon built in. Turnaround time includes customer-performed post-simulation layout. High-performance CMOS.
4 to 12	Library of analog and digital macro functions. Special cells located at chip corners. 5-mask process keeps costs down.
6 to 8 from design verification	Macrocell op amps and comparators. Dual-layer metal. Thin-film resistors. Kit parts available.
6 to 9 (standard cell) 3 to 4 (arrays)	Tiles have kit parts. Macrocell library includes op amps, comparators, timer/oscillator, video amplifier, bandgap reference, transconductance amp Schmitt trigger, NOR, NAND, flip-flop, and DAC.
9	Company has large library of cells. Process technology combines analog and digital circuitry and EEPROM.
10	Startup package with software and training course costs $15,000. Software runs on Sun workstation. High-speed designs, accurate models.
16 to 52	Specializes in high-performance, high-integration designs.

First of all, designing with tile arrays doesn't require designing exclusively with discrete transistors, capacitors, and resistors. Instead of transistors, for example, Raytheon Semiconductor uses gain blocks as the basic element in its arrays. Most tile-array vendors feature macrocells and defined tiles. In most cases, these tiles are located at specific locations on the tile array.

For example, Cherry Semiconductor's Genesis 5200 high-frequency array features a programmable bandgap voltage reference on the lower-left edge of the array. You can program the reference's voltage between 1.25 and $V_{CC}-2V$. By using a fuse-link trim option, you can achieve a voltage deviation of $\pm 3.5\%$. You can internally structure the tile in four configurations.

SGS-Thomson's TSFJ series of mixed bipolar arrays also have built-in bandgap references in addition to tiles for oscillators, voltage regulators, and R-2R ladders for a 6-bit DAC. Raytheon's RLA ICs consist of op-amp cells, comparator cells, and thin-film resistors. Plessey's ULA DA family of analog/digital arrays include a bandgap reference, voltage regulators, low-offset transistors, matched precision resistors, capacitors, and 120-mA transistors.

Tile arrays suit many applications, including military ones. Late last year, Harris Semiconductor announced the dielectrically isolated HTA2000 analog tile array. The two versions of the array meet class S and class B reliability requirements. The dielectric isolation lets the arrays use both vertical npn and pnp transistors. The arrays' library of cells includes op amps, comparators, S/H amplifiers, buffers, references, and differential video circuits.

Tile arrays get more flexible

Possibly the biggest design deterrent to using tile arrays is their inflexibility, but vendors are coming up with ways to make tile arrays more flexible. Tektronix's QuickTiles, relatives of the company's QuickChip family of ICs, combine full-custom fabrication with a tile-like design method. Designers define the circuit by snapping together standard tiles at any desired location on a coarse grid. Because the location of the devices in the arrays varies, all mask levels must be generated and the wafers must be fabricated from bare stock. The grid eliminates the risk of violating layout rules.

Both Exar and Custom Arrays Corp (formerly Interdesign) have tile arrays from which you can create either pnp or npn transistors. Exar's Flexar array lets you select either an npn or a pnp transistor from the same location using a single layer of metal. Custom Arrays' MV array has what the company calls a pnpn structure. The pnpn elements can serve either as lateral pnp or normal npn transistors. The arrays have a modular structure of cells that repeats throughout the chip. Thus, you can place macro functions anywhere on the array. Flexar's arrays come with a soft-macro library of proven circuits as well as kit parts and Spice device models. EDN

References

1. Quinnell, Richard A, "Mixed analog-digital ASICs," *EDN*, June 22, 1989, pg 147.

2. Pryce, Dave, "Semicustom circuits: Analog-digital ICs provide versatility," *EDN*, March 1, 1990, pg 91.

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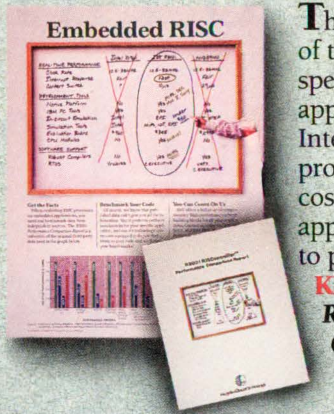

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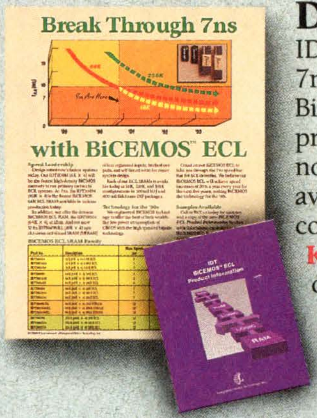

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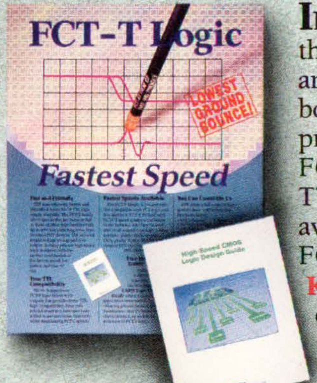

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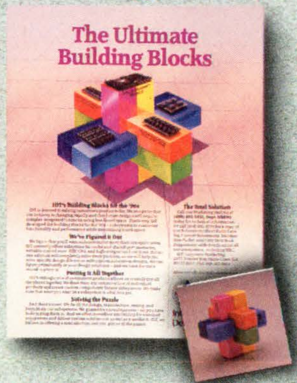

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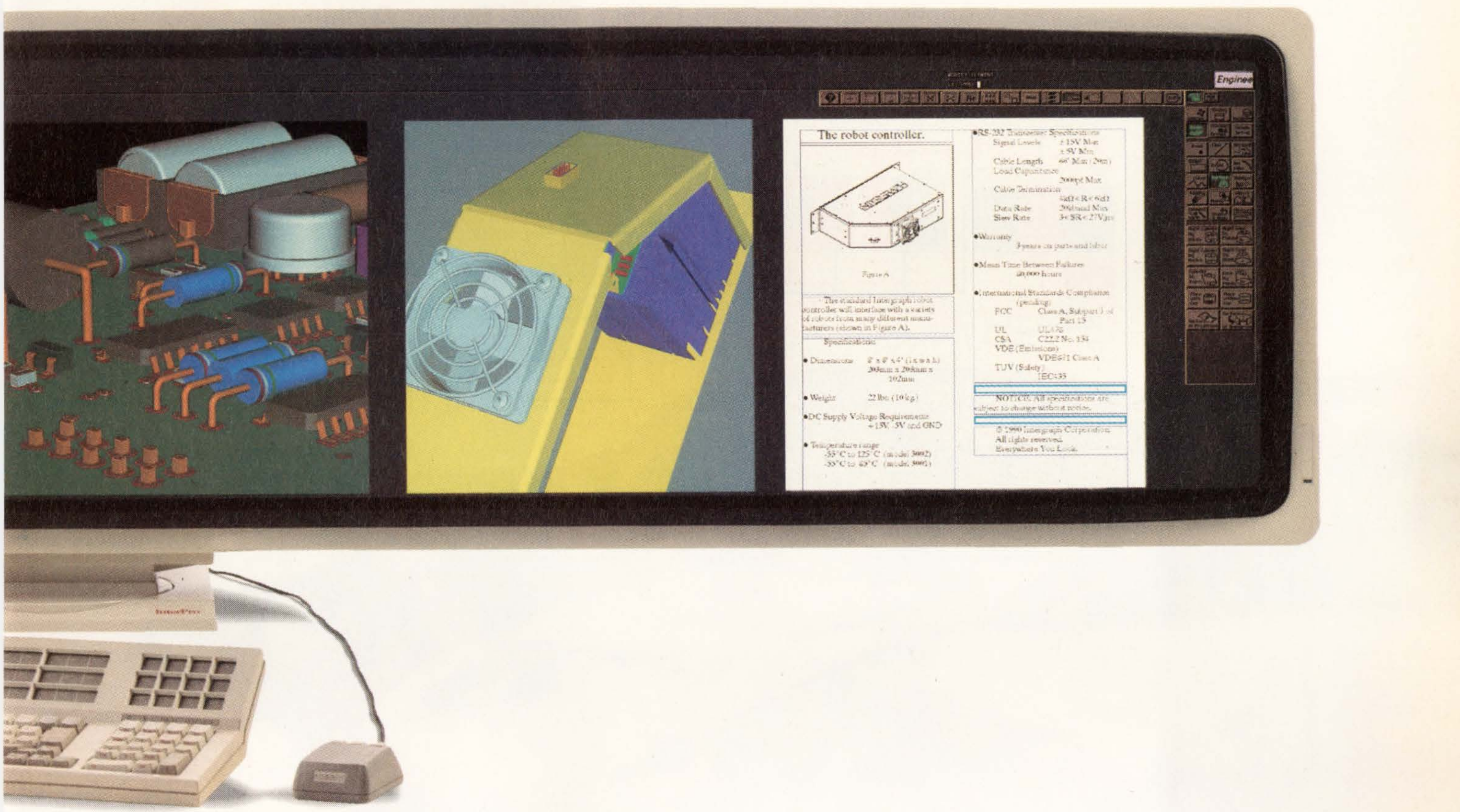

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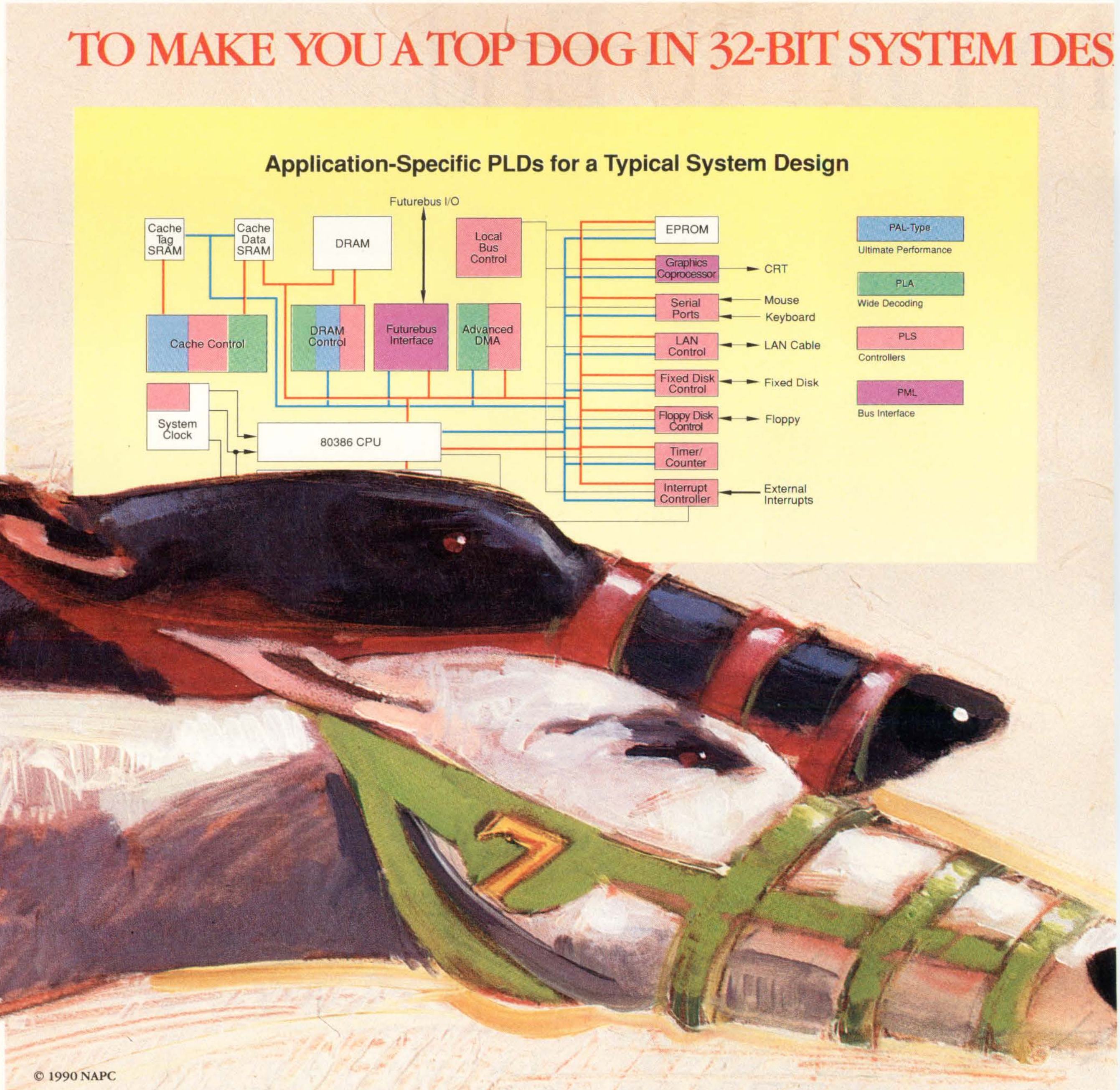

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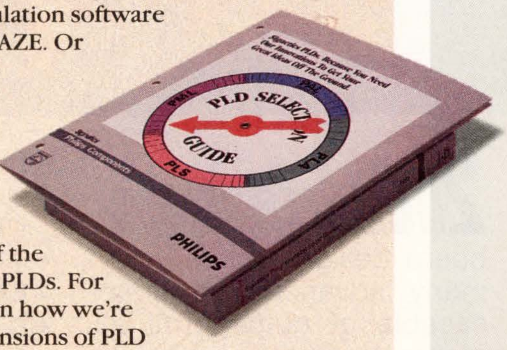

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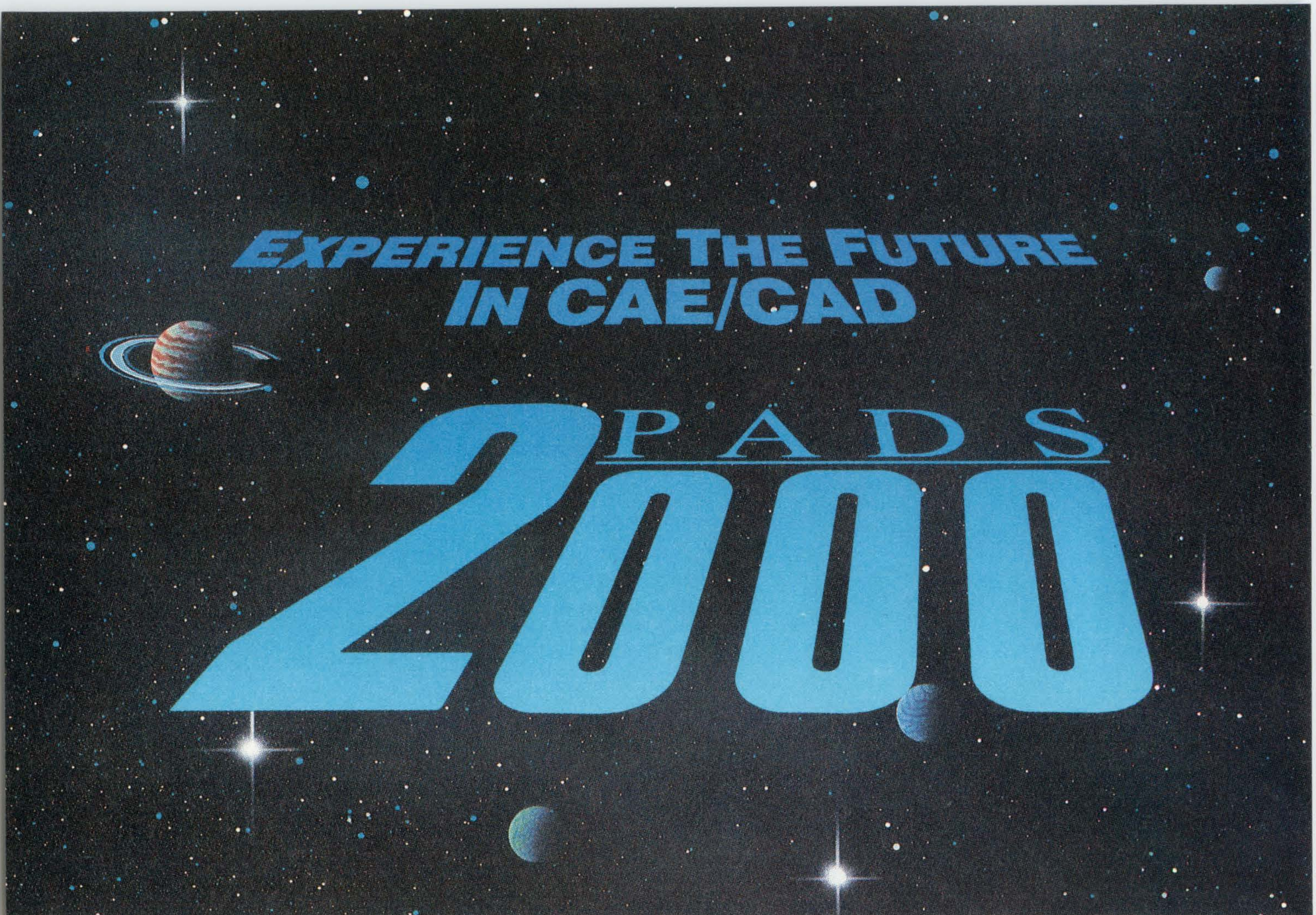

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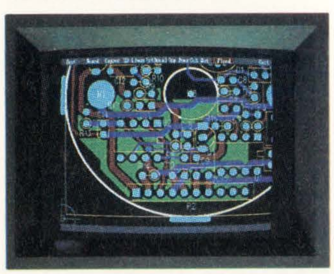

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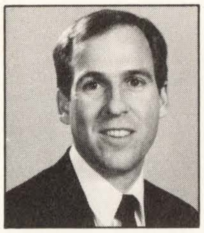
CIRCLE NO. 46

PC-BASED LOGIC SIMULATORS

Device capabilities are growing



Improvements in hardware and software are making PC-based logic simulation an alternative to workstations and mainframes for small-and medium-sized designs.

Doug Conner, Regional Editor

If you're already using a personal computer for CAD/CAE applications, you will find that you can use it for logic simulation as well. Before examining the details of PC-based simulation, it's worth looking at what simulation can offer you. Logic simulation software typically provides three types of simulation: functional, timing, and fault.

Functional simulation, normally the first step in verifying a design, checks the circuit's logic to see that it works the way you expect it to. Functional simulation typically uses unit timing delays instead of accurate timing models for component behavior. At the functional simulation level, you can find problems, such as inverted signals and improper sequential or combinatorial logic.

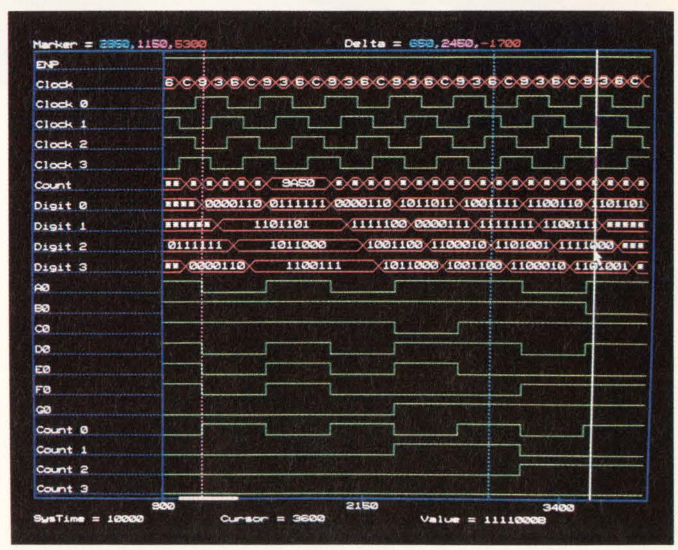
Once you've determined that the circuit executes the proper functions, you can concentrate on the timing simulation. Timing simulation makes more detailed demands of the simulator and the models used in the simulation. Therefore, accurate results require accurate models of the hardware.

Timing simulations often use gate-level representations. To simulate a circuit's operation more accurately, however, some designers use a switch-level representation, especially in IC design. Switch-level models represent the circuit at the transistor level, giving a more accurate simulation of the electrical characteristics. However, not every simulator supports switch-level modeling (see **Table 1**).

Fault simulation is useful for test operations where you want to find stuck-at-one and stuck-at-zero faults. A fault simulation uses a set of test or stimulus inputs to check out a design, finding the percentage of cases where stuck-at-one and stuck-at-zero faults are detected. Fault simulations are often useful when developing IC test programs.

Before you can reap the benefits of logic simulation, you have to go through three steps: entering the design, obtaining models for the components, and generating a set of stimulus or test vectors.

The usual method for entering a design into a logic simulator is via a netlist that describes how the components in the circuit are connected. Simulators



***The logic-analyzer-type output display** on OrCAD's VST simulator accommodates individual or bused signals. For bused signals, the display shows values in binary, octal, decimal, or hex. Cursors simplify timing measurements.*

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CXK581001P	128K x 8	70/85	DIP 600 mil	L
CXK581001M	128K x 8	70/85	SOP 525 mil	L
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PC-based logic simulators

typically accept netlists from various schematic-capture software packages.

The simulator also needs component models to simulate what each component does, both functionally from a logic standpoint, and for timing characteristics if you are performing a timing simulation.

You need either to purchase model libraries that cover the devices you are simulating or develop your own models. Simulation vendors usually provide model libraries or offer them as an option. If they don't, you can often buy the libraries from third-party vendors.

Don't assume all the models that you need are available. When shopping for a logic simulator, check out the available model libraries carefully, unless you are planning to develop your own models. Although the functional characteristics of models are usually straightforward, timing characteristics can vary considerably in their accuracy.

The model may measure only average timing characteristics, or be able to measure minimum, maximum, and average timings. In addition, the model may or may not have accurate data concerning correct setup, hold, reset, and clock intervals.

Even if you plan to use models from existing libraries, you should be aware of the methods available for generating models yourself. Undoubtedly you'll run into cases where you cannot find a model, or perhaps you need to modify a model to look at special behavior.

Developing your own models

To build logic models, you typically use the logic-primitive models provided with the simulator. These primitives include basic logic functions, such as AND gates, OR gates, and storage functions. High-level primitives, such as D and JK flip-flops, latches, RAM, and ROM may also be available. In addition to the logic functions, you need to know what timing constraints are included with the logic primitives.

For example, OrCAD's primitives have minimum and maximum gate delays. The storage primitives have setup and hold times and minimum clock-width parameters.

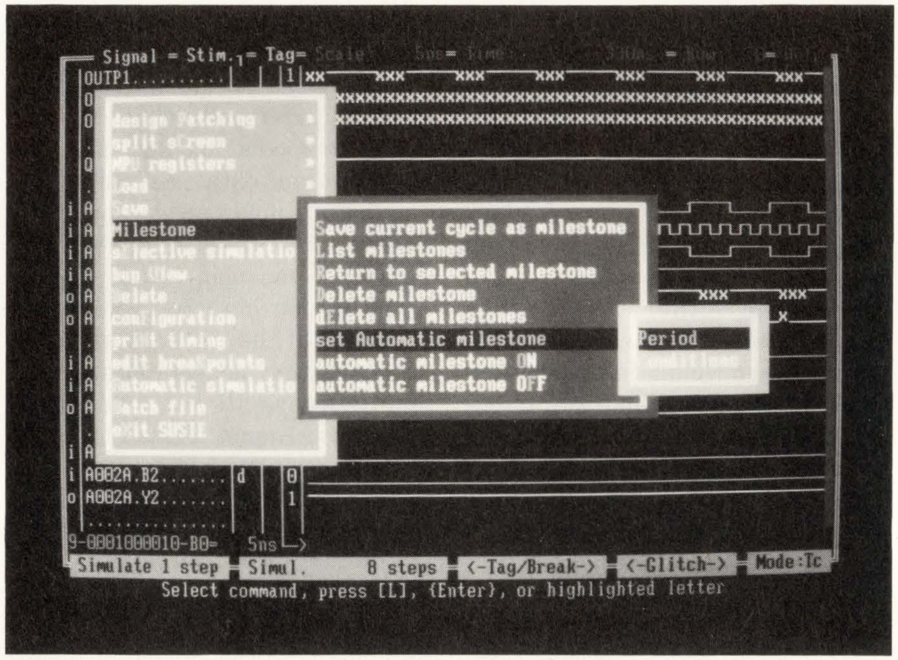
Building models up from primitives isn't the only way to develop your simulation. Behavioral or hardware description languages (HDLs) are another option on some simulators. For example, Viewlogic has an optional VHDL (VHSIC hardware description language) for modeling and simulation. Aldec's Mobic/T is a high-level IC modeling language for the company's Susie (standard universal simulation for improved engineering) series of logic simulators.

SimuCAD supplies the Silos behavioral modeling language for the company's Silos II logic simulator. You can use the modeling language to develop behavioral models that

Table 1—PC-based logic-simulation software

Manufacturer	Product	Libraries available[1]	Simulation levels	Computers supported	Price	Comments
Aldec	Susie 4	TTL[2], CMOS, ECL, memory, μP, PLD, FPGA	Gate, behavioral	IBM PC/XT, PC/AT compatibles	$995	Timing option $1495
	Susie 5	TTL[2], CMOS, ECL, memory, μP, PLD, FPGA	Gate, behavioral	IBM PC/XT, PC/AT compatibles	$1495	Timing option $2495 Virtual memory supported
	Susie 6	TTL[2], CMOS, ECL, memory, μP, PLD, FPGA	Gate, behavioral	IBM, 386/486, compatibles	$1995	Timing option $3995 Virtual memory supported
OrCAD	VST	TTL[2], CMOS[2], ECL[2], memory[2]	Gate	IBM PC/XT, PC/AT compatibles, P/S2	$995	
SimuCAD	Silos II/386	7400 series[3]	Switch, gate, behavioral	IBM, 386, compatibles	$2500	Fault simulation Virtual memory supported
	MacSilos II	7400 series[3]	Switch, gate, behavioral	Apple Macintosh II	$2500	Fault simulation
	P/C Silos	7400 series[3]	Switch, gate	IBM PC/XT, PC/AT compatibles	$1000	Limited version $400
Tanner	Gatesim	ASIC, FPGA, custom IC	Gate	IBM PC/XT, PC/AT compatibles	$1295	Fault simulation Virtual memory supported
Viewlogic	Viewsim/SD	ASIC, TTL, ECL, CMOS, memory, FPGA, PLD, μP third-party models also available	Switch, gate, behavioral	IBM, 386, PS/2 compatibles	$7500 to $19,000	Virtual memory supported VHSIC hardware description language available

Notes: 1. Optional unless otherwise noted.
2. Included in package.
3. Only available from third-party vendors.



Pop-up menus make selecting *different functions on Aldec's Susie series simulator easy.*

replace devices or blocks of devices in your simulation.

Behavioral or high-level description models let you design your circuit from the top down. The higher-level descriptions have faster simulation speeds than low-level descriptions, which can save development time.

Stimulus for the simulation

After you've entered the circuit's netlist and models for the components, the only remaining task is generating a set of stimulus or test vectors.

Developing stimulus vectors, and subsequently the correct response for them, is an important and potentially time-consuming part of the simulation process. The simulator can only help you verify whether a circuit design works properly by exercising the circuit simulation with input stimulus and knowing how the circuit should respond.

When developing test vectors, you typically need to concentrate on two different concerns. The first concern is making sure the circuit does everything it should do so that the design meets its specifications.

The second concern is to make sure the design doesn't do anything it should not do. For this you need to verify that the circuit behaves correctly with any legal input, and possibly with illegal inputs.

For example, if you are simulating a design for a circuit that receives its inputs from a bus, then you can test only the legal bus-cycle inputs and ignore what happens with illegal bus cycles. If you think illegal bus cycles will occasionally occur, you should test the circuit design for them. Although your design may not need to function properly with illegal bus cycles, you want to avoid a locked-up condition requiring a system reset. Therefore, you need to generate the test vectors to check out potential problems.

Simulators typically let you generate test vectors using equations, tables, or a mouse. Aldec's Susie series lets you draw test vectors manually, using a mouse, or create them using equations. OrCAD's VST includes a pop-up editor for generating stimulus vectors that lets you define as many as 200 signals. You can generate clock signals in relative or absolute formats.

When you enter your design into the stimulus vectors, you are ready to run the simulation and see the results.

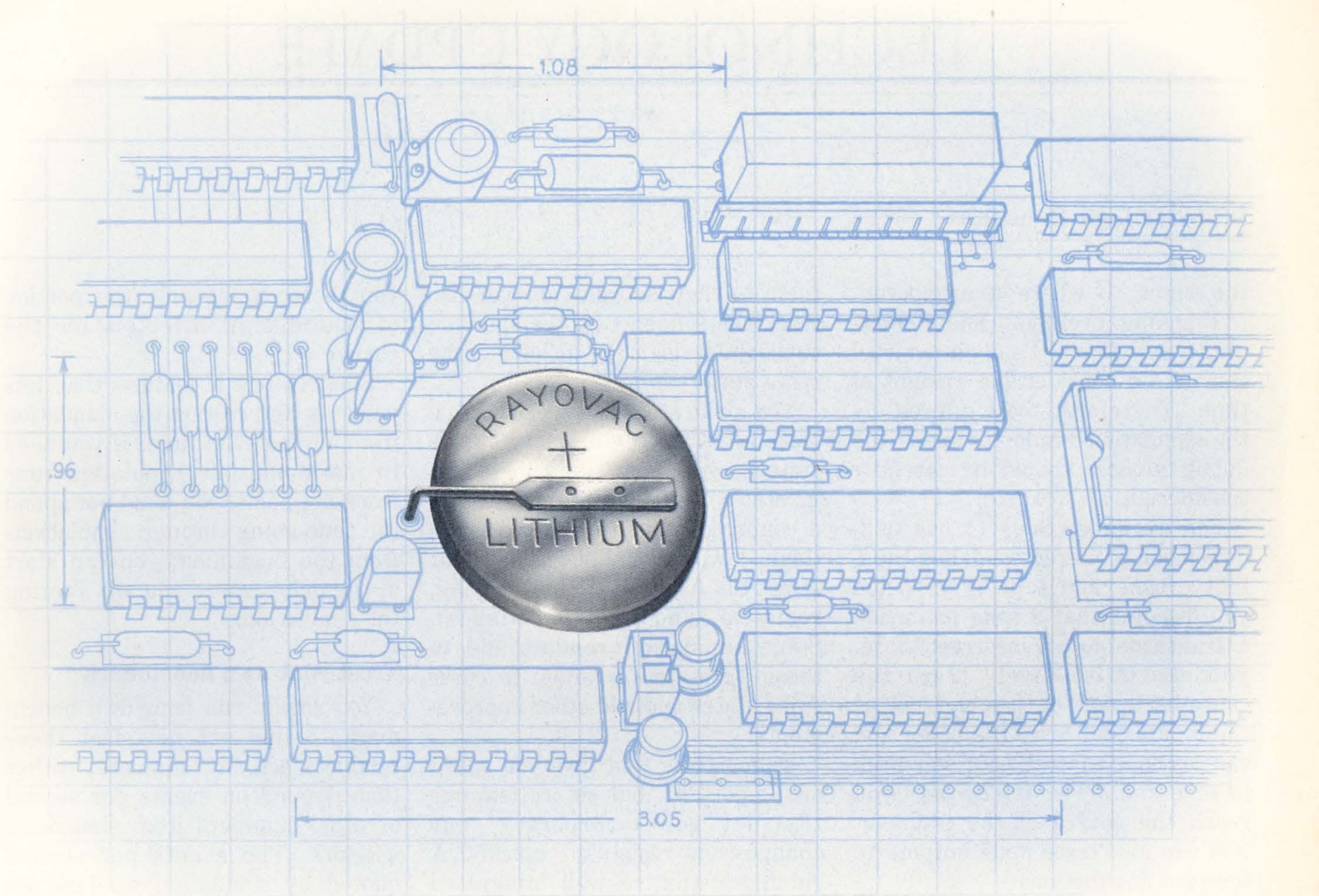
The usual format for simulator output is similar to a logic-analyzer timing display. The simulator presents the signal's state vs time or, in a bused format, it presents data states shown in binary, octal, decimal, or hex.

Simulators don't just leave you to hunt through these outputs for problems. They provide a variety of tools to help you zero in on problems. For example, breakpoints are available on some of the simulators, such as VST and the Susie series. Breakpoints let you look for specific logic conditions occurring when you run a simulation.

Simulators can also look for certain errors automatically. Most will flag setup and hold time violations, minimum pulse-width violations, or bus-contention cases where two devices attempt to drive a bus simultaneously. Some simulators detect race conditions, oscillations, and spikes.

Help for finding bugs

When you run a simulation and see incorrect results, you need to find the source of the problem and fix the error. Something as simple as an inverted output won't take a master sleuth to find and correct. Other errors start much further back in the logic cycle and will take some careful backtracking to get from the point where you observed



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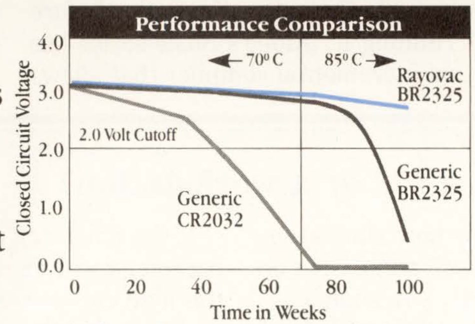

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the error to where it originated.

Tracking problems and debugging a design at the simulation level can take a considerable amount of time. Therefore, tools offered by the simulation vendor to speed the debug process should be carefully considered.

For example, Silos II has a 2-dimensional interactive debug capability (time and topology). When you discover that a node has made a transition to an incorrect state, you can interactively trace the cause backward in time and look at the inputs that drive the node. You can continue to work your way back in time and device inputs until you reach the source of the problem. You can also trace node outputs to forward destinations.

Silos II also supports spike simulation. A spike occurs when two or more edge transitions arrive at a device's input and the edges are spaced closer to each other in time than the propagation delay of the device, causing a state change in the device. Instead of swallowing the spikes, the simulator makes them visible, allowing you to trace them to their source. You can also track the influence of the spike on subsequent logic by following the spike state.

The spike state is a special signal state added to the ordinary twelve states covered by simulators. The 12 states are typically made up of a combination of three logic levels (high, low, and unknown) and four strengths (supply voltage, driving, resistive, and high impedance). Some simulation vendors add to these 12 states in order to cover spike states and add other improvements.

Debug tools that give you speed are important, but so are features that let you incorporate your changes and resimulate quickly. A simulator that is well integrated with a particular schematic-capture software package allows you to change the schematic representation and immediately resimulate with the changes in the design.

You also save time if, after making changes, you don't have to recompile the entire simulation before running it. Aldec's Susie series has an incremental compiler that allows you to recompile only the portion of the design affected by the change.

Silos II has a feature that lets you save and restart the simulation from any point in time. If you need to make multiple simulation runs from one point, you need not spend the time going through simulations from the beginning; you can start at the point where you are altering the simulation.

Trust your own benchmark

You should run your own benchmark to find out how fast these products actually simulate, rather than depend on events per second or other numbers from simulation vendors. The events per second quoted by simulation vendors are not all equivalent. Furthermore, some vendors quote simulation speed by stating a design with X gates and Y stimulus vectors will run in a given amount of time, but that speed depends on how the gates are connected and how the simulation vectors exercise the design. If you run your own simulation benchmarks on simulation soft-

Should you simulate on a PC or a workstation?

Designers sometimes want to know how simulation on personal computers compares with simulation on workstations and mainframes. First, you should note that two of the companies with PC-based simulation (SimuCAD and Viewlogic) also offer simulation products for workstations and mainframes. The software is essentially unchanged, regardless of the computer.

High-end PCs, such as 386- and 486-based computers and Apple Macintosh IIs, are approaching low-end workstation performance. Provided the systems have equivalent amounts of memory, you should get logic-simulation performance close to a low-end workstation.

If the efficiency of the simulation software is comparable, you'd expect greater simulation speed on the high-end workstation than on a high-end PC. Simulation software vendors whose products run on high-end workstations or mainframes like to point out that *their* customers aren't even happy with the speed of simulation on these high-speed computers. Designers simulating large designs will often turn to hardware accelerators to speed simulation.

If you're performing a timing simulation on a 50,000+ gate circuit, you'll probably find a PC-based simulator slow, even if the circuit fits. However, you shouldn't let that discourage you from using a PC-based simulator on smaller designs.

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NEWS

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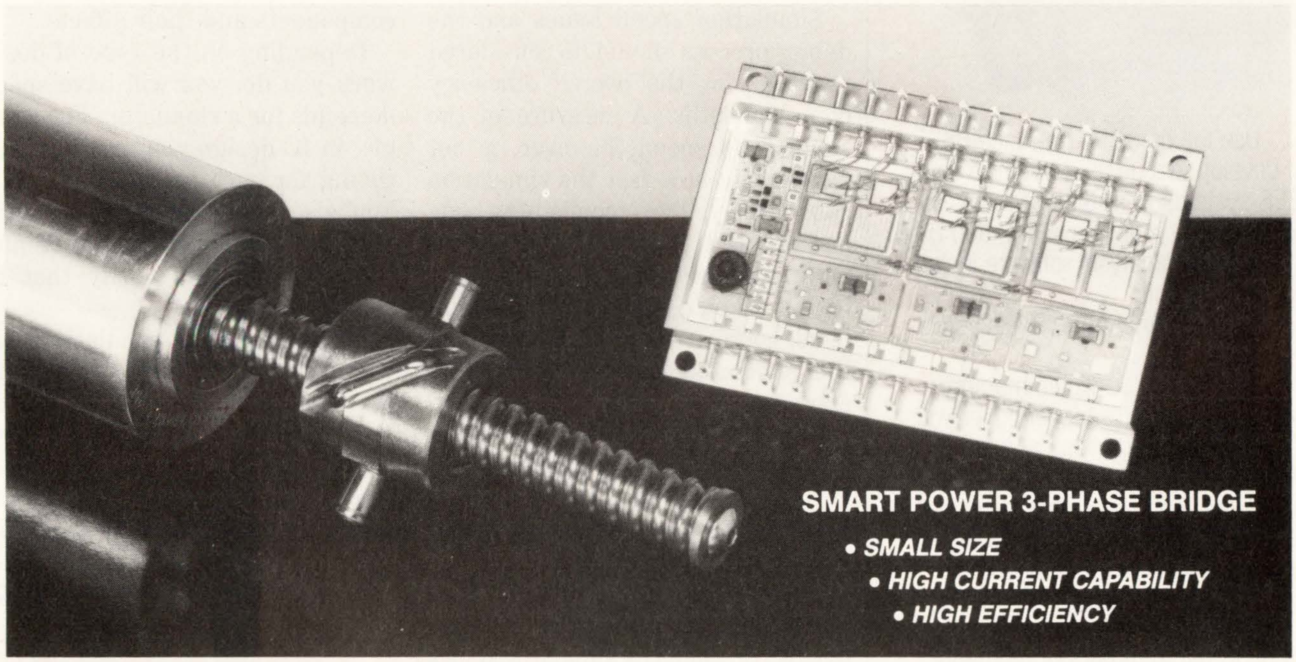

Motor Courtesy of Inland Motor, Kollmorgen Corporation.

That's right! The world is changing with the introduction of the PWR-82331, DDC's new family of motor drive products.

The PWR-82331 30A, 200V, 3-Phase bridge power hybrid consists of six N-channel power MOSFETS and six anti-parallel fast recovery diodes connected into a full 3-Phase bridge driver. Each MOSFET bridge is driven directly from a CMOS input through high and low side drivers without the need for external bias voltages.

Internal protection circuitry prevents in-line transistors from simultaneous conduction, but allows for multiple upper or lower conduction for sine drive or dynamic breaking. A constant voltage drive to control the MOSFETS is used to ensure uninterrupted performance of the drivers even in a motor stall situation — performance that cannot be achieved when a boot-strap configuration is utilized.

The PWR-82331 has its own built-in power source which supplies all the required internal biasing and logic supplies. The Vb input to the internal supply can either be hooked directly to the Vcc pin or to an additional external power source.

This highly efficient bridge uses all N-channel MOSFETS to ensure a very low on-resistance of 0.11 Ohm per leg and 50ns fast recovery power rectifiers to clamp inductive flyback. The PWR-82331 is packaged in a thermally efficient copper case with a typical junction-case thermal resistance of 0.5° C/W and measures only 2.1″W x 3.0″L x 0.375″H. This hybrid is designed to operate from –55° C to +125° C case temperature.

The PWR-82331 can be driven directly from the commutating logic and when combined with a pulse width modulator creates a Servo Motor Controller, which after proper derating, can drive motors up to 6 hp over the full MIL temperature range.

In addition to the PWR-82331, DDC has introduced the PWR-82340 which is a 2-phase version.

For additional product and application information, contact Bob Fryer at 1-800-DDC-1772, x 390, or contact the DDC office nearest you. □

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PC-based logic simulators

ware you are considering, you'll have meaningful results and you'll know more about what the simulator can do.

Simulation speed issues and the debug process should be considered together for the overall efficiency of a simulator. A measure of the simulator's speed, however, is not necessarily how fast the simulation runs after you've compiled the code and started the simulation. What you really need to know is how long it will take to simulate, find problems, correct them, and verify that the simulated design works properly.

The best measure for determining whether a particular logic simulator will work in your application is to try some circuit examples that gave you trouble in the past. If the simulator can find problems that you didn't discover until you had hardware, then the simulator shows promise of saving you time and money.

Some of the problems designers typically have to look for are setup- and hold-time violations and clock setup violations, such as the end of a reset pulse to the beginning of a clock cycle on a flip-flop. You might also be trying to detect glitches on components and their effects.

Depending on the type of design work you do, you will have special demands for a simulator. For example, in IC design you need different timing for each instance of a gate. You also need to transfer routing delays back to the simulator after physical layout to verify that the timing still works.

Most PC-based simulation software vendors have free or nominal-cost demo software that you can obtain to try out simulation. The packages have limitations either in design size or other features, but they will give you a start in evaluating the products for your applications. EDN

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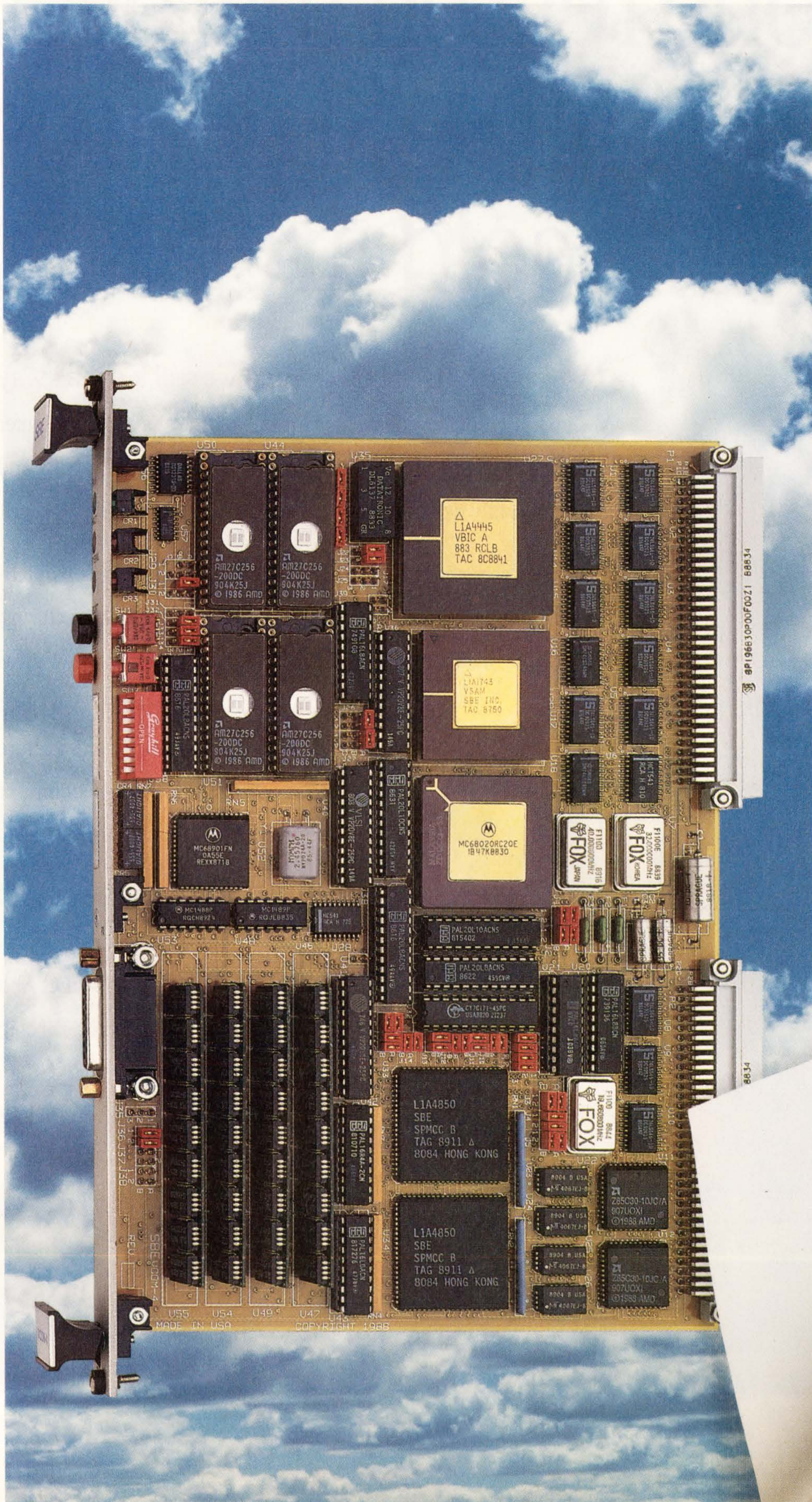

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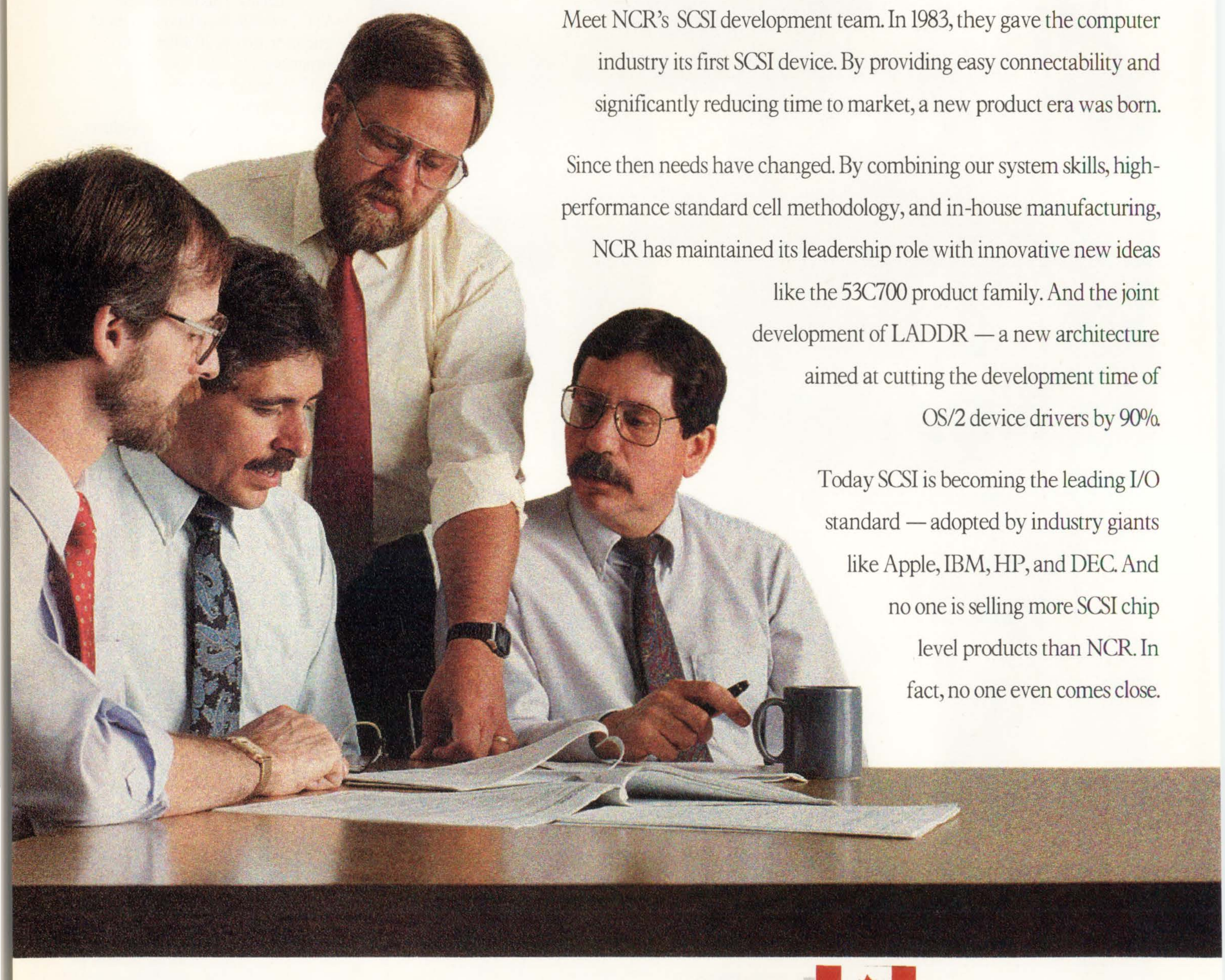
Here's one reason that over half of all SCSI devices sold are NCR.



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Part of the NCR SCSI Development Team: (left to right) **Jerry Armstrong**, Sr.Software Engineer; **Harry Mason**, Strategic Marketing Manager; **John Lohmeyer**, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and **Dave Skinner**, SCSI ProductManager.

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Here's another.

The NCR 53C700 SCSI I/O Processor... So good, *Electronic Design* named it the product of the year.

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Those are just a few of the reasons Electronic Design's "Best of the Digital IC's" award went to NCR's 53C700 last year.

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For the complete story on the NCR SCSI product line featuring the new 53C710, as well as the upcoming SCSI seminars with the NCR SCSI Development Team, please call:

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Creating value

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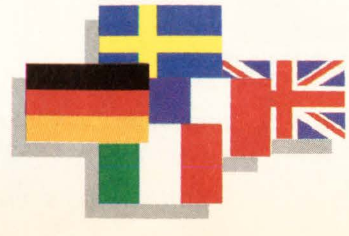

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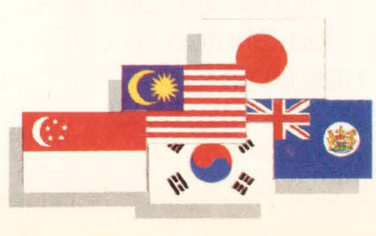

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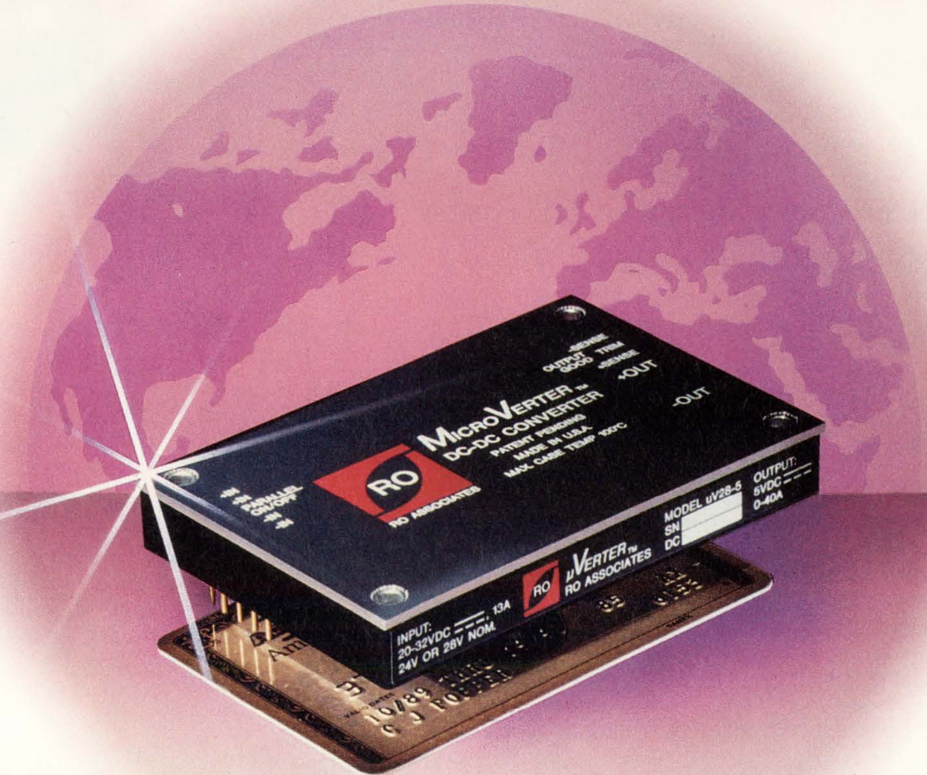

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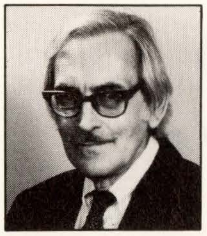
TIMING-DIAGRAM DESIGN TOOLS

Front-end tools reduce schematic drudgery



You can't draw a schematic until you find which timing requirements are critical. A new breed of computer tools takes the pain (and the pencil) out of this task.

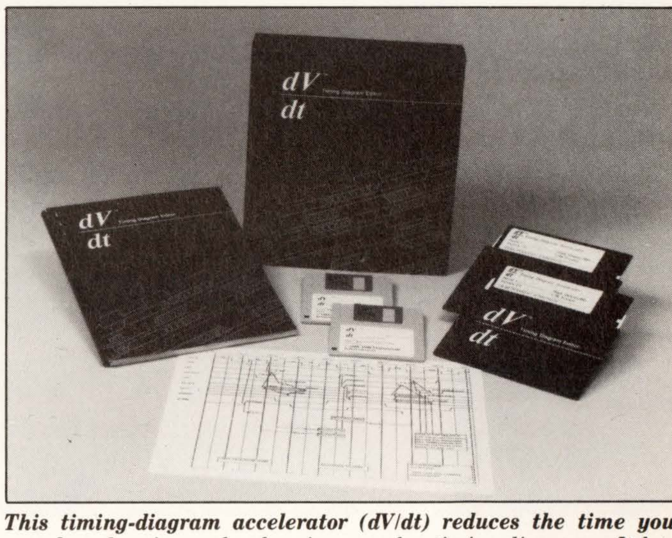
Chris Terry,
Associate Editor

Digital logic designers constantly live on the edge. They are on the edge of a critical waveform until they know it will satisfy complex timing requirements; on the leading edge of technology if their design works correctly; on the trailing edge of disaster if they miscalculate by a few crucial nanoseconds and the product has to be recalled. Engineers spend many hours (as much as 75% of the design phase) drawing timing diagrams, analyzing the circuits these diagrams represent, and calculating the potential effect of component changes at point A on timing tolerances at point B many gates downstream.

You may draw a skeletal schematic while you're working out the timing, but until you know the mutual dependencies of the waveforms, you're in no position to specify the component and IC part numbers that a schematic-capture tool will demand of you. So you take your colored pencils and you draw . . . and you draw . . . and you redraw . . . until the schematic comes out right. It's a repetitious, tedious, and frustrating task. If you make a nasty mess with the eraser, the documentation people may displace a signal edge by a significant amount. If you're tempted not to follow a dependency all the way through the many sheets of the diagram, the components' manufacturing tolerances may combine to make your design unreliable. Creating the final timing diagram is dogwork that often makes you wonder why you ever wanted to be an engineer.

In these days of computer-aided this and computer-aided that, why can't the computer do the dogwork? After all, that's what computers are for, isn't it?

The trouble is that CAE tool designers have so far been busy with the back end of the design. Many board-design tools include a timing simulator that will analyze your captured schematic and use the device characteristics of the automatically placed components to run checks against your design rules. For high-speed boards, some simulators will analyze the schematic and the layout to check for undesirable transmission-line effects.



This timing-diagram accelerator (dV/dt) reduces the time you spend *on drawing and redrawing complex timing diagrams. It lets you set propagation delays, verify requirements, and measure time between signal edges.*

However, these simulators all require

The F80 Programmable Filter

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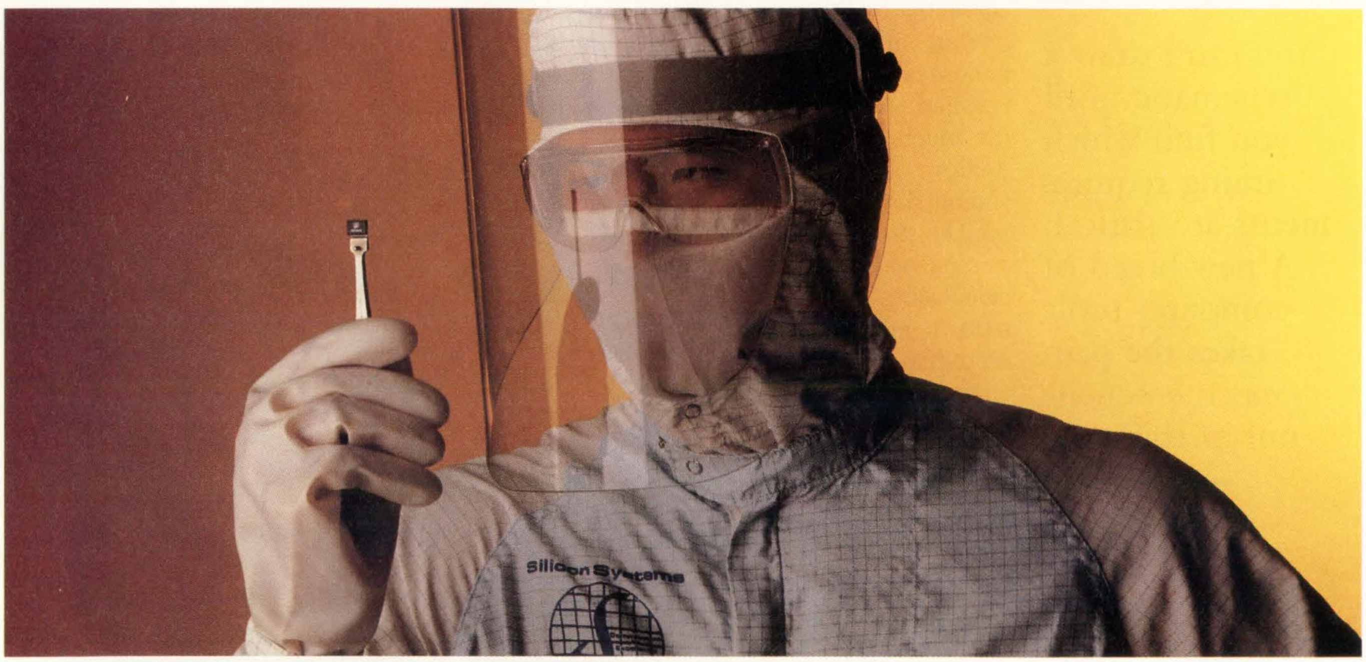

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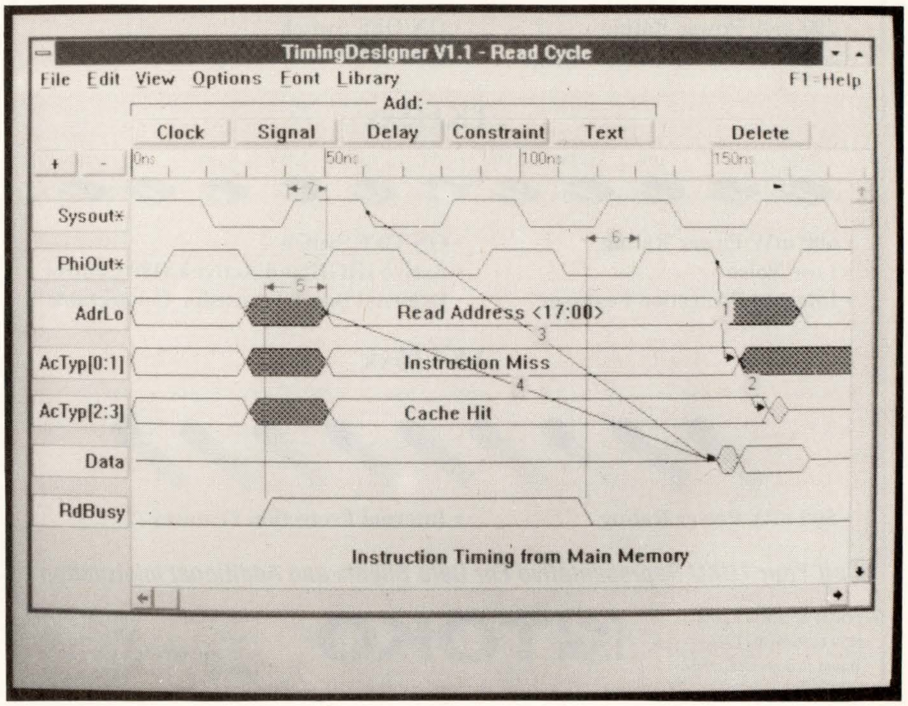
Timing-diagram design tools

that the schematic-capture, layout, and routing phases be complete. They can only verify your work on the waveform diagrams—they're not a substitute for that original work. They will flag timing violations—but then what? You have to go back to the start, either changing device types or modifying the schematic to correct the error. Then you run the simulation over again and hope that your changes have not caused more or different timing violations. These computerized iterations can take as much time and cause as much frustration as manual methods. You may find yourself drawing and redrawing timing diagrams by hand before you draw the schematic just so the simulator will give your design a clean bill of health the first time around.



Timingdesigner lets you specify constraints *and uses color to highlight violations of your design rules.*

Cavalry to the rescue

Two companies have turned their attention to the front end of the design phase and offer timing-diagram design tools that will help you solve your timing problems (*without* paper and pencils). Chronology Corp's Timingdesigner costs $1495 and runs on IBM PC/ATs and compatibles under Microsoft Windows 3.0. Doctor Design Inc's dV/dt Plus also runs on IBM PC/ATs and compatibles—with at least 1M byte of extended memory and DOS version 3.0 or higher—and costs $795. Doctor Design also offers a Macintosh version of dV/dt for $695.

Doctor Design Inc has—perhaps too boldly—trademarked a commonly used expression, "dV/dt," so you can expect another spate of physicist/mathematician jokes at the expense of engineers. Engineers have always been stuck at the bottom of the academic totem pole. Witness the mathematician's definition: "An engineer's a guy who uses a slide rule to multiply 2 by 2, gets the answer to 3.95, and then decides to approximate and call it 4." And a physicist was recently overheard saying about dV/dt: "It's a real nifty program, but if that's the best they can do for a name, maybe they should have stuck to designing doctors."

Dismissing quibbles about naming, both of these programs are valuable tools that can save you hours of drudgery. Indeed, they constitute an innovative breakthrough in a CAE world, which for several years has been refining known techniques rather than developing anything really new.

The programs offer similar facilities. You can enter duty-cycle, duration, phase, and jitter parameters for the clock. The clock generator then automatically generates clock signals throughout the diagram. You can also enter IC constraints such as setup, hold, or minimum pulse width, and the built-in ana-

For more information . . .

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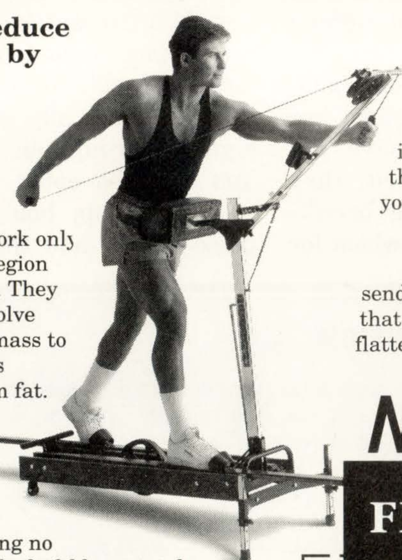

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CIRCLE NO. 6

UPDATE

Timing-diagram design tools

lyzer will highlight any violation of these constraints. You can display signal edges with minimum/maximum uncertainty, computed either on the basis of the known characteristics of standard library parts, or on the basis of variables such as temperature or voltage.

Both programs let you save, retrieve, and print timing-diagram files, so now you can provide accurate diagrams in a form suitable for incorporating into your design documentation. You won't have to risk the potential errors of redrawing rough sketches. The Macintosh version of dV/dt can output the diagrams to any "chooser-selectable" Mac printers, and dV/dt Plus works with all Epson MX series and HP LaserJet series printers. Timingdesigner will work with hundreds of printer, plotters, graphics cards, and monitors through Windows' device drivers.

If you're a Macintosh user, dV/dt is currently your only choice. If you're a PC/AT user running Windows 3.0, Timingdesigner will probably give you the best performance. But if you don't run Windows 3.0, then dV/dt Plus in the DOS environment will still let you jettison those pencils, scrap sheets, and napkins. EDN

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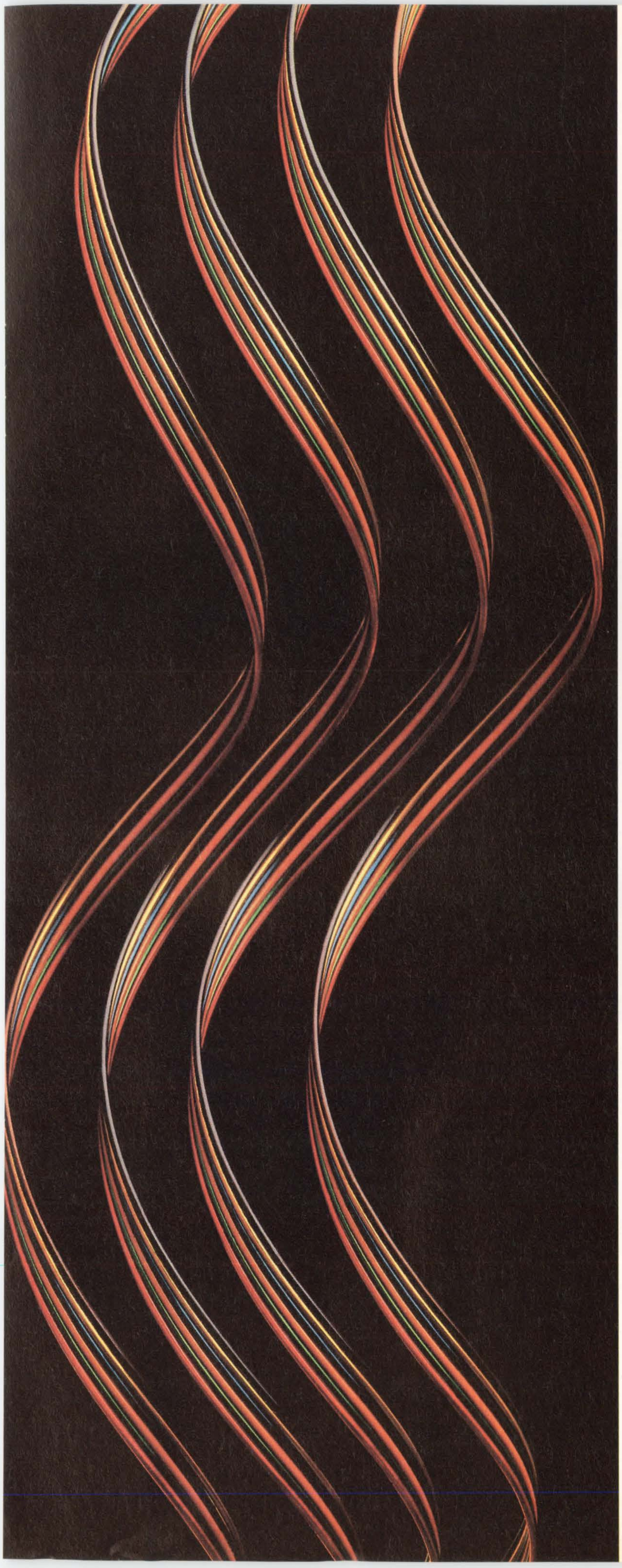

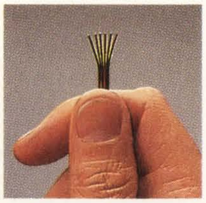

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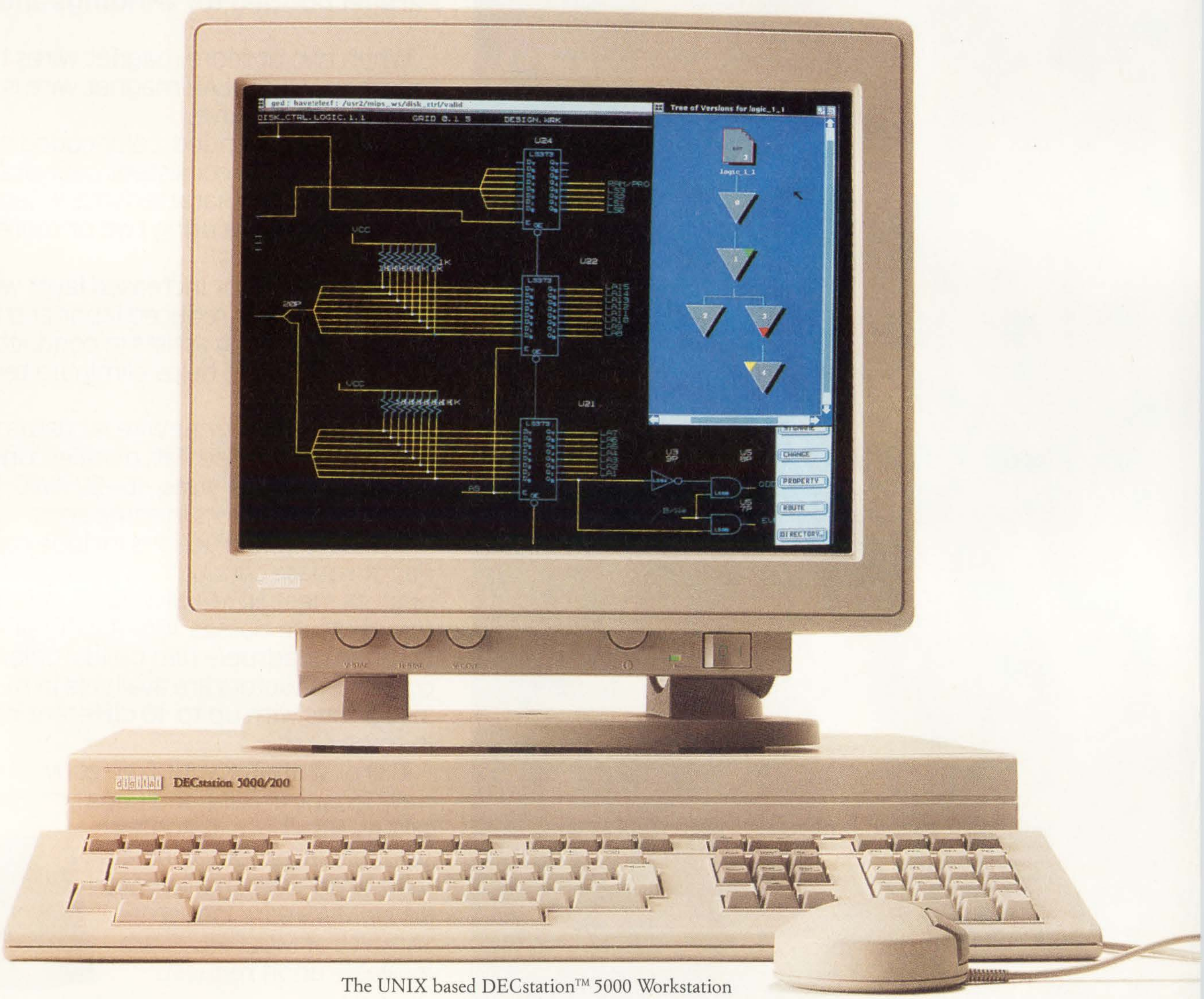


The UNIX based DECstation™ 5000 Workstation digital™

leads by example.

Example #1: Performance

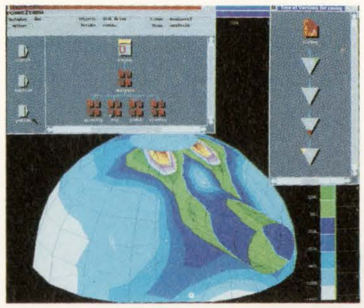
No matter how you measure it, Digital's DECstation 5000 workstation leads all others in performance. Whether it's raw CPU performance, 2D or 3D graphics speed, or price/performance, the DECstation 5000 workstation comes out ahead. In fact, for overall performance, nothing else is close. And we've got the numbers to prove it.

PERFORMANCE COMPARISON CHART (1)	SUN SPARCstation 1+	IBM 320/520	DECstation 5000 cx
Graphics & Windowing (2)	0.24	0.71	1.59
Integer	1.04 (3)	1.34	1.61
Floating Point	1.10 (3)	2.6	1.7
Overall Performance	0.65	1.35	1.63

(1) All data normalized to DECstation 3100. Comparable configurations tested. Geometric mean used to combine results. Performance will vary depending on applications and environment. (2) Graphics and windowing data measured using X11perf benchmark. CPU Integer and Floating Point performance measured from running SPEC V1.0 workload. (3) SPEC performance estimate based on SUN 4/330 results published by Sun Microsystems, Inc.

Example #2: UNIX based Applications

When you run with the leader, you know you're in good company. The DECstation 5000 workstation runs more than 1,500

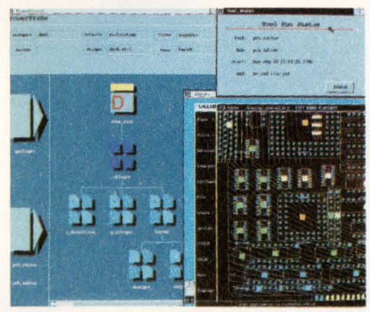


UNIX based applications, including the industry's most popular MCAD and EDA applications.

Example #3: PowerFrame™ for Design Integration.

With Digital's PowerFrame design framework, you can easily integrate the DECstation 5000 workstation with your existing UNIX based EDA and MCAD systems. PowerFrame is the most widely used framework for heterogeneous design management.

And, of course, as the leader in integrated multi-vendor networked computing, you can count on Digital for full service and support. We can help you design, implement and maintain an engineering computing strategy that capitalizes on today's technol-



ogy, while keeping your options open for the future.

For your copy of benchmark test results and a list of available applications, call 1-800-343-4040, ext. 970. These are filled with examples of what you expect from a leader.

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Specs for Hard Drivers.

Maxtor 7080

Simplicity of design makes Maxtor's Cheyenne Series inch-high 80MB 7080 disk drive the most reliable in its class. Compare Maxtor's four-head, two-platter design to Seagate's six-head, three-platter design. Fewer moving parts make Maxtor's drives inherently more dependable.

Power consumption is a very low 2.8 watts, making it one of the lowest in the 80MB class. The 7080 is also Novell Labs certified, and is available with either SCSI or AT interface, giving you flexibility for a winning system.

Exceptionally fast 17ms seek time and 32K cache buffer in the new generation inch-high form factor give Maxtor faster data throughput than the competition.

Call and ask about our entire Cheyenne family of disk drives with capacities from 40MB to 130MB. Don't fall for the off-the-wall claims. Give us a shot and we'll prove Maxtor specs can't be matched. **Call your nearest Authorized Maxtor Distributor.**

3.5-inch Disk Drive Spec.	**Maxtor 7080A**	Seagate 1102A
Seek Time	**17 Msec.**	19 Msec.
Standard Buffer Size	**32K**	8K
Form Factor	**3.5" x 1"**	3.5" x 1.6"
Heads-Disks	**4/2**	6/3
Avg. Power Consumption	**2.8 watts**	9 watts

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EDN EDITORS' CHOICE INNOVATION

Inexpensive 32-bit μP chip seeks embedded systems

While giant semiconductor companies are making 32-bit μP design look so formidable that few start-up companies even dream of developing competitive 32-bit designs, a small German company is ready to do battle. The battleground is the crowded embedded-computer market, where 10-person Hyperstone Electronics is determined to gain a beachhead in its campaign for embedded-system customers. Named the Hyperstone E1, the 85,000-transistor chip operates at a burst rate of 25 MIPS at 25 MHz. The μP requires no external cache, and it operates with external dynamic RAM (DRAM) chips, which it controls directly.

The E1 chip offers an address space of 4G bytes, and it has separate memory and I/O addresses. The chip supplies 19 global and 64 local registers, each of which has 32 bits. Programs can directly address as many as 16 global and 16 local registers. You can also reconfigure the registers in a variable-length stack, using from 2 to 16 frames. Most of the chip's instructions are 16 bits long, although complex instructions can consume as many as 48 bits. Benchmarks yield 38,000 Dhrystones. The throughput results from a combination of pipelined load instructions, an internal 2-stage decode/execute pipeline, and a look-ahead instruction cache.

This chip is not the quixotic dream of an eccentric engineer. Hyperstone's founder and leader is Otto Müller, a computer engineer who is known in Europe for designing computers for Telefunken, Nixdorf, and Triumpf-Adler. After designing computers for these large companies, Müller founded his own company, CTM, which produced computers for businesses. Müller's new company, Hyperstone, is 2½ years old and is already producing μP chips.

Although the company does not fabricate its own devices, it has a foundry in the USA that furnishes them. It has also licensed nonexclusive rights to the chip to Zilog, which currently has working silicon and expects to offer chips in March. Zilog will also offer the chip as a core in its Superintegration ASIC program.

You can purchase the E1 μP chip directly from Hyperstone for $150. However, the company expects the price to drop to less than $50 (10,000) by the end of 1991. A development board, which provides an E1 CPU, 1M byte of DRAM, 256k bytes of EPROM, and an RS-232C I/O port, is available for $1699. An assembler and a debugger cost $350 and $400, respectively. They run on an IBM PC or a compatible computer. You can load instructions and data into the development board through the computer's serial I/O port.

—Jon Titus

Hyperstone Electronics, GmbH, Robert-Bosch-Strasse 11, D-7750 Konstanz, Germany. Phone 07531-67789. FAX 07531-51725.

Circle No. 730

Zilog Inc, 210 Hacienda Ave, Campbell, CA 95008. Phone (408) 370-8000. FAX (408) 370-8056.

Circle No. 731

Driver IC distributes 20 clock copies and offers a primary output of 80 MHz max

You can use the SC3501 BiCMOS 20-copy clock-driver IC to handle clock distribution throughout an entire high-speed-CPU board. The IC outputs TTL-compatible signals with frequencies as fast as 80 MHz. Less than 500 psec of skew characterizes the 20 leading-edge synchronized outputs.

As input, the clock-driver IC requires a signal of double the desired output frequency. A differential ECL input signal from a crystal-controlled oscillator, operating between 5V and ground, provides a high-precision output signal. Optionally, you can drive the IC with TTL signals for low-frequency applications.

The SC3501 IC offers three groups of outputs. The first set of 10 outputs operate at the primary clock frequency of the chip (one-half the input frequency). You can set the second group of five outputs to be identical to the primary output frequency or to operate at one-half the primary output frequency. Likewise, you can set the third group of five outputs to a choice of one-half or one-fourth of the primary output frequency.

All 20 outputs provide waveforms with 50% high/low duty-factor symmetry centered around a threshold of 1.5V. You can adjust the clock-width timing symmetry in ±0.34-nsec increments via strappable input pins.

The outputs include complementary 24-mA-pk source and sink drivers. The outputs also feature internal source termination that minimizes signal overshoot or undershoot without requiring external termination networks. A maximum output slew rate of 2V/nsec minimizes simultaneous output switching noise and distortion. You can also connect the outputs in parallel to drive capacitance loads of 40 pF and higher.

The SC3501, in a 52-pin quad flatpack, costs $17 (1000).

—Maury Wright

Silicon Connections Corp, 6160 Lusk Blvd, Suite C-204, San Diego, CA 92121. Phone (619) 535-0442. FAX (619) 535-1635.

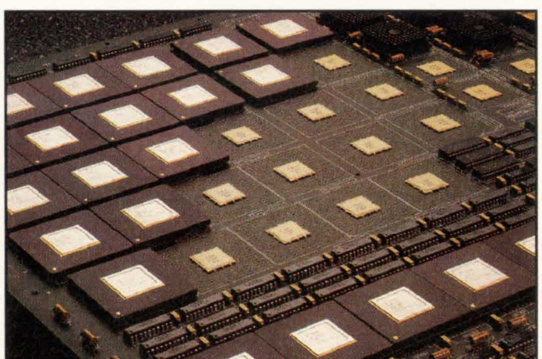
Circle No. 732

CUT FREQUENCY HIGHS DOWN TO SIZE

Micro/Q® 3000 Controls High Frequency Noise From ASICs

Design PGA packaged ASICS or MPUs into your board design and the noise level starts climbing. Surround these PGAs with standard 2 pin decoupling capacitors, and you'll use valuable board space and provide inferior decoupling.

Micro/Q 3000 decoupling capacitors from Rogers provide excellent noise suppression over a wide frequency range. For space savings, they're specifically designed to fit *under* PGA devices such as fully custom ASICs, MPUs and gate arrays - where low noise and high density are essential.



Micro/Q 3000 capacitors fit under PGA packaged ASICs and MPUs.

Featuring the high performance reliability you've come to expect from Rogers, this family of very low inductance decoupling capacitors is through-hole mounted *under* pin grid arrays, PGA sockets, and PLCCs/LCCs mounted in sockets. They are available for all PGAs in a variety of sizes and dielectrics, including X7R and P3J dielectrics for greater temperature stability.

Micro/Q 3000 capacitors. Excellent noise suppression for high performance.

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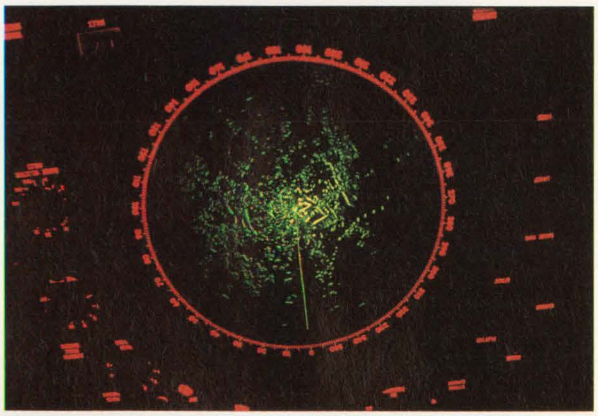
CIRCLE NO. 7

The only 16-bit, 500 kSPS SADC with guaranteed dynamic performance.

For the competition, that's not a pretty picture.

If you're working in spectral imaging applications, our new AD1382 presents a very pretty picture indeed. Because it's the first 16-bit, 500 kSPS single-package sampling A/D converter to offer guaranteed ac performance.



The use of the AD1382 is soaring in radar applications, thanks to its higher level of integration and guaranteed dynamic performance.

With its wide dynamic range and low noise, the AD1382 has a great image with people working in magnetic resonance imaging applications.

The AD1382 delivers guaranteed 100% production tested SNR, THD and peak distortion performance at three input frequencies and over two input ranges – testing that gives you the confidence to design for the best possible noise performance in your system.

You can also feel confident about the cost-effectiveness of the AD1382. It offers a higher level of integration with on-board track/hold and reference.

And since it's a single package, it's easier to design in and uses less board space than more expensive modular or multipackage solutions.

For a better picture of what the AD1382 can do for you, contact Analog Devices at 1-800-262-5643. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

AD1382

A 16-bit 500 kSPS SADC, the AD1382 provides excellent dynamic and static performance in a dual inline ceramic package.

Guaranteed (@25°C, ± 5 V input range):

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- **5 kHz 90 dB min**
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THD & Peak Distortion
- **5 kHz – 90 dB min**
- **100 kHz – 88 dB min**
- **200 kHz – 82 dB min**

DC specifications include:
0.0015% FSR INL, 0.0006% FSR DNL and NMC guaranteed to 16-bits

Other features include:
Zero offset autocalibration
± 5 V, ± 10 V Bipolar input range

An evaluation board for the AD1382 is available.

ANALOG DEVICES

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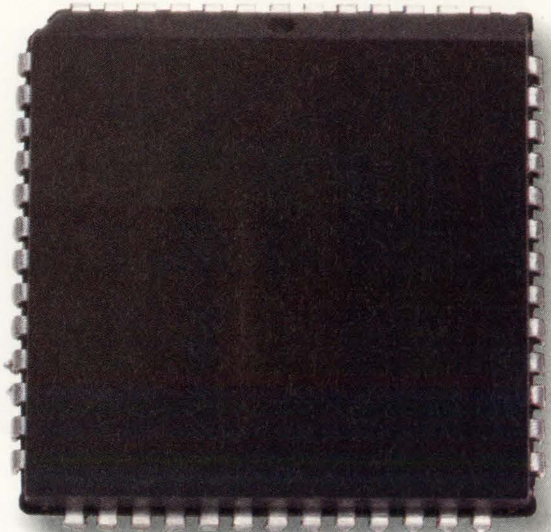
CIRCLE NO. 54

WHAT GOOD IS A BRAIN



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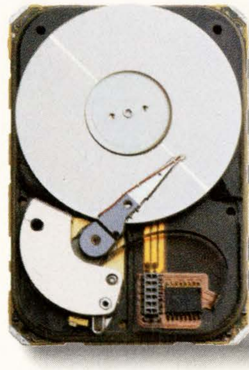
WITHOUT A MEMORY?



To hear most people in the computer business talk, you'd think the only valuable part of a system is its microprocessor.

Maybe they haven't lost their minds. But they've certainly forgotten about the hard drive. And the critical data it stores. Data which can't be easily replaced like a microprocessor.

So it's no surprise that many OEMs are reducing their risk of system failure with disk drives from Conner. Using proven technologies, our high performance drives consistently set the standards for form factor, reliability, and innovation.

That's because at Conner, we work closely with our customers to identify their needs sooner, and fill them faster. Providing them the quickest time to market; with exactly the right product. Plus, we're expanding our worldwide manufacturing facilities to meet growing customer demand around the globe.

All of which makes choosing Conner disk drives a low risk decision.

So call Conner today. The results should be quite memorable.

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Diminutive disk drives cram more and more data onto standard-size 3½-in. media. (Photo courtesy Quantum Corp)

HIGH-CAPACITY 3½-IN. HARD-DISK DRIVES

New 3½-in. hard-disk drives have capacities exceeding 500M bytes and perform as well as high-end 5¼-in. units. The small drives are as reliable as 5¼- and even 8-in. drives and can be found in workstations, file servers, and drive arrays.

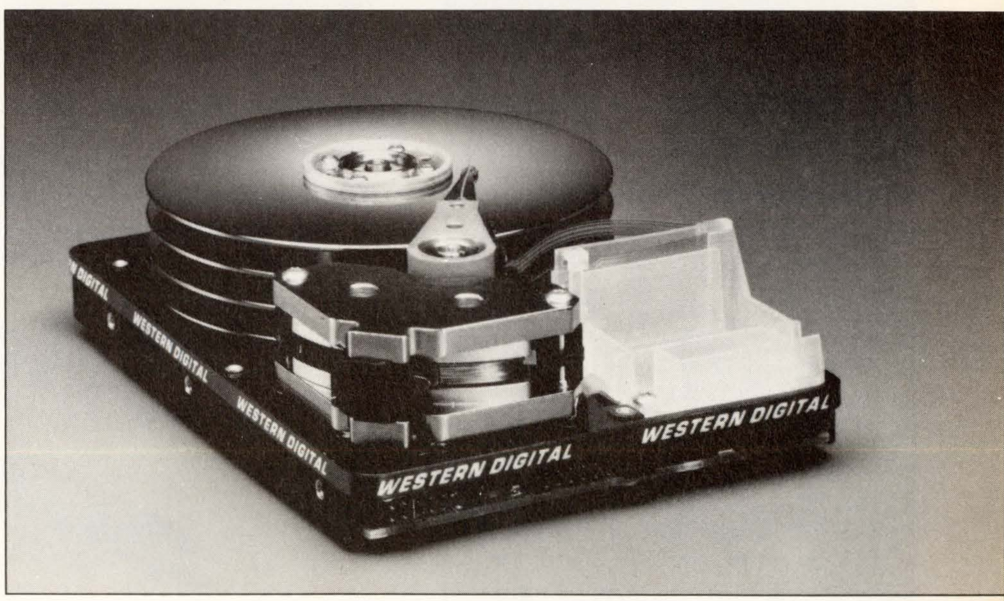
Maury Wright, *Regional Editor*

Most hard-disk-drive trends stay the same: higher capacities, smaller units, faster performance, and cheaper prices. This year is no exception. The latest round of 3½-in. drives includes units that have capacities exceeding 500M bytes. You can now buy 100M-byte 3½-in. drives that stand only 0.75-in. high. Some manufacturers offer drives whose spindle motor speeds exceed 3600 rpm. These drives have low rotational-latency specs and fast read-channel data rates. And many 3½-in. drives are now cheaper than comparable 5¼-in. drives and have MTBF specs as high as 200,000 hours.

In fact, the widespread availability and competitive pricing of 3½-in. disk drives has completely eroded demand for 5¼-in. units with capacities of 200M bytes and less. A year to 18 months ago, you paid a premium for a 3½-in. unit—even in a low capacity such as 30M bytes. Now you can buy 3½-in. units for less than what you'd pay for 5¼-in. drives at capacities of 200M bytes and less—with the exception of sporadic fire sales by manufacturers of 5¼-in. inventory. The discounted street prices of 100M-byte 3½-in. drives have reached $450, and some of the newer drives should drive that price lower within the next quarter.

The newly announced 400M- and 500M-byte 3½-in. drives will soon become the primary choice of designers of workstations and network file servers—applications currently dominated by 5¼-in. drives. The size of the smaller drives also suits them for arrays.

So chances are you'll be looking at 3½-in. disk drives this year unless your upcoming designs require fea-



A cache that adapts to ongoing operations optimizes the performance of Western Digital's WDSP4200 200M-byte 3½-in. drive. The on-drive controller chooses the cache algorithm number of segments and the segment size.

The emergence of 500M-byte $3\frac{1}{2}$-in. drives will erode demand for $5\frac{1}{4}$-in. drives, especially for workstations and LAN servers.

tures that other form factors can better provide. For example, laptop and notebook designs will most likely take advantage of the smaller size of $2\frac{1}{2}$-in. drives. (For more information on advances in $2\frac{1}{2}$-in. drives see **box,** "Capacities of $2\frac{1}{2}$-in. drives approach 100M bytes").

And a few reasons do remain to consider $5\frac{1}{4}$-in. drives. You can buy the larger drives in higher capacities—currently as high as 1.6M bytes. Some $5\frac{1}{4}$-in. drives offer features previously associated only with 8-in. drives. One such feature is split data channels, which doubles the raw data rate a drive can sustain. You can also buy $5\frac{1}{4}$-in. drives with a greater choice of interfaces, notably ESDI and IPI-2 (Intelligent Peripheral Interface), both of which are device-level interfaces. Drives with this type of interface require a host-resident controller board.

The new generation of $3\frac{1}{2}$-in. drives seemingly marks the end of device-level interfaces in disk drives. All the recently announced drives feature either SCSI or IDE (Integrated Device Electronics—also called the AT interface) intelligent interfaces. Drives with intelligent interfaces have embedded controllers, which make technological advances such as multiple-zone recording and on-drive caches and error handling possible. Advances in disk-control and -interface ICs have made the overhead previously associated with intelligent interfaces virtually negligible.

Few drives support ESDI

You must consider drive interface as a key system-design issue. Only a few companies offer device-level interfaces on $3\frac{1}{2}$-in. drives. Some older units have ST-506 device-level interfaces. Microscience International ships 110M- and 123M-byte members of its 5100 family of drives with ESDI interfaces. NCL America Computer Products also offers $3\frac{1}{2}$-in. drives with ESDI interfaces.

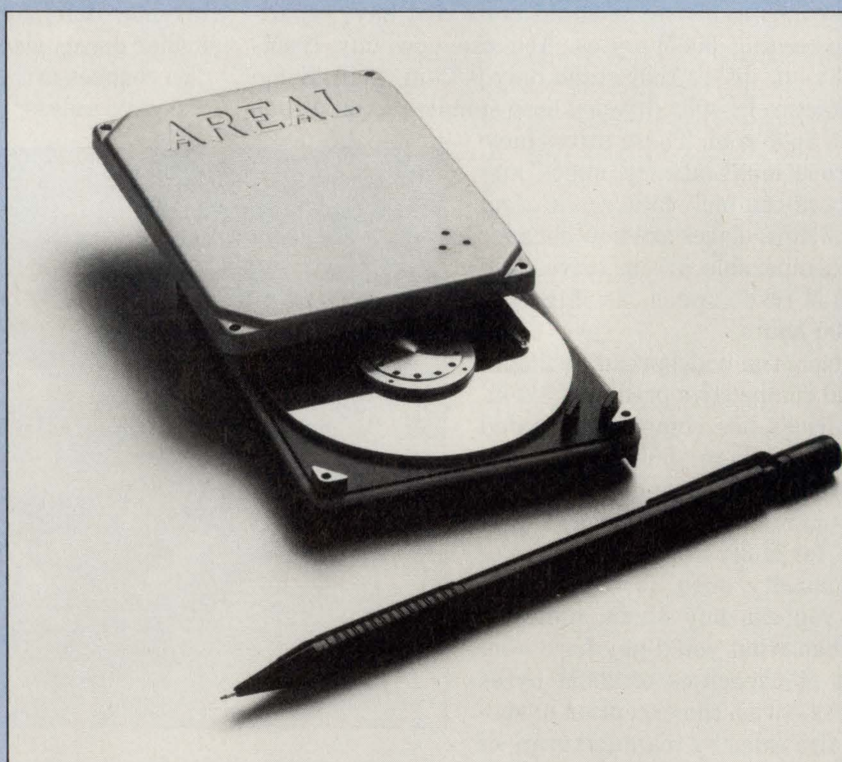
Dave Tovey, Toshiba's marketing vice president, says array designers will demand $3\frac{1}{2}$-in. drives with some type of device-level interface. Tovey thinks a simplified version of the ESDI interface—possibly with

Capacities of $2\frac{1}{2}$-in. drives approach 100M bytes

You can now buy 60M-byte $2\frac{1}{2}$-in. disk drives from several sources, and 80M- and 100M-byte units will soon follow. The drives suit traditional applications such as portable, laptop, and notebook computers. But expect the tiny drives to also find use in applications such as fax machines, laser printers, and even automobiles.

Prairietek leads the $2\frac{1}{2}$-in.-drive field. The company offers the PT-120 20M-byte drives for \$432 (100) and the PT-240 40M-byte drives for \$534 (100). The drives employ one and two platters, respectively. Along with Prairietek, Conner Peripherals and JVC have supplied most of the $2\frac{1}{2}$-in. drives shipped to date. Most of these units have been 20M-byte drives.

Several other companies have recently announced $2\frac{1}{2}$-in. drives, and more will soon follow. The 40M-byte drives are now main-



The $2\frac{1}{2}$-in., 63M-byte MD-2060 hard-disk drive from Areal Technology stores data on one glass-substrate platter.

no signal drivers because the cable runs would be short—might suit such applications. Neither Toshiba nor any other company currently offers a 3½-in. drive with such an interface, however, and no standard for such an interface exists. Most of the new IDE and SCSI drives do have some features, such as spindle synchronization, that support array designs.

The IDE and SCSI offerings should suit your needs for traditional system designs. Intelligent drives typically add less than one millisecond of overhead to I/O operations. The IDE units work only in IBM PC/AT bus systems and offer plug-and-play compatibility with the original IBM PC/AT ST-506 disk controller. In fact, newer IBM PC/AT-compatible mother-board chip sets from companies such as Chips and Technologies (San Jose, CA) and VLSI Technology (Tempe, AZ) regularly include the simple IDE host interface. A single header connector on the mother board provides the primary I/O capability. IBM has developed a similar interface for its Micro Channel-based systems and, along with Conner Peripherals, manufactures compatible disk drives.

SCSI drives require nonstandard operating-system drivers or BIOS additions for use on IBM-compatible personal computers. The drives offer performance advantages for multitasking operating systems such as Unix or Novell's NetWare that overlap I/O requests. SCSI drives are compatible with many other peripherals. You can use a single SCSI host adapter to connect tape drives, CD-ROM drives, scanners, and printers, as well as disk drives. Outside the world of IBM-compatible personal computers, the computer industry has endorsed SCSI as the interface of choice for most systems with less-than-mainframe power.

These high-capacity drives all support the SCSI-2 standard. Less than a year old, SCSI-2 formally defines a common command set for disk drives and other peripherals. The standard adds error-recovery features and command tags that facilitate command queuing. SCSI-2 also defines optional wide and fast data transfers. The wide transfer option defines the expansion of the interface from an 8-bit to a 16- or 32-bit bus. The fast option doubles the bus speed during synchronous transfers to 10 MHz, which results in a 10M-byte/sec rate on an 8-bit implementation.

The SCSI-2 drives available now don't support the optional wide or fast data transfers. Virtually all manufacturers of high-capacity 3½-in. drives plan to support

stream products, and higher-capacity drives are now emerging. Toshiba, for example, entered the market with the 40M-byte MK-1122FC drive that weighs 6.3 oz. The single-platter drive costs \$425 (100), includes a 32k-byte cache, and has an average seek time of 23 msec. The company also offers a 20M-byte version of the product. Quantum announced a single-platter 40M-byte drive, and Seagate offers a single-platter 20M-byte unit and a dual-platter 40M-byte drive.

Areal Technology, Conner Peripherals, and Western Digital have announced 60M-byte products. Western Digital's \$325 (100) 30M-byte WDAB130 and \$495 (100) 60M-byte WDAH260 drives include one and two platters, respectively. When combined with the company's 7600 Core Logic family of mother-board chip sets, the drives offer eight power-saving modes for battery-powered notebook computer operation. The combination also yields zero-wait-state memory access between the host CPU and the IDE controller. Typically, systems with IDE drives insert one or two wait states when accessing the controller.

Conner Peripherals includes 30M, 40M, and 60M-byte drives in its Pancho series of drives. The drives' prices range from \$395 to \$495. The CP-2064 60M-byte product employs two platters and features a 19-msec average seek time. The drive requires 1.3W and can withstand shocks of 100g.

Areal Technology's MD-2060 uses a single platter to store 60M bytes. The drives use glass-substrate media—a holdover from Areal's previous attempts to enter the 3½-in. drive market with a 1-in.-high 100M-byte drive. Areal now has a manufacturing agreement with Sanyo (Tottori City, Japan), and Sanyo holds an equity position in Areal. Evaluation units of the drive cost \$995, and Kirby says production units will be available in the first quarter.

Around midyear, expect to see 80M-byte 2½-in. drives. Prairietek has announced plans to build a 2-platter 80M-byte unit. Conner Peripherals offers a 0.75-in.-high, 85M-byte 3½-in. drive. If Areal succeeds in producing its 60M-byte unit on schedule, you may also see a 120M-byte, 2-platter offering from the company in the second half of the year. Finally, expect Maxtor to enter the market during the first half of the year with a drive designed at its Colorado division (formerly Miniscribe). Given Maxtor's reputation, expect the drive's capacity to exceed that of currently announced products.

New 3½-in. drives eschew device-level interfaces such as ESDI completely and instead offer the choice of SCSI or IDE interfaces.

fast transfers, at least as an option. Vendors of disk-controller ICs are busy adding the capability, so expect widespread availability of drives with the feature after midyear. The wide SCSI-2 data-transfer option should be more popular on 5¼- and 8-in. drives.

Choosing a disk-drive supplier will prove to be a much less exact science than choosing an interface. In the 400M- to 500M-byte product category, the list of suppliers reads like a who's who of the disk-drive industry. (See **Table 1** for suppliers and drive specifications.) Hewlett-Packard, Hitachi, IBM, NEC, Quantum, Seagate, and Western Digital all offer 3½-in. drives with capacities exceeding 400M bytes. IBM and Western Digital sell the same drive. IBM designed and builds the drive and handles sales to large customers. Western Digital sells the drives to smaller OEMs and through distribution.

Conner Peripherals, Fujitsu, Maxtor, and Rodime all offer drives with capacities exceeding 500M bytes. The companies offer depopulated versions of the drives (versions with one or more disk platters removed) that have capacities of 200M to 400M bytes. The 400M- and 500M-byte drives all have similar performance specs, but you should evaluate the actual performance of the drives in your application. Be aware that manufacturers measure performance in different ways, so comparing specified seek times or data rates is not necessarily like comparing apples and apples.

Fast spindle speed reduces latency

The Fujitsu M262XSA/T and Seagate ST1480 drives deserve note in the performance area. The drives feature a state-of-the-art average seek time of 12 msec. They have rotational speeds of 4400 rpm; most other drives have rotational speeds of 3600 rpm. The faster spin rate results in an average rotational latency spec (the time required for the platters to rotate half a turn) of 6.8 msec, compared with 8.3 msec for most competing products. The faster rotation also results in a faster raw data rate—approximately 3M bytes/sec.

Table 1—Representative high-capacity 3½-in hard-disk drives

Manufacturer	Model	Formatted capacity (M bytes)	Price	Number of disks	Track density (tpi)	Bit density (bpi)	Data encoding scheme	Spindle speed (rpm)	Average seek time (msec)
Conner Peripherals Inc	CP-3200	212	$660	4	1700	31,800	2, 7 RLL	3485	16
	CP-3500	510	$1295	6	2100	42,763	2, 7 RLL	3609	12
Fujitsu America Inc	M262XSA/T	520, 425, 330	$1750, $1500, $1250	6, 5, 4	1751	46,383	1, 7 RLL	4400	12
Hewlett-Packard Co	C2235S	422	$1225	5	1850	42,000	2, 7 RLL	3600	13
Hitachi America Ltd	DK314	419	$1780 (100)	7	1800	44,200	2, 7 RLL	3600	16.8
	DK312	251, 209	$975, $880 (100)	6, 5	1660	38,800	2, 7 RLL	3600	16.8
IBM Corp	WDS/A-3160	206	$625 (500)	4	1517	31,700	1, 7 RLL	3600	16
	*0661-371	320	$1000 (1000)	8	1201	37,341	1, 7 RLL	4316	12.5
	*0661-467	400	$1575 (1000)	8	1469	38,427	1, 7 RLL	4316	11.5
Maxtor Corp	LXT-213	213	$930 (100)	4	1600	28,000	1, 7 RLL	3600	15
	LXT-340	340	$1600 (100)	4	1600	44,000	1, 7 RLL	3600	13
	LXT-535, 437	535, 437	$1450, $1250 (100)	6, 5	1600	44,000	1, 7 RLL	3600	13
Microscience International Corp	7200	200	$1350	4	1561	37,341	2, 7 RLL	3600	18
NCL America Computer Products Inc	9220	200	$895	5	1378	29,700	2, 7 RLL	3565	16.5
NEC Technologies Inc	D3000	425, 330	$1200, $1000 (1000)	5, 4	2000	48,982	1, 7 RLL	3600	14
Quantum Corp	210S/AT	210	$750 (100)	4	1414	30,000	1, 7 RLL	3606	15
	425S/AT,330S/AT	425, 330	$1595, $1350 (100)	5, 4	1695	37,146	1, 7 RLL	3606	14
Rodime Inc	3004T	540, 426, 331	$1495, $1295, $1050	6, 5, 4	1905	38,000	1, 7 RLL	3600	14
Seagate Technology Inc	ST1239	210	$910	5	1543	28,103	2, 7 RLL	3600	15
	ST1480	426, 340, 331	$1950, $1855, $1740	5, 5, 4	1760	36,000	1, 7 RLL	4400	14, 12, 14
Western Digital Corp	ADP4200	212	$650 (1000)	4	1575	56,000	2, 7 RLL	3610	16
	*WDSC8320	320	$1350 (1000)	8	1201	37,341	1, 7 RLL	4316	12.5
	*WDSC8400	400	$1575 (1000)	8	1469	38,427	1, 7 RLL	4316	11.5

Key: N/A = Not applicable.
N/S = Not specified.

*IBM and Western Digital both sell these drives; IBM sells them only in large OEM quantities.

The features of intelligent controllers can sometimes improve the performance of disk drives beyond the capabilities of the drive hardware. Quantum has offered a multisegment cache on its drives for years. Its newest Prodrive 330 and 425 products include a 256k-byte cache. The controller continues to read sequential data after an I/O request completes. The drive can service subsequent requests with no seek time or rotational latency (typically close to 20 msec) on cache hits.

Drives with this cache implementation can continue to prefetch data and service incoming I/O requests simultaneously with no extra command overhead. Thus, a new I/O request never interrupts a prefetch operation that might be retrieving the requested data. On cache hits, the controller can continue a prefetch operation and transfer the requested data from the cache at the same time.

The 4400-rpm spindle speed of Seagate's ST1400 family of drives results in an average rotational latency of 6.8 msec and disk data-transfer rates as fast as 3M bytes/sec.

Stigma remains on write caches

You can also specify a write cache as an option on Quantum's drives. Product Marketing Manager John Klonick says that 50% of all I/O requests write data; a cache speeds such operations by holding data temporarily. Traditionally, system designers resist write caches because a system or power failure could result in lost data. Klonick points out that the typical Unix system has 8M bytes of data in main memory that disappear when failures occur, but only a few kilobytes are lost on the drive.

Track-to-track seek time (msec)	Disk data rate (M bits/sec)	Recording zones	MTBF (hours)	Cache size (k bytes)
5	12	N/A	50,000	64
4	16	N/A	100,000	256
3	19 to 24	4	200,000	256
3	14.1 to 20.6	3	150,000	64
7	14	N/A	150,000	64
7	16	N/A	150,000	32
5	12	N/A	45,000	32
4	16	N/A	150,000	64
3	16	N/A	150,000	128
3	9 to 15.7	6	150,000	32
3	13.3 to 20.5	8	150,000	128
3	13.3 to 20.5	8	150,000	128
4	12.5	N/A	60,000	32
3.8	10	N/A	50,000	64
N/S	19	N/A	50,000	32
4	10.8 to 16.3	8	50,000	64
4	12.2 to 21.7	8	150,000	256
3	13.6 to 21.6	8	100,000	256
4	10	N/A	150,000	64
2.5	17 to 25	26	150,000	64
5	12.6	N/A	50,000	64
4	16	N/A	150,000	64
3	16	N/A	150,000	128

Other companies have become serious about caching as well. For 400M- and 500M-byte 3½-in. drives, a 256k-byte cache is the rule rather than the exception. Conner Peripherals includes a 4-segment, 256k-byte cache on its CP-3500 drive. Previously, the company offered a simple 1-segment read-ahead buffer.

Quantum offers a controller feature called read on arrival. The drives can attempt to read data immediately upon arriving at the desired track without waiting for the heads to settle for a specified period. When the read is successful, the drive sometimes eliminates the latency caused by a full rotation of the disk. Of course, the technique can increase seek errors, so you can disable the feature with software.

In addition to performance, consider reliability and cost when choosing a 3½-in. drive. Manufacturers of disk drives have raised the MTBF spec of their products across the board in the last year. Hewlett-Packard started the trend by specifying an MTBF of 150,000 hours and a warranty of five years on all its drives. Fujitsu followed with a 200,000-hour spec on its products. Both companies have also published papers detailing the derivation of their published MTBF specs.

Other manufacturers have been less forthcoming with detailed information on drive MTBF specs. Manufacturers should explain the theoretical basis for a MTBF spec. Accelerated life testing should back up the theory. And field data along with ongoing life testing should further substantiate the spec.

Consider overall drive design, also, as an indicator of how producible and reliable a drive might be. A drive's design can also subtly indicate how reliable the company's next-generation product might be. Most manufacturers have specific technological strongholds that influence their drive design and how they achieve high disk-drive capacities. You can always increase a drive's capacity yourself by adding platters or increasing the bit or track density. Multiple-zone recording can boost a drive's capacity by as much as 50% and is virtually free once designed in. Also called zone-bit recording (a Seagate trademark), multiple-zone recording requires that the drive surface be divided into concentric zones. The outer tracks have more sectors than inner tracks and store more data than the inner tracks store.

Try to judge which drive-design parameters a manufacturer drives to the edge to achieve high capacities. Maxtor, for example, uses six platters, 1,7 RLL data encoding, and 8-zone multiple-zone recording to achieve the 535M-byte capacity of its LXT-535 drive. Conner Peripherals chose not to use multiple-zone recording in its 510M-byte CP-3500. The company achieved the capacity of that drive by pushing the track density to 2100 tpi; Maxtor's product has a track density of 1600 tpi.

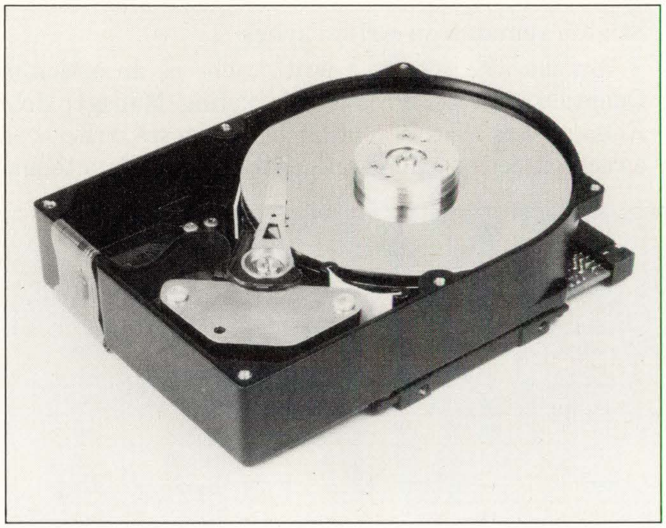
RLL boosts capacity and tightens margins

Michael Gluck, senior vice president of Fujitsu's Computer Products Group, warns that you should watch out for the data-encoding scheme drive manufacturers use. Gluck points out that 2,7 RLL data encoding offers a 50% capacity boost compared with MFM encoding; 1,7 RLL offers a 33% relative increase. Gluck says 2,7 encoding results in tighter read-channel window margins and a potentially less-reliable drive. Fujitsu's M262XSA/T uses 1,7 RLL coding, six platters, and 4-zone multiple-zone recording. In practice, manufacturers have proven that 2,7 RLL encoding will work reliably. However, soft read errors that don't show up as drive failures cause retries and hurt drive performance.

Hewlett-Packard, NEC, Quantum, and Seagate have not announced 6-platter drives yet and, therefore, have no 500M byte products. However, you can expect such products in the future. IBM and Hitachi use more than six platters in their 400M-byte products. IBM's Model 467 has eight platters, and Hitachi's DK314 has seven.

IBM and Hitachi chose to face stiffer packaging requirements and the associated head spacing and aerodynamic problems rather than push bit or track density to achieve high-capacity drives. Neither company currently employs multiple-zone recording. Thus, they have the potential to double the present capacities of their drives without adding more disks. For now, more heads and disks translate into higher cost.

Choosing a 3½-in. drive with a capacity of 100M- to 200M bytes typically requires more attention to cost than to any other detail. Conner Peripherals' CP-3100 family of drives has been among the most popular 100M-byte drives, and mail-order houses sell the product for less than \$500. Several Seagate drives in the 100M-byte range have suggested list prices of approximately \$500. Kalok just introduced the KL3100 100M-byte 3½-in. drive. You can expect discounted street prices to near \$400 after midyear.



Synchronous 10M-byte/sec SCSI-2 data transfers suit the 540M-byte Rodime 3004T drives for use in workstations and file servers. The drives also feature spindle synchronization for array applications.

You also have various sizes of 3½-in. drives to choose from in the 100M-byte range. Most of the drives are 1.625 in. high—the standard full height for a 3½-in. product—but over the last two years, several manufacturers have introduced 1-in.-high drives.

Conner Peripherals, Fujitsu, Maxtor, Quantum, Rodime, Seagate, Teac, Toshiba, and Western Digital have introduced 1-in.-high 3½-in. drives that store more than 100M bytes. You will find differentiating the drives' performance specs tough, so be sure to test the drives in your system if performance is a prime concern. Other key parameters include power consumption, noise level, and environmental specs.

The 1-in.-high drives assume many of the features present in full-height drives from the same manufacturers. MTBF averages 100,000 hours, and the products include caches—albeit smaller ones than the full-height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drives. Western Digital, for example, includes an adaptive 64k-byte cache on its 125M-byte AC2120. The controller monitors drive activity and adjusts the cache configuration during operation. For example, the controller can increase segment size while decreasing the number of segments available and vice versa.

You can buy a 0.75-in.-high, 85M-byte drive from Conner Peripherals, the $495 CP-4084. You can fit two of the drives into the space a single full-high 3½-in. drive requires. Thus, products should succeed in midlife system redesigns and updates and in the upgrade aftermarket.

Looking ahead, you can expect to see 1G-byte 3½-in. drives by this time next year. Fujitsu's Michael Gluck predicts that by 1998 the technology will exist for drives with areal densities of 1G bit/in.^{2}—10 times the density of the newest 500M-byte 3½-in. drives. The downsizing trend will not stop soon. Sherri Besser, Western Digital's marketing manager of 2½-in. drives, says these drives will cost less to manufacture than 3½-in. drives in two years. And some industry insiders have started talking about a new form factor that uses 1.8-in. media. EDN

Article Interest Quotient (Circle One)
High 485 Medium 486 Low 487

Manufacturers of disk drives

For more information on disk drives such as those discussed in this article, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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NCL America Computer Products Inc
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FAX (408) 943-0689
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Rodime Inc
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Toshiba America Information Systems Inc
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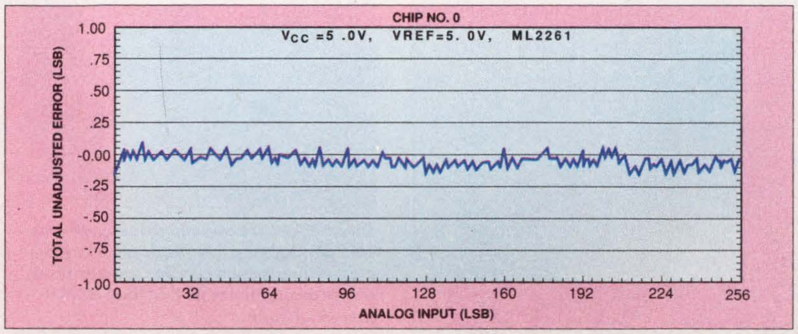
Devices are now available in standard 20-pin DIP or surface-mount PCC packages, with 100-unit prices beginning under $9.00.



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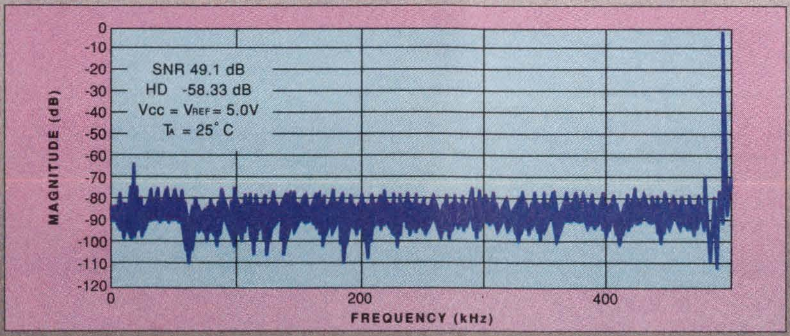
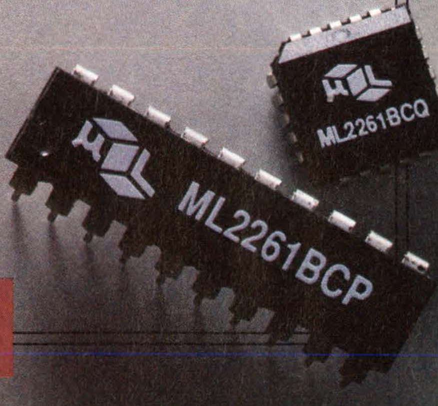


The ML2261 maintains ideal signal-to-noise ratios independent of increasing analog input frequencies to 500kHz.



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TAKE A LOT OF THE COSTS OUT OF CIRCUITS ASSEMBLY

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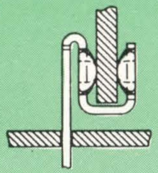
Inconsistent assembly steps. Time-consuming inspection procedures. Damage to existing connections on pre-populated boards. Expensive rework. All of these are significant cost factors in other circuits assembly methods that are eliminated by NAS solder and flux bearing edge clips. The result is a faster, less costly circuits assembly process.

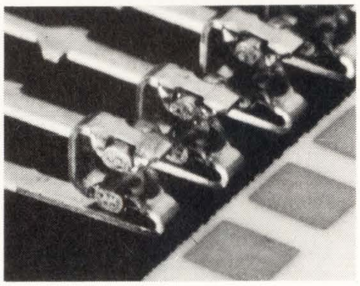
With NAS solder and flux bearing edge clips, solder paste, solder and flux dipping and board clean-up — steps in other methods that are inconsistent and yield high rates of rejects — are replaced by simple, one-step lead attachment and reflow operations. These operations consistently produce 100% solderability.



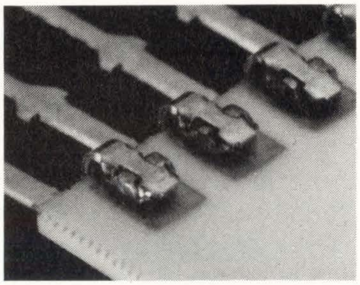
Because bonding of clips to conductor pads can be accomplished without raising the temperature of pre-populated boards to reflow levels, there is no damage to existing connections. Most, or all, of the inspection procedures required by other methods are unnecessary, and expensive rework is a thing of the past.

Preforms on edge clip terminals contain precisely the right amounts of the proper solder and flux for each application, and the exclusive NAS "Claw" grip holds each preform.

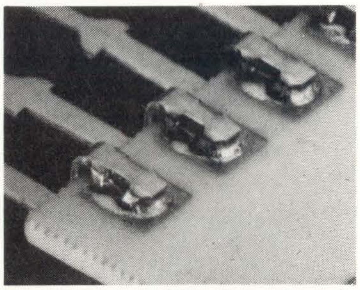
The simple, efficient method of applying NAS solder and flux bearing edge clips:



Direct contact between solder preforms and conductor pads produces a beneficial wiping action as clips are attached, either manually or with a lead attachment machine.



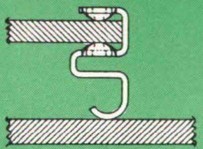
Interference fit holds clips firmly in position for reflow. Top and bottom preforms are reflowed in one operation using any method that raises temperatures to reflow levels.



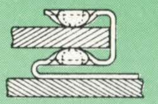
Precise amounts of the right solder and the shape of the "Claw" grip provide control of solder flow without a solder stop. This assures perfect mechanical and electrical bonding without wicking or bridging.

Unretouched Macro Photography

This unique grip design provides direct contact between solder and conductor pads, a beneficial wiping action as clips are attached, and positive control of solder flow. A single reflow operation for top and bottom preforms — using any method that raises temperatures to reflow levels — produces perfect solder joints every time.



Converting to the NAS solder and flux bearing circuits assembly method requires no specialized labor skills and no significant capital investment. Immediately, you can be producing more reliable, better performing products . . . in far less time and at significantly less overall cost.



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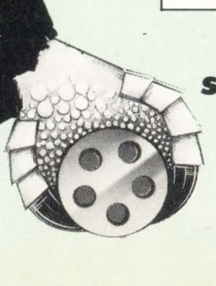

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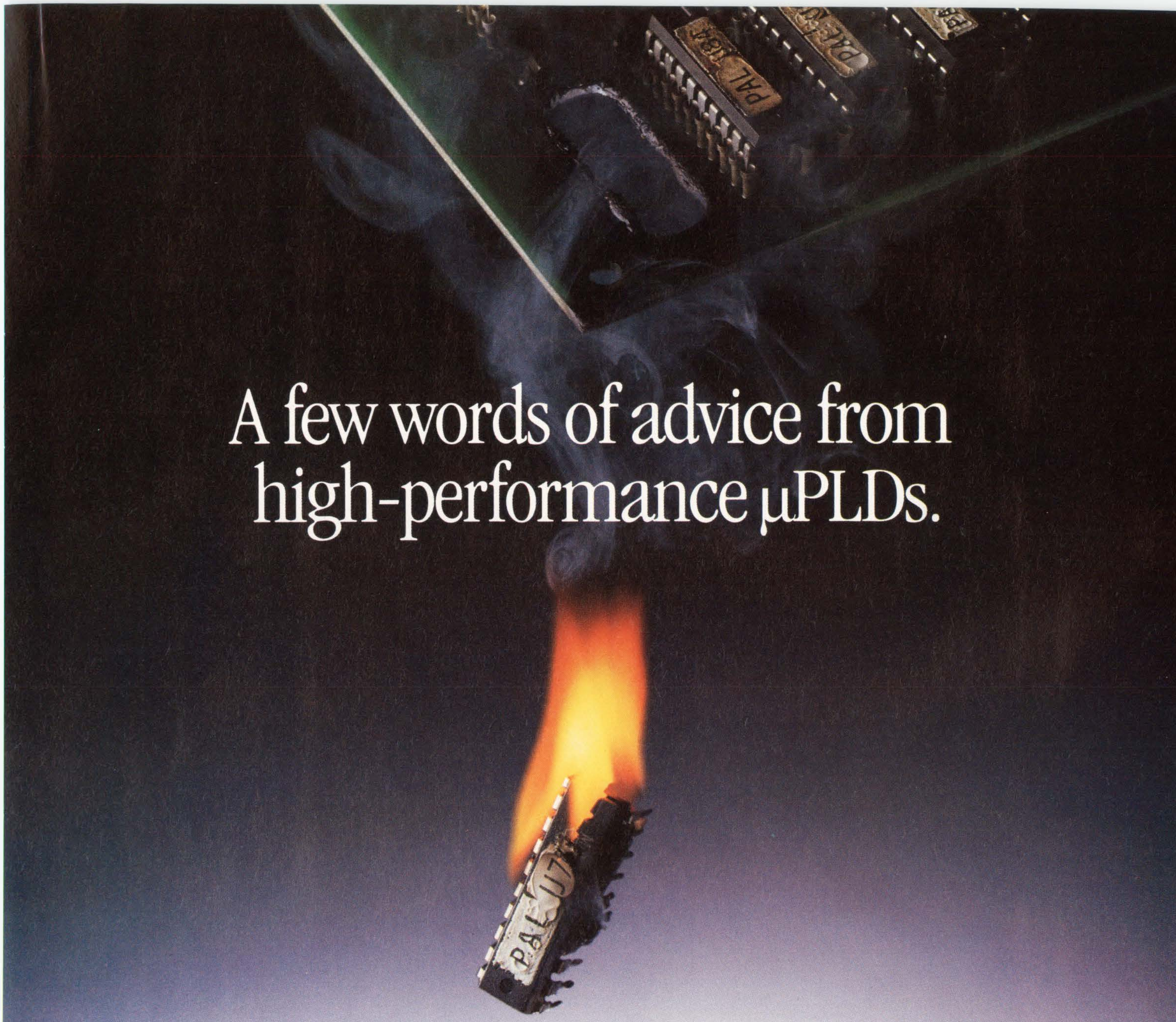

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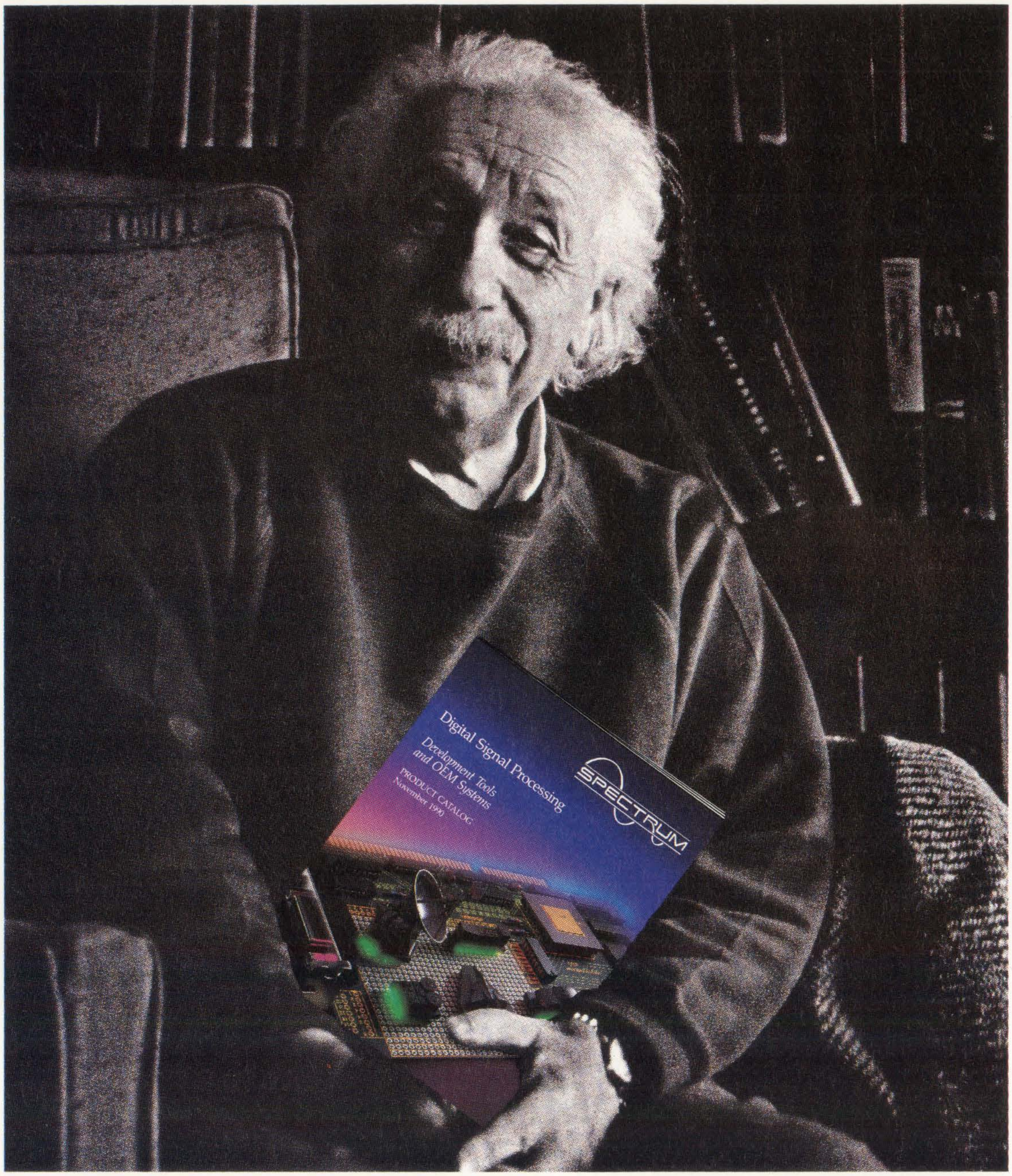

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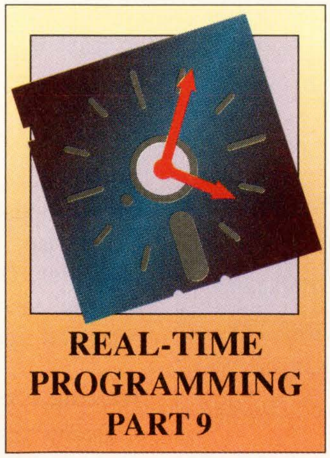

Semaphores and controlled shared variables

The discussion of task coordination methods continues in Part 9 of this series with an overview of how semaphores and controlled shared variables coordinate tasks in real-time applications. Part 10 will discuss task coordination and communication via signals.

David L Ripps, *Industrial Programming Inc*

In most applications, tasks must share sets of data, such as a table that is read by one task and updated by another. A second example of shared data are the global variables within a nonre-entrant procedure that could be called by different tasks.

A segment of code in which a task is accessing some shared resource is often called a "critical region" with respect to that resource. Not every reference to shared data forms a critical region, however. Accessing a fixed data table would not qualify. A region is critical only if there could be harmful interactions because of the sharing of the resource. For data, this means that the variables are both shared and alterable. More general resources, such as a printer or console, engender critical regions only when it is undesirable to intermix the output from different tasks on the same page or screen.

Shared resources must be protected against potentially harmful interactions by permitting only one task at a time to enter a critical region. In the first example, while the data is being read, the update task must be blocked; while the data is being updated, the reader task must be blocked.

In real-time applications, a critical region can be so small that its existence is easily overlooked. Suppose that a certain memory-mapped byte (call it *lamps*) is used to control eight lights: a 1 in bit **i** turns the **ith** light on; a 0 turns it off. Initially all lights are off. At some point task **TskA** turns light 7 on by OR-ing with 0x80. A higher-priority task, **TskB**, turns light 0 on by OR-ing with 0x01. Most of the time this works. But occasionally, because of an ill-timed task switch, the two tasks are in the critical region for *lamps* at the same time:

TskA	lamps	TskB
lamps=>reg	0x00	blocked
OR reg with 0x80	0x00	blocked
preempted by TskB	0x00	lamps=>reg
preempted by TskB	0x00	OR reg with 0x01
preempted by TskB	0x00	reg=>lamps
preempted by TskB	0x01	...
reg=>lamps	0x01	blocked
...	0x80	blocked

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Shared resources must be protected against harm by permitting only one task at a time to enter a critical region of code.

In this case, the final value is 0×80 instead of 0×81. Problems such as these are insidious since they arise from subtle timing relationships.

Critical regions must be protected by guaranteeing one-task-at-a-time access. The MTOS-UX operating system provides two different facilities to achieve such mutual exclusion: the semaphore (SF) and the controlled shared variable (CSV), the SF being the simpler of the two.

A semaphore is an operating system object that is created by task request. In most applications, a separate SF is created for each critical region. (You could utilize a single SF to protect several regions, but this usually leads to excessive contention delays.) Prior to entering a critical region, every task must invoke *waisem* to wait for the corresponding SF to be free. If another task already has taken that SF, the new task waits. Queuing is based on the current priority of the waiting tasks. Upon exiting a critical region, a task must relinquish control to the next waiting task:

```
task A: request SF, enter critical region, ..., release SF
                                                  |
      ----- time ----->                           |
                                                  |
task B:  request SF,   <blocked for SF>         enter critical
region, ..., release SF
```

A simple way to protect critical procedures is to make the first statement a wait-for-SF and the last statement before returning a release-SF. This method places all control aspects completely within the procedure. As a result, a caller does not have to know that the procedure is critical.

Creating a semaphore

A typical call to create a semaphore is

```
#define SF34 0x53463334

long int s34id;                         /*sample semaphore*/

s34id=crsem (SF34);
```

The argument is the external name associated with the semaphore. If a semaphore with the given key already exists, the function just returns the identifier. Otherwise, the OS creates the SF and returns the identifier. Only in the unlikely case of not having any internal resources remaining does *crsem* fail. The value returned upon failure is **QUEFUL**.

Waiting for a semaphore

Every task that wishes to enter a critical region protected by semaphore **SF34** must first issue a wait-for-semaphore-to-be-free request. In most cases, the call would specify wait-forever (**WAIFIN**) **coordination.**

```
long int result;                        /*result of request*/

waisem (s34id,&result,WAIFIN);
```

The first argument must be the identifier of an existing SF, as provided by *crsem*. Otherwise, the function returns a failure value of **BADPRM**. Failure values are also stored within the results buffer addressed by the second argument. As usual, a maximum wait time can be added to the coordination mode. Thus,

```
waisem (s34id,&result,WAIFIN+10+SEC);
```

waits up to 10 sec for the SF, while

```
waisem (s34id,&result,CLEF2+1+MIN);
```

waits no more than 1 minute for that SF and sets local event flag 2 as a completion indicator. The variable *result* receives the final status when the request is completed: **NOERR**, for success; **BADPRM, TIMOUT,** or **QUEFUL** for failure.

Each SF either is free or is "owned" by a task that issued a *waisem* without a corresponding release. Ownership is not permanent; once the release is given, the SF becomes free again to be owned by another task.

With some operating systems, the SF has just two states: free and in use. (In use means owned by some task, but the identity of the owner is not necessarily retained.) These are called binary semaphores. With a binary SF, any task, including the current SF owner, must wait if it issues a wait-for-semaphore request and the target SF is already in use.

MTOS-UX provides counting, not binary, semaphores. The difference between the two is that a task does not wait if it issues *waisem* targeted to a semaphore that it currently owns. The SF has an internal use-count that is incremented by 1 each time the owner issues a wait request and is decremented by 1 each time the owner issues a release. Note that the use-count is 0 when the SF is first created and when the SF is free.

There is value in providing counting semaphores, as opposed to just binary ones. In a complex application, it may be necessary for a task to make nested entries into critical regions for the same variables, say, in the main body of the code, and in some utility procedures. Each region separately needs the protection of the SF. With only a binary SF, it would be necessary for the task to know if it already has reserved the SF, and when it is safe to release it. With a counting SF, each critical region is bracketed by *waisem* and *rlsem* (release semaphore). Upon exiting from the last of these nested brackets, the SF count returns to 0, and the SF is automatically freed.

There is an essential difference between event flags and semaphores, even though both are used to achieve coordination between concurrent tasks. If several tasks are waiting for the same EF and it is set, then all those tasks continue simultaneously. If several tasks are waiting for the same SF and it is released, only one task (the one with the highest priority) continues; the others continue to wait.

The semaphore provided by MTOS-UX is similar to, but not exactly the same as, the semaphore proposed by Dijkstra (**Refs 1 and 2**). MTOS's *waisem* is close to Dijkstra's **P** or **wait**; MTOS's *rlssem* is close to Dijkstra's **V** or **signal**. The difference is that when a Dijkstra semaphore is created, a non-negative number (**s**) is assigned to the SF. Thereafter, s can increase or decrease (down to 0) via **P** and **V**. The action of **P** is

```
if (s > 0) then --s else block task on SF
```

The action of **V** is

```
if (any tasks are blocked on SF) then release 1 task else ++s
```

A Dijkstra SF need maintain only the use-count, **s**, and the list of tasks waiting for the SF; it need not record the current owner of the SF. Furthermore, the release **V** may precede the wait **P**, and the task that issues the release need not be the one that performed the wait. A Dijkstra semaphore permits s tasks to proceed into a critical region. These could be **s** different tasks, the same task **s** times, or any other combination that sums to s. MTOS-UX permits the same task to proceed any number of times, but blocks all other tasks.

Possession of a semaphore does not guarantee that a task cannot be interrupted by a task of equal or greater priority. Pre-emption is always permitted. However, having the SF does guarantee that a pre-empting task will not be allowed past a *waisem* for that SF.

Deadly embrace

There is no limit to the number of semaphores that a task can reserve and the number of *waisem* requests it can have outstanding. Thus, a task may wait for one SF while it has reserved another. But beware the deadly embrace. To illustrate this phenomenon, suppose that task **D** has reserved SF **SFN1** and seeks SF **SFN2**. Task **E** already has SF **SFN2** and seeks SF **SFN1**. Deadlock.

In principle, the solution is easy: Have all tasks that seek multiple semaphores always seek them in the same order. In complex cases, this may not be easy to arrange.

Deadly embraces can also arise from other combinations of limited resources. For example, a task that has a semaphore and is seeking a memory pool allocation can deadlock with a task that has a large portion of the memory and is waiting for that SF.

To reduce the effects of a deadly embrace, avoid unlimited waits. Use **WAIFIN** + 10 MS, rather than just **WAIFIN**. And when you fail to obtain one of the needed resources, relinquish other limited resources and then try again. Furthermore, you should use different time limits in different tasks to make it unlikely that the same deadly embrace will reappear on each cycle of retry.

Releasing a semaphore

The request

```
result = rlssem (s34id);
```

decreases the use-count of the given semaphore and releases it to the next user if the count becomes 0. If the argument is not a semaphore currently held by the calling task, the function returns a failure value of **BADPRM**. Two values represent success: **NOERR** means that the SF was released and is now free; **NOTFRE** means that the SF is still held since the count has not been reduced to 0.

For best overall performance, a semaphore should be released immediately upon exit from the critical region.

Deleting a semaphore

In a dedicated real-time application it is likely that control objects, such as semaphores, would be created

Beware the "deadly embrace." Two tasks are blocked, because each needs a semaphore that the other has reserved for itself.

by an initialization task and then remain "forever." In contrast, the semaphores created by transient (temporary) tasks are not likely to be permanent. Thus, the OS provides a mechanism to delete a semaphore once it is no longer needed.

```
result = dlsem (s34id);
```

If the argument is not the identifier of a semaphore, the function returns a failure value of **BADPRM**. The function returns **NOERR** for success.

Usually, the SF is not in use when it is deleted. If it is in use, the delete request is discarded, and the function returns the warning value **NOTFRE**. Each task that accesses a nonpermanent SF should delete the SF before it exits.

Controlled shared variables

As already noted, it is common in real-time applications for a set of tasks to share a group of alterable variables. The semaphore facility permits the OS to grant each task exclusive access to the variables to prevent possibly harmful interference.

In some cases, however, a task does not simply want exclusive access to the variables; it wants that exclusivity only after a certain relation exists among variables in the group. Until then the task must be blocked. For example, suppose the group contains 32 binary variables akin to event flags. The task might have to be blocked until a given set of these variables are all equal to 1. Thus, the task might have to leave the critical region so that other tasks can access and change the variables, but then re-enter the critical region when the desired relation is true (**Ref** 3). MTOS-UX includes five service calls that make it efficient to handle this type of coordination.

crcsv create a group of controlled shared variables

usecsv wait for exclusive access to a group of controlled shared variables

waicsv wait for given function of controlled shared variables to be TRUE

rlscsv release exclusive access to a group of controlled shared variables

dlcsv delete a group of controlled shared variables

Creating a group of CSVs

The first step toward establishing a group of controlled shared variables is defining their structure. To illustrate the creation and use of CSVs, assume that you are interested in maintaining multiple windows on a CRT screen. The supporting data is

```
#define NW 4                    /*maximum number of windows*/

struct mw
  {
   long   int wid[NW];   /*width*/
   long   int len[NW];   /*length*/
   short  int avl[NW];   /*0=available*/
   ...                   /*position and other data*/
  };
```

You can create a set of controlled shared variables having this structure via the sequence

```
#define WNDO          0x574E444F
#define MWSIZ         sizeof (struct mw)

struct mw *wndgid;    /*identifier of group=addr of first
                        variable*/

wndgid=(struct mw*) crcsv (WNDO, (long) MWSIZ);
```

The first argument (**WNDO**) is the usual key associated with the group of variables. The second argument (**MWSIZ**) is the overall size of the variables, in bytes. If a group with the given key already exists, the group identifier is returned as the value of the function when the current and original lengths match. When they do not match, **BADPRM** is returned. For a new key, the OS attempts to create the group. If successful, again the identifier is returned. If there is not enough internal memory currently available for creation, the function returns the error code **QUEFUL**.

The group identifier is also the address of the first variable. The group is created with all variables initialized to 0.

Waiting for exclusive access to CSVs

For tasks to share the variables successfully, all users must wait until the OS grants exclusive access. (This is the implication of the term controlled.) If the task needs exclusive access with no preconditions having to be met, it would invoke the unconditional form of the wait request. For example,

```
usecsv (wndgid,NOEND);
```

provides a wait without limit, while

```
usecsv (wndgid,100+MS);
```

sets a maximum of 100 msec to the wait. If the group does not exist, *usecsv* returns **BADPRM**. If the requesting task already has exclusive access to the group, the return value is **DUPTSK** (duplicate task request). If the group is available or becomes so during the specified interval, the return value is **NOERR**. Finally, if the group remains unavailable during the given interval, the request is canceled and the return value is **TIMOUT**.

Once exclusive access is granted, the task may freely and safely read and write the group variables. Recall that the group identifier is also the address of the first of the variables. Continuing the example just introduced,

```
if (usecsv (wndgid,100+MS)==NOERR)
  {
    printf ("Size of window #1 is %lx by %lx\n\r",
      wndgid->wid[0], wndgid->len[0]);
    .
    .
    .
  }
```

Releasing CSVs

When a task no longer needs its exclusive access to a group of CSVs, it must issue a release request.

```
rlscsv (wndgid);
```

The argument identifies the group. Once the group is released, the task must not alter any of the group variables, even though the OS does not have the ability to enforce this rule.

Calls to *waicsv* and *rlscsv* mark the entry into and exit from the critical region for the group, in a way analogous to *waisem* and *rlssem*.

Waiting for the function of CSVs to be true

If only unconditional waits for access are needed, it is easier and faster to implement the variables as a task-level, public structure and protect the structure with an ordinary semaphore. The strength of CSVs arises when a task wishes to enter a critical region only when a certain condition is met among the variables. Alternatively, a task already within a critical region may wish to leave it until a condition is met.

The C function to wait for a certain relation among CSVs to be true is formally defined as

```
int waicsv (gid,bfun,interval)
  long int gid,interval;
  int   (*bfun) ();
```

The first argument identifies the variables group, the second argument supplies the address of the evaluation function, and the third argument indicates the maximum time to wait before returning from *waicsv*. If the interval is **NOEND**, the service can never time out. Possible return values are **NOERR** (for success), **TIMOUT** (if *bfun* is never TRUE during the specified interval), **QUEFUL** (if the timer cannot be allocated), and **BADPRM** (if the group does not exist).

When it is called, *bfun* is presented with a pointer to the group variables as its only argument. The function must return an integer value of TRUE (nonzero) if the task is to be blocked or FALSE (zero) if the task is to be continued. No task-level service calls are permitted within *bfun*.

The wait service call may be made either as a way into the critical region or as a way to exit the region until *bfun* is TRUE. In either case, *waicsv* does not return successfully until both *bfun* is TRUE and the task has been given exclusive access to the variables.

The *bfun* evaluation function is called immediately after *waicsv* is invoked if the requesting task already has exclusive access to the variables or the variables are free. If the task is to be blocked, *bfun* will be called again each time a task leaves the critical region via *rlscsv* or *waicsv*. Whenever more than one task could be unblocked because its evaluation function is TRUE, only the highest priority task will be continued at that point. The others will have to wait until the variables are available again.

To complete the example already started,

```
static int idx;          /*index of available window*/
static int mwid;         /*min width of available window*/
static int mlen;         /*min length of available window*/

int testw ();            /*test value function*/

waicsv (wndgid,testw, 5+MIN);    /*wait for testw to be TRUE*/
 .
 .
 .
testw (data)             /*sample function*/
 struct mw *data;
  {
   register int i;       /*search index*/

   for (i=3;i>=0;--i)
    {
     if ((data->avl[i]!=0)&&
       (data->wid[i]>=mwid)&&(data->len[i]>=mlen))
      {
       data->avl[i]=1;   /*take window*/
       idx=i;            /*note which one*/
       return (1);       /*end wait*/
      }
     return (0);         /*keep waiting*/
    }
  }
```

Whether or not a task had exclusive access to the group originally, it loses this privilege while it is blocked and regains it when the task becomes unblocked because the evaluation function was satisfied. However, it does not have access upon a time out or other unsuccessful return. Thus, the application must have the following overall structure

```
if (waicsv (wndgid,testw,5+MIN)==NOERR)
  {
   .
   .
   .
   rlscsv (wndgid);
  }
```

Deleting a group of CSVs

When a group of controlled shared variables is no longer needed by any task, it may be deleted by invoking

```
result = dlcsv (wndgid);
```

The function returns **NOERR** for success and **BADPRM** for failure.

The same problem arises in deleting a group of CSVs as in deleting a group of public event flags: how to know when the last task is finished with the group so that it can be removed. The same solution is used. Thus, *dlcsv* does not immediately delete the group if there are any tasks waiting because of *waicsv*. If there are, the group is internally marked "deletion requested." Actual removal does not occur until there are no more tasks waiting. In the interim, all CSV functions may be applied in their normal manner.

Priority inversion

Once the OS grants task **LP** a semaphore, a group of controlled shared variables, or any other exclusive-access object, the OS is not free to take the object back and give it to another task. (That would defeat the whole purpose of providing exclusive-access objects.) As a result, if a higher-priority task (**HP**) seeks the same object, it must wait until **LP** releases the object. But, because **LP** is a low-priority task, it may take a very long time for **LP** to execute. Thus, a low-priority task can block a higher-priority one for an indefinite period. This is known as priority inversion.

Equivalent forms of priority inversion can occur when a task

- is blocked waiting to restart another task that is executing at a low priority,
- is blocked waiting to communicate with a partner that is executing at a low priority,
- or needs memory or another shared resource that is held by a low-priority task,

among other cases. This is not the same as a deadly embrace since in principle the high-priority task does get to run eventually.

In very simple cases, it is tempting to have the OS temporarily raise the priority of task **LP** to that of **HP** to break the inversion. However, because of the many and subtle ways in which priority inversions can occur, and the complexity of nested blockages, there is no easy way to avoid inversions completely. These problems are actively being investigated at the Software Engineering Institute of Carnegie-Mellon University (**Ref 4**) and other places.

To sum up, a critical region is a segment of code in which alterable variables or some other resource is being shared by two or more tasks. The resource must be protected against potentially harmful interactions by enforcing one-task-at-a-time entry into any critical region for that resource. Semaphores and controlled shared variables can provide the required mutual exclusion.

A semaphore is sufficient to protect a set of shared alterable variables when all entries into their critical regions are unconditional, that is, do not depend upon the current values stored in the variables. A semaphore is created for the set of variables. Before every task enters a critical region, it requests temporary ownership of that SF by issuing *waisem*. The OS allows only one task to proceed; it blocks all others. When a task leaves the critical region, it releases the SF by issuing *rlssem*. If there are no tasks waiting for the SF, the SF is set free. Otherwise, only the highest priority task is unblocked.

Controlled shared variables are a further refinement of the idea of semaphore protection. The request to enter a critical region can contain a condition function. Now the task may be blocked until both exclusive access can be granted and the function (evaluated with respect to the variables) returns TRUE. The same service also permits a task that is already in a critical region to exit until the same two criteria are met.

Part 10 of this series will discuss task coordination and communication via signals. EDN

References

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2. Deitel, HM, *An Introduction to Operating Systems*, Section 4.11, Reading, MA: Addison-Wesley, 1984.
3. Brinch Hansen, P, *Operating System Principles*, Englewood Cliffs, NJ: Prentice-Hall, 1973.
4. Locke, D and L Sha, et al, "Priority Inversion and Its Control: An Experimental Investigation," Second International Workshop on Real-Time Ada Issues, June 1988. Reprinted in Sha, L, ed, "An Overview of Real-Time Scheduling Algorithms," Software Engineering Institute, Dept of Computer Science, Carnegie-Mellon University, Pittsburgh, PA, June 8, 1988.

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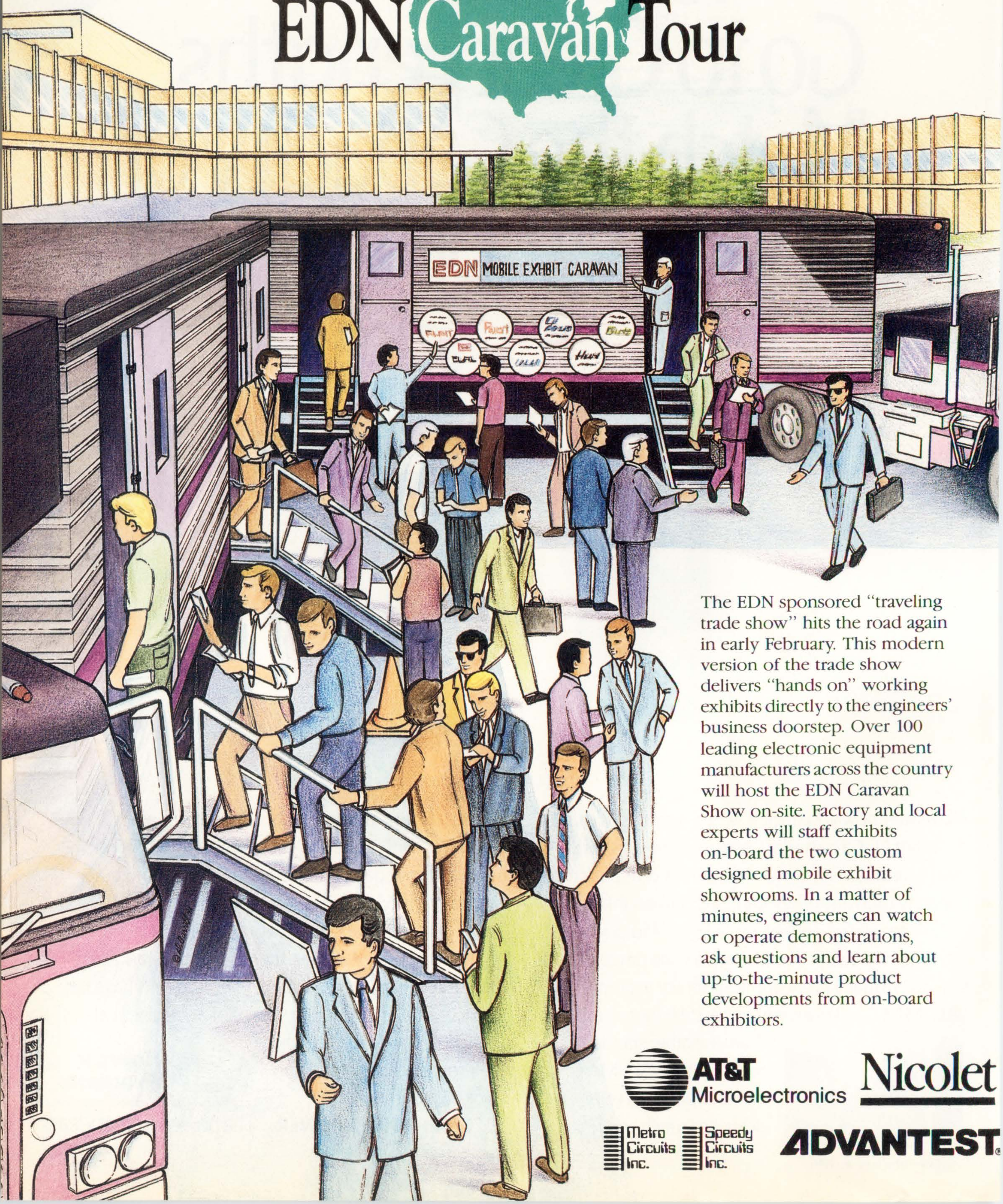

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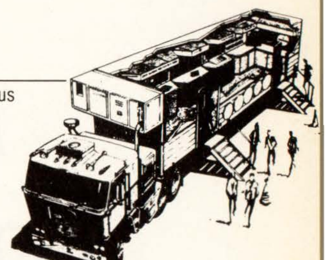

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3/5 Tuesday	11:30-1:00 AM-PM	ELDEC CORPORATION, Sensing System 22000 Bothel Way S.E., Bothel, WA
3/5 Tuesday	2:00-4:00 PM	SUNDSTRAND DATA CONTROL 15001 N.E. 36th Street, Redmond, WA
3/6 Wednesday	9:00-11:30 AM	BOEING AEROSPACE-Plant 2 7755 East Marginal Way So., Seattle, WA
3/6 Wednesday	1:00-3:30 PM	BOEING AEROSPACE-Developmental Center 9725 East Marginal Way So., Seattle, WA
3/7 Thursday	9:00-12:00 AM	BOEING COMMERCIAL AIRPLANE-Renton Plant Logan Avenue No., Renton, WA
3/7 Thursday	1:30-4:00 AM	BOEING ELECTRONICSS & SPACE CENTER 820 S.W. 41st Street, Renton, WA
3/8 Friday	9:00-11:30 AM	NEC AMERICA, INC. 3100 N.E. Shute Road, Hillsboro, OR
3/8 Friday	1:30-3:30 PN	SEQUENT COMPUTER INC. 15450 S.W. Koll Parkway, Beaverton, OR
3/11 Monday	8:30-11:00 AM	LAWRENCE LIVERMORE NATL' LABORATORIES 7000 East Avenue, Livermore, CA
3/11 Monday	1:30-4:00 PM	ROLM SYSTEMS INC. 4900 Old Ironsides Drive, Santa Clara, CA
3/12 Tuesday	9:00-11:00 AM	TANDEM COMPUTERS 19333 Vallco Parkway, Cupertino, CA
3/12 Tuesday	12:30-3:30 PM	APPLE COMPUTER, INC. 20650 Valley Green Drive, Cupertino, CA
3/13 Wednesday	8:00-10:30 AM	LORAL CORP., Western Development Labs 3200 Zanker Road, San Jose, CA
3/13 Wednesday	11:30-1:00 AM-PM	MAXTOR CORPORATION 211 River Oaks Parkway, San Jose, CA
3/13 Wednesday	2:00-4:00 PM	CONNERS PERIPHERALS 3061 Zanker Road, San Jose, CA
3/14 Thursday	8:30-11:00 AM	LORAL ROLM MIL-SPEC COMPUTER 3151 Zanker Road, San Jose, CA
3/14 Thursday	12:30-2:00 PM	UNISYS CORPORATION 2700 N. First Street, San Jose, CA
3/14 Thursday	2:45-4:30 PM	WATKINS-JOHNSON COMPANY 2525 N. First Street, San Jose, CA
3/15 Friday	9:00-11:30 AM	IBM CORPORATION 5600 Cottle Road, San Jose, CA
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CIRCLE NO. 60

State-machine design curbs illegal states and transitions

You can learn theoretical state-machine design from myriad sources, but most neglect to tell you how to design state machines that work reliably. Such neglect is unfortunate—and unnecessary—because reliability is fairly easy to come by.

Ricardo Rabinovich, *Librascope Corp*

Different design enhancements can decrease the likelihood that your state machine will reach an illegal state or illegally reach a legal state. Synchronizing or deglitching the inputs and filtering or decoupling the supply and ground rails are among the less obtrusive techniques you can use.

Unless the number of valid states in your state machine is a power of 2, the machine will have illegal states. An illegal state is a state that the machine cannot reach during its normal operation. The machine reaches an illegal state as a result of electrical noise, a power glitch, transient illegal input combinations, or other unfavorable conditions.

Another functional concern in designing state machines is the problem of the machine's reaching a legal state via an illegal transition. Most textbooks recommend that you explicitly specify a legal transition from illegal states to an initial idle state to recover from illegal state assignments. However, they generally do not address illegal transitions to legal states.

Unfortunately, in practical situations, defining an idle state is often difficult. Many state-machine designs have more than one idle state. Even when only a single idle state exists, changing to that state could hang-up the machine or system by leaving the system waiting for some output that doesn't occur.

Synchronizing and deglitching inputs require a simple circuit. **Fig 1** shows a circuit that synchronizes an input with the system clock regardless of the input signal's normal polarity. This circuit consists of three D-type flip-flops, one of which has a multiplexed input and an exclusive-OR gate. The same clock-edge clocks all three flip-flops. The exclusive-OR gate validates the input-level change before that input change is transmitted to the rest of the state machine. If both inputs of the exclusive-OR gate are the same, the mul-

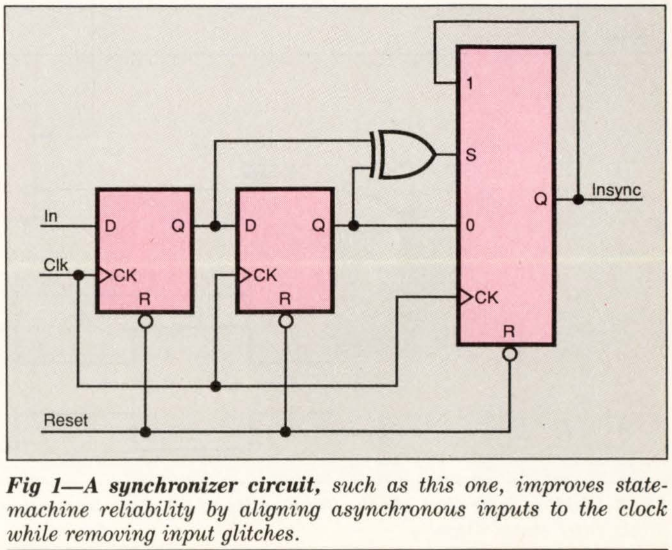


Fig 1—A synchronizer circuit, *such as this one, improves state-machine reliability by aligning asynchronous inputs to the clock while removing input glitches.*

State machines aren't supposed to reach illegal states, but because they occasionally do, you should design conservatively.

tiplexer selects the state machine's input signal. If the input levels are different, the multiplexer refreshes the existing signal. Therefore, the input signal must remain stable for at least one clock cycle before the state machine acknowledges it. In addition to synchronizing and deglitching inputs, this pipeline arrangement prevents a metastable condition from propagating through the state machine.

The second step toward freedom from illegal states is to filter and decouple the power and ground rails. Usually all you have to do is connect a 0.1-μF capacitor between the two. Be sure to connect the decoupling capacitor as close as possible to each component. Decoupling is especially important when using high-speed logic, such as FAST or FCT parts.

Even with these precautions, building a highly reliable state machine demands that your design include logic that specifically prevents unwanted states and illegal transitions to valid states. An effective technique for detecting and suppressing illegal transitions is to sample the value of the next state in the middle of the system clock cycle and compare it with the value of the present state. If the transition is legal, the next state becomes the present state at the beginning of the next clock cycle. If the transition is not legal, the clock latches the present state again, ignoring the next state.

Is the potential transition legal?

The block diagram in **Fig 2** demonstrates this technique. (For clarity, logic blocks have been labeled in all upper case, and signals have been labeled in lower case with an initial capital.) This circuit uses the SYNC block from **Fig 1**. Insync is the output signal of the SYNC block and is an input to the NSD (next-state decoder) block. The NSD is a combinatorial circuit that generates the next-state signal, Uns. Uns is strictly a function of Insync and the present state, Prst, of the state machine, and does not indicate the legality of the transition. The falling edge of the system clock latches Uns into the NSR (next-state register) in the middle of the clock cycle. The output of NSR and the Prst signal are inputs into the NSVAL (next-state validation) block of combinatorial logic, which evaluates the legality of the transition between states. The output of NSVAL controls a multiplexer. If the transition is illegal, then the NSVAL output is low, and the multiplexer feeds the state machine's present state back to

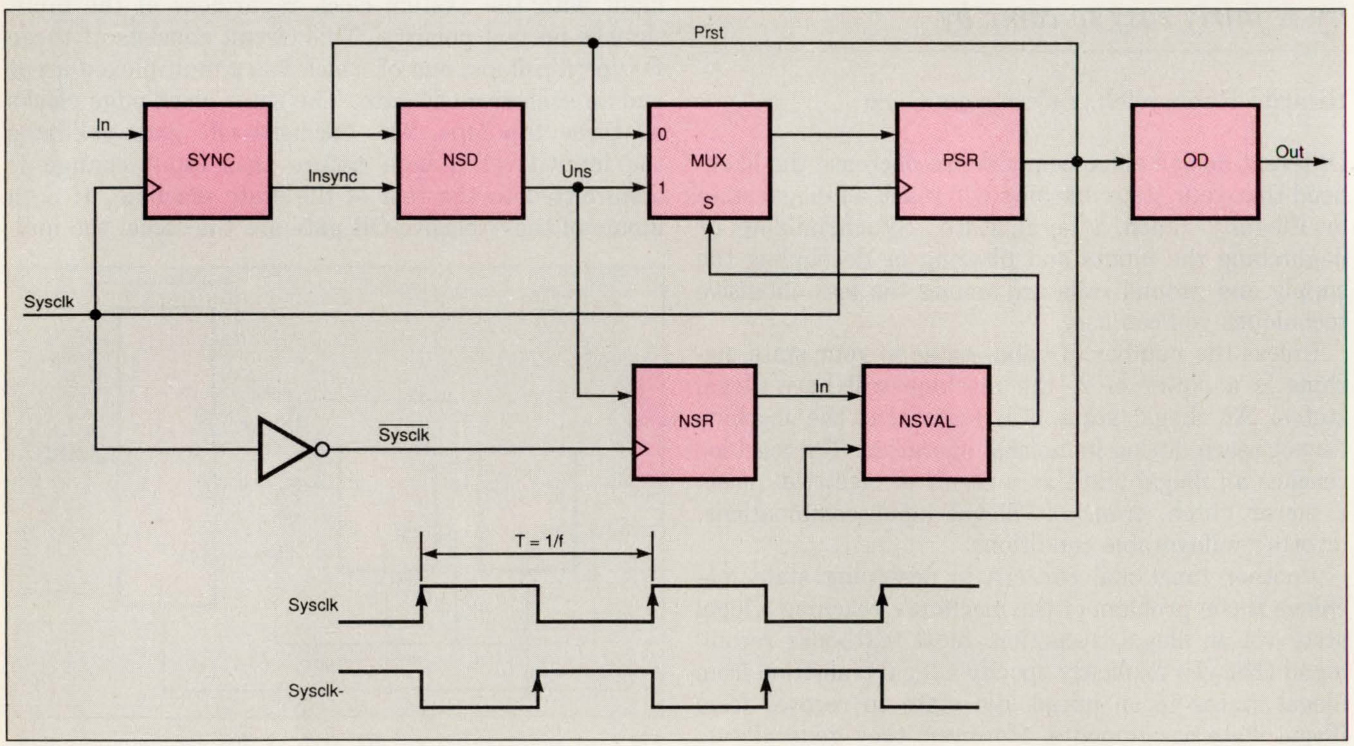


***Fig 2—Adding logic that checks the legality of all state transitions** before the machine executes them reduces the risk that your machine might enter states illegally.*

the PSR (present-state register). If the transition is legal, the NSVAL output goes high and the rising clock latches Uns into the PSR.

The NSVAL block checks whether a transition is legal on the rising edge of $\overline{\text{Sysclk}}$. The OD (output decoder) block drives the output signal, Out, as a function of the present state only, regardless of changes that occur at the input of the state machine. By definition, then, the state machine in **Fig 2** is a Moore machine, and its outputs are solely a function of the present state. A state machine whose outputs are a function of both the inputs and the machine's present state is a Mealy machine. You can use similar logic to design reliable Mealy machines. However, please note that Mealy machines are more prone to output glitches because the inputs and the system clock are asynchronous.

Designing a simple state machine will help clarify these reliability-ensuring techniques. Assume you must create a firing mechanism for a rocket launcher. To minimize the risk of false launches, the operation of the firing system requires the sequential assertion of two toggle switches. The wrong toggle-switch sequence invalidates the entry. The state diagram in **Fig 3** describes the machine.

Toggle switches X_1 and X_2 are the inputs to the system. The logic value of each switch is 0 when idle and 1 when active. Output variable Y controls the launch of the missile; the missile launches when Y is 1.

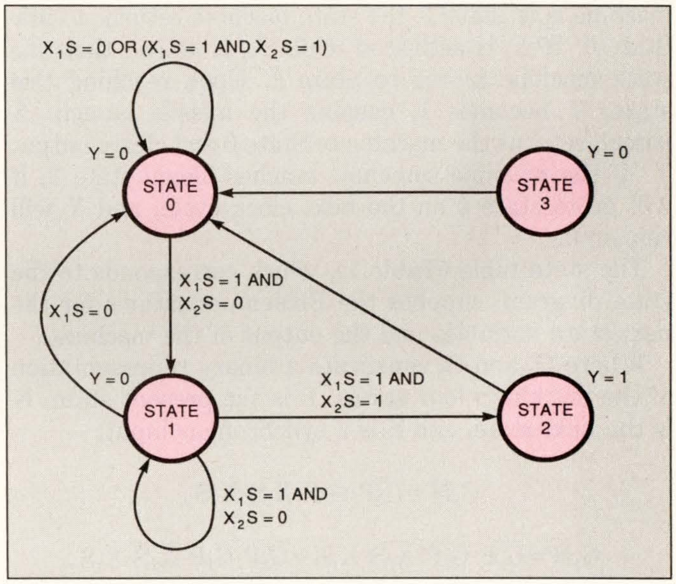


Fig 3—This state machine, controlled by inputs X_1S and X_2S, *launches a rocket from State 3.*

Calculating how fast the machine will run

After you have designed your state machine, you often want to know its maximum operating frequency: $f_{MAX}=1/T_{MIN}$. To simplify the calculations, you can assume the inverter delay is negligible. The worst-case delay among four circuit paths limits the maximum operational frequency. First, the delay through the SYNC circuit in **Fig 1** is

$$T_{MIN1}>T_{MET}+T_{XORD}+T_{FFMXS}$$

and

$$T_{MIN2}>T_{ckd}+T_{XORD}+T_{FFMXS},$$

where T_{MET} is the duration of metastability for a given MTBF, T_{XORD} is the exclusive-OR gate delay, T_{FFMXS} is the MUX and flip-flop data setup time, and T_{ckd} is the flip-flop clock-to-output delay.

Then, the half-cycle delay through the SYNC circuit and the next-state register in the state machine of **Fig 2** is

$$T_{MIN3/2}>T_{SYNCD}+T_{NSDD}+T_{NSRS},$$

where T_{SYNCD} is the clock-to-output delay of the SYNC block, T_{NSDD} is the NSD (Next State Decoder) block delay, and T_{NSRS} is the NSR (Next State Register) data set up time.

Lastly, the half-cycle delay from the NSR block through the present-state register in **Fig 2** is

$$T_{MIN4/2}>T_{NSRD}+T_{NSVALD}+T_{MUXD}+T_{PSRS},$$

where T_{NSRD} is the NSR (Next State Register) clock-to-output delay, T_{NSVALD} is the NSVAL (Next State Validation) block delay, T_{MUXD} is the MUX block delay, and T_{PSRS} is the PSR (Present State Register) data set up time.

The longest of the above four delays determines your state machine's operating frequency:

$$f_{MAX}=1/T_{MIN},$$

where $T_{MIN}=MAX(T_{MIN1}, T_{MIN2}, 2\cdot T_{MIN3/2}, 2\cdot T_{MIN4/2}$.

A state machine should test all transitions to determine whether they are legal before the machine executes them.

State 0 is the idle state. As long as X_1 is 0, the machine ignores the value of X_2 and Y remains 0. When only X_1 is activated, the state machine goes to state 1 while Y remains 0. If X_1 is released while the state machine is at state 1, the state machine returns to idle State 0. If X_2 is activated while X_1 is active, then the state machine moves to State 2. Upon reaching this state, Y becomes 1, causing the missile launch. A launch returns the machine to State 0 and clears output Y. If the machine somehow reaches illegal state 3, it will go to state 0 on the next clock cycle, and Y will remain 0.

The state table (**Table 1**), which corresponds to the state diagram, supplies the Boolean equations for the next-state variables and the output of the machine.

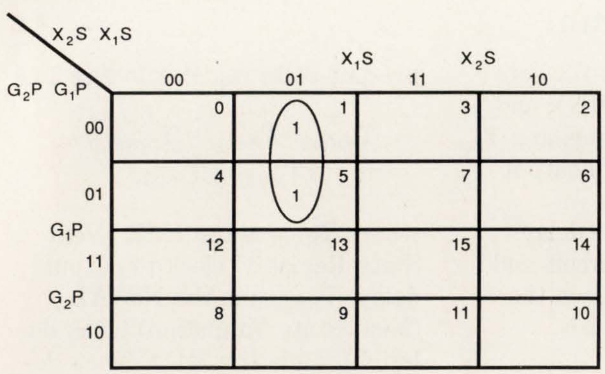
Where G_1 and G_2 constitute a binary representation of the machine's four states, P is the present state, N is the next state, and S is a synchronous input:

$$G_2N = \overline{G_2P} \cdot G_1P \cdot X_2S \cdot X_1S,$$

$$G_1N = \overline{G_2P} \cdot \overline{G_1P} \cdot \overline{X_2S} \cdot X_1S + \overline{G_2P} \cdot G_1P \cdot \overline{X_2S} \cdot X_1S,$$

$$\text{and } Y = G_2P \cdot \overline{G_1P}.$$

A Karnaugh map can help you simplify G_1N:



which yields

$$G_1N = \overline{G_2P} \cdot \overline{X_2S} \cdot X_1S.$$

The logic in the equations for G_1N and G_2N constitutes the NSD block. The equation for Y defines the logic for the OD block. The next-state validation circuit, NSVAL, is a combinatorial circuit that analyzes each next-state transition for all possible present states and determines whether the transition is legal. If the transition is legal, output variable M is 1. Conversely, M is 0 for all illegal transitions. The output of this circuit controls the multiplexer block.

Table 1—Missle launch when Y= 1

Present state		Inputs		Next state		Output
G_2P	G_1P	X_2S	X_1S	G_2N	G_1N	Y
0	0	X	0	0	0	0
0	0	1	1	0	0	0
0	0	0	1	0	1	0
0	1	X	0	0	0	0
0	1	0	1	0	1	0
0	1	1	1	1	0	0
1	0	X	X	0	0	1
1	1	X	X	0	0	0

Table 2—Multiplexer control logic

G_2P	G_1P	G_2N	G_1N	M
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

The diagram shows legal transitions

Inspecting **Fig 3** allows you to determine the legal transitions. These transitions are:

- From State 0, the state machine can go to State 0 or 1.
- From State 1, the state machine can go to States 0, 1, or 2.
- From State 2, the state machine will go to State 0.
- From State 3, the state machine will go to State 0.

The output variable, M, is a function of both the

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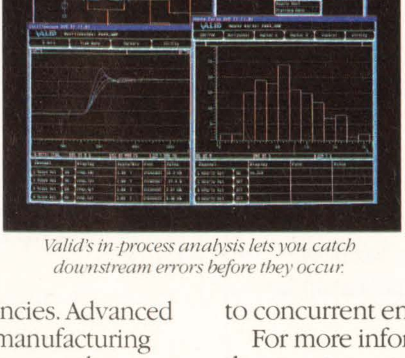

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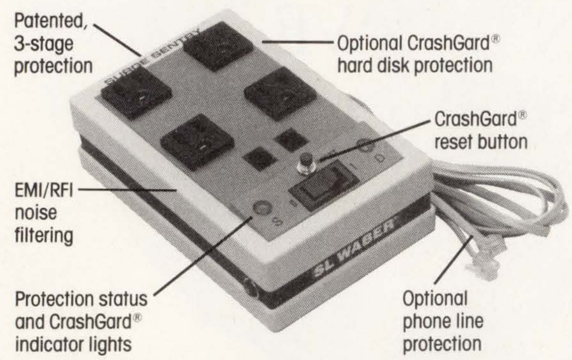

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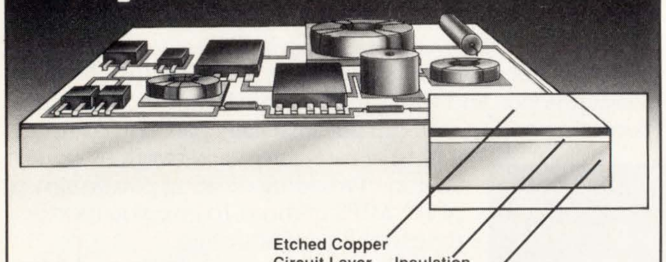

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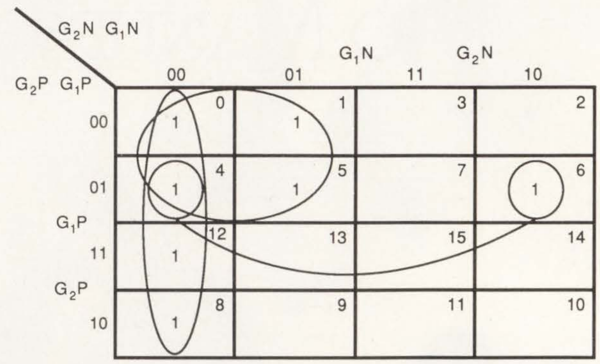
present- and the next-state inputs (**Table 2**). A Karnaugh map helps simplify the Boolean equation for M:



which yields

$$M=\overline{G_2N}\cdot\overline{G_1N}+\overline{G_2N}\cdot\overline{G_2P}+\overline{G_1N}\cdot\overline{G_2P}\cdot G_1P.$$

The equations for G_2N, G_1N, Y, and M provide the information you will need to build a simple state machine that is better protected against illegal states and illegal transitions.

Techniques such as synchronizing the inputs, preventing illegal transactions, and providing for the safe transition to an idle state from illegal states can increase the reliability of state machines. The requirements for your particular state machine will determine the most appropriate method to resolve illegal states or transitions. Design techniques that build forgiveness into your circuits are only part of your design arsenal. The best way to avoid state-machine hang-ups is to prevent noise from reaching the system and ensure clean input signals. EDN

Acknowledgment

The author would like to thank L Prater for his collaboration in the development of some of the concepts presented in this article.

Author's biography

Ricardo Rabinovich is a staff engineer with Librascope Corp (Glendale, CA). A graduate of an electronic-engineering program at Buenos Aires University, Ricardo is a computer design engineer. He has worked with 68020-based microcomputer designs and recently helped design an ASIC containing a VMEbus interface.

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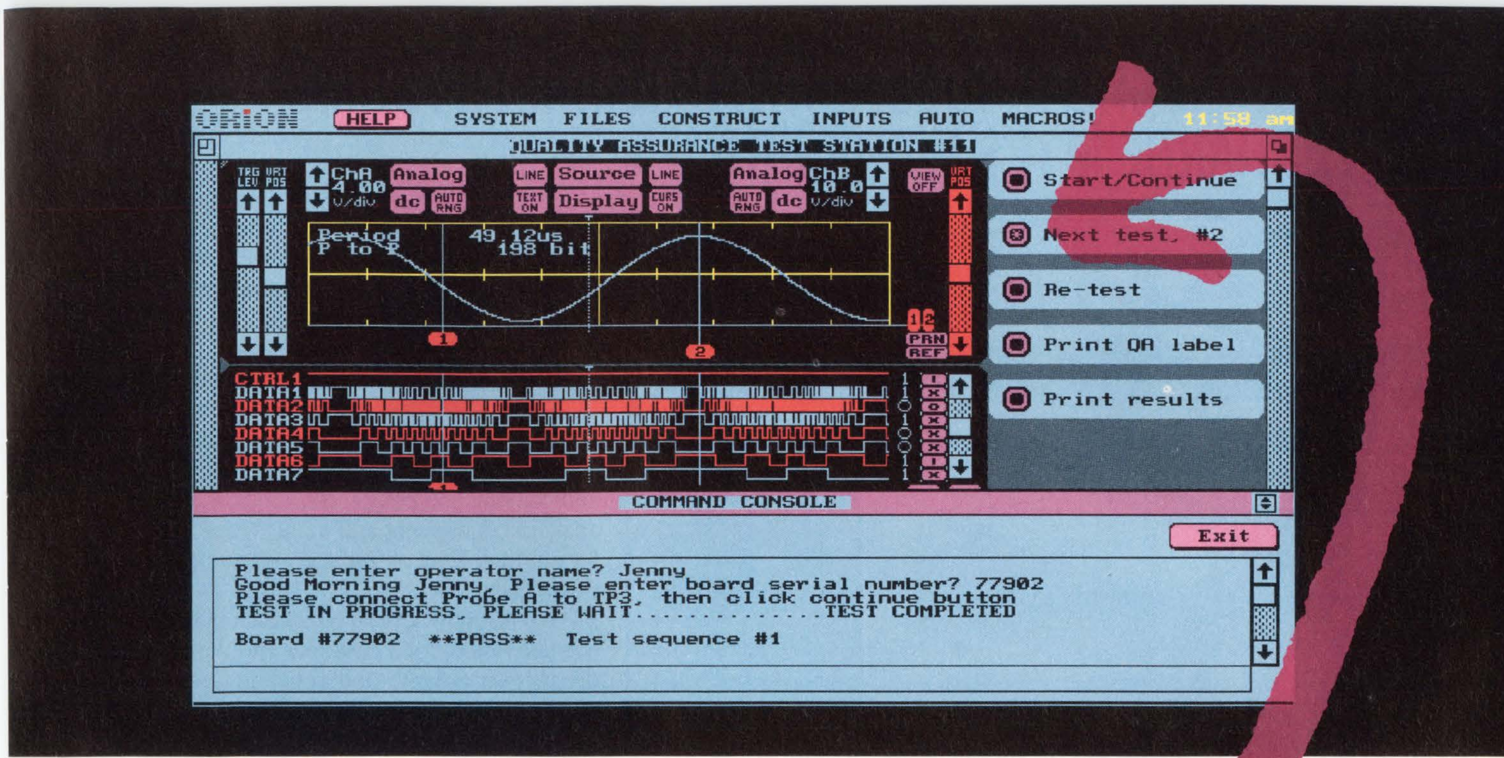

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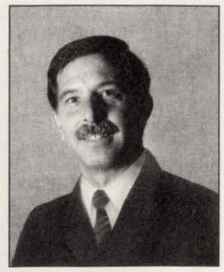

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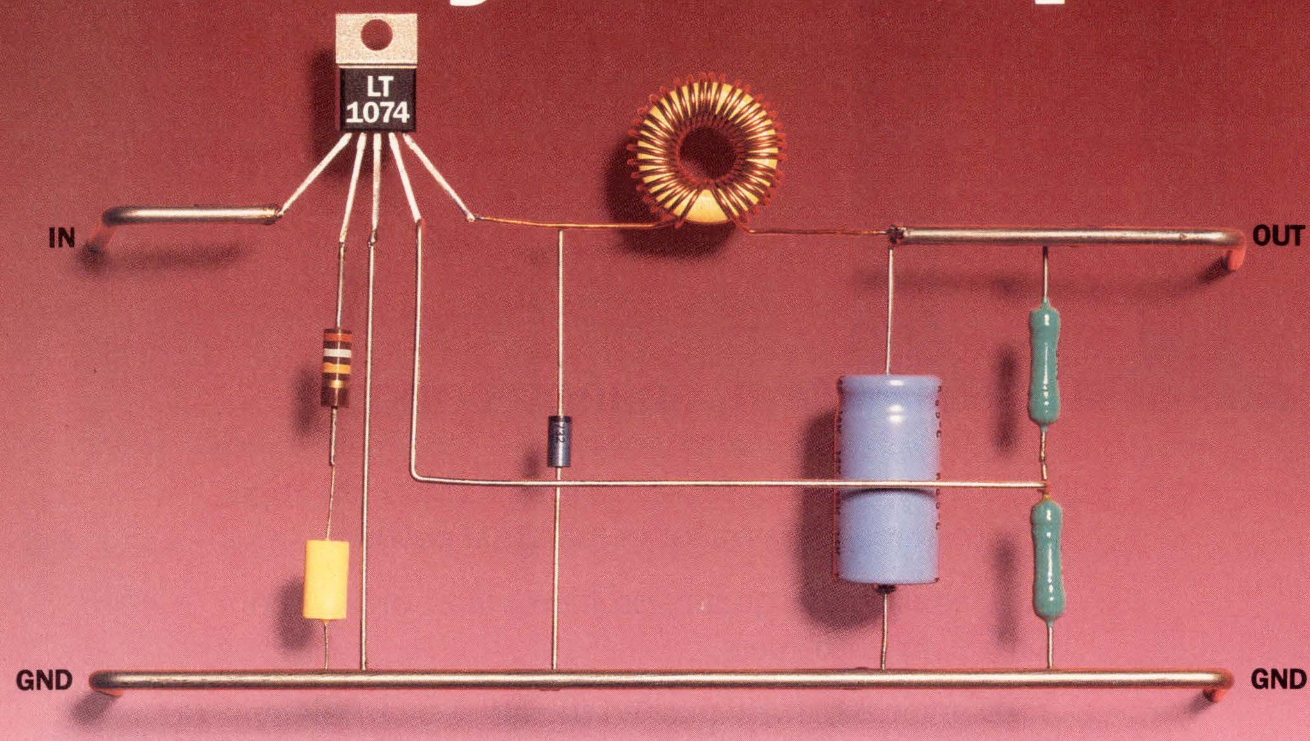
CIRCLE NO. 75

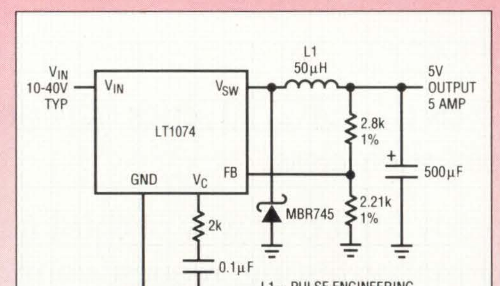
Pretty & Simple



5A positive or negative stepdown or positive to negative voltage conversion.

Talk about easy. Linear's new LT1074 is a simple, elegant solution for your stepdown and inverting switching regulator applications. It's a 5 amp monolithic bipolar regulator with up to 200kHz switching frequency and internal adjustable current limiting. Power switch, oscillator and control circuitry and output monitor are also on the chip. It's a positive "buck" (stepdown) converter with several LTC innovations that also allow the device to be used as a positive to negative converter, a negative boost converter, and a flyback or forward converter.

As a stepdown converter, the LT1074 input voltage range is 8V to 60V. The switch output can swing 40V below the ground, a feature that permits the regulator to perform positive to negative conversion with inputs down to 4.5V. It also allows the use of a tapped inductor for output currents up to 10A with no external switching transistor. A true analog multiplier in the feedback loop lets it respond quickly to input voltage fluctuations. The LT1074 is available in either a 5-lead TO-220 package or an 11-lead single-in-line package at $5.25 and $6.45, respectively, in 100-up quantities. For a data sheet and applications note contact: Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035 or call **800-637-5545.**



Basic Step Down Converter

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EDITED BY CHARLES H SMALL

Buffers stabilize oscillator

Maxwell Strange
Goddard Space Flight Center, Greenbelt, MD

Adding a CMOS buffer to a classic op-amp oscillator dramatically improves its performance, while preserving its low cost and low power consumption.

The overriding source of frequency drift in **Fig 1a** is the nonsymmetry and variability of the op amp's output-saturation voltages. These effects produce output-amplitude variations, which, when fed to the inputs via R_1 and R_2, produce switching-threshold changes. Supply voltage, temperature, loading, and op-amp selection also affect these saturation voltages. You can clamp the op amp's output with reference diodes, but these diodes are expensive and power hungry.

The circuit of **Fig 1b** overcomes these problems and has other advantages as well. Gates A and B produce a rail-to-rail voltage swing to feed back to the circuit's input, eliminating the saturation-voltage drops of the op amp. If you select the proper op amp, only the circuit's passive components will affect its frequency stability. The circuit's output symmetry is near perfect over a wide range of supply voltages. Further, the buffers' output transitions are much faster than the op amp's slew-rate-limited transitions, allowing you to use a micropower op amp.

The circuits' output frequency is

$$f_O=\frac{\log e}{2\log\left(1-\dfrac{2R_1}{2R_1=R_2}\right)RC},$$

$$R_1=\frac{R_1' R_2'}{R_1'+R_2'}.$$

$$\text{if } R_2=3R_1,\ f_O\approx\frac{0.979}{RC}$$

(EDN BBS DI #933)

To Vote For This Design, Circle No. 746

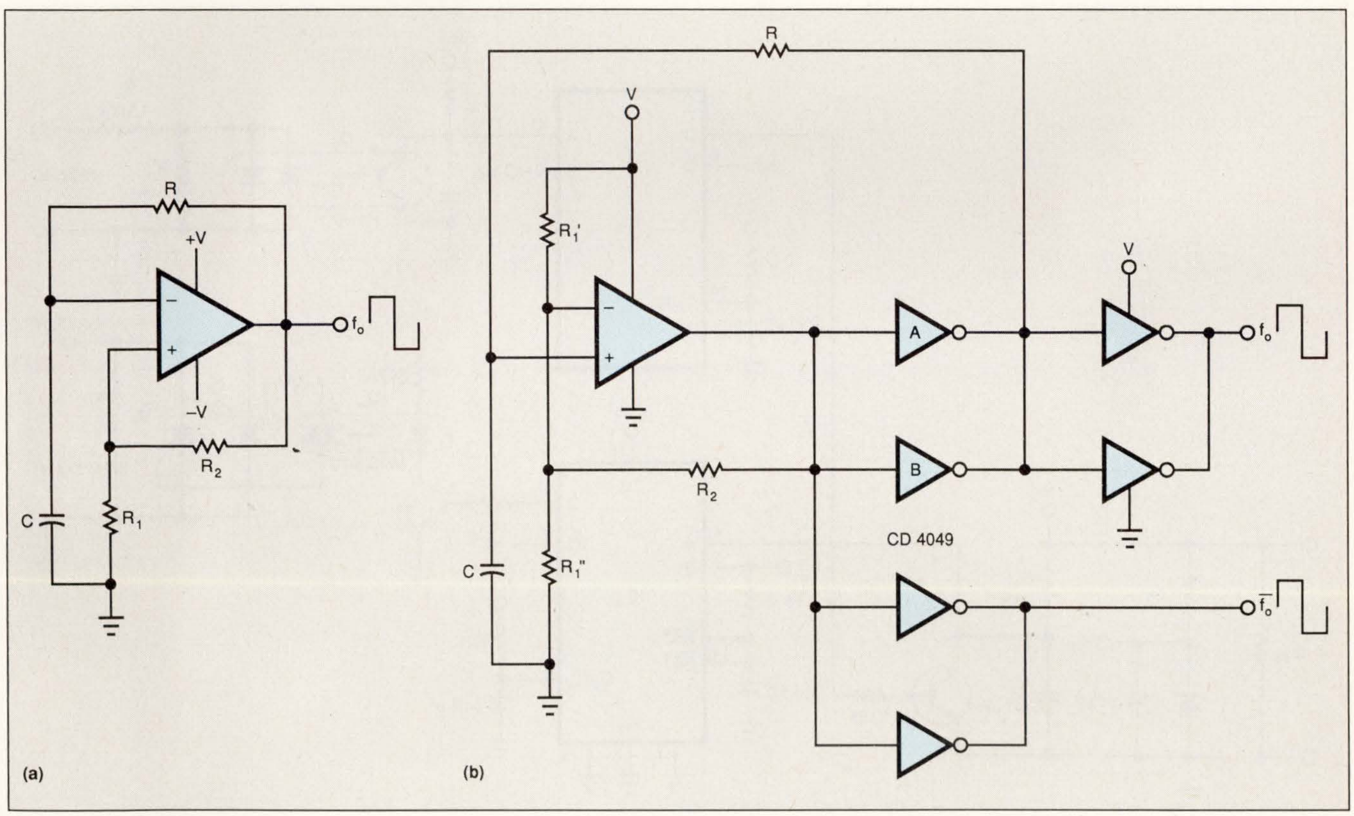


***Fig 1—Adding CMOS buffers to a** classic op-amp oscillator (**a**) improves the oscillator's performance without significant increases in power consumption or cost (**b**).*

Current loop controls SCRs

Robert Diffenderfer
Gordos, Rogers, AR

The circuit in **Fig 1** allows a 4- to 20-mA loop to control an isolated (4000V) SCR drive. The SCR drive can, in turn, control lighting intensity or motor speed. With a 4-mA control input, the SCRs will turn on at 90 and 270° with respect to the power input. By increasing the control input to 20 mA, the SCRs will turn on at 0 and 180°.

The current loop develops a control voltage across R_1. D_1 and associated components clamp this voltage to 5V max to power 1-shots IC_{1a} and IC_{1b}.

Optoisolator Q_2 detects the zero crossings of the 120V ac input, providing a low-to-high transition that triggers 1-shot IC_{1b}. R_3 and R_4 affect the transition's timing. You can adjust these components to compensate for propagation delays. When triggered, 1-shot IC_{1B} produces a 0.1-msec pulse. The pulse turns on Q_1, discharging capacitor C_2.

When Q_1 turns off, C_2 begins charging. The voltage across R_1 and the value of R_2 set the rate at which C_2 charges. IC_{1a} will produce a 0.1-msec pulse when the voltage on C_2 reaches approximately 2.5V. This pulse turns on either SCR_1 or SCR_2 via optoisolator Q_3. C_2's charge time is

$$t = -R_{32} \times C_2 \times \ln\left\{1 - \left(\frac{V_C - V_I}{V_F}\right)\right\},$$

where

V_C = the input-logic threshold voltage (voltage across C_2),

V_F = the voltage across R_1 (a function of the input curent), and

V_I = the voltage to which C_2 was discharged $\approx$0.3V).

You may want to adjust the values of R_2 and C_2 to compensate for highly inductive loads.
(EDN BBS DI #935)

To Vote For This Design, Circle No. 747

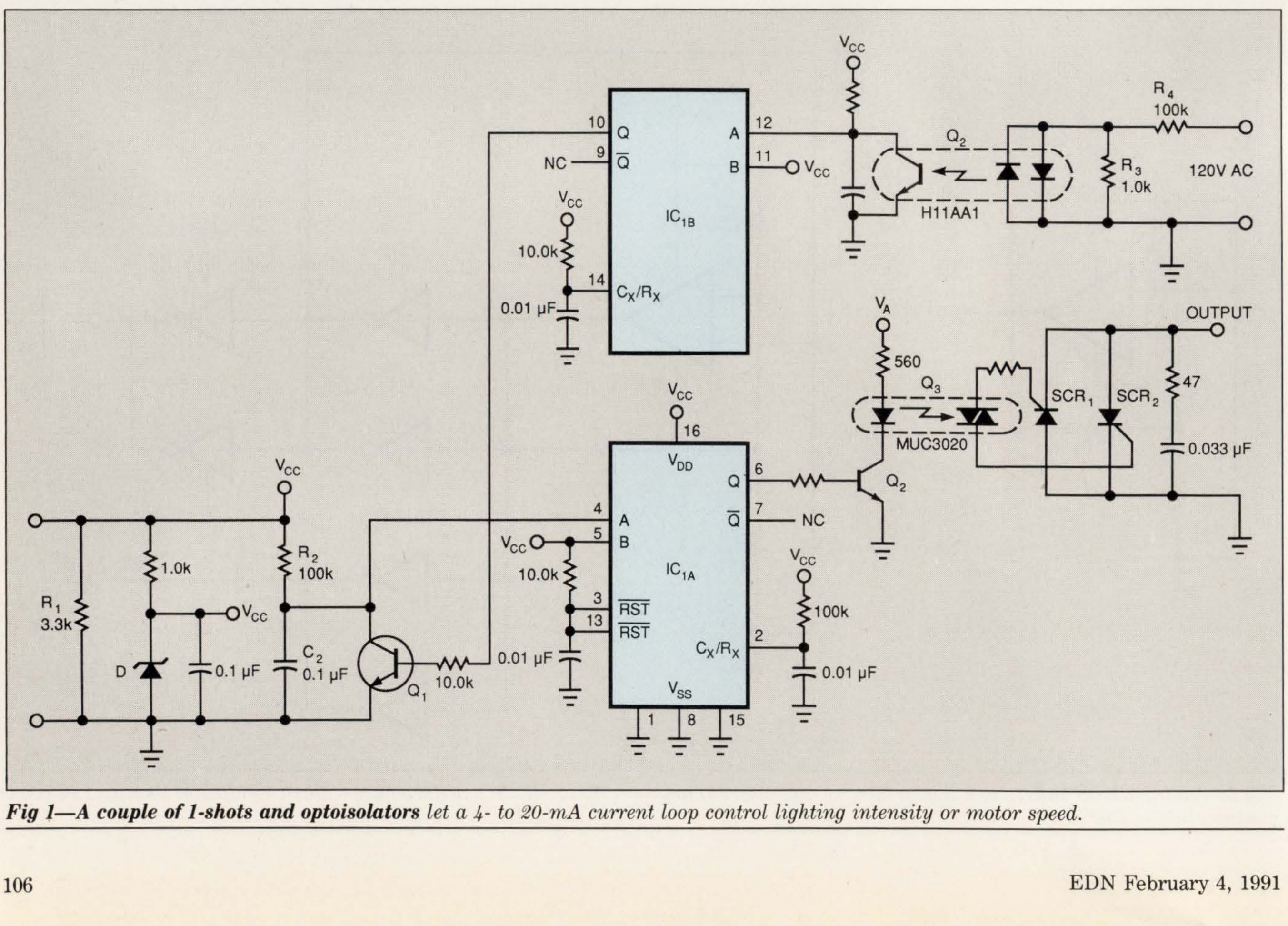
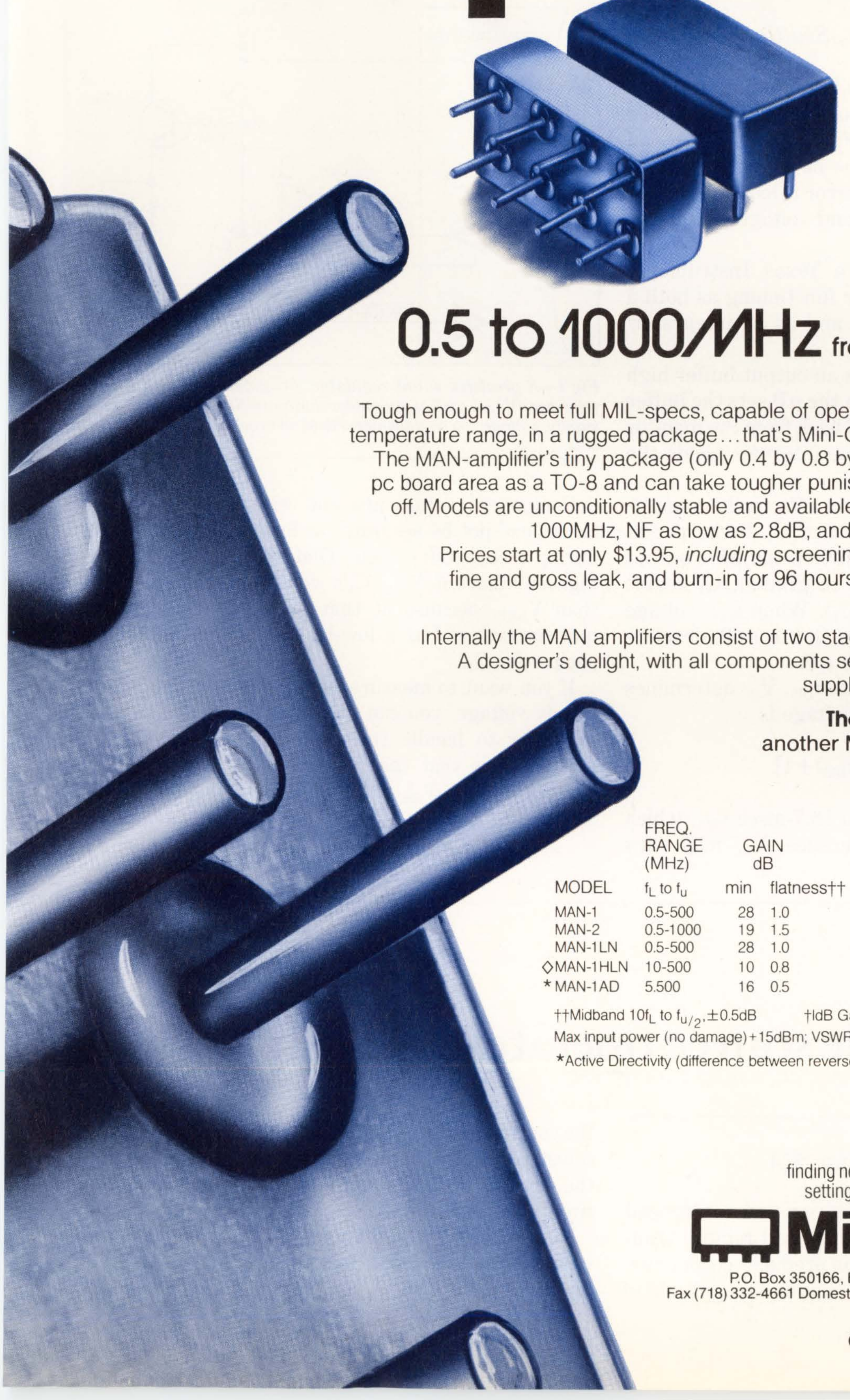


Fig 1—A couple of 1-shots and optoisolators *let a 4- to 20-mA current loop control lighting intensity or motor speed.*

rugged plug-in amplifiers



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◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
*MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_{u/2}$, ±0.5dB   †ldB Gain Compression   ◇Case Height 0.3 In.
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CIRCLE NO. 112

C118 REV. E

Regulator measures battery voltage

Mark Freeman
Stratos Product Development, Seattle, WA

If your low-power μP system is battery powered, the μP can use a precision regulator to monitor its own battery voltage. The circuit in **Fig 1** uses no precision passive components and requires no trimming. Error is less than ±3%, and linearity error is less than ±1%. You must write a short control and voltage-calculation routine for your μP.

The heart of the circuit is a Texas Instruments TL431 precision shunt regulator functioning as both a voltage reference (V_{REF}=2.5V) and as an integrator/amplifier.

In operation, the μP first sets an output buffer high for a programmed interval. Then the μP sets the buffer low and waits for a trigger signal back from the monitor circuit. The ratio of the two time intervals yields the supply voltage.

While the output buffer is high, effectively connecting R_1 to the positive rail, capacitor C_1 discharges at the rate of $(V_{CC}-V_{REF})/(R_1C_1)$. When the μP's output buffer goes low, connecting R_1 to ground, C_1 begins charging at the rate $(V_{REF})/(R_1C_1)$. When C_1's voltage reaches the turn-off voltage of Q_1, Q_1 turns off, developing the $\overline{\text{TRIGGER}}$ signal for the μP.

The μP fixes the discharge time τ_{DIS}. V_{CC} determines the charge time, τ_{CHG}. Battery voltage is

$$V_{CC}=V_{REF}[(\tau_{CHG}/\tau_{DIS})+1].$$

The components in **Fig 1** yield a 16.7-msec τ_{DIS}, which will integrate out 60-Hz interference. V_{CC} may vary between 3.5 and 6.0V.

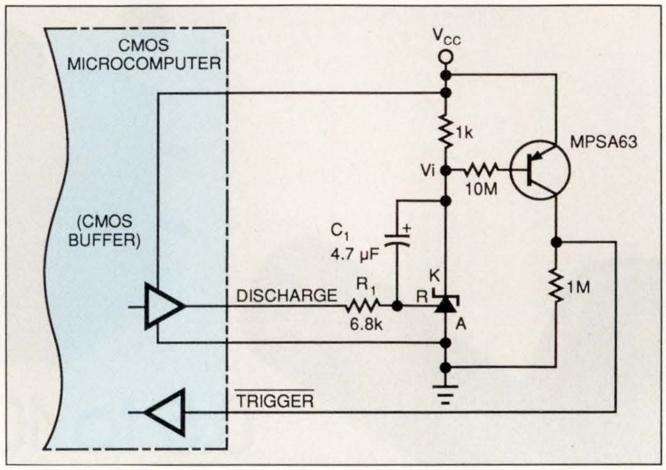

***Fig 1—A precision shunt regulator,** functioning as both a voltage reference (V_{REF}) and as an integrator/amplifier, measures its own supply voltage via voltage-dependent charge/discharge time intervals.*

Component values are not critical, and your μP's clock need not be accurate, as long as it does not drift during a conversion cycle. Choose C_1 such that at the highest value of V_{CC}, C_1's voltage never goes lower than V_{REF}, because at that point the regulator will quit operating. Use a low-leakage, solid-tantalum capacitor for C_1.

If you want to measure some voltage other than the supply voltage, you can use an external CMOS switch or buffer to handle the switching chores. The only restriction is that the voltage to be measured must be greater than V_{REF}. **(EDN BBS DI #932)** EDN

To Vote For This Design, Circle No. 748

Programmable source operates precisely

Jim Williams
Linear Technology Co, Milpitas, CA

Precise, voltage-programmable, ground-referenced current sources are usually complex and require trimming. **Fig 1**'s simple configuration produces output current in strict accordance to the sign and magnitude of the control voltage, V_{IN}. The circuit's dynamic response is well controlled, and the circuit requires no trimming; the circuit's accuracy and stability depend almost entirely upon resistor R.

IC_1, biased by V_{IN}, drives current through R (in this case, 10Ω and the load). Instrumentation amplifier, IC_2, operating at a gain of 100, senses the voltage across

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ISSUE WINNER

The winning Design Idea for the November 8, 1990 issue is entitled "Buffer increases precision," submitted by Barry L Siegel of Elantec Inc (Milpitas, CA).

Your vote determines this issue's winner. All designs published win $100 cash. All issue winners receive an additional $100 and become eligible for the annual $1500 Grand Prize. **Vote now**, by circling the appropriate number on the reader inquiry card.

R. IC_2's output closes the loop back to IC_1. Because IC_1's loop forces a fixed voltage across R, the current through the load is constant. The 10-kΩ/0.05 μF combination sets IC_1's roll-off, making the circuit stable.

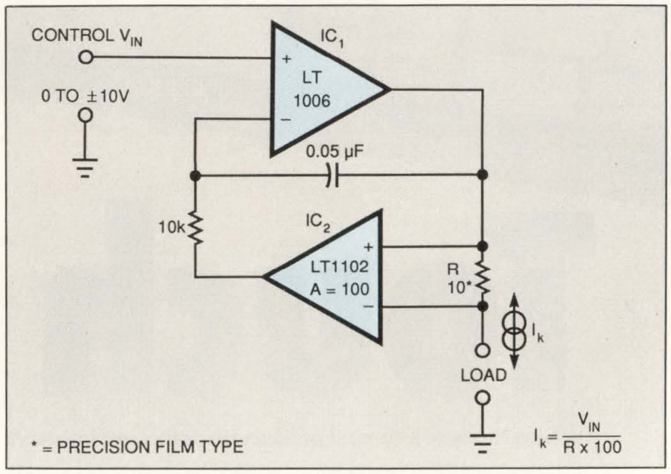

Fig 1—This programmable current source's dynamic response is well controlled, and the circuit requires no trimming.

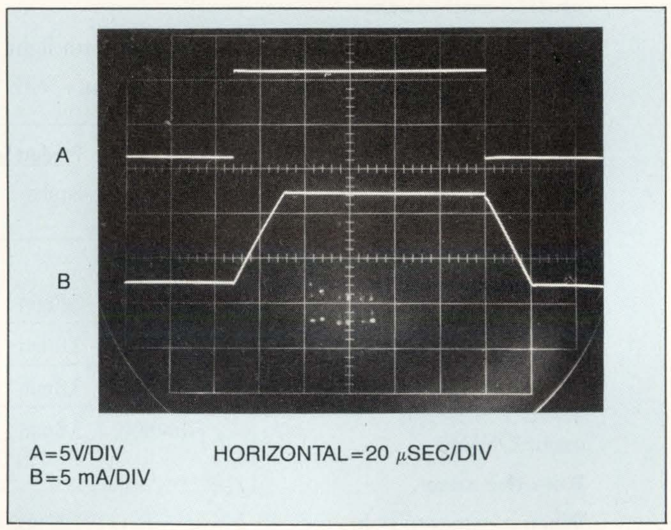

Fig 2—For a full-scale input step, Fig 1's response is clean with no slew residue or aberrations. Trace A is the voltage-control input, and Trace B shows the output current.

Assuming an errorless component for R, IC_2's 0.05% gain specification and its 5-ppm/°C temperature coefficient dominate the circuit's initial error. High-grade film or wirewound resistors will not degrade this level of performance.

Fig 2 shows the circuit's dynamic response for a full-scale input step. Trace A is the voltage-control input, and Trace B is the output current. Response is clean, with no slew residue or aberrations.

(EDN BBS /DI_SIG #931) EDN

To Vote For This Design, Circle No. 749

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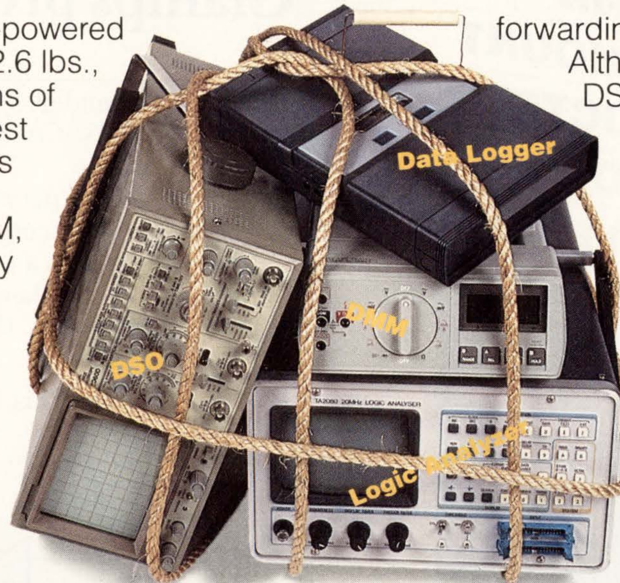

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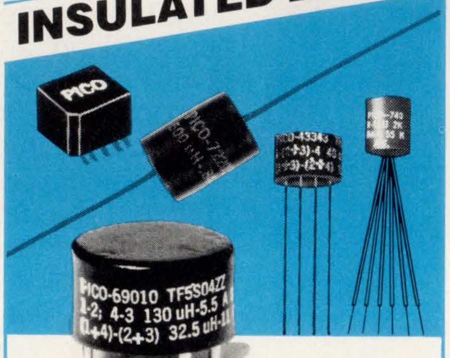

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Clamps provide self-test

Maxim Jay Skender
Microrobotics, St Charles, IL

You can get double duty from your clamping diodes if you tie them to the output of a D/A converter (or an op amp configured as a converter). In this fashion (**Fig 1**), you can use the clamping diodes as a controllable input during self-tests. **(EDN BBS DI #934)** **EDN**

To Vote For This Design, Circle No. 750

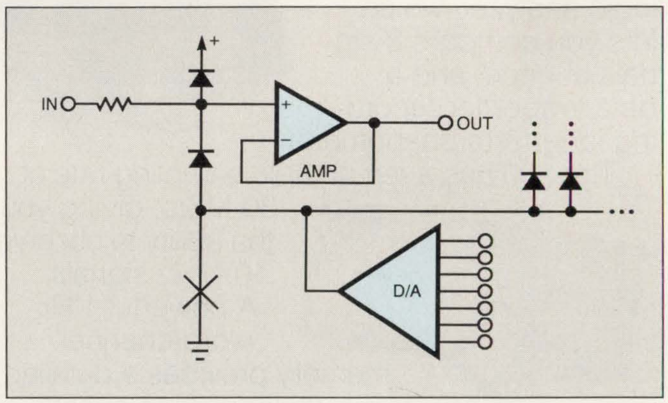

Fig 1—Clamping diodes become controllable *inputs during self-test if you connect them to a D/A converter instead of either the supply raid or ground.*

FEEDBACK AND AMPLIFICATION

PLD is really a PROM

We did some checking for an interested reader and found out that a part an author (and company) called a PLD was really a PROM. The Design Idea "PLD adds flexibility to motor controller" on pg 177 of EDN's March 1, 1990 **(DI #808)** issue contains a part labeled PLE5P8. This part number is an obsolete Monolithic Memories Inc designation for a simple 32×8-bit PROM.
Anne Watson Swager and Charles H Small
Design Ideas Editors **EDN**

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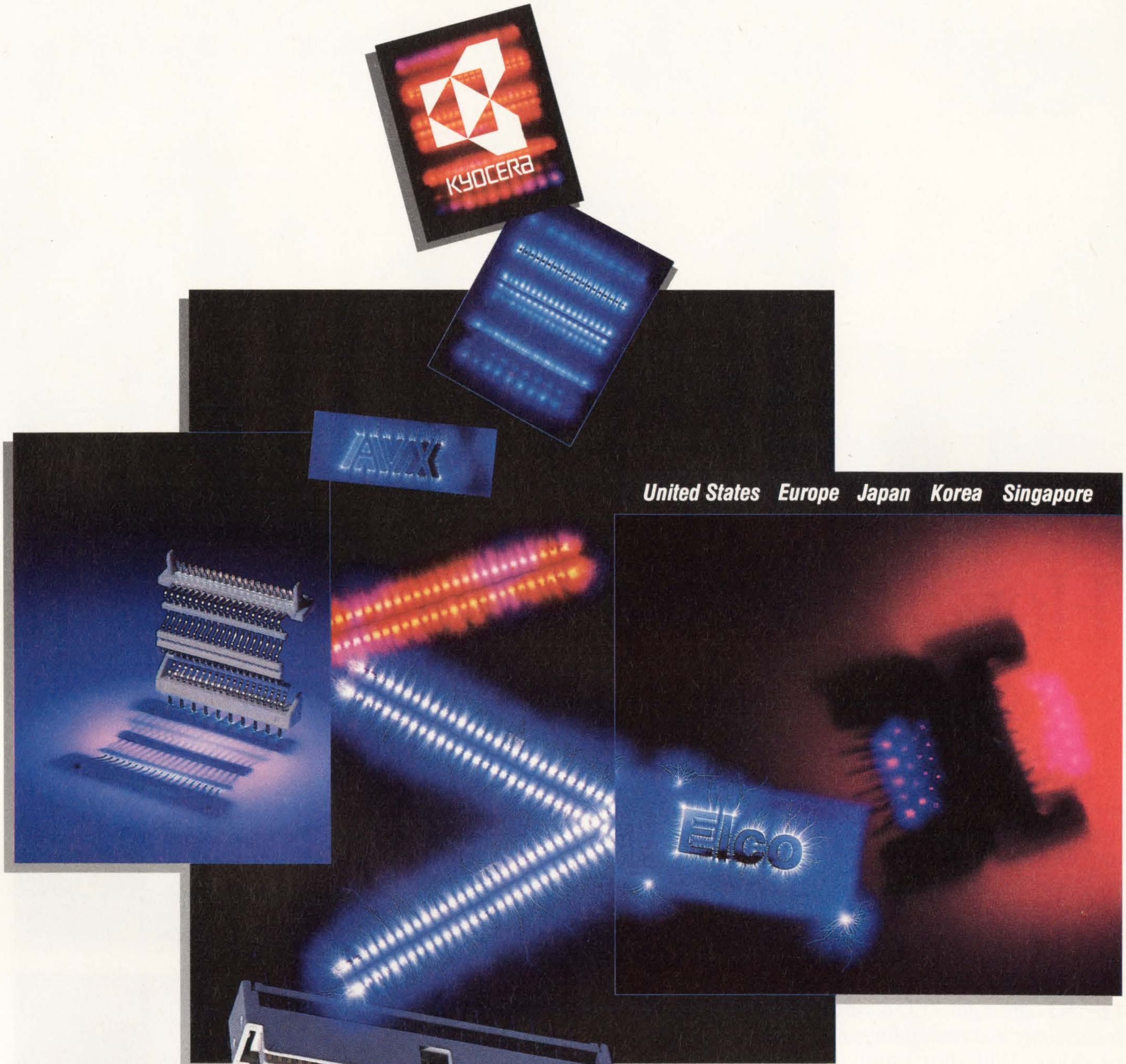

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CIRCLE NO. 70

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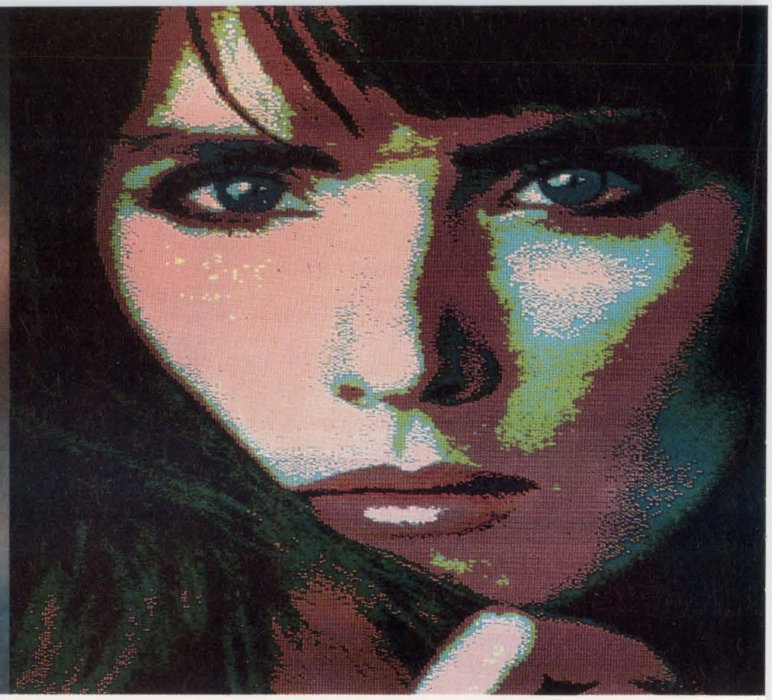

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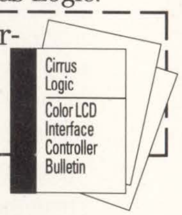

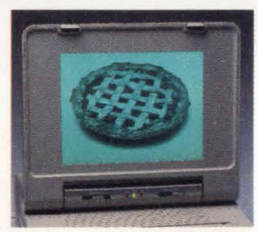

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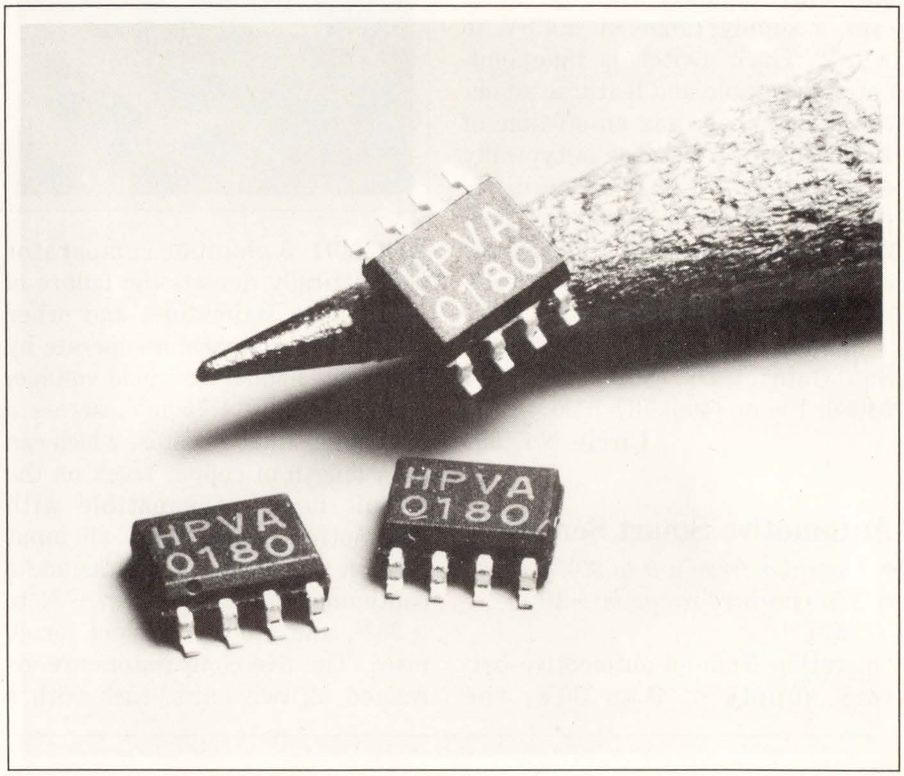
The HPVA-0810 is a monolithic variable-gain amplifier that features 20 dB of gain and gain control over its entire dc-to-2.5-GHz bandwidth. Operating from a single 6V supply, the amplifier dissipates only 250 mW. Designed for use in VHF/UHF receivers, RF data links and broadband local-area networks, the amplifier can replace more expensive hybrid devices, which typically have narrower bandwidths. The device is available in a surface-mount SO-8 package. HPVA-0810, $13.25 (100).

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 351



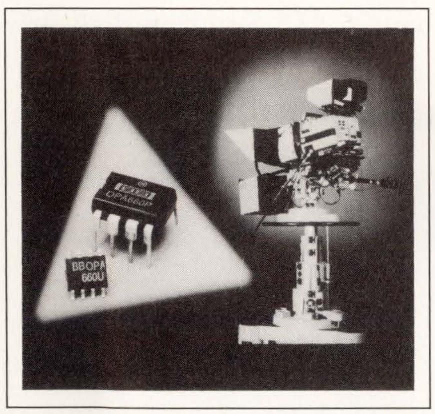
1M-Bit CMOS DRAMs

- *Feature 60-nsec speed*
- *Support μPs with speeds to 16 MHz*

With Read/Write cycle times as low as 110 nsec, the AAA1M300 series of CMOS DRAMs (dynamic RAMs) allows designers to implement zero-wait systems utilizing 16-MHz μPs. Complex interleaving or caching schemes are not necessary. The high-speed DRAM is also available in enhanced-page-mode versions with Read/Write cycle times of 25 nsec. The devices work over a supply range of 4.5 to 5.5V and a temperature range of 0 to 70°C. The DRAMs are available in DIPs, ZIPs, and SOJ packages with industry-standard interfaces and pinouts. $5 (10,000).

NMB Technologies, 9730 Independence Ave, Chatsworth, CA 91311. Phone (818) 341-3355. FAX (818) 341-8207. TLX 651340.

Circle No. 352



Transconductance Op Amp

- *Has 700-MHz bandwidth*
- *Slew rate is 3000V/μsec*

Called an operational transconductance amplifier (OTA), the OPA660 combines a voltage-controlled current source with a separate buffer amplifier. By programming the quiescent current using a single external resistor, users can optimize gain- and bandwidth-tradeoffs. The complementary emitter-follower buffer section provides a 700-MHz bandwidth, a 3000V/μsec slew rate, 0.06% differential gain error, and 0.02% differential phase error. Transconductance for the OTA section is 125 mA/V. You can connect the OTA and buffer sections to create a current-feedback amplifier. The OPA660 comes in 16-pin DIPs and SO packages, $4.35 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111.

Circle No. 353

Quad SPST Analog Switch

- *Operates from a 5 to 30V supply*
- *Needs no V_{REF} supply*

The HI-201 monolithic quad spst analog switch operates from a single 5V to 30V supply. The IC eliminates the need for a V_{REF} supply, which is normally required for operation with power supplies other than ±15V to maintain TTL compatibility without pull-up resistors.

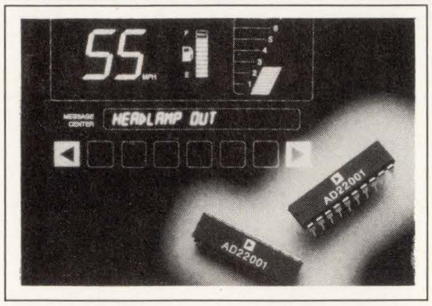
A plug-in upgrade for the Harris HI-201, the IC typically consumes only 4 mW of power while operating over a supply range of ±4.5V to ±18V. Each switch is independently selectable and features an on-time of 260 nsec and an off-time of 100 nsec. On-resistance is typically 45Ω. The device is available in 16-pin DIPs, ceramic DIPs, SO, and 20-pin LCC packages in commercial, industrial and military temperature ranges. From $2.06 (1000).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.
Circle No. 354

Automotive Smart Sensor

- *Operates from a 9 to 30V supply*
- *Temperature range is −40 to 125°C*

Operating from an automotive battery supply of 9 to 30V, the



AD22001 5-channel comparator automatically detects the failure of headlamps, indicators, and other lights. The comparators operate by detecting a small threshold voltage, nominally only 1.75 mV, across a low-value shunt resistor, which can be a length of copper track on the circuit board. Compatible with automotive applications, all input pins on the sensor will withstand a continuous dc voltage from −34 to +36V, and a 60V transient for 40 msec. The five comparators are arranged as two pairs, each with a common output, and one comparator with a dedicated output. The comparator pairs test any two related lights in either the on or off condition, indicating a failure of one or both. The single comparator is intended for brake-light testing. The AD22001, which comes in a 20-pin plastic DIP, is specified for operation of a −40 to 125°C temperature range. $2 (OEM qty).

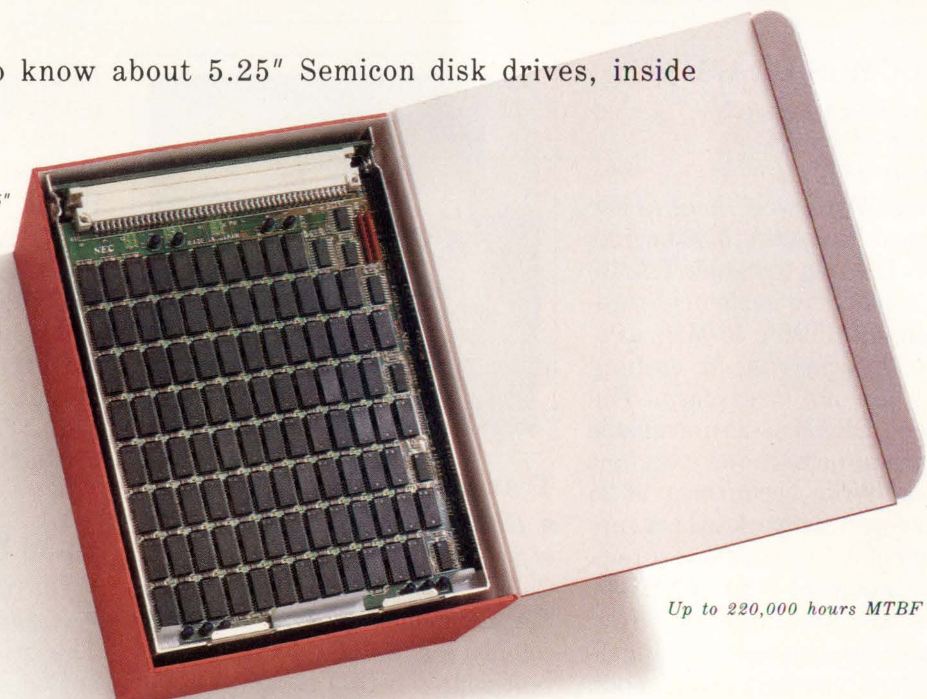
Analog Devices Inc, 804 Woburn St, Wilmington, MA 01887. Phone (617) 937-2381. **Circle No. 355**

Motor Controller

- *Needs no Hall sensor*
- *Compatible with Delta/Y/Star motors*

The first of the company's Hall-sensorless ICs, the SSI-32M595 provides motor speed control for both 5V and 12V Delta/Y/Star motors. The μP's starting the motor

All you need to know about 5.25" Semicon disk drives, inside



C&C
Computers and Communications

It's nice to know that NEC disk drives have the most advanced technical features. And it's reassuring that they're consistently available, and with a DOA rate of less than 1%,and up to 220,000 hours MTBF rate that they're reliable.

initiates the drive control, which activates EMF-induced self-commutation in the SSI-32M595. The controller's EMF circuitry typically detects motion within the first revolution of the motor. Speed control, which is implemented through a control loop, is maintainable over a range of speeds to an accuracy of ±0.017%. The controller operates from a single 5V supply and comes in a variety of packages, including a 28-pin SO package. $5 (1000).

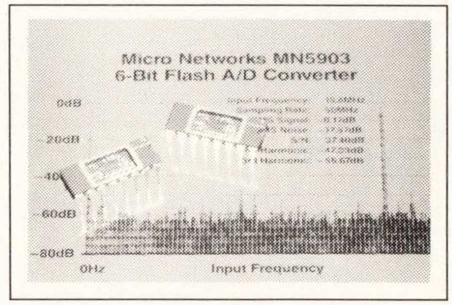
Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Phone (714) 731-7110. FAX (714) 669-8814.

Circle No. 356

High-Speed, 6-Bit Flash A/D Converter

- *Conversion speed of 75 MHz*
- *140-MHz full-power bandwidth*

A pin-compatible upgrade to the AD9000, the MN5903 offers improved S/N ratios and a wider bandwidth. At 540 kHz, the S/N ratio is 38 dB; at 35 MHz, it remains high, at 36 dB. Full-power bandwidth is 140 MHz. The converter is available in two logic configurations. You can also use the MN5903A as a standalone 6-bit ADC or as a terminating device for 7- or 8-bit applications. The MN5903 is for use as a cascading device with the MN5903A for

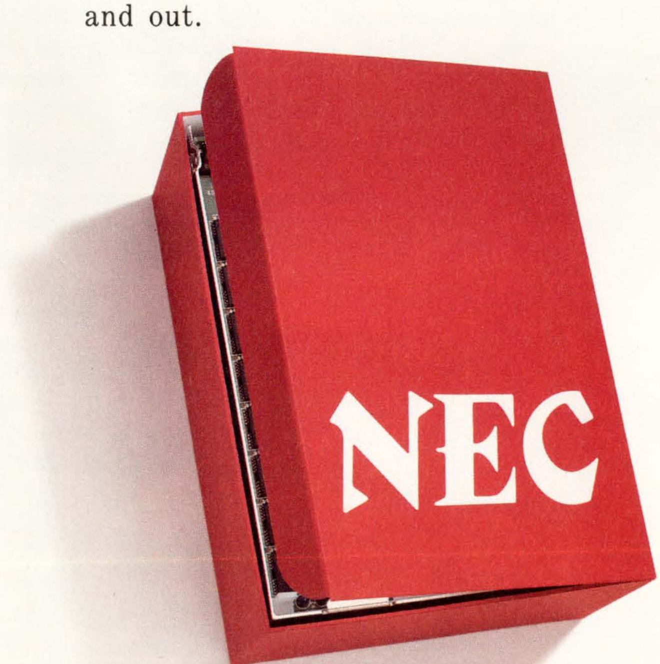


7- or 8-bit applications. The parts differ only in their output coding for signals greater than V_{REF}. In the overrange, the MN5903's outputs are set to a logic "0;" the MN5903A's outputs are set to a logic "1." The converters come in a 16-pin, hermetically sealed DIP. Commercial devices, from $39; extended-temperature-range devices, from $85 (100).

Micro Networks, 324 Clark St, Worcester, MA 01606. Phone (508) 852-5400. FAX (508) 853-8296.

Circle No. 357

and out.



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But all you really need to know is that they're made by NEC, a 24-billion-dollar company, and the fourth largest manufacturer of disk drives in the world. For more information, call 1-800-NEC-INFO.

NEC

CIRCLE NO. 11

CUSTOMIZING YOUR WAVEFORM ANALYSIS DOESN'T TAKE A PC.

IT JUST TAKES A LITTLE TACT.™

The company that gave you the first digital oscilloscope, the longest memory, best resolution and greatest storage capacity has gone a giant step further toward the perfect scope. All you need is a Nicolet 400 Series DSO - and TACT.™

TACT software elevates Nicolet's 400 Series DSO into the first application-specific oscilloscope. It gives you the power to say and do the right thing at the right time – to enhance the productivity of your test capabilities.

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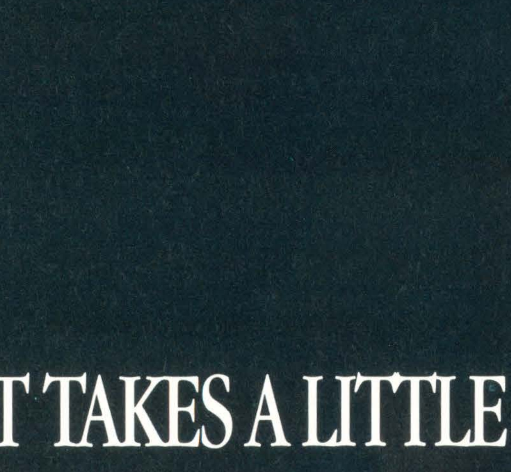
Other scopes give you waveforms. Nicolet gives you answers. Forget the PC. You don't need one. Program directly on the scope using a built-in, full-screen editor and 101-key PC-type keyboard. Creating your own custom programs, calculations and plots has never been this fast...this simple. Time savings are dramatic as TACT's LEARN mode writes and remembers most of your programs for you. Automatically.



Perform complex data reductions. Print a complete analysis. Plot trends from previous tests. And automate pass/fail decisions. They're no problem. You just need TACT.

BASIC language – SUPERIOR performance.
A built-in BASIC language with easy access to on-screen prompts and menus puts even more power in your hands. All scope functions, conditional testing, variable storage, custom printer and plotter output capabilities are just a touch away. With TACT, put waveforms in; get reliable answers out.

To simplify your testing you need two things. Nicolet...and a little TACT. Call Nicolet toll free 1-800-356-3090 for further information.

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Toll free in U.S. 1-800-356-3090.

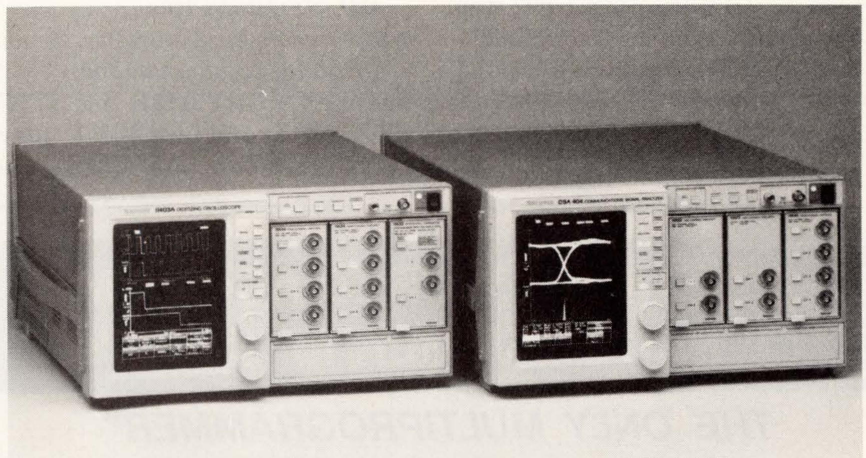
Nicolet
INSTRUMENTS OF DISCOVERY

CIRCLE NO. 91

TEST & MEASUREMENT INSTRUMENTS

1-GHz-Bandwidth Telecomm And General-Purpose DSOs

- *Automatically make eye-pattern measurements*
- *Make statistical measurements*



With appropriate plug-ins, the CSA 404 and 11403A DSOs have a 1-GHz repetitive-signal bandwidth. Both units have color displays. The CSA 404 makes measurements that are useful in communications work. For example, as it acquires signals, the DSO constructs a statistical database, allowing it to measure jitter and noise without user intervention. The same database enables the unit to make direct, automatic eye-pattern pulse measurements. To determine whether a device under test meets specs, the scope can make mask tests; it stores ten masks in nonvolatile memory. The 11403A, a general-purpose scope with DSP capabilities and as many as eight channels, also makes pass/fail tests. It can display six such measurements simultaneously. CSA 404, $22,000; 11403A, $18,950.

Tektronix Inc, Box 19638, Portland, OR 97129. Phone (800) 426-2200. **Circle No. 360**

Real-Time ICE For 33-MHz i960CA RISC µP

- *Interfaces with MS Windows 3.0*
- *Performs nonintrusive monitoring and control*

The Express Plus is an IBM PC/AT-hosted real-time in-circuit emulator that nonintrusively monitors and controls the 33-MHz version of the i960CA RISC (reduced-instruction-set computer) µP. The unit's software runs under MS Windows 3.0. The target processor remains in the target system, reducing the likelihood that connecting the emulator will interfere with proper target operation. Besides passively monitoring the µP's bus, the instrument uses all of the control information available from the µP to reconstruct programs executing from cache memory. It lets you halt the processor, execute single instructions, set software and hardware breakpoints, examine registers, and trace program execution. The unit is compatible with C-language tools from Intel and Microtec Research. You can obtain interfaces to the SGDB960 and Xray source-level debuggers. $28,750. Delivery, 60 days ARO.

Step Engineering Inc, Box 3166, Sunnyvale, CA 94088. Phone (800) 538-1750; in CA, (408) 733-7837. FAX (408) 733-1073. TWX 910-339-9506. **Circle No. 361**

Programmable Power Supply

- *Has three outputs—6V at 2A and dual 28.1V at 125 mA*
- *Uses 12-bit ADC to read back voltages*

The PPS-2806 is a triple-output programmable power supply on a card that plugs into the IBM PC bus. The unit contains one supply rated at 6V and 2A, and a pair of supplies that can produce 28.1V at 125 mA. Besides furnishing constant voltage, the last two supplies can produce or absorb constant current. You can also connect them in series or ground their positive or negative terminals. In addition to the supplies, the board contains a 12-bit ADC that can monitor voltage, current, or resistance. The board comes with menu-driven software that displays the outputs and ADC readings in numerical and graphic form. You can also control and monitor the board by reading from, and writing to, its registers. $1295.

Analyx Inc, Box 14644, Fremont, CA 94539. Phone (415) 656-8017. FAX (415) 657-0927. **Circle No. 362**

RTD Simulators

- *Produce errors as low as ±0.005%*
- *Use Waidner-Wolf shunt circuits to minimize errors*

The RTD-100, RTD-100X, RTD-200, and RTD-500/1000 simulate resistance-temperature detectors (RTDs), sometimes called platinum resistance thermometers. The RTD-100X is accurate to ±0.005% over its range of 10 to 1111.11Ω. To minimize errors caused by contact resistance, the units use Waidner-Wolf shunt circuits on their three most sensitive ranges. With this technique, a contact resistance of 1.5 mΩ affects the measured resistance by 4 μΩ, a value that represents a 0.4% error in a 1-mΩ step, the smallest step. $600 to $1795.

General Resistance, Box 185, North Branford, CT 06471. Phone (203) 481-5721. FAX (203) 481-8937.

Circle No. 363

VMEbus-Based Simulators For MIL-STD-1553 Bus

- *Test and simulate MIL-STD-1553 Bus*
- *Operate as bus controller, remote terminal, or bus monitor*

The EXC-1553VME/E and EXC-1553VXI/E are intelligent interfaces between the VME- and VXIbuses and the MIL-STD-1553 bus. The modules can also simulate and test the MIL-STD-1553 bus. The vendor furnishes the modules in B and C sizes. They can operate as bus controllers, remote terminals, or bus monitors. In all of these modes, they can detect errors; in the controller and terminal modes, they can inject errors under program control. The units have a memory-mapped interface. Options include sinusoidal and variable-amplitude transceivers. From $6995.

Excalibur Systems Inc, Box 6839, Fresh Meadows, NY 11356. Phone (718) 357-3500. FAX (718) 357-3544. TWX 650-347-3609.

Circle No. 364

EXPERIENCE A WORLD ACCLAIMED PLD PROGRAMMER for the 90's.

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BYTEK's Model 135H is a GANG/SET or Universal PLD MULTIPROGRAMMER® All-In-One Site. Performs well in both Production or Development environments. Purchase only the technology support you need today and expand support as required through simple micro disk device library updates.

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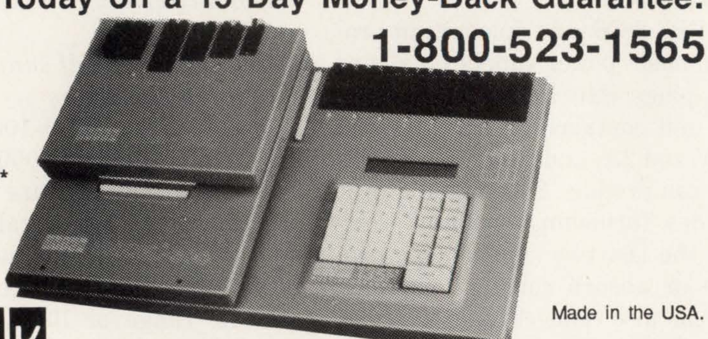

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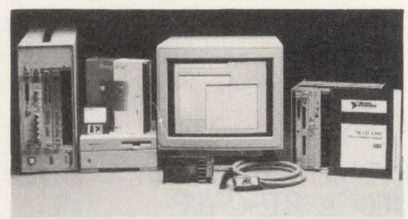


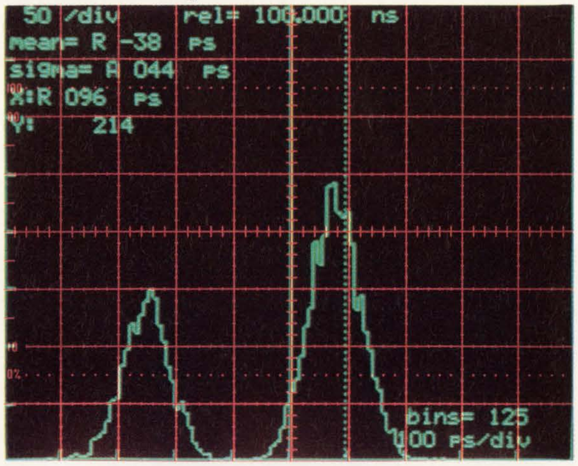
SPARCstation Interfaces To VXI and VME Buses

- *Plugs into workstation's Sbus*
- *Interfaces to 6U VME systems and B- and C-size VXI systems*

The VXI-SB2020 and VME-SB2020 kits allow you to control VXI and VME systems from Sun Microsystems' SPARCstation workstations. Each kit includes a card that plugs into the workstation's Sbus and generates the MXI (multisystem extensions interface) bus. A 2m MXI cable is included. Also in each kit is a module that receives the MXI bus and plugs into the VXI or VME bus. The VXI kit includes a C-size slot-0 board. The VME kit contains a 6U VME card that works in VME systems and in B-size VXI systems. Both kits include software tools that run under the SunOS operating system. These tools allow you to configure system resources and to control and transfer data to

A picture is worth a thousand points in a time interval measurement.

SR620 Output



HP5370B Output

The SR620 brings graphic statistical analysis to time interval and frequency measurements. The SR620 shows you more than just the mean and standard deviation - multimode frequency distributions or systematic drift for example. Histograms or time variation plots are displayed on any X-Y oscilloscope, complete with Autoscale, Zoom, and Cursor functions. Hardcopy to plotters or printers is as easy as pushing a button.

Of course, the SR620 does everything else you'd expect from a high resolution universal counter, such as frequency, period, time interval, pulse width, rise / falltime, and phase measurements. The SR620 offers 25 ps single-shot time and 11 digit frequency resolution and complete statistical analysis, all for a fraction of the cost of comparable instruments.

For the whole picture, call SRS and ask about the SR620.

SR620 $4500

- 4 ps single shot least significant digit
- 25 ps rms single shot resolution
- 1.3 GHz maximum frequency
- 10^{-9} Hz frequency resolution
- Sample size from 1 to 1 million
- Frequency, period, time interval, phase, pulse width, rise and fall time
- Statistics - mean, standard deviation, min max, and Allan variance
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- Hardcopy to printer or plotter
- GPIB and RS232 interfaces
- Optional oven timebase

SRS STANFORD RESEARCH SYSTEMS

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VXI and VME modules. C-size VXI kit, \$3700; VME/B-size VXI kit, \$3300.

National Instruments Corp, 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488 (US and Canada); in TX, (512) 794-0100. FAX (512) 794-8411.

Circle No. 365

Pocket-Size ESD Tester

- *Checks static-protective items*
- *Shows discharges produced by touching conductors*

The Zapflash electrostatic-discharge tester is the size of a pocket flashlight. You can use it to test static-protective devices, such as wrist straps and antistatic mats. It can also show when a discharge occurs as a result of touching high conductivity areas of objects charged to different potentials—for example, an IC pin and a pc-board trace. You can also use the unit for tests unrelated to static discharges; for example, it can find the "hot" terminal of an ac receptacle. \$19.95.

Anderson Effects Inc, Box 657, Mentone, CA 92359. Phone (714) 794-3792. **Circle No. 366**

SURVIVAL OF THE FASTEST

Cheetah makes your AT fit for the DSP jungle

At 49.5 MFLOPS (285 MOPS, total), Atlanta Signal Processors' Cheetah™ is one of the fastest cats around. The new DSP add-in board is based on Motorola's DSP96002 – the first floating point digital signal processor to use IEEE 754 Standard SP (32-bit) and SEP (44-bit) arithmetic.

In addition to the DSP96002, the Cheetah board houses two Motorola DSP56001 fixed point processors and up to two Mbytes of zero-wait state static RAM. A large family of special-purpose daughter boards is available to take advantage of Cheetah's flexible I/O and memory architecture.

The ASPI board is a versatile tool for developing DSP96002-based systems, including speech coding, color video, stereo sound, three-dimensional graphics and other multimedia applications.

Among the more useful daughter boards are an A/D-D/A data acquisition system, 64-Mbyte memory expansion board and a multi-processor interface.

And you don't need to be a fat cat to own a fast cat. Cheetah can turn your AT into a supercomputer for a very modest investment. For detailed specifications and prices, contact

aspi

WORLD LEADERS IN DSP DESIGN TOOLS

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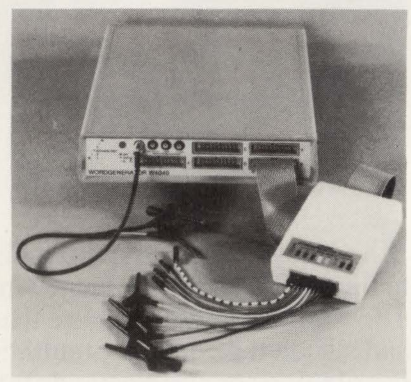
CIRCLE NO. 13



40-MHz, 36-Channel Pattern Generator

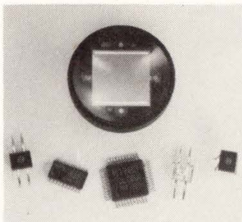
- *Interfaces to IBM PC via parallel port*
- *Each channel has 2k-bit data buffer*

The R3700 40-MHz digital pattern generator attaches to IBM PCs and compatible computers or IBM PS/2 series computers via a parallel port. It produces outputs compatible with TTL and CMOS logic in continuous, single-shot, and burst modes. The generator has 32 standard data channels and four channels with 3-state outputs. Also included are clock and trigger inputs and outputs. Each data channel has 2k bits of buffer memory (2k × 2 bits for the 3-state channels). The software that accompanies the generator allows editing of data and storing of files in a variety of formats. The software can also produce timing diagrams. \$2995.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. **Circle No. 367**

ADVERTISEMENT

Position-Sensitive/ Ranging Components

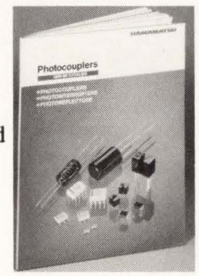


Hamamatsu offers a variety of auto-focus and position detectors especially designed for proximity switching, displacement sensing and optical distance measurements. They are smaller, faster, require less power and feature more stable performance than comparable types.

Applications include auto-focus cameras, computer disc drives, linear motion detection in industrial equipment, beverage dispensers, robotic controls and automated car wash equipment.

CIRCLE NO. 79

Hamamatsu Photocouplers

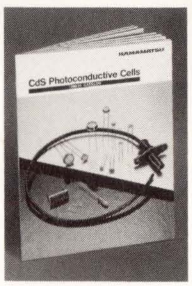


Don't miss our newest catalog. It covers the complete line of Hamamatsu photocouplers including CdS Cell, Photo IC and Phototransistor output types. Also included are photointerrupters and photoreflectors. Many can be used in surface-mount applications for non-mechanical position sensing and high voltage isolation of circuits.

Applications include color video signal interface for TV, high speed I/O computer interface, line receiver interface, electronic motor control and switching regulators.

CIRCLE NO. 79

Hamamatsu CdS Photoconductive Cells



This catalog is a must for every electronics designer. Hamamatsu CdS cells are available in plastic-coated, metal-case and glass-bulb type assemblies for a wide variety of applications.

Applications include exposure meters, light dimmers, musical equipment, flame monitors, street light controls and many others.

CIRCLE NO. 79

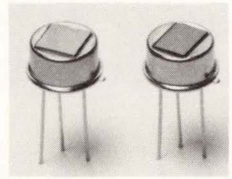
Hamamatsu Photodiodes

Did you know that Hamamatsu offers a complete line of photodiodes? From UV to IR, GaAsP, SI, PIN, APD and GaP, they're all here in our latest catalog. Send for it today.

Applications include high speed light sensors, CAT scanners, X-ray monitors, illuminance meters, light absorption meters, light-to-logarithmic voltage conversion circuits and more.

CIRCLE NO. 79

P2288 and P2613 Pyroelectric Detectors

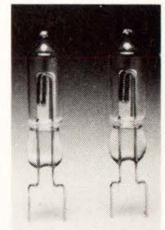


These competitively priced devices feature a large sensitive area and offer optimal spectral response in the near IR. Built-in impedance converting circuitry makes them easy to design into equipment.

Applications include intrusion and fire detectors, industrial robots and other electronic sensing devices.

CIRCLE NO. 79

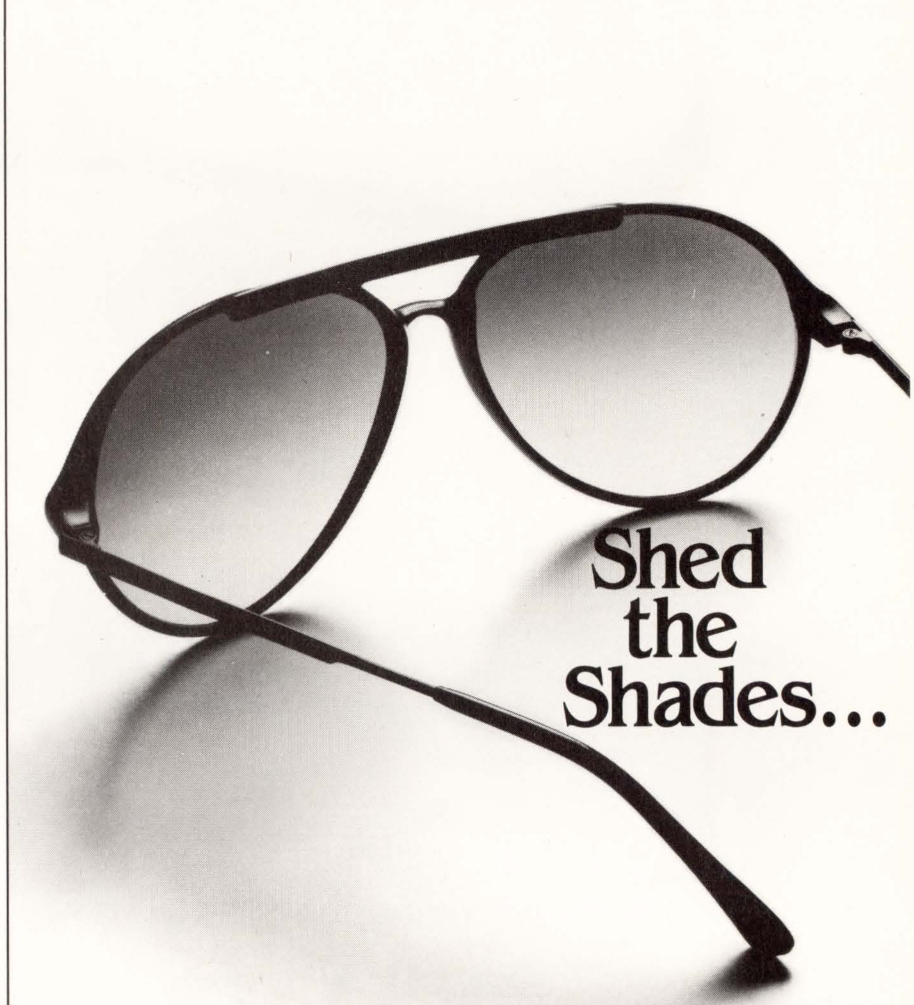
Hamamatsu UVtron R2868 Flame Sensor



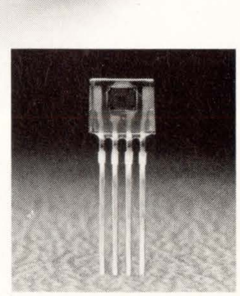
The UVtron flame sensor can detect the ultraviolet radiation of a match from distances greater than 15 feet. Quick detection, wide directivity and compact design make it easy to integrate the R2868 into your products.

Applications include flame detectors for industrial, automotive and petroleum plant environments; also in horse or livestock stables.

CIRCLE NO. 79



WITH SYNCHRONOUS OPTICAL DETECTION.



Hamamatsu's new S3599 Modulated Photo IC rejects background light up to 10,000 lux (5,000 minimum) without even squinting. That makes it ideal for component environments found in office equipment, industrial control equipment or anywhere photo switches are used.

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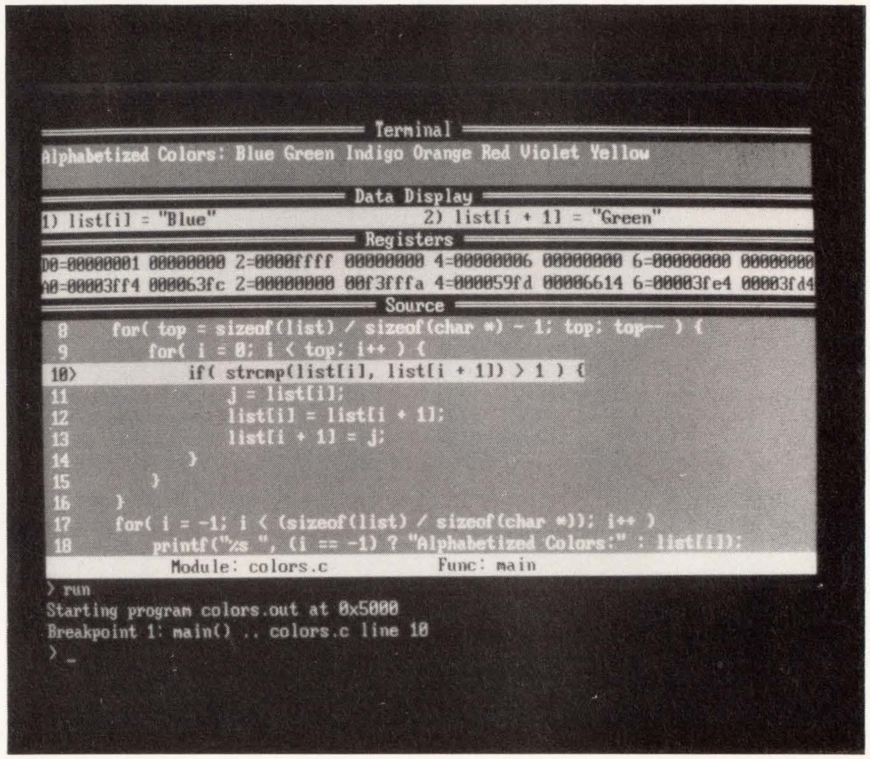
Source-Level C Debugger For Motorola's 68000 μP family

- *Includes cable to connect a target ROM socket to a PC host*
- *Provides six display windows for program I/O and debugging data*



The Quickfix C-language source-level debugger complements the vendor's cross-compiler for 68000-based embedded applications. The debugger makes use of a cable that connects the ROM socket of a target system to a parallel port on the host IBM PC or compatible. To configure the ROM socket driver, you need only specify the ROM socket base address, the socket width (8, 16, or 32 bits), and the ROM size. You can use host RAM in place of the ROM, or you can piggy-back the displaced ROM onto the cable so that both the ROM and the debugger operate simultaneously through the common socket. The debugger provides six windows: The source window displays the C or assembly-language execution context whenever the debugger stops; the register window displays the contents of the processor registers; the command window accepts your commands and displays their results; a data-display window shows the current values of specified C expressions; a terminal window emulates a terminal connected to the target and displays output from the program under test; and a help window provides on-line, context-sensitive debugger command and usage information. Quickfix, \$1750; Quickfix with the Sierra C compiler, \$1500.

Sierra Systems, 6728 Evergreen Ave, Oakland, CA 94611. Phone (415) 339-8200. FAX (415) 339-3844.

Circle No. 358

Printed-Circuit-Board Design System

- *All modules share the same database and user interface*
- *Symbol library includes IBM PC expansion-board symbols*

Eagle (Easily Applicable Graphics Layout Editor) handles all phases of pc-board design, from net-list input through layout to autorouting. All modules share the same database and menu-driven user-interface, so moving from one module to another is fast and easy. You can issue commands from a mouse, a keyboard, or a combination of both; the macro facility lets you assign frequently used command sequences to a function key; the total number of macros is limited only by the amount of available memory. The symbol library includes DIP and SMT devices, Zilog, Intel, and PAL devices, passive components, and standard IBM PC expansion boards. You can edit any of the library symbols and create your own symbols for inclusion in the library. The Undo/Redo feature backs up all command sequences in an unlimited history file, thereby allowing you to recover from errors or unsuccessful design steps. The system can work with both EGA and VGA graphics (color or monochrome) and can output to dot-matrix and laser printers, or to a Gerber photoplotter. To run the program, you need an IBM PC or compatible with at least 640k bytes of RAM and a hard disk; the program will use a mouse or a math coprocessor if these are present. Schematics editor, \$495; Eagle alone, \$399, or \$699 with autorouter; complete system with schematics editor, layout editor, autorouter, and Gerber driver, \$1199.

American Small Business Computers Inc, 327 S Mill St, Pryor, OK 74361. Phone (918) 825-4844. FAX (918) 825-6359.

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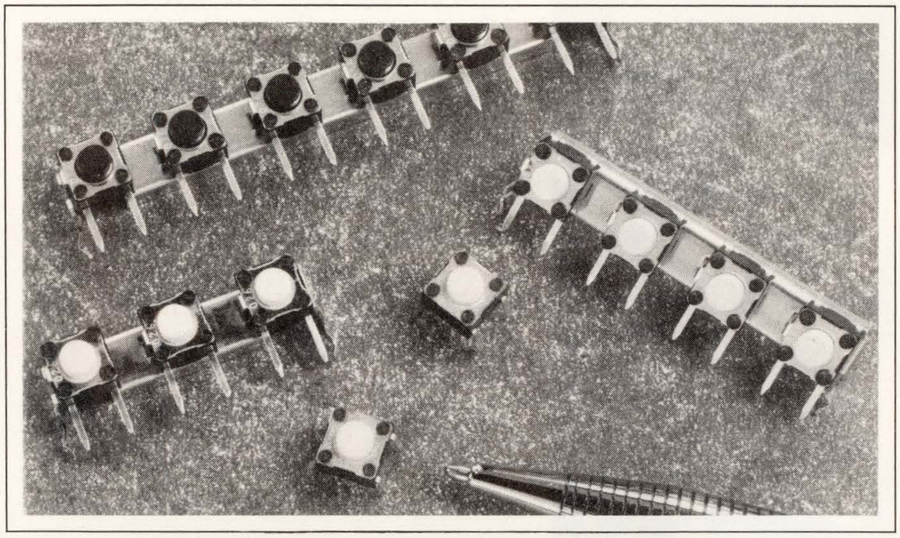
COMPONENTS & POWER SUPPLIES

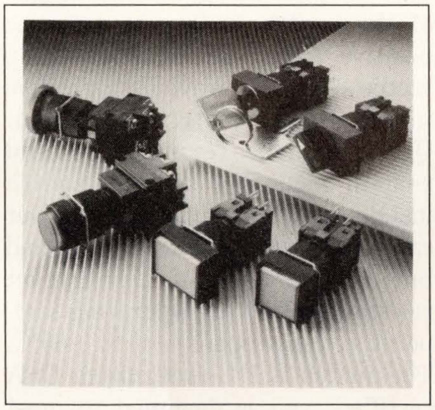
Low-Power Switches

- *Available in multiunit versions*
- *Have switch life of 100,000 operations min*

KS Series switches are available in individual (KSM) and multiunit (KSR) versions. The spst KSM units handle loads as high as 24V at 50 mA. Contact resistance measures 100 mΩ max, and switch life is 100,000 operations at rated load. Insulation resistance and dielectric strength equal 100V dc and 250V ac, respectively. KSR devices are available in 4-, 6-, and 14-switch blocks. Offered in spst and dpst configurations, the multiswitch units are rated for loads of 20V at 2 mA max. Insulation resistance and dielectric strength for these devices measure 100V dc and 150V ac, respectively. With a 5V/1A load, switch life for KSR devices equals 200,000 operations. Contact resistance measures 500 mΩ max. KSM versions, from $0.04 (OEM qty).



Hokuriku USA Ltd, 8145 River Dr, Morton Grove, IL 60053. Phone (708) 470-8440. **Circle No. 368**



Lighted Pushbutton Switches

- *Offer a choice of light sources*
- *Available with spdt or dpdt contact configurations*

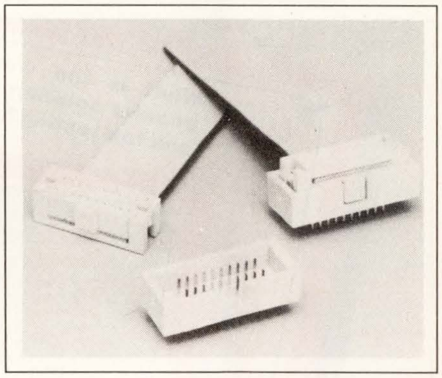
A3G LPB switches feature a snap-lock, socket-mount design that allows you to connect the actuator to the base easily. The units mount in 16-mm panel cutouts, have a 100,000-operation lifetime, and are available with spdt or dpdt contacts in momentary, alternating, or indicator versions. Pushbuttons and indicators are available in round, square, or rectangular styles with a choice of LED, incandescent, or neon light sources. General-purpose contacts are rated for 3A at 250V ac, 5A at 125V ac, or 3A at 30V dc. Ratings for low-level applications are 100 mA at 125V ac or 30V dc. The switches feature oil-resistant (IP65) service ratings. The line also includes nonlighted, selector switch, and key-type versions. Lighted switches, from $7.80; nonlighted models, from $5.90 (500).

Omron Electronics Inc, 1 E Commerce Dr, Schaumburg, IL 60173. Phone (708) 843-7900. FAX (708) 843-7787. **Circle No. 369**

IDC Sockets/Headers

- *Offer as many as 100 positions*
- *Rated for 5A at 30V*

The sockets in this line of IDC (insulation displacement connector) devices accept 0.025-in. pitch cable. The sockets and headers are available in sizes ranging from 10 to 100 positions and come with either straight or right-angle leads. The units accept #30 AWG pitch planar



cable and mate with 0.016-in. square pins. The socket and header combination is rated for 30V at 0.5A. The socket features a double-beam contact design. Contacts are phosphor bronze with 30 μin. of gold plating over 100 μin. tin. The glass-filled polyester insulators carry a 94V-0 UL flammability rating. $0.045 to $0.050 (1000) per position for sockets; $0.03 per pin for headers. Delivery, stock to six weeks ARO.

Carrot Components Corp, 4620 Calle Quetzal, Camarillo, CA 93012. Phone (805) 484-0540. FAX (805) 484-7458. **Circle No. 370**

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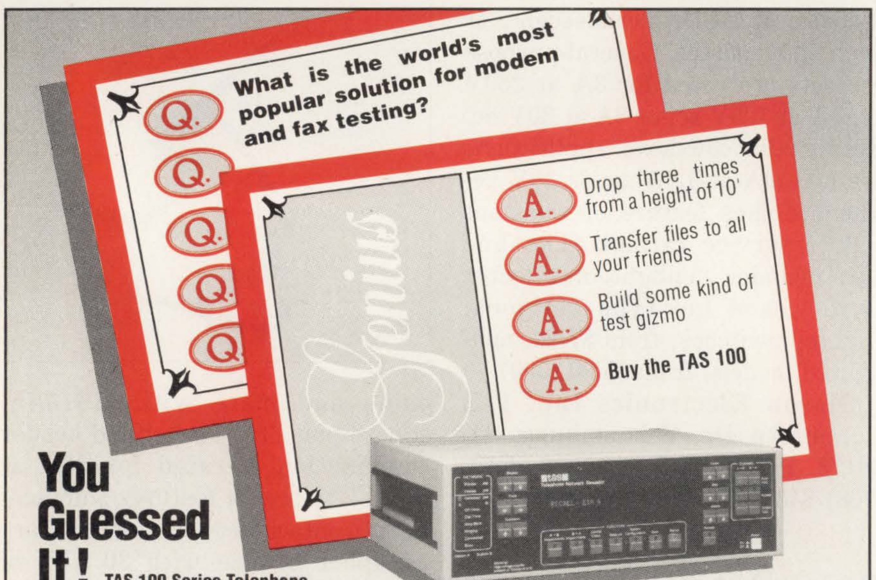
CIRCLE NO. 14



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CIRCLE NO. 15

COMPONENTS & POWER SUPPLIES

Rocker Switch

- *Handles 16A*
- *Provides tactile feedback*

STR Series 16A rocker switches are available in oval-shaped and rectangular versions. The units have tapered bezels and a recessed channel that extends along the full length of the rocker surface to promote positive finger positioning. Crisp tactile feedback provides a positive indication of switch activation. Quick-connect termination and snap-in mounting simplify switch installation. The devices have silver cadmium contacts. The housing and button are made of high-impact resistant polyester. Operating temperature range spans −40 to +65°C. The switch is UL recognized, CSA certified, and is designed to meet VDE standards. $0.57 (10,000). Delivery, 8 to 10 weeks ARO.

Micro Switch, 11 W Spring St, Freeport, IL 61032. Phone (815) 235-6600. **Circle No. 371**

Supertwisted LCD

- *Features a 640×400-pixel display area*
- *Has an 18-cd brightness*

The TLX-1641-G3B is a 640×400-pixel transmissive, electroluminescent-backlit, blue-mode supertwisted LCD. The unit features a 9.3-in.-diagonal screen, an outline di-

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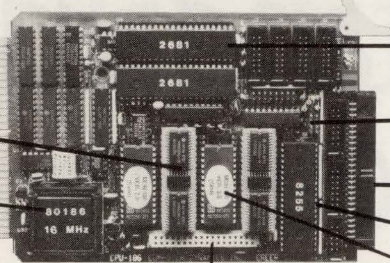

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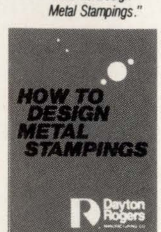

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CIRCLE NO. 17

mension of 256 × 146 × 10.5 mm, and an active area of 191.97 × 119.97 mm. Total weight of the display, including the electroluminescent backlighting, is 400g. Dot pitch and size measure 0.30 × 0.30 and 0.27 × 0.27, respectively. Typical contrast is approximately 5:1. At 2.7W, the display has an 18-cd/m^2 surface brightness. An integral 8-bit parallel interface is standard. $200 (10,000). Delivery, 12 weeks ARO.

Toshiba America Inc, 1 Pkwy N, Suite 500, Deerfield, IL 60015. Phone (708) 945-1500.

Circle No. 372

Cooling Fan

- *Features automatic speed control*
- *Reduces noise by 15 dB*

Smart Fan's self-contained electronics automatically controls its speed to regulate temperature in equipment enclosures against changes in room temperature, system power dissipation, flow resistance, and altitude. A self-contained thermistor senses the temperature changes, and proprietary control electronics adjusts the airflow to maintain a constant temperature once the system temperature exceeds a preset minimum level. This scheme protects critical components against temperature-related failure and reduces the overall noise by 15 dBA. The fans are available with an internal alarm, which activates when temperatures exceed the norm by 10°C, or when there is a loss of cooling-system power. The fans are offered in a variety of popular sizes including 4.7 × 4.7 × 1.5, 3.6 × 3.6 × 1, and 4.7 × 4.7 × 1 in. $15 (5000).

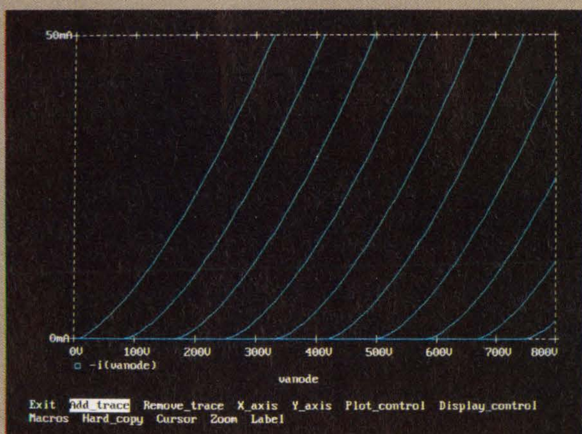
NMB Technologies Inc, 9730 Independence Ave, Chatsworth, CA 91311. Phone (818) 341-3355. FAX (818) 341-8207. TLX 651340.

Circle No. 373

PSpice

MicroSim Corporation

The Standard for Circuit Simulation



I-V curves of a triode vacuum tube

Analog Behavioral Modeling

The Analog Behavioral Modeling option for the PSpice Circuit Analysis package allows you to describe analog components, or entire circuit blocks, using a formula or look-up table. Linear blocks may be described using either a Laplace transform or a frequency response table. Once defined, you can use these blocks in all PSpice analyses, including DC, AC, and transient.

Modeling entire blocks of circuitry is a powerful aid in designing a system from the top down. You can describe a functional block by its behavior without worrying about how that function will be implemented. Later on in the design process, you can replace the block with the actual circuitry.

Another application is the modeling of electronic components which are not built into PSpice. The photo shows an example of simulating the DC characteristics of a 3/2-power-law device.

Since its introduction over six years ago, MicroSim's PSpice has sold more copies than all other SPICE-based programs combined. PSpice provides broad capabilities, accurate results, diverse options, and availability across a wide range of computer platforms. PSpice includes an extensive device library of 3,000+ analog parts and 1,300+ digital parts, at no extra charge.

Besides Analog Behavioral Modeling, PSpice provides the following options:

Digital Simulation: simulation of mixed analog/digital circuits with feedback between the analog and digital sections.

Monte Carlo Analysis: calculates the variations in a circuit's performance allowing for component tolerances. This option performs statistical analyses: Monte Carlo, Sensitivity, and Worst Case.

Probe: acts as a "software oscilloscope" to provide an interactive viewing and processing environment for simulation results (see photo).

Parts: is a parameter extraction program allowing the extraction of device model parameters from data sheet information.

PSpice is available on the PC (running DOS, Protected Mode DOS, or OS/2), Macintosh II , Sun 3, Sun 4, and SPARCstation, DECstation 2100, 3100, and 5000, and the VAX/VMS families.

In addition to the Circuit Analysis package, the PSpice family of products also contains the Circuit Synthesis package, which consists of our two filter synthesis products: Advanced Filter Designer and Standard Filter Designer. Filter Designer is an interactive design aid for synthesizing and analyzing active filters. Features include:

- Analysis of low pass, high pass, band pass, and band reject filter types.
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- Capability to synthesize arbitrary transfer functions and delay equalization filters (only available in Advanced Filter Designer).

Each copy of our Circuit Analysis and Circuit Synthesis programs comes with MicroSim's extensive product support. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022 or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

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CIRCLE NO. 85

Recording the Past...
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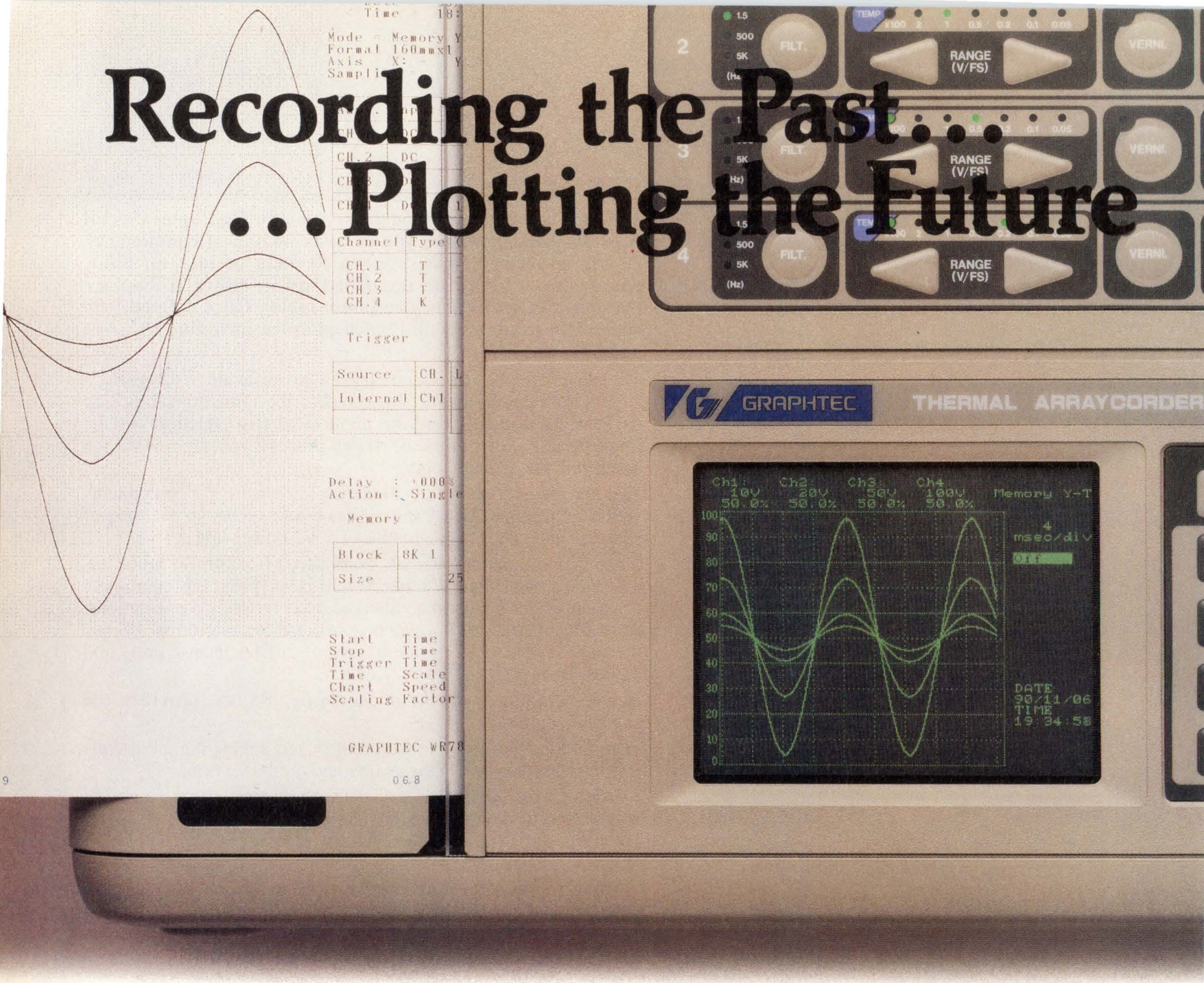

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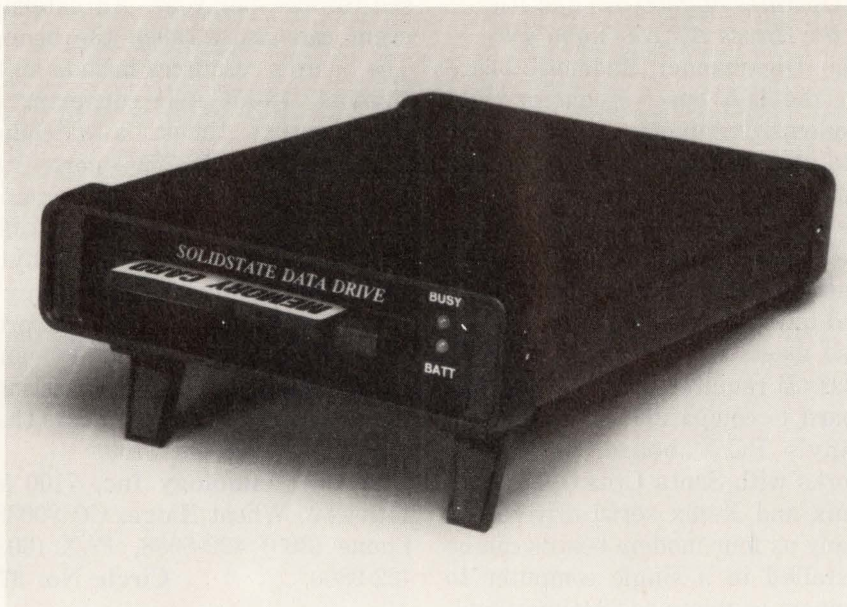


Solid-State Drive

- *Transfers data between memory cards and desktop computers*
- *Drives interface with RS-232C and parallel ports*

The family of Solidstate data drives can transfer data between memory cards used in notebook computers and desktop computers. Because the drives have either an RS-232C port, a parallel port, or a floppy-disk controller interface, virtually any desktop computer can access data on the memory cards. Memory cards are more reliable than floppy disks for two reasons: They don't require read-write heads that can crash, and they are less susceptible to shock and magnetic fields. Device drivers are available for MS-DOS-compatible computers. Drive with RS-232C port, $350; drive with parallel port, $350; internal drive with floppy-disk-drive interface, $295.

Adtron Corp, Box 1848, Gilbert, AZ 85234. Phone (602) 961-7511.

Circle No. 374

Sbus Expansion Boards

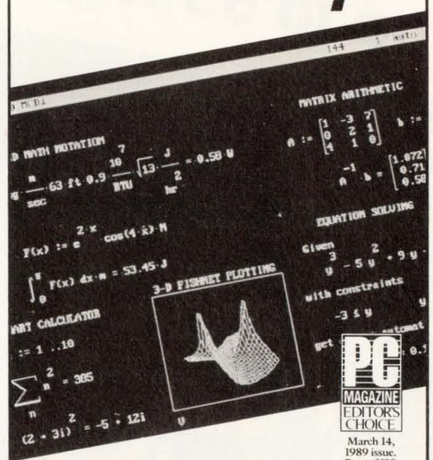
- *Consist of a SCSI host adapter and communication board*
- *Communications board has one parallel and eight serial ports*

Two Sbus expansion boards are available for the company's desktop SPARC workstations. The serial parallel controller, a communications board, has eight serial ports and one parallel port. You can install three boards in a SPARCstation 1/1+ to connect as many as 18 asynchronous devices such as modems, printers, and terminals. Each port on the card can transfer data at 38.4k baud. A SCSI host adapter connects as many as seven SCSI devices to the workstation. The board can transfer data at 5M bytes/sec and divides heavy disk traffic between two SCSI channels. It supports disk drives with as much as 2.6G bytes of storage. Serial parallel controller, $1095; SCSI host adapter, $495.

Sun Microsystems Inc, 2550 Garcia Ave, Mountain View, CA 94043. Phone (415) 960-1300. FAX (415) 969-9131.

Circle No. 375

Technical calculations made easy!



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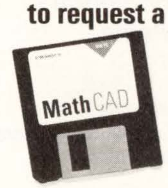

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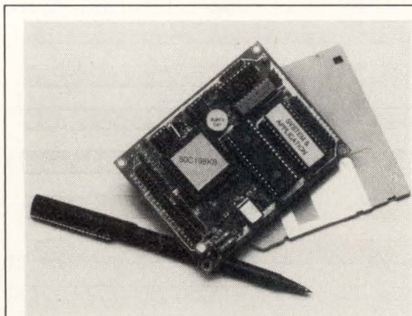
CIRCLE NO. 19

Modem Board

- *Has as many as eight modems on one ISA bus board*
- *Operates at 2400 bps and uses the Hayes AT command set*

The Digichannel Modem/X board for the ISA bus has four or eight modems. It can operate at 2400 bps and utilizes the Hayes AT command set. The modem conforms to the Bell 103, Bell 212A, CCITT V.22, and CCITT V.22 bis specifications. Besides providing autoanswering and tone or pulse dialing, the board also meets FCC Part 68 and FCC Class B requirements. Because the board is compatible with the company's PC/X board, the board works with Santa Cruz Operation's Unix and Xenix serial drivers. As many as four modem boards can be installed in a single computer to support as many as 32 users simultaneously. You can also configure the board's address and interrupt requests in software. 4-modem board, $1195; 8-modem board, $1995.

Digiboard, 6751 Oxford St, Minneapolis, MN 55426. Phone (612) 922-8055. **Circle No. 376**



Single-Board Computer

- *Measures 3×4 in.*
- *Uses 80C196KB μP and runs Forth programs*

The SBC196 single-board computer for embedded applications uses a 12-MHz 80C196KB or 80C196KC μP and measures 3×4 in. It runs from a single 5V supply and draws 80 mA while operating, 20 mA while idling, and <1 mA in a sleep mode. A real-time clock can awaken the board from the sleep mode at intervals varying from 100 times/sec to once per year. An external event can also awaken the board. The board's resources include an 8-channel, 10-bit A/D converter; a PWM output; timers; a watchdog timer; and an RS-232C port. You can use the serial port to communicate with an IBM PC-compatible computer. An onboard 32k-byte EPROM contains the company's version of Forth, F83+. You prepare source code on the PC and download it to the board for testing. The board has two serial buses that connect peripherals. $169.

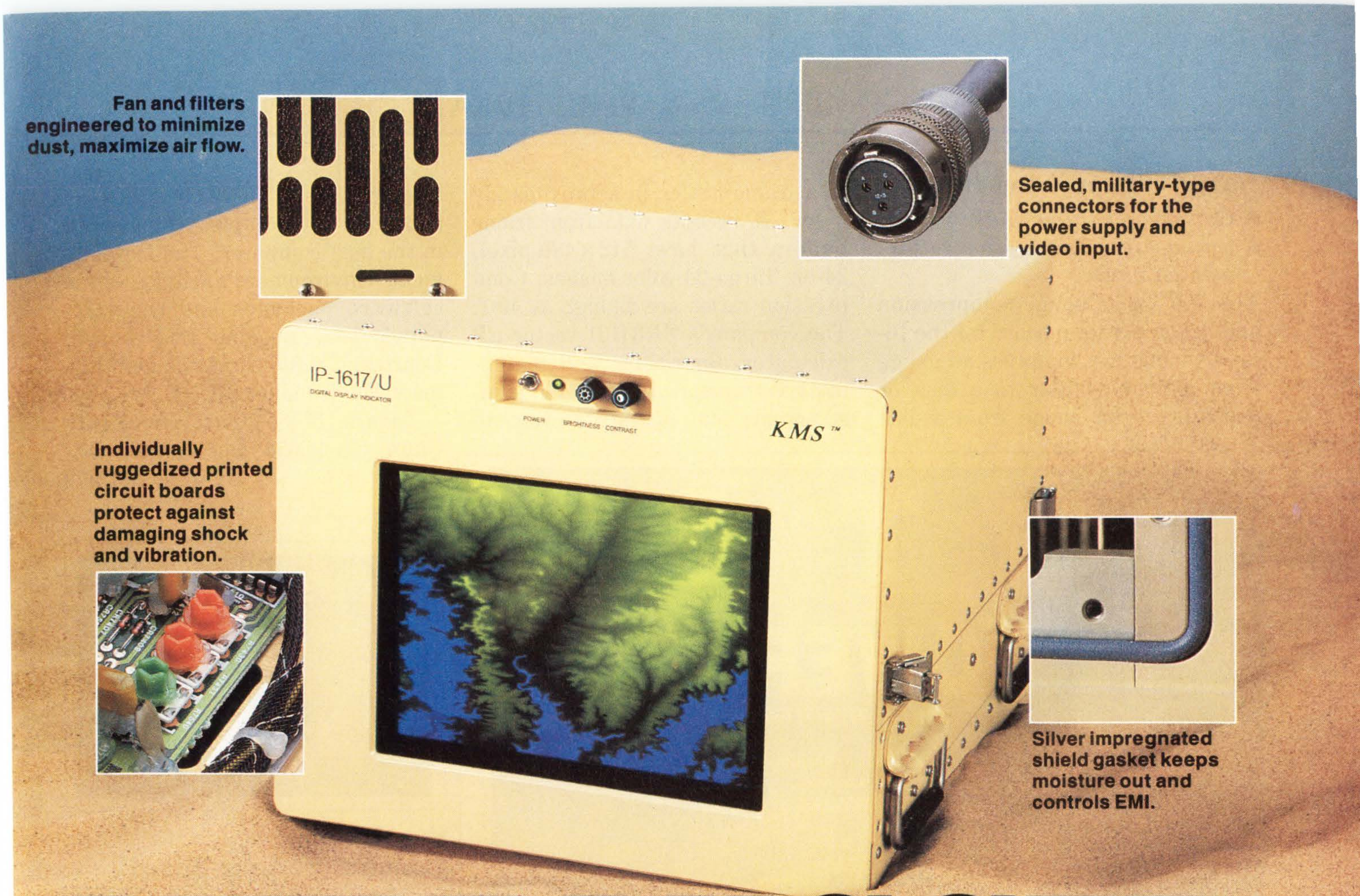
Vesta Technology Inc, 7100 W 44th Ave, Wheat Ridge, CO 80033. Phone (303) 422-8088. FAX (303) 422-9800. **Circle No. 377**

SPARC Workstation

- *Runs at 40 MHz and has 16M bytes of RAM*
- *Has three Sbus slots and Ethernet port*

The SPARCstation 2 family of workstations uses a 40-MHz CMOS SPARC integer and floating-point processor. The system's CPU board also contains a SCSI controller; an Ethernet controller; 16M bytes of memory expandable to 96M bytes; an audio port; and two serial ports. The system achieves 21 Specmarks, which is a figure that represents the geometric mean of 10 benchmark tests. The system runs the SunOS operating system and supports the following network protocols: NFS, TCP/IP, PC-NFS, and TOPS. Features include three Sbus expansion slots; a 3½-in., 1.44M-byte floppy-disk drive; and support for an internal 414M-byte drive. You can also attach an external drive for a total capacity of 7.6G bytes. A GS and a GT model has 3D color graphics. $14,995.

Sun Microsystems Inc, 2550 Garcia Ave, Mountain View, CA 94043. Phone (415) 960-1300. FAX 969-9131. **Circle No. 378**



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700 KMS Place, Ann Arbor, MI 48106-1868 FAX: 313/769-8660

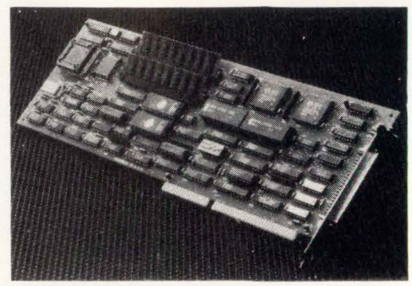
Image-Compression Board

- *Compresses frame-buffer images*
- *Can achieve compression ratios as high as 40:1*

The ZR73660 image-compression and decompression board for the 16-bit ISA bus can compress an image from a frame buffer to a disk or decompress an image from a disk to a frame buffer in approximately 3 sec. It accepts data from frame buffers that have 512×480-pixel, 24-bit Targa-24 color images. Compression ratios are as high as 40:1. The company's ZR34161 vector μP calculates algorithms and mathematical transforms, using single instructions that operate on the entire data set. The board has an 80286 μP and occupies a single slot in the host computer. The Development Environment includes three software packages and the company's Imagineering DSP board. Board and software, $875; Development Environment, $4500.

Zoran, 1705 Wyatt Dr, Santa Clara, CA 95054. Phone (408) 986-1314. **Circle No. 379**

CIRCLE NO. 26



Synchronous Communications Board

- *Has 80376 μP and DMA*
- *Two 16C30 multiprotocol chips control four serial ports*

A synchronous communications board is available for the 16-bit ISA bus. It uses Intel's 80376 μP, a member of the 80386 μP family for embedded control. The 16-MHz μP relieves the host of synchronous-protocol overhead and communications tasks. The μP has use of 256k bytes of dual-ported RAM, 512k or 2M bytes of local RAM, and from 32k to 128k bytes of EPROM. An Intel 82370 chip provides DMA for the serial communications channels. Two Zilog 16C30 multiprotocol controller chips control full-duplex data transfers at 10M bps for each of the four synchronous serial ports. An X.25 software package, which allows a Unix system to operate as a LAN server, is also available. Board, $1800; board and X.25 software, $2495.

Star Gate Technologies Inc, 29300 Aurora Rd, Solon, OH 44139. Phone (800) 782-7428; in OH, (216) 349-1860. FAX (216) 349-2056.

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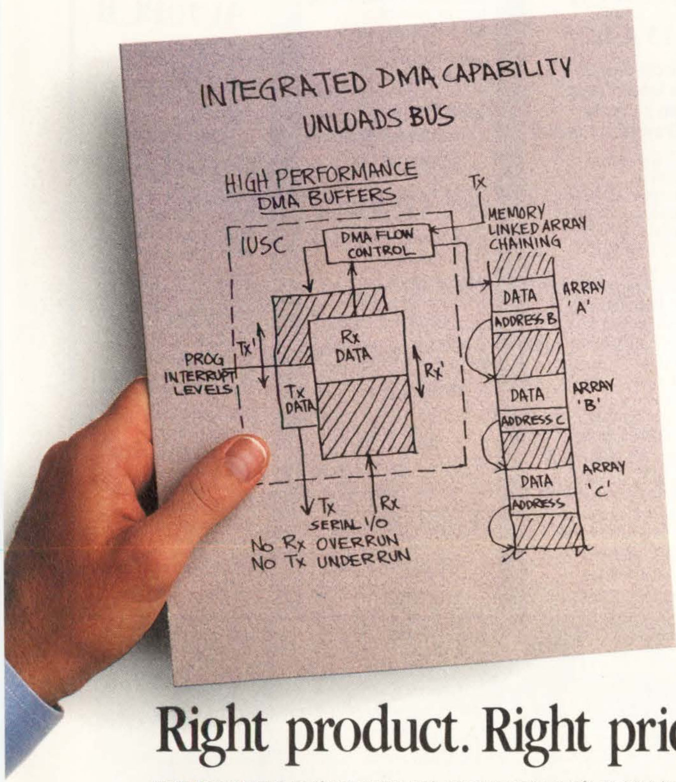

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Zilog's USC cell gives you 10 Mbits/sec speed for multi-protocol operation. It also gives you 32-byte RX and TX FIFOs for improved latency and up to 32-byte block moves. There's a Time Slot Assigner for multiplexing in ISDN/T1 applications, a flexible 16-bit bus interface — multiplexed or non-multiplexed — for easy CPU interconnect, and a daisy-chain interrupt structure for simpler interrupt handling. And, best of all, the USC can reduce the CPU workload as much as *60%*.

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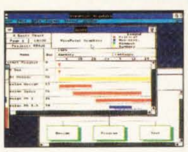

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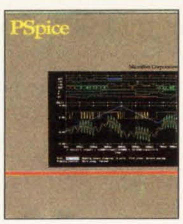

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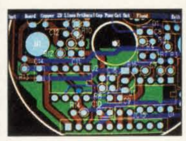

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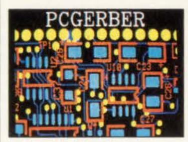

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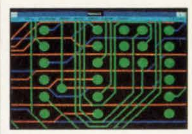

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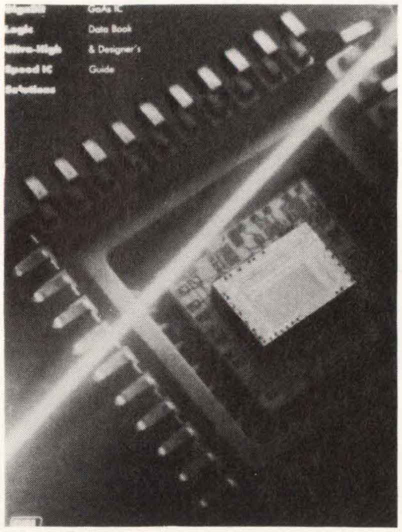

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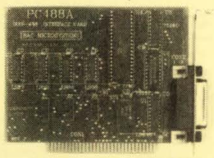

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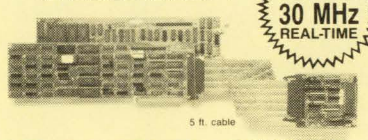

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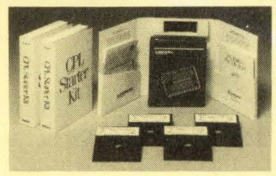

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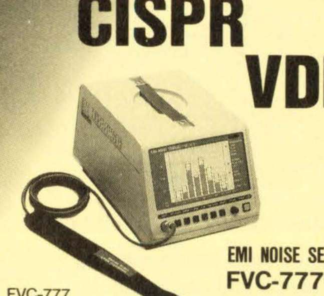

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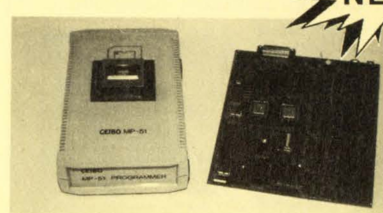

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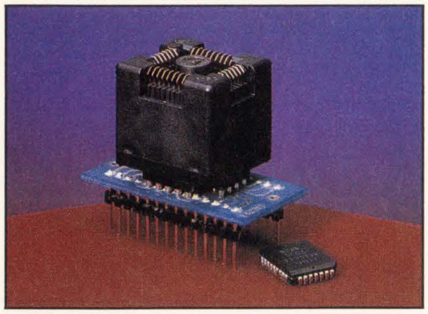

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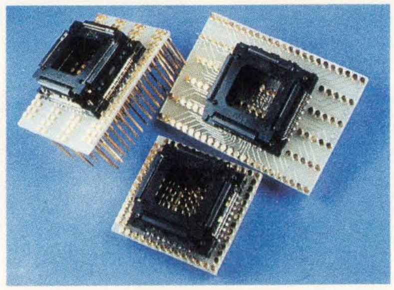

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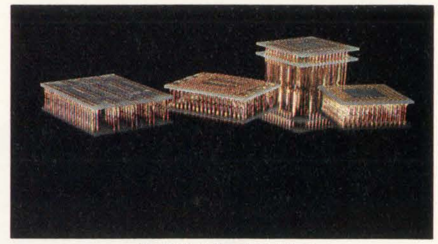

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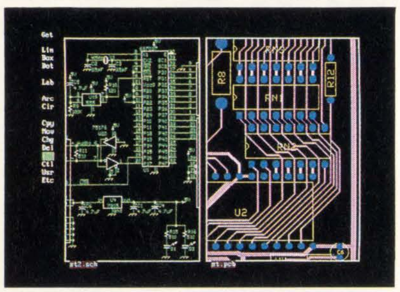

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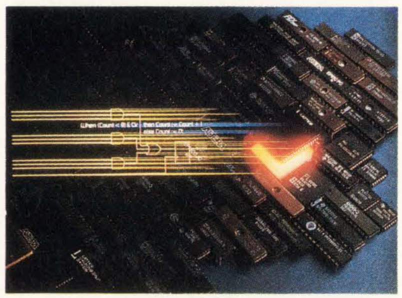

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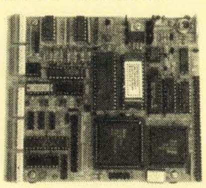

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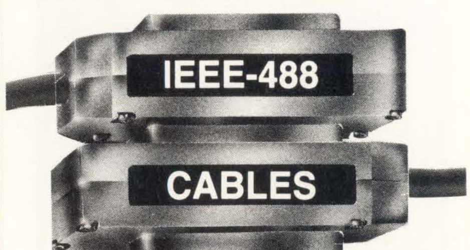

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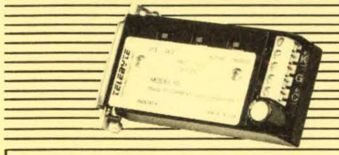

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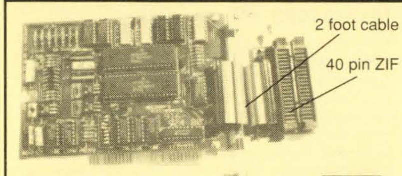

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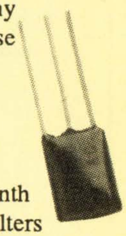

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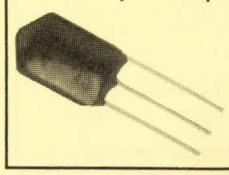

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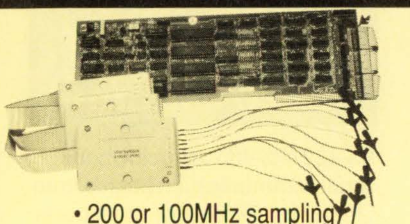

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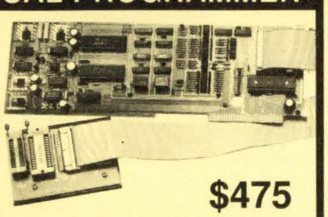

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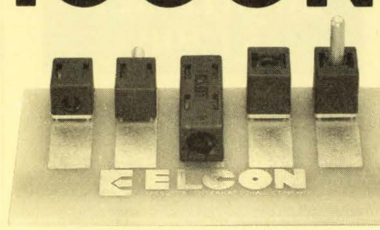

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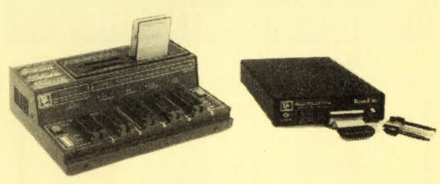

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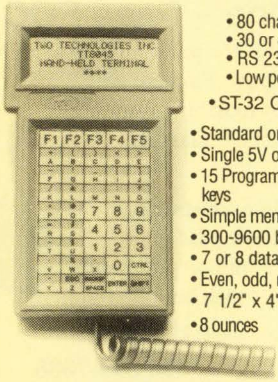

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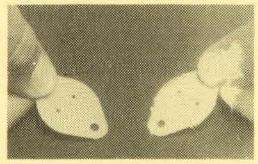

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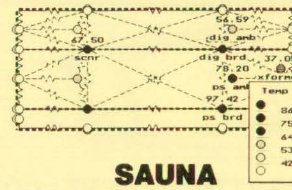

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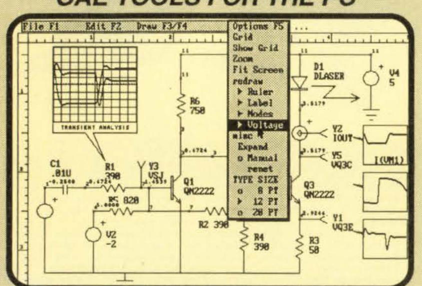

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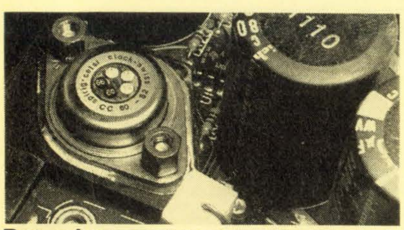

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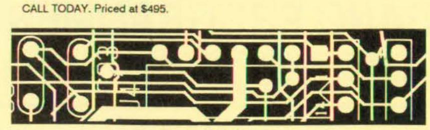

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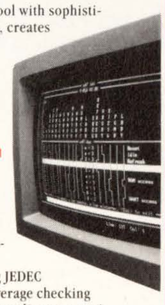

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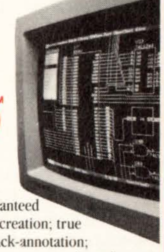

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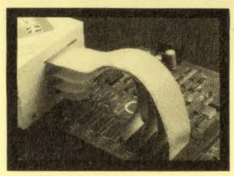

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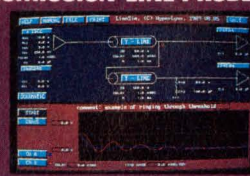

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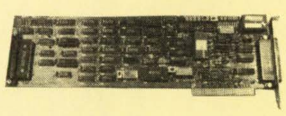

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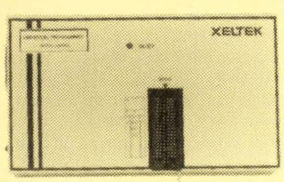

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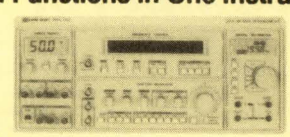

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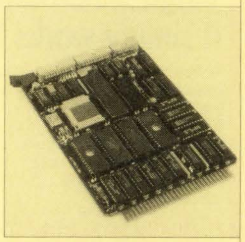

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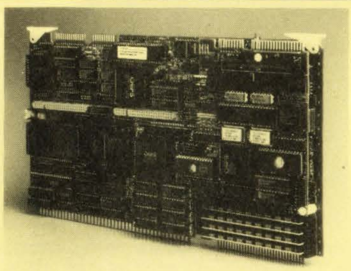

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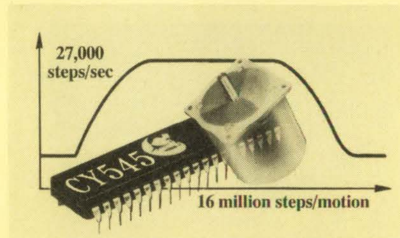

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Issue	Issue Date	Ad Deadline	Editorial Emphasis
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News Edition	Mar. 7	Feb. 14	Special Supplement: State of Engineering • Medical Electronics**
Magazine Edition	Mar. 14	Feb. 21	Software Tools, Computer Architectures, Materials Technology, ICs & Semiconductors/Instrumentation Circuits
Magazine Edition	Mar. 14	Feb. 21	Software Engineering Special Issue, (To be polybagged with the March 14th Magazine Edition issue)
News Edition	Mar. 21	Mar. 1	CAE, Computer Buses**, Regional Profile: Alabama, Georgia, N. Carolina**
Magazine Edition	Mar. 28	Mar. 7	ICs & Semiconductors/ Microprocessors, Software • CAE • Computer Boards, Electro Preview Issue
News Edition	Apr. 4	Mar. 15	Optical Interconnects, Automotive Electronics**, Electro Show Issue
Magazine Edition	Apr. 11	Mar. 21	Power Sources, CAE/ASICs, Test & Measurement, Sensors, Electro Show Issue
News Edition	Apr. 18	Mar. 29	Distribution, Optics**, Regional Profile: No. California**
Magazine Edition	Apr. 25	Apr. 4	Computers & Peripherals Special Issue, Computers & Peripherals/ Memory Design, Data Storage Technology, ICs & Semiconductors, ASICs
News Edition	May 2	Apr. 11	Automotive Electronics, ASICs**
Magazine Edition	May 9	Apr. 17	Analog Technology Special Issue, ICs & Semiconductors, Test & Measurement, CAE, Power Sources
News Edition	May 16	Apr. 26	ICs & Semiconductors, Telecommunications**, Regional Profile: Texas & Oklahoma**
Magazine Edition	May 23	May 2	ICs & Semiconductors, High Speed Memories • Computers & Peripherals, Graphics ICs, Packaging •
Magazine Edition	June 6	May 15	CAE • Software • Digital/Analog CAE • Time Analysis, ASICs
News Edition	June 13	May 23	Special Supplement: Electronic Design Automation (EDA) • CASE/CAE**
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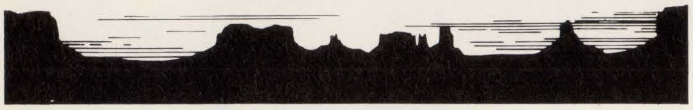

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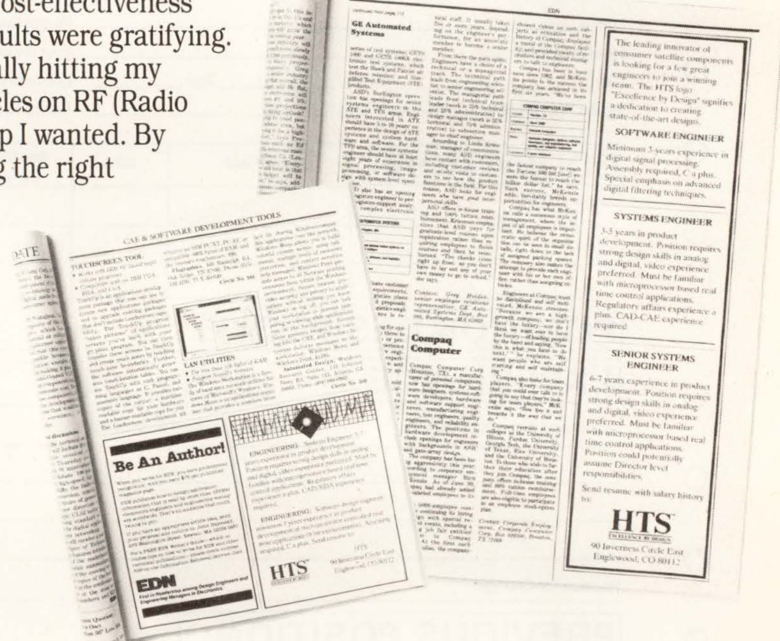

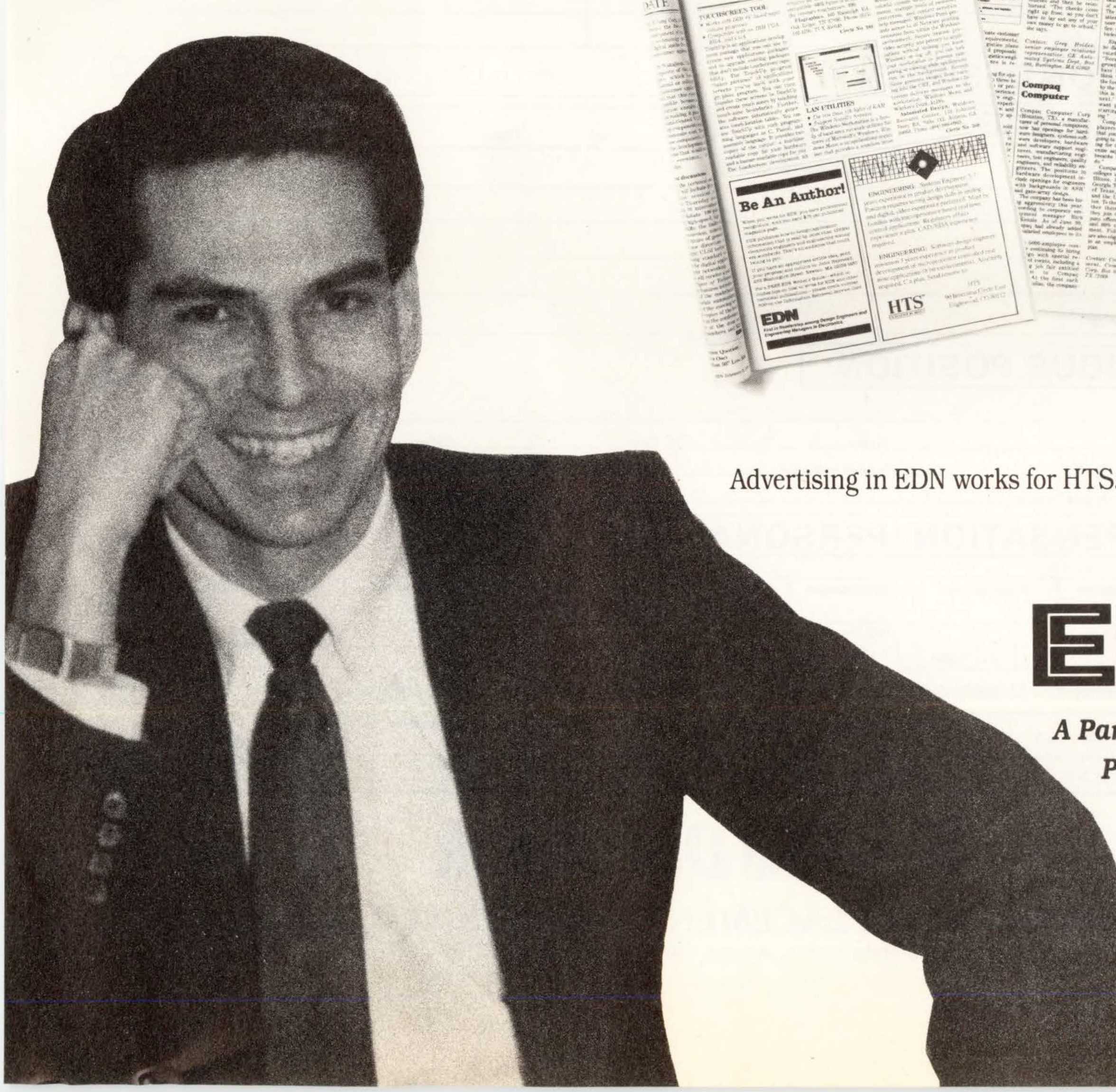

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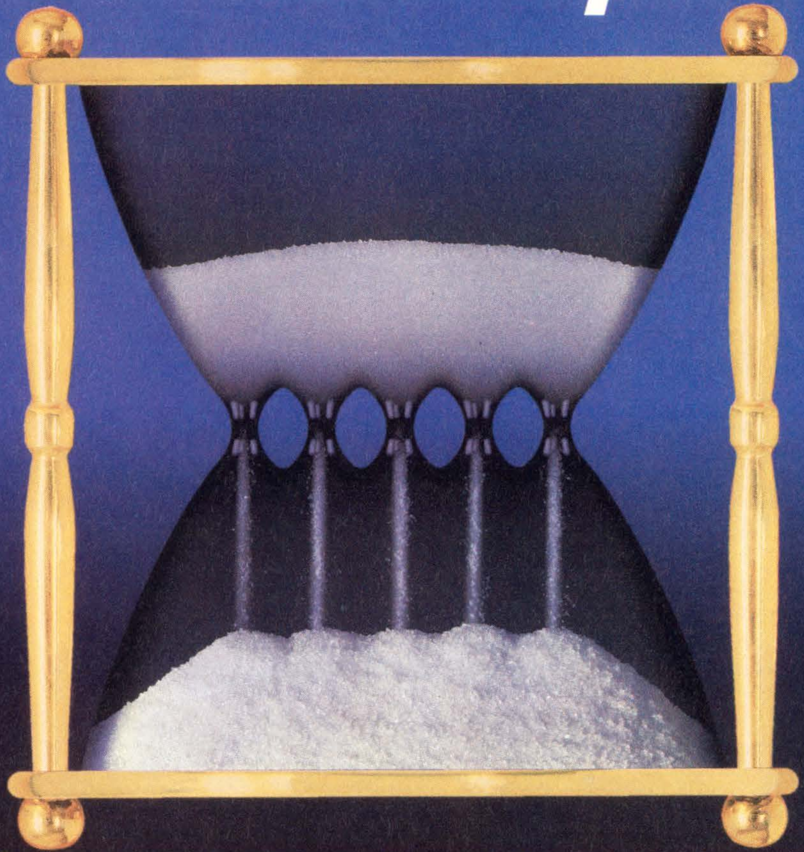

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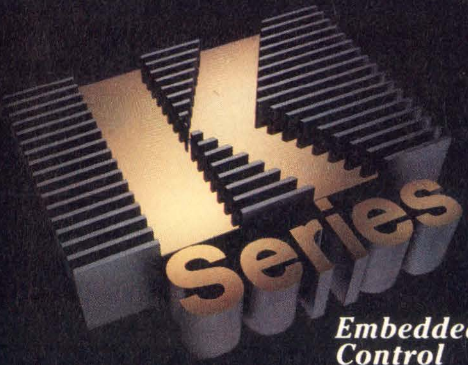

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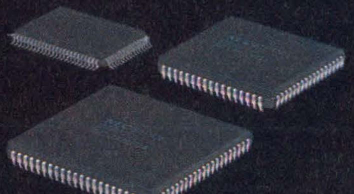

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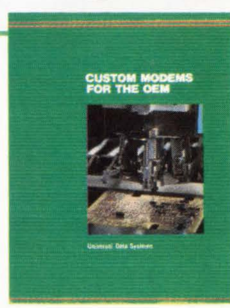

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