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FEBRUARY 4, 1988

EDN

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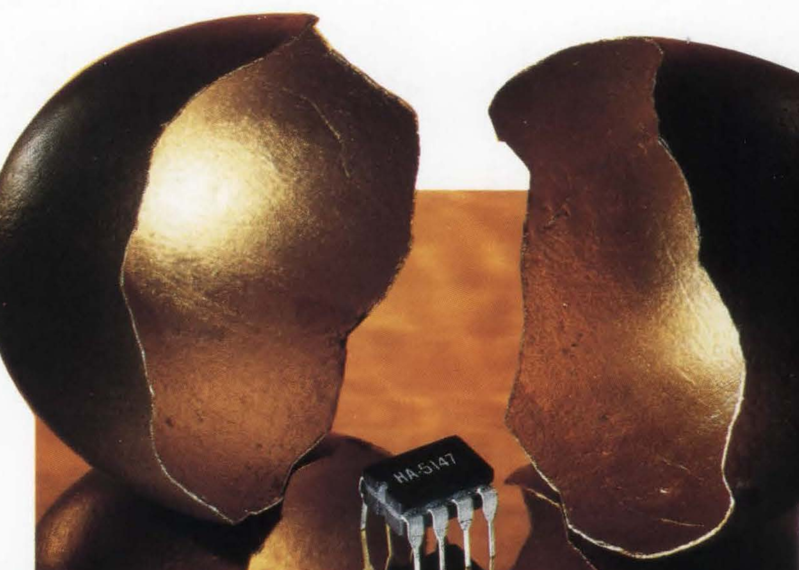

For free on-line information on the Harris HA-5147, call 1-800-345-7335 with any ASCII terminal or PC and 300 or 1200-baud modem (even parity, 7 data bits, 1 stop bit). Enter response code HA5147 (CR). In Connecticut, dial (203) 852-9201.

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The SCM-1 spans 1 to 500MHz with only 6.0dB conversion loss, 45dB LO-RF isolation, and 40dB LO-IF isolation. Housed in a rugged, non-hermetic 0.4 by 0.8 by 0.3 in. high (maximum dimensions) plastic/ceramic package. Spacing between connections is 0.2 in. The mixer is offered with leads (SCM-IL) or without leads (SCM-INL) to meet a wide range of pc board mounting configurations.

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When you think SMT for low-cost production, think of Mini-Circuits' low-cost SCM mixers.

SPECIFICATIONS (typical)	SCM-1L (with leads)	SCM-1NL (no leads)
FREQ. RANGE (MHz)		
LO, RF	1-500	
IF	DC-500	
CONVERSION LOSS (dB)		
Mid-Band (10-250MHz)	6.3	
Total Range (1-500)	7.5	
ISOLATION (dB)	(L-R)	(L-I)
Low-Band (1-10MHz)	60	45
Mid-Band (10-250MHz)	45	40
High-Band (250-500MHz)	40	35
PRICE	$2.49 (1,000 qty) $3.75 (10-49)	

Units are shipped in anti-static plastic "tubes" or "sticks" for automatic insertion.

CIRCLE NO 83

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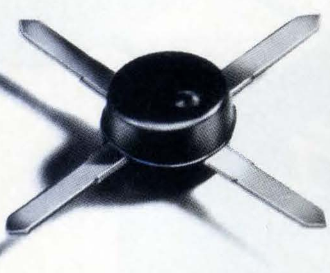
from 99¢



dc to 2000 MHz amplifier series

SPECIFICATIONS

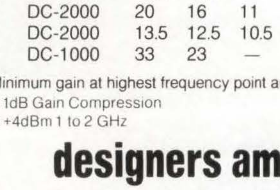
MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.
- • 1dB Gain Compression
- □ +4dBm 1 to 2 GHz

designers amplifier kit, DAK-2

5 of each model, total 35 amplifiers

only $59.95



Unbelievable, until now... tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 470, 680, 100 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047, .068, .1μf

† Minimum Order 50 per Value

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CIRCLE NO 107

C113-Rev. D

Volume 33, Number 3

EDN

February 4, 1988

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *Digital-ASIC simulation packages keep chip designs on course. See pg 118. (Photo courtesy Ikos Systems)*

DESIGN FEATURES

Continued on page 7

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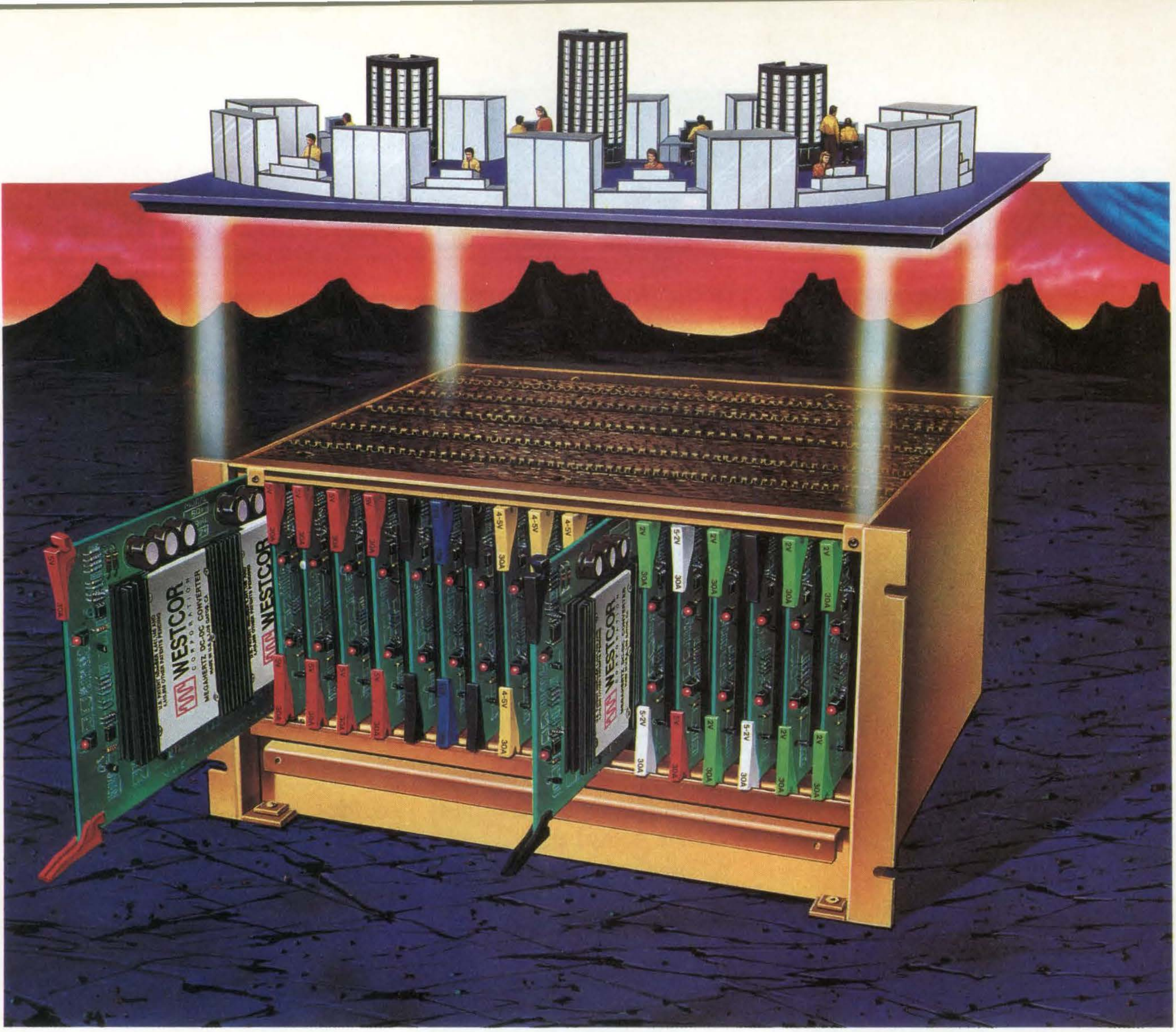

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Low profile (.8″) PowerCards supply single outputs from 2 to 75 VDC at up to 400 watts (outputs from 2 to 5 VDC limited to 60 amperes). Dual output cards source two isolated outputs each at half of the above ratings. Single output cards can be paralleled with current sharing to provide kilowatts via simple backplane configuration.

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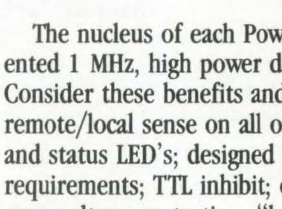

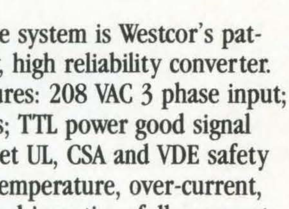

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Continued from page 5

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Continued on page 9

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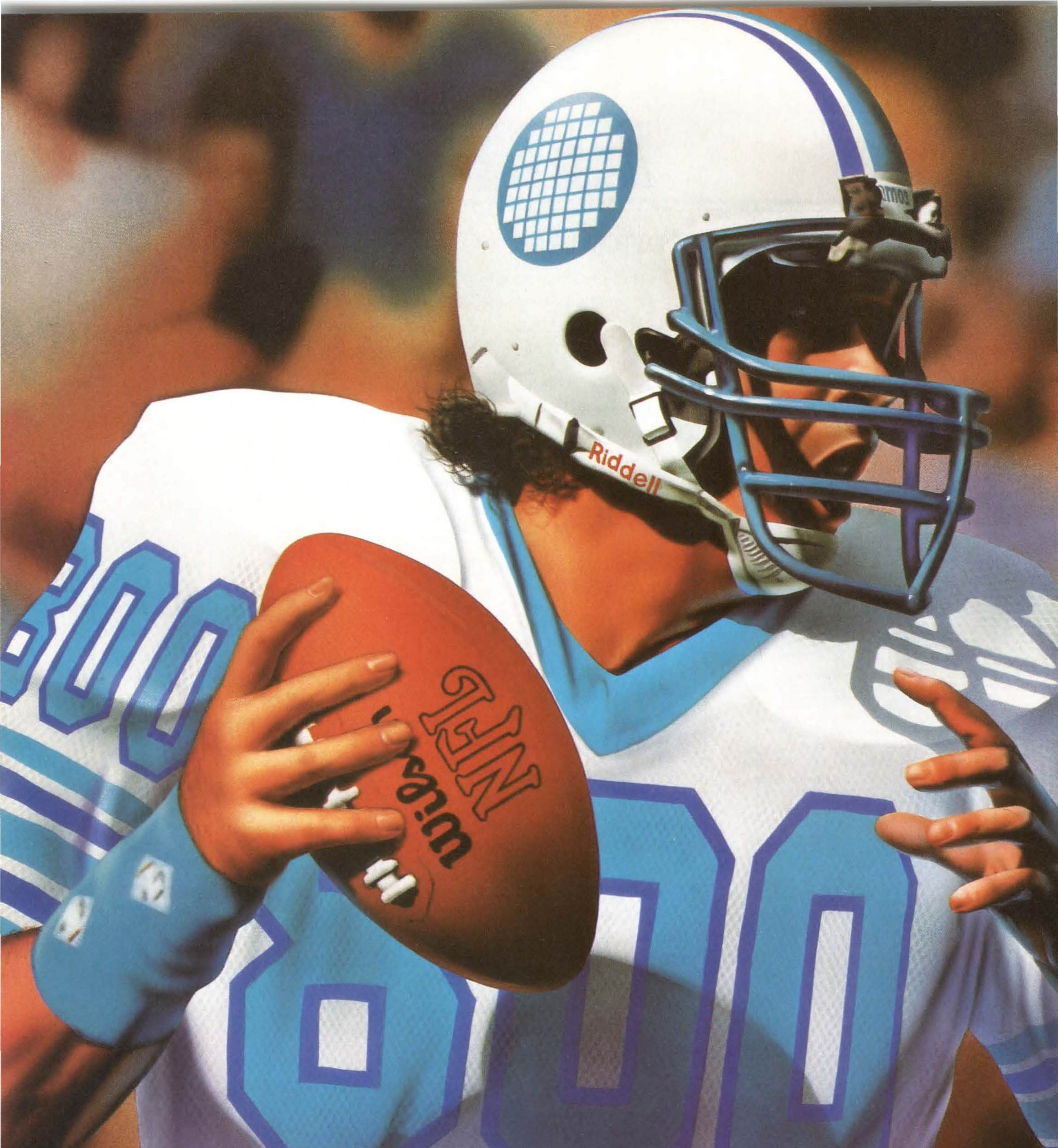
Continued from page 7



SINGLE PRECISION WHETSTONE LEAGUE

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1.8 MEGAWHETSTONES.

INMOS.
IMS T800 TRANSPUTER.
4.6 MEGAWHETSTONES.

MOTOROLA.
68020/68881 20 MHz
1.5 MEGAWHETSTONES.

DEC.
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DOUBLE PRECISION WHETSTONE LEAGUE

ONE T800 TRANSPUTER GIVES
2.5 DOUBLE PRECISION
MEGAWHETSTONES...
SO WHEN IT COMES TO
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INMOS T800 CHIPS COULD
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RATED AT 16.1 MEGAWHETSTONES
A REAL RUN FOR ITS MONEY!

MORE MULTIPROCESSOR MUSCLE. MORE RAW PERFORMANCE.

When you're out in the trenches fighting it out with ordinary microprocessors, running out of muscle is all too easy. That's why you should look to the new T800 Transputer from INMOS.

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32-bit enhanced RISC processor...64-bit on-chip IEEE floating-point processor...4K Bytes on-chip 50ns static RAM...Four 20 MBits/sec interprocessor communication links...Eight independent DMA engines. All on a single chip capable of sustained 1.5 MFLOPS...and 4.6M Whetstones!

And, if that's not enough raw power, the T800's links allow multiprocessor systems to be constructed quickly and easily – giving you 6 MFLOPS with four T800's...30 MFLOPS with 20...150 MFLOPS with 100...In fact, there's no limit to the number of Transputers you can use!

Programming Transputers couldn't be easier, with compilers for C, Fortran and Pascal, and the world's first concurrent programming language OCCAM.

Want to turbocharge your current system? No problem. Our exclusive Link Adaptor IC's allow Transputers to be connected to other microprocessors or peripherals.

Other team members include the pin compatible T414 Transputer, offering lower cost, 10 MIP performance and 0.75M Whetstones. Lined-up to provide all the I/O processing you need, the T212 16-bit Transputer is the ideal high performance controller and the M212 Disk Processor combines disk controller hardware and a Transputer on a single chip, supporting both Winchester and floppy disks. And the C004 Link Switch makes the design of software reconfigurable multiprocessor systems as easy as kicking an extra point.

Whatever field you're in – from real-time distributed systems to high-performance graphics, from fault-tolerant systems to robotics, Transputer technology can give you scalable performance at a cost you can afford.

Transputers are manufactured using an advanced 1.5 micron CMOS process which keeps the power consumption under one watt. So your system stays cool while under fire.

Transputers to MIL-STD 883C will be available in the first half of 1988.

If this all sounds like your kind of game, put the ball in play by contacting your local INMOS sales office today. And get ready to score.

DESCRIPTION			PERFORMANCE		AVAILABILITY		PACKAGE
Part No.	Word Length	Clock MHz	Integer Drystones	Floating Point Whetstones	Commercial	Military	
IMS T800-20	32-Bit	20	9500	4.6 Million	Now	Q2 88	84 PGA
IMS T414-20	32-Bit	20	9500	0.75 Million	Now	Q2 88	84 PGA
IMS T212-17	16-Bit	17	8000	–	Now	Q2 88	68 PGA
IMS T212-20	16-Bit	20	9500	–	Now	Q2 88	68 PGA
IMS M212-17	16-Bit	17	8000	–	Now	–	68 PGA

NETWORK SUPPORT PRODUCTS			AVAILABILITY		PACKAGE
Part No.	Description	Communication Speed	Commercial	Military	
IMS C004	Software configurable 32 way link switch	10 + 20 MBits/sec	Now	Q2 88	84 PGA
IMS C011	Link to system bus	10 + 20 MBits/sec	Now	–	24 Pin DIP
IMS C012	Link to system bus	10 + 20 MBits/Sec	Now	Q2 88	24 Pin DIP

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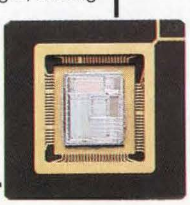

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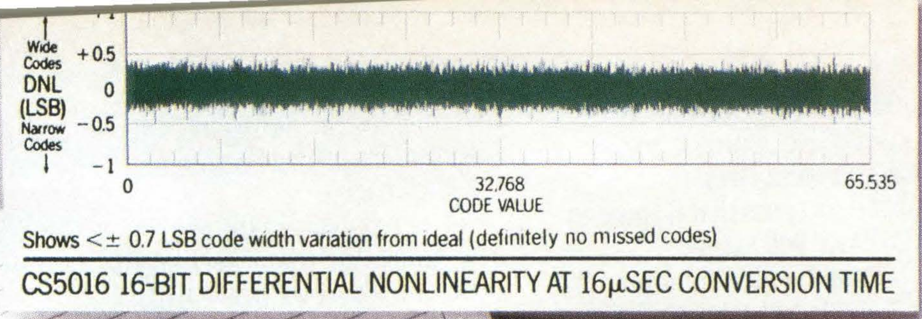

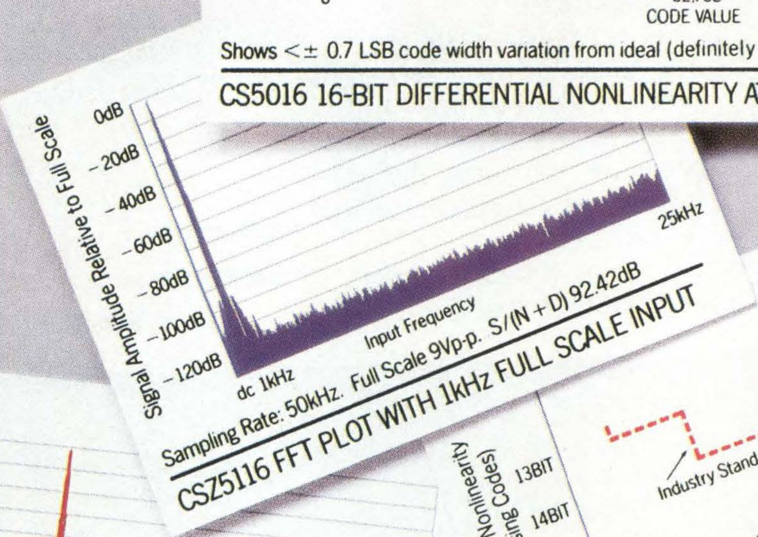

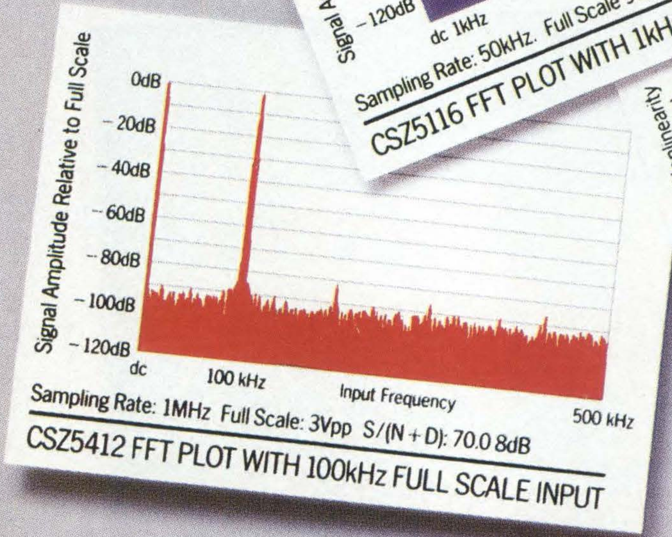

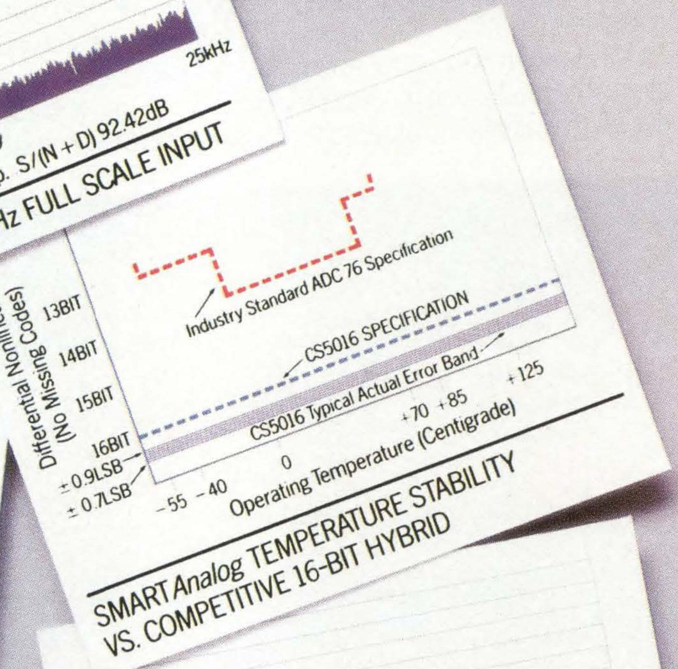

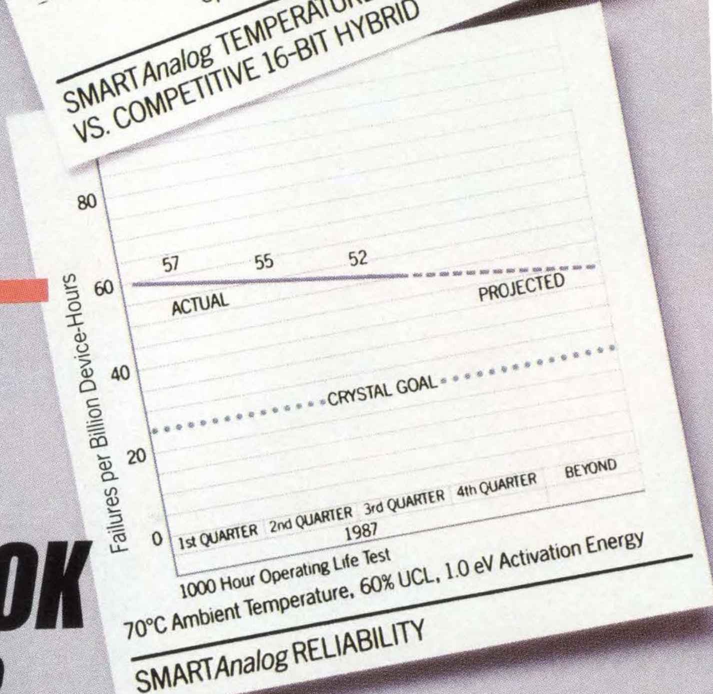

OUR 12-TO 16-BIT CMOS A/D CONVERTERS LOOK GREAT ON PAPER.

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Anyone can promise the world's best performance from monolithic CMOS A/D converters. Only Crystal can prove it.

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Dynamic performance really is 92 dB SNR over a 25 kHz bandwidth, or 70 dB over 500 kHz.

Differential Non-Linearity of 16 bits with no missing codes is so outstanding we've published a DNL plot no one else dares to.

Stability over temperature is dramatically better than the competition across the entire military range.

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What the plots don't show, you already know: monolithic A/D converters using CMOS technology mean lower design and assembly costs, higher reliability, lower power consumption, easier manufacturing and faster deliveries than hybrid or discrete designs can manage.

And our SMART*Analog* devices are the first with self-calibration at any time/temperature. Which ensures accuracy throughout their operating lives, correcting for gain, offset and even linearity errors. Automatically.

If that weren't enough, Crystal's SMART*Analog* line is the first line of 12- to 16-bit A/D converters with the converter, track/hold, digital interface, calibration circuitry and timing all on a single chip. So you can forget designing, building and characterizing discrete devices while trying to correlate component specifications with system requirements.

Prove to yourself how our revolutionary SMART*Analog* technology makes hybrids a very expensive proposition, indeed. Call 512-445-7222 today for your very own 12-, 14- or 16-bit evaluation board. Or ask for a demonstration at your facility.

Either way, you'll know why seeing a SMART*Analog* converter in action makes our promises on the opposite page seem flat by comparison.

DEVICE	STATIC-TESTED ADCs CS5016	CS5014	CS5012	CS7820	DYNAMIC FFT-TESTED ADCs CSZ5412	CSZ5316	CSZ5116	CSZ5114	CSZ5112
Resolution	16	14	12	8	12	16	16	14	12
Conversion Time (μsec)	16	14	7	1.3	1.25		16	14	7
Throughput Speed (kHz)	50	56	100		1000	20	50	56	100
Static Specifications:									
Linearity Error (% FS, max)	+/−.0015	+/−.003	+/−.012	+/−.2	+/−.01				
No Missing Codes (Bits)	16	14	12	8	12	16	16	14	12
Dynamic Specifications									
THD (%)					.02	.007	.001	.003	.008
S/(N+D) (dB)					70	84	92	83	73
Power Dissipation (mW)	120	120	120	40	700	220	120	120	120
On-Chip Sample and Hold	YES	YES	YES	YES	YES	YES	YES	YES	YES

The proof behind the promise: monolithic CMOS performance that beats even hybrids.

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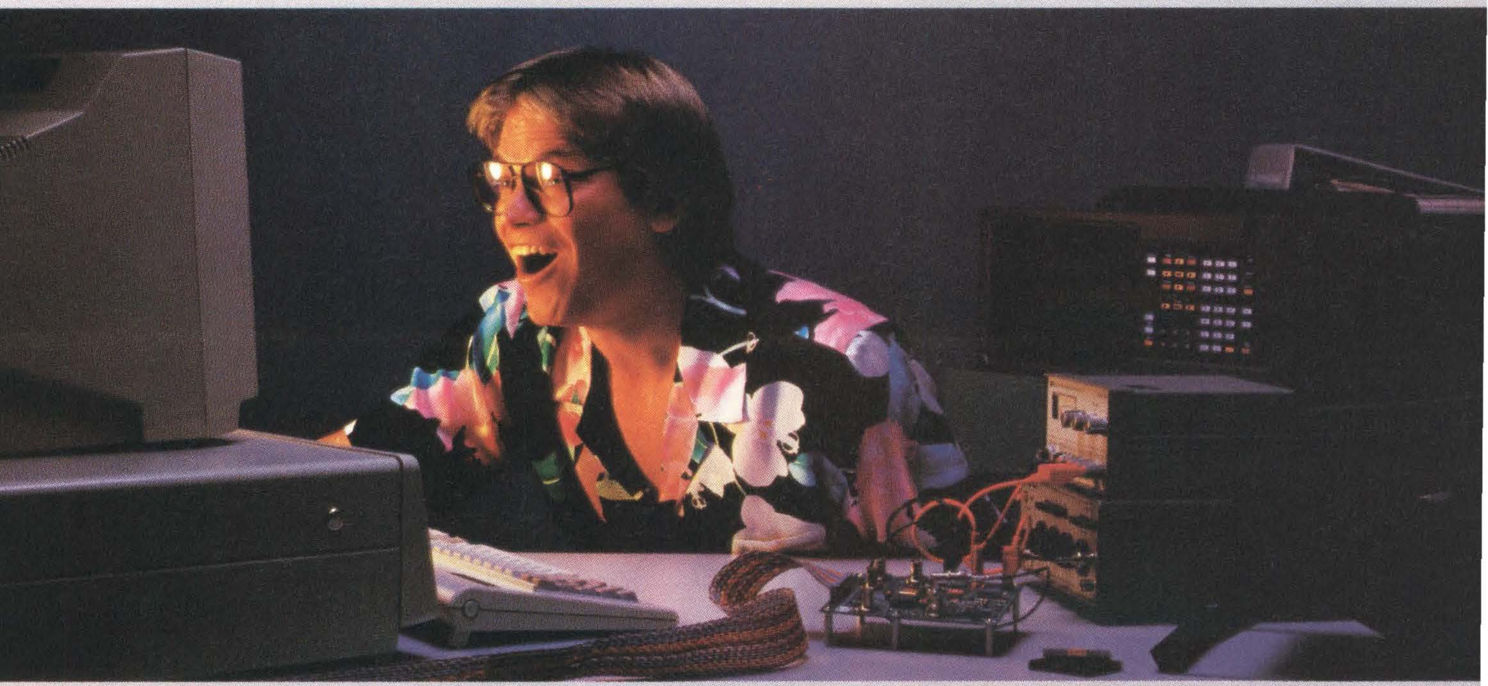

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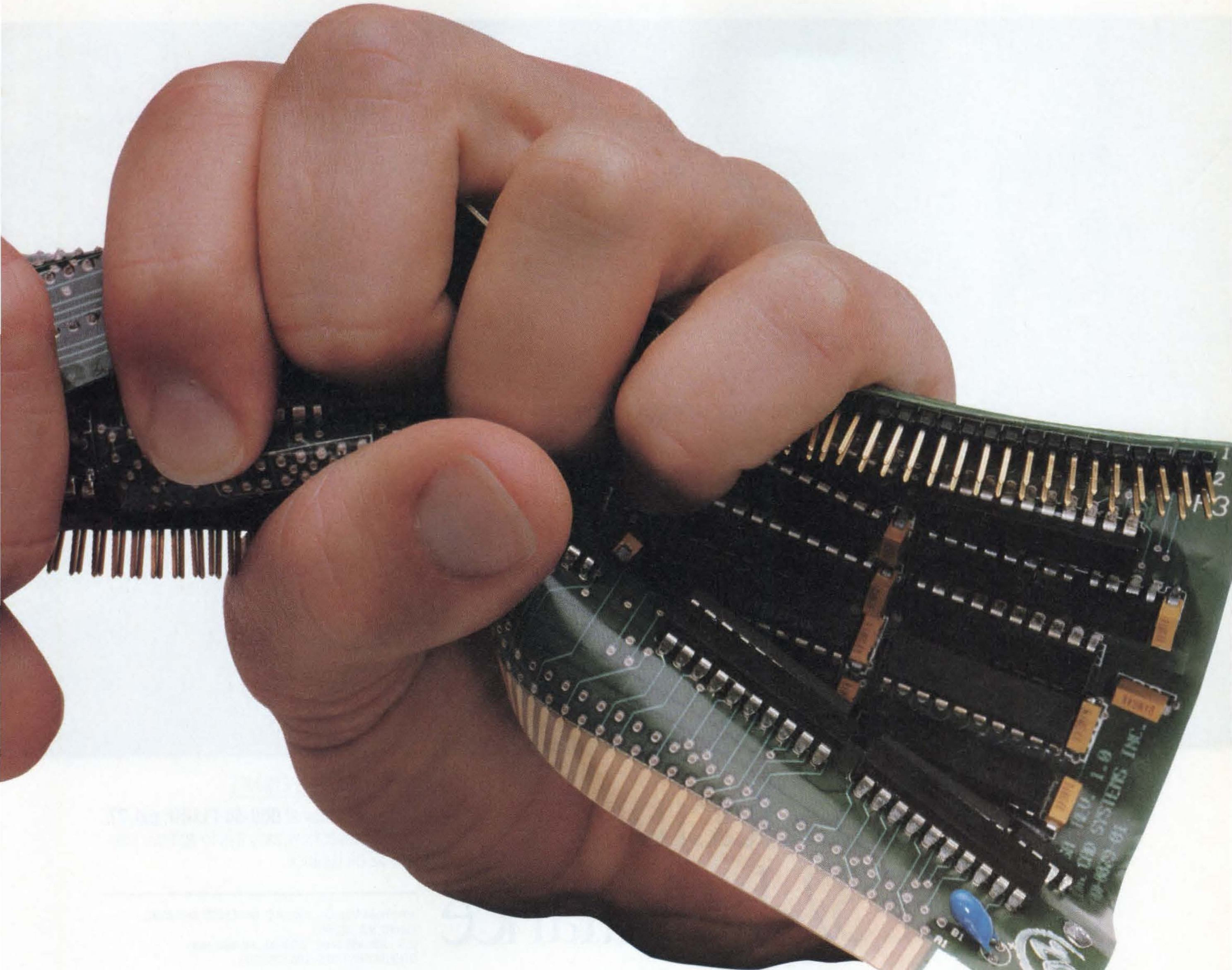

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CIRCLE NO 61

NEWS BREAKS

EDITED BY JOANNE CLAY

PLUG FOUR SMD DRIVES INTO YOUR SUN WORKSTATION

You can use the V/SMD 4400 Phoenix disk-controller board from Interphase (Dallas, TX, (214) 350-9000) to plug as many as four SMD or SMD/E disk drives into a Sun workstation. The board's BusPacket interface preformats packets of data in its high-speed bank of FIFO memory before acquiring control of the workstation's VME Bus. Then, once the BusPacket has control of the bus, the FIFO bank transfers the data as quickly as the bus and memory allow. This approach produces data-transfer rates over the VME Bus in excess of 30M bytes/sec. The board comes with installation software, boot ROMs, a queuing driver, a run-time formatter, and other utilities. You can purchase the board in single quantities for $3350.—J D Mosley

SCHEMATIC-ENTRY PC-BOARD CAD SOFTWARE SELLS FOR $395

The Capfast CF1000 software package for IBM PC/AT, PS/2, and compatible computers allows you to create pc-board schematics with an unlimited number of hierarchy levels. The package, from Phase Three Logic (Hillsboro, OR, (503) 640-2422), includes schematic and symbol editors, a symbol library containing more than 2000 components, a net-list extractor, a program for generating parts lists, and a plotting utility. The company claims that the software offers workstation-type features, such as on-line checking of electrical rules, dynamic panning, and split-screen capability.—Steven H Leibson

CMOS, MONOLITHIC 12-BIT A/D CONVERTER OFFERS 1-MHz SPEED

If you've been waiting for someone to develop a monolithic 12-bit A/D converter with the speed and accuracy of a hybrid device, you'll be pleased to learn that Crystal Semiconductor (Austin, TX, (512) 445-7222) now offers the CSZ5412-JC1—a CMOS device that operates at speeds as high as 1 MHz while consuming only 700 mW. Using a 2-step flash A/D conversion to achieve its high speed and accuracy, the CSZ5412 incorporates self-calibrating circuitry, pipelined acquisition and settling times, and overlapped conversion cycles. The chip also includes a track-and-hold amplifier, a 6-bit flash A/D converter, a 6-bit D/A converter, and a differential amplifier.

You can connect the CSZ5412 directly to a μP's data and control buses because it comes with an overrange output, 3-state output buffers, and a flexible control interface. Alternatively, the device can operate in stand-alone mode, independently of microprocessor control. The CSZ5412-JC1 costs $180 (100), and it includes the sample-and-hold circuitry that you must add to many competing hybrid devices. You can also order a similar device, the CSZ5412-JC2, which has a 500-kHz conversion rate and costs $115 (100).—J D Mosley

E- AND D-SIZE ELECTROSTATIC PLOTTERS PRODUCE PRINTS AT 1 IN./SEC

The 8500 Series monochrome plotters from Versatec (Santa Clara, CA, (408) 988-2800) employ electrostatic raster-printing technology that results in a 1-in./sec plotting speed. You can use the 24- and 36-in.-wide plotters as a department or network resource because of the fast output speed. The Model 8524 plots on 24-in.-wide (D-size) paper and costs $19,900; the Model 8536 uses 36-in.-wide (E-size) paper and sells for $24,900. The 8500 Series includes a controller that performs a vector-to-raster conversion. The controller accepts input in the Hewlett-Packard Graphics Language (HPGL) and Calcomp 906/907 vector data formats. You can choose among various types of media, including opaque, translucent, and vellum paper and clear and matte polyester films. The plotters are available now.—Maury Wright

NEWS BREAKS

AC/DC CLAMP-ON PROBE EXTENDS YOUR DMM'S CAPABILITIES

To measure current in awkwardly located cables, you can use the Model 159 ac/dc clamp-on current probe from Simpson Electric Co (Elgin, IL, (312) 697-2260). Specifying a dc to 400-Hz frequency band for current ranging from 0.1 to 500A, this autoranging probe lets you gain access to cables mounted in almost any position without breaking the circuit you're measuring. The maximum jaw opening of the clamp is 1.3 in. You can use the Model 159 with digital or analog meters. Its maximum operating voltage is 660V rms, and it sells for $169.—J D Mosley

$995 INK-JET PRINTER PRODUCES 2 PAGES/MINUTE AT 300 DOTS/IN.

Offering the look of laser printing without the high cost, the Deskjet printer from Hewlett-Packard Co (Palo Alto, CA, phone local office) emulates the company's Laserjet laser printer but costs $995. The Deskjet incorporates a drop-on-demand ink jet, and it can print text with graphics on plain paper at a rate of 2 pages/minute and with a resolution of 300 dots/in. It can print high-resolution or draft-quality text at 120 and 240 cps, respectively.

The printer's integral, front-loading sheet feeder accepts 100 sheets of paper and accommodates US letter, legal, and European A4 paper sizes. You can feed the printer #10 envelopes manually. The printer incorporates three built-in fonts—Courier, Courier Bold, and Courier Compressed—and accepts additional font cartridges through two accessory-cartridge ports. Each cartridge contains four or more fonts and costs $75 to $125. The printer's ink cartridge costs $18.95 and lasts for 200 to 400 pages, depending on the amount of graphics printed.—Steven H Leibson

SOCKET SUITS TEST AND BURN-IN OF VLSI LCC DEVICES

Suitable for use during the test and burn-in of VLSI devices packaged in ceramic leadless chip carriers (LCCs), the 132-contact Textool socket from 3M (Austin, TX, (512) 834-6792) has leads on 0.025-in. centers. The socket is made of glass-fortified polyphenylene sulfide, and the contacts are of beryllium copper plated with 30 μin. of gold over 50 μin. of nickel. A thruster spring in the body of the socket applies a constant pressure to the chamfered corner of the device, so that the device is properly and securely seated during use. A specially designed latching cover and two stainless-steel posts in the socket's body help reduce socket wear. The socket costs $38.94 (1000).—J D Mosley

80386-BASED WORKSTATIONS WILL RUN UNIX-BASED OPERATING SYSTEM

To create a common operating system for its line of 80386-based workstations, Daisy Systems Corp (Mountain View, CA, (415) 960-6591) has signed an agreement with Sun Microsystems whereby Sun will provide its Unix-based SunOS for Daisy's 80386-based workstations and Sun 4-based file servers. Daisy plans to release the SunOS-based workstations in the second half of 1988. The operating system will also incorporate the TCP/IP communications protocol (pioneered by the US Department of Defense) and Sun's Open Network Computing/Network File System (ONC/NFS).

The standard Unix-based environment will allow the workstation users to take advantage of the wide variety of available software-development tools and standard communications packages for integrating CAE networks with existing computer environments. The initial terms of the agreement between Daisy and Sun cover a 5-year period, during which Daisy will receive all enhancements made to the operating system, including any enhancements resulting from the joint development efforts of Sun and AT&T. Daisy doesn't plan to port SunOS to any of its 80286-based workstations.—Joanne Clay

NEWS BREAKS: INTERNATIONAL

μP PERIPHERAL CHIPS SUIT MILITARY AND SPACE APPLICATIONS

Marconi Electronic Devices Ltd (Lincoln, UK, TLX 56380; in the US, phone (516) 231-7710) has introduced several μP peripheral chips fabricated in the company's radiation-hard SOS (silicon-on-sapphire) technology, which makes the chips suitable for use in military and space applications. The MAS8237A 4-channel DMA controller, MAS8255A peripheral interface adapter, and MAS8251A universal synchronous/asynchronous receiver transmitter (USART) are pin and function compatible with the equivalent Intel parts. Military-grade versions of the chips sell for £280, £220, and £250 (100), respectively. For the same prices, you can obtain similar parts (the MAS28137, MAS28155, and MAS28151, respectively) that have the drive and timing requirements necessary for use with the McDonnell Douglas MDC-281 MIL-STD-1750A processor. You can also obtain the 54HST630, a radiation-hardened 16-bit parallel error-detection and error-correction IC. A military-grade version of this part costs £170 (100).—Peter Harold

VME BUS MODULE EASES SYSTEM INTEGRATION

By using the $2000 CVMEBS1 VME Bus stimulator module from Concise Technology (Aylesbury, UK, TLX 975646), you can exercise your operating-system and device-driver software before all your system's hardware is installed. The module allows you to generate VME Bus interrupts on any interrupt level and bus requests on any bus-request level. For interrupts, you can select the eight least significant bits (LSBs) of the 8-, 16-, or 32-bit Status/ID word, which the module places on the VME Bus during the interrupt-acknowledge cycle.

In addition to generating legal VME Bus conditions, the module can also generate spurious interrupts or bus requests, allowing you to test the system's response to ghost conditions. A special mode allows you to slow down the response of the module's interrupter and bus requester. The module also allows you to generate VME Bus SYSFAIL*, SYSRESET*, and ACFAIL* signals. Although it normally occupies two VME Bus slots, the CVMEBS1 has a detachable control panel that allows you to operate the module in a single VME Bus slot.—Peter Harold

MITI ASKS JAPANESE ELECTRONICS FIRMS TO BUY MORE US SEMICONDUCTORS

In the wake of renewed complaints from the US government, the Japanese Ministry of International Trade and Industry (MITI) has asked 10 of Japan's major electronics companies to purchase more US semiconductor products. MITI reportedly expects to see an increase of at least 10% in the procurement of US semiconductors by the major Japanese electronics companies, which include NEC, Toshiba, Hitachi, Fujitsu, Matsushita, and Mitsubishi. The Japanese government has apparently promised that US semiconductor firms will have a 20% share in the Japanese semiconductor market by the year 1991. MITI claims that the American share in the Japanese market has already grown to 12.7%.—Joanne Clay

FUNCTIONAL TRANSISTOR ACHIEVES 5.5 PSEC AT ROOM TEMPERATURE

Fujitsu Ltd has developed a resonant tunneling bipolar transistor that can operate at 5.5 psec at room temperature. Resonant tunneling bipolar transistors can replace six or seven conventional transistors. Previous versions of this type of transistor could operate only at very low temperatures, however. To create this room-temperature version, Fujitsu replaced the traditional materials—gallium arsenide and aluminum gallium arsenide—with indium gallium arsenide and indium aluminum arsenide.

—Joanne Clay

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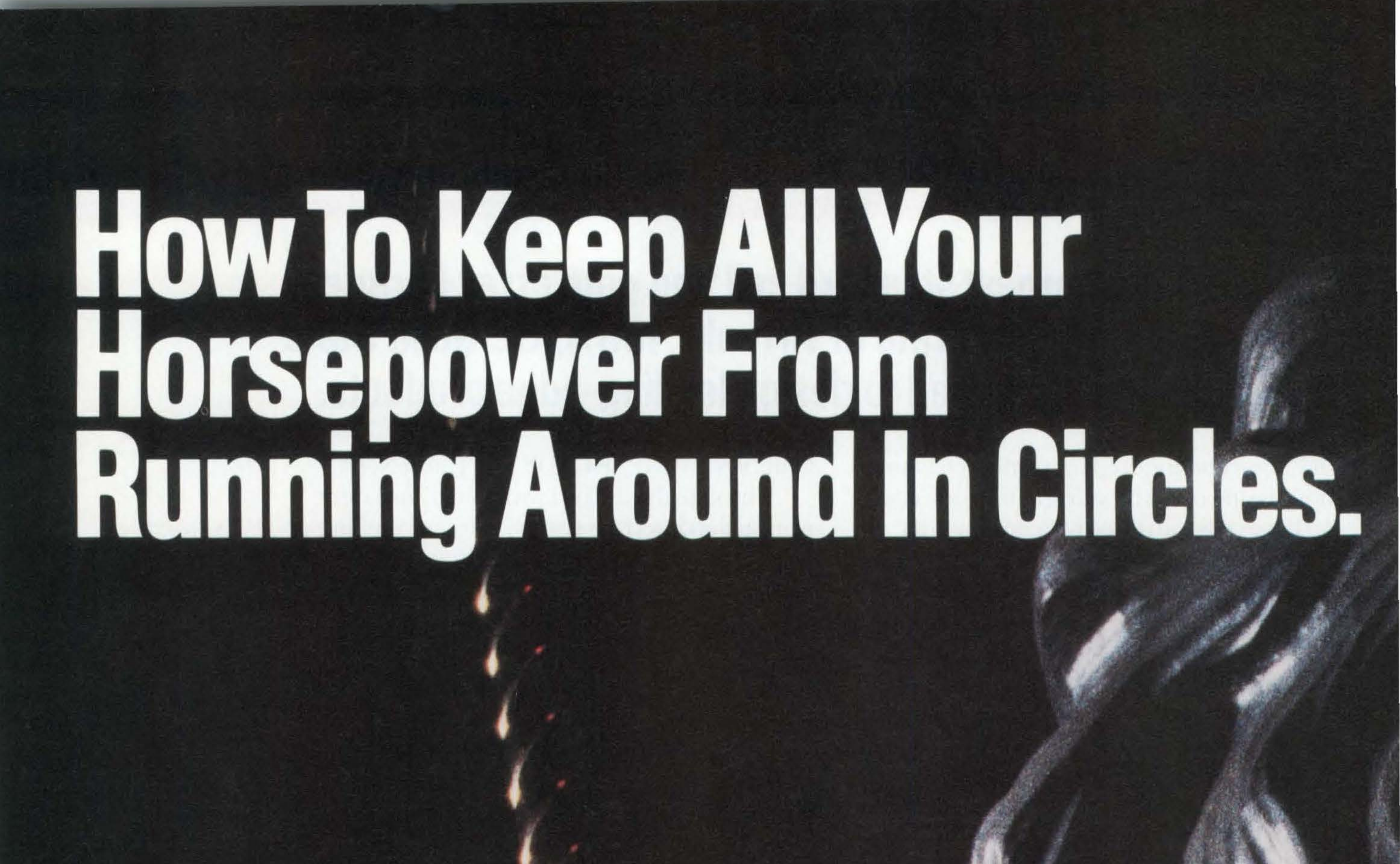

To really understand your performance problem, just turn traditional thinking around.

You see, your CPU is really more like a peripheral—it's usually your storage subsystem that sets the pace.

When you look at the problem that way, it's a horse of a different color. The solution, of course, isn't a CPU upgrade. It's better management of the data.

At System Industries, that's an idea we've championed all along. And the same one behind our new CLUSTOR™ family of shared data storage systems.

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SIGNALS & NOISE

A transimpedance amp by any other name . . .

In his article, "Use of transimpedance amplifiers minimizes design tradeoffs" (EDN, November 26, 1987, pg 205), Alan Hansford of Analog Devices uses the term "transimpedance amplifier" in a misleading way.

According to longstanding usage, that term refers to the function being performed, namely, actively converting a current to a voltage, not to the type of amplifier used as the active element. Any electronic negative-feedback amplifier having inverting and noninverting inputs will perform as a transimpedance amplifier if it's connected in the correct manner. The amplifier that the article describes has a −3-dB bandwidth that's nearly independent of closed-loop voltage gain—a nice feature, but transimpedance amplifiers have neither voltage-gain nor gain-bandwidth independence.

"IT'S GETTING SO YOU CAN'T EVEN TAKE TIME FOR ONE LOUSY CUP OF COFFEE AROUND HERE WITHOUT HIM BLOWING UP!"

So, if the amplifier isn't a conventional voltage-feedback op amp, (as Mr Hansford states in his article), and if transimpedance amplifier is an improper name, then what is the correct description? The accepted term is "current-feedback op amp." Comlinear introduced the term in 1982 to describe the first op amp with gain-bandwidth independence, a −3-dB bandwidth, and an extremely fast settling time. Current feedback is the key to this performance, but it's not an inherent property of a transimpedance amplifier, contrary to what Mr Hansford says. Comlinear has described the operation of its current-feedback op amps in numerous magazines and application notes since 1982.

The author's conceptual model of operation (pg 210) bears little resemblance to the op amp design that he describes. Rather, the described op amp is designed in accordance with the design that Comlinear invented, patented, and has used in op amps such as the CLC231. I'm flattered by Analog Devices' imitation of our products, but by failing to reference our pioneering work, it

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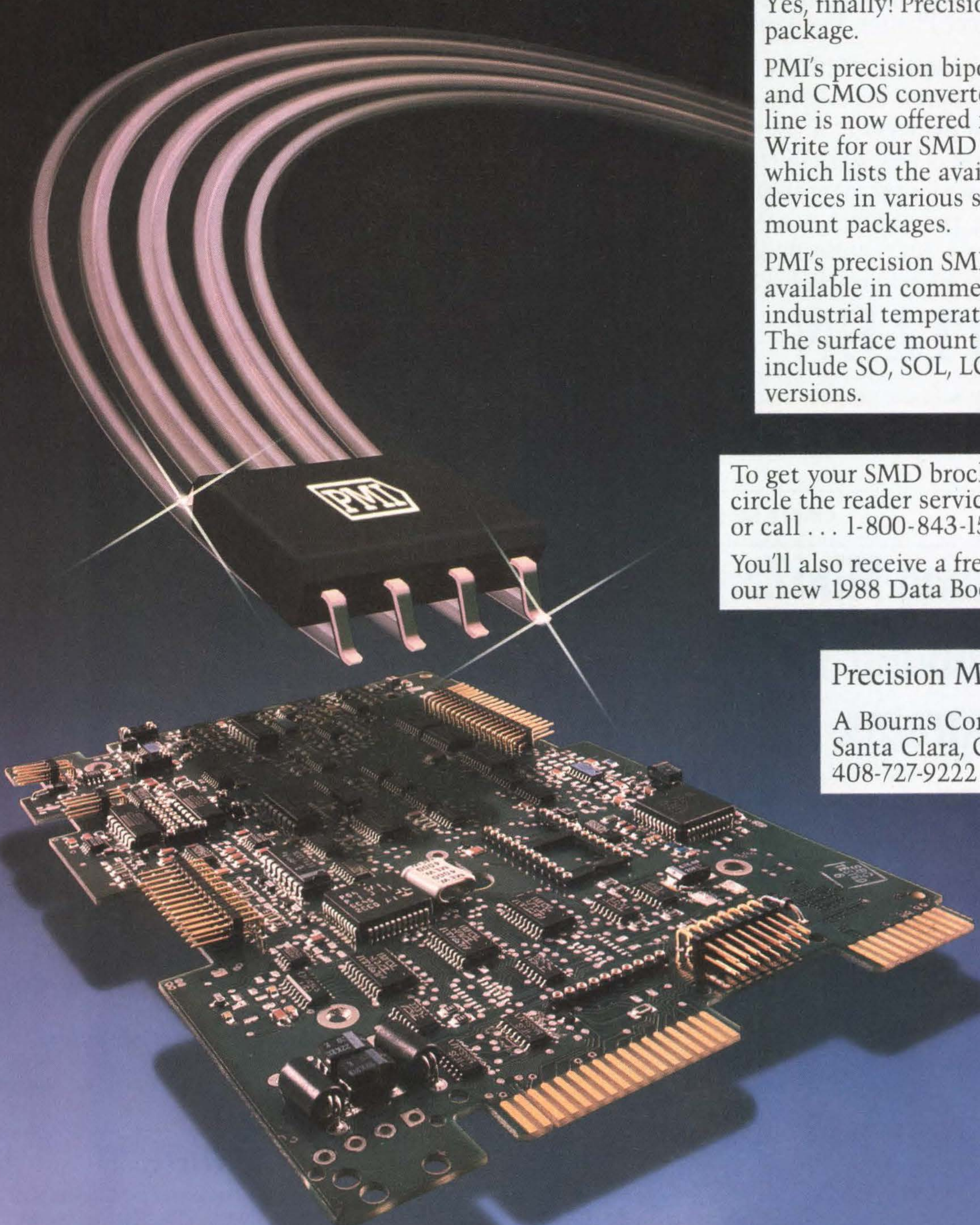

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makes one wonder if the company is trying to take credit for this new and useful class of op amp.

David Nelson
President
Comlinear Corp
Ft Collins, CO

Analog Devices responds:
Mr Nelson's comments are insightful and interesting. Two statements are slightly misleading, however, and require clarification.

The implication is that Analog Devices violated a Comlinear patent by bringing the AD9610 to market; a second implication is that Comlinear did the "pioneering work" in the field of "current-feedback op amps." Analog Devices is aware of the patents in question, and the AD9610 does not infringe on any Comlinear patent. As for the issue of pioneering work, current-feedback amplifiers have a long and well-documented history in the electronics industry. Innumerable textbooks contain references to and examples of current-feedback amplifiers. Many of these books were printed and copyrighted long before 1982.

Analog Devices identified a segment of users that was not totally satisfied with existing high-speed amplifiers, and subsequently introduced the AD9610. We stand by our products, our technology, and our reputation as leaders in this industry. Competition is the cornerstone of the American free-enterprise system.

Thomas Gratzek
Linear Products Marketing Manager
Analog Devices, Computer Labs Div
Greensboro, NC

WRITE IN

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MULTIBUS II TAKES YOU BACK TO THE BASICS

...AND INTO THE FUT

MULTIBUS II OPENS UP ADVANCED APPLICATIONS IN WAYS NO OTHER BUS CAN.

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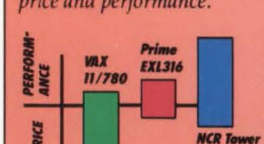
A new generation of microcomputer systems based on Multibus II is now emerging, to redefine standards of price and performance.



A bus capable of supporting vast new levels of microcomputer performance. To make possible low cost microcomputer systems that outperform minis, and rival mainframes.

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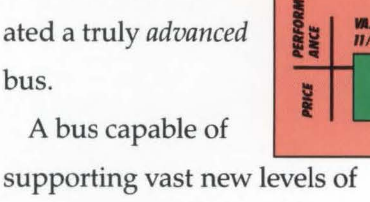

BASIC #2: HARDWARE-ASSISTED MESSAGE PASSING.
This advanced technique gives Multibus II a true sustained bandwidth of 32 megabytes per second. Standardized in a single silicon chip, message passing simplifies sytem design, and makes it possible to mix totally different microprocessor architectures and operating systems in the same application.

A more maintainable bus, to reduce the cost and complexity of configuration, trouble-shooting and repair.

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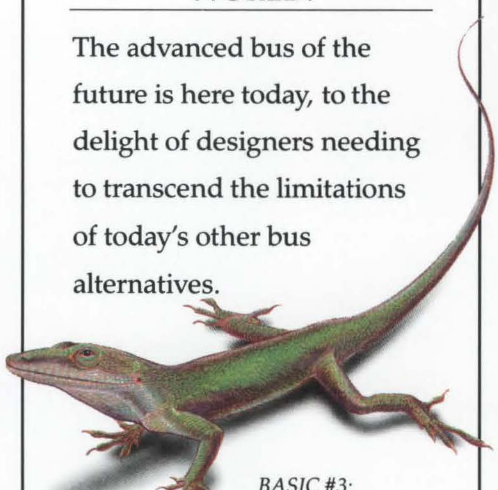

BASIC #3: AUTO CONFIGURATION.
Like a chameleon, Multibus II boards automatically configure themselves when system power is turned on, eliminating DIP switch hassles during configuration and maintenance.

BASIC #1: PARITY.
Multibus II's parity error detection provides the basic protection needed by advanced applications that process large volumes of data at high speeds.

For example, NCR and Prime based their newest Tower™ and EXL™ systems on Multibus II. Both provide several times the power of a VAX™ 11/780 minicomputer,

TRADITIONAL VS. AD

	CHARACTERISTICS	TRADITION
		MULTIBUS I
BASIC FEATURES	TIMING (Synchronous or Asynch)	ASYNCH
	PIN USAGE (MPX) Multiplexed (NON) Non-Multiplexed	NON
	ARBITRATION (CENT)ralized (DIST)ributed	CENT.
	INTERRUPTS (DED)icated (VIR)tual	DED.
	GLOBAL MEMORY Communications	YES
ADVANCED FEATURES	PARITY	NO
	AUTO-CONFIGURATION (Geographic Addresses)	NO
	MESSAGE PASSING (Hardware)	NO
	BUS I/F SILICON	NO
OTHER FEATURES	ADDRESS WIDTH (Bits)	20,24
	DATA WIDTH	8,16
	BOARD AREA (sq. in.)	84
	CONNECTOR TYPE	EDGE
	MAX. 5V POWER (Per slot)	24A

*Implemented outside IEEE 1014 using several proprietary schemes.

at a fraction of the price.

A major U.S. department store chain has put into operation a revolutionary home shopping network, based on Multibus II.

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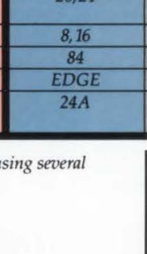

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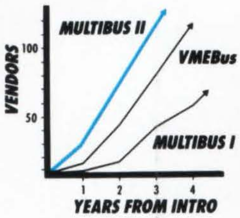
architecture for the future for advanced factory automation applications.



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VANCED ARCHITECTURES

AL BUSES	ADVANCED BUSES	
VME	MULTIBUS II	VAX BI
ASYNCH	SYNCH	SYNCH
NON	MPX	MPX
CENT.	DIST.	DIST.
DED.	VIR.	VIR
YES	YES	YES
NO	YES	YES
NO	YES	YES
NO*	YES	YES
AVAIL. '88	YES	YES
24,32	32	32
8,16,24,32	8,16,24,32	8,16,24,32
59.8	80	73.4
DIN	DIN	ZIF
6A	15A	Not Published

Throughout the world, these and scores of other companies have introduced or are now developing Multibus II applications that set new standards of performance, price and reliability.

BASIC #4: MULTI-VENDOR COMPATIBILITY.
A host of unique features ensure that Multibus II boards will work together efficiently and dependably. The IEEE 1296 specification is complete and concise. And, the Multibus II Message Passing Coprocessor (MPC), now universally available, ensures compatibility even between boards using different processor architectures and operating system software.

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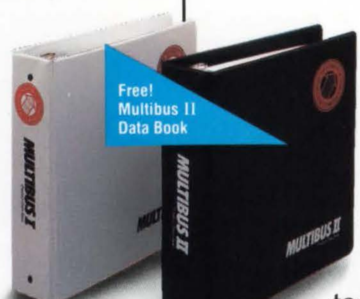

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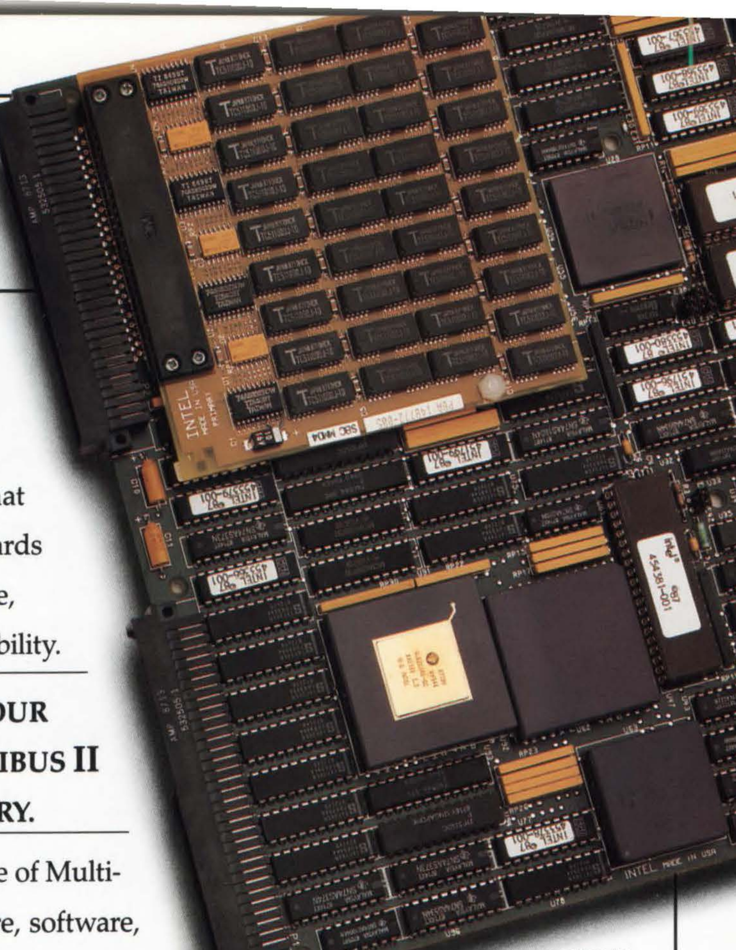

BASIC #5: MECHANICAL INTEGRITY.
Naturally, Multibus II uses DIN connectors, for the most reliable mechanical connections. But, it also incorporates built-in front panels for EMI shielding. And, its standard Eurocard form factor provides enough board space (a full 80 sq. in.) to accommodate complex designs.

So don't delay. Get the whole story on Multibus II and discover the new levels of performance and reliability that are possible with a truly advanced bus.

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Central Data	1602 Newton Drive Champaign, IL 61821 Contact: André Felix (800) 482-0315 FAX (217) 359-6904	•	•		•	•	•			•		
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The Multibus Manufacturers Group, or MMG, is dedicated to the proposition that everyone benefits from strong, open standards. Membership is open to hardware and software manufacturers, application integrators, end users and even students.

To learn more about what the MMG can do for you, contact Dan Fink, MMG executive director.

Use this convenient product reference guide to quickly locate the companies that offer the types of Multibus II products you need.

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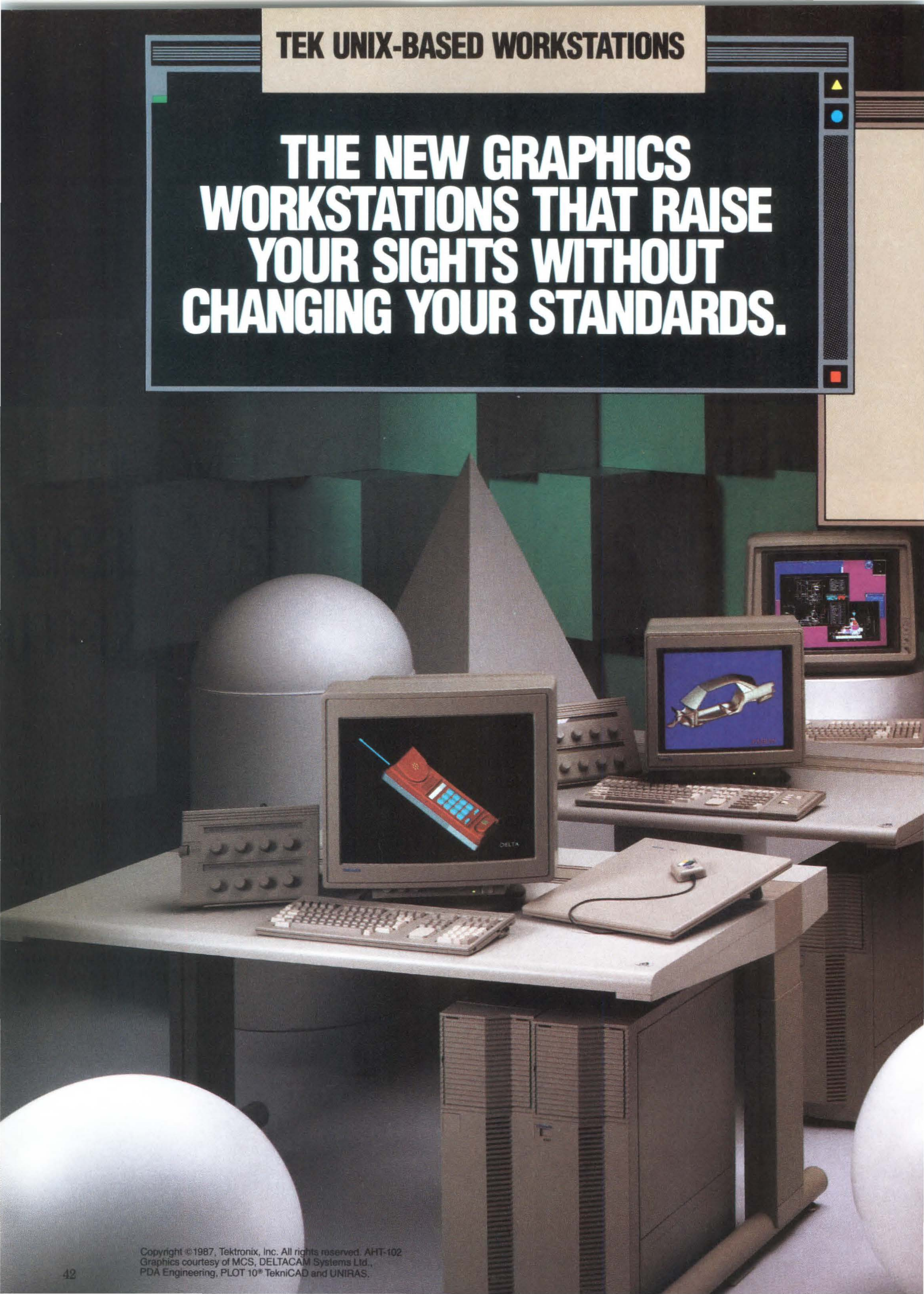
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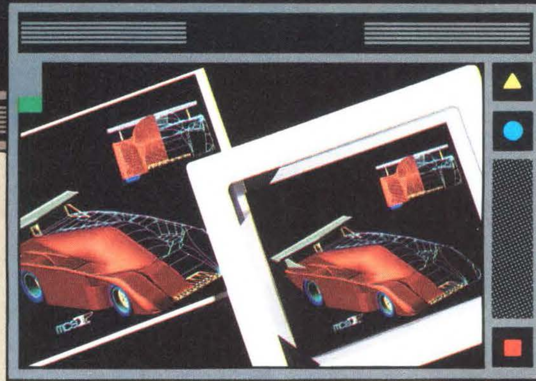

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CALENDAR

American Association for the Advancement of Science Annual Conference, Boston, MA. AAAS, 1333 H St NW, Washington, DC 20005. (202) 326-6448. February 11 to 15.

Semicustom Circuit Program Conference, San Diego, CA. Mackintosh Consultants, 209 W Central St, Natick, MA 01760. (617) 655-0001. February 17 to 19.

Software Development '88, San Francisco, CA. Miller Freeman Publications, 500 Howard St, San Francisco, CA 94105. (415) 995-2426. February 17 to 19.

Digital Signal Microprocessor and Microcomputer Chips and Development Systems (seminar), Palo Alto, CA. Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. February 22 to 24.

Compcon Spring '88 (33rd IEEE Computer Society International Conference), San Francisco, CA. Hasan AlKhatib, Dept of EECS, Santa Clara University, Santa Clara, CA 95053. (408) 927-1818. February 29 to March 4.

Microwave IC Technology (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. March 4.

Personal Computer Interfacing for Scientific Instrumentation Automation (short course), Blacksburg, VA. Linda Leffel, CEC, Virginia Tech, Blacksburg, VA 24061. (703) 961-4848. March 10 to 12.

Modern Electronic Packaging (seminar), San Diego, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. March 15 to 17.

CALENDAR

Microelectronic Packaging and Surface Mounting (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. March 18.

10th Annual Conference for Inventors and Entrepreneurs, Denver, CO. Rocky Mountain Inventors Congress, Box 4365, Denver, CO 80204. (303) 443-3818. March 18 to 19.

Neural Networks for Artificial Intelligence, Arlington, VA. Technology Transfer Institute, 741 10th St, Santa Monica, CA 90402. (213) 394-8305. March 21 to 23.

Digital Signal Microprocessor and Microcomputer Chips and Development Systems (seminar), Cambridge, MA. Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. April 4 to 6.

Microcircuit Interconnections and Assembly Methods (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 7.

Electrostatic Discharge (ESD): Concern or Over-concern? (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 12.

Hybrid Microcircuit Technology (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 18.

American Power Conference, Chicago, IL. Robert Porter, Chicago Institute of Technology, Chicago, IL 60618. (312) 567-3202. April 18 to 20.

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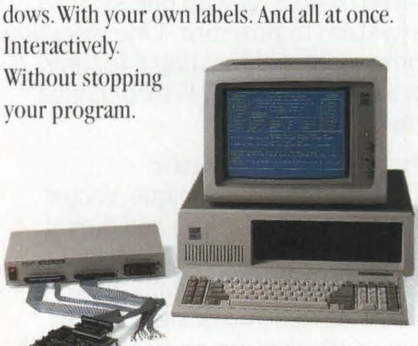

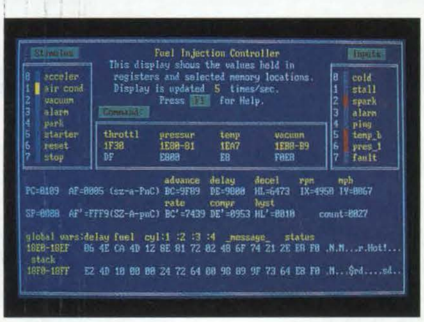

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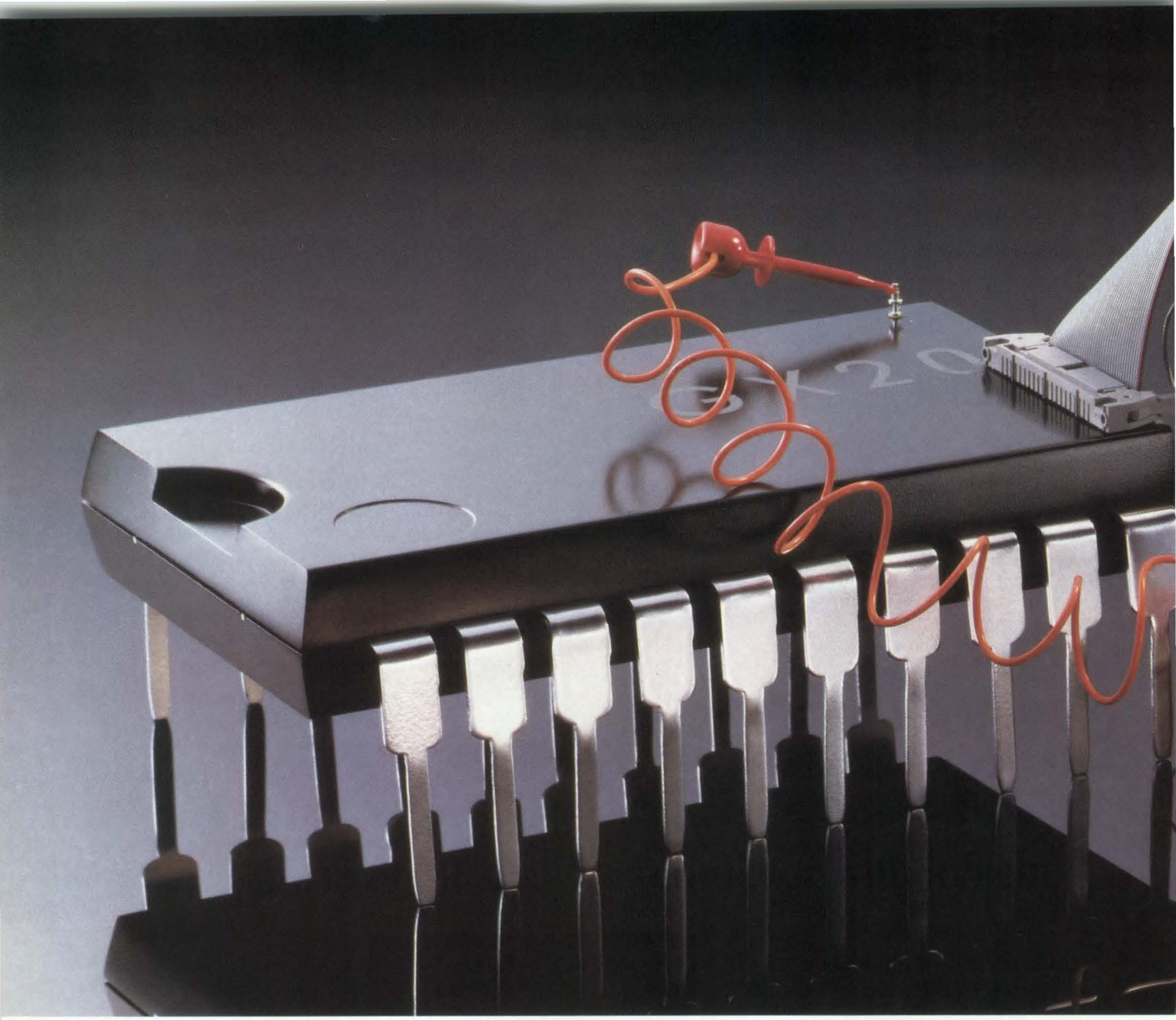

You wouldn't do this with your Analog VLSI devices.

You'll have to if you go to most ATE companies for a solution to today's sophisticated "system silicon" testing problems. Because all you'll get is a makeshift tester. And that means resigning yourself to man-months of custom hardware work integrating analog and digital instrumentation. And putting up with the long hours of low-level software development that go with custom solutions. Worse, you can expect these delays to cut your chances of getting your product to market on time.

Teradyne now has a simple answer to this complex testing problem. The A500 Analog VLSI Test System. It's the first of a new generation of systems specifically for AVLSI "system silicon" devices. A test system that can help you cut critical product development time by months or even years.

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The A500 allows you to do it all with one system. So there's only one system to program. One insertion to make for both component and functional testing. And only one data base to work with. Which means significantly less time to market.

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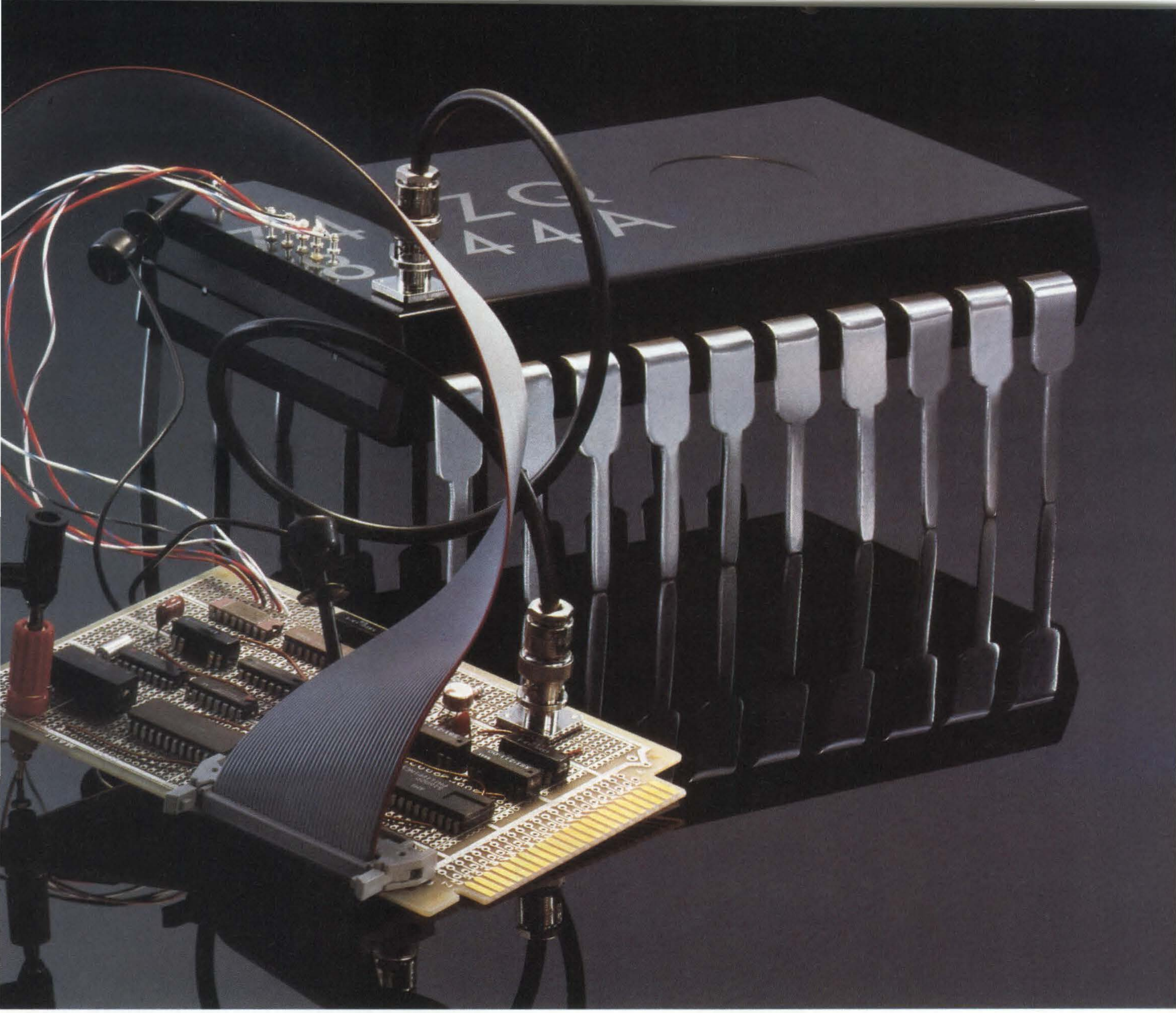
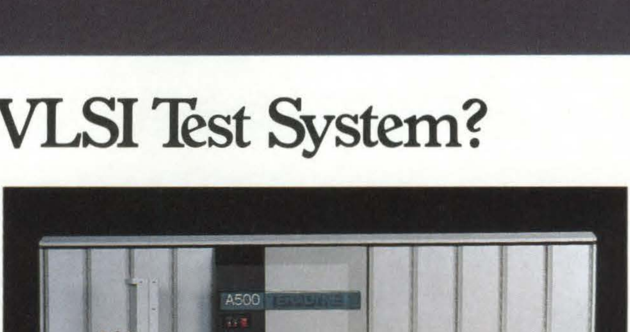
The heart of the A500 is Teradyne's unique Vector Bus II architecture. It integrates analog and digital VLSI test capability at the system level. Which means you won't have to build special applications hardware for every new device you design. Vector Bus II eliminates that costly custom-work bottleneck



Why accept it in an Analog VLSI Test System?

with such features as TimeMaster™ Synchronization, Mixed-Signal Event Control, and MultiSource Data Mixing.



A Picture's Worth a Thousand Keystrokes
The A500 also revolutionizes program development. Our IMAGE™ (Interactive Menu-Assisted Graphics Environment) software gives you graphics programming as powerful as device designers' CAD/CAE tools. Using a mouse to control multiple windows, pop-up menus and software "power tools," you move ideas rapidly from mind to screen. And much faster to market.

Teradyne's new A500 is the only test system with the features you need to win the race for Analog VLSI market opportunities. To find out more, call Beth Sulak at (617) 482-2700, ext. 2746. Or call your nearest Teradyne sales office or write: Teradyne, Inc., 321 Harrison Avenue, Boston, MA 02118.

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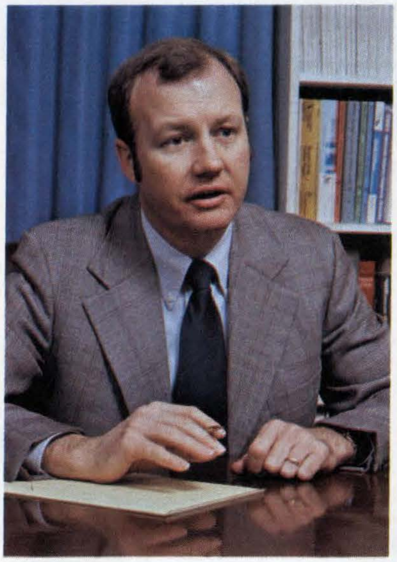
EDITORIAL

The IEEE faces extinction



Since Irwin Feerst gathered a respectable number of votes in the IEEE's 1986 annual election, the organization has renewed its determination to prevent dissidents from participating in IEEE affairs. Now, instead of facing up to the need for internal reform and external action on behalf of its members, the IEEE's board of directors is dabbling in election-policy changes. Those changes are driving the organization closer to extinction.

Because Feerst split—and almost won—the 3-way contest for president-elect in 1986, the IEEE decided to nominate only one IEEE-sanctioned candidate for the president-elect position in future elections. No more split elections, if you please. However, the hue and cry against having a single candidate was so great that the IEEE's board of directors has reconsidered. You'll now choose from two IEEE-backed candidates for president-elect.

But to ensure that no petition candidate splits an election with the two sanctioned candidates, the IEEE has adopted "approval" voting. In such a scheme, IEEE members get the chance to cast an "approval" vote for each candidate on a ballot. Thus, by not casting a vote, they withhold approval from a candidate. It's worth noting that the board of directors modified the election procedure by changing the organization's bylaws, not by asking members to amend the organization's constitution. The IEEE's board of directors has a case of siege mentality. Once an organization is infected with that disease, it's headed for extinction.

So, instead of real reforms or calls for action by the IEEE's "leaders," you'll see more of the same plodding and self-preserving moves that now characterize the IEEE. Working engineers will observe no action on tax or pension reforms, no action on age discrimination, and no action on other professional concerns. In short, no action at all.

The besieged IEEE will continue publishing journals and periodicals, but that hardly forms the heart of a vital *professional* organization—one that should be improving its members' profession and working environment. So, when it's time to renew your IEEE membership, consider the cost carefully. Are those journals and group life-insurance policies really worth it? If you still think the IEEE has a chance of surviving as a *professional* organization and you renew your membership, send Irwin Feerst's Committee of Concerned EEs a check for an equal amount. You may not agree with everything Feerst says and does, but he has probably done more to change the IEEE than anyone else who has won one of its lopsided elections.

Jon Titus

Jon Titus
Editor

Instant Grat

Go ahead. Indulge yourself. And say hello to BUSTER. The first user-configurable MPU peripheral. And the fastest and easiest way yet to get your proprietary design from concept to silicon.

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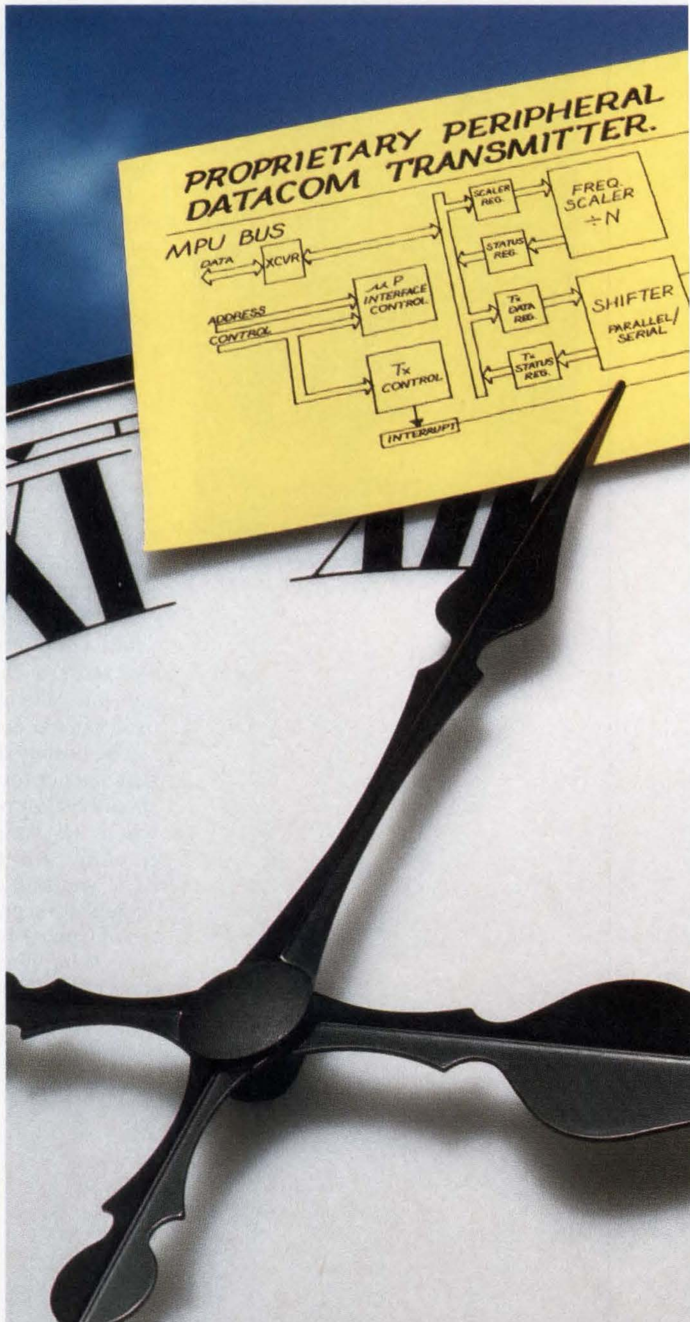


ification.

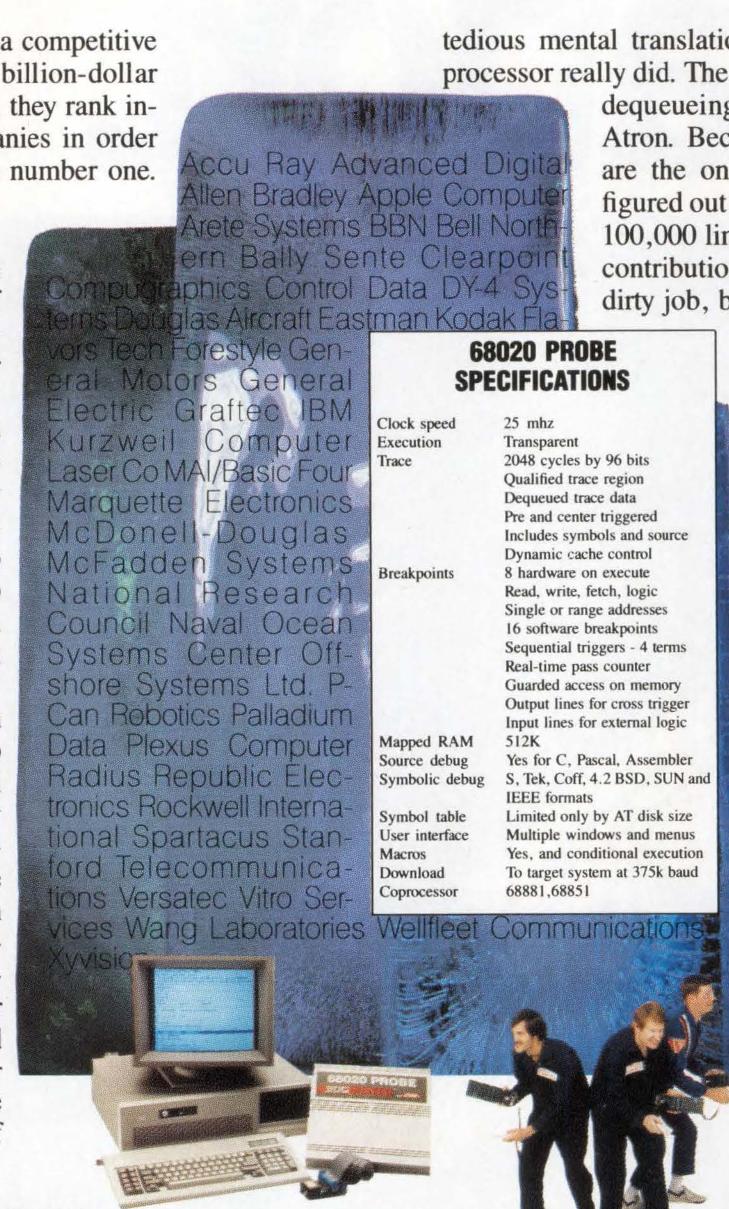
WHO YA GONNA CALL TO ICE 68020 BUGS? ATRON BUGBUSTERS!

We recently received a competitive analysis written by a billion-dollar competitor of ours. In it, they rank in-circuit emulation companies in order of importance. We were number one.

SO WHO'S ATRON?

Today, Atron is the number-one supplier of hardware-assisted software debuggers for 8088/80286/80386-based PCs. Nine of the top ten software packages were written by Atron customers. Everybody from AST to Borland to Oracle to Zenith. Now, we can make the same claim in the 68020 marketplace.

Everybody from Apple (MAC IIs) to Wellfleet (datacom) will attest to the superiority of Atron's 68020 debugging technology. One Atron customer even said, "We sent our non-Atron ICE unit out several months ago for repairs; nobody around here seems to know or care if it's back yet. The Atron unit is the tool of choice.'"



68020 PROBE SPECIFICATIONS

Clock speed	25 mhz
Execution	Transparent
Trace	2048 cycles by 96 bits Qualified trace region Dequeued trace data Pre and center triggered Includes symbols and source Dynamic cache control
Breakpoints	8 hardware on execute Read, write, fetch, logic Single or range addresses 16 software breakpoints Sequential triggers - 4 terms Real-time pass counter Guarded access on memory Output lines for cross trigger Input lines for external logic
Mapped RAM	512K
Source debug	Yes for C, Pascal, Assembler
Symbolic debug	S, Tek, Coff, 4.2 BSD, SUN and IEEE formats
Symbol table	Limited only by AT disk size
User interface	Multiple windows and menus
Macros	Yes, and conditional execution
Download	To target system at 375k baud
Coprocessor	68881,68851

25-MHZ, REAL-TIME, EMULATION: SOONER OR LATER, YOU KNOW YOU'LL NEED IT.

Why invest in a slower emulator (especially one that costs more)? Some bugs only occur in real time, and you know your next design will be 25 mhz. Before Atron's state-of-the-art design, there was no such thing as a 25-mhz emulator. There still isn't another one anywhere near our price.

PROBE CAN TRACE IT THROUGH THE PIPELINE, SO YOU WON'T LOSE YOUR MIND.

The 68020 has an on-board pre-fetch pipeline. Without Atron's 68020 PROBE, your best software engineer will spend a lot of time figuring out which instructions actually execute, and then, which bus cycles go with those instructions. The 68020 PROBE eliminates all these tedious mental translations and displays what the processor really did. The technology, called pipeline dequeueing, is only available from Atron. Because the Atron bugbusters are the only ones anywhere who've figured out how to do it. And it took us 100,000 lines of code. Consider it our contribution to your sanity. (It was a dirty job, but somebody had to do it.)

LET THE SOURCE BE WITH YOU.

Why spend all day doing mental translations between your C source code and the machine code in your target? These tedious operations are eliminated with Atron's source-level debugging capabilities.

Since PROBE uses a PC AT as its instrumentation chassis, you can get compiled code to its target via Ethernet, VAXNet, SUNNet, SCSI or RS-232. And whether you are compiling on a PC, a workstation or a VAX, Atron supports more object-module formats than anybody else (see specification box).

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☐ Please send me your 36-page 68020 PROBE user's guide, with its command summary and examples of use.

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EDN 020488

High-performance DMMs and calibrators bring standards-lab specs to the benchtop

Dan Strassberg,
Associate Editor

You don't have to take these meters out of service to calibrate them. *In Racal-Dana's Series 6000 DMMs, all components that affect calibration are in a module—removable from the rear of the instrument—that you can exchange when the unit needs calibration.*

To satisfy their customers' continuing demands for improved performance, engineers who design and test products such as data converters and automatic test equipment (ATE) must make increasingly accurate basic measurements in their labs, in production, and in systems. Manufacturers of digital multimeters (DMMs) and voltage/current/resistance calibrators are providing tools to meet these tightened measurement requirements. This new generation of rugged, affordable, and easy-to-use instruments offers accuracy that, until recently, was possible only in the cloistered and sacrosanct standards-laboratory environment. To realize the accuracy these instruments promise, however, you must apply them with consummate care.

DMMs measure ac and dc voltage and current, resistance, and voltage and resistance ratios. Not all the meters discussed here can make every one of these measurements. **Table 1** lists some representative high-precision DMMs. All of these DMMs offer resolution of 6½ digits or more; some provide resolution as high as 8½ digits. Depending on how the vendor defines a half digit and how it defines full-scale range (FSR), an 8½-digit meter may be able to resolve an input change as small as 2.5 parts per *billion* of FSR.

A question frequently posed about such high-resolution meters is, "Who needs so many digits?" In many cases, the ability to resolve six digits or more doesn't make previously impossible measurements possible—it just makes possible measurements much easier. For example, if you're measuring the temperature coefficient (TC) of a low-TC resistor, you might find it easier to read resistance directly from a DMM than to rebalance a bridge each time you want a reading.

If you're determining the accuracy of an attenuator, you could use a precision voltage divider (for example, a Kelvin-Varley divider) and a null meter. Alternatively, you could use an 8½-digit DMM and read the divider ratio with resolution as fine as 1 ppm, even when the output of the divider you're testing is only 1% of its input. To measure the divider ratio as accurately with a DMM that has lower resolution, you'd need to change DMM ranges. Range changing introduces the possibility of incurring additional errors. In both of these examples, the built-in computational capabilities of many available meters could make the job even easier—for instance, by computing the TC after you enter the temperature change, or by calculating and displaying the percent error in the attenuator.

If you're designing a process to test measuring equipment (A/D converters, for example), you could supply a signal to the unit under test (UUT) from a relatively inaccurate source having a low-noise, short-term-stable output that you monitor with a very accurate meter. Instead of using the meter and low-accuracy source, you can use a calibrator—a low-noise, stable, *and* highly accurate source of voltage, current, or resistance. Although the meter and low-accuracy source are more general-purpose instruments than the calibrator and might appear to offer a better value, you might achieve higher test throughput, and possibly even improved test accuracy, by using the calibrator directly. **Table 2** gives an overview of the capabilities of several representative calibrators.

The almost universal application of μPs and related components in high-performance DMMs and calibrators accounts for many recent

advancements in the instruments' stability and ease of use. Remember, though, that a very large portion of each of these instruments consists of circuits that are inherently analog, and computer technology can't solve all the analog measurement problems. For example, it's difficult to imagine (and probably impossible to construct) a dc-voltage-measuring digital meter that doesn't include a stable voltage reference and some type of voltage divider (or its functional equivalent).

The reference and divider, as well as the meter's A/D converter, are analog circuits. Note that although the reference must be stable over time, it really needn't be accurate. As long as you, or a standards lab, can compare the reference voltage against the accurately known output of another reference source, and store the amount by which the meter's reference differs from the ideal, you can correct your meter's readings so that they're more accurate than the internal reference is.

Basically, to calibrate is to determine how meter readings (or source outputs) differ from the ideal, and to insert corrections. The use of digital technology has significantly improved the ease and speed of instrument calibration, and has made it possible to eliminate major sources of calibration drift (that is, changes in calibration over time). Calibration used to require removing the covers from an instrument and adjusting potentiometers inside, an operation a prudent person would entrust only to a standards lab. Many newer instrument designs eliminate calibration potentiometers entirely, replacing them with nonvolatile memory that stores corrections, and µPs that apply the corrections to the A/D converter's output before driving the display.

Calibration under µP control offers several advantages. In some cases, you can perform it yourself, and thereby eliminate the need to take the instrument out of service for a trip to the standards lab. If an instrument receives heavy use, the ability to calibrate it on location can save the cost of a backup unit. The covers can stay on, so critical analog components will remain at the temperatures they experience in actual operation. And unlike potentiome-

Incorporating an easy-to-use self-calibrator, *the 8½-digit Model 1281 DMM from Datron also has a separate voltage reference, as well as dividers based on transformer turns ratios.*

TABLE 1—REPRESENTATIVE HIGH-PERFORMANCE DMMs

MANUFACTURER	MODEL	DIGITS	SPEED (READINGS/SEC) MAX	AT MAX RESOLUTION[1]	AT 6½ DIGITS[2]	UNCERTAINTY[3] DC	AC	FREQUENCY RANGE FOR BEST AC ACCURACY	PRICE[4]
DATRON	1061A	6½	35	1.5	1.5	30+80	1000+3000	45 Hz TO 2 kHz	$4140
	1281	8½	150	0.04	35	7.5+4	90+200	40 Hz TO 10 kHz	$7950
FLUKE	8506A	7½	500	5	500	15+70	250+0	40 Hz TO 20 kHz	$6265
HEWLETT-PACKARD	3457A	7½	1350	0.25	53	35+190	2300+2800	100 Hz TO 20 kHz	$2800
	3458A	8½	100,000	6	8000	8+1	80+200	45 Hz TO 1 kHz	$6000
KEITHLEY	193A	6½	25	25	25	80+300	2500+10,000	50 Hz TO 10 kHz	$2395
	196A	6½	1000	0.3	9	80+300	1500+10,000	200 Hz TO 10 kHz	$1395
RACAL-DANA	SERIES 6000	6½	34,000	10	35	30+100	800+7000[6]	100 Hz TO 20 kHz	$5960
SCHLUMBERGER	7061	7½	1500	0.5	5	25+20	450+1500	40 Hz TO 10 kHz	$2995
	7081	8½	100	0.019	2.5	7+4	220+700	40 Hz TO 10 kHz	$7595
YOKOGAWA	2501A	6½	1.67	1	1	50+50[7]	700+3600[7]	50 TO 500 Hz	$6000+

NOTES:

SPECIFICATIONS SHOWN ARE ABBREVIATED. CONSULT MANUFACTURERS' DATA SHEETS FOR FULL SPECS.

1. SPEED SELECTED TO MINIMIZE UNCERTAINTY.
2. HIGHEST SPEED AT WHICH VENDOR CLAIMS 6½-DIGIT RESOLUTION.
3. ±(PPM OF READING+µV), 10V RANGE, 1 YEAR, 18 TO 28°C
4. US LIST. EQUIPPED FOR DC/AC VOLTS AND RESISTANCE. IEEE-488 IS INCLUDED, EVEN IF OPTIONAL.
5. AVERAGE FROM 2^0 TO 2^{17} READINGS. WITH 60-Hz LINE AND 2^{17} SAMPLES AVERAGED, READING TIME IS 546 SEC.
6. AC UNCERTAINTY GIVEN IS FOR SIX MONTHS. DATA SHEET DOES NOT INDICATE 1-YEAR SPEC.
7. UNCERTAINTY GIVEN IS FOR 90 DAYS. DATA SHEET DOES NOT INDICATE 1-YEAR SPEC.

ter settings, which could shift because of vibration or temperature changes, the digital correction values remain constant.

Although it may be simple to store corrections in a µP-based instrument, you will still need a calibration reference source. If your facility uses several high-performance meters, you might find it worth the investment to have a calibrator on the premises. Datron Instruments, now a subsidiary of Wavetek, provides an independent self-calibrator in the recently introduced Model 1281 8½-digit DMM. This calibrator uses an internal voltage reference that's separate from the meter's reference, and a voltage divider based on inherently stable transformer turns ratios.

Racal-Dana houses all components that can affect the calibration of its Series 6000 DMMs in a small module that a user can replace from the rear of the instrument. If you can't afford to relinquish the meter periodically for calibration, you simply stock a spare module. When it's time to calibrate, you don't send the meter to the standards lab—you swap modules. Schlumberger Instruments (formerly Solartron) provides lifetime calibration specifications for its 7000 Series DMMs. Schlumberger also publishes tighter specs for situations in which you calibrate the instruments on a periodic basis. Currently, few—if any—other instruments offer lifetime specs, independent internal calibrators, or interchangeable calibration modules.

If you maintain an on-premises calibrator, you must decide whether

TABLE 2—SPECIFICATION ABSTRACTS FOR REPRESENTATIVE CALIBRATORS

MANUFACTURER	MODEL	STIMULI PROVIDED	AMPLITUDE RANGE	FREQUENCY RANGE	BASIC ACCURACY[1] [±(% SETTING+% RANGE) EXCEPT WHERE OTHERWISE NOTED]
BALLANTINE[3]	1620A-OPT20[2]	DC CURRENT AC CURRENT	20 µA TO 100A 20 µA TO 100A	DC DC TO 10 kHz	±(0.02%+0.02%) ±(0.15%+0.1%)
	6400A-OPT84	AC VOLTS AC CURRENT	10 µV TO 1100V 9 µA TO 2A	10 Hz TO 1 MHz 10 Hz TO 5 kHz	±0.0375% ABSOLUTE ±(0.035%+0.01%)
DATRON[3]	4000A	DC VOLTS DC CURRENT RESISTANCE	100 µV TO 1000V 100 µA TO 1A 1Ω TO 10 MΩ	DC DC —	±(0.0007%+0.000025%) ±(0.005%+0.0005%) ±0.001% SETTING
	4700A	DC VOLTS AC VOLTS DC CURRENT AC CURRENT RESISTANCE	1 nV TO 1100V 90 µV TO 1100V 9 µA TO 2A 9 µA TO 2A 10Ω TO 100 mΩ	DC 10 Hz TO 1 MHz DC 10 Hz TO 5 kHz	±(0.0015%+1 µV) ±(0.018%+0.004%) ±(0.01%+0.001%) ±(0.035%+0.01%) ±0.002%
DOWTY RFL	829M	AC VOLTS DC VOLTS AC CURRENT DC CURRENT RESISTANCE	20 nV TO 1100V 20 nV TO 1100V 200 pA TO 2A 200 pA TO 2A 10Ω TO 10 MΩ	10 Hz TO 20 kHz DC 10 Hz TO 1 kHz DC	±(0.02%+0.03%+70 µV) ±(0.002%+0.003%+5 µV) ±(0.03%+0.03%+1 µA) ±(0.01%+0.01%+0.01 µA) ±0.005%
ELECTRONIC DEVELOPMENT	520A	DC VOLTS	0.1 TO 1000V	DC	±0.002% SETTING
	4503	AC VOLTS	10 nV TO 111.111V	10 Hz TO 100 kHz	±(0.04% +0.004%)
FLUKE[3]	5200A-05	AC VOLTS	1 mV TO 100V	10 TO 100 kHz	±(0.02% SETTING+10 µV)
	5205A	AC VOLTS DC VOLTS	TO 1100V TO 1500V	10 TO 100 kHz DC	±0.05% GAIN UNCERTAINTY ±0.05% GAIN UNCERTAINTY
	5215A	AC VOLTS	TO 1100V	10 TO 100 kHz	±(0.04%+0.002%) GAIN UNCERTAINTY
	5440B/ 5442A	DC VOLTS	0 TO 1100V	DC	±(0.00035%+5 µV)
	5450A	RESISTANCE	1Ω TO 100 MΩ	—	±0.0012%
KEITHLEY	263	DC AMPS DC VOLTS CHARGE	50 aA TO 20 mA 5 µV TO 20V 0.5 fC TO 20 µC	DC DC —	±(0.025%+0.005%) ±(0.0125%+0.0025%) ±(0.5+0.005%)
ROTEK[3]	610B	DC VOLTS AC VOLTS DC CURRENT AC CURRENT RESISTANCE	1 µV TO 1000V 10 mV TO 1000V 1 nA TO 10A 100 µA TO 1A 1Ω TO 10 MΩ	DC 40 Hz TO 20 kHz DC 40 Hz TO 20 kHz	±(0.002%+0.001%) ±(0.025%+0.0025%+10 µV) ±(0.02%+0.002%+50 nA) ±(0.05%+0.005%) ±0.005%
	710A	DC VOLTS AC VOLTS DC CURRENT AC CURRENT RESISTANCE	1 µV TO 1000V 1 mV TO 1000V 1 nA TO 1A 10 µA TO 1A 1Ω TO 10 MΩ	DC 10 Hz TO 100 kHz DC 40 Hz TO 20 kHz	±(0.002%+0.0002%) ±(0.025%+0.0025%) ±(0.02%+0.002%+50 nA) ±(0.05%+0.005%) ±0.02%
VALHALLA[3]	2701C	DC VOLTS	1.2 TO 1200V	DC	±(0.0008%+0.0001%)
	2724A	RESISTANCE	100 µΩ TO 11 GΩ	—	±0.0007%+2 mΩ

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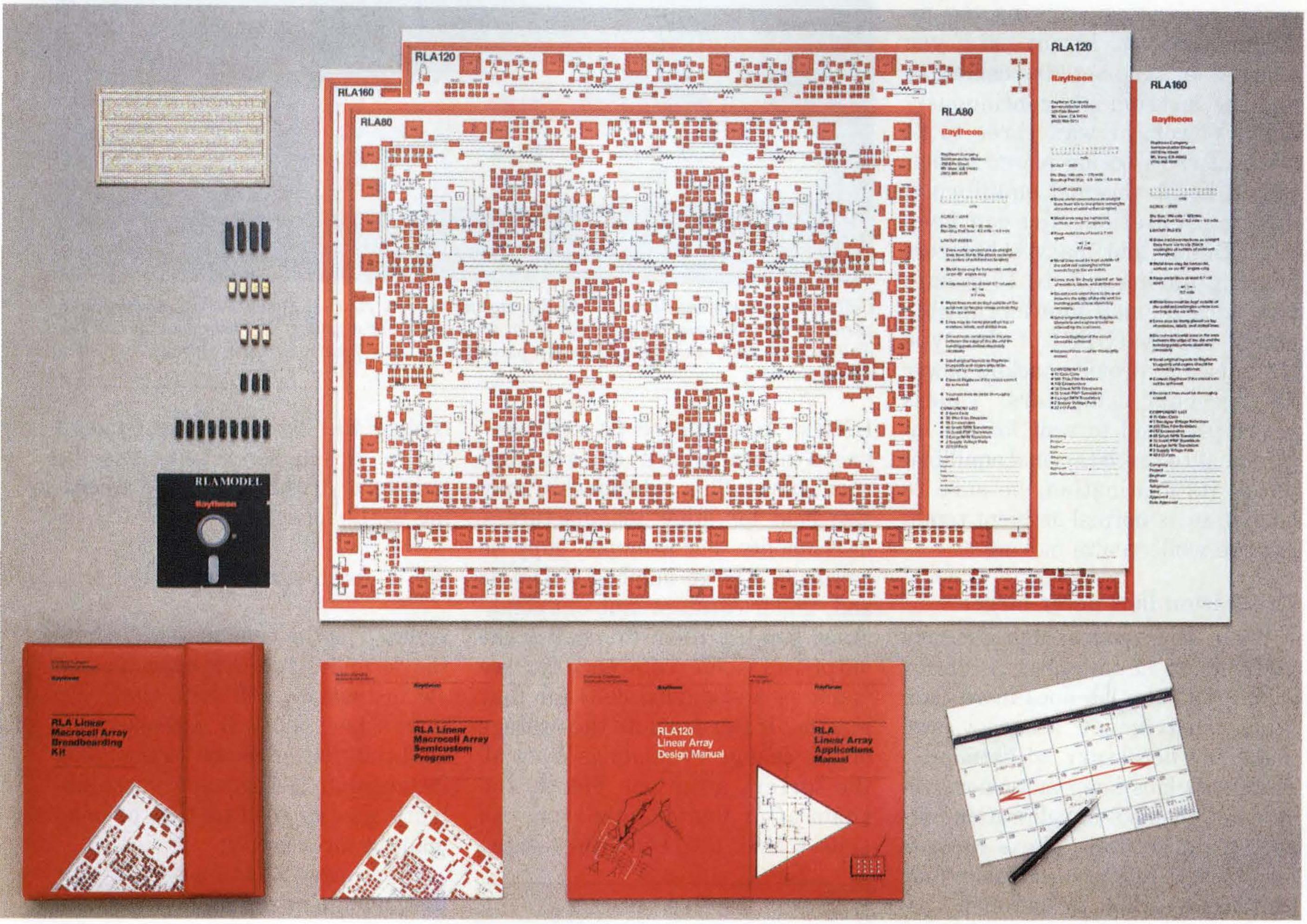

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[1]PSPICE is a trademark of MicroSim Corporation.
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Access to the right technology

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CIRCLE NO 102

you will bring it to the instruments you're calibrating or bring the instruments to it. In any case, you must either keep both the calibrator and the instruments continuously under power, or wait three to 24 hours after restoring power so that they'll be at thermal equilibrium during calibration. You can keep most DMMs and many calibrators running during a 5- to 15-minute trip with a small uninterruptible power supply (UPS) of the type often used to provide backup power for personal computers. Unless you're prepared to wait for the instrument to reach thermal equilibrium at its destination, be sure to keep it at its normal ambient temperature while you're moving it.

Called a "system multimeter" by its manufacturer, *Hewlett-Packard, the Model 3458A performs 100,000 conversions/sec at 16-bit resolution. For a year after calibration, on its 10V dc range it delivers 8½-digit readings accurate to 8 ppm of reading plus 1 μV at 6 conversions/sec.*

Calibration labs never forget

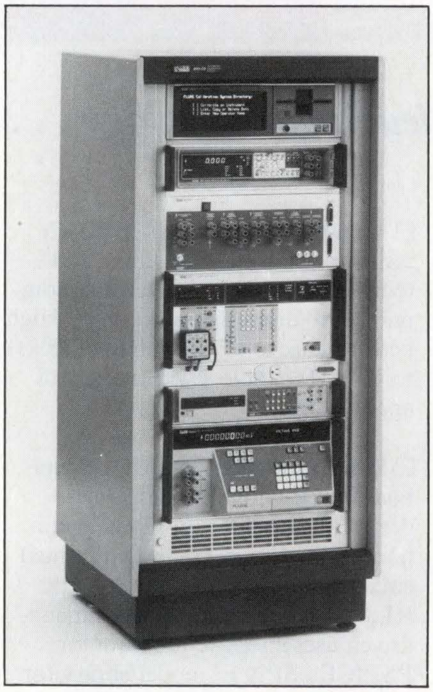
When you send a high-accuracy instrument to a standards lab for calibration, the lab does more than verify instrument accuracy and make the necessary adjustments. Standards labs keep meticulous records of changes in calibration corrections over time. These records form a part of the mechanism that establishes a link to nationally accepted reference standards. For example, the records serve to substantiate a claim that the accuracy of the product you're testing is traceable to the National Bureau of Standards (NBS).

If you perform on-site equipment calibration and fail to keep good records, you may be unable to provide satisfactory evidence of traceability, even though the accuracy of your measurements might be acceptable. Several calibrator manufacturers offer personal-computer-based software packages to facilitate the maintenance of calibration records. If traceability is important to you, you should consider adding a personal computer and calibration record-keeping software to your on-site calibration system.

Schlumberger Instruments has studied how calibration corrections change over time in its Series 7000 DMMs. A very good fit exists between calibration drift and a square-root curve. This relationship may also hold for other manufacturers' instruments. For example, suppose you have a large number of DMMs and, under constant ambient conditions, you use them to monitor the output of some reference source (such as a standard cell) for four months. If you compute the average of the change in readings from all the meters after one month and again after four months, you can expect that the 4-month-average change will be double the 1-month figure. Schlumberger specifies the long-term drift of its DMMs according to the formula

$$\text{(ppm of reading)}/\sqrt{T},$$

where T is the time in years. From the formula, you can infer that an old instrument will drift much less than a new one will. However, it's doubtful that anybody was building instruments 10 years ago whose stability was as good as that of units manufactured today.



This computer-controlled, mobile, configurable calibration station *is Fluke's Model A123. You can bring the station to the instruments you need to calibrate.*

If you need all the accuracy your instrument's vendor specifies, and you rely on an off-site standards lab for calibration services, you'd be well advised to determine how closely the operating environment in which you use the instrument approaches the standards-lab environment. In a well-run standards lab, temperature and humidity are under much tighter control than they are in a typical R&D lab or production-test area. Furthermore, when high-accuracy instruments are in actual use, it's quite common to see other instruments stacked on top of them, or to find them tilted at an angle that makes it easier to view the display.

Stacking instruments that dissipate a significant amount of power on top of a high-accuracy meter, or operating a meter or calibrator in a position different from that which its designers intended, can upset the meter's calibration. If these re-

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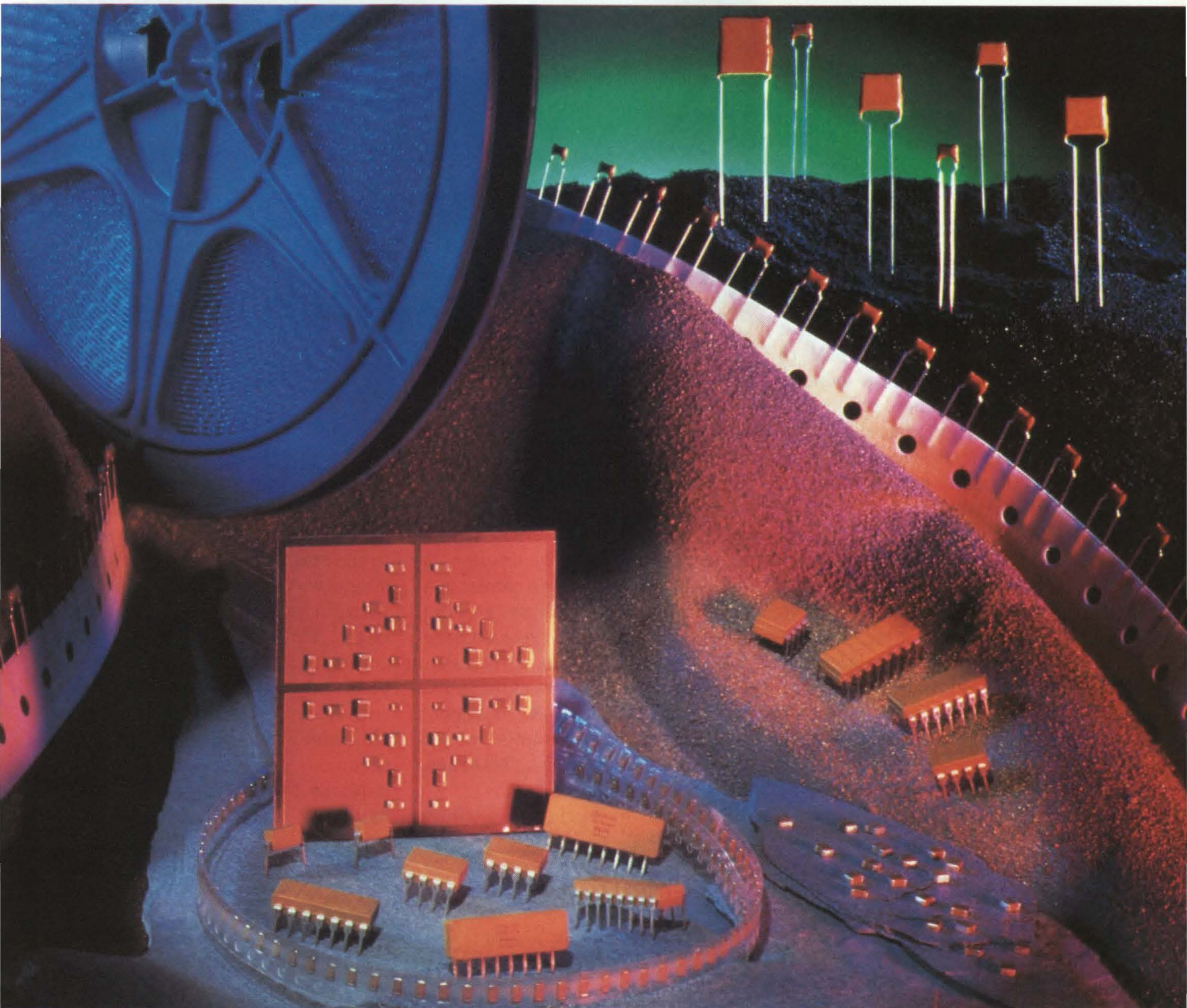
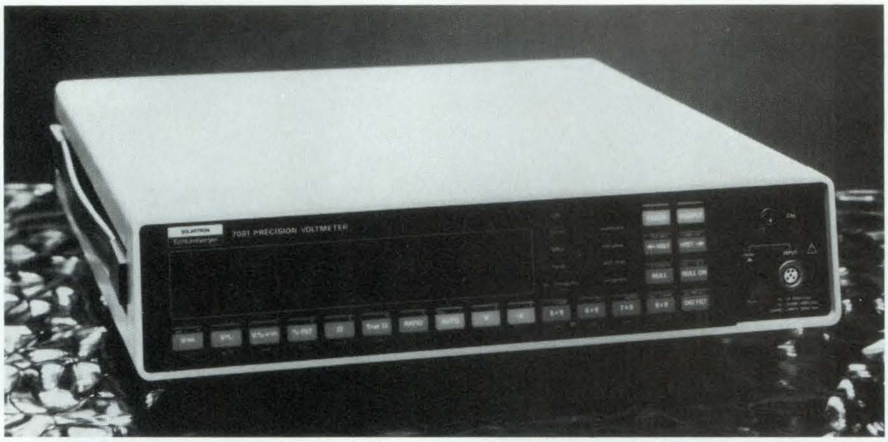


4SZ-7123

strictions appear to place unreasonable constraints on your use of high-accuracy instruments, consider obtaining instruments that you can calibrate right where you use them, and calibrators that you can bring to them.



A rarity in the DMM marketplace, lifetime calibration specs *are the hallmark of Schlumberger's Series 7000 DMMs. After nine years of use, measurement uncertainty is specified at three times the 1-year figure.*

Transfer mode enhances accuracy

An alternative to performing a full on-premises DMM calibration is to use the meter in "transfer mode." You can obtain extremely accurate readings if you first determine a correction by using the DMM to measure a quantity whose value is accurately known. Then, under constant conditions and after a minimal delay, you apply the correction to the measurement of an unknown quantity whose value is very close to that of the accurately known quantity. Some vendors publish separate specs covering the use of DMMs in transfer mode; as you might expect, transfer accuracy is even better than absolute accuracy 24 hours after calibration if the meter's temperature is held within ±1°C of the calibration temperature.

To measure ac voltages, DMMs convert ac voltage to dc and then measure the dc voltage. As with dc current, when a DMM measures ac current it first converts the current to a proportional voltage. Today, nearly all high-accuracy DMMs having ac ranges either use or offer the option of true rms-to-dc conversion, as opposed, for example, to sine-wave-calibrated, half-cycle average-to-dc or peak ac-to-dc conversion. However, it really isn't sufficient to characterize the ac-to-dc conversion technique as true rms-to-dc conversion. The latter process embraces several circuit approaches.

With the exception of a single specification, crest factor, vendors specify DMMs' ac-measurement accuracy for sine-wave inputs only. Crest factor is the ratio of the repetitive peak value of an ac waveform to the rms value. The crest factor of a sine wave is 1.41. Many possible waveforms exist for a given crest factor. Therefore, attempts to characterize crest-factor error might yield only an estimate of the inaccuracy in measuring *your* nonsinusoidal waveform. (Crest-factor error is the difference between readings for a nonsinusoidal signal having a given fundamental fre-

NBS goes into the standard-volts business

Most engineers don't think of the National Bureau of Standards as being in the business of selling hardware, but in a very limited sense, NBS *is* in the hardware business. To maintain NBS traceability, standards laboratories have, for decades, transported their dc-voltage references (unsaturated standard cells) to NBS facilities for periodic calibration. Because the cells are very fragile, labs can't entrust them to a common carrier, such as a package-delivery service. The usual practice is for someone from the lab to carry the cells *by hand.* If a flight is involved, the cells travel as passengers, not baggage. The process is obviously time consuming and expensive, and as the number of standards labs grows, existing NBS facilities might find themselves unable to handle the workload.

After 10 years of working on the problem, NBS in Boulder, CO, has developed a practical voltage standard that requires no calibration. Based on Josephson-junction technology, the standard uses an NBS-developed chip that operates at cryogenic temperatures. Clark Hamilton of NBS believes that organizations wishing to replicate NBS's setup can do so for about $100,000. If your company would like to own an inherently accurate voltage calibrator, write to Clark Hamilton at the National Bureau of Standards, Electromagnetic Technology Div MS 724.03, Boulder, CO 80303, or phone him at (303) 497-3740. If you can allocate funds to support a calibrator project, NBS will arrange for you to visit its facility. You can come away with the critical hardware items and the know-how you need to construct a standard like NBS's.

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quency and crest factor, and a sinusoidal signal having the same frequency and rms value.) Consequently, many DMM vendors merely specify the highest crest-factor signal their meters can accept without malfunctioning.

True rms is tough to measure

In theory, if you know all the frequency components and their respective amplitudes in a nonsinusoidal ac waveform, and you know the waveform's crest factor, you can predict how accurately a meter will measure the waveform's rms value. Don't count on making this prediction in practice, however. One reason why DMMs have difficulty in matching their sine-wave accuracy specs when measuring nonsinusoidal waveforms is that almost all of them, even those having thermal rms-to-dc converters, have active circuits in the signal path. These circuits have finite bandwidth and slew-rate capability, a limitation that can cause distortion and errors in measuring nonsinusoidal waveforms.

Bear in mind also that DMM accuracy is usually specified in terms of digits plus ppm of reading. For ac ranges, the vendor provides a table of specs covering different frequency bands. As the frequency rises, you'll find that both components of the error expression increase. The frequency dependence of the "digits" term implies that if you insist on making measurements at a small percentage of full scale, you'll experience degraded accuracy, particularly at higher frequencies.

Most high-accuracy meters provide a 4-wire ohms-measurement capability. The 4-wire, or Kelvin, configuration allows you to exclude the resistance of the current-carrying leads from the measurement. Another useful feature of some DMMs is a low-current ohms-measurement mode. At the expense of reduced accuracy, the low-current mode lets you limit the voltage across the resistor you're measuring. This ability might let you make a reasonably accurate measurement of the value of a resistor shunted by a diode, or it might minimize the self-heating of a temperature-sensitive resistor.

Translator software confers chameleon-like qualities *on Keithley's Model 193 DMM. By storing new command definitions in its nonvolatile memory, you can make the DMM's IEEE-488 vocabulary mimic that of competitive meters.*

Getting rid of noise

One of the prices you pay for high resolution in most DMMs is increased measurement time. Most of the high-accuracy meters will make faster measurements if you reduce the number of digits displayed. In a given instrument, increasing measurement time improves the repeatability of readings and allows a higher-resolution display. Truly random noise has a zero average value. Line-frequency-related "noise" (aka hum), averaged over an integral number of line cycles, also has a

For more information . . .

For more information on the DMMs, calibrators, and computer-controlled calibration systems described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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value of zero. The longer the period over which you compute the average, the more closely it will approach zero.

Most DMMs obtain noise rejection by using inherently slow integration, but some DMMs, such as Fluke's 8505A and 8506A, use a high-speed conversion technique and reject noise by averaging measurements. Although averaging large numbers of measurements can make such instruments very slow, Fluke's design lets you separately select the number of digits displayed and the number of samples averaged. Therefore, if noise doesn't invalidate the data represented by the digits of low significance, the instruments can make high-precision measurements at high speed.

Many meters allow you to switch in a normal-mode filter on dc ranges to improve the rejection of noise superimposed on the signal. If you opt to use the filter and attempt to make measurements at the meter's maximum rate, you'll probably find that after you change the input voltage, you must wait for several measurement periods to obtain a stable reading. The settling time of most such filters is greater than the DMM's measurement time.

All the DMMs and most of the calibrators discussed here offer an IEEE-488 interface, either as a standard feature or as an option. The commands you use to invoke specific functions vary from product to product—sometimes even within a single company's line. If you plan to control one of these instruments via the IEEE-488 bus, before you purchase the instrument be sure to ask the vendor for a manual that explains the programming language. Although you're unlikely to find that you *can't* program a particular instrument to do what you want, before you spend your company's money you should understand approximately what you'll have to do to write control programs for the unit of your choice.

To alleviate the problem of incompatibility among the command sets of different instruments, Keithley's Model 193, a 6½-digit DMM, includes a software package called Translator. This software lets you define a new command set for the 193—for example, to emulate a competitive instrument—and then store the command library in nonvolatile memory. If you're replicating an existing test system (for example, to increase capacity), the 193's user-definable command set enables you to substitute Keithley's meter for a competitive unit without rewriting the control software. **EDN**

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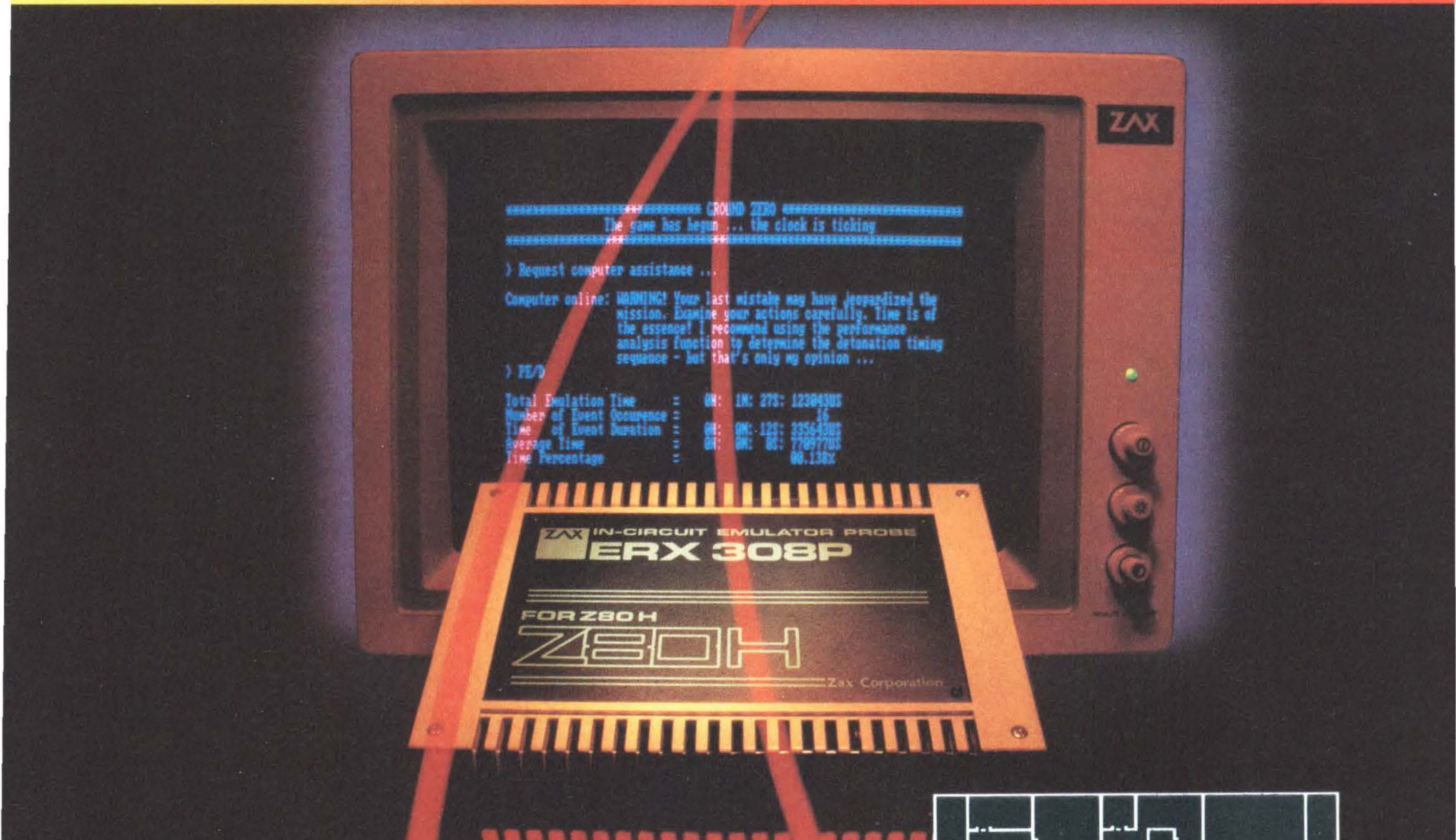
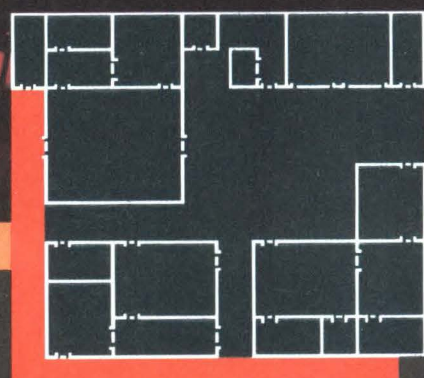


Diagram of Cramoisy Brigade camp. You'll need this to complete your mission.



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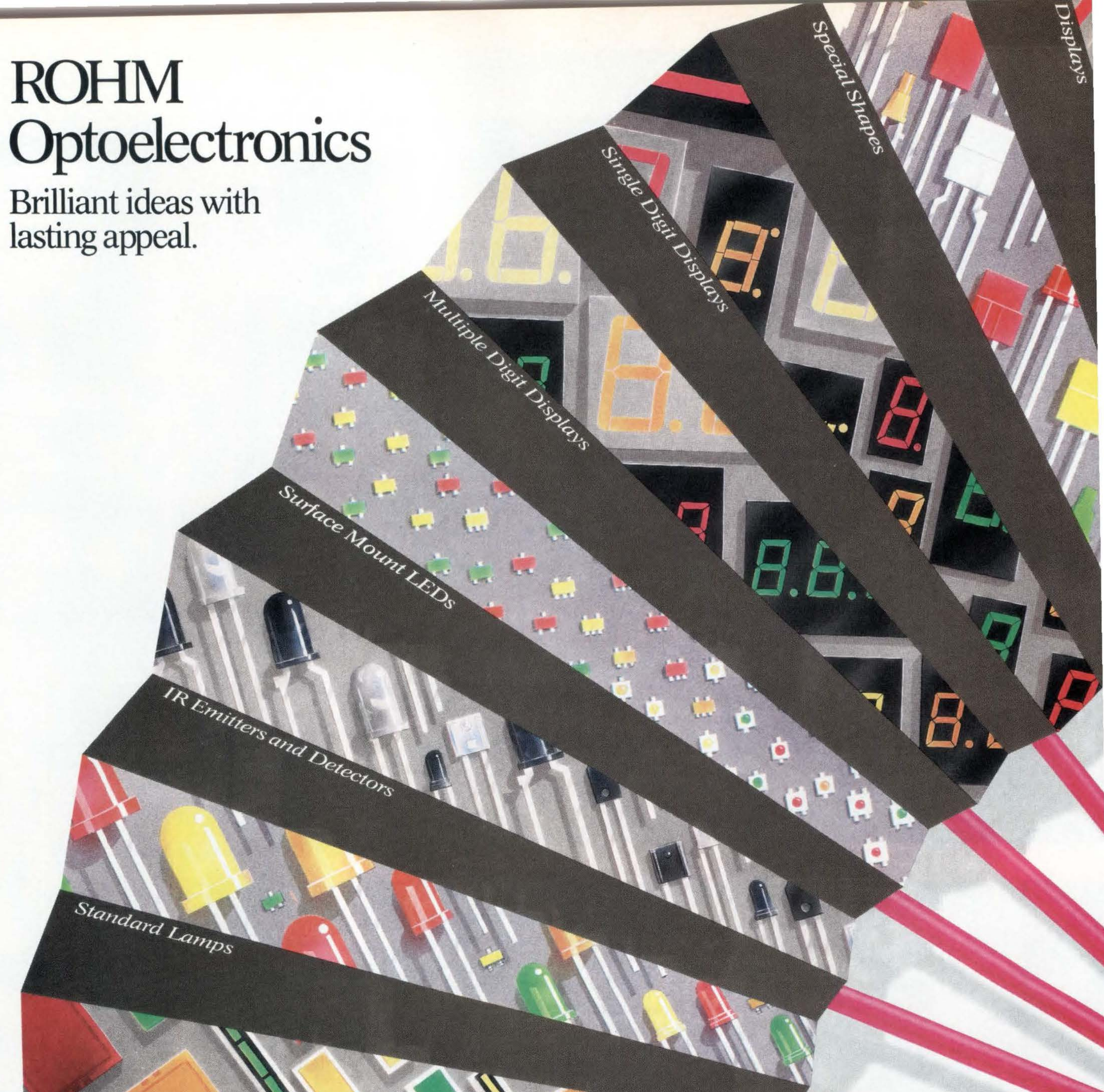

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CIRCLE NO 62

Innovations in monolithic display drivers improve flat-panel cost/performance ratios

Jim Wiegand, *Associate Editor*

Generally it's hard to beat the cost/performance ratio of complete flat-panel display systems, but you may have an application in which it makes sense to build, rather than buy, the displavs. There are driver ICs available that make it economical to configure flat-panel displays that meet your specific needs.

Consider an example of a build-vs-buy situation: If your product must operate in a harsh environment, then you must purchase and integrate the display's glass module and MIL-spec versions of the driver ICs. Also, the display configuration you need might not be available from high-volume manufacturers.

In such a case you must develop your own display. In this and similar applications, then, the best approach (although it might be counter-intuitive) is for you to purchase the glass panels and driver chips separately, then integrate them yourself. If you must build your own displays, it's useful to become acquainted with the various display-driver ICs and how you can use them.

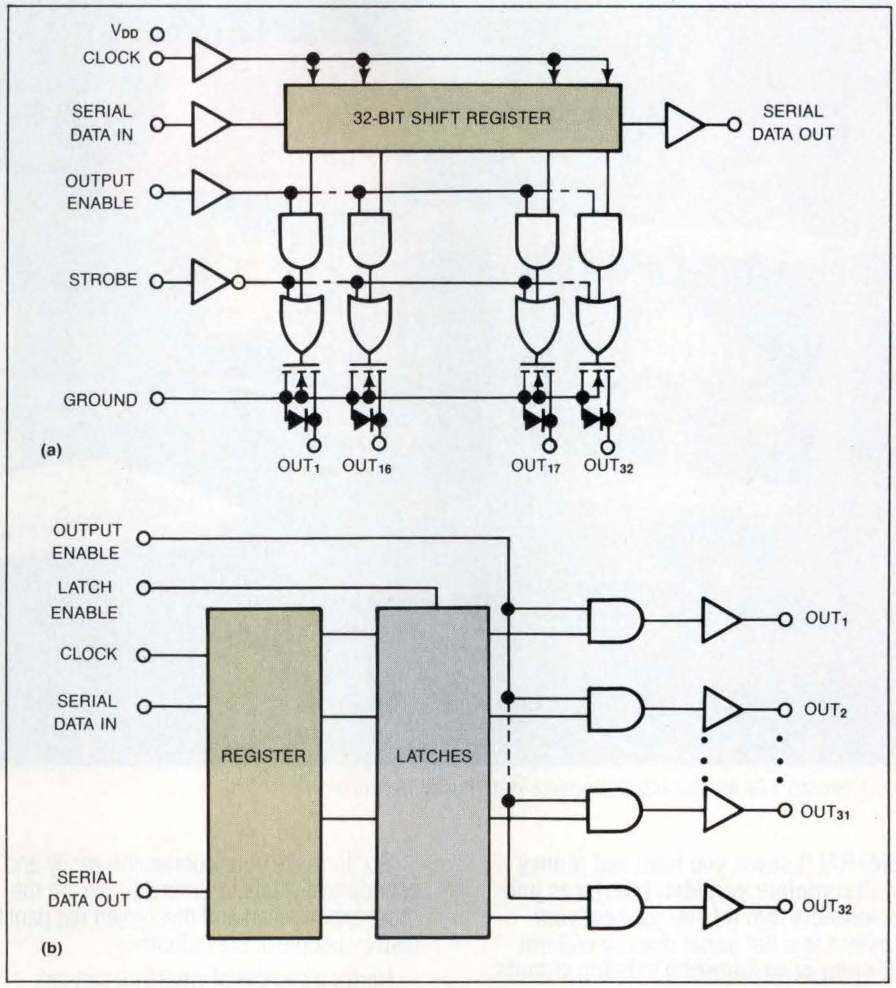

***Fig 1—The basic similarities of TFEL (thin-film electroluminescent) row (a) and column (b) drivers** are obvious in these block diagrams. The row drivers must, however, drive voltages as great as −225V, whereas the column drivers need to sustain only 60V at their outputs.*

Row and column drivers

Display drivers are generally configured to let you build displays in multiples of 20, 32, or 34 pixels. Drivers are of two types: row drivers and column drivers. The row drivers supply the negative high-voltage output (−200V or greater) necessary for driving thin-film electroluminescent (TFEL) displays; the column drivers provide the positive output (approximately 60V) required to bring the voltage on the designated pixel to the luminescence threshold level. (Most of the driver chips also operate with ac-plasma display panels, but that's beyond this article's scope.)

A row driver typically consists of a 20-, 32-, or 34-bit shift register having output-enable and strobe lines that you can use to turn all 20 (or 32 or 34) output lines on or off. You feed data into the shift register on a high-to-low clock transition, and a logical one put into a register causes its corresponding output to pull low.

In a typical application, you clock a single logical one through the shift register and pull each of the rows low one at a time by using the chip's output-enable signal. After a complete scan, you then pull the substrate's common pin high, thereby pulling all the outputs high. The block diagram of **Fig 1a** illustrates the structure of a typical row driver.

Like a row driver, a column driver (**Fig 1b**) contains a 32-bit shift register having a serial output that you

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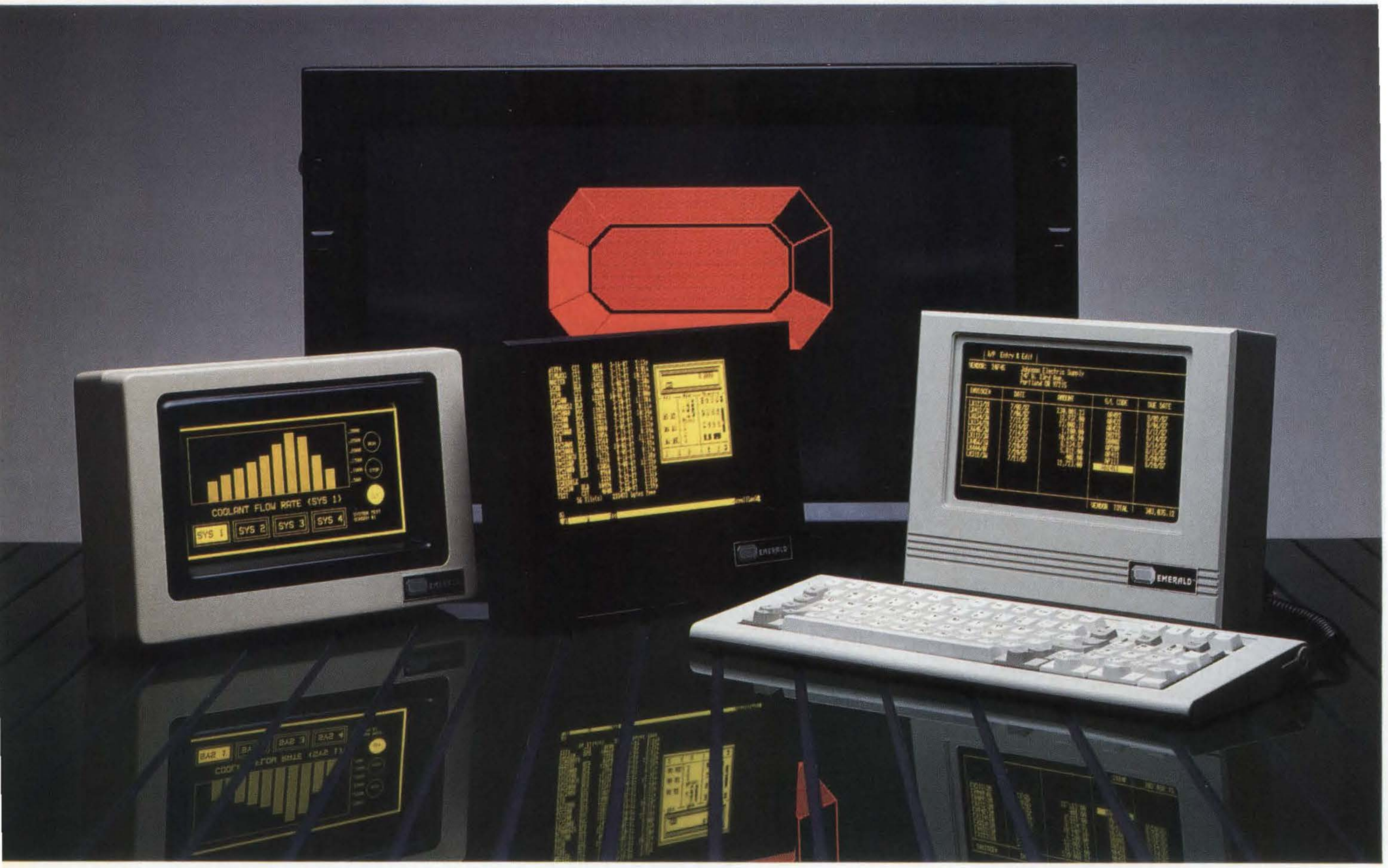

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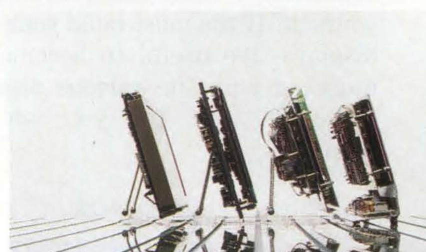

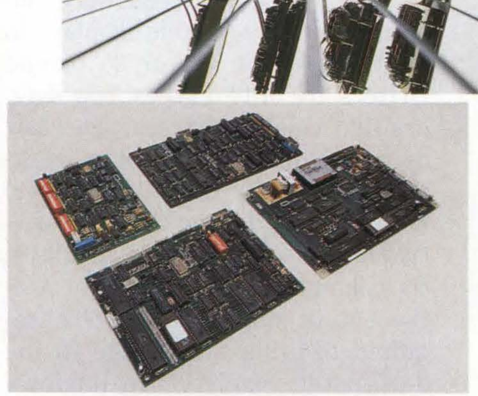

Interface and Controller Boards

CIRCLE NO 91

use to cascade column data into additional driver ICs. In the column driver, however, data enters the shift register on a low-to-high clock transition. A logical one turns on the corresponding output. In the on state, the driver's output sources current from its high-voltage Darlington stage, thereby producing an "on" pixel.

Column drivers also contain a 32-bit latch that lets you store currently displayed information while you clock a new set of data through the shift register. You transfer the data from the shift register to the latch by using the chip's latch-enable signal.

The configurations commonly available in these driver ICs let you readily build displays that have an overall configuration of 512×512 pixels, a popular display format. But suppose your application requires a 96×96-pixel display area. Such a configuration is uncommon, so it's not available in volume; therefore, you can probably produce such a display as inexpensively as the display manufacturers can. Furthermore, you'll need to use only three row drivers and three column drivers in your circuit.

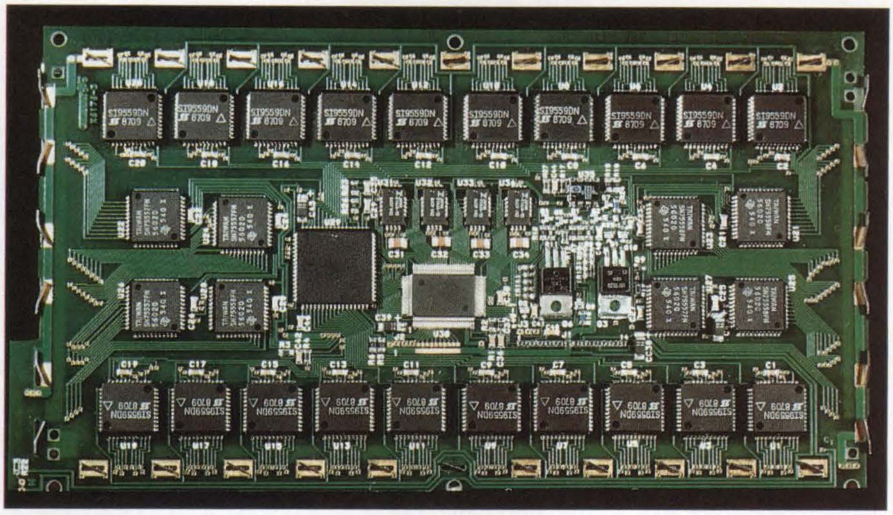

*Fig 2—**Packaging density is high in flat-panel displays,** as is evident in this photo of a board in one of Cherry Electric's dc TFEL displays. If you want to include your own peripheral circuitry along with a display-driver circuit like the one you see here, you should maintain high density to obtain the full economic benefit of the design integration.*

Home-brewed boards cut costs

One of the most compelling reasons to integrate your own display panels, however, is not to obtain an odd-sized display; rather, it is to combine your own peripheral-control circuitry with the circuits that drive the display. If your system is relatively simple (a μP, RAM, ROM, and minimal I/O, for example), chances are that you can include these chips on the display's pc board. Such an inclusion might seem to be an insignificant factor, but take a close look at your system's costs. You'll discover that this approach can reduce production costs significantly.

For example, suppose your system consists of interconnected control units, each of which requires a flat-panel display. You might implement the control circuits by using the previously mentioned μP, RAM, ROM, and a few ICs for I/O operations. Therefore, you could integrate this circuitry with the display-driving ICs on a practical-size pc board.

If you use two separate pc boards —one for the display and one for the control circuits—you'll be in for an unpleasant surprise at design-review time. Although the cost of the ICs (μP, ROM, etc) for your design may be as low as $30, don't forget the cost of the connectors, cables, standoffs, nuts, bolts, and assembly labor needed to construct a 2-board design. You'll quickly find that your product's cost is double or possibly triple the $30 cost of the ICs. So, combining the control and display-driver circuits on one board often makes economic sense. Now it's worth looking at several specific ICs that can help answer your display-driving needs.

A variety of driver ICs for TFEL-display panels is available from Texas Instruments. TFEL drivers include row (SN65563 and -4; SN75563 and -4) and column (SN65567 and -8; SN75567 and -8) drivers. The row drivers control 34 high-voltage outputs; the column drivers control 32 outputs. The chips employ BIDFET technology, which puts bipolar, double-diffused, n- and p-channel MOS transistors on one chip.

All inputs to TI's TFEL drivers are CMOS compatible. The sequence of the -4 devices' output lines is the reverse of that on the -3 devices. Similarly, the -8 devices' output-line sequence is the reverse of that on the -7 devices. The reversed-sequence availability greatly facilitates your board-layout task if you want to install these devices on both sides of your pc board or along all edges of a display module.

The row drivers are available with either open-drain or open-source outputs, which have ratings of 225V and 70 mA. The column drivers' totem-pole outputs are rated at 60V and 15 mA. Both the column and the row drivers feature serial inputs and outputs, so you can cascade the drivers easily for large-area displays. The 75563 and 75564 drivers, the most recently available of these ICs, cost $5.89 (1000).

Thin-film electroluminescent displays hold a great deal of promise for the future. A scrutiny of the ICs in Cherry Electric Corp's (Waukegan, IL) TFEL display **(Fig 2)** shows that Siliconix plans to help develop that market. In fact, Siliconix developed the Si9559 in conjunction with Cherry specifically for driving dc TFEL displays. The Si9559 constant-current column driver features 32 outputs, each rated at 90V and 15 mA. The chip costs $8.93 in quantities of 1000.

The company also offers the 34-output Si9560 electroluminescent symmetric row driver. Each output has a 235V push-pull structure that can source or sink 70 mA. Now available in prototype quantities, the Si9560 carries a price of $20.55 in 1000-piece quantities. In addition to the chips' intended application of driving flat-panel displays, Siliconix finds that they are being used in nonimpact printers, facsimile machines, and high-voltage line drivers. Those applications take advantage of the chips' high-voltage push-pull outputs.

Another source of TFEL display-driver ICs is the Semiconductor Group of Sprague Electric Co. Sprague manufactures the UCN5851 and UCN5852 BiMOS II TFEL row drivers and the UCN5853 and UCN5854 TFEL column drivers. The row drivers, rated at 225V and 120 mA, feature DMOS outputs. The column drivers offer totem-pole outputs that can source or sink 25 mA and can withstand 60V. The row driver and the column driver are both 32-bit devices that include clock, serial-input, serial-output, and output-enable lines. The 5851 and 5852 row-driver chips each cost $4.80 (1000).

To take full advantage of the TFEL drivers' features, be sure to consider your system's overall requirements. For instance, when a flat-panel display replaces a traditional CRT, the EL display's circuits usually use a raster-scanning refresh approach that is compatible with existing CRT systems. The refresh rates vary from 60 to 500 Hz. As you increase the refresh rate, you also increase the panel's power consumption and its brightness. At refresh rates lower than 500 Hz, the panel's brightness varies linearly with the refresh rate.

The scanning sequence for a TFEL panel begins with all columns grounded. All the rows then receive a positive refresh pulse from the row drivers. This refresh pulse may be as high as 225V in some systems (**Fig 3**). Next, the refresh signal turns on the row-driver IC; the row driver's outputs then follow the composite signal back to ground and allow the cell capacitances to discharge. The rows are left floating until each row is in turn selected by the row driver, which then drives the row to a negative potential.

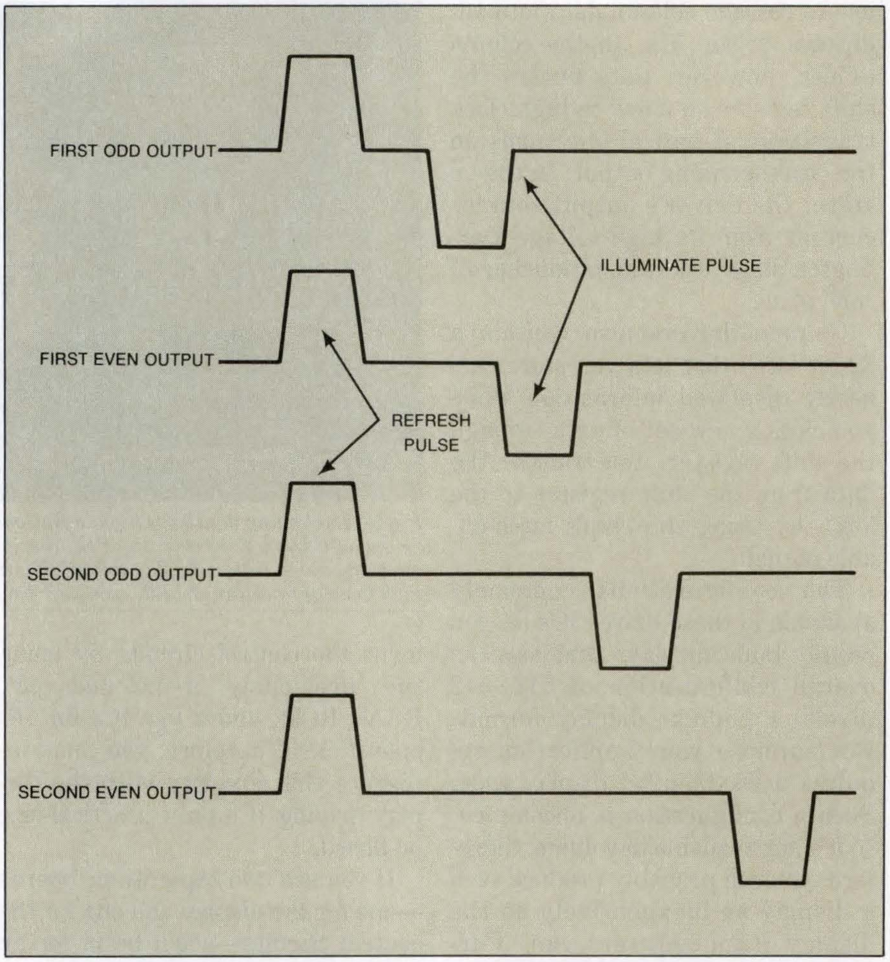

Fig 3—The output sequence that TFEL displays require *is illustrated here. Traditionally, the refresh pulses supplied to the displays have not been symmetrical, but if you design your circuit in such a way that the refresh pulses are symmetrical, you'll minimize the latent-image problem common with TFEL displays.*

You achieve the threshold voltage for light emission, approximately 210V, by driving the rows to −160V and then driving the columns to 50V. The difference between these outputs, 210V, is the voltage that appears across the cells you want to emit light.

Before you select a row, you must have the column data ready. First, you transfer the column bits into the column-driver chip's shift register and then latch the data for the output drivers. You can clock data for subsequent display lines into the shift register as soon as the current data enters the output latches. After the column and row bits are available, you enable the column drivers and force the row driver's output to a negative voltage.

Because the row-driver substrates are connected to the composite-row drive, you have to shift the logic levels of all the clock, data, strobe, and enable signals that connect to the row drivers. You can use optical isolators (logic levels on the inputs, high voltage on the outputs) to shift these signals. The column

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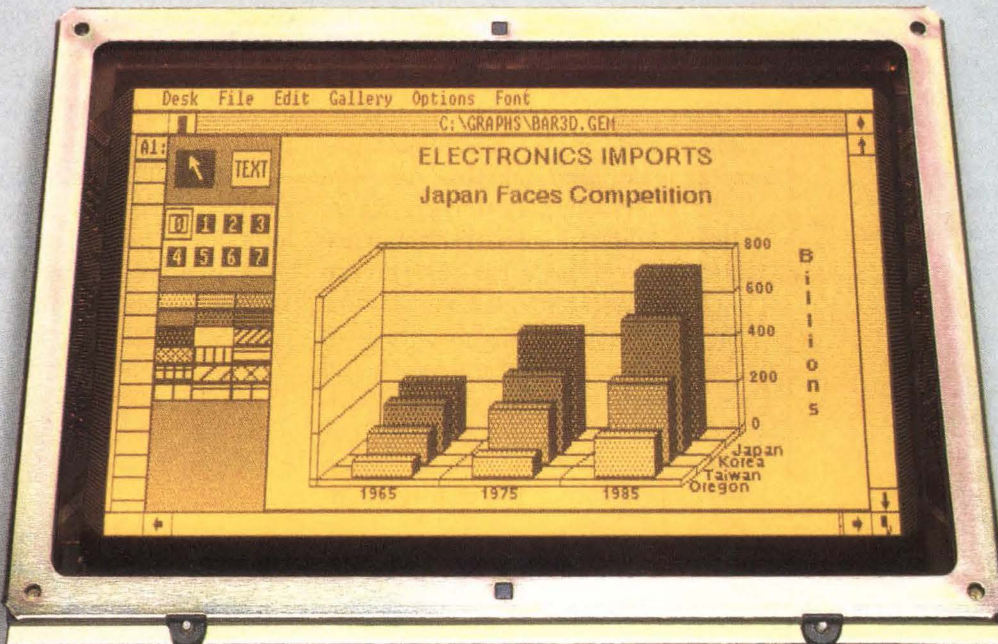

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drivers use ground as their reference; therefore, they don't require logic-level shifting.

Trouble in paradise

Beyond the architectural considerations previously discussed, you should be aware that TFEL displays have a tendency to display latent images. This latent-image problem—a differential-aging effect—results from using asymmetrical waveforms to drive the displays.

When TFEL-display panels are driven by an asymmetrical waveform, the pixels are driven by pulses of alternating polarity. Because the pulses, labeled illuminate and refresh, vary in amplitude and duration, as well as in polarity, a charge is left on the pixels. The charge can, in turn, "burn" pixels in the display. These burned pixels remain partially on, even when they aren't selected, causing latent images to appear on the display.

The key to solving the latent-image problem lies in eliminating—or at least compensating for—the asymmetric display-driving waveforms. Adding a compensation pulse both before and after the refresh pulse is one way to compensate for the asymmetry. The amplitude of these compensation pulses should be lower than the illumination-threshold voltage of the display, but their duration must be long enough to compensate for the charge buildup in the display.

Another compensation technique involves periodically moving the refresh pulse with respect to the panel's scan timing. This technique lengthens the time between the refresh pulse and the illuminating pulse, but it does so without degrading the displayed information. The extra time between pulses is long enough for the charge to bleed off each row, thereby eliminating charge buildup.

Although the described compensation methods reduce the differential-aging effect, such aging still takes place. By using a symmetrical-drive method—that is, if you drive each pixel with pulses of equal amplitude and duration but of alternating polarity—you eliminate the net dc charging of the pixels and, consequently, you eliminate burned pixels.

In addition, when you eliminate the refresh pulses, you improve the display's contrast ratio and reduce its power consumption. Until recently, however, you couldn't develop the symmetrical-drive waveform using integrated drivers, and using discrete-component drivers is an impractical approach.

To drive TFEL displays symmetrically, the row driver must combine logic-level input circuitry with 225V, 3-state output capabilities. Driver-IC manufacturers have just recently satisfied such output capabilities. The devices from Siliconix, Texas Instruments, and Sprague described here all fulfill these requirements. **EDN**

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For more information . . .

For more information on the display-driver ICs described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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Circle No 715

Sprague Electric Co
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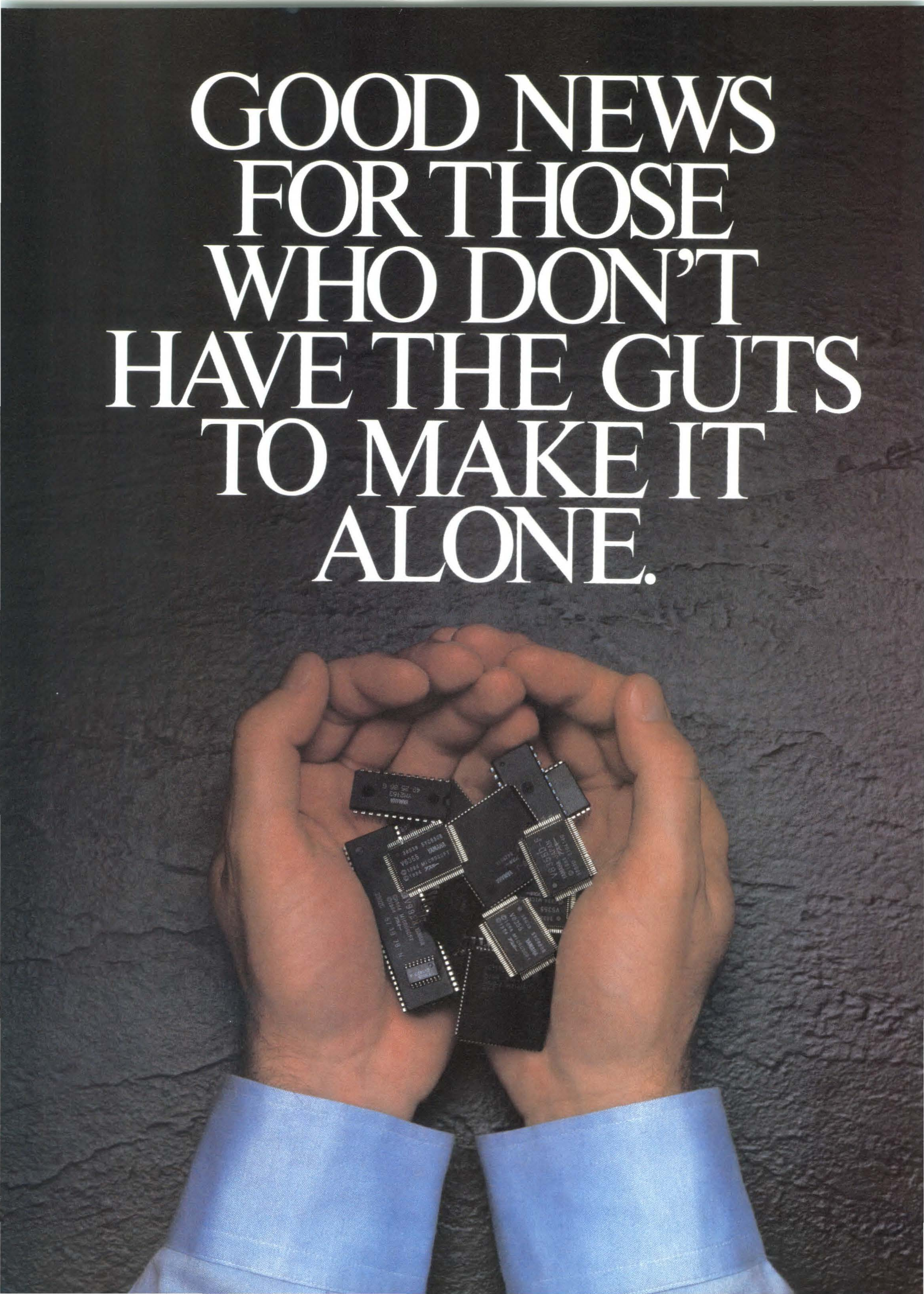
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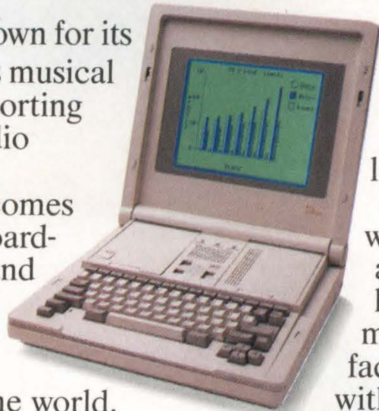

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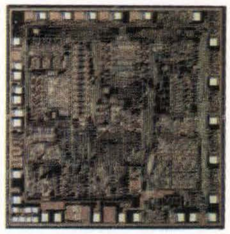

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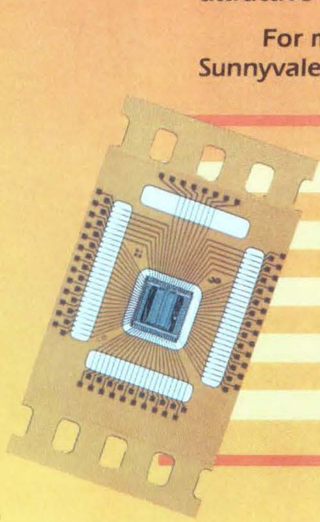

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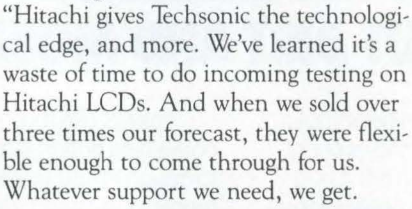

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CIRCLE NO 122

Plug-in boards let your personal computer perform parallel-processing tasks

J D Mosley, *Regional Editor*

Housing a maximum of four Transputers in a steel enclosure, *the Transputer Evaluation System (TES) from Sension Ltd lets you build a large Transputer network while monopolizing only one expansion slot in your PC.*

You can now select from a number of IBM PC-compatible expansion cards that give your desktop computer computational power approaching that of a Cray supercomputer. These cards each contain a μP that works in conjunction with the host CPU to execute software faster than a single μP could.

When you plug multiple processing cards into your PC or compatible computer, you increase the number of CPUs available for number crunching and problem solving. However, using such boards entails considerations that don't apply to the use of the typical Von Neumann serial-processing architecture found in most computers. The efficient use of multiple processors requires intelligent task parsing (process allocation) among the available processors as well as provisions for interprocessor communication.

The PC-based parallel-processing market is currently divided into three segments: boards based on Intel's 80386, ones based on Inmos's Transputer, and ones based on RISC (reduced-instruction-set computer) CPUs. Each has benefits and drawbacks, and your choice will depend on your application, on your programming skill, and on how receptive you are to learning new techniques.

If, besides writing multiprocessor applications, you also want to run several MS-DOS programs concurrently at the fastest possible speed, then you should consider the 80386-based cards. If you want to concentrate on parallel-processing development and prefer using a programming language designed specifically for that task, take a look at the Transputer boards and Inmos's Occam language. But, if your need for processing speed is greater than your need for programming flexibility, the RISC boards may be your best choice.

Although several expansion cards with an 80386 CPU are available, few are designed to work with the host CPU in your desktop computer. Expansion boards that require the removal of the host CPU are generally known as accelerator boards. The Inboard 386/PC from Intel Corp, for example, requires that you remove the host CPU from your PC/XT-compatible mother board, leaving the Inboard's 80386 μP as the sole processor—and obviously negating any chance for developing multiprocessing applications. You cannot link boards such as these together, either physically or with software, to provide a multiprocessing environment.

Conversely, coprocessor boards work in concert with the host CPU: The coprocessor performs CPU-intensive tasks, leaving the host CPU to perform housekeeping duties like I/O and task parsing. As a result, a coprocessor board doesn't accelerate such I/O tasks as display output, disk access, or printer control. For example, an 8088-based PC with a coprocessor board installed will execute a program slower than would a PC/AT-compatible or 80386-based host with the same board installed —the more I/O activity, the greater the difference.

In addition, though the coprocessor board can readily perform 32-bit-wide operations, to transport the results to you, the board must translate its 32-bit output into the 8-bit data patterns required for propagation along the host's bus. As a result, I/O-intensive MS-DOS software may actually run slower on a computer with a coprocessor board than it would on an unmodified PC.

To deal with this problem, Applied Reasoning Corp includes utility software with its PC-Elevator 386 coprocessor board that lets you decide whether to run an application on the coprocessor board or on the host CPU. So, even with the 386 board installed, you can run all of your MS-DOS application programs —even the ones with timing or

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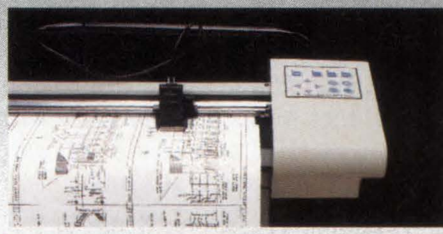

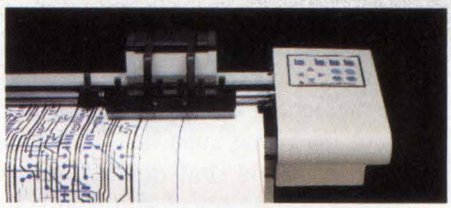

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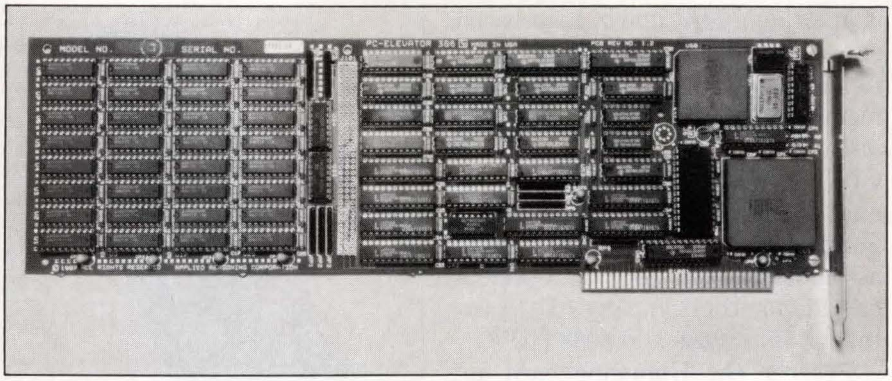
hardware sensitivity. A simple Up or Down command enables or disables coprocessor control.

In addition, you can plug as many as six PC-Elevator 386 boards into one PC-compatible computer. Thus, if you use an 80386-based PC for the host, you can tap the processing power of seven 80386 CPUs, which yields the potential computing power of 3.4 MIPS per processor. Each board sports a 16-MHz 80386 and 1M bytes of 100-nsec RAM with 4-way interleaving for zero-wait-state operation. The Norton index for this board is 18.7, which the manufacturer claims is 10 to 20 times the speed of an IBM PC/XT, 3 to 4 times that of an IBM PC/AT, and 10% faster than a Compaq 386.

You can add an extra 12M bytes of RAM by using as many as three daughter boards. Devoid of onboard ROM, the PC-Elevator 386 is controlled by disk-based software, which Applied Reasoning supplies. The manufacturer will provide PLAs to circumvent I/O-address limitations that ordinarily arise when you attempt to add more than four coprocessor boards to a PC host.



***You can pack six PC-Elevator 386 boards into a single PC-compatible computer** and still maintain MS-DOS compatibility. Applied Reasoning Corp provides PLAs that overcome the I/O address limitations likely to occur if you install more than four boards in your computer.*

The host computer uses eight consecutive I/O locations for coprocessor control, and it uses a 64k-byte window to read from and write to the onboard memory. An 8259 controls interrupt requests on board, but the host emulates all I/O and interrupt-acknowledge cycles. Therefore, the host's control program can detect error conditions in the coprocessor board and simulate any configuration of interrupt controllers. For $500, you can buy a software developer's kit that includes code and examples for programs that use more than one board for parallel-processing applications.

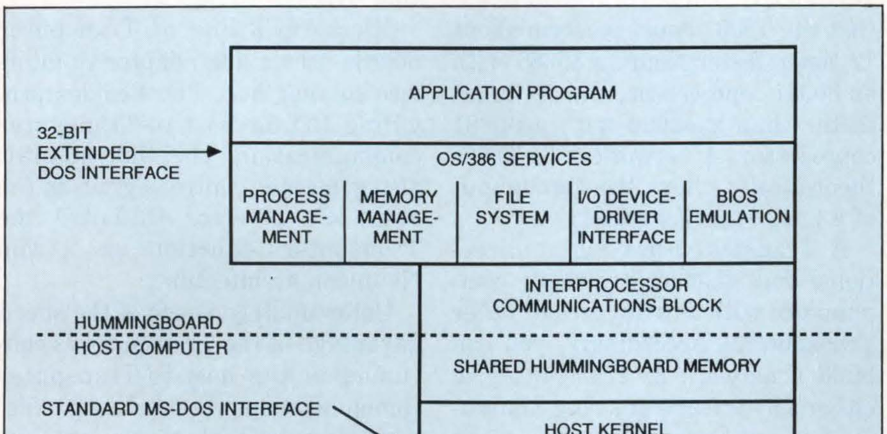
One program that the developer's kit includes and which illustrates the PC-Elevator 386's prowess in a multiprocessing application is based on the Mandelbrot set of complex numbers. Your computer displays this set as a 2-dimensional plane with an infinitely intricate border—a figure commonly referred to as a fractal and which is discussed at length in **Ref 1.**

Because the Mandelbrot set can offer an unending stream of computations, it's particularly well suited to illustrate the time savings attainable by applying more and more processors to the generation of the fractal pattern. This computationally intensive task presents an almost linear improvement in execution speed as you apply one to six boards to the problem.

The PC-Elevator 386 costs $1995; an 80387 arithmetic coprocessor adds $795; and each 4M-byte RAM daughter board costs $2000. For programming, you can use any language available for use with MS-DOS computers.

Another 80386-based coprocessor for PCs is the 386 Hummingboard from A I Architects. Using a 32-bit C language Dhrystone benchmark as a basis for comparison, the manufacturer claims that a 386 Hummingboard with a 20-MHz CPU runs 10.7 times faster than a 6-MHz IBM PC/AT running Microsoft C.

Best known as the hardware foun-



***The 386 Hummingboard includes a board-resident operating system called OS/386,** which provides extended, protected-mode 32-bit DOS services to applications running on the board. Developed by A I Architects, the OS/386 runs in conjunction with DOS, so you can run real- and protected-mode software simultaneously on the host and Hummingboard CPUs.*

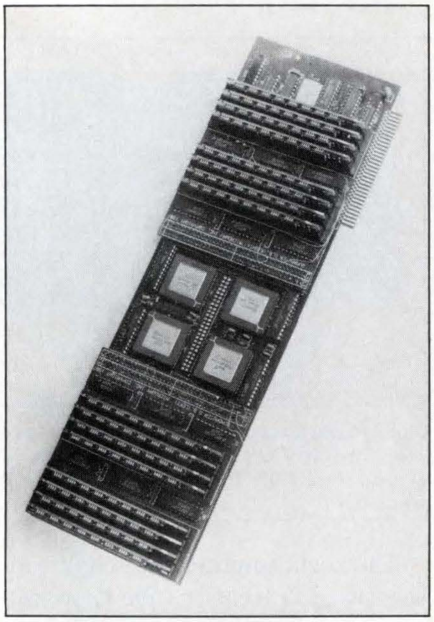
dation for Gold Hill Computers' (Cambridge, MA) line of Lisp-based expert-system software packages for artificial-intelligence development on PCs, the Hummingboard also runs in parallel with your PC's CPU. Software support includes 16- and 32-bit versions of C, Pascal, Fortran, and Ada, as well as an assembler and a software developer's kit for the company's DOS extenders for 80286 and 80386 μPs.

Because the Hummingboard appears to the host CPU as a dual-port EMS-compatible memory card, the design simplifies interprocessor communication through a shared memory scheme that provides the host μP with a 64k-byte window into the 24M bytes of 120-nsec physical memory that you can pack onto a single Hummingboard. The host μP controls I/O while the Hummingboard assumes central-processing control via its resident OS/386 DOS-extending operating system. As a result, certain MS-DOS programs that are sensitive to timing and hardware configurations may not run properly on a Hummingboard.

Although there is currently no software that specifically lets you use multiple Hummingboards in a PC for parallel operation, the company claims to have successfully installed four Hummingboards in a personal computer to execute a custom-designed application.

A 16-MHz 386 Hummingboard with 2M bytes of RAM sells for \$2895; a 20-MHz version costs \$3395. Pricing for a fully populated 24M-byte, 20-MHz 386 Hummingboard is \$18,950. You can add a \$695 16-MHz or a \$1195 20-MHz 80387 numeric coprocessor to the board, and you can select from several software options ranging in price from a \$495 software developer's kit to a \$895 32-bit C, Pascal, or Fortran compiler.

If you're looking for a board that's specifically designed to execute multiprocessing applications in a PC, you can select from a variety of



***Sporting four Transputers on one board,** the Quadputer from MicroWay provides as much as 10 MIPS per μP and suits parallel-processing applications. The board comes with an Occam-2 compiler for optimized program development.*

plug-in cards based on Inmos's T414 or T800 Transputer μPs. These 32-bit processors can crank out 10 MIPS, and the T800—which is a T414 with dedicated high-speed graphics functions and on-chip floating-point numeric processing—clocks in at 4 million Whetstones. Technically, these figures indicate that the T800 should perform about 12 times faster than an 80386 with an 80387 coprocessor, and six times faster than a 68020 with a 68881 coprocessor. A network of 64 T800s theoretically offers the throughput of a Cray supercomputer.

A Transputer has four bidirectional lines that let it directly communicate with as many as four other Transputers. Accordingly, you can build a network of Transputers in either a hypercube or a ring configuration to maximize efficiency in your multiprocessing application. Furthermore, these processors have 2k bytes of 50-nsec static RAM on chip, so each Transputer can execute a task independent of the other μPs and simultaneously share data stored in its on-chip RAM with the other processors in the network.

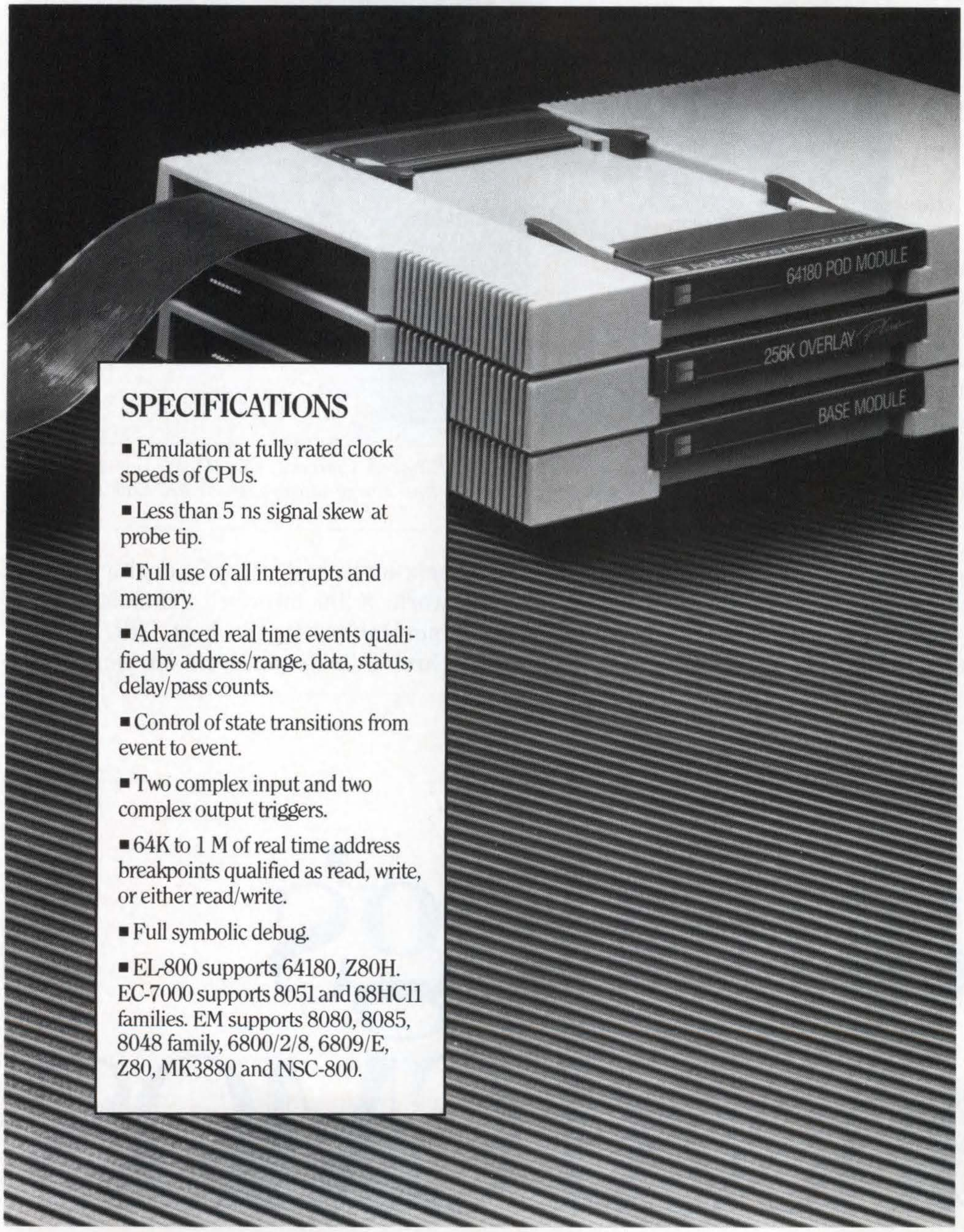
Converting your present programs for execution by a Transputer will require that you change compilers, because the Transputer's instruction set is completely different from the one that Intel uses. Accordingly, Inmos has developed the Occam assembly language for use with its Transputers. Specifically suited to the development of parallel-processing applications, Occam exploits the Transputer's interprocessor communication facilities, lets you specify which sections of code should run serially or in parallel, and supports time slicing for concurrent processing.

One company that gives you an Occam-2 compiler when you buy a Transputer board is MicroWay. Its single-Transputer board—the \$1495 Monoputer—comes populated with 2M bytes of 100-nsec RAM and a 20-MHz T414 Transputer. The T800 version costs \$1995. The company also offers Transputer-compatible compilers for C, Fortran, Pascal, and Prolog, however, which sell for \$750 each. In addition, MicroWay sells boards with either two or four Transputers at prices varying from \$3495 to \$8000. Memory upgrades range from \$1400 to \$5600 for 1M to 16M bytes of RAM.

MicroWay's line of Transputer boards uses a link adapter to interface to your host PC. Besides providing I/O for host-to-Transputer communication, the link adapter also generates control signals in the event of a μP error. On board, the Transputers function via a Von Neumann architecture.

Unfortunately, much of the speed advantage of the Transputer is consumed in the host-to-Transputer communication process. Using a file-server program that runs on your host PC under DOS, an Occam-2 program can only implement I/O functions such as reading the keyboard or writing to the CRT by passing messages to the Occam file server, which in turn passes them to the PC, which executes the task and relays the result via the file server

The first good reason in 5 years to buy new 8-bit development tools.



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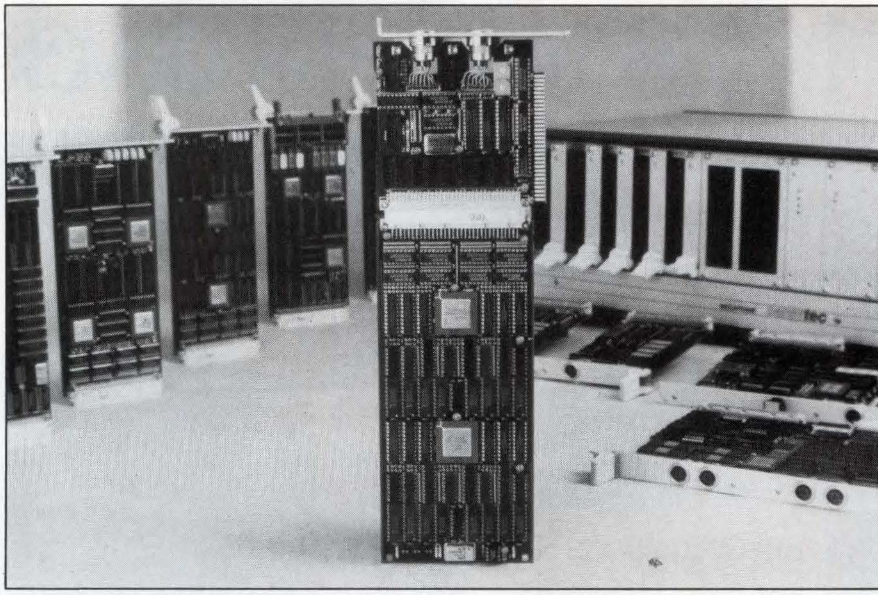
CIRCLE NO 41

back to the Occam program. MicroWay reports that an IBM AT with a Monoputer performs benchmark tests 50% faster than an 80386-based PC—not quite the speed advantage one would expect from its 10-MIPS CPU, but clearly a significant figure when you realize that you can theoretically network an infinite number of Transputers.

MicroWay prides itself on the software support it offers its customers. A $1500 Transputer Development System (TDS) provides an extra software layer that helps you link multiple boards by configuring a map of the system and determining what piece of code should go to which Transputer. The Occam language includes calls to access the TDS.



Convertible for use either with PC- or VME-based systems, *the Megaframe line of Transputer boards from Parsytec provides a bus-free, communications-oriented architecture for industrial computer systems.*

The Fast17 from Quintek Ltd sports seventeen Transputers on a single board to provide as much as 25M-flops processing power for your application. One Transputer, designated the master, has 4M bytes of local RAM for program code and data. The master controls a set of 16 slave Transputers coupled in a matrix-switched reconfigurable network. A link interface channels communications to the host CPU, and three 8-link connectors let you network the board to others. The Fast17 ranges in price from £12,050 to £16,450, depending on the Transputer you specify. The company also sells 4-Transputer boards; prices for these start at £3995.

Another company that offers multiple Transputers on a plug-in PC board is Definicon Systems. The $4990 DSI-T4 board has four Transputers and 1M bytes of RAM per computing section, and it comes with program development tools and a Parallel-C compiler with an assembler and linker. The package includes host server software, a macro assembler, a disassembler, and a debugging tool that lets you probe the memory of a specific Transputer. You can network these boards, but linking more than four boards requires the extensive use of jumper cables from an array of pins that line one long edge of the board.

Sension Ltd sells a Transputer Evaluation System (TES) that externally houses one to four T414s and 1M bytes of RAM and whose cost ranges from £1365 to £4750. A link-adapter board plugs into your PC to connect the TES cabinet to the host CPU. You have to purchase the software separately: A single-Transputer version of Occam-2 costs £300, and an Occam-to-IBM editor/compiler/configurer costs £1500 for a single-user license or £3000 for a multiuser system.

If you're considering parallel processing for an industrial application, you may want to consider the Megaframe/IBM board, which Parsytec has for sale. The basis of this company's line of Transputer boards is a set of Transputer modules that you can alter from VME Bus to PC bus compatibility by swapping interchangeable adapters, called bus bridges, which connect to the modules via a linking cable. The cable facilitates bidirectional signal transmission at a speed of 20M bps over a distance as great as 10m. The modules include boards with one to four Transputers, 1280×1024×8-dot graphics-display modules, a frame grabber, mass-storage controllers, and a 50M-byte/sec I/O interface. The Megaframe/PC adapter costs $595, and the Transputer modules sell for $1050 to $5650.

You can even purchase, from Levco, Transputer processor modules for your Macintosh II or SE computer. Priced at $2499 for the Mac II and $1899 for the Mac SE, starter kits include a Translink plug-in card, a 15-MHz Transputer module with 256k bytes of RAM, and a software tool kit. You can select from various other Transputer modules ranging in price from $1299 to $3499.

Finally, you also have the alternative of choosing a coprocessing board that uses a RISC processor instead of a full-featured µP. Acorn Computers' Springboard is marketed in the US for $2500 through VLSI Technology, and is built around a 32-bit Acorn RISC Machine (ARM) processor, which VLSI Technology manufactures. Because of the reduced number and simplified nature of the processor instructions available to RISC chips, such chips can execute code faster than standard μPs can. In addition, the ARM processor uses pipelined operation and hard-wired instruction decoding to further enhance the chip's performance.

The result is a plug-in board that performs twice as fast as the fastest Symbolics workstation, according to the manufacturer. Although the company primarily markets the Springboard for artificial-intelligence development, languages available for the board include ARM versions of C, Fortran, Lisp, Prolog, Basic, and Pascal—each priced at $500.

Another RISC coprocessor board for PC-compatible computers is the PC4000, which features a 16-bit Novix NC4016 RISC processor. Silicon Composers, the manufacturer of the PC4000, specifies the board's performance in the 4- to 8-MIPS range, or approximately twice the speed of a VAX 11/780. You can plug as many as six PC4000s into your PC, or more with an expansion chassis.

The PC acts as an I/O server, and the PC4000 has direct memory access to PC disks, I/O, and memory-to-memory transfers. Each board shares the PC bus and a minimum of 16k bytes of RAM with the host CPU to facilitate communications and data transmission. A 5-MIPS single-processor board costs $1295; a 6-processor 40-MIPS board sells for $9150.

The coprocessor boards that Opus Systems manufactures feature Intergraph's 32-bit, 33-MHz Clipper RISC chip and run Unix System V Release 3. The Personal Mainframe Series coprocessor boards provide processing speeds as fast as 5 MIPS (300PM models). Pricing for these models ranges from $3070 with 4M bytes of RAM to $6700 with 16M bytes. The price tag includes a C compiler and a Fortran-77 compiler, a device-driver library, and a real-time I/O executive that has provisions for scheduling, data management, and interprocessor communications. **EDN**

Reference

1. Dewdney, A K, "Computer Recreations," *Scientific American*, August 1985, Vol 253, No 2, pg 16.

Article Interest Quotient
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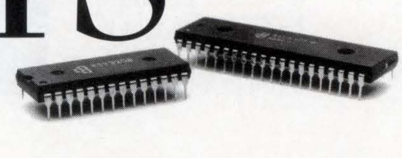

For more information . . .

For more information on the PC-based parallel-processing boards described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

A I Architects Inc
1 Kendall Square
Cambridge, MA 02139
(617) 577-8052
FAX (617) 577-9774
Circle No 701

Acorn Computers Ltd
Cambridge Technopark
645 Newmarket Rd
Cambridge CB5 8PB, UK
(0223) 214411
TLX 81152 ACNNMR G
Circle No 702

Applied Reasoning Corp
86 Sherman St
Cambridge, MA 02140
(617) 492-0700
TLX 6714194
Circle No 703

Definicon Systems Inc
1100 Business Center Circle
Newbury Park, CA 91320
(805) 499-0652
TLX 272849
Circle No 704

Levco Corp
6160 Lusk Blvd, Suite C-203
San Diego, CA 92121
(619) 457-2011
Circle No 705

MicroWay Inc
Box 79
Kingston, MA 02364
(617) 746-7341
TLX 503014
Circle No 706

MicroWay (Europe) Ltd
32 High St
Kingston-Upon-Thames
Surrey, KT1 1HL, UK
(01) 541-5466
TLX 9413790 MCRWAY G
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Opus Systems
20863 Stevens Creek, Bldg 400
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TLX 323114
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708 Mandrake Dr
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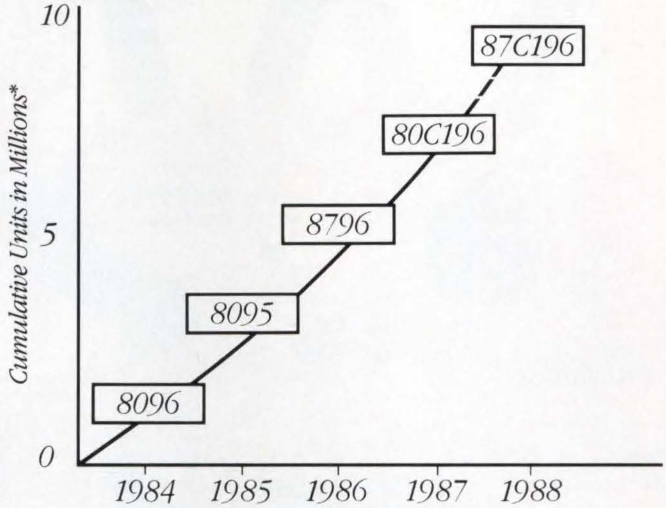

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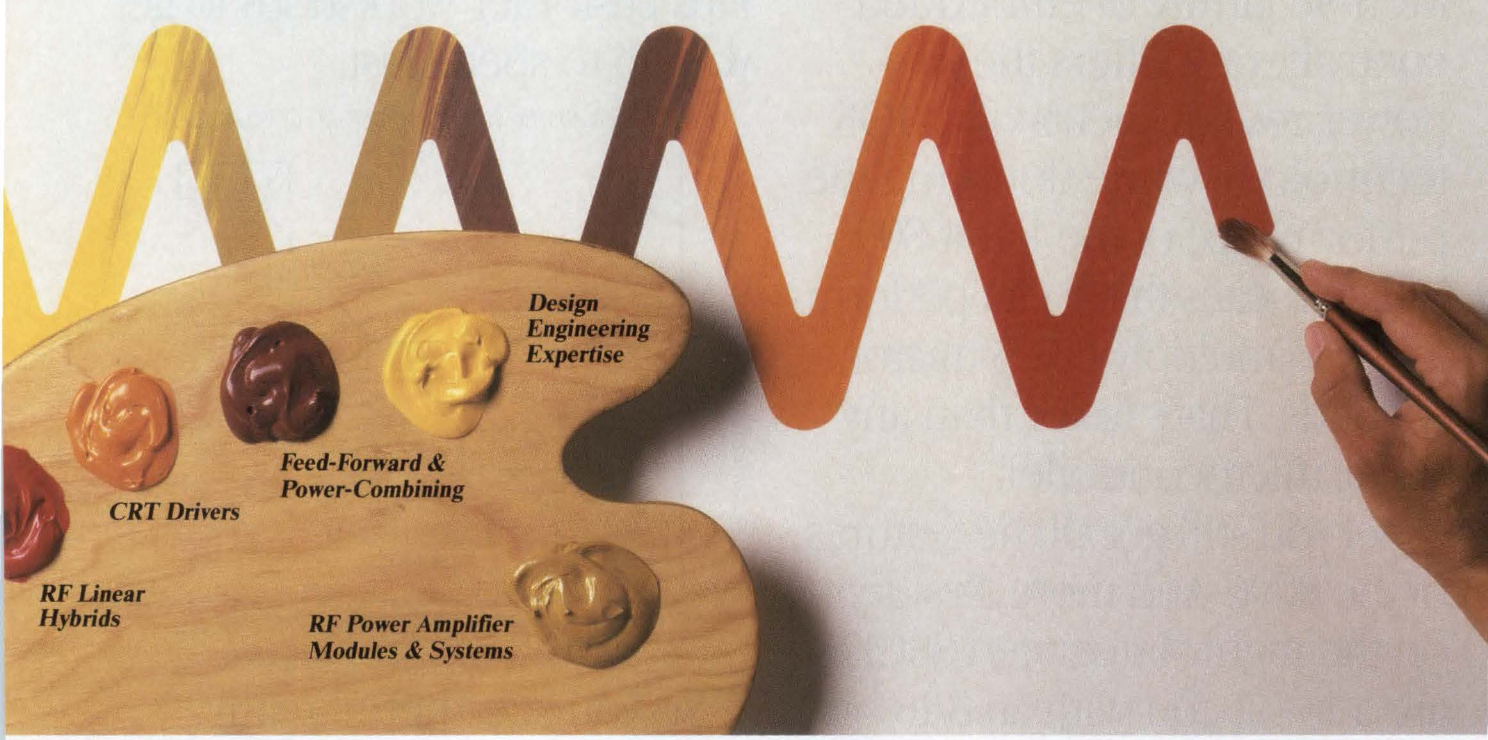

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CIRCLE NO 131

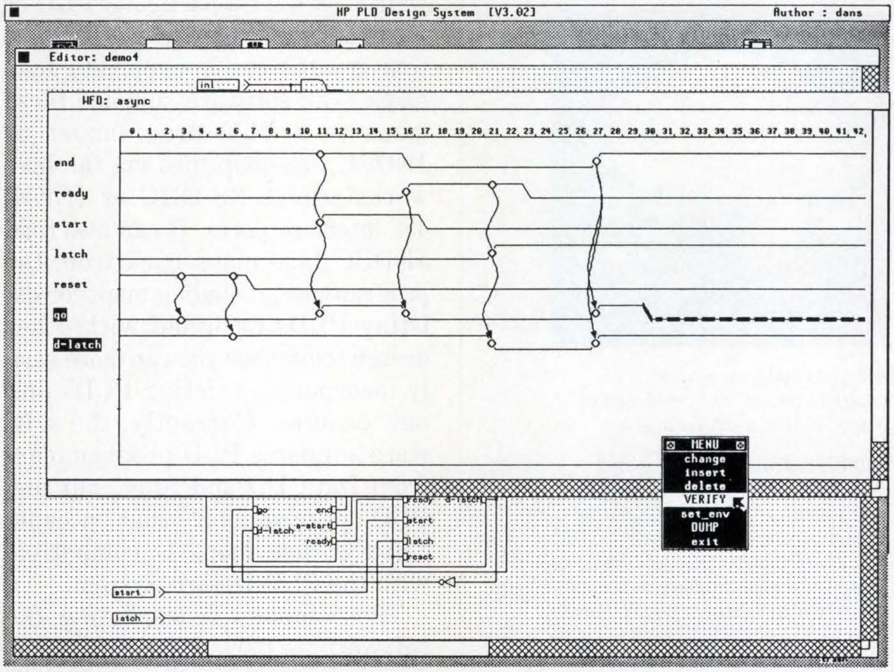
PLD design software accepts designs as schematics, waveforms, or tables

Featuring an interactive, graphics user interface, the Model 74150A PLD Design System software allows you to design PLD-based circuits by using any combination of Boolean equations, schematics, waveforms, or tabular data. The software runs on the company's Model 9000 Series 300 workstations. It takes your design, simulates the circuit's operation, checks for glitches, partitions the design to fit in one or more PLDs, and generates a fuse map and test vectors. You can select the target devices or use the software to automatically fit your design into appropriate PLDs.

The PLD Design System accepts circuit designs as schematics, state-transition diagrams, waveforms, Boolean equations, or truth tables. You can also take advantage of the software's hierarchical structure to break your design into modules and then use different design-entry methods to describe each module. In effect, the software allows you to match the design-entry method to the circuit or subsystem that you're developing.

The software's schematic editor provides an entry method similar to most CAD schematic-capture packages and allows you to attach simulated switches, oscillators, and logic probes to circuit nodes to aid debugging and verification efforts. A batch-mode debugger coupled with the schematic editor allows you to simulate your design's operation with input waveforms defined graphically in a separate stimulus file.

For synchronous circuit design, you can create state-transition diagrams (STDs) with a special STD editor that shows individual states as boxes linked with transition arrows. Pop-up transition tables allow



With the PLD Design System, you can design *PLD-based circuits by using either waveforms, schematics, or state-transition diagrams.*

you to enter state-transition conditions in tabular form. An interactive debugger coupled to the STD editor enables you to step through state transitions or to advance multiple states one at a time.

The software's waveform editor allows you to define a PLD, using timing diagrams that are especially useful for developing asynchronous circuits. The waveform display represents cause-and-effect relationships—causalities—using curved arrows that link the related waveforms.

The waveform editor and its debugger support six types of causalities: input edge to output edge, input value to output edge, input edge to output value, input value to output value, input edge and value to output value, and input edge and value to output edge. You can also define a PLD's structure with Boolean equations and truth tables, formats established by early PLD design tools. The PLD Design System minimizes equations automatically.

The software accepts designs without regard to a target PLD; this device independence allows you to try out various PLDs and find the most appropriate device for your design. You can also ask the PLD Design System to select the most appropriate device automatically from its PLD library, and you can narrow its choices by specifying parameters that pertain to your application—vendor type, inventory, or power consumption, for example. The PLD library currently contains device information about PLDs available from Altera, AMD, Intel, Lattice, Monolithic Memories, NEC, Ricoh/Panatech, Signetics, and VTI.

If your design won't fit into one PLD, the software allows you to partition the circuitry manually, or you can ask the software to perform the partitioning automatically. If your design has speed-sensitive signal paths, you can assign the critical signals manually and have the software to finish the job.

Once you've defined and compiled your design for a particular PLD or set of devices, the PLD Design System creates the appropriate fuse maps. The software supplies these maps to a PLD programmer as JEDEC fuse-map files via the host workstation's RS-232C or IEEE-488 interface ports. It can also read JEDEC fuse maps back from the programmer, including maps for existing PLDs designed with other design tools; thus you can more easily incorporate existing PLDs into new designs. Currently, the software supports PLD programmers from Data I/O and Stag, but any PLD programmer that accepts JEDEC fuse maps is compatible with the PLD Design System.

The company is marketing the software as part of its Electronic Design System, a collection of CAE software tools for electronics engineers. The PLD Design System exchanges circuit and simulation data with the other software tools in the Electronic Design System, using a proprietary representation format for schematic information and GenRad-compatible HILO-3 data files for simulation data. This data interchange allows the PLD Design System to convert circuits (or portions of circuits) designed with the Electronic Design System into PLD designs; it also allows more complete simulation of PLD designs by the Electronic Design System package's HILO simulator.

The PLD Design System costs $8000 to $14,500, depending on options. You can expect delivery approximately 12 weeks ARO.

—Steven H Leibson

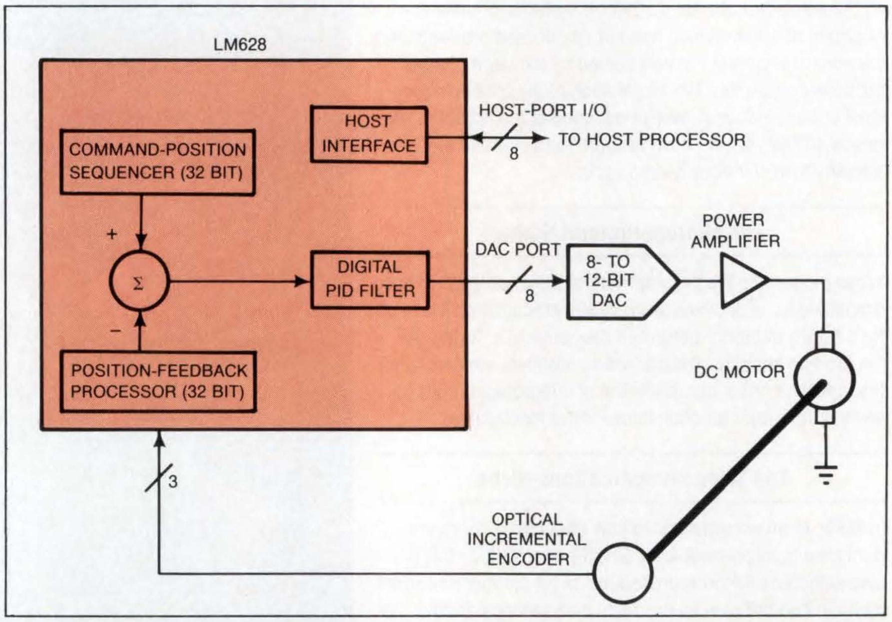
Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 700

Digital precision motion controller simplifies control of dc motors

The LM628 motion-control processor simplifies the control of dc and brushless dc motors by performing real-time computational tasks. Using this motion-control processor, you can build a servo system that requires only a dc motor, an optical incremental encoder, a DAC, and a power amplifier. A host processor controls the system via an 8-bit I/O port that uses a byte serial format wherein the data words follow the command word.

The host processor programs a trapezoidal velocity profile and a digital compensation filter. The trapezoidal velocity profile defines the operation of the motor in terms of maximum acceleration, maximum velocity, maximum deceleration, and final position.



The LM628 provides precision motion control *of dc and brushless dc motors and minimizes the parts count of a dc servo system.*

The digital compensation filter is a proportional-integral-derivative (PID) filter. It modifies the output of the controller to keep the servo system stable, and it compensates for the control loop. The LM628 subtracts the actual position, which is determined by feedback from the optical encoder, from the desired, or profile-generator, position. The PID filter processes the resulting position error to drive the motor to the desired position. The LM628 holds the motor at the desired position by subjecting it to a restoring force proportional to the position error, the integral of the error, and the derivative of the error.

An optical incremental encoder linked to the motor sends a 2-phase quadrature signal back to the LM628 to detect the direction of the motor's rotation and position. The motion-control processor uses this signal to control an up/down counter that keeps track of the actual position of the motor.

When the LM628 is in the position mode, you specify the motor's acceleration, maximum velocity, and final position. The unit then controls the motor to meet these parameters. At any time during a move, you can change the maximum velocity, the target position, or both, and the motor will accelerate or decelerate accordingly—which permits the unit to change profile or filter parameters on the fly.

When the unit is in the velocity mode, the motor accelerates to the specified velocity at the specified acceleration rate and maintains this velocity until it receives a command to stop.

The analog control signal from the LM628 can feed either an 8- or 12-bit DAC. The 12-bit output is multiplexed on the eight parallel digital outputs. The amplified output of the DAC controls the motor.

Traditionally, the servo-system host must poll the controller; with the LM628, you have the option of using interrupts. The unit provides index-pulse, absolute, or relative-position breakpoint interrupts, as well as wraparound, command-error, and end-of-profile interrupts. It also features an alarm register that you can set to cause an interrupt should the difference between the desired position and the actual position become greater than the programmable limit. This feature aids in the detection of rotor lock.

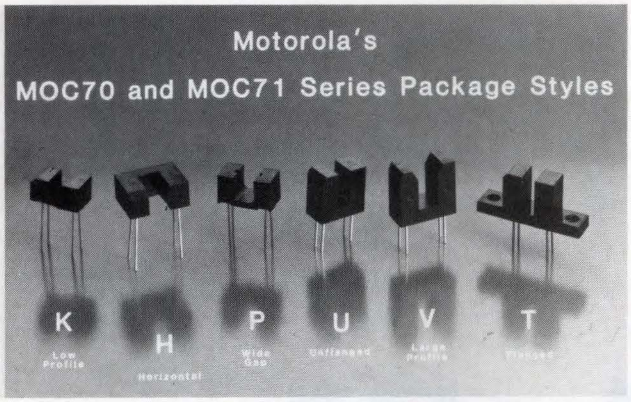
The LM629 is identical to the LM628 except that it provides a pulse-width-modulated output instead of a DAC-compatible output. Both motion-control processors come in 28-pin DIPs, operate over the −40 to +85°C range, and cost \$50 (100).—***David Shear***

National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95052. Phone (408) 721-4494.

Circle No 699

READERS' CHOICE

Of all the new products covered in EDN's **November 26, 1987,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **November 26, 1987,** issue.



▲ OPTICAL SWITCHES

Slotted optical switches are available with transistor (Series MOC70) and Darlington-type (Series MOC71) outputs (pg 267).

Motorola Inc.
Circle No 603

▲ VOICE MODULE

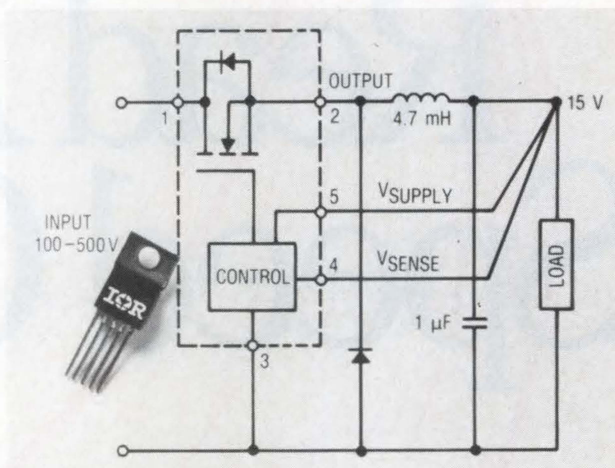
The low-bit-rate voice digitizer LBRV Codec Module produces voice-quality communications at 9600 bps. The pc board contains a µ-law codec that digitizes an analog voice input (pg 262).

Advanced Compression Technology.
Circle No 602

FILTER-DESIGN PROGRAM

The LCFIL stand-alone, menu-driven filter-design program runs on IBM PCs and compatibles or on the Apple Macintosh. You can design highpass, lowpass, and bandpass filters that have as many as 21 poles (pg 272).

BV Engineering.
Circle No 604



▲ DC/DC CONVERTER

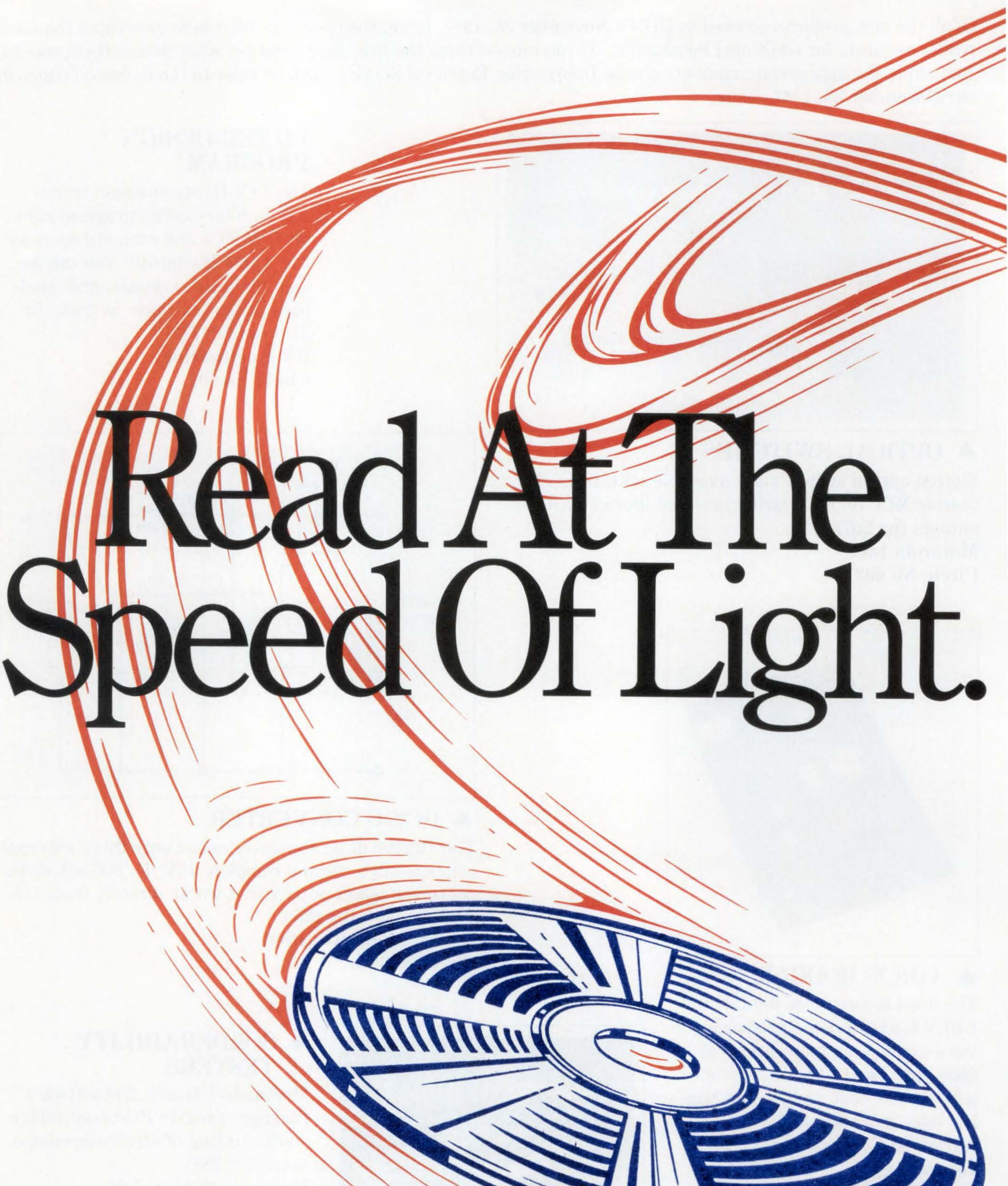
The IR2100 dc/dc converter needs only three external components to form a complete 15V dc, 500-mA dc/dc converter power supply that works directly from 115/230V ac lines (pg 257).

International Rectifier.
Circle No 601

◀ SOLDERABILITY TESTERS

Mustmate-100 and -200 software packages provide PC-based solderability testing of electronic components (pg 288).

Multicore Solders Ltd.
Circle No 605
Multicore Solders Inc.
Circle No 606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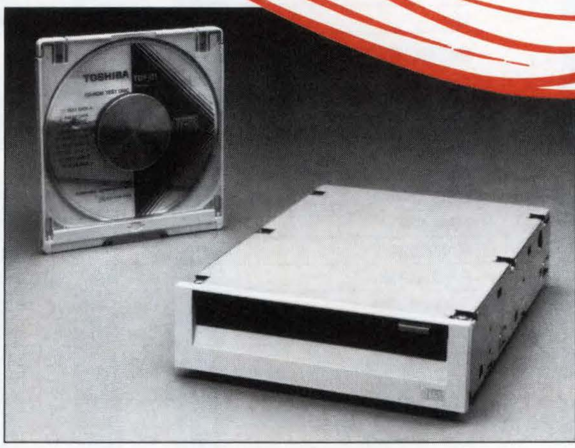

But then, taking pains to do it right is nothing new at Toshiba. After all, we shipped the first optical drive way back in 1981 and we've been in front ever since. With the products, the engineering and the support it takes to be the leader.

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Disk Products Division, 9740 Irvine Boulevard, Irvine, CA 92718

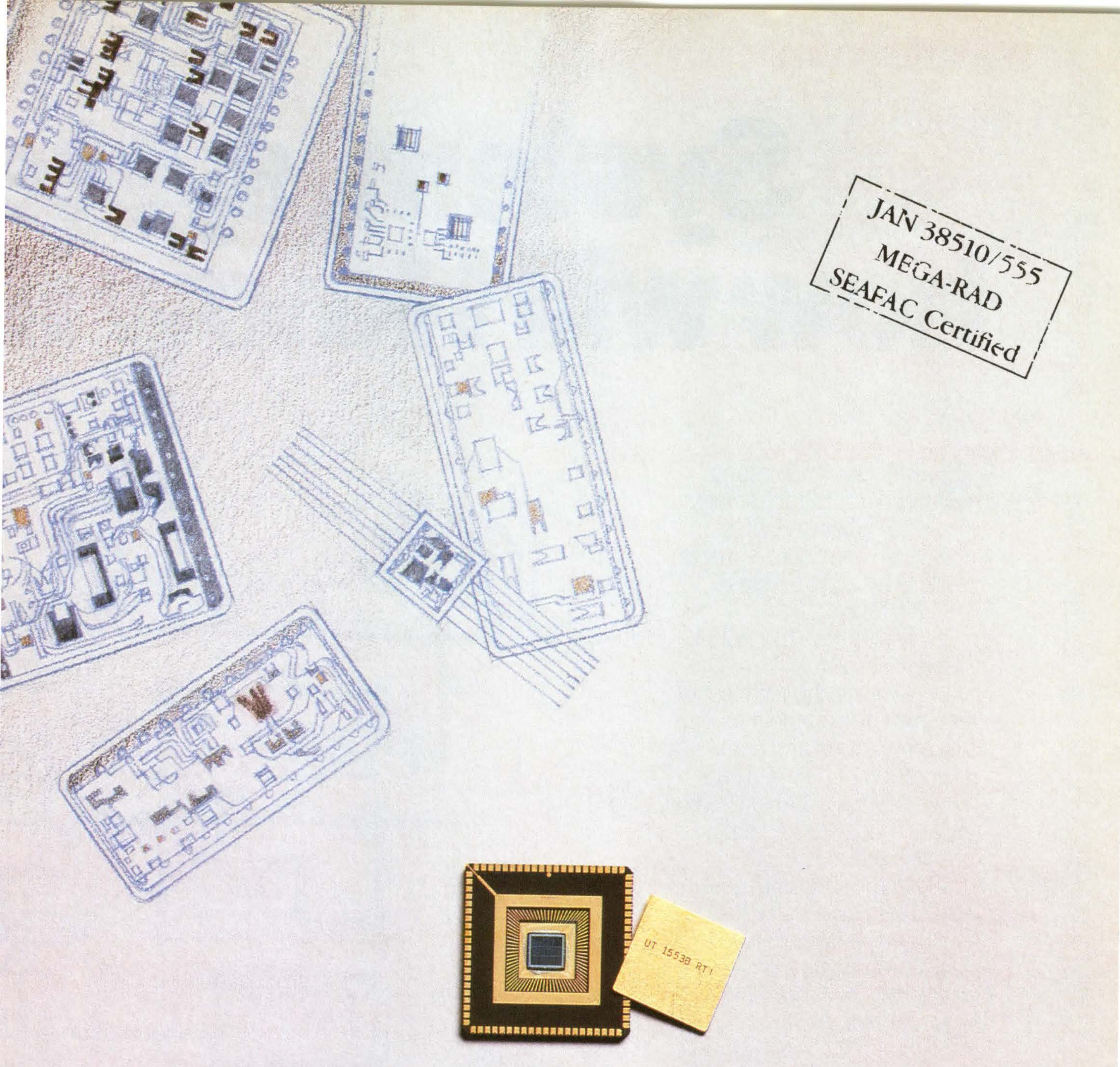
LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	8	58	17	17	0	0	5.7	9.3
Pot-Core	0	50	25	17	8	0	8.2	9.4
Laminate (power)	6	39	33	17	5	0	7.8	8.7
CONNECTORS								
Military panel	0	0	67	17	16	0	12.2	11.5
Flat/Cable	17	44	28	11	0	0	5.3	6.6
Multi-pin circular	10	40	20	20	10	0	8.0	10.0
PC (2-piece)	0	33	45	22	0	0	8.0	7.3
RF/Coaxial	13	40	13	27	7	0	8.1	6.4
Socket	6	67	11	11	5	0	6.0	5.3
Terminal blocks	25	45	15	10	5	0	5.4	5.6
Edge card	19	44	19	12	6	0	6.3	6.3
D-Subminiature	13	40	33	7	7	0	6.6	6.2
Rack & panel	0	45	33	11	11	0	8.6	6.8
Power	0	29	29	28	14	0	11.2	7.2
PRINTED CIRCUIT BOARDS								
Single-sided	0	74	21	5	0	0	4.7	5.1
Double-sided	0	46	50	4	0	0	6.0	6.9
Multi-layer	0	23	69	8	0	0	7.4	7.9
Prototype	5	85	10	0	0	0	3.4	3.5
RESISTORS								
Carbon film	35	45	20	0	0	0	3.0	3.6
Carbon composition	28	43	19	10	0	0	4.3	3.1
Metal film	15	50	35	0	0	0	4.3	4.4
Metal oxide	11	56	22	11	0	0	5.2	4.8
Wirewound	4	46	32	14	4	0	7.2	7.2
Potentiometers	7	55	31	7	0	0	5.2	6.4
Networks	16	37	32	10	5	0	6.6	4.7
FUSES	54	38	8	0	0	0	1.8	3.8
SWITCHES								
Pushbutton	11	72	11	6	0	0	3.9	6.0
Rotary	5	67	11	17	0	0	5.5	7.3
Rocker	6	59	23	12	0	0	5.5	5.7
Thumbwheel	0	69	15	16	0	0	5.7	8.4
Snap action	0	64	29	7	0	0	5.3	5.6
Momentary	7	60	26	7	0	0	5.0	5.6
Dual in-line	0	50	20	30	0	0	7.8	6.4
WIRE AND CABLE								
Coaxial	23	68	9	0	0	0	2.8	3.3
Flat ribbon	26	42	32	0	0	0	3.8	4.0
Multiconductor	25	50	25	0	0	0	3.5	4.6
Hookup	23	65	12	0	0	0	2.9	3.1
Wire wrap	38	54	8	0	0	0	2.2	4.8
Power cords	28	56	12	4	0	0	10.8	4.5
POWER SUPPLIES								
Switcher	6	41	29	24	0	0	7.2	10.1
Linear	0	55	27	18	0	0	6.6	9.5
CIRCUIT BREAKERS	7	33	27	33	0	0	8.3	8.2
HEAT SINKS	17	46	33	4	0	0	4.7	6.2
RELAYS								
General purpose	13	67	12	8	0	0	4.3	6.9
PC board	0	79	0	21	0	0	5.7	8.5

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
Dry reed	0	40	40	20	0	0	7.5	8.9
Mercury	20	40	40	20	0	0	4.4	8.8
Solid state	0	54	31	15	0	0	6.5	7.5
DISCRETE SEMICONDUCTORS								
Diode	32	42	19	7	0	0	3.8	7.8
Zener	35	35	15	15	0	0	4.7	8.8
Thyristor	8	38	31	23	0	0	7.2	9.5
Small signal transistor	37	32	21	10	0	0	4.3	8.8
MOSFET	6	44	28	22	0	0	7.0	8.0
Power, bipolar	15	31	39	15	0	0	6.4	7.5
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	0	50	33	17	0	0	6.8	9.3
CMOS	10	38	38	14	0	0	6.4	8.7
TTL	21	42	16	21	0	0	5.8	5.7
LS	19	48	19	14	0	0	5.2	5.9
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	8	42	33	17	0	0	6.5	8.9
OP amplifier	17	33	22	28	0	0	7.1	7.8
Voltage regulator	11	42	26	21	0	0	6.6	6.8
MEMORY CIRCUITS								
RAM 16k	0	46	27	27	0	0	7.8	7.3
RAM 64k	0	47	27	26	0	0	7.7	7.7
RAM 256k	0	20	47	33	0	0	9.5	10.0
RAM 1M-bit	0	20	30	40	10	0	11.8	11.1
ROM/PROM	9	36	18	37	0	0	8.2	8.7
EPROM 64k	0	36	43	21	0	0	7.8	8.5
EPROM 256k	0	36	36	28	0	0	8.4	9.7
EPROM 1M-bit	0	22	45	33	0	0	9.4	13.5
EEPROM 16k	0	40	30	30	0	0	8.3	9.4
EEPROM 64k	0	36	37	27	0	0	8.3	9.6
DISPLAYS								
Panel meters	8	38	46	8	0	0	6.0	7.2
Fluorescent	0	12	38	50	0	0	11.1	13.0
Incandescent	0	33	34	33	0	0	8.8	8.9
LED	18	32	41	9	0	0	5.6	6.8
Liquid crystal	0	10	40	50	0	0	11.3	9.8
MICROPROCESSOR ICs								
8-bit	28	27	18	27	0	0	6.5	7.8
16-bit	8	50	17	25	0	0	6.7	9.1
32-bit	8	42	25	25	0	0	7.1	8.9
FUNCTION PACKAGES								
Amplifier	0	50	38	12	0	0	6.4	10.2
Converter, analog to digital	0	31	46	23	0	0	8.2	9.8
Converter, digital to analog	0	43	29	28	0	0	8.0	10.7
LINE FILTERS	0	63	12	25	0	0	6.8	7.6
CAPACITORS								
Ceramic monolithic	21	32	37	10	0	0	5.5	6.3
Ceramic disc	26	30	29	15	0	0	5.6	6.5
Film	9	45	32	14	0	0	6.0	7.5
Aluminum electrolytic	12	42	27	19	0	0	6.4	7.2
Tantalum	15	41	29	15	0	0	5.9	7.1
INDUCTORS	0	44	31	25	0	0	7.7	7.6

Source: *Electronics Purchasing* magazine's survey of buyers



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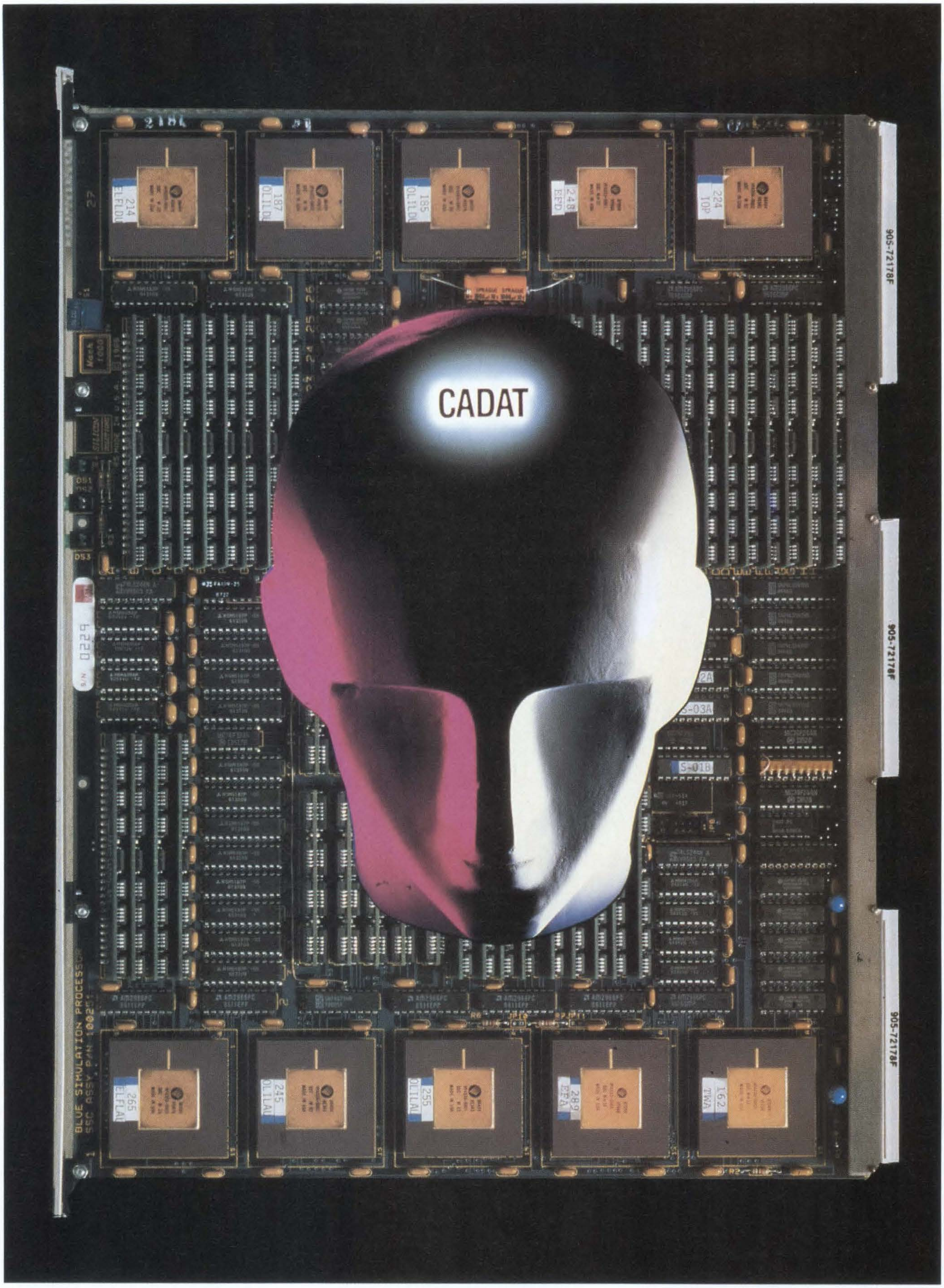


You can reduce simulation time by adding a hardware accelerator, *which implements simulation algorithms in hardware. The Cats accelerator from HHB Systems performs logic, timing, and fault simulation at around 300 times the speed of a VAX 11/780. The Cats accelerator starts at $200,000; for a VAXstation II, the basic Cadat simulation package costs $20,000.*

ASIC simulators

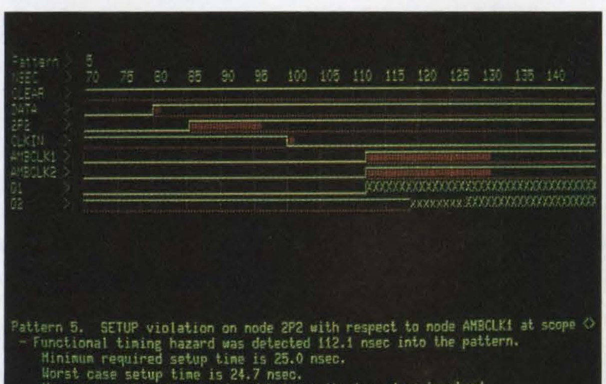
Sophisticated digital simulators can help you develop your application-specific IC (ASIC) designs. Simulators can prevent chip-level design problems and can often come up with good test-vector sets, but they can't correct failures resulting from the old engineering bugaboo—inadequate design specifications.

Margery S Conner, *Regional Editor*

Design flaws in application-specific ICs (ASICs) can be costly: Most ASIC foundries report prototype chip yields of 95%, but many of their customers regularly throw away 40 to 60% of those chips because of flaws in the original designs. Digital-ASIC simulation packages can help you identify and correct some of those flaws before your design goes into production.

Manufacturers of these new logic and timing simulators boast, with some justification, that their products can solve your thorniest ASIC-design problems. (Fault simulation packages are also available; see **box**, "Fault simulators verify testability.") But no simulator in existence now, or likely to exist in the near future—barring a massive breakthrough in artificial intelligence—can make up for the failure to specify your designs rigorously at the chip level.

You can obtain an ASIC-simulation package from one of three sources: You can use your foundry's in-house package, you can develop and support your own custom simulation package, or you can purchase a simulator from a third-party supplier. Each of these approaches has its advantages and disadvantages. The major advantage of using a foundry's in-house simulator, for example, is that the simulator is developed specifically for the foundry's processes and devices. When you use such a proprietary simulator, you are using a package that the foundry knows intimately and that is fine-tuned to model the foundry's proprietary process. What's more, if you encounter problems with your ASIC, you can get them solved promptly; you don't risk waiting around while the foundry and the simulation vendor argue about whose fault the problems are.



Capable of performing logic, timing, and fault simulation, *the Lasar simulator from Teradyne ranges in price from $15,000 for the VAXstation 2000 version to $280,000 for the VAX 8800 version.*

The second option—that of developing and supporting your own simulator—is impractical for most companies because it requires a large software effort. Developing a simulator is practical only for companies that already do a great deal of custom-IC work.

The big advantage of the third option, the third-party simulation package, is that it's portable: You can start with one foundry and later shift to another, as long as the simulator you choose supports both foundries' li-

Digital-ASIC simulation packages can help you identify and correct design flaws before your design goes into production.

braries of models. However, because of the huge number of foundries to choose from and the rapid advancements in model design, vendors of third-party simulators have not been quick enough to support new models.

Foundry supports third-party simulators

Until recently, many of the larger ASIC foundries have often refused to guarantee chips fabricated from designs simulated with third-party simulators. Now, however, some of the foundries show signs of bowing to their customers' demands for third-party-simulator support. VLSI Technology (San Jose, CA), for example, deals with many a potential customer that has already invested in a workstation package and doesn't want to purchase another one from a foundry. The company offers its Portable Library for the Daisy and Mentor workstations. The basic Portable Library interface is $10,000; the timing-module libraries cost $5000 each. (Each timing module is for a particular line width; ASICs with 1.2-μm line widths, for example, have different timing characteristics than do those with 1.5-μm line widths.) Because of the competition among foundries, third-party-simulator support will probably become the rule rather than the exception.

VLSI Technology chose Daisy's and Mentor's simulators because those two companies have large installed bases. That decision illustrates the Catch-22 situation that some of the younger simulator companies find themselves in: Designers are reluctant to commit to the newer simulator vendors, regardless of the quality or cleverness of their products, because newer companies' simulator libraries lack extensive foundry models. However, it's difficult for a younger company to develop a library of foundry models, because foundries usually choose only third-party simulators that are already in wide use.

When you're choosing a third-party simulator, it's

Fault simulators verify testability

The design engineer has traditionally been responsible for troubleshooting any logic and timing problems in an ASIC design. Now, however, the production problems associated with higher degrees of circuit integration—problems such as increasing circuit complexity and the lack of test points—are forcing design engineers to shoulder testability concerns as well. The reason that design engineers must consider testability is clear: The best point at which to determine whether a design is testable, and thus manufacturable, is the earliest one—the design stage.

To meet those needs, most vendors of ASIC-simulation packages currently offer fault-simulation packages in addition to their logic and timing simulators. Fault simulators help ensure that designs will be testable by inserting faults into a network model and running a network simulation for both the correct conditions (as an experimental control group) and the error conditions. For example, the most commonly used fault model, the "stuck-at" fault model, assumes that inputs and outputs of network primitives fail at either a high or a low state. The fault simulator looks for changes in the output for a stuck-at condition; if that output is different from the output exhibited in the fault-free state, then the input vector has detected a fault. The ultimate purpose of the fault simulator is to find out whether your fault-simulation vectors provide adequate fault coverage.

Note that these fault-simulation vectors are not test vectors. Rather, you use fault-simulation vectors to generate test vectors. Test vectors are the stimulus and response patterns that the ASIC foundry uses to verify that its chip meets your design criteria and that the manufacturing process has not varied. Once the chip is in volume production, the foundry monitors the manufacturing process by running the test vectors through each ASIC.

Because of production-time and cost restraints, an ASIC house can usually run about 4000 to 10,000 test vectors through the ASIC—for more vectors, you must pay a premium. Although 10,000 test vectors are usually enough to verify that a chip has been produced correctly and that the manufacturing process is not varying, they are not sufficient to verify that the design is good. Fault-simulation vectors, however, *can* verify that a design meets its specifications.

useful to consider the experiences of companies that have developed their own simulators. Such companies understand how simulators work and have practical experience in applying them. Further, because they don't sell their simulators, these companies are relatively unbiased about what a simulator's capabilities should be, and they're under few illusions about what you can expect from a simulator.

One company's experience

For example, Zymos Corp (Sunnyvale, CA), which designs and manufactures customizable IBM PC- and PS/2-compatible chip sets, wrote its own logic and timing simulator. Initially, the company let customers use the simulator to simulate chips that varied from Zymos's basic ASIC design. The company then took those designs and turned them into silicon.

Zymos discovered, however, that the chips developed from those simulations often did not work in the customers' systems. The problem was not that the simulations were wrong, but that the specifications the customer used in the simulations were incorrect. Because Zymos had incurred unnecessary nonrecurring engineering costs to develop prototype chips that it never produced, the company elected to require that all new designs be proven first in its hardware emulator. In essence, the company required a breadboard of the new design. The lesson to be learned from Zymos's experiences is not that simulation doesn't work, but that ASIC design still requires a great degree of engineering-design skill.

Look for a complete library of models

The three most important features to consider when choosing a simulator are the simulator's library of models, its modeling capabilities, and its timing-verification capability. The library is the most important of these features. It should have enough of the models you need and should be compatible with your foundry's processes. Be sure to find out exactly what models the simulator supports before purchasing it; don't assume that the simulator will have the models you need just because it has a large number of models.

For example, a 7400, 74S00, and a 74ALS00 are all implementations of a NAND gate, yet the simulator manufacturer may count them as three separate models. Although it's true that the different families have different timing characteristics, the timing differences don't affect the device model; timing parameters are loaded in at simulator run-time.

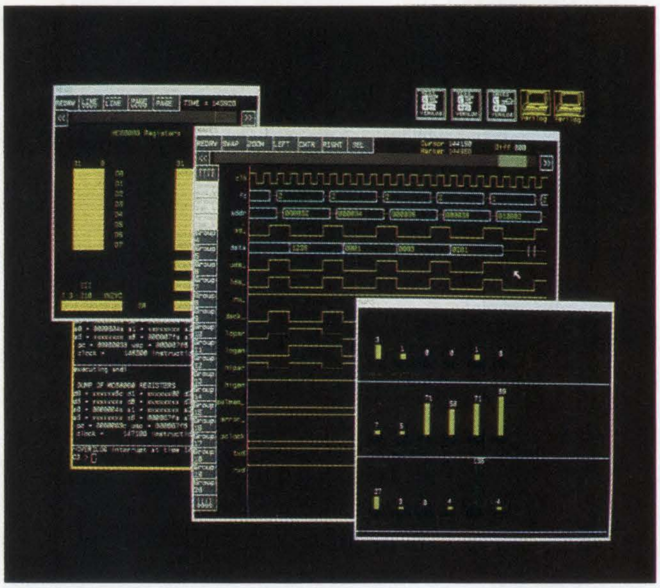
With the 192M-byte expanded-memory option, *the Compute Engine Model M can simulate designs having as many as 325,000 gates. The Model M typically allows Apollo workstations to perform logic simulations 24 times faster than they could without the accelerator. This acceleration allows you to perform mixed-mode ASIC simulation at the system level.*

If, like most companies, your company designs products in one general field, it's more important for you to choose a simulator library that has most of the devices you design with than it is for the library to have a broad selection of models you won't use. Even so, your company will probably need to develop proprietary models for devices; using these proprietary models is one way to give your ASIC designs a competitive edge over products from companies that use all plain-vanilla parts. All digital-ASIC simulators let you define proprietary device models.

Paradise Systems (South San Francisco), for example, designs products and ASICs for the video-display market. Paradise has found that no simulator library covers all of the video-related devices that it designs with. Paradise chose the Mentor simulator package and added to it by writing many simulator models in house. An alternative to writing extra models yourself is to arrange for another company, such as Logic Automation (Beaverton, OR) or Quadtree (Bridgewater, NJ), to develop the library models for you under contract.

Next in importance to the simulator's library is its

Simulation can help solve some design problems, but no simulator can make up for poor chip-level specifications.



To perform behavioral modeling from the gate level through the system level, *the Verilog simulator from Gateway Design Automation uses the Verilog-XL hardware-description language (HDL).*

modeling capability. Simulators that offer a behavioral language make it easy for you to model complex devices. Further, because behavioral languages can model devices at various levels, they're well suited for use in hierarchical system design.

When you model a device, you face two challenges—you must describe how the device works, and you must be able to specify stimulus and response patterns. To make this process as painless as possible, you should use a simulator that supports a hardware description language (HDL) that is a behavioral language. Behavioral languages are C-like languages with control structures (constructs), such as If-Then-Else statements, that are tailored for defining the behavior of a device and its response to a stimulus.

Theoretically, the best way to design ASICs for a complex system is to start by specifying the system requirements. Next, you divide the system into subsystems and define each subsystem's requirements, repeating this process through the board level to the individual-ASIC level until the system is completely defined. This complete set of requirements for each building block allows you to simulate ASICs completely in their environment.

That's the theory, anyway. In reality, according to Pete Johnson, a product marketing manager at Gateway Design Automation Corp, it's very rare for a company to do a complete hierarchical system design. Although more design engineers are seeing the benefits of specifying designs thoroughly from the system level to the chip level, Johnson notes, their managers don't always agree. The problem, he says, is that most engineering managers operating under a tight schedule feel more comfortable with hardware—even when it doesn't work and has to be rebuilt—than they do with the intangible results of a software simulation. They're not always willing to wait for a designer to completely specify and simulate a design before producing the actual part.

Cirrus Logic (Milpitas, CA), a designer of custom ICs for the peripheral-controller market, makes a good case for drawing up detailed design requirements. Because Cirrus's ASIC designs are specialized, the company can make the large software effort necessary to develop and support a custom simulator. However, George Alexy, the company's vice president of marketing, is quick to point out that no simulator is a panacea. More important than software tools are engineers who thoroughly understand what they're trying to design and can translate that understanding to good design specifications.

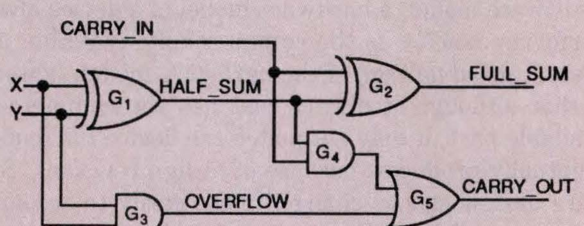
Cirrus, for example, committed itself to developing a fully custom IBM VGA-compatible chip for IBM PC- and PS/2-compatible machines in six months. Instead of jumping immediately into chip design, the company first developed a complete specification for the chip. After performing the design, Cirrus used a simulator that forced the designers to compare the simulated results with the initial requirements. This practice ensured two things: first, that the designers thoroughly understood how it expected the chip to perform in the system, and second, that the design would be completely documented.

No guarantee it's a duck

This detailed approach has obvious advantages over the traditional design technique that assumes, as the saying goes, that if it looks like a duck, walks like a duck, and quacks like a duck, it probably is a duck. Cirrus's results were impressive; it had delivered over 20,000 of the VGA-compatible chips before its competitors even started shipping. The project's success was largely due to the effort the company put into the initial design specifications.

Although they can emulate Cirrus by placing more emphasis on their designs' initial specifications, most small companies don't have the resources to develop their own simulators. Instead, they must rely on third-

(a)



(b)

```
module gate_adder(carry_out, sum, a, b, carry_in);

input[3:0] a,b;
input carry_in;
output [3:0] sum;
output carry_out;

addbit add3(carry_out, sum[3], a[3], b[3], c2);
addbit add2(c2       , sum[2], a[2], b[2], c1);
addbit add1(c1       , sum[1], a[1], b[1], c0);
addbit add0(c0       , sum[0], a[0], b[0], carry_in);

endmodule

module addbit(cout, sum, x, y, cin);

input x,y,cin;
output sum,cout;

xor g1(half_sum,x,y),
    g2(sum,half_sum,cin);

and g3(ov,half_sum,cin),
    g4(half_carry,x,y);

or  g5(cout,ov,half_carry);

endmodule
```

(c)

```
module func_adder(carry_out, sum, a, b, carry_in);

input[3:0] a,b;
input carry_in;
output [3:0] sum;
output carry_out;
wire [4:0] full_sum;

assign full_sum = a + b + carry_in;
assign sum = full_sum[3:0];
assign carry_out = full_sum[4];

endmodule
```

(d)

```
module alg_adder(carry_out, sum, a, b, carry_in);

input[3:0] a,b;
input carry_in;
output [3:0] sum;
output carry_out;

reg temp_carry,carry_out;
reg [3:0] sum;
integer i;

always @(a or b or carry_in)
begin
   temp_carry = carry_in;
   for (i=0; i<=3; i=i+1)
   begin
      sum[i] = a[i] ^ b[i] ^ temp_carry;
      if(a[i] + b[i] + temp_carry > 1)
         temp_carry = 1;
      else temp_carry = 0;
   end
carry_out = temp_carry;
end

endmodule
```

Fig 1—To compare and contrast gate-level, functional, and algorithmic behavioral models, *consider the 1-bit full adder shown in* ***a****. The gate-level behavioral model* ***(b)*** *of the adder demonstrates the detail needed at this level of modeling, even when you use a hardware description language (HDL). A functional model* ***(c)*** *of the same adder device is much less complex and requires a less-detailed knowledge of the device's gate composition—the code is basically just the Boolean equation for an adder. The algorithmic model* ***(d)*** *is the most abstract level of modeling. In this example it requires more lines of code than* ***c*** *does, but for more abstract devices it's the simpler of the two methods. Note that the first five lines of each model are the same; they are necessary to make the module appear to the simulator as a black box. These five lines describe the inputs and outputs and define an order in which the module can be accessed from another module. The language used in this example is Verilog-XL from Gateway Design Automation.*

party simulators to support the design effort from the system level down to the chip level. If you choose a third-party simulator, be sure to choose one that uses an HDL, which is invaluable in supporting this range of simulation levels.

Behavioral-language models

Most HDLs being developed now are behavioral languages. You can use most behavioral languages to model devices from the transistor level up through the algorithmic level. Although early simulators could use only transistor-level (or switch-level) device models, most currently available simulators can use a range of models, from the gate level to the algorithmic level. Devices are becoming so complex that even gate-level modeling is becoming impractical, however.

Developing a gate-level model of the 80386 could take a relatively long time—perhaps even a few years. In other words, it can take as long to model a device at the hardware level as it does to design it in the first place. At present, it's common to make behavioral-language models of complex chips at the more abstract bus level.

Some of the larger foundries now show signs of bowing to their customers' demands for third-party-simulator support.

Logic Automation developed such a model for the 80386 (which it offers for $1850) over several months.

Behavioral-language modeling models a chip by describing, in a behavioral language, how the chip acts ("behaves") in the system. Although it takes about as long to create a behavioral-language model of a simple device—a flip-flop, for example—as it does to construct a Boolean model of the device, you can model complex devices much more rapidly by using behavioral-language modeling rather than hardware-level modeling. Hardware-level modeling describes the specific physical structure of a device. Because a behavioral-language model describes the behavior of a device independently of its physical structure, foundries can make extensive changes in the physical structure—as long as they don't change the device's behavior—without invalidating the simulation results obtained with the behavioral-language model.

Strictly speaking, you can make a behavioral model of a design at any level. Practically speaking, however, you'll probably use a behavioral-language model only when your ASIC's gate count exceeds about 25 gates. The programming overhead associated with behavioral-language modeling (setting up variables, for example) is too great to be worthwhile for less-complex devices.

ASIC simulators that offer behavioral languages let you model devices at any of three levels: the gate, functional, and algorithmic levels. A gate-level model defines a device in terms of its gate interconnections. A functional model defines a device's behavior as a set of Boolean equations. An algorithmic model defines the device's behavior in terms of algorithms by making full use of a behavioral language's constructs and higher-level capabilities. **Fig 1** gives examples of gate-level, functional, and algorithmic models written in an HDL that is also a behavioral language.

Hardware modelers

If your design includes a commercially available component for which no software model exists, you can still use that part in your simulation by plugging a hardware model of the part into a hardware modeler. A hardware modeler is a unit that interfaces with (or is built into) the simulator's workstation. A hardware model is usually a board that contains the commercially available device and any required support circuitry. Companies such as HHB Systems, Ikos, and Mentor offer hardware modelers and hardware models of various parts for use with their simulators. HHB Systems, for example, offers its hardware modeler for $65,000 and sells hardware models for around $5400 each.

A big advantage of hardware modeling is that, unlike a software model, a hardware model of a device always performs exactly as the commercially available part does. A disadvantage of the hardware model, however, is that although it always matches the commercially available part, it may not match the device the foundry eventually produces, because of design revisions. Software models can be changed more easily to accommodate any revisions. Further, you can't use a hardware model to run timing simulation, because you can't change the timing parameters of the hardware model.

Consider performing a timing simulation

To draw up a detailed specification for your ASIC, you need to specify timing parameters. It's one thing to write an ASIC specification that baldly states the relationship among the logic levels; it's much more difficult to write a spec that explains the minimum and maximum timing for each signal. These timing extremes are important because they verify that the ASIC will work over the range of timing conditions the manufacturing process allows.

Although min/max timing verification is time consuming because of the number of variables the simulator must consider, consider running a timing simulation anyway: Timing-simulation information is critical because it is information that a breadboard can't give. If your design has more than 5000 gates, your timing simulation will probably run very slowly. To speed the simulation of large designs, consider using a hardware accelerator.

Hardware accelerators are optional units that implement the simulation algorithms in hardware. Mentor's Compute Engine Model M accelerator, for example, lets a workstation perform a logic simulation of a 23,000-gate circuit 24 times faster than it could without the accelerator. The accelerator interfaces with the Apollo Model DN400, -500, -600, and -3000 workstations. Prices for the Compute Engine start at $59,900.

However, accelerator prices cover a wide range. Zycad's line, for example, starts with the $38,000 Magnum and ends with the $2.5 million System Development Engine. Accelerators are also available for smaller budgets. One of the least expensive hardware accelerators is Aida's Persim, which performs 5 million evaluations/sec. The Persim Model 1 can model 64,000 gates; the Model II can model a maximum of 128,000 gates. The prices are $7500 and $20,000, respectively.

The reason the prices and simulation times quoted for

Third-party simulators are portable: You can start with one foundry and later switch to another, as long as your simulator supports both foundries' libraries.

the Persim models seem very low is that these simulators operate differently from the others. The Aida simulators perform levelized-compile-code simulation, which evaluates the output state of all logic gates in a design, in accordance with each change in the input pattern, and ignores timing delays. This type of simulation takes place much more quickly than do simulations that take gate delays into account. By ignoring any gate delays, the simulator can simply evaluate a Boolean equation. After you've performed the logic simulation and caught any obvious logic-design problems, you can then run the design through the timing-analyzer software, which determines the timing associated with all of the circuit's delay paths.

Because the Aida simulator doesn't take the gates' timing characteristics into account, this timing analysis only works for synchronous circuits; the simulator merely flags any asynchronous circuits. This scheme is generally adequate for most designs, however, because most large gate designs are synchronous.

Not all simulator manufacturers are fans of hardware accelerators. Prabhu Goel, president of Gateway Design Automation, claims that as engineering workstations gain more processing power, they'll no longer need separately accelerated simulation algorithms. For now, however, keep in mind that accelerators can commonly execute 500 MIPS, which is still far beyond the capability of a general-purpose workstation at pres-

Manufacturers of ASIC simulators

For more information on digital-ASIC simulation packages, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Aida Corp
5155 Old Ironsides Dr
Santa Clara, CA 95054
(408) 748-8571
Circle No 650

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Scotts Valley, CA 95066
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Calma Co
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Milpitas, CA 95035
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Menlo Park, CA 94025
(415) 324-0700
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SimuCad
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Suite 200
Menlo Park, CA 94025
(415) 321-2350
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Simulog Inc
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Viewlogic Systems Inc
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XCAT
2855 Anthony Lane S
Minneapolis, MN 55418
(612) 789-2050
Circle No 674

Zycad Corp
3500 Zycad Dr
St Paul, MN 55109
(612) 631-5555
Circle No 675

ent. It's likely that accelerators will continue to increase in popularity for high-gate-count designs and for accelerating PC-based workstations, while unaided workstations will provide acceptable performance for medium-gate-count designs.

Unlike the manufacturers that offer hardware accelerators, Ikos has taken a different approach. The company designed its simulators to implement all of their simulation algorithms in hardware. The Ikos 1900, for example, is a deskside tower that interfaces to an IBM PC/AT, Apollo DN3000, or Sun 3. The 1900, which starts at $46,500, simulates designs of as many as 16,000 gates. You can increase that number—to 245,000 gates—by adding as many as fourteen 16,000-gate evaluation boards at $11,000 each. **EDN**

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1. Wiegand, Jim, "Gate Array Directory," *EDN*, June 25, 1987, pg 134.
2. "1987 Survey of Logic Simulators," *VLSI Systems Design*, February, 1987, pg 71.

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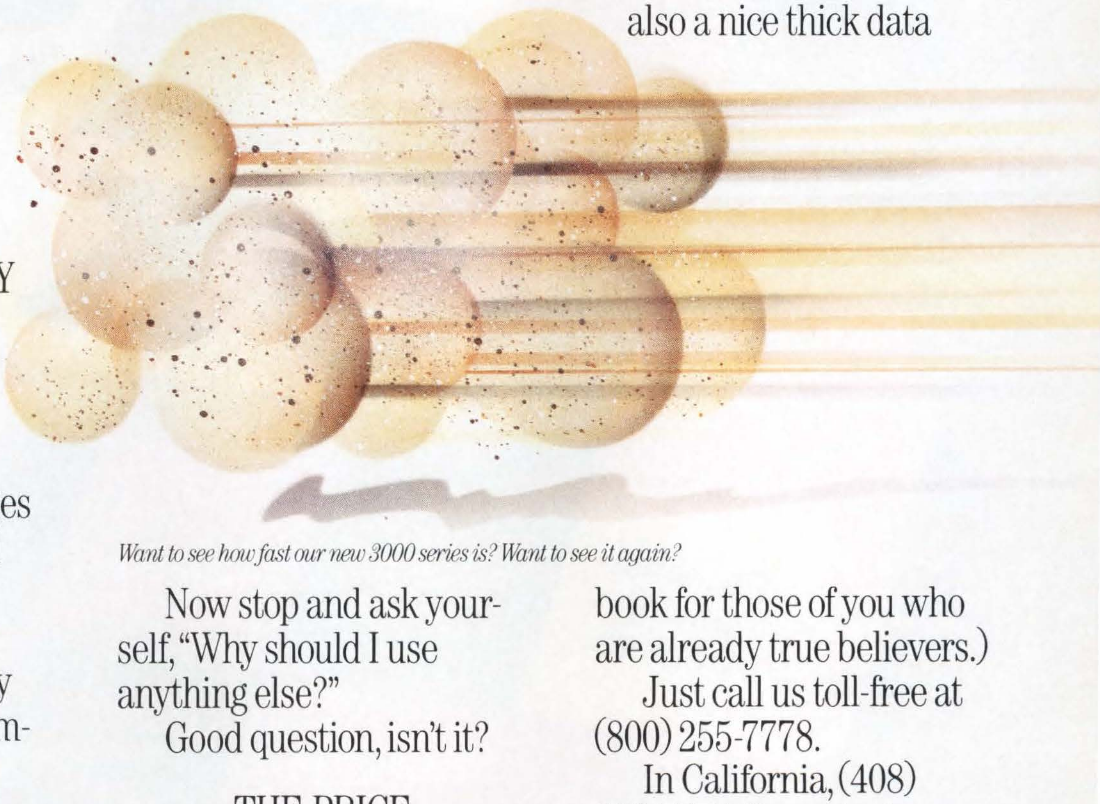

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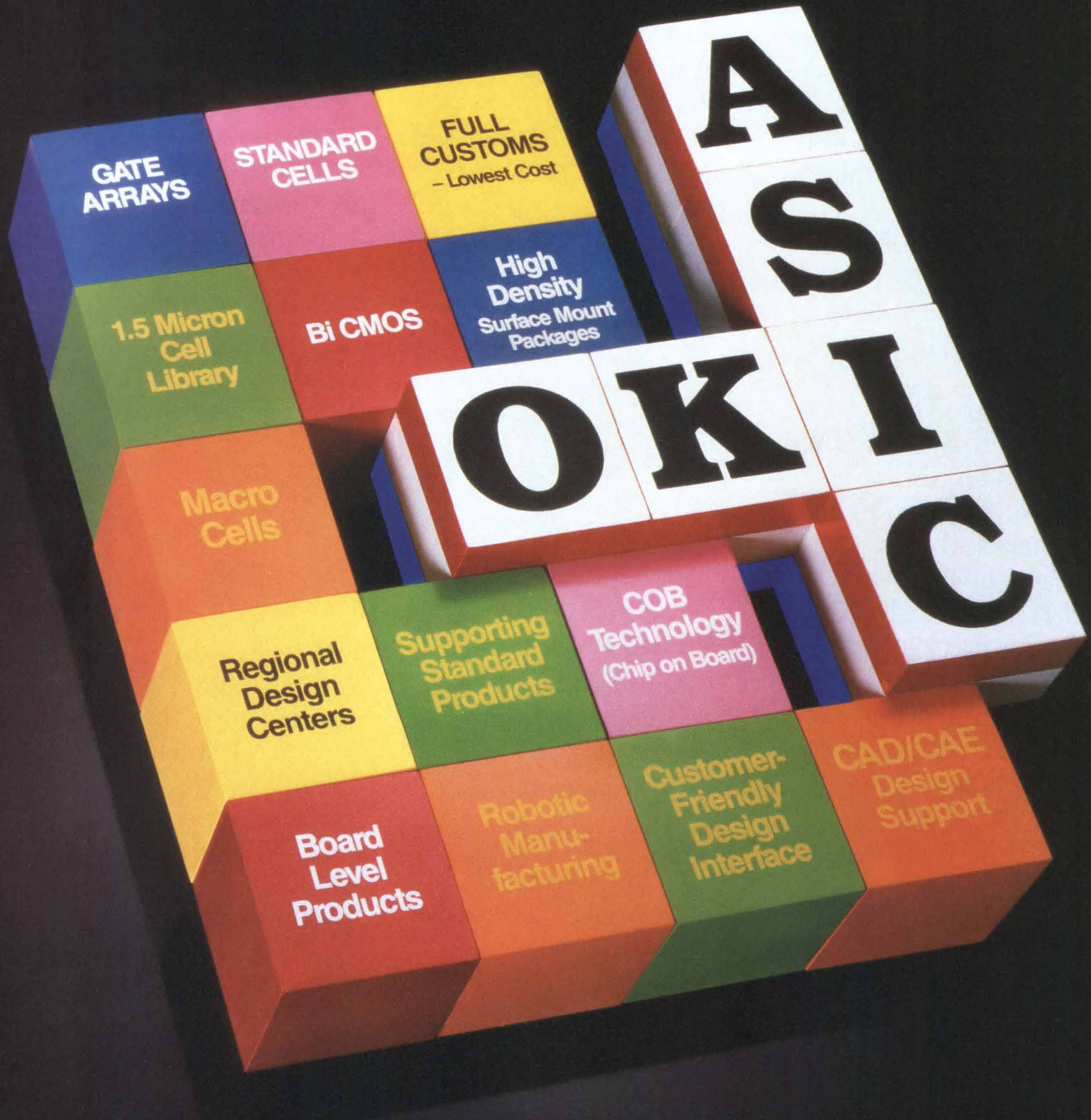
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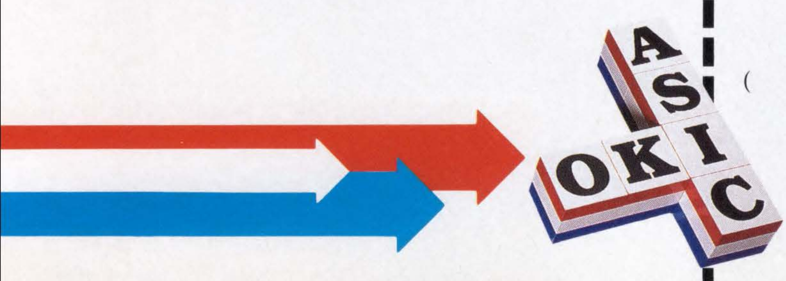

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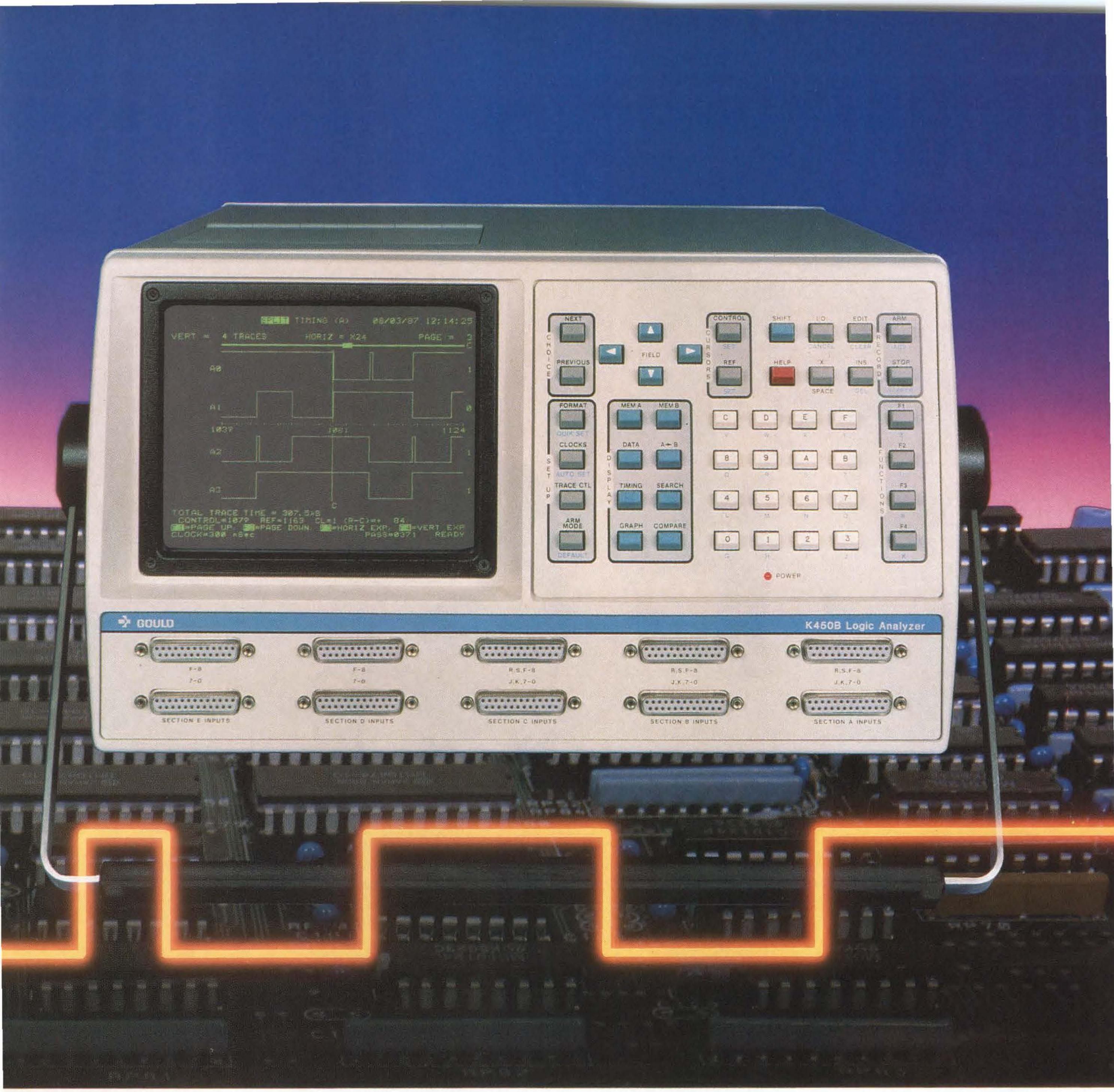

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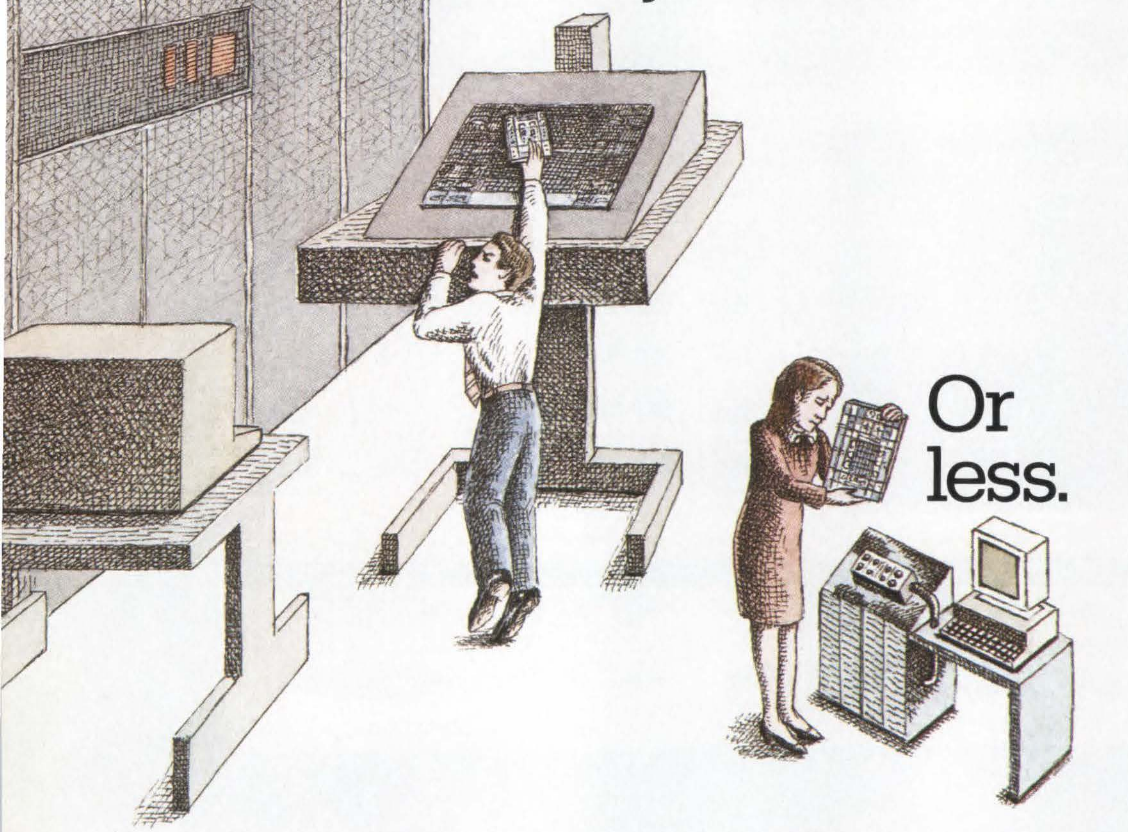

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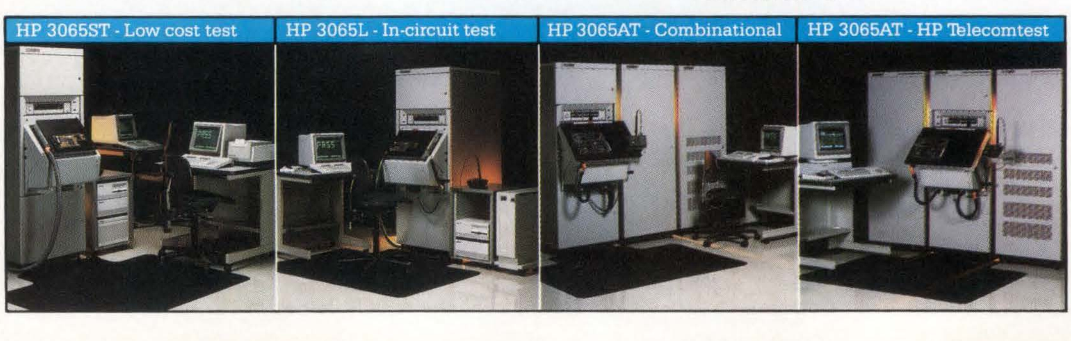

*Some restrictions apply.

Consider the tradeoffs when evaluating linear-semicustom ICs

System designers face special problems when creating analog circuits for semicustom IC fabrication. Unlike digital circuits, which you can readily subdivide into simple gates, analog circuits are highly irregular, require different design methods, and frequently need nonintegrable external components.

Bruce Moore, *Raytheon Semiconductor*, and
Will Ritmanich, *Consultant*

The problem of designing analog (linear) circuits suitable for semicustom fabrication is complicated by the nature of the active and passive devices available for IC fabrication. Because the fabrication process imposes constraints, transistors, resistors, and capacitors in IC form display performance characteristics different from those of their discrete counterparts. To help minimize the cycle time, cost, and risk involved in your design effort, it is important to understand these performance characteristics and the design approaches necessary to implement a successful linear-semicustom circuit.

Start with a list

The first step in preparing your design for integration is to rank the circuit's key requirements and features in order of their relative importance. This ranking is essential because the process of creating a semicustom-linear IC requires compromises involving a number of factors, including the following:

- available power-supply voltages
- desired power consumption
- required circuit speed
- desired accuracy
- operating environment
- I/O considerations
- time-to-market urgency
- volume vs device-cost tradeoffs.

To the extent that it is possible, you should assign objective specifications to each major functional block in your circuit. Successful monolithic designs are easy to manufacture and achieve good yields in volume production. If you impose parameter specifications tighter than those normally obtainable, you will limit production yields and substantially increase device costs. Don't make any specifications tighter than needed, even if you don't think that there's a chance of compromising manufacturability.

In reviewing your circuit for feasibility of integration, you should be aware of four generalized aspects of monolithic-IC circuit designs that distinguish them from discrete or hybrid designs:

1. **Matching.** Semicustom IC designs generally rely on the matching and tracking of component *ratios* rather than on absolute values. If possible, you should avoid circuits that depend on tight-tolerance absolute values, or change the circuits to rely on component matching. If the circuit needs precision components—timing resistors, for example—you'll usually have to leave them off chip.

2. **Component choice.** You can best accomplish semi-

Transistors, resistors, and capacitors in integrated-circuit form do not display characteristics identical to those of their discrete counterparts.

custom designs through proper partitioning, which entails leaving the difficult-to-integrate components outside the package. For instance, you must handle large-value capacitors in this manner because it is difficult and expensive to integrate more than 50 picofarads of capacitance on chip. Power transistors create similar problems; they commonly require special processing to achieve their rated performance, and the large die sizes and high power dissipation of high-current (>200 mA) power transistors usually preclude their use on chip. Medium-power transistors, however, are generally available on chip.

3. **I/O limitations.** Successful semicustom designs generally minimize the number of bonding-pad (I/O) connections and maximize the interconnection of internal elements. The number of I/O and power-supply connections is a major determinant of an IC's chip size, packaging yields, test costs, and reliability. Try to keep the IC pin count lower than 44 to take advantage of low-cost packaging, though any work to minimize the bonding-pad count will prove rewarding. In particular, for circuits that use many capacitors, you can often reconfigure the circuit to reduce the device pin count while providing performance equal to or better than that of the original design. If your circuit contains both analog and digital elements, you'll sometimes find it cost effective to split the design into two chips. Large semicustom chips using analog elements to provide digital functions are generally more difficult to design, manufacture, and test—and are much more expensive—than purely digital circuits with comparable logic performance.

4. **Infinite redesign.** Although a discrete design that is already in production can be modified, tweaks and fixes in an IC are expensive and difficult, and thus you should give some thought to the lifetime of the end product. Consider including options or adjustability features in your design before committing it to production. (For more information on this subject, see **box,** "Achieving first-pass design success.") If there's a great likelihood that your initial design may change before attaining substantial volume, then an array-based approach is probably your best choice. If circuit accuracy or volume requirements are a high priority, you may want to choose a standard-cell design or a full-custom design. An approach that many engineers have adopted is to use arrays for prototyping and low-volume production, and then to phase in full-custom designs later. This approach offers the best of both worlds—low initial design costs, low risk, a reduced time factor, and the provision for producing low-cost devices in large volume when you need them.

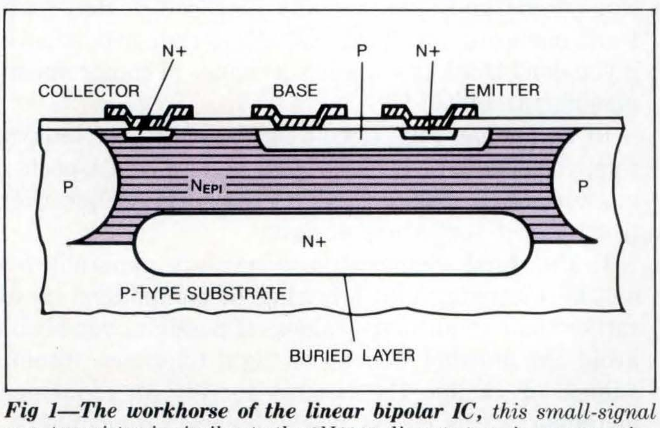

Fig 1—The workhorse of the linear bipolar IC, *this small-signal npn transistor is similar to the 2N3904 discrete type in construction and basic performance. Its saturation voltage, stray capacitance, and current-handling capability are inferior to those of the discrete device.*

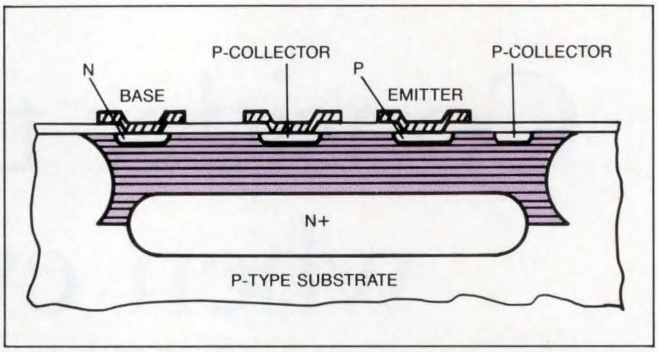

Fig 2—Having no practical discrete equivalent, *lateral pnp transistors operate laterally in the plane of the die surface. Their gain and frequency characteristics are poor in comparison with those of vertical devices.*

Bipolar workhorse is like the 2N3904

Fig 1 shows the structure of a small-signal npn transistor, the workhorse of the linear bipolar IC. Similar to the discrete 2N3904 in construction and basic performance, it has one outstanding difference. In a discrete transistor, ohmic contact is made directly underneath the base-emitter junction to minimize bulk collector resistance and $V_{CE(sat)}$. Because this interconnection technique isn't possible in a junction-isolated IC, manufacturers add a heavily doped, buried layer instead. This buried layer causes higher saturation voltages, a higher collector capacitance (about 3 pF), and a lower current-handling capacity (about 10 mA).

Frequency response of the integrated transistor is very good—the small npn transistors in Raytheon's

Achieving first-pass design success

A general problem that most system designers face is that they don't have the time to redesign malfunctioning circuits. Because most linear ICs start with a paper design followed by a discrete breadboard, you should avoid the possibility of a redesign by selecting the most suitable technology and methodology early in your design cycle. Reducing the risks by eliminating the unknowns is always a good idea.

The approach that Raytheon (Mountain View, CA) takes is to eliminate most of the design difficulties posed by semiconductor variables, by making the active and passive components behave more like familiar, off-the-shelf devices. To ease the design task, Raytheon has a kit available that includes sample devices, software, and design documentation.

Raytheon's RLA series of tile-based, linear macrocell arrays includes a variety of thin-film resistors ranging in value from 1.25 kΩ to 150 kΩ. Further, the configurable, tile-based differential gain blocks have high gain and provide performance approaching that of many off-the-shelf op amps and comparators. In addition, a proprietary 2-layer-metal process allows ease of routing and provides maximum array utilization and low NRE costs. Such features permit the creation of array-based circuits that rival the performance of standard-product ICs.

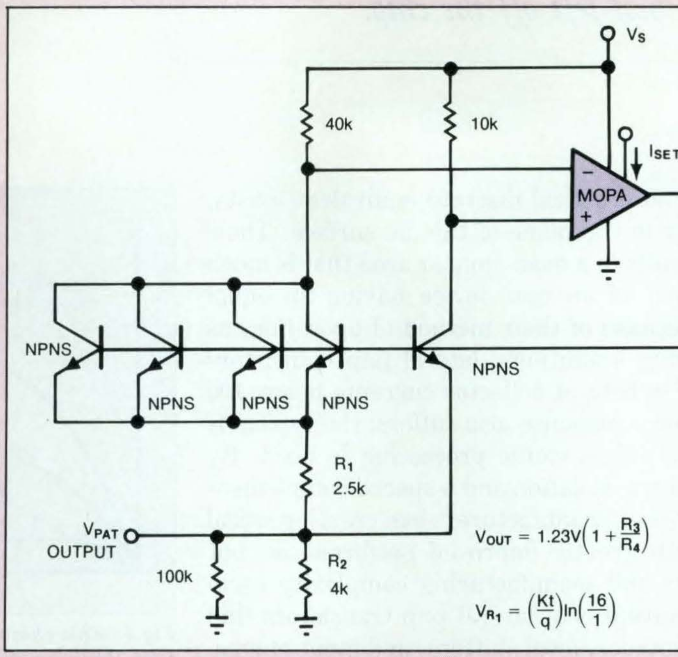

Fig A—This 1.23V bandgap regulator rivals discrete designs. *It has an initial circuit accuracy of ±2%, a typical TC of ±20 ppm/°C, and a load regulation of ±2 mV at currents to 20 mA.*

As an example of the performance attainable with this approach, **Fig A** shows a bandgap voltage reference that can also function as an electronic thermometer. The reference takes advantage of the thin-film resistors in the RLAs to generate an output voltage with a low temperature coefficient. The 1.23V output voltage has an initial accuracy of ±2% and a typical TC of ±20 ppm/°C. The load regulation is ±2 mV at load currents of 0 to 20 mA, and the line regulation is ±10 mV at supply voltages (V_S) ranging from 4 to 30V.

The transistors designated NPNS in the circuit are small-signal types. The MOPA gain block is a single macrocell location connected as an operational amplifier. The circuit generates the reference voltage by adding the V_{BE} of the single NPNS to the voltage across R_2.

V_{BE} has a negative temperature coefficient; the R_2 voltage has a positive temperature coefficient, which the voltage across R_1 determines. These voltages sum to produce a nearly zero TC at the V_{BG} terminal. The output, V_{PAT}, is the actual bandgap voltage, which is proportional to the actual temperature. You can scale this output to any convenient value by using a buffer amplifier having suitable gain.

RLA linear arrays have a typical f_T of 500 MHz. New bipolar processes have extended this figure to over 1 GHz. Manufacturers accomplish this frequency extension by using fine-line geometries, plasma etching, and electron-beam lithography. Thanks to their vertical structures, npn transistors have high current gain in a small device size. They also have a stable and predictable V_{BE} that has good device-to-device matching characteristics.

High-current (large) npn transistors have a geometry similar to the small npn types, but with substantially increased emitter- and collector-contact areas to handle the higher currents. As a result, these transistors have a lower frequency response and an increased parasitic capacitance (about 10 to 30 pF) from collector to substrate. Roughly comparable to the 2N2222, these IC versions handle a conservatively rated 200 mA, but exhibit higher saturation voltages.

Fig 2 depicts the geometry of the pnp transistors normally encountered in a monolithic IC. These transis-

High-value capacitors and precision resistors are difficult and costly to fabricate; they're often best left off the chip.

tors, for which no practical discrete equivalent exists, operate laterally in the plane of the die surface. Their construction results in a base-emitter area that is much smaller than that of an npn device having an equal emitter size. Because of their method of operation, as well as processing limitations, lateral pnp transistors exhibit a falloff in beta at collector currents below 100 μA. The frequency response also suffers; the typical f_T is about 4 MHz unless exotic processing is used. By employing dielectric isolation and a special complementary-bipolar process, manufacturers can create vertical pnp devices with greatly improved performance, but production costs and manufacturing complexity escalate rapidly. Conventional lateral pnp transistors find use as current sources, level shifters, and input stages.

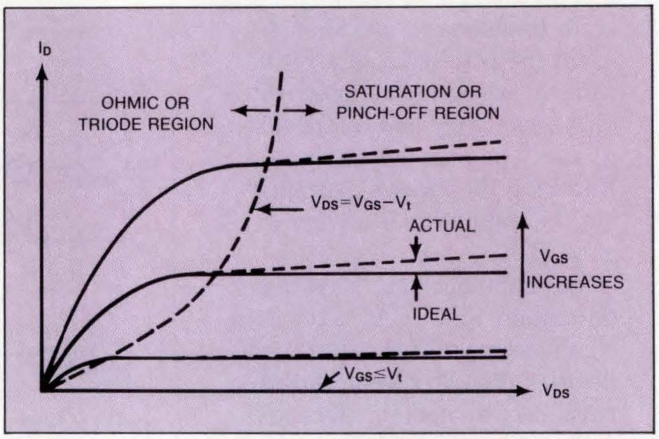

Fig 4—This characteristic of an NMOS transistor *plots conduction from the linear region to the switched region as a function of V_{GS}.*

MOS pros and cons

Manufacturers of linear ICs have used bipolar technology for a much longer time than they've used CMOS. However, many of today's applications employ CMOS to great advantage. The use of CMOS is especially valid for designs that must implement a sampled-data system. CMOS is very useful when a high degree of interconnection exists between analog and digital functions, such as in data-acquisition systems. Whereas linear bipolar devices are best suited for use in a current-steering mode, CMOS circuits work best in switching-type applications. This mode (always-on) eliminates the problems that storage-time delays create when the devices switch.

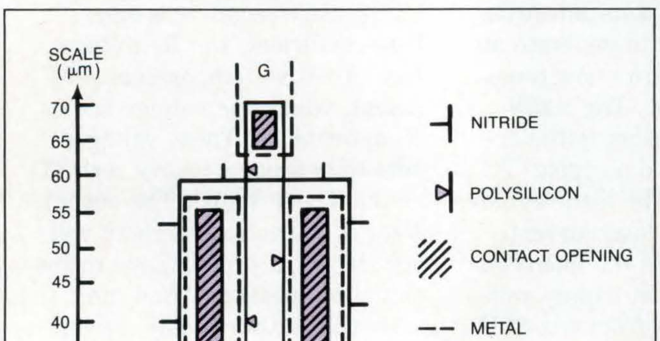

Fig 3—This layout of a typical n-channel, silicon-gate MOS transistor *shows the coding for the mask layers and the scale in microns.*

MOS devices, which use voltage rather than current to control their conduction characteristics, have both advantages and disadvantages. Their advantages include low input currents, high input impedance, and excellent logic compatibility. Their disadvantages involve higher noise, poorer matching (caused by processing and environmental variables), and a lower effective transconductance than that of bipolar devices of the same die size.

Fig 3 shows the layout of a typical n-channel MOS device. As the gate-to-source voltage (V_{GS}) varies **(Fig 4)**, the lateral conduction through the channel varies from the linear region to the switched region. This action illustrates a principal challenge in linear MOS designs—that of keeping the device properly biased. Unlike the base input of a bipolar transistor, the isolated gate of an MOS transistor exhibits a high input impedance and only a small diode-leakage current. This characteristic allows MOS devices to have low leakage currents at low temperatures and to function well as analog switches.

As current sources, MOS devices provide high output impedance; as switches, they allow bidirectional current flow and exhibit much lower impedance than that of bipolar devices. Voltage-noise performance is worse than that of bipolar devices, however, because running higher current through the MOSFET doesn't lower the noise nearly as much as in a bipolar transistor. Because

TABLE 1—BIPOLAR/CMOS PERFORMANCE COMPARISON

	JUNCTION-ISOLATED BIPOLAR		SILICON-GATE CMOS	
PARAMETER	NPN	LATERAL PNP	N-CHANNEL MOSFET	P-CHANNEL MOSFET
GAIN	VERY GOOD	GOOD	GOOD	FAIR
MATCHING	VERY GOOD	GOOD	POOR	FAIR
INPUT IMPEDANCE	LOW	LOW	HIGH	HIGH
OUTPUT IMPEDANCE	MODERATE	MODERATE	MODERATE	MODERATE
SPEED	VERY HIGH	LOW	HIGH	MODERATE
NOISE	VERY LOW	LOW	HIGH	HIGH
RADIATION RESISTANCE	GOOD	FAIR	POOR	FAIR
CONTROL ELEMENT	CURRENT	CURRENT	VOLTAGE	VOLTAGE
CONDUCTION PATH	VERTICAL	SURFACE	SURFACE	SOURCE

the current flow is lateral, rather than vertical, the transconductance of an n-channel MOSFET is less than 1/10 that of an npn bipolar transistor of the same size. As a result, achieving high-gain-bandwidth op amps is much more difficult with MOS than it is with bipolar devices.

P-channel MOSFETs are similar to n-channel devices in operation and construction, but have reversed polarities. Because they conduct by the movement of holes rather than electrons, p-channel devices operate at much lower speeds than n-channel types. However, PMOS devices are more stable than their NMOS counterparts; designers often use them as input stages for op amps and comparators. For both n- and p-channel devices, manufacturers can control the linear characteristics, such as power and speed, by scaling the width-to-length (W/L) ratio of the channel geometries. Logic transistors have a short channel of about 3 μm. Transistors suitable for use as linear elements generally have device channel lengths greater than 10 μm.

A common practice among manufacturers of CMOS ICs is to use ion implantation to selectively control the devices' operating characteristics. Because radiation affects the threshold voltage of MOSFETs, the devices are often not as well suited for aerospace applications as are bipolar devices. Also, operating at low (3V) supply voltages is generally more difficult with MOS devices than it is with bipolar types.

Table 1 shows a performance comparison between bipolar and CMOS circuits for a number of important parameters, and **Table 2** provides a comparison between bipolar and CMOS circuits in various applications.

Manufacturers of ICs create resistors in several ways. The most common approach is via diffusion or pinch diffusion of reverse-biased active devices. Ion implantation is another method that both bipolar and MOS technologies employ, and some fabrication processes also use sputtered, thin-film resistors.

Several factors determine the characteristics of an IC resistor. Of major importance is the sheet resistivity of the material used to create the resistor—a high value is generally desirable. Sheet resistivity determines the die area required for a given resistor value and tolerance, and the die area determines the cost of the resistor. Another factor to consider is the material from which the resistor is made. A drawback to using silicon for resistors is the nonlinearity of their resistance-vs-voltage characteristic.

The junction isolation separating the resistor from its surrounding material introduces stray capacitance that varies with the applied voltage. Further, a reverse-

TABLE 2—BIPOLAR/CMOS COMPARISON

APPLICATION	BIPOLAR	CMOS
OP AMP	VERY GOOD	FAIR
ANALOG SWITCH	POOR	VERY GOOD
COMPARATOR	VERY GOOD	FAIR
D/A CONVERTER	FAIR	FAIR
REFERENCE	VERY GOOD	POOR
REGULATOR	VERY GOOD	POOR
ACTIVE FILTER	GOOD	VERY GOOD
LOGIC COMPATIBILITY	FAIR	VERY GOOD
<3V OPERATION	VERY GOOD	POOR
RADIATION RESISTANCE	GOOD	POOR

The workhorses of a linear bipolar IC are the small-signal npn and the medium-power npn—roughly equivalent to the discrete 2N3904 and 2N2222.

biased diode associated with each resistor exhibits increased leakage-current flow when subjected to radiation. This radiation susceptibility is a possible contributor to major circuit errors.

It is a simple matter to create resistors from either MOS or bipolar active devices. As an example, **Fig 5** shows a diffused base resistor formed by the transistor's base-diffusion step. Because of the difficulty in controlling the depth and density of the impurity concentration, the resistance value can vary as much as ±30%. The low sheet resistivity, along with a distributed capacitance that is directly proportional to the resistor's value, as well as the need to reverse-bias the parasitic diode, limits the usefulness of this type of resistor.

The temperature coefficient of a base resistor's value varies nonlinearly from −600 ppm/°C at −55°C to 1200 ppm/°C at 125°C. Moreover, the difference in potential between the epi (epitaxial) island and the resistor terminals modulates the value of the base resistor. Although they're the most commonly used resistors in bipolar technology, base resistors require a highly experienced linear-IC designer and skillful layout techniques to avoid serious accuracy problems. An optimal base-resistor layout isn't possible in configurable linear-semicustom arrays.

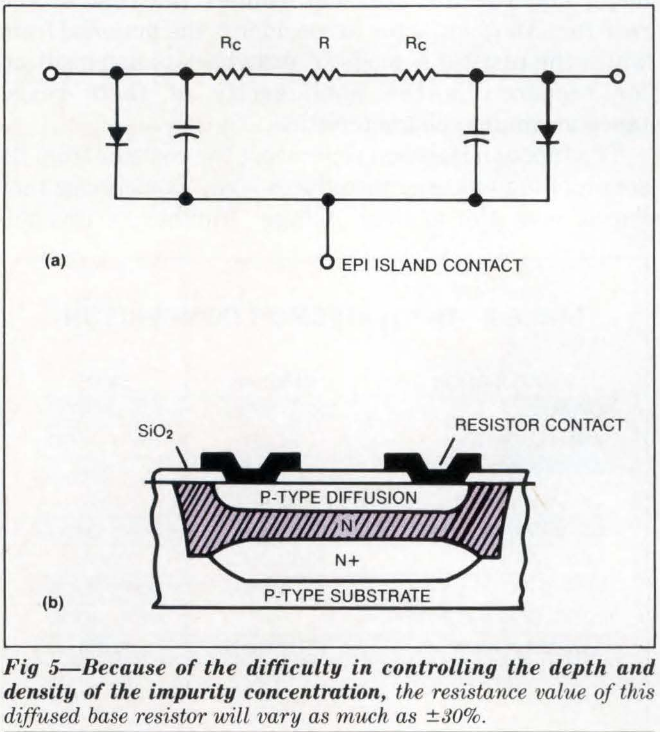

Fig 5—Because of the difficulty in controlling the depth and density of the impurity concentration, *the resistance value of this diffused base resistor will vary as much as ±30%.*

Fig 6 shows a base *pinch* resistor. An extra diffusion (the n+, which ordinarily forms the transistor's emitter) pinches the resistor channel, increasing the effective sheet resistance, but worsening all other characteristics. One disadvantage of the pinch resistor is that its value is directly related to the beta of the npn transistor. Another is that the fabrication process creates a parasitic zener diode that limits the maximum permissible voltage across the resistor.

An epi resistor offers a high sheet resistivity, but otherwise it has poor electrical characteristics. A pinched version **(Fig 7)** of the epi resistor has an even

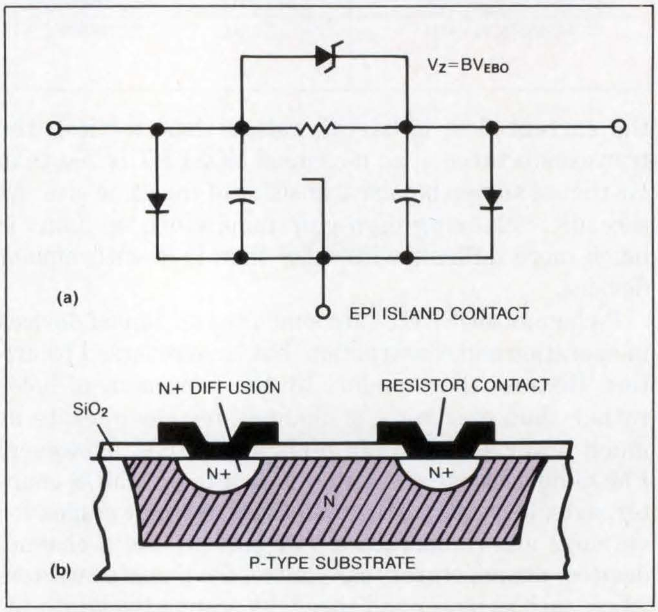

Fig 6—In this equivalent circuit (a) and cross-section (b) of a base pinch resistor, *an extra n+ diffusion pinches the resistor channel, increasing the effective sheet resistance, but worsening all other characteristics.*

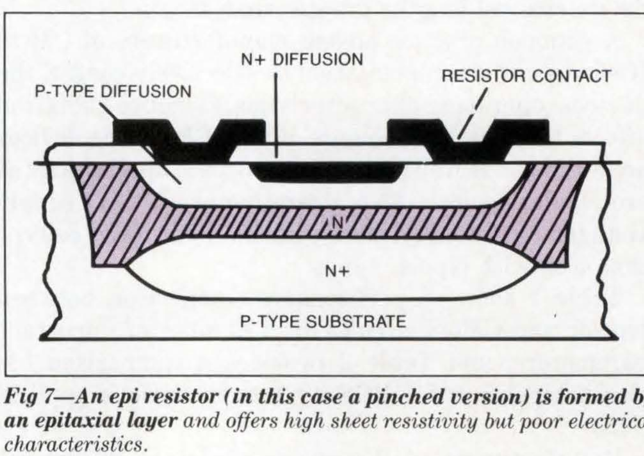

Fig 7—An epi resistor (in this case a pinched version) is formed by an epitaxial layer *and offers high sheet resistivity but poor electrical characteristics.*

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CMOS circuits are best suited to switching applications, or to designs having a high degree of interconnection between analog and digital functions.

TABLE 3—IC RESISTOR-TYPE COMPARISON

RESISTOR TYPE	SHEET ϱ (Ω/□)	ABSOLUTE TOLERANCE (%)	MATCHING TOLERANCE (%)	TEMPERATURE COEFFICIENT (ppm/°C)	VOLTAGE COEFFICIENT	RADIATION RESISTANCE
BASE DIFFUSION	100 TO 200	±20	±2 (10 μm WIDE) ±0.2 (50 μm WIDE)	−600 TO +1200	LOW	POOR
BASE PINCH	2k TO 10k	±50	±10	+2500	VERY HIGH	POOR
EPITAXIAL	2k TO 5k	±30	±5	+3000	HIGH	POOR
EPITAXIAL PINCH	4k TO 10k	±50	±7	+3000	VERY HIGH	POOR
ION IMPLANTED	100 TO 1000	±20	±2 (10 μm WIDE)	+1000	MODERATE	MODERATE
THIN FILM	2k TO 5k	±10	±1	±100	NIL	VERY GOOD

higher sheet resistivity and even poorer electrical characteristics. Fabricators can also create well-type resistors from MOS devices; these resistors offer similarly poor performance.

In CMOS circuits, manufacturers often form resistors by performing ion implantation of polysilicon material. Having oxide isolation, these resistors will tolerate voltages beyond the value of the supplies. Unfortunately, besides harboring a parasitic capacitance, they exhibit a low sheet resistivity (from 100 Ω/square to a maximum of 1000 Ω/square) that limits their usefulness in many applications, especially those requiring moderate resistor values. Processing tolerances in the polysilicon deposition, photolithography, and implant dosages limit the absolute tolerances of ion-implanted resistors to about ±20%.

Your best choice for precision designs is thin-film resistors. Their performance is equal to or better than that of most discrete equivalents, and is much better than that of the silicon resistors previously described. Thin-film resistors have no junction capacitance, are almost perfectly linear, and can tolerate voltages well beyond those of the power supplies. This voltage tolerance is often a major consideration in analog systems, many of which require an overvoltage capability. If you use junction-isolated resistors, the ac performance of the final circuit will often differ from that of the breadboard. Thin-film resistors, however, don't degrade the ac performance relative to that of the breadboard. **Table** 3 summarizes the performance available for the various resistor types.

Capacitors are difficult

Because the dielectrics used in the manufacture of an IC are very inefficient (compared with those found in discrete devices), the fabrication of high-value capacitors in an IC is very difficult. Nitride capacitors (such as those provided in the RLA arrays, as well as in some other manufacturers' ICs) provide higher capacitance and better reliability than do the thin-oxide capacitors that most manufacturers use. However, if your design calls for capacitor values greater than 50 pF, or requires absolute tolerances tighter than ±10%, then your best policy is to keep these capacitors off chip.

Some applications are naturally amenable to the use of on-chip capacitors. For example, active filters operating at frequencies to 50 kHz often lend themselves to the use of switched-capacitor techniques, which you can readily implement in CMOS. In these filters, capacitor values need not be large and the capacitors are easy to integrate. In another example, CMOS sample/hold circuits often include the (small) hold capacitor on chip. **EDN**

Authors' biographies

Bruce Moore is a linear applications engineer at Raytheon (Mountain View, CA), where he is presently involved in ASIC design. Bruce has an EET degree from Heald Engineering College and holds two patents. His hobbies include motorcycle road racing, skiing, and chess.

Will Ritmanich is an IC-design consultant living in Detroit, MI. His previous employment includes Precision Monolithics and Analog Devices. Will has a BSEE from San Jose State and has applied for two patents. His spare-time activities include camping and skiing.

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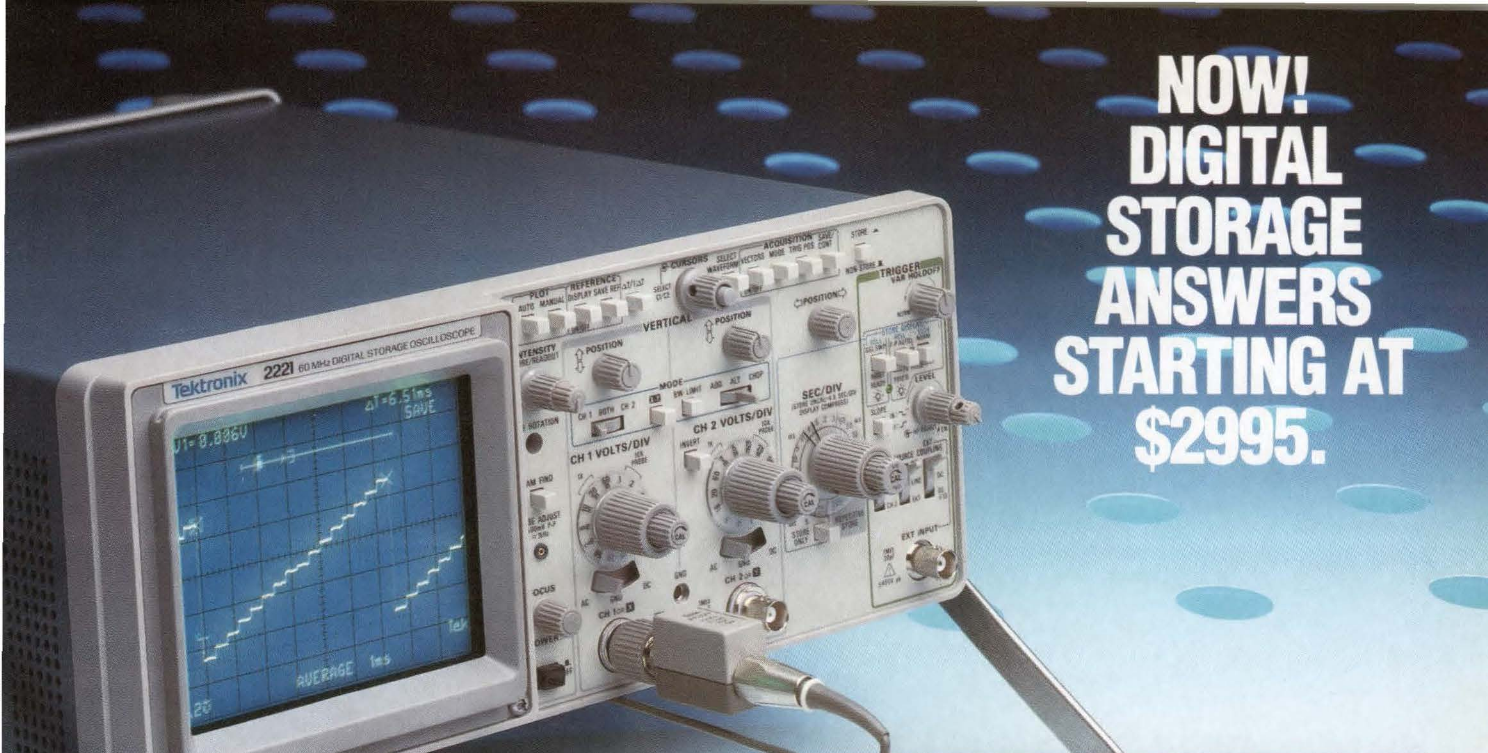

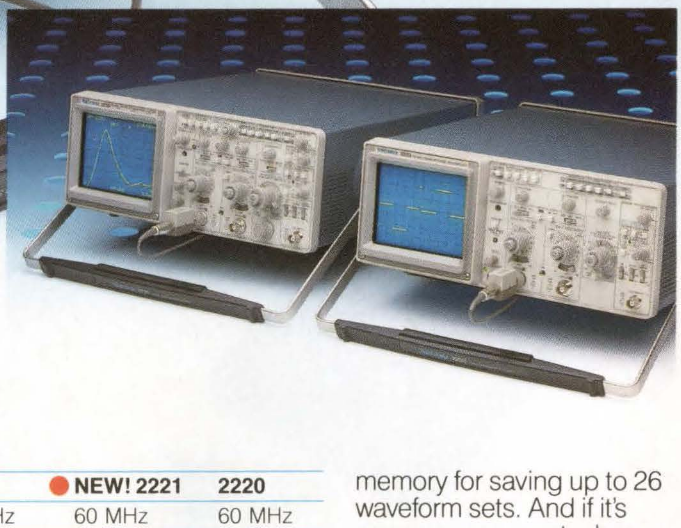

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Save Reference Memory	One, 4K Three, 1K	One, 4K	One, 4K
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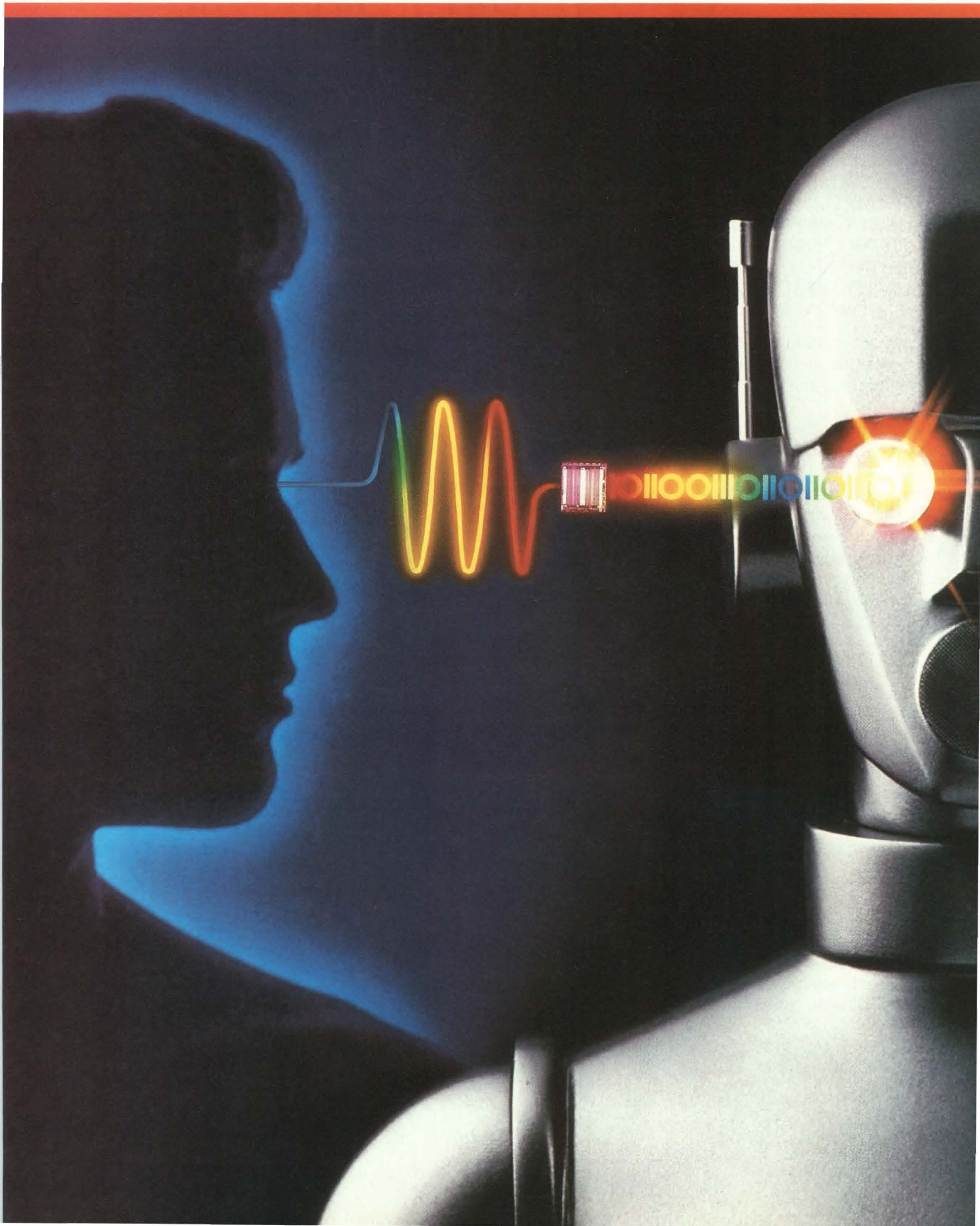

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CA3318E/3318CE	8	15M	150	24	38.50/24.00
CA3310E/3310AE	10	150K	15	24	6.00/8.00
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CA3338E/3338AE	8	50M	100	16	6.00/8.40
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Wren V	442	16	ESDI	10
Wren V	383	14.5	ESDI	10
Wren V	344	16.5	SCSI	10-15
Wren V H.H.	190	18	SCSI	10-15
Wren IV	307	16.5	SCSI	10-15
Wren III	182	16.5	ESDI	10
Wren III	160	16.5	SCSI	10
Wren III H.H.	106	18	ESDI	10
Wren III H.H.	91	18	SCSI	10
Wren II	96	28	ST506,ESDI	5
Wren II H.H.	51	28	ST506	5

H.H. = Half High Models
SCSI models list usable capacity formatted in 1024 Byte sectors.
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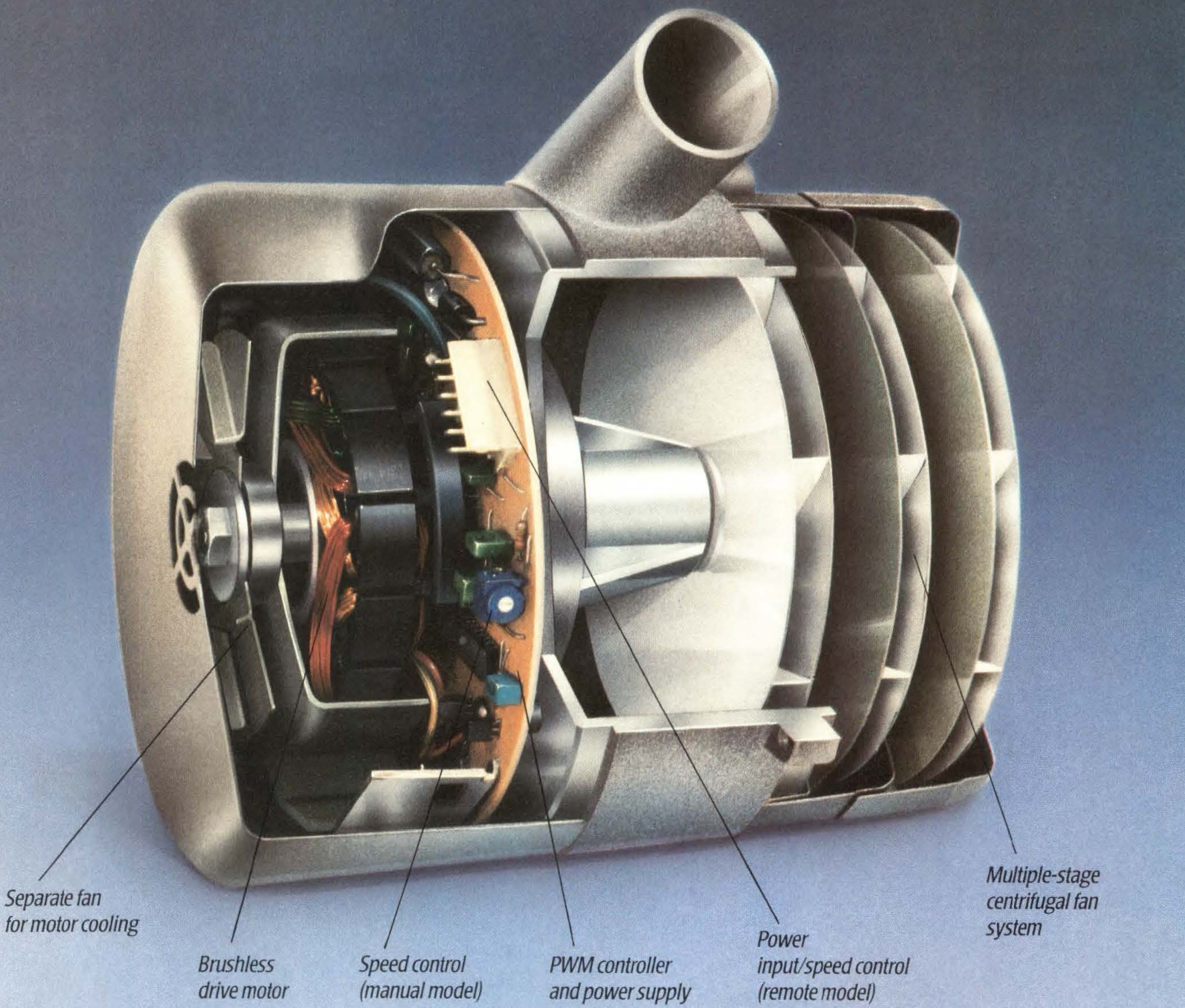

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S/H amp-ADC matrimony provides accurate sampling

When using an A/D converter to capture samples of moving signals, you usually need a sample-and-hold amplifier to hold the voltage steady at the converter's input. If you don't choose the right S/H amplifier for the application, signal degradation in the form of distortion and reduced dynamic range invariably results.

Al Little and Bob Burnett, *Harris Corp*

Choosing the optimum sample-and-hold amplifier for a particular A/D converter in a given application is often not an easy matter. The choice depends on the speed and resolution of the converter, the system's sampling rate, and several other variables. A less-than-ideal S/H amplifier-ADC match can result in reduced system efficiency or in degradation of the sampled signals. The discussion that follows uses three available monolithic S/H amplifiers and several industry-standard A/D converters as examples of how to arrange a harmonious S/H amplifier-ADC marriage for your application. The principles detailed here are universal; thus, they're equally applicable to other available S/H amplifiers and A/D converters.

The principal parameters of an S/H amplifier that come to bear on the accuracy you can obtain in a given A/D-conversion application are acquisition time, hold-mode settling time, aperture time, aperture jitter, pedestal, hold-mode feedthrough, and droop rate. The first four of these parameters set an upper limit on the allowable input frequency and the achievable sampling rate. The input-voltage-dependent pedestal can introduce nonlinearities into an S/H amplifier's transfer function. Finally, feedthrough introduces accuracy errors, and droop imposes a limit on the length of the A/D-conversion period. Before studying the effect of these parameters on A/D conversions, it's useful to review the parameters in some detail.

S/H terms are esoteric

Data sheets for S/H amplifiers use many terms that are peculiar to these devices. Sometimes they use several different terms for the same spec. The waveforms in **Fig 1** illustrate the parameters that are of principal interest in arranging a good match between an S/H amplifier and an A/D converter. First, consider the acquisition time. This quantity is the time the S/H amplifier requires to sample (more accurately, to track) the input signal to within a given error band after it receives a Sample command.

S/H-amplifier manufacturers usually specify the slew rate for the hold-to-sample transition. Note, however, that the acquisition-time spec takes into account both slew rate and settling from any overshoot and ringing. (If you want to calculate the specific effects of input slew rate on the S/H amplifier's overall performance, see **box**, "Take finite S/H-switch time into account.") Many data sheets specify acquisition time for two error bands: ±0.1% and ±0.01%. The ±0.01% figure equates roughly to ±½ LSB for a 12-bit conversion.

After acquiring the input signal, the S/H amplifier

An inappropriate match between an S/H amplifier and an A/D converter can result in degradation of the sampled signal.

tracks the signal until it receives a Hold command. Their internal connections commit many S/H amplifiers to unity-gain operation; the HA-2420, -5320, and -5330 families, however, contain uncommitted input amplifiers that allow feedback-determined gain in inverting or noninverting configurations. The two intervals immediately following the Hold command are aperture time and hold-mode settling time.

Aperture time is the interval required before the S/H switch can open; hold-mode settling time is the interval, after the receipt of a Hold command, in which the output settles within a given error band about its final settled value. The hold-mode settling time, which includes the aperture time, is the parameter of interest here, because the settled, held voltage is presented to the S/H amplifier's mating A/D converter during the conversion cycle. Aperture jitter (or uncertainty) is also of particular interest; it imposes a limit on the allowable input frequency.

When the S/H amplifier's output settles after the reception of a Hold command, it doesn't exactly settle to the value of the previously tracked input voltage imposed on the hold capacitor. Because of unavoidable stray capacitance between the S/H-command input and the hold capacitor, the sample-to-hold transition causes charge to transfer to the hold capacitor. According to V=Q/C, this charge produces a voltage step in the capacitor. This step is variously called pedestal (as in **Fig 1**), charge injection, offset step, hold step, or sample-to-hold offset.

To complicate matters, the pedestal is not always a constant quantity. It can be a function of the amplitude and the transition time of the S/H command, for example, and sometimes it can vary as a function of the analog input voltage. This latter dependency is itself a function of the S/H amplifier's architecture. **Fig 2** shows how a device's architecture can have a bearing on the relationship between pedestal and input voltage.

Two basic S/H-amplifier architectures are evident in **Fig 2.** In **Fig 2a,** the input amplifier, upon closure of the Sample/Hold switch, charges the hold capacitor to the voltage level to be held. After the switch opens, the hold capacitor has no discharge mechanism except the input-bias current of the output amplifier and the leakage resistance of the open switch, so it holds the sampled voltage. In **Fig 2b,** the input transconductance

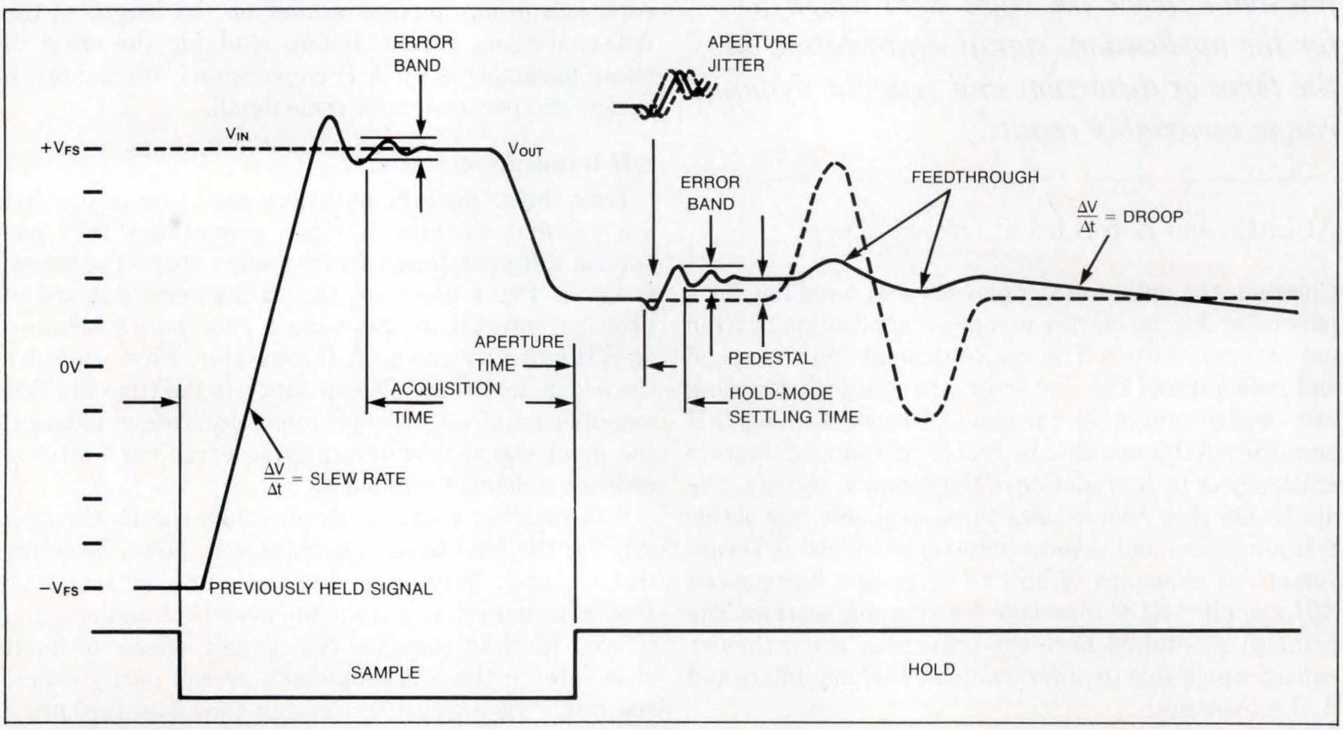


Fig 1—S/H amplifiers need their own dictionary, *as witness the esoteric terms in this timing waveform. What's more, many of the parameters can have several alternate names. For example, aperture time is sometimes called aperture delay, aperture jitter is also called aperture uncertainty, and pedestal is also referred to as charge injection, hold step, offset step, and sample-to-hold offset. The important parameters for timing considerations are acquisition time, hold-mode settling time, and aperture jitter.*

amplifier, upon closure of the switch, charges a hold capacitor connected in the feedback loop of the output amplifier. The amplifier provides a charging current proportional to the differential input voltage.

In **Fig 2a,** the voltage at the junction of the hold capacitor and the input of the output amplifier varies directly as a function of the input voltage. On the other hand, in the integrating configuration of **Fig 2b,** this junction is a virtual ground, held at 0V by negative feedback. The problem is that the amount of charge transferred to the hold capacitor in **Fig 2a's** circuit is a function of the voltage on the hold capacitor. This

Take finite S/H-switch time into account

Some of the specifications commonly given in S/H-amplifier data sheets can be misleading or confusing. For example, a data sheet might specify acquisition time for a 10V static signal, but not for a rapidly moving input signal.

Similarly, aperture time indicates the time it takes for the Sample/Hold switch to open from 10 to 90%. It's useful to study the effects this finite switch-opening time has on overall performance. In analyzing the effects, it's convenient to think in terms of a simplified equivalent circuit for an S/H device such as the one in **Fig Aa. Fig Ab** shows such a simplified circuit for the very fast, transconductance-input types of S/H amplifiers, such as the HA-5320 and -5330.

In this simplified form, the circuit is easily recognizable as a simple lowpass configuration. The characteristics of the lowpass circuit lead directly to the analysis of the S/H circuit. For example, high-frequency signal components will suffer from phase lag through the RC circuit. This simple circuit makes it possible to estimate the quantitative capacitor error voltage during the acquisition phase for any given signal.

Similarly, it's also possible to estimate sampling errors arising from aperture time. For example, suppose you're digitizing a 2V p-p, 20-kHz signal. The maximum rate of change, occurring at the signal's zero-crossing point, is given by

$$\frac{dV}{dt}(\text{MAX}) = \frac{d}{dt}\left[\sin 2\pi(20\text{ kHz})t\right]_{t=0}$$
$$= 1.257 \times 10^5\text{V/SEC.}$$

As the switch opens **(Fig Ac),** the resistance increases exponentially. To make a worst-case estimate, you can assume that for, say, a 10-nsec aperture time, the switch remains closed for an additional 5 nsec. What error voltage results from this prolonged closure? The capacitor continues to be charged at the rate of 125,700V/sec. For 5 nsec, the error is 628 μV, which is approximately a ¼-LSB error for a 12-bit, 10V FSR A/D conversion.

Modeling the S/H amplifier in this way gives you some insight into how the different S/H-amplifier specifications figure into the overall accuracy of the device for any particular application.

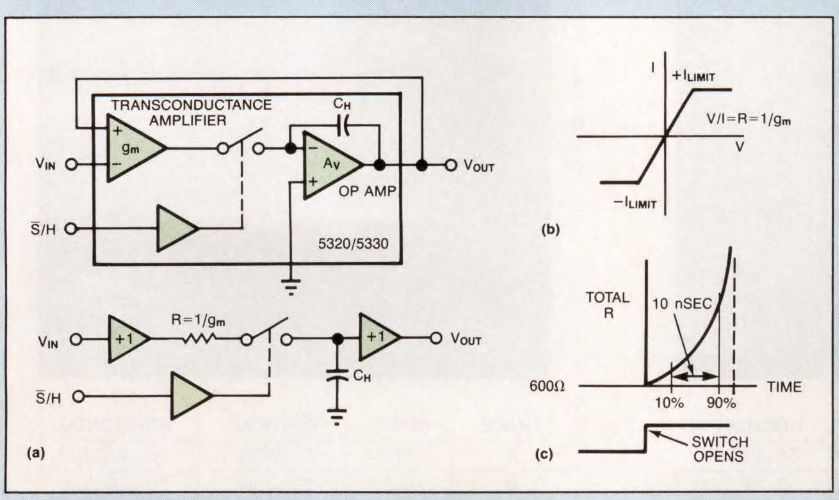


***Fig A—Modeling a sample-and-hold amplifier** such as the HA-5320 or HA-5330 **(a)** with a simplified equivalent circuit **(b)** enables you to understand the effects of finite aperture time. In the sample mode (switch closed) the R and C components introduce increasing error because of phase lag vs frequency. Then, following the switch-open command, the switch causes additional error by allowing the capacitor to continue charging for several nanoseconds **(c)**.*

To avoid harmonic surprises in sampled signals, be aware of how an S/H amplifier's pedestal varies as a function of the amplitude of the voltage to be sampled.

problem is compounded by the fact that the Sample/Hold switch often displays nonideal characteristics. For example, if the switch is a MOSFET, the gate-to-source (that is, S/H-logic-to-hold-capacitor) capacitance can vary as a function of the gate-to-source voltage, and hence as a function of the input voltage.

The scope photos in **Fig 3** illustrate the dependence (or independence) of the pedestal on input voltage. For all three photos, traces A, B, and C show the pedestals that occur for input voltages of +10, 0, and −10V, respectively. For **Fig 3a,** the S/H amplifier is an HA-2420 using a 1-nF hold capacitor. This IC is a nonintegrating device that uses the architecture shown in **Fig 2a.** The S/H units for **Figs 3b** and **3c,** the HA-5320 and -5330 (respectively), use the integrating structure shown in **Fig 2b.** You can see that both the pedestal and its variation are much smaller—in fact, negligible—for the integrating types.

Fig 4 shows the typical dependence of the pedestal on the input voltage for the HA-2420. The coordinates for the 1-nF curve come from the scope photo in **Fig 3a;** those for the 100-pF curve are from typical curves in the data sheet. As you can see, the pedestal with the 1-nF hold capacitor varies linearly with the input voltage. It's a simple matter to derive the equation for pedestal vs input, then to prove that this linearly

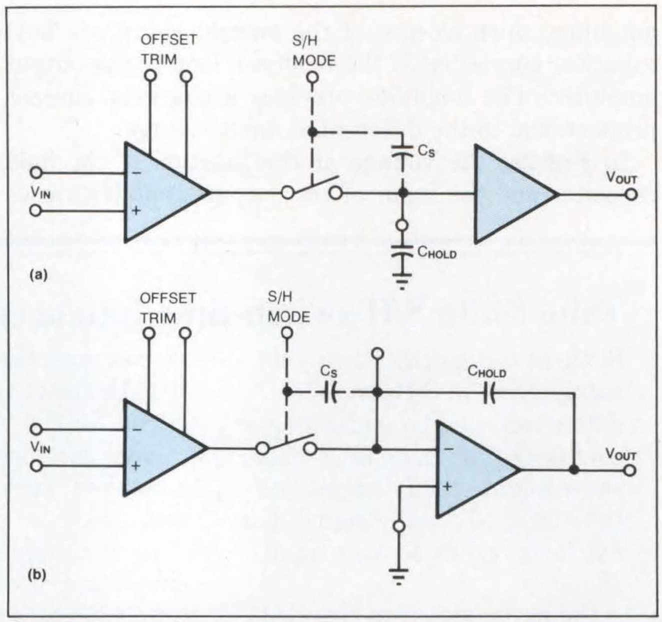
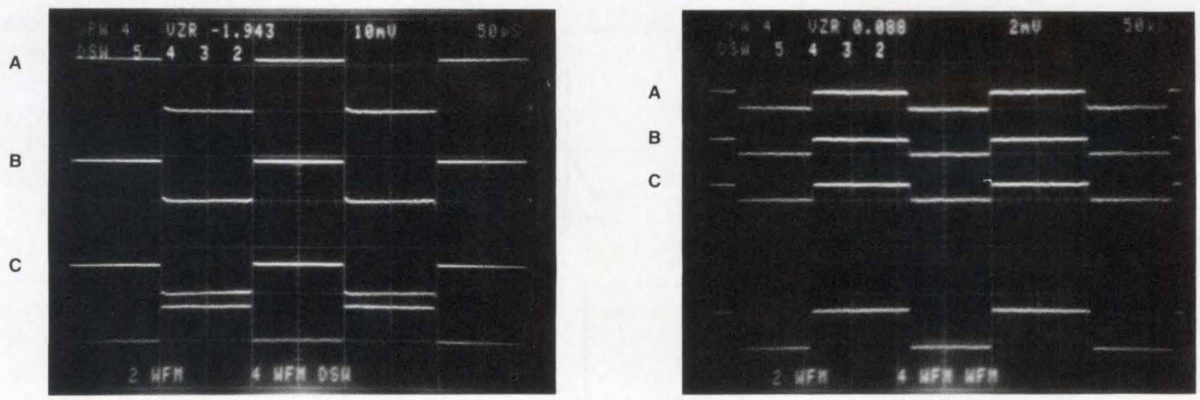


Fig 2—The architecture of an S/H amplifier has a profound influence on the device's pedestal. *In circuit configuration* ***a,*** *the voltage at the output amplifier's input terminal varies with the input voltage. This variation causes changes in the value of the stray capacitance C_S, and thus causes variations in the pedestal as a function of the input level. In* ***b'****s circuit, the voltage at the summing junction is invariant with input voltage; therefore, the value of C_S remains constant. The result is a constant pedestal voltage, which only adds a fixed offset to the S/H amplifier's output.*



(a)

TRACE	INPUT	VERTICAL	HORIZONTAL
A	+10V	10 mV/DIV	50 μSEC/DIV
B	0V	10 mV/DIV	50 μSEC/DIV
C	−10V	10 mV/DIV	50 μSEC/DIV

(b)

TRACE	INPUT	VERTICAL	HORIZONTAL
A	+10V	2 mV/DIV	50 μSEC/DIV
B	0V	2 mV/DIV	50 μSEC/DIV
C	−10V	2 mV/DIV	50 μSEC/DIV

Fig 3—Nonintegrating S/H amplifiers display a variable pedestal, *as seen in* ***a.*** *The pedestal for the HA-2420 under test varies from −6 mV for a −10V input to −11 mV for a +10V input. The HA-5320 and HA-5330 are integrating S/H devices; therefore, their pedestal is not a function of the input level, as seen in* ***b*** *and* ***c.*** *A linearly variable pedestal adds an offset to the S/H amplifier's output; a nonlinearly variable pedestal contributes nonlinearity in the form of harmonics.*

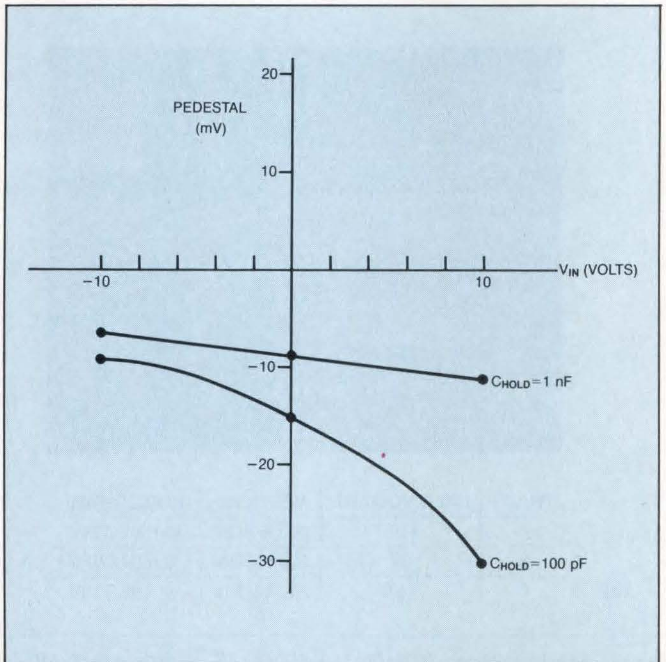
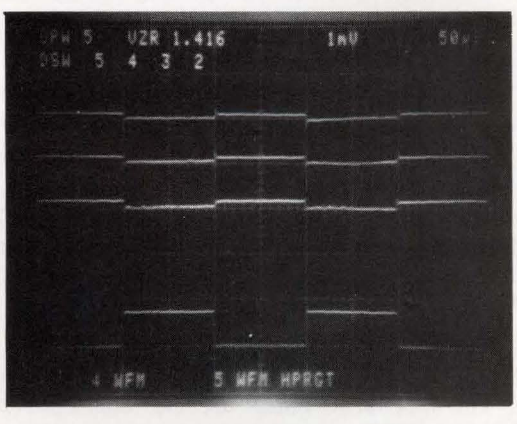


*Fig 4—**Based on measurements made at 95°C on a nonintegrating S/H amplifier** (the HA-2420), these curves show that the pedestal is a strong function of the input voltage. In the curve measured with a 1-nF hold capacitor, the pedestal varies linearly with input. For a configuration using a 100-pF hold capacitor, the pedestal-input relationship is a second-order one, and the result is harmonic distortion.*

A
B
C



TRACE	INPUT	VERTICAL	HORIZONTAL
A	+10V	1 mV/DIV	50 μSEC/DIV
B	0V	1 mV/DIV	50 μSEC/DIV
C	−10V	1 mV/DIV	50 μSEC/DIV

(c)

varying pedestal does not introduce nonlinearities in the S/H amplifier's transfer function:

$$
\begin{aligned}
P &= -0.0025V_{IN} - 0.009\\
V_{OUT} &= V_{IN} + P\\
&= V_{IN} - 0.0025V_{IN} - 0.009\\
&= 0.99975V_{IN} - 0.009\\
V_{IN} &= 10\sin\omega t\\
V_{OUT} &= 9.9975\sin\omega t - 0.009,
\end{aligned}
$$

where P is the pedestal in volts. These expressions reflect a ±10V sinusoidal input signal. The result shows that the linearly varying pedestal introduces a 0.025% gain error and a constant 9-mV negative offset voltage in the transfer function. You can easily compensate for these errors by simply adjusting the gain and offset of the S/H amplifier. The effects of a nonlinearly varying pedestal, however, are more insidious. The following expressions are based on a second-order (quadratic) pedestal-input relationship, derived from the coordinates of the 100-pF curve in **Fig 4**.

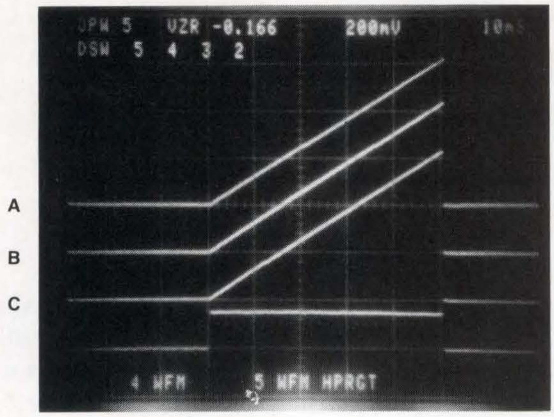
$$
\begin{aligned}
P &= -0.000045V_{IN}^2 - 0.00105V_{IN} - 0.015\\
V_{OUT} &= V_{IN} + P = 0.99895V_{IN} - 0.000045V_{IN}^2 - 0.015\\
V_{IN} &= 10\sin\omega t\\
V_{OUT} &= 9.9895\sin\omega t - 0.0045\sin^2\omega t - 0.015\\
\sin^2\omega t &= \frac{1 - \cos 2\omega t}{2}\\
V_{OUT} &= 9.9895\sin\omega t + \mathbf{0.00225\cos 2\omega t} - 0.01725.
\end{aligned}
$$

The obvious result of the nonlinear pedestal-input relationship is harmonic distortion. The $0.00225\cos 2\omega t$ term indicates that the output voltage will contain a 4.5-mV p-p second-harmonic term; this amplitude represents almost 1 LSB for the ±10V input range under discussion. A good way to minimize pedestal-induced nonlinearity in an S/H amplifier is to reduce the input excursions. For example, when using the HA-2420 with an industry-standard 574 A/D converter, you'd do well to use the lowest input range available: ±5V or 0 to +10V. A curve-fitting and equation-solving exercise for the −5 to +5V portion of the 100-pF curve in **Fig 4** reveals that the resulting second harmonic measures about 0.75 mV p-p, or only about ⅓ LSB for the 10V full-scale range.

Don't neglect droop

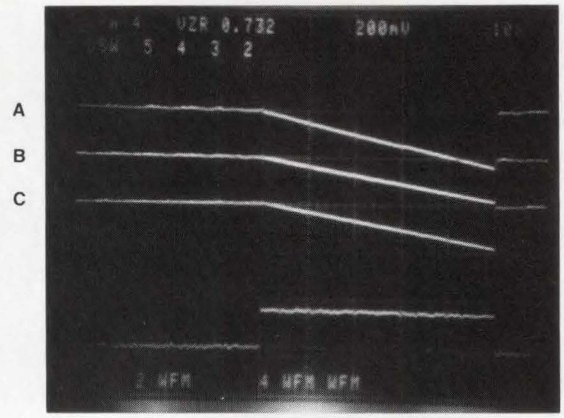
After the output of the S/H amplifier settles to within the specified error band following the sample-to-hold transition, two more error-producing phenomena arise

Acquisition time and hold-mode settling time impose an upper limit on the sampling frequency for an S/H amplifier; droop limits the ADC's conversion time.



TRACE	HELD VOLTAGE	VERTICAL	HORIZONTAL
A	+10V	200 mV/DIV	10 mSEC/DIV
B	0V	200 mV/DIV	10 mSEC/DIV
C	−10V	200 mV/DIV	10 mSEC/DIV

(a)



TRACE	HELD VOLTAGE	VERTICAL	HORIZONTAL
A	+10V	200 mV/DIV	10 mSEC/DIV
B	0V	200 mV/DIV	10 mSEC/DIV
C	−10V	200 mV/DIV	10 mSEC/DIV

(b)

Fig 5—An S/H amplifier's held voltage sags linearly with time, *as seen in these scope photos. In* ***a,*** *the HA-2420's voltage droops (actually, it rises—droop can be positive or negative, depending on the direction of the hold capacitor's discharge current) at 0.4V/sec. For the HA-5320 and -5330 of* ***b*** *and* ***c,*** *the respective droop values are 4.4 and 12V/sec. These droop characteristics were measured at a 95°C operating temperature.*

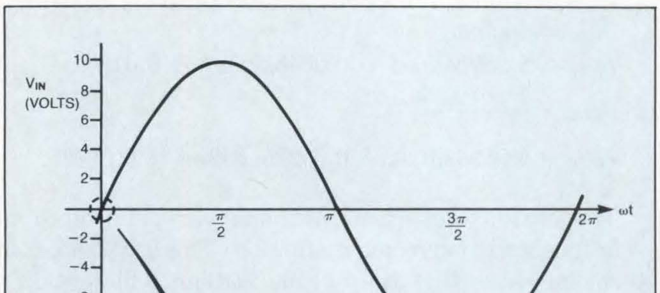


Fig 6—The maximum rate of change for a sine wave *occurs at zero crossing; this fact is both intuitively obvious and easily proven mathematically. For the small angular displacements shown in the expanded view, Asinωt=Aωt, and the maximum rate of change is Aω (10ω for the ±10V sine wave depicted). The ±0.012% ordinates shown correspond to ±½ LSB for a 12-bit A/D converter.*

for consideration: feedthrough and droop. Feedthrough is what its name implies: the transmission of input-voltage variations to the output while the S/H amplifier is in hold mode. For the S/H devices discussed here, this parameter is not a cause for alarm; the feedthrough specs for the HA-2420, -5320, and -5330 are −76 dB, 2 mV, and −88 dB, respectively. In all cases, these figures represent feedthrough that's considerably lower than 1 LSB. Note, however, that you must take measurement conditions (voltage and frequency) into account when interpreting feedthrough specs; these conditions vary in the data sheets for the various available S/H amplifiers.

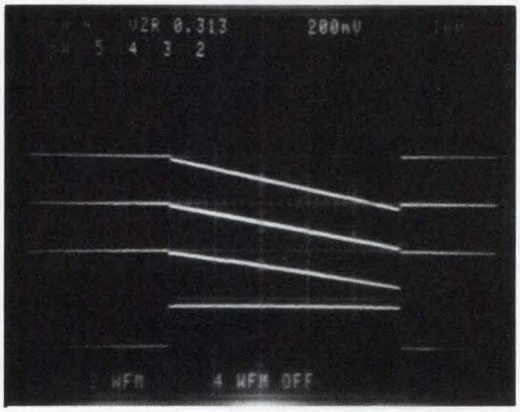
A parameter more worthy of attention is droop. This phenomenon is the change in output voltage that accrues from the inevitable discharge of the hold capacitor. The discharge paths are the bias current of the output amplifier and the leakage current of the Sample/Hold switch, as well as any leakage paths that may exist in external circuitry (in the case of S/H amplifiers using an external hold capacitor).

As is usually the case with semiconductor devices, these currents double with each 10°C rise in junction temperature. **Fig 5** shows the droop characteristics at 95°C for the HA-2420 **(a)**, the HA-5320 **(b)**, and the HA-5330 **(c)**. For this test, the HA-2420 used an

A

B

C



TRACE	HELD VOLTAGE	VERTICAL	HORIZONTAL
A	+10V	200 mV/DIV	100 mSEC/DIV
B	0V	200 mV/DIV	100 mSEC/DIV
C	−10V	200 mV/DIV	100 mSEC/DIV

(c)

external 1-nF hold capacitor; the other two devices used their internal hold capacitors. Take note that the leakage currents (also called drift currents) for some S/H amplifiers can be extremely difficult to measure. The 5-pA typ spec at 25°C for the HA-2420, for example, equates to about $3\times10^{12}\Omega$ impedance. This high impedance level also points up the need to exercise extreme care in laying out a pc board for an S/H amplifier that uses an external hold capacitor. Guarding techniques and moisture-avoidance measures are often necessary for these devices.

According to **Fig 5a,** the highest droop value at 95°C for the HA-2420 occurs with +10V input; at this level, the output voltage droops (or sags) at the rate of 0.4V/sec. For the HA-5320 and HA-5330, the droop figures are 4.4 and 12V/sec, respectively. Again, when you apply the ±½-LSB max criterion for output change, the longest times you can keep these devices in hold mode are 3, 0.27, and 0.1 msec, respectively. Based on the fact that the acquisition and hold-mode settling times are negligible in comparison with these figures, the lowest allowable conversion rates (assuming a 50% duty cycle for the sampling-conversion period) for ±½-LSB max error are 330 Hz, 3.7 kHz, and 10 kHz, respectively.

Slew limits ADC speed

To see why A/D converters usually need the assistance of S/H amplifiers, assume you've just procured a fast, 12-bit A/D converter—for example, the 12-μsec HI-674A. The 12-μsec conversion time tells you the device is capable of an 83-kHz conversion rate. If you were unaware of the idiosyncrasies of successive-approximation A/D converters, you might intuitively jump to the conclusion that the unassisted converter could digitize signals having frequency components as high as 41 kHz. Unfortunately, the allowable input-signal speed is far below this figure. The problem is that for a successive-approximation A/D converter to achieve rated accuracy, the input signal must remain constant (within ±½ LSB) during the conversion cycle.

To understand the implications of this constant-input rule on allowable input frequencies, refer to **Fig 6.** The sine wave represents a ±10V input signal presented to an HI-674 A/D converter, for example. The highest rate of change for the sine wave occurs at the zero-crossing point. The expanded view represents a ±½-LSB excursion around the zero-crossing point. The slope, or rate of change, of the curve at this point is $A\omega$, where A is 10V. If the conversion time, T, is 12 μsec, the maximum permissible rate of change is 200V/sec. When you solve for ω and divide by 2π, you find that the maximum allowable input frequency presented to the A/D converter is 3.2 Hz—a far cry from 41 kHz.

It's thus clear that, in most cases, A/D converters need the assistance of S/H amplifiers. The ADC-S/H mating having taken place, it's natural to assume that the only limitation on the input frequency would be Nyquist's criterion: a maximum of half the sampling frequency. Not so. Referring again to **Fig 1,** you can see that a parameter called aperture jitter or aperture uncertainty imposes a limit on the input's rate of change, and thus on the input frequency. This parameter is the uncertainty concerning the exact time the Sample/Hold switch opens; that is, variations in aperture time from one sample-to-hold transition to another.

Fig 6 shows a ±10V sinusoidal input signal, along with an expanded view of the zero-crossing point (again, the point of maximum rate of change for a sine wave). This time, the positive and negative T values on the time axis correspond to the aperture-jitter spec of an S/H amplifier. Again, the assumption is that ±½ LSB is the maximum variation permitted in the input voltage presented to an A/D converter. For a 12-bit converter, the maximum variation is thus ±0.012%. For the small excursions depicted in **Fig 5,** $A\sin\omega t = A\omega t$. From the aperture-jitter specs (±T) in the S/H amplifiers' data sheets, it's then a simple mathematical exercise to solve for ω, then for f. For the

Aperture jitter—in essence a random modulation of the time the Sample/Hold switch takes to open—imposes a limit on the input signal's slewing rate.

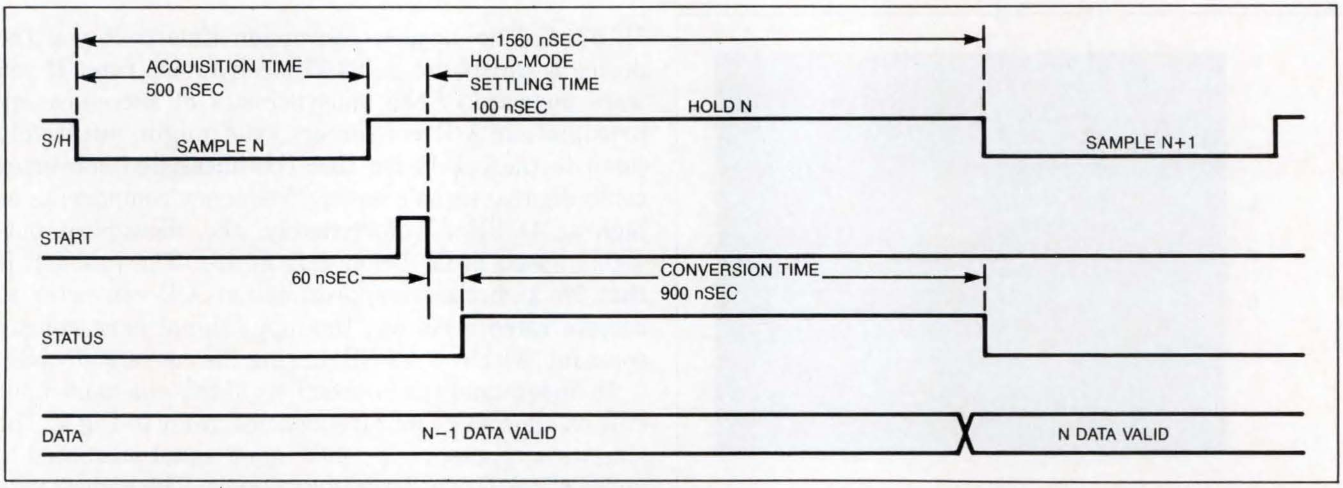


Fig 7—Sample-and-hold cycles and A/D-conversion times are additive, *as this timing diagram shows. Before the A/D conversion can begin, the S/H amplifier must acquire the input signal to within a ±½-LSB error band, and then settle in hold mode to within the same error allowance. This diagram applies to an HA-5330 S/H amplifier working with an MN5245 1-μsec A/D converter. The total acquisition, hold-settling, and conversion period for the S/H-amplifier/ADC combination is 1560 nsec.*

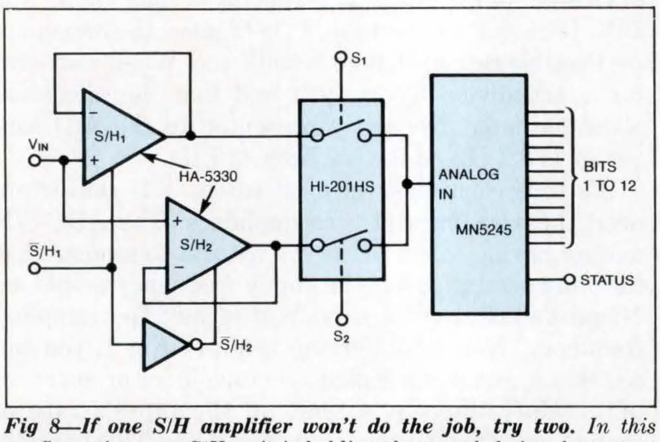


Fig 8—If one S/H amplifier won't do the job, try two. *In this configuration, one S/H unit is holding the sampled signal constant for the A/D conversion while the other S/H amplifier is acquiring the next sample. The result is a nearly 50% increase in sampling rate. If you used this circuit, you might be able to save money by using a slower A/D converter than you could use in a single-S/H-amplifier circuit.*

HA-2420, -5320, and -5330, the input frequencies that produce ±½-LSB max jitter-induced error are 7.6, 127, and 382 kHz, respectively.

Before leaving the topic of aperture jitter, note that this parameter is a relative (sample-to-sample) one, whereas aperture time is an absolute quantity. Because it remains constant from sample to sample, the aperture time has no detrimental effect on the accuracy of sampling for repetitive signals. However, if you must obtain accurate phase-related data for the signal you're sampling, you can simply advance the Hold command by an interval equal to the aperture time.

When using a fast S/H amplifier with a high-speed A/D converter, you must consider your timing budget carefully. The factors that come into play are the S/H amplifier's acquisition time and hold-mode settling time, as well as the A/D converter's conversion time and necessary timing overhead. For example, consider an HA-5330 S/H amplifier operating in tandem with Micro Networks' (and others') MN5245 A/D converter. The S/H unit has a 500-nsec acquisition time; the A/D converter specs 900-nsec conversion time. It might seem natural to jump to the conclusion that the combination can work with a 1400-nsec sampling period, but the conclusion would be wrong. **Fig 7** shows the timing considerations for the pair.

First, the S/H amplifier must acquire the input signal to within a ±0.012% error band; this operation takes 500 nsec. Next, the held signal takes 100 nsec to settle within this error band before the falling edge of the start pulse commands the A/D unit to start converting. A 60-nsec interval ensues between the start command and the conversion interval of the status line. Finally, the conversion consumes 900 nsec, during which the S/H amplifier must hold the acquired signal constant. The entire cycle takes 1560 nsec, not the 1400 nsec you might expect; the maximum sampling rate is thus 641 kHz, rather than 714 kHz.

The speed-limiting factor in this marriage is the fact that the S/H amplifier must hold the acquired signal during the entire conversion period and must not start acquiring a new signal until the conversion is complete. If it were possible for the S/H device to acquire while the A/D converter is converting, the cycle time would be considerably shorter. Fortunately, there is a way to shorten the cycle. If you use two S/H amplifiers and switch between their outputs by using an analog switch, one S/H amplifier can acquire while its companion unit is holding, and vice versa.

Fig 8 gives the schematic diagram of a circuit that embodies the dual-S/H-amplifier scheme. Each S/H

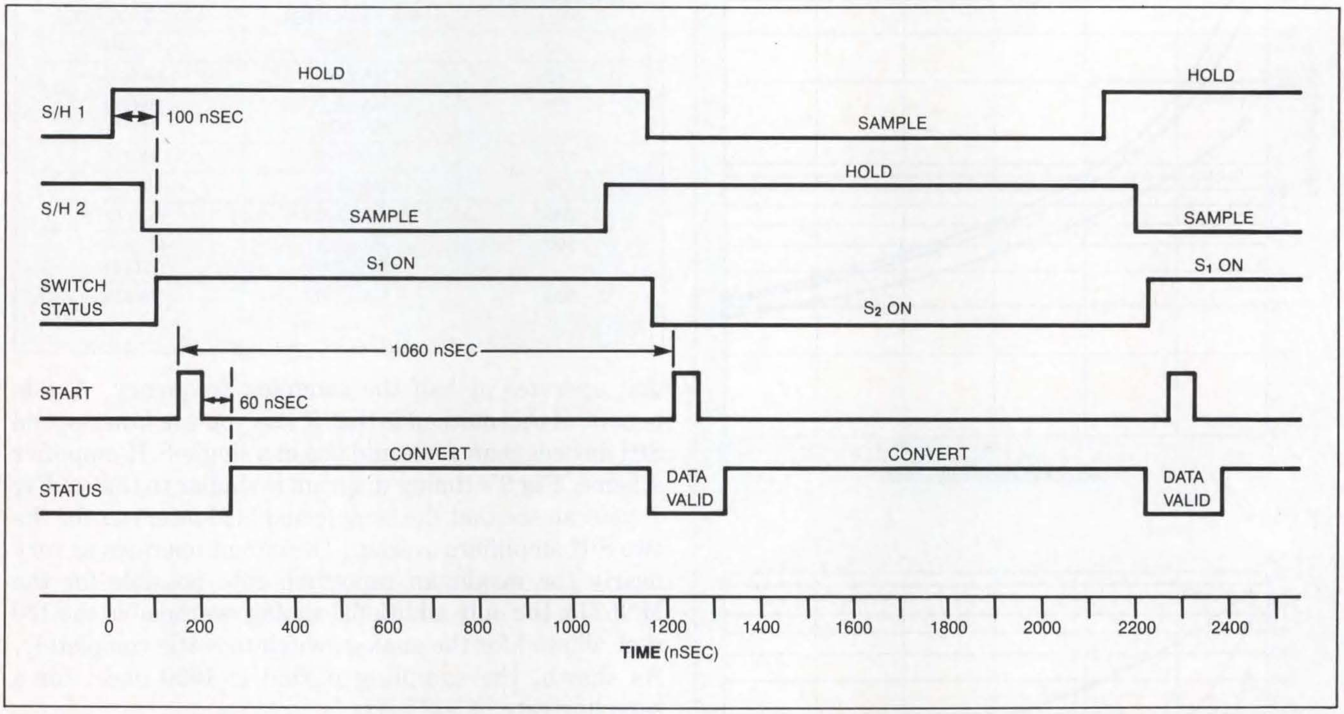


*Fig 9—**Two holds are better than one,** as you can see from this timing diagram for two HA-5330 S/H amplifiers driving an MN5245 A/D converter. Each S/H amplifier operates at half the 943-kHz sampling rate. While one S/H unit is holding the acquired input signal constant for the A/D converter, the other S/H amplifier is acquiring the next sample. The result is an almost 50% increase in sampling rate over that of the configuration that uses only one S/H device.*

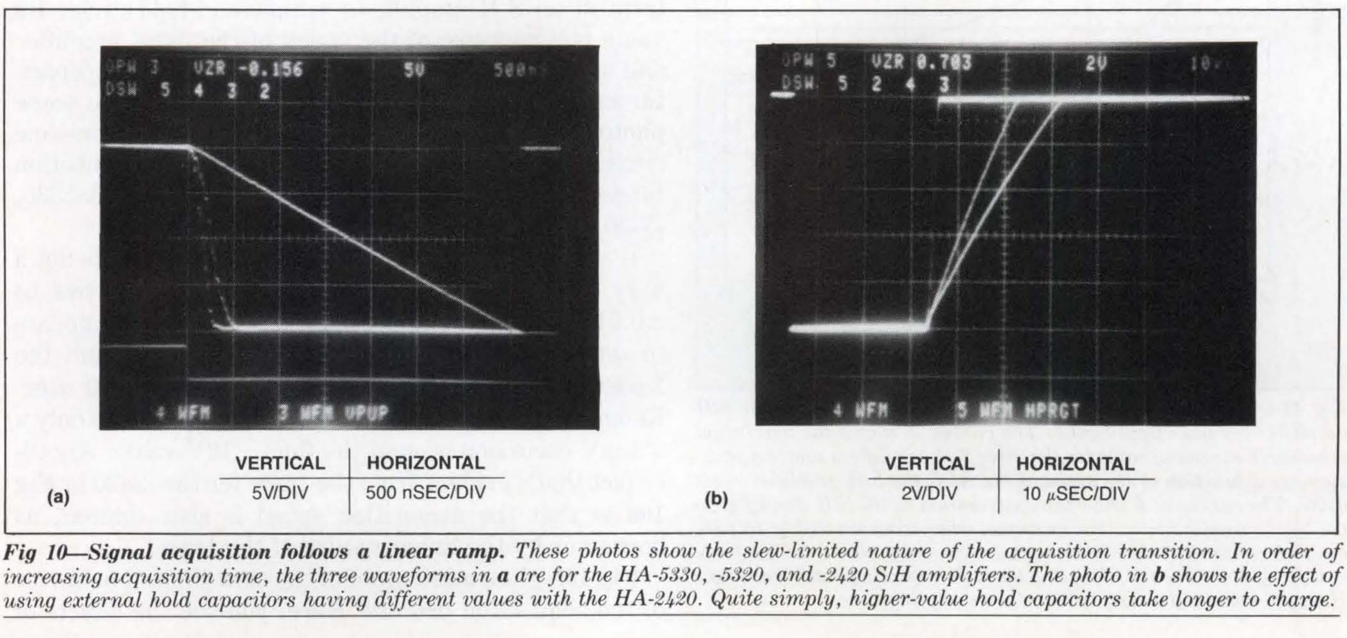


*Fig 10—**Signal acquisition follows a linear ramp.** These photos show the slew-limited nature of the acquisition transition. In order of increasing acquisition time, the three waveforms in **a** are for the HA-5330, -5320, and -2420 S/H amplifiers. The photo in **b** shows the effect of using external hold capacitors having different values with the HA-2420. Quite simply, higher-value hold capacitors take longer to charge.*

By using two S/H amplifiers instead of one to drive a high-speed A/D converter, you can increase the achievable sampling rate by a significant amount.

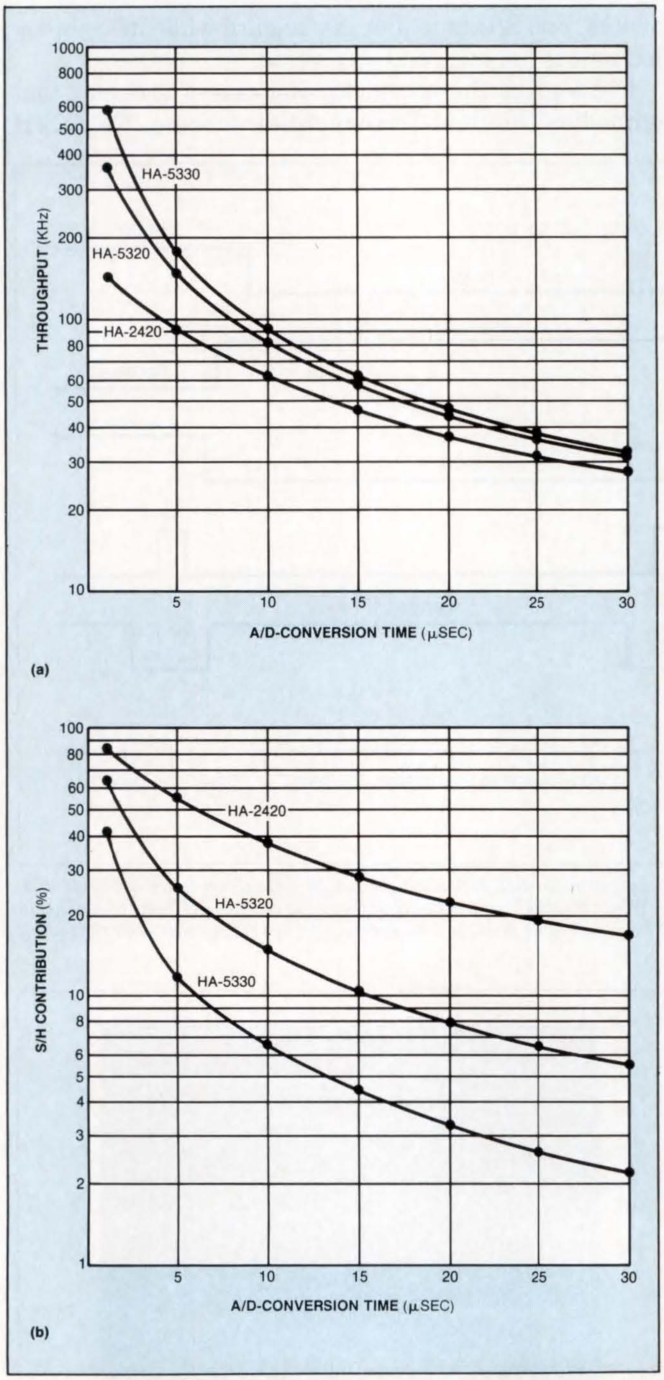


Fig 11—You can use these curves to choose the optimum S/H amplifier *for your application. The curves in* ***a*** *give the maximum achievable sampling rates for the three S/H amplifiers under discussion, as a function of the speed of the ADC the S/H amplifier must drive. The curves in* ***b*** *show the contribution of the S/H amplifier to the total sampling time. For example, when working with a 10-μsec converter, the fast HA-5330 contributes only about 6.5% of the sampling period at the highest achievable sampling rate; the slower HA-2420 contributes about 38% of the sampling time.*

TABLE 1—S/H AMPLIFIER-ADC COMBINATIONS VS THROUGHPUT

THROUGHPUT (kHz)	S/H AMPLIFIER	A/D CONVERTER
30	HA-2420	HI-574A
40	HA-2420	HI-674A
50	HA-5320 HA-2420	HI-674A HI-774
75	HA-5320	HI-774
100	HA-5330	HI-774A
200	HA-5320	ADC-817
300	HA-5320 HA-5330	MN5245 ADC-817
500	HA-5330	MN5245

unit operates at half the sampling frequency. A side benefit of this method is that it lets you use lower-speed S/H devices than you could use in a single-S/H-amplifier scheme. **Fig 9'**s timing diagram is similar to that of **Fig 7;** you can see that the sample and hold intervals for the two S/H amplifiers overlap. The circuit operates at very nearly the maximum repetition rate possible for the MN5245; the only additional timing overhead is the 100 nsec allowed for the analog switch to settle completely. As shown, the sampling period is 1060 nsec, for a sampling rate of 943 kHz.

Acquisition time is the determining factor

As you've seen, acquisition time is the preponderant term in an S/H amplifier's sample-and-hold cycle. Its value is a measure of the speed of the input amplifier and of the amplifier's ability to charge the hold capacitor rapidly to the value of the input signal. The scope photos in **Fig 10** show some typical acquisition-time measurements. **Fig 10a** shows comparative acquisition times for a +10 to −10V input step for the HA-5330, -5320, and -2420, in order of decreasing speed.

It's evident from **Fig 10a** that the naked eye is not a very effective measurement tool when it comes to ±0.01% settling. The 500-nsec (typ) HA-5330 appears to settle in an interval well under 500 nsec, and the 1-μsec (typ) -5320 seems to settle in about 500 nsec. Remember, though, that the ±0.01% represents only a ±2-mV excursion around the final −10V value. Another fact that's evident from the trace for the -2420 in **Fig 10a** is that the acquisition speed is slew limited, as borne out by the linear nature of the trace.

Fig 10b gives more proof of the slew-limited behavior of the acquisition process. Here, you see the effects of

The choice of the right S/H amplifier and ADC for a particular application often entails tradeoffs involving price, speed, and application-related features.

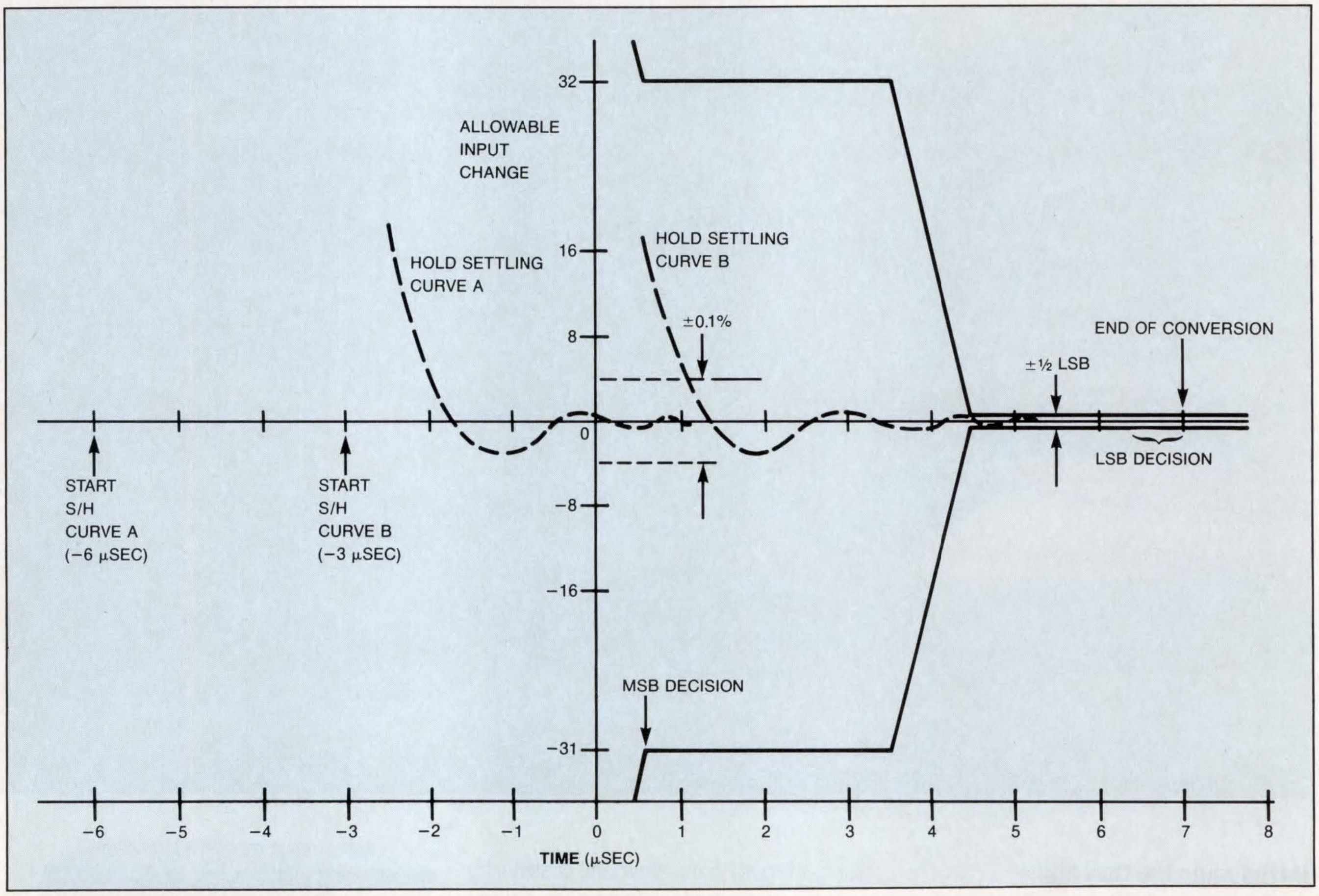


*Fig 12—**A fault-tolerant A/D converter can save time,** as this timing diagram shows. Because the HI-774A A/D converter can tolerate errors as high as +32, −31 LSB during much of its conversion cycle, it lets you initiate a sample-hold cycle much later than you could with less-forgiving converters. By taking advantage of the A/D converter's error-correction mechanism, you can increase the achievable sampling rate by about 30%.*

increasing the value of the external hold capacitor used with the HA-2420. The traces depict acquisition time for a 0 to 10V input step. In order of decreasing speed, the hold-capacitor values are 1, 68, and 100 nF. Again, it's evident from the linear traces that the input amplifier charges the hold capacitor with a constant current.

Timing and budget determine S/H-amplifier choice

Just as it's wasteful to use a cannon to kill a fly, it's unwise to splurge on an S/H amplifier that's overly specified for the application at hand. The prices of both S/H amplifiers and A/D converters, of course, are proportional to the devices' speed. Depending on the required throughput rate in your application, you often have a tradeoff decision to make. The tradeoff involves speed, cost, and application-mandated features in the S/H and A/D units.

Fig 11a can help you select the optimum S/H amplifier and A/D converter for a particular application. For the HA-2420, -5320, and -5330 S/H amplifiers, the curves give the maximum achievable throughput as a function of A/D-converter speed. The A/D-conversion times reflect the total conversion cycle—that is, the specified conversion time plus any timing overhead. For example, the timing overhead for the HI-X74 Series of A/D converters is 200 nsec. **Fig 11b** gives the three S/H amplifiers' percent contribution to total throughput time as a function of A/D-converter speed.

The data presented in **Table 1** comes from the graphs in **Fig 11a.** For each throughput rate, **Table 1** gives appropriate S/H-amplifier/ADC combinations. In each case, the cited S/H amplifier is the minimum (that is, the slowest and least expensive) one that will do the job. You'll note that, for 50-kHz throughput, a tradeoff is possible: the HA-2420 with the HI-774, or the HA-5320 with the HI-674A. Incidentally, in 100-piece quantities,

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It's unwise to splurge on an S/H amplifier that's overspecified for the application at hand.

the first combination is about $5.50 less costly. For throughput rates higher than 200 kHz, the HI-X74 Series has insufficient speed. The high-speed A/D converters chosen for this example are Datel's 2-μsec ADC-817 and Micro Networks' 1-μsec MN5245.

Forgiving ADC saves time

Most successive-approximation A/D converters are of an unforgiving nature. That is, they require that the input voltage be within a ±½-LSB error band of its final value from the beginning to the end of the conversion period. Again, this error band is ±0.012% for a 12-bit converter. However, a slight timing leeway is possible: The input signal doesn't have to reach its final value until the first (MSB) successive-approximation bit decision is made. This decision time varies from converter to converter. The leeway is very slight, however.

You can see, then, that to calculate throughput you must add the S/H amplifier's full acquisition time plus its hold-mode settling time to the ADC's conversion time. A more forgiving A/D converter, the HI-774A, uses error correction to reduce the timing demands on the analog input voltage. **Fig 12** shows that the analog input merely has to settle to within a −31- to +32-LSB envelope for much of the conversion cycle. This leeway lets you effectively advance the beginning of an A/D-conversion cycle in relation to the beginning of a sample-and-hold operation, and thus shorten the total acquisition-hold-conversion time.

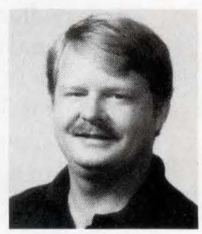
Fig 12 illustrates the timing requirements for an HA-2420 S/H amplifier working in tandem with an HI-774A A/D converter. Curve A gives the timing considerations for the S/H unit operating with a conventional 12-bit A/D converter, one that demands that the input signal be fully settled at the beginning of the conversion. Curve B shows how you can take advantage of the HI-774A's forgiving nature. For curve A, you must take into account the S/H device's full 12-bit acquisition and hold-mode settling times in starting the sample-hold cycle. For the HA-2420, this time is 6 μsec max.

For the situation represented by curve B, you can delay the initiation of the sample-hold cycle such that settling to a lesser accuracy occurs within a safe period at some time well into the conversion cycle. In **Fig 12**, the S/H amplifier settles to within ±0.1% in a 1-μsec interval after the start of the conversion. The HA-2420's spec for acquisition and settling to within ±0.1% is 4 μsec max. You can see that the initiation of the sample-hold cycle for situations A and B must take place no earlier than 6 and 3 μsec before the start of conversion, respectively. The total respective conversion times are thus 13 and 10 μsec, yielding maximum sampling rates of 77 and 100 kHz.

By taking advantage of the HI-774A's input-settling envelope, you can thus increase the conversion rate by about 30%. Note that the throughput rates determined in this example are based on the HI-774A's 7-μsec typical conversion time; the converter's maximum conversion time is specified at 8 μsec. **EDN**

Authors' biographies

Al Little is technical marketing manager for the data/comm product line at Harris Semiconductor. A 7-year employee at Harris, he obtained math and physics degrees from the University of the South at Sewanee, TN; a BSEE from Georgia Tech; and a master's degree in psychology from Nova University in Fort Lauderdale, FL. He holds a patent for an ECG-monitoring amplifier. Al's spare-time activities include playing the piano and electronic music synthesizers.



Bob Burnett is an applications engineer for data-acquisition products at Harris Semiconductor. He holds a bachelor's degree in psychology from the State University of New York at Oneonta, and a BS in electronic technology from the University of Central Florida. His hobbies include bicycling and motorcycling.

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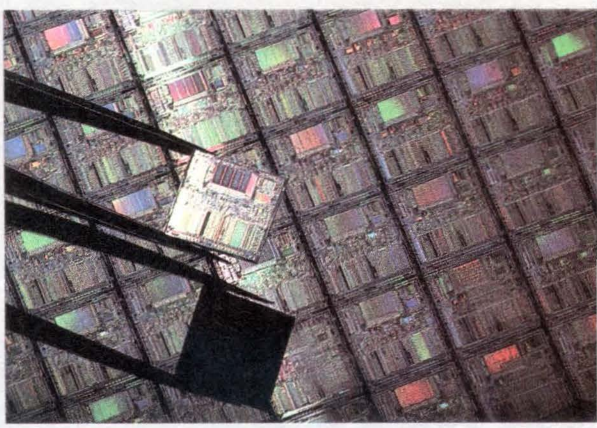

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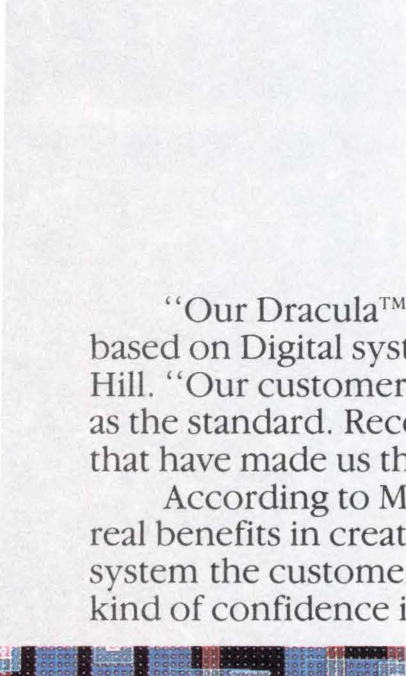

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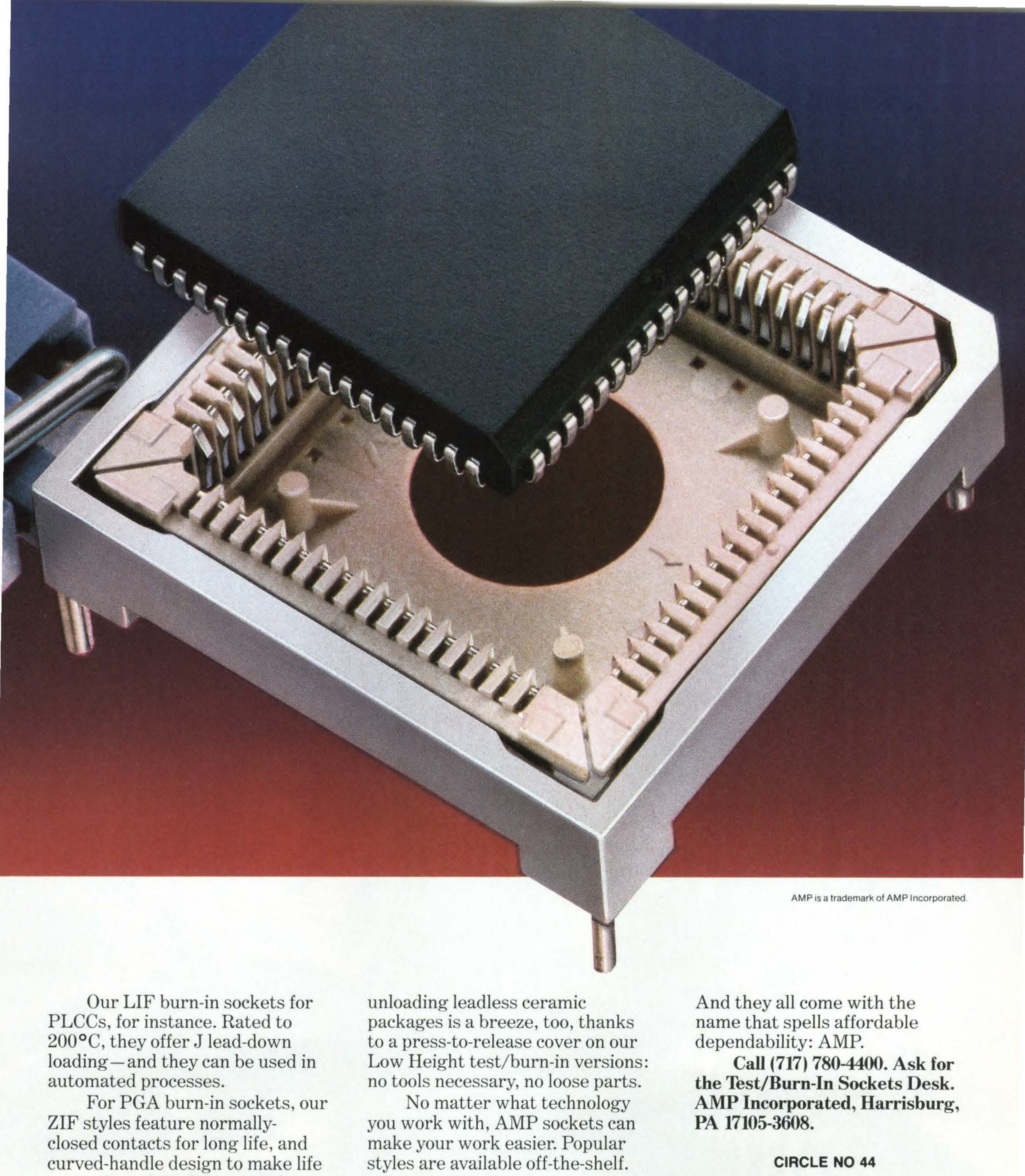

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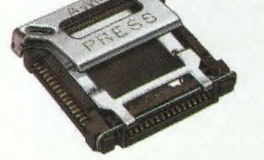

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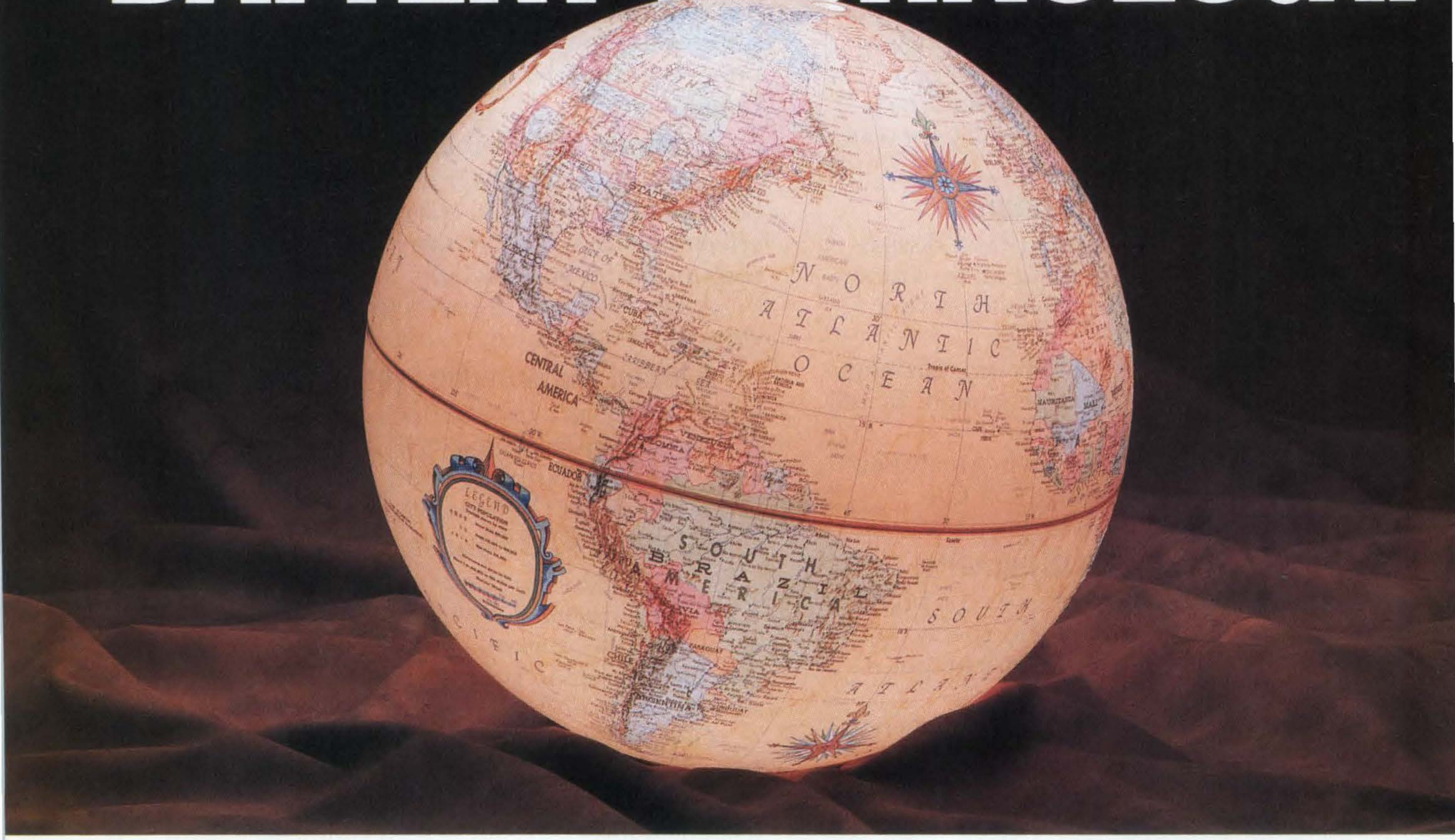

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Heed local norms when designing telecomm interfaces

In designing customer-premises telecomm equipment for foreign markets, you must account for the respective countries' national telecommunications standards. These norms often differ in significant ways from the FCC Rules Part 68, which governs telecomm equipment in the US.

Glen Dash, *Dash, Straus & Goodhue Inc*

Although most of the world's market for installed telecommunications apparatus remains closed to US suppliers, three major markets are open: Canada, the United Kingdom, and Japan. To gain approval for US-built customer-premises equipment (CPE) in these countries, however, you must demonstrate that the apparatus meets the national standards relevant to several aspects of the equipment's interface to the telecomm network (see **box,** "If you need standards information"). By using the test methods described here, you can prove that an installation complies with the key national norms governing safety, electrical performance, and other aspects of a CPE's operation. The tests cover voltage stress, hazardous voltages and currents, pulse and DTMF (dual-tone multifrequency) characteristics, signal power, impedances and line balance, and billing protection.

Many of the criteria for overseas telecomm interfaces differ significantly from the requirements delineated in FCC Rules Part 68, and you must be aware of these criteria during the telecomm equipment's design and testing stage. (**Ref 1** discusses corresponding test methods for Part 68.) Before going into the electrical performance of an export-destined CPE, it's helpful to see how the different countries recommend feeding dc power to the CPE.

In perusing the various standards and their test methods and circuits, note that many of the specs call for specific loop-current settings in the CPEs during testing. Indeed, several of the spec-limit graphs use the CPE's loop current as their abscissa. To impose the necessary dc-feed conditions, the standards offer what are in essence network power-supply schematics. **Fig 1** shows the recommended dc-feed circuitry (also called a loop simulator) for Canada, the UK, and Japan.

The feed circuit for Canada is the most elaborate, as it provides a ringing circuit for bringing the CPE to an off-hook condition. The 0 to 105V adjustable supply (nominally 48V) feeds a variable resistor that allows you to trim the loop current to the value specified for a given measurement. For any test, the + and − terminals connect to the CPE's tip and ring terminals, respectively. (The term "ring" in tip and ring is a carryover from the phone plugs that switchboard operators used in the days of yore.)

In the British telecomm documentation, the dc-feed circuit recommended for most tests makes no provision for ringing the CPE. Instead, the UK specs stipulate a

To gain approval for telephone equipment in foreign markets, you must prove that the apparatus conforms with national norms, according to mandated test methods.

separate circuit for testing the ringer. This configuration, like the Canadian circuit, allows you to adjust the loop current (I). Many of the British standards specify the loop current, and they also offer an alternative: "Compliance shall be checked by the test of (spec No) with an apparatus current of (spec) mA, or the current obtained when the apparatus is connected to a 50V dc source in series with a 400Ω resistor, whichever is the less."

The Japanese seem singularly unconcerned about testing various parameters under varying loop currents; their fixed-value dc-feed circuit for most tests is an inductively blocked 48V dc supply in series with a 440Ω resistor.

First, stresses and surges

National telecomm standards impose various requirements for dielectric strength and for excessive voltages and currents. The purpose of these requirements is twofold. First, the CPE must not subject the telecomm network to excessive voltages. Second, the CPE must protect the user from contact with any hazardous voltages that might originate in the network.

Consider the Canadian test for CPE resistance to voltage surges (lightning, for example). **Fig 2a** gives the Canadian test circuit for surge voltage. As is the case with most of the Canadian standards, it uses the dc-feed circuit of **Fig 1a.** The surge generator in **Fig 2b** provides the controlled-characteristic voltage surge shown in **Fig 2c.** The timing specs for this waveform are complicated and use some very idiosyncratic terms. For example, the waveform is defined as 1000V, 10 μsec max × 1000 μsec min. The 10 μsec, an index of the wave front, is the "virtual duration" of the front. This quantity is 1.67 times the interval for the voltage to rise from 30 to 90% of its crest value. The 1000 μsec, an index of the wave tail, is the interval from the tail's 50% point to "virtual zero," the point of intersection of the 0V abscissa with a line drawn through the tail's 90 and 30% points.

Esoteric terms notwithstanding, the way to perform surge-voltage testing on a Canada-destined CPE is to place S_1 and S_2 in position A and S_3 in position B, and then to fire the surge generator three times. This action applies the surge to the tip terminal; the ring is grounded. Next, place S_2 in position B (thereby reversing tip and ring) and fire the surge generator three more times. Now, adjust the surge generator to produce 1000V, 100 μsec max × 1000 μsec min and repeat the two preceding steps. Next, place S_1 in position B and operate the ring-up circuit to bring the CPE off hook. You then repeat the firings for both connections of tip and ring and for both surge-generator waveforms. Finally, you place S_3 in position A and repeat all the tests. The criterion for passing the surge-voltage test is

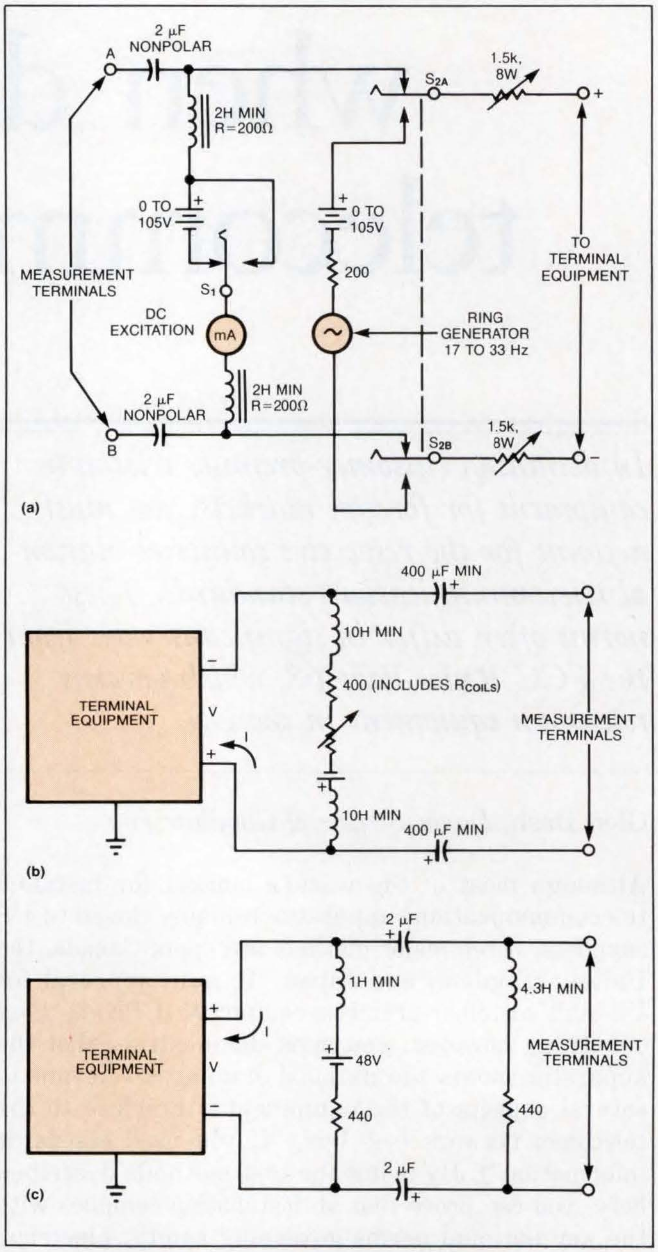


Fig 1—Generate the loop current for your CPE *by using one of these dc power-supply circuits. The Canadian dc-feed circuit* ***(a)*** *has a ringing circuit for bringing the terminal equipment off hook; the British* ***(b)*** *and the Japanese* ***(c)*** *dc-excitation circuits are simpler. All three provide essential capacitive dc blocking to the measurement terminals and inductive ac blocking to the driving-voltage source.*

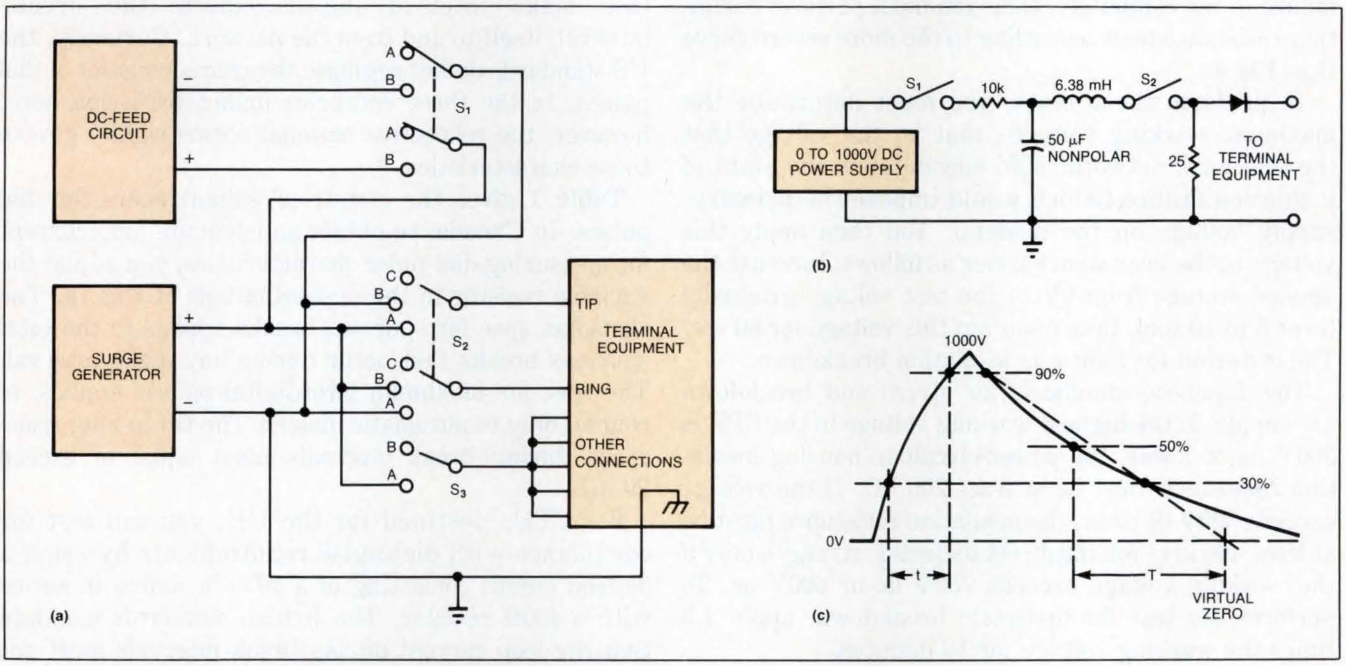


Fig 2—In this Canadian surge-voltage testing scheme, (a), *the surge generator* ***(b)*** *supplies impulses to the tip, ring, and other connections of the terminal equipment. The impulse's wave front and tail must have very particular timing characteristics* ***(c).***

as follows: The test sample, after testing, is fully operational in accordance with the manufacturer's instruction manual, or it must fail in a mode that will not cause harm to the network—for example, permanently on hook.

The UK standards, too, mandate a surge-voltage test to protect users from excessive voltages originating in the telecomm network. A simple RC network provides the surges **(Fig 3)**. To perform the test, you charge the 20-µF capacitor to 1.5 kV. Closing S_1 delivers the impulse to the CPE. The standards require 10 impulses each of both polarities, applied at 1-minute intervals. The terminals of the impulse generator are connected between all network-interface connections and all exposed conducting surfaces on the CPE. After applying the impulses, perform a 500V insulation-resistance test. The measured insulation resistance must exceed 2 MΩ.

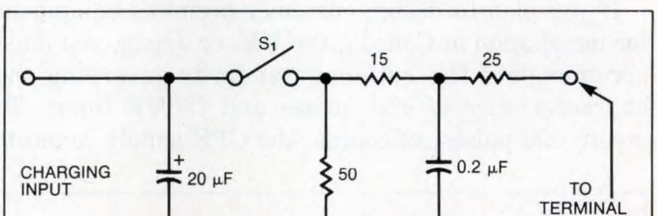


Fig 3—British impulses are easy to generate, *with the help of this simple network. You simply charge the 20-µF capacitor to 1.5 kV, then close S_1. This impulse test is actually a conditioning measure; you perform an insulation-resistance test after applying 10 impulses for each polarity of the terminal equipment.*

Another UK stress test involves measuring insulation resistance. The way you perform the test depends on whether your CPE's insulation barriers must serve as the entire insulation system between the network and any eventual hazardous voltages, or whether it will serve as supplementary insulation.

Consider the example of a modem. It connects to the telecomm network via its DCE port, to a computer via its DTE (RS-232C) port and, perhaps, to an auxiliary telephone handset. If the computer's insulation system complies with British safety standard BS6204, then you can consider the modem's barrier to be supplementary insulation. Satisfying BS6204 in this context means that the DCE-to-DTE interface in the computer is a "class 2" circuit. That is, the supply feeding the interface uses an approved transformer and supplies less than 42.4V at 8A. In this case, you would perform insulation-resistance tests according to curve A in **Fig 4**. If, however, the modem's insulation must be the primary barrier (for example, in the event of insulation

In performing tests to national standards, you must set up a dc supply that simulates conditions in the actual phone network.

failure in the computer), then you must perform insulation-resistance tests according to the more severe curve B in **Fig 4.**

To perform these tests, you must determine the maximum working voltage—that is, the voltage that the telecomm network could encounter in the event of insulation failure (which would impose the primary-supply voltage on the modem). You then apply this voltage to the insulation barrier as follows: Increase the applied voltage from 0V to the test voltage gradually (over 5 to 10 sec), then maintain this voltage for 60 sec. The criterion for failure is insulation breakdown.

The Japanese standards for stress and breakdown are simple. If the highest working voltage in the CPE is 300V dc or lower, the power-circuit-to-housing insulation resistance must be at least 200 kΩ. If the voltage exceeds 300V dc or ac, the insulation resistance must be at least 400 kΩ. You must test dielectric strength only if the working voltage exceeds 750V dc or 600V ac. To perform the test for dielectric breakdown, apply 1.5 times the working voltage for 10 minutes.

Take your pulse carefully

If you plan to design customer-premises equipment for installation in Canada, the UK, or Japan, you must accommodate the national standards governing the characteristics of dial pulses and DTMF tones. To create dial pulses, of course, the CPE simply connects (the "make" interval) and disconnects (the "break" interval) itself to and from the network. Curiously, the US standards do not regulate the characteristics of dial pulses. In the three countries under discussion here, however, the respective national norms rigidly govern these characteristics.

Table 1 gives the countries' salient specs for dial pulses. In Canada, to obtain an adequate loop current for measuring dial-pulse characteristics, you adjust the variable resistor in the dc-feed circuit of **Fig 1a.** The Canadian spec for spurious breaks applies to the total spurious breaks that occur during any make interval. The spec for maximum interdigital pauses applies, of course, only to automatic dialers. The tip-to-ring resistance during break intervals must equal or exceed 20 kΩ.

For CPEs destined for the UK, you can test for compliance with dial-pulse requirements by using a dc-feed circuit consisting of a 50V dc source in series with a 400Ω resistor. The British standards mandate that the loop current during break intervals must not exceed 500 μA. In contrast with most of the very carefully stipulated UK specs, the British spec for dial-pulse distortion is somewhat hazy: "The pulsing performance of the apparatus shall be adequate for

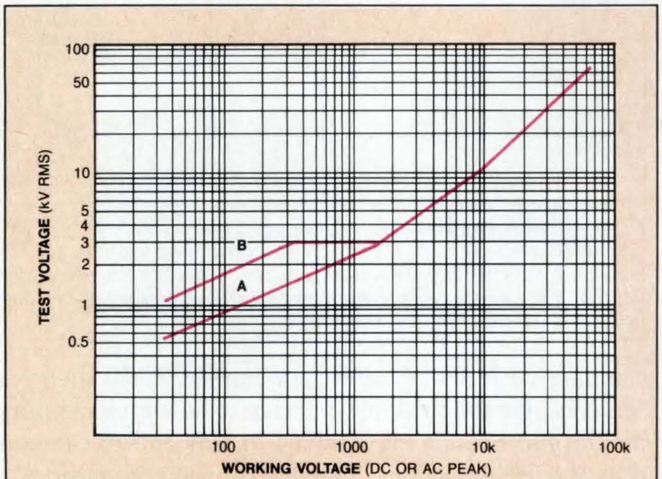


***Fig 4—Insulation resistance is of prime concern in the UK,** and the measurement of it depends on your CPE and its application. Use curve A if the insulation barriers in the other equipment connected to the CPE satisfy British standards. If, however, the insulation barrier in the CPE must serve as the primary barrier in the case of a breakdown, you must test according to the more stringent curve B.*

TABLE 1—DIAL-PULSE CHARACTERISTICS

PARAMETER	CANADA	UK	JAPAN
DIALING RATE (PULSES/SEC)	8 TO 11	9 TO 11	9.21 TO 10.8 OR 18.4 TO 21.6
MAKE/BREAK RATIO	36 TO 42%	28 TO 37%	30 TO 36%
INTERDIGITAL PAUSE	700 mSEC TO 3 SEC	AUTOMATIC: 720 TO 920 mSEC; MANUAL: 240 mSEC MIN	10-PPS MODE: 600 mSEC MIN; 20-PPS MODE: 450 mSEC MIN
SPURIOUS BREAKS	3 mSEC MAX TOTAL	NO SPEC	NO SPEC

TABLE 2—DTMF SIGNAL TONES

LOW (Hz) \ HIGH (Hz)	1209	1336	1477	1633
697	1	2	3	A
770	4	5	6	B
852	7	8	9	C
941	*	0	#	D

normal operation under extremes of conditions and configurations."

The UK standards explain the difference in automatic and manual (rotary-dial) interdigital-pause specs as follows: "Rotary dials normally have a lost-motion period of not less than 240 msec inherent in the design. In addition, it may be assumed that rotary dials have a wind-up time of not less than 180 msec for digit 1, and that the wind-up time increases for other digits. Together with user-selection time, this may be expected to give an average interdigital pause of about 800 msec."

The Japanese standards allow for two dial-pulse-speed classes of CPEs: 10 and 20 pps (pulses/sec). As **Table 1** shows, the ±8% dialing-rate spec is the most rigid of the three countries. The spec for interdigital pauses in Japan is the same for automatic or manual systems. Note that, neither the UK nor Japan, unlike Canada, specify spurious breaks during make intervals. Note also that the Japanese standards do not delineate the dc-feed conditions that must prevail during dial-pulse measurements.

DTMF tests set the tone

One thing the three countries agree upon is the set of DTMF frequency pairs that define the numbers 0 to 9, the asterisk (*), and the pound sign (#). In addition to these characters (found on a standard telephone handset), the tone pairs can define the four letters A, B, C, and D. **Table 2** gives the universally agreed-upon frequencies. Note that Canada, the UK, and Japan also agree upon a ±1.5% max frequency tolerance. Where the countries diverge is in the waveform characteristics and the signal-power levels of the DTMF tones.

Table 3 lists the Canadian, British, and Japanese telecomm standards for DTMF waveform characteristics. You can see that the three sets of specs are widely disparate, and you'll have to take account of these disparities if you're designing equipment for different markets. Consider the rise time of a DTMF waveform, for example. (The rise-time parameter applies to the composite-tone envelope.) In Canada, the rise time is the time it takes the envelope to reach 90% of its final value, starting from the −55-dBm level. The UK defines it as the time it takes the envelope to reach the specified tone-power limits. Japan has no spec at all for rise time.

Disparities in standards become really pronounced regarding DTMF-tone signal levels. In Canada, for example, DTMF network-control signals transmitted by the CPE to the network interface must meet the following requirements:

- The maximum power difference between the high- and low-group components shall not exceed 4 dB
- The power level of the high-group component shall equal or exceed that of the low-group component
- Loop-powered DTMF-signal power levels shall conform to the limits shown in **Fig 5**
- The total power of all extraneous frequencies transmitted by the CPE shall be at least 20 dB lower than the DTMF-signal power.

TABLE 3—DTMF WAVEFORM CHARACTERISTICS

PARAMETER	CANADA	UK	JAPAN
RISE TIME	STARTING FROM −55 dBm, ≤5 mSEC TO 90% OF FINAL VALUE	≤15 mSEC TO LIMITS IN FIGURE	NO SPEC
ON TIME	≥50 mSEC	≥68 mSEC	≥50 mSEC
INTERDIGITAL PAUSE	≥45 mSEC	≥68 mSEC	≥30 mSEC
CYCLE TIME	≥100 mSEC	≥136 mSEC	≥120 mSEC

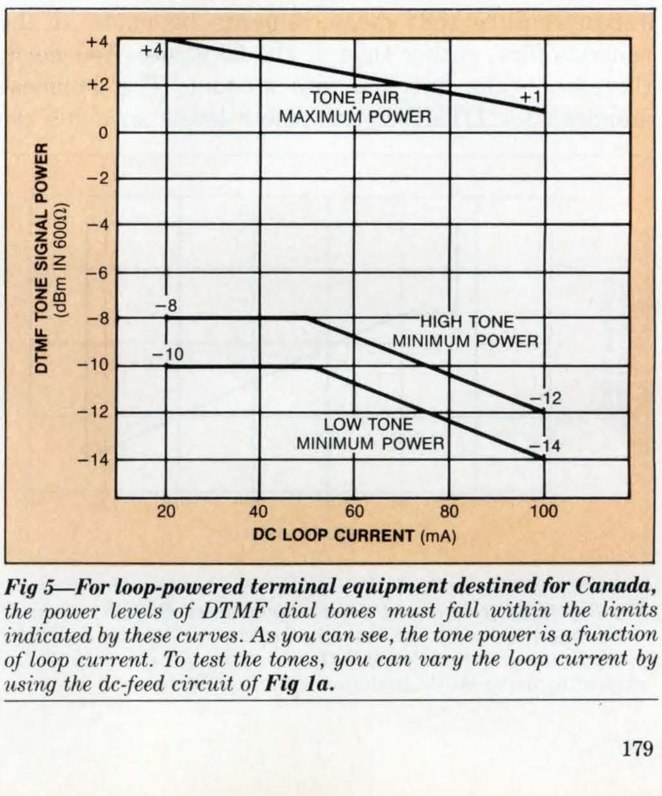


Fig 5—For loop-powered terminal equipment destined for Canada, *the power levels of DTMF dial tones must fall within the limits indicated by these curves. As you can see, the tone power is a function of loop current. To test the tones, you can vary the loop current by using the dc-feed circuit of* ***Fig 1a.***

Virtually all national telecomm standards view tests for hazardous voltages and dangerous leakage paths as of paramount concern.

For fixed-level, locally powered generators, DTMF-signal power levels have the following requirements:

- nominal power per frequency: −6 to −4 dBm
- maximum power per frequency pair: 2 dBm
- minimum power, high group: −10 dBm
- minimum power, low group: −12 dBm.

In Canada, for data equipment designed to have the DTMF level track the data signal level, the power levels of the high- and low-group DTMF signals shall not exceed that of the data by 2 and 0 dB, respectively. Finally, for autodialers, DTMF-tone average power levels shall not exceed 0 dBm, over any 3-sec interval and at any loop current.

Fig 6 gives the power-level limits for individual DTMF tones for CPEs destined for installation in the UK. Additional stipulations accompany these limits:

- The high-group tone amplitude shall be 2±1 dB higher than the low-group tone amplitude
- The transient peak voltage (associated with rise and fall intervals) for a DTMF tone shall not exceed 5V
- During DTMF signaling, the power level for a single unwanted frequency component shall not exceed −33 dBm, and the total power of unwanted frequency components shall be at least 20 dB lower than the lowest power level of any one signaling tone of a digit tone burst.

Unlike those in Canada and the UK, the standards in Japan require that measurements be made at the central office, rather than at the CPE site. You must, therefore, take line loss into account. The Japanese standard for DTMF-signal power levels specifies the low- and high-group limits as a function of the line loss. The low-group minimum and maximum power limits are (−16.5+0.8L) and (−6.5+0.8L) dBm, respectively; L is the line loss in dBm measured at 1500 Hz. The absolute maximum power level for the low group is −3.5 dBm. For the high group, the limits are (−16+L) and (−6.5+L) dBm, not to exceed −2.5 dBm.

Scrutinize signal power

In the three countries under consideration here, no other parameter is so closely regulated as the signal power that the CPE delivers to the telecomm network. Also, no other parameter displays such a disparity in specs. Consider the Canadian standards, for instance. **Fig 7** shows the permissible limits for transmitted signal power. Again, you'll find esoteric nomenclature. The term "metallic" applies to differential signals, and "longitudinal" refers to single-ended, ground-referenced signals.

Fig 7's limit curves reflect power levels measured over a 3-sec interval. The written specs allow short-term power levels beyond the curves' limits. For example, the spec limits metallic voice and data signals to −9 dBm; however, during a 250-msec interval, the power can attain 3 dBm max. The Canadian standards also regulate the maximum dc signals that the CPE may impose on the network. On hook, the metallic and longitudinal dc voltage may not exceed ±25 mV. Off hook, the longitudinal signals may not exceed 0V, nor be more negative than −0.5V. Note that, though **Fig 7** doesn't show it, the frequency range of 3995 to 4005 Hz

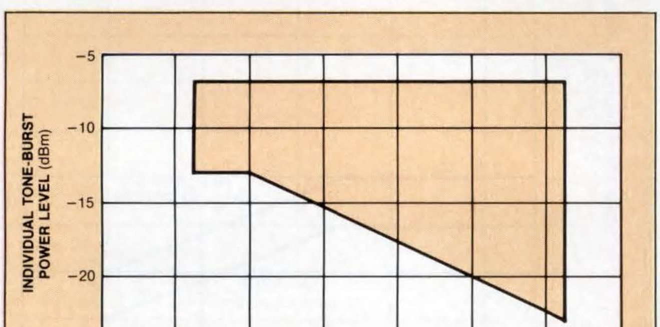


***Fig 6—DTMF tone-burst power must meet British norms** by remaining within this envelope. As they are in Canada, the DTMF power limits are a function of the loop current. You can vary the loop current by using the dc-excitation circuit of **Fig 1b**.*

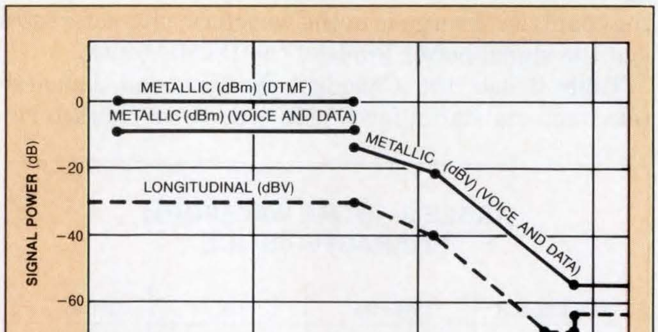


***Fig 7—Signal power is a crucial parameter in Canada.** The curves reflect measurements averaged over a 3-sec interval; shorter bursts (250 msec) have higher limits. "Metallic" signals are differential, tip-to-ring signals; "longitudinal" signals are single-ended signals, measured from tip to ground and ring to ground.*

is restricted: Metallic voice and data levels may not exceed −29 and −20 dBV, respectively. The telecomm system uses this frequency band for network control.

In the UK, signal-power limits are more complex than in Canada (or anywhere else). **Table 4** gives the limits for in-band frequencies. The tabular figures represent instantaneous power measured in a 10-Hz bandwidth. Besides these limits, the British standards mandate a 1-minute mean power level of −9 dBm max for fixed-level CPEs, and −13 dBm max for apparatus having adjustable power levels. For the adjustable CPEs, the installer must set the level at the time of installation, according to procedures prescribed by British telecomm authorities.

You should interpret **Table 4** in the following way: When a signal occurs in area A, it shall be accompanied by a signal or signals in area B, whose power level is not more than 12 dB lower than that of the signal in area A. Similarly, when a signal occurs in area C, it shall be accompanied by a signal or signals in area B, whose power level is not more than 12 dB lower than that of the signal in area C. When no signal exists in area B, the total power in the frequency range of 2220 to 2340 Hz shall not exceed −33 dBm. **Table 5** lists the limits for out-of-band signal power in the UK. These limits reflect 1-minute mean power measured in any 3-kHz bandwidth above 3.4 kHz.

As mentioned, the Japanese telecomm standards take account of transmission-line losses between the CPE and the central exchange, as borne out by the signal-power limits in **Table 6.** As you can see, the specs impose a maximum mean power level of (L−15) dBm, where L is the line loss. Assuming losses between 0 and 7 dB, the CPE should be able to transmit maximum mean power levels between −15 and −7 dBm.

You can consider the lines coming from the telecomm network to your CPE to be long, open-wire transmission lines. To be able to reject noise and hum (principally 50 and 60 Hz) and to minimize coupling to other telephone lines, these lines must remain in balance. Therefore, it's important that your CPE present balanced longitudinal impedances to the network. ANSI/IEEE-455 is the standard test procedure that Canada has adopted for terminal-equipment balance tests. **Fig 8** shows the proposed circuit for performing these tests; the accompanying table gives the Canadian limits for longitudinal-impedance balance. For data-terminal equipment, the minimum balance is 45 dB over the range of 200 to 4000 Hz.

To perform the balance test, you place S_2 in position B

TABLE 4—UK SIGNAL-POWER LIMITS

FREQUENCY (Hz)	POWER LEVEL IN A 10-Hz BANDWIDTH (dBm)	NOTES
0	−33	
100	−33	
100	−23	
200	−23	
200	−6	
450	−6	
575	−43	
775	−43	AREA C
865	−33	
900	−6	
900	−6	
1000	−23	
1000	−45	AREA B
2000	−45	
2000	−23	
2130	−6	
2130	−6	
2220	−33	AREA A
2340	−33	
2430	−6	
3200	−6	
3200	−23	
3400	−23	
3400	−33	

TABLE 5—UK POWER SPECTRAL-DENSITY LIMITS

FREQUENCY (kHz)	POWER SPECTRAL DENSITY (dBm)
3.4	−33
5.1	−40
8.9	−40
50	−70
10,000	−70

TABLE 6—SIGNAL-POWER LIMITS IN JAPAN

PARAMETER	FREQUENCIES	SIGNAL-POWER LIMITS
IN-BAND SIGNALS	4 kHz MAX	L-15 dBm MAX MEAN LEVEL 0 dBm MAX LEVEL
OUT-OF-BAND SIGNALS	4 TO 8 kHz 8 TO 12 kHz >12 kHz	P-20 dB MAX P-40 dB MAX P-60 dB MAX

NOTES:

1. L IS T HE LINE-TRANSMISSION LOSS BETWEEN THE SWITCHING FACILITIES OF A TELECOMMUNICATIONS CARRIER AND THE INTERFACE WITH THE TERMINAL EQUIPMENT, MEASURED AT 1.5 kHz.

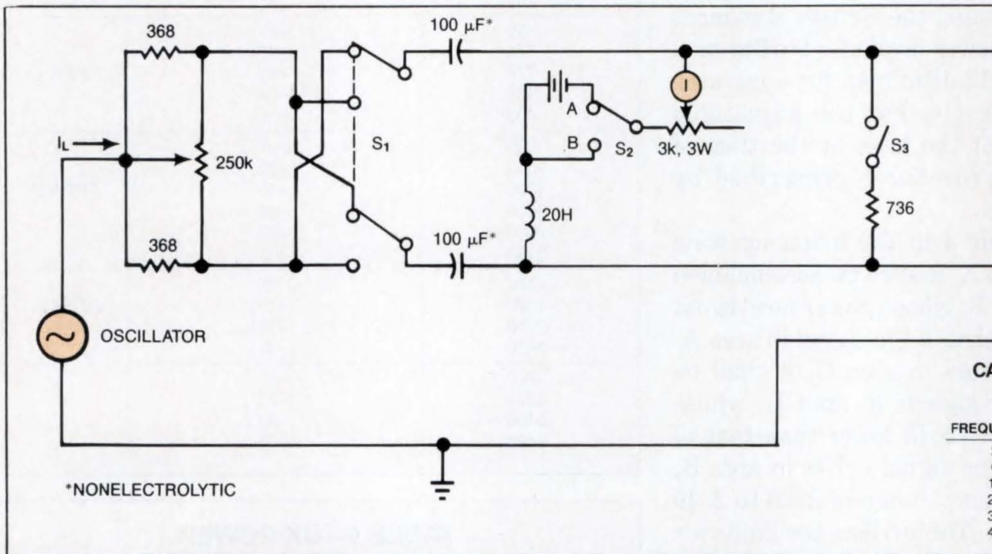
2. THE MEAN LEVEL IS THE AVERAGE SIGNAL POWER MEASURED AT THE TERMINAL EQUIPMENT. THE MAX LEVEL IS THE MAXIMUM PERMISSIBLE POWER LEVEL TO BE SET AT THE TIME OF ADJUSTING THE TERMINAL-EQUIPMENT OUTPUT.

3. P IS THE IN-BAND SIGNAL-POWER LEVEL.

4. THE DENOTED SIGNAL-POWER LEVELS APPLY TO SYSTEMS HAVING 600Ω BALANCED IMPEDANCE.

Thankfully, all three countries use the same DTMF frequencies, but the permissible power levels for the dial tones vary considerably from country to country.

and close S_3 to produce an on-hook condition. You then apply a 10V rms signal and measure the voltage from tip to ring at all the stipulated frequencies. The 250-kΩ potentiometer compensates for any mismatch between the 368Ω resistors; when these impedances are balanced, flipping S_1 shouldn't produce any differences in the tip-to-ring voltages. The balance figure is 20 times the base-10 log of the ratio of the oscillator voltage to the tip-to-ring voltage. You must test the CPE in an off-hook condition, too. For this condition, you open S_3 and adjust the loop current to obtain the lowest balance indication, and then repeat the balance tests.



CANADIAN LONGITUDINAL-IMPEDANCE BALANCE

FREQUENCY (Hz)	MINIMUM BALANCE (dB)
200	66
600	61
1000	57
2000	51
3000	47
4000	45

Fig 8—Balanced impedance to ground is of prime concern in Canada. *Longitudinal-impedance imbalance can cause noise and hum pickup, as well as interference with other phone lines. The table gives the minimum acceptable balance figures for various frequencies; the test circuit shown comes from ANSI/IEEE-455.*

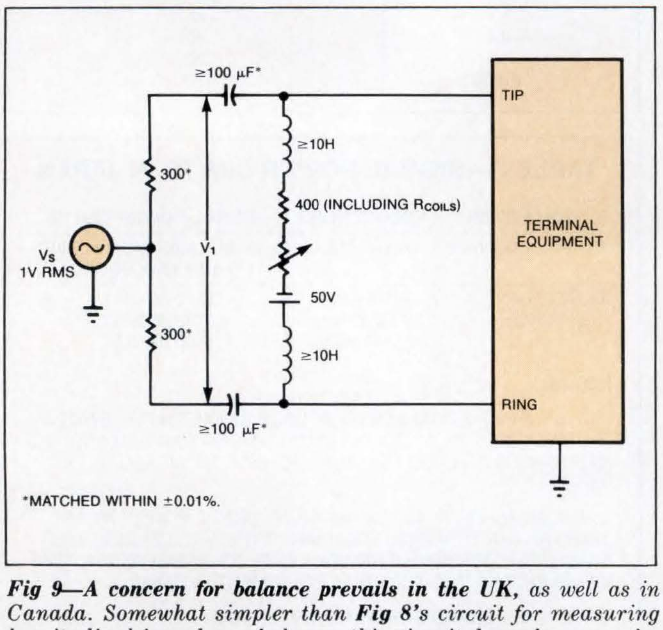


Fig 9—A concern for balance prevails in the UK, *as well as in Canada. Somewhat simpler than **Fig 8's** circuit for measuring longitudinal-impedance balance, this circuit depends on precise matching of components for its accuracy. The principle of operation and the test method are identical to those for Canadian CPEs.*

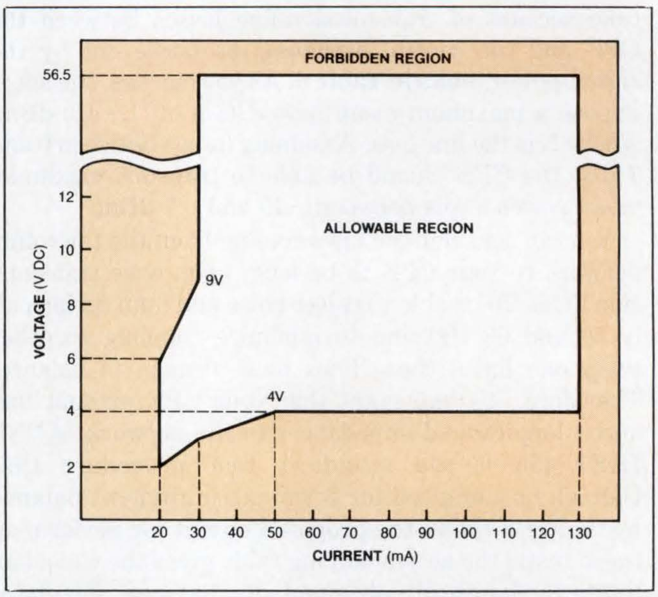


Fig 10—You must pay your phone bills in Canada, *thanks to these off-hook voltage-current limits set by Canadian standards. The CPE's off-hook impedance properties allow the phone company to detect off-hook conditions for billing purposes.*

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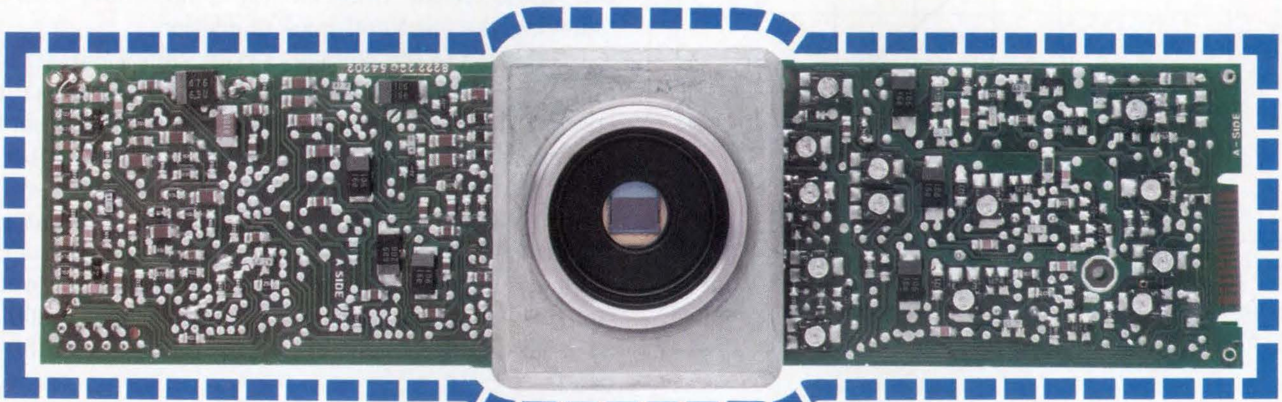

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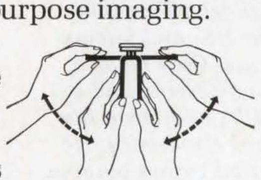

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Signal power is the most closely regulated parameter in all telecomm markets. Specs for the various countries vary widely.

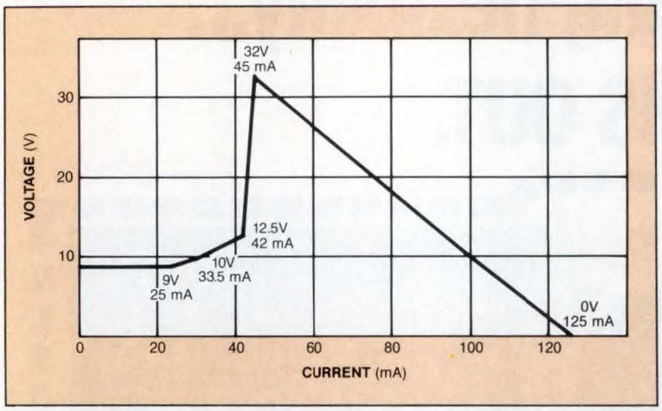

Fig 11—Off-hook impedance is important in the UK, *as is evident from this limit curve. The off-hook voltage-current status of a terminal allows the phone company to ascertain an off-hook condition for billing.*

The circuit prescribed by the UK standards for measuring longitudinal-impedance balance (called "impedance balance about earth" in the UK) is shown in **Fig 9.** The British specs simply stipulate that the balance, calculated in the same way as the Canadian standards, must exceed 46 dB over the range of 300 to 3400 Hz. Curiously, the Japanese telecomm standards do not specify longitudinal-impedance balance.

In order to be able to bill a caller, a telephone company must be able to detect that the caller's CPE is indeed off hook. One way to do this is to assign limits to the CPE's off-hook voltage-current relationship. An example of such a billing-protection spec is the Canadian standard off-hook V-I-limit diagram **(Fig 10).** The tip-to-ring voltage-current characteristic must satisfy the limits in the diagram for a minimum of 5 sec following the on- to off-hook transition.

In addition to the voltage-current limits shown in the diagram, Canada also stipulates that the measured current shall not decrease by more than 25% from the maximum value attained during the 5-sec interval following the transition. This last requirement does not apply if the current is greater than the current that would flow through a 200Ω resistor connected from tip to ring. As in the US, another Canadian billing-protection provision mandates that energy in the 800- to 2450-Hz band exceeds that in the 2450- to 2750-Hz band.

Although not labeled as a billing-protection measure as such, an off-hook V-I limit diagram forms part of the British telecomm standards, too. **Fig 11** shows the upper limits on the tip-to-ring voltage measured for currents ranging from 0 to 125 mA. The Japanese standards have no explicit billing-protection provisions. The only Japanese spec that corresponds to the Canadian and the British standards is the requirement that the CPE exhibit dc off-hook resistance between 50 and 300Ω. **EDN**

If you need standards information

The following companies provide standards information, testing services, and instrumentation necessary for testing telecommunications apparatus to the various national standards discussed in the accompanying article.

Standards information

Compliance Engineering
593 Massachusetts Ave
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1430 Broadway
New York, NY 10011
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Palo Alto, CA 94303
(415) 857-8000

Compliance Design Inc
629 Massachusetts Ave
Boxborough, MA 01719
(617) 264-4668

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1. Dash, Glen, "Understand FCC rules when designing telecomm equipment," *EDN*, May 16, 1985, pg 193.

Author's biography

Glen Dash is the founder of Dash, Straus & Goodhue Inc, a Boxborough, MA-based R&D organization that deals with FCC and VDE consulting and testing and with telephone-interconnect analysis for US- and foreign-standards compliance. Glen holds a BS in Electrical Engineering and an MBA, both from MIT, and has a law degree from Harvard University. He holds four patents and enjoys playing softball in his leisure hours.

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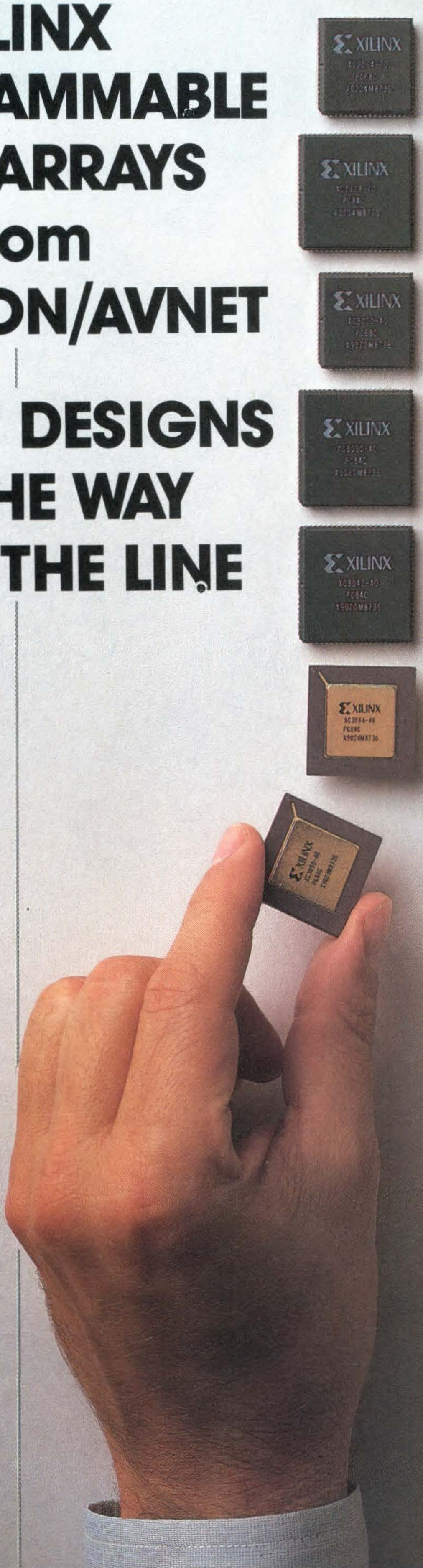

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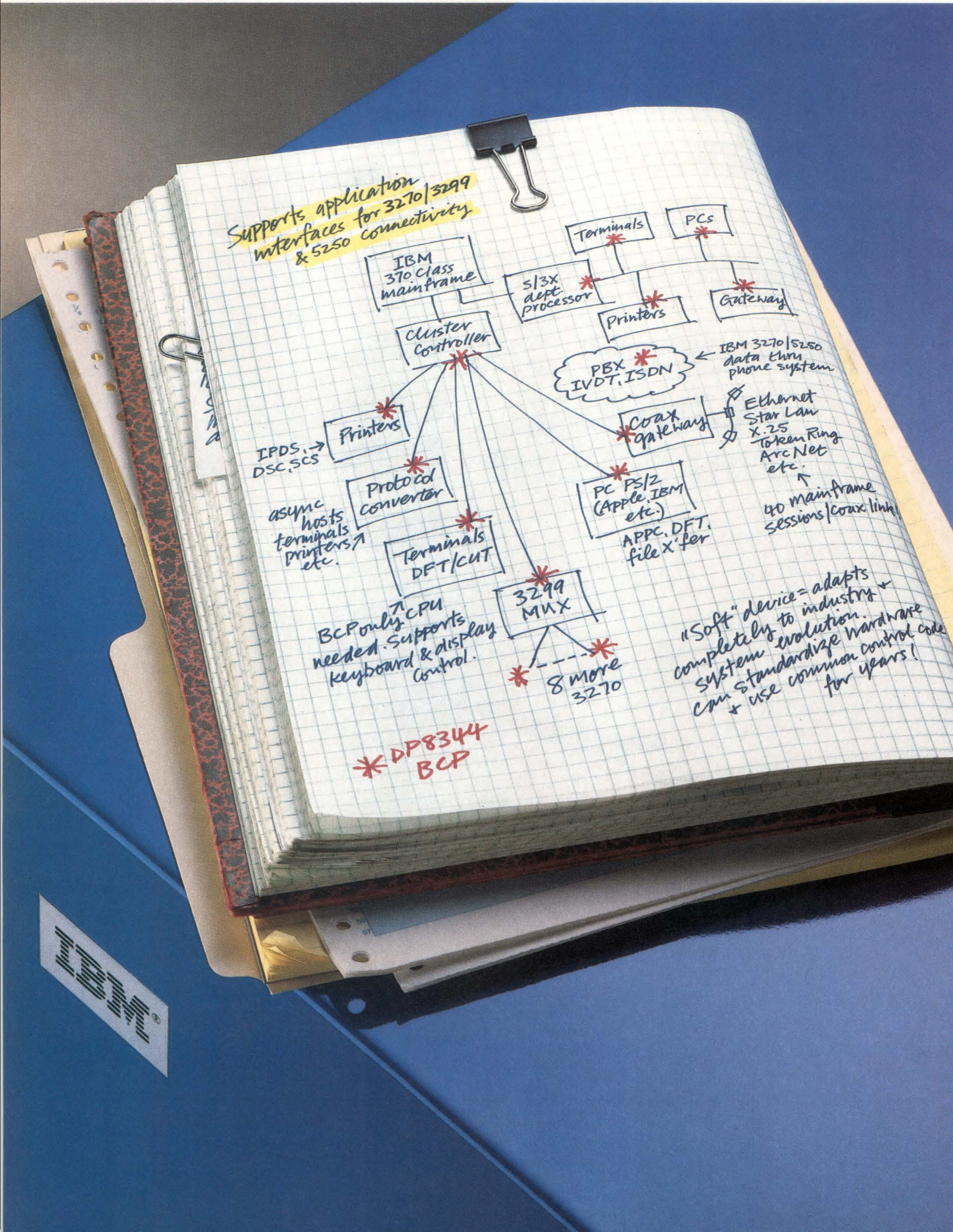

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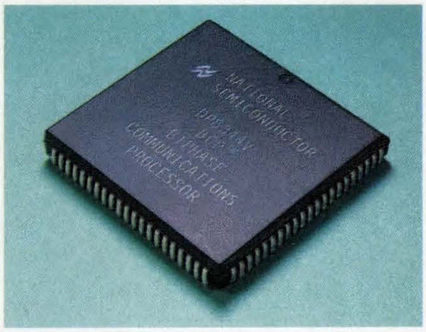

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Soft-start and delay protects power supply

William Andreycak
Unitrode IC Corp, Merrimack, NH

The **Fig 1** circuit governs the manner in which a switch-mode power supply returns to normal operation following a short-circuited output. (If the short remains, successive retrys can produce excessive power dissipation in the supply.)

Delays inherent in a typical switcher's PWM IC, drive circuit, MOSFETs, and current-sense filter contribute to power dissipation by delaying a short-circuit shutdown. Therefore, the small propagation delay of a high-speed PWM chip such as IC_1 helps to reduce the on-time following a short. Without protection circuitry, however, the supply will continue to deliver a finite-width current pulse during each period of IC_1's oscillator signal.

To further reduce power dissipation during retry attempts, you must minimize the pulse widths and pulse rate. You can control the pulse widths by incorporating a soft-start sequence in the control circuit. The soft-start delivers a narrow pulse to the load followed by successively wider pulses until the supply is back in operation or the short triggers another shutdown. You control the pulse rate by adjusting the R_5/C_4 time constant, thereby reducing IC_1's power dissipation as required.

The soft-start alone may produce an unacceptably slow buildup of supply voltage, however. The **Fig 1** circuit therefore introduces a restart delay of several tens or hundreds of milliseconds, which lowers the average rate of retry pulses while allowing supply voltages to rise at the turn-on rate required.

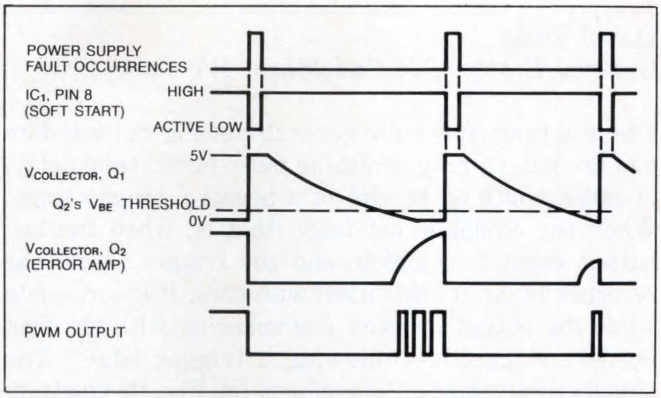

Fig 2—These waveforms show *how the circuit of **Fig 1** responds to repeated fault conditions.*

During normal operation, the pin-8 voltage (IC_2) is high, and both transistors are off. A fault (shorted output) then shuts down the supply and produces a low level at pin 8 (**Fig 2**). Q_1 and Q_2 turn on in quick succession, discharging the restart-delay capacitor C_2 and the soft-start capacitor C_4. When the fault is removed pin 8 returns high and Q_1 turns off, producing the restart delay by allowing a slow recharge of C_4.

The restart delay ends and the soft-start sequence begins when Q_1's collector voltage reaches Q_2's turn-on threshold, about 0.5V. Q_2 turns off, which allows C_4 to charge and unclamp the error amplifier's input voltage (IC_1, pin 2). R_5 and C_4 form the soft-start time constant. The circuit can respond accurately to fault conditions lasting longer than 25 nsec. **EDN**

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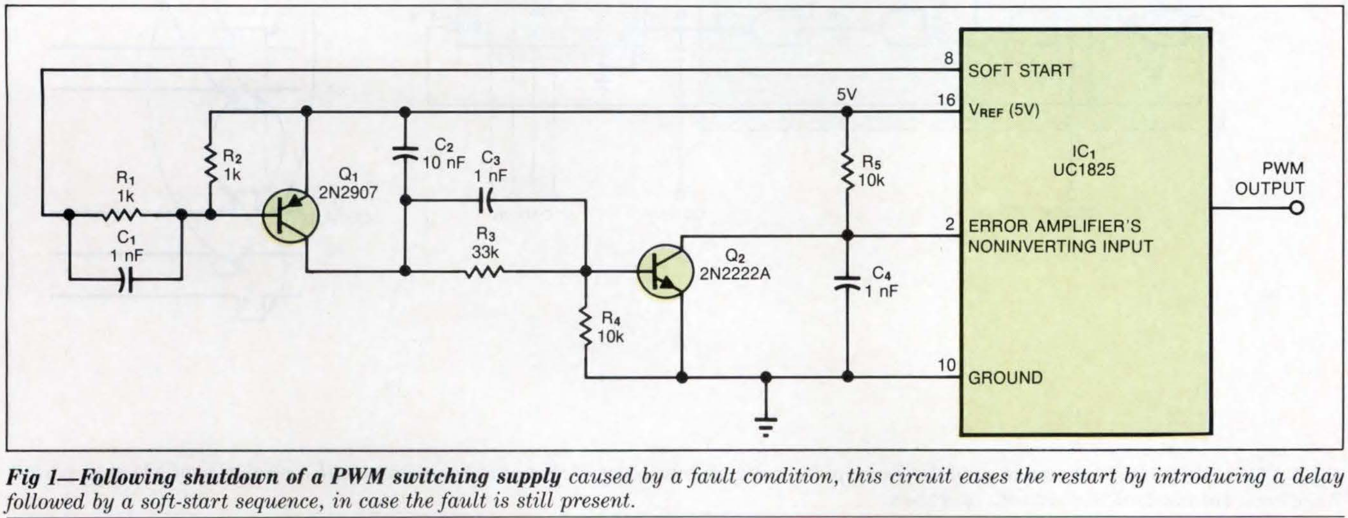


Fig 1—Following shutdown of a PWM switching supply *caused by a fault condition, this circuit eases the restart by introducing a delay followed by a soft-start sequence, in case the fault is still present.*

Pulse-burst generator is programmable

David Tutlo
General Electric, Philadelphia, PA

The programmable pulse generator of **Fig 1a** loads data and produces a programmable pulse burst, time delay, or pulse width on receipt of a negative trigger edge. When the circuit is not busy (that is, when the last output event is complete and the trigger signal has returned high), it loads itself with data. It ignores data while the output is active (commencing with the first positive clock edge following a trigger edge). The alphabetically labeled waveforms in **Fig 1b** illustrate the generator's operation.

By automatically latching the received trigger edges, the circuit accepts asynchronous triggers without producing fractional pulses. The generator also adjusts to the trigger waveform's duty cycle, with the proviso that new digital data enter the counter (IC_2) only when the trigger waveform is high. IC_2 is a 4-bit binary counter; by cascading one or more of these (or the BCD-equivalent 74192 counters) you can implement any desired binary or decade modulo.

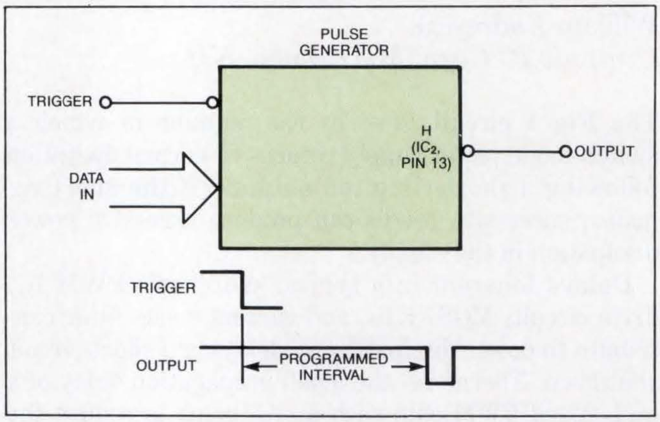


***Fig 2—One application** for the circuit in **Fig 1a** is to generate a programmable time interval, denoted by two negative edges.*

For binary inputs representing the decimal number N, the output exhibits an N-pulse burst (replicating the clock waveform) for each negative trigger edge received. Or, you can use waveform H (IC_2, pin 13) as an output, obtaining a programmed interval of N clock periods denoted by an end-of-cycle pulse **(Fig 2)**. And

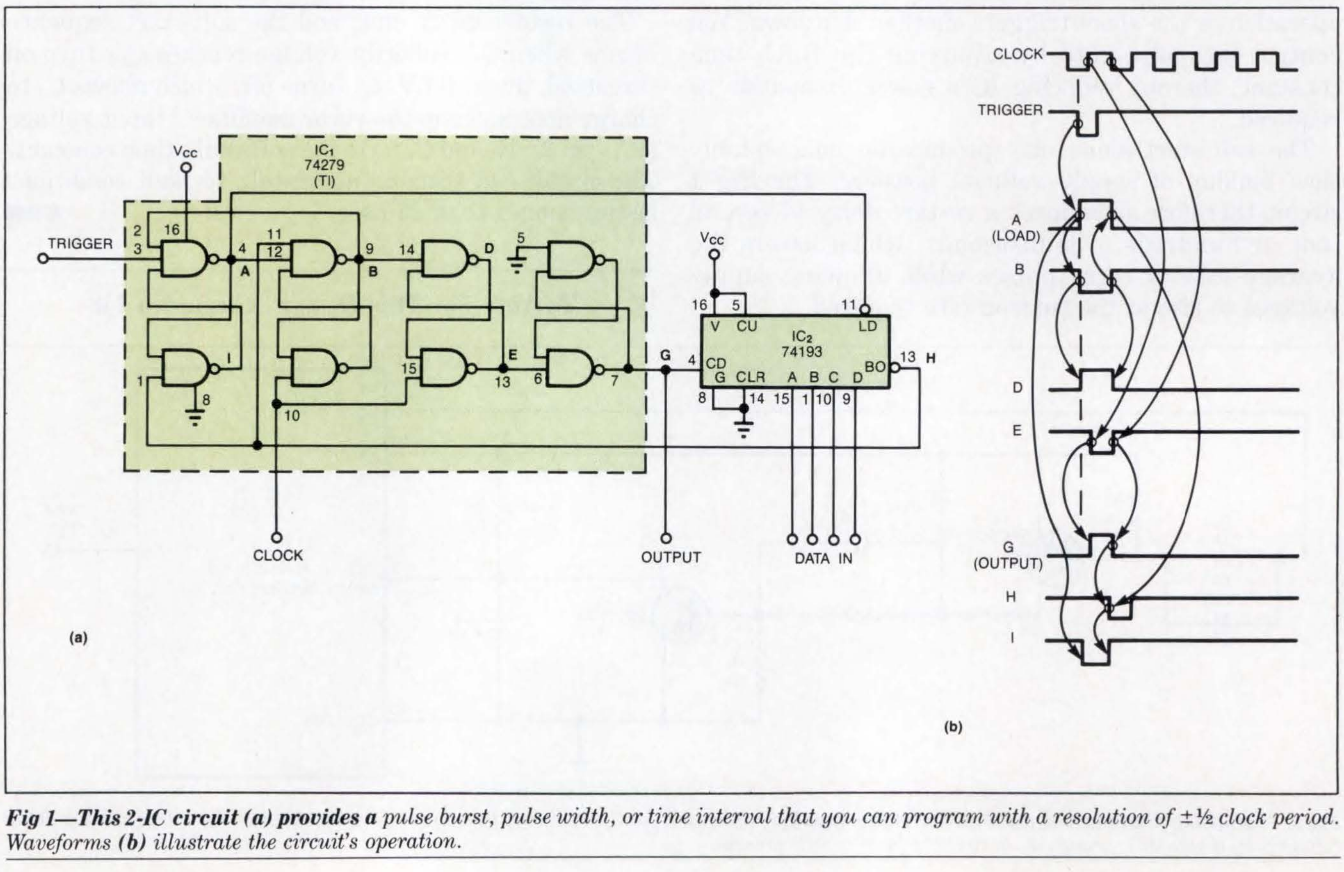
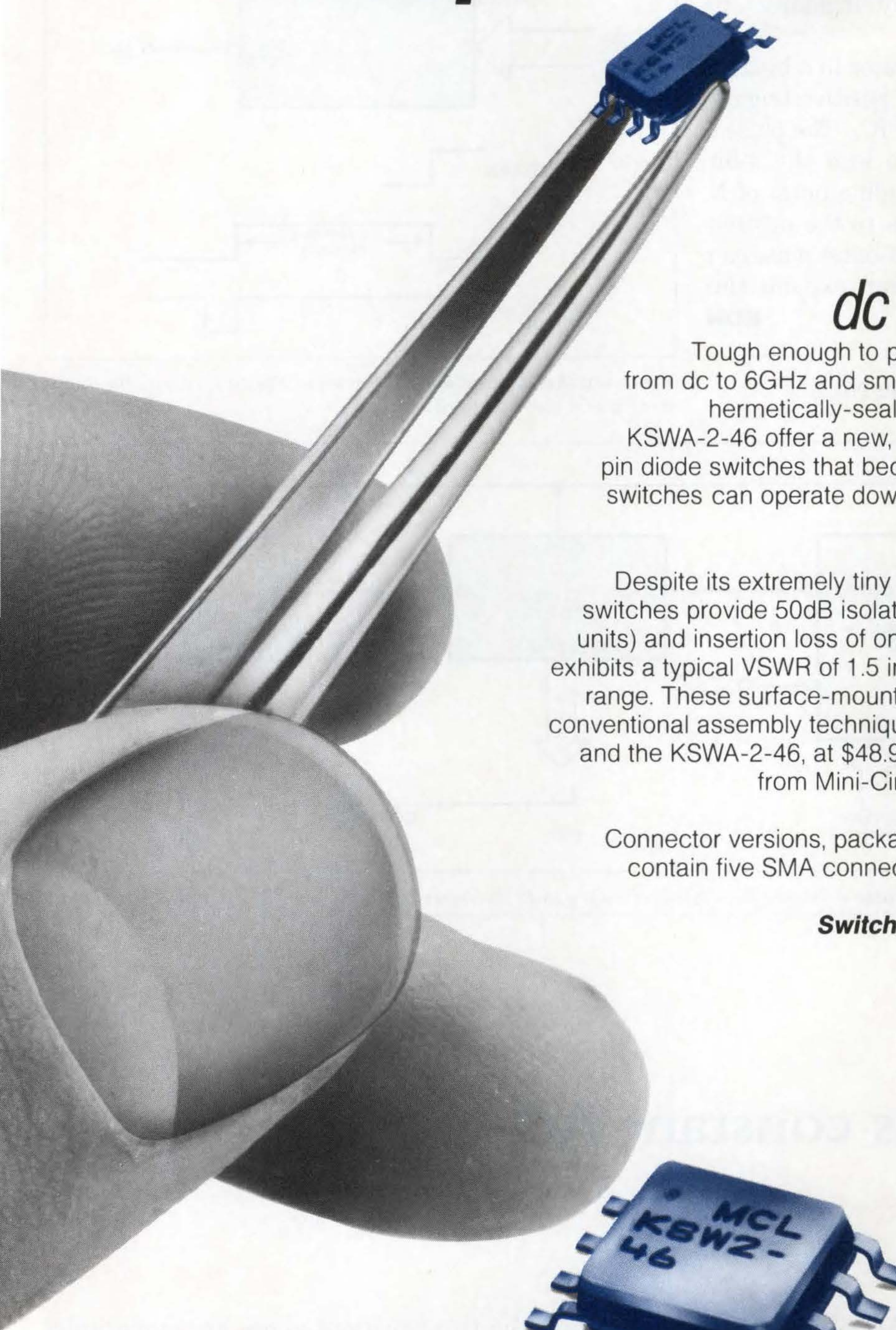


***Fig 1—This 2-IC circuit (a) provides a** pulse burst, pulse width, or time interval that you can program with a resolution of ±½ clock period. Waveforms **(b)** illustrate the circuit's operation.*

tiny SPDT switches

absorptive ... reflective



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SPECIFICATIONS

	KSW-2-46		KSWA-2-46	
	ZFSW-2-46		ZFSWA-2-46	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec)				
rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	−5V on, OV off		−5V on, OV off	
OPER/STOR TEMP.	−55° to +125°C		−55° to +125°C	
PRICE (1-24)	**$32.95**		**$48.95**	
	$72.95		**$88.95**	

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C 117 REV.B

CIRCLE NO 121

by using waveform A (IC_1, pin 4) as the output **(Fig 3)** you get a one-shot multivibrator, whose output is a pulse whose width is programmable. These circuits synchronize the trigger and clock signals by introducing as much as one clock period of delay, in addition to the programmed interval.

Finally, you can use the burst generator in a binary-to-BCD code converter **(Fig 4)**. Each positive trigger pulse clears the BCD counters IC_1 and IC_2. The pulse's trailing edge causes the generator to load the 4-bit binary data and then issue a corresponding burst of N pulses, which increments the counters to the desired BCD code for N. The generator's end-of-burst pulse can flag a host processor. Again, you can expand the counters to handle larger numbers. **EDN**

To Vote For This Design, Circle No 747

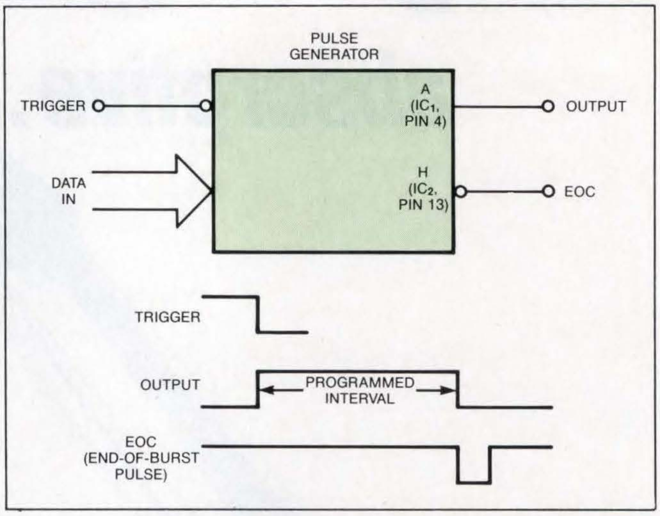

***Fig 3—In this application,** the circuit of **Fig 1a** serves as the digital analog of a one-shot multivibrator.*

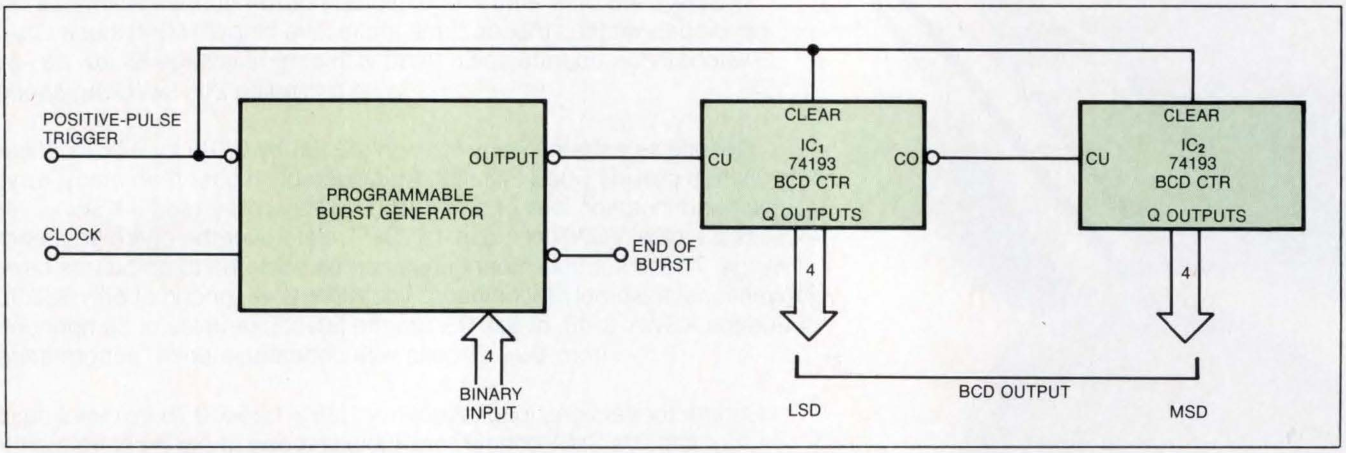

***Fig 4—Connecting the Fig 1 pulse-burst generator** as shown here forms a binary-to-BCD converter.*

Power circuit has constant full scale

James Bryant
Analog Devices, Newbury, UK

An analog computational chip such as AD538 can easily generate the relationship

$$V_{OUT}=V_{IN}^{M}.$$

The full-scale output V_{FS} varies considerably with M, however, for a given range of V_{IN}. You can produce a constant-full-scale output by adding a second IC **(Fig 1)**. This circuit inserts a factor into the above equation:

$$V_{OUT} = V_{FS}^{(1-M)}V_{IN}^{M}.$$

Note that the two equations above are numerically accurate but dimensionally incorrect. You must first normalize a voltage to a dimensionless quantity before raising it to a power—like this, for example:

$$V_{OUT} = \left(\frac{V_{IN}}{2V}\right)^{M} (2V).$$

(The circuit, in fact, does perform this normalization.)

Each IC has the transfer function $V_{OUT}=Y(Z/X)^M$, where X, Y, and Z are inputs (pins 15, 10, and 2). IC_2 applies $V_{FS}(2V/V_{FS})^M$ to the Y input (pin 10) of IC_1, which completes the desired expression by adding the factor $(V_{IN}/2V)^M$. Potentiometer R_3 lets you set V_{FS} in the range 2 to 10V. (You can obtain $V_{FS}=10V$ by simply opening the connection to pin 5; R_3 and R_4 are unnecessary in that case.)

The ganged potentiometers R_{5A} and R_{5B} let you set the power M. The maximum value for M depends on the common value chosen for R_3 and R_4:

$$M_{MAX} = \frac{R_3 + 200}{R_3}.$$

M_{MIN} depends on M_{MAX} and the common value of the R_5 potentiometer sections:

$$M_{MIN} = \frac{100M_{MAX}}{R_5 + 100}.$$

For a given circuit, you get the maximum M value by turning R_5 to zero resistance. You get the minimum M ($M_{MAX}\div21$) by turning R_5 to its maximum value of 2 kΩ. The accuracy of your chosen V_{FS} value depends on the matching between R_5 sections A and B. For many applications, 1%-tolerance sections are satisfactory. The circuit can handle signal frequencies as high as several tens of kilohertz, provided that V_{IN} remains positive. **EDN**

To Vote For This Design, Circle No 746

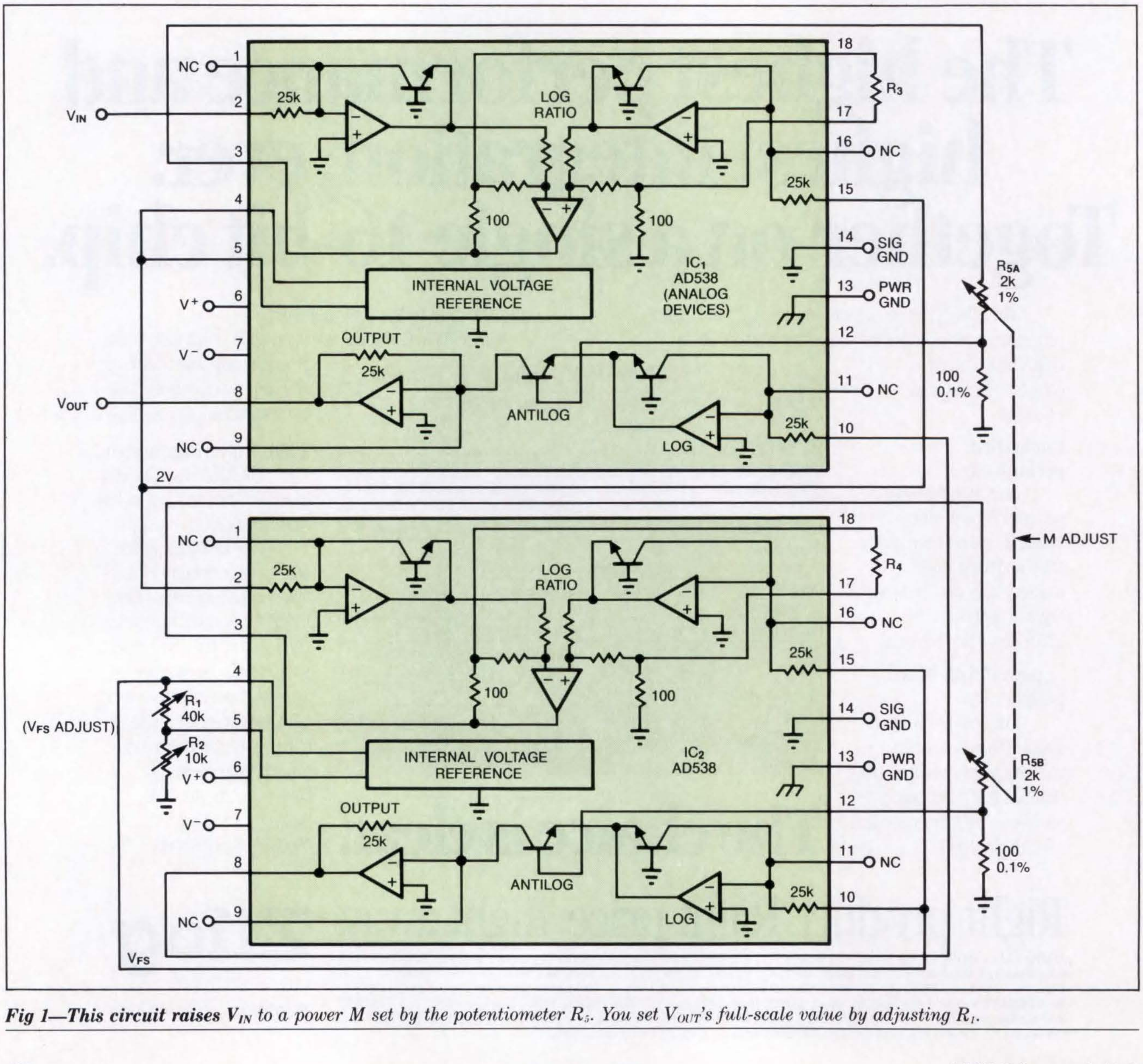

Fig 1—This circuit raises V_{IN} to a power M set by the potentiometer R_5. You set V_{OUT}'s full-scale value by adjusting R_1.

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CIRCLE NO 138

Switched signal powers analog switch

Jack Armijos
Siliconix Inc, Santa Clara, CA

The analog switch IC_1 in **Fig 1** can derive power from its input signal during power outages, provided the input signal amplitude exceeds 4V and its frequency exceeds 1 kHz. For normal operation, the supply voltage (V^+) is 12V, and you apply 5V at V_L for TTL compatibility. With these voltages present, a logic low at IN_2 closes the switch and produces a 45Ω on-resistance.

If V_L and V^+ are lost, the switch becomes a guest of the signal source and draws power from it. Typical CMOS switches can be destroyed under these conditions, but blocking diodes D_1 and D_2 prevent the chip from drawing excessive current from the source.

A positive input pulse turns on the clamping diode D_3 and charges C_1. Charge on C_1 powers the chip; operation is satisfactory because the chip requires less than 1 μA of supply current. Loading of the signal source is imperceptible **(Fig 2).** Switch resistance is a respectable 100Ω for this mode of operation.

Pullup resistor R_2 restores the output level for TTL data. If TTL control is lost, the pulldown resistor R_3 ensures that the switch will remain closed. IC_1 contains two normally closed switches and two normally open switches, so you can also configure a switch that opens when the control is lost. Either circuit requires inverted logic and handles data rates from 1 kHz to 1 MHz. **EDN**

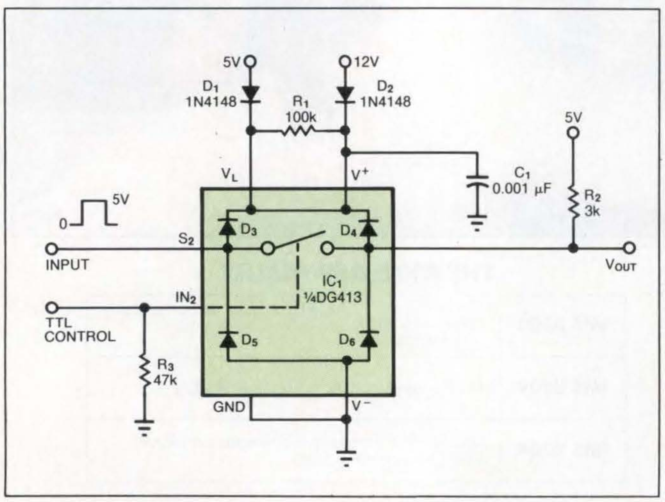

Fig 1—If this analog-switch circuit loses V_L and V^+ voltage, it will draw power from the signal source instead.

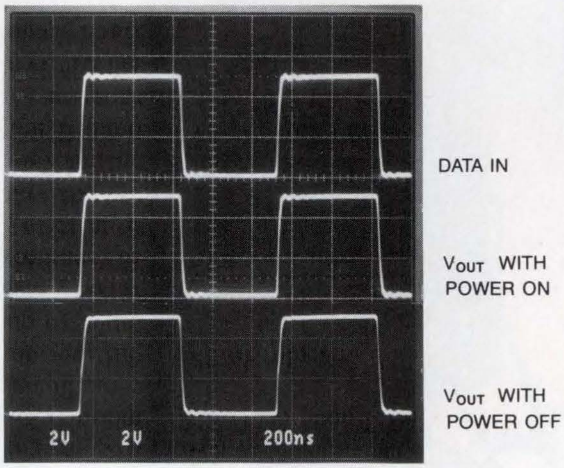

Fig 2—These waveforms show that the Fig 1 circuit passes TTL waveforms even when the power is removed. The data input must have at least a 4V amplitude and a 1-kHz repetition rate.

To Vote For This Design, Circle No 749

Zero-current sensor protects relay contacts

B Erik Valeur
Electronic Instrument & Specialty Corp, Stoneham, MA

The **Fig 1** circuit extends the life of a reed relay by allowing the relay's contacts to open only at moments of zero current. (Destructive arcing can cause rapid contact wear if the contacts open repeatedly while conducting current.) Unlike zero-crossing circuits that predict the zero-current moment, this circuit senses that condition and responds immediately, using a fast relay (K_1, 100 μsec).

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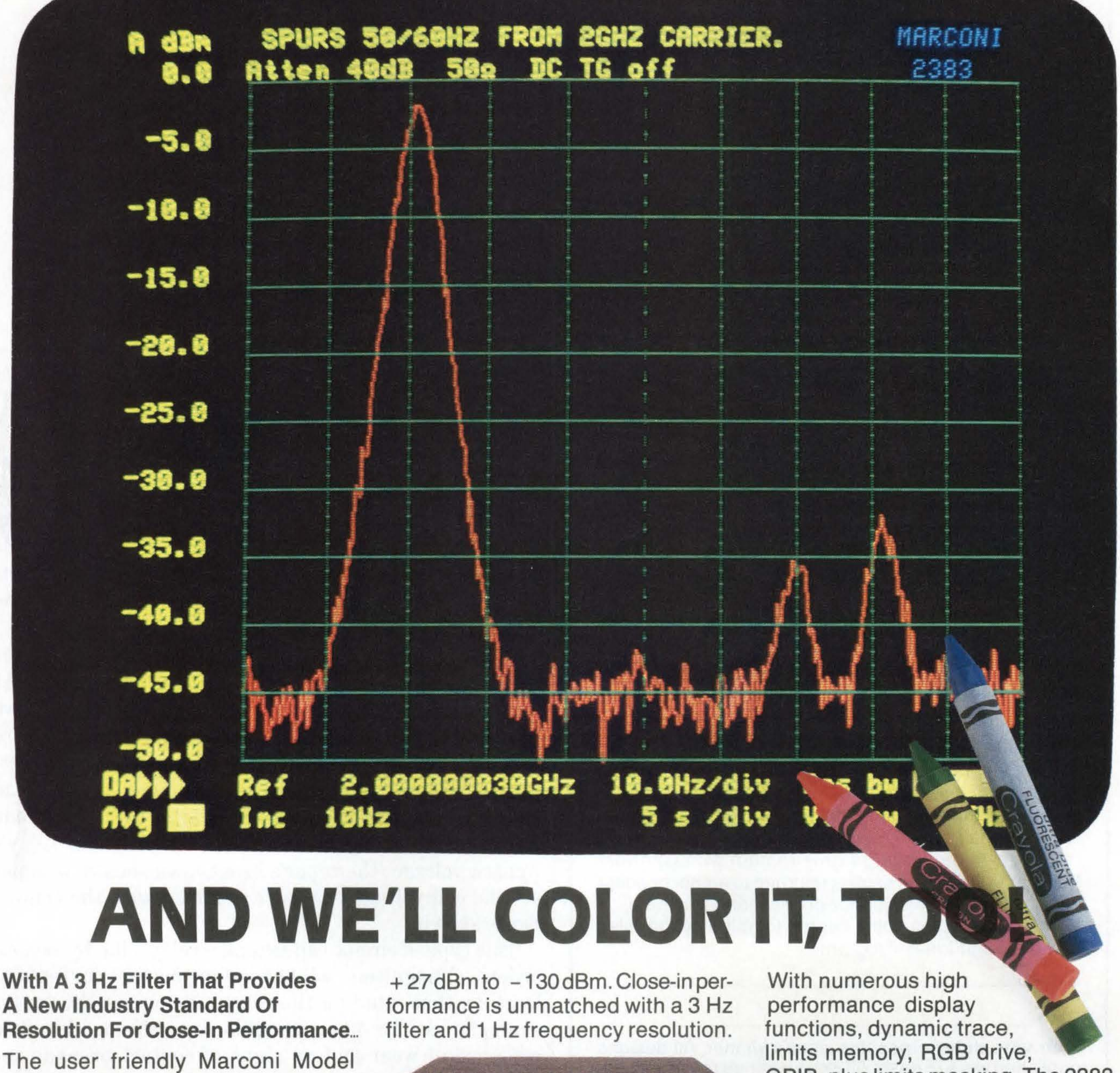

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CIRCLE NO 59

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ISSUE WINNER

The winning Design Idea for the October 29, 1987, issue is entitled "Debouncer for spdt switches uses few parts," submitted by Mounir Boukadoum of the University of Quebec at Montreal (Quebec, Canada).

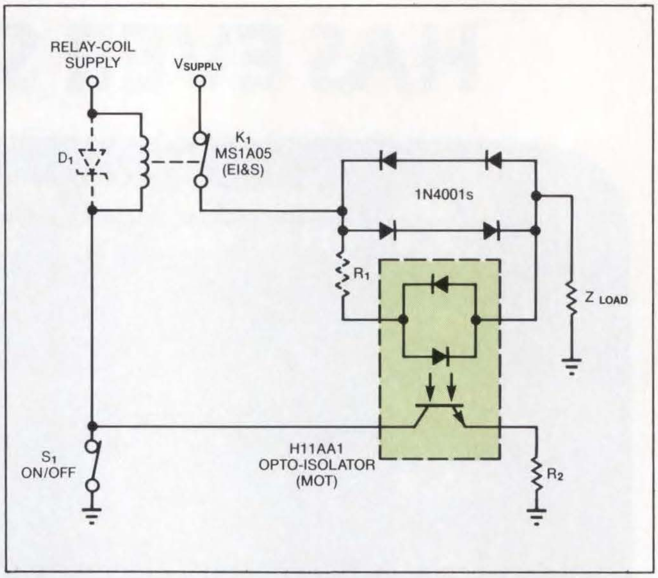

***Fig 1—You control this power circuit** by operating the S_1 switch; the diodes and the optoisolator prevent a response in the relay except when the relay contacts' current is near zero.*

The on/off switch S_1 controls the application of V_{SUPPLY} to the load by controlling K_1. Load current biases one of the diode pairs on, which in turn activates one of two LEDs in the optocoupler. This action turns on the phototransistor, ensuring that the relay remains closed while load current is flowing regardless of the state of S_1.

Conventional 60-Hz ac current, however, goes through zero twice per cycle, about every 8 msec. At that time the phototransistor turns off, and (if you have opened S_1) K_1 opens, at or near the moment of zero current. Resistor R_1 limits the LED current if necessary. (No limit is required in this circuit, which can handle one or two amperes.) Similarly, the zener diode D_1 protects the opto device by clamping the relay's flyback voltage (the zener's breakdown should be about 4× the coil voltage). D_1 isn't required with the components shown.

This type of circuit can extend a relay's life by several orders of magnitude while handling contact currents at least 2× that rated for the relay. The circuit shown, for example, ran for 40 or 50 million operations with little evidence of wear and no signs of contact breakdown.

EDN

To Vote For This Design, Circle No 750

Hitachi's 3-Chip Graphics System

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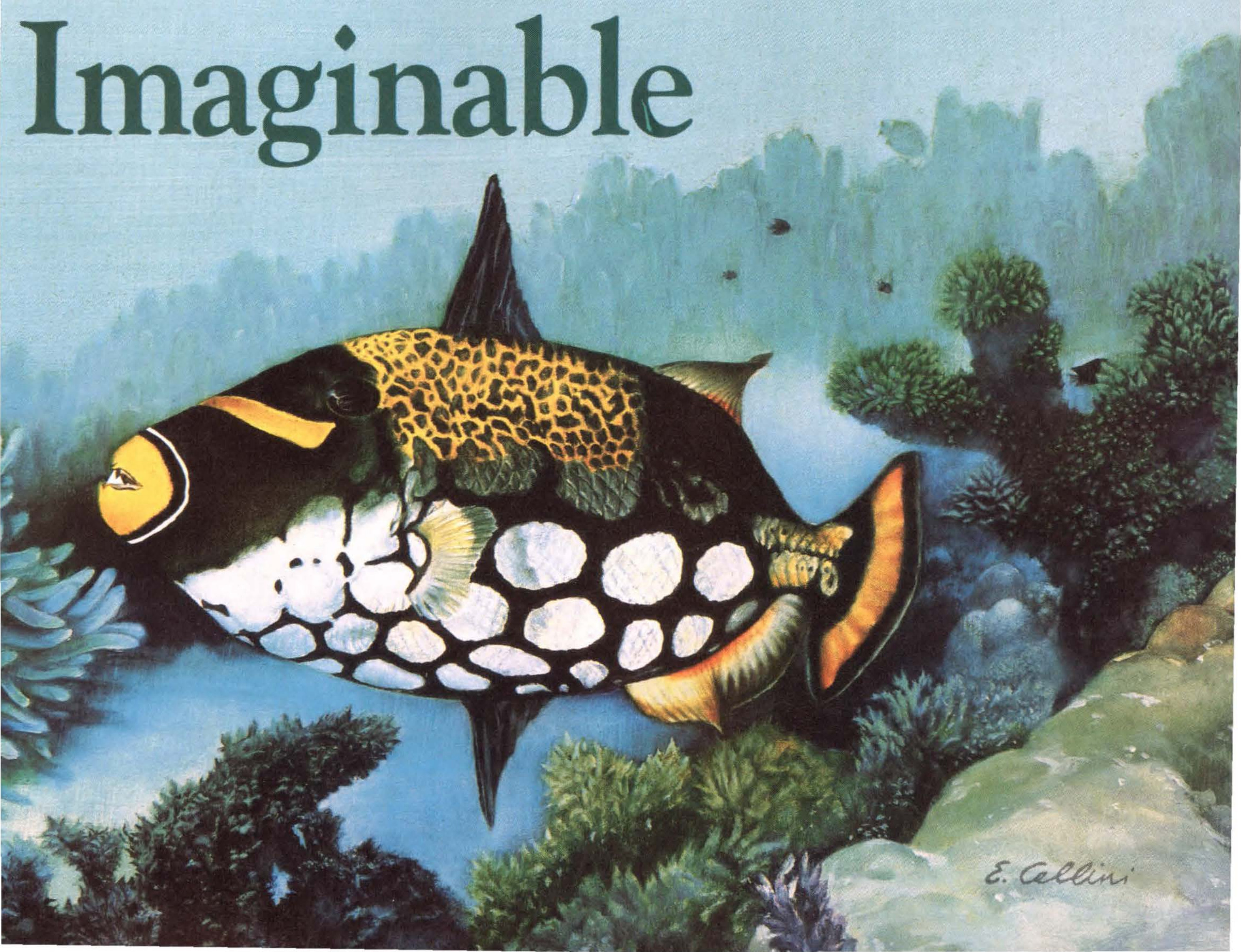
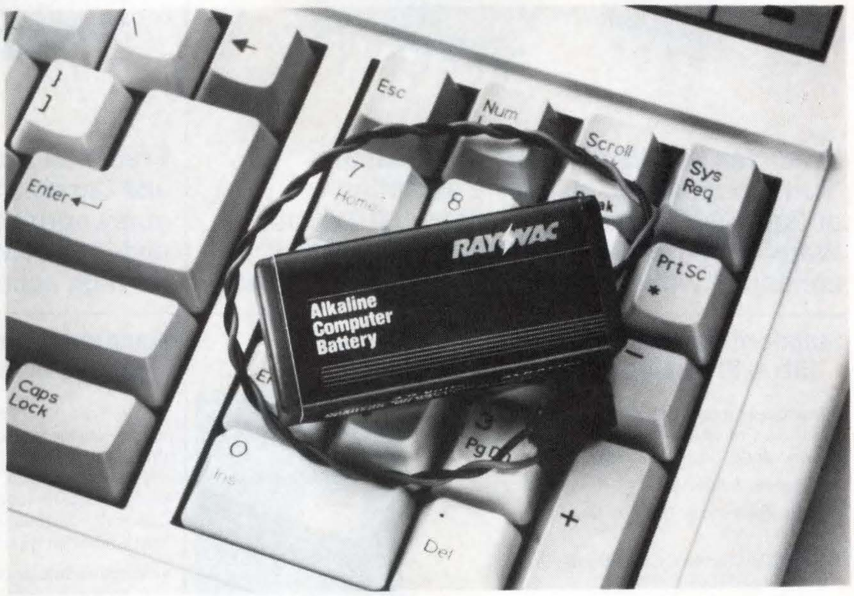


COMPONENTS & POWER SUPPLIES

CLOCK BATTERIES

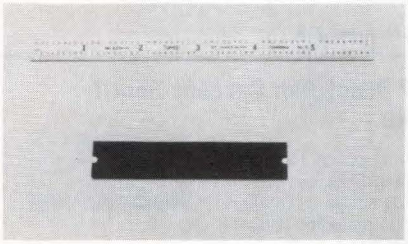
- *Maintain power to clock chip when computer is turned off*
- *2- to 4-year lifetime*



The Model 843 and 844 batteries utilize a 4.5V, 1-Ahr alkaline system and replace the lithium battery that comes with all IBM PC/AT computers. These clock batteries maintain power to the clock chip when the computer is turned off. The batteries also maintain the memory of the chip to prevent loss of the computer's system-configuration information. The 844 features a 4-pin termination that lets it directly replace the original lithium battery in most 80286- and 80386-based systems. The 843 comes in a 3-pin configuration. Unlike the 6.0V OEM lithium batteries, the 843 and 844 employ no internal voltage-dropping resistors. Thus, they have a lifetime spec of two to four years. $11.

Rayovac Corp, 601 Rayovac Dr, Madison, WI 53711. Phone (608) 275-3340. TLX 190428.

Circle No 351



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- *Temperature-independent operation*

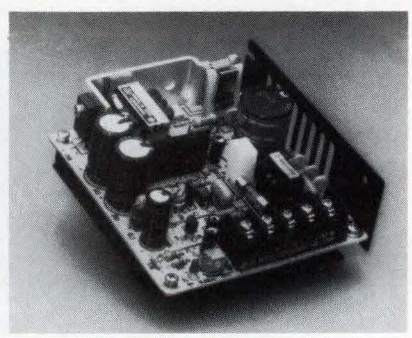
Essentially a metabolic rate indicator for inanimate systems, the Model MS-175 thermoelectric sensor is a flat-plate transducer that measures heat losses from any solid surface. When mounted on a motor housing, it can intercept a small fraction of the heat flow and thereby generate an electrical signal that's proportional to the local heat flux. Under normal load conditions, the transducer can deliver a steady-state signal that's independent of either the ambient or the operating temperature. High steady-state signals indicate inefficiency or incipient failure. You can read out sensor output signals on any millivolt recorder, potentiometer, or data logger. $125.

ITI Co, Box 309, Del Mar, CA 92014. Phone (619) 755-4436.

Circle No 352

POWER SUPPLIES

- *Have wide-range input capability*
- *Feature 300,000-hour MTBF*



PY Series single-output, open-frame switching power supplies feature a 300,000-hour MTBF rating. The supplies have an 85 to 132V ac input range and are available with 5, 12, 15, and 24V outputs. The family includes models with power outputs of 15 to 50W. Each model features inrush current limiting and overvoltage protection. All but the 15W models come with overcurrent protection as a standard feature. Each supply has a 70% min efficiency rating, a 16-μsec min holdup time, and ±3% regulation. The supplies' internal noise filters meet FCC B-Class requirements, and they provide full-load ratings at temperatures as high as 50°C. $28 to $46 (100). Delivery, four to six weeks ARO.

Shindengen America, 2649 Townsgate Rd, #200, Westlake Village, CA 91361. Phone (805) 373-1130.

Circle No 353

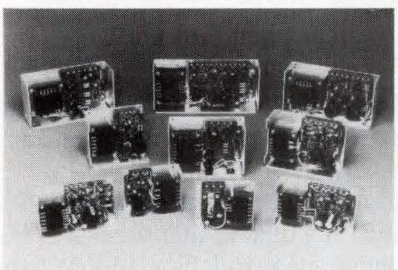
COUPLER

- *Requires no external power*
- *Converts current to isolated output voltage*

The TLP590/591 photovoltaic coupler converts the current output from a TTL device to electrically isolated output voltage. It converts electrical signals to light by using a GaAs infrared LED. A series-connected photodiode array receives this light and generates a photovoltage. Because the driving circuit is completely isolated from the control-signal circuits, you can use this photovoltage to drive power MOSFETs. The photovoltaic coupler provides enough voltage for direct MOSFET gate drive and thus requires no external power supply. $2 (1000). Delivery, 12 weeks ARO.

Toshiba America Inc, Semiconductor Products Div, 2692 Dow Ave, Tustin, CA 92680. Phone (714) 832-6300.

Circle No 354



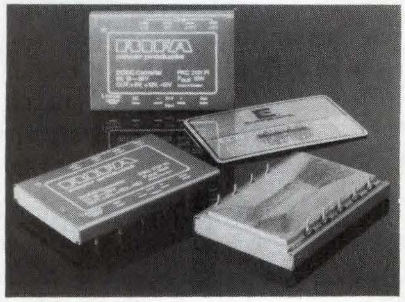
POWER SUPPLIES

- *±0.05% line regulation*
- *120,000- to 460,000-hour MTBF*

The Olympian Series linear power supplies feature calculated MTBF ratings of 120,000 to 460,000 hours. These international units are rated from 6 to 115W and conform to UL, IEC, CSA, and VDE requirements. With jumpers, they can accommodate ac inputs ranging from 100 to 240V. Standard features include line regulation of ±0.05% for a 10% line change, load regulation of ±0.05% for a 50% load change, short-circuit and overload protection, and remote sensing. $29.50 to $108 (25).

Tamura Corp of America, 1150 Dominguez St, Carson, CA 90746. Phone (213) 638-1790. TLX 664759.

Circle No 355



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- *Have 0.33-in. mounting height*

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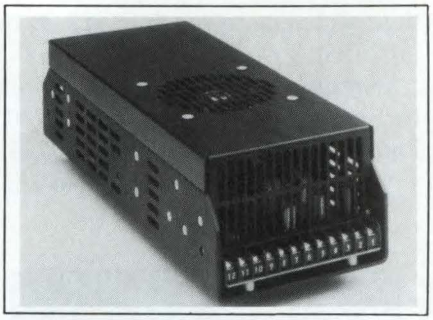
Rifa AB, Power Products Div, 16381 Stockholm, Sweden. Phone (8) 757-5000. TLX 10948.

Circle No 356

Rifa Inc, Greenwich Office Park 3, Greenwich, CT 06836. Phone (203) 625-7300.

Circle No 357



POWER SUPPLY

- *Designed to power disk drives*
- *Rated for 400W*

The QX-11 switching power supply is meant for applications that include several 500M-byte disk drives. The fan-cooled power supply is housed in a 5×3.4×13.5-in. chassis and provides three fully regulated outputs. The supply is rated at 400W and sustains 575W peak for 10 sec. The supply features a 0 to 50°C ambient-temperature operating range; an input surge-current limit; brownout protection; jumpers for 115/230V ac operation; and complete overload, overvoltage, and reverse-voltage protection. The supply has a typical efficiency of 75% and a holdup time of 20 msec. You can obtain remote on/off control and thermal shutdown as options. $349 (100).

Cherokee International Inc, 2841 Dow Ave, Tustin, CA 92680. Phone (714) 544-6665. TWX 510-101-0493.

Circle No 358

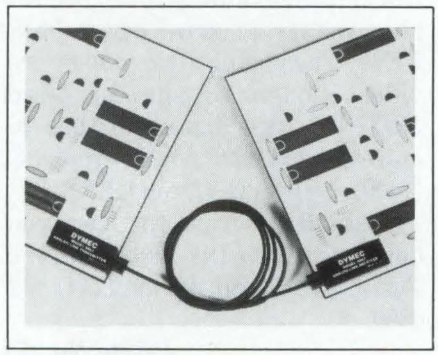
DIODE RECTIFIERS

- *Feature high efficiency*
- *Deliver 44A outputs*

The 40CPQ050 and 40CPQ060 dual-die, center-tapped, Schottky-diode rectifiers have repetitive peak reverse-voltage ratings of 50 and 60V, respectively. Housed in TO-3P packages, the devices handle 44A and are highly efficient—their forward drop/junction measures only 0.63V at 25°C. The units come configured with two anode input pins and have one cathode center-tapped output pin integrated with the base plate. Each device has a nonrepetitive surge-current rating of 525A, a peak reverse-current rating of 25A (at T_J=25°C), a junction-to-case thermal resistance of 0.6°C/W, and an operating junction-temperature range of −40 to +125°C. 40CPQ050, $6.41 (100); 40CPQ060, $6.58. Delivery, eight weeks ARO.

International Rectifier Corp, 233 Kansas St, El Segundo, CA 90245. Phone (213) 607-8837.

Circle No 359



DATA LINKS

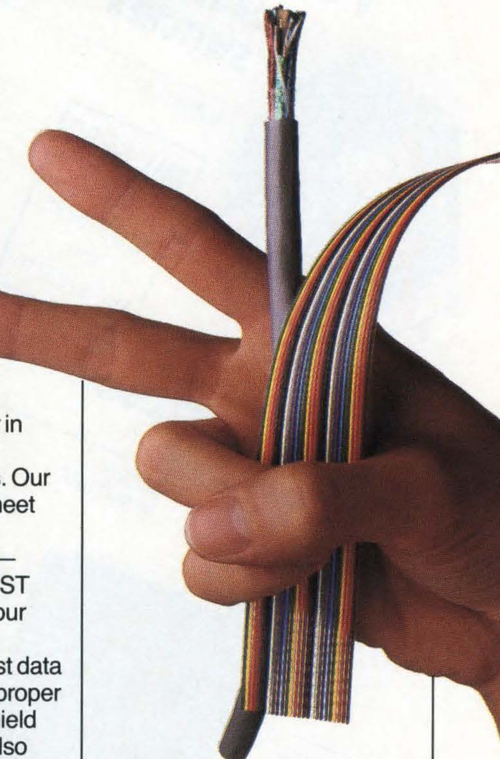
- *Feature pin-selectable inputs and outputs*
- *Single-supply operation*

The Series 5660 analog fiber-optic data links consist of a transmitter, a receiver, and a 50m cable. The transmitter and receiver are housed in 24-pin dual-in-line packages. Pertinent specs include a 10-kHz bandwidth, ± 0.025% FS linearity, an 80-dB signal-to-noise ratio, and a 100-ppm/°C temperature coefficient. Transmitter and receiver full-scale input and output voltages are pin-selectable for 0 to 1, 0 to 2, ±5, and ±1V. The transmitter and receiver modules operate from a single supply of 11.5 to 20V. The receiver includes a 3-pole, active lowpass filter, which you can bypass to suit your application. $200. Delivery, six to eight weeks ARO.

Dymec Inc, 8 Lowell Ave, Winchester, MA 01890. Phone (800) 225-1151; in MA, (617) 729-7870. TWX 710-348-6596.

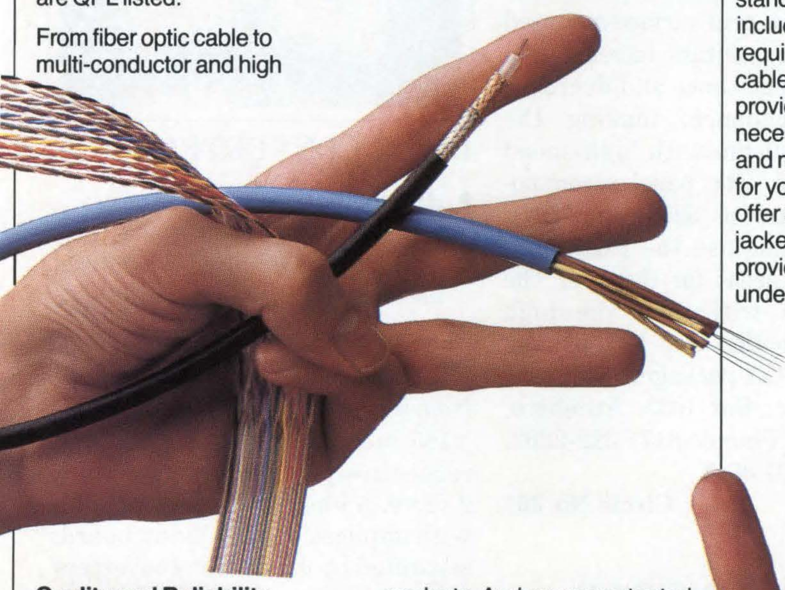
Circle No 360

4 REASONS TO SPECIFY BELDEN FOR YOUR GOVERNMENT AND MILITARY APPLICATIONS



Selection. We offer a broad line of electronic wire and cable designed to meet military specifications such as MIL C 17, MIL C 49055, MIL W 16878, MIL W 22759 and others. Many are QPL listed.

From fiber optic cable to multi-conductor and high temperature cables, choose the cable best suited to your specific application. Or work with our Product Engineering Group to design specialty cable to your exact requirements.



Quality and Reliability. After working with governmental and military applications for over 30 years, we understand the interrelationship of quality components and critical requirements. We believe quality is the responsibility of leadership. That's why our Quality Assurance Department has full authority to maintain high quality standards for our products. And we use patented testing methods to guarantee our product reliability. Choosing Belden means choosing high quality, reliable products.

Belden Innovation. We're a leading innovator in shielding technology and patented testing methods. Our shielding is designed to meet the highest performance standards in the industry—including military TEMPEST requirements. To make your cable decision easier, we provide you with all the test data necessary to choose the proper and most cost-efficient shield for your application. We also offer a variety of insulations and jacketing materials designed to provide superior performance under hostile environmental conditions. Critical application requirements are not a problem when you work with Belden.

The Belden Government Department. Since we understand how the government and prime contractors work, we provide you with full support services—from sales and engineering support to contract administration. We're ready to help with your design decisions where and when you need us.

To make your design project easier, call us for technical assistance. Because when you specify Belden, *There is no equal.*

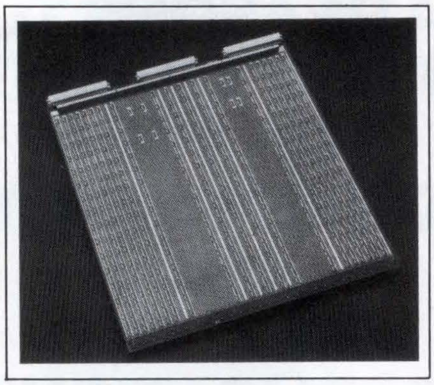
Contact the Belden Wire and Cable Government Department today. P.O. Box 1980, Richmond, IN 47375.

Phone: 1-800-BELDEN-4
(In Indiana, call 317/983-5200)

There is no equal.™

CIRCLE NO 46 **SEE OUR CATALOG IN EEM**

COOPER INDUSTRIES **BELDEN**



PROTOTYPE PANEL

- *Features 4-layer construction*
- *Includes area for PGA devices*

The 8136-VME940-03D is a 9U×400-mm wire-wrappable panel for use in VME Bus applications. It features 4-layer construction—two full ground planes and two full V_{CC} planes—that maximizes power distribution. Integral surface-mounted decoupling capacitors increase distributed capacitance and decrease overall impedance, making the panel compatible with high-speed logic devices. The panel accommodates as many as 595 16-pin DIPs when you also use the PGA (pin-grid array) areas for the ICs. The PGA areas withstand the high power dissipation that is typical of devices in PGA packages. $1583.

Augat Inc, Box 1037, Attleboro, MA 02703. Phone (617) 222-2202. TWX 710-391-0644.

Circle No 361

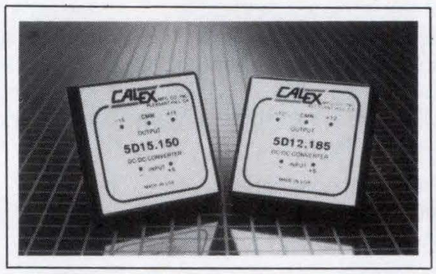
VF DISPLAY MODULE

- *For harsh environments*
- *Features single-supply operation*

The 31098-99 is a shock-mounted, ruggedized 6-line×40-character vacuum fluorescent (VF) display module for use in applications that require high tolerance to shock and vibration. The display operates over a −40 to +85°C temperature range and features 5.05-mm-high, 5×7-dot-matrix, blue-green characters. The module operates from a 5V supply. Its internal μP controls all display functions and easily interfaces to an 8-bit parallel TTL-compatible ASCII data bus. The module displays the complete 96-character ASCII font set, as well as ECMA (European Computer Manufacturers Association) characters and scientific symbols. It can also display user-defined fonts, which you can download with software. $4256 (10). Delivery, six to eight weeks ARO.

IEE Inc, Industrial Products Div, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311, ext. 418. TLX 4720556.

Circle No 362



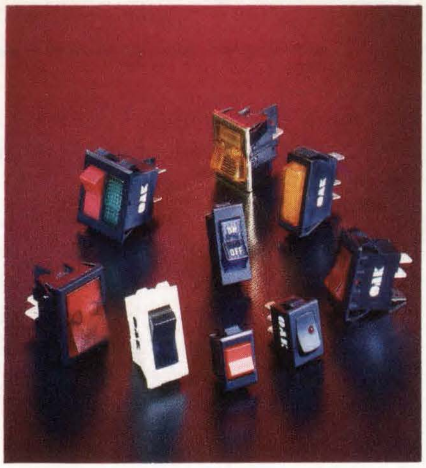
DC/DC CONVERTERS

- *Are compatible with 0.5-in. board-spacing applications*
- *Feature 0.02% line and load regulation*

The 4.5W Model 5D12.185 and Model 5D15.150 converters operate from 5V inputs and deliver ±12V at ±185 mA and ±15V at ±150 mA, respectively. Measuring only 2×2×0.375-in., they are compatible with applications involving boards separated by 0.5 in. The converters' key specifications include 0.02% line and load regulation; 10-mV p-p output noise; 0.3%/1000-hour long-term output stability; 500V dc isolation; 60% min efficiency; and 8-hour min short-circuit protection. The converters also furnish a 6-side shielded case and an LC filter that minimizes the amount of current noise that feeds back into the power bus. Their operating range spans −25 to +80°C. $105.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911. TLX 269888.

Circle No 363



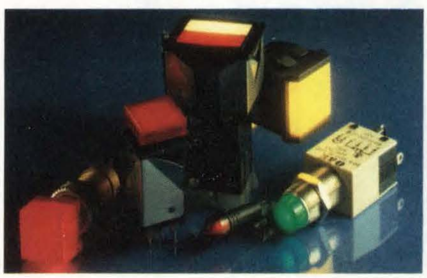
Off-The-Shelf Rocker Switches To Fit Your Design Parameters

Oak rocker switches are available in an assortment of designs, colors, sizes and styles to retrofit most existing design parameters. These attractive and highly-reliable switches are available in single or double pole, lighted, non-lighted or LED varieties. Choose from 6 standard colors and 9 profiles. Quick Connect terminations are standard, with other terminations available.

Oak rocker switches' off-the-shelf capability ensures prompt delivery. UL and CSA approved. Most have VDE, BEAB and SECV approval.

Contact: Oak Switch Systems Inc.
P.O. Box 517
Crystal Lake, IL 60014
Phone: 815/459-5000

Circle 110 for Literature   Circle 149 for Sales Call



Lighted Pushbutton Switches Meet Military, Commercial Specifications

Oak's Optolite lighted pushbutton switches and indicators are available in a wide variety of sizes to meet most design requirements. They feature nine custom colors, eleven pushbutton styles, custom legends including dual lamp/split legends, and choice of mounting options.

A wide range of electrical ratings (dry circuit to 15 amps) and contact configurations are available in both alternate and momentary operation with up to 10 million duty cycles. The switches are UL, CSA listed and many are available with international approvals.

Contact: Oak Switch Systems Inc.
P.O. Box 517
Crystal Lake, IL 60014
Phone: 815/459-5000

Circle 111 for Literature   Circle 150 for Sales Call

Standard and Custom Solenoids For Almost All Circuit Designs

Oak Switch System's extensive line of rotary and linear solenoids include box frame, tubular, flat pack, and rotary selector. All are engineered and manufactured to meet stringent quality standards.

Oak has standard solenoids for virtually any force/stroke requirement. Oak engineers will also custom design rotary or linear solenoids to meet client specifications.

Contact: Oak Switch Systems Inc.
P.O. Box 517
Crystal Lake, IL 60014
Phone: 815/459-5000

Circle 113 for Literature   Circle 152 for Sales Call

What you can't see is the experience.

Go ahead, look closely. Oak Micromotion membrane switch panels invite your rigorous inspection. From every angle, the quality is apparent. Colors are crisp, clean, and to your specifications. Graphics are exact. Options such as texture, LED's and tactile feel are just as you require.

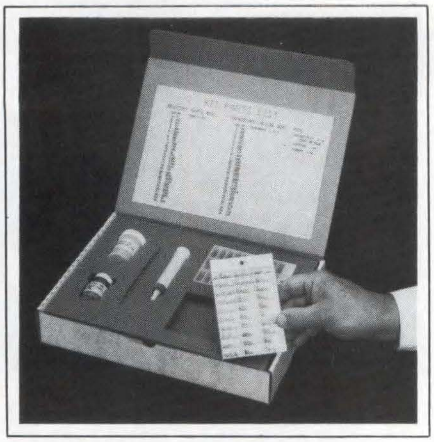
And while you can feel the quality, you can't see Oak's more than 50 years of switch manufacturing experience. But you can sense it from the moment you call. You immediately know you're talking with professionals, people who know the demands of industrial and commercial environments.

Take a good look at Oak Micromotion membrane switch panels. You'll see high reliability, unlimited graphic design options, competitive prices and fast delivery. You might not see the experience, but the quality tells you it's there.

OAK Switch Systems Inc.
P.O. Box 517
Crystal Lake, IL
Phone: 815/459-5000

OAK *Your Partner in Excellence*

Circle 114 for Literature   Circle 153 for Sales Call



RC NETWORK KIT

- *For prototyping surface-mount designs*
- *Includes assembly procedures*

The 9000 kit is for assembling prototype resistor-capacitor circuits that employ surface-mount components. Each kit contains metallized ceramic substrates as well as instructions and examples of typical circuits. Five substrates are provided for each of three circuit patterns to allow maximum flexibility in possible circuit configurations. Surface-mount components come assembled on a 10-pin SIP (single-in-line package) substrate to minimize the size of the finished device. The instructions include a discussion of surface-mount assembly procedures. $395.

Debtek Inc, 503E Vandell Way, Campbell, CA 95008. Phone (408) 866-7286.

Circle No 364

OPTOCOUPLERS

- *Accept ac or dc inputs*
- *Feature 1000V/µsec min CMR*

HCPL-576X Series 8-pin, hermetically sealed optocouplers accept either ac or dc inputs, which lets them serve in either voltage- or current-sensing applications. Typical applications include monitoring a limit- or proximity-switch, a relay-contact, or a power-supply protection circuit. HCPL-5760, the standard product, is a single-channel, ac/dc-to-logic interface optocoupler; HCPL-5761 is the version tested to MIL-STD-883 Class B requirements for use in military and high-reliability systems. Each unit has a guaranteed operating range of −55 to +125°C. Their CMR equals 1000V/µsec min at a withstand-test voltage of 500V. HCPL-5760, $61.90; HCPL-5761, $109.85.

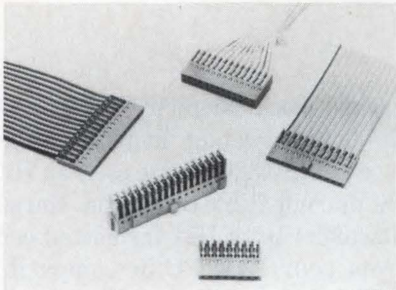
Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Call local office.

Circle No 365

SOCKET SYSTEM

- *Handles 1 to 3A current levels*
- *Available with tin-lead or gold-plated contacts*

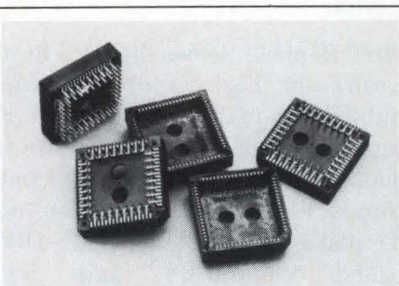
The CHG wire-mount socket system is designed for signal-transmis-



sion and logic-power applications requiring current ratings between 1 and 3A. Two contact options accommodate 22/24 or 26/28 AWG discrete-wire or prenotched ribbon cable on a 0.1-in. grid spacing. You can select 1- and 2-row sockets containing from 2 to 40 or 4 to 80 contacts without polarization or with center-bump polarization. The 2-row military and DIN versions contain from 10 to 80 contacts and are available with or without the center bump. The contact plating includes a choice of 0.1-μin. tin-lead (entire contact) or 10 or 30 μin. of gold over 50 μin. of nickel. $0.96 (1000) for a 1-row, 10-position socket with 30 μin. of gold plating and no center bump.

3M, Dept EP7-99, Box 2963, Austin, TX 78769. Phone (512) 834-1800.

Circle No 366



SOCKET

- *Has perforated construction that simplifies board cleaning*
- *Features insulator with 94V-0 UL rating*

The PLCC-068 socket accepts 68-pin plastic leaded chip carrier (PLCC) devices. The socket is JEDEC-qualified for type-A carriers and it has an 8×8-position contact array that places contacts on 0.050-in. centers. Its glass-filled polyphenylene sulfide insulator has a 94V-0 UL rating, and its preloaded, stamped-and-formed, copper-alloy contacts have a tin-lead plating. The socket features a compact low-profile design and perforated construction to ease board cleaning. The socket's design lets you probe the chip-carrier pins in the circuit. The socket operates over a temperature range that spans −65 to +125°C. $3 (100). Delivery, stock to eight weeks ARO.

Precicontact Inc, Box 798, Langhorne, PA 19047. Phone (215) 757-1202.

Circle No 367

COMPUTERS & PERIPHERALS

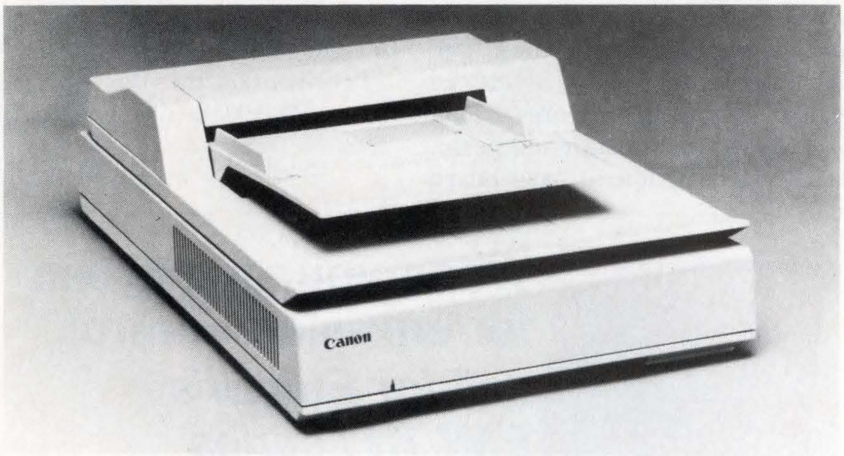


IMAGE SCANNER

- *Provides 300-dot/in. image scanning*
- *Scans at 16-sec/page rate*

The desktop IX-12F image scanner can scan documents for text, graphs, drawings, maps, and pictures and can enter them into a computer. It can scan images at a speed of 16 sec/page and can provide a resolution of 300 dots/in. It offers 32 levels of halftones, a useful feature for photo reproduction. The scanner has a CCD sensor and a halogen light source. An optional automatic document feeder can handle as many as 20 letter- or legal-size sheets of paper. The unit measures 14½×21½×3½ in. You can use an interface board to connect it to one of the vendor's personal computers or to an IBM PC, PC/AT, or compatible computer. Scanner, $1495; document feeder, $595.

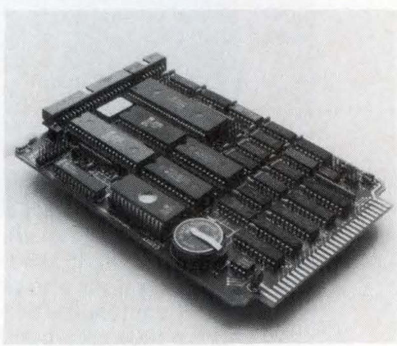
Canon USA Inc, System Div, 1 Canon Plaza, Lake Success, NY 11042. Phone (212) 688-1200.

Circle No 368

STD BUS BOARD

- *Uses a 4.6-MHz 64180 μC*
- *Features an 8-channel A/D converter for data acquisition*

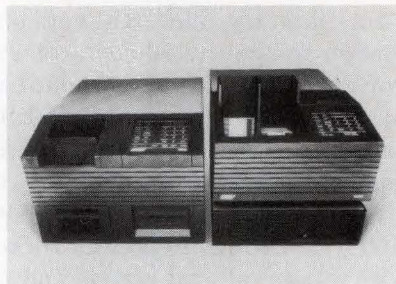
The Model 8020 all-CMOS CPU board for the STD Bus uses a 64180 4.6-MHz μcontroller chip. The board features three memory sockets, two of which have 32k bytes of battery-backed RAM. The remaining socket contains Debug software. You can also use this socket to hold a 27C256 EPROM (CMOS) or, if all-CMOS operation isn't required, a 27512 EPROM. The board's 64180 μC has two RS-232C ports with programmable baud rates. The board also has a synchronous, half-duplex serial I/O channel and a Z80



PIO IC that provides two 8-bit channels. An 8-channel, 8-bit A/D converter furnishes data acquisition through 0 to 5V inputs. Other features of the board include two 16-bit and four 8-bit cascadable counter timers, one watchdog timer, two DMA channels, and a battery-backed clock calendar. You can use the board's Debug firmware to link it to an RS-232C device or to an IBM PC or compatible computer. You can download Intel Hex-formatted code from your IBM PC or compatible and execute it in RAM with a breakpoint. The board's power requirements are 5V at 90 mA, 12V at 1 mA, and −12V at 4 mA. $395; with A/D converter, $445.

CμBit, 190 S Whisman Rd, Mountain View, CA 94041. Phone (415) 962-8237. TLX 797377.

Circle No 369



DISK COPIERS

- *Make duplicate floppy disks from hard disks or floppy disks*
- *Provide as many as 300 copies/hour*

MST Replica! Series diskette duplicators let high-volume software publishers make as many as 300 copies/hour of 3½-, 5¼-, and 8-in. double-sided media at each of their copy stations. The copiers can handle disks compatible with MS-DOS-based computers and with Commodore Amiga, Apple Macintosh, Atari, DEC, and Wang computers. A user-programmable batch mode permits the automatic duplication of several masters from either a hard- or floppy-disk original. The units can operate unattended after their initial setup. They can record serial numbers. You can order copiers whose options let you copy between various 5¼- and 3½-in. floppy

disks or allow you to use an IBM PC, PC/XT, or compatible to copy disks intended for the IBM PC/AT and PS/2 or Apple II. From $5500.

Media System Technology Inc, 16812 Hale Ave, Irvine, CA 92714. Phone (800) 443-8515; in CA, (714) 863-1201. TLX 4992344.

Circle No 370

PRINTER ADAPTER

- *Lets IBM PCs or compatibles drive high-speed laser printers*
- *Provides access to laser-printer formatting features*

The USA/PC enables IBM PCs or compatibles and IBM PS/2 computers to drive high-speed laser printers and Xerox ion-deposition printers. It drives high-speed laser printers by Datagraphics, Hewlett-Packard, IBM, Kodak, NCR, Siemens, and Storage Technology. Computers such as the PS/2 Model 80 and the Compaq 386, which employ 80386 μPs, or machines such as the PS/2 models 30 and 60, which employ the 80286 μPs, can drive the Xerox 8700 and 9700 and the IBM 3800 at full speed. IBM PCs or compatibles and the PS/2 models 25 and 30 can drive the Xerox 4050 and 4060 ion-deposition printers, which feature maximum operating speeds of 50 and 60 pages/minute respectively. The unit also grants access to such printer features as an unlimited selection of type fonts, type sizes ranging from four to 24 points, variable-line and -character spacing, variable-page width, and the capacity to print on both sides of a sheet of paper. $9000.

Spur Products Corp, 13469 Beach Ave, Marina Del Rey, CA 90292. Phone (213) 822-7100.

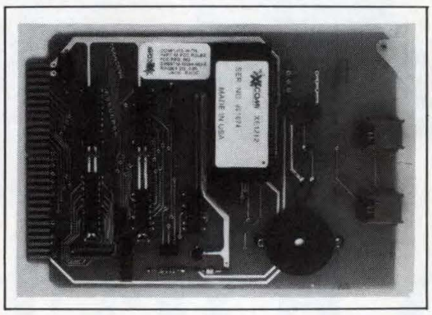
Circle No 371

SMART MODEM

- *Hayes AT-compatible 212A/103 modem*
- *Autoanswer and autodialing for DTMF and pulse*

The MCM-MODEM is a self-contained Bell 212A/102 and CCITT V.22 and V.21 compatible modem on an STD Bus card. It supports the full Hayes AT command set with additional features: autoanswer and autodialing for both DTMF and pulse dialing, and call-progress monitoring. The modem has an

COMPUTERS & PERIPHERALS



FCC-registered data-access arrangement (DAA) for connection to the telephone line and a 8250B UART-type interface to the STD bus. It's configured for 8- and 10-bit addressing and requires a total of eight consecutive I/O addresses. The board generates an interrupt whenever the following prioritized levels are active: received data available, transmitter holding register empty, receiver-line status, and modem status. The card is I/O mapped and processor independent —it can work with the 80186, 8088, 68008, HD64180, Z80, or 8085A. It comes with an audible telephone-line monitor and an auxiliary RJ-11 jack for a separate telephone handset. The unit requires 5V at 250 mA and −12V at 40 mA; it operates over 0 to 65°C. $395.

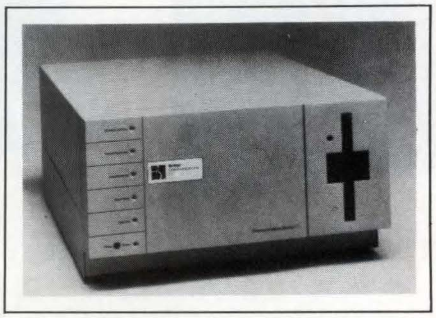
WinSystems Inc, Box 121361, Arlington, TX 76012. Phone (817) 274-7553.

Circle No 372

LAN SERVER

- *Implements the ISO Open System Interconnection protocol*
- *Connects as many as 64 peripheral devices to a LAN*

The CS/1-OSI LAN communications server implements the full 7-layer Open System Interconnection (OSI) protocol as defined by the International Standards Organization (ISO). It can connect as many as 64 computing and peripheral devices to a LAN. These devices can include



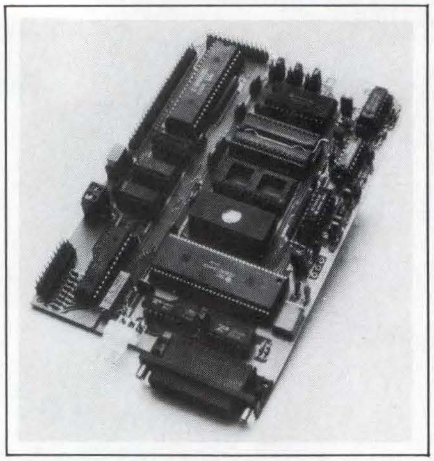
asynchronous, bit- and character-synchronous, and IBM-3270 Category A devices. The server is also compatible with the Technical and Office Protocols (TOP) 3.0, a specification of the OSI protocols layered over Ethernet (IEEE 802.3). In addition to Ethernet, the server is available in versions for token-ring LANs (IEEE 802.5) and for the vendor's 5M-bps CSMA/CD broadband LANs. The server's architecture uses a 16-MHz 68020 main µP and several 68000 µPs to offload communication-processing tasks from the host. A network-user log-in feature permits the independent configuration of each port in order to restrict access. The server also has a built-in packet generator, which lets you perform network diagnostics while the network is operational. Eight-port version, \$9900; 64-port version, \$16,000. OSI software, \$250. Delivery, 90 days ARO.

Bridge Communications Inc, 2081 Stierlin Rd, Mountain View, CA 94043. Phone (415) 969-4400. TLX 176544.

Circle No 373

μC BOARD

- *Uses a CMOS 64180 microcontroller chip*
- *Has floating-point Basic interpreter resident in ROM*



The Vitrax IX is a microcontroller board for digital control and data acquisition. It uses a CMOS 64180 μC that's compatible with the Z80 instruction set. The board contains a floating-point Basic-language interpreter in ROM, as many as 16k bytes of EPROM-based user code, and 16k bytes of CMOS static RAM that you can expand to 32k bytes. In addition, the device has an onboard EPROM programmer for code generation. It provides 24 bidirectional I/O lines; two full-duplex asynchronous RS-232C channels with data-transfer rates as high as 18,200 baud; a Centronics printer port; an optional 8-channel, 10-bit CMOS A/D converter; and an optional real-time clock/calendar. The unit operates on a 5V power supply with a current drain of less than 150 mA. It is supplied as a $4\frac{1}{2}\times6\frac{1}{2}$-in. pc board in kit and assembled forms. Basic kit and manual, \$139.50; 8-channel, 10-bit CMOS A/D converter, \$39.50; CMOS real-time clock/calendar, \$34.50.

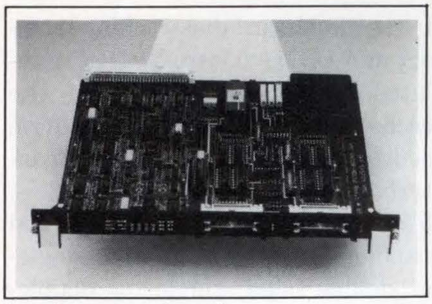
Sintec Co, 28 8th St, Frenchtown, NJ 08825. Phone (800) 526-5960; in NJ, (201) 996-4093.

Circle No 374

ANALOG I/O CARDS

- *Provide 12-bit, 64-channel analog input*
- *Available with software drivers for OS-9/68000*

The VME-68320-ADC and -68330-DAC are VME Bus-compatible ana-



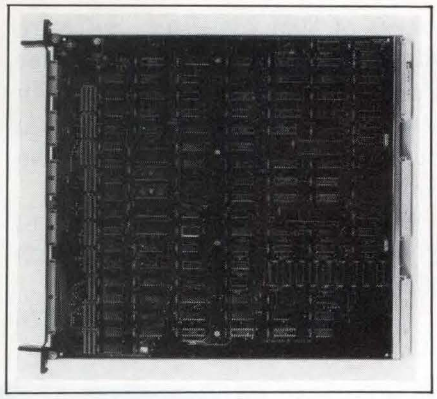
log input and analog output cards, respectively. The VME-68320-ADC provides 64 single-ended or 32 differential input channels, which are digitized to 12-bit resolution at a conversion rate of 50k readings/sec. The input ranges for the A/D converter are 10V for a unipolar input, or ±10 or ±5V for a bipolar input. A programmable gain amplifier on the front end allows you to introduce gain of ×1, ×2, ×4, or ×8, or a user-defined gain factor. A patch panel is provided next to each input connector so that you can add your own signal-conditioning circuitry. The VME-68330-DAC provides eight 12-bit analog outputs. You can select bipolar output ranges of ±2.5, ±5, or ±10V or unipolar output ranges of 5 or 10V. Both boards have onboard dc/dc converters that allow them to operate from the VME Bus 5V supply. Software drivers for the OS-9/68000 operating system are available for the boards. VME-68320-ADC, DM 2480; VME-68330-DAC, DM 1750.

EKF Elektronik Messtechnik GmbH, Weidekampstrasse 1A, 4700 Hamm 1, West Germany. Phone (02381) 12630. TLX 828621.

Circle No 375

DISK CONTROLLER

- *Board for Sun 3 workstations supports four SMD/SME drives*
- *Is the same size as Sun's triple-high, triple-wide cards*



An enhancement of the Rimfire 3200, the Rimfire 3220 is a VME Bus disk-controller board for Sun 3 workstations. The board has the same dimensions as do Sun's triple-high and -wide cards, and it can support four SMD/SME drives via faceplate connections. It uses an 80186 μP to manage a 512k-byte segmented cache memory; the cache eliminates unnecessary seek and rotational delays by prereading disk files that span track boundaries. The board can handle SMD E-drive data rates to 24 MHz and can burst data across the VME Bus at rates in excess of 30M bytes/sec. Software support includes device drivers for Unix BSD 4.2 and SunOS. You can also obtain software that boots a Sun 3 workstation directly from the controller. $3495.

Ciprico Inc, 2955 Xenium Lane, Plymouth, MN 55441. Phone (612) 559-2034.

Circle No 376

DISK CONTROLLER

- *Incorporates a disk cache to speed data transfers*
- *Handles four mixed-format floppy-disk drives*

To achieve disk access at data rates as high as 500k bytes/sec, the FCM1 floppy-disk-drive controller card for G64 Bus systems incorporates 8k bytes of onboard disk-caching memory and a DMA controller that regulates data transfer between the cache memory and floppy disk-drive controller. The Eurocard board interfaces with as many as four 3.5-, 5.25-, or 8-in. floppy-disk drives and handles any combination of single- or double-sided, single- or double-density drives. The device operates from a 5V supply and consumes 600 mA. You can obtain a driver for the OS9 operating system. £318.

Syntel MicroSystems, Queens Mill Rd, Huddersfield, Yorkshire HD1 3PG, UK. Phone (0484) 535101. TLX 51194.

Circle No 377

PHOTOPLOTTER

- *Achieves a resolution of 2540 dots/in.*
- *Accommodates film sizes to 18×24 in.*

Suitable for use with pc-board CAD systems, the L1 drum photoplotter uses a raster-scan technique and a 5-mW focused-beam argon-ion laser to provide a resolution of 2540 dots/in. The blue light emitted by the laser exposes low-cost orthochromatic film. The imaging area is 25×25 in. and supports standard film sizes as large as 18×24 in. The largest film sizes are exposed in less than five minutes. A vacuum holds the film against the inside of the drum during operation. The photoplotter links to a host computer via an RS-232C serial interface and accepts RS-274 (Gerber) photoplot data. It works with the company's S44 artwork editor and CAM workstation software. From 300,000 to 400,000 Sw Fr.

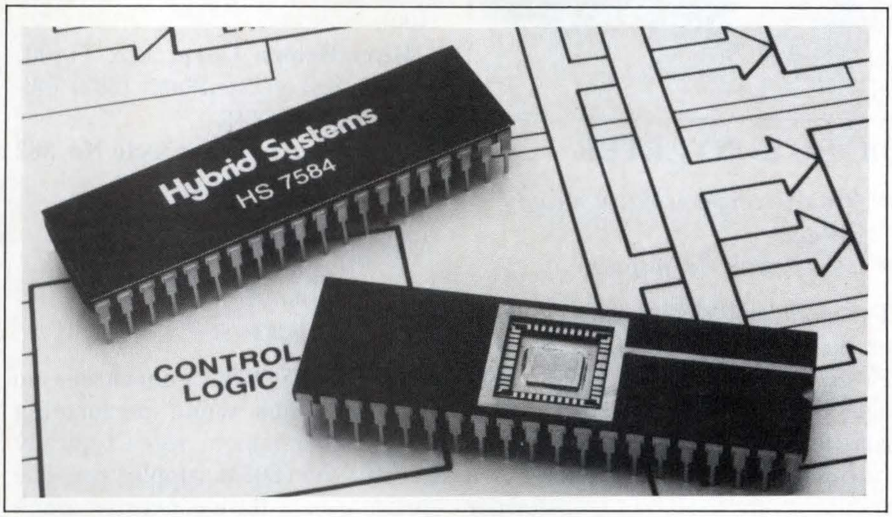
EIE Electronic Industrial Equipment SA, 15 rue Marziano, 1211 Geneva, Switzerland. Phone (022) 423260. TLX 429484.

Circle No 378

INTEGRATED CIRCUITS

12-BIT QUAD MDAC

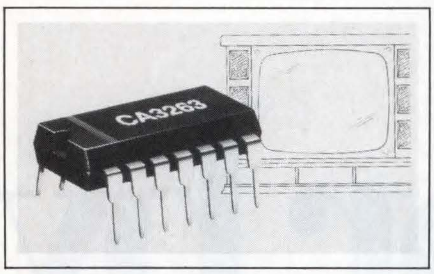
- *Four 12-bit CMOS DACs on a single monolithic chip*
- *Each DAC provides two outputs*



The CMOS HS-7584 contains four multiplying DACs, each having two current outputs and a separate reference input and feedback resistor. The double-buffered input structure accepts 12-bit parallel data or 8-bit/4-bit data, and interfaces with a μP. The use of thin-film resistors ensures 12-bit accuracy, and each DAC is laser trimmed for linearity and gain matching. The device's current-output settling time is 3 μsec max. The converter operates from a single 5V supply and draws 1 to 10 mA of current, depending on the input logic levels. The device comes in a hermetic 40-pin ceramic DIP or a 40-pin ceramic LCC. HS7584C, $62; HS7584B, $120 (100). Delivery, six to eight weeks ARO.

Hybrid Systems, 22 Linnell Circle, Suburban Industrial Park, Billerica, MA 01821. Phone (617) 667-8700. TWX 710-347-1575.

Circle No 379



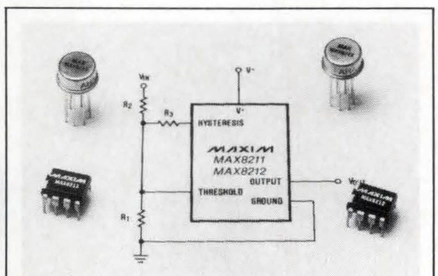
TV TUNER CONTROL

- *Supports multiple tuning functions*
- *For use in either frequency- or voltage-synthesized tuners*

The CA3263 provides interface control for TV/CATV tuning systems and can drive either frequency- or voltage-synthesizer tuners. Two logic-level inputs (0 or 5V) operate the IC's bandswitch controller, whose outputs drive the supply voltages of the VHF, UHF, and Superband bands in the tuner. At a supply voltage of 12V, the bandswitch controller's output voltages are 11.3V min at a current of 30 mA. You can use its inverting and noninverting op amps to amplify error signals or serve as active-filter elements with tuners using phase-locked loops. The IC comes in a 14-pin DIP and costs $1.00 (100).

GE Solid State, Route 202, Somerville, NJ 08876. Phone (201) 685-6994.

INQUIRE DIRECT



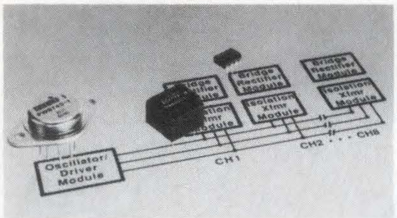
VOLTAGE DETECTORS

- *2 to 16.5V operation*
- *Three temperature ranges available*

The MAX8211 and MAX8212 are programmable voltage detectors for use in power-supply monitoring applications. They contain a comparator, a 1.15V (±40 mV) bandgap reference, and an open-drain N-channel output driver. The devices operate from a 2 to 16.5V supply and draw a maximum supply current of 15 μA. The 8211 provides a 7-mA current-limited output sink when the threshold pin is below the reference voltage. On the 8212, inputs above the reference voltage activate the output, which is not current limited and can typically sink 35 mA. The hysteresis-type output can typically source 10 mA, allowing you to apply positive feedback for noise-free output switching. The applications include undervoltage and overvoltage detection, battery-backup switching, and power-supply fault monitoring. MAX8211MTY and MAX8212MTY in hermetic TO-99 metal cans for military applications, $5.75; MAX8211EPA and MAX8212EPA in 8-pin plastic DIPs for industrial and commercial applications, $2.14 (100).

Maxim Integrated Products, 510 N Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 381



DC/DC CONVERTER

- *Provides eight isolated supply voltages*
- *±7 to ±20V dc outputs*

The modular PWS740 dc/dc converter consists of three components: PWS740-1, housed in a TO-3 package, is a 400-kHz oscillator/driver that drives as many as eight separate power outputs; PWS740-2 is a trifilar-wound isolation transformer in a plastic package; PWS740-3 is a high-speed rectifier bridge in a plastic, 8-pin miniature DIP. By sharing a common power driver among several channels and using board-mounted transformers and rectifiers, you can generate bipolar isolated power to ±30 mA for about \$6 to \$8/channel. PWS740-1, \$12.75; PWS740-2, \$2.50; PWS740-3, \$1.25 (100).

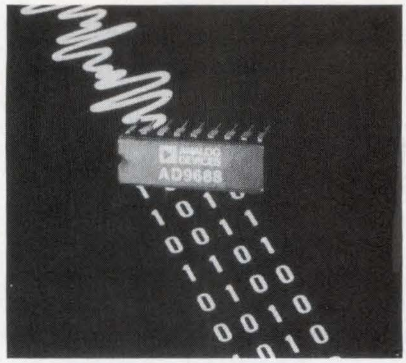
Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 382

A/D CONVERTER

- *4-bit output*
- *200M samples/sec*

The AD9688 ADC guarantees no missing codes while performing 4-bit conversions at rates typically greater than 200M samples/sec. The device uses a flash-converter architecture to provide 7-bit linearity, which equates to 0.0625 LSB for a 4-bit device, and you can stack multiple units to obtain 6-bit resolution via the overrange output terminal. The converter accepts analog input



signals between −2.7 and 3.0V; all digital inputs and outputs are ECL compatible. The device is pin compatible with the AMD AM6688. A small-signal bandwidth of 200 MHz (−3 dB) and low input capacitance of 13 pF eases the device's application in high-speed designs. The applications include ECM (electronic countermeasure), digital radio systems, and low-resolution radar guidance for smart munitions. Available in either an 18-pin ceramic DIP or a 20-pin ceramic LCC, the converter typically consumes <700 mW of power from 5V and −5.2V power supplies. From $20 (100).

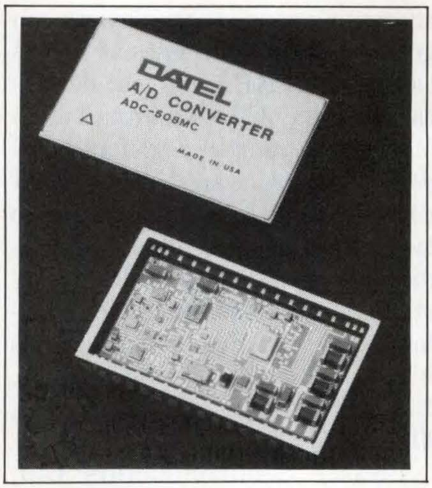
Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700. TWX 710-394-6577.

Circle No 383

12-BIT ADC

- *800-nsec conversion time*
- *Pin-programmable inputs*

Performing a 12-bit conversion in a maximum of 800 nsec and dissipating a maximum power of 1.9W, the ADC-508 offers the best speed/power ratio available in this type of product, according to the manufacturer. The converter's performance is a result of the digitally corrected, subranging architecture, which is enhanced by the use of a custom chip and laser-trimming techniques. The device's features include low



initial errors of 3 LSB for both offset and gain, CMOS/TTL compatibility, and 3-state outputs. Other features not usually available in 12-bit, high-speed converters are pins that provide different coding selections, an indication of signals that are above or below the full-scale range, and a means of improving throughput by putting the S/H function back into the sample mode before the circuit completes the existing conversion. The ADC-508 has three pin-programmable input ranges: 0 to 10V, 0 to 20V, and ±10V. For commercial temperature range, $330; for military temperature range, $399.

GE Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-3000. TWX 710-346-1953.

Circle No 384

ADDRESS GENERATOR

- *Provides programmable address sequences*
- *Cascadable for greater addressing range*

Suitable for use in DMA, database addressing, and waveform-synthesis applications, the PDSP1640A address generator allows you to generate complex 8-bit address sequences at speeds as high as 40 MHz. You can cascade devices to increase the

CIRCLE NO 24

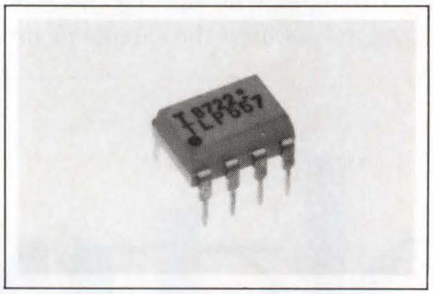
addressing range. Two devices can generate 16-bit addresses at speeds as high as 20 MHz, and four devices can generate 32-bit addresses at 15 MHz. Five internal registers allow you to perform variable increment counting and conditional jumps to two internally stored branch addresses or to an externally generated address. A masking facility allows you to jam selected address bits. PDSP1640A, in a 28-pin DIP, £35; PDSP1640, a 20-MHz version, £10 (1000).

Plessey Semiconductors Ltd, Cheney Manor, Swindon, Wiltshire SN2 2QW, UK. Phone (0793) 36251. TLX 449637.

Circle No 385

Plessey Semiconductors, 9 Parker, Irvine, CA 92718. Phone (714) 472-0303.

Circle No 386



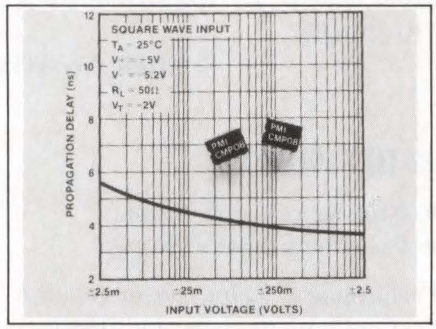
POWER OPTOCOUPLER

- *High-speed capability*
- *Can drive power transistors having ratings as high as 20A*

Packaged in an 8-pin DIP, the TLP557 contains a GaAlAs LED and a high-gain, high-speed integrated photodetector. The device's output current is suitable for driving power transistors that have ratings to 20A. An external resistor between pins 6 and 7 of the device creates a constant-current output that provides a stable base drive for power transistors or modules. The optocoupler has an input threshold current of 5 mA and a switching speed of 1 μsec, and operates from a 15V supply. $2 (1000). Delivery, 12 weeks ARO.

Toshiba America Inc, ECBS, Semiconductor Products Div, 2692 Dow Ave, Tustin, CA 92680. Phone (714) 832-6300.

Circle No 387



150-MHz COMPARATOR

- *Complementary ECL output*
- *9.5-nsec propagation delay*

The 150-MHz CMP-08 comparator responds in 6.5 nsec to a 5-mV overdrive. The maximum response time over temperature is 9.5 nsec for the industrial-grade device and 12 nsec for the military device. The device offers improved stability in the transition region; the resulting oscillation-free performance eliminates the need for a minimum slew-rate requirement for its inputs. The analog input range is −3 to 2.7V when connected to a 5V supply. It comes in an 8-pin miniature DIP. Industrial grade, $3.35; military grade, $7.10 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 310-371-9541.

Circle No 388

ANALOG/DIGITAL ASICs

- *Provide as many as 2500 analog and digital components*
- *Include on-chip power Darlingtons*

This family of five bipolar analog/digital arrays ranges in complexity from 400 to 2500 components that you can customize with 2-level metal. The arrays contain customizable tiles of I^2L and ECL logic elements, npn and pnp transistors,

and power Darlingtons. They also have standard analog functional blocks, including an RC- or crystal-controlled oscillator, a bandgap reference, a 6-bit D/A converter, a high-frequency op amp, a voltage reference, and an ECL reference. The npn transistors have an F_T of 3 GHz. The on-chip npn power Darlingtons can switch 200 mA, and you can configure them to create a 200-mA bridge output stage. Alternatively, you can use 30-mA pnp transistors to produce complementary output stages. The ECL elements have multiple emitters that allow you to produce stacked logic configurations that contribute to a high packing density and high-speed operation. You can configure inputs and outputs for TTL compatibility or as ECL-compatible inputs and outputs suitable for operation at frequencies as high as 200 MHz. The I^2L logic elements operate at speeds as high as 2 MHz. The arrays have a 15V operating voltage range. The company provides VAX-based CAD software with schematic entry, SPICE simulation, and autolayout facilities, and an IBM-PC based system that uses PCAD software.

SGS-Thomson Microelectronics, 101 Blvd Murat, 75016 Paris, France. Phone (1) 45241716. TLX 611220.

Circle No 389

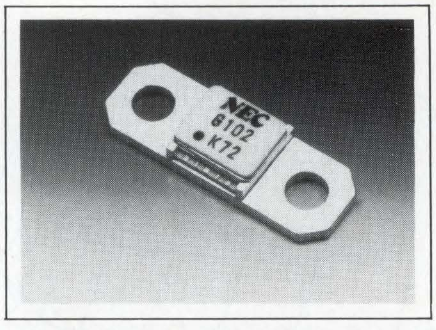
SGS-Thomson Microelectronics, 1310 Electronics Dr, Carrollton, TX 75006. Phone (214) 466-6000.

Circle No 390

GaAs MMIC

- *1- to 20-GHz bandwidth*
- *7-dB gain at 18 GHz*

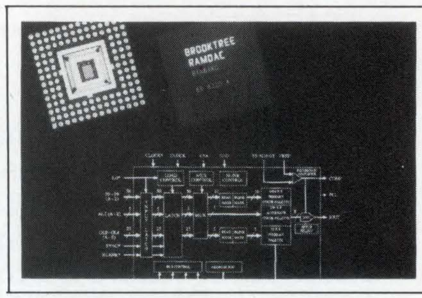
The UPG102 is the first in a series of new GaAs wide-band MMICs (monolithic microwave ICs) from NEC (Mountain View, CA). The device operates over an ultrawide frequency range from 1 GHz to 20 GHz and has a typical gain of 7 dB. The cascadable device has both its input



and output matched to 50Ω and has a power output of 10 dBm at 1 dB of compression. Typical applications are as a driver amplifier in commercial, military, and high-reliability applications requiring extreme bandwidths. The MMIC is available in chip form as the UPG102P and in a hermetic, ceramic package as the UPG102B. From $280 (100).

California Eastern Laboratories Inc, 3260 Jay St, Santa Clara, CA 95054. Phone (408) 988-3500.

Circle No 391



HIGH-SPEED RAMDAC

- *Operates to 175 MHz*
- *Offers 1024 colors plus a 256-color window*

The Bt461 second-generation high-speed RAMDAC incorporates a 1024×8-bit color look-up table, a 256×8-bit alternate palette, and a 32-word overlay palette. Constructed in CMOS, the RAMDAC includes an 8-bit DAC, a μP interface, and multiplexers. Originally designed to operate at 135 MHz, the final characterization of the 1.5-μm process shows a typical operating speed of 170 MHz. Applications for the RAMDAC are those requiring the display of large numbers of colors, such as true-color imaging and multiwindow environments. The de-

New Products

Control Point

Test and Control Systems Product News from Ziatech

Winter 1988 **Ziatech Corporation**

Inside Control Point

PAGE TWO

New Single Board Computers

The ZT 8808 and ZT 8809 are Ziatech's most IBM-compatible single board computers. The new computers feature a number of PC/XT peripherals, large on-board memory, and they support PC DOS, VRTX operating systems and user-developed ROM-based software.

PAGE THREE

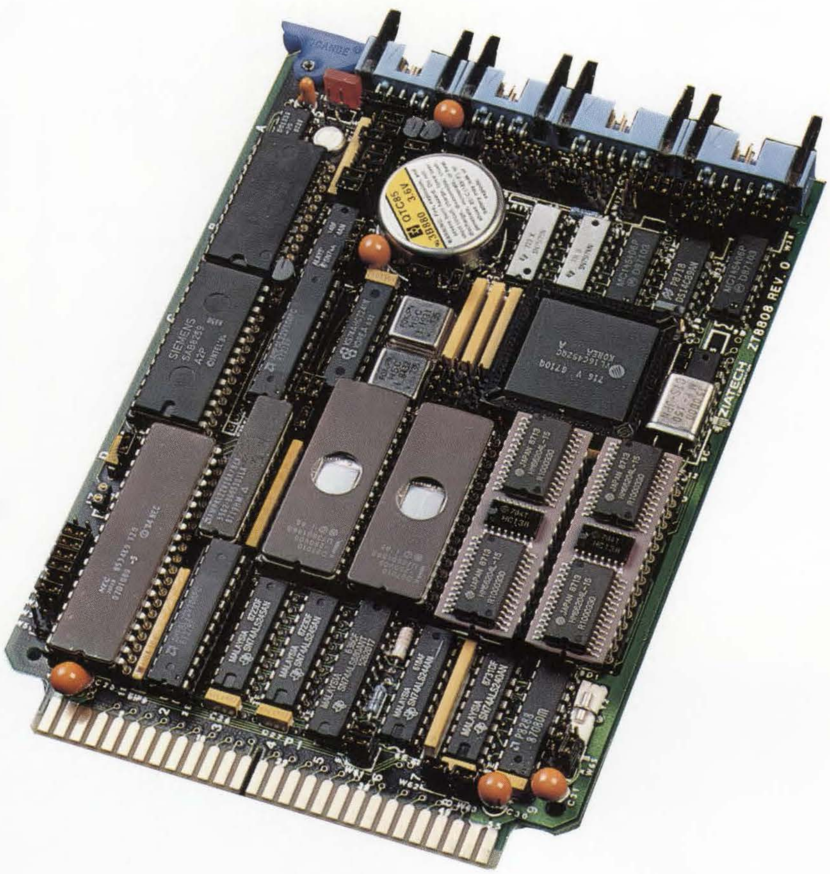
First Extended Memory System on STD Bus

Ziatech's new byte-wide STD Bus memory board extends the 8088/8086 family of processors' address space beyond 1 Mbyte via a memory-mapping technique called EMS. This memory board is supported in Ziatech's STD DOS systems for main memory expansion and as a RAM/ROM disk.

PAGE FOUR

Free GPIB, STD Bus Literature

Ziatech's STD Bus and IEEE 488 product lines are described in four separate catalogues. The Technical Data Book features the entire product line with separate technical guides also available on IEEE 488 products, STD DOS systems, and the Z-NET Local Industrial Network.



This new NEC V20-based Single Board STD Bus Computer, the ZT 8808, is the latest addition to Ziatech's family of single board computers (SBCs) for industrial control applications. The V20 microprocessor on the ZT 8808 is available in 5 or 8 MHz versions, giving the new SBC enhanced STD-8088 compatibility.

In addition to an on-board memory capacity of 512 Kbytes, the ZT 8808 contains several IBM PC/XT peripherals. These include three 16-bit counter/timers, two serial ports, a Centronics interface, and an interrupt controller. This new SBC features support for both operating systems and ROM-based systems, and will be available in a CMOS version later this year. (See story, page 2, and/or check box A on the return card.)

ZIATECH CORPORATION

New IBM PC/XT-compatible STD Bus Computers

Ziatech's new ZT 8808 provides a high level of functionality on a single board STD Bus computer at a reasonable cost. Based on the NEC V20 processor, a superset of the 8088, this single board computer (SBC) was designed to support both PC DOS and PROM-based industrial control applications.

PC/XT Peripherals

Available in 5 MHz (ZT 8808) and 8 MHz (ZT 8809) versions, these SBCs contain IBM PC/XT peripheral devices such as three 16-bit counter/timers, an interrupt controller, two serial ports, and a Centronics printer interface. 512 Kbyte on-board memory capacity and a wait state generator are also provided.

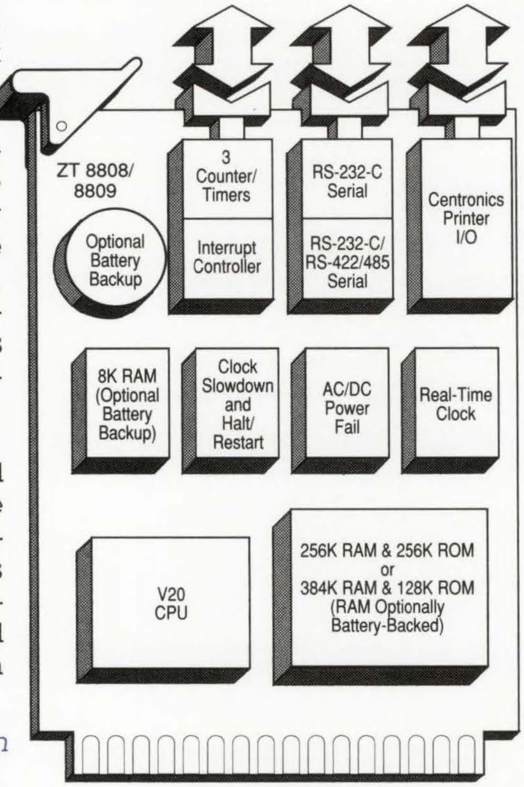
Software Development

The ZT 8808 and ZT 8809 are supported by STD DOS, Ziatech's implementation of PC DOS on the STD Bus. The PC compatibility of STD DOS allows developers to run sophisticated development tools on the STD target system to prepare for use with PC DOS or a PROM-based application. The new SBCs are also supported by Ziatech's STD Prototype Development System, which aids in the development of applications that don't need operating system support.

CMOS Version

The ZT 8808 and ZT 8809 will soon be available in CMOS versions for applications where low power consumption and extended temperature operation are required.

For more information on the ZT 8808/8809, check box A on the return card.



ZT 8808/8809 Functional Diagram

Ziatech's STD DOS Stand-Alone (SA) development system lets users develop STD Bus systems utilizing PC DOS or PROM-based operating software. The SA system is equipped with a monitor, keyboard and disk drives to enable it to function like a PC. Ziatech also offers a PC-assisted development system, which utilizes a user-supplied PC for its console and mass storage requirements.

About Control Point

Control Point is a bimonthly newsletter published by Ziatech Corporation for OEMs and system integrators designing industrial automation and instrumentation applications.

Control Point examines the new products, applications, and issues in today's test and control industries.

Ziatech Corporation, established in 1976, manufactures STD Bus-based computers, development and operating systems for the STD Bus, and IEEE 488 interfaces for MULTIBUS, STD Bus, and personal computer systems.

For more information on Ziatech STD Bus and IEEE 488 products, return the Control Point postcard, or call Ziatech at 805-541-0488.

Ziatech Brings Extended Memory System to Industrial Busses

The new ZT 8825 Extended Memory System from Ziatech is the first industrial bus memory board to use a unique memory-mapping technique which extends the amount of memory available to STD Bus systems. The ZT 8825 serves Ziatech's STD DOS systems in two different ways. It can function as a high speed, solid state disk, providing Ziatech's STD DOS systems with a 2 Mbyte PROM/RAM/BRAM disk capability. One RAMdisk can be configured (using multiple ZT 8825s) to contain many MBytes of data.

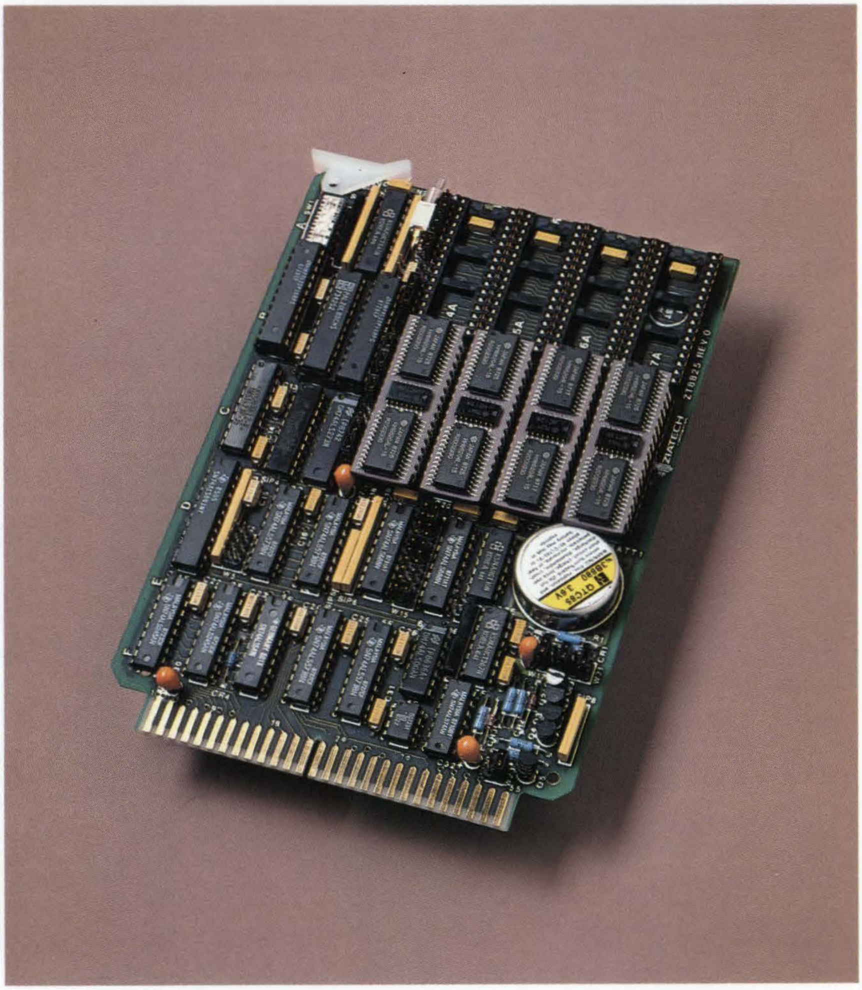
Expands Memory for STD DOS Systems

The ZT 8825 also can be used as an expanded address main memory. In this role it expands the logical address space while occupying only 16K of the base 1 Mbyte address space. The extended memory is mapped in the logical address space via map registers, which determine when and where the extended memory will be accessed. Lotus, Intel, and Microsoft jointly developed this technique, called the Expanded Memory System (EMS). EMS is becoming popular on PCs and is implemented in a growing number of PC software packages. The ZT 8825 also follows the "Enhanced Expanded Memory System," E^2MS, which is a superset of EMS.

Eight 32-pin JEDEC sockets

Eight 32-pin JEDEC sockets accept either EPROMs or RAMs in each grouping of four sockets. Battery backup is provided as an option.

For more information on the ZT 8825, check box B on the return card.



The ZT 8825 Extended Memory System is the first industrial bus memory board to use the Expanded Memory Specification (EMS).

ZT 8825 Extended Memory System Features

- *Direct 20- and 24-bit addressing (STD-8088 compatible)*
- *Two sets (4 sockets each) of independently configured 32-pin JEDEC sockets*
- *Optional 1 Amp-hour lithium battery for RAMs (BRAM)*
- *No wait states required at 5 or 8 MHz for fast memory device types*
- *Supports various combinations of RAM (32K, 128K, 512K chip size) and EPROM (16K to 1 Mbyte chip size)*
- *Supports PROM & RAM disk configurations in STD DOS*
- *Supports EMS and E^2MS paging specifications*
- *2 Mbyte maximum on-board storage, mappable in 16K pages*

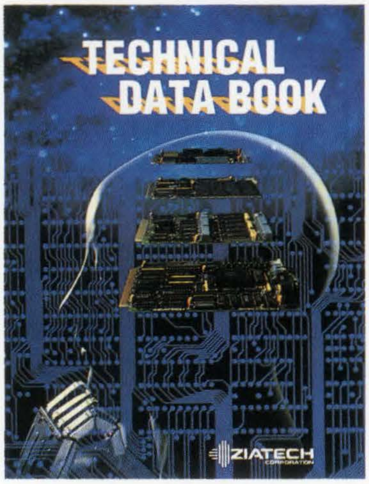
ZIATECH CORPORATION

CIRCLE **120** ON INQUIRY CARD

Free STD Bus, GPIB Product Literature from Ziatech

Technical Data Book Features Entire Ziatech Product Line

Ziatech's 200-page Technical Data Book provides product descriptions, photos, functional considerations and technical specifications of Ziatech's entire STD Bus and IEEE 488 product line.



The Technical Data Book also contains a New Product Section featuring Ziatech's most recently introduced products. It additionally features a comprehensive STD-8088 system designer's guide and the STD-8088 Bus specification.

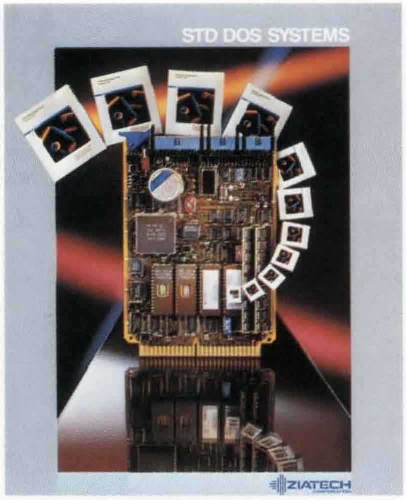
For a copy of the Technical Data Book, check box C on the return card.

IEEE 488 Products

A new 16-page brochure details Ziatech's line of IEEE 488 interfaces and driver software.

IEEE 488 interfaces for the IBM Personal System/2, the IBM PC, MULTIBUS systems and STD Bus systems are featured.

Complete descriptions and examples of Ziatech software support packages are also featured, including the new EZ.488, Ziatech's simplest driver software for integrating PC-based instrument systems.

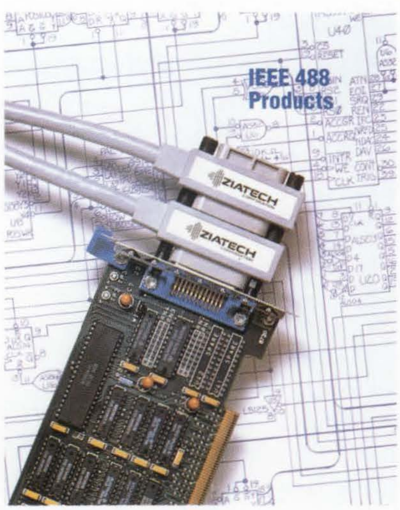


STD DOS Systems

A 24-page brochure describes Ziatech's line of PC DOS-based STD Bus systems, STD DOS.

Ziatech's STD DOS industrial computers execute PC-compatible software packages, both for system development and target operation. This brochure describes STD DOS architecture, performance, system configurations, options, software development, device driver software, and ordering information.

For a copy of the STD DOS brochure, check box F on the return card.

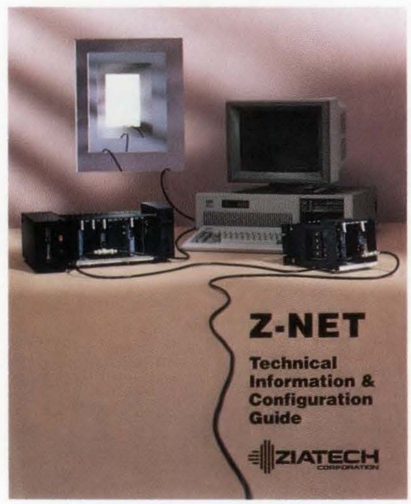


For a copy of the IEEE 488 brochure, check box D on the return card.

Z-NET Network Technical Guide

A new guide to Z-NET, Ziatech's Local Industrial Network for STD Bus and PC systems, is now available. Z-NET, based on the ARCNET protocol and ViaNet software, is a simple-to-use network that extends the capability of Ziatech's STD DOS systems for industrial applications.

The Z-NET Technical Information and Configuration Guide provides a comprehensive introduction to this STD Bus and PC network, and includes ordering information.



For a copy of the Z-NET guide, check box E on the return card.

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MEMBER
STDMG
STD MANUFACTURER'S GROUP

ZIATECH CORPORATION
3433 Roberto Court
San Luis Obispo, CA 93401 USA
ITT Telex 4992316
FAX (805) 541-5088
Telephone (805) 541-0488

vice provides the large palettes needed for superior graphics, and the 32×8-bit overlay palette gives the designer great flexibility in deciding what should run through the overlays, independent of the main graphics image. The device comes in a 132-pin pin-grid-array package and in three speed grades: 135-MHz, \$245; 110-MHz, \$204; 80-MHz, \$176.

Brooktree Corp, 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. TLX 383596.

Circle No 392

CMOS STATIC RAM

- *8k×8 bits*
- *Three speed versions*

Pin-compatible with the 2764 EPROM family, the MCM6064 requires no clocking for the chip-enable pins when operating in a fully static mode. The device has both active-high and active-low enable pins. The device goes into its low-power standby mode when either pin is not enabled. In standby mode, the device requires from 100 μA max to 3 μA min, at 5.5 to 2.0V, under typical operating conditions (a 0.6- to 1.0- μA version is available). Inputs and outputs are TTL compatible, and the outputs can assume a 3-state condition. The available speeds are 100, 120, and 150 nsec. Depending on speed selection, from \$3.36 to \$4.64 (500).

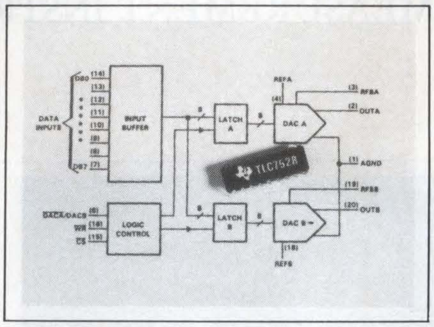
Motorola Inc, Technical Info Ctr, Box 52073, Phoenix, AZ 85074. Phone (512) 928-6705.

Circle No 393

CMOS DUAL DAC

- *Two 8-bit multiplying DACs*
- *Interfaces directly to DSP chips*

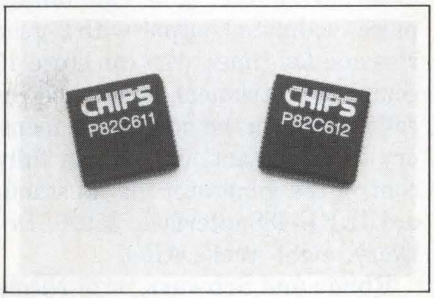
Designed with a high-speed control interface, the TLC7528 encompasses two, 4-quadrant 8-bit multiplying D/A converters on a single monolithic chip. Its control signals can interface directly with the TMS320 family of DSP chips. The



device's DACs use a common 8-bit input port. Each DAC consists of an inverted R/2R ladder, analog switches, and input data latches. Commercial grade, \$5.54; industrial grade, \$8.15 (100).

Texas Instruments Inc, Semiconductor Group (SC-775), Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.

Circle No 394



PS/2 CHIPS

- *Interface to IBM Micro Channel*
- *Provide memory, I/O functions, and peripheral control*

These chips provide a 100%-compatible interface to the IBM PS/2 Micro Channel architecture. The 82C611 furnishes memory and I/O functions, and the 82C612 provides control of peripherals. The products target manufacturers of add-in-board adapters. The 82C611 replaces 10 to 15 TTL devices, and the 82C612 replaces 25 to 30 TTL devices. The MicroChips are available in 68-pin PLCC and 80-pin PFP (plastic flatpack) packages. 82C611, \$8.65; 82C612, 11.10 (1000).

Chips and Technologies Inc, 3050 Zanker Rd, San Jose, CA 95134. Phone (408) 434-0600.

Circle No 395

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

SIGNAL GENERATOR

- *Covers 100 kHz to 1 GHz*
- *Has phase noise of −130 dBc at 100 MHz with 20-kHz offset*

The SMX signal generator covers the frequency range from 100 kHz to 1 GHz, providing output levels from −137 to +13 dBm in 0.1-dB steps at better than 1.5-dB accuracy. At 100 MHz, 20 kHz from the carrier, the phase noise is down at least 130 dB from carrier level. The generator provides both AM and FM at four fixed frequencies. An optional internal source modulates the carrier at a frequency that you can vary continuously over a range of 10 Hz to 100 kHz. If you use an external source, you can obtain pulse-modulated output with 2-μsec rise and fall times. You can store 40 complete instrument setups and recall them from the nonvolatile memory in an instant, or you can fully control the generator via its standard IEEE-488 interface. $5990. Delivery, eight weeks ARO.

Rohde and Schwarz, 4425 Nicole Dr, Lanham, MD 20706. Phone (301) 459-8800.

Circle No 396

CONVERTERS

- *Connect RS-232C and RS-422 devices to IEEE-488 bus*
- *Have μP with 64k- or 256k-byte buffer*

The GPIB-232CV and GPIB-422CV allow you to connect RS-232C and RS-422 devices to the IEEE-488 bus. They can interface to IEEE-488 instruments and controllers and provide transparent data conversion in either direction. Each converter is based on a 64180 μP (which features an integral DMA controller) and either a 64k- or 256k-byte buffer. This hardware permits data transferral from bus to buffer at 900k bytes/sec. When connected to a converter's serial port, the unit controls the rate at which the buffer empties. Each converter's μP automatically interleaves inbound and outbound data transfers. An SROEMPTY feature allows multiple users to share a single RS-232C or RS-422 device. With 64k-byte buffer, $495; with 256k-byte buffer, $695.

National Instruments Corp, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (512) 250-9119. TLX 756737.

Circle No 397

PS/2 CONTROLLER

- *Connects data-acquisistion modules to PS/2 Bus*
- *Uses one Micro Channel slot to connect 10 modules*

The PS/2 interface card, which occupies a single Micro Channel bus slot, connects the vendor's Series 500 data-acquisition system to the IBM PS/2 Model 50 and to higher models. The Series 500 chassis accommodates 10 data-acquisition modules from the vendor's catalog of 30 types, which include A/D and D/A converters; strain-gauge, thermocouple, and LVDT (linear variable differential transformer) signal conditioners; and digital I/O modules. The vendor supplies its software on 3½-in. disks for systems based on PS/2s. The latest software revision permits the transfer of data to applications software such as Lotus 1-2-3 and Asyst. $770.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (800) 552-1115; in OH, (216) 248-0400. TLX 985469.

Circle No 398

TEST GENERATOR

- *Runs on MicroVAX 2000 and VAXstation 2000*
- *Produces in-circuit and functional test programs*

VAXstation 2000 and MicroVAX 2000 can now run ATG-32 automatic test-generation software for the vendor's 227X family of midrange combinational test systems. ATG-32 runs four to eight times faster on the VAX hardware than it does on the PDP-11 series. After you simulate your pc board with the company's HiLo-3 simulator, the Hipost.DTS intelligent postprocessor converts the results into tester-specific functional test models. The test-generation software then uses these models to produce a combinational test program with functional and in-circuit tests. GRnet, the vendor's networking system, includes a test-procedure-management application that automatically uses Ethernet to transfer programs produced by ATG-32 from the VAXstation or MicroVAX to the tester. ATG-32 for VAXstation 2000, $15,000; for MicroVAX 2000, $20,000.

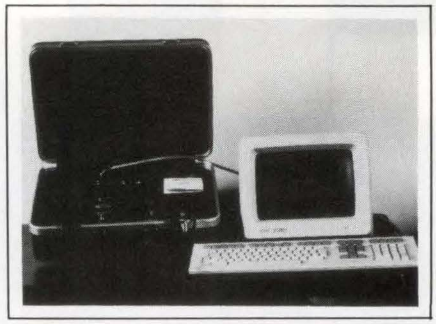
GenRad Inc, 300 Baker Ave, Concord, MA 01742. Phone (617) 369-4400.

Circle No 399

ETHERNET ANALYZER

- *Monitors network performance and isolates faults*
- *Includes lap computer acting as terminal emulator*

The LAN Specialist is a portable system that allows you to monitor the performance of an Ethernet network and diagnose network faults. It consists of a briefcase-sized unit and an IBM PC-compatible lap computer running software that makes it emulate a DEC VT-220 terminal.



You can use the analyzer separately from a network in order to verify the proper operation of units you plan to interconnect. You can also connect the analyzer to an operating network to obtain an indication of which units are producing errors (for example, transmitting messages that frequently collide). The analyzer can make quantitative measurements of network performance; for example, it can calculate network utilization, total errors, errors by station, and errors by type. It can also generate traffic to simulate the effect of expanding the network, thus providing a measure of the network's ability to accommodate additional nodes and additional traffic. $7600. Delivery, four to six weeks ARO.

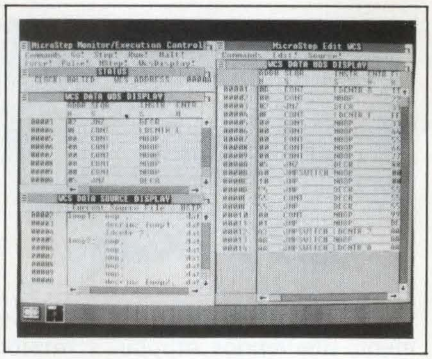
Cabletron Systems Inc, Box 6257, East Rochester, NH 03867. Phone (603) 332-9400. TLX 988059.

Circle No 400

DEVELOPMENT TOOLS

- *Let beginners develop microprogramming languages*
- *Work on IBM PC/AT*

The QuickLearn microprogram Starter Kit consists of a group of microprogram development tools: the MicroStep Personal Development Station, a plug-in board for the IBM PC/AT; the MetaStep Microprogram Language System; the EZStep Target System, a microprogrammable system on a board, and a tutorial; and the MetaStep Pro-



grammer's Environment. The Programmer's Environment software uses a menu-driven interface to help you define a custom microprogram language specific to your system's architecture. It also guides you through the processes involved in language development: definition, assembly, linking, and formatting. $6545.

Step Engineering, 661 E Arques Ave, Sunnyvale, CA 94088. Phone (800) 538-1750; in CA, (408) 733-7837. TWX 910-339-9506.

Circle No 401

VISION SYSTEM

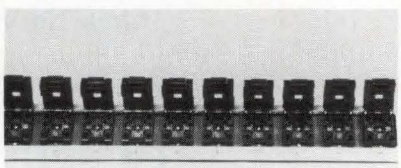
- *Uses 80386 with 16-MHz clock and zero-wait-state static RAM*
- *Compensates for light-intensity variations*

The Intellevue 386 vision computer is based on an 80386 μP with 1M bytes of zero-wait-state static RAM and an 80287 math coprocessor. A pattern-transform function provides gray-scale pattern matching independent of linear and nonlinear changes in light intensity and pattern contrast. A camera-calibration feature allows the system to compensate for nonorthogonal cameras, perspective distortion, and skewing. The system's windowing function allows you to treat six image buffers as a single spreadsheet and to define source and target windows across the boundaries of individual buffers. The system has four camera ports with standard RS-170 camera interfaces. For program develop-

ment, the vendor supplies a version of the Basic language containing extensions for machine vision. You can also develop programs for the system using the Microsoft C compiler on an IBM PC-compatible computer. $11,900 without camera; $14,900 with camera. Delivery, 60 days ARO.

Intelledex, 4750 SW Research Way, Corvallis, OR 97333. Phone (503) 758-4700. TLX 752441.

Circle No 402



SMD ADAPTER

- *Works with Data I/O 120/121A programmers*
- *Gang programs 10 PLCC EPROMs*

The Surface Mount Adapter works with Data I/O's 120/121A programmers and uses standard programmer instructions and readouts. It can gang program 10 PLCC (plastic leaded chip carrier) EPROMs on the programmer's 10 upper or lower sockets; you can employ two adapters simultaneously to program 20 devices. To use the adapter, you drop it into the programmer and lock it in place, then you place the master device containing the data to be copied in the first socket of the upper bank of 10. The PLCC sockets are vertically oriented; after programming, you actuate an ejector to pop the devices out of the adapter. $2000. Delivery, four to six weeks ARO.

Program Automation Inc, 22706 Aspan St, Suite 308, El Toro, CA 92630. Phone (714) 859-8200.

Circle No 403

HANDHELD DMM

- *Displays 4½ digits*
- *Provides 0.05% basic dc accuracy*

The 380451 4½-digit handheld multimeter's LCD readout provides dc accuracy of ±(0.05% of reading + two digits). The unit provides visual continuity and low-battery indicators, and a data-hold feature that lets you observe readings after you've disconnected the probes from the circuit under test. You select functions and ranges via a 24-position rotary switch. The meter's ranges cover 200 mV to 1 kV ac and dc; 2 mA to 10A ac or dc; and 200Ω to 20 MΩ. A 0Ω adjustment applies to the lowest resistance range only; the other ranges require no adjustment. The meter has a built-in tilt stand for benchtop use. $129.

ExTech Instruments Corp, 150 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440. TLX 940913.

Circle No 404

CONTINUITY TESTER

- *Uses IBM PC or compatible as host*
- *Learns continuity from known-good unit*

You can buy the PC-CAT continuity/discontinuity tester configured for either 128- or 256-point measurements and can expand it to handle as many as 64,000 points. You can choose a desktop, roll-around, or rack-mount model. The tester uses your IBM PC or compatible computer as a controller. Its PC-bus-compatible interface card also works in IBM's PS/2 Model 25 and PS/2 Model 30. Unlike some continuity testers, which merely determine whether the resistance is higher or lower than a fixed threshold value, the PC-CAT actually measures the value of resistance between selected points. This resistance-measuring capability lets you use the unit as a static in-circuit tester for loaded pc boards. To conduct high-volume testing, you mate the PC-CAT to bed-of-nails fixtures, which are available from other vendors. 128-point unit, $2395; 256-point unit, $2995.

CEI of Florida Enterprises Inc, 2050 2nd Ave S, St Petersburg, FL 33712. Phone (813) 822-3001.

Circle No 405

FUNCTION GENERATOR

- *Provides function-generator outputs for bench or ATE systems*
- *Has an optional, pulse-generator output*

The Model-4434 function generator provides sine, triangular, square, and pulse waveforms from 5 to 50 MHz. It features normal, gate, triggered, and synthesized modes. It can vary the duty cycle and can generate signal trains that have variable initial phases. If you obtain the B-channel option, the instrument will also provide pulse-generator functions such as adjust-

able pulse width, single or double pulses, and adjustable rise and fall times. Each channel has a maximum output amplitude of 30V p-p. You can drive the B channel directly from the function generator, or you can connect it to an external generator via the instrument's clock input. You can obtain more complex waveforms by summing two signals. The instrument's modulation modes include external FM and internal or external variable-rate AM. Its nonvolatile memory lets you store as many as 25 instrument setups. The instrument has an IEEE-488 interface. Single-channel version Fr fr 62,000; with B-channel option, Fr fr 80,000.

Schlumberger Instruments-Enertec, 5 rue Daguerre, 42030 Saint-Etienne Cedex 2, France. Phone 77252264. TLX 300796.

Circle No 406

Solartron Instruments, 2 Westchester Plaza, Elmsford, NY 10523. Phone (914) 592-9168.

Circle No 407

EMULATOR

- *Supports 68030 at 20 MHz*
- *Dequeues data to provide intelligible trace display*

The 68030 Probe/3 in-circuit emulator supports real-time emulation of Motorola's 68030 μP at clock rates to 20 MHz. To make the trace display intelligible, the unit's postprocessing program weeds out prefetched, but unexecuted, instructions and data. Though the

unit requires an IBM PC/AT or compatible computer for control, it provides both symbolic and source-level debugging support for code compiled on other machines, such as the Sun 4.2 BSD C compiler, Unix System V compilers that run on a DEC VAX or workstation, and Greenhills and Microtec Research compilers that run on a variety of computers. 16-MHz version, $16,450; 20-MHz version, $18,450.

Atron, 20665 Fourth St, Saratoga, CA 95070. Phone (408) 741-5900. TLX 989939. FAX (408) 741-1293.

Circle No 408

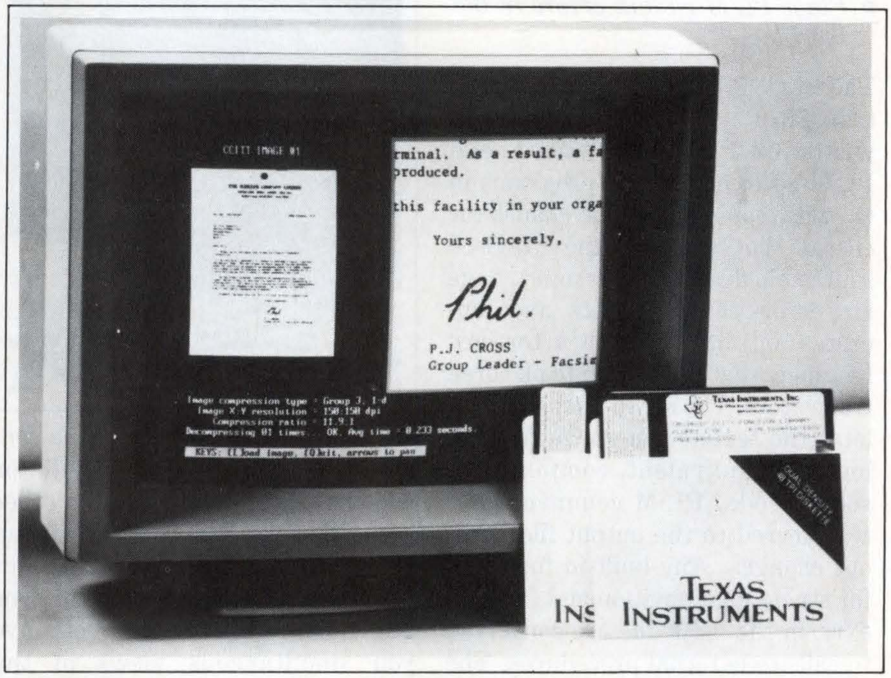
NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

FUNCTION LIBRARY

- *Provides image-compression and -decompression functions*
- *Conforms to CCITT Group 3 and Group 4 image standards*

The CCITT Function Library lets the vendor's TMS34010 graphics processor IC act as an embedded controller for facsimile, CD-ROM, image-scanner, and magnetic-storage systems, all of which have adopted the CCITT Group 3 and Group 4 standards in order to reduce a monochrome image's required storage space by a factor of 20 or more. The library consists of a compression function and a decompression function; both are written in TMS34010 assembly language. The routines come in source-code form (on a 5¼-in. disk or on 1600-bpi tape) and generate 38k bytes of object code. You can call either routine from a C applications program. Payment of the $3000 license fee entitles you to make unlimited executable copies.



Texas Instruments, Semiconductor Group (SC-772), Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.

Circle No 420

FILTER DESIGNER

- *Lets you design FIR and IIR digital filters*
- *Provides on-screen frequency-response plots*

The DFD program lets you design FIR (finite-impulse response) and IIR (infinite-impulse response) digital filters, and runs on the IBM PC and compatible computers. You specify the desired characteristics, such as filter type, sampling rate, cutoff frequency, and passband and stopband ripple; the program then computes the configuration and component values that will most closely approximate the filter characteristics that you want. The FIR-filter types include multiband pass or stop types, differentiators, and Hilbert transformers. The program can design lowpass, highpass, bandpass, and bandstop filters of Butterworth, Chebyshev, or elliptic types. $169.

Microcraft Corp, Box 513, Thiensville, WI 53092. Phone (414) 241-8144.

Circle No 421

IC DESIGN TOOL

- *Handles design from schematic entry to layout*
- *Includes analog and digital device libraries*

Solo-1200 runs on a variety of desktop workstations—including the IBM PC/AT, Sun, Apollo, and DEC units—and allows you to design mixed analog/digital ASICs. The package provides circuit description via schematic capture or use of the Model hardware description language; switch-level simulation; fully automatic placement and routing; and test-vector generation. To ensure design integrity throughout the design process, the package also contains a design manager that forces you to adopt good design practice. The system comes with a set of device libraries that include analog functions, gate-level and MSI-level components, 74LS family components, parameterized macros, and functional equivalents of the company's SystemCell standard cell library. Analog functions include 8-bit A/D and D/A converters, multiplexers, op amps and comparators, oscillators, and voltage references. Digital functions include compacted high-complexity RAM blocks; ROM and PLA blocks are being added to the library. Price for a system that runs on an Apollo or Sun workstation, £29,000.

European Silicon Structures Ltd, Mount Lane, Bracknell, Berkshire RG12 3DY, UK. Phone (0344) 525252. TLX 847724.

Circle No 422

PL/M-TO-C TRANSLATOR

- *Translates existing PL/M programs to C*
- *Flags PL/M syntax errors in the list file*

The PLC86, PLC51, and PLC80 are translators that convert programs written in PL/M-86, PL/M-51, and PL/M-80 to equivalent programs in C, with comments. The translator checks the syntax of the PL/M-86 source file designated as input, flags any errors that it detects, and generates an output file in a tertiary language that is common to all three translators. The second phase translates the tertiary-language file into logically equivalent, compilable C source code. PL/M comments are transferred to the output file without changes. Any built-in functions for string manipulation and I/O that exist in the input file are converted to calls to external procedures. The C source code conforms to the Kernighan and Ritchie standard, with the addition of the *enum* data type. To run any of the three translators, you need an IBM PC, PC/AT, or a compatible computer that has at least 256k bytes of RAM and runs under MS-DOS 2.1 or a later version. $475 each.

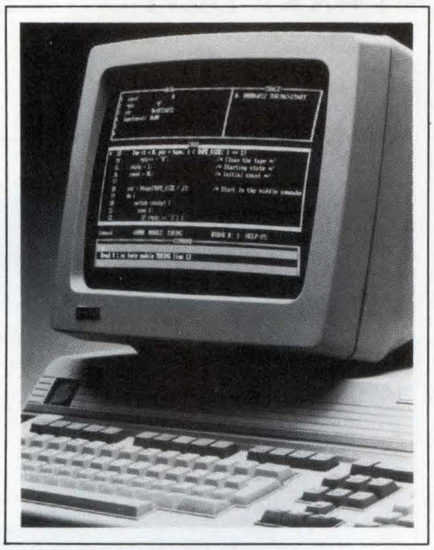
Micro-Processor Services Inc, 92 Stone Hurst Lane, Dix Hills, NY 11746. Phone (516) 499-4461.

Circle No 423

C DEBUGGER FOR VAX

- *Provides source-level debugging facilities for C programs*
- *Debugs code for 68000-family μPs*

Validate/XEL is a source-level debugger for C programs that runs on 68000-family μPs. This version of the debugger runs on VAX and MicroVAX workstations and consists of two portions: a source-level debugger and a C crosscompiler from Microtec Research (Santa Clara, CA). Two versions of the debugger are available: One is an inte-



grated tool that works with the vendor's ES 1800 in-circuit emulator and the target hardware; the other is a simulator that lets you debug your software before the target hardware is available. Both versions are window oriented, and both give you simultaneous views of the source code and the corresponding machine code, together with the contents of registers, variables, and stacks. The MCC68K crosscompiler creates compact code that is optimized for fast execution. From $12,500 for the MicroVAX version.

Applied Microsystems Corp, Box 97002, Redmond, WA 98073. Phone (800) 426-3925; in WA, (206) 882-2000. TLX 185196.

Circle No 424

SIMULATOR

- *Provides high-frequency, nonlinear-analysis capability*
- *Helps you design large-signal circuits such as limiters and mixers*

The Libra harmonic-balance simulation program combines linear analysis in the frequency domain with time-domain analysis of nonlinear elements. The package includes the vendor's Touchstone frequency-domain simulator for linear simulation. By extending the file to include appropriate models, you can add nonlinear-analysis capabilities. The simulator will show you time-dependent voltage waveforms at any node; time-dependent current into any nonlinear device; power density and total power; frequency-selective power; and frequency-selective voltage and current, including phase response. You can transfer all of the data from a simulation to a disk file. If you need steady-state response to sinusoidal waveforms, the package lets you obtain solutions based on the vendor's library of microwave components. A new large-signal and small-signal model for GaAs FETs improves the precision of nonlinear simulations of microwave active networks. The program currently runs on VAX/VMS workstations, Apollo Domain-IX workstations, and HP 9000, Series 300 computers under the HP-UX operating system. Prices start at $20,000 and depend on the system configuration.

EEsof Inc, 5795 Lindero Canyon Rd, Westlake Village, CA 91362. Phone (818) 991-7530. TLX 384809.

Circle No 425

GaAs LOGIC LIBRARY

- *Has simulation models for gate arrays and standard cells*
- *Lets you create schematic net lists and test vectors*

The ASIC Designer's WorkSystem has been augmented by a simulation model of TriQuint's (Beaverton, OR) TQ3000 GaAs gate array and simulation models for TriQuint's Q-Logic family of GaAs standard cells. These libraries let you use the vendor's Designer's WorkSystem to create schematic net lists and test vectors in the form that TriQuint requires for physical layout and manufacture of your design. The TQ3000 is an array of 3000 equivalent GaAs gates for applications that operate at frequencies as high as 1 GHz. The Q-Logic standard cells feature 100-psec gate delays, 2-GHz clock speeds, and integration levels as high as 1500 equivalent gates. TQ3000 design manual and

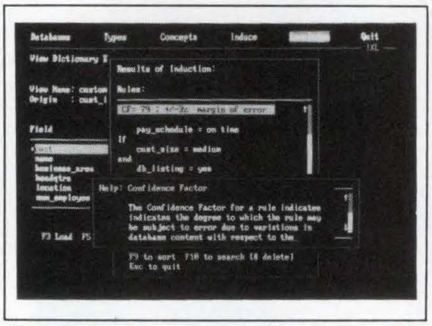
software libraries, \$3000; Q-Logic design manual and software libraries, \$495.

Tektronix Inc, CAE Systems Div, Box 4600, Beaverton, OR 97076. Phone (800) 547-1512; in OR, (503) 645-6464.

Circle No 426

DATABASE ANALYZER

- *Combines AI techniques with statistical techniques*
- *Can perform complex predictions on very large databases*



IXL: The Machine Learning System combines statistical methods, symbolic data analysis, induction, and deduction to explore and reveal previously unknown data interdependencies and relationships in very large databases. You can specify the level of error you are willing to accept, the kind of rules that the program should use, and the concepts (both exact and inexact) that the program should use in constructing the rules. The program presents its results in the form of the percentages of data elements that conform to each rule, with a confidence factor based on the variations in the database contents. The user interface is menu driven; it prompts you for all the information it needs, so you don't need any programming experience to use the program. To run the program, you'll need an IBM PC/XT, PC/AT, or a compatible computer that's equipped with at least 512k bytes of RAM and a hard disk. \$490.

IntelligenceWare Inc, 9800 S Sepulveda Blvd, Suite 730, Los Angeles, CA 90045. Phone (213) 417-8896.

Circle No 427

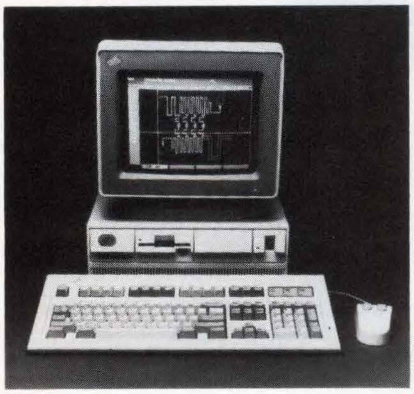
MATH SOFTWARE

- *Runs on 80386-based machines with 80387 or Weitek 1167*
- *Includes numeric analysis and matrix computation*

The 386-Matlab is a new version of the well-known Matlab (matrix laboratory) interactive mathematical software package for scientists and engineers. This version runs on 80386-based computers that are equipped with an 80387 numeric coprocessor. A second version, 386/Weitek-Matlab, runs on 80386-based machines that are equipped with the Weitek 1167 high-speed math coprocessor. Both versions run in the protected mode of the 80386 and can thus use all the memory in the system. The program accepts commands in standard mathematical notation, and its basic data object is a matrix that does not require dimensioning and that allows you to solve numeric problems in much less time than you'd need to write an equivalent program in Fortran, Basic, or C. The amount of physical memory in the system is the only limit on matrix or vector sizes, and on the number of variables that you can use. To run the program, you need an 80386-based computer equipped with an 80287 or 80387 numeric coprocessor or the Weitek 1167 coprocessor; at least 1M bytes of RAM; and an IBM CGA or compatible board, an IBM EGA or compatible, or a Hercules monochrome graphics card. 386-MATLAB, $1495. 386/Weitek-MATLAB, $1995.

The Math Works Inc, 20 N Main St, Suite 250, Sherborn, MA 01770. Phone (617) 653-1415. TWX 910-240-5521.

Circle No 428



ENHANCED CAD

- *Lets you create artwork for complex microwave/RF circuits*
- *Can activate as many as 35 drawing files simultaneously*

MiCAD II is an enhanced version of the vendor's earlier CAD program for designing microwave/RF circuits and subassemblies and for generating the corresponding artwork. Added features in the user interface include the ability to create user-defined shapes, a rubberbanding capability, better prompts and help screens, and the ability to use single or dual monitors. The database can now handle large and complex designs such as stripline layouts and microstrip; in addition, you can now activate as many as 35 drawing files simultaneously. A utility program lets you create a preliminary mask file, which you can later convert to another format (such as GDS II or Gerber) for use by your IC manufacturing service. You can run the program on an IBM PC, PC/XT, PC/AT, or compatible computer equipped with the Intel Above-Board (or equivalent expanded memory), or on a workstation such as the Apollo Domain, HP 300 Series, or Digital Equipment's VAXstation. For the IBM PC version, prices start at $8400, depending on options.

EEsof Inc, 5795 Lindero Canyon Rd, Westlake Village, CA 91362. Phone (818) 991-7530. TLX 384809.

Circle No 429

RECTIFIER ANALYSIS

- *Predicts dc and ripple output in rectifier circuits*
- *Accommodates a wide variety of load types*

RectSim is a simulator program that runs on the IBM PC, PC/XT, PC/AT, and compatible computers and provides fast and accurate performance predictions for capacitor-input rectifier circuits. The program can simulate single-phase, half-wave circuits, full-wave bridge circuits, and symmetrical doubler circuits; it predicts dc and ripple output voltages, dc and rms currents, and power dissipation. The program can automatically run a series of simulations that sweep any specified parameters over any desired range of values. To run the program, your PC must have at least 128k bytes of RAM and MS-DOS version 2.1 or higher. $99.

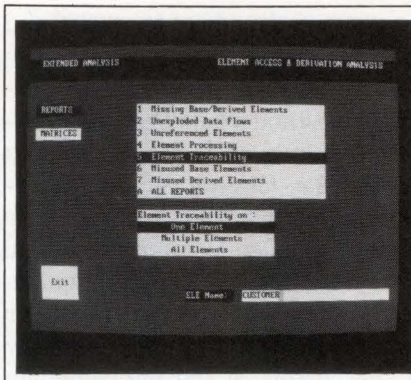
Design Automation Inc, 809 Massachusetts Ave, Lexington, MA 02173. Phone (617) 862-8998.

Circle No 430

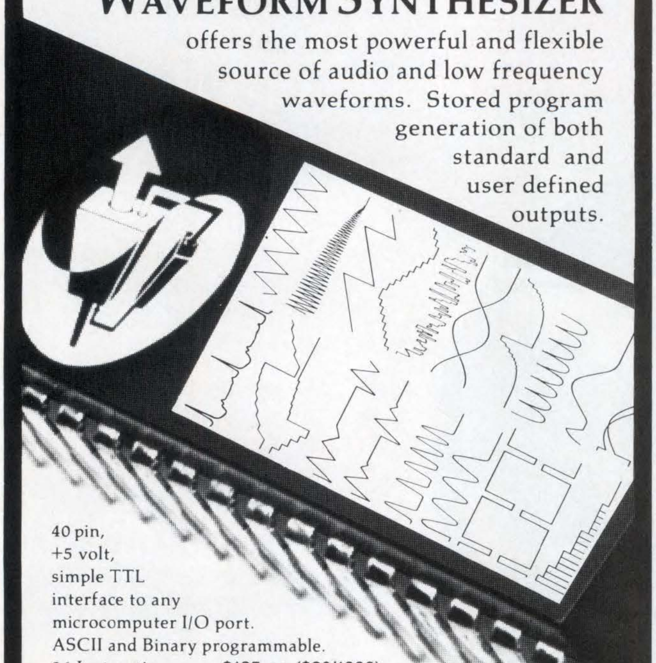
CASE ANALYSIS TOOL

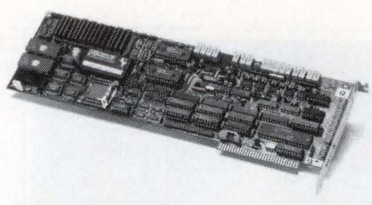
- *New features provide 33 types of analysis reports*
- *Lets you incorporate output in documents*

Excelerator is a CASE tool that runs on the IBM PC, PC/XT, PC/AT, and compatibles and the



IBM PS/2 Model 50 and Model 60. Version 1.8 contains substantial enhancements, particularly a new extended-analysis facility. This facility provides 33 types of analysis reports and 25 matrices, which help you evaluate the accuracy, completeness, consistency, and efficiency of system and database designs. The affinity-analysis feature identifies empty, incomplete, or redundant records, as well as screens and reports that have similar or equivalent contents. The data-modeling-analy-





VF Technology... The Bright Decision

Futaba, a world leading manufacturer of vacuum fluorescent displays, offers a wide assortment of *display tubes* in many sizes and formats. Also, Futaba offers *display modules* with all the electronics required to refresh the display and easily interface with the host system.

GRAPHIC DISPLAY

Both front glass phosphor, which provides maximum viewing angle and uniform surface appearance, and conventional back glass phosphor, with optimum brightness and software dimming capabilities, are available. All Futaba graphics modules offer complete drive electronics, bit mapped control with a DC/DC converter. All active components are surface mounted onto a single board.

DOT MATRIX MODULES

Utilizing Futaba's dot matrix displays, a completely intelligent line of "dot modules" is available. Each includes all drive, power supply and microprocessor components surface mounted onto a single board. Surface mounted technology results in higher reliability and allows for a smaller overall package and lower cost. All dot modules require only a 5V DC power source and can accept parallel or 8 possible serial baud rates.

GRAPHIC DISPLAYS/MODULES

Futaba Display	Futaba Module	Pixels (Row X Char.)	Brightness (FT-L)	Module Dimensions (in.)
GP1005B	GP1005B03	128X64	400	7.28X3.35X1.77
GP1006B	GP1006B04	256X64	200	9.84X3.35X1.77
GP1009B	GP1009B03	240X64	200	6.2X2.76X1.57
GP1010B	GP1010B01	176X16	200	7.32X2.16X1.70
GP1002C	GP1002C02	320X240	100*	7.10X6.30X1.60
GP1004B	GP1004B03	640X400	30	9.65X7.28X1.85

*Different Versions Available

DOT MATRIX DISPLAYS/MODULES

Futaba Display	Futaba Module	Char. X Row	Dot Format	Char. Ht. (in.)	Module Dimensions (in.)
20SD01Z	M20SD01	20X1	5X7	0.200	6.3X1.97X.75
20SD42Z	M20SD42	20X1	5X12	0.344	7.1X2.16X.88
40SD02Z	M40SD02	40X1	5X7	0.200	9.45X2.16X.88
40SD42Z	M40SD42	40X1	5X12	0.344	9.45X2.16X.88
202SD03Z	M202SD03	20X2	5X7	0.200	6.7X2.56X.90
402SD04Z	M402SD04	40X2	5X7	0.200	10.43X2.56X.90

MANY OTHER DISPLAYS — **NEW MODULES AVAILABLE SOON**

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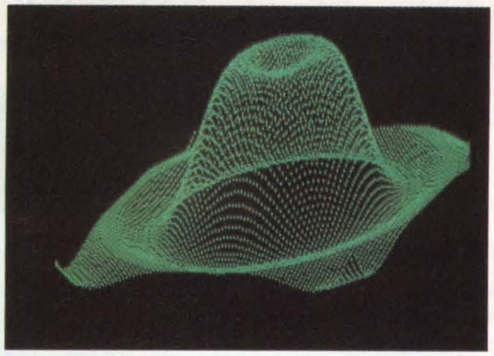
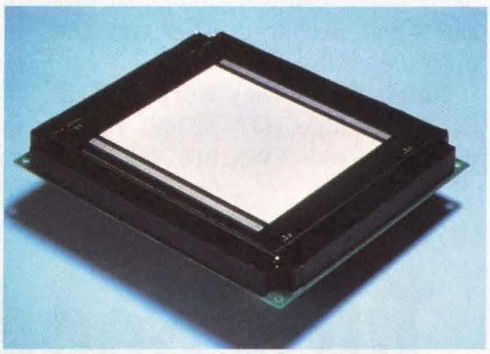
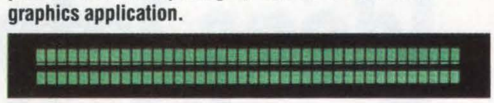
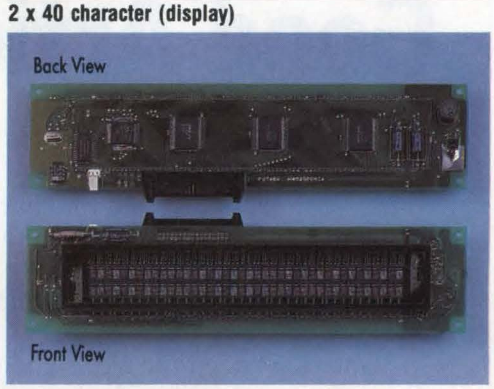




Compact, flat panel graphic displays and modules present clean, sharp images, whether for text or full graphics application.

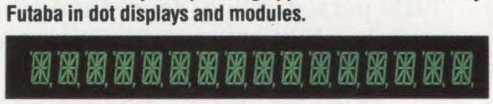


2 x 40 character (display)



2 x 40 character (module)

Pattern flexibility and pleasing appearance are offered by Futaba in dot displays and modules.



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sis feature locates records with missing, mislabeled, or multiple keys; compares connections on data-model diagrams with data relationships described in the data dictionary; and checks data-modeling normalization. The extended structure-analysis feature tracks the use of data at its lowest level to ensure that all data can be processed according to the design. Version 1.8 also lets you integrate Excelerator output with documents generated by Ventura's Desktop Publisher or printed on any laser printer that works with Adobe's PostScript command language. If you have an Excelerator and are covered by the warranty or the product-maintenance plan, you can change to version 1.8 at no charge; otherwise, the upgrade costs $500.

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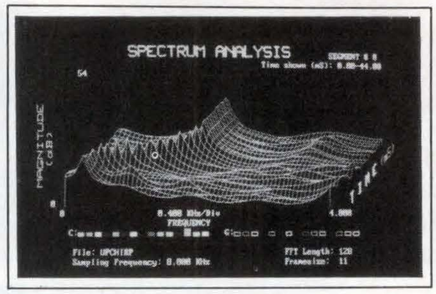

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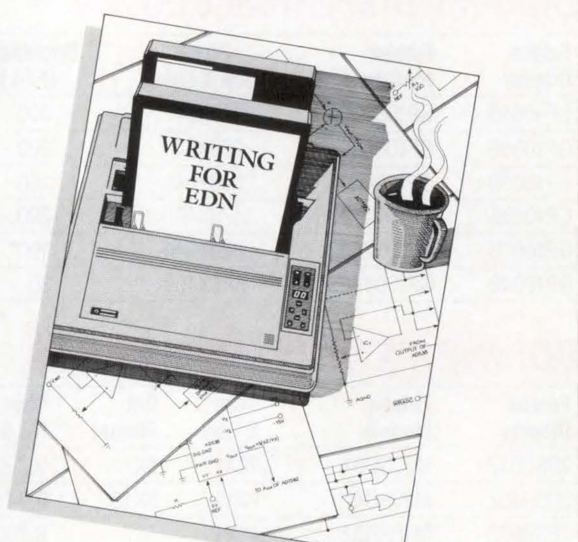

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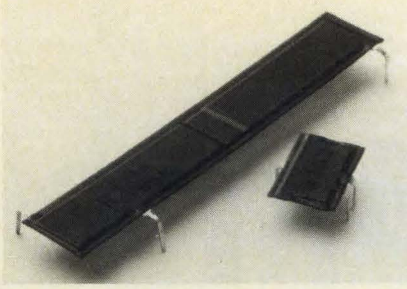

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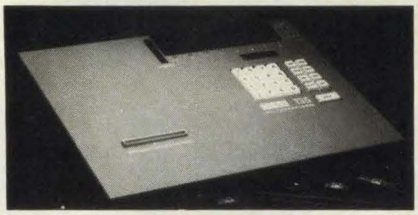

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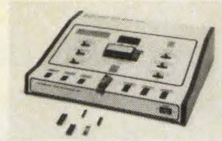

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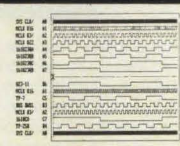

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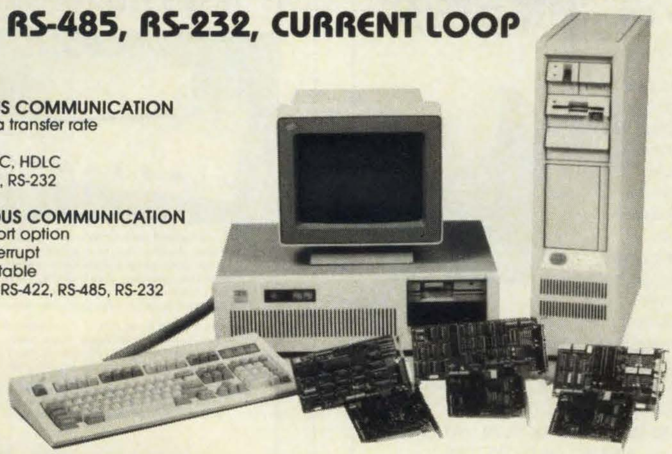

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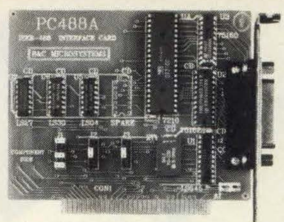

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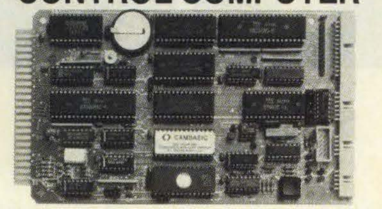

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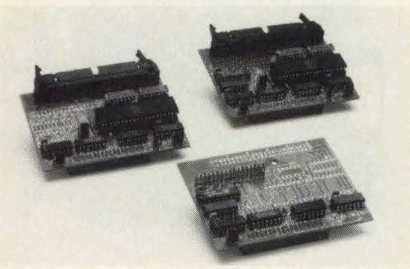

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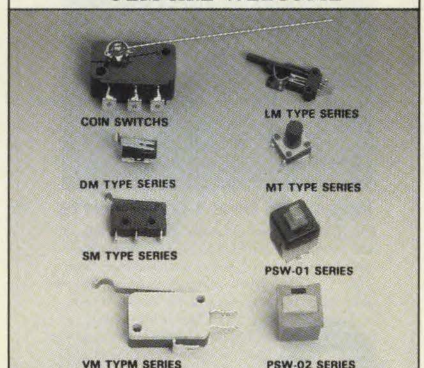

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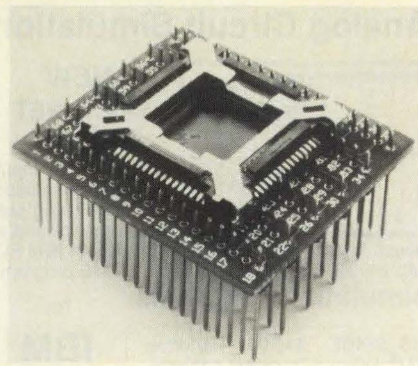

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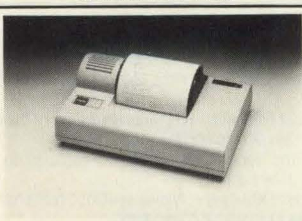

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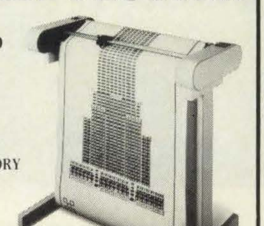

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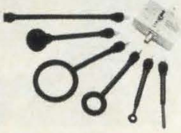

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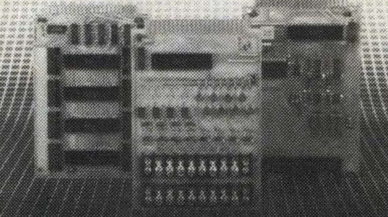

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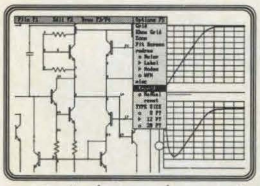

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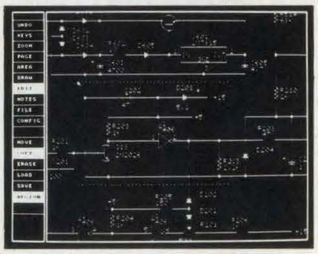

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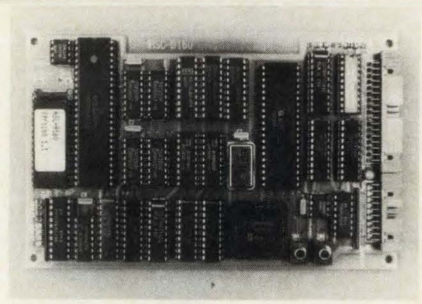

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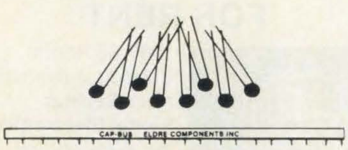

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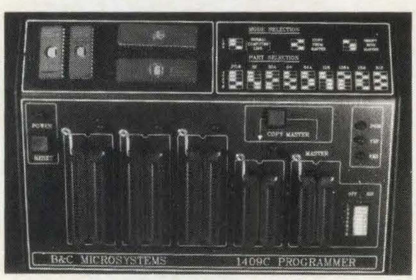

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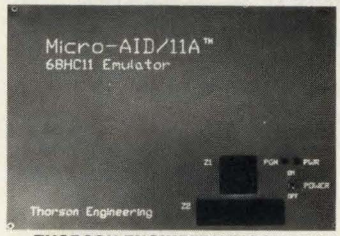

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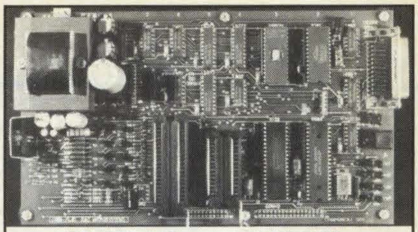

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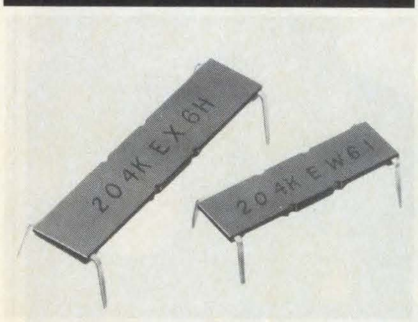

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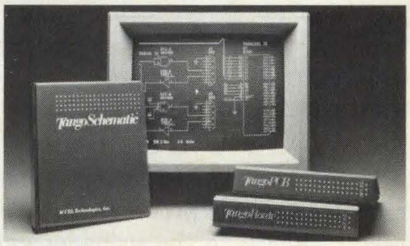

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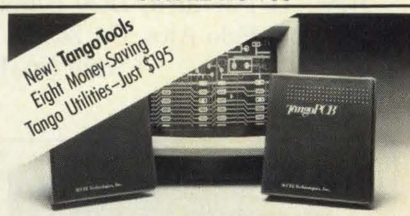

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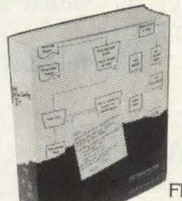

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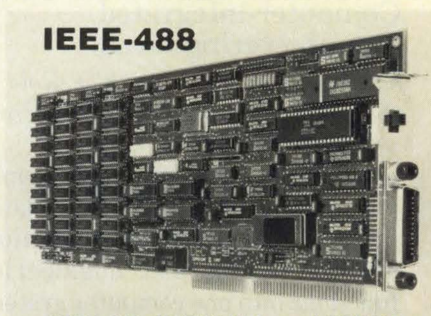

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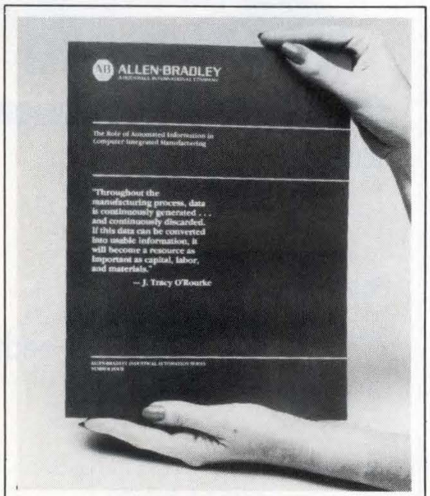
Product Note 8970B/S-2, *Applications and Operation of the HP 8970B Noise Figure Meter and HP 8970S Microwave Noise Figure Measurement System*, describes how to measure noise figure from 10 to 18,000 MHz. The publication examines the features and functions of the instruments and gives step-by-step instructions on different methods of measuring. It also serves as a general reference guide for the instruments.

Hewlett-Packard, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle No 409



Computer-integrated manufacturing ideas

The 12-pg publication, *The Role of Automated Information in Computer-Integrated Manufacturing*, presents the company's philosophy toward computer-integrated manufacturing: to unify all production, administration, and engineering functions into one computer system. The vendor's goals include improved productivity and higher quality. The brochure also presents major concepts involved in integrating management information and plant-floor information.

Allen-Bradley Response Ctr, Dept 5234, Box 92846, Rochester, NY 14692.

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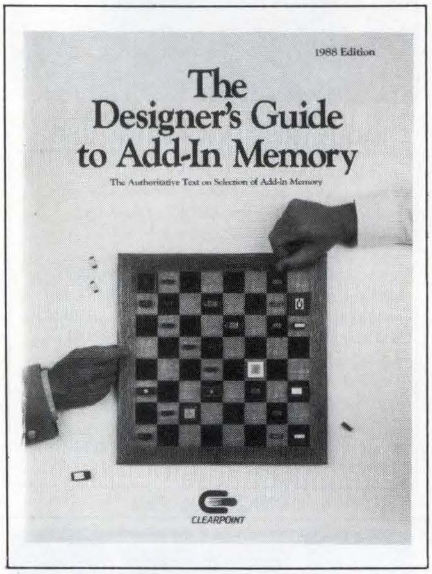

Guide to memory requirements

The 1988 Designer's Guide to Add-In Memory describes a broad range of memory products from the very technical to the management-oriented. The 80-pg catalog contains information about buses currently in use; DEC's latest offerings; where to find the best price and performance for memory products; and a survey of performance and memory options available from IBM. Also included are the features for the HP-9000 and the MIPS and number of megabytes that are available for the Sun 4/2XX and Apollo DN 4000.

Clearpoint Inc, 99 South St, Hopkinton, MA 01748.

Circle No 411

Linear/digital ASICs characterized

The 182-pg Exar/Exel Military Databook presents product specifications for military-compliant linear/digital ASICs and high-performance electrically erasable devices. It describes fabrication processes and procedures that are used to meet MIL-STD-883C. The fabrication descriptions appear in the sections on product assurance, documentation, military screening and qualification, and quality conformance inspection. Product data sheets include device features, performance characteristics, materials, drawings, and schematics. Special sections deal with custom and semicustom linear, as well as digital and linear/digital ICs.

Exel Microelectronics Inc, Box 49007, San Jose, CA 95161.

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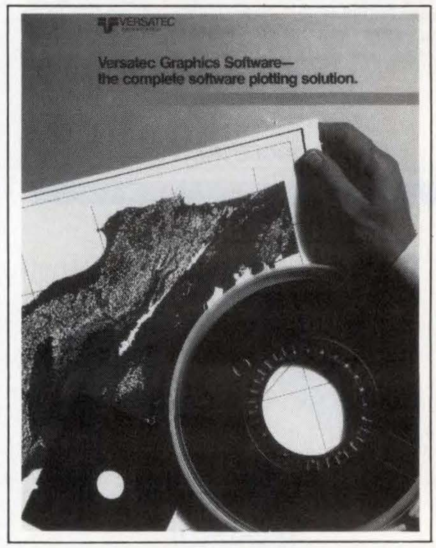

How to select the right plotting software

The booklet *Versatec Graphics Software—the complete software plotting solution* helps you choose the right software for your particular needs. It covers four types of software: Versaplot, Versaplot Random, Versaplot Random Enhanced, and a variety of plotting utility packages. The publication differentiates between each type of software and contains a listing of all available packages.

Versatec, 2710 Walsh Ave, Santa Clara, CA 95051.

Circle No 413

App note explains frequency synthesizer

Application note AN969 discusses the MC145159 phase-locked-loop frequency synthesizer, or more specifically, S/H phase detector. It explains that this phase detector is used as a fine-error signal and that the synthesizer also contains separate power-supply pins for the analog phase detector, a lock-detect output, and on-chip logic for control of the dual-modulus prescaler.

Motorola Literature Distribution Center, Box 20912, Phoenix, AZ 85036.

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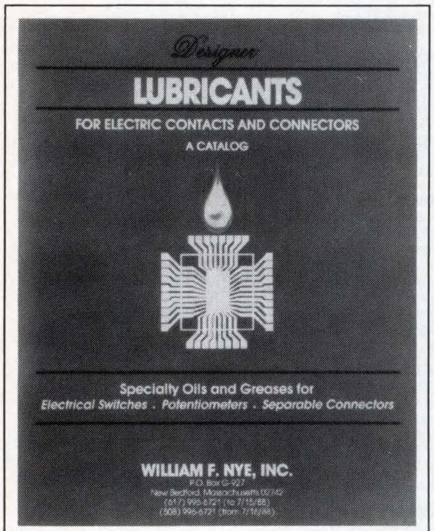

Catalog of lubricants

Lubricants for Electric Contacts and Connectors is the vendor's catalog of specialty oils and greases. It covers four application areas: greases for sliding electric contacts, as in electric switches; oils for sliding contacts and potentiometers; potentiometer greases; and lubricants for stationary separable electric connectors. It describes lubricant properties and operating-temperature ranges and discusses lubricants you can use to help suppress arcing conditions.

William F Nye Inc, Box G-927, New Bedford, MA 02742.

Circle No 415

Software package presented

This 2-pg data sheet focuses on the functions of the Com 2 software driver that provides control of the vendor's logic programmers. It features sections on auto-recall of preset parameters, color-enhanced displays, the main menu's device program sequence, and error statistics. It also explains the system requirements and provides a list of devices that the vendor's logic-programmer family supports. Color illustrations and a diagram of the package complete the publication.

Stag Microsystems Inc, 1600 Wyatt Dr, Santa Clara, CA 95054.

Circle No 416

DSP products categorized

The vendor's *1987 DSP Products Databook* includes four categories of DSP products: DSP μPs, microcoded support components, floating-point components, and fixed-point components. It also contains package information, application notes, and an appendix, which includes an ordering guide and a worldwide service directory. A guide to finding product data is provided inside the front cover. Numerous diagrams, tables, schematics, and listings complete the volume.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021.

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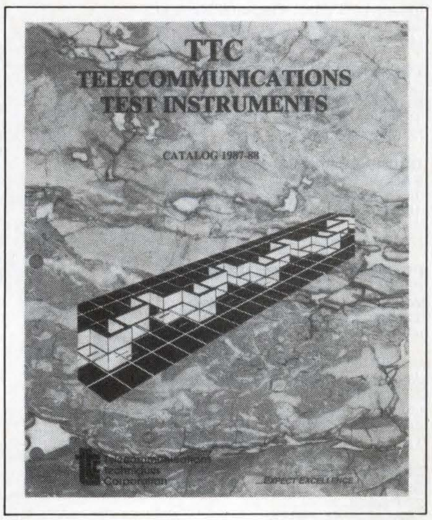

Test instruments described

The *TTC Telecommunications Test Instruments* catalog provides information about the vendor's products, their applications, accessories, key features, mainframe options, and specifications. The featured product lines include Fireberd and Data Sentry 10 data-communication analyzers, Model 124 drop and insert for T networks, and T-Berd T-carrier instruments, which analyze and monitor digital data-communication links, digital-communications simulators, and breakout boxes. Photographs and charts highlight the text.

Telecommunications Techniques Corp, 444 N Frederick Ave, Gaithersburg, MD 20877.

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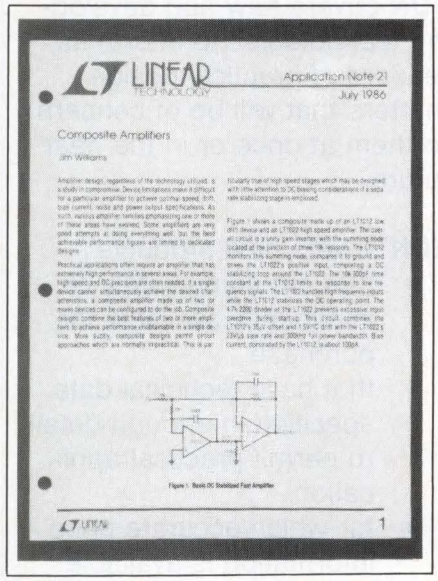

Discussion of composite amplifiers

The 12-pg application note *AN21: Composite Amplifiers* discusses the compromises you must make in order to achieve optimal speed, drift, bias current, and noise and power output from an amplifier. It provides schematics and descriptions of composite amplifiers, which are suggested as alternatives to simple amplifiers. It describes several applications including a wideband FET input-stabilized buffer; a gain-trimmable wideband FET amplifier; a fast, stabilized noninverting amplifier; and a stabilized, ultra-wideband amplifier with a slew rate exceeding 3000V/μsec.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

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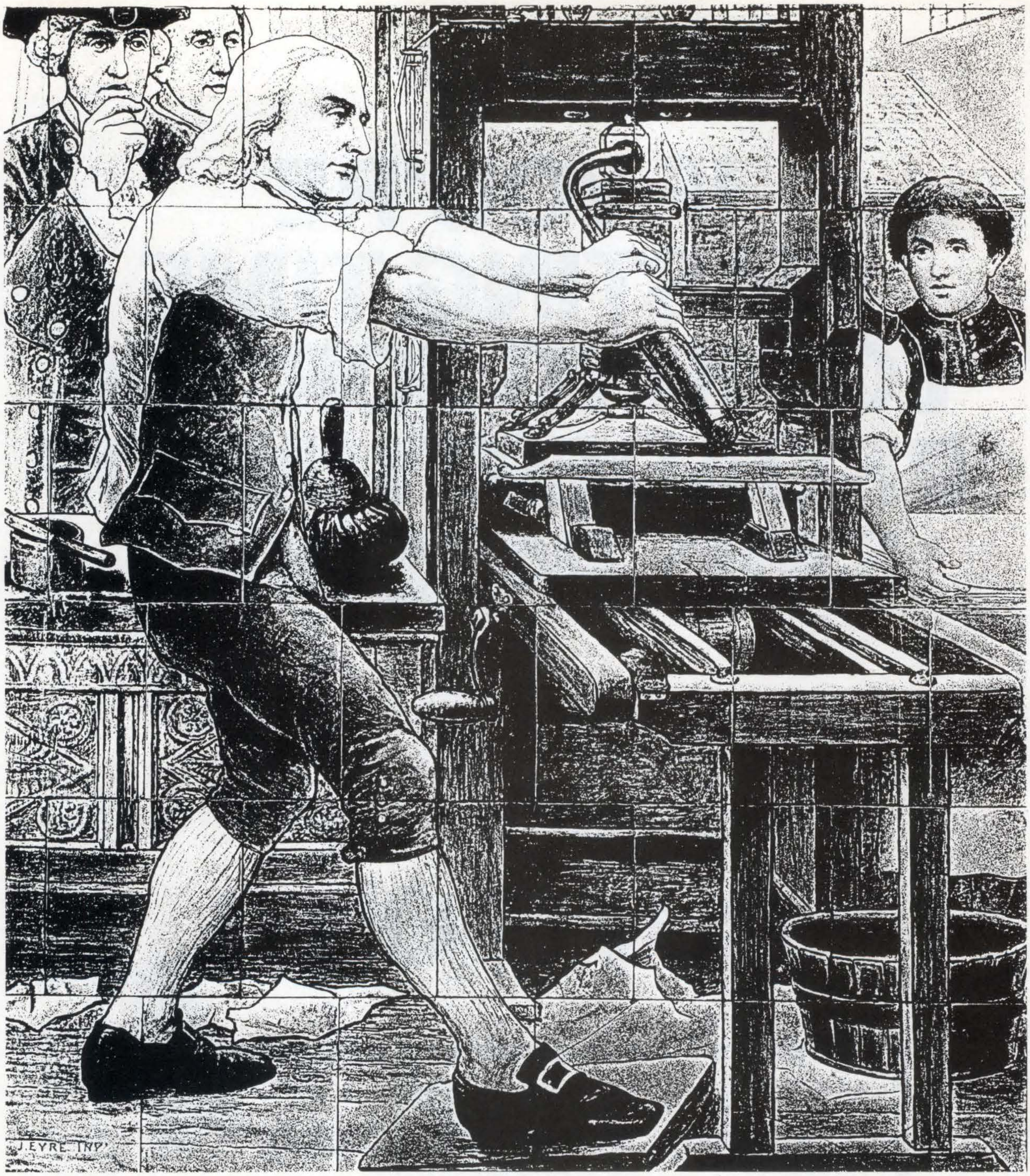

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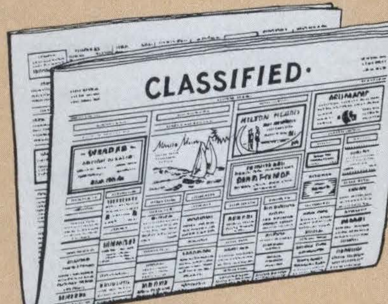

Let The Job Hunter BEWARE

Deborah Asbrand, *Associate Editor*

Placement agencies' opportunities always sound so attractive. Their large recruiting advertisements in the Sunday editions of most newspapers list dozens of high-salaried jobs in many industries. Some recruiters, using more personalized tactics, place phone calls or write letters to individuals to inform them of job openings that might interest them. And, best of all, the only thing you have to do in order to plug into this network of job opportunities is send in a resume.

The system seems almost too good to be true, and, in most cases, it is. Recruiters do indeed have access to unadvertised job openings, and an individual represented by a reputable agency can benefit from inside contacts. Job counselors, though, advise that recruiters handle only a small portion of available positions, and that anyone considering working with an agency should be aware that association with a disreputable firm could harm his or her career.

The two most common forms of placement service are search firms and employment agencies. Their methods of operation are different, but both types of business receive their commissions from the hiring company—which means that their primary allegiance is to the company, not to the job seeker.

Placement's elite

Search firms constitute the upper crust of the placement industry. Companies generally hire search firms to fill jobs that command salaries of $50,000 or more. Searchers are the true "headhunters": On receiving an assignment, they research their client's industry to identify the leading companies and then target talented employees who might be interested in the client company's job opening.

Search firms say that in their business, discretion is the name of the game. Their clients hire them to conduct judicious, thorough searches. To preserve their industry's sense of propriety, most search firms maintain low profiles and rarely advertise their services. Most politely decline to accept unsolicited resumes. As Jennifer Munro, president of a Greenville, SC, search firm, explains, "Search firms are not for people who are looking for jobs."

The search-industry's particular etiquette is reflected in its trade jargon. Searchers don't "place" people, they "complete searches." And the searchers themselves aren't recruiters, they're "consultants."

Searchers, who get a fee equal to 30% or more of the open position's salary, roll out the red carpet for clients. Munro's business, Consultants for Corporate Management, includes a researcher, recruiter, and reference checker on its five-member staff. The company spends seven to 10 days researching a job opening, gathering information on the industry involved, and compiling the names of at least 350 candidates before it begins placing phone calls. After reducing the number of candidates to five or six front-runners, Munro meets with each, sometimes traveling cross-country to do so; she then presents her client with the finalists.

Electronics companies typically hire search firms to fill managerial positions such as director of engineering, director of research and development, or vice president of engineering. But they also carry out searches for hard-to-fill engineering specialties. Munro, for example, recently filled a $60,000 slot for a supervisor of ruby- and sapphire-crystal growing.

Search firms take great pains to distinguish themselves from their distant relative, the employment agency. Most employment agencies work on a contingency basis—that

A search firm or contingency agency receives its commission from the hiring company—which means that it's working for the company, not for the job seeker.

is, they don't receive their commission unless the company hires a candidate they've submitted.

Mercurial and competitive

In contrast to the refined, low-key search industry, the contingency-agency business is mercurial and competitive. It's also booming, having grown 30% between 1982 and 1984. As a result, an estimated 18,000 agencies now elbow for the attention of both job seekers and employers.

Most states require agencies to be licensed or registered, but do not otherwise regulate or supervise them. The low overhead required to set up an agency—and the appeal of commissions that average 20% of a position's annual salary—attracts many newcomers to the field each year. "There are a lot of guys working out of the trunks of their cars," says Carl Tomforde, a recruiter with the Littleton Group, a Littleton, MA, contingency firm. Tomforde adds that a one-person shop doesn't necessarily imply a fly-by-night business. "Some [recruiters] work out of their homes, and they probably do a fine job. They can hand-pick their candidates and can really give them the attention that they're looking for."

Unlike search firms, most contingency agencies are volume businesses. Because an agency doesn't receive a commission unless it comes up with a winning candidate, it's in the agency's best interest to forward as many resumes as possible, increasing the odds that one of the resumes will interest a company and result in a hire.

A tarnished reputation

Not surprisingly, the cutthroat business practices that stem from employment agencies' constant vying for attention have accorded the placement industry a reputation on a par with used-car sales. Two professional associations that seek to promote a positive image are the

Guidelines for choosing an employment agency

- Check out an agency's reputation just as you would evaluate any other business whose services you engage. Ask your friends about agencies they've used or with which they're familiar.
- Most states require employment agencies to be licensed or registered. Call your state's labor office and ask whether any complaints have been filed against any agencies that you're considering approaching.
- Ask about the agency's professional affiliations. Is it a member of the NAPC? Have any of its recruiters been designated Certified Placement Counselors by the NAPC? The NAPC lists its members geographically and by specialty in the *Career Guide Handbook* ($19.95). For more information, write to the NAPC at 1432 Duke St, Alexandria, VA 22314 or phone (703) 684-0180.

National Association of Personnel Consultants (NAPC) and National Personnel Associates (NPA), both of which require members to adhere to ethical standards. NPA's occasional expulsion of a member, however, indicates the skewed nature of industry morality: The organization most often banishes members not for substandard behavior toward a client company or job hunter, but for infractions against another agency.

Despite the bad will created by unethical agents, contingency agencies can serve job hunters as yet another avenue to new employment. The NAPC estimates that its 2000 members place 50,000 individuals in jobs each year.

A bad rap

Career counselors attribute some of employment agencies' image problems to job hunters' misperceptions. "In all fairness to the agencies, lots of people go to their offices thinking 'here's a person who'll find me a job'—an erroneous expectation," says Libby Pannwitt, vice president at Mulford Moreland & Associates, a Cupertino, CA, outplacement firm. "The agency's main job is to fill job openings, not to help the job seeker."

In contrast to the refined, low-key conduct of the search industry, the contingency-agency business is mercurial and competitive.

Other counselors advise people not to rely on agencies when looking for a job. "Agencies handle 10 to 15% of available jobs, and that's about the percentage of job-hunting time that the job hunter should devote to them," says Ron Wade, a career-management counselor for Career Directions (Needham, MA.)

Failure to thoroughly check out an agency can ultimately hurt a job hunter's reputation. Some agencies, for example, engage in mass mailing, sending out as many as 200 copies of an individual's resume. Such an inundation of the market makes it nearly impossible for a job hunter to keep track of his resume's whereabouts. It also makes it that much easier for word of a job-hunter's search to enter the rumor mill and find its way back to his or her employer.

Recruiter Carl Tomforde also counsels job hunters to keep a tight rein on an agency's activities and to avoid viewing an agency as a job-hunt panacea. "My advice to candidates who call is to continue doing their own legwork and their own networking." **EDN**

Article Interest Quotient
(Circle One)
High 500 Medium 501 Low 502

What to look for in the agency you choose

- Visit the agency to meet with one of its recruiters and to see its operations. Be suspicious of agencies that don't ask you to come in for an interview.
- Find out how your resume will be presented to prospective employers.

  Find out whether the agency sends out copies of the resume you submit, or whether it formats your resume in a distinct agency style. Some agencies redo your resume, whereas others merely label your resume with a sticker that lists their name and contact information. Know whether your resume reflects you or the agency that you've sent it to.
- Ask to examine any documentation about you that the company plans to send out.

  Know how the agency presents you—and itself—to potential employers. Does it include a cover letter with the resumes it sends? Will your resume be mailed individually, or will the agency merely include your resume in a stack of others destined for the same company?
- Ask for the names of the companies to which your resume is being sent.

  When looking for a job, discretion is the watchword. Many agencies conduct mass mailings, sometimes sending an applicant's resume to as many as 200 companies. They claim that mass mailings offer job candidates broad exposure. Ask the company how it decides which companies it will send your resume to. Exercise quality control and ask to see those companies' names.

CAREER OPPORTUNITIES

1988 Editorial Calendar and Planning Guide

EDN

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
Jan. 7	Dec. 14	Computers & Software, Communications ICs	Closing: Dec. 21 Mailing: Jan. 14
Jan. 21	Dec. 30	Microprocessors, Software, Components	
Feb. 4	Jan. 14	Semicustom ICs, Computors & Peripherals	Closing: Jan. 21 Mailing: Feb. 11
Feb. 18	Jan. 28	Materials & Hardware, CAE, Power Sources	
Mar. 3	Feb. 11	Communications, CAE, High-Speed Logic	Closing: Mar. 3 Mailing: Mar. 24
Mar. 17	Feb. 25	Graphics, Filters, Software/CAE	
Mar. 31	Mar. 10	Power Semiconductors, Memory/Graphics, Fiber Optics	
Apr. 14	Mar. 23	Communication Technology Special Issue, Communication Systems	Closing: Mar. 31 Mailing: Apr. 21
Apr. 28	Apr. 7	Software, Industrial Computers, Interface ICs	
May 12	Apr. 21	Analog Technology Special Issue, Analog Converters	Closing: Apr. 28 Mailing: May 19
May 26	May 5	CAE, Software, Sensors/Transducers	
June 9	May 19	CAE, Analog ICs, Test & Measurement	Closing: May 29 Mailing: June 16
June 23	June 2	Data Communications, DSP, Components	
July 7	June 14	Product Showcase—Vol. I, Power Sources, Software	Closing: June 23 Mailing: July 14
July 21	June 30	Product Showcase—Vol. II, CAE, Test & Measurement	

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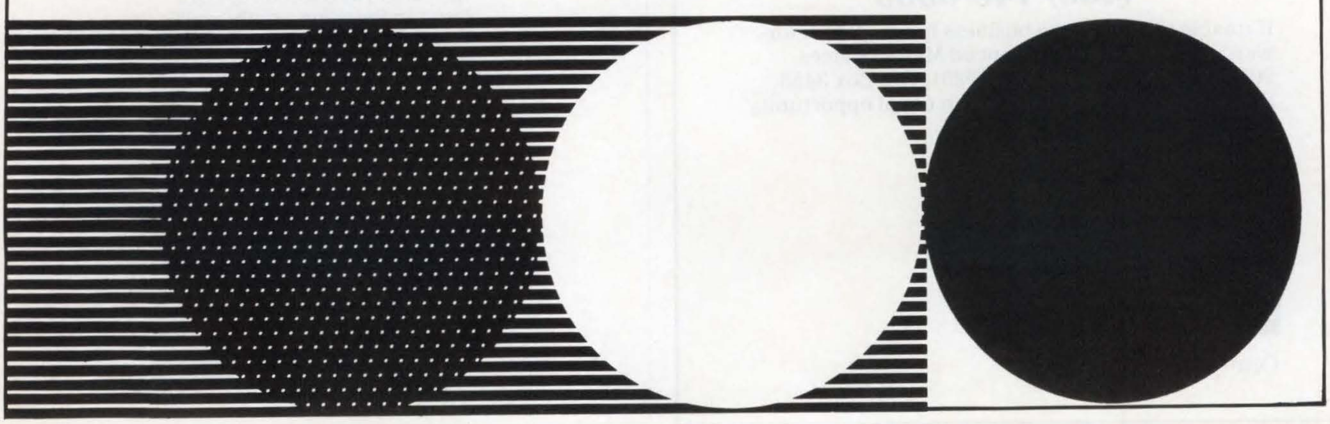

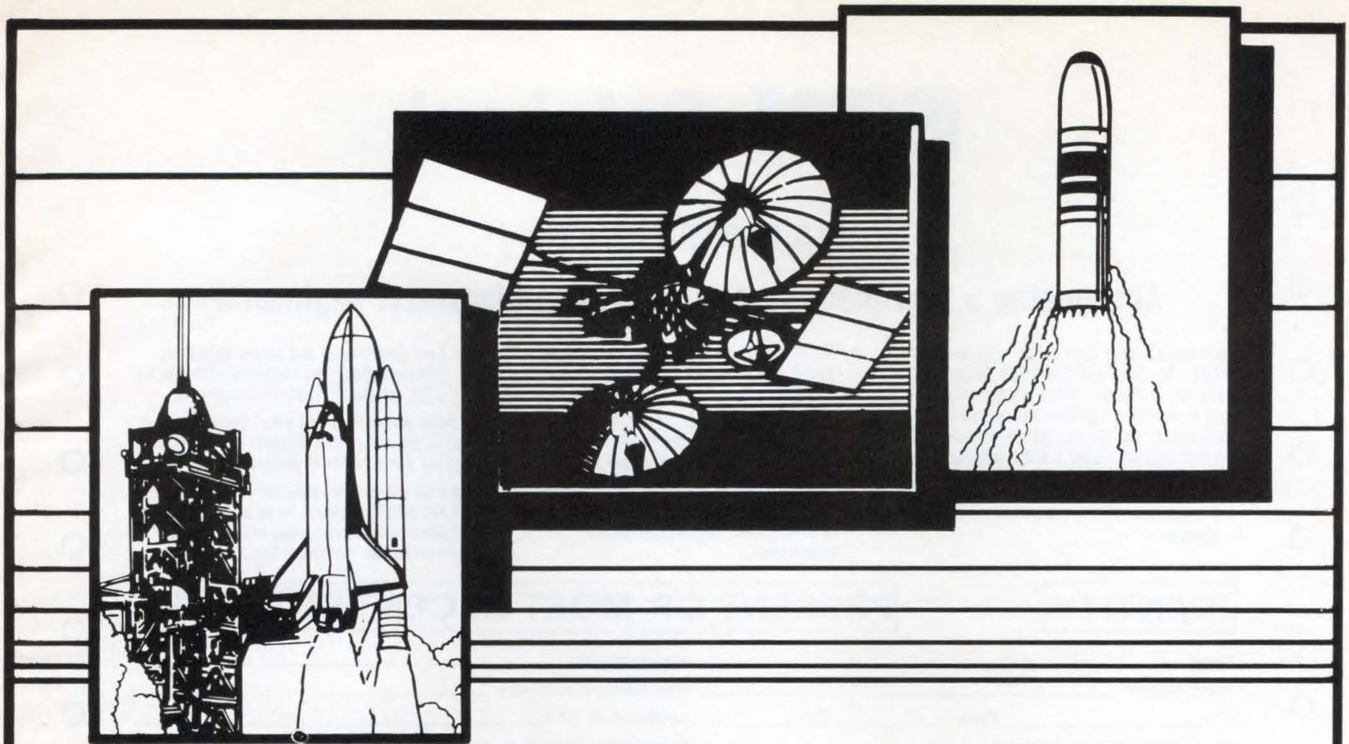

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LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG

Fax machines should see 25%/annum growth through 1991

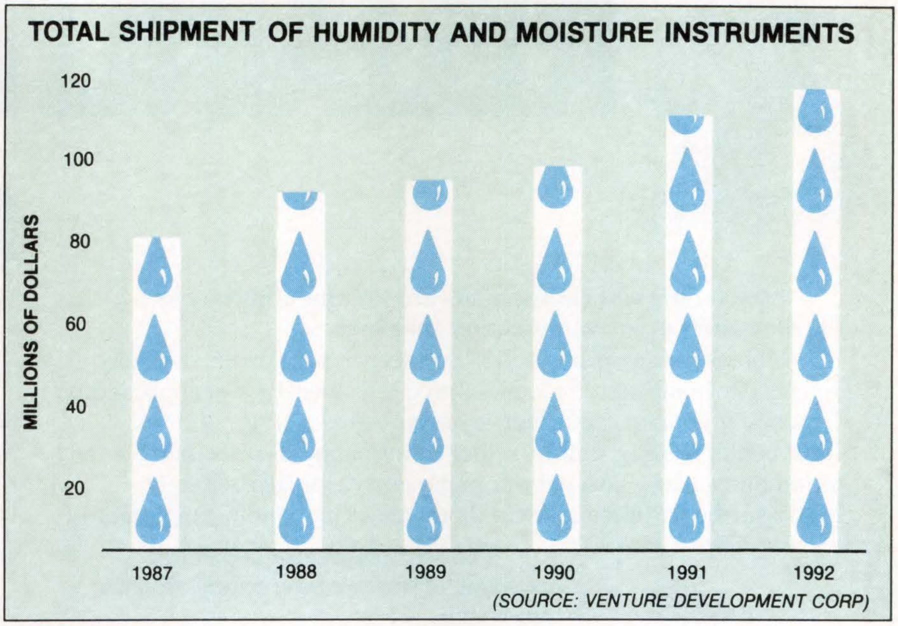
Speed, low cost, and ease of use—all of these advantages will combine to push US shipments of electronic facsimile machines to the 1,000,000 mark in the very near future, according to CAP International Inc of Marshfield, MA. CAP maintains that fax equipment is becoming as common in the office as are copiers and phone systems. Indeed, facsimile machines now present a reasonable alternative to overnight delivery systems. In 1987 alone, facsimile systems achieved an estimated 90% increase in shipments over the 1986 rate. From 1987 to 1991, the US market should experience a compounded annual growth rate of 25%.

Network providers will benefit from related opportunities. Mirroring moves by voice-system and data-telecommunications-system vendors, network vendors will begin to offer enhancements and options to their services, such as store functions and forward-messaging capacity. Within the next five to 10 years, CAP expects network providers to find high-volume applications that will use both stand-alone facsimile machines and computer-based image transmitters.

US FAX MARKET: 1986 TO 1991

	1986	1987	1988	1989	1990	1991
YEARLY REVENUE OF BOTH FAX BOARDS AND STAND-ALONE MACHINES	\$712M	\$1093M	\$1361M	\$1542M	\$1675M	\$1723M
SHIPMENTS OF FAX BOARDS	2500	11,500	33,070	70,250	151,000	227,500
SHIPMENTS OF STAND-ALONE MACHINES	191,000	365,000	490,000	605,000	655,000	715,000

(SOURCE: CAP INTERNATIONAL INC)



Humidity/moisture devices to gross $113.9M by 1992

Within the next few years, new technologies and improvements in old ones will substantially increase the market for instruments that measure humidity and moisture, according to a Venture Development Corp (Natick, MA) study. In 1987, the market for such instruments was about \$80.7 million; by 1992, the total number of units shipped will represent \$113.9 million in sales, reflecting a 7% projected annual growth rate.

Annual unit shipments will increase minimally throughout the forecast period, averaging just 2.9% through 1992. But revenue will grow more rapidly because, as technology improves and the use of electronic components increases, the selling price of each kind of instrument will rise proportionally.

The critical issue will be the replacement of organically based relative-humidity measurement devices with measurement devices of more sophisticated design. Despite numerous humidity-measurement applications in various products, processes, and environments, humidity remains one of the most difficult environmental conditions to measure. A great many potential users have expressed dissatisfaction with the limitations of organically based instruments and the contamination and calibration-drift problems that advanced devices currently pose.

As more sophisticated products become available, this group of potential users will prove an important source of sales for vendors—as will a second group composed of those who have yet to appreciate the cost advantages, reliability, and accuracy of these instruments.

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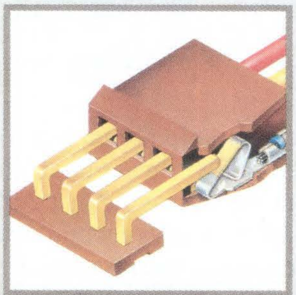

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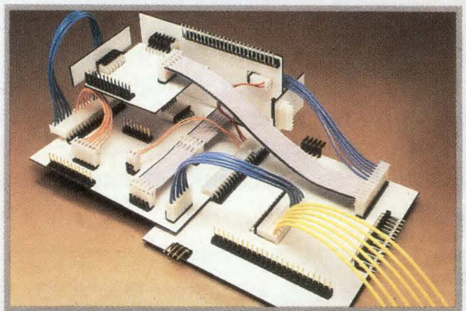

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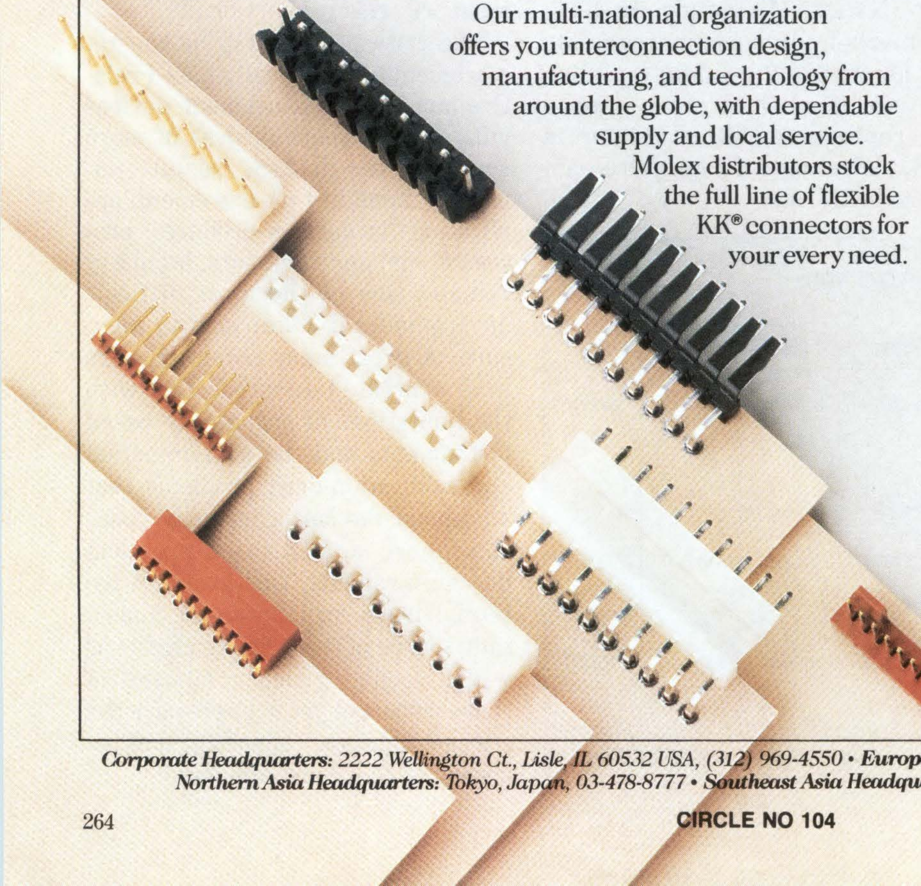

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