A MORGAN-GRAMPIAN PUBLICATION

DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS AUGUST 1985

- DSP FINDS SINGLE-CHIP SOLUTIONS
- VLSI BOOSTS GRAPHICS BOARDS PERFORMANCE
- ADA AND MODULA-2 CHALLENGE C AND PASCAL

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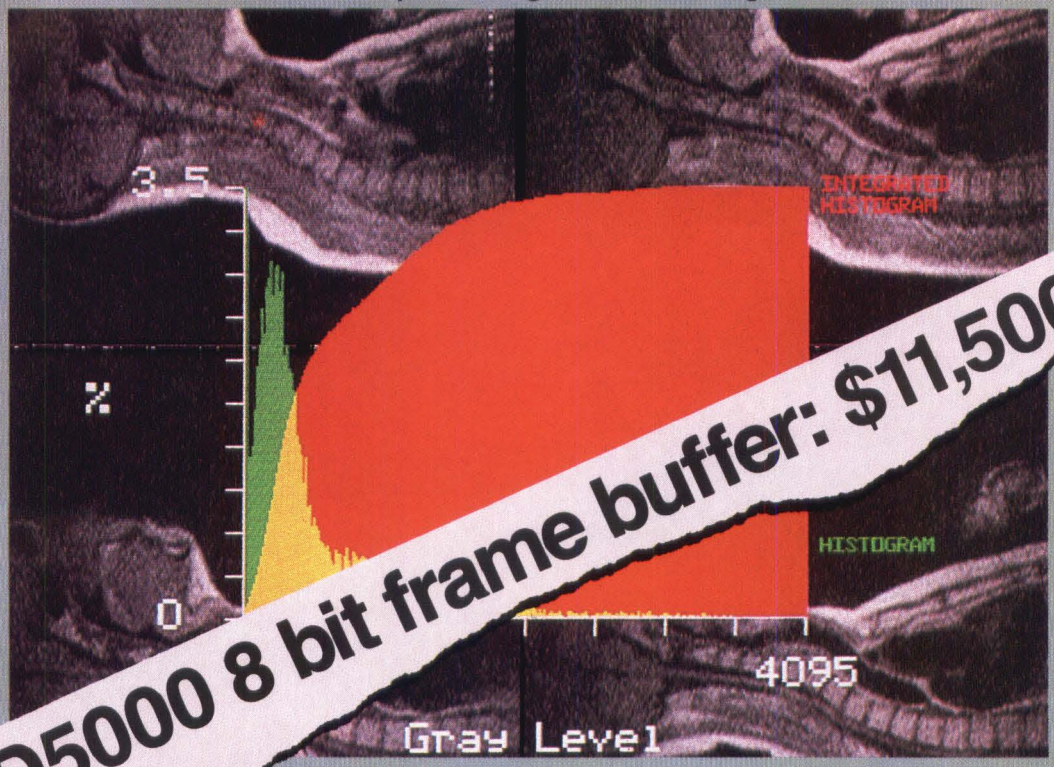
Gould...Innovation and Quality in Image Processing.



FD5000 8 bit frame buffer: $11,500.

Histogram of 12 bit magnetic resonance medical image with four (4) bit color overlay. Courtesy of Mallinckrodt, Institute of Radiology.

Gould's FD5000 Image Processor Introduces a Whole New Idea:

Performance *and* Economy.

An image processor can be expensive.

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Flexible Architecture:
Two 12 bit deep images or three 8 bit images with 4 bits of color or monochrome overlay provide monochrome, pseudocolor, and true color.

60Hz Flicker-Free Display:
Bright, flicker-free image display at 60Hz; 30Hz for image processing and real time input.

Feedback Processor:
Five times faster than host-based operations for convolutions, digital filtering, interactive math, regions of interest, and recursive filtering.

1024^2 x 32 Bit Memory Arrays:
Optional memory configuration provides user choice of image size and processing precision to display through 512^2 viewport.

MINI-LIPS Image Processing Software:
Interactive keyboard control; prompts for filters, real-time math, Look-Up Tables, histograms, geometric operations, utilities, and image storage; demo programs include source code.

The Closer Look:
The FD5000 will minimize the load on your host CPU and your processing staff. Peripheral or stand alone configurations are available.

Give Us A Call:
We'll be happy to discuss your application needs and the FD5000 at your convenience.

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Circle 6

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Our new IVG-128, for example, instantly turns any IBM PC into an economical, multi-feature image processing system.

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While our VG-128 for the Multibus and iLBX bus provides on-board arbitration logic for fast video data transfers between two host CPUs.

Each 128 Family board provides reliable, real-time digital video for machine vision inspection, teleconferencing, medical imaging, surveillance, and many other applications.

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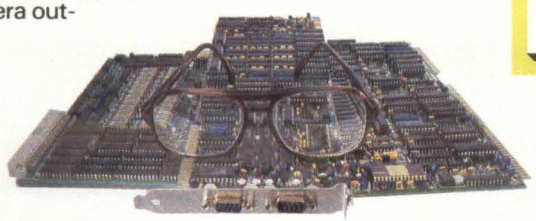

Circle 4

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with VMEbus
ultibus II

Sorry, Intel.
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Critical decisions for the likes of next-generation factory and office automation systems couldn't wait for the arrival of what would turn out to be merely a much-patched, already-dead-end bus structure.

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BUS COMPARISON

	ISSUE	VMEsystem	MULTIBUS® II	COMMENTARY
Commercial Issues	**Specification Quality, Stability, Standardization**	VMEbus spec available since 1981. Rev. C is a standard of clarity for the industry, very stable, and available now. VMXbus Rev. B available now; VMSbus completely specified, with Rev. B available in July '85. IEEE P1014 and IEC 47B committees have completed their work. Final approval expected later this year. VMXbus and VMSbus have been proposed to the IEC for standardization.	Various bus specifications available in draft form since late 1983. Complete draft has *never* been published for serial bus, iSSB™. IEEE Committee began work on Multibus® II in 1984. No known submission yet to IEC.	VMEbus IEEE activity represents the *first time* that the IEEE requested a committee be formed to standardize a microcomputer bus structure.
	Proprietary Constraints	None!	*Intel trademarks:* iLBX, iPSB, iSBX, iSSB, Multibus®, Multichannel *Intel patents:* pending on Multibus® II *Copyrights:* entire Multibus® II spec document *Licensing:* by Intel, with fee required.	VMEsystem *totally free* of patent, trademark, copyright, and trade secret restrictions. It is truly an open system, with unimpeded public access.
	Number of Vendors and Compatible Products	Over 150 announced VME vendors with over 700 compatible products, encompassing boards, systems, packaging, and software.	Less than 10 vendors with announced products. Intel is the only *major* vendor with board-level products. (Three Intel board designs announced.)	VMEbus supported worldwide by Motorola, Mostek, Signetics/Philips, Thomson, Plessey, and many, many others. AT&T has selected VMEbus for its first line of board-level products.
Technical Issues	**Bus Timing**	All VMEsystem buses are asynchronous, except for VMSbus (which by its very nature must be synchronous). Asynchronous timing allows bus performance improvements as chip technology improves.	iPSB™ is *synchronous*, fixed at 10 MHz clock. Performance cannot be improved without increasing this clock rate, instantly obsoleting all pre-existing product.	VMEsystem architecture allows smooth growth as technology improves. Today's technology *exceeds* 10 MHz clock of Multibus® II. (E.g., 12.5 MHz and 16.0 MHz parts in M68000 Family.)
	Interrupt Protocol	VMEbus interrupt handling may be either *centralized or distributed*. Direct interrupts are provided to handle on up to 7 prioritized levels, with location monitors allowing any number of virtual interrupts.	iPSB™ interrupt latency is unbounded, and no priority override is allowed.	VMEbus interrupt protocol provides much greater flexibility and performance and is better suited for real-time applications.
	Multiplexing	Completely non-multiplexed VMEbus address and data lines, along with separate address and data strobes, allow data transfer rates in single transfers to approach block transfer rates. This also supports performance improvements with address pipelining features of modern processors.	iPSB™ single cycle data transfer rate is only half that of block transfer rate, since address and data lines multiplexed. Address pipelining not supported.	Clear performance advantage for VMEbus.
	Serial Bus Protocol	• Sender Self-Check for VMSbus • Collision-Tolerant	• CRC ERROR checking • CSMA/CD protocol. (Complete iSSB™ specification has *never* been published.)	VMSbus message rate stabilizes under heavy usage. CSMA/CD *declines* under heavy usage.
	Bus Support Chips	Nine defined, six presently available, with samples for additional three in 3Q 85. Presently sole-sourced from either Motorola or Signetics/Philips (depending on chip).	iPSB™ design *requires* LSI support. Two chips presently defined, sole-sourced from Japanese vendor. The chip implementing the complex message-passing protocol is not yet available.	VMEsystem is far ahead with available support LSI.

Available products comparison.
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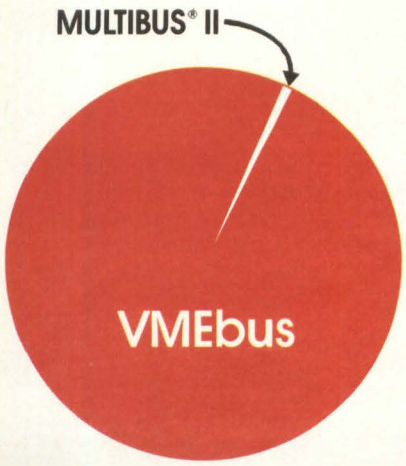

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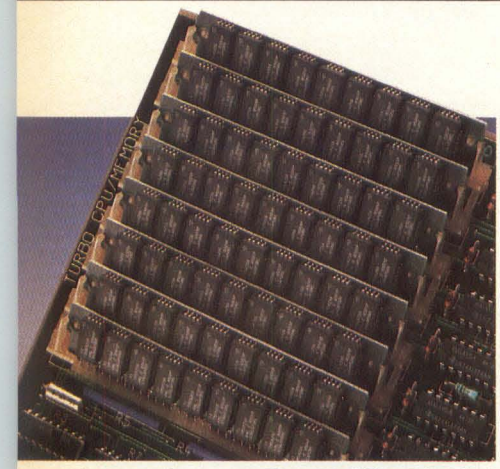

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ON THE COVER

Systems once demanding 50 to 100 ICs can now be implemented on a single chip with standard cell technology. Many semiconductor vendors are introducing 2-micron CMOS libraries that provide 20 to 50 MHz system frequencies. As a result, standard cell technology meets both the performance and functionality requirements of many applications. Developed by WaferScale Integration, the cover illustrates the numerous VLSI functions in the firm's cell library.

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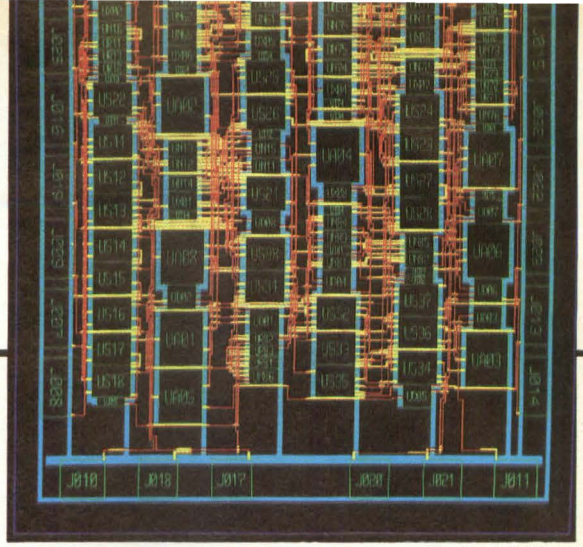
VLSI functions together with analog cells yield single chip systems.



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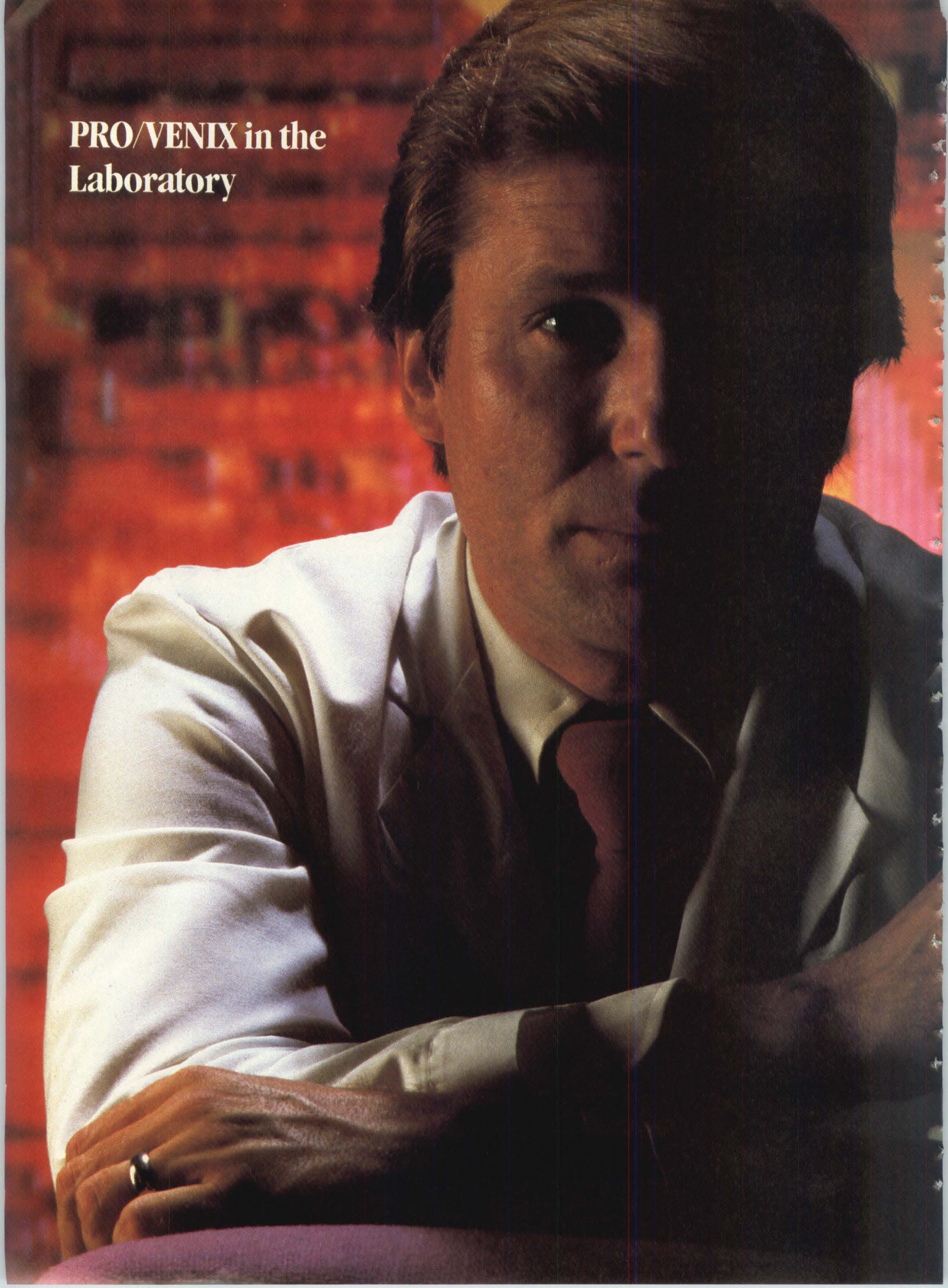
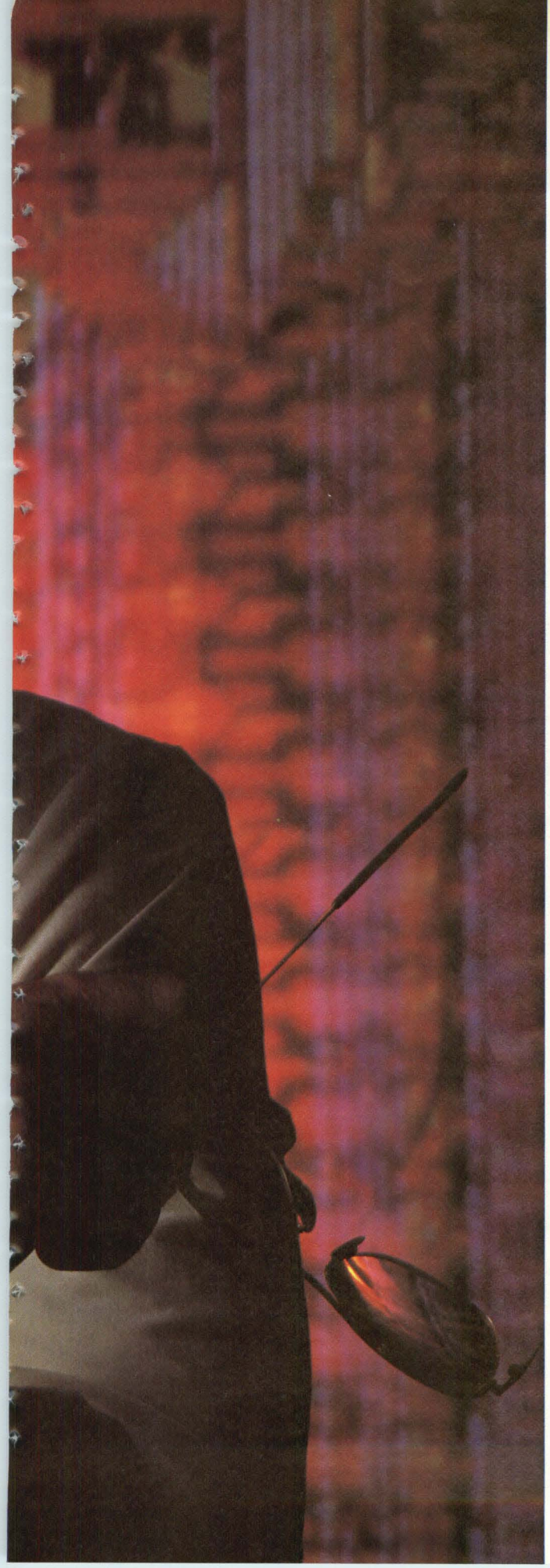

PRO/VENIX in the
Laboratory



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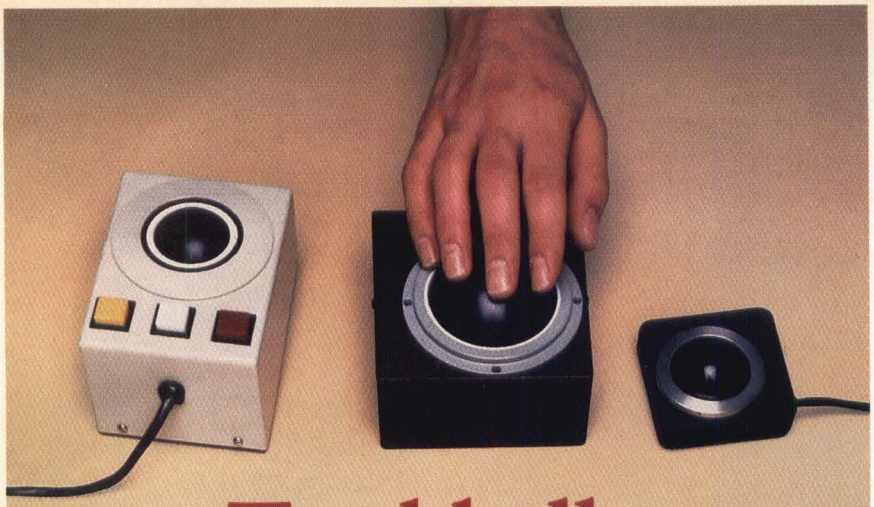

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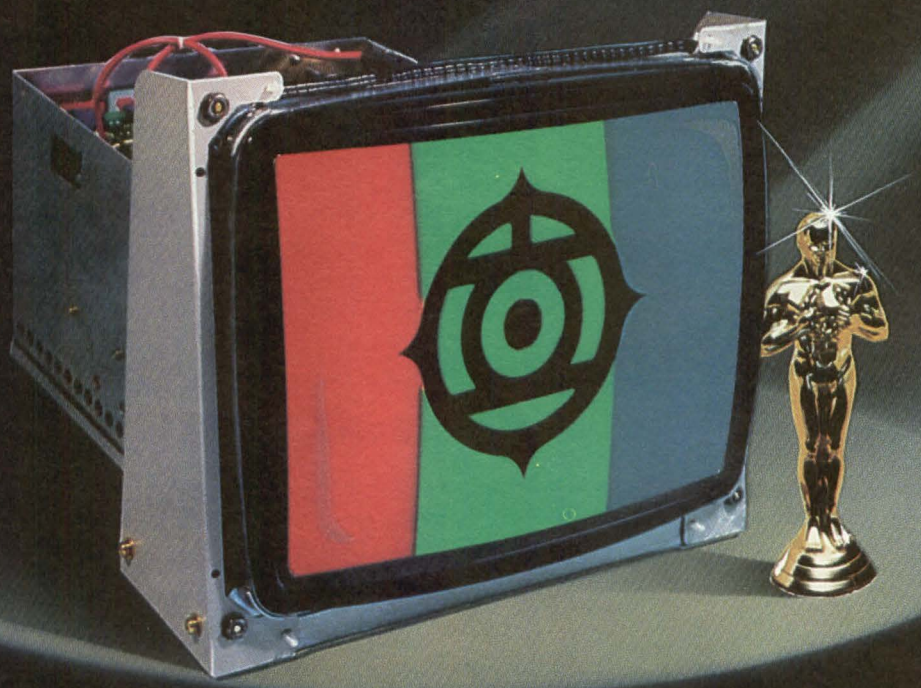

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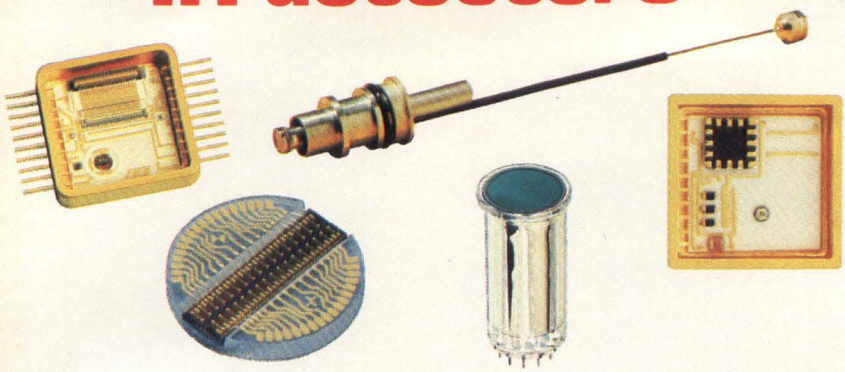

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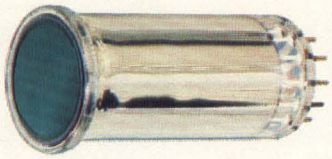

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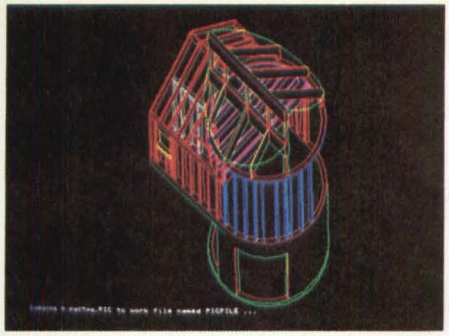
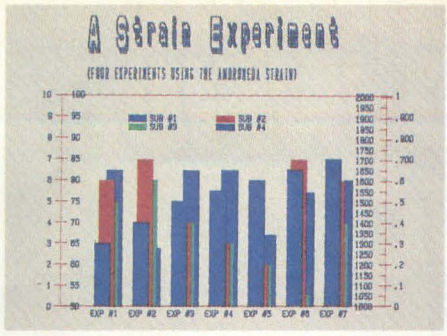
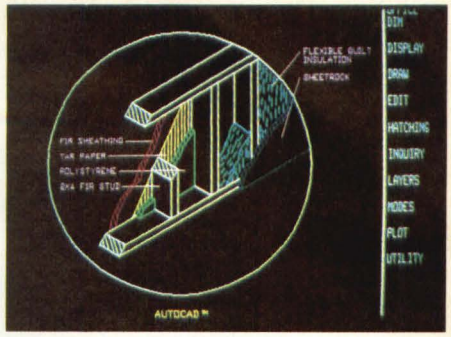


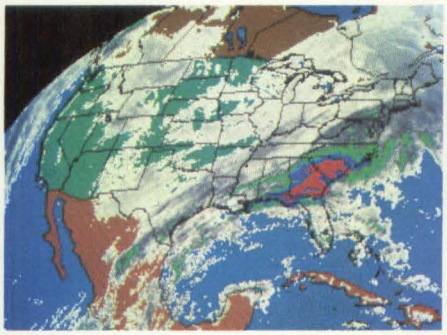
1. High Speed (MicroCAD Software)



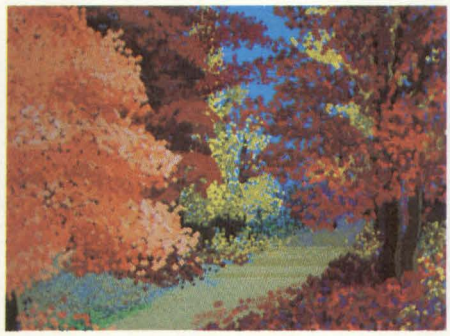
2. Dual Display Modes (Energraphics Software)



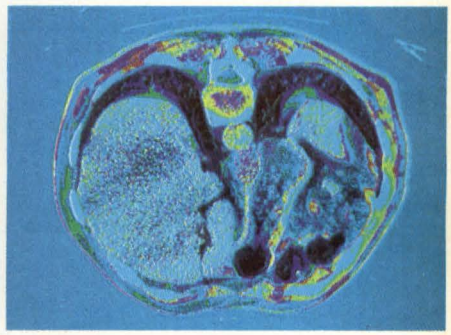
3. Simplified Processing (AutoCAD Software)



4. 9 Bit Planes (Courtesy WSI Inc., Bedford, MA)



5. 16.8M Color Shades (Courtesy Catherine Del Tito, Wave Graphics)



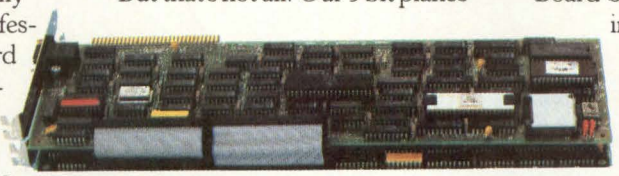
6. High Resolution (Courtesy University of North Carolina at Chapel Hill, Depts of Computer Science and Radiology)

Six reasons why professionals continue to choose Vectrix for quality IBM XT/PC graphics.

Even though IBM offers a color graphics card, professionals still choose Vectrix. It's not surprising. Especially once they've seen us in action. Professionals know that our VX/PC Board Set delivers the quality and performance they need for serious color graphics.

The VX/PC Board Set provides advanced features that help simplify sophisticated graphics design. Besides displaying 512 simultaneous colors from a palette of 16.8 million, the VX/PC supports an extensive library of on-board graphics macros for ease of programming and fast design, as well as full emulation of the IBM color card. And, an on-board 16-bit microprocessor frees your computer to concentrate on other tasks.

But that's not all. Our 9 bit planes add an extra dimension of sharpness and clarity to your image that must really be seen to be appreciated. That's why it's not surprising to see Vectrix color cards in applications such as medical imaging, weather satellite data mapping, computer aided design and drafting, and graphics arts, to name a few.



What you will find most surprising, however, is the price. Our VX/PC Board Set was designed with the OEM in mind. So when comparing the performance of Vectrix with the competition, check the price too. You'll like what you see. For more information, contact Vectrix Corporation, 2606 Branchwood Drive, Greensboro, North Carolina 27408. Phone (919) 288-0520. Telex 574417.

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THERE'S A LOT OF POTENTIAL LOCKED INSIDE EVERY MICROVAX II.

AND EMULEX HAS ALL THE KEYS.

Our complete line of high performance storage and communications products unlocks the processing power of DEC's new MicroVAX II.

Emulex products operate transparently to MicroVMS so as to permit ease of implementation and use. Furthermore, thanks to our accomplishments in advanced VLSI technology, you get superior performance and compactness.

THE KEY TO MICRO PERIPHERALS. The new Emulex QD01/D disk controller is a dual size board that's packed with capabilities. And with it, you get all the features of Mass Storage Control Protocol (MSCP). It controls up to two ST506 drives with a 2MB peak Q-bus transfer rate. Features include a 10K Byte data buffer, 22-bit addressing and 1:1 interleave.

The Emulex QT12 tape controller is also dual size and ideal for backup of micro peripherals. Through firmware, it operates transparently to the driver. It has a QIC2 interface to operate with 5¼" footprint ¼" tape drives.

THE KEY TO COMMUNICATIONS. Emulex delivers an edge in Q-bus communications multiplexers. Our high-performance CS02 doubles line capacity by putting 16 async lines in the space DEC uses for eight. The CS02 runs at up to 38.4 K baud per line and incorporates a 256-character FIFO buffer for fast, sure data transfers. For flexible configuration, the CS02 is RS-423 and RS-232C compatible.

Shown, left to right: SC03/MS disk controller, UC03 host adapter, TC03 tape controller, CS02 communications multiplexer and QD01/D disk controller.

THE KEY TO LARGE PERIPHERALS. Emulex's SC03/MS disk controller incorporates a fully transparent set of firmware which has the features of MSCP. It interfaces to industry-standard SMD drives, handling disk transfer rates of up to 1.8MB/sec.

Our tape drive story is equally impressive. Three Emulex controllers —TC02, TC03 and TC05—are fully compatible with DEC TS drivers.

With the TC02, you can take advantage of start/stop drives and streamers with 1600 bpi at 125 ips, or up to 6250 bpi at 25 ips. Formats available include NRZI, P.E., and GCR. Data rates can be as high as 200,000 characters/sec.

The new TC03 tape controller has all the features of the TC02 and also offers a large (3.5 KB) data buffer and block mode DMA for increased data throughput. It's also compatible with up to four Pertec industry-standard drives.

The TC05 handles 55 ips tape speeds, 8000 bpi densities on a Sentinel drive, and features a 3.5KB buffer.

THE KEY TO SCSI-BASED MICRO PRODUCTS. For a choice of micro storage products, start with the Emulex UC03 host adapter to interface your MicroVAX II with SCSI-based micro controllers. The UC03 supports multiple peripherals simultaneously through a complete family of Emulex micro controllers. These include disk, magnetic tape and optical disk.

THE KEY TO PACKAGED SUBSYSTEMS. Emulex's unique solutions for MicroVAX II extend to packaged micro subsystems.

The Emulex Decathlon can accommodate three 5¼" peripherals in rack-mount or tower packages. It provides a selection of both Winchester drives from 36-110MB (formatted) and ¼" tape streamers up to 60MB. The Emulex Medley incorporates a Winchester (up to 110MB) and back-up streamer (up to 70MB) in a rack-mount compact package. Whatever storage medium you choose, Emulex has the perfect package for you.

EMULEX. YOUR KEY RESOURCE. We can unlock the power of DEC's MicroVAX II. And our broad product line can also add new power to your high end LSI-11, Micro PDP-11, PDP-11 and VAX systems. Improved performance and unique features are yours in a full range of DEC system storage and communications enhancements.

Unchain DEC's machines for enhanced capabilities now. For product or sales information, call toll-free 1-800-EMULEX3. In California, call (714) 662-5600. Or write: Emulex Corporation, 3545 Harbor Blvd., P.O. Box 6725, Costa Mesa, CA 92626.

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The genuine alternative.

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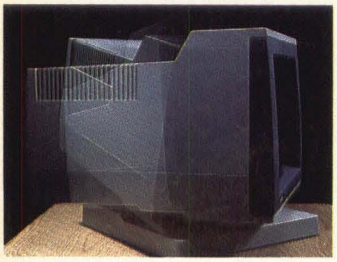
Most products shown are stocked nationally by Hamilton/Avnet, Kierulff Electronics and MTI Systems Corp.

GOOD LOOKS RUN IN THE FAMILY.

LEXIDATA'S LEX 90 FAMILY OF HIGH-PERFORMANCE DISPLAY PROCESSORS.



Lexidata's monitor enclosure design features a unique tilt and swivel movement with smooth and easy operation. All monitor connections and peripheral power supplies are located in the enclosure's base.

LOOKING GOOD. The LEX 90™ family is a good family to know. It's as advanced in a business sense as it is technologically. And what it has, compared to what it costs, makes it look very good indeed. For example:

Its software architecture is compatible both within the family and with our popular Series 3000 line. So performance upgrades are easy and economical. And software investments are well protected.

Every LEX 90 model has the same basic components which use the latest bit-slice technology for rapid execution of complex calculations and set-up times.

The family's flexibility allows you to buy only the functionality you need now, and gives you the ability to add on later as required.

Exclusive SimulRes functionality allows simultaneous display of 640x512 and 1280x1024 images on the same screen. A True Color configuration offers two buffers of 640x512x24 with an 8-bit color lookup table for each color. And where you're looking for high performance with high resolution, there's a LEX 90 model that can support up to 24 planes of 1280x1024 display memory at 60Hz non-interlaced refresh.

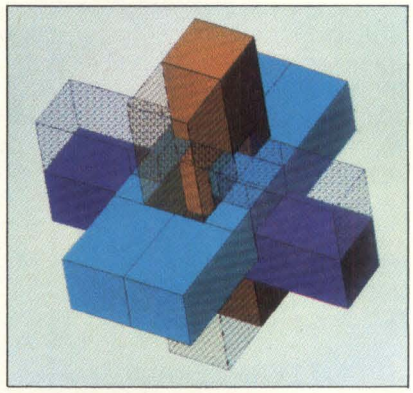
LEX 90's SimulRes enables the designer to mix theory with reality by allowing the simultaneous display of a wire-frame model with the real-life product. (Courtesy of PDA Engineering)

A tiger shows off its "true colors" with the LEX 90 True Color display system from Lexidata.

The extraordinary solid modeling display capability of our patented SOLIDVIEW™ technology is available in a 640x512 version. And for petrochemical applications, there's GEOVIEW,™ a three-dimensional geological interpretation package.

On-board diagnostics, based on a 6801 microprocessor, help maximize uptime. And the unique tilt-and-swivel movement of our monitor allows smooth and easy operation of your display.

Of course, the entire family is compatible with a variety of leading application software packages and minicomputers. Which makes everyone look even better.



SOLIDVIEW, Lexidata's patented technology for the display of solid models, is available as an option on selected LEX 90 display processors. Its translucent shading pattern allows you to see inside your solid model.

For a good look at the LEX 90 family and its expanding capabilities, call us at 1-800-472-4747. In Massachusetts, call (617) 663-8550. Or write: Lexidata™ Corporation, 755 Middlesex Turnpike, Billerica, Massachusetts USA 01865. TWX: 710-347-1574. In UNITED KINGDOM call: Lexidata Ltd., Hook (025672) 3411. In FRANCE call: Lexidata SARL, Rungis (1) 686-56-71. In JAPAN call: Lexidata Technical Center, Tokyo 486-0670.

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LOOKING GOOD.

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HOTLINE

MOTOROLA ARRAYS ON MENTOR VIA EDIF DATABASES Using EDIF physical databases, users of Mentor workstations will be able to directly download Motorola's 2- and 3-micron HCMOS Macrocell Array libraries from Motorola's mainframe.

20,000-GATE GATE ARRAY IN 1.5 MICRON GEOMETRY NEC Electronics is sampling the μPD 65200 19,551-gate gate array. Fabricated in 1.5μm geometry using CMOS-4, internal gate delays are 0.5 nsec. The seven other CMOS-4 ICs in the family have fewer gates.

SUN FIRST TO RUN P-CAD PORTED TO UNIX 4.2 Personal CAD Systems' simulation, PC board and PLD design and layout software has been ported to UNIX 4.2, and Sun is the first to run all of the P-CAD UNIX programs.

TWO FIRMS AIM TO REDUCE THE PC AT TO A FEW CHIPS Zymos announced a 4-chip version of the IBM PC AT: the 80286, 80287, 8042 and a standard cell. At the same time, the start-up Chips & Technologies is aiming to produce an AT in a 20-chip set.

HARDWARE MODELING, NETWORKING FOR VALID Valid now has a 68020 workstation upgrade and supports DECnet-TCP/IP networking. In addition, a hardware modeling and simulation accelerator called Realmodel, Teradyne's Lasar Version 6 logic simulation and ECAD's Dracula IC layout verification will run on Valid systems.

FUJITSU MASK-PROGRAMMABLE CMOS ROMs DEBUT IN US Two Fujitsu MB8300 series ROMs will be sold in the US. A 1 Mbit ROM and a 256K static ROM are initial offerings; both are TTL-compatible and organized ×8.

DG JOINS FORCES WITH THREE DESIGN AUTOMATION FIRMS Data General has invested in Cericor, and DG Eclipse MV and DS workstations will run Cericor's CDA-5000. DG's DS is also the base for RDS' AutoMate PC board design workstation. And Viewlogic's Workview software is available on the DG/One personal computer.

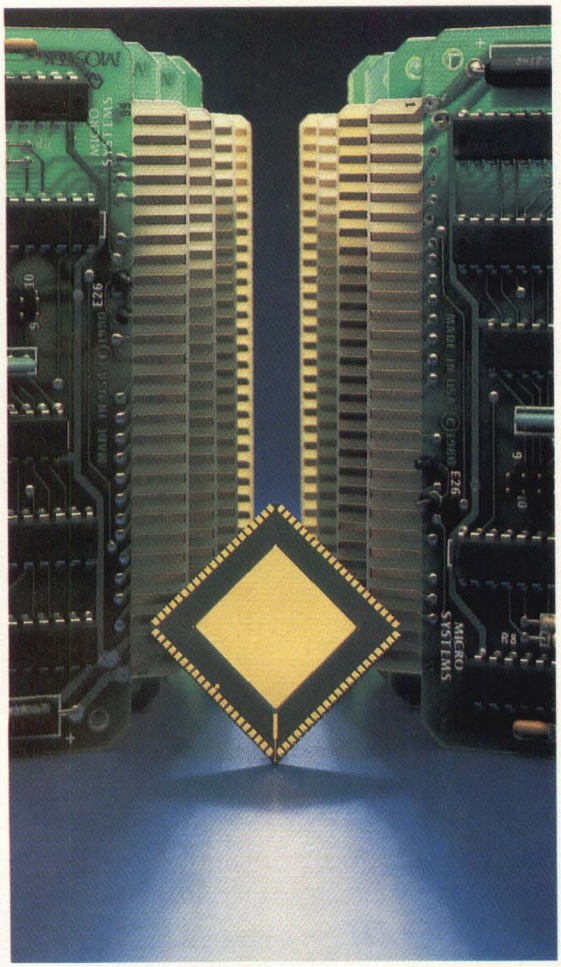
THREE IMAGE PROCESSING PACKAGES ANNOUNCED The first, Math Advantage from QTC, features 180 math routines callable from C or Fortran. The second, PICDMS III from MIB Chock, runs under PC-DOS for image processing and 2D or 3D model building. The third, announced by Process Software, is VIOS, with edge enhancement, differencing and integration for Datacube QVG systems.

CAE SYSTEMS RUNS ON MICROVAX II, HAS ADDED TOOLS Besides running on the MicroVAX II, CAE Systems has added an integrated simulator, MultiSim, and a layout editor called LEIA. Third party offerings include ECAD's Dracula II IC layout verifier and Seattle Silicon's Concorde module generator.

1.25 MICRON HCMOS GATE ARRAYS IN DEVELOPMENT Using TRW's HCMOS process, Custom MOS Arrays will develop and produce 1.25-micron gate arrays with 500 to 25,000 gates, up to 330 pins and 0.9 nsec typical gate delays.

VTI SILICON COMPILER, TOOLS AVAILABLE ON DAISY VLSI Technology's IC design and silicon compiler tools have been ported to Daisy Concurrent Chipmaster and Siliconmaster workstations.

THE GATE TO A SMARTER STD BUS.



STD BUS has always been a smart choice for flexible, cost-effective Z80® systems. And now, Mostek has made it smarter still. By adding a proprietary gate array to provide more intelligence to your system.

Our family of intelligent STD boards all feature a Z80 processor, DMA controller and on-board memory. And our custom gate array, which took three man years to develop. But that's where the similarity ends. Because we've provided different features on each board to make sure you get the best possible performance from each.

For example, we've got intelligent serial boards for short (250 feet) and long (1 mile) communication distances. We have another that implements the IEEE 488 General Purpose Interface Bus standard with speeds up to 300 Kbytes/second. And an IPIO with 32-bits of parallel I/O, suitable for high-speed control and data transfer.

The point is, Mostek designed these to be the most sophisticated STD BUS boards available today. Which is one more way in which we show our continuing commitment to STD BUS.

So to give your system some extra smarts, contact Mostek Corp., 1215 W. Crosby Road, MS1051, Carrollton, Texas 75006, or call 1-800-635-0200. In Texas, 1-214-466-8801. In Europe, (32) 02/762.18.80. In Japan, 03/496-4221. In the Far East (Hong Kong), 5.681.157-9.

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ICs

Modular Packaging Points To Denser Systems

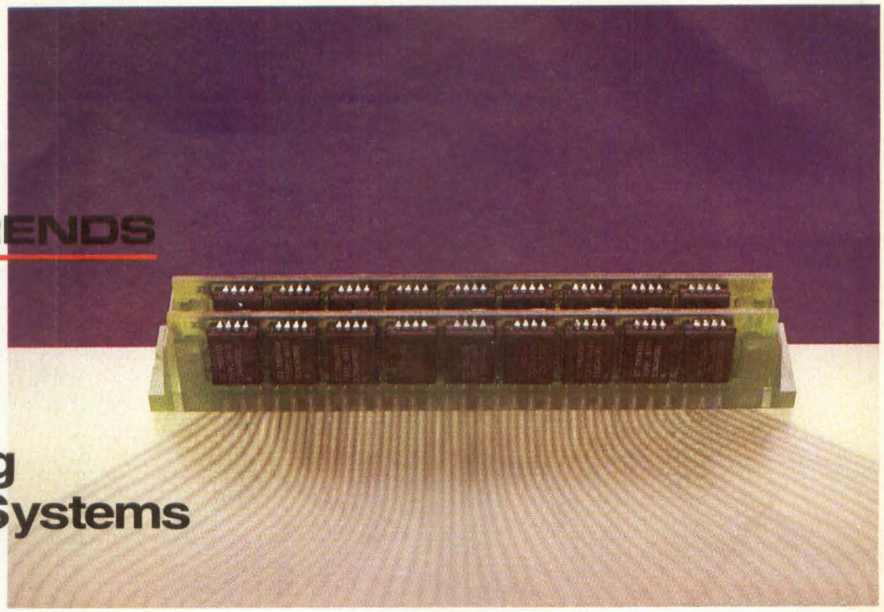


Figure 1: This Molex Single In-Line Memory Module socket acts as a connector for a high-density IC packaging system. Two baby boards with nine ICs each are SIMMs. Using plastic leaded chip carriers, even memory ICs can be mounted on standard epoxy-glass substrate baby PC boards with an edge connector and plugged into the SIMM socket.

The ability to upgrade systems with improved components or more memory has been hampered by the need to completely rework the PC boards. To overcome this, a module and socket packaging scheme has been developed by Wang (Lowell, MA), Molex (Lisle, IL) and Texas Instruments (Dallas, TX) that provides upgradable, dense circuitry. The Single In-Line Memory Module (SIMM) is a baby board onto which single in-line packages are surface mounted; two of these modules snap into a SIMM socket (**Figure 1**) which is wave soldered onto the main board.

A need for denser memory in Wang's Office Assistant was the impetus for the project. Texas Instruments (TI) provided surface mount expertise to create a leadless edge-card module from Wang's SIP package. Molex worked with Wang to make the pluggable socket. In addition to increasing density, using SIMM provides easy field or customer upgrade and repair. The project was initiated under full public disclosure, and others have joined. Shortly after the initial design, AMP (Harrisburg, PA) also began making a SIMM socket; besides TI, Toyocom (Tokyo, Japan) is in production with components and modules to fit the design. AMP's socket, though form and fit compatible with Molex's, uses a different design. It may be advisable to qualify them separately on both cost and performance.

The Molex SIMM socket uses zero insertion force (ZIF) contacts to hold baby boards in place; these allow up to 25 matings. Pegs are used to ensure proper placement of the socket on the motherboard and a rib and slot arrangement assures that the module boards load correctly into the socket. At present, no second source is available with this design. All SIMM modules hold up to nine ICs; though initially used for RAM, other ICs like I/O, logic or hybrids could be used on the module baby boards.

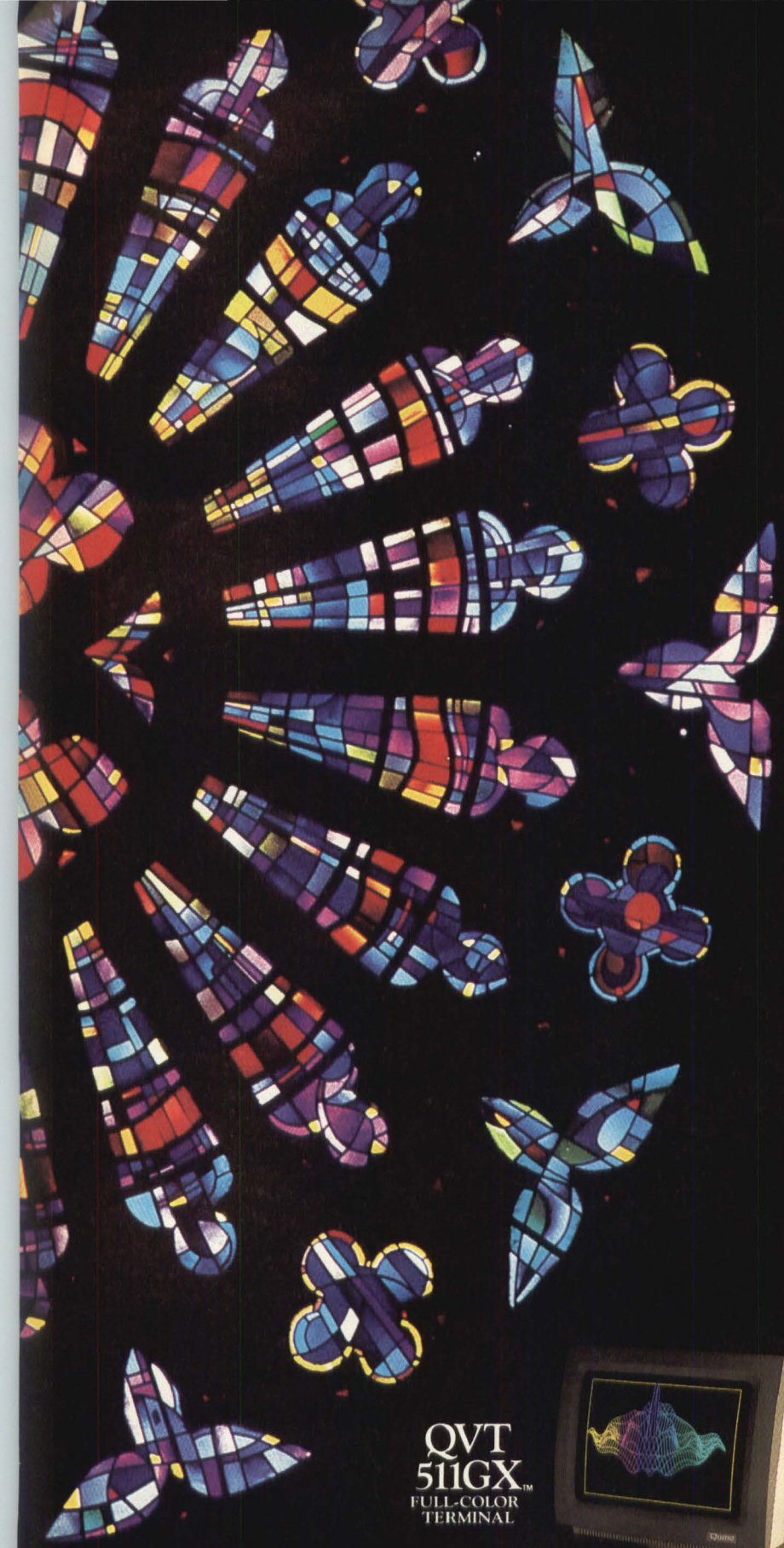
Plastic leaded chip carrier packaging has allowed lower costs as well as the ability to mount the components on standard epoxy-glass substrate baby PC boards. According to Wang, 1 Mbit DRAM density is available for the price of a 256K DRAM. Yield of surface mounting also improves with the smaller boards.

Two baby boards with nine 64K RAM ICs surface mounted to it plugged into one SIMM socket provide 512K of RAM (with eight chips used as storage). Mounting requires 60 holes on the PC board; the individual packages are surface mounted to baby boards. This is much easier to install than 18 discrete 64K chips in DIP packages, which would demand drilling and routing to 288 holes. For upgrading, 256K RAM chips could be mounted on the standard baby board and inserted into the same socket. The modules were designed to accommodate 1 Mbit and 4 Mbit parts as well. SRAM and DRAM modules are now in production.

According to Jim Clayton, principal microelectronic engineer at Wang's IC Technology R&D group, the major advantage this scheme provides is convenience and low risk for introducing surface mounted components into products. One problem manufacturers have had with surface mounted components is that a board generally is not all surface mounted, but also includes leaded components wave soldered into through-holes. Mixing of surface mount and leaded components means two soldering operations and generally low yields. With the SIMM scheme, surface-mount and through-hole components are on separate boards. SIMM sockets use through-holes, like the other components on the main board; components are surface mounted only on separate baby board modules. The Molex socket is made of a material that will withstand the temperatures used in surface mount soldering if that is desired.

The initial Wang design, in production since late 1983, has evolved from a leaded ceramic module to the PLCC on edge-connector module scheme. Modules in sockets of the Office Assistant stand at 90° from the motherboard; a product to come out soon uses SIMM sockets that hold modules at about a 25° angle (**Figure 2**), and work is underway to improve on that. By increasing the angle, board-to-board spacing could be improved from 0.9″ to 0.5″. Wang has also reported work on increasing the pin count of the connector from the current 30 pins. To further increase density, double sided baby boards might be used. This would provide 18 ICs in one module and up to 36 per socket.

Many major computer firms are evalu-



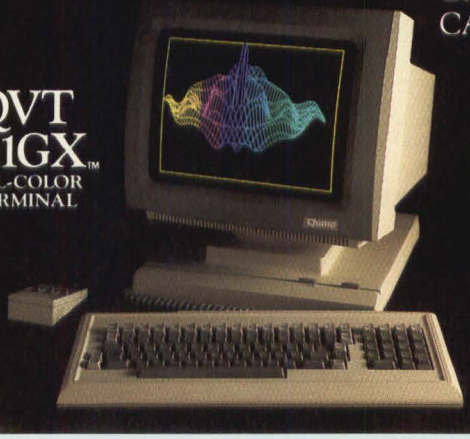
When you're ready for the brilliance of color, we'll be there.

Now you can have the beauty and precision of color graphics for business, engineering and scientific applications—at much less cost than ever before! Qume's new QVT 511GX™ terminal provides flicker-free, non-interlaced raster scan graphics, with a selection of up to eight colors from a palette of 64. The QVT 511GX is fully compatible with the Tektronix 4105 and accepts all of its software, including PLOT 10 packages. It can also be used in Tektronix 4010, 4100 and 4110 series environments, and works beautifully with the Tektronix 4695 color graphics copier. What's more, it conforms to both ANSI X3.64 and ISO 6429 protocols for text editing. A mouse device, capacitive keyboard, and advanced ergonomic design are all standard.

The QVT 511GX measures up to Qume's exceptional standards for performance, quality control, and reliability. And it's backed by our experience and resources as an ITT company. So whatever your applications, we'll be there with a dazzling display of technical support.

For full details on the new QVT 511GX and Qume's other graphics and alphanumeric terminals, or our full line of daisywheel printers and disk drives, call (800) 223-2479. Or write Qume Corporation, 2350 Qume Drive, San Jose, CA 95131.

QVT 511GX™
FULL-COLOR TERMINAL



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Circle 45

ating the concept for packaging memory and other functions. The field upgrade and service are a major impetus for Apple Computer (Cupertino, CA) choosing SIMM for memory in an upcoming product. Space saving is another important aspect for personal computers. Apple will use the 25° angle version to allow the low-profile keyboard to fit easily over the CPU. Northern Telecom's Bell Northern Research (Mountain View, CA) is evaluating the scheme for packaging codecs and other circuits; each line of the Meridian SL1 PBX could be implemented in a module. Here, the angled modules will fit into the board-to-board spacing.

One concept that designer Jim Clayton of Wang suggested is that logic modules in a SIMM configuration could act as instant gate arrays. To implement a complex function immediately while it is in the process of being designed into a single chip, baby boards with ICs to provide the desired functions could be plugged into a few sockets.

Another possibility is to use the scheme for personalizing compatibility; each user of a standard peripheral could implement an interface for a different system by plugging in different modules. Molex literature suggests that standard products could easily be customized by providing a SIMM socket and plugging in the appropriate modules. The density and upgradability will make SIMM an attractive scheme for minicomputer and peripheral makers, with the socket serving as a connector.

—Pingry

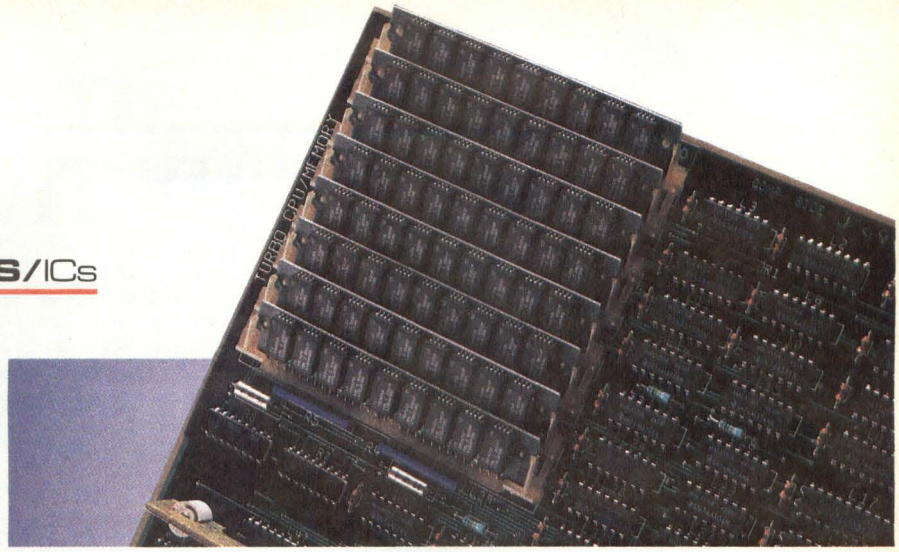


Figure 2: This Wang board shows an array of SIMMs in their sockets standing at an angle to reduce board-to-board spacing. The board shown will be used in a product to be announced soon. Since the module baby boards are not soldered in, customers can change and upgrade the system themselves without waiting for a repairman or an entire board to swap.

DESIGN TOOLS

Programming Silicon Compilers For IC Design

Only a few companies offer silicon compilation tools which allow system designers to rapidly generate custom ICs. One recent entry into this arena is Silicon Design Labs (SDL) (Liberty Corner, NJ) with a product for IC designers rather than system architects. The SDL software, called Generator Development Tools (GDT), allows IC designers to create customized silicon compilers by incorporating their own IC design knowledge into the compiler.

The primary difference between a silicon compiler built using SDL's software and other, off-the-shelf silicon compilers is the user's design expertise built into the tools. Competitors like Silicon Compilers Inc. (SCI) (San Jose, CA), Metalogic (Cambridge, MA) and Seattle Silicon (Seattle, WA) offer turnkey systems

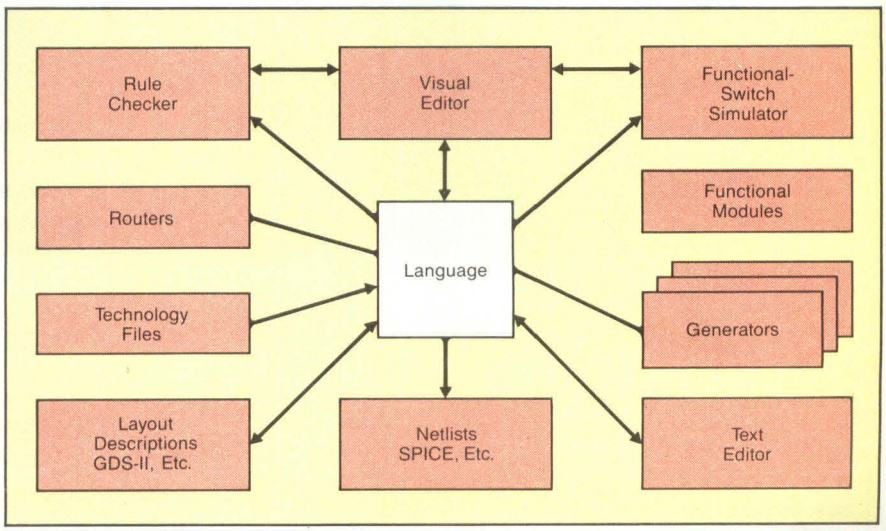
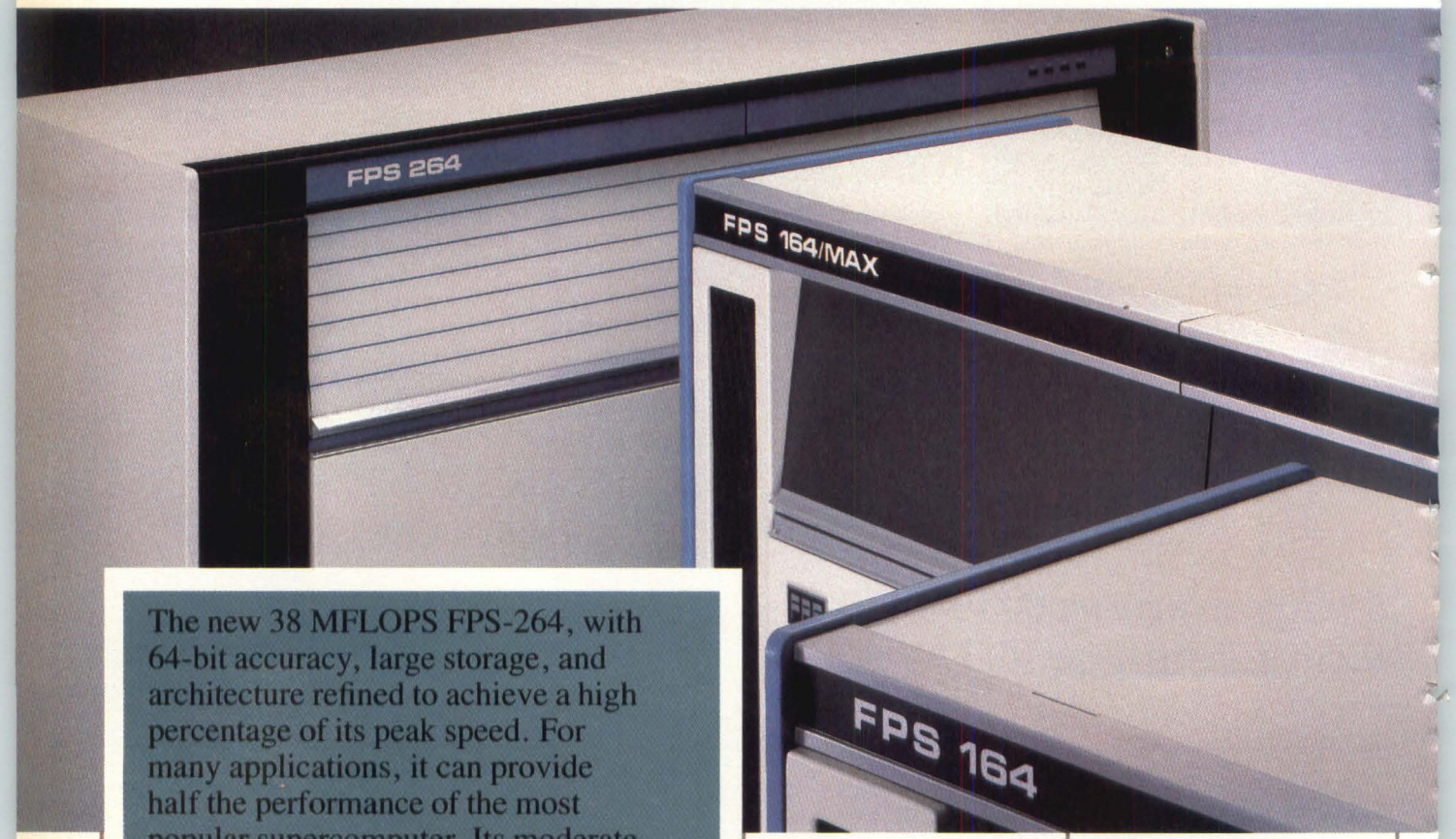


Figure 1: Customizing a silicon compiler with SDL's Generator Development Tools is done in an environment that includes interfaces to standard layout descriptions and common netlist formats. The L language is the heart of the development system.

THE FPS 64-BIT FAMILY: CONSIDER WHY THE MOST ACCESSIBLE SUPERCOMPUTERS MAY BE THE FASTEST WAY TO DO YOUR JOB.



The new 38 MFLOPS FPS-264, with 64-bit accuracy, large storage, and architecture refined to achieve a high percentage of its peak speed. For many applications, it can provide half the performance of the most popular supercomputer. Its moderate price and exceptional support liberates supercomputing from the realm of major corporate investment and puts it within practical reach of departments and teams.

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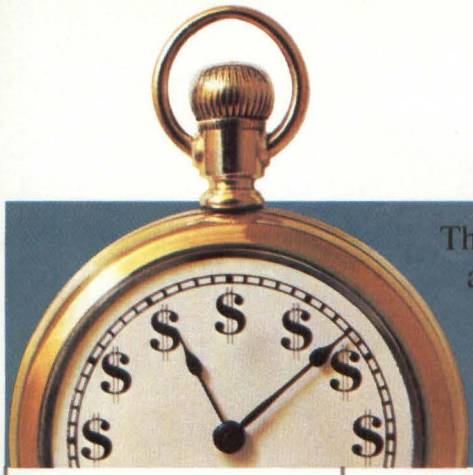
1. FPS protects and utilizes your existing software resources. FPS offers you an exceptional, proven software tool set. If your investment in FORTRAN is typical, the FPS Compiler will alone be a compelling advantage.

2. More applications software than for any other comparable computer. Compare quantity and quality of compatible third party software packages—for structural analysis, circuit design, reservoir simulation, fluid flow analysis, chemistry and much more—and the FPS advantage widens.

3. The FPS 64-bit family makes supercomputing speeds affordable at the department level. Even teams with remote access to Crays® and Cybers™ are



The FPS optimizing FORTRAN-77 Compiler lets you easily adapt code to FPS' pipelined architecture in a form that is nearly as efficient as hand-coded assembly language. With extensions for asynchronous I/O and for enhancing compatibility with other compilers, it is one of most comprehensive tools of its kind.

likely to find that the advantage of immediate, local access is well worth the sacrifice of standing in line for the "fastest" machines.

System prices start at $300,000 (U.S.) for the 11 MFLOPS FPS-164. The new 38 MFLOPS FPS-264, starting at $640,000, achieves 4-5 times the speed of the FPS-164 on many applications programs. The multiple parallel processing units and peak 341 MFLOPS of the FPS 164/MAX can run many matrix computations faster than supercomputers, for less than one-tenth the price.

Family Specifications

	FPS-264	FPS-164/MAX	FPS-164
Peak speed, MFLOPS	38	33-341	11
Dynamic range	2.8×10^{-309} to $9.0 \times 10^{+307}$	2.8×10^{-309} to $9.0 \times 10^{+307}$	2.8×10^{-309} to $9.0 \times 10^{+307}$
Word size	64 bits	64 bits	64 bits
Main memory capacity	4.5 MWords	15 MWords	7.25 MWords
Maximum disk storage capacity	16 Gbytes	3 Gbytes	3 Gbytes
Precision	15 decimal digits	15 decimal digits	15 decimal digits
Vector registers	4 x 2K	124 x 2K (max.)	4 x 2K
Scalar registers	64	184 (max.)	64
Host interfaces	IBM, DEC	IBM, DEC, Sperry, Apollo	
Program Development Software	FORTRAN Compiler, Overlay Linker, Assembler, Object Librarian, Interactive Debugger.		

Family Performance Measures

	FPS-264	FPS-164/MAX		FPS-164
		15 accelerators	1 accelerator	
Peak MFLOPS	38	341	33	11
Peak MOPS	190	1705	165	55
Peak MIPS (Instructions are multi-parcel)	19	5.5	5.5	5.5
Typical MFLOPS, LINPACK Benchmark	9.9	20.0	6.0	2.6
Whetstones, KWIPS (64-bit)	19,000	5440	5440	5440
1000x1000 matrix multiply, seconds	53	10	66	189
$K/MFLOPS (system price/peak speed)	$17K	$2.5K	$12K	$27K

4. The FPS family is expandable. Proven dependable. Well-supported. In other words, a safe, farsighted investment. You can upgrade your existing FPS computer, or evolve from one level of performance to another, with minimal disruption. And you can bank on a record of reliability that begins with exhaustive manufacturing testing and extends to our 30 field office service facilities worldwide.

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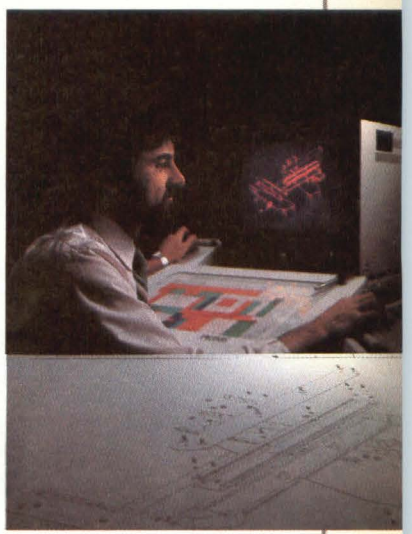

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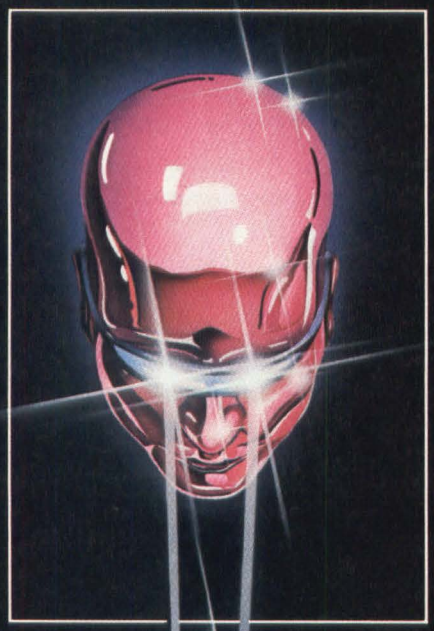

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based on the firms' IC design knowledge.

Two distinct kinds of silicon compilers exist: behavioral and structural. Behavioral systems require designers to specify only the device's behavior. This description is typically in the form of an algorithm, an I/O specification or a Boolean expression. GDT allows a designer to create structural silicon compilers, which bring designers closer to traditional design methods by requiring a block level specification of the function.

According to Peter Rip, SDL's vice president of marketing, merchant and captive semiconductor manufacturers are among the potential users that will benefit from GDT. NCR Microelectronics (Fort Collins, CO), one of SDL's first customers, has been a beta site for the product. The two companies also have an agreement involving the licensing of SDL's silicon compilation technology to NCR in exchange for NCR's CMOS fabrication processes.

An important aspect of any new CAD/CAE tool is how well it integrates into existing design environments. With this in mind, SDL designed a software package that translates layout and netlist data to and from various standard formats. For example, layouts can be output in GDS-II or CIF format, and netlists can be put in SPICE format. GDT is written in C, developed under UNIX and runs on workstations from Apollo (Chelmsford, MA) and Sun Microsystems (Mountain View, CA).

GDT is comprised of the L compiler and its routers, a graphical editor with an interactive rule checker and a mixed-mode switch/logic simulator. The heart of the Generator Development Tools is L, a proprietary layout description language. Hierarchical descriptions of IC layouts, layout generators and circuit/logic elements are created with L.

On the lowest level, the language describes geometric objects such as polygons, rectangles and lines. Geometric objects are included in L to allow the designer to enter geometric constructs but

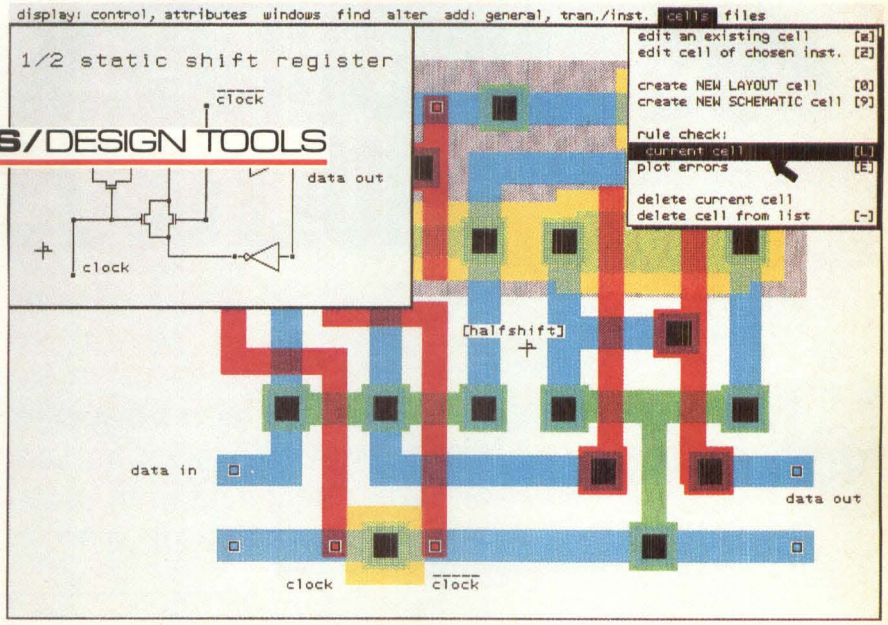

Figure 2: L-Editor, an interactive graphical editor, is the primary means of viewing the output of generators written in L. Its role is to aid in the development of module generators. Multiple windows and pull-down menus are among its features.

are not the preferred working level. Higher level electrical objects such as wires, contact cuts, terminals and transistors provide a more powerful means to build a generator. Designers lay out handcrafted ICs by directly placing and interconnecting these circuit primitives. This is done with either the graphical editor or the text editor.

Since the tools are based on a hierarchical language, creating layouts and layout generators can be done in a structured fashion. The basic building block in L is a cell containing wires, polygons and transistors. Cells can contain calls to other cells, and generators can call other generators. L also has automatic routing statements that call various routers to wire cells together. The particular router accessed depends on the configuration of the module being generated.

L-Editor and L-Simulator are the other parts of the tool set. L-Editor is an interactive graphical editor that also does rule checking and logical simulation of L files. It reads all L language constructs and is used to view the output of generators written in L. L-Editor has an interactive interface to L-Simulator. An event-driven logical simulator, L-Simulator can mix switch simulation of individual transistors with functional simulation of arbitrarily sized logical blocks. The complexity of these blocks ranges from transistors to VLSI functions.

When using GDT, generators can be built from the top down or the bottom up or a combination of the two styles. Top down design begins with blocks interconnected using L-Editor and described functionally via L-Simulator. High-level design verification is then performed by executing test vectors with L-Simulator. As the design progresses, functional blocks are given more detail. The procedure continues until the blocks can be replaced with low-level circuit generators.

Bottom up design can be done in several ways. One method uses L-Editor. The procedure entails drawing the layouts, simulating the circuit and running a design rule check. Timing verification is then performed by passing the netlists to a timing simulator.

When using silicon compilers built with GDT, as with other structural compilers, the designer's primary task is to define the functional blocks necessary to implement the device. By inputting the chip's architectural specification and letting the machine generate the logic and layout, the system architect is removed from lower level design tasks. The main advantage of a custom-built compiler is that a particular IC designer's expertise may be built into the system.

— Collett

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3	4	--		iSBC MEM/310 1 Mbyte Mem board
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6	10	--		iSBC CSM/001 Cent. Serv. Module
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8	5	--		iSBC PKG/609 9 slot cardcage & PSB backplane
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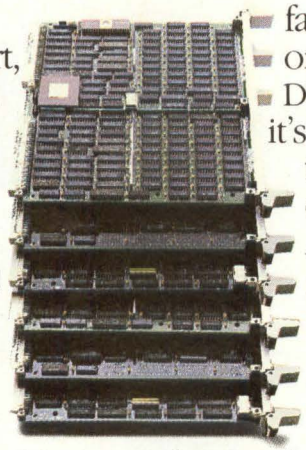

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Supercomputer Exploits Parallel Processing

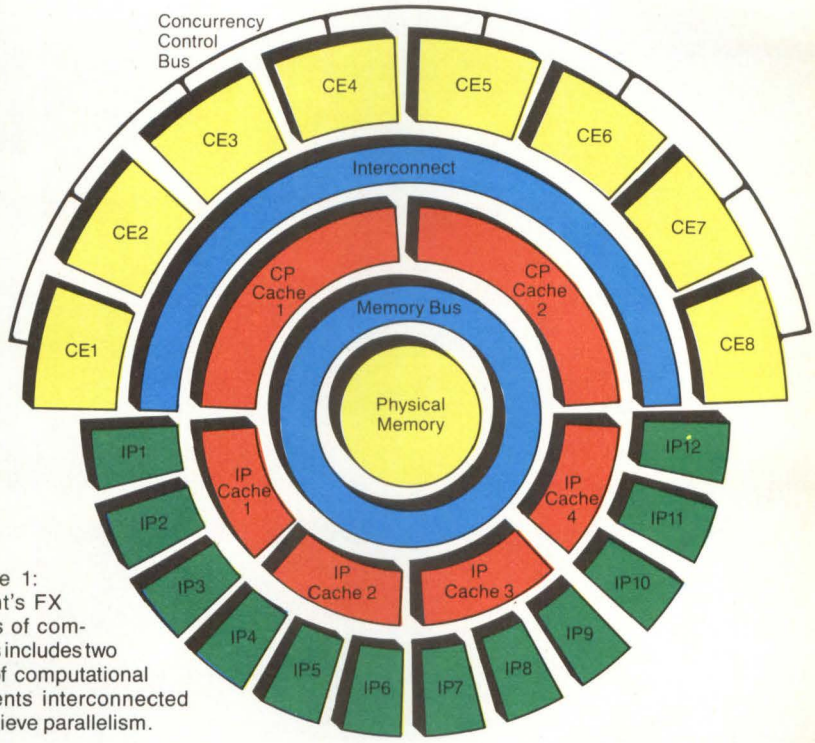

Figure 1: Alliant's FX series of computers includes two sets of computational elements interconnected to achieve parallelism.

As the cost of processing elements decreases, it is possible to build computer systems with a number of processors sharing the burden of executing complex programs efficiently. Alliant Computer Systems Corp. (Acton, MA) has combined three forms of parallel processing, increasing not only system throughput but also program execution speed in the FX series of computers. This combination shows why there is some confusion when describing the sorts of architectures currently on the market.

Parallel processing describes three forms of processing. In the first, instruction level parallelism, a single CPU instruction operates on multiple functional units. This design is typically used on all mainframes and supercomputers. The second form executes independent jobs in parallel on independent processors. Used in many microprocessor-based systems, this design increases system throughput, but not the execution speed of individual programs. In the third form, parallel processing employs multiple general-purpose computers to reduce the time-to-solution performance of a single application.

Using all three forms of parallel processing, Alliant claims one-fourth the performance of a Cray for the high end of the FX series. This has been achieved by using two classes of computing resources (**Figure 1**). Computational elements (CEs) are pipelined processors with integrated vector, IEEE floating point and parallel processing hardware. Up to eight CEs may be interconnected to a computational complex with common memory through a 376 Mbit/sec switch as well as interconnected with each other through a dedicated parallel processing control bus. All of the processors in the complex are applied to the execution of a single program, transparent to the programmer.

At the same time, an expandable pool of interactive processors (IPs) execute in parallel with each other and the CEs. The IPs enable the CEs to concentrate on computational tasks while maintaining system responsiveness for interactive users by running the operating system and interactive applications. The Alliant operating system, based on UNIX Berkeley 4.2, transparently orchestrates queues of ready to run tasks for the two types of processors. Computational jobs are scheduled for the computational complex, interactive and operating system activity for any available IP.

Perhaps the most important part of the Alliant system is its ability to run existing Fortran programs without reprogramming. Alliant's FX/Fortran compiler automatically transforms Fortran source code for scalar concurrent, vector and vector concurrent execution. Also DO loops that execute in vector mode on supercomputers are compiled to run as parallel vectors on the FX/8.

Alliant currently plans to offer two versions of the supercomputer. The FX/1 will be a desk-high system with a single computational element and one or two interactive processors that share a UNIX-based kernel and operate in parallel. The FX/8 will be a series of machines that can be expanded with the addition of up to eight computational elements.

Perhaps the FXs' closest competitor is the C-1 from Convex Computer (Richardson, TX). The C-1 is a 64-bit scientific computer that also supports scalar and vector processing. Like Alliant, Convex provides a Fortran compiler, Convex Fortran. The compiler performs data flow analysis on iterative sequential procedures to produce parallel executable code for the integrated vector processing of the hardware. However, unlike Alliant, Convex does not produce a range of machines that can be configured and upgraded.

Late in 1986, another parallel processing system will enter the market when ETA Systems (St. Paul, MN) announces its ETA 10, a system that can be configured with two, four, six or eight processing elements. Each processing element is expected to contain both vector and scalar processors. Parallel processing machines are just now making an impact on the market. In the future, all machines will take advantage of some form of parallelism to increase performance.

—D. Wilson

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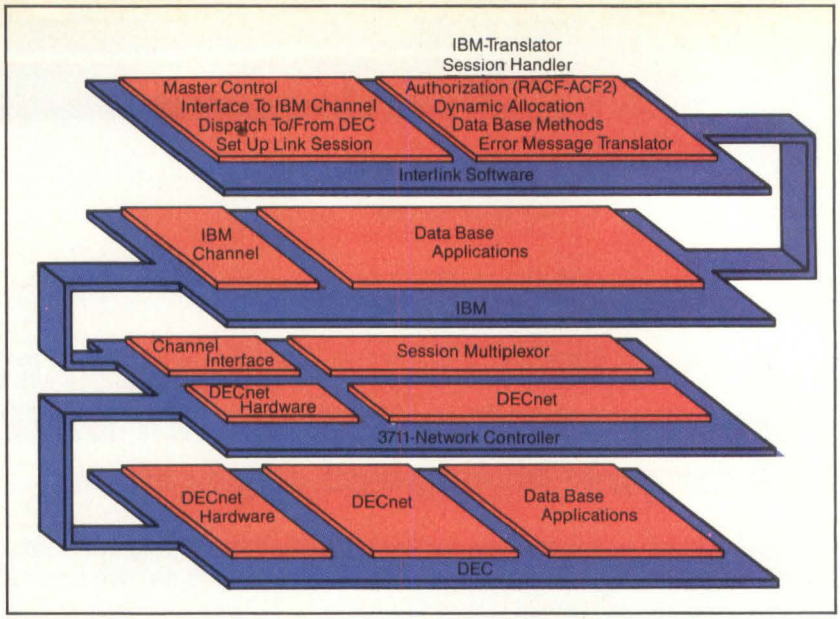


Figure 1: Both software (top) and hardware (3711 Network Controller) are used in Interlink's IBMmvs/DECnet Gateway. The 3711 is channel-attached to an IBM host and connected via Ethernet or synchronous link to DECnet nodes. By performing data conversion, this gateway allows DEC users accessing IBM data to see a familiar screen, and IBM users working with data from DECnet to work with the screen they know.

About 50% of IBM mainframes use SNA/SDLC as their primary communication protocol, making SNA interface products attractive. Protocol converters and terminal emulation products are common. Gateway and translation products provide LAN interfaces to SNA. IBM's increasing use of LU 6.2 for program-to-program communication is an important factor in the effectiveness of products developed by other firms for SNA connection.

There are fundamental differences between SNA and common LAN protocols. SNA is a hierarchial network, based on hosts, controllers and terminals. In contrast, LANs are for peer-to-peer communication. Most LAN protocols deliver several services to every node. Different pieces of software are needed for various SNA functions on various machines.

One sign of SNA importance to other networks is Digital Equipment Corp.'s (Tewksbury, MA) DECnet/SNA gateway. In addition to providing access to IBM-resident applications and computers from DECnet nodes, the gateway allows SNA users to take advantage of resources on DECnet. Recent software includes terminal emulation for Micro/RSX and programming interfaces from VAXes. One package provides Advanced Program-to-Program Communications (APPC) under LU 6.2, the first SNA system to allow universal, peer-to-peer SNA communications. None of the DEC SNA products run on IBM systems, but by building to IBM's DIA/DCA (document interchange and content architecture) guidelines, compatibility is assured.

Combining the advantages of DECnet and SNA from outside those two firms is Interlink (Fremont, CA). The IBMmvs/DECnet Gateway, now available for VM as well as MVS systems, comprises an Interlink controller and software to run DECnet in IBM systems. The controller is connected to Ethernet and channel-attached to the IBM system (**Figure 1**). Unlike the DEC product, Interlink's gateway box performs data conversion. The result is that users on IBM equipment see the standard IBM user interface and those on DEC systems see the screen familiar to them, whether DEC or IBM programs are running. Interlink feels that DEC's gateway will be limited by SNA; the IBM mvs/DECnet Gateway software provides file transfer and the more extensive functions of DECnet to the IBM system.

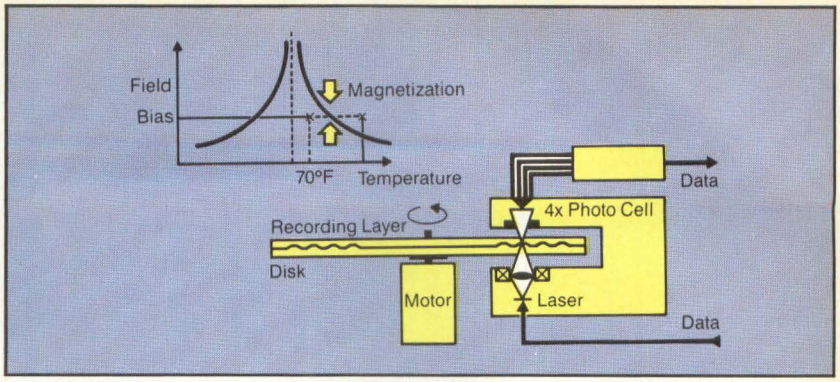
Computer and networking firms may want software to use with their own hardware for gateways to SNA. Access/SNA from Control Data's Communications Solutions Inc. (San Jose, CA) was designed for OEM use. Written in C, Access/SNA emulates an IBM 3270, 3770 or 5250 cluster controller. This emulation is not as limited as terminal emulation. An upcoming release will include LU 6.2 peer-to-peer APPC functions and DIA to interface applications to DISOSS in a mainframe. These could enhance the effectiveness of connections greatly.

A software product based on LU 6.2 has already been introduced by Rabbit Software (Malvern, PA). Called SNA-Plus, this implementation of LU 6.2 protocols provides peer-to-peer and program-to-program communications between IBM and non-IBM machines. Programs in two different languages can communicate directly. With LU 6.2 capability, only the information needed is transmitted, not the emulation of an entire screen of information. The increased operating efficiency, network responsiveness and application flexibility provided by this direct communication will make LU 6.2 products highly desirable.

Network Applications Inc. (Austin, TX) bases SNA connectivity on software products in the IBM mainframe. The most recent product, transNET 2.0, supports non-IBM to IBM interchange of DISOSS 3.2 editable documents. This SNA connectivity for DEC All-In-One, Wang OIS and VS, IBM PC and DG CEO is primarily for volume end users.

Connecting non-IBM equipment into SNA networks by point-to-point links or terminal emulation packages limits functionality and speed. Hyperchannel from Network Systems Corp. (Minneapolis, MN) provides a high-speed host-to-host network, but software for network services is mainly left up to the user. Generally, a gateway between SNA and some other network architecture is most effective. Choices are somewhat limited, but an effective connection to SNA may be a significant factor in choosing a network.

—Pingry



Verbatim uses a thermo-magneto-optical process to store 40 Mbytes on a 3½" disk. A laser temporarily heats a storage film to reduce its coercivity and to permit writing by an external magnetic field. The bits are stored when the film returns to room temperature and its normal high-coercive state. Reading occurs when a beam of polarized laser light shines through the transparent film and a photodetector senses the degree of rotation of the polarized light.

Thermo-Magneto-Optical Disk Promises High-Capacity, Low-Cost Removable Storage

At the 1985 National Computer Conference, Verbatim Corp. (Sunnyvale, CA) demonstrated a 3½" erasable optical disk capable of storing 40 Mbytes. In contrast to optical systems with read-only and write-once media, this approach uses a reversible medium that, like magnetic disks, can be rewritten endlessly. Verbatim envisions these disks as a low-cost, high-density removable storage medium for small systems.

To achieve read/write capabilities, the prototype disk drive uses thermo-magneto-optic recording. Writing on the disk uses a magneto-thermal process that temporarily reduces the coercivity of selected spots on a film composed of terbium, iron and cobalt by raising its temperature with the laser. This allows the magnetization direction in these regions to be reversed by a small external bias field.

Storage of these recorded bits occurs when the reversed domain returns to room temperature with its resultant high coercivity, ranging from 2000 to 3000 oersteds. Erasures and rewrites use the same procedure as writing but with the applied field reversed. In fact, thermo-magneto-optical films are more resistant to accidental erasure than magnetic media since their coercivity is much higher than the 300 to 600 oersteds typically found in conventional recording surfaces.

Magneto-optical reading first requires that a beam of low-intensity polarized laser light be focused on the disk. As it passes through the storage film, the plane of polarization is rotated slightly according to the up or down direction of the magnetic fields. A photodetector and analyzer are used to identify the polarization state of the transmitted light. The head/media separation of greater than 1 mm is much larger than that for magnetic recording, providing better reliability. Pregrooved media permits track alignment within 0.1 μm.

Unlike other types of optical recording media—namely, read-only and write-once—this recording scheme may compete directly with magnetic disk storage. Read-only memory is provided by inexpensive laser-read disks that are pressed from a master disk. Read-only memories are typically used as interactive videodisks for educational training and program or database distribution.

Although they permit the user to write on the disk to encode information, write-once storage devices cannot be rewritten because the reflectivity of the medium is permanently changed by the writing process. These disks are ideally suited for archival storage replacing tape or for on-line mass storage of documents.

In contrast, erasable optical disks will be used in the same way as magnetic disks; Verbatim has pursued optical technology because of a belief that it is better suited to high-density storage than conventional magnetic recording. Dr. Geoffery Bate, senior vice president for engineering, notes that increasing the areal density of magnetic recording is increasingly difficult beyond the typical limits of 9,600 bits/in and 96 tracks/in for double-density floppy disk drives, since the separation between the heads and media must be halved to double the bit density. For example, to achieve a bit density of 50,000 bits/in requires the separation between the head and media be no more than five millionths of an inch.

Means to increase the areal density of rigid magnetic disks may also create problems. Sputtered or plated disks have higher coercivity but may require smaller separations between the disk and magnetic heads. According to Bate, thin-film heads with smaller head gaps to read increased bit density disks have good reading characteristics but poor writing ability. Increasing the track density often requires embedded servo tracks.

Optical recording techniques are capable of achieving increased areal densities with less trouble. Bate estimates that an areal density of 50,000 bits/in and 20,000 tracks/in is the technology limit envisioned today. In comparison, the prototype disk starts out rather conservatively with an areal density of 15,825 bits/in and 6,350 tracks/in. Bate projects that a capacity of 100 Mbytes can be readily achieved by just increasing the track density to 15,000 tracks/in.

The company estimates the cost of the optical disk drive will range from $200 to $300 since many of the electronic components are borrowed from the compact audio-optical disk. Furthermore, the estimated media costs of $30 for the 3½" disk (also borrowed from the compact disk world) make it competitive with existing tape and rigid disk cartridges of similar capacity, as well as high-density floppy disks. Verbatim hopes to use the increasingly popular Small Computer System Interface (SCSI) as the drive interface. There is no word when production versions will be available.

—Aseo

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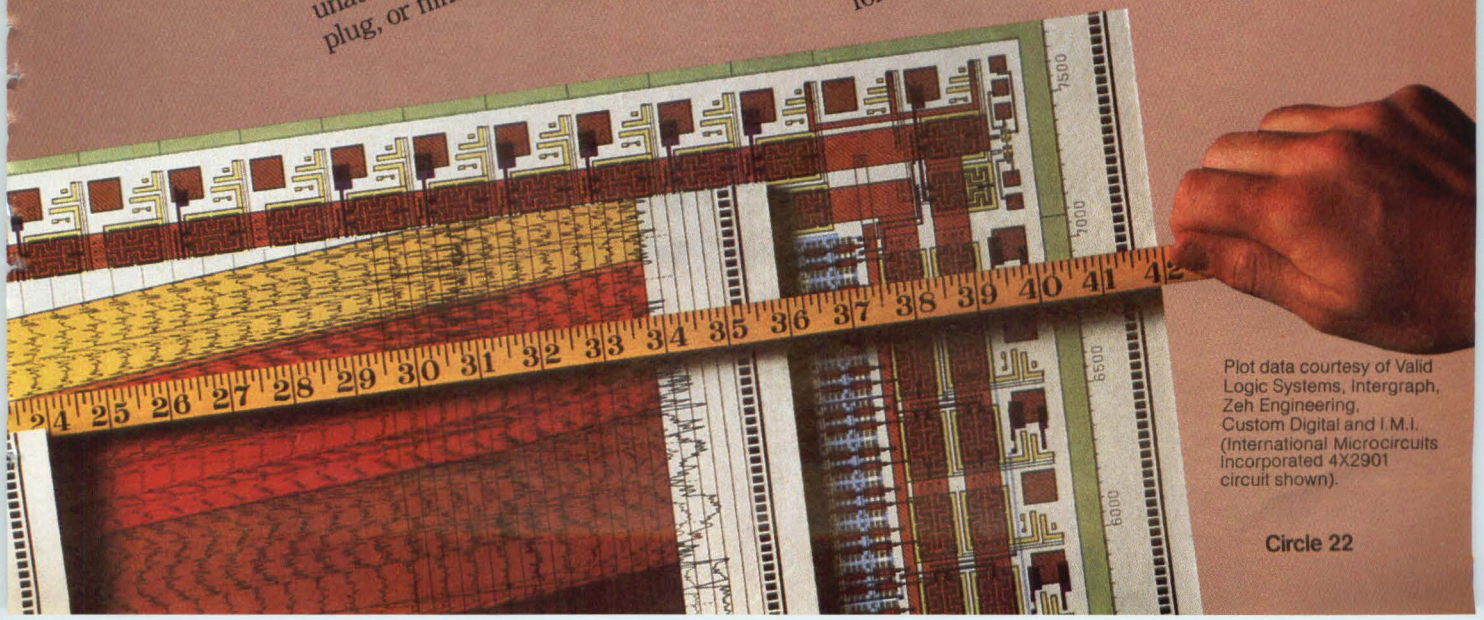
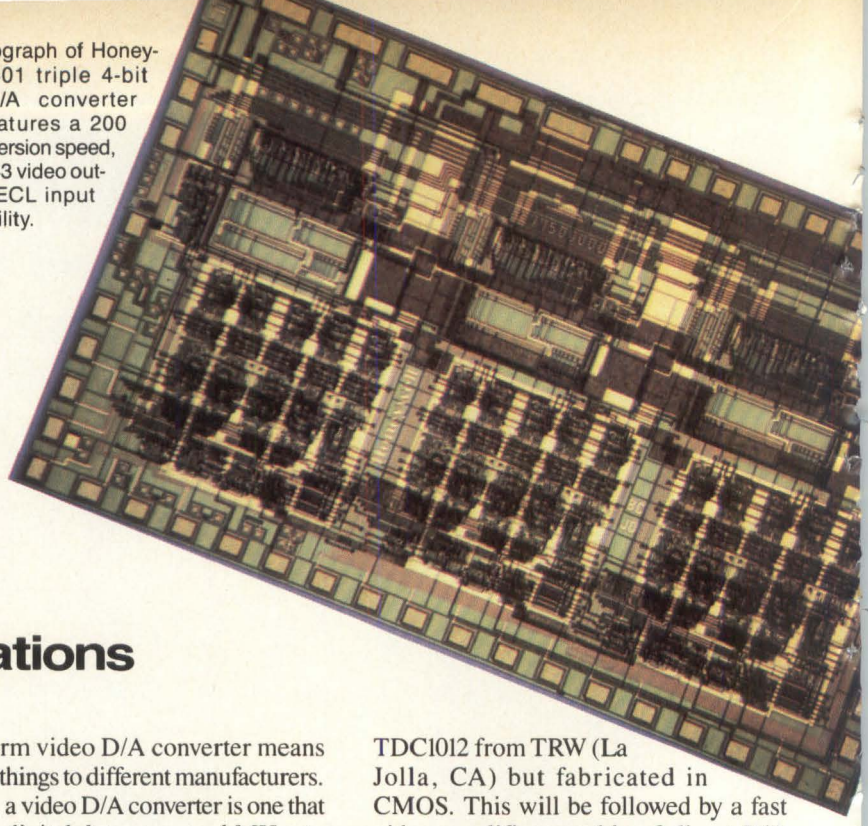


Plot data courtesy of Valid Logic Systems, Intergraph, Zeh Engineering, Custom Digital and I.M.I. (International Microcircuits Incorporated 4X2901 circuit shown).

Circle 22



Die photograph of Honeywell's 3401 triple 4-bit video D/A converter which features a 200 MHz conversion speed, RS330/343 video output and ECL input compatibility.

High-Speed D/A Converters Target Imaging Applications

Many different types of high-speed digital-to-analog (D/A) converter are available, implemented in both unipolar and bipolar technologies. Monolithic CMOS, hybrid video and high performance bipolar D/A converters may exhibit very different operational characteristics. **Table 1** shows five D/A converters introduced during the past month. Although not typical of the range of parts the companies offer, the chart does show the design diversity now available.

One of the most important parameters of a video D/A converter is speed, usually specified in MHz. For a 60 Hz noninterlaced 1024 × 1024 display, the scan rate is about 63 MHz. Thus, many manufacturers claim that a 65 MHz D/A converter is required to support such displays. But since the beam is blanked for 25% of the time for retrace, the pixel scan rate is about 84 MHz.

The term video D/A converter means different things to different manufacturers. To some, a video D/A converter is one that converts digital data at several MHz; to others, the output must be RS330/RS343 compatible. To add to the confusion, many high-speed D/A converters are current-output devices and require output op amps. These op amps, if incorrectly chosen, will slow system performance by orders of magnitude. Other considerations include resolution, trade-offs between bipolar and CMOS devices and differences between hybrid and monolithic devices.

One interesting introduction is a series of D/A converters developed in CMOS by Brooktree Corp. (San Diego, CA). In addition to the BT-102 in the table, the company will offer a series of video products by the end of the year. According to company president Jim Bixby, the first of these will be a 12-bit 30-MHz D/A converter similar to the bipolar 20-MHz TDC1012 from TRW (La Jolla, CA) but fabricated in CMOS. This will be followed by a fast video amplifier capable of direct D/A converter interfacing which will produce a 60V output with 1.5 nsec rise time. The company also plans to release details on a 250 MHz 8-bit bipolar D/A converter with ECL-compatible inputs. Brooktree has also signed a licensing agreement with Toshiba Corp. which will allow Toshiba to use Brooktree's technology to develop both 14- and 16-bit D/A converters for optical disk players.

At present, Bixby says, the main contenders for the 8-bit D/A converter market are the TDC1018 from TRW and the AD9700 from Analog Devices (Norwood, MA). Others poised to take a piece of the pie (*Electronic Imaging*, August 1984, p. 55) include Analogic Corp. (Wakefield, MA) with the AH-8308E 8-bit composite D/A converter with a maximum conversion rate of 150 MHz, Intech Corp. (Santa Clara, CA) with the 4TD hybrid D/A converter with three channels of 4-bit video output for RGB-type displays with up to 40 MHz conversion rate and Epitek (Ogdensburg, NY) with the EDH 13400 hybrid containing three 4-bit D/A converters each operating at 100 MHz.

As designers of high-performance, high-resolution display systems demand increased performance, high-speed D/A converter manufacturers will be forced to produce higher speed conversion products. As more manufacturers compete in this area, diversification will occur, producing products which will solve more than the display's conversion problem.

—A. Wilson

Manufacturer	Analogic	Analog Devices	Brooktree	Honeywell	TRW
Conversion speed	100MHz	150MHz	75MHz	200MHz	20MHz
Device number	AH8308TC	HGD-0805	BT-102	DAC3401	TDC 1012
Precision	Triple 8-bit	8-bit	8-bit	Triple 4-bit	12-bit
Fabrication technology	Bipolar	Bipolar	CMOS	Bipolar	Bipolar
Pin compatibility	TTL	ECL	TTL	ECL	TTL
Power dissipation	3W (max)	2W (max)	0.5W	1.8W	1W (approx.)
Output	RS330/343 75 Ohm	RS330/343 75 Ohm	RS330/343 75 Ohm	RS330/343 75 Ohm	40mA max. output current

Table 1: Five D/A converters have been introduced by semiconductor manufacturers in the past month. Although not typical of any range of parts offered by these companies, the table shows the various specifications of high-speed D/A converters.

Range Of Computer Vision Expanded By Artificial Intelligence

At the recent Conference on Computer Vision and Pattern Recognition in San Francisco, the importance of artificial intelligence (AI) to the latest work in machine vision was apparent. AI aids machine vision because an enormous amount of data must be processed and the relationships between the data are conducive to symbolic manipulation. Machine vision systems face the problem of comprehending new or ambiguous data or both. Applied AI systems are designed to learn from and discern imperfect information.

Computers' ability to extract useful information from visual data is widely used in the automotive and aerospace industries. Machine vision is critical in robotics for understanding depth, shadows, movement and hidden objects. Other applications are remote sensing, and geophysical and biomedical analysis.

Machine vision is being used in some surprising applications, including a system discussed at the conference for automatic lip-reading from facial movements. Eric Petajan, now at AT&T Laboratories in New Jersey, did the work through the Computer-based Education Research Laboratory at the University of Illinois at Champaign-Urbana. A 68000-based computer combined with a Voterm II voice recognition system was used. The system analyzes a 244 × 248 pixel image at 60 Hz, representing 6.25 Mbytes for an utterance of 1.25 seconds. Predictive differential quantizing (PDQ) was used for data reduction. PDQ is a compromise between run-length encoding and contour tracing. It allows the coding of multiple gray level images and computes region parameters efficiently.

Another application for machine vision is automatic analysis of electrophoretic gels, developed by Michael Skolnick of Rensselaer Polytechnic Institute. It takes an expert about 20 minutes to analyze ambiguous gray spots. Implementing AI techniques, computer analysis takes less than 5 minutes. The expert system builds a model of the visual environment and the symbolic relationships within. Decisions are made by a matching algorithm which creates a pattern of hypotheses. The rules are applicable in any environment where image comparison is of interest.

A direct AI-based application is the classification of galaxies being studied at INRIA in Valbonne, France. The enormous amount of data is difficult for humans to compare and classify. Several expert methodologies were tested, including fuzzy pattern matching. Fuzzy set theory, introduced in 1965, has been applied to a broad spectrum of problems in set theory and lately in pattern recognition. Fuzzy reasoning is based on relationships that are "certain" or "possible." The results are determined according to the proximity of a tested pattern to the threshold of a rule. A fuzzy prototype may be thought of as a simple knowledge base consisting of fragments of procedural and declarative knowledge. The INRIA prototype of information about galaxies is information based on "likelihoods." The expert system featuring fuzzy pattern matching can classify one galaxy in 180 seconds.

Some of the computer vision problems that use AI for recognition and analysis are shape determination, motion analysis, 3D object construction, stereo vision, contour analysis, optimal path routing and character recognition. A moving object, potentially behind other objects, must be completely understood. This means that the definition of a 3D object must include what cannot be seen. The software must be able to create the object using conventional solid modeling technology. The AI program must be able to generate a description of the object in CSG (constructive solid geometry), B-rep (boundary representation) or a hybrid of several techniques.

Another example of the combination of AI and computer vision, in use at Martin Marietta Corp., is a rule-based system for pattern recognition that exploits topological constraints. The research for this aerospace application was done by Mitchell Nathan at Martin Marietta and Michael Magee at the Artificial Intelligence Laboratory at the University of Wyoming. Edge types that join at functions form higher level objects. From this fact, a set of rules is developed that describes known models. Object recognition by the processor is rule-driven. Facts are asserted (or unasserted) through deductive rule checking. Two sets of rules are used. Topological rules are based on how junctions, edges and surfaces exist in a planar, trihedral world.

Rules based on models, however, are application driven. They build on topological rules and describe how anticipated objects would appear. The interaction of the two theories produces the knowledge base. The results are promising. When line segments are missing, the system can hypothesize the location of the missing features in an image, so a complete image can be constructed from incomplete information. The process is automated further by autogenerating model descriptor rules and expanding the system's knowledge base to include curves and more complex objects.

The increasing use of AI in machine vision is going to translate into different hardware and software tools for research and applications. Many researchers are presently using conventional VAX hardware and C software. However, they are now turning to Symbolics and LMI hardware and implementing their programs in LISP or Prolog.

— MacNicol

Standard Cells Pave Road To Systems On Silicon

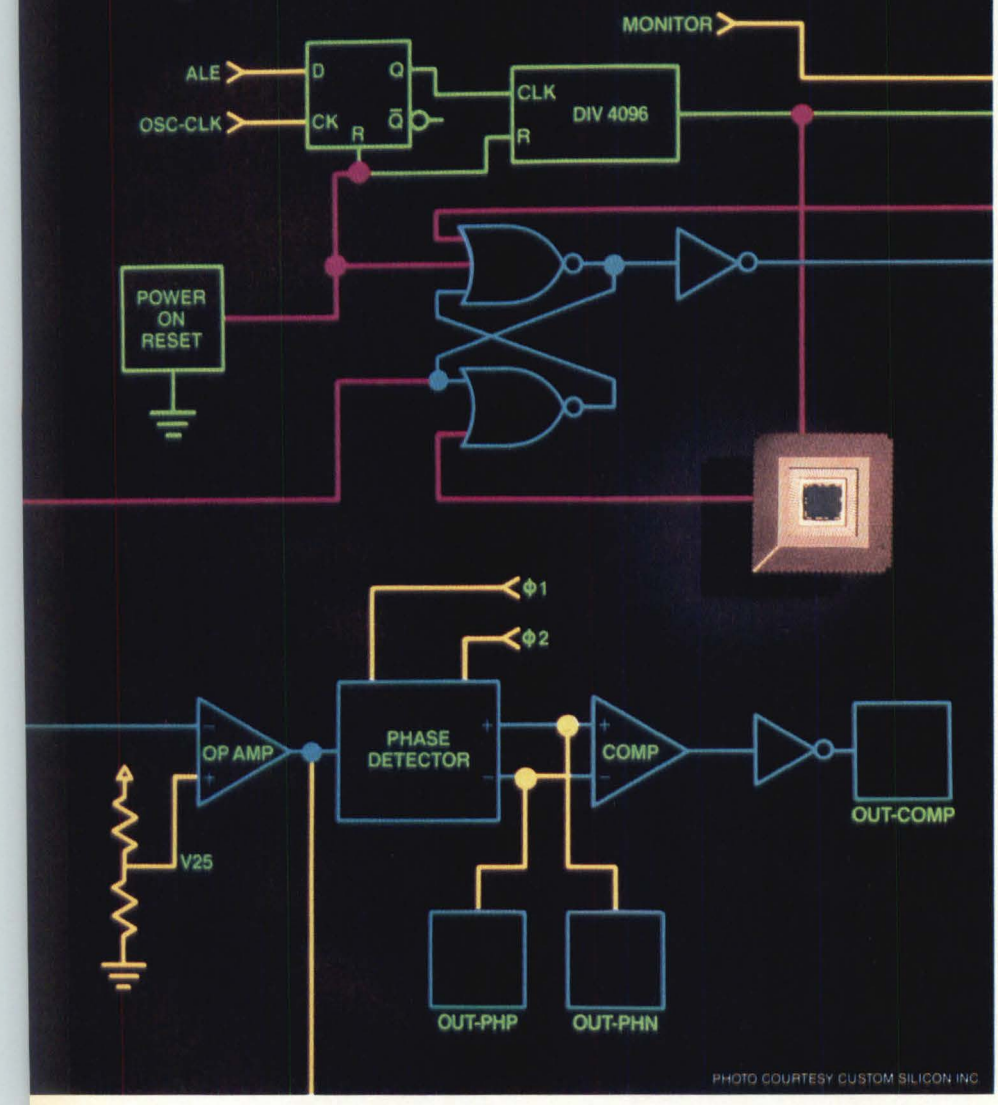


PHOTO COURTESY CUSTOM SILICON INC

by Ronald Collett, Sr. Technical Editor

Microprocessors, analog circuitry, LSI functions, various types of memory and glue logic are now part of many standard cell libraries. As a result, systems once consuming several boards are being put on a chip. Because of the complexity of these cell-based designs, semiconductor vendors must also supply sophisticated CAD/CAE environments. IC fabrication technologies, however, continue to outpace the CAD/CAE tools necessary to fully automate the design of single chip systems.

When CAE tools fall short, gaps are often bridged by manual methods, causing design cycles to become lengthy. Creating the numerous test patterns for verification of these VLSI devices is an example of a CAE void. Manual test vector generation often consumes a large portion of the design cycle. Routing of highly integrated cells that have irregular dimensions is another task that often requires manual intervention. Automatic routing software for these LSI and VLSI functions is an area under development. Simulating circuits that include both analog and digital circuitry is also a major problem. Presently, there are no simulators that adequately handle mixed mode simulation.

Standard Cell Design

From the designer's viewpoint, there are no differences between the gate array design cycle and the standard cell design cycle (**Figure 1**). Using either technology, designers work from the IC vendor's cell library, use similar verification tools and maintain a close relationship with the IC vendor. Hence, both standard cells and gate arrays can be grouped together as semicustom devices.

From a manufacturing standpoint, however, gate arrays and standard cells are very different. Gate arrays require only one to three customized masks during the fabrication process. These last few masks are used to connect the predefined rows of gates. Standard cells, on the other hand, demand a full set of up to 12 customized masks since there are no predefined gates on the die. Another difference between the two technologies is turnaround time; standard cells typically require 8 to 12 weeks for prototypes and another 8 to 12 weeks for production parts. Gate array prototypes are usually ready in 4 to 8 weeks with production parts available in another 6 weeks. Despite the higher number of masks and longer turnaround time, most designers view standard cell devices as semicustom rather than full custom.

Standard cell libraries that include PLAs, memory, microprocessors and analog functions offer the most architectural design flexibility. However, prices rise dramatically when complex functions are integrated onto the chip. Non-recurring engi-

The central issue surrounding standard cell technology is whether the CAD/CAE tools can support single chip system design.

neering (NRE) costs for standard cell designs range anywhere from $25,000 to $140,000, and these figures do not include computer charges. Large volumes are necessary to absorb the higher cost. One way to circumvent computer charges is to use a workstation. Most standard cell vendors support either Mentor Graphics (Beaverton, OR), Daisy (Mountain View, CA) or Valid Logic (San Jose, CA) workstations. Among the factors contributing to higher prices are the cost of building a full set of masks, computer time for simulation and routing, the IC vendor's engineering charges and developing special test hardware and test software.

Traditional standard cells have fixed heights and variable widths, contrasting to gate arrays, whose cells have both dimensions fixed (**Figure 2**). Variable width permits greater optimization of die area, which is the key parameter in any customized chip. The common standard cells found in most vendors' libraries include SSI and MSI components. But since many functions are larger than standard size cells, they do not conform to the fixed height/variable width concept. Routing considerations come into play because of the functions' irregular rectilinear dimensions; UARTS, RAM, ROM and core microprocessors are examples of LSI and VLSI blocks often demanding special attention.

An additional routing stage is necessary to incorporate these irregular shaped functions into a standard cell design. Automatically wiring large blocks to the other sections of the chip requires a block router, which connects macrocells having nonstandard dimensions. When block routers are unable to complete the job, manual routing techniques are used. As might be expected, designs needing hand routing can take longer to complete (days or weeks depending on the routing complexities) than those done with automatic tools.

Before layout, the design is simulated using fixed timing delays. With these timing models, designers get a rough idea of how the chip will function after layout. At this point, critical paths are identified to receive special attention during the layout phase. Once the chip undergoes placement and routing, actual wiring delays (i.e., layout capacitances) are extracted from the layout and used in the resimulation of the design. Back annotation of these layout capacitances is especially important in CMOS designs because device delays are a function of capacitive loading.

Unlike gate arrays, fixed height/variable width standard cell designs are always 100% routable. A gate array's wiring channels have fixed widths, often making 100% routing impossible. Standard cell routers simply extend the width of a routing channel if it becomes too congested. An increased die size occurs when channels are enlarged. And the larger the die, the more expensive the chip.

Placement and routing is a crucial stage in the design cycle since it directly determines the circuit's timing. Because this phase of the design cycle is so important to producing a working chip, most vendors prefer to do the layout themselves. At the same time, most logic designers are unfamiliar with IC layout and often choose not to get involved. One drawback of being removed from the layout stage is a loss of control. Although this is not a major problem, any time a design is out of the creator's hands the possibility of a design error increases. Standard cell designers will eventually assume responsibility for layout as they become better acquainted with semicustom technology.

A widely used standard cell automatic placement and routing

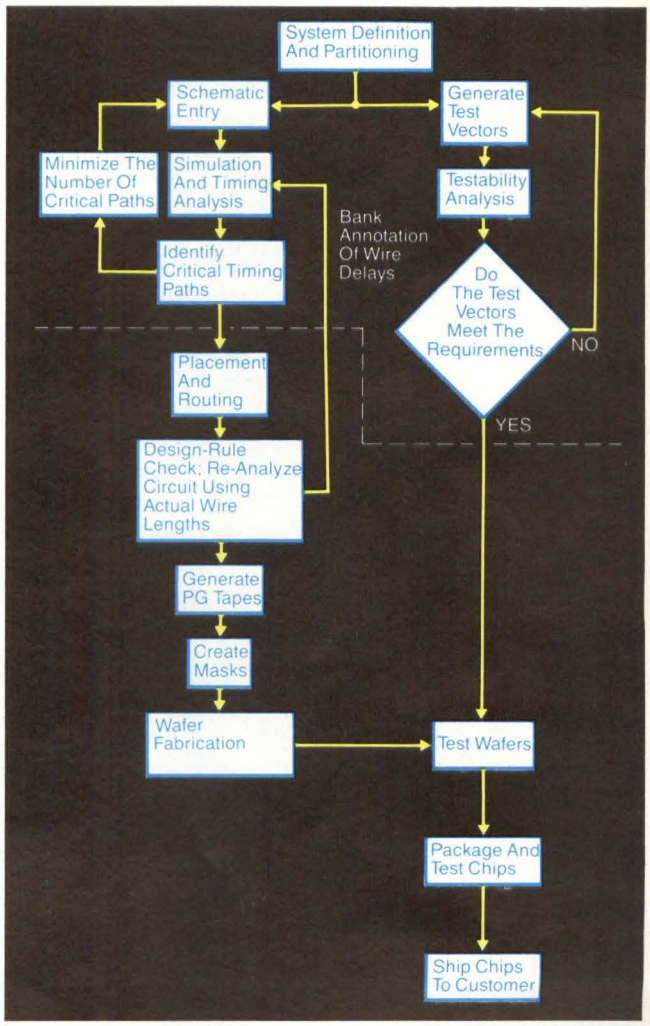


Figure 1: From the designer's perspective, there is little difference between the gate array design cycle and the standard cell design cycle. The flow chart shown applies to either methodology. From the mask maker's viewpoint, however, the two differ sharply because standard cells require 10 to 12 customized masks, whereas gate arrays need only 1 to 3 levels of customization.

layout package is CAL-MP from Silvar-Lisco (Menlo Park, CA). The package's three main programs are Place, Interact and Route. Place is used for either interactive or manual cell placement; Interact allows designers to modify autoplaced cells; and Route does the automatic routing between cells. CAL-MP is technology independent and is designed to lay out CMOS, bipolar and p- and n-channel MOS circuits. Its other capabilities include 2- or 3-layer routing, routing of cells that are more than one row high (like memory), routing of rectangular cells with variable dimensions, automatic power and ground routing, cell placement between pads, manual preplacement of critical cells and back annotation of layout capacitance.

CAL-MP runs on IBM's 3000 and 4000 systems under the VM/CMS operating system, DEC's VAX under VMS and on Prime and Apollo computers running under PRIMOS and AEGIS, respectively. Interface programs are available to merge CAL-MP's database with remaining integrated circuit layers on a custom layout station to produce pattern generator (PG) tapes for mask making. In addition, interface programs are available for producing Calma's GDS-II and CIF.

Two standard cell automatic layout systems aimed at competing with CAL-MP are CellPlus from Calma (Milpitas, CA) and StandardEdge from SDA Systems (Santa Clara, CA). Unlike CAL-MP, CellPlus is tailored to the design rules of specific semiconductor manufacturers. Motorola (Phoenix, AZ) is the first vendor to sign an agreement allowing Calma access to its proprietary design rules and process information; technology transfers with other IC makers are reportedly underway.

CellPlus uses several place-and-route algorithms that lay out both fixed height/variable width standard cells and variable height/variable width cells (**Figure 3**). It includes an automatic standard cell placer and router, interactive placement and routing editors, connectivity and design rule checkers and post layout delay analysis utilities.

One problem with auto-place-and-route software is the huge quantity of data that must be manipulated. As designs become more complex, automatic placement and routing tools frequently get bogged down. To minimize the amount of data that SDA's StandardEdge must handle, the system uses abstract representations containing bounding boxes and pins, rather than complete cell layout geometries. This increases speed and efficiency since the system handles less graphics data.

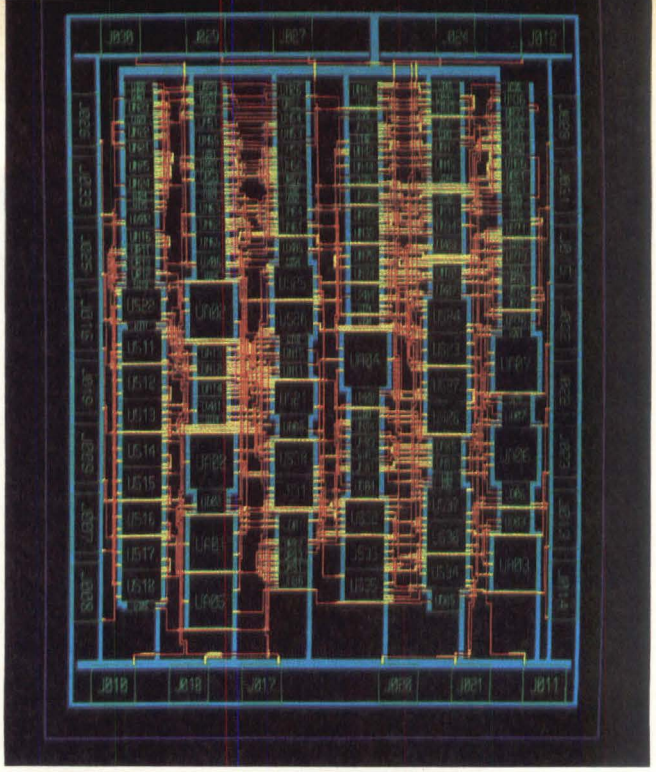


Figure 3: Calma's recently announced CellPlus standard cell layout software is the first commercially available package tailored to the design rules of specific IC vendors. Several place-and-route algorithms enable CellPlus to lay out both fixed height/variable width standard cells and variable height/variable width cells.

System = Analog + Micros + Macros + Memory

Until now, only a few IC vendors offered all of the cells necessary to put a complete system on a chip. Recently, however, several semiconductor manufacturers upgraded or introduced libraries that include analog circuits, memory cells, LSI functions and core microprocessors.

NCR Microelectronics (Fort Collins, CO) and Zymos (Sunnyvale, CA) were among the first standard cell vendors offering core micros in their libraries. NCR has an enhanced version of the CMOS 65C02. Designated the 65CX02, the cell has 59 additional op codes including 14 new instructions and two additional addressing modes (**Figure 4**). Bit manipulation instructions were added to facilitate software control of memory-mapped I/O and control registers. Zymos offers the 80C48 and 80C49 processors, which are pin compatible with Intel's (Santa Clara, CA) off-the-shelf versions of the parts (**Figure 5**). The 80C51 is also under development at Zymos. The core micros have a 1.36 μsec instruction cycle time while running at 11 MHz and consuming 12 mA. Zymos recently introduced a 2-micron CMOS library with 1 nsec gate delays, for clock frequencies of 30 to 35 MHz. NCR's 65CX02 operates at up to 3 MHz and consumes as little as

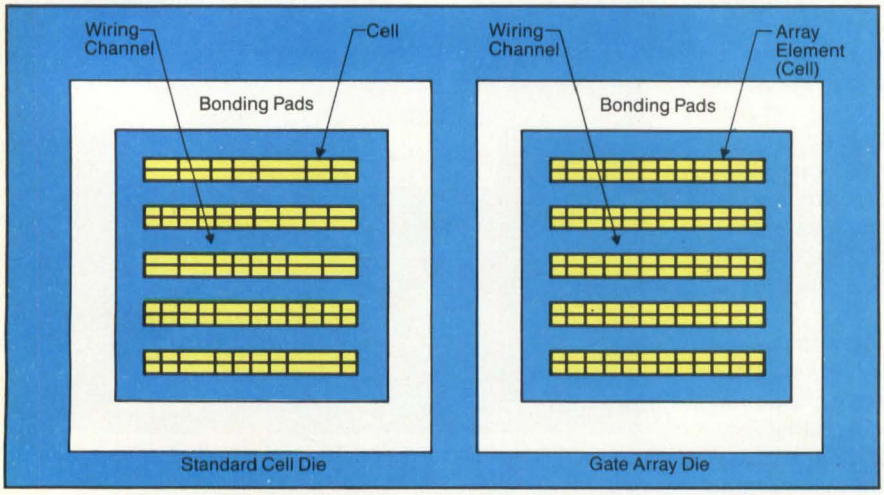


Figure 2: Traditional standard cells have fixed heights and variable widths. In gate arrays, the basic cell has a fixed height and a fixed width. When defining a logic function on a gate array, a complete cell must be accessed whether or not all the transistors within the cell are used. Since all of the masks in a standard cell design are customized, 100% of the transistors are utilized.

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Testing core microprocessors is a central issue in designs based on these VLSI devices. Imbedded processors present problems for several reasons. First, the processor is typically buried deep within the chip's surrounding logic, so exercising the CPU becomes difficult when peripheral logic is complex. Since many of the processor's I/O pins are not brought out to the chip's external pins, test points are less than optimal. To exercise the processor, designers and test engineers must develop complex test vectors that penetrate peripheral circuits. Another difficulty is that the complexity and size (in terms of gate count) of a processor-based standard cell device requires a huge number of vectors to adequately test the logic. As many as 50,000 to 100,000 vectors may be necessary to test such a design.

Developing the quantity of patterns needed to test a VLSI standard cell device requires a significant effort. Almost all manufacturers require customers to assume complete responsibility for this task. Many of the design problems detected after a chip is fabricated are the result of inadequate test vectors. When test vector development is given second priority to design, particularly subtle problems often go undetected.

Both NCR and Zymos are putting significant effort into test development to facilitate testing of core processor-based designs. Intel (Chandler, AZ), a firm expecting to become heavily involved in the standard cell market by early 1986, is also addressing the test issue. The first processors Intel is offering in its library are the 80C49 and 80C51. Both devices are modified versions of the company's standard products. A ring of test logic and buffers replace the bonding pads and pad logic. This isolates the core cells from the rest of the logic and permits separate testing.

NCR has a unique method of interfacing to its customers who do not work out of the Colorado facility. Instead of establishing company design centers, NCR offers its tools, technology and fabrication facilities to independent firms. By doing this, NCR claims it can focus its efforts on fabricating semiconductors. Design support is left to the independent design houses.

An advantage of working with an independent design shop is that there is usually a tighter interface between the customer and independent. Moreover, independents typically find that supplying the customer with engineering support is in the best interest of both parties, since it often leads to a more rapidly completed chip that is less likely to have a design flaw. One firm under agreement with NCR is Custom Silicon Inc. (Lowell, MA), one of the first to offer a cell library on the IBM PC. The library runs on Futurenet's (Canoga Park, CA) Dash workstation.

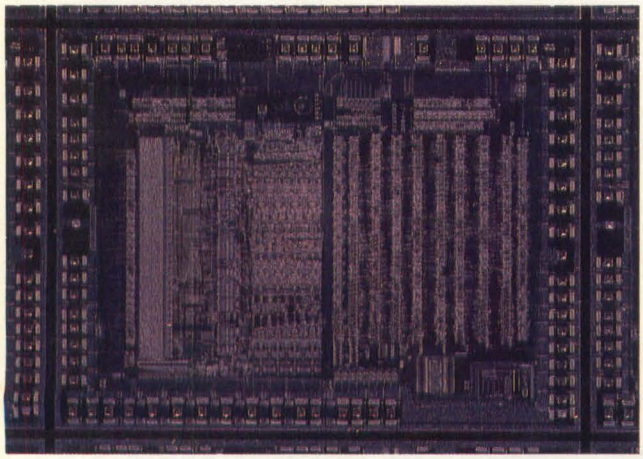

Figure 4: This standard cell design from NCR Microelectronics controls the movements and generates the sound for a programmable toy robot that walks and talks. The chip was designed using analog cells, ROM, RAM and a 65CX02 core microprocessor.

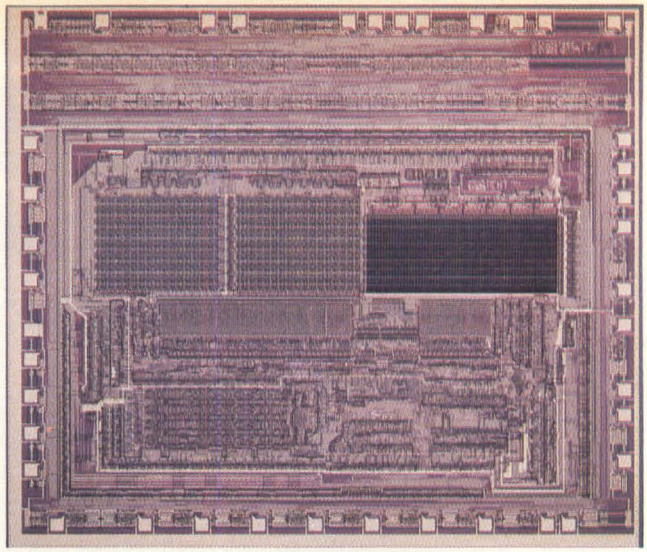

Figure 5: Zymos offers memory, analog cells, LSI functions, glue logic and core microprocessors in its cell library. Shown is a design based on the 80C49 core processor.

Other firms offering libraries on IBM's PC include Gould American Microsystems Inc. (AMI) (Santa Clara, CA), and Matra Design Systems (Santa Clara, CA). AMI's PC-based software package, designated SCEPTRE II, performs simulation with a 10-state event driven MOS logic simulator, placement and routing, timing analysis, layout verification and netlist generation. Gould AMI offers a Z80 CPU and is investigating including others in its library. Emphasis has also been on bringing up its 2-micron HCMOS library and increasing the number of analog cells and LSI macrocells. An 87 stage ring oscillator was recently fabricated using the 2-micron process which exhibited propagation delays of 460 psec/gate with a fanout of 1, operating at 5V.

Matra's PC-based system offers 18-state logic simulation, testability analysis software, fault simulation, automatic place-and-route tools, design rule checking and back annotation of wiring delays from the actual layout. The firm also has a software package that automatically converts programmable logic device (PLD) designs into standard cell designs.

AMI, NCR and Zymos each offer a wide selection of analog cells. NCR's analog capabilities include comparators, 8-bit A/D and 8-bit D/A converters, a general-purpose operational amplifier, an analog switch and current bias generators. One area that AMI specializes in is switched-capacitor filter design (**Figure 6**). The filter shown is constructed using a switch array cell with external capacitor cells and an operational amplifier cell. Either high-pass or low-pass filters can be designed by simply eliminating the appropriate capacitor. (For high pass filters, C1=0; for low pass filters, C2=0.)

One of the most popular devices currently in use is Advanced Micro Devices' (Santa Clara, CA) 2901 bit-slice CPU. Until now, the 2901 was available only as an off-the-shelf component. Although the part is used when high speed is a primary requirement, its performance advantages are frequently offset

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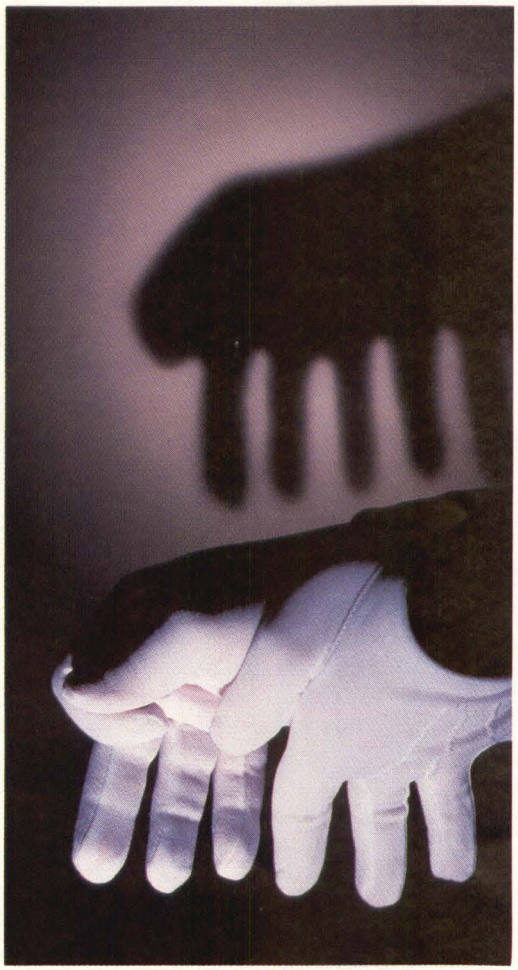

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by high package counts and lengthy interconnect wiring between the processors and peripheral devices. General Electric Semiconductor (Research Triangle Park, NC), LSI Logic (Milpitas, CA) and WaferScale Integration (Fremont, CA) are providing a solution by offering functionally equivalent CMOS 2901-based core processors in their standard cell libraries.

Limited only by chip size, General Electric's GE2901 and GE 2910 cells can be configured to form a processor of any bit length that is a multiple of four. CMOS chips are usually slower than their bipolar counterparts because as interconnect wiring lengthens and fan-out rises, capacitance increases, causing longer delay times. However, by integrating multiple 290ls onto a chip, interconnect wiring is minimized and performance is vastly improved. When four GE290ls are configured to form a 16-bit bit-slice processor together with the GE2910 microprogram controller, the resulting core processor yields 100 nsec cycle times. GE's cell library is based on a 2-micron technology that yields 1.7 nsec (fan-out =2) gate delays. Other 2900 family members in GE's cell libary include the 29C03, the 29C09 and the 29C11.

WaferScale Integration is providing designers with 4-bit, 16-bit and 32-bit bit-slice CPUs, all based on the 2901 and fabricated in 2-micron CMOS. Designated the 59C032, the 32-bit machine runs at 15 MHz, includes a scratch pad 32-word × 32-bit static RAM, has a datapath delay time of 82 nsec and dissipates 300 mW. In comparison, eight off-the-shelf 4-bit bipolar 290ls linked together to form a 32-bit function has a datapath delay of 91 nsec and dissipates over 12 W. The 2902, 2904, 2909 and 2913 as well as CMOS EPROM cells, with sizes ranging from 64 bits to 64 Kbits, are also available in WSI's library. Like several other vendors, WSI's library runs on DEC's VAX, Daisy's workstation and IBM's PC AT.

International Microelectronic Products (IMP) (San Jose, CA), a firm specializing in both handcrafted full custom and standard cell design, includes one-time programmable PROM cells in its library. The PROM is based on a programmable contact technology, as opposed to either blown fuse or blown junction transistors. IMP's current 2-micron technology produces 4 nsec gate delays, but a 1.25 micron library that will yield gate delays of 1.2 nsec is under development. IMP is also putting significant resources into cell compilers development. Until now VLSI Technology Inc. (VTI) (San Jose, CA) has been one of the few companies offering cell compilers. However, IMP recently completed a RAM compiler and a pad compiler. The

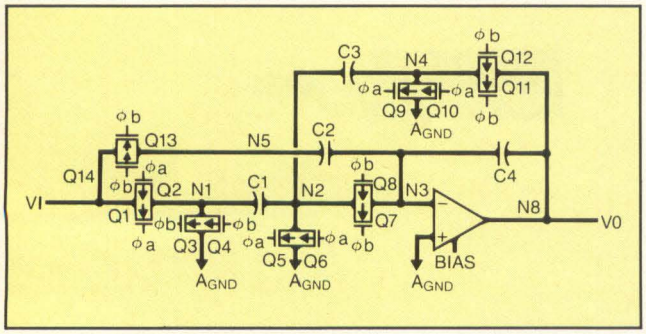

Figure 6: Switched-capacitor filters can be constructed easily with Gould AMI's library. The filter is designed using three cell types: a switch array, an operational amplifier and capacitor cells. Eliminating C1 results in the formation of a high-pass filter, eliminating C2, a low-pass filter.

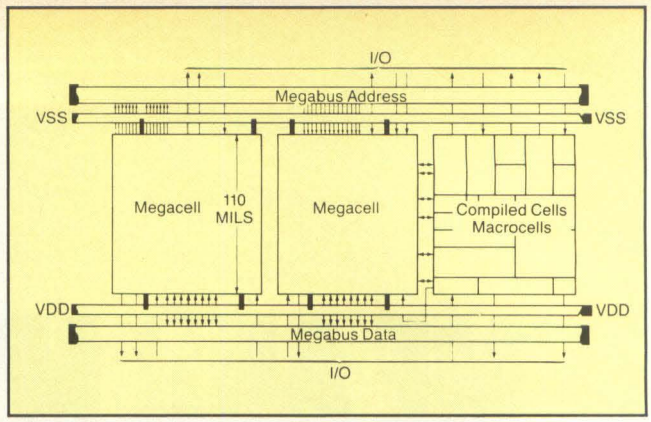

Figure 7: VLSI Technology's Megacells are equivalent to standard cells since they have fixed height and variable width. To further optimize chip area and design time, VTI's megacells are interconnected via an address bus and data bus architecture.

RAM compiler allows designers to construct an n × n-sized RAM by simply specifying the dimensions. Similiarly, the pad compiler generates a wide range of I/O circuit variations. IMP is working on a ROM compiler and a PROM compiler and is set to introduce a new analog cell library.

VLSI Technology started out offering strictly cell compiler-based designs; however, the company has expanded into gate arrays, programmable logic and Megacells – a fixed height/variable width technology. Die area is optimized by interconnecting Megacells, macrocells and cell-compiled functions via an address and data bus architecture (**Figure 7**). VTI claims that this busing approach results in greater silicon efficiency than traditional methods. The following Megacells are included in VTI's library: the 6845 HMOS and 68C45 CMOS controllers; 16K, 32K, 64K 128K HMOS ROM; the 82C54 CMOS counter/timer; the 82C84 CMOS clock generator; the 82C50 UART; the 82C59 interrupt controller; the 82C88 CMOS bus controller; the 82C37A CMOS DMA controller; and the 65C02 CMOS microprocessor.

An established gate array manufacturer, LSI Logic is attacking the application-specific IC (ASIC) market with a three-prong strategy. Aside from the firm's gate array business, LSI Logic is introducing structured arrays, standard cells and structured cells. LSI Logic's standard cells are shrunken versions of the firm's gate array cells. Structured arrays are gate arrays that, in addition to an uncommitted sea of gates, have a core processor or some other large cell prefabricated on the chip.

Structured cells are aimed at applications demanding high performance and the utmost architectural flexibility. Bit-slice (2901) processors, multipliers, multiplier/accumulators, register files and multiport RAMs are among the cells available to designers using this technology. Although many functions in the structured cell library could be implemented using LSI Logic's standard cells, more die area would be consumed. Comparing technology performance, system frequency speeds are 40 MHz for the company's LL7000-series of high performance gate arrays and 50 MHz for structured cells.

LSI Logic is also introducing LDS IV, an upgrade of the LDS III development system that now includes linking software. The design methodology of structured cells revolves around simulating large complex blocks independently. Once the blocks are simulated, the various sections of the chip can be linked, compiled and simulated. Since LDS IV includes linking software, the circuit does not have to be recompiled each time a small change is made in the logic.

Ricoh (San Jose, CA) is the only firm currently offering standard cells that combine bipolar and CMOS components on the same chip. Operational amplifiers, A/Ds, D/As and comparators are among the devices Ricoh will incorporate onto a standard cell design. Also available are CMOS EPROM cells, SRAM cells, DRAM cells and PLAs. A 65C02 core microprocessor is expected to be introduced in the fourth quarter.

Texas Instruments (Dallas, TX) offers a 3-micron library with over 250 cells including RAMs, ROMs, PLAs and ALUs. Harris Semiconductor (Melbourne, FL) offers a wide selection of macro functions in its standard cell library. Among the cells available are the SM4702 programmable bit rate generator, the SM6402 UART, the SM82C37A DMA controller and the SM6406 programmable asynchronous communications interface. Other companies providing standard cell libraries are Mostek (Carrolton, TX), Fujitsu (Santa Clara, CA), Silicon Systems (Tustin, CA) and National Semiconductor.

Looking Down The Road

Once a hope of the future, systems on a chip have arrived and standard cell vendors are racing to provide customers with as wide a selection of cells as possible. With the multitude of vendors providing standard cell technology, the competition is fierce. Aside from the extensive range of cells currently under development, vendors are in a heated battle over performance. Most are developing 2-micron libraries, but during the next 18 months many manufacturers will begin work on cells with feature sizes in the 1-micron range.

Meanwhile, the tremendous number of variations of a particular function are driving many vendors into the development of cell compilers. Although only a few have made announcements, many have cell compiler projects underway. Cell compilers that generate RAM, ROM, I/O pads and shift registers are usually among the first to be developed because the size of these cells varies with each design. Rather than building every variation of a function, vendors are finding it much easier to shift their efforts toward cell compiler development.

A wider variety of core microprocessors will also be available soon. LSI Logic, for example, may offer Texas Instruments' TMS320 single chip digital signal processor in its structured cell library. Intel will be adding several of its more advanced processors to its cell library. And several other manufacturers who currently do not offer processors are testing the market and will soon include micros in their libraries.

As far as analog cells are concerned, only a handful of vendors offer linear capability. Of those, most have the basic functions such as op amps and comparators, but a few provide A/D and D/A converters. Over the next 18 months, flash converters and a variety of other analog cells will be introduced. DD

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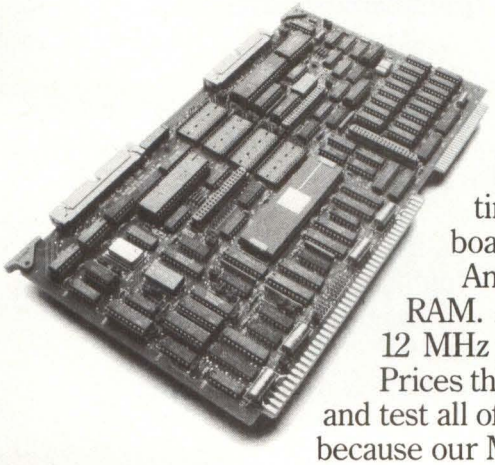

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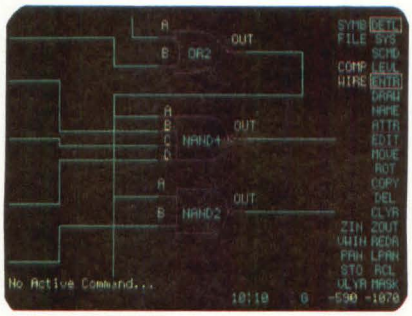
PART 1

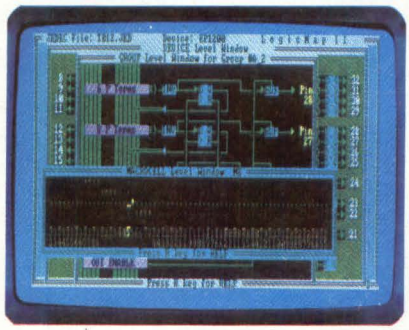
Erasable Programmable Logic Devices Simplify Logic Design

by Clive McCarthy, Altera Corp.

Erasable programmable logic devices (EPLDs) have opened up a new level of versatility in logic design. They permit engineers to integrate digital circuit functions quickly and efficiently onto fewer devices. At the same time, using EPLDs does not involve the high costs and long lead times associated with full custom or semicustom alternatives. EPLDs are devices that, like EPROMs, can be programmed to implement virtually any logic function, erased with ultraviolet light and reprogrammed. Both the programming and reprogramming take place in the customer's facility, under complete control of the designer.

This article—the first in a two-part series—focuses on EPLD technology and internal structure as well as comparisons to other technologies. The second part of the series will examine design methods for use with EPLDs.





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Programmed EPLDs can replace many SSI/MSI parts; the actual number of parts replaced depends on the number of equivalent gates provided by the device. But whatever its capacity, the programmable device requires far less board space than an equivalent discrete-logic circuit. And because one EPLD can implement a wide variety of logic devices, designers do not need to stock each discrete logic device that might be needed. This reduces production costs.

User-Defined Logic Alternatives

TTL devices, gate arrays and custom circuits are part of the overall logic design picture, of which EPLDs constitute the latest development. Implementing a design in custom or gate-array technology involves customization of the wafers during manufacturing. When completed these customized devices can be used to implement complex logic circuitry as well as to minimize per-unit costs if a large number of devices is needed.

However, developing a standard-cell, gate-array or full-custom device entails significant development costs and long prototype lead times. For example, full-custom development typically costs between $50,000 and $250,000 for each design, with a nine to eighteen month prototype lead time. Employing a cell library lowers these figures to a range of $30,000 to $90,000 and a four to six month lead time; gate arrays push development costs down further to the $10,000 to $40,000 range with a one and one-half to five month lead time. If changes are required in the design after initial fabrication, the production cycle lengthens further. And once the devices have been manufactured, they must be stocked by the user as dedicated inventory.

Fuse-programmable logic devices were developed to avoid some of these drawbacks. With fuse-programmable PLDs, instead of developing a logic design and sending it to a custom-chip foundry, designers program the chips in the field by blowing PROM-like fuses. This approach reduces lead times to a few hours and cuts the entry price to about $3 to $25 for simple to moderately complex PALs*; complex devices cost as much as $200. Users can also stock one type of device that can be programmed to act as many different circuits. Fuse-programmable PLDs are available under the trademark PAL and the generic name programmable logic array (PLA).

Despite their advantages, fuse-programmable PLDs have some of the drawbacks of PROMs. For example, the bipolar technology used consumes a large amount of power and limits the number of gates that can be incorporated. Additionally, manufacturers cannot fully test fuse-programmable devices; fuses can be blown only once, so it is impossible to know before programming whether the device will function correctly.

Overcoming Fuse-Programmable Limitations

Just as CMOS EPROMs overcome the power and programming

*PAL is a trademark of Monolithic Memories Inc.

Clive McCarthy is Director of Applications for Altera Corp. in Santa Clara, CA.

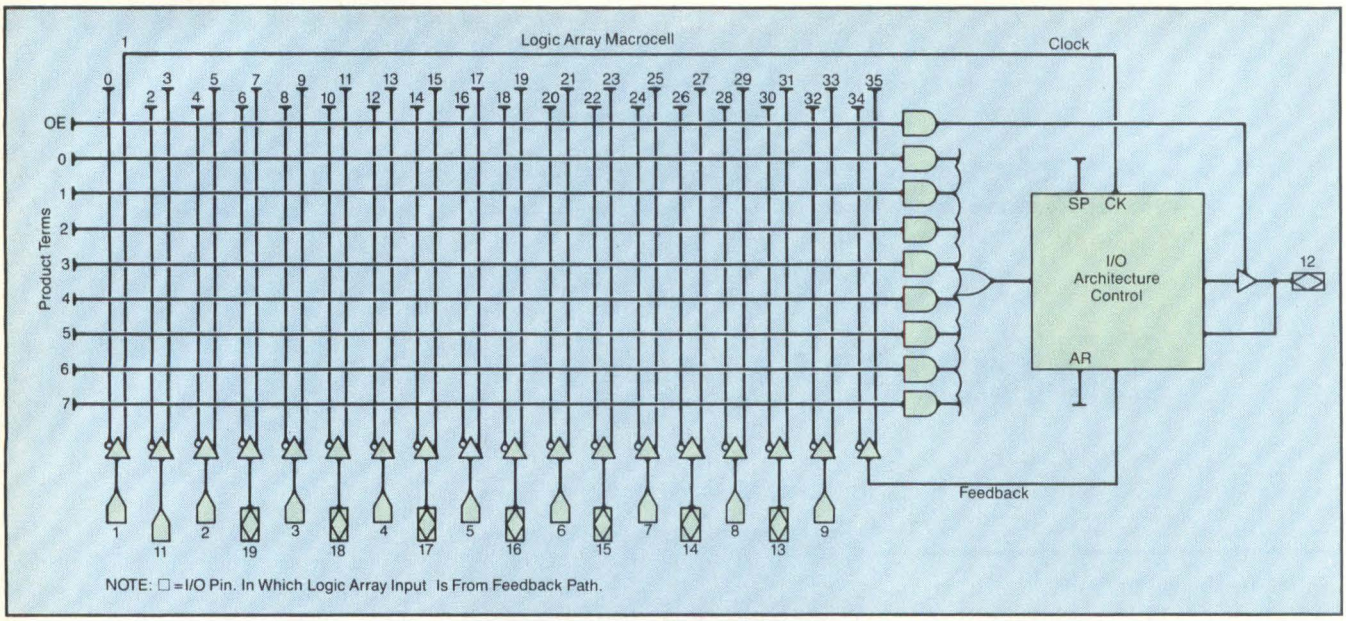

Figure 1: One macrocell shows that the structure underlying any EPLD consists of an EPROM-like memory array that controls I/O circuitry. An electrically programmable transistor lies at the intersection of each line in the array. This diagram illustrates one of the eight macrocells in Altera's EP300.

limitations of bipolar PROMs, CMOS EPLDs solve many fuse-programmable PLD problems. CMOS technology reduces power dissipation drastically. For example, a fuse-programmable MegaPAL from Monolithic Memories Inc. (Santa Clara, CA) and Altera's CMOS EP1200 EPLD contain about the same number of equivalent gates* and operate at about the same speed, but the power dissipation of the MegaPAL is rated at 3.3W standby and active, whereas the EPLD dissipates only 15 mW standby and 400 mW active. The EPLD device is also smaller and less expensive than the fuse-link device.

In addition, the CMOS EPROM cells in the EPLD can be erased using ultraviolet light. Manufacturers can therefore perform complete functional tests before shipping. Erasability also permits users to correct their design errors or change logic designs in the middle of a production cycle without the expense of throwing away previously programmed devices.

An inherent advantage of CMOS is that a CMOS EPROM cell is significantly smaller than a bipolar fuse-based cell. A state-of-the-art EPROM bit occupies only 36 square microns, while a state-of-the-art fusible-link bit takes 513 square microns of silicon area. CMOS therefore offers a much better potential for high gate densities at low cost. Moreover, advances in CMOS such as Intel's CHMOS II-E process (available to Altera through a technology exchange agreement) provide the basis for EPLDs that operate at TTL speeds but with about 80% less power. The integration density made possible by CHMOS allows EPLDs to offer a true alternative to gate arrays.

Design security is another CMOS advantage. It is possible to decipher the design implemented in a fuse-programmable device by prying it apart and examining the fuse pattern under a microscope. In contrast, the structure of an EPLD's array prevents anyone from decoding the design visually. To prevent anyone from reading out an EPLD's contents electrically, Altera includes a user-programmable security bit. The bit cannot be erased without erasing the entire design, so security is assured.

**Editor's Note: MMI claims MegaPAL has an equivalent gate count of 5,000, not 1200 as suggested here.*

Because of the established popularity of fuse-programmable PLDs, the first CMOS EPLDs were designed as direct replacements for existing fuse-based devices. Since then, EPLD technology has developed in directions that enhance the basic concepts used in fuse-programmable parts.

EPLD Architecture

An EPLD's programmability is based on an EPROM-like programmable AND array (**Figure 1**). The EPLD's variable AND array and fixed OR structure implement logic functions in sum-of-products form, with each input to the OR function representing a product term. The result of ORing product terms (called a sum of products) goes to an I/O architecture control cell that can contain flip-flops and other elements. The I/O cell can also feed a signal back to the programmable array.

An EPROM transistor is situated at each intersection of a product term and an input or a feedback line. Initially, the EPROM transistors complete all the connections between these

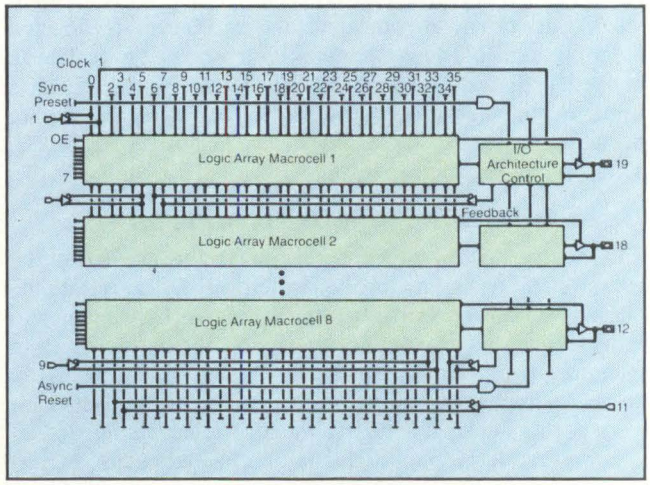

Figure 2: A number of macrocells constitute a complete EPLD, in this case the EP300. Note how the feedback and control lines connect among the device's internal elements.

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lines, causing both the True and the Complement of each input to connect to each product term. When the EPLD is programmed, some of the connections made by the EPROM transistors are opened. Thus, the program can connect any product term to the True and the Complement of any input.

When both the True and Complement connections of any input are left intact, a logical false results on the output of the product-term AND gate. If both the True and the Complement connections of any input are programmed open, then a logical "don't care" results for that input. If a user wants the output of a product term to be TRUE, all the inputs for that product term must be programmed open.

Figure 1 shows only one macrocell out of this device's total of eight. A more global view appears in **Figure 2**. With multiple macrocells, feedback from one output cell can act as an input to another macrocell, thus providing a way for the EPLD to implement complex logic functions.

EPLD Architectures Can Adapt

A key to EPLD versatility lies in the programmability of its I/O structure. Using the I/O cell of the EP300 as an example (**Figure 3**), output and feedback multiplexers can provide as many as 20 different operating conditions. The output multiplexer selects inverted or noninverted, registered or combinatorial outputs. The feedback multiplexer permits combinatorial, registered or bidirectional I/O feedback. Each of the I/O options is selected by programming specific bits, which are termed architecture bits because they alter the EPLD's internal structure. Although the architecture bits do not participate in the sum-of-products logic, they are part of the device's programmable array.

Compared to PALs, which have about the same number of equivalent gates as the smallest EPLDs (about 300), EPLDs offer gates that are generally more useful. Because of the configurable I/O block, EPLDs can implement the functions of many different PALs, yet the same number of pins (20) as the PALs.

Even more architectural flexibility is necessary when a PLD's number of equivalent gates reaches about 1200, since there are four times as many gates in a package that has only twice as many pins. **Figure 4** shows how a 1200-gate EPLD is segmented into two sections to make its gates more useful. Each half of the

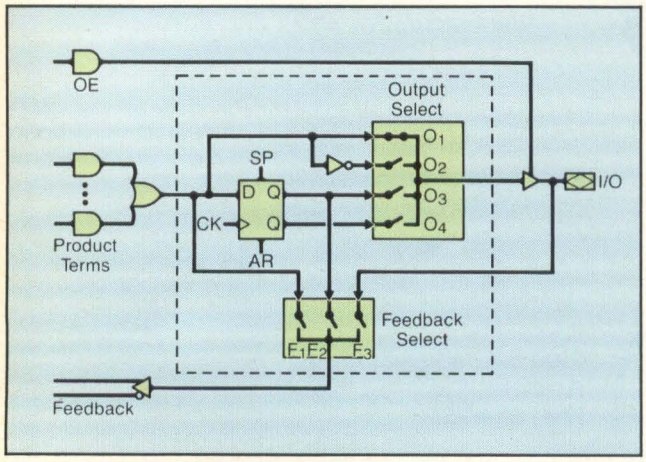

Figure 3: Programmability can control the structure of EPLDs such as the EP300. The switches shown in this I/O architecture control cell are actually implemented by EPROM transistors to let users choose among 20 different I/O conditions.

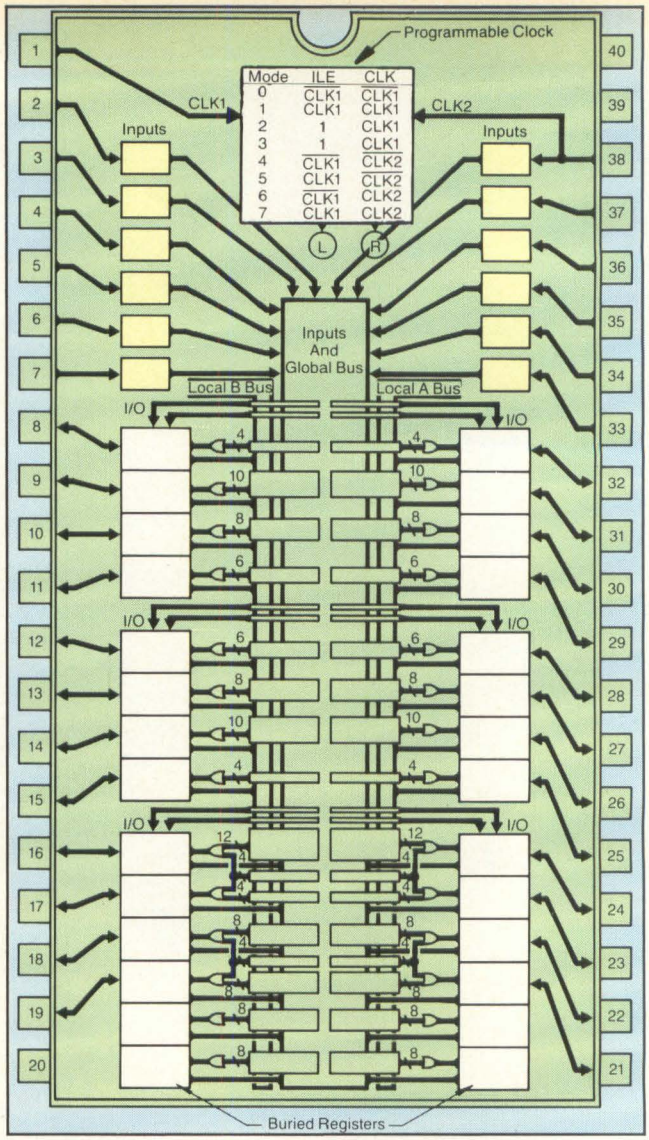

Figure 4: An EPLD that furnishes as many equivalent gates as Altera's EP1200 (about 1200) must incorporate special features to manage internal complexity. This block diagram indicates three of those features: buried registers, programmable clocks and local and global feedback buses. The table at the top center indicates the programmable clock states.

device's EPROM array has both local feedback and global feedback. The global feedback connects the EPLD's two sections and can drive any other macrocell in the device. Local feedback lines can drive only macrocells in the same section.

This division of feedback connections is virtually always transparent to users, but it allows maximum use of resources with minimum overhead for unused interconnections. If all the feedback lines in the large EPLD were global, it would be like making a printed circuit board whose wiring paths could accommodate all possible connections between all the components on the board. Even dealing with a handful of devices would require a big, complex board. But by laying out the board so that chips with common connections lie near one another and those that have few or no direct connections are placed farther apart, the board can be greatly simplified.

The 1200-gate EPLD's design follows a similar philosophy. Closely related functions can reside in the same section of the chip and employ local feedback. Connections between more loosely related functions in different sections can use global

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feedback. If this approach were not taken, the array size would grow as the square of the number of macrocells and the EPLD would occupy a much larger, more complex chip.

Some applications also benefit from an array design that allows some adjacent macrocells to share product terms. **Figure 5** shows how two macrocells can share four product terms in addition to the eight product terms dedicated to each of these macrocells. The shared terms are wired into both macrocells' OR gates. Sharing is used primarily in state machine and counter applications, where common product terms are frequently required among output functions.

Another innovation for large EPLDs is the use of buried registers. Instead of providing flip-flops only at I/O pins, an EPLD can include four buried flip-flops that may be used in feedback paths to other macrocells – an approach that conserves I/O. The device thus squeezes additional capabilities into a 40-pin DIP.

Buried registers are less practical in fuse-programmable PLDs because of the difficulty in testing a flip-flop that isn't directly associated with an I/O pin. These PLDs must connect flip-flops to I/O pins so that the elements can be easily observed and preconditioned. In an EPROM-based EPLD, however, all the flip-flops can be preconditioned in a special mode and tested fully by the manufacturer.

Additional options that can benefit 1200-gate EPLD designs are input latches and programmable clocks. The clocks consist of both input-latch and I/O-register clocks; users can select different clock enabling edges, in addition to enabling or disabling either or both of the clocks. This feature is especially beneficial in systems with multiple timing requirements.

Counting Equivalent Gates

One of the most important comparisons between different PLDs – their number of equivalent gates – is a matter of confusion. Part of the difficulty lies in the definition of what constitutes an equivalent gate. In a gate array, the accepted definition is that a gate equals a 2-input NAND gate. The resources in a PLD must be compared with the gates required to implement an equivalent set of functions in a silicon-gate CMOS gate array. Establishing this gate exchange rate is fairly straightforward for the functions in the I/O cells. For instance a D-type flip-flop can be implemented with nine 2-input NAND gates.

The evaluation gets more complex for the AND-OR array. Taking Altera's EP300 as an example, the 74 product terms (programmable AND gates) each have 18 True and 18 Complement inputs. Because an 18-input AND gate would consume at least nine 2-input NAND gates in a gate array, it could be said that the EP300's array equates to 666 (74 × 9) gates.

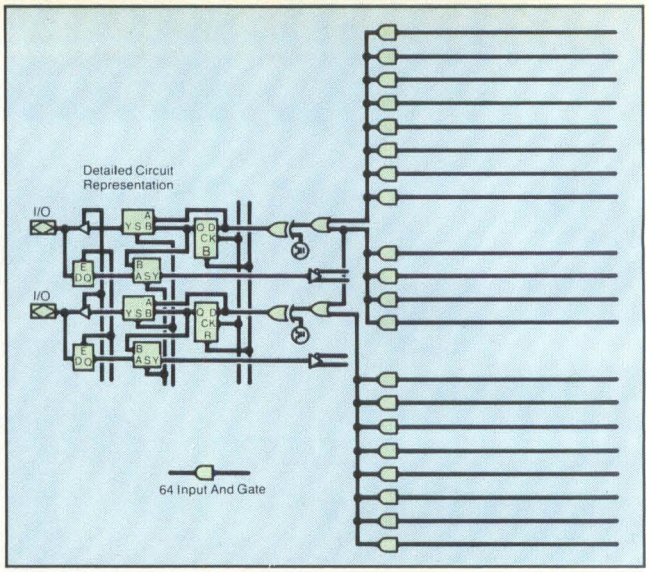

Figure 5: Shared product terms help an EPLD implement some counter and state machine applications efficiently. The two I/O cells shown here share the four middle product terms.

However, as any designer who has used a PLD knows, not all of these gates are usable in practical designs. A more realistic method is to convert PLD equations to an equivalent function as it would be implemented in a gate array, then determine how many gates are needed to implement that function. Comparing a large variety of functions indicates that each OR output in a PLD equates between 15 and 30 gates, with the lower value probably more typical. By this measure, the EP300 achieves a typical equivalent gate count of 320 gates and a maximum of 440 gates. **Table 1** compares some other available PLDs according to the same standard.

The programmable architectures used in EPLDs such as the EP300 and the EP1200 do not greatly increase the equivalent gate count as evaluated here, even though they improve the devices' usefulness. Comparing different PLDs thus demands more than a simple tabulation of gates. The real value of any programmable logic device lies in its usefulness in applications. DD

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Useful 617
Somewhat Useful 618

Resource	Manufacturer and Part Type							
	Altera EP300		AMD 22V10		MMI PAL 16R8		Signetics 82S159	
	Number	Gate Equivalents	Number	Gate Equivalents	Number	Gate Equivalents	Number	Gate Equivalents
Inputs	18	72	22	88	10	40	18	72
Flip-Flops(1)	8	72	10	90	8	72	8	72
Outputs (3-state)	8	56	10	70	8	56	12	84
OR Array Outputs	8		10		8		12	
(15 gates per OR)		120		150		120		180
(30 gates per OR)		240		300		240		360
Total Gates								
Typical		320		398		288		408
Maximum		440		548		408		588

(1) Assumes D-type flip-flop option.

Table 1: Gate complexity of various programmable logic devices.

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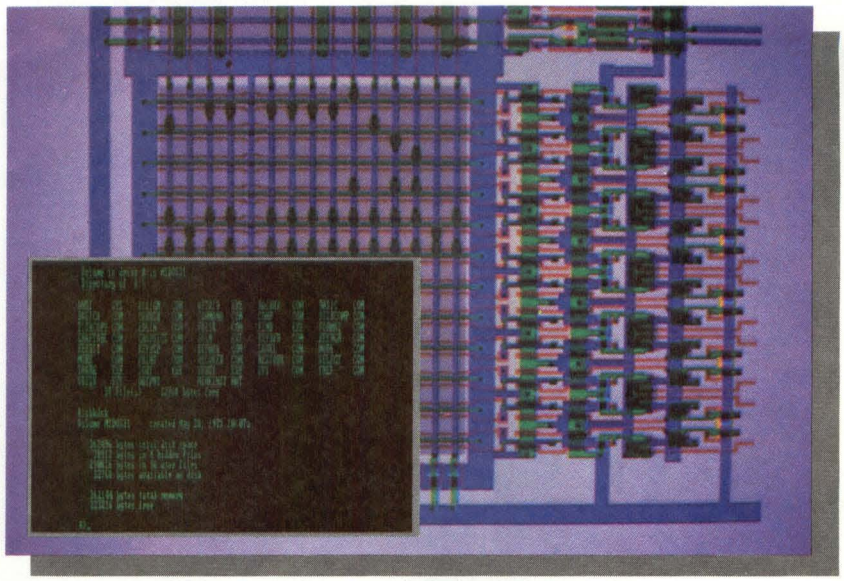

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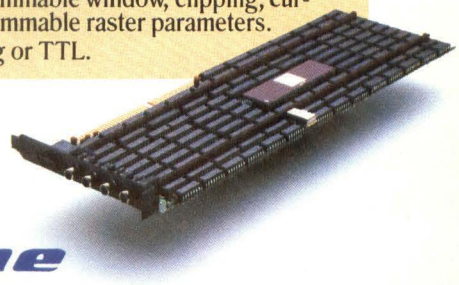
Output: RGB analog or TTL.



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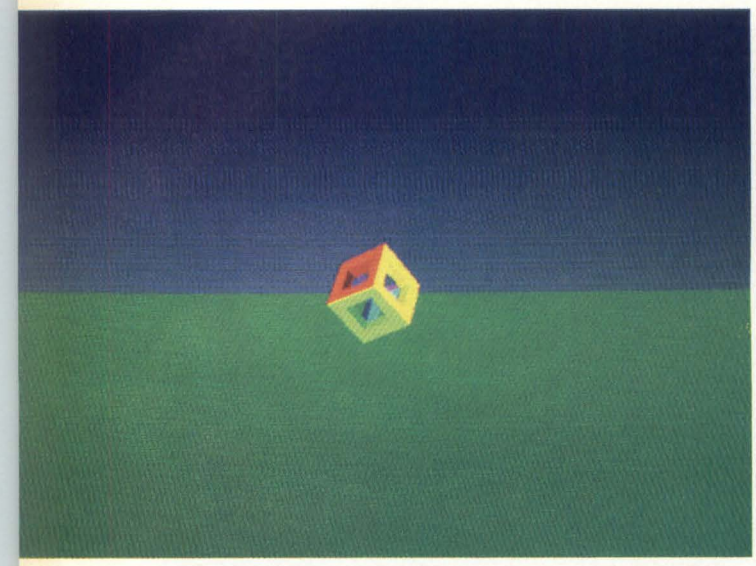


High-Resolution Graphics — Implementing Software

by Andrew C. Wilson, Sr. Technical Editor

Solid modeling of three-dimensional objects is now technically feasible because of the evolution of computer graphics technology. However, it has only been commercially viable because of the availability of more powerful host CPUs and the development of graphics systems with near real-time shaded graphics image rendering. In mechanical CAD/CAM applications, solid-modeling application software and systems are becoming increasingly popular. Likewise, other applications, such as architectural design, medical diagnostic imaging and molecular modeling are using solid modeling and shaded graphic display techniques.

Before the advent of high-speed VLSI devices, most three-dimensional algorithms were implemented in software. Since the color value and visibility of each pixel must be calculated separately, a tremendous amount of computational time was needed to render a shaded image. With high-resolution monitors, this time often stretches to hours, even days, of compute time, which is prohibitively long for many graphics applications. However, since operating algorithms are normally simple but need millions of repetitions, VLSI devices present a good solution.

Bit-Mapped Vs. Vector Displays

Images generated on graphics display systems can be divided into two classes: raster scan (or bit-mapped) and random scan (or vector). In bit-mapped graphics the image is constructed from a 2D array of pixels. Each of these can take on an individual color and brightness value to form the graphics image. To display fine detail, there must be a large number of pixels, each mapped from a screen position to a corresponding memory location in the frame buffer where each data value specifies the attributes of the pixel.

In the vector scan method, all the drawings are constructed from straight lines, lines specified from given end points. With this method, curve construction is realized by a piecewise approximation method. Solid areas are represented by lines displayed close together. When used for simple images, the technique is useful because large amounts of image memory are not required. However, as images become more complicated, the number of line sequences increases, causing screen flicker to occur.

Since the introduction of 256K and 1 Mbit DRAMs, the cost of implementing a high-resolution bit-mapped display has reduced so dramatically that the bit-mapped method now dominates most graphics applications. This has led to two factors affecting graphics board design: the realization that powerful graphics systems can now be implemented on small printed circuit boards (many are available on the IBM PC bus) and the realization that these graphics boards can now be used with other peripherals, such as imaging devices that can store images as well as graphics using the graphics bit-map.

Monochrome Graphics

In many applications, such as publishing workstations, the use of color is not required. Rather, the system must support a large bit-map and be able to move characters and text very quickly. Typical resolutions, often greater than 1024 × 1024 × 1, allow characters and icons to be stored in "nonvisible memory" and brought on-screen very quickly. And because of the limited nature of the application, graphics commands can be microprogrammed into the graphics controller, or specialized VLSI devices can be used. Bit block transfer (BIT-BLT), for example, is a function which transfers a 16-bit region of a graphic bit-

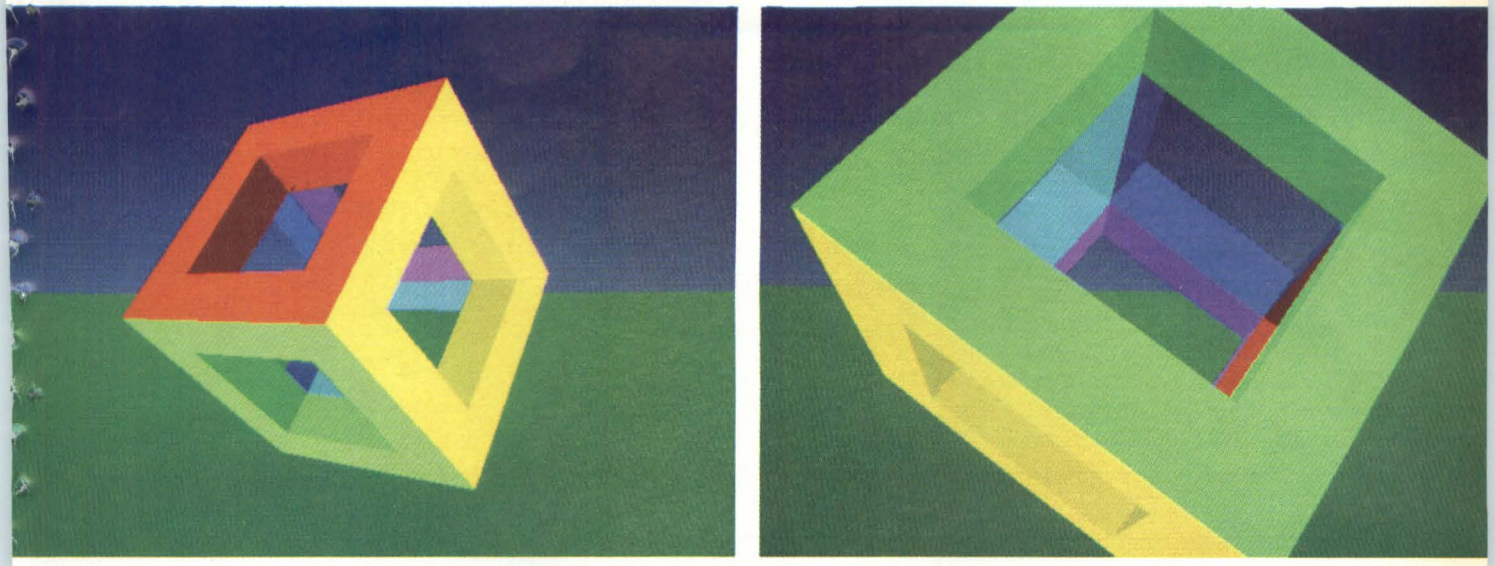


Figure 1: Pictured are four single-frame shots of a real-time display running at 60 frames per second, noninterlaced, on the XTAR (Elk Grove, IL) Polygone IBM PC-compatible graphics board.

In Silicon

map from one location to another. Originally developed by the Xerox Palo Alto Research Center (PARC), the technique allows rapid transfer of graphics or text.

In the development of its VG-150 graphics controller board, Datacube (Peabody, MA) used the technique implemented as microcode stored in on-board PROMs (*Electronic Imaging*, June 1984, p. 76). Using Advanced Micro Devices' (Sunnyvale, CA) 29116 on-board processor, the 150 Multibus board is optimized for the BIT-BLT operation. Other manufacturers have committed this function to silicon to improve speed and PC boards (*Digital Design*, June 1985, p. 24). At Sun Microsystems (Mountain View, CA), a BIT-BLT chip was developed for its workstation by Silicon Compilers (Los Gatos, CA) and is now being marketed through VLSI Technologies (San Jose, CA). Pacific Mountain Research (Seattle, WA) also has this kind of chip, designated the PMR 96016, which also was developed using silicon compliation at Seattle Silicon (Seattle, WA).

Another commonly used function in monochrome graphics systems is image companding, or the compression and expansion of bit-mapped images for purposes of fast image transmission. Using techniques such as modified Huffman run-length encoding, companding has, up until now, been implemented in microcode in a similar fashion to the BIT-BLT operation. At AMD, an IC has been developed which performs these functions and which will find its way onto the next generation of graphics boards. Designated the Am7970, the CCITT Group 3 and 4 compatible chip capitalizes on the high pixel-to-pixel correlation in monochrome images, recoding the data to eliminate redundancy. For example, an 8½" × 11" document scanned at 200 dots/in across and 200 dots/in down consumes 467.5 Kbytes. Compression, using the 7970, can reduce this to typically 10-100 Kbytes, saving both memory and transmission time.

Future implementations of graphics boards will employ co-processors to offload commonly used functions from the graphics controller. Future silicon developments will include such chips as window management ICs to automatically control a number of independent graphics windows at high-speed. This and other advances will lead to true multiprocessing graphics controllers operating at high speed. Advances in ASICs technology will encourage the development of these graphic controllers.

Color Graphics Systems

As the human visual system can only discern approximately 256 levels of gray, systems which use 8 bits of image depth are useful in depicting realistic images. For color systems with three primary colors, 24 bits are required. The more bits per pixel, the more subtle the effect created can be, especially in applications which demand functions such as natural scene shading. Most graphics systems currently available are not designed to produce a full range of colors and shades.

To offer a large range of colors without using large amounts of memory, output look-up tables (LUTs) can be used. The data value of a pixel is not used directly to control the color or intensity, but acts as an entry address within the LUT. The value obtained is used to determine the pixel color and intensity. For an 8-bit-per-pixel system, two bits per primary color and two bits for intensity could be used. This would produce 12 bits of color data with a possible 4096 definable colors. However, the trade-off is that only 256 of these colors can be chosen at any one time.

Although many color graphics boards use VLSI devices as display controllers, they are not capable of such graphic calculations as light source modeling. For example, ICs such as the NEC 7220 and the Hitachi ACRTC perform commands such as "draw circle," "draw rectangle" and "draw line" without host intervention. These ICs – and boards based on them – are not cable of such functions as image rotation or interpolation of

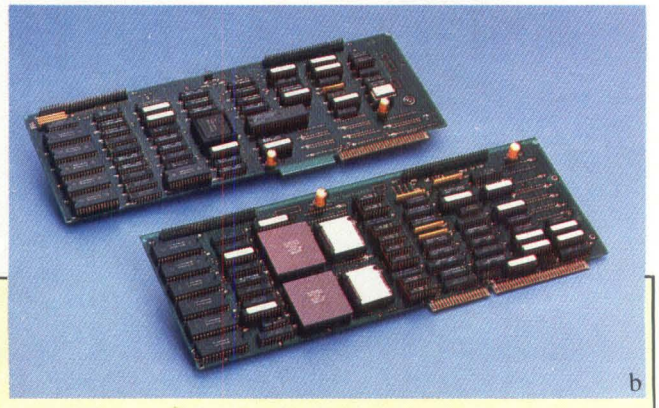
polygon vertex intensities (for Gouraud shading).

Because of this fact, potential designers, integrators and users of these systems must be aware of their limits which are often clouded. In some advertisements, manufacturers will show images—often computed on a Cray or a VAX—next to a photograph of a graphics board which is incapable of producing the images.

Color Graphics Boards

Many of the available graphics boards use VLSI devices as display controllers. These VLSI devices include the 7220 from NEC (Mountain View, CA), the 7300 from NCR (Colorado Springs, CO), the RMS chip set from Motorola (Phoenix, AZ) and the 95C60 from AMD (**Figure 3**). The graphics boards available include the IV-1651 VME graphics board from Ironics (Ithaca, NY) which uses the 7220, the Revolution 1280 × 4 IBM PC board from Number Nine Computer (Cambridge, MA), which uses the Hitachi ACRTC, and the Short-Port Color Card for the IBM PC from Emulex (Costa Mesa, CA), which uses the Hitachi 6845.

Other manufacturers have developed their own graphics chips to incorporate onto board-level products to improve performance. Last month, Xtar (Elk Grove, IL) announced a PC graphics card based on its own GMP chip set. **Figure 1** shows a cube rotating about three axes and zooming toward the viewer.



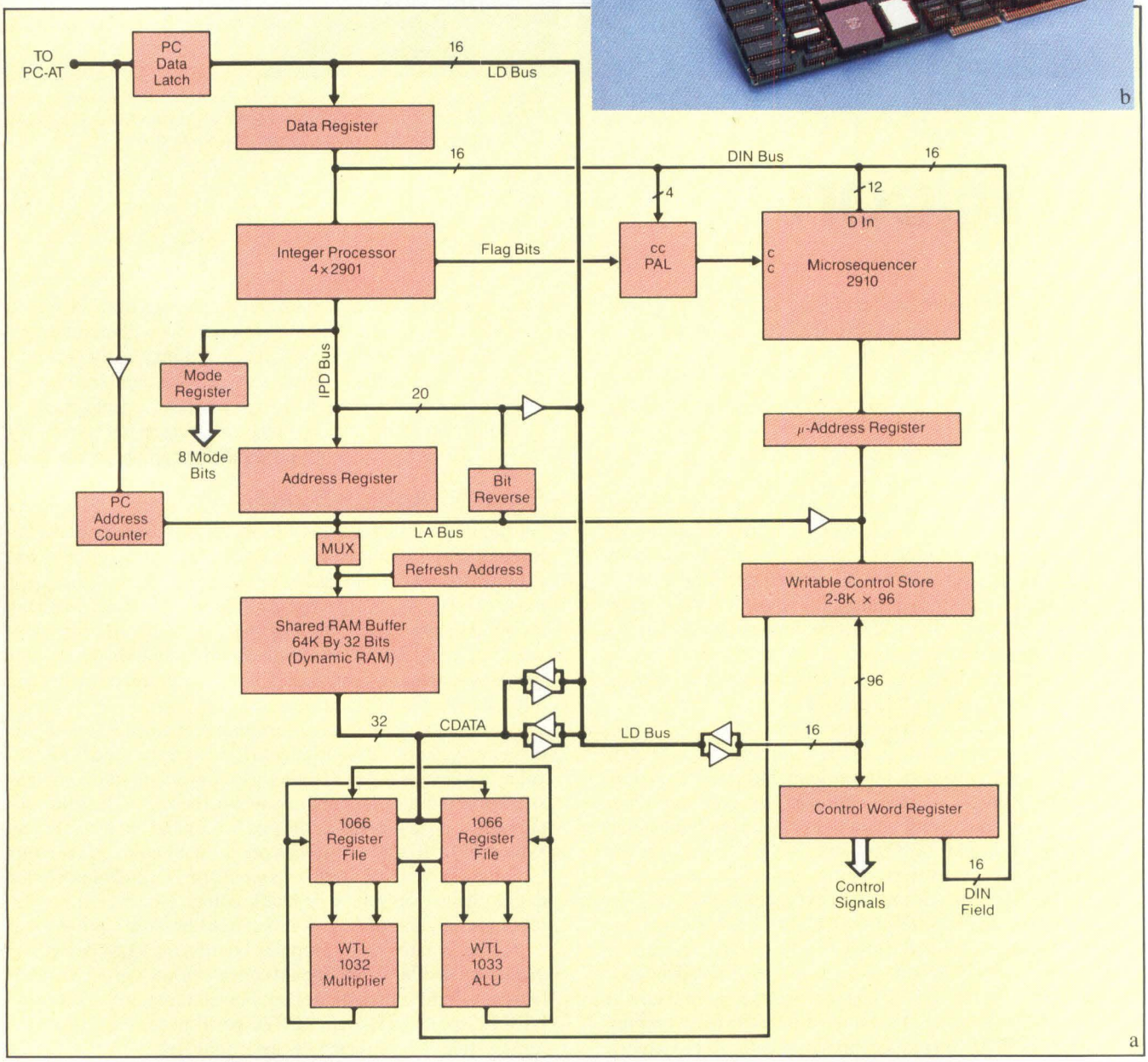


Figure 2: (a) Block diagram of Weitek's solids modeling engine which was first shown at SIGGRAPH last month. (b) The two-board set, implemented on the IBM PC/AT, is capable of complex graphics functions.

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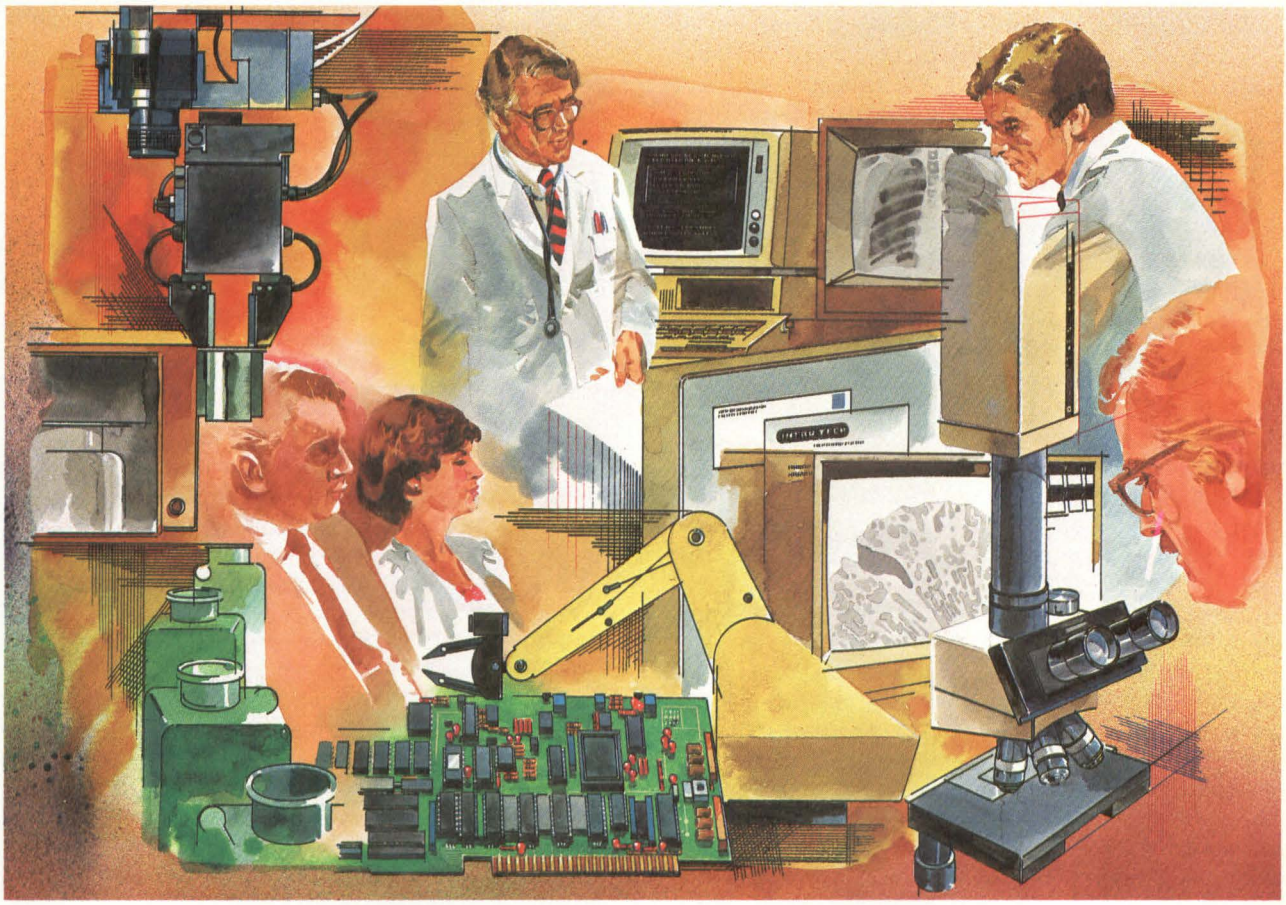

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The cube is redrawn every 16.7 msec into a 640 × 400 × 4 bit-frame buffer. For each frame, the host processor (in this case, the IBM PC) calculates the data for the Polygone board's display list. Standard matrix multiplication routines are used to rotate the cube about its center and to translate it along the Z axis. A binary space partition (BSP) algorithm sorts the polygons in the Z direction. Conventional projection routines then calculate the screen coordinates of each vertex of each polygon. The resulting two-dimensional polygonal database is then sent to the Polygone board, which draws the scene into the frame buffer.

The background shading from light to dark green and light to dark blue is accomplished using the dithering capability of the Polygone board. Dithering is also used for some of the intermediate shades of the cube faces. Eighteen different colors are used in the cube, with several more shades being used to create the background. The Polygone board's dithering capability makes it possible to draw this picture on a 4-bit-per-pixel system, which would normally be limited to 16 colors.

In a similar move, Matrox (Dorval, Quebec, Canada) announced its PG-640 and 1280 IBM graphics boards which use custom VLSI drawing processors to execute graphic commands rapidly.

Whichever chip set is chosen, most currently available graphics boards implement the same kind of functions. Graphics primitives can be used for 3D drawing functions, matrix transformations and look-up table programming. However, many of these boards have a limited ability to render objects.

To perform rendering it is necessary to use techniques such as antialiasing, hidden surface removal, Phong or Gouraud shading and ray tracing. These functions are useful in applications such as CAD/CAM, video animation and medical applications. Many graphics companies see these types of functions as not only belonging to the purely graphics area but also to the graphics/imaging or solid modeling area. Because of this, many of the more complex graphics functions may appear either in microcode or in dedicated ICs.

At last month's SIGGRAPH show in San Francisco, Weitek (Sunnyvale, CA) introduced a high-performance graphics board for the IBM AT called the solids modeling engine. At the heart of the two-board set is a floating point ALU consisting of the company's 1032 multiplier, 1033 adder and two 1066 register

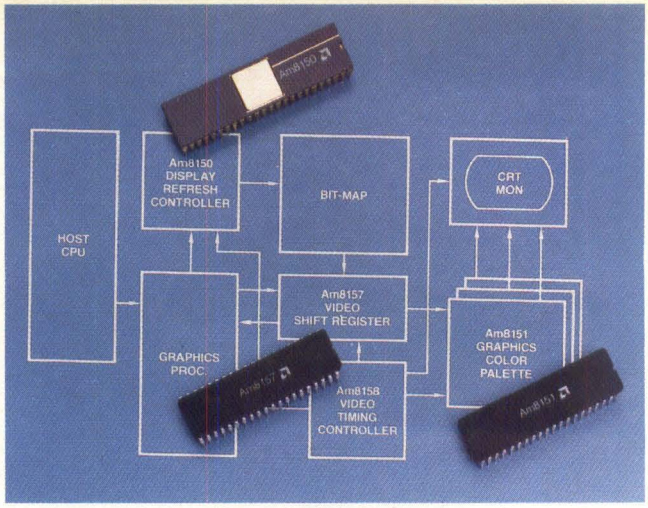

Figure 3: AMD's programmable three-chip graphics chip set is typical of the VLSI devices now available for graphics. Shown are the Am8150 display refresh controller, the Am8151 graphics color palette and the Am8157 video shift register.

files (**Figure 2**). A 2901 microsequencer controls the solids modeling engine and is pipelined for high-performance. Microcode embedded in the writable control store (a bank of 2K × 96 bits of static RAM) controls virtually everything on the board set and is loaded by the AT during initialization.

Weitek's integer processor is a 16-bit machine made up of four 290ls that calculates addresses for the shared RAM buffer. It also can be used for command parsing and logical operations. Because it uses the IBM graphics controller, the solids modeling engine is interesting for two reasons. By choosing a microcoded design, the two-board set is not limited to a set of graphics primitives, thus the boards are capable of all the standard graphics primitives such as transformations and clippings. Also, the machine can be used for solid modeling, performing such functions as hidden surface removal, variable shading, translucency and light source modeling.

Combining Imaging And Graphics

Although more graphics functions will be implemented in VLSI, many graphics manufacturers are studying ways of combining graphics and image processing. Bit-map memory systems have allowed systems to be configured which use bit-mapped graphics memory to store images as well as graphics, opening application areas in medical, industrial and military

Z-Buffer Eases Complex Calculations

Originally proposed by Edwin Catmull, the concept of the z-buffer extends the concept of an x-y image space into depth or z-coordinates. By doing this, graphics calculations, such as hidden-line removal, become less complex. This is because the elements of an image do not need to be written into the frame or z-buffer in depth priority. For example, if a new element in a scene is to be displayed, then the depth or z-value of the new image can be compared to that already in the z-buffer. If the pixel's z-value will be less than the z-value already in the frame buffer, then the new pixel is behind the image already in the frame buffer and no action is taken. If the new pixel's value is greater than the frame buffer value, then the frame buffer will be updated with the new value.

The concept of the z-buffer eliminates calculations of an image depth sort while increasing image-memory size to accomodate the buffer. Also, since the pixels in the frame buffer are written to in an arbitrary order, it is more difficult to perform such tasks as prefiltering antialiasing, transparency and translucency effects. Techniques to overcome the limitations of these factors include postfiltering using a resolution larger than display space resolution for antialiasing and using separate transparency, intensity and translucency buffers to overcome the transparency and translucency problems of the z-buffer.

The z-buffer concept may also be extended to include other forms of graphical effects, such as shadow effects. Despite the large amounts of memory needed to implement these concepts, recent semiconductor advances have allowed many of these techniques to become commonplace.

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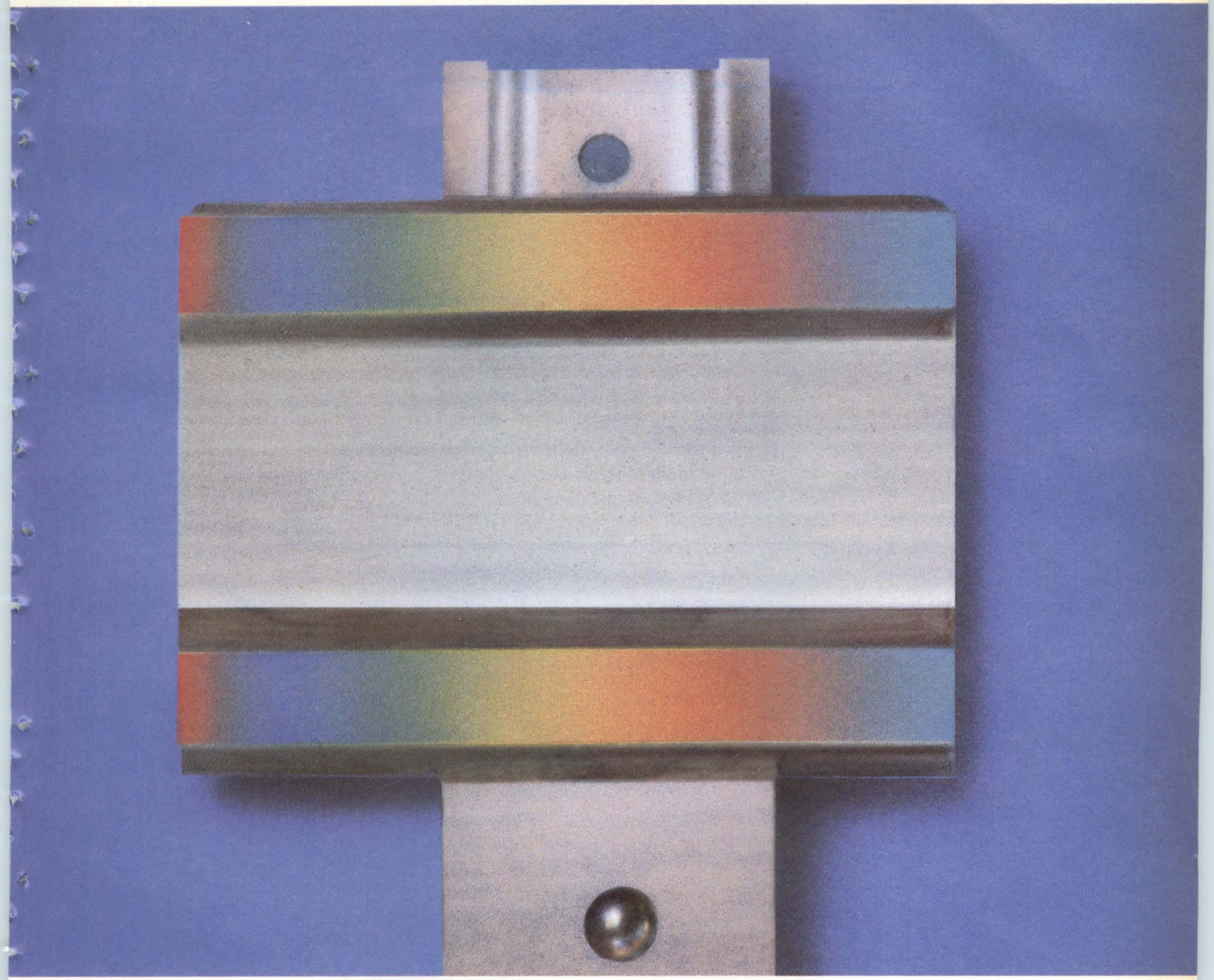

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applications (*Electronic Imaging*, April 1985, p. 42). At US Video (Washington, DC), a single IBM PC-compatible board has been developed which allows users to combine both imaging and graphics. Designated the Raster Master RM-110, the board is capable of superimposing graphics and information over images generated by any NTSC-compatible source. At the low end, these systems will be useful for video production and special effects systems. At the high end, these systems will prove useful in other areas.

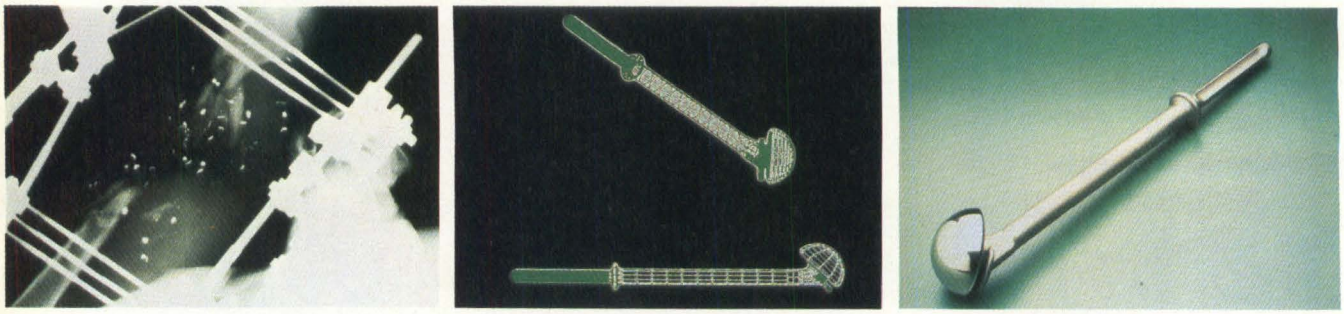

Figure 4: Graphics and image processing combine on systems such as this from MPDI. This figure shows (a) an X-ray of a patient with a shattered arm bone, (b) the CAD/CAM display of the upper arm bone generated on a Unigraphics II system after image pre-processing and vectorization and (c) a custom humerus shaft manufactured by CAD/CAM instructions.

At this year's NCGA in Dallas, TX, a system was discussed which combined both image and graphics processing to produce detailed prostheses for medical purposes (Reference 4). The system, discussed by Dr. Michael Rhodes of Multi Planar Diagnostic Imaging (Torrence, CA), uses Data General (Westboro, MA) minicomputers to perform region growing and thinning algorithms on CT data. This data is then vectorized and sent to a CAD/CAM system where it is used to construct a graphical prosthetic image. After this, the data is reformatted and sent to a milling machine where the prosthetic implant is manufactured (**Figure 4**). Although much of this computation is currently being performed on minicomputers, advances in graphics technology will soon allow these functions to be performed on personal computers.

VLSI Enters The Picture

Much of the current research in graphics systems is aimed at improving the image generation speed by dividing the display into small regions, each handled by separate concurrent processors (Reference 5). Until the introduction of the Graphics Engine by Dr. James Clark of Silicon Graphics (Mountain View, CA), not much progress had been made in combining graphics and VLSI technologies. At the 1985 VLSI Chapel Hill conference at least three papers were presented on VLSI graphics systems. One, from John Poulton of the University of North Carolina (Chapel Hill, NC), described a pixel planes graphics engine designed to replace the rasterizer, frame buffer and video controller of a conventional system. The main component of the system is a smart frame buffer composed of custom VLSI memory chips which addresses the graphics problem with a highly parallel processor that mimics a processor per pixel. Using the pixel planes system approximately 30,000 four-sided polygons can be processed per second.

At Stanford University (Palo Alto, CA), Scan Line Access Memory (SLAM) has been developed to rasterize images in a highly parallel manner. Stefan Demetrescu of Stanford described an image memory built with SLAM devices which is capable of filling an arbitrary horizontal pixel line segment in one memory access. When rasterizing polygons of 100 × 100 pixels, the SLAMs increase the bandwidth to the frame buffer by factors of 100 to 1600 times, allowing very fast rasterization speeds. Similar research was described by Nader Gharachoroloo and Christopher Pottle from Cornell University (Ithaca, NY). The Super Buffer they described consists of two main parts: a Scan-line Processing Unit which buffers and transforms high-level polygons into intermediate scan line instructions and a VLSI Raster Graphics Engine which simultaneously updates, buffers and refreshes one line of the raster image. Updating the image is performed by transforming each input scan line command into several low-level pixel painting instructions. The image buffer is, therefore, only one scan line and contains only 512 locations. Output of the engine is a raster scan of pixel intensities synchronized with the raster beam for direct screen refreshing.

Although many graphics methodologies such as temporal antialiasing have not yet been fully exploited, today's graphics systems implement many functions needed by systems integrators. Future systems, using either microcoded processors or off-the-shelf VLSI graphics processors, will allow graphic systems to be implemented at low cost. As this occurs, imaging processing functions and graphics functions will merge into systems capable of performing a range of tasks at high speed. DD

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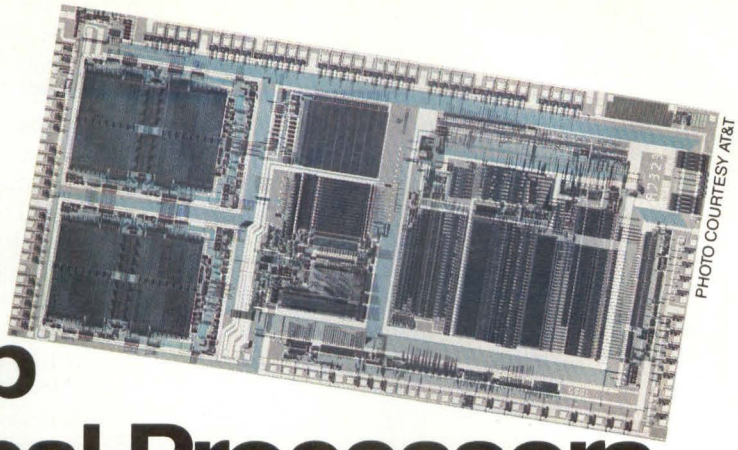

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Single-Chip Digital Signal Processors Challenge Multichip Solutions

by David Wilson, Executive Editor

Rapid improvements in fabrication technology and the cost-effectiveness of digital VLSI technology and high-performance A/D and D/A converters continue to challenge the role once held by analog technology in the design of signal processors. When designing a digital signal processing system, designers can choose one of two approaches. The first is to base the design on a single-chip digital signal processor, choosing from a growing number of products. These products are usually best suited to lower speed applications, where performance constraints may not be so severe and where cost-sensitivity is important. The second approach is to use a multichip solution, designing the system with arithmetic/control blocks configured in a manner that best suits the application. Over the past few years, there has been a steady progression in the number and sophistication of features offered by digital signal processing (DSP) chips.

Since virtually all digital signal processing can be reduced to the three operations of delay, multiply and add, it is not surprising that many single-chip products look somewhat architecturally similar.

Devices have evolved and now offer many features previously found only on microprocessors; however, they also differ from general-purpose micros in a number of ways. For example, in a standard microprocessor-based system, there is a single data bus on which three distinct types of data transfers take place. First, there are instruction fetches. Second, data bytes are moved in either direction between the CPU and locations in memory. As the input and output ports are effectively located in the memory address space, I/O transfers between the CPU and the ports are the third type of data transfer.

In many DSP chips, a Harvard architecture is more common. With this architecture, the program memory space and the data memory space are separated. It is no longer necessary for the word lengths in the two areas to be the same; instructions may be longer than data or vice versa. Each memory space is connected to a bus of the appropriate width. The Harvard architecture, with its two buses, also offers a method for simultaneous instruction fetch and execution. Another requirement of DSP chips is that they implement flexible I/O structures, primarily

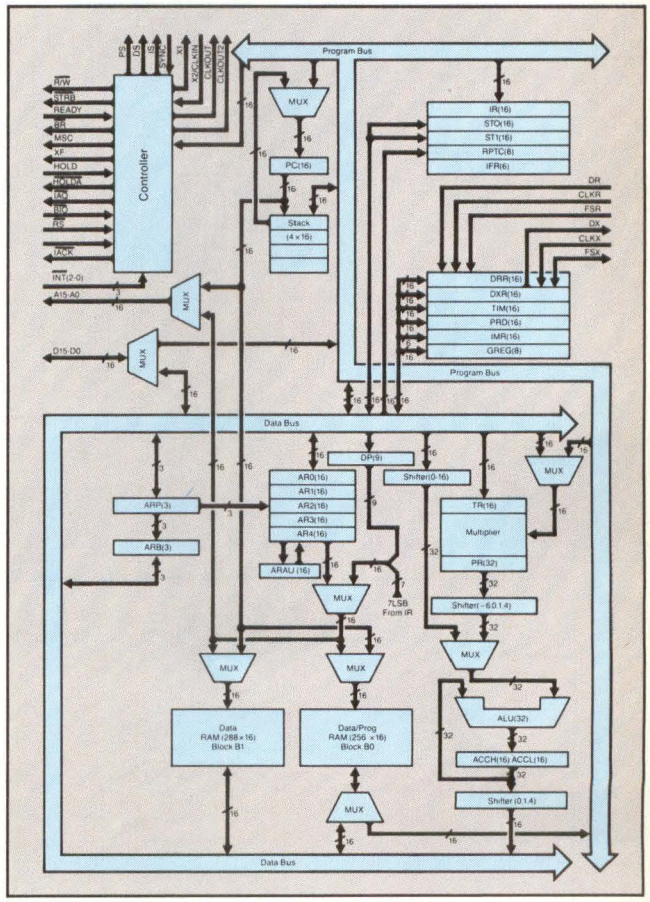

Figure 1: TI's 32020 digital signal processor has a modified Harvard architecture that provides parallelism between instruction generation and execution.

for codec interfaces. Hence, some DSP chips have serial I/O ports. In some applications, having A/D and D/A converters on the same device as fast processors and the large data and program memory may be useful. Unfortunately, this is currently pushing the state-of-the-art, and most vendors have elected to leave the converters off chip.

A fast multiplier is essential. Pipelining the multiplier is acceptable because most DSP routines are written in-line, so the pipeline rarely needs to be flushed and refilled. Routines that loop or branch still tend to confine their arithmetic computations to in-line segments.

Because of the requirements for placing so many functions on a single chip, most single-chip DSP devices are geared toward executing an algorithm for which the entire program and data can be stored on-chip. Performance benchmarks generated by the manufacturers of such devices may look impressive, but most probably have been specifically tailored toward the memory size of the parts. Although some offer the ability to access off-chip memory, often the performance will decrease because of the overhead.

Address generators, too, are fairly basic. For more sophisticated addressing, the designer must turn to the multichip solution. Most single chips are limited by their use of fixed point rather than floating point multipliers. Those chips that have floating point capability may have such a high pin count and such a high cost that they restrict their own use.

Because the DSP market is performance driven, most manufacturers have aimed toward not only greater performance in their second generation devices but also lower cost. Today's single-chip devices are not measured solely in operations per second but according to their capability to perform a 16-bit fixed point, a 24-bit fixed point or a 32-bit floating point operation.

Advantages of the single-chip approach over the bit-slice approach include easier software development, easier board design and lower board costs when the chip price drops. However, where processing speed is of primary importance, it will be a long time before bit-slice techniques are redundant.

One of the first DSP devices was the TMS32010 from Texas Instruments (Houston, TX). Although the device is very popular, it had early limitations including a limited address space and a slow execution speed (the device took two cycles to multiply/accumulate).

TI's second generation device, the TMS32020 has a number of improvements. The processor has a modified Harvard archi-

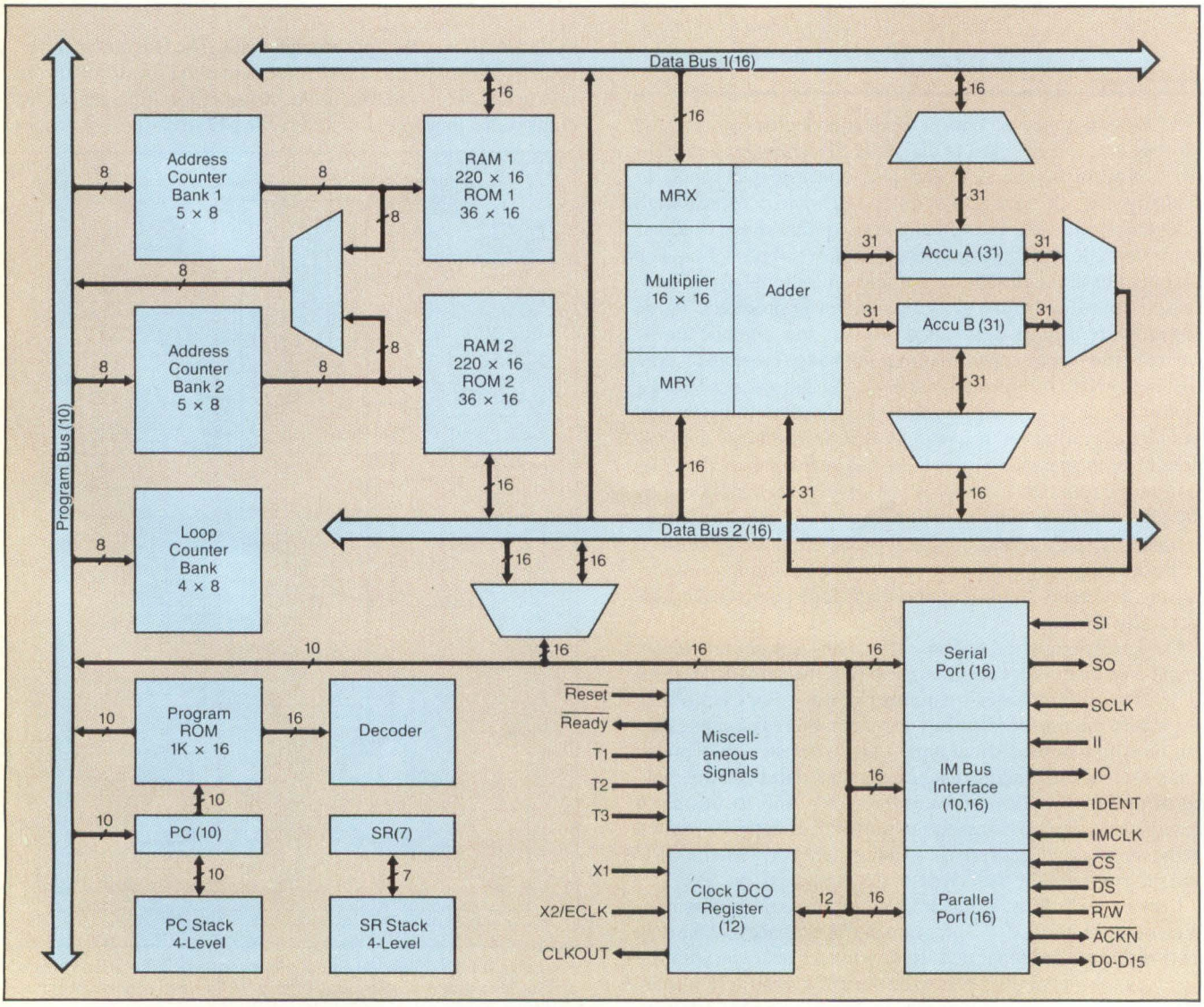

Figure 2: ITT Intermetall's digital signal processor has a data bus divided into two equal parts.

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tecture that provides parallelism between instruction generation and data computation. The heart of the architecture is its dynamically reconfigurable twin-RAM organization in which a total of 544 × 16 bits of RAM have been split into two different blocks (**Figure 1**). The first RAM block (288 × 16 bits) has been permanently mapped into the data memory space. The second RAM block (256 × 16 bits), under program control, can be mapped into either the data or the program memory space. All 544 words of on-chip RAM can be used as data memory and instructions may be supplied from off-chip devices at full speed. In another system configuration, 288 words of on-chip RAM can be used as data memory while 25 words remain as program-cache memory. Therefore, instructions can be downloaded from slower off-chip devices to the on-chip RAM and then executed at full speed.

The twin-RAM architecture also allows for the execution of a multiply/accumulate instruction in a single cycle. The 32020 also has several provisions for supporting a multiprocessing interface in which part of the external data memory can be shared by several processors, which can be synchronized together at the clock level. Also, a serial port, not available on the 32010, simplifies communications with A/D converters, codecs and other serial peripherals.

Like the TI part, the DSP128 from STC Semiconductors (Sidcup, Kent, UK) is also based on a Harvard architecture. Also known as the Cascadable Real-Time Signal Processor or CRISP, the DS0128 has a system bus, exclusively for I/O operations and an on-chip DMA controller added to it. The functional elements of the chip include two identical blocks of 256 16-bit words of RAM with their own data address units, an ALU with a 35-bit accumulator, a 16 × 16 multiplier and a DMA controller.

Unlike the TI part, the DSP128 program memory is off-chip, and a block load instruction is used to transfer words from program memory space to the internal RAM blocks. This is typically used at the start of an algorithm to load the multiplication coefficients into the required RAM locations. Many tasks can be partitioned between several devices to improve system throughput.

As a direct continuation of the Harvard architecture idea, ITT Intermetall's (Freiburg, West Germany) DSP chip, the UDPI 01, has a data bus divided into two equal parts. Although the main feature of a digital signal processor that distinguishes it from a standard microprocessor is the hardware multiplier, there are other features which are often underrated. These features include how quickly data can be made available to the multiplier or how quickly its results can be retrieved for further processing. In the ITT device, two values may be fed to the multiplier in each cycle via the data buses therefore enhancing the throughput of the device. **Figure 2** shows the internal architecture. The arithmetic unit consists of a 16 × 16-bit multiplier and a 31-bit adder. In the UDPI 01, the address space is 1K words × 16 bits, and the program memory is designed as an on-board ROM that may be mask programmable by the user. ITT will offer another version of the processor called the UDPI EC that will address external storage instead of ROM.

The data memory has a total capacity of 512 16-bit words. It is subdivided into two sections, each having 220 words of static RAM and 36 words of ROM. Each of the sections is connected to one of the two data buses. In addition, one parallel and two serial interfaces are available. The parallel interface uses a handshaking process that is compatible with the 68000 for data transfer. The serial interfaces simplify the programming of the

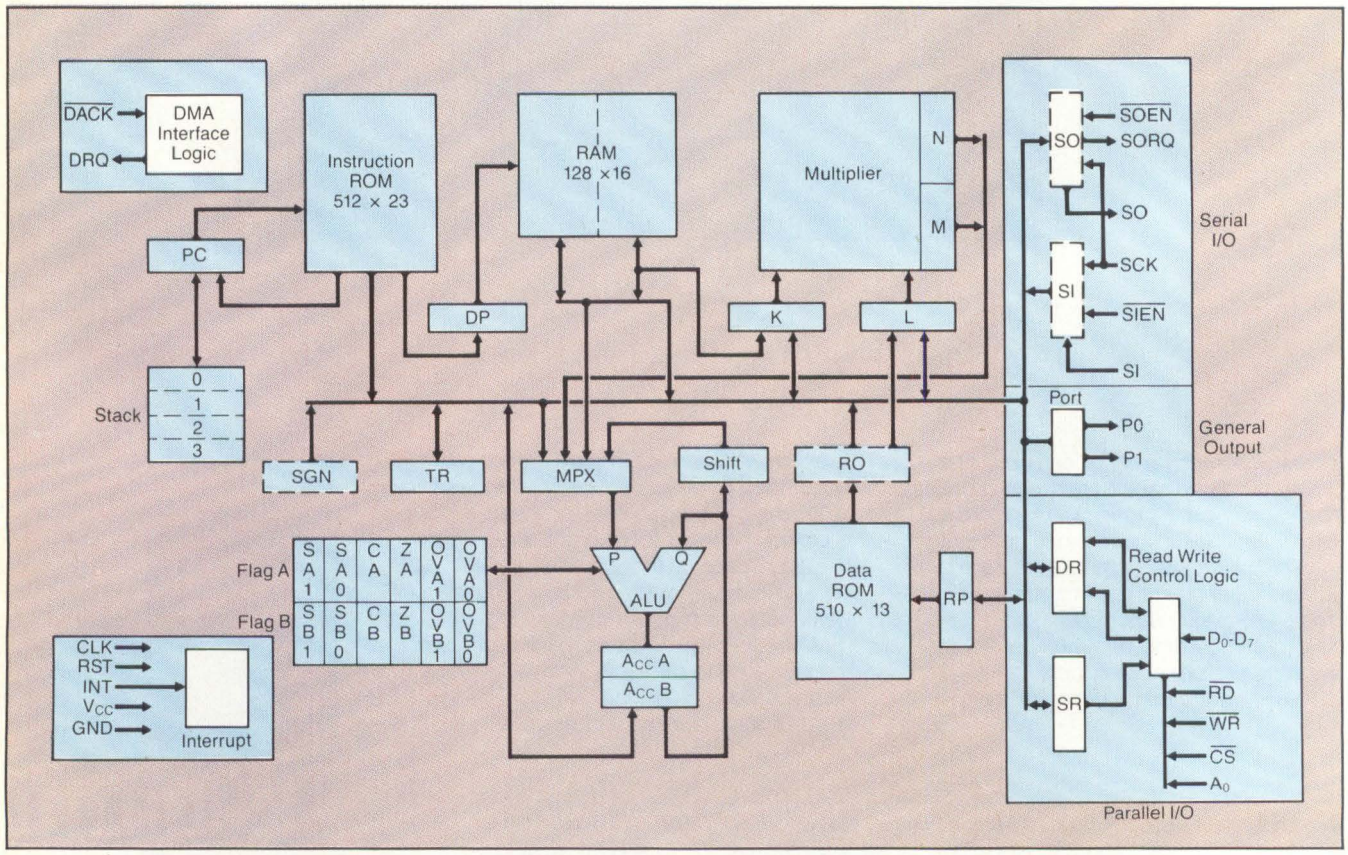


Figure 3: The 7720 from NEC (second-sourced by Gould/AMI), allows a sum of product operations in a 250 nsec instruction.

cyclic procedures that are a feature of digital filtering. Using this procedure, serial data can be transferred at a transmission rate of 5 Mbit/sec. Like TI's TMS32010, which is second sourced by General Instrument, NEC's (Mountain View, CA) 7720 is sourced by Gould AMI Semiconductors (Santa Clara, CA) as its S7720. Although the AMI chip does not differ in functionality from the NEC part, it does differ in power consumption and temperature performance. Whereas the NEC part dissipates 1.2W, AMI's dissipates 950 mW; NEC's part operates over a −10°C to +70°C operating range, AMI's operates between −40°C to 85°C.

Nevertheless, the chips are remarkably similar. Computational logic is provided by a 16-bit ALU and a separate 16 × 16 fully parallel multiplier that allows a "sum of products" operation in a single 250 nsec instruction cycle. Two serial I/O ports are provided for interfacing to codecs and other serially oriented devices whereas a parallel port provides both data and status to conventional microprocessors (**Figure 3**).

Memory is divided into three categories: program ROM, organized as 510 × 23-bit words; data ROM, organized as 510 × 13-bit words; and data RAM, organized as 128 × 16-bit words.

While Gould/AMI research is focusing on the cost-sensitive end of the DSP market, NEC appears to be investigating higher performance products. Although most of the DSPs discussed so far have only fixed-point capability, the next generation devices may include some floating point capability achieved at a much greater device density.

The latest device described by NEC includes over 110,000 transistors in a 132-pin pin grid array. The chip's architecture (**Figure 4**) includes three separate buses. Data on the X bus and the Y bus are fed into a two-operand floating point adder and floating point multiplier. Data on the Z bus is used for storing output data coming from the arithmetic multiplier and adder and the instruction ROM and RAM. The floating point chip is designed specifically for signal processing by use in a multichip configuration.

To integrate the floating point architecture on the Hitachi (San Jose, CA) DSP device, the HD61810, while retaining a part in a small (40-pin) dual in-line ceramic package, a new technique was adopted. The HD61810 is for speech and telecommunications applications. The accuracy of the floating point arithmetic

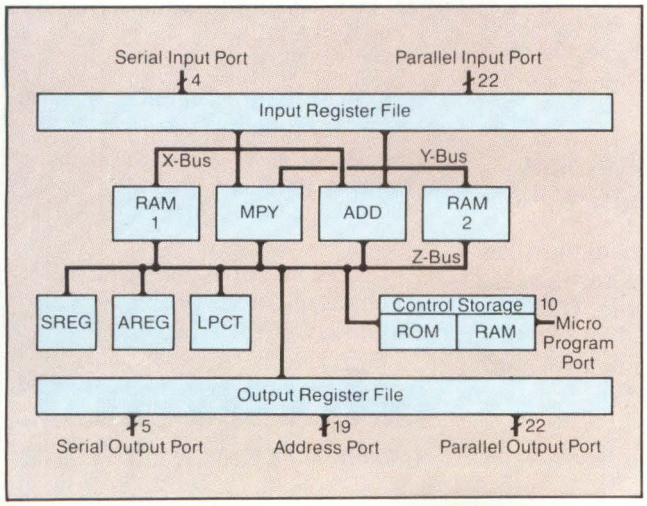


Figure 4: NEC's next generation device includes three separate buses.

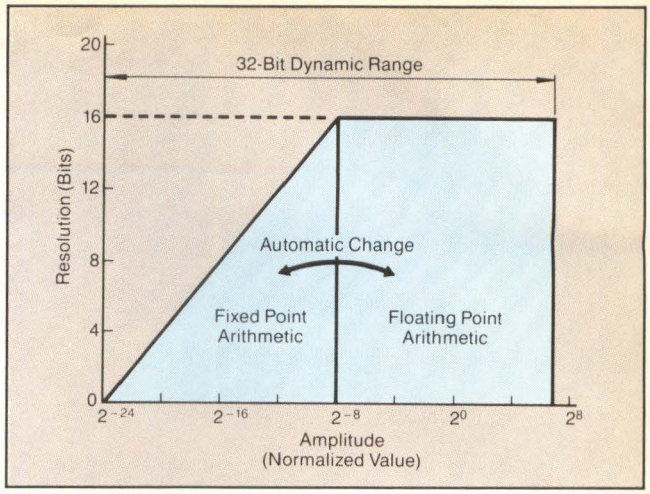


Figure 5: Hitachi's digital signal processor, the HD61810, achieves a 32-bit wide dynamic range and maximum 16-bit resolution using floating point arithmetic.

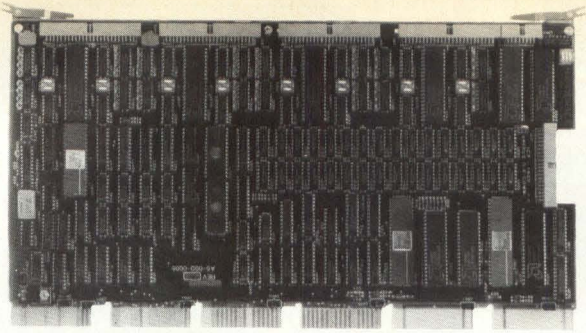
can be represented by a 32-bit dynamic range and a 16-bit maximum resolution as shown by the shaded area in **Figure 5**.

The left part of the shaded area can be determined by fixed point arithmetic, the right part by floating point arithmetic. If fixed point arithmetic is used, only the left part will be realized. The Hitachi part automatically switches between the two different types of arithmetic, floating point and fixed point, by distinguishing the amplitude of the data. The Hitachi signal processor features an internal multiple bus structure, horizontal-type micro instructions and a two-port RAM. Another part, the HSP-RM, has a large capacity RAM instead of the data and instruction ROM of the HSP.

Perhaps the largest DSP chip manufactured is the DSP32 from AT&T. The chip, containing 155,000 transistors was described at the 1985 ISSCC in New York. The on-chip data arithmetic unit, configured for multiply/accumulate, is the primary execution unit for signal processing algorithms. A full 32-bit floating point multiplier and adder have been implemented that, according to AT&T, are capable of eight million floating point operations per second.

The DSP32's on-chip memory includes 2 Kbytes of ROM and 4 Kbytes of RAM with auto-refresh. The memory can also be expanded to include 5 Kbytes of directly accessible off-chip ROM or RAM. The DSP includes two additional I/O ports, a serial I/O port that provides an interface to time division multiplexing and a parallel I/O port that may be used for direct microprocessor interfacing. Both ports include a user selectable DMA mechanism for directly transferring data or programs between I/O and DSP memory without interrupting a program in process. The DSP is packaged in a 40-pin DIP as well as a 100-pin array. The 100-pin package is required for external memory expansion.

AT&T recently announced commercial availability of its 32-bit chip set (*Digital Design*, July 1985, p. 21) and had working samples of the DSP at the ISSCC. The part may become available as soon as 1986. Other vendors also have single-chip DSP devices in the works. Two of these vendors are Motorola (Austin, TX) and Analog Devices (Norwood, MA). Analog Devices currently offers a range of DSP products that include its Wordslice family. TRW LSI Products (La Jolla, CA), an industry leader in DSP and a vendor of a range of standard parts, currently offers designers a standard cell library from which to design their own parts. This functional building block approach



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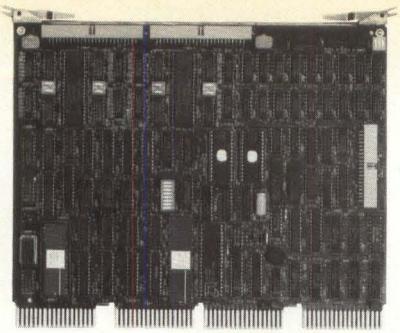

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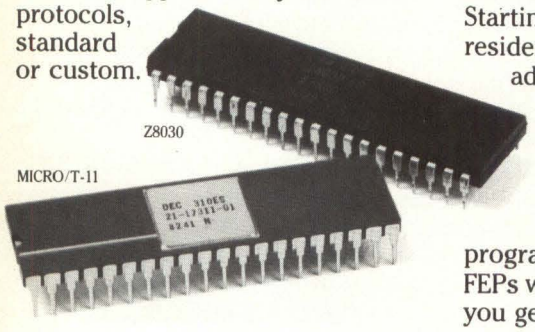

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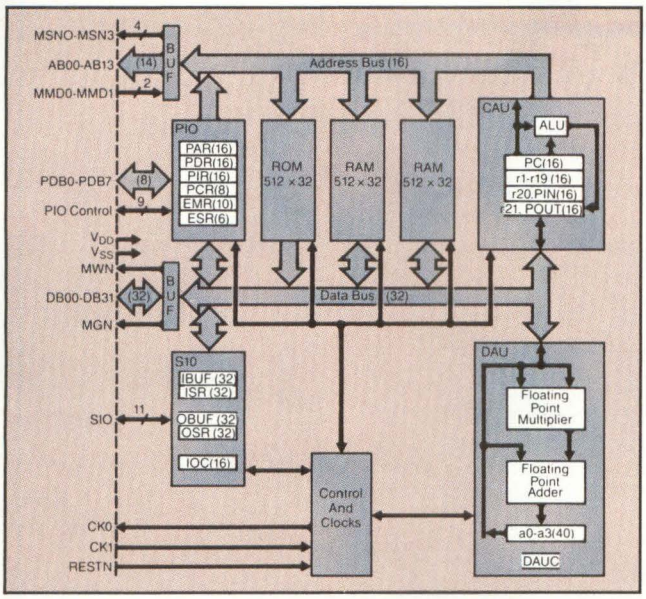

Figure 6: According to AT&T, its digital signal processor with 32-bit floating point arithmetic has a performance of 8 MFLOPs.

enables users to tailor the chip to their particular requirements, choosing from a variety of parts in the cell library.

CMOS will become the preferred technology for most next generation devices. Currently, both ITT and Fujitsu (Santa Clara, CA), with its MB8764 DSP, offer parts in CMOS, but other vendors are not far behind. DD

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by Joe Aseo, West Coast Technical Editor

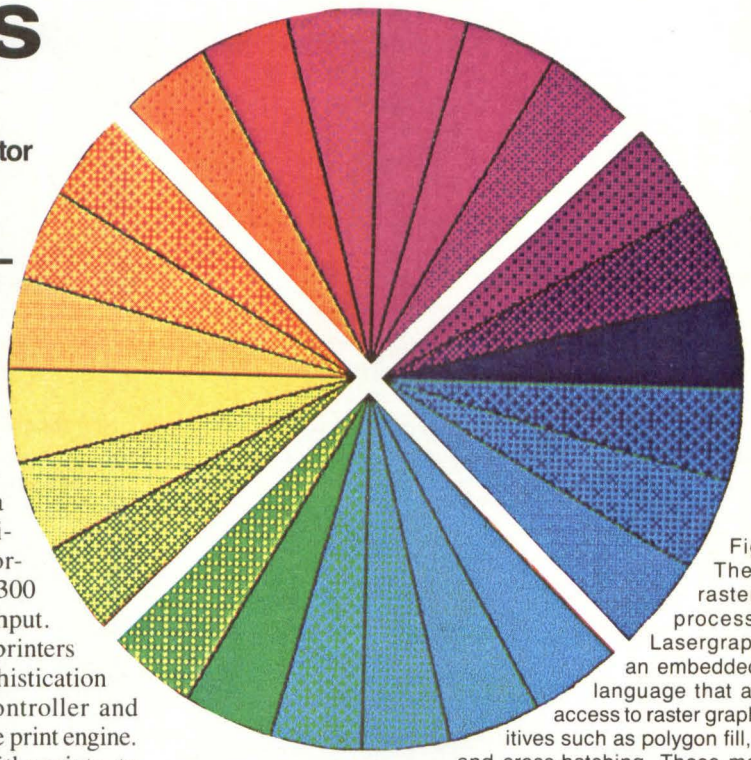

Figure 1: The UI-100 raster image processor from Lasergraphics has an embedded graphic language that allows full access to raster graphics primitives such as polygon fill, shading, and cross-hatching. These merged images were first processed on the UI-100 and downloaded to a Xerox 6500 color printer.

Judging a book by its cover may be a poor rule of thumb for users evaluating the latest generation of laser printers. The use of common print engines such as the LPB-CX from Canon USA (Lake Success, NY), the 4120 from Ricoh (West Caldwell, NJ) or the XP-24 from Xerox Printing Systems Division (El Segundo, CA) means there is little difference in a laser printer's outward appearance or its specifications for resolution and throughput. The majority of printer manufacturers tout numbers like 300 dots/in resolution and 8-24 pages/min throughput.

However, this should not imply that all laser printers are created equal. On the contrary, the true sophistication of a laser printer is attributed more to its controller and associated software than the raw capabilities of the print engine. Therefore, users need to dig deep into the guts of the printer to determine the degree of implementation of such desirable capabilities as text/graphics merging and vector-to-raster conversion. The sophistication of a laser printer controller can fall into two broad categories: printer emulators and raster image processors. Less expensive print emulators offer basic functionality, whereas raster image processors have greater flexibility and use the host CPU less intensely.

Printer Emulators

Printer emulation makes it easier to integrate laser printers into established systems by using existing device drivers for daisy wheel or dot matrix printers. Typically, such controllers intercept commands, in the form of control or escape codes, meant for the emulated printer and translate them into commands understood by the laser printer. Two of these printer emulators are the Laserjet from Hewlett-Packard (Boise, ID) that emulates Diablo 630 daisy wheel printers and the LP-300 from Corona Data Systems (Westlake Village, CA) that mimics Epson dot-matrix printers. Application software need not be rewritten to work with these laser printers.

Robert Harp, chairman of the board of Corona Data Systems, points out that graphic-oriented programs like Lotus 1-2-3 and Multiplan make provisions to access the graphics primitives supported on dot matrix printers. Likewise, text processing programs usually support output on daisy wheel printers.

However, there are disadvantages to printer emulation. Strict emulation limits the functionality of the laser printer to only those capabilities supported by the mimicked device. In terms of graphics capabilities, the resolution output of a dot matrix printer is much lower than that of a laser printer, 24 dots/in for a dot matrix printer compared with 300 dots/in for a laser printer. Likewise, emulating only daisy wheel functions for text output prevents laser printers from providing such useful capabilities as proportional spacing, superscripts, subscripts and italics.

Printer emulators can overcome these obstacles if they dump the images generated for video display directly to the marking engine rather than rely on the control codes issued for the emulated printer. Print engines like the Canon LPB-CX make provisions for screen dumping with a video interface. The resolution is much greater than through emulation of dot matrix printers—ranging from 720 × 380 pixels for IBM personal computers to 1024 × 1024 pixels for graphic display terminals.

Text applications also benefit from bit-mapped graphics since characters can be readily placed anywhere on the screen rather than occupy fixed positions typical for character-oriented graphics.

The Corona Data Systems laser printer can enhance the image by duplicating pixels in horizontal and vertical directions so that the output is scaled properly for the printer. According to Harp, a circle drawn on an IBM PC would appear as an ellipse on the laser printer since the horizontal and vertical resolutions differ.

Still, like printer strict emulation, screen dumping also has limitations. Even the resolution of dedicated graphics terminals does not match the 300 dots/in resolution possible with laser printers. And increasing the resolution of bit-mapped images is difficult. As with photos that are blown up in size, complex images that are scaled up look more "grainy" as pixels spread farther apart. Sophisticated image processing algorithms are needed to duplicate pixels so that the enlarged image has the same amount of detail as the original.

Furthermore, screen dumping relies on the host CPU not only to generate the image, but also to scale and position it on the page. This occurs as the bit map that describes whether any given pixel is on or off is generated. Image generation can easily consume the bulk of a processor's resources and effectively shut out any other task processing. For example, the Xerox 6500 color printer uses a three-pass process that can easily consume the processing resources of a mainframe or superminicomputer to transform the displayed image and download it to the printer itself.

Raster Image Processors

Laser printer controllers have increased in complexity to take on the tasks of image processing and page composition. These

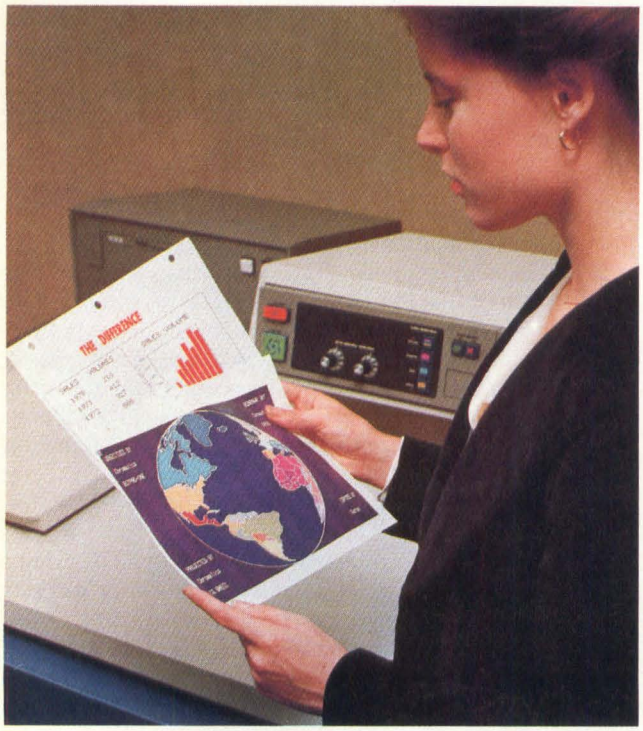

Figure 2: The 6500 color printer from Xerox combines laser scanning and xerography to produce 3 pages/min with 100 dot/in resolution.

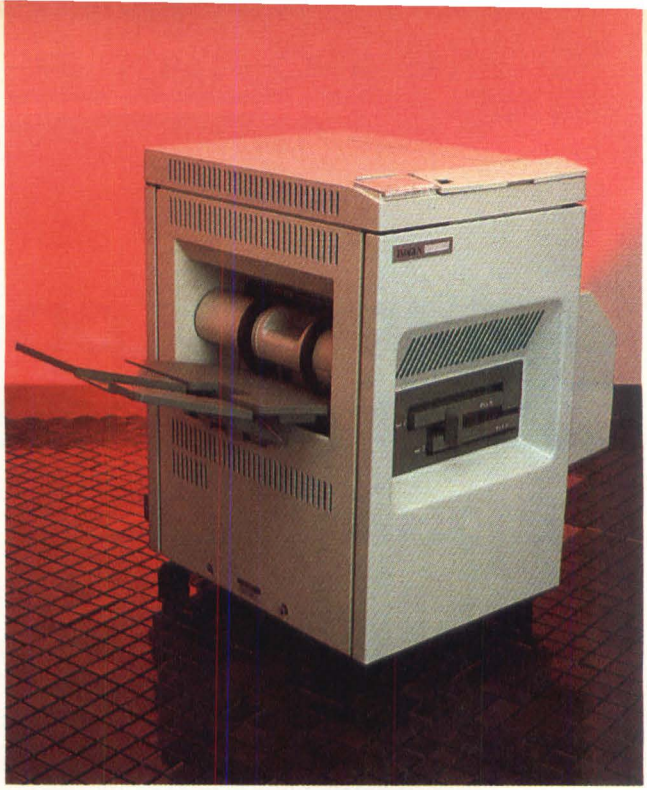

Figure 3: The 24/300 laser printer from Imagen can print 24 pages/min with 300 dot/in resolution and is based on the Xerox XP-24 print engine.

raster image processors (RIPs) are often as sophisticated as a host computer with 16-bit microprocessors and 1 Mbyte of memory to hold bit maps. RIPs have sufficient intelligence to convert graphic primitives like lines, circles, polygons and alphanumeric characters into pixel representations stored for printing. In fact, many of these processors can execute graphic routines directly since they have embedded graphic languages. These controllers include the UI-100 from Lasergraphics (Irvine, CA), the Lasergraphix 2000 and 3000 from Quality Microsystems (Mobile, AL) and the Laserwriter from Apple Computer (Cupertino, CA).

Dedicated processing power can slow the actual throughput of the Canon LPB-CX printing engine from 8 pages/min to 6½ pages/min. This happens because the controller cannot send the bit map to the print engine until the last description is stored. Therefore, pages cannot be preprocessed since the bit map cannot be updated until that last description is printed by the engine. This kind of preprocessing requires separate bit maps for each page. For 300 dots/in resolution printers, each bit map would occupy 1.1 Mbytes to 1.4 Mbytes.

To keep up with the 1 Mbit/sec writing speed of the marking engine, Imagen (San Jose, CA) employs separate MC68000 processors to handle page compilation and actual rasterization. The page compilation engine sets up a pointer list to store images in memory for a selected portion of the bit map memory (typically one to two rows). Since it stays ahead of the rasterizing engine, the page compilation engine can preprocess the display list while the rasterizing engine is feeding the processed bit map to the marking engine. According to Dave Buchanan, product manager with Imagen, memory requirements are also reduced from the megabyte range to 512 Kbytes in the largest controller configuration.

Text/Graphics Merging

Raster image processors only provide the canvas on which images are created. Software is needed to provide the actual form

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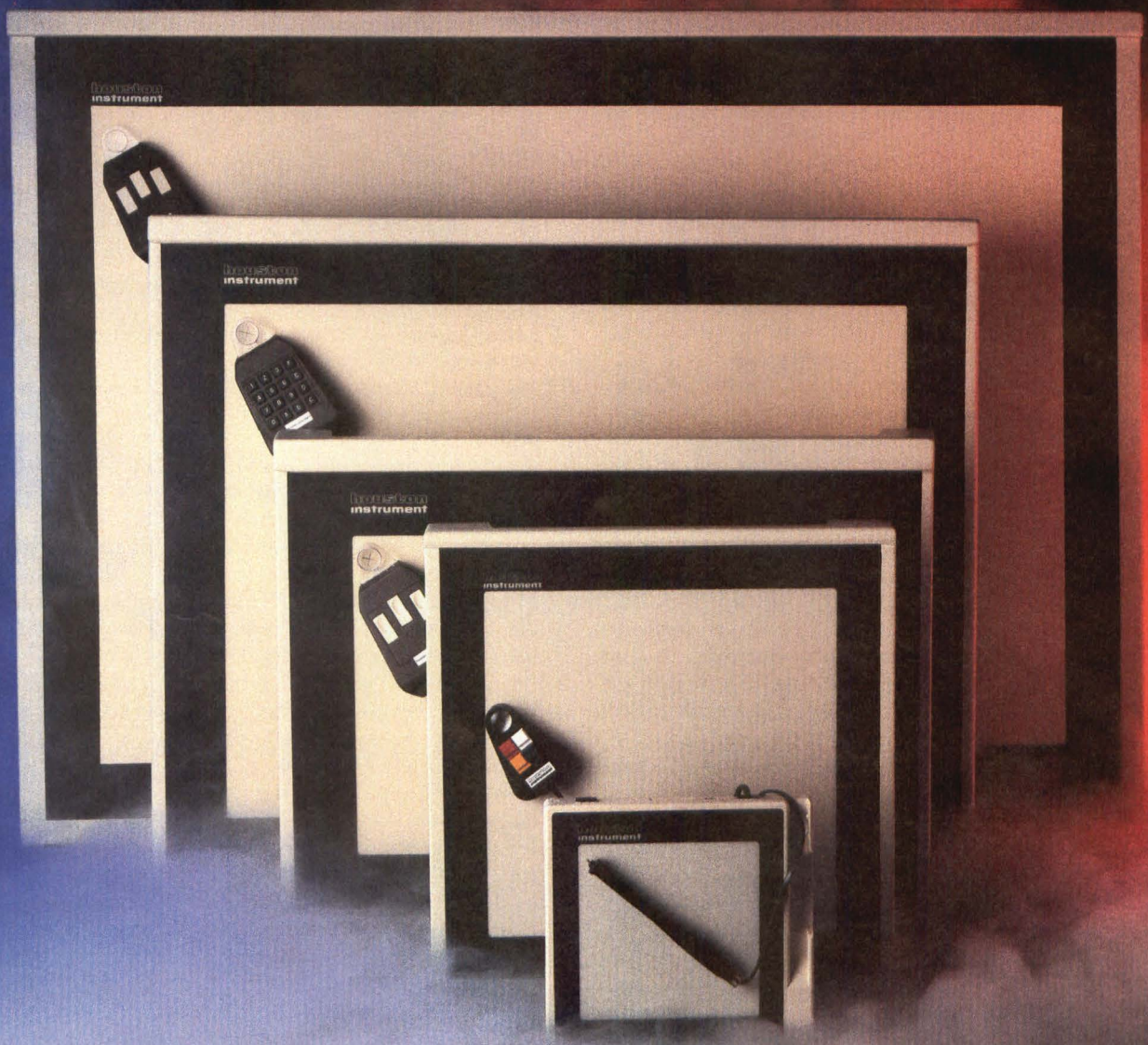

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and texture. For example, software plays a key role in determining a laser printer's ability to merge text together on a single page and its ability to reproduce vector-oriented graphics. In both cases, the sophistication of the software determines the degree to which these capabilities are implemented.

Text/graphics merging deals with the ability of the software to mix different types of information in the same bit map. Text is not character-oriented graphics of fixed size and position. In fact, each letter is a graphic primitive with individual pixels that must be described. Taking a page of typesetting, text fonts describing the graphic characteristics of an alphabet (e.g., uppercase, lowercase, bold, italic) are used to compose words, sentences and paragraphs. These characters must be scaled and positioned on the page in much the same manner as other graphic entities such as circles, lines and polygons.

Yet unlike primitives, bit-mapped characters may not have a fixed spatial relationship to each other. Therefore, the software must be intelligent enough to treat blocks of text as a graphic entity composed of graphic primitives or characters and still allow for the individual placement of characters to accomplish proportional spacing, right or left justification and variable spacing between lines for page composition. Software also must be able to differentiate between text and other graphics images that have fixed spatial relationships.

Beyond allowing maximum flexibility in the placement of text, the software must have the ability to scale and to position graphic images in fixed-size gaps. The issues of scaling images is much the same as that for screen dumping. If an image needs to be increased in size, there must be sufficient detail for the software to duplicate pixels in an intelligent manner. The situation is reversed when an image is scaled down since pixels must be eliminated without losing detail.

The intensity of the processing involved with scaling images for merging with text forces vendors to decide whether to scale images "on the fly" or to defer such processing until the text is already rasterized. Concept Technologies (Portland, OR) chooses to have the text and graphics merged at the same time for display on its IBM PC-based implementation. This requires separate raster image processors for the video display and the laser printer. Talaris Systems (San Diego, CA) has its QDRIVE package process the text portion of the document and leave user-defined windows for size and height for each image to be merged. The scaling of each image is then left as a post-processing step before the final output to the print engine. This approach only relies on the raster image processor in the laser printer.

From Primitives To Languages

How such images are represented is also important – particularly with vector-oriented graphics. Since a vector-oriented image is composed of end points connected by lines or arcs, it must be converted to an image composed of individual pixels in a bit map before it can be sent to the print engine.

Many graphic software packages written for pen plotters like PLOT-10 from Tektronix (Beaverton OR) and DISSPLA from ISSCO (San Diego, CA) are supported by filter routines that convert vector-oriented commands to raster-oriented commands to create such primitives as circles, lines and polygons. Like printer emulation, these filters make laser printers easily accessible from existing software. However, filtering limits the ability of the software to access purely raster-oriented graphic primitives as polygon fill, shading, half-tones and clipping. This approach provides only upward compatibility from vector-oriented to raster-oriented printers.

Figure 4: The LP-300 laser printer from Corona Data Systems prints at a rate of 8 pages/min with a resolution of 300 dots/in. It is based on the Canon LPB-CX print engine.

To provide full raster graphics capabilities, existing software packages can be rewritten in dedicated languages that implement such primitives. Languages like QUIC from Quality Microsystems and ImPress from Imagen allow placement of graphic primitives anywhere on a page. Procedural languages like LL from Lasergraphics and Postscript from Adobe Systems (Palo Alto, CA) not only describe the placement of graphic primitives, but also have high-level control structures so that users can include program logic as well.

Unfortunately, high-level graphics languages make it difficult to work with application programs written in other procedural languages like C, Pascal or Fortran without a well-defined interface to pass controls and data. Concept Technologies overcame this limitation by using the Virtual Device Interface (VDI) as the means to generate graphics primitives (see *Digital Design*, April 1985, p. 66). Application programs written in high-level languages access graphic primitives through a series of library calls. These calls are then interpreted by the raster image processor to generate desired images. This approach provides an effective interface for high-level programs, and isolates the device-independent portions of graphics routines from those sections that deal with the laser printer. This allows programs to be moved easily from one laser printer to another.

Users Beware

Prospective users must carefully weigh the printing needs of their applications against the sophistication of any given laser printer. Basic needs as text output or business graphics can be easily handled by those that emulate dot-matrix or daisy wheel printers. Advanced requirements like text/graphics merging and vector-to-raster conversion will require printers with more advanced controllers and software. Users should be reminded that sophistication is more than skin deep. DD

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Ada And Modula-2: True Systems Languages?

by Brita Meng, Technical Editor

Choosing a language for a relatively large software project is not easy. Over 300 languages exist, each with its benefits and pitfalls. C, FORTRAN and Pascal, in particular, have become popular options for such endeavors, perhaps because they have come the closest to providing the language facilities needed for large projects. But many programmers claim those languages are not ideal. Therefore, two new languages which emphasize program segmentation, Ada and Modula-2, may have considerable impact upon the choices in systems programming.

Although the origins of the two languages are vastly different, Ada and Modula-2 do have some characteristics in common. Both are data abstraction languages, with features allowing encapsulation of data and operations on that data. Each enables low-level programming and machine-level access. And Modula-2 and Ada are strongly typed languages, with the type of a data element completely determining its storage requirements and the uses to which the element may be put.

Ada's beginnings lie in the United States Department of Defense's (DoD) realization that it was spending more on software maintenance than on the hardware for its embedded computer systems. To solve this problem, a group was formed in 1975 to investigate the feasibility of specifying and adopting a common high-level language for use on all embedded computer systems.

Since no existing language completely fit the desired requirements of hardware interface and modularity, the DoD sponsored an international language design competition. A Pascal-based proposal from the design team at CII Honeywell Bull in France was declared the winner and was given the name Ada. The official military standardization document defining Ada, MIL-STD-1815, was released in December 1980. In February 1983, the American National Standards Institute Inc. (ANSI) approved the revised specification, MIL-STD-1815A.

The requirements for the Modula-2 language were defined by Niklaus Wirth, author of Pascal. In 1977, a project was begun in Zurich to design a computer system, later called Lilith, in an integrated approach. Only one high-level language was to be used to program the entire system, requiring additional capabilities for low-level programming of parts interacting with the machine hardware.

Like Ada, Modula-2 is Pascal-based. Wirth also drew on other languages; the module concept came from Mesa, the in-house language at Xerox Corp.'s Palo Alto Research Center. The syntax of Modula-2 is similar to another experimental Wirth language, Modula, which was strongly oriented toward concurrent processing.

The first definition of Modula-2 was released as a technical report in March 1980. However, while Ada has a declared specification, Modula-2 does not. The Modula-2 Group of the British Standards Institute is examining proposals for both language and I/O library standardization; no similar efforts are ongoing in the United States. In the meantime, Modula-2 programmers must use Wirth's book, *Programming in Modula-2*, as the sole guideline for such libraries, resulting in various I/O modules and program incompatibility.

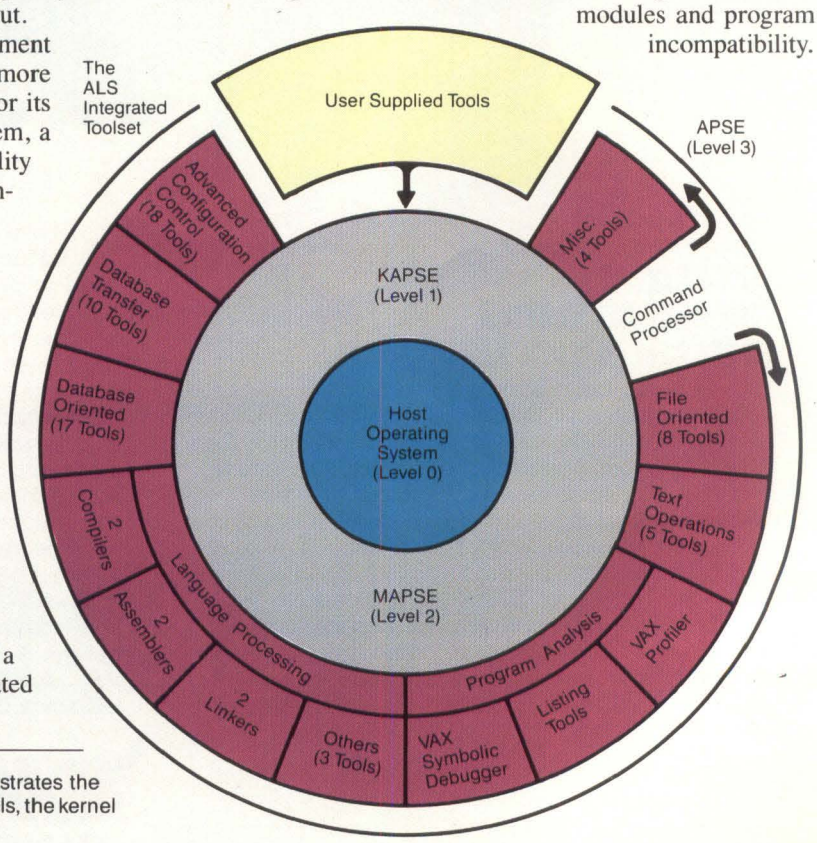


Figure 1: The ALS Integrated Toolset from SofTech illustrates the relationship between the 74 MAPSE and user-defined tools, the kernel and the host operating system.

Features In Ada And Modula-2

Since Pascal was not really considered a true systems-implementation language by many—including its author—several features needed to be included in Modula-2 and Ada which were not available in the base language. The most obvious is the ability to compile parts of a single program separately. This modularity is beneficial during the development of large software projects, when a program may have to be divided into several parts among programmers for coding, debugging and maintenance.

The module in Modula-2 is a defined program unit that groups related variables and the procedures to manipulate those variables. Each module is kept in the program library and referenced whenever a program is loaded and executed. Frequently used operations such as I/O do not need to be reprogrammed each time they are used. Unlike programs in Pascal, a Modula-2 program can be compiled in sections. Object modules can be combined into libraries for later reuse.

An information-hiding feature restricts interaction between sections of a program. A referencing module imports variables and procedures to another module which exports those objects in order to access them. Irrelevant details of the program are hidden while important selected variables are useable by other modules.

Separate compilation normally implies a lack of control over which details of a module are visible to other modules. To solve this problem, the Modula-2 module is divided into two parts for compilation: the definition module and the implementation module. **Figure 2** is an illustration of the definition module; the portions of the module that are visible from the outside are declared. Definition modules declare exported objects as well as any imported objects necessary to declare the exported objects.

The compilation output of the definition module is contained in a symbol file. If the compiler compiles an importing module, it uses the symbol file of the exporting module. Since the compiler makes consistency checks between modules, Modula-2 requires that full information be declared about module interfaces. Even though the language allows separate compilation of modules, compilation is not necessarily an independent procedure.

The implementation module (**Figure 3**) contains the complete procedure declarations for the corresponding definition module and declares any other objects not exported. Compiling an implementation module produces an object file.

The Ada package, like the Modula-2 module, is separated into two parts for compilation and stored within library files. The specification part is analogous to the definition module in Modula-2, containing all the information the programmer needs to know, or is permitted to know, about the package. The first list in a specification package is called the visible part, and items declared in it are accessible to all other program units outside of the package itself. An optional list, the private part, is not visible outside of the package.

The Ada package body is the active portion of the package unit, implementing the declarations in the specification part, like the implementation module in Modula-2. It is inaccessible to the programmer except through the specification.

Another facility Modula-2 and Ada have in common is the capability of low-level programming. The languages do this by including facilities for accessing devices controlled by the computer and breaking the data type compatibility rules otherwise designated by the definition of the language. Specifying an absolute address for a specific data element or routine allows implementation of interrupt handlers and memory-mapped I/O.

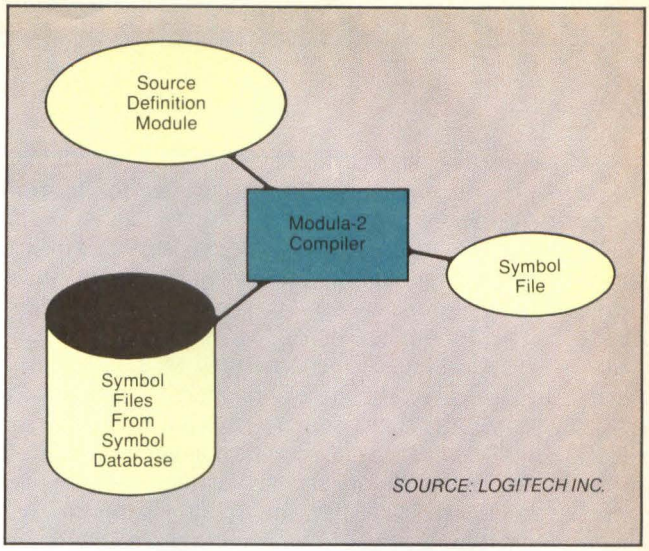


Figure 2: The definition module in Modula-2 acts as the interface between the module and the external world.

Strong typing is also characteristic of Modula-2 and Ada, but both are more lenient than their ancestor Pascal. Modula-2 provides implicit type conversions in some situations, e.g., when a value is assigned to a differently typed data element. The function VAL allows the recovery of enumerated values from unsigned integers. A built-in function does type conversion on certain data types; unfortunately, this feature appears to be system-dependent.

Ada enforces strict typing like Modula-2 and possesses similar built-in functions for type conversion. However, the types available to be shared and converted in Ada are better defined than those in Modula-2; the procedure is independent of any implementation.

All languages allow the explicit transfer of control from one part of a program to another. Ada and Modula-2 provide more structured methods of control transfer through such constructs as procedures, functions, conditionals and loops. In both, the return statement for either a procedure or a function cuts the procedure or function off and transfers control back to where it was called. Because neither Ada nor Modula-2 have a distinct syntactic which represents the result of the function, the programmer must explicitly specify an appropriate return value, as in C. Reaching the end of a function without a return statement generates a run-time error.

Exit statements within a program loop in Modula-2 and Ada allow the programmer to transfer control directly to the first statement after the loop. Ada allows exits from nested loops of any depth. In Modula-2, only the innermost loop can be exited easily; this may lead to unnecessary code in escaping from deeply nested loops.

Statement lists in the two languages, such as those in conditional, loop or case statements, must be terminated in some fashion because of the lack of explicit bracketing for the beginning and end of such constructs. Ada's solution may be more helpful in determining the cause of syntax errors: END IF, END CASE and END LOOP. Modula-2 simply reserves the word END for all three.

Ada is a much larger language than Modula-2 because it has

more facilities. And although robustness of a language is important, Modula-2 programmers claim that the extent to which this occurs in Ada creates problems when writing a good Ada compiler, as well as when learning the language. Mastering Modula-2, especially if a programmer is familiar with Pascal, may take less than a week; proficiency in Ada is not as easy to achieve.

Programmers of Ada have dubbed Modula-2 "the poor man's Ada" because it lacks some of Ada's features. Modula-2 is a bare bones language, relying upon the library for facility additions. Although some Ada features such as exception handlers and generics can be duplicated to a certain point in the Modula-2 libraries, the lack of library standardization may mean that several versions of such modules may result. Examples of Ada features unable to be written in Modula-2 are overloading and representation, the ability to specify what a floating point or fixed point number looks like. Both these facilities add size to the Ada language.

Ada gives the programmer strict control over the size and relative location of data elements. In Modula-2, the compiler controls the size and the location only within each memory area. This fact may create problems in the generation or the use of predefined, externally formatted data, when control over an element's size and location is necessary.

Overloading in Ada allows a situation in which the same identifier is used in several different specifications within the same subprogram group. The compiler must then choose the correct identifier meaning, according to its context. Basic operators such as addition, subtraction and multiplication can be redefined in Ada. However, many programmers question the benefits of overloading because it may lead to ambiguities within a program. For example, if 5 is added to a pointer, it may refer either to 5 bytes or 5 structures. Unless an overloaded procedure, function or operator is clearly documented, a maintenance programmer may not be able to understand what the original programmer did.

Error situations which may occur during program execution are called exceptions. Certain ones, for example an arithmetic error such as division by zero, can interrupt execution at almost any point in the program. Testing continually for such errors may not be feasible. Ada provides for these circumstances by allowing exception handlers, which are essentially case statements with one response branch for every possible exception. Every time an exception is raised, the appropriate branch is taken. However, Ada exception handlers cannot return the program to the place where it occurred after the routine has dealt with it. They merely keep the exception from propagating. Modula-2 does allow exception handlers to be built into libraries.

Modula-2, since it was designed for implementation on a single-processor computer, offers only basic facilities for the specification of quasi-concurrent processes and of genuine concurrency for peripheral devices. These processes are actually coroutines, or processes executed by a single processor one at a time, and are considered to be low-level facilities.

The monitor is a module which guarantees mutual exclusion of processes, in addition to mutual exclusion of data access. Specifying a priority value in a module heading makes it a monitor, to which all process interaction should be confined. However, because the monitor should be implemented on a single-processor computer, concurrent interaction is impossible by definition. A module priority heading is therefore redundant.

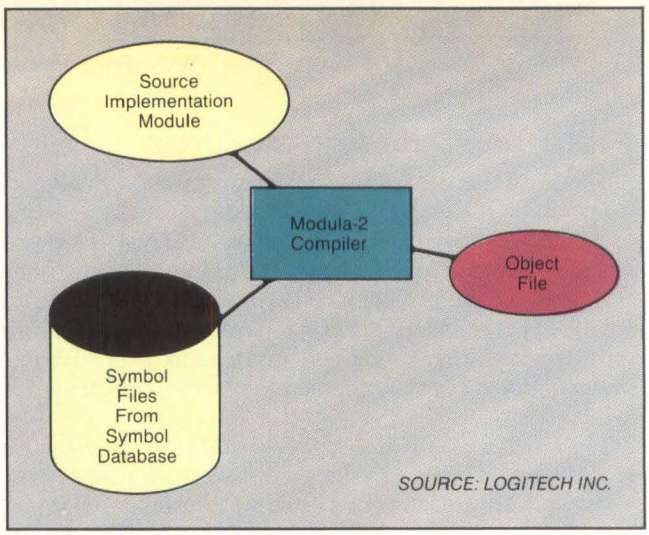


Figure 3: The implementation module in Modula-2 implements the data of the definition module into a form useable by the external world.

In Ada, a task is a nested program entity operating within either procedures or packages which permits real-time concurrent, or parallel, operations between two or more program units. Multiple concurrent tasks may execute on either a multiprocessor system or a single computer. The distance between microprocessors implementing any number of tasks is unimportant, as long as these tasks are under the control of the same procedure. The rendezvous is a control mechanism, which synchronizes two or more tasks for communication, data exchange or both. It occurs after an entry point in the specification of a task is called by the calling task and the called task accepts the call with an accept in its body. Until the accept is reached, the calling task goes into a wait state.

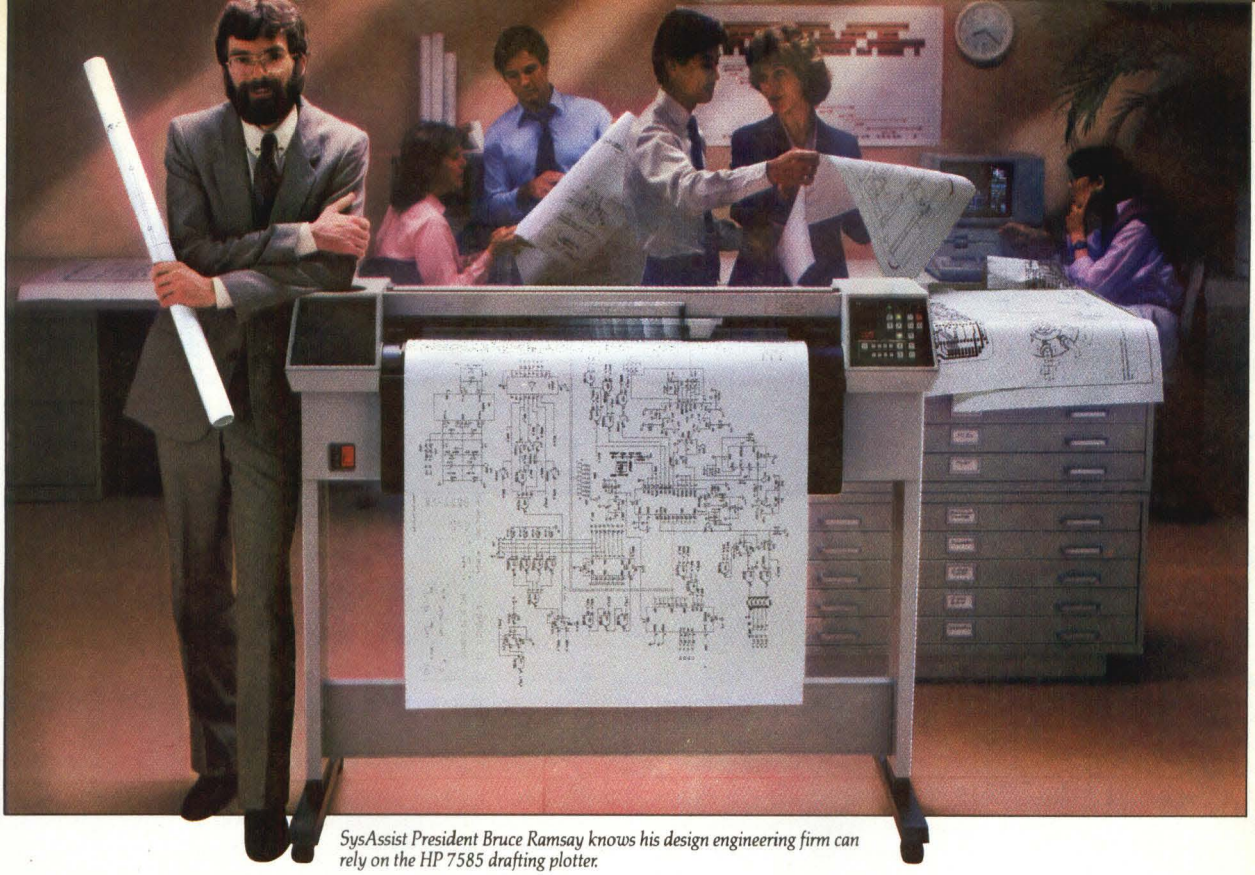
Some programmers claim the rendezvous construct, peculiar to Ada, has no place in a low-level systems-implementation language. Others claim the task approach to real-time parallel operations is a significant step in multiprogramming.

A feature of Ada unable to be completely duplicated in Modula-2 is generic program units or generics. These units are basically program modules that are templates of algorithms, written in general form, that can be customized for any number of applications during compilation. The same generic unit can be used over and over again within one program.

Implementing a generic requires the specification of a collection of parameters along with a routine or package which uses those parameters. Although the algorithm is shared, each instance of a generic produces not only a new version of the underlying routine or package, but also a new piece of Ada code. This means that each copy of a generic requires its own memory.

The use of generics is therefore a sophisticated compile-time process, which can be a large burden on the compiler. One beta test site for DEC's (Maynard, MA) VAX Ada compiler found that the compiler could run up to 2000 lines per minute without generics. With generics, however, the speed of the compiler fell below 1000 lines per CPU minute. The importance Ada programmers attach to generics is illustrated by the fact that many predefined packages in Ada such as TEXT_IO and INPUT_OUTPUT are actually generics filed as library units.

Modula-2 allows procedures and functions to be passed as parameters whereas Ada does not. For example, if a parameter



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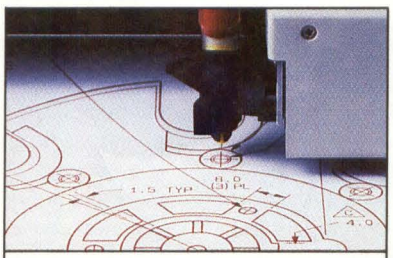

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of a procedure is given the type WORD, its corresponding actual parameter may be anything, including a function, that returns the type WORD without requiring an explicit type transfer. This solution could be a problem because all type checking by the compiler is bypassed.

Functions and procedures can be dealt with as data values in an arbitrary data structure, not just as parameters to a routine in Modula-2. Specifying the number and the types of parameters allows types whose values are procedures to be declared and indicating the type of the result enables the same for types whose values are functions. Such procedure types can be located anywhere in memory and can be included in high-level structures as well as low-level structures.

Support Tools For Ada

The primary reason for the dearth of Ada compilers is the size and complexity of the language. Since the DoD expected only one compiler to be built under military contract for military use, Ada was not designed for ease of compilation. Only two companies have government contracts for compiler development, Intermetrics (Cambridge, MA) and SofTech (Waltham, MA). All the other companies developing Ada compilers, more than the DoD expected, are doing so without major government funding.

One of the primary goals in developing Ada was language standardization. The Ada Joint Program Office (AJPO) created a group called the Ada Validation Facility (AVF) to supervise the administration of a validation test suite which determines how fully an Ada compiler implements the language. The Ada Compiler Validation Capability (ACVC), developed by SofTech, consists of approximately 2000 tests. Most of them are relatively short programs, 15 to 20 lines, intended either to compile correctly and run or to generate specific error messages.

The AJPO keeps a list of all validated Ada compilers, in addition to tracking the status of all other ongoing Ada development projects; this information is available to the public. Most of the validated compilers are currently marketed, as are several compilers which are in the process of being validated or completed for the validation test.

Most companies agree that the test suite is necessary to maintain the standardization of the Ada language as well as the portability of Ada compilers. However, compiler developers and Ada programmers have one major complaint about the validation suite: it does not evaluate code quality, compiler speed or compiler bugs. Nothing internal to the compiler is evaluated. Instead, the suite seems to concentrate on testing the potential misunderstandings of the language definition in the Ada manual.

As a result, most of the Ada compilers which have been validated by the ACVC are slow, awkward and large. Compiled Ada code can be very cumbersome; with all of the exception handling and tasking checks, the code generated is usually an "expansion factor" larger than the source code. Indeed, the only Ada compiler which has been used in an actual in-flight military situation is an unvalidated one from Irvine Computer Science Corp. (Irvine, CA). In response to the complaints, work on a validation test suite to evaluate compiler optimization, called the Ada Compiler Evaluation Capability (ACEC), has begun.

It costs approximately $15,000 (not including travel, per diem fee or the estimated cost of stopping work at the company during formal validation) to validate one host/target compiler combination. In addition, each combination must be revalidated every year to maintain its good standing with the AJPO. The complex procedure ensures that the AVF does not waste its time on compilers which are not ready to be validated and requires that a company set a strict timetable for validation before it even begins the official procedure. If a deadline is missed, the company forfeits its place in line and must reapply for the initial scheduling step.

Program portability is a promise of the Ada language but is not yet a reality. The many existing Ada development systems are, for the most part, hosted on and targeted to the same system. The question then becomes how to make the differences within various host or target operating environments transparent to an Ada compiler or applications program.

These interfacing problems fall into a lowest level of the Ada Programming Support Environment (APSE) called the Kernel Ada Programming Support Environment (KAPSE). The APSE (**Figure 1**) is the DoD's approach to an integrated programming support environment, calling for a hardware-independent user interface to the host computer operating system and a set of coordinated tools to support the software system throughout its life cycle.

The KAPSE is the APSE link to the host computer operating system; it is unique to each host and is not transportable. The Minimum Ada Programming Support Environment (MAPSE), the middle level, is the programmer interface to the APSE and when complete, contains software tools ranging from language translators to debuggers to project management support facilities. Software on the MAPSE level can be moved from one host to another.

A number of Ada programming environments have been or are being developed along the lines of the APSE. SofTech received the Army contract for the Ada Language System (ALS) and delivered its product earlier this year. The company's version of the ALS for the Navy, the ALS/N, is well underway. Intermetrics has the Air Force contract called the Ada Integrated Environment (AIE). Other companies such as Gould (Ft. Lauderdale, FL) and Vertix (McLean, VA) also have completed environments.

Ada is one of the only languages standardized before its implementation; this fact could result in some problems for applications programming. Computer Corporation of America (Cambridge, MA), which wrote a relational database management tool in Ada was satisfied with the language capabilities but is concerned about the DoD mandate against Ada extensions, which it did have to use. The mandate may hamper application programmer productivity and program portability and may even limit the efficiency of program execution. Because of its strict standardization, many programmers question Ada's ability to break out of the military domain and into commercial programming. And the proliferation of unvalidated Ada compilers defeats the whole idea of an established standard.

Support Tools For Modula-2

Modula-2 compilers have also been hard to find, despite the claim that the smaller a language is, the easier it is to build a compiler. The main reason may be that the language is simply not well-known enough and therefore fewer companies are building compilers. Ada has the DoD's support, but Modula-2 is relying on a grassroots movement in order to gain popularity.

Unlike Ada compilers, many Modula-2 compilers are available for microcomputers. The variety of offerings on the larger machines is not as great as that of Ada, though it is growing.

Modula-2 compilers also cost much less than those for Ada. The cost differential is due to the development cost for Ada compilers and the definite military market for them.

Despite this relative lack of compilers, Modula-2 is slowly beginning to make strides in the programming world. Several companies, such as DEC (at the Western Research Facility) and McDonnell Douglas, are using the language for experimental systems development. Tartan Laboratories (Pittsburgh, PA) has even written the front end of a validated Ada compiler in Modula-2. Other companies such as Elite Computers (Wichita, KS) are beginning to change over to Modula-2 as the primary programming language for commercial products. Even general purpose applications software written in Modula-2 is currently available.

Programming environments for Modula-2 have also been slow to develop because of the lack of financial support behind the language. Environments are available from Interface Technologies (Houston, TX) and Pinnacle Systems (Houston, TX). But no standard document for a Modula-2 programming support environment exists; again, this could be a problem should the language become widespread.

To most Modula-2 programmers, the main problems facing the language are the lack of language standardization and the lack of a validation suite for Modula-2 compilers. One suite, currently in beta test this summer, is expected to be released soon and will be distributed by the British Standards Institute. In offering such a validation suite earlier in the language life cycle, Modula-2 may avoid the problem of language extensions which has plagued Pascal.

Conversely, some programmers fear doing so will stagnate language development, believing that the versatility of Modula-2 results from its flexibility. They cite the potential problems caused by the DoD Ada directive as something to avoid with Modula-2. It seems that most programmers believe the primary drawback of Ada is its strict standardization while the main complaint about Modula-2 is its lack of such.

Supporters of both Ada and Modula-2 claim that each respective language has the potential to supplant Pascal and even C because of their modularity. In order to do so, factors such as educational support and support tools, which helped popularize C and Pascal, will also play a large part. Ada may do everything – but not well. Modula-2 does things well – but does not do everything. Since both languages are new, perhaps only time will tell whether one or both will become standard systems programming and applications languages. DD

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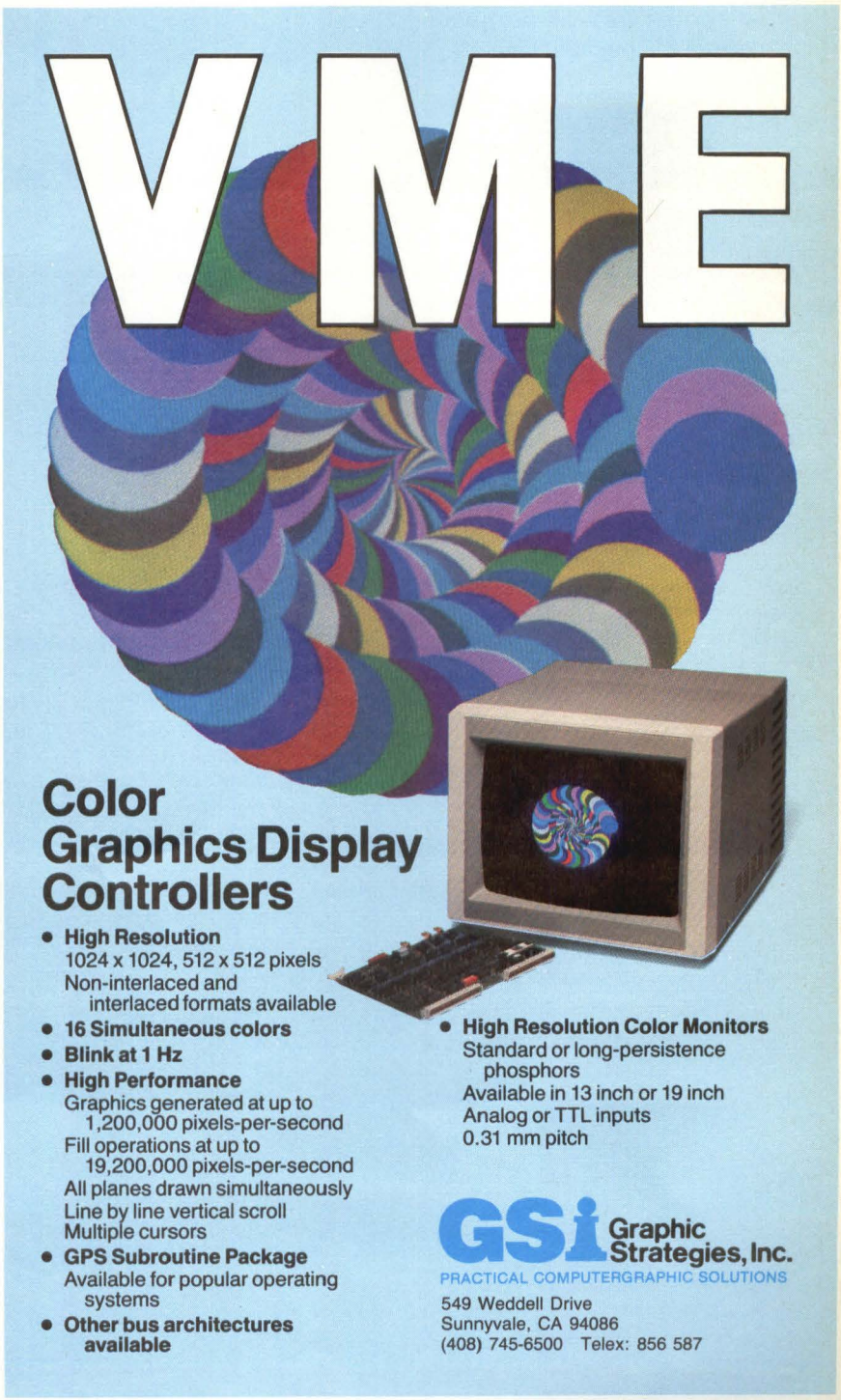

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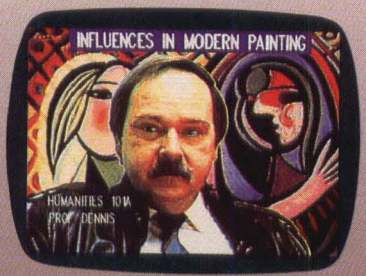

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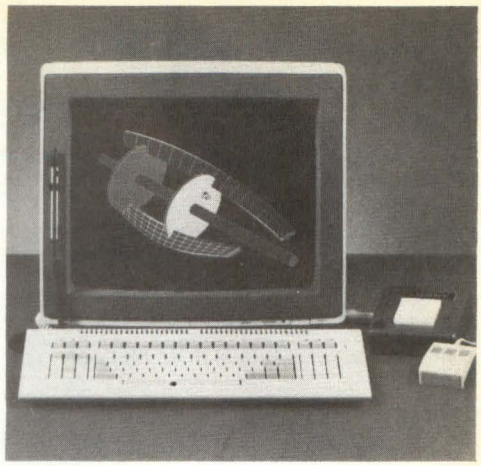
NEW PRODUCT FOCUS

S Y S T E M S

Five Color Raster Graphics Workstations



Lundy Electronics and Systems (Glen Head, NY) has added five graphics workstations to its product line; all are color raster models, and most use a dual graphics engine.

The GTC-327 is a replacement for the TEK 4027. With a dual graphics processor, 14″ monitor with antiglare filter and detachable keyboard, the GTC-327 gives users the capabilities of the 4027 while supporting their software. Resolution is 640 × 480 and eight colors can be displayed simultaneously from a palette of 4096. Priced at $4,100, the GTC-327 is more compact than the 4027 and offers two RS-232 ports at speeds up to 19.2 Kbaud. An auxiliary port supports graphic I/O devices.

Designed to compete against PC-based systems, the Lundy 2000 standalone workstation supports CP/M-86 and MS-DOS operating systems, as well as Fortran, Cobol and Pascal. The 80186-based system simultaneously displays 256 colors from a palette of 16.7M with a resolution of 768 × 512 pixels. With a 15″ tilt/swivel monitor, the 2000 is priced at $21,900 with substantial quantity discounts. The Lundy 2000 also offers two DMA channels, three event counter/timers, a 256K RAM and a single side, double density, 48 tpi floppy drive.

Similar to the 2000, except for lower resolution and greater storage capacity, the Lundy 3000 is designed for printed circuit board design, chemical and molecular modeling and architectural floor plans. With a 19″ diagonal monitor, the 3000 also displays 256 colors simultaneously from a 16.7M palette at a resolution of 1536 × 1024 pixels. Its price is $26,800, with quantity discounts also available.

A 3D color raster workstation, the UltraGraf III is software compatible with its predecessors, the UltraGraf and UltraGraf II. With up to 16 bit planes, the UltraGraf III sports a 19″ monitor and displays 256 colors simultaneously from a 16.7M palette and has a resolution of 1024 × 1024. Priced at $45,995, it can run the PDGS (Product Design Graphics System) software, suited for automotive manufacturing, allowing automobile suppliers to use color.

Finally, aimed at the process control industry, the LT5684 is a second generation product of the Lundy 5000 series. Using a nonmembrane touch screen, giving a fairly bright display, therefore reducing eye strain, the LT 5684 displays 16 colors from a palette of 4096 with a resolution of 768 × 512 pixels. All of Lundy's graphics workstations are available immediately.

—Lamneck

Circle 233

C O M P O N E N T S

Chip Supports Multiple Interfaces

The OMTI 5080 SCSI multifunction chip from Scientific Microsystems (Mountain View, CA) supports multiple device- and system-level interfaces. The chip replaces most of the discrete logic needed to implement the Small Computer System Interface (SCSI). The chip provides similar support for the QIC-02 and ANSI X3T9.6 streaming tape interfaces as well as fixed disk interfaces such as ST506/412, ST412HP and Enhanced Small Disk Interface (ESDI).

In its primary role to support SCSI applications, the chip provides the necessary control signals and handshaking logic for host and target roles – including arbitration and selection/deselection. Furthermore, users can implement any version of the ANSI X3T9.2 specifications for either single- or multiple-host configurations since the timing involved during the arbitration and selection phases are programmable from the clock input. The chip can be used in either the host adapter or peripheral controller, or embedded on the tape and disk drives that have SCSI ports.

When used to support disk interfaces, the 5080 chip handles as many as four drives at asynchronous data transfer rates as high as 1.5 Mbytes/sec. It has single-ended drivers and receivers suitable for connecting disk or tape drives and provides six bus driver ground pins.

The 5080's separate DMA and I/O paths allows overlapped DMA transfers. Its internal registers can be programmed by any eight-bit microprocessor to control the type of interface support, I/O or DMA transfer mode, interrupt mode, bus parity checking, and hard and soft reset modes.

The 5080 chip complements other members of the company's chip family, such as the 5050 data sequencer and 5060 DMA controller. The 5080 interface chip is fabricated in CMOS to provide low power consumption (50 mA). Price is $15 in quantities of 10,000.

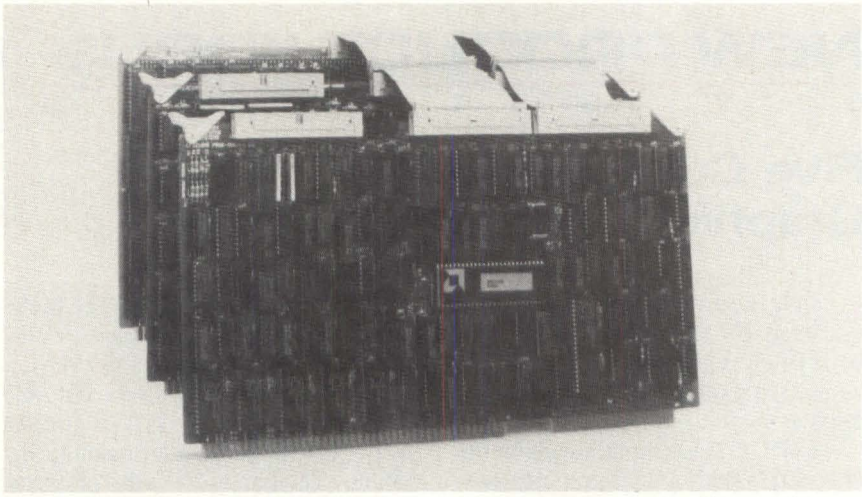
—Aseo

Circle 231

Floating Point Processor Enhances Array Processors' Performance

The ZIP 3232 8- and 16-MFLOP array processors from Mercury Computer Systems (Lowell, MA) use the AMD 29325 chip. A three-board set for the Q-Bus and Multibus, the ZIP is supported on Sun, Intel and Motorola systems, as well as the MicroVAX II.

Geared for signal, image and scientific processing, the ZIP 3232 has a typical performance of 2.8 msec for a 1024 point complex FFT, 279 msec for a 3 × 3 convolution on a 512 × 512 image, 1.9 μsec/output for a 16 tap FIR filter and less than 0.75 sec for a two-dimensional FFT on a 512 × 512 image. The ZIP 3232 is built using the same architecture as the ZIP 3216 16- and 32-bit block floating point coprocessors. The control processor, based on the AM 29116, is on one board; memory (128 Kbytes expandable to 16 Mbytes) is on another; and the arithmetic processor is on the third. Only one board needs to be designed to upgrade the ZIP 3216 for 16- and 32-bit block floating point computations. The programming environment features the ZIP/C compiler and off-line development tools for program writing, debugging and benchmarking on computers including the VAX, 68000-based systems and IBM PC, without the hardware present.



The ZIP can interface directly to external devices through its 32 Mbyte/sec internal bus, through discrete I/O channels or through the host interface.

Currently available on Multibus and Q-Bus, the ZIP 3232 is expected to arrive on the VMEbus later this year. It is supported under UNIX System III and V, Masscomp RTU UNIX, Sun-Berkeley UNIX, Idris, Regulus, RSX-11M, RT-11, MicroVMS, iRMX and VersaDOS.

The 16 MFLOP version is priced at $15,000 and the 8 MFLOP is $11,500, with discounts up to 35%.

—Lamneck

Circle 232

High-Level Debugging Moves To Target

TargetSCOPE 186 from Intel Development Systems Operation (Hillsboro, OR) moves symbolic debugging from the host CPU to the system. With TargetSCOPE users can download, execute and modify high-level language programs (C, FORTRAN, Pascal and PL/M) running on 80186- and 80188-based systems. The debugger executes on the Intel's Intellec Series III or Series IV development systems, as well as the IBM PC-XT or PC-AT.

TargetSCOPE serves as an intermediate step between the PSCOPE software debugger and the in-circuit debugger found in the company's I²ICE emulator. All provide source-code symbolic debugging with the ability to single-step through source code statements as well as entire routines. To effectively perform this task, the symbol tables generated by the high-level language compiler must be accessible by the linker, loader and symbolic debugger. In addition, these debuggers must have the ability to insert breakpoints (at either the source code or assembly language level). This allows program execution to be halted when necessary, as well as trigger a trace history of bus transactions.

TargetSCOPE can run without imposing processor wait states since it utilizes a special bondout version of the 80186 chip on its hardware probe (see *Digital Design*, June 1985, p. 75). User programs execute out of its 96 Kbyte memory space, while programs of up to 1 Mbyte can be mapped into the prototype hardware in 1 Kbyte increments. This allows entire programs to be executed at full-speed until the flagged instruction is reached.

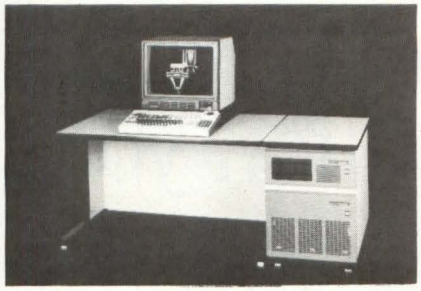
TargetSCOPE shares the same command interface as Intel's other debuggers and it is priced at $5,495.

—Aseo

Circle 230

COMPUTERS/SYSTEMS

Color Graphics Computer



Designed for mapping, CAD/CAM/CAE, command and control, the CM 1024 colorgraphic computer combines a 19″ 1024 × 768 60 Hz noninterlaced monitor with a display engine digital drawer for both host-driven and workstation applications. The digital drawer, processing 64,000 vectors/sec, features a 16-bit MC68000 processor, 4K CMOS RAM, hardware vector generator, 24-slot card cage, plotting, complex fill and raster processor graphics. Available software includes the IDRIS operating system, Fortran 77, C, Pascal and DI 3000 Extended. Storage is up to 80 Mbytes fixed. Price is $23,995. **Chromatics**, Tucker, GA **Circle 127**

32-Bit Target/Development System

Based on the Series 32000 μP family, which supports demand-page virtual memory, the VR32 Target/Development system can be used for Series 32000 software development or can be implemented directly as the application target system. A Multibus system bus with four empty slots provides the hardware development for Multibus-based applications. Development tools for the VR32 include an editor, C compiler, Series 32000 assembler, linker, symbolic debugger and all Genix operating system utilities. Price is $14,450. **National Semiconductor**, Santa Clara, CA **Circle 137**

Performance Enhancement Packages

Similar to a 16 MHz 68020- based CPU, these Performance Enhancement Packages are intended to increase base-level performance of the firm's 500 Series systems. The PEP-501 package consists of a 16 MHz 68020-based CPU and 2 Mbytes of memory incorporating 256K memory chips. The CPU contains instruction and data cache with a MMU. Also included are a 32-bit memory interconnect bus for the 68020 and a floating point processor chip. The PEP-502 package incorporates a board-level floating point processor designed to increase system performance and a 16 MHz CPU, memory and interconnect bus, identical to the first package. Prices are $7,900 (501) and $12,900 (502). **Masscomp**, Westford, MA **Circle 133**

μP Development System

Providing real-time hardware/software emulation support for the MC68HC11 microcomputer and the MC6809/MC6809E and M6801/03 μP families, the HDS-300 μP/microcontroller Hardware Development Station is a standalone system, requiring only the target object file from the host system. Almost any terminal with a standard RS-232-C port can be used with the HDS-300. It consists of a control station with a built-in 5¼″ disk drive for program execution to the target processor, user target code, user macros and terminal configuration data. **Motorola**, Phoenix, AZ **Circle 136**

System Development Engine

Capable of simulating 1.5M gates at 1 billion events/sec, the System Development Engine incorporates a distributed modeling technique with supercomputer architecture. The system can be integrated into an existing CAD system using Zilos software interface or other translators from the company. Other features include event-driven, hardware-based algorithms, 12-state simulation, interactive speeds, selectable reporting and self testing. **Zycad**, St. Paul, MN **Circle 140**

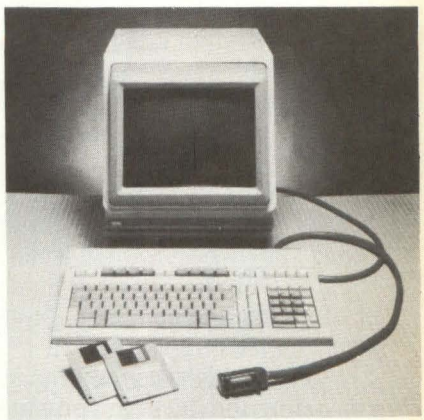
Multibus Multiuser Microcomputer Systems

The SMS 8000 Model 50 microcomputer system is available in many custom versions. All are based on an SMS Foundation Architecture and include system enclosure, a choice of fixed/removable peripherals, 8086/80286 processors and up to 16 Mbytes of main memory. Multibus compatible, the system will run all software developed for Intel's RMX 86/286 or Xenix operating systems, and CP/M-86, and UNIX system V and concurrent CP/M-86/286 which will be available soon. Price starts at $6,800 with the foundation module, one serial port, 12 Mbyte Winchester, 5¼″ 700-Kbyte floppy, 8086 CPU and 512 Kbytes of main memory. **Scientific Micro Systems**, Mountain View, CA **Circle 131**

Full-Color DASH Schematic Designer System

A full-color version of the DASH PC-based CAE workstation, DASH-3C, allows a designer to assign a preferred color or use of the system's predefined default colors to identify four separate groups of graphic display elements. The complete system includes an IBM PC, XT or AT with minimum of 256K RAM; an IBM enhanced color display and enhanced graphics adapter board with graphics memory expansion card; an IBM keyboard, MS/DOS software; mouse and parallel port board with cable and modular plug and a C.Itoh 15″ Prowriter II printer with cable and DASH-3C software. Prices are $5,980 (add-on package) and $10,880 to $14,380 depending on the IBM included. **Futurenet**, Canoga Park, CA **Circle 132**

Touchscreen Technical Personal Computers



These two touchscreen PCs integrate business and technical applications. The Touchscreen HP-IB controller and the Touchscreen PC-IB controller enable users to perform test/measurement procedures and run many MS-DOS software packages currently available for HP Touchscreen PCs: 1-2-3 Lotus, Wordstar and PFS. The HP-IB controller consists of a Touchscreen II base system, the HP-IB command library and the Touch accessory. The PC-IB controller consists of a Touchscreen II base system, the HP Touch accessory, a 384K RAM memory board, a PC instruments interface and GW Basic. Storage for both can be a 3½″, double-sided microfloppy with 710 Kbytes capacity each or 3½″ Winchester disk drives with 10 or 20 Mbytes capacity. Prices are $4,395 (PC-IB) and $4,495 (HP-IB). **Hewlett-Packard**, Palo Alto, CA **Circle 139**

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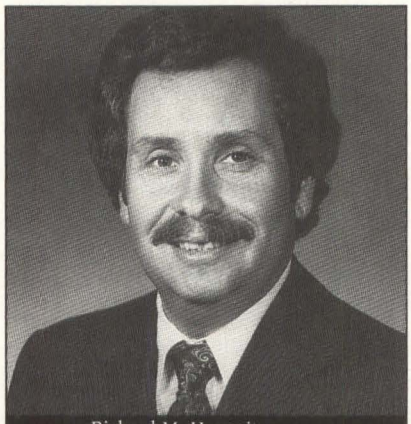

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Allowing programming in the conventional mode or in an intelligent mode (offered by Fujitsu and Intel), the AVAL PKW-1000 programmer programs a variety of MOS, CMOS EPROMs and EPROM-based single chip microcomputers and operates as a gang programmer. A 64K buffer RAM allows data edit and storage, and a 2K CMOS system RAM stores system parameters up to two months after the unit has been turned off. A hexadecimal keypad, a contrast- adjustable 2 lines × 16 characters LCD display and built in interfaces for RS-232-C and Centronix-compatible equipment are among standard features. Price is $1,600. **ECD Industries**, Los Angeles, CA **Circle 129**

7-Slot Multibus Enclosure

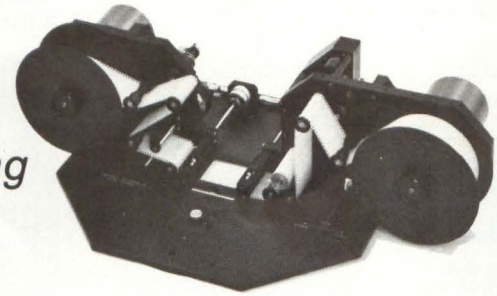
With power and mounting provisions for two 5¼" half-height peripherals and room for a full-height 5¼" Winchester drive, this 7-slot Multibus chassis (SE-607) includes a 225W switcher. Available in tabletop or rackmount, the enclosure is designed to meet FCC part 15 class A EMI/RFI specs. Vertical rack height is 7". The two half-height peripherals are accessible through standard bezel openings. A variety of P2 backplanes are available, including an iLBX bus. Prices are $1,695 (tabletop) and $1,795 (rackmount). **Electronic Solutions**, San Diego, CA **Circle 130**

PCB Layout/Design Workstation

A workstation for the design and layout of PC boards, the Boardmaster system integrates CAE and CAD functions. It performs engineering and layout functions including schematic entry, logic simulation, timing verification, automatic placement and routing and CAM outputs. The Boardmaster uses a gridless router with an approach based on the actual geometry of the board and its design rules rather than on artificial grid or channel routing. The system also performs component packaging. Available in September, Boardmaster's price is $110,000. **Daisy Systems**, Mountain View, CA **Circle 138**

Film Transports

with electronic drive systems for film recording or retrieval of information



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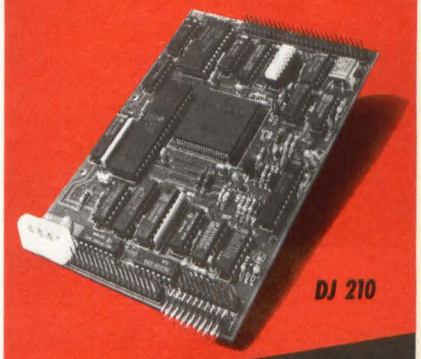
3½ INCH DRIVE-MOUNTABLE HARD DISK CONTROLLER

ST-506/412 to SCSI/SASI



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Circle 62

Automated VLSI Design Systems

An addition to the firm's Genesil family of automated VLSI design products, the Genesil 100 and Genesil 500 Silicon Development Systems design application-specific ICs, working from high-level functional descriptions from the user. The Genesil 100 is a single-user, MicroVAX II-based system with 2 Mbytes of RAM, 184 Mbytes of hard-disk storage, a 95 Mbyte magnetic tape drive, an 8-port RS-232 I/O interface, a color graphics terminal, a 1200-baud modem and the Ultrix operating system. The five-user Genesil 500 system is based on the ll/785 VAX and provides 8 Mbytes of RAM, 450 Mbytes of hard-disk storage, a 1600 bpi 9-track magnetic tape drive, two 8-port RS-232 I/O interfaces, two 1200-baud modems and UNIX Berkeley 4.2 BSD operating system. Prices are $165,000 (Genesil 100) and $640,000 (500). **Silicon Compilers**, San Jose, CA **Circle 126**

Functional Equivalent Of IBM 3270/PC With Graphics

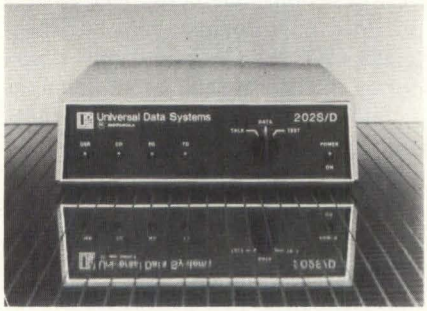
IRMAX Graphics, a hardware and software package enables an IRMA-equipped IBM PC, IBM PC/XT/AT or compatible to function as an IBM 3270/PC with graphics. It is compatible with IBM's host-based Graphical Data Display Management Systems (GDDM) and operates in a SNA teleprocessing environment. The product also allows a PC to function as an IBM 3278 S3G or IBM 3278 S2G monochrome terminal or an IBM 3279 S3G or IBM 3279 S2G color terminal. Display hardware supported with the color displays include IBM's enhanced color graphics adapter and Tecmar's Graphics Master card. **Digital Communications Associates**, Norcross, GA **Circle 135**

Color Logic Analyzer

An enhanced version of the 1240 Logic Analyzer, the new 1241 model adds a liquid crystal color shutter and the vertical expansion of timing diagrams on the display. The colors, yellow, green and red, are used for grouping common elements and highlighting important features. Yellow can be used for highlighting important settings, green for background and standard menu parameters and red for error messages and glitches. The company quotes a 40% time reduction for an experienced user performing a task and a 30% reduction for a user knowledgeable but rusty with the instrument. Price is $8,6000 to $21,000 for 9- to 72-channel systems. **Tektronix**, Beaverton, OR **Circle 128**

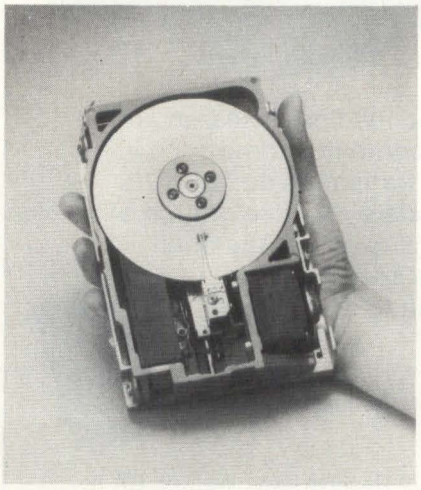
PERIPHERALS

μP-Powered Bell Type Modems



Five new modems have been announced by Universal Data Systems. The 202S/D is a 0-1200 bps half duplex modem for async data transmission or 1200 bps sync data transmission over the PSTN. The 201B is a 2400 bps async/sync modem designed for use over 4-wire private lines and the 201C is a 2400 bps sync modem for use over the PSTN. The 212A is a 300/1200 bps modem with automatic answer and the 212A/D is a 300/1200 bps modem with auto-dial and auto log-on. Prices are $495, $685, $685, $495 and $545, respectively. **Universal Data Systems**, Huntsville, AL **Circle 153**

20-Mbyte 3½" Winchester Drive



The Model TM362 3½" Winchester disk drive employs a unique closed-loop positioning system and plated media to achieve a formatted capacity of 20 Mbytes and an average access time of 80 msec. The half-height TM362 measures 1⅝" high, 4" wide, 5⅜" long. The firm is also introducing the Model TM262 3½" drive in a 5¼" half-height form factor. The same height as the TM362, the TM262 is 5¾" wide and 8" deep. The drives use a pseudo-closed-loop-positioning system; servo positioning data is embedded in the microscopic index wedge located on each data track. The drive checks its location during each revolution and corrects its position if needed. Price for the TM362 is $300. **Tandon**, Chatsworth, CA **Circle 150**

IBM 3274 Fiber Optic Coax Multiplexer

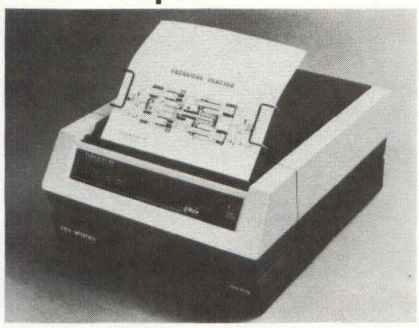
Supporting multidrop configurations, the FMX-32 fiber optic multiplexer can be set up in a point-to-point configuration or in a hybrid filter and coaxial configuration. The FMX-32 completely eliminates as many as 32 coaxial cables and can include from one to four 8-channel cards for 8-, 16-, 24- or 32-channel capacity. It can send signals as far as 15,000', compared to the 5,000' maximum of coaxial cables. Prices are $1,930 (8-channel) and $3,860 (32-channel). **FiberCom**, Roanoke, VA **Circle 142**

Video Camera For Machine Vision

Designed to work with machine vision systems, this video camera allows 360° image rotation, 6× electronic zoom, aspect-ratio changes, translation and software control of camera settings. The Rotazoom camera has a square aspect ratio to prevent images from geometrically distorting during rotation. All commands are entered during a normal 16 msec frame. While the camera is capable of being set to 8× zoom, the noise tends to degrade magnifications greater than 6×. The rotational resolution is 256 steps per quadrant (about .35°). **Key Image Systems**, Chatsworth, CA **Circle 146**

PERIPHERALS

Video Copier



The Superplot 80T video copier prints an average CRT screen image in less than 15 secs. It is a monochromatic fixed-head thermal printer/plotter teamed with a page level video interface. Sync data sampling of standard RS-170 composite video data provides alphanumeric and graphic screen reproductions from most video monitors and terminals. With a screen freeze time of 2 secs, the 80T can operate as a 75 lps or 500 cps near-letter quality printer/plotter interfaced to a CPU through available parallel or serial interfaces. Price is $3,450. **Graphic Instruments**, East Greenwich, RI
Circle 154

Ion Print Engine

An extension of the firm's proprietary ion printing technique, first demonstrated in the earlier 2460 print engine, this 90 page/minute continuous feed print engine (2490) is designed for electronic print environments requiring up to 2M pages/month. The 2490 prints at rates of 88 feet/minute with a resolution of 240 dpi. Power consumption of the engine is 230W, and it does not require a specially conditioned environment. Contained in a 20″ cubic system, the 2490 accepts raster video input on a byte-wide interface at an average rate of 1.125 Mbytes/sec. It uses TTL logic signals with a basic handshaking protocol. **Delphax**, Westwood, MA **Circle 177**

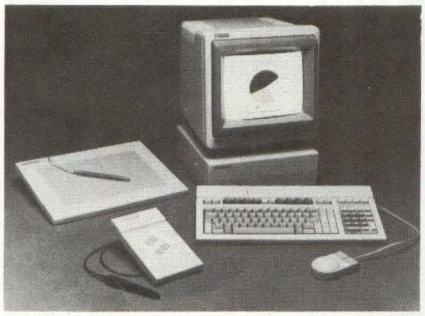
130-Mbyte Disk Subsystem

The Super Quicstor-Plus subsystem functions in multiuser environments, addressing mass storage, reliable backup and fast operating speeds. It includes a 130-Mbyte hard disk drive and has a data access time of 18 msec and a data transfer rate of 10 Mbits/sec. Super Quicstor-Plus integrates five IBM PC-compatible expansion slots, a hard disk and a ¼″ cartridge tape backup unit with a formatted capacity of 69 Mbytes. It may also function as a file-server on a variety of LANs including the IBM PC Network, 3COM EtherSeries, Corvus systems' Omninet and Proteon's ProNET. Price is $10,595. **Alloy Computer Products**, Framingham, MA **Circle 149**

Letter Quality Printers

Four new letter quality data processing printers have been introduced by Genicom. They feature Diablo 630 emulation, IBM PC graphics and ANSI X3.64 protocol support, both serial and parallel interfaces and more. The 3320/Quiet provides letter quality at 180 cps with graphics resolution of 72 or 144 dpi, 288 dpi optional. The 3310 features a 9-wire print head capable of 300 cps in data processing mode, 90 cps in lq mode and graphics resolution of 72, 144 or 288 dpi. The 3310/Color adds printing in up to seven colors to the 3310's features. The fourth new printer, the 3410, has a parallel 18-wire print head for print speeds of up to 40 cps in data processing mode and 100 cps in lq mode. **Genicom**, Waynesboro, VA **Circle 156**

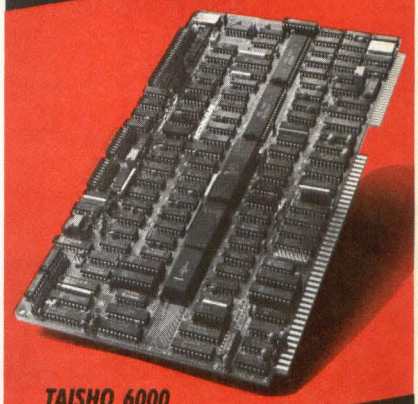
Graphics Terminal For HP 3000/1000/9000



Compatible with the HP 2623A graphics terminal, the HP 2923A graphics terminal works with the HP 3000 business computer and the HP 1000 and HP 9000 scientific/engineering minicomputers. It also works with the VAX and can emulate a Tektronix graphics terminal. The HP 2393A's interface options include RS-232-C/HP 422 system port, video interface, HP-HIL and optional peripherals port; up to four different input devices can be daisy-chained directly to the keyboard. The 2393A provides bit-mapped vector graphics in a dual-mode resolution of 512 × 390 pixels or 640 × 400 pixels. It also provides full alphanumeric capabilities and up to 12 pages of text can be stored in display memory. Price is $1,995. **Hewlett-Packard**, Palo Alto, CA **Circle 145**

MULTIBUS* DISK and TAPE CONTROLLER for

- ST506/412 HARD DISK
- 5¼″ or 8″ FLOPPY
- FLOPPYTAPE



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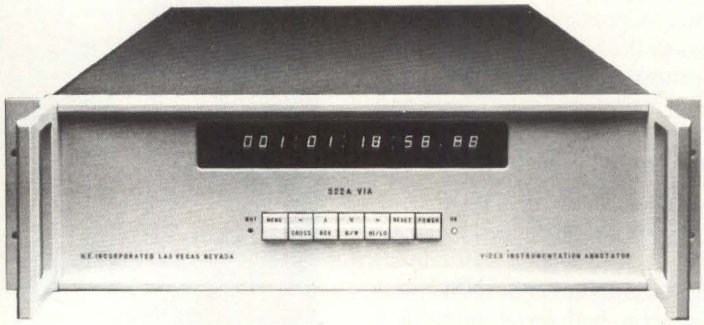

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NEW PRODUCTS

COMPONENTS

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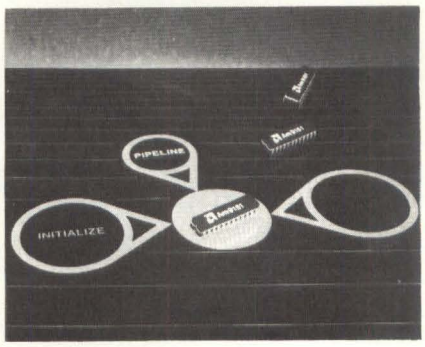


With pipelining, initialization and diagnostic capabilities, this SRAM with on-chip registers uses N-channel MOS processing techniques to achieve a 40 nsec cycle time. The Am9151's diagnostic capability is provided by the Serial Shadow Register (SSR) that can detect system- or board-level malfunctions, as well as load microcode serially into the Am9151's memory array. Available in a 24-pin ceramic DIP, the Am9151 is priced at $25 (40 nsec, commercial) and $45 (50 nsec, military) both in 100s. **AMD**, Sunnyvale, CA **Circle 178**

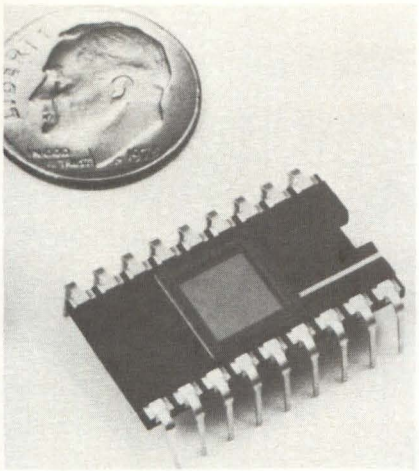
8-Bit Bit-Slice Processor

Using the Impact technology, these 8-bit bipolar bit-slice devices, the SN74AS888-1 and SN74AS888, offer a 1200 mW typical power dissipation. They perform 14 arithmetic and logic functions and feature add and subtract immediate instructions, signed magnitude to/from twos complement conversion, CRC polynomial code accumulation, signed and unsigned divides with overflow detection, signed, mixed and unsigned multiplies, BCD conversion in a single clock cycle and bit, byte and word instructions. Both devices operate in -55°C to 125°C ranges. Pricing in 100s is $155: SN74AS888-1GB and $55: SN74AS888GB. **Texas Instruments**, Dallas, TX **Circle 181**

40 nsec 64K × 1 SRAM

This 64K × 1 SRAM achieves a 40 nsec access time. The μPD4361 is implemented in mixed MOS technology; the memory cells are designed in MOS and the output drivers are CMOS for lower power and TTL compatibility. Speeds available are 40, 45 and 55 nsec in a LCC and 45, 55 and 70 nsec in a DIP. Price in 100s ranges from $46 to $93. **NEC**, Mountain View, CA **Circle 187**

512 × 403 CCD



Intended for producing standard interlaced 525-line video with precision image geometry, the SID504 CCD contains 512 vertical × 403 horizontal pixels (206,336 picture elements). It has a spectral response that includes both visible wavelengths between 400 and 700 nm, and wavelengths extending into the near-infrared spectrum to about 1100 nm. **RCA**, Lancaster, PA **Circle 191**

CMOS Z80 Family

Zilog's Z80 family is now available in CMOS. The CMOS version of the Z80 μP, the Z84C00, will be used in instrumentation and medical production where low power consumption and noise immunity is required. The Z84C30 clock timer controller will be targeted for handheld industrial instrument applications with the same environmental requirements. The Z84C20 PIO is also geared for designs where noise interference could hamper the effectiveness of products. Prices are $4.55 (Z84C00) and $4.00 (Z84C20 and Z84C30). **Zilog**, Campbell, CA **Circle 183**

15 nsec 256K PROM

Complementing the firm's 20B family of 15 nsec programmable array logic devices, the PL87X288 PROM has five inputs, eight outputs, a fixed AND array generating all 32 product terms and a programmable OR array. Typical power dissipation is 550 mW. Operating over the 0°C to 70°C range, the PROM is also available in a 20 nsec military version. Housed in plastic DIPs, the device costs around $3 in 100-up quantities. **National Semiconductor**, Santa Clara, CA **Circle 185**

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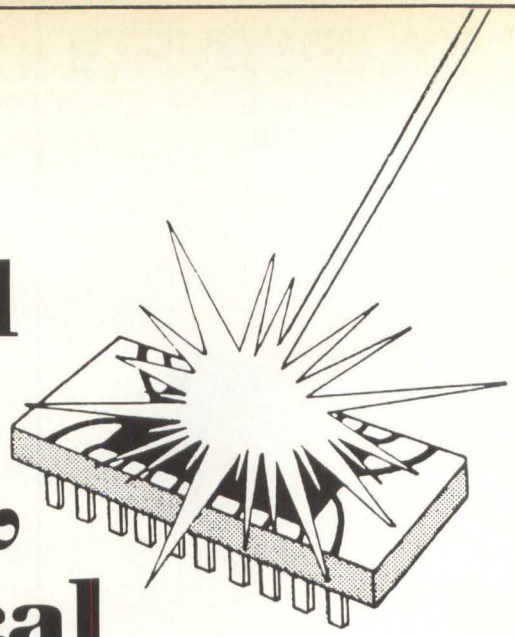

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256K Static-Column CMOS DRAM

Using advanced 2-micron CMOS processing, this static-column DRAM is available in row access times of 100 nsec, 120 nsec and 150 nsec, static column access times of 45 and 55 nsec and cycle times of 180 nsec and 210 nsec. The HM51258P typically consumes 250 mW in active mode; in standby mode, power consumption is reduced to 10 mW. Refresh of 256 cycles takes 4 msec. Packaged in a 16-pin, JEDEC-standard DIP, the device is priced at $35. **Hitachi**, San Jose, CA **Circle 189**

CMOS Color Graphic CRT Controller

This graphic CRT controller allows a complete display system to be built with five to nine additional circuits: one decoder and four to eight 64K DRAMs. The RF5C16 model is designed for use in NTSC video systems, and the RF5C17 is for use with PAL-SECAM video. Each chip consumes 300 mW and includes refresh circuitry to support DRAM storage. Prices begin at $28.50 in 100s. **Panatech Semiconductor**, Santa Clara, CA **Circle 188**

Error Detection/ Correction Chip

Pin and function compatible with the industry standard AM2960C, this Error Detection and Correction (EDC) unit (N2960) corrects all single-bit errors in high-speed μP-based systems. In operation, the N2960 generates check bits on an 8- or 16-bit field. Worst case for data into error detect is 32 nsec and 65 nsec worst case for data into corrected data out. **Signetics**, Sunnyvale, CA **Circle 192**

CMOS μP Family

This family of CMOS μP and peripheral devices operate at 0°C to +70°C. It consists of 18 CMOS μPs with operating frequencies to 3 MHz and supporting devices, including peripheral interface adapters, RAM-I/O timers, and async communications ICs. Prices are $4: G65SC02P-1 μP, $3.05: G65SC21P-1 peripheral interface adapter, $4.10: G65SC22P-1 versatile interface adapter, $4.75: G65SC32P-1 RAM-I/O timer and $4.30: G65SC51P-1 async communications interface adapter. **GTE Microcircuits**, Tempe, AZ **Circle 184**

Video D/A Converters

Available with or without on-board look-up table memory, the AH8404 triple (RGB) video D/A converters provide color display systems with a TTL-compatible, composite video subsystem in a 24-pin DIP. A color-mapped video version is designed for color graphic systems where space is plenty. Dissipating 800 mW max, it features a triple video D/A converter and 32-word color look-up table memory supporting a pixel rate of 20 MHz. The D/A converter-only version for systems with their own look-up table supports a 25 MHz pixel rate with max power dissipation of 600 mW. Pricing ranges from $52-$80 in 100s. **Analogic**, Peabody, MA **Circle 186**

Circle 40

BOARDS

PC/AT-Compatible Image Processing Board

This single board image processing subsystem, the FG-100-AT, can digitize analog video from standard RS-170 video sources, processing the imagery in real time and displaying the stored image in monochrome or pseudocolor. Containing 12 bit-planes of frame memory, with a resolution of 512 × 512 pixels, the FG-100-AT has an 8-bit A/D converter for digitization to 256 levels of gray, a dual-stage phase-locked loop for synchronizing with video tape recorders, zooming by 2, 4 or 8 and single pixel pan and scroll. **Imaging Technology**, Woburn, MA **Circle 197**

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Circle 59

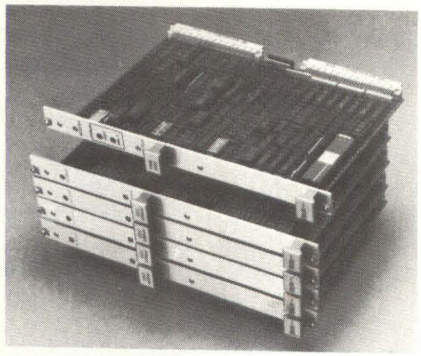
80M BPS LAN

Connecting up to 240 Unibus or Multibus workstations using any combination of twinax or fiber optic cabling, the ProNET-80 token-passing star-shaped ring network transmits data at 80M bps. It is software compatible with the firm's original 10M bps network, the ProNET-10. The network will correct parity errors and determine the exact location by inserting a format error message in the ProNET host interface. Price is $8,000 per host interface. **Proteon**, Natick, MA **Circle 198**

Monochrome Adapter Board For IBM PC

A monochrome display adapter with full IBM software compatibility and an optional printer port, the Mini-Mono Card measures 4″ × 6″ and will fit into a short slot in the PC/XT, or a full size slot in the PC or AT. The display area is 80 characters × 25 rows. Using 4 Kbytes of display memory—2 Kbytes for characters and 2 Kbytes for attributes—the Mini Mono Card can perform DMA operations directly to or from the display memory. Price is $225, with printer port, $250. **Emulex**, Costa Mesa, CA **Circle 165**

VMEbus Memory Sub-System With ED/C



Comprised of a VME-ECC memory controller card and one, two or four VME-ECC memory array cards, the MK75703 VMEbus board set contains 2 Mbytes of memory (on each card) using 64K RAMs, expandable to 8 Mbytes using 256K RAMs. Performing error detection and correction and containing a checkbit register in the diagnostic mode of operation, the VME-ECC controller card is also available in half-populated versions so that subsystem memory can be configured in 1, 2, 4, 8, 16 or 32 Mbytes in up to five VMEbus slots. Price is $18,360. **Mostek**, Carrollton, TX **Circle 199**

SOFTWARE

Software Interface Packages

Linking Sperry's Series 1100 36-bit, general-purpose mainframes with Floating Point Systems' FPS-164 Scientific Computer, the Multiuser APEX Interface Package and the System Job Executive Interface Package for single-user systems were developed and are supported jointly by the two firms. Each package provides the interface between one or more FPS-164 computers and a Sperry 1100/7X, 1100/8X or 1100/9X environment and supports the execution of scientific and engineering application programs on the PFS-164. The package lets up to eight users of a Series 1100 system gain access to one or more FPS-164 computer. It includes an optimizing Fortran-77 compiler for the FPS-164, which generates code that takes advantage of the PFS-164's parallel, pipelined architecture. Prices are $71,000 (Multiuser APEX) and $31,000 (System Job Executive). **Floating Point Systems**, Beaverton, OR **Circle 175. Sperry**, Blue Bell, PA **Circle 176**

Tektronix 4107 Emulation Package For MS-DOS PCs

Allowing a PC to communicate with a range of host-based graphics software by performing graphics functions currently available on dedicated terminals, the TGRAG-07 software package is a Tektronix 4107 emulation software package for MS-DOS-based PCs. On the IBM PC, TGRAF-07 supports boards that start at the 640 × 480 resolution of the 4107 and range up to 1024 × 1024 resolution. Supported boards include the IBM Professional Graphics Adapter, the Verticom M-16, the BNW Precision Graphics Adapter and the TAT Galaxy Series. **Grafpoint**, San Jose, CA **Circle 168**

XENIX 286 Versions Of High-Level Languages

Microsoft has released XENIX versions of four high-level languages: Fortran, Pascal, COBOL and Basic. Source-level compatibility makes it possible to take programs written in a previous MS-DOS version of a language and transport them to the XENIX environment with little or no modification. Users can link directly into the XENIX system libraries, so programs can take advantage of the operating systems multitasking and multiuser capabilities such as shell support, pipes and record and file locking. Retail prices are $350 (Basic), $995 (COBOL) and $495 (Pascal and Fortran). **Microsoft**, Bellevue, WA **Circle 171**

Library Of Software Applications

Supplementary to the company's Third Party Software Program offered through individual suppliers, this library of software applications has been developed for the firm's 32-bit supercomputer users. Twelve titles are housed in the library, with more expected in the near future. Available titles include Linpak: a collection of subroutines analyzing and solving various systems of simultaneous linear algebraic equations; Kermit: a protocol for transferring files between computers; and XLISP: an experimental programming language that combines features of LISP with an object-oriented extension. There is a five dollar handling charge, $30 for non-MUS (Masscomp User Society) members. **Masscomp**, Westford, MA **Circle 170**

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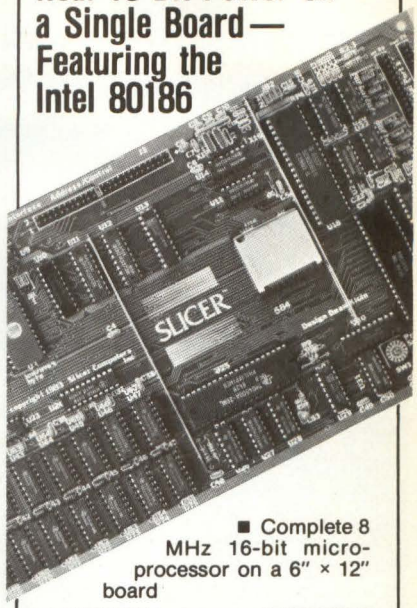

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NEW PRODUCTS

Real-Time Cross Development Tools

Allowing generations of real-time multitasking software for embedded μP systems, the Real-Time C (RTC) package consists of a C language compiler designed for the multitasking environment that executes under VAX/UNIX and VAX/VMS and targets the 68000 and 8086 μPs. Also included is a utility package that consists of a cross-assembler, linker, cross-reference facility and librarian. The C compiler and the utilities are fully integrated with the firm's real-time operating systems component family, which includes the VRTX real-time executive, IOX I/O executive, FMX file-management executive and TRACER multitasking debugger. RTC employs constant expression folding, operator strength reduction, redundant jump elimination and code hoisting. The compiler also supports PROM/RAM separation; separate modules are generated for the code and initialized annd uninitialized variables. Price is $9,000. **Hunter & Ready**, Palo Alto, CA **Circle 173**

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