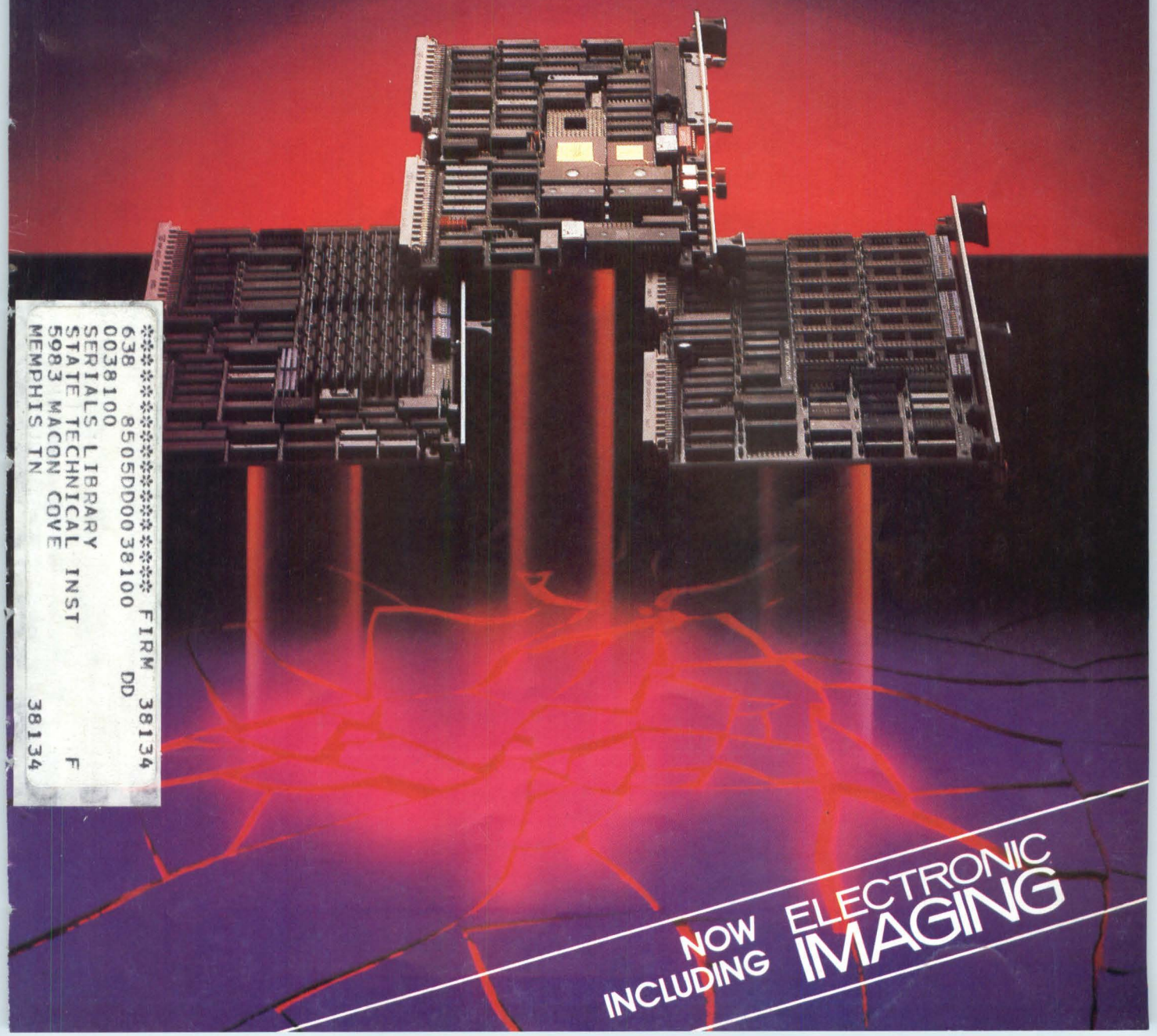
A MORGAN-GRAMPIAN PUBLICATION

DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

MAY 1985

- VME BUS CHALLENGES MULTIBUS I AND MULTIBUS II
- TEST DRIVING A SILICON COMPILER
- PRINTED CIRCUIT BOARD DESIGN
- MICROSTORAGE ■ GRAPHICS ARCHITECTURE



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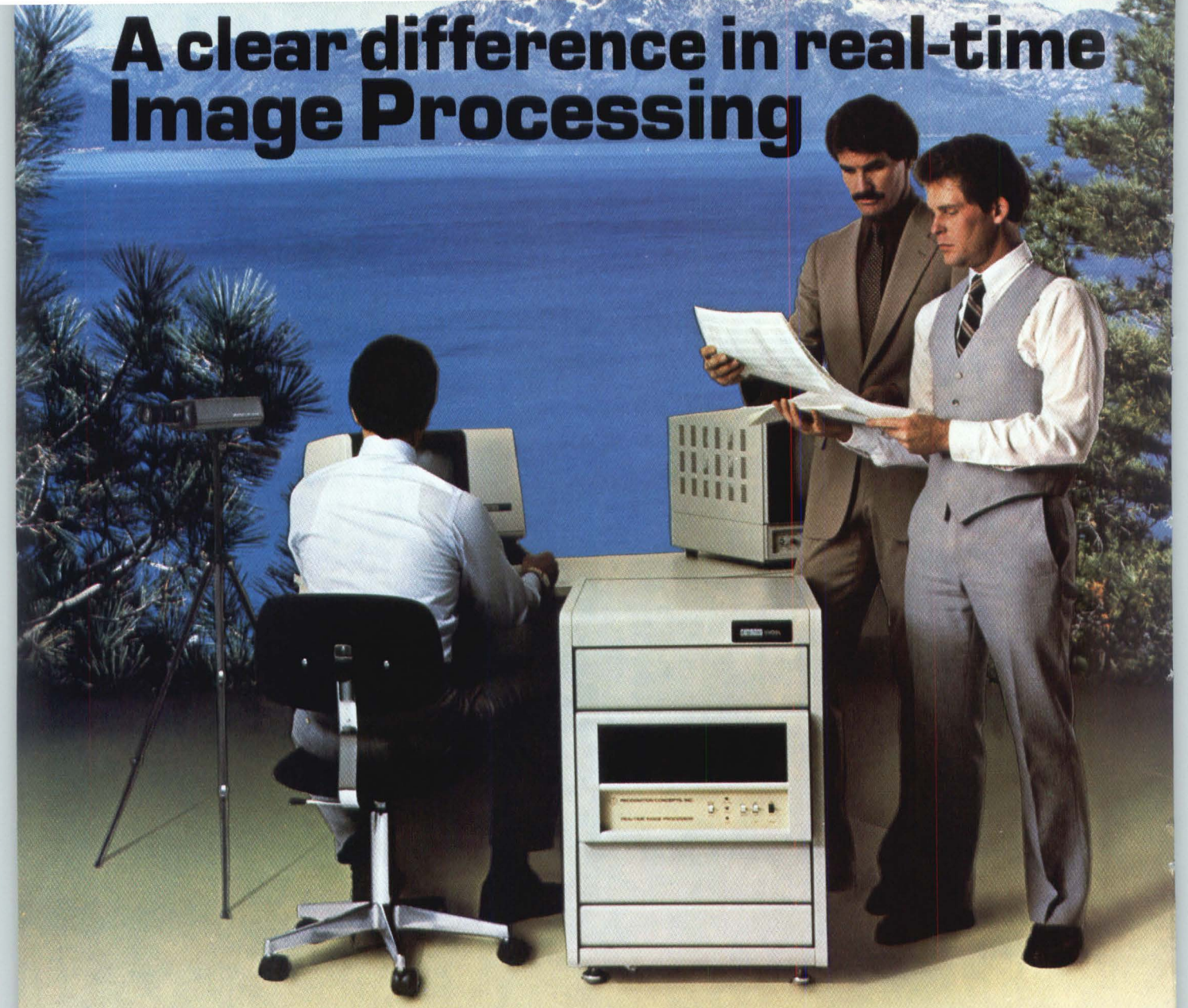

Whether you need a turn-key system or a peripheral to connect to your computer, the **TRAPIX™ 5500** Image Processors have been carefully designed to meet your specific needs. They're compact and rugged enough to withstand most hostile environments, yet they carry a commercial price tag and are backed by a full year factory warranty — the best in the industry. They don't require special power or air conditioning and they use standard programming languages and operating systems — features designed to make them easy to own and use.

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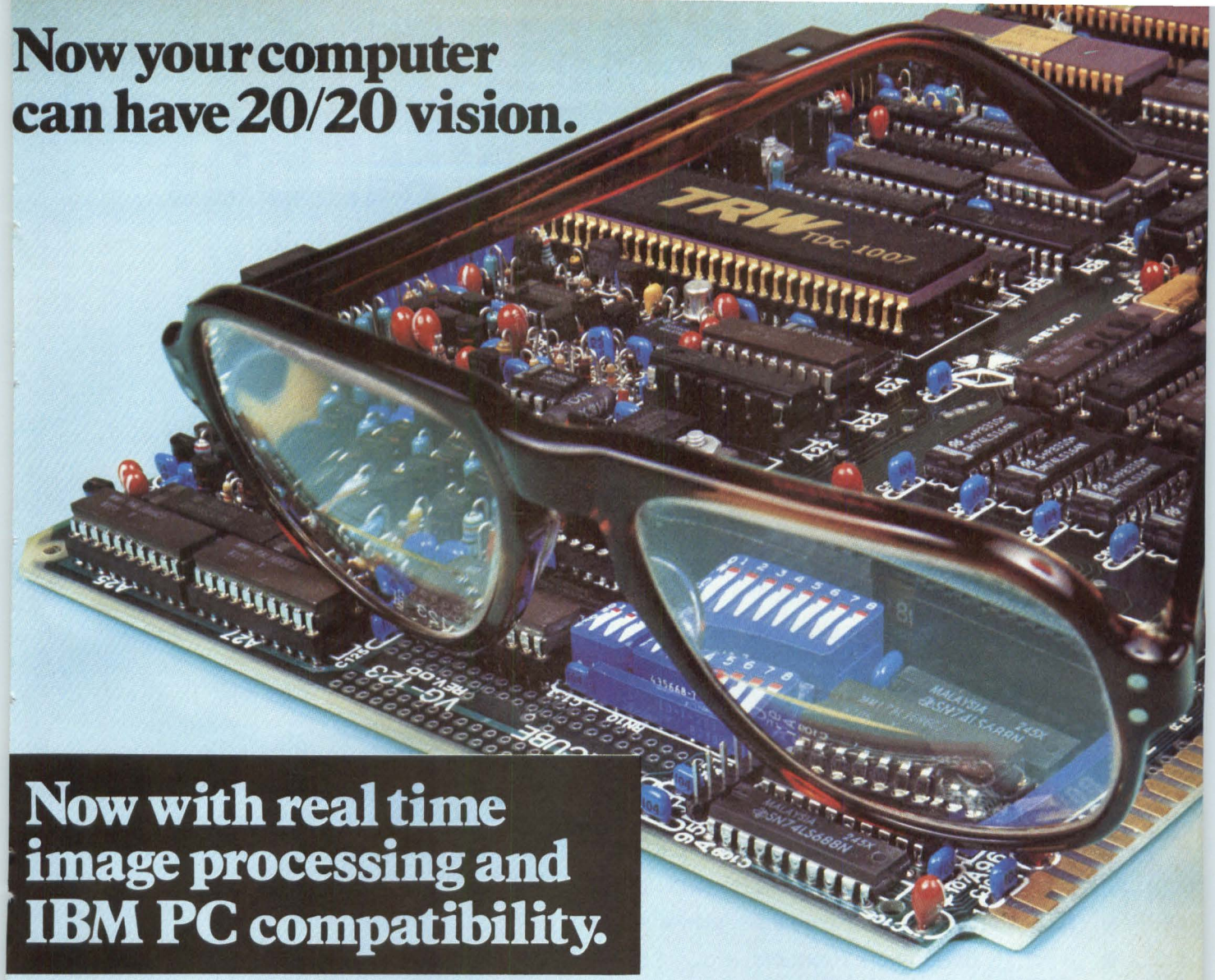
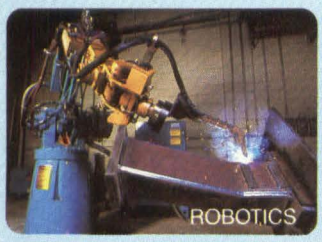
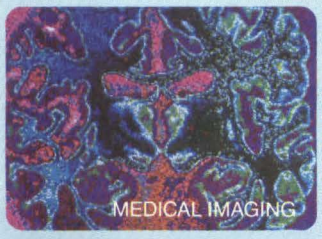


Now with real time image processing and IBM PC compatibility.





Datacube continues to be the single source leader in image processing and graphics for your Multibus, Q-Bus, and now IBM PC's. Solutions are available from single boards to fully integrated systems.

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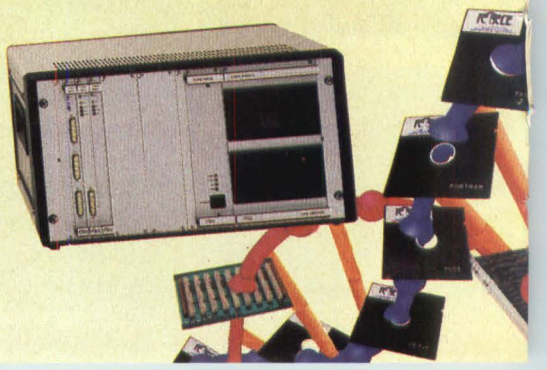

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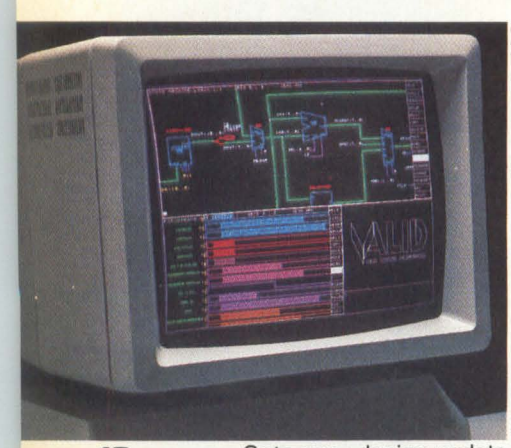

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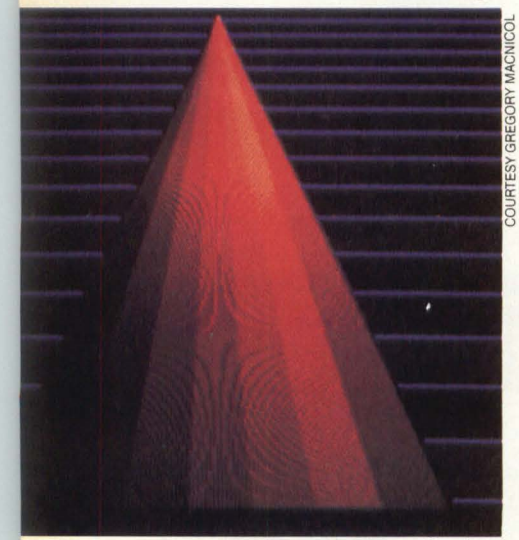

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TECHNOLOGY TRENDS

ON THE COVER

Currently the only widely supported 32-bit bus structure, the VME bus, is being considered by many systems integrators as a logical 32-bit upgrade solution to their existing Multibus designs. The front cover this month depicts three new products from Motorola Microsystems including a 68020-based CPU board. Photo courtesy Motorola Microsystems, Inc.

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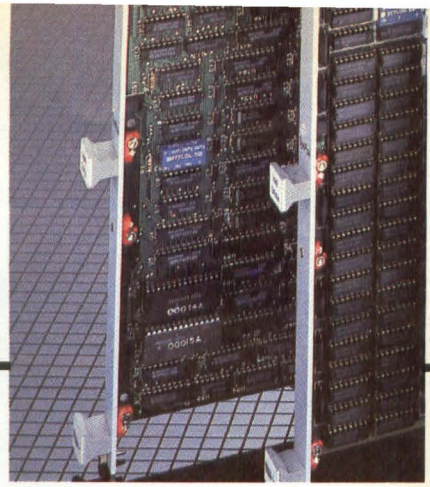

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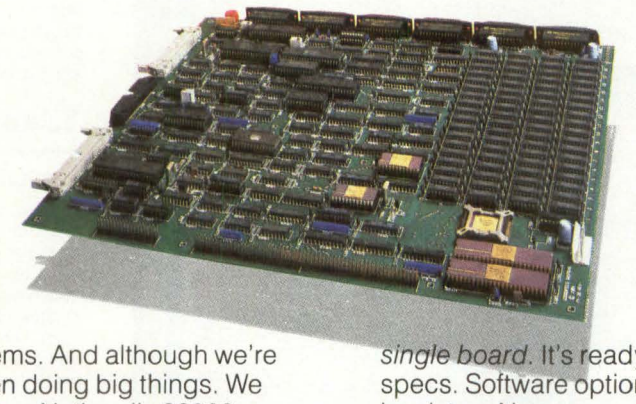

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From offices to factories across the country—hour after hour, day after day—Genicom 3000 printers have been proving their quality and reliability under even the toughest conditions for years.

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EDITOR'S COMMENT

DIGITAL reDESIGN

As promised last month, this is our first issue incorporating *Electronic Imaging* into *Digital Design*. The merger effects a number of important changes in this magazine.

To accommodate additional graphics and imaging articles, along with our usual subjects, the feature section of *Digital Design* has been divided into four subsections: Electronic Imaging, Systems Architecture, Semiconductor Technology and Design Technology. The systems, semiconductor and design sections are what we have been doing all along; imaging is new.

Although graphics, array processing and much of the other coverage in *Electronic Imaging* fall within our normal purview, articles with a purely imaging cast are new to *Digital Design*. To help us keep it all sorted out, Andrew Wilson, Executive Editor of *Electronic Imaging*, will be responsible for the expanded graphics and imaging coverage.

Systems architecture covers our traditional computer-related subjects. That includes computer systems, peripherals, buses, communications and expanded software coverage. Technical Editor Brita Meng will be in charge of the section.

Because semiconductor advances make most systems progress possible, *Digital Design* has always provided IC coverage. Now we are formalizing it with a feature section devoted exclusively to semiconductor technology. Our Executive Editor, David Wilson, is responsible for this section of the magazine.

In the past, *Digital Design* has offered a great deal of design coverage such as PC board and gate array design, workstations and development systems. Because of the importance of these topics to design engineers, a section of the magazine is now devoted to design technology. Senior Technical Editor Ron Collett is responsible for the section.

Each of the feature sections will have at least one article per issue and often more. Our goal is to provide balanced editorial every issue. To ensure that balance, the Technology Editors in charge of each of the four sections will continually track their segments of the industry, keeping up to date on the latest technology.

All of the Technology Editors have degrees in either Electrical Engineering or Semiconductor Physics. But despite their broad knowledge of the industry, they know that they can't do it all themselves. So they will be looking for help in the form of good contributed articles.

We've made a few other changes as well. Last month you saw the replacement of Departments with Technology Trends and the addition of New Product Focus reports. Now the whole news section of the magazine has been redesigned to pick up many of the visual elements of *Electronic Imaging*.

For example, Update has been replaced with Hotline (as in *Electronic Imaging*) to underline the immediacy of news in that section. Technology Trends has picked up the graphics style of *Electronic Imaging*'s news section but otherwise remains the same as established last month. Staying on top of the news is Senior Editor Julie Pingry's responsibility, although much of the input will come from the Technology Editors.

All of these changes represent a commitment to our readers. We are trying to provide the best written, most balanced design editorial package in the industry. Let us know how you feel about it.

—John Bond, Editor in Chief

An Array Processor this fast and flexible can't sell for only $4100.

Or can it?

Marinco makes it possible!

The imaging requirements of a geophysical research project at sea demanded intense mathematical calculations.

An array processor was the answer.

But space aboard the ship's computer was limited. Only a single Multibus slot remained.*

Marinco engineers, driven by necessity, pushed beyond the horizons of conventional array processor design.

A Single Board

They discovered how to shrink circuits to a single board — and to do so without sacrificing performance.

In fact, they enhanced it. Keeping signals within a single board actually made significant speed gains. Then they added other performance enrichments such as memory mapping and an auxiliary port for direct high speed I/O.

Easy to Program

Perhaps as important, the board is easy to program, even for someone with only high-level language experience. Standard routines may be adapted. Or new ones created. Marinco's assembler automatically generates the microcode and tracks the 48-bit control word.

Imaging Productivity

The speed and flexibility of the APB-3000 series can dramatically increase your imaging productivity. Use it for coordinate transformation, hidden line removal, vector-to-raster conversion, interpolation, image enhancement and many other operations.

Very Low Price

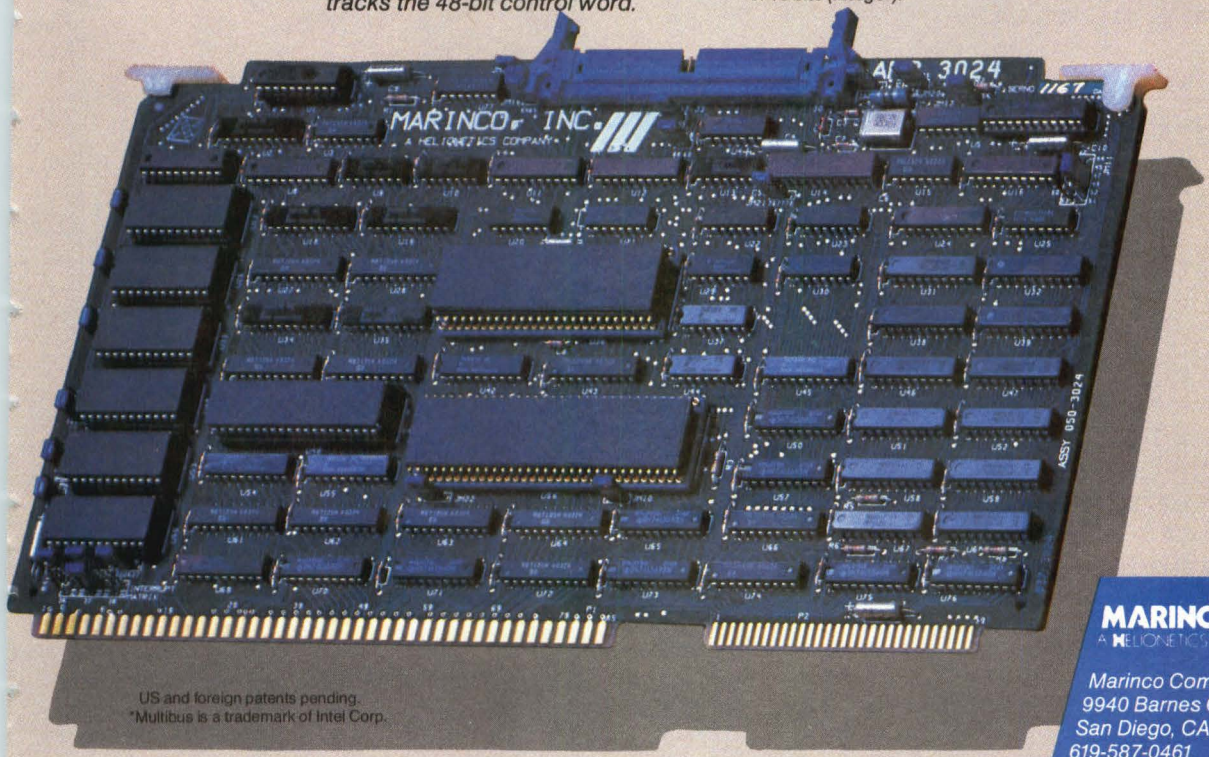
Even with all these advantages, Marinco innovations make it possible to offer the Multibus version for only $4100, quantity one, U.S. price. IBM PC and PC AT versions are also available.

Can an array processor this fast and flexible really sell for such a low price?

Thanks to practical demands and Marinco innovations, it can. Call us toll-free for details.

Specifications

***Program Memory** 2K X 48-bits **Data Memory** 8K words **Data Word** 24 bits long, 8-bit exponent, 16-bit mantissa (floating pt.) or 16 bits (integer).*



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HOTLINE

32-BIT BIT-SLICE ADDED TO STANDARD CELL LIBRARY Wafer Scale Integration is slated to announce the addition of a 15 MHz 32-bit CMOS bit-slice processor to their standard cell library at the Custom Integrated Circuit Conference in Portland, OR this month. In the third quarter, WSI plans to offer the processor as a standalone chip.

EDIF VERSION 1.0 RELEASED The Electronic Design Interchange Format (EDIF) specification is now available to industry. EDIF can be used as a standard interface between engineering, design, test and manufacturing tools. The first meeting of the EDIF Users' Group will be June 27 during the Design Automation Conference in Las Vegas.

STRETCHED DISK FACILITY OPERATIONAL The process development and pilot production plant for 3M's stretched disks has begun operation. Stretched disks promise higher recording capacity than floppy disks, yet use flexible media to circumvent the high cost and fragility of rigid disks. Current 5¼" versions hold about 12 Mbytes and may reach 100 Mbytes.

FAULT-TOLERANT SYSTEM ANNOUNCED BY IBM The System/88 is IBM's first fault-tolerant computer; the system is supplied by Stratus Computer under an agreement for IBM to buy and resell some Stratus products. The System/88 is based on Stratus 32 processors and software.

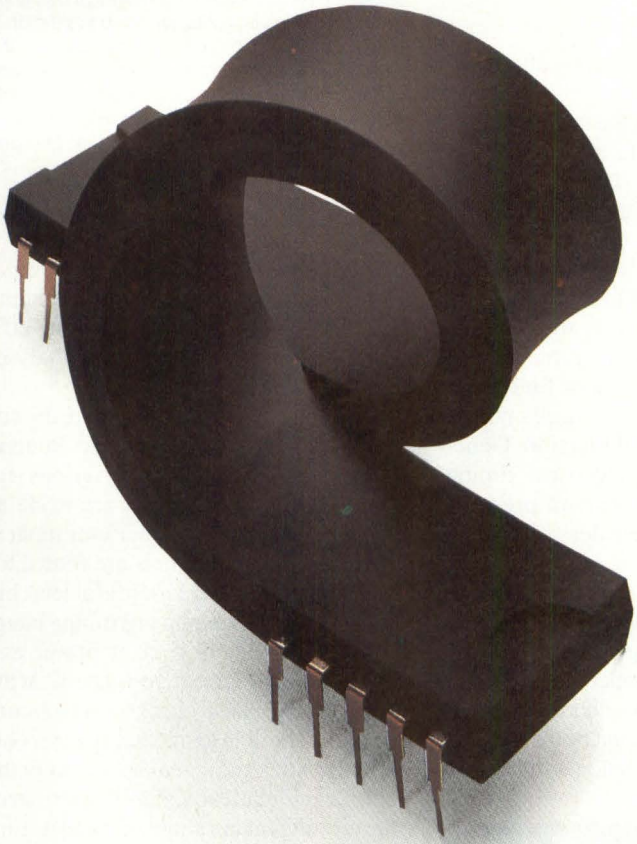
8086/8088 FAMILIES IN CHMOS Intel has announced that their 8086/8088 microcomputers and peripherals will be produced in CHMOS. 80C86 and 80C88 parts will be fully compatible with the existing NMOS versions. Samples of the CHMOS kits are available now, and quantity production is scheduled for fourth quarter.

THREE GaAs VENTURES TAKE-OFF Gallium arsenide manufacturing plants have recently been completed by Honeywell and Ford Microelectronics. Tektronix introduced its first GaAs product in December 1984, but has just formed a subsidiary for GaAs IC marketing and manufacturing called TriQuint Semiconductor. The Honeywell line is expected to be in full production by July, and Ford is shooting for the third quarter.

BOTH 4.2 AND SYSTEM V UNIX PORTED TO APOLLO Apollo Computer Inc. has become the first computer manufacturer to offer both Berkeley 4.2 and System V UNIX on a 32-bit workstation. The twin port, called Domain/IX, allows users to run either 4.2 or System V or both simultaneously on the same node.

MAINFRAME LINES TO VIE FOR IBM MARKET Both National Advanced Systems and Burroughs have introduced new mainframe computer lines. These come in the wake of IBM's Sierra and appear aimed at the same markets.

DON'T LET SPEED SLOW YOU DOWN.



The Mostek BiPort FIFO takes your processor out of the loop.

Until now, buffering two devices with different data rates meant one of two things. Either extra hardware design effort. Or software loops to slow your processor down while it's waiting for a peripheral or a coprocessor to be available.

But now there's a better way. The BiPort™ FIFO from Mostek. You can do away with the need for extra hardware design and software loops, and let your processor operate at its optimal performance level.

Our MK4501 is a 12.5 MHz CMOS device with access times as fast as 65 ns. It can handle asynchronous and simultaneous reads and writes from each respective port. And its 512 x 9 architecture is fully expandable by word width or depth. It even has a retransmit capability.

There's nothing quite like it. Except our MK4511. The MK4511 is similar, but has the added advantage of being a true dual-port RAM that's randomly-accessible for bi-directional applications.

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CAD

Designing ICs With A Silicon Compiler

- 32 inputs organized as 8 groups of 4-bit buses.
- 32 outputs organized as 8 groups of 4-bit buses.
- 3 control lines to select the active input group.
- 3 control lines to select the active output group.
- Clock, power and ground pads.
- During any clock cycle, there is one path active from one input group to one output group.

Figure 1: As opposed to specifying a design in terms of logic elements, silicon compilation is based on the high level architecture of the design. The architectural specification is made up of inputs, outputs, control lines, clock, power and ground. The specification shown illustrates the parameters of *Digital Design*'s digital crosspoint switch.

Digital Design is currently implementing a crosspoint switch onto a gate array. (See *Digital Design*, January, February, March 1985). In addition to the gate array design, we recently implemented the same circuit using a silicon compiler from Silicon Compilers Inc. (SCI) of San Jose, CA.

Genesil System Description

The Genesil silicon compiler system hardware consists of a VAX 11/750, 4 Mbytes of main memory, 450 Mbytes of Winchester disk storage, a 1600 bpi tape drive, four 1024 × 780 color terminals and a mouse. System software includes packages for function synthesis (i.e, the compiler), auto place-and-route, functional simulation, timing analysis and geometric layout.

Integrated circuits are designed with the Genesil silicon compiler using a hierarchical set of objects: chip-set, chip, module and block. Blocks, the most primitive objects, are synthesized according to the needs of the user. Modules are composed of blocks and other modules; chips are modules that have bonding pads, and chip-sets are collections of chips.

The first step in the design process is to select a generic type of function from the function set menu. Next, the block is tailored to the design's requirements by selecting the electrical and functional parameters necessary to implement a specific instance of that function. Genesil automatically flags electrical, timing and clocking violations and prevents blocks violating these rules from being synthesized.

Once the block is defined, Genesil compiles three distinct views: the geometric view (i.e., the actual transistor layout), the timing model and the functional model. These models can be used for immediate verification by the system's timing analysis and functional simulation subsystems. Based on *Digital Design*'s gate array design experience, separating timing from simulation is far more efficient than performing the two analyses concurrently.

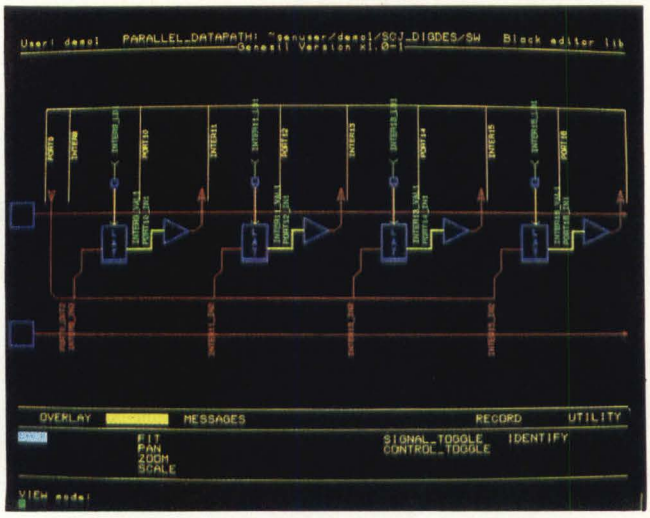

Figure 2: After exploring several architectural possibilities, *Digital Design* and the SCI Applications Engineers concluded that this would be the best implementation of the crosspoint switch. The final design consists of two data paths, an 8-to-1 by 4 mux and a decoder PLA. In this schematic, only the data path is shown.

After verification is complete, the circuit undergoes place-and-route. Routing priorities can be assigned to various signals so that critical paths are made as short as possible. No other user input is required. All bus signals are routed together, providing for a more efficient chip layout and maintaining bus timing integrity. The router also sizes power and clock lines to minimize resistances. At the same time, Genesil checks that interconnects will be able to maintain proper current densities and signal levels. After the chip is automatically placed and routed, the circuit is again simulated and its timing verified using actual wire delays.

Preparation for tooling is the final stage of the silicon compilation design cycle. In readying the chip for fabrication, Genesil produces a magnetic tape containing a layout optimized for a specific foundry fabrication line. At present, Genesil can generate NMOS designs. However, SCI will shortly introduce software that allows designers to build CMOS devices.

Genesil automatically generates a full report of the design that includes detailed manufacturing instructions. In addition, the designer can produce timing data sheets at any level from block to chip-set, document ROM and PLA truth tables, and generate hard copies of block, mod-

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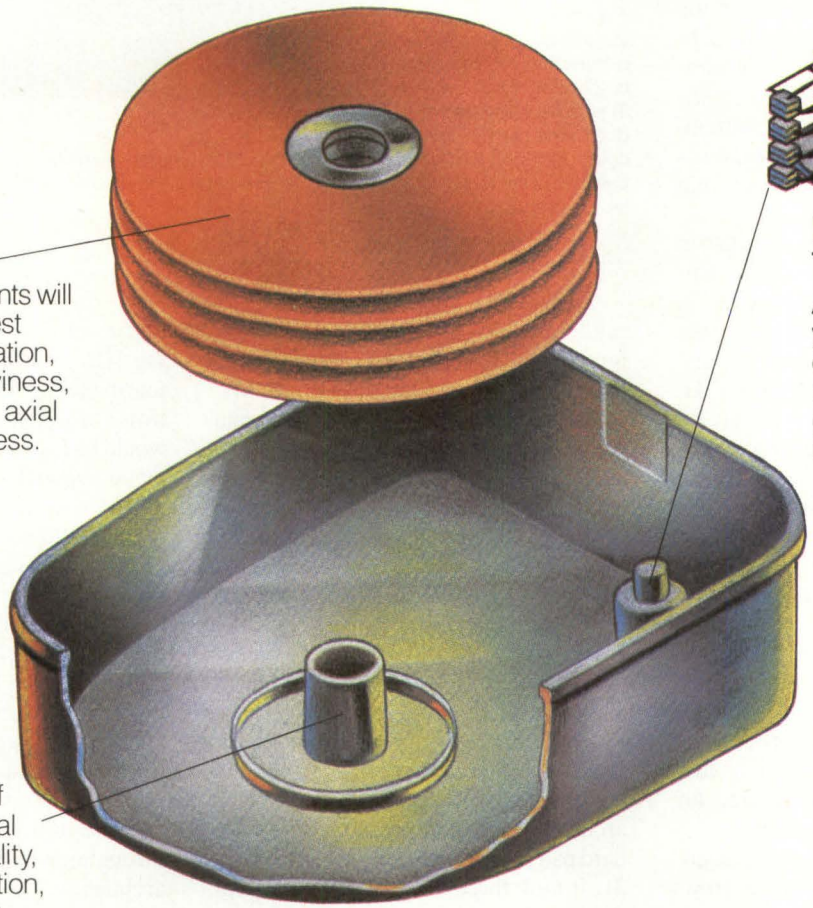

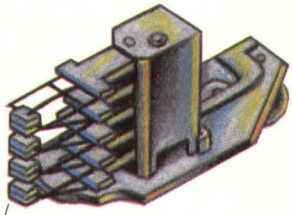

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ule and chip specifications.

Taking Genesil For A Test Drive

Like most engineers given a design task, we were accustomed to working with gates, registers and multiplexers. Despite a clear understanding of how the chip was intended to function, we did not attack the design from a system level approach. Instead we began describing the circuit at a detailed level (i.e., flip-flops and multiplexers). This was the wrong route to follow because the silicon compiler's strength is in removing the designer from specifying logic.

To exploit Genesil's power, we began to formulate the crosspoint switch's architectural, or block level, description. A specification emerged based on the switch's inputs, outputs, control lines, clock, power and ground (**Figure 1**). Once described at this level, several architectural possibilities were proposed. The most efficient solution seemed to be a 4-bit parallel data path structure. The switching function would be accomplished by a general input port, a general output port and a tri-state bus connecting the input and output stages. In addition, a programmable logic array (PLA) would be used to decode the input control lines. The decode mechanism configures the switch for routing signals between the input and output stages. This architecture was entered, compiled and plotted for silicon area in less than one hour.

Since the circuit was not yet simulated, the design was far from complete. However, we did have the die size, performance and propagation delay data necessary to make informed trade-off decisions. Of paramount importance is whether this implementation of the crosspoint switch satisfies cost and performance requirements dictated by the design specification.

In discussing how to reduce die area with several SCI system engineers, an input multiplexing scheme using random logic, (i.e., four 8-to-1 multiplexers) emerged. Genesil's function set includes

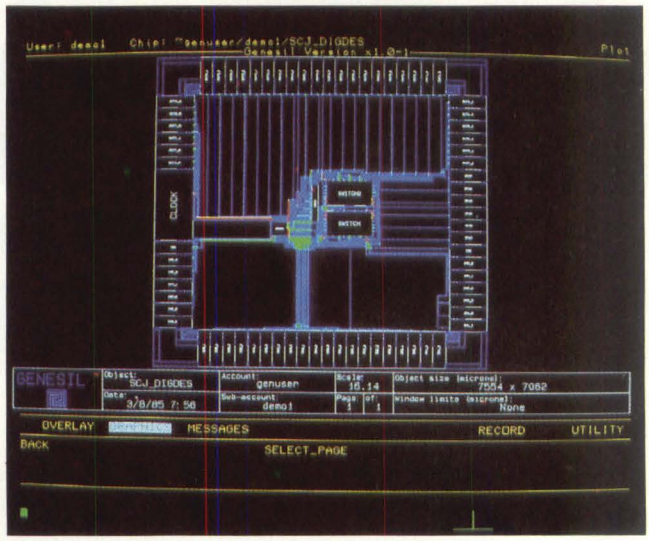

Figure 3: The layout of the crosspoint switch indicates that the die size is 297.3 × 277.9 mils. This rather large area is due to the high I/O pin count; bonding pad sizes are fixed by the chip manufacturer. The active part of the die consumes only 5% of the total silicon area. Implementing the crosspoint switch in two separate chips might be a better solution.

random logic. Other building blocks found in Genesil that were unnecessary for this design include RAMs, ROMs, FIFOs, Stacks, 4- to 32-bit wide data paths, ALUs and Barrel Shifters. Since the input stage uses multiplexers, the remainder of the data path must handle output multiplexing and latching (**Figure 2**). In this instance, splitting the output muxing into two sections provided increased floorplanning flexibility. The resulting crosspoint switch architecture consists of two data paths, an 8-to-1 by 4 (depth) mux and a decoder PLA (**Figure 2**).

After entering the architectural modifications, the chip was again compiled. In conjunction with compilation, the new architecture was combined with a standard pad ring, routed and plotted (**Figure 3**). It took three hours to input the updated architecture and pad ring, to compile and to route. Naturally, before transforming the design to silicon, the switch would undergo more simulation and timing analysis.

The circuit uses 891 transistors. Comparing overall die size to active area (**Figure 3**) shows very inefficient silicon usage. The "core," or active area, is less than 5% of the total chip size. Actual chip size is dictated by the bonding pad size. Implementing the design on two chips instead of one would reduce the number of pads on each chip. Each of the resulting ICs would be approximately one-fourth the size of the present implementation. Moreover, two smaller devices would be less costly than one larger part. Of course, if decreased chip count is the ultimate system goal, the single chip route would be followed.

The primary advantage of silicon compilation is the speed it provides for custom IC design. The entire implementation of this chip, including exploration, took only five hours. In addition, this technology offers the ability to explore alternate architectures rapidly. Analyzing size and power consumption of several different implementations of the same design offers the designer tremendous leverage throughout the design cycle. As a result, architectural creativity is maximized.

At the same time, however, a silicon compiler is a sophisticated tool that demands an experienced system design engineer. In order to utilize the full power of Genesil, the designer must be intimately familiar with system design considerations. Although Genesil can be used by logic designers, an understanding of system design is needed to exploit the silicon compiler's capabilities. A true systems architect would be the best candidate to use Genesil.

—Collett

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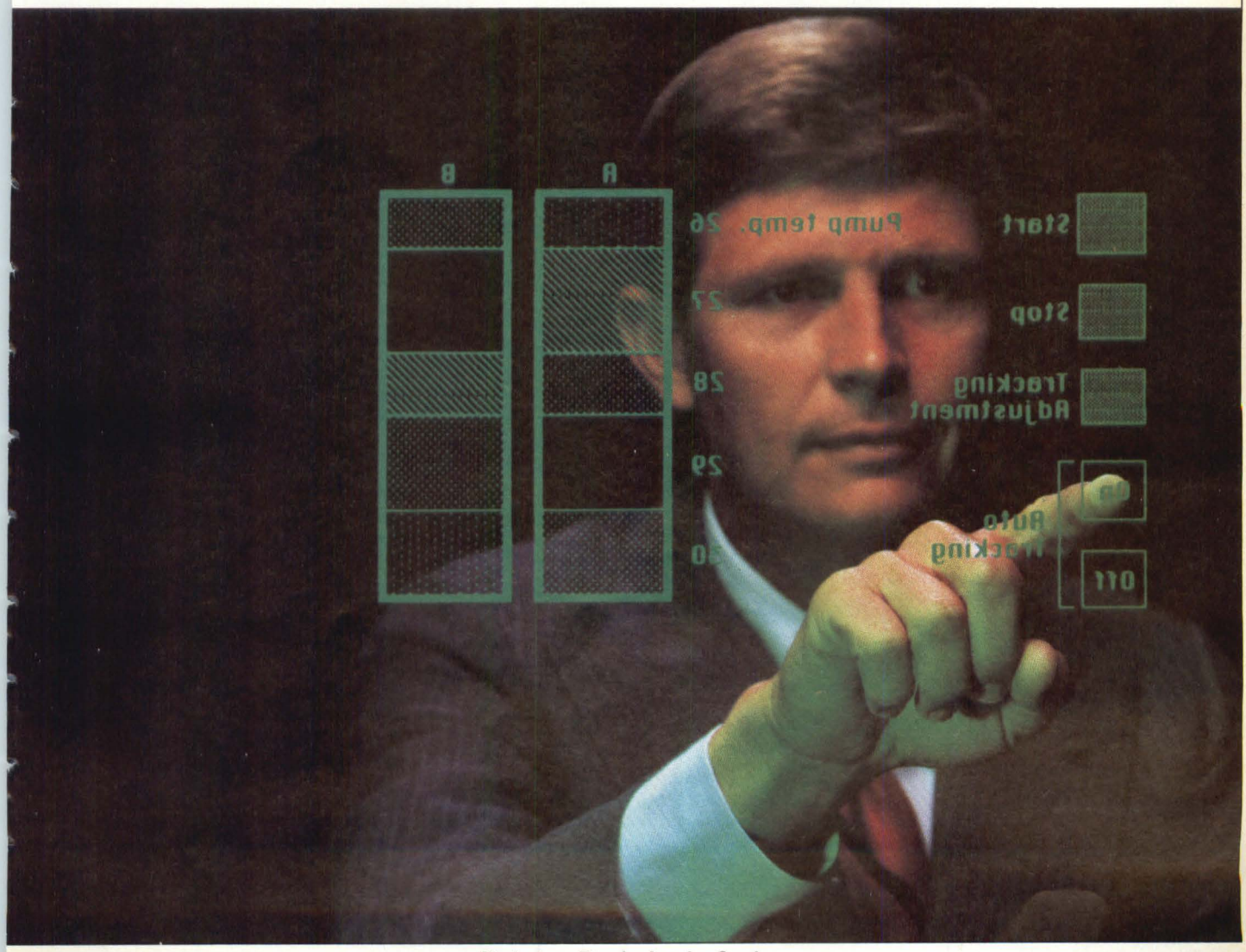

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GATE ARRAY DESIGN UPDATE

Design Verifier Flags Potential Problems

Valid Logic's Scaldsystem workstation is being used to implement a CMOS gate array supplied by LSI Logic. Valid recently unveiled a new model of the Scaldsystem with color display. Valid's primary competitors, Daisy (Mountain View, CA) and Mentor Graphics (Beaverton, OR), also offer color displays.

Digital Design published a three-part series on designing a digital crosspoint switch using a CMOS gate array in January, February and March of this year. The vendors participating in the project are LSI Logic (Milpitas, CA), Valid Logic Systems (San Jose, CA) and Datacube (Peabody, MA). LSI is supplying its cell library; Valid's contribution is the Scaldsystem workstation; and Datacube designed the circuit. Since the project was still underway when Part III went to print, progress reports will be published periodically. This update focuses on the network summary generated by LSI Logic's Design Verifier.

The Design Verifier, highlighted in Part II, runs on Valid's Scaldsystem. Its purpose is twofold: to provide the designer with statistically based interconnect wiring delays for simulation and to generate a network summary. The information compiled in the network summary includes network connectivity, number of gates used, number of bonding pads required, number of I/O pins required and percentage of interconnect wires that can be automatically routed.

After entering the schematic and compiling the logic, the designer invokes the Design Verifier. The most difficult step in using this tool is choosing the right gate array. LSI Logic offers three array families: the LL3000, the LL5000 and the LL7000. The LL5000 Series satisfies our performance requirements, so a particular chip in that family must be selected. Since only a preliminary estimate of the circuit's size is available, picking the proper array is done by trial and error. The crosspoint switch (**Figure 3**) has an estimated gate count of 1400 gates. Among the various arrays in the LL5000 family, the LL5140, a 1404-gate chip and the LL5220, which has 2224 gates, potentially satisfy the circuit's requirements.

Both devices were input to the Design Verifier. Each run executed in less than two minutes; the results are given in **Figures 1** and **2**. As shown, the switch uses 1263 gates. Even more important is wireability measure, which indicates whether a particular chip meets the needs of the design. This percentage is calculated as a function of number of gates used, average pins per net (i.e., average fanout per node) and number of signal nets, excluding outputs.

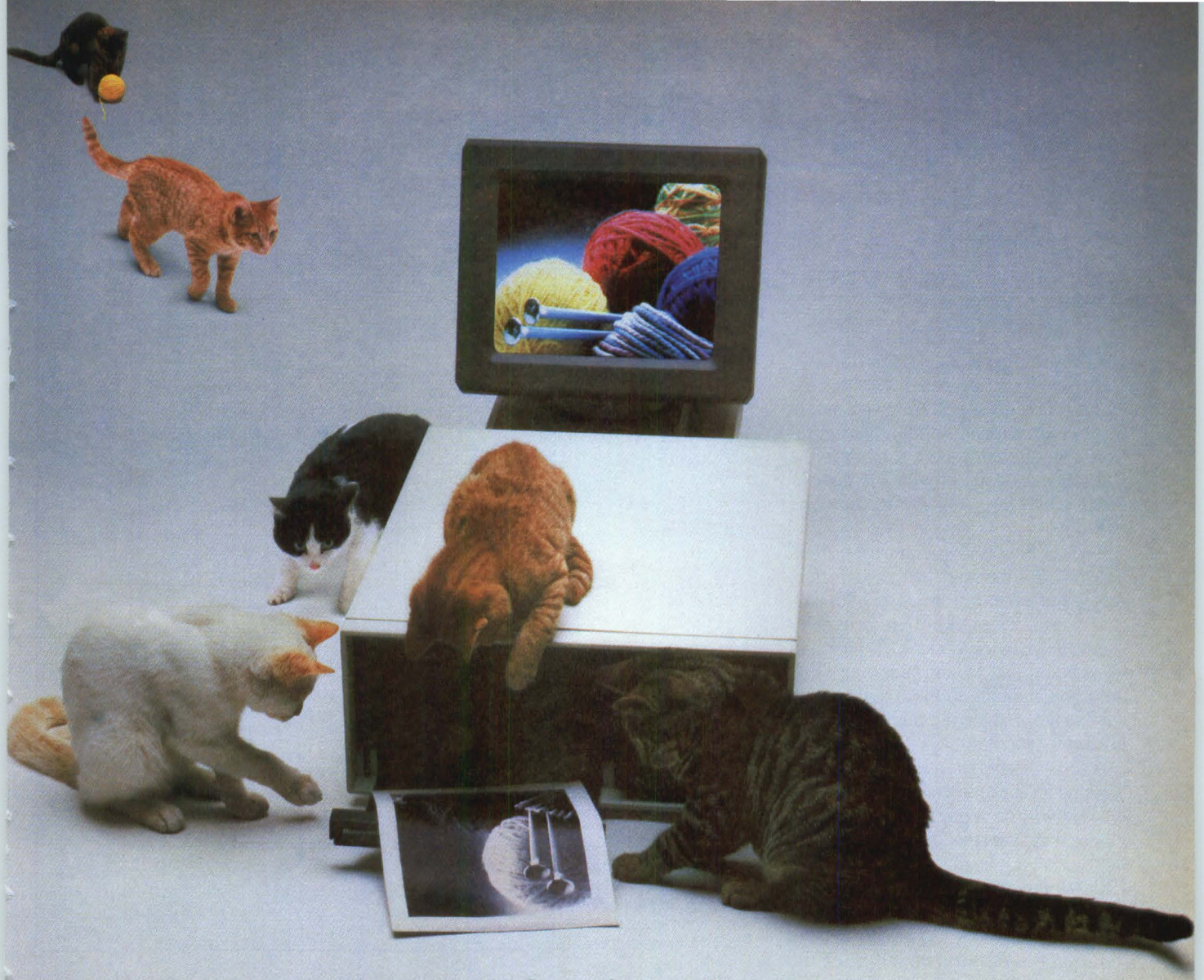
Other information gleaned from the summary includes the number of additional V_{DD} and V_{SS} pads, a comparison of total number of chip pads to number of array pads actually consumed and maximum pins per net. Extra V_{SS} and V_{DD} pads are necessary because certain buffers in the circuit require added current drive capability.

Several problems with our design are flagged by the Design Verifier. The most

LDS DESIGN VERIFIER (VALID) NETWORK SUMMARY

COMP. NAME:	DIGDES	TECHNOLOGY TYPE:	CMOS5K
ARRAY SIZE (FAMILY):	LSI5140	LIBRARY REV.:	2.17 (10/15/84)
Tue Apr 2 16:26:43 1985		VERIFIER REV.:	84.Q4.26
NUMBER OF CELL TYPES:	11	NUMBER OF CELLS USED:	569
NUMBER OF GATES USED:	1263	GATE USAGE (PERCENT):	89.13
ARRAY USAGE (PERCENT):	98.17		
NUMBER OF INPUT PINS:	42	NUMBER OF OUTPUT PINS:	32
NUMBER OF BIDIRECT. PINS:	0	NUMBER OF INTERNAL PADS:	6
NO. OF ADD. V_{DD} PADS:	3	NO. OF ADD. V_{SS} PADS:	1
NO. OF REQ. V_{SS2} PADS:	2	TOTAL NO. OF SIGNAL PINS:	74
***NOTE: TOTALS DO NOT INCLUDE PREASSIGNED POWER PADS AND PINS			
TOTAL ARRAY PADS USED:	116	AVAILABLE CHIP PADS:	92
PACKAGE PINS USED:	78	AVAILABLE PACKAGE PINS:	88
CELL INPUTS TO V_{DD}:	0	CELL INPUTS TO V_{SS}:	0
NUMBER OF SIGNAL NETS:	537	NO. OF UNC. CELL OUTPUTS:	88
AVERAGE PINS/NET:	3.600	MAXIMUM PINS/NET:	65
WIREABILITY MEASURE FOR AUTOMATIC LAYOUT: 88.68%			

Figure 1: The output of LSI Logic's Design Verifier provides a complete summary of the circuit's physical requirements. Of primary importance are wireability, number of chip pads and I/O requirements. In this instance, the LL5140, a 1404-gate chip, was the target array loaded into the Design Verifier.



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critical problem is a need for 116 array pads (i.e., bonding pads). Neither the LL5140 nor the LL5220 have enough bonding pads for this circuit configuration. Only 92 pads are available in the LL5140 and 114 are provided in the LL-5220. Therefore, the design must be modified.

One solution is to use internal buffers drawing less current. LSI Logic offers several different buffers. The high current driving (8 mA) buffers originally used require twice as many I/O pads and more power and ground pads than 4 mA buffers. Changing to these low current buffers will reduce the number of pads needed by about 30.

A second problem is routing the chip. Assume for the moment that the number of pads will be reduced to 86. At first glance it appears that the LL5140 would be the best choice. But using the LL5140, the autorouter can make only 88.68% of the connections. Since the LL5220 is a much larger device, the autorouter can perform 100% of the routing. The issue is whether to manually route the remaining connections of the LL5140 or use the LL5220.

Each solution has a drawback. Manually routing the chip could require many additional man-hours to complete—if 100% routing is possible at all. On the other hand, the LL5220 is more costly, and using it wastes approximately 700 gates. These gates could be utilized if more logic were put onto the chip, but this may also create problems. Additional logic, in this instance, demands more bonding pads. Moreover, adding circuitry not part of the original design specification would require spending more time on the project. The upshot would be an extension of an already delinquent project's design cycle.

The ideal solution would be to use an 1800-gate array, but LSI Logic does not offer such a chip in the LL5000 Series. Problems of this nature are discussed at length in Part I (January 1985).

The next update report will cover which array is to be used and the basis on which that decision is made. Details on the feasibility of manually routing the LL5140 or simply using an LL5220 will be provided. Timing verification and simulation results will also be included. —*Collett*

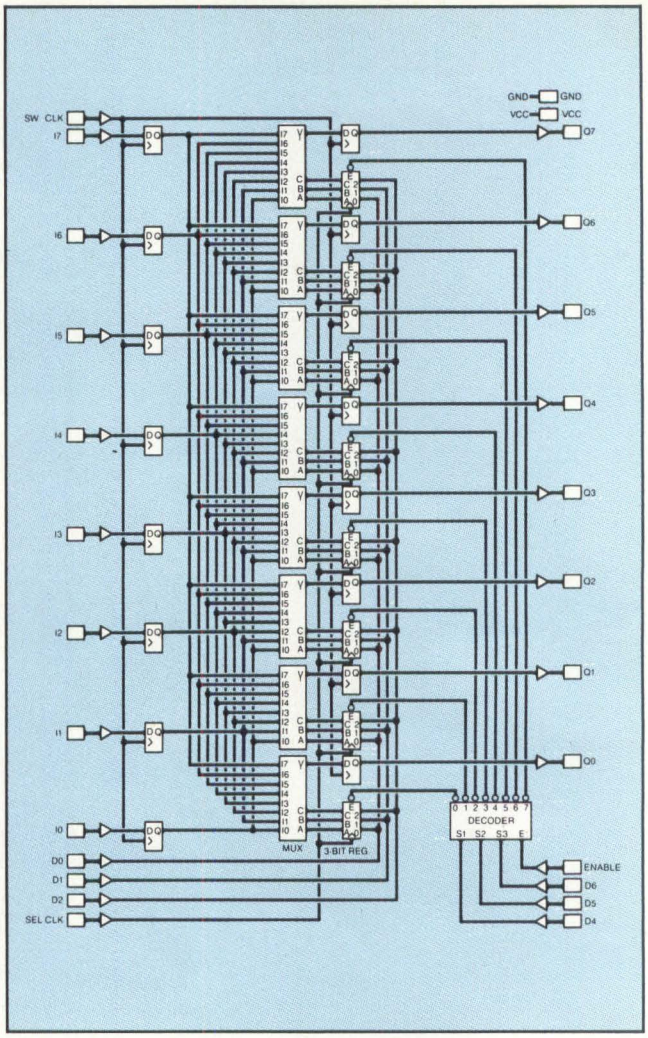

Figure 3: This schematic illustrates the basic operation of the crosspoint switch: any input signal (I0-I7) can be routed to any output (Q0-Q7). In the actual design, there are eight 4-bit wide inputs and eight 4-bit wide outputs.

LDS DESIGN VERIFIER (VALID) NETWORK SUMMARY

COMP. NAME:	DIGDES	TECHNOLOGY TYPE:	CMOS5K
ARRAY SIZE (FAMILY):	LSI5220	LIBRARY REV.:	2.17 (10/15/84)
Tue Apr 2 16:14:35 1985		VERIFIER REV.:	84.Q4.26
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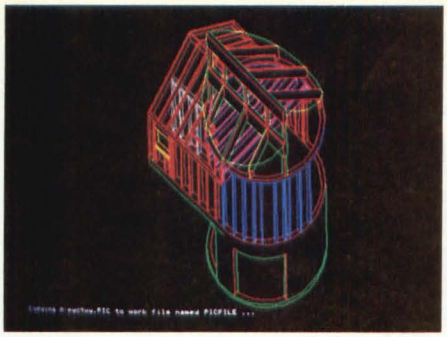
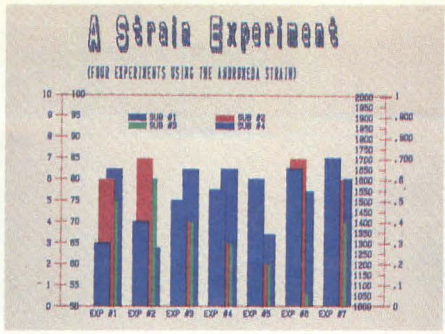
NO. OF ADD. V_{DD} PADS:	3	NO. OF ADD. V_{SS} PADS:	1
NO. OF REQ. V_{SS2} PADS:	2	TOTAL NO. OF SIGNAL PINS:	74
***NOTE: TOTALS DO NOT INCLUDE PREASSIGNED POWER PADS AND PINS			
TOTAL ARRAY PADS USED:	116	AVAILABLE CHIP PADS:	114
PACKAGE PINS USED:	78	AVAILABLE PACKAGE PINS:	110
CELL INPUTS TO V_{DD}:	0	CELL INPUTS TO V_{SS}:	0
NUMBER OF SIGNAL NETS:	537	NO. OF UNC. CELL OUTPUTS:	88
AVERAGE PINS/NET:	3.600	MAXIMUM PINS/NET:	65
WIREABILITY MEASURE FOR AUTOMATIC LAYOUT: 100.00%			

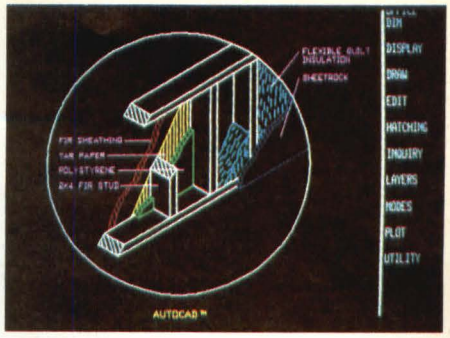
Figure 2: Since only 88.68% of the LL5140's interconnections can be autorouted, as shown in **Figure 1**, the Design Verifier was run a second time with the LL5220, a 2224-gate chip. Although the autorouter can make all of the interconnections, there are too few chip pads to accommodate the design.



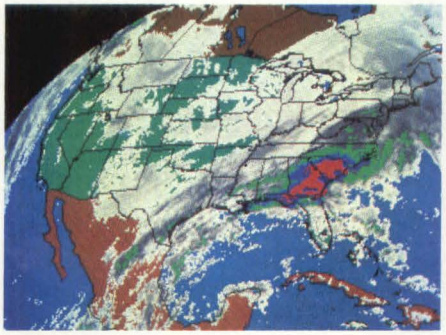
1. High Speed (MicroCAD Software)



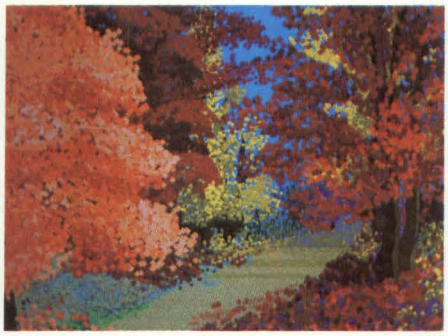
2. Dual Display Modes (Energraphics Software)



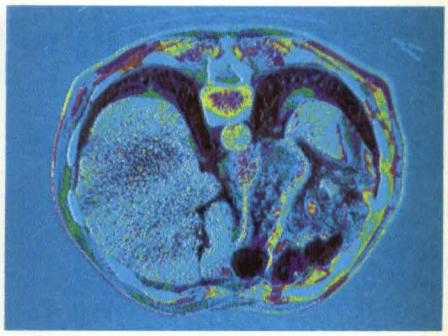
3. Simplified Processing (AutoCAD Software)



4. 9 Bit Planes (Courtesy WSI Inc., Bedford, MA)



5. 16.8M Color Shades (Courtesy Catherine Del Tito, Wave Graphics)



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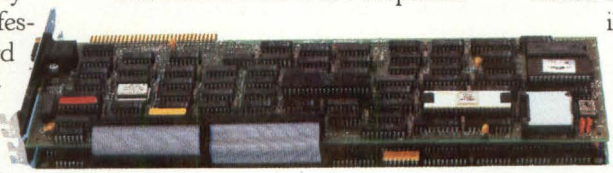

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SOFTWARE

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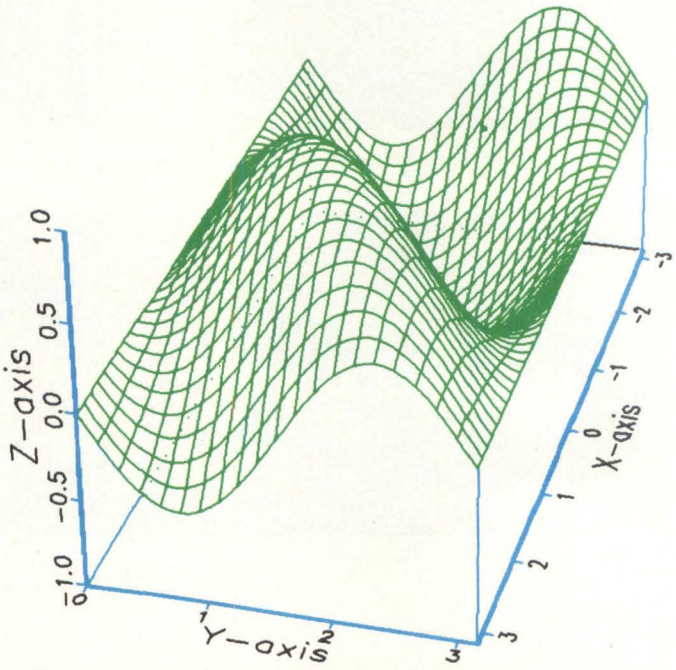

Figure 1: GraphiC can display a 3D plot with hidden line removal and text like this one in approximately 10 seconds. Though the program runs on an IBM PC, display list output files are in Tektronix format for high resolution display and printing or plotting.

High quality presentation graphics displays such as scientific plots require high resolution. Although scientific calculations are often performed on personal workstations, the graphics resolution of the IBM PC is not adequate to create accurate detail. A software package from Scientific Endeavors (Kingston, TN) produces complex scientific plots on the IBM PC.

Called GraphiC, the software is a set of C programs for creating plots, graphs and text for scientific and engineering applications. Although the program runs on a PC, the resultant graphics are not limited to the IBM PC display resolution. For high resolution display, the software can create a display list output file for driving Tektronix-compatible output devices. This is useful for entering and previewing scientific data or formulas on the PC, then displaying the results on plotters or high resolution display devices that read Tektronix files.

This software directly addresses the needs of scientific environments. These settings require high quality graphics images but may mainly use limited resolution computer hardware. However, many academic, scientific and industrial organizations do have access to devices that read Tektronix graphics files. Therefore, the authors of GraphiC turned to the IBM PC for program and graph development and to Tektronix format for intermediary display files. This combination creates the accurate plots and displays needed while allowing users to manipulate information on their personal workstations.

GraphiC is modeled around DISSPLA from ISSCO (San Diego, CA). The GraphiC package is a collection of graphics routines written in C. Users can write simple C programs and use the graphics subroutines for creating complex plots. Hidden line and 3D routines are standard (**Figure 1**). All plots are created with the Tektronix format 4096 × 3120 pixel resolution. In addition to graphics capabilities, GraphiC also has 10 fonts, four of which are simultaneously available. Greek letters and math symbols are available in two fonts. Unlimited levels of superscripts and subscripts may be employed. All font heights are continously variable.

Features of GraphiC include the ability to zoom, shrink and shift. Routines are available for creating linear, log, semi-log, log-log, 3D and contour plots. An error file is created during execution for debugging. If a plot requires a font not on the current disk, the letters would not be seen, and a file indicating a file not found would be created. GraphiC can reconstruct any Tektronix file from another computer, providing the entire plot was created in graphics mode.

One of the useful features of GraphiC is the ability to print plots on popular dot matrix printers. A C. Itoh or Epson printer can print a 96 × 144 pixel per inch image, whereas an Okidata yields somewhat lower resolution.

GraphiC is designed for use with several compilers; however, the DeSmet compiler is recommended. Complete source code is provided so the end user can create and modify programs. If the user's system has an 8087 installed, which is highly recommended, the software will access and utilize its capabilities. The result is faster execution of arithmetic-intensive graphics such as 3D.

The software was tested at *Digital Design* using the DeSmet compiler. A program was written to display a 3D plot on the PC and create a Tektronix file. The file was then displayed on a Qume QVT-211GX terminal, which has 4010/4014 capability. The resolution quality of the Qume was excellent. A complex 3D display using an 8087 took approximately 10 seconds.

—*MacNicol*

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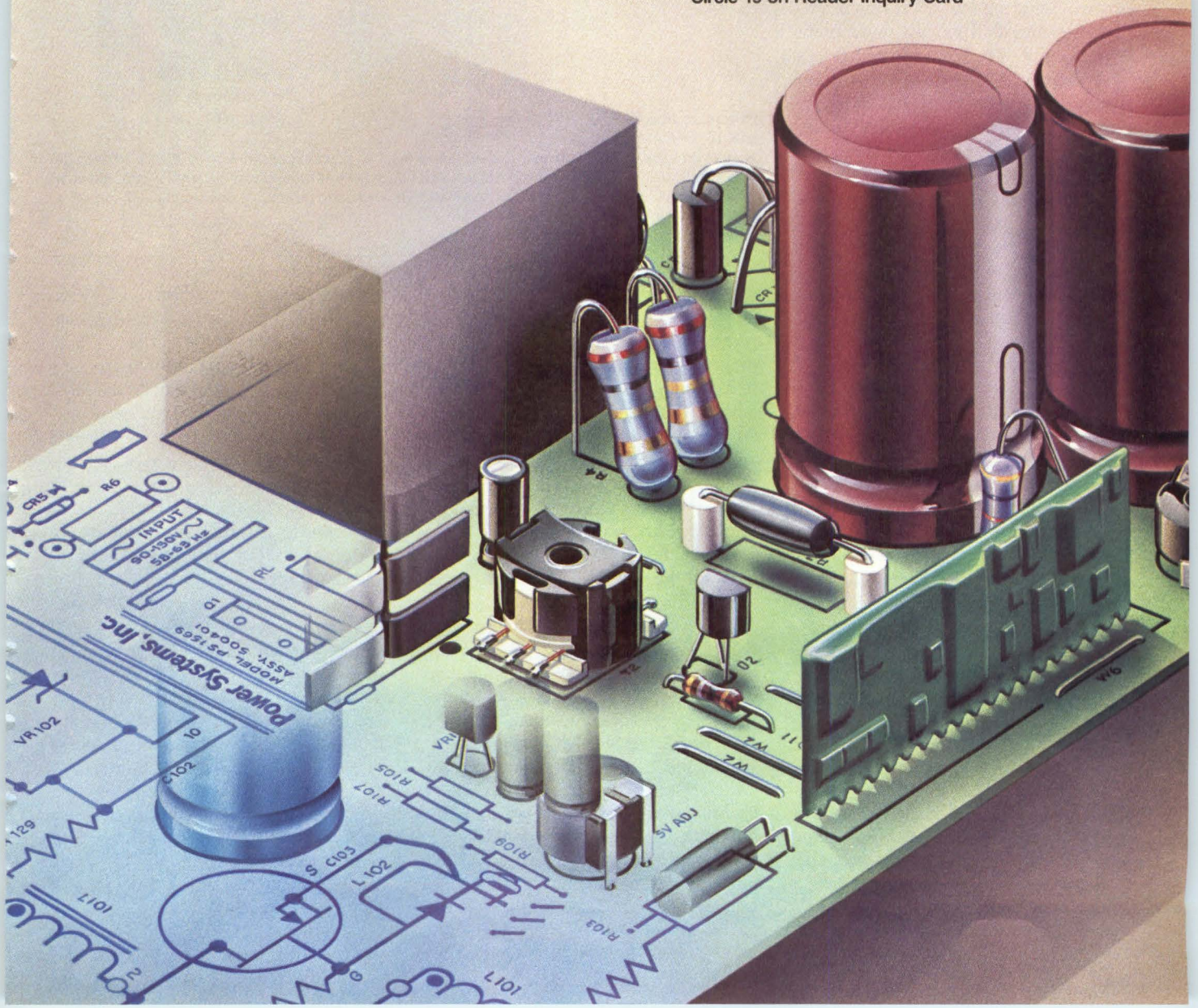
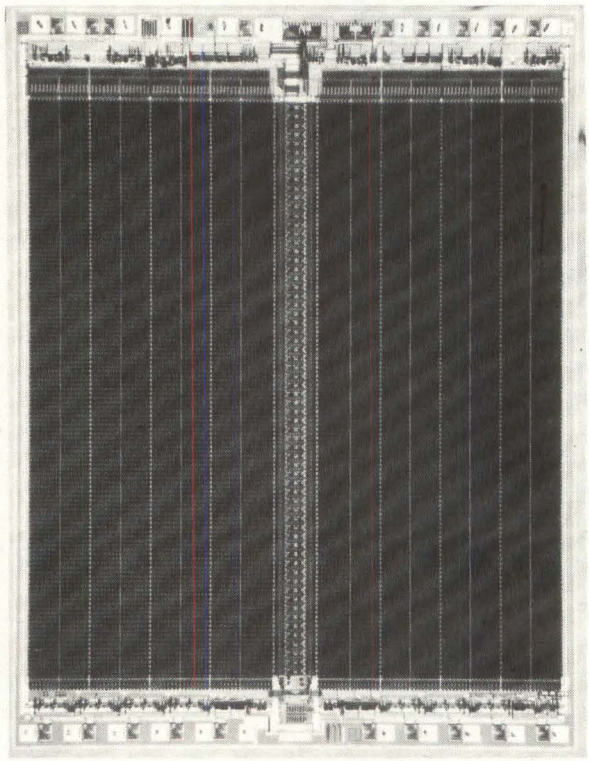


ICS

64K × 1 SRAMs Vie For DRAM Applications



Fairchild's new CMOS 64K × 1 SRAM offers access times of 45, 55 or 70 nsec with maximum active power consumption of 70 mA. To keep die size small, NMOS is used for the memory cell and peripheral support circuitry is processed in CMOS. This combination of CMOS and NMOS is also used by Hitachi and Inmos in their 64K × 1 SRAM parts.

The increasing size of main memory in multiprocessor systems demands that memory ICs be small, fast and inexpensive. Static random-access memories (SRAMs) are small and fast, and require no refresh circuitry. However, high prices have kept SRAMs out of most main memory applications, where dynamic random-access memories (DRAMs) are preferred. SRAMs have become special-purpose devices used primarily by systems architects requiring low power consumption, high speed, board space savings or ease of use.

Nevertheless, companies such as Fairchild Camera and Instrument Corp. (Puyallup, WA), Hitachi (San Jose, CA) and Inmos (Colorado Springs, CO) are very optimistic about the future for the new generation of 64K SRAMs. According to Dan Pichulo, SRAM product marketing manager at Hitachi, SRAMs organized as 64K × 1 lend themselves to several applications.

One possible use of these devices is as the main memory for either mainframe computers or superminicomputers. High performance machines demanding very fast access times may find CMOS SRAMs comparable in speed to ECL memories, without the problem of high power dissipation. Richard Phlegar, memory products planning manager at Fairchild's Memory and High Speed Logic Unit, believes that SRAMs with the ×1 organization are particularly well suited to error detection and correction in mainframes and minicomputers. However, unless the costs of SRAMs decrease, a main memory using SRAMs may not be forthcoming in the near future.

The good access speeds of SRAMs may also make the devices viable as fast writeable control stores for software. A nonvolatile memory such as a ROM can take up to 150 nsec to access the software program; for some users, this may not be fast enough. Present 64K × 1 SRAMs have access speeds between 45 nsec and 70 nsec. In addition, the CMOS SRAM can almost function as a nonvolatile memory due to its low power requirements—a battery would maintain the current necessary to retain memory.

By far the largest potential applications for the 64K × 1 SRAM are cache and buffer memories for high performance systems. The mismatch between microprocessor speed and DRAM memory speed has caused systems architects to rely on caches in order to minimize frequency of access to main memory. With new MOS SRAMs offering higher speeds and lower power dissipation, the switch from ECL parts to SRAMs for cache memory applications will certainly continue.

Fairchild, Inmos and Hitachi have taken similar manufacturing approaches to their 64K × 1 SRAMs: the memory cell is processed in NMOS and the peripheral support circuitry is CMOS. Kirk MacKenzie, Vice President of Marketing and Sales at Quasel Inc. (Santa Clara, CA) approves of the mixed process devices, saying that it may be the most cost-effective way to produce low power, high speed SRAMs. NMOS allows a higher density storage element and enables a smaller die size than a fully CMOS SRAM. CMOS peripherals reduce power dissipation problems. In addition, CMOS circuits are more resistant to soft errors.

Even with the access time improvements made on MOS SRAMs, several supercomputer and superminicomputer manufacturers still feel that the new generation of 64K × 1 devices are simply not fast enough. They would like to see the larger SRAMs comparable in access time to smaller SRAMs such as the 16K × 1, which can now reach speeds of 25 nsec. If SRAM manufacturers can push the 64K × 1 SRAM to those times, then perhaps systems architects for those larger systems will view the device as a better upgrade.

—Meng

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COMMUNICATIONS

Options Multiply For High Speed Unibus Communication

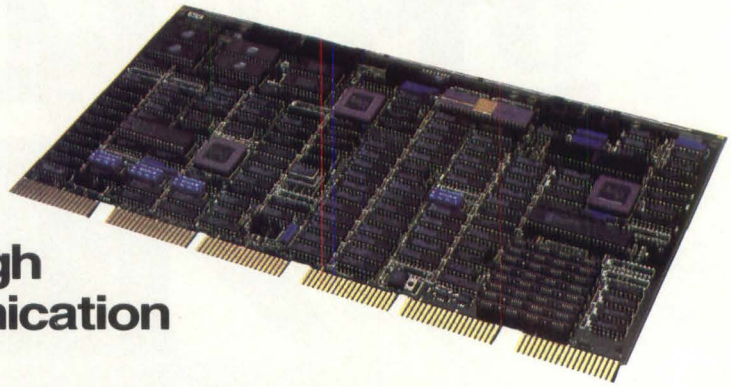

Figure 1: Host-to-host communication at 1.544 Mbits/sec is provided by ACC's ACP 6100 Unibus board. A four-bus architecture is used to achieve such high speed.

A single Unibus board may now provide 1 Mbit/sec or faster data communication for DEC minicomputers. The DMZ 32 from Digital Equipment Corp. (Maynard, MA) provides a 1.544 Mbit/sec T1 trunk for 24 multiplexed lines; it comprises a distribution panel and a Unibus module. DEC is also manufacturing a 1 Mbit/sec interface board for links to AT&T's Datakit Virtual Circuit Switch. The KMS11-K will be offered by AT&T Technologies (Morristown, NJ). For host-to-host links, Advanced Computer Communication (Santa Barbara, CA) offers the ACP 6100 (**Figure 1**) for nonmultiplexed T1 connection.

AT&T's Datakit-to-Unibus board will provide a multiplexed channel between computer and data switch. This board will operate at 1 Mbit/sec, not the 320 Kbits/sec of products linking AT&T 3B computers to Datakit. Initially, AT&T will use the KMS11-K internally for telephone company links. Distributors of Datakit as a twisted-pair local area network will also offer the board.

Although the DEC and the ACC boards both have Unibus and T1 interfacing, they serve different purposes. T1 speed is used on DEC's product as a trunk for multiplexing up to 24 lower speed lines, while ACC uses the entire channel for a single 1.544 Mbit/sec link. The DMZ 32 is an extension of DEC's asynchronous multiplexer line (*Digital Design*, March 1985), in which distribution panels are used for multiplexing and demultiplexing channels (**Figure 2**). A DMZ 32 panel may be next to the computer or remote, connected by two cables for the T1 link. The Unibus board at the host contains RAM shared by the Unibus and the 1.544 Mbit/sec T1 line.

An active distribution panel manages the individual terminal lines. Maximum speed on each line is 19.2 Kbits/sec. The DMZ 32 provides modem control and split baud rate on all lines. The system also has DMA capability on transmit. The board architecture speeds communication functions, and the distribution panel off-loads line handling.

With the ACC front-end processor board, Unibus computers can transmit and receive one full-duplex channel of HDLC at 1.544 Mbps. While the DEC board uses shared RAM between the Unibus and the T1 interface, the ACP 6100 centers around a four-port DRAM array surrounded by four 68000 microprocessor buses (**Figure 3**).

Each bus in the "Quadbus" system is independent and electrically isolated, resulting in high throughput and minimum waiting for bus access. RAM access is made central to the system, not the microprocessor bus, since memory is what peripherals need. Individual bus segments are connected or disconnected according to bus activity.

In addition to the 68000 CPU bus (CBUS), there is a peripheral bus (PBUS), a DMA bus (DBUS) and a Unibus (UBUS). Three-state buffers isolate each bus from memory signals. An 8409 provides DRAM timing and control. Ar-

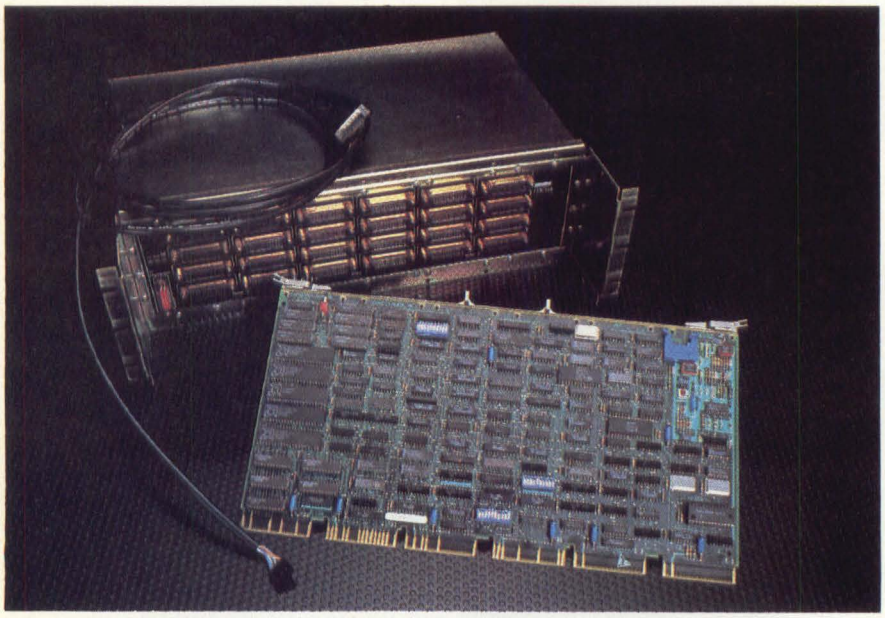

Figure 2: T1 speed of 1.544 Mbits/sec is used as a trunk to multiplex up to 24 channels in the DEC DMZ 32. T1 and Unibus interfaces share on-board RAM. The distribution panel in the background handles multiplexing and demultiplexing of individual lines.

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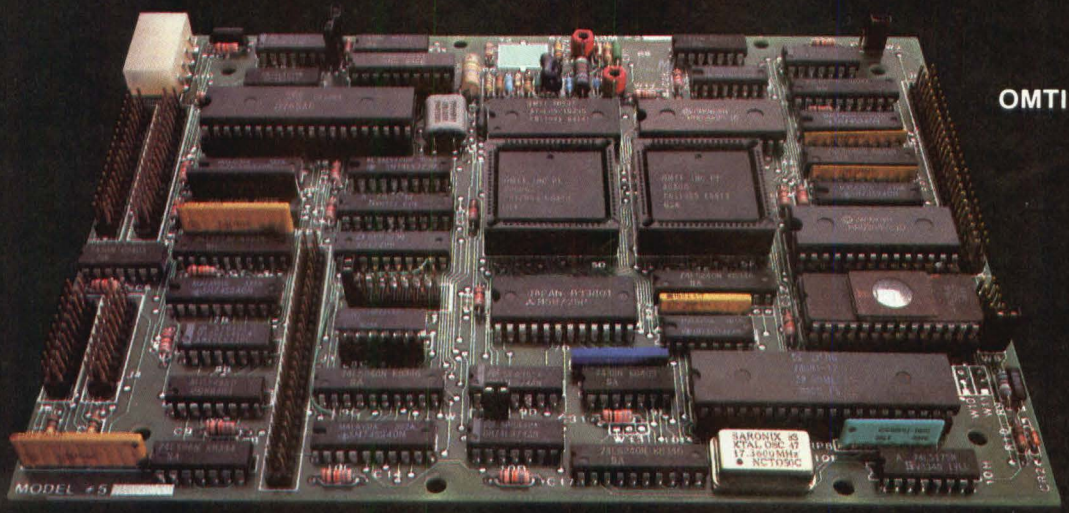

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bitration and timing to determine which of the buses gets memory cycles is implemented in PALs. The PBUS is given highest priority for memory access because it may interface to high burst rate devices like network controllers. Next priority is the Unibus, then the DMA bus and lowest priority is the CBUS.

Since 68000 and Unibus memory organizations differ, data transfer between the two is via the DBUS interface. A four-port 68450 DMA controller programmed by the 68000 exchanges bytes in a word for transfers to and from the Unibus. The 68450 also ties into an 8068 for data encryption. This security feature meets National Bureau of Standards Data Encryption Standards (DES).

Using the four-bus architecture of the ACP 6100 for a single channel provides speed adequate for computer-to-computer transfers. In contrast, most communication lines operate at several hundred Kbits/sec maximum. ACC calls this the first iteration of the Quadbus architecture and plans to use it in other products where RAM access is the bottleneck.

These are only three of the available Unibus communications products. Since they occupy only one backplane slot, a variety of connections can be made from one host. Microprocessor control and shared RAM architectures will allow communication boards to act as front-end processors and extend access to valuable resources.

—Pingry

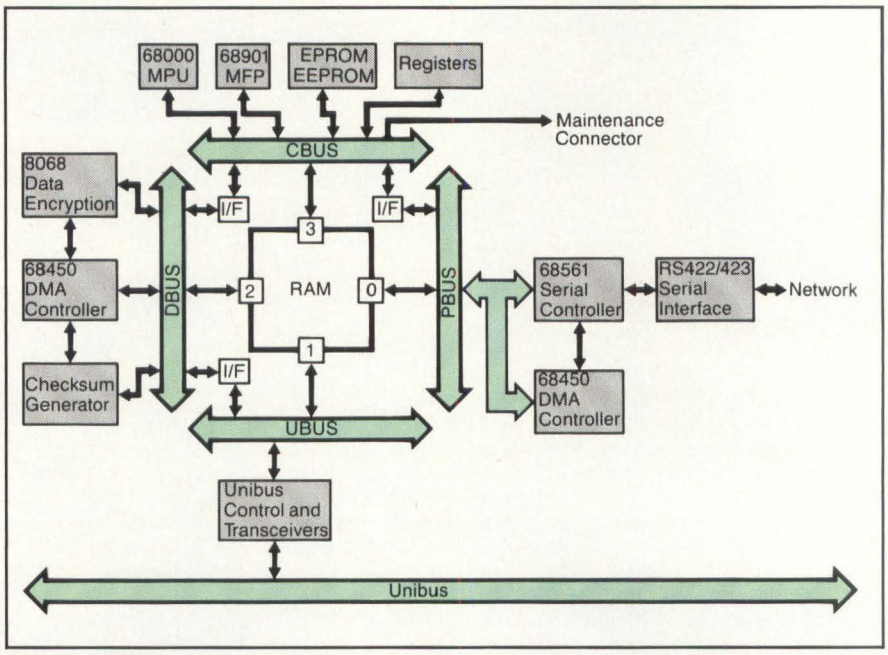

Figure 3: ACC's Quadbus architecture is optimized for memory access. A central RAM array has ports into the Unibus (UBUS), the DMA bus (DBUS), the CPU bus (CBUS) and the peripheral bus (PBUS). Interface modules between buses allow transparent connection of devices on two adjacent buses (except UBUS to PBUS).

Fiber Optic Transmission Schemes Expand Standard Local Area Network Possibilities

Fiber optics suppliers have long been seeking nontelephone applications for the technology. Now fiber optics can realistically compete in the active local area network market. Several companies have had optical links for single node connection into a coaxial cable network for years. Totally fiber networks have been available from only a few sources and operate on a passive star scheme. WhisperNet, an all-fiber network from FiberCom (Roanoke, VA), is an active ring topology Ethernet, more like coaxial systems (**Figure 1**).

Fiber optics are best suited to point-to-point links, mainly because taps (as in a bus configuration like Ethernet) cause large power drops. The all-optical 802.3 Ethernet systems that have been available for several years have put point-to-point links from all nodes into a central wiring cabinet (**Figure 2**). Within the cabinet is an optical star coupler, where input signals are distributed to all output fibers. Both Siecor (Hickory, NC) and Codenoll Technology (Yonkers, NY) use this star-shaped broadcast system.

One reason that these optical networks do not use a physical ring is that if any node in a ring fails, the entire network goes down. FiberCom has a bypass scheme that assures the network will continue to function even if three consecutive nodes have failed. Fully reversing bypass switches developed and produced by Kaptron (Palo Alto, CA) used at each WhisperNet station provide this ring reliability. With star-shaped networks, the active collision detection components in the central cabinet can also bring down the entire network if they fail. Siecor has

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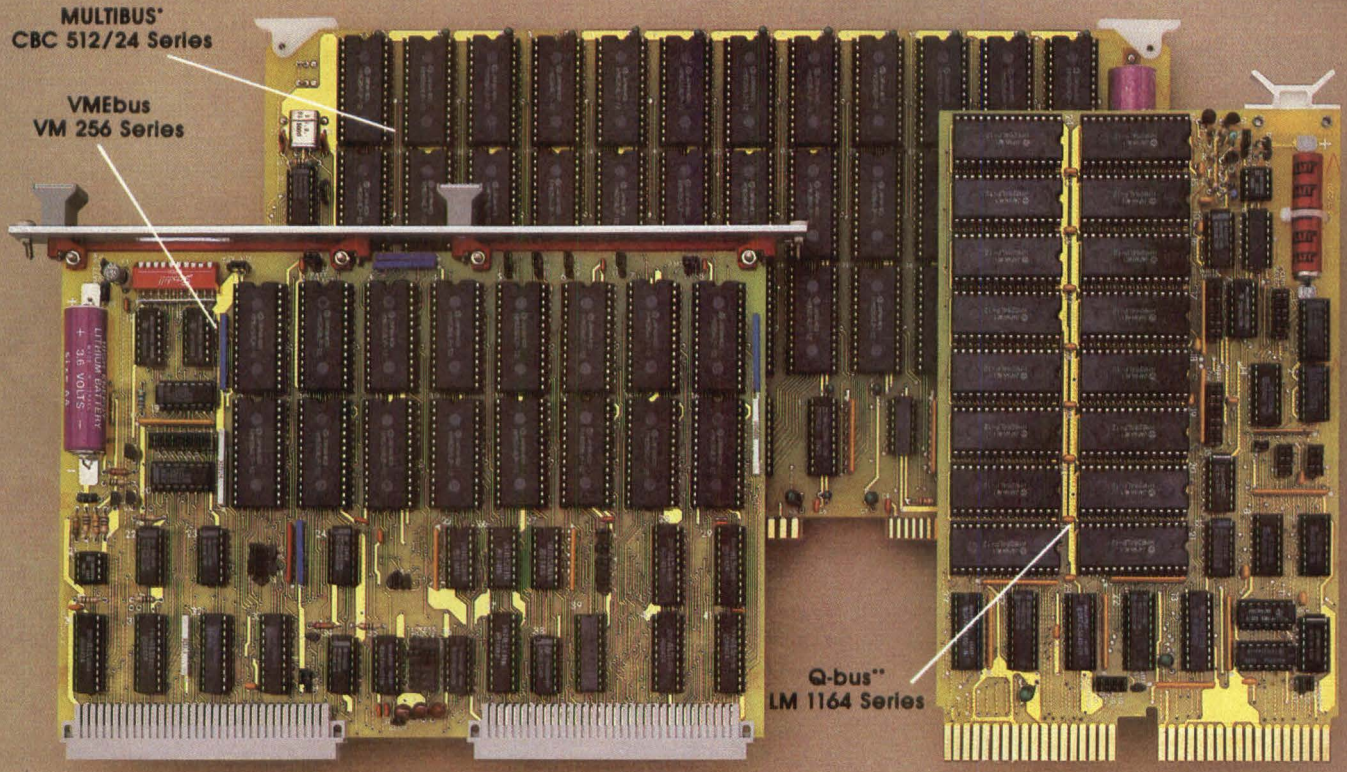

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addressed that problem by providing collision detection in the transceivers and a fallback passive mode for the wiring center.

Despite the limitations of point-to-point networking, some other features of fiber optics are attractive. It is immune to EMI and RFI; many current optical links are installed to minimize induction effects from lightning or industrial equipment. Conversely, since signals are optical and not electrical, they do not radiate. This makes meeting FCC regulations easier, and WhisperNet can meet military Tempest specs as well. Optical links are free of ground loops and dielectrically isolate attached devices. In addition, bandwidth is broader (requiring no equalization), and attenuation rates are much lower for optical cable than for coaxial. Longer transmission links can be made without repeaters using optical fiber.

Fiber optic data communication links are mainly used to extend the distance between two devices. This benefit may extend to optical networks as well. Ethernet nodes on a coax system are specified at a maximum of 1.8 km apart with 500 meter maximum segments. Siecor claims Net 10 segments can be up to 2.5 km long. To maintain total Ethernet compatibility including propagation delay, Siecor uses the same 2.5 km end-to-end maximum as coax systems.

The WhisperNet ring can be up to 4 km end-to-end. Whereas the 1024 node maximum Ethernet configuration using coaxial cable can cover 5 square km (1.9 square miles), a WhisperNet network of 1024 nodes can cover 50 square km or 19 square miles. This assumes multiple rings, such as one on each floor of a building or one 4 km ring in each building of a campus linked together to make a large system. How Ethernet timing is acheived over these longer links and whether it is strictly 802.3 compatible has been questioned. The extra distance, however, can be a major advantage in using optical cable. FiberCom claims they meet all performance specs.

In the maximum node 5 square km coaxial system, about 100 repeaters are needed. Unlike signals in coaxial cable, optical signals do not attenuate rapidly. The optical network covers 10 times the area but needs no repeaters. The number of repeaters is not the only part of a coax network that is more expensive than the optical equivalent. Optical cable is now as inexpensive as $0.60 per foot, compared to over $2.00 for Ethernet coax.

Installation costs of optical cable networks have always been an advantage because the thin cable is easier to carry, bend and maneuver. In some instances, Ethernet cable is so bulky that it will not fit in remaining duct space. Until recently, however, transmitter and receiver component costs have more than offset the installation savings. Dropping prices of optical cable and components have allowed FiberCom to proclaim their network lower cost than coaxial in most instances. Siecor points out that a central star eases diagnostics and fault isolation, one of the largest factors in installation.

The 1024 node limit is not necessarily the maximum number of devices that can be connected. Computers, terminals or other devices link into in a WhisperNet either through TFT-10 transceivers or communications servers called WhisperServs. Servers can link up to 32 devices into the network. In the Codenoll CodeNet system, an optical star coupler is needed for every 16 nodes. Stars can be connected together for a "snowflake" topology network. Either Codenet 2020 transceiver boxes or transceiver hybrid modules used on a circuit board connect nodes to the star coupler.

Wiring centers for Siecor's Net 10 include star couplers with 8 × 8 (8 input and 8 output = 8 nodes), 16 × 16 or 32 × 32 ports. As the star broadcasts a signal to all input ports, passive taps pull

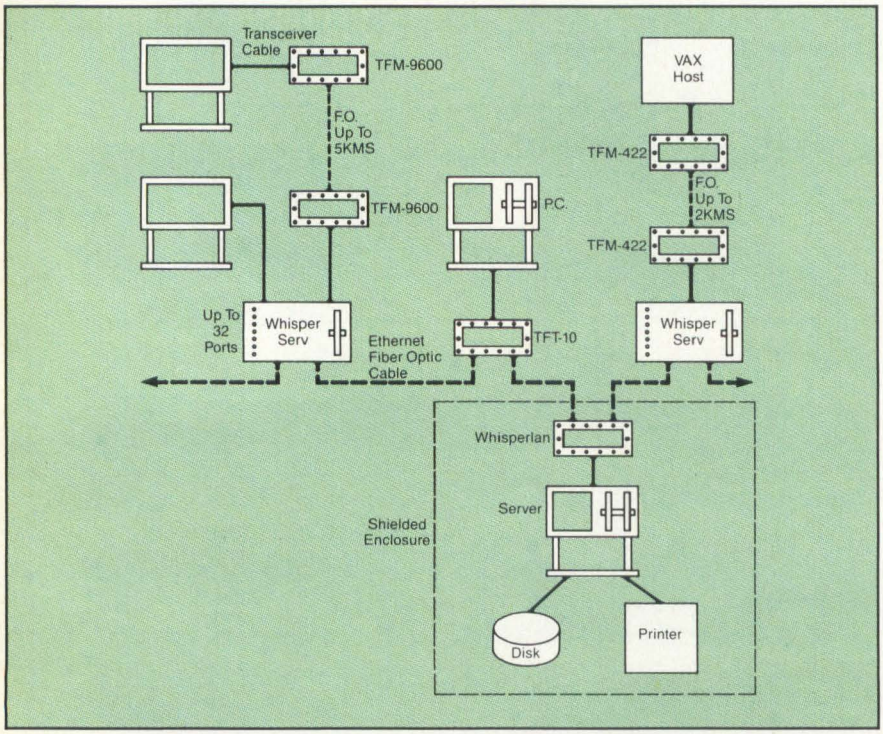

Figure 1: WhisperNet is the first commercial optical fiber local area network that uses a ring topology. Unlike the star configuration common in optical networks, it needs no central node, and collision detection is performed at the node transceiver. Though this is a point-to-point cabling scheme, it resembles the Ethernet bus topology more closely than do star networks.

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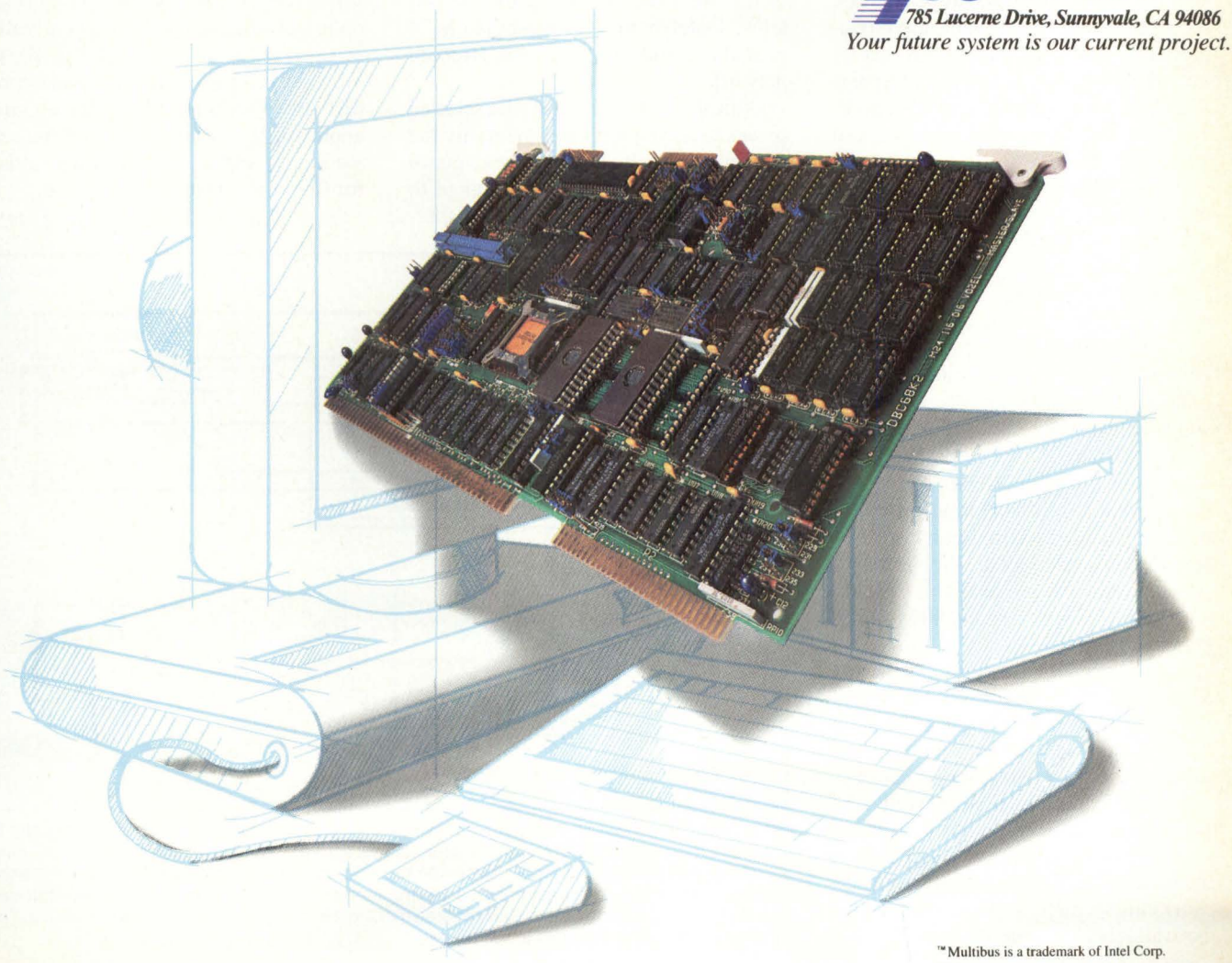

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part of the signal off (**Figure 3**) into collision detect electronics (CDE). Since the signals here are not electronic the CDE cannot use voltage differences to detect collisions like coax CSMA/CD systems. A collision is determined by the presence of more than one signal.

There is no center in Whispernet, which means collision detection resides in the transceivers. As with a coax network, the 8-wire transceiver cable provides one pair for collision detection, one for transmit, one for receive and one power pair. To further enhance industry compatibility, Whispernet will run standard XNS and TCP/IP protocols. The WhisperServ communication servers, supplied by Bridge Communications (Cupertino, CA), can be specified as servers for either protocol. Actual throughput is 200 packets/sec; with 512 byte XNS packets, the maximum throughput is about 1 Mbit/sec.

Ethernet is not the only network being implemented in fiber optics; Raycom Systems (Boulder, CO) offers ARCNET products. Datapoint's (San Antonio, TX) ARCNET is a 1 Mbit/sec token-passing system, and Raycom offers transceivers and a three-port active hub. These products can be used for an all-fiber network or be combined with coaxial cable into a single network.

The star-shaped ProNet local area network from Proteon (Natick, MA) has been promoted as operating on either twinax (shielded twisted pair) or fiber optics. Two versions of the ProNet token-passing network are available: totally compatible 10 Mbit/sec and 80 Mbit/sec systems. Both ProNet 10 and ProNet 80 are star-shaped logical rings that use the same wiring center concept as Siecor and Codenoll fiber optic networks. Proteon networks include networking software and can use all or part fiber for cabling.

Though commercial systems may be years off, an ANSI committee is working on a 100 Mbit/sec optical ring network standard called FDDI. A high-speed network chip set for this optical scheme may be available as soon as the specification is complete. Texas Instruments and Motorola are designing encoder/decoder chips for this 80 Mbaud throughput. Advanced Micro Devices (Sunnyvale, CA) is also designing several ICs to support that type of network. IEEE 802.8 is a fiber optic task force looking into several issues of optical network schemes.

In addition to these complete optical network systems, an array of companies provide single links into various standard networks. ARCNET links are available from Grass Valley Group (Grass Valley, CA) and Canoga Data Systems (Canoga Park, CA). Optical Ethernet link extenders are sold by Canoga Data Systems as well as the firms offering complete systems. Optelecom (Gaithersburg, MD) provides a link into Apollo's Domain network.

Optical links have been used in selected places to solve problems, primarily the distance limits of coax but also to guard against lightning or noise damage to signal integrity. Schemes like Whisper-Net and Net 10 may be used for entire networks. Suppliers of other types of fiber optic systems are also looking carefully at the LAN market. Corning Glass Works (Corning, NY) has announced the dBF fiber, optimized for networking applications. This is a good sign that networking is becoming a significant market for fiber optic systems.

—Pingry

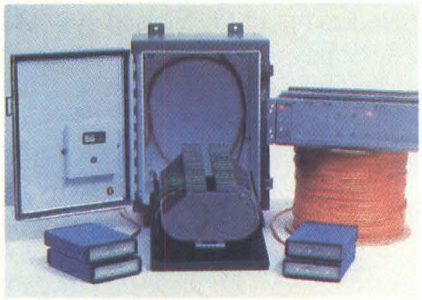

Figure 2: The Net 10 system from Siecor Electro-Optic Components uses optical fiber cable medium, shown here with orange jacketing. Small transceiver boxes are used at the nodes, and the large case in the center of the photo is the central Star Wiring Center. The star coupler is hidden here by the coils of fiber from individual nodes.

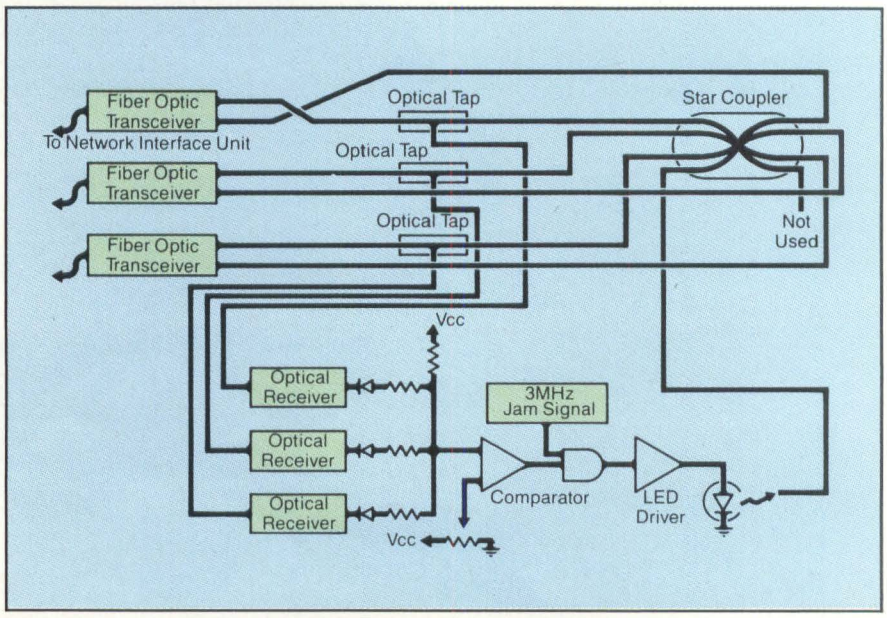

Figure 3: Collision condition determination is performed in the central wiring center in the Net 10 Ethernet-compatible optical network. Signals output from each node are broadcast to other points in the network by the star coupler. Part of the signal is tapped off for collision detection. If the collision detect circuitry senses more than one transmission, it sends a jam signal to the input side of the star coupler. Each transceiver sending data notifies the attached node of the collision. The node then times out and tries to retransmit.

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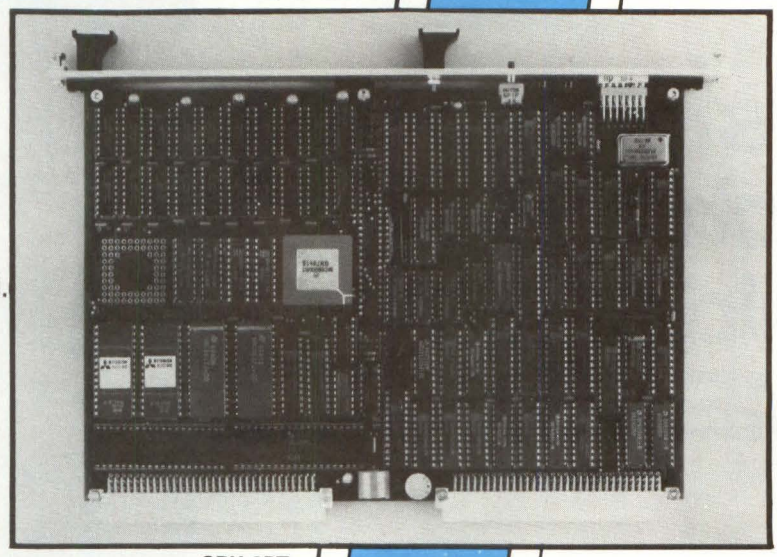

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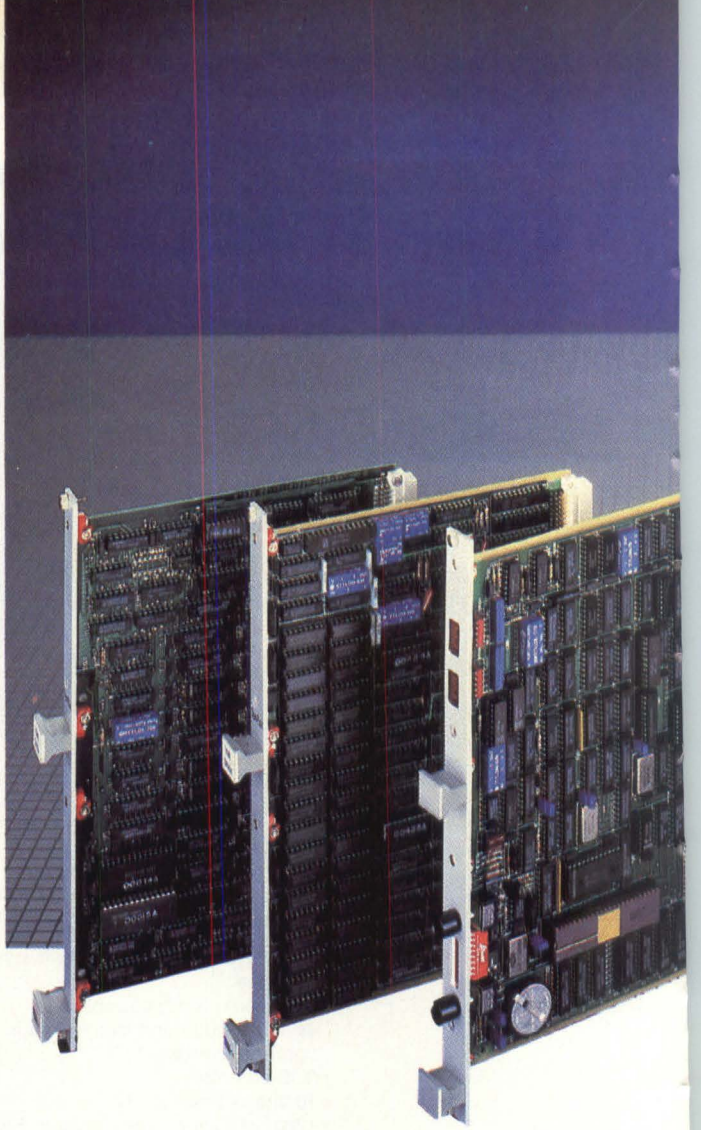
Systems Architect's Guide To The VME Bus



by David Wilson, Executive Editor

In a recent survey, Gnostic Concepts estimated that the single-board computer market would grow to $1.55 billion by 1988. Gnostic predicted that the Multibus I and the Multibus II were projected to take the largest share—44%. The VME bus is expected to have a 19% share.

There are several reasons why the VME's marketshare may be larger than predicted. One of the main indicators of the success of any bus structure in the marketplace is the number of smaller players with vertical market niches who endorse a given specification. Over the past few months, several of this type of manufacturer have either announced products based on the VME or disclosed plans to bring out new products in the next few month. In many cases, these companies virtually own a niche within the Multibus I marketplace.

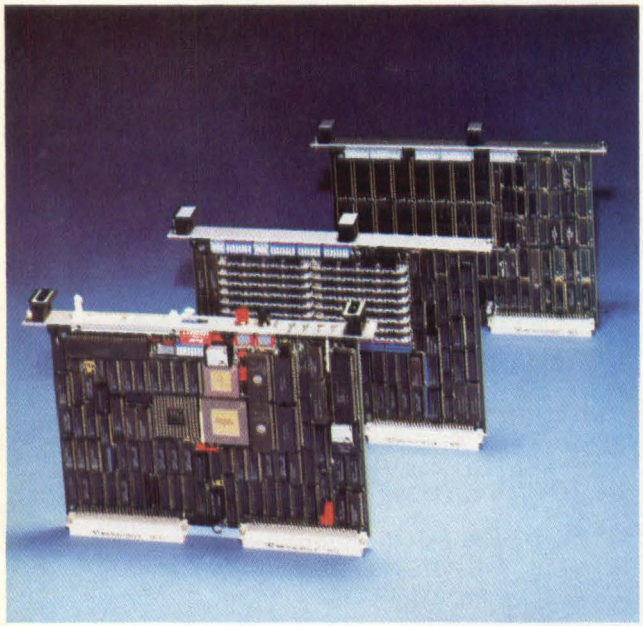


Figure 1: Motorola's latest VME offerings include a 68020-based CPU board.

Xylogics (Burlington, MA), for example, whose customer base includes Sun Microsystems (Mountain View, CA) and Masscomp, has long held the lion's share of the Multibus I disk controller market. However, Xylogics's latest disk controller, dubbed the 751, is based on the VME architecture. The board can control two SMD drives at data transfer rates from the disk up to 2.4 Mbytes/sec and DMA speeds of 10 Mbytes/sec.

Metacomp (San Diego, CA), who possibly has the largest part of the Multibus I intelligent communications controller business with its MPA-2000, has announced plans to enter the VME market with a similar product. Datacube (Peabody, MA), a more vertically based company, also recently disclosed information about a VME board set designed for electronic imaging that can be mixed and matched to a particular customer's requirements. As with any engineering decision, there are trade-offs when deciding which bus structure to endorse.

At the present time, only a few buses can support 32-bit processors—VME, Multibus II, NU Bus and Futurebus. Of these four, the only products commercially available are on the VME and the Multibus II. Of these products though, only one CPU board is available on the Multibus II, the recently announced

VME goes head-to-head with Multibus I and Multibus II

PHOTO COURTESY MOSTEK

286 board from Intel (Hillsboro, OR). VME, on the other hand, sports over 30 manufacturers (**Table 1**). Such companies as Motorola (Tempe, AZ) (**Figure 1**), Ironics (Ithaca, NY) and Matrox (Quebec, Canada) even have 68020 designs on the market today.

An important consideration when deciding which bus structure to endorse is not only the number of manufacturers, but also the potential upgrade path for the product. Multibus I has the largest portion of the OEM board marketplace; a share that is not likely to disappear overnight. Many designs in the market are based on 8-bit CPUs, and the sheer volume of vendors of Multibus I products will make it easy for the systems integrator to upgrade to 16-bit solutions. Furthermore, some smaller vendors have even proposed to upgrade to 32-bit solutions. It is likely that this may lengthen the life of the bus, too.

In the past, the limitation of a 16-bit bus structure has prevented true 32-bit μPs from being available on Multibus I systems. True 32-bit μPs with 32-bit internal and external data paths could not effectively be used on the Multibus I because two 16-bit memory accesses are required for each 32-bit memory access. But Owl Computer (Encinitas, CA) has effectively attacked this problem in the same way that DEC has attacked the design of the MicroVAX 1 (based on the Q-Bus). Instead of using the Multibus, Owl has chosen to implement a proprietary "over the top" bus between its NS32032-based CPU board and a dedicated memory board. The processor, therefore, does not require the use of the Multibus to access main memory. The systems integrator may not require additional Multibus memory boards to configure a system although additional Multibus memory boards can be used to increase the total amount of memory. Currently, Owl offers a minimum of 256 Kbytes and up to a maximum of 4 Mbytes.

Although the upgrade path to 32-bits is obviously a smoother road on the VME than on the Multibus I, those designs based on the Multibus I have used mainly Intel iAPX processors. The VME, on the other hand, is primarily a 68000 family-based bus (**Table 1**). Hence, the problem for those systems integrators wishing to switch from the Multibus I to the VME bus becomes more of a software issue than a hardware issue.

To address the problem of migrating from an older bus structure to a new one, Intel initially promised they would provide an interface from the Multibus I to the Multibus II, but so far no such interface product has been announced. When Sun Microsystems was looking for a 32-bit bus for future workstations in October 1983, it examined both the Multibus II and the VME bus and chose to go with the VME bus. According to Vice President of Technology Andy Bechtolsheim, the Multibus II is the strongest for tightly coupled multiprocessors, but weaker for single-processor systems. This is because the Multibus II is a synchronous bus in which the master and the slave have to synchronize the bus. This maximizes available bandwidth in multiprocessor systems, but degrades performance for a single-processor system with asynchonous master and slave because of the number of synchronization points. Multibus II also required custom-bus interface circuits that were not available.

Sun's implementation of the VME bus was done on triple height/full depth Eurocards (366.66 mm $\times$ 400 mm) so that major system components could be placed on a single board

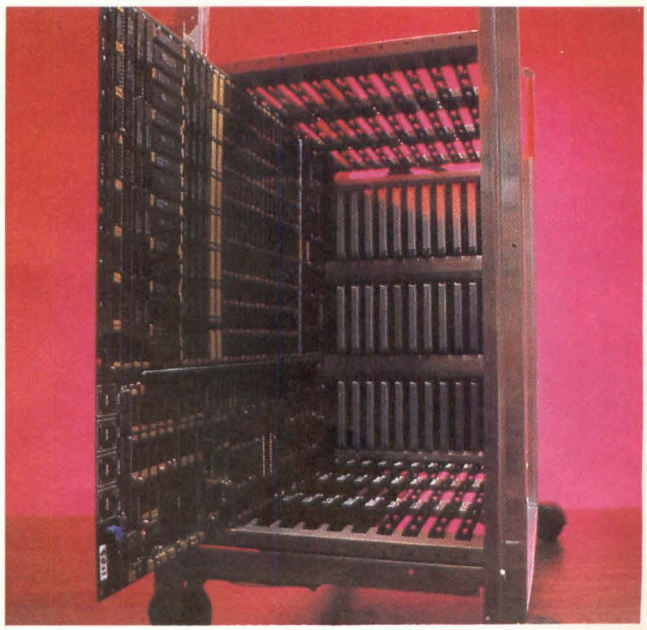


Figure 2: Sun Microsystems' VME-based workstation is based on triple-height full-depth Eurocards.

(**Figure 2**). Multibus II system builders may find that they are faced with the same space constraint problems as their VME counterparts, especially if they wish to include all the features of the bus such as unsolicited data messages and sequential transfers. NCR Corp. (West Columbia, SC) has already proposed a triple height version of the Multibus II, but has been forced to design three custom 84-pin gate arrays to support the advanced features of the bus. For the OEM, the form factor of newer buses is a vital consideration. Products available on the VME today are most commonly found in a single or dual category. But as the use of custom VLSI increases and number of dedicated VME ICs from Signetics (Sunnyvale, CA) and Motorola increases, the single-height module may become more popular.

One company banking on that trend is Microcosm (Beaverton, OR). It recently entered the VME market with a line of VME products that center on a cache-based 68000 board. The companies' future product plans include a VME bus system controller board, an EPROM/Static RAM board and a 512 Kbyte dynamic RAM board. Microcosm's main competitor is Mizar (St. Paul, MN) who has been in the market with a 68000-based single-height VME card for some time.

Another interesting fact to consider when choosing a bus structure is the systems integrators' familiarity with the older bus structures and their modes of operation. In terms of its structure, it would be more appropriate to class the VME in a group of older bus structures, such as the S-100 and the Multibus I, rather than directly compare it to the Multibus II. However, this may turn out to be more of a benefit than a detriment to the success of the bus. Going the VME route, the systems integrator would clearly not have to go through a re-education process as he may have to with Multibus II.

The major market for both the Multibus I and the VME is the area of real-time control. One of the most important requirements of this market is to provide an interrupt handling and generating mechanism to schedule various tasks. In many machine control situations, a number of dedicated processors are controlling an external process. In most cases an architecture of this kind is a single handler system which has a supervisory processor that receives and services all bus interrupts. This allows the supervisory processor to service all interrupts in a prioritized manner. The dedicated processors are not required to service interrupts from the bus, but give primary attention to the interrupts received from the machine or process they control.

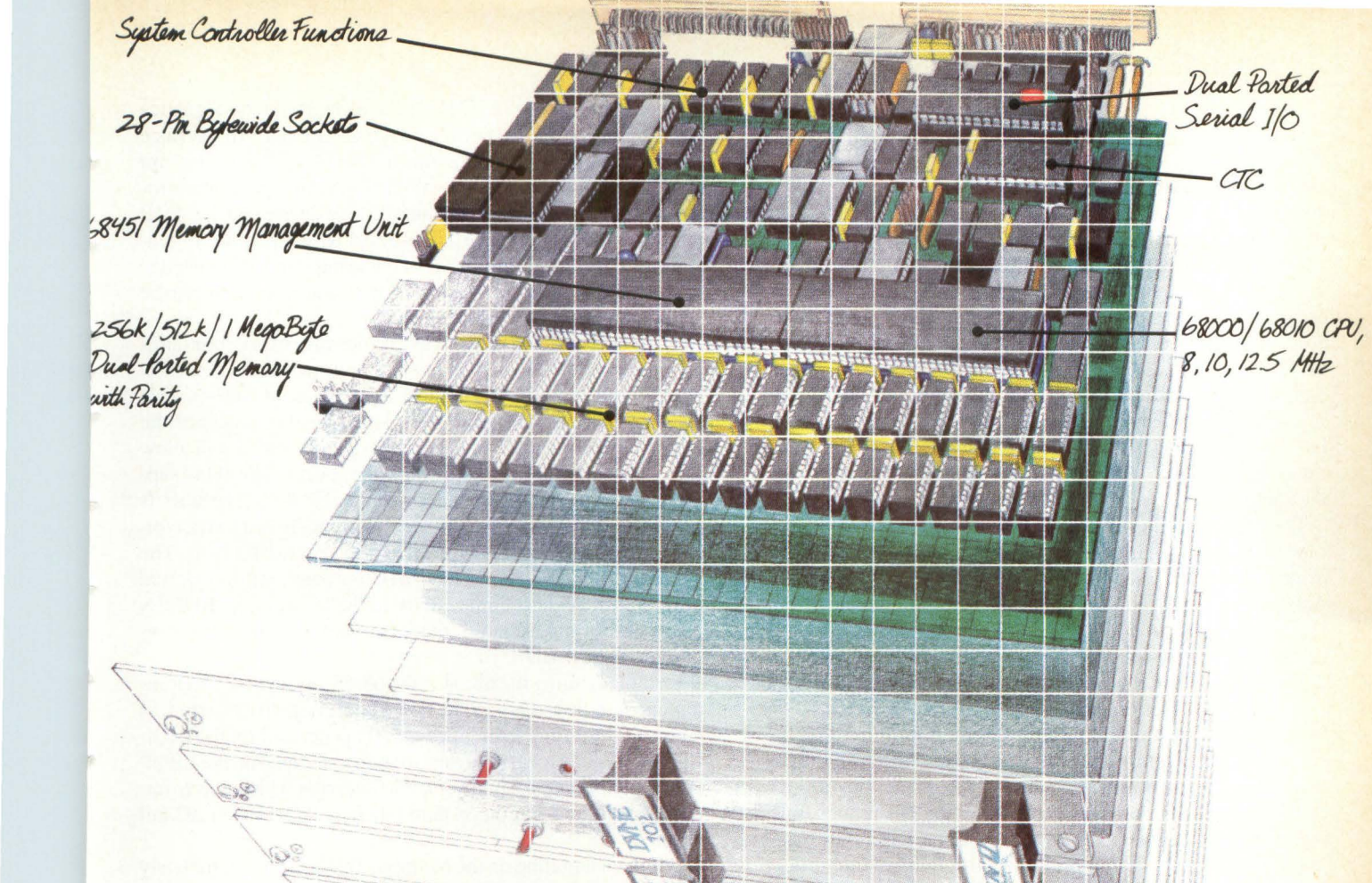
In the Multibus I system, the interrupt service lines (INTO* to INT7*) are used by any bus module to activate an interrupt service request from the system master. A requesting device activates the interrupt signal and keeps it active until serviced (INTO* has the highest priority). An interrupt acknowledge (INTA *) is generated during interrupt cycles on the bus. It is

VME Product Quick Reference Guide

CPU/MPU	68000	Z-80	80186	Z8000	16000	Form Factor Single	Form Factor Dual
Arcom Control Systems				X			X
Astraea	X	X					X
Beston	X						X
Colex	X		X				X
Compcontrol	X						X
Dec-Tec	X						X
Dual Systems	X						X
Dy-4 Systems	X	X					**
Ebnek					X		
Elec. Mod. Sys.	X						X
Electronic Solutions	X						X
Eltec Electronic	X						X
Force Computers	X						X
Hubner & Worm	X						X
Intac		X					X
Integrated Solutions	X						X
Ironics	X						
Kontron Mikrocomputer	X					X	
Manudax	X						X
Micro Computer Systems	X						X
Microsys	X						X
Mizar	X					X	X
Motorola	X						X
Omnibyte	X						X
Pacific Microcomputers	X						X
PEP Electronik Systeme	X					X	X
Performance Tech.	X						X
Philips International							
Sigen	X						X
Signetics/Philips	X						X
Sky Computers	X						X
Systemforschung	X						X
United Technologies—Mostek	X						X
Wormald	X						**

**Non. Std. depth

Table 1: Over 30 CPU products are available on the VME bus. Note, however, the lack of Intel processors that are supported.



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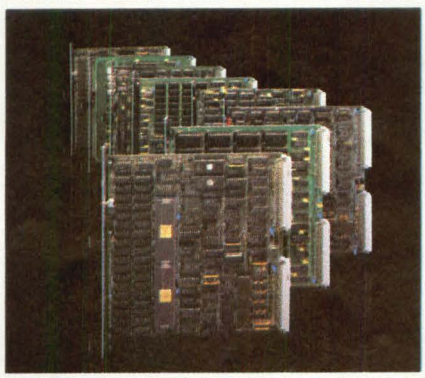

DVME-*105* – 68000/68010 CPU with dual-ported serial I/O and 14 bytewide sockets.

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DVME-*351* – A 512K Byte memory board with 10Megaword per second raster video port. Supports 16/32 bit VMEbus read/writes.

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used to freeze the interrupt status of all the interrupt controllers in the system and then get the interrupt vector address from another module in the system. Multibus supports two interrupt implementation schemes: nonbus vectored and bus vectored.

The VME also has dedicated signal lines for handling interrupts. Although the VME bears some resemblance to the Multibus I, it is in the area of handling interrupts that the VME and the Multibus II differ the most. In the VME system, dedicated modules are specified for interrupt handling and generating. This relieves other masters in the system from this task. However, Intel has chosen to handle interrupts without dedicated devices. Intel's solution is done through a message passing routine from one master to another.

The interrupt scheme on the VME bus consists of an Interrupt Handler and an Interrupter. The signals involved are seven priority Interrupt Request lines, IRQ1*-IRQ7*, one Interrupt Acknowledge line, IACK*, and two Interrupt Acknowledge Daisy-chain lines, IACKIN*/IACKOUT*. The Interrupt Handler generates the interrupt acknowledge signal, which drives the interrupt request lines, IACKIN*/IACKOUT*. The seven interrupt request lines IRQ1*-IRQ7* are driven by the Interrupter. The way the interrupt portion of the VME bus works is similar to the way the arbitration portion of the bus works. The seven prioritized Interrupt Request lines, IRQ1*-IRQ7*, work in much the same way that the bus request lines works. When a device wants to access the bus, it generates a bus request with one of the four prioritized Bus Request lines, BRx*. Similarly, a device that wishes to generate an interrupt will drive one of the seven prioritized Interrupt Request lines, IRQx*. The interrupt request lines are driven by the Interrupt, and the Interrupt Acknowledge line is driven by the Interrupt Handler. The Arbiter monitors the Bus Request lines, and when the bus is available, it will drive the appropriate bus grant line. The Interrupt Handler monitors the seven interrupt request lines, and when the bus is available, it will drive the Interrupt Acknowledge line.

To ease the design of VME board level products, Signetics has recently added two new devices to its list of VME interface products – an interrupt generator (68154) and an interrupt handler (68155). The Signetics 68154 interrupt generator provides an interface between the interrupting device and the VME bus (**Figure 3**). The device has three primary functions: to generate bus interrupt requests, to sit in the interrupt acknowledge daisy chain and to allow a status/ID byte (interrupt vector) to be supplied to the system if needed.

The 68154 provides a vehicle for interprocessor communications on an intelligent peripheral controller board or a CPU board. Local data pins (LD1-LD7) serve as a local data bus. This allows a local master to access two internal registers of the 68154. During an interrupt acknowledge, the 68154 will allow for a status/ID byte to be supplied to the system. The 68154 supplies seven of the eight needed Status/ID bits. The user is allowed to externally supply the least significant bit (LSB), typically the system address line A1 of the Status/ID byte. The IRQ1-IRQ7, DTACK and BD1-BD7 outputs require external buffers to provide adequate drive to the system bus. BUFEN provides the output enable control for the data buffer that is required for BD1-BD7.

Complementing the 68154 is the 68155, an asynchronous interrupt handler. The 68155 can handle interrupts from 14 sources: seven bus interrupt requests generated on the IRQ1-IRQ7 inputs, six local interrupt sources generated on the LRQ1-LRQ2 inputs and one nonmaskable interrupt which may originate locally or from the system (such as the systems AC fail signal).

Interrupt handling on the Multibus II is done in a completely different way. For example, there are no signal lines on the iPSB to handle interrupt; interrupt generating and interrupt handling is under the control of each individual master in the system. When a device wants to interrupt another device, it does so by passing a message to that device. This involves arbitrating for the bus, gaining access and passing the information. Message passing is achieved through a particular address space called the message address space.

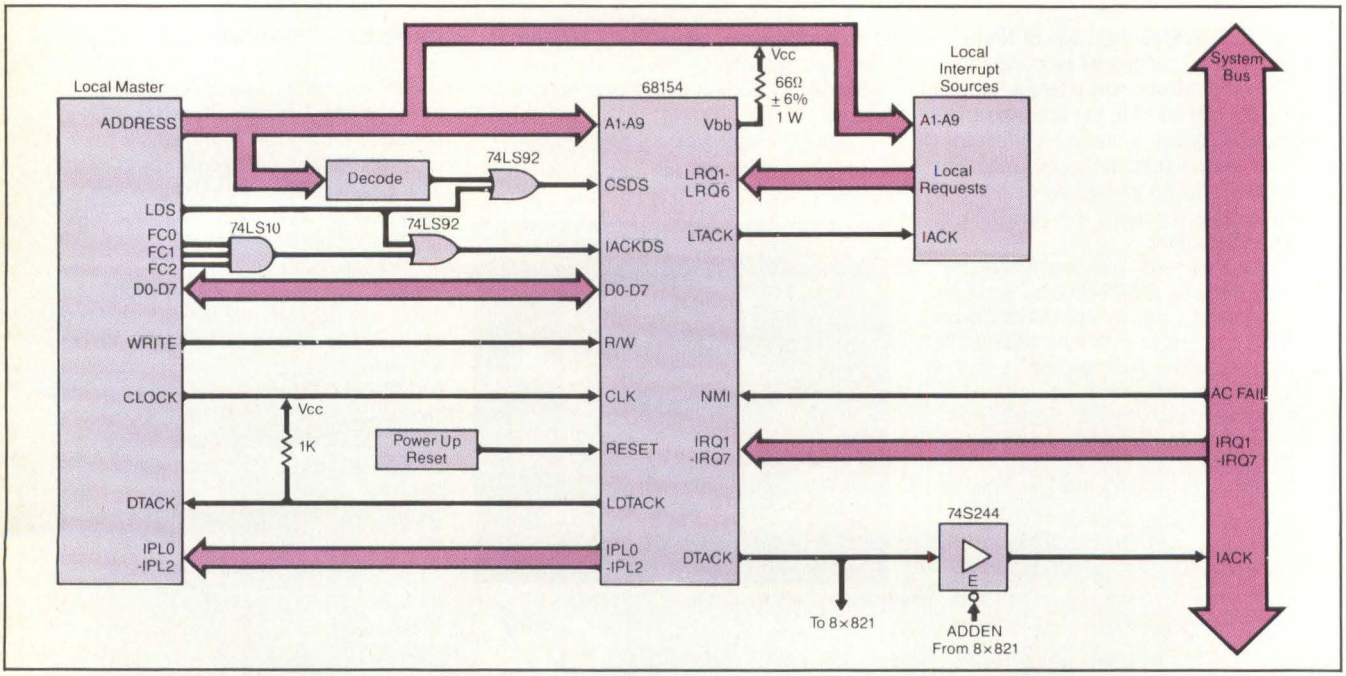
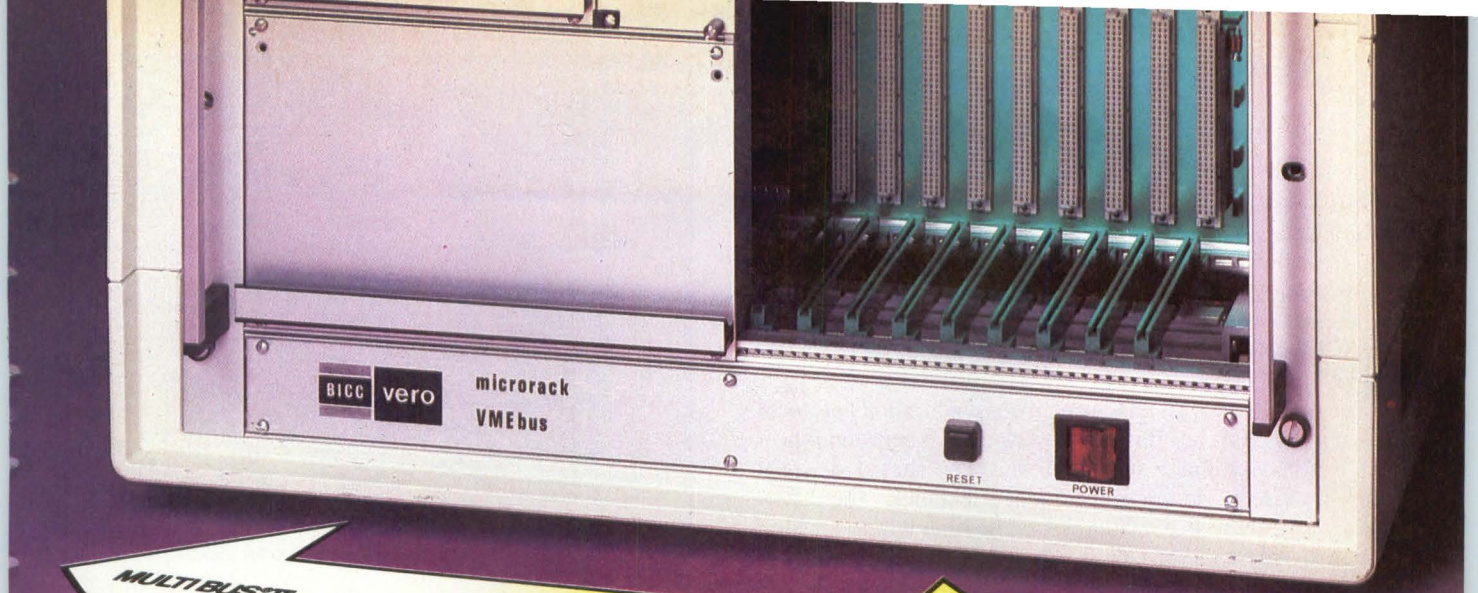
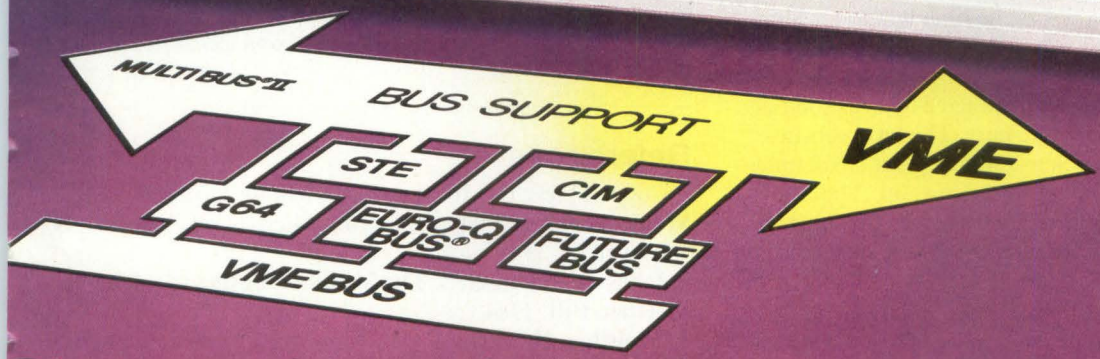


Figure 3: Signetics' 68154 interrupt generator provides an interface between an interrupting device and the VME bus.





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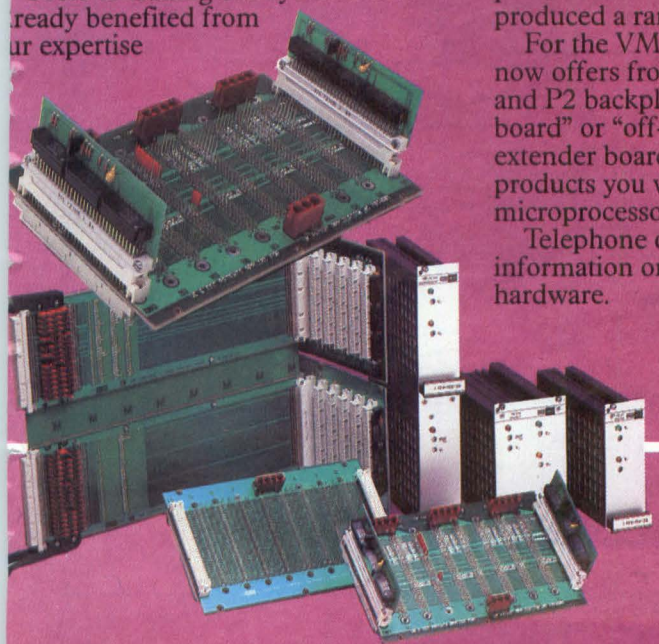

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VME BUS SUPPORT HARDWARE

In the past six months, a great deal of marketing activity and several documents have attempted to compare the VME and the Multibus II. Many have added a great deal of confusion rather than clarification to the situation. The whole issue of what the difference is between an asynchronous bus and a synchronous bus has been confused, mainly to the advantage of the VME camp.

The VME bus is an edge-sensitive asynchronous protocol whereas the Multibus II is a level-sensitive asynchronous protocol. The Multibus II technique has been named synchronous because of the presence of a central clock. The difference between the two techniques is the time window within which signals are considered valid. With the edge sensitive technique, the signal lines are always considered valid and any state transition (signal edge) will be acted upon as soon as it propogates from one board to the next. The level sensitive technique utilizes a central clock to define regular small time windows during which the signal lines are valid. This technique requires that all signals are settled and remain stable (at one level) during any valid time window. These differences are illustrated in **Figure 5**.

Apart from the asynchronous versus synchronous issue, the Multibus II may now be perceived as an architecture that is unsuitable for applications in real-time control systems, primarily due to its novel message passing architecture. This, however, is clearly not the case. When Intel announced its set of boards (*Digital Design*, February 1985, p. 24) it did so with the real-time operating system iRMX86. Furthermore, Intel actually claims that the Multibus II is faster than the VME in real-time applications. Whether this is true or not, it does appear that the two buses will compete in the same market.

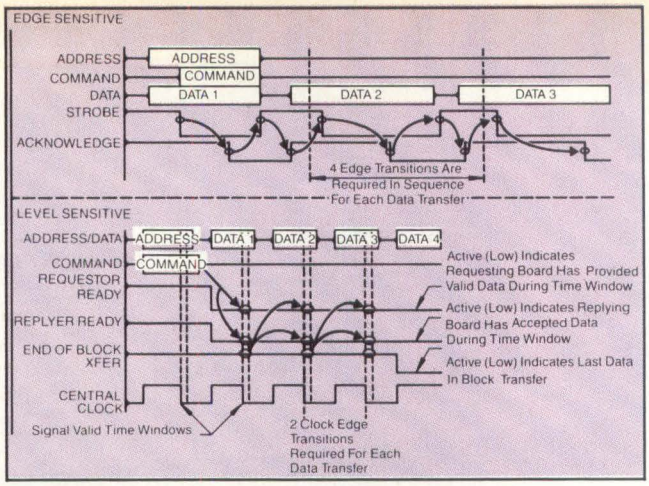

Figure 5: Edge-sensitive versus level-sensitive handshake techniques (shown is block write).

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2. Johnson, J., Kassel, S. **The Multibus Design Guidebook**. McGraw-Hill, 1984.
3. **Multibus II versus VME**. Motorola Document. August 1984.

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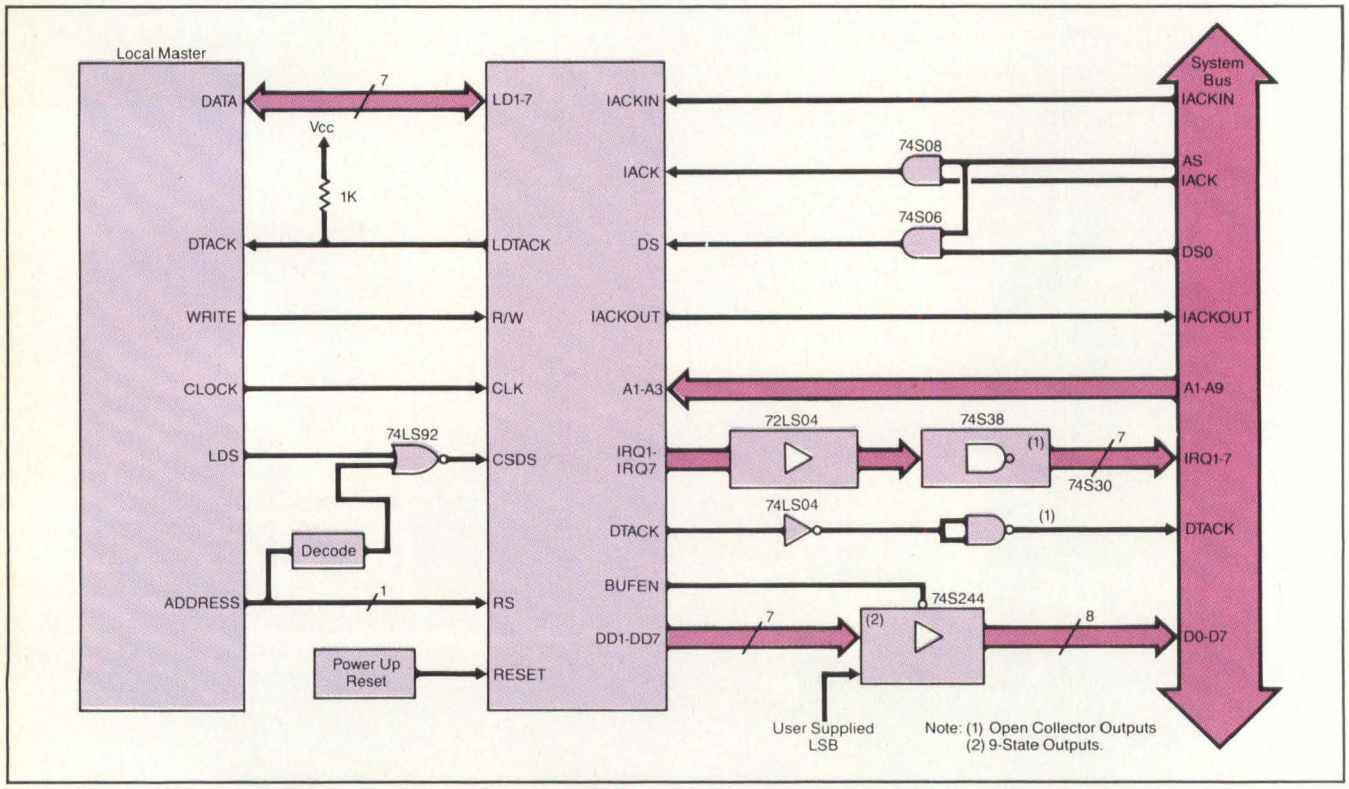

Figure 4: Typical system configuration for the Signetics 68155 asynchronous interrupt handler.

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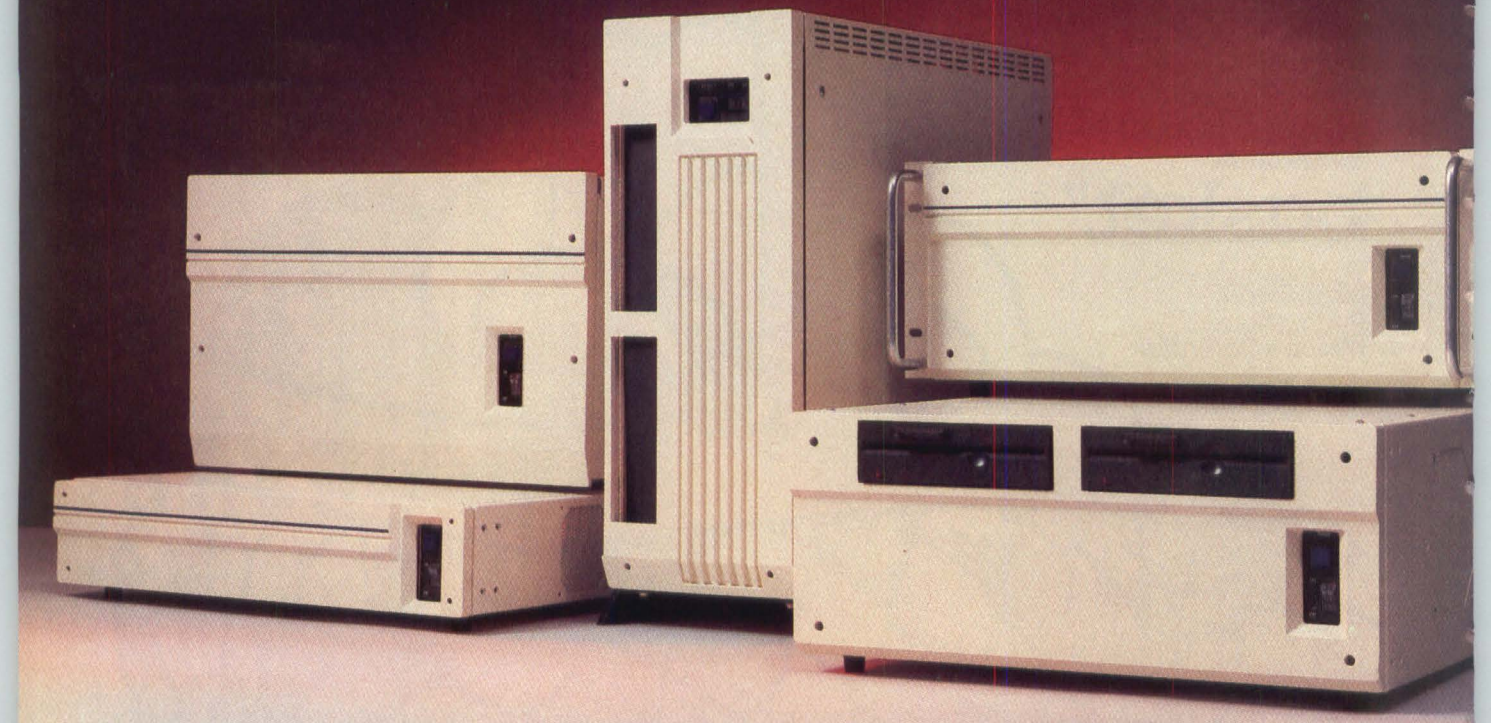

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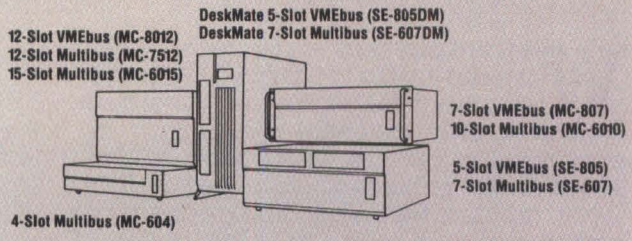

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Little Drives That Can

by Bob Hirshon, Contributing Editor

Sub-4″ mass storage devices, like this Winchester drive from Hewlett-Packard, pack large amounts of memory into a little space.

Mass memory devices fitting the 3½″ form factor have emerged to fill the demands of designers who need to get the most out of every cubic centimeter.

Engineers designing systems for space-constrained applications ask a lot of their mass storage devices. Disk and tape drives for such applications must pack nearly as much data as standard-sized drives with far more recording surface area. They must use less power than standard-sized drives. They must cost less since the total cost of the final system will probably be low. They must withstand far greater thermal stress since they will be installed in a tight spot with little space for heat dissipation and, if the system is portable, they may travel from a freezing car to a warm office. And they will be expected to withstand extreme shock and vibration—even though standard-sized drives have been known to crash as a result of doors slamming several offices away.

Over the past year, the number of companies building drives to meet these demands has grown considerably. Today, a variety of flexible disk, magnetic tape and rigid disk drives are available that fit the sub-4″ form factor.

Common Requirements For Portability

Sub-4″ drives are increasingly being used in such portable applications as transportable computers, portable test equipment, data logging and consumer electronic devices. In addition to small size and low weight, certain requirements are common for all of these applications: resistance to shock and vibration, low power consumption, high tolerance to temperature varia-

Bob Hirshon, Contributing Editor, Peripherals, for Digital Design, *is a Boston-based science writer.*

tions and low cost.

Physical dimensions. Although most drives claiming to fit the 3½" footprint have the same faceplate dimensions set by Sony's (Park Ridge, NJ) current microfloppy drive – 1.625" × 4" – there are exceptions. Hewlett-Packard's (Greeley, CO) Winchester follows Sony's original microfloppy footprint which was 2" × 4". Winchester drives from Rodime (Boca Raton, FL) and SyQuest (Fremont, CA) use sub-4" media, but overall drive width is larger than the Sony standard footprint because the drives were introduced before the Sony footprint was adopted as a *de facto* standard.

Some microfloppy drives are actually slimmer than the standard form factor and have larger bezels available for applications where they must fit an existing standard footprint. Finally, it is important to remember that published drive dimensions often exclude control electronics and shock mounts.

Shock and vibration tolerance. Resistance to shock and vibration is of particular concern for rigid disk drives operating in a transportable environment. Fortunately, merely downsizing the drives helps make them shock resistant. Short R/W head armatures are resistant to torque and vibration stress, as are the smaller platters and the drive shell.

Low mass heads and sliders are also more tolerant to shock and vibration. Plated or sputtered media resists damage during head/media contact. If oxide disks are used, a dedicated landing zone or, even better, retractable heads minimize damage.

Most transportable applications also require some form of shock mounting. Depending on the amount of isolation required, this can add considerably to the drive's dimensions since substantial sway space may be necesssary for the shock mounts to function effectively.

Winchester drives vary greatly in the amount of shock mounting they require to achieve their published specs. Hewlett-Packard claims that their sub-4" Winchester drive needs no shock mounting. Others provide so much sway space that the drives may take up more room than a 5¼" Winchester (but presumably provide far more shock resistance).

Especially with Winchesters, shock and vibration specifications should be viewed skeptically. "Anyone can print '40 Gs' on a spec sheet," says Alan Shugart, President of Seagate Technology (Scotts Valley, CA). "Whoever has the newest brochure has the best specs."

Power requirements. Power consumption is a major concern in most portable applications. Most sub-4" memory devices keep power consumption down by use of CMOS components. In addition, they inherently require less power because they use smaller disks or less tape; and the drive motors, which account for most of the power consumption, are correspondingly smaller. Tape drives draw the least power, ranging from a low of under 2W to 10W. Microfloppics require from 3W to 10W, and sub-4" Winchesters can draw up to 15W for multiplatter models.

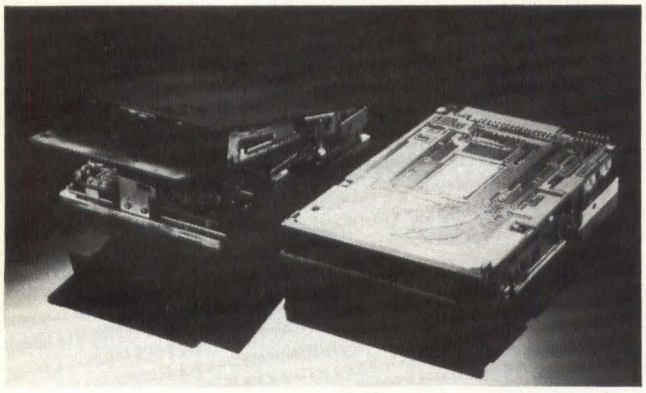

Figure 1: Citizen offers their slim, 1" high microfloppy drive in a top-load configuration.

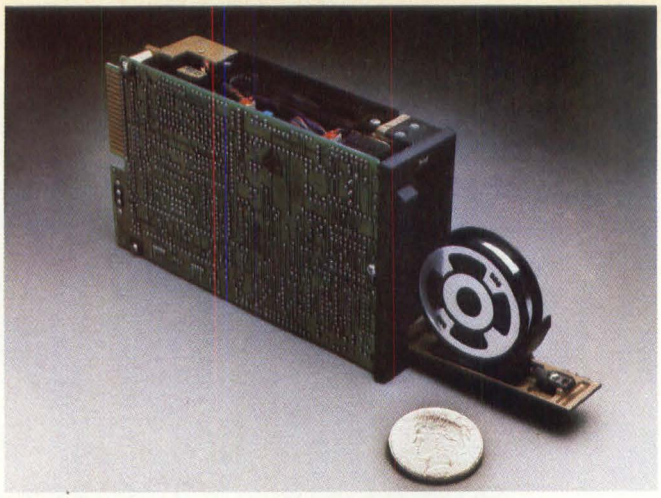

Figure 2: Interdyne's 3½" footprint tape drive stores 20 Mbytes on a 2¼" reel of quarter-inch tape.

Thermal considerations. While most mass storage devices can count on relatively stable operating climates, tolerance to extreme thermal changes is a necessity for sub-4" mass storage devices that travel out of the office. Read/write errors or data loss due to thermal off-tracking is the primary concern.

The solution is either to be extremely conservative at the head/media interface (writing wide and reading narrow) or to use a servo positioning system to actively keep the heads on track. The conservative approach means lower capacities because of lower data densities. The servo approach allows high densities, but also adds expense and complexity.

Cost. Target applications for sub-4" tape and microfloppy drives are frequently systems with a total cost of under $1500. Those using sub-4" Winchesters may cost only a little more. Therefore, there is little demand for "premium" micro drives. All of the problems associated with downsizing the drives and designing them to withstand the rigors of a mobile environment must be accomplished as cheaply as possible, with special attention given to low cost, high volume production. As a result, there is a considerable gap between what is technologically possible and what is actually available.

Microfloppy Disk Drives

After several years of industry wrangling, Sony's 3½" microfloppy has emerged as the industry standard. Even though the media and the drives have undergone so many refinements that today they bear little resemblance to those originally introduced by Sony, the 3½" diskette diameter remains unchanged. With the support of Hewlett-Packard, Apple and IBM, microfloppy disk drives using other sized media are destined for decreasing niche applications. Now that the dust has settled, both media and drive manufacturers can gear up for volume production, which will be essential to the success of microfloppies.

Production Moves Off-Shore

With the departure of Shugart from the market, Tandon (Chatsworth, CA) remains as the only large US-based manufacturer

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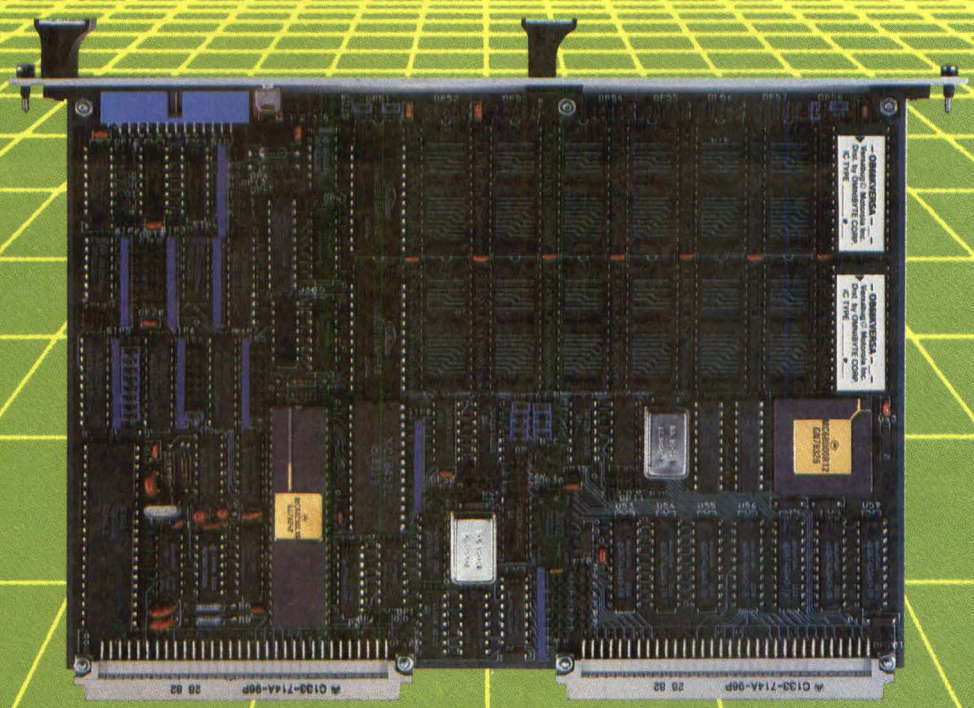

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of microfloppy drives. Japan has always dominated the market based on Sony's lead. But today the entry of other large volume foreign manufacturers has all but eliminated the US. In 1984, manufacturers not based in the US accounted for 97% of all microfloppies shipped, according to Disk/Trend (Los Altos, CA), a market research firm specializing in mass memory. The completion of large microfloppy drive production facilities in Japan indicates that Japan should continue its dominance of this market for the foreseeable future.

Small Differences

The lack of distinguishing characteristics among microfloppy drives shows that standardization has finally taken hold. Designing a drive to fit a standard footprint, using a standard interface with a standard, interchangeable media, all at the lowest possible cost, doesn't leave much room for innovation. However, there are a few small exceptions.

For applications in which space is more important than a standard footprint, several microfloppy drive manufacturers build low-profile low-weight drives. JVC (Elmwood Park, NJ), Citizen (Santa Monica, CA) and others offer drives just over 1" in height (rather than the standard 1.625") and weighing a little over one lb. Where size and cost is even more critical, and capacity and interchangeability are not, Tokyo Electric Co. (Tokyo, Japan) offers a 2½" microfloppy that records up to 64 Kbytes on a single spiral track.

Citizen offers a top loading, rather than front loading, version of its microfloppy (**Figure 1**). And Au Peripheral Products (San Jose, CA) has a microfloppy drive that it claims offers recording characteristics superior to those of the big company drives, at a comparable price. President Sik-Kee Au, formerly with IBM, hopes to offer an alternative to the mass produced drives imported from overseas.

Microfloppy Trends

Last year, microfloppy disk drives accounted for more than 10% of all floppy disk drives sold, according to Disk/Trend. By 1987, they should account for more than 30% of all drives shipped.

Thus far, most of the microfloppies have been single-sided drives, but double-sided, 1-Mbyte microfloppies are now becoming available and will account for an increasing number of the sales. This year drives with 1.2 Mbytes of formatted capacity should be announced. The media supply is beginning to catch up to demand and should bring prices down. Low cost, readily available media will go a long way in helping microfloppies compete effectively against 5¼" minifloppy drives.

Figure 4: Newbury Data's four-platter Penny Winchester is the first 50-Mbyte 3½" Winchester.

Figure 3: Tallgrass Storage Devices, like Irwin Magnetics and APTEC, now offers minicartridge tape drives for OEMs. The Grasshopper currently uses 3M's DC1000 minicartridge and will accommodate the quarter-inch tape DC2000 minicartridge when it becomes available later this year. This will allow a capacity of 40 Mbytes.

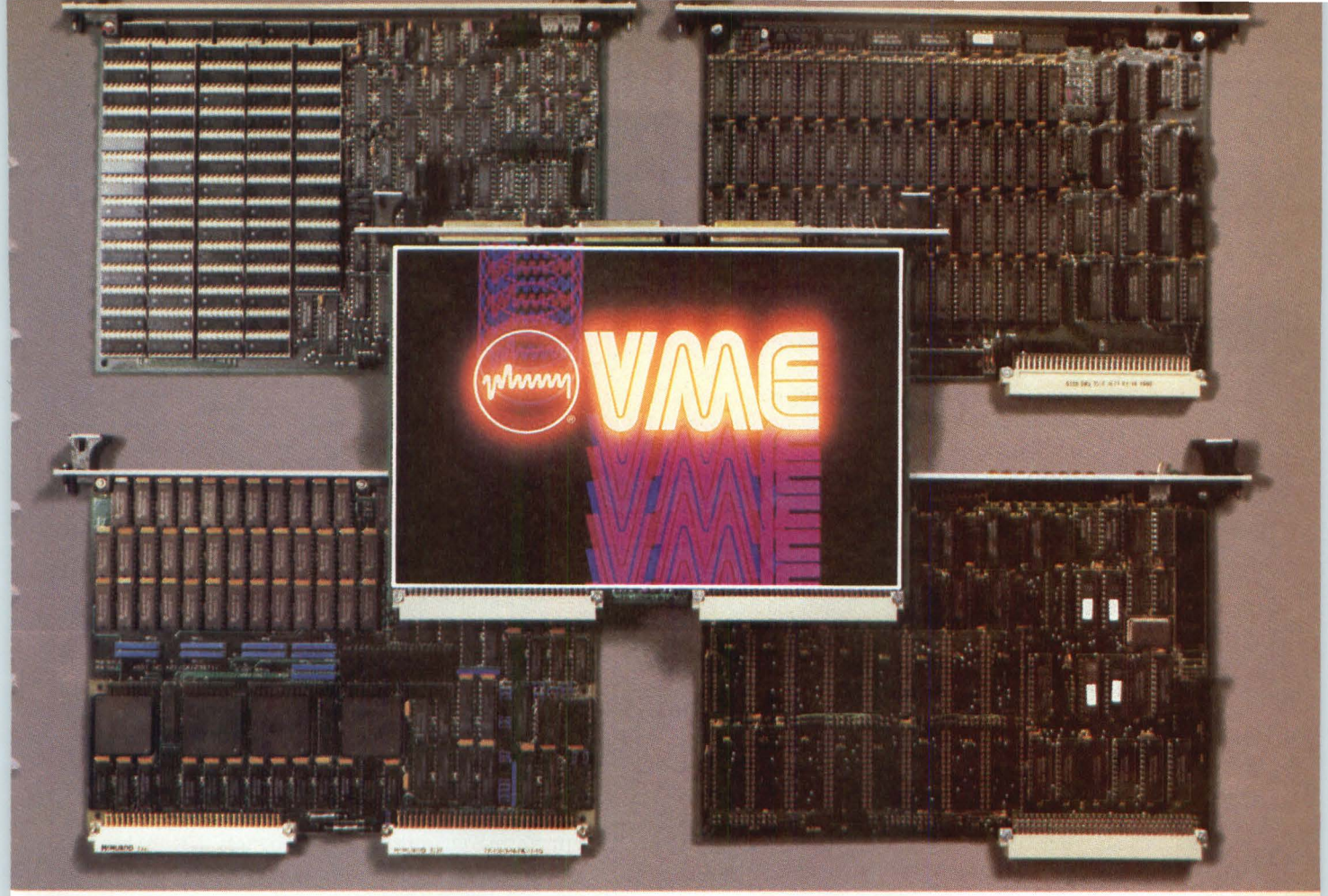
Sub-4" Tape Drives

There are a number of tape drives fitting into a sub-4" footprint. They may use minicartridge media, cassette (also known as miniature reel-to-reel) media or drive-unique media. For applications that don't require fast access times, such as data recording devices, some test equipment and very low-end computers, they may serve as primary data storage devices. However, they more commonly provide removable, back-up mass storage for Winchester drives.

Minicartridge drives. Minicartridges were developed by Hewlett-Packard 10 years ago and then licensed to 3M (St. Paul, MN). Dubbed the DC100, they were scaled-down versions of 3M's DC300 quarter-inch tape cartridge and were used extensively by HP and DEC in their intelligent terminals, small computers and test equipment. They contained 140' of 320 oersted and .15" wide tape, and capacity was under 1 Mbyte.

In 1979, Irwin-Olivetti built a 5¼" Winchester drive with a built-in DC100 drive for back up. The Irwin DC100 drive had 5 Mbytes of formatted capacity. When Irwin-Olivetti became Irwin Magnetics (Ann Arbor, MI), they left the Winchester business and focused exclusively on the DC100 tape drive.

Last summer 3M announced the DC1000, a DC100 with 185' of 550 oersted tape, which allows capacities of 10 Mbytes or more. More recently, 3M announced the DC2000, using quarter-inch tape in the same minicartridge shell, which allows capacities from 20 Mbytes to 40 Mbytes. As a result, other companies have joined Irwin in making minicartridge tape drives, and many more are eyeing the market.



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Ironically, Hewlett-Packard, who used the minicartridge extensively when there was little outside interest in it, has moved slowly away from the media and now appears ready to phase it out in favor of the standard DC300/600 quarter-inch cartridge. "They're basically stretching right now to get 10 Mbytes on a DC1000," explained Frank Carew, R&D section manager for HP's tape activities. "So our focus is on the larger cartridge. We're hesitant to commit to devices that are 20 Mbytes or less."

Meanwhile a number of companies are anything but hesitant about developing drives for the DC1000/2000 media. One reason is that the minicartridge, unlike the standard quarter-inch cartridge, is small enough to fit into a sub-4" form factor. Some companies believe it will be the ideal back-up companion for sub-4" Winchester disk drives.

In addition to Irwin Magnetics, APTEC (Columbia, MD) and Tallgrass Storage Devices (Boulder, CO) are currently offering minicartridge tape drives. And some manufacturers of DC600-based tape drives are planning to introduce minicartridge drives. Therefore, the Quarter-Inch Cartridge Working Group (QIC), a committee consisting of company representatives dedicated to developing standard recording formats and interface specifications for DC600 cartridge drives, spun off a sub-group to work out standards for DC1000/2000 drives. A standard spec would, in theory at least, allow media interchange between drives from different manufacturers. Despite Frank Carew's contention that current drives already push the capacity limits of the media, the QIC group plans on packing 40 Mbytes onto a single minicartridge.

Cassette drives. Another group working on a 40-Mbyte standard spec for a sub-4" form factor tape drive is D/CAS. The media is a slightly modified audio cassette, manufactured specifically for data storage use. The companies currently involved are Memtec, (Salem, NH), Raymond Engineering (Middletown, CT), Braemer (Burnsville, MN), Teac (Montebello, CA) and Verbatim (Sunnyvale, CA).

Capacity is less of a problem for cassette drives because cassettes contain about twice the recording area of a DC1000 minicartridge and about 50% more area than a DC2000. Memtec announced a 40-Mbyte 5¼" half-height drive two years ago and has been shipping them in quantity since last fall. The delay in a 3½" form factor version is more a result of a slowly developing market than of any technical difficulties. Cassette drives would seem to be ideally suited to 3½" Winchester back-up applications, and media is already available from Verbatim.

Drive-unique media. Why would a tape drive manufacturer build a drive that uses nonstandard media? "We control our destiny because we have the design of both (drives and media)," explains Frank Gilovich, Chief Executive Officer of Interdyne (Van Nuys, CA). "The Irwins and the Memtecs are controlled by somebody else." Interdyne's 3½" form factor ID1000 (**Figure 2**) uses 2¼" reels of quarter-inch tape to store up to 20 Mbytes of data. A future version of the drive uses half-inch tape to store 40 Mbytes.

"Everyone's talking about standards," says Gilovich. "There's really only one true tape standard, and that's IBM machines that are single reel, self-threading and fixed head. And the reason it's a standard is that it's very easy to interchange." Interdyne's drive is also single reel, self-threading and fixed head and, presumably, easy to interchange. To ease OEMs' concerns about supplies of the media, Interdyne recently licensed Shape (Biddeford, ME), a leading manufacturer of video tape cassettes, to produce the Interdyne tape reel.

Figure 5: Miniscribe's new sub-4" Winchester stores over 200 Mbytes of formatted data.

Entrepo (Sunnyvale, CA) also produces a small footprint tape drive with unique media. But while Interdyne looks to 40 Mbytes, Entrepo builds drives storing 256 Kbytes on a "microwafer." They plan to undercut low-end floppy drives, providing slightly less capacity and much slower access time but at a third of the price. Target applications include low-end personal computers and intelligent typewriters. OEM price of the drives is between $20 and $30.

Sub-4" Winchesters

Available from over a dozen manufacturers and ranging in capacity from 10 Mbytes to 50 Mbytes, sub-4" Winchester drives have finally moved from the drive designers' drawing boards to the systems designers' drawing boards. This year the results will become apparent as a new crop of personal and portable computers are announced sporting the sub-4" drives.

Most of the sub-4" Winchester makers cite ruggedness as the chief advantage of their drives, but few demonstrate it quite as graphically as Hewlett-Packard. To illustrate their 10-Mbyte drive's tolerance to shock, they attach the drive to a chain and enclose the drive in a plastic box. Potential customers are invited to pull on the chain while the drive performs data seek operations. "I think most people were impressed," says Rex James, HP's operations manager for Winchester activities.

The HP drive stays on track by means of servo information interleaved in each sector, "not just a wedge servo, with information once around the track," explains James. The hard sputtered media, which HP makes itself at its Boise, ID factory, coupled with light minimonolithic R/W heads, prevents damage to the recording surface.

HP offers just a mechanics-only drive. They chose not to incorporate a standard ST506 interface, and the drive has a transfer rate of 4 Mbits/sec, rather than the ST506 standard 5 Mbits/sec rate. Their target customers must be willing to build their own controllers, or buy them from a third party. Adaptec has worked with HP to develop a SCSI controller for the drive.

"We're talking to a number of people who are willing to design their own controllers with unique interfaces on their internal buses, and for them the ST506 interface is not a prerequisite," says James. "Quite frankly, there are other people that we have talked to that would very much like to have a 506," he adds, "and, we aren't providing that."

Avoiding the ST506 interface makes the drive family easier to upgrade and, ultimately, allows systems integrators to develop a less costly mass storage subsystem, according to James. "We left the interface on the Winchester such that it did not require a microprocessor on board. . . .Then a high level controller

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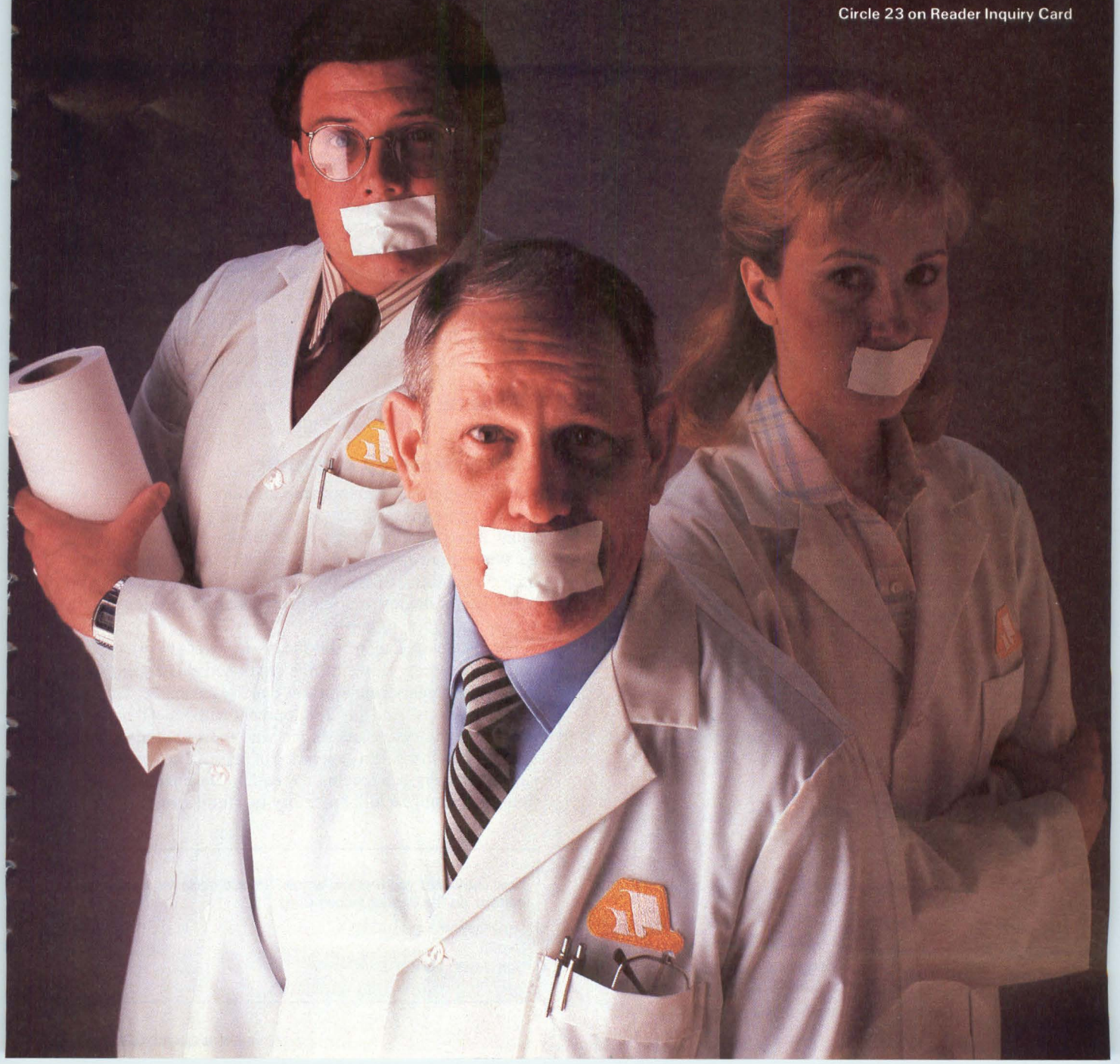

could be used, for instance SCSI, which uses a single microprocessor and controls both the interface and the drive itself, therefore, providing a lower system integration cost."

Upgradability was also a key reason to avoid the ST506 interface. "As we develop future drives," explains James, ". . .that will improve capacities from 10 to 20 to 40 to 80 Mbytes, we can stay with that same high level controller and not have to redesign that interface in the system."

Newbury Data (Staines, Middlesex, England; Woburn, MA) has a somewhat different approach with its 3½" Penny drive. It stores 50 Mbytes, unformatted, on four plated disks and has an average access time of 40 msecs. Aimed at less sophisticated OEMs, the drive uses a standard ST506 interface. Newbury Data also offers mounting kits for installing the drive into a half-height or a full-height 5¼" Winchester footprint. In all, Newbury Data has done everything to make their drive easy to integrate with a minimum of effort.

Drives from the major domestic Winchester manufacturers also use the ST506 interface, but have far lower performance and capacity than the Newbury drive. Seagate, Tandon, Miniscribe and others all offer low cost drives targeted at the high volume needs of the major OEMs.

Although they historically haven't competed effectively in the small Winchester market, Japanese drive manufacturers also are looking at the 3½" market. Hitachi (Torrance, CA) and Nippon Peripherals (Kanagawaken, Japan) have already introduced competitive products into the US market; NEC (Boxborough, MA) and others will join them soon. Bruce Thatcher, Director of Marketing for NEC Information Systems' Peripheral Products division, predicts that beginning in 1986, the 5¼" market will slowly decline to a million units annually, and 3½" disks will rise to 2.75 million units annually. In addition, he forecasts that OEM prices for 3½" drives will drop steadily during this period – to $180 from $380.

Micro-Memory Outlook

For all types of sub-4" mass storage products, the next year looks good for systems designers and difficult for drive designers. Many drive manufacturers – both foreign and domestic – see the sub-4" drive market as crucial to their future. They are determined to establish themselves in the market, no matter what it takes. This is already resulting in price wars in a market that isn't yet big enough to fight over.

For systems designers, this means drives at low prices, from multiple sources. However, the continued existence of those multiple sources depends on how quickly the market for sub-4" drives develops. And any development will depend on the ingenuity of the systems designers and their ability to exploit sub-4" drives in the next generation of personal computers, portable computers, subsystems, test equipment and other applications that require a lot of memory in a little space. **DD**

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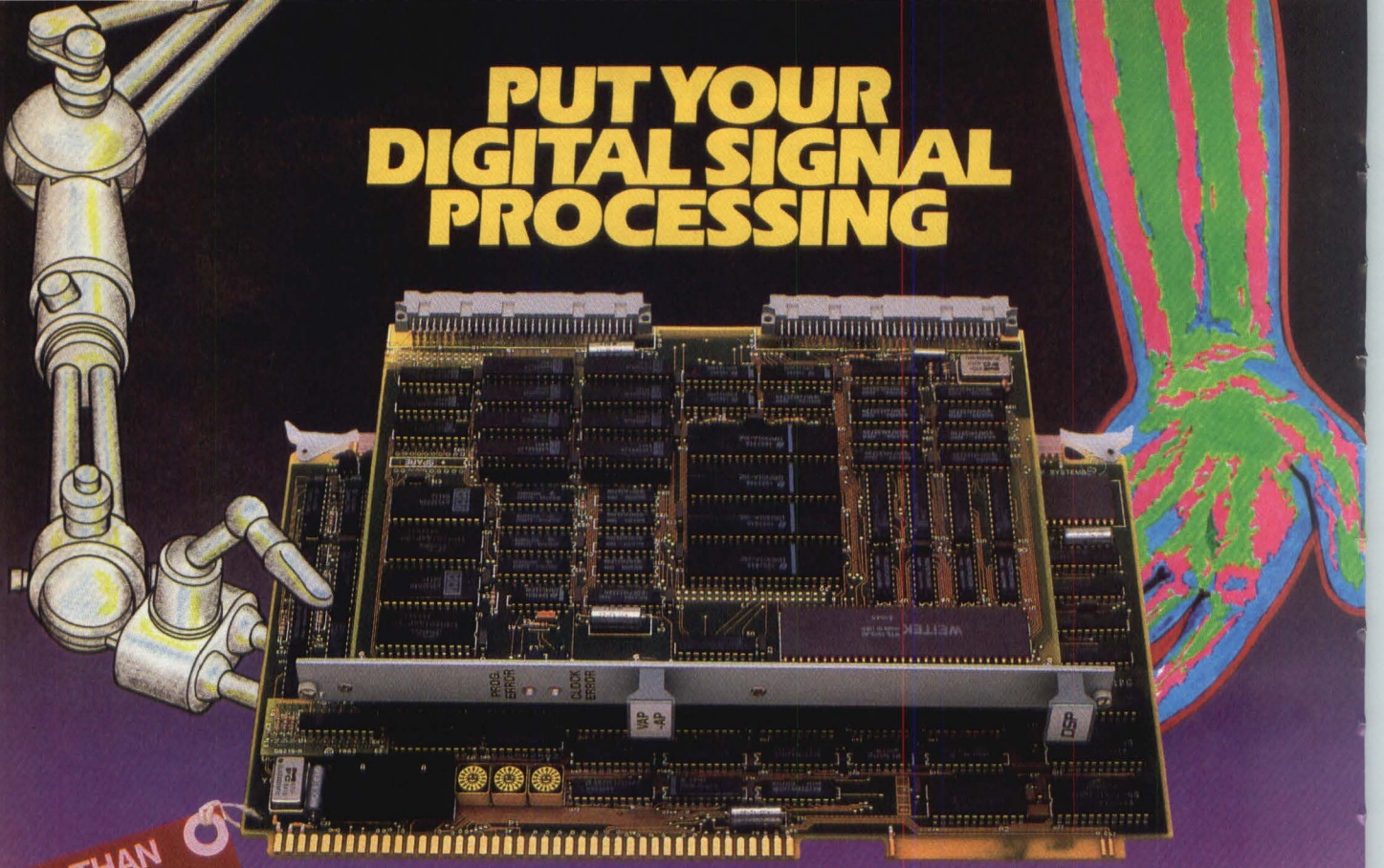

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Graphics Architecture — New ICs Promise Better Performance

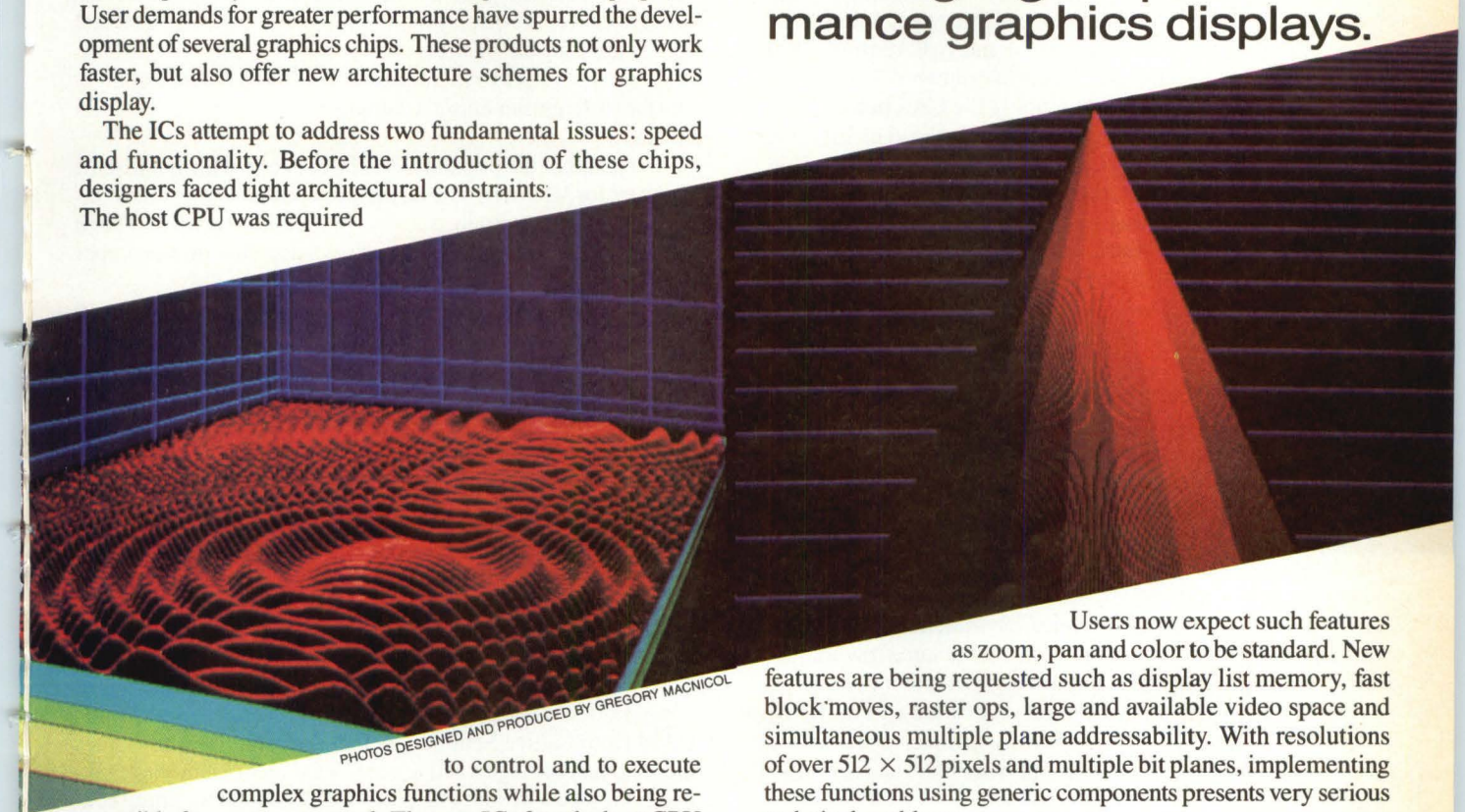
by Gregory MacNicol, West Coast Technical Editor

Driven by user demands for faster, smaller, more capable and less expensive computer graphic systems, semiconductor manufacturers are introducing chips that provide rapid bit-mapped medium to high resolution displays. Until recently, the low resolution home/game computer market was the primary volume market for chips aimed at graphics. User demands for greater performance have spurred the development of several graphics chips. These products not only work faster, but also offer new architecture schemes for graphics display.

The ICs attempt to address two fundamental issues: speed and functionality. Before the introduction of these chips, designers faced tight architectural constraints. The host CPU was required to control and to execute complex graphics functions while also being responsible for memory control. The new ICs free the host CPU from graphics functions and avoid memory contention problems. The result is much faster graphics systems capable of true graphics interactivity.

Technological developments are not the only factor in the increasing quality of graphics systems. Dropping memory costs and availability of high quality, inexpensive RGB monitors are also contributing factors. Monitors with resolutions of over 1024 × 1024 pixels previously were expensive and poor quality. Now there are more manufacturers, and many offer display resolutions of over 2000 × 2000.

Dedicated graphics chips are inviting better and faster architectures for creating higher performance graphics displays.



PHOTOS DESIGNED AND PRODUCED BY GREGORY MACNICOL

Users now expect such features as zoom, pan and color to be standard. New features are being requested such as display list memory, fast block moves, raster ops, large and available video space and simultaneous multiple plane addressability. With resolutions of over 512 × 512 pixels and multiple bit planes, implementing these functions using generic components presents very serious technical problems.

A major problem with graphics architecture is the video refresh rate. The video refresh controller must supply data to the video output hardware where the pixel display time is less than the memory cycle time in video output hardware. Video refresh rate is closely tied to memory bandwidth. The use of faster memory chips solves the problem but means higher component costs. The next problem is the ability to read, modify and write to display memory without contention problems or update speed loss. Demanding applications increase the architectural problems in today's graphics systems.

Memory

Memory has been and still is the key issue in graphics systems. Memory used for graphics applications is different than conventional computer memory. The issue is not just one of speed, cost and size, but how the memory is used architecturally. The memory organization controls performance through such factors as the relationship of memory speed to display update/refresh bandwidth, memory size, organization and overhead requirements. Despite the declining cost of memory over the last few years, price, as well as availability and organization of memory, is still a critical issue.

A fundamental problem in bit-mapped displays is that pixel generation occurs during refresh requiring a high memory bandwidth. Memory bandwidths of 100 MHz or more are common in medium to high resolution systems and at this rate, bandwidth requirements are too high even for static RAMs. The problem is further compounded at higher resolution. External buffering, blanking (flash mode) or unusual retrace periods also burden bandwidth.

Novel schemes have been devised for graphics applications to help solve some of the constraints. Some of the solutions are based on standard DRAMs with special fast cycles. Inmos (Colorado Springs, CO), for example, integrates a $\overline{CAS}$ before $\overline{RAS}$ into their line of 64K DRAMs. Texas Instruments' (Dallas, TX) new 256K DRAM family can employ the $\overline{CAS}$ before $\overline{RAS}$, $\overline{RAS}$ only refresh or hidden refresh cycling. Other solutions rely on video bus exchanges, bus arbitration or cycle stealing. Fast static RAMs are sometimes used as a solution in spite of their expense. The Metheus (Hillsboro, OR) 2500 series of display controllers, for example, uses 70 nsec static RAMs for display memory. Another alternative is double buffering where two separate display planes are used, one for display and the other for writing. However, this scheme means the cost of twice the display memory.

Approaches such as nibble mode and static column addressing are sometimes used. Static column decoding is an access mode that eases the raster display bandwidth problem by providing high speed access to a serial bit stream. The fast access also allows cycle stealing so that a pixel processor can "steal" random update cycles during display time as well as during blanking intervals. Static column addressing used with an optimized memory technique called symmetrical cell addressing allows better update performance. Symmetrical addressing assigns a rectangular area of the screen to the same row address, rather than organizing the RAM row addresses along scan lines.

TI introduced a memory chip last year called a Video RAM, or VRAM (**Figure 1**). The TMS4161 is unique because it was specifically designed for graphics applications. The dual-ported nature of the TMS4161 allows a graphics processor to control the DRAM portion of the device. Pixel data for refresh display is provided through the use of an on-board 256-bit shift register. The combination of shift register and 64K × 1 RAM significantly reduces costs and parts count while supporting pixel clock rates from 5 to 150 MHz. TI claims that using the chip in a 1K × 1K black and white system would reduce parts count by 72 chips (48 memory and 24 logic) using 16K × 1 chips. Chip reduction using 16K × 4 chips would be 24 chips.

An application note from TI describes a 640 × 480 display where five devices per pixel plane are used. One approach uses external parallel to serial registers for each plane, whereas another approach uses the 256-bit serial shift register to link the ICs of each plane together. Use of the TMS4161 allows almost 100% access to the display memory for updating. An additional use of the 256-bit shift register is the clearing of a display. Loading the VRAM's memory with 256 0s and loading them into the shift register erases a complete screen image in only 255 cycles.

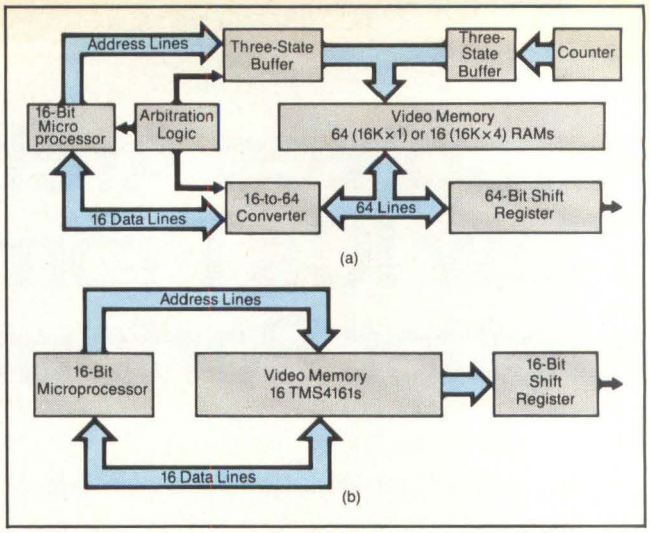


Figure 1: Use of Texas Instrument's VSC in conjuction with their dual-ported 4161 VRAM reduces parts count of a conventional graphics display system. Here the VSC/VRAM is composed with 64K × 1 and 16K × 4 DRAMs.

As a result of the popularity of the concept of on-board shift registers for VRAMs, several memory manufacturers have announced plans to introduce their own versions soon. The TI unit will probably have variations, such as a decrease in the number of tap lines in the shift register.

Although it may seem better to use larger memories such as the 256K × 1, they also have bandwidth problems. 256K × 1 DRAMs can store a 1024 × 1024 pixel display, but all the data cannot be accessed from them in time to support the dot rate of 12 nsec. Thus, graphics designers prefer nibble mode where data can be read in ×4 increments.

An additional, but often overlooked, aspect of graphics architecture is the power supply for the massive amount of RAM. Although static RAMs use more power than dynamic RAMs, dynamic RAMs must be refreshed. The amount of inrush current required to refresh Mbytes of memory can easily cause a strain on marginal power supplies and can cause the display system to oscillate audibly.

Many manufacturers have developed parts that reduce power consumption while increasing speed. A 35 nsec 16K × 4 static RAM from Lattice Semiconductor (Portland, OR) consumes only 100 mA during its active state. NEC (Mountain View, CA) has developed a memory chip that is able to hold the entire contents of a video display. The μPD41221 DRAM uses a 75 nsec serial access scheme to store 320 rows of 700 columns (224,000 bits). Because of its unusual organization, the memory requires 320 refresh cycles every 2 msec. This refresh rate allows from 1 to 700 bits to be shifted in a single scan period. Additionally, it has a counter which can be set, reset, incremented and decremented.

VLSI Graphics Display Controllers

Ever since the introduction of the 7220 from NEC in 1981, graphics display controllers have made a major impact in the

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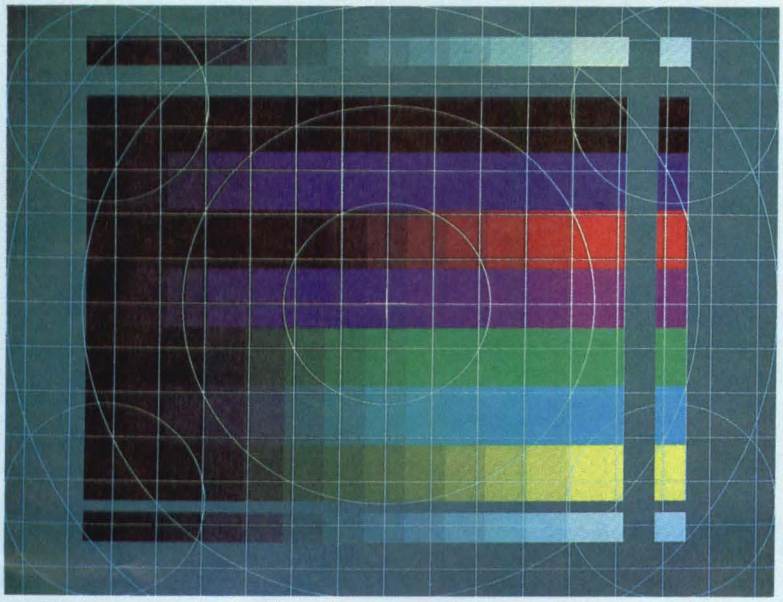

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- Dot patterns
- Cross-hatch patterns
- Window patterning functions

← This is a sample display frame generated using the VG-807A. It shows the superimposition of circular patterns, cross-hatches, horizontal color bars, vertical gray-scale patterns, a center marker, and six windows on a gray background plane.

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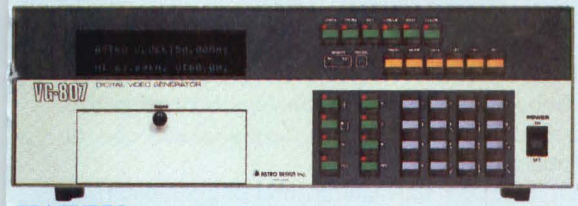

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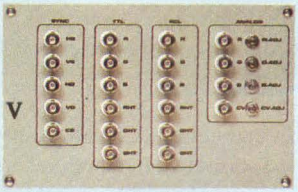

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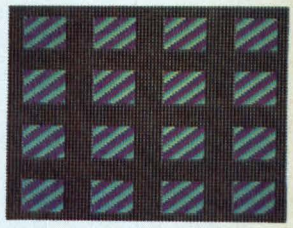

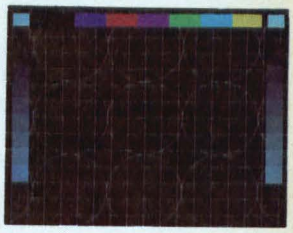

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graphics market. Over 40 companies depended on the 7220 for their graphics display systems last year. The 7220 is second sourced by such major firms as Intel, with its 82720, and Thompson-EFCIS, with its 9367. The success of the 7220 confirms the validity of using a VLSI chip to centralize and to control graphics functions.

Some of the target goals of the next generation of display controllers are implementations of graphics standards, use of the 16 basic logical operators (AND, XOR), raster operations, programmable transparency of the background, windows with management and high speed control of pixel data to and from the frame buffer. Several IC manufacturers are presently developing products that will support many of these functions.

A chip set from NCR (Colorado Springs, CO) and a set from Hitachi (Tarrytown, NY) represent the second generation of graphics controllers. The NCR 7300 Color Graphics Controller (CGC) works with the 7301 Memory Interface Controller (MIC) to form the basic blocks of an intelligent graphics system (**Figure 2**). Central to the performance of the chip set is the ability to translate high level graphics commands into machine language instructions. Additionally, the set can perform fast block transfers with raster ops, such as read-modify-write, being executed during display transfer. Memory management, DMA, cursor control, internal color look up table and analog RGB outputs are provided in the 7300, allowing display of 256 simultaneous colors. The system is designed to incorporate such graphics standards as CORE, GKS and NAPLPS. The architecture helps programmers by providing control of the memory refresh, window management and soft font text generation.

The Raster Memory Controller (RMC) and the Raster Memory Interface (RMI), both from Motorola (Phoenix, AZ), have features that are intended for low-cost systems. The chip set can display 320 × 210 pixels with 16 displayable colors in the NTSC format. The RMC can display eight sprites (bit-mapped blocks) and can provide smooth scrolling, alphanumerics and memory control.

The Advanced CRT Controller (ACRTC) from Hitachi performs such advanced graphics functions as drawing of primitives, split screens and windows, clipping and X-Y addressing (**Figure 3**). The X-Y addressing must be computed by the processor for each pixel using other architectures; this takes up valuable time. The 8 MHz unit can draw up to 2 million pixels per second. The controller is comprised primarily of three processors: the drawing, the display and the timing processors. Other functional blocks such as the CPU interface, DMA and interrupt controller and CRT interface constitute the support circuitry. The drawing processor interprets commands into the physical pixel addresses. The display processor controls the screen format and display parameters for driving the display. The timing processor controls the internal timing in the chip, as well as the correct timing for the display. The chip is unusual because it has independent 8-bit read and write FIFOs for transferring main memory to display memory. This lessens bus traffic contention during data transfer and increases speed.

A recent trend is the use of chips that provide specialized functions. For example, the new TMS32020 chip from TI is designed for signal processing and is excellent for specific arithmetic problems. The TMS32020 supports 3D rotation which requires scalar-to-vector conversion in real time. Normally this floating point calculation is done on the host microprocessor.

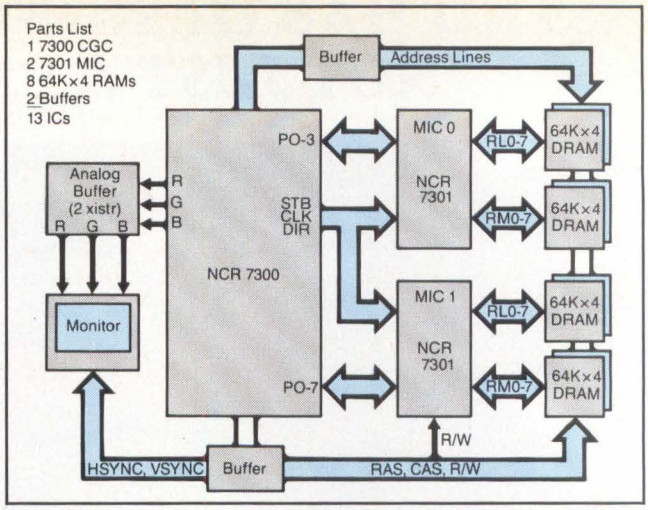


Figure 2: The NCR graphics chip set is an example of the VLSI approach to graphics architectures. A 16-color 640 × 640 pixel system having a 1024 × 512 frame buffer is shown using a 7300 and two 7301s. The only other components required are the TTL buffers for address on control of RAM and the analog drivers.

The architectures of the latest graphics controller chips make it clear that the industry is supporting bit-mapped displays rather than table-look-up graphics and text. Bit-mapped displays represent exactly what is in memory on the display.

CPU Vs. Bit-Slice

A major influence on the speed of graphics systems has been the implementation of bit-slice architectures. The ability to efficiently microcode wide-word architecture outweighs the problems encountered in programming unusual and untested code. Programming time is much longer with microcode than with conventional languages having good support tools. Raster Technologies has taken the bit-slice approach, as has Metheus. They use the AMD 2900 series of bit-slice chips and support circuitry. In addition to using bit-slice technology, both companies use generic microprocessors such as the 68000 and Z80 for general I/O management.

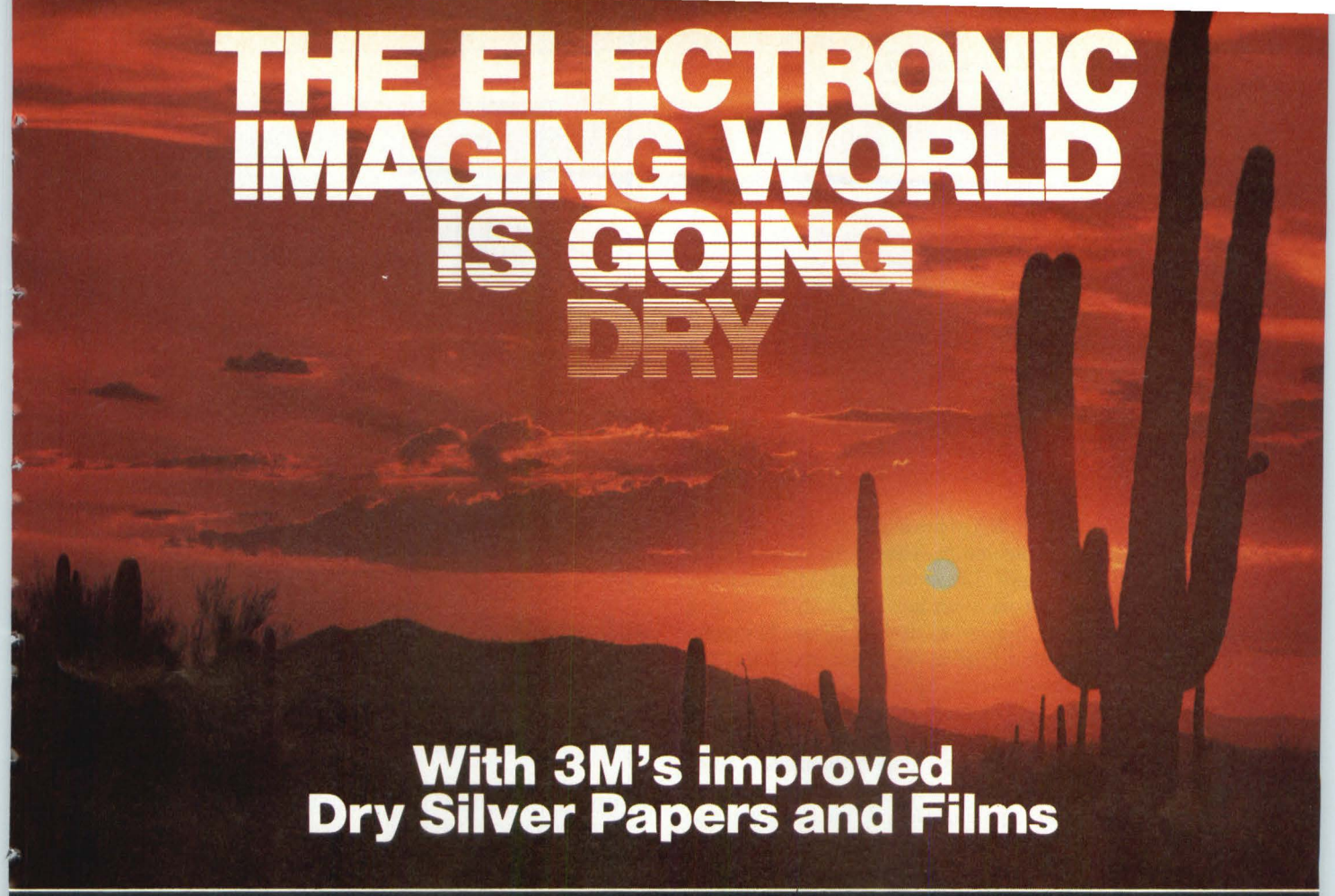
Qubix (San Jose, CA), the manufacturer of a computerized technical publishing system, chose to use a distributed function architecture consisting of multiple 68010s for their 2240 × 1680 × 1 pixel display. Using dual-ported RAMs, the 64K × 64 bit bit-mapped system runs at a clock rate of 155 MHz. By scanning in 64-bit raster words, the system operates on only 1/64 of the clock rate, which is about 2.2 MHz.

Parallax (Sunnyvale, CA) uses a different approach. The bit-slice architecture is not implemented by commercially available bit-slice CPUs but through the use of discrete TTL. The versatility gained by this architecture on their 1000 Series of board level products allows a drawing speed of 88 million pixels per second at a resolution of 1024 × 768 pixels, 60 Hz, noninterlaced. The vector draw rate is 1 million pixels per second. Use of Programmable Logic Arrays (PLAs) and simulation before construction makes the design efficient and well tested.

Several companies are now using AMD's newer 29116 series of bit-slice devices. The 29116 combined with the AMD 29516/517 16 × 16-bit multiplier makes possible multiple intensive rotation algorithms in 65 nsec per multiply.

Going Custom

The problems encountered in determining what to load in the bit map has led several system architects to seek alternatives to



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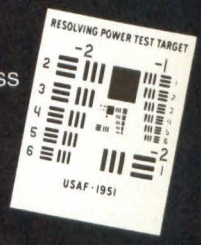

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relying on a host CPU or commercially available products. Sun Microsystems (Mountain View, CA) incorporates the concept of RasterOps which allows rectangular areas of raster display data to be modified according to a preselected operation. This concept grew from the early days of Smalltalk and was implemented on the Xerox Alto computer as BitBlt, for Bit Boundry Block Transfer. The function is now implemented on a custom VLSI chip created by a silicon compiler. The design of the chip at Silicon Compilers (Los Gatos, CA) took only five months and replaces about 80 TTL packages. The chip uses a 16-bit data path and can handle 256 functions, including all bitshifts and bitmasks. It is now manufactured and sold by VLSI Technology (San Jose, CA).

Xtar (Elk Grove Village, IL) offers a two-chip set that computes the pixel-by-pixel calculations for drawing into the frame buffer quickly. The Graphics Microprocessor (GMP) is a 16-bit processor designed to work with the Video Shift Register (VSR), which controls 16K × 4 DRAMs. Xtar claims the GMP/VSR combination can display 168 million pixels/sec. The key to this speed is the internal architecture that allows filling of polygons during a single memory cycle. Segments of 64 or more pixels can be drawn at about 5 nsec per pixel.

Weitek (Sunnyvale, CA) has focused on the high end of computer graphics architecture by providing a fast floating point chip and two specialized chips aimed at solid modeling applications. Called the tiling engine and transformation processor, the ICs are only available on a Multibus board set. The boards allow high-level equations that describe a parametric cube patch and display the image at 100,000 3D points per second. These ICs facilitate the computation-intensive transformation process. The floating point chip has found its way into many high-end systems, such as the One/380 from Raster Technologies, a manufacturer of high end graphics display controllers. The Weitek chips were also chosen for Sun Microsystem's newest color graphics display.

Faced with the traditional set of graphics architectural problems, Mindset (Sunnyvale, CA) chose to use a full-custom graphics coprocessor chip set. Consisting of a graphics coprocessor chip and a display processor chip, the set produces display resolution of 320 × 200 at 16 colors from a 512 color palette. The chip set can produce eight different bitblt operations that are Boolean operations or set by a series of masks.

Also relying on the capabilities of dedicated, custom VLSI, Silicon Graphics (Mountain View, CA) addressed the most basic problem with displaying complex images: numeric computation. Using 10 to 12 Geometry Engines provides 32-bit floating point calculations for real-time 3D display. A newer Geometry Accelerator assists the Geometry Engines by buffering data for maximum system throughout and converting user's data into floating point format. This addition to the original architecture has increased speed of display by 10 times.

Lexidata (Billerica, MA) uses a custom gate array to integrate video shift registers for their 60 Hz, noninterlaced graphics controller system. Fifteen thousand gates were implemented to provide a mixture of TTL and ECL for I/O. The video shift register gate array allows an eight plane, 1280 × 1024 resolution memory and display system to be put on one PC board. The gate array provides 80 bits of high speed latches, a 20-bit shift register to make the beginning of a video pipeline and a 20:1 multiplexer for pixel read back. For eight planes of memory,

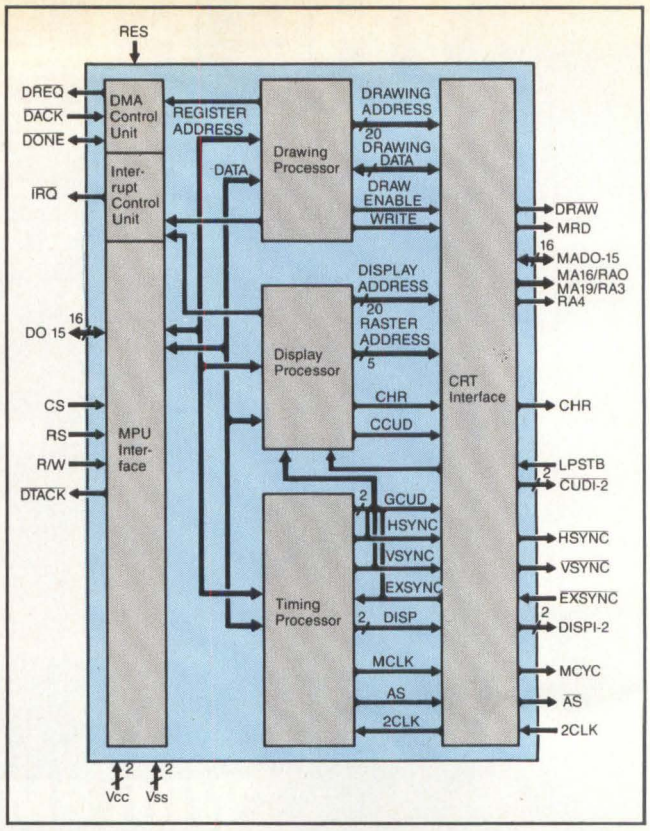


Figure 3: The 63484 from Hitachi uses three processors to perform master operations. The three processors are the drawing processor, the display processor and the timing processor.

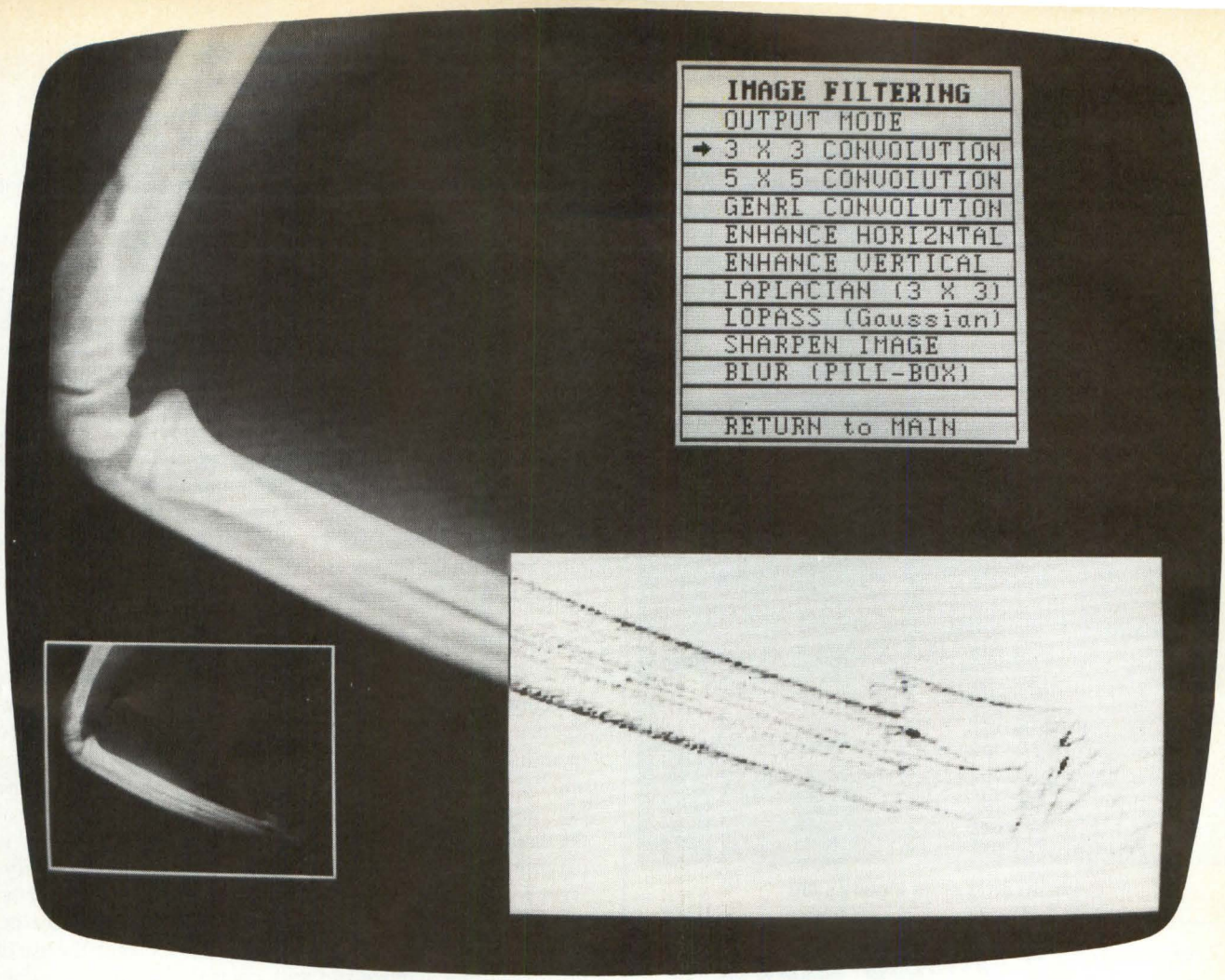
four arrays are required. The part has low enough gate delays to provide the 112 MHz operation.

Adding Glue

Glue chips, common to all architectures, can be a major cost factor and source of potential problems. Too many generic TTL ICs for support of VLSI or special functions can change the cost of a system, making it unprofitable. This is a serious consideration in all graphics systems. One solution is the use of PLAs. Raster Technologies uses a CMOS 750 gate array replacing a 15 sq. in. board. Cost savings such as this are important, as is increased reliability, especially for a system that uses a dot clock of over 100 MHz.

TI has a solution that effectively uses their 4161 VRAMs. The Video System Controller (VSC) is a single chip that replaces the additional circuitry that is usually required for memory support and control in display systems. The VSC provides for DRAM refresh and CRT control; it is programmable, allowing different horizontal and vertical intervals, interlacing control and external sync. The VSC supports resolutions up to 4K × 4K. The combination of the VSC plus VRAM provides a solution to the basic problem of accessing video memory for data modification during display. The approach TI is taking departs from the graphics controller tack. The use of the VSC/VRAM is designed to access and modify memory of the bit map in contrast to pre-processing the data for display.

There is another serious architectural consideration basic to all graphics systems. After the graphics data is created in memory, it must be driven as an output to the display system. This has posed problems in the past as the bandwidth has gone beyond 100 MHz. The components that presented a major block a few years ago were the digital-to-analog converters. In the last



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two years or so, several vendors have created components that are directly targeted at graphics systems.

One problem with graphics architecture was the conversion of TTL signals to high speed ECL. Using a combination of monolithic and hybrid technology, Analogic (Wakefield, MA) created an 8-bit, 150 MHz D/A converters that converts the TTL signal to ECL internally and drives a 75 Ohm monitor. Monolithic D/A converters are available with 8-bit precision at conversion rates of 125 MHz from TRW (La Jolla, CA). To further ease system integration, Intech (Santa Clara, CA) offers a D/A converters in a hybrid package that accepts all three RGB inputs and includes a 256 × 8 color look-up-table with an update rate of 100 MHz. The importance of these components rests in the fact that analog circuitry is very difficult to manage at high clock rates and without analog expertise. A well-thought-out architecture can be executed poorly with disastrous results.

Comparing Architectures

With the flurry of activity in graphics design, two fundamental directions of the architecture exist: incorporating graphics intelligence and functions on VLSI and controlling the video memory better. The goal of incorporating graphics intelligence and funtions on VLSI is to use a chip smart enough to execute high level commands, to control video memory and to control the display functions. With video memory control, the goal is to optimize the memory so that a processor can read-modify-write without interrupting the display. This means control of the graphics functions can be incorporated easily by the processor, window memory or multiple memory planes. With the use of host-based intelligence and with control of easily accessible video memory, greater versatility can be achieved.

While both alternatives acknowledge the importance of the VRAM, controversy still exists regarding the display controller route. Proponents of the VRAM approach claim that the support circuitry of the VLSI approach is expensive, constrained and takes up too much board area. Proponents of the VLSI approach argue that software is a key issue, and the implementation of software into hardware is faster, more efficient and easier.

A difficulty in comparing graphics architectures or systems stems from nonuniform benchmarks. Many vendors highlight specifications that are somewhat true, but in practice seldom achieved. The fill rate is a common example where the specifications are made under optimum conditions. Without regard to setup times and word size, the figures are meaningless. It is clear that a common benchmark is needed where the coordinates (floating point or 32-bit), polygon number and size are specified. Until a standard is accepted, buyers will be confused and the game of "specmanship" will hinder the growth of the graphics industry.

The demands of users of computer graphics systems are fueling the competition for better, faster and less expensive systems. It will not be long before systems that are truely interactive and answer the needs of end users are available. **DD**

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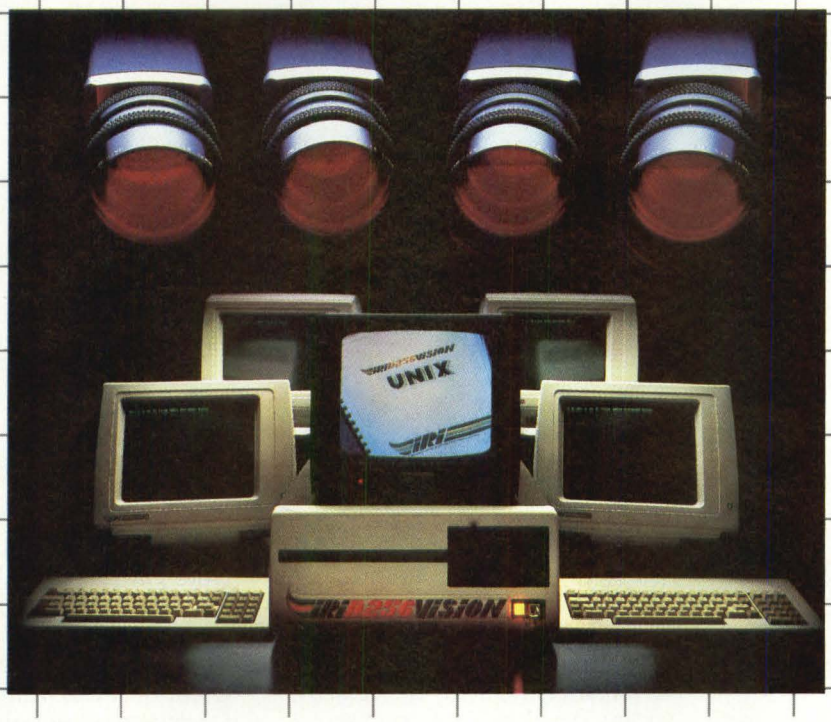

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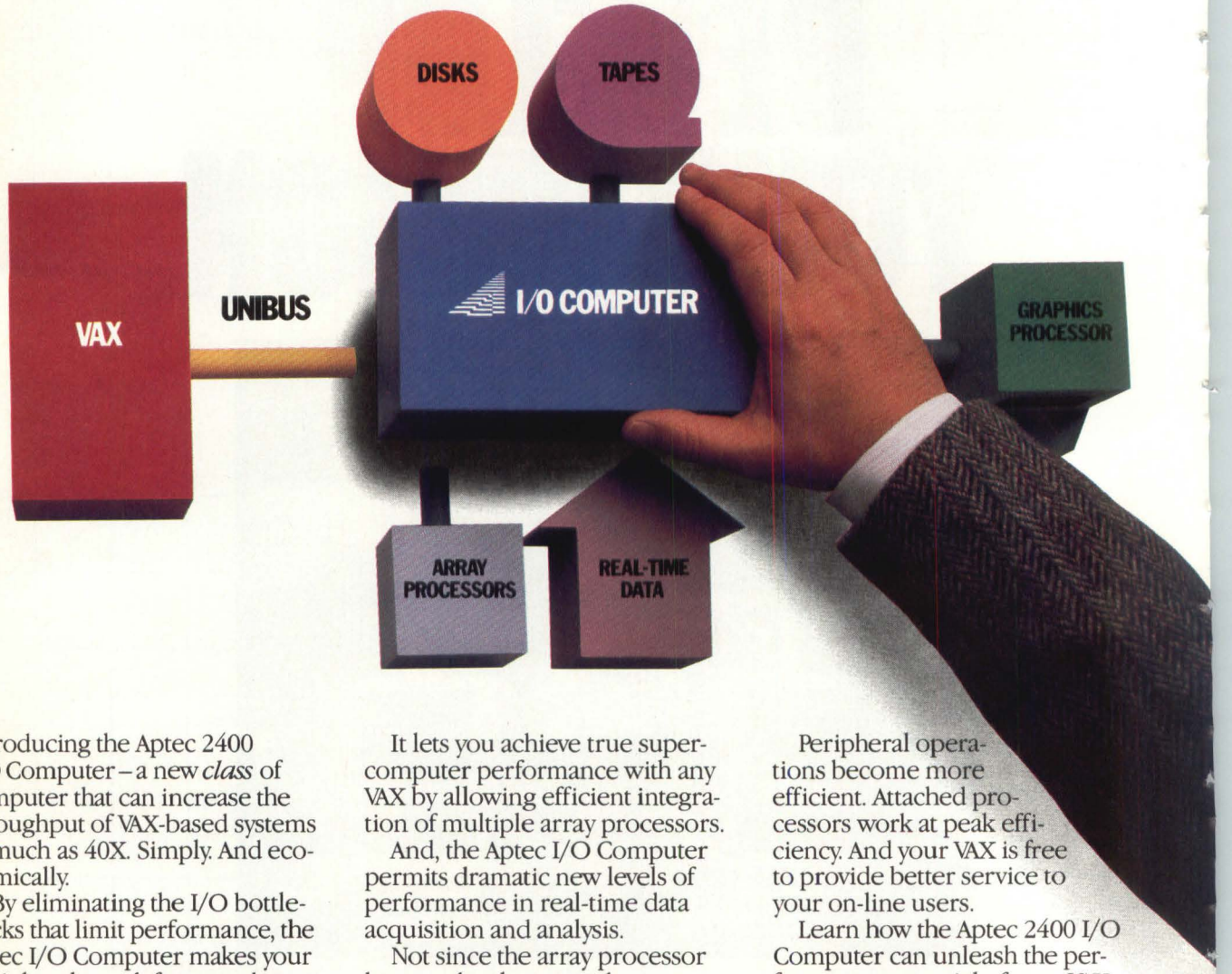

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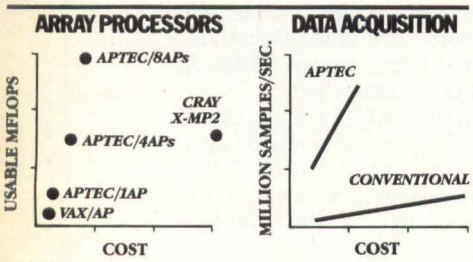

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Peripheral I/O Processor Speeds VAX Performance

by H.D. Meitzen and Delbert L. Taylor, Information Products Systems, Inc.

Computer systems for seismic processing, signal processing in data communications, real-time graphics and high-resolution scanning in medicine handle massive amounts of data. In geophysical exploration, for example, raw seismic data is collected on magnetic tape in contiguous records typically 1 Mbyte and up. The full digital file of acoustic measurements recorded in one test shot amounts to about 6 Mbytes today and is expected to reach 65 Mbytes within a few years – and even a small ground survey can easily require 5,000 shots.

The optimum computer system for work like this combines a multiuser interactive environment for controlling data processing with an I/O subsystem that permits peripheral devices to exchange data at very high speeds with minimal attention from the host. In off-line seismic systems, it becomes feasible to process very large files very quickly. In on-line applications, such as graphics and communications, large amounts of data can be processed in real time. In a multiuser environment, concurrent operation of two or more independent seismic processing terminals or graphics workstations enhances the productivity of both users and computer resources.

The multiuser interactive environment needed for control can be provided by the VMS operating system and DEC's VAX computers. The interactive environment provides the flexibility needed in exception processing: users can examine early results and, if necessary, modify processing parameters for the rest of the run. On the other hand, running programs as is requires attention only in set up.

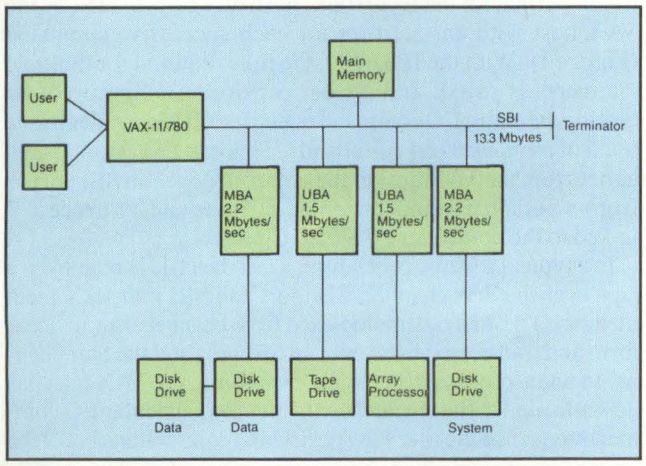

Figure 1: A VAX-based seismic processing system provides the users on the left with the computer resources to retrieve files of seismic data from magnetic tape, demultiplex the file, have the data processed in an array processor and store the output on tape or disk.

The high-speed I/O system is provided by the IPS 6000 Peripheral Processor System, which is housed in a backplane module that mounts inside standard VAX cabinets. The subsystem's bandwidth and dedicated intelligence help create an overall processing capacity equivalent to mainframe systems. In comparison with the customized superminicomputers currently in use, the combination of a VAX system and IPS 6000 has nearly twice the I/O bandwidth at about two-thirds the total cost.

Extended VAX Capabilities

The typical VAX-based seismic processing system in **Figure 1** provides the two users on the left with the resources to retrieve files of seismic data from reels of magnetic tape, have the data processed as required in an array processor and store the output on magnetic disk or back on tape, perhaps in several different formats and subsets.

Between the time a raw seismic file is copied off tape and finally stored on tape or disk, the data has very likely passed several times over the internal Synchronous Bus Interface (SBI) that forms the backplane of the VAX-11/780's board cage and through board-level Unibus bus adaptors (UBAs) and Massbus bus adaptors (MBAs). The Unibus channels handle multiplexed I/O traffic to and from tape drives and array processors; the Massbus channels handle block-mode traffic to and from the system and data disk drives.

Capacity of the system in **Figure 1** – the number of Mbytes it can process in a second – is determined by the bandwidths of the data paths between the computer and main memory at top and the various peripheral devices below. The SBI itself has a bandwidth of 13.3 Mbytes/sec; the bandwidths (or aggregate data rates) of the Unibus and Massbus channels are, respectively, 1.5 Mbytes/sec and 2.2 Mbytes/sec for the VAX-11/780. The bandwidths of the Unibus and Massbus channels are wide enough for typical VAX applications but can limit performance in handling the special demands of seismic and high-volume real-time systems.

The principal extension of VAX hardware architecture through the IPS 6000 subsystem must then be wide bandwidths into and out of the SBI – wide enough so that the SBI is being used at nearly its maximum bandwidth (during portions of the seismic processing cycle in which it is active). In conjunction

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with this, the subsystem must also support very high data rates for direct transfers between peripherals (during portions of the seismic processing cycle in which the SBI is not active). Fast direct transfers are necessary in handling multiple array processors and the new tape and disk drives, which have progressively higher data capacities and transfer rates.

Multiple array processors are designed to provide users with dedicated or shared array processors for the seismic data they are currently processing. Array processors, which have typical data rates of about 4 Mbytes/sec, perform two types of on-line processing tasks, relatively simple data conversions and complex matrix manipulations. Integer to floating point conversions are performed on very large data arrays: a single array of raw marine seismic data, for example, consists of 3000 scans of 4 bytes of data in each of as many as 1024 channels (96 to 240 channels are typical now). On-line matrix manipulations in seismic processing extrapolate velocity data to create a subsurface density profile, and the resulting model is analyzed by changing velocity data.

The high performance tape drives used today in seismic processing have densities of up to 6250 bpi and data transfer rates as high as 780 Kbytes/sec. In the near future, tape densities will be over 18,000 bpi in 18-track transports, and transfer rates will be more than 3 Mbytes/sec. A typical disk access time today is 26 msec, and data transfer rates are up to 2.2 Mbytes/sec.

The highest performance magnetic disk drive that is currently supported for in-process storage with the IPS 6000 is the IBIS Winchester drive based on 3380 technology. The IBIS has an access time of 16 msec, and data transfer rate of 12 Mbytes/sec; its data capacity is 1200 Mbytes formatted or 1.2 Gbytes.

The trend in seismic processing is toward archiving on larger and larger disks rather than on tape. Optical storage devices such as Storage Technology Corp.'s 7640 will have data capacities on the order of 4 Gbytes and offer significantly lower cost per stored Mbyte, about $.05, in comparison to about $.09 for tape, and superior data density (in Gbytes per cubic inch). Moreover, magnetic tape must be rewritten every two years, whereas optical disk storage is permanent.

System Design

The capabilities of the seismic processing system in **Figure 1** have been extended in **Figure 2** by adding the IPS 6000 Peripheral Processor System. The high-speed data path is IPS 6000's Star channel, a time division multiplexed (TDM) bus synchronized with the VAX's SBI. The Star channel provides for communication of commands, data and status (including addresses) as well as priority information and clock signals. Its bandwidth is 40 Mbytes/sec; that is, the 64-bit-wide channel transfers 64 bits of information in each 200 nsec TDM time slot. This bandwidth is large enough so that one Star channel can handle concurrent data transfers over two 13.3 Mbyte SBIs on the host side and between several sets of devices on the peripheral side.

Data is transferred between the SBI and Star channel over one to four SBI port interfaces which translate between the communications protocols on the SBI and Star channel. An SBI port duplicates the functions of a Massbus adaptor (RH780-A) and has twice its bandwidth. The SBI ports support all types of peripheral devices that are on the Unibus and Massbus devices in **Figure 1**. Although, like the Massbus adaptor, an SBI port can transfer data to only one device at a time, one Star channel is capable of supporting as many as 10 active SBI ports (4 Mbytes/sec each).

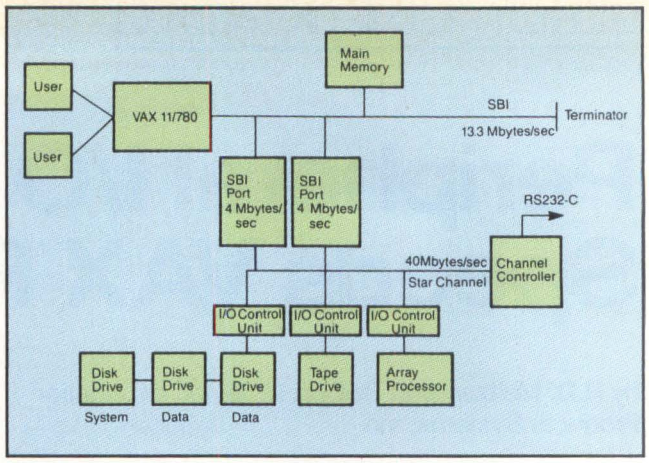

Figure 2: The capabilities of the VAX-based seismic processing system have been extended by adding an IPS 6000 Peripheral Processor System. The I/O subsystem has introduced a high-speed data path between peripheral devices and has reduced the host's participation in the processing cycle.

Channel Controller

The channel controller has three principal functions: mapping physical data formats between the SBI and Star channel, furnishing diagnostics access to the IPS 6000 subsystem and executing I/O command queues. Mapping registers are under firmware control on the controller, instead of in hardware on the Massbus adaptor. The controller automatically runs channel diagnostics on start-up and provides an RS-232-C communications interface for remote diagnosis. Any register in any device on the Star channel can be read or written into, which is useful for external control of the I/O process.

The intelligence in the channel controller is based on a custom AMD 29116 16-bit bit-slice microprocessor in order to attain an execution speed high enough for the channel. Since the controller handles words from 48 to 64 bits wide, a less expensive off-the-shelf 16-bit integrated microprocessor would have been too slow because it breaks up words for transfer.

I/O Command Queues

The I/O commands involved in controlling data transfers between peripheral devices would normally be provided by the VAX host with an interrupt for each successive command (**Figure 1**). With the IPS 6000, the time required for multiple interrupts is saved, and system performance improved, by writing the entire I/O command queue into the controller in one burst of as many as 64 commands. This can be accomplished either from the VAX host to the controller over an SBI port or from a personal computer or other independent processor linked to the controller's RS-232-C port.

In a typical seismic procedure, a test data file is read from a tape over the Star channel, SBI port and SBI into VAX main memory. The data is demultiplexed from channel array to linear form and transferred back over an SBI port and the Star channel to an in-process disk. In the meantime, the VAX host has down-loaded to the channel controller the particular I/O command sequence the user has specified to control transfers of the linear file into and out of an array processor (the transfers typically involve large numbers of small data blocks, ranging between 1024 and 4096 bytes in length). There may be several passes through an array processor using different algorithms

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I/O Control Units

There are special I/O control units for disk drives, tape drives and array processors. All have buffers, ranging from 16 Kbytes to 256 Kbytes in size, to compensate for differences in data transfer rates among peripherals and between peripherals and SBI ports. Like the channel controller, all control units are based on AMD 29116 16-bit bit-slice technology.

There are two types of disk control units for the IPS 6000 and both can handle as many as four drives. The enhanced Storage Module Device (SMD) serial interface unit supports and aggregate data transfer rate as high as 24 Mbytes/sec. The modified Intelligent Peripheral Interface (IPI) unit supports the IBIS disk drive. Disk drives that are compatible with either type of control unit appear to the VAX host's VMS operating system as either a Digital RM or RP series drive. VMS modifications are therefore not required (drives emulating RM can be linked to the same control unit as drives emulating RP).

The I/O control units are also compatible with VMS-standard diagnostics. The disk control units support full-track buffering (eliminating rotational latency in sequential operations) and extended disk I/O features (remote position sensing, overlapped seeks, mapping two or more logical units into one physical unit). The tape control unit supports three interface standards: ANSI, STC and Telex. Each unit controls up to eight drives.

There are I/O control units for three makes and speeds of array processors: Star Technologies (100M FLOPS), Numerix (30M FLOPS) and Floating Point (10M FLOPS). One control unit is required for each array processor.

Maximum system performance is attained with one array processor for each concurrent processing task. As long as it has adequate execution speed, however, an array processor can be shared by two or more tasks under control of the channel controller.

System Configurations

The three standard IPS 6000 subsystems, which contain different numbers of SBI ports and I/O control units, are identified by the widths of their backplane modules that are mounted in the VAX computer's CPU board cage or extension cabinet. The 4″ model (which supports the subsystem in **Figure 2**) fits into the cage space normally occupied by a four-board MBA and consists of six extended-hex boards: two SBI ports, three I/O control units and one channel controller. Board space has been reduced – an SBI port provides the same functions as an MBA on only one board – through extensive use of bit-slice and gate array technologies.

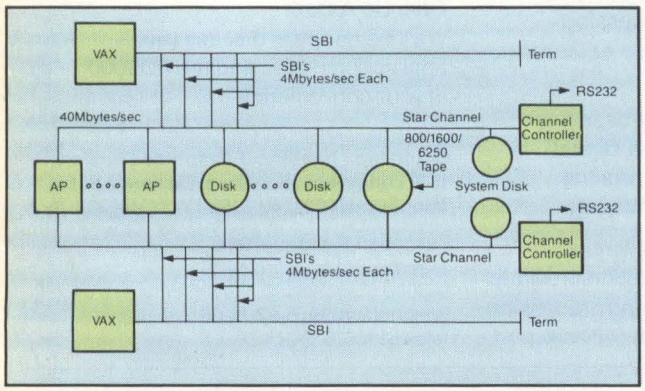

Figure 4: All elements are duplicated, including hosts and system disks, to achieve high reliability in real-time systems such as nuclear reactor control and satellite communications processing.

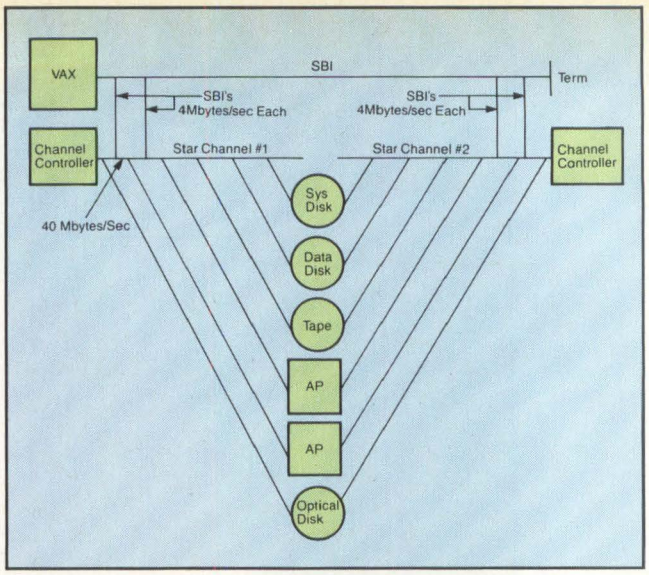

Figure 3: A high-reliability system based on a single-host computer provides duplicate high-speed paths over two Star channels to dual-ported drives and array processors.

The 3½″ IPS 6000, which occupies the SBI terminator's space (the terminator is plugged into the back of the IPS 6000 module), comprises one SBI port, two I/O control units and one channel controller. The 8″ model, which occupies the space of two MBAs, comprises four SBI ports, eight I/O control units and one channel controller.

As limited by the addressing capability of a 32-bit host, the IPS 6000 can support very large data bases. The 8″ module, for example, has a maximum configuration of four disk drives on each of eight control units. Maximum data storage with IBIS 1.2 Gbyte disks is then 38.4 Gbytes.

High Reliability Systems

The representative system configuration in **Figure 2** can be modified in a number of ways to meet the needs of different types of applications. For example, the host can be the smaller VAX-11/750, the more powerful VAX-11/785 or any other larger member of the VAX computer family. There can also be two hosts to provide additional capacity and high reliability or fault tolerance. The two high reliability systems in **Figure 3** and **4** are based on a single host and dual hosts, respectively. In **Figure 3**, two Star channels on the same SBI provide duplicate high-speed paths to dual-ported drives and array processors. The system will continue to operate when a single fault occurs at any point below the SBI. In **Figure 4**, there are also duplicate hosts, SBIs and system disks to attain extremely high reliability in real-time systems such as for nuclear reactor control and satellite communications processing. **DD**

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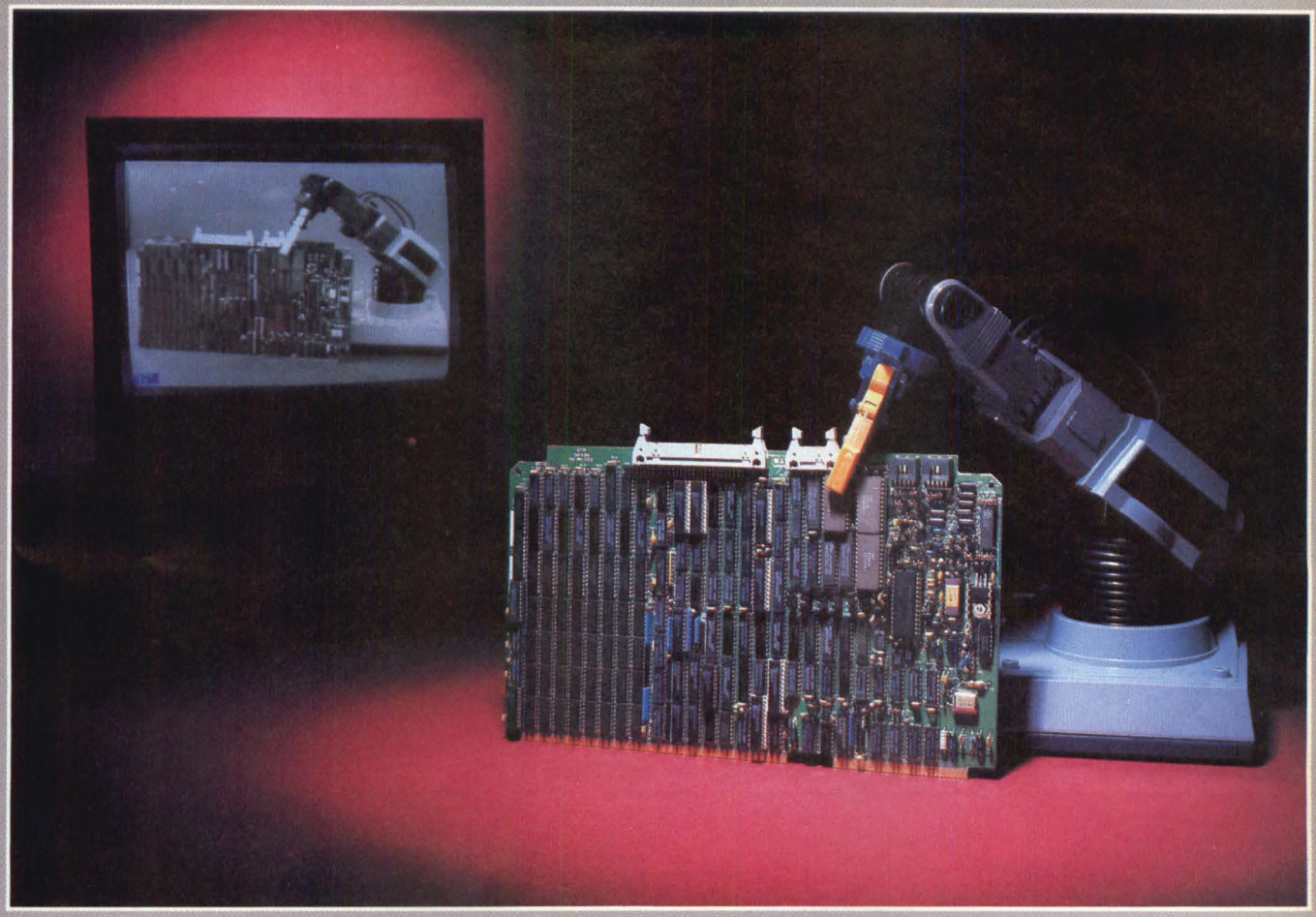

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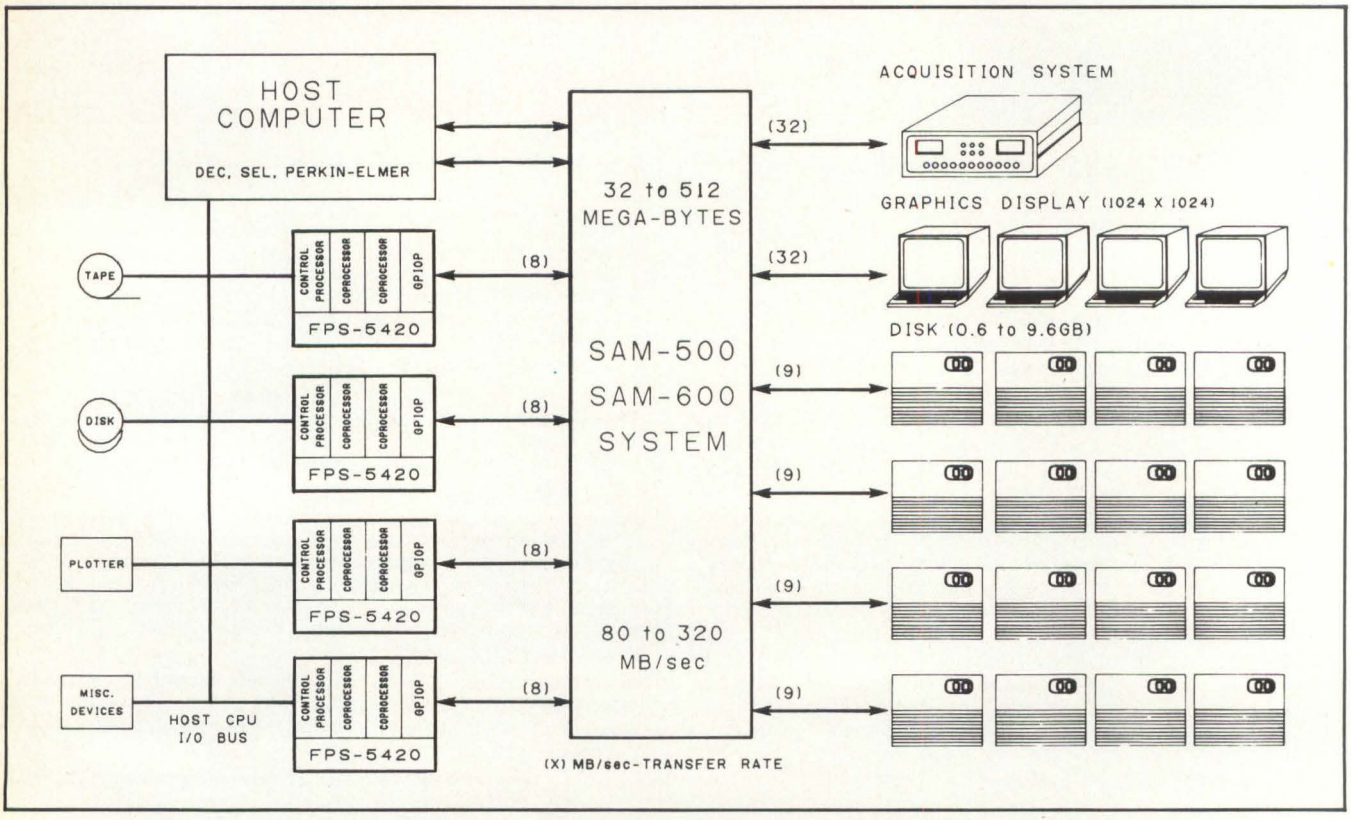

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Printed Circuit Board Design Demands Versatile Integrated Tools

by Julie Pingry, Senior Editor

Makers of printed circuit board design automation tools are hard-pressed to keep up with designers' desire to use new components and packages. PC board layout systems that allow different pad shapes, specifying device areas on both board sides and fine traces on multiple layers for surface mounted devices are only one aspect. Board design programs need flexibility and interactive features to accommodate mixing TTL with ECL, CMOS and discrete analog devices on increasingly dense and large boards.

Integration of design stages to allow accurate updated documentation is critical as well. If there is a problem or gap while the circuit is being designed (especially common with R&D situations and new types of boards), the engineer should be able to revise a board being laid out by simply changing the schematic. The reverse, back annotation, is also important to design integrity. This allows a schematic to be updated with reference designators and pin numbers as components are placed and swapped for optimum routing.

Interactive changes at every turn allow circuits to meet design constraints. Every board must not only meet speed and function requirements, but also be manufacturable. Some board design systems handle many types of components easily. In contrast, fast and efficient automatic layout algorithms often recognize fewer part types. Computer-aided design programs should not take away engineers' ability to use all of their experience to advantage.

Using Non-TTL Components

Different kinds of devices, like ECL, CMOS and discretes, operate best with particular connection schemes. Since the mainstay of logic components is still TTL, these connections must usually be mixed with TTL-type traces on a board.

Almost all PC board layout systems claim that analog components are handled easily and can be intermixed with digital. However, the way that discrete parts and DIPs are mixed can vary greatly. Autoplacement programs that do not differentiate between analog and digital may place discretes together rather than in association with various ICs.

Another difference is that DIP components generally need only 25- or 50-mil grids and diamond-shape pads. Discrete analog parts present particular problems to automatic placement packages and autorouters that only operate on standard grids. Many systems allow users to define grids as fine as one mil. Nevertheless, placing and routing to these grids is usually only interactive. This means the process of laying out and routing a board including discretes may take nearly as long with CAD as by hand.

> Layout systems must operate by section to combine TTL, ECL, CMOS, DIPs, SMDs and discrete components on a board.

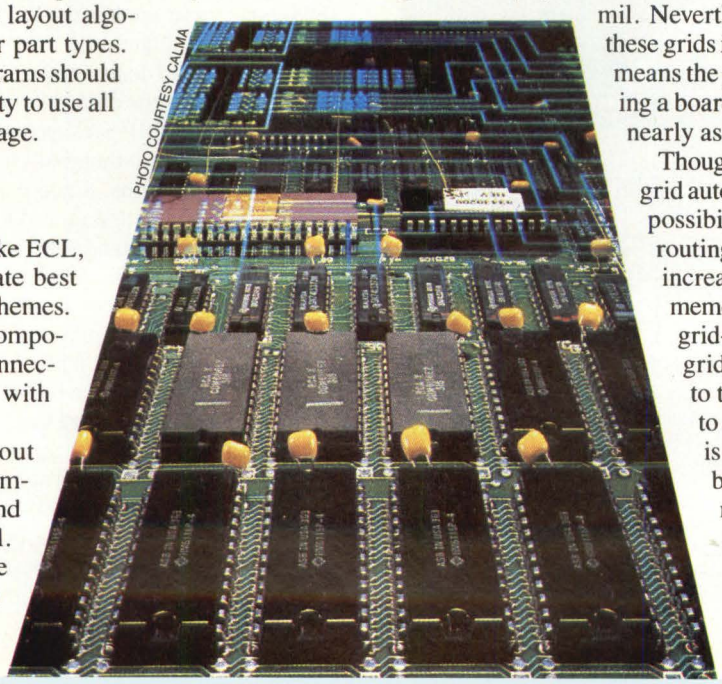


PHOTO COURTESY CALMA

Though some systems now offer fine-grid automatic routines, increasing the possibilities for pad placing and trace routing 25- or 50-fold significantly increases software, processing and memory requirements. One way that grid-based systems may handle off-grid parts is to autoplace and route to the grid and then post-process to actual placement. The danger is that design rule violations may be introduced when components are moved back to actual positions. Current revisions of programs such as Scicards address the severe limits grid-

based algorithms place on design by moving to a gridless system. With gridless programs, the disk space and CPU power of the layout system set limits on board and trace parameters. The algorithm itself is virtually limitless.

High frequency design is particularly tricky. Many high speed designs use ECL components. However, improved CMOS processes yield high speed devices, and transmission line theory may soon apply to these components as well. A number of PC board design systems treat high-speed components the same as any others. On systems that allow the designer to set special restrictions on particular signals or groups of signals, ECL parameters can be met. But this method requires lengthy pre-design work.

One approach is to have a special system for high frequency, as Zuken America (San Jose, CA) does. Their Analog Designer uses the same file format to define the graphic library as plotters use. Therefore, curves on the Zuken system are as accurate as a photoplotter can generate them, and not just orthogonal and 45° traces. With these curves, a fast signal won't propagate in a straight line instead of following the bend. Users of most systems must modify traces by hand for curved corners.

If ECL figures prominently in a company's boards, PC board CAD systems with special ECL design rules checking (DRC) and a special ECL router package will be helpful. Companies offering this feature include Racal-Redac (Westford, MA) with Maxi and Visula, Scientific Calculations (Fishers, NY) with Scicards and ASI (Brookfield, WI) with PRANCE. More restricted algorithms for routing, as well as strict design rules checking, help ensure that high speed circuits will operate as planned. Zuken's system allows designers to create a look-up chart for spacing requirements on the basis of line voltage. The system then autoroutes high-voltage nets with more spacing than others, as the user specifies. Trace parallelism and net analysis programs are included in the Scicards 85.01 revision, scheduled for release next month.

Traditional orthogonal routers tend to create jagged traces

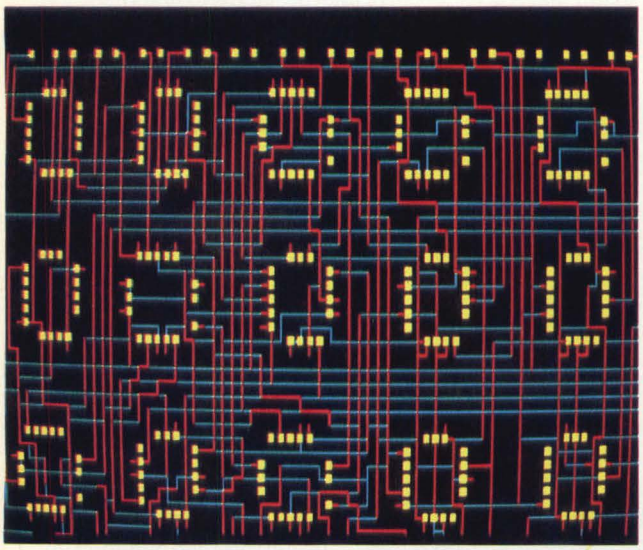


Figure 2: This is how surface mounted devices appear on the screen of a Data General GDC 1000 system running RDS AutoMate software. Board designs using SMDs are supported by variable grid structures and hidden vias. This program is one of the few that will automatically swap components between two sides of a board.

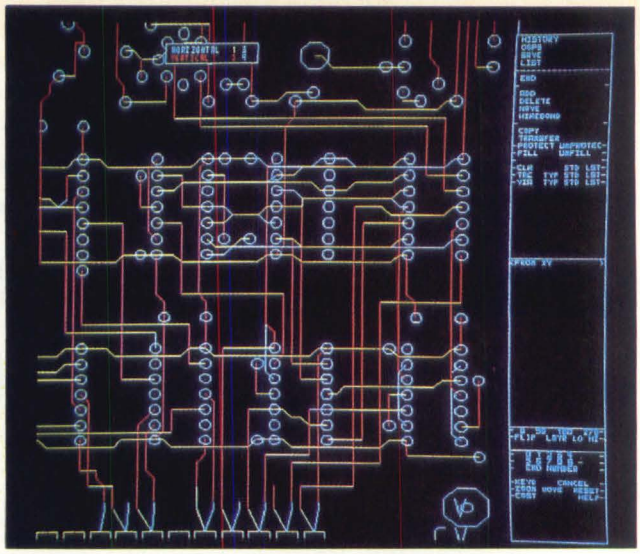


Figure 1: Scicards system designing multilayer board with 45° angle etch. Programs that automatically route traces at 45° as well as horizontal and vertical help keep lines short. Memory routers need these angles as well. The newest version of Scicards also includes a parallelism analysis for ECL trace checking.

that look like stairsteps and are longer than they need to be. Zuken, Calay (Irvine, CA) and Cadnetix (Boulder, CO) provide packages that minimize trace stairstepping to straighten and thus shorten lines after routing is complete. Short traces are always desirable, but with high-speed logic, the difference may be between proper and faulty circuit function.

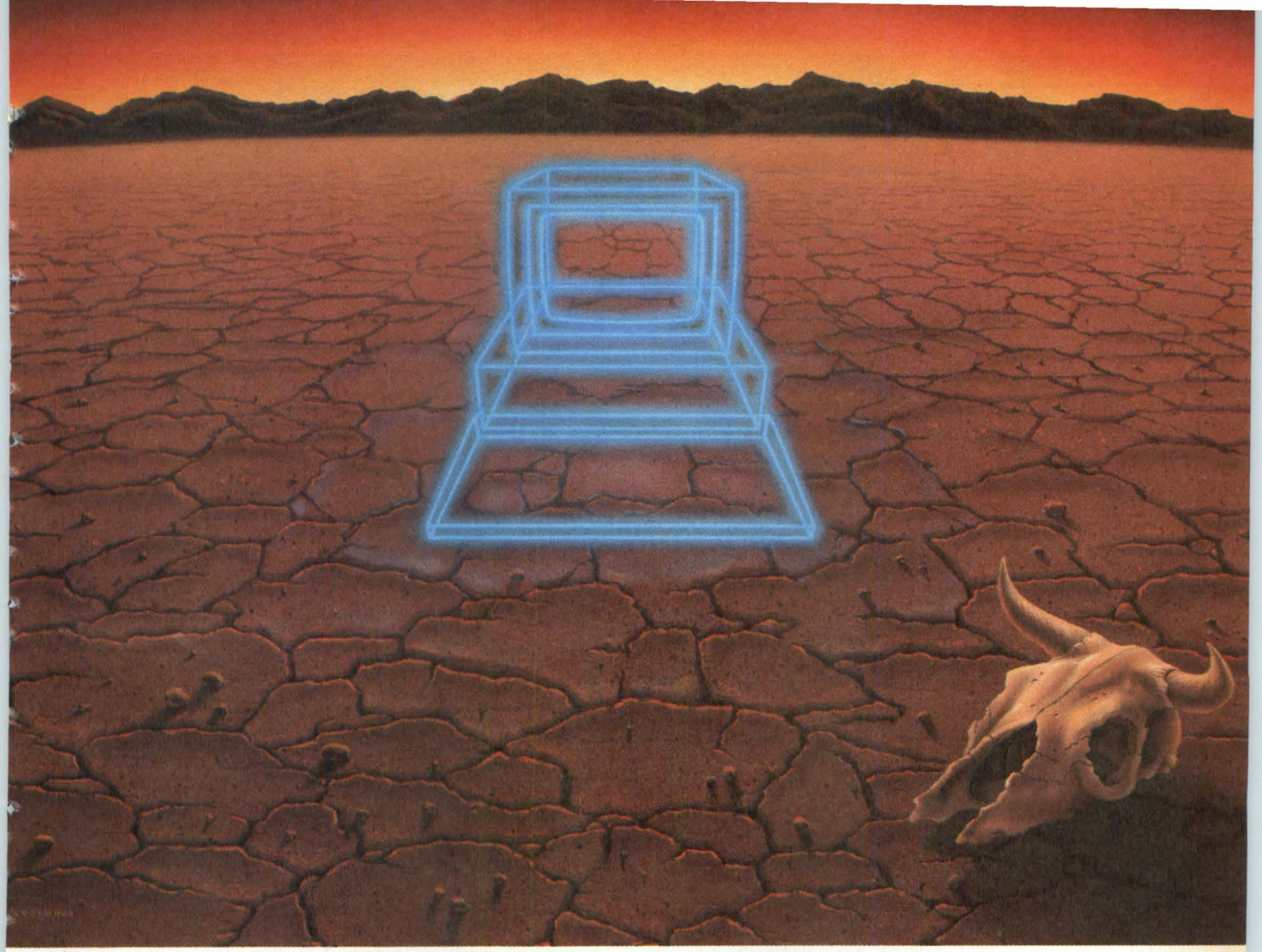
Routers like the Applicon Bravo PCB that can place traces at 45° angles instead of just orthogonally have less need for this post-router processing. Look for 45° autorouting in updated versions of layout systems such as Scicards soon (**Figure 1**). To reduce the risk of crosstalk, automated programs should also check for parallel traces that are too close together for long runs.

Designing With New Packages

Two thrusts in system design, higher performance and smaller area, are converging into a demand for more functions per unit space. Complex devices may now be packaged in any of a variety of pin grid array, leadless and surface mounted devices (SMDs). These packages present a big challenge to board design and manufacture.

Most PC board design systems allow the designer to specify size and shape of the package and pads. Still, most systems do not address non-DIP packages well. SMDs are not on 100-mil centers like DIPs, so their pads tend not to fall on 25- or 50-mil place-and-route grids. Since there are several SMD package types, only a few with standard footprints or outline, they cannot yet be added to standard shape libraries. In addition, pads and component spaces should appear on only one side of the board. In designing two-sided boards, nearly all systems now require the engineer to place each part on one side or the other. Even companies like Cadnetix that provide a special SMD handling capability make two-sided placement manual.

Some newer board design systems like the Visula system from Racal-Redac will permit automatic swapping between two sides. Automatic layout programs as used by some service bureaus like Algorex and RDS AutoMate (Palo Alto, CA) also perform swapping between sides. Though these programs have not been available for in-house design use, Data General's (Westboro, MA) agreement with RDS AutoMate covers Auto-



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Mate's two-sided autoplacement program (**Figure 2**). The processing and memory requirements of packages with these advanced algorithms are, predictably, fairly large.

The density of boards using small, high-pin-count component packages may require multiple trace layers. Including power and ground layers, Scicards handles 20 layers. The new revision will handle 32 layers. Calay can route 8 signal layers; Cadnetix and VR's (Austin, TX) Merlyn systems route up to 24 trace layers; Vectron specifies 25. Racal-Redac's newest systems will handle 16 layers, up from four. ASI claims that hardware places the only limit on the number of layers PRANCE can lay out. Though current designs may not require many layers, high limits are better insurance for future needs.

CAD Systems for multiple signal layers need different routers. Most programs route two layers at a time. To better distribute density over the entire board, a few companies offer simultaneous routing on several layers. For example, Calma's T-Boards routes four layers at a time; Applicon claims multilayer routing with the Algorex software as well. Autorouters in the 32-layer Scicards release will operate on all layers at once.

Buried vias are often used for SMDs and complex multilayer boards. With multiple signal layers, vias may only need to go between pairs of layers and not all the way through the board. This is a feature many companies' multiple layer systems already have. Some who do not, like Applicon, claim that through-holes may be more cost-effective in manufacturing than buried vias. Though few current designs really require the space on each layer that unused vias occupy, space saving is undoubtedly gaining importance.

Since a vast majority of boards currently use few if any SMD or exceptionally high-speed parts, systems must accommodate combinations of TTL, ECL, DIPs, SMDs and CMOS discrete components without bogging down unduly. To place and route mixed component boards, CAD systems must provide optimized routines for each type of component. Placement and routing programs should be specified by nets, layer, name prefixes, individual signals or physical section of board.

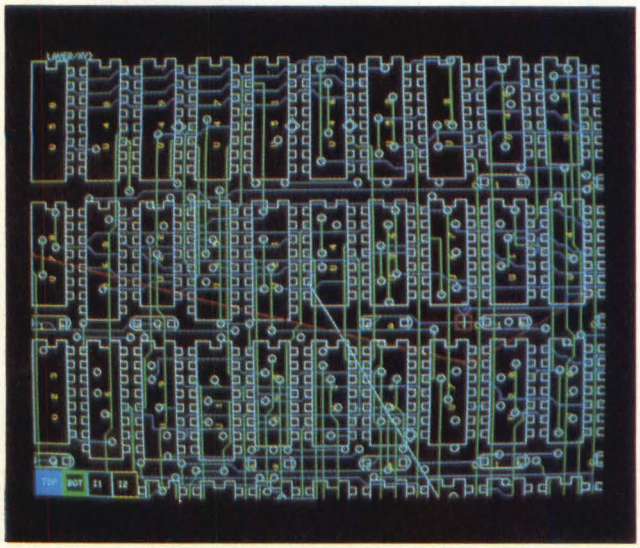

Figure 4: Real-time DRC as with Calma's T-Boards flags routing errors (in red) and will not allow the designers to continue until they are corrected. This on-line checking assures that the designer does not spend time designing on the basis of components and traces that need to be moved for manufacturability and electrical continuity.

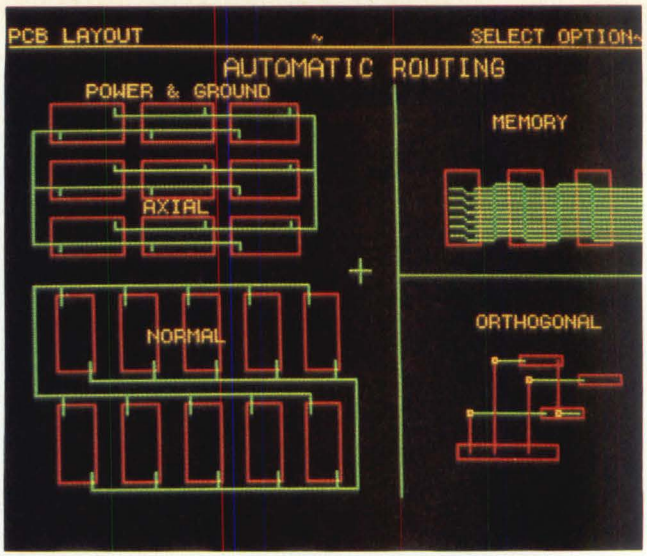

Figure 3: The Redboard system from Racal-Redac runs on an IBM PC or XT and has separate routers for power and ground, memory and orthogonal traces. By choosing components to be routed by each of these programs, optimum trace layout is possible with nested 45° angles on memory traces.

Ways To Skin The Cat

Key to mixing different technologies and packages is the system's ability to work with only part of a board during an operation. CAD system flexibility includes three other main features. First is a combination of automatic and interactive routines for placement and routing. Although a fully automated batch system may speed the design, critical component placement and trace routing are nearly always best done by the engineer. Second is a variety of algorithms available for each task. Third is DRC override, which also enhances the designer's ability to complete the board: All of these make automated design more like manual design.

The origin of a PC board design system may indicate its interactive capabilities. Those that originated in a design service bureau environment will tend to accommodate large boards and nearly any type of component but have few or no interactive features. Vectron Graphics (Santa Clara, CA), for example, began as a bureau. ASI is still primarily a service bureau, but they now offer PRANCE users a routine to allow some interaction via Megatek color graphics terminal plus IBM PC AT. And Applicon's agreement with Algorex permits both powerful automatic routines and interactive capabilities.

Most CAD systems concentrate on routing, but placement can aid efficient autorouting. Optimizing placement routines are standard with Telesis' (Chelmsford, MA) EDA-3000 PCB; Calay autoplacement software anticipates their router's algorithms and places components according to how easily connections may automatically be made. RDS Automate concentrates a good deal of effort on placement as well.

Another feature that can ease autorouting is placement histograms, which show density of connections on the board as it has been placed. Very dense areas appear as peaks on PRANCE and Telesis density histograms. Manual re-placement can level out the graph, or several placements can be displayed for the most promising.

Automatic routing programs are notoriously inflexible. Static router programs that lock a trace into place as soon as it is routed

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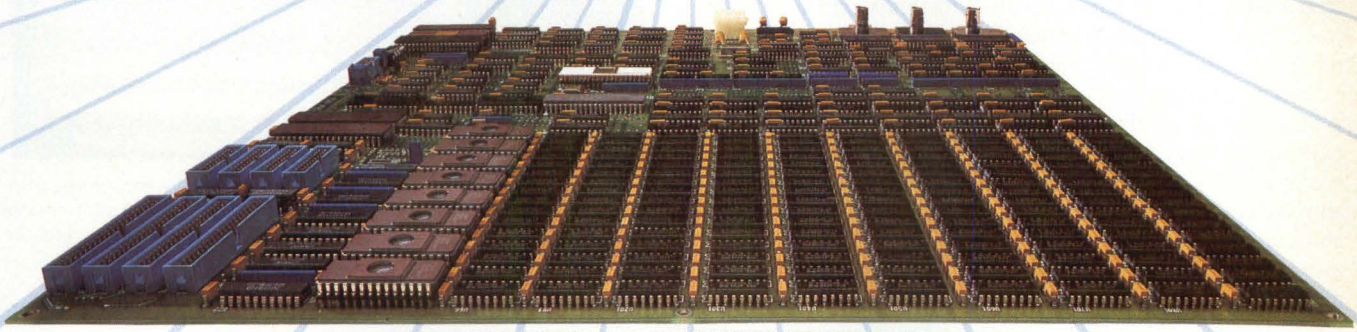

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can block pins, making connection fails that must be manually maneuvered to open paths to the pin and complete routing. Others rip up completed routes to connect fails. This is normally done in a batch after an analysis of hot-spot areas that are too dense to complete all traces. Some systems, such as Applicon's Bravo, allow trace-at-a-time rip up. With this scheme, only one trace is unconnected rather than the entire hot-spot area. The intent is to leave intact as many good routes as possible.

Interactive routers are not as critical with efficient automated routing algorithms. If the user can set parameters and fix critical paths in advance, any routing program is more flexible. Combining several routers may be even better. For example, Vectron's router uses pattern fitting first. This router tries to create straight, then L-shaped with a via and inverse L traces first, for the cleanest possible initial routes. After this, the system runs an exhaustive Lee algorithm router (the most common autoroute algorithm) to finish.

Other approaches include even more routers. Scicards has five different routers; PRANCE has four, as do Racal-Redac's larger systems, and Telesis workstations and Racal-Redac's PC-based systems (**Figure 3**) use three routers. Normally, if only one rip-up algorithm is available, full re-entrance for user interaction is critical. Exhaustive rip-up autorouters generally run for several hours, and intervention may allow more reasonable completion times.

The goal is not just to autoroute 99% of the board in the shortest possible time; it is to finish routing a board that has optimum performance and is fully manufacturable. Often, the 1% not routed by automatic routines is nearly impossible to route. Sometimes, that 1% cannot be completed in the time that a full 10% could be done after a combination interactive and automatic route. And experienced designers can often foresee problems with particular ICs, traces or nets that no algorithm can handle.

Two approaches are generally taken to design rule checking. On-line DRC (**Figure 4**) generally does not let spacing violations occur. Though this is an aid to users doing interactive work, it can slow down a program considerably. In addition, designers often violate design rules intentionally to make difficult connections and complete dense boards.

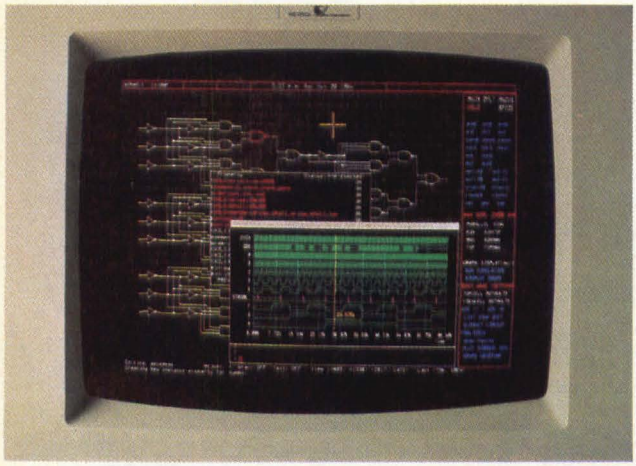

Figure 6: On the Metheus-CV workstation, the HILO simulator in the foreground is accessible while in the schematic editor. Metheus workstations also interface to Computervision CADDS systems for PC board placement and routing. This combination of integrated design tools increases accuracy of input at each stage of the design cycle.

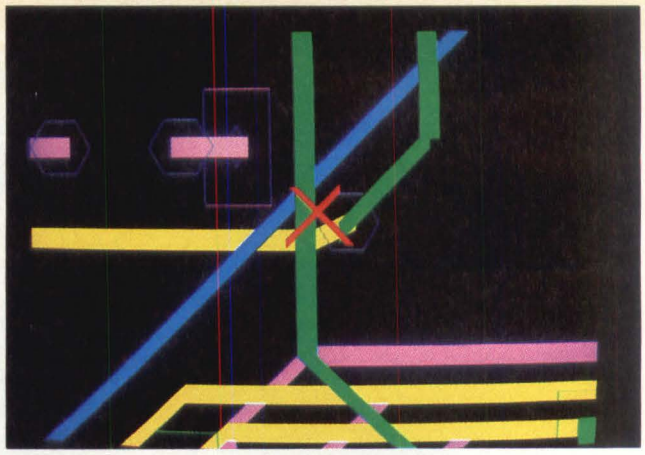

Figure 5: Design rule checking on a Telesis System recognizes true component pad sizes and shapes. Here, a pad too close to a line of etch is highlighted with a red X to remind the designer where a correction may be needed.

Many systems provide batch DRC. Output of a batch check is generally a netlist mismatch or spacing violation list; the best of these programs also provide a visual display of where rules have been violated (**Figure 5**). The designer can then find and fix unintentional violations, leaving intact those that were introduced to allow completion.

With several approaches available at each design stage, the options of manual design are combined with automated speed. Either full re-entrance at every step of an automated process or a full complement of algorithms used by the automatic router can provide this range. Some of the faster routines are the least flexible and create boards that are difficult to complete and to manufacture.

ECOs and Back Annotation

The normal design cycle begins with schematic capture, from which a netlist is generated. Once the design has been verified, placement and routing programs take over, and after optimum layout, artwork and machine tapes are generated. All of these stages are becoming computerized, and though this speeds the process, applications must be integrated for smooth hand-off from engineer to layout designer to manufacturing personnel.

Entering schematics on a small computer is extremely attractive; many firms use IBM PC software for front-end engineering from FutureNet (Canoga Park, CA), Case Technologies (Menlo Park, CA) and P-CAD (Los Gatos, CA). Companies using a mainframe or service bureau for routing may invest in a minicomputer or supermicro-based workstation for several other functions. For this to be effective, interfaces must be written between systems.

Vendors of all levels of CAE and CAD products are developing interfaces that allow not only uploading a netlist to a mainframe, but also downloading for back annotation of schematics. Formatting a netlist for use on another system is only part of the information flow needed; an engineer must be able to make circuitry changes at any point needed as well as be advised of pin and gate assignments finalized during placement and routing. The engineer must also be able to specify pins that cannot be swapped, maximum line lengths and line widths for critical paths in the job library.

Back annotation may be automatic; generally, it is preferable

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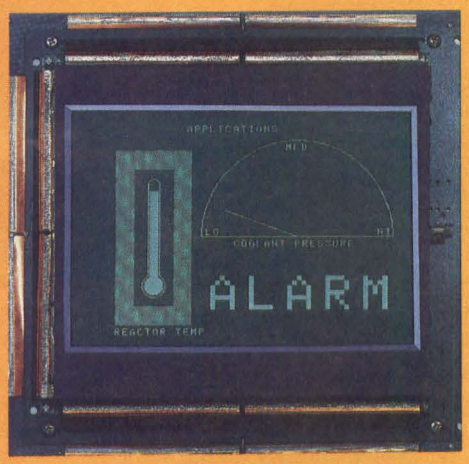

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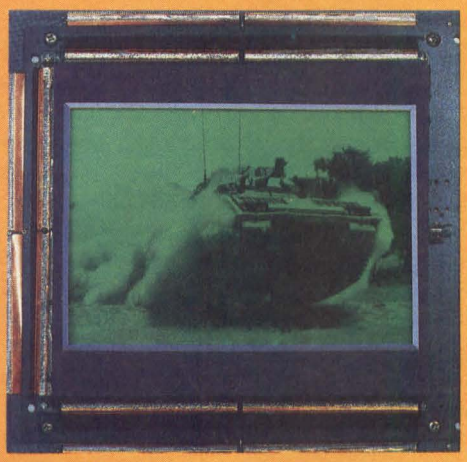

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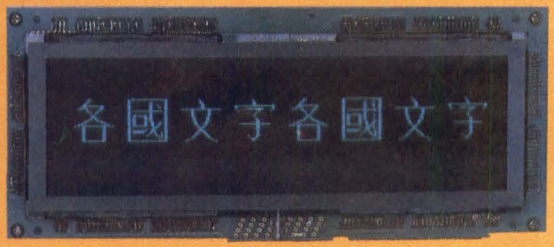

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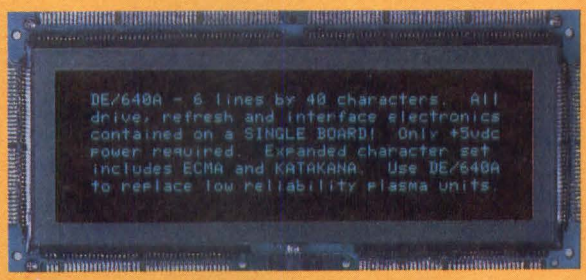

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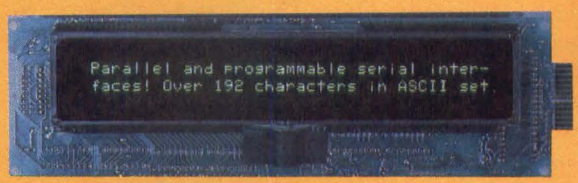

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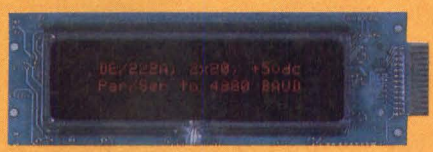

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to have a command for batch back annotation. That way, until all of the design is finished, no interaction between schematic and layout is required. Accurate documentation available to the engineer at every step eliminates time wasted on work with faulty circuit designs. Interfaces between design tools and simulation and test systems are also critical.

Users may want to use engineering workstations to enter schematics and to format the netlist for larger computers for PC board layout and routing systems. HP 1000-based Zuken systems interface to Daisy and Mentor front-end workstations via IGES files. Likewise, Computervision's CADDS 4X and Metheus-CV workstations can communicate for updating schematics on the Metheus workstation.

For a complete design cycle, Metheus-CV also provides an interface into GenRad's (Santa Clara, CA) HILO logic simulator (**Figure 6**). FutureNet schematic capture, which interfaces to several PC board layout systems, offers HHB Softron's (Mahwah, NJ) CADAT logic simulation with their IBM PC XT or AT CAD system. Cadnetix also offers CADAT with their schematic entry and board placement and routing tools. Companies like Calma provide a variety of software tools to cover engineering, verification, design and test.

One way of assuring integration of software for various design stages is to get all of the packages from one company. Racal-Redac uses several different hardware bases that share a common binary database structure. This provides all users and applications rapid response to even complex commands. Using an IBM AT or XT, autoplacement may be performed in seconds, routing in a few minutes. Very large designs can be shipped off to a VAX-based Redac Maxi system over RS-232. Even vendors of mid-range workstations like Telesis now provide back annotation to IBM PCs.

Documented Circuits Inc. (Kingston, Ontario, Canada), Vectron, Calma (Santa Clara, CA) Cadnetix and others tout total solution systems (**Figure 7**) with schematic entry as well as placement and routing capability. Integration can be on common hardware; Data General (Westboro, MA) offers Cericor's AI-based schematic entry system and RDS Automate layout and routing software. Scientific Calculations offers the Schemactive package for a front-end to Scicards. A master file in the Vectron system keeps all nomenclature used for one part, and a back annotation command can attach updated reference designators to a schematic. Although most companies' PC board design programs have some weak links, forward and back annotation are best served by one-vendor solutions.

Beware The Panacea

There are clearly many approaches to designing a board at each step of the way. Different CAD vendors have focused on different aspects of the problem, and finding one piece may or may not help speed the completion of the puzzle. Versatility, choices and completeness take many forms. With the array of PC board design methods provided by various layout systems, comparison may be difficult.

Potential customers must be wary of vendor claims. Some of the most widely installed CAD systems are "multiapplication," which means they perform mechanical and 3D design as well as electronic. This may be appealing, but the specific demands of electronic design are often not well addressed, leading to long, frustrating PC board design cycles.

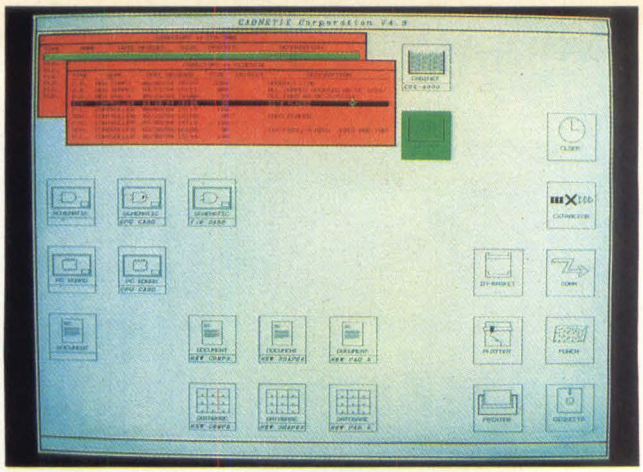

Figure 7: From the orange menu box on the Cadnetix screen, a board with all ICs placed is chosen. Note that the menu on the right side uses icons as well as English words to display function choices for all stages of board design.

Fully automated placement and routing packages speed up part of the cycle, but often leave the most difficult nets for the designer to connect. Overall design time may increase with faster automatic functions. A prime example of this is autorouters advertised as 100% routers. There always will be some boards that cannot be routed to completion. Furthermore, these are usually rip-up routers that blindly connect as much of the design as possible and then disconnect areas of the board with fails, repeating the process as each rip up creates new problems in adjacent areas.

One feature that can shorten routing completion time is intelligent placement packages. Asked about their autoplace program, most companies say theirs is as good as any; this is not a good sign. Forecasts of density and routability from initial placement speed the entire cycle greatly.

Perhaps the most comprehensive wool-pulling act of PC board CAD companies is benchmarks. Companies can play all sorts of tricks to make their systems appear fast. Users should never give the vendor a design in advance, and once the benchmark begins, the user should stay through the entire ordeal. On-line design rule checking can be turned off to speed programs; be sure to request documentation of either batch or ongoing DRC. Finally, there should be criteria other than layout speed. For example, are there extra vias? Could line lengths be shorter? If the board is not 100% routed, are the unconnected traces the most difficult? And above all, is the board manufacturable with the customer's technology? Two or three fine traces between pads may not be feasible, while six simpler layers, though expensive, could provide the same functions.

The board from a CAD system should be totally finished, from schematic to artwork and manufacturing output tapes, in less time than without it. Speed is just one factor. Design automation is only a help if the finished product is as good as an equivalent hand-design or better. In many cases, designer intervention will be needed to achieve this optimum design. DD

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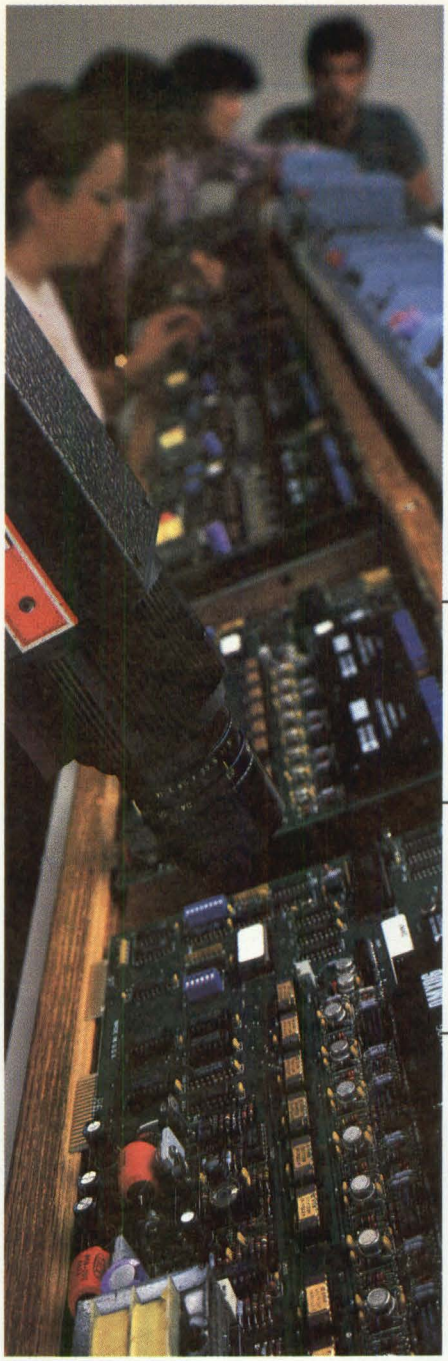

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DMA Controller Relieves Host Of I/O Management

by Scott Searcy, Intel Corp.

I/O subsystems for high-performance computers must not only process and transfer large amounts of data, but also interface to a large number of peripheral devices. Traditionally, an I/O board has been used to meet these system needs. The Intel 82258 pipelined 16-bit advanced DMA processor combines many of the I/O capabilities of a board onto a single chip (**Figure 1**).

Command chaining and data manipulation capabilities of the 82258 enable it to execute sophisticated channel programs in memory-based command blocks. The data chaining feature of the 82258 allows it to either gather a link of data blocks into a single area or scatter them in the reverse operation.

Optimized for the iAPX 86 microprocessors, the 82258 has an on-chip bus interface for full CPU memory addressability with the pipelined, nonmultiplexed 80286 bus as well as the multiplexed bus of the 80186/188 and 8086/88. Both local and remote interfaces with the processor are supported.

Device Architecture

The 82258 has four channels (called selector channels 0-3) that can service high speed peripherals, generally block devices such as Winchester and floppy disk drives. Each selector channel comprises its own dedicated register set and three control lines. Peripherals initiate DMA requests by activating the DREQ (DMA request) input. The 82258 acknowledges that it has recognized the request by activating the $\overline{\text{DACK}}$ (DMA acknowledge) output. When used by a peripheral, the bidirectional $\overline{\text{EOD}}$ (end of DMA) line tells the 82258 to terminate the current transfer. The controller uses the $\overline{\text{EOD}}$ line to inform the peripheral as well as the CPU that the current transfer has been completed and that the status of the transfer is available.

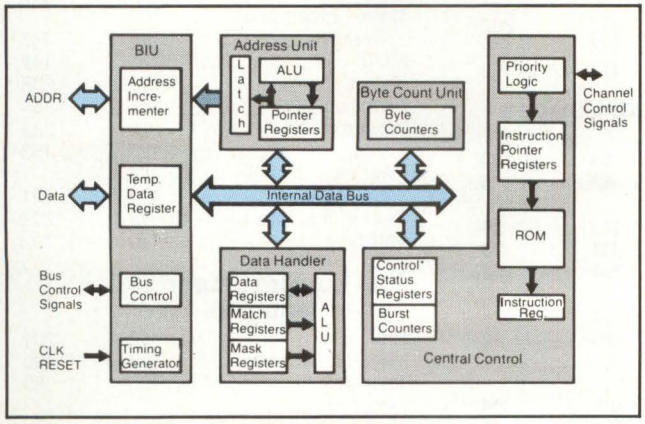

Figure 1: By pipelining the architecture of the 82258, different units can work in parallel, resulting in high-performance data transfers at full bus bandwidth.

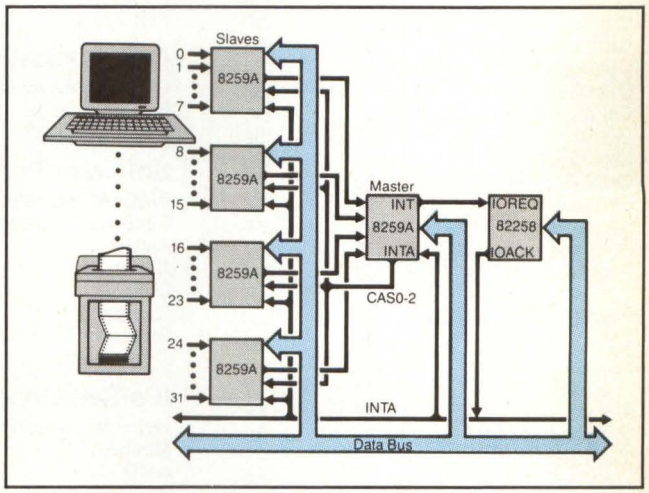

Figure 2: A single 8259A master and its slaves comprise the external circuitry required for the multiplexor channel. When programmed as a multiplexor, channel 3 is capable of servicing up to 32 subchannels.

Selector channel 3 can be programmed as a multiplexor channel to support up to 32 subchannel requests. Subchannels typically handle slow-to-medium speed character devices like CRT terminals and line printers. One or more 8259A interrupt controllers multiplex, arbitrate and prioritize the subchannels (**Figure 2**). After receiving a request, the master 8259A signals the DMA controller via the I/O request (IOREQ) line that a subchannel needs servicing. The DMA controller responds with two I/O acknowledge (IOACK) pulses, which strobe the 8259A to make the interrupt vector available on the data bus. The interrupt vector is used as an index into a multiplexor table to obtain the address of the command block for the appropriate subchannel. The command block is then executed. Using the multiplexor channel, DMA processing can be provided for a wide variety of devices with just four channels. High speed devices can get the majority of the servicing, while low speed devices share the servicing and transfer rate of one channel.

Like the 80286, the 82258 recognizes two separate address spaces, I/O and memory, and allows all transfer permutations between or within the two spaces. To perform these transfers,

(continued on p. 86)

Scott Searcy is an 80286 Applications Engineer for Intel's High Performance Microprocessor Operation in Santa Clara, CA. He has a BS in Computer Science from Purdue University.

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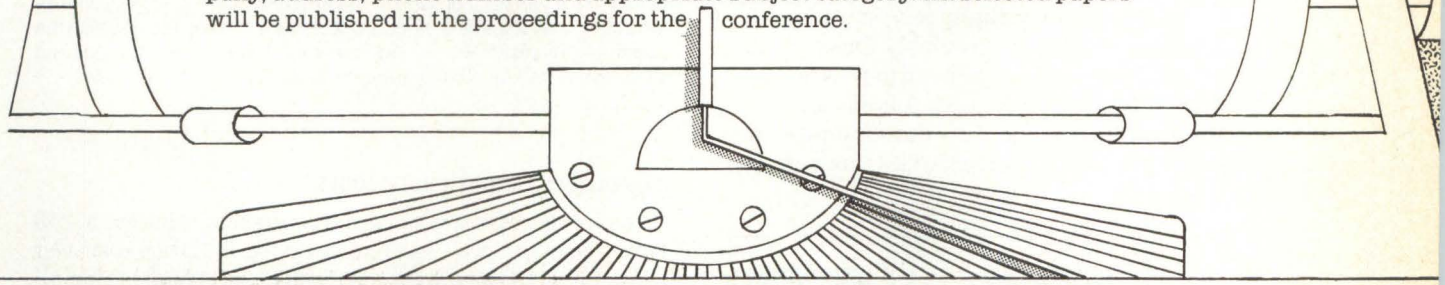

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(continued from p. 79)

the 82258 uses either a single-cycle or a two-cycle method. A single-cycle transfer offers the advantage of speed. Although two-cycle transfers require an additional bus cycle, they allow additional data manipulation operations with the data transfer.

In single-cycle transfers, an address is put out during the single-bus cycle to access a byte or word in memory. The peripheral is selected by the $\overline{\text{DACK}}$ signal asserted by the 82258. Data travels directly between the selected I/O peripheral and memory (or addressed peripheral), not passing through the controller. Since the data is sent directly to the destination, only two of the concurrent data manipulation operations are possible: mask/compare and verify-and-save.

During a mask/compare operation, the DMA controller masks the source bytes or words and compares the result with the value stored in the channel's compare register. At the completion of single-cycle transfers, it is only possible to determine whether a mismatch or match existed in the block. This mask/compare operation can be used to search through a data block for a specific byte or word and halt when it is found. The verify-and-save operation is used to compare the source data block with another block in memory. This is useful for comparing data block identification headers.

Although two-cycle transfers typically require an additional bus cycle, they are more flexible. Data is actually stored in an internal register of the DMA controller on its way to the destination. As a result, more data manipulation operations are possible. For example, the mask/compare operation can be halted when the first instance of a mismatch or match is recognized. Unlike the single-cycle verify-and-save, the verify-and-halt operation transfers no data, but simply performs a block compare. As with the two-cycle mask/compare, however, the transfer can be halted on the first instance of a mismatch (or match).

Two functions are possible only during two-cycle transfers: translate and automatic assembly/disassembly. During translate, each source byte is used as an index into a translation table from which the destination byte is derived. Automatic assembly/disassembly supports transfers between dissimilar bus widths, allowing 16-bit processors to interface transparently with 8-bit peripherals.

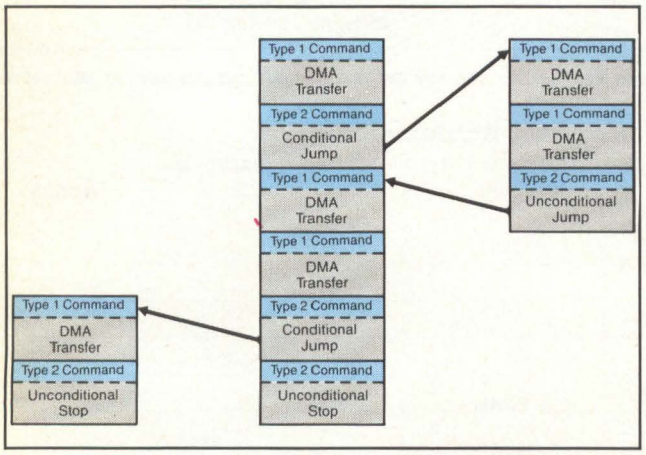

Figure 3: Command chaining uses two types of commands. Type 1 commands specify the DMA transfer and type 2 commands determine the flow of control. Complex "programs" can be described using command chaining.

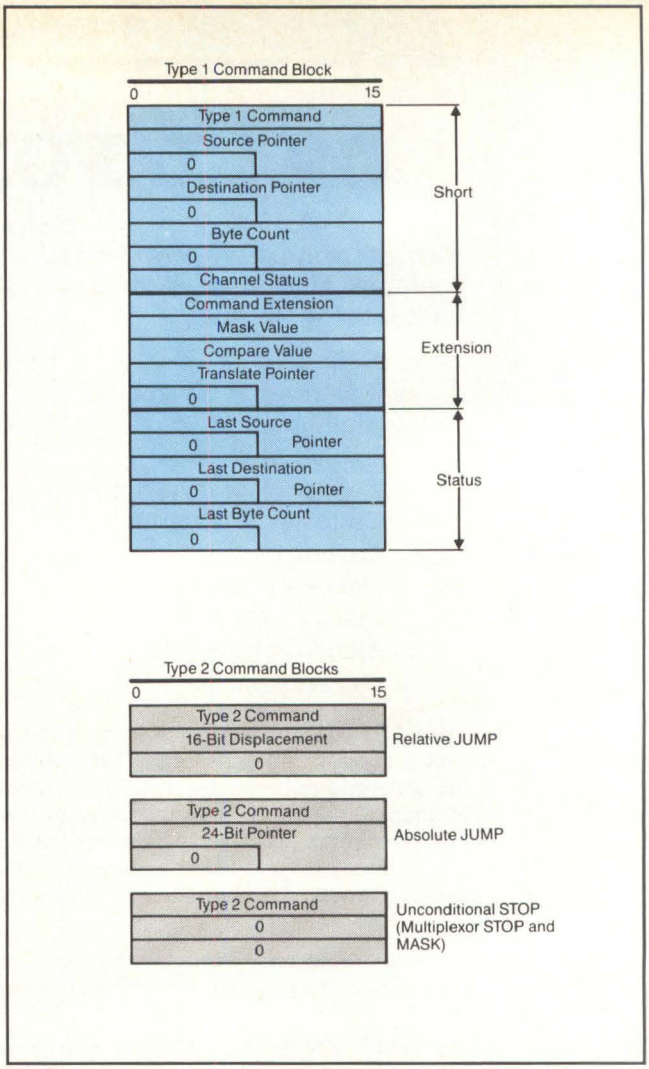

Figure 4: Type 1 short command blocks contain all of the parameters needed for a transfer. For simultaneous operations, the extension block is needed, and the status block is optionally included if specified in the command extension word. Type 2 command blocks specify jumps and stops which can be conditionally performed on status information.

System Configuration

A microprocessor system can be configured using the 82258 either remote or local. As a remote device, the DMA controller can act as an I/O processor and maintain minimum communication with the processor. In this mode, the processor can access its own resources over the system bus while the 82258 controller performs transfers across its resident bus on which its own memory and peripherals reside.

Alternatively, the 82258 can be installed for local mode operation, which has been optimized to support the 80286. For this mode, the 82258 is a coprocessor sharing the system bus resources with the CPU. These shared resources can only be referenced by either the processor or the DMA controller at one time, somewhat reducing system throughput. However, local mode uses less board space and minimizes chip count since the controller shares the bus support components of the processor.

In both local and remote modes, the main exchange of control information between the processor and the registers of the 82258 is through command blocks located in memory. The DMA controller can be mapped in either memory space or I/O space. The locations a controller occupies are decoded into its

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chip select signal, providing access to its internal registers. These registers are divided into a set of five general purpose registers and four independent sets of channel registers.

General registers specify system parameters such as channel priorities and bus widths, optimum bus loading, channel command (start, stop, single step) and current status. Channel registers (one set per channel) hold all of the transfer specific parameters like source and destination addresses, byte count, channel command and mask/compare values. All but one of these channel registers are loaded from the command blocks by the chip itself to execute the transfer. Therefore, the slave interface is used mainly to set the general registers and the channels' command pointers, or to examine the value of the registers during debugging efforts.

All of the information needed for the 82258 to perform a transfer is stored by the CPU in control blocks for each channel. After the command pointer register is assigned, the CPU reads the starting address of the command block and a start channel command is given. The controller then loads that particular channel's registers. When synchronized externally, the 82258 then waits to perform the transfer until it receives the DREQ (or IOREQ) from the device needing service. If synchronized internally, the 82258 begins the transfer immediately when the start command is issued. This is particularly useful for memory-to-memory transfers.

Command Structure

Command chaining is accomplished by placing individual DMA transfer command blocks sequentially in memory (**Figure 3**). In this way, once one DMA operation is completed, the internal registers are loaded from the next control block and the next operation is started. The 82258 knows that it must stop making transfers when it fetches a command block which contains a "stop" command.

Two types of command and associated control blocks are used in command chaining (**Figure 4**). A type 1 command block describes the actual transfer that is to take place, specifying the addresses and the byte count. If needed, the translation table pointer and mask/compare values are also included in an extended type 1 command block. A status word and, optionally, a status block are updated when the 82258 finishes the DMA transfer. Type 2 command blocks provide a mechanism to branch to another transfer or to stop the selector channel (or subchannel) currently running.

A type 2 command checks the information in the status register, which is written to the command block at the end of each DMA operation. The system then makes a conditional jump (absolute or relative) or a conditional stop. The four conditions which can be tested are termination due to reaching the byte count, a match or mismatch occurring in a mask/compare transfer, a mismatch occurring in a verify transfer and receiving an external end of DMA signal. Unconditional branches are also possible by testing all of the status bits since at least one will be set. This branching mechanism gives the 82258 the intelligence to perform sophisticated operations such as error detection and processing.

Data chaining allows the 82258 to organize data before and after transfers. For example, one block of data may need to be dispersed into several different blocks, or vice versa. This is called scattering and gathering of data. For DMA controllers with no data chaining capabilities, either separate transfers must be specified or the CPU has to manage the data blocks before and after the transfer. In contrast, the 82258 controls all of the scattering/gathering and only one DMA transfer command is needed. This is accomplished by regarding the source or destination address as a pointer to a list of data blocks. The list can be either a sequential list or a linked list (**Figure 5**).

Data blocks in sequential lists are described contiguously in memory, as if they were in an array. The 82258 transfers one block and then proceeds to the next one, needing only 1 μsec of linking time, until it sees a block which has a byte count of zero. Though the speed is attractive, it is difficult to perform insertions and deletions on sequential lists.

Flexibility is the overwhelming advantage of linked list chaining (**Figure 5**). Here, the structure describing the data blocks contains a pointer to the next block to be transferred, and insertions and deletions are performed by rearranging those pointers between blocks. The 82258 requires slightly more linking time when using linked list because of the additional pointer, but that additional time will be offset if the chain list is modified often.

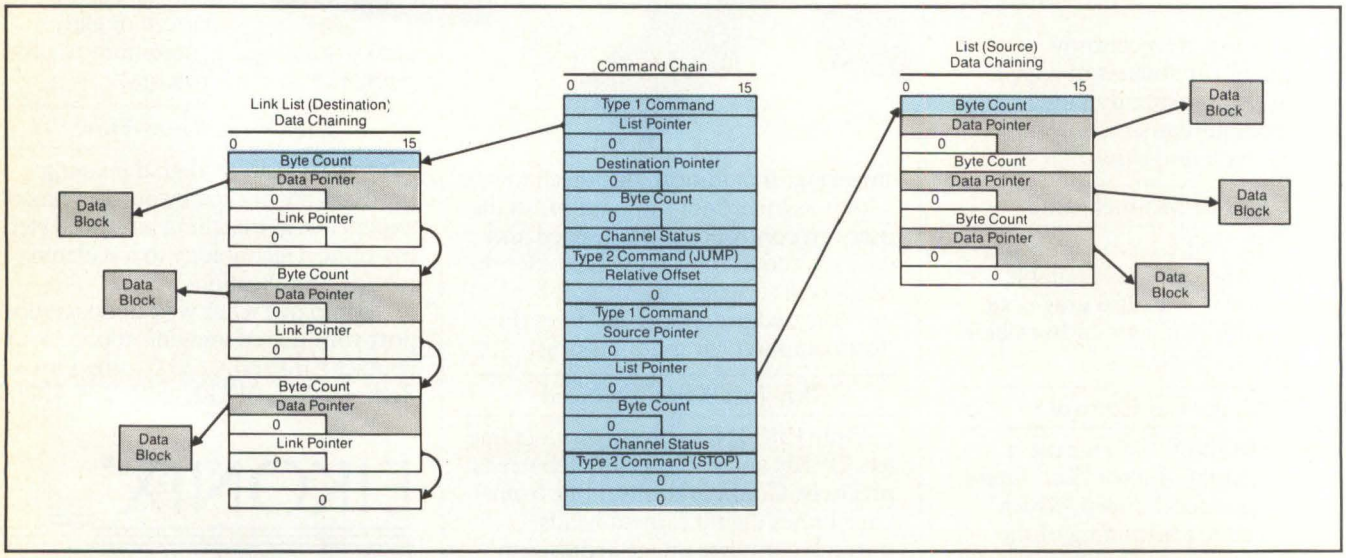

Figure 5: Data chaining gives the 82258 the capability to scatter or gather data blocks. Linked list chaining (left) is flexible, allowing insertions and deletions to be made easily. List chaining (right), however, requires less space and less linking time between blocks.

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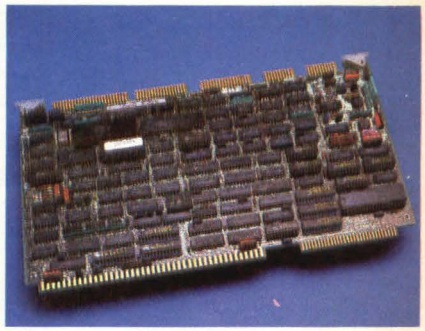

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80286 System Impact

The 82258 would work particularly well for high performance systems, in which peripherals tend to adversely affect system performance. A 80286-based multiuser engineering workstation running the UNIX or XENIX operating system (**Figure 6**) is a good example.

This workstation is well-suited to software development and hardware prototype testing. The resources needed for each of these applications can be separated into shared and dedicated. Expensive peripherals such as laser printers are often shared by many groups, most likely over a local area network. Low cost devices such as Winchester and floppy disk drives are tied directly to the workstation. The 82258 can support this variety of local and shared resources.

Fast devices are allocated to selector channels 0-2 of the 82258 because their performance depends upon fast transfer rates. Single-cycle transfers result in 8 Mbyte/sec bursts for one channel. Since both UNIX and XENIX systems heavily utilize the Winchester disk for code and data swapping, fast transfers are essential to system efficiency. However, if the DMA command block uses the verify or mask/compare features, the data rate will drop to 4 Mbytes/sec for two-cycle transfers.

Slower devices that generally require a lower burst rate are handled with the multiplexor channel. A combined data rate of 275 Kbytes/sec is supported by the multiplexor channel for single-byte or single-word transfers. This same data rate could also be achieved for a single subchannel burst. If each of the 32 subchannels maintained an asynchronous rate of 9600 baud (approx. 960 bytes/sec), only 23% of the 82258's channel capacity would be used. Consequently, selector channels would be able to obtain most of the chip's bandwidth.

The multiplexor channel will support all the user terminals of this multiuser workstation. In systems without a DMA controller, terminal I/O is typically handled through interrupts that signal the CPU that an external controller, such as the 8274 serial CRT controller shown, requires servicing. In its DMA mode though, the 8274 will issue separate requests for transmitting and receiving data. These requests are acknowledged with an encoding of the DACK signal from the 82258. By using individual requests, the DMA controller does not need to look at status information to determine which operation is requested. Consequently, the overhead involved in servicing requests is minimal.

An alternative approach to using two subchannels per CRT terminal is to use the single interrupt signal from the 8274 when it is in interrupt mode. The serial controller generates the single interrupt signal to request a transmit or a receive operation. To determine which operation is needed, the 82258 can read the status registers of the 8274 with a type 1 command. Using a type 2 command, the 82258 would then branch to the appropriate command block for the needed operation. Reading status information imposes overhead in manipulating the serial controller in interrupt mode, but it offers the advantage of using only one subchannel per terminal.

Because the 82258 uses 24-bit pointers to the data areas, it can address the same 16 Mbytes of memory and 64 Kbytes of I/O space that the 80286 can. The DMA controller, however, does not directly support virtual addressing of a processor running in protected mode. It performs its operations only with physical addresses that were translated by the 286 from virtual addresses. This is not a problem because the operating system kernel is responsible for checking all of the protection rules when command blocks are created. The kernel is the only software allowed to access the registers of the 82258. Therefore, the system will be secure even though the controller uses physical addresses.

Tight coupling between the DMA controller and the 80286 in local mode configuration saves space. Both the 82258 and

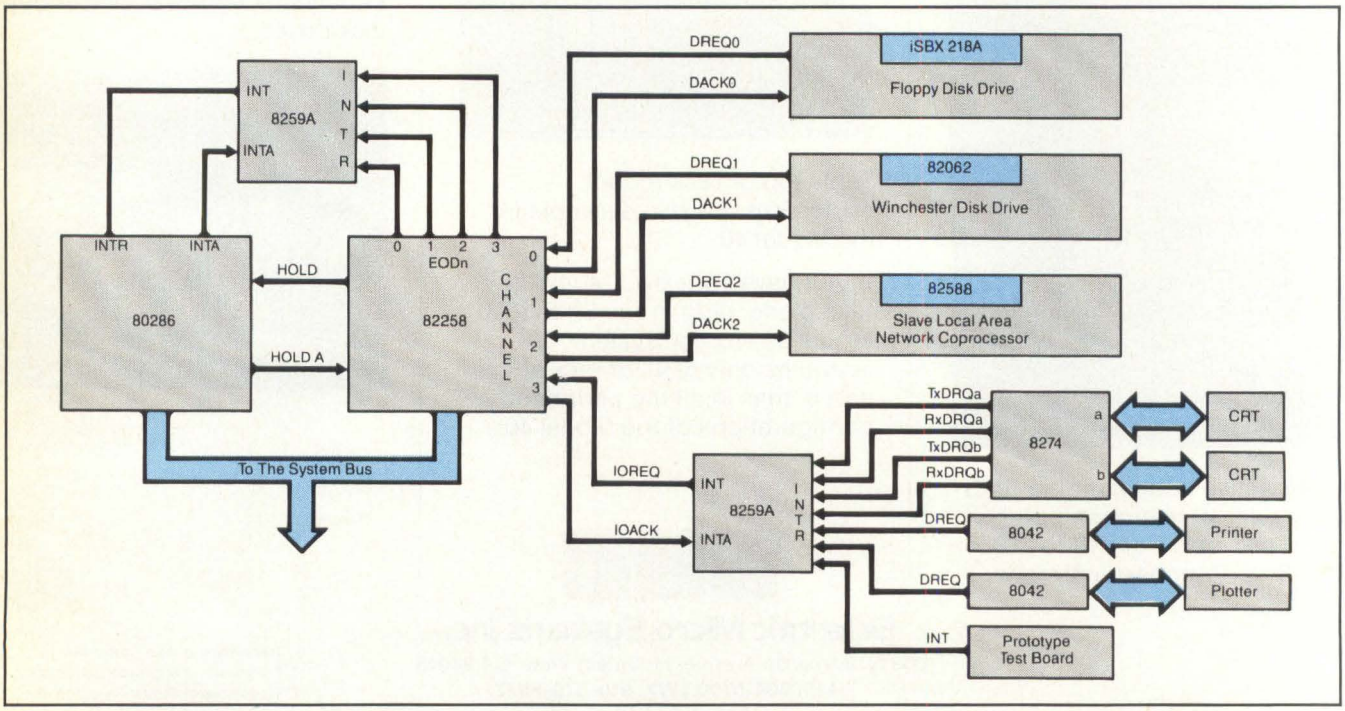

Figure 6: An 80286-based workstation provides an example of the benefits of using the 82258. Local mode gives a compact CPU-to-82258 interface while three selector channels and a multiplexor channel give fast service to a wide variety of resources. If channel 3 were not used as a multiplexor channel, it could be used as another selector channel.

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THE ARRAY PROCESSORS

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the processor use the bus support components; the 82288 bus controller, a 82284 clock generator, the 8282 latches and the 8286 transceivers are shared. This local mode of operation regards the 82258 as a co-bus master with the 80286 using the HOLD/HOLDA arbitration protocol. When the DMA controller wants control of the bus, it asserts its HOLD signal. The CPU responds with a HOLDA signal which allows the 82258 to take control of the bus. When the 82258 releases the HOLD, the 80286 regains the bus after inactivating HOLDA.

Division of bus utilization between the 82258 and the 80286 can be optimized by manipulating the values of the GBR (General Burst Register) and the GDR (General Delay Register). The GBR specifies the maximum number of continuous bus cycles for which the controller can control the bus. The burst counter is decremented by one for every bus cycle that the 82258 controls the bus. When its value reaches zero, the controller releases the bus and starts decrementing the delay counter which gives the minimum number of clocks between burst accesses. When its value reaches zero, both the burst and delay counters get loaded from the GBR and GDR, allowing the 82258 to request the bus, again using the HOLD/HOLDA protocol. These registers and their associated counters give the user programmable control of the system bus loading and prevent the 80286 from being denied access to the bus.

With the advent of the 82258, functions such as error handling and retry attempts are possible on a DMA controller. The command blocks that control the 82258 are prepared exclusively by the kernel of the operating system. The kernel builds the appropriate sequence of type 1 and type 2 commands in a memory area, then writes the starting address value of the command block to the CPR (Command Pointer Register) at the address at which the on-chip register is mapped. When a start channel command is then written to the CCR (Channel Command Register), the 82258 will wait for a DREQ signal if it is synchronized externally, or immediately begin execution of the command block if synchronized internally. Each channel and subchannel may use a separate command program.

A read from the Winchester disk illustrates how command chaining can be implemented to perform operations normally handled by the 80286 (**Figure 7**). Given a read command and its associated cylinder and head numbers, the 82062 Winchester controller retrieves data from the disk and puts it in an external sector buffer. The 82258 is then responsible for moving the data between the controller buffer and system memory. Before the transfer to system memory can be done, the DMA controller will check that no error was detected by the 82062 and that the data header matches what is expected. If there was an error in the disk controller operation, DMA execution stops. A mismatch between the header and the expected string results in the data still being transferred, but the MHeader variable is loaded with a value of all hex Fs. When the CPU receives the $\overline{\text{EOD}}$ interrupt from the 82258 signaling that the DMA was completed, it will be able to look at the status register, the CPR, and the value of MHeader to determine the cause of the DMA termination. Without command chaining, this complete read function would not be possible.

In the Winchester read operation, data could be used for the setup of a hardware prototype test board. The first section of the data sector describes the test parameters which the CPU uses to initialize the test vehicle. The two data blocks that follow the

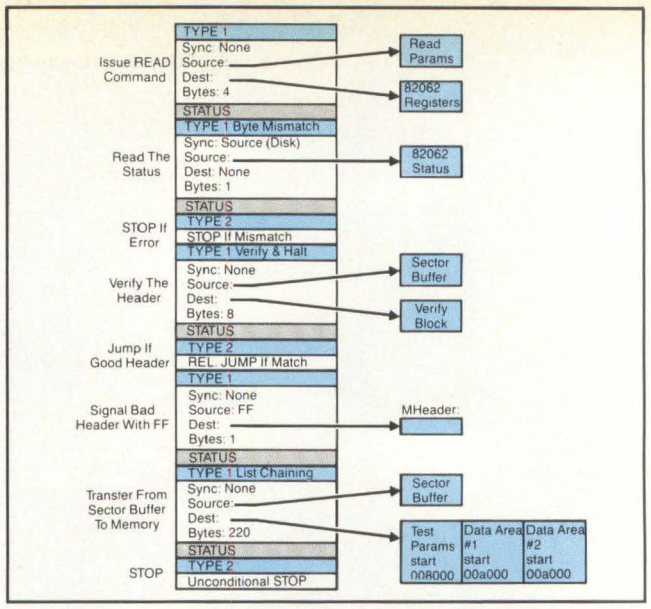

Figure 7: A command block that performs a read from the Winchester disk is easy to construct. The read command and its parameters are sent to the 82062 controller. The CPU can examine the command pointer to determine how the command block terminated. The variable MHeader indicates a mismatch of the header.

test parameters are actually manipulated by the test board and occupy noncontiguous addresses. Data chaining allows the data transfer to be specified with one command block, making efficient use of the control space. An alternative to data chaining is to use command chaining to simulate the function of a data list. However, this technique uses more space and requires more linking time than data chaining. List and linked-list data chaining provide an efficient and versatile method of scattering and gathering data.

Two variations of the standard transfer are shown in the disk reading example: transfers without a source and transfers without a destination. If specified in the type 1 command, the 82258 will take the value of the low byte or word of the source pointer and use it as a literal value which it will transfer to every destination byte, useful when initializing a data block to a particular constant. To read (not transfer) the value of a single byte or word, the type 1 command indicates that no destination is used. The data actually goes to the internal data assembly register (DAR) where a comparison can be made on it.

I/O On A Chip

As 80286-based systems increase in performance, corresponding I/O management capabilities are needed to support their performance. Jointly defined by Intel and Siemens, the 82258 is the result of an attempt to meet these requirements on a single chip. The 82258 provides 80286 and other iAPX 86 CPU systems a large bandwidth supported by its maximum transfer rate of 8 Mbytes/sec. Its four channels and unique multiplexor channel also allow systems to interface with a large number of I/O devices. **DD**

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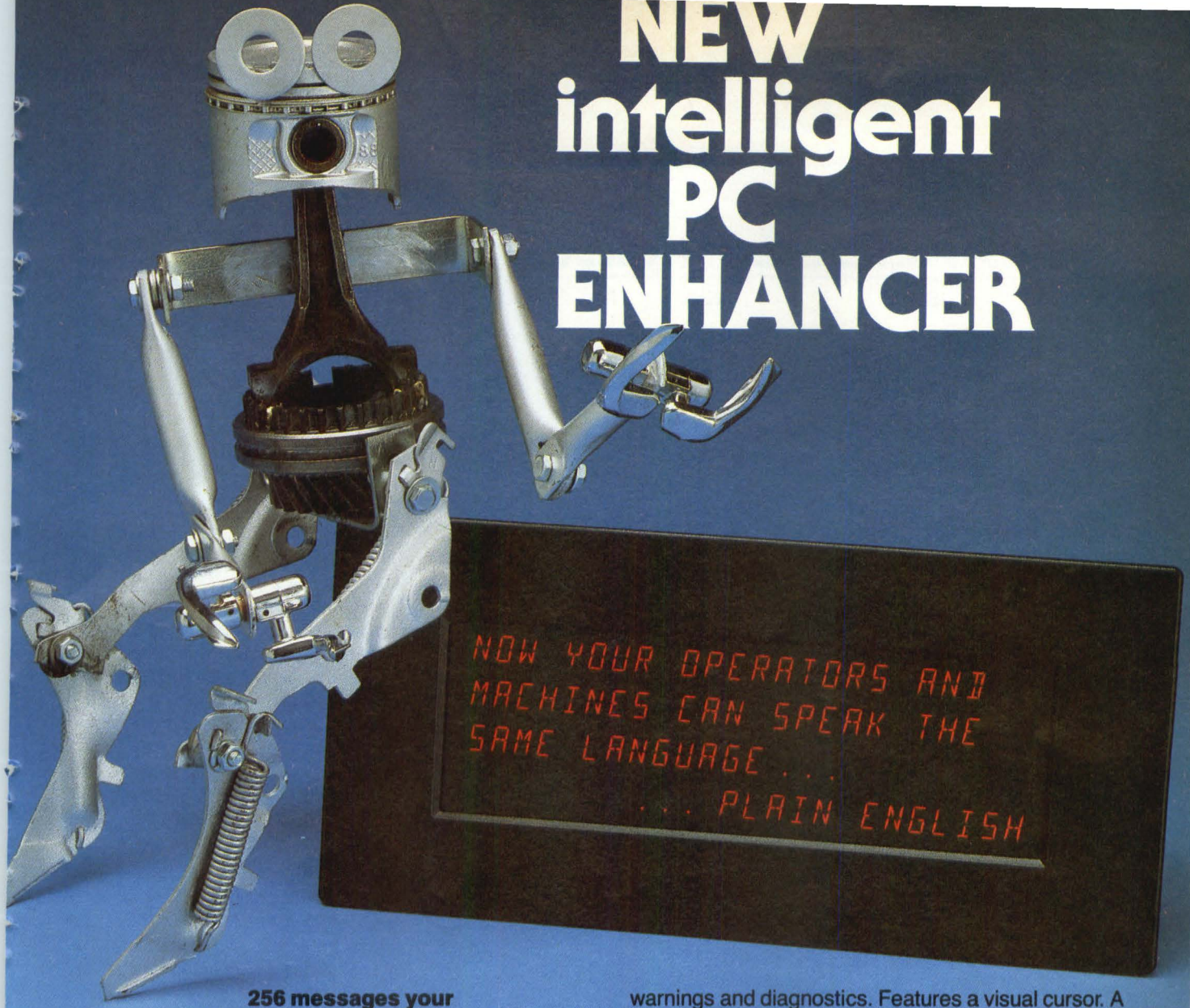

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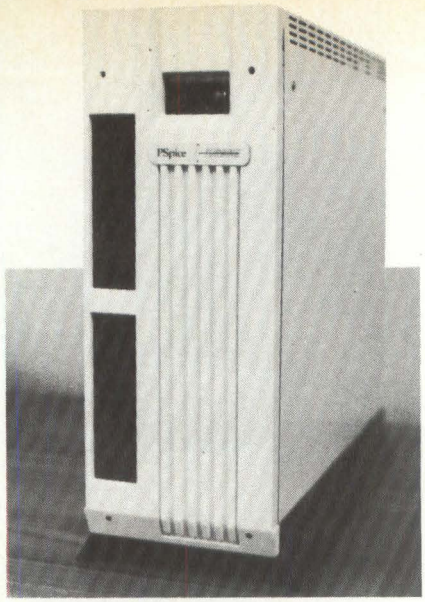


MicroSim Corp. (Tustin, CA) has developed the PSpice Turbine, the first accelerator designed for one of the Spice circuit simulators. With the Turbine, PSpice runs the same speed as Spice on a VAX 11/780 (with the floating point accelerator). This performance level significantly reduces expenses required for time sharing.

Housed in a standalone chassis about the same size as the IBM PC chassis, the Turbine interfaces to the PC through an interface card that plugs into a short slot in the backplane. A 6' ribbon cable in turn connects the card to the Turbine. With the exception of distortion (DISTO) analysis, PSpice offers all the capabilities of Spice. When using the Turbine, all PSpice features are available, including the User-Changeable Models option which allows a user to customize device equations through access to Fortran source code. Another option, the Probe graphics post-processor, supports the IBM color graphics adapter, the Hercules graphic adapter, the Okidata ML92 and ML93 printers and the Epson FX-80 and FX-100 printers. The current maximum circuit size when using the Turbine is 200 transistors.

Self-test diagnostics are performed whenever the Turbine is powered up. Upon failure, the faulty board will be bypassed, and the Turbine will continue to run at a slightly slower speed. The defective board can then be replaced at any time. The price for the PSpice Turbine (including the PSpice program and user's manual) is $19,500.

—Lamneck
Circle 230

SOFTWARE

Software Converts Fortran Programs To C

As the number of UNIX and C users increases, there is a trend to standardize the programming environment to support C and its utilities. A common problem has been the transition from one language to another. A major investment in programs written in other languages such as Fortran creates a problem: Should the programs be translated or should new programs be written from scratch? Although it has difficulty handling large programs, Fortrix-C from Rapidtech (New York, NY) offers a solution to this common problem by transforming Fortran programs and files to C.

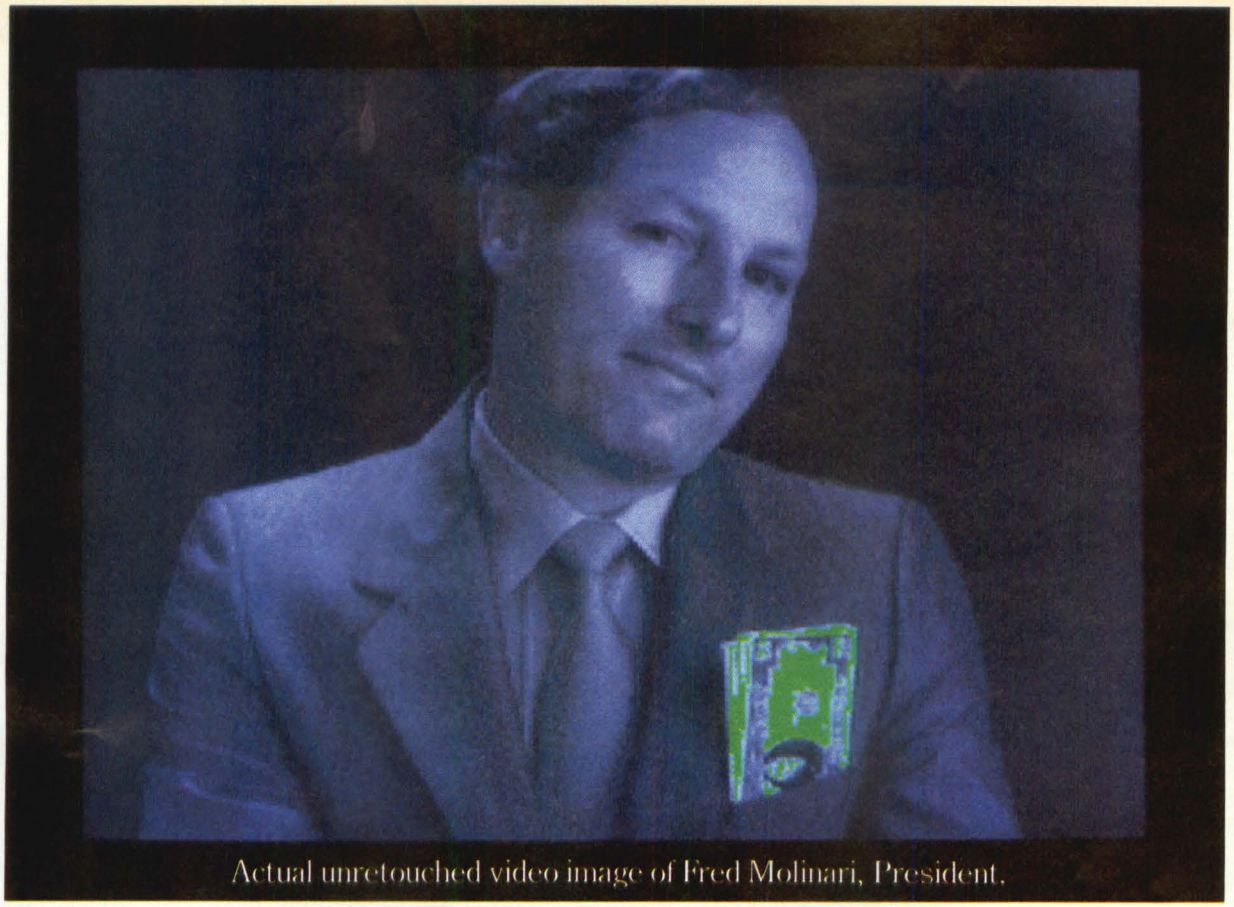
The operation of Fortrix-C is based on query. After asking for information about the program, such as whether it is a main program or subroutine, the program accepts the Fortran program line-by-line. A well-commented Fortran code will still retain its original comments into the C program. This process makes comparing code easy to debug and modify. The process of conversion involves parsing each line, identifying its function, determining the best appoach for converting and generating the C function.

Configured to meet the requirements of the UNIX environment, the package includes integer to string converters, space allocation and string parsers. All flow control statements, such as Do, Goto, If Else and Continue, are converted to the equivalent of C instructions and program format. Fortrix-C takes all functions and subroutines and recasts them as C functions. Dummy variables within the functions are identified by address so that variables may be passed between the program called and the calling program. All format statements are made into a separate file. This produces a modified Fortran-like file for processing. Fortrix-C also separates all Implicit, Common, and Equivalence statements and declarations into intermediate files. Warning statements and queries of ambiguity are created during conversion. Error validation is incorporated because of the parsing process. Several types of errors are trapped and flagged with diagnostic constructions for debugging.

The C code produced by Fortrix-C is longer than Fortran when converting I/O calls. The loadable module occupies about 35% less disk space because Fortran does not show all of its I/O processing in its source code. Rapidtech claims the resulting C program runs about 15%-30% faster than its Fortran equivalent and transfer rate is 600 lines/min.

Fortrix-C requires a good understanding of Fortran and is available in three versions: -C, -C+ and C'. The -C version is standard. The C+ version includes the ability to handle Common and Equivalence statements and provides for character and I/O control. The C' is all of the above for a non-UNIX system. The program is available in either disk or tape format.

—MacNicol
Circle 234



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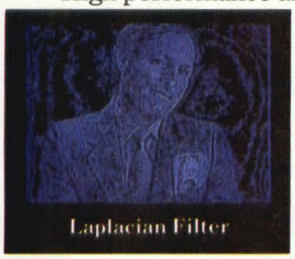

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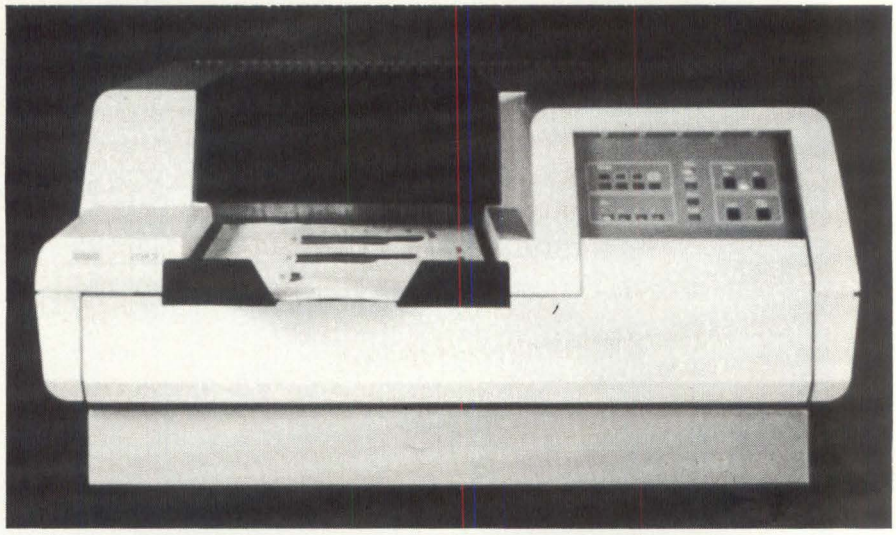
Ink-Jet Printer Combines Color Printing And Graphics Processing



Designed for use as a shared resource, Digital Equipment Corp.'s (Maynard, MA) LCP01 ink-jet color graphics printer produces color output on both paper and transparencies. It contains an integral on-board J-11 graphics processor that handles the display file processing of REGIS, GIDIS, NAPLPS or Color Sixel formatted data and a page buffer memory that takes the burden of the graphics processing off the host system.

Working with the VAX, PDP-11 and Professional 350 computers, the printer connects to the host CPU by a standard serial-line interface (RS-232-C or 20 mA). With a print resolution of 154 dots per inch, the LCP01 produces eight true colors (yellow, magenta, cyan, red, blue, green, black and white) in up to 216 combinations and shades. Print image resolution is 1536 × 1152 dots (maximum). Hard copy graphics are produced in approximately two minutes per copy on A or A4 size paper. The printer feeds, processes and stacks 100 sheets of paper or 50 transparencies automatically; transparencies are completely dry when taken off the printer. The LCP01 also features self-test diagnostics.

The LCP01 is compatible with PRO/GIDIS (Graphics Interface Descriptor Instruction Set); DECslide, a menu-driven text and diagram-generating tool; DECgraph, an interactive business graphing tool that generates six different types of graphs; and Datatrieve office software. Price for the printer is $14,595.

—Lamneck

Circle 231

Controller Sustains 8.1 Mbyte/sec Data Rate

The Concept 21 from Storage Concepts (Costa Mesa, CA) represents the first off-the-shelf disk subsystem to support a sustained transfer rate of 8.1 Mbytes/sec for the M2350 parallel transfer disk drive from Fujitsu America (Santa Clara, CA). Intended to support the real-time needs of such applications as image processing and satellite communications, the controller also handles burst transfers as high as 9.3 Mbytes/sec when all five of the disk drive's read/write channels operate at their 1.86 Mbyte/sec peak transfer rate. Previous implementations required several disk drives and several disk controllers to achieve multichannel operation.

Central to the design of the disk controller is a 80 word by 16 byte FIFO that buffers the data being transferred from the disk for easy handling by the dedicated processor. As a result, sustained or burst data transfers occur even during track-to-track seek operations. Furthermore, the Concept 21 formats disk surfaces (20 in all) in such a way that data transfers continue after one-half of a disk revolution rather than a full revolution. By staggering the zero logical sector from cylinder to cylinder, track-to-track seek times are minimized as each succeeding cylinder is at a minimum physical distance away from the next zero logical sector.

Users can also access the disk drive's 474 Mbyte storage capacity in a single-channel mode for data transfers to the host computer requiring less than the full data transfer speed. The controller uses separate buses for commands taken from the host CPU and the actual transfer to the dedicated processor. The host adaptor communicates with the system bus at a rate of 1.8 Mbytes/sec, with the high-speed port operating at 8 Mbytes/sec. As a result, high-speed transfers incur no overhead on the host system bus once the command has been issued.

The Concept 21 follows error correcting code and data and cycle redundancy check on headers in both system disk and data disk operating modes. Layered error handling and sector skipping specifications have been defined with an emphasis on five channel operation.

No extensive modifications of existing device drivers are needed other than a small device driver that links its 50-pin data and command bus to the host adaptor. The commands that need to be implemented are limited to diagnostics and maintenance (e.g., format bad sector), head positioning while seeking and read/write operations in single channel and five-channel modes. In addition, the controller can support as many as four parallel-transfer disk drives.

—Aseo

Circle 235

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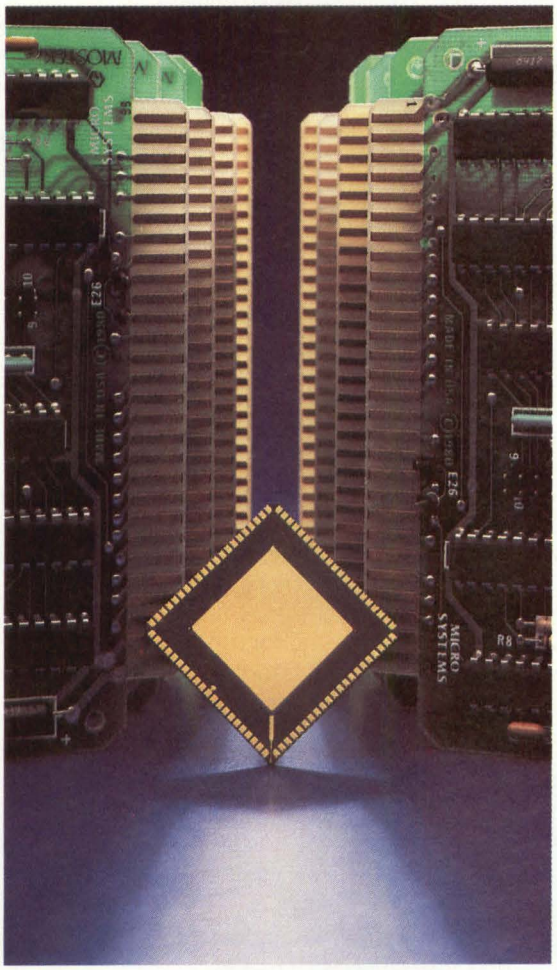

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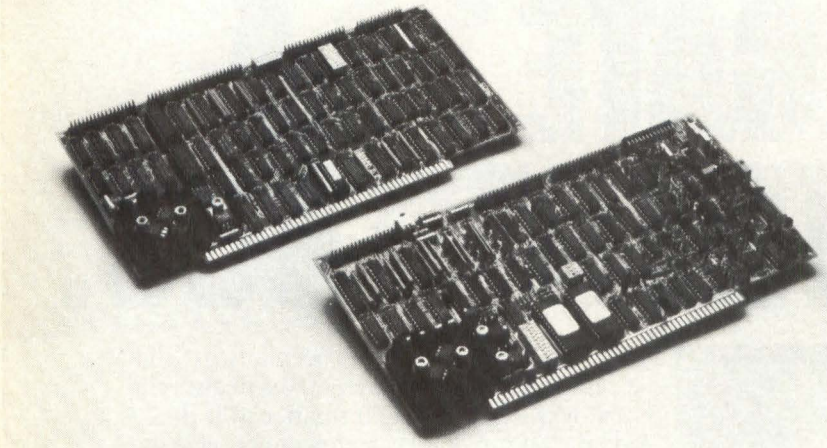
Graphics Boards Support Video Applications



Two of the four new video support graphics boards from Cromemco.

The computer graphics marketplace is becoming more diverse and segmented because generic graphics hardware cannot do all things for all users. Video is an important and sometimes overlooked segment of this market. The hardware for video systems represents different architectural concerns. The resolution of a video-oriented system is fixed below 525 lines, and the importance of colors, frame capture, signal quality, speed and versatility is higher and different than with CAD systems.

Two board manufacturers recently introduced products supporting video functions: Cromemco (Mountain View, CA) and Parallax (Sunnyvale, CA). Cromemco has four new boards that use the S-100 (IEEE-696) bus which, combined with their SDD digitizer board, forms the company's S-series of graphics interface boards. The four boards, which support either NTSC (National Television Standards Committee) or PAL standards of video transmission, are a video generator, a video memory controller, 256K of dual-ported memory and a color modulator board. Together the boards provide a 256K color palette with image overlaying, full color digitizing, 4-1 continuous zoom, panning and scrolling and image wrap-around.

The video generator and memory controller work together to form the basic system that generates a 756 × 484 pixel display from a 1024 × 1024 image space. Three memory controller boards can be combined for independent zooms and pans. The dual-ported memory allows access or update of the image by the CPU or DMA device, and up to six can be used simultaneously. The importance of dual-ported memory means that the display board can be accessing memory while the CPU may be modifying the data. The net result is higher speed of operation. The modulator board takes the RGB signals from the video generator board or another source and converts it to a professional quality composite signal.

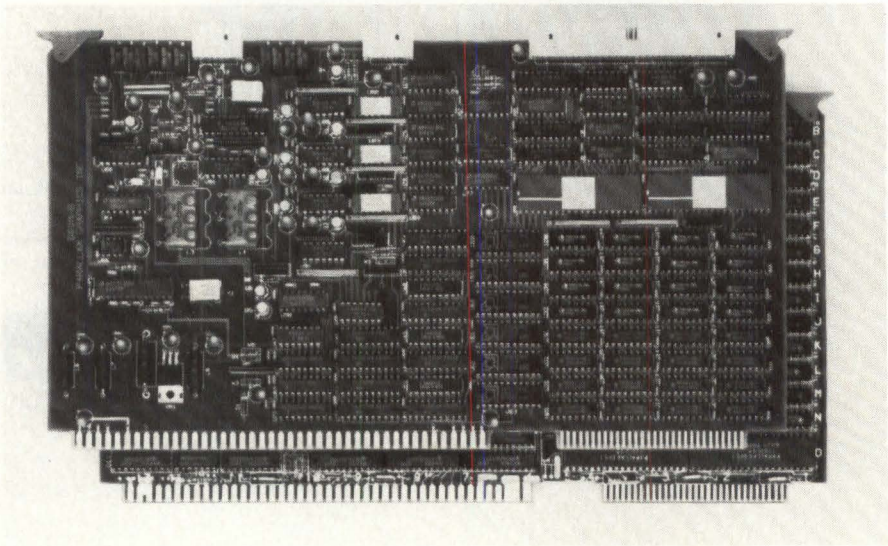
Each graphic memory board holds 512 × 1024 4-bit nibbles or image space. If two boards are used, either a 1024 × 1024 × 4-bit or a 512 × 1024 × 8-bit image can be stored. Four boards can store a full 1024 × 1024 image with the capability of displaying 256 simultaneous colors. The digitizer board of S-series is capable of accepting a color camera or VCR input and outputs an RGB signal for computer manipulation, display or special function device. Together, the system is capable of creating special effects, interactive graphics for training, pattern recognition and simulation.

The video board from Parallax is actually an extension of their 600 series of their Multibus-based graphics display system. The board is designed for real-time video digitization in a professional environment. The video circuitry resides on the 600-8 which is an add-on board. It makes the standard 16 color board (600-4) into a 256 color (8 bits each for RGB) system.

The capabilities of the graphic display system allow NTSC signals to be an input or output. The NTSC input signal is decomposed into its RGB components and control of hue, saturation and contrast is adjustable via trimpots on the edge of the board. For black and white signals, a 6-bit gray scale is used. The color scaling is a mapping of 6 bits of RGB into 3 bits of R and G and 2 bits of B. The estimation of colors can be increased in apparent quality through hardware dithering. Dithering is the process of redistribution of colored pixels to increase the apparent depth of colors through the creation of mixed intermediate colors. One of the colors can be used as video for overlaying. The overlay generator is a 2:1 digital multiplexer that mixes the digitized video signal with the color map of the 600.

—MacNicol

Cromemco **Circle 232**
Parallax **Circle 233**



The 600 series video/graphics controller from Parallax.

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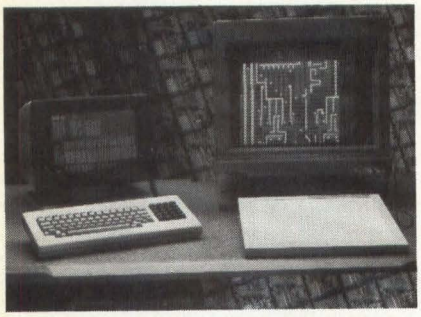


Powered by the Data General 32-bit DS/4000 CPU, the GDSII/32 workstation is linked to larger GDSII systems based on the DG Eclipse computer. The system includes 2 Mbytes of RAM, a hardware floating point accelerator, a 737 Kbyte floppy disk drive, a 15 Mbyte cartridge tape unit, two 5¼" Winchester disks with a total of 210 Mbytes and an integrated I/O controller board. The GDSII/32 also offers a graphics display terminal with 1024 × 1280 resolution, 60 Hz noninterlaced color monitor and 4-bit planes. Price is around $95,000. **Calma**, Santa Clara, CA **Circle 156**

Supermicros With 16 Mbyte ECC RAM

Available with 4, 8 or 16 Mbytes of error-correcting RAM, the CS-400 Supermicrocomputer offers a choice of a 140 Mbyte or 280 Mbyte high speed hard disk drive, controlled by the STDC controller, with cache memory. The system comes with a standard 5¼" floppy disk drive (390 Kbytes) and a 32 Mbyte cartridge tape drive for backup. All models are delivered with UNIX System V installed and have a capacity of 21 boards. **Cromemco**, Mountain View, CA **Circle 163**

Infrared Spectral Analyzer

Designed to make measurements from .7 to 20 microns, this dedicated spectral radiometer, Model SA-1 Infrared Spectral Analyzer, offers a choice of fields-of-view, spectral regions and detectors. Consisting of an optical head and electronics, the Model SA-1 can display either volts, irradiance, radiance or temperature for any spectral region. The standard instrument uses a 1 cm diameter collecting optics which gives the system a 2° field-of-view. **Minarad Systems**, Fairfield, CT **Circle 195**

UNIX/Coprocessor Subsystem

Designed to convert an IBM PC to a 32-bit UNIX workstation, the Opus 516 Personal Mainframe consists of a complete port of UNIX System V (Release 2.0) and a 32-bit coprocessor for the IBM PC and plug-compatible computers. The coprocessor is based on National Semiconductor's Series 32000 chip set. With standard memory management and floating point processing capabilities, memory on the Opus 516 is expandable to 2 Mbytes. Also included are C and Fortran 77 compilers, an assembler and debugger. Price is $3,140. **Opus Systems**, Los Altos, CA **Circle 219**

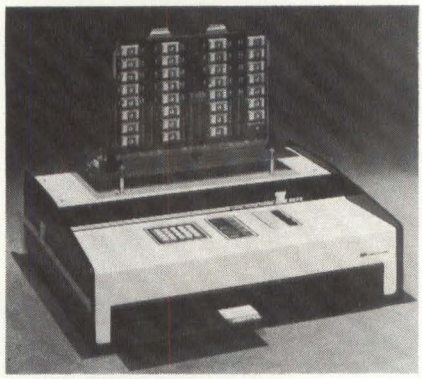
Raster Graphics Workstation

Introduced as an alternative to the IBM 5080 Graphics System, this raster graphics workstation, the 6080, is based on the "Ocean" graphics engine. The 6080 features a 50 nsec/pixel drawing speed, local pan/zoom/scroll and local highlighting techniques. Among the software packages that run with the 6080 are CADAM, CATIA, Integrated Prance CADAM (iPC); CBDS2, CAEDS, McAuto's Unigraphics and Precision Visuals' DI-3000. With 256 Kbytes of system memory, expandable to 1.25 Mbytes, the 6080 includes a 19", 1024 × 1024, 60 Hz noninterlaced display with antiglare screen. Prices range from under $18,000 to $22,000. **Adage**, Billerica, MA **Circle 215**

XENIX 3.0-Based Multiuser System

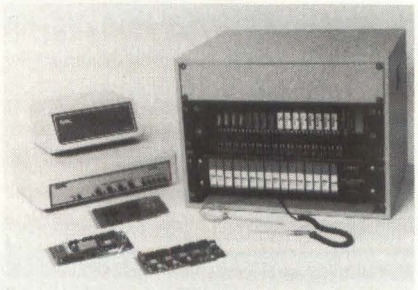
Supporting up to four users with expansion available for up to eight users, this multiuser supermicro system uses MicroSoft's XENIX Release 3. The Esprit X16 implements a network-in-a-box architecture and uses terminals as user workstations. With an 80186 16-bit μP, the X16 comes with 512 Kbytes of RAM standard and 13 offered with 40 Mbytes or 105 Mybtes of 5¼" Winchester disk storage. Providing a parallel printer port and an RS-232 serial port, the X16 offers an optional Multibus-compatible expansion chassis with six slots for Multibus-compatible boards. Price is $9,000. **Esprit**, Montgomeryville, PA **Circle 216**

In-Circuit Programming System



Designed to program several boards at once and up to 32-bit-wide words in its standard configuration, the Z-2500 In-Circuit Memory Board Programming System is a disk-based bench-top, programmer. Housed in a ¼" thick aluminum chassis containing a 125W switcher, two 8" double-sided, double-density disk drives, 64K RAM and a Z80A-based computer, the system is self-calibrating, using a built-in .05% reference. **Sunrise Electronics**, Glendora, CA **Circle 157**

IBM PC Data Acquisition/ Control Signal Conditioning System



The Analog SC Series of rack mounted signal conditioning products includes a variety of modular plug-in input and output capabilities for direct conditioning of thermocouples, RTDs, Strain Gages, mV Frequency and 4-20 mA process signals. SC backplanes are designed to accept direct sensor input and provide cold junction compensation for thermocouples and excitation voltages for 2-, 3- or 4-wire RTDs and strain gages. All analog SC modules are fully isolated to ±1500 VDC and operate over a -25°C to 85°C range. **Cyborg**, Newton, MA **Circle 164**

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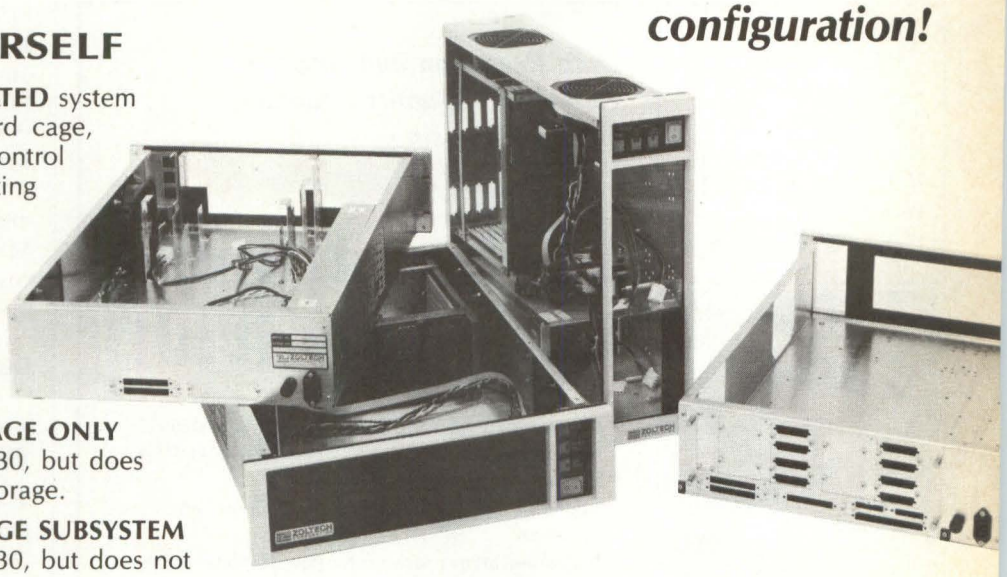

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Zoltech manufactures a variety of systems and other Q-Bus related components. The VQ-11 system packages are designed to maximize reliability and versatility while minimizing cost and lead time. **Call or write** today for a quote or for our catalog of system packages, boards, drives, software and accessories available for your Q-Bus needs.

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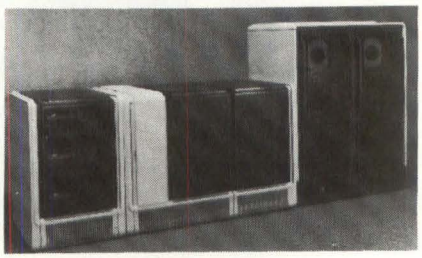
Circle 12 on Reader Inquiry Card

NEW PRODUCTS

Enhanced Supermini

Enhanced to support up to 16 Mbytes of directly addressable memory, the Model 3210 superminicomputer is part of Perkin-Elmer's Series 3200 family. Using the firm's OS/32 operating system, the Model 3210 runs all PE languages including its Fortran VII family, Pascal, COBOL, Basic and Coral 66. The XELOS operating system, a derivative of AT&T's UNIX System V, is also available for the Model 3210. Other members of the PE Series 3200 family of superminis include the 3205, the 3230, the 3250XP and the 3200MPS. **Perkin-Elmer**, Oceanport, NJ **Circle 218**

High-End 32-Bit Supermini



An enhanced version of the company's MV/1000 supermini, the Eclipse MV/10000 SX superminicomputer is based on a single-board processor that uses ECL macrocell microcircuitry developed by Motorola. Also announced are 256 Kbyte DRAM-based memory boards (4 and 8 Mbytes) that enhance the maximum configurability of the Eclipse MV/10000 SX to 32 Mbytes. The coprocessor has a dedicated control store and microsequencer to store and execute its own 115-line microcode instruction set. **Data General**, Westboro, MA **Circle 158**

Briefcase-Size PC

The latest addition to the TI PC family, the Pro-Lite computer features a 12″ LCD that shows 80 columns × 25 lines. With up to 768 Kbytes of RAM, the Pro-Lite can accommodate software packages like Ashton-Tates' framework. The entry-level configuration includes 256 Kbytes of memory, a 16-bit 80C88 CPU, with an 80C87 numeric coprocessor available as an option. The 10.5 lb Pro-Lite has a single, 3½″ floppy drive; diskette storage capacity is 720 Kbytes. A second disk drive and a battery pack can be added and an optional 300 baud modem is also available. Price is $2,995. **Texas Instruments**, Dallas, TX **Circle 217**

Can you picture a single-board PC graphics controller with 32-bit planes?

© Image courtesy of Artronics/3M by Scott Lewczak.

The New REVOLUTION™ 512 x 32.

We built a combination of advanced capabilities into the latest Revolution board... like our unique megabyte of multi-ported display memory, 16 million colors with overlay capabilities, hardware zoom and optional video broadcast compatibility. The kind of architecture you'd like to specify for your system needs.

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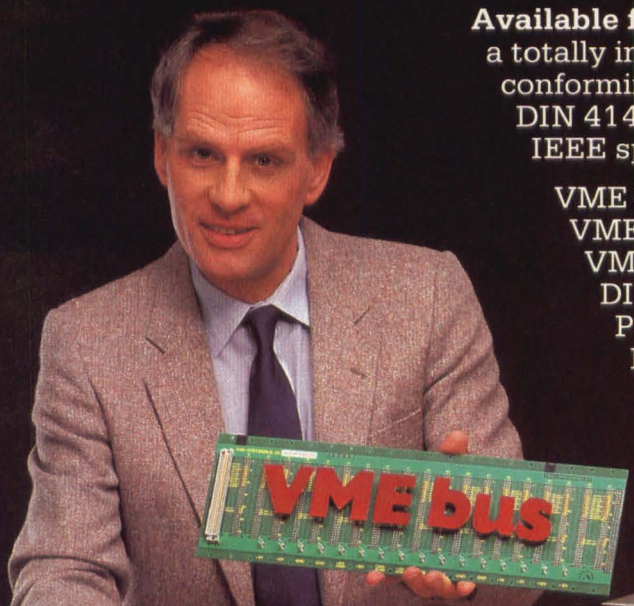

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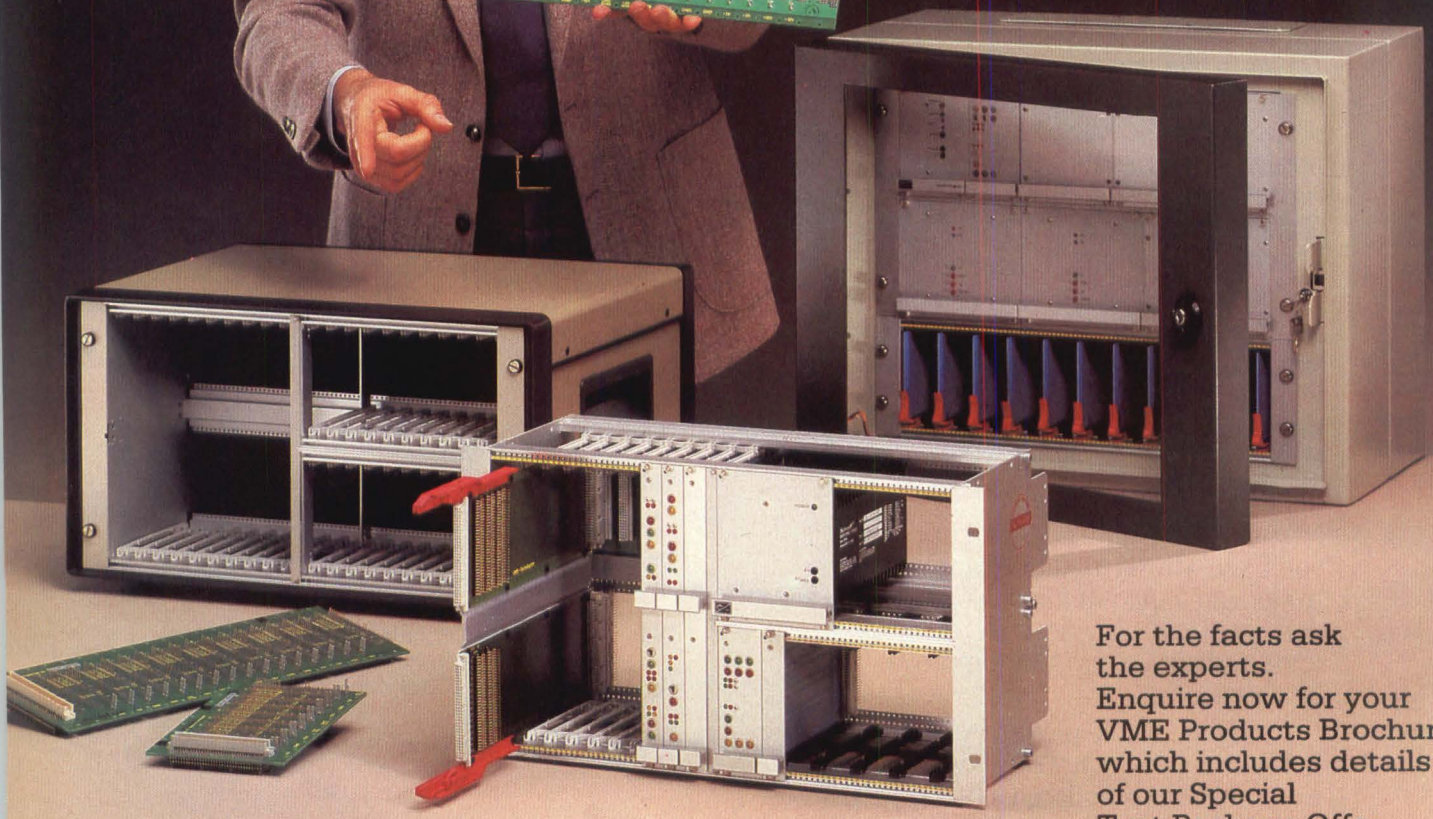

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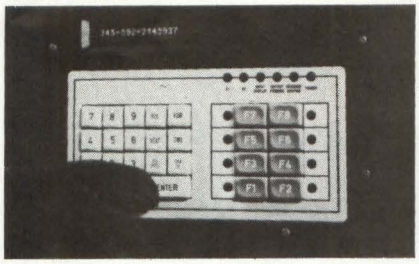
NEW PRODUCTS

PERIPHERALS

Compact Modems

Converting data for transmission over leased telephone lines between terminals and host computers, these modems (the 3833 and the 3834) operate at 2,400 bps and 4,800 bps in networks using sync data transmission. These shoebox size modems are fully compatible with IBM communication network management and problem determination programs. The units also include an extended diagnostic function which permits remote diagnostic tests. Price is $1,700 (3833) and $2,600 (3834). **IBM**, Rye Brook, NY
Circle 169

Microterminal



Requiring only one host communications port or multidrop address, this Microterminal, the TM200, provides a data entry and display station with I/O capability. Internally, it consists of a logic board and a keyboard/display module. The 0.21″ high 40-character green vacuum flourescent display can be read from a distance of 10′ in a variety of ambient light conditions. The display message, up to 80 characters long, can be scrolled bidirectionally. **Burr-Brown**, Tucson, AZ
Circle 178

3½″ Microfloppy Drives

Featuring a 3½″ format, the YD-600 Microfloppy disk drives are offered in two models: the YD-620/25 providing 0.5 Mbyte on 80 tracks and the YD-640/45 with 1.0 Mbyte double-sided storage on 160 tracks. The drives are interface-compatible with most 5¼″ drives and consume 3W power. With MTBF of 10,000 POH, transfer rate for both models is 250 Kbits/sec. The YD-620/25 has a 5 msec track-to-track access time and a track density of 67.5 tpi with an 8547 bpi recording density. The YD-640/45 has a 3 msec track-to-track access time and a track density of 135 tpi with an 8717 bpi. **C. Itoh**, Los Angeles, CA
Circle 213

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Maxi-Switch is out front in keyboard technology

Have you taken a close look at Maxi-Switch lately? We're the company that introduced conductive elastomer keyboard technology in 1981. Maxi design leadership is proven on the job, every day, in thousands of terminals and personal computers

Our conductive elastomer switch features "Maxi-Touch," with unique tactile response. It's rated at over 50 million cycles. Typists appreciate the comfortable low-profile design and smooth key action. Engineers appreciate the new technology, its simplicity and long life.

This keyboard is offered in an IBM PC format for OEM customers, and with a matching enclosure, cable and connector for PC and PC-XT keyboard replacement. Users can choose the standard keytop layout, an enhanced version, or the increasingly popular Dvorak format.

Apply Maxi's conductive elastomer keyboard technology to your keyboard problems. Call the Leader for price and delivery.

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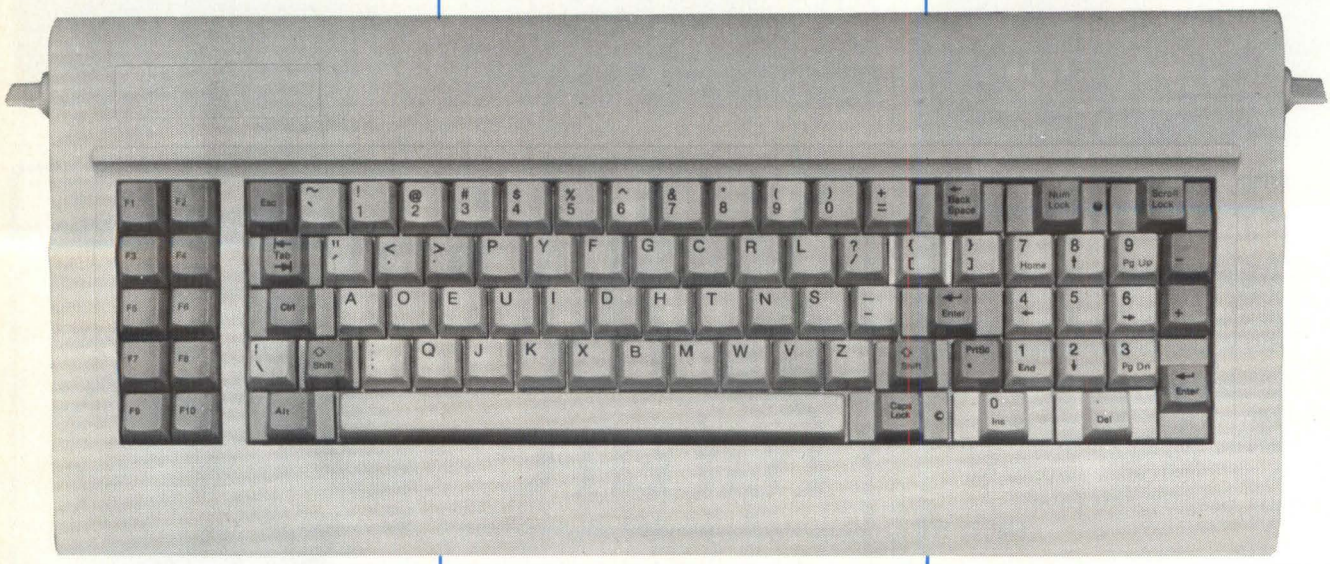

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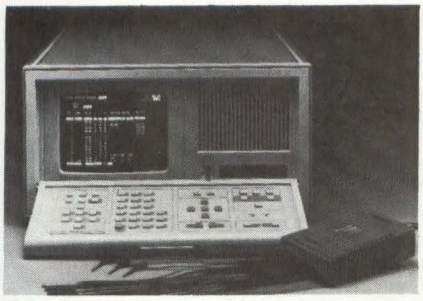
50 MHz Pattern Generators



Used as standalone stimulation sources or linked with data acquisition to provide a test system for debugging and verifying components, boards and systems, these pattern generation modules (91S16 and 91S32) operate at up to 50 MHz. The 91S16 module features 16 data channels of algorithmic pattern generation along with two strobes and two clocks. The 91S32 offers 32 data channels (stored pattern generation), four strobes and four clocks. Prices are $6,900 (91S16) and $10,400 (91S32). **Tektronix**, Beaverton, OR **Circle 159**

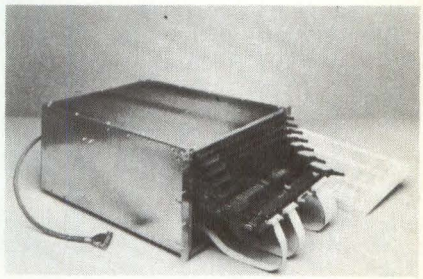
Full-Function Industrial Computer

Designed for mid- to upper-range industrial automation applications, this mid-range dedicated computer, the 984 Programmable Controller (PC), offers options for machine diagnostics and arithmetic equations. Communications capabilities include three built-in ports that allow two users to extract information from the PC through host computers. The 984 also incorporates a tamper-proof memory, bit slice technology and a hand-held data access panel. Price, with 16 Kbytes memory, is $6,200. **Gould**, Rolling Meadows, IL **Circle 155**

Data Acquisition/Control System

This data acquisition system (Model 1150) collects analog and digital data, compares it with previously programmed limits, generates control actions based on the comparisons and reports the collected data and control actions over the IEEE-488 GPIB. A GPIB system controller may be programmed to scan analog and digital signals to detect any out-of-limit states, at which time the system controller assumes control as necessary. Price is $1,895. **Racal-Dana**, Irvine, CA **Circle 165**

Database Hardware Sorter



Designed to offload a host's data sequencing overload and accelerator database set operations, the DBA 1000 Database Accelerator consists of a front-end processor, memory control unit and from one to five self-sorting memory modules. The front-end processor, incorporating the 80186 μP and multiported memory, communicates via Ethernet LAN with the host. **Accell Technologies**, San Diego, CA **Circle 161**

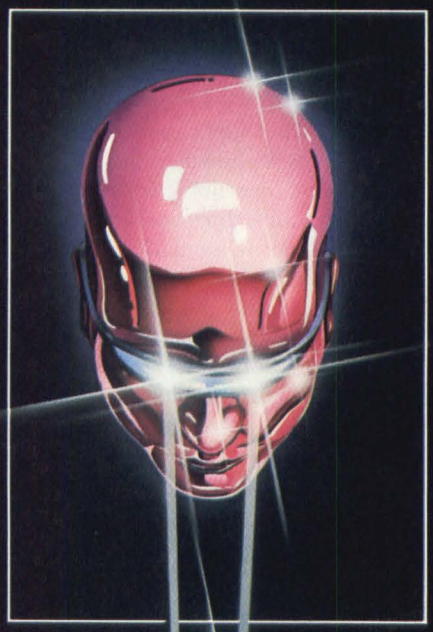
The Convergence Factor.

Convergence: the single most critical factor in color CRT performance.

Until now, Delta-gun tubes were the best way to achieve near perfect convergence, but only with costly adjustment electronics. Meanwhile, many in-line tubes are plagued by perceptible misconvergence. Which can lead to poor picture quality. A poor quality image for your product. And poor, bleary-eyed operators.

The Panasonic achievement: low cost in-line color CRTs with better-than-Delta convergence performance.

Without complex adjustment electronics . . . and none of the convergence drift inherent in active correction systems. At last, high resolution in-line tubes with stable performance that stands up to the ravages of time and tough office/industrial environments.



How did we do it? With a preconverged in-line tube/yoke combination unlike any other. Our precision S/ST (saddle/saddle toroidal) deflection yoke is ideally matched to each tube, for near perfect convergence, high repeatability and stability over a wide range of operating conditions.

We combine it with a specially-designed OLF (overlapping field lens) gun and unitized grid construction, providing spot uniformity across the entire screen and near-Delta resolution.

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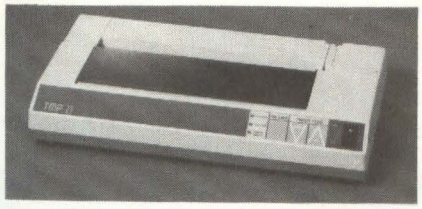
Portable Thermal Printer



On ordinary or thermal paper, this thermal/thermal transfer portable printer, the TMP-21, prints 80 cpl with a 16 × 10 dot matrix. In the graphics mode it performs bit imaging with a 16 × 960 matrix. The TMP-21 prints at 30 cps and is capable of standard or enlarged 40 cpl printing. The battery-powered unit uses 4 C cells or an optional AC adapter. A standard parallel-Centronics interface or an optional RS-232 interface is available. Price is approx. $200. **Acroamatics**, Danbury, CT **Circle 168**

Dot Matrix Printers

These 3000 Series printers, offering speeds from 45 to 400 cps, are included in the Tempest product line. The 3184, 3304 and 3404 are among the new additions to the Tempest Series. Each model offers draft printing at speeds from 180 to 400 cps, letter quality printing from 45 to 100 cps and high resolution dot addressable graphics. Available options include fonts, eight color process printing and paper handling accessories. **Genicom**, Waynesboro, VA **Circle 176**

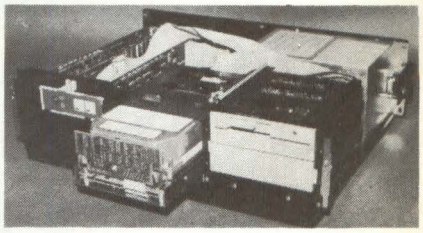
GCR Tape Subsystem

An addition to the firm's Shamrock GCR tape subsystem family, the Model 9270 Shamrock is a 75 ips start/stop, autoload/autothread vacuum column tape drive with embedded GCR formatter. Dual and tri-density models (6250/1600/800 bpi) are offered. The peak throughput rate at 6250 bpi is 468.7 Kbytes/sec. Fully compatible with the 9250, 50 ips start/stop tape drive family, the 9270 offers Pertec STC and Telex interfaces. The Price is $15,899. **Telex**, Tulsa, OK **Circle 175**

1600-Line High-Resolution Video Camera/Monitor

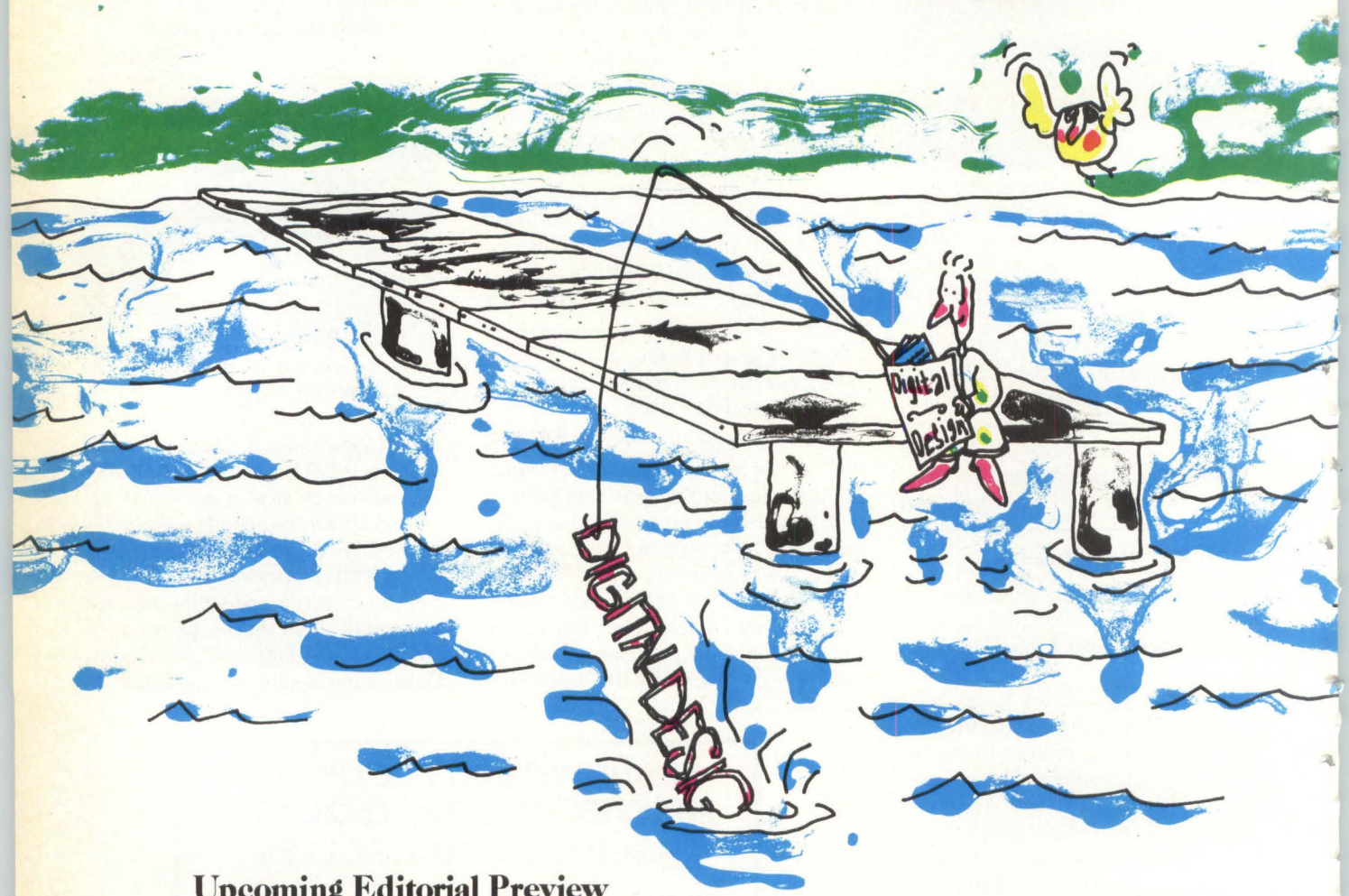
Achieving 1600-line resolution, this video camera, the Precision 81, features multirate scanning of up to 2048 lines, 40 MHz bandwidth, plug-in bandwidth filters and adjustable transfer characteristics. Also announced is the HR-2000 solid-state Video Monitor that offers 2000 TV lines of resolution. Features of the HR-2000 include auto-locking to multiple scan rates, 50 MHz bandwidth, differential inputs, variable video enhancement, selectable A-B video input and separate data input channel. **Dage/MTI**, Michigan City, IN **Circle 194**

Internal Hard Disk Drive For PC/AT



Designed to be housed inside the IBM PC/AT, this 30 Mbyte hard disk drive (StorageMaster 630) has a typical access time of approximately 30 msec. Two storageMaster 630 Winchester drives can be housed side by side in the PC/AT processor cabinet and operate with the resident PC/AT disk controller. Each drive comes with an adaptive software diskette that allows users to operate the drive with standard PC DOS Version 3. Price for the StorageMaster 630 is $2,145. **Control Data**, Minneapolis, MN **Circle 174**

Prime Time Reading



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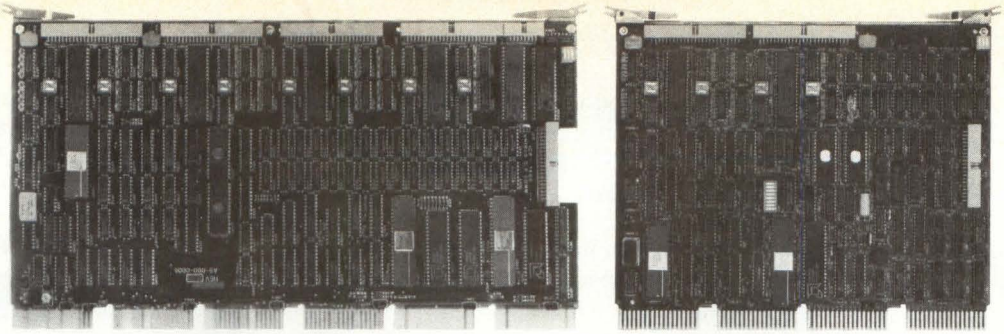
DIGITAL DESIGN
SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS



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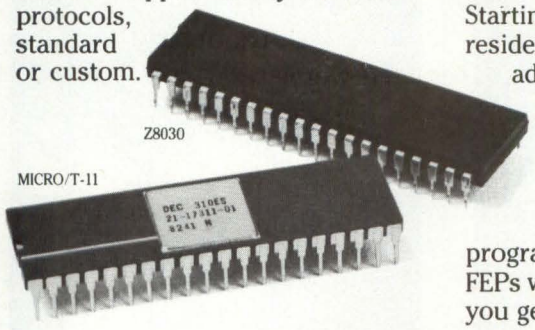

All ports on our FEPs are individually programmable for baud rates, synchronous and asynchronous protocols, RS-232C, RS-449 (RS-422, RS-423), MIL-188C and MIL-188-114.

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We can also provide turnkey packages for Telenet certified X.25 LAPB protocol software (CCITT 1980, Levels 1, 2, and 3) and HDLC (LAPB) frame and link level software. More standard protocols are on the way.

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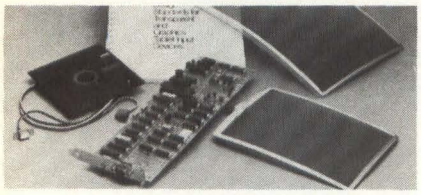
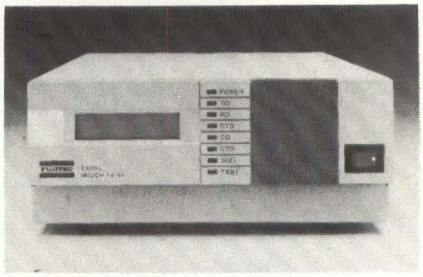
Touchscreen Development Kit



Developed for the firm's Touchscreen, this Engineering Development and Evaluation Kit is comprised of a 9″, 12″ or 13″ neutral-density analog-contoured touchscreen, a controller interface, demonstration programs, design manual, connectors and mounting adhesives. The Touchscreen is a transparent resistive touchsensor that achieves 4096 × 4096 screen resolution and 1% linearity. Price for the kit is $2,400. **Dorman Borgdnoff**, Andover, MA **Circle 167**

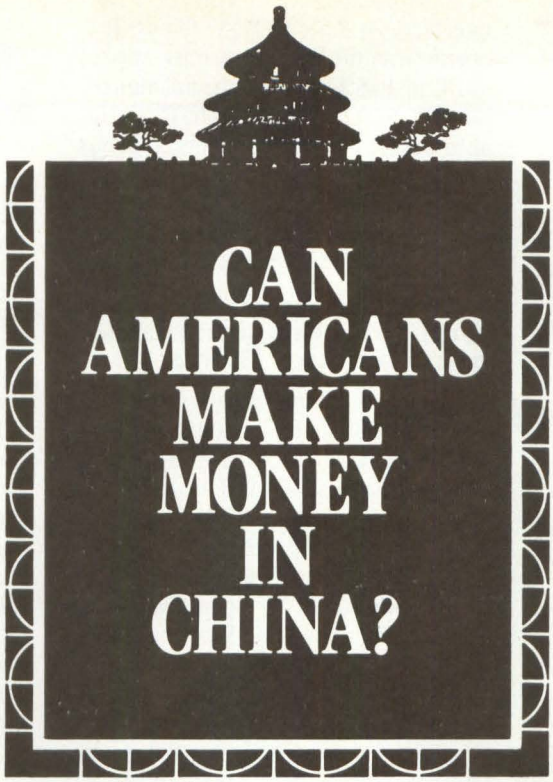
14,400 BPS Trellis-Coded Modem



An addition to the fixed line of modems, the M1926L 14,400 bps Trellis-coded modem is a standalone unit for use on four-wire leased lines. It can also operate at fallback speeds of 9600, 7200 or 4800 bps in compliance with CCITT V.29. A built-in six-channel multiplexer allows up to six 2400 bps channels to be transmitted simultaneously over a single based telephone line. The M1926L has an automatic adaptive equalizer that can bridge dropouts of up to two seconds. Price is $6,875. **Fujitsu America**, San Jose, CA **Circle 170**

Video Color System

Designed to record and replay pictures in slow motion, this high speed Video Color System can be used for time-study. A rotary shutter changes the normal 1/60/sec exposure rate of video cameras to 1/1,000/sec and up to 1/10,000/sec. Every color picture, with time and date recorded on it, can be moved to any part of the picture. Every tape can hold 324,000 pictures. All 60 pictures/sec, as recorded, can be seen in sequence at any playback speed. **Sun Vision**, Waukesha, WI **Circle 193**



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Circle 66 on Reader Inquiry Card

COMPONENTS

On-Chip Address Latching For CHMOS EPROMs

An enhanced version of the 27C64 CHMOS EPROM, this 64-Kbit CHMOS EPROM (87C64) contains the interface circuitry required to connect it with Intel CHMOS microcontrollers and μPs, therefore reducing chip count and eliminating the need for an external latch. Developed using the firm's CHMOS II-E process technology which uses epitaxial processing, the 87C64 has a maximum access speed of 200 nsec. In quantities of 10,000, the 87C64 sells for $14.70. **Intel**, Santa Clara, CA **Circle 141**

Plastic D/A Converters

Designed for digital audio, three new models of the PCM53 Series of plastic-packaged 16-bit monolithic D/A converters includes an internal zener voltage reference, a resistor ladder network, current switches and a fast-settling, low-noise output op amp. The Series now has two electrical grades: JP and KP. All offer 16-bit resolution, a 96 dB range and 16-bit monotonicity. Total bipolar drift and bipolar zero drift are typically ±25 ppm of FSR/°C and ±4 ppm of FSR/°C, respectively. **Burr-Brown**, Tucson, AZ **Circle 191**

ECL 1K RAMs

Designed for high speed scratch pad, control cache and buffer storage applications, these three RAM devices feature full on-chip address decoding, separate data inputs, noninverting data outputs and an active low write enable. The MCM10422 is a 1024-bit Read/Write RAM with 256 words × 4-bit organization; the MCM10422L10 has a 7 nsec typical address access time (TAA) and 10 nsec max. A reduced speed version, the MCM10422L15, has a TAA of 15 nsec max. **Motorola Semiconductor**, Phoenix, AZ **Circle 131**

ALS-Equivalent CMOS Logic Family

This fully 54/74ALS-equivalent CMOS logic family, AHCT, will include approximately 150 part types, with the first 22 octals available now. AHCT devices provide 4 nsec typical gate delays and 3-state outputs with high drive current (I_{OL} = 24mA at V_{OL} = 0.5V) for direct bus interface. At 4.5V to 5.5V, the devices operate over the full commercial range of -40°C to +85°C and over the full military range of -55°C to +125°C. The first available devices include buffers and bus drivers, transceivers, flip-flops, latches, decoders/encoders and multiplexers/demultiplexers. **Zytrex**, Sunnyvale, CA **Circle 129**

One-Time Programmable and Fast-Turn ROMs

Packaged in 24-pin plastic DIPs, the MCM68769 is an 8K × 8-bit MOS OTP ROM and the MCM68768 is an MOS 8K × 8-bit Fast-Turn ROM. Both devices are mutually compatible, TTL compatible and pin compatible with the MCM68766 UV EPROM and MCM68366 Mask Programmable ROM. Operating voltage range, using a single +5V power supply, is +4.5V to +5.5V. Operating temperature range is 0°C to +70°C with power supply current at 85 mA max. Maximum access times from address are 300 nsec and 350 nsec. Maximum access time from Output Enable are 150 nsec and 120 nsec. **Motorola**, Austin, TX **Circle 132**

Double-Bit Error Checker/Corrector

An expansion of the firm's (DP8400) family of memory interface devices, the DP8400-2 16-bit Expandable Error Checker/Corrector contains a 16-bit detect/correct function in a 48-pin DIP. Word sizes can be expanded to 32 or 64 bits. When used with a 10 MHz CPU, the DP8400-2 allows for write cycles with no wait states and read cycles with one wait state in the always-correct mode. The DP8400-2 also features a bidirectional syndrome port and supports byte parity checking generation and correction. Price in 100s is $49.95. **National Semiconductor**, Santa Clara, CA **Circle 128**

Digital Logic Devices

Introduced as a pin-compatible licensed alternate source for Motorola's MECL-10KH family, this family of 12 ECL devices (ECL10KH) includes gates, multiplexers, latches and special function devices. Typical propagation delay for the ECL10KH devices is 1 nsec with a max rise-and-fall time of 2.2 nsec (1.6 nsec typical). Power supply current for each device varies (lowest is 29 mA) and power dissipation averages 25 mW per gate. Housed in 16-pin ceramic or plastic DIPs, the ECL10KH devices operate on a power supply of -5.2V, ±5%. **Monolithic Memories**, Santa Clara, CA **Circle 137**

256K DRAM Controller/Driver

Eliminating wait states, replacing discrete logic controllers for addressing and driving more than 2 Mbytes of DRAM, the DP8419 single-chip 256K DRAM Controller/Driver works with CPUs at 10 MHz or more. This ALS-type device offers on-chip DRAM address multiplexers, delay lines, on-board high-capacitance drivers and a refresh counter. With automatic refresh and access modes (1 and 5), the DP8419 drives 88 DRAMs (50 pf load) over the full temperature (0°C to +70°C) and operating supply range. The DP8419 is housed in a 48-pin DIP. **National Semiconductor**, Santa Clara, CA **Circle 127**

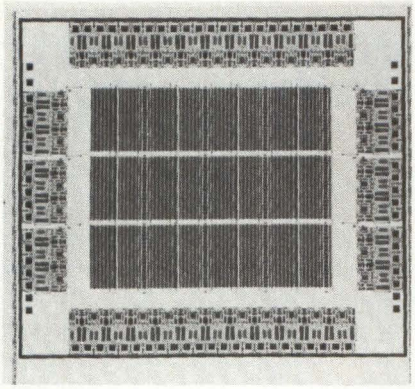
2-Micron MicroCMOS Gate Arrays

An expansion of the SCX6200 family of MicroCMOS gate arrays, the SCX6206 (6000 gates), the SCX6218 (1800 gates), the SCX6232 (3200 gates) and the SCX-6244 (4400 gates) feature 2-micron drawn geometry with 1.4-micron effective channel length allowing sub-nsec gate delays. Allowing TTL and CMOS compatibility, outputs are selectable for 1, 2 or 4 mA drives. The SCX6200 Series features dedicated, multiplexed Dflip-flops incorporated into the internal array core, as well as built-in self-test circuitry. **National Semiconductor**, Santa Clara, CA **Circle 143**

12-Bit A/D Converter

Using CMOS and laser-trimmed bipolar die, the ADC674A is a 12-bit successive approximation A/D converter. With no missing codes over temperature (0°C to +75°C; -55°C to +125°C), the ADC674A is fully specified for operation from +5V and ±12V or ±15V supplies. Full scale and offset errors can be trimmed to zero externally. Internal scaling resistors provide selectable analog input signal ranges of 0 to +10V, 0 to +20V, ±5V and ±10V. Max conversion time is 15 μmsec, while bus access time is 150 nsec. Price in 100s ranges from $39.25-$153. **Burr-Brown**, Tucson, AZ **Circle 139**

New Gate Array Architecture



Using a new gate array architecture, this family of CMOS arrays, the P²L (Programmable Performance Logic), achieves standard cell gate densities while retaining gate array turnaround time. P²L provides programmable speed/power product of individual gates, the ability to incorporate ROM and PLA on the array and the ability to achieve high fan-in with one logic delay level. The P²L CMOS family is available in arrays up to 9000 gates in plastic and ceramic packaging. **Integrated Logic Systems**, Colorado Springs, CO **Circle 142**

Bipolar Array

The FLEXX array offers both gate arrays and standard cells on the same chip. Using an oxide-isolated ISL process that provides typical per-gate propagation delay of 900 psec and allows designers to create application-specific designs of up to 2000 gates, the FLEXX array employs the "soft macro" structure. The initial FLEXX array ISL library consists of 50 soft macros developed to emulate 7400 TTL functions. A FLEXX array IC is capable of replacing up to 100 SSI and MSI logic ICs. **Signetics**, Sunnyvale, CA **Circle 203**

16-Bit A/D Converter

Achieving a 17 μsec maximum conversion time, the AD376 hybrid 16-bit A/D converter guarantees no missing codes to 14 bits over a 0°C to 70°C temperature range. Specified for operation with ±1V DC and +5V DC supplies, the converter typically consumes 1100 mW. Guaranteeing maximum linearity error of ±0.006% FSR for the J grade, the AD376 accepts bipolar input signals of ±2.5V, ±5V, ±10V and unipolar inputs of 0 to +5V, 0 to +10V and 0 to +20V. Prices in 100s are $189 and $219. **Analog Devices**, Norwood, MA **Circle 198**

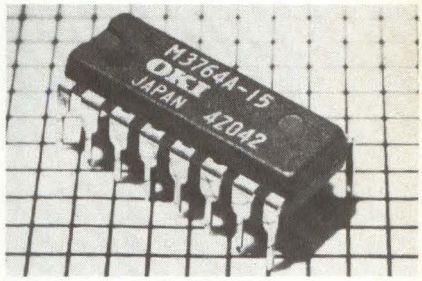
64 Kbit PROM

Organized in 8K × 8 bits, the AM27S49 64 Kbit bipolar PROM is available in 40 nsec and 55 nsec commercial versions. This PROM incorporates three-state outputs and features platinum-silicide fuses. Produced in this firm's proprietary IXOM-S process, a scaled, ion-implanted, oxide-isolated bipolar process, the AM27S49 has applications in high-density microprogrammed control store memory. Housed in a 24-pin 600-mil ceramic package, the 55 nsec version is priced at $72.50 and the 40 nsec device is $108, each in 100s. **AMD**, Sunnyvale, CA **Circle 200**

Photomultiplier Tubes

Measuring only 55 mm in overall length, these 3/8" diameter, head-on type photomultiplier tubes are now available with solar blind, UV-visible, visible or visible-IR characteristics, and in both cylindrical and rectangular shapes. Applications include CT scanners, multichannel spectrophotometers, scintillation counters, TOF counters and hodoscopes in high energy physics research, and other compact photometric equipment. **Hamamatsu**, Middlesex, NJ **Circle 197**

64K DRAMs For PC/AT Compatibles

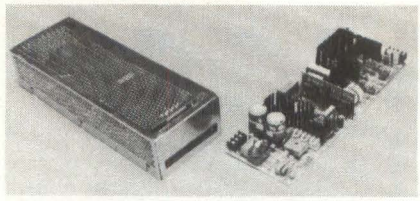


Designed for use in PC/AT compatibles, the MSM3764A 64K DRAM is functionally compatible with its predecessor DRAMs; it is fully decoded and organized as 65,536 one-bit words. With 128 refresh cycles at 2 msec and noncritical clock timing requirements, the MSM3764A requires a single +5V supply with ±10% tolerance and is TTL compatible. Three access speed ranges are available: 120 nsec, 150 nsec and 200 nsec. Packaged in a 16-pin plastic DIP, the MSM3764A is priced according to range. **Oki Semiconductor**, Sunnyvale, CA **Circle 135**

Linear Mosaic Arrays

Each semicustom chip in the FB300 Series of linear mosaics is composed of distinct component groupings that fit together like individual tiles, forming a mosaic. Each tile is treated like a mini chip designed so one or more macro cells fit on each one. Currently, a library of 24 macro cells are defined for the FB300 Series. The Series features transistors with 1 GHz f_T and a dual layer metal for circuitry interconnection. The FB300 Series is supported by the firm's CAD package, Linear CAD I, which performs schematic capture and SPICE circuit simulation on the IBM PC and compatibles. **Micro Linear**, San Jose, CA **Circle 204**

MOSFET Switching Power Supply

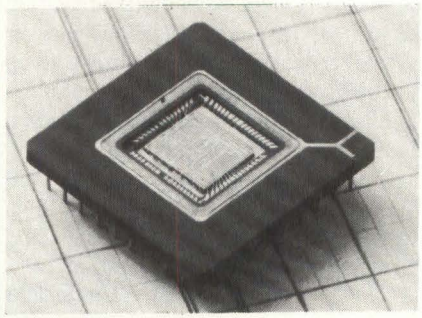


An addition to the firm's "S" Series of MOSFET switching power supplies, this four-output, 175W unit features a 50 kHz switching frequency and built-in brown-out protection. At outputs one through three, load regulation is 4% across the no-load to full-load range. At output four, the load is regulated ±4% over the same range. The unit reliability exceeds 78,000 hours MTBF on a demonstrated basis. **NCR**, Lake Mary, FL **Circle 136**

Fiber Optic Lamps

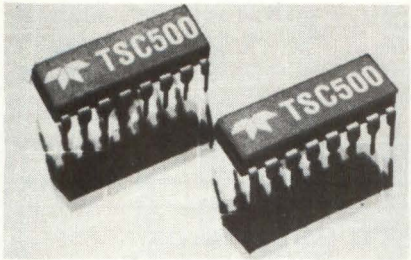
Interfacing directly with fiber optic cables, assemblies and single fibers, these miniature Fiber Optic Lamps, the L1006 and L8006, form an intense spot of illumination at a distance of 1.0 mm from the tip of the lamp. The L1006 interfaces with single fibers of 10-500 microns in diameter and operates at 3.5V. Operating at 5.0V, the L8006 interfaces with larger size bundles and assemblies. Both are priced at $5-$6. **Gilway Technical Lamp**, Woburn, MA **Circle 190**

DMA Controllers



Designed to support the M68000 MPU family, these DMA controllers (MC-68440, MC68442 and MC68450) are directly compatible with the M68000 as well as with the VMEbus and VERSA-bus. The MC68440, a two-channel DMA device, supports a 24-bit linear address space. The MC68442 is an extended version of the MC68440, with 32 bits of linear addressing and an additional function output. The MC68450, a four-channel DMA controller, is upward pin and register compatible with the MC68440. **Motorola**, Austin, TX **Circle 133**

Precision Analog Converter



Containing the analog circuits necessary to make a dual slope integrating converter, this CMOS A/D converter, the TSC500, can be used in applications at 8- or 14-bit resolution with only a software change. The TSC500 features a differential analog input and reference for ratiometric conversion with a zero scale temperature drift of 2 μmV/°C. Nonlinearity is 0.005% max, with differential nonlinearity at 0.002% max. The CMOS differential input leakage current is 15 pA max with resolution guaranteed at 50 ppm. **Teledyne Semiconductor**, Mountain View, CA **Circle 130**

8-Bit Microcomputer In SNOS

With 32 bytes of EEPROM, in two 16 byte banks, as well as 512 × 512 bit program ROM and 32 bytes of RAM, the PIC16E57 8-bit microcomputer uses a SNOS process. The on-chip voltage synthesizer uses the standard 5V power source to generate the EEPROM write voltage. Pin compatible with the PIC-1657, the PIC16E57 provides EEPROM instructions that allow it to read and write to EEPROM registers. Available in temperature ranges from -40°C to +110°C, the PIC16E57 is priced at $3 in 50K quantities. **General Instrument**, Hicksville, NY **Circle 126**

Enhanced Floppy Controller

The FDC 9266 enhanced floppy disk controller combines the FDC 765A with the FDC 9229 Floppy Disk Interface Chip in a 40-pin DIP. Maintaining software compatibility with the FDC 765A, the FDC 9266 can control up to four drives: single or double sided 3½", 5¼" or 8" drives. Its programmable sector size capability allows the FDC 9266 to interface to CP/M and MS-DOS. Working in DMA, processor polled or interrupt mode, this controller also features a built-in precompensation generator. Price in 100s is $25.30. **Standard Microsystems**, Hauppauge, NY **Circle 202**

4-Bit Composite Video D/A Converters

These TTL compatible converters in the AH8304 family are available with or without memory and feature advanced single chip design. The AH8304 is a self-contained, 4-bit composite video subsystem in a 24-pin DIP. The AH8304TM color-mapped triple (RGB) 4-bit video D/A converter has color look-up table memory designed for the color graphic system. The AH8304TC is a triple video DAC-only version for use with systems that require a different configuration of look-up table memory. **Analogic**, Peabody, MA **Circle 199**

CMOS 32-Bit μP Development

Fabricated in 1.3 micron CMOS, 2-layer metal process technology and containing over 300,000 transistors, this 32-bit microprocessor test chip operates at 5 MIPS. The Micro 32 test vehicle incorporates a proprietary pipelined system architecture and a cache memory scheme permitting high speed interface with I/O processors and file processors. Featuring a 200 kbit ROM with a 50 nsec cycle time and a 32-bit ALU, the chip measures 6.5 mm × 9.0 mm. No definite packaging configuration has been chosen. **Hitachi**, San Jose, CA **Circle 201**

CMOS FIFO

The IDT 7101/7102 CMOS parallel In-Out FIFOs are built with a RAM Pointer architecture, eliminating fall-through time and allowing for a faster read/write cycle. The IDT 7202, a 1024 × 9 organization, and the IDT 7201, a 512 × 9 organization, achieve commercial access times of 50 nsec, 80 nsec and 120 nsec, and military access times of 55 nsec, 85 nsec and 120 nsec. Operating requirements are 80 mA: commercial and 100 mA: military units. On standby, the power requirements drop to 8 mA and 15 mA, respectively. **Integrated Device Technology**, Santa Clara, CA **Circle 205**

10-Bit 800 Nsec A/D Converter

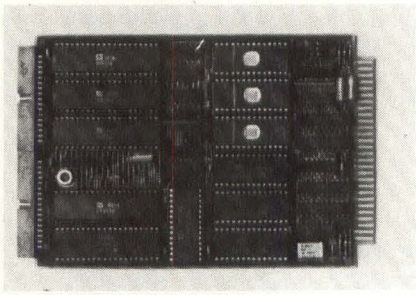
With an 800 nsec max conversion time, this 10-bit hybrid A/D converter (AD ADC-816) specifies a typical conversion time temperature coefficient of ±0.06%/°C. Guaranteeing max differential linearity of ± ½ lsb and no missing codes, the 816 provides a pin-selectable

NEW PRODUCTS

internal reference and three unipolar input ranges: 0 to -5V, 0 to -10V or 0 to -20V; and three bipolar ranges: ±2.5V, ±5V or ±10V. Three grades are available in 0° to +70°C, −25°C to +85°C and -55°C to +125°C. **Analog Devices**, Norwood, MA **Circle 138**

BOARDS

STD Bus Boards



Five 6502-based board level computers have been announced by Cubit. Both NMOS and CMOS CPU boards feature serial and parallel I/O, memory and peripheral control capabilities. Programming can be done in Basic or Assembler running under Cubit's DOS/65. Forth will be available soon. Peripheral support is provided by an intelligent CRT/printer/keyboard controller. **Cubit**, Mountain View, CA **Circle 144**

Q-Bus Winchester/ Floppy Controller

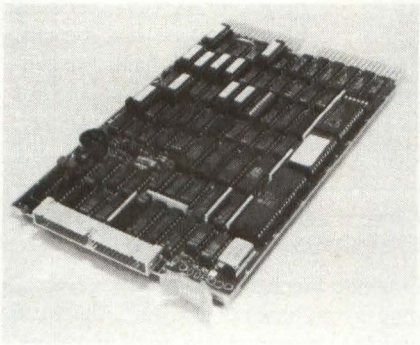
Compatible with DEC's MSCP software, the UDC11 dual-width Winchester and floppy disk controller is compatible with the Q-Bus. Under MSCP, the UDC11 allows the use of ST506 interface drives of any capacity. Hence, system integrators can design MicroPDP-11 and MicroVAX-I and II compatible systems with RX50 emulation. The UDC11 can also control any combination of up to four Winchester cartridge and floppy drives. Price is $1,795. **Andromeda Systems**, Canoga Park, CA **Circle 207**

1-Mbit Bubble Memory Eurocard

Compatible with the G-64 bus, the Gesbul-1 1-Mbit bubble memory board is organized as 128 Kbytes of nonvolatile magnetic storage. The board uses a DIN 41612 indirect connector and is powered by a +5V and +12V on the G-64 bus. Using a bubble memory device and associ-

ated circuitry from Intel, the Gesbul-1 can be upgraded to accommodate 4-Mbit devices. Able to work with all microprocessors on the G-64 bus, including the 6809, 68000, 8088, 8085, Z80, 16032 and J-11, the Gesbul-1 is priced at $1,250. **Gespac**, Mesa, AZ **Circle 206**

Async Controller For LSI-11



Maintaining software compatibility with DEC's DZ11 subsystem, the Optimux/8DZ async communications controller allows users to interface up to eight devices per controller card. Contained on a dual-height PCB that connects to its DEC H3006-compatible distribution panel, the controller allows up to 16 lines to be interfaced to the LSI-11 system from each panel. Providing 15 software-selectable data transfer rates from 50 bps to 19.2 Kbps, it contains a 64 character receive FIFO buffer. Price is $770. **Dilog**, Anaheim, CA **Circle 150**

IBM PC Processor Board

Intended to increase the processing speed of the IBM PC and XT, the Model PC-286 processor consists of a single PCB containing an iAPX286 processor chip, room for an optional 80287 math coprocessor and up to 640 Kbytes of RAM. The PC-286 can be run at 4, 6 or 8 MHz and may include 256K to 640K RAM. A piggyback card can add from 512 Kbytes to 2 Mbytes of additional RAM. The PC-286 board replaces the 8088 chip with a 40-pin header, allowing the PC-286 to take over the PC bus completely. **Seattle Telecom and Data**, Redmond, WA **Circle 209**

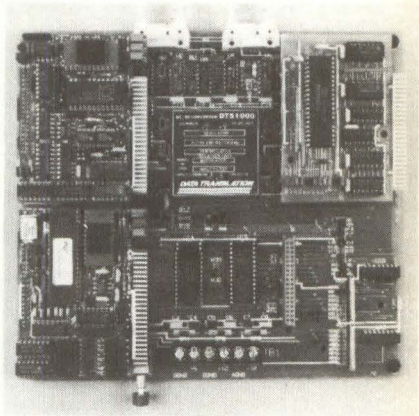
Image Processing Boards For VMEbus

Designed for machine vision, imaging and graphics applications using the VMEbus, the VMACC-Series boards are especially built for high speed enhanced image processing. The boards include: the Image Acquisition Board which interfaces to linear CCD-array camera including programmable video tables for preprocessing; the Image Buffer Board: 256 Kbyte RAM for refresh of 512 × 512 matrix in 17 msec; and the Image Processing Boards such as Convolution, Streaming and VARDIG that perform image algorithms for dimensional and/or surface analysis. Price ranges from $2,000 to $5,000. **Advanced Computer Concepts**, Costa Mesa, CA **Circle 196**

VMEbus Microcomputer Board

Designed for real-time processing applications, this VMEbus-based microcomputer board features a 12.5 MHz 68000 in a pin grid package. With async and sync dual serial communications ports, the board provides three 16-bit timers and 16 bits of parallel I/O. The CPU-2RT can access 128K dual-ported DRAM, upgradable to 256K with no wait states. Sockets for two EPROMs and two SRAMs are available as well as an on-board VME arbiter, allowing the CPU-2RT to occupy slot 1. Price is $2,450. **EMS**, Dallas, TX **Circle 210**

Intelligent Controller Interfaces Bitbus



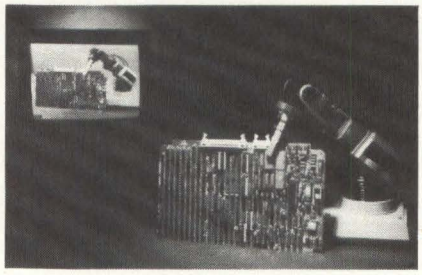
Part of a line of distributed control modules compatible with the Intel Bitbus network, the DT901 Intelligent Standalone Controller interfaces the Bitbus to iSBX modules for remote measurement and control. The DT901 functions as a remote controller or an I/O expansion device. As an intelligent controller, it monitors the multiple process points status and executes user-supplied control software. As an I/O expander, the DT901 collects measurement and control information and transfers data via the Bitbus to the host. Price is $495. **Data Translation**, Marlboro, MA **Circle 151**

NEW PRODUCTS

IBM PC Color Graphics Board

Plug-compatible with IBM's Color Graphics Adapter, the ColorView graphics board provides 32K memory, allowing the user to create two complete pages in the graphics mode. ColorView also features two true colors (1 of 16 for the foreground and 1 of 16 for the background) in the IBM high resolution graphics mode. Display memory can be accessed at any time by the microprocessor without causing glitches on the screen. Price is $289. **Princeton Graphic Systems**, Princeton, NJ **Circle 211**

Single-Board Multibus Image Processor



Performing real-time image processing and image display on a single Multibus board, the MIP-512 contains a 16.7M color palette. With data storage and 256 Kbytes of on-board RAM that provide 512 × 512 resolution with 256 colors/pixel, the MIP-512 also offers a 90 nsec bit slice ALU. The dual-ported RAM allows memory mapped CPU access and true DMA. Eight input and eight output look-up tables are available. Price is $2,995. **Matrox Electronic Systems**, Dorval, Quebec **Circle 147**

Dual-High Display Controller

With two display interfaces on the same dual-high board, the VRS-Q Q-Bus graphics card uses a 60 Hz noninterlaced display to produce a 512 × 512 monochrome dot graphics image. An optional 50-line × 80-character alphanumeric image that overlays the dot graphics can be scrolled without blurring or creating ghost images. The dot graphics image is stored in a 16K word memory and acts through an independent CRT controller. The alphanumeric display data is stored in a separate 4K-word memory and also acts through a separate CRT controller. Price is $1,650 with alphanumerics. **Peritek**, Oakland, CA **Circle 153**

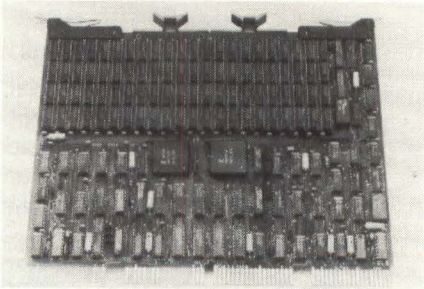
Double Wide SBX Board

Combining two independent RS-232-C or RS-422A/449 serial I/O channels, a battery-maintained real-time clock/calendar and 2 Kbytes or 8 Kbytes of battery-maintained CMOS RAM, the UDX-221 Multifunction Multimodule plugs directly into any iSBX bus compatible host board. Each of the UDX-221's two serial channels may be configured for EIA RS-232-C or RS-422A/449 interfaces with async, bit-sync or byte-sync formats. Each channel has its own baud rate generator and may be operated from 37.5 bps to 1.23 Mbps. **Microdesigns**, Tucker, GA **Circle 208**

Graphics Controllers and Displays

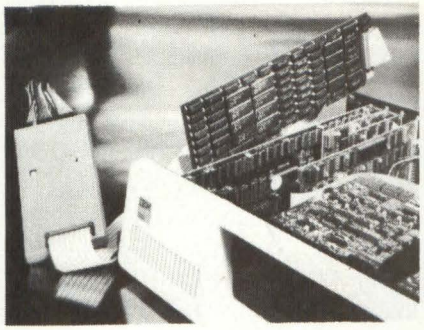
Drawing images at 1M pixels/sec, these plug-in graphics controllers, the M-16 and M-256 provide 16 and 256 colors, respectively from a palette of 4096. The drawing capability is generated by the firm's two-micron CMOS graphics controller chip set with an on-board 68000. To operate with the controllers, a 60 Hz noninterlaced RGB display, the CD-1, with 640 × 480 resolution has also been announced. Controllers range from $2,250-$2,850 and the display costs $1,025. **Verticom**, Sunnyvale, CA **Circle 192**

EDC Memory and Software Support



Built for the LSI-11/73 and MicroVAX, the CI-1173-EDC Memory with error detection and correction and a software support module for Q-Bus compatible systems is available in configurations ranging from 256 Kbytes to 2 Mbytes on a single card. Worst case access and cycle times are 60 nsec and 240 nsec, respectively. Internal and distributed refresh are built into the memory, which requires less than 900 mA power from a +5V battery source for up to 2 Mbytes of memory. **Chrislin Industries**, Westlake Village, CA **Circle 152**

32-Bit Logic State Analyzer



When plugged into an IBM PC, XT or compatible expansion slot, the PCI-4304-1 transforms the computer into a 32-bit logic analyzer. The PCI-4304-1 system includes a plug-in PCB, 3′ ribbon cable and instrument pod that extends from the computer to the digital system under test, a set of color-coded input leads with probe clips and the system operating software. The data path is 32-bits wide, data setup time, 20 nsec and data hold time, 0 nsec. With 1024 × 32-bit words memory, the PCI-4304-1 is priced at $2,750. **Burr-Brown**, Tucson, AZ **Circle 145**

VMEbus Mini-Array Processor

An enhanced version of the firm's first VMEbus mini-array processor (VAP-64), the VAP-64B fixed-point mini-array processor provides three more instructions and is fully compatible with the VAP-64. The 21-instruction set includes complex demodulation, an FIR instruction and Peak Pick instruction. The VAP-64B also features 10 MOPS, 50 kHz real-time processing bandwidth and built-in self-test. **DSP Systems**, Anaheim, CA **Circle 148**

20 MHz Q-Bus SMD Controller

With data transfer rates up to 2.5 Mbytes/sec, the MLSI-DK11 disk controller will operate disk drives with SMD interface that can operate at the standard SMD rate of 1.2 Mbytes/sec as well as drives with 1.8 or 2.4 rates. The MLSI-DK11 has up to 22-bit direct DMA data transfer addressing range and Block Mode DMA data transfer capability. The controller can support two physical drives at 1 or 2 logical units per drive for a maximum of 4 logical units. Price is $2,330. **MDB**, Orange, CA **Circle 149**

Compact Q-Bus Interface

Compatible with DEC's DZV11, the Octomux 8-port async multiplexer has 8 ports in a dual board. With programmable baud rates to 38.4 Kbaud and a double density distribution panel, the Octomux features character length, parity, stop bits and Transmitter Enable. Onboard DIP switches permit selection of base address, interrupt vector, interrupt priority and baud rate table. Four addresses access six device registers. **Minntronics**, St. Paul, MN **Circle 154**

Color Graphics Card For IBM PC

Providing an optional parallel printer port and composite color output on a single short slot board, the Persyst Short-Port Color Card is fully compatible with standard IBM color graphics software and monitor. Video output is direct drive (IRGB) or optional composite color output. Graphic character display is 7 × 7 dot characters in an 8 × 8 field. Alphanumeric display mode is 40 characters × 25 rows, low resolution and 80 characters × 25 rows, high. **Emulex**, Costa Mesa, CA **Circle 146**

SOFTWARE

Interactive Design Rule Checker

Designed for VLSI layout on the Designer III workstation, the CAEPAC III Design Rule Checker software package checks for violations interactively as each element is placed or modified. When a violation in the design rules occurs, CAEPAC III highlights the area and displays a user-defined error message. The software allows designers to see violations as soon as they are created. This occurs in real-time during layout and editing. **Caeco**, Tucker, GA **Circle 179**

Real-Time Intelligent Machine Interface

Enabling LISP programs or expert systems to deal with real-time processes, the RTIME (Real-Time Intelligent Machine Interface) is designed for the firm's family of LISP machines. Written in C code, RTIME uses the parallel processing capabilities of the Lambda/Plus series of LISP machines, which feature both a dedicated LISP processor for AI-related tasks and an MC68010 numeric copro-

cessor. With RTIME, the MC68010 coprocessor of the Lambda/Plus monitors and screens incoming information on a real-time basis, thus freeing the LISP processor. **LMI**, Granada Hills, CA

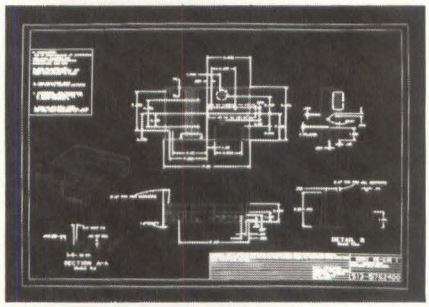
Circle 222

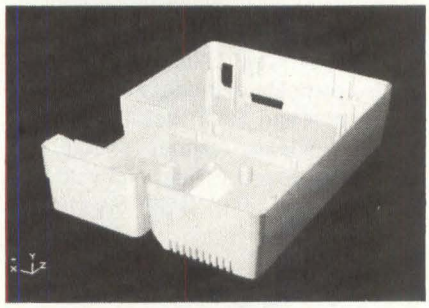
C Compiler For HP-9000

Running on the HP 9000/500 series with the HPUX operating system, the C68 C compiler generating code for the MC68000 family is a full implementation of the Kernighan and Ritchie language specification. Consisting of a macroprocessor, compiler, relocatable assembler, linker loader, support library and utilities, the compiler generates assembly language source which is assembled with the firm's assembler and linked with their linking loader. Price is $1,495. **Alcyon**, San Diego, CA

Circle 227

2D Drafting and Dimensioning

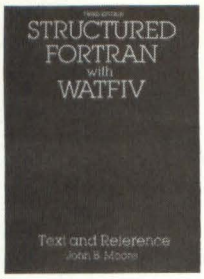




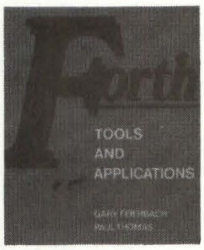
Interfacing directly with the Geomod solid modeler, this 2D drafting and dimensioning module (Geodraw) offers a "T" square feature that emulates the traditional drafting machine. The dimensioning capability provides real-time use; users can create text dimensions, labels and balloons and interact with the system to arrange arrows, and position text. Geodraw presents linear, radial and diametrical dimensions in English or Metric units. Price ranges from $12,500 to $25,000, depending on the system. **Structural Dynamics Research**, Milford, OH

Circle 185

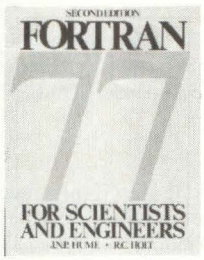
NEW LITERATURE



Structured FORTRAN With WATFIV. This 500-page third edition by John B. Moore discusses how to run WATFIV jobs under the CMS operating system and how to use the interactive debugging facilities available with WATFIV. Sections have been added to emphasize the use of top-down design and stepwise refinement in algorithm development.
Reston Publishing Co. **Circle 255**



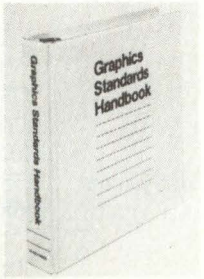
Forth—Tools and Applications. This 150-page book by Gary Feierbach and Paul Thomas demonstrates the development of Forth-based tools to help the programmer design and debug Forth applications. Programming design aids are hinted at, debugging techniques are shown and utilities are analyzed. Listings for Forth routines are provided by line numbers, rather than screens.
Reston Publishing Co. **Circle 252**



FORTRAN 77 For Scientists and Engineers. In this book, J. N. P. Hume and R. C. Holt aquaint students with the ideas and technical terminology connected with computers and provide a detailed presentation of programming so the computer can be used professionally. Programming is taught using the FORTRAN 77 language.
Reston Publishing Co. **Circle 253**

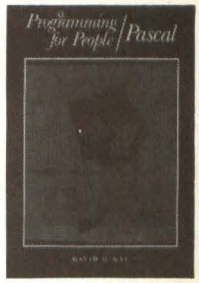
Introduction to Computer Engineering Hardware and Software. This third edition, written by Taylor L. Booth, discusses the various classes of digital information processing systems and devices and the interrelationship between the hardware and software techniques that can be used to solve a particular problem. The unifying theme throughout the book is the concept that the steps involved in solving a problem must first be represented by an algorithm.
John Wiley and Sons **Circle 254**

Linear ICs Reference Book. This 34th edition of Linear ICs, published by D.A.T.A. Inc., lists 15 component categories and 62 specific device functions within those categories. Manufacturer information is compiled in one section and a cross-referencing "Functional Equivalance Index" lists currently available linear ICs from 80 manufacturers by pin-for-pin equivalent groups, with generic numbers that refer directly to schematic drawings.
D.A.T.A. Inc. **Circle 259**

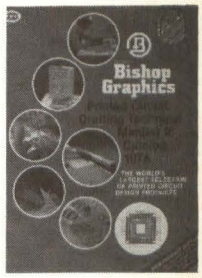


Graphics Standards Handbook. This 1985 edition of the Graphics Standards Handbook published by CC Exchange describes a three-dimensional extension to GKS (Graphics Kernal System), sponsored by Holland and now being considered by ANSI's Technical Committee X3H3. The new edition of the Graphics Standards Handbook also reflects name change alterations in two other standards: Virtual Device Metafile and Virtual Device Interface.
CC Exchange **Circle 260**

PC Data Acquisition/Control Interface Handbook. This 68-page handbook from MetraByte Corp. describes the firm's line of data acquisition and control plug-in interface boards for the IBM PC, XT, AT and compatibles. Included in the book are detailed sections on applications, configuration guides and a utility software description.
MetraByte Corp. **Circle 258**



Programming For People/Pascal. David Kay presents the fundamentals of computer programming, using Pascal as the example language in his 640-page book. The book approaches issues such as employing logical, disciplined algorithmic problem solving methods, managing the complexity of large systems and understanding the reasons behind the rules.
Mayfield Publishing Co.
Circle 256



Printed Circuit Design and Drafting Manual. This 220-page manual and catalog from Bishop Graphics lists printed circuit design and drafting products. Divided into two segments, the manual is an expanded product catalog and an updated technical manual. New products included in the book cover Bishop's line of microelectronic artwork patterns. Also included is the Accupunch deal system punch, designed to give users the hole pattern of their choice for overlay drafting applications.
Bishop Graphics **Circle 262**

CALENDAR

June 3

Technology Issues in Networking Seminar. New York, NY. Contact: Robert Weiner, Technology Concepts Inc., Old County Road, Sudbury, MA 01776. (617) 443-7311.

June 3-5

X.25 Educational Seminar. Alexandria, VA. Contact: Dynatech Packet Technology Inc., 6464 General Green Way, Alexandria, VA 22312. (703) 642-9391.

June 4-6

Data Communications and Network Design Concepts Courses. Montreal, Canada. Contact: The Computer Communications Institute, 98 Peckham Ave., Willowdale, Ontario M2R 2V5. (416) 222-3145.

June 5-7

Optical Storage For Small Systems Conference. Los Angeles, CA. Contact: Judy Hanson, Technology Opportunity Conference, PO Box 14817, San Francisco, CA 94114-0817. (415) 626-1133.

June 6-7

Networking IBM PCs and Compatibles Seminar. Raleigh, NC. (Also five other dates and locations) Contact: Center For Advanced Professional Education, 1820 E. Garry St., Suite 110, Santa Ana, CA 92705. (714) 261-0240.

June 9-11

Three Dimensional Display Techniques Conference. Monterey, CA. Contact: Richard Murray, Institute For Graphic Communication Inc., 375 Commonwealth Ave., Boston, MA 02115. (617) 267-9425.

June 9-13

Computer Vision And Pattern Recognition Conference. San Francisco, CA. Contact: IEEE Computer Society, 1109 Spring St., Suite 300, Silver Spring, MD 20910. (301) 589-8142.

June 10-11

Artificial Intelligence Seminar. Dallas, TX. Contact: Ken Orton, Future Computing Inc., 8111 LBJ Freeway, Dallas, TX 75251. (214) 437-2400.

June 10-13

Short Wavelength Laser Systems Course. Dallas, TX. Contact: Engineering Technology Inc., PO Box 8859, Waco, TX 76714-8859. (817) 772-0082.

June 10-13

ATE East Conference and Exposition. Boston, MA. Contact: Stephen Schuldenfrei, Morgan-Grampian Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215. (617) 232-EXPO.

June 19-21

Nepcon East Exposition. Boston, MA. Contact: Cahners Exposition Group, Cahners Plaza, 1350 East Touhy Ave., PO Box 5060, Des Plaines, IL 60018. (312) 299-9311.

June 19-21

Local Area Networks Seminar. Cambridge, MA. (Also in St. Louis, MO – June 5-7 and Albany, NY – June 12-14.) Contact: Center For Advanced Professional Education, 1820 E. Garry St., Suite 110, Santa Ana, CA 92705. (714) 261-0240.

June 23-26

Design Automation Conference. Las Vegas, NV. Contact: Lawrence O'Neill, Bell Laboratories (213 327), Crawfords Corner Rd., Holmdel, NJ 07733. (303) 530-4333.

June 24-25

Micro-Mainframe Links Seminar. Seattle, WA. Contact: Software Institute of America Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

June 25-27

Computer Graphics '85 West Conference. Los Angeles, CA. Contact: National Computer Graphics Association, 8401 Arlington Blvd., Fairfax, VA 22031-4670. (703) 698-9600.

ADVERTISER INDEX