A MORGAN-GRAMPIAN PUBLICATION

Digital Design

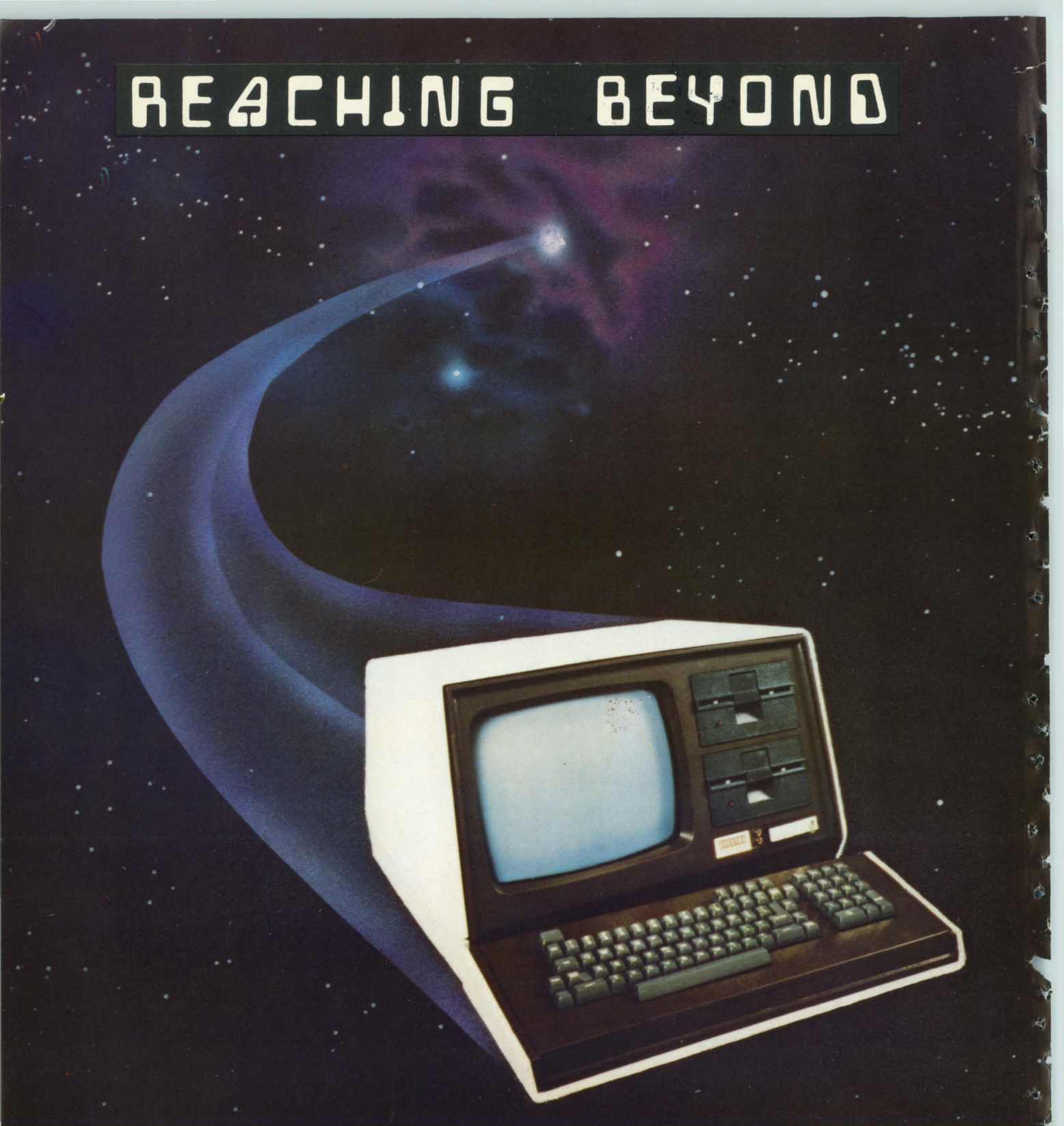
COMPUTERS/SYSTEMS · PERIPHERALS · COMPONENTS · 6/82

New Concepts Brighten Desk-Top Designs

Tape Technology Meets Back-Up Needs
Simplify Your A/D To µP Interface
Color Graphics • Comdex • SIGGRAPH

VOL. 12
NO. 6

REACHING BEYOND



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The SPECTRA 123 is configured with 128 KB MOS memory, a 2MB 5¼" dual floppy RX02® compatible subsystem, 3 serial ports, complete with an integral VT100® compatible CRT terminal and detached keyboard.

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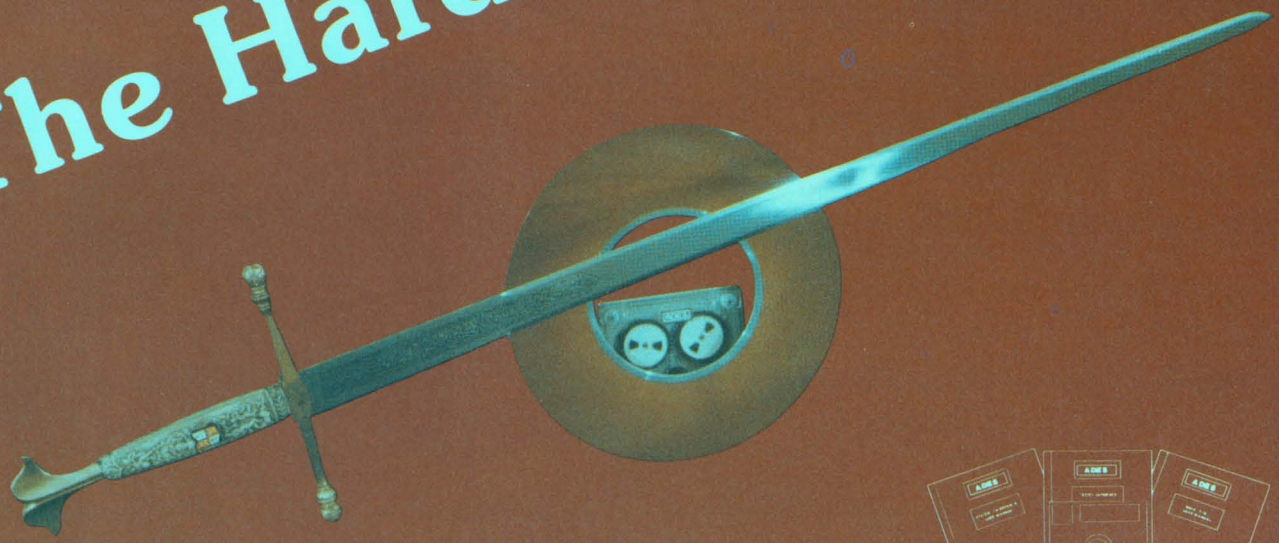
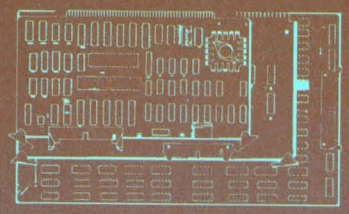
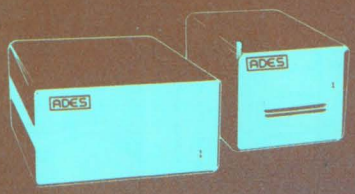
The Hard Edge in performance







SYSTEMS
Whether you are a systems integrator or computer OEM, *ADES* subsystems provide the ultimate solution to your needs. As a fully supported product, *ADES* subsystems provide a revolutionary product capable of displacing cartridge disk drives and floppies.

SYSTEM 8
As a standalone table top or rackmount package, the *GYPSY* based SYSTEM 8 provides the user a disk of 10 MB, 34 MB, or 70 MB of disk capacity with 10 MB or 20 MB removability via the streaming tape.

SYSTEM 14
The *SYSTEM 14* provides 33 MB or 66 MB of disk storage with 20 MB removability via the streaming tape, disk tape packaging.

THE ULTIMATE SOLUTION
With all the performance of the *ADES GYPSY* controller, the *SYSTEM 8* or *SYSTEM 14* can meet your total memory subsystem requirements.

GYPSY
At the heart of the *ADES* product line is the *GYPSY* Winchester/Streaming Tape formatter. By combining the disk and tape functions into a single card, the *GYPSY* provides unprecedented system capabilities.

With a 5 Mbyte/minute offline disk to tape transfer rate, a user can backup or restore a 20 Mbyte logical drive in less than four minutes. When operating in the "Transparent Mode," the host can still access the disk while the *GYPSY* moves data between the disk and streaming tape. In multiuser systems, individual users can backup or restore logical elements without affecting other users on the system.

MORE THAN JUST BACKUP
Compiling the *GYPSY* disk/tape commands with the direct tape access commands provides a system capable of Operating System load, Program Exchange and Selective File storage and retrieval. The streaming tape thus provides more than just backup.

EASY INTEGRATION
The power and flexibility of the *GYPSY* is only surpassed by the ease of host integration. With as few as five 7400-type components, the *GYPSY* can be interfaced to most mini or microcomputers.

EXPANDING HARDWARE SUPPORT
ADES currently supports Priam and Century Data Disks in conjunction with DEI, Archive and Cipher ¼" cartridge streaming tapes.

SUPPORT
ADES supports the most widely used micro-computers, and their operating systems.

GYPSY HOST INTERFACE ADAPTERS (GHIAs)
For the user who desires to bring up his system quickly, *ADES* offers S100 and Multibus host adapters in both Programmed 1/0 and DMA configurations. In conjunction with *ADES* software, the *GHIAs* provide a rapid means of integration, with minimal effort.

THE Z80 CONNECTION
For the Z80-based systems, *ADES* provides the GHIA-Z80 which allows connection of *GYPSY, SYSTEM 8* or *SYSTEM 14* directly to the CPU, thus eliminating the problems of specialized base configurations.

SOFTWARE
ADES support of CP/M™ and MP/M™ makes the *GYPSY* and SYSTEMS 8 and 14 easy to integrate and use. Support levels range from the "non-programmer" and user to the systems integrator configuring high performance MP/M™ systems.

CP/M
The *ADES "BIOS ATTACH"* program allows a user to configure the program to his system configuration, and begin using the disk/tape subsystem as an integral system resource under CP/M 2.2.

MP/M
For the system integrator who must design a complete BIOS or XIOS, *ADES* supplies a series of detailed application notes. These publications allow quick and complete integration of *ADES* subsystems into all system applications.

UTILITIES
All disk/tape subsystems running with CP/M are also supported with an array of utility programs. Format and Verify, Defect Compensation and Backup and Restore are only a few examples.

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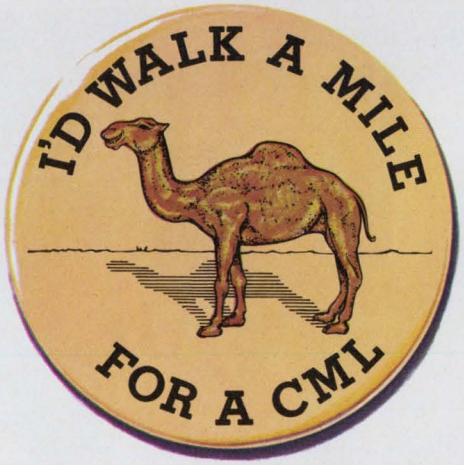

This month the Gate Array Supermarket features CML (Current Mode Logic). Like the ship of the desert it is dependable with a five mask process, high radiation immunity, and on chip regulators. Our CML is fast, prop delay 7ns and clock rate 20MHz and efficient with a speed power product less than 1.0pJ.

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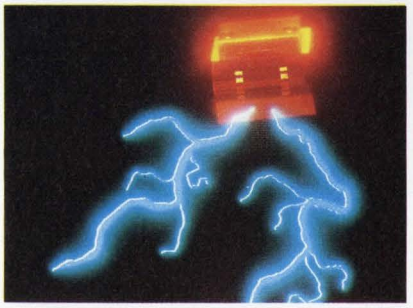

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Our cover photo symbolizes the latest generation of desk-top computers and the boards that go into them. Coverage of desk-top computers is on pages 64-73. (Cover courtesy of Augat, 33 Perry Ave., Attleboro, MA 02703: cover photography by Steve Grohe, 186 South St., Boston, MA 02111.)

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DILOG GOES WITH LSI-11, PDP-11, VAX-11*

Dilog offers the widest range of single board DEC emulating disc and magnetic tape controllers for LSI-11, 11/2, 11/23, PDP-11 and VAX-11 compatibility.

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DISC—5¼″, 8″ or 14″ WINCHESTER/SMD/CMD/LARK/CARTRIDGE/FLOPPY controllers with RX02, RK05, RL01/RL02, RP02/RP03, RK06/RK07 and RM02/RM05 emulations and features like 22-bit addressing, 32 or 56-bit ECC, universal formatting (allows you to mix drive types on the same controller without hardware modification), and automatic media flaw compensation.

MAG TAPE—¼″ cartridge/½″ NRZI/PE, streaming or conventional couplers or controllers with TM11, TS03 and TS11 emulations.

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- DU 132 TS-11 emulating coupler with expanded buffering for streaming or conventional ½″ industry standard magnetic tape drives. One coupler can accommodate up to 4 drives at speeds to 125 ips, and you get dual density 800/1600BPI as an added feature. RT, RSX, RSTS and VMS software compatibility.
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- DU 218 RM02/05 emulating SMD disc controller for SMD and Winchester applications with full software transparency under RSX and RSTS as well as Media compatibility when used with 80 and 300 MB SMD (CDC 9762/9766) compatible disc drives.

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- DQ 444 CDC FINCH interface. Intelligent uP module mixes any two drives of this class with universal formatting. RL01/02 emulations. Built-in drive capacity expansion handling.

All DILOG controllers are price competitive with significant OEM discounts being offered under a Mix and Match plan. 30-day delivery is standard. Distributor inquiries invited. For complete price/performance details, contact DILOG.

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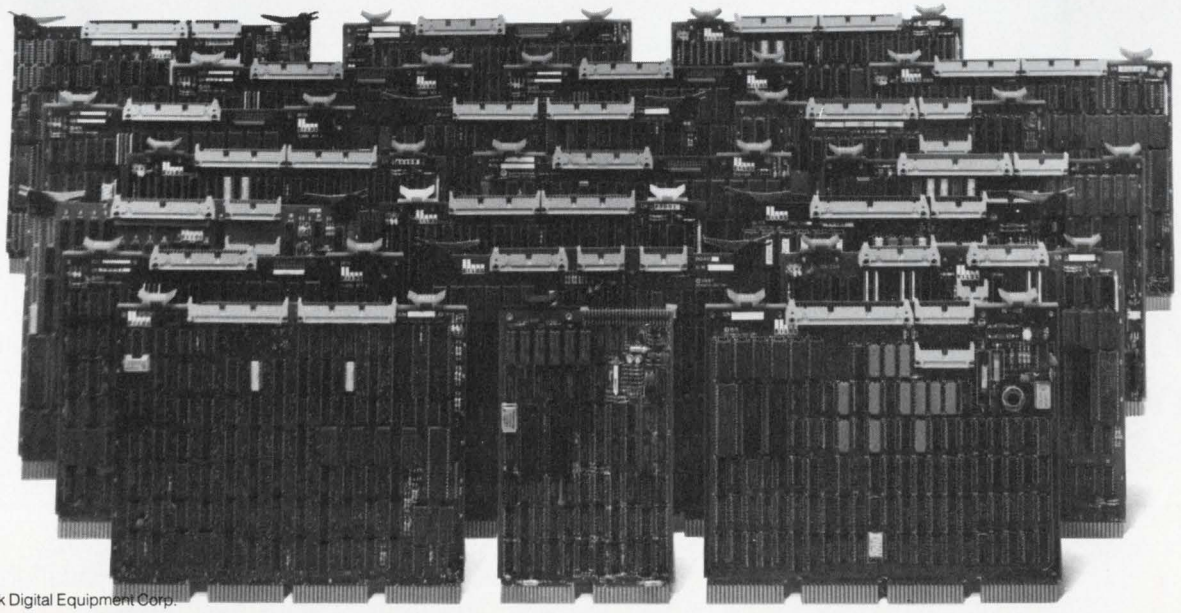

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Ampex is a leader in high-capacity Winchester technology. We've put together an aggressive, highly-experienced disk engineering group and it's paying off in disk drives that are configured to span the entire spectrum from 4 megabytes to 1 gigabyte. Take our new high-capacity drive families: 14″ Capricorn disk drive with 165 and 330 megabytes; 8″ Scorpio disk drive with 50 and 83 megabytes; and 5-1/4″ Pyxis disk drive with 4, 8, 12 and 16 megabytes. They combine outstanding technical innovation with high performance and cost-

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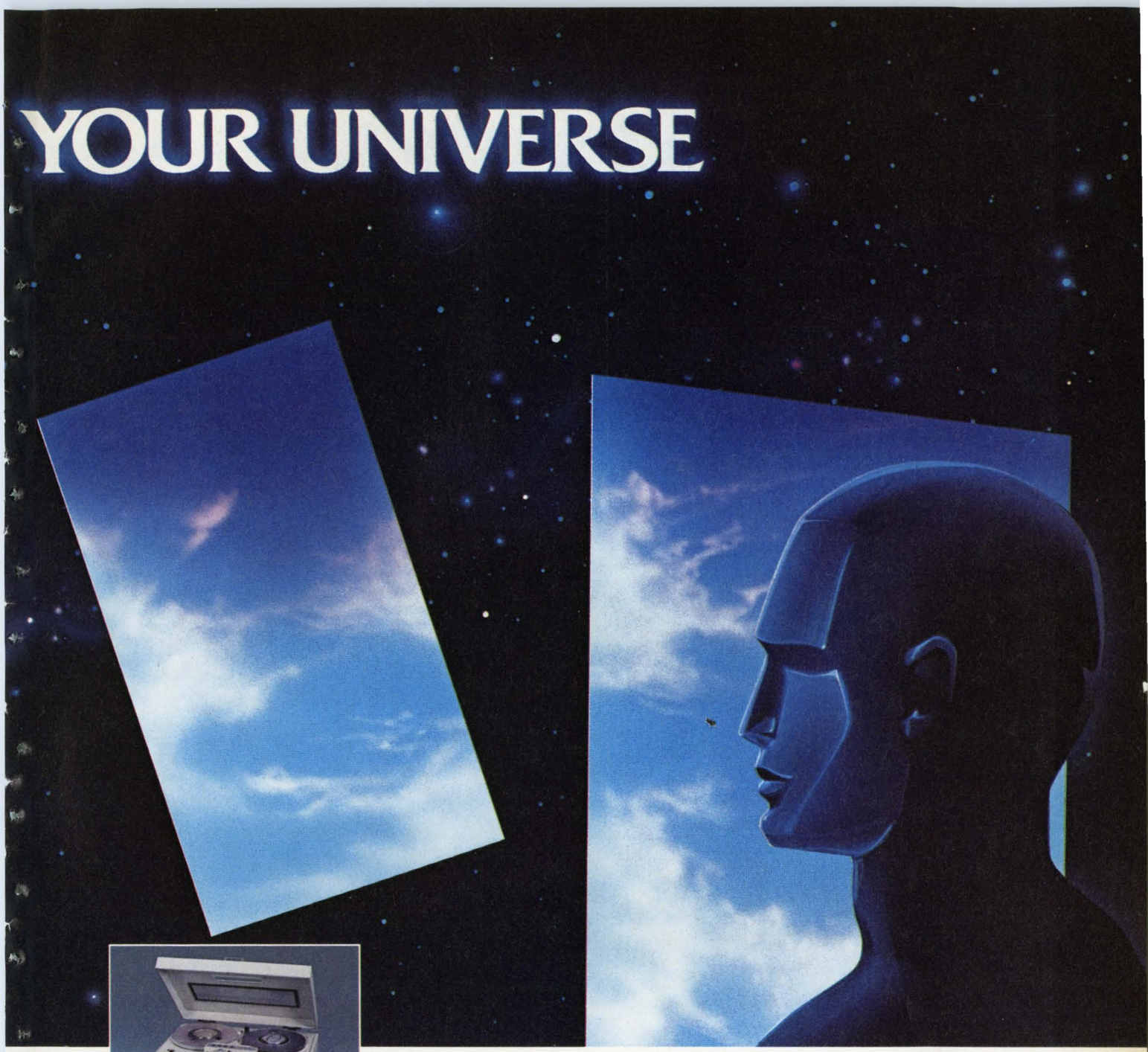

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effectiveness. And we back them up with our new Virgo 1/2″ 40 megabyte IBM format compatible streaming tape drives and our fixed/removable media Superwinchesters in 16/16, 48/16, and 80/16 megabyte capacities. We're high performance in our technical support, too, as well as in clean-room production capabilities that mark us as a major manufacturer committed to Winchester technology now and in the future.

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What's Coming in July:

SINGLE BOARD COMPUTERS – *The article on single board computers will cover the economics of single board products, why OEMs should consider them, and for what applications OEMs should choose them. In addition to the "whys", West Coast Editor Bill Groves will cover the "hows", exploring some specific applications for single board computers.*

SOFTWARE – *To tie in with the summer-time graphics conferences (NCGA and SIGGRAPH), the DIGITAL DESIGN July software feature will include the exclusive introduction of an advanced new graphics software package. Also, there will be a discusssion of microcomputer operating systems.*

HARDWARE, PACKAGING, AND INTERCONNECTS – *Chip interconnection is the focus of our July feature on hardware, packaging, and interconnects. East Coast Technical Editor Nicholas Mokhoff will discuss several different hardware interfacing and packaging alternatives, including a number of solutions that were presented in papers at this year's Electronics Components Conference.*

RASTER COLOR DISPLAY TERMINALS – *The July issue will showcase these terminals and describe their capabilities.*

SHOW COVERAGE – *Show features slated for July include reviews of SIGGRAPH and COMDEX.*

Letters

S-100 Interface Needed

Dear Editor:

I need your help in finding an S-100 interface card to a CalComp model 114 disk drive. These drives (which originally cost about $20,000 each) are very rugged mechanically and the removable disk packs can each store about 30 MBytes. Unfortunately, this drive does not have an SMD interface.

I thought I had found an electronic development company on the West coast to build an interface but the press of other business has shelved the project for two years with no completion date in sight. Hence I'm again looking for a supplier.

There were thousands of these drives built and they are now being replaced by newer technology so it seems there is a market for an S-100 card. I have complete technical information on the drive which I'll make available if needed.

Ron Tipton
The Systems Shoppe
104 E. Main St.
PO Box 227
Greenwood, MO 64034

Tell Us Your Thoughts

Digital Design is your forum. Your input helps keep the magazine interesting and vital to the design community. So let us know how you're doing and how we can serve you better in the future.

If you have any thoughts your peers should know about, put them in a letter to:

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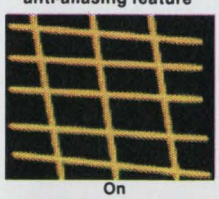
Da Vinci would have traded all his notebooks for this new AED767 graphics terminal.

Today, Leonardo da Vinci's notebooks are priceless objets d'art. They also contain many unique engineering concepts, like the one shown above of the iron framework he designed to reinforce the head and neck moulds for 'Il Cavallo', the horse. Although da Vinci worked periodically on 'Il Cavallo' for 16 years, the gigantic bronze statue, which was to stand some 26 feet tall, never materialized.

AED 767's unique anti-aliasing feature



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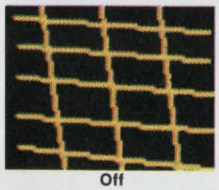

Off

Instead, his patron, the Duke of Milan, used the casting bronze for canons in a war against France.

But what took Leonardo many years to devise could have been achieved in mere hours with the help of AED's new 767 color graphics and imaging terminal. Available in desktop or 3½" high rackmount configuration, this new CAD machine has the kind of innovative features you'd expect only from AED. Features like built-in anti-aliasing (which virtually eliminates jagged lines common to raster-generated vectors). 1K x1K x 8 virtual address space. 768 x 575 pixel viewing window. Up-to-256 simultaneous colors from a palette of 16.8 million. A blue line reference grid that doesn't utilize video memory. Plus a refresh rate, adjustable from tv standard to flicker-free 45 Hz.

The AED767 gives you smoother drawings than any CAD station on the market—and at lower cost. So be a latter-day 'da Vinci' and use the best computer-aided design tool at your disposal. The AED767.

Advanced Electronics Design, Inc., 440 Potrero Avenue, Sunnyvale, CA 94086. Phone 408-733-3555 Telex 357-498. Outside California, Hawaii and Alaska call 800-538-1730.

All images shown taken from screen of AED767.

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Calendar

July 6–9

Increasing Software Productivity Tools and Techniques. Washington, DC. Provides an understanding of tools to improve software productivity. Includes manual techniques and off-the-shelf support tools. Covers: program techniques, management control and tool use, and new technology in LANs, networking, etc. Continuing Engineering Education, George Washington University, Washington, DC 20052. (202) 676-6106.

July 12–13

Speech Recognition and Synthesis Technology. New York, NY. Covers: speech production and perception, variability, automatic speaker identification, assessing current products, applications and emerging products. Contact: Carol Clark. McGraw-Hill Seminar Center, 305 Madison Ave, Room 3112, New York, NY 10017. (212) 687-0243.

July 12–16

Software Summit Series. Orlando, FL. Five one-day seminars cover: software acquisition, structured methodology for development, software configuration management, software quality metrics and computer-aided software. DPMA Seminars, Dept. SWS, 5959 W. Century Blvd., Suite 1016, Box 91295, Los Angeles, CA 90009. (212) 670-2973.

July 12–16

Computer Software With Industrial And Engineering Applications. Covers: software hierarchies and system organization, a sampling, hardware/software for data acquisition, signal analysis, spectral analysis, correlational analysis and digital filtering, extraction of signals from noisc using statistical processing algorithms, Kalmar filtering and signal estimation/detection. Office of Graduate and Continuing Studies, Wels House, 1 Union Ave., Union College, Schenectady, NY 12308. (518) 370-6288.

July 13–16

Intelligent Robots: Integration of Microcomputer and Robotic Technology. Covers: applications, mechanics, sensory components, software, dexterity, work space, coordinate frames and intelligence. Continuing Engineering Education, George Washington University, Washington, DC 20052. (202) 676-6106.

July 13–16

Software Project Management. Boston, MA (July 13–17); also Los Angeles (July 20–23) and San Diego (Sept. 21–24). Covers: methodology for avoiding cost/schedule overruns and unreliable, unmaintainable software for real-time micro/mini projects. Contact: Ruth Dordick. Integrated Computer Systems, 3304 Pico Blvd, Box 5339, Santa Monica, CA 90405. (212) 450-2060.

July 13–16

Hands-On Pascal Workshop. San Diego, CA. Covers: coding, partioning problems and structured problems, driving external devices with Pascal modules, and I/O interfacing. Integrated Computer Systems, 3304 Pico Blvd, Box 5339, Santa Monica, CA 90405. (213) 450-2060.

July 19–21

Summer Computing Simulation Conference. Marriott-Center City, Denver, CO. Lawrence Sashkin, Program Director. The Aerospace Corp, Box 92957, Los Angeles, CA 90009. (213) 648-5934.

July 19–22

Planning A Digital Data Acquisition and Control Computer System. Schenectady, NY. Covers: interconnection of devices from sensors to final control elements, on-site testing and built-in documentation. Office of Graduate and Continuing Studies, Wells House, 1 Union Ave, Union College, Schenectady, NY. (518) 370-6288.

July 19–22

Software Quality Assurance. Edison, NJ. Provides in-depth study of methodology, procedures and administration functions. Stat-A-Matrix Institute, Box 2021, Menlo Park Station, Edison, NJ 08818. (201) 548-0600.

July 20–21

Symposium on Reliability in Distributed Software and Database Systems. Pittsburgh, PA. Contact Prof. Bharat Bhargava, Computer Science Dept. A-319, University of Pittsburgh, Pittsburgh, PA 15260. (412) 624-6448.

July 20–23

Speech Synthesis and Recognition: Voice I/O For Computers. Boston, MA. Covers: voice processing algorithms/software, VIO hardware/systems, speech synthesis techniques, designing voice recognition systems and implementing VIO systems. Integrated Computer Systems, 3304 Pico Blvd,. Box 5339, Santa Monica, CA 90405. (213) 450-2060.

July 26–30

Microprocessor And Microcomputers: Theory And Applications. Washington, DC. Continuing Engineering Education, George Washington University, Washington, DC 20052. (202) 676-6106.

July 26–30

Siggraph '82. Boston, MA. The ninth Annual Conference on Computer Graphics and Interactive Techniques will have over 140 exhibitors in computer graphics with courses and technical sessions. Contact: Elaine Sonderegger, Conventures, Inc., 45 Newbury St, Boston, MA 02116. (617) 267-3456.

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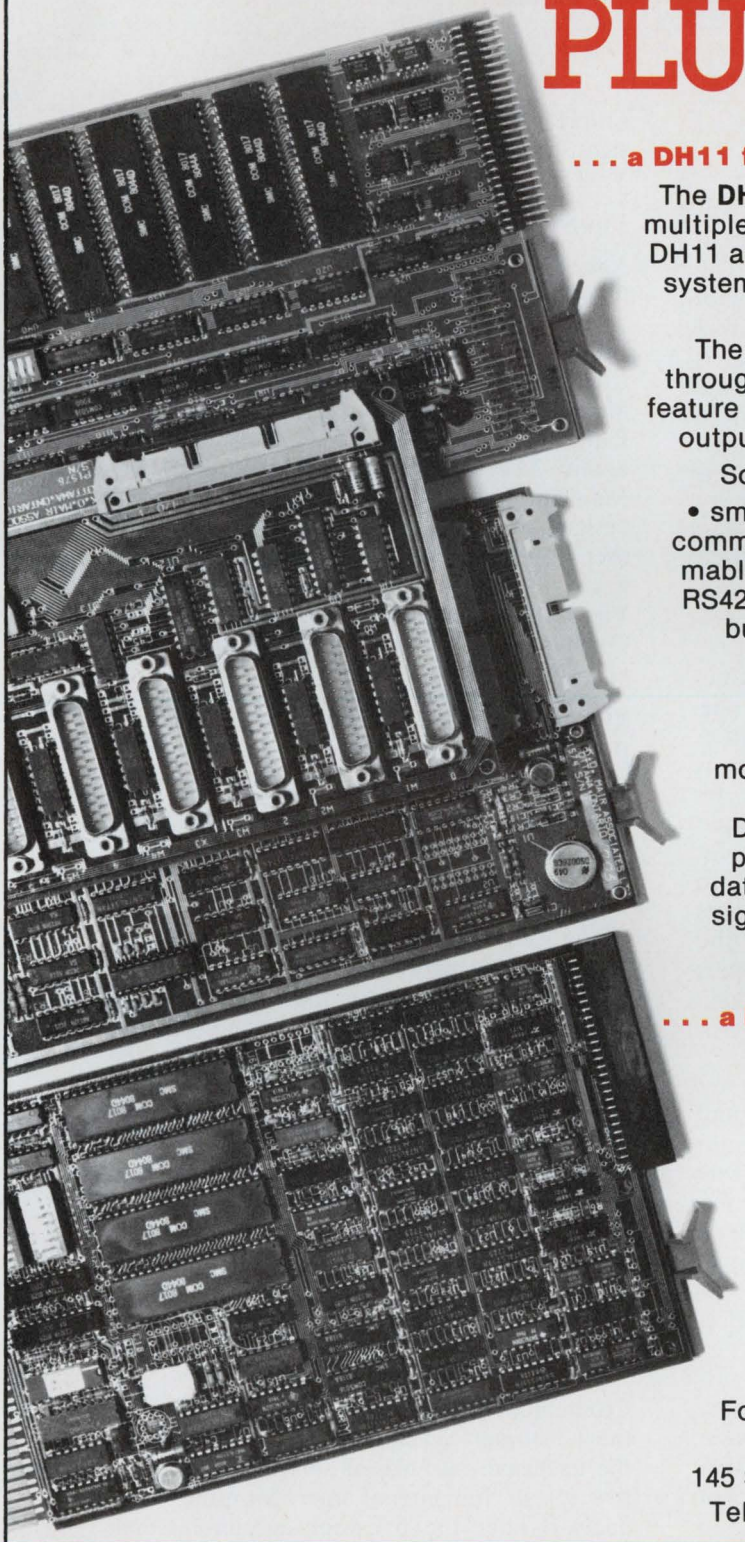

. . . a DH11 for the LSI-11

The **DHK11** is an eight line serial asynchronous multiplexer. Software compatibility with Digital's DH11 allows DHK11 operation with all operating systems that support the DH11 such as RSX11, RSTS and UNIX.

The DHK11 outputs data direct from memory through eight independent DMA channels. This feature relieves the LSI-11 from having to handle output data on a character-by-character basis.

Some other features of the DHK11 include:

• small size — only two dual size cards • all common baud rates to 19.2K baud • programmable line parameters • RS423 (RS232C) and RS422 capability • 64 character FIFO receive buffer • PCB distribution panel with eight DP25P type connectors

The **DMK11** is a dual size board option available for the DHK11. It provides full modem control for up to eight modems and is software compatible to Digital's DM11-BB modem controller. A distribution panel board is provided that combines the data signals for the DHK11 with the modem signals of the DMK11 into eight DP25P type modem connectors.

. . . a DZV11 at ½ the size

The **DZM11** is a four line serial asynchronous multiplexer for the LSI-11. It provides complete software compatibility with Digital's DZV11 plus:

• small size; one dual board half the size of the DZV11 • additional modem control; 7 signals per modem • split baud rates; independent receive and transmit baud rates can be configured • RS423 (RS232C) and RS422 capability • low power consumption.

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News Update

Jupiter Systems Formed For Color Graphics

Jupiter Systems, Inc. of Berkeley, CA, was formed to develop and manufacture a line of sophisticated color graphics terminals. The first product is a 768×575 raster graphics terminal with 256 simultaneously displayable colors. Hardware and software expertise is being provided by Jupiter Vice Presidents Pete Harris and Jack Klingelhofer. Prior to joining Jupiter Systems, Harris and Klingelhofer designed color graphics terminals for license by Videographics. Their 512×512 design has been manufactured and marketed by AED for the past three years and is widely used throughout the industry.

Table-Top Laser Plotter

Benson, Inc. of Mt. View, CA, a manufacturer of graphics hardcopy equipment, announced a laser-optics, high-resolution table-top plotter, the Laserwriter. Output copy is high-contrast, black-on-white, which may be produced on a variety of media. Finished copy is completely dry and automatically cut to size. Output resolution is 200 dots/inch in both directions and integral character fonts are on a 16-by-16 matrix. Print time for the first 8.5″ page is 12 sec. Consecutive copies require 7 sec. each. Paper speed is 1.73 ips. Prices are $6.15k to $8k.

Able Offers Three Computers

Product diversification is accelerating, and firms that began as plug compatible manufacturers are broadening their offerings. One recent example is Able Computer's upcoming foray into computers. Identified as the 44 Magnum Computers for OEM Applications, the new Able 44 Magnum Computers for Field Operations and Magnum+ for Office/Communications Systems and three new systems mark Able's entry into computer systems. Also introduced, the VaxDH, a VMS-compatible, 16-line DMA multiplexer, significantly outperforms the 16-line DEC DH-11AE. VaxDH is the latest in a series of DMA multiplexers made by Able for use in Magnum and DEC UNIBUS systems. It extends the utility of the Able VaxDZ and the Able DH/DM, each of which may be migrated up or down to meet varying user needs by simple PROM set exchange. One-board-design is common to the VaxDZ, DH/DM and VaxDH.

Via Systems To Enter IC Design

Via Systems, Inc. of Nashua, NH, announced its formation and entry into the interactive graphics systems market. Following two years of development and with funding from Charles River Partnership of Boston; Morgenthaler Associates, Cleveland, OH; Pathfinder Venture Capital Fund, Minneapolis, MN; and North Star Venture, Inc., Minneapolis, MN, Via Systems, Inc., will design, manufacture and market a single-user, turnkey, interactive graphics (CAD/CAM) system for use in the design of VLSI. Via Systems acquired all the assets of DMT Corp, a New Hampshire-based interactive graphics company.

Floating Point Systems Leases Array Processors

Floating Point Systems of Beaverton, OR, and Decimus Corp. of San Francisco, a subsidiary of BankAmerica Corp. announced a leasing program that lets Decimus lease FPS-164 Array Processors.

The FPS-164 is a powerful, high-speed 64-bit arithmetic processor that attaches to a host computer to process the computationally-intensive portions of engineering and scientific computer programs. As a result of the agreement, prospective FPS-164 users now have the option of leasing array processors from Decimus, as well as purchasing them outright from Floating Point Systems. Documentation, software support, installation, training, spare parts inventory, and service/maintenance agreements will all continue to be handled by Floating Point Systems for Decimus lessees.

TRW Services Cromemco Micros

Cromemco of Mt. View, CA, has selected the Customer Service Division of TRW as the exclusive authorized service representative for its full line of microcomputer products. Under the five-year agreement, nationwide service of Cromemco products commenced on April 1, 1982 from 30 locations, with additional locations to be established.

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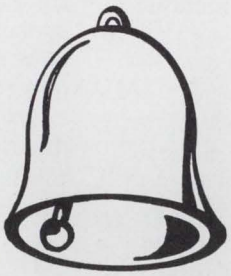

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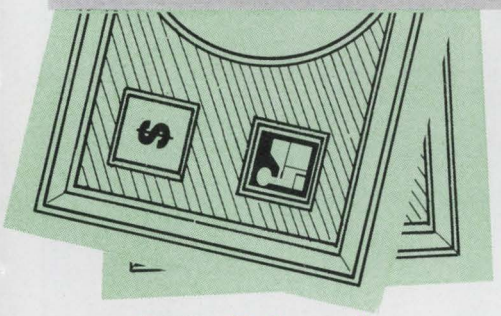

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News Update

National Introduces All-CMOS SBC Line

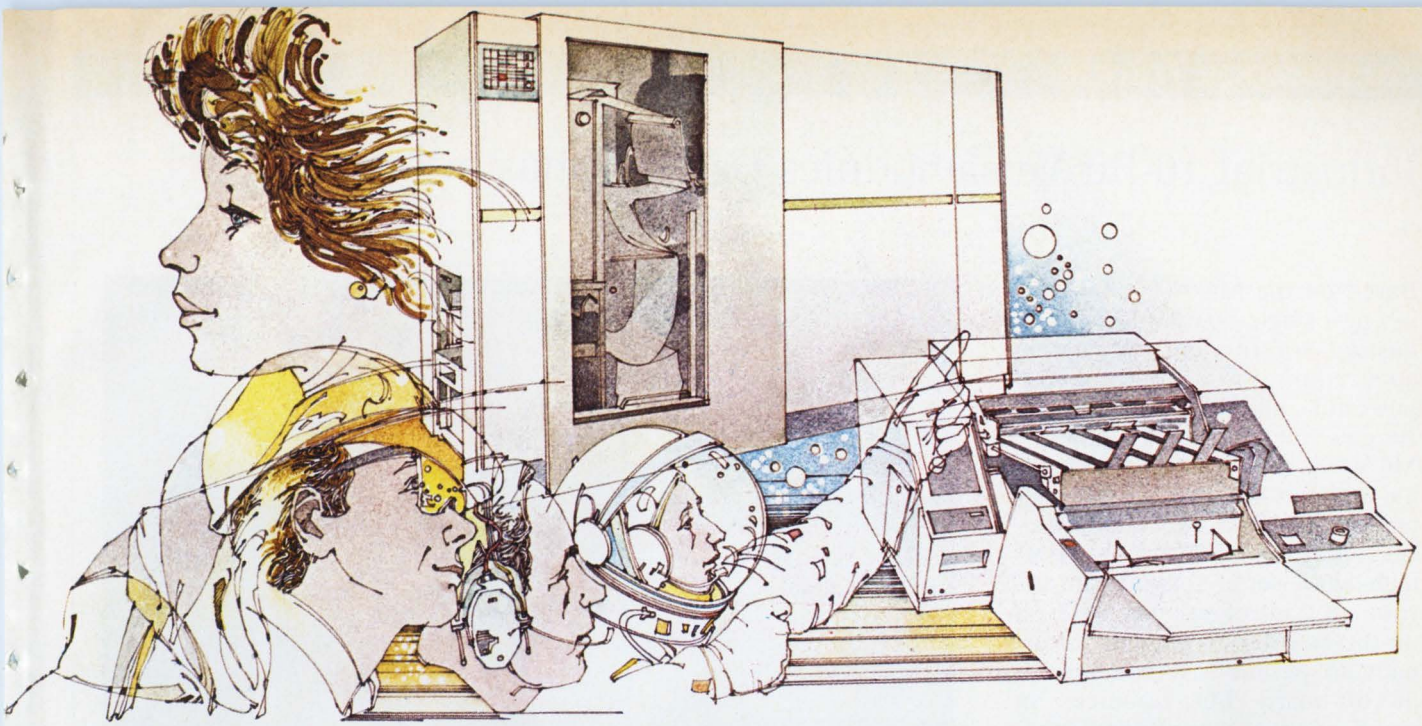
The rush to CMOS single board computers and memories continues to gain new semi houses and OEMs. Latest entry is National Semiconductor of Santa Clara, CA. National has just made available the first 19 members of the new Series/800 line of CMOS Industrial Microcomputer (CIM) boards. The new line uses the single-wide Eurocard format, and is based on the company's NSC800 P²CMOS. Targeted for applications in harsh environments, the new board line functions over an operating range of -40°C to +85°C. Power dissipation is as little as 1/30th that of equivalent NMOS functionality.

The single-wide Eurocard format was chosen by National for the new CMOS Series/800 board line because its form factor allows the electronics enclosure to be relatively small; it allows the user to purchase only the functionality he requires for his application.

Joint Support For 68000 Family

Three major US semiconductor manufacturers joined forces to support the 68000 family. Motorola, Signetics and Mostek will source 15 new VLSI components, all expected to be available in production, or for sampling, by the end of 1983. The line-up includes three new processor chips that extend M68000 compatible performance over a range from 8-bits to 32-bits, a microcomputer chip with on-chip memory and I/O and 11 VLSI peripheral chips that make 68000-based microcomputer systems applicable from control applications to very large systems with the power approaching that of current mainframe computers.

The combined projected offerings by these three companies, alone, will extend the 68000 product family to at least four compatible MPUs and 22 associated VLSI controllers and other peripherals by the end of 1983.



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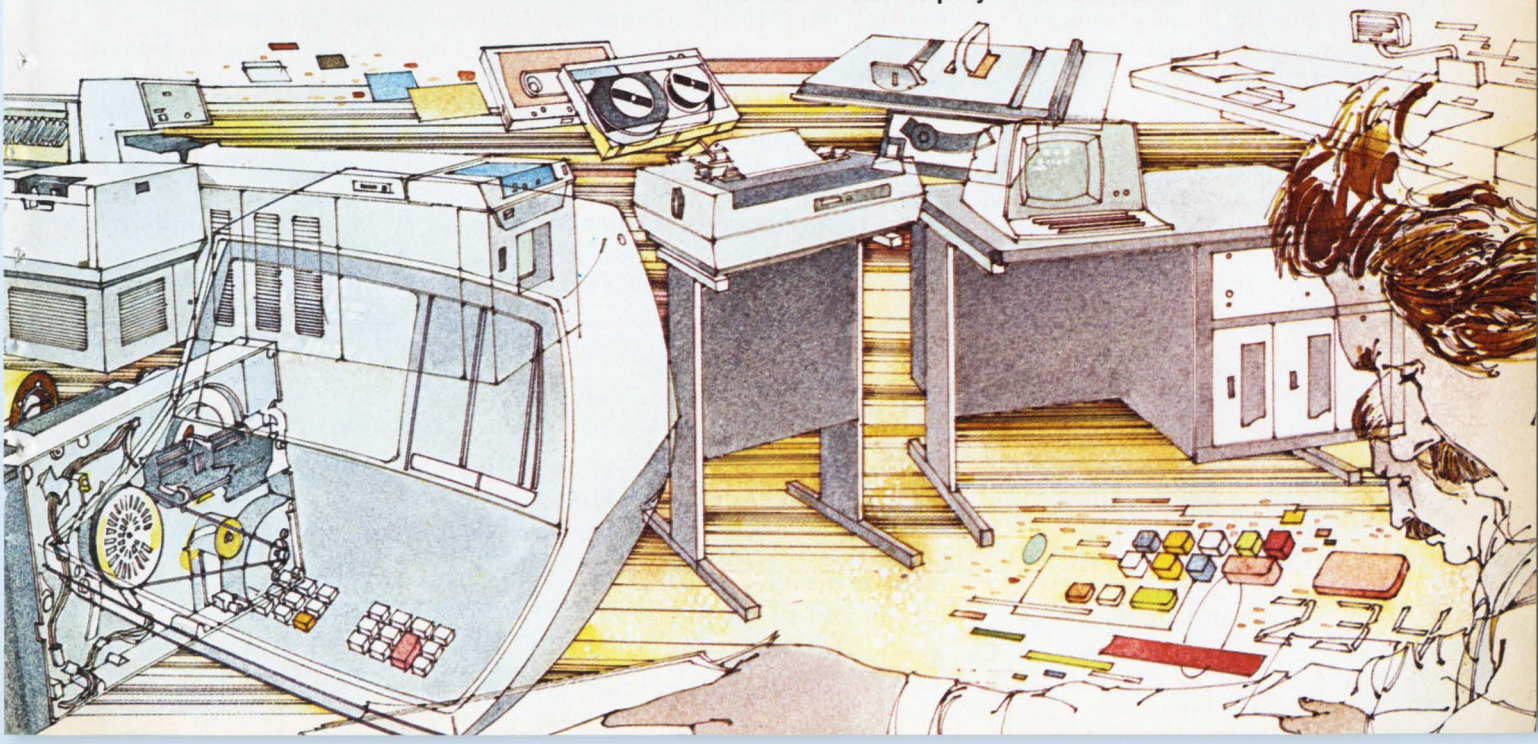

Industrial 16-Bit Versamodules Use Versabus Interface

Based on the MC68000, Motorola's new single-board micro for industrial control and automation applications is one of the most powerful microcomputer board systems yet developed using the MC68000. This M68KVM02 module uses the standard Versabus interface. It offers two multiprotocol serial I/O ports to support high-speed serial networks in distributed control systems. A local on-the-board bus extends externally to permit easy assimilation of off-board I/O resources in small modular configurations. DMA is via 128K bytes of on board dual-port RAM.

Extension of the local bus feature, called the I/O channel, is a physical extension of the on-the-board bus by means of a 50-pin ribbon cable that can be up to 12 feet long without degrading I/O performance. With the I/O channel system, I/O functions can be added in small, modular amounts external to the main Versamodule card cage. The I/O channel feature allows I/O transfers to proceed at rates of up to 2 Mbytes/sec, independently of any on-going activity in the higher speed Versabus system interconnect.

Supporting I/O capability, Motorola offers a variety of compatible I/O modules to meet some of the common industrial needs. Included are D/A and A/D converters, solid-state relay I/O, TTL compatible I/O, and RS-232C Serial I/O boards. All of these I/O modules are available in either single or double Eurocard format (5¼ × 16″ board with field-wiring termination strip and provisions for signal conditioning).

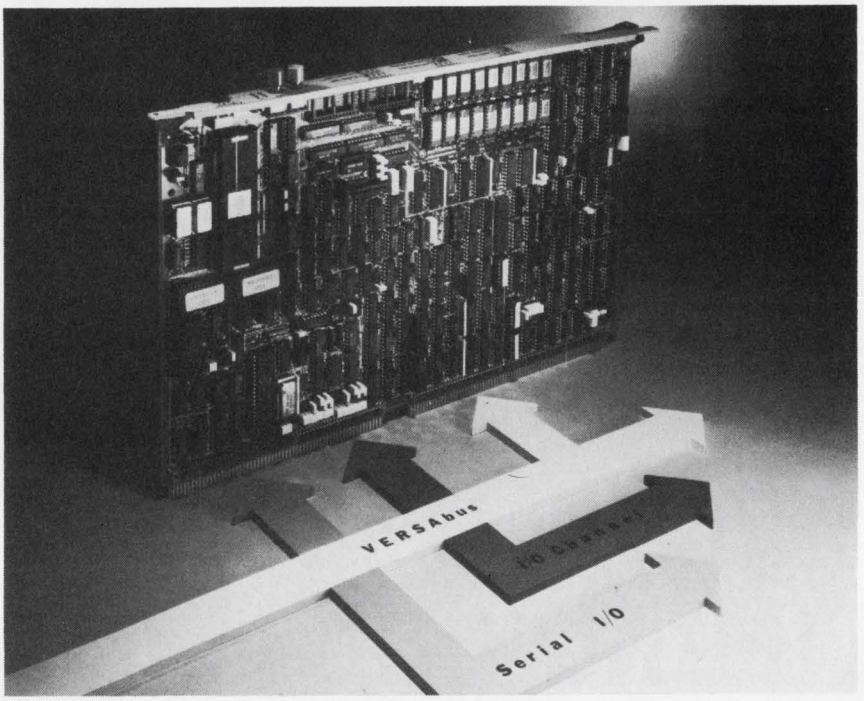

Figure 1: Motorola's newest monoboard microcomputer, M68KVM02, incorporating the MC68000, is especially designed for industrial applications. A separate I/O Channel permits use of diverse interactive peripherals without impacting VERSAbus system interconnect operation.

Real-time software support for the M68KVM02 board is with the Motorola Versados real time multitasking disk operating system with file management capability, and the RMS68K real time multitasking ROMable executive package.

The MK68KVM02 board is also supported by a wide range of intelligent peripheral control and memory expansion modules such as a Universal disk controller, a floppy controller, a color graphics controller, plus a 32/64/128K byte dynamic RAM module and a 256/512K byte dynamic RAM module with error correction.

Motorola quotes a price of $3900 for the M68KVM02-3 monoboard computer with 128K of RAM. Substantial price discounts are available to OEMs on large quantity purchases.

This microcomputer board looks like it will find many industrial control and automation applications, especially in areas like robotics. It appears to have the I/O flexibility needed for a wide range of applications requiring a full 16-bit microcomputer.

—Groves

Oxide-Isolated CMOS Gate Arrays

Using an oxide isolated silicon gate CMOS process, Universal Semiconductor of San Jose is offering six gate arrays ranging from 360- to 1500-gate complexity. These arrays can be produced in either 3-micron gate width technology for high speed (75-MHz toggle rate), or in 6-micron technology for standard performance (30-MHz toggle).

A choice of 1- or 3-ns propagation delays are available depending on gate width. The arrays offer the low power consumption characteristic of CMOS devices with high noise immunity. The oxide isolated silicon gate process

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Technology Trends

LOGIC CELLS AVAILABLE	ISO-3 SERIES 3-MICRON			ISO-6 SERIES 6-MICRON		
	Tr	Td	Tpd	Tr	Td	Tpd
Inverter	1.35ns	0.45ns	0.9ns	4.3ns	1.7ns	3.0ns
2-Input NAND	1.5ns	1.0ns	1.25ns	4.5ns	3.5ns	4.0ns
2-Input NOR	2.85ns	0.55ns	1.7ns	9.5ns	2.1ns	5.8ns
3-Input NAND	1.6ns	1.7ns	1.65ns	4.8ns	7.0ns	5.4ns
3-Input NOR	4.4ns	0.6ns	2.5ns	13.0ns	2.5ns	7.8ns
4-Input NAND	1.7ns	2.3ns	2.0ns	5.0ns	7.0ns	6.0ns

COMMON FEATURES			ISO-3 SERIES 3 MICRON		ISO-6 SERIES 6 MICRON	
ARRAY SIZE	GATE COUNT	BONDING PADS	Tpd	Ftogg	Tpd	Ftogg
133 × 133 mils	360	44	1ns	75MHz	3ns	30MHz
133 × 165 mils	540	58	1ns	75MHz	3ns	30MHz
133 × 207 mils	720	64	1ns	75MHZ	3ns	30MHz
161 × 207 mils	960	70	1ns	75MHZ	3ns	30MHz
188 × 207 mils	1200	74	1ns	75MHZ	3ns	30MHz
188 × 240 mils	1500	80	1ns	75MHZ	3ns	30MHz

Figure 1: These six gate arrays from Universal Semiconductor range from 360- to 1500-gate complexity and can be produced in either 3-micron gate width technology for high speed, or in 6-micron technology for standard performance.

is also less expensive than metal gate CMOS. All of the arrays are CMOS, TTL, and LSTTL compatible with 15 mA sourcing capability. All outputs can be three-state. Source and drain contacts are fully programmable, and the I/Os can be guard-banded against latch up.

Each array consists of a series of geometrically balanced P-type and N-type devices which are stepped and repeated in the center portion of the chip. An individual cell comprises three complementary pairs and can accommodate a three input gate or a two input gate and an inverter. While the gate contacts are fixed, the source and drain contacts are mask programmable to facilitate the metal interconnect. Up to 12 interconnect traces can be routed over the logic cells, and up to 10 traces can be routed around the periphery between the array devices and the I/O devices. In addition, fixed metal paths running in the Y direction of the array permit long interconnects to be made without excessive time delays.

There are several approaches to designing an IC using Universal gate arrays. For engineers with the inclination and ability to do VLSI IC design, Universal can provide all the necessary tools including a design manual, macrocell library, planning and layout sheets, and applications and CAD support. For those organizations with internal CAD capability, the Universal data base and macrocell library can be supplied in gridded magnetic format. In cases where significant volumes are involved, Universal can work from a customer specification and provide all design and integration services.

The development charges for Universal arrays range from $6500 to $25,000, depending on the array and technology selected. Turn around for prototypes from finished design is 8 to 10 weeks.

—Groves

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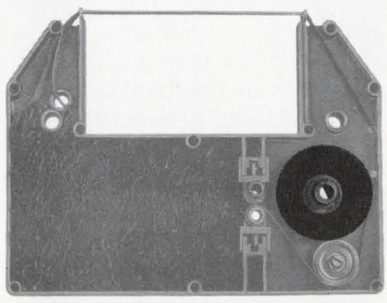

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Computers Penetrate Small Business Market

Market penetration of computers costing less than $100K into small businesses will surge in this decade, reaching 44% in 1985, 77% in 1990. That increase will be on top of a growing number of businesses suited to computerization in the first place—namely three million establishments by decade end, or 500,000 more than in 1980.

According to a study prepared by Frost & Sullivan (New York, NY), nearly four million small business computers will be sold during the 1980s. Most startling, more than 75% of these will be computer systems that cost less than $10,000.

During the 1980s, some $50 billion cumulatively will be expended by small businesses on computer systems in the US. Of that, $35 billion will be spent on hardware and systems software; $17 billion on applications software.

Since computer systems range widely in price, even within the "small business systems" category, the F&S study examines the marketplace in terms of well-defined price categories:

- Between $5,000–$10,000: The minimum for a business μC with software.
- Between $10,000–$25,000: This includes a high-end μC and low-end minicomputer systems.
- Between $25,000–$50,000: A single-terminal minicomputer system.
- Between $50,000–$100,000: A minicomputer with hard disk, perhaps several terminals, but not including "super-minis."

IBM Corp, according to the study, will dominate every price category but one: the $10,000–$25,000 range. Here, F&S believes, DEC will be the "leader throughout the decade."

Several Japanese companies also figure prominently in this market. These include Sharp, Sanyo, Canon, and Casio.

For further information, contact Customer Service, Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038; (212) 233-1080. Ask about Report 971.

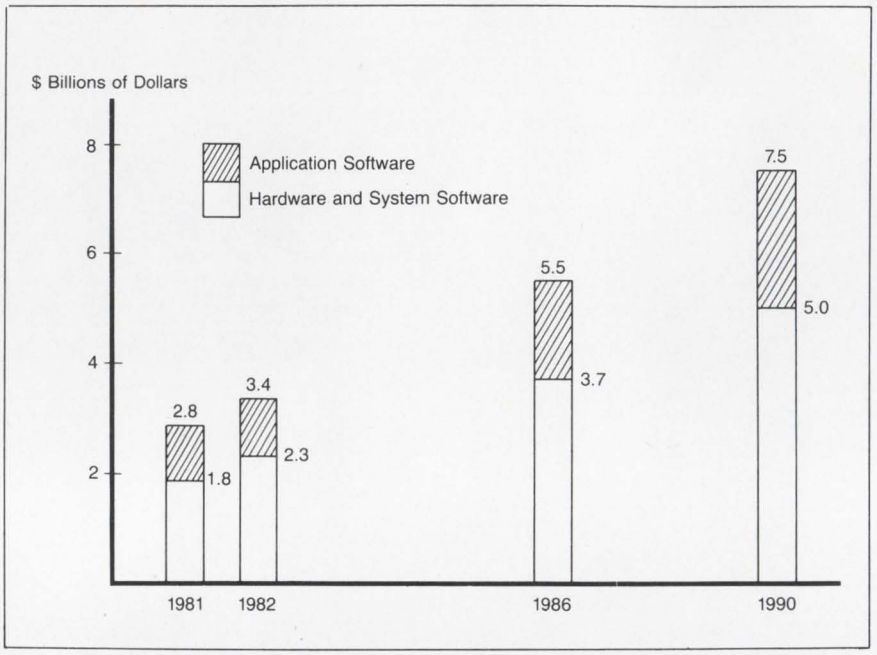

Figure 1: Sales of business computers will nearly triple during the 1980s, according to a recent Frost & Sullivan study.

European Robotics Market Growing

The European market for industrial robots will reach $572 million by 1986, as high labor costs, declining productivity and fierce international competition increasingly pressure companies to automate. Although the robot "boom" that has occurred in the United States has not reached Europe, the market is rapidly gaining momentum, according to a market analysis by Creative Strategies International of San Jose.

Over the next five years, the market is expected to grow at a compound annual rate of 58%. Growth rates will be highest through 1983, with many orders coming from companies that already have one or two robots and that now have sufficient operating experience to commit themselves to additional investment. The highly labor-intensive assembly application will exhibit the most dramatic growth through 1986: a compound annual rate of 80%. Assembly work is ideally suited for robots and this application may come to be the dominant sector of the European robotics market, in terms of units installed. With high unemployment rates, however, job security has become a major union issue, and union resistance to robots—especially in assembly task—will increase.

Although the robot is perceived as a multipurpose machine not limited to a particular task, most manufacturers have developed ex-

(Continued on pg. 26)

Ten-Element Bar Graph Displays Analog Signals In Digital Form

Multi-element bar graph LED ICs, such as the H-P HDSP-4820/4830 series of ten-element (standard red, high efficiency red and yellow) LED bar graphs, all offer designers advantages over panel meters and discrete indicators. They eliminate high parts counts, troublesome mechanical and optical alignments, and intensity and color variations, not to mention design headaches. Users need not worry about element-to-element matching within the package, and bar graph arrays may be easily stacked from an electrical and mechanical viewpoint, with interlocking mechanisms on bar graph ends for firm alignment.

Although displaying a digital output in bar graph format is common, it is perhaps more common to directly display an analog signal in digital format. These two circuits do this with minimum parts count.

The circuit in **Figure 1** displays a 0V to 5V signal on the HDSP-4830 high efficiency red bar graph array. The full scale reading is determined by the adjustable voltage at the REF OUT node. The LM3914 forces a nominal 1.25V constant voltage between REF OUT (pin 7) and REF ADJ (pin 8). In **Figure 1** this voltage is applied across resistor R1. Since this voltage is constant, a constant current flows through R1 giving an output voltage REF OUT as calculated: REF OUT = 1.25V (1 + R2/R1) + 1_{ADJ}(R2).

The value of R1 also determines the LED current. Approximately ten times the current that flows from REF OUT (pin 7) is drawn by each lighted LED. The calculation of LED current is: 1_{LED} = (1.25V/R1) (10).

Therefore, by choosing R1 for the desired LED brightness, and using the value of 1_{ADJ} stated in the LM3914 data sheet (75 μA typical), R2 can be determined. By using a potentiometer for R2, the value of REF OUT can be adjusted to the precise level desired.

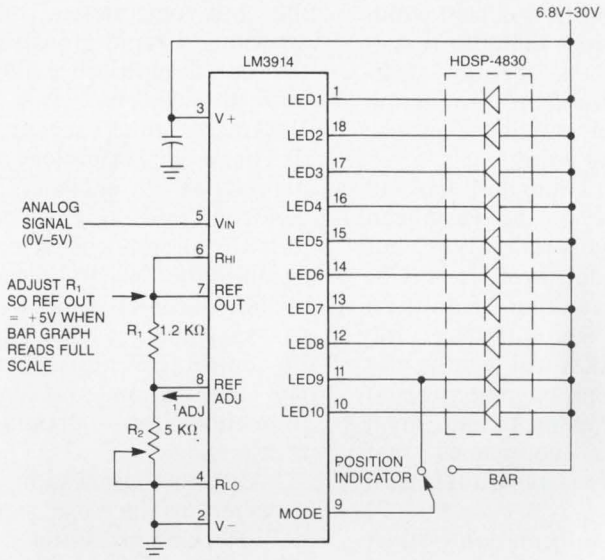

Figure 1: Bar graph circuit displays a 0V to 5V signal. R1 and R2 values shown may be varied to alter LED brightness and adjust REF OUT. Note the parallel LED arrangement.

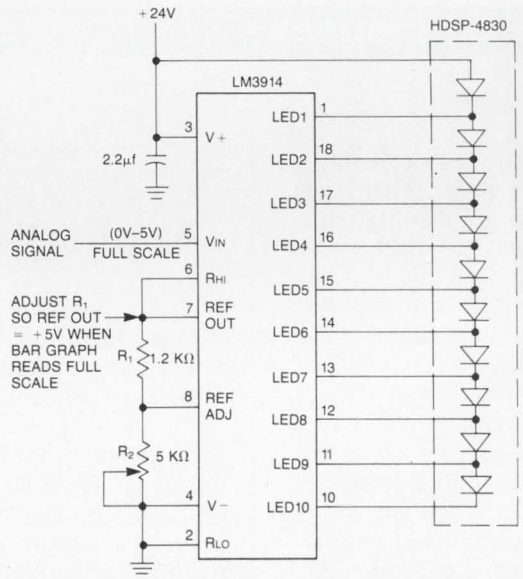

Figure 2: In this low power 0V–5V bar graph meter, the only change is that the LEDs are in series and LED 1's anode is connected to +24Vdc.

The LED current has been set nominally to 10 mA DC using the techniques described above. When operated in position indicator mode with Vcc = 6.8V, the power dissipation is approximately 110 mW. The worst cast power dissipation when operated in bar mode (10 elements on) is approximately 720 mW.

If low power dissipation and full bar graph decoding is desired, the LM3914 can be operated as shown in **Figure 2.** The LM3914 is again operated in position indicator mode. However, the ten

Market Trends

(continued from page 24)

pertise in one type or range of robots for specific applications. Flexibility and adaptability—the cornerstones of robot automation—are a more relevant commercial criterion than universality. Also, robots are not "gift-wrapped" solutions to production problems, and systems expertise is a vital selling point.

Historically, Unimation has had a major share of the European market for industrial robots, but this is now under threat from US, Japanese and other European competitors. New entrants to the European market will include major multinational engineering and electronic companies, and small entrepreneurial companies that offer specific products and services.

For further information contact Creative Strategies International, 4340 Stevens Creek Blvd., Suite 275, San Jose, CA 95129; (408) 249-7550.

Voice Industry Begins Expansion

Human speech interaction with computers has progressed beyond the embryonic stage. Today it is spawning a rapid-growth industry that could approach a billion dollars in sales by 1988. Gerald Beckmann, chief executive officer of Threshold Technology, told the nation's design engineers at a recent conference that "voice recognition is already cost effective for a multitude of applications that include materials handling, industrial machine programming, quality control, inventory control, office automation and anti-fraud protection for electronic fund transfers."

"And the application base is expected to increase significantly," Beckmann continued, "because of the combined effects of increased functionality and significantly lower costs."

Four circumstances in which voice communication is effective are:

- when information is needed immediately, without transcription delays.
- when the computer user requires mobility.
- when the user's hands and eyes are needed for other tasks.
- when the user is unskilled at typing.

A recent study conducted by the U.S. Navy reported that skilled keyboard operators performed data entry tasks 17.5% faster and reduced errors 64.6% using voice rather than a keyboard.

Beckmann noted that market forecasts by independent research organizations agree that voice recognition "is going to be a big business" but vary widely on the pace at which the market will evolve.

Applications Notebook

(continued from page 25)

LEDs are driven in series from a +24V power supply. The REF OUT voltage is adjusted so the bar graph reads +5V full scale. When VIN lies between 0V and +0.5V, no LEDs will be on. When VIN lies between +0.5V and +1.0V, Output 1 is enabled and LED 1 is illuminated. Each time the input voltage increases 0.5V, the 10mA sink moves to the next output pin, illuminating an additional LED. When the input voltage is +5V or more (+35V mixmum), all ten LEDs are illuminated with the same 10 mA. To the observer, the bar graph appears to operate identically to the one in **Figure 1** when in BAR mode. However, the worst case power dissipation has been reduced by approximately one-half to 380 mW.

Design Staff, Hewlett Packard, 640 Page Mill Rd, Palo Alto, CA 94304.

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When you send in your program or circuit idea, include enough detailed program or circuit description. "Should I worry about grammar?" is a question we're often asked. The answer is "No," since we will edit it. Include flow diagrams, printout, schematics, block diagrams and a detailed description. Please type and leave a space between each line.

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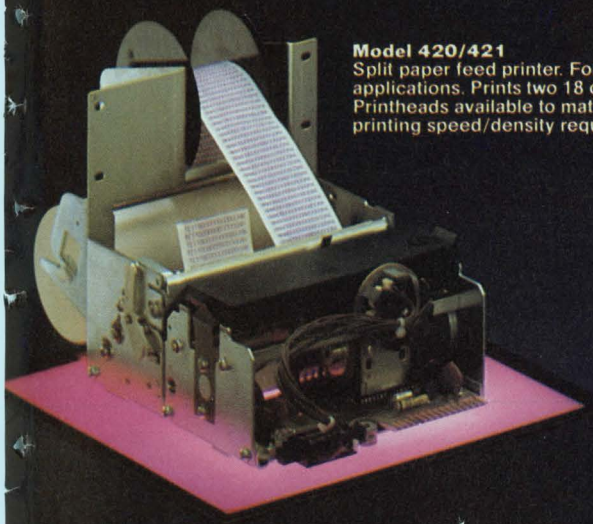

Model 420/421
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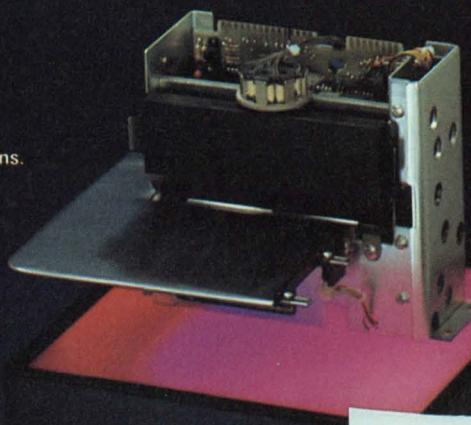

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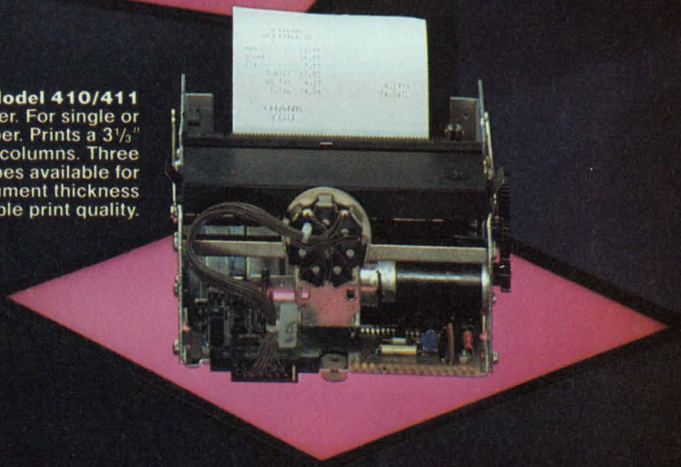

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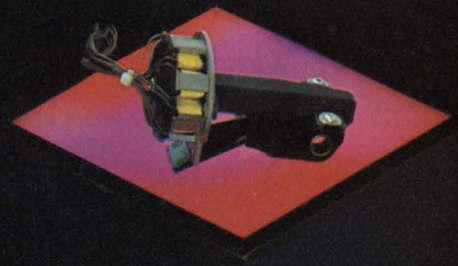

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SIGGRAPH '82: Art And Technology Find Common Ground

This year's SIGGRAPH conference, held July 26–30 in Boston, covers every phase of computer graphics.

by Bob Hirshon

Dedicated to the proposition that not all computer technologies were created equal, SIGGRAPH '82 combines the latest developments in computer graphics with a measure of *art nouveau* elitism. The result is a show generally regarded as the industry's most prestigious conference on computer graphics—and one which takes a good share of both praise and criticism for its staunch anti-commercialism.

When SIGGRAPH began nine years ago, they had no vendor exhibits; the show consisted entirely of tutorials and technical sessions. At this year's show, there will be 140 companies exhibiting their wares. But even with vendor exhibits, SIGGRAPH tries to maintain an educational, rather than a marketing, atmosphere. The vendor exposition is invaluable, according to SIGGRAPH, because it pro-

Figure 1: This picture was generated on a Cray 1 with a III FR–80 graphics device (courtesy Melvin Prueitt, Los Alamos National Laboratory).

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vides demonstrations of the latest in computer graphics hardware and software. The marketing angle is minimized; and, at a time when most conferences are stressing the number of qualified buyers they have among their exposition attendees, SIGGRAPH still provides student discounts. SIGGRAPH's goal is the widest possible dissemination of knowledge about computer graphics—not the greatest possible sales of vendors' products.

Graphics Courses

Classes are SIGGRAPH's main event; they are divided into three basic types: tutorials, seminars, and technical sessions. Tutorials are introductory courses, lasting one or two days each, that assume little prior knowledge of computer graphics and that stress fundamental principles. Seminars also last either one or two days, but are more specialized than tutorials, and generally are more advanced. Technical sessions are one or two hour classes that may be either presentations of technical papers or panel discussions on specific topics.

The 14 tutorials include four two-day classes, which are: Introduction to Computer Graphics; Low Cost Graphics; Computer Graphics Hardware; and The Application of Computer Graphics to Engineering, Scientific, and Design Problems. The ten one-day tutorials are: Introduction to Raster Graphics; Psychology for User-Computer Interfaces; How to Design User-Computer Interfaces; Device-Independent Graphics Software; Two-Dimensional Computer Animation; Presentation and Publication Graphics; Graphics and Data Bases; Distributed Graphics and Communications; Computer Graphics in Office Animation and Electronic Publishing; and Demographics: Mapping, Marketing, and Computer Graphics.

The 10 seminars, each lasting one day, except where noted, are: Advanced Image Synthesis; Introduction to TV, Film, Video, Printing; Three-Dimensional Computer Animation; State-of-the-Art in Image Synthesis; Graphic Design and Information Graphics (2 days); Business Graphics for Managers; Introduction to the SIGGRAPH '82 Exhibition; Introduction to CAD (2 days); Solid Modelling; and Freeform Surfaces.

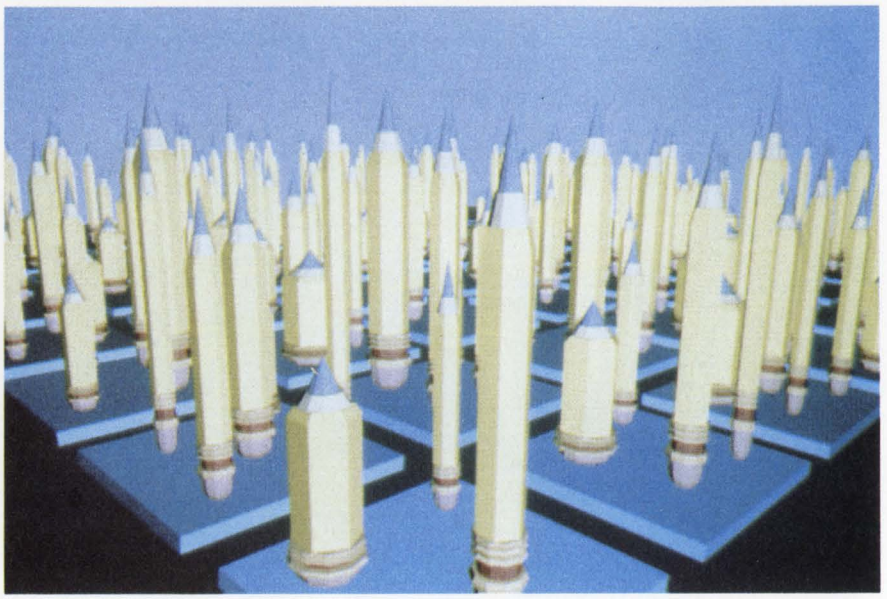


Figure 2: This picture, "Pencil City," was generated using a VAX 11/780 computer and a 640x512x32 frame buffer (courtesy Michael Collery, Cranston-Csuri Productions, Inc., Columbus, OH).

Running over the last three days of SIGGRAPH, the technical program consists of an opening session, with program review and awards presentations, 10 panel discussions, 11 technical sessions during which 37 papers will be presented, and a President's Forum.

Panel discussion will cover: The Impact of Graphic Standards; Professional Workstations; The Graphics CAD/CAM Industry: Financial Perspectives; Approaches to Solid Modelling; Voice Recognition as Input Technique; The Challenge of CAD/CAM Education; Graphic Input Interaction Techniques; Business Graphics—What is it?; The Role of Videotex; and Health and Safety Issues in Computer Graphics.

Technical sessions, featuring papers by industry experts such as James Blinn and Kellogg Booth, fall under 11 categories: Image Generation; Eurographics Session: Graphics Standards; Modelling; User Interface; Hardware Architecture; Visible Surface Algorithms; Data Base Applications; Applications; Curved Surface Display; Paint and Animation; and Raster Systems.

Finally, in the President's Forum, Donald Fedderson of Applicon, Ralph Linsalata of Lexidata, Peter Preuss of ISSCO, and Richard Spann of Adage discuss problems and opportunities in the computer graphics industry.

Vendor And Art Events

This year's SIGGRAPH features User Group meetings for a number of different graphics companies, and a two-day vendor forum presenting companies' introductions of new products. For the more artistically-oriented attendee, there will be a juried exhibition of computer-generated art running at the Sheraton Boston Hotel the entire week of SIGGRAPH.

Undoubtedly the most popular SIGGRAPH events are the evening videotape/film shows. The shows feature the finest computer-generated films and videotapes, shown under nearly-ideal conditions with the best audio-visual equipment currently available. Two shows are scheduled for this year, one presenting the best films and tapes produced in recent years—a sort of "oldies-but good-

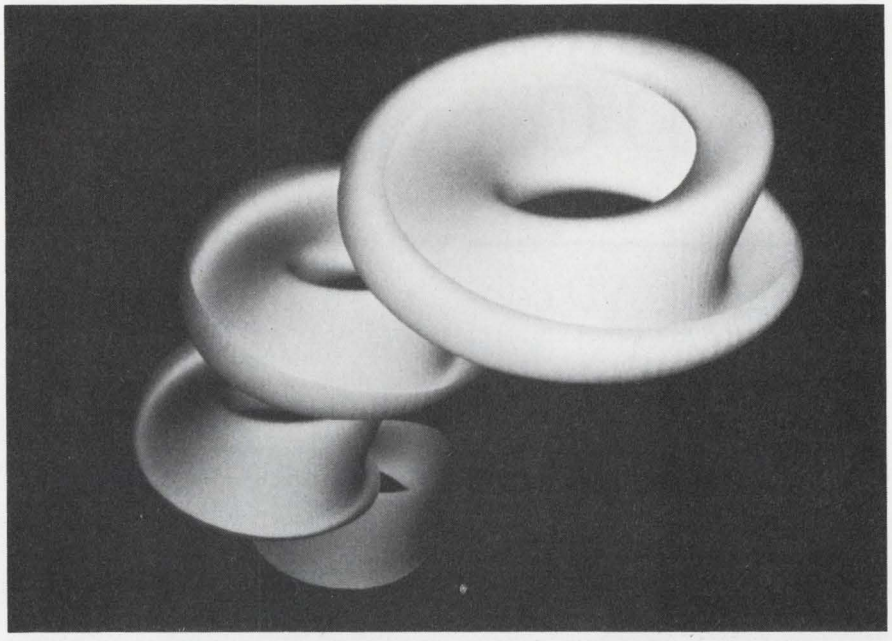


Figure 3: A Klein bottle assembled in four-space in such a way that the projections into three-space have a self-intersection curve that is the intersection of two mobius bands. This picture was generated using a VAX 11/780 running Unix, and a Ramtek 9400 with a 1280x1024x8 frame buffer (courtesy Dave Salesin, Steve Feiner, and Tom Banchoff, Brown University, Providence, RI).

ies" night—and the other showing all new material produced within the last year.

The popularity of the videotape/film shows reveals the thread common to all SIGGRAPH attendees; regardless of whether they've come to buy, sell, or learn, the thing that they find most attractive about the field is probably the technology's unmatched capacity for pure, dazzling artistry.

It is this artistic factor that sets computer graphics apart from—aficionados would say "above"—other computer technologies. Computer graphics maintains a certain measure of romance. Rarely in other technologies would one find the "art-for-art's-sake" vs. "art- for-money's-sake" debate raging so vitally.

And in the midst of that debate, SIGGRAPH thrives. Criticized for its snobbishness, praised for its conviction, SIGGRAPH remains, after nine years, one of the industry's few remaining class acts. □

Simplify The μP Interface To Your 12-bit A/D Converter

By D. C. Pinkowitz

Interfacing A/D converters (ADCs) with μPs depends primarily on the ADC data rate—the key to simplifying the interface is to recognize the I/O category that is most appropriate for the ADC.

A/D converters (ADCs) and μPs are companions in an endless variety of applications. The ADC digitizes real world analog parameters such as temperature, pressure and velocity, and the μP provides digital computation, processing and control. ADCs with a 12-bit resolution are available from numerous manufacturers with conversion times ranging from 1μs to 10ms. 8-bit μPs are good choices for processing 12-bit ADC output data, since they have powerful instruction sets, and are also inexpensive and widely available. For most applications, it is a simple matter to successfully interface 8-bit μPs with 12-bit ADCs.

The choice of interface technique used with the ADC and the μP depends primarily on the required ADC data rate. Conversion times which are long compared to a μP instruction cycle would waste valuable processor time if the processor were to idle while the ADC completes its conversion. For this reason, if the ADC conversion time is greater than 100 μs, it is best that the μP ignore the ADC until it receives an interrupt request. Slow ADCs in this category are best interfaced to the μP as isolated I/O. Self contained peripheral interface circuits, providing the required control and interrupt handshaking signals, are available to implement the isolated I/O interface.

A/D converters with conversion times faster than a μP instruction cycle would waste much of their data if programmed instructions were required to read the data. For this reason ADCs with conversion times faster than 1 μs are best handled with a Direct Memory Address (DMA) interface. A DMA interface requires a special DMA controller circuit, which stops the μP and takes control of the Address, Data, and Control Bus lines. ADC data is read directly into memory completely transparent to the processor.

The great majority of ADC applications require conversion times greater than 2 μs and less than 100 μs. Typical examples of multiple source 12-bit ADCs in this category are the DDC-5240 (5 μs), the ADC87 (10 μs) and the DDC-5200 (50 μs). These converters are best handled with a Memory Mapped I/O interface. With this simple interface technique the A/D converter is treated like read/write (RAM) memory. No handshaking is required.

Memory Mapping

At the expense of a small amount of memory address space, treating the ADC as memory mapped I/O yields the benefits of simple soft-

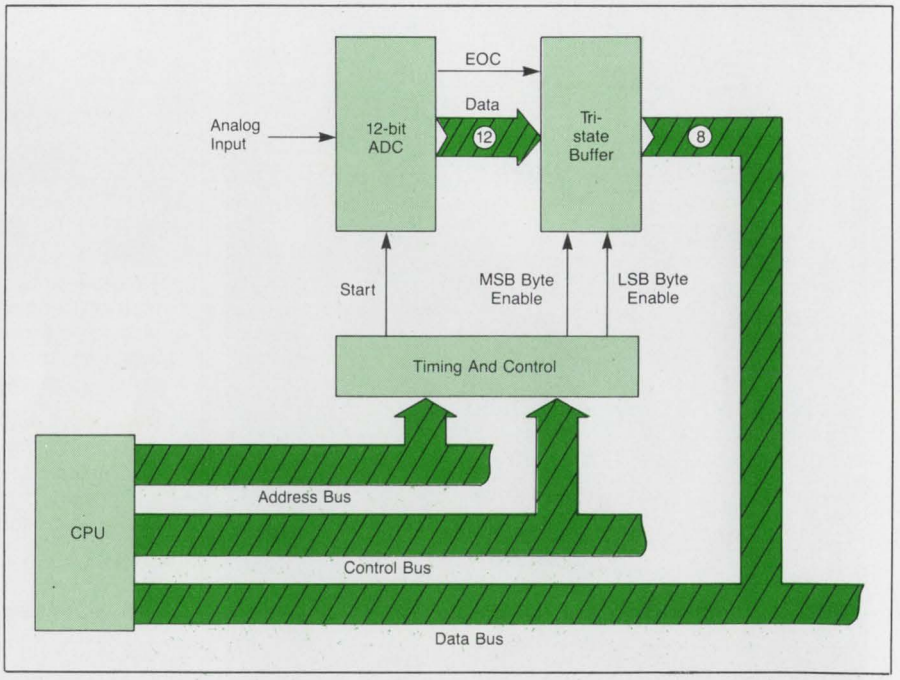


Figure 1: ADC memory mapped interface to a μP; a tri-state buffer and timing control circuits complete the interface.

David C. Pinkowitz is a Product Manager with the ILC Data Device Corp., 105 Wilbur Place, NY, NY 11716.

Control	Address (Hex)	Data*								Comment
		D7	D6	D5	D4	D3	D2	D1	D0	
Write	FFF2	X	X	X	X	X	X	X	X	Starts ADC
Read	FFF1	EOC	X	X	X	MSB	B2	B3	B4	Enables MSB Byte
Read	FFF0	B5	B6	B7	B8	B9	B10	B11	LSB	Enables LSB Byte

* Data is shown right justified

Figure 2: μP address, control and data states; program instructions to three ADC addresses start the conversion and generate output data enable signals.

ware and increased processing speed. Processing of memory mapped ADC data is also more flexible, since most program instruction sets contain numerous memory processing instructions.

Figure 1 is a functional block diagram of a 12-bit ADC which is interfaced to a μP as memory mapped I/O. The 12-bits of ADC output data are connected to the 8-bit Data Bus by means of a tri-state buffer. Since the ADC appears to the μP as RAM, data is output to the Data Bus by a Read instruction. Two successive Read instructions accomplish the 12-bit transfer of an MSB data byte and an LSB data byte. Each data byte is assigned an address, as if it were a memory location. The two addresses, along with appropriate Control Bus signals, are input to the Timing and Control circuits when the ADC Read operations are performed. The Timing and Control circuits generate the MSB Byte Enable and the LSB Byte Enable signals, which activate the tri-state buffer. In a similar fashion, the ADC Start signal is assigned an address and is activated by a memory Write instruction. The ADC Start signal is generated by the Timing and Control circuits in response to the address and control inputs produced by the Write instruction.

Figure 2 illustrates a typical assignment of Control, Address and Data states for a 12-bit ADC treated as memory mapped I/O. Three addresses are assigned to the ADC. It is assumed that all 65,536 addresses available on the 16-bit Address Bus are being used. For simplicity, 3 of the 16 highest addresses are assigned to the ADC. Address FFF2 (hex) corresponds to the Start signal. Addresses FFF1 and FFF0 correspond to the MSB data byte and LSB data byte respectively. When the Control Bus carries the Write signal and the Address Bus carries FFF2, the ADC Start signal is generated. During the ADC Write operation, a Don't Care condition exists on the Data Bus, since the ADC does not respond to input data.

When the Control Bus carries the Read signal and the Address Bus carries FFF1, the ADC MSB Byte Enable signal is generated. This causes the MSB data byte to appear on the Data Bus. Data is shown with right justification. The End of Conversion (EOC) signal appears on Data Bus line D7, and 4 MSB data bits appear on Data Bus lines D3 through D0. When the Control Bus carries the Read signal and the Address Bus carries FFF0, the ADC LSB Byte Enable signal is generated. This causes the LSB data byte to appear on the Data Bus. The 8 LSB data bits appear on Data Bus lines D7 through D0.

Address Decoding

The circuits required to generate the ADC Start signal and Byte Enable signals, in accordance with the Control and Address states discussed above, are quite straight forward. **Figure 3** shows the required ADC Address and Control interface circuits. The Start signal

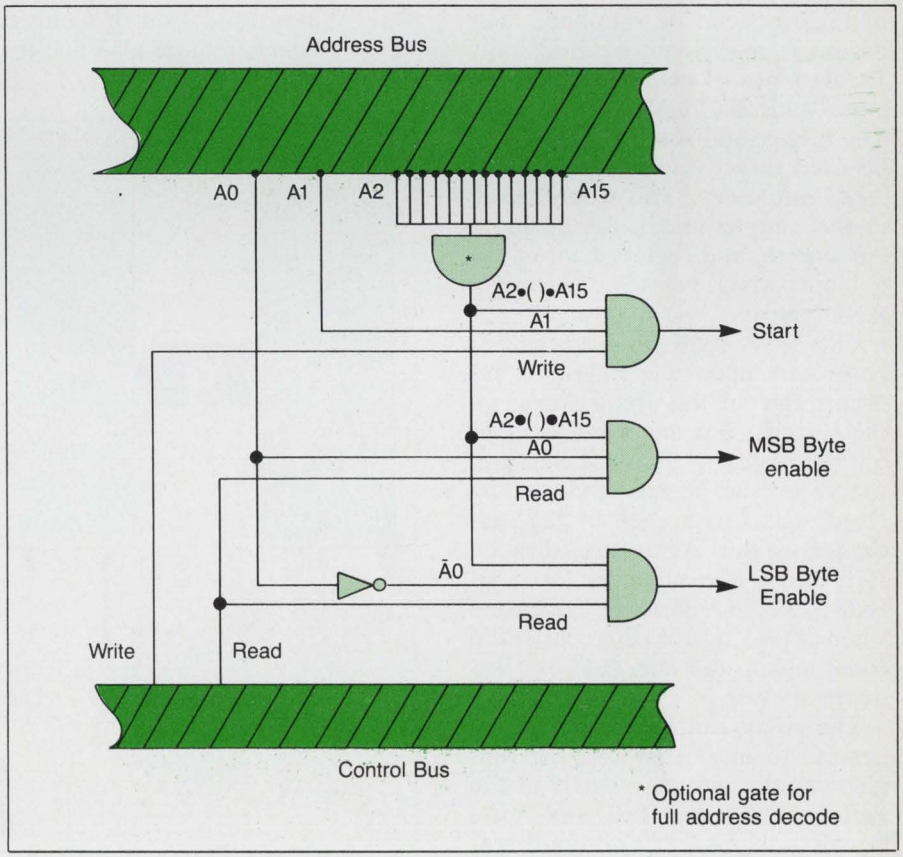


Figure 3: ADC address and control bus interface; gating of address and control lines produces start, MSB Byte enable and LSB Byte enable signals.

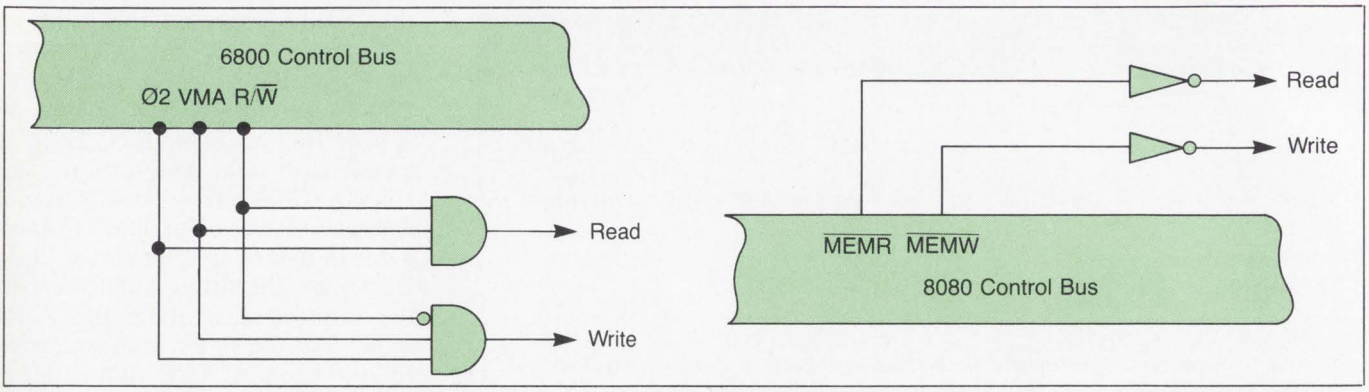


Figure 4: Read and Write control circuits; different control signals for the 6800 and 8080 μPs require different gating circuits.

is generated upon the simultaneous occurrence of the Write signal on the Control Bus and address FFF2 (hex) on the Address Bus. This corresponds to the logical AND of the Write signal with each of the Address Bus lines A1 through A15.

It must be noted that the addresses selected for the ADC were based upon the assumption that all 65,536 memory locations were being used. In smaller systems, requiring far less memory, the circuit of Figure 3 can be simplified. For example, a system requiring only 16,384 bytes of memory would not need address lines A14 or A15. These two Address Bus lines could be used directly to generate the 3 ADC addresses. This would result in the elimination of the 14 input AND gate, and replacement of the 3 input AND gates with 2 input AND gates.

The MSB Byte Enable signal is generated upon the simultaneous occurrence of the Read signal on the Control Bus and address FFF1 on the Address Bus. This corresponds to the logical AND of the Read signal with each of the Address Bus lines A0 and A2 through A15. In a like manner, the LSB Byte Enable signal is generated when the Control Bus carries a Read signal and the Address Bus carries FFF0.

The circuits of **Figure 3** apply in general to most μPs. All μPs implement the address signals in the same way, but the Read and Write signals are usually different for each. **Figure 4** illustrates circuits which can be used to generate Read and Write signals from Control Bus signals available on the 6800 and 8080 μPs. The 8080 provides individual Complemented Memory Read and Complemented Memory Write signals. The 6800, on the other hand, provides a single Read/Complemented Write signal. The 6800 also requires the use of control signals Phase 2 clock and Valid Memory Address.

Tri-State Buffer

As mentioned above, the ADC Data Output and End of Convert (EOC) signals require a 13 line tri-state buffer interface to the 8-bit μP Data Bus. **Figure 5** shows the ADC interface to the Data Bus. The interconnection of the 13 tri-state buffer output lines to the 8 Data Bus lines is shown for right justification of data, as illustrated in **Figure 2**. This configuration makes the data appear to the μP as an integer between 0 and 4096. An alternative configuration, left justification, would consist of 8 MSB bits in the MSB byte and 4 LSB bits on lines D7 through D4 in the LSB byte. This configuration makes the data appear to the μP as

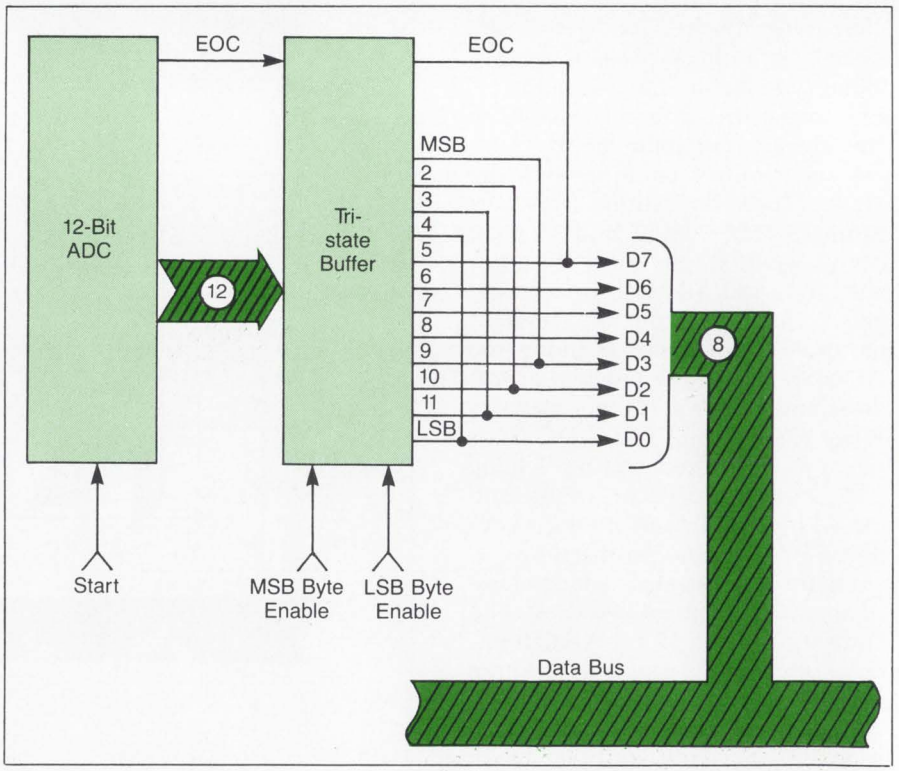


Figure 5: ADC Data Bus interface; a tri-state buffer with separate MSB and LSB enable signals allows transfers of 12 data bits to the 8-bit Bus.

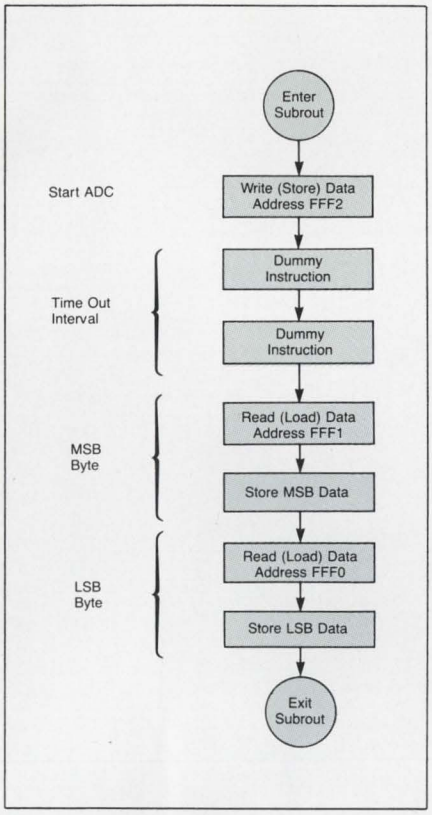


Figure 6: Software flow chart for timed out A/D conversion; dummy program instructions are used to generate a time out interval to ensure valid ADC output data.

a fraction, N divided by 4096.

Transfer of the EOC signal onto the Data Bus is optional. The EOC signal is required to validate the ADC output data, if the μP software subroutine makes use of status polling of the ADC. An alternative software subroutine, where the ADC is Timed Out, does not require the EOC signal. This is because adequate time is allowed for completion of the A/D conversion before the Read instructions are generated.

Simple Software

The circuits and signals required to interface a 12-bit ADC with an 8-bit μP have been discussed. μP program instructions, or software, is used to generate the correct signals, in the proper sequence, at the correct time intervals. Specifically, the program instructions must generate a Write command and the address FFF2 to start the A/D conversion process. When the A/D conversion has been completed the program instructions must generate two successive Read and Store commands corresponding to addresses FFF1 and FFF0. It is critical that the A/D conversion be completed prior to the storage of the data.

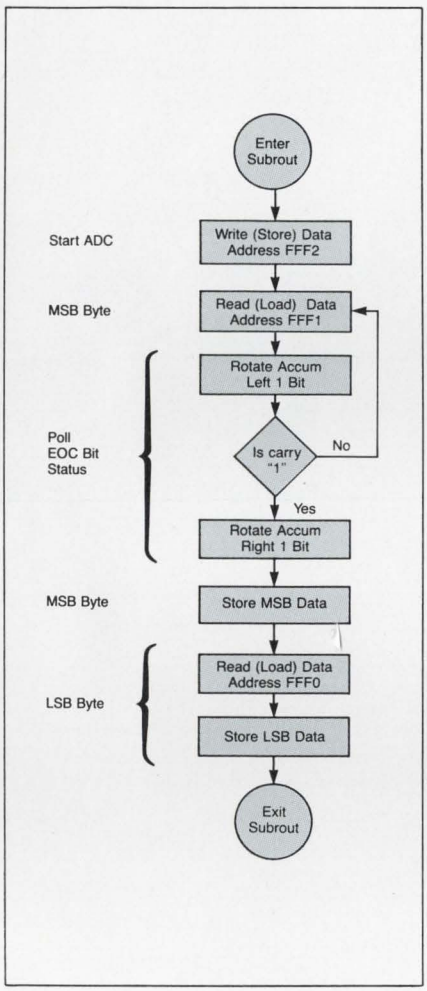


Figure 7: Software flow chart for status polling A/D conversion; a test loop which polls the status of the EOC bit is used to ensure valid ADC output data.

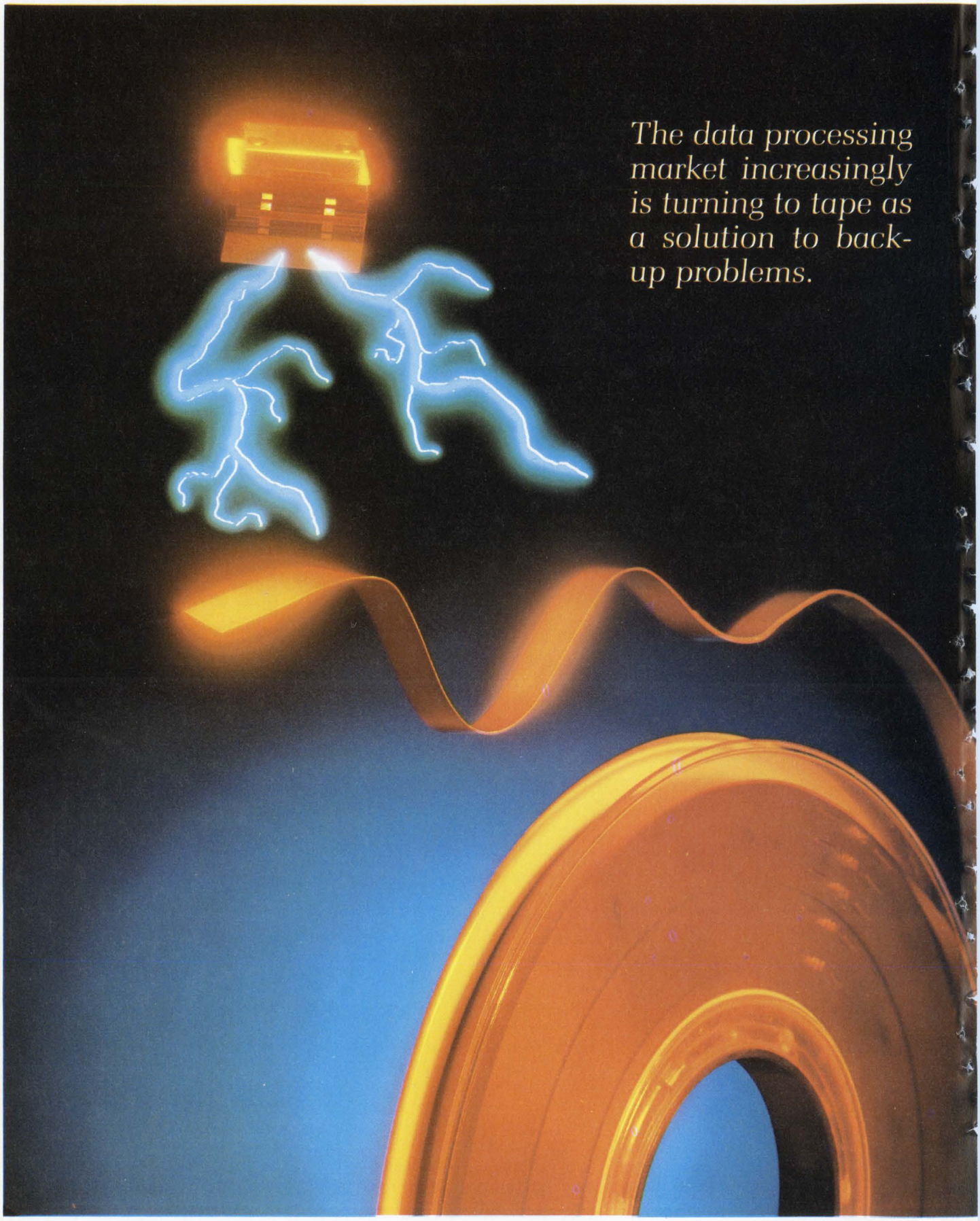
Two software routines, Timed Out A/D conversion and Status Polling, are commonly used to ensure that A/D output data is valid. **Figure 6** is a software flow chart for Timed Out A/D conversion. Following the A/D conversion Start by a Write instruction at address FFF2, dummy instructions which consume a known amount of time are performed. As an example, if a time out interval of 10 μs is required, dummy instructions which required 10 cycles of a 1MHz clock would be used. After the dummy instructions have ensured completion of the A/D conversion, Read and Store commands at addresses FFF1 and FFF0 complete the ADC subroutine.

Figure 7 is a software flow chart for Status Polling A/D conversion. Following the Write command at address FFF2, which starts the A/D conversion, the μP enters a test loop which polls the status of the End of Conversion (EOC) bit. The MSB data byte, which contains EOC in D7, is Read at address FFF1. When the accumulator is rotated left by 1 bit, the EOC bit becomes a carry bit. If the EOC carry is not a "1", the subroutine test loop is repeated. When the A/D conversion has been completed, and the EOC carry bit is a "1", the accumulator is rotated right by 1 bit. This retains the MSB data byte to its original position so that it can be stored. Read and Store commands at address FFF0 complete the subroutine.

Simple Interfacing

The key to simplifying the interface of a 12-bit ADC to an 8-bit μP Bus is to recognize the I/O category that is most appropriate for the ADC. For ADCs with conversion times faster than 1 μs, Direct Memory Access (DMA) is the correct category. ADCs slower than 100 μs should be treated as peripheral I/O. ADCs with conversion times between 2 μs and 100 μs should be interfaced as memory mapped I/O.

Conveniently, the most commonly used A/D converters are also the simplest to interface. All that is required to interface a medium speed ADC as memory mapped I/O is a tri-state buffer, a few logic gates, and some simple software. My company has successfully interfaced a 5 μs ADC (DDC-5240), a 10 μs ADC (DDC ADC87), and a 50 μs ADC (DDC-5200) using the same circuitry and software. Therefore, once the circuitry has been fixed, higher speed performance improvement can be accomplished with a minor software change. □



The data processing market increasingly is turning to tape as a solution to back-up problems.

New Technology Promises A Bright Tape Future

by P.J. Badum and S.D. Cheatham

Today's data processing requirements are driving data storage subsystem manufacturers to employ new technologies. Disk technology has moved to non-removable storage, allowing for much higher track densities, better reliability, and expanded DP applications. The tremendous amounts of data assembled and processed require a very reliable backup device to retain data integrity in the event of a hardware, software or human failure.

The DP market has turned to tape as the cost-effective solution. Manufacturers of tape drive subsystems are employing higher technologies and offering greater capabilities to meet the challenge.

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Today's Tape Standard

Data processing applications on ½" magnetic tape today are performed in one of three industry-standard formats: non-return to zero on ones (NRZI), phase encoding (PE) or group-coded recording (GCR).

NRZI recording writes 800 bits of information per inch (bpi) of tape on either 7 or 9 tracks. NRZI relies on a magnetic flux change in the oxide coating of the tape to indicate a "1" bit of information. The absence of a flux change signifies a "0". The format provides 100% recording efficiency because NRZI requires a maximum of one flux change for one bit of information. The format cannot correct errors and, unfortunately, mechanical skew considerations limit NRZI density to the 800 bpi range.

PE, using a self-clocking approach, was developed to overcome the limitations of NRZI. Like NRZI, PE records nine tracks on the tape. However, it records the "1" and "0" bits via a flux

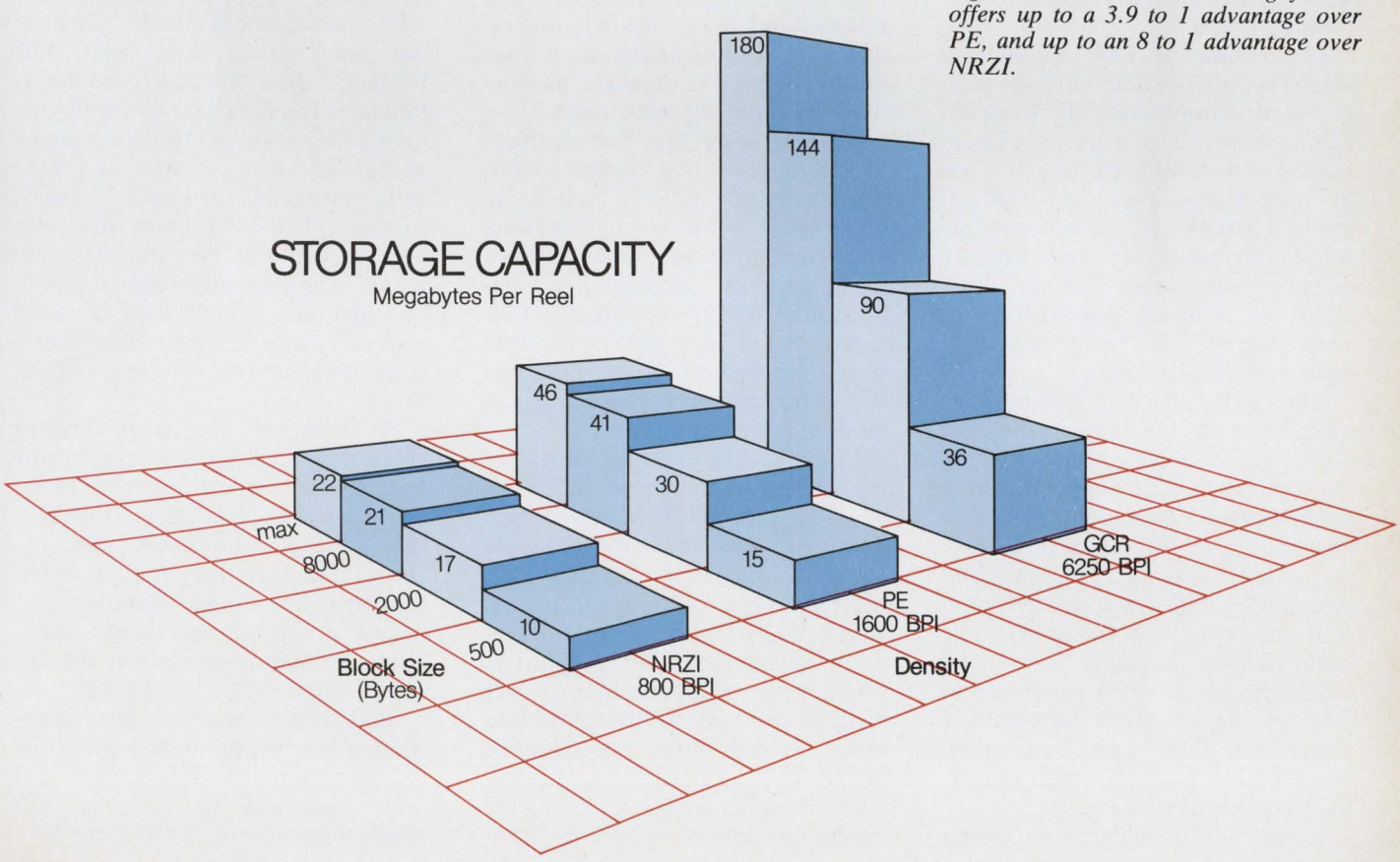

Figure 1: The GCR recording format offers up to a 3.9 to 1 advantage over PE, and up to an 8 to 1 advantage over NRZI.

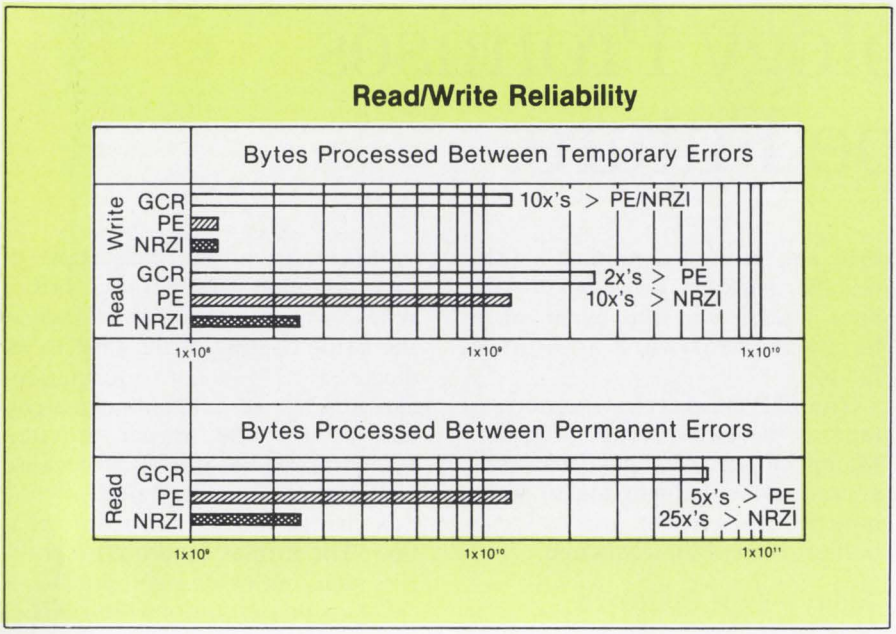

Figure 2: A substantial improvement in read/write reliability and a substantial savings in system overhead are provided by GCR. Time that otherwise would be spent in retries and error recovery procedure can be used for computing.

change. The difference between the two bits depends on the direction of flux change. PE has the drawback of requiring as many as two flux changes per bit of information. PE has a recording efficiency of 50%.

PE records at 1600 bpi density since the independent clock of each of the nine tracks virtually frees PE from skewing problems experienced with NRZI. PE can be used at higher densities, but the increased frequency of flux changes begins to cause an unacceptable signal-to-noise ratio. Further, dual-track error correction, not provided for by PE, becomes important at higher densities.

The GCR recording format takes advantage of NRZI's efficiency while incorporating the clocking procedures of PE. Supported by a sophisticated approach to error correction, GCR writes in a 9042 flux-changes-per-inch (fcpi) density and has a dual-track error detection and correction capability. The data density realized is actually 6250 bpi, which when processed at 200 ips, equals 1.25 Mbytes per second—a data rate compatible with many of today's high-performance computer channels.

GCR, with its higher areal density and interblock gaps of just 0.3", offers up to a 3.9 to 1 advantage over PE, and up to an 8 to 1 advantage over NRZI (**Figure 1**). Because GCR packs so much more data onto a single reel, fewer tape mounts and fewer rewinds are required. Operator intervention is reduced, helping to increase productivity by reducing labor costs.

Incorporating the best features of NRZI (low flux-change to bit-density ratio) and PE (self-clocking), GCR provides a substantial improvement in read/write reliability (**Figure 2**). Substantial savings in system overhead also are provided by GCR, since time that would otherwise be spent in retries and error recovery procedure can be used for computing.

If it were not for the existence of tape libraries recorded in NRZI and PE, the choice of which tape density to use would be a simple matter.

High-usage tape applications, where GCR has become the standard, include the energy industry, where geological seismic recording is done for oil well exploration; space exploration for photographic image and data recovery; government record keeping; and the transaction-intense airline reservation services. The amount of data they record is in the Gbyte and Tbyte range.

On the low-use end, PE ½" magnetic tape drives, ¼" cassette tapes and even floppy disks back up subsystems. Once a file reaches 50 Mbytes to 100 Mbytes in size, these products suffer from performance and capacity constraints.

Streaming Or Start/Stop?

The streaming tape drive is becoming popular as an optimized disk backup and restore device. While streaming tape drives are very cost-effective for mass data dumps, streaming does have some performance limitations of which design engineers and DP managers should be aware. Streaming begins to create problems when a write-temporary-error correction is encountered and the subsystem attempts to do a backspace, erase gap and rewrite of the record. A significant amount of throughput is lost on write operations whenever a tape error occurs.

Another disadvantage is that streaming keeps the channel to the CPU tied up, effectively blocking out other drives—and other DP business. Data flow has to be maintained at the data rate of the device or it will go out of streaming mode and go into a stop/start cycle, typically taking several hundred msecs to stop, then back-space the tape and reposition it for the next command. The time involved is orders of magnitude greater than the time required with a traditional start/stop mechanically buffered tape drive.

A string of start/stop devices (**Figure 3**) facilitates single record access. One record can be read, the drive stopped, other drives in turn addressed to access other records, and then the original drive re-addressed almost instantly, as during a sort or sort/merge operation. Streaming drives are not designed for these types of jobs.

Start/stop tape drives are somewhat more flexible in their operating characteristics, and can be used in a wider variety of customer job applications than streaming-only

drives. Seventy to 75% of all named data sets are sequential, and sequential access comprises 60 to 70% of the total data processed in a typical day. Sequential processing jobs involve short gaps between the required records during which the drive must stop and then quickly be started again to read the next record, providing data to the CPU in a relatively short time. This cannot be accomplished with a streaming device without sacrificing performance. However, the streaming concept can be modified, making it a start/stop device and retaining all the advantages of the streaming environment, thus being a much more flexible device that the customer can use to do many more types of jobs efficiently—not just back up disk drives.

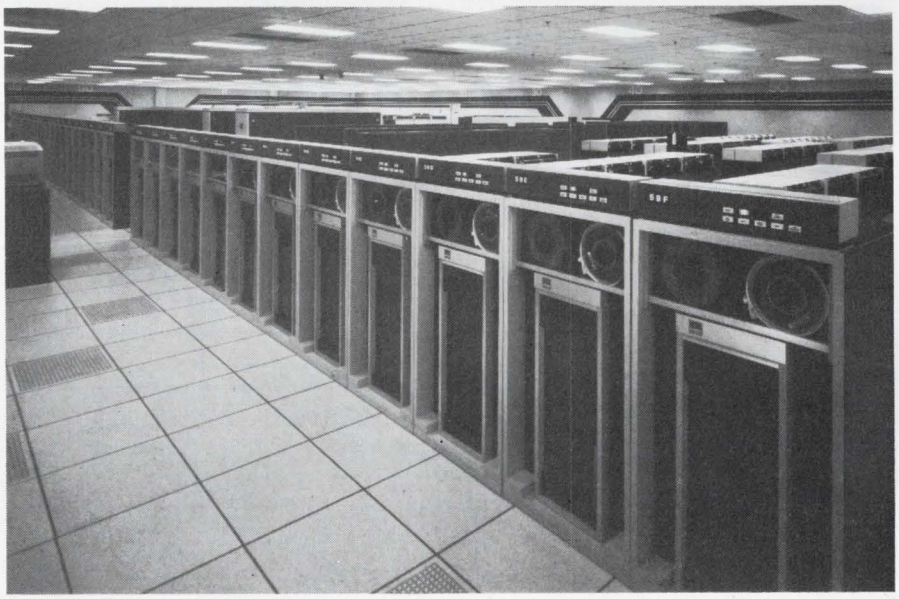

Figure 3: Single record access is facilitated with a string of start/stop devices. Streaming drives are not designed for these types of jobs.

New Technology

Magnetic tape technology is far from dead. The thrust of new technology in the areas of media, new formats, read/write heads and the incorporation of large-scale integration (LSI) will have a significant impact on future magnetic tape products. Greater storage capacities, higher performance via higher data rates and buffered data transfers, smaller packages, improved reliability and reduced costs due to fewer components are some of the likely benefits that are extending tape's product life.

The advancements in magnetic tape technology and their benefits to the customer are becoming a key part of the next generation of tape products. Applying new technologies today to the existing PE and GCR drives already is resulting in better selection, price/performance and reliability for the customer.

Media is one example. Working with the physical imperfections of the tape substrate material to double the density of bits stored is no trivial task. Disk engineers have achieved most of their density increases by pressing technology—flying read/write heads closer to the surface of the disk and making the oxide coatings thinner. The entire head-disk-assembly is sealed against contamination from airborne dust and other potentially damaging particles. With tape, there is a limited amount of control that can be applied to the environment. Tape, whether mounted on a drive or stored in a library, is exposed to the atmosphere, where contamination is a problem.

Gamma-iron oxide is the most common oxide coating used on ½" magnetic tape today. With GCR, the medium is recorded at just over 9000 fcpi. Correction algorithms, in the drive's microcode, constitute overhead and result in the difference between 6250 bpi and 9000 fcpi.

Coatings presently used on ½" tape are approximately 300 μin thick. Coatings in the 100 μin range are needed to achieve the higher recording densities that are planned for the future.

Further, as tape becomes thinner and thinner, any roughness in the substrate has an increasing effect upon the thickness of the coating and how the tape conforms to the tape head. Tape is essentially a contact-recording medium. It should ride virtually in-contact with the tape head. Occasionally, a separation of up to 10 μin can occur due to substrate inconsistencies and must be allowed for in the tape head's electronics.

Standard data processing iron oxide tape, without modification, will support linear densities of approximately 10,000 fcpi. It is considered impractical in the industry today to try to take the present medium to an operating density higher than GCR. To go above these densities and achieve equal-to or greater-than today's data integrity and recording reliability, a different type of media must be developed. This can take several forms. It can be a cobalt-modified iron oxide, a chromium dioxide, or some variation thereof. The primary effort for the future presently is towards chromium dioxide.

Normal iron oxide particles typically have a 3 to 1 aspect ratio, at best. Doping of the iron oxide improves the recording density characteristics of the medium. Cobalt is added to the iron, modifying the molecular structure and altering the coercivity and acicularity of the particles. Chromium dioxide, a particulate with an aspect ratio usually greater than 5 to 1, is being looked at as another method to improve the density capability of tape: 80,000 fcpi are possible. However, chromium dioxide is considered to be more abrasive than iron oxide, potentially reducing the life of the recording heads.

The ability of metal read/write heads currently employed to ad-

Figure 4: The STC 1900 series tape drive handles either NRZI, PE or GCR formats at speeds of 50, 75 or 125 ips. Developments in microcode interface technology allow OEMs to adapt easily these tape drives to any processor.

Figure 5: Detachable diagnostic devices, remotely tracing equipment problems, will soon be used routinely by field engineers. Failures in the field can be solved in this fashion 95% of the time.

dress increased flux densities fades past the 12,000 fcpi range. Their density limits are subject to signal-to-noise, fabrication and frequency limitations. Using new magneto-resistive techniques for detecting the signals will be more reliable than attempting to stretch present inductive techniques into a new generation of products.

When the high densities of which new tape will be capable are reached, the signal levels will be significantly lower. Because the magneto-resistive technique senses flux, it is not velocity sensitive. This characteristic can be helpful to the system designer. The magneto-resistive technique, also able to detect lower signals with less noise, is necessary to achieve maximum data read/write performance.

A major effort in developing a new recording system is defining the media defect sizes, identifying the type of error-correction code necessary, and how many tracks can be corrected. The data integrity of GCR is an order of magnitude better on a per-bit basis than PE, because of the kind of error correction and overhead that has been put into the system. Another order of magnitude improvement in reliability is expected when the jump from 6250 to 32,000 bpi is made.

Metal heads have reached their limits from a technology standpoint. A technology that can be batch-fabricated while offering a quantum leap in recording capability is needed. Batch fabrication, using evaporation techniques similar to LSI circuit techniques, currently is being studied. Chances for another magnitude increase in data reliability in the future are very good for the next generation of machines.

New thin-film recording heads will allow a six-times areal density increase, achieved by a two to three times increase in track densities, and a doubling of effective linear densities, resulting in storage capacities of some 780 Mbytes on a 2400″ reel of ½″ tape.

A high level of integration using CMOS and bipolar analog IC technologies will significantly reduce unit size, cost and maintenance while increasing reliability. Tape products under development will use 25% of the card space used by current products; future products will replace whole cards with bipolar or CMOS ICs.

Industry (ANSI) standards call for accurate control of velocity variations in written data. This degree of required control is difficult to achieve. μP capstan control systems are one solution compensating for changes of acceleration and velocity, as well as resonance effects that occur within the tape itself during the time the drive is operating in a start/stop mode. These tape-induced velocity variations are nearly impossible to control without an intelligent capstan control system.

Reducing User Costs

The power that a drive draws is a function of the basic velocity of the device, i.e., whether it is a 75 ips or a 200 ips device, the length of

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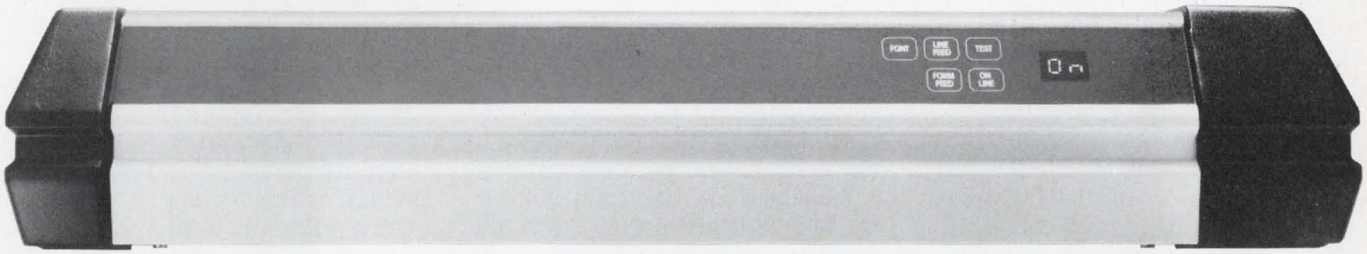

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the vacuum columns or buffer devices, the mass of the tape and reels, and the degree of start/stop decoupling.

The basic speed of the device is largely a steady-state power consumption consideration. The length of the vacuum column affects transient conditions. The longer the column, the longer time the reel has to achieve a velocity that is commensurate with the speed of the tape moving over the read/write head. The shorter the column, the less time and, therefore, the more power that is required.

The present big tape units use long vacuum columns. Consequently, the unit itself must be physically large, to accommodate buffering requirements at 200 ips, start/stop, with a specified amount of power. These are areas that must be addressed by the drive designer when considering the cost/performance characteristics of the unit.

Ownership costs of high-performance tape drives are more than merely the operating costs. Maintenance on these units can be relatively high, and this is another significant area that is being addressed by manufacturers.

Field engineers soon will be using detachable diagnostic devices **(Figure 5)** to trace equipment problems. Subsystems will be attached via RS-232C interface, either locally or to a modem, which gives a direct communications link via telephone to the company's centralized service area. Failures in the field will be rapidly diagnosed at headquarters; the local field office will be instructed as to how the problem must be corrected and what parts or microcode need replacement. Problems can be solved in this fashion 95% of the time.

Sensors are being incorporated into products which will sense when a particular mechanical operation is not functioning properly. This allows for quick identification and replacement of mechanical parts that have failed.

Ultimately, companies will run maintenance diagnostics at the customer level with much of the diagnosis done via programs resident on a floppy disk at the processor or in the subsystem. The user can assess which components (units) have to be replaced and repair the equipment with spare parts stocked at his location.

In the final analysis, today's customers are requiring in tape devices a higher level of technology that supports better performance, better reliability and a variety of DP applications while giving greater storage capacity within smaller packaging sizes, less power consumption and faster and easier maintenance. In response, design and system engineers are rapidly adapting and developing both tape drives and the tape media itself, to meet these very real needs. □

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Comdex 82: Selling in Springtime

Dedicated to business, marketing and financial issues, this year's show will also introduce the latest wares from computer vendors.

by Nick Mokhoff
East Coast Technical Editor

Comdex 82, to be held this year June 28–30 in Atlantic City, NJ, will present more than 450 exhibiting companies and will attract more than 8,000 independent sales organizations (ISOs). Primarily designed for dealers, distributors, turnkey vendors and computer retailers, the show and conference will highlight the latest equipment from computer vendors and discuss marketing and sales techniques with respect to third party sellers.

The show is sponsored by the Interface Group (Framingham, MA) which stages the two Interface conferences and the other national Comdex and Comdex/Europe shows as well as the Federal DP Expo. As Janet Taylor, senior conference coordinator, explains: "Comdex/Spring is a national show just as the Comdex show that is usually held in Las Vegas each fall. Both shows serve as a staging for the introduction of numerous new computer products while the sessions are geared to keeping the ISO up-to-date on hardware, software, marketing and sales strategies."

Kenneth G. Fisher, former president of Prime Computer, will give the keynote address at the show. Mr. Fisher resigned the presidency six months ago, after spending six years with Prime. During that time, the company increased sales a hundred-fold, from $4 million in 1975 to close to $400 million in 1981. During the past half year Mr. Fisher has been watching the mini- and microcomputer markets and advising prospective entrepreneurs on the direction they should be heading. His address on this subject should be stimulating, and fits in appropriately with the theme of

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the show's program: Skills for survival.

The program is divided into 13 session groups, with each group entailing from three to seven sessions. Most are aimed at marketing and sales techniques for the ISO, although some sessions deal with hardware and software trends in the computer industry.

In session FYF3—Forecasting your future, Jean Yates of Gnostic Concepts (Menlo Park, CA) a market research firm, will introduce three speakers who will look ahead and analyze important trends in the computer marketplace. The markets for personal computers and small business computers will be highlighted for their dramatic expansion and dependence on ISO channels of distribution. The second speaker will discuss Vendor Market Share Data, addressing the ongoing race among vendors of mini/micro computers, peripherals and software and how ISOs can plan strategies for their long-term product plans.

The third speaker will focus on specific trends taking shape in small system software, and will bring the ISO up to date as to where his place in this market should be.

A couple of plenary sessions, PWP-2 and PWP-3, should be of interest to most attendees. The first—Personal information services: Opportunity for the 80's—will address the field of teletext and videotext systems, so far only in testing trials around the world. These one-way and two-way information retrieval systems have an enormous potential for computer vendors and ISOs to sell to both the business and the home markets; so far, however, they have proved too cumbersome to be used by the average consumer. One area that the session speaker will address is the user-friendliness that must be incorporated into these systems before they will be accepted by the mass of consumers.

PWP-3—The ISO Vendor—pits three vendors against three ISOs on one panel that discusses problems faced on both sides of the fence.

Andrew Roman (Roman Associates, Inc) will offer hardware/software solutions, both available and planned, for business graphics systems. In that same session group, titled Profits Producers for Integrators (PPI-1,2,3), speakers will explore disk, tape, terminal and printer peripheral preferences. The areas of local networks and datacomm for small businesses will also be highlighted.

Overall, the Comdex/Spring program is intended to remind attendees of the need for increased sales, marketing and management skills in today's economy and competitive environment, and allow them to browse through close to 425 exhibitors' booths. □

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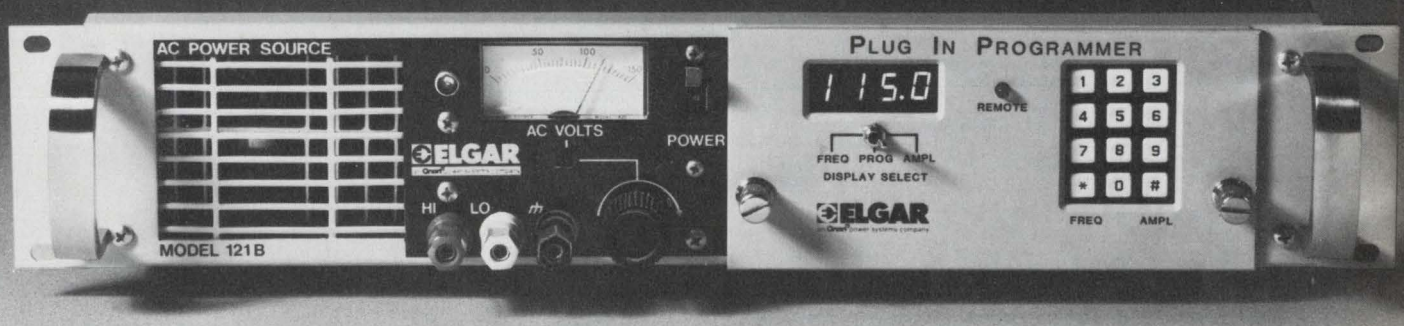

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Designer's Guide To The GPIB/HPIL

by Paul Snigier

The Hewlett-Packard Interface Bus or HPIB was standardized in 1975 into the IEEE - 488 and became the general-purpose interface bus for test and measurement instruments that are used in automatic test equipment (ATE) and for programmable bench instruments and μC-to-peripheral data transfer devices. The bus standard has greatly simplified system design when assembling programmable test and measurement instruments from different manufacturers.

If you are interested in designing test instruments into a benchtop or field environment, consider the GPIB and HPIL to meet your design needs.

Prior to 1975, instruments were manufactured with dedicated interface structures that had unique signal, control and data lines. Data rates, logic levels, and codes also varied. These instruments were often interconnected with cables that had up to 100 wires.

In 1972, when the situation had grown intolerable, an IEEE-488 standards advisory committee met to explore a standard bus. The result, the IEEE-488 Standard - 1975 "Digital Interface for Programmable Instrumentation," was published in April of that year and upgraded slightly in 1978 to clarify textual ambiguities. Minor changes included a 0.4 to 0.5V change for drivers to handle certain new Schottky devices. Others included coded identification I/O markings on instruments to prevent obfuscation.

The HPIB was later adopted by companies other than HP as the General-Purpose Interface Bus (GPIB). The 488 bus standard permits up to 15 devices to operate on the bus, with a maximum 20m distance for interconnecting cables. The standard is divided into mechanical, electrical, functional and operational specifications. These define the type of cable and connectors to be used, the circuits and voltage levels into and between nodes and the interface signals.

Unlike the rigidly defined STD bus, covered in April's *Digital Design* the 488 bus specifications leave some interfaces optional or undefined. As a result, noncompatibility resulting from device-dependent program codes, output data formats and a data coding can lead to problems. If care is taken in reading the product literature the

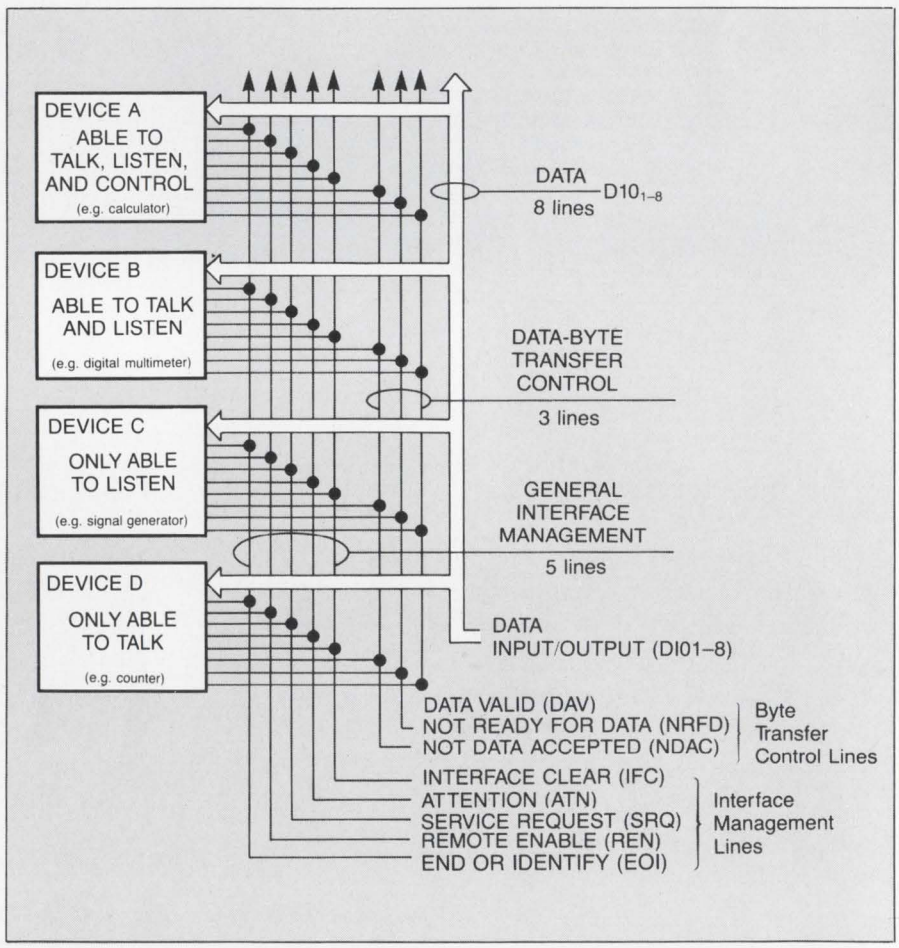


Figure 1: The byte-serial, bit-parallel, negative-logic scheme of TTL-level signals transfer data and commands between instruments or components on 16 lines: (1) data on the DI01–8 lines, (2) handshaking commands on the three data-byte-transfer-control lines, and (3) service requests on the five interface-management lines.

interface problems can be minimized. The standard avoids rigid specification, thus leaving the door open for designers to try new approaches.

After wading through the volumnous 488 document, we must agree with critics who accuse it of being tedious to read. In all features, we do feel that the state diagram notation is more precise and lucid than timing diagrams and does create less ambiguities, compared to other interface standard documentation. Let's now turn to the 488 bus standards in greater detail.

Point-to-point transfer of data over 16 signal lines on the 488 bus is accomplished via devices that are either "talkers" (transmitters), "listeners" (receivers), controllers, or a combination. A talker sends data over the bus, listeners only accept data from the bus, and a controller supervises the others by addressing devices and letting talkers talk. At any time, only one controller or talker can be active. All devices have separate addresses, so each can be uniquely addressed by the controller. Although a controller may address many listeners, data is generally transferred between a speaker and one listener. A printer could be a listener, a waveform generator could be a talker and a digital cassette drive could be both.

All three device types terminate signal lines with 6.2kΩ pulldown and 3kΩ pullup resistors, thereby providing a uniform bus impedance and good noise immunity. Drivers sink 48mA; receivers use Schmitt-type inputs.

The 488 bus byte-serial, bit-parallel, negative-logic scheme has three categories of TTL-level signals. These are eight bidirectional data lines (DIO_{1-8}), three data-byte-transfer-control lines and five general-interfaces-management lines. The eight bidirectional data lines can carry either one byte of either address, data or command.

The three byte-transfer-control lines are "data valid" (DAV), "not ready for data" (NRFD) and "not data accept" (NDAC). When a talker device forces the "data valid" (DAV) line low the device signals to all the listeners that information on the bus is valid and all listeners can read it. A listener that is ready to accept an information byte releases the wired-ored "not ready for data" (NRFD) line, which then floats HIGH. After a listener receives and accepts data bus information, it alerts all other devices on the bus by releasing the wired-ored "not data accept" (NDAC) line. After all listeners release it, the NDAC line goes HIGH and the talker removes its message from the data line. In this way, data transfers proceed along at the pace of the slowest listener, and data is not lost.

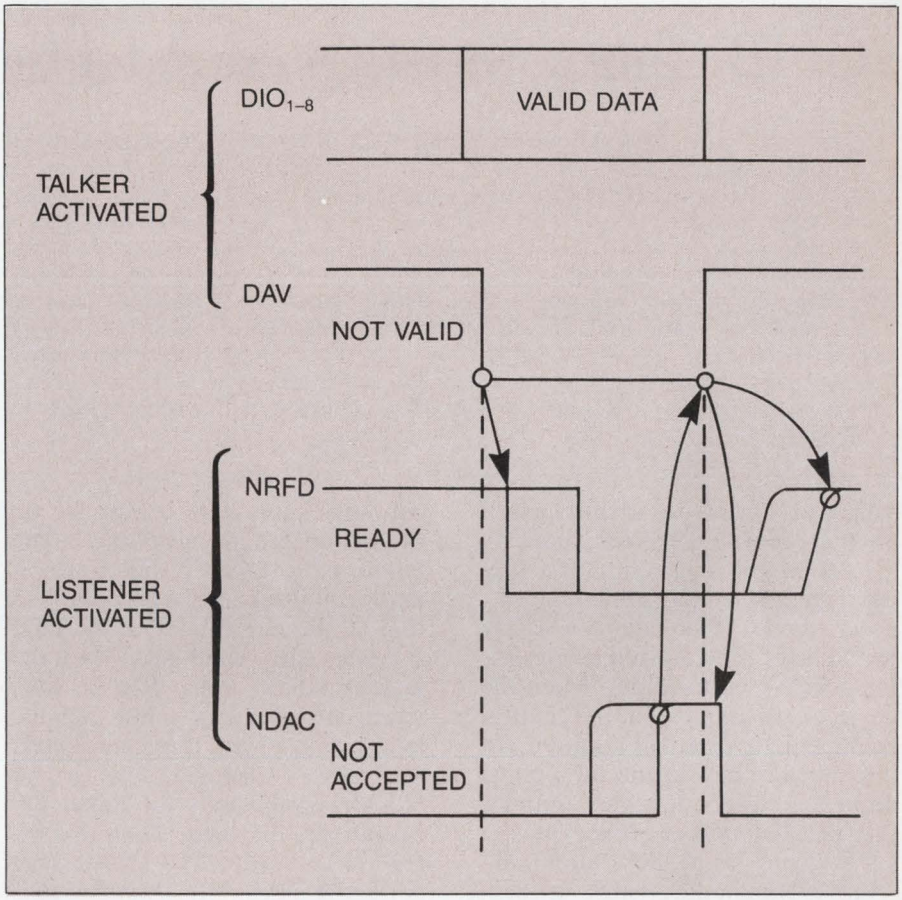


Figure 2: Every byte transfer is accomplished by an asynchronous three-wire handshake on the byte-transfer-control lines. Only when the data valid is sent LOW by the talker will the listeners read the data on DIO1–8. Next, the listener pulls the not-ready-for-data line LOW. The not-data-accepted line is released after the data is accepted, after which the talker removes the data from DIO1–8 (assuming this listener is the slowest one). Once the listener releases NRFD, it floats HIGH, indicating the listener is ready for the next data byte.

The five interface-management lines include: ATN, IFC, SRQ, REN and EOI. The "attention" (ATN) line is pulled LOW by the controller to alert other devices that the data lines hold an interface address on command. "Interface clear" (IFC) resets all interfaces by the contoller to a particular condition. The user can hardwire it as a reset line, to reset for initial conditions 100 ms after power is applied. If a device needs service, it sends the "service request" (SRQ) wire-ORed line LOW. A device can be remotely controlled from front panel controls by the "remote enable" (REN) line. If HIGH, devices go to local control; if LOW, the controller runs them. To signal the listener of the end of a multiple message-transfer sequence on the data I/O lines, the EOI line is pulled LOW (true) by a finishing talker on its last byte. Or, EOI can be pulled LOW by the controller,

GPIB Characteristics At A Glance.

1. Interconnected devices: permits a maximum of 15 devices on any contiguous bus.
2. Interconnection path: Linear or star network with a maximum 20m length.
3. Signal lines: 16 active, total; 8 data lines; and 8 for critical control/status messages.
4. Message transfer: scheme is byte-serial, bit-parallel, asynchronous data transfer via interlocked three-wire handshaking.
5. Maximum data rate: 1 Mbyte/s over limited distances with perfect design; otherwise, 250 to 500 kbytes/s over full path.
6. Addressing: primary addressing permits a maximum of one talker and up to 14 listeners (at a time). Primary addresses—31 talk and 31 listen; secondary (two-byte) addresses—961 listen.
7. Control transfer (shift): if there is more than one controller, only one is active (at a time). The presently-active one passes control to one of the others, and only that controller designated as system controller can assume control.
8. Interface circuits: both driver and receiver circuits are TTL-compatible, with the higher power dissipation and higher speeds of this logic family.

asking a device to identify itself after it sent a "service request" (SRQ) to the controller. To prevent the controller from servicing every device that sends a LOW SRQ signal the controller first asks for device identification. When the device receives this EOI (Identify) command, it places its unique address on the bus during the polling sequence. The controller initiates this parallel poll sequence by the EOI signal with the "attention" (ATN) command, which it activates by sending it LOW. ATN can be asserted only by the controller and only during the addressing or command sequence. The controller can poll up to eight devices.

Data Transfer

Data input/output lines (DOI 1–8) resemble μP I/O ports, and carry 8-bit parallel data to and from the CPU. When PRINT, INPUT, GET and similar operations are used the CPU controls the IOD lines which handle transfer control handshake signals and interface management line signals.

The control line logic levels are negative-true: if the level is under 0.8V, the signal is logic ONE; if it is from 2.0V to 5.0V the signal is a logic ZERO. The 0.8V to 2.0V level is undefined. This is the opposite of many μP systems. More about this later in the section on the CPU electrical characteristics.

Handshaking between talkers, listeners and controllers is functionally accomplished in the following manner. Every byte transfer occurs with an accompanying asynchronous three-wire handshake on the byte-transfer-control lines. The talker pulls DAV LOW (once it knows all listeners are listening), so that all devices know that the DOI 1–8 lines carry valid data. Then the fastest talker pulls NRFD low, which lets everyone know that the talker is busy with that byte. Later, the slowest listener lets go of NDAC, which tells the talker everyone got the data. Then this listener removes its DOI 1–8 message and pulls DAV HIGH, which tells the listeners to pull NDAC LOW. The talker and controller then are ready to be "spoon-fed" more data. The cycle then repeats: the talker asserts DAV as soon as it senses NDAC went LOW and NRFD, HIGH. There, in a nutshell, are the simple 488 bus basics.

Functional Partitioning and Messaging

Devices are divided or partitioned into four functional component areas. GPIB bidirectionally interfaces first through drivers and receivers that exchange data through the message coding section, which in turn, transfers its signals to the device through a collection of interface functions: SH, AH, T/TE, L/LE, SR, RL, PP, DC, DT and C. These "interface functions" regulate the bus control circuitry states. Since these interface functions are mutually independent, only one state is active at a given instant. State diagrams specify this set of functions. Obviously the device functions are not covered by the 488 standard. Device functions include modes of operation, capabilities, types of measurement and the like. The 488 drafters wisely left the device functions unspecified because these functions are unique to each instrument.

Of the ten interface functions, any given device probably will be capable of using only a few, although it could handle all of them. Each function about to be described uses one or more bus lines we previously discussed to perform the operation. The "source handshake" (SH) lets the talker talk. All the handshake interdevice transfer originates with SH. The listener returns the "acceptor handshake" (AH), with the slowest listener setting the return rate. The T/TE is used to send device-dependent data. The talker is active only if addressed by one byte while the extended talker requires a two-byte address. The corresponding "listener or extended listener" (L/LE) interface function receives device-dependent data with either a one-byte (listener) or two-byte (extended listener) address. The service request signal is sent to the controller as a single-bit reply in the status byte during a serial poll.

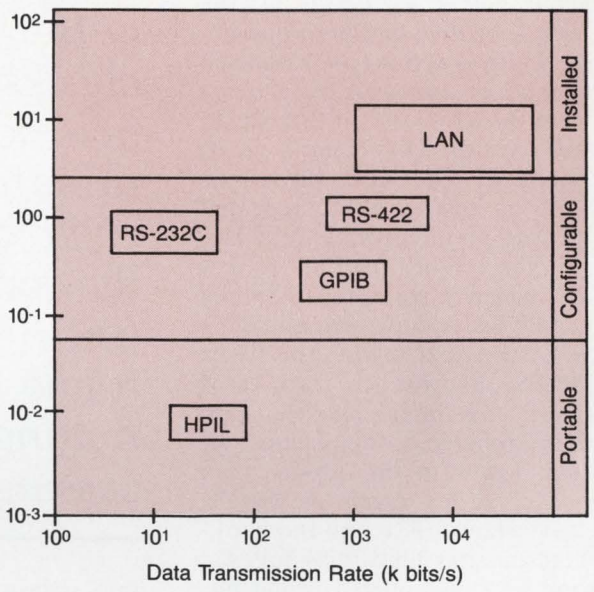
The remaining five are controller-related functions. "Remote local" (RL) enables or disables the manual front panel controls. "Parallel Polling" (PP) permits eight devices to send a status bit over the DIO lines. The "device clear" (DC) sequence clears and initializes devices, so that remote restarting of device operation can be

done with the "device trigger" (DT). Finally, the "controller" (C) function can do several things, such as initiate device addresses and transmit universal and addressed commands. More than one controller can be on the bus, but when one device is transmitting commands or addressing devices, the others must be idle.

Messages are local (between device and interface function logic) or remote (between device and bus). If remote, they can cause a state transition in some interface functions or depend upon device(s) for internal control, with remote messages determined by the designer. When two devices try to transmit simultaneously, the active transfer takes priority over the passive one.

With this background behind us, we can proceed to look at a recent extension to the HPIB or GPIB: the HP Interface Loop (HPIL). Although only introduced a few months ago, HPIL already promises to become a de facto standard. Aside from a few differences, it is identical to the GPIB, and the material we have already covered also applies.

Figure 3: When portability, low cost and battery operation is paramount, but the transmission rate is not, consider the HPIL loop system. GPIB, being byte-wide and TTL compatible, is faster but consumes more power. Though not as easy to assemble as HPIL, GPIB can be assembled to a desired configuration, but with a bit more work. In comparison, local area networks (LAN) are installed, less flexible, consume more power, but are fastest.



Portable Instrumentation

Like the GPIB, the Hewlett-Packard Interface Loop (HPIL) interfaces instruments, controllers, peripherals and the like. Unlike its big brother, however, HPIL is intended for low-power, portable instrumentation.

HPIL is suited to CMOS, battery-powered instruments. HPIL devices transmit data serially in a loop at up to 20 kBytes/sec. HPIL interfaces HP-41, 83 and 85 hand calculators to small cassette drives, microprinter/plotters, small DMM LVDTs and the like built by Hewlett-Packard. HPIL could be hooked up aboard an attack class sub, for example, with an HP-41 running a tape cassette and microprinter/plotter, and be quickly disconnected after the tests. On the other hand, a sophisticated avionics test system will mandate GPIB, as speeds are higher.

HPIL, unlike GPIB, has a remote, power-down control, so the controller can put devices in a standby-state of low power consumption. Unlike GPIB's byte-wide data bus (IOD 1–8), the serial data format helps cut power use. Only one device at a time uses power to transmit to the next device in line. To cut costs, two-wire, differential - drive links cancel out noise and raise SNRs over distances of 100m rather than GPIB's 20m. An added advantage, automatic addressing on HPIL makes programming easier, an area that has caused designers to grumble about the GPIB. Compared to GPIB's linking 15 devices maximum the HPIL can link up to 31 devices, and with extended addressing can address 961 devices, on a low-cost, two-wire cable.

The 82166A convertor provides a general-purpose I/O-to-device interface for interfacing to a noncompatible device. With this converter the engineer can connect several peripherals from different vendors. Under a typical arrangement, an HP-41C could be pre-programmed to take DMM and counter readings, with its commands retransmitted by each device and only acted upon by the addressed device, which also re-transmits the message. In this application the data is transmitted at a slow 5 kbytes/sec through the closed loop and is rechecked for errors by the HP-41C. Typically, the HP-41C could command a thermal printer/plotter to print out data.

With a special interface card (costing above the $125 base price for the HPIL module and calibre), the HP-41 will interface to the HP-83 and HP-85 and 87 desktop computers. Thus the HP-41 can be programmed to collect data in the field or bench and later transfer this data into the HP-85 for analysis and storage. This new data can then be downloaded later into the HP-41 for later use. A more complicated hookup would allow several controllers, with the first taking control upon powerup and others taking over according to the application-specific protocols. Protocols permit a higher-priority-but-idle controller to interrupt another active one.

Code and Interfacing

Since HPIL uses two-wire lines and is asynchronous, a self-clocking three-level code is used. HPIL uses four control bits: 1,0, 1S and 0S—the last two used for reference syn-

chronization at the start of each frame.

The three levels are ±1.5V and 0V. Logic ONE is a positive and negative pulses; a ZERO, just the reverse (negative and zero pulses). Pulse width is about 1μs, with each bit sequence followed by a delay (0V) of 2μs or more. In this way, a spike or transient coming in is overlooked. The sync bit 1S or ONE-S is just a ONE repeated twice with no inter-sequence delay, that is the trailing edge of the first ONE, which is rising to 0V simply becomes the positive-going leading edge of the next ONE. The 0S or ZERO-S, likewise, is two zeros without any inter-sequence gap. This is a reliable coding scheme, although lower in bit density than two-level codes (such as NRZI, Delta Distance, F2F and the like).

Transmission time is as follows: a sync bit takes 6μs; a frame bit, 4μs. A complete frame of 11 bits, one data byte, takes 46μs (10 times 4 plus 6). Ideally, a 21.7 kbytes/sec loop data-transmission rate could be approached; realistically, existing devices are between 3.0 and 5.0 kbytes/sec.

The talker will not send a frame until it gets back and checks the previous one. To avoid transmission delays, each device copies the command frame and passes the frame on, thus permitting parallel processing.

Handshaking and Messages

The talker transmits its message one 11-bit frame at a time. The talker refuses to send the next frame until it gets back the previous one and does an error-correction check on it.

To avoid this unacceptable slowness, each device copies the command frame and passes the frame on, thus permitting parallel processing. After the controller gets back this command frame, it then will not transmit the next command frame until it transmits a "ready for command" (RFC) message and receives it back. The RFC signal is passed along from device to device in the loop—but only after each device has handled the previous command frame.

Updated information is available on the 488 Bus Standard from IEEE at a cost of $10 ($9 for IEEE members), plus $2 for shipping. Write to: IEEE Service Center, 445 Hoes Ln., Piscataway, NJ 08854. □

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¼" Tape Drives — Slowly Getting Better

by Bill Groves

Mature technology is perhaps the best term that characterizes the entire field of magnetic tape recording. It has been around since the late 1940s and improvements have been impressive. Right now, the technology appears to be on a plateau, with good innovations taking a long time to appear. Part of the problem is the amount of tape equipment now in use and the media itself. Both factors tend to limit the need to change and to get better—but things are happening.

Until fairly recently, the computer tape business has only been a minor driving force in the total tape business. Expensive high speed applications received the most attention; applications such as hard disk backup have only existed for a short time. Tape and drive technology for backup can trace its history most directly to the audio recording field, and instrumentation applications of tape have created the greatest demands on tape technology. The background is from these two market drivers: one, demanding highest quality at lowest cost; the other demanding highest reliability combined with the ability to record large amounts of data on the least amount of tape.

The ¼" cartridge tape drives for computer system backup have evolved from these two bases, resulting in high quality/low cost/high capacity data backup.

More Bytes Per Buck

How many Mbytes of storage can you get for today's dollar? According to Stan Miller, 3M's Tape Drive Marketing Manager, "a reasonable cost for a cartridge tape drive should be under $50 per Mbyte of storage for the drive alone." He bases this figure on 3M's model HCD-75 drive system that stores 67 formatted Mbytes on a 600' standard data cartridge. This 16-track streamer is one of the few available today that offers storage capacity twice as great as that of a 2400' reel of ½" tape. 3M's HCD-75 is the highest capacity cartridge drive now available. 3M plans to announce a 60 ips version of the HCD-75 by mid-year. The speed increase will double the data transfer rate but not alter capacity.

Cost of storage is a significant part of any decision, but there are many more trade-offs to consider.

The Forgotten Components

Reliability in a cartridge drive is dependent on mechanical operation. Mechanical considerations begin with the cartridge. The lowest cost element of the system is more critical than it appears. The cartridge controls linear tape tension and provides guidance. If these parameters vary, so does the material being recorded. Saving a few dollars on the cartridge may

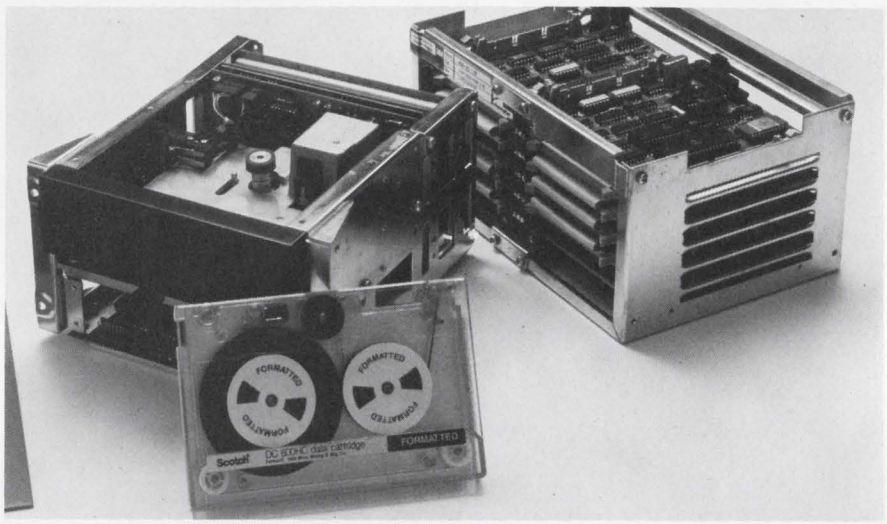

Figure 1: 3M Co. holds the lead in cartridge drives with this 67 Mbyte formatted drive. It can back up most 8" Winchesters without a cartridge change. The overlooked element in tape drive operation is the cartridge. Low-cost cartridges control linear tape tension and guidance for the drive. This 600' cartridge is the largest available from 3M; it uses a smooth base film, a simple tape path, controlled backside friction, and a highly uniform magnetic coating. The formatted cartridge contains end-of-tape and beginning-of-tape information for each of the 1024 bytes of user data blocks on the tape.

As an answer to the Winchester disk backup problem, ¼" cartridge drives may be the cheapest solution available today.

Bill Groves is **Digital Design's** *West Coast Technical Editor. Operating out of the Campbell, CA office, Bill can be reached at (408) 371-9620.*

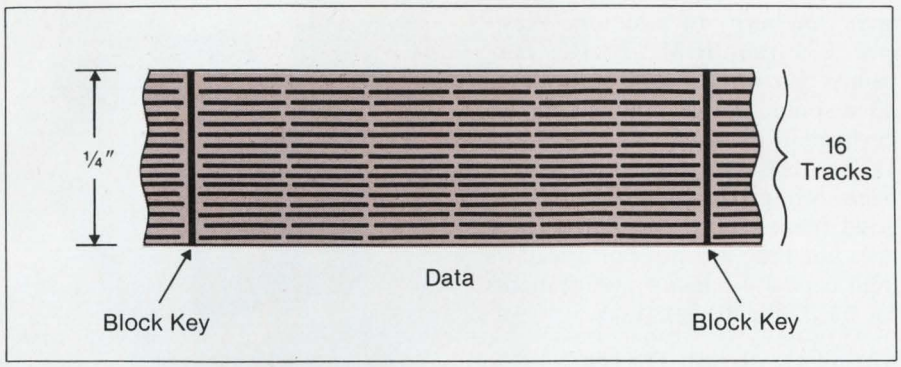

Figure 2: Sixteen tracks on a ¼" tape is the method 3M uses to achieve 67 Mbytes on a 600' cartridge. A single head controlled by a stepper motor is used to locate the tracks; a total of 19 steps are used to move the head from the center of one track to the center of the next. The head also seeks the edge of the tape for precise alignment, and the tape-to-head alignment is maintained by the μP. Data are recorded in blocks of 1024 bytes of user data plus synchronization, header and error correction information. These blocks of data are recorded between the block key data already recorded on the formatted cartridge.

cost many more in lost system performance. OEM designers should evaluate cartridges very carefully and recommend specific brands to reduce user complaints about recording quality.

Tape quality is also very important; uniformity of the oxide and other specifications are not easy to evaluate, but the major tape producers can provide guidance. Dropouts and other tape problems will be around for a long time. Dropouts resulting from flaws in the tape are often impossible to detect when the tape is being manufactured. The best solution to the problem is adding more error detection and correction to the hardware control. High energy tapes are better—new oxides are coming, but error-free tape may be a long way off.

Lubrication of the cartridge is also a critical factor in drive performance. Cartridges are self-lubricating, but that will deteriorate with use and age. High tape speed also degrades lubrication more rapidly because of the increased friction that increases temperatures rapidly. Since the cartridge cannot be oiled and kept in use, suggestions should be considered about the number of uses for a specific cartridge.

Some of the drive manufacturers are beginning to add cooling fans to the drive motors. Most existing drives are convection cooled, so the tape cartridge will heat rapidly. At 90 ips speeds, cooling should be considered for more reliable operation. If control electronics are to be added to a dumb drive, then adding more air flow to keep the cartridge close to cabinet ambient temperature should be considered.

Drive motors are usually cooled by heat sinks or self-driven fans. Most drive manufacturers use

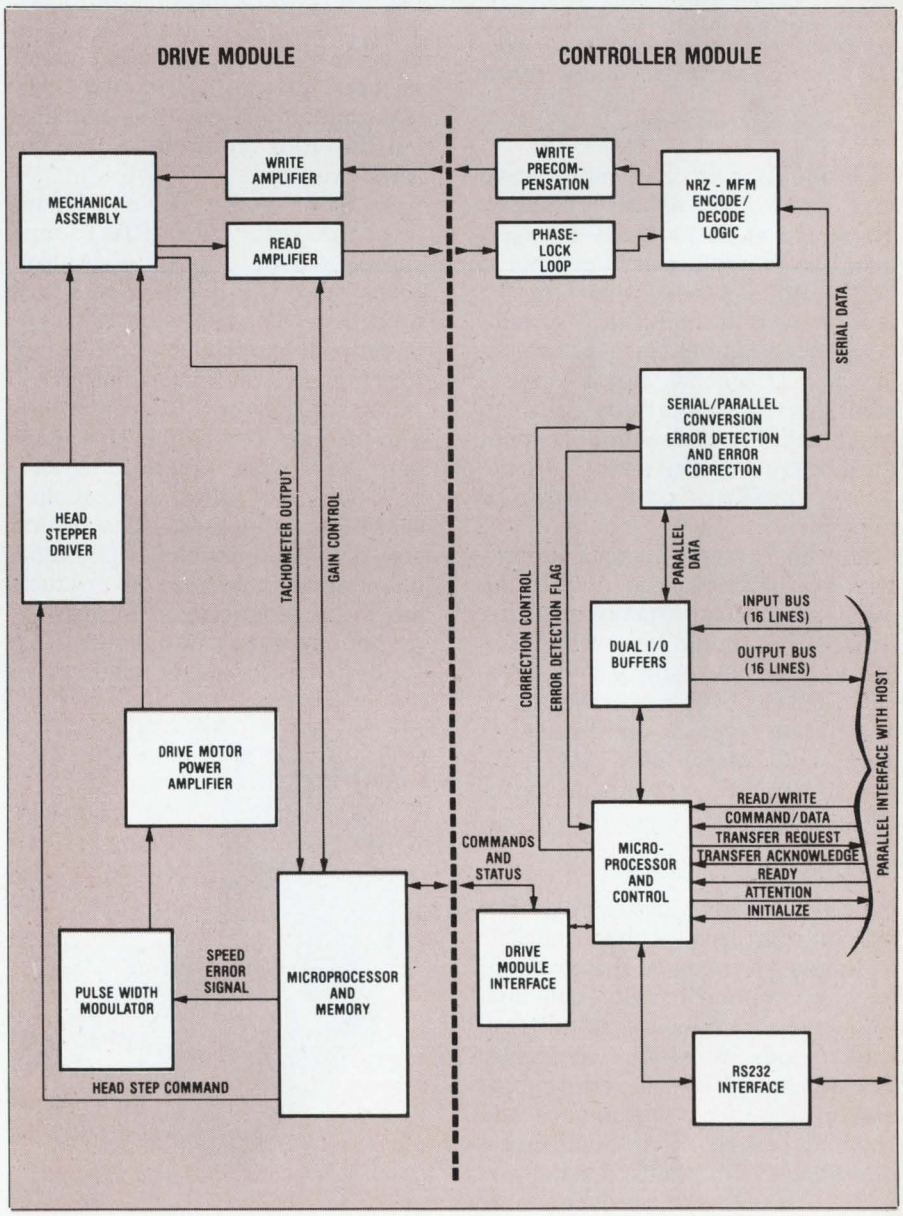

Figure 3: Two 6800 μPs are used in 3M's HCD-75 drive. One is used exclusively to control the basic drive operation, and the other provides the intelligent control for recording and interface operations.

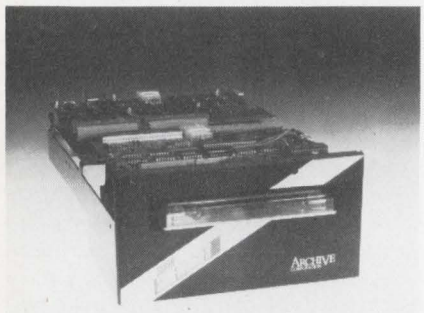

Figure 4: Archive Corporation's Super Sidewinder model provides 45 Mbytes of formatted capacity at a cost of about $20/Mbyte. The Sidewinder model handles 20 Mbytes of formatted data. These drives are capable of backing up Winchester drives in the 15 to 160 Mbyte range.

tried-and-proven drive motors and servo controls to assure reliability. These are areas most drive buyers take for granted, but they should be carefully considered. Once a tape drive is installed in a system, it will need maintenance and cleaning. If it also needs motor replacement, service or warranty costs can go up rapidly. A few dollars spent for a heavy duty drive motor by the drive maker can improve reliability.

Housings, frames, shock mounting, cooling, motors, and all of the other mechanical aspects of a cartridge drive should be evaluated as carefully as the control and interface. Like any electromechanical component, tape drives do fail, so it is usually wiser to buy MTBF on the front end than try to cure problems in the field.

Performance Levels

Neat performance divisions do not exist in the cartridge drive market. A simple grouping of drives based on the number of bits per inch (bpi) they can record is an easy way to look at what is available. The oldest and lowest performance end of the drive business is the 1600 bpi range of products using the 300′ ANSI standard data cartridge. This class of product is now produced by manufacturers such as 3M, Kennedy, Data Electronics, Electronic Processors, Quantex and Tandberg. In addition, Western Electric, IBM, NCR, Tektronix, Burroughs and others produce some captive products in this performance range.

The 1600 bpi range drives have been around longest and have a good track record (no pun intended), but they are not up to today's high capacity backup requirements for hard Winchester disks.

Smart Or Dumb Drives

How many drives will you need? If the answer to this question is "a lot," then you should consider adding your own control electronics. Then, the end product value will increase. Some of the drive manufacturers do produce custom controls and interfaces, like Archive but this adds more cost to the finished product.

A basic dumb drive contains only the read/write (R/W), tape speed, and head position control. If the drive will interface to a host processor, then an 8- or 16-bit bidirectional controller is necessary for command and data transfer.

Smart drives cost more, but usually they are compatible to a standard serial data interface. However, they do offer a complete subsystem approach. The added cost of this approach is significant, but if small quantities of products are to be produced or the drive is to be integrated into an existing system, the plug-in or smart drive may be the most economical answer. Let production volume and the ability to produce a control system influence this part of the decision.

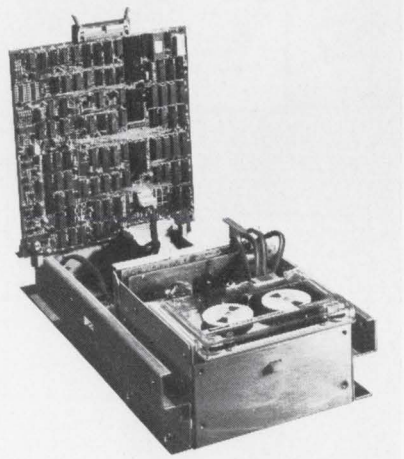

Figure 5: Kennedy Company offers the popular 6450 model in a 23 Mbyte start/stop unit. It is an intelligent unit with a self-contained μP controlled formatter.

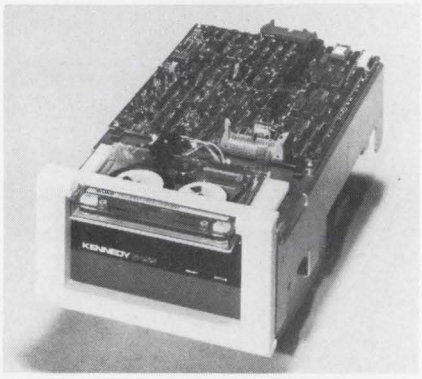

Figure 6: A start/stop drive for archival storage that acts like a streamer is what the Kennedy Company has produced in its model 6455. It stores up to 23 Mbytes and uses a "gap on the fly" technique to add location codes and gaps to a streaming type of drive. The result is easier data retrieval.

Stream vs Start/Stop

With backup drives, a mirror image of the data recorded on a hard disk is also recorded onto a continuous stream of tape. All of the data are preserved in serial form, in case of a catastrophic failure of the main storage media. In most cases, the only use for the backup data is to replace lost data.

A streaming tape packs in the data as tight as possible and without gaps. It is extremely difficult, if not impractical, to attempt to retrieve any specific piece of data from a streamer. However, streaming has one advantage that sets it apart—it is inexpensive. It does not require a great amount of control or precision unless you are trying to record at extremely high density.

Streamers also come in very reliable packages, partly because of their simplicity and partly because they represent the mature segment of the market. The technology also happens to be the fastest growing market for cartridge backup.

Start/stop ¼" cartridge recorders offer the ability to retrieve data easily. Each block of data is recorded with location and other

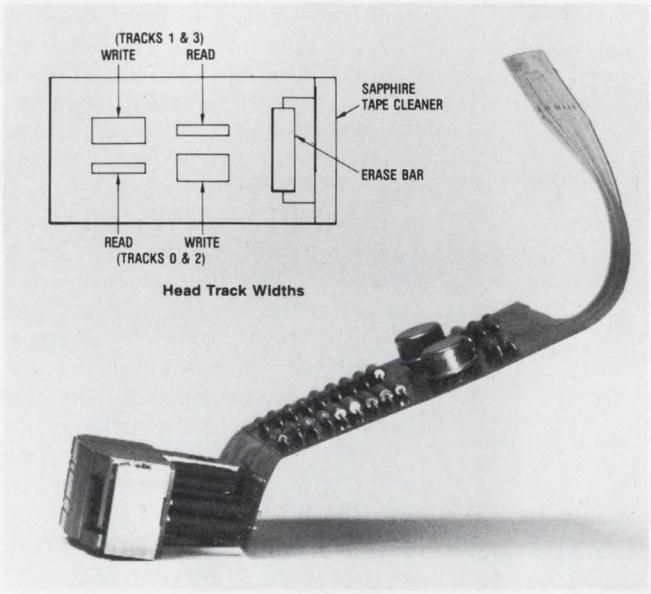

Figure 7: Data Electronics Inc. uses a unique head arrangement in its Streamer and Streaker models to minimize head travel. Only 2 positions are required for track location.

coding to permit easy retrieval. For archival storage where the data must be reused, these drives offer the lowest cost approach. The data recording is serial, but it can be retrieved. The penalty is a higher cost drive, more control circuitry, and less efficient use of tape. Again, start/stop is hard to beat in terms of cost per Mbyte.

Stream or start/stop are very basic decisions. Matching a cartridge drive's capacity to a Winchester is not as easy. The high performance drives can almost match the disk capacity, but some tape change may be needed. If changing from tape to tape or from drive to drive is no problem, then the mid-range performance drives may do the job at low cost. If you are replacing a floppy backup, the tape change will be less frequent than floppies, but if changing tapes is not practical then high capacity is the answer.

High Performance Drives

So far 3M's HCD-75 Data Cartridge Drive, at 67 Mbytes, offers the largest recording capacity. It is about equal to many 8" Winchester disks in capacity and is also able to back up some 14" Winchesters, with tape changes.

The HCD-75 drive system and its cartridge provide 67 Mbytes of user data storage capacity (unformatted tape capacity is 144 Mbytes.) This capacity, coupled with a continuous information transfer rate of 17.5 kbytes/sec, makes the system the ideal backup for fixed disk drives.

Formatting at 4096 1,024 byte blocks per track (16 tracks 65,536 blocks total) allows any block position on the tape to be addressed from a single 16-bit word. Length of spacing between keys gives added protection when overwriting and also increases the margin for interchange between machines in cases where one machine is on the low side of specs and the second machine is on high side of specs. This change is designed to accommodate "worse case" conditions.

The drive utilizes a single track, specially designed ceramic R/W head. A μP controlled servo mechanism positions the head to address one of 16 tracks across the ¼" tape width. Data is written or read in a "serpentine" mode (alternate forward and reverse directions as track assignments change) to eliminate time-wasting rewinds. The servo-controlled stepper motor that controls the single record head will take 19 steps to move from the center of one track to the center of the next. The head also seeks the edge of the tape, not cartridge position, to begin its track search. This μP-controlled head servo provides precise track location independent of cartridge condition or position. It also compensates for changes in tape tension.

Two 6800 series μPs are used for tape drive control, diagnostic self-test (cycled continuously while the system is idle) and sophisticated error-detection and correction during data read functions. μP control of tape transport operations eliminates all manual adjustments.

Physically, the system's tape cartridge is similar to 3M's original DC-300A data cartridge. The DC600HC formatted High Capacity Data Cartridge, however, contains 600' of specially formulated high density tape. The drive is the same size as a standard floppy disk drive (4.62" × 7" × approximately 19" including formatter controller modules).

Higher capacity is also a result of recording information in contiguous pre-recorded data blocks defined by forward/reverse reading block keys; this eliminates the need for "inter-record gaps." Asynchronous 16-bit words are recorded and read in 1,024-byte blocks. The use of pre-recorded block keys permits unlimited, precise recordings. The system's error-detection and recovery capabilities can accommodate substantial signal loss or tape dropouts, according to 3M.

In the "streaming" mode, with continuously running tape, an average rate of 17.5 Kbytes/sec is claimed. A 4 Mbyte/sec transfer rate is the maximum achieved in the "burst" mode, unloading into an integrated buffer storage system.

With its simple I/O structure, the HCD-75 can be interfaced to either a high speed processor-controlled channel or a direct memory access (DMA) channel. One μP-controlled module can direct one to four cartridge transports.

Archive's Supersidewinder model manages to squeeze 9 record tracks onto a ¼" cartridge. Using the ANSI standard 450' cartridge, 45 Mbytes of formatted data are stored on the cartridge. Both Archive and 3M use a tape speed of 90 ips to achieve their high density. They do, however, use different lengths of tape to develop their maximum capacity specifications. These two drives are very competi-

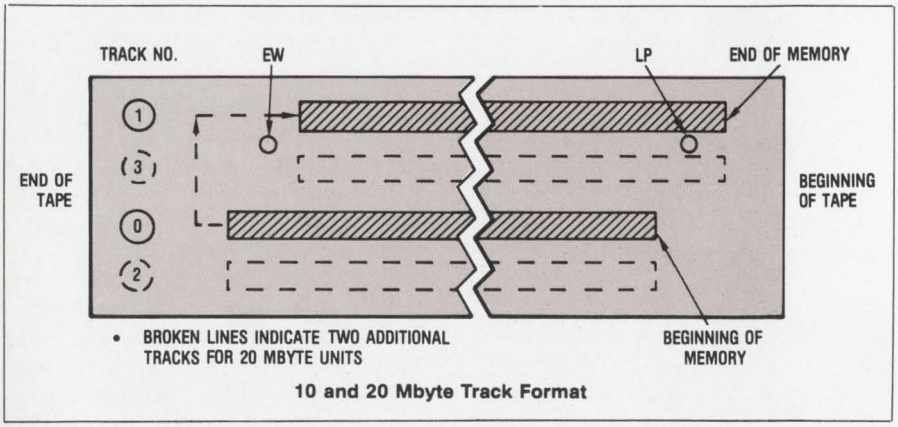

Figure 8: DEI uses a serpentine recording technique to use as much tape as possible without stopping the drive. Without moving the head, the drives can record 10 Mbytes; with head travel, the capacity is doubled.

tive, but 3M wins in number of tracks-length of tape, and total capacity.

The intelligent Supersidewinder's controller based on an 8049 CPU offers functions such as formatting, data interrupt, error and file mark processing, and tape positioning. Automatic read-after-write error detecting, block buffering and read retries are transparent without host intervention. If the host controller cannot meet the Supersidewinder's streaming rate, it will stop, reposition and start again.

In addition to the 3M HCD-75 system and the Archive Supersidewinder, CDC and Tandberg both have offerings in the 40 Mbyte range using 8 tracks.

These high performance cartridge drives do have some problems not found in the lower performance 4-track machines. The greatest problem is finding the center of a track on a ¼" wide piece of tape that contains from 8 to 15 other tracks. 3M has a reliable solution using a single track head and a stepper motor. Cartridge heating can also present some problems at 90 ips; it also increases wear reducing cartridge life.

In The Middle

The largest segment of the ¼" cartridge drive market is the midrange capacity equipment—6400 to 8000 bpi or 10 to 30 Mbytes of record storage.

Kennedy's popular model 6450 start/stop model offers a 6400 bpi recording density capable of 23 Mbytes of unformatted data or 18 Mbytes formatted capacity on the 600' 3M data cartridge. It uses a 4-track record head and a serpentine read-after-write recording arrangement to eliminate rewind delays. The serpentine format reduces dump time for 20 Mbytes to about 15 minutes.

The model 6450 includes an embedded formatter with a full command repertoire. During read entry, 3 different thresholds are automatically selected. A phase-lock loop is used for data recovery, and the 6450 has full edit capability for block data at any location on the tape. Kennedy also produces a model 6455 start/stop model that uses a "gap on the fly" technique to make it perform like a streamer, yet offer the advantages of archival retrieval. The 6455 also has an unformatted capacity of 23 Mbytes.

Archive's chief offering in the 20 Mbyte range is the Sidewinder streaming drive. It is available with a choice of either 30 or 90 ips speeds. The main difference is recording time, not storage capacity. The Sidewinder will record 20 Mbytes in 4 minutes at 90 ips or in 12 minutes at 30 ips. The factory selected speed is not selectable in operation but the speed options should keep pace with some of the faster hard disk systems. Archive also claims to use 97% of the tape.

Unlike start/stop machines, the Sidewinder does not have to withstand the stress and wear of start and stop operation. Archive has selected a durable glass-reinforced polycarbonate material for its mounting frame. J. V. Howell, Archive's VP of Engineering, claims that, "the polycarbonate frame is a more reliable mechanical base than a metal frame because it is more flexible. It has the same thermal characteristics as aluminum and seems to wear better." Archive uses rubber shock mounts to unload torques and stresses from the frame to the mounting structure.

Archive provides a unique controller with the Sidewinder to relieve the host of functions such as formatting, data interrupt, error and file mark processing and tape positioning. Automatic read-after-write error correction, block buffering, and read entries are transparent without host intervention. It also includes automatic stop, repositioning, and restarting if the host is unable to meet the streaming rate.

Sam Thompson of Data Electronics expresses a good deal of confidence in the ¼" cartridge drive market. He guesses that it will grow from a level of 100,000 drives in 1982 to more than 250,000 by 1985 for ¼" streamer drives alone.

Major members of the Data Electronics Inc. disk backup family include "The Funnel"—a high density digital cartridge start/stop tape drive, with a capacity of 17.28 Mbytes, a recording density of 6400 bpi, a cost per kbit of about 1¢ and a data transfer rate of 192 kbits/sec; "The Streamer"—a streaming tape drive that includes a μP-based controller/formatter, 10- or 20-Mbyte capacities, dual-track bidirectional read-while-write recording heads, digital servo electronics, digital magnetic tachometer, group code recording, and up to 5 Mbytes per minute data transfer; and "The Streaker"—a stripped version of "The Streamer" that does not include the streaming electronics but sells for under $500 in OEM quantities.

Data Electronics' Streamer is configured as a high-level, byte-parallel, FIFO memory; there is no

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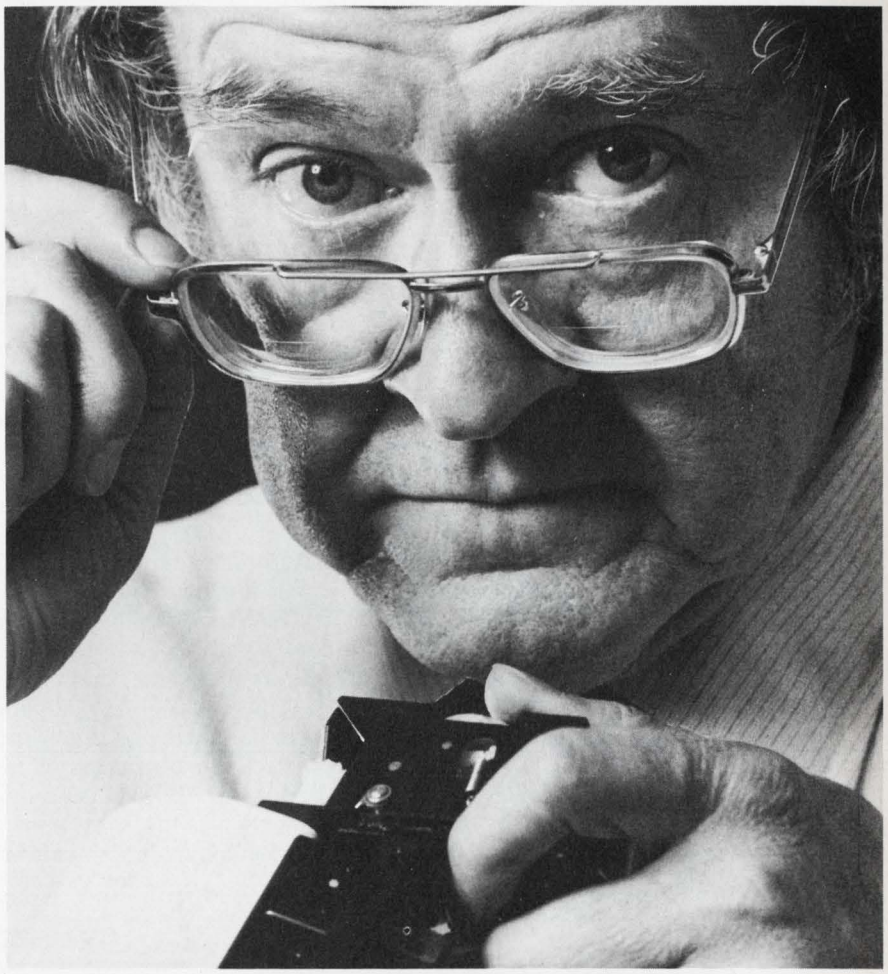

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restriction on block size. All algorithms for recording of data, restoration of data, and recovery of errors are included in the Streamer's controller. Data is sent to and from the Streamer via a simple asynchronous handshake. The Streaker is the "dumb" version and includes only R/W and servo electronics. All data written by the Streamer is checked for integrity and any incorrect or marginal data is rewritten without stopping streaming operation. The Streamer then qualifies the media and establishes a very high level of data integrity by setting the read-while-write threshold as high as possible. This is achieved by using a 3-bit D/A control of the read channel and using the eight available read thresholds for data verification and error recovery. The written data is verified byte-by-byte with the input data. The mechanical configuration of the read-while-write head, and the electrical design of the data channel assures interchange of data written on one Streamer at one environmental extreme and read on a different Streamer at the opposite environment extreme.

Currently, there are few high performance ¼" cartridge drives; however, more drive makers will be announcing products in the 40 to 100 Mbyte range later this year.

The read-while-write head is configured so that the read head follows the write head independent of tape direction, and the read track is narrower than the write track. Data is written in the standard ANSI GCR (ONES intensive) code to provide maximum separation between data bandwidth and speed variation (flutter) bandwidth, and provides maximum recovery window with frequent clock information. This provides for data interchange between cartridge tape drives operating at 30 ips and 90 ips.

Data written on a 10-Mbyte Streamer can be read on a 20-Mbyte Streamer. The first 10 Mbytes of data written on a 20-Mbyte Streamer can also be read on a 10-Mbyte Streamer. This upward compatibility is achieved by using the identical head design for both the 10- and 20-Mbyte Streamers. In the 10-Mbyte Streamer, the head is fixed. In the 20-Mbyte Streamer, the head is held against two precise surfaces.

The Data Electronics Funnel is a start/stop cartridge tape drive designed to back-up small fixed disk systems. The drive has the capability of a full tape peripheral with file search, track select, and the capacity to change or add to existing records. A high duty cycle motor with continuous start/stop capability enables the Funnel to construct

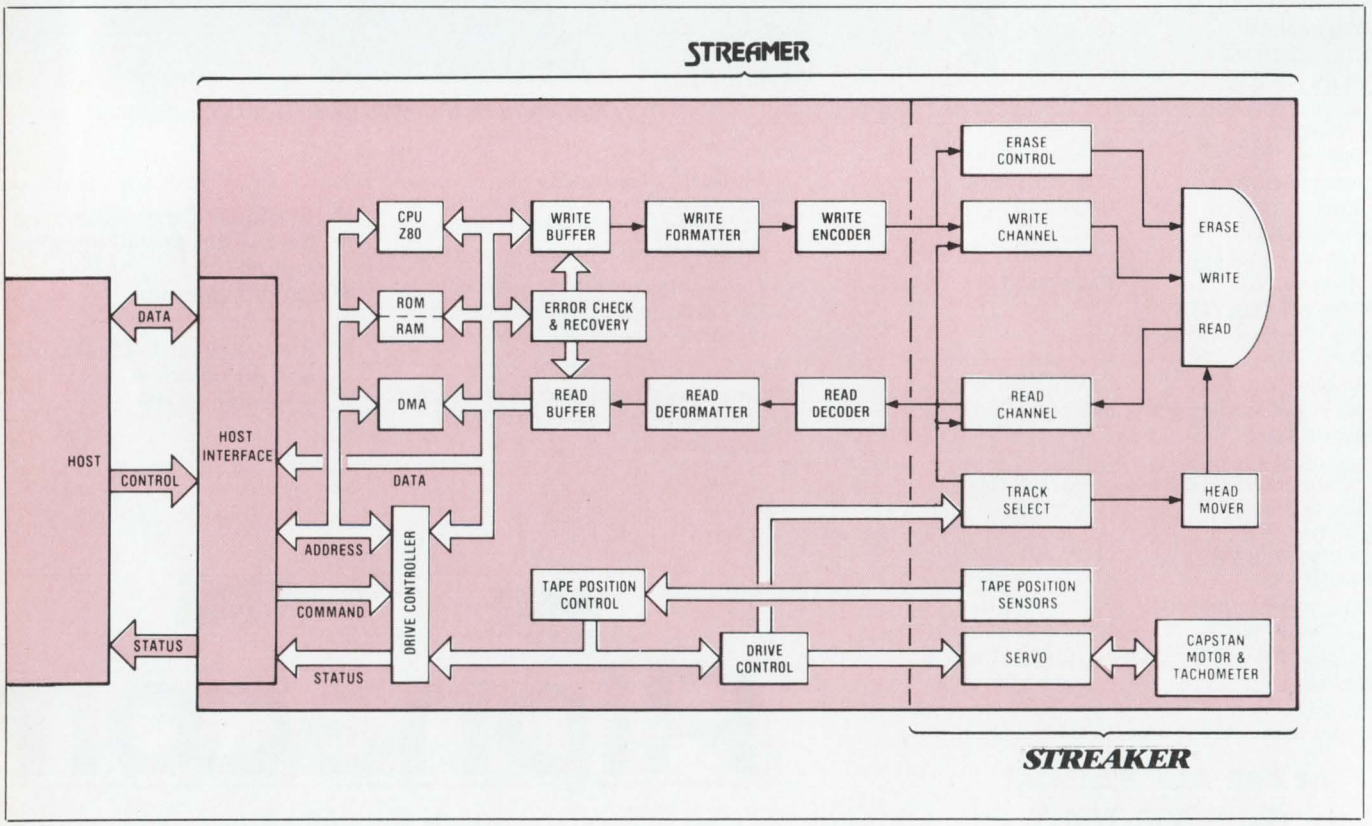

Figure 9: DEI's Streamer is a smart drive with full control and interface. The Streaker is the same mechanically without full control.

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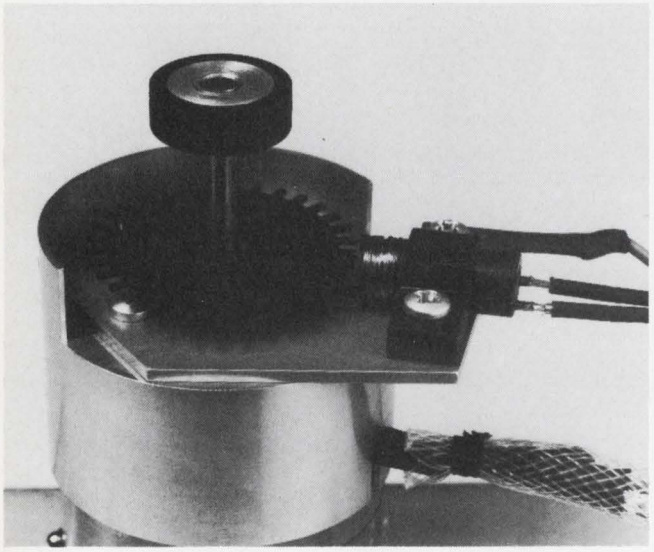


Figure 10: A simple magnetic tachometer is used by DEI to provide more precise tape speed control.

and read files with standard ANSI interblock gaps at 30 ips and locate and read these files at either 30 or 90 ips in both the forward and reverse directions. Up to 17.3 Mbytes of data can be stored on 4 tracks.

Standard features of the Funnel include an integral tape cleaner which greatly enhances error-free performance. A patented center-of-gravity mounting of the capstan motor allows the drive to be mounted in any position or attitude. A proprietary dual gap head provides for read-while-write data verification and has a separate erase to assure maximum data reliability.

Up to 8 Funnel drives can be connected together on a common Bus. A codec card provides data encoding of Binary (data and strobe) to a self-clocking MFM code and decoding MFM to Binary (data and strobe).

ANSI standard media is available from multiple industry sources, and controllers are available from a growing number of independent companies. The interfaces available include μ Nova, Nova, Q-Bus, S100, Multibus, LSI-11, Unibus and RS-232.

Cipher's Series 400 ¼" streaming cartridge tape drive, the Quarterback, was designed specifically for backup of lower capacity Winchester disks. When backing up 14", or 8" or 5¼" Winchester drives, the Quarterback can transfer 20 Mbytes of formatted data in just over 4 minutes.

Automatic read-after-write, error correction, block buffering, and read retries are performed transparent to the host, and the drive's interface design minimizes hardware and software compatibility problems.

Data is recorded onto the tape in 528.5 byte blocks. 512 of these are user data and 16.5 are overhead bytes, providing data separation, synchronization and error checking every 528.5 bytes. This unique format, when used with the run length limited coding techniques, provides data reliability and error detection and correction. Three 512 byte buffer memories are used, reducing software complexity while providing for interrupt handling.

Errors are detected and corrected automatically before the data is presented to the interface. All error detection and correction procedures are transparent to the host system and therefore no user subroutines or knowledge of error correction detection systems are required. During the write operation, should the read-after-write operation detect an error, the block is automatically rewritten.

The Quarterback tracks and reports through the interface, upon command, statistical error data which prevents progressive deterioration of the tape system due to bad tapes and marginal components.

Electronic Processors Inc. offers a 17.3 Mbytes (unformatted) storage capacity. The EPI model STR-Stream has all of the features of a full tape peripheral including construction of formatted data blocks, file updating, track select, read-after-write and CRC generation and verification. The standard STR-streamer deck includes R/W circuitry, NRZ to MFM encode/decode, infrared tape position sensing, formatter command and status lines, 4-track read-after-write head, CRC circuitry, and interface circuitry. EPI uses a heavyduty motor with an optional encoder for speed control.

How Do They Compare?

High performance ¼" cartridge drives like the 3M and Archive offerings stand alone without competition at the moment. More drive makers will be announcing products in the 40 to 100 Mbyte range later this year, so the competition may get tougher.

The mid-performance range of cartridge drives all look much alike and the choices are easier to make. The fact that there are so many products in this class helps the buyer get a better price. Reliability is probably the most important selection factor considered. Start/stop drives must be the most reliable because in operation they undergo the most stress. Streamers are less expensive because they are cheaper to build. The designer selecting any type of cartridge drive should be most concerned with MTBF. Most of the drive makers know the MTBF number they can meet. A few like Data Electronics specify greater than 3500 hours MTBF. 3M offers 10000 hours MTBF with routine maintenance on their 67 Mbyte unit. Kennedy publishes greater than 5000 hours as a MTBF design goal. The others do not usually include MTBF as part of their specifications. Perhaps they should—it would certainly be a help to the OEM designer.

On the mechanical side, the drives are even more difficult to

compare. Each should be judged on its merit. Motor size, cooling, plastic versus metal frames are all there is to compare. There are no giant companies in the ¼" cartridge drive market. Even 3M participates only in very limited areas. Companies in the market have their futures on the line, so the OEM designer should be able to count on these eager suppliers to be willing to meet his needs.

Inexpensive Solutions

As a backup, ¼" cartridge drives are the cheapest solution available today. They are inexpensive to purchase and operate. A good rule of thumb says that the backup should not exceed 50% of the cost of the main media. This type of cost is about where the cartridge drive manufacturers have priced their products. Products on the low performance end of the spectrum (1600 bpi) sell for as little as $400, and as performance increases, so does price. If the reader can find a reliable drive costing ⅓ to ½ that of the Winchester it backs up, then this is probably a reasonable choice.

Inexpensive to purchase and operate, ¼" cartridge drives are the cheapest backup solution available.

The Future

Operation at 90 ips with a cartridge drive may be a physical limit now, but improved cartridges may make higher speeds feasible. Tape tension and guidance by the cartridge need to be improved even if speeds remain fixed. Better media is also needed. Work is underway to bring some of the chrome and other high recording density materials into the data cartridge market. 3M currently produces tape for professional audio recording applications capable of 27,000 flux reversals per inch. As head technology for digital recording improves, this high density tape will probably find its way into the digital market.

Cartridge drives in the 120 Mbyte range should appear in the next year or two. Instead of competing with 3M at 67 Mbytes, the other leaders in cartridge drives may elect to go to the 100 Mbyte range.

The ¼" cartridge drives available today from the dozen or more manufacturers represent highly refined, reliable products. They are inexpensive and meet most of today's backup needs. □

Designing The DECmate II

by Jerry Cox

The DECmate II is a member of Digital Equipment Corp's recently announced family of personal computers; designed for use in office management and word processing, it has operational software compatibility with its predecessors.

Like its predecessors, the DECstation and the DECmate I, the DECmate II employs a 12-bit-word-length μP, in this case, a custom-designed second-generation 6120 μP that employs an extended version of the PDP-8 instruction set. Unlike its predecessors, the mechanical organization of the DECmate II has been developed to take advantage of components standard to Digital's new personal computer family, including 5.25″ floppy disks, a 5.25″ Winchester disk, the 12″ monochromatic CRT and keyboard.

In the case of both the DECstation and DECmate I, video terminals were extended to the role of terminal/processors. In the case of DECmate II, the processor has been located in a separate "system box" enclosure.

With no surprise innovations in the hardware, DECmate II builds on existing customer software base for support.

In both predecessor systems, the central processor was located in the video terminal (thus, the DECstation terminal/processor is also known as the VT78; the DECmate I, the VT278). The VT78 was designed from a VT52-like terminal, and the VT278 from a VT100.

Characters were written to the screen on a DECmate I at a speed roughly equivalent to writing to a conventional terminal running at 9,600 baud. With DECmate II, the equivalent is on the order of 50 to 70 kbaud. On the basis of performance, it takes something less than 2 sec to perform a full screen update on a DECmate I and on the order of 0.1 sec on a DECmate II.

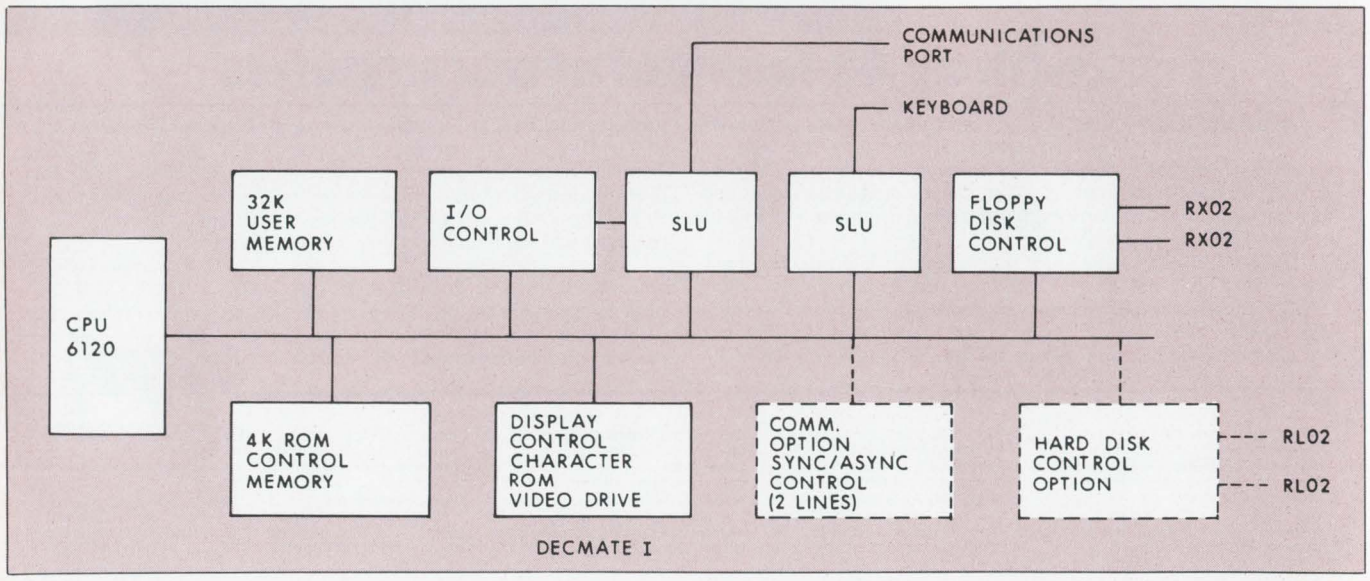
In the DECmate I, the processor was built into a VT100 video terminal shell but design considerations eliminated some of the standard VT100 functions such as split screen and smooth scroll.

When the DECmate I was used as a terminal to a VAX-11's VMS operating system, there were problems, since the VMS applications programs were written on the assumption that it could use all the functions on the VT100's specification sheet when it was talking to a video terminal. So the decision was made that DECmate II would appear to a host computer as *at least* a VT100.

As with Digital's VT100 series of video terminals, the attributes such as standard or reverse video, 80 or 132 column mode, auto-wrap-around, cursor, and scrolling type, are selectable by the user. The system has certain video terminal de-

Jerry Cox is Product Manager of the DECmate II, at Digital Equipment Corp, 129 Parker St, Maynard, MA 01754.

Figure 1: Basic structure of DECmate I shows internal bus connections. Connections to peripheral equipment is made through ports.



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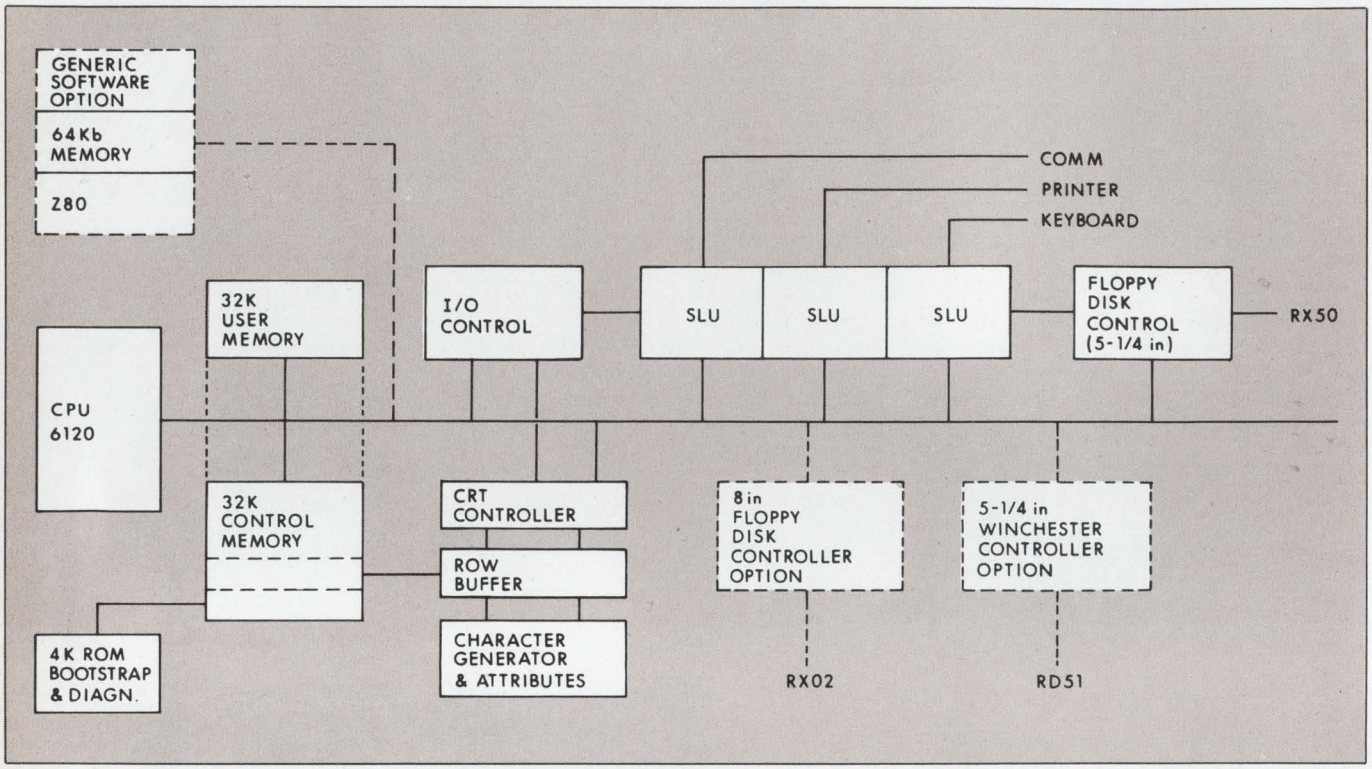


Figure 2: Basic structure of DECmate II illustrates direct evolution from DECmate I. The unit employs a full 32 Kword control memory, which includes screen buffer. Note that the auxiliary processor option (APO), designed to run CP/M 80 application software, is a full secondary processor assembly complete with independent memory.

fault characteristics (e.g., white letters on a dark screen background), which the user may modify for specific applications.

The transition to the 5.25″ floppy disk (sometimes called "mini-floppy") was interesting for the DECmate II design in that both of its predecessors employ 8-inch floppy disks; and, related PDP-8-based word processing systems can also employ 8″ floppies as document diskettes. The new smaller disk is formatted with 80 tracks and 10 sectors per track as opposed to 77 tracks with 26 sectors per track on the 8″ floppy disk, and has a capacity of 408 Kbytes (204 Kwords) as opposed to 256 Kwords for the larger disk.

The controller for the new floppy disk drive is incorporated into the basic processor board rather than being on separate boards as on the DECmate I. The controller has its own μP and its own ROM and RAM dedicated to handling the floppy disk.

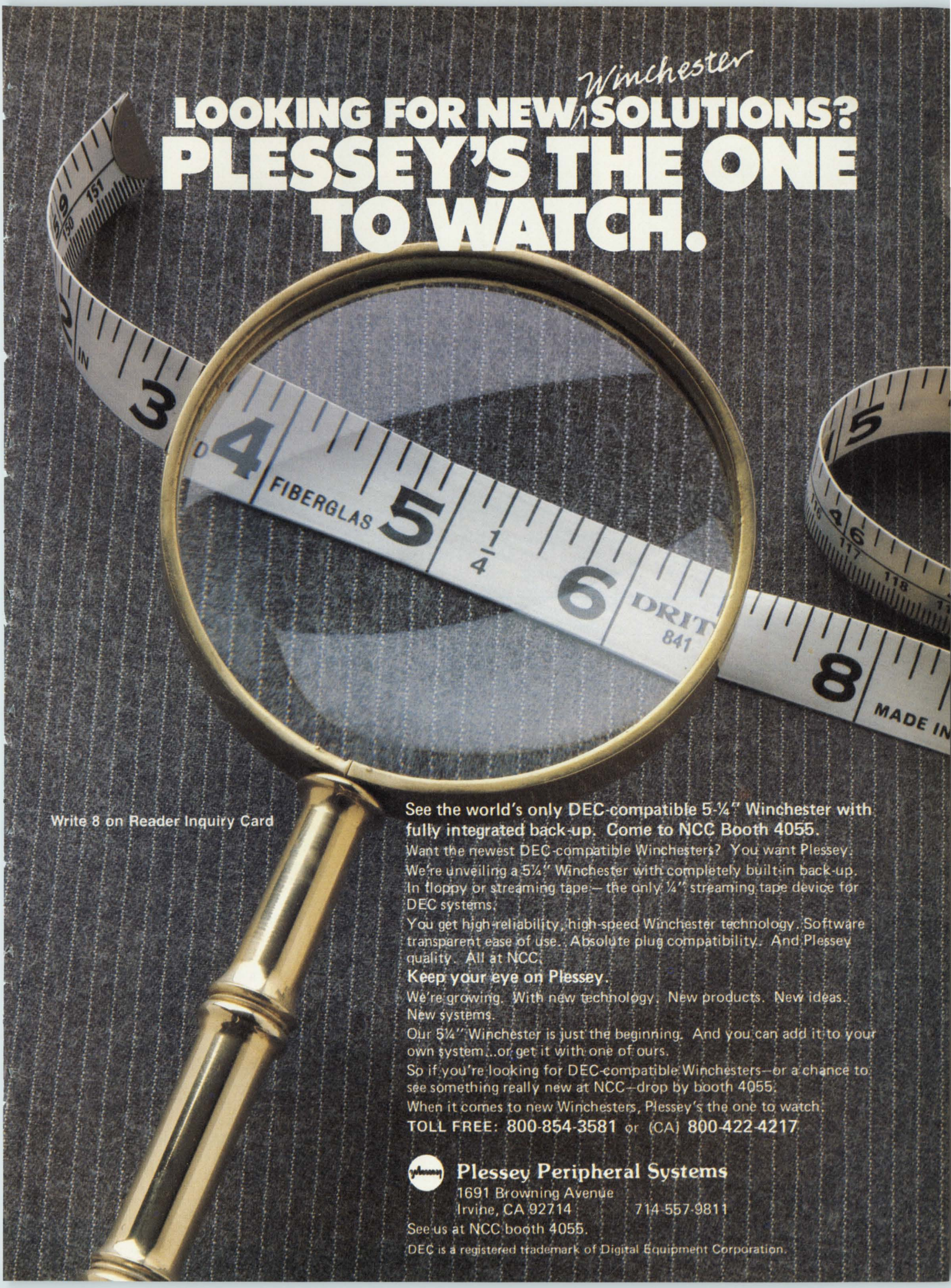
The PDP-8/As through DECstations through DECmate I and into DECmate II are software compatible. It is only necessary to make changes to accommodate the fact that the 5.25″ disk has a different number of sectors per track, a different number of tracks, and a different total capacity than the old disk. It becomes a relatively simple job to adapt the software, not a major rewrite.

One of the design requirements of the DECmate II was to enable a user who has a number of files on 8″ floppy disks to be able to use those files with DECmate II. To achieve this, an interface was designed that would enable users to add 8″ floppy-disk drives if desired. The disks can either be used as document diskettes as before, or the files can be transferred onto the new 5.25″ disks if the user desires. Besides being able to maintain files in mixed media, this capability also ensures that users can exchange document disks between different word processing systems.

A result of this design decision is that people requiring more than one word processing system in a facility can buy a DECmate I with confidence, since the 8″ floppy disk option on DECmate II insures that the DECmate I will not become immediately obsolete.

The adapter to enable the standard 8″ floppy disk drive, the RX02, to interface to the DECmate II is one of several possible options designed to work with the new personal computer. Another of these is a daughter circuit card with a Z80 μP and 64 Kbytes of associated memory that plugs into a pre-defined slot connecting to the DECmate's internal bus.

The "auxiliary processor option" (APO) gives DECmate II the ability to run CP/M 80 application programs. This feature was added for two reasons: one was the easy availability of low-cost generic software for those wishing to implement a computer system with specialized application programs at low cost; the second was that the other members of Digital's family of personal computers were all planned to have the capability to run CP/M 80 programs, thus developing a potentiality for commonality between all current members of



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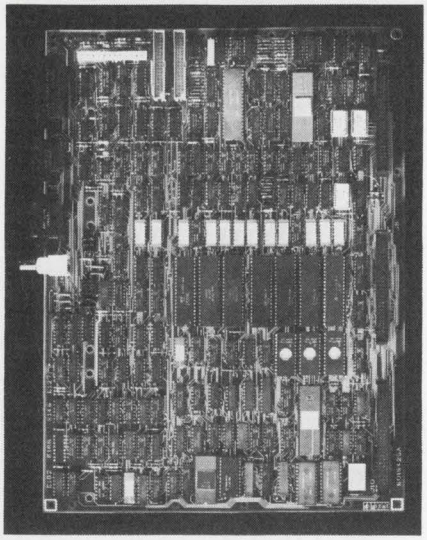

Figure 3: View of the processor board, which contains all (non-dotted) elements shown in the DECmate II diagram.

the family, and with the VT100 terminal with the VT18X CP/M option added.

In developing this option, advantage was taken of the structure of the DECmate II for I/O operations. When the APO is in operation, the 6120 processor, which still controls the overall system, functions as a controller for the Z80 subsystem, transferring communications between the APO and other system elements.

The design of the disk controller makes it possible for it to test and identify disks by format and content. This makes it possible to employ Z80 disks in the same drive as for PDP-8+ disks; the system disk has to be formatted specially, but application-program file disks can be in the same format as those used on other Digital CP/M 80 personal computers or options.

Another daughter-board "slot" was added to enable users and system integrators to add Digital's newly announced 5.25″ Winchester storage disk. The size of the current DECmate II system box requires that the Winchester disk be located externally.

The one thing we cannot have with any device connected through the interfacing slots is DMA. The lack of a standard bus prevents this. DMA can occur only within specific units on the mother board.

Another item integrated directly onto the mother board is the communications controller. On the DECmate I, the communications controller had to be on a separate card (i.e., not on the processor card) and was an option. Although it had provisions for two lines, it was determined that the majority of users only had need for a single line. The communications controller is standard on DECmate II, uses a single line, and provides a full-duplex serial port for either asynchronous or synchronous operation. In synchronous operation, either bit- or byte-oriented protocols may be selected by the user. Full modem control is provided.

With the communications facility, DECmate II can take advantage of its software facilities associated with its word processing application program. It can be integrated into electronic mail systems, using its CX facility, and can be connected to subscription services such as Dow Jones. Its DX communications facility enables it to transfer documents electronically to other word processors or host systems with DX capabilities, including the DECmate I.

Physically, the development of the DECmate II was dictated in large part by the dimensions of the system box common to it and to two of Digital's other personal computers, the RAINBOW 100 and the Professional 325. This gave a different environment than the terminal shell of DECmate I.

One of the concerns in the DECstation and DECmate I was the environment in which the processor board(s) had to operate. As noted earlier, both these devices were convection-cooled, and the addition of more circuitry increased the heat dissipation of the whole assembly. One design goal, therefore, was to limit the amount of power to the processor and associated circuitry.

The system box of DECmate II has a dual floppy-disk drive, and therefore a fan. This means that forced-air cooling is built into the system, and higher power levels could be used—including those employed by the improved 6120 μP. □

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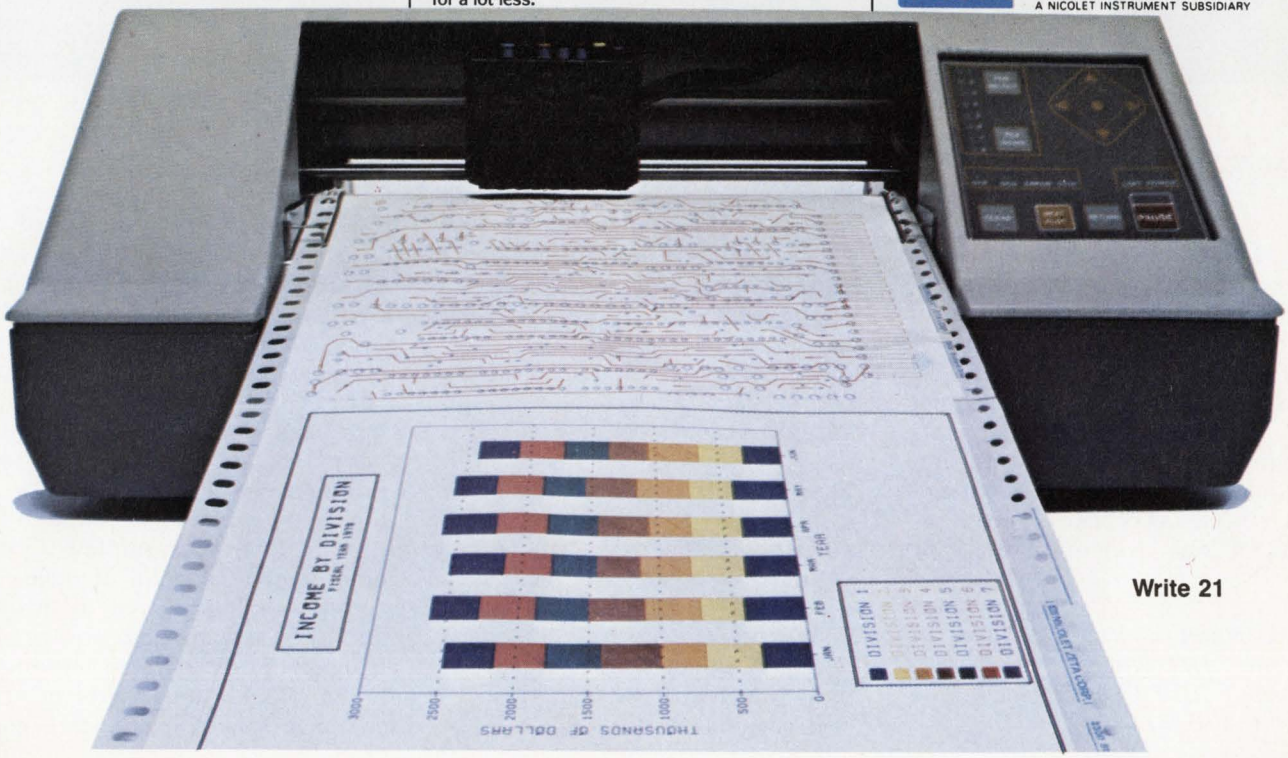

Write 21

A New Concept In Workstation Design

by M. C. Hahn

The Corvus approach to distributed processing with shared mass storage and peripherals has led to the development of Winchester disk systems and the Omninet local area network for several different μCs. But to provide a completely integrated system without the inevitable compromises of standalone μCs as network workstations, it was evident that a new type of personal workstation was needed, a new design that would integrate Omninet hardware and Constellation II network management software.

This personal workstation would have to provide a user interface to the Omninet network, and be compatible with existing software and hardware bases. Yet, it would need to have a small enough footprint to fit on the corner of a desk, and fit in the under $5,000 personal computer price range.

Trade-offs between the latest generation of hardware and some innovative software solutions have enabled Corvus Systems to achieve these goals with the Corvus Concept personal workstation.

Mark Hahn is Vice President of Product Development at Corvus Systems, 2029 O'Toole Ave., San Jose, CA 95131.

Screen Display

One of the major elements of the Concept's human interface is the screen display. For maximum ease of use, a high-resolution (35 MHz), full-page display which could be used interchangeably in either the portrait or landscape configuration has been provided. This feature minimizes the need for a local printer at each workstation by allowing the user to view either a full page of text or a complete 13 column spread sheet all at once. To accomplish this degree of flexibility, the screen had to be bit mapped. The typical hardware solution would have involved two complete sets of character genera-

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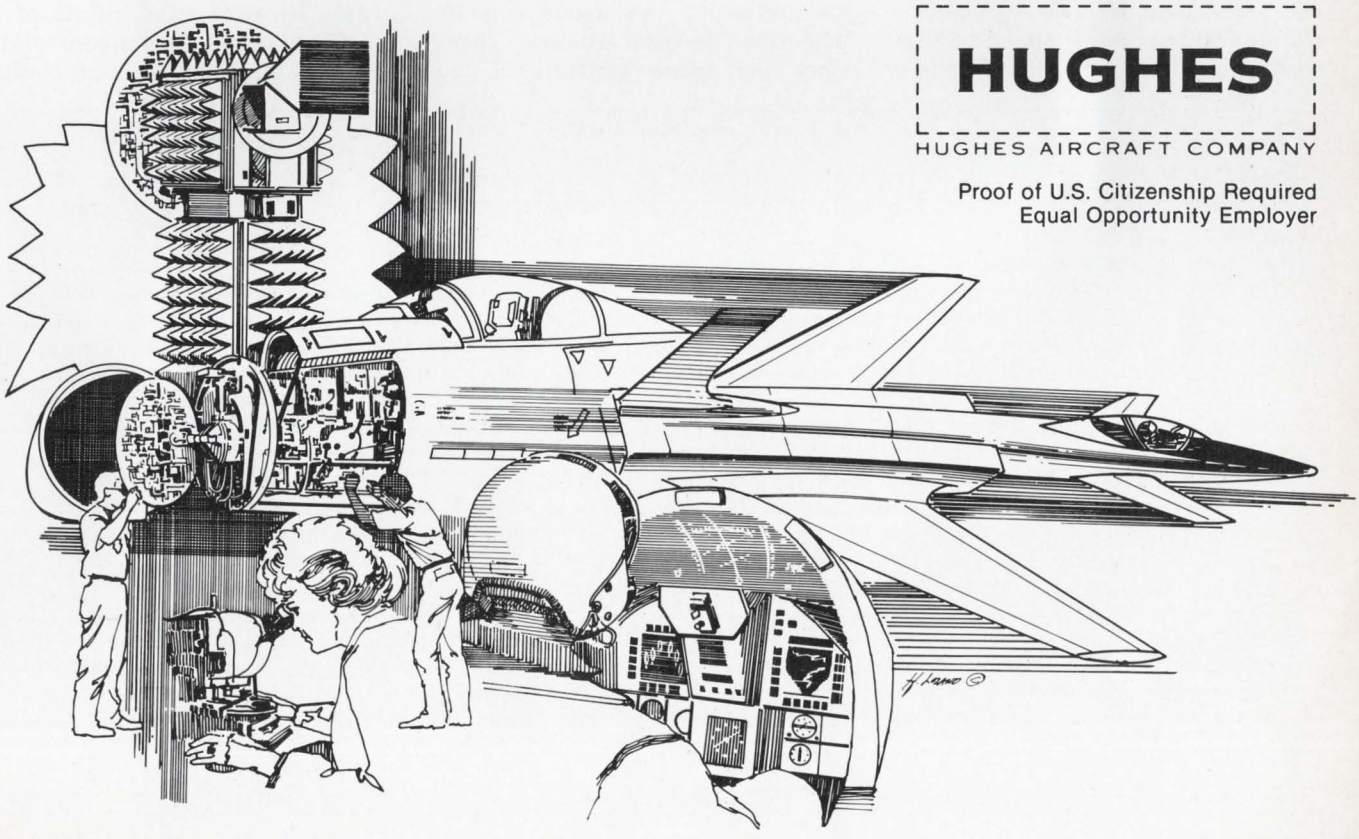


Using trade offs between the latest generation of hardware and innovative software, Corvus has introduced its latest product—a personal computer workstation.

tion hardware, one for each orientation. Instead, by taking advantage of the power of the Motorola MC 68000 and the standard 256K RAM board, these design goals were accomplished with no character generation hardware whatsoever.

The Corvus Concept actually paints the fully adjustable screen (both tilt and swivel) under complete software control. Approximately 55K of main memory is ported directly to the 720 × 560 pixel screen under DMA. Thanks to the 8MHz pipeline speed of the 68000, the characters can be painted at a 25 Kbaud rate—a faster rate than the 19.2 Kbaud limit of the RS-232 port used for most terminals.

Less hardware means less board space, smaller power requirements, and lower cost for the user, and it also means greater flexibility. For instance, the Concept offers either a white on black or a black on white display with no hardware overhead. In addition, multiple character sets of varying sizes can be created easily by the end user without additional PROMs because all character generation information is stored in software. The change from the portrait to the landscape orientation is accomplished automatically by loading the appropriate software for each orientation at system boot up. In the portrait orientation, the screen displays 72 lines by 80 columns with the standard character set. In the landscape orientation, it displays 120 columns by 56 lines at once.

Another feature made possible by the software-controlled screen is the standard multiple-window operating system. The screen can be divided into a number of windows, and different operations can be performed in each window. Then, since the entire contents of the screen are stored in main memory, the resulting display can be dumped to a printer just as it appears on the screen. This feature allows the user to combine text and graphics on a single page.

Keyboard Interface

The same software-based approach was used with the other major user interface—the keyboard. In this case, however, the overriding concern was not to eliminate hardware but to provide greater flexibility. In the final design, every key of the Concept's Selectric-style keyboard (including the 10 programmable function keys) are controlled by system software. In hardware, every key appears the same as every other key, and each key generates an interrupt both when it is pressed down and when it is released. In effect, the keyboard is key mapped into main memory just as the screen is bit mapped into main memory.

It may appear that the key map approach to keyboard control would involve undesirable tradeoffs in data entry speed. With the existing generation of 8-bit machines this could have been the case. However, the speed of the 68000 allowed the implementation of key mapping without compro-

Omninet LAN Connects Concepts

The Omninet local area network (LAN) connects as many as 64 Corvus Concepts or other μCs or peripheral devices on a common bus using twisted-pair cable as the network medium. By using an intelligent network interface—the transporter—Omninet implements the first four layers of the ISO/OSI network protocol (up through the transport layer) without the need for a master controller or host computer. It can transmit data at the rate of 1Mbit/sec over network lengths of up to 4,000 ft., and the integral intelligence of each transporter allows different brands of computers to communicate over the same network.

The heart of the Omninet design involves three ICs: a custom gate array, an Advanced Data-Link Controller (MC 6854), and a single-chip μP (MC 6801) with a custom mask. The resulting design uses carrier-sense multiple-access (CSMA) for network control, but the intelligence in the transporter obviates the need for costly collision detection circuitry. With two levels of carrier-sensing hardware as well as collision-avoidance software, collisions are almost always avoided.

Omninet was designed to require a minimal amount of additional hardware for direct memory access (DMA) to almost any processor bus. This feature makes it easy to design in the required hardware right on the motherboard of the computer. This was the approach used in implementing Omninet on the Corvus Concept. The same approach is being followed by other computer manufacturers who have licensed the Omninet technology from Corvus.

The ability to design Omninet with just a few ICs allowed large cost advantages when compared with other networking schemes. (It is estimated that including Omninet added less than $100 to the retail price of the Corvus Concept.) It provides each user automatic access to Corvus Winchester disk mass storage (currently up to 80 Mbytes) and Corvus Mirror video tape Winchester backup as well as to printers and other peripherals. Later this year, Omninet will also offer an X.25 broadband gateway to other Omninet local networks up to 40 miles apart.

mising the quality of the user interface. As a result, auto-repeat, type ahead, shifting, and many other features that are hardware controlled in other systems are software controlled in the Concept. This type of control makes it a simple matter to change the function of any key for any present or future application.

Software Compatibility

To offer compatibility with an existing software base, it was felt that the Concept should provide users access to CP/M, without the cost of providing a separate 8-bit processor. As a result, Corvus took advantage of the power of the 68000 to create a Z80 emulator which is completely software driven.

The emulator creates a 64K space which represents the memory space of a virtual Z80 machine. The effective speed of this virtual machine is slightly over 1 MHz for compute-bound programs. But, because the BIOS is outside the 64K space, all I/O is done in 68000 native code. The resulting execution speed of any program with a reasonable amount of I/O is actually faster than the typical 2 MHz Z80 speed. The Concept's ISO Pascal (with UCSD extensions) and FORTRAN-77 native code compilers work together with the Z80 emulator to provide compatibility plus the power to create the next generation of software.

Hardware Compatibility

Compatibility with an existing hardware peripheral base was also an important design goal, and a choice had to be made between offering back plane connectors or an I/O bus. Considering the network orientation of the Concept, relatively few I/O requirements were needed at each individual station. Also, the reliability of back plane connectors was a concern together with the additional hardware support they would require.

As a result, the 50-pin Apple II/III card sockets were chosen for local I/O. This choice enables access to a large existing peripheral base. Four 50-pin card sockets are at the back of the board in a pull-out drawer; combined with the Omninet connector and the two RS-232C ports on the back panel of the base unit, this arrangement offers the potential for expansion. This is especially true because the Concept's built-in calendar/clock and optional memory expansion (to 512 k) do not require the use of card sockets.

By using the power of the MC 68000, the Corvus Concept offers an integrated user interface to the Omninet local network. It also provides software and hardware compatibility by applying innovative software solutions to what have traditionally been hardware problems. □

Low Cost Components Make Color Graphics Practical

by D. L. Ruhberg

Probably the slowest link in most computerized control systems is the display of information for human interpretation. In applications where a large amount of information must be displayed in the same screen area, a color graphics system can easily provide this information by using a wide range of contrasting colors. Until recently, the high cost of sophisticated components and color monitors required to generate and display color information has been the main prohibitive factor in development of these systems.

Now, the cost of components and color monitors has moderated to the point that using a color graphics system offers a viable solution to information display.

A state-of-the-art color graphics system using the MC68000 16-bit μP with an economical MC6845

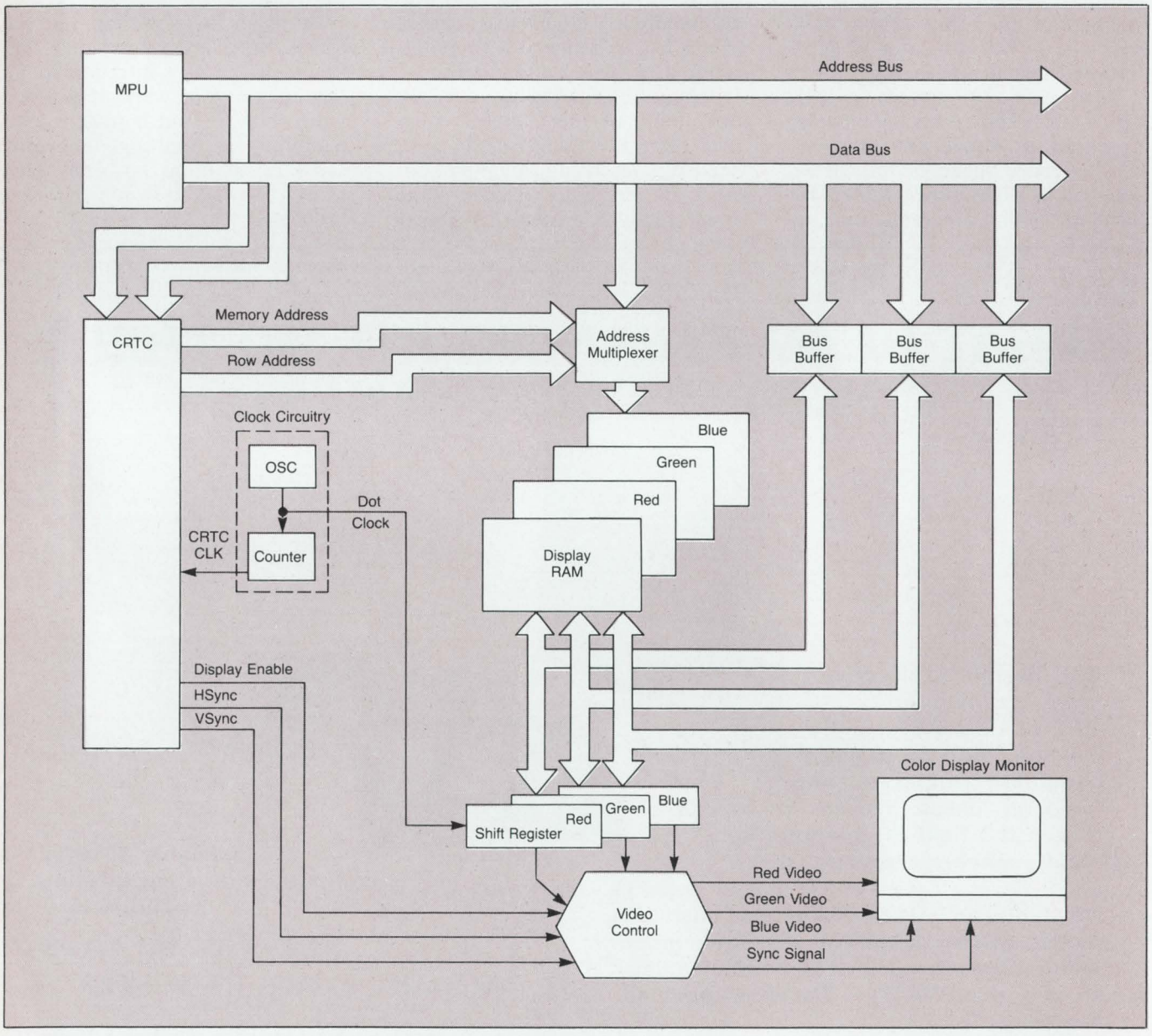


Figure 1: Block diagram of the color graphics system.

A color graphics system using the MC68000 and the MC6845 offers state-of-the-art performance at low cost.

CRT controller (CRTC) is described in this article. Hardware improvement is evident in data movement occurring in 16-bit words and multiply and divide commands, while software compatibilities are greatly enhanced with a processor that executes instructions that operate on 8-, 16-, or 32-bit operands.

General Graphics Approach

The general approach to a color graphics system is straightforward and almost identical to a black and white graphics system. The μP has two responsibilities to the graphics system: first, to initially program the CRTC, and second, to transfer data to the display RAM.

Once the clock circuitry is running, the CRTC is initialized and the address lines to the display RAM begin incrementing sequentially. As this occurs, the appropriate data from the display RAM is loaded into the shift register and then gated out serially by the dot clock input to the shift register. The display monitor then interprets the data as either turning a particular pixel on or off.

A color graphics system **(Figure 1)** uses the same principle as a black and white system except that it has to control three color guns (red, green, and blue) instead of just one. Therefore, there is an increase in the amount of hardware involved, but not in circuit complexity. The software becomes more involved due to the fact that more information is being handled and displayed. The basic display system works on the principle that three bits (one for each color) control each pixel instead of just one as in a black and white system. If two guns are on, the resulting color is a combination of the two. If all guns are on, white is the result. With this configuration a total of eight colors, including black and white, are available. Since the three bits needed to control a pixel do not fit into an eight-bit byte evenly, the unused bits could be used to obtain more colors or some other function. In addition, color systems usually require a separate sync input.

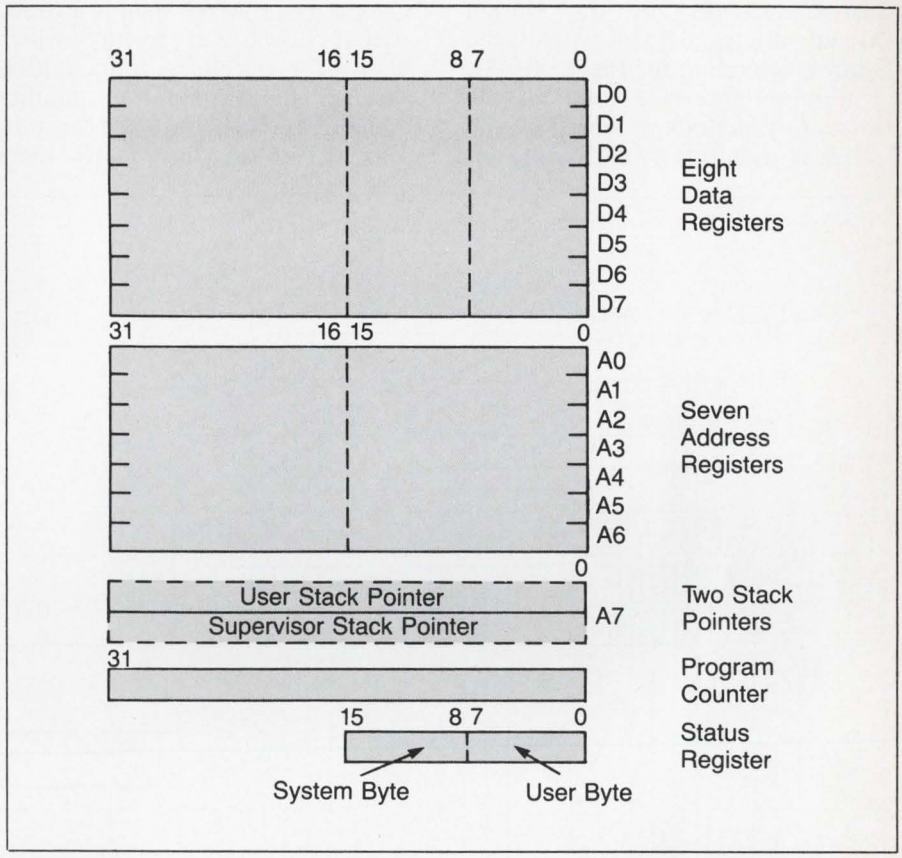


Figure 2: MC68000 programming model.

The versatility of the internal architecture of the MC68000 **(Figure 2)** enhances the effectiveness of the color graphics system. Besides containing a 32-bit program counter yielding 16 Mbytes of direct addressing range, the MC68000 also contains eight 32-bit data registers (DO–D7) and seven 32-bit address registers (A0–A6). The eight data registers are used for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The seven address registers and the stack pointer may be used for word and long word address operations. In addition, all address and data registers may be used as index registers.

System Hardware

This graphics system consists of two boards: a CPU board and a video board. The CPU board contains the processor, scratch-pad RAM, stack RAM, the program EPROM, and a terminal interface. The video board contains the CRTC, display RAM, multiplexers and buffers, parallel-to-serial shift registers, and the D/A drivers for the color display monitor.

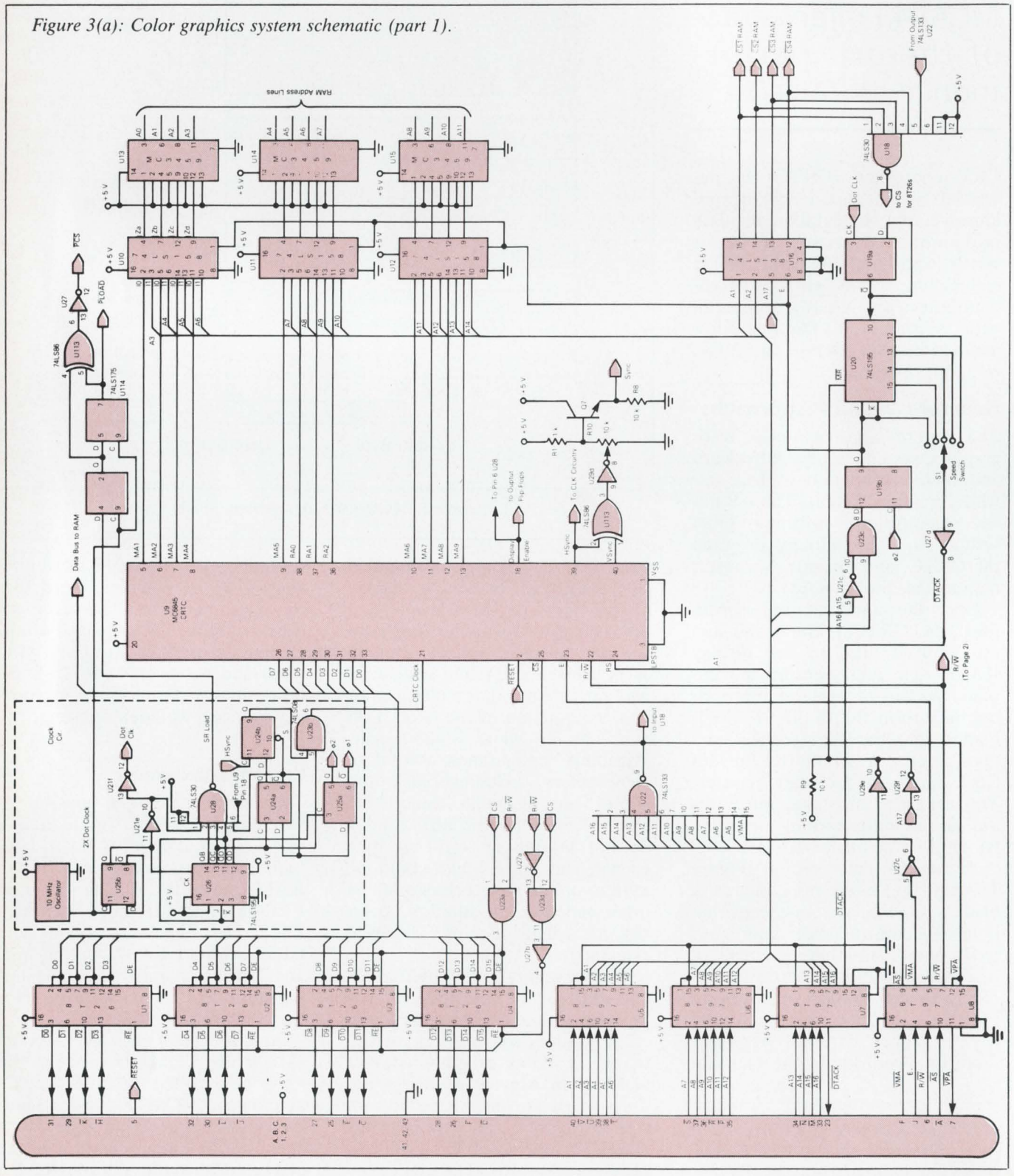
An MC68000 Design Module (MEX68000KDM) is used as the CPU board. The resources available on the MC68000 Design Module allow more design time to be spent on the unique features of the system. The major portions of the

David L. Ruhberg is a Microcomputer Systems Engineer with Motorola Semiconductor, Austin, TX.

system provided by the Design Module are the μP (MC68000), the address decoding for the EPROM, a terminal interface, and all the software functions provided by the resident monitor (MACSbug). Included in the MACSbug is a transparent down-load feature which allows the system to communicate through the terminal to another system. The other system can provide access to the floppy disks needed by this color graphics system for saving a full screen of data at a time.

The video board **(Figures 3a, b, and c)** contains more of the unique hardware features of the color

Figure 3(a): Color graphics system schematic (part 1).



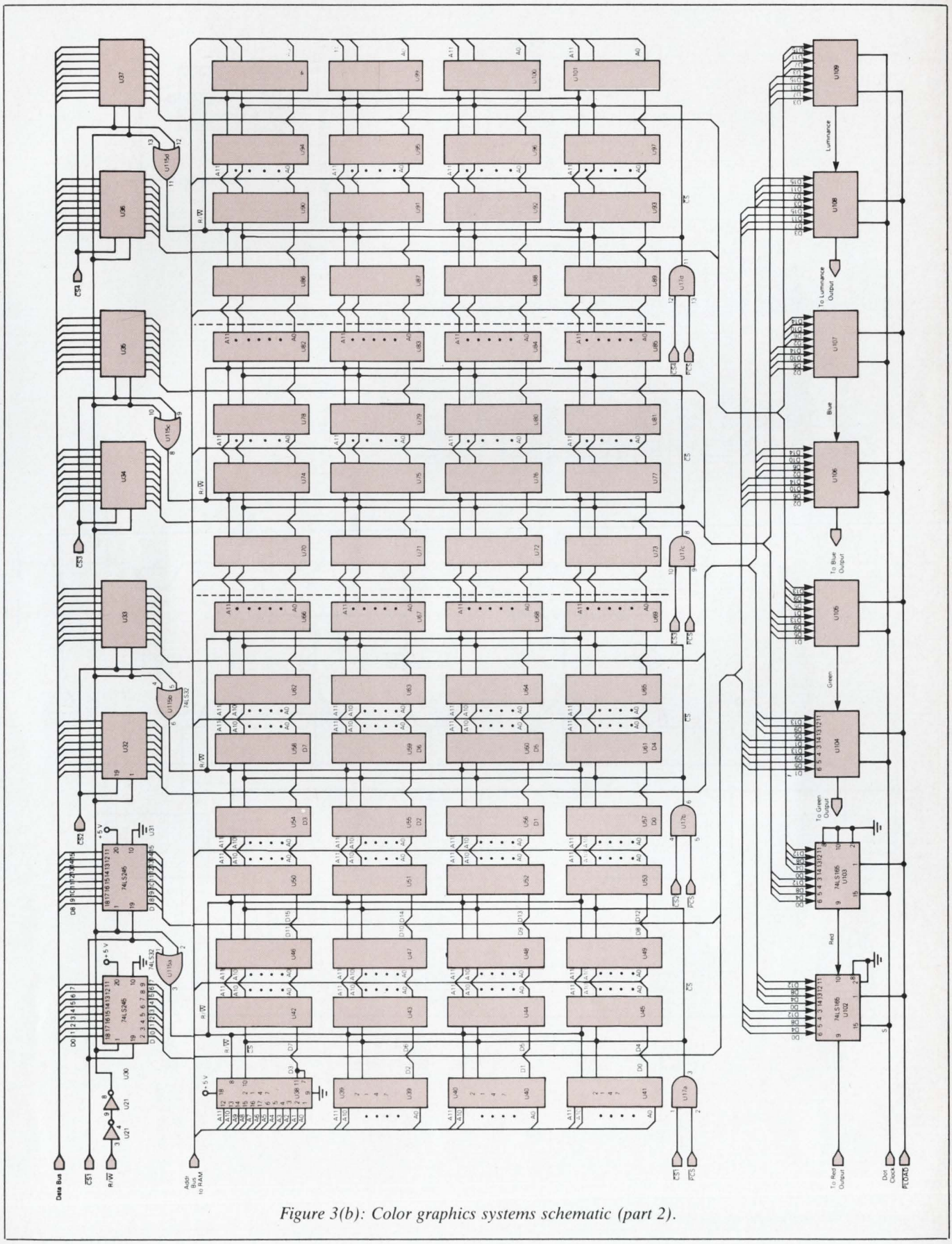
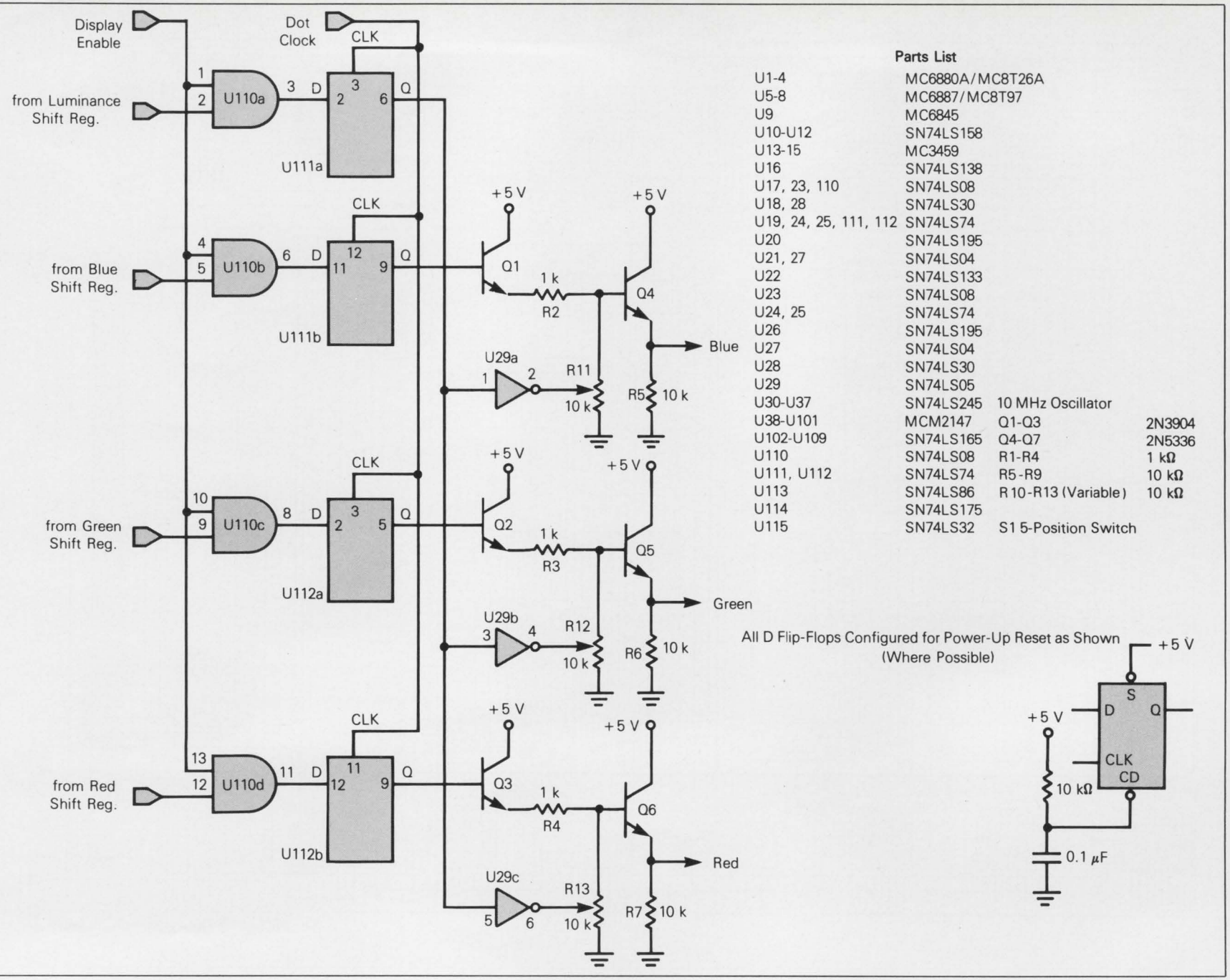


Figure 3(b): Color graphics systems schematic (part 2).



Parts List

U1-4	MC6880A/MC8T26A		
U5-8	MC6887/MC8T97		
U9	MC6845		
U10-U12	SN74LS158		
U13-15	MC3459		
U16	SN74LS138		
U17, 23, 110	SN74LS08		
U18, 28	SN74LS30		
U19, 24, 25, 111, 112	SN74LS74		
U20	SN74LS195		
U21, 27	SN74LS04		
U22	SN74LS133		
U23	SN74LS08		
U24, 25	SN74LS74		
U26	SN74LS195		
U27	SN74LS04		
U28	SN74LS30		
U29	SN74LS05		
U30-U37	SN74LS245	10 MHz Oscillator	
U38-U101	MCM2147	Q1-Q3	2N3904
U102-U109	SN74LS165	Q4-Q7	2N5336
U110	SN74LS08	R1-R4	1 kΩ
U111, U112	SN74LS74	R5-R9	10 kΩ
U113	SN74LS86	R10-R13 (Variable)	10 kΩ
U114	SN74LS175		
U115	SN74LS32	S1 5-Position Switch	

Figure 3(c): Color graphics system schematic (part 3).

graphics system. The video board can be separated into seven areas: the clock circuit, CRT controller, the DTACK circuit, the bus multiplexers and buffers, the display RAM, the shift registers, and the D/A converter drivers.

The clock circuit generates the five timing signals used throughout the video board; they are: a dot clock, a CRTC clock, a 2X dot clock, a shift register load, and a ø2 signal. The dot clock is used to drive the serial shift registers. The CRTC clock is used to drive the CRTC. The 2X dot clock and the shift register load are gated together to generate the parallel load (PLOAD) and chip select (PCS) signals for the shift registers and display RAM, respectively. The ø2 signal is also used to control accesses to the display RAM. A timing diagram of these signals is shown in **Figure 4.**

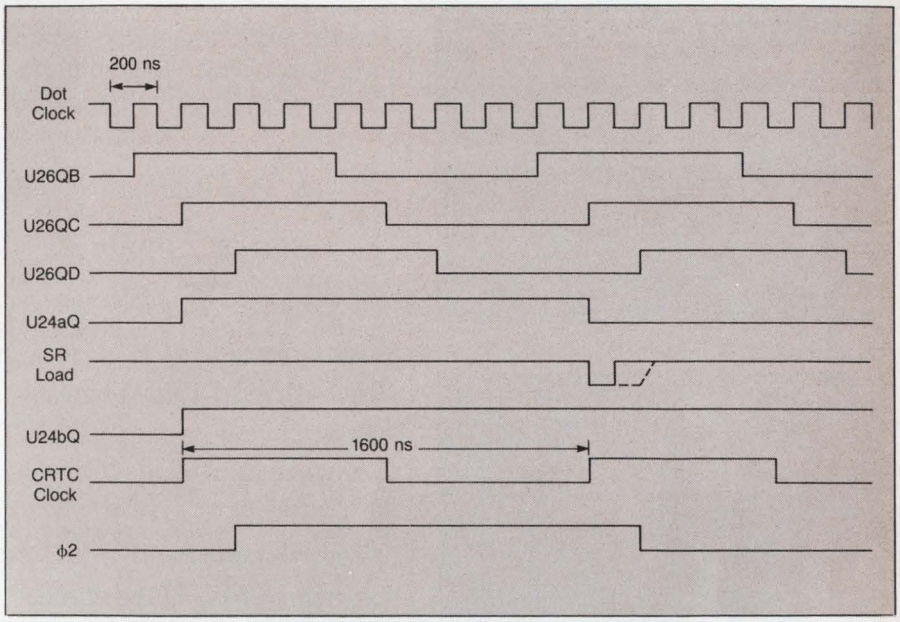


Figure 4: Clock circuitry timing signals.

CRT Controller

The MC6845 CRT controller (CRTC) is a programmable controller used to prepare the information in the display RAM for use by a video display monitor. The CRTC generates the signals required to provide data at the appropriate times. Since the length and period between these signals varies from system to system, the CRTC is designed to be programmed by an MPU.

In this system the internal registers are accessible synchronously through hex ($) address locations $1FFFD and $1FFFF. After programming, the CRTC provides the addresses, horizontal and vertical sync signals, and the display enable signal to the display system. The addresses, output by the CRTC in conjunction with the parallel chip select ($\overline{PCS}$) signal, are responsible for the correct data getting to the serial shift registers at the correct time.

The horizontal and vertical sync signals, after being "exclusively ORed," generate the sync signal required by the color display monitor. The display enable (DE) signal is gated (U28) into either the clock circuitry to inhibit the parallel load and $\overline{PCS}$ signals or is gated (ANDed at U110, if a low represents black on the screen) with the data stream to keep the guns in the CRT off during vertical and horizontal retrace.

In some cases, DE must be delayed due to specific requirements of the CRT being used. A one-shot on the output of the DE pin is usually more than adequate for providing the delay.

The $\overline{DTACK}$ circuitry is used to return an asynchronous data transfer acknowledge ($\overline{DTACK}$) signal to the MC68000 from a synchronous device (the display RAM). The ø2 signal from the clock circuitry in conjunction with address lines A15 and A16 develop the $\overline{DTACK}$ response required by the MC68000. When the display RAM address is between $10000–$17FFF, the $\overline{DTACK}$ signal is returned in 400 ns increments from zero up to 1600 ns after the enabling signal goes out to the multiplexers. This time is selected by the RAM speed switch, S1. Returning $\overline{DTACK}$ to the processor is the asynchronous access method by which the MC68000 can access external devices (RAM, ROM, and peripherals). This access method was chosen over the synchronous access method used to address the CRTC because it is faster and, since this is a highly repetitive operation, any time saved here will be significant in the overall speed of the system. The synchronous access method is used to access the CRTC since the CRTC is only initialized once and this method uses fewer components.

Multiplexers And Buffers

The multiplexers and buffers are used to feed the various control signals to the rest of the system. Multiplexers U10, U11, and U12 determine which address bus will access the display RAM. When the

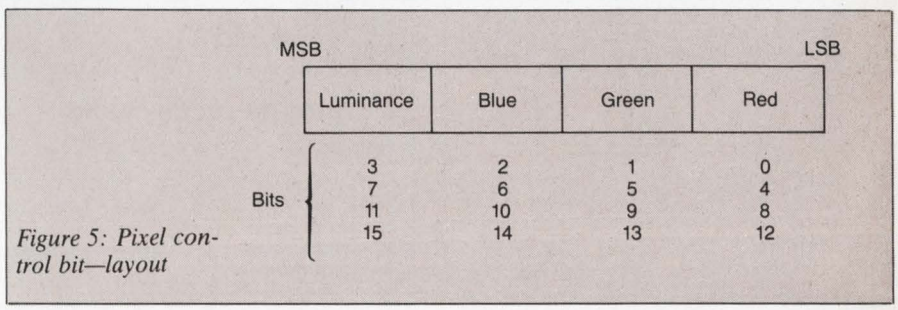


Figure 5: Pixel control bit—layout

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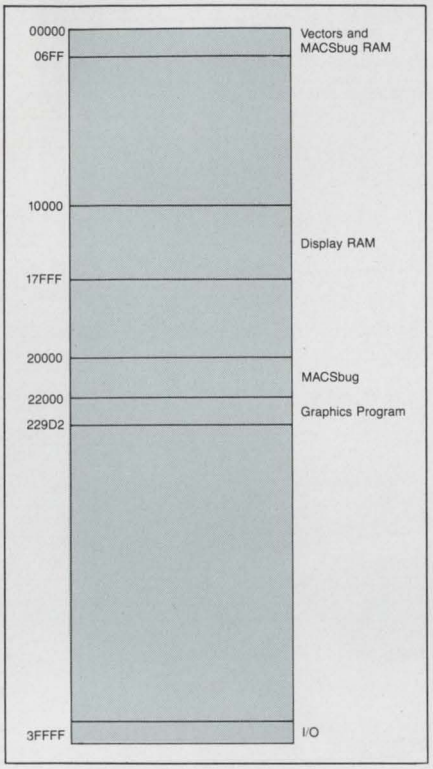

Figure 6: Memory map.

control signal is high, the MC68000 has access to the RAM and when low, the CRTC has access. Buffers U13, U14, and U15 are used to drive the large number of devices on the address bus. Data buffers U30–U37 are used to isolate the four banks of RAM from each other. Buffers are also used for almost all the signals coming onto the video board. These board buffers interface with the modified EXORciser bus which the Design Module uses. This bus has only sixteen address lines coming from the Design Module, so address line A17 must be run separately to keep the display RAM from being accessed at the same time MACSbug or the controller program is accessed (addresses $20000 and $22000).

The display RAM is organized into four banks (red, green, blue, and luminance). However, the address lines are configured so that consecutive words are located in consecutive banks of RAM. This was done to allow the programmer to visualize accessing one 16-bit wide bank at a time instead of accessing red, green, blue, and luminance banks all at the same time. The memories used are 4K × 1 static RAMs (MCM2147) which simplify some of the chip select circuitry. Dynamic RAMs could be used and should definitely be considered in a production system since they lower the hardware cost as well as power consumption. They were omitted in this application to simplify the system configuration. It should be noted that the CRTC keeps incrementing its address lines during horizontal and vertical retrace to keep the dynamic RAM refreshed. The speed of the static memories is not critical due to the presence of the speed selection switch explained earlier. As far as the CRTC and the serial shift registers are concerned, the memory looks like one 4K × 64-bit bank of RAM.

Shift registers U102–U109 consist of eight 8-bit, parallel-load, serial shift registers. They are configured to look like four 16-bit shift registers, one for each of the color guns and one for luminance. With the RAM and shift registers configured in this fashion, the RAM is accessed only 25% of the time. This means that the RAM has four times the amount of setup time and slower RAM can be used. The dot clock then clocks the data out to be gated with display enable.

Conversion from digital to analog voltages in this system is needed because a luminance bit is used to obtain more colors than are possible with the three guns digitally. The luminance bit is used to indicate half luminance when set and full luminance when clear. When all guns are off, the screen is black and the state of the luminance bit has no effect. Since the color display monitor uses an analog input on each gun, any number of colors may be obtained if the supporting hardware is provided. The D/A conversion used in this system was done to save space. A cleaner method would be to use special D/A converters and special line drivers for this function.

Software Description And Considerations

The software included to exercise this system consists of five basic commands:

CM— Clear Memory
BX— Box Draw
Q8— Random Line
ED— Edit
BA, SH } Provides the capability of saving (BA) a screen on floppy disk and calling (SH) it back.

The clear memory (CM) command clears the screen. The box drawing (BX) command draws continuously concentric boxes which close in on each other. This gives the effect of running up a hallway. The random line (Q8) drawing command picks random points and connects them together until they form a multisided polygon and then it continues to repeat that shape, all the while collapsing in on itself and changing colors. A scaling function has been implemented to keep the figure occupying a major portion of the screen. The edit (ED) command allows the user to draw figures on the screen using the cursor controls on the terminal and allows a choice of colors. The BA command is used to store a screen full of data on floppy disk and display it on the screen.

Each of the routines which write to the display RAM use the basic data layout for every pixel on the screen. Each pixel is controlled by four bits. Each bit corresponds to either luminance, blue, green, or red, as shown in **Figure 5.**

A memory map for this application is given in **Figure 6.** The complete program is available from Motorola. Request application note AN-834 from Motorola Semiconductor Products, P.O. Box 20912, Phoenix, AZ 85036.

The resolution of the display in this application is 256 × 256 pixels. The density could be doubled in both directions to 512 × 512 by quadrupling the memory. This can be easily done if dynamic RAM is used since 4K × 1 and 16K × 1 dynamic RAM can be arranged in the same basic configurations. As space was one of the design criteria in this application, some of the more straightforward approaches were not taken. □

B & W Raster Terminal Has Highest Resolution

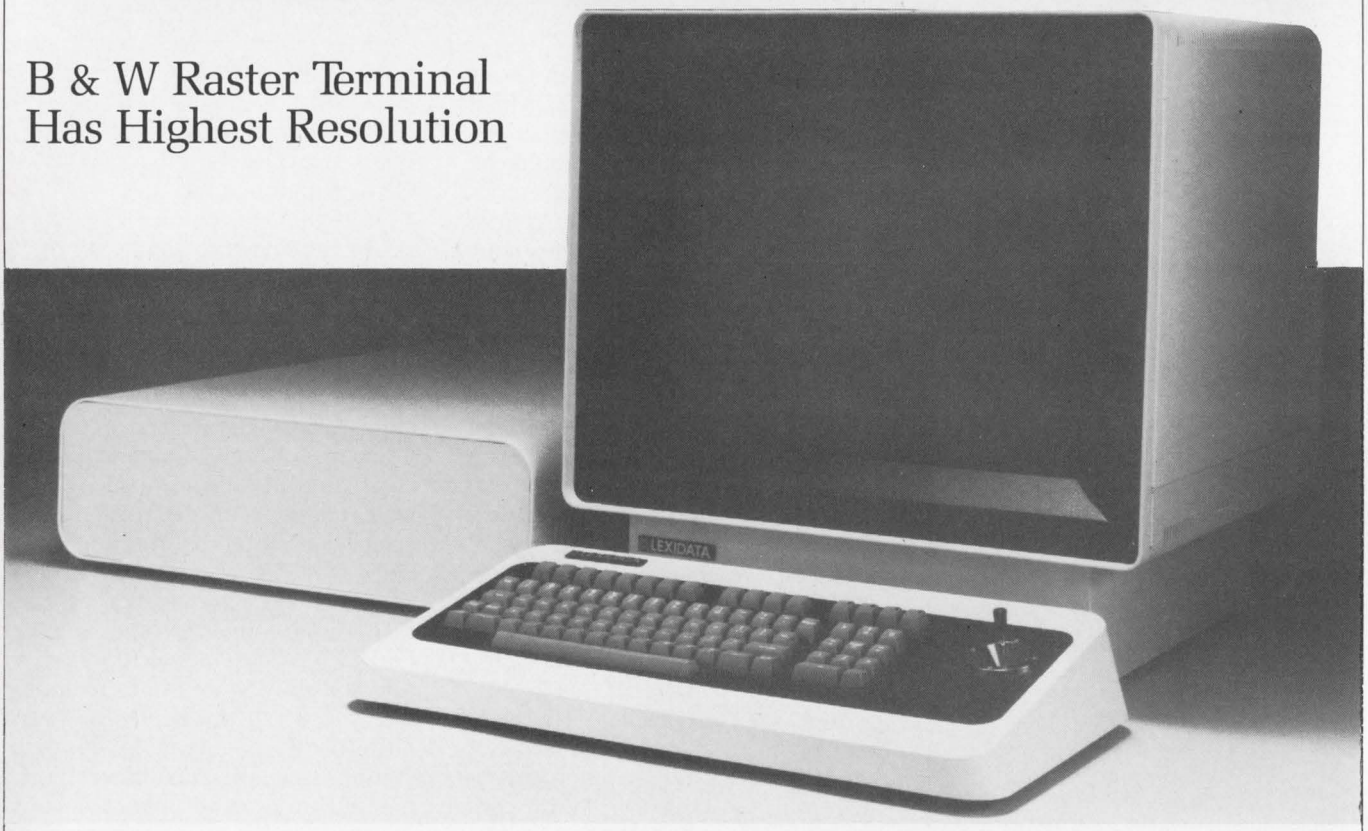

Figure 1: With a resolution of 1280 × 1024, Lexidata claims their Model 2400 is the highest resolution black and white graphics workstation available.

Shown for the first time at NCGA, the Model 2400 is an intelligent, monochromatic raster display system designed specifically for OEMs. The 2400 is the first member of the new System 2000 family from Lexidata, which will soon include medium and high-resolution color terminals as well.

The 2400 consists of a single electronics module containing all system electronics, a 19″ monochromatic, 125MHz monitor, and a detachable 85-key ASCII keyboard (which generates all 128 ASCII characters) with proportional-rate joystick.

With a resolution of 1280 x 1024, Lexidata claims that the 2400 is the highest resolution black and white raster terminal on the market. To fight flicker, the refresh rate is 50/60Hz non-interlaced.

The architecture is based around the 68000 μP, which is configured with the video display memory on a single board. The raster memory is part of the processor's address space. Five processor option slots on the board allow upgrading of system functionality. Optional boards can provide additional serial ports and program memory (up to 256K Bytes per option board). In addition, the processor option slots allow OEMs to add peripheral storage devices and customized interfaces.

Configuration of the video display memory allows a unique feature: the division of the screen

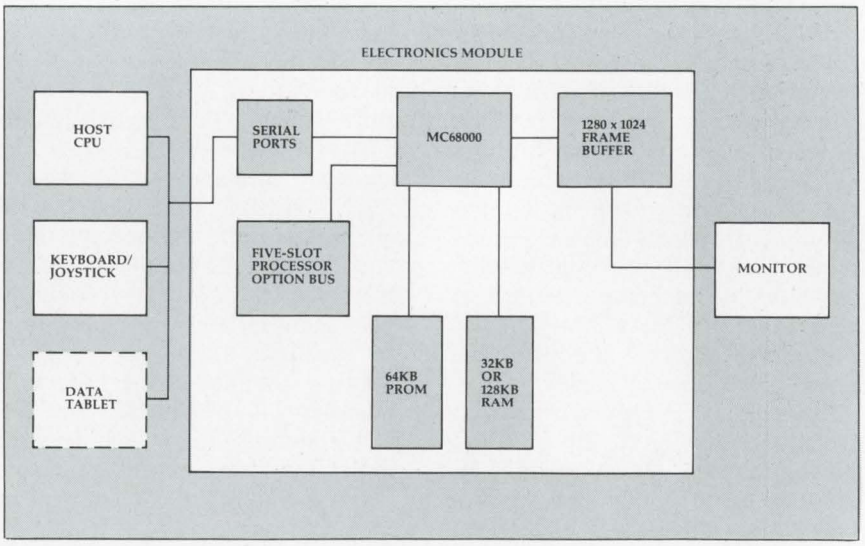

Figure 2: In its basic configuration, the new Model 2400 is comprised of an electronics bay including the MC68000 (64KB ROM/32KB or 128KB RAM), five processor option slots and two RS232 interface ports, a 19″ black and white monitor; and, a detachable, 85-key ASCII keyboard with twelve user-definable keys and an integral, proportional-rate joystick.

into four individual workspaces, each designed to handle specific functions. Each workspace is adjustable in size, and not all four workspaces need be used. Workspace 1 features pan, zoom, and other interactive graphics operations; workspace 4, on the other hand, is a fixed space for logging error messages or annotating keyboard function keys. Lexidata explains that these workspaces enable users to perform interactive graphics, conduct system dialogue, maintain a system select menu and log error messages simultaneously in a single unit.

The 2400 supports two different command formats, one by Lexidata, and the other based on Tektronix Plot-10 code. The Lexidata format is based on an English language command structure. Software architecture is based on 68000 resident firmware and consists of 64Kbytes of PROM and 32Kbytes or 128Kbytes of RAM. This RAM is for downloading user fonts and application software; the PROM contains the operating system.

Lexidata's new terminal is aimed at a variety of distributed graphics applications, especially CAD/CAM. Soon-to-be-announced products will further address the CAD/CAM market, as well as the business graphics and graphic arts markets.

Model 2400 options include an 11″ x 11″ data tablet with ballpoint stylus or four-button puck, and video hard copy.

Prices for the terminal start at $11K, with deliveries 90 days ARO. Deliveries of a color version, which will sell for approximately $20K, are expected before the end of the fiscal year.

Write 197

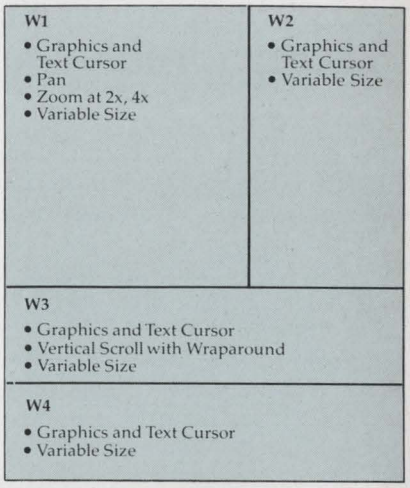

Figure 3: Model 2400's programmable, four-way split screen enables users to select the optimal screen workspace for handling a specific function.

Lexidata
755 Middlesex Turnpike
Billerica, MA 01865

100 mm (3.9 inch) 5Mbyte Winchester Solves Back-Up Problem

As most cartridge disc drive suppliers are quick to say, the true solution to the problem of back-up lies with a removable disc cartridge. The cartridge is identical to the fixed disc it backs up in data format transfer rate, etc. However, its one significant drawback thus far has been media cost. A removable cartridge costs anywhere from $80 on up for either the 5¼″ and 8″ class of drive. Moreover, the drive's unit cost itself is normally higher than the fixed disc drives.

In the past, the solution to reducing the unit cost of the removable cartridge drive has come in the form of combining a fixed and removable drive together so that both share the same spindle. However, this has meant that some functionality is being sacrificed. Data on the fixed portion is not accessible when the removable cartridge is being changed. In addition, since both drives share the same actuator, it is not possible to independently address different tracks on the two drives simultaneously. These devices are also quite expensive.

For storage requirements in the under-40-Mbyte storage capacity range, these back-up problems have been solved by the SQ306, 5-Mbyte, 100 mm removable cartridge drive from Syquest Technology. It provides storage capacity sufficiently great to effectively offload up to 40-Mbytes easily. Moreover, the back-up operation can occur in less time than would be required to do the job with streaming tape drives since 5 Mbytes can be offloaded in under 4 minutes.

The device can fit electrically into any system currently supporting a Seagate Technology or comparable 5¼″ Winchester disc drive with no modifications. In addition, the form factor for the 100 mm cartridge is exactly half the height of a minifloppy drive, hence the package will easily fit into any system containing a 5¼″ hard and/or floppy drive. In fact, the system can contain two 100 mm removable cartridge drives (10 Mbytes of storage) in the same space presently containing a single minifloppy or hard Winchester drive and present many more features/applications to the system user such as the swapping, file compression and seek overlaps.

Write 198

Figure 1: The SQ306 from Syquest Technology offers 5 Mbytes of storage in a 100mm removable cartridge drive.

DEC-Compatible Winchester Has Removable Winchester Backup Cartridge

The removable Winchester Cartridge backup for the Winchester disk drive offers advantages over other backup schemes. These advantages were recently brought together in a 41.6 Mbyte, LSI-11 compatible Winchester disk system from Charles River Data Systems of Natick, MA. This unit, the RLX3010, features a removable-cartridge Winchester drive for on-line storage and backup.

Five key advantages exist: (1) the unit has two independently-operating drives, so that removing one will not halt system operation, (2) the R/W heads are non-removable, saving costs, (3) single-button front-panel diagnostics test the disk separate from the CPU, (4) a second version uses floppy backup for those that prefer it and (5) an optional Q-bus backplane saves space, cabling, power and cost by eliminating a separate processor box.

Describing the unit, Bill Nimee, vice-president of product development at Charles River Data Systems, said, "We think the Winchester-Winchester combination is the best solution to the Winchester backup problem. It combines the reliability and high-density storage of a Winchester with the convenience of removable media."

The new RLX3010 incorporates both an 8″ fixed Winchester with 31.2 Mbyte (formatted) capacity, plus an 8″ removable-cartridge Winchester with 10.4 Mbyte (formatted) capacity. In its 7″ enclosure, the RLX3010 has total capacity equal to four DEC RL02's (which require 42″ of rack space and weigh about 300 lbs).

The RLX 3010 is fully software compatible with LSI-11/23 systems and runs, without software modification, under RSX-11M and RT-11. It also supports 22-bit addressing.

The five advantages, listed earlier, are in more detail as follows.

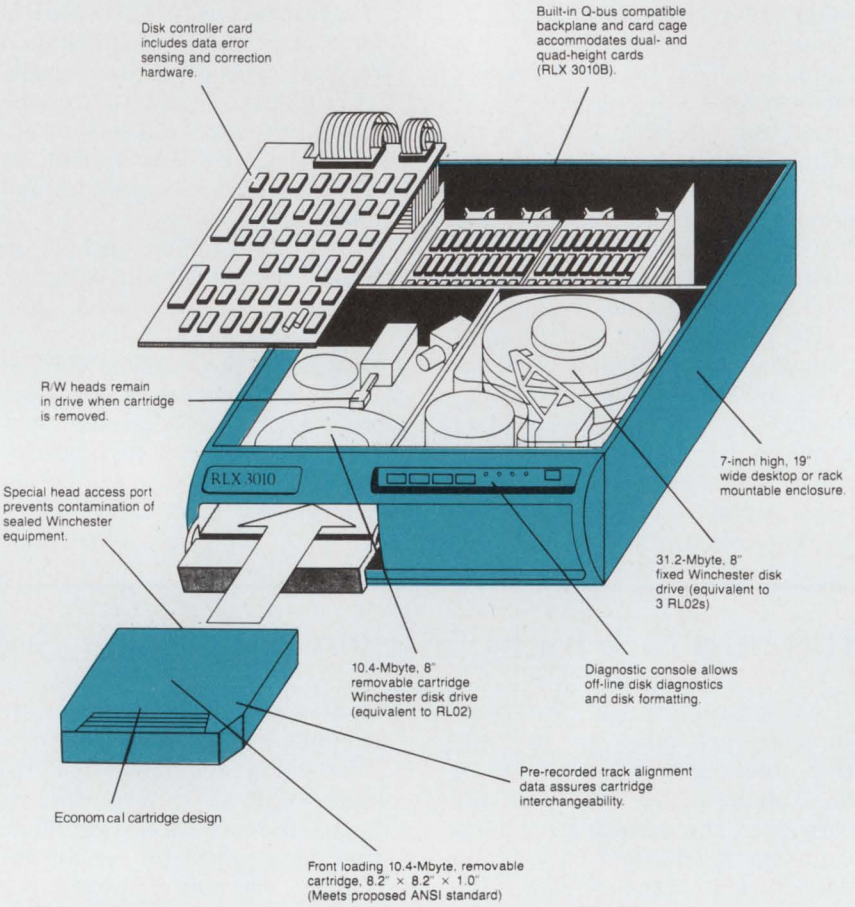

Figure 1: The RLX3010 includes in a 7″ high chassis, a 31.2 Mbyte 8″ Winchester with a 10.4 Mbyte (formatted), 8″ removable Winchester cartridge. Combined, formatted capacity equals that of four DEC RL02s.

First, the two Winchester disks operate independently, with each mounted on its own spindle. The entire 41.6 Mbyte capacity can be used to store programs and data. The removable Winchester can also be used for file-oriented backup and program swapping. Normal production work or programming can continue on the fixed disk while cartridges are mounted or dismounted or while a program is loaded or backup data is transferred to the removable disk.

Second, the removable cartridge loads and unloads through a door in the unit's front panel. R/W heads remain in the disk drive when the cartridge is removed. Because the cartridge does not include expensive R/W heads, it is an economical medium for secure off-line storage of user-proprietary software, off-line database storage or infinite archival storage.

Third, the RLX3010 includes a front panel diagnostic console that allows the disk to be tested independent of the central processor. The user can run diagnostics by pushing a single button. Error messages are displayed by console

indicator lights. The disk can be reformatted from the front panel. Standard DEC disk diagnostics can be used.

Fourth, a second disk system, the RLX3001, was also announced. It incorporates the same 8″ fixed Winchester as the RLX3010, but includes, in place of the removable cartridge Winchester, a 1 Mbyte, RX02-compatible floppy disk drive.

Fifth, a built-in Q-bus backplane is available for both the RLX3010 and the RLX3001, making is possible to mount standard LSI-11 processor, memory and interface boards in the RLX chassis. "The optional backplane lets users package an entire system, including CPU, main memory, and 41.6 Mbytes of disk storage, in a single 7″ box," said Nimee. "It reduces space, cabling, and power requirements, and eliminates the need for a separate processor box, which can save from several hundred to over a thousand dollars per system."

OEM discounts are available. At the quantity ten discount level, the price of the RLX3010 is $9,800. Systems are available for delivery in from 60 to 120 days, ARO, depending on the model. Systems are covered by CRDS 90-day warranty and service program.

Write 200

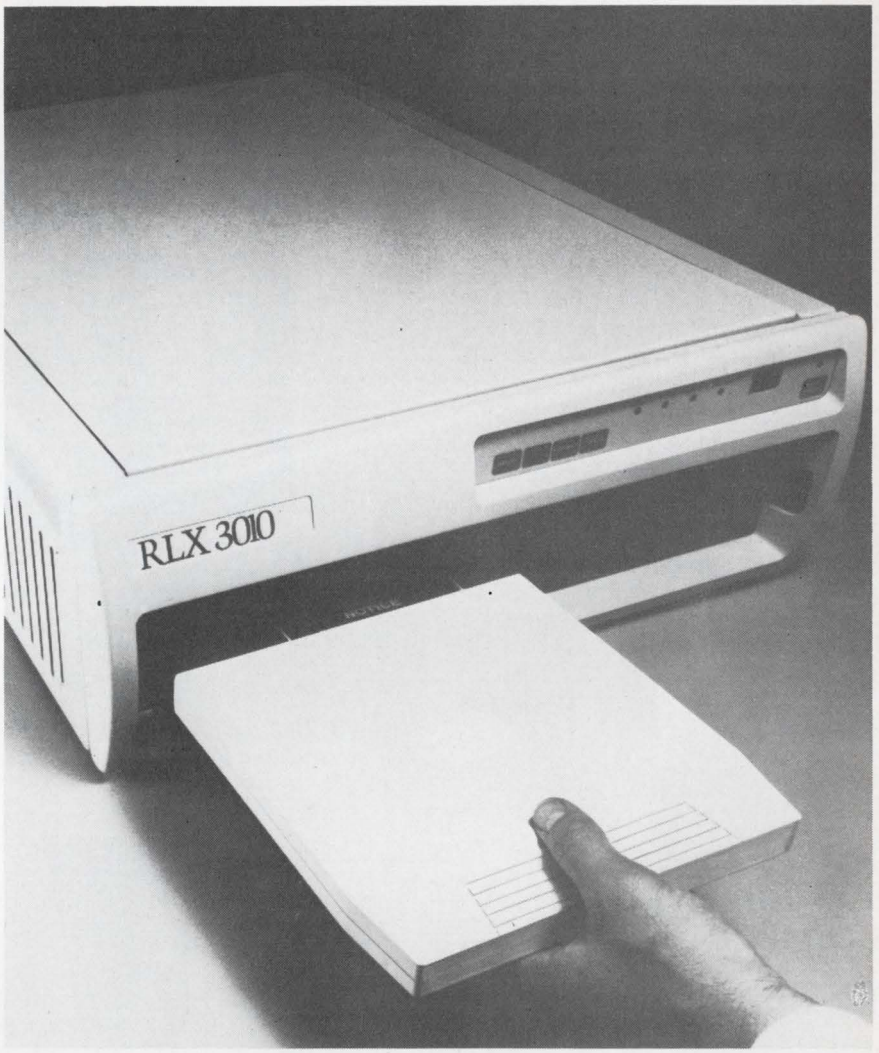

Figure 2: The RLX3010 fixed disk holds 31.2 Mbyte unformatted and 10.4 Mbyte removable Winchester backup. The Winchester cartridge can be loaded while the fixed disk is running. The head remains in the drive.

Card Guide Solves LSI-11 Half-Quad Board Center Support Problems

Sagging, shorting and other possible failure conditions occur when half-quad boards are utilized in LSI-11 full-quad size card cages. To prevent this potentially damaging condition, ADAC of Woburn, MA, has just introduced an exclusive card guide that provides a permanent, mechanically stable solution over clip and spacer devices which transfer support loads from one board to another.

This injection-molded center support device is now standard equipment in the card cage of all ADAC System 1000 and 1000TU LSI-11 bus enclosures and backplane assemblies. The card guide is easily field-modified to accept combinations of full- and half-quad boards. The high-capacity card cages of System 1000 and 1000TU can accept up to 11 full-quad boards and up to 22 half-quad boards or any combination thereof with the new card guide. Top and bottom screws assure continued rigidity and proper vertical spacing even if the card guide has been cut to accept full-quad boards.

Large horizontal slots in the card guide permit unimpeded air

flow across the cage. A full-height flange on the guide snaps firmly into the backplane for positive positioning of support tracks in relation to PC connector strips.

The tilt-up card cages can now be locked in full vertical as well as traditional 30° position. The cage cooling fan and baffle assembly is now mounted on the tilt-up cage of all current production System 1000 units as it has been on all System 1000TUs. Proper cooling is maintained during start-up and system diagnosis when operating with the card cage in an up position.

Factory-wired 22-bit addressing is now an optional extra for both System 1000 and System 1000TU backplanes. The new card guide is standard at no extra cost. List price is $15.

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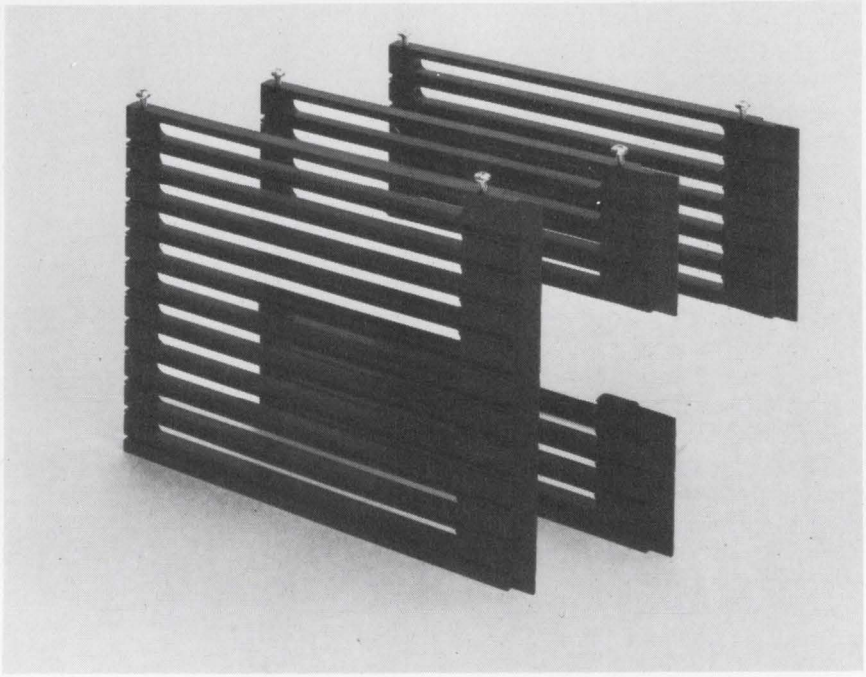


Figure 1: Half-quad panels or cards in card cages designed for full-quad cards can lead to structural problems that these board center supports can prevent.

ALIGNMENT PROGRAM

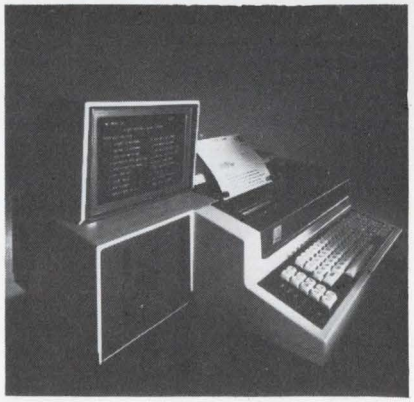
Measures Floppy Disk Head Alignment

Without the use of oscilloscopes or other test equipment, an operator can verify alignment of his 5¼" and 8" floppy drives in minutes to save time in set-up and test. Data interchange assurance can also be achieved with this test. Merely by using ADC's familiar two letter mnemonics, the user can perform all available tests. Operation consists of three simple steps: boot the appropriate ADC system diskette, insert a Digital Diagnostic diskette into the drive to be tested, and issue the appropriate commands via the system console. The complete package consists of a system diskette, manual, and the diagnostic diskettes required for the system. **Applied Data Communications,** 14272 Chambers Rd, Tustin, CA 92680. **Write 185**

DESKTOP COMPUTER

Fully Integrated System With Winchester Disk

The 900 offers up to 15MB of on-line storage. An auxiliary fixed disk is also available to add about 7 or 14MB of capacity. The 900 features a keyboard, printer, CRT and disk drives integrated into a system not much larger than a typewriter. For data processing and internal correspondence, it provides bidirectional dot-matrix printing at up to 200 cps. The



900XR has a dual mode printer. In addition to its data processing capabilities, it can be switched to a high resolution mode to produce letter-quality documents. The 900 stores a variety of type styles and sizes in memory. Foreign language characters and special fonts can also be created or modified. **Durango Systems,** 3003 N. First St., San Jose, CA 95134. **Write 190**

CP/M-BASED COMPUTER

Provides Low-Cost Entry Into The HiNet Local Area Network

The DSC-3/F desktop system combines in one portable, 30 lb. unit the DSC-3 (Z-80A) processor, a 9" diagonal CRT, two 5¼" single- or double-density, double-sided floppies (formatted capacity of 307.2 kB/drive), the network interface, 4 RS-232C ser-

ial ports, and two 8-bit bidirectional parallel ports with status lines. The system, which provides 64 kB of RAM and 1 kB of ROM, has an access speed of 250 ns, with no wait states. It includes application software for payroll, general ledger, accounts receivable and accounts payable. DMS also offers Wordstar or Select for word processing, Selector V or dBMS II for data base management, and Microplan for financial budgets and finance. Programming languages include Basic, Cobol, PL/1, Fortran, and Pascal. When a multi-user system is required, the Fox can serve as a workstation or the master station in the HiNet local area network. $3995, qty discounts avail. **Digital Microsystems,** 1840 Embarcadero, Oakland, CA 94606. **Write 191**

COMPUTER SYSTEMS

Nova Compatible

The Series 4000 features a full 16-bit minicomputer with up to 128 Kbytes of memory on a single-board CPU, DG NOVA equivalent instruction set, fast instruction execution, extended instructions, standard or high-speed data channel, memory parity check, battery back-up, front-loading 6-slot chassis with jumper-free back plane and separate power supply. The system runs under IRIS, IOS, BITS, BLIS/COBOL or VMOS operating system software. The Series 5000 includes all of the features of the Series 4000 with memory capacities of 256 kB and 512 kB. Should more memory be required in either Series, Model 300 can be added. This is a Megamite solid-state, fixed-head disk emulator. The Megamite is available in 3 capacities—256 kB, 512 kB and 1024 kB, and can dramatically increase the system throughout by effectively eliminating disk-swapping overhead and normal seek/rotational latency of the disk I/O. Series 4000 is $6000; Series 5000, 256 kB system is $8250; and the 512 kB system is $10,340; OEM discounts avail. **Bytronix Corp,** 2701 E. Chapman Ave, Fullerton, CA 92631. **Write 186**

MINICOMPUTER SYSTEMS

768 kB of Executable Address Space and High Density Memory

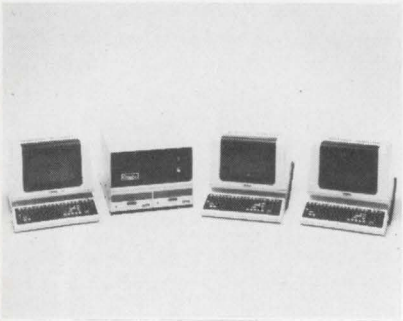
The H80-1A and H100-1A are based on a new CPU with an 18-bit program counter. This allows them to run programs with up to 768 kB of executable code per user, four times the maximum of their forerunners, the H80 and H100. Like the H80 and H100, the new models support up to 32 concurrent interactive users, include 6,144 kB of virtual memory and address up to 768 kB of real memory. Designed around a system bus capable of an aggregate transfer rate of 19 MB/sec, the systems' central processors overlap instruction fetch with execution. They also feature error-correcting main memory and an optional hardware floating point unit. The H100-1A combines the processing power of the H80-1A with a flexible I/O structure for interfacing bulk storage devices and other peripherals to its system bus. Both support up to 24

logical I/O channels. Using the new VOS operating system, the new models offer users the benefit of concurrently supporting multi-stream batch processing, interactive time-sharing and real-time processing modes. The H80-1A is $44,950 and the H100-1A is $55,000. For current H80 and H100 users, a field upgrade package is available for $9500. **Harris Corp,** 2101 W. Cypress Creek Rd, Ft. Lauderdale, FL 33309. **Write 195**

MULTI-USER OS

Runs 8-Bit/16-Bit Programs Simultaneously

A proprietary implementation of the Digital Research MP/M 86 operating system, MP/M 8-16 utilizes CompuPro's 8085/8088 CPU card and features 62 Kbytes of user program space for 8-bit CP/M 2.2 compatible software.



It is designed to perform both single-user and multi-user functions while running any combination of CP/M 2.2 or CP/M 86 compatible applications software for as many as 8 users. Users who have a substantial library of applications software will now be able to protect their investment and meet future requirements for the more powerful 16-bit programs. For creating or running 16-bit CP/M 86 compatible software, standard 8-bit programs such as editors and database managers can be used to supplement future applications programs. In addition, 8086 software development is provided through a wide range of cross assemblers and 8080/Z-80 to 8086 translators. MP/M 8-16 is $995. **CompuPro,** Oakland Airport, CA 94614. **Write 188**

COMPUTER SYSTEMS

Desk and Cabinet Models

The Series 5200 Desk Model and Series 5300 Cabinet Model are both Winchester-based systems with 64 kB of main memory storage that is expandable to 256 kB. The basic 5200 also includes a CPU, one 1.23MB flexible disk drive, a CRT terminal and a 24MB Winchester disk drive. A 32MB Winchester is also available. It can support two 32MB drives for a total capacity of 64MB. A maximum of 10 CRTs can operate on the 5200 system. Under $22,000. The basic 5300 features 64 kB of main memory, a CPU, one 1.23MB flexible disk drive, a CRT terminal and a 24MB Winchester drive. It can support up to three 32MB Winchesters for a total capacity of 96MB and supports up to 20 CRTs. $24,000. A variety of matrix printers and line printers, as well as a character printer for word processing, are available, **Centurion Computer Corp,** 1780 Jay Ell Dr, Richardson, TX 75081. **Write 189**

BOARD-SET COMPUTER

Designed For The OEM Market

The QUADRABYTE 32-bit board-set computer is specifically targeted at graphical analysis, numerical control, data communications, test and measurement, CAD/CAM, factory automation, and energy applications. It consists of a 32-bit CPU, an I/O processor, and an integrated memory module with either 512 Kbytes or 1 Mbyte of ECC MOS Memory. The CPU is capable of executing up to 660 K Whets/sec. Systems with up to 16 Mbytes of memory can be configured by the OEM for his particular application. Under $14,000 in OEM qty. 100. **Gould S.E.L.,** Computer Systems Inc, 6901 W. Sunrise Blvd, Ft. Lauderdale, FL 33310. **Write 194**

32-BIT SYSTEMS

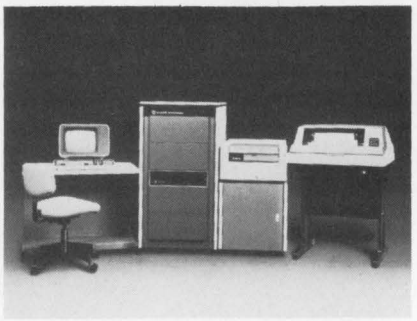
Two New Desktop Models

The Universe 68/15 incorporates a 32-bit central processor, 256 kB of main memory, and a 16MB disk, housed in a 14″ high package. Base price is $19,200; $12,480 in qty. 20. The Universe 68/17 is identical to the 68/15, except that it includes 512 kB of main memory on a single card. It can be expanded to 2MB in a 7″ high cabinet. Base price is $21,200. Both models are fully compatible with previously announced Universe 68 systems, and support UNOS, a UNIX-like operating system. Languages supported are Fortran, Basic, C, and Pascal. **Charles River Data Systems,** 4 Tech Circle, Natick, MA 01760. **Write 187**

MINICOMPUTER FAMILY

Improved Price/Performance

The Series 900 is the basic element of a long-term growth plan in the industrial automation and commercial systems marketplace. Through scheduled releases, including Pascal and 'C' language compilers under Control and UNIX System III, customers can use the Series 900 as a bridge to migrate their investment in software to even more powerful systems as they become available. Features include: bit-slice processing for implementation of existing instruction sets and software compatibility; gate array logic chips which increase overall system reliability; and optional cache memory that improves system throughput. Users can select from 14 distinct con-



figurations of the five basic models. These can be expanded with additional main memory, cache memory and cabinetry. From $6995 to $20,950. **General Automation Inc,** 1055 South East St, PO Box 4883, Anaheim, CA 92803. **Write 193**

IMAGE PROCESSING

Software For DEC And Unix Operating Systems

The IPEX package includes both "single cycle" and "high level" subroutines that call on basic, low level subroutines from Grinnell's standard Fortran package. The basic Fortran package, which is available with device drivers for most DEC operating systems, and some others, gives users full access to all display functions of Grinnell systems without the need for machine language programming. IPEX expands this capability and allows users to perform complex image processing tasks, including both point and spatial processing functions. Images can be partitioned into processed and unprocessed areas through use of a spatial area mask and/or an intensity table transformation. Single cycle, logical and arithmetic routines are included for multiple image operations. Most operations are performed in 1/30th second for complete $512 \times 512 \times 8$-bit images. Basic Fortran Subroutine/Device Driver Package is $500, plus $500 for the IPEX Extension. **Grinnell Systems Corp,** 2159 Bering Dr, San Jose, CA 95131. **Write 192**

When You Need . . .

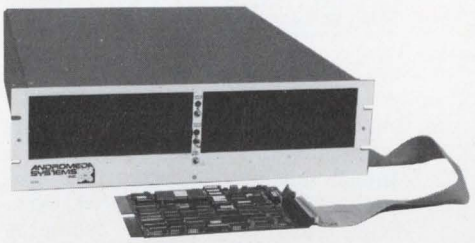
WINCHESTER DISK SYSTEMS

FOR THE Q-BUS

ADD-ON SUBSYSTEMS

MWDS

WDS



RPX60

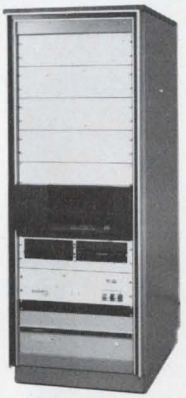
5-1/4″ DISKS

11/M-W

8″ DISKS

11/B-W

14″ DISKS



11/B-WTS

FULL TURNKEY COMPUTER SYSTEMS

. . . think of Andromeda

Andromeda Systems, Inc. offers the Q-Bus user a wide selection of Winchester disk based mass storage systems. Both add-on subsystems and full turnkey computer systems are available. Current storage capacities range from 2.5mb to 160mb. The Winchester disk controllers emulate DEC RK-05, RL-01/02, and RP-02/03 devices for compatibility with existing operating systems. Winchester disks in 5¼″, 8″ and 14″ formats are used to obtain the best possible performance in a variety of package sizes.

Back-up is to floppy disk or streaming magnetic tape. The 5¼″ and 8″ systems may be specified with an intregral floppy disk drive; these systems use the Andromeda WDC11 controller that includes an RX-02 emulating floppy disk controller on the same dual-width card. Also available for backup is a separate, high performance, non-emulating floppy disk controller, the DFDC11/DMDC11. This proprietary controller offers 25 to 61 percent more storage along with a data transfer rate 2.25 times faster than the RX-02.

We offer a complete line of Q-Bus based systems and other LSI-11 related products. For details, contact:

ANDROMEDA SYSTEMS INC.

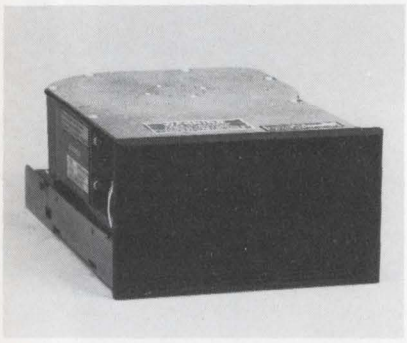
9000 Eton Ave.
Canoga Park, Calif. 91304
Phone: 213/709-7600
TWX: (910) 494-1248

Write 23 on Reader Inquiry Card

5¼" WINCHESTER DRIVES

From 6.7 To 26.7 MB Unformatted Capacity

The enhanced Pyxis Series is available in four models: Model 7, a single-disk device with 6.7 MB of unformatted capacity; Model 13, a two-disk device with 13.3 MB; Model 20, a three-disk device with 20.0 MB; Model 27, a four-disk device with 26.7 MB. Average access time, including head settling, is 90 ms with a data transfer rate of 5 Mbits/sec. Recording densities are 360 tpi and 8,800 bpi providing 10,417 bytes/track on 320 cylinders. The interface, form factor, mounting and power requirements are all compatible with 5¼"



Winchester industry standards. All models feature dual front panel status indicators, a fail-safe spindle brake, automatic sensing of the step pulse rate, temperature-compensated head positioning, and require just 27W of DC power. The closed-loop recirculating air system between chambers assures contamination-free operation. From $680 to $1280. **Ampex Corp,** 401 Broadway, Redwood City, CA 94063. **Write 155**

8" WINCHESTER

16 MB Removable and 32 MB Fixed Storage

The C8048 meets the high capacity, high performance requirements of large business systems, multi-terminal word processing, multi-functional office systems and larger, general purpose minicomputers. An embedded servo on the removable media improves signal to noise performance, which in turn allows greater data storage capacity. To control the heat in the drive a ventilated spindle evenly disperses air over the drive's disks, thus balancing temperatures, reducing off-track error, and improving data integrity. Additionally, because each sector contains track positioning information, shifts in track positioning due to head nonalignment and thermal effects are virtually eliminat-

ed. Fail-safe mechanisms such as one which allows the drive to power up only after the cartridge is properly seated, are provided to assure operational reliability. **Century Data Systems,** 1270 N. Kraemer Blvd, Anaheim, CA 92806. **Write 156**

BUFFERED TERMINAL

For Portable And/Or Remote Communications

The TransTerm 2 consists of a single line 80 character liquid crystal display and a 58 key TTY style membrane keyboard packaged in a 1.75" high by 12.75" wide by 6.9" deep case. The unit communicates in full duplex RS-232 series async ASCII with 20 mA current loop or RS-422 available as options. One of 8 baud rates (110-9600) can be switch selected as can the character parity (even/odd/mark/space) at 7 data bits per character. Memory capacity holds 24 lines of displayed data which can be locally viewed under operator control. Three switch selectable operating modes provide teletypewriter compatibility, a block send mode, or multidropped/

polling operation (up to 32 units). Optional features include expanded data memory of up to 12K bytes, a 40 column A/N printer, and battery powered operation. $549. **Computerwise Inc,** 4006 E. 137th Terrace, Grandview, MO 64030. **Write 157**

ENCRYPTION/DECRYPTION

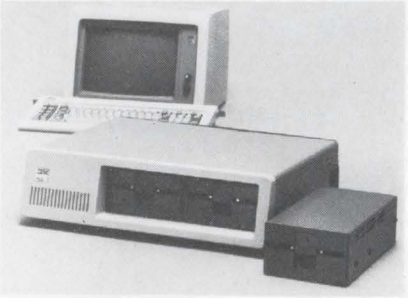
High Speed S-100 Board And Software

Encryptor is an encryption/decryption unit employing an S-100 compatible board. Featuring programmed I/O for key, data, commands and states, it provides supporting software for CP/M , MP/M and OASIS systems, and takes only 25 ms to encrypt or decrypt 8 bytes. Allowing for the security of microcomputer data, it represents an effective method of protecting the confidentiality of sensitive files, whether stored or in transmission. Data may be secured on any system equipped with the encryptor (and supporting software) and may be sent to any compatible system. $395. **Data Star Ltd,** 9700 Fair Oaks Blvd, Suite G, Fair Oaks, CA 95628. **Write 158**

DISK STORAGE

For IBM Personal Computers

Expanded disk drive storage for the IBM personal computer, including the first double sided drives that provide up to 672K bytes of formatted storage (dual drive system), is avail-



able. They can be installed as internal drives, using the IBM cabinet and power supply, or can be added as an external drive with cable, cabinet and power supply included as part of the drive assembly. The models include a single sided drive with 168K bytes of formatted storage and a doubled sided drive with 336K bytes. Combinations possible include two double sided drives internally for 672K of formatted storage; two single sided drives internally; two single sided drives or one doubled sided drive externally; or, two single sided drives internally with a double sided drive externally. From $470 to $670, qty. **Interface Inc,** 20932 Cantara St, Canoga Park, CA 91304. **Write 162**

FLOPPY DISK

Compact 3″ By 4″ Unit

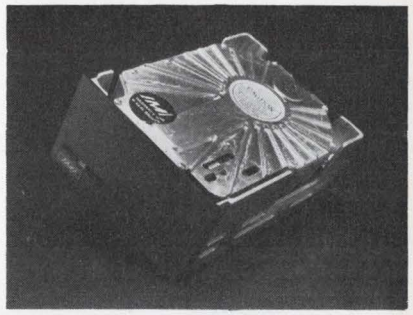
Hitachi Maxell, Hitachi and Matsushita have made a joint announcement of the establishment of a technical standard for a new compact floppy

disk. It will be used in disk drive systems that are compatible and interchangeable with conventional floppy disk drives. Capacity is 125K bytes for the single sided, single density version and 500K bytes for the double sided, double density type. The companies believe that this new standard for a 3″ compact floppy disk will be adopted by many computer hardware manufacturers, and expect that various disk drives using this new 3″ disk will begin to appear in the marketplace toward the latter part of 1982. **Maxell Corp,** 60 Oxford Dr, Moonachie, NJ 07074. **Write 163**

5¼″ WINCHESTERS

New Design With 2-Piece, Shock Mounted Chassis

The new drives, offered initially in 12.76 and 19.14 MB capacities, are ST 506 compatible and offer the latest in data integrity under a wide range of operating environments. The 2-piece chassis with shock resistant design reduces the chances of head or media damage from external sources, and isolates the drive mechanism from distortion transferred from the chassis during mounting. Increased data reliability is achieved by utilizing plated disk media that is harder and more durable than the more commonly used oxide coated media. Plated media also makes it possible to increase data density in the future,



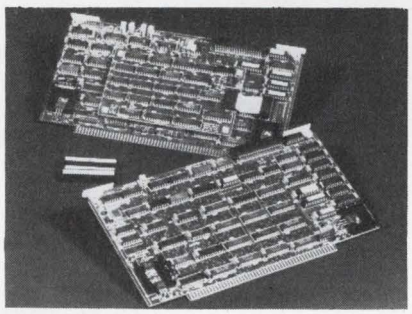
since it allows optimized head flying heights and maximized areal density. Advanced thermal design allows accurate head positioning (and therefore reliable data transfer) under a wide range of operating conditions. **International Memories Inc,** 10381 Bandley Dr, Cupertino, CA 95014. **Write 161**

COMPONENTS

ETHERNET CONTROLLER

For S-100 Bus Users

The two board controller set conforms to the Ethernet specifications and comes with either 16K or 64K of



dual ported memory. The buffered memory can handle either 8 or 32, 2K byte message packets arriving at 9.16 μsec spacing. With memory mapping, dynamic address recognition and four levels of interupt, the controller is designed specifically to eliminate any overhead on the S-100 bus associated with processing Ethernet packet data on 10 Mbits/sec. Intended for a wide range of office automation and distributed processing applications, the Filtabyte 2.0 Ethernet controller boards, are $1295 in OEM qty. **Perex, Inc.,** 1798 Technology Dr, San Jose, CA 95110. **Write 136**

300-GATE ARRAY

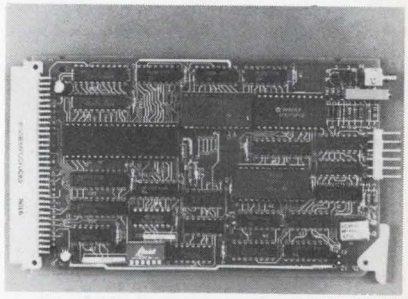
Configurable Schottky TTL Array

The CGA 300 features include dual-layer metalization, 6 ns typical gate propagation delays, and 56 maximum I/O buffers. The device is available in ceramic dual-in-line packages or leadless chip carriers as standard packaging selections. Special customer screening and MIL-STD-883, Classes B and S are also available. Flexible development interfaces are offered. The customer may input a logic diagram, critical timing path definitions and a truth table and Raytheon does the rest of the development. Or, the customer may perform placement, routing and digitizing from furnished array design specification and Raytheon implements the circuit design. Then, 25 assembled and tested prototypes are supplied. **Raytheon Semiconductor,** 350 Ellis St, Mountain View, CA 94040. **Write 137**

CRT CONTROLLER

Joins Rockwell RM 65 Board Family

The RM65-5102 CRT controller module (CRTC) generates upper and lower case alphanumerics and semigraphics. It includes an R6545-1 device for timing and control, 4K ROM character generator, 2K ROM firmware to configure format and handle data, and a 2K refresh RAM. The module outputs HSYNC, VSYNC and video signals and composite video. It operates to NTSC (60 Hz, 525 lines) and European (50 Hz, 625 lines) raster formats. 5 × 7 dot matrix characters are generated in a 7 × 10 field and configured into displays in 6 formats, ranging from 40 columns by 16 lines to 80 columns by 25 lines.

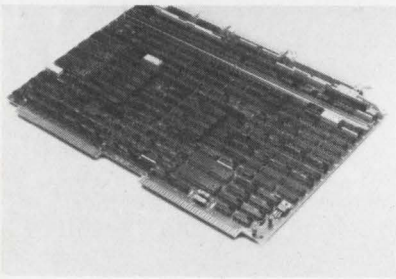


The module is RM 65 bus compatible, intended for use in 6502-based RM 65 board-level systems. It also can be used as an expansion of the AIM 65 and AIM 65/40 microcomputers. The RM65-5102E is $250, qty discounts avail. **Rockwell International,** 3310 Miraloma Ave, Box 3669, Anaheim, CA 92803. **Write 138**

DISK/TAPE CONTROLLERS

For TI 990 Minicomputers

The SPECTRA 16 disk controller and the multifunction SPECTRA 26 and SPECTRA 46 controllers that eliminate the need for separate disk and tape controllers are available. The SPECTRA 16 supports SMD drives with transfer rates as high as 2MB/sec, and the dual bipolar μP architecture of the SPECTRA 26 and SPECTRA 46 can additionally support streaming tape drives with transfer rates of up to 320KB/sec. The SPECTRA 16 has on-board 32-bit ECC to correct burst errors up to 7 bits in length transparently in the control-

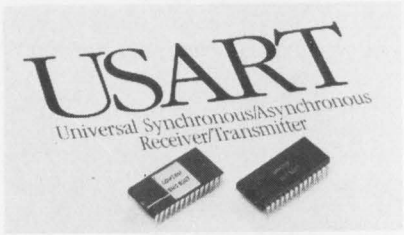


ler's buffer. Four sector (1,024 byte) data buffering eliminates "data lates" and allows multiple sector transfers up to 64K bytes. $2800 (qty 50). The SPECTRA 26 offers simultaneous control of 4 SMD disk drives and 8 formatted ½" tape drives without modifying operating system software. The SPECTRA 46 offers simultaneous control of 4 SMD disk drives and 4 Archive/Cipher formatted ¼" tape drives. The controller also provides low-cost back-up of Winchester disk drives with economical ¼" tape media. $3300 (qty 50). **Spectra Logic Corp,** 1227 Innsbruck Dr, Sunnyvale, CA 94086. **Write 139**

COMMUNICATIONS USART

USART and Programmable Baud Rate Generator On One MOS/LSI Chip

The COM 2661 interfaces μPs or μCs to data communication links or peripherals. It accommodates all standard async formats and all standard character-oriented sync formats such as IBM's BiSync. Features in the async mode include programmable character formats, programmable clock rates, on-chip line break detection and generation, automatic serial echo and two loop-back modes. Character formats are programmable in the sync mode. In addition, the COM 2661

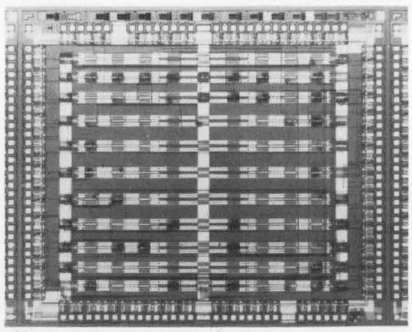


may operate in both transparent and non-transparent modes with automatic SYNC insertion and stripping. Available in 28-pin packages, $10 in plastic and $32 in ceramic in 100 qty. **Standard Microsystems,** 35 Marcus Blvd, Hauppauge, NY 11788. **Write 140**

SCHOTTKY ARRAYS

Feature 1000 or 2000 Auto-Routable Gates

The TAT010 and TAT020 are fabricated with 2-micron design rules using Advanced Schottky transistor logic (ASTL) technology. Both devices have typical internal-gate propagation-delay times of 1ns, with a typical power dissipation of 300 microwatts per gate. Both also have a large number of I/O buffers—88 on the TAT010 and 120 on the TAT020—which allows them to be interfaced to a wide range of circuits. These include: +5V TTL, +3V TTL, −2V 10K ECL, and +5V to −5.2V STL to ECL translators. Up to 80 logic

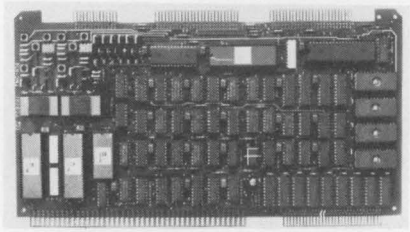


combinations of I/O buffers are possible in a single I/O cell. The two logic arrays also feature a fully isolated array ground and external ground. **Texas Instruments Inc,** SC-370, PO Box 202 129, Dallas, TX 75220. **Write 141**

NUMERICAL CONTROL BOARD

Eliminates Development Of An Interpolation Algorithm

Model TNC102 provides precise X and Y axis control signals by direct monitoring of an IEEE 796 Multibus. Applications include numerical control, robotics, plotters and industrial instrumentation and control systems. It accommodates both linear and circular interpolation (parabolic, logarithmic, and exponential are optional). By not requiring development of an interpolation algorithm, there is much less software development and less debugging time. The system is directly pin compatible to Intel Multibus. The TNC102 comprises an 8-bit

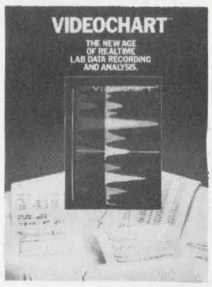


μP, interpolation pulse generator, X-Y comparison controllers, and X-Y D/A convertors. **Toko America Inc,** 5520 W. Touhy Ave, Skokie, IL 60077. **Write 142**

SPEECH SYNTHESIZER

Unlimited English Vocabulary

The speech synthesizer board converts ASCII coded text into immediately intelligible, clearly enunciated speech output. The proprietary synthesis-by-rule firmware, resident on the PROSE 2000, allows words and sentences to be spoken with human-like intonation by simply inputting the text representation. When attached to a host computer, arbitrary text messages stored on the host can be downloaded and spoken to communicate instructions, status and alarms. Messages may be changed, updated, or modified on an on-going basis without concern for the vocabulary capability; there are essentially no vocabulary restrictions. The PROSE 2000 board is Multibus compatible and is equipped with an RS232C serial port. An 8086 μP, single chip PDSP formant synthesizer and 108 kB of memory (EPROM and RAM) are used to produce spoken English in real-time at rates up to 250 words/minute. Additional on-board circuitry performs data I/O, D/A conversion, and audio amplification to directly drive a loudspeaker. Available in a single Multibus-format board and a peripheral which packages the board in an enclosure with a power supply and appropriate connectors. The PROSE 2000 board is $3500, the PR2020 peripheral is $4800. **Telesensory Speech Systems,** 3408 Hillview Ave, Palo Alto, CA 94304. **Write 143**



Realtime Recording And Analysis System.

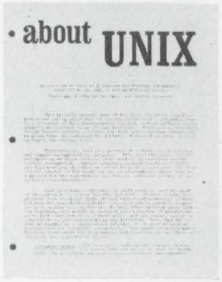
This 6 pp. brochure describes the capabilities of the VideoChart Recorder, a user-interactive data acquisition, manipulation and display instrument for research and development labs. The literature includes information on system features such as a recording range of 100,000 to 1 which virtually eliminates the need to rerun samples, all-electronic recording, and integrated digital/graphic data display. It allows direct comparison of two recordings side by side, superimposed or subtracted from one another.

Instrumentation Graphics **Write 259**

Data Communication Devices.

This catalog brings together over 200 items specifically designed for today's data communicator. Detailed product descriptions and photos (with prices) bring the store to the shopper for convenient ordering. Included are 3 models of IBM compatible protocol converters, and a new programmable communication adapter.

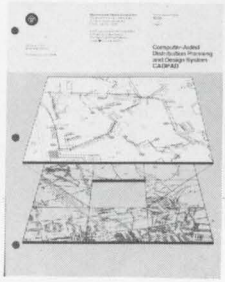
Black Box Catalog **Write 251**



Unix Overview.

This 4 pp. bulletin on Unix and related computer operating software has been compiled by Uni-Ops, a user group. Intended primarily for potential Unix users, the bulletin briefly outlines the systems' technical fundamentals, then lists 20 sources for further information on various aspects.

Uni-Ops **Write 273**



Distribution Planning.

The 16 pp. booklet covers application and benefits of CADPAD. Long-range and short-range distribution planning concepts are presented. Application and features of load forecasting are described since it is considered the foundation of distribution system planning. A brief case study highlights the key advantages of the CADPAD system over traditional approaches to distribution planning and design.

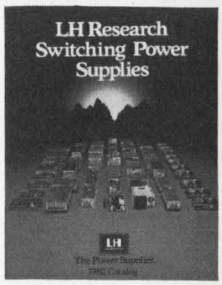
Westinghouse Electric **Write 274**

SIPMOS Power FET Transistors.

The 42 pp. brochure discusses product applications and configurations. Detailed technical data, absolute maximum ratings, electrical characteristics, dynamic parameters, thermal characteristics and inverse diode characteristics, for each device is also included. SIPMOS transistors are suitable for power electronics as power switches in motor control or ultra-sonic generators; and in data processing as a power stage in printers or stepping motor control.

Siemens **Write 270**

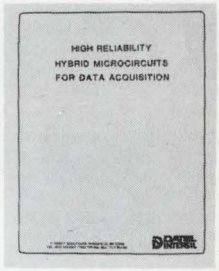
Full Switcher Line.



Containing a complete range of standard, off-the-shelf switching power supplies, the 52 pp. reference includes: a comprehensive specification chart, covering in detail the performance specs on the company's six separate lines of supplies; a Selection Guide Matrix, illustrating product availability by power, voltage and amperage, in from one to seven outputs; and electrical specifications and detail model selection information on its six switcher series. Complete mechanical drawings and specifications are also included, along with detail information for modification or custom design of switching power supplies.

LH Research **Write 261**

High Reliability Processing.



This 12 pp. brochure, High Reliability Hybrid Microcircuits For Data Acquisition, details high reliability processing for military standard components. It includes information on high reliability screening procedures, qualification testing, military specifications, MIL-STD-883B screening and test procedures and ordering information. A hybrid assembly flow chart for high reliability processing is also included.

Datel Intersil **Write 254**

DC-DC Converter Catalog.

This 8 pp. catalog details the electrical and mechanical parameters on DC-DC Converters. The brochure is a complete presentation to the design engineer. Detailed specifications on Power General's DC-DC Converters are presented in tabular form and includes complete case, pin and socket configurations.

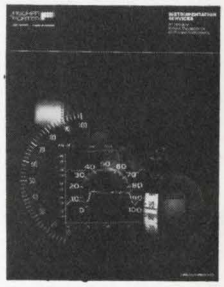
Power General **Write 265**

DC/DC Converters.

The 2 pp. technical data sheet provides product descriptions, applications information, and electrical/mechanical specifications on the EM900 Series of low-cost, semi-regulated DC/DC converters. Includes photos, features, and dimensional drawings. The EM900 Series consists of 10 single and dual output models providing DC outputs of 5, 12, 15, ±12, or ±15 volts from inputs of 5VDC or 12VDC.

Power Products **Write 267**

Instrumentation Services.



The 8 pp. brochure describes the range of instrumentation services available from Fischer & Porter. Plans cover installation service, calibration and commissioning, startup and operation, demand service, training-instrument system maintenance, and contract maintenance service. Advantages of each plan are given so the user has a basis for selection. Catalog No. 91FS.

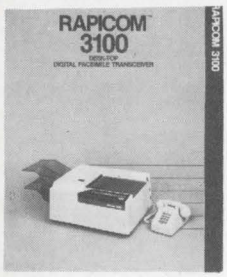
Fischer & Porter **Write 255**

New Literature

9520 Software Development System.

The 9520 is designed to work on its own or in conjunction with the 9508 MicroSystem Emulator for developing 8-bit μP-based systems or the 9516 MicroSystem Integration Station for developing 8 and 16-bit μP-based systems. It offers a unique multitasking capability which allows users to manage as many as three separate functions simultaneously. Catalog, 22 pp.

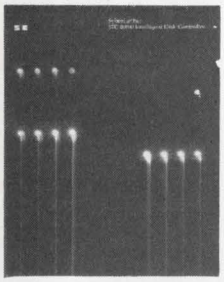
Millennium Systems **Write 263**



Desk-Top Digital Facsimile.

Benefits and features are explored in two brochures that also provide specifications on the Rapicom 3300 and 3100 desk-top digital facsimile transceivers, which are low cost units capable of transmitting the contents of a standard size document at high resolutions in 45 seconds.

Rapicom **Write 268**

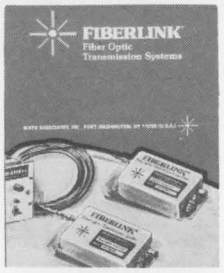


8890 Intelligent Disk Controller.

Describing the solid-state cache and disk controller, this 6 pp. brochure looks at today's complex computing environment and the I/O bottlenecks that result from the disparity between processor speed and disk response time. It explains how Sybercache solves these problems, slashing I/O response as much as 75% by eliminating deficiencies in the communication path between host and disk.

Storage Technology **Write 269**

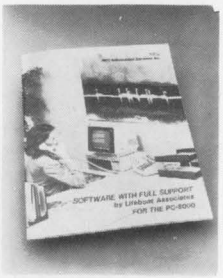
Fiber Optic Systems.



This 24 pp. catalog describes a comprehensive line of fiber optic transmission systems. Analog, digital, video, RS-232, audio and a host of other systems, along with a wide range of compatible optical fibers and cables are also described.

Math Associates **Write 262**

PC-8000 Software.



"Software with Full Support by Lifeboat Associates" presents over 100 application packages for the NECIS PC-8000 personal computer. The 10 categories include System Tools, Telecommunications Languages, Data Management, and Office Aids. The 15 pages of listings also offer packages for Medical, Dental and Insurance offices as well as other specialized vertical application areas.

NEC Information **Write 264**

Wire Switch Brochure.

The 4 pp. brochure describes in detail the fostering of a new type of low-profile rotary switch for OEM's and end users. Its unique form C contact arrangement supersedes all other types of switches and virtually eliminates contact bounce. It is a low profile configuration designed for PC board mounting. The brochure includes actual size photo to give OEM's a clear design definition for sizing and packaging.

Porta Data **Write 266**

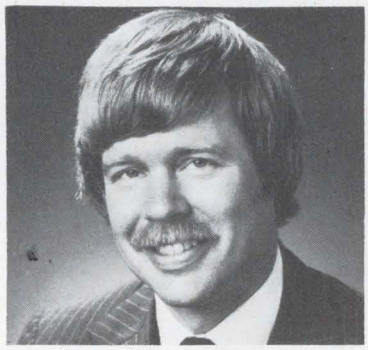
Advertiser Index

Will FTM Keyboards Dominate The 80s?

Full travel membrane (FTM) keyboards/pads have been proposed as a solution to one of the biggest obstacles confronting membrane keyswitches: lack of true tactile feedback. But, are FTM keyswitches as great as many (particularly those who manufacture them) claim they are? To get the answer to this question, *Digital Design* asked several industry spokesmen what they thought. Here are their observations.

No Single Keyboard Technology Will Dominate The 80s

by John C. Overby
Advanced Input Devices, Coeur d'Alene, ID



One must first understand that there are two basic functional types of keyboard products: limited-travel (also called micromotion) and full-travel (conventional typewriter looking). The limited-travel markets will be dominated by dome-switch and flat panel membranes (FPMs). Both of these provide unique packaging, human factors and cost structures not available in full-travel technologies.

The full-travel markets will be dominated by two technologies, capacitance and full-travel membrane (FTM). The FTM will win over capacitance in "wired-only" (non-encoded) applications and where rugged environments are predicted. The capacitance will lead in applications for detachable keyboards where encoding in either a serial or parallel mode is preferred.

Like any new technology, FTM will slowly build in popularity in the same manner as did capacitance during the late 70s. Many leaders in FTM will be newer companies that have no "axe-to-grind" with previous technologies that are rapidly becoming too expensive for mainstream applications.

Significant Growth Through The 80s

by Jack L. Tucker
Oak Switch Systems Inc, Crystal Lake, IL

Full travel membrane keyboards combine the industry-standard, human-engineered touch and feel of full travel key design with proven, highly reliable membrane switch technology, providing users with a price/performance combination unmatched by any other type of keyboard. For example, FTM keyboards can provide a higher than industry standard life expectancy (up to 100 million cycles per key) at a low price ($25 to $35 for 60 key standard configurations without electronics). In addition, they can offer EMI/RFI shielding and protection against multi-key rollover and static discharge. Front panel sealing is an added plus exclusive to the FTM keyboard.

The ease with which the FTM keyboard interfaces with μP and associated electronics positions it very well for significant growth through the 1980s. Sales should outpace the average growth of the electronics industry in general. Total projected sales for all types of alphanumeric keyboards should reach $194 million this year and $425 million by 1985. Membrane based keyboards will probably account for 25% of the total market by 1985—up from just 1% in 1981. The economics and reliability of FTM keyboards should lead to a dominant market position by the mid-1980s.

Applications are and will continue to be concentrated in mainframe computer systems, CRT remote terminals, keytape systems, teletype communications systems, personal computers and WP systems.

FTMs Will Rival Existing Capacitance Technologies For Dominance

by Mark Tiddens
Keytronic Corp., Spokane, WA

We feel that full-travel membrane keyboards will rival existing capacitance keyboard technologies for the dominate position by the end of the 80s. Existing capacitance keyboard technologies are the most cost effective for encoded applications (keyboard with electronics) today and it took about six years for them to achieve the dominate position they have now. The keyboard is such a critical part of computer and terminal equipment that users are wary of trying out new technologies. This is especially true as the keyboard has received more attention because of increased human factors (ergonomic) concerns which require that the keyboard have good quality, reliability, and flexibility.

FTM keyboards will definitely become the dominate technology for wired-only applications, as opposed to detached keyboard applications which require some electronics to provide serial output thru a cable. Wired-only applications involve those where the main electronics in the computer or terminal can scan the contact switch matrix directly. The keyboard has to be housed in the same enclosure as the main terminal or computers electronics so that the interconnection is as short and inexpensive as possible since there can be as many as 20 lines from the X-Y matrix for an 8 × 12, 96 station keyboard, for example. The cost advantage of a FTM keyboard in wired-only applications is that an inexpensive silver-contact membrane with backplate replaces a PCB and soldered-in, gold-contact switches. Otherwise, the number of switch parts required is identical to a low cost capacitance switch. Adding a separate PCB with connector and electronics to create an encoded membrane keyboard defeats this cost savings over a low-cost encoded capacitance keyboard.

No Single Technology Suits The Variety Of Needs

by Rand J. Eikelberger
Cherry Electrical Products, Waukegan, IL

Variables such as number of keys, number of operations and environment have significant influence on choice of the appropriate technology. We believe there is a market for FTM keyboards, but feel that that market is substantially more limited than has been touted. The attraction of FTMs has been the desirability of a sealed design and the low price. A major disadvantage is the inability to repair the membrane.

Addressing the topic of the sealed design, some customers have already learned to their dismay, of the effects of barometric pressure on a sealed design. A few manufacturers have overcome this with air reservoirs to prevent collapse of the switches under these conditions. This approach appears workable, but does away with some of the price advantage. The price advantage also only seems to exist for designs that do not require rigid PCBs. These keyboards do not lend themselves to true N-key rollover. In some instances, a pseudo N-key rollover may be sufficient.

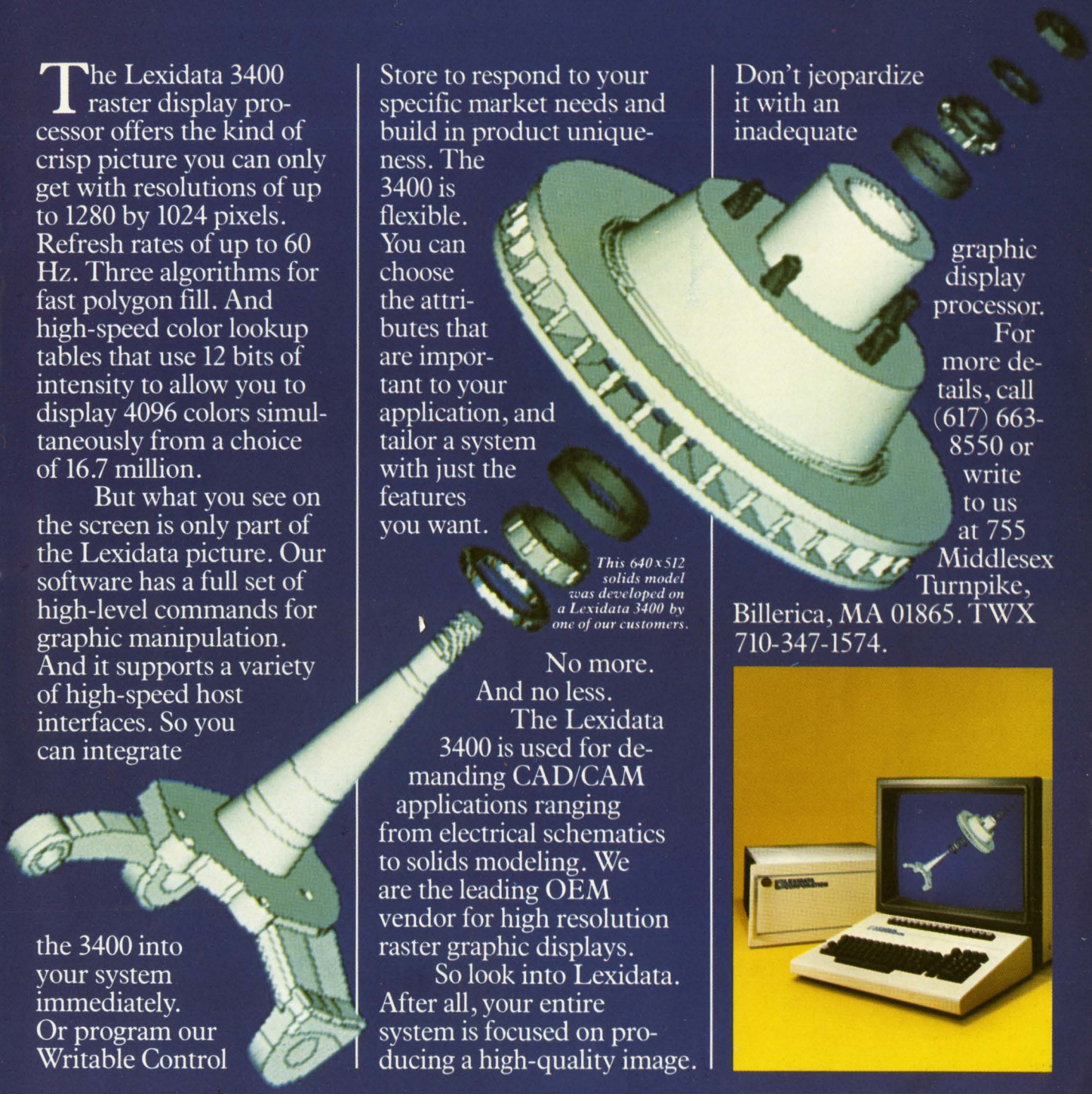
The cost of the users' end product using a membrane keyboard with no rigid PCB as part of it now includes two additional connectors and quite often a rigid PC board with encoding electronics on it. In our opinion, this does not usually offer a price advantage to the manufacturer for his end product.

We believe the life of a membrane keyswitch to be substantially lower than that of other existing technologies. We have not precluded offering a FTM keyboard, but have announced the higher priority program to pursue the development of conductive elastomer technology for full travel designs. We expect this technology to offer roughly the same degree of sealing and economies for those who can tolerate the kind of life that a FTM keyboard has. Also, the elastomer offers the benefit of tactile feel.

The Lexidata 3400. As close as you can come to reality.

The Lexidata 3400 raster display processor offers the kind of crisp picture you can only get with resolutions of up to 1280 by 1024 pixels. Refresh rates of up to 60 Hz. Three algorithms for fast polygon fill. And high-speed color lookup tables that use 12 bits of intensity to allow you to display 4096 colors simultaneously from a choice of 16.7 million.

But what you see on the screen is only part of the Lexidata picture. Our software has a full set of high-level commands for graphic manipulation. And it supports a variety of high-speed host interfaces. So you can integrate the 3400 into your system immediately. Or program our Writable Control Store to respond to your specific market needs and build in product uniqueness. The 3400 is flexible. You can choose the attributes that are important to your application, and tailor a system with just the features you want.



This 640 x 512 solids model was developed on a Lexidata 3400 by one of our customers.

No more. And no less.

The Lexidata 3400 is used for demanding CAD/CAM applications ranging from electrical schematics to solids modeling. We are the leading OEM vendor for high resolution raster graphic displays.

So look into Lexidata. After all, your entire system is focused on producing a high-quality image. Don't jeopardize it with an inadequate graphic display processor.

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The IP8500 memory access and architecture are superior in storage capacity, speed and addressing flexibility. Our new extended memory option quadruples previous storage with up to 20 individual 1024x1024x8 bit-image tiles based on 64K dynamic RAM memory. Each has independent zoom, pan and scroll, as well as a selectable intensity transformation table. A new high resolution option is also available and includes a video output controller offering 1024x1024 pixel imagery in monochrome or full color. And for those whose requirements are limited to 12 memory tiles, Gould DeAnza offers the IP8500A image processor with standard and extended features included at a substantial savings.

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The IP8500 can support from one to four display channels, each with an optional cursor generator and its associated joystick or trackball and alphanumeric overlay generator.

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Gould DeAnza is the leading supplier of image processing systems to the LANDSAT, medical and printing industries. The IP8500, with its dazzling performance and affordable price, is just one reason why. Call today and we'll help you choose the system that's right for you.

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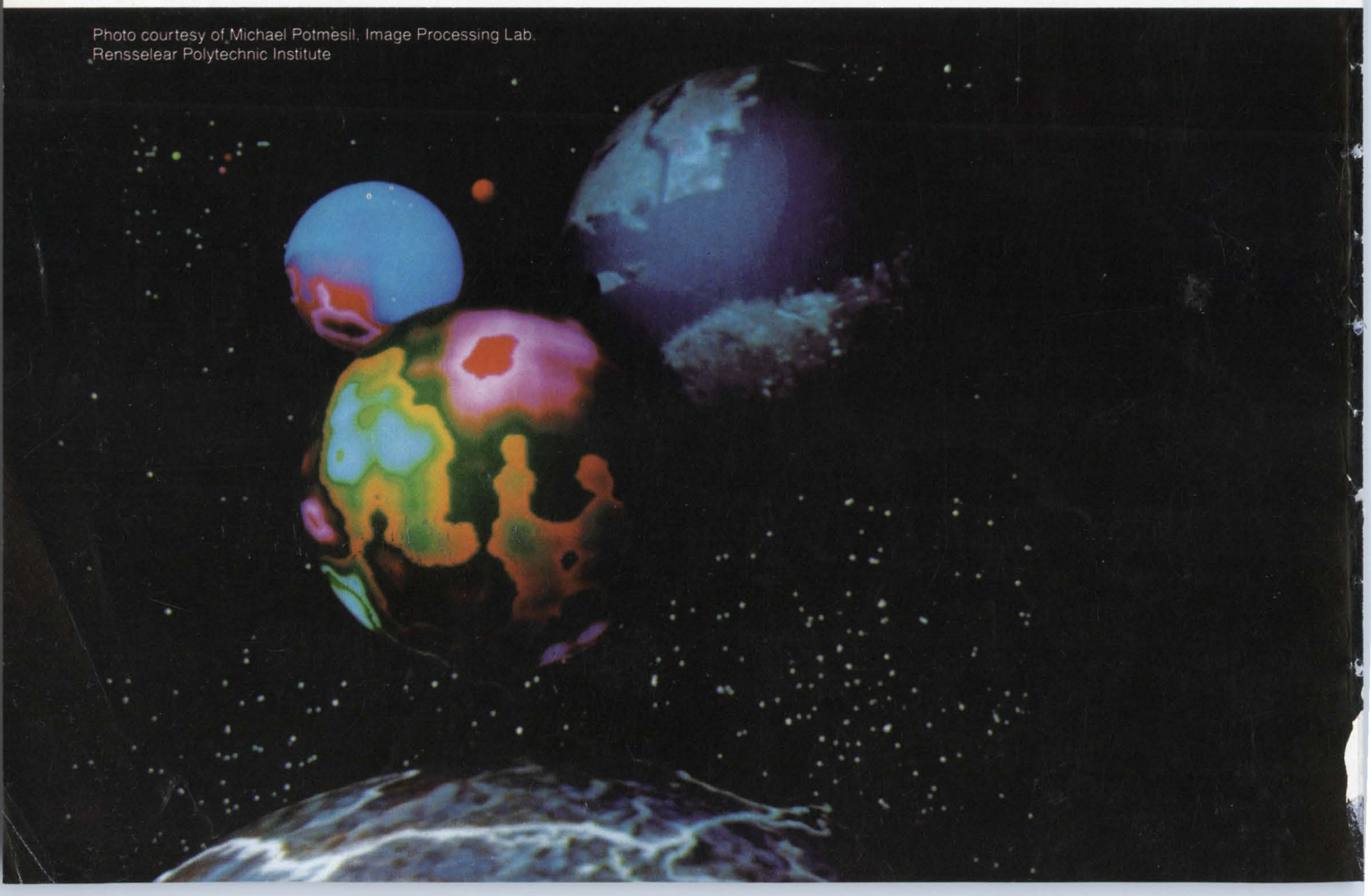

Photo courtesy of Michael Potmesil, Image Processing Lab, Rensselear Polytechnic Institute