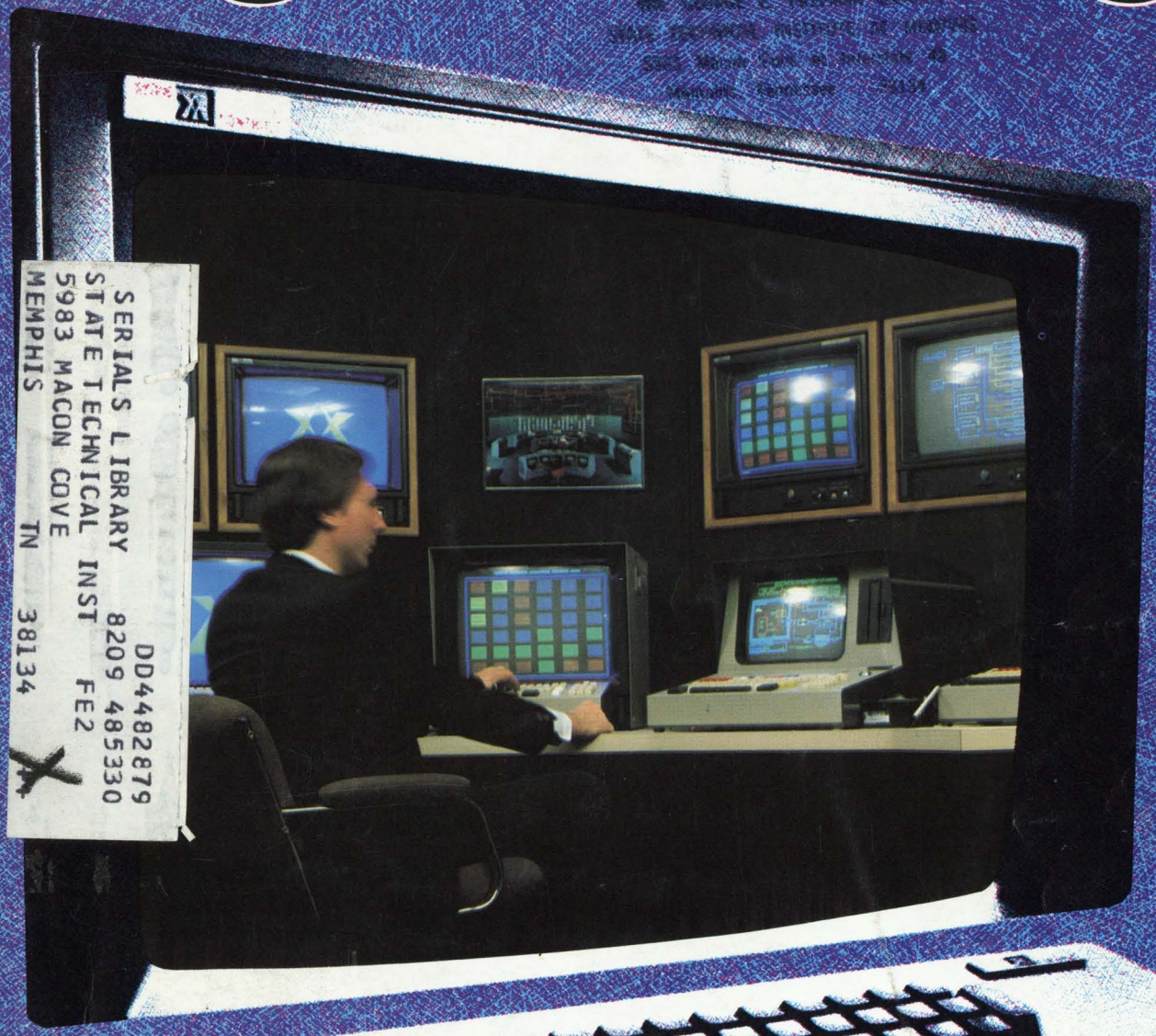
A MORGAN-GRAMPIAN PUBLICATION

Digital Design



COMPUTERS/SYSTEMS • PERIPHERALS • COMPONENTS • 2/82

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Dedicated Computers Improve Graphics

Your Refresh Scheme May be Killing Your μP
New Medical Applications • High IQ Terminals

VOL. 12
NO. 2

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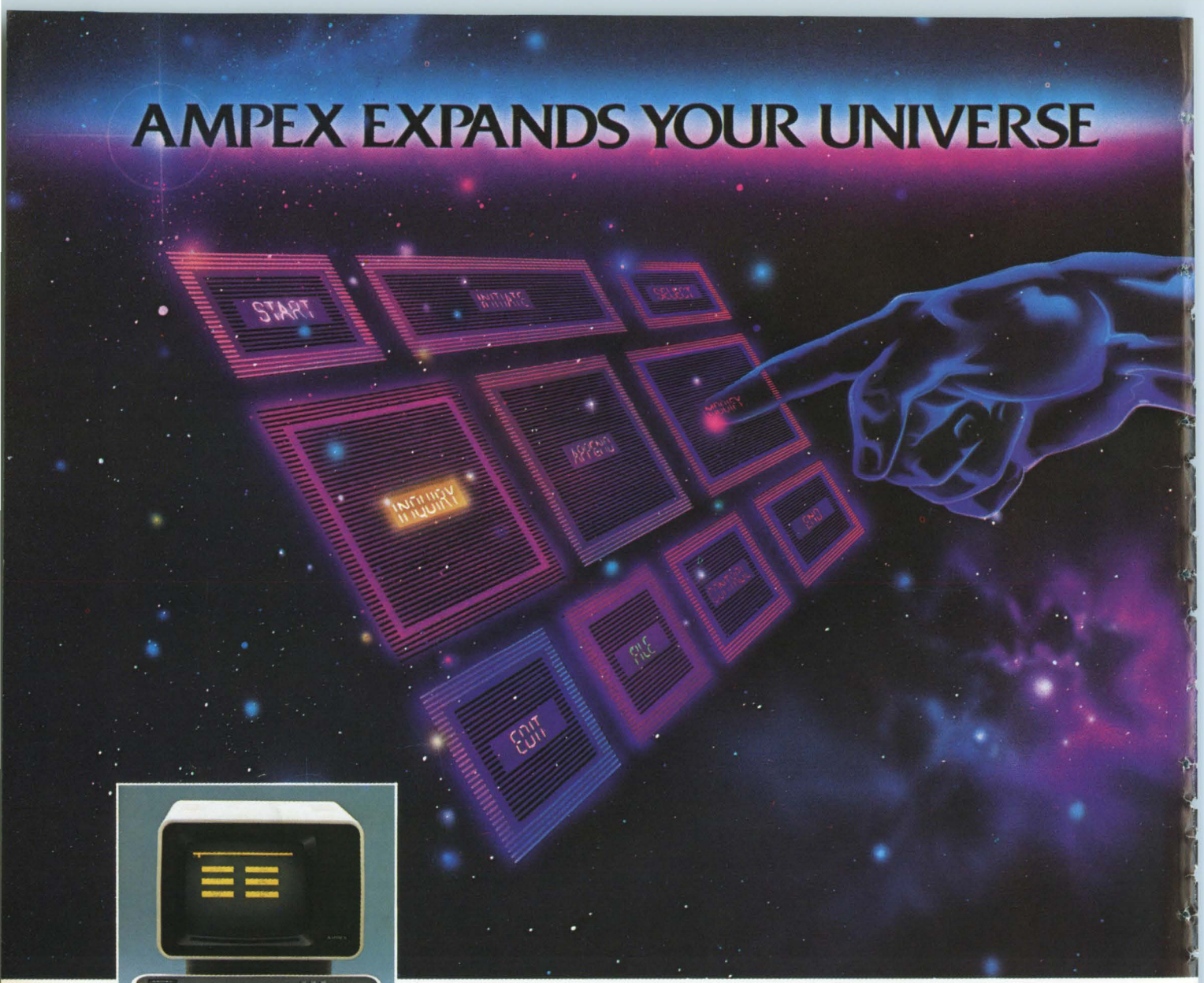

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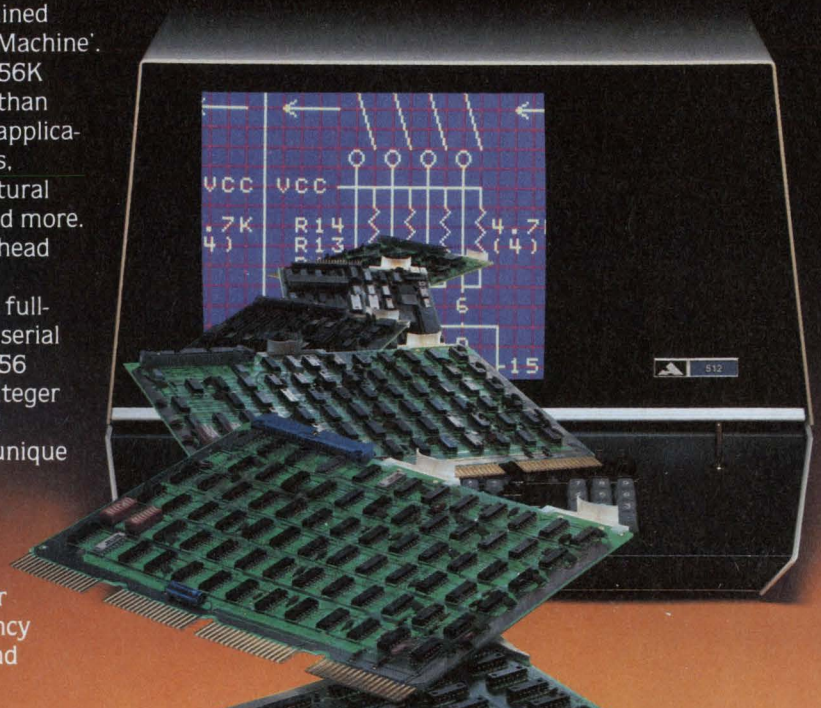

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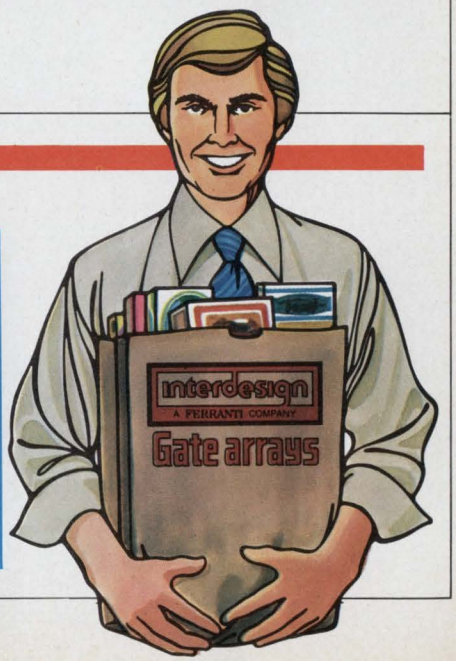

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VOL. 12, NO. 2

Digital Design

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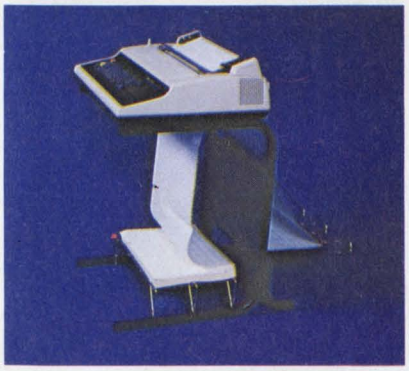

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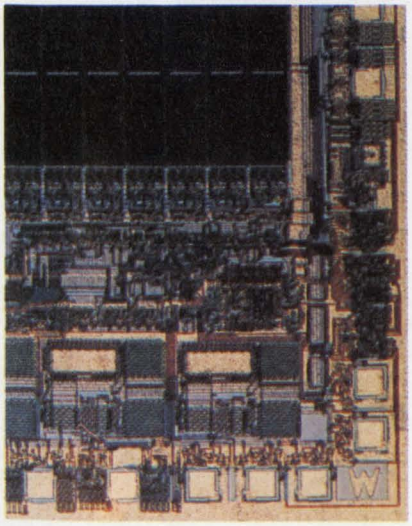

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Cover

Our cover photo, which illustrates the world of computer graphics as seen through a CRT terminal, comes to us courtesy of Aydin Controls, Fort Washington, PA.

COMPUTERS/SYSTEMS

PERIPHERALS

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Postmaster, send address corrections to : Morgan - Grampian Publishing Company, 1050 Commonwealth Ave., Boston, MA 02215. 2nd class postage paid at Boston, MA and additional mailing offices.

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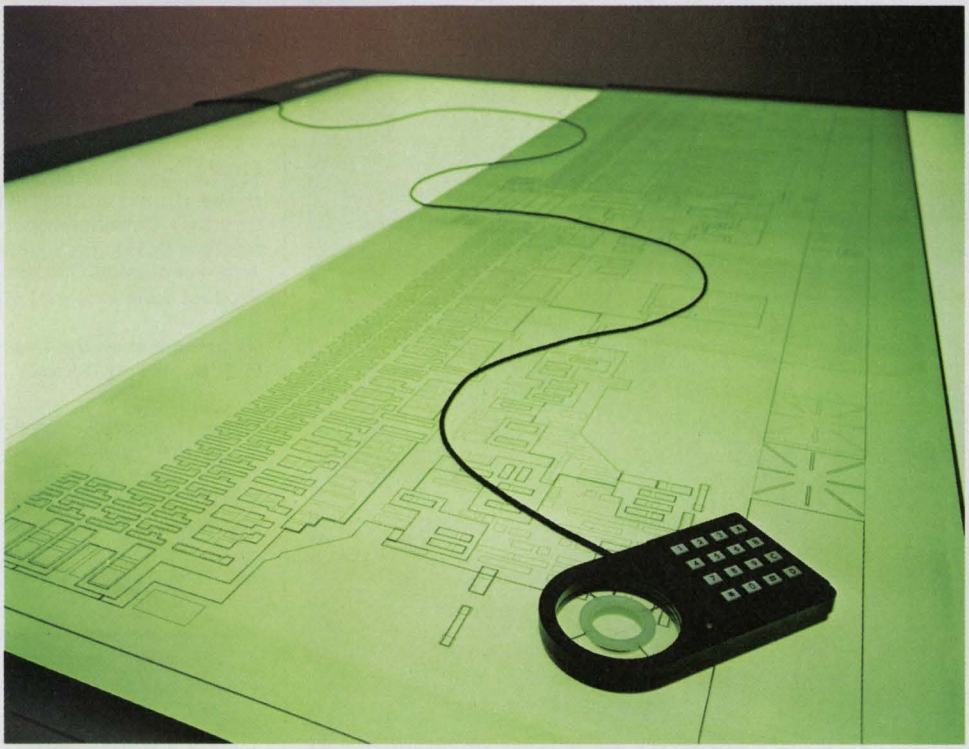
Most digitizers are pretty much alike... the New CalComp 9000 Series is the exception.



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Writing Tight Code Is Costly

Dear Editor:

In your October 1981 issue on page 24 of your article, "The Pros of Pascal," you wrote the following four laws: 1. Not everything worth doing is worth doing well, 2. If you can do a quick and dirty job and it works, do it, 3. There is no such thing as perfect code and 4. Learn when to stop striving for perfection. In summary, you say that the price of perfection is bankruptcy. Your four laws break the IEEE code of ethics, as well as the ethics of most other engineering organizations. How can we maintain high standards of diligency, creativity and productivity if "quick and dirty" workmanship is the goal for productivity?

Malcolm Drummond
60 Marberth Drive
Henrietta, NY 14467

Ed. Reply:

I am sorry that my advice was mistaken as an invitation to violate ethics; it's not what I meant. I think if read in context, the four laws will be seen as referring to what every programming writer/author has been saying now for half a decade. These laws are not mine; they are espoused by leading software experts. Writing the tightest possible code is fine if there's no choice, as I stated, but otherwise is itself unethical, since such "bit jockeys" are wasting their firm's resources in a less optimum approach—and often doing so knowingly. Fortunately, this affliction to strive for perfection was exhibited mainly by EE hardware-designers-turned-programmers in the 1975-1979 time frame. Some maturity and sophistication has set in since then.

DEC Compatible Equipment

Dear Editor:

We are about to select a vendor for communication line interfaces to our workstations which are based on DEC's LSI-11/23 Q-bus CPU. We are searching for an interface that: supports HDLC, SDLC and other bit- and byte-oriented protocols, has data rates of 300 Kbits/sec or more, is compatible with the electrical recommendation EIA RS-232-C and EIA RS-422 or at least one of them, and preferably that has a DMA facility to reduce CPU load. This means an interface more or less equivalent to DEC's COMM IOP-DUP for UNIBUS.

If anyone knows of vendors that supply such interfaces, we would be pleased to receive vendor references including telex and phone numbers.

Arne Kjaeras
ICAN a. s.
Moloveien 1, Box 31
9191 Horten, Norway

Motor Generators Provide "Ride-Through"

Dear Editor:

I read with interest October's article "Uninterruptible Power Sources Provide Systems Insurance," by P. Snigier (pp. 28-33), and would like to congratulate you on bringing this very serious power problem to the attention of your readers. The article, which dealt primarily with computer power quality problems, as opposed to power continuity problems (blackouts) unfortunately did not discuss the synchronous motor-generator as the ultimate solution to power quality problems. Providing the highest quality of power (and actually required by some manufacturers as an interface between the UPS and the computer), the synchronous motor-generator provides a significantly higher quality of power than UPS transformer-type power conditioners, AC line regulators and ultra-isolators. The synchronous motor-generator power conditioner, with its inherent rotating stored energy to ride-thru momentary interruptions (up to 500 ms), provides a pure sine wave with less than 3% harmonic distortion, output voltage regulated to + 1% and a true 120° phase shift between phases far exceeds the power quality of any other technology on the market today.

In your article, you indicated that transformers would cure power factor capacitor switching problems. However, our experience is that a major percentage of our installations are to replace various types of transformer devices which have failed to resolve this specific problem. Also, a major problem not identified is utility grid switching caused interruptions (flickers) of 50 ms or more which the transformer devices cannot correct since they have no ride-thru capability.

In regard to protection from lightning strikes, again the motor-generator provides the ultimate protection. With hundreds of installations throughout the world, we do not have a single known case of motor-generator or computer damage caused by either direct or indirect lightning strikes. We recently received a letter from Old National Bank who experienced a direct hit on their transformer bank outside the building but caused no damage to the motor-generator or the computer. I do not believe any other technology can make this claim. In cost per KVA, the motor-generator is approximately 25-30% of the cost of a UPS; however, it provides over 99% protection against the power line disturbances indentified in the IBM report.

You identified the "PoweRotor" as being one of the innovative designs cropping up in the power backup field. I am enclosing a copy of a letter we received from Continental Power Systems dated October 13, 1981, indicating they have terminated all sales activity and are not accepting orders for the "PoweRotor".

Finally, in your discussion of UPS basics, you describe the on-line and off-line UPS, and the advantage of an off-line UPS life-time as being considerably longer. We currently are developing an off-line Rotary UPS. By taking advantage of the ride-thru characteristics of the motor-generator, we eliminate the risk of introducing a disturbance on the output. A further advantage is that even with an inverter failure, the motor-generator will continue to furnish clean power and protection against all power problems, except blackouts, until the inverter is serviced.

Another advantage of the motor-generator is that the synchronous

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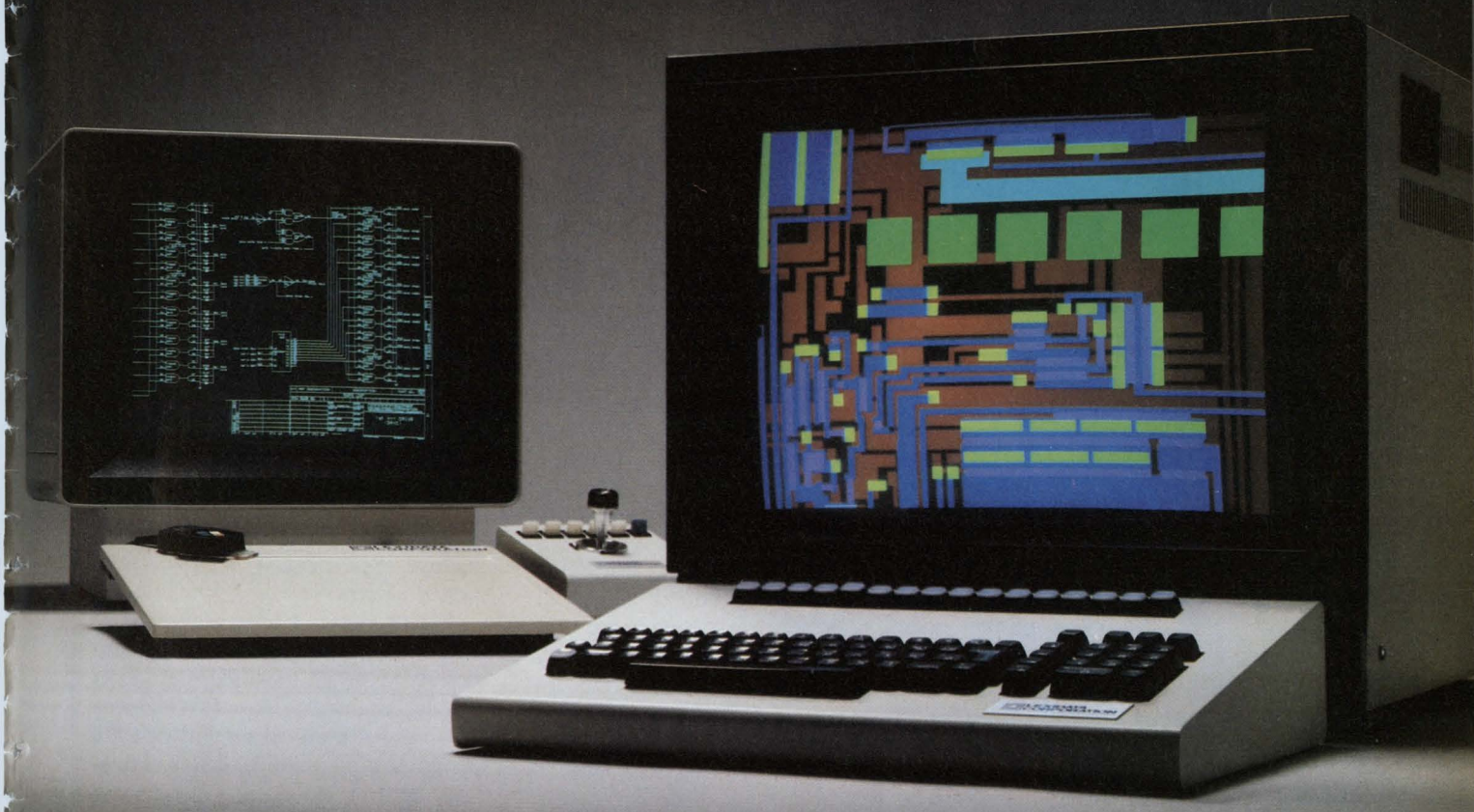

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R.N.Bowyer
Vice-President, Marketing/Sales
Computer Power Products
2900 E. Olympic Blvd.
Los Angeles, CA 90023-3468

Bubble's Future Is Bright

Dear Editor:

After reading "Compatible Computer Memory", by P. Snigier (pp. 12-26) in November's issue, I feel compelled to come to the defense of bubble memory. You seem convinced that the bubble's future is bleak and at worst non-existent. As a happy user of bubble memory for two years, I disagree.

Our company offers a line of bubble memory based products, including a portable text-editing terminal used in the publishing industry. We recently introduced a S-100 compatible bubble memory subsystem, offering from 128kB to 1MB of nonvolatile online storage. Both these products are based on the Intel 7110 bubble memory device, but we have considerable experience with the other vendors you mention in your review.

I'd like to comment on several points in your article. First, regarding the departure of Rockwell, National and TI from the market, I have been close to this market since 1979 and have personally spoken with several leading commercial experts in the bubble memory business, most of whom have offered the same general rationale for the departure of "the big three" —profitabilty. Inaccurate market size projections was a contributer, but profitability was a major short-term concern. Problems ranged from non-conservative designs to process control to test problems; all of which negatively impacted yields. Additionally, the primary business of all three vendors is the manufacture of semiconductors. Semiconductor manufacturing differs somewhat from successful bubble memory manufacture, and these differences are key. Of the US manufacturers, only Intel and National (and now Motorola) have viewed the market as a system market rather than a component market, and supplied interface components to allow simple interface to μPs.

Regarding price, there is no doubt that costs have not declined nearly as fast as predicted. However, this is no longer the case. Intel is guaranteeing prices of 30m¢ per bit in 3Q82 (not predicting them as you maintain), and Motorola's projections are in line with Intel's. In addition, entry cost declined rapidly, and should undercut that of rotating memory (specifically, 5-¼" floppy disks) within three or so years.

Many early market projections predicted a multi-billion market by 1985, and this was admittedly wrong. If, however, you look at the projections of those companies still in the business, you will see much more conservative numbers (Intel, for example, projects $500 million, while Motorola is more conservative at $226 million).

You comment that Intel has placed their best designers on RAM/EPROM designs. Remember, bubble memory is not a semiconductor. "Monolithic magnetics" differ significantly in their design from semiconductor memory, and different talents are required.

Last, you seem to feel that bubble memory will find only limited market acceptance, in "hostile environments, portable terminals, and little else." Be careful not to downplay the ramifications here. Bubble memory will open new product possibilities in these markets. There is a host of possibilities for products which will operate in hostile environments which do not currently exist solely due to the lack of suitable mass storage. Bubble memory will open the door for many such applications which have not yet been conceived.

In summary, it is important for engineers and managers to see through the haze of bad publicity recently cast on bubble memory. The market admittedly has a number of scars and bruises, but take it from a successful user—the patient is in good condition. The injuries caused by incorrect projections and vendor pullouts are painful, but not critical. Let's not lower the flag to half-staff.

David L. Airel
Teleram Communications Corp.
Manager, Advanced Development
100 Ford Rd.
Denville, NJ 07834

Ultra-isolators Beat Blackouts

Dear Editor:

I was pleased to see the Topaz Problem-Solver Guide and 81000 diagram in November's UPS discussion. It will help readers decide which product is best for their power conditioning needs. However, the word "Ultra-Isolator" was used as a generic term for isolation transformer. It is the registered name of Topaz.

Patrick K. Hallinan
Topaz Electronics Division
Topaz, Inc.
3855 Ruffin Rd.
San Diego, CA 92123

68000 Development System

Dear Editor:

As developers of the 68000, we are pleased to have yet another company (CM Technologies) join those already involved in the development of equipment based on this MPU. However, Mr. Lichtgarn's opening statement in your November issue (page 68) that the system he describes is the only available development system for this processor is incorrect: Motorola's EXORmacs Development System was introduced almost concurrently with the processor itself.

Moreover, stating that the Multibus was chosen for the system described rather than the faster VERSAbus because the latter (8MHz) was too fast for peripherals that operate at 5MHz is an obvious technical misstatement.

Lothar Stern, Manager
Technical Communications
Motorola Inc.
Semiconductor Group
5005 East McDowell Rd.
Phoenix, AZ 85008

INCOMPARABLE.

Pigments and pixels can both arrest an instant for eternity—but, their comparison fails after that. So too, digital image processing and computer graphics. Some may claim to give you both in the same system, but with today's technology, it can't be done well. Either, it's a digital image processing system or a graphics system. At COMTAL, we provide certain graphics capabilities, but not at the expense of the image processing architecture.

Also, image processing is not the same as image display. Some "image processors" are little more than a refresh memory pumping data through a display buffer. And if it's a software-based system, forget real-time, interactive operations.

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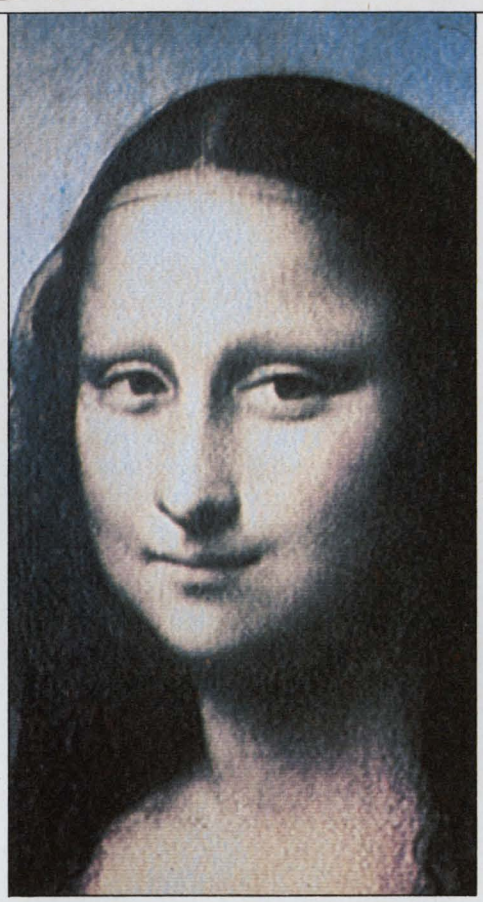

Image of Mona Lisa processed by Combined Logic Research, Hollywood, CA, on a COMTAL Vision One/20 using histogram equalization and function memory modifications for brightness, contrast and color correction.

4x zoom using pixel replication.

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Mona Lisa's elusive smile defies comparison. It is quintessential art. In image processing, COMTAL is the state of the art. We invite your comparisons. But, measure for measure, we think you'll judge us incomparable. COMTAL Corporation, a subsidiary of 3M, 505 West Woodbury Road, Altadena, CA 91001 Telephone (213) 797-1175.

COMTAL

■ Image Resolution and Bit Depth ■ Number of Images (i) & Graphics (g) In Typical Configuration			Function Memory Processing	Small Area Processing	Real-Time Arithmetic	Dual User Capability
Image Display/ Processing	8000-R Model 30	512^2 x 8 3i, 4g	■			
	8000-R Model 65	1024^2 x 8 3i, 4g	■			
Stand-alone Image Processing	VISION ONE/10	512^2 x 8 4i, 4g	■	■	■	
	VISION ONE/20 Model M8	512^2 x 8 7i, 8g	■	■	■	■
	VISION ONE/20 Model M10	512^2 x 8 15i, 8g	■	■	■	■
	VISION TEN/24	1024^2 x 8 4i, 8g	■	■	■	■
	VISION ONE/12	$256^2/512^2$ x 12 3i, 12g/1i, 4g	■			
Image Input	Digital Video Input Processor	Acquires and digitizes filmed images illuminated by a light table; integrates as many as 256 frames; images can be transferred to a VISION ONE/20 or host computer.				

Calendar

March 1-3

Symposium on Architectural Support for Programming Languages and Operating Systems. Palo Alto, California. Contact David R. Ditzel, room 2C-523, Bell Labs., Computing Science Research Center, Murray Hill, NJ 07974.

March 1-4

Robots VI, industrial robot conference and exposition, at Detroit's Cobo Hall. Co-sponsored by Robotics International of the Society of Manufacturing Engineers (RI/SME) and the Robot Institute of America (RIA), an affiliated association of SME. Contact: Robotics International, P.R. Dept., One SME Drive, P.O. Box 930, Dearborn, MI 48128; (313) 271-1500, Ext. 362.

March 1-5

ELECTREX '82, International Electrotechnical Exhibition, National Exhibition Centre in Birmingham, UK. All types of electrotechnical equipment for power production and transformation, transmission and distribution, power application. Contact: Electrex Ltd, Wix Hill House, West Horsley, Surrey KT24 6DZ England. Telephone: 0483 222888. Telex: 859460 Electx G. Cables: ELECTREX, West Horsley, Leatherhead.

March 3

FIPS Software Documentation Workshop/NBS, Gaithersburg, MD; sponsored by NBS; contact: Albrecht J. Neumann, A369 Technology Building; National Bureau of Standards, Washington, D.C. 20234; (301) 921-3486.

March 3-7

Microcomputer Week '82, Jersey City, New Jersey. Contact: Catalyst Conference H-112, Jersey City State College, 2039 Kennedy Blvd., Jersey City, NJ 07305; (201) 434-2154.

March 9

Micro-Delcon '82—Fifth Annual Conference on Computer Technology, Newark, DE. Contact: John DeGood, Research and Development, Hewlett-Packard, Route 41 and Starr Rd., Avondale, PA 19311.

March 9-11

Seventh International Zurich Seminar on Digital Communications, Zurich, Switzerland. Contact: M. Frey, EAE, Siemens-Albis AG, POB, CH-8047 Zurich, Switzerland.

March 11, 18, 23

Third International Invitational Computer Conference, London (11th), Stockholm (18th) and Frankfurt (23rd). Featured products include streaming and conventional tape drives, graphic terminals, printer/plotters and μC-based systems and peripherals. Contact: B.J. Johnson and Associates, Newport Beach, CA; (714) 644-6037, Telex number 67840. UK and European inquiries, contact: Tom Lewis, telephone: (01) 994-6477, Telex number 8811418.

March 15-17

Human Factors In Computer Systems/NBS, Gaithersburg, MD; sponsored by NBS and Association for Computing Machinery; contact: Albrecht J. Neumann, A369 Technology Building, National Bureau of Standards, Washington, D.C. 20234; (301) 921-3486.

March 15-18

International Workshop on Physics and Engineering in Medical Imaging, Asilomar, CA; contact: Dr. Orhan Nalcioglu, Dept. of Radiological Sciences, University of California, College of Medicine, Irvine, CA 92717.

March 16-18

The Mathematics of Computer Sciences, Paris, France. Contact: Secretariat du Colloque "Mathematiques pour l'informatique," A.F.C.E.T. 156 Bld Pereire—F. 75017, Paris, France; Tele. 786-24-19/766-24-23.

March 16-18

SOFTWARE/expo-West, Anaheim Convention Center. Contact: SOFTWARE/expo-West, Suite 400 -222 West Adams St., Chicago, IL, 60606; (312) 263-3131.

March 17-19

15th Annual Simulation Symposium, Tampa, FL. Contact: Edward A. DeYoung, Caterpiller Tractor Co., 600 W. Washington St., East Peoria, IL 61630.

March 17-19

16th Annual Conference on Information Sciences and Systems, Princeton, NJ. Contact: Stuart Schwartz, Dept. of EE and Computer Science, Princeton University, Princeton, NJ 08544.

March 18-19

Workshop On Standardization Of Speech I/O Technology/NBS, Gaithersburg, MD; sponsored by NBS and Naval Air Development Center; contact: Davis S. Pallett, A214 Technology Building, National Bureau of Standards, Washington, D.C. 20234; (301) 921-3427.

March 19-21

Seventh West Coast Computer Faire, San Francisco, CA. Contact: Laurie McLean, 333 Swett Rd., Woodside, CA 94062; (415) 851-7075.

March 22-24

MMT'82 Fourth Annual Microelectronics Measurement and Test Conference, San Jose, CA; show theme is "Operation Quality Update", featuring courses, workshops, seminars and exhibits. Contact: Microelectronics Measurement and Test Conference, 1050 Commonwealth Ave., Boston, MA 02215; (617) 232-5470.

March 22-24

National Conference on Information Systems Education, Chicago, IL. Contact: Conference Manager, USPDI, 12611 Davan Dr., Silver Spring, MD 20904; (301) 622-0066.

March 22-25

Interface '82 Dallas Convention Center; data communications/information processing conference and exposition. Contact: The Interface Group, PO Box 927, 160 Speen St, Framingham, MA 01701; (800) 225-4620 or (617) 879-4502 (in MA).

March 22-26

Computer Graphics for Design and Construction Productivity, Washington, DC. Contact: World Computer Graphics Association, Inc., 2033 M St. NW, Suite 333, Washington, DC 20036; (202) 466-5896.

March 22-26

Tutorial Week East '82, Orlando, FL. (Being held in parallel with IEEE Southcon/82). Contact: Tutorial Week East, PO Box 639, Silver Spring, MD 20901.

March 23-25

Southcon/82, Orlando, FL. Contact: Robert Myers, 999 N. Sepulveda Blvd., El Segundo, CA 90245; (213) 722-2965.

March 24-26

Second National Symposium on EDP Quality Assurance: Doing It Right the First Time. Chicago, IL. The conference will stress solutions to EDP quality problems, with emphasis on the methods to improve quality and to reduce costs in the areas of systems development, testing, maintenance, auditability, and software installation. Contact: U.S. Professional Development Institute, 12611 Davan Dr, Silver Spring, MD 20904; (301) 622-0066.

March 26-27

Southern New England Microcomputer Show, New Haven, CT. Contact: North East Productions, Inc, 970 Asylum Ave, Hartford, CT 06105; (203) 247-7111.

March 29-31

PCI/MOTORCON '82, Moscone Convention Center, San Francisco, CA. The Fourth International Power Conversion Conference (First in the USA) concurrently held with the Second International Motorcon Conference (Electronic Motion Control). Contact: Intertec Communications Inc., P.O. Box 2889, Oxnard, California 93034; (805) 985-1595; Telex: 182218 nupower oxn.

March 29-April 1

National Design Engineering Show, McCormick Place, Chicago. Contact: William C. Little, Clapp and Poliak Inc, 245 Park Ave, New York, NY 10167; (212)661-8410.

March 29-April 2

Infocom '82, Las Vegas, NV. Contact: Infocom 82, PO Box 639, Silver Spring, MD 20901; (301) 589-3386.

March 30-April 1

CAD 82, Metropole, Sussex, UK. Contact: Alan Pipes, IPC Science and Technology Press, PO Box 63, Westbury House, Bury St., Guildford GU2 5BH, UK.

News Update

EIA Testifies On US Trade Policy

Testifying here today before a House Ways & Means Subcommittee, the Electronic Industries Association (Washington, DC) urged Congress to take action to reduce foreign governments' intervention so that US firms can compete on a fair basis, or to put into place US government policies which serve to equalize the intervention of foreign governments and thus increase the international competitiveness of our companies. To encourage joint research, EIA President Peter McCloskey proposed antitrust laws be amended so companies within the scope of an approved review letter from the Justice Department be immune from both civil and criminal action for activities conducted within the scope of the approval. McCloskey noted that such a measure would remove antitrust uncertainty relating to joint research and lead to increased R&D and a more effective use of scarce human resources, thus substantially benefiting the nation's international competiveness.

RCA's 50-City Digital Message Service

RCA Network Services, Inc., filed an application with the FCC to construct and operate a nationwide digital electronic message service (DEMS) among the nation's 50 major metropolitan areas. RCA's DEMS network will provide high-speed, end-to-end private line and switched services to the public. It will handle 2.4 kB/sec to 1.5 MB/sec digital bit streams, and handle many user applications such as communicating WPs, remote computer entry, high-speed fax and videoconferencing. The proposed service will use satellite and microwave facilities for long-haul transmission and the new Digital Termination System (DTS) technology for transmission within cities.

$500 K Microelectronics Planned By SRI

SRI International of Menlo Park, CA (formerly Stanford Research Institute) announced it is now accepting applications for sponsorship of the largest multi-client supported research project in microelectronics ever to be undertaken. The half million dollar study, "Microelectronics—Technology, Trends, and Devices," will be directed toward manufacturers and users of microelectronics and to companies who supply fabrication equipment to manufacturers. SRI projects that even though the world semiconductor market will grow to $74.1 billion by 1990 (a 23% annual growth through the 80s), ever increasing IC complexity will present serious problems to semiconductor manufacturers due to accelerating competition from the Japanese and the Europeans.

MSI Agreement With Matsushita

MSI Data Corp (Costa Mesa, CA) concluded an agreement with two major Japanese companies under which MSI will market worldwide a new low-cost, handheld data entry terminal. The MSI data entry terminal will be produced to MSI's specifications in Japan by Matsushita Communication Industrial Ltd. (MCI) and purchased by MSI through C. Itoh Electronics.

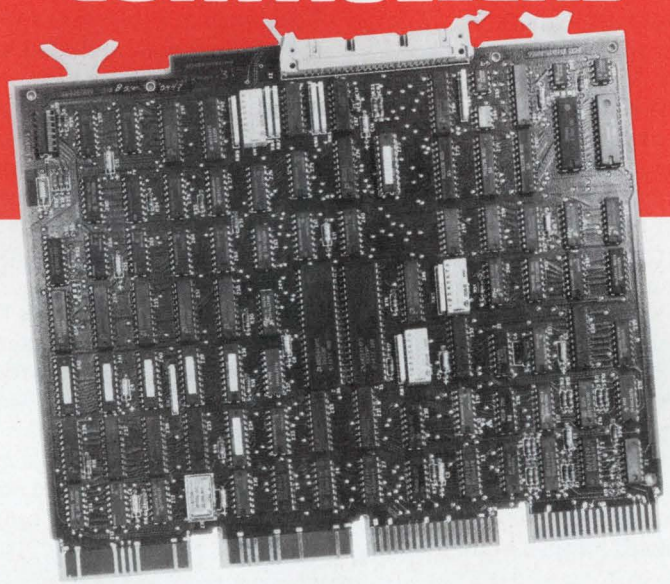
Four Phase To Merge With Motorola

Motorola and Four-Phase Systems jointly announced that both companies have approved an agreement in principle for the acquisition of Four-Phase by Motorola. The agreement is intended to provide each Four-Phase shareholder with a value of $45 per Four-Phase share in Motorola common stock.

New Desktop μC System

A low-cost system allowing users to see a computer's internal mathematical and logical operations in action from Datamac (Sunnyvale CA), offers a first in the industry: a Systems Activity Monitor that lets users see bytes (characters) of data as they migrate from one location to another in computer memory and undergo various mathematical and logical operations. The $2650 -$4670 Datamac 1200 series also offers the CP/M operating system, Corvus compatibility, intelligent terminal emulation, a "help key," and programmable function keys.

DEC®-COMPATIBLE PERIPHERAL CONTROLLERS



Dataram Corporation offers the industry's widest range of DEC-compatible peripheral controllers — from comparatively simple NRZI tape controllers to complex 300 MB storage module drive (SMD) controllers.

An impressive array of state-of-the-art controllers, all built around high-speed bipolar microprocessors. All software compatible with the host LSI-11®, PDP®-11, or VAX® minicomputer...and all available now.

And Dataram's controllers are designed to save you money, and, more importantly, space — our controllers typically occupy half the space required for the comparable controller from DEC. Doing it with a level of performance that makes any member of this family worth looking at.

The chart shows our current family of peripheral controllers, growing every day. If you don't see the controller you need, we're probably working on it right now. Call us and discuss your requirements.

CONTROLLER	DESCRIPTION	COMPATIBILITY
C03	Cartridge disk controller	RK05
C33	Cartridge disk controller	RK05
T03	NRZI mag tape controller	TM11/TU10
T04/N	NRZI mag tape controller	TM11/TU10
T04/D	Dual density mag tape controller	TM11/TU10
T34/N	NRZI mag tape controller	TM11/TU10
T34/D	Dual density mag tape controller	TM11/TU10
T36	Dual density mag tape controller	TM11/TU10
S03/A	80 MB/300 MB SMD controller	RM02/RM05
S03/A1	80 MB/160 MB SMD controller	RM02
S03/B	80 MB/300 MB SMD controller	RK07
S03/C	200 MB/300 MB SMD controlle	RP06
S03/D	96 MB CMD controller	RK06
S33/A	80 MB/300 MB SMD controller	RM02/RM05
S33/A1	80 MB/160 MB SMD controller	RM02
S33/B	80 MB/300 MB SMD controller	RK07
S33/C	200 MB/300 MB SMD controller	RP06
S33/D	96 MB CMD controller	RK06

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DATARAM CORPORATION

Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

Write 15 on Reader Inquiry Card

Ikier Introduces High-End Computer Graphics System

New from the recently-formed company Ikier Technology (16 Sears St, Burlington, MA 01803) is the Eagle-1 Graphics Computer. Brainchild of Hans Ikier (founder and ex-president of Lexidata), the Eagle combines a high resolution (1024 x 800 pixel) monochrome CRT with a 2 megapixel memory plane, and features hardware vector/raster conversion at 800 nsec/pixel and DMA block transfers at 750 KB/sec. The computer system consists of an Intel 8086 16 bit CPU, Intel 8087 floating point processor, up to 1 MB of system memory and a Multibus card cage. The system also features a 1 MB floppy disk (also usable as a 256 KB floppy for CP/M-86 compatibility), a 10 MB Winchester disk, four port multiplexers for RS232 devices and a detachable keyboard with 31 function keys. Eagle marks a growing trend in flexibility of graphics systems: it can operate as a stand-alone graphics system, or it can be integrated into a distributed graphics network, operating as a highly intelligent graphics terminal.

Glass Strands Provide New Communications Link

A three-mile cable containing six glass strands as fine as human hair, which transmit information at 50 Mbits/sec, is being installed at Los Alamos National Laboratory. The fiber optic strands that are being adopted by the communications industry will link two of the lab's technical areas. The cable is the longest ever installed at the lab. The fiber optics can operate efficiently without amplifiers (optical power boosters) required by other communications materials, such as coax cables and telephone lines.

These fiber optics come in lengths measuring one and a half miles. To string them three miles, they joined fibers by fusing them with heat, but lost very little power capability at the splices.

Data transmitted through such a system is passed through a multiplexer— a mechanism for changing the relatively slow input of computers and terminals and converting it, so that it can be transmitted through the fiber optics at a space-age speed. The process is reversed at the line's receiving end.

Only two of the six strands in the new system will be used initially. They will transmit information at the rate of 1.5 Mbits/sec. The remainder of the high-speed trunk line will be held for future expansion, possibly within six months.

The fiber optics line will be used primarily to link two computers in the lab's Implosion Physics Group and the Materials and Image Evaluation Group. Computer terminals in one group will talk to a computer in the other, which is already linked to the Laboratory's Central Computing Facility.

Super IC Speeds DP

Electronic circuits that resemble an array of 100 LA street maps printed on a thumb tack are in development at Hughes Aircraft Company. The high-speed, VHSIC chips will be more reliable and require less power than the ICs now in use.

Under a three-year, $26.5-million Phase 1 VHSIC contract with the U.S. Army Electronics Research and Development Command, Hughes' Electro-Optical and Data Systems Group will develop chips for use in a variety of high-speed signal processing applications. Additionally, the company will build a brassboard demonstration processor for the Army's Battlefield Information Distribution System (BIDS), containing VHSIC chips.

Slated for the 1990s, BIDS is a portable, two-way system for position location reporting and communications among Army troops. It will be an adaptive, or electronically alterable, communications system that will allow for an automatic increase in its data rate for less intense jamming situations.

Hughes' Research Laboratories in Malibu, CA, received a separate $8.1-million Army contract to develop a high-speed EB lithography system that will focus beams of electrons to "write" circuit patterns in submicron— less than $1X10^{-6}m$— dimensions. These circuit patterns will be converted into transistors and interconnects smaller than any now in production.

"In addition to advancing the state-of-the-art in this technology, the program will introduce these advances into fielded military systems as well as those on the drawing board," said Dr. Art Chester, manager of the Hughes program.

To design, lay-out and test the VHSIC chips, Hughes is developing CAD programs that will be able to describe a signal processor simultaneously at many different levels of detail.

"This capability will enable us to design a system so complex that it

is almost beyond human comprehension and then predict the system's performance under a variety of operating conditions. VHSIC will offer significant improvements in speed, reliability, power requirements and memory capacity for a processor regardless of the environment in which it is used- in the air, on the ground or in space," Chester said.

The semiconductor technology being used in the Hughes VHSIC program includes complementary metal oxide semiconductor (CMOS) and silicon on sapphire (SOS). Hughes Aircraft is the only contractor in the Department of Defense VHSIC program pursuing SOS technology.

"We feel SOS technology for VHSIC has significant potential for military systems," said Chester, "since, unlike CMOS, it is inherently hardened against radiation."

Software Expands EXORmacs Development System

Addition of two software packages that enhance the capabilities of Motorola's EXORmacs development system are available. The first is a series of 8-bit Macro Assemblers and a Linkage Editor that permit EXORmacs to be used efficiently for the development of 8-bit MPU/MCU programs based on Motorola's extensive complement of 8-bit μP's. Second is an EXORmacs-resident Fortran compiler which provides a new dimension to its support for the M68000.

The 8-bit Macro Assembler Series provides assembly language programming capability for the M6809, M6805, M6801 and M6800 families on the EXORmacs development system. The assemblers are available separately to support the individual programming requirements of each processor family.

Each assembler features macro instruction capability, evaluation of complex expressions, and inclusion of input from other disk files. In addition, the assemblers produce a symbol cross reference listing, and relocatable object on EXORmacs disk files for input to the 8-bit Linkage Editor.

The associated 8-bit Linkage Editor also runs on the EXORmacs development system, and takes the relocatable object module disk file produce by the 8-bit Macro Assembler Series as its input. The output of the 8-bit Linkage Editor can be a comprehensive listing and /or an absolute load module file in Motorola's S-Record format.

New Generation DOD Automatic Digital Network

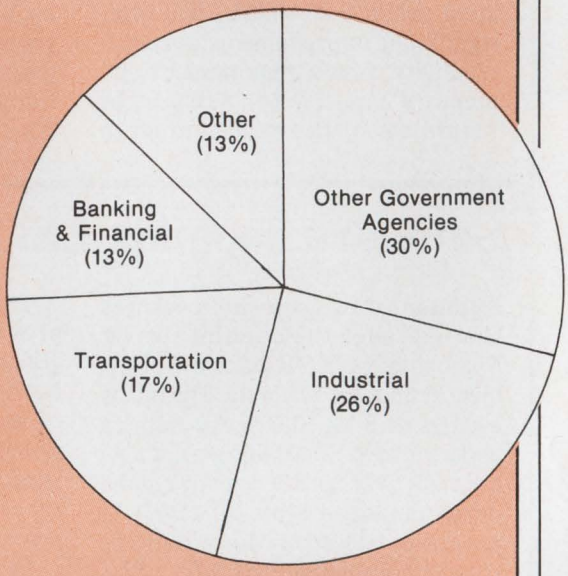
The Defense Department automatic digital network, commonly referred to as AUTODIN, which links U.S. armed forces installations around the globe, consists of automatic switching centers, packet switching and interconnecting trunk networks. A program now underway to modernize DOD Autodin networks will lead to equipment procurements by the armed forces.

Current-generation automated-message processing exchanges and automatic switching centers are approaching the end of their economic life. Phase-out will occur during the mid-1980's—no easy task, given the complexity and scope of the Autodin network. Autodin I represents a traditional store and forward message switching and generally serves as an automated teletype or narrative message exchange system. It is very human-interface oriented. The Autodin II packet switching system, however, is more oriented to exchanging information between computers and other high-speed machine devices.

DOD's intent is to interconnect Autodin I and II and operate them in parallel for several years. Simultaneously, the DOD plans to develop an integrated Autodin system whose network elements are all to be functionally standardized.

The key transitional element lies with a system, dubbed Inter-Service/Agency Automated Message Processing Exchange (I-S/A AMPE), and comprising a central processor, peripherals, and remote stations. There will be a minimal network requirement, specifically 92 I-S/A AMPEs plus the potential for an additional 14 systems by decade end.

Besides the basic system configurations, this network market also comprises some 1,600 remote displays, 650 remote printers, 975 input devices, and 325 remote magnetic tape facilities. The Autodin upgrade program is referred to as a unique vertical marketplace, where contenders vying for the business must understand the economics, politics, as well as the technology. Cost benefits to the DOD are estimated to exceed $20 million a year.



Over the next five years, there will be a $379 million spin-off potential generated by the Department of Defense's automatic digital network. According to Frost and Sullivan (report no. 919) most of this will go to industry and other government agencies.

Nor does the market potential end with the DOD. Other federal agencies and large-scale industry could also apply the technology. The non-DOD federal market potential is estimated at $115 million, with airline, trucking, and shipping industry networks alone, totalling $66 million. The marketplace stretches from the simple home computer terminal into nationwide networks.

Want more information?
Contact:
Frost & Sullivan, Inc.
106 Fulton St.,
New York, NY, 10038.

Independent Controller Manufacturers Surpass In-house Products

In-house development of controllers generally connot compete with the independent controller industry in most important respects, including price, quality, and technology, according to James S. Toreson, president of Microcomputer Systems Corp. (MSC) of Sunnyvale, CA.

"The in-house engineering team, in general, is not made up of experts in state-of-the-art disk controllers," Toreson said. "That can result in missed market opportunities. And the designs are often sub-optimal. This results in inadequate products which are not cost effective in their marketplace."

According to Toreson, the disk drive controller industry "hasn't often been reported on in industry research journals, mainly because it's been a marginal market." Many controller manufacturers have, Toreson said, "abandoned the business for greener pastures" over the last 10 years. Toreson believes this lack of credibility in much of the controller industry has led many companies to develop their own controllers in-house, even though there are many disadvantages.

According to Toreson, the advantages of dealing with an independent controller supplier are that: (1) being a controller expert, the independent will more likely come up with a product that meets the customers needs; (2) an independent is generally extremely responsive to customer requirements; and (3) an in-

dependent can deliver new designs more quickly than an in-house engineering department.

"As far as control is concerned," Toreson said, "manufacturing licenses are typically available, allowing the customer company to have control over the product (developed for them) and its destiny."

Toreson defined a controller as "a computing system element that controls the execution and post-originated transactions on peripheral devices and reports on their disposition." This definition takes into account many types of peripherals, including line printers, data communication equipment, tape drives, as well as disk drives and disk controllers.

The relevance of a controller, he said, is that it stands between the CPU and peripheral device. "In the case of a disk", he said, "it can either compete with or enhance several parameters in a computer, including system availability and reliability."

The original user of a disk drive controller, Toreson said, was primarily technically-oriented, but today's user is often non-technical. "Today's user is more solution-oriented," he said. "Major growth in the controller industry has been in the business area and distribution. Most of today's business systems are data base-oriented."

"Yesterday's systems were low performance," he continued, "with small memory and little emphasis on availability. Basically, the CPU was king and the systems were computation-oriented."

By contrast, newer controllers gone to high performance and large memories— both main and backing— with a heavy emphasis on availability. In this environment the peripherals are king. The computer is primarily used for information management and not computation.

One of the biggest advances in today's controllers, Toreson said, is the advent of intelligent controllers which can give users a number of benefits including enhanced operational functions, enhanced subsystem fault isolation, and, as a result, little or no down time.

"Intelligent controllers also provide users with flexibility, either from the standpoint of the host CPU or the storage device," Toreson said. "Both of those items allow the controller and the system to accommodate the inevitable change in the host and peripheral environment."

Toreson feels there is a need for sweeping industry-wide standards for controller design. "I feel it's very important that our industry start to adopt standards," he said, "because of the impact on compatibilities with the peripheral subsystem environment." According to Toreson, the industry has a number of "de facto" standards but almost no official ones. Standards are currently needed, he said, for the 5¼-inch Winchester drive bus, the intelligent controller bus, and the way drives should be handled by the controller.

Toreson concluded by discussing future technical and business developments expected in the controller industry over the next few years. "We feel the peripheral subsystems are going to be more important in the future in terms of their ability to function on their own", he said. "We'll see the merging of peripheral processors— basically, operating systems which are distributed within the host environment."

Other technological advances Toreson forecast include more multifunction disk controllers and back-end file processors. "From a controller technology viewpoint," he said, "advances and future prospects are inevitable. The question that remains to be answered is whether the controller manfacturers will participate in the opportunities available to them."

There's Nothing Magic In Japan

Charles E. Sporck, president of National Semiconductor Corp, recently told a select group of employees, "We're at war with Japan, not with guns and ammunition, but an economic war with technology, productivity and quality." To bring that message to all employees, National Semiconductor sent a team of four employees, representing a cross section of the company, along with an Emmy Award winning documentary film maker, to Japan to view firsthand what "made in Japan" really means. The result is "On The Line", a 37-minute documentary film focusing on the competitive challenge facing the American semiconductor industry in the '80s. Produced and directed by King Arthur Productions, the film was made possible by a grant from National Semiconductor Corp.

For the past several years, National was taking aim on productivity and quality issues through people programs such as QUEST and TAP. QUEST (Quality Enhancement Strategy) is the human side of management, relying primarily on people resources to improve the quality of their performance that influences productivity. A positive, highly productive work environment is created through "back to basics" strategies such as setting clear personal goals and objectives, involvement of employees and a continuous striving to improve. TAP (Target Analysis Process) is a tool that involves employees in productivity improvements. Used across several cultures and at all levels in the organization, TAP involves employees in identifying and implementing productivity ideas in their work area. "On The Line," an awareness heightening film, is the newest element of the company's total on-going program.

"On the Line" is now being premiered for all employees to heighten their awareness of the Japanese challenge and to prepare them for the next steps in reaching productivity and quality goals. The film, the first place winner in the Employee Information category at the San Francisco Film Festival and winner of the Cine Golden Eagle, will be made available to other American companies, organizations and network television, to assist others in meeting the foreign challenge.

Industry Unready to Standardize LANs

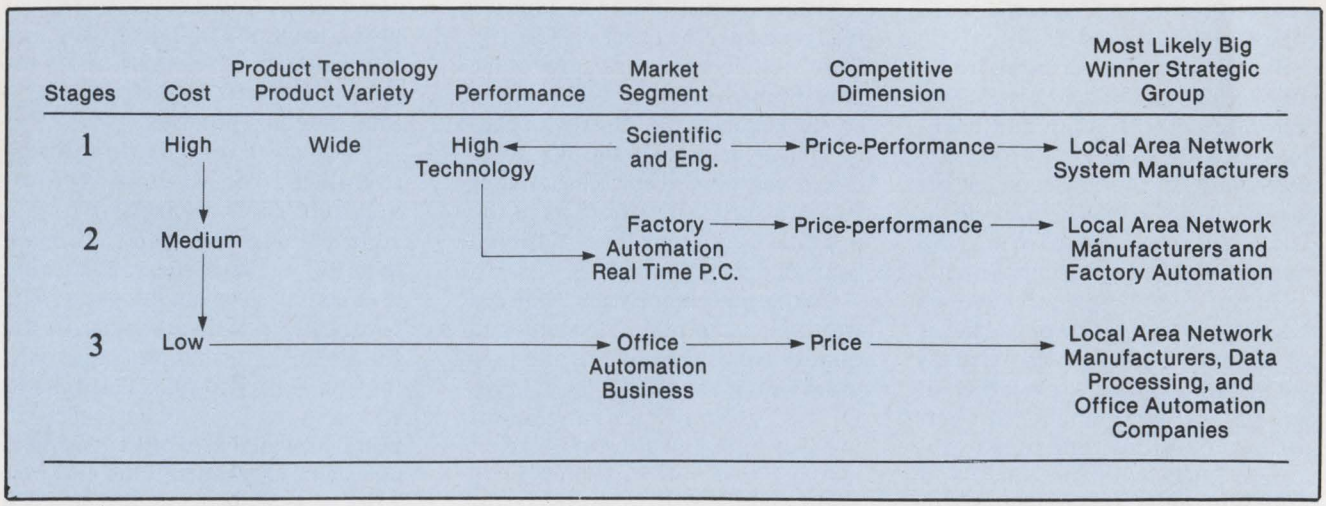
Some large companies may be going astray. Ethernet, the Xerox local area network company which is attempting to set the industry standard, has limited growth potential, according to a local area networks (LAN) study just released by Venture Development Corp. (Wellesley, MA). LAN market will reach$1billion/year level by 1990, making the market a major growth area. This emerging market might develop along any of three courses. First, there is the scenario in which a dominant low-cost system becomes standard and captures most of the market; further technological development would then tend to be stifled. Ethernet is attempting to set this standard. VDC thinks success is improbable; the system is somewhat primitive.

A second scenario, the most probable, predicts a technological jungle in which the marketplace is filled with different, innovative products, each fighting for its share on the basis of improved price-performance ratios. A dominant design will emerge after a shakeout.

A third possibility is that computer and office automation companies will use LAN as a competitive weapon to sell their own computer or office automation systems. Each local area network system would be incompatible with every other, so that a system user would be locked into a particular vendor's hardware (computers, terminals, WPs, printers, etc.). This is an irrational scenario which will hold back the development of LANs and retard market penetration.

The figure below shows the market evolution under the second scenario, which the VDC report ways is most likely. In the first stage of market development, there will be a wide variety of high-cost products. On price-performance, LANs will dominate engineering applications. LAN manufacturers will be big winners at this stage. As the price-performance ratio improves, because of technological advances from experience gained in scientific and engineering applications, LANs will penetrate the real time factory automation process control market segment with benefits to both local area network and factory automation companies. Futher reductions in price resulting from increased volume and a position further along the learning curve will next allow penetration of data processing and office automation markets, with all participants the big winners.

If DP companies like DEC continue on their present course, of locking into sub-optimal technology, they will be losers. Xerox would have much to gain if they could set an industry standard, built on Ethernet, early in the game, but probably cannot accomplish this. Companies which make computer and peripheral hardware would be well advised to sell LAN as part of an integrated system. They should develop networking software which would make their devices independent of the access method used by the local area networks. That way, they could take advantage of their large existing installed bases. Companies that are preparing to supply only hardware and software subsystems will have limited long-term growth and profitability due to the probability of forward integration by computer and office automation companies or backward integration by system houses and system integrators. Local area network system companies, like Ungermann-Bass, have excellent prospects if they provide a complete system to interconnect equipment from many manufacturers and develop local area networks with superior performance. If the scenario developed in which a local area network design with inferior performance became an accepted official or de facto standard, the market development would be less promising for local area network systems companies. However, potential users are more interested in obtaining an optimal system than conforming to an industry standard, making unlikely the long-term acceptance of a standard which unduly limits performance characteristics.



Local Area Networks could evolve along several different scenarios. The above represents the most probable, according to Venture Development Corp.

Flat Panels Compete With CRTs

Flat panel displays, until recently used mostly for small displays such as in calculators and watches, are now viable contenders for computer displays and TVs. The market for flat panel displays will push past the $500 million level by the end of the 1980s, up from about $50 million in 1981.

The "pocket" television has arrived. Four Japanese firms (Hitachi, Matsushita, Shinsu Seiki and Toshiba) have demonstrated prototype flat panel "pocket" TVs, and several will be in quantity production soon. Flat panel technologies will provide a more compact TV. However, Sinclair and RCA are working on modified versions of CRTs, in which the positioning of CRT components is rearranged to provide a relatively flat profile. Other companies are working on large-screen flat panel TVs to compete with present-day projection TVs. Commercial viability will be by 1985.

As for flat screens for the "executive workstation," one computer terminal (the Q1 Microlite) already has a flat panel display, but most computer terminals will continue to use the less expensive CRT type of display. Probably CRTs will continue to be the dominant display types for computer terminals, but flat panels will be used for portable terminals and also for executive workstations. The executive's desktop represents the most costly real estate around, and it makes sense to pay a premium for flat, compact, non-intrusive displays for higher echelon workers. About 15% of all computer terminals will use flat panel displays by 1985.

The military still sets the pace. More than half of today's flat panel display market is attributable to orders from the U.S. Army and Navy. Although militarized flat panel display terminals are very expensive, at $16,000 and up, they are much more likely to survive on a battlefield than more delicate and power-hungry CRTs. Magnavox, Photonics and Litton are leading suppliers of military flat panel displays and Sharp's Hycom subsidiary is making a major effort to become the leader in hand-held battlefield terminals utilizing an advanced form of electroluminescent flat panel. "Full-scale" procurement of portable battlefield terminals is forecast for 1984 or 1985. The Army is leaning toward electroluminescent displays rather than the heavier gas-discharge flat panels. In addition to their use in portable battlefield terminals, flat panel displays are also used on military ships and helicopters. There is a growing worldwide market for these applications.

An increasing requirement for "top of the line" electronic typewriters is expected to result in a growing market for flat panel displays in these and other types of office automation equipment, although most full-screen word processors will probably continue to be designed around the use of CRTs.

Want more information? Contact: *IRD at 30 High ST., Norwalk, CT, 06851*

CONTENDERS FOR THE NEW FLAT-PANEL DISPLAY MARKET

LCDs
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- Amperex
- Beckman
- Crystaloid
- Epsom-America
- Fairchild C&I
- General Electric
- Hamlin
- Hitachi
- IEE
- Kylex
- Ladcor
- Matsushita
- Racal
- Sanyo
- Sharp
- Sony
- Stanley
- STC
- Thomson-CSF
- Toshiba
- UCE

DC PLASMA
- Beckman
- Burroughs
- Cherry Electronics
- Dale Electronics
- Lucitron

TFEL
- Aerojet
- GTE
- Honeywell
- Hycom
- IBM
- Rockwell
- Sharp

TFT
- PanelVision

LEDs
- General Instrument
- Hewlett-Packard
- Litton Systems
- Sanyo

AC PLASMA
- Control Data Corp.
- Dale Electronics
- Electro Plasma
- Fujitsu
- IBM
- Interstate
- Magnavox
- NCR
- Norden
- Photonics
- SAIT

FLAT CRT
- RCA
- Sinclair
- Zenith

VACUUM FLUORESCENT
- Chemetrics
- Futaba
- IEE
- Ise
- NEC Electron

Over fifty companies compete in the flat panel display market, according to International Resource Development, Inc.

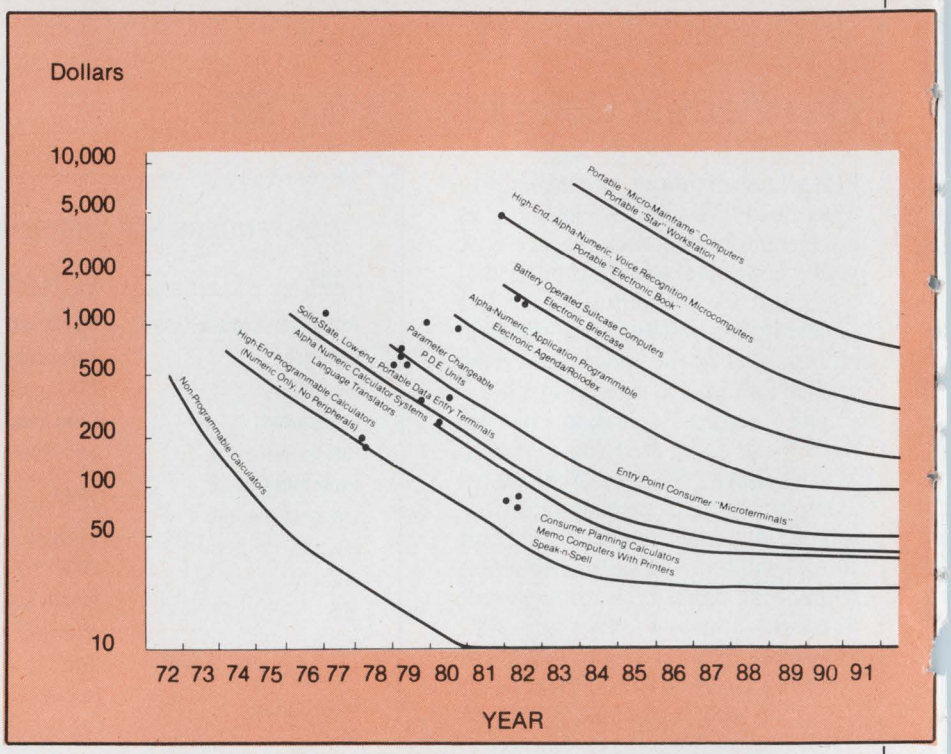
Portable Computers Key to Productivity

Clocking in and out has long been part of many blue collar jobs. In factories and in offices, workers have been accustomed to being timed (keystrokes per hour of data entry, units assembled per hour, etc.). Field workers have been much more difficult to monitor, however, due to the

lack of suitable equipment. Postal routes, meter reading routes, industrial and agricultural field work, etc. have typically been characterized by "a reasonable day's work" assigned by the supervisor.

Software-intensive portable products (SIPPs) can measure and increase field workers' productivity, according to a new IRD (Norwalk, CT) study. There is a large market for the use of portable products capable of monitoring field personnel performance as a by-product of the use of the equipment for data entry or access to information and intelligent field processing.

SIPPs will play an increasing role in the fast moving "computerization" of society, ultimately moving past those users who need portability to carry out their jobs to those who simply want the ease, convenience, and status of such devices. Therefore, a substantial consumer market will grow out of the industrial, commercial, and military markets that exist today.



This graph depicts the decrease in price that portable computers will experience over the next ten years (source: International Resource Development, Inc).

User Friendliness Necessary

A great many factors will contribute to the commercial success of portable computers: size, obviously, and self-suffiency; intelligence; memory; price; and, perhaps most importantly, so-called "user friendliness." Since SIPPs are generally geared toward non-technical users, such as salesman or executives, the study concludes that "the man/machine interface of any successful product must be of the highest quality. The computer will have to react to the user in much the same way that another human being would— it will have to make sense or it will be rejected." The advent of widespead voice-recognition and synthesis will go a long way in achieving this end, as will careful planning of keyboard design (QWERTY vs. alphabetical) and display type (LED vs. LCD).

Similarly, provision will have to be made for a certain amount of user programming. One successful approach, according to the report, is to provide "a simple natural-like language through which the user can describe control structures and system functionality." While inefficient from a systems perspective, it will perform tasks in a manner desired by the user.

By definition, SIPPs must live and die by their software, especially when trying to build in such features as just discussed. There are problems, however, starting with the high cost of software labor, rising in some places by as much as 16% annually, and the chronic shortage of software programmers, currently estimated at more than 50,000. By 1985, software cost will outweigh hardware counterparts by 3 to 1. Steps taken to lower costs include unbundling of software from hardware in the hopes that the customer will get hooked on one company's products due to hidden costs of buying from other suppliers (cheap camera, expensive film). Software maintenance, too, has come into its own as a legitimate product, with users paying for support rather than risk "technological obsolescence." In fact, before much longer software maintenance contracts will be as common as service contracts on office copiers and other machinery.

On-line software sales will become increasingly common by the decade's end, as users become more familiar with electronic banking and other remote transaction processing. Further, by 1985 approximately 80% of all software package sales will be for applications software.

Pricing will be largely irrelevant for business, but consumers will look for bargains. Ultimate size of the business market of SIPPs will be relatively independent of the prices charged for the units. Those thought to be too low will be viewed with suspicion, particularly regarding vendor support. Payback periods used in particular industries should be used here. Profits will be higher in the business sector even though growth will be slower, due largely to lower marketing and distribution costs for the larger users.

Consumers, on the other hand, will be looking for more and more functions at the entry-level prices. Ease of use ranks high in determining consumer acceptance, and so most products for the next few years will probably move toward terminals used in conjunction with cable TV networks. The truly portable consumer computer will put in its appearance later in the decade.

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Write 23 on Reader Inquiry Card

N-Key Rollover Implementation Updated

W.V. Subbaroa missed the main issue in his note on N-key rollover (''Designers' Notebook,'' November, 1981). Simply stated, the point he makes is that N independent binary variables (e.g. switches) must be encoded into N binary variables (e.g. logic signals) to avoid losing information. The remainder of his article discusses a way of accessing these N signals using multiplexing.

But the context in which N-key rollover is almost always discussed is that of a keyboard, and the important information is not only ''which switches are closed (pressed),'' but ''which switches have been pressed and in which order.'' For example, a touch-typist typing the word ''the'' might well overlap typing ''t'' and ''h'' keys, and the typewriter or terminal must be able to recognize that the ''t'' came first. Simple combinatorial readout of the key states, as with Mr. Subbaroa's N sense signals, is not sufficient.

Thus the essential characteristics for a system to implement N-key rollover are (1) a means of determining when a key *has been* pressed, rather than just whether each key-contact is closed; and (2) memory for storing a sequence of key-closures, in the order in which they occur, until the receiving system can process the information.

A common, but by no means the only, way to implement these features is shown in **Figure 1.** The keys are connected with multiplexers, as in Mr. Subbaroa's example, thus making the state of one particular selected key available at the multiplexer output. Free-running scan logic sequences through all keys and, in parallel, through corresponding locations in a memory, which holds a bit for each key that represents the previous state of that key. When the logic finds a key closed and the corresponding memory bit indicates that the key was previously open, it considers this a new key-closure and generates the appropriate output signals. If key-closures can come more rapidly than the receiving system can accept them, a FIFO memory may be used as shown to store key data temporarily.

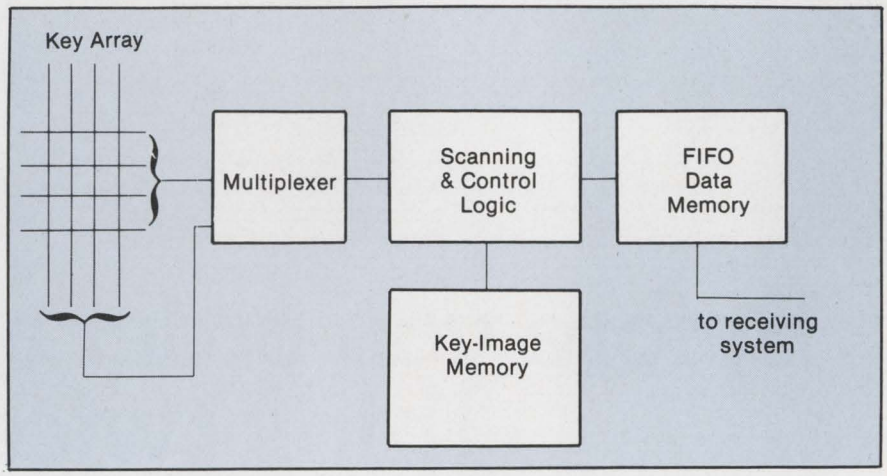

Figure 1: This is a common way to implement the features of N-Key rollover.

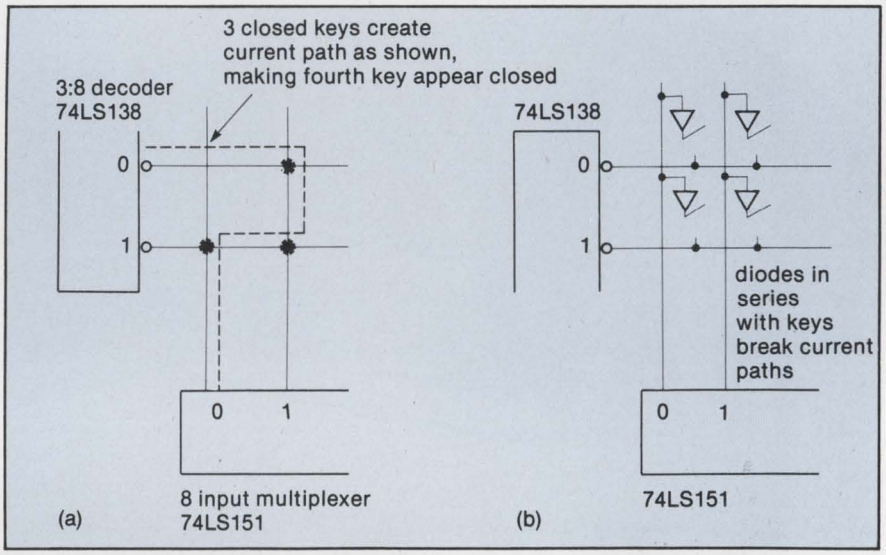

Figure 2: Subbaroa's circuit does not implement true access to 64 independent keys.

For this scheme to work, the rate at which the keys are scanned must be significantly faster than that at which key closures occur. Additional features such as key debouncing may also be implemented in the scan logic. Of course, if a μP or computer is available and not otherwise busy, the scan functions may be implemented in software.

Incidentally, the keyboard circuit as shown in Mr. Subbaroa's article does not implement true access to 64 independent keys. In **Figure 2 (a),** three keys simultaneously closed as shown create a sneak path by which the fourth indicated key appears closed although it is open. This can generate false outputs. **Figure 2 (b)** shows a configuration in which diodes in series with the keys eliminate the sneak paths. This configuration is commonly used in keyboards with N-key rollover.

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Effects Of Ground Spacing On High-Speed Digital Signals

The trend in modern digital systems has been toward increasing information density. As information density grows, so does the use of interconnections. Because of digital system speed and density, the transmission properties and geometry of board-to-board interconnections must be considered.

Transmission Properties

The passage of digital signals within a system is governed by high frequency transmission line properties. These properties depend on the interconnection path geometry and material which affect the capacitance and inductance of the pathway. Related factors are propagation velocity, effective electrical length and characteristic impedance.

For purposes of this discussion, propagation velocity is essentially fixed at an effective speed somewhat less than the speed of light in air, due to the signal traveling through dielectric material as well as air. This means that the effective electrical length of interconnection paths is a major determinant of the maximum rate of signal transfer in a system.

The characteristic impedance of a transmission line also affects signal rates, and is determined by its geometry and the properties of the materials through which the electromagnetic energy of the line flows. Assuming that line losses are negligible, which is reasonable for board-to-board interconnections, the characteristic impedance has a real value. Changes to the physical structure of the transmission path can alter this impedance, causing ringing and resulting in signal delay or even loss of proper transmission.

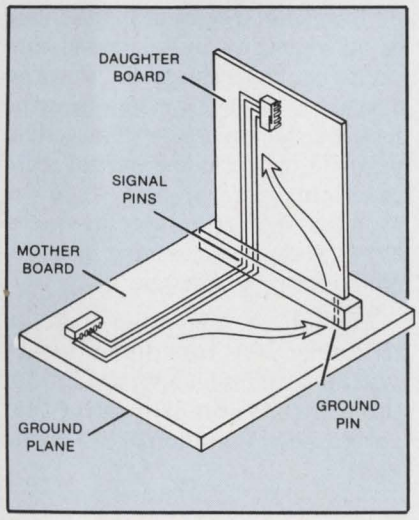

Figure 1: Board geometry illustrates typical board-to-board interconnections as found in most system applications.

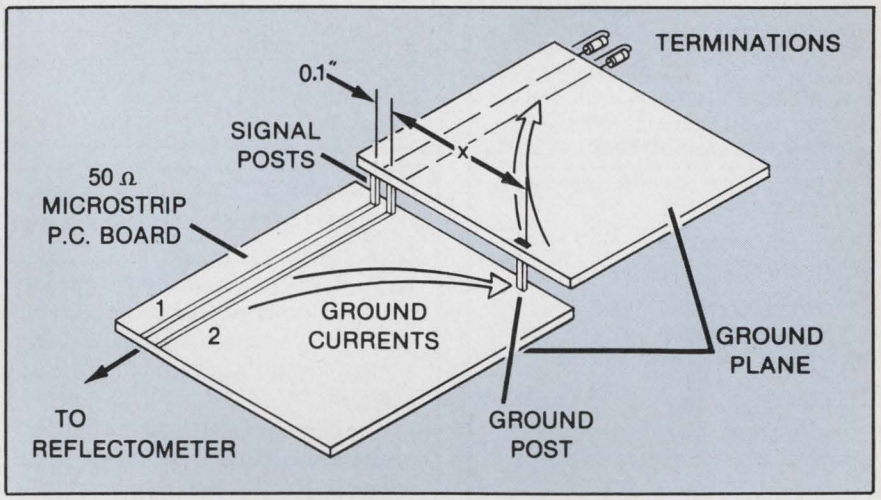

Figure 2: A board-to-board interconnection model portrays signal-to-ground spacing effects and how they may vary under different conditions.

Effects of Geometry

Geometry determines the distributed inductance and capacitance of a system. Changes in inductance and capacitance are related to characteristic impedance and also influence crosstalk.

For a transmission line in air or other homogeneous medium, it can be demonstrated that any change in geometry will proportionately inversely affect inductance and capacitance. For transmission lines with mixed dielectric media, such as plastic and air, capacitance and inductance are not exactly reciprocal but still inversely related.

Transmission paths associated with board-to-board connections always require two conductors. Capacitance is always distributed between these two conductors, and inductance is always associated with two conductors carrying signal and return currents. Generally speaking, increased coupling between signal and ground due to a change in geometry will increase capacitance and decrease both inductance and characteristic impedance.

The foregoing principles can provide controlled signal transmission when applied to board-to-board interconnections. There are numerous types of interconnections available, including card edge connectors and two-piece connectors based on .025" square post technology in single- and multiple-row configurations. Cables such as ribbon, flat etched circuitry, transmission cable and coax are also used as interconnections.

The performance of board-to-board interconnections as transmission media depends to a large degree on the assignment of signal and ground positions in the connector as this determines capacitance and inductance.

Geometry similar to that found in many board-to-board interconnections is shown in **Figure 1.** Ground connections are often limited in number and placed at the ends of the connector. Although the physical contact length of the connector may be short, the effective electrical length is much longer due to the long ground

Applications Notebook

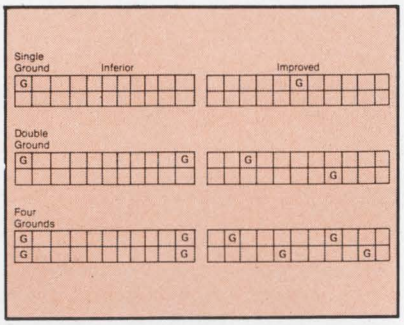

Figure 3: Improved ground placement, as portrayed here, are for a two-row connector. Simple rearrangement increases performance and keeps costs down.

path. The signals farthest from the ground connections suffer the greatest degree of degradation. Those closest to the ground are least affected.

The degree of transmission impairment should be evaluated with respect to the performance requirements of the system. Signals with faster rise-times may be degraded by a circuitous ground path while slower signals would not be disturbed. Fast logic families may require an improved board-to-board interconnection scheme.

Test Fixture

To demonstrate the effect of signal-to-ground spacing, a board-to-board interconnection model, as shown in **Figure 2,** was used. Two printed circuit boards with two signal traces were interconnected using .025" square posts attached to the signal lines. A ground post was placed a variable distance, X, from the signal lines. As distance X was increased, the impedance and effective inductance increased greatly. In addition, crosstalk pulse amplitude and width also increased substantially. Thus, ground connection spacing may cause noise which has sufficient width and amplitude to interfere with adjacent circuits. Crosstalk is compounded when many signals switch simultaneously.

Interconnection Design

Most board-to-board interconnection devices allow the arbitrary assignment of signal and ground connections. The performance of a card edge or two-piece connector can be tailored to the application by suitable choice of the number and placement of ground connections. Many factors will influence the number of grounds needed, such as the rise-time and noise immunity of the logic used, the number of interconnections in a signal path, the desired level of system reliability and the number of signals being interconnected. Examples of improved ground placement are shown in **Figure 3** for a typical two-row connector. Simple rearrangement will increase performance at no cost in density or contact positions. The maximum spacing from any signal to ground should be minimized, and critical signals should be adjacent to a ground.

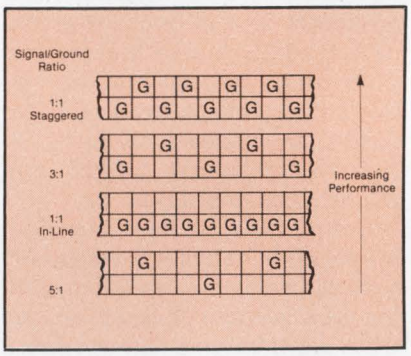

Figure 4: As shown here, grounds are distributed at regular intervals. As expected, the more grounds, the better the performance.

Figure 4 shows arrangements which have grounds distributed at regular intervals throughout the two-row connector. In general, the larger the number of grounds, the better the performance. The resulting decrease in signal density and increased connector line requirements may have no alternative in some systems using the fastest logic families. A small system designed to preclude electrical noise problems may work with fewer grounds; a large system may need more. A case by case analysis is required for proper design.

The success of board-to-board interconnections for contemporary systems requires an appreciation for the transmission properties that govern the propagation of fast digital signals.

Staff Report, Amp Inc., Harrisburg, PA 17105.

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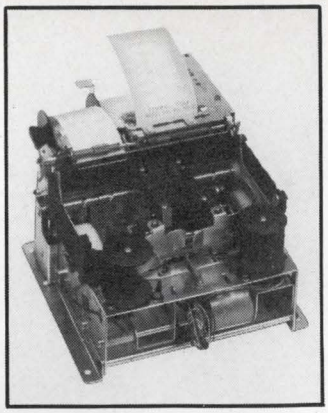

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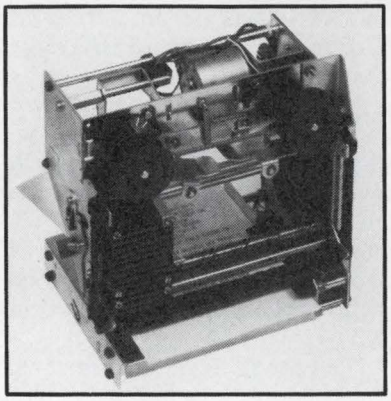

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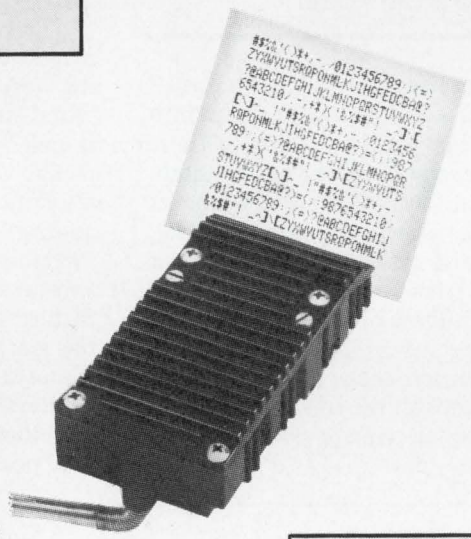

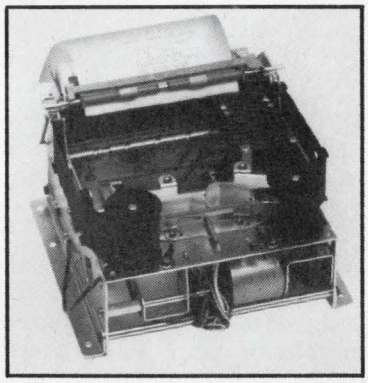

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- Easy Top Paper Insertion
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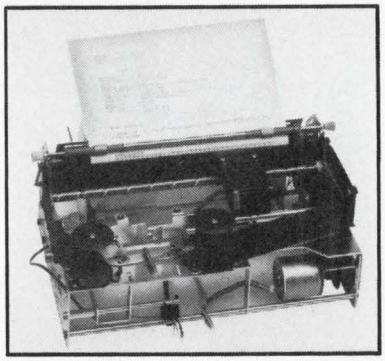

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- Bi-Directional Printing
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Write 21 on Reader Inquiry Card

High Intelligence Key To Printing Terminal Growth

Staff Report

Printing terminal markets continue to expand, with outlooks favorable for intelligent units and daisywheels.

Teleprinters, though predating computers by 30 years, are now going through rapid evolution. Increased intelligence will increasingly alter more terminals.

Dumb, Smart and Intelligent

Dumb teleprinter terminals generally have no intelligence of their own and rely on the host computer for instructions. Smart teleprinters have editing capabilities. These editing features consist of the capability to enter data, store it locally, make corrections or rearrange the data and send it to the host unit. Intelligent teleprinter terminals are user-programmable. They have a processor capable of performing many functions normally handled by the host unit. Intelligent teleprinters have all the editing features found on smart terminals plus the additional capacity of creating their own editing functions through their processor. Another feature normally associated with intelligent teleprinters is the ability to drive auxiliary devices and other terminals.

With the increased use of word processing as a teleprinter application, smart and intelligent teleprinters will be much more in demand than they have been in the past. In fact, by 1985, 86.4% of teleprinter shipments will be used for word processing. For this reason, certain letter quality teleprinter manufacturers have plans to increase the intelligence of their word processing teleprinters.

Other companies are trying to beat out the teleprinter manufacturers by offering teleprinter "enhancement" kits that add intelligence to dumb teleprinter terminals. One of these companies is Tri-Data of Mountain View, California. They offer a product that adds forms control, text editing, unattended data collection and other capabilities to KSR teleprinters. Although these products can enhance the large installed base of dumb teleprinter terminals, they cannot provide them with the full capabilities of intelligent teleprinters, which is where the largest growth is. As a result, Tri-Data's products will not directly compete with smart and intelligent teleprinters.

Daisywheel Teleprinters

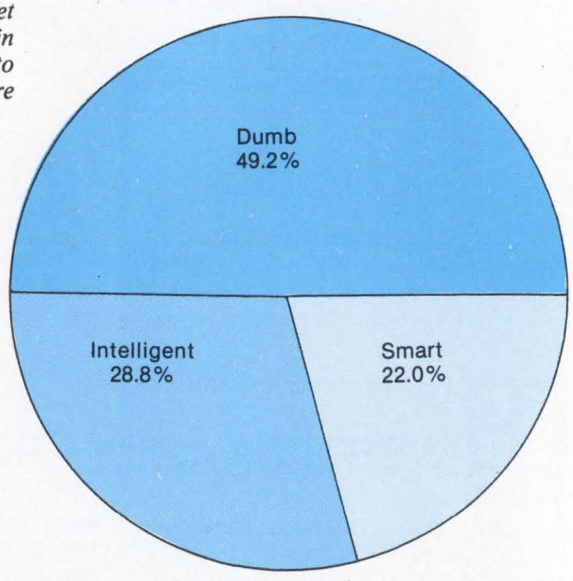
Although letter-quality teleprinters have a rather small share of the current teleprinter market, they will grow substantially over the next five years. Growth of fully-formed character teleprinters will exceed 15% through 1985.

The growth in fully-formed character teleprinters is a result of the growing word processing market. By 1985, word processing will be the most popular application for teleprinters.

The U.S. fully-formed character teleprinter market is headed by three companies who comprise over 50% of 1980 fully-formed character teleprinter shipments. Certain Japanese manufacturers are also strong contenders in this market. It is rumored that they are manufacturing letter quality teleprinters that are faster and cost less than those manufactured in the U.S.

A possible threat to the daisywheel

Figure 1: Teleprinter market share by intelligence level in percent of dollars, according to research data from Venture Development Corp.



Information contained in this article was provided by Venture Development Corp, 1 Washington St., Wellesley, MA, and by Creative Strategies International, 4340 Stevens Creek Blvd, San Jose, CA.

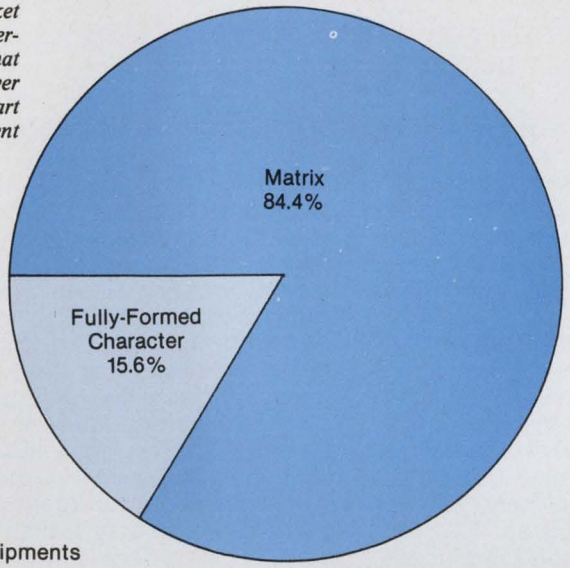


Figure 2: Teleprinter market share by character type in percent of dollars shows that matrix teleprinters hold over four fifths of the market (chart courtesy Venture Development Corp).

teleprinter market is posed by high resolution dot matrix and ink-jet technologies. Both are still in the early stages of development and will require a lot of R & D before they can print reliably at correspondence quality.

High-resolution dot matrix teleprinters will require large matrices to fill the spaces left between dots. Currently, this is being done with multipass units, such as the one manufactured by Sanders Technology, where the print head passes over the paper four times so that the dots overlap, forming a full character. The problem with this method is that by passing over a line several times the print speed is reduced to that of a daisywheel, therefore producing a character of lesser quality at the same speed.

Ink-jet technology looks very promising, with growth rates of over 400% quoted by industry analysts. Siemens Corp. has an ink-jet teleprinter on the market that is doing quite well printing at 200 cps, but the resolution is not high enough to compete with daisywheels. The most popular ink-jet unit is the IBM 6640, with a resolution of 240 dots/inch. This printer is already being used on word processing systems. There are many new patents out on ink-jet technology, and the printer industry is heavily into R & D. The current problems with ink-jets have to do with the plumbing and ink clogging up the nozzles of the print heads. This makes for a very unreliable product at the moment which cannot compete with daisywheels in the area of reliability. There is a good possibility, though, that these problems will be overcome in the next five years, at which time ink-jets and high resolution dot matrix teleprinters will begin cutting in on the daisywheel teleprinter market.

Distributed Teleprinters

By 1985, worldwide sales of communicating keyboard printers, or teleprinters, will exceed $1 billion, reflecting a compound annual growth rate of 21.2%. During the same forecast period, unit shipments will grow at a rate of nearly 32%, compounded annually. Here are some projections:

- The emerging home market will expand at over 50% per year until about 1987, after which the growth rate could explode.
- A notable percentage of keyboard/printer equipment for the home market supplied by public news services and other network service vendors will be used teleprinters that were in service before 1980.
- New very-low-cost teleprinter models will be entering the market.
- Over the next five years, a cumulative 18% of new teleprinter products and installations will be related to electronic mail, office automation, and interoffice message systems.
- Unit shipments of medium-value-added (MVA) teleprinters—those with editing capability—will see a compound annual growth rate exceeding 43% through 1985.
- A new breed of entrepreneurial firms, like the anticipated Japanese entrants, will challenge established vendors by offering high-quality, reasonably priced specialty products.

The Industry

Participants in the teleprinter industry tend to specialize in teleprinter products and product differentiation by adding customized features. This trend has been made possible by the technological advances available—for example, magnetic bubble memories, fiber optics, μPs, large scale integration, non-impact print techniques, protocol converters, compression technology, and distributed data processing. The future holds an even greater promise of technological advancements.

The most implemented applications for teleprinters are still in the areas of data entry and retrieval, including inquiry and update of files, transaction processing, and batch processing. WP-related activities are new to this area. Over the next five years, teleprinter growth will surge in the area of enhanced information transfer. The bulk of increased applications will be made up of automated electronic mail activity, intelligent data entry, and network oriented data transmission. Other information transfer areas to be developed for teleprinters are facsimile transmission and, possibly, teleconferencing.

Teleprinters and video display devices will evolve toward separate markets; teleprinters will incorporate LED's/ LCD's to facilitate input, reading & editing.

End users will be encouraged to use teleprinters by such factors as new pro-

Remote Line Printing Doubles Throughput

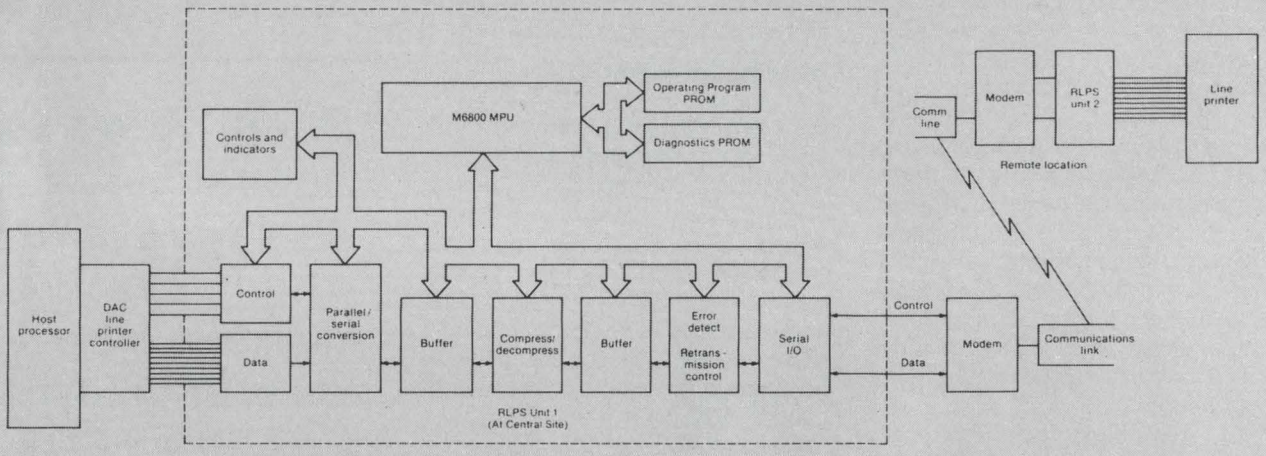
The need for remote printing from a minicomputer is an increasing evolutionary trend. All of today's minicomputers support low speed teleprinters off their communications ports. However, as user requirements for higher volume printing at remote sites grow, these teleprinters are pushed beyond their duty cycles. The obvious solution has been to replace the teleprinter with a line printer.

The conversion to a remote line printer is not without its difficulties. First, minicomputers are poor communicators, experiencing host processor degradation that can reach 30% when a line printer is installed at a remote site (every data bit has to be sensed before transmission through the communications port). Secondly, the maximum speed an RS-232 connected line printer can achieve is 500 LPM with a costly 9600 baud dedicated line. Thirdly, unless expensive intelligent modems are used for error detection/retransmission, it is necessary to retransmit an entire print job when a line fault occurs.

An alternative solution to high volume distributive printing, introduced by Digital Associates (1039 E Main St., Stamford, CT 06902, is the Remote Line Printer System (RLPS). What makes the RLPS unique is that it operates off the minicomputer's *print port* instead of the communications port. The RLPS assumes the burden of the communications protocol/overhead formerly placed on the minicomputer and accepts data in the more efficient parallel mode, rather than in a serial mode. The result is the elimination of CPU degradation caused by printers operating from the RS-232 port. The RLPS also employs data compression and block mode transmission which can more than double the throughput speed of RS-232-based line printers. As a result of this throughput increase it is possible to reduce the line speed requirements with the RLPS: A 2400 baud voice grade line for 300 LPM, a 4800 voice grade line for 600 LPM, and a 9600 baud dedicated line for 1000 LPM.

The need for intelligent modems is eliminated because error detection/retransmission are standard on the RLPS. When a line fault occurs, only the block of data in error is retransmitted, again yielding the line use savings.

The RLPS is currently 100% plug compatible (no modifications to existing hardware/software) with DEC, Data General, IBM Series/1 and Prime minicomputers. Compatibility with additional minicomputers will be announced in the near future.



duct functions, the availability of public data networks, and the rising cost and reduced efficiency of traditional communications means (i.e, U.S. Postal Service, telephone, and travel). As teleprinters, like CRTs, become increasingly affordable, end users will rely on them more and more for data entry, information transfer, and network information processing.

The Market

The market for keyboard teleprinter units has increased from an installed base of 641,000 general-purpose teleprinter terminals in 1976 to about 2,142,000 teleprinter units by the end of 1979. This represents a compound annual growth rate of nearly 50%. However, in view of the unique and new markets opening for teleprinters within the next decade, the current installed base remains only a small fraction of the long-range potential.

CSI segments the market for interactive communicating teleprinters in two ways; product offerings are divided in terms of (1) functional value added, and (2) the applications environment. With regard to the first division, high-value-added (HVA) units generally offer full editing capability and some degree of user-programmability. Medium-value-added (MVA) terminals have text editing capabilities. Low-or-no-value (LVA) terminals feature neither editing nor programmability. This last segment comprises the majority of terminals in this report, both currently and projected for 1985; however, by 1985 the MVA group will be nearly as large as this one.

With regard to the second division, the four segments of the applications environment are network, office, home and business applications. Spurred by growth of distributed data pro-

cessing, teleprinter demand in network applications will be the fastest growing, with a compound annual growth rate of over 60% by 1985. Used in conjunction with either internal corporate networks or public business and consumer data network services, these terminals will be predominantly LVA units.

Technology

The rapidly changing technologies within all areas of the electronics industry affect the constantly changing teleprinter industry. Teleprinter pricing is mostly a function of these changing technologies. When design, development, and production of μPs cost less, these lower prices are passed on to the customer as a matter of course. In addition, the range of applications available at that low cost is constantly being enlarged. Modems or multiplexers are an integral part of the teleprinter configuration used in distributed applications. Integral modems are constantly contributing to higher functions, while reducing bulk and separate attachments.

Technical Advances (new print technologies, integral modems) and market changes contribute directly to printing terminal growth.

While CRT devices have been thought of as seriously contending for the attention of teleprinter users, teleprinters and video display devices will probably evolve toward separate markets. Instead of having a full-size CRT display in conjunction with teleprinter activities, a 2- or 3-line LED/LCD display will be incorporated to facilitate input, reading and editing of material prior to transmission.

Competition

The existing three dozen U.S. suppliers of teleprinter terminals with KSR and communications capability are expected to be joined by at least a dozen more by the end of 1985. Competition in the teleprinter marketplace of the 1980's will be based on price/performance, customization, and innovative marketing to teleprinter users.

Technological expertise and creativity in implementing new technological developments will be a key characteristic of vendors who maintain significant market shares over the coming years. Prices are going down relative to current inflation and the increased functions available at a given price are increasing.

Most important will be the vendor firms' ability to market teleprinter products to the non-technical markets, such as the office segment and the home segment. The emerging retail outlet for computer products is the most innovative and promising of the new marketing distribution channels.□

Dedicated Graphics Computers Boost System Efficiency

by James A. Lohr

The advent of low-cost memory and high-performance μPs now make it possible to develop a new type of computer: the graphics computer.

Dramatic advances have been made in the area of color raster displays. Memory and color CRT technologies are now such that displays with spatial resolutions of 1024 x 1024 elements are not only possible but economically feasible. Some applications of computer graphics require color and intensity (z-axes) resolutions up to one part in 2^{24}. Indeed, the requirements for display resolutions of up to 1024 x 1024 x 24 are relatively commonplace. This demand for more resolution has closely followed the semiconductor memory price decrease.

These technological advances have created a new set of problems which can be both easily and economically solved by combining the features of a display generator with those of a general purpose computer into a single device. The resultant system would have capabilities far greater than the sum of the parts.

Sequential Scanning

There are two basic methods used to define a computer graphics picture. The first uses data generated by a sequential scanning device, such as a TV camera, by Landsat satellite, or a tomographic, facsimile, or X-ray system. These devices generate a word of data to describe each element of the picture. This smallest picture element is called a pixel. The spatial and z-axes resolutions vary with each application, but 1024 x 1024 x 24 bits is not uncommon. This requirement points to the first problem encountered: The graphics computer must have a massive data base.

A single 1024 x 1024 x 24 bit picture requires 24 million bits of storage. To store this amount of data, general purpose computers use a virtual memory system where small amounts of real memory are made to look larger by paging data to and from a disk memory. As a result, a significant burden is placed on the computer to process a single picture. The result is poor utilization of available system resources. In most systems, the output device for this image is a CRT which uses a raster-scan refresh display generator. The display generator must have a bit-map memory to store one picture in order to keep the CRT screen refreshed. By combining display generator and computer technologies, that refresh memory is

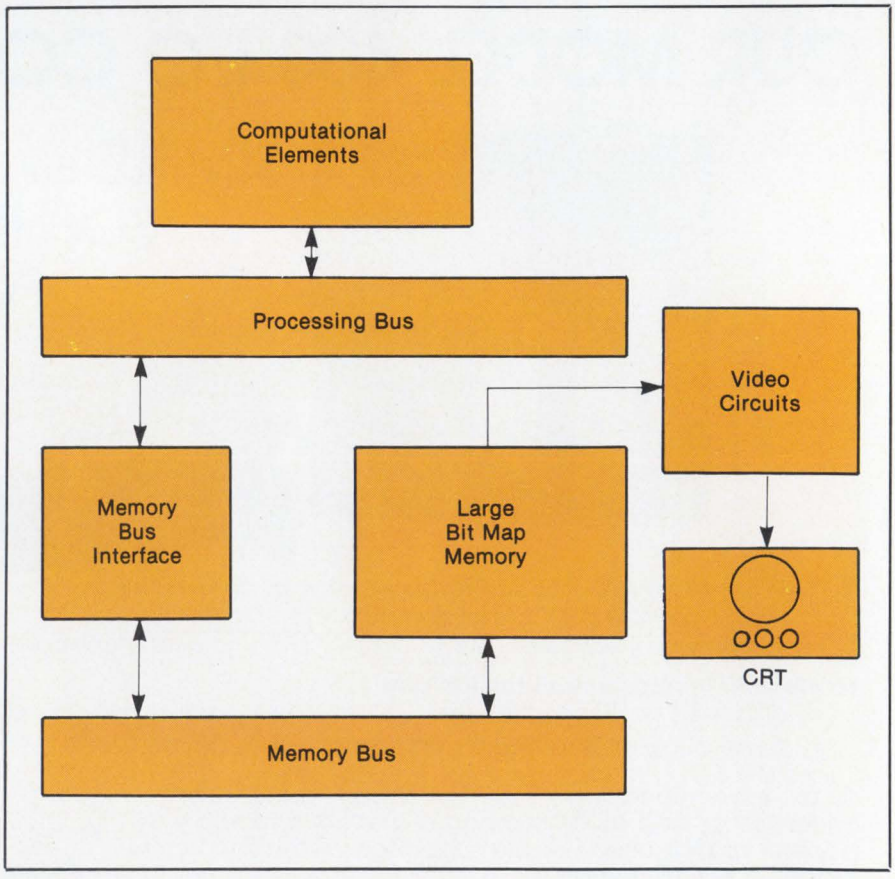


Figure 1: A dual-ported memory in a dual bus is mandatory for graphics computers, as shown in this simplified diagram.

James A. Lohr is Vice President of Special and Advance Systems at Aydin Computer Systems, 414 Commerce Dr, Fort Washington, PA 19034.

directly available to the computer. Thus, a fundamental requirement of the graphics computer is that *a large amount of memory should be directly addressable by the computational elements.*

A 1024 x 1024 picture, refreshed 30 times/sec requires one pixel (or word of data) to be read from refresh memory and presented to the CRT, through video processing circuits, every 24 ns. If the z-axis resolution is 24 bits, the effective transfer bandwidth is 1 bit/ns. It is therefore not adequate simply to add large amounts of memory to a general computer architecture. Because a raster CRT is refreshed sequentially left-to-right, top-to-bottom, there are several memory commutation methods that work well. One such system requires that the refresh memory be organized such that 64 sequential pixels are read simultaneously in one memory cycle. With a 24-bit z-axis, 1536 bits/word are required. Because 64 pixels are read in one memory access, that refresh access must occur every 64 pixel times, or once every 1.6μs. Current high density MOS memory technology allows memory cycles in the order of 500 ns. This feature allows the basic bit-map refresh memory to be multiported in order to render to the computer two accesses for each refresh cycle.

Because the bit-map memory is busy refreshing a CRT one-third of the time, it is advantageous to isolate it on a bus separate from the bus used by the computational elements. Thus, simultaneous activity can occur on both busses. The refresh process would therefore never be interrupted (interruptions would create objectionable flashes on the screen due to data loss), nor would other elements of the system which are connected to the processing bus be slowed down. Another requirement of the graphics computer is that it have *dual-ported refresh memory in a dual bus architecture* **(Figure 1).**

A problem unique to raster devices using bit - map memories is "common dot erasure" in which common bits between primitives are erased.

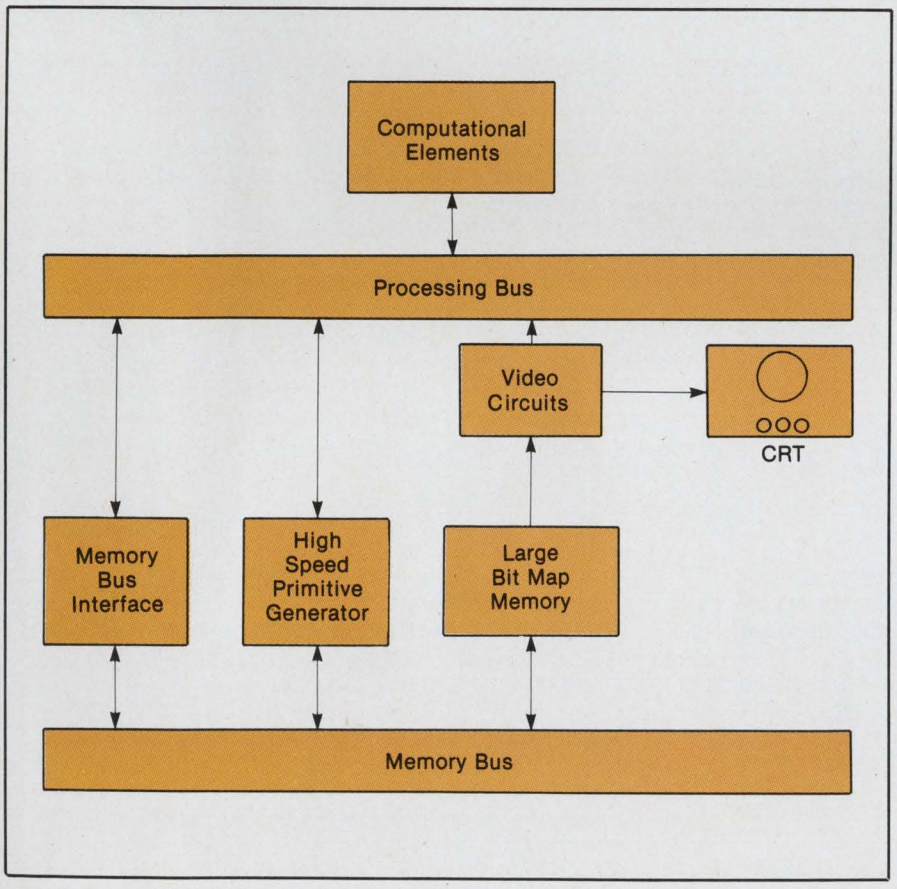


Figure 2: "Rasterization" process, as portrayed in this functional block diagram, shows bidirectional flow.

Graphic Primitives

The second method of describing a picture, and the more common, uses graphic primitives (vectors, circles, arcs, polygons, etc.) and primitive attributes (line style, line thickness, character size, intensity, etc.) to define an image. Raster technology also allows surfaces to be solid as well as wireframe, and permits pictures to be displayed in color, or as multi-intensity monochrome images.

These primitives and their attributes are then converted by a "best fit" algorithm to the resolution of the bit-map memory and are then written into the indicated locations of that memory. This process is called "rasterization." In real-time applications rasterization must be carried out by very high speed processing elements so that system throughput is as high as possible. The graphics computer should therefore *possess special purpose hardware to rasterize primitive commands very rapidly* **(Figure 2).**

A problem unique to raster devices using bit-map memories is "common dot erasure." When two or more primitives intersect (i.e., two vectors cross) and one of the primitives is deleted, the bits that are common between the primitives are also erased, and "holes" are left in the remaining primitives. One way to solve this problem is to write static (background) data into one set of bit-map memories and dynamic (foreground) data into another set of memories and then combine the outputs. This solution is expensive because it requires extra memories and it is not foolproof in the case where dynamic data intersect.

Another solution to this problem is

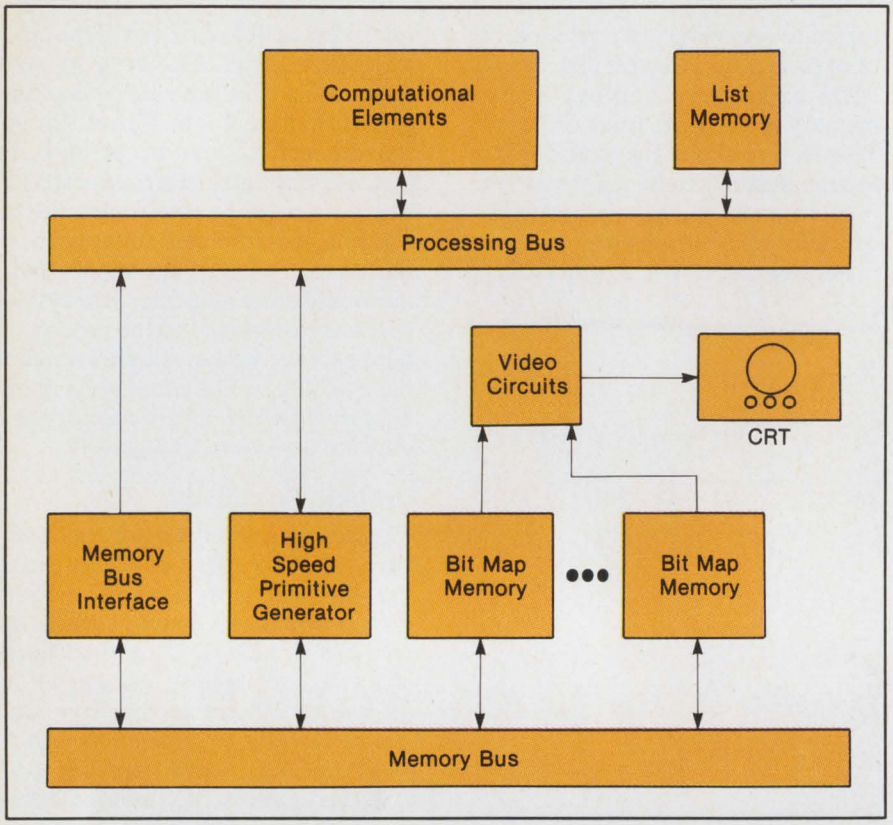


Figure 3: Multi-bit-map support is an essential graphics computer capability.

"re-rasterization." When a primitive is deleted, all remaining primitives are re-rasterized in order to fill in the "holes". This re-rasterization can be automatic and under control of the local computer, if the graphic computer contains command memory (sometimes called list memory) in addition to the bit-map memory. Because of the time involved in re-rastering a complex picture, a combination of command memory and multi-bit-map refresh memories proves to be most efficient. The graphics computer should thus be able to *support multi-bit-map memories as well as list memory* **(Figure 3).**

Computational Section

The advent of the 16 -bit high performance μP makes it relatively easy to add significant computational power to the graphics computer. **Figure 4** shows a processor module which sup-

What Resident SW Does Graphics Require?

What should or should not be part of a graphics language is a subject much discussed. The two data types used will mainly dictate the requirements. In the pixel mode (i.e., data received from a scanning device), image processing algorithms are appropriate. These include:

- FFTs
- Convolutions
- Histogram Equalization
- Rotation
- Spatial Warp Correction
- Edge Detection/enhancement
- Bilinear Interpolation
- Cubic Convolution
- Contrast (Brightness) Correction
- Picture Editing

For systems based on graphic primitives, there are two major subdivisions: those working in 2D coordinate space and those working in 3D coordinate space.

Both applications benefit greatly by use of virtual coordinate space addressing and picture segmentation. The first allows the application to operate without regard for the physical device address space, and the latter makes picture definition and referencing easy to use and efficient.

The 2D system should support:

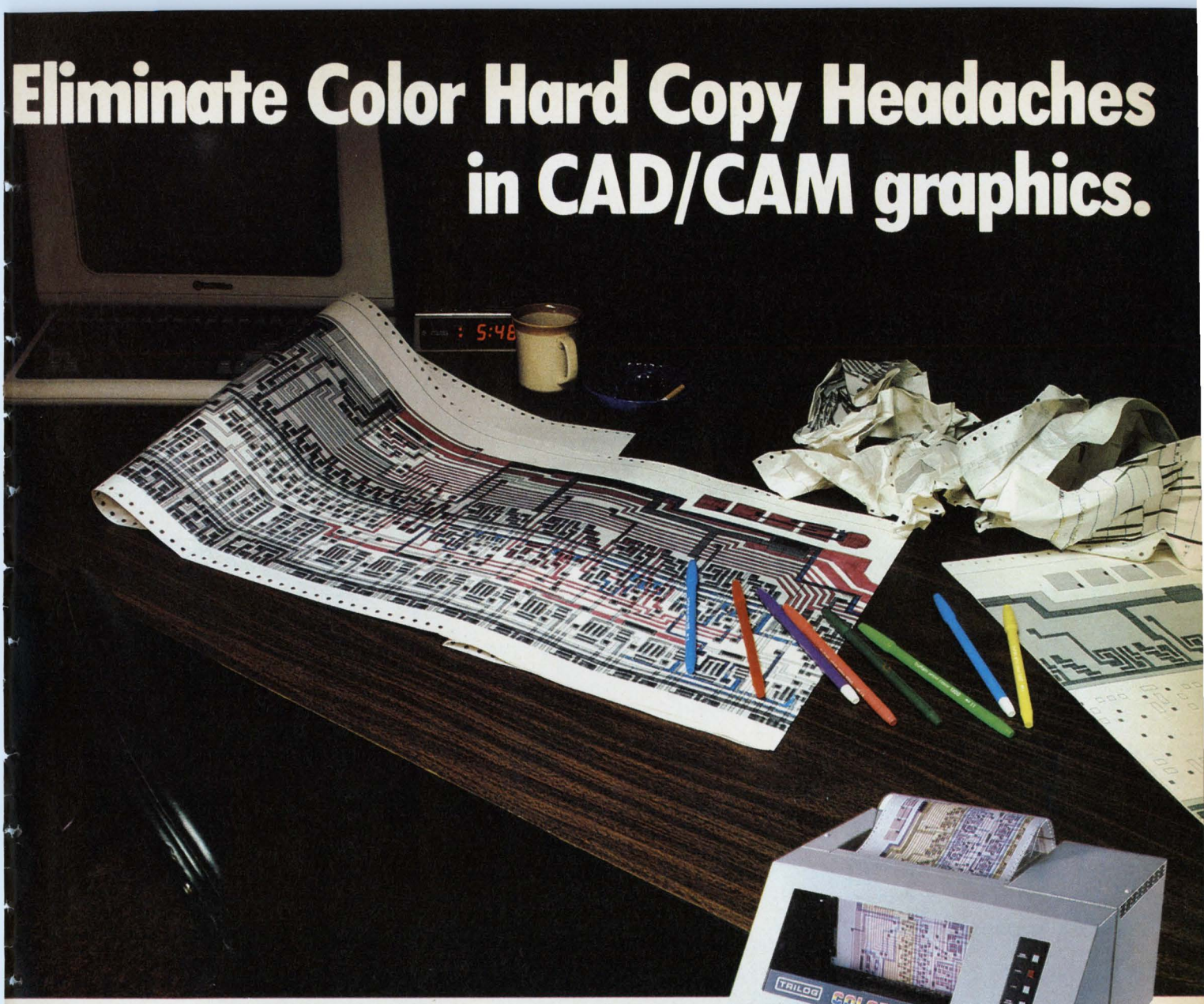
- 2D mathematics (add, subtract, multiply and ratio) for XY pairs.
- Fractional support for trigonometric functions
- Virtual and device-dependent coordinate systems
- Full transformation control for scaling, rotation and translation
- Windowing/viewporting
- Primitive commands for vectors, arcs, circles, rectangles, triangles, polygons, markers and trapezoids
- Text in at least three qualities
- Plotting support
- Operator interaction via keyboards, graphic tablets, cursor devices and/or trackballs or joysticks

In addition to 2D functions, the 3D systems should support:

- 3D mathematics
- Viewing projections (parallels and perspective)
- Lighting and shading controls
- Solid shapes (spheres, tetrahedrons, parallelepipeds and lines)
- Statistical support of polyhedra (volume, center of gravity and moment of inertia)
- Hidden surface removal
- 3D clipping (left/right, top/bottom and front/back)
- All of the operator interactive devices listed in 2D

By providing the graphic computer with preprogrammed image, 2D and/or 3D routines common to both a stand-alone or a distributed processing system, the burden on the applications programmer is significantly lessened. By doing so in a standardized manner, the advantage of portability for both application and people will result.

Eliminate Color Hard Copy Headaches in CAD/CAM graphics.



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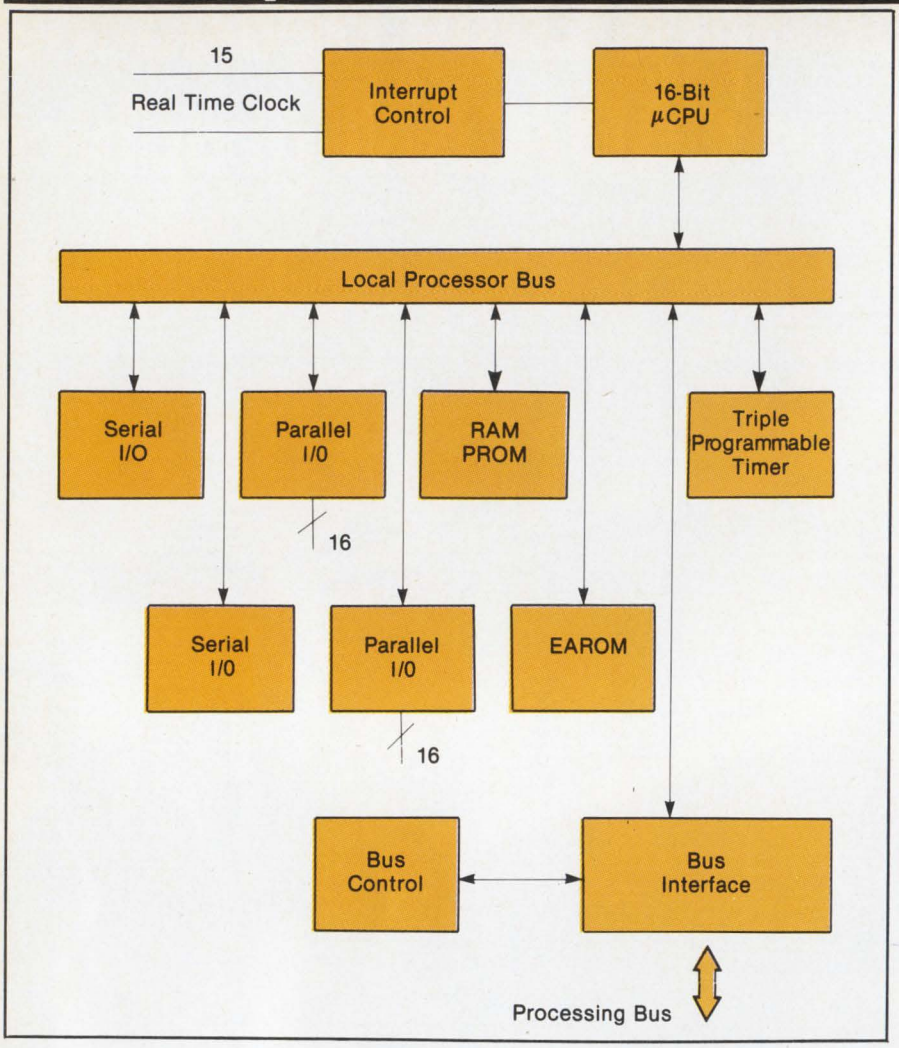
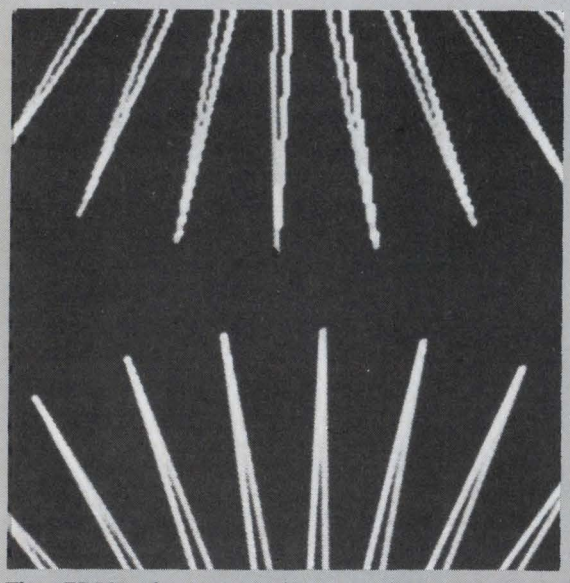


Figure 4: Processor module supports elements of a typical computer. Operator peripherals are integrated via serial and parallel interfaces.

ports all of the elements of a modern small computer. Serial and parallel interfaces allow the connection of operator peripherals. Local RAM and PROM provide storage of both data and programs. Because of the anticipated need for more processing capability, this processor module contains a local bus which is isolated from the system processing bus. Thus accesses from local memory can be made simultaneous with other activity on the system bus.

For use in stand-alone environments, a variety of mass storage devices ranging from a floppy disk to large capacity hard disks must be supported. The application will dictate the speed and amount of storage required. Because the modern 16-bit μC can directly address large amounts of memory, the expansion RAM can be added to the processing bus for storage of "list" type data as well as programs. At least 512K bytes of expansion RAM should be available in order to store the

Firmware Anti-Aliasing For Raster Graphics



The AED767 color raster graphics terminal allows the user to create anti-aliased images at draw time. The image on the top shows the effects of aliasing—stepped or jagged lines. By contrast, the anti-aliased image on the bottom has a much smoother appearance. (Images are unretouched, taken directly from the AED767 screen).

A contingent of attendees at last year's SIGGRAPH conference on computer graphics sported T-shirts with a unique design: a staircase over which was superimposed a circle divided by a diagonal bar. The message implied by the symbol was Stamp Out Aliasing—those jagged lines generated by raster graphics terminals. The anti-aggies protest came mostly from computer graphics artists, whose creativity has long been stifled by their graphic displays' inability to produce a smooth line.

Scarcely a half-year after SIGGRAPH, Advanced Electronics Design (440 Potrero Ave, Sunnyvale, CA 94086) has announced their answer to the jaggies: a firmware-anti-aliasing terminal that creates smooth-edged graphics without the need for prior processing by the host computer.

AED's model 767 achieves anti-aliasing via a process called *ramping.* Ramping involves blending the vectors with their background to give the lines a smooth appearance. The result, says AED, is "optically superior resolution, more lifelike drawings, and greater convenience for users who need no longer wait for computer time to run anti-aliasing programs."

Price of the AED767 is $18K. Along with built-in anti-aliasing, the terminal also features a 1K x 1K x 8 virtual address space with a 768 x 575 viewing window; up to 42 KB of RAM/ROM; support of two serial RS232 ports and one parallel interface; and Tektronix family emulation.

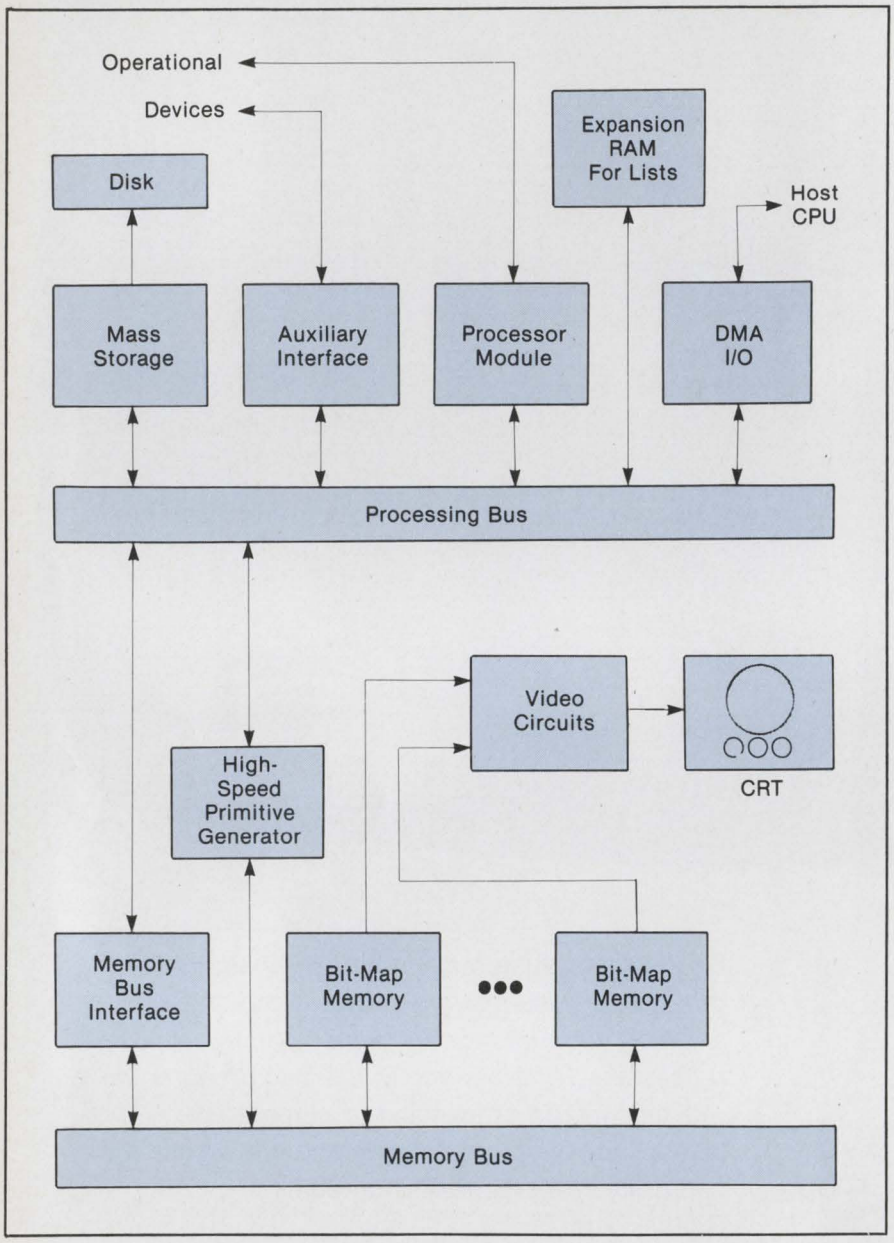


Figure 5: Fully configured graphics computer functional block diagram portrays DMA I/O interface capability.

more complex pictures represented by graphic primitives.

When used in a distributed processing system, the graphics computer will require both low speed serial and high speed DMA interface capability. The graphics computer should therefore have DMA interface capability and expansion serial interface capability. **Figure 5** shows a full configured graphics computer.

Software Systems

Now that the hardware architecture is optimized for the graphics computer, it is necessary to tie all of the pieces together with a software system. This system must be optimized for computer graphics and yet retain the capabilities of a general-purpose computer.

For stand-alone operation, the traditional software tools found on most general purpose computers are necessary. These tools include a text editor, file managers, assemblers, linkers, loaders, and a high-level language compiler. It should not be necessary for a user to learn a new programming language; that need would defeat one of the purpose of the graphics computer: ease of use.

For use in distributed processing systems, the display computer may or may not require the general purpose utilities described above, but an additional software system designed to ease the burden of the application programmer will be needed. For this system, the use of a syntax that is patterned after one of the proposed standard graphic programming languages is strongly recommended. The CORE systems proposed by ACM-SIGGRAPH (GSPC, under consideration by ANSI) and the GKS system (DIN-0066252 under consideration by ISO) are both good examples of the standards efforts presently underway. To be consistent with the philosophies of distributed processing—namely sharing the workload and off loading a host computer—the selected standard language should execute on-board the graphics computer with minimal software resident in the host computer. The host software package should be a library of subroutines, compatible with the host language, which does little more than command the graphics computer to perform the desired function. Thus, all of the benefits of a standard programming language will be achieved: portability of software from host to host, portability of programmers (people) from application to application, plus the benefits achieved through distributed processing. Again, the graphics computer would yield results greater than the sum of its parts. □

It should not be necessary for a user to learn a new programming language; that need would defeat one of the purposes of a graphics computer: ease of use.

Made in USA

Aydin Patriot™ Color Monitors

Aydin Controls introduces its American-made, in-line gun, high resolution Patriot Series of Color Monitors.

Aydin Controls, a leader in high resolution color display terminals, now manufactures Patriot™, its own in-line gun series of color monitors. The Patriot series will supplement Aydin's well known family of delta and in-line gun monitors.

Patriot's 13-inch Model 8810 and 19-inch Model 8830 both offer the latest state-of-the-art features plus all of the advantages of American technology and manufacturing. Patriot features high video bandwidth, wide horizontal line rates, fixed convergence, excellent high voltage regulation, modular construction, analog or TTL inputs and rack mountability. The Patriot Series can be customized to fit special needs.

Patriot monitors provide outstanding performance at an attractive price coupled with an 18-month OEM warranty; off-the-shelf availability; quick delivery of spare parts; and fast, reliable service. For more information contact Aydin Controls, 414 Commerce Drive, Fort Washington, PA 19034. Tel: 215-542-7800 (TWX 510-661-0518).

AYDIN CONTROLS

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Extending The Limits Of AC Gas Discharge Display

Although CRTs are ideal low-cost, versatile display devices for most applications, they're less than ideal when large-area display is required. CRTs are somewhat unwieldy in any size, but become impossibly so at diagonal measurements above 75 cm. CRTs approaching one meter diagonally are little more than extremely large conversation pieces.

Of all the alternative display technologies, the one that's made the most remarkable progress in recent days is AC gas discharge. Photonics Technology, working jointly with Magnavox, recently announced that they would be introducing a flat display measuring three meters diagonally later this year. Resolutions will top 2500 pixels/cm², and the displays will be available with four-color capability (red, green, blue and white).

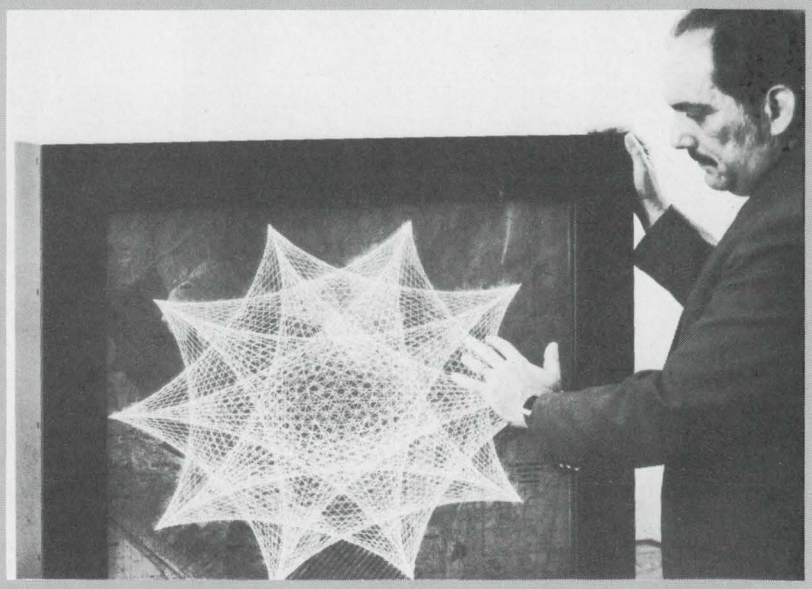
Photonics' displays look like large panels of framed, transparent glass, and can be mounted in front of static graphics, such as maps or grids. The one-meter display Photonics is now marketing has a resolution of 400 pixels/cm², with two million total pixels. Address rate is 80 million pixels/sec.

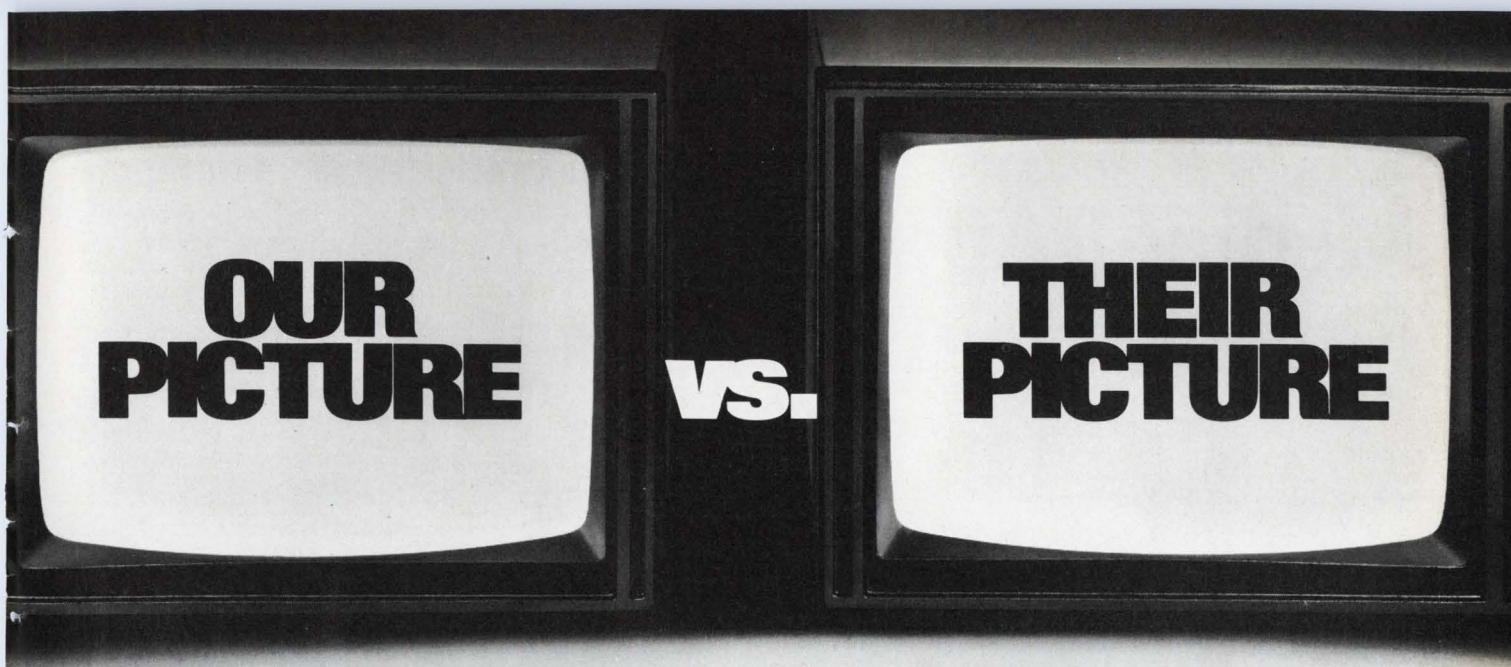
The displays are made by sandwiching a neon-based gas between two glass substrates. Each of these substrates has a parallel array of thin-film electrodes, insulated from the gas by a transparent dielectric coating. The one-meter display has a 1600-line array on one side and a 1200-line array on the other. The two arrays are orthogonally oriented; pixel elements occur at each array cross-over point.

Photonics' large displays have all drive electronics, power supply, Z-80 or Intel 8086 μPs with RS232 interface packaged within the displays' 4″ wide by 4″ deep picture frame housing. Operating power for the one-meter display is less than 200 watts with every pixel lit; voltage is 90V to 100V.

Price of the AC gas discharge displays is proportional to size: according to Donald Wedding, Photonics Vice President of Administration, price goes up by a factor of ten as area increases four times. Cost of the one meter display is about $250K; the 60 cm diagonal display sells for about $30K.

The high cost of these displays (compared to CRTs) means that they're used only in specialized applications where their high viewing area and slim profile are essential. Today, this is primarily in military and government applications. However, the displays' costliness is due primarily to the fact that they are currently custom manufactured. In the near future, mass manufacturing will lower their cost to the point where they compete head-to-head with CRTs in a variety of applications.





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Medical Applications For System Design

by Paul Snigier and William Sniger

This article discusses products, specifications, obstacles, and design approaches in this rapidly-growing technology.

As a rehabilitation tool, μCs/μPs (microcomputers/microprocessors) promise to aid handicapped individuals, particularly spinal cord injury (SCI) victims with damage to the central nervous system (CNS)—paraplegics (paras) and quadraplegics (quads). It is a new and growing market, well-suited to system designers and small engineering firms, software houses and new technology.

High Technology Invades SCI Markets

By their low power consumption, flexibility, support, lessened maintenance and repair, small size, reliability (long MTBF), repairability (short MTTR), upgradability, lightness and low cost, μCs/μPs are creating a new market in the SCI field. This new market is on the edge of rapid, although limited, growth with few competitors. It is not a field large enough to attract computer giants, so long-term survival for small OEMs looks good. Many existing SCI aids can now be re-designed and upgraded; and old-line firms in the field lack the know-how and marketing expertise to creatively apply μCs.

Startups and small firms are most successful if they seek out a small, rapidly-growing field (or sector of that field) that will remain vertical and yet not grow too large. This avoids attracting the big companies (who can squash you like a bug), and allows you to establish a market share and keep it as that market sector expands. The SCI field is just this sort of field. Expect annual production runs to be low (perhaps in the hundreds range). As a result, adapting off-the-shelf hardware/software will be the name of the game, plus heavy semicustomization, installation, maintenance, field upgrades and support. Although large firms (Radio Shack, Apple, IBM, Texas Instruments and Intel) will profit, it will be from sales to small OEMs. This installation-, maintenance- and support-intensive field will remain safe for small OEMs.

Elaborate distribution channels, now working, won't help giants like Radio Shack, Apple and DEC much in the SCI field. Most newcomers to the μC field sell through a direct sales force (IBM), independent retail stores (Apple, Data General) and their own retail stores (Radio Shack, DEC). To reach new markets, these firms set up a dealer and distribution network to reach consumers and small businesses.

New Products Require Micros

The market is embryonic. There are numerous product, marketing and design opportunities, including:

1. Modification of existing aids, such as wheelchairs, is needed. Wheelchairs are suited to redesign by CAD/CAM, μP-based electronics, on-chair radio communications systems, control systems, voice synthesis, etc.
2. Custom-programmed μP systems that stimulate and exercise muscles naturally prevent atrophy of body muscles and joints. Otherwise, joints become loose or freeze, muscles wither and limbs atrophy. Nothing, including physical therapy (PT), can replace actual muscle contraction. This will require lots of software that is updated and semi-customized, so it promises to become lucrative.

The Myoflex is one such device; it duplicates body frequencies, the same patterns registered on electroencephalograms (EEG). Rapid healing of sprains and bone fractures by these Myoflex electrical frequencies is well-established. Further, when moistened Myoflex electrodes are placed on volunteers' shrivelled limbs, muscles respond and limbs flex and move, toes and fingers curl and uncurl. This treatment can restore muscle tone to unused, paralyzed limbs.

Earlier electronic muscle stimulators were developed by other researchers, notably Dr. John Ziegler, a pioneer in sports medicine, and Michael Mentzer. This machine could contract any of the body's skeletal muscles to varying degrees all the way from complete rest to maximal contraction, where every fiber of a given muscle was activated. Dr. Ziegler and Mentzer administered treatments to athletes and cripples. The theoretical framework for this research was laid by Dr. Hans Selye whose GAS ("general adaptation syndrome") stress concepts were only partially applied to the treatment of SCI. Much research remains, and this field promises high-growth for electronic muscle stimulators— ones controlled by μPs and algorithms writ-

William Sniger, himself a victim of spinal cord injury, is President of the Massachusetts Chapter of the Spinal Cord Society devoted to the non-profit dissemination of information on cure-oriented and computer-assisted research for the handicapped.

ten in the software.

3. Progressive muscle resistance devices must be designed for use with electronic muscle stimulators. Existing PT is first-generation. Second-generation units could follow single-joint (isolation) with compound-joint movements within ten seconds; third-generation units would incorporate μP control and feedback to the patient via the Myoflex or other device, with data recorded by a mini or μC. This field was pioneered by Arthur Jones (for machines) and Michael Mentzer (for free weights). Recent research indicates that machines alone create problems, and that a machine-free weight combination is best.

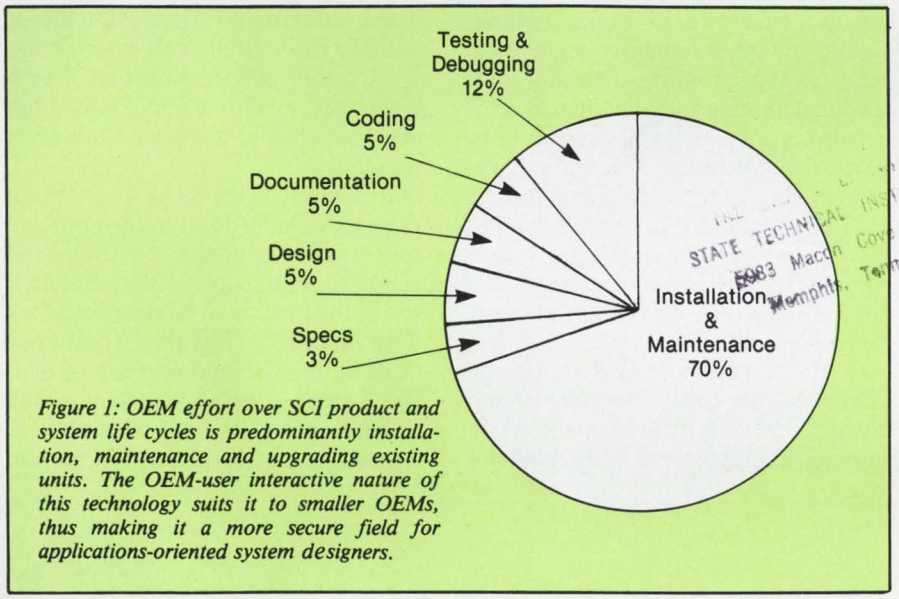


Figure 1: OEM effort over SCI product and system life cycles is predominantly installation, maintenance and upgrading existing units. The OEM-user interactive nature of this technology suits it to smaller OEMs, thus making it a more secure field for applications-oriented system designers.

Any progressive resistance training that places a torque upon the spine (particularly the lumbar) should be avoided, as this gradually may create intervertebral disk degeneration or aggravate an existing degeneration caused by repeated torquing or sudden impact.

4. Computer and electronic pain-killers— such as Johnson and Johnson's TENS (Transuctaneous Electronic Nerve Stimulator)— can replace more costly, often daily, dosages of sometimes-dangerous and partially-effective pain-killing drugs. Other devices exist, and some are even partially-successful for some surgery.

5. Products include sophisticated, μC-controlled prosthesis and control systems aids.

6. For display, using VDTs (video display terminals) or TVs as terminals is one low-cost solution; another is B&W or multi-color flat panels placed above quads, who presently spend their lives on their backs in a rehab bed, occasionally wearing 90° prism lenses to watch TVs mounted on the far wall. Flat panel display use is growing rapidly for video games, "pocket TVs," automotive displays, etc. Their flat profile, lower power needs, compactness, ruggedness, portability and declining costs suit them for many paralytic systems. Contenders for the market are: LCDs, AC and DC plasma, TFEL, LEDs, flat CRT and vacuum fluorescent.

7. Computer Aided Instruction (CAI) is needed and can cut existing costs of tutors, aids, transportation to colleges and present education for the handicapped. As it is, electronic-based education is about to undergo phenomenal growth— a fact that has not escaped traditional textbook publishers (many who are now getting heavily into software). Meanwhile, traditional colleges, facing threats to their existence, are experimenting with alternative, electronic-based CAI. Another factor about to make CAI commonplace are low-cost, hand-held "teaching units." TI talking language translators and Radio Shack/Sharp pocket computers are the primitive forerunners of this explosive market. This market will be driven by availability of high-capacity RAM/ROM chips. Home degree programs are a new market for many universities facing bankruptcy; CAI is the only salvation for many. Private firms may be more adaptable and quick to enter this new market niche; and, already, firms are offering lucrative training courses more practical than college courses. Some, like DEC and Wang, are starting their own schools or colleges. As for the severely handicapped field, once again, it's a sheltered market that larger firms will wish to avoid. For the small OEM, it is a market in which he will purchase education programs and re-package them for his unique system. Or, the small OEM may wish to specialize in a vertical specialty, such as writing software packages for the 8 million handicapped children in US rehab centers. As an example, by eyeball manipulation (corneal reflection), quads could conduct chemical lab "experiments" by manipulating "flasks" and "test tubes" on a color graphic terminal (TV screen or flat panel). Recreational video games could also be altered for the disabled, adding some joy to learning, with interfaces to other devices, networks, robot manipulator arms and other peripherals.

8. A mind-boggling VDT "travel" system from MIT (that must be seen to be believed) could aid paralytics. Developed by Prof. Kenneth R. Sloan and others of the MIT Dept. of Architecture, it allows viewer-controlled "travel" to remote locations via a new video disk and TV. For example, MIT used the town of Aspen. Viewers on this MIT system "drive" down any Aspen street at will, at any speed, stop, look around, zoom in on any building, "enter" it and "walk" about, "interview" people there, or later fly over the town at any altitude or speed, controlling pitch, roll, and yaw at will. By switching "season modes," Aspen is portrayed in any desired season. A "time mode" permits the "visitor" to view buildings as they appeared at different times in the past. The system is run by screen touch control, but could be adapted for paralytics with corneal reflection or other I/O control. In "line perspective mode," the town appears as line drawings, whether seen from ground level or air. Applications extend primarily to systems for travel, advertising and insurance agencies, architects, city and industrial planners,

lenders, mall and city planners, highway departments and military training.

Future mass memory, such as R/W optical disks, could allow real-time interaction with displays. Displays could extend from geographical and architectural uses to "traveling" through history, arteries in the body or plants; in labs, rehabilitative vocation training; incredible realism for video games, and anything imaginable.

9. Home security, teleshopping, telebanking and local area networks (LAN) will be high-growth areas. Communication via phone, electronic conversation and home information systems (HIS) will open up inter-paralytic communication, within rehab installations or between home-based paralytics and others. Currently, paras are limited to chess and first-generation video games.

10. Many indirect SCI markets exist. Mini and μC systems are needed to aid SCI research, whether it is CAD/CAM, cure research, monitoring, accounting, WP, DP, inventory control and sophisticated patient-monitoring systems.

The most significant development in the field was the recent, nationwide Johns Hopkins (sponsored by NSF and Radio Shack) "First National Search for Applications of Personal Computing to Aid the Handicapped." Widely publicized in the trade press, this competition for prize money inspired ideas, devices, methods and computer programs to help the handicapped cope with community, home and work problems. Of the 6,500 inquiries, 800 designs competed to yield 100 regional and 30 national finalists.

Winners included infrared SCI eye trackers (causing computers to speak), lip-reading trainers, etc. Off-the-shelf pocket computers/programmable calculators were integral to many aids.

Robots Aid Paralytics

Robots can aid the handicapped by doing tasks in rehab hospitals, homes, in public, or at work. Tasks include eating and other functions, movement and transportation, dressing and bathing, moving and orienting objects, retrieving and sorting files and books, and other functions. Wheeled mobile robots, though of little use in industry, will be invaluable in rehab installations, as a visit to one will quickly convince you. Before we proceed, let's look at some robot basics as they apply to paralytics.

Robots are articulate linkage mechanisms based on simplified models of the human arm, with enough intelligence to make elementary decisions. They possess flexibility and dexterity to perform an intricate sequence of motions without human intervention. Most have six degrees of freedom. They are not limited to mere transfer, manipulation or human-extension. They are reprogrammable, operate automatically by themselves, perform many dissimilar tasks and make elementary decisions via sensing and control systems. Most are in production-line jobs on auto lines, ovens, painting, materials handling and the like. Most operating robots are still first-generation blind slaves—senseless and dumb machines that are difficult to reprogram and unable to adapt to varying conditions. Second-generation robots, now available, are active thinking partners— intelligent enough for limited decision-making, with many programmable in new languages, with touch and limited optical, pattern and character recognition capability.

In "manual teaching" or "teach programming" (the dominant method of programming), users move the robot through required motions and it stores the motion in its memory. This may include retrieval of food containers, opening and pouring of contents, preparation and feeding, as well as retrieving selected books, etc. Although easy to program, manual

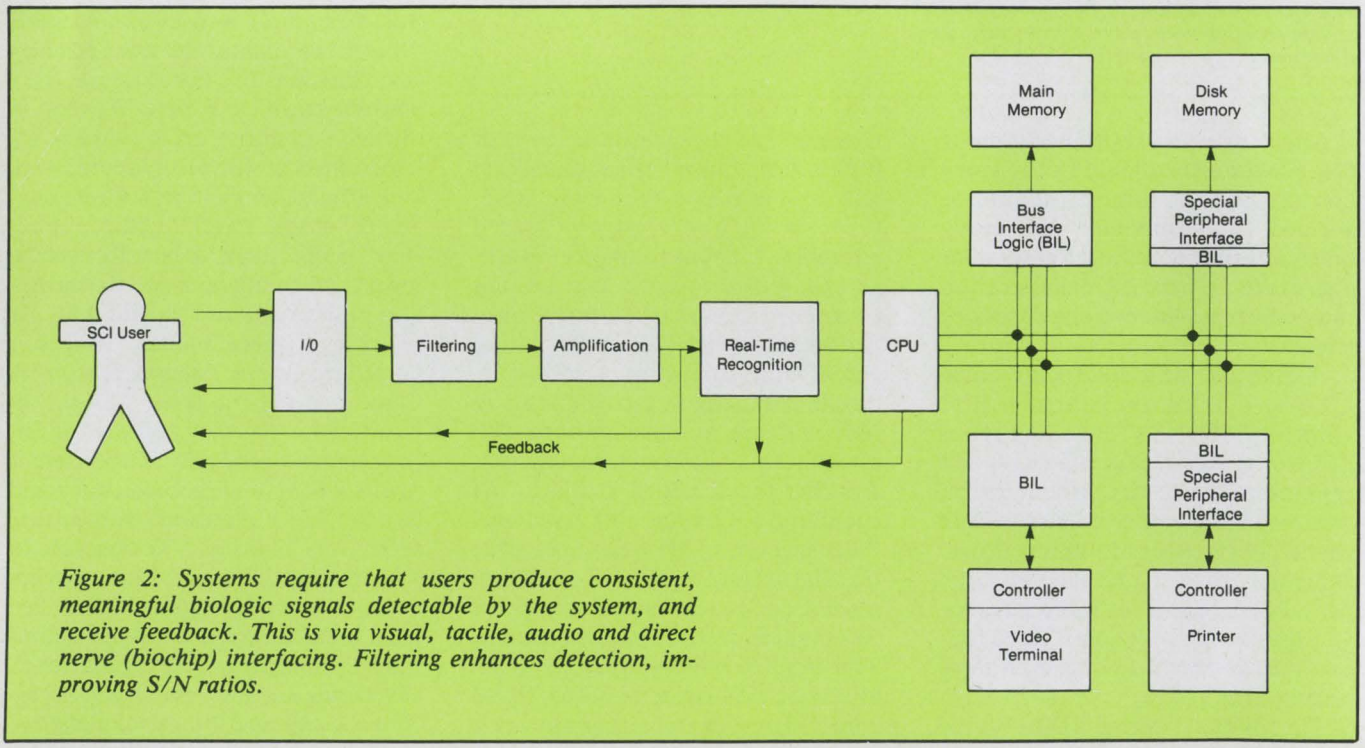
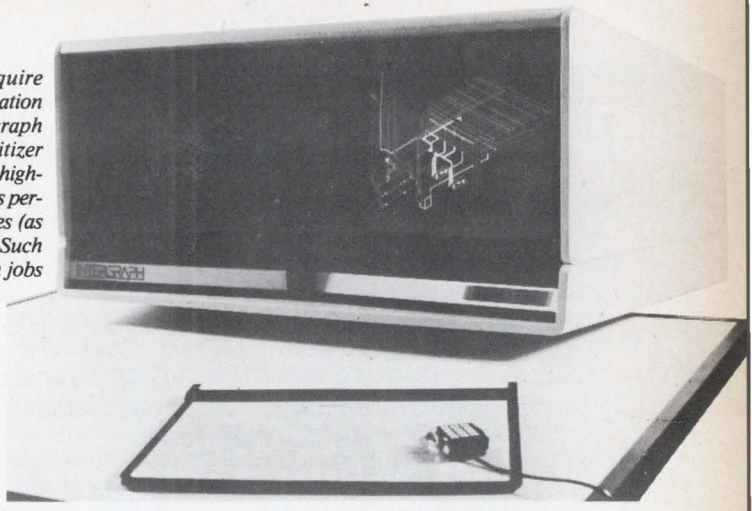


Figure 2: Systems require that users produce consistent, meaningful biologic signals detectable by the system, and receive feedback. This is via visual, tactile, audio and direct nerve (biochip) interfacing. Filtering enhances detection, improving S/N ratios.



Interfacing constraints require OEMs to enhance communication speeds. Although this Integraph touch-sensitive, surface-digitizer pad, entry-system is used in high-tech applications, similar pads permit direct selection of choices (as opposed to scanning units). Such units open up more high-tech jobs to the handicapped.

teaching is time-consuming, error prone in complex tasks and may require total reprogramming if slight changes are needed.

With "off-line programming," you use explicit and implicit high-level languages to describe movement sequences. Callable subroutines describe frequently-used repeated procedures. "Explicit language" commands define detailed motions or actions; "implicit language" (mostly experimental) commands describe tasks. Third-generation adaptive robots, now experimental, require less programming and use artificial intelligence (AI). Speech recognition and voice synthesizer (speaking) robots are in use, and will lead to conversant robots that listen to and obey doctors, nurses or paralytic operators.

In "point-to-point" programming, only trajectory end-points are recorded, and it is generally used if path velocities are less important. In "continuous-path" programming, the entire motion is recorded, usually in the "teach programming" mode.

In either case, you will encounter a problem: robot movements must be debugged or inadvertent collisions will damage the robot arm and objects— not to mention the paralytics. Negligence with the software, EMI troubles or other problems could kill your reputation and even lead to some history-making lawsuits. Judging from the quality of some software packages pawned off onto unsuspecting OEMs, and the ensuing blame-throwing, there is reason for caution.

To avoid damaging prototypes, researchers now use 3D graphic modeling to simulate robot movements; when collisions occur, a beep warns the programmer. Since it is displayed on a graphics terminal screen, no damage is done.

Aside from artificial intelligence, no areas will improve robots like vision and touch. Some second-generation robots use CCD photosensor arrays or TV cameras to digitize the image, process it and recognize silhouettes or shapes by comparing them with stored shapes. With future 3D vision, depth perception and advanced deduction will permit a robot to identify objects not in its memory and to operate more on its own with less programming. Some sighted robots are guided by converging light or laser beams.

Robots using new piezoelectric transducers and skin-like arrays can detect subtle pressure changes, creating more dexterous robot arms.

Other researchers are studying people as if they were robots (and vice versa), since robots are designed to do human jobs. This information, though intended to improve robots, is also invaluable to understanding paralytics. For example, the human runner was modeled and found to possess 13 degrees of freedom; a human hand, 29. Walking, bipedal-locomotion robots— or robot exo-skeleton suits for paralytics (Cornell Project)— aren't easy to design; they are unstable. Since four-legged "mule" robots are better suited to this, but are experimental, mechanized wheelchairs will be around for a while.

Mechanized walking machines and exo-skeletons were attempted by the Cornell Project of the 1960s to enable soldiers and warehouse workers— wearing metal skeleto-suits with mechanical amplifiers— to become super strong and handle enormous weights with ease. If surrounded by heavy body armor and a self-contained life-support system, such "amplified men" could function in hostile environments: undersea at great depths, in space under high G-conditions, and under heavy enemy fire, while immune to gases, toxins and biological agents (with some resistance to radioactivity).

Less dramatic "walker projects" are developing multi-legged military vehicles to navigate terrain too rugged for armored vehicles or jeeps. To our knowledge, SCI researchers have not adapted this vast body of technology.

For the near-term (and more practical and profitable), the retrofitting of cars, vans and lifts is more likely to gain a return-on-investment. Driving a mechanized wheelchair, even with a plastic enclosure, is difficult in winter, and usually dangerous.

Although micropositioning is not needed for most handicapped user applications, the developments are applicable, since anything that increases robot arm rigidity also can be used in all robots to lower costs. (See "People As Robots: Robots As People," by Ted Black, *Design Engineering,* Jan. 1980, pp. 63-67).

The robot market for the handicapped is still in the "gee whiz" stage, but promises sudden growth soon. This will occur with third-generation robots whose vision, voice recognition, speaking, touch and AI well-suit them as SCI aides. Lowered costs and mass production for industrial users will increase availability and drive costs down. For more information, see "Robotics Technology for the 1980s: Flexible Automation," by Edward Goodridge, *Circuits Manufacturing,* Nov. 1980, pp. 27-40; and "Computing and the Handicapped" Special Issue of *Computer,* IEEE Computer Society, Jan. 1981.

Interface Problems Require Improved I/O Units

Interfacing μC systems and the handicapped will be a very serious obstacle: unlike the able-bodied (TAB) users, the handicapped often cannot operate interface devices, or do so slowly. Many are non-vocal and cannot even signal for a nurse. I/O devices are limited to hand joystick controllers, sip and puff pipes, corneal reflections that convert eyeball movements to signals,

Product Selection Criteria

Product selection in this field has many familiar requirements, but also has its own special criteria. Before specifying, consider the following.

1. What should you look for before specifying?
   - Analyze in terms of current needs and projected growth.
   - Define criteria based on: speeds, protocol, interface, intelligence, environment, flexibility, software/hardware system support needed, etc.
   - Evaluate potential suppliers: cost/price performance ratios, reputation, quality, warranty, ergonomics, maintainability, service capability, delivery, cost of consumables, lease and purchase options, supplier commitment and anticipated survival.
2. What problems plague these product/systems?
   - too bulky
   - limited display size
   - poor ergonomics (for SCI)
   - paper handling problems (unique to SCI)
   - noise level
   - reliability
   - size and weight
   - special environments
   - difficult to locate failures
3. What new CRT terminal criteria count most?
   - Extensive ergonomics (human engineering), including ...
     - — tactile and audio feedback
     - — sculptured keytops stepped for minimum finger extension/comfort.
     - — large display font with line and character spacing.
     - — darkened/etched glass to diffuse reflection/enhance contrast.
     - — tube tilt (possibly robot controlled to adjust for ambient lighting).
     - — audible/visible alarms with controls for instant user feedback.
   - Built in diagnostics.
   - modular design (for upgradability and customization).
4. What printer (terminal) criteria count most?
   - convenient handling (perhaps robot)
   - inexpensive consumables (ordinary paper)
   - forms handling capabilities
   - downloadable
   - quiet
   - compact, light, easily relocated
   - rubber, non-skid base

hum detectors, mouthstick extensions, etc. The signal-to-noise ratio (SNR) is often low.

Fortunately, there is a solution. The μC is flexible, as a single software change can modify μC response to accept new inputs to provide different outputs, such as an extra algorithm to filter out spastic movements (noise) from the signals. μC-based I/O units must sense some SCI-generated, meaningful biological signals, convert these and provide feedback. This will be visual, tactile, audible or even direct to the CNS or brain.

One solution to communicate alphanumeric characters or to position VDT cursors requires the display of letters; some devices display them cyclically from A to Z and 0 through 9, with ASCII commands thrown in. More efficient detectors take a binary decision-tree approach. Others display higher-frequency (of usage) characters such as ETAON first. Selection is by sip and puff, corneal reflection, etc.

Our best technology can do no better than these primitive, inefficient and slow human-to-μC interfaces. But, "I/O biochips" and brainwave detectors now under development will break the interface barrier and permit rapid man-to-computer communications for executives, pilots, researchers— and paralytics. This may be the most significant development in computers; for obvious reasons, it will shake society to its foundations.

Although research done with crude sensor brain implants and detecting electromagnetic fields surrounding the skull (about 3″ out) is promising, direct nerve probes (which are still large and crude) may succeed first. New "biochips"— large arrays of ultra-small electrodes on VLSI chips now under development— will permit electrical monitoring and stimulation (or control) of defective nerves, thus permitting paralyzed persons to move by bypassing damaged nerves; and, if used in reverse, can stimulate nerve, bone and tissue growth. (See "Will I/O Biochips Create Computer Peripherals Revolution?" by Dr. J.R. Barker, U. of Warwick, U.K., *Digital Design*, Dec. 1980, pp. 18-19.)

With a 64,000-plus transistor IC array in a 4 mm² area (and 0.02μm/cell), each cell will approximate large molecules of cellular matter in size. Such a fine "mesh" placed over a portion of neural networks promise to bypass damaged nerves and permit a rapid man-to-computer communication synergism.

Implantable VLSI chips face three obstacles: chemical insulation, host compatibility and electrolysis. To insulate against saline fluids and prevent sodium dopant ions from ruining the silicon, a several-hundred-angstrom inert, non-toxic insulating layer must be bonded to the biochip.

Unique Obstacles Exist

There are some very unusual obstacles in this industry not commonly known to OEMs entering it. If you're aware of these potholes, you can avoid or minimize them.

Obviously, money is your first concern: most handicapped and their families are cash poor, or soon get there. Who will pay for your systems? Mostly, third-party payments from insurance companies, Medicaid, Social Security, state rehab agencies and local civic groups. Get to know how to sell to or through third-parties and to the agencies. Relative to other fields, the rehab field is more modest financially; it's not one most big firms will ever go after and has many vertical niches within it. Small OEMs that position themselves properly have a good chance of long-term survival. Many other OEMs are beginning to wish they had done so with more care; and, many

now find themselves coping with competition from other OEMs, changing technology, price wars and even their own vendors, who may now bypass them and sell to end users.

To keep from designing a good product that fails to sell, keep in mind the following points:

1. If your products help make paralytics do productive, salaried work, they will sell; and, if they're multi-functional, pro rata funding could aid sales.

One example, Lift Inc. of Northbrook, IL., trains and pays competitive rates to handicapped people to work at home as programmers. Other firms are doing this.

Information work is well-suited to paralytics. An epidemic of computer-generated mountains of raw data—volumes of detailed and wasted figures that become obsolete before being used— are plaguing organizations. Firms are seeking some way to convert the flow of raw data (now used mainly for tactical short-term decision making only) into digested information that executives can use for longer-term strategic decision making. Networking, DBMS, the electronic office, and remotely-accessible data bases is making this a natural job for the disabled at remote workstations, who could summarize such data into reports.

2. Avoid designing the "ultimate system" and adding too much into units, as this will make them unaffordable. Since annual production runs will be small, perhaps in the hundreds, it's best to stick to off-the-shelf hardware. Your value-added could be in software or hardware, installation, maintenance, fitting, repair, retrofitting and support. Use judgement and try to add features or upgrade functions, especially if at minimal cost. Remember, too, that in some systems, multifunctions might be the way to go. A one-unit system may handle HIS, WP, security, robotic/cell control, phones and fill a niche more cheaply than several systems.

3. Keep upgradability in mind, so that as competitors introduce improved units, you can field-upgrade existing units. Potential purchasers feel safer knowing that not only is your product supported, but that they won't be stuck in two years with a non-upgradable turkey. Upgradable systems sell fence-sitters.

It's mostly not a quick-buck mail-order or product-selling business, but one that involves installation and customization and support. It will require teams to install door and window sensors, servomechanisms, alarms, etc.

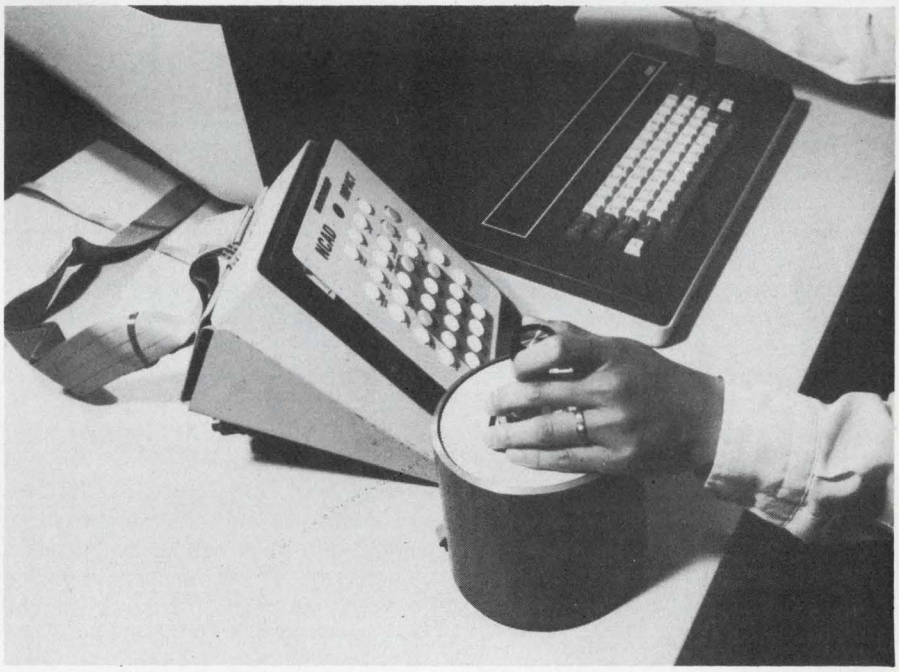
4. Ergonomics (human engineering) takes on new meaning in this field, and most existing furniture, and some wheelchairs, induce scoliosis or further spinal damage. More CAD/CAM is needed.

5. Red tape is a problem. Learn all the regulations, permits and guidelines involved early, as well as the groups that pass on your product. This is far more tedious in the US than in Europe; and, some experts claim overly-strict US regulations hamper innovation. μC-based systems will come under increasing bureaucratic scrutiny, testing, and possibly over-regulation in the name of safety. If you learn how the game is played early, while the markets are still embryonic, you'll minimize this danger. Get to know end users, the paralytics, and visit rehab centers, installations and hospitals.

6. After gathering information, identify your blind spots, and hire someone to compliment your weaknesses; or, at least learn from experts in these areas. Consider hiring consultants and renting equipment, such as development systems.

7. Don't count on higher capacity memory chips or other projected devices, and don't rely on projected falling hardware costs, or even availability, which may vary dramatically. Bubbles and 64-K RAMs are two examples. Avoid designing around preliminary spec sheets. Don't count too much on lead time stability; they are now shortening, with less multiple ordering, but lead times change rapidly. Firms like DGC, unable to obtain 4116s a few years ago, could afford to ride through quarterly losses. You may not.

8. As for market research, it's more important to do it personally, as very little is available. Establish contact, read widely and collect everything remotely related to the field from other disciplines. Cross-disciplinary OEMs have a big edge. Fortunately, since the markets are rapidly evolving, your chances of identifying and positioning yourself properly in the safest and



Control or joysticks, although not new, are a principal I/O device in this field. Although not used in handicapped systems, this joystick (Northrop Adage 4370 3D graphics terminal) rotates and zooms images in a manner directly applicable to handicapped systems.

most lucrative sectors is good. To avoid being surprised by changing niches, keep track of SCI regeneration cure research: it will prove a financial threat to certain market niches, and no other activity so seriously threatens your chances of success or failure in given market niches. The Spinal Cord Society newsletter (about 15 pp./month; $20/yr.) is the only comprehensive source of information in the field. (Dr. Charles E. Carson, Pres., SCS, 2410 Lakeview Dr., Fergus Falls, MN, or Box 69, Minneapolis, MN, 55440.)

9. Old mental barriers that SCI is irreversible may work to your advantage, as many established, old-line firms in the field are not research— or marketing-savvy, are less savvy in high technology, and aren't especially innovative. They've never faced changing market niches, or sudden changes, and may never learn about market research and high technology until it's too late for them.

10. Consider psychological aspects (fear of change, job threats, etc.) when designing systems and in advertising and sales pitches. You will encounter serious attitudinal obstacles to innovation, as some medical aides and patients mistakenly fear cure, innovation or change (particularly from computers). Medical personnel may see them as an economic threat and hope to maintain the status quo. On the other side, certain paralytics fear and fight cures/innovation because their illness fills deep psychological needs (''suffering cripple syndrome''). Either type can ''sandbag'' your products, without you being any the wiser. As an alarming example, in a hospital near Boston, it was recently reported in the computer trade press how health aides were deliberately entering false patient data to sabotage the hospital's new computer systems!

Nerve-Bypass Systems Aid SCI Regeneration

Microcomputers with computerized electrode implants have re-established anatomical connections, bypassing damaged spinal cords. In lab experiments with SCI cats, the paralytic animals ''walked'' via μC-based systems.

One research area that will require μP-based systems (with sophisticated algorithms written in the software) is organ, limb and SCI regeneration. Experiments applying negative DC voltages (10-μA currents) caused limb, nerve and bone regeneration with mice. For man, however, it may require more sophisticated μC-based systems to generate complex waveforms, varying in response to feedback. Application of μC-generated waveforms, possibly in the presence of Naloxone (already proven effective in SCI regeneration), could effect even quicker regeneration. Regenerated axons displace earlier sprouting and reclaim their original target sites (formerly believed ''impossible''). Such clubbing axons often send out pseudopods like amoebas, trying to probe and regenerate, sometimes spontaneously; in collateral sprouting, adjacent (rather than injured) neurons regenerate. Experiments have grown peripheral nerve bridges from the brains of rats half-way down the spinal cord via Schwann cell activity. This means that since certain chemicals attract and stimulate axon growth to appropriate targets, that application of μC-generated complex electrical and/or electromagnetic waveforms may further enhance regeneration.

μC's with computerized electrode implants have re-established anatomical connections.

Even without electrical and/or electromagnetic stimulation, Naloxone and similar drugs are partially-to-totally-effective when administered promptly. In one experiment (by Dr. Naftchi), 26 SCI cats experienced 100% recovery. (For human paralytics, the rate was 50%.) Other SCR regeneration cures exist for acute cases (steroids, TRA, surgical cooling, HBO, enzymes, DMSO and 20 others) and chronic cases (late decompressions, synthetic bridges, omentum and brain cell transplants, Kao-type nerve grafts, etc.). Judging from experiments, a hybrid approach combining these cures can be combined with carefully-shaped and varying μP-generated electrical and/or electromagnetic waveforms.

Complete nerve fiber loss rarely occurs; and, even if completely divided, the cord retains a vast, if untapped, regeneration potential. ''Broken neck'' or back is a misnomer: over 90% of SCI cords are not severed; and, if as little as 10% is intact, the victim can expect to walk again, although with less precise coordination. For all of these cases, if regained coordination from regeneration is not total, μC-based nerve bypass systems with custom-written software (with algorithms tailored to each specific case), could restore the remaining coordination to the paralytics.

Nothing To Fear

As a system designer entering this field, you will become part of the vast support system, rehab, medication and care industries. According to statistics (NINCDS Fact Book, 1979), SCI victims and their families pay $2.3 billion annually in direct medical expenses alone. This source cites that the total 35 million neural cases cost $55 billion annually. There exist 70 million disabled, of which 500 thousand are SCI, with 15 thousand more injuries per year. Room and board alone cost $7k/month/patient, plus more for drugs, therapy, medical bills, etc. Actual costs, however, are incalculable, as the non-productivity of these disabled is a far greater sum.

Perfecting spinal cord regeneration and μC/μP-transducer systems will automatically lead to breakthroughs in similar-but-less-accessible problems of brain damage, stroke, epilepsy, anti-aging, MS, palsy, amputees, etc. In fact, many ostensibly unrelated afflictions may actually share interrelated common denominators. Unfortunately, shortsightedness has hampered computer and cure-oriented research, such as the defeat of the Walgren Bill (HR 4358), which designated $16 million for SCI cure/innovation research. In reality, computers and cures will create more business—not less—and there is nothing to fear about the new market niches. In designing

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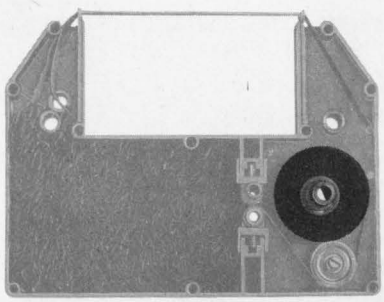

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your systems products, systems, sales and ad campaigns, if you appeal to security motives, you will have an edge over your competition, many who are high technology designers innocent to the unique problems of this field.

While we have discussed the design and technology aspects, another factor—the humanitarian aspect—also exists. SCI paralysis from a broken spine is the most terrible affliction known to man—all the malfunction and suffering of terminal cancer extended to a lifetime. Many things go wrong at once, among them: constant life-threatening bladder/kidney infections, digestive/bowel ailments, loose or frozen joints, life-threatening pressure sores, muscle atrophy and denervation, and bone deterioration, to name a few. Many victims are left isolated forever from family and friends; and, eventually, fewer visitors come to visit. Some beg to be killed.

. . . all the wheelchair ramps and traditional aids and curbcuts in the world won't make a paralytic walk.

Ten years ago this writer (W. Sniger) was rendered paralyzed from the shoulders down due to a spinal cord injury (broken neck). To an SCI victim, being unable to walk is the least of his problems. He is confronted with a lifetime of constant medication and hospitalization due to a myriad of problems including the loss of bladder and bowel control, kidney complications, and severe skin ulcers from lying or sitting, unable to move.

Reduction of architectural and attitudinal barriers, increased accessibility, more curbcuts on street corners and the like are laudable, of course. But, as much as we need them, all the wheelchair ramps and traditional aids in the world won't make a blind person see, a deaf person hear or a paralytic walk. Now, for the first time, there is hope: a combination of cure-oriented regeneration and μC-based systems. □

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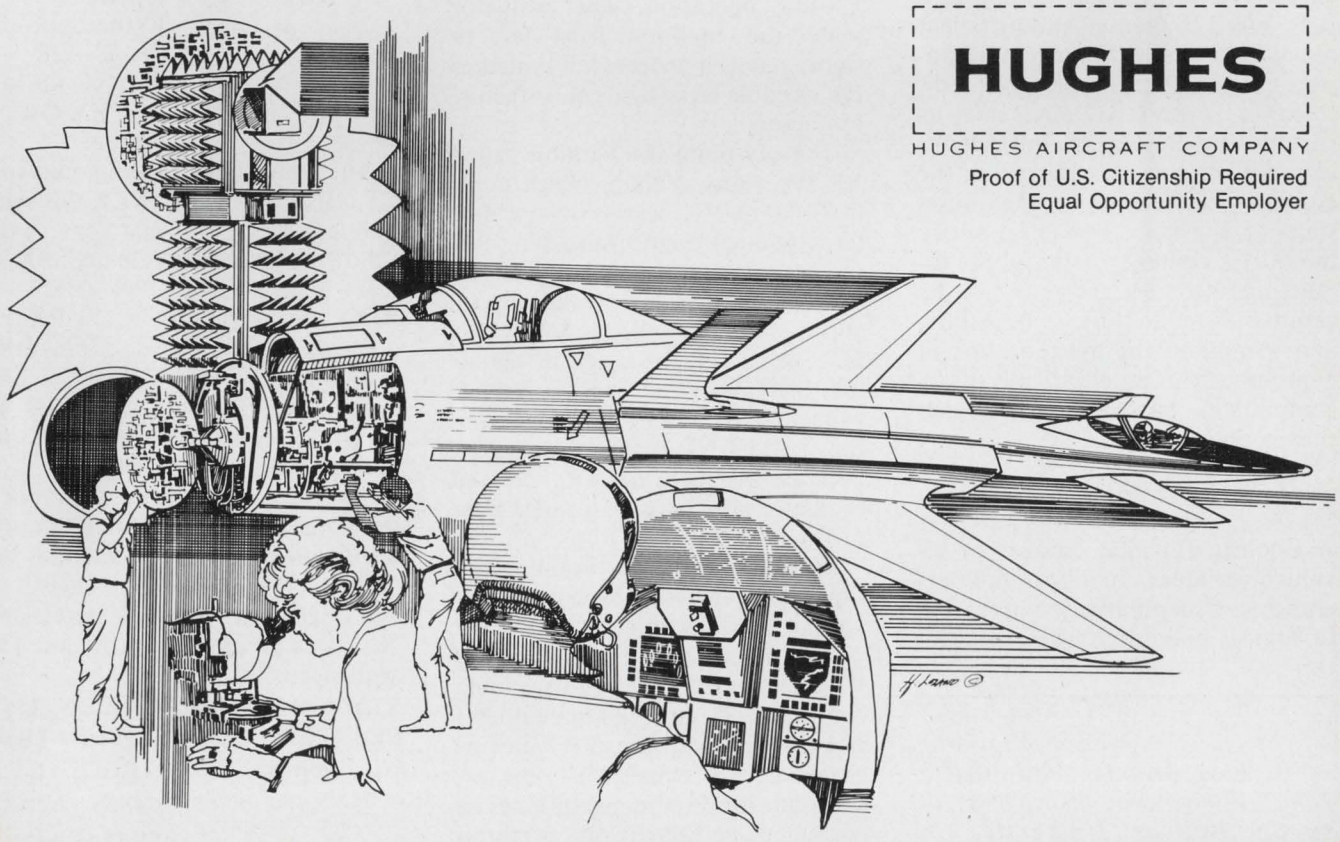

Boolean Resolver Operates As Combinatorial Or Sequential System

by Profs. Luis Alvarado and Angelo Yong Wong

Using an algorithm to evaluate Boolean functions and a μP system that incorporates the algorithm lets users program this machine to behave as a combinatorial or sequential system. It is a tool for studying digital techniques. By verifying their designs before mounting them on a breadboard, instructors and EEs can illustrate designs in a more tangible way, since simulations take only a few minutes to set up. This evaluator algorithm is a software approach for replacing digital circuits when time is not critical.

This evaluator algorithm allows verification of designs before they're mounted on a breadboard so EEs can illustrate designs in a more tangible way.

User Interaction

In this version, which we supplied with only a condensed and sufficient set of commands, the user may: input the Z- and Y-equations; edit them in a primitive way, such as substituting characters, but not inserting them except at the end of the equation buffer; input the initial state of the state variables, verify the buffer contents; solve all the input equations once and return to the command mode to check results; and command the machine to run continuously as an electrically TTL-compatible, but obviously much slower, logic circuit.

Boolean Function Evaluator

A Boolean function consists of bivalued variables, operators and parentheses. Commonly used operators or logical operations with Boolean variables are AND, OR, NOT and EXORS. For example: f(A,B,C,D, X1,X2,X3,X4) = X1 × 2′ + X3#A′ (BC#X2″)″D)X4, where # *equals* EX-OR operation. The evaluator scans the equation from left to right, and as it proceeds, it evaluates the variable term-by-term or factor-by-factor.

The key point is a variable called VP (Previous, Value), which is initialized to "1" every time a new term goes through evaluation. For the equation in the given example, VP is ANDed with the values of X1 and X2″ and the result is left in VP. Since what follows is an OR operator, the evaluator checks the VP value and assigns a "1" to the function "f", if VP = "1"; otherwise a "1" is assigned to VP and the evaluator goes on with the next item of the function.

When the evaluator examines an expression enclosed by parentheses and an inside term equals "1", the whole parentheses is disregarded, VP is assigned a "1" and scanning continues. If an open parentheses symbol appears, the VP value is checked; if it equals "1", the expression inside the parentheses is evaluated; otherwise it is disregarded.

These features of an evaluator reduce evaluation time significantly. To handle EX-ORs and parentheses in a function, we need to define a special stack. The reation to the appearance of an EX-OR symbol saves the VP in the stack and evaluates whatever shows up to the right of the EX-OR symbol to compute the EX-OR operation. The data structure used is:

PX→	CP∅ CP∅ VPX1	=Counts the number of "(" previous to the first EX-OR symbol.
	CPX1 VPX1 VPX2	=Stores the VP value here, when the EX-OR symbol is found.
	CPX2 CPX1 etc.	=Counts the number of "(" to the right of the EX-OR symbol, up to next EX-OR symbol.

The pointer PX always points to a CP cell except when an EX-OR symbol appears. In that case, the following actions take place: PX ← PX+1, (PX)←VP, PX←PX+ 1, (PX) ← 0, VP← 1. PX is decremented and EX-ORs evaluated, when CPXi = 0 and either an OR, ")", or END of FUNCTION symbol appears during the scanning process.

To understand the algorithm better, consider the stack manipulation during evaluation of function f = X1X2′ + X3 # A′ ((BC # X2″)″D)X4, where single letters and Xs with a number are variables. The sequence is:

STACK POINTER	STACK CONTENT OR OPERATION
PX = CP∅	(PX)←0/*Initialize parentheses counter*/

Profs. Luis Alvarado and Angelo Yong Wong are instructors at Simon Bolivar University in Caracus, Venezuela.

```
PX+1    =VPX1   (PX)←X3/*
                X1X2'=0
                assumed*/
PX+1    =CPX1   (PX)←0
                (PX)←1
                +1=
                2/*A'=1
                assumed*/
PX+1    =VPX2   (PX)←BC
PX+1    =CPX2   (PX)←0
                /*A")" is
                found*/
PX-1    =VPX2   VP←BC#X2'
PX-1    =CPX1   (PX)←(PX)-
                1=1
                VP←VP'
                /*(BC#X2')'
                VP←VP.-
                AND .D
                /*A")" is
                found*/
PX      =CPX1   (PX)←(PX)
                -1=0 VP←
                VP .AND
                .X4
                /*A'((BC #
                X2')'D)
                X4*/
                /*A
                FCTFIN
                is found*/
PX-1    =VPX1   VP←X3#VP
PX-1    =CP∅    (PX)=0 end.
```

The evaluator assumes that we have written the function correctly, except for the check it performs over the number of "(" and ")" parentheses. The nearby "Program Description" lists the detailed operations taken with each of the items of a given function.

System Description

At the university, we built a machine that incorporates the algorithm into a larger program that allows the machine to behave as a combinatorial network or as a synchronous or asynchronous sequential circuit. For combinatorial functions, we can define up to eight (Z1 to Z8) functions corresponding to eight outputs. The functions argument may include any of eight input variables (A to H) and/or the name of other functions. The user must be careful not to produce feedback loops among the functions.

Sequential circuits can handle up to eight state variables (Y1 to Y8), plus the eight output equations Z1 to Z8. When we symbolize the present states by X1 to X8, the state equations are characterized as follows:

$Y_i = f_i(A\text{-}H, X_j, Z_j)$

$i,j = 1$ to 8

$Z_i = g_i(A\text{-}H, X_j, Z_{j\neq i})$

Here the restriction for the Z-equations holds as before.

Hardware Description

We implemented the whole system around two μPs. One of them executes the evaluator program and the other is dedicated to user I/O interfacing.

Around the **first** μP, a 4-MHz Z-80A, we placed a 2708 EPROM, eight 8017 dynamic memories, one 8255A programmable peripheral interface (PPI) and ten small TTL ICs. The processor is powerful and allows a simpler, more elegant system design. For instance, the processor automatically refreshes the dynamic memories at the end of each fetch cycle without additional circuitry. We configured the 8255A PPI for eight inputs (variables A to H), for eight outputs (Z-equations),

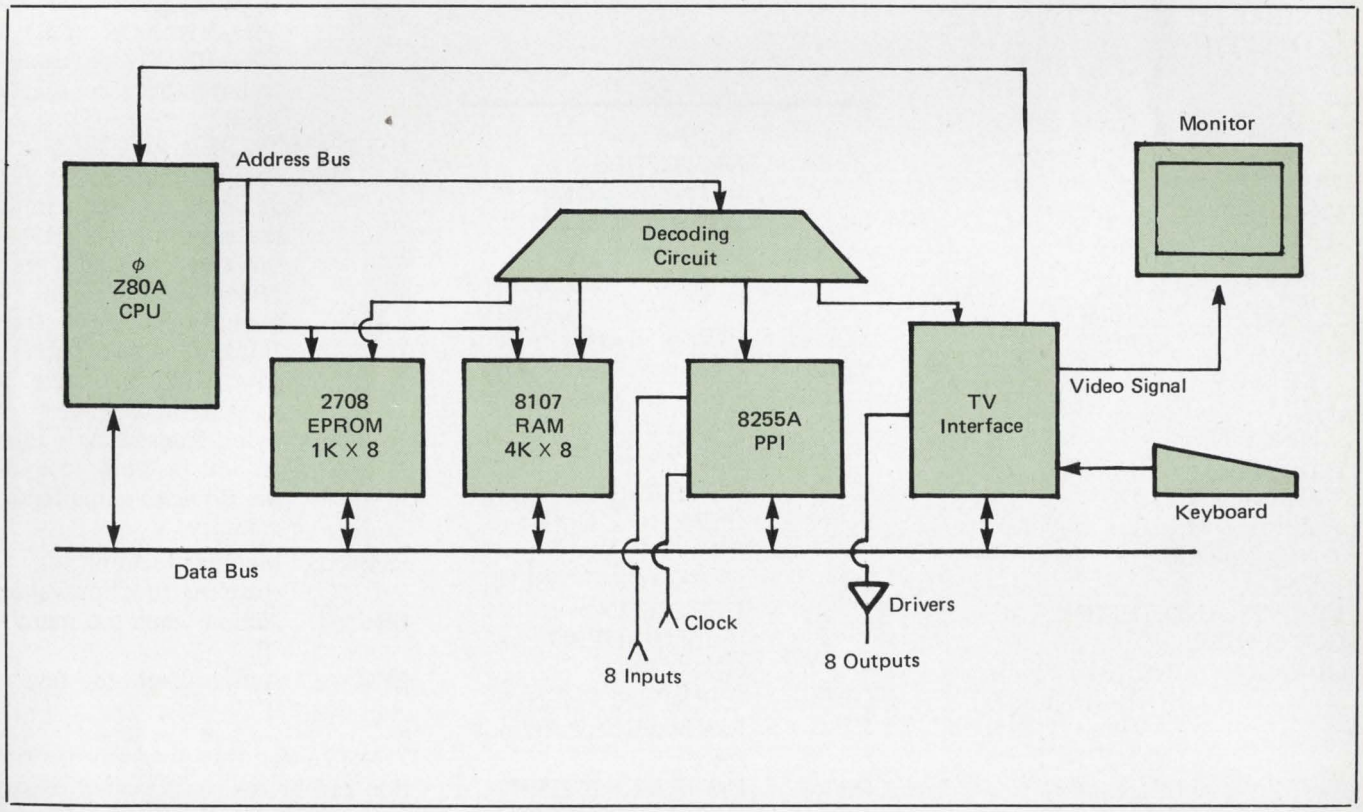

Figure 1: System block diagram. One μP executes the evaluator program; the other is user I/O-dedicated and is in the 22-chip block handling video screen character display.

and one line to clock state changes when simulating a synchronous sequential network.

The **second** μP is the heart of a 22-IC, low-cost circuit that displays characters on a raster-scan CRT. This circuit produces a video signal of about 3.5 MHz, compatible with conventional TV sets to display up to 512 characters. You can connect a TV set through a VHF modulator or a modified TV set to accept composite video to the circuit. The TV interface also accepts input from an ASCII keyboard. You may also connect this interface to any μP system as a conventional peripheral. The arrangement transfers characters at approximately 2000cps.

Program Description

Here is the program description for the Boolean function evaluator:

```
EVAL:PX←CP∅/*Initialize stack
pointer*/
INCI∅:(PX)←∅/*Parenthesis
counter with no XOR's
(CP∅)=∅*/
INCI1: VP←1/*Previous Value*/
INCI: NEXT ITEM/*Increment
FCT. Pointer*/
NINC: IF ITEM = FCTFIN THEN
GOTO FFIN
                    ='
                    ='('
                    =')'
                    ='+'
                    ='#'
                   INCI
                   OPEN
                  CLOSE
                   ORF
                   XORF
  TEMP←CALL      VALUE
(ITEM)/*  Item is variable*/
  NEXT ITEM
  IF ITEM=COMPLE-
  MENT THEN DO
  TEMP←TEMP'
  NEXT ITEM
  END
VP←VP .AND.TEMP
GOTO NINC
OPEN:      INC (PX)/*
           (PX)←(PX)+1*/
           IF VP=1 THEN
           GOTO INCI
           CALL LOC
           DEC (Px)
           NEXT ITEM
           IF
           ITEM=COMPLE-
           MENT THEN
           GOTO INCI
           GOTO NINC
CLOSE:     If (PX)=0 then
           DO IF PX=CP∅
           THEN GOTO ERR
           + CALL EXORSU
           GOTO CLOSE
           END/*For (A # B #
           C')' D type*/
SIGU:      DEC (PX)
```

The system is made up of two μPs — one executes the evaluator program, the other is used for I/O interfacing.

```
           NEXT ITEM
           IF ITEM=COMPLE-
           MENT THEN DO
           VP←VP'
                    GOTO INCI
                      END
           GOTO NINC
XORF:      PX←PX+1/* Storing
           VP in Stack*/
           (PX)←VP
           PX←PX+1
           GOTO INCI∅
FFIN:      IF(PX)=/∅GOTO
           ERR-
           IF PX=CP∅ THEN
           GOTO FIN
           CALL EXORSU
           GOTO FFIN
ORF:       IF(PX)=/0 THEN/*
           Parenthesis counter not
           zero*/
OR1:       DO IF VP=0 THEN
           GOTO INCI1 ELSE
           DO CALL LOC GOTO
           CLOSE END
OR2:       IF PX=CP∅ THEN
           DO CALL EXORSU
           GOTO ORF
           END/*Evaluates
           previous XOR*/
OR3:       IF VP=∅ THEN
           GOTO INCI1
FIN:       RESULT←VP/* Evalu-
           ation finished*/
SUBROUTINES
LOC:       /* Search for matching
           '('*/
           TEMP←(PX)
L1:        NEXT ITEM
           IF ITEM=FCTFIN
           GOTO ERR-
           IF ITEM='(' THEN
           DO TEMP←TEMP+1
                    GOTO L1
                      END
L2:        IF ITEM=')' THEN
                    GOTO L1
           TEMP←TEMP-1
           IF TEMP+1≠(PX)
           THEN GOTO L1
                      RET

EXORSU: /*EVALUATE XOR
           FUNCTION */
           PX←PX-1/*VP value
           from stack*/
           VP←VP .XOR. (PX)
           PX←PX-1/*Pointing
           to parenthesis counter*/
           RET
USER PROVIDED ROUTINES
VALUE:     Returns the Boolean
           value of a variable in
           the accumulator. Ob-
           serve that variables are
           related to address in
           memory containing their
           Boolean values. There-
           fore, VALUE receives a
           variable name (one
           byte), transforms it into
           an address and retrieves
           the Boolean value from
           memory.
RESULT:    Memory location to
           store the function value.
ERR+:      Action when too many
           ')'.
ERR-:      Action where too few
           ')'.

/*Notice that this program descrip-
tion can be easily translated to any
assembly or BASIC-like language.□
```

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Is Your 64K Dynamic RAM Refresh Scheme Killing Your μP Performance?

by Dick Brunner, Motorola, Inc., MOSIC Div., Austin, TX

One of the major applications for 64K dynamic random access memories (DRAMs) is main memory for μPs and computers. Their high density, low power and fast access make them ideal for this application. To accomplish this high density and low power, the 64K dynamic RAM employs a storage element consisting of a select transistor and storage capacitor. Digital information (logic zeros and ones) are stored on these storage capacitors by the presence or absence of charge. This type of storage mechanism requires a periodic update of the capacitor charge state to insure that the stored information is not lost due to leakage current.

To insure the capacitor's charge state, a periodic refresh cycle is performed on all memory cells; which for most 64K DRAMs is accomplished with 128 refresh cycles every 2ms.

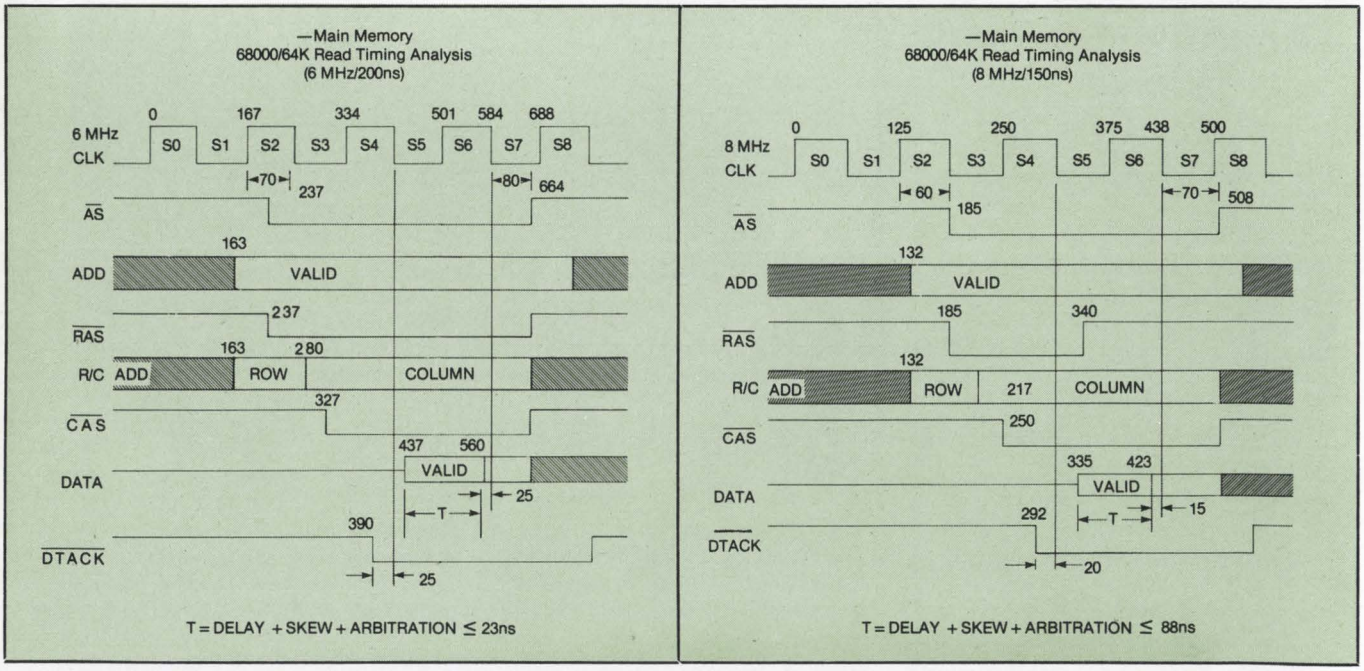
Potential increase in data throughput is 22% if MPU refresh control is used vs. that with memory controlled refresh.

On the surface, it appears that implementation of the refresh cycles along with the normal μP or computer cycles would be straightforward and have minimal effect on data throughput. However, a close look reveals that implementation of these refresh cycles dramatically impacts data throughput of all high performance asynchronous μPs and computers.

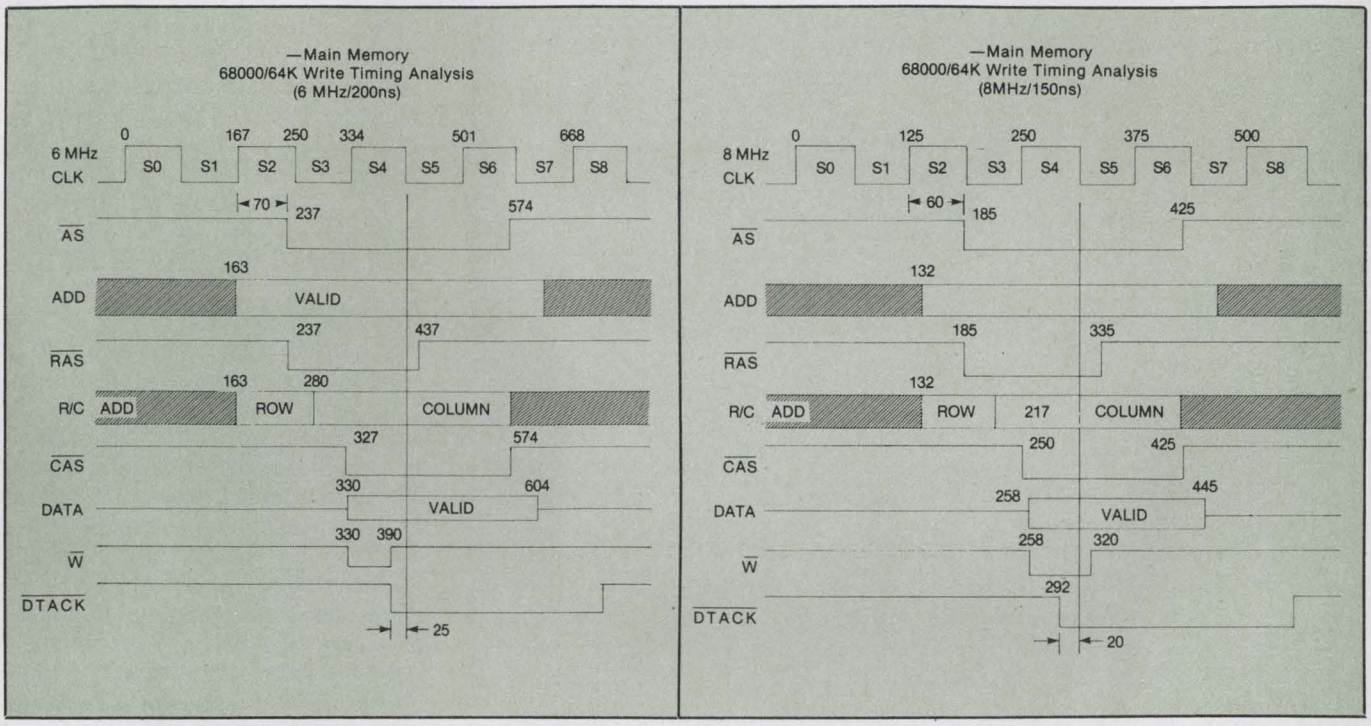
Slave Peripheral

Main memory is not generally regarded as a peripheral, but is in actuality. In fact, the memory is a slave peripheral that must interface with at least two master controllers—μP or computer and a refresh controller which will insure that the memory maintain valid data. Since both controllers are asynchronous to each other, there will be brief periods in time when both are trying to access the memory at the same time.

To insure an orderly synchronization of these signals during the periods of contention, arbitration logic is necessary. When two signals of dif-



Figures 1a and 1b illustrate the maximum data valid window for a read cycle for both a 6MHz and 8MHz 68000, with respect to both a 200ns and 150ns access part.



Figures 2a and 2b show the comparable worst case timings for a write cycle. Note that data valid does not occur at the beginning of the cycle.

ferent frequencies are to be synchronized, there will be periods when input parameters are violated and the logic device output will enter an undefined state for a period of time. Eventually the logic device output will settle into a stable state. For an S74 type latch this period can be as long as 75ns.

This extended period of time for a bi-stable latch to settle out can be sufficient for a high performance μP system to result in a design that requires the μP to generate wait states on all memory cycles. To illustrate this, let us examine the bus timing of the 68000 with respect to the timing requirements of the MCM6665 (64K DRAM). **Figures 1a and 1b** illustrate the maximum data valid window for a read cyle for both a 6MHz and 8MHz 68000, assuming no wait states, with respect to both a 200ns and 150ns access part. Note from these figures that for a worst case 68000 read cycle time, and assuming zero logic delays, that the minimum to maximum data valid window T is only 123ns and 88ns, respectively. If arbitration is required in the memory control logic to accomodate the refresh cycles, then the available time left for bus and timing logic is only 48ns and 13ns, respectively. Even using Schottky logic it would be virtually impossible to have a conservative design that would not require wait states during the read cycle.

The comparable worst case timings for a write cycle are given in **Figures 2a and 2b.** Note for a write cycle that the

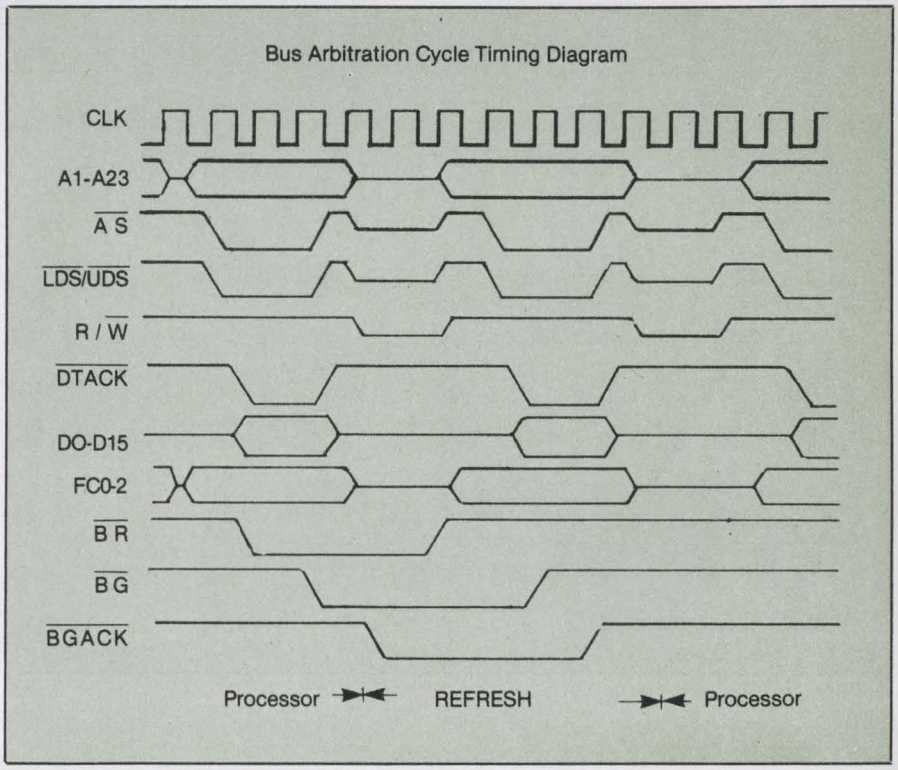


Figure 3: The 68000 can handle the bus arbitration of the refresh cycle requests.

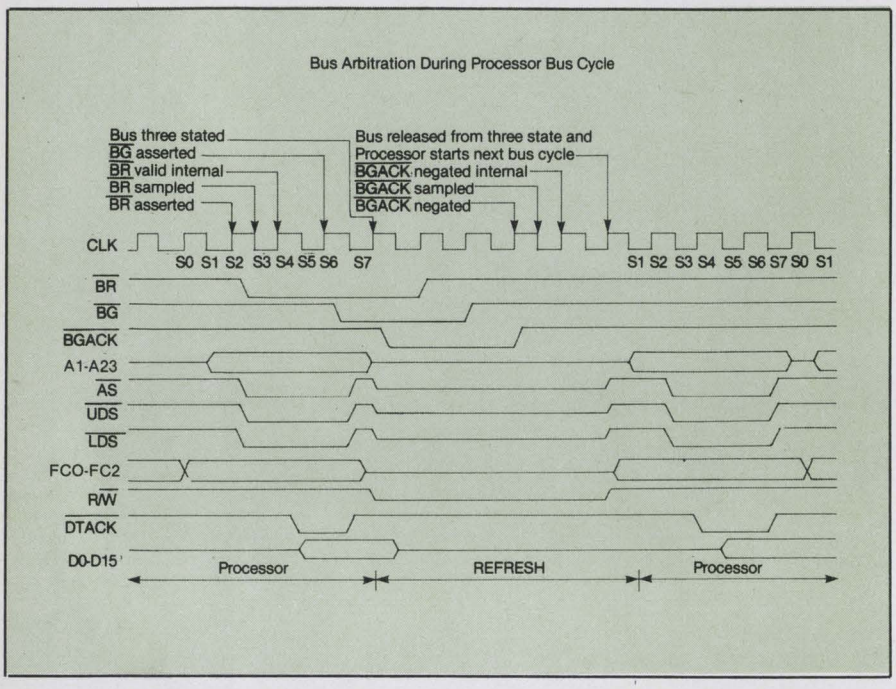


Figure 4: The 68000 acknowledges the refresh cycle and the refresh controller originals that it has control of the bus.

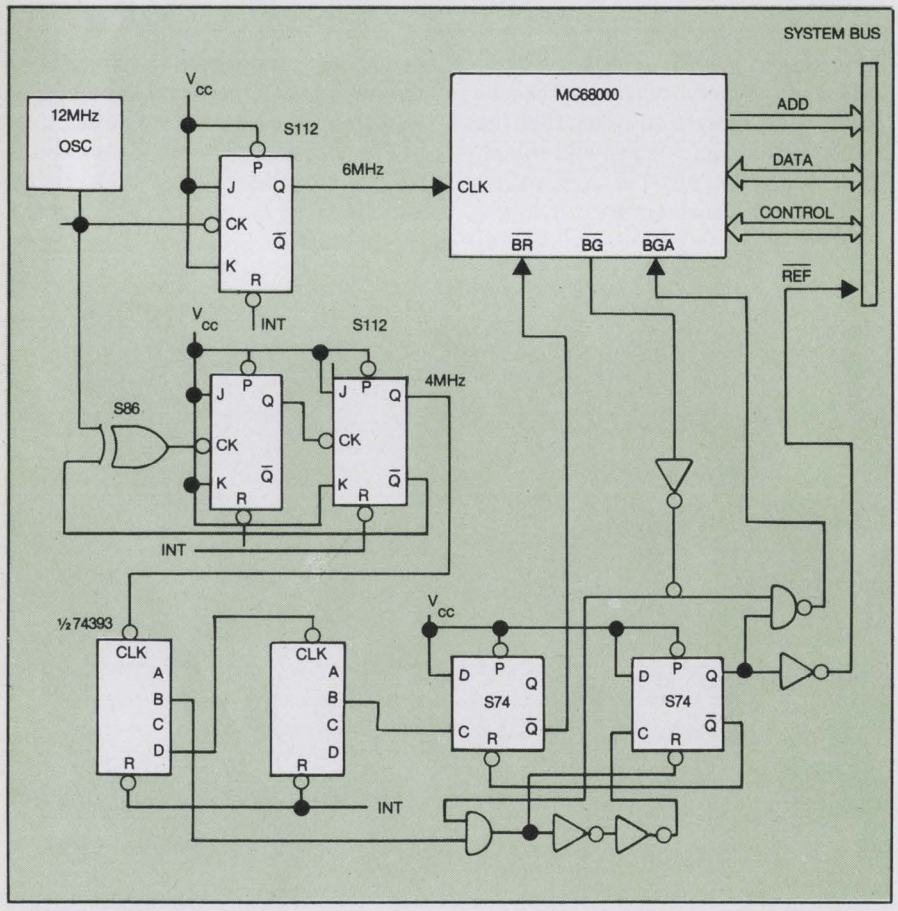


Figure 5: Illustrating a refresh control scheme for a 6MHz μP.

timing of the 68000 and the 64K are more compatible; hence, they will not require wait states to accomodate arbitration. It should be noted however, that the data valid does not occur at the beginning of the cycle ($\overline{AS}$ going True); hence, to minimize the write cycle time and accommodate the late data valid, a late write cycle is required.

Moving onto the μP Card

Fortunately, there is an alternative system design approach that will accommodate the dynamic refresh without having to suffer the arbitration overhead on every memory cycle. The refresh control logic can be moved to the μP card and integrated into the control and clock circuitry of the μP. Since the 68000 is an asynchronous μP, it was designed to easily accomodate asynchronous interrupts. It has internal logic to arbitrate incoming asynchronous interrupt requests such as refresh. And, noted in **Figure 3,** the 68000 can handle, very time efficiently, the bus arbitration of the refresh cycle requests. Through the bus arbitration logic of the 68000, a refresh cycle request can be initiated by driving the bus request ($\overline{BR}$) input low. The 68000 will acknowledge the refresh cycle when bus grant ($\overline{BG}$) is asserted. The refresh controller signals that it has control of the bus with a bus grant acknowledge ($\overline{BGACK}$) signal: this sequence is illustrated in **Figure 4.** The above refresh control scheme for a 6 MHz μP can be accomplished with the logic design given in **Figure 5;** the system design for the μP/memory interface and refresh logic is illustrated in **Figure 6.**

This μP/memory refresh scheme will require only two μP read cycles to accomplish the refresh cycle. The following analysis gives the maximum possible data throughput possible with MPU refresh vs that possible with a wait state for every memory cycle:

μP Refresh Control (memory cycle = 668ns). Refresh Period = 16 μs. Maximun number of cycles possible during this period is 24. Total μP cycles possible is 22.

Memory Refresh Control (memory cycle = 835ns; assume one wait state for each cycle). Refresh Period = 16μs. Maximum number of cycles possible during this period is 19. Total μP cycles possible is 18.

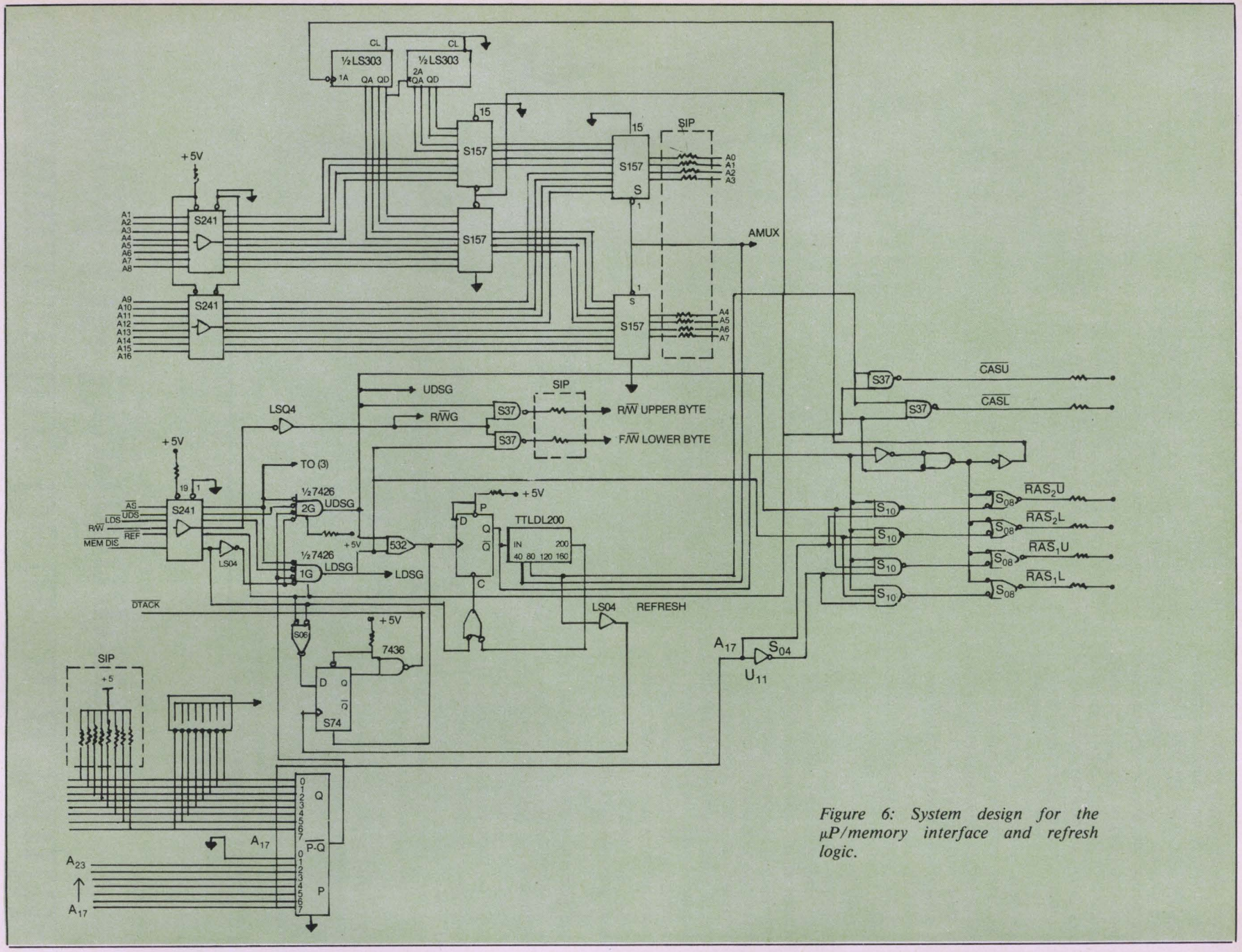


Figure 6: System design for the μP/memory interface and refresh logic.

Communicating Data in a Multiprotocol DP Environment

by Michael Roberts

Soon, millions of computer terminals in the distributed processing environment will tie into tens of thousands of interconnected computers in hundreds of different commercial, industrial, governmental and educational networks.

The needed links between widely dispersed equipment and data bases will be provided first by programmable multifunction and multiprotocol information resource management terminals. These terminals will be successors to today's mainframe dependent and protocol specific "dumb" and "smart" terminals. Unlike earlier generation units, new multiprotocol terminals can, under user control, "talk" in any communications protocol. Eventually, with the introduction of high performance 16-bit μPs, high density RAMs, and new specialized peripheral ICs to the design of such terminals, they will be succeeded by sophisticated information stations. The means of communication in these stations will be completely transparent to the user, will automatically recognize what is coming over the transmission line, will automatically catalog the protocol and will automatically switch into that mode.

How far away are such multiprotocol, multifunction information stations? To determine that, it is necessary to review requirements of various data processing environments within which terminals must operate.

Michael Roberts is with ECS Microsystems, Inc.

Multifunction, multiprotocol information systems ease the distributed processing confusion.

Confusion Reigns

The present distributed processing environment is at the very least confusing. Not only is the variety of network control architectures confusing; but also bewildering are transmission systems and technologies, data communication software, processor configurations and hardware requirements.

The confusion is most obvious when one looks at the network control architecture options that are available to the user. Whether he wants them or not, there are a variety of choices that must be made at various protocol levels, including: physical interfaces, electrical interfaces, link controls and message handling.

Physical interfaces. This is probably the only level at which there is some universal agreement. Most manufacturers agreed on the RS-232C for connections between data terminal equipment and data communications equipment.

The RS-232C defines electrical interface requirements. But there are a number of new options available here also, including RS-422 and RS-423, to name a few. Outside the United States there are the CCITT telecom standards.

Data link protocols. The next protocol level is that of link control, including asynchronous protocols (Teletype and IBM 2740); synchronous character oriented protocols; binary synchronous character oriented protocols; synchronous bit-oriented protocols (SDLC, ADCCP, HDLC, X.25, BDLC, BOLD and CDCCP); and synchronous/asynchronous byte-oriented protocols (DDCMP, NSP and DAP). Each single protocol has a number of subprotocols, corresponding to the levels or layers in various network architectures.

Transmission systems and technologies. The variety of transmission systems and technologies is almost as confusing as the number of protocols. The most common transmission systems, but by no means the only ones, are common carrier microwave networks, value added common carriers and satellite networks. Each uses a variety of transmission technologies, including: voice-grade telephone lines, private lines, terrestrial microwave radio, satellite technology, millimetric waveguides and optical fibers.

Network structure types. The terminal user must contend with a variety of network structure types including the hierarchical, star, ring and multistar or starred ring approaches.

Data comm software. In terms of software, there are at least two levels or layers. Terminal users must contend with the operating system and the communications based access software.

There are as many operating systems as there are CPUs. They vary in scope from large scale

systems for general purpose mainframe computers to specialized systems for minicomputers. The various types of operating systems associated with some well-known mainframes include: BOS/360, TOS/360, DOS/360, OS/360 PCP, OS/360 MVT, OS/360 MFT, CP-67/CMS, TSS/360, DOS/VS, OS/VS-1 and VM/370.

Associated with each operating system are a variety of communications-based access software modules. For IBM mainframes, there are at least three: VTAM, the basic telecomm access method; TCAM, the standard telecomm access method; and VTAM, the virtual telecomm access method.

This proliferation of protocols and interfacing requirements is continuing, with new procedures introduced with each new CPU. This is hardly an environment conducive to distributed data base use.

Some Partial Solutions

Fortunately, there are partial solutions available— systems incorporating some elements of the relational solution. These user programmable terminals are available now from a variety of firms, including Applied Digital Data Systems, Codex, Datapoint, Digi-Log, Four Phase, Incoterm, Sycor, Ontel, Ramtek, Raytheon and Zentec.

These systems have two drawbacks: In terms of marketing, few if any are aimed at the standalone market. Most are aimed at emulating the terminals used in various mainframe-oriented hierarchical networks. Even those which have cluster capability are still tied in one way or another to a specific CPU or network.

A More Complete Solution

There is a more complete solution to the problem of interfacing too, and operating within a multiprotocol distributed processing environment. That solution would combine all the elements just discussed into a single multifunction, multi-protocol information resource management terminal.

Unlike limited data processing function terminals just discussed, advanced terminal designs can support all major mainframe protocols and can be used in a variety of configurations, including: standalone data processing, distributed processing (functional and hierarchical), network operation (ring, star and strip) and point to point communications.

An advanced terminal design can be built around a noninvasive architecture and software which can interact with the host as well as the terminal functions. This requires that the terminal's operating system handle the host protocol functions to which it is currently connected. It can then respond to the inquiry of any one of a number of mainframe host CPUs and convert to the terminal's native mode. Via a wide array of software packages, units can be programmed to operate in a variety of different data protocol environments. Let's look at several.

Small systems. As a standalone system, it would have sufficient memory capacity and I/O ports to operate a printer equipped with a serial ASCII interface.

Small networks. The single serial I/O port would be used to link systems together.

Mainframe-connected networks. It will be most useful as devices which are on-line only, thus alleviating much communications overhead required at the central computer. The broad range of ECS communications modules and software packages makes possible connections with most computer systems.

Long-line communications. Communications between a maximum of eight systems linked via a common co-axial cable up to 4500-m long and at rates up to 19,200 baud are possible. A coaxial signalling unit incorporated on an optional input/output module accomodates full duplex communication of data and modem control signals by time-division multiplexing.

Flexible communications capability involves a software library of communications modules that would include the IBM (3270), ICL (7181), Honeywell (VIP7750), Burroughs (TD830), Univac (U200), NCR (NCR796), H-P (HP2640A) and DEC (VT52).

In a disk-based computing terminal, the protocol software is loaded into the system memory from disk. This is done to service the communications interface when it is connected to a central computer system. The modules would all have identical interface parameters to standardize their linking with other system or user programs.

The key concept in architecture is that major subsystems all operate automatically and independently of each other. Thus the processor video subsystem, disk subsystem, and memory should all share a common interconnection bus, with the first three capable of independently accessing the memory. Such a system would incorporate a dual-drive floppy disk system with a special track format. Such a disk system makes possible the storage of 250,000 characters/diskette and 208-kB RAM arranged in up to four banks. These banks could be switched into the 64-k address space one at a time by the CPU for non-simultaneous access by any bus subsystem.

DOS must be selected for maximum compatibility with existing μP application software written by others. Thus, it should immediately accept, in almost all cases without any modifications to the particular application program, a broad range of accounting, stock control, WP and other applications written into, say, the CP/M standard. CP/M is commonly employed in μP DOS.

Protocol interfacing. If communications protocol modules are loaded into the system memory from disk to service the communications interface when it is connected to a central computer system, then modules should all have identical interface parameters to standardize their linking with other system or user programs.

There are two basic types of interface routines — data transfer requests and wait requests. A **data transfer request** initiates the transfer of data to or from the record specified via specified protocol. Only one transfer request of a particular kind is allowed to be in operation at any one time. Any attempt to do otherwise will be ignored, and an error condition is generated. Received

data is buffered and data can be received at any time provided that there is buffer space available. A receive transfer request initiates the transfer of data from the buffer to the user record area. If no data is available at the time that the request is issued, then transfer will commence once the data has become available. The programmer must ensure that the receive request has terminated "complete" before trying to access the data record.

Transmitted data is not buffered. Data is transmitted directly from the user record area. Consequently, once a transmit request has been issued, the programmer should ensure that the request has terminated "complete" also before changing the record being transmitted.

The **wait request** is a generalized "idle" routine and returns upon the completion of any current data transfer request. When it is returned a status information byte will be stored at the address. The meaning of the status information is dependent on the implementation; and similarly, the address facilitates for data transfer requests are also implementation-dependent. But usually, the address will appear at the start of the user data record.

Achieving Protocol Transparency

Today's programmable terminals aren't suitable for complex distributed processing environments. They lack protocol transparency; that is, operator intervention is required to select protocols.

Until recently, few computer systems (let alone terminals) had this feature. The exception was in some large front-end communications processors where multiple protocols are supported (as in Univac's Distributed Communications Processor). These large units are the start of automatic protocol recognition, but are limited to specified port allocations and function as large switchboards to the host.

This, however, is a different activity from the one a terminal performs. The terminal must recognize a number of protocols which are sent to it from a number of different hosts. Along these same lines, in sending data to a host, the terminal must recognize or know the host's protocol. The protocol can be deciphered in the handshake routines. However, the host must not respond in an ambiguous manner nor disconnect before the analysis has completed its task. The technique for this function is similar to decoding. This pattern matching procedure can be adapted to terminal designs by building on top of the existing operating system software or building a completely new system where portions of the multiprotocol capability are made available in hardware.

Implementing protocol transparency into a terminal using software techniques is fraught with difficulty.

Software solutions. Implementing protocol transparency into a terminal using software techniques is fraught with difficulties. Although similar in format to allow much commonality in software, they are not interchangeable. Control and response code differences exist and the different bit-oriented protocols may not share the same classes of procedures. These classes establish procedural differences for different applications. Each class implements a subset of the elements of procedure. All classes use the standard frame structure, however. Nonetheless, ANSI has defined six classes covering normal, asynchronous, and primary to primary nodes. ISO has five classes covering the same basic applications.

Another problem with software approach: protocol layer implementation is very performance sensitive. If, for example, lower level protocols are implemented in a way that would result in excessive operating system overhead, total system performance will degrade. If, on the other hand, lower level functions (data link and end to end data transfer control) are removed from the various protocol layers and imbedded in the operating system (to improve total system performance) the clarity and flexibility associated with strict hierarchical layering will be lost.

Hardware solutions. Fortunately, significant activity has taken place in terms of incorporating data link control protocols into hardware, either into separate microprocessors, or into data link control ICs.

As a result, next-generation successors to today's programmable, information-resource management terminals will see much of the software-supported data-link control function taken over by hardware.

Since most are programmable, they can support more than one data link protocol. Also, some of these chips can support data rates up to 2Mbps and several protocols such as Bisync and DDCMP. In addition, features such as modem control for point-to-point communications, loop back for self test, secondary address comparison and global address recognition have been incorporated into several of these chips.

A Long Way To Go

Data link protocols satisfy only one problem level. They are not a network protocol nor do they control the flow of information between users in a multinodal network. Mechanisms to unravel these additional layers are in development; the ultimate solution will be a software/hardware combination.

Incorporated into the multifunction, multiprotocol information stations of the near future, these solutions will result in all data handling capabilities concentrated into one local unit, providing both local transaction capability and access to all system functions. As a result, an entirely new type of distributed processing network environment will evolve, a network optimized for information-base management functions based on multifunction, multiprotocol information stations. □

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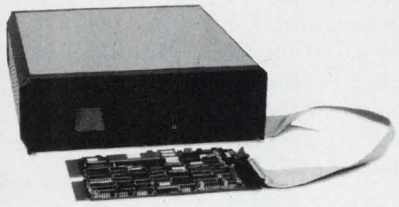

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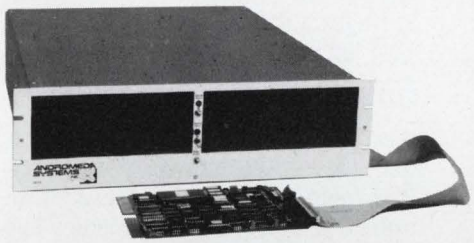

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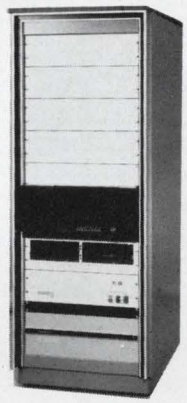

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Optical Memories Increase Disk Capacity

by Richard Klein

Since the digital computer emerged from its cradle, engineers proposed and built a bewildering variety of data storage equipment utilizing optical techniques. Using combinations of elements such as lasers, holograms, liquid crystals, etc., these optical memories have had one factor in common: they had no commercial impact or importance. This is now beginning to change.

The disappointing history of optical memories will come to an end with the current effort and progress in optical disk storage. The optical disk, developed for an entirely different market, may ultimately find its most important application in computers.

Optical disk memory is a stepchild of the consumer video disk development effort. In video disk technology, several technically incompatible methods were brought to market, primarily a laser-based system (Magnavox/Philips) and capacitive system (RCA). It is unclear which, if either, will prevail.

Independent of the outcome, the Optical Data Storage (ODS) market appears certain to impact computers. The technology is based on the laser disk approach, the only practical alternative because of the laser's ability to write and read stored information.

As in the video area, much of the pioneering work was done by N.V. Philips. Other pioneering companies include RCA, Thomson/CSF, and Drexler Technology.

One reason for the interest is shown in **Figure 1.** For mass storage, ODS promises the lowest cost/bit.

ODS Technology

At present, ODS is a write-once/read-only memory. In simplified form, the system consists of an optical disk 30cm in diameter. The disk is coated with an ablative material encapsulated within an optically transparent glass or plastic envelope. A laser, focused to a submicron point, is initially used to write data onto the disk by blasting tiny pits into the ablative materials as the disk rapidly rotates. The same or a different laser detects the presence or absence of these pits to read out stored information. Let's consider ODS system elements in greater detail.

The Optical Disk

One major advantage is the extremely high data density achieved with optical techniques. Magnetic tape data density is 40 bits/mm; magnetic disks, 150 bits/mm; optical disks, 1500 bits/mm. Informa-

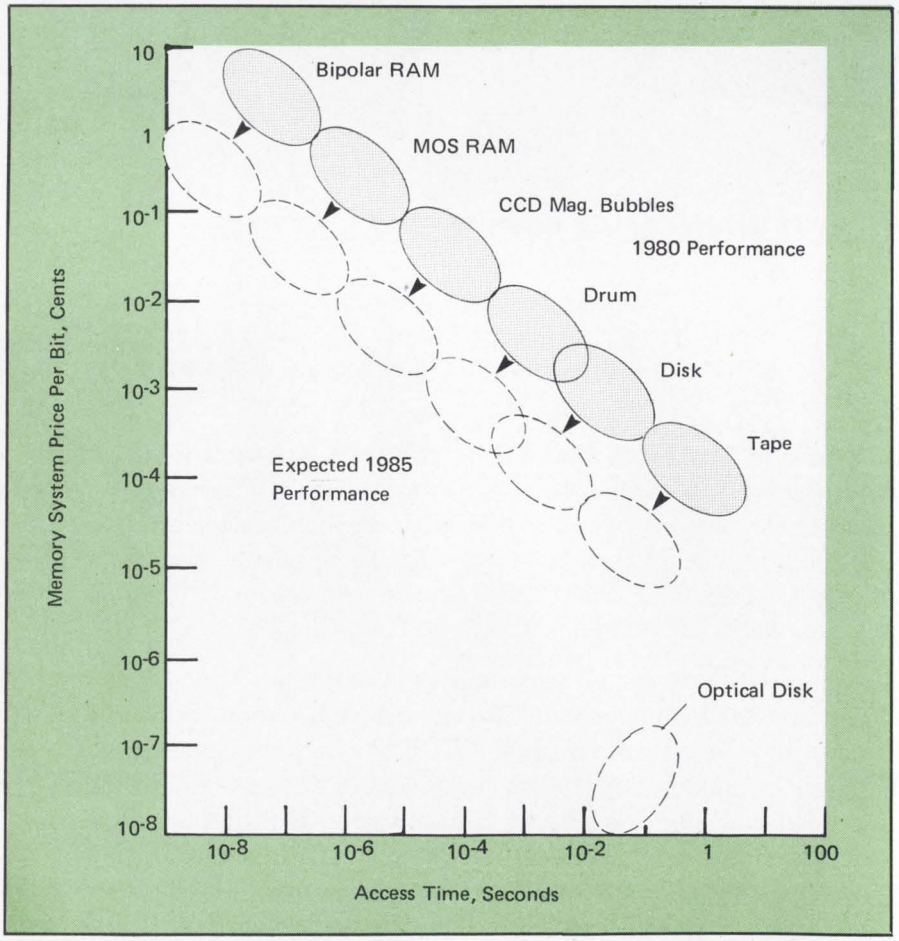


Figure 1: Price per bit versus performance for various computer storage technologies.

Richard Klein is Device Marketing Manager for Laser Diode Laboratories, Inc., 1130 Somerset Street, New Brunswick, NJ 08901.

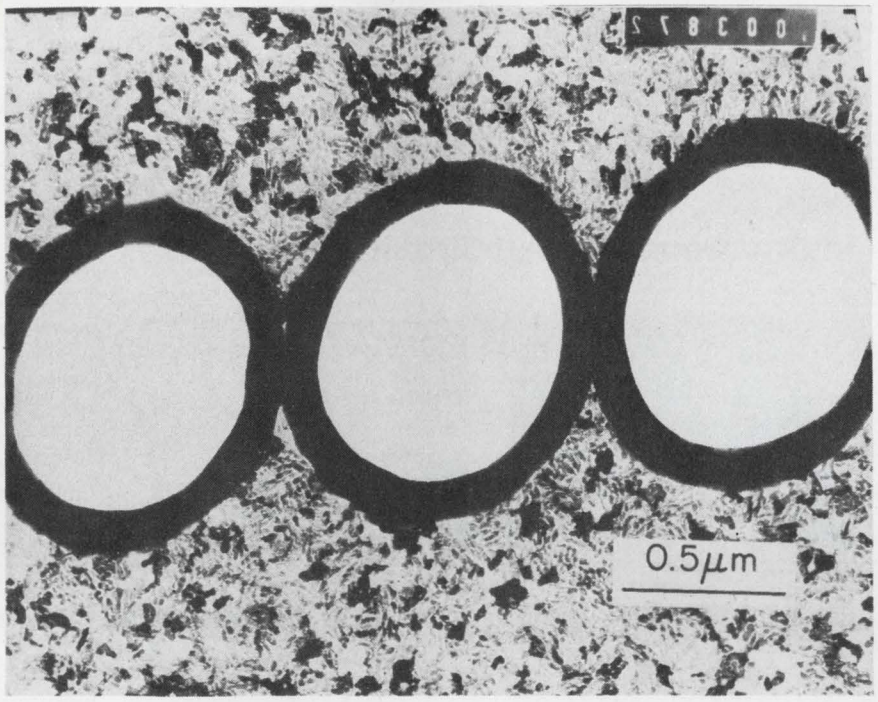


Figure 2: Laser generated pits in tellurium compound optical disk. (Source: N.V. Philips).

tion packing density for optical storage is an order of magnitude greater than for magnetic media.

A typical magnetic disk, such as the IBM 3340, has a 70-Mbyte capacity with a 35-ms access time and 70-Mbs data rate. A magnetic tape system such as the IBM 3420-8 contains 91 Mbytes with a 45000-ms access time and 3.3-Mbs data rate. The N.A. Philips optical disk, on the other hand, has a capacity of 2500 Mbytes (2-sided disk), a 500-ms access time and 5.2-Mbs data rate.

Philips and Drexler Technology pioneered disk development. Philips originally used pure tellurium as the ablative disk coating. More recently, tellurium-based compounds were used due to better life, easier handling and reduced toxicity. **Figure 2** shows pits burned into such a tellurium compound optical disk material by a gas laser. Note the extremely small size of the spots and very high packing density.

Drexler Technology, alternately, developed an ablative coating of fine, reflective metallic particles (typically silver) colloidally suspended in an organic film. Drexler projects archival life of over ten years. Other companies such as Kodak, Xerox, RCA and 3M are developing their own disk coatings.

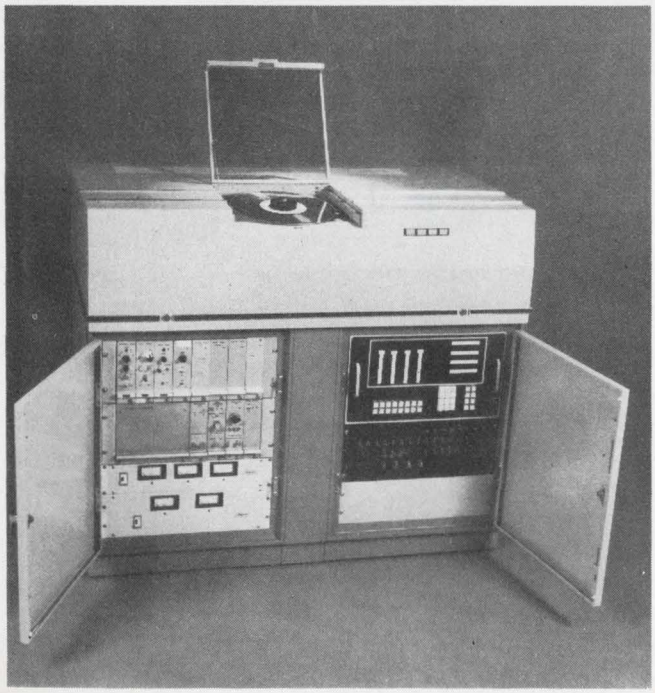


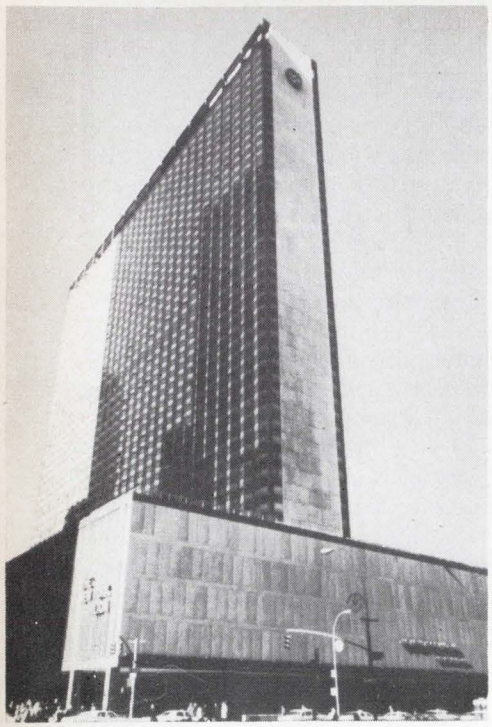
Figure 3 Optical Data Storage system developed by N.V. Philips.

The Laser

Original development efforts in ODS were achieved using gas lasers, typically Argon or HeCd types. The N.A. Philips optical data storage system shown in **Figure 3** employs such a gas laser. Recent advances in laser diode technology give promise that these semiconductor lasers will be used in the vast majority of future optical memory systems.

Being a semiconductor, the injection laser diode is inherently much more compact, rugged, efficient, simple to operate and, most importantly, potentially less expensive than other laser technology. The diode laser is typically packaged in a transistor-type can. A typical laser package (a coaxial TO-5 can) is shown in **Figure 4**. Its output is directly related to the current passing through the diode, making it simple to modulate and control.

Many technical problems must be overcome before these laser diodes are optimized for the ODS market. Areas under intense investigation are the output power required, laser's mode structure, laser's output wavelength, packaging, associated optics and feedback control, and most significantly, the cost of the laser. Despite all these unresolved questions, ODS systems using diode lasers have been demonstrated. The laser diode is the laser of choice for most presently-planned commercial systems.



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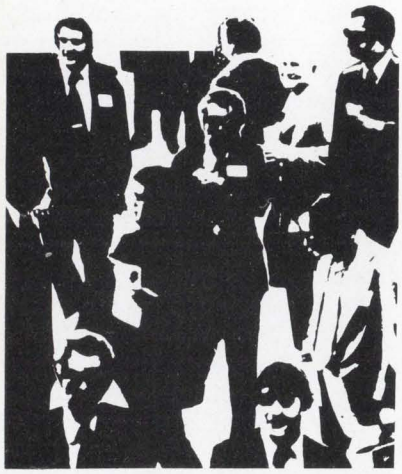

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Additional Considerations

Other problems exist. For example, disk life is unresolved. No uniform testing or measurement techniques were proposed or adopted. Laser lifetimes are arbitrarily specified. In both cases, however, experience indicates adequate lifetimes (however defined) are presently available.

"lazy susan" type disk changers. The latter, resembling familiar audio record juke box changers give promise of mass memories of 25 x 10^{12} bytes of storage with an access time of 5 to 10 secs for any information bit. Estimated cost is under $250,000.

Another outgrowth of this technology is for document storage. The

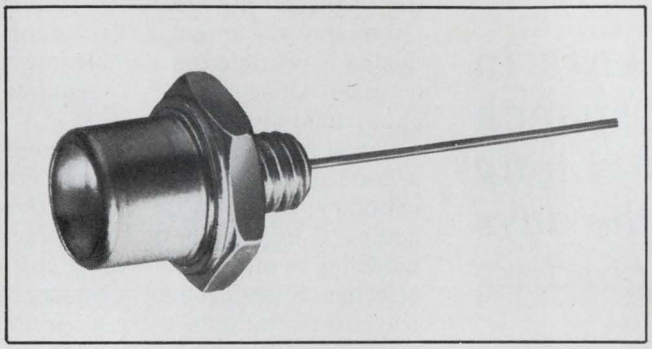


Figure 4: Typical diode laser package. (Source: Laser Diode Labs)

Given the write-once/read-only technology, error detection and correction is important. Schemes were proposed and evaluated. Philips' "sectoring" technique checks data and rewrites it in a following sector if there is an error. Using this technique, Philips obtained a BER of under 10^{-10} on an operating system. Obviously, whatever scheme of error correction is used, it will reduce useful storage capacity. However, capacity will still exceed 10^{10} bytes/disk.

Several companies, such as RCA and KDD Research and Development Labs, are working on erasable disk materials. Eraseable disks will eventually become available and provide direct competition to magnetic media.

The consumer video disk systems assign approximately six information bits to each pit. ODS to date has generally assigned only one bit/pit giving it a better SNR. As technology improves, some of the S/N margin can be traded for higher data storage densities. Thus, individual disk capacities of over 10^{11} bits may soon become feasible using more compact encoding schemes and improved optical design.

Multiple Memories

Proposed mass-storage methods range from stacks similar to magnetic disk packs to "juke box" and "Megadoc" system demonstrated by N.V. Philips can store up to 25,000 standard 8½" x 11" documents in high-resolution video format on a single disk using information compression techniques. Tying such a system into a company's computer may rapidly revolutionize future document and record keeping procedures.

The Immediate Future

Many companies are committed to major programs in this field. Magnetic Peripherals' major effort is at their Colorado Springs facility. Storage Technology established its own effort in Boulder and recently purchased Exxon's Star Systems operation and is moving it to Boulder. Shugart formed a division named Optimem to pursue work in this area. RCA received over $4.5 million in funding from various DoD agencies in support of development of a military version of ODS. Drexler Technology and Philips pioneered this technology and remain strongly committed to many different aspects of it. Other potential players include Omex, Xerox, Kodak, NCR, Burroughs and almost certainly IBM.

The question is when will ODS enter the market — not whether it will. Initial introduction could be by 1983, with full-scale manufacture by late 1984. □

Electronic Speech— A New Dimension

Compiled by Philips, Eindhoven, The Netherlands

Developments in electronic speech have come a long way since the days of tape recording systems.

Early all-electronic systems converted speech into digital signals and stored them in semiconductor memories. However, this method required a massive amount of memory for only a short announcement time.

Today's voice synthesis, dramatically reduces memory requirements. Memory size depends on the speech quality. Synthesizing speech is possible because the signals contain redundancy and are very predictable.

The Three Criteria

Judge voice synthesizers by understandability, speech quality and cost. Human-like speech is high quality; if robotic, it is low quality. And, in many consumer applications, synthesized speech should sound like the voice of a particular speaker.

Compromises must be made between speech quality and cost. Every application weights the three factors differently. For large vocabularies, cost depends on memory size.

What Is Speech?

The phoneme, the basic element of speech that represents a simple sound, cannot by itself distinguish words. Although English has about 40 phonemes — 16 vowel and 24 consonant sounds — there is much redundancy. Normal speech rate is 10 to 15 phonemes/sec., including silence intervals. Since about 40 phonemes can be coded using 6 bits, the normal bit rate for phoneme reproduction is around 90 bps. This is only phoneme information and is one of the many parts of speech to be reproduced. Combined with inflection, volume, emphasis and so on, phonemes are the building blocks of speech. Any satisfactory voice synthesizer must therefore faithfully reproduce all the necessary speech attributes.

Bits per second directly affects the number of words that a system can remember. The more bits used to describe a sound, the more accurate the sound's re-creation. However, because of limited data storage, the more bits used per sound, the smaller the sound storage capacity.

Methods Of Voice Synthesis

The following three principal methods of generating speech are applicable to LSI.

Phoneme coding slices words into their building block sounds, and each phoneme is programmed into the voice synthesizer's memory. Phoneme codes are extracted from memory and combined as needed. Data rates are very low (typically 70 bps), but speech quality is poor. If a human-like voice is essential, forget phoneme coding.

Waveform coding samples, digitizes and compresses the waveform by eliminating symmetrical redundancy and silence intervals, and adjusts phase information (in the digitized speech). It stores this simplified waveform in a memory chip. To regenerate a sound, it reverses the process to recreate sound resembling the original. Very good quality is possible for high bit rates; a male voice synthesis requires about 1000 bits/word.

Vocal tract modeling if you need a good quality voice and large vocabulary, the linear predictive coding (LPC) method (vocal tract modeling is one form) is most cost-effective. Speech sounds are converted into digital data using a special mathematical model. In an LPC voice synthesizer, a speech signal sample is calculated from a weighted sum of N previous samples, where N is the order of the predictor. For speech signals limited to a 4-kHz bandwith, 8-10 LPC coefficients are enough; higher quality speech requires 5-kHz (which requires 12 LPCs).

To recreate speech, proper codes are retrieved from the memory and passed through a circuit that simulates the functions of the vocal tract. It follows that the same word can take on different qualities by altering the vocal tract model.

Vocal tract simulation offers much better quality sound, without using high data rates. A comprehensive analysis of the speech to be recorded is necessary to produce the codes to be stored.

Architecture

The synthesizer is completely digital with 8 kHz sampling rate and 16-bit accuracy; most parameters will therefore be 16 bits long. If these values were used as the codes to be stored, some 5 to 10 Kbps would be needed. Fortunately, the parameters can be considerably quantized before the speech output is noticeably affected. Because the human vocal tract changes its characteristics rather slowly, we can afford to refresh the parameters, say,

every 25 ms, if a linear interpolation of the parameters is performed between successive values. This implies that the parameters are stored in a coded, compressed format and that a translation table is needed for every parameter. Although the voice synthesizer will typically be used as a peripheral in a μP system, it is advisable to free this processor from the burden of parameter decoding.

It follows that translation tables have to be built on to the chip, including the interpolation logic. Minimization of the tables is important; therefore, the resonators which are implemented as second-order filters, are made with three multipliers instead of the usual two. **(Figure 2).**

Acceptable Performance

Acceptable performance is obtained when 5 bits are used for the codes of the two lower formant frequencies, 3 bits for the third formant and none for the fourth. All bandwidth codes are 2 bits each. The two amplitude codes can be combined to a single one of 4 bits, together with some way of voiced-unvoiced decision.

Internally, two distinct amplitude values are maintained. In case of a change-over from a voiced to an unvoiced speech frame, the voiced amplitude parameter is gradually diminished to zero by the interpolation algorithm and, at the same time, the unvoiced amplitude parameter is gradually increased from zero to its defined value.

Although we mentioned a code frame duration of 25 ms, we can often tolerate a longer frame duration (e.g. when long vowels have to be reproduced), whereas other speech fragments require a faster frame refreshment (e.g. in the case of plosives). Therefore, a dynamic frame rate is desirable. Using values of 8, 16, 32 and 64 ms, 2 bits in every frame are needed to define its duration.

So far we have defined 27 bits in a frame, only the pitch parameter remains to be defined. One frame of codes should be a multiple of 8 bits in view of the byte-oriented processor environment, in which the voice synthesizer will normally be used. The 5 bits are not sufficient to define the pitch parameter directly. Fortunately, in actual speech, the pitch shows moderate variations in time. Hence, we apply the difference in pitch over one frame, instead of the pitch itself; at the beginning of speech reproduction, the synthesizer has to be loaded with the starting value. One frame is now defined as a sequence of 4 bytes.

Simple melodies increase the device's value—pleasing effects can be obtained by exciting a resonator with a high Q.

Simple Melodies

Simple melodies or other sound effects increase the device's value. Pitch increments can be directly programmed for making melodies, but more pleasant effects are obtained by exciting a resonator with a very high Q. Such high Qs are never present in speech and therefore not foreseen in formant filters, but can be achieved by two equally tuned resonators in series.

The two lower formants are chosen to overlap each other over a frequency span of 400...1100 Hz. In this range, the formant frequencies must have an interval of $12\sqrt{2}$ in order to realize a tempered tone scale.

Clock Generation

The speech IC contains an on-chip oscillator capable of running on an external crystal of 3.5. . . 4.0 MHz (nominally 3.84 MHz). A separate input for an external clock is provided. Internally, this frequency is divided by 3 to generate the system clock of 1.28 MHz. A buffered output on this frequency is also provided, for use as a clock for other circuitry, e.g. the μP.

Output Configuration

The 8-kHz samples from the digital filter section are indirectly fed to the built-in 8-bit DAC. A linear interpolation scheme is adopted for calculating 7 intermediate samples. The effective output sample rate is thus 64 kHz, greatly reducing the complexity of off-chip analog post-filtering.

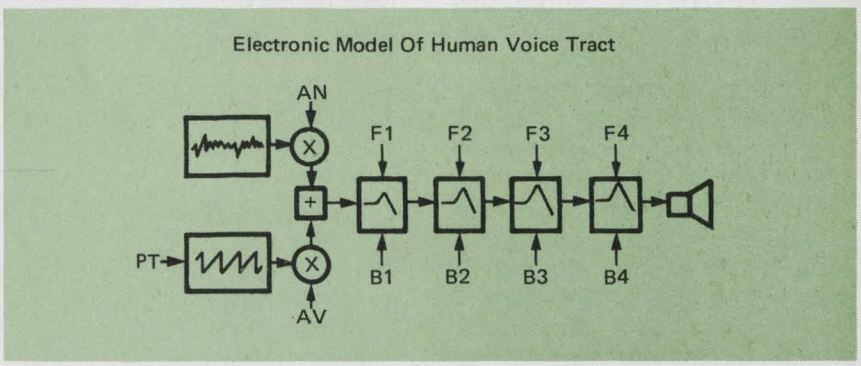
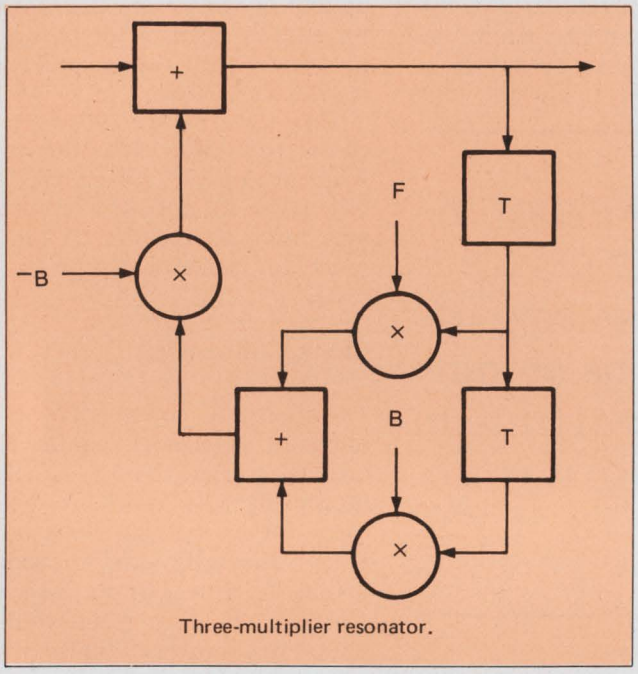
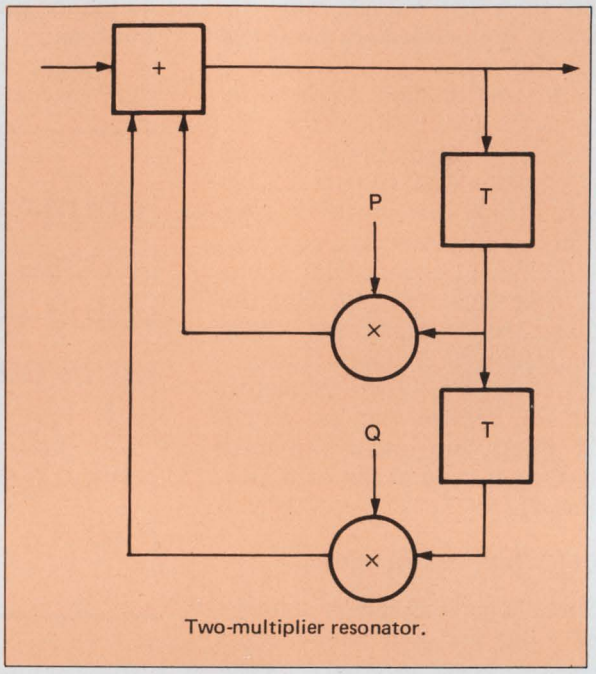


Figure 1: A mixture of a periodic signal (representing the original speech pitch) and an aperiodic signal (representing the speech noise) is fed to a series of resonators. Every resonator makes up a pronounced peak in the frequency spectrum, according to one of the formats in the original speech, and is controlled by two parameters, one for the resonance frequency (F1,F2,F3,F4) and one for the bandwidth (B1,B2,B3,B4). System output is defined by pitch frequency, amplitude values and resonator settings. Periodically updating all parameters permits a good replica.



Three-multiplier resonator.



Two-multiplier resonator.

Figure 2: In the two-multiplier resonator, the filter parameter P depends on both resonance frequency and bandwidth and would therefore need a two-dimensional parameter table. In the three-multiplier resonator, both filter parameters F and B each depend on one variable only; their corresponding tables are therefore one-dimensional.

The DAC combines two techniques to achieve 8 bits of accuracy. The output pin is connected to two parallel open drain current sources of amplitudes of I and 16I. The current I is equal to an externally injected DC current using a second pin. The least and most significant 4 bits are used to control the pulse width of both current sources independently. To prevent limited rise and fall times affecting the average output level, both current sources are turned off for at least two and on for at least three periods within one 64-kHz sample.

In the System Configuration, the synthesizer chip is designed as a peripheral chip in μP controlled systems. The speech code data is stored separately in ROM or as part of microcomputer memory.

Interfacing With A CPU

The speech code structure has been chosen so that interfacing with any 8-bit CPU is easy and flexible. In principle, the whole IC behaves as a peripheral device. The CPU has access to speech input data buffer, containing the 32 bits of code for the next speech frame; command register, containing mode select bits and a software stop/reset; and status bit.

For the accompanying R/W control signals, 3 pins are available: $\overline{CE}$, $\overline{R}$/W and $\overline{W}$. This provides the option of using processors offering either separate read and write strobe signals, or with a R/W select but combined strobe. The request for the next byte of speech code appears both in the status register and on one of the pins if required.

Controller Function

The controller has three main tasks. First, it must determine which stored element of speech is to be spoken and where it is located in ROM. Second, read the data from ROM, and third, supply the data to the synthesizer chip in the required format.

The 4 bytes of data for the next frame need not be supplied immediately by the processor; the input buffer provides a margin of one frame duration. Therefore, the circuit designer is free to connect the request pin to the processor interrupt or to let the processor frequently poll this pin or the internal status.

Implementation

The MEA8000 synthesizer chip is designed in two-phase dynamic MOS logic with a 4.8-μ technology, resulting in a chip area of 30 mm^2, mounted in a 24-pin DIP.

Designing the MEA8000 as a true peripheral device without on-chip speech ROM virtually eliminates using an environment without μP or CPU. A minimum solution for a vocabulary of 15 sec. (about 25 words) uses a μC with 2 Kbytes of on-chip ROM, most of which is dedicated to the storage of speech code.

The optimal application area is in systems which already contain a μP for other purposes. The extra cost of adding speech amounts to the cost of the MEA8000 and typically 1000 bits of memory for every second of stored speech. □

Invitation to attend the fourth annual...

MMT '82
Microelectronics Measurement & Test Conference

March 22-25, 1982 Hyatt San Jose, San Jose, California

The fourth annual Microelectronics Measurement and Test Conference now offers a specialized technical program and exhibition

Microelectronics industry leaders focus on the technology and management involved in the application and use of inspection, measuring instruments, monitoring and test equipment for microelectronics manufacturing.

Participants in this annual event include engineers, managers, supervisors, corporate executives and procurement specialists in design, test, production, computer software, QC, QA, R&D, manufacturing and processing, in companies producing and using semiconductors/hybrid microcircuits including wafers, devices, photomasks, thin films, thick films, etc. By bringing the buyers who make critical equipment decisions directly to you, MMT '82 will provide your company quality sales leads at the lowest cost.

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March 23-24, 1982

The two day equipment exhibit offers a prime opportunity to: • display test equipment, measuring and monitoring instruments to the industry • meet one on one with equipment users and buyers • demonstrate the capabilities of your product to a targeted audience • participate in the only exhibit exclusively for microelectronics measurement, inspection, monitoring and test equipment — and in the heart of Silicon Valley.

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March 22-24, 1982

For the fourth year, intermediate and advanced level professionals have the unique opportunity to examine specific measurement and test topics:

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Short Courses

March 22-25, 1982

In addition, five intensive two-day quality assurance and ATE courses will be held. Successfully produced in Boston, Los Angeles and Chicago, these courses attract key measurement and test professionals. They provide in-depth studies at introductory, intermediate and advanced levels in the selection, implementation and management of test, measurement and monitoring equipment — hardware and software.

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DD2/82

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Capturing Waveforms In μP-Based Systems

If you have ever been involved in design or troubleshooting of a μP-based system, you have probably run across difficult-to-see transients which you wanted to record and analyze. Perhaps you needed to measure a noise margin on a critical signal, or capture a transient which seemed to be occurring intermittently at some point in the μP program.

You might have tried to look at the signal of interest on an oscilloscope. If the signal repeated fairly often, this technique might have enabled you to get some idea of its amplitude and duration.

If the signal did not repeat often enough to see on the oscilloscope, you might have tried to make it repeat more often, by shortening the μP program to a minimum loop. This technique is difficult to use because running a short program often removes the source of noise on the transient.

You might also have tried recording the signal using a storage oscilloscope. However, even if you were able to capture the critical portion of the signal this way, a lack of resolution still made estimates of voltage levels inaccurate at best. Also, although this technique would help you to see the signal temporarily, the displayed recording fades away quickly.

An answer to this problem—one which allows you to record the waveform you are interested in, beginning either before, at, or after a selected trigger point—is the waveform recorder or transient digitizer. This instrument samples, digitizes, and stores representations of single-shot or repetitive waveforms. Hewlett-Packard's newly-introduced 5180A waveform recorder, provides 10-bit resolution (60 dB dynamic range) and a 20 MHz sampling rate, which means that a wide variety of waveforms with frequency components up to 10 MHz may be accurately digitized.

HP's waveform recorder is well-suited to recording single shot or transient waveforms, since its precise digital trigger ensures reliable triggering based on waveform samples. Digital trigger level selection allows maximum user control of the trigger location. Finally, pre- and post-triggering features allow the waveform recording to begin either at the trigger point, or a selectable amount before or after, so that the critical portion of a waveform will not be missed.

Waveform recorders are capable of capturing signals occuring in your μP-based system. In addition to a waveform recorder, you will need a logic analyzer to provide a trigger when the μP reaches a user-selected instruction address. The waveform recorder, logic analyzer, and system under test should be configured as shown in **Figure 2.** The trigger point is selected by specifying a μP instruction address as a trace condition or trigger for your logic analyzer (1). Then, the logic analyzer's trigger output may be used as an external trigger signal to a waveform recorder (2), causing the waveform recorder to store the signal from the circuit you are testing (3).

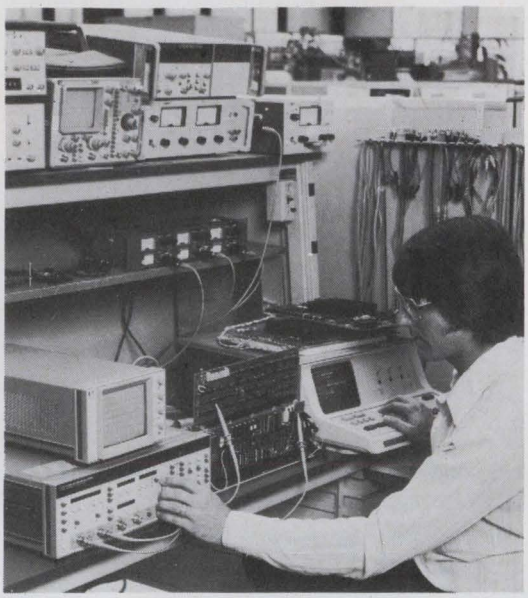


Figure 1: Waveform recorders aid in troubleshooting and designing μP-based systems, allowing the user to sample, digitize, and store representations of single-shot or repetitive waveforms.

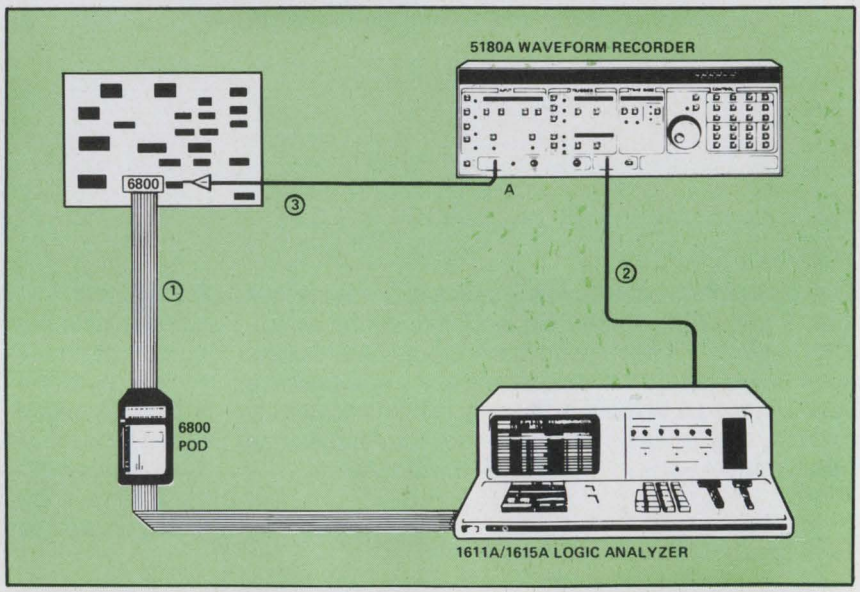


Figure 2: The above configuration of a waveform recorder and logic analyzer is necessary to capture waveforms in a μP-based system.

Innovative Design

μP-Based Systems
continued

Since many waveform recorders offer pre and post triggering features, it is possible to begin recording waveform information a selected amount of time either before or after the trigger point. The signal of interest often begins before the μP reaches the instruction address defined as the trigger point, so you may want to use pre-trigger recording to store waveform information before the waveform recorder receives a trigger signal. For example, if you suspect a transient is causing a branch to an incorrect μP instruction address, you might select this address as a trigger point, and record the transient beginning before this trigger reaches the waveform recorder. Once recorded, you can analyze the transient in detail to determine whether it could indeed be the cause of the branch.

. . . you may want to use pre-trigger recording to store waveform information before the waveform recorder receives a trigger signal.

Depending on the logic analyzer used, there will be some delay between the time the μP reaches the selected instruction address and the time the trigger signal from the logic analyzer reaches your waveform recorder. This delay should be taken into account when selecting the portion of the incoming signal to be recorded before the trigger is received by the waveform recorder.

—Eileen Bridges

Hewlett-Packard,
1820 Embarcadero Rd,
Palo Alto, CA 94303 Write 199

Modular Systems For Data Acquisition

The increasing cost of designing printed circuit boards by users with a minimal number of systems to be produced, has meant that the concept of using preassembled and existing modular products has become more popular.

The Micromodule line from Motorola was designed to meet 8-bit processing needs, particularly in the data acquisition area. It offers a variety of boards as well as processors. Earlier boards were available with the 6800 and 6802, the latest designs include the 6809.

The Micromodule 17, that features the 6809, is designed to accommodate a broad range of RAMs. If static RAM devices are installed, they can be accessed from an off-board DMA controller. The module also has the timing and control logic to provide an immediate DMA response. If a dynamic RAM module is added to the system, the Micromodule 17 has built-in control logic to provide the refresh operation.

One parallel and two serial input/output ports are provided on the board. The parallel I/O is a buffered PIA port. The pin-out of this parallel port is pin-to-pin compatible with the industry standard optically-isolated solid-state relay mounting racks (Crydom Model MS-16 or Opto 22 Model PB-16). The two serial I/O ports are ACIAs, with user option for baud rates from 75 to 9.6K and for the RS-232C terminal or MODEM interface.

An MC6840 triple programmable 16-bit counter/timer is included for counting or timing requirements.

A high-performance DEbug/Monitor/Linker firmware package, SUPERbug (Model M68MM19SB) is available for use with Micromodule 17. SUPERbug is provided as three 2K ROMs offering advanced Monitor and DEbug features, a program linkage and RAM allocation manager, and down-line or up-line loading of programs between Micromodule 17 and a host system (mainframe computer or EXORciser).

Motorola has also recently introduced Micromodule 16 which provides RAM, ROM, I/O and timer expansion for the Motorola Micromodule series of 8-bit monoboard microcomputers. The idea behind the board is to duplicate memory and I/O features found on the Micromodule 19, which is also a 6809-based single board microcomputer. By the addition of this extra board to the Micromodule 19, it is possible to almost double the amount of memory and I/O features, without resorting to several separate boards.

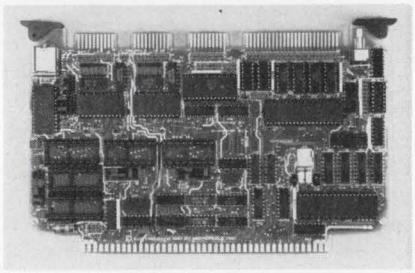


Figure 1: Micromodule 17 is an 8-bit Monoboard μC that uses a 6809 MPU, updating the existing range of 6800 and 6802 based boards.

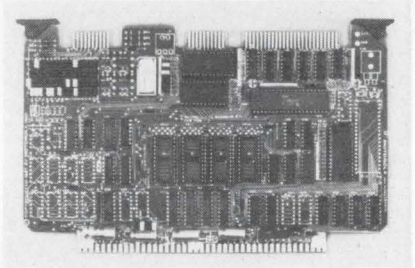


Figure 2: Bus compatible with the complete line of micromodule and EXORciser family of monoboard μC's, Micromodule 16 provides RAM, ROM, I/O and timer expansion.

Micromodule 16 incorporates 2K bytes of static RAM which can be backed up with an external battery and power-fail detect circuit, and mounts an additional four 24-pin sockets in which the user may install his choice of 1K, 2K, 4K or 8K EPROMS, MOS or Bipolar PROMs, mask ROMs or pin-compatible RAMs for up to 32K of additional memory.

Both parallel and serial I/O are provided on the board. The parallel I/O is shipped as a standard Centronics-type interface, but can be configured by the user as a buffered PIA port. The serial I/O is shipped as an MC6850 ACIA (Asynchronous Communications Interface Adapter) with user option for baud rates from 50 to 19.2K and for RS-232C, RS-422 or RS-423 interface applications. The user can replace the ACIA with an MC6852 SSDA (Synchronous Serial Data Adapter) if the system requires synchronous serial communications. An MC6840 triple, programmable, 16-bit counter/timer is included.

Other features of Micromodule 16 include 1 MHz or 2 MHz operation and on-board address, data and control bus buffers.

Micromodule 16 is bus compatible with the complete line of Micromodule and EXORciser family of Monoboard Microcomputers, Memory (ROM and RAM), I/O (Digital and Analog) and Packaging Hardware, including card cages and rack-mount chassis.

A parallel I/O adapter (M68MMI/OC1, 2, 3) is available that translates the pin-out of the parallel port connector to the pin-out requirement of the industry-standard optically isolated solid-state relay mounting rack. This allows Micromodule 16 to monitor and control high voltage, high current AC and DC signals.

Micromodule 16 is available in any of the following three versions: M68MM16-1—Micromodule 16 RAM-ROM-I/O Timer Expansion Module for use with the M6800-based Micromodule 01 series of Monoboard Microcomputers ($575); M68MM16-2—Micromodule 16 with compatible address map to the M6809-based Micromodule 19 series of Monoboard Microcomputers ($575); M68MM16-3—Micromodule 16 for use in an EXORset 30A development environment ($575).

Motorola, Austin, TX, Write 198

68000 Hooks Up To Multibus

Over the past few years, Multibus compatible single board computers have become very popular, partly due to the formidable product ranges of Intel and others.

However, some users of Multibus based systems were faced with a problem if they required an alternative processor to the 8086.

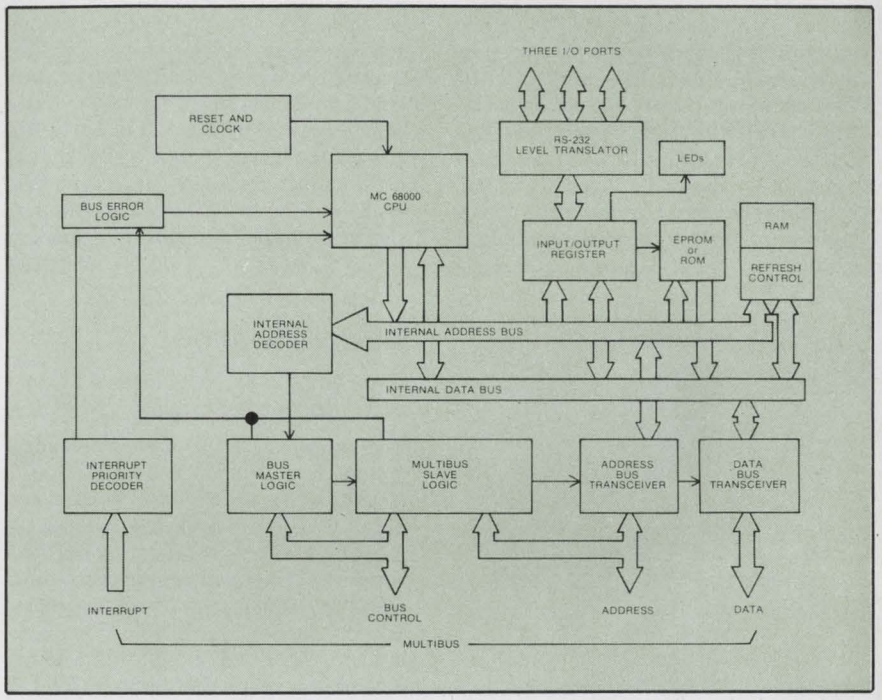
One recent entry into the SBC market has adapted the philosophy of taking the popular Multibus and adapting it to the 68000 to offer an alternative to these customers. The CMT CPU68000 board can be used in conjunction with additional I/O and memory boards to create a multiuser, multitasking system. Bus arbitration logic permits a shared bus and shared memory environment (shared with other processors, DMA devices, etc.).

The processor board features 64K bytes of read/write dynamic memory. RAMs are accessible in bytes or words. The CPU transfers data to RAM over a 16-bit wide data bus. A dynamic RAM controller simplifies RAM operation and provides refresh and arbitration functions. RAM is refreshed at 64kHz from the clock divider chain.

The board provides three firmware driven serial I/O ports to facilitate development and diagnostics. These RS232C compatible interfaces can be used for terminal, host and printer. They are presented to edge connectors opposite the Multibus edge of the board.

I/O capacity may be expanded and additional functions added using Multibus compatible extension boards. Memory may be expanded up to 1Mbyte using additional memory boards and up to 16Mbytes using the Multibus P2 connector.

Backing up the 16-bit board is the CMS 16/DS1, designed to be used in conjunction with a user terminal and DEC's PDP-11, serving as host computer to provide edit, store and file functions. The system features the CMT-CPU 68000 μP board with 64K bytes of dual port RAM and 8K bytes of EPROM including MDEBUG monitor/debugger firmware.



Multibus-compatible systems can now take advantage of the power of the 68000. The above shows a block diagram of the CMT 68000 board from CM Technologies.

Look for further information on Multibus compatible products in the May issue of Digital Design.

An MC68000 cross macro-assembler implemented in PDP-11 Fortran IV allows efficient translation of 68000 source programs into object code. It is provided in RT-11 format on an 8" floppy diskette. The CMS 16/DS1 also includes CMT's synchronous/asynchronous serial I/O board with two connecting EIA RS232 cables.

The development system can function in three modes in relation to the user terminal and the PDP-11 host computer. The DS1 is connected in-line between the two and can operate in a transparent mode, a debug/operate mode, or a download mode.

In the first mode, the user terminal communicates with the PDP-11 directly. The CMS 16/DS1 remains in a "transparent" state, monitoring the transactions, ready to intercept relevant signals that will switch it into another mode. In the debug/operate mode, the user terminal communicates directly with the DS1 68000 machine. In this mode, on-line debugging of 68000 code is possible. In the direct to host mode, the CMS 16/DS1 communicates with the PDP-11 and allows down-loading of programs from the PDP-11 to the 68000. All necessary firmware and hardware is provided to connect the CMS 16/DS1 in line to the asynchronous serial I/O ports of the terminal and host computer.

CM Technologies, 525 University Ave., Palo Alto, CA. **Write 200**

BUSINESS MICROCOMPUTER

Desktop Size And Low Cost

The 9000 has a 16-bit μP to allow execution of complex programs. The basic system comes standard with 128 kB, internally expandable to 256 kB or 512 kB. Disk capacity is 1.2MB. Human engineering features include typewriter-size detachable keyboard including a user defined function key to simplify program operation and a standard numeric 10-key pad for data entry. The system includes a tilt and swivel CRT to accommodate a

variety of viewing positions. The display component is detachable for individual positioning. The display features a dual format. In the normal mode it approximates the type written page of 80 characters by 25 lines. In expanded format, under program control, the character generator displays 132 characters by 50 lines. The screen also simultaneously displays high resolution graphics, bar and pie charts, diagrams and schematics. Array of software applications designed to meet specific business needs are available. The Victor 9000 is $4995. **Victor Business Products,** 3900 N. Rockwell St, Chicago, IL 60618.

Write 187

CAD/CAM COMPUTERS

Plus 36 New Products to Advance CAD/CAM

The APU 32-bit computer provides increased computing power to designers and engineers needing capabilities for complex engineering analysis programs such as kinematics, finite element analysis and advanced circuit analysis. It can be added to existing Designer V systems through a field upgrade. CGP-200X, a more powerful extension of the CGP-200 CAD/CAM Computer, provides improved performance and functionality without obsoleting investments of Computervision's customers in their existing hardware, software and databases. Among the other new products are Solidesign, a solid modeling software package that allows users to quickly and interactively define complex 3D parts and structures from solid geometric building blocks as well as lines and surfaces. DCU (Display Control Unit), an enhancement for Computervision's monochromatic and color Instaview raster scan graphic workstations, provides high-resolution graphics and an available color spectrum of 250,000 hues. **Computervision Corp,** 210 Burlington Rd, Bedford, MA 01730. **Write 196**

MC68000-BASED μ C

Expands To A Complete Medium-Sized Business System

The Fortune 32:16 features an operating system derived from Bell Labs' UNIX system and has a full range of business application software packages. For ease of use, a comprehensive set of user-oriented support aids encompassing everything from the initial system set-up to application conversion is available. The basic model includes a 32-bit μP with a 16-bit data path, expandable memory (128 kB -1MB) 5-¼ ″ floppy disk drive; keyboard; and a 12″ video display. A Winchester disk drive, with optional 5, 10 or 20MB of storage, is available. Its single-user configuration is designed to be readily expandable in an inexpensive fashion to a

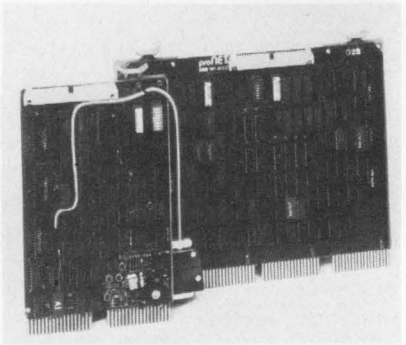
multi-user, multi-application system. The Fortune 32:16 basic configuration is $4995. **Fortune Systems Corp,** 1501 Industrial Rd, San Carlos, CA 94070.

Write 181

LOCAL AREA NETWORK

For Unibus And Q-Bus Applications

The 10MB/sec local area networking system, PRONET, consists of two boards. The Controller (CTL) hardware implements a token-arbitrated ring network. The communications medium is typically twisted-pair for short runs and fiber optics or broadband links for longer hauls. Interface to the host is implemented by the Host Specific Board (HSB) which includes full duplex DMA circuitry for fast data transfer to and from the host. The HSB also implements most of the communication algorithm in hardware so software drivers are relatively simple and easy to integrate into existing software. Drivers have been integrated into UNIX, RT-11, VMS, etc. PRONET intercon-



nects rings with DC, fiber optics or microwave links. Each ring can support up to 255 users. Both Unibus and Q-bus compatible models are available; a Multibus model will be available shortly. Cost per node (no transceiver, no master control required) is $2875. **Proteon Assoc. Inc,** 24 Crescent St, Waltham, MA 02154.

Write 192

SOFTWARE PACKAGE

Increases Productivity For Intel's Intellec Micro Development System

With MAPSOFT, programmers need only create modifications to source files and MAPSOFT will automate the production of all the object and binary files which should be produced as a result. It also tests for errors and does not produce any products for which a component was in error. A resume of the results of each step is produced in concise tabular format. In addition, each modified file is given an identification number. A tree structure of the files, giving names and numbers of all the components of a file, is displayed so the user can verify that he is using the right memory map and listings for debugging. **Morvan Software Corp,** 2 Hemlock Lane, Glen Cove, NY 11542. **Write 202**

REPORT WRITER

For UNIX Relational Database Management System

ACE allows users of the MARATHON Relational Database Management System to produce report programs with less effort than a conventional programming language. MARATHON includes an in-

teractive query language, interactive data entry and maintenance program and easy-to-use utility programs for the creation and optimization of relational databases. Formatting features of ACE include hierarchical sorting, sort break control, automatic page header and trailer printing as well as adjustable page lengths and margins. ACE also provides for complete arithmetic expressions which can involve automatically calculated aggregate values. The printing of the numeric values can be controlled using powerful formatting strings. Special PRINT statements aid the production of mailing lists and address-based reports. ACE is $2000 to users of MARATHON on 16-bit μC's. MARATHON is $4000. **Relational Database Systems Inc,** 1208 Apollo Way, Suite 503, Sunnyvale, CA 94086.

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ELECTRONIC MAIL

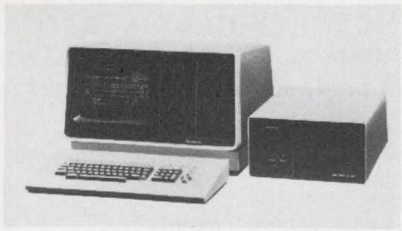
Software For DEC RSTS Users

INTECOM exchanges messages among designated users of any RSTS system and notes each transaction in the user's IN, OUT and HOLD baskets. It supports multiple user domains, group sending, message forwarding and replying, dated message sending, selective message archiving, hardcopy queueing, message keyword labeling, message query and personal calendar scheduling, on-line HELP, and more. It includes its own virtual text editor or may be used with existing RSTS editors, and supports a variety of terminal types including the DEC VT-series (with automatic keyboard message-waiting light). INTECOM requires no special resident libraries or run time systems. Single CPU license is $2880. **North County Computer Services Inc,** 2235 Meyers Ave, Escondido, CA 92025. **Write 190**

DESKTOP COMPUTER

With Optional Fixed Disk Drive Unit

The JD-850M features increased data storage capacity of more than 8.4 bytes with the optional 8″ fixed disk drive unit, Model JK-7600. The computer covers a wide range of business applications by making it possible to use with a large variety of software currently available on the market. The computer can serve on its own or as an on-line terminal for other computers. It features a separate keyboard with an improved key arrangement, a 12″ non-glare CRT display; two 8″ double-sided floppy disk drives; an optional parallel interface; GPIB (IEEE-488), increasing the unit's flexibility to



connect with a variety of measuring and control equipment; and a magnetic tape for memory backup (optional). The JD-850M can also be programmed with a Basic interpreter, a Basic compiler or in 8085 Assembler. $8000. The JK-7600 fixed disk drive is $3500. **Panasonic Co,** One Panasonic Way, Secaucus, NJ 07094

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Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

This index is provided as an additional service. The publisher assumes no responsibility for errors or omissions.

WP AND DP SYSTEMS

Provide Long-Term Upgrade Path

This family of business systems is designed to simplify a reseller's initial product commitment, to provide a logical, long-term upgrade path to more powerful and fully compatible systems which perform more business functions at better price/performance levels. The basic Xerox 820 hardware, upon which the new Parrot systems are based, includes a 24-line by 80-character B&W display screen, an adjustable alphanumeric keyboard and 5-¼" or 8" floppy disk drive. To this, Shasta adds successively more sophisticated WP software, business-level DP software and high-end configurations of hardware which include both word and data processing capabilities. The company also offers increasingly sophisticated peripherals including a high-capacity 1.4MB 5-¼" floppy drive, a 5.7MB Winchester hard disk, and a choice of two high-speed printers. Extensive resale and Independent Sales Organization packages are available. **Shasta General Systems,** 1329 Moffett Park Dr, Sunnyvale, CA 94086. **Write 185**

INFORMATION PROCESSORS

Modular Secretarial Workstations

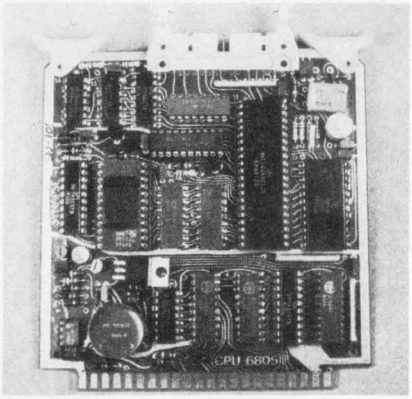
The 2 new models serve as the springboard to a new system concept based on interconnected intelligent workstations tailored to both WP and DP requiremants. Friendly operator instructions (user interface) and simple keyboard design provide ease of use. The interface is based on the soft key concept in which the meaning of the keys changes with the context; simple prompts on the display explain the changes, leading the operator to the right choice. As a result, almost any function can be accomplished in one or two keystrokes. Both the 510 and 520 are offered in standard configurations of a

CPU, CRT display, keyboard, printer and disk drive. To simplify WP tasks the units include column manipulation, forms mode, document assembly, help and explain functions, and footnote handling. In addition, the 520 has a 50,000-word expandable dictionary that highlights errors and corrects spelling. It also includes math and records processing. In standard configuration the 510 is $9250, $25/month for software, $580 monthly rental. **Exxon Office Systems Co,** 777 Long Ridge Rd, Stamford, CT 06923. **Write 201**

SINGLE BOARD COMPUTER

For The Ultra Low Power Market

The CPU-6805 is a CMOS single board computer based on a 146805E2 CMOS CPU, and designed specifically for battery-based operation. It comes with 1K of RAM, 8 lines of digital I/O, 8 analog inputs, a power switched EPROM, a real time clock, and a switching voltage



regulator, yet measures only 4.5″ x 5.25″. The board has full C-44 bus compatibility using high speed CMOS buffer chips to access up to 128 off-board ports, and 32K of off-board memory. The CPU-6805 is $395. **Synapse Corp,** 199 Main St, N. Falmouth, MA 02556. **Write 194**

NEW EDITION OF PILOT

Advanced Disk Version For CP/M-Based Systems

This new implementation of John Starkweather's PILOT is a string-oriented language designed for interactive applications such as data entry, programmed instruction and testing. It helps a person with no previous computer experience to develop dialog programs. As a companion language for Basic, Cobol and Pascal, it solves training and documentation problems. Nevada PILOT meets all the PILOT-73 standards with many new features including integrated full screen text editor and the ability to drive optional equipment such as video tape recorders and voice response units. Nevada PILOT is $149.95 including diskette and manual. **Ellis Computing,** 600 41st Ave, San Francisco, CA 94121. **Write 188**

ADVANCED μ P PASCAL

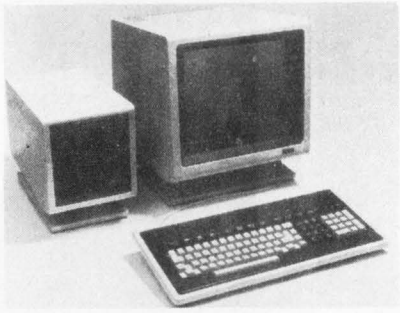
Eases Software Development For Large Memory Space Applications

Providing full memory mapping capabilities, the MPP 4.0, or Advanced Microprocessor Pascal, includes a comprehensive toolset oriented towards the large programming projects often required for 16-bit μP applications. It is the latest release of TI μP Pascal, a μP-oriented version of Pascal developed by TI to support the TMS9900/99000 family. It combines the advantages of Pascal with features that address a critical problem—that of maintaining uniformity in complex software-development programs which involve large memory spaces, multiprocessing and concurrency. Currently available software-development systems for 16-bit μP's do not provide automated support for locating collections of small program modules in a large memory-address space. Advanced μP Pascal automates this time-consuming and error-prone task via a memory manager, the BINDER, which assigns program modules to physical addresses and resolves all extended-addressing requests. $3200 for floppy diskette; $3500 for DS31, DS10 hard disk; $3900 for T25, T50 hard disk. **Texas Instruments Inc,** PO Box 202129, Dallas, TX 75220. **Write 203**

DISPLAY COMPUTERS

Support DP, WP and Comm.

The 1500 series consists of the 1505 display Computer for standalone business applications and the 1507 display computer for sophisticated applications including



standalone or clustered operation with a variety of storage options: diskette, 5-¼″ and 8″ Winchester or cartridge disk systems. OPL software language, CPM operating system and RETRIEVE, a data base inquiry system for μP computer users, are also available. **Ontel Corp,** 250 Crossways Park Dr, Woodbury, NY 11797. **Write 182**

SOFTWARE PACKAGE

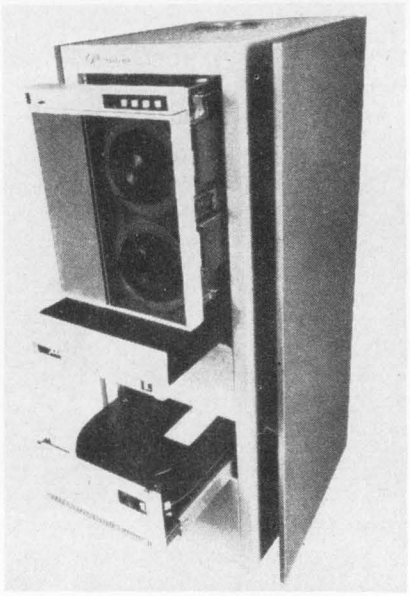
Provides 3270 Emulation

CLEO will be provided to Zenith Data Systems for world-wide distribution with the Zenith microcomputer product line. The CLEO software package enables the Zenith microcomputer to emulate a 3276 Model 2 with attached CRT and printer. **Phone 1 Inc,** 1011 River Lane, Loves Park, IL 61111. **Write 191**

DEC-COMPATIBLE SYSTEM

Low Cost, 11/23-Based System

Fully compatible with all DEC peripherals and software, the Z-11/23-75 includes a 165MB Winchester disk drive and a 75 ips vacuum column tape drive, all integrated into one 69″ cabinet. In addition to the DEC 11/23 CPU, it includes a 256 kB memory, a KEF-11AA floating point chip, a DLV-11J 4-port serial interface, and a VT-100 video terminal. The system supports either the RSX-11, UNIX or RT-11/TSX operating systems. The chassis



holds 8 extra dual slots, making it easy to add peripherals and interfaces. Custom configurations are available. The Z-11/23-75 is $45,100. **ZZY Systems,** 1900 Lafayette St, Santa Clara, CA 95050. **Write 195**

CROSS SOFTWARE TOOLS

For The Motorola 68000 μP

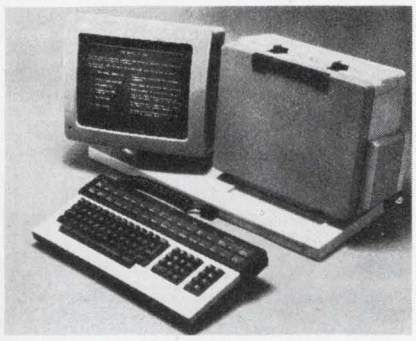
The programs are written in Fortran IV and run on most general purpose digital computers with a word length of at least 16 bits. The Assembler features conditional assembly, program-assisted base register usage, 16 user-named relocatable program sections, and the ability to produce a symbol or cross-reference table. It automatically selects an addressing mode from the many possible modes or the user may specify a particular mode. The Loader combines several independently assembled relocatable object modules into a single absolute program. Large pro-

grams can be subdivided into smaller units to facilitate reduction in assembly. The Librarian creates and maintains program libraries from frequently used relocatable object modules. It reads these program libraries and selects only those modules necessary to resolve all otherwise undefined external references. The Assembler package (ASM68K) including the Loader and Librarian is $1750. **Microtec,** Box 60337, Sunnyvale, CA 94088. **Write 189**

COMPUTER-BASED SYSTEMS

Human Engineered Information Systems

These information systems feature interchangeable Touchpanel command strips which eliminate the memorizing of keystroke codes; a technique for automatically custom-tailoring programs; and on-screen "Program Assisted Learning" (PAL) offering a self-training capability which is interactive with application software. The two families consist of the Information Station series 2000, 4 models of information workstations with storage capabilities to 20.5MB, and 4



models of the Information Station series 1000, compact desktop systems designed for more limited requirements. An operator HELP function on the Touchpanel causes an explanation of application functions to appear on the screen. Another command, UNDO, enables the operator to cancel the latest input, and retrieve earlier versions of work in progress. DP software packages will feature a method for tailoring programs specifically to individual customer applications. The series start at under $7800. **Savin Corp,** Valhalla, NY 10595.

Write 186

DEVICE-INDEPENDENT GRAPHICS

For VAX-11 Computer Systems

QPLOT is written in Fortran and can plot on virtually any graphics device that can draw a vector. Its device-independence permits the use of low cost graphics terminals for program development and output preview with subsequent final product plotting directed to higher resolution devices. Two basic modes of operation include output directly to a selected device during program execution, and an intermediate plot file (IPF) during program execution. The IPF then may be directed via the post-processor to selected devices without re-execution of the application program. Both modes may be used independently or together. Operating mode and output device selection is controlled by a single parameter. The QPLOT library includes routines for 2D rectangular and polar plotting, 3D rectangular plotting with hidden line removal, flow charting, mapping and typesetting. $3000 for a single CPU license. **QTECH Assoc,** Box 952, Old Lyme, CT 06371. **Write 184**

FILING SYSTEM

Simple To Learn, Easy To Operate

FILE-FAX Data Base Management System, offers quick access to files and records, retrieving information at high speeds, and includes a unique and easy-to-use report generator. It is written in machine language. Once the program is loaded, the operator never has to swap disks. It is user-friendly, with numerous text-editing features, and help screens that permit a review of any command function at any time. The data base itself, designed with a

full screen editor, has no set format, the operator sets it up exactly as he wants it to appear. While only a single disk drive is required, it can grow with a data base to accommodate up to 8 disk drives. FILE-FAX runs on Apple II or Apple II plus computers, with versions available for NEC PC 8001, Atari and Commodore. Versions will soon be available for the IBM Personal Computer and the Osborne 1. **TMQ Software Inc,** 390 N. East River Rd., Des Plaines, IL 60016. **Write 223**

COMPUTER SYSTEM

Fail-Safe Hardware Architecture

The Failsafe system features an innovative software development system that: automates the logical process of structured programming for developing applications software; reduces the cost of maintaining applications software; and reduces the possibility of downtime caused by software failures. Its hardware architecture provides redundancy to virtually eliminate downtime caused by hardware failures, prevents loss of the data base, and eliminates long response time for on-line applications. It eliminates common sources of programming errors by automating major portions of the development process and thereby prevents the writing of programs that could cause system failures. The rigorous enforcement of programming

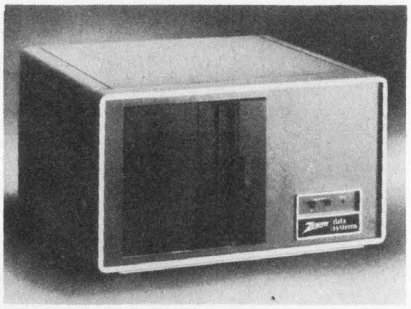
discipline results in programs that are simple and hierarchical in design and easy to debug and update. Designed for on-line use, powerful individual computers are provided at each of the 32 workstations the system can support. A basic system configuration including two 80MB disks, two 16MB disk cartridges, two data base manager computers, two data base controller computers, two 200 cps printers, one workstation, one supervisor station, dual power supplies, and software is $79,400. **DOSC Inc.,** 175 I.U. Willets Rd., Albertson, NY 11507. **Write 220**

PERIPHERALS

WINCHESTER DISK

Triples Storage For Zenith Computers

The non-removable Winchester in the Z-67 increases the storage capacity of Zenith microcomputers to almost 10MB, with the 8″ floppy diskette backup providing an additional 1MB. The Winchester also reduces the time needed to retrieve stored information by finding and transferring data at faster speeds than floppy disk systems. The Z-67 features front panel switches to protect data on



either the Winchester or floppy disk. The floppy disk drive is provided for backup, data interchange and portability of programs and data. It is compatible with the industry standard IBM 3740 format and will record in single or double density; either single-sided or double-sided. $5995. **Zenith Data Systems,** 1000 Milwaukee Ave, Glenview, IL 60025. **Write 157**

EXPANDED DISK LINE

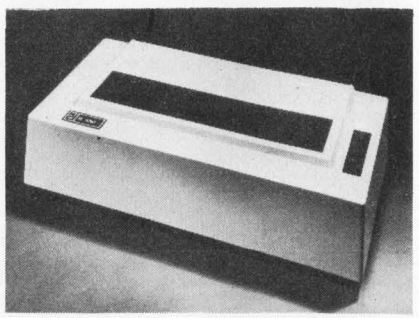
8″ Rigid Disk Technology

The device provides 13.5 MB of formatted data storage, 6.75 MB of fixed media and 6.75 MB easily stored, removable media. A covered compartment beside the disk drive holds 3 spare cartidges. Features include front loading media, high throughput, μP-based logic and high reliability. The new controller, Model 4180, mounts in any CLASSIC CPU, and can control up to two drives. The drives may be the new Model 4181 8″ drives or the existing 26, 67 or 256 MB single port drives in any combination. The 13.5 MB disk with the new controller is $11,775; additional drives are $6475. **Modular Computer Systems Inc,** (MODCOMP), 1650 W. McNab Rd, Ft. Lauderdale, FL 33310. **Write 153**

DOT MATRIX PRINTERS

Modular Design For Easy Service

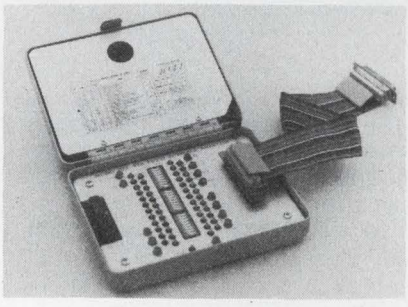
Performance characteristics of the printers include: 80 or 132 columns; 150 cps; bidirectional, logic seeking; 9 x 9 matrix; 6 or 8 lpi; 10, 12 or 16.5 cpi; 96 ASCII printable characters; Centronics compatible, Serial RS-232C or current loop interfaces; 350 character standard buffer expandable to 3,422 characters; cartridge ribbon; expanded, condensed and double density characters; standard, alternate and downloadable character sets; 600 million character life printhead; tractor and optional friction feed; multiple copies (6 part maximum); quiet operation (60 dba); and graphics. Fully-featured Series 900, 80 and 132 col models are $995 and $1195. **Hi-G Co, Inc,** Printer Products, 580 Spring St, Windsor Locks, CT 06096. **Write 152**



INTERFACE ANALYZER

EIA RS-232 Analyzer

Model 700 is a diagnostic tool for use at the EIA RS-232 or CCITT V.24 data interface of modems, multiplexers, terminals and computers. It is inserted in series between the Data Terminal Equipment (DTE) and the Data Communications Equipment (DCE) to provide access to and monitoring of all data, timing and control signals. Model



700 utilizes state-of-the-art tri-state LED's to clearly display polarity, activity and validity of all key interface signals, simultaneously, in red, green, and red-green mixtures. Out-of-spec signals and open circuits are spotted instantly. The unit is compact and battery powered for portability. $275; qty discounts avail. **Electro Standards Laboratory Inc,** Box 9144, Providence, RI 02940. **Write 151**

MILITARIZED MONITOR

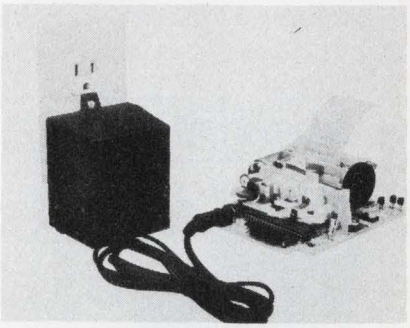
High Resolution Color Raster Scan Display

The IP-1394/G, developed under a Military Adaption of Commercial Items (MACI) contract, has the unique feature of special anti-magnetic circuitry. The militarized tube has been tested to 30 g shock, 5 g's RMS vibration and to temperature extremes of −40°C to +50°C. The militarized monitor utilizes a 19″ high resolution shadow mask CRT and incorporates a special capability enabling normal operation in up to a 5 gauss magnetic field environment, which would destroy the color integrity of standard color monitors. It provides high quality graphics/alphanumerics while operating in a rugged, hostile military environment. **Hazeltine Corp,** Commack, NY 11725. **Write 147**

12 COLUMN PRINTER

Easily Adds Fast Printing To Equipment

Powered by only 6V, 800 mA (nominal when printing), data can be parallel, BCD or RS-232 serial (110-9600 bps) input



form. Printing is electrosensitive dot matrix, in a 64 character set at 5 lps from a 3-5/8″W x 4-5/8″H x 4-1/″D unit (power supply is separate). Tear bar, paper advance, a one line buffer, expanded print, and self-test are standard. The SS-12 Printer Subsystem with power supply is $150 (100 qty). **Hycom Inc,** 16841 Amstrong Ave, Irvine, CA 92714. **Write 155**

LINE PRINTER

Interfaces With Virtually Any Minicomputer

The T-340 enables minicomputer users to increase their print speed from 300 to 340 lpm while spending up to 30% less for each lpm of speed. It features superior print quality, a 100 million character

life cartridge ribbon, 10 cpi, and an 840 character library for application flexibility. Belt technology enables replacement of individual characters for less than $3.00 each. It also features quiet operation and low cost contract maintenance. **Digital Associates Corp,** 1039 E. Main St, Stamford, CT 06902.

Write 149

KSR PRINTER

With Printwheel Interchangeability

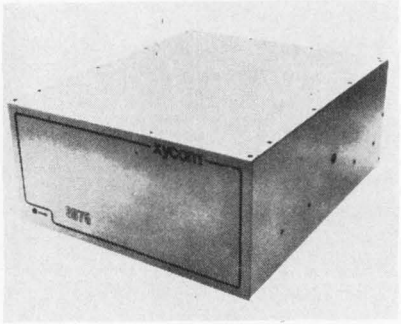
Model 630 KSR offers an RS 232C serial interface and other communications features that include a 16 byte input buffer, word processing firmware features, extensive diagnostics for host control and transmission rates ranging from 110 to 9600 baud. The 630 KSR

also offers 128 bytes of non-volatile RAM with battery backup. This feature provides up to a 31-character long "Here Is . . ." message and stores all necessary system and operating parameters such as margins, tabs and page sizes. And, via a remote reset, carriage and printwheel selection-related commands can be restored from the non-volatile RAM. This means no reinitialization is required between power-offs. A word processing firmware option is available offering right margin verification, text centering, line editing, vector plotting, and two-color ribbon utilization. $2795. Also available with keyboards for APL, French, German, Norsk or Scandinavian all include a 10-key numeric pad. **Diablo Systems Inc,** A XeroxCo, 24500 Industrial Blvd, Hayward, CA 94545. **Write 145**

WINCHESTER DRIVES

10 And 20MB Capacity

The drives are fully supported by Xycom's software development systems, Ladder Diagram Translator Systems,



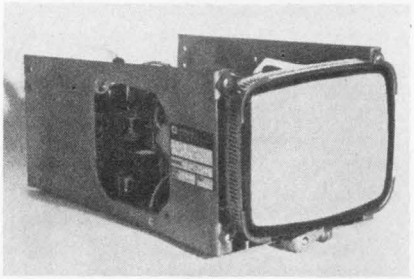
180+ "Industrial Grade" μP board family, and the original 180 line of processor and I/O modules. The RS 422A interface allows the disk package to be remotely located from 180+ systems operating in harsh environments. The SDLC communications protocol provides for an efficient method of transferring data to and from the hard disk system. The ISS and LDT drivers partition the hard disk drive into 8 unit I/O devices. Features include automatic head locking; 500K baud internal clock rates or external clock rates up to 800K baud; error recovery and logging; read buffering; Winchester style recording, and fixed media. The 10MB Model 3875 is $7950; the 20MB Model 3876 is $8850. **Xycom Inc,** 750 N. Maple Rd, Saline, MI 48176.

Write 156

5″DISPLAYS

With Chassis, In Kit Form, Or Specially Constructed

The BHD-500 Series incorporates numerous design and performance features including optimized corner focus, resolution, bandwidth and geometry. The single circuit board is compatible with industry standard data display video input connectors on a pin-for-pin basis. The series can accommodate either direct TTL level input



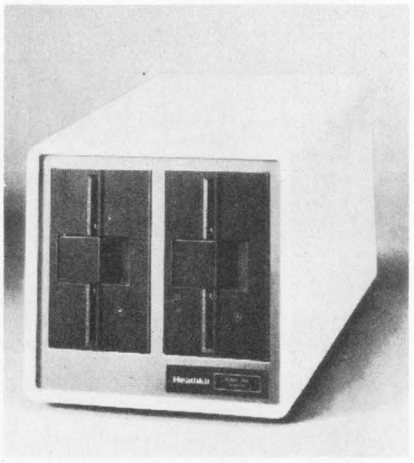
signals or — by addition of an optional circuit — composite video input signals. Other options include phosphor type (EIA P4 is standard) and a horizontal scan frequencies between 15,750 and 21,000 Hz. **Dotronix Inc,** 160 First St. SE, New Brighton, MN 55112.

Write 148

EXPANDED DISK STORAGE

Over 640,000 Characters/5.25″ Diskette

This increase in diskette storage makes it possible to put large programs on 5.25″ diskettes instead of 8″ diskettes, lowering cost and saving desk space. The H-37 dual diskette drive can store 160 tracks of information on a diskette and retrieve information 40% faster. The HS-3-2, with 2 drives, increases data storage capacity to 1.28MB (640,000 bytes/drive); $1345. The single drive HS-37-1 is $850. The

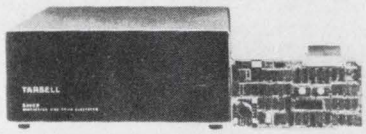


double-density disk controller card, the Z-89-37 increases the storage capacity of Heath's 5.25″ drives from 100 kB to 160 kB. It operates with either the 40-track drives provided in the H-87, or with the new 160-track drives in the H-37. $395. **Heath Co,** Dept. 350-335, Benton Harbor, MI 49022. **Write 146**

S-100 SUBSYSTEM

Expansion From 10 To Over 200MB

These Winchester hard-disk subsystems, 33MB and above, use a voice-coil actuator which provides an average access time of 50 ms. Data comes off the disk into the deblocking



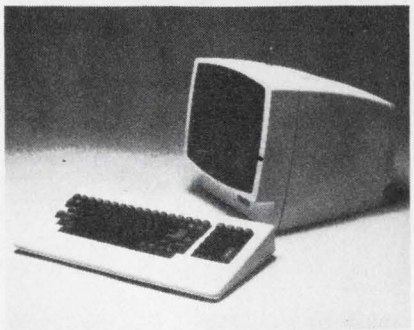
buffer at the maximum possible speed of 1MB/sec, meaning that a 24 kB file can be loaded into memory in about one second. Additional features include onboard CRC performed on data, automatic alternate sector assignment, 512-byte onboard deblock buffer and the use of only one S-100 board slot. The subsystem includes S-100 interface, drive, cabinet, power supply, cables, software and all documentation. **Tarbell Electronics,** 950 Dovlen Place, Suite B, Carson, CA 90746.

Write 229

LOW-COST CRT TERMINAL

Fully Emulates Burroughs Model TD-832

The 932 achieves plug-to-plug, code-to-code emulation of the TD-832. It incorporates a 6800 μP, with 8 kB of RAM. It includes RS-232 and sync or async TDI interfaces and features an independently addressable printer port.



No switches are required for formatting since a programmable nonvolatile memory is built into the terminal. Standard features include dual page capability and built-in concatenation. Additionally, the 932 features a durable, detachable keyboard with the same layout and functions as those of the Burroughs model, plus a built-in numeric keypad. $1895. **Emulog,** 3730 Yale Way, Fremont, CA 94538.

Write 150

80-COLUMN PUNCH

Directly Connects To DG Nova

The PC200/51 has card punching speeds of 100 to 250 cards/minute. In order to accommodate volume punching operations, the input hopper and output stacker have a capacity of 1000 cards each. Card punch verification is accomplished through echo check error detection. A 100 card capacity reject stacker is provided for automatic selection of cards that do not pass the echo check verification. An RS232C serial version of the punch will also be available. The PC200/51 is $12,500, OEM discounts avail; lease price is $357/month. **Cardamation Co.,** Box 746, Frazer, PA 19355.

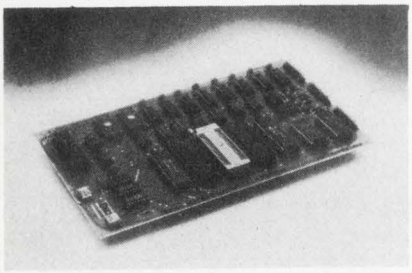
Write 226

Write 26 on Reader Inquiry Card

EPROM/PROM PROGRAMMER

Zero Hardware Redundancy

Since most companies using programmers already have hardware such as terminals and power supplies on hand, the P & E Programmer eliminates them. Terminal strips connect this compact PC board to I/O devices (RS-232), power supply and computer.

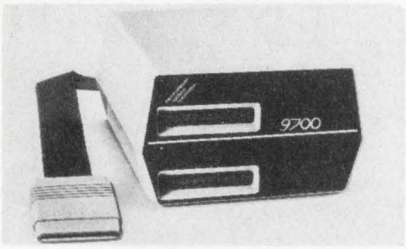


It is based on the Z80 μP with 4 kB of RAM, the firmware is two 2716 EPROMs. Two RS-232 data ports provide transfers as rapidly as 19.2 kB/sec. With only a terminal, the Programmer is fully capable of burning data into almost any EPROM/PROM. Protocols for 15 standard PROMs and EPROMs are internal. Its three operating modes are: stand alone, computer driven and the transparent mode. When used with a cross assembler resident in the host, the Programmer can become the center of a low cost mini-development system. It is actually a small general purpose computer system with 4k of EPROM, 4k of RAM, 2 serial ports and 48 parallel I/O pins. Hence it may be used for other purposes. $450, qty discounts avail. **P & E Microcomputer Systems**, Box 2044, Woburn, MA 01888. **Write 239**

HARD DISK SUBSYSTEM

For Personal/Professional Computers

Through the use of interchangeable Host Adapter Personality Cards, the MSC 9700 Winchester disk storage subsystem can be adapted in moments

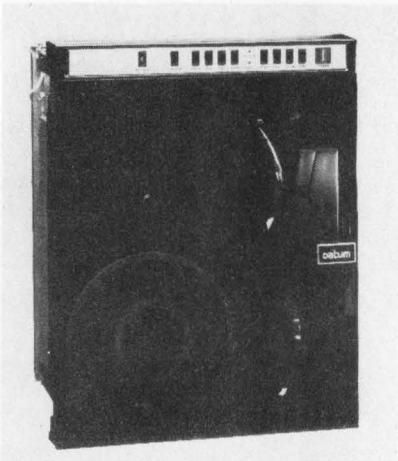


to be compatible with a variety of microcomputer systems. Host Adapters already available include Apple II, Xerox 820, IBM PC, TRS-80, Q-bus, S-100, Multibus and STD bus. When used with a specific Host Adapter, the MSC 9700 emulates the software protocol of the host. The user has the option of selecting either a one- or two-drive version of the subsystem for either a 5- or 10MB on-line storage capacity. Backup is available in two forms: a second Winchester disk drive provides one-on-one protection of data stored on the first drive, or a mini-floppy disk drive option is available. The standard subsystem includes one Seagate ST-506 5-¼" Winchester disk drive, the Xebec S1410 controller, and a reliable 115V/230V power supply. Basic MSC 9700 is under $3000; average list price of Host Adapters is under $200. **Microcomputer Systems Corp.**, 432 Lakeside Dr., Sunnyvale, CA 94086. **Write 235**

TAPE TRANSPORT

Combines Start-Stop And Streaming Capabilities

Gemini is a 45 ips drive for transaction processing that converts on software command to a 125 ips streaming mode for backup, eliminating the need for two different tape drives. The unit is faster and less expensive that the two units it replaces. In the streaming mode it constantly monitors the data rate for any mismatch with Winchester or SMD disks. If such a mismatch exists,

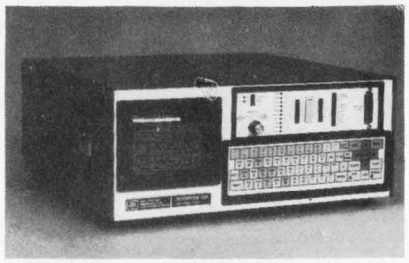


the drive automatically returns to its 45 ips transaction pace for increased efficiency. Components such as hard-faced R/W heads for longer life, high-performance servos and mechanically isolated elements provide optimum performance throughout the speed range. The embedded formatter controls the host drive and supports 3 additional, daisy-chained drives. It accommodates both NRZI (800 bpi) and PE (1600 bpi) formats in the 45 ips mode and PE (1600 bpi) for streaming, IBM/ANSI compatible for 9-track units, with density selection available from the front panel. The DMF-1000 Gemini is $4800 in qty. **Datum Inc.**, 1363 S. State College Blvd., Anaheim, CA 92806. **Write 233**

DATA ANALYZERS

Field Service, Tech Control And Starter Applications

The testers are available in three models: Interview 29A, a low cost data



analyzer with HEX keyboard; 30A with fully code converted ASCII keyboard; and the 40A fully interactive data analyzer. The friendly sophistication of the testers is operationally compatible with the more powerful, engineering oriented 3500/4500 series units, thus encouraging cooperation between engineering and field personnel to more quickly solve problems. Offering a fully code converted ASCII keyboard, each unit displays 512 characters of data and protocol sequences from an 8k buffer. It provides a directory for access to many complete diagnostic tests that identify specific data communications problems. Standard basic setups include 3270 bisync, 3276 SNA, X.25, and IPARS. The user can add up to 50 tests of his own design, the programmer is built in for permanently storing and duplicating tests for field distribution. **Atlantic Research Corp.**, 5390 Cherokee Ave., Alexandria, VA 22314. **Write 231**

MONOCHROME MONITOR

High Horizontal Resolution

Model 10VM965 features 800 lines or better horizontal resolution, DC restoration and a variety of phosphors. The monitor has all silicon solid-state circuitry for maximum performance, long life and low power drain. The single module construction is plugable to provide any possible on-the-spot maintenance. Other features include bandwidth in excess of 20 MHz, 2% or

less of geometric distortion/linearity, 75 ohm termination switch for video input, BNC connectors, AC fuse and line cord, and optional rack mount. Also available are a series of flexible CRT data displays. The 9 and 12″ models are offered as selfcontained units with a single circuit board mounted on the CRT neck, as kits for designer control of circuit board mounting, and in frame versions with variable mounting configurations. **Audiotronics,** 7428 Bellaire Ave., North Hollywood, CA 91609.

Write 224

8.4MB HARD DISK

Storage For TRS-80 Model II Computer

This new storage system eliminates the need for repetitive handling of floppy disks when using different programs, since multiple programs can reside simultaneously in the hard disk system. Up to 3 secondary hard disk drives may be added for a total storage capacity of over 33MB. The system incorporates the TRSDOS operating system, making it immediately compatible with most existing Model II software. All current TRSDOS library commands are available, plus two new utilities: the Save utility saves data from the hard disk onto one or more backup floppy disks; Restore writes data from a floppy disk onto the hard disk. It incorporates two 8″ platters, permanently sealed in a dust-free environment. Both surfaces of each platter are accessed by their own R/W heads. The hard disk system (26-4150) is $4495; secondary hard disk units (26-4151) are $3495. **Radio Shack,** Div. of Tandy Corp., 1800 One Tandy Center, Ft. Worth, TX 76102.

Write 241

MATRIX PRINTER

Records Graphics/Alphanumerics From Autograph 150

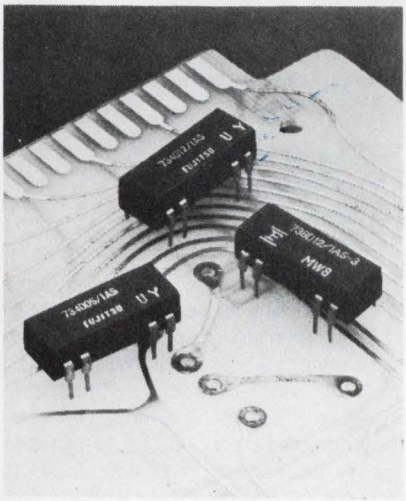
The Autograph 1000 functions as a "scratch pad" printer to record the 250 X 512 resolution pictures displayed on the Autograph 150 preview screen. Printer resolution is 72 dots/in. vertically. A full screen display is copied on continuous fan fold sheet fed paper in approximately 45 secs. The Autograph 150 display terminal emulates the Tektronix 4010 terminals and additionally offers independent memory viewing, selective erase and impact printing. The 1000 printer is also a high performance, quiet data printer. At 200 cps and a 7 X 9 dot matrix, it produces expanded and double density printing in 10, 12 and 16.5 cpi with bidirectional, logic seeking. All 96 ASCII characters and optional alternate and down loaded character sets are printed from transmissions of up to 9600 baud. $1995 for the printer, $2595 for the display, $4500 purchased together. **MQI Computer Products,** 2615 Miller Ave., Mountain View, CA 94041. **Write 237**

COMPONENTS

REED RELAYS

Microminiature DIP Series

This series of microminiature DIP reed relays are designed for use in DP and security systems, telecommunications and test measurement and control equipment. The FRL 730 series relays have 1 Form A contacts with a rating



of 10 VA. They can be mounted in the standard 14 pin DIP socket PC board on a 2.54 x 7.62 mm grid pattern. The relays are of epoxy molded construction for safe immersion cleaning. Optional electrostatic shielding and coil shunt diodes are available. From $1.56/1000. **Fujitsu America Inc.,** Component Div., 918 Sherwood Dr., Lake Bluff, IL 60044. **Write 249**

COSMAC MEMORY BOARD

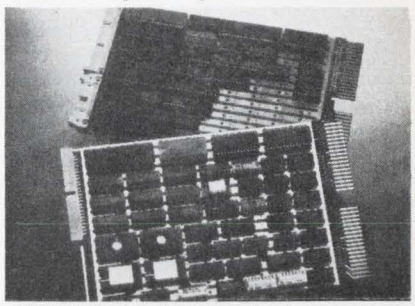
Accepts Wide Variety Of Memory Chips

This universal memory board is capable of being loaded with combinations of ROM, EPROM and RAM devices, and operates with the CDP1800 COSMAC Microboard series. The CDP18S626 supports either 32 or 64 kB of memory. It has onboard address latches and decoders, along with buffered address and data lines that minimize loading of the Microboard bus interface. Its 16 (24-pin) sockets can be populated in a variety of memory configurations. An important feature is its ability to inhibit 1, 2 or 4 kB segments of contiguous memory in selected banks. The board incorporates all the high-performance features of the COSMAC Microboard system including single-supply +5V operation, low power, high noise-immunity, a simple system interface and expandability through the Microboard Universal Backplane. **RCA Solid State Div.,** Box 3200, Somerville, NJ 08876. **Write 213**

NETWORKING DATA LINK

Increases CPU Power

This local area network data link incorporates an Intel 8086 μP to offload link and network software from the host computer to the coprocessor. Microlink features multi-layered PROM embedded software to free the host from tasks associated with generating and controlling protocol. It permits an LSI-11 or PDP-11 to communicate by means of HDLC protocol to as many as 255 other stations at distances up to 30,000′. Transmission



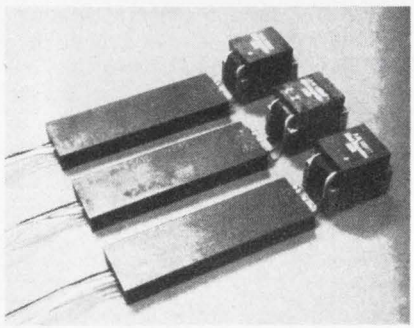
occurs at a 1-megabaud rate down a multidrop line, such as coaxial cable. Link interface, networking, transport layer, and HDLC protocol handling software programs are included. **Standard Engineering Corp.,** 44800 Industrial Dr., Fremont, CA 94538.

Write 216

MINIATURE POWER SUPPLY

For Field-Effect Transistor (FET) Amplifiers

The unit is designed to withstand shock, vibration and altitude, and can be customized to meet other environmental requirements. It operates from a prime power of 115 VAC, 57-420 Hz, single phase, and requires 20W of input power. When loaded with an impedance so that output current is between 0.25 and 0.70A, the unit will provide 4.2 to 6.5 VDC (±1% regulation) with less than 5mV of output ripple (peak-to-peak). This output is provided at both high and low line over the frequency range, and over a baseplate temperature range of −30°C to +85°C. Maximum output power is 5W. Other output-voltage and input-power ranges are available upon request. It offers small size, rugged construction and AC input power with military environmental and component specifications. **Varian Associates,** Microwave Components & Subsystems Div., 3200 Patrick Henry Dr., Santa Clara, CA 95054. **Write 217**



DATA SHARE BOARD

Expands Single User System Into Multi-User System

Compatible with S-100 bus systems, this board gives each user full processor capacity, assuring maximum efficiency by overseeing each user's operation and contact with the storage devices and other peripherals. It allows the addition of processing capacity and full memory to each satellite user rather than sharing the master processor. It also provides software for better utilization of the central processor and memory by each satellite user. The board has a 4 MHz Z80A processor, 64K RAM, 2K EPROM, 2 serial ports and 1 parallel port. The S-100 bus board can be adapted to interface with other bus systems. **Computer Manumatic,** 22077 Telegraph Rd., Southfield, MI 48034. **Write 244**

128K MEMORY BOARD

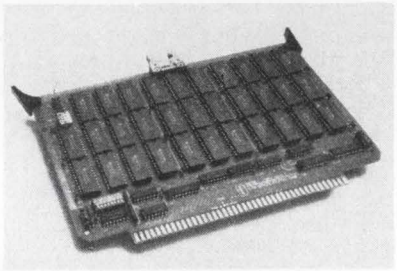
Full Compatibility With S-100μC Systems

The IEEE compatible Dynamic Memory incorporates 8 totally independent 16kB software selectable banks with each bank independently addressable on any 16K boundary. Up to 8 banks (512K) are supported per I/O port for each of the 256 ports. The 128K board also features parity for single bit error detection, 24 bit extended addressing, 10 on-board diagnostic LEDs and Z-80 4MHz operation using transparent refresh and low power requirements, 8W maximum. Start at $1595, qty prices avail. **Systems Group,** 1601 Orangewood Ave., Orange, CA 92668. **Write 215**

64K STATIC CMOS RAM

Operates With M6800/6809

The 9638 module is pin and outline compatible with the EXORciser and Micromodules. It provides 65,536 bytes when fully populated to 64 kB. Partially populated versions provide 32K, 48K and 56K bytes. The 9638 is configured as eight 8K blocks which can be independently placed in the memory map by onboard switches. The module also provides decoding for 4 additional address lines for use in memory management systems. Typical access time is under 200 ns. Power required is 150mA typical from a single 5V supply. The 64K version is $1095, qty discounts avail. **Creative Micro Systems,** 3822 Cerritos Ave., Los Alamitos, CA 90720. **Write 243**



DOT MATRIX PRINTER

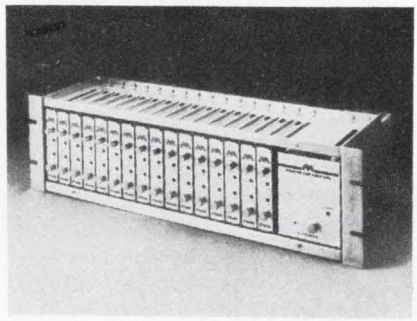
Single Heavy-Duty Print Hammer

The GP100 impact printer has a single heavy-duty print hammer (Uni-Hammer) rather than the 7 or more individual solenoids and print wires found in conventional dot matrix printers. It uses standard fanfold paper, up to 9-½" in width and allows dot graphics, alphanumeric characters and double width characters to be mixed within a single line. It uses a rotating platen with protruding lengthwise splines positioned behind the paper. A precision gear train assures the exact positioning of the print hammer relative to the splines on the platen, providing excellent print quality and uniformity of the 5 X 7 dot matrix. The GP100 is $389. **Axiom Corp.,** 1014 Griswold Ave., San Fernando, CA 91340. **Write 242**

CARD FRAME/POWER SUPPLY

Houses Up To 16 Variable Speed Z9600C Modems

The Z9600 family of async modems are designed for short haul operation of up to 10 miles at speeds up to 9600 bps. The Z-Frame provides modular designed, rack mount convenience. Edge connectors provide all power and signals to the Z9600Cs. Each modem card slot in the frame operates independently and is connected to external devices via RS-232 and line connectors attached to the motherboard. Downed lines do not affect the operation of other modems in the frame. The Z-Frame is a standard 19" frame, 5-¼" high. Power is 110V/60 Hz with 220V/50 Hz optional. $337. **Madzar Corp.,** 37490 Glenmoor Dr., Fremont, CA 94536. **Write 210**



VOLTAGE SURGE PROTECTOR

For Sensitive Electronic Equipment

Model 718 provides 7 isolated outlets to deliver pure power to protect computers and word processors. It is also recommended for sensitive digitals, medical and diagnostic electronic equipment, and offers immunity from the complex causes of unwanted signals and electrical interference. It features a 7 stage transient voltage and RFI/EMI filter network, dual protection of 50 Joules on both transverse and common modes, and 15A circuit breaker. **National Field Sales Inc.,** 2660 W. Chester Pike, Broomall, PA 19008. **Write 211**

IBM/OCR INTERFACE

Connects AlphaWord III To IBM Display Writer

AlphaWord III OCR PageReader is a high-speed data-entry system which increases word processing productivity by up to 600%. Text typed on Selectric or other single-element typewriters is outputted directly to the IBM Display Writer with automatically inserted for-

mat codes. AlphaWord III reads text at a rate of 270 pages/hour. When scanning is done in an unattended mode, unrecognized or "best guess" characters appear as question marks and/or a stop code. These characters can then be easily located by using the search feature on the Display Writer. The interface is $2000. **CompuScan Inc.**, 900 Huyler St., Teterboro, NJ 07608. **Write 204**

GRAPHICS BOARD

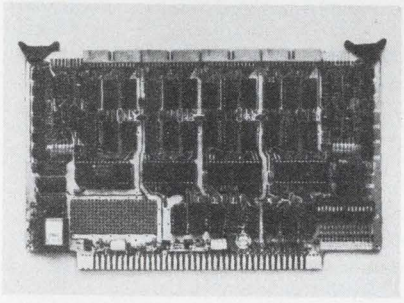
Tektronix 4014 Emulation For VT100

The SG200 consists of a single graphics board that is field installable in the terminal's existing card cage. Featuring direct Tektronix software compatibility, a VT100 terminal with the SG200 emulates a Tektronix 4014 with an addressable plot area of 4096 X 4096. Plot modes consist of normal, point plot, and incremental plot, while the vector variation modes include solid lines, dotted, dot dashed, short dash, and long dash lines. The SG200 board also features a full page break capability, enabling the operator to sequence through graphics images. It also has its own powerful native mode that is supported by friendly, inexpensive software. Patterned after its predecessor, the SG100, the native mode includes a μP-based vector generator to simplify programming. Commands to create arcs, circles, lines and boxes can be generated with a single command. Includes a printer port for RS232 communication to CPU or hardcopy up to 9600 baud. $1595. **Selanar Corp.**, 437-A Aldo Ave., Santa Clara, CA 95050. **Write 214**

ACIA/TTY MODULE

Four Ports And Programmable Control

The quad ACIA/TTY module, GMS6511, controls up to 4 channels of ACIA and TTY, with each channel operating to 3 standards (RS232, 422, 423) through replaceable chip sets, and with programmable baud rates, stop bits and interrupt control. It matches the Motorola EXORciser/Micromodule and Rockwell System 65/AIM 65 bus structures. Available in 1 MHz and



2 MHz versions, it also offers data set/modem control functions and a wire wrap section for custom clock circuitry. Each of the 4 channels of the ACIA (Async Communication Interface Adapter) module can be operated at different interface standards and baud rates, and each can also control a TTY. The GMS6511 is $343. Also available with 4 ACIA ports only, with 2 ACIA/TTY ports, or 2 ACIA ports only. **General Micro Systems Inc.**, 1320 Chaffey Ct., Ontario, CA 91762. **Write 205**

MEMORY EXPANSION BOARD

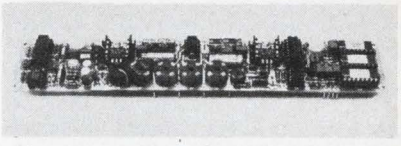
For IBM Personal Computer

The board allows IBM Personal Computer users to directly address up to 1MB of memory. It can be configured in a variety of sizes: 64kB, 128kB, 192kB and 256kB with parity. IBM Personal Computer users will now be able to configure much larger systems since fewer expansion slots will be required for memory and more slots will thus be available for peripheral devices. Starts at $499 for the 64kB version. **Datamac Computer Systems**, 680 Almanor Ave., Sunnyvale, CA 94086. **Write 247**

DC CONVERTER

20 Watt Programmable Model

The PC77020 requires a supply of +12V DC. It can be programmed for an output voltage over a range of 0 to +40.96V in steps of 10mV and for a load current over a range of 0 to 2.56A in steps of 10mA. Both voltage and current control loops are continuously



active; crossover between constant voltage and constant current control modes is automatic as determined by the more restrictive of either the voltage or current reference at any point in time. A programmed step in voltage is completed in 2ms. $394. **Interplex Inc.**, 2680 Bayshore Frontage Rd., Mountain View, CA 94043. **Write 251**

POWER SUPPLY

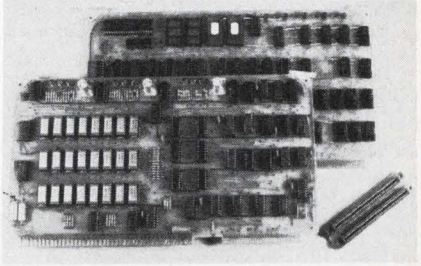
Multiple Output Switching Power Supply

This high efficiency convection cooled unit has minimum components for maximum reliability. The PEC SMPS Series with user selectable input voltage, under voltage protection and a ripple/noise factor peak to peak of 2% maximum, is designed to provide an efficiency of 80% TYP at maximum output power at nominal line voltage. **Power Electronics Corp.**, 96 Milton Rd., Rochester, NH 03867. **Write 252**

GRAPHICS GENERATOR

For RGB Color Applications

The RG-GG6C Graphics Generator is a two board set of Multibus compatible boards designed for RGB color applications. It features a smart vector generator board which generates both



text and graphics and, a refresh memory board with two sets of three 512H x 480V memory planes for dynamic display applications. $1895. **Raster Graphics**, Box 23334, Tigard, OR 97223. **Write 255**

FIBER-OPTIC MULTIPLEXER

For Local Area Terminal Communications Links

Model 39301A provides 8 EIA RS-232-C/CCITT V.24 duplex channels. The duplex fiber-optic cable, HFBR-3100, connects the multiplexing units for communications up to 1000 meters between any host processor and remote terminal clusters. The link is immune to electromagnetic interference, such as lightning strikes, noisy motors, static discharge and crosstalk. Capacity can be expanded from 8 to 16 channels with the HP 8120-3569 adapator

cables. Each of these 16 full duplex channels accommodates async data at rates up to 19.2K with a bit error rate less than 1 in 10^9 bits. Each channel may be used independently with different protocols and baud rates without any adjustments to the multiplexer. The HP 39301A fiber-optic multiplexer is $2500 each (qty 2); the HP 8120-3569 adaptor cables are $102 each (qty 24); the HFBR-3100 fiber-optic duplex cable is $4.50/meter for up to 4999 meters. **Hewlett-Packard Co.**, 1820 Embarcadero Rd., Palo Alto, CA 94303. **Write 207**

POWER MOSFETS

N- And P- Channel Units

The ZVN13 and ZVP13 feature low input capacitance (C_{iss} less than 30 pF) and fast switching speeds (t_{on} less than 5 ns, t_{off} less than 7 ns). The devices can be easily paralleled without the need for base current sharing resistors and do not exhibit thermal runaway and thermally induced secondary breakdown. Both consist of 8 devices each, with voltages ranging from 40 to 200 V and maximum drain currents up to 1.5 A. Each is available in TO-39 and TO-92 packages, as well as 14-pin DIL packages (also available in dice form). Both series are ideally suited for applications including μP and IC logic interface driving, sensing and timing circuits, and general purpose switching. ZVN1306A is $.60 in qty of 100+; ZVP1306A, $.75 100+. **Ferranti Electric Inc.**, Semiconductor Products, 87 Modular Ave., Commack, NY 11725. **Write 248**

DC-DC CONVERTERS

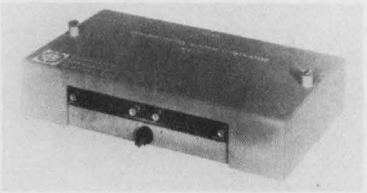
1 And 2 Watt Models

The 400 Series of miniature DC-DC Converters are designed for point of load regulation. The line consists of 28 models. Input voltages are either 5 VDC or 12 VDC with single outputs of 5 VDC, 12 VDC and 15 VDC and dual outputs of ±12 VDC and ±15 VDC. All electrical and mechanical specifications are outlined in detail in a 2 pp. data sheet. **Power General**, 152 Will Dr., Canton, MA 02021. **Write 254**

MODEM ELIMINATOR

Eliminates Need For Back-To-Back, High-Speed Modems

The ME-31 allows interconnection of data terminal equipment without the need for modems in applications such as IBM's TeleProcessing Network Simulation (TNPNS) program. It regenerates data and clock interface signals so that a full 50′ interface cable may be used at each RS-232 terminal interface. The unit supplies Data Set Ready to both terminal devices and presents Carrier Detect to either terminal when the other terminal's Request-to-Send lead is activated. In

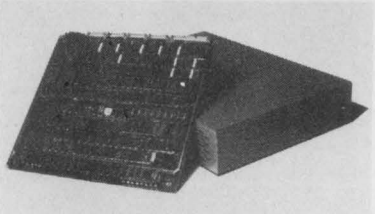


sync applications, it generates highly accurate send and receive clock signals used by both terminals. The signals are derived from an internal crystal generator or, optionally, from a clock produced in either terminal unit. Request-to-Send/Clear-to-Send delay is strapped for 0, 10 or 50 ms. Operable at strap selectable rates of 1.2, 2.4, 4.8, 9.6 and 19.2 Kbps (options at 3.6 & 7.2 Kbps), the ME-31 is a compact and lightweight unit available in rack-mounted, multichannel or stand-alone configurations. $315. **Datacomm Management Sciences Inc.**, 25 Van Zant St., East Norwalk, CT 06855. **Write 246**

SMD CONTROLLER

Interfaces SMD-Type Disk Drives With HPIB Systems

The UP-1697 is a compact, μP-based disk controller that operates up to 4 SMD-type disk drives. It specifically complements HPIB systems such as the HP 3000 Series. Providing command set compatibility and software transparency, the disk controller permits HPIB systems to perceive all attached drives as HP drives. Features include data buffering, automatic track seek and position verification,



automatic alternate track processing, automatic ECC, extensive controller and drive diagnostics, diagnostic software tests, MSI μP technology and a low parts count. To prevent data overruns/underruns during a data transfer, it has an internal 4 kB data buffer with parity, which smooths the data flow between the HPIB and the disk. Under $10,000. **United Peripherals**, 432 Lakeside Dr., Sunnyvale, CA 94086. **Write 256**

SUPPORT CIRCUITS

Write Driver And Sense Functions For Bubble Memory

CL9001 and CL9002 are both organized in 4-channel format and require a minimum of external components. On-chip facilities allow expansion at the system level. The CL9001 sense amplifier has a programmable sensitivity in the range 2 to 10mV, while tolerating a DC offset of up to ±100mV. Four input channels are muxed into two tri-state TTL output stages. Data is latched prior to the output stage. Strobe and multiplex inputs are TTl-compatible. An externally applied voltage is used to set the switching threshold. The CL9002 write driver has a 300mA drive capability and includes comprehensive protection facilities to prevent fusing of the delicate bubble memory device under fault conditions. Protection circuitry limits the max pulse width and repetition rate of the output current pulse, thereby limiting the mean power which can be applied to the device. **Plessey Research Ltd**, Allen Clark Research Centre, Caswell, Towcester, Northants NN12 8EQ. **Write 253**

AC/DC MOTORS & DRIVES

Programmable Controls Plus Service

This 24-pg illustrated brochure describes Reliance AC and DC motors, adjustable speed drives, plus Dodge, Master and Reeves mechanical power transmission products. Containing descriptive material for over 100 products, the brochure (A-2603-1) identifies Reliance Duty Master AC motors and SUPER RPM DC motors for both standard and specialized industrial applications plus Reliance VS Drives with ratings from ¼ to 3000 HP. The drive section also contains a convenient guide to drive selection for matching the units to specific production requirements. **Reliance Electric Co,** 24701 Euclid Ave, Cleveland, OH 44117. **Write 126**

COMPONENTS

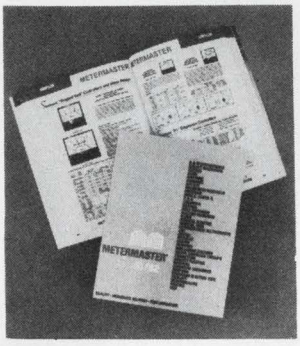
C&K Miniature And Subminiature Switch Products

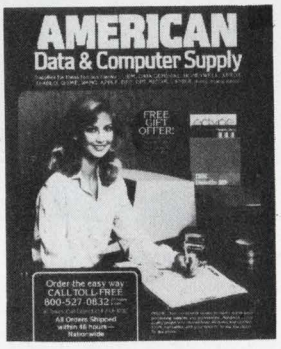
The 72-pg catalog (no. 8105) features descriptions, specs and ordering information on a complete selection of miniature and subminiature switches including a variety of toggle, rocker, pushbutton, slide and rotary switches. Also featured is a selection of hardware and accessories available for application and installation. **C. Tennant Electronics,** 1051 Blake St, Edwardsville, KS 66113. **Write 129**

TEST AND MEASUREMENT

Features Design and Performance Specs

This 432-pg catalog contains design and performance specs for all meters, oscilloscopes and other test and measurement products. In addition, the publication has been created to serve as an in depth reference source for both engineers and buyers. Product and test equipment categories are organized alphabetically according to manufacturer, and a special glossary has been added. The company represents nearly 40 manufacturers, covering the full range of the test and measurement instrument market. **Metermaster,** 5646 Jillson St, Los Angeles, CA 90040. **Write 127**





COMPUTER SUPPLIES

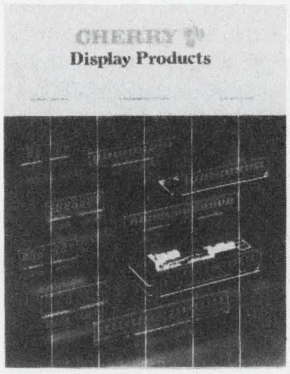
New Technology Products And Accessories

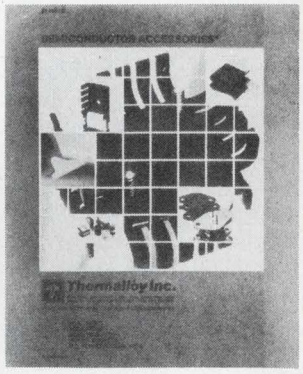
This 32-pg catalog offers hundreds of New Technology office products and accessories from name brand manufacturers at "factory-to-you" savings of up to 50%. Items include flexible disks and minis, cassettes, disk cartridges and computer tapes, ribbons and furniture from manufacturers like IBM, Memorex, Syncom, Pelikan and others. The catalog includes compatibility guides enabling buyers to select the exact products specified for the system they're using. **American Data & Computer Supply,** 2828 Forest Lane Suite 2071, Dallas, TX 75234. **Write 128**

DISPLAY PRODUCTS

Describes Gas Discharge Displays

The complete line of Cherry gas discharge displays and display systems is included in this 16-pg handbook and catalog. Included in the full-color publication are application data and specs for the expanded Cherry line of standard display panels, special custom format display panels, alphanumeric display systems. Catalog CE-987 describes gas discharge displays available in a choice of 7 segment numeric; 7, 14, or 16 segment alphanumeric, or custom format readouts. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60087. **Write 133**





SEMICONDUCTOR ACCESSORIES

Labor-Saving Products Emphasized

Labor-saving options and accessories are highlighted in this 1982 Semiconductor Accessories catalog. Heat sink options such as solderable stud and solderable mounting tab, to accommodate wave soldering, and device mounting stud are identified throughout the book by special symbols on specific applicable products. Insul-Cote pre-coated insulators, snap-on card ejectors and pullers are also detailed as labor-saving accessories. Complete with technical and testing data, the 64-pg catalog is a concise guide for the engineer, designer or specifier relating to heat sinks, insulators, mounting pads, power sockets and PC board accessories. **Thermalloy Inc,** Box 340839, Dallas, TX 75234. **Write 135**

COMPUTER EQUIPMENT & SUPPLIES

Includes Hard To Get Items

"The World's Largest Selection Of Computer Supplies" is a new 64-pg catalog which contains many hard to get items such as: computer tape and storage, disk packs and storage, disk cartridges and storage, control panels and wires and storage, computer ribbons, insulated disk and computer tape files, diskettes and storage, magnetic cards and storage, word processing cassettes and supplies, digital cassettes and storage, video cameras, personal computers, computer room furniture and protective equipment, CRT terminal workstations, and acoustical cabinets to reduce noise. **Edward Ochman Systems,** Box 141, Fairfield, CT 06430. **Write 132**

POWER SUPPLY CATALOG

Includes Applications And Selection Guide

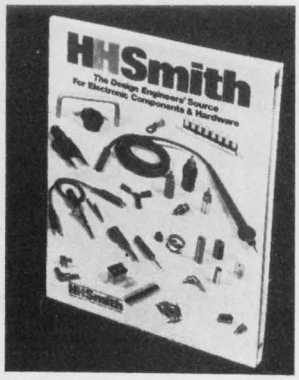
The 56-pg, 1982 edition of the full-line catalog contains detailed information on power supplies providing outputs from 1 to 200V, to 60A. Comprehensive lines of miniaturized

power modules (in both PC board and chassis-mounting versions), in addition to plug-in, premium performance, general purpose, narrow profile, laboratory benchtop, programmable and unregulated power supplies, and a new line of redundant output power systems, are included. Many models provide dual and triple outputs. **Acopian Corp,** Easton, PA 18042. **Write 134**

ELECTRONIC COMPONENTS & HARDWARE

Includes Technical Illustrations And Product Specs

DIP sockets, connectors, terminals, carriers and a comprehensive group of Type SMA, SMB, SMC Subminiature RF connectors are among the new products in the expanded, 1982 edition of this 112-pg, full line publication. It includes an enlarged selection of spacers; modular and safety test leads; prod, probes and other items in demand by design engineers and purchasing agents. Enlarged technical illustrations, product specs in chart form, complete with descriptions, and sectionalized product categories, are all part of a new design format. The book is subdivided into 9 general sections that include over 20,000 items. **Herman H. Smith Inc.** 1913 Atlantic Ave, Manasquan, NJ 08736. **Write 136**



TEMPERATURE MEASUREMENT HANDBOOK

Describes Over 12,000 Products

This 1982 Temperature Measurement Handbook And Catalog contains over 400 pages in full color describing over 12,000 temperature measurement products — from fine-diameter unsheathed thermocouple wire to sophisticated computer interfaces for μP temperature data. Helpful reference text includes latest NBS Thermocouple Calibration Tables; Alloy Property Data and Trade Names; Useful Ranges of Thermocouples; a Material Selection Guide; Temperature vs. Resistance Tables; Radiation Emissivity Tables for Metals and Non-metals; plus other technical data. **Omega Engineering Inc,** One Omega Dr, PO Box 4047, Stamford, CT 06907. **Write 137**

DATA CONVERSION CATALOG

Covers Theory of Operation, Applications

This 288-pg catalog describes A/D, D/A, Synchro and 1553 data bus products. DDC's Data Conversion Products are organized into 9 general categories. Each section is preceded by a discussion of the theory of operation and pertinent application notes. An alphanumeric product index listing all of DDC's Data Conversion products is included. The information on each product is designed to give all of the information necessary to choose the precise product for your application. Each detailed data sheet is self-contained. Military specs, where applicable, are also listed. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716. **Write 141**

TEST PROCEDURES

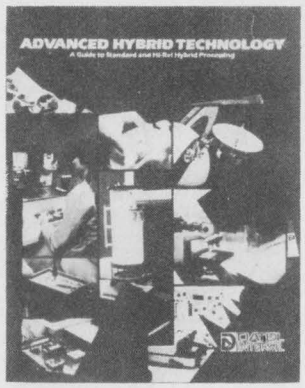
For High Voltage Power Supplies

This 12-pg bulletin (STP-783), "Standard Test Procedures For High Voltage Power Supplies," describes high voltage power supply loading methods for both constant and changing load; test set-ups and procedures for voltage calibration; and test set-ups and methods for both static and dynamic output voltage regulation. It also contains instruction for checking output current regulation, ripple, temperature coefficient and stability. Charts show applications and features of typical Spellman high voltage power supplies. **Spellman High Voltage Electronics Corp,** 7 Fairchild Ave, Plainview, NY 11803. **Write 142**

ADVANCED HYBRID TECHNOLOGY

Also Describes Thin-Film Resistor Technology

A new facilities brochure, "Advanced Hybrid Technology," is a 4 color, 20-pg booklet. It provides detailed information on the high level of hybrid production technology and thin-film resistor technology at Datel-Intersil. Also included is information on high reliability processing for MIL standard devices conforming to MIL-STD 883B. **Datel-Intersil,** 11 Cabot Blvd, Mansfield, MA 02048. **Write 139**



COMPUTER RELATED PRODUCTS

New Items Include Decollator, Testers

This 100-pg, 4 color catalog lists over 2000 computer related products. The publication introduces a score of new items including an RS232 line tester, a power line tester and a rapid throughput decollator. Also newly featured are a media rack and truck for efficient storage and transportation of magnetic tape and a data file for organizing printouts. **Inmac,** Dept. 36, 2465 Augustine Dr, Santa Clara, CA 95051. **Write 140**

UPDATED BIPOLAR LSI DATABOOK

Includes Bipolar Memory And Logic Circuits

This 362-pg "Bipolar LSI 1982 Databook" contains data sheets of all Monolithic Memories bipolar memory and logic

circuits. Nearly twice as large as last year's version, the 1982 databook has been expanded to include new products and new product categories. New sections include chapters on HAL (hard array logic) and HMSI logic families. Expanded existing sections include PROM; ROM; character generators; PAL; FIFO; arithmetic elements and logic; multipliers /dividers; and octal interface. $7. **Monolithic Memories,** 1165 E. Arques Ave, Sunnyvale, CA 94086. **Write 130**

RAM TEST SYSTEM

Describes High-Volume Testing Of DRAMs

This 16-pg color brochure shows how the J385A RAM test system provides the quality of measurement required for high-volume testing of dynamic RAMs, while keeping the total cost of testing low. The brochure notes that the initial capital cost of a test system is only one component of the cost of testing. Recurring costs such as maintenance, programming and downtime must be considered when evaluating the total test cost, as well as lost revenue and market share from missed shipments. The brochure also provides technical information about the system. **Teradyne Inc,** Semiconductor Test Div, 21255 Califa St, Woodland Hills, CA 91367. **Write 131**

SNAP SWITCH CATALOG

Provides Specs And How-To-Specify Aids

This 32-pg catalog describes 12 families of snap-action switches. In addition to basic switches, there are several sealed push button and toggle action groups, military and commercial versions and many special purpose designs to spark your application solutions. In addition to specs and how-to-specify aids, Catalog 101 offers a Glossary of Terms; a technical discussion about ratings, loads, contracts, materials, applications and approvals; and a pictorial explanation of the patented Otto snap-action mechanism. **Otto Engineering Inc,** 2 E. Main St. Carpentersville, IL 60110. **Write 138**

COMPUTER GRAPHICS

Guide To Markets, Companies And Business Activities

Computer graphics is a key to industrial and business productivity improvement. As a result, computer graphics markets are thriving, and companies and businesses in the field have become of keen interest to corporate planners and managers, investors and entrepreneurs. The guide contains succinctly written descriptions of market intelligence, recent public offerings, entrepreneurship, and mergers/acquisitions, including (where appropriate) the name of each subject company, address, person to contact and phone number. Sources outside the US are also included. For free copy write on letterhead and enclose a self-addressed, stamped envelope (37¢ US; $1.20 elsewhere). **Markets CG Guide,** C/O The Harvard Newsletter On Computer Graphics, Service Dept., PO Box 89, Sudbury, MA 01776. **Write 257**

If your address label is printed in 'Red', your subscription is about to expire. See page 52 for details.

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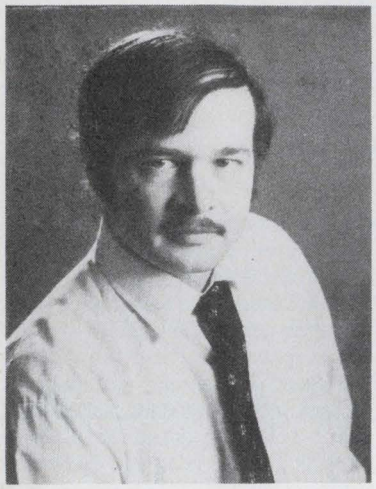
Advertisers Index

For a complete listing of all products in this issue, check the Product Index on page 80.

Continued Growth Ahead



Paul Snigier, *Editor*

If you've read **Digital Design** over the past three years, you already know that we've provided the most current and comprehensive design and product information on add-in memories, Winchester and floppy disks, power supplies, software, development systems, terminals, logic analyzers, printers and other state-of-the-art subjects.

But now, we are going to pull out all the stops. What's in store? In coming issues you'll see more of these popular features, and joining them will be an increasing number of design-oriented application articles. This is a massive undertaking, but we think you'll find it worth our effort. We are expanding our editorial horizontally and vertically to include circuit design, connectors, enclosures, electromechnical devices used in peripherals, and just about anything our readers design with and specify. Included in our feature material for 1982 will be:

April	Hard Disk Drives/Backup Storage
	Power Supplies
	Home Information Systems
May	Computer Input Devices
	Add-In/Add-On Memories
	Speech Synthesis/Speech Recognition
June	Tape Drives
	Desktop Computers
	Data Acquisition
July	Alphanumeric Displays
	Graphic Displays
	Single Chip Microcomputers
August	Single Board Computers
	Software
	Hardware, Packaging, Interconnects
September	Hard Copy
	Microcomputer Development Systems
	Semi-Custom Logic
October	Hard Disk Drives, Backup Systems
	Minicomputers
	Networks
November	Computers and Peripherals
	Power Supplies
	CAD/CAM
December	Printers
	Development Systems
	Logic Analyzers

We're accepting article proposals on many of these subjects. If you'd like us to consider your proposal, send us a two-page detailed summary (remember, we have a three-month lead-time on all editorial material). We will pay $35 to $75 per page upon publication. Application Notebook entries get a flat $70 payment upon acceptance. Send to: Features Editor, **Digital Design,** 1050 Commonwealth Ave., Boston, MA 02215.

Finally, we would like to thank you for your inputs. Your comments in letters, on reader service cards, on the phone and in person have provided our design editors with valuable feedback. So, stay with **Digital Design** throughout 1982 and into the future, and you'll get more top-notch product and design ideas.

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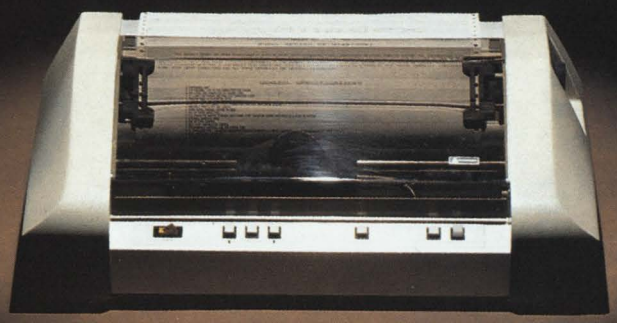

Since their introduction in mid-1980, the Anadex high-resolution DP-9500 Series matrix printers have set new standards for printer quality and performance. All models feature the rugged Anadex 9-wire print head that combines long life with resolutions of 72 dots/inch vertical and up to 75 dots/inch horizontal. With this kind of resolution, fineline graphics (under data source control) and razor sharp characters are pluses built into every printer.

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