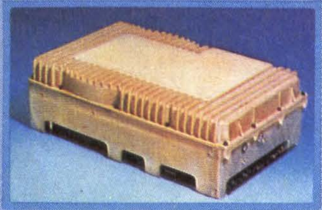
VOLUME 11, NO. 12 DECEMBER 1981

Digital Design

Computers • Peripherals • Systems

Photos below courtesy of Pertec and Dolch Logic Instruments



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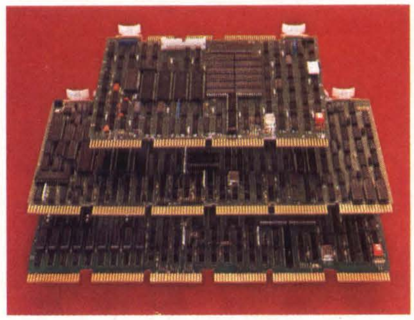

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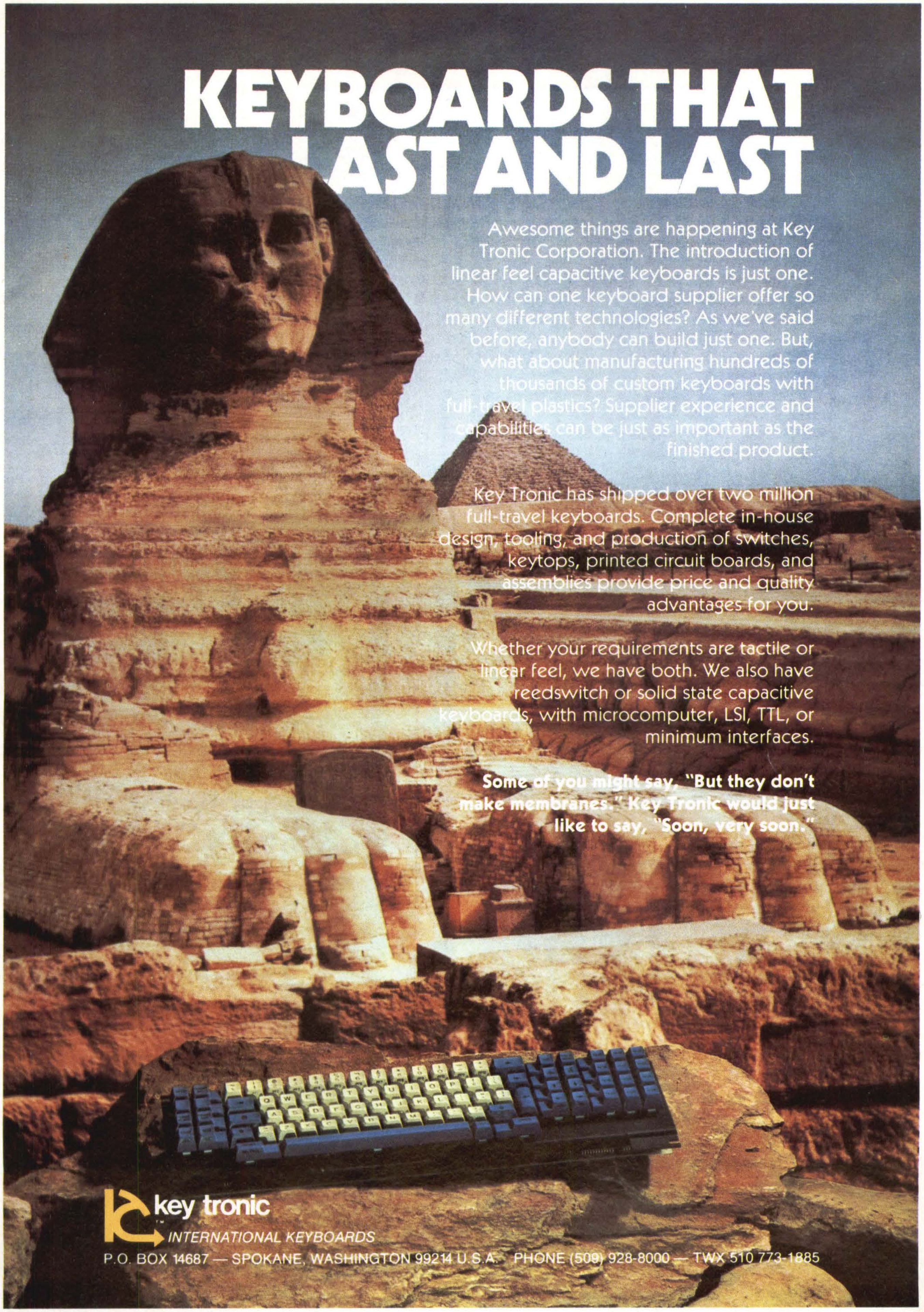

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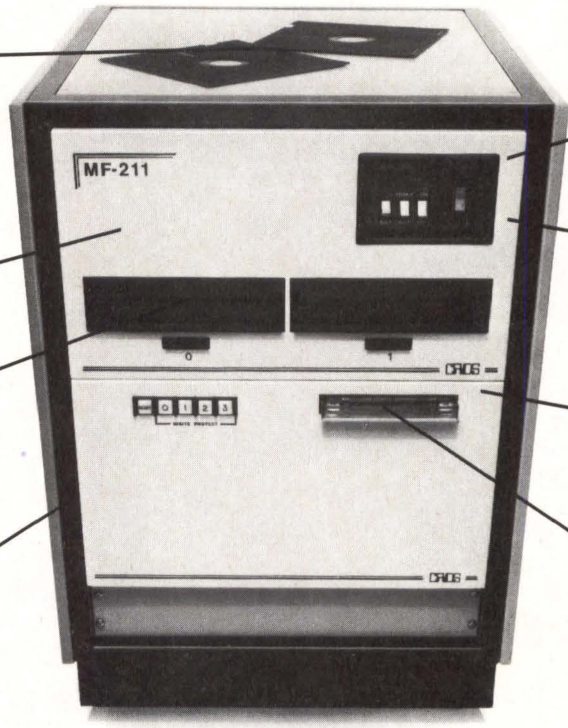

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Letters

ad problems annoying

Dear Editor:

Regarding your July 1981 editorial ("Do Prices Count?"), there are additional problems that are quite annoying:

1. Never getting responses to written or telephoned requests for information or getting a response several months after the request was made. I generally conclude that any company exhibiting this lack of response before any sale is made will be even less responsive after the sale and are therefore dropped from further consideration.
2. Receiving a copy of the ad which caused one to make a request. If you want a copy of the ad, you can make one for yourself or cut out the one you saw.
3. Receiving literature for products other than for those requested. One company is notorious for sending literature about their training courses in response to requests for their hardware catalog!

The lack of at least order of magnitude prices in ads leads one to believe that the advertiser's products are not competitive. Is this the attitude the advertiser's are trying to create?

Everett M. Greene
504 N. Mono
Ridgecrest, CA 93555

Pascal typos corrected

Dear Editor:

Thanks for a nice summary of the Pascal Language in the October issue. A couple of errors appear which bear correcting:

Page 24, col. 1:	VAR D, E:REAL: M, N:INTEGER:
should read:	VAR D, E:REAL; M, N:INTEGER;
Page 24, col. 2:	TYPE COLOR (RED, GREEN, BLUE, YELLOW, PURPLE);
should read:	TYPE COLOR = (RED, GREEN, BLUE, YELLOW, PURPLE);

I always enjoy your articles, particularly those on languages. Keep 'em coming.

Dick Lucas
Compugraphic Corp.
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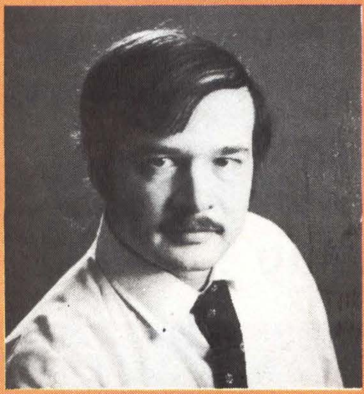
Speakout



Paul Snigier, *Editor*

We are looking for authors to write heavy, technical articles. Starting January 1, 1982, we will pay authors an honorarium for articles and Designers' Notebooks submitted after this date at a rate of $35 to $75 per printed page for feature articles and $70 for Designers' Notebooks. The exact amount depends upon how well the article is written and organized, the amount and quality of artwork (we prefer camera-ready art, but it's not essential), and how much extra work must be done by our editors and artists on your text and figures. Upon receipt of your article, we will mail you an "acknowledgement of receipt." After a review, your article will be accepted, rejected, or tentatively accepted (subject to your revisions). Upon publication of your article, you'll receive a complimentary magazine copy and your check.

What do we want? Problem and solution topics include, but are not limited to: microcomputers, minicomputers, buses and interfaces, power supplies, software (Ada, Pascal, assembly, etc.), printers, plotters, tape drives, floppy and hard disk drives, voice I/O, video display terminals, microcomputer development systems, logic analyzers, etc. Occasionally, we also run submitted engineering management and product buying guides. The technically "heavier" your article is, the more we (and our readers) like it.

Contributed articles fall into four categories:

- Design Articles — specific schemes or methods used to solve a problem.
- Tutorial Articles — educational discussion of a subject, including examples.
- Survey (Special Report) Articles — covers a specific subject, including technology, products, industry trends and selection criteria. A manufacturers' listing and chart of models with specs is often included.
- Application Articles — describes how equipment, system or subsystem(s) were applied, using a case history format. Emphasis is upon the application — not upon the heavy design aspects, as in a design article.

Although these are the four major submitted categories, they are not always distinct and may overlap.

Known as "design ideas" or "cookbook" circuits or software, Designers' Notebook articles are short descriptions of design problems and solutions, circuits or brief programs/subroutines that are clipped by EEs and used in designs. Have you designed and breadboarded a novel and useful circuit that would interest other engineers? Or have you written a unique microcomputer (or even programmable calculator) subroutine or program? If so, then we invite you to share your experiences with our readers. Circuits and software programs must not be previously published (house organs or scientific/technical journals excepted). Finally, we ask that you include schematics, block diagrams and that your program be debugged and your circuit bench-tested.

Requirements. Articles must be original, commercial-free (avoid "product puffing"), useful, accurate, unpublished elsewhere (except for technical or limited journals), and a *sole-submission* to us. Articles simultaneously submitted to other magazines will not be considered.

Format. Most feature articles are between 8 and 20 pages long, the average being about 12 typed pages of double-spaced text. Typically, 3.5 manuscript pages convert to one published page. Number all figures, provide three-line captions, and try to include camera-ready artwork. Label pinouts and callouts clearly. Include computer printout of your programs (don't type or print it).

Writing Procedure.

1. *Abstract*. Submit a *detailed* abstract before starting (of course, if the article is already done, send it directly, along with the abstract).

2. *More details*. After reviewing your abstract, our editors will provide suggestions, how-to information and details of what we require.

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Paul Snigier

Encryption Stampede Falters

Encryption of data and voice is performed by only about one quarter of major communications users, according to a new 151-pg. report from IRD of Norwalk, CT. There will be a significant rise in the use of some types of encryption equipment over the next few years. But, the overall market for encryption devices will be relatively small, reaching some $180M in 1991, compared with the current $70 M level.

IBM and semi makers unhappy

The promulgation of the NBS Data Encryption Standard (DES), coupled with the introduction of DES encryption equipment by major vendors such as IBM, was expected to trigger a big movement towards the use of encryption equipment by commercial and industrial users. But, three years later, the sales of IBM's 3845 and 3846 data encryption devices are "very disappointing". Eight semiconductor vendors have introduced DES chips or chip sets, actions which are "ridiculous, considering the very small number of devices which are required on the market, and the high cost of engineering new LSI chips". If by 1991 all digital encryption devices (except the super-secret COMSEC equipment) are equipped with semiconductor DES chips, the total market will come to only about 10,000 chips that year.

Two years ago, about one-third of major users had set up some type of formal study group to look at the advisability of data encryption. But most telecommunications users chose not to bother with encryption in most cases. Most of the data, text and voice encryption activity is attributable to the military, oil companies and other well-defined user categories — the same folks using encryption techniques ten years ago. One group of users which increased its use of encryption is the financial community. But most bankers still view internal embezzlement and swindling, plus armed robbery, as much more serious problems than wiretapping. Nevertheless, most automatic teller machines now use encrypted data transmission between the machine and the bank's computer, so that telephone taps do not yield customers' account numbers, authorization numbers, etc. which could then be fraudulently used to withdraw cash.

vendors scramble for SOM

The overall leader is Motorola, which has three separate divisions involved in production of encryption devices (communications, government and Codex operations). Next is the relatively small specialty electronics supplier Datotek (Dallas, TX) followed by Rockwell/Collins (which produces encryption devices both in its Dallas, TX and Cedar Rapids, IA facilities) and Controlonics (Westford, MA). Other specialized U.S. suppliers include Technical Communications Corp. (Concord, MA) and Mieco (Cockeyesville, MD).

U.S. Encryption Equipment Vendor Rankings

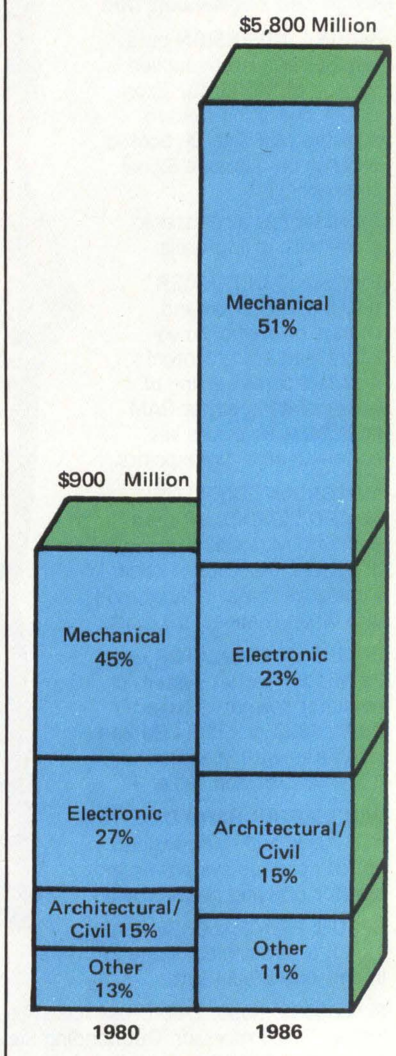
1 Motorola
2 Datotek
3 Rockwell/Collins
4 Controlonics
5 Mieco
6 IBM
7 Rapicom
8 Technical Communications Corp.

Source: International Resource Development Inc.

The relatively small size of the encryption market and its fragmented nature will continue to make it attractive to small specialty vendors — not the IBM's and AT&T's — since the latter generally require a significant production volume to achieve profitability.

1986 CAD/CAM Market Will Exceed $5.8 Billion

The worldwide market for CAD/CAM will exceed $5.8B in 1986, up from $900M in 1980, reports Input of Palo Alto. The worldwide installed base of CAD/CAM graphics workstations will reach 100k units by 1986, increasing at an average annual growth rate of 35% per year from 17k units in 1980. Worldwide concern over industrial productivity is the driving force behind CAD/CAM.



Source: Input

Mechanical engineering, the dominant market sector, will reach $3B by 1986, increasing over 39% per year. The manufacturing and production portions of this market sector are virtually untouched by CAD/CAM technology today and will provide a new market impetus as CAD/CAM systems become further integrated.

Architecture/civil engineering is the smallest segment and will become one of the fastest-growing, reaching nearly $900M by 1986. The electronics market, showing recent softening, will increase more than 32% per year between 1982 and 1986, as users begin implementing new design tools and major in-house developed systems.

Quiktalk Talks 180 WPM

The closest approach yet to connected-word or continuous speech recognition, Threshold's Quiktalk (TM) feature more than doubles the rate at which users speak to computers. It eliminates the 0.1-0.2 sec. inter-word pause required by earlier systems. Users may now speak in a faster, more natural manner. Moderately experienced operators have achieved better than 99% accuracy at entry rates of 180 wpm — far above most keyboard entry speeds.

Power Supplies In 1982

The power supply industry, which includes plug-in, linear, switcher, uninterruptible, line conditioner, and high voltage power supplies, is expected to reach $7.5 billion by 1985. However, this 14% compound annual growth rate gives little indication of the many changes that will occur within the industry, according to a market analysis released today by CSI of San Jose, CA.

Two distinct types of manufacturers comprise the power supply industry — captive and noncaptive. In the past, the noncaptives have had difficulty penetrating the captive market, which currently accounts for more than 75% of total U.S. power supply revenues. This situation is changing.

Growing end-user demand for more sophisticated electronic equipment at lower prices will cause captives to reevaluate their engineering efforts and manufacturing costs. Recognizing, in some cases for the first time, that significant resources are being used for the design, development, test and evaluation of power supplies, many firms will begin negotiating with noncaptives to meet their power supply needs.

Increasing competition from overseas manufacturers will also impact the marketplace during the forecast period. Large quantity orders are becoming commonplace, with a uniformity of outputs and general specifications. This standardization will allow foreign competitors to achieve significant penetration into the U.S. market. Japan and Korea are currently leading non-U.S. competitors with well-developed, high-quality production techniques.

VHSIC Creating Super Chips

VHSIC chips that resemble an array of 100 Los Angeles street maps printed on a thumb tack are in development at Hughes Aircraft Company. Under a three-year, $26.5-million Phase 1 VHSIC contract with the U.S. Army Electronics Research and Development Command, Hughes' Electro-Optical and Data Systems Group will develop chips for use in a variety of high-speed signal processing applications. Additionally, the company will build a brassboard demonstration processor for the Army's Battlefield Information Distribution System (BIDS), containing VHSIC chips.

Slated for the 1990s, BIDS, is a portable, two-way system for position location reporting and communications among Army troops. It will be an adaptive, or electronically alterable, communications system that will allow for an automatic increase in its data rate for less intense jamming situations.

Hughes' Research Laboratories in Malibu, Calif., received a separate $8.1-million Army contract to develop a high-speed EB lithography system that will focus beams of electrons to "write" circuit patterns in submicron dimensions. Perkin-Elmer/ETEC Corp., Hayward, Calif., is the major subcontractor for the lithography system.

Signetics And Honeywell Gate Array Pact

The recent Signetics and Honeywell formation of a joint technology exchange covering Integrated Schottky Logic (ISL) gate array technology allows Honeywell access to Signetics' present bipolar ISL gate array technology and establishes a cooperative design approach to future products.

Honeywell will adopt the Signetics arrays as their standared ISL gate array design approach and establish and maintain sourcing compatibility between Honeywell's captive semiconductor operation, the Solid State Electronics Div., and Signetics.

Once sourcing compatibility is established, Honeywell and Signetics will collaborate on the development of new arrays with higher gate count and more inputs/outputs (I/Os) for use within Honeywell and for Signetics standard ISL family. The two firms will also co-operatively implement next-generation oxide-isolated ISL arrays to achieve lower power and reduce gate delays from the current 4 ns range to a 1 to 2 ns range.

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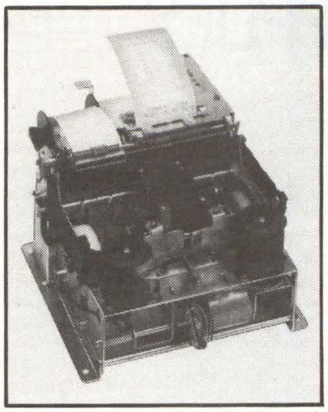

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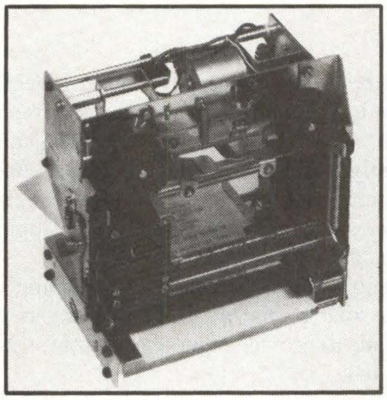
Basic models illustrated on this page are obtainable with various options to suit your application needs. Data sheets with technical specifications for each of these products are available upon request.



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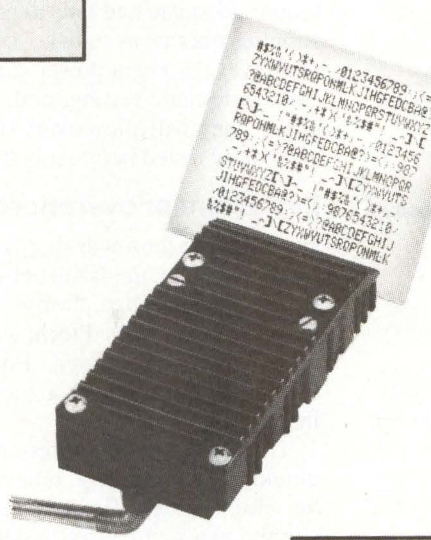

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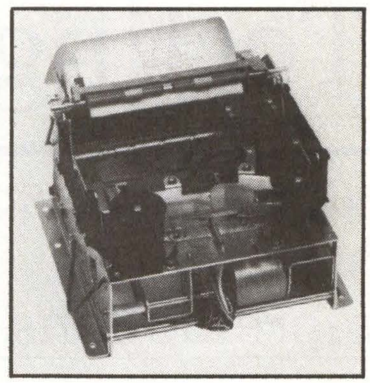

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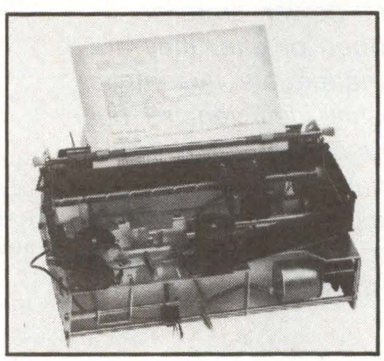

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Economical Power Supply Testing

new power supply testers offer more options

Methods used to test power supplies — before they are shipped or after they are received — are woefully inadequate. Automatic testers eliminate manual testing inefficiencies, but the price — averaging around $100,000 — is too steep for many potential users. With the introduction of lower-cost supply test systems, complete, efficient power supply testing will become available to almost any power supply manufacturer or user.

by Ray Parker

Power supplies must be tested thoroughly and efficiently before they are shipped. Yet too often, they are not. Why? Because until recently, it was impossible or economically impractical to efficiently test every power supply manufactured, thoroughly documenting where and how failures occurred or giving users a written assurance that the supply met all acceptable standards.

A complicating factor, the increasing sophistication of power supplies means that partial or sample testing is no longer adequate and fails to provide complete assurance that supplies operate as stated.

However, recent power supply test systems provide low-cost, automatic testing; and, the future will see more systems. They will allow every supply shipped to be thoroughly and easily tested before it is shipped.

inefficient or overpriced

Even though thorough supply testing is more important than ever, testing methods fall between inefficient and haphazard. Until three years ago, the only way to test power supplies was manually — a skilled technician with an oscilloscope, voltmeter and screwdriver. For a company manufacturing thousands of supplies a month, this was inefficient and inadequate.

Then came automatic testers. They sorted out bad supplies quickly and uniformly, relieving the technician to use his or her skills more efficiently to repair bad parts. Testing and supplying a written pass/fail report, which would have taken a technician 30 to 40 minutes for each power supply, was now easily accomplished in two or three minutes by production line-level personnel.

The automatic supply testers significantly improved the consistency of testing, ensuring that the same test was performed every time, raising the confidence level in the testing accordingly, and increasing output. In short, automatic power supply testers were a real breakthrough.

There was one problem: the price. The admission price into the automatic power supply tester club was, at an average of approximately $100,000, enough to scare away most potential users. Even if they did make the investment, many found the automatic tester could only handle some of their supplies — usually the most expensive. It was simply impractical to purchase enough of the expensive test equipment to be able to use it on every $50 power supply coming off the production line.

Ray Parker is president of Microcomputer Power, Inc. in Santa Clara, CA.

Some companies tried to strike a balance by building their own in-house versions of the automatic testers, but too often most were not nearly as flexible as the commercially-produced testers, and therefore not as useful.

In-house models were generally geared toward testing one power supply model. If a spec changed or new products were added to the line, an engineer had to spend hours modifying the program. Often, after the work was done and the system built, the company found it would have been more cost-efficient to have simply bought a power supply tester.

the new generation

With the introduction of new (and future) power supply test systems, automatic power supply testing is reaching the next rung on its evolutionary ladder. Such automatic supply testers now fit the budget of most power supply manufacturers. Let us examine what the new generation of low-cost, automatic testers will be like. As a means of comparison, we will use the recently introduced MPI-7505 ($25K). Future testers will offer similar features.

The new generation will match the more expensive power supply testers in almost every respect without taking short-cuts on quality.

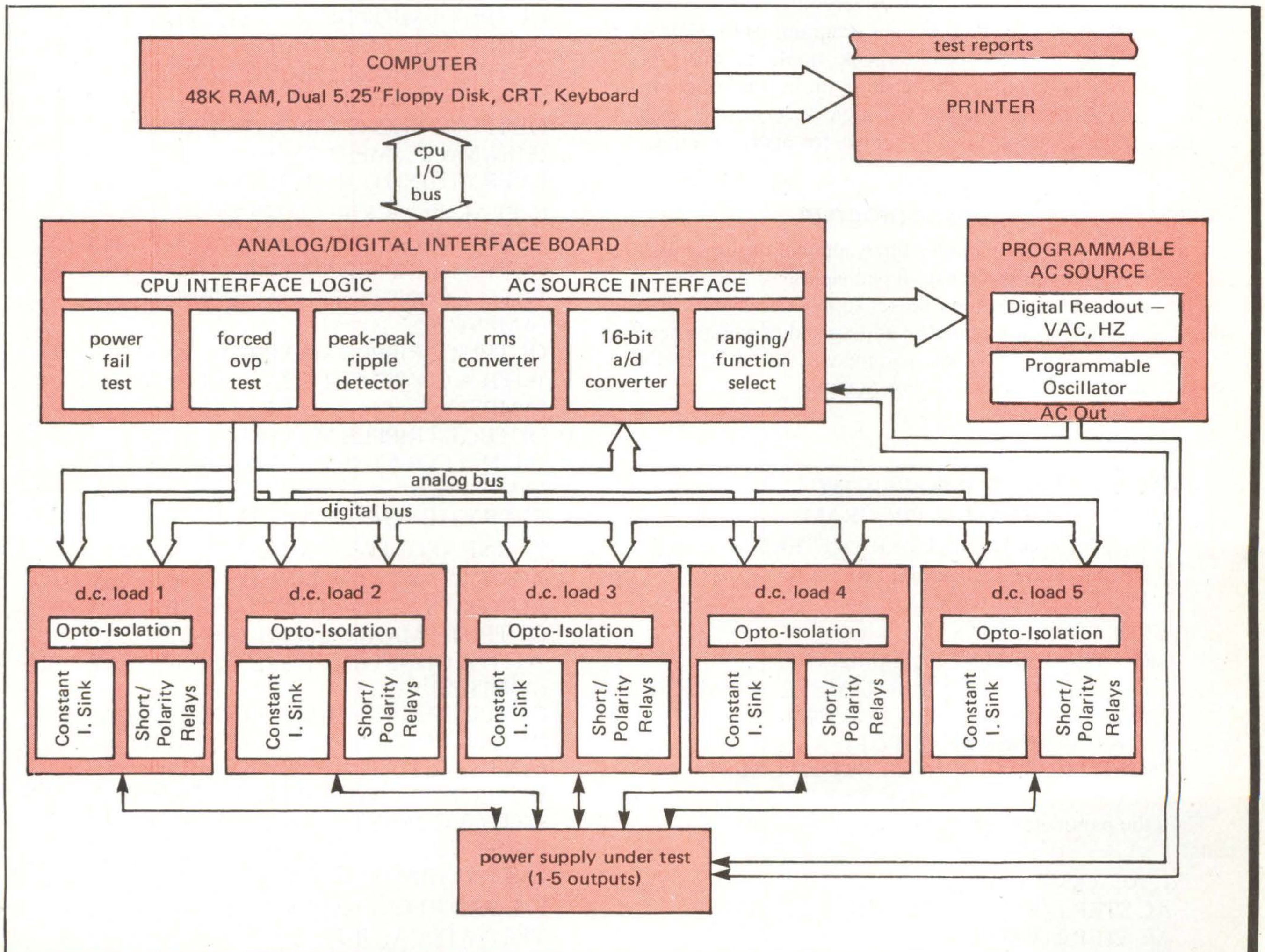
Those firms that manufacture a full line of open frame linear and switching power supplies — unlike most manufacturers of automatic power supply test equipment — will be intimately familiar with the need for (and problems involved in) testing thousands of power supplies a month. If they make testers, they have a natural edge over competitors. Many have or will develop new testers to fill their own need to quickly, efficiently and flexibly test the many different supplies in their product line.

Instead of basing their tester on a large computer selling for $35K, they will incorporate much less expensive micro-computers, such as a TRS-80 with a printer, into the new testers. In addition, they will have a single board interface rather than many PC boards, making it easier to produce. This means fewer parts than comparable testers, making them more reliable and easier to service.

They will contain all software needed to create and edit program specs. The maker will provide users with the source for all programs written for the tester, so users can customize software to use the tester for specific applications.

The user can write his own specs for the supplies to be tested, store those specs in the computer on a floppy disk, and be testing the supplies within a half hour of delivery.

Advantages are obvious. A company can now afford approximately four times as much automatic testing power as it could afford with the more expensive testers. For many companies, this means every supply coming off the production line can be thoroughly and uniformly tested. Even non-technical personnel can test complex, multi-output switching or linear DC power supplies. Manufacturers can provide their customers with a printout showing in detail that the units supplied meet specification. Power supply users can ensure that every one of their supplies meets specs and provide



Power supply test system architecture shows power supply under test (bottom), system, programmable AC source and computer.

documentation back to suppliers showing exactly where returned supplies failed. Throughput and efficiency will be increased dramatically.

the basic system

The basic system includes a 500W programmable AC source, five 25A loads, controller board and Z80-based computer.

The system conducts eleven tests. (1) An AC ramp-up test for AC current when DC outputs are unloaded; aborts test if AC current exceeds maximum programmed limit. (2) An AC power unloaded test for AC power (RMS) when DC outputs are unloaded; aborts test if AC power exceeds programmed limit. (3) A voltage test for output voltage when unloaded min/max limits are programmed; also prompts the operator for adjustment of trimpot if applicable. (4) A current limit test for the current limit point; min/max limits are programmable, and test prompts operator for adjustment if applicable. (5) A short circuit test for short circuit current; min/max limits and load current are programmable. (6) A line regulation test for changes in output voltage when the AC input varies from the programmed AC min/max input limits; max volt change and load current are programmable. (7) A load regulation test for changes in output voltage when the programmed min/max load current varies; max volt change limits are programmable. (8) A combined line/load regulation test for changes in the output voltage when the AC line varies from programmed min/max input limits and the DC load current varies from min/max limits; min volt change limits are programmable. (9) An overvoltage test for the OVP trip point; min/max limits are programmable. (10) A drop-out ripple test for peak-to-peak ripple at the programmed AC input; max volt change limits are programmable. (11) A power-fail test for logic level 0 or 1 with programmed AC input; this test allows for operator adjustment when necessary.

flexible software: easy to program

The system's software includes three applications programs simple enough to allow almost immediate use of the tester.

The first program creates a power supply parameters disk file, also allowing for parametric editing and printing a hard copy of the power supply test parameters. It can be easily programmed in a few minutes. For example:

```
>READY
>RUN
MICROCOMPUTER POWER, INC.
ATE TEST CREATION PROGRAM
1. CREATE NEW TEST PARAMETERS
2. PRINT TEST PARAMETERS
3. EDIT TEST PARAMETERS
ENTER SELECTION? 1
CREATE NEW TEST PARAMETERS
ENTER PROGRAMMER'S NAME? R. T. PARKER
ENTER MODEL NAME? FCBB524
ENTER NUMBER OF OUPUTS? 3
ENTER MESSAGE (256 CHR)? FINAL TEST
EVERYTHING O.K. (Y/N)? Y
```

Then the parameters are entered for each of the tester's 11 tests:

```
1. AC RAMP-UP TEST
AC STEP 1 (VAC, HZ)? 20, 60
AC STEP 2 (VAC, HZ)? 50, 60
AC STEP 3 (VAC, HZ)? 115, 60
MAXIMUM AC CURRENT (MA)? 125
EVERYTHING O.K. (Y/N)? Y
2. UNLOADED AC INPUT TEST
TEST WITH AC INPUT AT (VAC, HZ)? 115, 60
MAXIMUM INPUT POWER (WATTS)? 5
MINIMUM INPUT POWER (WATTS)? 1
EVERYTHING O.K. (Y/N)? Y
3. OUTPUT VOLTAGE TEST
TEST WITH AC INPUT AT (VAC/HZ)? 115,60
OUTPUT 1 VOLTS (MIN/MAX)? 23.5, 24.5
LOOP FOR OPERATOR ADJUSTMENT? Y
OUTPUT 2 VOLTS (MIN/MAX)? -5.1, -4.9
LOOP FOR OPERATOR ADJUSTMENT? Y
OUTPUT 3 VOLTS (MIN/MAX)? 4.9, 5.1
LOOP FOR OPERATOR ADJUSTMENT? Y
EVERYTHING O.K. (Y/N)? Y
4. CURRENT LIMIT TEST
TEST WITH AC INPUT AT (VAC, HZ)? 115, 60
OUTPUT 1 CURRENT LIMIT IN AMPS
(MIN/MAX)? 3.4, 5
LOOP FOR OPERATOR ADJUSTMENT? N
OUTPUT 2 CURRENT LIMIT IN AMPS
(MIN/MAX)? .7, 1.2
LOOP FOR OPERATOR ADJUSTMENT? N
OUTPUT 3 CURRENT LIMIT IN AMPS
(MIN/MAX)? 3, 5
LOOP FOR OPERATOR ADJUSTMENT? N
5. SHORT CIRCUIT TEST
TEST WITH AC INPUT AT (VAC, HZ)? 115, 60
OUTPUT 1 SHORT CIRCUIT CURRENT
(MIN/MAX) AMPS? .05, 1
OUTPUT 2 SHORT CIRCUIT CURRENT
(MIN/MAX) AMPS? .05, .5
OUTPUT 3 SHORT CIRCUIT CURRENT
(MIN/MAX) AMPS? .05, 1
EVERYTHING O.K. (Y/N)? Y
6. PEAK-PEAK RIPPLE TEST
TEST WITH AC INPUT AT (VAC, HZ)? 115, 60
OUTPUT 1 RIPPLE MAXIMUM (MV)? 10
WITH A CONSTANT LOAD CURRENT AT
(AMPS)? 3
OUTPUT 2 RIPPLE MAXIMUM (MV)? 5
WITH A CONSTANT LOAD CURRENT AT
(AMPS)? .5
OUTPUT 3 RIPPLE MAXIMUM (MV)? 5
WITH A CONSTANT LOAD CURRENT AT
(AMPS)? 2.5
EVERYTHING O.K. (Y/N)? Y
7. LINE REGULATION TEST
AC VOLTS AT LOW LINE (VAC, HZ)? 105, 60
AC VOLTS AT HIGH LINE (VAC, HZ)? 125, 60
OUTPUT 1 MAXIMUM CHANGE (MV)? 10
WITH A CONSTANT LOAD CURRENT AT
(AMPS)? 3
OUTPUT 2 MAXIMUM CHANGE (MV)? 10
WITH A CONSTANT LOAD CURRENT AT
(AMPS)? 2.5
OUTPUT 3 MAXIMUM LOAD CHANGE (MV)? 10
WITH A CONSTANT LOAD CURRENT AT
(AMPS)? 2.5
EVERYTHING O.K. (Y/N)? Y
8. LOAD REGULATION TEST
TEST WITH AC INPUT AT (VAC, HZ)? 115, 60
OUTPUT 1 MAXIMUM CHANGE (MV)? 10
FOR A CURRENT CHANGE IN AMPS
```

(MIN/MAX)? 1.5. 3
OUTPUT 2 MAXIMUM CHANGE (MV)? 10
FOR A CURRENT CHANGE IN AMPS
(MIN/MAX)? .2. .5
OUTPUT 3 MAXIMUM CHANGE (MV)? 20
FOR A CURRENT CHANGE IN AMPS
(MIN/MAX)? 1.2. 2.5
EVERYTHING O.K. (Y/N)? Y

9. COMBINED LINE/LOAD REGULATION TEST
AC VOLTS AT LOW LINE (VAC.HZ)? 105. 60
AC VOLTS AT HIGH LINE (VAC. HZ)? 125. 60
OUTPUT 1 MAXIMUM CHANGE (MV)? 20
WITH (LOW-LINE. HIGH-LINE) LOAD AT
(AMPS)? 3.0
OUTPUT 2 MAXIMUM CHANGE (MV)? 20
WITH (LOW-LINE. HIGH-LINE) LOAD AT
(AMPS)? .5. 0
OUTPUT 3 MAXIMUM CHANGE (MV)? 20
WITH (LOW-LINE. HIGH-LINE) LOAD AT
(AMPS)? 2.5. 0
EVERYTHING O.K. (Y/N)? Y

10. OVERVOLTAGE PROTECTION TEST
TEST WITH AC INPUT AT (VAC. HZ)? 115. 60
OUTPUT 1 OVERVOLTAGE AT (MIN. MAX)
VOLTS? 0. 0
OUTPUT 2 OVERVOLTAGE AT (MIN. MAX)
VOLTS? 0. 0
OUTPUT 3 OVERVOLTAGE AT (MIN. MAX)
VOLTS? 5.7. 6.1
EVERYTHING O.K. (Y/N)? Y

11. DROP-OUT RIPPLE TEST
TEST WITH AC INPUT AT (VAC. HZ)? 105. 60
OUTPUT 1 MAXIMUM PK-PK RIPPLE (MV)? 5
WITH A CONSTANT LOAD CURRENT AT
(AMPS)? 3
OUTPUT 2 MAXIMUM PK-PK RIPPLE (MV)? 5
WITH A CONSTANT LOAD CURRENT AT
(AMPS)? .5
OUTPUT 3 MAXIMUM PK-PK RIPPLE (MV)? 10
WITH A CONSTANT LOAD CURRENT AT
(AMPS)? 2.5

A second applications program, equally simple, prints complete details of failed tests while the system is running and also allows the option of printing the test report for each tested supply. The third applications program simulates manual test procedures.

A user can generate supply test parameters in 10 to 15 minutes. Automatic testing requires approximately 15 to 25 sec. per output.

the future? more options, lower costs

More and more systems will incorporate advanced features. Among them, a data logging system will allow test parameters from each supply tested to be saved and logged, and a program that will analyze the results for trends. For example, if the supplies are beginning to near the low end of a certain parameter, the problem can be caught before dead power supplies begin turning up on the production line. Expect widespread use of talking, step-by-step guided probe testing. Training a technician to manually test power supplies efficiently can take up to 90 days. With guided probe testing, a tech could be working at full speed the first day. D

Computer Furniture

design and quality determine selection

Today's data processors demand styling crafted for a particular environment. The numerous arrays of furniture and enclosure designs provide both the modern and traditional "look". A broad spectrum of options permit freedom of arrangement without sacrificing technological advances offered in contemporary processing systems.

by John Koltzau

Utility and appearance count today. Your first design requirement will demand that the furniture "fit" your equipment. Computer-oriented furniture falls into three major categories: desks that offer a work surface, combine a work surface with an electronic mounting capability, and vertical electronic cabinetry. Options transform such "bare bones" items into sleek, sophisticated, console-like furniture that is eye-pleasing and functional. You can fit the most basic desk with such options as vertical and horizontal cable troughs, power strips and desk top cutouts for hardware and wiring. With judicious use of these options, you can make safe, as well as unobtrusive, unsightly and sometimes dangerous wiring interconnects.

If your system uses drives or a CPU, you may want an electronic bay to house that equipment. Depending on system size, you may use more than one bay, mounting them at either end of a desk to provide a system enclosure and workstation in one integrated unit. Options like vented panels and fans eliminate heat problems and plexiglass doors, trim and color options supply aesthetics.

Larger systems may need vertical cabinets. A family of matched options takes most utilitarian concepts into account, providing coordination with other furniture.

examine materials

Computer-oriented desk tops, most made of particle board laminated with high pressure plastic, must be thick so they will support terminals, office machines and other parts over an extended time. If the top is too thin, bowing will rapidly develop. Often overlooked, particle board sealing if improperly treated can absorb moisture; and, in time, the top can develop ripples and waves.

Many desks provide a slanted edge along the front (the "Comfort Edge") for operator comfort and efficiency. Due to its placement, that edge receives heavy use and pressures. If the edge is machined from the top, this is superior to the

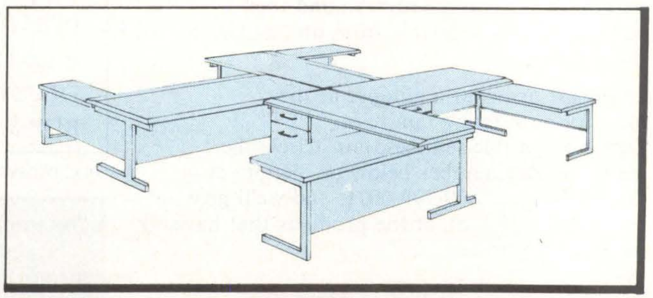


Figure 1: Whole systems are created by combining the modular components of various subsystems. Here, a number of operator stations have been combined.

John Koltzau is marketing manager for Systems Furniture Company, a Los Angeles firm specializing in furniture for the data processing environment.

attached and separate piece.

Two major stylings offer tubular steel legs that give the furniture a light, airy look and laminated particle board slab sides that extend to the floor and give the furniture a "bank" look. Choice depends on taste and the image you want your system to project. If you select slab sides, be certain some form of protection is provided near the floor. High pressure laminates are stain- and scratch-resistant, but they are not indestructable. A kick plate will help immeasurably in preserving furniture appearance. If you choose the steel leg configuration, demand that the manufacturer thoroughly cleans the metal before painting and bake the finish on for longer lasting beauty. Look for little touches as rounded corners that eliminates snagging or ripped clothing and cuts.

Examine furniture fastening methods and options. Preassembled furniture ensures maximum strength, but shipping costs more and limits easily replacing damaged parts.

Other furniture uses snap fasteners, eliminating tools for assembling or dismantling. The fit with snap fasteners may not be as precise or secure. The literal "nuts and bolts" approach allows for reasonably easy assembly, dismantling and damaged parts replacement. Since they can ship the furniture "knocked down," shipping and warehousing costs are much lower.

Determine how drawers, pedestals and small electronic bays are fastened to the desk's underside. Sheet metal screws driven into particle board is acceptable when furniture supports light loads. Greater strength, durability and safety results from tee or Rozan-type nuts, or other reinforcing devices that accept machine screws.

consider manufacturer track records

Few computer furniture features or designs are patentable. Examine manufacturer credentials. How long was he in business? Who are his customers? Can he provide workable modifications of standard products to meet specific needs? Can he supply custom items?

An important item is UL approval. Electronic cabinetry houses heat-producing equipment. Does the cabinet provide adequate ventilation? Are power panels and strips UL-approved and properly installed? Is the particle board flammable or fireproof? A responsible manufacturer supplies UL certification upon request.

Consider, too, the entire product line integrity. Is it modular in concept? Can you add options or delete them easily without destroying furniture aesthetics? Can maintenance personnel easily make modifications or must you return furniture to factory (time-consuming and expensive)?

Judicious selection of compatible furniture ensures proper operation, easy maintenance, longevity and aesthetics. D

Ergonomic Standards Improve CRT Workstations

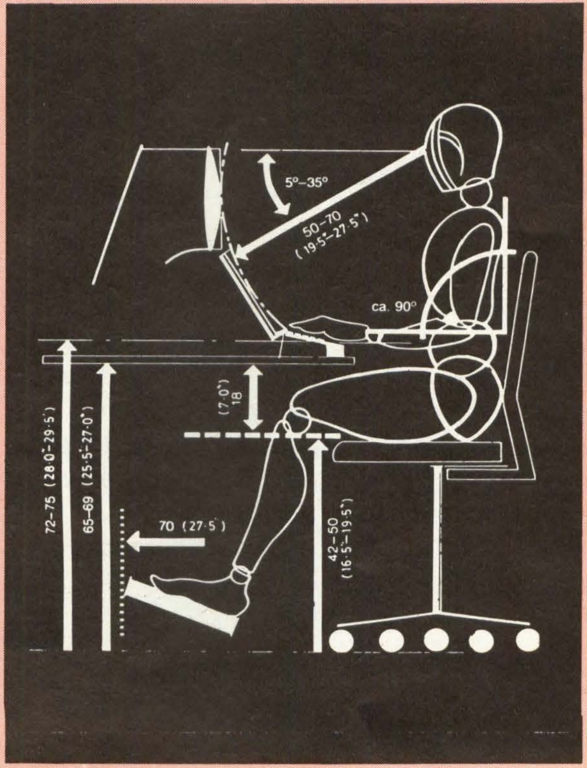
Ergonomic standards for CRT workstations are beginning to impact U.S. regulatory bodies such as OSHA and NIOSH. Ergonomically-designed workstations increase worker productivity through reduction or elimination of fatigue. Such equipment reduces worker fatigue due to eyestrain, headaches and backaches associated with prolonged sessions at CRT or WP workstations. Martha Phillips of Ergotech, the Woodland Hills, CA distributor of Karl Gutman Inc. advanced ergonomic workstations, offered the following advice to OEMs.

Meeting European ergonomic standards is a demanding challenge for furniture vendors. Major parameters designed into CRT workstation furniture to comply with European standards are indicated in the figure.

Besides the head and neck, European standards define the important parameters for arms, legs and feet. The optimal working angle for arms is 90° and legs require 7" of clearance between the bottom of the CRT workstation table and top of the operator's chair.

Leading U.S. and European vendors do not limit their design considerations to basic parameters. They enhance operator comfort by designing furniture to exceed existing standards. Before specifying, look for capabilities such as height adjustability through hydraulic, electromotive or gas cylinder means. To enhance adjustability, which plays an important role in worker comfort, look for movable terminal base plates that tilt, rotate and can be pulled forward or pushed backward, as well as separate keyboard heights and tilt adjustments for CRTs with detachable keyboards.

If you're selecting advanced furniture designs, require more from the vendors. In addition to optimal adjustability, demand extra comfort; such as, padded arm rests on CRT workstations, modularity of design for maximum configuration flexibility and enhanced structural strength of furniture through steel underframe design. D



European standards define the optimal viewing angle of the CRT within a 30° arc in front of the eyes to maximize comfort of the neck and head. The solid arrow drawn from the eyes to the area below the video screen indicates the optimal placement of material that is being copied onto the CRT.

New Directions in GP-IB Controllers

problems and solutions for development applications

This article will deal with what we learned from experience with the GP-IB system concept, and what we might expect in next-generation controllers. Although the controller's primary role is programming and sequencing the instruments in the system to perform the desired operations, it normally has many other functions, such as data reduction and display, report generation and system diagnostics.

by Robert M. Hallissy

First-generation controllers were characterized by the exclusive use of program language statements oriented to the bus hardware concepts. The bus was treated differently from other I/O devices and the programmer needed an intimate knowledge of bus protocol to obtain the desired result.

First-generation controllers had the CMD statement, which allowed the programmer to send an arbitrary sequence of multi-line bus messages to the bus. Second-generation GP-IB controllers are characterized by program language constructs that represent a message organization on a level above the bus hardware message concept. Statements are designed around a set of high-level operations called meta-messages. Each statement initiates a series of actions on the bus which implements a meta-message. The programmer needs only to understand the results of the high-level messages to implement complex systems. This means that controlling the bus is much easier using second-generation machines.

life cycle of a system

We will discuss here the life cycle of a GP-IB test and measurement system as it occurs today to highlight problems. In some cases, possible solutions are suggested that may not yet exist or be technologically feasible.

System life cycle can be analyzed in two segments: development phase and production phase. The two segments have different needs and different users. Also, many GP-IB systems are used in benchtop environments where the system is reconfigured and reprogrammed often (this will be treated as a separate item).

development phase

A system's development phase is the time between system conception and incorporation of the final system into the production environment. System users during this phase are test and system engineers.

During feasibility studies, engineers identify critical system constraints and evaluate potential system components against these constraints. For the controller, three areas of constraint are difficult to measure: bus data rate, I/O throughput (including formatting) and computation throughput. This is partly because controllers are basically computers and not easily characterized. As GP-IB controller technology grows, users will demand that such characterization be possible.

An example is specifying bus data rate. It is possible for two devices, one with a specified 100-kB/sec talk rate and the other with a 100-kB/sec listen rate to communicate at only 50 kB/sec because devices are specified as if we are

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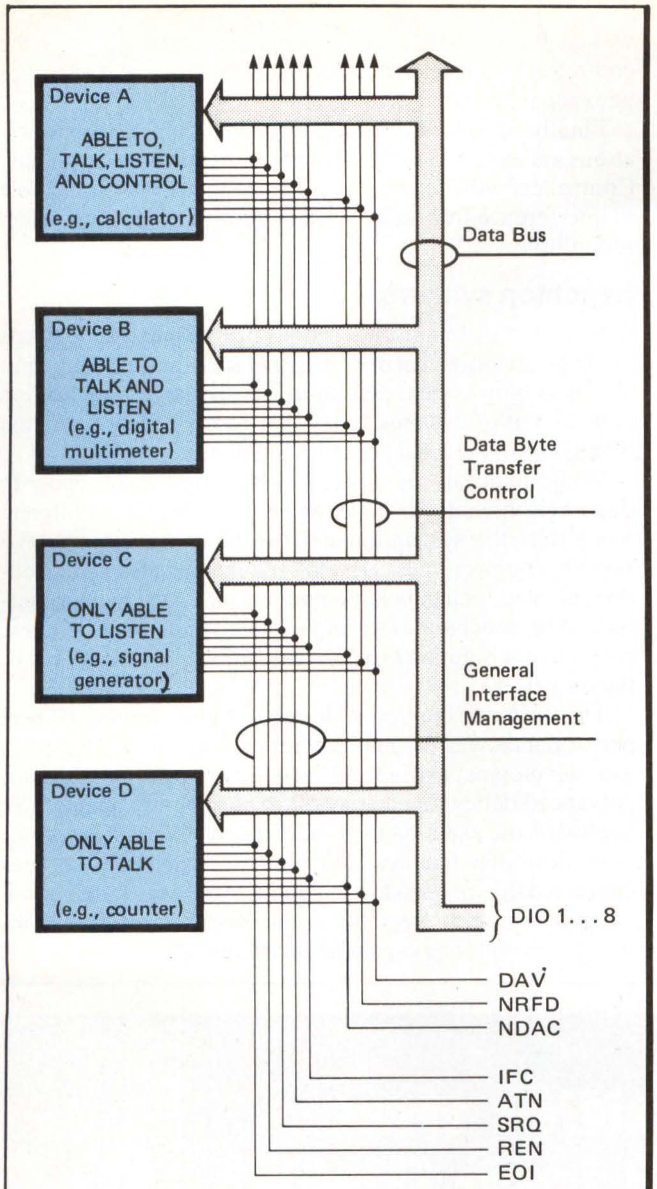


DIO	1-8	Data input/output lines
DAV		Data valid
NRFD		Not ready for data
NDAC		Data not accepted
IFC		Interface clear
ATN		Attention
SRQ		Service request
REN		Remote enable
EOI		End or identify

Figure 1: The general-purpose interface bus (GP-IB) uses a 16-line cable to connect devices equipped with appropriate interface circuitry into a system. Data transfer is byte-serial, bit-parallel at rates up to 1 megabyte per second. Up to 15 devices can be connected to one bus.

dealing with zero-delay partners. Real partners worsen data rate. Specifying data rate as a function of each device's delay parameters might solve this problem in the future.

Measuring throughput (both I/O and computation) has always been a problem for computer users. Throughput depends on application and code implementation. Benchmarks commonly help designers in comparing machines. Select benchmarks that reflect the application. Test and measurement benchmarks are not readily available today. This may remain a problem.

After feasibility studies are complete and system implementation starts, several new problems emerge. The first is compatibility. Although the GP-IB provides electrical, mechanical and protocol compatibility, the higher levels of information on and off the bus are still a problem. Two critical areas to designers are the data message and software investment.

For many reasons, the definition of GP-IB leaves the data message on the bus undefined. This leaves the system designer at the mercy of instrument and controller manufacturers. For example, do you want to provide an option for the system to use a high-speed voltmeter instead of the normal one? You may find the two alternate devices require different character sequences to obtain the required instrument setup. You must design the controller software to handle either one.

Although standardizing the data message for all instruments would eliminate the problem, such a solution might be difficult to achieve. An alternate solution involving only the controller would be to design the controller language so that such inconsistencies can be easily handled. Advances in data formatting and controller program constructs will make it possible to easily program around incompatibilities in system devices.

Manufacturers are also recognizing the large investment that system designers make in developing controller software; except for a few companies, it is difficult to upgrade a controller without reinvesting in new software. Need for software compatibility is causing steady advances in this area.

Another problem is that although instruments and controllers are getting smarter, it is hard for the system designer to fully use all this intelligence. For example, while the first bus-compatible voltmeters just read voltages, they can now pace themselves for sequential readings, control scanners for automatic channel scanning and perform averaging or other computation on the readings before giving values to the controller.

Instruments are being built with large data buffering capability, computational capability and even bus controller functions. One major force in directing the increase in instrument intelligence is the goal to remove all real-time requirements from the bus. Inherently, the bus is incapable of responding in real time to events because there is no maximum time that an instrument can hold up a handshake. Capabilities in the instrument such as data buffering, self pacing, scanner control and alarm detect reduce the real-time response required on the bus.

Raw bus data rate will continue to be important in the future. High bus rates will be demanded to take advantage of the data buffering being designed into instruments, although system operation and integrity will not depend on these high rates.

Techniques for using these new capabilities are sure to lag behind their emergence, but there will probably be some new tools available to the designer to ease the design task. For example, some controllers do not operate cleanly or at all as non-controllers on the bus. Non-controller features such as device trigger, device clear and service request are necessary to enable the designer to implement multiple-controller systems.

production phase

A GP-IB system's production phase starts when the system is turned over to production personnel for continuous operation. Then the production department becomes dependent on reliable system operation in order to meet customer demand. Let's examine some constraints, other than those due to actual system test procedures, that influence the future direction of controller technology.

First, the production operator will probably not have the same background as the test or system engineers who designed the system. It is important that the system and its language be comfortable and easy for the operator to use. The system/operator interface should also be designed to be fail-safe and self-prompting.

New future standards for environmental considerations are expected to be legislated or required by customers. Controllers will emit less interference and be less susceptible to interference from other sources.

Second, while no system is maintenance-free, production cost can be reduced by lower maintenance cost. In the preventive maintenance area, the designer should see more accurate self-check procedures built into future controllers. Also, as part of the standard system startup procedure, the operator should be able to initiate, via the controller, self-diagnosis and fault isolation for all system components.

Improved reliability levels will be emphasized in both controller hardware and firmware. This may include options for the more expensive hardware features such as fault-correcting memory, redundancy, uninterruptible power supply and ruggedized packaging. Higher-quality firmware will enable unattended and remote site operation in which the controller can automatically recover from a variety of unexpected faults.

Finally, new future standards for environmental considerations are expected to be legislated or required by customers. Controllers will emit less interference and be less susceptible to interference from other sources, resulting in higher system reliability.

benchtop systems

A benchtop system fulfills various instrumentation demands made by an individual or group in an R&D-like environment. The benchtop system may represent the largest application area of GP-IB systems today. Its ease of reconfiguration makes GP-IB the ideal benchtop interface.

While many of the arguments presented above apply to this environment, the benchtop user has basically different goals than the system engineer of the earlier system. The system engineer must develop a reliable, efficient, well-documented, maintainable solution with a good human interface. The benchtop user, on the other hand, wants a quick, easy, ad hoc solution to a one-time problem where he will be the only user.

This affects controller features tremendously. Where performance was the major criterion, we now have ease of use, development speed and versatility as primary concerns. Advanced debugging features such as stepping, tracing, live keyboard and examination/modification of variables become very desirable features. While these features have been characteristic of desktop computers for years, the minicomputer makers are showing increased compliance. This will continue for next-generation controllers.

Tape Drives And Heads In 1982

a look at the past and a glimpse at the future

For many years the computer industry has been predicting the demise of tape drives due to the increased capacity of disk drives. It didn't happen. Instead, Winchester technology, with non--removable media, created a tape drive resurgence. Today, the future of tape drives looks better than ever. Their popularity stems in part from their durability — and this has been enhanced by current tape head reconditioning techniques.

by Charles J. Spinnler and Robert Sillers

During the '50s and '60s, tape drives were used as primary storage with densities to 556 bpi and tape speeds up to 37½ ips. Early drives were costly to purchase and maintain. One of the most critical and costly components of the tape drive was (and is) the head. The first digital R/W heads were patterned after audio heads, using separate record and reproduce stacks which required precision alignment, keeping both head and drive costs extremely high. A major cost factor in drive maintenance was head replacement. Because head recovery was non-existent at this time, every head failure meant a new head purchase.

By the late '60s, tape speeds and bit densities doubled. Phase encoding recording raised bit densities past 800 to 1600 bpi, and tape speeds increased to 125 ips. Read while write capability allowed the tape drive to double-check errors while operating rather than rewinding the tape for error checking. Gap-to-gap spacing (timing) became more critical. This brought about the development of the three-piece head.

three-piece head developed

The three-piece head utilized a common center component which housed both the write and read return cores as illustrated in **Figure 2.** This allowed the head manufacturer to hold the dimensional tolerances for skew, scatter, and gap-to-gap spacing. A significant result was reduced drive manufacturing costs since now the burden of tolerance control shifted from the drive manufacturer to the head manufacturer. Perhaps even more important to the drive user was that after the head wore out, the three-piece head could be disassembled and the gap depth re-established to that of a new

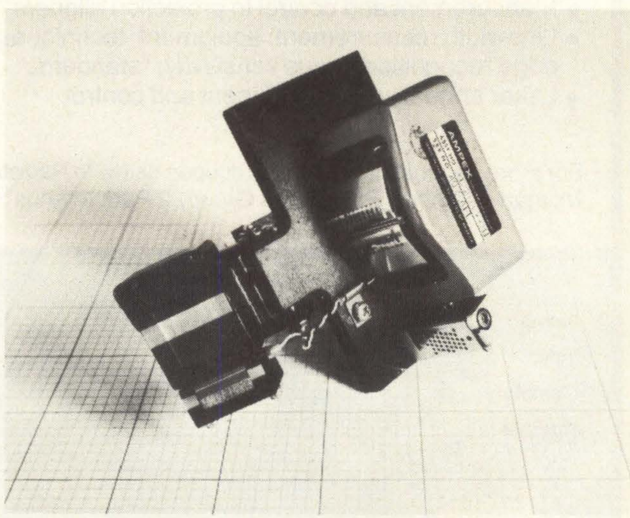


Figure 1: Four piece head with shield assembled. When worn-out, these heads can now be reconditioned rather than replaced.

Charles J. Spinnler is Director of Marketing and Robert Sillers is Director of Sales Engineering at Magnetic Recovery Technologists, Inc., Valencia, CA.

head. The field maintenance cost savings were substantial after the development and introduction of tape head rebuilding (by Magnetic Recovery Technologists, Inc. in the mid '70s).

During this time we also saw the advent of the auto-load tape drive, which necessitated advances in head shielding technology. Copper plating was most commonly used to internally suppress write to read cross-feed since an external flux shield could no longer be used. In addition to copper plating, hard chrome plating or other hard coat processes were introduced to combat the more rapid wear experienced in the higher speed drives.

At about this same period of time (mid-to-late '60s), the disk drive was introduced. The disk drive provided greatly improved access times, and gradually began to take over as the primary storage medium. Tape drive and head manufacturers countered in the early '70s with the development of GCR (Group Coded Recording), which increased bit densities to 6250. Tape speeds also increased from 125 to 200 ips. GCR encoding produced no major structural advances in head technology, but demanded many refinements and redefinitions of precision (See "GCR Increases Data Recording Rates and Reliability," **Digital Design**, July 1981, pp. 34-39). For example, a head gap in the '50s could be 0.00025″ or larger, where the 6250 bpi read gap must be 0.00004″ ±0.000005″. Head to tape interface became extremely critical as tape speeds reached 200 ips. This meant further refinements in head contours. Since the introduction of GCR in the early '70s there have been no major advances in tape drive or head technology.

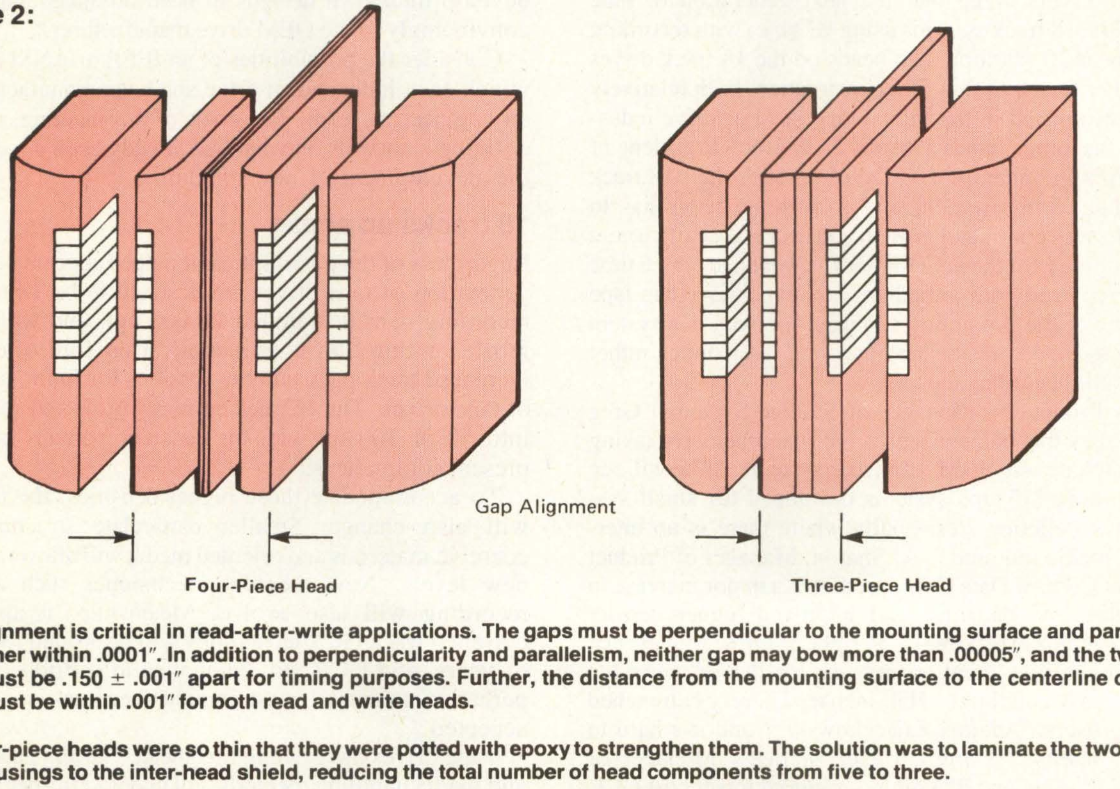
As Ray Freeman of Freeman Associates stated in an abstract he presented at an IEEE Workshop in June of this year, computer tape product technology advances essentially stopped in 1973. In the meantime, disk technology has continued an aggressive rate of improvement in performance and economy. The only evidence of technological advances has been in the area of contour refinement and experimentation with various hardcoat materials. These changes were initiated primarily by the head manufacturers, with each claiming his own particular method as best. However, changes have taken place in tape drives. There has been a trend toward size reduction and miniaturization.

disks boost tape sales

With the trend toward smaller business systems, large tape drives were no longer essential. Smaller drives were developed to fill that need. Cassette and cartridge tape drives were introduced at about the same time as disks began their predominance. They were used in the same function as ½″ drives, but for the separate, small system marketplace. Instead of 7 or 9 track heads on ½″ tape, the cassette and cartridge have developed their own track formats and use 0.150″ and 0.250″ tape widths. Recently, through advances in disk technology, the cassette, cartridge and ½″ drives have found themselves intimately involved with major computer applications. It is ironic that the same disk drive technology which almost drove tape drives to obsolescence has now brought about their resurgence.

The downward trend of tape drive use changed when the Winchester shot its way to the forefront of computer technology. The Winchester-type drives provide great advances in disk drive storage, but due to rigid tolerances and cleanliness requirements the disks themselves cannot be removed. Once the disk is full, the drive is useless unless the data can be transferred rapidly and economically to another media freeing the disk for more data. Streaming tape drives have

Figure 2:



Gap alignment is critical in read-after-write applications. The gaps must be perpendicular to the mounting surface and parallel to each other within .0001″. In addition to perpendicularity and parallelism, neither gap may bow more than .00005″, and the two gap lines must be .150 ± .001″ apart for timing purposes. Further, the distance from the mounting surface to the centerline of each track must be within .001″ for both read and write heads.

The four-piece heads were so thin that they were potted with epoxy to strengthen them. The solution was to laminate the two return core housings to the inter-head shield, reducing the total number of head components from five to three.

It becomes evident that machining, grinding, lapping, assembly, and alignment is not only far more accurate, but significantly easier in the three-piece head. It also allows disassembly for rebuilding, making it recoverable and providing the user with possibly two or more additional performance periods during the overall lifetime.

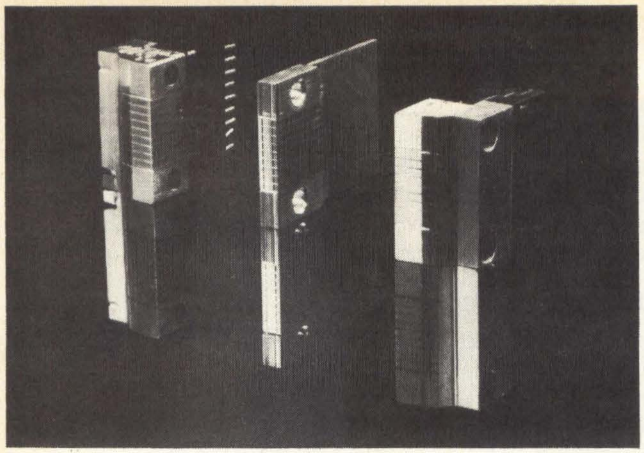


Figure 3: Three piece head, disassembled.

been developed for this purpose and include a niche for cassette, cartridge, and ½" drives. The streaming drives do not introduce new technology. In fact, they are in some ways evolutionary throwbacks, simply combining refinements of earlier technologies and current PE and GCR recording densities.

IBM compatibility mandatory

What then does the future hold for tape drives and the heart of the drive, the tape head? The industry is waiting for IBM to announce its next generation of tape drives. No one knows for sure, but it seems the announcement will be forthcoming sometime in early 1982. It's sometimes frustrating that an entire industry must wait for IBM. No one, apparently wants to produce a product that will not be IBM compatible. Compatibility and interchangeability have become mandatory for users and manufacturers around the world.

Most observers agree that the next generation of tape drives will be 18 track systems using ½" tape, with recording densities near 20,000 bpi. The heads on the 18 track drives will be either ferrite or thin film construction, both relatively unknown or untried in the digital tape head or drive industries. On the other hand, Donald J. Wilson, President of Telex Corp's Peripheral/OEM Division, feels the "18 track is not a huge improvement and something better has to come." He sees continued growth and acceptance of current GCR technology for the next four or five years, at which time it will be replaced with a medium less expensive than tape drives. One of the possibilities Wilson foresees is a system similar to the video disk, perhaps using laser optics rather than magnetic recording technology.

Wang's Production Manager of Storage Systems, Greg Pelletier, sees the independent drive manufacturers taking years to catch up with IBM's 18 track systems. "We will see more and more ¼" tape systems developed for small systems," says Pelletier, "especially where there is no interchange of media required." Al Sharon, Manager of Product Planning at Control Data Corp, predicts "a major increase in ¼" cartridge, ½" cartridge and improved higher density media." Joseph Zajaczkowski, Peripheral OEM Manager of Sperry Univac sees great advantages for the ½" cartridge because of easy handling. "Half inch tape is very entrenched by the big users," claims Zajaczkowski, "and it's hard to break old habits." Darrell Meyer, Pertec's Manager of Product Marketing and Planning, sees more lower cost GCR drives. However, their role will go from "active to passive moving more and more into a form of backup and offline storage." In Meyer's opinion, tape drives will be around for many years just as punch cards have been.

current media nears limit

Most industry observers feel that tape is still a highly economical, easy to store, and easily transported media which will continue in popularity for at least the foreseeable future. This foreseeable future may also be one of evolutionary transition. "Current iron oxide tape media is near its maximum capability for density," states Lewis Frauenfelder, Vice President of Tape Engineering at Storage Technology Corp. "New media will have a new particulate base and will be capable of greater than 25,000 bpi recording."

"Since at first, the new tape subsystems will be used for dump/restore type functions, the migration to these will be evolutionary," Frauenfelder adds. "As iron oxide tape wears out, users will replace it with the new particulate media and will also replace current technology drives with the new particulate capable drives."

In the evolutionary process, was higher density 9 track technology overlooked? Higher density 9-track technology is available, and rumor has it that a large drive manufacturer was planning to announce it, but pulled back to wait for IBM. No one today wants to be a pioneer and be incompatible with IBM in the future. Most agree that higher density 9 track would only be an interim step which should not be taken since IBM's 18 track appears to be close at hand. Whether or not we like it, IBM is our de facto standards-setter.

Head manufacturers must stay abreast of new trends and flex as technology changes. The independent head manufacturer is in no position to dictate bit density, track pack, speed, configuration, or initiate new trends in technology. Yet, according to Frank Chiaverini, President of Alternatives in Magnetics, Inc., "the independent head manufacturer may be in the best position today to innovate, create, and implement that which is necessary to breathe new life into the tape drive industry. Tape head manufacturers may have to develop their own designs in head products and sell them convincingly to the OEM drive manufacturer."

Consider the possibilities of an IEEE or ANSI meeting to which each independent drive and head manufacturer sends an engineering team. The goals of this meeting, rather than defining standards on what had already been done, could be the development of new standards.

18 tracks up ahead

Regardless of the possibilities, it indeed appears that the next generation of tape drives are destined to be 18 track, with recording densities around 20,000 bpi, and with heads of ferrite or thin-film construction. Thin film offers greatly increased track pack and bit densities for future generations of tape drives. The 18 track currently projected could evolve into 50 or 100 tpi with bit densities perhaps beyond our present comprehension.

To accommodate those higher densities, the tape media will also change. Smaller particulate structure, higher coercive materials and oriented media will allow recording at new levels. New recording techniques such as vertical recording will also evolve. Meanwhile, it appears that current 9 track GCR technology will be around for a number of years, and GCR will be applied to cartridge drives and perhaps cassettes as streaming becomes more widely accepted.

Tape drives have a long life ahead. Current heads, media, and media handling methods will undergo further refinement through the evolution of streaming drives. And finally, we will soon see the first new technological advances in almost a decade, with promise of a strong future for both tape drives and tape heads.

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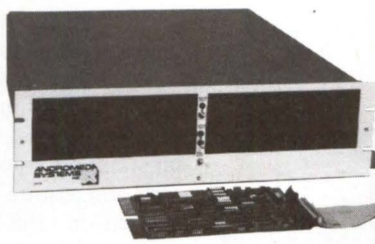

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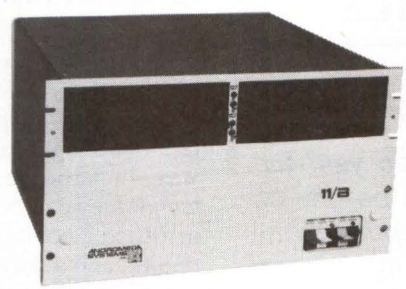

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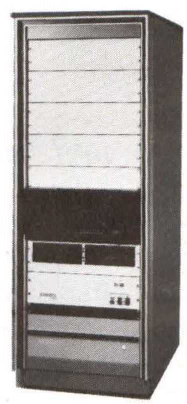

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Matrix Printers

increased emphasis is on applications-oriented output and graphics

Just as 1981 has been a dramatic year for matrix printers, 1982 promises to be one of continued rapid evolution. This is due primarily to an overall industry demand for more information handling capacity at less cost, and the burgeoning need for more intensive, applications-oriented output. Clearly, matrix printer technology will continue to play a major role in the ever-expanding application of information systems, from the μP to the 32-bit superminis.

by Peter M. Craig and Edward Winslow

While each of the various categories of matrix printers has unique competitive and technological features, a number of common attributes are stimulating growth in all categories.

Of these virtues, reliability is premier, for as more and more business functions become dependent on micro/minicomputer systems, it naturally follows that simplicity and durability assume major proportions as selection criteria. Matrix printers, whether serial or line devices, incorporate substantially fewer moving parts than their full-font counterparts and require significantly fewer service adjustments. For this reason, 1982 will find more matrix printers of all categories employed on a wide range of systems.

versatile output

Next to durability and ruggedness, the inherent versatility of matrix technology is an extremely significant factor in its continued acceptance. It, in itself, is literally an expansion force in systems application since it allows output forms to be tailored to application requirements in a virtually unlimited way. In particular, application utilization of matrix printing technology can be expected to mount dramatically in 1982, in office automation/near-letter-quality output, in graphics output, and in color hard copy. Let's briefly examine each.

Office automation/near-letter-quality output applications are the result of advances in matrix print quality. These refinements occur through more accurate, more repeatable dot placement, multiple-pass head technology, incremental dot positioning, and improved paper handling characteristics for precise paper registration. While it would be imprudent to suggest that matrix printers will supplant daisy wheel devices as the mainstream word processing printer, there is an extremely broad domain of business applications for which the forthcoming 1982 print quality levels of matrix printers will be more than a match. These include high-volume internal correspondence, bulk text documents, and draft reports. In particular, on smaller systems, the versatility of matrix printers allows multi-function application using a single output device. The consequential economic benefits are expected to attract more and more users to matrix printers as alternatives to many full-font devices.

The second key versatility benefit is the output potential of graphics — not only for data representation, but for special symbology such as bar codes and OCR labels, attention emphasis, pictorial imaging, and forms generation. Graphics output is a most significant factor, because it transcends the constraints of fixed-font printers, and it allows information to be portrayed in the most easily assimilated form appropriate to the application.

Peter M. Craig, Product Marketing Manager, and Edward Winslow are with Printronix, Box 19559, Irvine, CA 92713.

In 1982, practically every major printer vendor will offer equipment with some form of graphics capability, and the use of μP imbedded intelligence will make it even easier to implement graphics applications.

The third versatility benefit of matrix technology is color hard copy. Matrix technology vendors have been on the fringes of color output for about two years, with product offerings by IBM, Trilog and a few others. Color output has also become a major issue for graphic CRTs and for low-end micro-based systems of the Apple class.

The use of color in hard copy output greatly enhances the information content by providing category differentiation and attention emphasis. Matrix printing technology is extremely well suited to color output since the combination of three primary hues can create literally a "full" color spectrum similar to television technology.

A number of major vendors have had experimental development projects for some time. In 1982 there is a substantial possibility that major new product offerings will come forth with full color output.

economic value

The final universal growth attribute for matrix printers is economic value — due not only to versatility and reliability, but also to competitive pricing.

Continued downward price pressure is likely in 1982 for medium-speed as well as potentially high-speed serial devices. This will be similar to the competitive price erosion that occurred in 1981 in the low-speed printer market, where the unit price dropped to below $500, with no sacrifice in product integrity. The impact of this value clearly pushes matrix technology into the forefront of hard copy output techniques.

four basic categories

With these aggregate issues underlying all matrix printer categories, let's turn to each specific area.

Matrix printer devices can be divided into four basic categories:

Low-speed serial printer (100 cps and under)

Medium-speed serial printers (less than 200 cps, but above 100 cps)

High-speed serial printers (faster than 200 cps)

Matrix line printers (100 to 600 1pm)

Low-speed serial printers experienced major price erosion in 1981. Led by Shinshu Seiko's Epson MX devices, the under-$1000 printer of 1980 became the under-$500 printer barely 12 months later. Judging from Epson's success in landing major OEM contracts at IBM and Philips Datasystems, quality has not been seriously compromised by the price cutting, if at all. Consequently, Epson has established a de facto standard in quality and value that continues to characterize this segment. The ability of Centronics, Integral Data, Anadex, Okidata, and others to follow the Epson lead will be the question of 1982. This segment will most likely witness continued aggressive competition, with weaker products and companies falling out.

Medium-speed serial printers, operating in the 100- to 200-cps range, and priced between $1000 and $2000 (to the end user), are the domain of Texas Instruments' 810 series, Centronics' 700, Dataroyal, Mannesmann-Tally, and numerous other suppliers. This segment attracted many new participants in 1981, ranging from divisions of large companies to small enterprise startups, plus not just a few Japanese offerings. These products are undergoing design changes to reach both the graphics and the high-print-quality applications discussed above. It can be expected that vigorous price competition will force prices downward for these products, probably led by Japanese offerings. Prospective buyers of medium-speed units will need to closely examine vendors as well as their products, since the increased competition can be expected to create a shakeout.

High-speed serial printers, i.e., those operating above 200 cps, generally priced above $2000, are presently paced by the Florida Data OSP model, which provides both data and word processing print quality. Offering the highest in serial matrix print speeds, it is also the highest priced, with an announced list price just under $4000. Other vendors are Dataproducts, Tally, Anadex, and Malibu.

All of these units are substantially more rugged than their lower-speed counterparts and offer throughput capacities similar to the low-speed line printers with which they will compete. In 1982, more entrants will offer high-speed units and, again, significant price competition will occur. These downward price pressures, however, are not expected to be as severe in the medium-speed market.

Matrix line printers deliver both durability and workhorse performance. While the low-end models have throughput comparable to the high-speed serials, these devices offer substantially higher sustainable duty cycles due to fundamentals of construction and physics. In traditional line printer designs, employing machined castings rather than sheet metal frames, the impact elements are arranged across the page and disperse their living energy into a much larger volume than with a multi-wire serial print head. Consequently, heat buildup in the firing element can be managed much more effectively, and long life can be designed into the mechanism.

Matrix line printer speeds extend upwards to 600 lpm and offer print quality that is superior to other full-font line printing technology at competitive prices. New domestic suppliers are not expected to enter the matrix line printer market in 1982 because of the intensive engineering involved; however, a number of firms, including several Japanese companies, are known to be conducting development programs. Matrix line printers, of course, have all the application versatility of their serial counterparts and represent outstanding value for all ranges of minicomputer and μC systems.

1982 trends

To summarize, the major trends for 1982 in matrix printing should be:

- Increased emphasis on applications-oriented output, and graphics in particular
- Increased functional intelligence within printers, making them easier to use
- Increased price competition in medium- and high-speed serial units, probably led by Japanese vendors
- Direct competition between high-speed serial units and low-speed line printers, with the pricing edge going to the serials and with high-duty-cycle durability on the side of the matrix line printers
- Increased office use of matrix printers for noncorrespondence applications and within small firms for many routine output uses

Most important in 1982 will be the general recognition that to use matrix printer technology only as an alphanumeric printer is an unnecessary restraint on a versatile and flexible output device.

Current and Future Problems Face Digital Displays

flicker and inadequate standards are just two of the difficulties that today encumber this human/computer interface

Among the many problems still to be overcome in producing trouble-free digital display systems is "flicker." At a recent Society of Information Display meeting in New York, an evening panel discussed potential health hazards of CRT terminals. Unfortunately, major emphasis was on microwave radiation. Although several experts in the audience brought up "flicker," no panel members would acknowledge such a problem existed. In fact, several panel members seemed unaware of flicker problems in digital DVTs!

by J. M. Heines

Clearly, flicker research is inadequate to date. Data bank surveys by myself and others prove that only 5 or 6 pertinent documents exist on the subject. This was also confirmed in a paper by John M. Booth and Richard J. Farrell on "An Overview of Human Engineering Considerations for Electro-Optical Displays" presented at the S.P.I.E. Conference at San Diego in August, 1980. Most flicker research was done in 1965/1966, with some attempts of higher levels of interlace later, which did not work out.

Turnage of General Dynamic, as published in SID 1966 in his classic paper, did extensive flicker studies and identified the problem of intensity modulations effects and refresh rates, with the problem of line-to-line or spot-to-spot brightness ratios occurring typically on a raster, interlaced display. Deutsch in an IEEE paper on Transactions BC-11 in 1965 already identified the digital dot or pixel or pel flicker problem, which he called "scintillation effect," now so visible on color monitors used as digital −N or symbol units. He further found that there was a jizzle snow flake phenomenon, a modulation effect of the scintillating dots, and he reported that snowflaking was very annoying to the eye.

In the analog (home TV, 525 lines 2:1 interlace) situation, TV lines are overscanned (see **Figure 1**) and the video pictures are pattern (thus intensity) correlated. This is not the case in digital TV whereby each pel or pixel or dot is presented uncorrelated to the rest of the scene; and, as such, close to the full 100% modulations index is present, requiring a refresh rate for P-31, P-4 (black/white TV) and P-22 (color) phosphors of about 45-48Hz.

There is no display engineering escape from this problem, in spite of the various hocus pocus schemes presented in the last decade and implemented over the last 10 years on digital raster displays. This has put us in today's predicament, with a market of $500-$600 million per year in digital terminals, but with many of them not properly designed.

The key issue is that while low-power and low-cost, high-speed resonant flyback raster displays came out of the communications sector, more conventional display designers concentrated on random-drive strobe displays which were severely bandwidth-limited in deflection (and thus restricted in data display). With their small sales base, they became and remain very expensive. Several DOD programs now look at the $1,000,000 display console, a real disappointment for program managers, caused by a lack of competitive procurement.

analog standards inadequate

In the early seventies, several companies started to use raster in display technologies, and established the basic technological premises on how to do this with digital computers driving the units. It soon became clear that the analog raster TV with its 2:1 interlace was a poor approach, in spite of the

J. M. Heines is Staff Engineer for Raytheon's Submarine Signal Division, PO Box 360, Portsmouth, RI 02871.


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525-line raster; only about 250-pixels-by-240-lines could be presented, or only 60,000 data points, which is rather inadequate for the spot sizes, CRTs and 16- and 32-bit μPs available. The RS-170 spec, however, had an associated high-resolution display technique spec, RS-343; but very few monitors were available to this spec, and costs for these monitors were very high.

By using the RS-343, 875-line raster and driving it noninterlaced and at a slightly modified line rate, we produced the 512 × 512 pel line matrix successfully for several programs. But in the end, when demands for more data on the tube persisted, we developed our own raster monitors with video bandwidth (4-bit level) of 30-40 MHz and resolutions of 600-700 pixels with 700-800 lines in a noninterlaced fashion (Raytheon's SC-80 display for example).

In a few cases where analog TV-like pictures were needed in correlated data waterfall displays for radar, sonar and IR/LLLTV, interlace was used, but highly selectively, with specially designed phosphors. When personal computers coupled to TV monitors came, we were in trouble: coupling a μP with a 525-line TV monitor invites problems. To add further insult, the shadow mask color triad was even worse, especially when used in single colors, creating a high modulation level.

Lack of proper digital TV standards is the biggest problem, as the industry has been struggling along with the EIA analog RS-170, RS-343 specs for the home TV systems. Only recently in England an agreement was worked out for a new digital raster standard whereby the representatives of SMPTE (not SID, EIA of SPIE!) from the USA agreed with the European representatives to decide on better-suited line resolutions.

With satellite wide-bandwidth communications systems now entering business in the US, and teleconferencing proven to be cost effective and less time consuming, high-resolution EIA TV standards and digital standards must be developed. With 1,000-line monitors now available at low cost and video amplifiers which can run at 200 MHz, there is no need to struggle with 4.5-MHz data rates; computers can run at 20-50 MHz, and video disk technologies have been shown to be able to handle 150 Mbits per second. In addition, fiber optics will increasingly replace copper and coax and become a major pressure in communications bandwidth improvements.

vision vs. video display

The human eye, with its 22-27 million receptors (shown in recent research) handles 100-200 Mbits per second in certain cases and has a 10^{15}-bits storage capacity (equivalent to 10,000 optical video disks). This enormously powerful

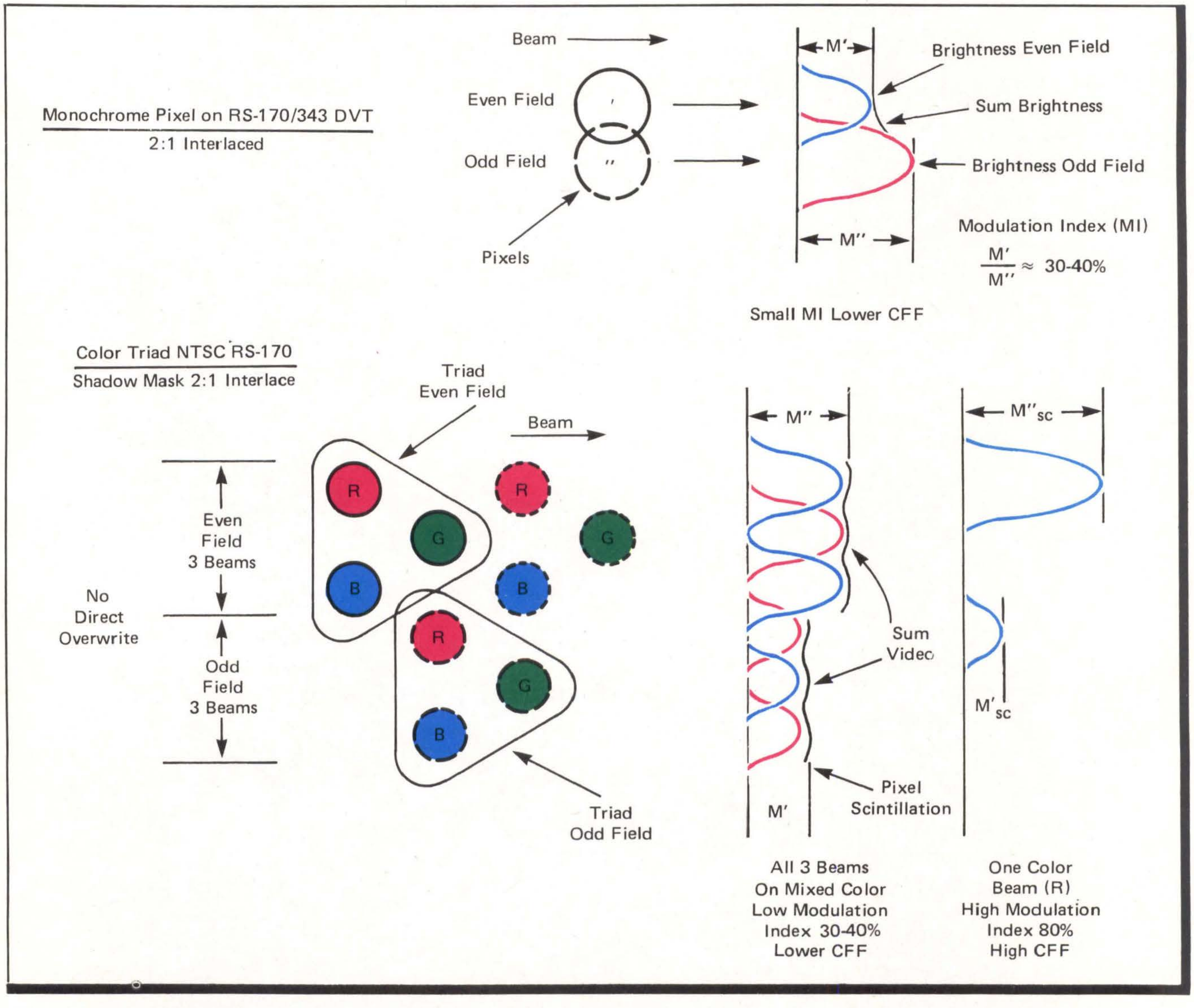

Figure 1: Multicolor, single color and monochrome modulation index situations.

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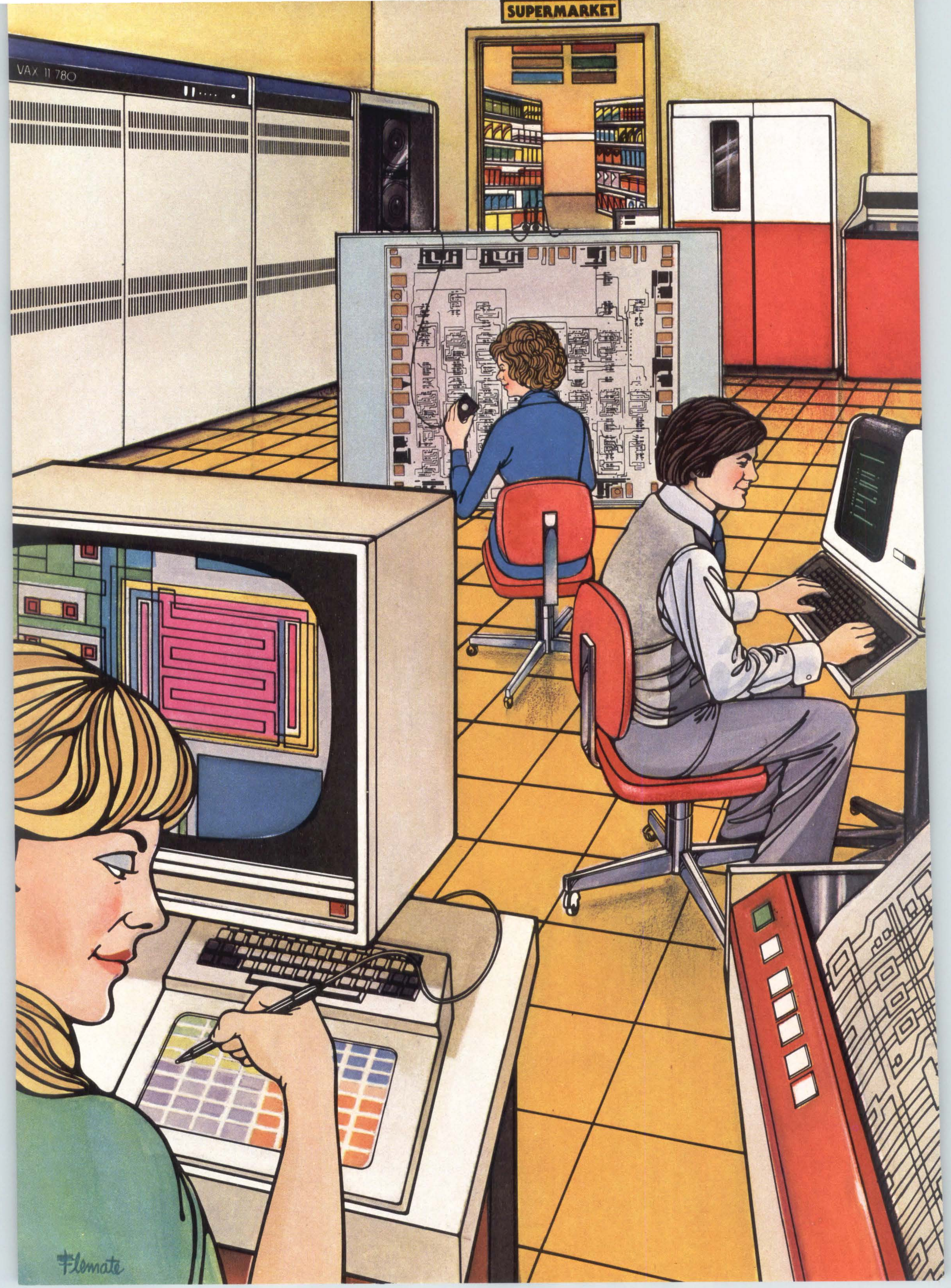
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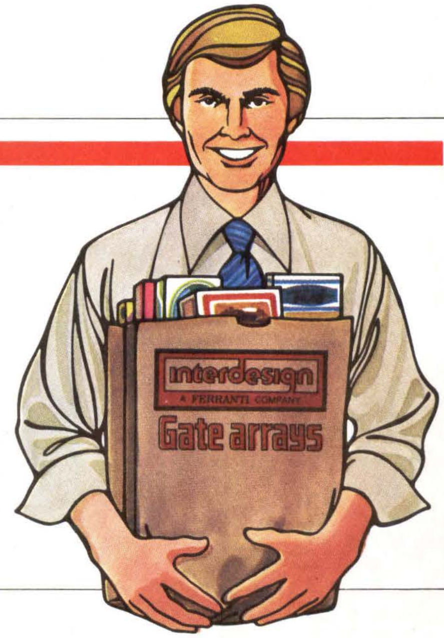

human computer needs better matching to display processors. All this does not come for free: major R&D investments are required. With new display technologies using VLSI and VHSI technology-implementable stereo-vision TV, 3-D TV using either holography interferometer patterns or pseudo-3-D perspective techniques with the fast-developing solid state panel technologies will be available within a few years. While little work is done in US R&D labs, the Japanese and Europeans are working furiously.

Let us review the ideal display field for the operator. While no official US industrial standard exists for display operator interface — in spite of millions spent on human engineering research — a good standard to use as a guideline is MIL-STD-1472. This has given the military excellent operator display interaction and allowed our aircraft cockpits to be the best in the world (with the new Boeing 757 and 767s probably the edge-of-technology).

The human eye can resolve, on the average, 1′ of arc, so that at a typical DVT 18″ viewing distance, a 5-mil visual resolution can be achieved in the brain. The eye is a scanning device with a 2″-3″ elliptical focal vision area and a 180-190° total peripheral and has a typical 30° "preferred" low dynamic fatigue viewing-cone with an angle of 30°. A 30° angle at 18″, therefore, requires a display face of about 9-10″; the 10″ square CRT display-face on the 15″ tube is now in the military industry an "agreed upon" standard.

Since, often due to background/foreground as well as command/menu and data display processing, two simultaneous display eyes are needed, the lower data face is placed at the 30° eye rest depression angle axis and the command and control face at the zero-angle eye-rest axis. However, DVTs are usually alphanumerically command-type-oriented; and, using TV-type CRTs (3/4 ratio), a 16″ or 17″ tube is acceptable.

If we now match eye resolution to pixel or pel resolution, we see that a 10″ square display should have 2000 pels-per-line, and a line width (1/2 brightness point) of 5 mils to a total of 2000 lines or, in digital terms, a 2048 by 2048 or 11×11 matrix. Larger screens at closer ranges have caused excessive eye movements (especially on moving platforms) creating vertigo effects due to inner ear balance system interaction with visual systems: the 30° angle is an important limit for low-stress, low fatigue environments for the operator.

We built 19″ displays for sonar use, but received complaints from the operators. More notably, several highly-skilled crews during the failed hostage rescue attempt in Iran were flying on the terrain-avoidance displays whereby radar, IR/LLLTV data and other navigational sensors are displayed on several displays. The crews suffered severe vertigo effects, which combined with sand storm turbulence, and forced some of them to return to the carrier — a classic case of motion effects overriding human capabilities.

film slide quality

Having established the ideal film slide quality display of 11×11 bits, we now calculate the display parameters behind this unit. Since the display has to be flicker-free to avoid operator visual fatique and annoyance, the proven refresh rate of 50 Hz is needed, which gives 20 msec/frame. Assuming a vertical beam reset (flyback) of 20 lines to settle the beam properly for the next frame, and a line flyback time of 7 μs (most standard commercial TV monitors take 10 μs to reset line by line) we find that the line rate (r) must be $2000r + 2000 \times 7 = 20{,}000 - 20r$, or the active line time

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AYDIN CONTROLS

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would be about 2.9μs. This is much too low, as it requires a beam writing rate of 3.45 in./μs, which is much too high; and, a video pel rate of 2900:2000 = 1.45μs or about 700 MHz is required, also. This is technologically unachievable even several years in the future.

The first thing is to decrease the RS-343 line flyback rates of 7 μs. This has been done in several designs and a rate of 3 μs per line was achieved using special flyback transformers and circuitry other than standard TV techniques. An active line time of about 6.9 μs and video rate of about 3.5 μs or about 300 MHz video bandwidth as a minimum is needed. This is now possible in the realm of display technology, and such monitors could be available with deflection rates of 1.4-1.5 in./μs, but will need further improvement in coil design and use of high voltage power supplies. It is obvious that the 11 × 11-bit design, fully flicker-free and film-slide quality monitor would be rather expensive and incompatible with low-cost μPs. In addition, it would probably be replaced in the mid-eighties by solid state display panels.

The question is this: how far do we ease off in resolution? The home TV 2:1 interlace only allows 250 × 250 (8 × 8 bit). With a 5 × 7 dot matrix character or 7 × 9 character matrix area, it allows only about 35 characters/line with 28 lines of character or about 1000 characters per frame to be displayed, flicker free. Any attempt to increase this deteriorates character set quality. With bandwidth increase, more characters/line can be achieved — but the vertical line set for this resolution will stay the same. Lowering the refresh rate from 60 Hz to 50 or 40 Hz using P-39 phosphor will allow more data display; but, due to the afterflow after frame change and cursor tail smear effects, monitor quality will again suffer. Low refresh-rate phosphors also are less efficient in lumens/watt, need more power and higher beam current, and therefore suffer from a lower tube life.

Using the 875-line TV monitors, and using the 525-line noninterlaced line rates (together with wider-bandwidth video amplifiers), the 512 × 512 (9 × 9-bit) display can be used. This number is now being challenged by the new 512 × 512 plasma panels, which have limited data update rates (unlike TV) and can only get brightness/intensity changes by change of refresh rates at the cell level. This display approach allows a character display of 72 characters/line and 52 lines totalling a satisfactory 3600-3700 characters, and is utilized as such in limited cases. Again, however, price is a problem — not only for CRTs but also for the plasma panel, although the latest SID conference projected plasma panels below \$800/unit. This is about twice that of commercial 825-line TV monitors, but with power consumption about half of them.

The next level is the long-strived-for 1,000 × 1,000 pixel/lines display or the typical 10 × 10 bit raster device. In addressing capabilities, this has been available since the early seventies for the strobe displays, but not in data since these were and still are limited to about 4,000-5,000 vectors/frame. The alphanumerics on such a display would now use close to 16,000/frame (A/N go up with square of pel resolution). In practice, however, an operator frame limit of about 4,000 characters should be envisioned as an upper bound. If we again calculated the 1,000-pel flicker free display technology requirements, we find an active line time of about 16 μs/line with a reasonable 4-μs line flyback time, and a video rate of 16 ns or 66-MHz bit rate and equivalent video bandwidth of 150-160 MHz (sine wave response) for full grey scale display. Apart from the required writing rate of about 0.6″/μs, which is now state-of-the-art, the problem

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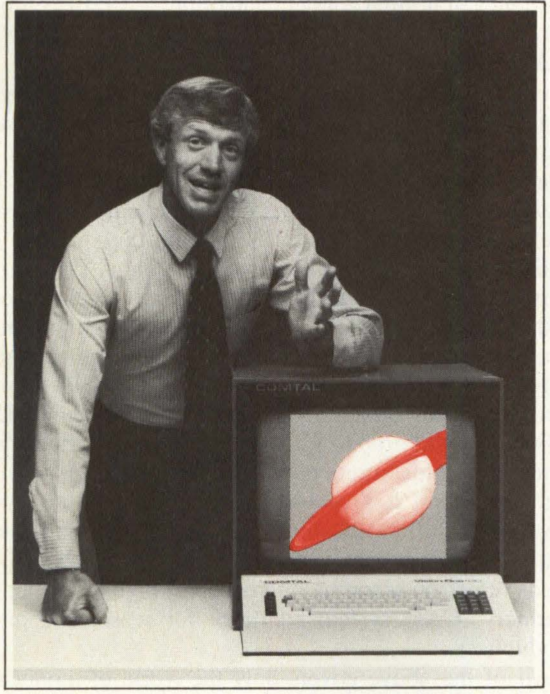

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of refreshing at this rate out of BIT image memories would require ECL ICs in the video buffers — at least until GaAs ICs become available, as well as flash-type D/A converters. Again, such a monitor will not be cheap, but those built for military consoles are now reasonable from military-equipment cost levels and are emerging rapidly.

We can, therefore, conclude that to obtain flicker-free DTVs, the standard TV monitor with 2:1 interlace should have dual-dot matrix characters; and, the 5 × 7-dot character is really a 5 × 14-matrix unit, which allows about 1,000 characters, or a graphics display of 250 × 240 pixels. In this case, the pels are due to interlace larger vertically than horizontally, unless the video pulsewidth is matched, producing basically two overlapping ellipses. To run the display as a single-line address will create flicker, as display refresh of each pel is 30 Hz, or 50% below the critical flicker frequency at normal ambient and brightness (20-25 ftlbt).

high resolution displays

A more expensive technique using RS-343, 875-line, 16-MHz TV monitor will allow (with larger bandwidth) a 525-line 550 pels non-interlaced display good for about 4000 characters (5 × 7) or about 3000 characters for the better quality 7 × 9-dot matrix character. The long-awaited 1000-line, non-interlaced display is now on the verge of being available and will be able to produce quality raster-graphic displays (and, when produced in quantity, at a reasonable cost). The RS-343 1029-line 2:1 interlaced monitors are now available at costs of about $1000. Telefunken (Germany), and US suppliers, were shown at the New York SID show. The non-interlaced version will probably cost about $5000-$6000, but will drop to $2,000-$2,500 when various display terminal manufacturers pick them up. Several experimental high-resolution 2000 × 1000 and 2000 × 1500 monitors are now being built for the Air Force and Intelligence Branches, but will be too expensive for merchants trade unless specific needs (electron scanning microscopes, high resolution CAT scanners, CAD systems) emerge for reasonable quantity productions.

All of the above covers only the world of monochrome displays; and, as can be seen, are technology-wise, except regarding price at the high end. In this area CRTs will certainly be challenged by the solid state display panels with LCD, LED and ELD technologies. Also, in the area of large screen displays, due to limitations of the projection tubes and physical size limit of CRTs, the future for solid state panels in this area looks good. This is true especially since several of these panels allow epitaxial growth, have high lumens per watt output, long life, do not need refresh, and require low power.

The color situation for DVTs however is in poor shape due to the high, high-voltage requirements of shadow mask tubes (18-22KV). There's also some controversy that its radiation levels are harmful (see **NY Times** 12 May '81). But the key issue is the flicker problem again. Specifically, the shadow mask tube both for delta and linear 3-gun arrangements has a serious modulation index problem; this is quite serious and has created a rash of customer problems. Operator walkouts occurred in California.

Flicker frequency on refreshed CRTs is very complex. Critical Fusion Frequency (CFF, the frequency at which flicker will or can be seen) is dependent on beam brightness level (higher brightness — higher critical flicker rate), the phosphor type or composition used both in fluorescence and phosphorescence (as was the case in P7: the initial blue flash created, in spite of being a slow phosphor, a very high CFF), and the modulation index (Turnage, 1966) which is the ratio of brightness for each field of adjacent pixels, vectors or other polygon areas (**Figure 1**). This latter is quite perceptible as we look at a strobe or flickering lights and occurs because the eye/brain connect has several resonant frequencies. As used by the medical profession for EEG-brain damage surveys, cases of flicker-frequency-induced epilepsy by using strobe lights are well-known, and high-level strobe light techniques can introduce rapid unconsciousness. Those who drive a tree-lined road at sunset with the sun flickering know well the rapid discomfort of this, and will select a speed of tree-induced modulation flicker away from the critical frequencies.

The modulation index at 100% is equal to the usually quoted critical flicker frequency. At lower modulation ratios, it could drop 25-30% which allows, due to the Knell, overscan vertical raster compression on home TV, a relative flicker-free display at 30-Hz frame rate with a 60-Hz field rate for P-4 phosphors. However, the half line edges do flicker. In digital display, pel or pixel flicker at 30 Hz is called *scintillation*; an effect of brightness field modulation is called *snowflaking; beat flicker* is where there is cross-modulation difference for frequency between the ambient lighting and refresh rates. The classic example of beat flicker is the film taking of DVTs and TV sets where, with the $2 \times 24 = 48$ film frame rate looking at a 60-Hz TV picture, beat flicker of 12 Hz is seen. A proper TV video camera should run therefore at frame/field rate to obtain stable pictures.

So what happens in color for a typical 3-gun shadow mask color tube if one does not interlace data by pattern coherence? **Figure 1** shows the typical kernel triad NTSC pattern whereby all 3 beams light up the 3 triad pixels on the tube. As can be seen, there is a coherence of modulation. If, however, the display is run digitally by one field at 30 Hz and at a specific color, the modulation index is now close to 100%; and the pixel will flicker in a severe manner, causing the operator to experience phenomenon called red or green dream problems.

This problem is clearly visible in several computer monitors I have seen. At 80-90% modulation levels, color DVTs running at a specific color will flicker at 47 Hz. By using a circular polarized filter in low brightness, this might be reduced to 40-42 Hz, but the 30-Hz frame refresh level at which the digital field runs will create extensive dot scintillation flicker. In fact, there is no known research published on digital interlaced and non-interlaced "color mask" flicker studies at present. As I have stated on many occasions, the only way out is a non-interlaced technique at 50 Hz which will give, due to the slot or triads, still smeary but acceptable flicker-free characters. Again, an 875-line color monitor running at 50 Hz non-interlaced frame rate will give reasonable performance.

Loral recently designed a two-gun color penetron which uses separate anode level settings for each gun, and works very effectively. By extending this to three guns, a truly three-color penetration tube could be developed to allow proper high resolution and high data-density color displays, rather than today's shadow mask tubes (which are not very good for close up view). It further allows mixed raster and random mode in each color simultaneously (SID 1981).

Hopefully, solid state display panel technology R&D — now only pushed by a few companies under the Army's supervision (ERADCOM people) and some lukewarm industrial support — will increase appreciably in today's political and technological climate. D

Disassembling The 6800/6802

higher channel capacity logic analyzers meet new demands

Disassembling or converting CPU signals back into listings of instructions in their mnemonic format is a powerful, popular procedure for testing computers. It has limits, particularly if data bus signals are not identified as opcodes, as with the MC6800/6802. And, to store the signals during disassembly, buffer circuitry is needed, plus a clock frequency range that ensures timing of data at the time of their validity.

Logic analyzers with sufficient channel capacity are appropriate storage devices. These channels (32 or 40 on some) are enough for most 8-bit CPUs, which require 24 channels (16 for addresses and 8 for data) and sufficient additional channels for control of the subsequent disassembly process.

by Edmund Breuer

If a logic analyzer is used for disassembling, input channels must be adapted to the precise CPU pin-out with the personality probe. Such personality probes guarantee that all required information will be accepted when valid and transmitted to the logic analyzer.

The problem of identifying processor opcodes is difficult and requires special debugging techniques and specialized circuitry that makes the personality probe operate properly in the disassembler mode.

the conventional technique

To identify opcodes, the technique used in personality probes incorporating disassembler circuitry is to halt the CPU at the end of each instruction using a HALT signal. This status is recognized with BA (bus available) activated. If HALT is then deactivated, the CPU resumes normal program activities after BA is reset. The first byte to appear on the data bus is an opcode. Thus, sampling the BA state controls the entire disassembling process.

This straightforward technique is often employed in personality probes for 8080, 8085 and Z80 processors, where disassembly into mnemonics is desired. A significant disadvantage of this approach — especially when used with processors such as the 6800/6802 which do not deliver any information on how the bus signals relate to certain data types such as opcodes, data accepted or delivered — is that each instruction execution is prolonged by two clock cycles.

Thus, real time processing is impossible. Additional problems are introduced using the WAIT instruction. WAIT also activates BA, contrary to statements made earlier. In this case, only part of the interrupt vector is read after resetting BA by the CPU, but not an opcode.

cycle count method

It is necessary to mark each reading cycle of an opcode in real time. Once identified, the number of clock cycles required by the CPU (to proceed with the program sequence) can be securely decoded. By counting these cycles, it is simple to find the subsequent opcode, which, in turn, can be decoded. Still remaining, however, is how to securely find that first opcode.

With the MC6800, the most direct way is to use the processor's own INTERRUPT and/or RESET procedures. These activities load a vector from a fixed address. If one of these is addressed, an opcode, delayed by two clock cycles, appears on the data bus. From this opcode, the number of cycles required by the CPU can be determined.

Circuitry required to allow a 6800 personality probe to operate properly in the disassembler mode is shown in **Figure 2**.

All outgoing lines from the CPU are fed into an input buffer block to lower the load at each pin. One LS-TTL load

Edmund Breuer is an Application Engineer for Dolch Logic Instruments, GMBH Dietzenbach, West Germany.

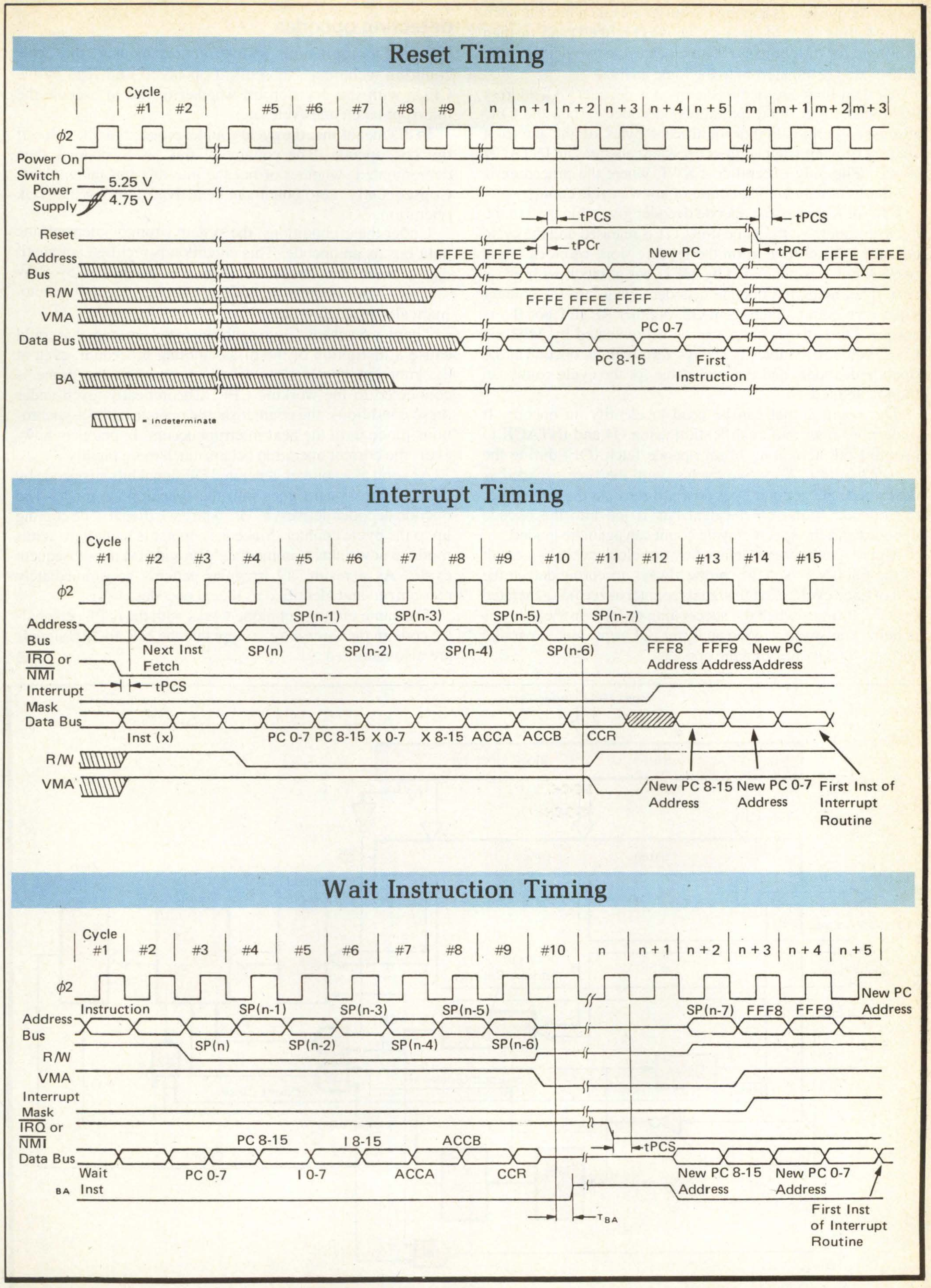

Figure 1: Reset, interrupt and wait instruction timing diagrams. Midrange waveform indicates high impedance state.

is specified. Signals leaving the buffer are taken into the latch on the falling slope of clock cycle two **(Figure 1)** and are then available for further uses. With clock cycle two delayed, the latch status is transferred to the logic analyzer.

All data lines are tied to the opcode decoder. All address lines lead to an interrupt address decoder. When the CPU addresses certain higher significant bytes of the interrupt vectors, the interrupt address decoder generates an INTACK signal. The only exception is SWI, where the procedure is similar to having an instruction of known cycle count.

INTACK makes the opcode decoder give a binary 2 to the cycle counter. At the same time, G1 is released and the cycle counter is reset to zero on the leading slope of clock phase two. A pulse is generated by MF1, out of clock with phase two. This loads the opcode decoder signal into the counter via a zero count signal from G2. Neither RESET nor BA is active. Thus, the counter can be decremented by MF2 via G3. The cycle counter is always zero with an opcode at the opcode decoder, and the new value for the cycle count can then be loaded.

The count signal can be used to identify an opcode. It undergoes a second qualification using G4 and INTACK to prohibit the activating of an opcode fetch (OF) during the vector loading. After two cycles, with the vector loaded as described, the counter goes down to zero. At the same time, the opcode found on the data bus is fed into the opcode decoder and the specific cycle count can again be loaded.

Signal evaluation is delayed by one clock cycle — a result of the 6800's personality probe always accepting data at the end of each cycle. An OF signal (counter at zero) is generated exactly at times when the succeeding opcode on the data bus is being transmitted to the analyzer. OF is present in parallel format, thus identifying the opcode.

detecting opcodes

If during a program run an interrupt occurs using this cycle counting technique, subsequent opcode is still read by the CPU, with the decision on whether or not to execute the interrupt taken one cycle later.

In the meantime, the cycle counter proceeds to the value of the last opcode. The content of this last opcode is then decremented, whether or not the interrupt has taken place. Consequently, zero count can be activated during the stack operation.

Under these conditions, the system wrongly interrupts the data bus as an opcode. This condition is rectified automatically, since the illegal OF flags are recognized by R/W signals. After reading the interrupt vector, the system automatically resynchronizes.

There is no chance of irregularity in the program that could cause a disruption of the disassembling procedure, even at the moment power is switched on or when the probe is connected to the working CPU. Theoretically, even under these conditions, the counter should operate in the asynchronous mode until the next interrupt occurs. In practice, however, the correct operation occurs much more rapidly.

As soon as a counter generated OF signal hits an opcode by chance, the system goes into the synchronous mode. The opcode decoder delivers a "1" with each illegal code coming up to the cycle counter. Since the counter is in the zero status mode, a new value is immediately provided in the subsequent cycle. As a result, all irregular patterns are immediately recognized and identified as illegal opcodes.

The same circuit technique works with the 6802 personality code in the same way, except that the MR and RE signals are also recorded.

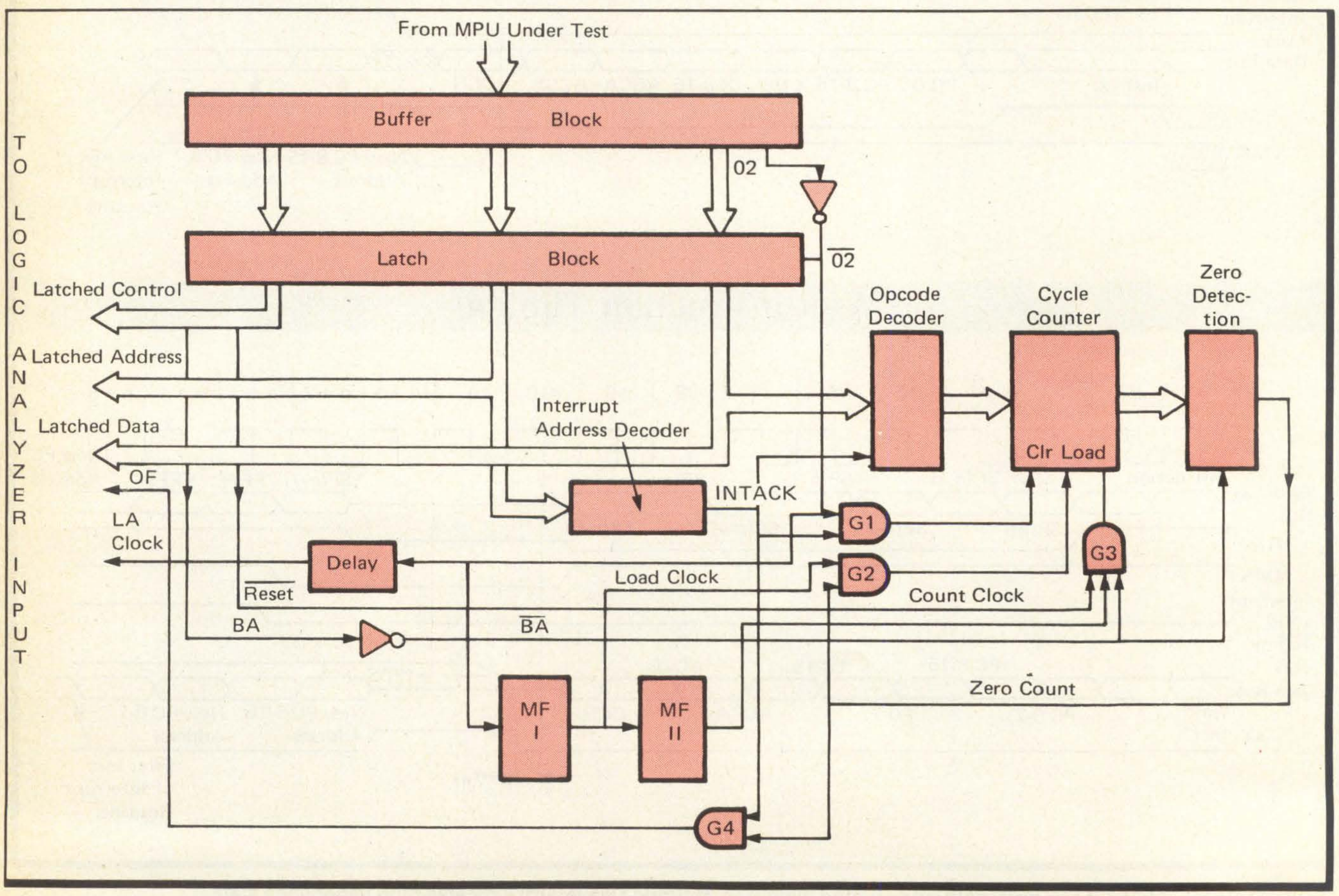

Figure 2: Circuitry enables 6800 personality probe to operate properly in the disassembler mode.

Keyboards Continue Evolving

despite challenges from other input devices, keyboards will remain on top

Keyboards are undergoing major changes due to cost pressures, modularity trends and ergonomic considerations. Keyboard designs remain custom and unique to every terminal and computer product, but certain functional characteristics have become common to most applications.

by Mark E. Tiddens

The most popular method of entering data into a system is via a full-travel keyboard (full-travel defined as 0.150″ or greater). It might appear that other data entry devices such as micromotion keyboards, (less than 0.150″ travel), flat panel keyboards (no travel), OCR (Optical Character Recognition), voice data entry, and hand print data entry could decrease the use of full-travel keyboards for data entry. However, for most data entry applications where full-travel keyboards are currently being used, these other devices are not as efficient. These newer data entry methods are enhancing existing data entry applications and finding new applications, rather than replacing full-travel keyboards.

If increasing the efficiency of data entry was truly a major objective in exploring the use of other data entry devices, a major effort would be put into using an improved keyboard layout. The conventional Q W E R T Y layout was originally designed to slow data entry so an operator could not exceed the capability of the old keyboard designs. Proponents of the Dvorak simplified keyboard, for example, which merely rearranges the keys, say that an operator could produce the same output for 5% of the effort.

Keyboards will remain the most popular form of data entry since increased efficiency is not obtained in most data entry applications with devices other than keyboards, and also since all of the other devices cost more than keyboards. And although flat panel and micromotion keyboards have become popular in replacing pushbuttons in many applications, the operator feedback of a full-travel keyboard appears to be necessary for the entering of strings of alphanumeric data into a system.

keyboard fundamentals

Full-travel, data entry keyboards are arrays of switches which are placed in rows on 3/4″ centers. Most of these keyboards are arranged according to the Q W E R T Y layout. The horizontal offsets between the rows of keytops is 3/8″, 3/16″ and 3/8″ respectively, from the top row to the bottom row above the spacebar.

Each key position is composed of a keytop and switch. The switch has a plunger that the keytop snaps onto, a housing which is either molded individually or together in a single block with the other switch housings, and some kind of switch mechanism. Switches are located electrically in an X-Y switch matrix so that each switch has a unique X-Y location which can be identified. For example, when the Y lines are scanned by applying a signal to each one successively, any appearance of a signal on the X lines would indicate that a switch closure or coupling has occurred. The position of the key that has been operated is identified by the X line where the signal appeared coincident with the Y line

Mark E. Tiddens is product manager for Key Tronic Corp, based in Spokane, WA.

where a signal was applied. A typical 80-station keyboard would have eight X lines and ten Y lines.

The entire switch matrix must be scanned and keys validated within 2 to 3 msec to allow high speed operation. It has become common to scan the switch matrix twice to confirm that a key has been depressed. This protects against false key closures caused by any interference. This double-scan verification and related algorithms have been developed and proven by keyboard manufacturers based on many years of usage in many applications.

The keyboard has to be totally impervious to differences in operator touch and speed, combinations of which cause switch teasing, bounce or several keys down at once. The ability of the keyboard to accept a number of keys down at once is called "rollover." The most popular rollovers are two key rollover — the second key that is depressed is validated when the first key is released, and N-key rollover — every key is immediately validated as it is depressed, regardless of how many keys are down elsewhere on the keyboard. When keys are actually depressed simultaneously i.e. within one scan of the switch matrix, this is obviously an error condition because an operator cannot know which key was meant to be hit first. This can be treated in many ways, including processing just one of the keys arbitrarily, both of the keys in whichever order they appeared in the matrix scan (the most popular method), or none of the keys with perhaps some kind of error message to the operator. In any case, the scanning of the keyboard switch matrix appears to be much simpler than it is, so an experienced keyboard manufacturer should be used or consulted.

which switch?

The choice of switch technology involves first, the application planned for the keyboard. If it is an application which has other electronics in the same enclosure as the keyboard, it should be considered if the other electronics can service the keyboard with minimum extra cost and components. If, for example, the microcomputer in the terminal or small computer has enough time to service the keyboard scanning and validation, a wired-only keyboard could be used to minimize cost. In this case, a contact switch technology would be selected for the keyboard to facilitate direct scanning of the keyboard.

In the past, reedswitches, Hall-effect switches, and gold-contact switches were popular for wired-only keyboard applications. However, these technologies are too expensive today because of their magnet and reed capsule, precious metal content, and semiconductor and magnet, respectively. Membrane keyboards are quickly becoming popular replacements for these technologies — not only do they eliminate the costly switch mechanisms, but they eliminate the use of an expensive printed circuit board.

However, membrane keyboards are still in their infancy for full-travel keyboard applications. Several manufacturers have introduced them and, as has always been the case, the reception of a new technology is somewhat cool until it has been thoroughly proven in the lab and in field use.

Oak Industries was one of the first to introduce a full-travel membrane keyboard. Subsequently, Key Tronic and Micro-switch have introduced their versions. All three claim their membranes are unique and have been specially designed for full-travel keyboard requirements. Althouth initially it seems that a membrane keyboard is simple, manufacturers claim that very special design and production precautions must be taken to insure reliability to maintain acceptable features, such as a reasonable operating point tolerance. The pretravel, or distance to point of operation, of a switch must be between 50 to 60% of the key travel and not vary more than ±0.035". Otherwise, adjacent keys will throw an operator off by being too touchy at the top of the keystroke.

detached keyboards

Portable, detached keyboards have become popular. They allow the operator to orient the keyboard to a comfortable position. For detached keyboards, the cost of the cable between the keyboard and terminal is significantly reduced

Keyboard Ergonomics

Keytop appearance (including shape, legend quality, matte finishes), smooth switch feel, and tight operating point (pretravel) tolerances are critical to operator comfort and throughput. Achieving, and maintaining, consistent and acceptable human factors is as important to a keyboard manufacturer's success as reliability, price, and delivery.

Europe, especially Germany, has led a recent trend towards increased ergonomic concern. The height is the most significant area affecting keyboards. It has been demonstrated that the keyboard should sit lower on the desk for increased operator comfort. Although there still remains some debate regarding the proposed DIN specifications, the height reduction agrees with an ongoing trend towards lower profile (e.g. the 1/2" reduction in 1975 to achieve more portability and a sleeker appearance).

Two technologies available are tactile-feel capacitance and linear-feel screened contact. A capacitance keyboard is the most cost effective package for all encoded applications (those with electronics immediately associated with the keyboard), especially in detached keyboard enclosures where an inexpensive μP can provide a three or four wire serial output. Detached keyboards are becoming increasingly important for operator comfort in high use applications and are recommended by the German specifications. Tactile feel has become preferred in high duty applications because it provides the necessary operator feedback without an objectionable noise or forcing the fingers to impact the bottom of the keystroke.

The screened-contact technology is cost effective for wired-only keyboard applications. These applications are typically lower-duty terminals and small computers in which the keyboard is not in a detached enclosure. The keyboard does not require dedicated electronics because the X-Y lines of the switch matrix are scanned and keys processed by the main electronics in the unitized enclosure. The cost savings of the screened contact keyboard is due to elimination of the printed circuit board (and electronics). Adding back either an integral PCB or a separate daughter board (plus connector and mounting) defeats this advantage over a low-cost capacitive keyboard design.

A sculptured keytop shape is clearly preferred by the major terminal and computer manufacturers, and can be seen on IBM's new typewriters, IBM's new personal computer and Apple's new personal computers. The single-axis dish is the "fresh, new look" on the low profile ergonomic keyboards. The dish is MT1055 matte finish and the sides are SPI/SPE #5 matte finish to meet the reflectivity requirements i.e. reduce glare. It appears that the truncated Selectric III shape will allow one line of legend on the front skirt, although IBM has disposed of front legends and put more legends on the top (the Selectric III dish is .460" by .560"). The home row shape will be used for stepped keyboard requirements. At the present time, it appears that all sloped (flat) keyboards will become stepped or sculptured, and that the new dish will be used for all applications. D by using a serial data interface. This allows the use of an inexpensive, four conductor cable which carries data in (optional for a handshake interface or driving lighted or audio feedback on the keyboard), data out, power, and ground. Most popular of these cables are the inexpensive standard phone cord and modular connectors.

The necessity of serial output to reduce cable costs requires electronics immediately associated with the keyboard. The most cost effective method is to use an inexpensive switch technology with a small microcomputer, such as the Intel 8021/8048 family, which provides key scanning, validation and serial data output at TTL-compatible levels through the cable. Since a printed circuit board must be used in the keyboard enclosure to mount the serial interface electronics, capacitive keyboard technologies, which also use the printed circuit board as part of the switch mechanism, are the most cost effective for this application.

Membrane keyboards, in addition to not yet being fully proven, require a separate daughter board for the serial interface electronics, which defeats the savings gained by using the membrane. In short, the number of parts for a membrane keyboard with daughter printed circuit board is greater and more costly than that of a capacitance keyboard.

a new profile

There has been an increasing demand for a lower profile, full-travel keyboard in which the keys sit lower on the desktop. Germany actually specifies a lower profile in proposed industry standard specifications which call out a maximum 30mm height from the top of the second or home row keytop to the desktop. Even though these German DIN specs state that a higher keyboard can be used if a wide palm rest is provided, computer and terminal manufacturers are looking for a new keyboard appearance. Keyboard manufacturers are scrambling to introduce low profile keyboards to meet this demand. Most have used it as an opportunity to introduce new switch technologies — either the old switch technologies were not cost effective or would not fit into the new profile.

a new keytop shape

The sculptured keytop appearance, where the top and bottom rows are higher than the center rows, has become popular in all full-travel keyboard applications. In addition, a semi or rough-matte finish for the keytops reduces glare, and a new keytop dish, which has a single radius curvature, is quickly replacing the complex radii dish keytop. The new dish, even though it does not offer a significant increase in square area available for legends, allows more flexibility in placement of legends — the simple curvature allows legends to be placed closer to the sides and corners of the dish.

Computer and terminal manufacturers are taking the opportunity to update their equipment with the new keytop features along with the change to the lower profile.

final result

New computers and terminals are being introduced with detached keyboard enclosures using inexpensive phone cable connections to the CRT. The keyboard is lower profile and has sculptured, matte finish keytops with a simple curvature dish. Thus, portability is offered, the keyboard is more comfortable, glare is reduced and the keytop legends are relocated as desired. The result is a fresh, new look on a product that is much more acceptable functionally to the dramatically increasing number of users. The 1980s will see increased trends in these directions. D

Microcomputer Operating System Trends

advances in VLSI and other technologies force the development of advanced operating systems

As the use of μCs expands, demand for high-level languages and human machine methods of interfacing will expand in 1982 and beyond. One major component of the expanding demand concerns μC operating systems.

by Peter I. Wolochow

An operating system performs resource management and human-to-machine translating functions. Technically, it is just another computer program — a series of instructions that tell the machine what to do under a variety of conditions. Major operating system functions include management of memory, I/O peripherals, and the central processor.

When computers were first developed, the programs (or instructions) were entered into the machine each time a particular job was started. Only with the ability to store a program in the computer's memory, over 30 years ago, did the concept of computers as we know them today truly emerge. The ability to store a program meant that a computer could perform repetitive tasks while the operator had only to enter information upon which calculations were performed.

Once it became possible to store programs, the development of operating systems began. Operating systems were stored in the computer's memory, and provided the user with a bank of stored computer instructions that could be used with a number of different application programs.

Over the years, operating systems have evolved to the point where they have three main purposes. First, they provide clear, consistent, and easily understood guidelines to users concerning how the machine works. A sub-objective is to provide an easier, more "friendly" human interface to the μC. Second, they perform initialization and start-up functions "automatically" so that — to the user — the machine is ready to perform its basic functions. This initialization function originally included only initial start-up, but now often includes methods to recover from errors in both hardware and software. Third, they provide efficient machine and storage resource management so that different users or programs can

Network Development Systems		Increasing Development Throughput (Lines Of Debugged Code/Day)
Unix	MP/M	
CP/M86	Isis (Series III)	
CP/M	Isis (Series II)	

Figure 1: These microcomputer operating systems are primarily for efficient program development.

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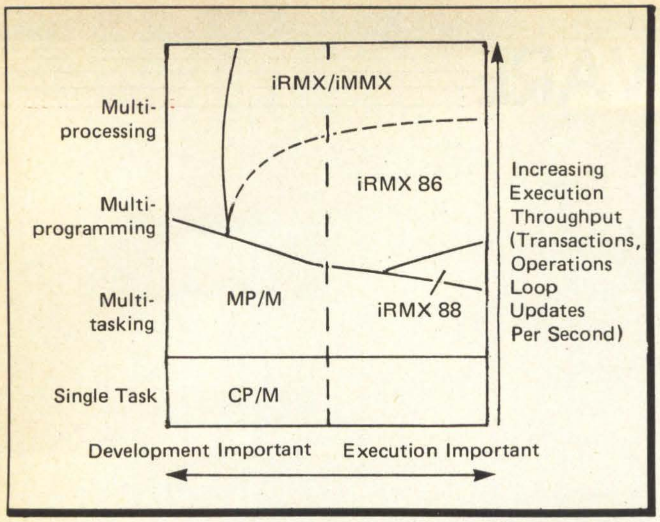

Figure 2: These microcomputer operating systems are primarily for efficient execution.

share the same resources, (e.g., memory, peripherals, I/O ports, a floating point program or the processor itself).

Although virtually all μC operating systems provide users with methods to accomplish these three main purposes, certain operating systems — designed for specific types of applications — have gone far beyond the three common objectives.

One method of viewing μC operating systems has to do with the primary purpose to which the μC is directed. Two major distinctions exist. On one hand, some μC operating systems are used primarily to develop new software systems. In this case, the operating system often includes only features and routines that are useful to persons writing and compiling software programs.

On the other hand, other μC operating systems are directed primarily at efficient execution of software programs for various applications. In this case, the operating system often includes routines and abilities targeted to fast, easy program execution.

software development OS

Within the current world of μC operating systems, examples of those oriented to efficient software development include such products as UNIX (developed by Bell Laboratories) and its related XENIX from MicroSoft, CP/M and CP/M-86 from Digital Research, and ISIS and Networked Development Systems from Intel. CP/M and ISIS-Series II are examples of operating systems designed for the technology and power of 8 bit μC systems. UNIX was designed to match the 16 bit minicomputer, (e.g., DEC PDP-11) and now is being ported (e.g., XENIX) to the newer, more powerful 16 bit μC systems.

Development oriented software systems provide growing levels of programmer support. CP/M, for example, is a single user, single terminal system. UNIX provides support to multiple terminals, so more than one person can be developing software at one time. Intel's Networked Development System provides support for both multiple users over a network, and support for development on multiple processors as well.

execution oriented OS

The second major category of operating systems comprises those primarily targeted to meet the needs of efficient execution of application software already written, developed, and tested. This category includes the largest number of systems, and is often critical to effective utilization of μCs in applications such as industrial control, communications, transaction and word processing, interactive graphics, and simulation.

Often, execution programs working in conjunction with execution-oriented operating systems are developed on a mainframe or minicomputer, with a cross-translator. The other alternative is to develop the software on a μC using a development oriented operating system that has tailored its human interface more to the trained programmer than users of the end product.

In addition to the standard purposes of an operating system — simple human interfaces, initialization, and resource management — operating systems for efficient program execution have a number of other objectives as well. These include real-time operation, multiprogramming, multitasking, multiprocessing, and effective scheduling and priority determination.

real-time operation

Many real-time operations are dedicated to specific applications, such as controlling a machine or series of machines. As such, they often run the same software programs over and over again, depending on inputs received from monitoring and measuring devices attached to the machine they control.

The primary characteristic of such applications is that the data or input that causes the μC to act is not regular, and does not occur at a particular rate. As a result, the μC program and operating system must be able to handle inputs as they occur, and to monitor or control activities based on these real-time inputs.

multiprogramming

This refers to the ability of an operating system to support several independent applications executing concurrently. If a μC, for example, is used to provide an integrated business office system, the software might be divided into a number of separate applications. One might focus on WP, another to manage the printer, and perhaps another to manage an inter-office electronic mail service. Each of these applications would involve a number of tasks devoted to different parts of the system.

An operating system that supports multiprogramming allows this division, and consequently makes it easier to develop the different applications separately, and insure that they do not interfere with each other. This is accomplished by establishing a separate environment for each application. These environments provide the basic appearance of a series of individual machines, while sharing the resources of only one. A multiprogramming operating system must manage this division, keep track of the tasks and requirements of each application, and ensure that each task is given the correct priority.

multitasking

Multitasking refers to the ability of an operating system to effectively manage several tasks, of one computer program, that are operating simultaneously. Multitasking is an important sub-set of multiprogramming, wherein several programs are concurrently being executed. Many applications require that one applications program involve different tasks. Often, these tasks must operate based on data developed in other tasks, and hence a form of task-to-task communication is required. Generally, operating systems designed for efficient program execution require some form of "executive" to manage tasks, priorities, and intertask communication. As a result, common resources such as μP memory and I/O devices can be shared by multiple tasks and can be kept as busy as possible, adding to overall system efficiency.

multiprocessing

Multiprocessing refers to the ability of an operating system to support multiple processors. In certain applications, the demands of the applications exceed the capacity of a single processor or μC. As a result, more processors may be added. When this occurs, the role of the operating system is to efficiently allocate different processing requirements to the various processors, to keep track of which jobs have been sent where, and to assure that the total system resources are effectively utilized. Multiprocessing is becoming more attractive as a way to expand the functions of particular μC applications without the need to entirely rewrite a program. As μCs become less costly compared to software development and maintenance, many systems will use multiple processors, and operating systems will be required to efficiently manage multiprocessing configurations. A means for linkage of multiple processors and operating systems is Intel's iMMX 800 (Multibus Message Exchange) software and iSBC 550 Erthernet communications controller. They support the needs of local area network applications such as office automation, distributed data processing, factory data collection, research data collection, intelligent terminal and other EDP-related applications.

scheduling and priority determination

As μC operating systems are required to manage even more complex functions — such as multiple programs, multiple

Processor Management:	iRMX 86	UNIX	CP/M	RSX-11M	RT-11	MTOS-86
Scheduling	Realtime	Multiprogram	Batch	Realtime	Realtime	Realtime
Multitasking	Yes (64K)	No	No	Yes (64K)	No	Yes (4K)
Priority Levels	255	None	None	250	None	255
Multiprogramming	Yes (64K)	Yes (64K)	No	Yes (64K)	Foreground /Background	No
Multiprocessor	iMMX	No	No	No	No	Yes (16)
Multiuser	Release 5	Yes	No	Yes (4)	No	No
Interrupt Management	Yes	No	No	Yes	Yes	Yes
Error Management	4 levels	Yes	No	Yes	Yes	No
Powerfail Protect	No	No	No	Yes	No	No
Memory Management:	**iRMX 86**	**UNIX**	**CP/M**	**RSX-11M**	**RT-11**	**MTOS-86**
Dynamic	Yes (1MB)	Yes (64K)	No	Optional	No	Yes (64K)
# of Memory Pools	64K	One	One	8	One	32
Memory Resident	Yes	No	Yes	Yes	No	Yes
Application Loader	Yes	Yes	Yes	Yes (11S: No)	Yes (RT^2: No)	No
Bootstrap Loader	Yes	Yes	No	Yes	Yes	No
(P) ROM'able	Yes	No	No	No	No	Yes
Device Management:	**iRMX 86**	**UNIX**	**CP/M**	**RSX-11M**	**RT-11**	**MTOS-86**
Concurrent I/O	Yes	Yes	No	Yes	Yes	Yes
I/O Buffering	Yes	Yes	No	Yes	Yes	No
Reentrant I/O	Yes	Yes	No	Yes	Yes	Yes
Asynchronous I/O	Yes	No	No	Yes	Yes	Yes
Synchronous I/O	Yes	Yes	Yes	Yes	Yes	No
Device Independent I/O	Yes	Yes	Yes	Yes	Yes	Yes
Max. # of Drivers	64K		256	256	16	256
Data Management:	**iRMX 86**	**UNIX**	**CP/M**	**RSX-11M**	**RT-11**	**MTOS-86**
File Support:						
1. Sequential	Yes	Yes	Yes	Yes	Yes	Yes
2. Indexed Seq.	No		No	Yes	No	No
3. Direct Access	Yes	Yes	Yes	Yes	Yes	Yes
Swapping	No	Yes	No	Yes	No	No
Overlays	Yes	Yes	Yes	Yes	Yes	No
Hierarchical Directories	Yes	Yes	No	No	No	No
Stream Files	Yes	Yes	No	No	No	No
Mailboxes	Yes	No	MP/M	No	No	No
Critical Regions	Yes	Yes	No	No	No	Yes
Host System For Development	Yes (With UDI)	Yes	Yes	Yes (11S: No)	Yes (RT^2: No)	No

Figure 3: Comparison of microcomputer operating systems

tasks, and multiple processors — the ability of the operating system to schedule activities becomes a primary consideration. In early multiprogramming operating systems, many of these scheduling routines were time driven. That is, one program would be allowed to execute for a certain time. It would then be interrupted, and another program would be allowed to execute. This time driven scheduling, in effect, forced multiprogramming to occur, but also often involved a significant amount of operating system overhead to manage the process.

Subsequently, the approach of event driven scheduling was developed. With this approach, programs and tasks are allowed to proceed until some predetermined event causes the operating system to interrupt the running task and substitute another. In many applications, event driven scheduling is the most efficient manner of allocating resources. In addition, event driven operating systems can often be modified to include some time driven scheduling routines, where the reverse is not possible. As a result, event driven systems are more flexible and can manage the μC and other system resources more efficiently.

future issues

As the μC world continues to evolve rapidly, changes in semiconductor technology will continue to force evolution and improvement in operating systems. As this evolution occurs, a number of trends and developments will influence the user's choice of appropriate operating systems. Some of these developments include:

Very Large Scale Integration (VLSI) Trends. As more complex functions are integrated into μC chips,operating systems will be required to support a broader variety of needs and application programs. The benefits of VLSI — such as increasing density, substantial improvements in function, and rapidly declining costs per function — accrue to those who rapidly use the newest technologies. As a result, μC users on the leading edge often can build significant competitive advantages by being first to market.

With regard to operating systems, trends toward greater VLSI integration imply that operating systems should be evaluated based on their ability to most rapidly use technological advances. This ability to capitalize on VLSI trends includes:

- Operating systems with the potential to be integrated into silicon. Intel, for example, has introduced a device that integrates timers, an interrupt controller, and multiprogramming and multitasking operating system "primitives" into one device. (These operating system functions are equivalent to those of the iRMX 86 kernal.) In essence, some of the traditional software functions will become part of the hardware. Such a development opens a number of vistas for future integration.
- Operating systems organized to take advantage of new trends in μC architecture. One of the most promising developments in this area is object-oriented architecture such as that implemented on iAPX 86 processors under the iRMX 86 operating system and on Intel's new iAPX-432 32 bit micromainframe product family. Essentially, an object-oriented architecture treats different kinds of data and instructions as "objects" and provides common functions that can manipulate objects in a consistent manner. Moreover, the object oriented architecture also meshes closely with the new types of high level languages — such as Ada — now being brought to market. These developments begin to provide μCs designed to optimize both program development and execution.

Transaction Processing

by John Huie

"Transaction processing" takes its name from the "transactions" of an accountant's journal. When Smith Liquor Wholesalers sells a case of Brand-X Vodka to Joe's Bar and Grill, a transaction has occurred which must be recorded. More specifically, Smith must record each of several components of the transaction: one fewer case of Brand-X Vodka remains in stock, the accounts receivable balance due from Joe's is increased, etc. To record this transaction, Smith could use a manual accounting system, a batch processing system, or an on-line transaction processing system. While characteristics of on-line transaction processing systems vary widely, they share a few basic properties. First, all records are on-line and continuously available. Second, all information pertaining to a single transaction is entered into the computer at the same time and need be entered only once. Third, all information is automatically verified at the time it is entered. Fourth, all records affected by a transaction are updated at the same time the transaction is entered.

Typically, three software components exist in a transaction processing system. Their functions are as follows: First, "interaction with the person(s) entering the transactions" software allows convenient entry of transaction data into the blanks of forms displayed on a video screen. Second, "accessing and updating records" software must support various records and allows accessing them efficiently by "key" value. In the above example, it is necessary to access the record that contains the quantity-on-hand of Brand-X Vodka. The stock code that identifies Brand-X Vodka is the "key" value in this case. Ideally, it should be possible to access the same record by any of several "key" values. This would allow a logical grouping of all Brand-X products or all vodkas, for example. If more than one person will enter transactions simultaneously, this software must provide facilities to ensure that simultaneous updates do not cause unwanted interaction. Third, is "application specific processing." The first two software components (often general purpose) are provided by the hardware manufacturer; the third usually is provided by the end user.

Available products combine these three components in two distinct architectures. The central difference is whether a general-purpose forms package (component 1 above), or application specific logic, is the controlling element.

Application specific logic is usually the controlling element in single user systems and timesharing systems. This architecture is the simpler, but is the more flexible because application specific decisions can control the sequence in which forms are displayed, and even the sequence in which information is accepted into the blanks of a form. The characteristic disadvantage of this architecture is the amount of computer memory and computer processing power required for each person entering transactions. This is typically reflected in *high hardware costs* and/or annoying *delays in processing transactions*.

Transaction processing controlled by a general purpose forms package was developed in the early 1960s to increase the number of persons who could simultaneously enter transactions into a computer with limited (and very expensive) memory. These systems achieve increased computer utilization at the expense of more complex application system development and decreased flexibility. In this architecture, application specific logic is read into memory only after an entire transaction has been entered. Such general

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purpose packages have relatively limited mechanisms for verifying the data entered into each blank of each form, and for selecting the appropriate application specific logic to process the transaction.

A local resource sharing network (cluster) is well-suited for transaction processing because it provides the flexibility and ease of application development of the first architecture at the operational cost of the second. Shared mass storage provides controlled access to a common data base, while the dedication of a powerful (but low cost) computer to each person entering transactions provides immediate response to each entry. Application-specific logic controls the highly flexible and multi-key, multi-user product, producing low operational cost, fast response, simple application system development and application flexibility.

Information processing systems exist for a broad range of computer systems to meet demanding requirements of OEM system builders. They are based on multifunction, display-based desktop minicomputers that operate in standalone, cluster and network configurations. Compact workstations combine an ergonomic human interface with the processing power of a medium scale minicomputer.

Let's examine our multifunction workstation. It incorporates a high resolution 15" video display and OEM-oriented keyboard. Its video display is mounted horizontally in "landscape" mode. The display is fully articulated and tilts as well as rotates. The screen displays 34 lines containing 80 or 132 characters. Each character is displayed in a 10×15-dot cell. The screen can split into an unlimited number of independent frames. Each frame can then be scrolled independently.

The screen is refreshed 60×/sec directly from characters and their associated display attributes stored in main memory. Display attributes include: reverse video, blinking, underline, and half-bright. The video controller supports an unlimited number of character sets. Each character set contains 256 characters. The current character set is defined in a special high-speed memory.

The detachable typewriter-style keyboard has 98 keys which include a 14-key numeric pad, 8-key control pad, 6-key cursor pad and 10 user function keys. Eight keys contain LED indicators. For maximum flexibility, the keyboard μP reports "up" as well as "down" key transitions of all keys (including the SHIFT and CODE keys).

Workstations have two programmable serial communications channels; each is programmable independently to support asynchronous protocols, byte-synchronous protocols (such as Bisync), and bit-synchronous protocols (such as ADCCP, SCLC, and HDLC). Both channels provide access to status and control signals such as ring, data set ready, secondary data, etc. Other standard workstation features include: a printer interface, real-time clock, programmable timer and power-fail/auto-restart.

Each workstation is connected to a mass storage subsystem, high-speed cluster data link, or both. Mass storage subsystems match configurations, ranging from standalone workstations to 16-station clusters, by utilizing a combination of Winchester disks and floppy disks to provide from 1 to 240 Mbytes of storage.

Multifunction workstations can be interconnected into a cluster configuration — a local resource-sharing network that provides controlled sharing of common files and reduces cost by sharing disks and printers by several workstations. Responsiveness exists: each cluster workstation executes its own interactive application program. Each user in a cluster configuration has a dedicated minicomputer.

A cluster configuration has a master workstation and up to 16 cluster (slave) workstations connected via a high-speed data link. Files on master workstation disks are accessible to each cluster workstation, subject to password protection. In

(continued on page 56)

The benefits of VLSI — such as increasing density, substantial improvements in function, and rapidly declining costs per function — accrue to those who rapidly use the newest technologies.

Standards for μC Languages. μC applications have evolved requiring higher level languages so less technical users can easily participate in VLSI technology. Without substantial advanced planning, the use of higher level languages can cause significant problems with operating systems. One example of how advanced planning is done is Intel's approach. Intel's iRMX 86 operating system contains both a Universal Development Interface (UDI) and a Universal Runtime Interface (URI). These two interfaces provide a standard upon which high level languages can be both developed and run. In essence, the UDI/URI approach is developing a "software bus" or series of standards for easy and consistent language development. Without such an approach to standardization, each new language could be retarded in its development and each new processor could require a completely new set of compilers.

Among the many benefits of this approach are those of particular interest to persons who have been hesitant to use μCs because of the lack of standardized, high-level computer languages. With the development of the UDI/URI approach in iRMX 86, for example, languages currently or soon to be available include FORTRAN 86, PASCAL 86, PLM/86 and ASM 86.

Another major advantage of software standards now being developed is that many vendors can now create languages that will operate effectively on the same operating system. The software bus concept provides these vendors assurance their languages will operate, and it also provides μC users with a significantly broader range of application languages and even pre-developed software. Among the newer computer languages currently under development by independent software vendors as a result of the UDI/URI standardization are BASIC, COBOL, and "C".

This one development — the standardization of software development and runtime environments — has the potential to be as significant to μC users as earlier efforts to standardize on communications methods (such as the IEEE 488 standard) or μC standardization such as the Multibus (IEEE P796). Once a standard is developed and accepted, many different manufacturers can develop products with the assurance that they will be compatible with other products. Hence, the user obtains a broader selection and applications innovation is enhanced. Moreover, users need concentrate only on learning one approach, with a corresponding improvement in speed and productivity of applications efforts.

Standards for μC Networks. Increasing use of VLSI means that μC costs per function are declining. As a result, many new applications will become cost-effective. One of the major new application areas VLSI is stimulating is local area networking. The costs of μCs and supporting memory are now declining to the point where local and even global area networks make more and more sense. As networking becomes more practical, however, new approaches to networking standards will be required.

(continued from page 55)
addition, each cluster workstation can have private files on a local disk.

In a cluster configuration, the operating system is distributed between cluster workstations and master workstation. In the master workstation, the OS concurrently supports local application processing and resource sharing for the other cluster workstations. The master workstation provides all cluster workstations with data base management, file management, printer management, 3270 emulation and 2780/3780 emulation. Other services, such as video and keyboard management, are provided independently by each cluster workstation.

The distributed nature of the operating system allows cluster transparency to application programs. An application program can be transported from standalone to cluster or from cluster to standalone with no change.

file management system

While providing convenience and security, the CTOS File Management System delivers full throughput capability of disk hardware. Optimizations include: disk arm scheduling, volume control structures located on center disk cylinders (to minimize disk arm movement), frequently accessed structures cached in memory, and randomization (hashing) techniques used to access directories (to reduce the number of disk accesses needed to open a file).

Asynchronous I/O is the native mode of the file management system. This means that a process requests an I/O operation and then resumes execution while the I/O transfer occurs. A single read or write operation can transfer up to 127 512-byte disk sectors. If the sectors are continuous, the transfer is performed in a single continuous DMA operation. For simple programs, a procedural interface is available to suspend the execution of the requesting process until the completion of its I/O operation.

File system reliability is enhanced by the duplication of critical volume control structures. This protects the integrity of disk file data against transient hardware malfunction. Even under adverse circumstances, the backup utility is able to recover a file by using this redundant information.

The CTOS File Management System provides hierarchical organization by volume, directory, and file. Each file resides on a named disk volume and is grouped into a directory. Volumes, directories, and files are protected by passwords.

Each file can have a 50-character file name, a 12-character password, and a file protection level. A file can be dynamically expanded or contracted as long as it fits on one disk. Concurrent access is controlled by shared-read and exclusive-modify access modes.

Each CTOS file consists of one or more groups of contiguous 512-byte disk sectors. If possible, a file consists of only one group. Because the information needed to describe the groups is very compact, and is retained in memory while a file is open, any sector of any open file can be read or written with one disk access.

Several methods augment the file management system. These access methods are as follows. First, Sequential Access Methods (SAM): SAM allows the sequential reading and writing of byte strings of arbitrary length. Second, Record Sequential Access Method (RSAM): RSAM allows the sequential reading and writing of variable length records. Third, Direct Access Method (DAM): DAM allows reading, writing and deleting by record number. The fixed length of the records in a DAM file is specified when the file is created. Fourth, Indexed Sequential Access Method (ISAM): ISAM allows fixed length records to be sorted, updated, retrieved, and deleted by any of multiple record keys. The implementation uses a balanced tree (sometimes called a "B-tree" or "block splitting"). ◘

Standards are particularly important for networking μC operating systems, since the operating system will be required to manage many of the networking resources. In this regard, Intel Corp, Xerox Corp, and Digital Equipment Corp have joined together to develop Ethernet, a local area network standard. (Many other firms are also becoming involved with Ethernet, including Hewlett-Packard, Siemens, Nixdorf, Olivetti, and Zilog.)

One of Intel's Ethernet responsibilities is to provide standard modules and standard interfaces for Ethernet users. These include high level, data link layer interfaces to an Ethernet controller on the standard Multibus, a new Multibus Interprocessor Protocol (MIP), and a method to support Ethernet with the iRMX 86 operating system in conjunction with Intel's new Multibus Message Exchange (iMMX). Intel intends to provide VLSI implementations of these standards, up to the data link layer. As futher Ethernet standards evolve, the major benefit to networking μC users will be the ability to take advantage of a wide variety of products with the assurances they will work together effectively.

Protection of Software Investment. Many μC users have substantial investments in μC software and are consequently concerned that these investments do not become obsolete before having provided an adequate return on the resources invested. Many current minicomputer users, for example, would like to take advantage of the density, size, and low cost per function benefits of μCs but are hesitant to redevelop their existing application software.

Recent developments in μC software are directed toward solving this concern. The trends toward software and networking standards, for example, will provide a basis for rapid development of new language compilers, and emulators that allow minicomputer users to migrate to more technically advanced μCs without a commensurate reinvestment in software development.

Other trends in μC operating systems, such as increasing modularity and configurability, also support this direction. Intel's iRMX 86 operating system, following this trend, is developed in modules. This allows future integration of certain modules into silicon as conditions warrant. Modularity and configurability also mean users can eliminate portions of the operating system not appropriate to their application without a performance penalty. In addition, Intel's approach to operating system design means that current μC systems users can easily and cost-effectively move most of their existing software from 8 bit to 16 bit μCs as their application requirements expand. This design consideration, most noticeable in the iRMX 86 operating system, guarantees substantial user software investments are protected while users can, at the same time, rapidly take advantage of the latest developments in VLSI technology.

hardware advances mean change

Rapidly advancing developments in μC technology are causing a corresponding change in μC operating systems. More and different operating systems are becoming available as users' needs evolve and become more specialized.

The rapid march of VLSI technology also pressures manufacturers, OEMs, and end users to develop and evaluate operating systems based on their ability to directly translate VLSI advances into applications.

Moreover, the need for a series of operating systems standards is clear. Without standards such as the UDI and URI, operating system development could retard the widespread and fast growing use of productive microelectronics technology. ◘

Voice Digitizer/Encrypter Provides Data Security

Most voice digitizers perform the same function: they provide a method for transmitting multiple, high-quality voice and data messages through a telephone line. Voice digitizers can help realize cost savings in communications expenditures substantial enough to make the office-of-the-future arrive sooner. The main difference among digitizers from various sources besides physical appearance, is the application of technology. Some manufacturers seem reluctant to discuss specific in-house steps that lead to substantially the same market-wide result. Information describing technological breakthroughs or refinements may be quietly side-stepped, under a proclaimed need for product protection, in favor of user application information.

Racal-Milgo's entry into the digitizer marketplace, the Phoneplex-24, allows up to four simultaneous voice conversations, or a combination of voice (analog) and data (digital) communications, to share a common facility link when used in conjunction with multi-port modems. The device relies on a sampling and prediction technique called linear predictive coding (LPC). Even though there is nothing new about applying LPC technology, Racal-Milgo hesitates to reveal its exact application. The firm has made what it calls "major refinements" in LPC technology use and augmented it with its own research work.

Phoneplex-24 takes your voice and tone, samples them, goes to its processor, and predicts what the next sound will be. It then samples the next tone and does a comparison to the prediction it made, adjusts it and ultimately transmits it through a high speed processor. By predicting speech bits, Phoneplex-24 condenses a voice from, say, 64,000 bits down to 2400 bits per sec.

So what distinguishes Phoneplex-24 from other units? According to a Racal-Milgo spokesman, "You listen to it, you recognize whom you're speaking to and you understand what they are saying. Whether the quality of the voice is good is a subjective opinion based on listening to other voice digitizers."

dollar savings

The major point of interest, the firm says, is the dollar savings for domestic long-haul and multinational circuit users. If you amortize the basic unit price of $9000 over a five year period and then compare it to the current AT&T tariffs for leased telephone facilities, Racal-Milgo predicts the break even point (cost of hardware versus the rental price of leased line facilities) will occur within the 350-400 mile range.

communication security

A combination of Phoneplex-24 with Racal-Milgo's Datacryptor II stand-alone encryption product can provide voice communication security. The digital Datacryptor typically sits between a modem and a terminal. In an application with Phoneplex-24, it connects to the digital side of the device and encrypts the ones and zeros.

Phoneplex-24 can also work in conjunction with the diagnostic and control capabilities of the firm's CMS 1000 and CMS 2000 communications network management system consoles. These diagnostic central site devices control optional μP-based boards and all Racal-Milgo's modem products. Datacryptor ultimately multiplexes into Racal-Milog terminals so that any piece of equipment marketed by the firm can come under the control of the communications management package.

by Peter Lichtgarn

Racal-Milgo Inc., 8600 N.W. 41st St., Miami, FL 33166 **Circle 198**

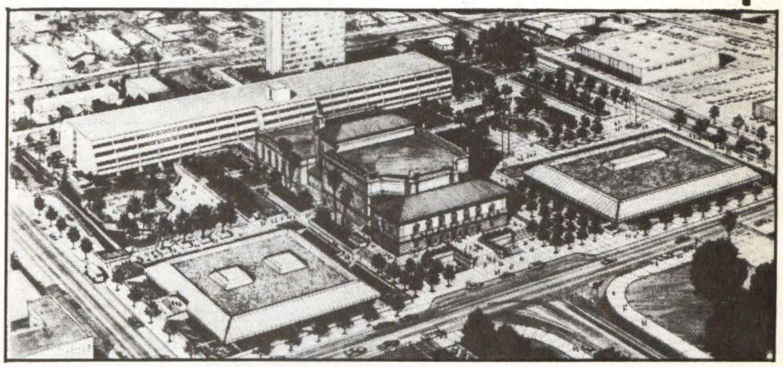
Figure 1: For security, Phoneplex-24 encrypts voice transmission to protect against eavesdropping. Because voice input is transformed into a digital format, data can also be encrypted when used with Racal-Milgo's Datacryptor II. The datacryptor sits between a modem and a terminal, connects to the digital side of the Phoneplex-24 and encrypts the ones and zeros to keep messages secure. Instead of renting separate lines for voice and data, Phoneplex-24 allows you to combine them into one circuit. Utilizing a 9600-bps multipart modem, one voice transmission occupies only 25% of the available bandwidth.

Workshops

1. Standardized Measurement System Integration Using the IEEE 488 Interface Bus
2. Problems in Automatic Testing of High Speed Digital Systems
3. Digital In-Circuit Test — A Look at Different Techniques
4. The ATE Selection Process for Analog, Digital and Hybrid Functional Test Systems
5. How to Manage an ATE Test Programming Group
6. Digital Diagnostics Beyond the Node
7. Standards for Aids and Components In an ATE Facility
8. Introduction to Testing of Microelectronic Devices
9. How to Get Started in ATE
10. Designing-In Testability
11. PCB Test Method Decisions
12. Experience with Automatic Collection of Signatures and Subsequent Circuit Fault Isolation
13. Analog In-Circuit Component Test
14. Quality Control in the Generation of Functional Test Programs
15. Power and Grounding for ATE Systems
16. Field Test ATE Needs
17. Planning and Implementing a Modern ATE Facility for Testing RF Equipment
18. Digital Test Strategy — What Cost to Test
19. Choosing Equipment for and Integrating to IEEE-STD 488 Automatic Test Systems
20. Testability
21. Test Equipment Selection Procedures
22. Dynamic Functional Testing of μP-Based Circuits Using Signature Analysis
23. Analog Testing Using In-Circuit Techniques
24. To be Announced
25. ATE as Used in Automated Integrated Manufacturing
26. Test Fixturing Applications and Techniques
27. Alternative Approaches to Testing μP-Based Products
28. How to Manage an ATE Facility
29. Evaluating Costs of Test Alternatives in a Typical Manufacturing Environment
30. To Simulate or Not to Simulate — A Question of Economics

Equipment Exhibit

January 19-21, 1982



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ATE MATE
A.T.E. SYSTEMS
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AUTOTEST
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BECKMAN INSTRUMENTS
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BENDIX
BOONTON ELECTRONICS
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COMPUTER CONSOLES
COMPUTER DATA SYSTEMS
DATA I/O
DATATRON
DAYMARC
DIGALOG SYSTEMS
DIT-MCO INTERNATIONAL
DT SYSTEMS
EAGLE TEST SYSTEMS
EATON TEST SYSTEMS
EG&G WAKEFIELD
E-H INTERNATIONAL
ELECON
ELECTRO-MECHANICAL SYSTEMS
ELECTRO FIX
ELECTRONIC MANUFACTURERS SERVICES EMS
ELECTRO-SCIENTIFIC INDUSTRIES
E. LEITZ
EMD ASSOCIATES
ENGINEERING CONSULTANTS & PUBLICATIONS
ES•P
EVERETT/CHARLES
FAIRCHILD TEST SYSTEMS GROUP
FLUKE AUTOMATED SYSTEMS
FTS SYSTEMS
GENRAD
3H INDUSTRIES
W. M. HAGUE ASSOC.
HEWLETT-PACKARD
HHB TEST
HILEVEL TECHNOLOGY
HUGHES AIRCRAFT
HUNTRON INSTRUMENTS
ICS ELECTRONICS
INSTRUMENTATION ENGINEERING
INTERFACE TECHNOLOGY
INTERSTATE ELECTRONICS
LEASAMETRIC
LEXICO
LOMAC
LTX
MARCONI ELECTRONICS — INSTRUMENT DIV.
MARCONI ELECTRONICS — ATE SYSTEMS DIV.
MCT
MCT BROWNE
MCT MARIN
MICROCOMPUTER POWER
MILLENNIUM SYSTEMS
NATIONAL INDUSTRIES
NH RESEARCH
NORLAND
ONEAC
OSTBY & BARTON
PLANTRONICS/ZEHNTEL
PRACTICAL TECHNOLOGY
PRAGMATIC DESIGNS
PRECISION AUTOMATIC EQUIPMENT
PROGRAM DATA
PYLON
RACAL-DANA INSTRUMENTS
RELIABILITY
ROD-L ELECTRONICS
SCIENTIFIC ATLANTA (ADAR PRODUCTS)
SENSITEK
SIEMENS
SOLARTRON INSTRUMENTATION GROUP
SYSTRON DONNER INSTRUMENT DIVISION
T&B/CABLESCAN
TEKTRONIX
TEMPTRONIC
TERADYNE
TEST ENGINEERING SOLUTIONS
TESTMASTER
TEST SYSTEMS
THALAMUS ELECTRONICS
THREE PHOENIX
TRACE INSTRUMENTS
TRIGON INDUSTRIES
UTI INSTRUMENTS
VERSATILE INTEGRATED MODULES
VIRGINIA PANEL
WESTMINSTER ENGINEERING
ZIATECH

Produced by Electronics Test and co-sponsored by *Circuits Manufacturing, Digital Design* and *Design Engineering* magazines.

Disk Subsystem Provides H-P Mass Storage

The MSC-9800 series Winchester disk drive storage subsystem enables users of Hewlett Packard's personal professional computers and other IEEE 488 bus-based systems to replace four conventional double-sided, double-density, 8″ floppy disks with a single compact desktop unit that is one-fourth the size, one-third the weight, and one-third the cost of an equivalent floppy disk system.

The 9800 Series was specifically designed for use with the entire line of HP personal professional computers, including the Series 80 and the HP 9845.

It is an emulation of the HP 9895 floppy disk subsystem on a 5-1/4″ hard disk drive. It includes a disk, controller, power supply, and interface to the GP-IB (IEEE-488) bus.

Software transparent to the command set of the HP computer, the 9800's capacity allows the user to go one-on-one with the HP personal professional computer configured with the GP-IB interface and the Mass Storage capability.

The disk drive connects directly to the computer, which provides all the necessary interface controls so that the disk drive and the computer can communicate.

The 9800 incorporates the proven Seagate Technology 5-1/4″ disk drive, which provides up to 4.6 Mbytes of formatted storage capacity on two rigid disks with four heads — the equivalent storage capacity of one double-sided floppy disk on each 9800 hard disk surface. With address mapping the computer sees four individual units with up to 75 tracks per recording surface, two heads, 256 bytes per sector, and 30 sectors per track.

The 9800 Series single board, standalone, intelligent controllers are based on MSC's 9000 Series Micro Modules. This "black box" contains 75% of all controller circuitry in a unit only 3″ square but, according to MSC, with all the features found in larger, more expensive controllers.

Other features include automatic 22-bit burst error detection and 11-bit burst error correction, partial sector transfers, a full 256-byte data buffer for optimal transfer rates, needed for storing and transferring data.

The drive uses only DC voltage, which is provided by the 115V/230V power supply included in the 1980.

Costly software conversions are avoided because the 9800 attaches directly to the computer bus. The entire 9800 unit, which measures only 6-3/8″ × 10-1/2″ × 12″ is designed to be performing reliably and inexpensively 20 seconds after being powered up. Unit prices are under $4000.

Microcomputer Systems Corp, 432 Lakeside Dr, Sunnyvale, CA 94086.
Circle 199

Nova-Compatible Subsystem Includes Winchester Disk/Streaming Tape

Until recently, low-cost, reliable Winchester disk drives couldn't be supplied with an integrated streaming tape cartridge for the Nova-class computer. But Microtech's Dart-MS1 subsystem provides a 14″ Winchester fixed disk drive in 34 Mbyte or 68 Mbyte capacities; a 1/4″ 20 Mbyte streaming tape cartridge drive for backup; the new Microtech Dart controller board; a chassis; and a high-performance power supply.

The subsystem also includes four ports of MUX (device code 30), master console support (device code 10/11), a real time clock (device code 14) and a parallel printer.

The subsystem's controller can accommodate up to four daisy-chained disk drives for a total storage capacity of 272 Mbytes. And it's compatible with most Nova-type computers, featuring drivers for the IRIS and RDOS operating systems (other drivers available soon).

List price for the 34 Mbyte Microtech MS1 subsystem is $8,700; $9,500 for the 68 Mbyte version.

Microtech Business Systems, 3180 Pullman St, Costa Mesa, CA 92626.
Circle 200

Microtech Business Systems' new DART-MS1 subsystem supports terminals, a printer and more with a 14-inch Winchester hard disk drive in 34Mbyte or 68Mbyte capacities and a 20Mbyte streaming tape cartridge drive for backup.

New Products

NOVA-COMPAT MINICOMPUTER

Fast 100 ns Machine

The MiniMate features an Instruction Execution Time of 100 ns (Arithmatic), 200 ns load and store. Memory access time is 55 ns to a capacity of 128kB. DMA transfer time is 800 ns, but a slow-speed channel is also available. The backplane features priority encoding, making it easier to change configuration: 8 of the 9 slots are free, providing greater system flexibility. Other features include: execution/DMA overlap; modular, field-replaceable power supply; virtual front panel; and software compatibility with a range of operating languages. An on-board battery backup maintains memory for 3 days, even if the board is removed. Several models are available from a single-board computer to complete systems. $5025 to $15,275. **Integrated Digital Products,** 3150 E. La Palma Ave, Suite D, Anaheim, CA 92806. **Circle 130**

FLEXIBLE DISK HEAD

Improved Media Interchangeability

This dual-sided flexible disk head assembly has an adjustable upper arm that improves reliability of media interchange for systems with track densities of 96 tpi and greater. This new design is adjustable to within 50 millionths of an inch as compared to the industry-wide required tolerance for 96 tpi head zero to head one alignment of 200

millionths of an inch. Drives which can use this head assembly do not require modification — simply replace the existing head assembly. **Nortronics Co,** 8101 Tenth Ave North, Minneapolis, MN 55427. **Circle 161**

TINY CORE MEMORY

Ideal For Nonvolatile Storage Of μP Data

Model 120 is a four bit array which can store a status word upon power shutdown or loss and retain it for an infinite time. Intended to

displace designs built around CMOS RAMs with batteries and chargers, or multivoltage MNOS devices, the 120 operates with only +5V and utilizes low cost common TTL logic chips as support circuits. In a typical application the 120 would be accessed by a μP I/O port in response to a power-down sequence. Data is loaded sequentially in four cycles, and retained indefinitely on shutdown. On bring-up, the data is sequentially loaded back through the I/O port to return the status word. The Controlex 120 is packaged in a 14 pin DIP, and is available as a core module only, or with supporting circuitry mounted on a 1" by 2" PCBA ready to plug into the host system. Speed is $1\mu s$ cycle time. Variations, including longer word lengths (ie: 8 bits), parallel access, and custom support circuitry are available. Delivery from stock; $6.90 (OEM qty). **Controlex Corp,** 16005 Sherman Way, Van Nuys, CA 91406. **Circle 171**

TAPE ADAPTER

Interfaces Cipher F880 To TI 990 Tiline Bus

The unit's cipher drive provides the logic for data encoding and decoding, character deskewing, error detection and correction, data storage, and tape motion control. The Cipher F880 writes and reads ANSI-compatible 1600 bpi PE tape at 100 and 25 ips. Consisting of a TI990 board which mounts inside the computer, the 1995 uses the TI 990 peripheral control store to pass commands to and read status from the Cipher drive. The 1995 also contains the Tiline DMA hardware and converts the 8-bit parallel data to or from the drive to 16-bit parallel data to or from the host. Its software processes the command control of the tape drive using the device driver routine. $1000. **Microcomputer Systems Corp,** 432 Lakeside Dr, Sunnyvale, CA 94086. **Circle 148**

New Products

DUAL WIDE MEMORY CARD

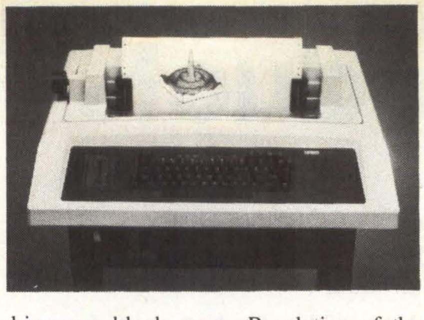
Several Configurations For Q-Bus

The MK8022 has several configurations including 128kB and 256kB parity versions. It features standard 22 bit addressing which extends the card's address range to 4MB. The boards are also designed with an internal distributed refresh capability, onboard parity generate and check, and battery back-up for memory retention if the primary power fails. The 128 kB board is $1200, 256 kB is $2075. The MK8023, a quad-wide board for LSI-11 products, is also available. **Mostek Corp,** 1215 W. Crosby Rd, Carrollton, TX 75006. **Circle 133**

RASTER GRAPHICS BOARD

Graphics Now Available For Digital's LA120

The SG120R is a raster graphics board manufactured specifically to expand the range of versatility of the LA120 DECwriter into the field of graphics. It can be installed in less than one minute, using no tools except those necessary to open the rear door of the printer. Maximum input data rate is 9600 baud and average printing rate is 752 graphics columns/sec, with speed enhancement features that allow the print head to



skip over blank areas. Resolution of the board is 110 dots/inch horizontally by 72 dots/inch vertically; maximum number of horizontal dot columns is 1452. There is no maximum to the number of vertical rows that may be printed. $600. **Selanar Corp,** 437-A Aldo Ave, Santa Clara, CA 95050. **Circle 170**

LSI-11 SYSTEM BOXES

22 Bit Addressing Capability

The MLSI-BA11-600 series incorporate a ruggedized backplane/card cage assembly. One model backplane, the BPA84A, has 14 slots dedicated to Q-bus signals with slots for DECs RLV11/RLV21 hard disk controllers. A switching power supply provides +5 VDC @ 25A, +12 VDC @ 4A and −12 VDC @ 1A. The series also provides 22 bit addressing and includes power failure sequencing circuitry and a Line Time Clock. $1450; under $900 in qty 100. **MDB Systems Inc,** 1995 N. Batavia St, Orange, CA 92665. **Circle 131**

VIDEO DISPLAY

Graphics Capability

The Graphicus-80 is a high resolution intelligent terminal with a large 21" display. It is a stand alone system with keyboard. Resolution is 4096 × 4096. Features include 2D clip, rotate, translate; optional 3D; and, serial or parallel interfaces. It has an 80 line readout, the number of char/line depends on the size of the characters. Readout colors are P39 green, P40, P4 and white. **Vector Automation,** Village of Cross Keys, Baltimore, MD 21210. **Circle 139**

EXPANDED PRINT OPTION

Choose From 42 Type Sizes

This option for Datapoints 160 cps matrix printers provides 42 type sizes and allows the programmer to design and download custom character fonts. Character height is controlled by the line space value with a selection of 8 values from .75 to 8 lpi. The horizontal spacing value determines character width with a selection of 6 values from 1.25 to 16.5 cpi. Firmware options are invoked through a menu-driven software package supplied with the option. The program can also set tabs on the printer, print characters directly to the printer so the user can see what they look like, and download user-designed character sets to the printer. $200. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284. **Circle 153**

WINCHESTER SUBSYSTEMS

Fully PDP-11 Unibus, RT11 And RSX-11M Compatible

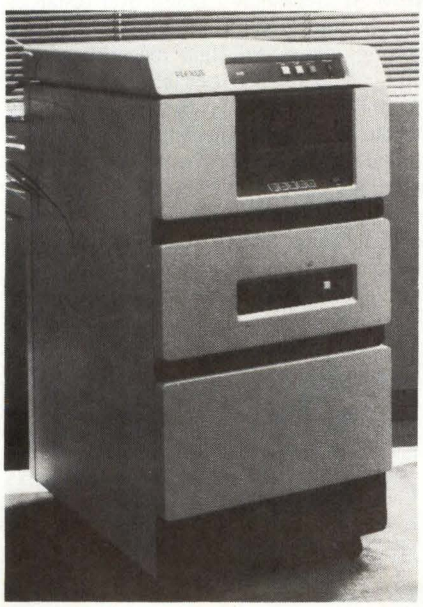
These Winchester fixed disk drive subsystems complement the DSS 1100 cartridge disk subsystems emulating DEC RL02 drives and offering full compatibility with LSI-11 Q-bus processors. The DSS 1300 series is available in several configurations. All include CII-HB Cynthia D 162 disk drives, power supply packaged in a dual drive 19" rack mountable drawer and a disk controller that plugs into any single Hex slot of a PDP-11 processor. The various configurations include 56, 84 and 112MB of storage. A second drive can be mounted in the same drawer for up to 224MB. The DSS 1300 controller can handle two DSS 1300 for a total storage capacity of 448MB. Priced 50 to 60% below DEC list in OEM qty. **Cynthia Peripheral Corp,** 3606 W. Bayshore Rd, Palo Alto, CA 94303.

Circle 149

MINICOMPUTER SYSTEM

Designed To Advance UNIX State-Of-The-Art

The P/40 is a 16-bit commercial UNIX-based system for use in business/computational-intensive application environments in which ease of program development and software transportability are important. Its Compatible Base Architecture gives users instant compatibility with all existing computer systems that run the Bell Laboratory-licensed UNIX. This multi-user minicomputer system uses C as its fundamental programming language and can support up to 24 simultaneous users. It provides up to 1MB of main memory using 16K RAM memory technology and up to 580MB of disk storage. Using C, P/40 users can readily transport their application programs from one UNIX-based system to another. It



incorporates the Multibus peripheral controller to optimize data transfer rates and gives users many compatible, readily available peripheral devices to choose from. A typical 8-user P/40 system, consisting of a central processor with 512 kB of main memory, 72MB of disk storage, an 8-channel intelligent communications controller, and 9-track magnetic tape unit, is $49,500. A UNIX license is $5000. **Plexus Computers Inc,** 2230 Martin Ave, Santa Clara, CA 95050.

Circle 142

VIDEO DESKTOP ENCLOSURES

Provides Ability To Create LSI-11/2 Or -11/23 Workstations

The NET-PAC 95 provides video features similar to the DEC VT-100 with systems options over the VT-103. It is an 80-column video enclosure with an 8 quad, 16 dual height Q-bus backplane capable of housing 5-1/4" dual floppies or micro Winchester disks, +5 and +12V internal power supplies, and a detachable keyboard. Also included are a complete self-test capability on power up, and a field proven linear power supply. $3000 including 12" diagonally measured video display, a detachable VT-100 compatible keyboard, a full 8 quad slot (16 dual height) backplane assembly, front panel switch group, internal linear power supplies (+5V, +12V), internal cooling and RS-232 serial port. **Netcom Products Inc,** 430 Toyama Dr, Sunnyvale, CA 94086.

Circle 160

New Products

PERSONAL COMPUTER

Lowest Cost System Available

Measuring just 6 × 6.5 × 1.5 inches and weighing 12 ounces, the ZX81 uses a new master-chip which replaces 18 chips in the ZX80 and adds important new circuitry. It

has a powerful 8k Basic ROM enabling operation in decimal arithmetic with full scientific functions. Also available is a range of cassette-based software. Features include single stroke key-word entry, powerful edit facilities, automatic syntax checking of every statement line and a 24 line by 32 character display. It can also operate in 2 software selectable modes, Fast and Normal. In Normal the ZX81 will both compute and display simultaneously which allows continuously moving, flicker-free graphics. $149.95; $99.95 in kit form. The ZX Printer is available for under $100. **Sinclair Research Ltd,** 2 Sinclair Plaza, Nashua, NH 03061. **Circle 167**

COMMUNICATIONS SYSTEM

Provides IBM SNA Support For DS990 Computers

The Distributed Network Communications System (DNCS) software, provides a means to offload the host mainframe and implement distributed processing. It provides communications between a DS990 system and an IBM host computer and allows DS990 system VDTs to emulate a 3278 display station, permitting users to interface DS990 application programs with SNA software. DNCS is based on a building-block approach in which computing resources may be added when and where they are needed. It handles up to 8 of TI's Four Channel Communications Controllers (FCCC). Each FCCC can handle up to 4 communications lines, its maximum aggregate line speed is 19.2K bps. Future releases will support the international X.25 packet switching network architecture and a family of remote communications terminals. Software license is $5500 to $7100. **Texas Instruments Inc,** Box 202146, Dallas, TX 75220. **Circle 168**

GENERAL PURPOSE KEYBOARD

Custom Features in Off-The-Shelf Model

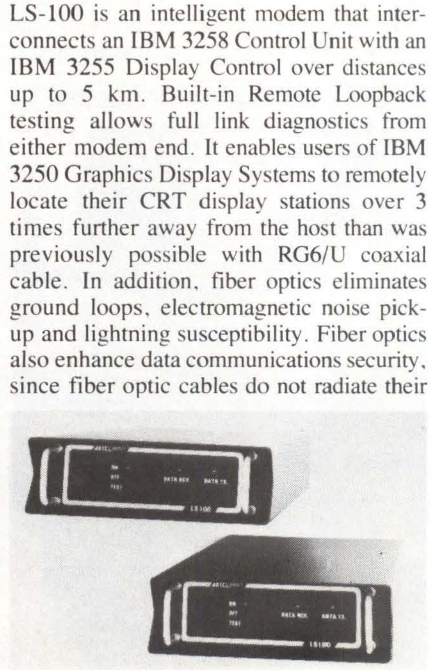
The KS99 is a 74-key alphanumeric keyboard. An EPROM enables it to be pro-

grammed for a variety of uses, such as in business computers and word processing systems. It is intended for low-volume users who want the performance of Digitran's keyboards without paying for special engineering and tooling. Features include a patented moving-plate capacitor, a patented tease-proof switch detection circuit, a single-piece unitized frame that is impervious to moisture and dust, bounceless keyswitch operation, and an advanced μP. The KS99 has numeric, function and cursor pads, alternate action, and series or parallel output. It is ASCII encoded and TTL compatible. It has automatic repeat keys, N-key rollover, and stepped, sculptured keytops. $129.95 (1-99); $99.95 (100 or more). **The Digitran Co,** 855 S. Arroyo Pkwy, Pasadena, CA 91105. **Circle 134**

FIBER OPTIC MODEM

Fiber Optic Industry's First IBM-Compatible Data Transmission System

LS-100 is an intelligent modem that interconnects an IBM 3258 Control Unit with an IBM 3255 Display Control over distances up to 5 km. Built-in Remote Loopback testing allows full link diagnostics from either modem end. It enables users of IBM 3250 Graphics Display Systems to remotely locate their CRT display stations over 3 times further away from the host than was previously possible with RG6/U coaxial cable. In addition, fiber optics eliminates ground loops, electromagnetic noise pick-up and lightning susceptibility. Fiber optics also enhance data communications security, since fiber optic cables do not radiate their

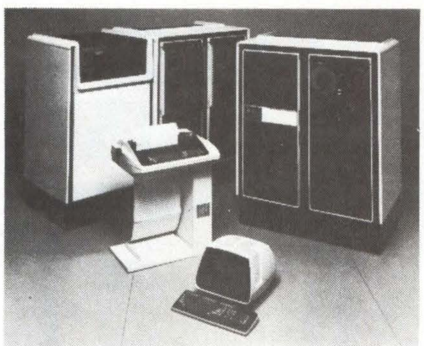


signals. **Artel Communications Corp,** Box 100, West Side Station, Worcester, MA 01602. **Circle 128**

32-BIT COMPUTER

New Mid-Range Eclipse MV System

A general-purpose computer for both commercial and scientific applications, the ECLIPSE MV/6000, stores up to 2 million characters of information in main memory and can access up to 4 billion characters using virtual memory. In addition, 2 new Winchester-type magnetic disk subsystems offer 73MB and 147MB of mass storage. The new computer accommodates up to 64 user terminals. It operates DG's 32-bit system software — the Advanced Operating System/Virtual Storage (AOS/VS). The system also runs their entire library of 32-bit commercial and scientific programs and utilities, including COBOL and FORTRAN, DG/DBMS database management software, TRENDVIEW graphics display software, word processing software, and other programmer and end-user productivity aids. It also operates all DG's communications products, including the XODIAC network management software, based on the X.25 worldwide standard, and the IBM SNA-compatible communications product, DG/SNA. A small ECLIPSE MV/6000 system configuration with 1MB of main memory, 1600-bpi streaming tape drive, 73MB sealed-media disk subsystem, system display console, 16 DASHER display terminals, one intelligent async controller, 300 lpm printer subsystem, initial license for AOS/VS (including software support services) is $172,000. **Data General Corp,** 4400 Computer Dr, Westboro, MA 01581.



Circle 132

256 AND 512 kB MEMORY

Add-In Cards For VAX 11/750 And PDP 11/70

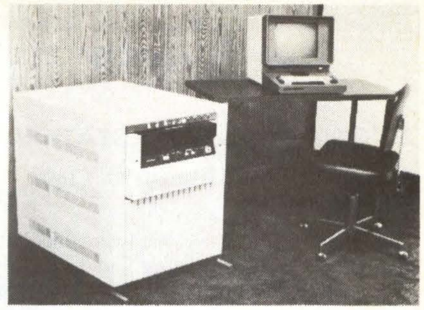
The MU-5750-256 and MU-5750-512 are direct substitutes for DEC products, offering full hardware and software compatibility and an on-line, off-line switch for easy maintenance. The 256kB size is similar to the DEC product. The 512kB size gives additional reliability with an MTBF 1.5 to 2.0 times longer than 256kB equivalents. The products can be covered under any of 5 service plans, including turn-key service for both installation and servicing. The MU-5750-256 is $1500; the MU-5750-512 is $2315; qty discounts avail. **Intel Corp,** Memory Systems Operation, 1302 N. Mathilda Ave, Sunnyvale, CA 94086.

Circle 158

32-BIT MINICOMPUTER

Entry-Level MEGAMINI Series 3200

Model 3210 is a small, cost effective system for both technical and business computing environments. When integrated with Reliance commercial software for transaction processing, the 3210 provides complete facilities to develop business application programs. It is packaged in a low profile 30" cabinet and can address up to 4MB of main memory and support up to 32 users running a variety of large, complex application programs. The basic configuration includes 512kB of MOS memory, system console, power supply with battery backup, 27MB cartridge disk drive, selector channel, and disk controller; $49,900. **Perkin-Elmer Corp,** 2 Crescent Place, Oceanport, NJ 07757.



Circle 162

New Products

ENGINEERING WORKSTATION

Computer-Based System With 1MB Of Memory

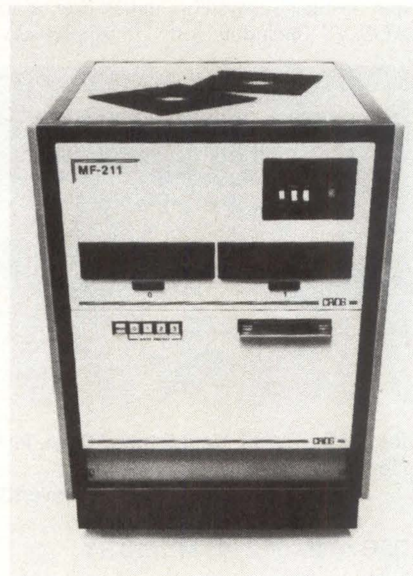
The workstation allows hardware and software development, testing and laboratory applications, technical manual preparation and documentation control in one compact engineering workstation. Each workstation consists of a desktop display and detachable keyboard. Mass storage and electronics are located in a compact floor-standing module that fits under a desk. Up to 16 workstations can be combined on a plug-in basis. For central data base access, individual workstations or clusters of workstations can communicate with a mainframe to upload or download large-scale programs or data bases. For hardware development, it offers 5 IEEE 796 standard Multibus slots for linking and testing of peripherals and instruments. The engineering workstation with 128kB of RAM, 10MB of Winchester and 1/2MB of floppy disk storage is $22,500; OEM qty discounts avail. **Convergent Technologies,** 2500 Augustine Dr, Santa Clara, CA 95051.

Circle 150

LSI-11/23 PACKAGE

Offers Winchester Disk And Choice of Software

The MH-11 is built around DECs LSI-11/23 central processor and offers complete DEC software compatibility, one-stop procurement, compact packaging and economical prices. The Winchester disk has a 20.8MB capacity and is software equivalent to 4 DEC RL01 disk units. A cartridge tape backup unit is optional. The MH-11 with 128kB of memory, 4-port serial interface, 20.8MB Winchester, dual double-density floppy disk drives and 30″ office-style enclosure is $16,000. **Charles River Data Systems Inc,** 4 Tech Circle, Natick, MA 01760.



Circle 151

ENCLOSURES

For 8″ Floppy And Winchester Disk Drives

Horizontal-mount, 3 piece, all aluminum enclosures for single or dual floppies (5 1/4″ height); or Winchester, floppy, and controller combination (7″ height). Available in 19″ rack mount or table top models. Complete package includes power supply, fan, cords, switch, fuseholders and wiring harness. Empty cabinets and kits are also available. **Axis Inc,** 4706 Ruffner St, Suite B, San Diego, CA 92111. **Circle 127**

TOUCH SENSITIVE CRT

Easy Information Retrieval By Non-Data Processing Personnel

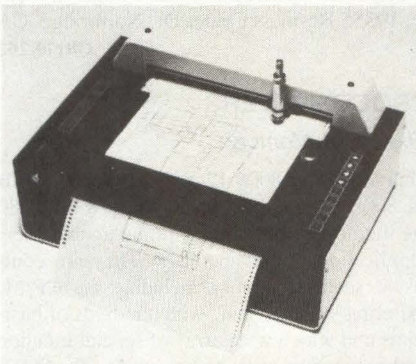
Model 40's touch sensitive screen has 80 discrete touch positions. Its 12″ diagonal, non-glare, screen has a format of 24 lines by 80 characters, and a character set with 128 displayable ASCII codes. The screen also has 5 display modes which can be used in any combination. The terminal uses an RS-232C interface, and has a transmission speed up to 9,600 bps. With the Touch Command Terminal, users are not required to learn special codes or have typing or data processing skills. **A.R. Shaw,** 10800 Lyndale Ave. S, Bloomington, MN 55420.

Circle 146

11″ DRUM PLOTTER

With Broad Array Of Interfaces

With 5 different format configurations, the COMPLOT CPS-20 one pen 11″ drum plotter is a single machine that can be easily interfaced to virtually any computer in the marketplace. High efficiency, very effective dampers assure ultra quiet operation and smooth plotting in practically all environments. New touch type controls are conveniently mounted atop the housing. Swapping a single interface board is the only alteration needed for use with different computers. Operation is 3 ips at a resolution of .005″ with plots as long as 144 feet. Metric versions are also available. From $3995. **Houston Instrument,** One Houston Square, Austin, TX 78753.



Circle 137

DEC-COMPATIBLE CONTROLLER

For 5-1/4″ 96 TPI Minifloppy Disk Drives

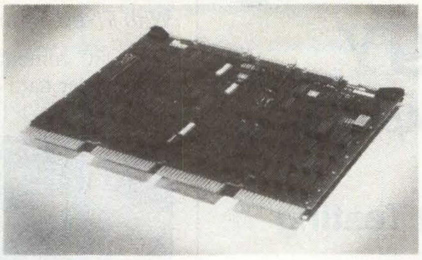
The DSD 4120 emulates DEC RX02 subsystems by making the 5¼″ floppy drives appear to the computer as single-sided 8″ floppy drives. DEC software and applications programs can now run on 5¼″ floppy drives with no modification. The 4120, on a single dual-wide card, supports up to two 5¼″ minifloppy disk drives providing 1.2MB of formatted storage capacity. Shugart's SA460 double-sided, double-density 96 tpi and Tandon's T-100-4 minifloppy disk drives are also supported. $1250, OEM discounts avail. **Data Systems Design Inc,** 2241 Lundy Ave, San Jose, CA 95131.

Circle 152

μP WINCHESTER CONTROLLER

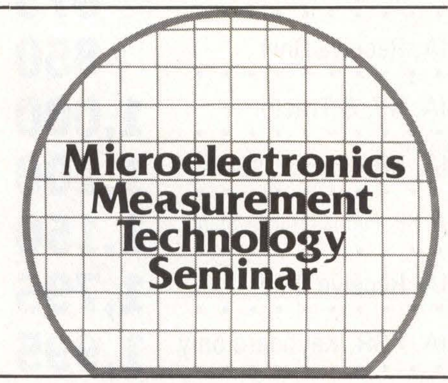
Interfaces 2 Seagate Compatible Drives With LSI-11

The DQ604 interfaces 2 Seagate ST506 or ST512 compatible drives with RL01/RL02



emulation to LSI-11 systems. The quad size board plugs into a single Q-bus slot for minimum space and power requirements. It runs under the RT-11 and RSX-11 operating systems using standard DEC RL01/RL02 drivers. A format diagnostic routine is supplied with each controller. Other features include an on-board multiple device hardware bootstrap, bad sector mapping when formatting, automatic flawed media compensation for hard errors on the disk, automatic read retry for soft errors, and full sector data buffer to eliminate DMA latency. $2050. **Dilog,** Distributed Logic Corp,12800 Garden Grove Blvd, Garden Grove, CA 92643.

Circle 135

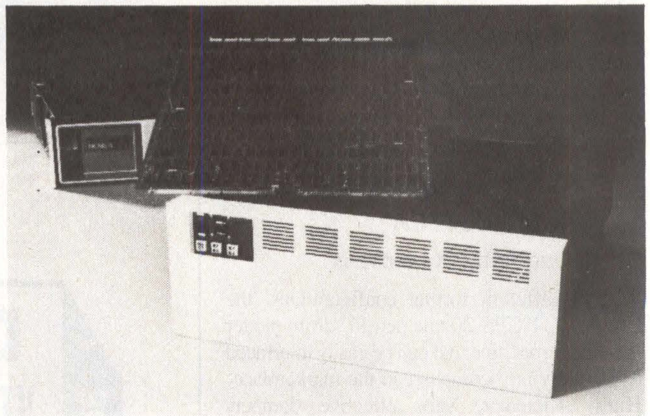


New Products

WINCHESTER SUBSYSTEM

With Fixed-Head Option

The Q80 combines a single-board disk controller with an 80MB Winchester hard disk drive. Using IBM 3340-type disk heads, the drive features a fast data transfer rate of 1MB/sec and an average

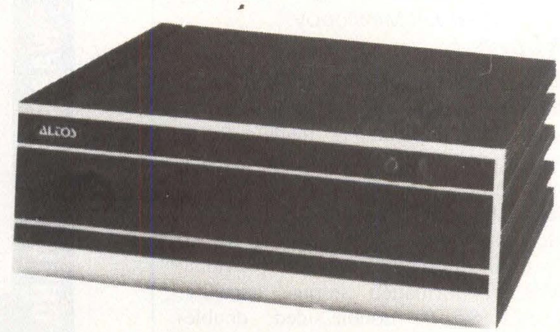


access time of 38 ms. Up to 2.4MB of additional storage is available with the fixed-head option at a faster access time of 10 ms. The disk controller, Model 6010, features PROM-controlled microinstructions and contains 9 programmer-accessible registers for minimum DMA and driver overhead. It also includes an 18-word FIFO buffer. The total package is designed for DG Nova, Eclipse and emulating computers at one-third the cost of comparable DG equipment. The subsystem is $8000, the fixed-head option adds under $4000. **Quentin Research Inc,** 19355 Business Center Dr, Northridge, CA 91324. **Circle 163**

MULTI-USER MICROCOMPUTERS

Expanded Integral Fixed Disk Memory

Using Winchester technology, the 8000-12 system offers 20MB storage capacity and the 8000-14 provides 40MB. These 8-bit, Z-80 systems have 4 separate memory partitions permitting up to 4 users to perform different applications simultaneously. They are compatible with an extensive software library including the CP/M, MP/M, and OASIS operating systems; and, with hundreds of business application programs and with a wide array of special function software including data base management and graphics. The 8000-10 family features 208kB of internal RAM memory (48K per user), 6 programmable RS232 serial ports, a parallel port, and a communications port to handle network data rates up to 800K baud. Additional 20MB disks can be added to the 8000-12 for a total disk system capacity of 40MB; and, 40MB disks can be added to the 8000-14 for 80MB of hard disk storage. The 8000-12 is $9990 with



floppy disk, and $12,500 with magnetic tape cartridge backup. The 8000-14 is $11,990 with floppy disk, and $14,500 with tape backup. **Altos Computer Systems,** 2360 Bering Dr, San Jose, CA 95131. **Circle 145**

Designers' Notebook

Print Heads Key To Print Quality

Print heads establish serial, dot-matrix printer print quality. Two factors influence print head performance: electro-magnetic design and print needle configuration.

Characters are formed by the impact of the print needles on an inked ribbon and paper. The needles are housed within the print head and are actuated by circuitry within the printer. The number of needles and their spacing determines the aesthetic quality of printing.

Regardless of print needle configuration a matrix print head moves at a uniform horizontal velocity across the paper. Needles are actuated by timing signals synchronized with the movement of the print head. The print needles in most dot-matrix printers are activated "on the fly," that is, as the head is moved across the paper. In contrast, with daisywheel printing, the carriage is stopped momentarily when printing is performed.

The first widely used dot-matrix print heads used seven needles arranged in a vertical row. This provides characters that fit within a matrix that is five dots in the horizontal and seven in the vertical direction.

With an industry standard of 10 cpi, the typical 5×7 dot-matrix allows a one-dot intercharacter space and a five-dot character width. In a variation, some manufacturers use only four horizontal dots for upper case letters T, E, H, F and L while maintaining the same 10 cpi density. This speeds character printing, but results in a visible clear space between dots.

The next generation of dot-matrix printers went to a nine-needle print head, which provides the capability for character descenders and underlined characters.

A further enhancement in character appearance is obtained by interlacing. In this technique, the character width remains five dots, but four dots can be interlaced above or below. Although this provides nine possible printable dot positions on any horizontal row, adjacent dots cannot be printed closer than one dot interval apart.

Interlaced dots produce smoother characters, particularly with curved and diagonal lines within the character. This is referred to as a 9×9 dot matrix.

Aesthetic appearance of dot-matrix characters is now getting another boost by going to an 18-needle print head, consisting of two vertical rows of nine needles that are offset from each other. This can print up to 18 overlapping dots in the vertical dimension with one horizontal print head pass.

Similar-appearing characters can be generated by making multiple passes of a nine-needle print head: up to nine dots are printed in the first pass; the paper is moved vertically a small amount; another pass adds another nine dots displaced slightly from those of the first pass; and this process is repeated until the required number of overlapping dots is produced.

The single-pass, 18-needle head has a faster character throughput than the two-pass, nine-needle printer. Also, the print load in 18-needle print heads is shared almost equally between two groups of nine needles. Actual mechanical wear, compared to a nine-needle head, is greatly reduced for a given number of characters printed.

A potential problem with the multiple pass technique is the difficulty in obtaining good registration between dots printed from pass-to-pass. This approach requires a carefully controlled paper movement during small, incremental shifts from one pass to the next, which increase the cost of the print mechanism. To provide good printing quality, tighter tolerances than that of a single-pass system must be built into the print head drive system and maintained over equipment life.

print head details

The drive mechanism for a single print needle consists of a U-shaped sintered iron-core electromagnet with a pivoted clapper (lever arm) and the print needle. To obtain the appropriate print quality, the needle is made of tungsten and has a carefully polished face that makes contact within the ribbon.

One example is the ballistic print head. At rest, the end of the needle and clapper are in contact. When a current pulse is applied to the coil, the electromagnet pulls the clapper down and pushes the print needle down toward the ribbon and paper. Then the needle strikes the ribbon, paper and printing surface and rebounds back to its rest position.

With the ballistic approach, the clapper seats or stops before the needle strikes the print surface. Thus, the needle is in free flight when it strikes the print surface. The clapper and the needle return to the rest position at the same time after the clapper energizing current has decreased.

In a non-ballistic head, the needle is driven into the print surface by the clapper. Here, the clapper always maintains contact with the end of the needle; this is usually referred to as printing in the "crush" mode.

The ballistic approach has less physical contact between the needles and the clapper; there is less wear in the drive mechanism and greater print head life.

print head performance

Another factor affecting print head performance is the current energizing the electromagnet. For optimum performance, the current pulse is carefully shaped to provide the proper match with the magnitude and overshoot. Power dissipation is minimized at maximum operating frequency.

Factors influencing overall performance and upper frequency limit of dot-matrix print heads include, most importantly, print gap (distance the needle travels to strike the print surface).

Most true ballistic print head printers employ a user-adjustable gap, allowing a wide variety of paper thicknesses (usually up to five copies). This overall print head system is carefully tailored to allow a reasonable and practical range of gap settings, so users need not set gaps precisely.

by Anthony B. Lappas

Anadex, Inc, 9825 DeSoto Ave, Chatsworth, CA 91311

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