

COMPUTER DESIGN

JUNE 1968

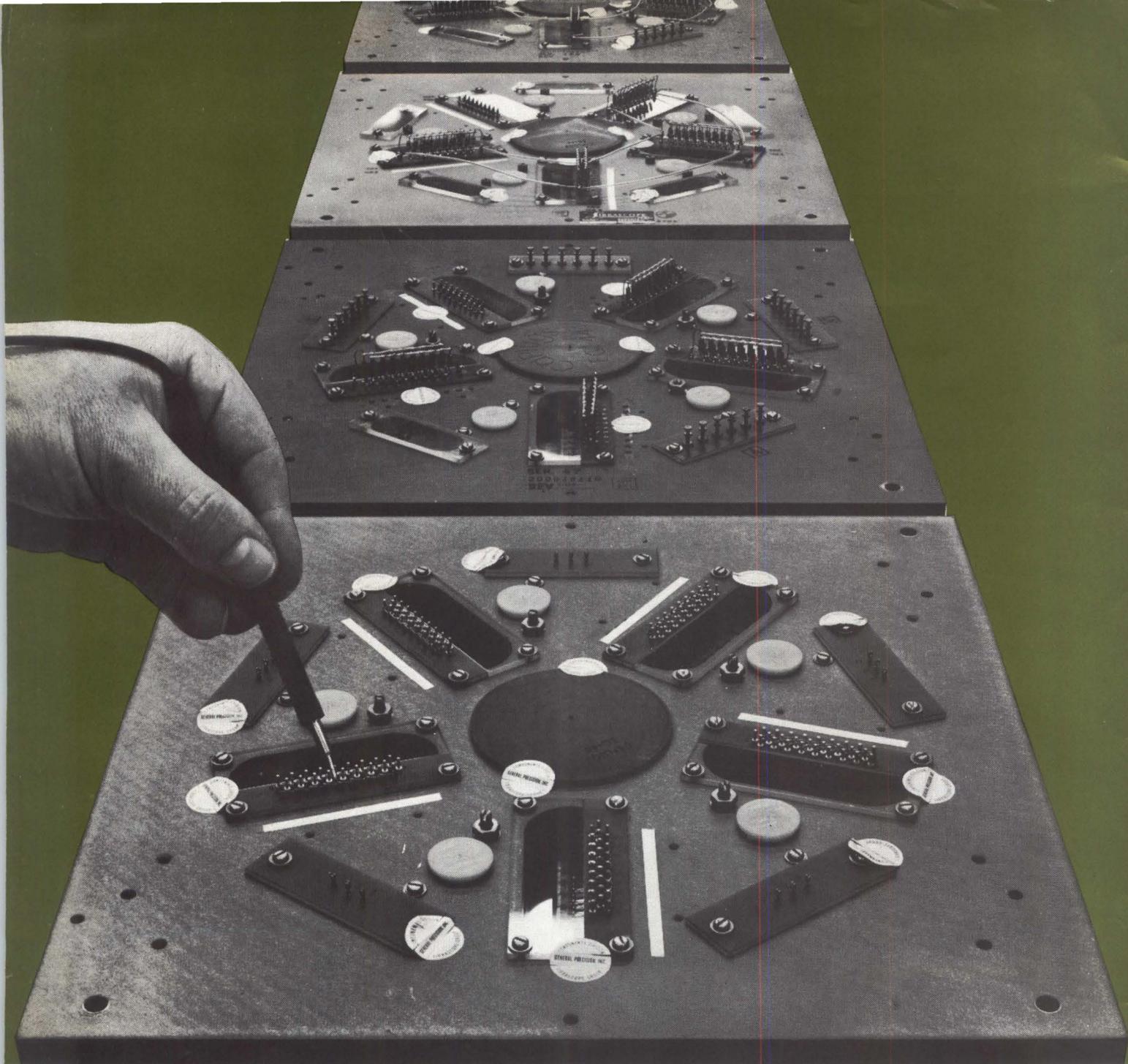
THE MAGAZINE OF
DIGITAL ELECTRONICS

The Applications and
Implications of LSI

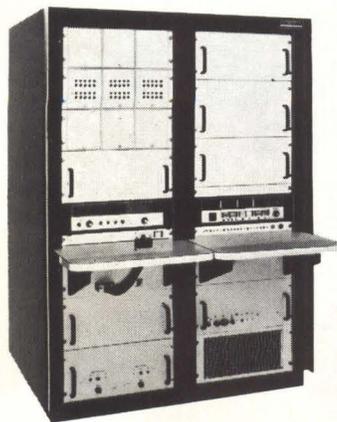
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Fairchild has these fond memories of Librascope



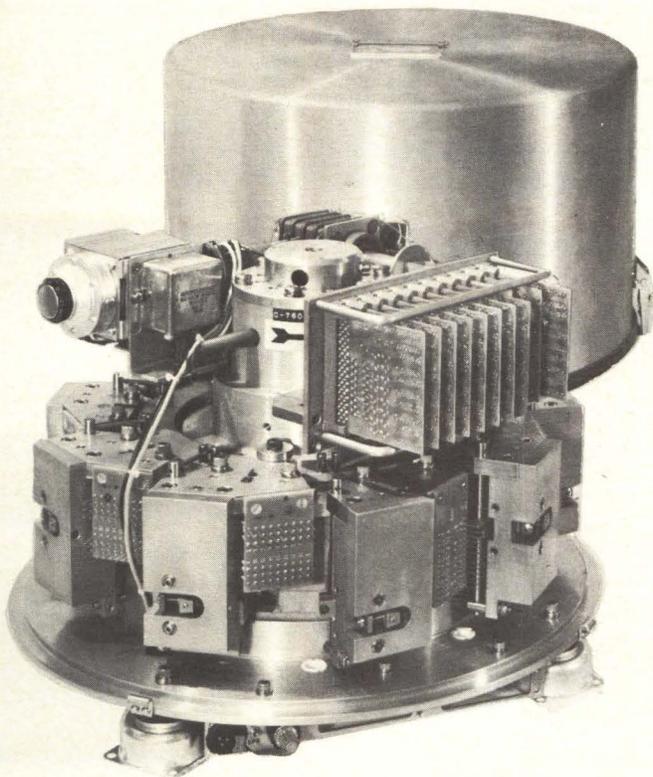
Unlimited programmed testing with flexible test sequencing is one reason why. That's the advanced state-of-the-art job called for by the programming unit of Fairchild's new Series 4000M Automatic Integrated Circuit Testing System. Librascope's Series L100 Disc Memory got the call. Each stores 900 test programs—grouped in sequences of 25—and runs up to 60 per second. The same testing line accepts a variety of devices for high-speed processing. A simple keyboard programs the disc—no accessory hardware needed. And an entire sequence is reprogrammed in minutes. Proven reliability (over 600 L100 units in use) stems from conservative, no-compromise design. Yet the L100 is probably the lowest-cost disc memory on the market.

Thanks for the memory order, Fairchild—reputations are made of this. For the brochure detailing the longest line of discs in memory, write: General Precision, Inc., Librascope Group, Components Division, 808 Western Avenue, Glendale, California 91201.

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... in a 17½" diameter by 12⅝" high dusttight package, including all electronics required for head selection, writing and reading data. Get the intriguing performance details on our brand new high-density 1004S Drum Memory option in Bulletin TIB-6803.

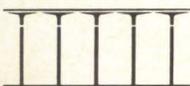
And while you're at it, check out the tremendous versatility of the entire VRC drum line, covering a storage range of 328,000 to 64,307,200 bits, in five standard packages. Ask for 12-page brochure DB-6803.

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COMPUTER DESIGN

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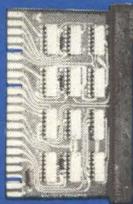
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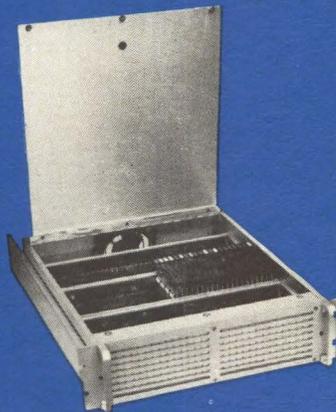
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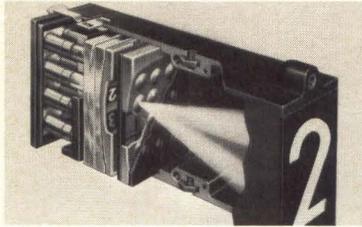
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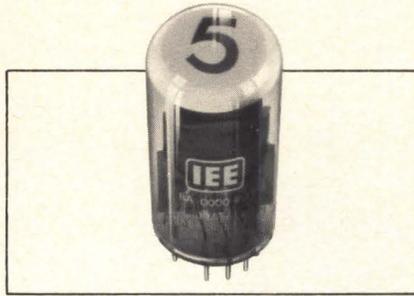
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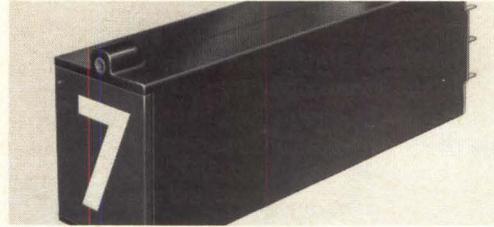
Quick guide to bright, legible, wide angle readouts



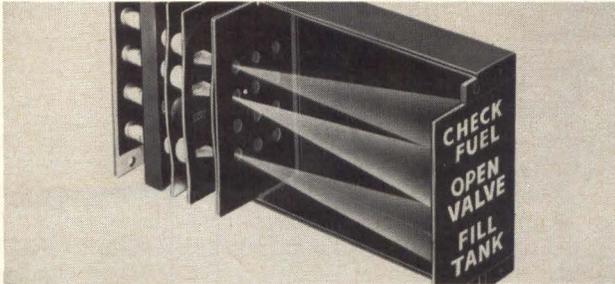
Series 360H Displays 2" high characters easily read from over 50'. Yet unit is just 3" H x 2" W x 7.75" D. New lens system provides bright, crisp display.



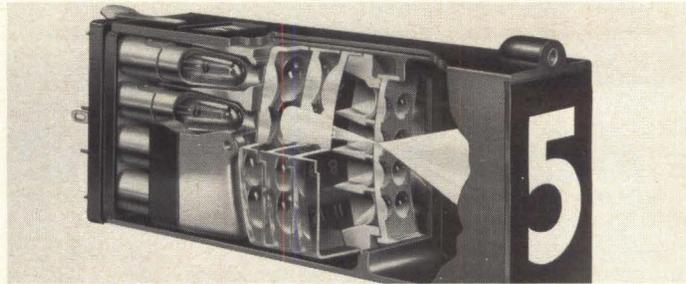
CRT Display 10-gun CRT projects single-plane digital or word displays onto fluorescent screen. Easy reading, even in direct sunlight. Wide viewing angle. Ideal for instrumentation applications.



Series 160H Exceptionally large viewing area (1.56" H x 1.12" W for overall size). New lens system increases character brightness; reduces chance of reading error. Message lines may be displayed simultaneously with symbols.



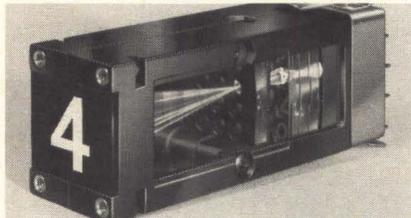
Series 80 Large screen unit particularly suited for annunciator applications . . . factory call systems, production control boards, etc. Message or character 3 $\frac{3}{8}$ " high; can easily be read at 100', 160° viewing angle.



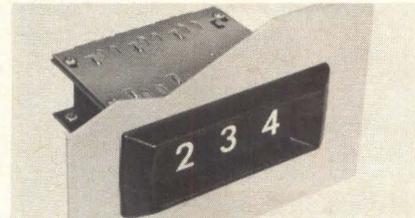
Series 10H World's most popular readout. And we've improved it. Double condensing lens provides exceptional character brightness. Greater clarity at wider angles and longer distances, even under high ambient light. .937" H x .937" W viewing area. Mil-spec version available.



Series 345 IEE's smallest rear-projection readout. Viewing area .38" H x .34" W. Based lamps. Low cost. Individual readouts plug into permanently wired housing for quick message change. Easy front panel access.



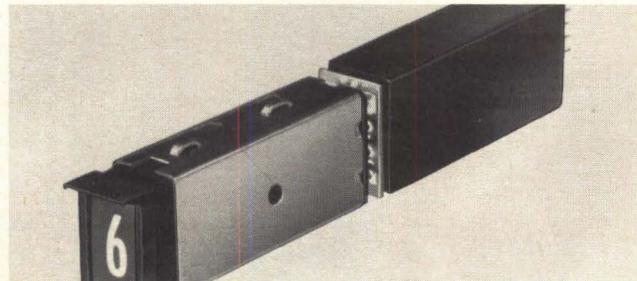
Series 120H Miniature (.62" H x .62" W) rear-projection readout. New lens system increases character brightness 50%. Easily read from 30' even with high ambient light. Quick disconnect lamp assembly for speedy lamp replacement.



Series 220H Miniature, plug-in, rear-projection readout meets MIL-R-39027. .62" H x .62" W viewing area. Special lens system increases character brightness 50%. Excellent readability from wide angles and long distances.



Series 875 Miniature, 24-position, rear-projection readout with .62" H x .62" W viewing area. Overall size just 1.39" H x .90" W x 3.095" D. Exceptional character brightness and clarity. Quick disconnect lamp assembly for easy replacement.



IC Driver/Decoders Small, solid-state units for IEE Series 10H, 120H, 220H, 340 and 360 readouts. All models accept a variety of binary codes for decimal conversion. Take normal signal voltage. Draw less than 2 ma. (Many options, including memory.)

Any characters desired. Any colors or combinations. Any input, BCD or decimal. Any input signal level. Any mounting, vertical or horizontal. Many sizes. Many configurations. Many options and accessories. Many brightness choices. Long lamp life (to 100,000 hours).



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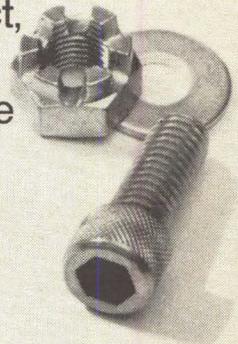
CIRCLE NO. 4 ON INQUIRY CARD

COMPUTER DESIGN/JUNE 1968



**Computers are big, expensive components.
Bit for bit, ounce for ounce, some are a bargain.**

When you tie another man's computer into your product, you're staking your reputation on his equipment. Your reputation is worth shopping for. Naturally you want the most for your dollar. Like reliability at 130° F. Hewlett-Packard computers are designed for rugged dependability—as well as high performance. All things considered, they're something of a bargain.

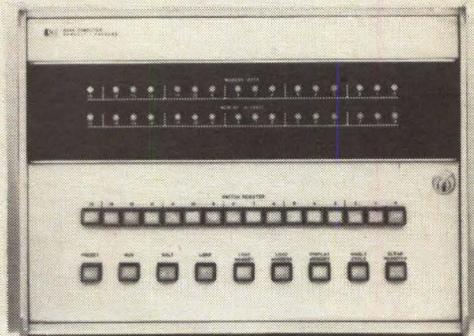


We've been selling quality instruments to original equipment manufacturers for years. We know the problems. So we back our computers with excellent training, complete service and our traditional warranty. We'll train your people or your customer's people in maintaining the computer and in using the software.

We supply plug-in I/O interfaces and the software drivers for peripheral devices. You buy only the equipment you need for interfacing your system. And you tie it in with minimum engineering time because both hardware and software are operational and fully documented.

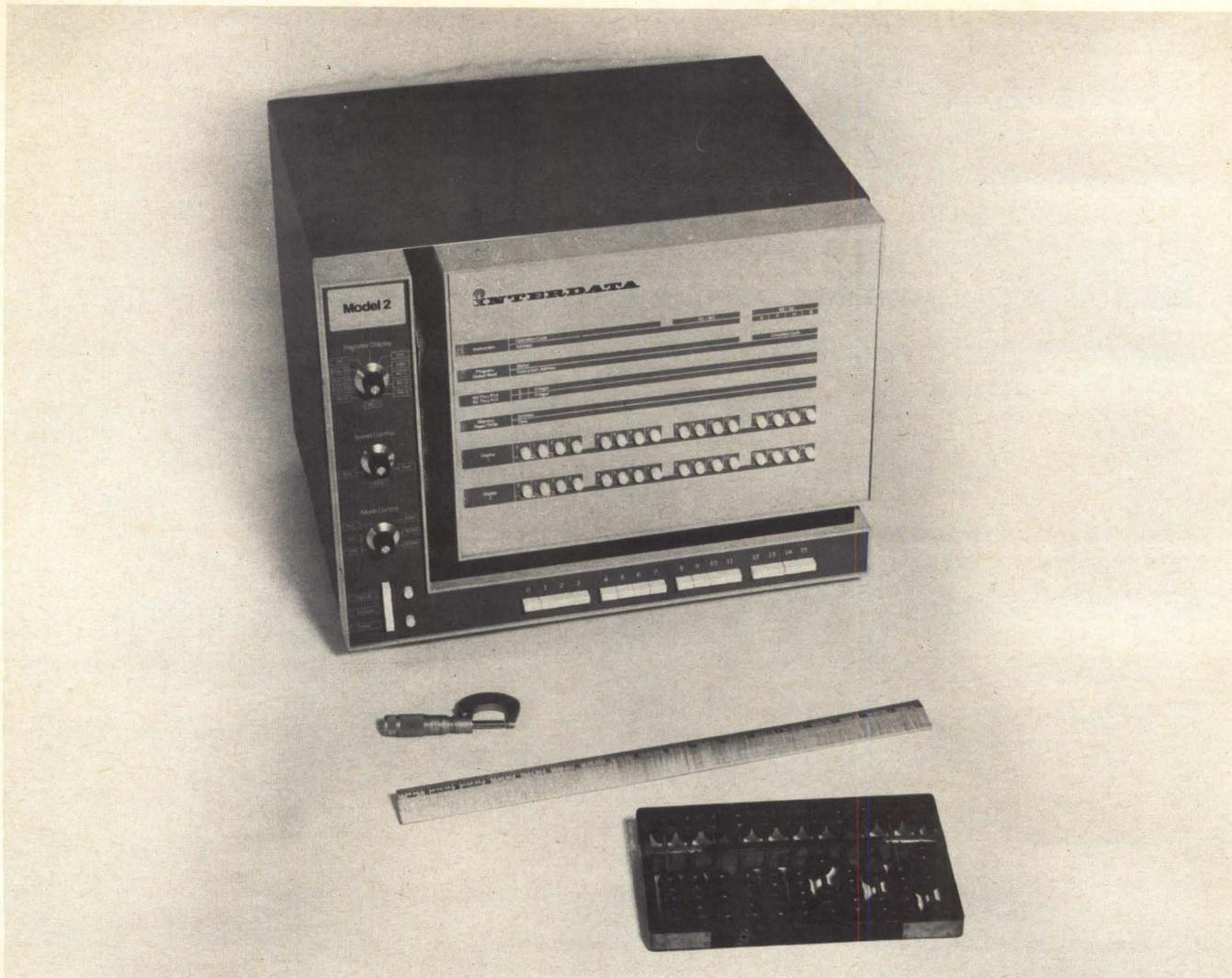
The 2114A pictured here measures 16¾" x 12¼" x 22½" including its power supply. It uses 16-bit words, operates with 4K or 8K memory, and has a two micro-second cycle time. Price: \$9,950.

For more information about a computer that will live up to your reputation, call your local HP field engineer. Or write Hewlett-Packard, Palo Alto, California 94304; Europe: 54 Route des Acacias, Geneva.



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- Speed: 1.8 μ s memory cycle time; 3.9 μ s add time on Model 4, 35 μ s on Model 3.
- Interrupts: priority system for up to 256 devices; status and device number obtained without polling.
- Addressability: directly to 65, 536 bytes of core memory with indexing; no paging required.
- Arithmetic: 16 general registers for arithmetic operations; optional hardware multiply/divide and floating point instructions.
- Data Transfer: direct to memory a byte or block at a time; cycle stealing access to memory by byte or halfword.
- Peripherals: selected for reliability and performance; quality conversion equipment and system modules.
- Expandability: in the field and upward between models; our measurements are modular.
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- Software: assembler, program diagnostics, math library; plus the new dimension of interactive FORTRAN.
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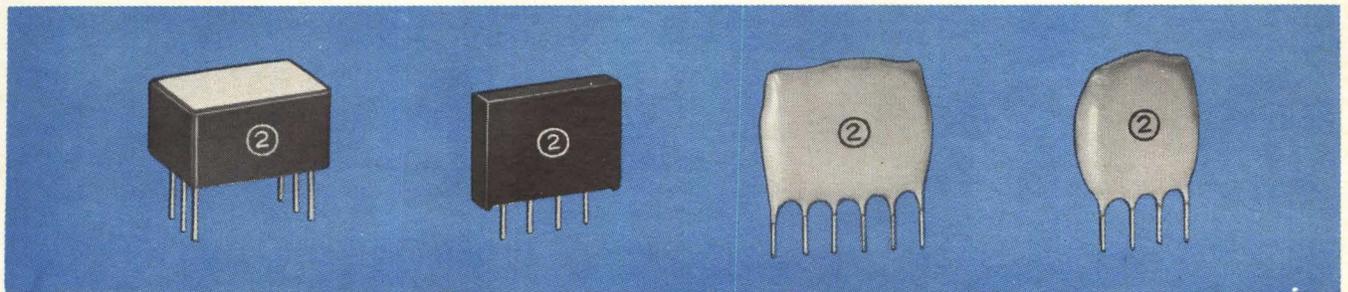
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Some of the case styles in which Sprague DST Pulse Transformers are available. Note the in-line leads.

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<p>August 12, 1968</p>	<p>August 19, 1968</p>	<p>August 26, 1968</p>	<p>September 2, 1968</p>	<p>September 9, 1968</p>	<p>September 16, 1968</p>	<p>September 23, 1968</p>	<p>September 30, 1968</p>

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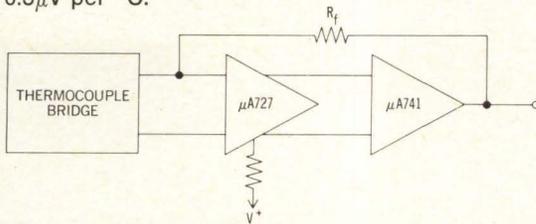
μA727
TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMP

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μA741
FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER

THERMOCOUPLE BRIDGE AMPLIFIER

By combining new products #29 and #31, you have the basis of a very low-drift amplifier for low-level transducers and precision analog computers. In fact, four components (two new linear integrated circuits plus two resistors) are all you need to produce a thermocouple bridge amplifier with a closed loop gain of 1000, accuracy of 0.01%, input resistance of 300 Megohms and temperature drift of $0.3\mu\text{V}$ per $^{\circ}\text{C}$.



Key Features:

Temperature Drift	$0.3\mu\text{V}/^{\circ}\text{C}$
Closed Loop Gain	1000
Gain Accuracy	0.01%
Input Resistance	300 MΩ

New Product #29 is the μA727 temperature-controlled differential preamp. It's held at a constant temperature by active internal regulator circuitry.

As a result, it can provide:

$\Delta V_{OS}/\Delta T = 0.6\mu\text{V}/^{\circ}\text{C}$	$R_{in} = 300$ Megohms
$\Delta I_{OS}/\Delta T = 2\text{pA}/^{\circ}\text{C}$	$V_{CMR} = \pm 13\text{V}$
$I_{OS} = 2\text{nA}$	$V_{in} = \pm 10\text{V}$

New Product #31 is the μA741 frequency-compensated operational amplifier. It has internal frequency compensation built directly on the chip

(that eliminates the need for external stabilization components). The μA741 is a successor to the μA709 and a pin-for-pin replacement for it. Key μA741 features include:

- short-circuit protection
- adjustable input offset voltage
- no latch-up when the common mode voltage range is exceeded

$V_{in} = \pm 30\text{V}$	$R_{in} = 1\text{M}\Omega$
$I_{OS} = 30\text{nA}$	$V_{out} = \pm 13\text{V}$
$V_{OS} = 1\text{mV}$	$V_{CMR} = \pm 15\text{V}$
$A_{VOL} = 200,000$	$P_{DISS} = 5\text{mW}$

This is only one of many applications possible with the μA727 , μA741 and other new linear ICs from Fairchild. The coupon below will get you a whole package of applications information including schematics, parts lists, and individual data sheets.

Please send me the Linear IC Applications Pack.

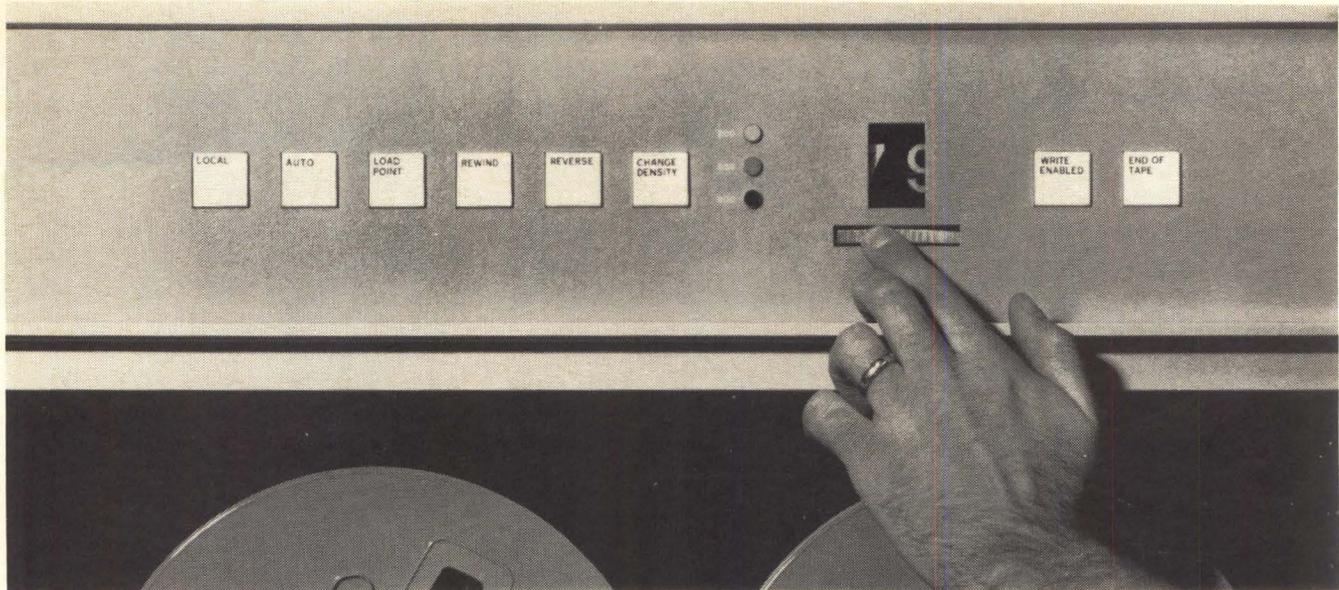
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digital tapes?**

**Change
tape formats
with one
finger**

A single tape unit that reads both of the industry-standard digital tape recording formats—with format selection at the flip of a switch. You no longer need *two* tape units for those installations processing computer-written tapes; include a Hewlett-Packard READ/READ Tape Unit that will read *both*.

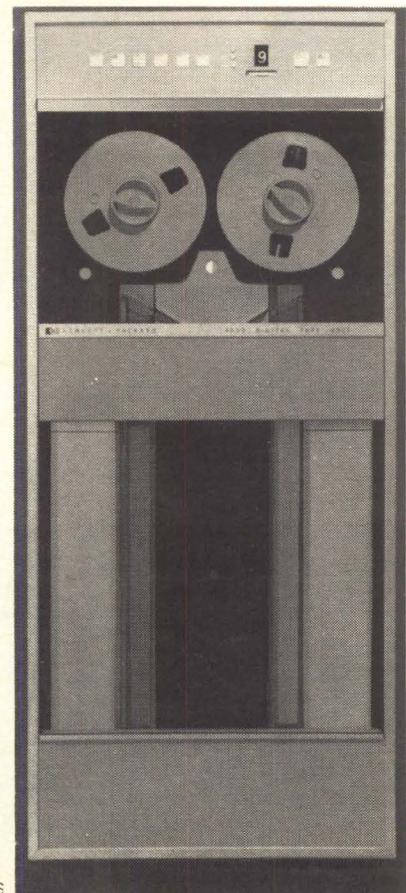
Think of the savings this offers in the design and production of *your* digital system—and the flexibility you'll be able to offer the *user*.

Your choice of tape units for READ/READ operation may be either the 3030 Series with tape speeds to 75 ips, or the 2020 Series offering the optimum in economy of tape speeds below 45 ips.

Other tape units in the 2020 and 3030 Series class offer single-format capabilities for both writing and reading.

Whatever your application, the flexibility of Hewlett-Packard's 2020 or 3030 Series Digital Magnetic Tape Units can provide a tape unit with the optimum configuration to interface to *your* digital system.

For more details, call your local HP field engineer or write Hewlett-Packard, 690 Middlefield Road, Mountain View, California 94040.

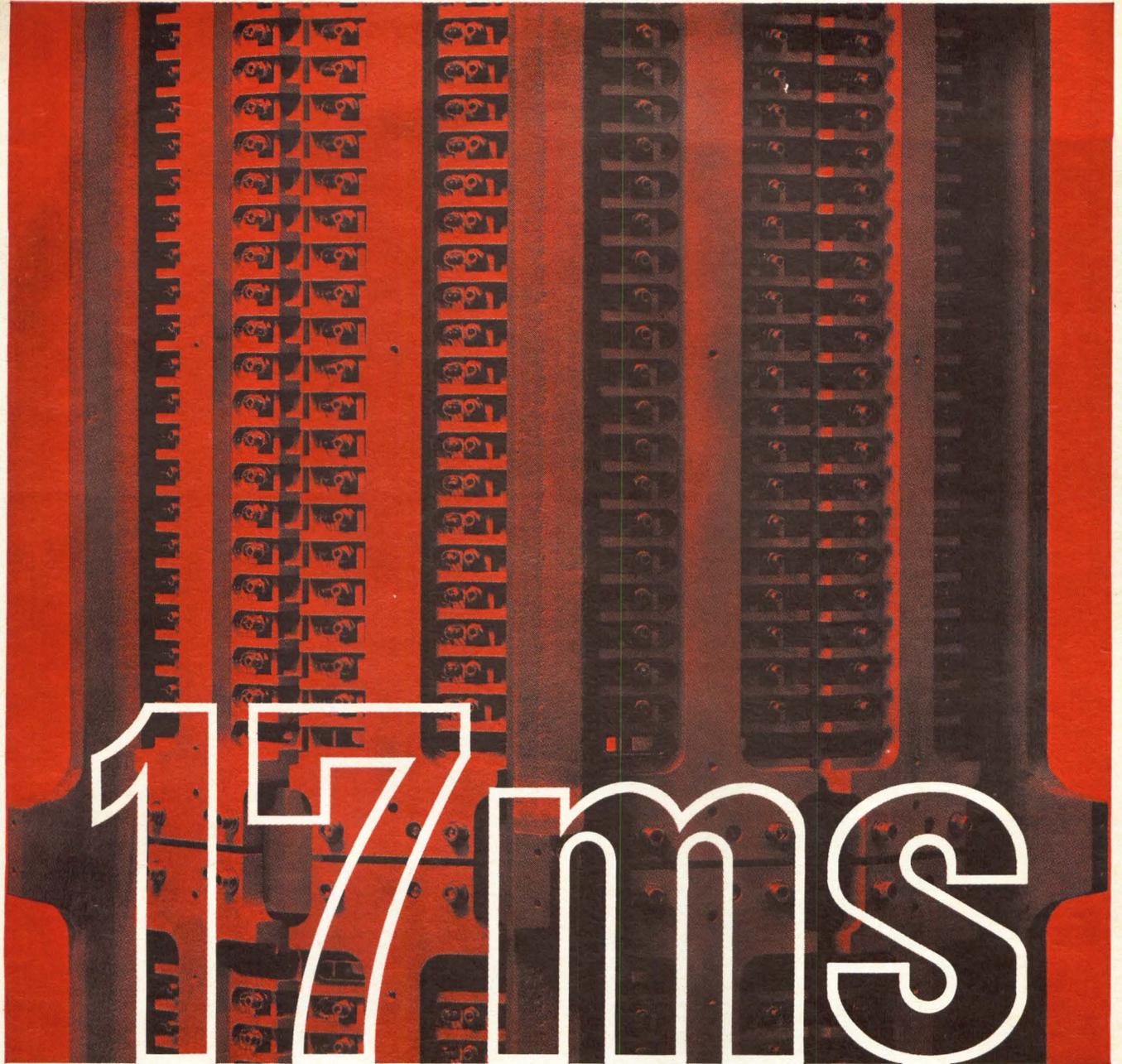


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3030 SERIES

CIRCLE NO. 8 ON INQUIRY CARD



1,000,000,000 BITS—FAST!

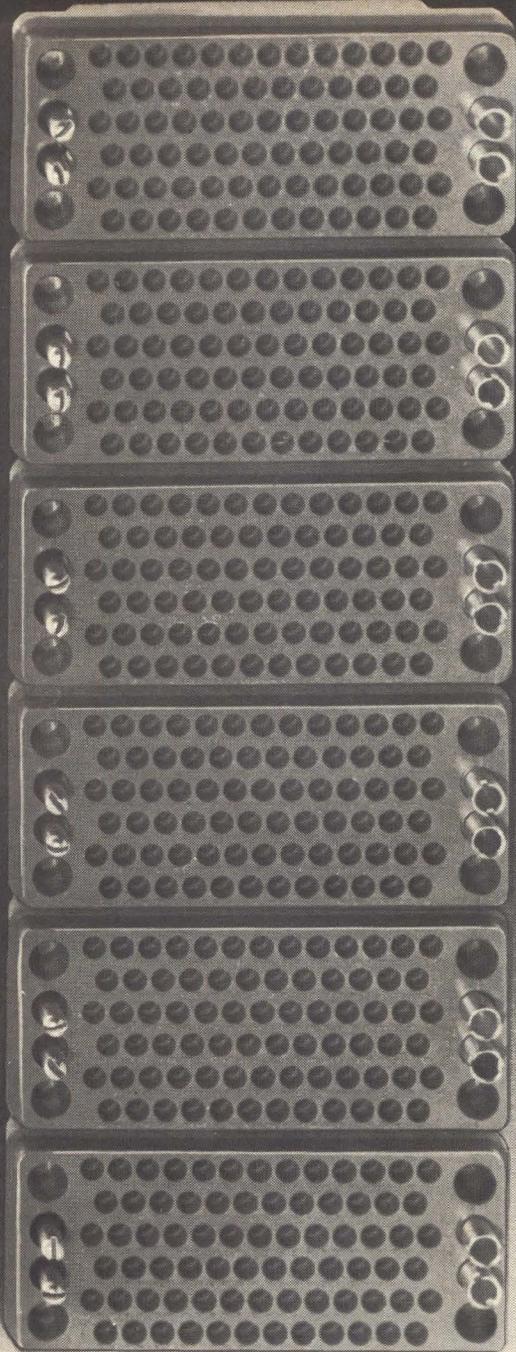
More memory! Faster access!! More memory!!! Faster access!!!! This is the constant need of "Time Share" and "Management Information" Systems. How about 1,000,000,000 bits with an access time of 17 milliseconds... enough in a hurry? At Magne-Head, memories are made for this! For information on any of our high-performance Magnetic Memory Systems or Components, write or call today. Write for free 16-page bulletin.



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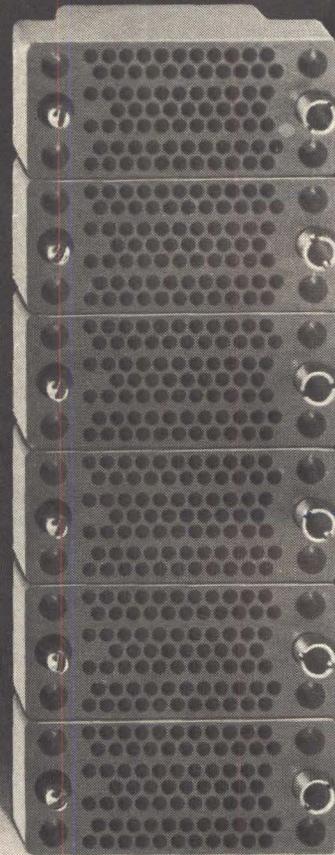
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CIRCLE ON. 9 ON INQUIRY CARD



Standard Crimp Removable Contact Connectors, Actual Size

High Density Crimp Removable Contact Connectors



NEW! Microminiature Crimp Removable Contact Connectors, Actual Size

Series MMM Microminiature Connectors Have As Many Contacts As Standard Units — at a Fraction of the Size and Weight.

Sizes: 5, 7, 9, 11, 14, 18, 20, 26, 29, 34, 44, 50 & 75 Contacts

Pins and closed entry sockets are designed with a rugged, three-tine tension spring clutch, and are fully interchangeable with either plug or socket moldings. This feature provides an infinite variety of polarization arrangements and wiring versatility. A choice of guide pins and guide sockets, polarizing screwlocks and aluminum hoods can be supplied on order.

Microminiature center screwlock versions are also available with 50, 76, 100 and 200 contact sizes.

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We're offering you smaller size... but greater contact density and design flexibility.

Connect... with a Continental Connector

CONTINENTAL CONNECTORS

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For the Sales Representative Nearest You, See Our Listings in EEM and VSMF Directories

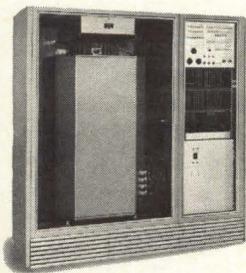


**Buy as much of our plug-in mass storage system
as you need at 27¢ a thousand characters.**

You can start with one Bryant memory drum or disc file and end up with as many as eight. Increasing your system's capacity from 8 million to 5 billion characters. All at 27¢ a thousand characters anywhere along the line.

And there's plenty to offer for the money.

For example, the universal controller system interfaces to just about any computer made with the push of a plug. It can operate in several different modes, both serial and parallel. It features word transfer rates from 50 microseconds to 900 nanoseconds per word—to and from two computer central processors. And it comes with a software package, complete with handler and maintenance routines (if specified).



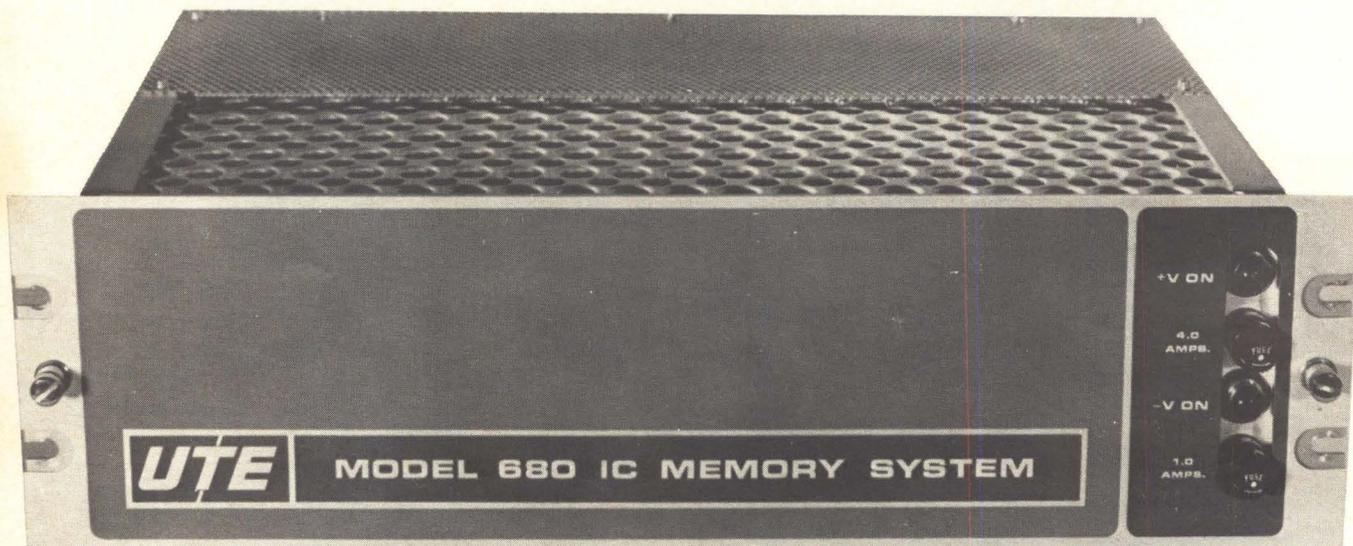
XLO-1000 Controller plug-in
Auto-Lift Drum System

Skeptics beware. We're out to make Bryant Believers out of you. Write and see. Ex-Cell-O Corporation, Bryant Computer Products, 850 Ladd Rd., Walled Lake, Michigan 48088.

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IN CASE YOU MISSED IT AT SJCC* HERE IT IS

"The System Designer's Breadboard"



An all plug-in module, fast access buffer memory system featuring

- ★ Plug-in memory stack, fully removable from the front with stored data.
- ★ Plug-in regulator, with crowbar protection and temperature tracking control
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ALL PC BOARD MODULES

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Operates in any access mode
in any cycle mode
from $\pm 5\%$ DC input power



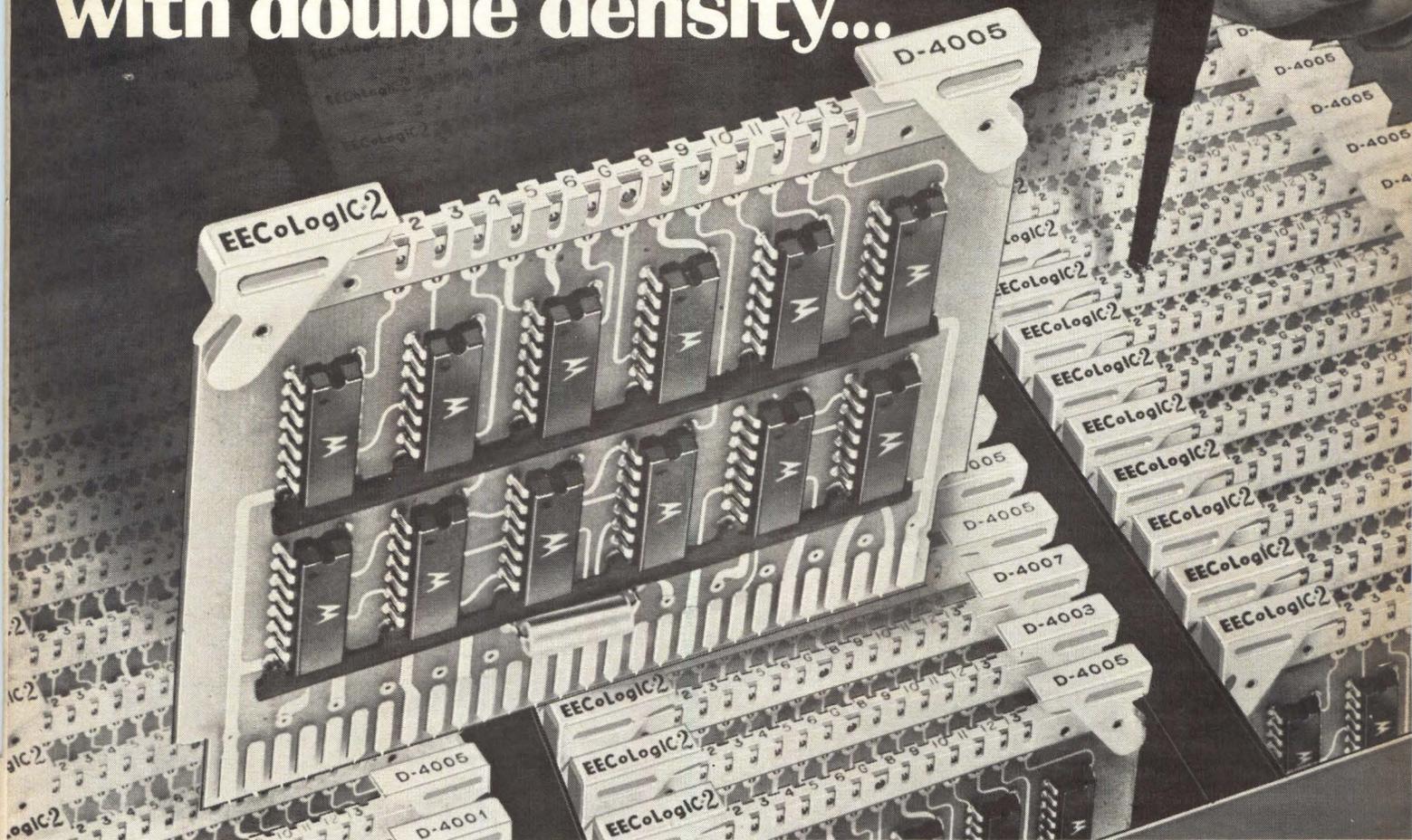
For further information, write

MEMORY SYSTEMS DIVISION

UNITED TELECONTROL ELECTRONICS, INC., 3500 Sunset Avenue, Asbury Park, N. J. 07712

CIRCLE NO. 12 ON INQUIRY CARD

INTRODUCING All new EECoLogic^{®2} with double density...



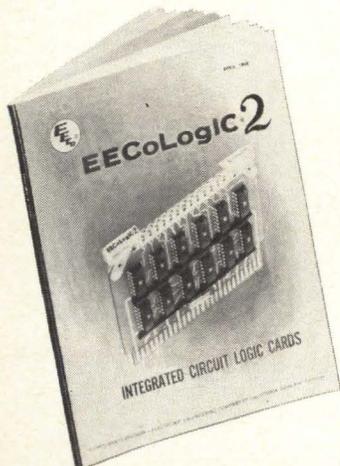
to cut digital system costs

Digital system costs drop with EECoLogic² IC Digital Logic Cards because . . . prices per logic function are reduced about 10% . . . double density cards mean more of any system fits in a standard 19" drawer (up to 6240 pin connections/drawer) . . . the number of drawers required can be halved . . . wiring costs are minimized since fewer drawers mean less interface wiring and cabling.

OTHER EECoLogic² ADVANTAGES:

- WIRE WRAP and TERMI-POINT wiring capability using manual or automatic machines, as well as soldering.
- 13 TEST POINTS accept probes, clips or hooks and make system check-out fast.
- INTEGRAL LOCKING/EXTRACTOR HANDLES hold each card securely in the card frame, identify the circuit and make card removal easy.
- LAMINATED POWER BUSES on each card and in the power wiring of each drawer reduce high frequency noise.

The EECoLogic² line of DTL logic modules with over 30 card types is available with a comprehensive selection of hardware and accessories. The new EECoLogic² catalog describes the entire line and includes practical application data. Send for your copy today.



COMPONENTS DIVISION

ELECTRONIC ENGINEERING COMPANY OF CALIFORNIA

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RECOGNITION EQUIPMENT

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LINE/PRINTER*
makes sure they
don't have to!

Recognition Equipment Incorporated uses the LINE/PRINTER with their Electronic Retina™ Computing Reader because optical character reading demands sharp, clear print-out, straight lines, and an unusually high degree of reliability.

Recognition Equipment chose the Model 4300 LINE/PRINTER, with a special OCR drum, printing at speeds to 1000 lines-per-minute. It features our Mark-II print hammer, which is virtually friction-free, and requires no periodic adjustments.

No-compromise requirements for quality, reliability, low-cost and maintainability led Recognition Equipment to choose the LINE/PRINTER.

LINE/PRINTERS are serving OEManufacturers in many other demanding areas. You don't have to read between the lines to know why. For detailed literature write *data products* (OEM Products Div.), 8535 Warner Drive, Culver City, Calif. 90230.

P *data products*

"the peripheralists"

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data products manufactures

LINE/PRINTER®, DISCFILE™, Core Memories, Tape Cleaners, Off-Line Printer Systems, Card Readers & Punches

CIRCLE NO. 13 ON INQUIRY CARD

What's happening today in keyboards is what's happening at MICRO SWITCH



Typical Communications Keyboard
Shown Below: Typical Data Preparation Keyboard

An important key to future keyboard design is what's happening at MICRO SWITCH.

Already we have successfully launched Happening No. 1: Introduction of complete wired and encoded keyboards ready to interface with your equipment.

Shown here are two typical keyboards. Each gives you dry reed switch input, solid-state-encoding, and a variety of exclusive options.

And they provide a flexibility that is unavailable elsewhere. You get a customized keyboard. Key array, format, added options, code change—you select the features required for your system.

Options include strobe and electrical monitor outputs, bounce gates and shift. For example, two interlock options are provided to improve operator speed and efficiency. An electrical monitor output triggers a detector circuit for blocking data or initiating error signals. A unique two-key rollover option permits typing at "burst" speeds without generating erroneous codes.



MICRO SWITCH

FREEPORT, ILLINOIS 61032

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CIRCLE NO. 14 ON INQUIRY CARD

But that's not all. Coming very soon is Happening No. 2. Through advanced design concepts, complete engineering facilities, innovative assembly techniques, and unique quality assurance procedures, MICRO SWITCH is preparing to supply your every keyboard need. This means new reliability and flexibility in mass-production quantities with attractive customized appearance giving new sales appeal to your equipment.

Make no decisions on keyboards until you see what's happening at MICRO SWITCH. Call a branch office or call us at Freeport: phone 815/232-1122.

From idea to hardware in 50% less time, at 30% less cost, and with the highest degree of accuracy in the industry!

Completely eliminates heating problems associated with backplane wiring.



◀ 36 card assembly of "blue chip" logic cards, showing readily accessible color coded test points for all functions.

How is it done?

Data Technology has the answer with automated logic card chassis wiring. Write for complete information on this unique production technique that will slash costs, shorten the time span between concept and completion, and put documentation in a new perspective.

Automated logic card chassis wiring is another example of the total service package provided by Data Technology.



Data Technology Corporation, 2370 Charleston Road, Mountain View, California 94040. Phone (415) 964-2600, TWX (910) 379-6476.

▲ Typical backplane wiring for Data Technology's "blue chip" logic cards. Three card cages with up to 2,000 logic functions can be wired in one operation.

CAPROCON



The Fairbanks Morse Caprocon system speeds the processing of cargo—automatically, for United Airlines.

A key to the system is Kleinschmidt

For high speed in automated communications, there's only one answer: Kleinschmidt.

Take the Fairbanks Morse CAPROCON™ system. At United Airlines Cargo Terminal in Los Angeles, Caprocon, aided by Kleinschmidt data printers, brings new speed and efficiency to the processing of random parcels.

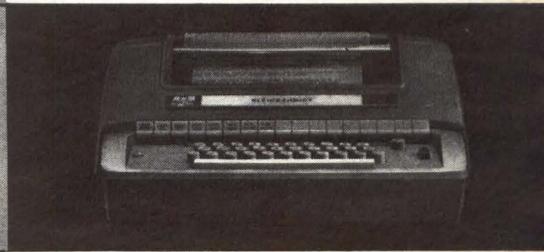
Working at a rate of 800 parcels per hour, Caprocon weighs and measures parcels instantly. It feeds the information on cubage and density to Kleinschmidt data printers. Bills, labels, and shipping instructions are printed out automatically. Result: more efficient palletizing, more economical aircraft loading, faster service than ever before.

Kleinschmidt 311™ Data Printer works at speeds up to 4 times faster than most other teleprinters. And, with 70% fewer moving parts, it's extremely reliable.

Like other Kleinschmidt data printers, the 311 is compatible with *all* makes of telecommunication equipment. You can fit it directly into your present system or into one being designed for you.

If you have a problem in telecommunications, shouldn't you communicate with Kleinschmidt?

KLEINSCHMIDT
DIVISION OF SCM CORPORATION
DEERFIELD, ILLINOIS 60015 • TELEPHONE: 312 945-1000



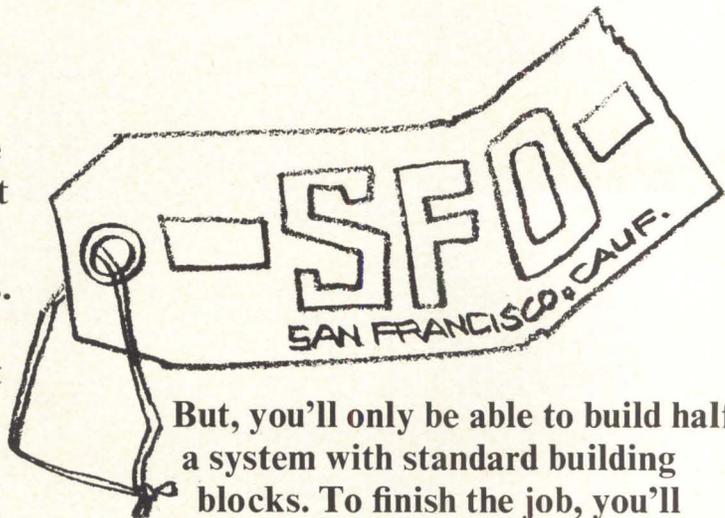
CIRCLE NO. 16 ON INQUIRY CARD

Do you want to go LSI now?

If you really want LSI now, grab the next plane to Mountain View. (It lands in San Francisco.) It's the quickest, least expensive way to get LSI into your system.

Plan to bring along your blueprints. And be ready to answer a lot of questions. We'll need to know what you have in mind for sub-systems, functions and specs. And, don't be surprised when we ask "why" a couple of times. It's all part of Fairchild's systems approach to complex circuitry.

We'll take your requirements and match them against our family of fundamental building blocks. We've got LSIs (and MSIs) that work in any digital logic system. The most advanced circuitry on the market. Offspring of computer-aided design and double-layer metal technology. And, they're all so versatile, we can probably give you a counter that has a dozen other applications in your system.



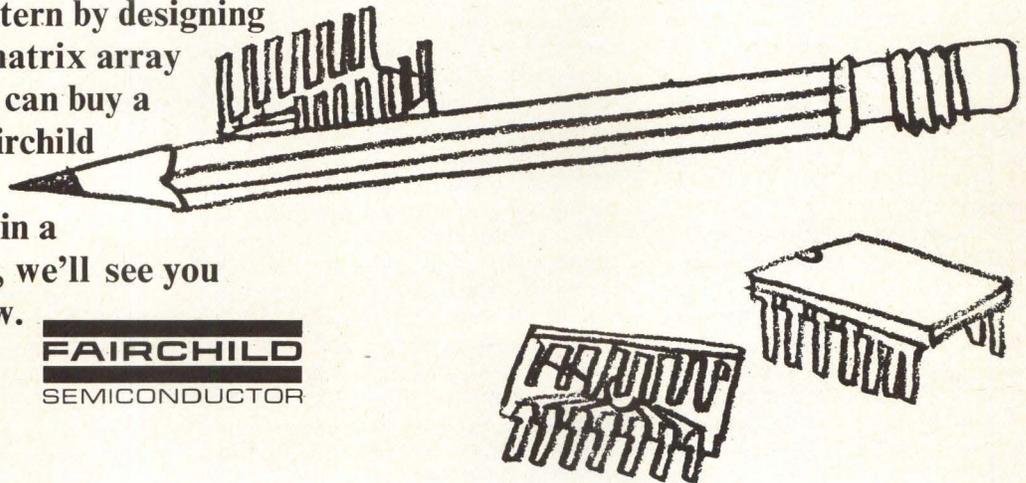
But, you'll only be able to build half a system with standard building blocks. To finish the job, you'll need interface devices to tie the whole thing together. And, here's where Fairchild can really save you time and money. We don't have to custom design each LSI interface circuit. We use Micromatrix™—a unique cellular array that's completed when we add your specific interconnection pattern. Your specs customize the entire array for your system.

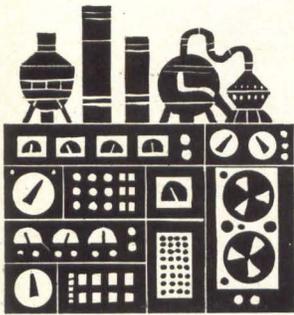
Of course, there's a lot more to the story. But, you ought to hear it in person. Just call your Fairchild salesman. He knows the flight schedule to San Francisco.

Or do you want to think about it?

We've got an LSI design kit. It's based on our new 4500 Bipolar Micromatrix Array – the first device in a highly versatile LSI family. The 4500 is an eight-cell array that can be customized for virtually any function. All it needs is your interconnection pattern. You can determine the pattern by designing your own Micromatrix array with our kit. You can buy a kit from your Fairchild distributor for about \$100. And, in a couple of months, we'll see you in Mountain View.

FAIRCHILD
SEMICONDUCTOR





INDUSTRY NEWS

DIAGNOSTIC SERVICE AID PROVIDES BETTER CUSTOMER SERVICE — A new service aid to diagnose programming and machine malfunctions without stopping the computer's work in progress is helping International Business Machines Corporation provide better service to its customers.

The development was conceived by the company's Field Engineering Division for use by customer engineers, who install and service IBM information-handling systems and equipment.

Termed a "trap," this diagnostic development acts like an electronic "camera" that takes snapshots of instantaneous trouble conditions internally, while the computer is running at full speed. In effect, it's a little like having a device on your car that would pinpoint the cause of that nagging rattle which always seems to stop when you take it in for service.

Here's how the "trap" works. Suppose that one small step, or bit, drops out of an operating program when the computer performs certain processing operations.

The IBM customer engineer, called in to correct the flaw can use the "trap" first to "patch in" a program around the trouble. Then he can have the machine, while running, call out or trap the steps of the defective program, and also have them printed out. Finally, still without shutting the machine down, he can analyze the printout, locate the defect, and thus, correct it.

Intermittent equipment failures can also be diagnosed by a customer engineer using the trap, as well as more persistent troubles in both programs and equipment.

The new development is a basic design feature of the recently announced System/360 Model 25, IBM's first computer with an electronically changeable control storage.

IMPACT EXTRUSIONS USED FOR MEMORY DRUMS

— Aluminum impact extrusions believed to be the largest ever made are now being supplied by Kaiser Aluminum, Forge Division, Erie, Pa., to UNIVAC Division of Sperry Rand Corporation, for use as memory drums with the new UNIVAC® 1108 and 494 computers. The impact extrusions in their raw form are approximately the size of 55-gallon drums with 1½" walls. They are finished out to open-end cylinders measuring 24.4" outside diameter by 36" long.

Aluminum impact extrusions were selected, according to UNIVAC engineers, because they provided the greatest density, were easy to machine, were non-magnetic, and met strength requirements. They provided all these advantages while being more economical than any other form. Density was an important consideration. The impact extrusion process assures a machined surface free of porosity, thus enabling UNIVAC to maintain the minimum-thickness magnetic coating required for reliable data recording and transferral. Since aluminum is non-magnetic, it serves as an effective base for the magnetic recording media.

The memory drums are made of 6061-T6, an aluminum forging alloy that provides for ease of impact extrusion, has good machineability and offers the best corrosion resist-

ance of all aluminum forging alloys. To convert the raw impact into a finished drum, the closed end of the impact is sawed off and the cylindrical shape is bored out. Ends are assembled into the cylinder and the rotor is turned down to size, with balancing to precise requirements essential. Weight of the assembled drum is 485 pounds.

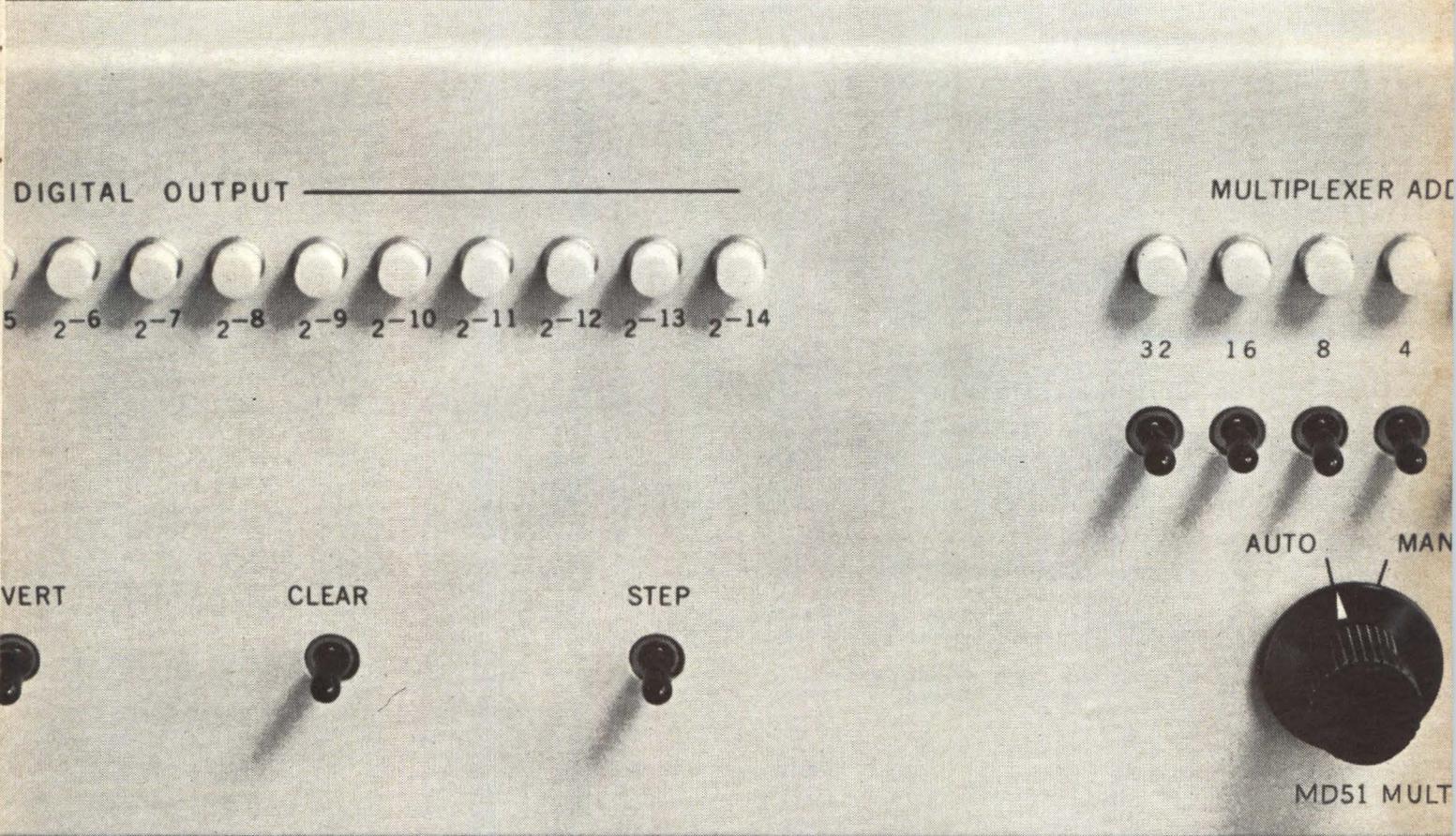
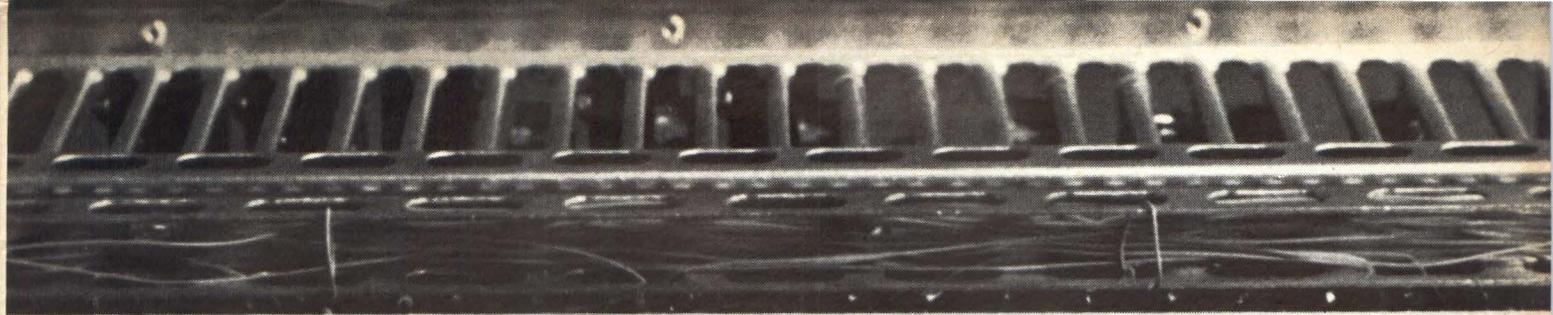
MASS MEMORY ACCEPTED FOR ARTIFICIAL INTELLIGENCE PROJECT

— A mass memory produced by Librascope Group, General Precision Systems Inc., Glendale, Calif., recently completed a successful 28-day acceptance test at Stanford University's Artificial Intelligence Laboratory in Palo Alto, Calif. The test consisted of continuous operation, on-line to a PDP-6 computer and off-line in a self-test mode.

The LIBRAFILE 4800 is one of a series of large capacity, high-speed, head-per-track disc file memories developed by the Systems Division of Librascope Group. It has a capacity in excess of 400 million data bits, with an average access time of 35 milliseconds. Additional memory modules may be added to increase storage and the head-per-track design permits bit parallel data transfers to meet interface and speed requirements.

Stanford's unit will provide an important link in the time sharing system used in the Artificial Intelligence Project. The purpose of the project is to investigate the use of computers to do work that requires intellectual ability.

The memory system stores the data and programs necessary to
continued on page 24



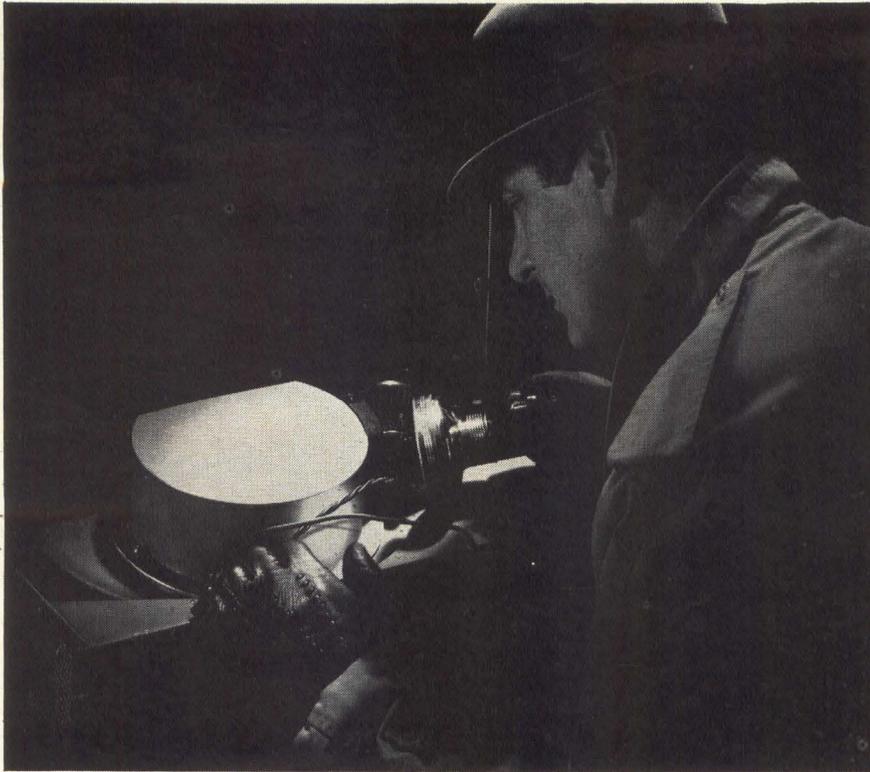
It's the fastest. It's the most accurate.

The MD51 is a high-level 64 channel multiplexer, a sample and hold amplifier and a 15-bit A to D converter, all in a single chassis. It has a total sample and conversion time of 10 microsec-

onds max. and an accuracy of 0.01%. And it sells for under \$10,000. If that doesn't say it all, write for the rest.

SDS
Scientific Data Systems,
Santa Monica, California

CIRCLE NO. 18 ON INQUIRY CARD



Have you noticed which disc memories your competitors use now?

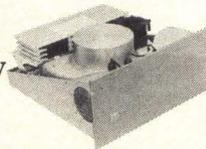
Five computer manufacturers and six data systems builders have adopted Data Disc memories as a standard rapid-access peripheral storage.

They've discovered that Data Disc memories cost about 35% less than any other head-per-track disc memory of equal storage capacity. Complete machines, including electronics, sell for 1/10¢ per bit in quantities of ten.

Perhaps you wonder how a top-quality machine can cost so little. Well, cost per disc, per track, per head or per drive is no less than any other reliable memory. But cost per bit stored is far less—simply because our “in-contact” recording technique stores twice as many bits per inch as older “floating head” techniques.

“In-contact” recording—in which heads ride in gentle contact with a highly polished disc—is five years old now. It has proven its long-

term reliability in hundreds of Data Disc memories now operating across the nation. We guarantee an error rate less than 1 part in 10^{10} , and tests by our customers show typical error rates 1000 times better.



An F-Series head-per-track system

Our F-Series head-per-track system comes with storage capacities of 0.8, 1.6, 3.2 and 6.4 million bits. It has an average access time of 16.7 ms, and stores 100,000 bits on each track—enough to fill the core memory of a small computer. And the whole system fits in $8\frac{3}{4}$ ” of rack space.

For complete information contact Data Disc, Inc., 1275 California Avenue, Palo Alto, California 94304, Phone (415) 326-7602.



DATA DISC

CIRCLE NO. 19 ON INQUIRY CARD

duplicate “hand-eye” coordination required in an assembly operation, and also to assist in the work being conducted in the area of computer-aided speech recognition.

“Hand-eye” actions presently involve a computer and TV camera linked to a mechanical hand that stacks blocks. The long-range goal of the project is to mechanize assembly and inspection tasks of greater complexity, similar to those that are performed in modern industrial plants.

ELECTRONIC TEST SYSTEM MINIATURIZED

—The Navy's first miniaturized automatic electronic test system has been delivered to Grumman Aircraft Engineering Corporation by North American Rockwell Corporation's Autonetics Division. It is the first of 25 C93-M BACE (Basic Automatic Checkout Equipment) portable systems being built by Autonetics for A6A and E2A aircraft maintenance shops under a \$3.8 million contract. Called “Mini-BACE,” the unit is a microminiaturized and improved version of Autonetics' C93-B BACE which has monitored performance of RA-5C, E2A and A6A aircraft avionics systems for more than six years.

The C93-M's development is particularly significant, according to Autonetics Project Engineer John Mossar, because it proves the feasibility of updating and phasing new microelectronic equipment into existing military programs. The new checkout unit, in replacing the C93-B, had to be designed to have the same external performance, use the same program tapes, and tie into existing test type stations.

The C93, reduced from 52 to 2.4 cubic feet in size and trimmed from 1500 to 112 pounds, releases valuable maintenance shop space for other equipment and provides portability for possible off-site use. The compact unit is being matched with other electronic maintenance checkout equipment at Grumman for fleet installation, according to Autonetics Vice-President R. M. Bukaty.

Advantages of microminiaturizing existing military equipment include saving space, cost and power, improving reliability, and adding self-check and modularity maintenance features.

Power requirements were reduced, air cooling was eliminated and self-inspection was improved, Mossar said. The C93-B isolated errors within itself down to specific drawers, while the C93-M pinpoints

faulty modules in the drawers. Modular construction has simplified field maintenance, with the tape reader, control panel and electronics easily detached and replaced.



DATA SETS OPERATE WITH WIDE VARIETY OF BUSINESS MACHINES — General Telephone & Electronics Corporation, Northlake, Ill., has developed two new data sets that will transmit and receive data from a wide variety of business machines. Individual data sets have been designed in the past to operate with a specific business machine, such as a teletypewriter, a card reader, or other types of terminal communications equipment.

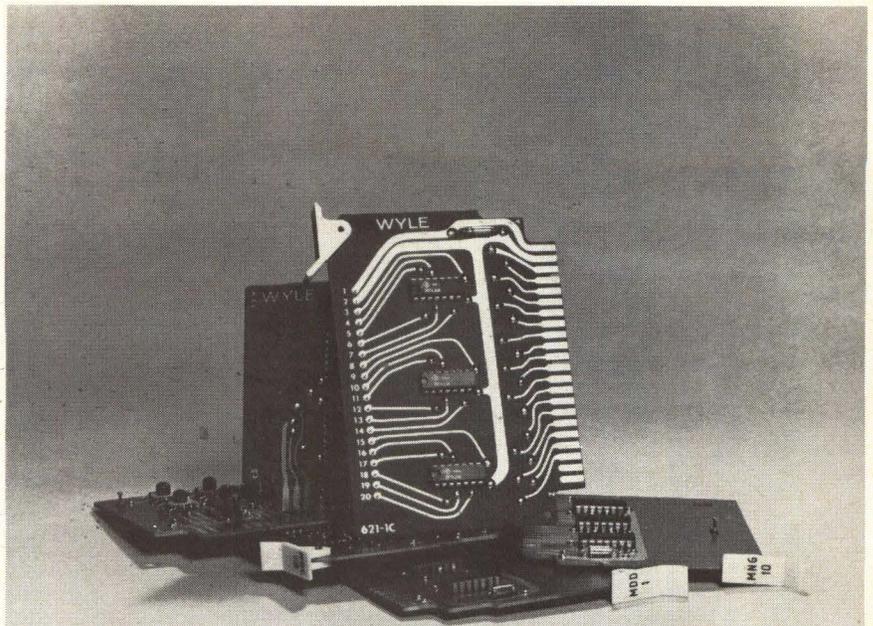
Developed by Automatic Electric Company, a GT&E subsidiary, the versatile new units were designed to meet rapidly changing requirements in data communications. Robert J. Gressens, President of Automatic Electric, said "with a great many types of business machines coming into use, it became apparent that a standard data set was necessary that could operate at speeds up to 300 words per minute."

The new AE 103A data set was developed for use over the commercial telephone network, and the AE 103F data set for private-line or "dedicated" communications systems that are established for individual customers. Both data sets are designed to provide the data transmission services offered by telephone operating companies. Each set has an independent transmitter and receiver, and can transmit and receive data simultaneously.

A special data telephone was introduced with the AE 103A data set, which operates over the commercial telephone network. The telephone provides voice communications between operators of the data terminals at each end of the circuit, and also enables them to supervise the operation of the data sets.

In addition to a conventional rotary dial, the data telephone includes six pushbuttons which control the voice and data transmission functions and various test operations.

The AE 103F data set for private-line communications systems does not require the associated data telephone. On such a system, the data sets can be adjusted permanently for transmission or reception, or the business machines utilized in the system can change the direction of transmission.



We'll give you service whether you buy from us or not

Our business is solving problems in the most effective, economical way, rather than trying to sell you what we happen to have on hand. If you have a quick question call (213) 678-4251. For a complete analysis, send us a logical block diagram describing your system, and tell how large a segment you want us to tackle. You'll receive a complete list of cards and quantities plus a description of other hardware and a detailed price analysis, without obligation.

If your problem is larger than logic cards, write us anyway. We can provide black-box

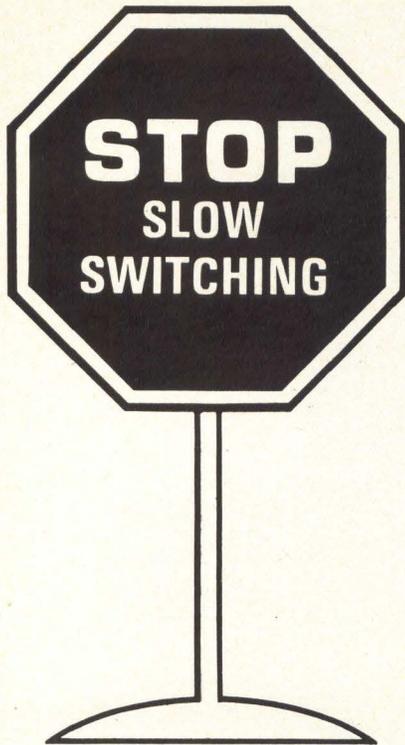
special purpose systems, or complete systems with any computer you choose. We'll even supply software.

Because we take a systems approach, rather than a product approach, when you compare total costs you'll find Wyle highly competitive.

Our main business isn't selling logic cards, it's solving problems. Logic cards happen to be one way we do this.

Call or write Mr. Norm Conwill, Wyle Systems Div. Wyle Laboratories
128 Maryland Street
El Segundo, California 90245

WYLE



Get the fastest solid state transfer switch anywhere — TRW's Minuteman.

It transfers power in a **MAXIMUM of ONE-FOURTH cycle!** That means you'll have virtually uninterrupted power.

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Minuteman switches are fast, dependable and maintenance-free. Built with the same care we use for Minuteman missile components.

To find out more . . .



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Dept. 0855, 23555 Euclid Ave.
Cleveland, Ohio 44117

TRW

CIRCLE NO. 21 ON INQUIRY CARD

UNIQUE COMPUTER TUTORIAL FILM SERIES DEVELOPED—Computer Methods Corporation, Rochville, Centre, N.Y., a subsidiary of Coburn Corporation of America has announced development of a unique film and text series designed to respond to one of the most pressing problems currently facing the data processing industry: professional obsolescence.

The tutorial film series for professional programmers and systems analysts, represents a new, efficient and economical method of staying abreast of current developments in the computer field. By jointly pooling its talents with those of leading professionals in the computing, motion picture and text industries, the company believes it has developed an approach which will revolutionize the manner in which programmers and systems analysts are taught.

Irving Bernstein, president of Coburn, said, "Now we have developed a new method of keeping the computer professional abreast of recent advancements in computer hardware, software and systems."

The first set in the series, "Data Communications," featuring Donald C. McNelis, assistant manager, telecommunications, at American Can Company, and Ernest Heau, president of Systems Group One, is available for sale now at \$500, which, Mr. Bernstein noted, "is substantially less than the average cost incurred by one programmer attending a professional seminar."

The film on "Data Communications" runs for 45 minutes, broken down into three 15-minute reels accompanied by three specially created full-size texts. The presentation is designed for use by programmers and systems analysts with a minimum of two years experience.

The second and third sets in the series, currently in production are on "Direct Storage Methods" and "On-Line System." The films will be available in either standard 16 mm reels or super 8 technicolor cartridges for portable daylight viewing.

UNIQUE TERMINAL COMPUTER

—Burroughs Corporation, Detroit, Mich., has announced that production of revolutionary new electronic terminal computers has started in the United States and will soon get underway in Scotland and Belgium. Called the Series TC500, they are designed for use with on-line data processing systems.

The computers were described by President Ray W. Macdonald as a "dramatic innovation in preparing and communicating information between a remotely-located terminal device and a centrally-located computer system."

The new terminal computers have the unique ability to pre-process and concentrate data which is to be transmitted and to "burst" or expand data being received by the same or other TC500 terminals.

They provide terminal editing and checking of an operator's input, thus freeing the central computer from this time-consuming and non-productive chore.

The central computer programming task is simplified since editing and formatting is under local terminal programming control with the TC500's.

With these new terminals the user may enter data in the sequence best suited to his needs and his problem. The terminals can internally re-format and transmit data to meet the needs of the central computer program. This ability permits the central computer to service many remotes with one program, even though the input and output sequence at the various remote points may vary, based on their local needs.

With the Series TC500 Terminal Computers, more efficient use of communication facilities is provided by such features as data editing, variable field length transmission and complete buffering. The terminal computers will always be on the line at rated line speeds, not at the terminal input or output speeds. The data communication processor can transmit up to 2,000 bits-per-second.

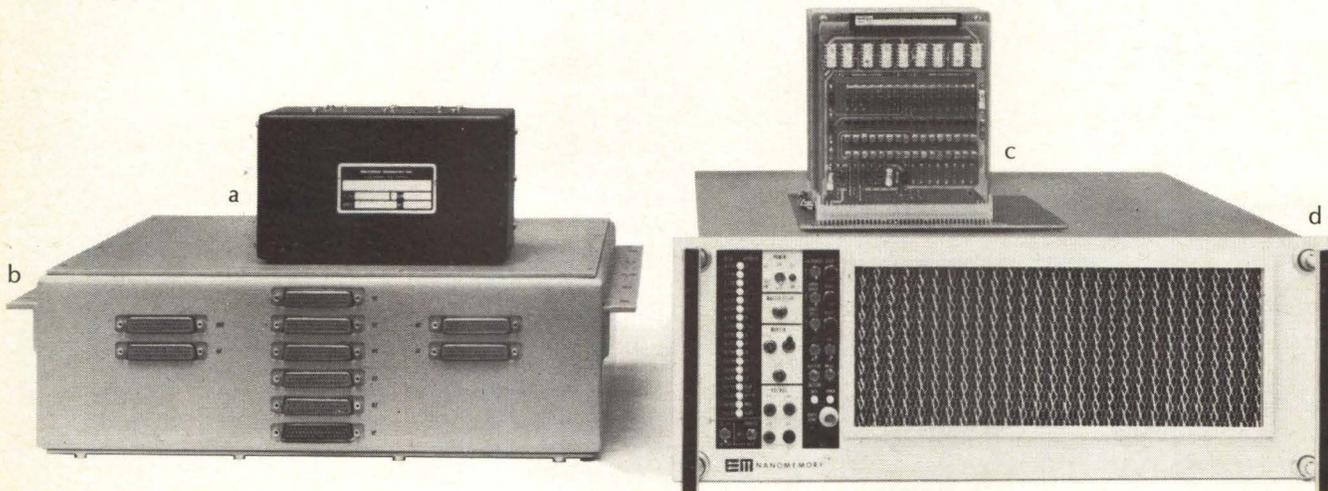
"These capabilities make the new terminal computers very responsive and economical tools, ideally suited to the design of on-line systems," Macdonald said.

The TC500's which permit more effective use of the central computer system and more economical use of transmission lines, will be available in five models. Varying in size of memory and program capacity, the models range in price from \$9,900 to \$14,400. Lease rates range from \$250 to \$360 per month.

Depending upon their memory size, the various models of the TC500 can perform a variety of tasks including the responsibility of programming, editing and other housekeeping chores which previously had to be performed by the central computer prior to actual processing.

two hawks

two doves



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(a) SEMS 5—Designed for airborne applications, the SEMS 5 has a 2 microsecond cycle time, packs 131,062 bits into only 132 cubic inches and meets applicable portions of MIL-E-5400, MIL-E-4158, and MIL-E-16400.

(b) SEMS 7—Developed for ground based applications, this rugged memory has a 2 microsecond cycle time, a 327,680 bit storage capacity and meets applicable portions of MIL-E-4158, MIL-E-16400 and SCL-6200.

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CIRCLE NO. 23 ON INQUIRY CARD

FERRITE CORE MEMORY SELEC- TED FOR SENTINEL SYSTEM —

Lockheed Electronics Company has been selected by Bell Telephone Laboratories to design and produce 15 large capacity 500 nanosecond core memories for the prototype subsystems of the Sentinel Anti-Ballistic Missile System. The memory system involved is the Model CD-50 redesigned for fabrication with qualified high reliability components meeting the weapons system requirements. Employing 18 mil lithium ferrite cores in a 2½D magnetics organization, the system offers capacities up to 65,000 words. This model is a faster version of the CD-65, 650 nanosecond memory produced at the company's Los Angeles facility.

The selection of a ferrite core memory as one of the critical subsystems in this weapons system is a vote of confidence for core technology, according to R. D. Miller, National Sales Manager of Lockheed Data Storage Products. Development efforts at Lockheed in several areas such as plated wire and thin film certainly appear to offer future possibilities in high speed applications. However, Mr. Miller said, present experience with thin film and plated wire memories is limited, particularly in the area of long term reliability. Production of batch manufactured memory elements has not progressed to a point where the increase in speed justifies the higher costs.

He sees the future challenges as faster speed and increased reliability at lower cost per bit of storage. These challenges will be met, he predicts, by a number of new techniques, but the core memory still remains the single most effective means of meeting these objectives for the major portion of the Electronic Data Processing Industry.

REFINERY USES COMPUTER CONTROL TECHNIQUE —

Computer control of petroleum refinery operations has taken a major step forward with the successful start-up and operation by The Foxboro Company and Esso Petroleum of the largest, most advanced computer control system ever designed and implemented in the hydrocarbon processing industry. Performing with great reliability at Esso Petroleum's Fawley, England, refinery, the control system using the Fox-

boro PCP 88 multi-computer approach is designed to control the majority of the refinery's fuel processing units.

The sophisticated computer control technique has already demonstrated that it can reduce variations in process flow rates, temperatures and pressures, according to Esso engineers. It also increases plant efficiency and centralizes control of widely scattered process units.

The system organizes two or more computers in a master-slave arrangement. At Fawley, the master or supervisory computer provides sophisticated control capability relieving the operator of many tasks previously required of him. These tasks include the determination of the proper settings of such important manufacturing values as temperature, flow rates and pressures. The supervisory computer also performs production and inventory accounting; and communicates with the slave computers.

Direct digital control (DDC) of primary plant variables such as temperature, level, pressure and flow is performed by slave computers for more than a dozen complex refining processes.

The supervisory computer is programmed in FORTRAN. The control computers which perform DDC are programmed in machine language. Esso can add or change supervisory programs without risk to the DDC program and without interrupting the process.

Foxboro Model 97400A computers are used in the system. These central processors utilize hybrid, integrated type circuits. An economical high-speed bulk memory is included for storage of complex supervisory calculations.

One centrally located control building houses the computers and replaces several noncomputerized centers which formerly controlled the processing units.

The operator consoles display flow rate, temperature or pressure readings sampled by the computers and contain temperature recorders and alarm systems.

The computer control installation was designed and manufactured by The Foxboro Company Digital Systems Division of Foxboro, Mass. Foxboro-Yoxall Ltd., Redhill, Surrey, England, supplied the electronic measurement transmitters, pneumatic/electric and electric/pneumatic transducers, panels and consoles, and are responsible for the servicing of the complete system.

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RCA





DEVELOPMENTS

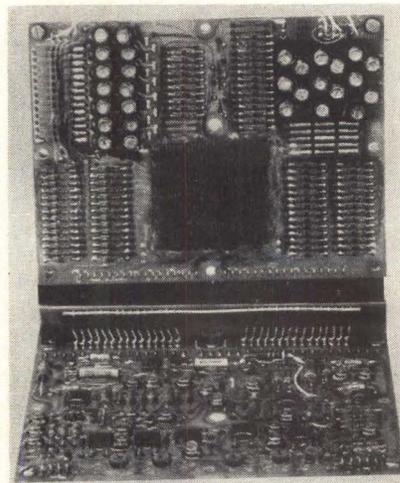
TINY SCRATCHPAD MEMORY REDUCES HARDWARE REQUIREMENTS

An extremely compact spacecraft memory has been developed by Electronic Memories, Inc., Hawthorne, Calif. It combines the properties of a memory and a fixed program thereby eliminating the hardware normally required for fixed programs. Developed for the Philco-Ford Corporation's Space and Re-entry Systems Division, Palo Alto, Calif., the memory unit will be used aboard the Pioneer spacecraft and Apollo lunar surface science package as a data processor scratchpad memory for magnetometer experiments designed to gather information on magnetic fields. Philco is developing the Apollo and Pioneer magnetometers under contract to NASA's Ames Research Center, Mountain View, Calif.

The memory system is extremely lightweight (0.7 pounds) and occupies only 29 cubic inches of space.

Parallel by bit and serial by word, the system is also magnetically "clean." This was necessary because the magnetic field normally radiated by electronic components would interfere with the accuracy of magnetic experiments. The memory has a maximum magnetic field of only 1.8 gamma at 2 feet. (1 gamma equal 10^{-5} gauss; the earth's magnetic field is about one-half gauss.)

The program function of the memory is achieved by accessing the 54 words x 30 bits of the memory in a specified sequence. Rather than the normal alternating read/write, read/write order, the memory performs read and write operations in a quasi-random sequence, as determined by the wiring pattern. For example, nine words are written into the system before any are read out. Further, at some points in the sequence, the memory is merely required to "mark time" without accessing a memory word. To



achieve this sequencing, a new design principle was developed incorporating a novel configuration of ferrite cores. Predicted reliability of the memory is 0.93 for 10,000 hours or an unusually high mean time between failures of 143,000 hours.

FIRST FLEXIBLE MULTILAYERED PRINTED CIRCUIT

The successful development of the first flexible multilayered printed circuit by the Electralab Division of Tyco Laboratories, Inc., Encinitas, Calif., now makes it possible to combine the space saving characteristics of the flexible circuit with the density of the multilayered circuit.

According to Burt Isaacson, president of the Electralab Division, the new development provides a number of advantages for equipment designers. The first is the basic physical characteristic of flexibility. Since the circuit can be bent, twisted, and shaped to fit any contour, the problem of packaging an electronic circuit to fit within odd configurations is greatly alleviated. As a result, the designer will now be able to utilize space that might otherwise have been wasted. Moreover, the basic flexibility will release previous restrictions on the shapes that electronic equipment could assume.

Secondly, the light-weight pliancy of

the flexible multilayer will allow the equipment designer to achieve higher levels of circuit density, while simultaneously reducing total equipment weight.

Third, the flexible multilayered circuit will greatly increase equipment reliability and decrease equipment maintenance because it eliminates all hand-wiring in equipment manufacturing.

Fourth, the equipment manufacturer's investment in the design of flexible multilayer printed circuits will result in substantial reduction in the total cost per connection. The lower cost would result not only from the lower maintenance, but also from ease of manufacture, elimination of random error and reduced assembly and testing time.

Electralab currently is producing prototypes of a flexible multilayer for a military weapons system developed at Picatinny Arsenal, Dover, N.J. This system, which has many major components, will utilize three different versions of the new type circuit: a two-sided plated through flexible circuit;



a flexible/rigid combination consisting of seven rigid areas with integral flexible interconnections; and a flexible plated through multilayered circuit consisting of 16 separate layers of circuitry interconnected by plated through holes. This latter circuit consists of three discs, each approximately 12" in diameter. Each disc contains a different number of layers which combine to total 16. All three discs are integrally interconnected with flexible circuitry. With the new circuitry, more than 500 soldered connections were eliminated.

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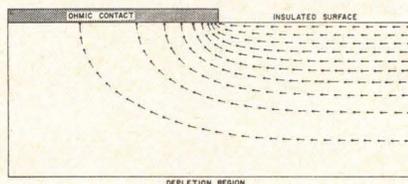
CIRCLE NO. 43 ON INQUIRY CARD



DEVELOPMENTS

DIFFUSED RESISTOR ANALYZED MATHEMATICALLY

The first detailed mathematical analysis of a diffused semiconductor resistor was reported in the May issue of the IBM Journal of Research and Development. An article by David P. Kennedy and Philip C. Murley, of the East Fishkill, N.Y., laboratory of IBM's Components Division, shows that electric current crowding in this micro-electronic device is far greater than had previously been suspected. This finding has important implications for the design of diffused resistors, Mr. Kennedy said.



"Most attempts to reduce electric current crowding by providing a larger contact will be unsuccessful because most of the contact is not being used," according to Mr. Kennedy. Instead, the electric current is concentrated along one edge of the contact, where the current flow changes direction by 90 degrees. "Qualitative studies had already shown that current crowding was going on in these structures, but no one realized how severe it was."

The Kennedy-Murley study is based upon solutions of Poisson's equation for a mathematical model that approximates the resistor. The required calculations, about 20 million, could not have been made without use of a computer. The studies were supported in part under contract F19(628)-C0116, Air Force Cambridge Research Laboratories, Office of Aerospace Research.

PHOSPHOR COATING MAKES INFRA-RED VISIBLE

Two researchers have developed a new phosphor lamp coating which converts normally invisible infra-red radiation into visible light, a feat considered highly improbable until now. The development was announced at a recent Physical Society meeting in a joint paper by Ralph A. Hewes, research physicist, and James F. Sarver, research inorganic chemist, both of the GE Lamp Division's Lighting Research Laboratory in Cleveland, Ohio.

The company's Miniature Lamp Department simultaneously announced the first application of the new phosphor: the industry's first gallium arsenide solid state lamp able to produce green light. The green color emitted by the lamp will be particularly useful as a "go" indicator in aircraft, computer and space-ship applications.

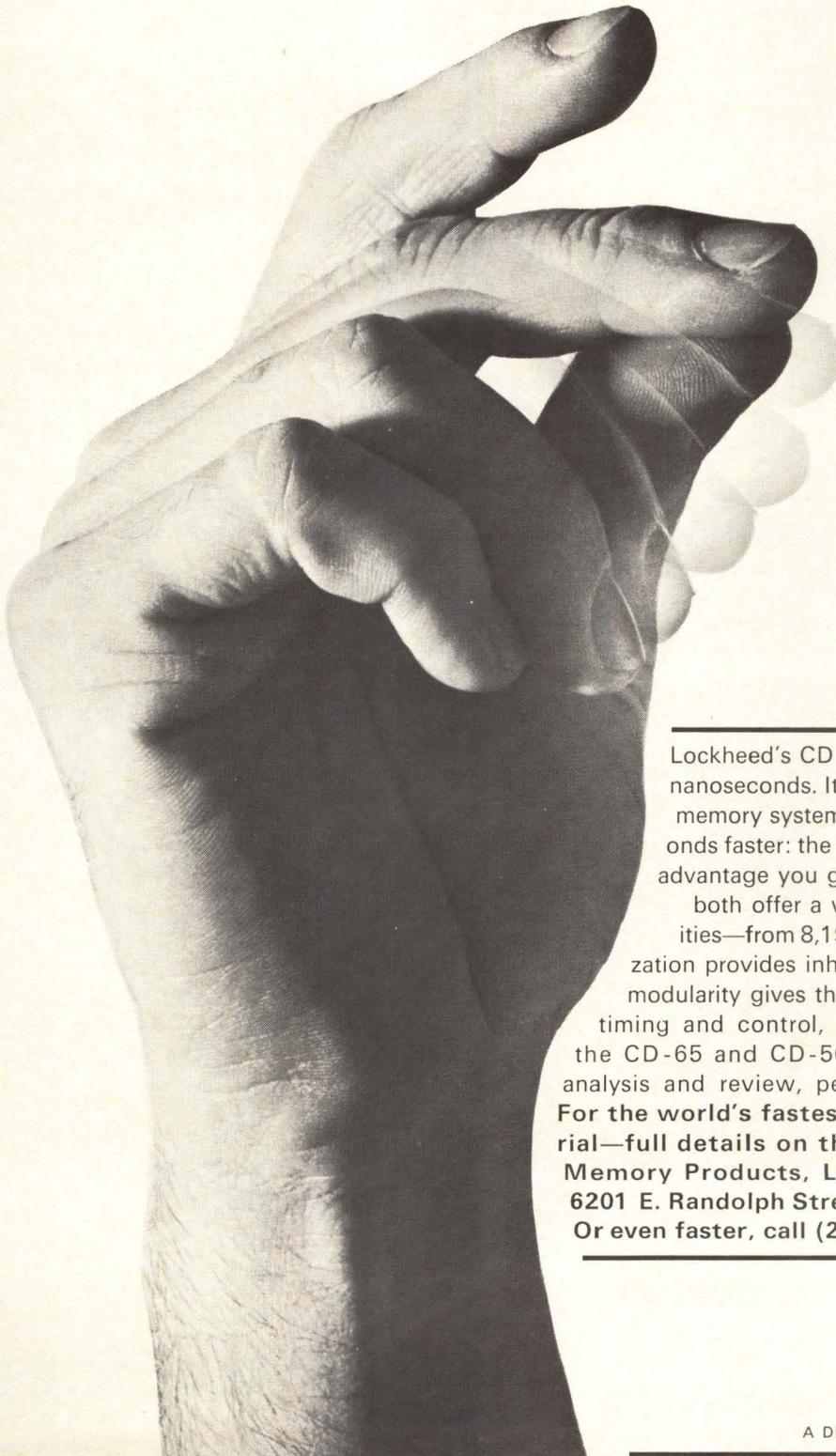
Called the SSL-3, the new lamp is under laboratory test and will be introduced at the Western Electronic

Conference (Wescon) in Los Angeles, California, in late August. Basically, it is an infra-red source coated with the new phosphor, a specially activated lanthanum fluoride. The lamp has switching capabilities of 1,000 cycles per second which make it "compatible with its intended use as an indicator," according to Miniature Lamp Department engineers.

The phosphor is a white, powdered substance. When coated on a high energy (invisible) infra-red source, it yields a highly visible green light. Laboratory tests of the new phosphor indicate an unusually long life for a phosphor, on the order of 20,000 hours. The phosphor itself has possible application including visible screens to facilitate aiming and focussing of infra-red beams.

Co-inventors of the phosphor-diode combination are Dr. Ralph M. Potter of the Lighting Research Laboratory in Cleveland and Dr. Simeon V. Galgaitis of the company's Research and Development Center in Schenectady, N.Y.

Lockheed has in production the world's fastest 2½D memory system.



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Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

CAN WE AFFORD DESIGN ASSURANCE?

As the scientific, business, and social communities become increasingly dependent on digital computers, the potential economic loss through computer error, malfunction, or faulty design becomes astronomical. The cost is borne by (1) the user, who must pay for computer and associated equipment downtime, in addition to the problems resulting therefrom; (2) the computer manufacturer, with the responsibility to correct a computer problem with all its ramifications.

Can computers be designed with that degree of reliability needed to coincide with current and potential applications? Yes. Can satisfactory performance be maintained at an economic level? Yes. Economical reliability can be established through design assurance.

Design Assurance and Computer Capability

Design assurance provides a degree of surety that a computer can perform satisfactorily within a given set of conditions. A classic problem is one of achieving an economic balance between design assurance expenditures and expenditures aimed at increasing computer capabilities... while remaining economically competitive.

In a commercial computer company, design assurance functions as a participant throughout development programs. It views each product from the aspect

of its intended performance. It is the product specification that dictates design assurance expenditures.

The amount invested in design assurance for a general-purpose computer depends, to some extent, on the applications for which the computer is intended. These applications might well include such a wide range as real-time simulation, direct digital control, shipboard navigation, and scientific laboratory research. Computer design must be reviewed in the light of effects from potential hazards. However, it is *not* necessary to assure operation under conditions and/or situations that will not exist.

Some of the obvious areas of concern in design assurance are:

- Electromagnetic Interference
- Intrinsic Safety
- Environmental Capability
- Maintainability Criteria
- Parts Qualification
- Standards

Too many safeguards could increase the cost of a general-purpose computer beyond its worth. To avoid this, each requirement must be viewed in relation to product specifications and the intended applications governing the original design. Let's more carefully assess each of these requirements:

Electromagnetic Interference (EMI)

This requirement has become increasingly significant. For example, installations such as airports have strobe light systems with power line perturbations that can create a serious computer malfunction. Computer-

The author of this month's CD Commentary, Mr. R. P. Berkowitz, is Manager of the Products Assurance Department, Honeywell, Inc., Computer Control Division. He is responsible for planning and developing basic quality assurance and reliability procedures.

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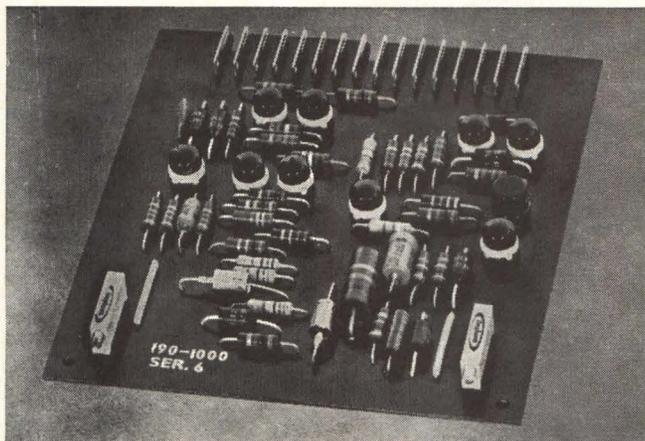
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Any number of power controller modules can be controlled by one amplifier. OMNIMOD has a current limiting parameter, over voltage protection, voltage sequencing, and remote sensing.

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1. design one input power converter to change unregulated line ac power to unregulated dc power

2. select the number of plug-in OMNIMOD power control modules to supply the power needed for each output

3. package these elements with filter capacitors and a plug-in amplifier module for each output

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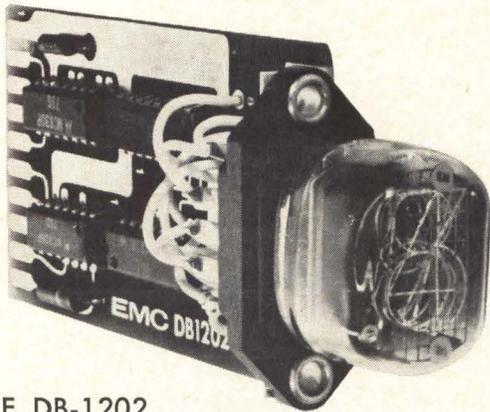
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THE DB-1203 (with memory)

A family of plug-in cards, using the same 20-pin edge connector and the same card size and construction, is available to provide a display memory function in addition to the counting function of the DB-1202. Transient BCD information may be transferred to this card and displayed independently of the source until a new set of information is accumulated.

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CIRCLE NO. 29 ON INQUIRY CARD

generated interference may result in degradation with-in adjacent communication equipment. Noise from machine tools may inhibit computer operations. Consequently, the capability of a digital computer to withstand EMI has become an important consideration in the control of certain processes adopted by commercial manufacturing. In fact, both federal and military establishments have generated and implemented EMI specifications to provide test techniques for measuring conducted and radiated EMI levels. Certain techniques to achieve a higher tolerance to electromagnetic interference can be incorporated as an integral part of the commercial design without question of economic justification. Or, when the requirement for military EMI suppression is only a possible condition, commercial design can have provisions for later incorporation of EMI suppression devices.

Intrinsic Safety

Intrinsic safety is a prime requirement for direct-digital-control technology. Where the possibilities — both physical and economic — of catastrophic failure exist, the computer system must present an intrinsically safe design. This is most important when the operating requirements include the hazards of an explosive atmosphere and human intervention, and where unforeseen and/or inexplicable failure modes constitute a hazard to life and property. After identifying potential hazard zones, their consideration must be implicit with the design criteria for the basic computer system.

Environmental Capability

This is an inherent part of the computer product definition, particularly where a general-purpose machine will be used in a wide variety of applications. In addition to the obvious environmental factors — shock, vibration, temperature, and humidity — other environmental considerations need definition and exploration. Restricted air flow due to human intervention; rapid changes in ambient room conditions; shipping; acoustical vibration in areas, for example, adjacent to an airport; low-level vibration possibly experienced with plenum chambers — all must be considered as part of the environment. It is important to adequately describe all combinations within the environment and relate them specifically to the overall computer specification prior to final implementation within the design.

Maintainability Criteria

Maintainability criteria defines the adaptability of a computer to be repaired . . . usually in terms of average dollars per repair and/or hours per repair. Any machine could fail sometime during its life, and hardware maintenance costs might outweigh the initial investment in a few years. In fact, downtime of certain systems is prohibitively expensive, and in some applications, through redundancy or alternate techniques,

the computer provides partial operability during malfunction. The development of specifications for commercial digital computers must include, as part of the design, criteria of maintainability: accessibility for parts replacement, diagnostic routines, spare parts list, and verification routines. It is only when these items are stipulated and assessed for value, prior to initial development, that they can be economically incorporated.

Parts Qualification

This is a necessary part of any development program. It is here that the balance between cost objectives and reliable performance is most clearly discernible. It may be that a component part of faulty design is more expensive to use than a higher priced, but more reliable, part. This economic question requires quantitative data to be resolved when establishing a parts qualification program. Because a computer is comprised of many small parts, cost would be prohibitive to inspect and test each of these components. Techniques must be employed to assess the "goodness" of an entire population of parts, such that reasonable assurance is obtained that it is economically advantageous to use all of the parts. Quality control engineers use sampling plans which allow a balance to be maintained between the cost of failure and the cost of inspection. The design assurance role is to relate this technique to the application of the component part in the computer.

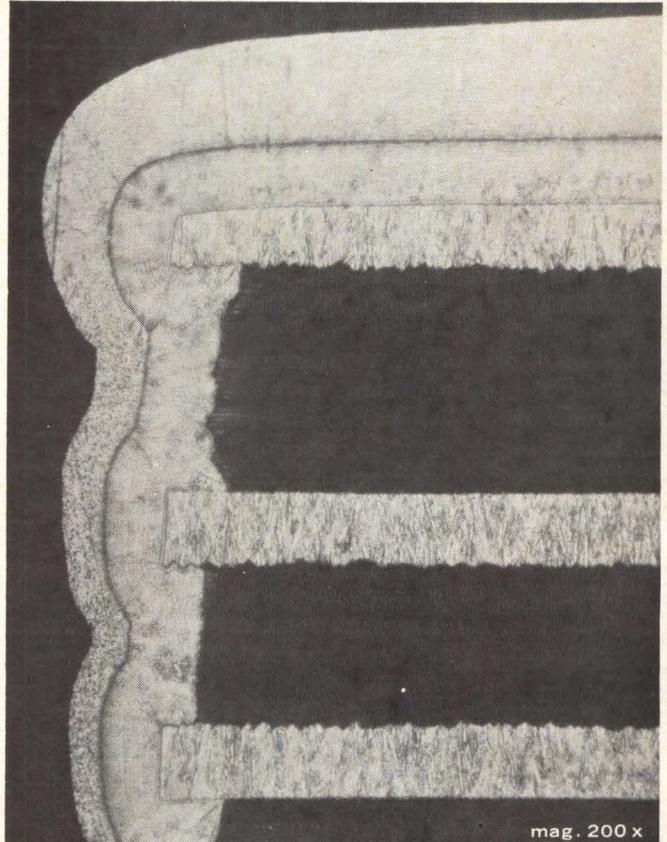
Standards

The standards by which any company develops and fabricates equipment is the backbone of the organization. These standards define practices, construction techniques, and design criteria. They establish the reliability and quality of the end product. Standards must insure feasibility for manufacture, and provide the capability of allowing engineering changes to be reviewed and rapidly processed. They should not impede the speedy solution to any potential or latent problems. The success of any design-assurance program can be measured on the basis of its satisfactory impact on the company's basic standards.

Conclusion

The development of commercial digital computers cannot lack design-assurance functions. The costs of faulty performance and faulty design are becoming progressively expensive. With the introduction of committed logic and large-scale integration, the cost of corrective action tends toward the prohibitive. The increased dependency on commercial digital computers makes the role of adequate design assurance programs ever more important. Implementation of design assurance programs can no longer be limited to the military; they must be part of the earliest development programs for commercial digital computers.

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Some of the more important aspects of large-scale integration as it relates to logic and memory systems are highlighted in this article. In certain cases, detailed explanations are given to illustrate how this technique is actually implemented. The implications of large-scale integration to the system's designer and the system design itself will be discussed.

THE APPLICATIONS AND IMPLICATIONS

Over the last decade, a number of devices have promised to alter profoundly the direction and rate of development of the digital computer art. The cryotron and the Esaki diode are two of them which have not lived up to the early claims.

Large-scale integration (LSI), the latest development which has caught the imagination of the computer world, is not a suddenly discovered implementation of a physical phenomenon. It is, rather, a product of a rapidly accelerated refinement in widely used semiconductor processing and fabrication techniques. It has the potential to produce more of a jump in the growth of the computer field than any single development to date. The explosive growth of semiconductor technology is illustrated by a 10:1 price reduction in silicon transistors during the past four years and the introduction of integrated circuits, containing from 5 to 50 transistors and associated components, into widespread military and commercial use. The belief in the future of LSI is based upon the production yields of present integrated circuits, the prototypes of much more complex devices now being made on a pilot plant basis, and the fact that LSI is an evolutionary extension of a known technique, revolutionary only in the speed of technological development.

Industry recognition of the importance of large-scale integration is evidenced by the fact that at least three symposiums have been organized for, and attended by, representatives of the component and processor industries^{1,2,3} and many papers on the subject have appeared in the technical press.

LOGIC APPLICATIONS

Multifunction Subsystems

The term "multifunction" describes an integrated device in which *two* or more circuits are on a single chip.

With all inputs and outputs exposed on the package terminals, all signal-carrying leads are available for interconnection with other packages and for testing⁴.

Until two years ago, it was uncommon to see anything more complex in a single package than dual gates. There has been a steady trend toward increasing the number of circuits per package. Today, most integrated circuit (IC) manufacturers offer such multifunctions as quad-2 gates (4 gates per package, each with 2 inputs and 1 output), triple-3 gates, etc. Fig. 1 shows examples of commercially available multifunction IC's. Note that in every case, for a 14-pin package, all the available pins are used.

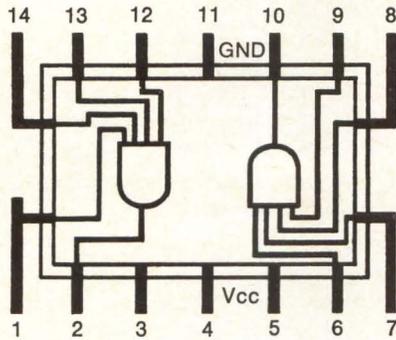
As the integrated circuit fabrication art has progressed, the circuit package has become pin-limited. In other words, it has become possible to fabricate, with high yield, more logic functions on a single monolithic chip than the package leads will allow. To take advantage of these advances, we must either increase the number of pins per package or introduce complex functions within the present packaging.

If the number of leads for a single circuit package was increased to 25 or 50, the pack would hold what is generally on a discrete-component printed-circuit board: 3 to 10 logic circuits. Increased economy can be realized from this approach.

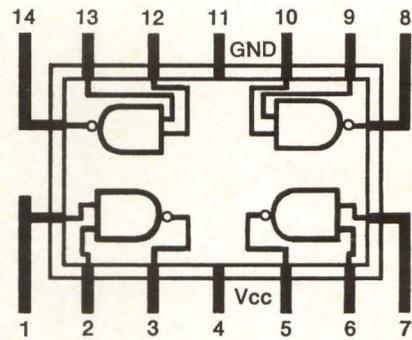
In a paper presented at the National Symposium on the Impact of Batch Fabrication on Future Computers⁵, T. H. Bonn predicted that "the total cost of a monolithic equivalent of a printed circuit board can be much less than the cost of a board with discrete components. The use of plastic packaging with connector leads molded into place may make it possible to use monolithic circuits as exact replacements of today's equipment.

OF LARGE-SCALE INTEGRATION

DAVID M. HUDSON
 Honeywell, Inc.
 EDP Division
 Waltham, Massachusetts



(a) DUAL 4-INPUT GATE

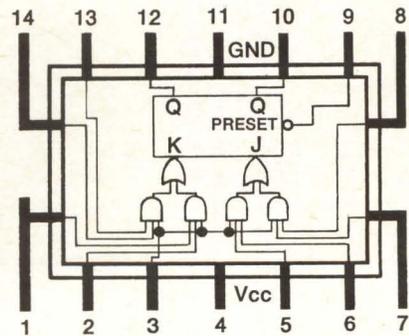


(b) QUAD-2 NAND

While the above statement may be true, and even desirable in certain cases, it is frequently impossible to effect direct one-for-one replacement of existing first-generation microelectronics by second-generation devices.

Moreover, as new classes of circuit and functional-design techniques become available, system implementation methods previously considered impractical may prove to be the most economical and reliable form to adopt.⁶

Simply increasing the circuit density per chip may not be the most advantageous approach. This is especially true if all interconnections must still be made by printed circuit wiring on a carrier board and by backboard wiring. As circuit-delay times decrease to the nanosecond range, almost any interconnection begins to exhibit delays compared to those of the circuit. If costly and space-consuming package terminals and termination networks are to be avoided, more logic interconnections must be made at the circuit



(c) J-K FLIP-FLOP

Fig. 1 Dual in-line 14-Pin multifunction integrated circuit packages.

level (e.g., between circuits on the same chip). It will no longer be economical or desirable to bring all logic signals to the device terminals.

COMPLEX FUNCTIONS

The term "complex function" is used to describe an integrated device in which *three* or more logic circuits (nor, nand, FF, etc.) are integrated on a single chip. Their interconnection provides some logic function which is at a higher level of organization than the individual logic elements.⁴

Interconnection patterns for a function are predetermined by a fixed mask; no wiring discretion is available for yield purposes. The inputs and outputs of all the circuits are *not* normally exposed to the package terminals. Typical examples of a complex function are a full adder and a multibit serial shift register shown in Fig. 2.

This approach has in part helped solve interconnection problems. But each package is very specialized in its function. Adders and shift registers do not make up a large proportion of the circuits in a computer. At best, in large parallel machines, only 40 to 50% of the circuits are of a repetitive nature that will allow this type of approach.⁵ In small machines, the percentage is lower. In order to take a major step forward, it is necessary to make the control and quasi-random interconnections on the semiconductor substrate.

Logic Arrays

The term "logic array" is used to describe an integrated device in which fifty or more circuits are on a single chip. The circuits are on the chip to form some logic function at a higher level organization than a single circuit.

Logic arrays are constructed by the interconnection of many logic elements on a chip. The basic concept of logic arrays is not new. The early work of Maitra, Canaday, Minnick, and Hennie^{7,8,9,10} however, has been of limited practical value. Generally, they concentrated on cellular logic with the severe restrictions (since made unnecessary by technological advances) that only identical circuit types could be used and connections were made only to the nearest neighbors of any cell, so as to avoid more than one layer of interconnect metalization. Theoretical work is continuing, by Minnick at Montana State University and by Kautz and Goldberg at Stanford Research Institute, on more modern forms of cellular logic. The new work is concentrating on logic in memory. A sorting memory, interconnection array, encoding—decoding arrays, and a matrix inversion array are among the complex arrays being studied.

Minnick's concept of a cutpoint array is one aspect of the early work that is receiving continuing development. A standard regular array is deposited with all possible nearest-neighbor interconnections. The array is particularized to perform a specific function by breaking some of the interconnections. One method of breaking connections is to place a fuseable link in the appropriate signal paths. The fuse can be blown or opened by a surge of current, but the connection is not disturbed by normal operation. A 15 x 15 diode decoding-encoding array which uses this principle is being offered commercially. The code is selected by blowing a fuse in series with each diode. The fuse consists of a narrowed section of the aluminum interconnect wiring.

The three concepts of major importance in large arrays are discretionary wiring, 100% yield, and master slice. The silicon single crystals which are used in the manufacture of LSI are not perfect and have a certain number of defects per unit area. The larger the piece, the greater the probability of occurrence of a defect which will result in a faulty circuit at that point. In the discretionary wiring approach, the occurrence of faults is planned. Large pieces of silicon, sometimes the entire 1½- to 2-inch diameter of the crystal, are used. Extra circuits are deposited. The circuits are individually tested and the faults entered into a computer. The interconnect wiring pattern which will accomplish this specific function and bypass the faults is computed by the design automation programs. A special set of interconnect masks is then designed by machine for the particular silicon slice. This procedure is now considered too costly, except perhaps for semiconductor memories.

In the 100% yield approach, a chip size is chosen such that the yield of chips with all good devices is in the economic range. The same interconnect mask can then be used for each chip of the same function. Knowledgeable industry sources predict that by 1970, the most economical chip—in logic circuits/dollar—will be ¼" x ¼" in size. It will contain from 250 to 1000 circuits, depending on the complexity of the circuits and the size of the device. As our ability to produce defect-free crystals improves, it is further predicted that the most economic chip size will increase.

The master slice concept is a proposal for overcoming the major problems in the use of large arrays: the length of time required to make logic changes due to last-minute specification charges, logic design errors, and the requirement for rapid construction of prototypes. A general-purpose, 100% yield array of logic circuits, not interconnected, is provided by the semiconductor manufacturers and stored ready for use. The interconnect pattern is then calculated, masks made, and interconnection packaging and testing performed. This approach is being developed by a number of semiconductor and computer manufacturers.

The system can also be used to decrease startup costs for infrequently used arrays. Where only a few of a given type of array are used in each machine, the money spent on design and mask making may be the major cost over the production life of the device. The design automation procedures, automatic layout, automatic generation of test specifications, and automatic mask making now being developed for the master slice are expected to drastically cut both turnaround time and startup costs.

Two basically different types of devices, bipolar and MOS, are used in LSI arrays¹¹. The bipolar devices are the usual type of transistors which depend upon the diffusion of holes and electrons for power gain. MOS is a newer type of transistor that depends upon the propagation of electric fields across an insulating layer for power gain. Generally speaking, bipolar devices are five to ten times faster than MOS devices. However, MOS devices require fewer process steps, occupy $1/2$ to $1/4$ the surface area of silicon, and have lower dissipation. The processing of MOS devices appears to be more critical and sensitive to spectrographic levels of impurity than bipolar. It is expected that MOS devices will find wide use in peripherals, where the speed of bipolar devices is not required.

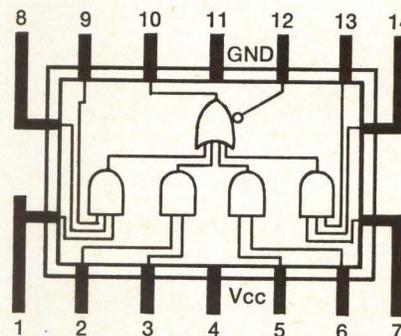
Commercially available today are such packages as multibit parallel adders, decimal-to-binary and binary-to-decimal converters, and 4-bit shift registers with parallel read in/read out. Two recently announced single-package logic arrays indicate the success that has been achieved in implementing ultra-complex functions. They are: (1) a 16-channel, random-access multiplexer complete with address storage and decoding capability, and (2) dual 50-bit, MOS shift registers. (100 bits if a single external connection is made).

MEMORY APPLICATIONS

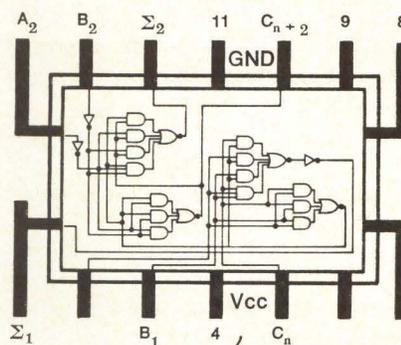
Conventional Storage

Of all the potential applications of large-scale integration, new memory techniques are the most startling. Ferrite core memories have just about reached their limit in terms of access speeds required for internal scratchpads. Magnetic-thin films, while fast enough, are too costly. Studies show that because of LSI, semiconductor memories are less costly than any other approach for speeds from 25 to 200 nanoseconds and for capacities up to 20,000 bits — just the range required by scratchpads.

Available now are such devices as a 1-bit wide, 16-location memory chip in a single, 14-pin, dual inline package¹². Used in Honeywell 4200 and 8200 systems, its cost is comparable to a single set-reset flip-flop. Fig. 3 illustrates this device. Normally, all input lines are at ground potential. Selection of a cell in the array is

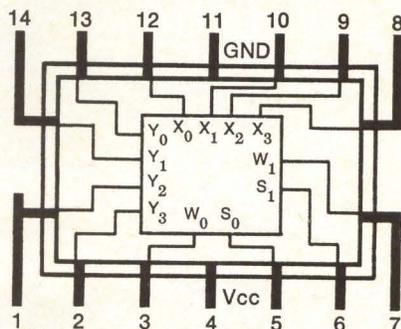


(a) 4-WIDE 3-2-2-3 INPUT AND-OR EXPANDER



(b) 2-BIT BINARY FULL-ADDER

Fig. 2 Complex-function integrated circuit packages.



PIN	FUNCTION
1	"Y" Selection
2	" "
13	" "
14	" "
8	"X" Selection
9	" "
10	" "
12	" "
3	Write "Zero" Strobe
5	"Zero" Sense Output
7	Write "One" Strobe
6	"One" Sense Output

Fig. 3 4 x 4 Memory matrix.

accomplished by the coincidence of an X and Y selection line being in the HIGH (3.5v) state. When this occurs, the state of the selected cell is indicated by S_0 and I_1 output leads. Output S_0 indicates the negation output, while S_1 indicates the assertion output. Whenever a cell is selected, its state may be changed by pulsing either the W_0 or W_1 inputs. W_0 provides for writing in a ZERO, while W_1 effects a ONE.

Read-only Storage

The implementation of read-only memories as the control element in a computer has significance for maintainability and emulation¹³. Instruction decoders and controls present a difficult problem to the designer. These elements contain no repetitive patterns like those in data paths and arithmetic units. In addition, they have many external connections. A read-only memory can be used to provide these same control signals. It would contain a long list—hundreds or thousands—of microinstructions. Each program macroinstruction from the main memory addresses a sequence of microinstructions in the read-only memory. Each microinstruction in the sequence describes the state of the entire machine during its next cycle. The read-only memory divides easily into segments, since its only external connections are the word address inputs and control signal outputs. LSI read-only memories are being offered by several manufacturers.

Associative Memories

In the past, associative or content addressable memories of any significant size have been impractical for widespread use. Relatively small associative memories have been built with various technologies, such as multiaperture ferrite cores, cryotrons, and various thin-film techniques. The logical flexibility of microelectronics now makes at least scratchpad-size associative memories practical.^{14,15}

Partitioning an associative memory into sections that can be built with integrated circuits is easier than dividing a conventional memory, because there are no address inputs. Yang and Yau¹⁶ have reported the application of the cut-point cell to an associative memory system. The bit memories, word sequential-control networks, word match-tag networks, and bit-output networks have identical structures. Thus, the entire memory can be implemented by a set of identical modules which contain an array of cutpoint cells of various indices.

Queue Stacks

Inexpensive integrated circuit memories now make inclusion of various queueing systems within the hard-

ware attractive. LIFO or FIFO stacks can be adapted for address or operand processing.

Amdahl and Flynn¹⁷ describe the organization of a super speed computer using extensive internal storage for effecting instruction look-ahead. By scanning the instructions stored, certain out-of-sequence operations may be performed and the effective execution time of a program segment greatly enhanced.

Third generation computer systems make extensive use of multiprogramming. The control group registers of the 8200 system which store the status of up to eight concurrent programs, are a natural application for LSI.

IMPACT OF LSI ON SYSTEM ORGANIZATION

Central Processors

The advent of large-scale integration and its resultant economy has made it clear that a complete re-evaluation of what makes a good computer organization is imperative. Methods of machine organization that provide highly repetitive logical subsystems are needed. As noted previously, certain portions of present computers (such as successive stages in the adder of a parallel machine) are repetitive; but others (such as the control unit) tend to have unique nonrepetitive logical configurations.

Both the Soloman and Holland machines belong to a growing class of so-called "iterative machines." These machines are structured with many identical, and often interacting, elements¹⁸.

The Solomon¹⁹ machine resulted from the study of a number of problems whose solution procedures call for similar operations over many pieces of data. The Solomon system contains, essentially, a memory unit, an instruction unit, and an array of execution units. Each individual execution unit works on a small part of a large problem. All of the execution units are identical, so that all can operate simultaneously under control of the single instruction unit.

Holland²⁰, on the other hand, has proposed a fully distributed network of processors. Each processor has its own local control, local storage, local processing ability, and local ability to control pathfinding to other processors in the network. Since all processors are capable of independent operation, the topology leads to the concept of "programs floating in a sea of hardware."

In contrast to the Solomon and Holland machines, the UCLA Variable Structure Computer²¹ introduces a variable topology in which sets of system connections and nodes are alterable under program control. The

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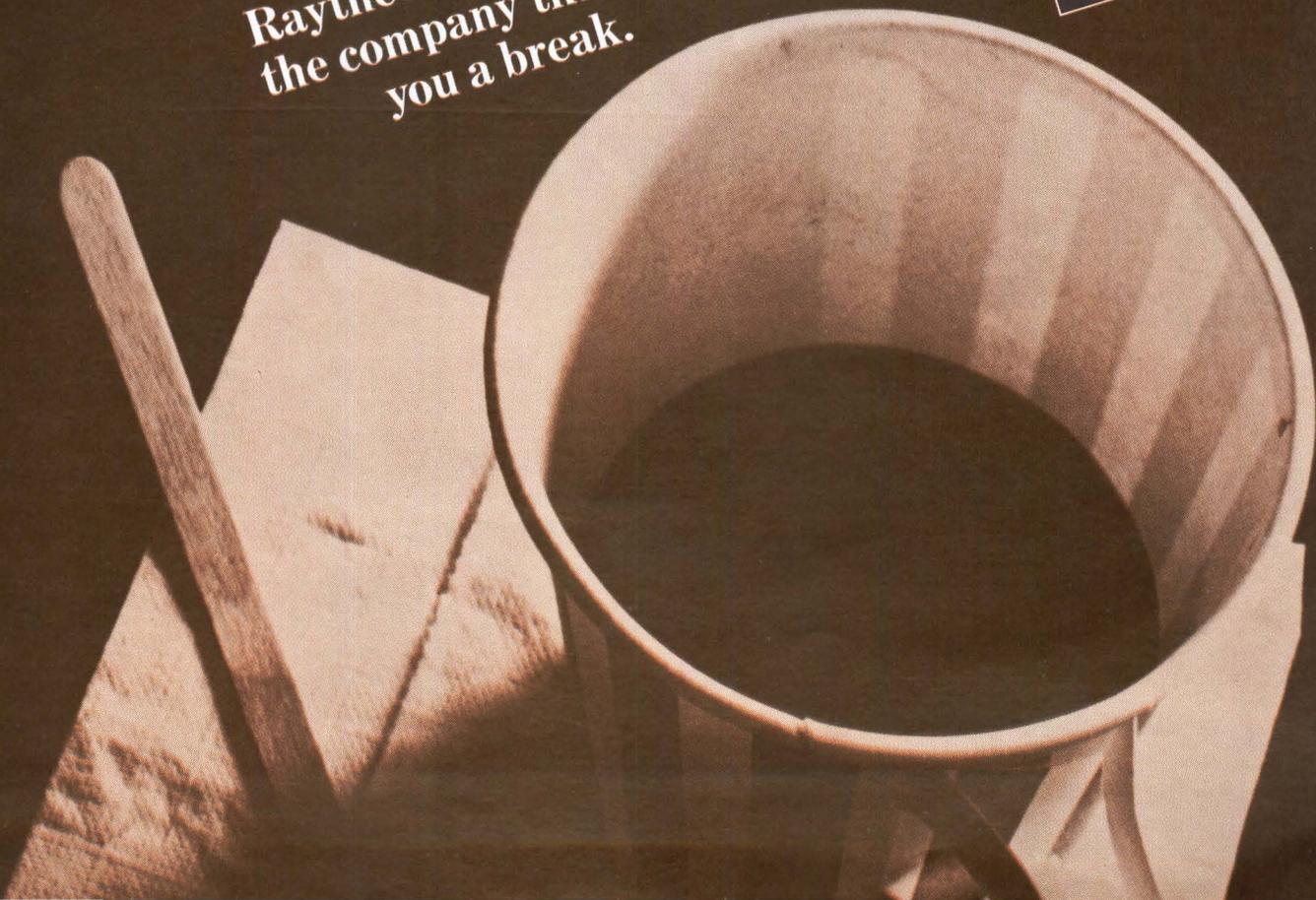
The \$15,000 IC Systems Computer with \$1.50 spares. The 703 is the only small systems computer built like third-generation million dollar computers. The CPU is wire-wrapped with plug-in IC's on one motherboard. A unique CPU self-diagnosis solves its own circuit malfunctions. When necessary, you can simply plug in a new IC. Time: about 30 seconds. Cost: about \$1.50

The 703 is like larger computers in other ways. It's a 16-bit machine with 1.75 usec cycle time and is expandable from 4K to 32K. It has word and byte manipulation instructions, an executive and real-time interrupt system and hardware multiply-divide option. Software includes

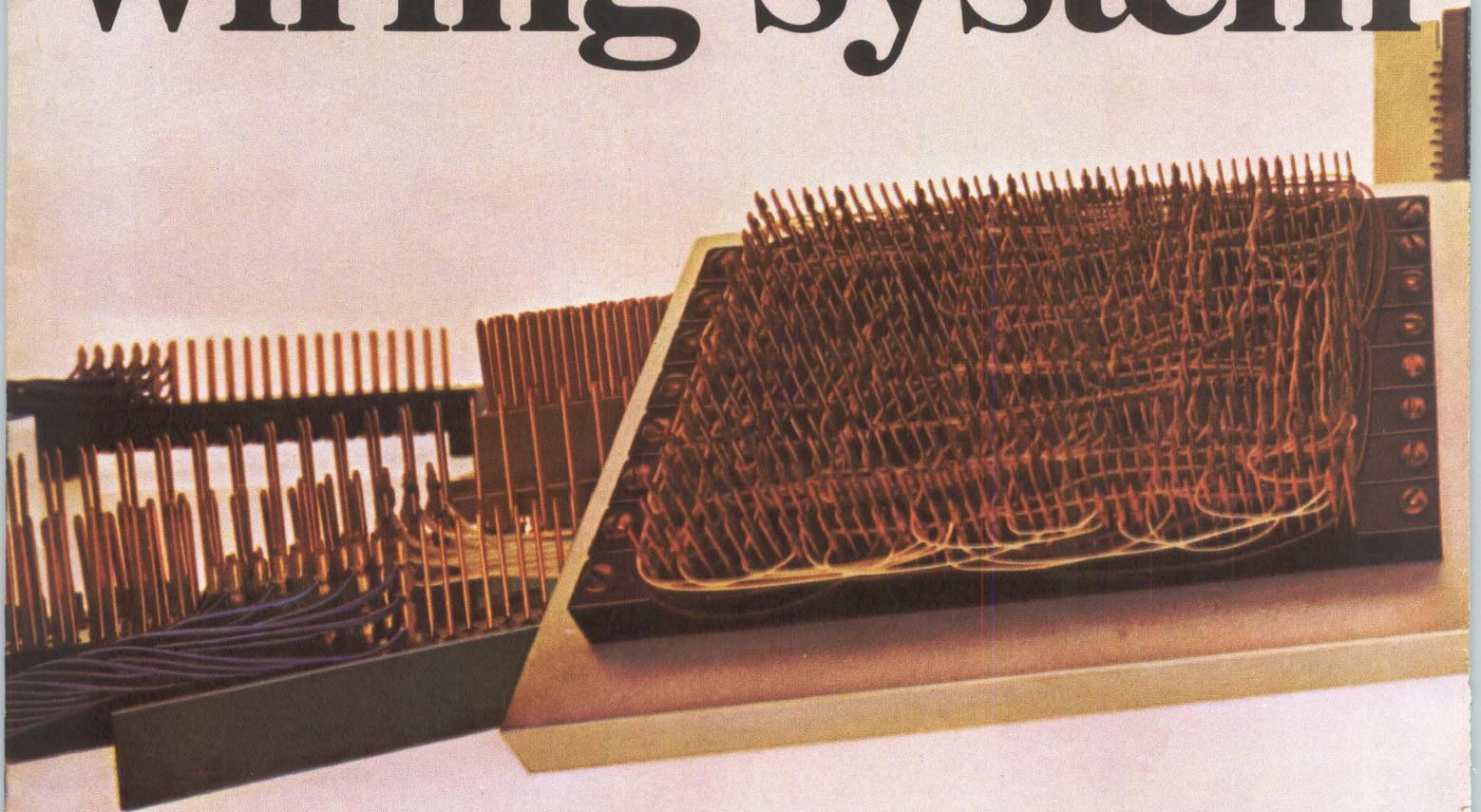
The 703 interfaces with all standard peripherals, including disk. Beyond this, Raytheon Computer offers extensive and compatible IC analog instrumentation like the MINIVERTER™ (multiplexer, sample-and-hold, and A/D converter) assembled from IC analog and digital modules. The complete line of modules and hardware is available for easy system design to your particular requirements. And you can even order your system wire-wrapped, to save you more time, money and sweat.

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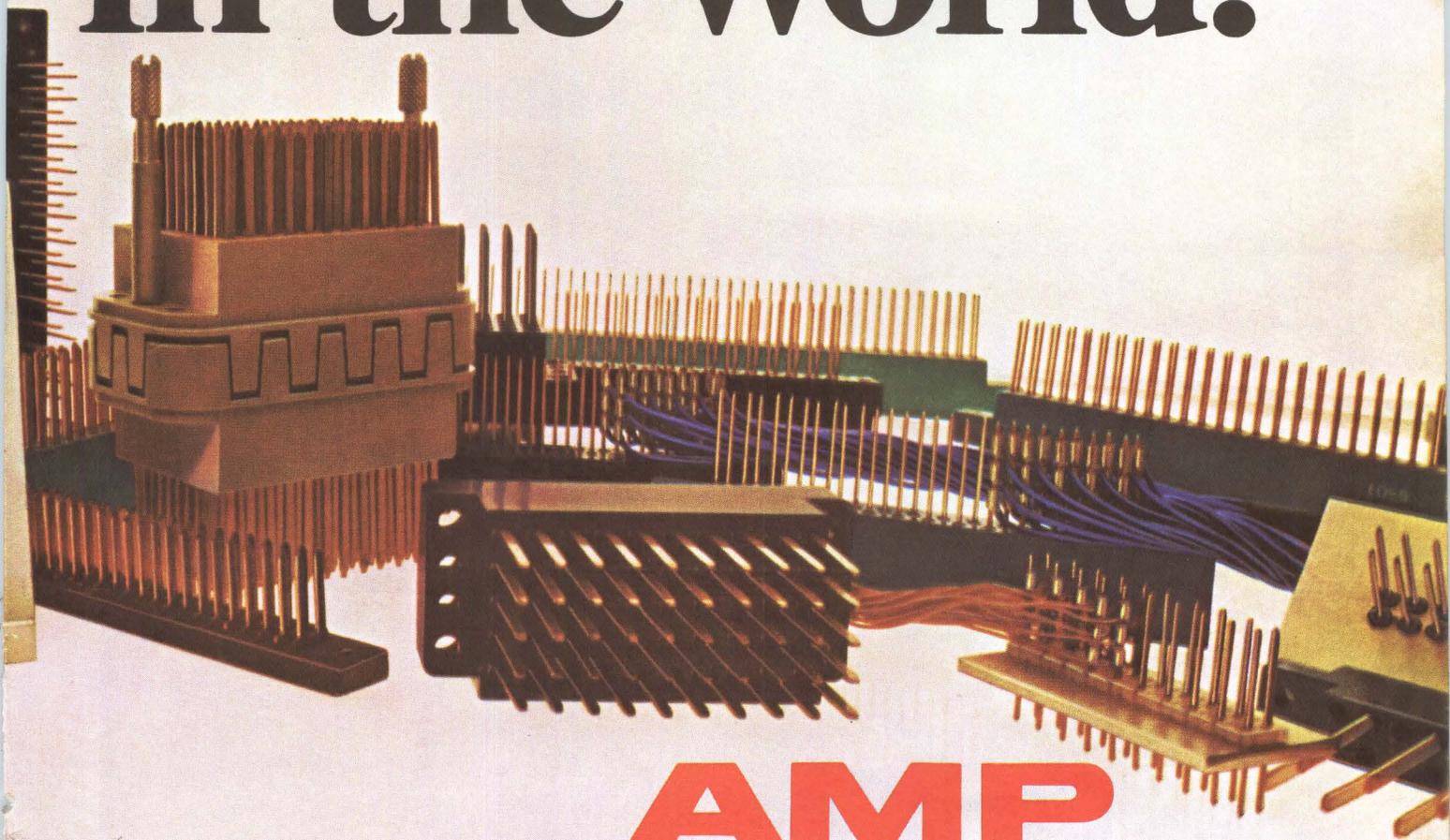
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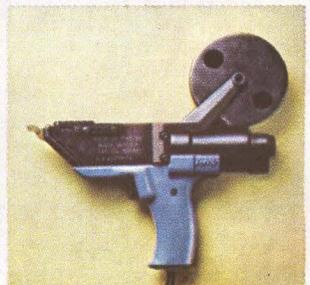
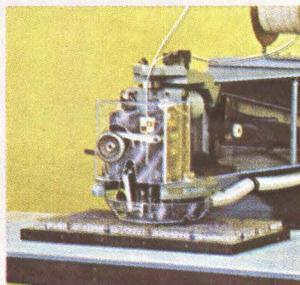
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system operates on a description of allowable topologies and their associated cost-performance functions. In addition, it considers the descriptions of incoming processes to produce altered topologies and assignment of tasks. Conceivably, this machine could emulate the two previously described.

To obtain a more conventional and practical proposal for a system organization which has an inherently better utilization of LSI, the first step is to partition functionally the data paths into groups of data registers and an associated processing matrix.⁵

The unique feature of many new proposals of system architecture is a second step which subdivides control into functionally independent partitions and distributes these partitions among the data path arrays. In effect, this step separates information transfer control from data process execution control.²²

Peripheral Units

No matter how small, inexpensive, and reliable we build the central processor of future systems, the electromechanical peripheral units required for bulk information storage, input/output, and man-machine communication will be the limiting factor in reliability, speed, and maintenance cost. Today, peripheral units comprise more than 50% of the value of shipments by computer manufacturers and by far the major maintenance expense.

Of course, the cost of electronics associated with peripherals will be drastically reduced by LSI. But the promise of LSI is greater than that. Functions that are now handled by mechanical parts will be performed by electronics. More logic will be built into terminals, and I/O devices such as graphic displays, in which the major cost is circuits, will come into more general use.

The peripheral equipment designer will be able to afford more electronic circuits for checking the operation of the remaining mechanical parts and for maintenance.

IMPACT OF LSI ON THE CIRCUIT LOGIC AND SYSTEM DESIGNER

The New Outlook

The first two generations of computer hardware were designed under the "First Law of Computer Design"—MINIMIZE. Elimination of the last unnecessary or redundant diode was paramount in the designer's mind. Much time and money has been spent developing analytic methods for achieving this principle. The literature is packed with many elegant and even some practical minimization techniques.

Spectacular cost reductions realized by the advances in integrated circuits have brought the cost of an entire logic circuit to a level that is lower than many of the individual components of a few short years ago. The basic generality of multifunction packages and arrays introduces inherent inefficiencies in circuit usage. On the other hand, these arrays offer the designer new and perhaps previously unrealizable logic organizations. The decrease in processor size due to LSI will allow a considerable increase in speed because of the shorter lead lengths.

It is difficult to visualize an error-free translation from unit-logic specification to large-scale integration and first-pass perfection in masks. There is now, more than ever, a great need for logic and system simulation techniques. Errors detected in a prototype are not going to be corrected by changing discrete backboard wires. The designer must have a high confidence in his design before he commits it to hardware.

The current interconnections and the device geometrics in LSI are becoming so minute that it is very difficult to breadboard circuits. Furthermore, the devices have non-linearities that make hand computations long and tedious. The circuit designer must place increasing reliance on computer-aided circuit design. The Net 1 program, which has been used extensively at Honeywell, is illustrative of the power of available circuit design programs. Complete AC, DC, and transient analysis can be obtained by feeding into the computer the value and placement of the parts in the circuit. Complex interconnected networks with as many as 40 transistors, 75 diodes, and 400 resistors, inductors, and capacitors, can be analyzed.

Improved design automation methods will be needed to generate the required interconnection masks. Where large memory arrays are needed, discretionary wiring principles may be implemented if good yields are to be realized. The designer must take this into consideration from the very start of his design.

To implement the device phase of the design process, computer languages have already been developed to permit the designer to describe the patterns and structures required.²³

The language is a convenient, shorthand way of assisting the designer in generating proper masks with the minimum likelihood of error. It permits him to express his design by means of an easily-learned but powerful language and, from that point on, rely on a computer to generate the actual masks.

The mask-generating procedure is initiated when the designer draws up a representation of the mask to be produced. The designer specifies the set of statements in the layout language (they may even

be Boolean equations) which is then fed to a computer to produce a plotted representation of the desired mask. If necessary, the statements may be corrected and a new plot obtained. This process is repeated until the designer is satisfied. In the last steps, a magnetic or paper tape is produced to control an automatic drafting machine which actually generates the art work.

CONCLUSION

Several years ago, the high manufacturing yield of discrete transistors showed that larger devices — integrated circuits — were practical. Now, the increasing yield of integrated circuits points to the feasibility of a still more complex semiconductor device — LSI. This evolutionary process has been occurring at a rapid rate and has resulted in sharply decreasing costs for computer logic and functional elements, such as scratchpads, shift registers, and associative memories.

Between the second and the middle of the third generation of computer systems, circuit costs have decreased by a factor of 10 due to this rapid progress in semiconductor technology. It is not difficult to foresee another factor of 10 decrease in the next decade. This progress has widespread implications for the systems designer. The economic basis of design trade-offs has shifted widely. It will be possible to use circuits much more freely to effect savings in: Maintenance, Software, Mechanical Parts, User Training, Data Compatibility, and Program Compatibility. Like all profound advances, LSI presents new problems. The best way to use it has not been found. Certainly the logic structure of peripherals will not change and LSI will find wide use there. However, the number of functions performed by electronics will increase compared to the number of mechanical functions. In central processors, the application of LSI is not as clear. This much is obvious — LSI scratchpads, registers, buffers, and associative memories will be used in large quantities. But this leaves a large portion of the logic where a new approach is needed. Perhaps some of the new schemes for processor logic and partitioning now under study will provide the answers, or perhaps the fabrication cost of non-repetitive, low-volume circuits can be reduced through automation. Work is proceeding in both directions and, while the new design approach is not yet clear, the effects of the design process are certain.

A higher degree of automation in the computer design process will result, principally due to the impetus of LSI. Improved simulation programs will result in high confidence in the accuracy of designs. Documentation for manufacturing, testing, and maintenance will be automatically produced.

One can now look forward to placing all the logic of a peripheral on one chip, and the ultimate implication of LSI is an entire computer on a chip.

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STANDARD V_{out} SETTING (INTERNAL) 12.000 \pm 25 mV				
Characteristic	Min.	Typ.	Max.	Units
Line Regulation V_{in} (15V \pm 10%)		.75	2	mV
Load Regulation I. 0-100 mA		.75	2	mV
Thermal Line Regulation (Per 100 mW Δ Pwr. Dissap.)		1	2	mV
Thermal Load Regulation (Per 100 mW Δ Pwr. Dissap.)		1	2	mV
Ripple Rejection (DC to 100 Hz)	80	90		dB
(100 Hz to 10 kHz)	50	80		dB
Output Z (DC to 100 Hz)		.003	.005	Ω
(100 Hz to 10 kHz)		.075	.1	Ω
Temperature Stability V_{out} Max. - V_{out} Min (-55° to $+125^\circ\text{C}$)		10	20	mV
Long Term Stability 1000 hrs.		± 10		mV

The NC562 can be externally adjusted to any other output voltage from $+10\text{ VDC}$ to $+20\text{ VDC}$ while maintaining identical precision. Custom variations are also available internally pre-set to voltages within this range.

To guarantee ultimate reliability and consistency of operating specifications, each NC562 is subjected to the following 100% preconditioning:

UNIT PRECONDITIONING (100%)		
High Temp. Bake $T_A +175^\circ\text{C}$	24 hrs. min.	Non-Operating
Power Burn In $T_A +125^\circ\text{C}$	168 hrs.	300 mW
Constant Acceleration	Y_1 orientation 20,000 G 1min	
Gross Leak	$\gg 10^{-8}$ cc/sec	
Fine Leak	$\leq 10^{-8}$ cc/sec	

The NC562 is available in a 12 lead, 0.5 inch diameter hermetically sealed TO-8 style can.

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(In Europe contact General Instrument Europe, Via Turati 28, Milano, Italy.)



An example of the extension of third generation design techniques to the manufacturing process is the automatic wiring verifier described in this article. Final test time on production equipment chassis has been reduced considerably by the use of the tester. Wiring verification set-up time, always a problem, has virtually been eliminated.

AUTOMATIC WIRING VERIFIER

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Scientific Data Systems
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With the advent of the third-generation Sigma digital computer, SDS recognized that it was necessary to develop a new test media to verify the integrity of back panel wiring for digital computer logic — one that would minimize human intervention and maximize wiring integrity.

The newly developed test media AWV (automatic wiring verifier) replaces a manually operated tester known as the "octopus" — so named because of many cables extending from the tester. With the octopus, half of the cables were connected manually to the chassis under test and the other half connected to a master chassis of known wiring configuration. The corresponding wire in the cables from the unknown chassis and the master were tied to a node through equal value resistors. The test was performed at each junction by applying +150 VDC to the unknown side and -150 VDC to the master side. Any wiring error would cause voltage off balance at the node, and the lamp associated with the node would illuminate.

Although the octopus seems primitive compared to present standards, it still serves its function splendidly for the SDS second generation 9-Series computers. A time study of the octopus operation showed that to test a 32-connector (47 pins per connector) chassis took approximately 1 hour and 30 minutes as follows:

12%	Set-up
38%	Test
25%	Fault isolation
25%	Repair

The wiring verifier now used to test backpanel wiring

features an automatic inserting fixture that reduces set-up time from approximately 30 minutes (for 3 high-chassis of 32 connectors each) to 25 seconds. Test and fault isolation time is reduced from almost 3 hours to approximately 12 minutes. Furthermore, repairs (based on automatic error type-out) are made off-line.

AUTOMATIC WIRING VERIFIER

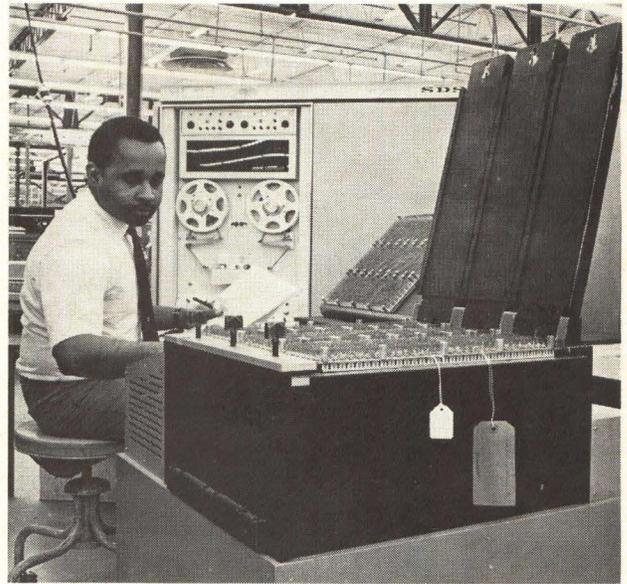
The automatic wiring verifier (AWV) is a computer-based test equipment comprising a SDS 910 computer with 8K of core memory, a 300 char/sec photoelectric paper tape reader, a 1500 char/sec Magpak magnetic tape system and 15 char/sec typewriter used for operator control. The photoreader is used primarily to load the resident executive program and to perform diagnostics on the computer complex. The AWV and the computer communicate via the POT (parallel output) and PIN (parallel input) lines.

The AWV proper consists of four bays of control electronics and switching matrices to verify the integrity of the logic back-panel wiring. Each "motherboard" or housing for the electronic modules associated with the Sigma Series computer is tested individually and connects to the AWV via an automatic insertion fixture capable of making connection to a maximum size motherboard (three high) in less than 25 seconds.

To test the integrity of connector contacts on a motherboard, the motherboard is connected, at the electronic module plug-in points, to the AWV. Once

connection is made, verification of wiring can begin. During the course of the test, two categories of errors are typed out: missing wires and extra wires (or a combination of the two). The words "missing wires" and "extra wires" are used rather loosely. In fact, a missing wire can be a broken etch on the motherboard or a physical wire. An extra wire is any short less than 1.5K ohms to a pin not part of the string. (It should be noted that although a specific error location can be given for a missing wire, it is not practical to isolate electronically the exact point to which an extra wire is tied.) Error typeout indicates the category of error and the error locations. The source number (a number assigned to each wiring string and thus, a number that provides a cross reference to the wire list) is also typed. This capability allows testing for high impedance as well as for wiring errors. Every wiring string and internal etch is verified. Furthermore, all "empty pins" are tested to verify that they are, in fact, empty.

The need for the master chassis (used with the octopus) is eliminated by the connection test list (CTL). The CTL and its revision control will be discussed after the hardware is described.



Automatic Wiring Verifier (AWV) controlled by an SDS 910 computer. Automatic insertion fixture reduces set-up time (for 3-high chassis of 32 connectors each) from approximately 30 minutes to 25 seconds. Test and fault isolation time is reduced from almost 3 hours to approximately 12 minutes. Repairs, based on automatic error typeout, are made off line.

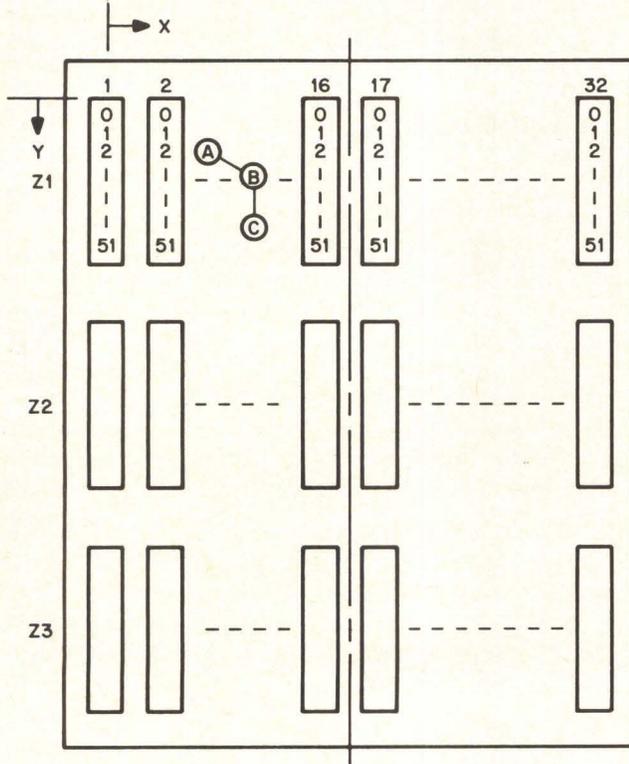


Fig. 1 Motherboard test configuration.

MOTHERBOARD DESCRIPTION

Motherboards are single chassis, double chassis, and triple chassis configurations in which a chassis consists of 32 connectors of 52 pins each. Combinations of various size motherboards are interconnected to a maximum size of nine chassis. The AWV is capable of testing one-, two-, or three-chassis motherboards.

For purposes of test and description the following three-dimensional matrix subdivisions were chosen:

X-AXIS: 1 to 32 connectors

Y-AXIS: 0 to 51 pins

Z-AXIS: 1 to 3 chassis (expandable to 9 chassis with additional hardware)

A unique definition of the XYZ point will specify a point or pin on the motherboard. A typical three-chassis motherboard is shown in Fig. 1.

TEST METHODOLOGY

A typical test on a wiring string is performed as follows: Point A, which is geometrically the uppermost left-hand point on the string, is designated as the "activation point" and is grounded via the Select Matrix. All other points on the motherboard are electronically scanned to find those points on the motherboard that are connected to Point A. In the example given in Fig. 1, points A, B, and C will be detected. The scanning operation is performed via the Scan Matrix. If the correct string points are known, the information obtained from the scan operation permits the integrity of the string to be verified. If there is a wiring error, its type and location are

evident; missing-point and/or extra-point wiring error can be deduced.

SELECT OPERATION

Figs. 2 and 3 show a block diagram of a typical select operation on a single-chassis motherboard. It has not yet been determined where and how the parallel output (POT) data is obtained, nor the origin of the increment command as shown in the figure. Let us assume for the time being that the data and the command are available to fit our needs. To select any one of the 1664 points ($52 \text{ pins} \times 32 \text{ connectors}$), the X and Z registers are employed, and the stepper switch is advanced or stepped "Y" amount of times. On Fig. 2 it can be seen that the ground path to the particular "activation point" is established through the Z relays that provide path from the wipers of the steppers to the 32 X relays. One of the 32 X relays is picked, thus providing a path to ground. The position of the stepper determines the pin selected.

SCAN OPERATION

The scan operation, as opposed to the select operation (where any one point in the matrix can be specified electronically), interrogates the matrix or motherboard in a group of 16 points at a time. To accomplish this, the matrix was split in half. As shown in Fig. 1, the motherboard was divided into two sectors so that all pins located on connectors 1 through 16 are in one sector (defined by $X = 0$), and those pins located on connectors 17 through 32 belong to the other sector ($X = 1$). The "Y" and the "Z" axes are defined identically as before. Thus, a unique state of the XYZ matrix in scan operation defines a group of 16 pins whose pin numbers and chassis levels are identical.

Hardware required for the scan operation is shown in Figs. 2 and 4. The actual scan is controlled by the scan counter whose register configuration is shown in Fig. 4. The "X" bit is the least significant bit of the counter followed by "Y" and "Z" bits, respectively. The "Y" portion of the counter is capable of 52 states and the "Z" portion counts to 9 states. As previously noted, a nine-high (nine-chassis) motherboard is the maximum interconnecting configuration.

The scan matrix itself is essentially $(X) \times (Y) \times (Z) = 4992$ OR gates of which 16 gates are energized or gated-on at any specific state of the counter. There are 16 outputs, corresponding to the 16 energized gates, which are stored in the continuity register. These outputs, together with the state of the scan counter, can define a unique point in the matrix. The counter starts at all zero states and advances one sector at a time until the state of the counter equals the state of the scan limit register. The content of the scan limit register is prestored and is dependent upon the size of the motherboard under test.

In Fig. 1, the scan operation is performed from pin 0 of the upper left hand sector of the motherboard through pin 51 at the lower right hand sector.

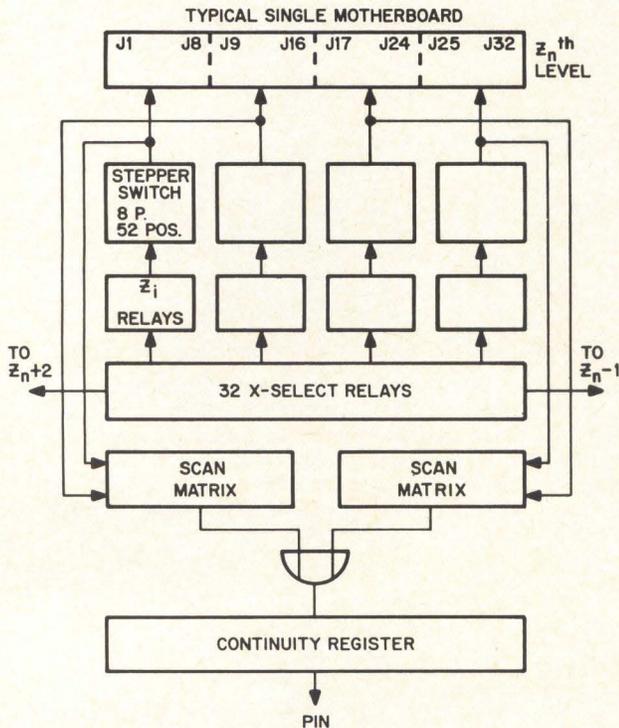


Fig. 2 Hardware configuration.

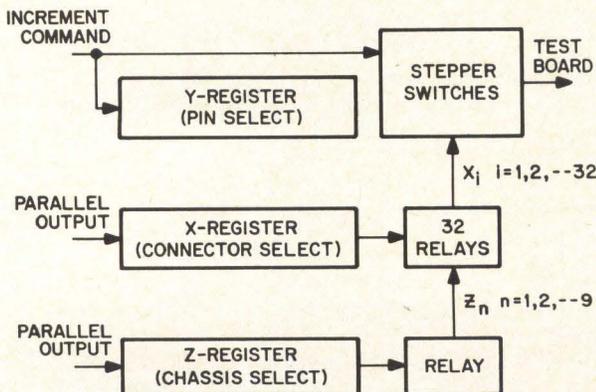


Fig. 3. Select operation.

SYSTEM OPERATION

The total AWW hardware configuration is illustrated in block diagram form in Fig. 5. The resident executive program in the SDS 910 computer controls the sequential nature of the AWW operations by means of the following interface signals:

1. Parallel output (POT) operation is always preceded by an EOM (energize output memory) command. This allows direct output from the memory of 24 bits in parallel to any register selected by the preceding EOM command.

2. Parallel input (PIN) operation is likewise always preceded by an EOM command. This allows direct input into the memory, a 24-bit word from an external system.

3. Interrupt and SKS (skip if signal not set) commands are means by which the communication path from an external device to the computer is initiated. Whenever the AWW must communicate with the computer, an Interrupt is given. The computer gives immediate service to the originator of the Interrupt and interrogates (by means of the SKS operation) the Interrupt. Depending on the reason for the Interrupt, the computer takes the appropriate action. Hence, the interrupt capability allows efficient use of the computer time.

4. EOM operation, described previously, can be used as a command signal. For example, in the previous discussion of the select operation, an EOM command was used to increment the stepper switch. In a like manner, it can be used for such commands as System Reset, Start, Stop, etc.

A typical test sequence can now be examined in light of this interface capability (see Fig. 5). The activation point is first established by means of the EOM-POT operation into the X and Z select register. The Y-stepper is advanced by appropriate increments and the scan limit register is set to the maximum scan position of the motherboard under test by means of the EOM-POT operation. The starting point of the scan counter is POTed and the Start Scan EOM is given.

The scan counter is advanced automatically until continuity is detected or scan limit has been reached. In either case, an Interrupt to the computer is given. The computer interrogates the AWW via SKS commands to determine the source of the Interrupt. If the Interrupt was caused by the continuity detector, the continuity register and the scan counter are PINed for subsequent comparison with the proper string list contained on the connection test list (CTL), described later. If the source of the Interrupt is the scan limit detector, the program is returned to the executive region to verify the integrity of the string just tested. If an error is detected, the error information is stored in a stack table, and the error message is typed whenever the computer is idle to do so.

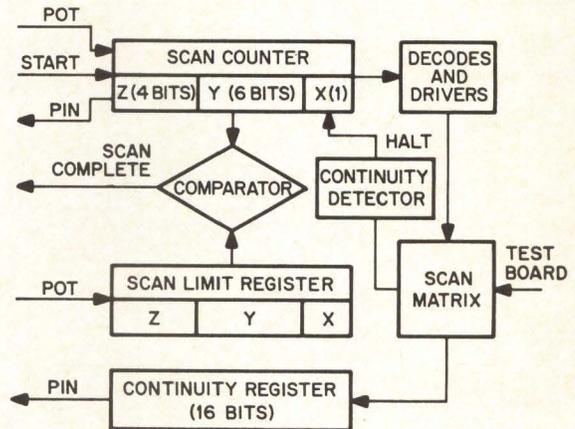


Fig. 4 Scan operation.

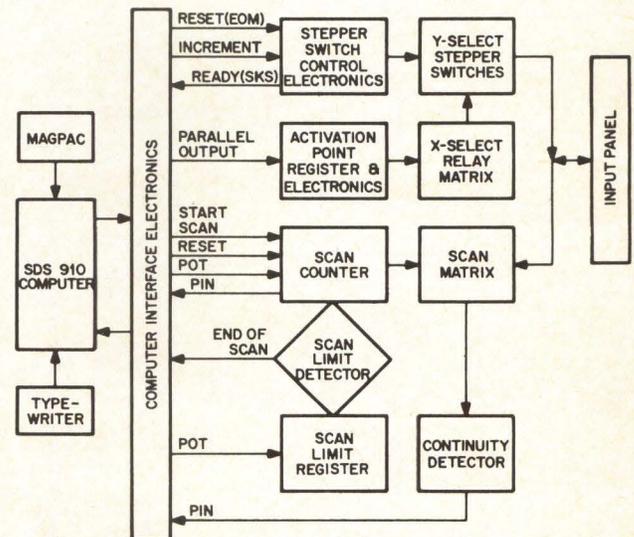


Fig. 5 AWW block diagram.

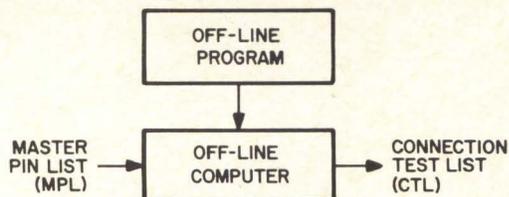


Fig. 6a Off-line operation.

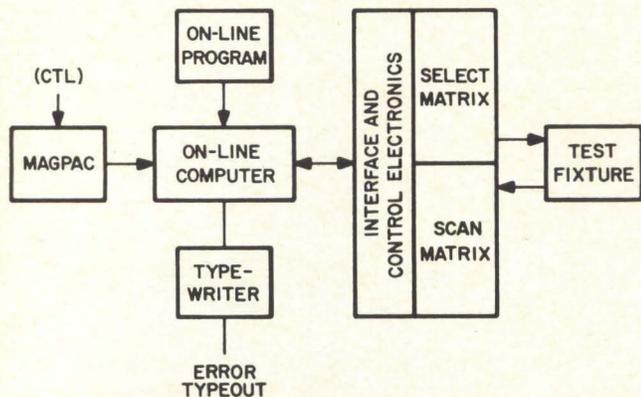


Fig. 6b On-line operation.

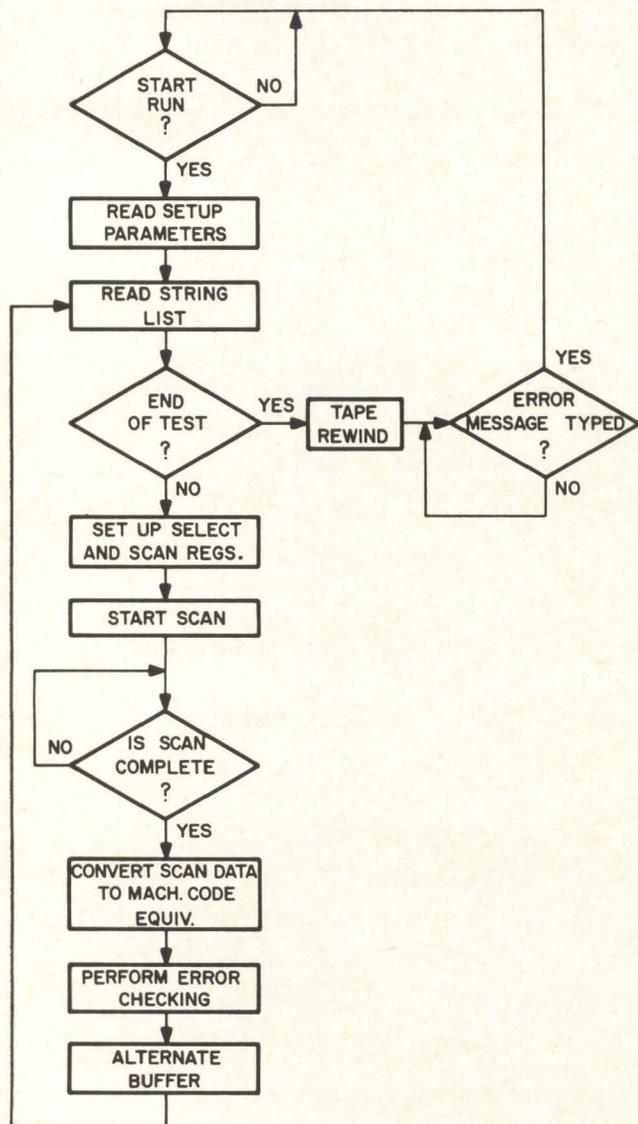


Fig. 7 AWW executive program-flow diagram.

To aid the assembly personnel in quickly and accurately correcting the wiring error, the error typeout must contain the error category, location of error, and the cross referencing information to the wiring book or stringlist. The error categories are missing point (MP) and/or extra point (EP), which can be deduced by merely comparing what the string should have been (CTL input via Magpak) to the string information indicated by the AWW.

The above sequence of operation is repeated until all wiring strings on a motherboard have been verified.

CONNECTION TEST LIST

The CTL is generated for each unique chassis assembly and is written on a magnetic tape cartridge (Magpak cartridge). Each Magpak cartridge holds 600 feet of Mylar-base tape containing two independent tracks of information with 1.5 million characters (6 bits plus parity) per track. This is sufficient to record on a single track all information necessary to test a maximum size motherboard.

Generation and revision of wire lists for every chassis to be tested on the AWW is accomplished by the SDS Design Automation Group. Complete wiring information is recorded on a magnetic tape file designated the Master Pin List (MPL). Whenever a new wire list is generated or an old one revised, a CTL is generated automatically. In this manner, every motherboard tested on the AWW is tested in accordance with the latest revision. (Refer to Fig. 6a & b.)

The first information contained on the CTL is the assembly drawing number and the chassis letters. As was mentioned earlier, the maximum number of chassis in a rack is nine, interconnecting various sizes of motherboards. Position of the chassis in the rack is designated by a letter in the alphabet known as the chassis letter.

To insure that the wrong CTL is not used, the operator types in the assembly number and the revision letter of the motherboard to be tested. When the CTL is read, the assembly number on the CTL is compared by the resident executive program with the number requested by the operator. The test is continued only if the numbers match.

Subsequent information on the CTL is blocks of test information, each block being grouped as follows:

- Source number—a unique number assigned to every wire string in a given assembly.
- Activation point—the pin that is grounded by the select matrix.
- String points—a list of string pins in the order that the motherboard is wired.

The end of the CTL is indicated by a file marker.

Fig. 7 shows a flow diagram of the executive program operation. Although not indicated in the figure, the interrupt capability enables error messages to be typed out while tests are in progress.

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This article presents equations for calculation of system "Transfer of Information Bits" (TRIB) and block lengths which will maximize the system. Derivation of the equations is detailed. Factors which affect the system are discussed and TRIB curves and optimum block length are shown.

TRANSFER RATE OF INFORMATION BITS

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The digital data transmission system is becoming an increasingly important part of information processing systems. Where the processing equipment formerly operated in an isolated environment, there are now many applications where information is entered and retrieved from geographically remote locations through a data transmission system. Data thus entered and retrieved is usually required to be placed in a format acceptable to the transmission equipment. The result of this formatting is the transmission of non-information bits (as far as the processing equipment is concerned) in the form of control characters. It is also necessary in many instances to ensure that data is not modified in the transmission process. This is normally accomplished by transmitting redundant bits in the form of special codes or parity bits for the purpose of detecting and/or correcting errors. These redundant bits, likewise, convey no useful information to the processing equipment.

USASI Sectional Committee X 3 has published a tutorial paper* in which the "Transfer Rate of Information Bits" (TRIB) is presented as a standard means of testing and grading data transmission systems. TRIB, as proposed by USASI, is defined as the (number of information bits accepted by the sink) divided by the (total time required to accomplish the transport of all bits required to get those information bits accepted) and does not consider residual (uncorrected) errors. TRIB, in conjunction with a measure of residual errors, could benefit the data transmission

system user by providing a method of comparing the many various equipments and services available. It could also serve as a useful tool for the data transmission system designer since the transfer of information is his primary goal.

The USASI paper lists examples of TRIB calculation and measurement. The article presented here will deal only with calculation and, in particular, the system parameters which affect TRIB. The equations and optimum block length are written in terms of known system parameters such as transmission rate and error rate. From these equations one can deduce the effect that any one parameter will produce on the system.

CALCULATION OF SYSTEM TRIB

In a two-way alternate data transmission system which employs re-transmission of blocks which are detected to be in error, the system may be calculated as*

$$\text{TRIB} = \frac{k(m-c)(1-r)^m}{t + m/v} \quad \text{bits/sec}$$

where,

- m = transmission block length (characters)
- v = transmission rate (characters/second)
- r = character error rate (errors/character)
- k = information bits per character (bits/character)
- c = non-information characters per block (characters)

t = time between transmission blocks (seconds).

* See Appendix A for equation derivation.

* *Communications of the ACM, Vol. 8, No. 5, May 1965, pp. 280-286.*

Since some of these parameters may not be constant (e.g., error rate) average values are assumed in the equation. The non-information characters include transmission formatting characters such as SOH, STX, and ETX (ASCII code), all characters appearing in a heading which are not used by the processing equipment, any characters used to correct errors (such as back space—delete), and any parity characters. It is expected that a "standard list" of non-information characters to be used in calculating TRIB will be specified by USASI.

The time between transmission blocks, t , normally will consist of two line-turn-around times, the reply time, and two-way propagation time. If it is desired to include setup time, handshaking time, etc. in the TRIB calculation, an average (per message) value for each should be calculated and added to t . If retransmission of blocks received in error is not employed, the $(1-r)^m$ term in the equation should be eliminated.

BLOCK LENGTH FOR MAXIMIZING SYSTEM TRIB

For a given set of system parameters, the optimum block length (for maximum TRIB) can be calculated as*

$$M_t = \frac{c-vt}{2} + \left[\frac{v^2 t^2}{4} + \frac{cvt}{2} + \frac{c^2}{4} - \frac{vt+c}{\log e(1-r)} \right]^{1/2}$$

SAMPLE CALCULATIONS AND CURVES

The equation for calculating system TRIB may be inconvenient to use because of the term $(1-r)^m$. This term may be replaced by the approximation $(1-mr)$ which is more convenient to calculate. The TRIB calculated by using this approximation will be low by less than 5% if the product mr is less than about 0.28.

Fig. 1 shows the results of calculations using the exact and approximate TRIB equations. The right-hand column illustrates the relation between TRIB and information characters/second. The system parameters used for this illustration are as follows:

$$v = 2000 \text{ bits/sec.} \times 1/8 \text{ character/bit} = 250 \text{ characters/sec.}$$

$$k = 7 \text{ bits/character (8th bit is parity)}$$

$$r = 10^{-4} \text{ errors/bit} \times 8 \text{ bits/character} \times 0.5 = 4 \times 10^{-4} \text{ errors/character}^{**}$$

$$t = 2 \times .150 \text{ sec. (line-turn-around time)} + .050 \text{ sec. (reply time)} = .350 \text{ sec.}$$

$$c = 12 \text{ non-information characters/block.}$$

Computer programs were used to generate curves of optimum block length vs. bit error rate E for common transmission rates in synchronous and asynchronous systems. These curves are presented in Figs. 2 and 3, respectively.

* See Appendix A for equation derivation.

** Bit error rate as used in this article refers to the effective bit error rate denoted E . This is less than the actual bit error rate because errors which occur during a 150/200 millisecond line-turn-around do not affect transmission of data. The 0.5 factor is used since two bit errors will result in one character error on the average, because of bit errors occurring in bursts.

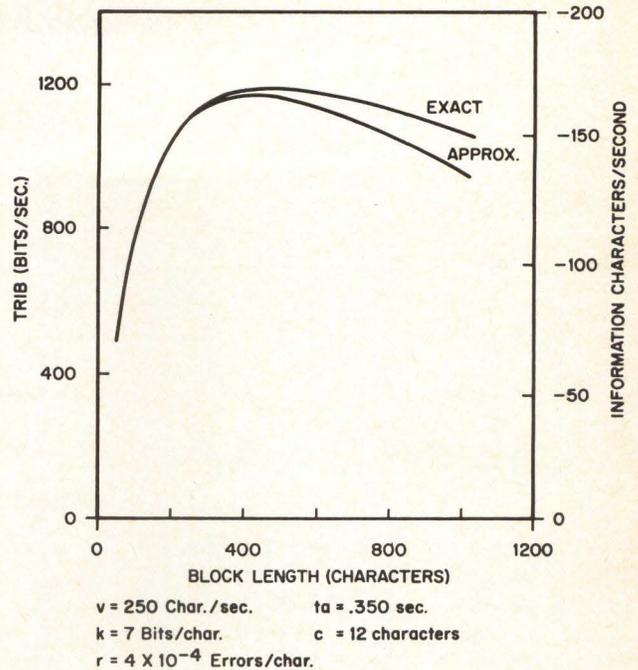


Fig. 1 Error resulting from TRIB approximation.

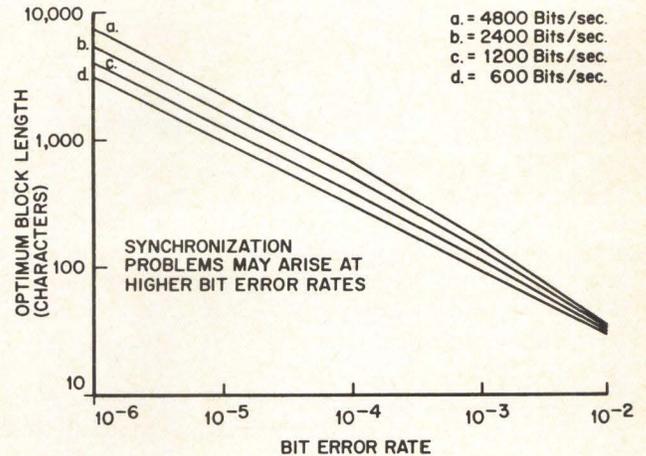


Fig. 2 Optimum block length for synchronous transmission.

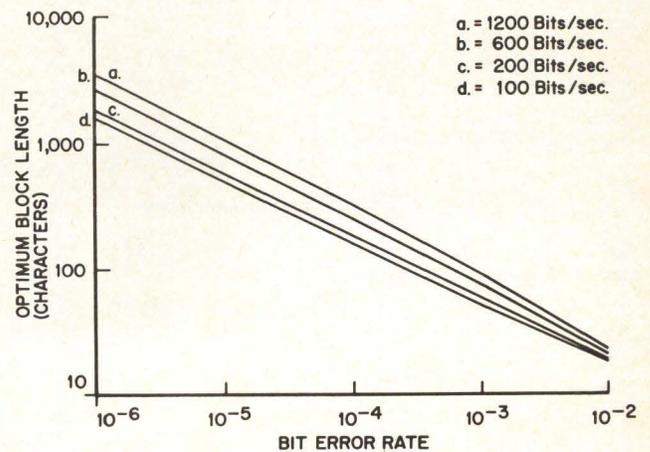


Fig. 3 Optimum block length for asynchronous transmission.

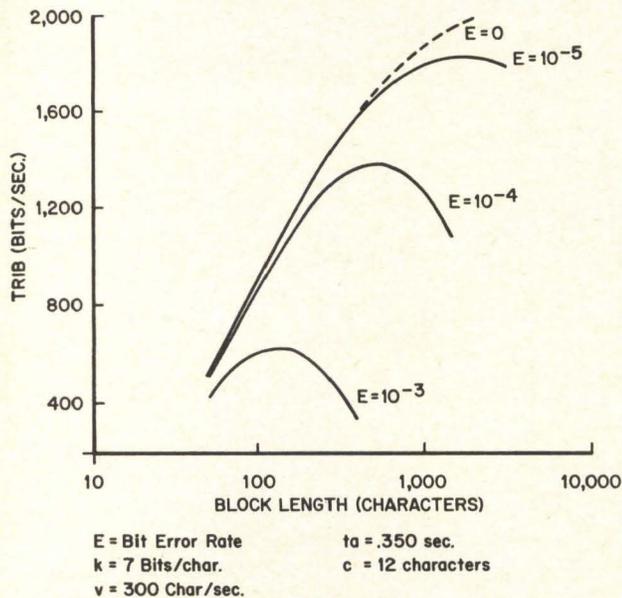


Fig. 4 Effect of error rate on TRIB.

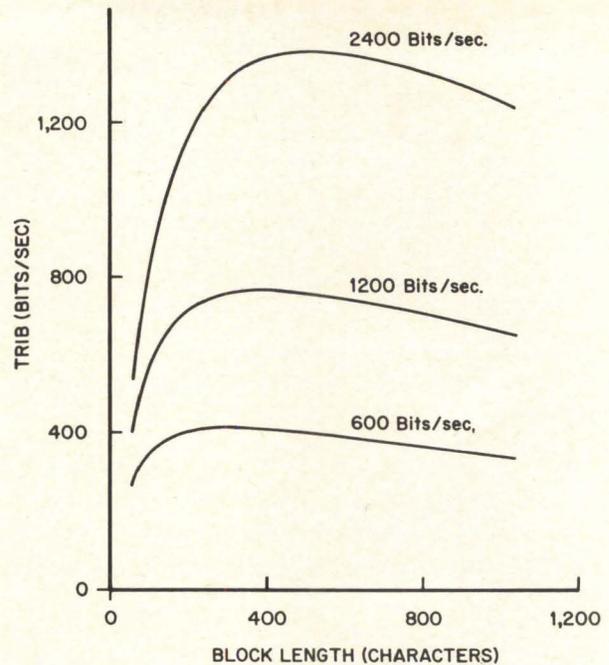


Fig. 5 Effect of transmission speed on TRIB.

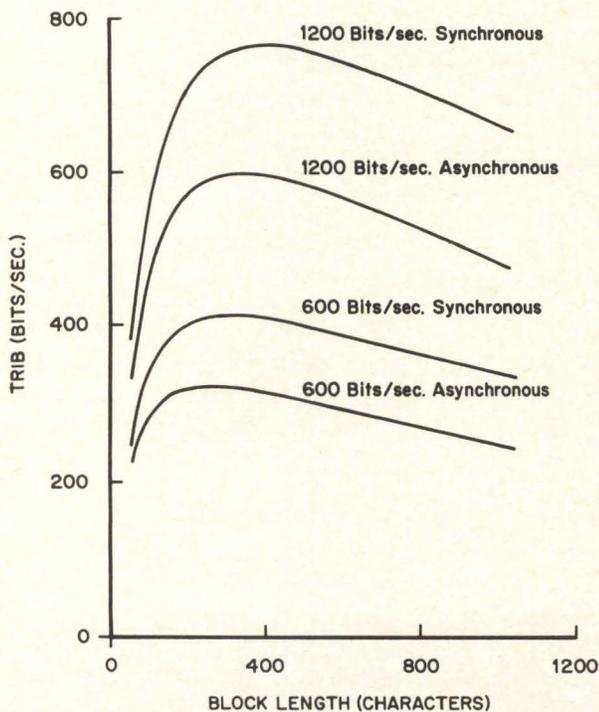


Fig. 6 Comparison of TRIB for synchronous and asynchronous transmission.

The curves for the synchronous system are based on the following parameters:

k = 7 bits/character

c = 12 characters/block

t = .350 sec. (Western Electric 201 Data Set and .05 sec. reply time)

Two bit errors in one character error. (8 bit characters are used)

For the asynchronous system, the following parameters were used:

k = 7 bits/character

c = 8 characters/block

t = .450 sec. (202 Data Set and .05 sec. reply time)

Two bit errors result in one character error. (10 bit characters are used)

The effect of bit error rate on system TRIB is shown in Fig. 4. The broken curve, labeled E=0, gives TRIB values for error-free transmission, and represents the limiting values on TRIB vs. block length for the assumed system parameters. The effect of bit error rate on system TRIB and optimum block length is obvious from the family of curves. While data transmission is possible at an error rate of 10^{-3} (assuming short block lengths are useable) the increase in system TRIB resulting from going to an error rate of 10^{-4} may well justify the delay required to obtain a "cleaner" transmission line.

Fig. 5 shows the effect of transmission speed on TRIB and optimum block length. The family of curves is drawn for a constant bit error rate of 10^{-4} and a constant inter-block time of 0.350 seconds. In reality the inter-block time should decrease slightly as the transmission rate is increased because reply time is reduced.

Fig. 6 gives a comparison of synchronous and asynchronous transmission at given transmission rates. The system parameters used are the same as those for Figs. 2 and 3, discussed previously. It can be seen that, although synchronous transmission requires more non-information characters per block (e.g., 4 synchronization characters), the start and stop bits required for asynchronous transmission result in lower TRIB for a given transmission rate.

CONCLUSIONS AND COMMENTS

TRIB is a measure of a system's information throughput which discounts control characters, redundant bits, inter-block time, and block re-transmission as "lost time" during which no information is conveyed. It can be calculated from known system parameters or measured, as explained in the USASI paper. The user of data transmission systems can use TRIB to compare error correction schemes, transmission formats, etc. of various systems to determine which will transport the required information per unit time. The system designer can compare calculated with measured TRIB, using prototype equipment, to check his design and recommend possible improvements. For a given set of system parameters a block length can be calculated which will maximize TRIB.

The equation for TRIB presented in this paper includes the term $(1-r)^m$ to approximate the probability that a transmitted block will not contain errors and will not require re-transmission. In a particular system application, if the re-transmission rate, X , is known or can be calculated more accurately because of sufficient knowledge of the bit error characteristics, this term should be replaced with $(1-X)$. Since this term is the only approximation used in the TRIB equation, it behooves the user to use the best approximation available.

Strict adherence to USASI's proposed definition of TRIB would require inclusion of equipment downtime, setup time, etc. in the calculation. This can be done by computing an average (per block) value for each and adding to the inter-block time, t . However, since downtime and setup time (such as message typing or card punching) normally will not preclude other use of the transmission channel, the author feels that these should not be included in TRIB. This is a matter to be resolved by USASI.

APPENDIX A

Derivation of TRIB and Optimum Block Length Equations

TRIB is defined as:

$$T = \frac{\text{number of information bits accepted by the sink}}{\text{total time required to get those bits accepted}}$$

which, for error-free transmission may be written as

$$T = \frac{k(m-c)}{t + m/v} \quad (\text{A-1})$$

Since residual errors (non-corrected errors) are not considered in TRIB, it can be seen that if a system does not employ re-transmission of blocks received in error, Equation A1 should be used to calculate system TRIB. Any errors which do occur are considered to be residual errors. If a system employs re-transmission of blocks which are detected to be in error, the time required to get a given number of blocks accepted by the sink is increased by a factor which is a function of the error rate. Conversely, in a given length of time fewer information bits will be accepted by the sink because of time required for re-transmission.

Since r , the character error rate, is a statistical quantity giving the probability that any one character is received in error, $(1-r)$ is the probability that any one character is received correctly. The probability that m consecutive characters will be received correctly is then $(1-r)^m$. This is an approximation since burst noise, the primary source of errors, is not truly random. If a character error is considered to contain two bit errors however, the approximation is fairly accurate. When averaged over a period of time, the number of information bits per message which will be accepted by the sink is $k(m-c)(1-r)^m$. Therefore, for systems employing re-transmission of blocks received in error, system TRIB is given by:

$$T = \frac{k(m-c)(1-r)^m}{t + m/v} \quad (\text{A2})$$

The block length for which TRIB will be maximum can be determined by setting the derivative with respect to m of Equation A2 equal to zero and solving for m as follows:

$$dT/dm = \frac{(t + m/v) [k(m-c)(1-r)^m \log e (1-r) + k(1-r)^m] - k/v(m-c)(1-r)^m}{(t + m/v)^2}$$

$$m^2 + m(vt-c) + vt/\log e(1-r) - cvt + c/\log e(1-r) = 0 \quad (\text{A3})$$

$$m_t = (c-vt)/2 + [v^2t^2/4 + cvt/2 + c^2/4 - (vt + c)/\log e(1-r)]^{1/2}$$

The use of an asynchronous interface between the main storage (MS) and the central processor unit (CPU) in a parallel digital computer is explained in this article. The described interface is used in the IBM Four-Pi family of computers. An asynchronous interface permits the MS characteristics to be changed at any time with no impact to the CPU logic. Thus, the MS characteristics may be adjusted to compensate for remote MS location.

DESIGN OF AN ASYNCHRONOUS MAIN STORAGE — CENTRAL PROCESSING UNIT INTERFACE

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COMPUTER DESIGN GOALS

When the computer designer is given either a set of main store or logic circuit characteristics, he should choose the characteristics of the other variable to give the most cost effective design. A reasonable goal is to perform simple operations (Add, Subtract, etc.) within the time required for main store instruction and data cycles. That is, the designer should strive for a 100% MS duty cycle when executing most instructions. This goal imposes certain restrictions on the computer organization and logic circuit switching time, which in turn, determine the CPU cycle time. The CPU cycle time is the rate at which the arithmetic unit in the CPU can perform successive operations. At first thought, it seems that the CPU cycle time should be fast enough to achieve the desired speed but no faster. However, several considerations may cause the selection of a faster logic circuit and CPU cycle time than absolutely necessary. Three of these considerations are:

- Availability of faster circuits at a slight or no cost increase.
- Thought of future product improvement by using a faster MS.
- Desire to execute those instructions which are not limited by MS cycle time as fast as possible. (Multiply is an example.)

An asynchronous MS-CPU interface will be described by establishing an example machine with detailed timing relationships between MS and the CPU.

CPU TIMING

The timing relationships within the CPU are simpler than the MS timing requirements and will be explained first. A simplified CPU data flow is given in Fig. 1. A CPU cycle is defined as the time required to change the state of the instruction sequencer, add the contents of two registers, and place the result back in

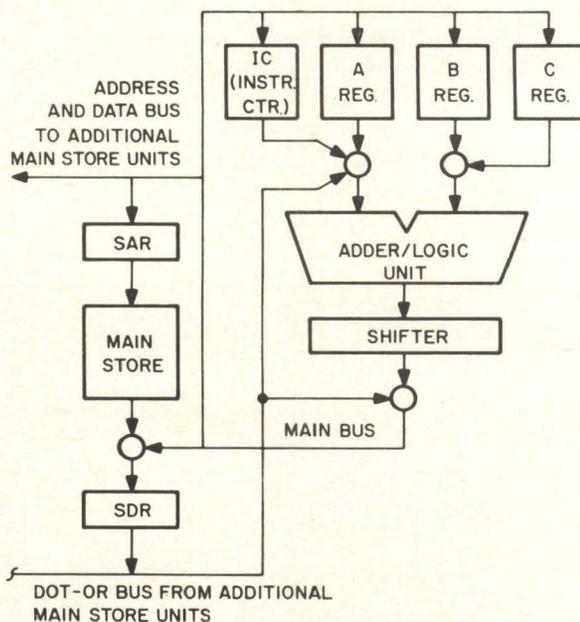
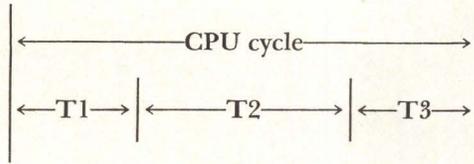


Fig. 1 CPU data flow.

a register. This sequence is illustrated below.



- T1—An instruction control state is entered at T1 time. As an example, this state may command "Add A and B, shift the result right 1, and place it in the instruction counter (IC) and the storage address register (SAR)."
- T2—The addition and shift specified by the current control state is performed during this time.
- T3—The result of the addition and shift is placed in IC and SAR at this time.

The CPU timing in this article has been simplified somewhat for explanatory purposes. In general an instruction sequence state may be entered before the result of the last state operation is placed in a register. That is, T3 and T1 may overlap. This overlap hides the sequencer decode time under data flow operation. These variations have no real impact on the subject at hand but of course must be considered by the computer designer.

MAIN STORE TIMING

The main store timing requirements are more complex than those of the CPU due to the larger number of variables that must be satisfied. These variables and their relationships are explained in the following paragraphs:

Main store access time is the time from the main store "Select" or "Start" signal until the output data is stable in the storage data register (SDR). Main store cycle time is the minimum time required between successive Selects.

Suppose the following rules are given for main store:

- 1) Main store Selects may be given no closer than every 2.4 microseconds.
- 2) The SAR must be stable 200 nanoseconds before a Select is given and until 900 nanoseconds after a Write is given.
- 3) The SDR outputs are available 800 nanoseconds after a Select.
- 4) The SDR outputs must be stable from 100 nano-

seconds before and until 1.2 microseconds after a Write is given.

5) A Write may be given no sooner than 900 nanoseconds after a Select. There is no maximum time limit. A Write command must follow each Select. A Select can occur no sooner than 1.2 microseconds after a Write.

CPU-MAIN STORE TIMING RELATIONSHIPS

After considering the MS timing rules and available logic circuits, let us suppose the computer designer decides to use a 400 nanosecond CPU cycle. Fig. 2 shows the CPU cycles where the MS commands can be given according to the MS usage rules. The following observations can be made concerning the CPU-MS timing relationships in Fig. 2.

- 1) MS is selected in CPU cycle 1. The Select can be given only if MS is available for use and the SAR has been previously loaded.
- 2) CPU cycle 2 is available after MS is selected and before the MS output (SDR) is available. In many cases, no useful calculation can be performed by the CPU during this cycle since the MS output is not yet available.
- 3) The SDR output becomes stable 200 nanoseconds into CPU cycle 3. This leaves sufficient time for the data to be routed to a register (IC, A, B, or C) before T3 time of cycle 3. There is not sufficient time for the output to be routed through the adder and shifter in cycle 3. A store may be accomplished in the minimum time by placing the main bus contents into SDR at T3 time of cycle 3.
- 4) CPU cycle 4 is the earliest time that a Write command can be given. It is also the earliest cycle that the SDR output can be routed through the adder.
- 5) Calculations by the CPU which require the MS output can proceed during CPU cycle 5. MS is not yet available for any other use.
- 6) The SAR can be changed at T3 time of cycle 6 in preparation for the next MS cycle.
- 7) The next MS cycle can be initiated in CPU cycle 7. Cycle 7 and cycle 1 are identical.

After the CPU-MS timing relationships have been determined, it is necessary to define the communication signals required to let the interface operate asynchronously. Two signals called Busy and Advance which are generated in the MS can accomplish the necessary feedback to the CPU. Busy provides information concerning the MS cycle time and Advance

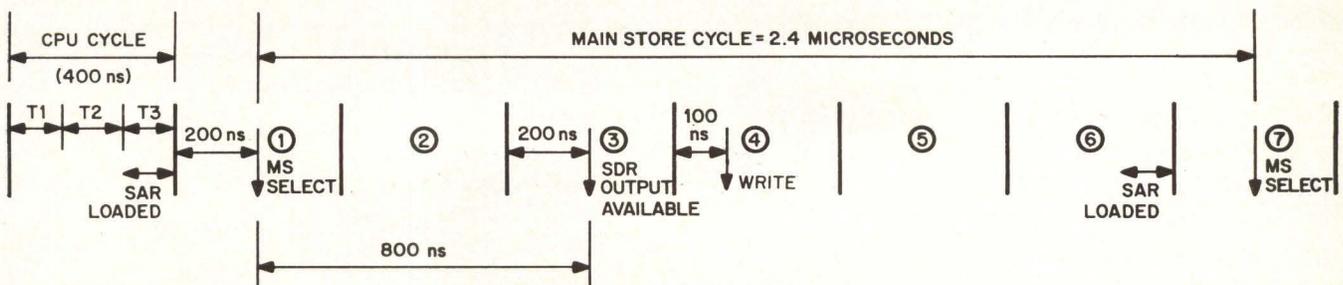


Fig. 2 Main store timing.

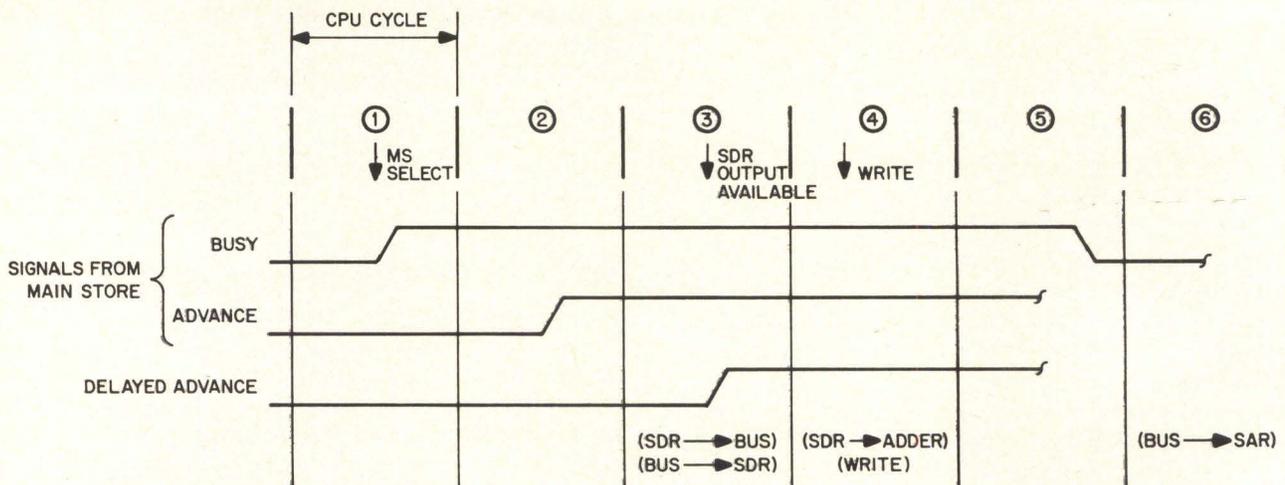


Fig. 3 Main store-CPU interface timing.

gives an early indication of the access time. These signals are defined in Fig. 3. It is assumed that Busy and Advance signals from each MS unit are "dot ORed" onto common Busy and Advance lines which feed the CPU logic.

Two signals are sent from the CPU to MS. They are Select and Write. Additional control signals used in the CPU data flow which require a proper timing relationship with the MS are:

- "Main Bus to SAR" (Bus → SAR)
- "SDR to Main Bus" (SDR → Bus)
- "SDR to Adder" (SDR → Adder)
- "Main Bus to SDR" (Bus → SDR)

The "Main Bus to SAR" command must not be executed until the CPU cycle at which SAR may be changed. The SAR may be changed in CPU cycle 6 or later as shown in Figs. 2 and 3. The "SDR to Main Bus" command may be executed in CPU cycle 3 or later. "SDR to Adder" may be executed in CPU cycle 4 or later and "Main Bus to SDR" in CPU cycle 3 or later. The "Write" command may be executed in CPU cycle 4 or later. The earliest CPU cycles in which these commands may be executed are indicated in Fig. 3 by the commands in parenthesis.

USE OF "ADVANCE"

The following discussion will illustrate the use of "Advance" to:

- Make the instruction control logic independent of MS access time, and
- Reduce the number of instruction control states for the defined MS and decrease instruction execution time when product improvement provides an MS with a faster access time.

Suppose an instruction control state is entered at T1 time of CPU cycle 3 in Fig. 3. This is the earliest control state that can command "Bus → SDR" for the MS which has been defined. The presence of the "Bus → SDR" command and Advance allows SDR to be changed at T3 time of cycle 3. The Advance signal is, of course, unnecessary for the above case where the MS access time is as planned and designed for.

However, suppose after design completion it is found that a remote MS has a longer effective access time due to cable delays. It is then only necessary to delay the rise of Advance by the proper number of CPU cycles. The presence of the "Bus → SDR" command before Advance arrives will cause the CPU timing to be stopped before T3 time. The absence of clock pulses will "freeze" the CPU in its present state until Advance arrives. As soon as Advance arrives, the CPU clocks will start, the proper SDR contents will be placed on the Bus and into a register at T3 time, and computation will proceed as if the clocks had never been stopped. It can readily be seen that if the MS access time lengthened from 800 to 1600 nanoseconds, it would only be necessary to also delay the rise of Advance by an additional 800 nanoseconds. Each MS cycle and CPU instruction execution time would be correspondingly increased, but no change would be required in the CPU logic. Thus, the CPU logic is independent of MS access time.

As was pointed out earlier, CPU cycle 2 in Fig. 3 is available after MS is selected and before the output is available. In many cases, no useful calculation can be performed by the CPU during this cycle. An asynchronous interface permits this state to be omitted from the instruction sequencer. The sequence state following cycle (state) 1 can command "Bus → SDR." The absence of Advance will stop the CPU until Advance arrives. When Advance does arrive, the command will be executed. A reduction in MS access time from 800 to 400 nanoseconds would reduce instruction execution times by one CPU cycle for those instructions that do not use CPU cycle 2. This increased speed would be achieved with no CPU logic changes. If CPU cycle 2 is used in an instruction sequence, the faster access time would not affect execution time.

USE OF "BUSY"

The Busy signal indicates the MS cycle time and is used to:

- Make the instruction control logic independent of MS cycle time, and

- Reduce the number of instruction control states for the defined MS and decrease instruction execution time when product improvement provides a MS with a faster cycle time.

The storage address register (SAR) normally cannot be changed until CPU cycle 6. The instruction control state entered at T1 of cycle 6 can command "Bus → SAR" and the command will be executed since Busy is down at that time, as shown in Fig. 3. If Busy is up when the "Bus → SAR" command is generated the CPU timing will be stopped before T3 time. Absence of clock pulses will "freeze" the CPU in its present state until Busy goes down. The SAR will not be changed until Busy does drop and the clocks start again. Thus, the use of a MS with a slower cycle time than 2.4 microseconds requires that Busy be held up for a correspondingly longer time. The control logic need not change.

CPU cycle 5 in Fig. 3 is the second computation cycle available after MS access and as such may be unnecessary for many instruction executions. The SAR cannot be changed for the next MS cycle until CPU cycle 6. Cycle 5 can be eliminated from the instruction sequences when it is not required, as was cycle 2. The control state entered at T1 time of cycle 5 can command "Bus → SAR." The presence of Busy will stop the CPU before T3 time and prevent the SAR from changing in cycle 5. Busy will be down and SAR will be changed at T3 time of CPU cycle 6. A reduction in MS cycle time from 2.4 to 2.0 microseconds would reduce instruction execution times for those instructions that do not use cycle 5. If cycle 5 is used in an instruction sequence, the faster cycle time would not affect execution time.

USE OF "DELAYED ADVANCE"

A signal Delayed Advance is also shown in Fig. 3. This signal is required to control the commands SDR → Adder and Write. It has been assumed that the Write command can occur for all main stores in the cycle following the SDR load. If the Write cannot occur this soon for some MS, the MS must provide the additional delay if the CPU logic is to remain unchanged. Alternatively, a Write Advance signal could be included along with Busy and Advance in the signals fed back to the CPU from MS.

DESIGN CONSIDERATIONS

The Boolean equation for stopping the CPU clock as a function of Busy and Advance can be determined from examination of Fig. 3. The equation is:

$$\begin{aligned} \text{Stop Clock} = & (\text{SDR} \rightarrow \text{Bus} + \text{Bus} \rightarrow \text{SDR}) \cdot \text{Advance} \cdot T_2 \text{ time} \\ & + (\text{SDR} \rightarrow \text{Adder} + \text{Write}) \cdot \text{Delayed Advance} \cdot T_2 \text{ time} \\ & + (\text{Bus} \rightarrow \text{SAR}) \cdot \text{Busy} \cdot T_2 \text{ time} \end{aligned}$$

Of course when the clock is stopped it must be started again with the proper clock pulse. The above equation and the signals defined in Fig. 3 assume that

decisions to stop and start the clock are made early in T2 time of each CPU cycle. The signals Busy and Advance must be stable at that time but still have considerable latitude concerning the exact times of transition. That is, the signal transitions may typically occur anywhere in the last half of a CPU cycle.

The MS access and cycle times are assumed to be multiples of the CPU cycle time even though the MS-CPU interface is asynchronous. For example, the Advance signal defined in Fig. 3 is based on an 800 nanosecond MS access time. If this access time were shortened to 600 or lengthened to 850 nanoseconds, the definition of Advance would not change. If the access time were lengthened to 1000 nanoseconds the Advance signal would rise 1 CPU later, just as for a 1200 nanosecond access MS. Exactly where the apparent access time changes from 800 to 1200 nanoseconds must be determined for each design from logic delay analysis.

COMPUTER INPUT/OUTPUT DESIGN

Another important advantage of an asynchronous MS-CPU interface is the simple incorporation of a MS cycle stealing Input/Output interface. An I/O sequencer can be designed to use MS just like the CPU instruction sequencer. When either sequencer tries to load the SAR and MS is Busy, that sequencer clock will be stopped. Thus, two sets of clocks are required: one for the CPU instruction sequencer and one for the I/O sequencer. MS can be Busy as a result of a request from either source. It does not matter if the CPU sequencer clock is stopped as a result of a previous CPU-MS request or as a result of I/O using the MS. The equation for stopping the CPU clock remains essentially the same except for added terms required for "tie" requests from the I/O.

CONCLUSIONS

The standard MS-CPU interface described here has been used in both microprogrammed and hardware controlled machines. The interface has also been used to adapt a slow MS unit for computer checkout purposes. The checkout MS is approximately 40 times slower than the MS designed for delivery but permitted checkout to proceed with no CPU logic changes.

Some advantages of an asynchronous MS-CPU interface are:

- Multiple main stores can have different characteristics, thus compensating for remote main store location. (The Busy and Advance signals define the main store characteristics.)
- Main store cycle stealing Input/Output design is facilitated.
- Sequential control logic is simplified.
- Product improvement by using a faster main store is simplified.
- Slower main stores may be substituted, thus, lowering power requirements whenever reduced computer performance is acceptable.

Special Cable Assembly Solves Wiring Density and Flexibility Problems of "Flying Head" Data Systems

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In "flying head" data system applications, where high wiring density, maximum flexibility and extreme reliability over a wide range of specific environmental and mechanical characteristics are required parameters, Cicoil Super-Flex cable assemblies can offer the solution. The applications discussed in this note cover the Control Data Corp. 6638/814 disk file and the Univac FH 432/FH 1782 drum file memory systems.

Both systems utilize a read/write "flying head" assembly, that floats on a thin layer of air over a magnetic oxide surface at extremely high speed. The cable requirement for these flying heads presented a design challenge. In both cases, the design required an unusual cable assembly, consisting of high-strand copper wire encapsulated in a special formulation of silicone rubber. The extremely high flexibility, plus maximum conductor density and wide range environmental characteristics of "Super-Flex" cable, developed and manufactured by the Cicoil Corp., Van Nuys, Calif., proved to be a key factor in the ultimate success of both systems.

DRUM UNIT CABLE ASSEMBLY

The FH series magnetic drum storage units vary from the ultra fast FH 432, with an average access time of 4.3 milli-seconds, to the larger capacity FH 1782, with a 12.5 million alpha-numeric character storage capability at 17 milli-seconds average access.

Binary information is written on and read from the oxide surface of the magnetic drum by flying read/write heads, which are supported by a boundary layer of air that flows around the drum immediately adjacent to its surface, caused by the high speed rotation. In order to provide the rigidity required for paralleled read/write operation and maintain a reasonable cost per channel, many head sizes and shapes and associated interconnections were evaluated.

Since this head is flying on a boundary layer of air, similar in principle to a hydrodynamic air bearing, the minimal mass and maximum freedom to pivot around its pivot bearing are extremely important.

The FH432 and FH1782 use a 54 channel head assembly with channels spaced .0495 inches apart. To achieve a nominal track spacing of .0165 inch, three assemblies are interlaced. The head is attached to a cradle by a pivot bearing. This pivot bearing is a ball and cone on one side of the cradle for locating, while providing movement parallel to rotor axis on the other end for temperature expansion by means of a ball and elongated cone. Fig. 1 represents a 54 channel head with .010 inch wide core pieces and the

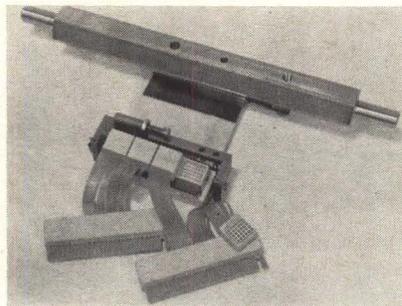


Fig. 1 54 channel head body assembly showing pivot bearing.

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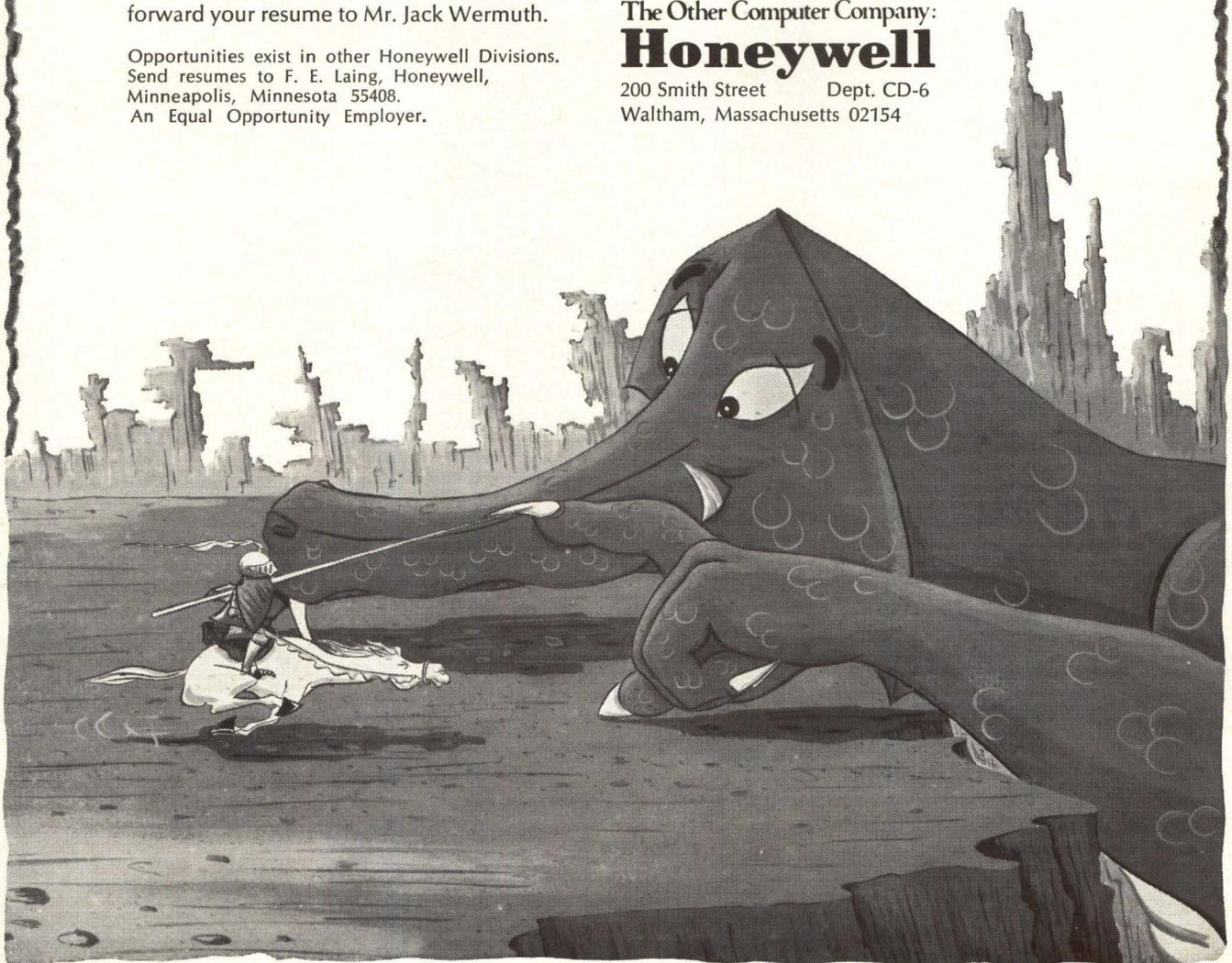
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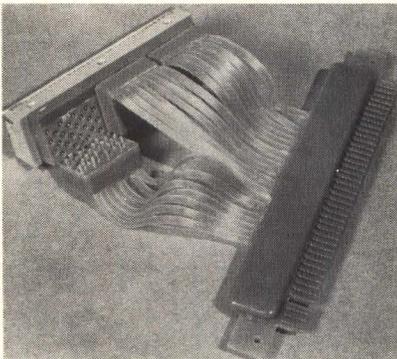


Fig. 2 Univac 33 channel head body with cable assembly slit for maximum flexibility.

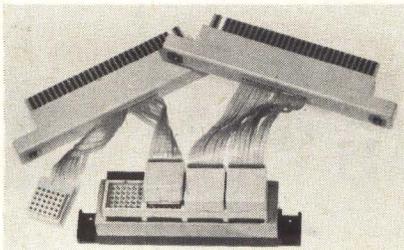


Fig. 3 Univac 54 channel head body showing two cable assemblies with 108 conductors.

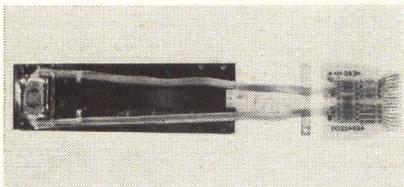


Fig. 4 Control Data flying head assembly with Super-Flex cable exposed.

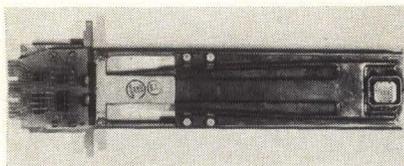


Fig. 5 Control Data flying head assembly showing read/write head and diodes on circuit board.

ball and socket pivot center incorporated. Figs. 2 and 3 show the various types of cables and associated head body connectors as used with 33 and 54 channels.

Conventional wiring was used on a 22 channel head (equivalent to 32 gauge, consisting of 19 twisted strands of 40 gauge). Toleration of this added stiffness in the pivot bearings is acceptable since only 44 conductors are required. On the 33 and 54 channel head, 66 and 108 conductors are required and conventional wiring proved too stiff.

In order to solve the problem of stiffness encountered in the use of conventional wiring, a special Cicoil cable assembly was developed. This assembly consists of an extremely flexible 36 gauge cable made up of 25 strands of 50 gauge oxygen free hard copper wire encapsulated in a special formulation of silicone rubber. The conductors are placed on .030" centers in three separate tapes from a common printed circuit connector to three 24 pin plugs. The individual tapes are slit between every three conductors to provide added flexibility. The result is a nearly friction-free connection between the flying head block and the stationary support, with minimum space and mass allocated to the interface connector.

As state-of-art techniques in read/write transducers advanced, continued mounting of larger numbers of transducers per flying head block has occurred. In the past several years Univac has gone from 22 to 54 transducers per flying head block. Since the present design requires two electrical conductors per transducer, 108 conductors are required to accommodate the 54 transducers. In the future, as more transducers per head assembly are desired, the number of conductors required may further expand. The key design characteristics in space mass and flexibility that make Cicoil "Super-Flex" cable assemblies superior to previous methods, will allow the continued improvement and added capabilities of the FH series magnetic drum units.

DISK FILE CABLE REQUIREMENTS

In the 6638/814 disk files, there are 19 inches of cabling in the dynamic area from the flying head to the fixed connector to the read-write card chassis. The head cable assembly (Figs. 4 & 5) is from the head to a printed circuit diode board. This assembly, as part of the headarm, is dynamically positioned by a hydraulic servo-mechanism with a 6.2 inch stroke, and has a high acceleration force. In addition, the cable at the head must be flexible and allow the head to gimbal to follow the undulations of the rotating disk surface. The cable shown has 16 conductors from the 6-channel head. There are 134 of these assemblies in a 6638 disk file which means 2,144 conductors that must function with utmost reliability. Size was considered and the conductors are on .030 centers. In addition to being flexible the cable cannot change in physical condition over a period of years and must not open or short.

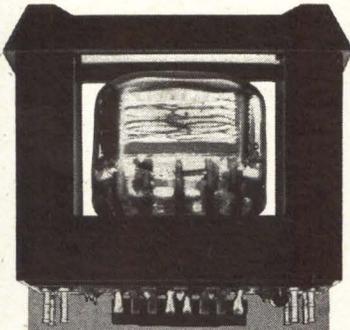
Several cable types were tried such as: laminated printed circuit conductors, vinyl coated conductors, stranded teflon coated conductors and single stranded conductors. All failed because of cracked conductors, stiffening after a period of time, shorting, and damage in handling. The Cicoil silicone encapsulated cable with stranded .001 diameter oxygen free copper conductors was tested and passed all of the requirements. In experimental testing, this cable proved very reliable in production files.

The second part of the cable requirement is a 44 conductor assembly, with 8 assemblies per 6638 disk file, which conducts the input-output data from a common matrix multi-layer board mounted on the head arm positioner to the fixed connector. The cable requirements in this application are more severe than the head cable, since the head arm positioner moves 6.2 inches relative to the fixed connector. The life requirements on the 44 conductor cable is 30,000,000 cycles, which is the calculated moves of the positioner during the life of the file. The positioner moves at speeds of

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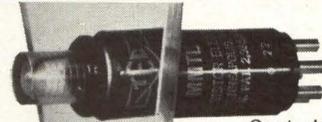
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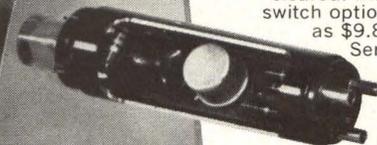
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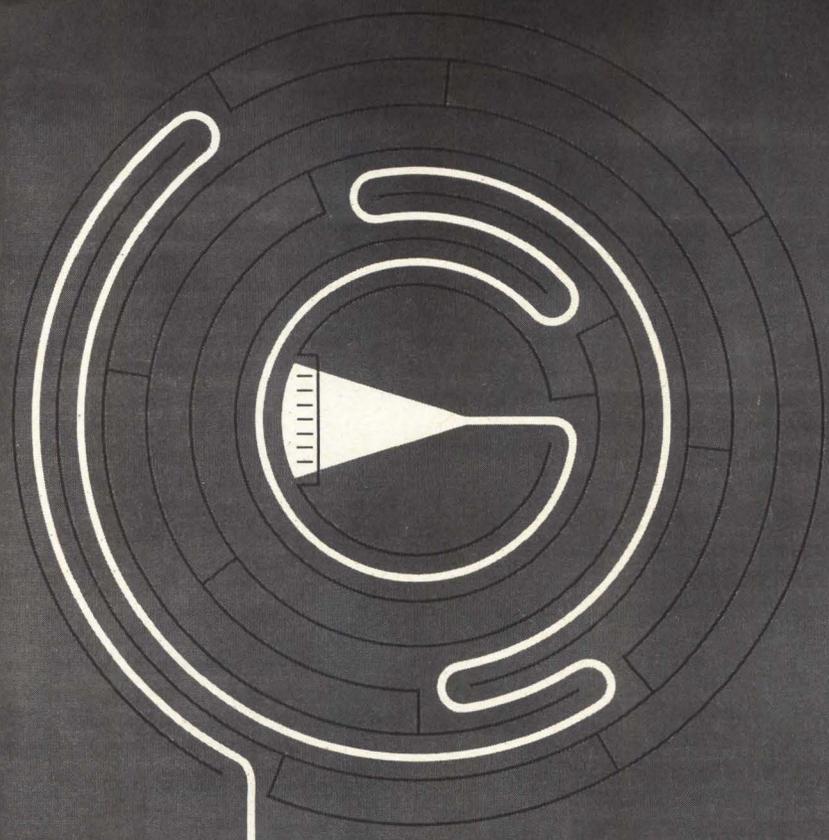
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up to 150 ips with accelerations of 10 G's. A rolling type action was selected, similar to tape movement in a loop box on a tape transport, to minimize movement at any one point of the cable. If a hinged type connection were used the cable would flex at the same point every time the positioner was moved. In the rolling action the flexing is spread over the length of the cable (Fig. 6) with a different part of the cable being flexed depending on the location of the positioner.

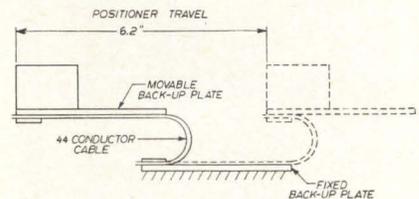


Fig. 6 Diagram showing the travel of the positioner in relation to the fixed back-up plate.

Back-up parts are used to guide the rolling motion. In testing various cables the requirements were no opens, no shorts and actually no change in resistance which could be caused by broken strands or partially broken conductors. To evaluate the cables a 420 cycle per minute tester with a 5 inch stroke was used. Some of the various cable types tested are listed in Table I.

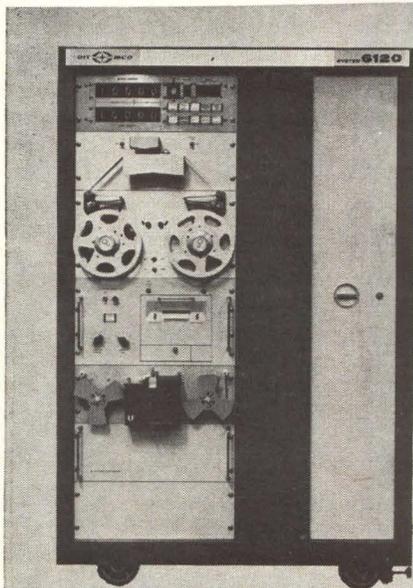
After the initial design of the 44 conductor assembly with the Cicoil conductors was completed, several other features were added. Handling was a problem, so a nylon strap, shorter than the cable length, was added to prevent the cable from being strained, when handled by the connector or pulled. Also three 32 AWG cadmium-chrome conductors were added on each side of the main cable for strain relief and to give better rigidity to the cable in the rolling action.

In conclusion the Cicoil silicone rubber encapsulated conductor cables have helped make the 6638 disk file a reliable recording device. These two examples are typical of the advancing technology in interface and internal wiring systems required in computer memory systems. Greater wire density, added flexibility where needed and better connectors will enable more efficient and effective systems.

← CIRCLE NO. 39 ON INQUIRY CARD
COMPUTER DESIGN/JUNE 1968

TABLE I
CABLE EXPERIMENTAL TEST RESULTS

CABLE TYPE	CYCLES TO FAILURE	REMARKS
Vinyl coated conductor .007 stranded copper	2,000,000	High resistance, wire breakage
Solid steel conductor vinyl coated	490,000	Broken conductor
.002 X .030 Copper on teflon base	20,000	Broken conductor
.002 X .030 Copper on mylar base	53,000	Broken conductor
.002 X .030 Copper on glass base	120,000	Broken conductor
Cicoil "Super-Flex" Cable .001 Dia. X 44 Strands of copper wire		Tested for 70,000,000 cycles with no failure



FASTEST WIRING SYSTEM ANALYZER IN THE WEST AND EAST AND NORTH AND SOUTH.

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LOW COST MASS CORE MEMORY SYSTEM

**FERROXCUBE CORP.
SYSTEMS DIVISION
ENGLEWOOD, COLORADO**

A randomly-addressable, low cost magnetic mass core memory system with a storage capacity of 0.5 megabytes at a cost of 1 to 2 cents per bit is now available from Ferroxcube's Systems Division. The new memory offers the optimal compromise between cost, bit transfer rate and capacity. It has a full cycle time of 2.5 μ s. and is capable of operation in ambients to 105°F. The memory system can be organized in word capacities of from 9 to 144 bits (in multiples of 9) per 524-K byte module. Any number of modules can be connected for series or parallel operation to build systems of almost infinite storage capacities. A total of 4.7 million cores are used in the unique 2½ D selection organization, which incorporates an extra wire for sensing the interrogated bits. The total package with all electronics and power supplies measures 72" x 25" x 28".

SYSTEM DESCRIPTION

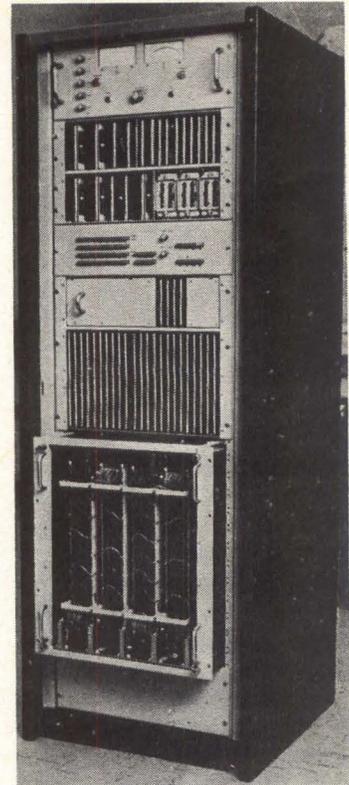
The standard system uses 2½ D selection organization, because of its many inherent advantages such as low core-stringing costs, high speed, negligible heat dissipation within the core stack. Separate sensing wires are used, enabling sectoring of the stack into reasonable small planes that can be efficiently produced in quantity. It is designed for maximum utility having five operation modes: Read, Write, Read-Restore, Read-Modify-Write and Clear-Write with cycle times from 0.9 to 2.5 μ secs, and without restriction on address sequence, or the number of times an address may be selected sequentially.

The interface electronics allow format reorganization to obtain word storage up to 144 bits (16 bytes) per word, increasing the memory transfer rate from 0.5 megabytes per second to 3.2 megabytes per second. The new interconnecting technique employed in the system allows two or more systems to be combined to obtain even larger storage capacities. It also enables very compact stack construction (31" high x 15" wide x 20" deep) including associated electronics and permits removal and replacement of stack sections in less than a half hour, without special skills or tools. The selection diodes used are not mounted on the stack, but are on separate printed circuit card plugged into rear connectors for easy access and maintenance.

The effects of variation in signal delay and attenuation according to address location are compensated by automatic electronic control of strobing time and sense amplifier threshold level, assuring exceptionally reliable, highly uniform performance of the system; the technique employed radically reduces the transformer complement ordinarily required, with a significant reduction in both size and cost of the installation.

MEMORY CORE STACK

The n^{th} bits of all words are arrayed schematically in a rectangle of 256 bit lines by 2048 word lines. Nine rectangles make up the complete matrix of 2304 bit x 2048 word lines. Since a matrix of this size with 30 mil cores at 30 mil centers would be unwieldy, it has been divided into 36 sub-matrices.



The nine sub-matrices in each column are arranged to make four sub-stacks, each containing 130,000 words of nine bits each. The word lines split into nine sections by the division into sub-matrices, can be easily reconnected by dip-soldering. The cards carrying the word line selection diodes, are located by sockets mounted on each sub-stack. Conventional wiring is used between the socket pins and the word line terminals on the sub-stack.

Reconnecting the bit lines separated by the sub-division is more complex. Both ends of each bit line in each sub-matrix are connected to conductors printed on polyimide foils. The correlated bit lines of corresponding matrices in two adjacent sub-stacks can be interconnected by simply pressing the foils together.

The two outermost sub-stacks are connected by pressing their associated foils against glass epoxy strips, on which are printed the same patterns of conductors as on the polyimide foils. These conductors are then joined by conventional wiring to the pins of the sockets mounted on the main stack frame, which locate the cards carrying the bit line selection diodes. The frame also carries the clamping devices for

pressing the polyimide foils together, and the rails along which the sub-stacks slide into position. Typical drive conditions for the cores used in this memory are: Full current — 700 mA (at 25°C); Rise time — 0.1 μ s and Pulse width 0.4 μ s. Under these conditions, the typical response values are: rV_1 — 53 mV; wV_z — 6 mV (disturb ratio = 0.5); Peaking time — 0.2 μ s and Switching time — 0.4 μ s.

MECHANICAL CONFIGURATION

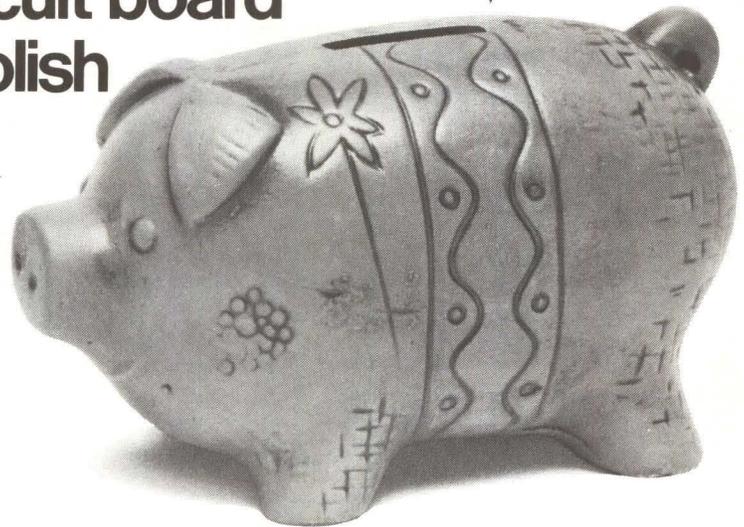
The various circuit components are mounted on double-sided, epoxy-glass printed circuit cards. The cards carrying the principal memory control electronics such as the selection and drive switches, timing circuits and read amplifiers, measure 12½ x 10 inches. The cable amplifiers and terminating resistors are mounted on 12½ x 5 inch cards. The cards slide into compartments that can be mounted in a standard 19 inch rack. The compartment housing the cable amplifier and terminating resistor cards also contains the cable connectors.

In order to take full advantage of the low heat dissipation within the core stack, the container housing the stack is positioned at the base of the cabinet. The dissipation within the stack container is only 4.5 W in a volume of 84 litres (22 gals.).

The compartments housing the memory electronics are located immediately above the stack container. The power supplies are packaged in two compartments which occupy the upper part of the cabinet. Another unit housing transformers and certain control circuits is located in an adjacent position. Mounting the various sub-assemblies in this manner allows the temperature sensitive units to be positioned below those which generate the most heat, thereby eliminating the need for forced cooling. Access to the printed circuit cards is via the front door of the cabinet, an exception being the selection diode cards which are accessible at the rear of the cabinet.

For additional information circle No. 199 on the Inquiry Card.

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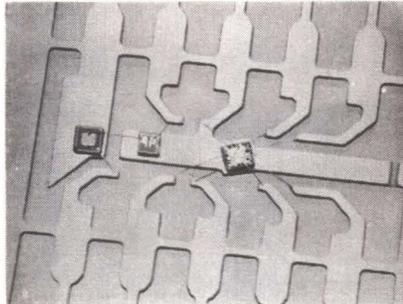
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NEW PRODUCTS

PLASTIC DIP HYBRID CIRCUIT

Using the transfer mold process of semiconductor packaging, Fairchild Semiconductor claims to have introduced the industry's first hybrid circuit in a plastic Dual In-Line (DIP) package, a high current, high voltage driver that offers hybrid capabilities at prices previously available only in discrete functional counterparts. The transfer mold process lends itself to high volume and low cost production. Called the SH2002-P, the new device is a plas-



tic 10-lead version of Fairchild's hybrid SH2002, now being widely used for

lamp, relay and line driving applications. Both are DT μ L devices with a current sinking performance of 150 mA and a sustaining voltage capacity of 40 volts. For industrial users, the device is suitable for tape read-out, go-no-go test equipment, solenoid drivers in telephone systems, and various display systems such as lamp and relay driving with latching capabilities. In commercial computers, it can function as a memory or clock driver and as a read-out component in peripheral equipment.

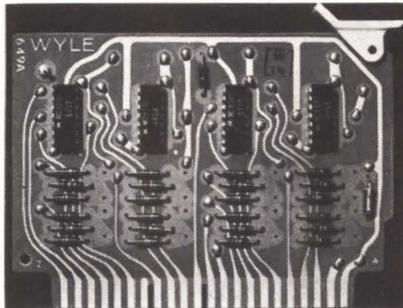
Fairchild Semiconductor, Mountainview, Cal.

Circle No. 200 on Inquiry Card

IC INPUT LEVEL CONVERTER

An input level converter incorporating eight independent circuits for converting any signal to DTL logic levels from positive or negative voltages of up to 48 volts is available in Wyle Laboratories' line of Series M integrated circuit logic modules.

Designated as the MIS-8, the input level converter contains eight level shifting or level converting amplifiers, each amplifier consisting of an input resistor network, an integrated circuit (RTL) dual-input NOR gate, and an integrated circuit (DTL) inverter.



The input resistor network contains three "universal" resistance values. By connecting the appropriate resistor to the signal to be converted

and connecting the remaining resistor or resistors to a bias voltage or to ground, the level converter can accommodate virtually all of the commonly used levels.

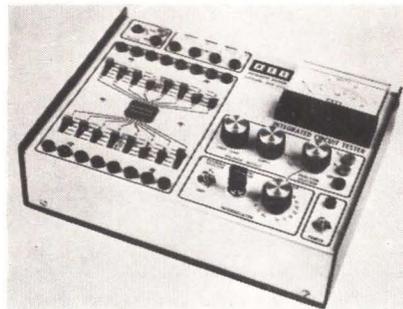
One input of all eight NOR gates is connected to a common DTL inverter, to allow the card's outputs to be gated, or strobed, if desired. The DTL inverter on the output of each level shifter is designed to insure output compatibility with DTL levels. Systems Division, Wyle Laboratories, El Segundo, California.

Circle No. 201 on Inquiry Card

LAB IC TESTER

Integrated circuit tester, model 101 from AEI Instrument Division of Andresen Enterprises, Inc., is said to fill a long-felt need for a low-cost laboratory unit for fast, reliable testing of individual IC's.

Priced at \$275, the tester features two independent power supplies for Vcc and logic level "1". The two supplies are so designed that logic level "1" can be no higher than 0.5 volts below Vcc. Range of the Vcc supply is 1 to 15.5 volts and for logic level "1",



0.5 to 15 volts. Both supplies are short-term short circuit proof.

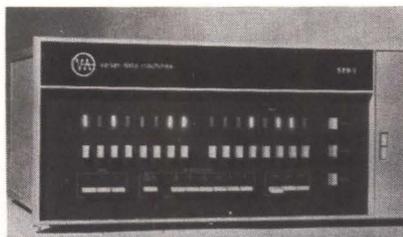
A 4 x 16 matrix permits easy programming of the test. Through the matrix any one pin of the IC can be programmed for either Vcc, logic level "1", ground, or no connection.

Following tests and measurements can be made: Icc all inputs low, Icc all inputs high, shorts between inputs, input loads, output "0" level, output "O" level under load, output "1" level, output "1" level under load, minimum logic level "1", minimum Vcc. AEI Instrument Co., Div. of Andresen Enterprises, Inc., Cleveland, Ohio.

Circle No. 232 on Inquiry Card

DUAL PROCESSING COMPUTER

A systems-oriented computer called the 520/i recently announced by Varian Data Machines brings some useful computing innovations to the low-priced computer field. Designed to function as a dual processor, the new computer is equipped with two complete sets of "hardware" operating registers. It has 2 separate 32-bit accumulators, 2 separate 16-bit hardware index registers, 2 separate 16-bit program counters, 2 one-bit overflow registers, 2 two-bit registers whose con-

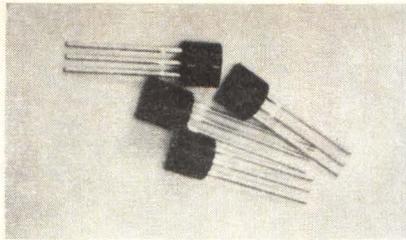


tents determine word length.

Its greatest versatility is said to be its multi-precision capability to handle 1, 2, 3, or 4 byte operands. Special in-

structions establish word length or precision independently for each set of registers, and a program can change its own precision at any time. In this way it can process within the same program data with word lengths of 8, 16, 24, or 32 bits. Eleven interrupts in four priority levels are included in the basic price of \$7,500. Available software includes an assembler, utility program and subroutines, and a complete set of diagnostics. Varian Data Machines, Newport Beach, Cal.

Circle No. 203 on Inquiry Card



PLASTIC DRIVER TRANSISTORS FOR NIXIES®

Two new plastic transistors called 2N4409 and 2N4410, with the high breakdown voltage capabilities essential to neon display tube drivers, are priced to fit the requirements of the small quantity user.

Since a display tube driver in the "off" state must withstand approximately one-half of the tube firing voltage, the minimum breakdown voltage specification, BV_{CEX} , is set at 80 and 120 volts for the 2N4409 and 2N4410, respectively.

In addition, the low leakage current basic to tube driver operation is insured by an I_{CBO} for both devices of 1.0 μA max. at 100°C. And their performance is further aided by a typical h_{FE} figure for each device of 150 at $I_C = 1.0$ mA.

Both transistors are readily available from factory and distributor stocks. In 1000 quantities the price of the 2N4409 is \$0.34 each while the 2N4410 sells for \$0.48 each. Motorola Semiconductor Products Inc., Phoenix, Ariz.

Circle No. 204 on Inquiry Card

FLIP-CHIP TRANSISTORS

Three new series of NPN silicon planar epitaxial transistors have been added to the flip-chip line of Hughes Aircraft Company's Newport Beach division.

GAT 1200, GAT 1202 and GAT 1203 are designed for switching applications, and feature F_T to 400 MHz and gain to 300. Glass ambient construction affords hermeticity and 100 mW rating. Prices begin at \$.62 for quantities of 100 and up.

GAT 1215 and GAT 1216, designed for low power amplifier applications, have F_T to 300 MHz, voltage ratings to 70 volts and gain to 200. Power rating is 100 mW. Prices for 100 and up begin at \$.80.

GAT 1222, GAT 1223 and GAT 1226, for general purpose power applications have current gains to 300 at 150 mA and 40 minimum at 500 mA, and power rating of 250 mW. Prices for 100 and up begin at \$.59. Hughes Aircraft Co., Newport Beach, Cal.

Circle No. 209 on Inquiry Card

Introducing...



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margins at elevated temperatures. In addition, the new memory provides easy interfacing and great I/O flexibility, with input levels of $\pm 0.5V$ and 2.5V to 24V, output of any voltage from 1V to 15V, and drive current up to 80ma.

Front panel display is provided for all registers, and it comes with timing and control flags, test points, and optional self-test for simplified system checkout. Matching power supplies are available.

VersaSTORE III is the third, most advanced, and newest of our highly successful VersaSTORE designs. We've prepared an equally new brochure full of vital information about our new memory—we'll be glad to send it to you, just call or write.



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CIRCLE NO. 40 ON INQUIRY CARD

NEW PRODUCTS

COMMUNICATIONS BUFFER AND RETRIEVAL SYSTEM

A buffer storage system has been designed for use, with a minimum of special interface circuitry, as an economical sub-system in both computer and communications buffering applications.

The system utilizes a magnetostrictive delay line as its memory element and is said to achieve low cost per bit, low power consumption, noiseless operation, absence of moving parts, and simplicity of interface circuitry. The delay line operates at one megahertz in a recirculating mode and gives four thousand bits of storage, sequentially. Storage capacities up to 100,000 bits are available.

To meet the requirements of most computer applications, the Model 5001 system operates by Read-Write commands for information storage or read-out. The Model 5002 system operates from direct commands from a teletype

machine functioning in either the send or receive mode.

Special features of the system include provisions for external clearing of the buffer, indication of memory fullness, and input inhibition when the buffer is full. Laboratory For Electronics, Inc., Commercial Products Operation, Waltham, Mass. Circle No. 222 on Inquiry Card

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TIME-SHARED SYSTEM

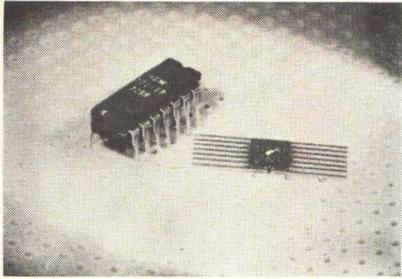
A new 16-terminal time-shared system reduces user terminal costs considerably below that of conventional commercial time-sharing services. With only light use — 340 hours per month, equivalent to 4 terminals used 4 hours per day — the terminal cost is less than \$7 per hour (exclusive of teleprinter and data communications charges). With all 16 terminals in use, the cost goes down to less than \$7 per terminal per day. The system, with one control teleprinter, sells for \$89,500. It can be located at the user's facility, and be available 24 hours a day, every day of the week.

The HP 2000A Time-Sharing System achieves this economy by restricting itself to one programming language — Conversational BASIC — and by using a relatively small computer. This computer, HP Model 2116, uses 16K of core memory, augmented by a disc memory with an additional 348K words. 500 to 1000 average sized programs may be stored on the disc, and for larger requirements, disc storage can be expanded. The computer has a 16-bit word length and a memory cycle time of 1.6 microseconds.

User terminals are standard ASR-33 or ASR-35 teleprinters (with Data-phone interface) available from HP, Teletype Corporation, or local telephone companies. Connection between system and user terminals is either direct-wired or via telephone lines. Conventional telephone Data Sets or portable acoustic couplers provide connection. Up to 16 teleprinters can be serviced simultaneously. The ability to accommodate a mix of direct lines and phone lines represents another innovation in time-share systems. Hewlett-Packard, Palo Alto, Cal.

Circle No. 220 on Inquiry Card

CIRCLE NO. 42 ON INQUIRY CARD



IC'S PERFORM EXPANDED FUNCTIONS

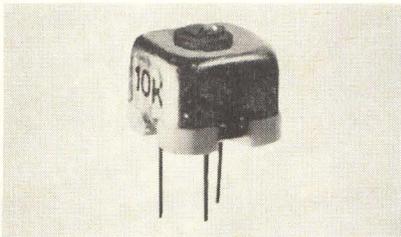
Ten new integrated circuits are now available which perform expanded functions that previously could be attained only by the improved interconnection of two or more units of the DTL 930 series.

The new devices consist of: a 10-input complementary gate (SW770 & SW771), a triple R-S flip-flop (SW772 & SW773), a triple 3-input AND gate (SW774 & SW775), a dual AND/OR gate (SW776 & SW777), and a dual 4-input complementary gate (SW778 & SW779). Even-numbered units are with 6K pull-up resistors for lower power consumption, and odd-numbered units are with 2K resistors for faster rise times.

Since each of these units replaces more than a single unit in the basic 930 series, the new 770 series permits the designer to cut down in improvisation, IC package count, and external wiring.

All units are available in standard, 14-lead ceramic flat-packs or dual in-line packages. Single unit prices for the industrial temperature range (0°C. to +75°C.) start at \$2.25; and unit prices for the military range (-55°C. to +125°C.) start at \$5.36. Stewart-Warner Microcircuits, Inc., Sunnyvale, Cal.

Circle No. 205 on Inquiry Card



CERMET TRIMMER

CTS Series 340, a new 1/4" x 1/4" x 0.220" single turn rotary cermet trimmer, has top adjustment and resistance range of 50 ohms to 500K ohms with ± 20% standard resistance tolerance. Power rating is 3/4 watt @ 25°C or 1/2 watt @ 85°C. Other features include positive stops, nickel plated brass housing and enclosed construction. CTS of Berne, Berne, Ind.

Circle No. 235 on Inquiry Card

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20 years of leading engineering experience have made LFE the name to remember in delay lines and memory systems. Today, magnetostrictive and glass, as well as quartz delay lines, are readily available and can be supplied with associates electronics. Also, memory modules are designed for any number of bits. Analog and digital information processing systems are also a prime capability.

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CIRCLE NO. 41 ON INQUIRY CARD

NEW PRODUCTS

IC LOGIC MODULES

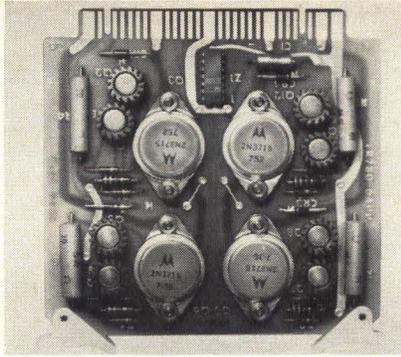
Honeywell's Computer Control Division has announced 16 integrated circuit logic modules including a new high-speed 10 MHz series, which increase the division's total line to more than 75 modules.

The new 10 MHz series contains NAND cards, gated flip-flops, transfer gates, master clock and multivibrator clock modules. Toggle and shift frequency of the flip flops is actually 25 MHz, but is conservatively specified as having an operating frequency of 10 MHz.

Added to the five MHz module series are a fast carry up/down counter, universal logic card, new transfer gate, fast recovery delay multivibrator, analog comparator and two Nixie driver modules.

The division also introduced an analog comparator and three "blank" circuit cards for mounting dual-in-line and flat pack devices. Honeywell Computer Control Division, Framingham, Mass.

Circle No. 244 on Inquiry Card



HIGH CURRENT DRIVERS

Cambridge Thermionic Corporation announces the addition of a new high current driver to its growing family of logic assemblies. Designated part number 780-6404, this assembly has four high current drivers on one card. Each driver circuit can withstand up to 5 amperes of current and 40 volts. The new logic card may be used to drive components such as stepping motors, solenoids, or in many comparable applications requiring high current and reasonably high voltages. Cambridge Thermionic Corporation, Cambridge, Mass.

Circle No. 243 on Inquiry Card

SILICON RECTIFIER DIODES

Amperex Electronic Corporation has now extended the capability of its BYX controlled-avalanche silicon rectifier diodes to include fast recovery characteristics. A new series of power rectifying diodes, designated BYX-30, is now available for use in fast switching applications such as high frequency power supplies, thyristor inverters, and multi-phase power rectification circuits.

With working voltages from 200 to 600V, the series offers switching speeds up to 200 amperes per microsecond at frequencies as high as 50,000 Hz with minimum power loss due to reverse recovery.

The advantages of working with power rectifying devices that have specified avalanche breakdown characteristics are that the designer can optimize or eliminate transient-suppression networks and that he can employ smaller safety factors than would be required with less completely specified diodes. Reproducible voltage-division characteristics of the BYX family of devices allows them to be used in series in applications not previously considered feasible for power rectification devices. Amperex Electronic Corporation, Semiconductor and Receiving Tube Division, Slatersville, R.I.

Circle No. 208 on Inquiry Card



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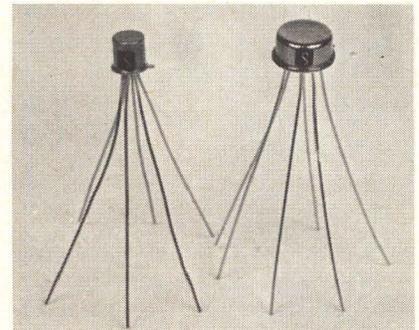
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CIRCLE NO. 37 ON INQUIRY CARD



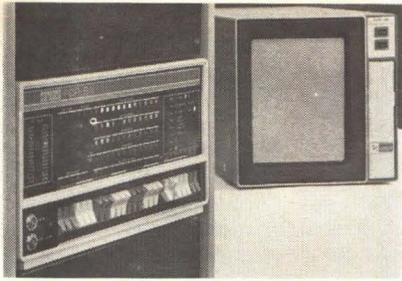
SMALL SIGNAL PNP AND NPN DIFFERENTIAL AMPLIFIERS

Low-cost small signal line of PNP and NPN differential amplifier transistors, hermetically sealed in TO-78 and TO-71 cases, will track over a wide temperature range with temperature co-efficients as low as $3\mu\text{V}/^\circ\text{C}$.

Typical characteristics of the units include matched gains to within 3%, voltages up to 120V, leakages less than 20pA and low level gains typically 100.

Some typical circuit applications of the devices include series and switching regulators, low noise amplifiers, complementary differential amplifiers, dc amplifiers, series shunt choppers and other circuits where tight tolerance feed-back is essential. Solitron Devices, Inc., Riviera Beach, Fla.

Circle No. 207 on Inquiry Card

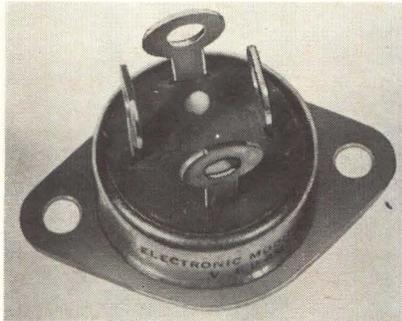


DISPLAY-SYSTEM CONTROLLER

An inexpensive control unit for computer driven storage tube display systems, recently announced, allows rapid conversion of digital computer data to graphic and tabular form and can be used with most storage scopes.

The new VD-8/1, priced at \$3,500, requires no display refreshment and operates at comparatively fast output rates. It permits display files and file-linking subroutines to be stored in highly compact algorithms and generated as required, thus reducing the amount of core storage needed to generate a given display. Digital Equipment Corp., Maynard, Mass.

Circle No. 217 on Inquiry Card



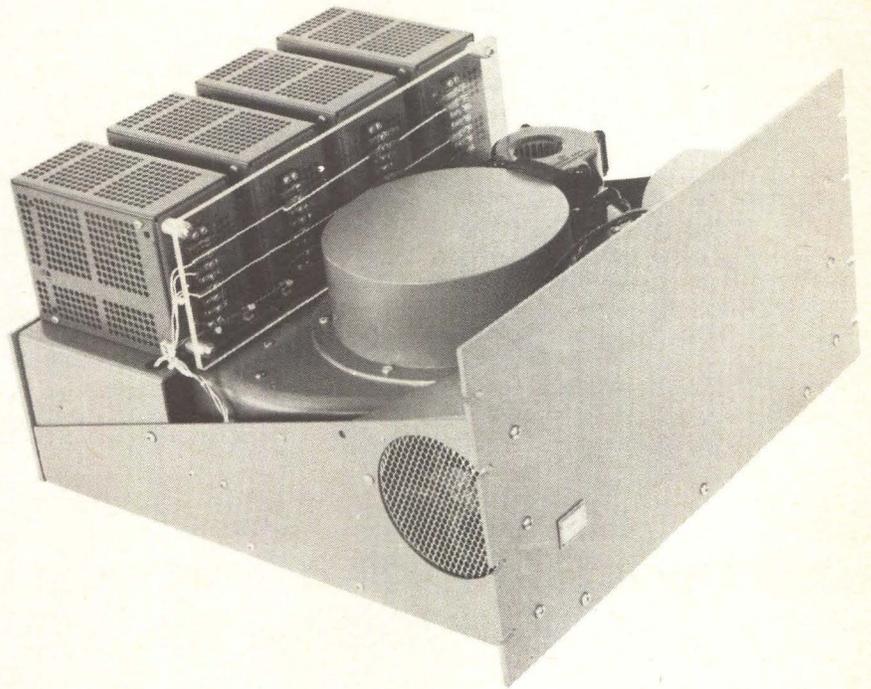
10 AMP THICK FILM BRIDGE RECTIFIER

Utilizing hybrid fabrication techniques and a unique concept in packaging, a new thick film 10 Amp integrated bridge rectifier offers a new circuit component for the design engineer at an attractive price.

Packaging combines the mounting versatility of a TO-3 standard package, with the advantages of a plastic encapsulant. Applications for the new thick film rectifier include power supplies, AC to DC converters and motor controls. Electrical features include: 10A average DC output current at $T_C = 65^\circ\text{C}$.; 100A peak one-cycle surge current $T_A = 25^\circ\text{C}$.; 25A peak surge current, 1 sec at 60 Hz and $T_A = 25^\circ\text{C}$.; Junction operating and storage temperature range T_J and $T_{STG} = -65^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{RM} = 100$ to 600 volts. The Bendix Corporation, Bendix Semiconductor Division, Holmdel, New Jersey.

Circle No. 206 on Inquiry Card

more display channels per dollar



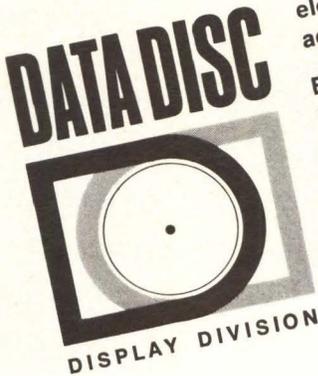
Data Disc's new digital/video disc memory opens a whole new world of display possibilities. Think about how you can use up to 72 completely independent tracks — each with its own head and read/write/clock electronics — to store up to 100,000 bits per track — accessible at a 3 megabit/second rate.

Because the data is clocked in and out, using TTL logic, track-combining techniques can provide up to 7.2-megabit capacity at up to 216 megabits/second. Write on any track without disturbing the displays being read from adjacent tracks.

Applications include X-Y CRT and TV-monitor refreshment, digital-television storage, and high-speed parallel buffer memory.

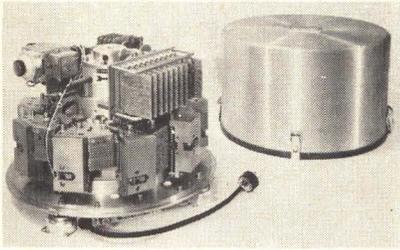
Price for the FPD? \$4,870 plus \$300 per track. Delivery? 30 days! Application and interface details? Call Bill Stevens at (415) 326-7602 or write:

Data Disc, Inc., Display Division,
1275 California Ave., Palo Alto, Calif. 94304



CIRCLE NO. 26 ON INQUIRY CARD

NEW PRODUCTS



SMALL, HIGH-DENSITY DRUM MEMORY

Vermont Research Corporation's small drum memory, Model 1004S, is now available in an optional version with nearly double the storage capacity.

Identical in size to the original Model 1004S, the new high-density version packs a total capacity of 4,224,000 bits into a dust-tight enclosure measuring 17½" in diameter by 12⅝" high. It includes, within the drum case, all electronics required for head selection, writing and reading data. The total package weighs 75 pounds.

Other basic specifications of the new high-density 1004S option (with corresponding figures for the standard version in parentheses) are: bits per inch, 1000 (650); bits per track, 33,000 (20,500); data tracks, 128 (128); operating frequency, 1.8 MHz (1.2 MHz).

Availability of the 1004S option means rotating memory users can now gain drum performance attributes (such as average access of 8.7 msec) along with high capacity and small size at a price competitive with that of small disks and other rotating memory devices. Vermont Research Corp., N. Springfield, Vt.

Circle No. 210 on Inquiry Card

CORE MEMORY SYSTEM WITH FIELD EXPANDABILITY

An economical, compact, modular, random access core memory system, recently introduced, offers storage capacity up to 4,096 words per module, 6 to 26 bits, with word expandability to 32,768 by adding on additional modules. Expansion beyond 26 bits is possible by driving modules in parallel. Either word or bit field expansion requires no special interface circuitry.

The new modular memory will operate at speeds of 1.75 microseconds full cycle and 1.0 microsecond half cycle; access time is 750 nanoseconds. Integrated circuits and modular printed board design make possible improved reliability and package density. All necessary timing, control, address/data register and flag signals are provided. The special "Memory Select" control input, in conjunction with unique expansion techniques, allows for easy decoding of memory blocks.

The Model 470 can be supplied with or without power supply, and requires no external cooling to operate over the temperature range of 0°C. to 50°C. Interface circuits are designed to be compatible with a wide range of logic levels typically encountered by small to medium sized computer central memories, interface buffers or control memory systems. Fabri-Tek Incorporated, Edina, Minn.

Circle No. 224 on Inquiry Card



TAPE TRANSPORT

Midwestern Instruments, Inc. has announced a new tape transport, known as the Midwestern 4840, that will be a plug to plug replacement for the IBM 2420 tape drive recently introduced by IBM.

The input/output and power connectors will be identical. To aid in smooth interchange, both the operator panel layout and nomenclature also will be identical to the 2420.

Tape speed of the replacement transport is listed at 200 inches per second, with 2 millisecond start time and stop time. Both tape and reels are IBM compatible, as is tape format (8 data bits with 1 parity bit) and accepts a density of 1,600 bits per inch, phase encoded.

Any Midwestern 4800 Series unit can be field converted to 200 ips. Midwestern Instruments, Inc., Tulsa, Okla.

Circle No. 215 on Inquiry Card

amnesia (am nē'zhə or am nē'zhīə)
loss of memory due to a 10% voltage swing. *n.*

Raytheon Computer's 300 memory keeps right on reading and writing data reliably even when operating voltage and drive currents vary as much as $\pm 10\%$. And over a full temperature range of 0°C to 50°C. The 300 is a 2½D 900 nanosecond core memory for general data systems use. ■ If your definition of memory is: high performance, high reliability, high capacity, and delivery in 60-90 days, see us. Raytheon Computer, 2700 So. Fairview St., Santa Ana, Calif. 92704. (714) 546-7160.

RAYTHEON

CIRCLE NO. 44 ON INQUIRY CARD

REMOVABLE DISC STORAGE DRIVE

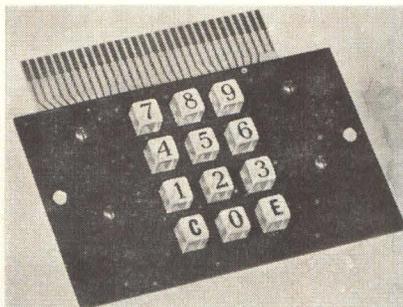
The General Electric Company has introduced a removable disc storage drive unit featuring advanced integrated circuitry and improved data protection features.

The new unit, a removable media memory system, is plug and data system compatible with similar disc drives being used on GE and IBM computer systems and can be used as a replacement for existing devices without changes in software or in systems configuration. The drive uses a standard six-disc pack, such as the IBM 1316 or equivalent.

A new circuit design eliminates the need for potentiometers and selected value components. As a result, no electrical adjustments are required to install or maintain the unit.

The single spindle disc drive will have a capacity of 7.68 million 6-bit characters or 7.25 8 bit bytes (60 million bits, unformatted).

The unit provides an average point-to-point access time of 75 milliseconds. The drive will be priced to the system user at \$25,510 for purchase or \$590 per month for lease. It will also be available to other system suppliers on an OEM basis. Information Devices Dept., G.E. Co., Oklahoma City, Okla. Circle No. 218 on Inquiry Card

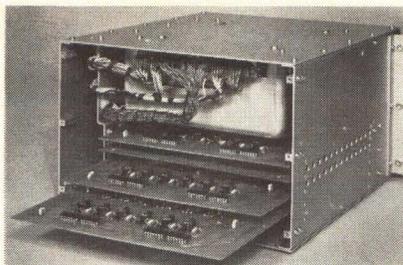


PRE-ASSEMBLED KEYBOARD

12-Key data entry keyboard with momentary contact is supplied assembled to a printed circuit board for mating connector or for hardwiring to external circuitry. It uses $\frac{3}{8}$ " square keys on $\frac{5}{8}$ " centers in adding machine or telephone configuration. Standard colors are black on white. Important characteristics of the keyboard are: light touch (5 ounces contact pressure), short throw (.1 inches), extremely low profile (only $3'' \times 5'' \times 1''$ deep), and light weight (5 ounces assembled).

Life rating is 5 million cycles at 100 mil., 6v. dc. for computer data entry applications. Price \$1.75 per button in quantity. Nutronics, Paramus, N.J.

Circle No. 245 on Inquiry Card



COMMERCIAL CORE MEMORY WITH MILITARY FEATURES

A compact, 8K x 40 random access core memory with a 2 microsecond full cycle speed and many rugged features of military systems has been designed for commercial applications.

Featuring an 800 nanosecond access time, the Series 500 can perform over a wider temperature range and is less sensitive to shock and vibration than most commercial memories. Only $19'' \times 11'' \times 5\frac{1}{4}''$, the memory contains three circuit module types. All modules and the memory stack are plug-in units that can be replaced quickly. The system features an optional self test which provides the full test capabilities of zeros and ones, worst case, and worst case complement. Test controls, pattern generator, data and ad-

dress indicators are contained in the plug-in self test module.

Input signal levels range from +2.6 to +5V with a 160 microamp minimum current for logical "1," and 0 to +0.8V with a 6.4 milliamp current for logical "0." Output signal levels range from +4V, sourcing 1.0 milliamp maximum, and 0 to +0.4V sinking 16 milliamp maximum. Memory Product Department, Sanders Associates, Inc., Nashua, N. H.

Circle No. 221 on Inquiry Card

DATA INTERFACE

New low cost data interface accepts parallel BCD data from as many as 24 input devices of up to seven digits each. The output drives printers, teletype, paper tape, magnetic tape and card punches. Optional buffer storage allows data accumulation to resume during readout.

A variety of input and output codes can be accommodated. No modification of either input or output devices is required. Special identification characters may be inserted between channels. Prices start at \$985. Digital Automation Co., Inc., Pennington, N.J.

Circle No. 225 on Inquiry Card

ESC DELAY LINES

breakthrough

in high density packaging

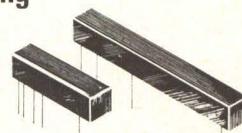


Only $\frac{1}{4}''$ Wide

Model 54-67



Model 13A27



SM Series

An example of ESC's sophisticated design capability is our Model 54-67 (size: $3'' \times \frac{1}{4}'' \times 1\frac{1}{2}''$ H). Used in an airborne application, this rugged flat pack unit with an overall thickness of only $\frac{1}{4}''$ is an excellent example of high density packaging. It has a time delay of 29 usec. with a tap at 11 usec. The rise time is 1.8 usec. maximum with an impedance of 400 ohms and an attenuation of 2 db maximum. It meets the requirements of MIL-D-23859A. The delay line which this unit replaced occupied over three times the volume as the 54-67.

Our Model 13A27 (Size: $.490'' \times .490'' \times .370''$ H) is transfer molded and illustrates a low cost, high production run unit. Designed for printed circuit board use in a computer application, the 13A27 has become one of a series of "custom standards" to a valued ESC customer. It has a time delay of 7 nsec. with taps at 4, 2 and 1 nsec.

The SM series of subminiature nanosecond delay lines provides a high figure of merit in a small volume without compromising reliability. Standard items range from 10 to 1,200 nsec. at impedance levels of 100, 200 and 500 ohms. Available off-the-shelf in two standard sizes: $1 \times 0.32 \times 0.32''$ and $2 \times 0.32 \times 0.32''$, both with $2\frac{1}{2}''$ leads. Conforms to MIL-D-23859A.

Write for complete catalog.



ESC ELECTRONICS CORPORATION

a subsidiary of Simmonds Precision

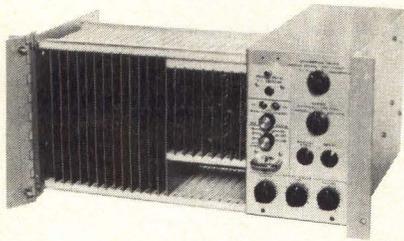
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World's Leading Producer of Delay Lines

CIRCLE NO. 45 ON INQUIRY CARD

Need to sample low-level transducers?

cut your per-channel cost with IEC's new MX 500 Series Low Level Analog Multiplexer.



The MX 500 benefits both designers and users of Data Acquisition Systems:

- Eliminates data amplifiers in each channel
- Reduces system costs sharply
- Simplifies system interface
- Reduces system size, power, and cooling
- Increases system reliability
- Simplifies system checkout and operation
- Reduces system maintenance and spares

Outstanding features include:

- ± 5 mv to ± 500 mv full scale inputs (± 10 v full scale output)
- Up to 50 kHz sample rate
- Easily expandable up to 1000 differential, guarded channels
- 120 db common mode rejection
- Sequential or random address channel selection
- Automatic and programmable gain selection
- Overload protected
- Solid state—FET switches—IC logic
- Available with or without AD converter

The new MX 500 interfaces easily with any Data Acquisition System. Need more information on how you can use the MX 500 in your system? Simply call or write, today.



IEC

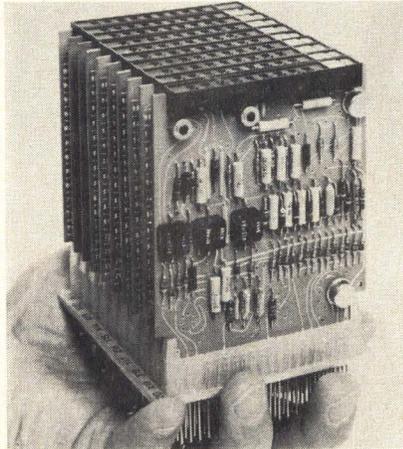
INTERSTATE ELECTRONICS CORPORATION

Subsidiary of "AUTOMATIC" SPRINKLER CORPORATION OF AMERICA

707 E. Vermont Ave., P.O. Box 3117
Anaheim, California 92803 (714) 772-2811

CIRCLE NO. 46 ON INQUIRY CARD

NEW PRODUCTS



IC DATA ACQUISITION SYSTEM

Raytheon Company has recently introduced their 12-bit Miniverter^(TM) Data Acquisition System which does the same job as the company's Multi-verter[®] system yet sells for about $\frac{1}{3}$ as much.

Priced at \$1,950, the new system includes a 16-channel multiplexer, a high performance sample and hold amplifier, a 12-bit analog-to-digital converter plus power supply and control logic. The unit consists of nine integrated circuit modules installed on a connector block assembly, wired, tested and ready to plug into a company or customer supplied chassis.

The basic 16-channel system can easily be expanded. A typical expanded unit in a standard $5\frac{1}{4}$ " by 19" chassis could contain 256 multiplex channels, the sample and hold and a/d conversion functions and 85 additional IC modules for logic and control.

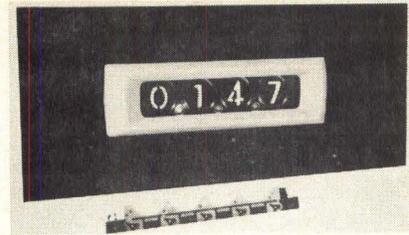
The 12-bit Miniverter operates at a 35 KHz throughput rate with overall accuracy of 0.05%. Raytheon Computer, Santa Ana, Cal.

Circle No. 202 on Inquiry Card

CORE-MEMORY SYSTEM

Datacraft Corporation has announced the beginning of full scale production of their Model DC-32 magnetic core memory, a medium speed 3D system with 4096 and 8192 word basic modules available from 4 to 26 bits in 2 bit increments. Full cycle time of typical 4096 x 8 unit is 1.5 microseconds and will vary up to 40% in larger configurations. Access time is 600 nanoseconds. A full line of options is available and delivery, in small quantities, can be made 30 days after receipt of order. Prices for production units start at \$3350. Datacraft Corporation, Fort Lauderdale, Fla.

Circle No. 228 on Inquiry Card

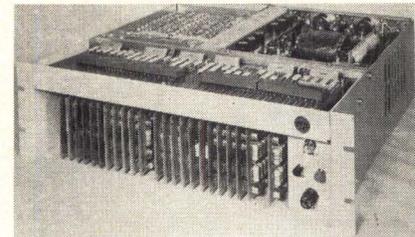


CRT READOUT WITH DECIMAL POINT

Industrial Electronic Engineers, Inc. announces the availability of an external decimal point for their well known 10 Gun CRT Readout.

Using incandescent T-1 lamps (driven independently of the tube) and mounted on specially formed PC boards designed to fit the tube assembly, this additive can be installed onto an existing assembly or ordered in conjunction with the CRT. Double assemblies may be mounted on the display to form colons if desired. Industrial Electronic Engineers, Inc., Van Nuys, Cal.

Circle No. 242 on Inquiry Card



ONE MICROSEC COINCIDENT-CURRENT MEMORY SYSTEMS

Using the standard module approach, RCA says it can now offer a broad line of one micro-second coincident-current memory systems as close to "off-the-shelf" as the industry can provide. With capacities from 4,096 words by 4-bits to 16,384 words by 40-bits and a full-cycle time of one microsecond, the RCA MS3300 Series memory systems are three-wire coincident-current systems featuring integrated circuit interfacing, logic, timing, and sense amplifiers.

"These 3-wire, 3D memory systems provide all of the advantages of 4-wire systems but are smaller, faster, more reliable, easier to maintain, and less expensive," according to B. Walley, Manager, Marketing, Memory Products Division. "They feature high-level TTL logic with excellent noise immunity, have low power requirements, are stable over the temperature range of 0°C to 50°C, and have a full range of options available for greater flexibility." Memory Products Div., RCA/Electronic Components, Needham Heights, Mass.

Circle No. 216 on Inquiry Card



MULTIPLE X-Y RECORDER

Four-pen versatility for multiple X-Y plots, combined with repeatable accuracy of 0.25% are features of the new "contour/riter" II recorder introduced by Texas Instruments Inc.

Overlapping pens and reversible chart drive combine to make the new recorder a "profiling" device, suited to unattended recording of numerous types of process runs, analog traces of computer results and experimental or production test regimes. Other interesting applications: pressure vs. volume, antenna radiation patterns, and analysis of hysteresis loops typically encountered in stress analyses and evaluation of electronic components. Texas Instruments Inc., Houston, Tex.

Circle No. 229 on Inquiry Card

WIDE RANGE OHMMETER VOLTMETER

Reasonably priced digital ohmmeter automatically measures resistances between 100 micro-ohms and 120 meg-ohms.

Fast, accurate resistance measurements are presented on a 6 window display when using the NLS Model X-1 digital ohmmeter/voltmeter. Eight full scale resistance ranges of 12/120 Ω , 1.2/12/120 K Ω , 1.2/12 and 120 meg-ohms and five full scale voltage ranges of 120 mv and 1.2/12/120 and 1000 volts in one 5 $\frac{1}{4}$ "-high rack mountable package provide both physical and measurement versatility.

Automatic ranging and polarity are standard. Resistance measurements are 4-wire, guarded. Box-in-box construction provides 120 db CMR. A standard 3-pole active filter allows accurate resistance measurements even in the presence of large amounts of degrading noise.

The X-1 wide range ohmmeter has mid-scale specifications of: $\pm 0.001\%$ of full scale + 0.01% of reading; measurement speed of 10 readings per second; and passes a current through the resistor under test of one milliamp or less. Non-Linear Systems, Inc., Del Mar, Cal.

Circle No. 233 on Inquiry Card



MINIATURE T-1 3/8 NEON LAMPS

Said to be the world's smallest, a new line of subminiature T-1 $\frac{3}{8}$ neon lamps have been introduced that feature an extremely small envelope size and a very unusual ring-electrode construction thus allowing maximum brightness when viewed from the end.

The entire surface appears to glow when excited with DC as compared with only a single electrode glowing on the conventional NE-2 series.

The round unobstructed glass envelope allows the illuminated electrode to be placed close to the round end where it may be viewed to advantage, especially when used in a panel holder. Alco Electronic Products, Inc., Lawrence, Mass.

Circle No. 240 on Inquiry Card



SMALL INSTRUMENT ENCLOSURES

Small instrument enclosures featuring styling with economy and "draft cooling" permit ambient air to be drawn through the enclosure's base and flow out through louvers in the cabinet by natural rise. The resulting cooling can eliminate the need for forced air cooling in many applications.

These rugged units are available in six different standard sizes that increase in increments of 1 $\frac{3}{4}$ " from 5 $\frac{1}{4}$ " high to 14" high, each for 19" panel mounting. Cabinets are constructed of sturdy 18-gauge cold rolled steel and finished in durable textured vinyl blue. Amco Engineering Co., Chicago, Ill.

Circle No. 236 on Inquiry Card

IT'S FLAT

IT'S FLEXIBLE



IT'S VERSATILE



IT'S TEMPBRAID

...the solution
to packaging
problems.

HITEMP BRAIDED RIBBON CABLE IS:

- Flat — as the insulated conductor
- Flexible — much more flexible than bonded and laminated cables
- Saves Space — up to 60% over round cables
- Light Weight — no jackets or fillers
- Easily Terminated — uses commercially available connectors
- Versatile — any combination of insulated conductors — any width

For more information and literature, contact:

1200 Shames Drive
Westbury, New York 11590
Tel: 516-333-4600



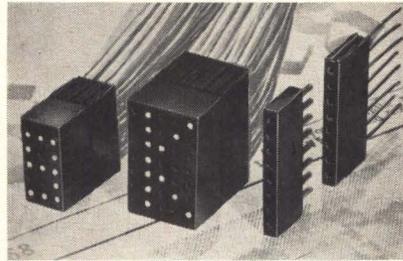
CIRCLE NO. 47 ON INQUIRY CARD

NEW PRODUCTS

SYNCHRO TO DIGITAL CONVERTER

Synchro to digital converter with resolution of 0.001° and overall accuracy of .002° features a 6 decade in-line visual readout as well as an electrical BCD output compatible with computer or printer interfaces.

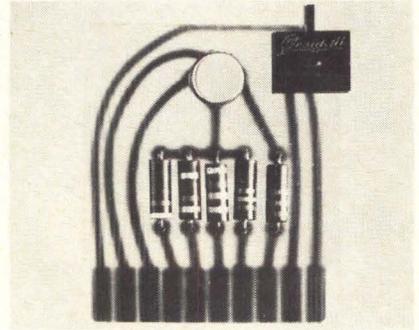
Input can be synchro or resolver signals at 11.8, 26 or 90 volts line to line at 400 Hz. The basic measuring element, a high precision toroidal transformer bridge, makes the unit extremely insensitive to wide variations in frequency, voltage and phase shift, as well as to harmonic distortion and noise. The high input impedance characteristics of the toroidal transformers eliminate the necessity for synchro signal amplifiers with their resulting gain and stability problems. Astro-systems, New Hyde Park, N. Y. Circle No. 234 on Inquiry Card



MODULAR STRIP FOR PINLITES

Pinlites Inc. now offers a modular strip incorporating their lamps.

Stack-Lite 75 is a narrow strip of molded plastic (0.075" wide) in which microminiature lamps (Pinlites) are spaced 0.075" apart to form an integral unit. These strips can be supplied in any length (within reason) as an inline display for such applications as meters, gauges, speedometers, etc. (particularly where the ambient lighting is poor). They can be stacked (as building blocks) for matrix applications. Figures, symbols, and letters can be formed by energizing the appropriate lamps. Pinlites, Inc., Fairfield, N.J. Circle No. 238 on Inquiry Card

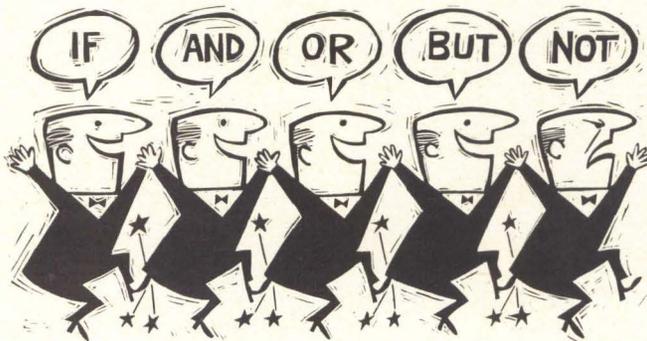


P-C PUSH BUTTON SWITCH

Grayhill's new Series 39-200 printed circuit, right angle push button switch is a SPDT, two circuit switch. The complete package extends less than 1/3" off the P.C. board and fits in a 1/2" by 0.6" rectangle. Gold plated terminals are provided for ease of soldering and allow wave soldering techniques to be used. Flush or stand-off mounting is possible with the two styles that are available.

The switch is rated at 1/4 amp., 115 VAC, resistive load for 250,000 cycles of operation. Grayhill, Inc., La Grange, Ill.

Circle No. 237 on Inquiry Card



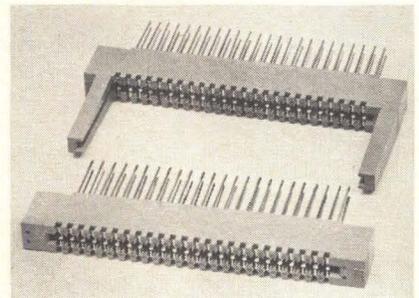
LOGIC DESIGN

Disciples of George Boole and John Venn: We have basic design positions in system organization and logic for real-time, airborne computer systems (also MOS LSI distributed logic processors). Experienced logic designers and theoretical mathematicians are invited to write Mr. Jim Anderson.

—An equal opportunity employer M/F—



LITTON INDUSTRIES, Guidance & Control Systems Division
5500 Canoga Avenue, Woodland Hills, California



CARD-EDGE CONNECTOR

Available with or without integrally molded card guides, this new card-edge receptacle incorporates 48 dual-readout contacts with 0.025-in. square posts spaced on a 0.125-in. square grid suitable for programmed wiring. It accommodates a 1/16-in. PC card.

The beryllium-copper contacts, because of a built-in preload, exert optimum contact force on the card and maintain a consistent, comparatively wide gap between facing contacts; their cantilevered design ensures maximum flexibility for resistance to set. Rated at 3 amperes, the contacts exhibit a maximum contact resistance of 6 milliohms. Standard plating is gold over nickel. Elco Corporation, Willow Park, Pa.

Circle No. 241 on Inquiry Card



MINIATURE DIGITAL PANEL METER

Compact DigiTec digital panel meter, OEM series 180, features accuracy of 0.05% of reading + 1 digit, obtained through the use of high stability circuits. Readability is enhanced by combining the non-ambiguous presentation of digital readout with the resolute qualities of analog display. Decimal points may be placed in any desired position.

The basic 100MV full scale range may be extended to as high as 1000V by choice of a single range resistor installed internally or externally. Non-linear functions can be designed to match the readout to non-linear transducers. Price is \$175.00 in quantities of 80 to 159. Delivery from stock. United Systems Corp., Dayton, Ohio. Circle No. 231 on Inquiry Card



MAG-TAPE CLEANER

Where most cleaning methods for magnetic tape leave some lint or chemical residue, and can abrade delicate surfaces, a new precision cleaning kit contains materials developed for total, non-contaminative cleaning.

The kit contains a 16 ounce aerosol can of Freon TF solvent and 600 4" x 4" Texwipe lint and static free disposable cloths which are 100% cellulose, totally lint-free, highly absorbent, non-

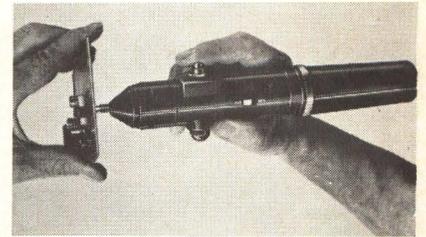
abrasive and can be used dry or with solvent cleaners. 50 lint-free urethane Foam-swabs are included for hard to reach places. The Texwipe Company, Hillsdale, N.J.

Circle No. 239 on Inquiry Card

MULTI-TAP DELAY LINE

A series of reliable, printed circuit, multi-tap delay lines have been developed which offer up to 6 separate programmable tapped sections in less than 0.6 in.³. Delay times range from 3 nanoseconds to 300 nanoseconds with delay tolerances of $\pm 2\%$ or less. Rise times are as low as 1 nanosecond. Impedance ranges from 50 to 2000 ohms. Output pulse distortion is less than $\pm 10\%$. Temperature coefficients of less than 50 PPM/ $^{\circ}\text{C}$ can be maintained over the entire temperature range of -55 to 125°C . Daven Division, Thomas A. Edison Industries, McGraw Edison, Grenier Field, Manchester, N.H.

Circle No. 246 on Inquiry Card



PORTABLE SEMICONDUCTOR TESTER

A portable, hand-held tester that checks transistors and diodes while they are still in the circuit gives a quick "go — no go" check for both conduction and cutoff characteristics, without the need for costly unsoldering. The battery-powered unit which is just nine inches long and $1\frac{1}{4}$ inches in diameter and weighs only six ounces, can be used anywhere by technicians, servicemen, inspectors, on the production line, or in the laboratory. Telvac Instrument Company, Tarzana, Cal.

Circle No. 230 on Inquiry Card

*We have talent at
Electronic Memories.*

We could use more.

*Particularly if you have digital experience in engineering,
production, marketing, or management. Call or write John
Link, Personnel Director, Electronic Memories, Inc., 12621
Chadron Avenue, Hawthorne, California 90250 (213) 772-5201*

CIRCLE NO. 48 ON INQUIRY CARD



Thick Film Package Design

A 6 page engineering report entitled "Standard Thick Film Package Design for Hybrid Micro-electronic Devices" presents a comprehensive study on the need for standard packages for hybrid circuits. Outline drawings on 3 configurations of the standard package are illustrated. The Bendix Corporation, Holmdel, N.J.

Circle No. 304 on Inquiry Card.

MosFet Device Book

A 48-page book describes the application of MOSFET devices to electronic circuits. The book describes some of the basic circuits which may be implemented successfully by taking advantage of the unique electrical characteristics of MOSFET. Full schematic diagrams are given in each case. Copies are available for \$1.50 each from Hughes distributors, or by writing to Hughes MOSFETs, 500 Superior Avenue, Newport Beach, Calif. 92663.

Card-Edge Connector Guide

This 28-page guide describes and illustrates a complete line of high-reliability card-edge connectors. An illustrated index permits instant location of the connector required for the application. The guide features a new series of connectors incorporated simple-cantilever contacts with noses that are preloaded in the insulator to exert optimum force on the p.c. card and to maintain a comparatively wide, consistent gap between facing contacts. Also covered in detail are insulator materials, contact materials, and plating. Elco Corp., Willow Grove, Pa.

Circle No. 319 on Inquiry Card.

Component Selector

This 68/69 Component Selector completely describes and catalogues the entire CDE product line—capacitors, filters and relays. The 120-page book includes Application Charts, Type Selector Charts & Standard Rating Tables arranged to guide the designer/purchaser to easy selection of the proper device and rating. Cornell-Dubilier Electronics, Newark, N.J.

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Terminal Use in Education

A 2-page fact sheet describes how Teletype terminals can be used in computer assisted instruction. The literature tells how the teletype-writers are used to assist students in the primary grades, high schools and colleges by providing a link from classrooms to a remote computer. Several case histories are given. Covered in the literature are Teletype Models 33, 35 and 37 equipment. Teletype Corporation, Skokie, Ill.

Circle No. 308 on Inquiry Card.

Digital-to-Analog Converter

Numerous applications for 12-bit digital-to-analog converter modules are described in a new 12-page booklet. Applications described include normal mode operations, four quadrant multiplying, data distributor, full or half wave digitally controlled modulator, central system calibration, source point plotting on visual display device, and line generation on visual display device. Numerous diagrams and oscilloscope traces are shown as well as detailed specifications, characteristic curves and data coding tables. Redcor Corp., Canoga Park, Calif.

Circle No. 307 on Inquiry Card.

Process Control System

Bulletin L-26 lists features and specifications of the M/97600B Process Control System. The system uses a computer for large-scale data acquisition and monitoring and other functions including automatic turbine start-up and performance calculations. The 6-page publication supplements bulletin L-24. Foxboro Company, Foxboro, Mass.

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Programming Devices

A new booklet, entitled "Design Ideas for Engineers" provides a diversified number of case-history applications for program boards and switches. The handbook describes programming devices as applied to aerospace, data logging, semiconductor testing, machine-tool programming, biological research, cable testing, and many others. It is well illustrated with photos and schematics. Sealectro Corporation, Mamaroneck, N.Y.

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Multiplier Applications

An 8-page applications handbooklet is designed to aid the applications engineer in using a new series of six high performance, four quadrant multipliers. The booklet includes twelve basic application notes ranging from performing the simple multiplication of two variables through sampling techniques, squaring, second harmonic generation and modulation to sophisticated correlation computation. The handbooklet is well illustrated and includes complete specification information and prices on each of the series of multipliers. GPS Instrument Co., Newton, Mass.

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Power Transistors

An easy-to-use catalog listing a line of military approved silicon power transistors available to the industry. Transistors are first listed numerically, then again as NPN, PNP or Planar. In these latter classifications the transistors are arranged in order of increasing "use" current, i.e., current at which gain is specified; and in order of increasing collector voltage. Complete mechanical and electrical design data is given for each transistor while additional listings give full information on 68 germanium power transistor types. Silicon Transistor Corp., Garden City, N.Y.

Circle No. 305 on Inquiry Card.

Terminal Block Selector

A 24-page catalog No. 368 features the complete line of Terminal Blocks. New additions include the compact SW-Series polypropylene snap-in track-type terminal blocks and the GB-Series single screw barrier terminal blocks for surface connection or feed-thru solder and p-c connection. Complete information with illustrations, dimensions, descriptions, and prices are included, plus a handy terminal block selection chart for fast, easy reference. Curtis Development & Mfg. Co., Milwaukee, Wis.

Circle No. 316 on Inquiry Card.

IC Accessories

A 6-page catalog covers the complete line of IC accessories, including dual in-line sockets, flat-pack holders, pluggable circuit cards, patchcord kits, connectors, IC breadboards and wrappable wiring panels. Fully illustrated and detailed with specifications, performance and ordering data, Catalog 91 provides the user with compact, easy-to-use reference literature on the entire assortment of IC accessories for testing, bread-boarding or sub-system-to-system planning. Cambridge Thermionic Corporation, Cambridge, Mass.

Circle No. 301 on Inquiry Card.

Readouts

This 8-page short form catalog describes the full line of rear-projection readouts; a remarkable CRT display; smaller IC driver/decoders for driving incandescent lamps; and a broad line of subminiature incandescent lamps. Gives specifications, advantages and pricing information on readouts. Industrial Electronic Engineers, Inc., Van Nuys, Calif.

Circle No. 314 on Inquiry Card.

Multilayer PC Boards

Complete in-house multilayer printed circuit board manufacturing capability is the subject of this color brochure. Illustrations and narrative descriptions cover clean-room and quality control processing equipment and facilities. Actual micro-cross-section photographs are used to illustrate proprietary "etch-back" method and plated-thru hole processing. National Technology, Inc., Santa Ana, Calif.

Circle No. 312 on Inquiry Card.

Flexible Cable

Four page bulletin offers more comprehensive information on flat flexible copper or aluminum cable than has previously been available. Extensive data is provided on a new line of flexible printed circuitry and outlines all pertinent parameters including material, specifications, shielding percentages, and catalog numbers. Coleman Cable, River Grove, Ill.

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Miniature Switches

An illustrated 4-page data sheet, number 413, provides complete electrical and mechanical specifications on a new line of miniature snap-acting switches. The data sheet illustrates the choice of standard switch configuration and a wide variety of lever actuators. Also shown are four types of terminals including the new 1/4 inch quick-connect. Unimax Switch, Wallingford, Conn.

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ELECTRONICS ENGINEERS

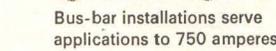
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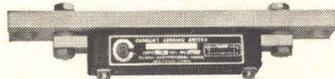
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LITERATURE

Power Supply/Voltmeter

A laboratory instrument, which can serve as either a high-precision power supply or a power differential voltmeter, is described in a new 12-page, well-illustrated brochure. Bulletin LS describes the basic LS Series high-precision power source and the two plug-in accessories designed for use with the basic power source. The bulletin gives complete specifications, capabilities, and prices. Lambda Electronics Corp., Melville, L.I., N.Y.

Circle No. 300 on Inquiry Card.

Logic Handbook

This 512-page book includes a digital logic primer covering numbering systems, Boolean algebra, binary-coded decimal codes; 27 pages of module application notes; a complete 68-page study of analog-to-digital conversion and a 23-page computer catalog. Complete technical information is included on M Series integrated circuit and K Series industrial modules. It also includes five appendices on MIL STD 806B and DEC symbols; a powers of two table; a list of standard electronic abbreviations, definitions, a bibliography and price list. Digital Equipment Corporation, Maynard, Mass.

Circle No. 315 on Inquiry Card.

IC Test System

A 12-page descriptive brochure details features of the Series 5000 Integrated Circuit Test System. Basic features of the system, inherent capabilities, the modular design concept, options for future enhancement, programming, and applications are discussed in the brochure. Included are block schematics of the system, multiplexing, and the Digital Time/Voltage Module, a high-speed time and voltage measurement circuit with automatic calibration during all measurements. Fairchild Instrumentation, Sunnyvale, Calif.

Circle No. 310 on Inquiry Card.

Printed Circuit Connectors

A simplified, 20 page catalog showing details of standard PC connectors is available. It has been designed to make the selection of connectors easier by the inclusion of a Chart-Index in the front of the catalog. Arranged according to contact spacing, connectors start with .050" microminiature and progress through .100", .125", .150" and .156" contact centers. The catalog also covers available test point connectors for PC cards. Viking Industries, Inc., Chatsworth, Calif.

Circle No. 302 on Inquiry Card.

Wafers and Dice

This catalog contains information on wafers and dice including PNP transistors, NPN switches, NPN amplifiers, diodes, zener diodes and silicon dioxide capacitors. It includes detailed specifications (including typical chip yield) for procurement of family types of PNP and NPN transistors for use as switches, both high and lower power amplifiers, and in oscillator applications. Also included are illustrations of typical devices and dimensional drawings for all devices listed in the catalog. United Aircraft, Trevose, Pa.

Circle No. 311 on Inquiry Card.

Semiconductor Data Book

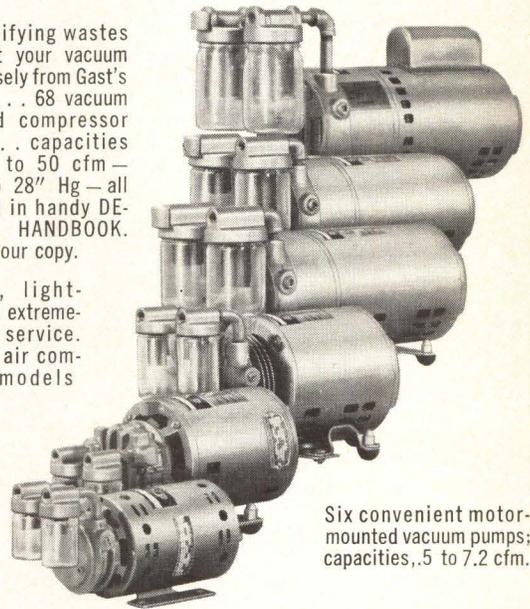
The third edition of *The Semiconductor Data Book* identifies and characterizes all semiconductor devices with 1N, 2N and 3N prefix numbers registered with the EIA, plus a large number of in-house types. The book has more than 1750 pages, containing complete data sheet specifications for over 3,000 devices in 14 different product categories. Also included is a special section on mounting hardware, I.C. patchboards, and power transistor heat-sinks. Sixteen application notes to aid the user in his understanding of the data contained in the book are included. Priced at \$4.95, it may be purchased from any authorized Motorola Semiconductor Distributor, or by writing to Motorola Semiconductor Products Inc., Dept. TIC, Box 13408, Phoenix, Ariz.

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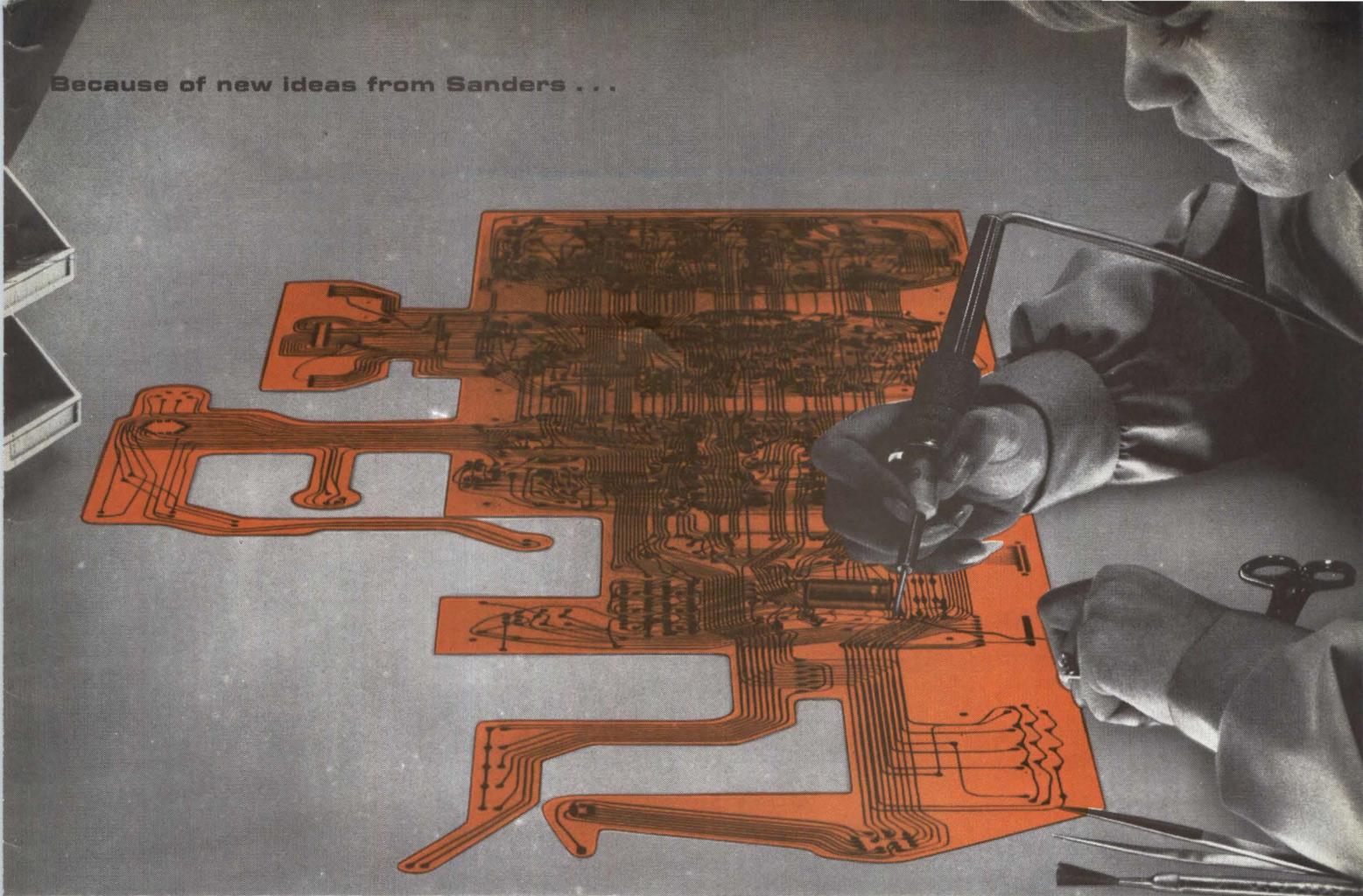
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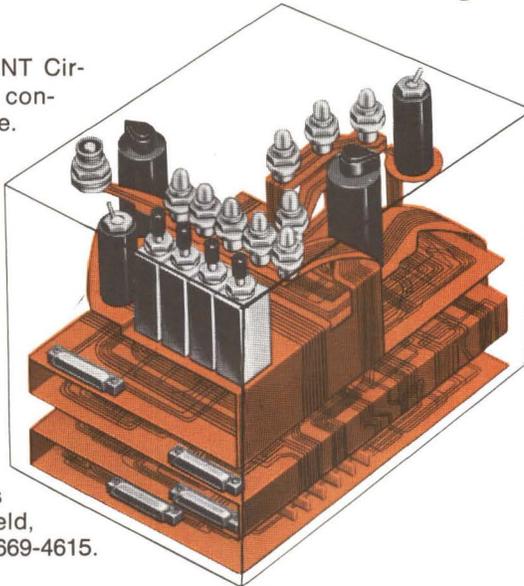
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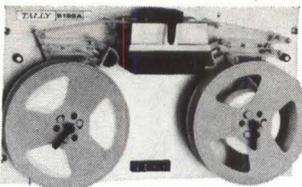
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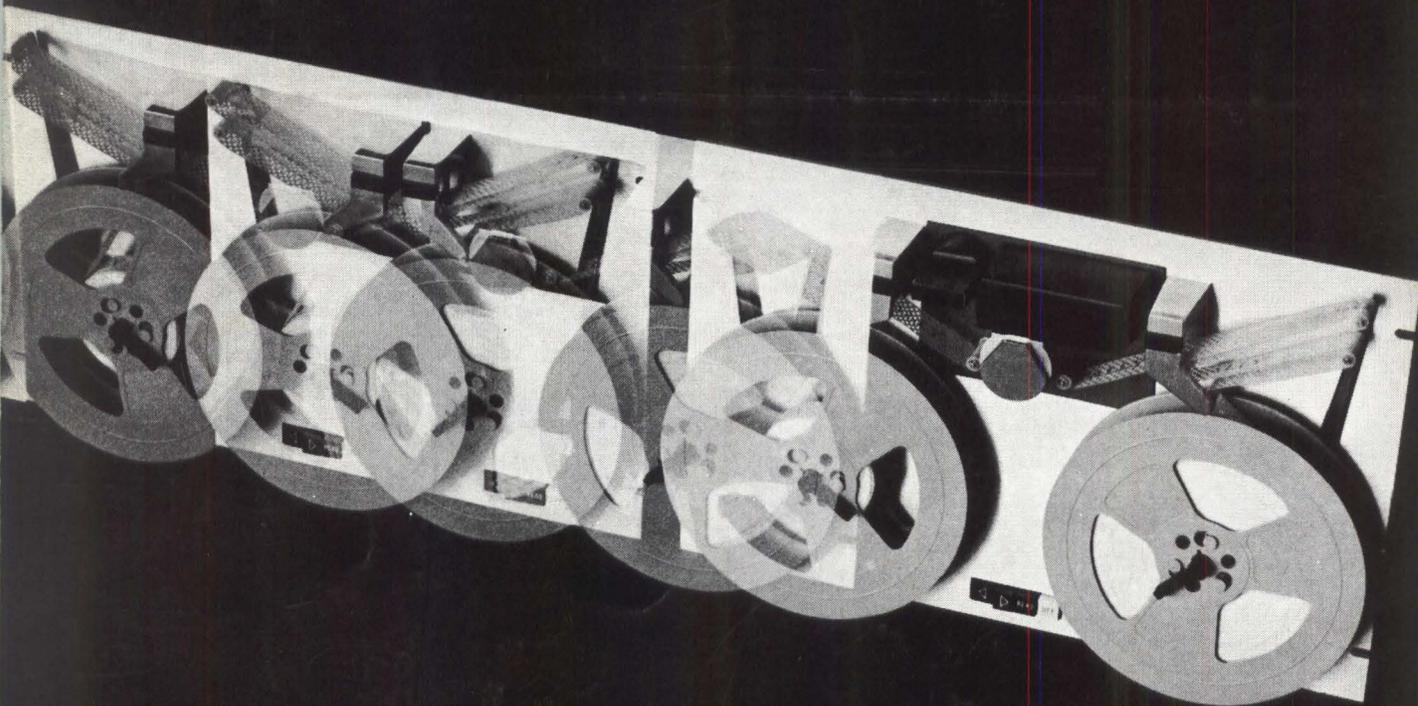


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