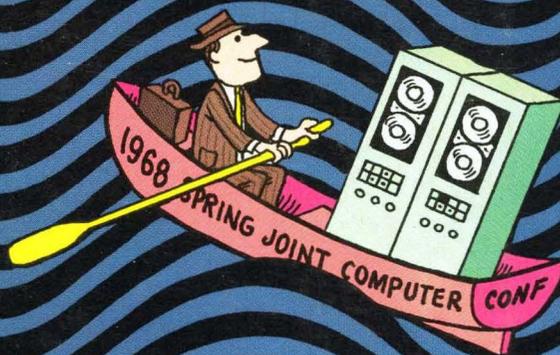


COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

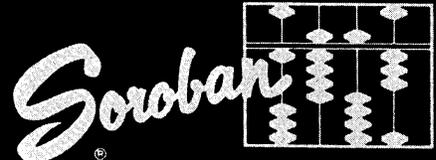
APRIL 1968



Super Compact Card Reader

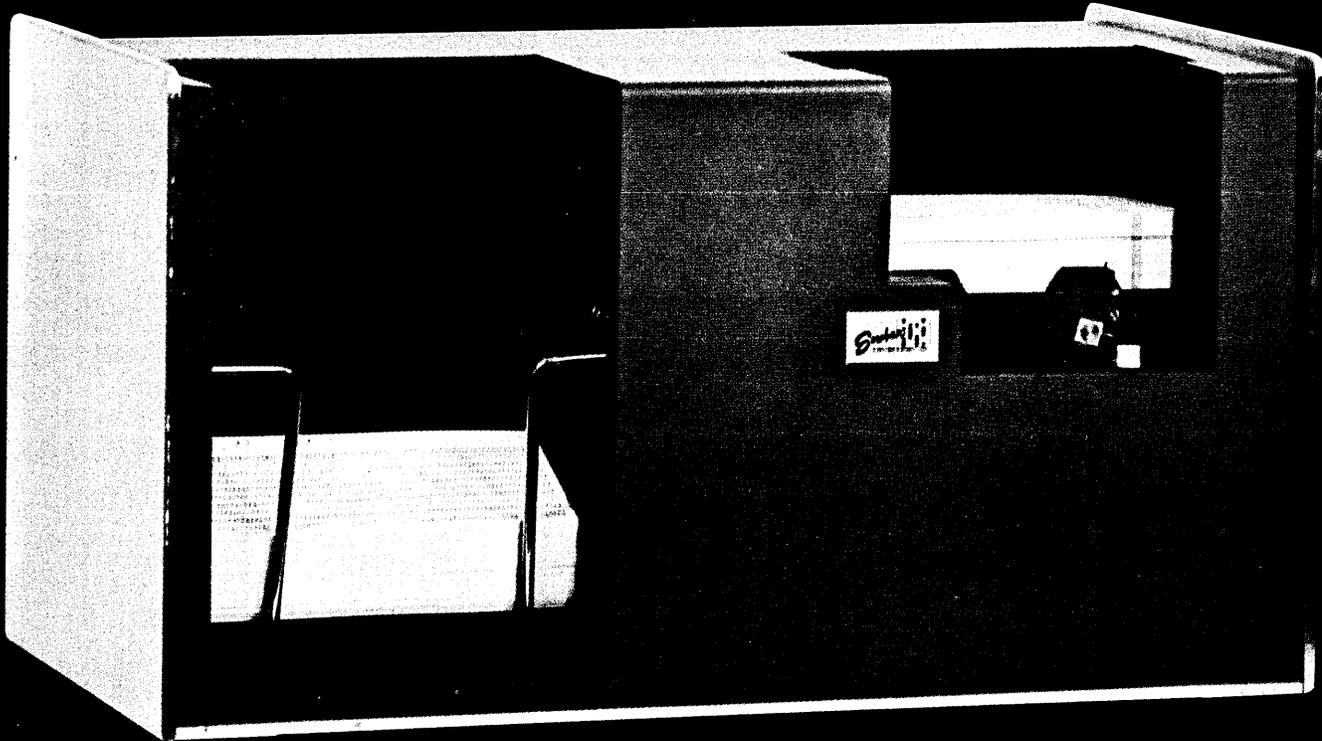
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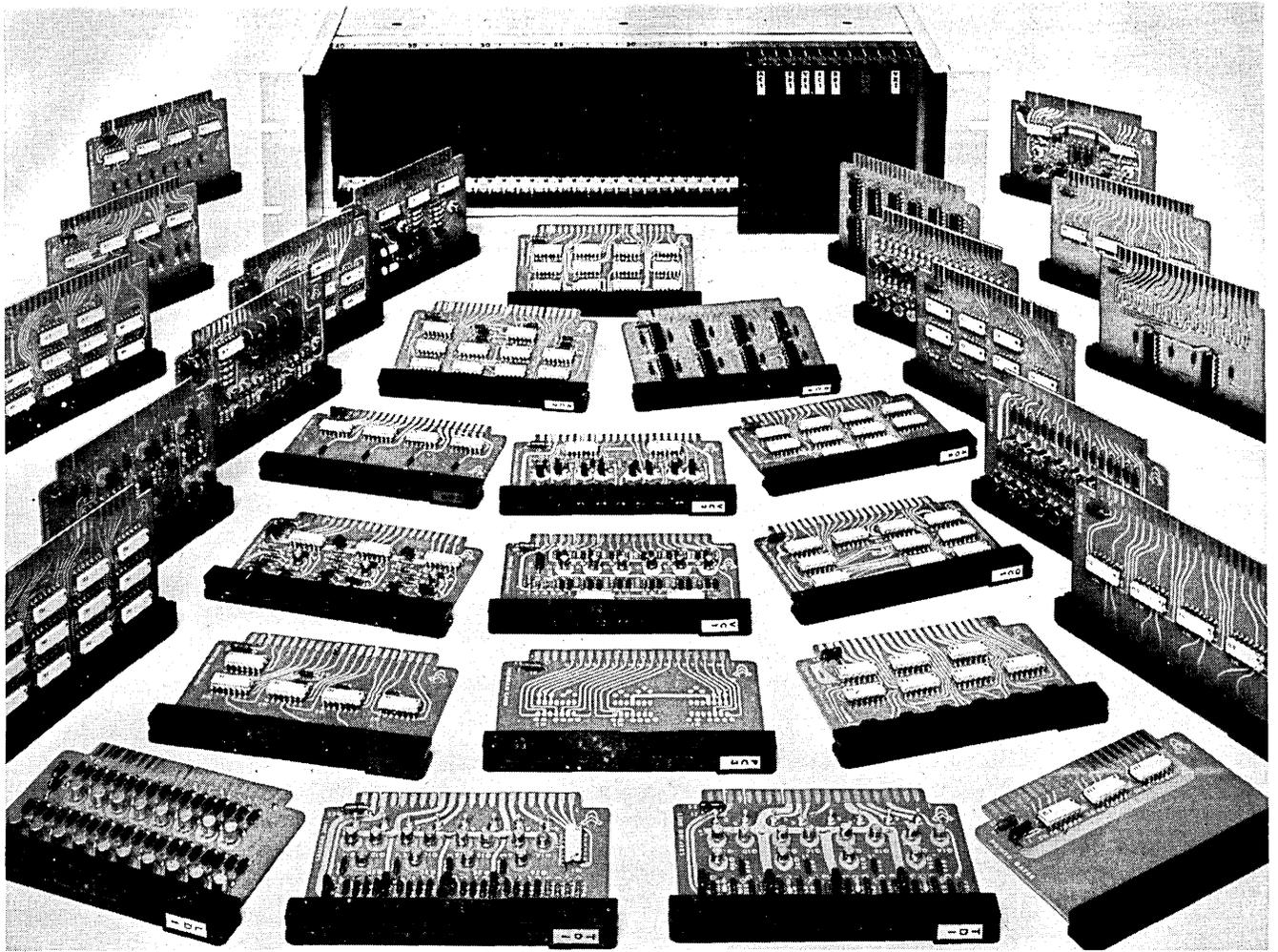
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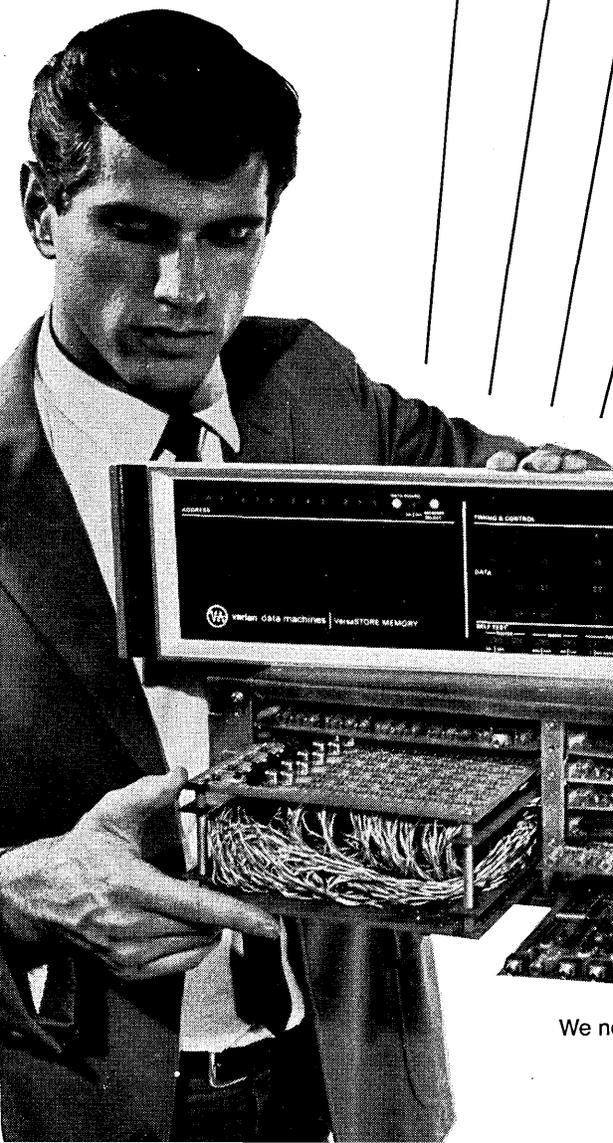
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COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

FEATURES

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A description of improvements and techniques used in designing small memories for 360 computer systems.

72 A HIGH-SPEED GENERAL PURPOSE INPUT-OUTPUT MECHANISM WITH REAL-TIME COMPUTING CAPABILITY

Non-incremental input-output mechanism performs high-speed calibration and redundancy reduction on data received as phase modulation on carrier wave forms and presents the partially processed data in convenient whole-word format to a digital computer.

80 A NEW DISPLAY TERMINAL

Filling the gap between the teletypewriter and expensive, refreshed, CRT displays, this terminal, developed for computer time sharing, provides alphanumeric and line drawing capability at moderate cost.

88 COMPUTER CIRCUIT NOISE IMMUNITY AND SYSTEM NOISE

This article provides a broad coverage of the spectra 70 and an advanced computing system in terms of their circuit noise immunity and system noise source.

94 BULK CORE IN A 360/67 TIME SHARING SYSTEM

Comparison by analysis and test of a 360 time shared system with drum storage and with Large Capacity Core Storage reveals that the LGS provides nearly an-order-of-magnitude-better performance, in terms of response time, availability, capacity and generality, than the drum system.

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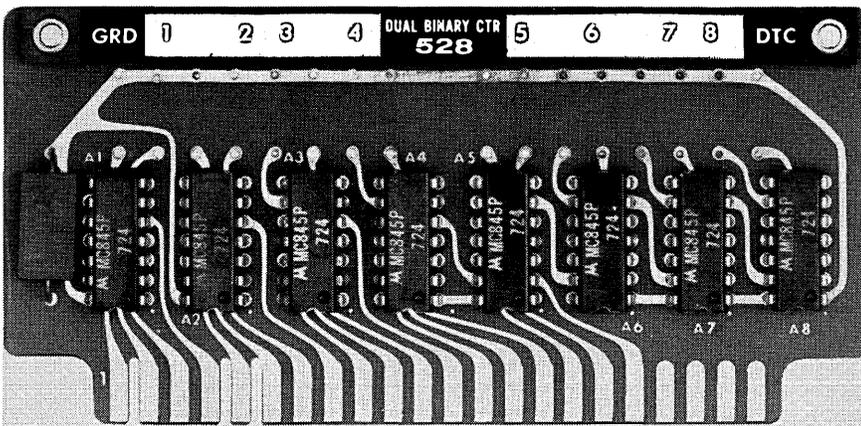
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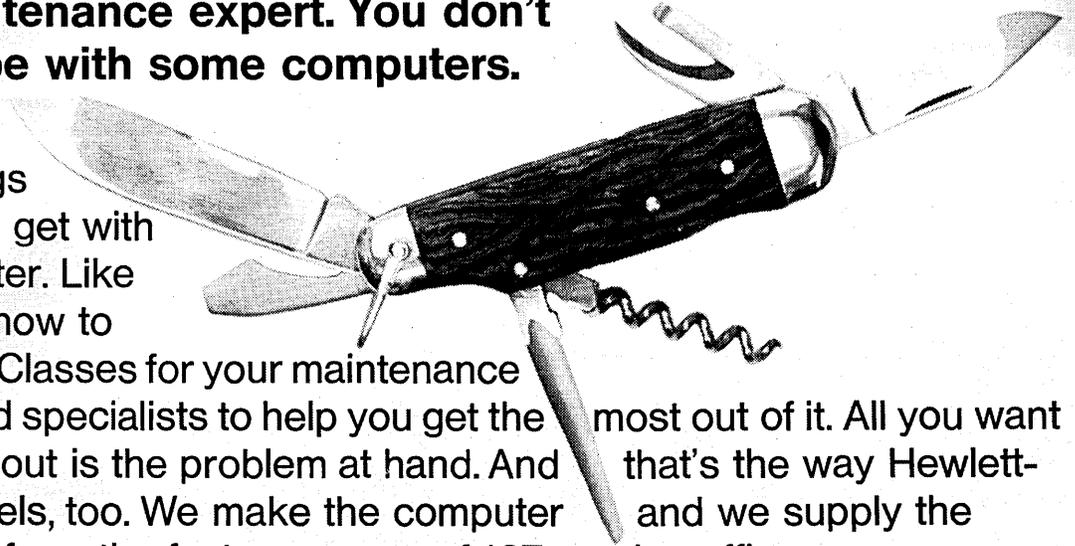
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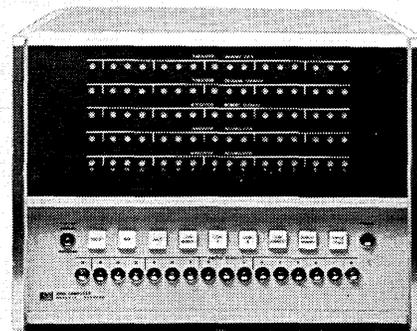


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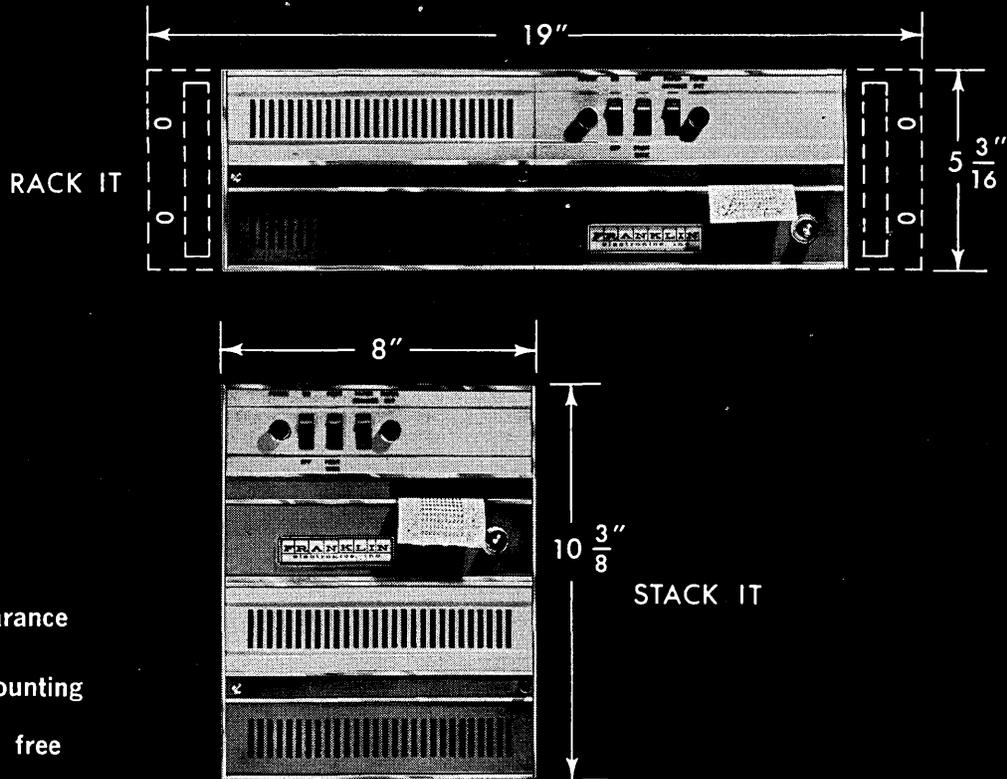
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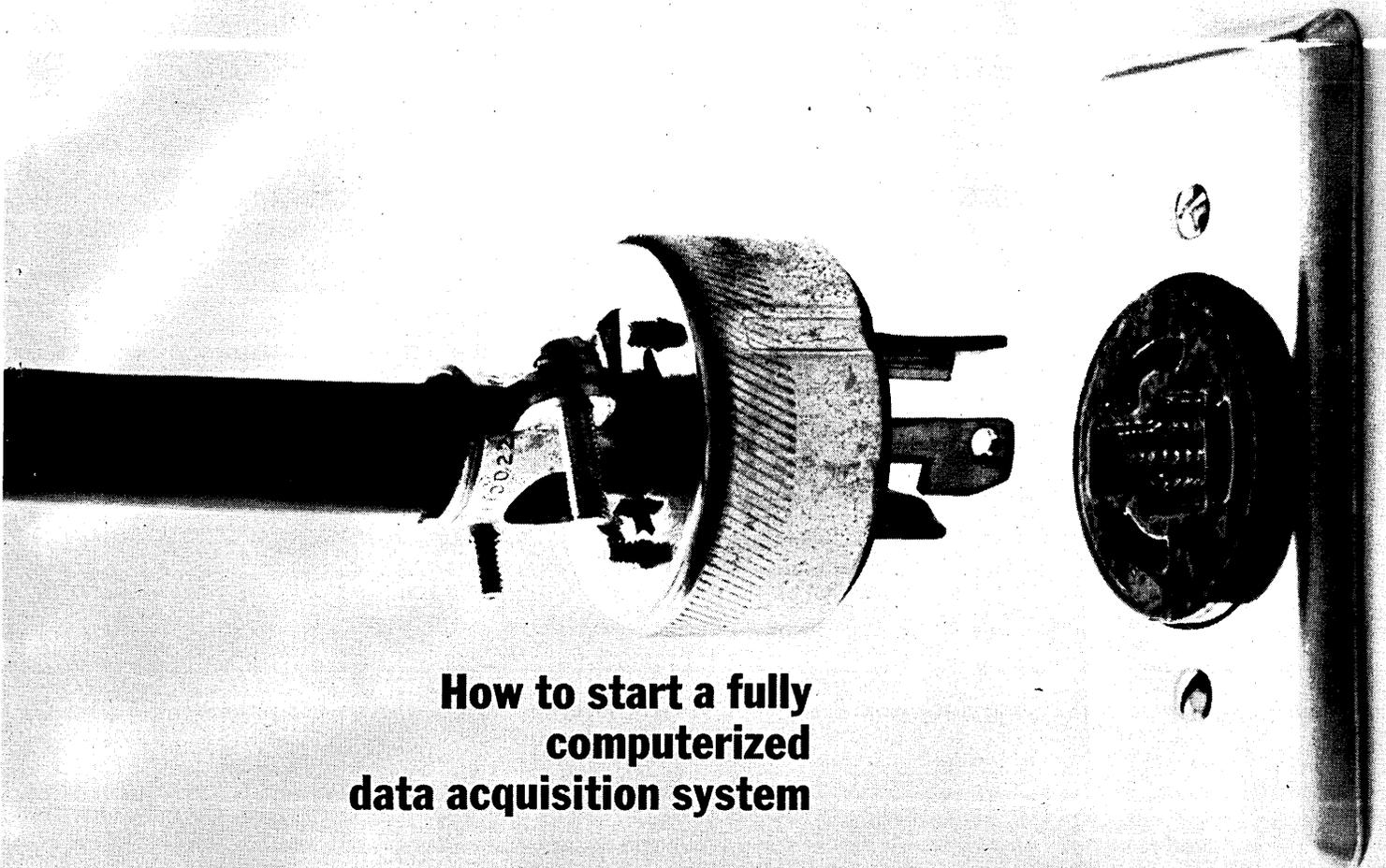
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			NUMERIC	ALPHA-NUMERIC
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812D-4	4	12	✓	
812D-6	6	12	✓	
812D-8	8	12	✓	
812D-10	10	12	✓	
1200	12	20	✓	
1200	12	30	✓	
1200	12	40	✓	
1600	16	20	✓	
1600	16	30	✓	
1600	16	40	✓	
2200	22	20	✓	
2200	22	30	✓	
2200	22	40	✓	
2200	22	20		✓
3200	32	20	✓	
3200	32	30	✓	
3200	32	40	✓	
3200	32	20		✓

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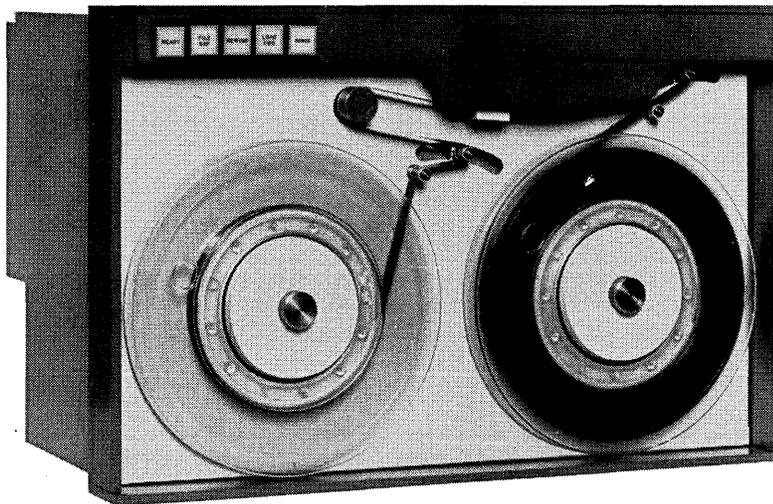
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Do you benefit? You bet you do because you are guaranteed that a magnetic tape written on

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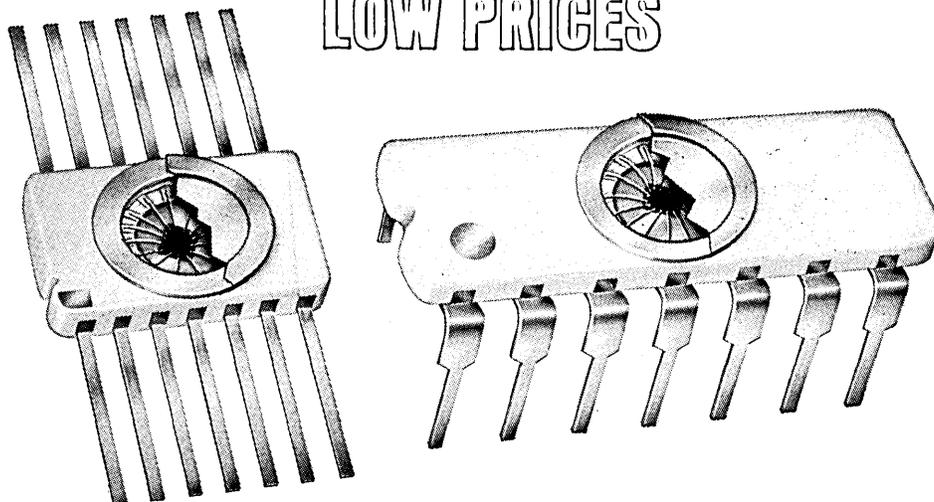
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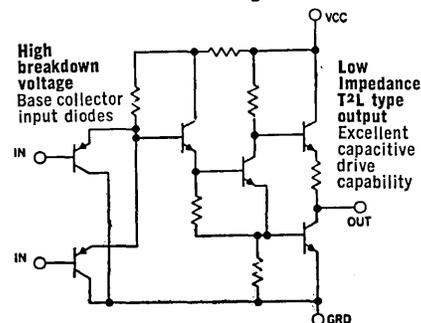
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REGAP:

3300 25-BIT MOS STATIC SHIFT REGISTER

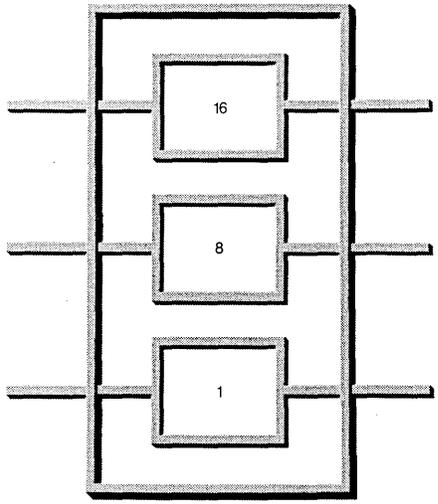
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The 3300 is the first MOS device we've introduced since December 11, 1967. (The first four were the 3701 six-channel multiplex switch, 3702 three-input gate, 3700 four-channel multiplexer switch, and the 3300 four-bit dynamic shift register.) The 3300 is a monolithic IC utilizing Planar P⁺-channel enhancement mode MOS technology. It is designed to be used for digital delay lines and long serial memory storage in radar systems and computers. It has applications for data storage in memory systems.

The 25-bit device comes in a TO-9 can and will operate over the entire temperature range from -55°C to +85°C. There are independent 15, 8, and 1-bit data inputs within the package. Power dissipation is typically 200mW per bit. Speed is typically 500ns. The clock drive circuit is simplified by a single-phase clock input. The output is buffered to improve drive capability.

Volume quantities of the 3300 are now available. Fairchild distributors have it in stock. Write for complete space and applications information. Ask about our other new products, too.

Phone in a separate format please.



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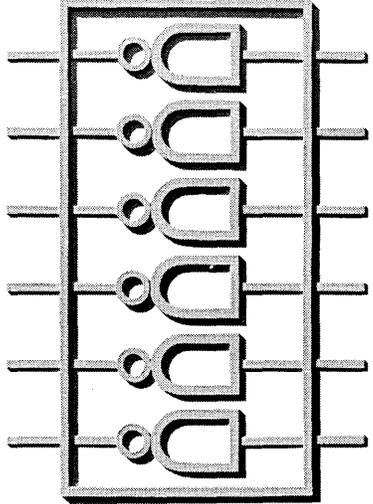
CIRCLE READER SERVICE NUMBER 119

9110 HIGH LEVEL LOGIC HEX INVERTER

Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **20**.

The 9110 is the fundamental element of our new high noise immunity family. It features worst case DC noise immunity of 0.5 volts. And AC noise immunity is even better (it can reject pulses of 100 nanoseconds duration and 20 volts amplitude minimum). Other members of the family provide interfacing capability to make the 9110 compatible with TTL levels.

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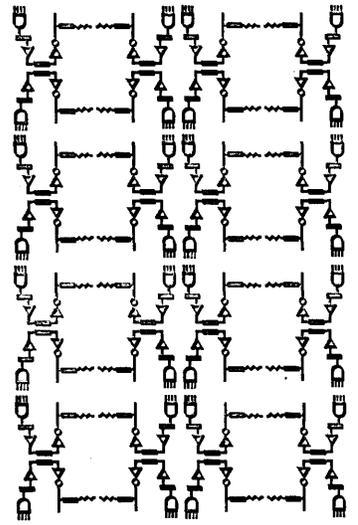
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Since the 4500 series is completed without your specific requirements, we've prepared a kit to help you design your own custom circuits. It's at your Fairchild distributor now. Write for detailed space and applications information.



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CIRCLE READER SERVICE NUMBER 121

3320 MOS 64-BIT, 4-PHASE SHIFT REGISTER

Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **22**.

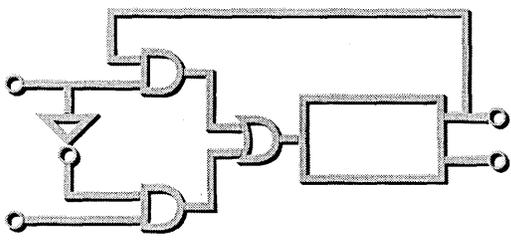
The 3320 is an anti-regulator accumulator. Its input logic can be used to control the loading of new information, or the refreshing of existing information. In the device, its primary applications include (1) data accumulation in memory systems; (2) long serial memory for applications long delay time in radar equipment and industrial serial system control.

No DC power supplies are required for 3320 operation. It comes in a TO-9 can and is operable over the entire temperature range from -55°C to +85°C. Both data and de-accumulation outputs are provided. Power dissipation is approximately 200mW per bit at 2MHz.

The 3320 is a product of Planar P⁺-channel enhancement mode technology. It is the sixth monolithic MOS IC we've introduced since December 11, 1967. (The others are the 3701 six-channel multiplexer switch, 3702 three-channel multiplexer switch, 3300 three-bit dynamic shift register, and the 3300 25-bit static shift register.)

Volume quantities of all six devices are available. Your Fairchild distributor has them in stock. Write for complete space and applications information.

Phone in a separate format please.



Fairchild Semiconductor, A Division of Fairchild Camera and Instrument Corporation. 202 Parkside Drive, Mountain View, California 94034. DTL 80-0411. TYP. 810-274-6400.

CIRCLE READER SERVICE NUMBER 122

Fairchild is introducing a new integrated circuit every week. The last two months look like this.

FAIRCHILD
SEMICONDUCTOR

Starting October 8, 1987, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **23.**

3705 8-CHANNEL MOS MULTIPLEX SWITCH

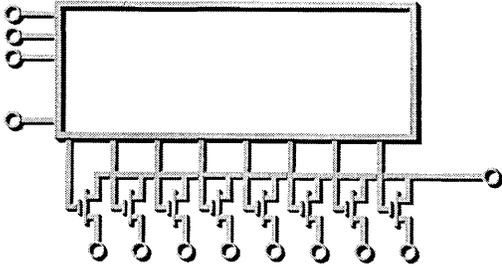
The 3705 is designed for use in analog/digital converters, multiplexing applications, digital transmission systems, airborne and ground instrumentation signal routing functions, and replacement of mechanical relays in CCS, computers and has binary-coded logic inputs and an channel blanking output.

The 3705 is our seventh new MOS device. (Since December 11, 1987, we've introduced the 3701 8-channel multiplex switch, 3.152 three-input gate, 3700 four-channel multiplex switch, 3302 32-bit dynamic shift register, 3300 32-bit static shift register and the 3301 84-bit, 4-phase shift register.)

The 3705 is a product of Planar[®] P-channel enhancement mode technology. It features zero offset voltage, input gate protection, typical ON resistance of 150 Ohms (20V input), leakage from 0 to +6 volts, nano-ampere leakage currents, and input-blanking section to minimize level through. It comes in a standard hermetic DIP and will operate in a range from -55°C to +85°C.

You can get volume quantities of all new Fairchild devices now. Your Fairchild distributor has them in stock. Write for complete specs and applications information.

*Planar is a registered Fairchild process.
To order the 3705, ask for:
Part No. 3705
Ask 480 884 Part Price \$1.00 (100,000)
Ask 480 814 Part Price \$1.00 (100,000)



FAIRCHILD SEMICONDUCTOR A Division of Fairchild Camera and Instrument Corporation
FAIRCHILD SEMICONDUCTOR 815 Fairchild Drive, Mountain View, California 94035, (415) 961-8111 FAX: 415-961-8242
CIRCLE READER SERVICE NUMBER 123

Starting October 8, 1987, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **24.**

μA722 PROGRAMMABLE D/A - A/D CONVERTER CURRENT SOURCE

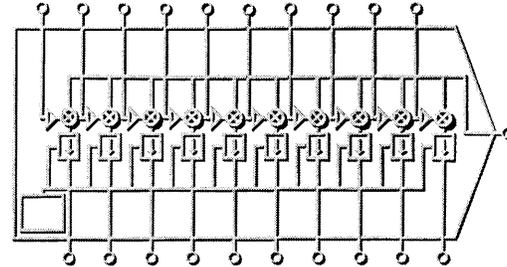
Fairchild's $\mu A722$ is the first MOS linear integrated circuit. It's compatible with other linear ICs (702, 709, 710) as well as CMOS and other digital circuitry.

The $\mu A722$ is a high-speed, current summing, programmable, digital-to-analog converter. It's the result of a breakthrough in monolithic technology—the extensive tight matching of more than 70 active components. The device consists of a reference supply and 10 current sources connected to a single output terminal through 12 associated current steering switches. All on a single monolithic chip. Both the full-scale output range and the coding format (BCD or binary up to 10 bits) can be varied with an external resistor array. $\mu A722$ performance specs include 8-bit or 10-bit accuracy, 10-bit resolution, 100ns settling time, 20mA maximum full-scale current, and 2.5mA maximum full-scale current.

The new device can be used as a basic building block in a number of accurate, sensitive, instrumentation and computer systems. Its most important application will be as a D/A converter in high-resolution A/D converters. With the $\mu A722$, you can build a 81000 A/D converter for less than \$200. It can also be used as a logarithmic D/A converter, a D/A multiplier, a limited-range multiplier, and as a meter drive in digital systems where the meter is used for monitoring.

The $\mu A722$ comes in a 24-pin hermetic package. It will operate over the entire temperature range from -55°C to +85°C. It's available in volume quantities. Your Fairchild distributor has it in stock now. Write for complete specs and applications information.

*Standard package.
To order the $\mu A722$, ask for:
Part No. $\mu A722$
Ask 480 884 Part Price \$1.00 (100,000)
Ask 480 814 Part Price \$1.00 (100,000)



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CIRCLE READER SERVICE NUMBER 124

Starting October 8, 1987, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **25.**

4510 DUAL FOUR-BIT COMPARATOR

The 4510 is the first standard off-the-shelf circuit produced with double-layer metalization. It's the first 40100 CMOS design. It is based upon our 4000 Microchannel[®] Array New Product (NPA), which can be customized for virtually any function in any digital logic system.

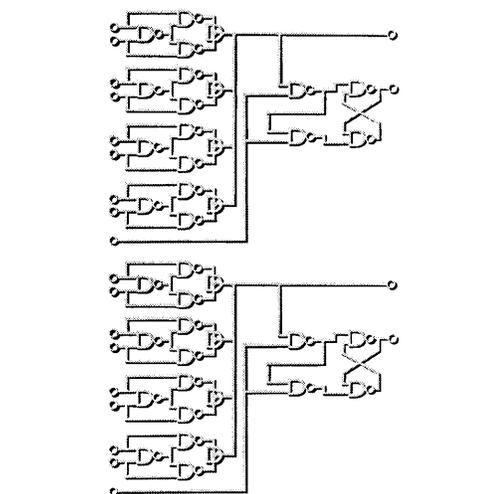
The 4510 is designed for applications requiring the equivalence of two numbers in real time. It consists of two identical 4-bit comparators. Each comparator accepts two 4-bit numbers and provides an output signal when they are identical. Inputs and outputs are CMOS-compatible. A third lead shows the comparison output when the clock input is high. Outputs may be wire ORed together to expand the comparison capability to 8-bit characters.

Applications for the 4510 include digital printers where it can be used to select the proper character in each print cycle, in digital leaders to permit dot-range functional testing and in programmable counters.

The 4510 is available in both a standard hermetic DIP and in a flat-pack. It will operate over military and industrial temperature ranges (-55°C to +125°C and 0°C to +70°C). We have the new device in volume quantities. It's on your Fairchild distributor's shelf now. Write for complete specs and applications information.

To order the 4510, ask for:

Part No.	Package	Temperature Range	Q-100	Q-100	(100,000)
Ask 480 884	DIP	-55°C to +125°C	\$1.00	\$1.00	\$1.00
Ask 480 814	Flat	-55°C to +125°C	\$1.00	\$1.00	\$1.00



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CIRCLE READER SERVICE NUMBER 125

Starting October 8, 1987, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **26.**

9034 256-BIT READ-ONLY MEMORY

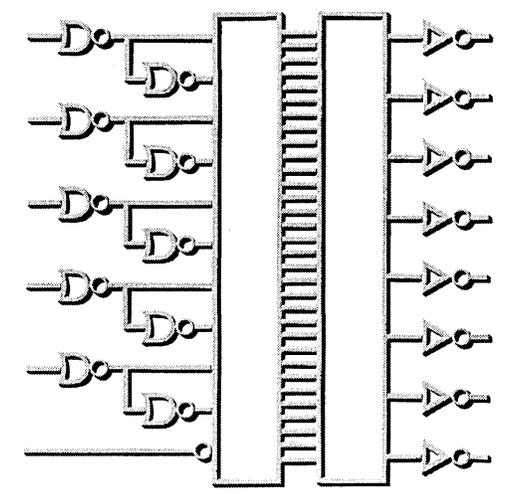
The 9034 is not only CMOS-compatible, but also has an access time of less than 10ns. It is particularly suited for control of high-speed systems, for microprogramming, for high-speed data bus look-up, high-speed code comparison and display driving applications.

Five input lines control selection of one of 52 8-bit words. An enable input controls the selection of the 9034 as either a parallel-addressed device. The equivalent outputs of several 9034s can be ORed together to produce an 8-bit output on each of the 8 bits. Each address line, and the enable line, represents an TTL load. The outputs can sink 10mA.

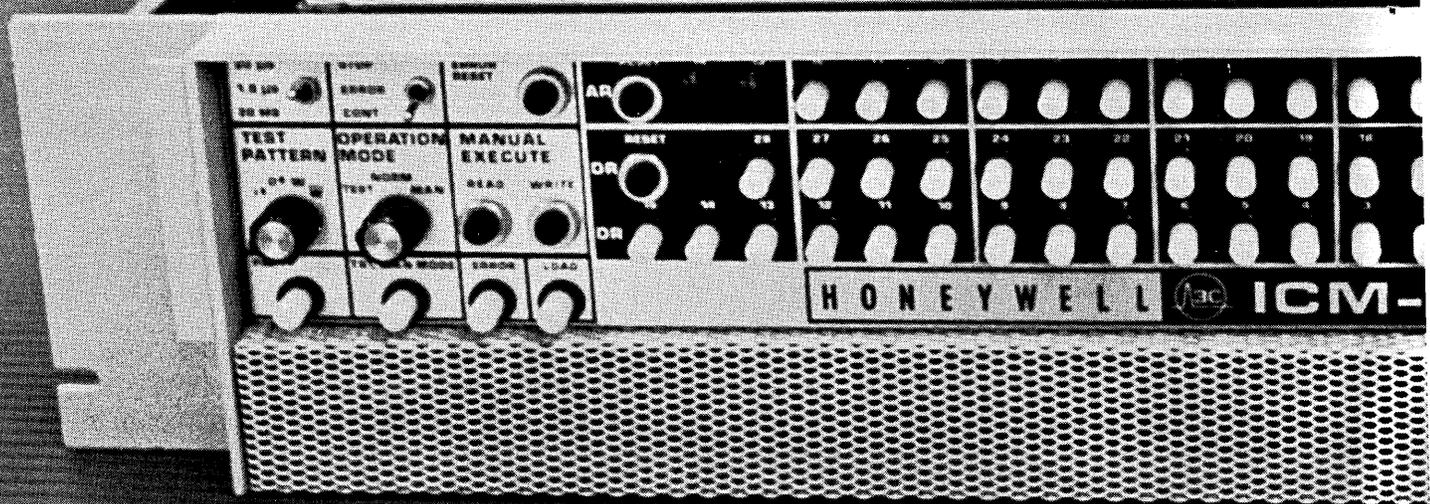
Power dissipation is 450mW maximum.

The 9034 operates with 5V power supply and comes in a 24-pin hermetic DIP and operates over both military and industrial temperature ranges (-55°C to +125°C and 0°C to +70°C). The 256-bit device cannot be customized without your custom specifications. However, if you'd like to play around with it (for more), we've prepared a sample device that represents 0 through 4 of an alphanumeric character generator for 8-bit dot display. It is called the 9034B. You can get it at your Fairchild distributor (see Part No. and price below for the sample), write for complete specs and applications information on the 9034. To order the 9034B, ask for:

Part No.	Temperature Range	Q-100	Q-100	(100,000)
Ask 480 884	-55°C to +125°C	\$1.00	\$1.00	\$1.00
Ask 480 814	0°C to +70°C	\$1.00	\$1.00	\$1.00



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FAIRCHILD SEMICONDUCTOR 815 Fairchild Drive, Mountain View, California 94035, (415) 961-8111 FAX: 415-961-8242
CIRCLE READER SERVICE NUMBER 126





3-week delivery...

on the standard 1 μ -sec
I/C memory system
that packs 1/2 million
bits in a single
5 1/4" high unit.

That's the ICM-40. A fast, highly reliable core memory system that's ready to meet your system requirement.

And when you say so, we'll give you 3-week CFS (Certified Fast Shipment) under our accelerated shipment plan.

What's more, the ICM-40 is a standard product... a proven performer with over 5,000 hours of life test without failure. Plus, some 400 actual installations; same success rate. What you'd expect from the most experienced memory maker.

I/C Construction — The ICM-40 is a 1 microsecond, full-cycle, magnetic core memory designed for operation as a high-speed random-access store. It is a basic system module that takes maximum advantage of the high reliability and low power consumption of integrated circuitry.

Packaging — Compactness and a high degree of maintainability are achieved in the ICM-40 design by packaging all of the circuitry on readily accessible, removable circuit modules.

Capacity — The ICM-40 packs nearly 1/2 million bits in a single 5 1/4" high module. The basic unit can be specified for up to 16K words, 4-26 bits per word. It's big brother, the ICM-40E with capacities of 32K words, 4-78 bits per word is available with 60-day CFS.

If you've drawn a block marked "core memory" recently, why not find out more about the ICM-40/40E. You'll be pleased by their versatility. And the standard-product pricing. And our Certified Fast Shipment commitment.

Now, don't you think it's about time you called us? Or, write Honeywell, Computer Control Division, Old Connecticut Path, Framingham, Massachusetts 01701.

Honeywell

 **COMPUTER CONTROL**
DIVISION

CIRCLE ON. 9 ON INQUIRY CARD



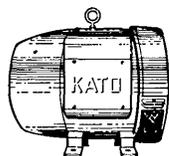
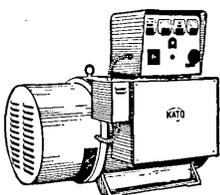
For the kind
of clean power
it takes to
keep computers
efficient,
**Control Data
Corporation
calls on KATO**

KATO Engineering is one of the major suppliers of matched motor-generator sets for line isolation and cycle conversion...at CDC and throughout the computer industry.

When precision equipment demands *pure* power, free from line transients, phase unbalance and frequency fluctuations, a KATO Motor-Generator Set is the answer. In the computer industry, in communications, ground-support operations and industrial process-control functions, KATO M-G Sets take imperfect commercial power and provide the exact, balanced, regulated output desired, with continuing efficiency and absolute minimum maintenance. KATO offers the widest possible range of M-G Sets and control equipment *plus* 40 years of power engineering experience. Why not get the details?

Free 8-page folder gives complete information on KATO M-G Sets. Write for your copy today.

Typical KATO M-G Set supplied to CDC—common-frame, common-shaft construction. Motor is 30 H.P., 220/440 volt, 3-phase, low-slip, squirrel-cage induction type. Generator delivers 20 KVA, 120/205 volt, 400-cycle, 3-phase and features brushless excitation. Free-standing cabinet houses both motor and generator controls.



*KATO makes many power products...
AC Generators • DC Motors and Generators*



KATO ENGINEERING COMPANY

1403 First Avenue • Mankato, Minnesota 56001

Introducing the Varian Data 520/i

New - dual environment computer for systems applications

The Varian Data 520/i is our newest systems-oriented computer with some remarkably useful innovations. We've designed the Varian Data 520/i to handle independent, dual tasks quickly and efficiently, and that's why we've called the 520/i a dual-environment computer. To do the job we've equipped the 520/i with two complete sets of hardware registers, including index registers.

These independent registers allow the 520/i to run parallel programs, each program using its own set of registers. And a single 1.5 microsecond instruction is all it takes to transfer control between parallel programs or between processing and I/O programs.

For easy adaptability to the user's data needs, we've designed the Varian Data 520/i to manipulate data in multiple 8-bit bytes. This multi-precision capability allows the 520/i to perform arithmetic in 8, 16, 24 or 32 bit lengths, within the same program! And—each program can change its own precision at any time.

Our new Varian Data 520/i, with a 4K memory, sells for less than \$10,000. If you'd like to know more about it, write for a Varian Data 520/i brochure.

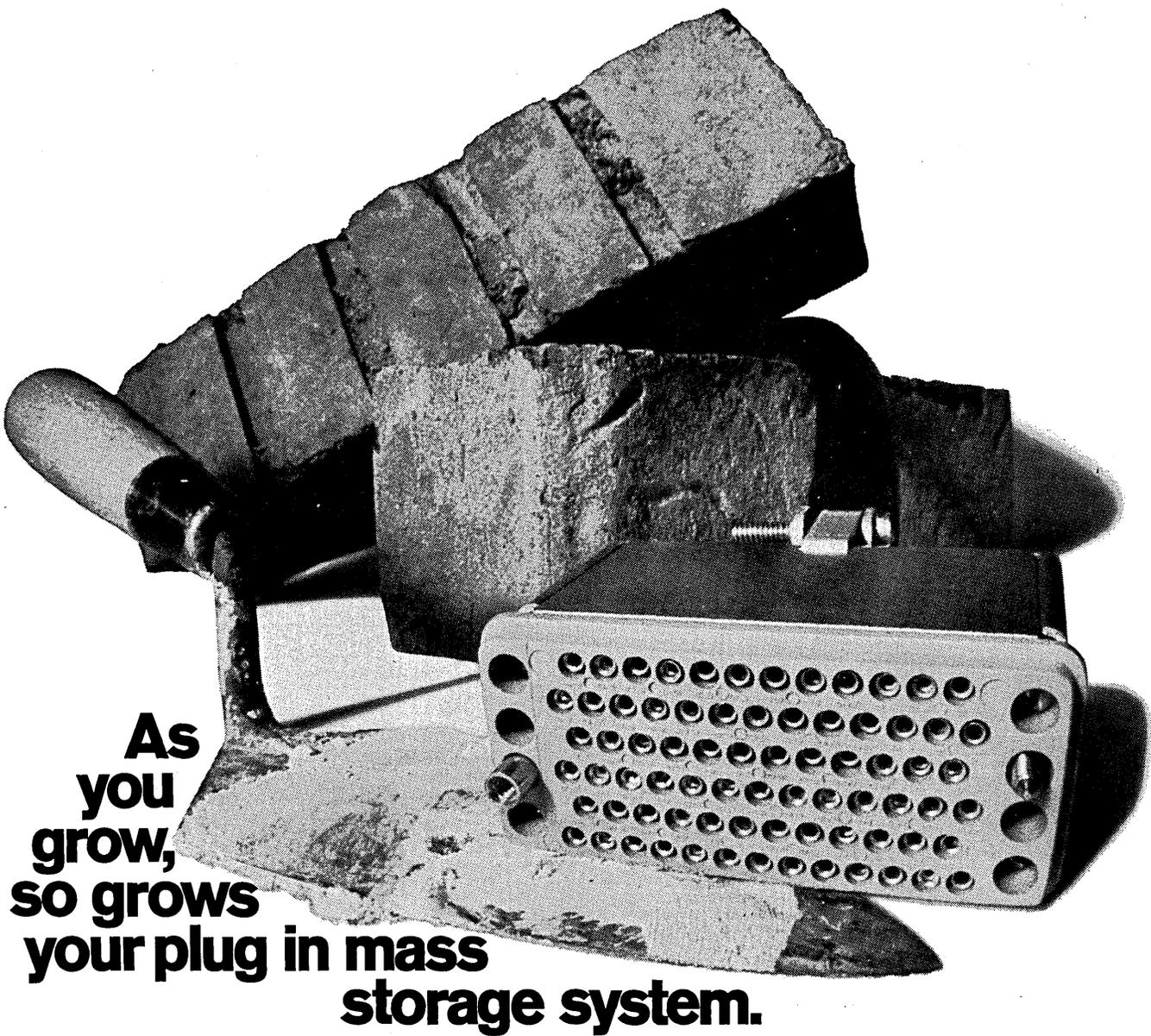


Formerly Decision Control, Inc.

1590 Monrovia Ave., Newport Beach, Calif. / (714) 646-9371 TWX (910) 596-1358

See the new Varian Data 520/i, and the 620/i, at Island Q, SJCC.





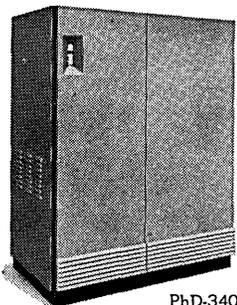
**As
you
grow,
so grows
your plug in mass
storage system.**

Our new universal controller system is completely modular.

As many as eight data storage devices (or as few as one) can be operated from a single controller. You can actually expand your system's memory capacity from 8 million to 5 billion characters. Economically. Quickly. With one simple plug that links it to just about any computer made.

And there are lots of other features calculated to turn you on. For example, the system operates in several different modes—both serial and parallel—with word transfer rates from 50 microseconds to 900 nanoseconds per word. To and from two computer central processors. You can even add a comprehensive software package that includes generalized flow diagrams and detailed machine language programs.

Drop us a line. Ex-Cell-O Corporation, Bryant Computer Products, 850 Ladd Rd., Walled Lake, Michigan 48088. We bet our "Bryant Believer" philosophy will grow on you.

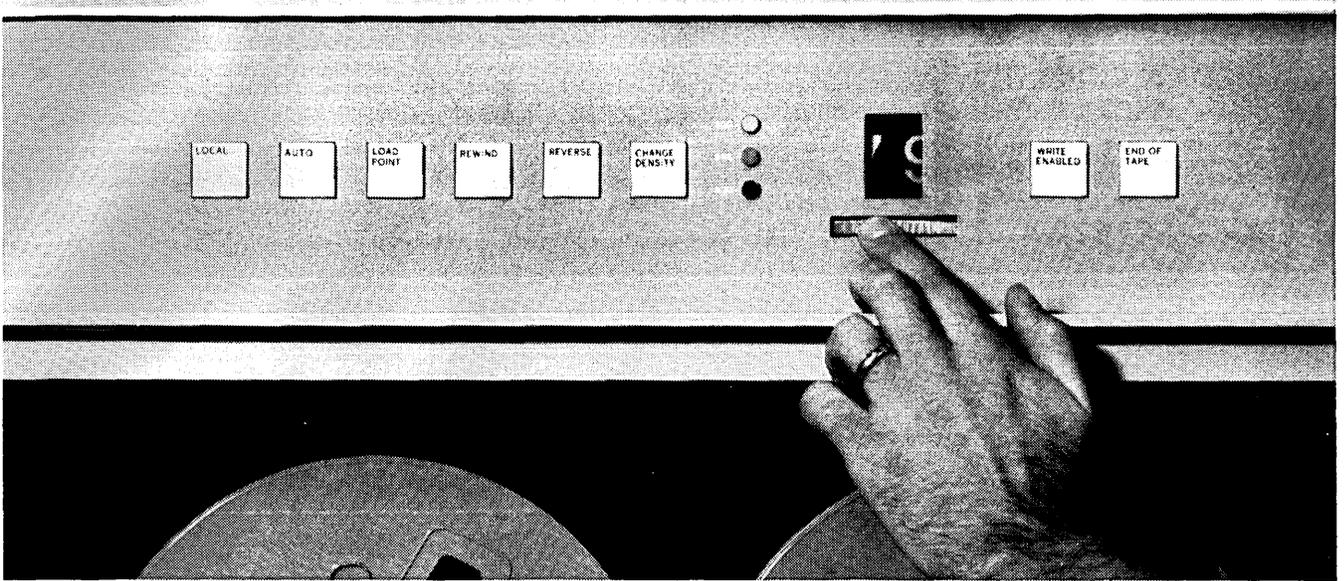


PhD-340
plug-in Positioning
Head Drum System

**BRYANT
COMPUTER PRODUCTS**



CIRCLE NO. 12 ON INQUIRY CARD



**Reading both
7 and 9 track
digital tapes?**

**Change
tape formats
with one
finger**

A single tape unit that reads both of the industry-standard digital tape recording formats—with format selection at the flip of a switch. You no longer need *two* tape units for those installations processing computer-written tapes; include a Hewlett-Packard READ/READ Tape Unit that will read *both*.

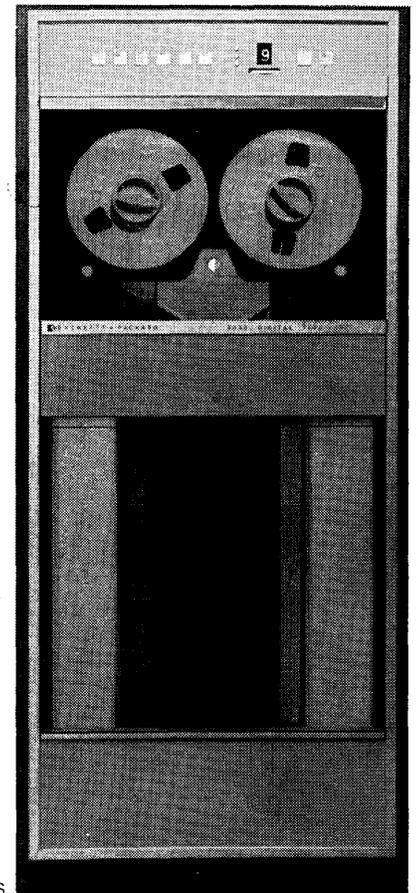
Think of the savings this offers in the design and production of *your* digital system—and the flexibility you'll be able to offer the *user*.

Your choice of tape units for READ/READ operation may be either the 3030 Series with tape speeds to 75 ips, or the 2020 Series offering the optimum in economy of tape speeds below 45 ips.

Other tape units in the 2020 and 3030 Series class offer single-format capabilities for both writing and reading.

Whatever your application, the flexibility of Hewlett-Packard's 2020 or 3030 Series Digital Magnetic Tape Units can provide a tape unit with the optimum configuration to interface to *your* digital system.

For more details, call your local HP field engineer or write Hewlett-Packard, 690 Middlefield Road, Mountain View, California 94040.



HEWLETT  PACKARD

MAGNETIC RECORDERS

3030 SERIES

42708

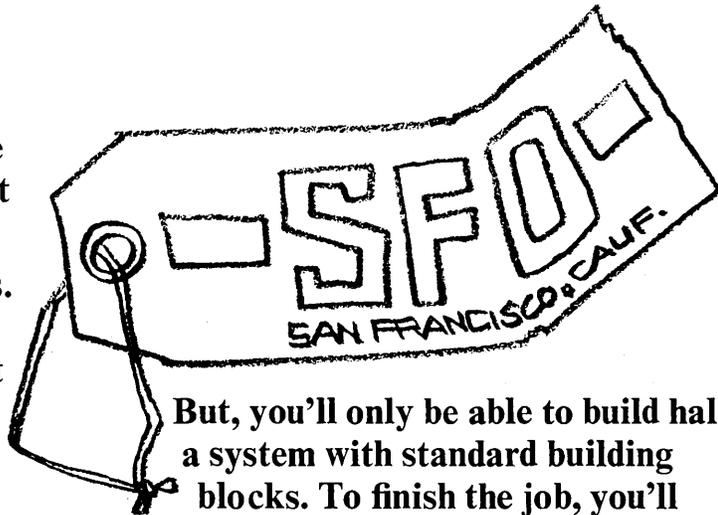
CIRCLE NO. 13 ON INQUIRY CARD

Do you want to go LSI now?

If you really want LSI now, grab the next plane to Mountain View. (It lands in San Francisco.) It's the quickest, least expensive way to get LSI into your system.

Plan to bring along your blueprints. And be ready to answer a lot of questions. We'll need to know what you have in mind for sub-systems, functions and specs. And, don't be surprised when we ask "why" a couple of times. It's all part of Fairchild's systems approach to complex circuitry.

We'll take your requirements and match them against our family of fundamental building blocks. We've got LSIs (and MSIs) that work in any digital logic system. The most advanced circuitry on the market. Offspring of computer-aided design and double-layer metal technology. And, they're all so versatile, we can probably give you a counter that has a dozen other applications in your system.



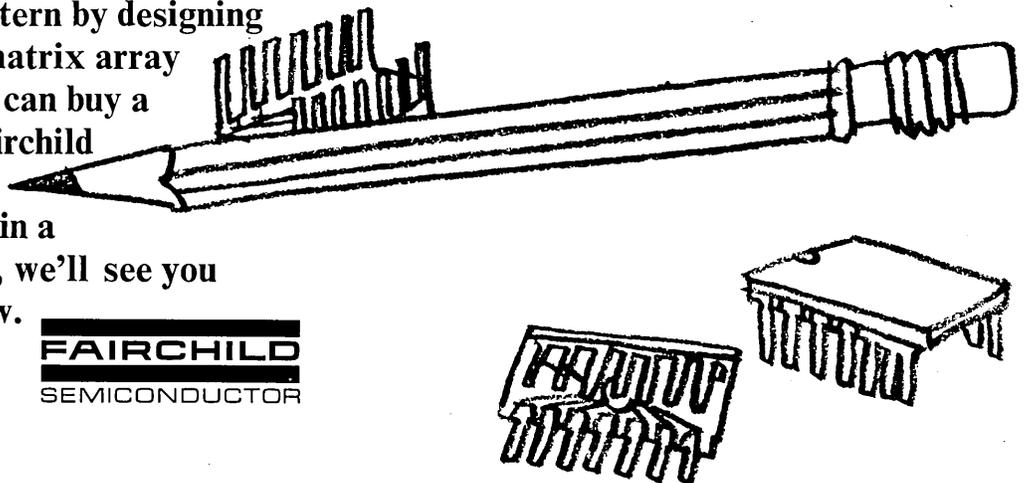
But, you'll only be able to build half a system with standard building blocks. To finish the job, you'll need interface devices to tie the whole thing together. And, here's where Fairchild can really save you time and money. We don't have to custom design each LSI interface circuit. We use Micromatrix™—a unique cellular array that's completed when we add your specific interconnection pattern. Your specs customize the entire array for your system.

Of course, there's a lot more to the story. But, you ought to hear it in person. Just call your Fairchild salesman. He knows the flight schedule to San Francisco.

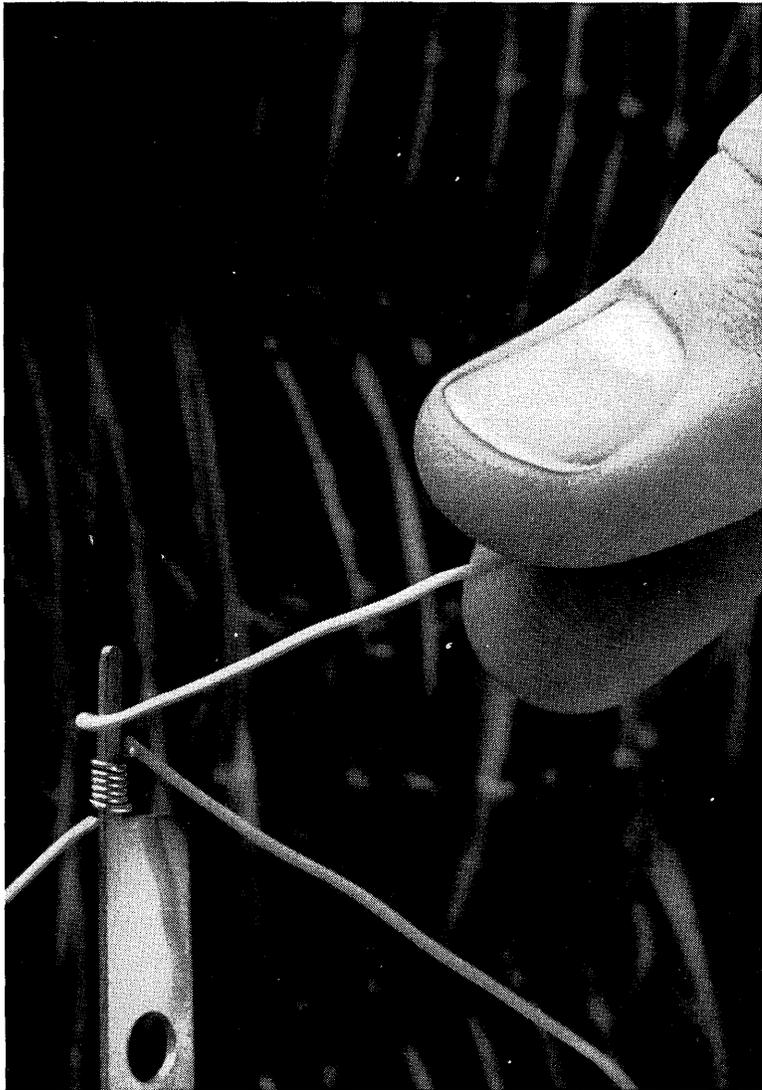
Or do you want to think about it?

We've got an LSI design kit. It's based on our new 4500 Bipolar Micromatrix Array—the first device in a highly versatile LSI family. The 4500 is an eight-cell array that can be customized for virtually any function. All it needs is your interconnection pattern. You can determine the pattern by designing your own Micromatrix array with our kit. You can buy a kit from your Fairchild distributor for about \$100. And, in a couple of months, we'll see you in Mountain View.

FAIRCHILD
SEMICONDUCTOR



30-gage wire can't have much insulation



**It's got
to be tough**

**That's why
it's Kynar[®]**

Kynar has superior cut-through and abrasion resistance . . . double the mechanical strength of other fluoroplastic insulations. It withstands bending . . . vibration . . . resists cleaning solvents . . . operates from -80° to 300°F . . . feeds, cuts and strips smoothly in hand and automatic wiring machines.

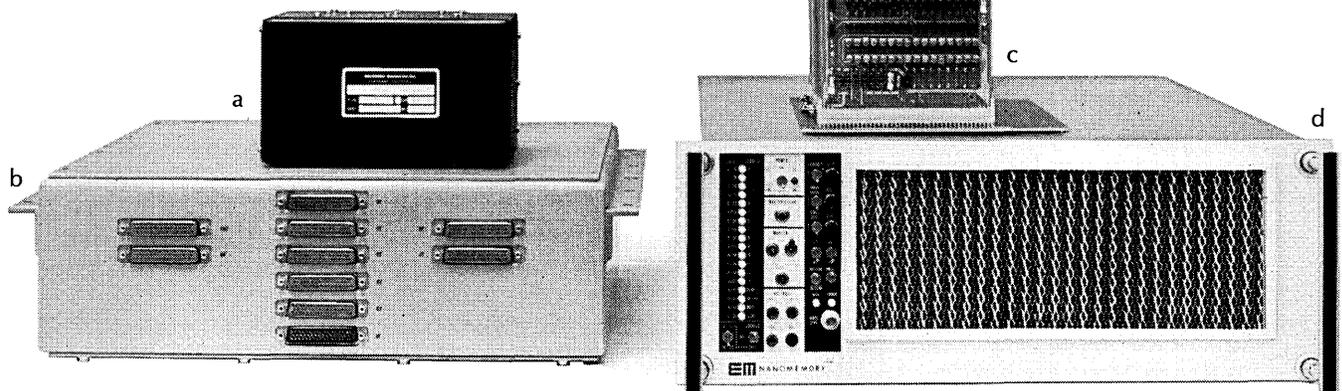
Wire insulated with Kynar is available from leading manufacturers. For data, write or call Plastics Department, Pennsalt Chemicals Corporation, 3 Penn Center, Philadelphia, Pa. 19102.

Kynar...the fluoroplastic that's tough!



two hawks

two doves



These two military and two commercial memories round out the broadest system line in the industry. Whatever your environmental requirement, we have a system to meet it. And we have it available right now.

There are other advantages in letting us build your system. The design techniques we've mastered for our military memories have been adapted for our commercial devices. You get the benefit of features like pluggable stacks and electronics for easier maintenance, integrated circuits for increased reliability, and space-saving design concepts.

Brief specs are listed below, but

for the full story write to Electronic Memories, Inc., 12621 Chadron Avenue, Hawthorne, California 90250.

(a) SEMS 5—Designed for airborne applications, the SEMS 5 has a 2 microsecond cycle time, packs 131,062 bits into only 132 cubic inches and meets applicable portions of MIL-E-5400, MIL-E-4158, and MIL-E-16400.

(b) SEMS 7—Developed for ground based applications, this rugged memory has a 2 microsecond cycle time, a 327,680 bit storage capacity and meets applicable portions of MIL-E-4158, MIL-E-16400 and SCL-6200.

(c) MICROMEMORY™ 1000—Taking up

only 400 cubic inches, the 1000 features a 32,768 bit capacity and a 2.5 microsecond cycle time. It uses a unique 3D drive configuration permitting a particularly low component count, with correspondingly high MTBF, and a price less than 10 cents per bit in small quantities.

(d) NANOMEMORY™ 2000 SERIES—Combining integrated circuit electronics and a unique 2½D drive system, the 2000 Series has a 294,902 bit capacity, cycle times of either 650 or 900 nanoseconds, and a configuration measuring only 21.5 inches deep by 19 inches wide by 7 inches high, including power supply and optional tester.

EM electronic memories

See our complete systems line at SJCC Booth Z1-Z3.

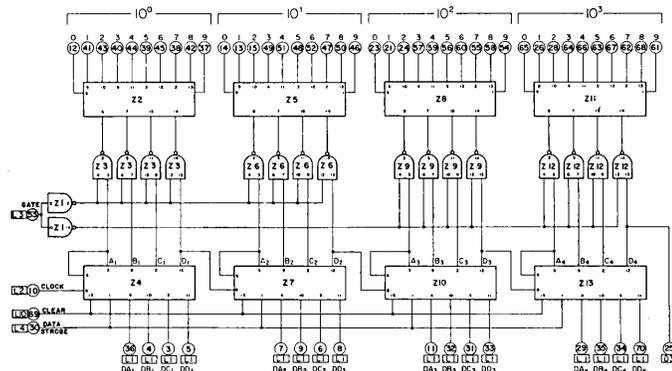
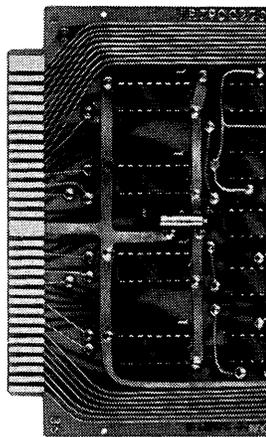
CIRCLE NO. 16 ON INQUIRY CARD

We have something for no-nonsense design engineers

who want to make
the best investment
in IC logic assemblies.

Design with CAMBION® IC Logic Assemblies. You get more for your money . . . more functions on every logic card . . . an exclusive 70-pin input/output that lets you bring more functions through to the outside world.

With this unique connector capability, we've developed both standard and those hard-to-find cards . . . grey code logic, arithmetic logic, counters, decoders, registers, comparators . . . all the odd-ball assemblies you need. Look at these advantages:



SPEED — IC logic assemblies with speeds to 25 MHz.

NOISE — Exact component location with precision etched interconnections achieve “short-leads” and prevent signal cross-coupling. BCD counters with decoder/Nixie* drivers all on a single card are but one example.

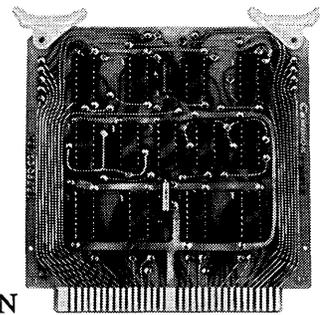
PACKAGE DENSITIES — 70-pin input/output, plus a great array of complex functions and you've got what it takes for high-density packages. (You use fewer cards this way, too.)

VARIETY — Over 250 card types for difficult applications.

DELIVERY — Immediate . . . from stock . . . honestly.

DOCUMENTATION — CAMBION's new logic manual has the data, including application and helpful reference formulas.

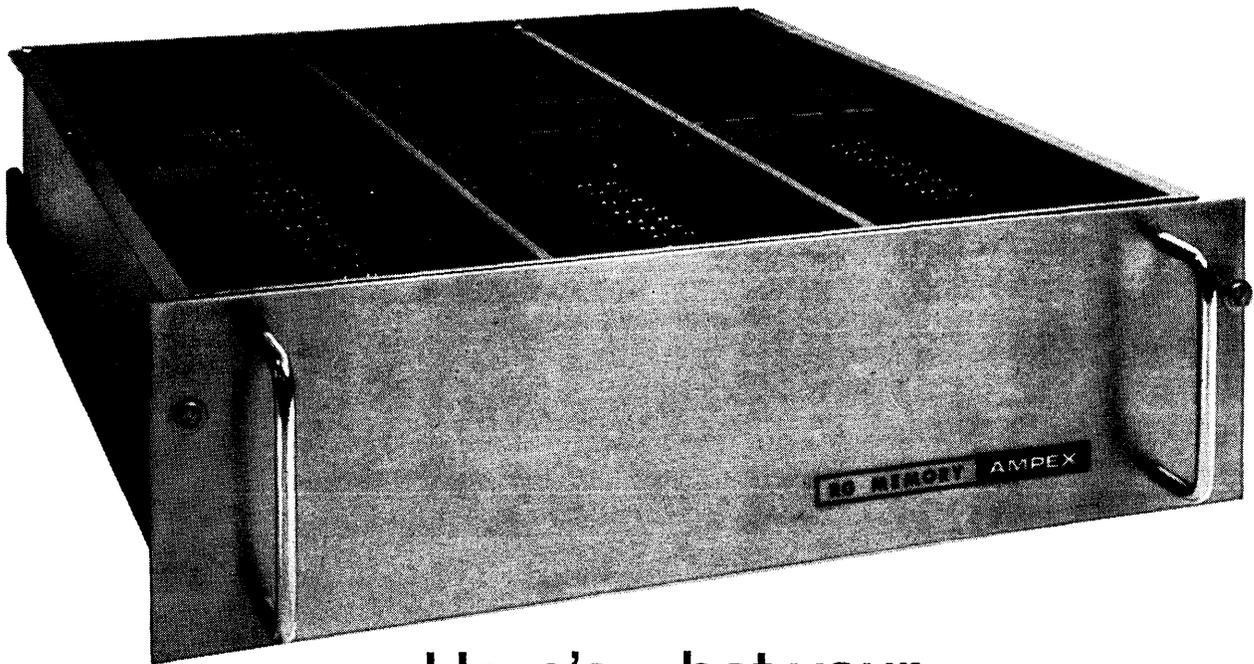
NO-NONSENSE — Make the best investment in IC logic assemblies. Call or write Cambridge Thermionic Corporation, 453 Concord Avenue, Cambridge, Massachusetts 02138. Phone: (617) 491-5400. In Los Angeles, 8703 La Tijera Boulevard. Phone: (213) 776-0472.



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*Trademark, Burroughs Corp.

CAMBRIDGE THERMIONIC CORPORATION
CAMBION®

Standardize on CAMBION . . . the guaranteed logic assemblies

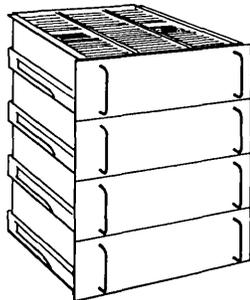


Here's what your computer can do with the **NEW AMPEX RG MEMORY**

1. Access data in 350 nanoseconds
2. Expand in modules to 5 million bits
3. Sell for less

When you're outlining the requirements of your new computer or system, pause a moment and consider what our new RG core memory offers: 350 nsec access; 900 nsec full cycle time; integrated circuitry; and expansion from a 4K memory all the way to 64K by addition of modules.

We think you'll want to design these features into your next system. The RG is low in cost, too. You pay less for the RG; your customers pay less for your system.



ALSO NEW FOR 512-TO-4096 WORD TASKS —THE RF-4 CORE MEMORY

This new, high-speed core memory, similar to our RF-1 memory, is built on one large PC board and is capable of word lengths to 20 bits. It uses integrated circuitry and gives you high speed (1 microsecond cycle time) at low cost.

Check the specs. If they serve your purpose, please drop us a line, or circle the Reader Card number. We would like to send

you our literature about these new workhorse memories. We'll even tell you how little they cost.

IMPORTANT SPECS		
	RG	RF-4
Access time	350 nsec	400 nsec
Full cycle	900 nsec	1000 nsec (half cycle: 650 nsec)
Size (inches)	5¼ x 19 x 21 (per memory module)	5¼ x 19 x 21 (including power supply)
Capacity:	4096; 8192; 12,228; or 16,384 words, expandable in modules to 65,536 words	512 to 4096 words
Word length:	24 to 80 bits	4 to 20 bits

Ampex at S.J.C.C.

See the RG, RF-4 and a new core memory with a 750 nanosecond cycle time in the Ampex booth at Spring Joint Computer Conference at Atlantic City, N.J., April 30-May 2. Also see the latest in cores, stacks and tape transports.

AMPEX

CIRCLE NO. 18 ON INQUIRY CARD

IS YOUR "COMPUTER-COMPATIBLE" DIGITAL INCREMENTAL MAGNETIC TAPE RECORDER REALLY COMPATIBLE WITH YOUR COMPUTER?



To assure full computer-compatibility, CALMA's new family of incremental recorders is equipped with a unique CBD (Constant Bit Density) controller to maintain character spacing variations within the specifications of the major computer manufacturers. In addition, electronic de-skewing is employed in our high-density recorders to control the alignment of bits within each character.

To eliminate a troublesome source of electrical noise (a cause of data errors in recording devices), CALMA has replaced the traditional electromechanical reel servo relays with an all-solid-state control circuit.

For automatic collection of digital data from telephone and Teletype lines, investigate our Model 220 Digital Data

Interface / Recorder. This new system features automatic IRG-generation and sophisticated noise discrimination to reduce the effects of transient noise commonly encountered on communication channels. Write, phone, or circle our number on the reader service card for a comprehensive description of the new CALMA family* of incremental recorders.

CALMA
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* Model 200-200bpi, 7-track, 0.500cps, computer-compatible Model 600-556bpi, 7-track, 0.500cps, computer-compatible
Model 800-800bpi, 9-track, 0.500cps, internal CRCC generation, SYSTEM/360-compatible



How do you measure a ^{MINI} computer?

Not by ordinary means. Here are some new dimensions:

- Hardware: designed for the IC generation, not adapted to it.
- Speed: 1.8 μ s memory cycle time; 3.9 μ s add time on Model 4, 35 μ s on Model 3.
- Interrupts: priority system for up to 256 devices; status and device number obtained without polling.
- Addressability: directly to 65, 536 bytes of core memory with indexing; no paging required.
- Arithmetic: 16 general registers for arithmetic operations; optional hardware multiply/divide and floating point instructions.
- Data Transfer: direct to memory a byte or block at a time; cycle stealing access to memory by byte or halfword.
- Peripherals: selected for reliability and performance; quality conversion equipment and system modules.
- Expandability: in the field and upward between models; our measurements are modular.
- Interface: inter-connecting logic components for do-it-yourself systems with minimal engineering.
- Software: assembler, program diagnostics, math library; plus the new dimension of interactive FORTRAN.
- Repertoire: over 70 instructions common to all processors; no reprogramming between models.
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- Compatibility: a family of processors to choose from; peripherals and system modules connect to any processor.

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CIRCLE NO. 20 ON INQUIRY CARD

American Micro-systems, Inc. introduces low voltage MOS devices compatible with DTL/TTL

+5 VOLT SUPPLY LMOS

Dual 50-bit register RD12D features: Direct interfacing with DTL or TTL circuits Very low power—10 mW at 1 MHz Low clock levels—minimal clock drive circuits. For further information on RD12D or other low voltage (**LMOS**) circuits, call for application information or request data sheets.



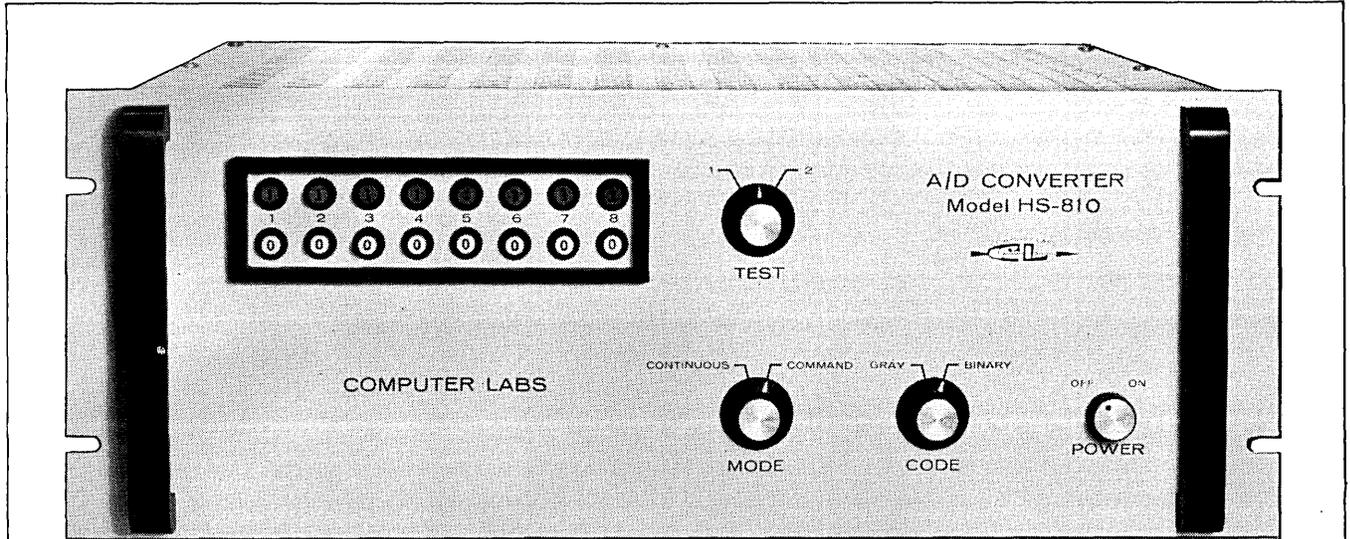
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CIRCLE NO. 21 ON INQUIRY CARD

13 is lucky...

when it's the number of A/D Converters
in the world's fastest line

All with Internal sample-and-hold and power supply.



HS-810 A/D Converter 8-bit Conversion at 10MHz

BITS	MODEL NO.	WORD RATE (MAX.)	APERTURE	WEIGHT OF LSB.	ACCURACY	ANALOG BW FOR RATED ACCURACY	MAX. ANALOG BANDWIDTH	PRICE
4	HS-425	25 MHz	1.0 ns	128 mv	64 mv	12.5 MHz	15 MHz	\$5800
4	HS-406	6 MHz	3.0 ns	128 mv	64 mv	3 MHz	5 MHz	\$4200
5	HS-520	20 MHz	0.8 ns	64 mv	32 mv	10 MHz	15 MHz	\$6400
5	HS-505	5 MHz	2.5 ns	64 mv	32 mv	2.5 MHz	5 MHz	\$4800
6	HS-615	15 MHz	0.6 ns	32 mv	16 mv	7.5 MHz	15 MHz	\$7490
6	HS-604	4 MHz	2.0 ns	32 mv	16 mv	2 MHz	5 MHz	\$5500
7	HS-710	10 MHz	0.4 ns	16 mv	8 mv	5 MHz	15 MHz	\$7950
7	HS-703	3 MHz	1.5 ns	16 mv	8 mv	1.5 MHz	5 MHz	\$5900
8	HS-810	10 MHz	0.4 ns	8 mv	4 mv	5 MHz	10 MHz	\$8750
8	HS-808	8 MHz	0.35 ns	8 mv	4 mv	4 MHz	10 MHz	\$8650
8	HS-802	2 MHz	1.0 ns	8 mv	4 mv	1 MHz	3 MHz	\$6400
9	HS-905	5 MHz	0.2 ns	4 mv	2 mv	2.5 MHz	10 MHz	\$9660
9	HS-901	1 MHz	0.5 ns	4 mv	2 mv	0.5 MHz	3 MHz	\$6800



That isn't all...

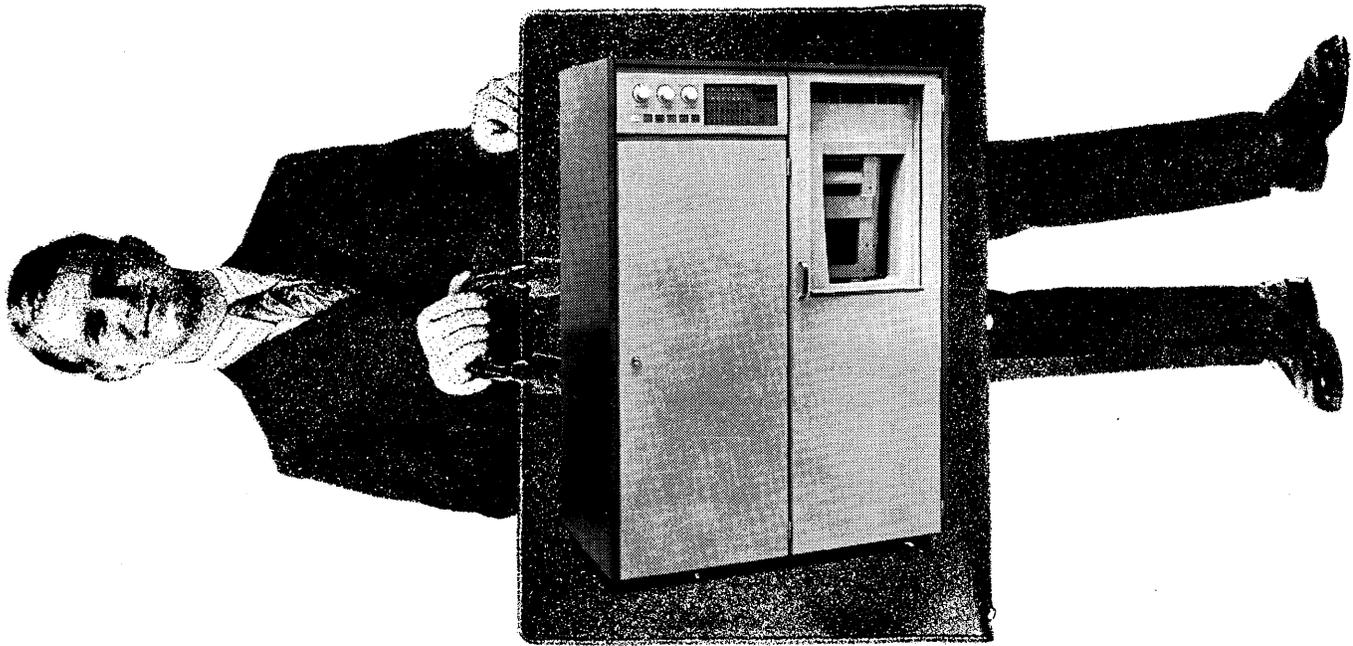
We are always improving and adding to our product line. If you have special problems or need other ideas, call us.

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The Peripheral People announce the availability of CRAM 5 (a 580 million bit, 90 to 150 ms retrieval Card Random Access Memory)



They all laughed when we sat down and developed CRAM. Now we announce our third generation, available for OEM sales. Our competitors are still trying to solve the problems of their first born.

Now, instead of 112 million bits, you can store more than five times as many and find your data 1/10th of a second faster.

With a single controller, you can hook up 16 of the new CRAM 5 units to accommodate over nine billion bits. And don't forget, you can change a cartridge in 30 seconds. We have lots of electro-mechanical experience so you know we know how to make it work. And keep on working. Quickly. Accurately. Inexpensively. Reliably. Well.

N C R

**The
Peripheral
People** 
Card Readers, Tape Punches, Tape
Readers, Printers, MICR Readers,
CRAM (Card Random Access Memory)

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CIRCLE NO. 23 ON INQUIRY CARD

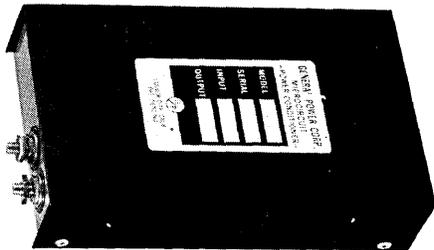
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OF THESE UNITS!**

**MAKES ALL DC POWER
SUPPLIES OBSOLETE!**

PKG. SIZE—1-3/16" H, 3-1/4" W, 5-3/16" L
WEIGHS Approximately 19 Ounces



10 AMPERE SERIES

CONTROL YOURSELF AND READ ON!

Series	POWER-CURRENT	SIZE (Inches) (Height—Width—Length)
PD1	20W. or 4A. max.	1-3/16 x 3-1/4 x 4-3/16
PD2	50W. or 10A. max.	1-3/16 x 3-1/4 x 5-3/16
PD3	100W. or 20A. max.	2 x 4 x 6
PD4	250W. or 50A. max.	2-3/8 x 6 x 9
PD5	500W. or 100A. max.	2-3/8 x 6 x 9
PD? Special Unit Price and Delivery Information Available on Request.		

HOLD ON; YOU'RE ALMOST THERE—

SPECIFICATIONS

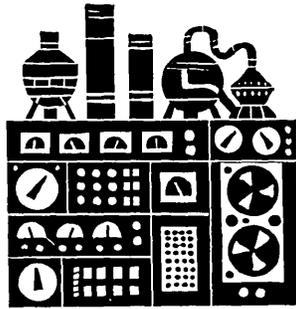
- INPUT: 105-125V, 47 — 1600 Hz.
- REGULATION: \pm 1% MAXIMUM deviation for line change and/or 10% to 100% load change.
- RIPPLE: 1% PP maximum across the output terminals.
- POLARITY: Can be used + or —, case ground floating.
- PROTECTION: Overvoltage.
- TEMPERATURE: 71°C MAX. at the mounting base.
- ISOLATION: The input to output is transformer isolated.

CONGRATULATIONS — YOU MADE IT! NOW RUN RIGHT DOWN TO YOUR FRIENDLY PURCHASING DEPARTMENT AND ORDER A HANDFUL. YOU MAY BE THE FIRST MEMBER OF YOUR GROUP TO ORDER A MICROCIRCUIT D.C. POWER CONDITIONER — BUT YOU WON'T BE THE LAST!

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CIRCLE NO. 24 ON INQUIRY CARD



INDUSTRY NEWS

DECTAPE, DECDISC AVAILABLE TO ALL—Digital Equipment Corporation today announced it will market two of its most popular mass storage devices as separate units. Included is their DECTape, priced at \$2,300 and their DECDisc at \$3,000. Formerly, the company would sell these devices only to users of PDP computers. According to a company spokesman, this change in marketing policy was made in response to many requests from system designers who desired to obtain inexpensive mass storage for newly designed computer systems, and other data handling systems which may not necessarily include a computer. Also, this permits the popular DEC components to be added to existing computer installations, regardless of their lineage.

\$3 MILLION SATELLITE COMMUNICATIONS AWARD—General Telephone & Electronics recently announced receipt of a \$3-million Air Force award for satellite communications equipment which will provide multiple access capability to ground terminals. The contract to design, develop, and construct electronic equipment which will allow many ground, shipboard, and airborne stations to communicate simultaneously via satellite was awarded to Sylvania Electric Products Inc., a GT&E subsidiary, by the Electronic Systems Division of the Air Force Systems Command, Hanscom Field, Massachusetts.

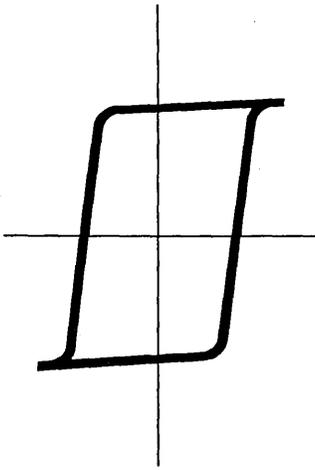
AIR FORCE AWARD TO STUDY COMMUNICATIONS ERROR REDUCTION—Sylvania Electric Products Inc. announced recently receipt of an Air Force Contract to study methods of reducing error between transmission and reception of data communications. Various information feedback techniques with full duplex operation will be investigated during the 15-month effort, according to a company spokesman. By means of a feedback channel,

the receiver can ask the transmitter to repeat only that portion of the message that was in error, eliminating the need for re-transmitting the entire communication. The objective is to achieve maximum use of radio channels despite the presence of noise, the major hindrance to such communications.

IRISH COMPUTER BUREAU SERVES U.S. AND EUROPE—Computer Bureau (Shannon) has installed a Honeywell 120 computer system to improve its capacity as an international keypunch center and to establish itself as a computer service bureau for Ireland. The company was formed in 1963 as a key-punching center where documents flown in from the United States could be processed and flown back in the form of punched cards or magnetic tapes. The bureau recently joined University Computing Company of Dallas, Tex., which operates ten computer centers in the United States and sends its data preparation work to Shannon.

Trans-Atlantic jet service offers 24-hour service to the Dallas firm and to its American customers. Charges for the service, including air freight, are less than they would be if the material were processed in the United States.

COMPUTER EQUIPMENT ANALYSIS—IBM Product Test engineers have devised a television system that displays and measures the operation of high-speed computer parts in slow-motion or in stop-action. Normally, movement of fast moving mechanical parts is checked by studying high-speed movies of the part in operation. The new system is said to replace this method partly by allowing engineers to see slow motion operation of repetitive mechanical actions immediately, rather than waiting for motion picture processing. Currently, it is being used to analyze moving parts in printers and other computer equipment. The system is said to combine



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That's what Datacraft Corporation engineers into each memory, whether it's an off-the-shelf 512 x 8 unit or a custom designed 65536 x 32 system.

The model DC-31 for example, is a high speed, linear select, coincident-current, magnetic core memory especially suited for systems requiring small high speed units. It comes with a full complement of field proven options that enable the customer to select a custom system at minimum expense.

The basic DC-31 features include: less than one microsecond full cycle time; 450 nanosecond access time; capacities up to 1024 x 12 in one bit per word increments; 30 days delivery. Prices start at \$1210.

For detailed specifications on the DC-31 and information on other models, call (305) 565-9441 now, or write

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the advantages of television, immediate playback and low recording costs, with the advantage of stroboscopic lighting techniques that are equivalent to a high speed camera with a shutter speed of 1/200,000 of a second.

MULTI-MILLION \$ CONTRACT —

One of the largest purchase contracts in the computer peripheral equipment industry has been awarded to Memorex Corporation for the purchase of Peripheral Systems 630 disc drive units by Management Assistance Inc., (MAI). According to Robert M. Brumbaugh, President of Memorex subsidiary Peripheral Systems Corporation (PSC) of Sunnyvale, California, the contract is a 5-year phased program, potentially valued at 20-million dollars within 3 years. The largest single purchase contract in Memorex history; it is estimated to exceed 4 million dollars in 1968. Initial deliveries of the equipment, under development since 1966 by PSC, were in March and will scale up to an annual rate of 500 units in early 1969. MAI will place the equipment on lease with lessees of its IBM Series 360 computer systems as replacements for IBM 2311 disc drives otherwise employed by MAI customers.

NEW SMALL COMPUTER — Scientific Control Corporation announced that the SCC 2700 digital computer has been added to their product line. The unit will be unveiled at the Spring Joint Computer Conference. The SCC 2700 is said to represent a completely new approach to the small computer field. Because of its utilization of the most advanced concepts and techniques, the manufacturer claims the computer presents the user a cost-performance ratio that cannot be matched by any other machine of its class.

MISSILE COMPUTER CONTRACT

—Burroughs Corporation has received a \$10.2 million contract to supply computer systems for the U.S. Army's Pershing 1-A Missile System. Under the terms of the contract, Burroughs Defense, Space and Special Systems Group will provide the Martin-Marietta Corporation's Orlando Division with D84 integrated circuit computers. The D84 computer, a compact, rugged, high-speed, electronic data processing system, performs precountdown,

countdown, missile readiness and guidance calculations which are essential for the quick reaction capability of the missile system. The Pershing 1-A, a 400-mile-range ballistic missile, provides the Army with a supersonic nuclear deterrent against aggression in the field.

COMPUTER COMPLETES 37,000 HOURS NON-STOP OPERATION

—At Brookhaven National Laboratory an SDS 910 computer has been running almost non-stop 24 hours a day, seven days a week for just over 37,000 hours. This machine, used by the neutron physics group, is located in the Reactor Experimental Area and controls two real-time neutron physics experiments at Brookhaven's High Flux Beam Reactor.

NEW COMPUTER — A new dual-memory, multi-lingual data processing system said to offer scientists and engineers ultra-high-speed and memory capacity at medium prices has been announced by Standard Computer Corporation of Los Angeles, Cal. A company executive said the new IC-4000 employs an exclusive dual-level programming technique which facilitates the mixing of machine-language routines with micro-programmed routines in separate control memories. Utilizing this dual-level programming approach Standard produced a high-efficiency Fortran compiler. These new developments in the IC-4000 are said to reduce job turnaround times by greatly increasing compiling and execution speeds. First deliveries are scheduled for August of 1968. The IC-4000 hardware has a large main memory, 36-bit word parallel operations, an overlapped control memory and a wide selection of card, printer, tape and disk devices.

MICROBE IDENTIFYING LASER/COMPUTER

—A new technique which could provide instant and unique identification of human tissue types and microbes with little or no laboratory preparation is now under development at Optics Technology, Inc., Palo Alto, California.

The identification methods now in use, i.e., throat cultures, biopsies, and other routine laboratory studies, require hours and sometimes days before positive results can be obtained. The new technique, called biophosphor-analysis, employs a laser light source and a small digital

computer to accomplish the same result in minutes, saving both valuable diagnostic time and the extensive laboratory facilities now required.

The new method uses ultraviolet light, produced by a laser, to irradiate a sample that has been taken directly from the body. No special preparation is required, other than cooling the sample to very low temperature. Under these conditions, the cell structure itself produces phosphorescent radiation. When the laser is turned off this phosphorescence dies away. A highly compact computer monitors the rate at which the phosphorescence decays and by matching this information to previously stored data is capable of identifying the presence of specific microorganisms or tissues.

NCR UNVEILS NEW CENTURY SERIES COMPUTERS — Minimum sales target is 5,000 systems. The National Cash Register Company today staked a claim for a substantially larger share of the total computer market as the company introduced worldwide a major new family of data processing systems. A company official said NCR expects to install a minimum of 5,000 of its new Century series computers. This initial sales target represents a total value of over a billion dollars worth of the new equipment.

"The introduction of this advanced new computer family is the third and by far the most significant step in the company's long-term program to win a sizable share of the huge electronic data processing market," the official said. The Century program represents an investment of \$150 million in research, engineering, software, new production facilities and equipment, and in training of marketing and service personnel.

HONEYWELL ANNOUNCES RUGGEDIZED COMPUTER — Honeywell's Computer Control Division has announced a ruggedized version of its DDP-516 integrated circuit computer designed to provide the advantages of commercial computers for military users. The ruggedized DDP-516 can be used for aircraft, shipboard and van-mounted applications where full military specifications are not required. An electromagnetic interference (EMI) suppressed model with or without ruggedization is also available. Modified DDP-516's are said to have

the advantages of the standard commercial models including software, options, low price, rapid delivery, service support and proven design, and meet the more severe requirements of military, marine and other users.

REAL-TIME SYSTEM PLOTS 2 YEARS OF PSD IN ONE DAY — A new real-time power spectral density system which can operate on-line was announced recently by Federal Scientific Corporation. The Model PSD-7C Ubiquitous® Power Spectral Density System processes

noise or vibration data as it occurs. It operates in 1/500th the time of conventional sweeping analysis systems without the need for time-consuming tape loops. 500 days or two years of analysis can thus be processed in one day. In analyzing tape data, the system can be used first to monitor the data to select the sections of interest, and then perform PSD analysis in the minimum possible time. Additional modifications allow plotting of complex cross-PSD and System Transfer Function, as well as Auto- and Cross-Correlation, all in real time. Price is approximately \$40,000.

Ticket Printers and Terminals Now Operating OLRT

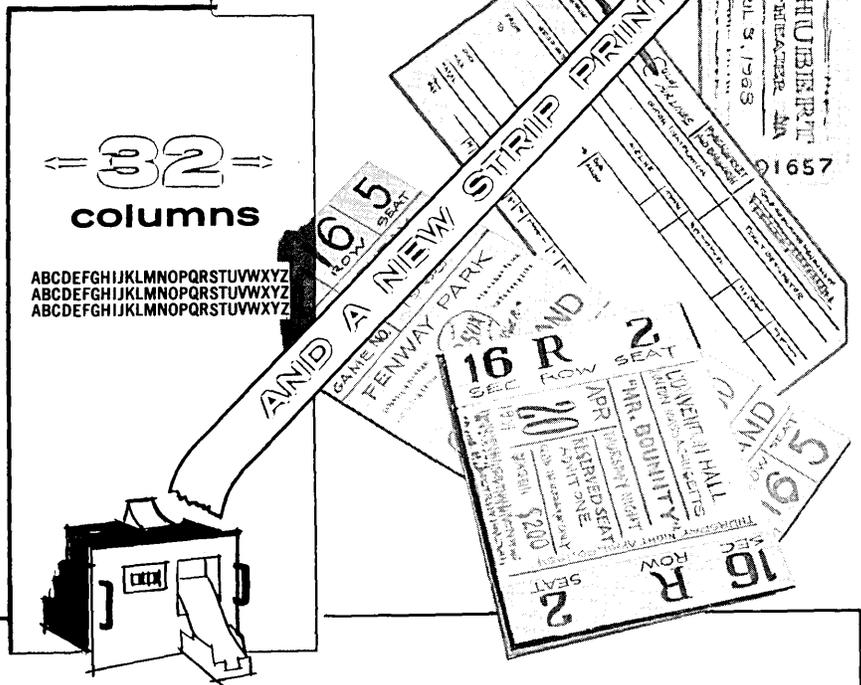


Di/An is the first to offer terminals for on-site printing of tickets and reservations. The keyboard talks to the computer — the computer talks back via the ticket printer. For AIRLINES, THEATERS, SPORTS EVENTS — more to come.

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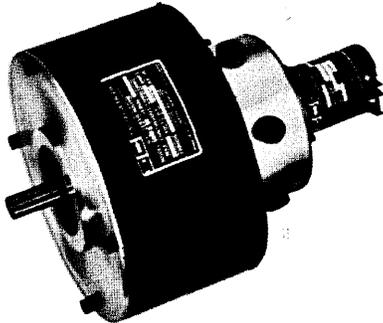
Our standard alphanumeric Lister/Printers and Data Loggers are available in from four- to thirty-two-column models, which have output rates as high as forty lines per second. Moreover, data can be listed vertically or horizontally along the length of the paper. We call that versatility.

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■ Electro-Craft offers a wide choice of MOTOMATIC® MCM low inertia, ultra high performance, dc servo motors and compatible driving amplifiers, available either as a complete package or as separate modules.

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■ MOTOMATIC® MCM, moving coil motors feature; acceleration in excess of 10^5 rad/sec.², time constant of 2m-sec., high pulse torque, extremely low inductance, high efficiency, long-life and integral feedback tach-generator.

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WRIGHT LINE TO MARKET HONEYWELL DISK PACKS — Wright Line, Division of Barry Wright Corporation has signed a contract with Honeywell, Inc., whereby Wright Line will purchase for resale under its own name \$3.5 million dollars worth of computer data storage disk packs over a two year period beginning in April, 1968. The agreement calls for Wright Line to market Honeywell's Model M4005 disk pack under the Wright Line label. As other disk pack models are developed and produced by Honeywell, Wright Line will also have the right to market them under their own label. The M4005 Disk Pack is a stack of six fourteen inch disks and will store up to 9.2 million characters of information. It is the first consumable computer supply item manufactured by Honeywell's recently formed Special Products Division.

TEN YEARS WORK IN HALF HOUR — Hughes' Flexible Automatic Circuit Tester ("FACT"), is reported to require only thirty minutes instead of ten man-years by human hand to test computerized defense systems. "FACT" is said to inspect in half an hour the 40,000 electrical termination pins found in large circuit panels of modern computerized defense apparatus. In comparison, it would take a work force of 28,000 to accomplish the same task in similar time.

NEW GROUP TO PROVIDE COMPUTER MANAGEMENT EDUCATION — Computer Sciences Corporation has formed a major new organization known as Computer Sciences Institute. The Institute, it is reported, will serve industry, government, the military and the public education markets through the development of complete education systems and by providing managerial, professional and technical training in the information sciences, and will also undertake contract research for these markets. A CSC executive said the new organization will help to reverse one of the prime drains on corporate profits today: the inefficient management of costly computer resources by executives inadequately trained in their utilization and control.

The three areas of service of Computer Sciences Institute are:

1. Education in computer concepts and techniques for top and middle management and advanced technical training for data processing personnel.
2. Development of complete education systems in schools and for occupational training in technical fields, such as electronics assembly.
3. Contract research into planning and functional problems of business and government.

Computer Sciences Corporation, the parent company, provides advanced programming, computer systems design, management consulting, and related services to industry, science and government.

Norman H. Carter has been named vice president and general manager of Computer Sciences Institute. Carter formerly was vice president for Corporate Planning and Research at Union Bank, Los Angeles. Earlier, he was associated with Lockheed Aircraft Corporation where he directed the design and development of Lockheed's Automatic Data Acquisition system one of the largest and most complex real-time management control systems yet developed for industry.

He is the author of **Introduction to Business Data Processing**, a text

He is the author of *Introduction to Business Data Processing*, a text published by Dickinson in 1968, and of numerous lectures and articles on the subject.

"Never before has management committed so many millions of dollars for equipment it knows so little about," Carter says. "The computer is misunderstood and misutilized in many organizations, although it may be the tool which will enable management to survive the growing squeeze on profits."

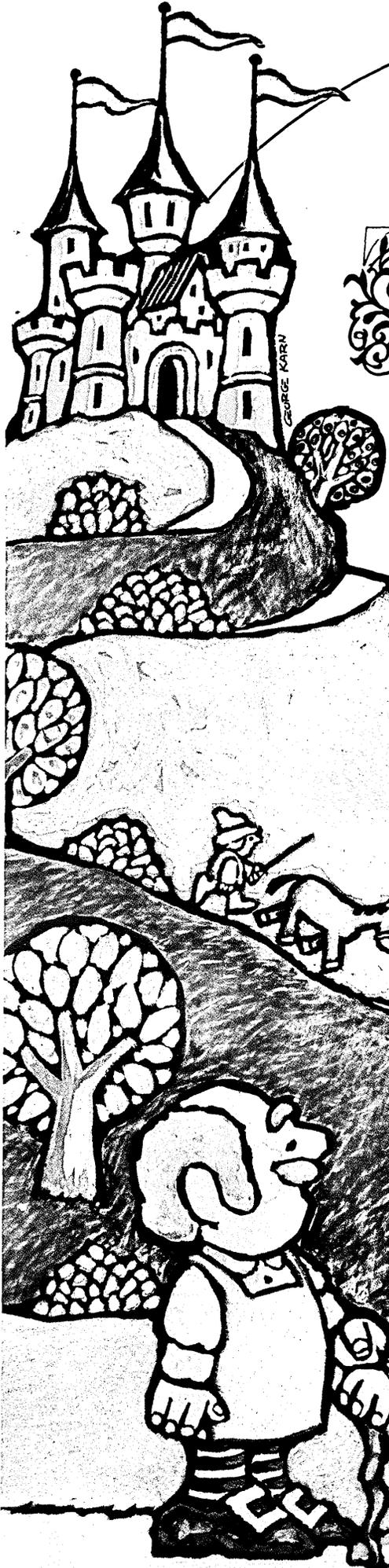
The Institute says its integrated approach to computer education is designed to replace orientation courses now available, which either try to turn executives into computer programmers or stop at the theoretical level.

Carter said the Computer Sciences Institute training systems represent an advance over any courses now available and are unique in that they employ the Structured Learning Technique developed by the Institute and copyrighted by it.

A structured follow-up program will be offered to keep executives updated after they return to their jobs.

Computer Sciences Corporation has 2,100 professionals on its staff of

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COMPUTER DESIGN/APRIL 1968



GEORGE KARN



The House on Memory Mountain

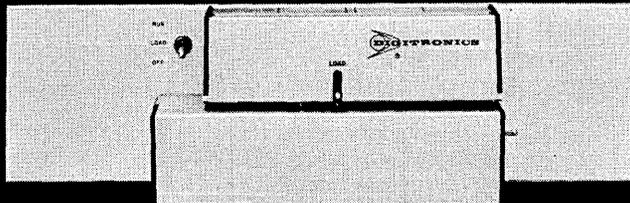
You've been looking around for some help in designing your memory system. You want peak technology and manufacturing. Look up. The House on Memory Mountain is open for inspection.

Inside, you'll find virtually no limit to variety and range of product. Small, slow core buffer memories. Large mass core memories with up to 20 million bit capacity. Then there are core memory stacks. And magnetic thin film systems with a cycle time of 300 nanoseconds. Just for examples.

If this were a story, its moral would be: computer manufacturers write to Bob Rife at our home office. He has a mountain of information of how Fabri-Tek can help you come out on top.

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Over 10,000 readers and handlers, over three generations, over seven years of experience in high-speed photo-electric reading have been blended with the latest technology to create a fourth generation tape reader which offers more performance per dollar than any other in today's market.

- Speedup more than 25%
- Pricedown more than 10%
- Electrical Adjustmentsdown from 10 to 1
- Read amplifier adjustmentseliminated
- Interface costscut more than 50%
- Parts countdown 25%

These are just a few of the milestones achieved by the Model 2540 Perforated Tape Reader.

The Model 2540 operates at slow speeds up to 400 characters per second, or can be stepped asynchronously at up to 150 characters per second. The unique modular design of the Model 2540 affords increased versatility. The basic 2540 starts out as an unidirectional or bidirectional tape transport with I/C logic compatible read head. This basic configuration may be expanded by adding the following: (1) an electronics unit, containing I/C data and sprocket amplifiers and drive controls circuits; (2) a power supply, which provides dc operating power for the electronics unit and drive mechanism; and (3) a rack adapter, which permits the 10-inch wide 2540 to be mounted in a 19-inch RETMA rack.

For complete information, and the most detailed data sheet in the industry today, contact your nearest Digitronics representative (he's listed in EEM or EBG) or write Digitronics Corporation, Albertson, N.Y. 11507. (516) 484-1000.

 **DIGITRONICS**

when every bit counts
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3,000 people. The knowledge of these experts in numerous computer applications is being drawn upon for course development, and they also will be available to back up the Institute's staff in training assignments.

DIGITAL EQUIPMENT CORP. OFFERS LEASING AGREEMENT — A leasing agreement offering schools a 4096-word general purpose computer, Teletype and software at a cost as low as \$450 per month was announced today by Digital Equipment Corporation.

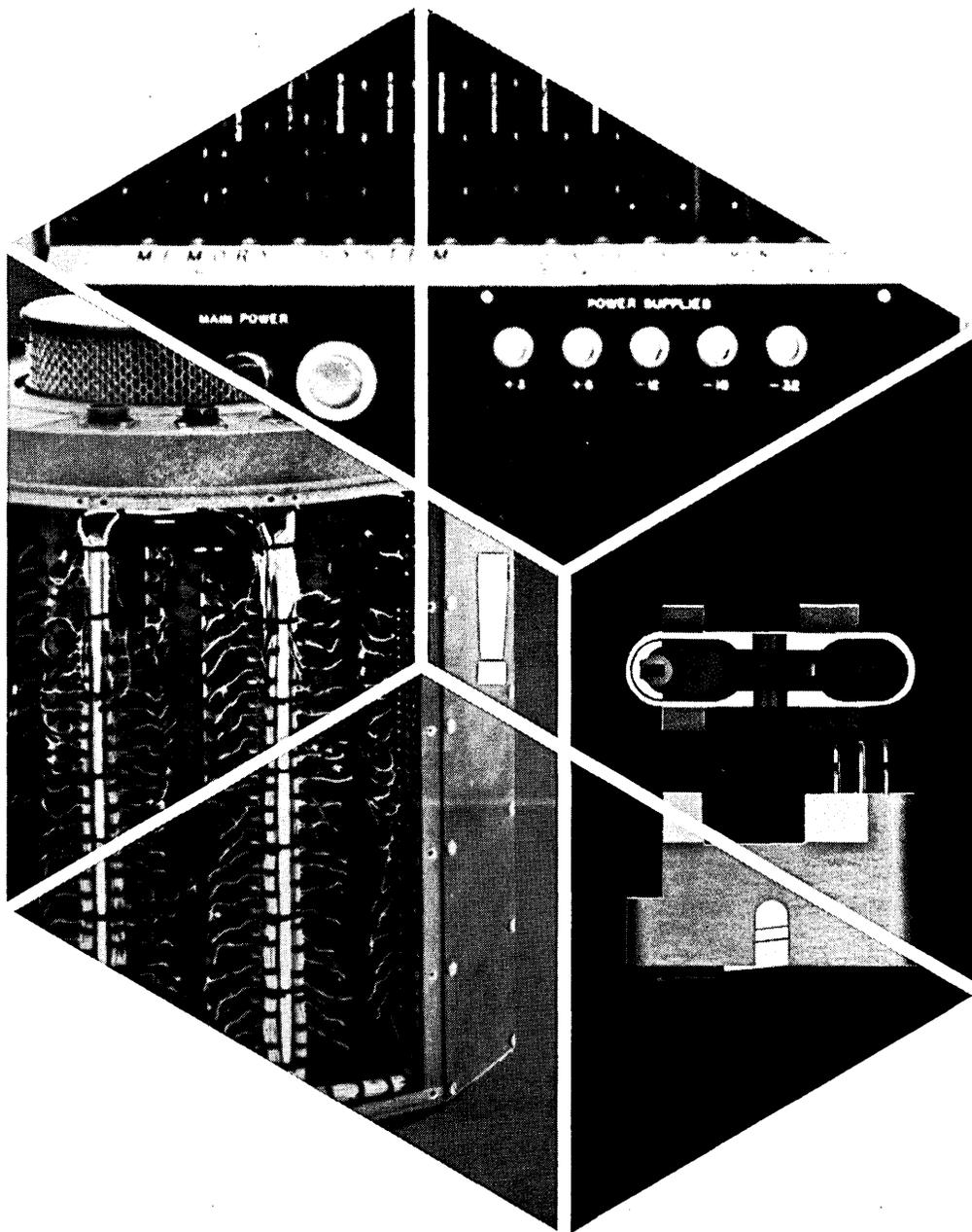
The heart of the system is a PDP-8/S computer which is being used in more than 1,000 installations. About 70 of Digital's computers are installed in high schools, university education and psychology departments, medical schools and technical/vocational schools throughout this country and Canada.

The \$450 charge is figured on a 39-month plan and includes purchase option credits. The term can be extended after expiration at a reduced rate. Four basic configurations are being offered by Digital; however, schools may tailor special systems to fit their needs. Extra memory, mass storage devices, paper tape readers and punches, displays, analog to digital converters and a data communications interface also may be leased. The same basic configuration and peripheral equipment is available on a 12-month plan.

Up to now, Digital has sold their equipment outright. The move to leasing was part of the company's developing commitment to provide the educational market with proper hardware and easily usable software for instructional purposes.

CONTROL DATA CANADA, LTD. OPENS NEW DATA CENTRE —

A subsidiary of Control Data Corporation, CDC, LTD. has opened a data processing service centre in Ottawa, Canada. In announcing the new Data Centre, a company official said this first expansion into Canada of the company's extensive information processing service brings a new level of computer availability to Canadian firms and institutions. The Ottawa Data Centre soon will have direct access to a CONTROL DATA 6600, which is scheduled to be installed at the Boston Data Centre sometime this year. The 6600 computer is capable of performing approximately three million operations per second.



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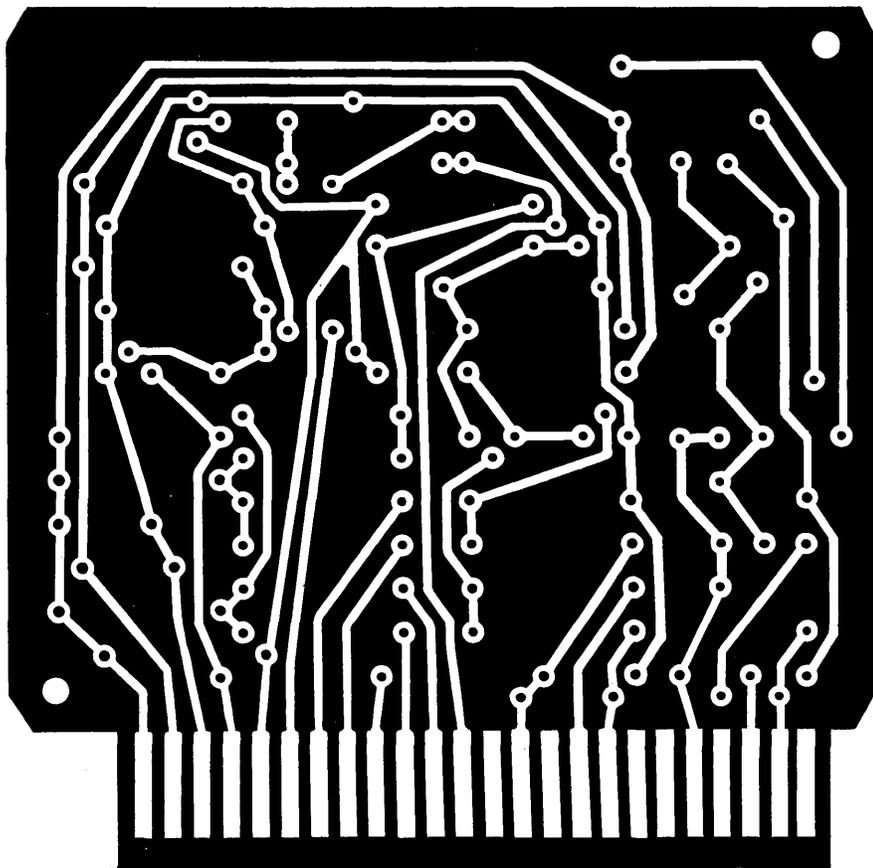


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COMPUTER TO INSURE WORLD PEACE THROUGH WORLD LAW?

— It would be a step in the right direction if the World Peace through Law Center in Geneva gets what it wants. The legal group, world-wide in scope, comprises thousands of jurists from over 100 nations. Their goal is to build a computerized library of legal precedent on which countries could settle their disputes. The lawyers hope to store the legal codes of every nation, and by so doing, have access to needed references by key-work codes within 15 seconds.

NEW DATA PROCESSING LINE

— A broad line of new data processing instrumentation devices will be introduced by Raytheon Company at the Spring Joint Computer Conference in Atlantic City (April 30-May 2, 1968). The instruments employ Raytheon's M-Series integrated circuit modules assembled in different configurations expanding the company's 703 IC computer systems. An operating data acquisition and processing system demonstrating the capability and performance of the new products will be featured in the Raytheon Computer exhibit (Booths 501-503). Included in the new line are analog-to-digital converters, digital-to-analog converters and the company's exclusive Miniverter.

The Miniverter is available in a 10 or 12-bit binary version plus a 13-bit BCD version. Number of channels is expandable from 16 to 256 and throughput rate of any configuration is 50 KHz.

Complete information on the new products is available at the Raytheon booth (501-503) or from Raytheon Computer, 2700 South Fairview Street, Santa Ana, Calif. 92704. (Telephone (714) 546-7160).

COMPUTER DIAGNOSES MOTORS' MALADIES

— Computers are doing everything these days — they're even checking government cars for mechanical defects at the Atomic Energy Commission's Hanford plant in Southeastern Washington State. And it doesn't take long, according to a recent report, just 90 seconds for the computer to check a vehicle's cranking, distributor, ignition and charging systems and cylinder efficiency under load. If any defects are found in any of these systems the vehicle is scheduled for repair, and the quality and practical data processing of the repair work will be rechecked later by the computer. The

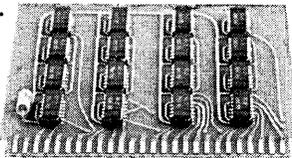


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AEC contractor charged with the responsibility of maintaining these vehicles, in addition to providing a multitude of other specialized support services at the giant nuclear installation, is ITT Federal Support Services Inc., a subsidiary of International Telephone and Telegraph Corporation.

TRW INSTALLS 940 TIME-SHARING COMPUTER—An SDS 940 time-sharing computer has been installed at the Software and Computing Center of TRW Systems Group, Redondo Beach, Calif., to augment the on-line computing facilities available to TRW technical personnel. Initially, 45 Teletype terminals throughout the Systems Group of TRW will have access to the SDS 940.

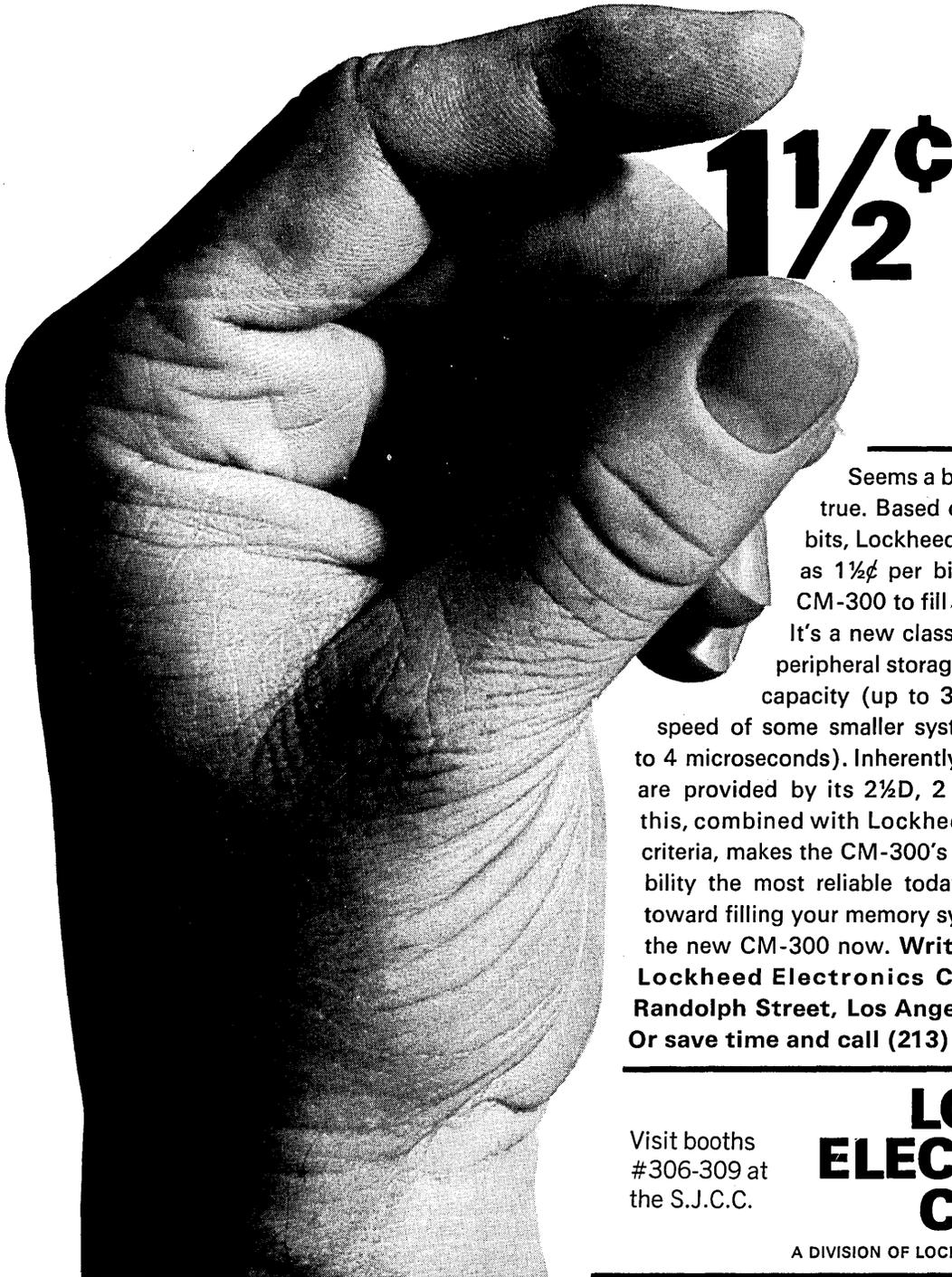
The system will be used for solving, by two-way conversation with the computer, immediate problems in spacecraft structure analysis, heat transfer, fluid dynamics, electronic circuit design, orbit determination, drawing and layout detail verification, aerosciences laboratory research, computer-aided design, bids and proposals, and other applications.

The time-sharing computer includes 64 words of core memory, two two-million character Rapid Access Data (RAD) files, a 65-million character disc file, two magnetic tape units, paper tape reader and punch, card reader, card punch, line printer and keyboard printer.

NEW COMPUTER SYSTEMS CORPORATION—The concept of "distributed data processing", stemming from programs developed for the U.S. Air Force, is the reason for being of a new company, Viatron Computer Systems Corporation of Burlington, Massachusetts. Organized by over a dozen key scientists from the Mitre Corporation and top-level marketing and manufacturing people from firms in the data processing industry, Viatron will direct its efforts to commercial utilization of distributed data processing systems and equipment.

In essence, distributed data processing provides maximum flexibility at multiple locations without multi-user dependence on a complex computer. In time-sharing systems, "non-thinking" peripheral equipment communicates with a large, central computer. In distributed data processing, low-cost programmed equipment permits highly economical data processing in a range of commercial applications.

Lockheed's new bulk-capacity memory system costs just a little bit a bit.



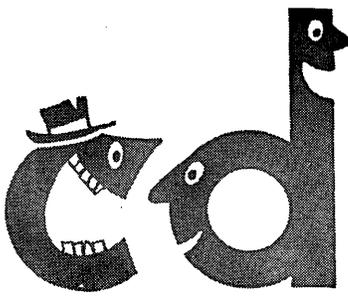
1 1/2¢

Seems a bit hard to believe, but it's true. Based on 1 million words at 32 bits, Lockheed's CM-300 costs as little as 1 1/2¢ per bit. □ Lockheed built the CM-300 to fill the memory system gap. It's a new class of random access, EDP peripheral storage system. It couples bulk capacity (up to 32 million bits) with the speed of some smaller systems (full cycle time—2 to 4 microseconds). Inherently high operating margins are provided by its 2 1/2D, 2 wire organization. And this, combined with Lockheed's worst-case design criteria, makes the CM-300's peripheral storage capability the most reliable today. □ Take the first step toward filling your memory system gap. Inquire about the new CM-300 now. Write: Memory Products, Lockheed Electronics Company, 6201 East Randolph Street, Los Angeles, California 90022. Or save time and call (213) 722-6810.

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commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

HOW TO GET STARTED IN COMPUTER GRAPHICS

Cathode Ray Tubes have been available on many computers for a number of years, and in some applications, they are beginning to see fairly wide use. A basic division can be drawn between displays capable of presenting alphanumeric information only, and those which are capable of presenting graphical information as well. The former are the type of displays that are beginning to be used widely as inquiry stations for airline reservations, insurance companies, banking systems, and in other information retrieval applications. Since a well established market, significant operating experience, and a fairly obvious line of development exists for these devices, they will not be considered further in this commentary. Attention will be devoted to the exciting, and I believe much more far reaching, possibilities of graphic displays.

Computer Graphics

Since the demonstration of sketch pads in 1962, the use of a cathode ray tube display on a computer has stirred the imagination of mechanical engineers, architects, draftsmen, educators, and others concerned with the presentation and manipulation of pictorial information. The dramatic possibilities of a drawing that can be constructed dynamically with a light pen and then modified, repeated, expanded or contracted, developed into three dimensions, and simultaneously subjected to precise computational analysis is something that has fascinated computer users everywhere. One imagines a mechanical engineer, while shaving one morning, having a brilliant idea for a new differential mechanism for the automobile he is designing. An hour later at the office, he sits in front of a CRT display console and sketches the arrangement of gears and linkages with his light pen. Rotation of

The author of this month's CD Commentary, Dr. C.B. Newport, is Manager of the Information Systems Department at Honeywell, Computer Control Division. He is responsible for communication control, scientific control and display and applications in the General Systems section.

the drive shaft on the drawing indicates a few problems he had overlooked (the wheels rotate in opposite directions), but this is soon rectified by moving the gears and adding an extra idler. The computer is requested to undertake stress calculations on the housing, develop the detailed profile of the gear tooth, and determine the total weight of the system. The system is not quite as desired, but a few deft modifications with the light pen eventually produce a design that satisfies the engineer as being close enough to the optimum. The computer is then requested to produce the numerical control tapes for the machines that will manufacture the parts, and to produce the required assembly drawings on a plotting table.

The N-C tapes are then passed to the production control organization for scheduling through the machine shop, and two days later, the designer has an assembled prototype ready for testing.

The attraction of such a system is enormous. The designer at the CRT console has at his fingertips a graphic modelling tool which allows him to develop and perfect his idea, and then check it with the resources of a powerful computer. Even more important, the full manufacturing information is produced automatically. The designer does not have to explain his idea to a draftsman and the draftsman does not have to translate his understanding of the idea into instructions for a machine operator only to discover, some weeks later, that the prototype is not quite what the designer intended. The major part of the fallible human communication link from idea to the final hardware realization has been eliminated by the computer graphics system, and the designer is sure that his idea has been converted accurately into hardware. If it does not work, it is his fault alone. The potential speed and ease with which *ideas* can be converted into *objects* is, I believe, the major reason for believing that there is a revolutionary future ahead for computer graphics.

Theory to Practice

The practical realization of these techniques is, however, many years ahead, and sober consideration needs to be given to the tedious, mundane, and difficult

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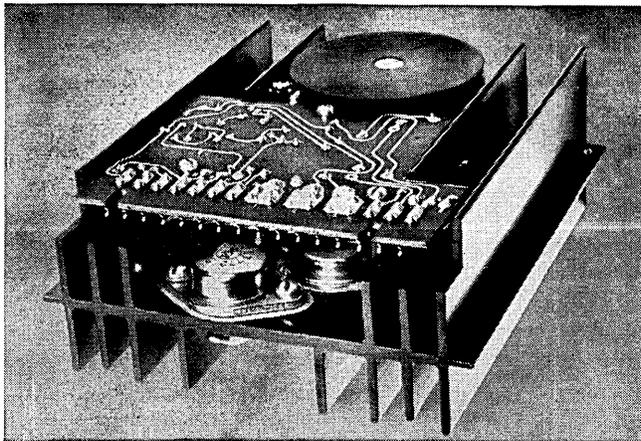
Add-on power capability by using more modules?

?

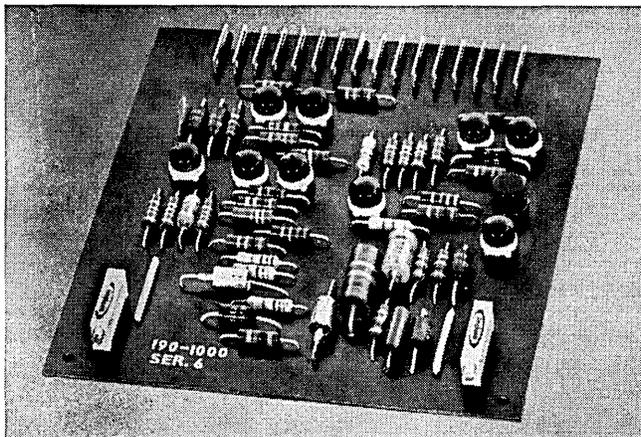
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Output can be regulated between ± 2 and ± 60 dc at up to 20 amperes using the OMNIMOD family of modules WITHOUT MODIFICATION OR ADJUSTMENT. Higher current ratings are obtained by paralleling power control modules.

Any number of power controller modules can be controlled by one amplifier. OMNIMOD has a current limiting parameter, over voltage protection, voltage sequencing, and remote sensing.

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2. select the number of plug-in OMNIMOD power control modules to supply the power needed for each output

3. package these elements with filter capacitors and a plug-in amplifier module for each output

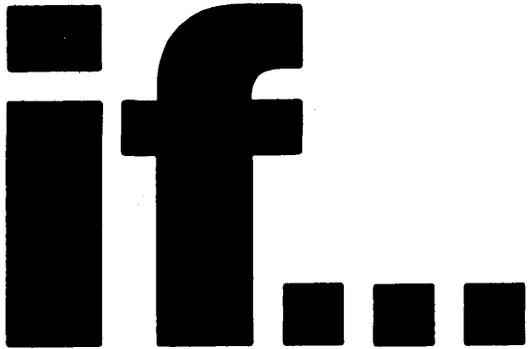
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steps which must be taken to achieve the goal. It is necessary that those involved, particularly at management levels, have a good understanding of what can and cannot be done. Potential users of sophisticated systems, as well as manufacturers, tend to go through a series of oscillations before stabilizing on a realistic course.

Glowing reports of possibilities (as described above) tend to lead the partially informed observer to believe that computer graphics will have the solution to every problem by about this time next year. However, next year and many thousands of dollars later, when the proud programmers and system designers demonstrate that they can draw and manipulate lines, circles, and squares on a cathode ray tube, management may see little future for such a "simple" facility and complain that the system is no more than a programmer's toy. At that stage, disillusionment can set in and the idea that computer graphics can do everything may wane into a feeling that computer graphics are impractical. Perseverance will eventually reveal that computer graphics can do a great deal, but it is not going to be easy.

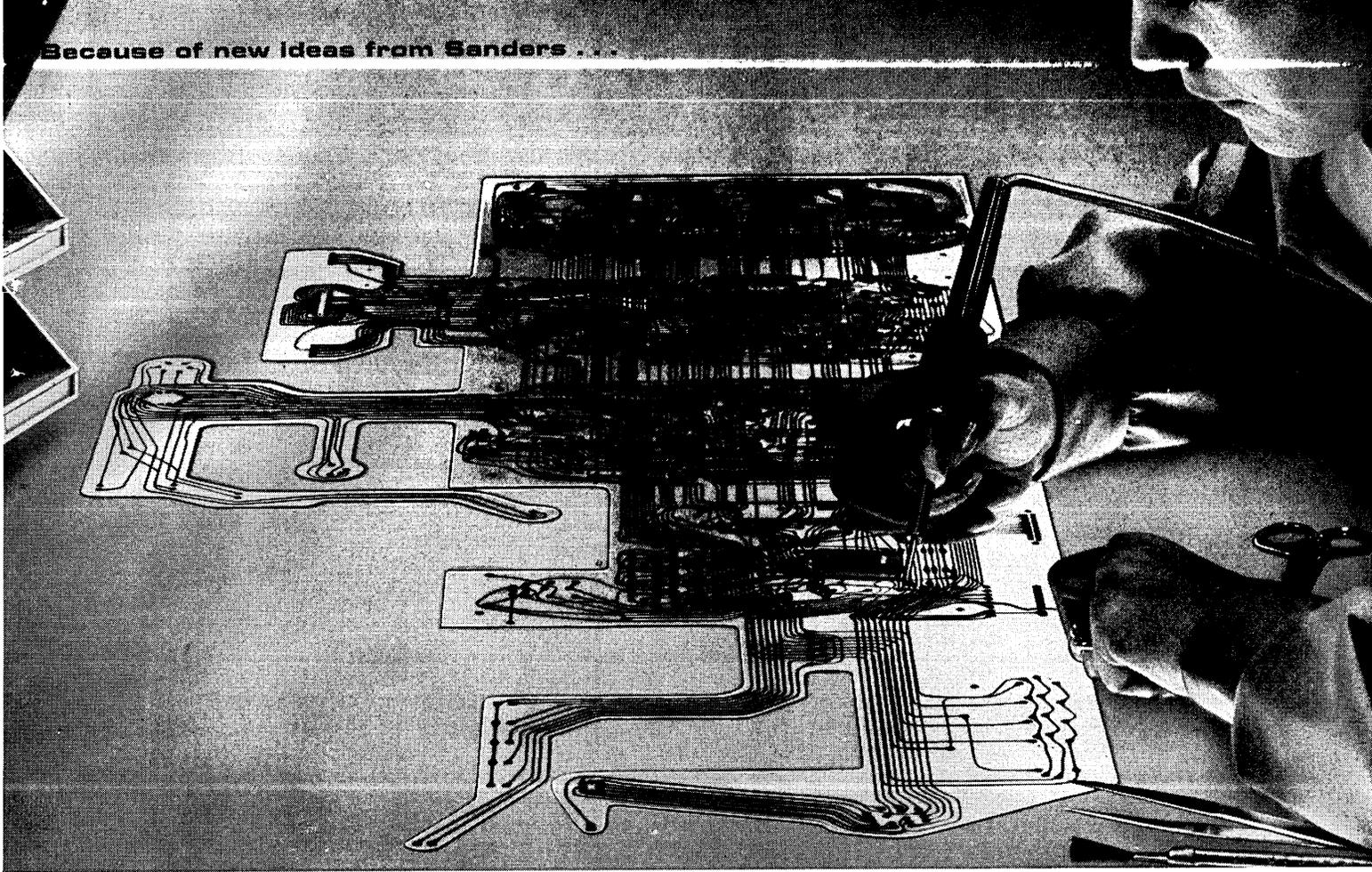
The Route to Success

This presumptuous subtitle will serve to introduce a few ideas about how a potentially successful computer graphics application for replacing a conventional drawing system might be chosen.

Some organizations, particularly government sponsored laboratories, the aerospace industry, and a few large commercial organizations have invested millions of dollars in big time-sharing computers and huge programming teams to obtain an operating computer graphics system for some particular application. Such systems have already demonstrated success, or partial success, and have laid the groundwork for future developments. Notable among these are the systems developed at MIT, Lockheed-Georgia, Bell, General Motors, and in-house systems developed by IBM. However, it is doubtful that any of these projects can really prove that they are paying their way, and are therefore appropriate for wide-scale use. There are many organizations that can see the potential of computer graphics and would be interested in investing a limited amount of money in a small scale project for which the prime aim is to demonstrate the economic feasibility of such a system.

A more gradual approach toward development of a fully effective system is very attractive. Limited investment for limited capability (with the possibility of future expansion) will result in many more graphics users, and hence more over-all experience, than large investment with the promise of extensive facilities.

To demonstrate a viable system, it is necessary to choose the application very carefully. Many possible applications spring to mind, such as the design of mechanical parts (as described above), the design of electrical circuits, the design of buildings, the layout and the checking of logic block diagrams, and possibly the teaching of scientific subjects to children. The proof of economic viability is essential, and the considerations which go towards making a valid choice of applications include:



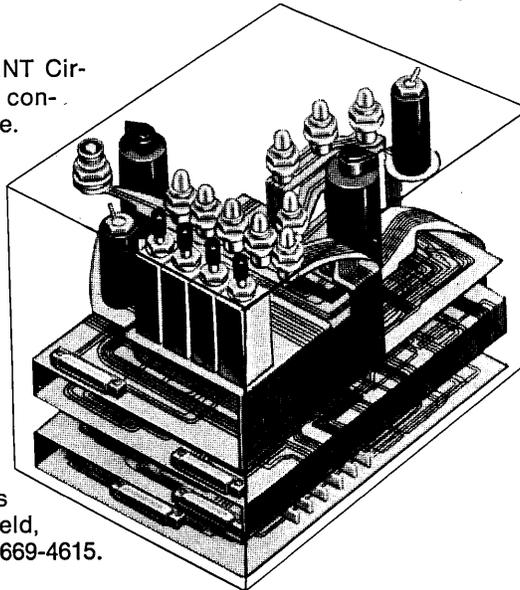
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This new two-layer FLEXMAX circuit is made from high-temperature material, providing excellent inherent dimensional stability. This insures constant electrical and mechanical characteristics over a wide environmental range.

This typical example of a FLEXMAX circuit fits in a package 8" x 10" x 4" high. In the flat form, its dimensions are 40" long x 17" wide. Approximately 200 components can be mounted on the circuit.

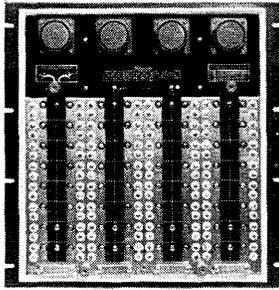
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New Directions
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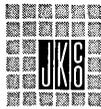
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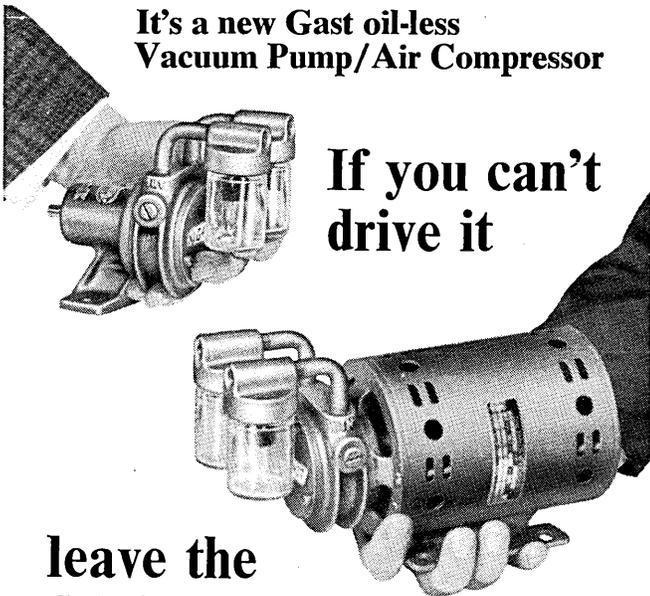
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1. The task should be simple and clearly defined.
2. It should include the potential of increasing the output of one man by a large factor (perhaps 5 or 10 times).
3. It should aim to take over tedious routine work, and not attempt to provide "creative" assistance to the user.
4. It should provide simple but important work other than drawings. For instance, the making of parts lists and schedules.
5. CRT quality drawings should be acceptable to the user. Present-day CRTs do not produce drawings having the same pictorial quality as a typical engineering drawing. (They do, however, in their digital representation, have considerably greater accuracy.)
6. The drawings should be basically two-dimensional with possible simple excursions into the third dimension.
7. The drawing system should be viable without requiring a large computer and extensive software to undertake elaborate back-up calculations.
8. The drawings should be capable of being built up quickly from a small number of predefined objects.
9. The system should be capable of being used by a number of people in quick succession (and eventually simultaneously), since most drawing tends to be about 20% actual drawing and 80% thinking and discussing.
10. The application should be one that occurs widely in, essentially, identical forms so that the software cost can be spread over a number of installations.

The above considerations point to simple drafting applications as being the most appropriate, particularly when a simple layout drawing specifies the requirements completely, but extensive detailed drawing is needed to get the equipment manufactured. It is important that the task chosen be the simplest possible one that has a good opportunity of demonstrating economic viability.

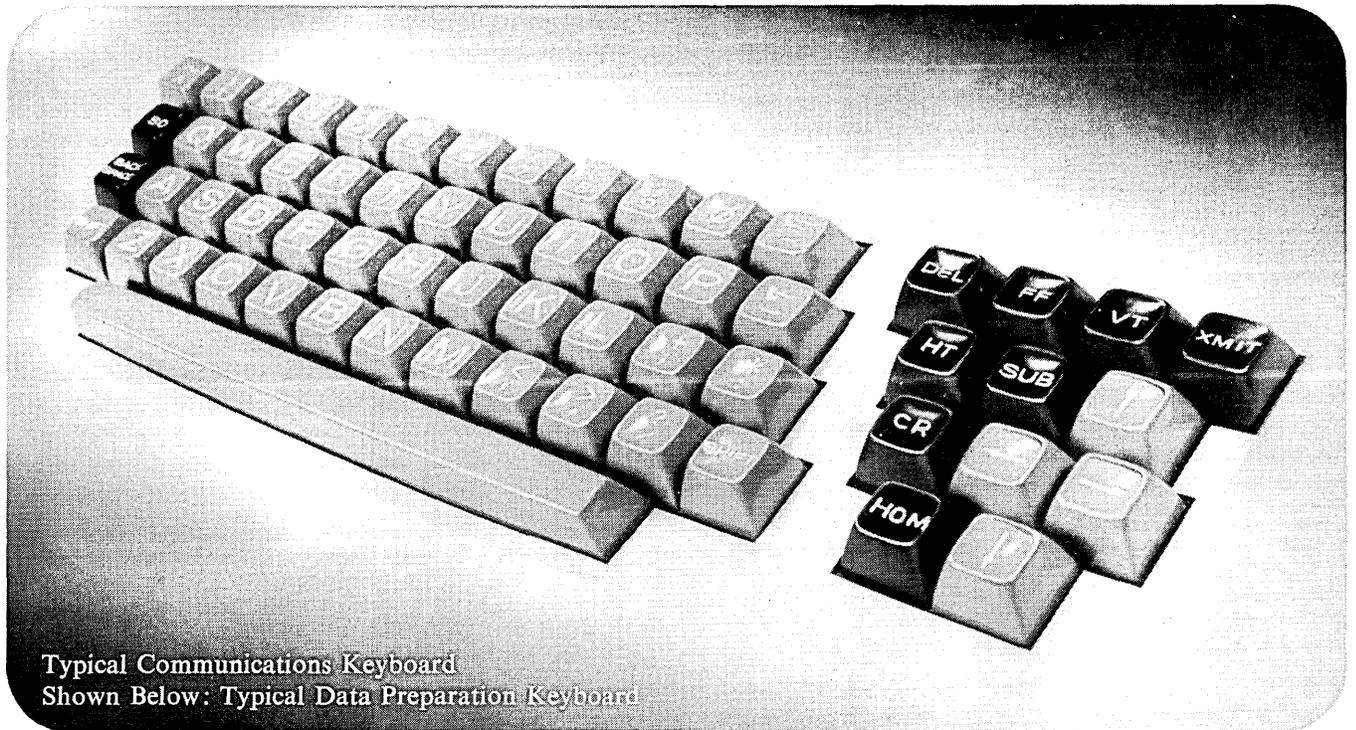
Hardware

A minimum hardware configuration consists of:

1. A CRT display system capable of resolving 1024 by 1024 separate points over an area at least 12" square, and capable of drawing full screen vectors in about 50 μs .
2. A light pen and alphanumeric keyboard.
3. A small high-speed computer with about 16K of memory (DDP-516 class).
4. A disc-store of at least one to five million characters for holding the current data base.
5. Possibly a mag tape drive for dumping the current data base when switching to another user. This would not be necessary if a replaceable disc-pac can be used for item 4.
6. Some device for producing hard-copy drawings and schedules. In the simplest system, this may consist of a camera photographing the CRT and a typewriter for printout. For more elaborate systems, a digital plotting table would be needed.

This configuration of hardware might cost in the region of \$150,000.

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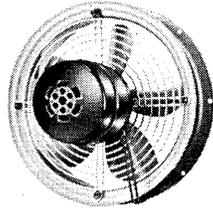
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Software

It is important that the basic software be established with a firm general purpose foundation and that it can be added to, rather than modified, to meet the requirements of a particular application. It is necessary to establish a flexible data structure in which the explicit and implicit content of a particular drawing is held in a form that can be easily processed by the computer. Largely due to the work of Ivan Sutherland, at MIT, a ring-type data structure has been found to be the most suitable for describing pictures within the computer. In principle, this technique allocates a number of memory cells—8, 12, or 16 (called a "bead")—to each distinct item of information, be it a point, a line, a transistor, a bolt, or some other identifiable unit. Pointers within each bead are then used to show how this item is related to other items in the system.

The data structure is, therefore, a whole collection of interlinked beads with each bead strung on a series of rings which relate it to those beads containing associated information.

The complete structure, and the interlinking of the beads, can be built up step by step from the CRT console as the operator uses his light pen. He will see a meaningful set of lines on the CRT and need not be aware of the data structure being built up within the computer. This technique is relatively extravagant in memory but it is general, relatively easy to implement, and allows particular applications-oriented subroutines to process the data in any required way.

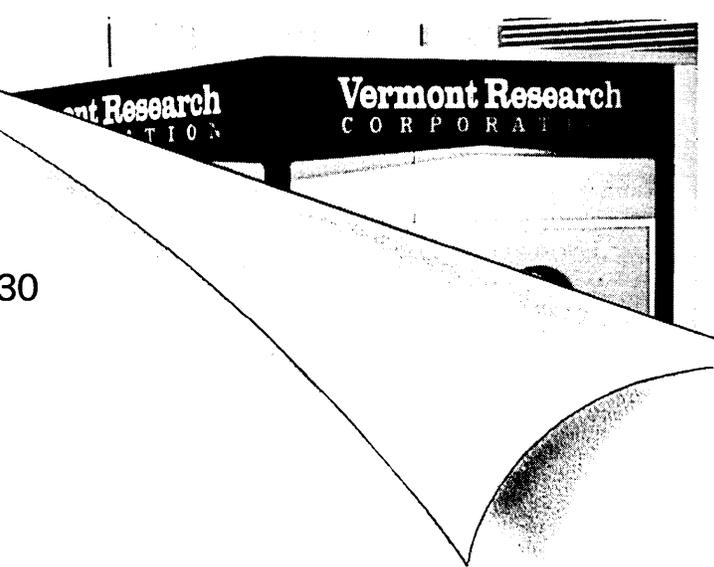
Ideally, the whole structure will be held in core at one time, but this is clearly impractical for any reasonably sized drawing. Because of the highly interlinked nature of this data, it is difficult to isolate it into records for transfer to and from a disc-backing store. It is therefore necessary to devise ways in which the structure can be partitioned, with as few links as possible, to adjacent partitions. Almost all related beads would then be in one partition and searching of rings would not require multiple disc transfers.

With the availability of a generalized data base, as described above, the additional software required for a specific simple application need not represent a major undertaking, perhaps between one and three man years.

Conclusions

A small computer system used solely for computer graphics can be an economic proposition. The rental cost of such a system might be equated to the cost of employing two or three men. If it could be made to produce more than three men could (which should be fairly easy to do), the system could be profitable in relatively small and unsophisticated industries. If small-scale computer graphics can be shown to be a viable proposition, similar to the way in which small-scale business data processing has proven to be, then wide-scale application can be expected. This will foster greatly accelerated progress toward the idealistic system described at the beginning of this commentary.

TO BE OPENED
APRIL 30



Fact:

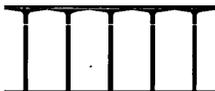
Two very pleasant surprises await users of random access, rotating memories at Booths L1-L2, SJCC.

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MOS SILICON P-CANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTORS (T _A = 25°C, BODY GROUNDING)									
TYPE	V _{DS} (VOLTS TYP)	I _D (mA TYP)	I _{SS} (mA TYP)	I _{SS} (mA TYP)	V _{GS} (VOLTS)	V _{GS} (VOLTS)	V _{GS} (μmhos TYP)	C _{iss} (PF TYP)	f _{oss} (Ω TYP)
MEM 511	-4.0	-6.0	-0.5	-0.1	-30	-30	2,500	2.0	150
2N4353	-4.0	-6.0	-0.5	-0.1	-30	-30	2,500	2.0	150
MEM 517	-3.5	-6.0	-0.8	-0.1	-30	-25	12,000	10	30
MEM 517A	-3.5	-6.0	-0.8	-0.1	-30	-25	12,000	10	30
MEM 517B	-3.5	-6.0	-0.8	-0.1	-30	-25	12,000	10	30
MEM 520	-4.0	-6.0	-0.5	-0.3	-30	NA	2,500	2.0	150
MEM 550*	-4.0	-5.0	-0.1	-0.1	-30	-25	1,400	1.1	250
3N151*	-4.0	-7.0	-0.2	-0.5	-30	-30	2,000	NA	250
MEM 551*	-4.0	-5.0	-0.5	-0.3	-30	NA	1,400	1.1	250
MEM 556	-4.0	-7.0	-0.1	-0.1	-65	-70	950	0.3	700

*Dual Device

MOS SILICON N-CANNEL DEPLETION MODE FIELD EFFECT TRANSISTORS (T _A = 25°C, BODY GROUNDING)									
TYPE	APPLICATION	FEATURES	V _n (μmhos TYP)	C _{iss} (PF TYP)	G _{ss} (dB TYP)	NF (dB TYP)	V _{GS} (VOLTS TYP)	V _{DS} (VOLTS)	f _{oss} (Ω TYP)
MEM 554	LINEAR VHF AMP & MIXERS	DUAL GATE CASCODE	12,000	.02	18 @ 200 MHz	3.2 @ 200 MHz	-1.5	-20	50
MEM 554C	LINEAR VHF AMP & MIXERS	DUAL GATE CASCODE	10,000	.02	17 @ 200 MHz	3.7 @ 200 MHz	-1.5	-20	50
MEM 557	VHF AMP	SINGLE GATE	10,000	.40	16 @ 200 MHz	3.2 @ 200 MHz	-1.5	-20	25

MOS SILICON N-CANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTORS (T _A = 25°C, BODY GROUNDING)									
TYPE	APPLICATION	V _{DS} (VOLTS TYP)	I _D (mA TYP)	I _{SS} (mA TYP)	I _{SS} (mA TYP)	V _{GS} (VOLTS)	V _{GS} (μmhos TYP)	f _{oss} (Ω TYP)	C _{iss} (PF TYP)
MEM 562	GEN. PURPOSE SWITCH	1.2	20	1.0	.01	30	4000 @ 10 mA	150	1.0
MEM 563	HIGH GAIN SWITCH	1.2	60	1.0	.01	20	7000 @ 10 mA	50	1.0

LOGIC CIRCUITS		POWER CONSUMPTION (mW MAX)	SUPPLY VOLTAGE (VOLTS)	PROPAGATION DELAY (nS TYP)	LOGIC LEVELS				FREQUENCY
TYPE	FUNCTION				INPUT		OUTPUT		
MEM 1000	DUAL FULL ADDER	55	-13V = 1V -27V = 1V	350	-10V	-2.0V	-11V	-1.0V	—
MEM 1002	DUAL 3-INPUT NOR GATE	35 per Gate	-27V = 1V	200	-10V	-2.0V	-11V	-1.0V	—
MEM 1005	R-S-T FLIP-FLOP	70	-27V = 1V	950 (Max.)	-10V	-2.0V	-11V	-1.0V	dc to 500 kHz
MEM 1008	DUAL EXCLUSIVE OR/NOT GATE	60 per Gate	-27V = 1V	300	-10V	-2.0V	-11V	-1.0V	—
MEM 1013	QUAD 2 INPUT NOR GATE	13 per Gate	-13V = 1V -27V = 1V	200	-10V	-2.0V	-11V	-1.0V	—
MEM 1014	QUAD 2 INPUT AND GATE	14 [Circ 1,2,3] 42 [Circ 4]*	-13V = 1V -27V = 1V	250	-10V	-2.0V	-11V	-1.0V	—
MEM 1015	DUAL J-K FLIP-FLOP	82 per Flip-Flop	-13V = 1V -27V = 1V	300	-10V	-2.0V	-11V	-1.0V	dc to 1.0 MHz
MEM 1022	9-BIT PARALLEL PARITY DETECTOR	80	-27V = 1V	500	-10V	-2.0V	-11V	-1.0V	dc to 500 kHz
MEM 1050	4 STAGE BINARY UP-DOWN COUNTER	300	-27V = 1V	—	-10V	-2.0V	-11V	-1.0V	dc to 160 kHz
MEM 1050B	4 STAGE BINARY UP-DOWN COUNTER	300	-27V = 1V	—	-10V	-2.0V	-11V	-1.0V	dc to 2.5 MHz
MEM 1051	BUFFERED D/A CONVERTER	35	-13V = 1.5V -25V = 3V	—	-10V	-2.0V	-11V	-1.0V	dc to 500 kHz
MEM 1055	4 STAGE BINARY UP-DOWN COUNTER WITH RESET	300	-27V = 1V	—	-10V	-2.0V	-11V	-1.0V	dc to 2.5 MHz

*The MEM 1014 provides Four 2-Input AND Gates (Circuits 1,2,3,4); Circuit 4 also provides a NAND Output

MULTIPLEXER CIRCUITS		OFF RESISTANCE (Ω TYP)	ON RESISTANCE (Ω TYP)	CAPACITANCE (pF Cgd)	V _{GS} (VOLTS)	V _{DS} (VOLTS)
TYPE	FUNCTION					
MEM 2002	5 CHANNELS (4 Channels -Common Drain)	10 ¹⁰	200	1.1	-30	-30
MEM 2003	4 CHANNELS (Protective Diodes)	10 ¹⁰	200	1.1	-30	-30
MEM 2004	4 CHANNELS (No Diodes)	10 ¹⁰	200	1.1	-30	-60
MEM 2005	4 CHANNELS (Dual 2 Channel)	10 ¹⁰	200	1.1	-30	-30
MEM 2006	3 CHANNELS (2 Channels -Common Drain)	10 ¹⁰	200	1.1	-30	-30
MEM 2009	6 CHANNELS (Protective Diodes)	10 ¹⁰	150	1.9	-30	-30
MEM 2017	6 CHANNELS (Protective Diodes)	10 ¹⁰	700	0.5	-50	-50

MAKE THIS STATEMENT:

SERIES SHUNT CHOPPER		OFFSET VOLTAGE	CLOCK ϕ	FREQUENCY (kHz)	ON RESISTANCE PER UNIT (SERIES OR SHUNT) (Ω TYP)	OFF RESISTANCE PER UNIT (SERIES OR SHUNT) (Ω TYP)	SIGNAL VOLTAGE HANDLING RANGE (TYP)
TYPE	FUNCTION						
MEM 2008	INTEGRATED SERIES SHUNT CHOP. CIRCUIT	0	1	100	6K	10^{12}	$1\mu V - 10V$

SHIFT REGISTERS		STATIC	DYNAMIC	FREQUENCY	NUMBER OF BITS	INPUT		OUTPUT		NO. OF CLOCKS	SUPPLY VOLTAGE (VOLTS)
TYPE	FUNCTION					PARALLEL	SERIES	PARALLEL	SERIES		
MEM 3005PP	5-BIT PARALLEL IN/ PARALLEL OUT	X		dc to 1.0MHz	5	X	X	X	X	2	-13V \pm 1V
MEM 3005SP	5-BIT SERIAL IN/ PARALLEL OUT	X		dc to 1.0MHz	5		X	X	X	2	-13V \pm 1V -27V \pm 1V
MEM 3008PS	8-BIT 2 ϕ PARALLEL IN/SERIAL OUT	X		dc to 1.0MHz	8	X	X		X	2	-13V \pm 1V -27V \pm 1V
MEM 3012SP	12-BIT SERIAL IN/ PARALLEL OUT	X		dc to 100kHz	12		X	X	X	1	-27V \pm 1V
MEM 3016-2	DUAL 16-BIT	X		dc to 1.0MHz	32 (16,16)		X		X	2	-13V \pm 1V -27V \pm 1V
MEM 3020	20-BIT	X		dc to 1.0MHz	20		X		X	2	-13V \pm 1V -27V \pm 1V
MEM 3021	21-BIT	X		dc to 500kHz	21 (1,4,16)		X		X	1	-27V \pm 1V
MEM 3021B	21-BIT	X		dc to 250kHz	21 (1,4,16)		X		X	1	-27V \pm 1V
MEM 3032	6-1 ϕ BINARY WEIGHTED	X		dc to 1.0MHz	32 (1,1,2, 4,8,16)		X		X	1	-13V \pm 1V -27V \pm 1V
MEM 3040	40-BIT	X		dc to 1.0 MHz	40 (4,4, 16,16)		X		X	1	-13V \pm 1V -27V \pm 1V
MEM 3050	DUAL 25-BIT		X	10kHz to 500kHz	50 (25,25)		X		X	2	-27V \pm 1V
MEM 3064	64-BIT SERIAL ACCUMULATOR		X	10kHz to 5.0MHz	64		X		X	4	NONE
MEM 3064B	64-BIT SERIAL ACCUMULATOR		X	10kHz to 2.0MHz	64		X		X	4	NONE
MEM 3064-2B	DUAL 64-BIT SERIAL ACCUMULATOR		X	10kHz to 2.0MHz	128 (64,64)		X		X	4	NONE
MEM 3100	DUAL 50-BIT		X	10kHz to 2.0MHz	100 (50,50)		X		X	2	-18V \pm 1V
MEM 3128	128-BIT		X	10kHz to 2.0MHz	128		X		X	2	-18V \pm 1V
MEM 3198	TRIPLE 66-BIT		X	10kHz to 1.0MHz	198 (66,66,66)		X		X	2	-27V \pm 1V

LARGE DIGITAL SUBSYSTEMS		POWER CONSUMPTION (mW)	SUPPLY VOLTAGE (VOLTS)	CLOCK RATE	DESCRIPTION
TYPE	FUNCTION				
MEM 5014	A/D-D/A CONVERTER ELEMENT	135	-27V \pm 1V	dc to 200 kHz	Complete logic and analog switching for 10-bit successive approximation A/D converter.
MEM 5015	16 CHANNEL RANDOM ACCESS MULTIPLEXER	80	-27V \pm 1V	dc to 100 kHz	Sixteen Channel Multiplexer with address storage and decoding.
MEM 5021	DDA ELEMENT	100	-13V \pm 1V -27V \pm 1V	dc to 500 kHz	Ternary type DDA performing rectangular integration.
MEM 5031	SERVO ADDER	25	-13V \pm 1V -27V \pm 1V	dc to 1.0 MHz	Shift Register content decision unit used in conjunction with the MEM 5021.
MEM 5035	2 INPUT DELTA "Y" SUMMER	80	-13V \pm 1V	10 kHz to 500 kHz	2 Input Delta "Y" Summer used in conjunction with the MEM 5021.
MEM 5116	16 CHANNEL RANDOM SEQUENTIAL ACCESS MULTIPLEXER	100	-27V \pm 1V	dc to 500 kHz	Sixteen Channel Multiplexer with parallel access counter and decoding.
MEM 5132	RANDOM ACCESS MEMORY CELL	100	+5V \pm 0.5V -12V \pm 1V	dc to 500 kHz	32-BIT Random Access Memory Cell for large and small Memory Systems.

4th GENERATION SYSTEMS		POWER CONSUMPTION (mW)	SUPPLY VOLTAGE (VOLTS)	CLOCK RATE	DESCRIPTION
TYPE	FUNCTION				
S-C-100	MINIATURE A/D CONVERTER SYSTEM	300	-27V \pm 2V -15V \pm 2V +15V \pm 2V REF. VOLT	dc to 100 kHz	Complete 10-BIT A/D Converter System
S-C-101	MINIATURE D/A CONVERTER SYSTEM	300	-27V \pm 2V -15V \pm 2V +15V \pm 2V REF. VOLT	dc to 200 kHz	Complete 10-BIT D/A Converter System



All 61 MTOS devices listed are available off-the-shelf from your authorized General Instrument distributor.



Write for complete information. (In Europe contact General Instrument Europe, Via Turati 28, Milano, Italy.)

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CIRCLE NO. 43 ON INQUIRY CARD

Tomorrow morning you can build a system with compatible digital hardware from Raytheon Computer and enjoy your coffee break. You'll have it made.

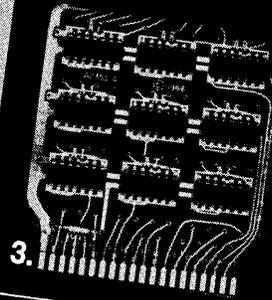
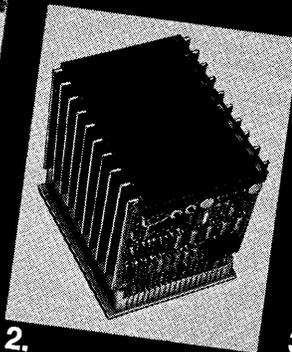
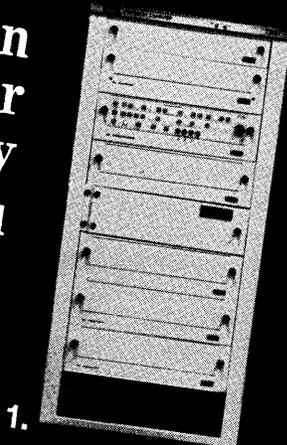
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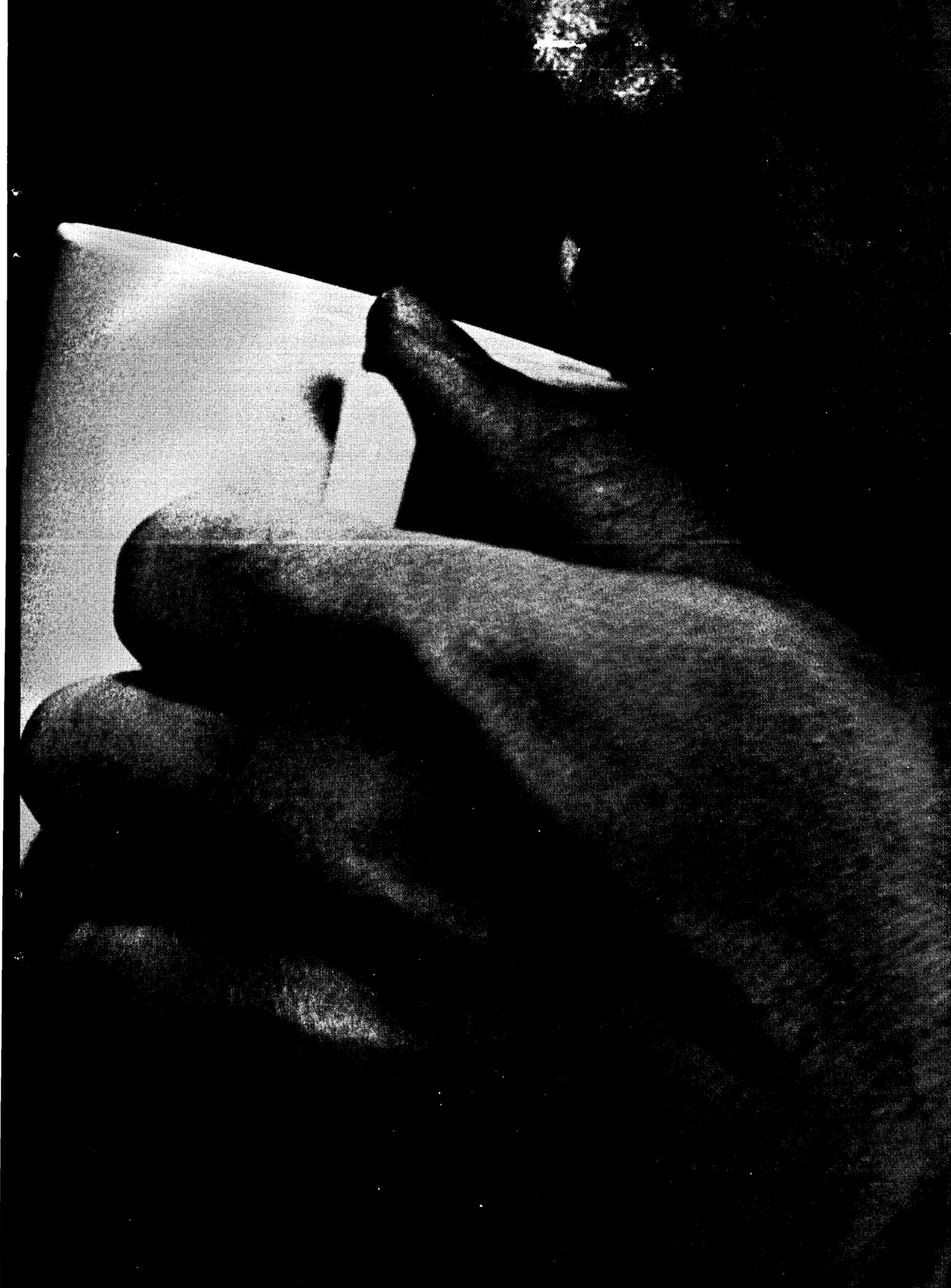
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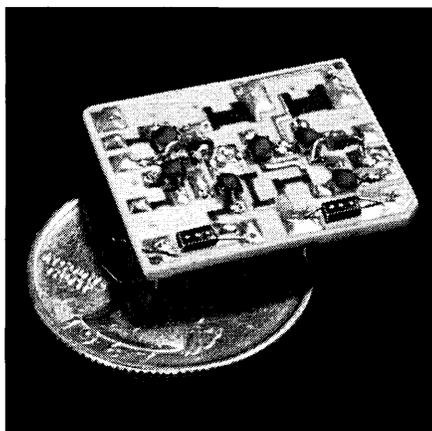




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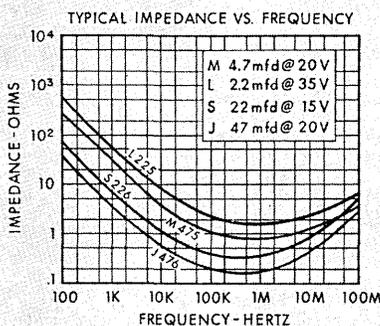
to 125°C, they are available in values from .001 to 220 mfd., with axial or radial leads.

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(others available from .001 MFD @ 50 VDC)

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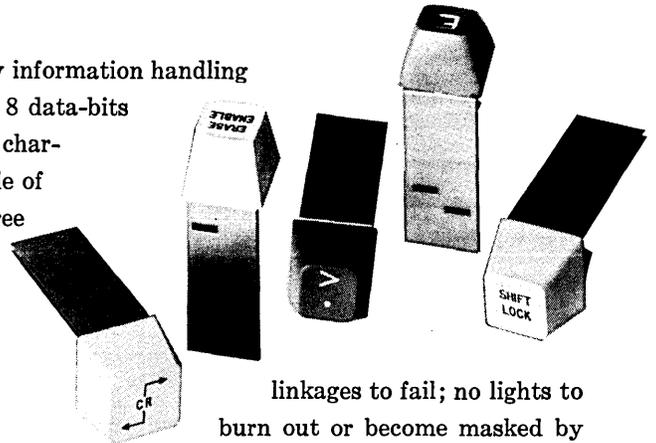
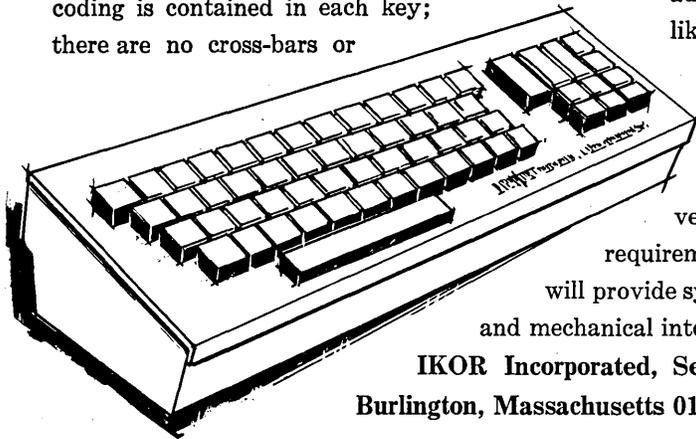
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NM	
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- Incremental write/incremental read
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- 0-500 character/second write

Basic 1600 specifications are:

- Reel size: 8½" 1200' capacity
- Recording format: 7-track IBM compatible
- Recording speed: 0-300 characters/second
- Skip rate: 1000 increments/second
- Density: 200 or 556 BPI
- Parity generation: Internal odd or even
- Gap generation: Internal BOT, EOR, EOF
- Input logic levels; IC compatible (DTL)
0 V \pm .5 V false +4 V (min) true
- Output logic levels: IC compatible (DTL)
0 V \pm .5 V false +10 V $\frac{+0}{-2V}$ true
- Size: 19 x 12¼ x 10 deep
- Power: 115V 60 Hz 120 watts

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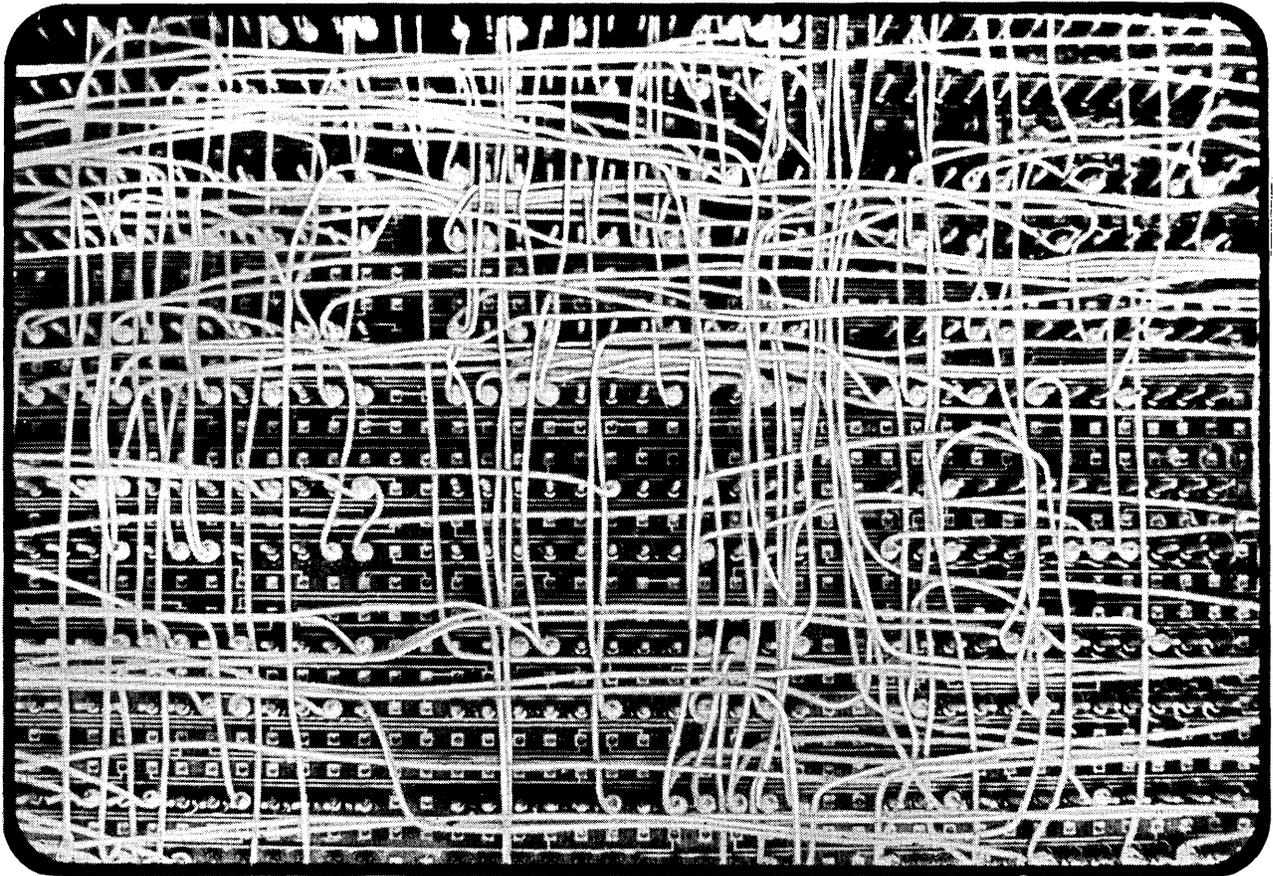


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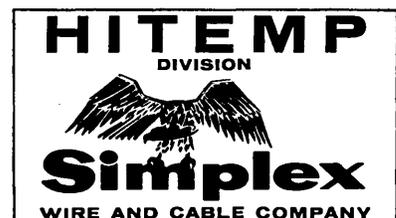


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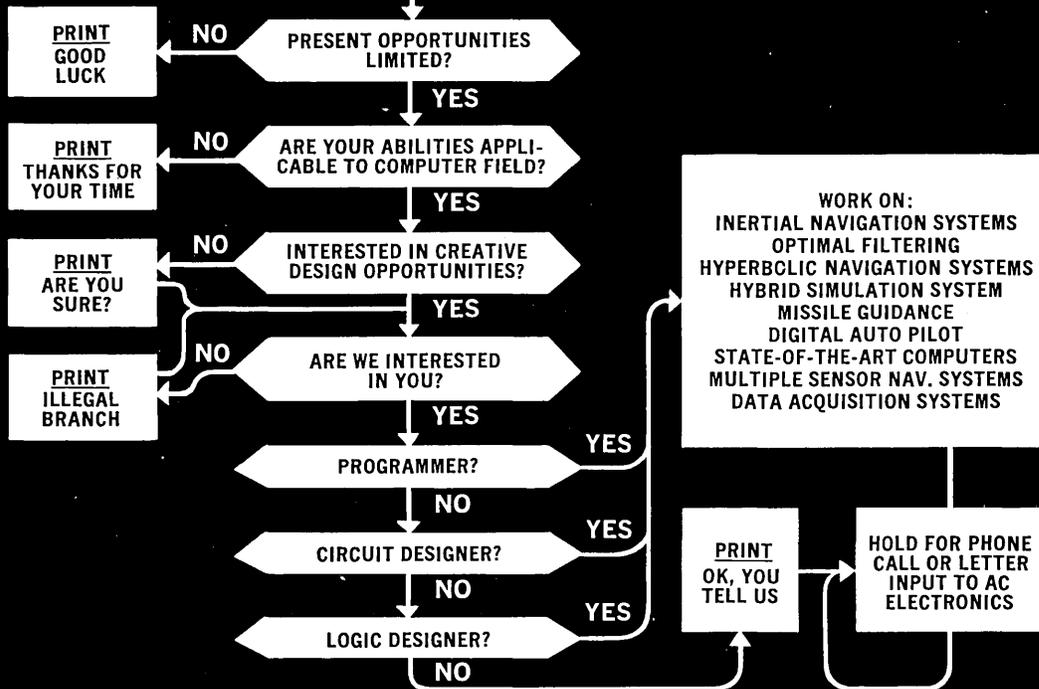
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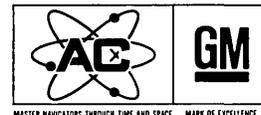
Instrumentation Systems Designers —

Perform logic and circuit design, development and check-out of airborne and ground instrumentations systems.

Computer Logic Designers —

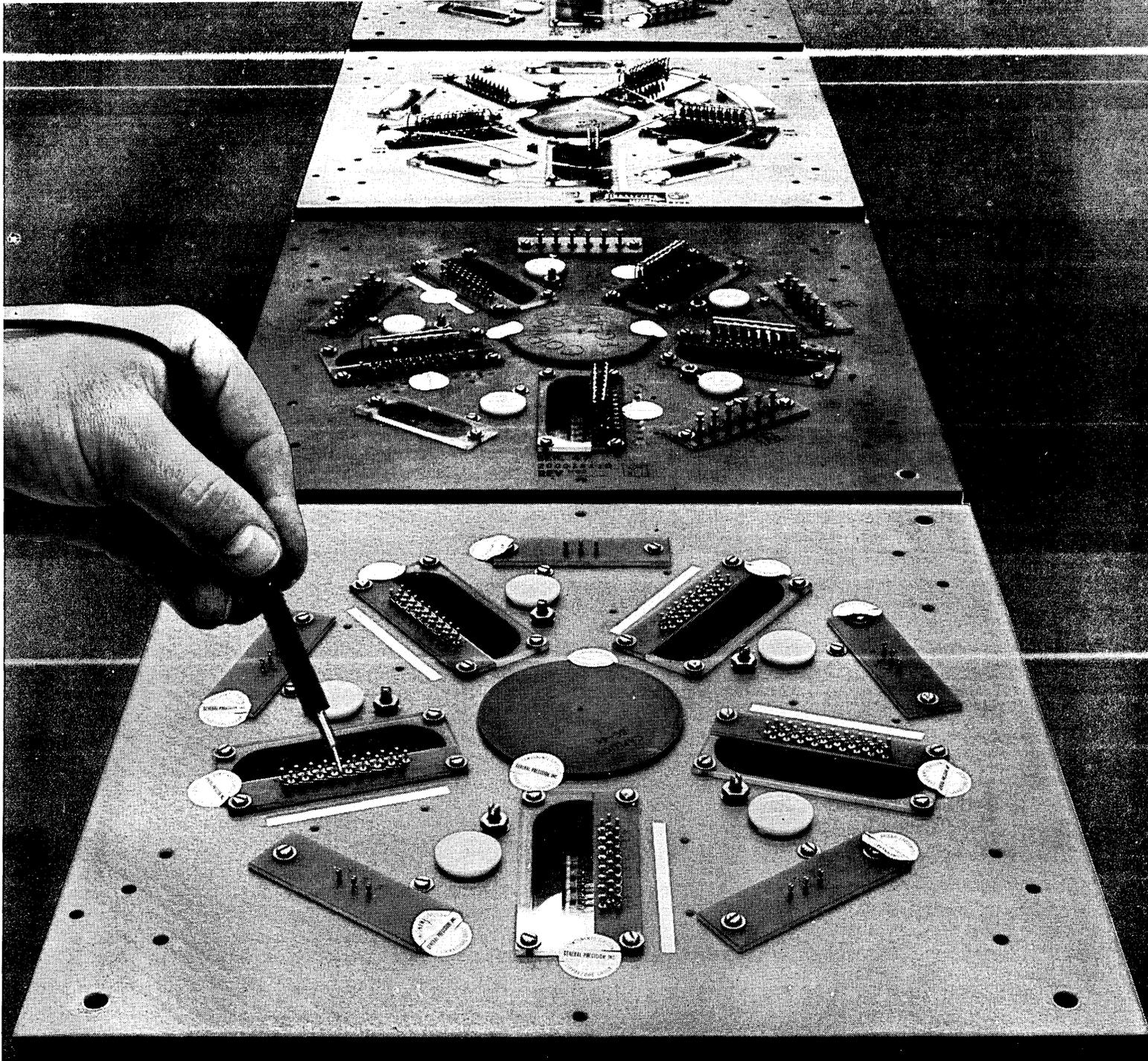
Develop and optimize advanced logic input-output design for use in real time computer application.

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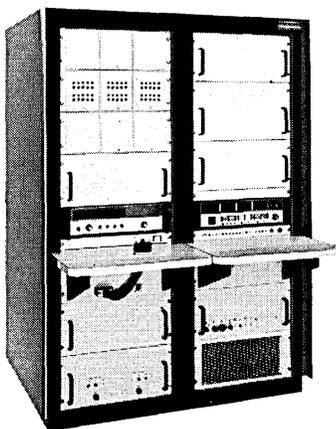


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CIRCLE NO. 900 ON INQUIRY CARD



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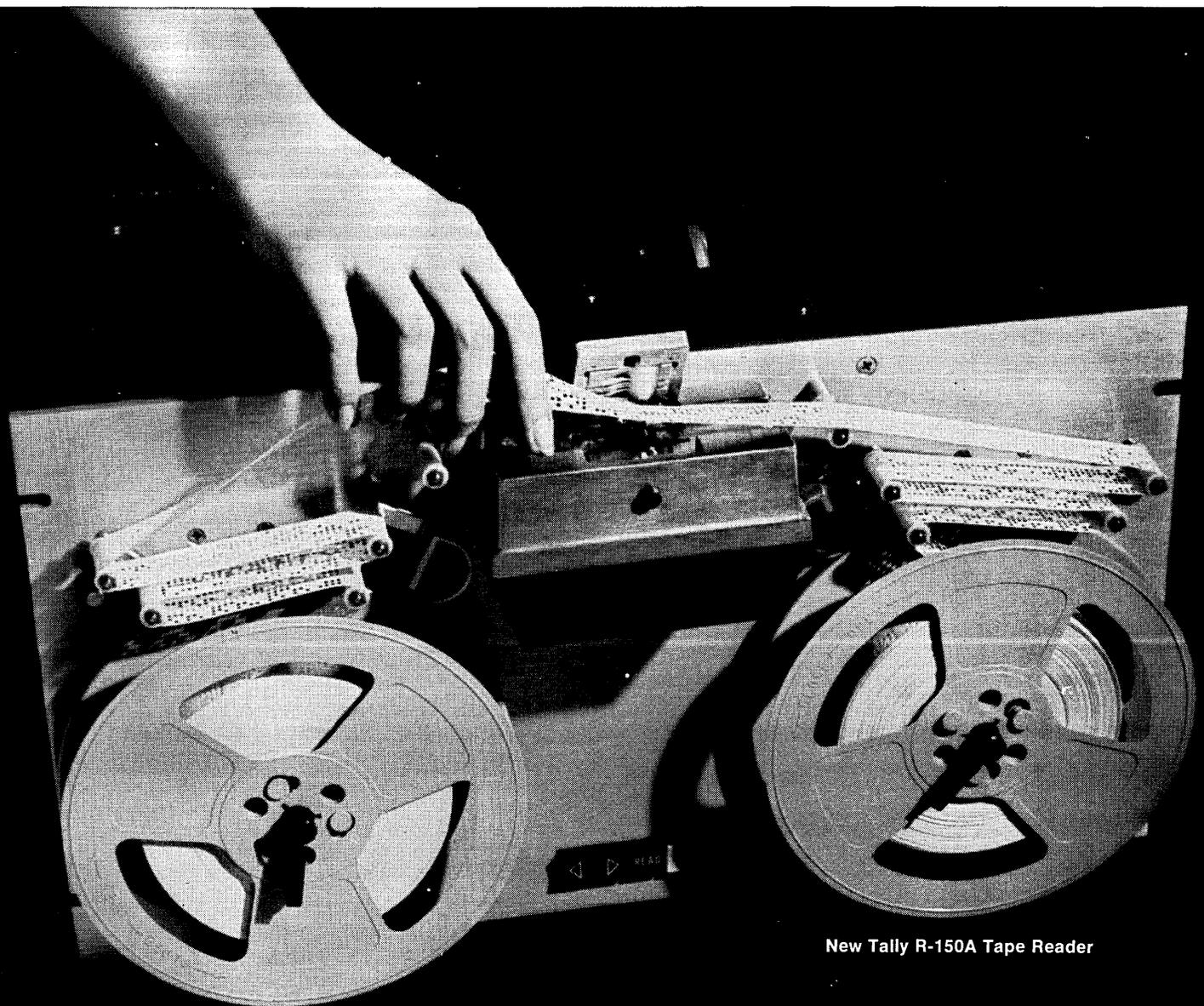
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TALLY

This article describes solutions to the problems of designing small core memories for systems using Solid Logic Technology — IBM's hybrid circuit and packaging technology developed for 360 systems.

DESIGN OF MODULAR, LOW-COST FOR SLT SYSTEMS

Two ferrite core memories, of similar design, were developed to meet a need for small modular core storage units. In a smaller system, such as the IBM 1130 Computing System, the units function as the main memory. The larger System/360 processors use them for local storage and as buffers.

The design parameters were for a low-cost, compact unit, which would require a minimum number of adjustments, be capable of operating with wide margins, and could be built with normal production tolerance components. The criteria were met by using

- Pluggable arrays mounted on the SLT "large board." ("Solid Logic Technology" is the hybrid circuit and packaging technology that IBM developed for System/360. Terms "small card" and "large board" refer to second and third level packages, respectively. See Figure 18 for example.)

- A three-wire-per-core array winding system.
- A "crossbar" drive rather than the conventional direct-drive system. (Use of the "crossbar" causes a dramatic reduction in drive circuits.)
- Common parts numbers for units of different size and speed.
- A novel circuit, resulting in a very simple sense-amplifier with an extremely good common-mode rejection ratio.

The unit is suitable for a variety of applications, since the electronic circuitry was designed to interface readily with standard SLT.

The basic $4 \mu\text{s}$ core storage unit is available in either 4K words or 8K words (18 bits/word). 16K and 32K memories are made up from multiple 8K units. The compatible higher performance units have the same capacities but operate on a $2 \mu\text{s}$ cycle.

ELECTRONICS DISCUSSION — $4 \mu\text{s}$ VERSION

Low Power Levels — A Basic Parameter

To enable the use of low power levels, the array package and its interconnection to the large board were designed for low resistive drop and a short electrical

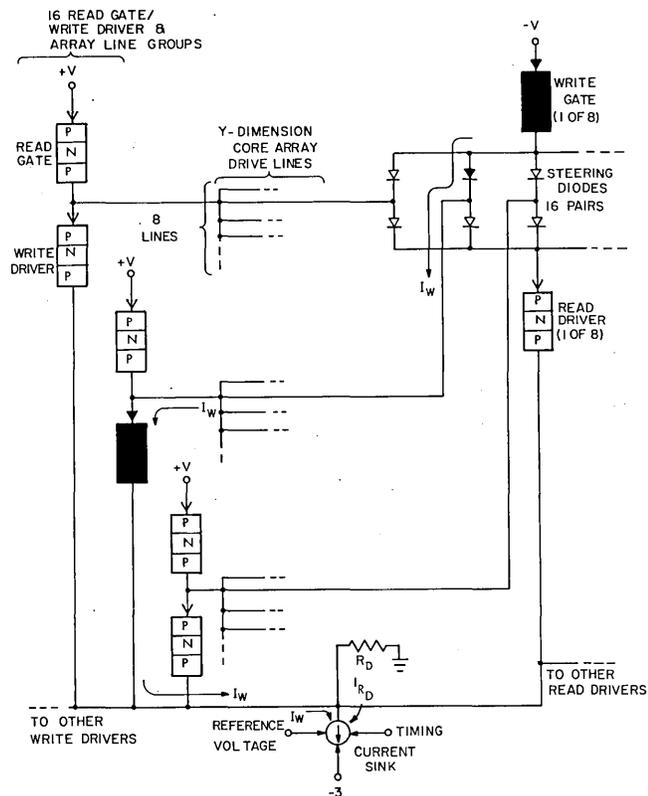


Figure 2. $4 \mu\text{s}$ core memory crossbar drive system.

transmission line length. The units are thereby able to use relatively low-speed drive systems, operating with supply voltages lower than 15 volts. The $4 \mu\text{s}$ version operates satisfactorily without requiring true termination of drive lines, thereby saving on the cost and power dissipation of multiple terminating resistors.

"Crossbar Drive" Reduces Component Count

A method that has come to be known as the "crossbar drive" was used to minimize the number of selection elements (see Figures 1 and 2). The conventional direct-

CORE MEMORIES

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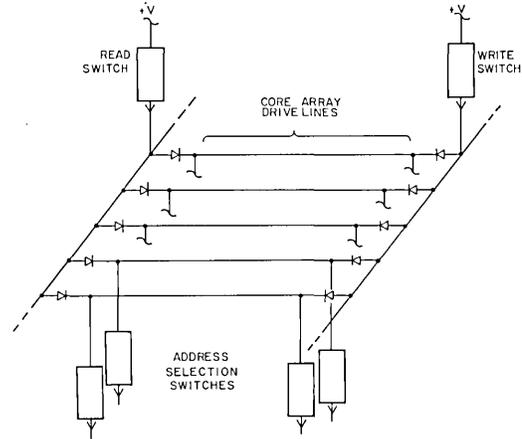


Figure 3. Hybrid direct drive system.

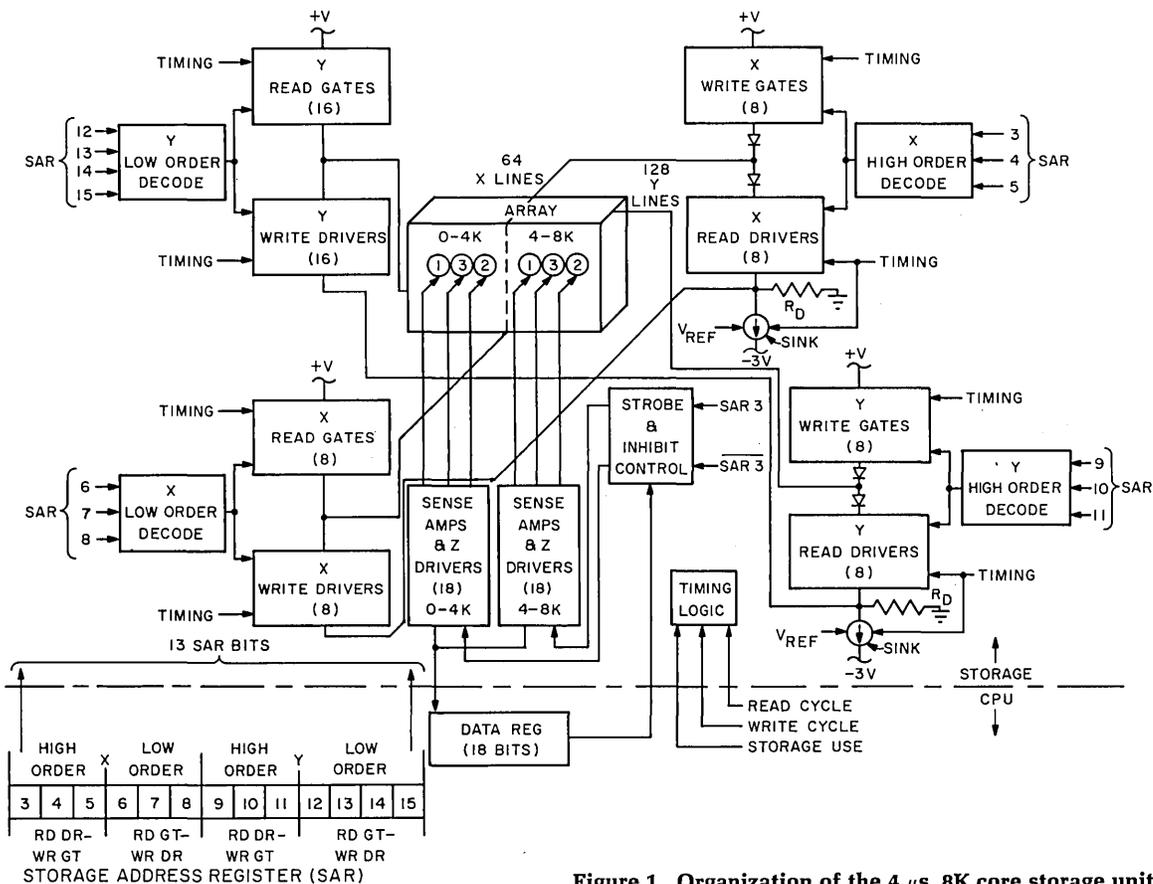


Figure 1. Organization of the 4 μs, 8K core storage unit.

drive system (see Figure 3) for the 8K array (dimensions 64 x 128) would have required 768 selection transistors to perform read and write operations. There would be 384 separate connections between the array package and the drive circuits. Some improvement could be made by using a combination of transistors and steering diodes, which are less costly than transistors. However, the configuration would still require 384 transistors and 384 diodes, and the number of connections would not be reduced. By contrast, the crossbar drive

requires only 80 transistors, 384 diodes and 56 connections between array and drive circuits. The implications for cost, size, and reliability are obvious.

The overall logical organization of the storage unit is seen in Figure 1. It requires 13 bits of Storage Address Register (SAR) to select one out of 8192 addresses. These 13 bits are decoded in groups of 3, 3, 3 and 4 to select the appropriate gates and drivers. The gates and drivers are saturating switches which complete a path between the +V supply and the pulsed current sink.

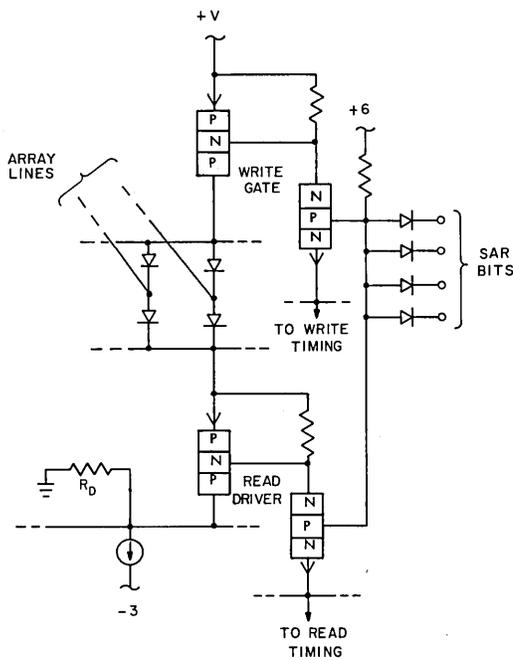


Figure 4. 4 μ s core memory gate/driver circuits.

This is seen in detail in Figure 2. The shaded components are the elements that would be selected to drive write half-select current I_W through the Y drive line shown. R_D functions as an approximate termination. However, it can be seen that the selected array line is also shunted at the left end by the other lines in its group. Thus, a precise termination is impossible for current, and R_D must be chosen for the best compromise between read and write current waveforms.

The complete gate and driver circuits are shown in Figure 4. The address bits are decoded by a conventional SLT AND gate, the output of which drives the predriver circuit of one Gate and one Driver. Both circuits are packaged on the same SLT small card to optimize use of card contacts. Timing is accomplished by pulsing the groups of preamp emitters negative. Only that preamp which is selected at its base will conduct. Its collector current will saturate the output stage, allowing array current to flow.

The steering diodes shown in Figure 2 are required in the crossbar drive for prevention of sneak path current. Figure 5 shows what will happen if a diode is shorted. The magnitude of I_{sneak} is enough to limit severely the SCHMOO margins of a practical memory². (See Sidebar 1 and Ref. 2). The diodes are packaged on top of the array on a glass-epoxy circuit board. Commoning connections between diodes are made on this board. Commoning connections between lines at the other end of the drive system are made on another glass-epoxy circuit board at the bottom of the array. Figure 6 diagrams the actual physical path the Y drive current takes.

Three-Wire Sense and Inhibit System

Three wires were used per core, rather than the four or more customary in a three-dimensional core storage system. This innovation in core design was developed at IBM's Poughkeepsie location. Each array plane is wound with two mats of cores (see Figure 7) which are

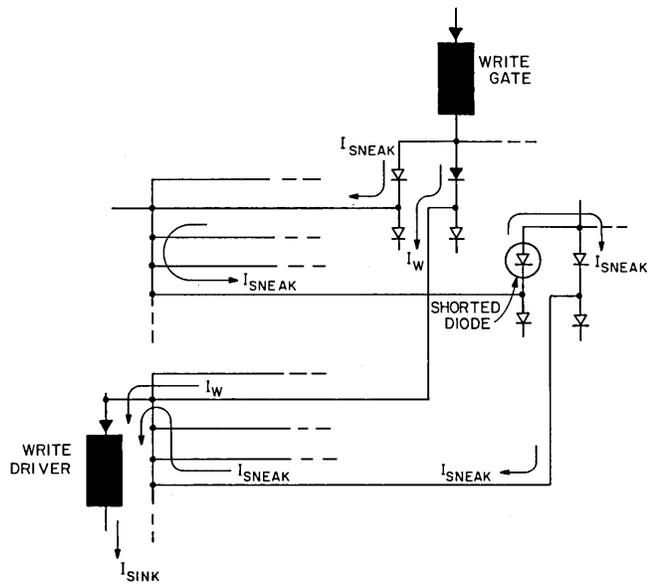


Figure 5. 4 μ s memory sneak path.

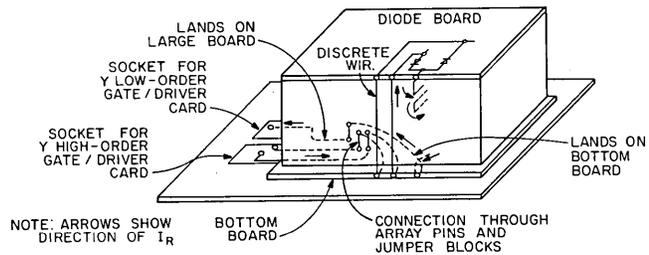


Figure 6. Half-select drive, 4 μ s core unit.

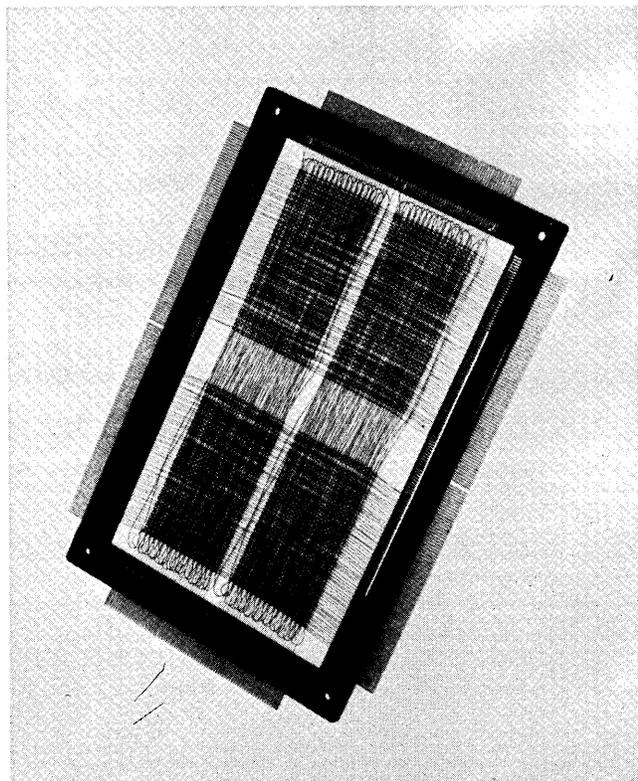


Figure 7. Core plane for the 4 μ sec and 2 μ sec memories.

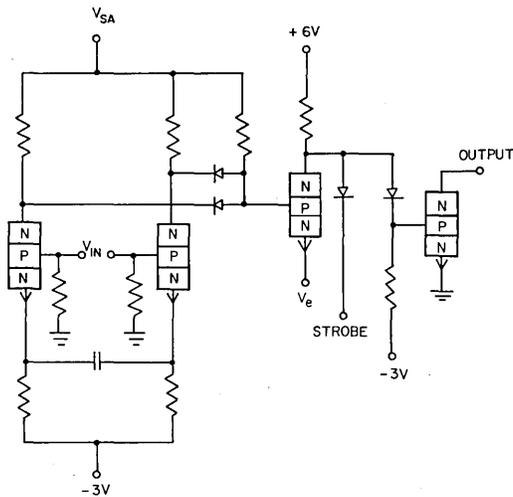


Figure 11. 4 μ s core memory sense amplifier.

Statistical Circuit Design

The sense amplifier, shown in Figure 11, is a simple, inexpensive circuit designed statistically (see Sidebar 2 and Ref. 4) to accommodate normal component tolerance.

The 36 sense amplifiers in an 8K unit share a common threshold-setting voltage (V_{sa}) and emitter offset voltage (V_e). The difference ($V_{sa} - V_e$) determines the precise input signal amplitude which causes an output. Making V_{sa} variable allows the gray area to be translated to the most favorable region for operating conditions (see Sidebar 2). A common strobe pulse network turns on all 18 sense amplifiers in that half of the array being read. Strobe timing is controlled by a single shot and can be varied to optimize this important parameter.

The inhibit driver is a simple saturated switch which connects the sense/inhibit winding through a resistor to a voltage source. The capacitor that shunts the limiting resistor (Figure 9) provides some speedup of current risetime. Current through the resistor splits and flows through the two halves of the sense/inhibit winding. The driver transistors have an upper limit placed on $V_{ce(sat)}$, since this drop, along with the resistive drops, controls the equality of the current split.

Operable Over Wide Temperature Range

The storage units were designed to operate over an environmental temperature range of 40-125°F. The magnetic properties of the cores change considerably from one temperature extreme to the other. One solution is to provide a special cooling plenum for the array and to stabilize the temperature within this subsystem. This is effective, but it is also costly and space consuming. The alternative we chose was to change the drive currents to track with temperature. The reference voltage (V_{ref}) shown in Figure 2 controls the current pulse amplitude at the sink. It is quite easy to generate V_{ref} from a network which includes a temperature-dependent resistive element, in this case a Thermistor.[®] The topology chosen for this

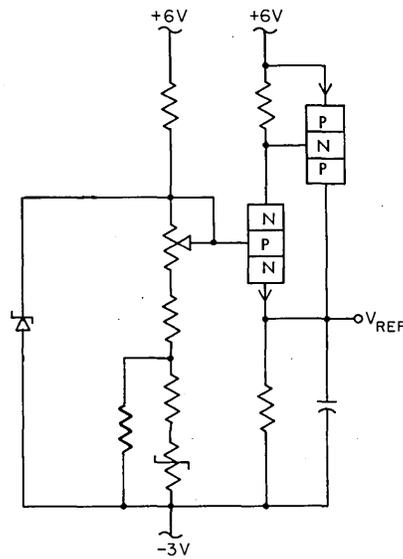


Figure 12. 4 μ s core memory reference voltage circuit.

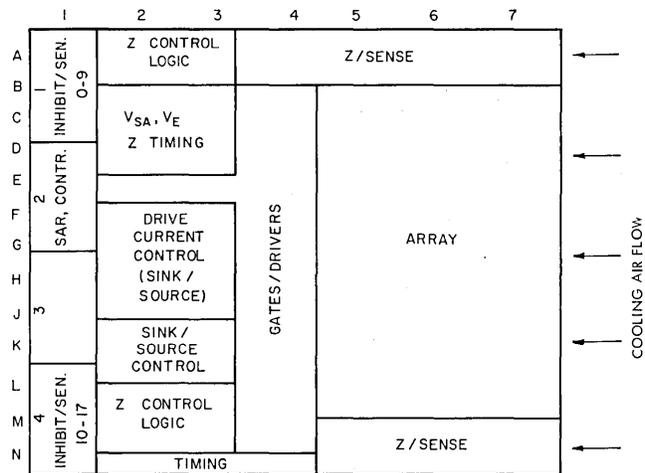


Figure 13. SLT "large board" layout.

application is shown in Figure 12. As temperature increases, V_{ref} becomes smaller, and, therefore, drive current becomes smaller. The padder resistances are chosen to match a curve determined empirically from SCHMOO data taken over the temperature range.

Increased Maintainability by Minimizing Number of Adjustments

Three potentiometers are used in the storage unit: V_{ref} , V_{sa} , and Strobe Time. This low count results from use of statistically designable circuits which can be mass produced and still operate as intended. The benefits to field maintenance and reliability are considerable. A side benefit is reduced cost, since stable hermetically sealed potentiometers cost several dollars apiece.

Cooling Determines Circuit Placement

The circuits do not all require an equal flow of cooling air. This allows a choice to be made as to which circuits to place in locations difficult to cool. Figure 13 shows the physical layout of the SLT "large

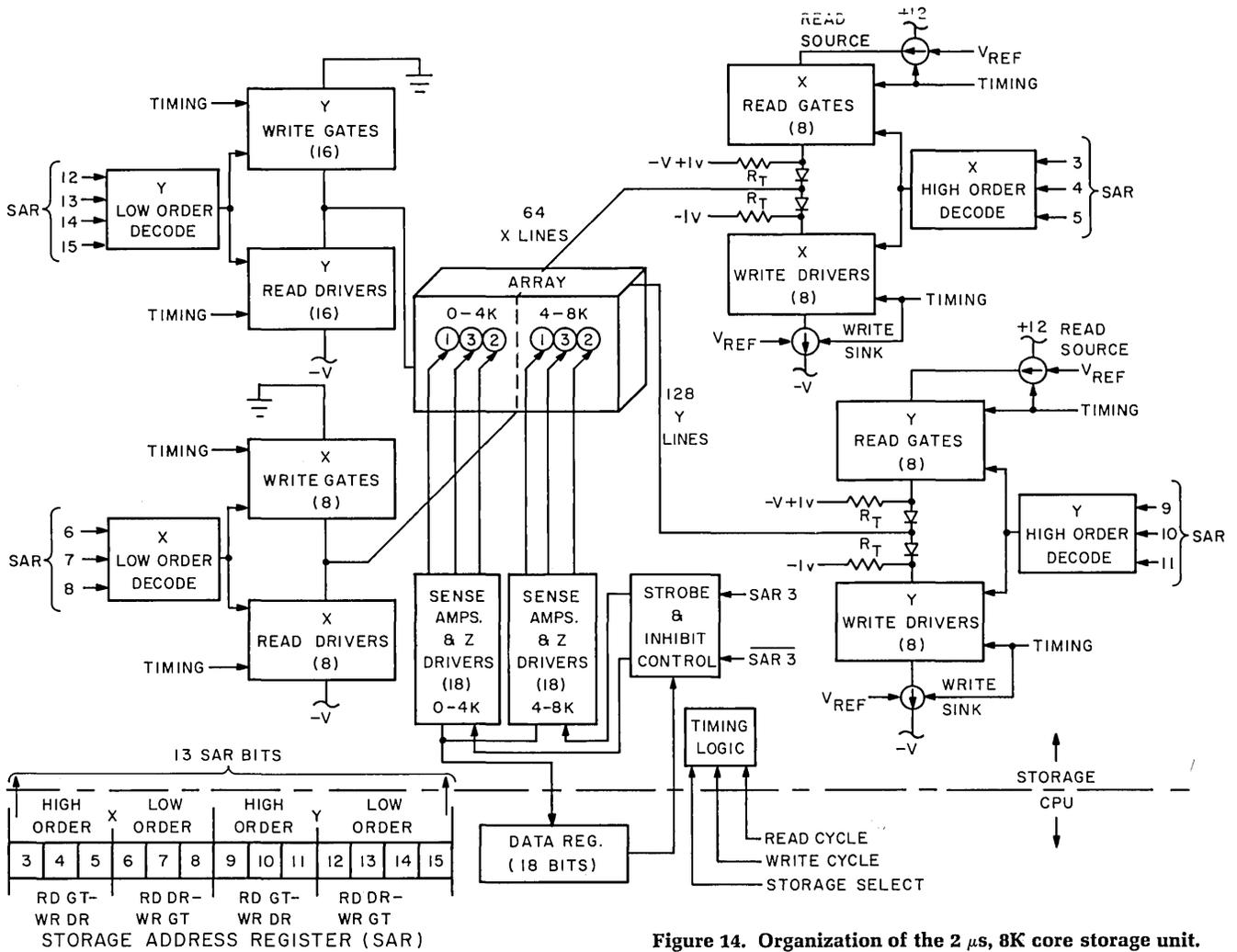


Figure 14. Organization of the 2 μ s, 8K core storage unit.

board." Since the inhibit driver is a relatively high dissipation circuit, the sense/inhibit cards are located in the outside cooling columns, where the array does not obstruct air flow.

The gates and drivers can be cooled with only 150 feet/min. of air. Therefore, they are placed in the array shadow. The current control circuits, such as the sink, have high dissipation. So they are placed in the second row above the array. A hump in the card cover bypasses air over the array and mixes it with the array exhaust. This brings up the average velocity in the top row sufficiently to cool the sink.

ELECTRONICS DISCUSSION — 2 μ s VERSION

To meet the need for performance upgrading of small systems, a compatible, faster series of core storage units was developed. The same basic design was used with suitable modifications to meet the faster risetime requirements. The crossbar drive system was found to be practical when a more accurate way was found to terminate the drive lines (see Ref. 1). Figure 14 shows the logical organization of the 8K, 2 μ s version. A comparison with Figure 1 will demonstrate the basic similarity of the two. The most significant difference is in the use of two current control elements, a sink and a source, to control I_{write} and I_{read} , respectively (see Figure 15). The crossbar switch elements on the

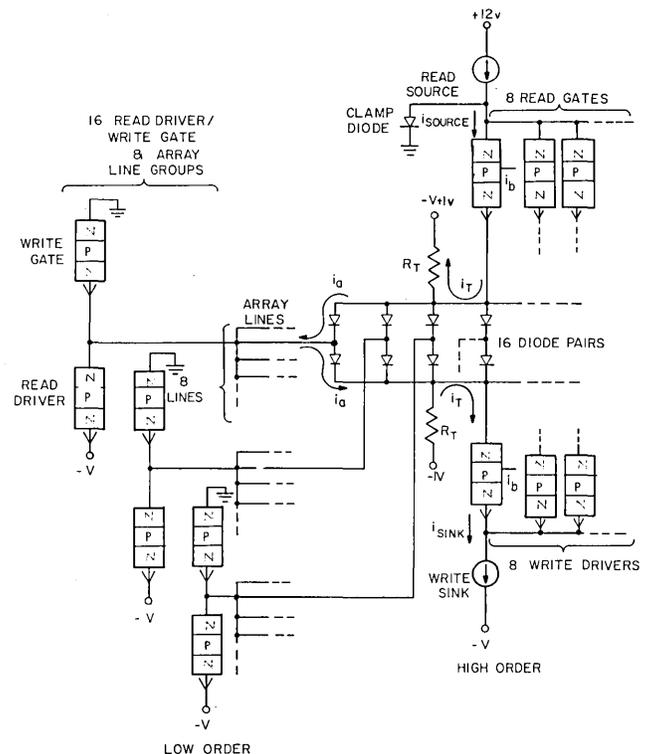


Figure 15. Y dimension drive, 2 μ s unit.

left are used to connect the array line group either to ground or to the $-V$ supply voltage. The diode end of the array is connected to the sink at write time or the source at read time. There are two terminating resistors for each diode group. Since the diodes isolate the 15 nonselected lines from the resistor as soon as the turn-on transient is over, a considerably improved termination can be achieved. Of course, a single terminator right at the source and at the sink could be used, merely extending the analogy with the $4 \mu\text{s}$ system. However, placing the resistors as shown, it is possible to terminate capacitive charge currents as well. These currents flow in the nonselected lines as a result of the voltage shifts imposed at the beginning of the drive pulse.

Improved Sense/Inhibit System

The $2 \mu\text{s}$ unit uses the same basic sense/inhibit system as the $4 \mu\text{s}$ unit. Certain changes are necessary, however, due to faster risetimes and larger voltage transients. Figure 16 shows the complete system. When this is compared to Figure 9, it is apparent that the method of driving inhibit current through the winding from the center tap places a lower common-mode signal at the sense amplifier input. This improves recovery following inhibit turn-off but costs an additional termination register, R_D , to control the voltage excursion at the center tap, plus two clamp diodes (D_1 and D_2 in Figure 16).

Novel Sense Amplifier with Improved Characteristics

The sense amplifier must handle a faster rep rate and generally more stringent operating conditions. The amplifier circuit is shown in Figure 17 in greater detail. It can be seen by a comparison with Figure 11 that the emitter cross-coupling capacitor in the input stage has been replaced by a collector load transformer. This is connected such that common-mode signals see virtually a dead short, while differential signals see a very high impedance shunted by the resistive loads. The transformer prevents the normal imbalance in quiescent collector currents from having an adverse effect on detection threshold.

Statistical Analysis of Performance by PERT

As cycle times are pushed down, core memory access times (time to fetch data) tend to occupy larger fractions of the cycle time. Accordingly, it becomes difficult for a computer to use a faster memory even if the computer logic itself is capable of operating at a faster clock rate. Thus, in the case of the $2 \mu\text{sec}$ memory, access time *did* become a critical parameter. A cursory pass at a "worst-case" delay study indicated a hopeless situation.

A statistical design approach was needed to give a realistic picture of the actual performance. The well-known PERT technique was found to be the most practical tool (Ref. 5). The PERT analysis indicated that less than three out of a thousand units would fail to meet the design specification. Worst-case analysis would have dictated an access time specification

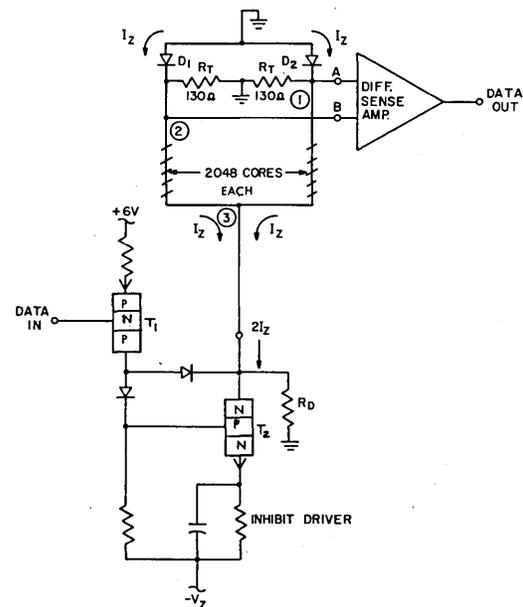


Figure 16. Sense/inhibit system, $2 \mu\text{s}$ unit.

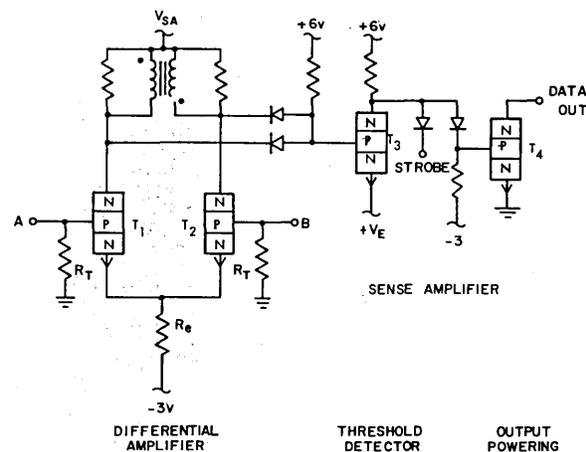


Figure 17. Sense amplifier, $2 \mu\text{s}$ unit.

around 80% slower. Production experience has validated the PERT projection quite nicely.

PACKAGE DESIGN

The Parameters

The packaging design task centered in on two main areas:

- Developing compact electrical interconnection methods, both permanent and pluggable; and
 - Providing proper cooling, using standard available SLT gate hardware designed for logic applications.
- Standard SLT design, processes, and parts were used wherever possible for reasons of parts procurement and cost. Certain new design features were developed to meet the space requirements, reduce manufacturing and repair time, and improve reliability.

Diodes Mounted on Top of Array

The diode card which mounts on the top of the core array contains 98 diode packs of 4 diodes each for the

8K word version. These diode packs must be field replaceable. Normally such packs mount with the lead side down against a printed circuit card. To do so in this case would make field replacement nearly impossible because access to the back of the card would be necessary for soldering operations on the leads. Over 200 terminal welds joining the card to the array would have to be broken.

The diode replacement problem was solved by inverting the diode packs and forming the five leads back parallel to the side of the pack. When soldered into the card, a considerable portion of the lead is exposed, as can be seen in Figure 18. To replace a pack, one merely cuts the leads where they enter the old pack and leaves them standing in the card. The leads of the new pack are then crimped around the standing leads and soldered.

Batch Processed Weld Terminals Used

Another problem which was encountered in the design of the diode card was that of providing 216 weldable terminals on the periphery of the card. The usual design is to solder terminals into plated-through holes. New terminals were designed for batch process attachment without holes. They are made from a copper alloy brazing material. A strip of approximately 40 terminals is punched and formed into an S-like shape (Figure 19). The selvage strip is left on each end of the terminals for support during further processing. A portion of the terminals is dip-tinned with eutectic solder. The glass epoxy card has a matching set of printed circuit tin-lead plated lands on both surfaces along the edges. The strip of terminals is aligned to and pushed onto the lands. The edge of the card is then dipped in hot palm oil to reflow-solder the terminals to the lands. The terminal spring force holds proper location during the soldering operation. After attachment, the selvage strips are broken off at previously stamped score lines. The lands on the card provide support in excess of the bending strength of the terminals.

Pluggable Core Array Assemblies

One of the principal interconnection problems was that of making the core array pluggable to the SLT board. A pluggable array was required for separate testing and for ease of replacement. Approximately 180 connections are necessary.

A multisocket connector on the bottom of the array assembly would make all the connections at once. The idea was rejected because the insertion-extraction force would have been at least 80 pounds if contact springs giving sufficient contact pressure for a reliable low-voltage connection were used. A series of flat cables soldered to the bottom circuit board and individually plugged into the SLT board would have been bulky and introduced impedance and noise problems.

The connection system adopted maintained the required compactness, yet allowed for small groups of high-contact pressure connections to be made. It consists of a special printed circuit card assembly, to be discussed later, which is connected to the bottom of

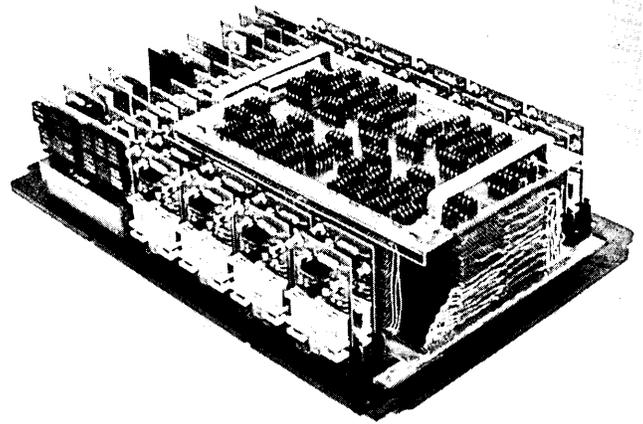


Figure 18. Core memory module (8K word, 18 bit, 2 μ sec). The array package and 38 small cards plug into a single SLT large board to make up the complete basic operating module.

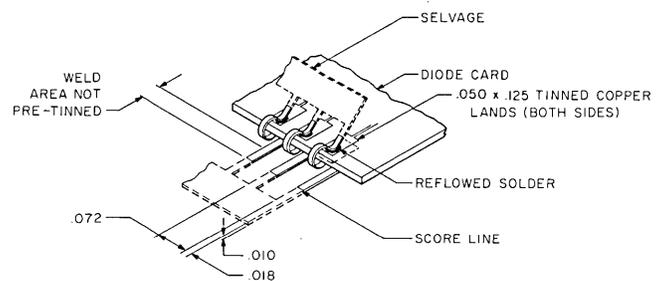


Figure 19. Weld terminal. Strips of stamped, formed, and tinned copper-brazing alloy terminals are pressed onto the edge of the circuit card. The card edge is then dipped in hot palm oil (525°F for 10 sec) to reflow the solder. Selvage strips are then broken off at score marks.

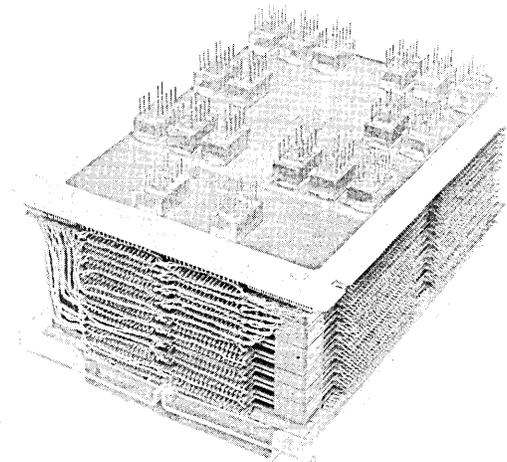


Figure 20. Bottom of 8K word array assembly showing I/O connector pins. Pins molded in plastic blocks are bonded to the circuit card assembly and soldered to upper surface of the card.

the core array. Gold-plated .0028 in. diameter contact pins supported by plastic moldings are soldered and bonded to the card (see Figure 20). When the array is mounted to the card side of the SLT board, as shown in Figure 18, the pins extend through the board and align with rows of the SLT board's gold-

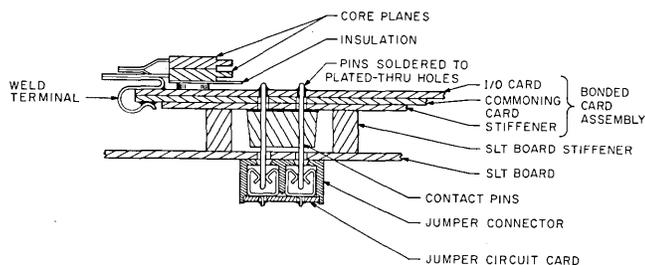
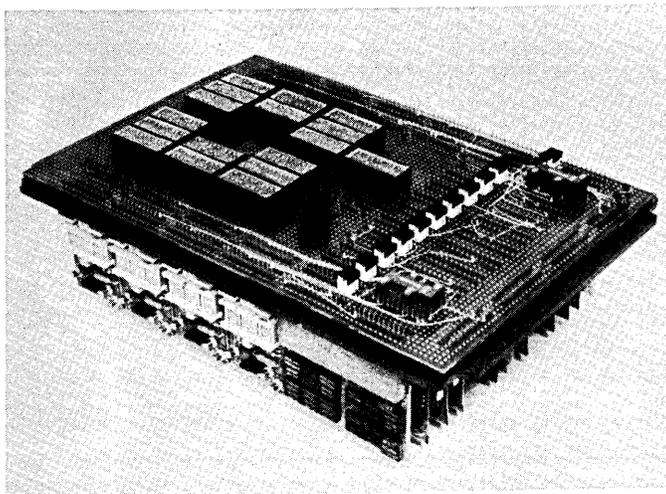


Figure 21 (a & b). Array to SLT board pluggable connection scheme. The array is mounted on the SLT board with I/O connector pins extending through clearance holes. A jumper connector connects groups of 10 pins to an adjacent group of 10 SLT board pins. Eighteen connectors make 180 I/O connections with high connector contact forces for reliability.

plated pins (Figure 21a). The ten array pins are then connected to the adjacent group of ten board pins, and thus to the board circuitry, by means of a jumper connector (Figure 21b). This connector carries twenty female contacts and a small jumper circuit card. Figure 21a shows connectors assembled to the back of the SLT board.

The standard SLT board has 24 contact pins in each card socket position. Four of the pins are assigned for voltages and ground. The following changes were then necessary in those socket locations to be used for array plugging:

- The voltage and ground pins were omitted to ensure against inadvertent shorting to the array.
- Ten of the remaining 20 pins were omitted, and 0.045 in. clearance holes were drilled in their place.

A highly reliable connection was obtained because each contact spring contacted the pins at two points with approximately 1 pound force. The insertion-extraction force of each jumper connector is 10-20 pounds. This provides more than sufficient retention during vibration. The contact spring chosen was previously approved for use on the SLT back panel pins which are squared for wire wrapping. By making the small modification of adding a tine for soldering to a plated-through hole in the jumper circuit card, considerable connector evaluation time and expense normally required for new connectors was avoided.

Four plastic blocks bonded to the SLT board provided screw retention points for the array.

Multifunction Circuit Card on Array Assembly

A special printed circuit card was developed for the bottom of the array. It provided:

- Connections and circuitry for commoning the drive lines
- A connection method for sense wires
- I/O connection circuitry from the drive and sense lines to the connector pins
- Mechanical support for the array

The card assembly (Figure 21b) consists of two glass-epoxy circuit cards and a plain glass-epoxy stiffener board bonded together. The upper card has I/O circuitry on its top surface only, which connects the edge terminal pads to the I/O connector pin plated-through holes. The second card has the drive line commoning circuitry etched on both sides. Around the edge of the card assembly, the S-shaped weld terminals are again used to make connection to the array. However, this time they also make the required interconnection between the I/O and commoning circuit cards. They eliminate the need for having plated-through holes to interconnect the bonded assembly.

Whereas the 2 "S" clips are on a .072 in. interval for drive line connections, similar clips, spaced on a .026 in. interval, are used as solder terminals for the sense wires. There are 6 sense wires (two groups of three twisted) from each core plane which are ultimately connected by printed circuitry to the I/O connector pins. After soldering, these terminals are painted with a flexible insulating compound to prevent shorting.

Cooling — A Critical Design Parameter

From a functional point of view, proper cooling of the array and circuits was the most critical packaging design factor. There are three principal requirements to be met:

- The temperature rise of the air passing through the array could be no more than 2°C or excessive skew would occur between the drive currents required at the extreme ends of the core plane.
- Adequate air flow past the two rows of circuit cards above the array had to be assured.
- The pressures and bulk air flow rates required to cool the memory had to be within the capacity of the standard SLT gate blowers.

To meet these requirements, the flow characteristics of the array were measured, and the pressure drop across the array needed to provide adequate flow was calculated. Then the bulk flow rate through the entire storage unit at that pressure drop was determined. The flow was found to be inadequate in some applications for cooling the additional logic boards located above the memory. Modification of the card cover was made to remedy this and to divert additional air flow to the cards in the second row above the array.

A flow chamber was used to measure the pressure drops across and flow rates through the core arrays. During the test, as in the actual storage unit, the spaces between core planes on the long sides of the array were sealed with rubber strips, and the upper and

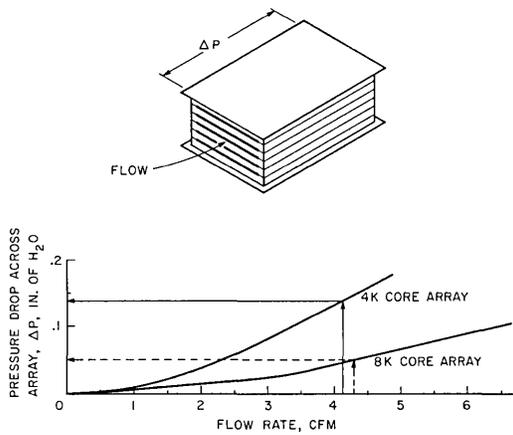


Figure 22. Pressure drop vs flow rate 4K and 8K core arrays.

lower surfaces were sealed with the respective circuit cards. Thus, all the air entered and exhausted through 0.030×3.45 in. slots between each pair of planes. The resulting curves are shown in Figure 22. Since the 4K core array is one-half the height of the 8K version, it has one-half the flow rate at any given pressure.

The maximum power dissipated in the $2 \mu\text{s}$ array occurs when all zeros are being written. In the 8K array it is 4.89 watts and in the 4K array 4.7 watts. Noting that the power dissipation of the 4K array is nearly the same as for the 8K, it is obvious that the highest pressure drop is required for the smaller size array in order to force more air through it.

To determine the required pressure drop, the flow required to give a 2°C temperature rise of the air was calculated (see Sidebar 3). Then the pressure drop was read from the flow curve, Figure 22. The minimum allowable pressure drop for the 4K array is 0.14 inches of water.

Making the worst-case assumption that only the array exhaust air is available for cooling the first row of cards above the array, the average bulk air velocity for the cooling of the cards was calculated to be 150 fpm. Since this approaches the minimum specified for cooling SLT cards, the precaution was taken to place only low dissipation gate and driver cards here.

The total air flow rate for the entire 8K storage unit was measured in a flow chamber. The 8K unit has more circuit cards and the higher core array. It therefore had the highest flow impedance and would be the one most likely to restrict flow to logic boards located above the memory. With a standard card cover which essentially sealed off flow over the top of the diode card, the flow rate was 70 cfm at a 0.16 in. of water drop across the array. By adding a bypass over the diode card as shown in the cross section of the memory in the gate (see Figure 23), the bulk flow rate met the required 100 cfm. Thus, the modified card cover is required.

Superimposing the storage unit flow curves onto the SLT gate blower characteristic curve, the standard blower was found to meet the cooling demands.

Sufficient pressure drop across the 8K array, as de-

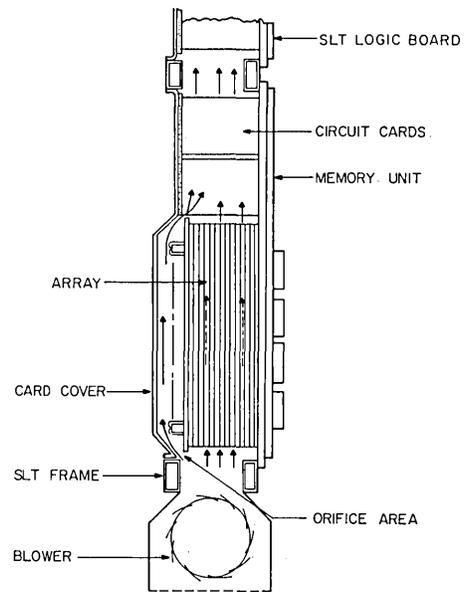


Figure 23. Air flow through memory with modified card cover. Air is bypassed over the array but the orifice area causes sufficient back pressure to force flow through the core array.

termined previously, is caused by the impedance of the orifice formed by the edge of the diode card and the gate hardware, a $0.25 \text{ in.} \times 5 \text{ in.}$ slot. Since the 4K array is lower, there is considerably more space between the top of the array and the card cover; thus, there is not sufficient impedance to cause the needed pressure drop. Therefore, the handle for the smaller array was designed as a baffle that extended toward the gate hardware to form an orifice similar to that formed by the 8K array.

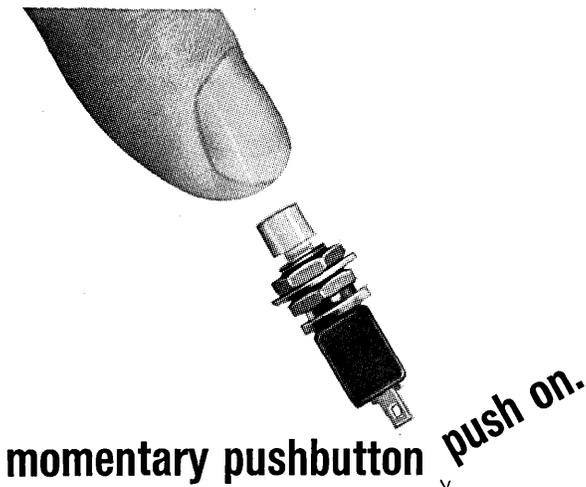
Cards directly above the array were adequately cooled by the air diverted toward the SLT board by the bypass in the card cover.

SIDEBAR 1

The SCHMOO

It has become traditional to refer to the operating margin plot in the Inhibit current versus Drive current plane as a SCHMOO. Reference 2 is an excellent source of detailed background on the subject. The term SCHMOO can be generalized to include margin plots in other planes also of importance to the core storage design. Figure 1a shows how two such plots are related to the traditional SCHMOO.

In the design of the units under discussion, the SCHMOO's in both the I_z vs $I_{x,y}$ plane and the sense threshold (V_{sa}) vs t_{strobe} plane were optimized quantitatively. This represents a distinct advance over the usual procedure in which only the I_z vs $I_{x,y}$ SCHMOO is actually optimized. Since the plots shown are all affected by a change in any of the four parameters, it is in general impossible to achieve the largest SCHMOO's in all plots simultaneously. As an example, let us see what we must do simply to maximize



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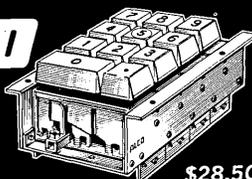
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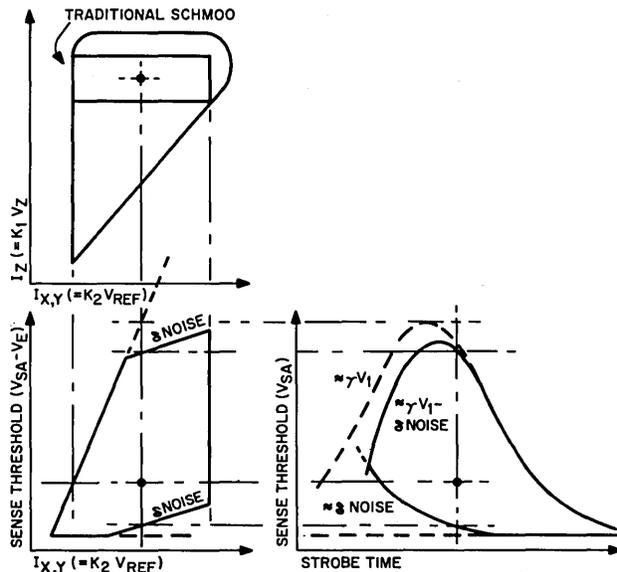


Figure 24. Relationship between SCHMOOs on $I_z/I_{x,y}$ plot, and V_{sa}/t_{strobe} plot.

the traditional SCHMOO. It may be seen from Figure 24 that lowering the V_{sa} operating point or moving the t_{strobe} operating point left will cause the left margin on the $I_z/I_{x,y}$ SCHMOO to move left. Thus the largest traditional SCHMOO will be achieved when V_{sa} is just above its margin. Obviously then, any slight change in either V_{sa} or t_{strobe} can cause an error (i.e., cause the SCHMOO to collapse completely).

It should be possible for the designer to calculate or measure the stability and repeatability of the operating points for the four critical parameters:

- (1) $I_{x,y}$
- (2) I_z
- (3) V_{sa}
- (4) t_{strobe}

He should then decide what margins he realistically needs in the $I_z/I_{x,y}$ and the V_{sa}/t_{strobe} planes.

A process of trial-and-error iterations can be used to zero-in on an operating point that meets the margin requirements on both SCHMOO's. It should again be stressed that this will not be the largest possible traditional SCHMOO. It will, however, yield the most reliable operation overall.

SIDEBAR 2

Statistical Design Program Using Monte Carlo Methods

The design program assigned values to all components, calculated the input signal required to produce a "ONE" at the output, stored the results, and repeated. Each time through, new component values were chosen randomly. After 1000 such runs, the cumulative results were plotted as a histogram which closely approximated the Normal Density Function. The 3σ points were taken as the limits of the "gray area." In other words, any input smaller than the lower 3σ point is a guaranteed "zero," any input greater than the upper 3σ point is a guaranteed "one," and any input between is indeterminate (see Figure

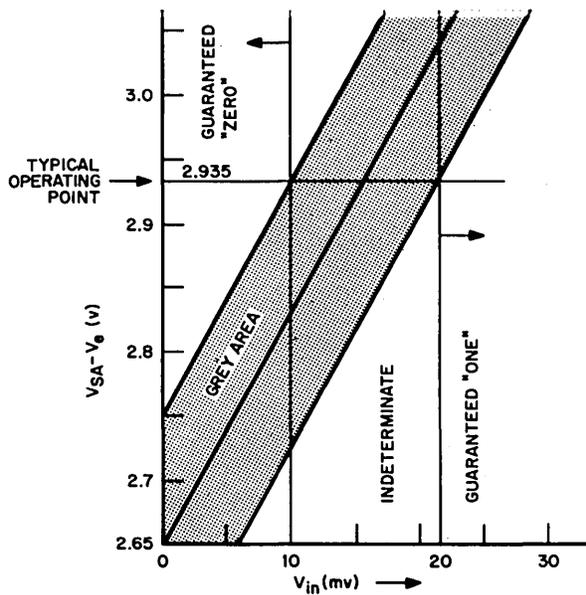


Figure 25. Illustration of statistical program using Monte Carlo methods.

25). Complete details of this powerful design concept are available in Reference 4.

SIDEBAR 3

Flow Rate Calculation

Knowing the allowable air temperature rise and the power dissipation within the core array, the required air flow rate through the array is

$$Q = \frac{.0316W}{\rho \text{ Cp } \Delta T}$$

where:

Q = Flow Rate, cu. ft. per min.

W = Power dissipated, watts.

ρ = Density of air at standard conditions, .075 lb/cu ft.

Cp = Specific heat of air at standard conditions, .24.

ΔT = Temperature rise, °C.

The constant converts units from the basic thermodynamic equation to this more usable form.

The flow rate required for a 2°C rise through the core array is,

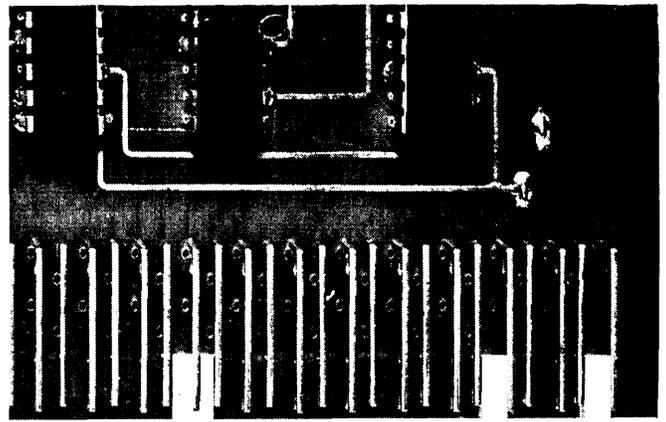
$$Q = \frac{.0316 (4.7)}{.075 (.24) 2} = 4.1 \text{ cfm}$$

From Figure 22, the pressure drop required to force this flow through the array is .14 in. of water.

For the 8K core array, W = 4.89 watts, giving a Q of 4.3 cfm and a pressure drop of .05 in. of water.

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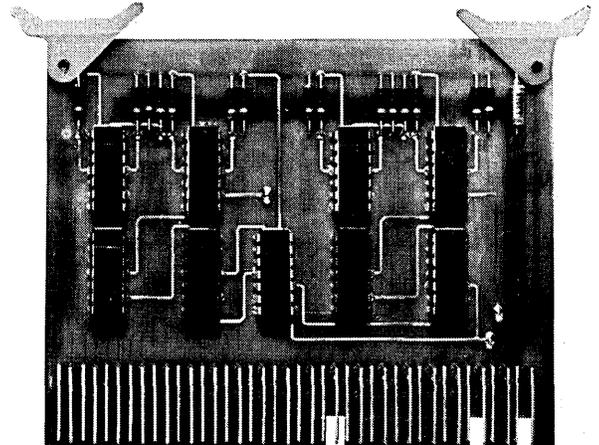
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This non-incremental input-output mechanism receives, partially processes and encodes data for transfer between transducers and real-time digital computers. It is particularly well suited for performing high-speed calibration and redundancy reduction on data received as phase modulation on carrier wave forms, and for presenting the partially processed data in convenient whole word format to the computer.

A HIGH-SPEED GENERAL PURPOSE WITH REAL-TIME COM

Real-time data acquisition and control systems incorporating a general purpose digital computer (GPC) will be considered for this discussion to be composed of three parts: transducers and transmission paths, an input-output mechanism (I/O), and the GPC. The transducers and transmission paths considered in particular are those resulting in the desired data being phase-modulated on carrier waveforms. This type of phase-encoded information may be received from a variety of sources, among which are shaft-angle resolvers with sine-cosine excitations, and Doppler navigation systems. The primary focus of attention in this article is a new I/O which can receive the phase-modulated waveforms directly, perform a variety of processing functions on the raw data in its phase-modulated form, and present the processed data in a convenient binary format to the GPC. The new I/O can process data from a number of sources in parallel at relatively high speeds, thereby leaving the GPC time for monitoring, adaptive parameter adjustment, and other sophisticated decision and control functions. Similar techniques utilizing different phases of the computer clock signal permit the GPC to generate digital and/or analog commands to transducers via the I/O.

Some examples of transducers and transmission links are presented briefly as background material and motivation for a discussion of the I/O itself. The operation of the I/O is then discussed in detail with reference to a practical system for obtaining and processing whole-angle data from a multi-speed shaft-angle resolver and, in more generality, with reference to a wide variety of signal sources producing phase-modulated information.

Ease of performing analog/digital conversion (and its inverse) with phase information is the key element in the I/O discussion. As a result, the real-time control problem and hybrid computer problem may be considered as essentially the same time shared computer problem, and the traditionally complex I/O problem of tying analog elements to the GPC may be solved in the same simple way.

Several significant improvements can be made in computer usage by the proper design of an I/O. In particular, the programming can be simplified, more useful computing can be carried out in a given time interval, and greater system flexibility can be achieved.

TRANSDUCERS AND TRANSMISSION LINKS

In preparation for the detailed discussion of the I/O, some examples of transducers and transmission links producing phase-encoded information are given. These examples serve to introduce some simple but useful mathematical notation and to provide a physical interpretation of the origin and meaning of the phase-encoded waveforms that are central to the discussion of the new I/O. The examples also serve to introduce the ideas that there may be several information sources (either independent or dependent) operating simultaneously and that the information can conveniently be multiplexed without altering the phase-encoding. The new I/O has the natural capability of processing the phase-encoded information from several sources simultaneously.

A typical example of a transducer producing phase-modulated information is the shaft-angle resolver shown in Figure 1. These transducers are found in equipment ranging from inertial to machine-shop. The input signals e_1 and e_2 are any periodic waveforms with fundamental components $E \sin 2\pi ft$ and $E \cos 2\pi ft$, respectively. The resolver produces an output

$$e_0 = e_1 \cos \phi + e_2 \sin \phi \quad (1)$$

where ϕ is the mechanical resolver angle. Hence the fundamental component of the output is

$$\text{fund}(e_0) = E \sin(2\pi ft + \phi) \quad (2)$$

which is linearly phase-modulated by the resolver angle. Henceforth, we shall assume for convenience that the input waveforms are square waves with frequency f and phase angles 0° and 90° ; these are denoted by $f \angle 0$ and $f \angle 90$, respectively, as shown in Figure 1. Implicit in this notation is the assumption of a reference zero phase angle, which we shall assume is established by a reference clock. [A clock is a high-

INPUT-OUTPUT MECHANISM PUTTING CAPABILITY

KENNETH FERTIG
DUNCAN B. COX, JR.
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frequency oscillator followed by a (typically binary) countdown chain from which several signals with locked frequencies and phases may be obtained.] The output of the resolver we shall denote by $f \angle \phi$ to indicate the fundamental component of the waveform is of frequency f and phase angle ϕ .

Often an m -speed resolver, yielding an output $f \angle m\phi$, may be used with a one-speed resolver on a common shaft to assign roughly equal parts (in the

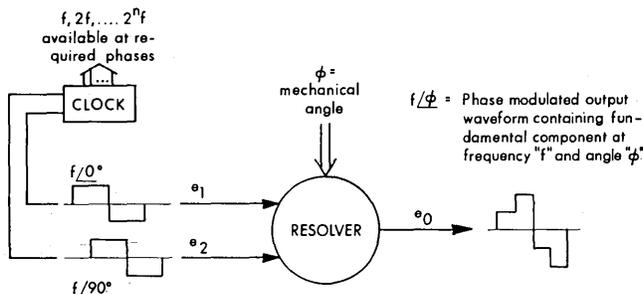


Figure 1. A shaft-angle resolver with phase-modulated output.

sense of double precision) of the desired angle information to each of two modulated waveforms. (An m -speed resolver has windings with m pole pairs so that its output phase angle passes through 360 degrees when the mechanical shaft rotates through 360/ m mechanical degrees.) Where there are several resolvers, their outputs may be time multiplexed over a common transmission path with, e.g., four samples of each waveform taken per cycle, without distorting the phase of the fundamental component.¹ Another possibility is to effect frequency multiplexing by choosing the excitation frequencies for different resolvers as binary multiples, e.g., f , $2f$, $4f$, etc. Of course, both time and frequency multiplexing may be used simultaneously. In that case the outputs of the time multiplexer would be several zero-order-held waveforms, each resembling the resolver output waveform shown in Figure 1, but at different excitation frequencies. These phase-modulated outputs would be received by the new I/O. The frequency demultiplexing of the information is auto-

matically achieved in the new I/O because an integral part of the new I/O is a set of phase-locked loops.

Other examples of transducers yielding phase-modulated information abound: Loran, Doppler radar, sonar, etc. In these systems phase shift data correspond to measurements of distance. Two or more carrier frequencies (often multiplexed on a third) are often used to measure the same distance variable. This tech-

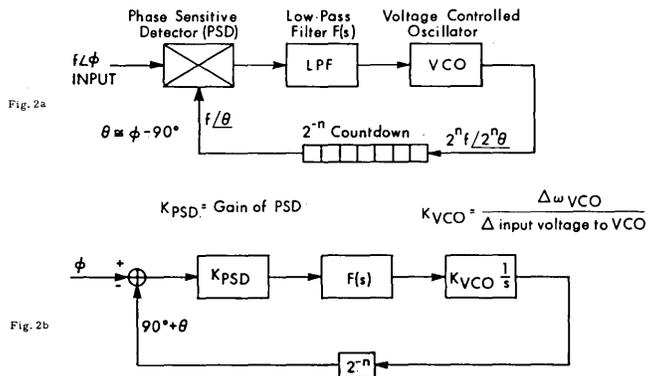


Figure 2. The phase-locked loop.

nique is completely analogous to that of using one-speed and m -speed resolvers to measure a common shaft angle.

THE NEW I/O

A basic element in the new I/O is the phase-locked loop shown in Figure 2A. (For good sources of information on the behavior, design, and use of phase-locked loops the reader is referred to Tausworthe² and Gardner.³) It consists of a phase-sensitive detector (PSD), a low-pass filter (LPF) with transfer function $F(s)$, a voltage-controlled oscillator (VCO) (any simply controllable oscillator is usable, including digital oscillators made by DDA techniques), and a binary n -stage forward counter (countdown). The countdown output $f \angle \theta$ is a square wave which in normal operation is locked in frequency and phase with the funda-

mental component of the input $f \angle \phi$ to the phase-locked loop. Ideally, θ is equal to ϕ plus 90° ; careful loop design can insure that this relation is maintained reasonably well, in many cases to within a small fraction of a degree. The PSD can be a simple switching modulator that multiplies the input waveform by $+1$ or -1 , depending upon the state of the countdown output. The LPF extracts the average value of the PSD output and, in its most general form, performs several other filtering functions. The basic phase-locking operation of the loop depends upon the action of the PSD in producing an error signal to increase or decrease the frequency of VCO oscillation in order to drive the phase error to zero. This mechanism is illustrated by the block diagram in Figure 2B. Because of the presence of the n -stage countdown, the VCO frequency is 2^n times the input frequency. Loops of this type have been operated satisfactorily with VCO frequencies as high as 5 mc and with as many as ten countdown stages. Standard heterodyning techniques can be used to accommodate input frequencies that are impractically high for the basic loop shown in Figure 2A.

The effect of phase-locked loops is to create a set of square waves, each wave being the output of one stage of the countdown in Figure 2A, that track the phase ϕ of the fundamental component of the input waveform. The phase angle θ of this set with respect to a reference clock waveform $f \angle 0$ is easily determined by the process diagrammed in Figure 3. At the instants when the clock waveform $f \angle 0$ changes states in the positive going direction a determination of the states of each of the countdown waveforms is made. Knowledge of whether $f \angle \theta$ is up or down narrows the uncertainty in the angle to a 180° region; knowledge of whether $2f \angle 2\theta$ is up or down further narrows the uncertainty in the angle to a 90° region; etc. This process, referred to hereafter as "strobing the countdown waveforms with the clock waveform," results in a unique synchronous binary encoding of the angle and is the heart of the new I/O. A functional implementation of the strobing technique to measure a resolver angle is diagrammed in Figure 4. (Note that the process could be modified to obtain angle encoding by having the signal $f \angle \theta$ from the phase-locked loop strobe the signals in the clock countdown, in which case the phase-locked loop would be acting as a filter and zero-crossing detector. However, with this arrangement, the precise times at which the data strobes occur would not be known a priori, and this uncertainty could be an important disadvantage when precise dynamic measurements are required.

The strobing process for obtaining binary encoding of phase angle can easily be extended to the case where there are two signals available corresponding to a common measurement variable, as from one-speed and m -speed resolvers on a common shaft. The one-speed signal $f_1 \angle \phi$ and the m -speed signal $f_2 \angle m\phi$ can, of course, be encoded separately, each with its own phase-locked loop strobed from a common clock. However, with this arrangement, as with any independent encoding scheme, unavoidable misalignment between the one-speed and m -speed data will cause, for certain angles, an inconsistency in the binary encoded data. An example of such data from 1-speed and 16-speed

resolvers on a common shaft is shown in Figure 5. The inconsistency lies in the fact that the overlapping bits do not agree. In this case it is necessary to establish the direction of phase misalignment and to add or subtract a unit from the coarse word accordingly. However, with the new I/O a bit can be added to the coarse word merely by delaying the coarse-word strobe. Hence, an efficient and easily implemented technique

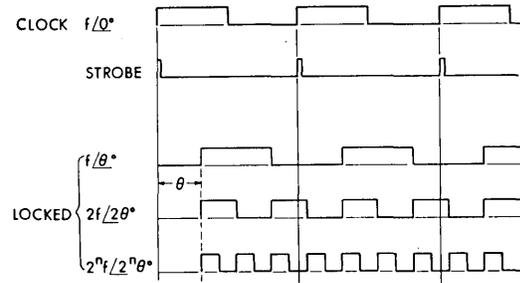


Figure 3. Strobing waveforms.

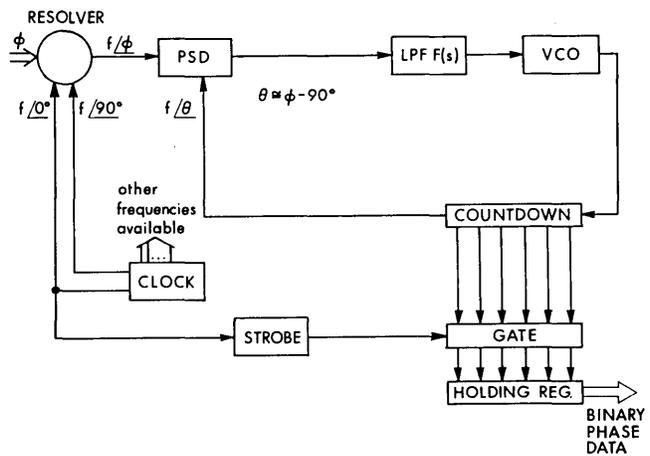


Figure 4. Strobing technique to obtain binary phase output.

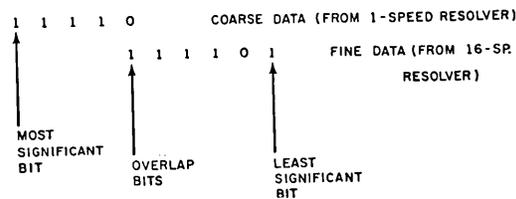


Figure 5. Data misalignment.

for data alignment is as follows:

Introduce a phase misalignment in the waveform $f_1 \angle \theta$ from the countdown of the coarse-data loop such that the waveform corresponding to the least significant bit from that loop lags the waveform corresponding to the most significant bit from the fine-data loop by about 90° . Strobe the countdown of the coarse loop as usual (on the same clock signal as for the fine loop) if the overlap bits agree. Otherwise, delay the strobe of the countdown of the coarse loop until the overlap bits do agree. (Clearly, this is not the only possible method of data alignment. It bears similarity to a double-precision operation involving a carry bit.)

Introduction of the correction signal for misalignment angle is easily accomplished by adding a small fixed voltage to the signal at the output of the PSD

of the coarse-data loop. Then the indicated strobing scheme results in whole-word data being obtained jointly from the one-speed and m-speed phase-modulated signals.

The elementary I/O as described has been constructed and operated satisfactorily to obtain 13 bits of whole-word data at a 1 KC synchronous strobing rate from a 1- and 16-speed shaft-angle resolver.

COMPARISON WITH CONVENTIONAL ANGLE-MEASUREMENT TECHNIQUES

The elementary I/O is in essence a new and powerful technique for measuring and encoding phase angles of time waveforms. On this basis alone, without consideration of the additional processing and computing capabilities, the elementary I/O offers several advantages over conventional phase measurement techniques.

Almost all phase measurement techniques require the conversion of the phase-modulated waveforms to rectangular or square waveforms which are in turn used directly for timing measurements. In the new I/O, as often in the field of radio telemetry, the conversion is made through the use of phase-locked loops. In conventional systems for measuring resolver angles the conversion to square waves is done through the use of zero-crossing detectors, perhaps preceded by band-pass filters. The phase-locked loop has a superior capability to discriminate against noise (thereby avoiding totally false readings due to multiple false triggering of level detectors) and, in addition, avoids errors that occur as a function of frequency shift in direct transmission through a band-pass filter. The new I/O broadens the area of application of phase-tracking techniques long known in the communication field.

Conventionally, the timing measurements on the square waves are performed by either of two basic methods: One of the methods is to use a linear analog phase detector to determine the phase of the zero-crossing detector output with respect to a clock waveform. The phase detector output must then be filtered and A/D converted to obtain a numerical representation of phase angle. This method relies strongly on the linearity of the phase detector, and results in significant dynamic errors due to the filter. The new I/O offers the advantage of utilizing a nulled phase detector, which need not be linear, and the advantage of greatly improved dynamic performance. It also has the advantage of relative ease and simplicity (and therefore economy of A/D conversion. The other conventional method of processing the zero-crossing detector outputs is to use their rising and/or falling edges to start and stop a counter that is driven by the reference clock. The final counter outputs (at variable clock times) are the encoded phase angle data. This method is the open-loop counterpart to the strobing method of A/D conversion used in the new I/O. In the new I/O the counter is incorporated in the phase-locked feedback loop and numerical angle data is obtained at known clock times by the strobing process. Hence, the elementary I/O combines the signal-tracking capabilities of the phase-locked loop with the capability of synchronous angle encoding by the strobing process.

The new I/O has the additional advantage that it can easily be generalized to perform a wide range of simultaneous signal processing tasks that cannot be performed as effectively by conventional schemes.

PROCESSING AND COMPUTING CAPABILITIES OF THE NEW I/O

Sensor as Part of System Memory

One important capability of the new I/O is the ability to provide synchronous whole-word data from a single or multi-speed source without the requirement of memory registers. After momentary interruptions in power sources, communication channels, etc., the current data word is completely restored. In a very real sense, the analog data source — e.g., the resolver — can function as part of the system memory and is an adjunct to the computer memory. Similarly, the I/O is akin to an addressing mechanism for the system.

Equally important is the capability to perform simply and rapidly a useful set of computing (data processing) functions, which will be enumerated presently. When a multiplicity of data sources are present these computations are performed simultaneously by the individual sections of the I/O, and the processed data can be addressed serially, randomly, or otherwise, by the GPC and/or by an off-line processor. In this manner the new I/O can take on a rather large real-time computing load which otherwise would have to be assigned to the GPC.

Filtering

One type of data processing function naturally performed by the I/O is filtering. Because the phase-locked loops are tracking filters with limited bandwidth, they serve not only to discriminate against electrical noise in the transmission path, but also to smooth the angle data itself. This smoothing function is particularly useful in the cases where the angle variations to be "smoothed out" are relatively rapidly varying. In those cases real-time smoothing by means of a GPC would require computations to be performed at a frequency more than twice the highest important frequency component in the power spectrum of the angle data. The new I/O performs the filtering operation automatically on the phase-modulated waveforms and thereby relieves the GPC of a rather large computing load that it is generally not designed to handle in the first place. The general purpose computer remains free to alter the filtering time constants according to either a programmed or adaptive control law by altering the parameters of the low-pass transfer function $F(s)$.

Time-Derivative Data

Often, particularly when the data is being used in a control loop, it is desirable to obtain the time derivative of the variable being measured. When the data represent mechanical angle the GPC is often assigned to compute the derivative, a task which it cannot efficiently perform at high speed. The new I/O can provide the time-derivative (angular velocity) data di-

rectly in the form of a shift in the VCO frequency from its nominal value $2^n f$. Because both the frequency shift and the nominal frequency of the transmitted phase-modulated signal are magnified in the phase-locked loop by the factor 2^n (where n is the number of countdown stages), the determination of the shift can be made both accurately and rapidly. Many convenient and practical methods of measuring frequency shifts have been developed over the years for Doppler navigation, FM data transmission, etc. Any of these can be used to obtain the encoded time-derivative data. As an example, Figure 6 shows an analog frequency-difference detector followed by an A/D converter to provide encoded time-derivative data to the GPC. An alternate rate signal may be derived from the error

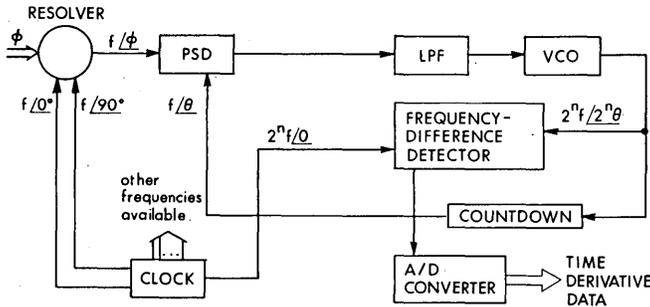


Figure 6. The generation of time-derivative data.

signal to the VCO in the phase-locked loop and the choice is a matter of signal-level and hardware considerations.

Compensation of Periodic Errors

Another type of computation that the new I/O can usefully perform is the removal of periodic instrument errors. Ideally the electrical phase angle of the transmitted data is linearly proportional to the quantity to be measured, e.g., shaft angle. Departures from linearity are objectionable and are often called "errors." However, the accuracy of the transducer may be considerably greater than its linearity, in which case it is desirable to remove the known non-linearity from the data numerically or otherwise. Although this is an extra and perhaps unwieldy task in real time for a GPC, the new I/O handles the task readily in the following manner: Suppose, for example, that the lowest-frequency signal $f \angle \theta$ in the phase-locked loop in Figure 2a is multiplied (an "exclusive-or" operation on square waves) by the signal $f \angle \theta$ from the clock. The average value of the product is a triangular function of the angle θ and, hence, of the angle ϕ . If this product signal is added to the signal at the output of the PSD in the phase-locked loop, the output data angle θ will be displaced from the input data angle ϕ by the triangular correction function (here assumed to be suitably small so that the effective gain of the PSD can be considered fixed). Similar correction functions can be generated with different periods and phase angles as a function of θ by using different frequencies and angle references in time as indicated in Figure 7. By using a set of correction voltages generated in this manner, essentially any nonlinearity can be compensated for if it is a known periodic function of ϕ . In this manner the binary angle (and angular

rate) data is compensated for before delivery to the GPC. The latter remains free, for example, to oversee the correction process, perhaps to set adaptively the correction parameters, e.g., K_c and a in Figure 7, which can be temporarily or permanently stored in the I/O itself.

In Figure 7 the square wave $m\phi \angle m\theta$ is shown as an output from a frequency synthesizer. The function of the synthesizer in this case is to take the waveforms $f \angle \theta, 2f \angle 2\theta, 4f \angle 4\theta, \dots, 2^n f \angle 2^n \theta$ from the phase-locked loop counter and generate square waves at any desired missing integral multiples of f , such as $3f \angle 3\theta$. This can be accomplished, with phase information preserved, by a novel technique, developed at MIT/IL, for frequency heterodyning. (The technique, which is akin to single-sideband operations and results in a flexible frequency synthesizer,⁴ was developed by Edmund Foster and Kenneth Fertig.) The function accomplished by the heterodyner is diagrammed in Figure 8.

Correction of Phase Delay as a Function of Frequency

In some resolver applications, energy-storage mechanisms associated with the transmission path can introduce a phase shift into the carrier waveform as an

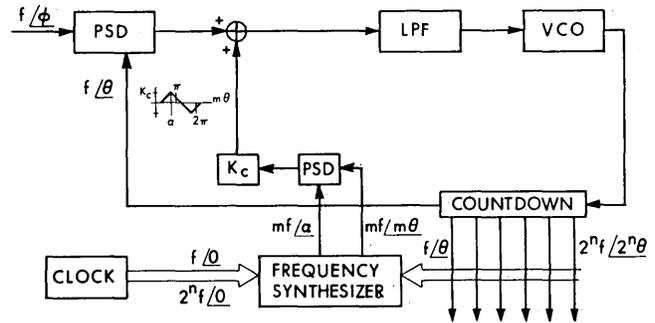


Figure 7. Correction for periodic instrument errors.

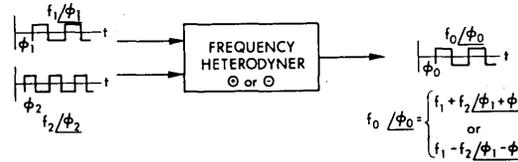


Figure 8. Fundamental element of frequency synthesizer.

approximately linear function of frequency. The new I/O can easily compensate for this phase shift, which can be considered as a dynamic phase error, by adding a small voltage from the frequency-difference detector to the voltage from the PSD as shown in Figure 9. This type of correction, not easily handled by the GPC, would be particularly valuable in applications where instantaneous angle data is desired from a resolver rotating at high angular velocities.

Redundancy Reduction

In many applications, the behavior of the phase and frequency of the incoming waveform to the I/O is approximately known *a priori*, and the real data of interest is the departure of the actual data from the nominal data. Examples of this situation arise in a

number of Doppler-type navigation systems when the approximate course of the vehicle is known from other sources of navigation information. In such cases it is useful to be able to reduce the computing load of the GPC by subtracting the expected data in real time from the actual data. This is easily accomplished in the new I/O.

Suppose that the expected Doppler shift is $K_1 f$ cps, where K_1 is some rational number less than unity. This can be removed from the data by using a strobe waveform

$$f \angle 0 \oplus K_1 f \angle 0 = (1 + K_1) f \angle 0 \quad (3)$$

where \oplus indicates the heterodyning operation in Figure 8. If this strobe signal is used, and if the actual data is equal to the expected data, the strobed binary angle is a fixed number. Small deviations in the actual data from the expected data result in slowly varying binary data. The GPC in turn has to process only the slowly varying data, which contain the significant information, and can ignore the rapidly-varying unprocessed data containing redundant information on the already-known nominal path. By using the strobe waveform in place of the clock-waveform as an input to the frequency-difference detector, the redundancy reduction of the time-derivative data is also effected.

The I/O can perform frequency correction also as a function of the frequency of the incoming signal. This is accomplished by letting the strobe waveform be

$$f \angle 0 \oplus K_1 f \angle 0 \oplus K_2 f \angle K_2 \theta \quad (4)$$

Figure 11 shows a functional diagram of the new I/O with provision included for the computing options mentioned thus far. By placing the phase-preserving frequency synthesizer under GPC control any schedule

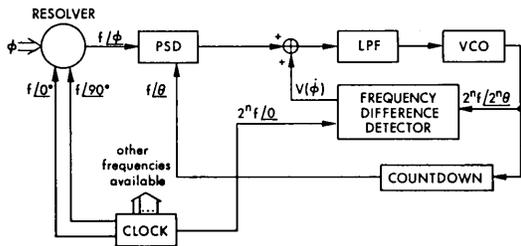


Figure 9. Phase correction as a linear function of frequency.

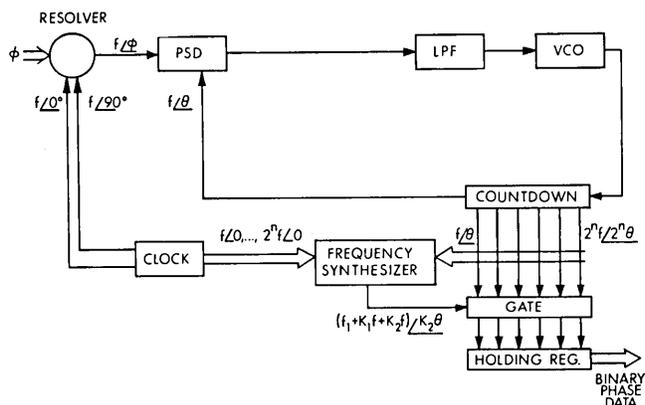


Figure 10. Method of correcting frequency as a function of frequency.

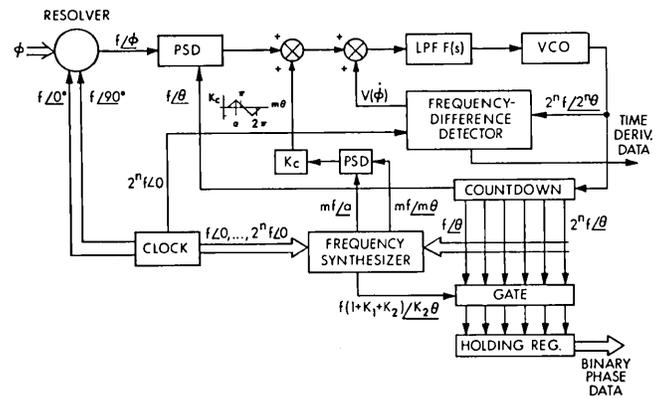


Figure 11. Composite correction mechanism. The GPC controls $F(s)$, the frequency-difference detector, and the frequency synthesizer.

of expected data may, in principle, be used in the redundancy reduction process. Moreover, the GPC may be used to perform a monitoring function to determine the extent of redundancy and error reduction and to modify the synthesizer accordingly.

Other Computing Capabilities

The computing capabilities discussed in the foregoing are substantial but rather obvious once the basic operation of the new I/O is understood. Many other types of computations can be performed, and it is likely that those mentioned are only the beginning of a long list. Some of the other possibilities presently under investigation are summarized briefly below:

- 1) Ladder networks can be used in conjunction with the holding register to form linear and transcendental functions of the strobed angle data.
- 2) A countdown in one phase-locked loop can be strobed with a signal from another phase-locked loop to obtain relative-angle data.
- 3) Digital-differential-analyzer ideas can be incorporated to allow products of data words to be obtained.
- 4) Generalized hybrid computation may be considered where the ladder networks of 1) are excited by voltages related to real signals. Depending upon where the feedback loop is closed with respect to input and ladder output, analog multiplication, division, etc., can be performed as shown in Figure 12. If the ladder is on the countdown, a continuous presentation of data on a modified carrier may be obtained. By using the multiplication and data-storage capabilities, correlation of data can be performed.
- 5) By incorporating logic circuitry in the clock to allow generation of waveforms at independently controllable phase angles, GPC outputs may be phase encoded for subsequent processing by the new I/O. The I/O could present the results in digital, analog, or phase-encoded form.

Generalization: Instrument Servo and New I/O

The properties of the new I/O result from the action of the VCO in the phase-locked loop. The properties of the instrument servo of prehistoric analog computer days were largely dependent on the motor which acted as an integrator in the sense that a voltage applied to the motor control winding resulted in an

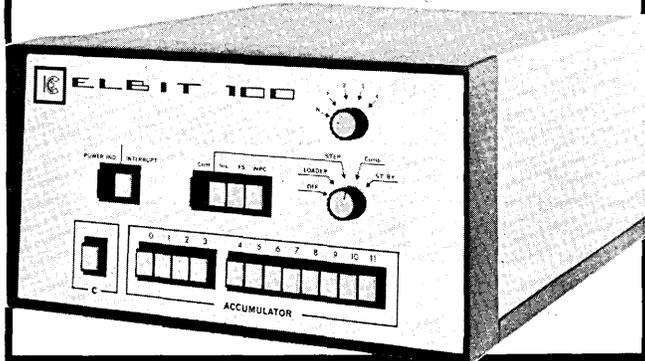
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angular velocity, the integral of which is angle. Similarly, the voltage input to a VCO controls frequency whose integral is phase. In the old servo, the motor shaft could be loaded by tachometers, resolvers, synchros, potentiometers, etc. In our phase-locked loop, the VCO and counter may be loaded by FM detectors (note that the loop error signal is the Doppler shift), ladders, etc., as shown in Figure 12. Clearly, the similarity between the phase-locked loop and the instru-

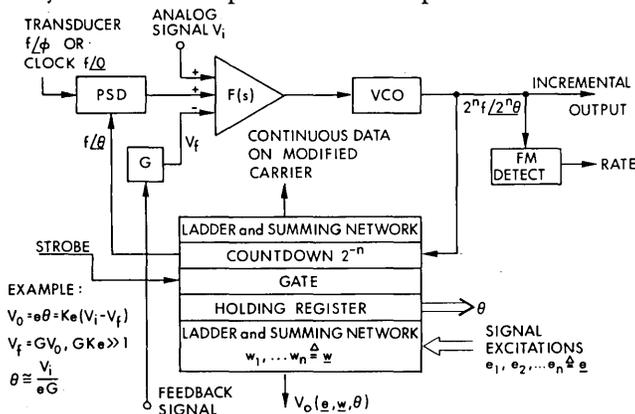


Figure 12. Hybrid computer element.

ment servo is being stressed. From this similarity, all of the computing capability obtained previously with the instrument servo may be obtained from the electronic servo — the phase-locked loop.

As a result of the preceding discussion, a further generalization may be made which is incidental to the discussion of I/O. The phase-locked loop is really an

accurate operational amplifier and the technique may be used to make a family of analog computing elements, servos, etc.

Hardware Implications

The circuit elements that are used to make a phase-locked loop lend themselves to microminiaturization. Developments in integrated circuits and large scale integrated arrays make hardware I/O improvements attractive.

Further, examination of existing I/O's for several real-time computer/control systems shows that the system designers, in order to alleviate the computer data-processing load, have placed in the I/O adders, forward-backward dual-rank counters, A/D converters, etc. The phase-locked loop, utilizing, a forward-only counter, etc., appears to lend itself to a building block concept that represents no increase in hardware but rather a regrouping and a considerable increase in flexibility.

CONCLUSION

A simple high-speed I/O with real-time computing capability has been described. The I/O is particularly well suited for performing high-speed calibration and redundancy reduction on data received as phase modulation on carrier waveforms, and for presenting the processed data in a convenient whole-word binary format for further processing by a general purpose computer. The I/O is non-incremental in nature and, hence, is completely self-restoring after momentary equipment interruptions and can be adaptively manipulated under general purpose computer control.

The new I/O is a step in the direction of freeing a general purpose computer in a real-time measurement and/or control application from high-speed but routine data-reduction tasks (for which it is not well suited) to perform computation, sophisticated monitoring, and adaptive adjustment tasks (for which it is particularly well suited). Although the examples have been about inputs to the general purpose computer from continuous sources, the techniques described would apply to the generation of outputs from the general purpose computer that commands or controls some element of a system.

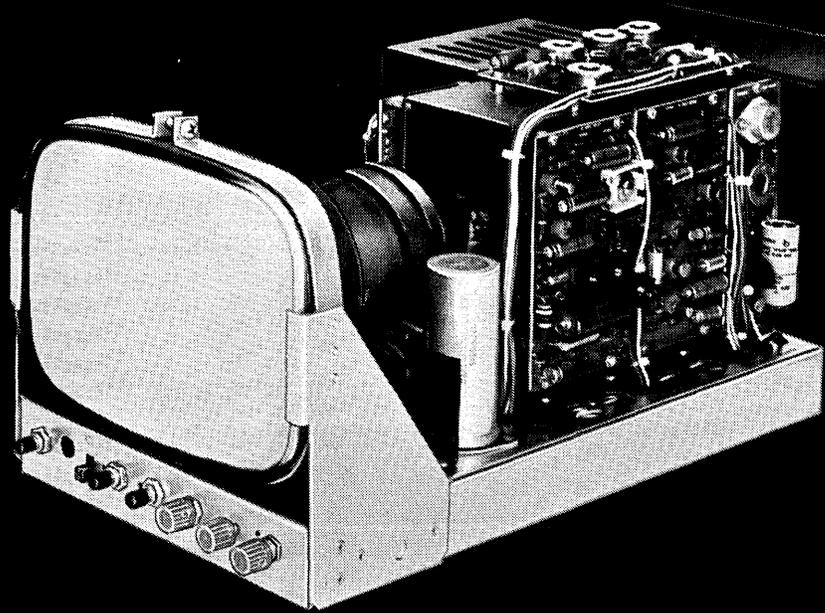
The concepts of I/O have been generalized to include the general problem of analog computation and simulation and to lead naturally to hybrid computation techniques.

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4. Foster, E., "A Circuit to Perform Frequency Addition of Square Waves," Master of Science Thesis, Massachusetts Institute of Technology, MIT Instrumentation Laboratory Report T-475, Cambridge, Massachusetts, January 1967.

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CIRCLE NO. 59 ON INQUIRY CARD

Filling the gap between the teletypewriter and expensive, refreshed, CRT displays, this terminal, developed for computer time sharing, provides alphanumeric and line drawing capability at moderate cost.

A NEW DISPL

Graphic Displays in Time-Sharing

The introduction of time-sharing computers has led to a new surge of interest in graphic display terminals. This is quite natural since time-sharing provides an economic, convenient manner of getting the on-line computational capability needed to make displays useful. By the same token, graphics is a natural means of communication with a computer which is quicker and more expressive than the pure text offered by standard teletypewriter terminals or character-only displays. The economic justification for time-sharing over batch processing is that it utilizes the programmer's time better and provides new ways of doing problems. This same justification can be applied to employing graphics in time-sharing. At the price of an increase in terminal cost the user is able to communicate in a more meaningful manner and problems can be attacked in new ways.

Unfortunately, graphic displays have been too expensive to justify their use in most commercial environments. Typically, graphic display console prices start at \$30,000 and go up to \$100,000 and more. For time-sharing systems the trend is toward coupling these displays with their own small general purpose computer. This brings the minimum cost per terminal above \$60,000. Small computers have come into popularity to provide display memory and the real-time dynamic response normally associated with graphic consoles. In order to alter displayed pictures fast enough to give the illusion of continuous movement, response times in milliseconds are required, which few time-sharing systems can provide. It has become a popular misconception that a graphic display must be this dynamic to be useful.

Experience at Project MAC has shown that it would be highly valuable if the computer could simply make "static" graphic drawings at the user's console. With this ability, circuits can be easily depicted, flow diagrams drawn, graphs plotted. In virtually every intellectual endeavor, line drawings help communication. There are few applications of time-sharing computers where an ability to portray data graphically

could not be helpful, whereas the number of applications that require "moving pictures" is very small. Incremental x,y plotters have been used to provide this graphic capability but their slow plotting rate makes them unsatisfactory for on-line operation.

To this end the Display Group of the Electronic Systems Laboratory of M.I.T. has designed for Project MAC a low-cost CRT terminal for computer time-sharing capable of rapid alphanumeric and graphic display, but without 'dynamic' capability in the sense defined above. A basic assumption of the design of this unit was that the communication link to the time-sharing system would be the voice-grade switched telephone line. This assumption was made because the phone system represents the only communication network that is widely available, relatively inexpensive, and convenient to use. The narrow bandwidth of the phone line requires that the display memory be in the terminal itself. By not attempting to provide dynamic graphic display, it was possible to utilize image storage techniques for the terminal memory and thereby achieve significant cost savings in the terminal electronics while at the same time enhancing the quality of display and the quantity of data that can be presented, as compared to refreshed displays. The narrow bandwidth of the telephone line also requires that data be in a highly coded form in order to achieve satisfactory plotting speed. It was thus necessary to include both symbol and vector generators in the terminal and to devise a low-cost realization for these functions. The resultant terminal is called the Advanced Remote Display Station (ARDS).

An ARDS unit has been operating on Project MAC's time-sharing system for several months. The unit appears to the user's programs as just another teletypewriter, with the special property of being able to plot pictures. This simple interface allows all programs written for teletypewriters to run unchanged. To the person operating the ARDS terminal, text is plotted about 10 times faster than on a teletypewriter which is a great improvement. The only other operational difference is the lack of paper copy falling to the floor.

AY TERMINAL

ROBERT H. STOTZ

Electronic Systems Laboratory
 Department of Electrical Engineering
 Massachusetts Institute of Technology

Since this article was written, Mr. Stotz has joined Computer Displays, Inc., Waltham, Mass.

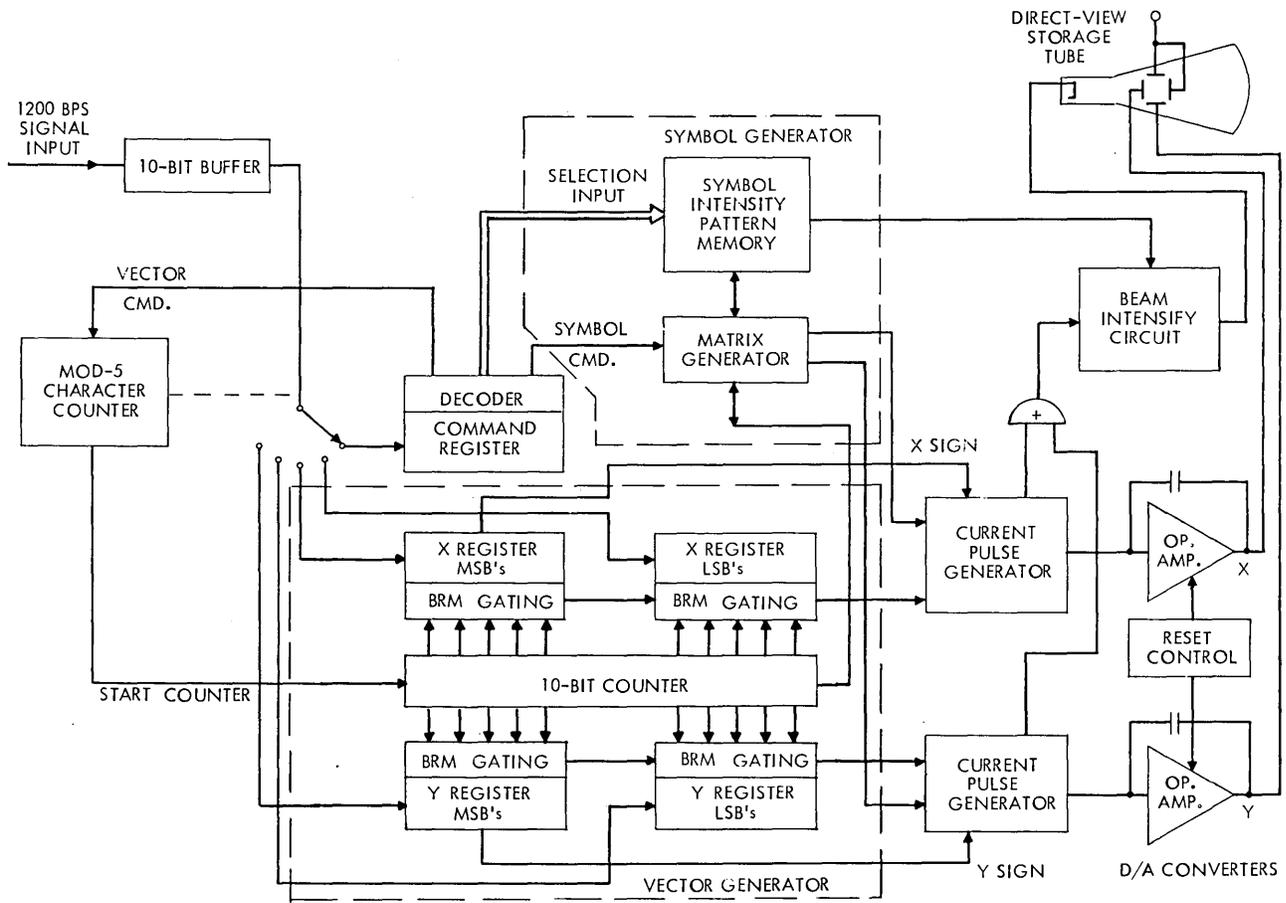


Figure 1. Block diagram of ARDS controller.

ARDS Hardware

ARDS is a complete, remote graphic station. It consists of three basic sections: a controller, a display unit, and a keyboard. The controller contains the logic for decoding bits from the input line or the keyboard, a symbol generator and a vector generator. Figure 1 is a block diagram of the ARDS controller.

The display unit consists of a direct-view storage

CRT. The surface of the display unit acts as the console's memory, and serves the double purpose of image storage and viewing screen. Once data is written on the surface of the display unit, it can remain visible for hours without noticeable degradation until erased. To clear the viewing surface for fresh data, the screen of the display unit erases within a fraction of a second.

INTRODUCTION

QED is a program for editing symbolic text. QED runs under CTSS and is designed to be interactive under that system. Its input and output are either console, 6-bit, 12-bit, or ascii files, or a combination of these. It has extensive facilities for inserting, deleting and changing lines of text, a search feature, a macro feature and a large number of possible text buffers.

GENERAL DISCUSSION

QED, like most editors, performs operations on text in a workspace. In QED the workspace is called a 'buffer'. A buffer consists of from zero to (ideally) any number of lines of normal text. Each line must be terminated in an end-of-line (carriage return) character. Not counting the end-of-line character, a line consists of from zero to (ideally) any number of characters.

QED, unlike most editors, has another level of hierarchy. The text in QED's workspace is broken up into from one to (ideally) any number of buffers. Each buffer is identified by a name of from one to five characters. There is one current buffer and all of the other buffers are auxiliary buffers. The auxiliary buffers allow temporary workspace to store text. Any of the auxiliary buffers can become the current buffer; at which time the old current buffer becomes an auxiliary buffer.

QED accepts commands and text from a stream of characters. This stream normally comes from the console. Special characters in the stream can divert the stream to a text buffer. In this way, predefined commands can be placed in a buffer and then executed by diverting the command stream to this buffer. This buffer in turn may divert the stream to another buffer or (recursively) to the same buffer. At any time, the stream can be diverted to the console for one line of text.

QED has a very uniform command format. Each command acts on text in the current buffer and possibly on an entire auxiliary buffer. The text in the current buffer is specified by a series of from zero to (ideally) any number of line addresses. Two adjacent line addresses are separated by either a comma or a semicolon. Only the last two addresses are 'remembered' although one address may affect the evaluation of subsequent addresses. The command is represented by a single character. This character is usually mnemonic of the action of the command. Depending upon the command, qualifying data may be needed after the command character.

Actual details on commands and addresses follow.

REGULAR EXPRESSIONS

Regular expressions can best be described by example. In the following examples, the characters '/', '|', '*', '(', and ')' are operators in the

Figure 2. Example of text output on ARDS (Actual size).

In normal operation the keyboard provides alphanumeric input to both the computer and the display unit. An additional graphic input device allows the user to draw directly on his display and transmit this graphic information into the computer.

Display

The display is a Tektronic Type 611 Storage Display Unit with a 8½" x 6½" viewing area. The long axis is normally oriented vertically. The spot size of the

TYPE 1

ARDS (MEMO) 01/19 1302.2

ARDS is a totally new type of computer terminal. It contains a symbol generator and a vector generator and uses a direct view storage tube as its display screen.

ARDS symbol generator contains the 94 printable symbols of the ASCII set. This set includes:

```
abcdefghijklmnopqrstuvwxyz  
ABCDEFGHIJKLMNOPQRSTUVWXYZ  
1234567890-_[!@; <> , . /  
! " # $ % & ' ( ) * + , - . / : ;  
? [ \ ] ^ _ ` { | } ~
```

Its vector generator allows ARDS to make extremely detailed drawings, as illustrated below.



Figure 3. Example of text and graphs on ARDS (Actual size).

display unit is nominally 8 mils. When two spots are plotted together on 12 mil centers, they will merge together to form one elongated dot. Spots plotted on 20 mil centers will usually appear as discrete dots. With the excellent resolution of the display unit, it

is possible to plot over 4,000 legible symbols when displaying text. Figures 2 and 3 illustrate the quality of the ARDS display.

For graphics the display screen is defined to contain 1081 x 1415 addressable points (these are not neces-

sarily resolvable points). With a vertical orientation of the long axis of the screen, the vertical edges have x addresses of +540 and -540, and the horizontal edges have y addresses of +707 and -707. The point 0, 0 is in the center of the screen. Both the number of addressable points and the location of 0, 0 can be adjusted. Because of the method used to keep track of beam position, pictures can run more than 1400 points off the screen in any direction before causing any distortion in the visible (on-screen) portion.

The display generator can draw lines at the rate of 1/2 inch per millisecond. Characters are drawn in 1.2 milliseconds. However, the transmission rate of the telephone line limits the effective writing rate. Typically, a full page of 4,000 characters is printed in 33 seconds using a 1200 bit-per-second line. The display unit erases in 500 milliseconds.

ARDS is unique in that any image displayed, no matter how complex, will be absolutely free of drift, wobble or flicker. The amount of data displayed in no way affects the visual quality of the display. When multiple display units are coupled to a single controller there is no decrease either in the quantity or the quality of the data displayed on each individual CRT. This performance is achieved through use of the direct-view storage CRT.

Controller

The controller contains the logic for decoding messages and creating symbols, points and lines. The format for the commands is described later.

The symbol generator set contains the 94 printable symbols of the American Standard Code for Information Interchange (ASCII). The standard symbol size is 12 characters per inch; however, size can be adjusted.

In Symbol mode ARDS acts as any teletypewriter, plotting the character received and moving the beam to the right one symbol position. In addition to the symbols, ARDS interprets the New Line (LF), Back Space (BS), and Form Feed (FF) characters. Form Feed erases the screen and positions the beam at the left margin on the top line of the page.

It should be noted that the Tab function is not implemented in the ARDS hardware. The Tab key will transmit the Tab code (011) but the display will ignore it. Because of ARDS random point plotting and vector generation capability, Tab, half-line-feed (subscript and superscript) and similar carriage controls can easily be implemented in software.

The vector generator operates on sign-magnitude numbers and draws vectors (Δx , Δy) relative to the last beam position. Magnitude values for Δx and Δy are 10 bits each and thus lines can have x and y components up to 1023 increments, which is almost full screen width. An increment is approximately 0.006 inches. The vector generator is able to draw any line in 8.33 milliseconds, the time required to accept one character at 1200 bits per second. The vector is in-

tensified if the Invisible control bit is off.

Set Points are specified as absolute coordinate values in sign-magnitude numbers. Magnitudes for x and y are 10 bits each. The Set Point is intensified if the Invisible control bit is off.

Format

The data format of ARDS is compatible with ASCII (see Fig. 4). The symbol set contains the 94 printable ASCII symbols. To accommodate graphic input and output, ARDS operates under mode control. ARDS is set into Symbol mode by any of the ASCII control characters (bit 7 = bit 6 = ZERO) with exception of three that are reserved for Graphic mode. In Symbol mode, ARDS interprets each non-control code as a symbol to be plotted.

Since ASCII does not have any provision for sending "graphic" information, a scheme for extending the code for ARDS has been adopted. This extension, which does not violate the basic precepts of ASCII, provides for a large number of "graphic commands", each of which can interpret "binary" arguments. Most of these commands are not assigned and are available for future extensions. Presently, ARDS responds to three graphic commands as indicated below:

1. *Set Point* will locate the beam to any absolute location on the screen, and intensify if requested,
2. *Long Vector* will draw a relative vector any length up to 1023 increments in any direction, blanked or visible,
3. *Short Vector* will draw a relative vector in any direction any length up to 31 increments, always visible.

ASCII control codes GS, RS or US (octal 035, 036, 037) will cause ARDS to enter "Graphic mode" and in particular the Set Point, Long Vector or Short Vector submodes respectively. Once in Graphic mode ARDS looks for "binary" characters to be arguments of the submode. Binary characters are defined as those with bit 7 = ONE, thus they contain just 6 bits of information. This format was chosen so that binary data never looks like communications control characters which may cause undesired actions along the communications lines (such as EOT turning off the line).

ARDS will stay in a graphic submode until it receives a character that takes it to another submode or back to Symbol mode.

Set Point (GS) submode interprets the next four binary characters as x and y data (sign plus 10 bits magnitude each) plus a bit to control whether to intensify the point or not. Succeeding groups of four binary characters are interpreted as data for more Set Points.

Long Vector (RS) submode interprets the next four binary characters as Δx and Δy data (sign plus 10 bits magnitude each) plus a bit to control whether to intensify the line or not. Succeeding groups of four binary characters are interpreted as data for more Long Vectors.

Bit Positions				b7				0	0	0	0	1	1	1	1
				b6				0	0	1	1	0	0	1	1
b5				0	0	1	1	0	0	1	1	0	1	1	
b4	b3	b2	b1												
0	0	0	0	NUL	DLE	SP	0	@	P	`	p				
0	0	0	1	SOH	DC1	!	1	A	Q	a	q				
0	0	1	0	STX	DC2	"	2	B	R	b	r				
0	0	1	1	ETX	DC3	#	3	C	S	c	s				
0	1	0	0	EOT	DC4	\$	4	D	T	d	t				
0	1	0	1	ENQ	NAK	%	5	E	U	e	u				
0	1	1	0	ACK	SYN	&	6	F	V	f	v				
0	1	1	1	BEL	ETB	/	7	G	W	g	w				
1	0	0	0	BS	CAN	(8	H	X	h	x				
1	0	0	1	HT	EM)	9	I	Y	i	y				
1	0	1	0	LF	SUB	*	:	J	Z	j	z				
1	0	1	1	VT	ESC	+	;	K	[k	{				
1	1	0	0	FF	FS	'	<	L	\	l					
1	1	0	1	CR	GS	-	=	M]	m	}				
1	1	1	0	SO	RS	.	>	N	^	n	~				
1	1	1	1	SI	US	/	?	O	_	o	DEL				

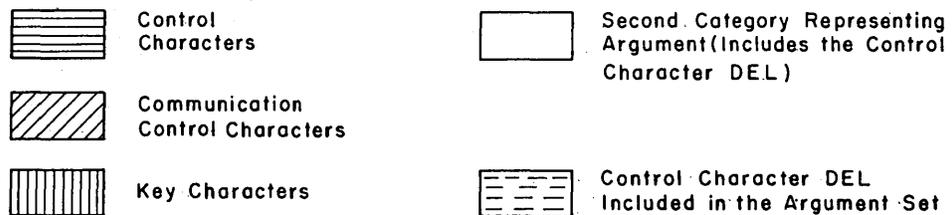


Figure 4. USASCII Character Assignments.

Short Vector (US) submode interprets the next two binary characters as Δx and Δy data (sign plus 5 bits magnitude each). Short Vectors are always intensified. Succeeding groups of two binary characters are interpreted as data for more Short Vectors.

In addition to the three submodes described, 32 unassigned submodes are provided. These are entered from Set Point, Long Vector or Short Vector submodes by receiving one of the group of 32 characters which have bit 7 = ZERO, bit 6 = ONE, called "Key" characters. These submodes are reserved for adding optional features to ARDS (e.g., multiple displays, dotted lines, circles, etc.) or for control of other equipment (tape recorder, hard copier, etc.).

ARDS is returned to Symbol mode by any ASCII control character other than GS, RS or US. In addition to returning to Symbol mode, ARDS will act properly on the control character (i.e., FF will pull ARDS out of Graphic mode, erase the screen and reposition the beam).

Graphic Input

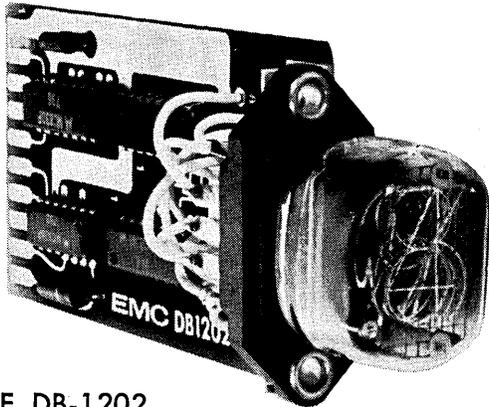
This feature allows the user to converse conveniently with the computer in a graphic dialogue. Pictures can be drawn on the screen by the user and the data transmitted to the computer as it is being drawn. Furthermore, screen locations can be identified to the

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THE DB-1203 (with memory)

A family of plug-in cards, using the same 20-pin edge connector and the same card size and construction, is available to provide a display memory function in addition to the counting function of the DB-1202. Transient BCD information may be transferred to this card and displayed independently of the source until a new set of information is accumulated.

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computer quickly and easily by means of a graphic input device. Two such devices are available. One is a hand-held hemisphere (similar to Stanford Research Institute's "Mouse") that indicates relative x and y positions as it is moved over a surface. The second device, called a "Tablet", consists of a resistive sheet with voltages applied to its boundaries and a pick-up stylus. These devices were designed for simplicity and low cost.

The graphic input devices control a non-storing cursor (a 0.05 inch diameter circle) on the display screen. Moving the graphic input device causes the cursor to move on the screen in an identical manner. Two buttons are provided to cause encoded graphic input messages to be sent to the computer. If the Set Point button is depressed the message sent is the Set Point character (GS) followed by four binary characters to represent the absolute coordinate position of the cursor on the screen, and a final FS character to end the message and return ARDS to Symbol mode. If the Line button is pushed, the Vector character (RS) is sent, followed by four binary characters to represent the relative vector from the last beam position. An FS character ends this message also. Since the messages sent to the computer are also interpreted by ARDS, points and lines entered in this way will plot on the scope. The end point for a line becomes the starting beam position for any new line.

Further Improvements

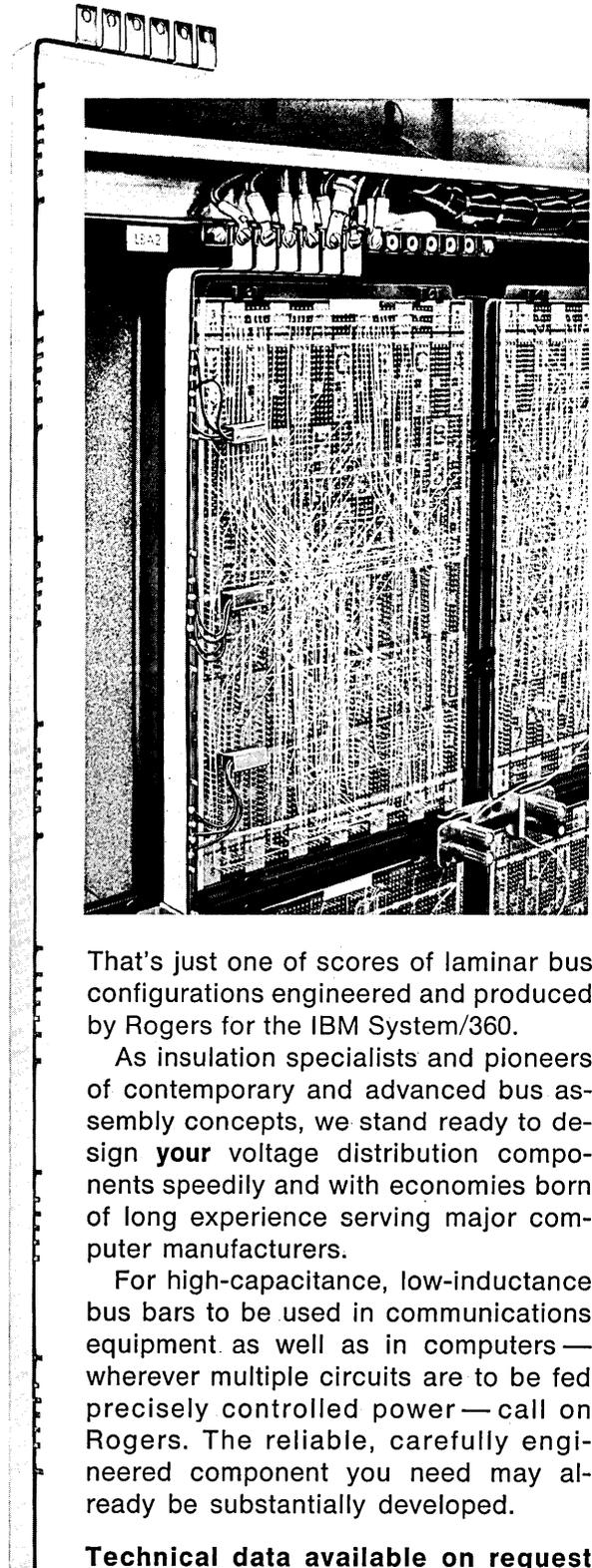
The most fertile area for future developments to ARDS lies in the new image storage devices which are being developed across the country. The direct-view storage tube, while yielding excellent picture quality, still leaves several things to be desired. The display size is too small for many problems. With the present display size and resolution ARDS is not satisfactory for group viewing or for presenting large engineering drawings. The display brightness is another drawback. Special attention must be paid to placement and/or hooding of the direct-view storage tube in a brightly lit room.

Selective erasure would also be a valuable asset to an image storage device for ARDS. With the present storage tube, pictures can be added onto, but the entire screen must be erased and redrawn if any part of the picture must be deleted. This is not a hardship in most applications, but selective erasure would allow more flexibility in ways the terminal could be used.

Conclusions

ARDS is a new type of graphic display which promises to fill the gap that has existed between the inexpensive but slow and clumsy teletypewriter and the expensive, powerful graphics consoles with internal general purpose processors. Although designed for telephone-line operation in a time-sharing environment, ARDS also shows promise of being very useful when connected directly to a computer over a wide-band link. The design of ARDS trades the "dynamics" of conventional refreshed CRT displays for low cost, large quantity of data presented and high quality of display.

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This article provides a broad coverage of the Spectra 70 and an advanced computing system in terms of their circuit noise immunity and system noise sources. The fundamental parameters of each system are detailed and a general evaluation of noise sources in high speed computer systems is discussed. Further, a graphical technique for calculating circuit noise immunity is detailed. With this knowledge, the logic circuit and systems designers can make favorable and economical tradeoffs without impairing system reliability or increasing circuit costs.

COMPUTER CIRCUIT NOISE IMMUNITY AND SYSTEM NOISE

The University of Illinois under an award from the Department of Defense will design, develop, and operate a large-scale highly parallel computing system — ILLIAC IV. RCA was involved in Phase I of this project which was a study directed toward developing a system design optimized on the basis of hardware and software considerations. The results of these studies are the basis for this comparison of a "next generation" computer with the existing Spectra computer.

In terms of circuit requirements, the Spectra and ILLIAC IV computers are quite similar. Each uses current-mode-logic circuits in a monolithic silicon integrated form. The logic pair delays are 24 ns for the Spectra 70-45/55 computers and 5 ns for the advanced computer. Of interest here is the faster risetime circuits associated with the decreased logic delay (3.5 ns and 0.4 ns respectively). The packaging requirements of these systems are substantially different and can be characterized adequately by their transmission line impedance. For the Spectra, 100-ohm lines are used while the advanced computer will use 50-ohm lines.

The design of computing systems has always involved a number of compromises between many conflicting requirements; depending on the technology employed, and problems to be solved, a priority level was established for each requirement. Today, with the advent of high speed circuits and high density packaging, the most stringent requirement, aside from the basic gate delay, is noise immunity. In general, as faster system risetimes are experienced, the greater is the requirement for high circuit noise immunity.

To manufacture high speed circuits of the next generation will require more complex fabricating processes and higher resolution artwork. The result is that the circuit specification yield compared to its slower speed predecessor (Spectra) drops considerably if the same system noise immunity is required. Thus two alternatives — accepting reasonably priced, reduced noise immunity circuits or higher priced maximum noise immunity circuits — are available to the system designer. When considering that fast risetime

circuits may not only increase the magnitude of machine noises but also introduce new sources of noise, the above tradeoff is not easily made.

Noise Immunity

The circuit schematic for a Spectra-70 gate is shown in Fig. 1. Transistor Q_2 is at a fixed bias of -1.2 volts provided by the bias driver. As the input (V_{IN}), which for this example is assumed to be -0.8 volt initially, approaches -1.2 volts Q_1 will start turning off. When Q_1 turns off, the NOR output will change from -1.6 volts to -0.8 volt and the OR output from -0.8 volt to -1.6 volts. Therefore the circuit provides both inverted and noninverted outputs for a given input.

The -0.8 volt level, which is the most positive level, will be defined as the logical ONE level, and the -1.6 volts level will be defined as the logical ZERO level. The operating boundaries of the gate are shown in Fig. 2. In the following discussion, note that "greater than" and "maximum" mean more positive and "less than" and "minimum" means more negative.

For any input voltage excitation greater than or equal to the MIN-ONE level, the NOR output voltage will indicate a level less than or equal to the MAX-ZERO level and the OR output will indicate a level greater than or equal to the MIN-ONE level.

For any input voltage excitation less than or equal to the MAX-ZERO level, the NOR output voltage will indicate a level greater than or equal to the MIN-ONE level and the OR output will indicate a level less than or equal to the MAX-ZERO level. $V_{MIN ONE}$ is the minimum allowed input ONE level in a logic system; $V_{MAX ZERO}$ is the maximum allowed input ZERO level in a logic system. Therefore, restricted areas of operation have been defined for the gate as shown by the cross-hatched areas. The operation of the gate should exist within these boundaries under any steady-state condition of operation of the gate.

Various interpretations of circuit noise immunity and the effects of machine noises in system operation have been made. In this work, circuit noise immunity

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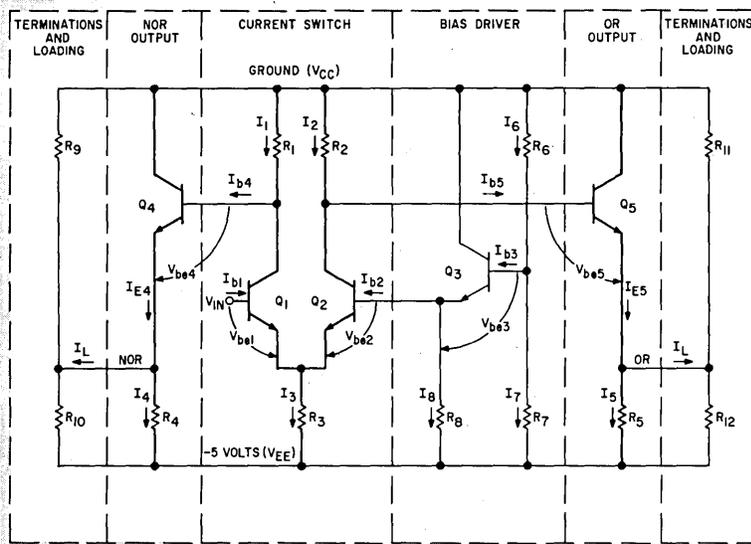


Figure 1. The basic Spectra 70 gate circuit.

is defined as the magnitude of change of input signal from a steady-state input level that will produce a detectable output level change. Also, strictly speaking, both a DC and AC circuit noise immunity for the Spectra circuit were experimentally determined to be greater than DC noise immunity. The relationship of AC-to-DC noise immunity is shown in Fig. 3.

The noise immunity of this circuit is analyzed by developing worst-case equations (Table I) of the following:¹

- 1) Bias driver output voltage;
- 2) Minimum value of the high-level voltage (0.8 volt);
- 3) Maximum value of the low level voltage (1.6 volt); and
- 4) Minimum value of the input swing voltage required to switch the transistors.

By the use of a DC computer-map program, the equations listed in Table I with their appropriate device characteristics, tolerance, and thermal coefficients, can be used to describe the logic levels and bias driver

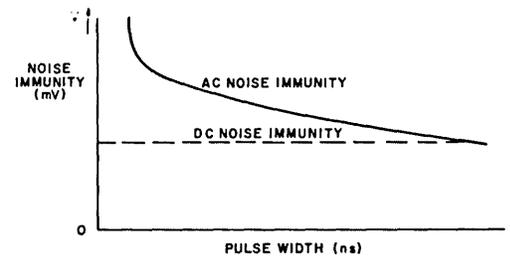


Figure 3. AC and DC noise immunity relationship.

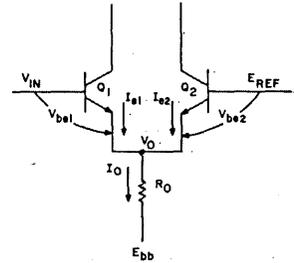


Figure 4. Model for input voltage swing.

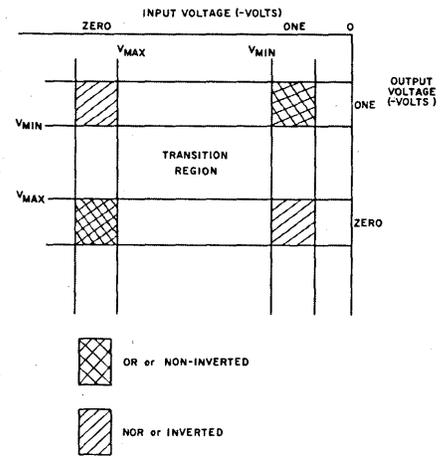
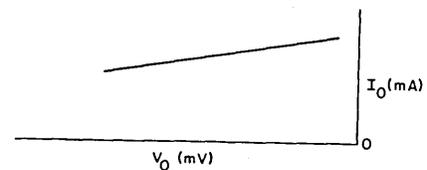


Figure 2. Logic levels for Spectra gate.

voltage over the temperature range of interest.²

The next analytical step is computation of the minimum value of voltage input swing required to switch the current-switch transistors. For this analysis, consider Fig. 4 which shows the basic current switch under analysis.¹¹ By using the relationship $I_o = (E_{bb} - V_o) / R_o$, I_o can be plotted as a function of V_o . This yields the following curve:



Next we make the valid assumption that Q1 and Q2 transistors are identical so that V_{be1} is equal to V_{be2} for given values of current. This follows from the fact that transistors Q1 and Q2 are on the same integrated circuit chip.

TABLE I. LOGIC LEVEL AND BIAS DRIVER EQUATIONS

Voltage Input High

Voltage Input Low

OR

$$E_{OR} = \frac{(R_2/R_5) V_{EE} - \beta_5 V_{bc5} - I_L R_2}{\beta_5 + (R_2/R_5)}$$

OR

$$E_{OR} = \frac{(R_2/R_5) V_{EE} - (R_2/R_3) \alpha_2 \beta_5 (V_{REF} - V_{be2} - V_{EE}) - \beta_5 V_{bc5} - R_2 I_L}{\beta_5 + (R_2/R_5)}$$

NOR

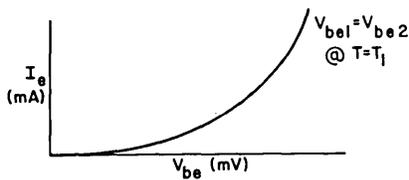
$$E_{NOR} = \frac{(R_1/R_4) V_{EE} - (R_1/R_3) \alpha_1 \beta_4 (V_{IN} - V_{bc1} - V_{EE}) - \beta_4 V_{bc4} - R_1 I_L}{\beta_4 + (R_1/R_4)}$$

NOR

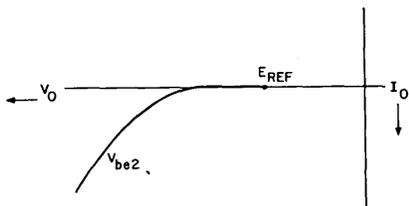
$$E_{NOR} = \frac{(R_1/R_4) V_{EE} - \beta_4 V_{bc4} - R_1 I_L}{\beta_4 + (R_1/R_4)}$$

BIAS DRIVER

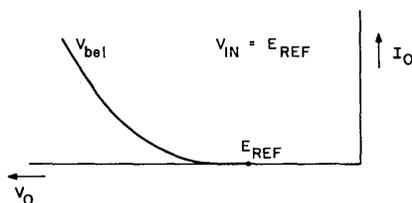
$$V_{REF} = \frac{V_{EE} - \frac{R_7 2I_{b2}}{\beta_3} + \frac{R_7}{R_8} \frac{V_{EE}}{\beta_3} - V_{be3} \left(\frac{R_6 + R_7}{R_6} \right)}{\frac{R_6 + R_7}{R_6} + \frac{R_7}{R_8} \frac{1}{\beta_3}}$$



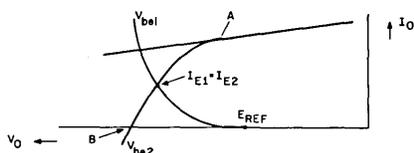
The V_{be} data used in the analysis are specifically for a two-stripe geometry integrated circuit transistor at the outer limits of the V_{be} spread. A two-stripe transistor is characterized by the number of contacts in the base and emitter diffusion areas ($1b$, $1e$). The curve can then be modified for the particular temperature of interest by using a V_{be} temperature coefficient of $2mV/^\circ C$. From the nodal point, designated V_o , the current I_{E2} and the quantity $(V_{be2} + E_{REF})$ are seen to be negative. This yields the following plot.



Since the currents I_{E1} and I_{E2} are equal when $V_{IN} = E_{REF}$, the following relationship can be derived:



The composite characteristic would then be



Transistor Q1 is turned on fully by shifting V_{be1} to the right until it intersects point A so that $I_{E1} = I_o$.

Shifting V_{be1} to the left until it intersects point B will make $I_{E1} = 0$ so that Q2 is fully on and $I_{E2} = I_o$.

The results of the complete analysis are shown in Figure 5. These data are from an unterminated line condition, and this example represents but one of many test cases run. For convenience the noise immunity of a typical case at the high and low levels at $70^\circ C$ is given.

BASIC DIFFERENCES BETWEEN SPECTRA AND ILLIAC TYPES

Parameters

To make some statements in regard to noise immunity, it is first necessary to discuss the parameter changes in the two systems.

System Noises

There are many sources of noise in digital computer systems. Only those noises related to the circuit, interconnections, and power distribution are considered; noises related to radiation, static charges, or mechanical switching are not. One of the first considerations is circuit risetime, which forms the base for many of the calculations. Fig. 7 shows the marked decrease in computer risetimes for various systems. As an indication of expected risetimes, consider the idealized circuit of Fig. 6.³

The switch represents a transistor, the load capacitance (C), and the TERMINATING resistance (R_o). Such a circuit is closely approximated by any high speed device driven by a constant current. Then $I = C \Delta V / \Delta t$, where Δt is risetime, ΔV is voltage swing, and C is $n(C_i + C_s)$; and where n is circuit fanout, C_i is circuit input capacitance; and C_s is capacitance of connection to transmission line. I is the available current which is equal to the supply voltage divided by the total power of the supply. Therefore

$$t_r = [n (C_i + C_s) \Delta V] V_s / P_s$$

For the case, $n (C_i + C_s) = 20$ pF, $\Delta V = 0.8$ V, $V_s = 5$ V, and $P_s = 200$ mW: $t_r = (20 \times 10^{-12}) (0.8) (5) / 200 \times 10^{-3} = 0.4$ ns

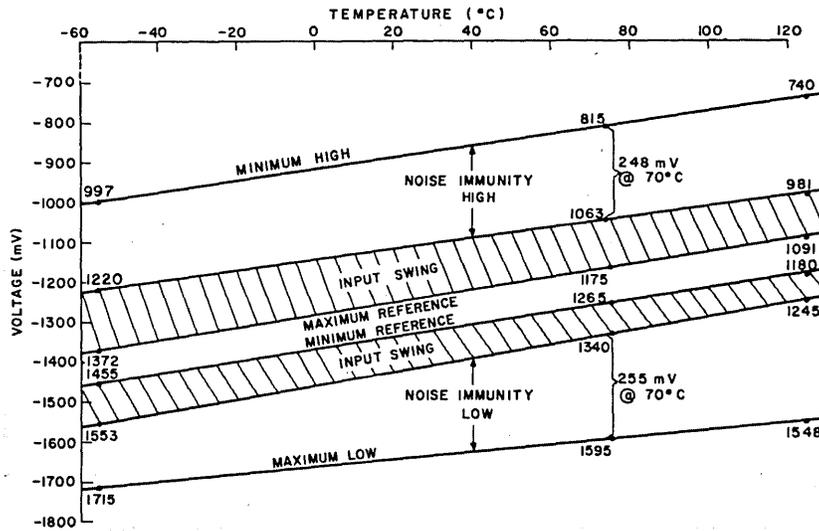


Figure 5. Noise immunity as a function of operating temperature.

For the next generation of machines, risetimes of 0.4 ns may be expected.

Generally, crosstalk and reflection phenomena and the power distribution scheme are the sources of machine noise. Specifically, in the circuit this noise is attributable to phantom-OR connections, feedthrough noise, OR-NOR level difference, actual capacitive loading and OR/NOR unbalanced loading. Fanout noise sources are serial net loading along with radial net undershoot and overshoot. Platter-generated noise includes crosstalk, impedance mismatch, capacitance of via holes, and the dc platter drop. Plug-in crosstalk and power distribution noise, and wiring crosstalk and mismatch are additional sources. Of course connection discontinuity is always a potential noise source.

The details of these calculations for the Spectra and ILLIAC type machines are contained in Reference 4. For our purposes, cases will be selected to show fundamental differences and how they are handled.

First, consider a major source of noise: the serial net loading noise. The percent reflection will reduce for the advanced computer case even though its risetime is 4 to 5 times as fast; however, this is not necessarily true of all cases. The gate input capacity for both circuits is assumed to be 5 pF. If the product of the line impedance and capacitance per load is kept constant, the value of reflection is kept constant.

$$\begin{aligned} Z_1 C_1 &= \Gamma_1 \\ Z_2 C_2 &= \Gamma_1 \end{aligned}$$

Solving for C_2 ,

$$C_2 = \frac{Z_1 C_1}{Z_2}$$

$$C_2 = \frac{50 \Omega}{100 \Omega} \times 5 \text{ pF} = 2.5 \text{ pF}$$

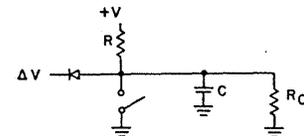
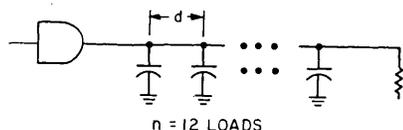


Figure 6. Idealized circuit for risetime evaluation.

Therefore, in going from a 100-ohm to 50-ohm impedance system, the effective capacity is reduced by one-half. Design curves from Reference 7 give

Spectra	Advanced Computer
$r_i = 4 \text{ ns}$	$r_i = 1 \text{ ns}$
$Z_o = 100 \text{ ohms}$	$Z_o = 50 \text{ ohms}$
$C = 5 \text{ pF}$	$C = 2.5 \text{ pF}$
$n = 12 \text{ LOADS}$	$n = 12 \text{ LOADS}$
3-inch electrical spacing	3-inch electrical spacing
Reflection = 25.5%	Reflection = 13%

Thus we have the interesting result that the percent reflection decreases for the faster risetime system. Again caution is needed in the analysis of particular cases.

Second, consider the platter crosstalk noises. Crosstalk effects can be conveniently compared by the two crosstalk constants, K_B (back crosstalk) and K_F (forward crosstalk). The equations are:

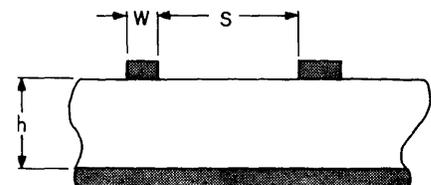
$$V_B = K_B V_o,$$

where V_B is the magnitude of backcrosstalk and V_o is the input swing;

$$V_F = K_F l \frac{dV}{dt},$$

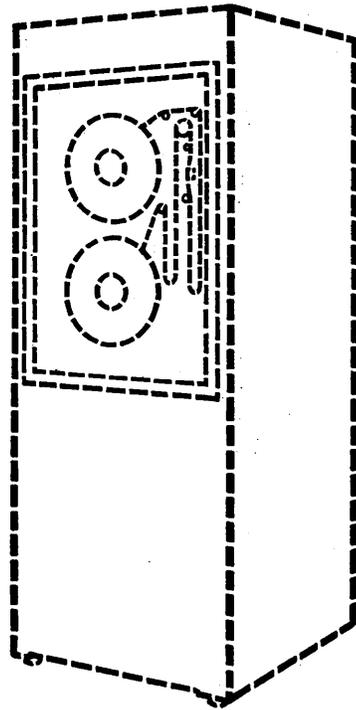
where l is the line length and dv/dt is the slope of the input signal.

The platter cross-section appears as in the sketch below.



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In Table I, the Spectra line spacing was 25 mils while the advanced computer was 15 mils. The K_B would increase as the line spacing gets closer.⁷ Note however that in going from a 100-ohm to 50-ohm system, the H decreases significantly. The results is that K_B decreases.

Both the platter and plug-ins in the ILLIAC computer will use coated transmission lines. It has been

shown that the forward crosstalk constant K_B of a coated line can be reduced to zero.⁸ Therefore the forward crosstalk is less in the advanced machine than in the Spectra. Again this is an interesting result since V_F is proportional to the risetime.

Thus, two opposite results, in terms of crosstalk and reflection, have been produced. Both are attributable to the packaging format chosen. Normally, these phenomena would be expected to increase when going from a 4 ns to a 1 ns system. One may begin to conclude that a faster risetime system is easier to build so that a reduced noise immunity circuit may be used. However, this is not the case. Actually, while some of the noise sources are decreasing in value others are increasing.

Consider the signal connector for both the Spectra and the advanced computer. The Spectra connector is not a controlled impedance connector. The signal connector in the advanced computer must be a controlled impedance connector since it may have to handle 0.4 ns risetimes. Therein lies the problem: For risetimes of 0.4 ns, impedance discontinuities could occur for line lengths of 1 inch. Therefore, the separable connector should have its overall length (signal plus ground) reduced. In addition, the effective connector impedance should be as close to 50 ohms as possible. For example, if the effective impedance were 80 ohms instead of 50 ohms, the percent reflection would be

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} = \frac{80 - 50}{80 + 50} = 23\%$$

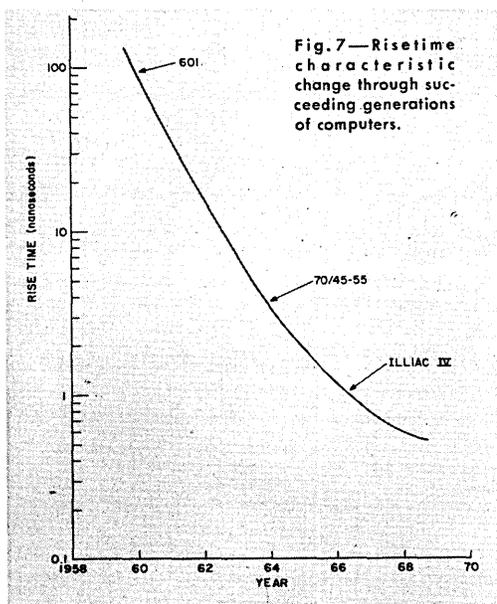


Fig. 7—Risetime characteristic change through succeeding generations of computers.

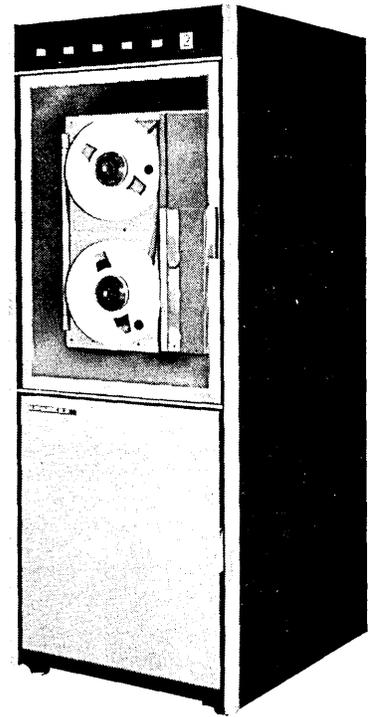
Figure 7. Risetime characteristic change through succeeding generations of computers.

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Crosstalk between signal pins of a connector is now a major problem for operation at the risetimes of interest.¹⁰ In addition, the grid spacing of the platter has been reduced from 125 mils to 100 mils for the advanced computer, thus placing the pins closer together. Again, shorter signal conductors must be used, ground paths must be shortened, and ground planes must be added to isolate the various signals on pins in the same proximity.

Another major problem area is the actual power distribution system. The next generation of computer will be a high gate-density system. Therefore, a very low impedance system will be needed to handle the increased currents and faster risetime circuits.

Conclusions

Spectra is a computer that has been built and for which the circuit noise immunity and appropriate wiring rules have proven to be adequate. ILLIAC IV represents a class of computing machine that may be the very next generation computer in terms of the circuit densities and circuit risetimes. This type of system requires close scrutiny in terms of evaluating system noises and specifying circuit noise immunity.

In the Spectra, a one-third allocation of noise immunity was made for reflections (80 mV), crosstalk (80 mV), and power distribution (80 mV).⁶ It is very unlikely that a faster risetime computer could utilize a circuit with less than 240 or 250 mV of noise immunity. Yet this prospect exists because the artwork and process problems associated with smaller geometry

devices are expected to significantly increase the cost of the new high speed circuits.

One step toward the realization and use of a reduced noise immunity circuit is first in understanding the strong interplay between circuits and packaging. With a knowledge of both circuits and packaging parameters, a re-allocation of noise immunity may be made to handle the noise problems of new design areas such as a separable controlled impedance connector.

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In time-sharing systems where programs and data move frequently between storage media, performance measured in terms of response time, availability, capacity and generality depends on the ability of the system to move information quickly and promptly on demand. Comparison by analysis and test of a TTS/360 with drum storage and with Large Capacity Core Storage reveals that the LCS system provides nearly an order-of-magnitude better performance than is possible with a drum system.

BULK CORE IN A 360/67

In the fall of 1965, Carnegie Institute of Technology decided to install Large Capacity Core Storage (LCS) as the auxiliary storage device on its IBM 360/67 Time-Sharing computer system. The bulk core will be used as a swapping device, replacing the drums of conventional configurations, and as an extension of main core memory. The decision was motivated by an analysis that yielded the following results:

- The effective rate at which the system can deliver pages to user tasks is increased to its theoretical limit with LCS, representing a significant improvement over drum performance.
- The potential response time to users is decreased because LCS has no rotational delay.
- Less main core is needed for effective system operation.

In addition, LCS provides the memory necessary to support specialized computing requirements such as artificial intelligence research or large table-driven compilers.

In this article, we will present the assumptions and analysis that shaped the configuration, look at a model of a drum-oriented system, compare it to LCS, present the Carnegie system and implementation plan, and summarize the results from a test implementation.

BACKGROUND AND ASSUMPTIONS

When a task executes in machines of the class of the IBM 360/67 or GE 645, only the local portion or neighborhood of its program and data that is actually relevant at a given moment need be in core. What the program "sees" is not physical core, but a space of addresses called a *virtual memory*. A hardware mechanism translates each address into a core location, if that address is part of the neighborhood in core, or to a supervisor interrupt if it is not. In the latter case, the monitor causes the block of virtual memory, called a *page*, which contains that address to be read from a

swapping device into core. Thus, a machine with a small physical memory can allow several large programs to share it simultaneously. The user is absolved from preparing overlays and deliberately fragmenting his program, while the system bears the burden of swapping pages in a timely and efficient manner. It is the efficiency of this swapping process that concerns us here.

There are some special restrictions on the user program in this system. For example, it is unwise to refer randomly to locations in virtual memory; that would generate a very high demand rate for pages. Rather, the task should work in reasonably small neighborhoods for relatively long periods of time. The system is, however, a step toward the goal of providing a comprehensive time-sharing system in which users can operate conversationally or non-conversationally, without restrictions on language, facilities, or program structure. While we are realistic enough to see that this goal will not be closely approximated for several years, we do allow it to affect our thinking.

What we have just described is a system which simulates a large core memory with on-line storage, usually a disk or drum. The time-sharing capabilities come with the structure of that memory, not its size. It is worthwhile then to look at a large core simulation system. One successful machine, at the University of Grenoble, provides an 800,000 LISP word memory on a 7044 with disk.¹ In this system, a swapped program ran approximately one-third as fast as the same program residing in core. However, from the published data, it can be seen that the mean time between calls for new pages in print (one might call it the *mean free path* of the program) is a function of the number of pages already in core, and is usually greater than three seconds. If it is smaller, then the swapping overhead time becomes large relative to the user task time, and the system loses efficiency.

Clearly, the mean free path depends on the struc-

TIME SHARING SYSTEM

HUGH C. LAUER
Computation Center
Carnegie-Mellon University

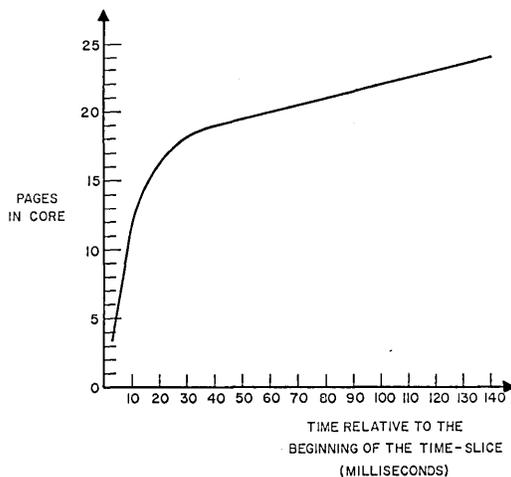


Figure 1. Reproduction of data presented by Fine, et. al., SDC.¹

ture of the programs in the system. Investigators at SDC have examined the behavior of several programs that might be typical in a time-sharing environment.² Existing jobs from the Q-32 machine were run under a simulated paging system, and the mean free paths were measured as a function of the number of pages in core. It was discovered that with small neighborhoods of only a few pages, the mean free path was extremely small and the demand rate for pages per unit of task CP time was high. In Figure 1, the number of pages in core is plotted against the time within a time slice, assuming that the task starts out with no pages and each is brought in on demand. It can be seen that once a *working set* of pages is available, the demand rate goes down from its initial high level. However, the authors point out that with the program structure as it is, the paging mechanism is bound to congest very quickly, and "there would be little chance of processing-fetching overlap." Paging demands would overwhelm the system.

We must be careful about translating such experiences to other computers, for the environment has a heavy impact on the character and structure of programs. For example, in the Q-32 analysis, they were 30-46 pages long. In the 7040 and 7090 systems, programs are less than 32 pages long; yet results for these machines strongly influenced the design of the 360/67 and its software.

In the IBM Time-Sharing System/360 (TSS), there is a tendency to code in many small modules, to separate data from procedure, to write re-entrant routines, and to functionally fragment programs. None of this appeared in earlier machines, and all of it tends to increase paging demands. Early experiences at Lincoln Laboratory and at IBM with TSS indicate that estimates such as Figure 1 are conservative, and that the system is more page-bound than was anticipated. In particular, the knee of the curve lies at about 40 pages. The Carnegie LCS-oriented system is an attempt to create a machine that is not page-bound while minimizing restrictions on the structure of task programs.

In the analysis that follows, we must make some assumptions and avoid others, based on experience and "what's reasonable." In particular:

- We assume that the system is page-bound, with a demand rate of the order of hundreds of pages per second. Specifically, we assume that the amount of swapping channel time is greater than the amount of CP time it supports, and we direct our efforts to eliminating the consequent CP idleness at a reasonable cost.
- Our analysis will be oriented about the stochastic nature of the system. We assume that each task, and all random variables describing it, are independent of all other tasks in the system.
- We are unwilling to assume that any random variables have particular distribution functions, with only the following exceptions:

- 1) The wait-time between the moment a task requests a page to be read and the time at which the swapping device becomes available to service it is uniformly distributed over the length of the swapping channel program.
- 2) The variable designating the location of a page or group of pages on the swapping device will have either the uniform or singular distribution.

Both are justified because the state of the art does not now provide mechanisms for decreasing the expected wait-time to find pages in this environment. Any such techniques depend inherently upon program structures, about which we know very little.

- We ignore file activity and concentrate only on the swapping process. A more comprehensive analysis, which will extend these results to account for other devices, will be made in the future.

- We will ignore correlations between the state of the system at the end of a time slice of a task and the state at the beginning of the next time slice for that same task. We can treat shared pages, which are swapped only infrequently, if at all, as part of the resident system, and not part of the swapping load. The demand for space for non-shared pages will be sufficiently high that only a negligible number of them will survive in core during the interval between time slices.

- After we have experience with the system, we will take advantage of correlations between system states to improve scheduling algorithms; now we can only do this in a limited way.

- Inefficiencies in monitor coding can be ignored. We are interested in the hardware capabilities, not software performance, so we will assume the ability to write clean code. The supervisor overhead for an interrupt can be assigned to the task that caused it. Consequently, the *task time* is the total amount of CP time dedicated to that task for both user computing and overhead, i.e., the marginal increment of computing load added to the system by that task. The fact that overhead may amount to 1% or 90% of the task time is irrelevant to us here.

With these assumptions, we can proceed with the analysis.

DRUM-ORIENTED SYSTEM

The drum we will consider as a swapping device has one read-write head for each track, but only one head can be connected to the channel at any moment. There are p pages recorded on the circumference of each track, and there is sufficient space between pages to permit head switching. Thus, it can read the first page on track a , followed by the second page on track b , and so on through the p^{th} page on track x , all in one revolution. We can regard the drum then as a sequence of p slots passing by a single head. When the head is over a particular slot, one and only one page may be read or written in that slot. The drum operates asynchronously from the CP under the control of its own *channel program*. Once an operation has been started, it may not be interrupted or altered except in the case of malfunctions.

Figure 2 will help describe the system that we model. At time A , a channel program was initiated to run until time B . Tasks 1, 2, 3, 4, and 5 execute in turn

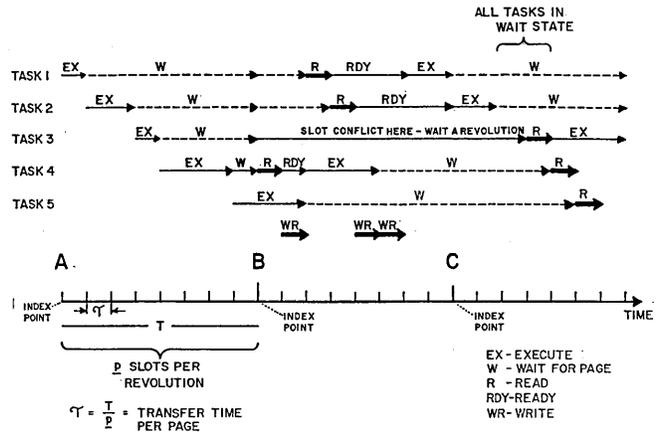


Figure 2. Example of system execution.

until each develops a page request. By time B , all requests have been analyzed and a new channel program has been prepared. The figure shows examples of what can happen:

- 1) The page for task 4 was located on the first slot, so that task 4 is ready to execute almost immediately.
- 2) Task 1 is serviced next, then task 2.
- 3) The page request for task 3 happened to fall in the same slot as that for task 2, so it must wait a full revolution before it can be serviced.
- 4) Task 5 has a long wait because of the location of its page on the drum.
- 5) Several slots that are not needed to service tasks at the moment are used to write out old pages from core in order to make room for new pages.
- 6) Shortly after time C , the CP enters the wait state because all of the tasks are waiting for pages, and there are no others ready.

Though we had four requests at point B , we could only service three of them because of a slot-conflict. Of course, had the system been able to anticipate either the slot conflict or the idle time, it would have taken corrective action; but our assumptions about the independence of tasks and the randomness of page locations preclude this.

In the following paragraphs, we will calculate the rate at which the drum can deliver pages and observe the relevance of this to the mean free path of tasks. Then we will discover a *lock-out* phenomenon, by which the drum causes pages to be withdrawn from usable core. We will also explore some ideas to swap groups of pages as a means to overcome some of the problems we encounter.

Deliverable Page Rate — Demand Paging

We consider the case in which all channel programs are the length of one drum cycle, of time T . The expected rate at which pages are read is a function of k , the number of tasks in the drum queue, and f , the probability that a page must be written out to make room. It is possible that $f < 1$, since some pages in core may have valid copies on the drum already (by virtue of being re-entrant, or otherwise not changed since being read). Then for each page requested, the swapping channel must handle an average of $1 + f$ pages. Thus, the maximum average request rate that a p -slot

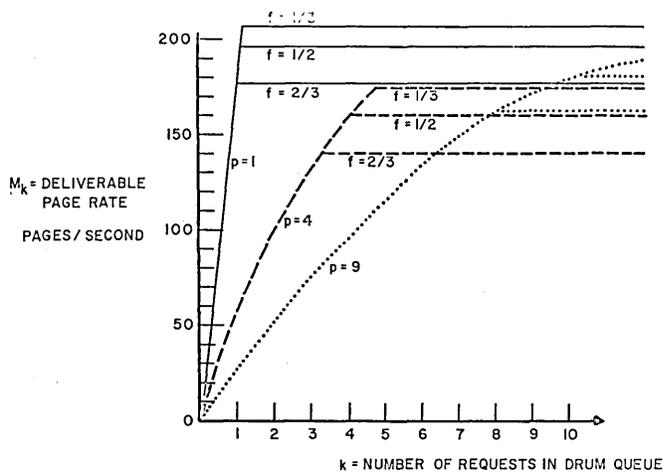


Figure 3. Deliverable paging rate.

drum can service is $p/(1+f)$ pages per revolution or $p/[(1+f)T]$ pages per second. The one-sided effect which occurs when f is greater than its mean is negligible if the system maintains a buffer of free pages into which the drum can read.

Because of slot conflicts, this rate can only be approached. A classical probability exercise known as the Urn-model Occupancy problem gives us the result.³ With p slots and k requests, the probability, P_i , that exactly i pages [$1 \leq i \leq \min(p, k)$] can be read in one revolution is given by

$$P_i = \frac{p!}{(p-i)! i!} \sum_{v=0}^i (-1)^v \binom{i!}{(i-v)! v!} \left(\frac{i-v}{p}\right)^k$$

The average or expected number of pages the drum can read, given k is

$$M_k = \sum_{i=1}^k i P_i.$$

If M_k is less than $p/(1+f)$, there will be sufficiently many unused slots in each revolution to do the necessary page writes. Slot conflicts pose no concern during writing because the supervisor chooses the output location after the read requests have been scheduled. Thus, for queue of length k , the drum can deliver

$$Q_k = \min\left(M_k, \frac{p}{1+f}\right).$$

pages per revolution. The total effective swapping rate is the mean of the Q_k weighted over the probability distribution of k . (This distribution can be determined empirically or by making assumptions about the program structure.)

In Figure 3, we plot M_k as a function of k and f for several examples. The case $p=9$ and $T=34$ msec is the TSS drum system, where 9 pages are recorded on two tracks (the length of a page is 4096 bytes = 1024 words). The case $p=4$, $T=17$ msec, is the same drum reformatted to waste some space in favor of reducing the length of the cycle. The final case is a hypothetical drum which can hold only one page per track, but rotates with $T=3.4$ msec, the maximum speed of the channel.

We see from the figure that the hypothetical drum requires only one task queued for service in order to maintain the maximum swapping rate, but the others require 3-4 tasks and 8-10 tasks in the queue for $p=$

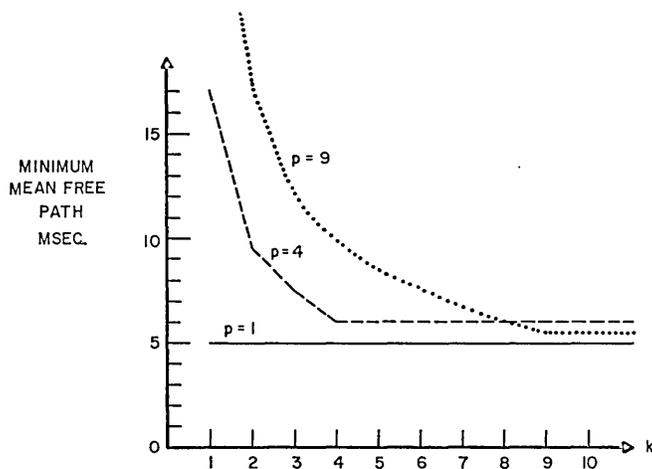


Figure 4. Minimum allowable mean free path.

4 and $p=9$, respectively. If k is smaller, then some slots are idle while tasks wait because of slot conflicts. But those slots must still pass the read-write head, and this wastes channel time. Our initial assumption was that channel time is at a premium and cannot be lost; so if we use one of these drums, we must operate with a large k . Main core must then be big enough to contain the many tasks that make up the drum queues plus some tasks that are ready to execute. We will see shortly just how much core this must be.

The effect of adding drums on separate channels can be seen from this model. Although they would not be synchronized, they could be coordinated and scheduled together. Then for n drums, the maximum page rate is $n.p/(1+f)$. One could also plot a graph of M_k versus k , and one would find a more rapidly rising curve than in the case of a single drum. This can be attributed to the fact that there are n times as many slots passing the heads in the interval of time T , and thus less chance of a slot conflict for a given k .

Requirements of Mean Free Paths

We would like to maintain complete processor-swapping overlap. To do so, the total amount of CP time necessary to do the work must be at least as great as the total amount of channel time necessary to support the CP. From this, we can determine the minimum mean free path of tasks. If k is the drum queue length, then in a revolution of time T , M_k tasks are delivered to the CP, on the average. Their total execute time must exceed T so that the mean free path must exceed T/M_k . In Figure 4, we plot this value as a function of k . For large k , there is little difference between the three cases; but for k equal to two or three, the hypothetical drum restriction is less by a factor of two to four. (We will see that LCS, when operated with a core-to-core channel is a realization of this hypothetical machine.)

From this calculation, we can discover how short our average time slice can be. An example will help. Suppose that tasks exhibit the behavior of Figure 1 with the knee of the curve at one millisecond and ten pages. Suppose that the drum can deliver 100 pages per second. Then the time slice must be at least 100 milliseconds, for the drum can "set up" no more than

ten tasks per second. Any attempt to run with a smaller time slice will automatically generate CP idling.

It should be pointed out that this discussion deals with averages, and not the statistical fluctuations of random variables. Thus, our requirements are only necessary; they are definitely not sufficient. For example, if all tasks with free paths less than the mean were scheduled together, followed by all others, first the CP would idle, then the channel. On the other hand, if there is one task with an infinite free path, then there is no restriction on the others provided that one is not bumped from core. When a more comprehensive model and some empirical evidence are available, we will be able to generate sufficient conditions for complete overlap.

The Lockout Effect

Suppose we are able to keep the CP ahead of the channel. We will make an estimate on the amount of core necessary to support this — i.e., the amount of core necessary to contain the tasks that are in the page-wait state. To do this, we want to calculate first the amount of time a task spends waiting for a single page, a function of the rotational delay of the drum. Suppose for the moment there are no slot conflicts.

Then the wait time is

$$w = t_1 + j \cdot \tau$$

where

t_1 = a uniformly distributed random variable representing the time to the beginning of the next channel program;

$$0 \leq t_1 \leq T.$$

j = the slot position of the page requested, uniformly distributed over

$$1 \leq j \leq p.$$

$\tau = T/p$ = the transmission time of a page.

Then the mean wait time is

$$\bar{w} = \bar{t}_1 + \bar{j} \cdot \tau = \frac{T}{2} + \frac{p+1}{2} \tau = T \left(1 + \frac{1}{2p} \right).$$

If n pages are requested by a task during a time slice, it spends n times the value \bar{w} in the wait state. When we consider slot conflicts, this value could increase by as much as 50%. However, we must know the stationary distribution of k in order to make explicit calculations.

Let a task begin a time slice. It demands its first page and waits an expected time of \bar{w} milliseconds, and *ties up one page of core for that time*. A short while later it demands its n^{th} page, it ties up n pages of core for \bar{w} milliseconds. During the entire time slice, it causes a total of

$$1 \cdot \bar{w} + 2 \cdot \bar{w} + \dots + n \cdot \bar{w} = \bar{w} \sum_{i=1}^n i = \bar{w} \frac{n(n-1)}{2}$$

page-milliseconds of core to have been devoted to waiting for the drum to spin. These page-milliseconds are not available for any other purpose, but only to support the task for its time slice of length, say, t . In other words, we must expend $\bar{w}n(n-1)/2t$ page-milliseconds of core in page waits to get a millisecond of useful work. I.e., in complete processing-swapping overlap conditions, *an average of $\bar{w}n(n-1)/2t$ core*

pages are tied up waiting for the drum at all times.

Let us calculate an example using the SDC data of Figure 1 applied to the 360/67. From the figure, we see that if $t = 160$ milliseconds, then $n = 24$ pages. For a conservative estimate, we ignore slot conflicts and take $\bar{w} = T[1 + (1/2p)]$. Then,

$$\bar{w} = 36 \text{ msec if } T = 34 \text{ msec, } p = 9;$$

$$\bar{w} = 19.1 \text{ msec if } T = 17 \text{ msec, } p = 4; \text{ and}$$

$$\bar{w} = 5.1 \text{ msec if } T = 3.4 \text{ msec, } p = 1.$$

The total wait-time for all 24 requests is

$$860 \text{ msec if } T = 34, p = 9;$$

$$460 \text{ msec if } T = 17, p = 4; \text{ and}$$

$$122 \text{ msec if } T = 3.4, p = 1.$$

(I.e., the setup time for a 160 msec time slice is 860 msec in the case of the nine-slot drum. During this time, others are computing, but the conversational user will see the delay in the form of poor response time.) The lock-out core amounts to

$$62 \text{ pages for } T = 34, p = 9;$$

$$33 \text{ pages for } T = 17, p = 4; \text{ and}$$

$$8.8 \text{ pages for } T = 3.4, p = 1!$$

With regard to slot conflicts, observe that each conflict adds only 3.4 milliseconds to \bar{w} in the case of $p = 1$, but it adds 34 milliseconds to \bar{w} in the case $p = 9$. Thus, the high probability of conflict on the hypothetical drum is offset by the expense of conflict on the nine slot drum. In actual operation, we would find that the number of pages locked out would be greater than the values we calculated by roughly the same factor for each of the three cases.

These costs in core to support demand paging with conventional drums are very high, and nearly all of it can be attributed to the rotational delay. The analysis can be generalized and the same kind of results can be obtained for file operations from disks. It can also be applied to non-360 time-sharing systems to obtain similar results. Neither must one restrict himself to fixed sized pages or a demand-paging concept. The principle is clear that the best device is one that rotates with a cycle of no more than the transmission time of the smallest swap, or one that does not rotate at all — i.e., LCS.

Affinity Paging From a Drum

Several proposals have been made to improve drum performance over the demand paging case. Most of these involve swapping groups of pages that have an affinity for each other. I.e., if one page is requested, the supervisor recognizes that certain others will be requested with a high probability and initiates the swaps for those at the same time. In this way, the wait time for several requests is overlapped, and the amount of core necessary to support the drum is cut by an appropriate factor. Among the proposals are that of swapping whole programs at once (CTSS at Project MAC), reading in at the beginning of a time slice all of the pages that the task used during the previous one, or maintaining a set of links in the page tables in the supervisor that relates every page to its companions.

One can either require that all related pages be written in contiguous slots on the drum or allow them to be located randomly; each has advantages. In the former case, there is no possibility of slot conflicts

between pages of the same group, and there need be a delay of at most one rotation to access them all. However, if two tasks each request groups of pages, and the sequences of slots for these pages overlap, one task has a very long wait while the other reads plus an additional wait while the drum spins to the proper place. The latency for two independent requests cannot be overlapped as it could in the demand paging case. Furthermore, when the system must write pages, it must find a sequence of slots long enough to contain all of the group. Our analytical techniques are not sufficient for calculating the deliverable page rate or the amount of locked out core under this configuration. Neither can we determine here whether the advantages offset the disadvantages.

In the latter case, where pages are located randomly on the drum, the calculation of the deliverable page rate for the demand paging drum applies. If a task demands m pages, this is equivalent to m tasks each demanding a page, at least from the point of view of the drum. In fact, we increase the effective value of k in those calculations, increasing the swapping rate, without adding more tasks to core. The fact that the latency of the m pages is partly overlapped also reduces the total amount of core time necessary to support a time slice of computing. Clearly, this type of affinity paging is an improvement over demand paging.

If swapping is done from LCS, affinity paging is useful only if the swapping channel is not busy. Since there is no latency time, the amount of waiting for two pages is twice that of one page. If the channel is free, then we can initiate a swap for the task that is executing before it demands that page. But if other tasks are demanding immediate service, they must be handled first to reduce the chances of the CP idling for lack of work in the ready state.

We should point out that we assumed the system supervisor has some way of recognizing page affinities. This might result from a heuristic operating in a demand paging environment that "learns" which pages are related. We might require the user or his compiler to specifically define the relationships before run time. Or some other method could be used. In any case, affinity paging appears to be a necessity for systems committed to using drums for swapping. But the benefits of using LCS go beyond the realization of the hypothetical one-slot drum, as we will see.

Comment

We have seen that a drum cannot deliver pages to tasks at the maximum rate of the swapping channel unless we allow large queues for service to build up. This is because of its inherent rotating nature, which wastes channel time with slot conflicts. Only in the degenerate case of $p = 1$ is it possible to get maximum performance with short queues. The rotational delay causes tasks to spend a disproportionate amount of time in the page wait state, relative to the computing they do; and this eats up core. Affinity paging reduces these problems, but so does LCS with a swapping channel. Carnegie has chosen the latter path.

The concept of giving each user a slice of CP time out of an operational cycle of say, one or several

seconds, has been very popular in time-sharing circles — indeed, some will take it as the definition of time-sharing. But our analysis has shown that there are other costs in providing computer service, such as core space-time, and channel time. If the user demands these in unusual proportions, the system can get bogged down. Perhaps when we allocate his time slice, we should also allocate core time, channel time, I/O time, and other resources. If he exceeds any one allocation, or perhaps if he exceeds some function of them, his turn in the operational cycle should be considered ended. If, for example, we granted a core time slice instead of a CP time slice, he would be entitled to squeeze as much computing out as he could, provided he did only little paging. Or he would be entitled to swap heavily but only compute a little. But whatever the allocation scheme, it should be designed to keep the demands for the various scarce resources in proper balance to avoid waste.

We have examined the system costs with respect to channel time and core space, but we have not discussed the effect of fixed size pages. In the 360/67, this is irrelevant because the hardware is designed for 4096 byte pages. In the larger domain of time-sharing, variable size pages should be considered, for it is apparent that a lot of swapping is done to gain access to only a few words. If only those words were swapped, it might be possible to save significant amounts of overhead. LCS will provide us a crude approximation of this ability by allowing direct accesses to words stored there.

THE CARNEGIE LCS-ORIENTED SYSTEM

In place of a drum, we provide an equal amount of bulk core storage with 8 μ sec cycle time, addressed as an extension of main core. A core-to-core channel (known as the Storage Channel) allows information to be block-transferred from any memory location to any other, independent of and overlapped with CP operation. This channel behaves exactly like any other I/O channel on the system and operates slightly faster than a drum channel. Thus, we can treat the LCS as an on-line device that does the page swapping.

Because there are no rotational delays, the channel can access any page as soon as it finishes a previous operation. In this sense, it is like the one-slot hypothetical drum we discussed above. With it, we can enjoy the maximum possible paging rate without maintaining large queues of idle tasks. The restriction on the mean free path of programs is less than it would be if we allowed only a small number of tasks in core and a low drum paging rate. Perhaps most significantly, we do not need to maintain the extra 30 to 60 pages of fast core to drive the drum. Each task spends less time in main core waiting for pages and, consequently, gets through its time-slice in less real time.

An equally important benefit of LCS is the fact that it is addressable directly by the CP as an extension of main memory. It is possible that when a task references a page, it may not be worth the overhead to swap it. For example, only a few words from the page may be needed for the immediate processing. If the page resided on a drum, it would have to be swapped, no matter what. But if it resides in LCS,

then the page tables can be set so that the CP thinks it is in core and accesses the information directly, word by word. The cost involved is the CP degradation due to the long cycle time of bulk core; the savings come from the fact that there is no swap or other system overhead. The trade-off point is determined by the usage of the page.

For example, suppose that it takes 500 μ sec of CP overhead to process a paging interrupt. Suppose also that it takes 4 μ sec to fetch a double-word in LCS, over and above the normal access time in fast memory. Then by not swapping a page, we can buy 125 direct accesses to LCS; we leave the Storage Channel free for other use; and we do not tie up a page of fast core. One can easily think of many data structures that occupy a thousand words, but are not referenced more than 125 times per time slice: e.g., a data set catalog, a portion of a large IPL-V list, or a string of post-fix code to be executed by an interpreter.

A. L. Sherr has pointed out that there is much to be gained from small page sizes, provided the overhead of swapping can be conquered.⁴ What the LCS configuration does is provide two different page sizes—the one is the 4096 byte page which is swapped, but which remains available throughout a time-slice; and the other is a double-word “page” which is accessed only at the cost of an LCS cycle, but which is highly transient and must be re-accessed each use. Each serves its own function; the larger supports normal computing, while the smaller provides efficient access to large data structures. This duality decreases the rate of demand for swapped pages by the task, or equivalently, increases the ability of the system to meet the demand rate.

The question of how to decide which pages should be swapped and which should be accessed directly is an unsolved one, not unlike the question of defining affinities between pages. We propose no solution here, but we observe that a simple method is to require users and compilers to identify which pages are which. Certain stimuli can be created to induce users to do this efficiently, but caution is important. Our object is to fit the machine to the users, not the users to the machine.

The Machine Configuration

Figure 5 shows the single-processor simplex system initially installed. The machine differs from a standard 512K byte 360/67⁵ by including over four million bytes of IBM 2361 Large Capacity Storage and the Storage Channel for core-to-core transfers. No drum will operate in the system. The LCS has an 8 micro-second memory cycle, a 4 microsecond access time, an 8 byte (64 bit) data width, and is two-way leaved. Thus, it can support a data rate of two million bytes per second. The Storage Channel is controlled by the same type of channel program as other 360 channels, and can transmit 1.6 million bytes per second (400

pages/second) between locations in core.

This machine costs more than the equivalent drum machine. Suppose c is the cost of a basic 512K 360/67 with one drum and a normal complement peripheral gear. Then, the drum and its channel represents about 7% c , while the same capacity of LCS (with

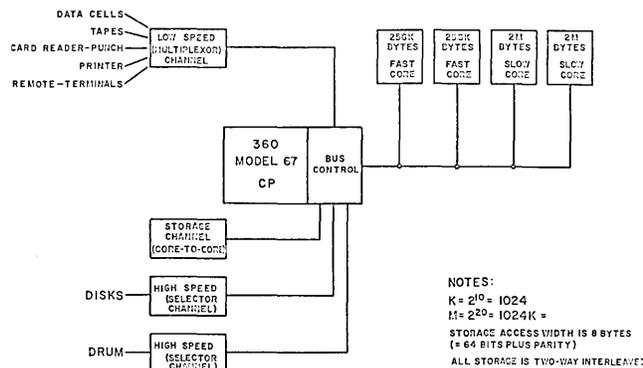


Figure 5. Simplex 360/67 with LCS

Storage Channel) costs 25% c . The amount of fast core locked out by the drum, but which is available for other use in the LCS system, cost 6%-12% c . The same basic system with LCS cost

$c - (\text{drum}) - (\text{locked out core}) + \text{LCS}$
 or 7%-12% more than the drum machine. However, for this, we get a faster paging rate and a much more flexible machine.

A duplex system scheduled for operation at Carnegie in the future is shown in Figure 6. The system has two Central Processors and two Channel Controllers, each with an independent access path to memory modules. Attached to each Channel Controller is a Storage Channel as well as conventional multiplexor and selector channels. There are no drums, but other I/O devices are configured in the same way as on a standard Model 67.

A half-duplex system is essentially half of the system in Figure 6; i.e., one CP and one Channel Controller each with an independent access to memory. It is logically identical to the simplex system, but functionally the conflicts between I/O, Storage Channel, and CP are resolved at the core modules rather than at the storage bus. The resolution circuitry introduces a delay of 150 nano-seconds per memory access, which degrades CP performance from specifications. However, high I/O rates and Storage Channel transmission *also* degrade CP performance in a simplex system by causing memory bus interference. The trade-off point between the simplex and half-duplex systems was determined by simulation⁶ and corroborated by analysis of manufacturer's reports. Essentially, if the utilization factor of the Storage Channel is less than approximately 50%, then the simplex system gives better performance. Otherwise, the half-duplex system gives better performance. There is no suitable half-duplex machine available to compare to the simplex machine

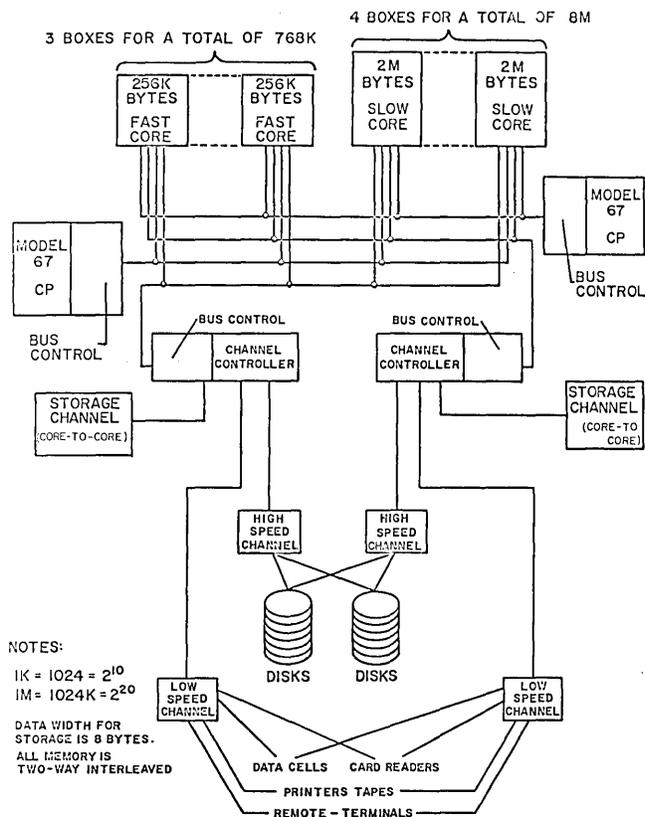


Figure 6. Duplex 360/67 with LCS.

in order to verify these results. If the present analysis holds up, Carnegie will upgrade its initial system to a half-duplex machine when practical.

CONCLUSIONS

From the analysis presented in this paper, Carnegie Institute of Technology has discovered that it cannot live with time-sharing on a drum-oriented machine with demand paging. The swapping rates which it can support are too low for practical operation, unless we admit a lot of extra, expensive main core. Paging from bulk core, where there are no slot-conflicts, yields a factor of two to four better performance. At the same time, the LCS allows a reduction in the page demand rate because it can be directly referenced. We have also discovered that the inherent rotational delay of the drum has the effect of withdrawing 30 or more pages of memory from usable core at all times. This in itself is expensive.

We recognize that, like all models, our model is only an approximation. However, we feel confident that we have effectively handled the first major problem of understanding what is required to make time-sharing work. Whether we have made forward progress or whether another equally big problem is hiding behind this one, only time will tell.

All of the improvements that come with LCS are

needed, and they more than justify the extra expense. A rotating memory is too inflexible and inaccessible to support a comprehensive time-sharing facility, just as it was found to be too inflexible and inadequate as the main memory for second generation computers.

In fact, before the "fourth generation", we will probably find that large non-rotating memories assume increasing importance both as swapping devices and storage for large on-line files. Carnegie cannot afford to wait for this trend.

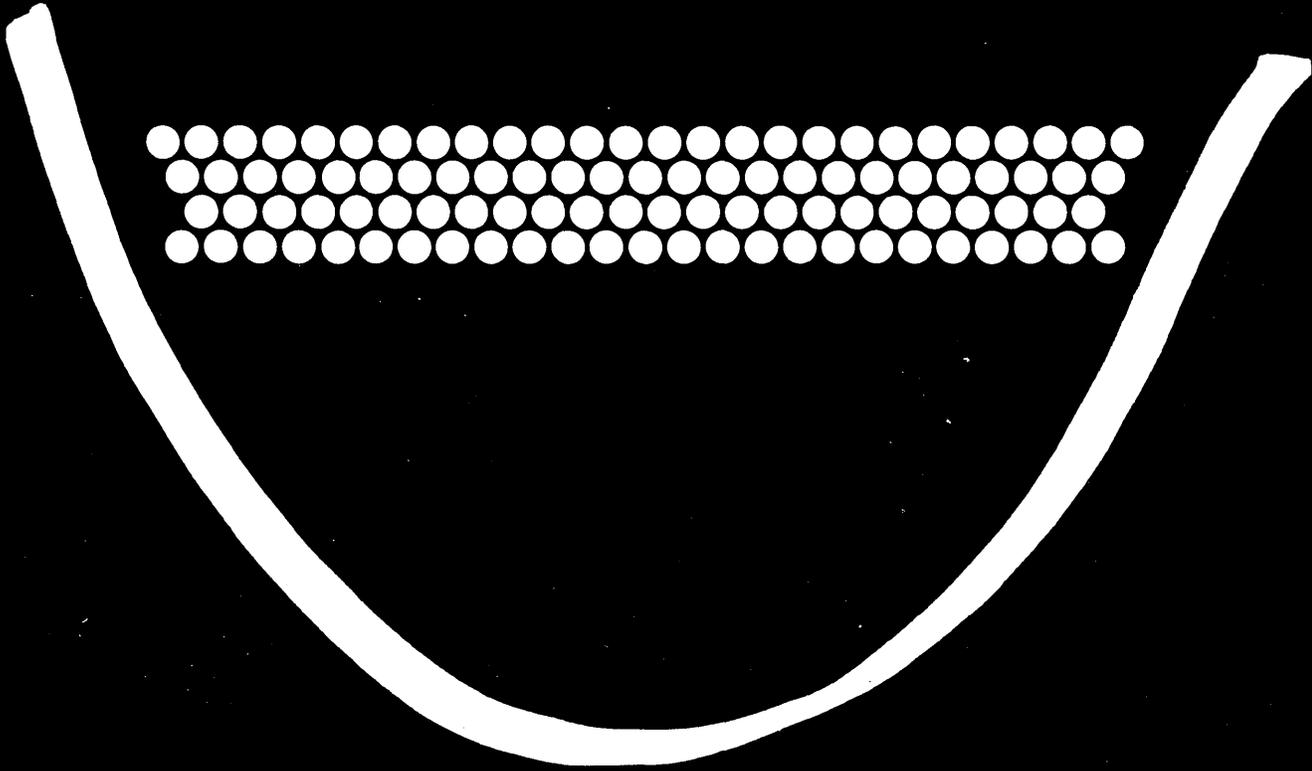
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SUMMARY OF RECENT EXPERIENCE WITH TSS/360 AT CARNEGIE-MELLON UNIVERSITY

Since the time the foregoing article was prepared, an implementation of LCS in a pre-release version of TSS (Version 58) was done to test the validity of the theoretical analysis. It was found that paging from LCS did reduce central processor idle time significantly, but a much bigger reduction in system overhead was accomplished by allowing direct reference to pages in LCS. Sharable pages—mainly system pages and pages containing pure procedure—were swapped between LCS and fast memory, while private pages—those containing mostly data—were left in LCS for direct reference. While this algorithm is certainly not optimal (and is probably very far from being optimal), we did obtain performance improvements of more than two orders of magnitude over the drum-oriented TSS. These results were obtained by running conversational assemblies with syntax checking from eight terminals, the maximum number lines available at the time. It must be noted that the results were heavily corrupted by bugs in both systems and by the fact that the experimental job stream was not necessarily representative of reality. However, we expect the performance improvement to carry over to stable, usable versions of TSS with 30-50 terminals under actual operating conditions.

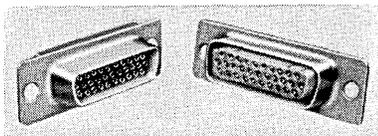
An implementation of LCS in the new version of TSS is currently being done. Additional work is being done in the area of core management for LCS and on decision algorithms for referencing pages in LCS directly or not. A more detailed report of this work will be presented at the 1968 ACM National Conference.



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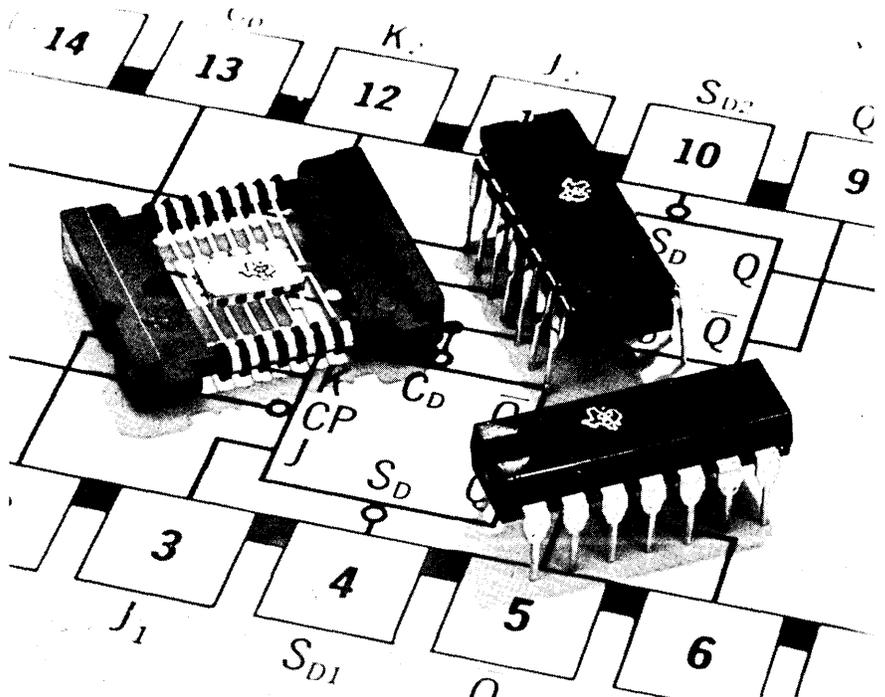
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NEW PRODUCTS



DTL INTEGRATED CIRCUITS

Four dual flip-flops, two hex inverters, and three fast-rise-time gates have been added to Texas Instruments' Series 930/830 DTL line. All are available in flat-packs and ceramic and plastic dual in-line packages, and with military or industrial temperature ratings. Two of the dual J-K flip-flops—types SN15 9093 and SN15 9094—are dual versions of standard single 945 and 948 DTL flip-flops. Types SN15 9097 and SN15 9099 include common clock and clear capability. For greater reliability, all four dual

flip-flops are single monolithic bars, instead of two interconnected chips. Prices range from \$9.30 to \$2.86. The hex inverters, types SN15 936 and SN15 937, are six inverting gates capable of cross-connection as flip-flops. Prices range from \$5.50 to \$1.68. Fast-rise-time gates, the SN15 949 quad gate, the SN15 963 triple gate, and the SN15 961 dual gate, have 2000-ohm pull-ups for higher speed. Prices are \$1.50 for the quad and triple gates and \$1.40 for the dual gate. Texas Instruments, Dallas, Texas.

Circle Number 217 on Inquiry Card.

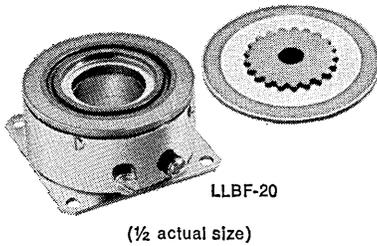
TIME/SHARE DISCFILE

The first high-capacity random access Discfile memory system, model 5085, designed specifically for time-sharing applications, stores over 5 billion bits, and features lower access times and greater operational flexibility than has been previously available to the industry. The new system introduces a unique modular concept which permits preventive and corrective maintenance to be performed upon individ-

ual components while the remaining modules are operating on-line with the computer. Each positioner module can be withdrawn, and individual heads, arms, or associated electronics can be serviced without shutting down the system. Preventive maintenance devices, which monitor critical system components, are incorporated so that failures can be anticipated and avoided. Data Products, Culver City, California.

Circle Number 201 on Inquiry Card.

APILON®- FACED COMMERCIAL CLUTCHES/BRAKES

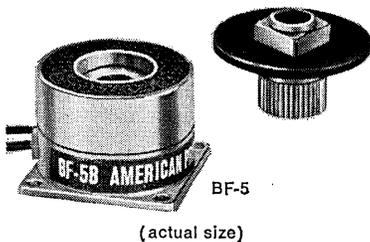


American Precision Industries' Apilon®-faced electro-magnetic clutches and brakes, at rated loadings, have life expectancies of 100 million cycles. The unique Apilon® friction facing outlasts conventional types 10 to 1, virtually eliminating the need to replace facings. An added benefit—no unsightly or contaminated wear products.

Apilon® ceramic friction-faced clutches and brakes are ideally suited for applications where unusually severe loads are placed upon the product for long durations, such as in high-speed printers or in tape tensioning devices where continuous slippage occurs.

Units are available in ratings of 2 lb. in. to 70 lb. in. of torque, in sizes of 1" to 2 5/8" body diameter.

HIGH-TORQUE COMMERCIAL CLUTCHES/BRAKES



A low-cost line of commercial clutches and brakes is also available for less demanding applications.

These units can transmit torque without burnishing and are available in the same size and torque ratings as the Apilon® line. Standard coil voltage, 24 VDC. Other voltages available at no additional charge.



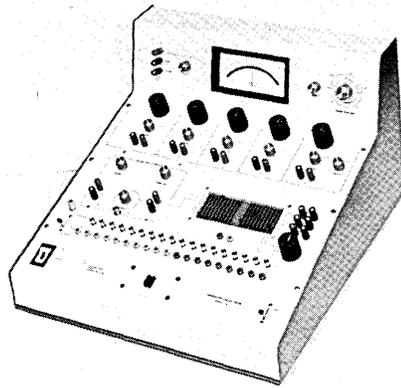
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CIRCLE NO. 64 ON INQUIRY CARD

NEW PRODUCTS



INTEGRATED CIRCUIT TESTER

Tester for integrated circuits, designated Model 7101, is designed for laboratory analysis and incoming inspection of a variety of circuit types including RTL, DTL, TTL and ECL. The tester contains four adjustable voltage supplies, a current supply and a 10 MHz square wave generator for providing test forcing functions. DC measurements are made on a 1% taut band meter, and oscilloscope connections can be made for dynamic measurements. Computer Test Corp., Cherry Hill, N.J.

Circle Number 228 on Inquiry Card.



LIMITED MESSAGE FIFO BUFFER

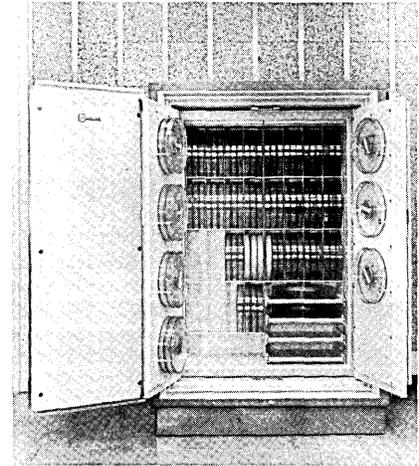
A limited message FIFO buffer, designated the 608E-2, is said to fill the need for low-cost buffering of small messages from keyboards, card readers, printers, punches, or teletype and telephone data communications systems.

Designed with all the addressing and control logic, the system inputs are serial or parallel data, load and unload commands, and DC power. Outputs from the system are serial or parallel data, shift-in and shift-out pulses as required, and clock. Storage capacity is up to 8192 bits.

Input and output data rates of up to 4800 baud can be accommodated.

Package size is approximately 12" x 14" x 1 1/2". System can be supplied for 19" relay rack mounting with a 1 3/4" panel height. Digital Devices, Syosset, N.Y.

Circle Number 229 on Inquiry Card.



UL-APPROVED TAPEGUARD SAFE

Tapeguard safes for protecting data processing tapes and disc packs against the hazards of fire, smoke, and moisture have been approved by the Underwriters' Laboratories. Originally introduced in 1965, the Tapeguard safe is now constructed with a new, lightweight insulation that has reduced the total weight and allows greater storage capacity. Sectional interiors accommodate disc packs or tape seals, or a combination of the two. Interior flexibility includes storage of tab card and microfilm trays, NCR Cram cartons, IBM Data Cells, etc. Mosler, Hamilton, Ohio.

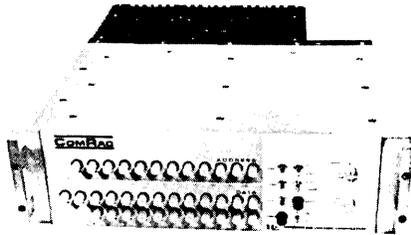
Circle Number 230 on Inquiry Card.

DATASET ELIMINATOR

A passive crossover network is said to eliminate type 103A, F & 202C, D datasets between customers EDP equipment & the remote terminal for lab checkout purposes or for installations to 2000 feet.

Interface to the E103 is two standard 25 pin RS232B female connectors. The remote terminal dataset cable plugs into one connector and the EDP dataset cable into the second. Normal data & control functions are maintained. The unit occupies less than 6 cubic inches and is contained in a steel case. Western Telematic, Arcadia, California.

Circle Number 225 on Inquiry Card.



1μs CORE MEMORY SYSTEM

Line of 1 microsecond core memory systems designed specifically for small data processing and data collection systems, designated the ComRac Series (Commercial Random Access Core), will be available in several models. The ComRac 100 exhibits a cycle time of 1 microsecond, an access time of 0.45 microseconds and is available in capacities up to 4096 words by 24 bits or 8192 by 12 bits. The memory systems are organized as four-wire current systems and employ 20 mil lithium ferrite cores. They can be operated in the standard modes of Read/Restore, Clear/Write, Buffer Read, and Buffer Write. The entire memory including power supply, is packaged in a 5 1/4 inch rack-mounted chassis. Interface characteristics are designed to be compatible with DTL and ITT logic. Information Control, El Segundo, California.

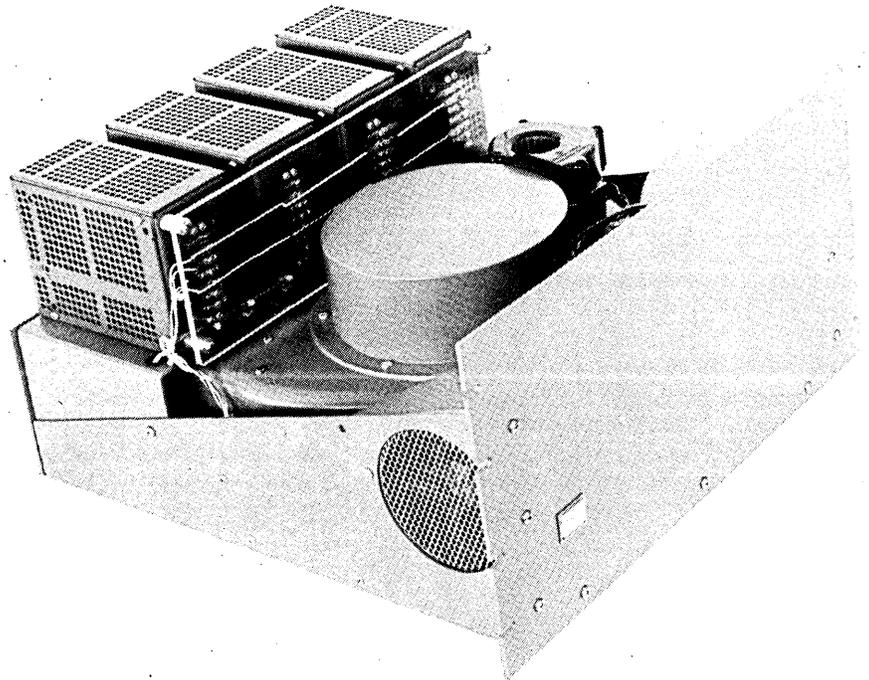
Circle Number 203 on Inquiry Card.

PORTABLE TIME-SHARING TERMINALS

The TC-1 Teletype carrying case is said to be specially designed to house the model 33 KSR Teletype to make it portable. The TC-2 is for the ASR version. Available as accessory equipment for those who already own a Model 33 Teletype, the cases can also be supplied as a system with the Teletype and connection cable to the company's portable acoustic data couplers installed. Together with the ADC 260 Acoustic Data Coupler they provide a portable remote terminal for computer time-sharing use which can be employed wherever there is an ordinary telephone available. Weight of the KSR in its case is approximately 65 lb. Weight of the ASR version is about 75 lb. Anderson Jacobson, Mountain View, California.

Circle Number 210 on Inquiry Card.

more display channels per dollar



Data Disc's new digital/video disc memory opens a whole new world of display possibilities. Think about how you can use up to 72 completely independent tracks — each with its own head and read/write/clock electronics — to store up to 100,000 bits per track — accessible at a 3 megabit/second rate.

Because the data is clocked in and out, using TTL logic, track-combining techniques can provide up to 7.2-megabit capacity at up to 216 megabits/second. Write on any track without disturbing the displays being read from adjacent tracks.

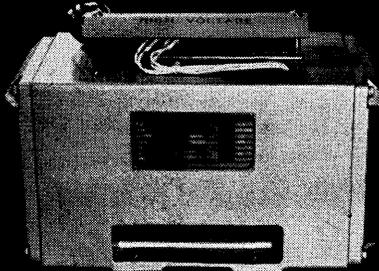
Applications include X-Y CRT and TV-monitor refreshment, digital-television storage, and high-speed parallel buffer memory.

Price for the FPD? \$4,870 plus \$300 per track. Delivery? 30 days! Application and interface details? Call Bill Stevens at (415) 326-7602 or write:

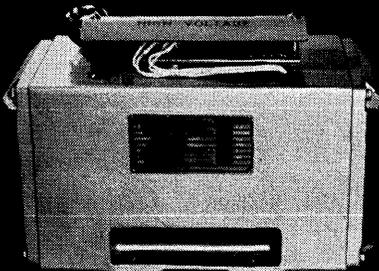
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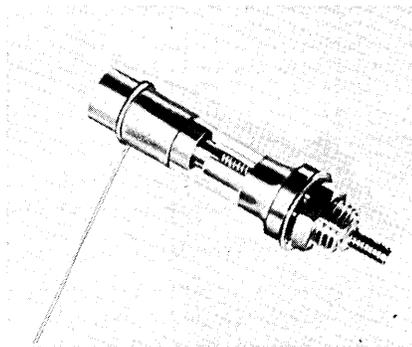
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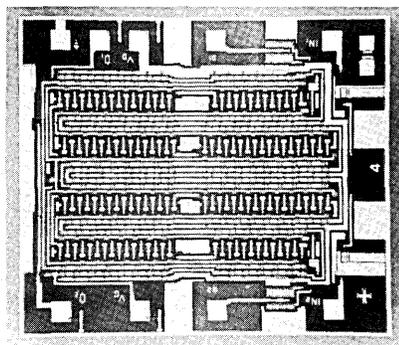
NEW PRODUCTS



NON-MAGNETIC TRIMMER CAPACITOR

Trimmer capacitor constructed entirely out of non-magnetic materials, type V1288, is of the rotating piston design and features internal arms from the bushing which form a sliding contact to the rotating shaft-piston assembly. This is said to provide a direct electrical contact to the bushing and eliminate the necessity of using the screw as a current carrying part. The capacitor has a range from 0.7 pf to 18.0 pf. Its Q factor is 550 measured at 20 MC. Direct current working voltage is 750 volts and dielectric withstanding voltage is 1500 vdc. Temperature coefficient is +400 PPM/°C. A feature is that it exhibits no self resonance to above 1200 MC for high frequency applications. Voltronics, Hanover, New Jersey.

Circle Number 214 on Inquiry Card.



"COMPUTER-DESIGNED" MOS INTEGRATED CIRCUITS

Computer-aided design of MOS integrated circuits is said to promise more flexible custom IC development; shorter, more economical production runs; and faster logic-

to-product time. The line, believed to be the first cataloged semiconductor products designed by computer, consists of dual 16, 25, and 32-bit static shift registers, a dual full adder, a dual 3-input NOR gate, a 6-channel analog switch and an R-C coupled audio amplifier. All are immediately available. Texas Instruments, Dallas, Texas.

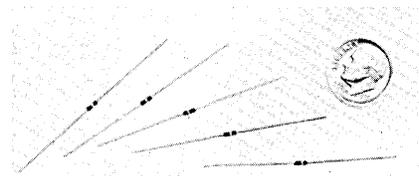
Circle Number 215 on Inquiry Card.

HEAT-SENSITIVE DECALS

A temperature indicating decal, called Temp-Plate, is said to give a permanent, irreversible reading and record of peak temperatures. The product utilizes a spot of pastel-colored chemical which instantly turns black when heat reaches a calibrated level of specified temperatures from 100-1100°F. The product is a precision instrument, providing an accuracy factor of ±1%.

Easily applied, it will adhere to any clean, dry surface. Designed for use wherever a record of high temperature is needed and it is impractical to take a continuous reading from a standard temperature gauge, the decals have fifty-four temperature selections, in any desired size or number of indicators. Temp-Plate, Santa Monica, California.

Circle Number 212 on Inquiry Card.



SUBMIN MONOLITHIC CAPACITOR

Type MA capacitor is a molded, axial-lead unit, measuring only 0.130" long by 0.045" in diameter. It is claimed that this is the smallest monolithic molded capacitor available. Capacitance ranges to 820 pf are offered at 50 volt dc rating and to 470 pf in the 100 volt dc rating, both in BX characteristic.

Tolerances of ±5%, ±10%, and ±20% are available, and all values perform in accordance with MIL-C-11015 requirements. Prices range from \$0.39 to \$2.88. American Components, Conshohocken, Pennsylvania.

Circle Number 213 on Inquiry Card.



RECTANGULAR CATHODE RAY TUBE

High-deflection sensitivity and high-brightness are two of the features that make this new electrostatically-focused cathode ray tube useful for oscillographic and data display applications. The tube has a center line width of 0.015 inch (15 mil) and acceleration of the electron beam occurs after electrostatic deflection. The 5-1/2 x 4-1/2-inch cathode ray tube, designated type WX 30764, has an aluminized, rectangular screen. Westinghouse Electronic Tube Division, Elmira, N.Y.

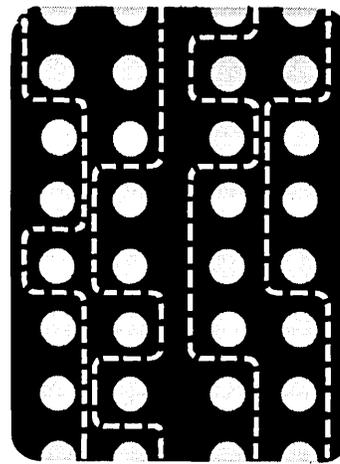
Circle Number 222 on Inquiry Card.

COMPUTER POTS

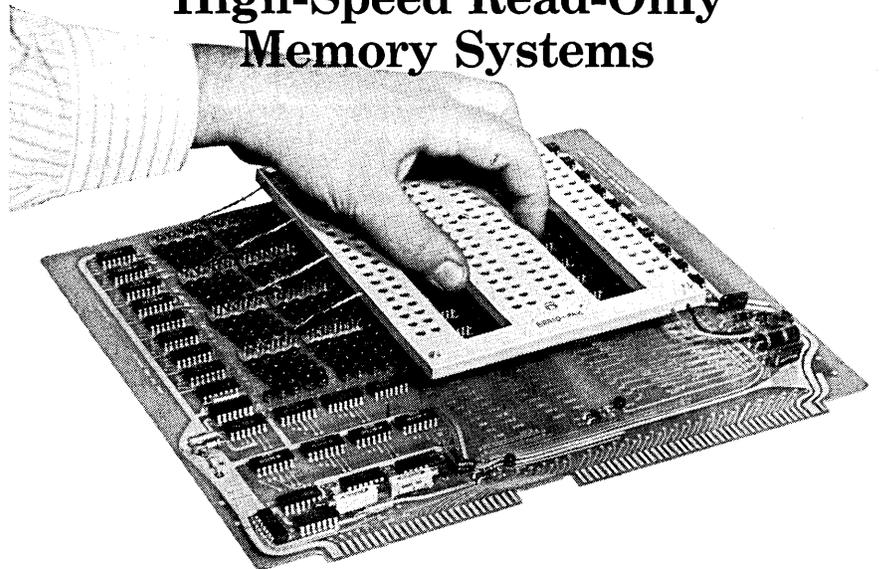
Line of electronic components includes a new "infinite resolution" potentiometer for advanced airborne and other types of computer systems. Several models of a conductive plastic potentiometer are available in metal housings ranging from 7/8 inches to 3 inches in diameter. The devices are incorporated in computation equipment to control electrical potentials as applied to computer circuits.

The new CP potentiometers can be used for as many as 100,000,000 cycles of operation, which amounts to approximately twice the useful life of conventional wire-wound devices, according to the producer. The devices are said to be particularly suited to computation equipment used on advanced aircraft fire control systems, or industrial on-line process control systems. Perkin-Elmer, Norwalk, Connecticut.

Circle Number 202 on Inquiry Card.



"BRAID-PAK" reduces cost of High-Speed Read-Only Memory Systems



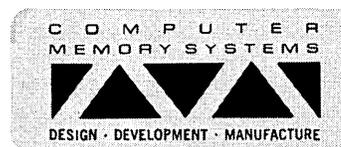
By combining the art of braiding with electronic logic, Memory Technology's new high-speed, read-only "Braid-Pak" Memory Systems cost significantly less, yet provide far better performance than systems using conventional storage techniques.

There are two classes of these non-volatile, high-speed, read-only braid transformer memory systems. One class provides capacities up to 10,000 bits. The other accommodates up to a million bits or more. The illustration shows the Model SBS-1B, a complete 10,240 bit Memory System on a 10" x 13.5" printed circuit board. The memory pro-

gram may be changed by simply replacing the "Braid-Pak" as shown. All inputs and outputs are buffered and feature DTL and TTL compatible integrated circuits with 500 nanosecond read-cycle and 200 nanosecond access times.

Applications include binary word generators for CRT displays, code conversion, pattern generation, computer micro-programming, look-up tables, industrial process control, high speed arithmetic computation, automatic typesetting, automatic machine controllers and other fixed read-only memory requirements. Write for data.

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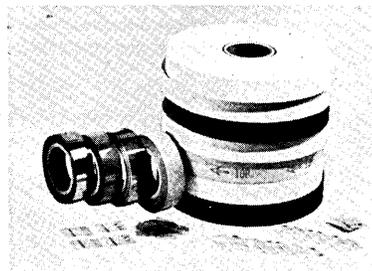
NEW PRODUCTS

VERTICAL-READING MICROFICHE

New method permits computer paper print-out columns to be micro-filmed with a rotary copying camera, and the film is then applied to an optically-clear acetate sheet with a special pressure-sensitive adhesive. Computer film output can be applied directly to the sheet. The computer can be programmed to stop and skip spaces so that each column can be clipped and edited to be compatible with the space on the sheet.

Each resultant 105mm x 145mm microfiche can hold up to nine columns or approximately 10,000 lines. Other fiche configurations up to 5" x 8" are also available. The vertical reading format is claimed to assure faster data retrieval and to simplify handling and filing. Atlantic Microfilm, Spring Valley, New York.

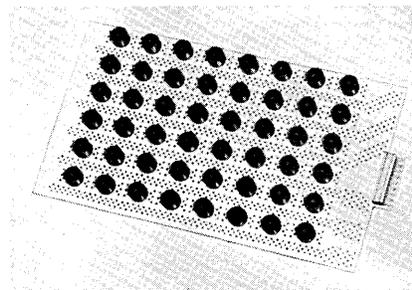
Circle Number 226 on Inquiry Card.



PERFORATOR TAPES SAMPLER KIT

Kit containing sample rolls of 11 different perforator tapes contains representative samples of the complete Robins line for computer, data processing, communications, and numerical control applications. It is priced at \$27.50. Said to be ideal for testing, experimentation and trials, as well as for actual use, the kit consists of paper, laminated mylar, and cellulose tapes, one-inch wide, which come in an assortment of colors and vary in length, depending on the material, from 100 to 1,000 feet. Included are a quantity of both paper and mylar tape splicing patches. Robin Industries, Flushing, N.Y.

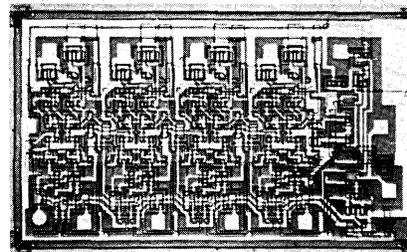
Circle Number 227 on Inquiry Card.



LARGE-CAPACITY, HI-TEMP BREADBOARDS

Breadboards which are operational over a range of from -65° to 150°C and can accommodate up to 56 eight-lead "TO" integrated circuits or 48 of the ten-lead type are designed for simultaneous quantity testing or aging of "TO" devices, or for the plug-in interchange of these I.C.'s in developing circuit configurations. The breadboards feature a large number of spring jacks (a total of 1524 on the eight-lead board) for maximum flexibility in I.C. arrangement or interconnection. Barnes Corporation, Lansdowne, Pennsylvania.

Circle Number 221 on Inquiry Card.

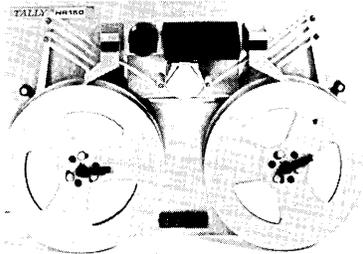


TTL SHIFT REGISTERS

Three complex-function, integrated-circuit shift registers are said to reduce IC package count, and improve system reliability by eliminating many wires required in conventional designs. As an example, a new 14-pin left-right shift register replaces two dual J-K flip-flops and two dual AND-OR-INVERT gates having a total of 56 pins. The circuit series includes 4-bit and 5-bit shift registers with parallel-input capabilities matched to either parallel or serial outputs. Primary applications for these devices are shift-left/shift-right registers, storage

register generator counters. First registers, shift counters, Johnson counters, and shift-register generator counters. First production runs will appear in air-control information systems, airborne computers, electronic-counter-measure receivers, and industrial radiation counters, according to the manufacturer. Texas Instruments, Dallas, Texas.

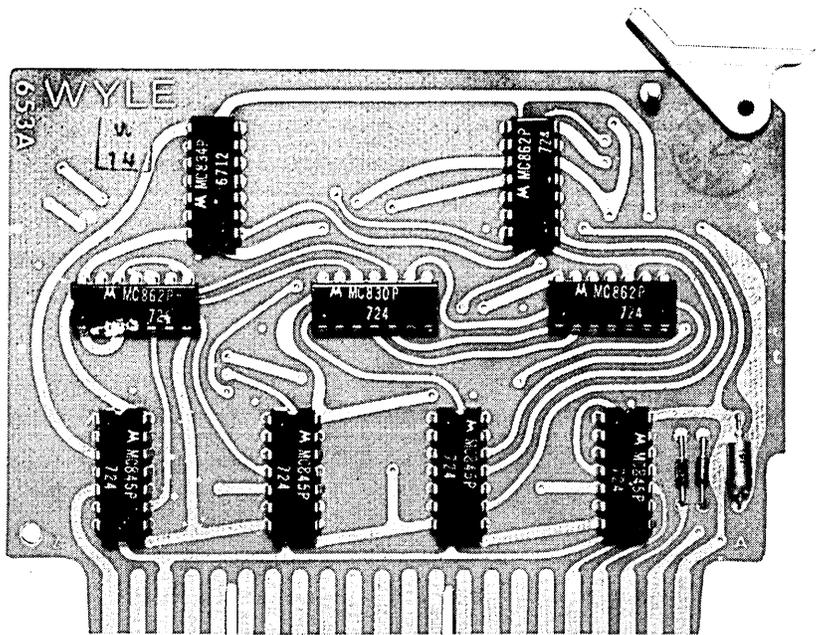
Circle Number 218 on Inquiry Card.



HI-REL READER

A new high-speed, high-reliability, perforated tape reader that features extremely long operating life with essentially zero preventative maintenance and minimum corrective maintenance has been announced by Tally Corporation. The new reader, designated the HR-150, operates asynchronously and bidirectionally at up to 150 characters per second. High-reliability in the reader is achieved principally through the incorporation of a new stepping motor technique, which is said to achieve true step-by-step operation and avoid the wear caused by continuously moving parts. Projected minimum life before even minor failure is 10,000 hours. In typical reader application situations, failures would occur less than once a year. Even then, downtime would be exceedingly low, according to the producer. Other features include compact modular design and low noise level. The unit is available with or without integral reeling. Options include end of tape sensor, tape motion sensor, teletypesetter configuration and solid-state drive electronics. Basic price is \$855. Delivery is 60 days after receipt of order. Tally Corporation, Seattle, Washington.

Circle Number 219 on Inquiry Card.



WYLE LOGIC MODULES

FAST DELIVERY

TECHNICAL ASSISTANCE

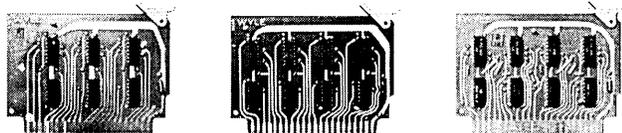
LOW COST

GENERAL PURPOSE DESIGN

BROAD SELECTION

TEN-YEAR WARRANTY

STATE-OF-THE-ART DESIGN



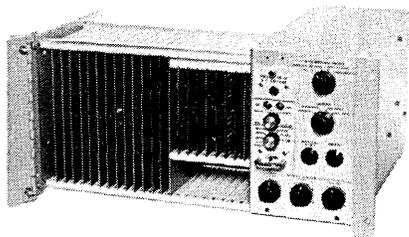
The above are some of the subheads in the Wyle Integrated Circuit Logic Modules short-form catalog. They are seven of the twelve reasons Wyle logic cards may be your best buy. If you want to discuss the other five reasons (or get more detail on the Big Seven), drop us a line on your company letterhead, and we'll send you the catalog. Or better still, call Don Tothe, our product manager, and let him fill you in on what Wyle can contribute specifically to your system. Systems Division, Wyle Laboratories, 128 Maryland Street, El Segundo, California. (213) 678-4251.

WYLE

CIRCLE NO. 69 ON INQUIRY CARD

Need to sample low-level transducers?

cut your per-channel cost with IEC's new MX 500 Series Low Level Analog Multiplexer.



The MX 500 benefits both designers and users of Data Acquisition Systems:

- Eliminates data amplifiers in each channel
- Reduces system costs sharply
- Simplifies system interface
- Reduces system size, power, and cooling
- Increases system reliability
- Simplifies system checkout and operation
- Reduces system maintenance and spares

Outstanding features include:

- ± 5 mv to ± 500 mv full scale inputs (± 10 v full scale output)
- Up to 50 kHz sample rate
- Easily expandable up to 1000 differential, guarded channels
- 120 db common mode rejection
- Sequential or random address channel selection
- Automatic and programmable gain selection
- Overload protected
- Solid state—FET switches—IC logic
- Available with or without AD converter

The new MX 500 interfaces easily with any Data Acquisition System. Need more information on how you can use the MX 500 in your system? Simply call or write, today.



IEC

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Subsidiary of "AUTOMATIC" SPRINKLER CORPORATION OF AMERICA

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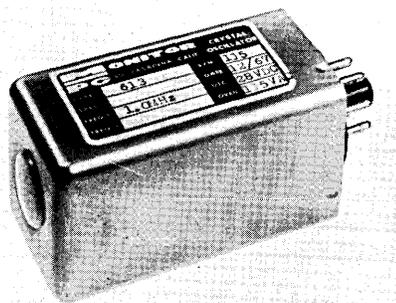
CIRCLE NO. 70 ON INQUIRY CARD

NEW PRODUCTS

INCREASED MAGNETIC-LEDGER STORAGE

Users of the series 500 computer will now be able to increase the magnetic-ledger storage capacity of their systems by 50 percent, according to the producer. By decreasing the space between words of information stored on the magnetic stripes, the storage density has been stepped up from 216 digits to 324 digits. Systems are said to be easily equipped with a "retrofit" feature on the customer's premises, to adapt the system to their present magnetic ledger cards. Increased storage capacity is expected to be extremely helpful to hospitals, for example, due to the insurance and Medicare data which now complicate patient accounting. Over 1,500 systems have been installed in hospitals, small manufacturing firms, government units and other organizations. National Cash Register, Dayton, Ohio.

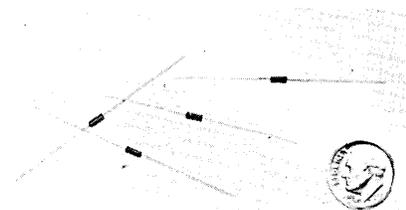
Circle Number 223 on Inquiry Card.



PRECISION FREQUENCY STANDARD

Model 613, 1000KHZ precision frequency standard combines a solid state switching oven, high-reliability crystal and integrated circuit oscillator with a T.T.L. output. Frequency stability of the Model 613 is $\pm 7 \times 10^{-9}$ per day typical, after 30 days of dynamic aging. Power input is 115VAC or 28VDC to the oven and 12 or 28VDC to the oscillator. Output is square wave; logic "0" + 0.45V max., logic "1" + 2.8V min., into a 2K ohm load. Monitor Products, South Pasadena, California.

Circle Number 211 on Inquiry Card.



MOLDED RN50 and RNR50 MINIATURE RESISTOR

A molded precision metal film resistor, 0.065" diameter by 0.150" long, features rugged end-cap construction. The resistor, ACI Type EE-1/20, conforms in all respects to type RN50 of MIL-R-10509F and RNR50 of MIL-R-55182C. Range coverage is from 10 ohms to 110K, and higher values to 500K are available at reduced specifications. Wattage rating is 1/20 at 125°C. Prices range from \$0.19 to \$2.07. American Components, Conshohocken, Pennsylvania.

Circle Number 220 on Inquiry Card.

DIGITAL PLOTTER

Digital plotting system operating from punched paper tape, called the PTD system (Punched Paper Tape Delta Incremental Plotting), plots engineering variables from time-shared computers at a remote terminal or verifies tapes for numerical control machine tools.

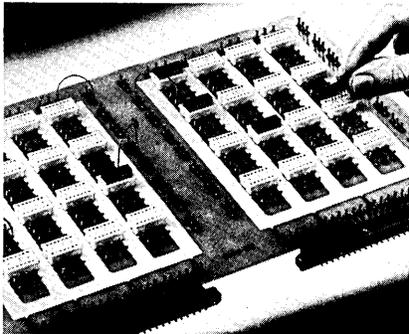
Special features include multiple-step programming, which allows up to 127 incremental steps in either of two two-dimensional directions from a single input command. This type of programming allows the plotter to be driven from paper tape supplied by a teletype, and is ideal for remote-terminal graphics, permitting data to be transmitted in delta format, affording significant savings in computer and transmission time. The system employs either a low-cost 12-inch plotter or a more flexible 30-inch plotter. Computer Industries, Van Nuys, California.

Circle Number 224 on Inquiry Card.

OPTICAL CHARACTER SCANNER

A new optical character scanning system, which speeds up getting information into computers, reads both hand and machine-printed characters and transfers the data directly to magnetic tape for input to computers. The OpScan 288 consists of two units. One transports the documents, scans them, then stacks them. The other unit contains the logic circuitry needed to put the data from the documents onto magnetic tape. The system is free-standing and operates off-line, completely independent of the main computer. The basic price is \$98,088, or rents for a monthly fee of \$1,988. The monthly rental fee is approximately equal to the monthly salary and overhead cost of only four keypunch operators, according to Optical Scanning Corporation, the producer.

Circle Number 205 on Inquiry Card.



IC BREADBOARD PANELS

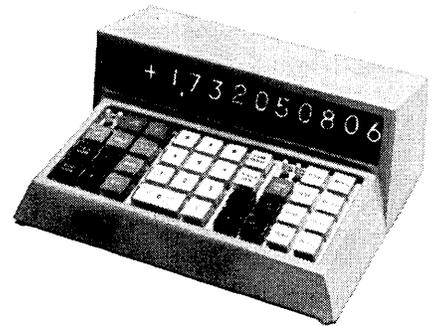
A new Series of integrated circuit panels called "Omny-Pac" made for breadboarding new IC designs with 16 or 32 plug-in type dual-in-line IC sockets and featuring a new laminar bus bar design for power and ground distribution, has been developed by Methode Manufacturing Corporation. The Series consists of two Omny-Pac breadboard panels which combine advanced circuit design and engineering concepts of several of Methode Electronics' divisions. Each socket is designed for easily inserting 14-pin dual in-line IC's. The rugged, one piece, molded 14-pin socket body is approximately .850" long, .450" wide and .250" high and incorporates a visual index slot matching that of the indexing slot of the IC. Methode Manufacturing, Rolling Meadows, Illinois.

Circle Number 207 on Inquiry Card.

The keys to Log & Exponential power



...exclusively on WANG electronic calculators



Wang's unique approach to data manipulation (a revolutionary electronic circuit which digitally generates the natural logarithm of any number entered) reduces complex calculations to simple, logical keystrokes and eliminates from 67 to 93 per cent of calculation time.

On keyboard displays, about the size of a telephone, all basic arithmetic functions ($+$, $-$, \times , \div , $\frac{1}{x}$) are performed silently, in milliseconds. Optional keys produce X^2 , \sqrt{x} , $\text{Log}_e x$, e^x by a single keystroke. (For unmatched economy, up to 4 keyboards can operate simultaneously from a briefcase-

size electronics package located up to 200 feet away.)

Other options include: 4 additional random-access storage registers (two are standard), 80 step, plug-in card programmer and/or built-in programs for single keystroke calculations of $\sin \theta$, $\cos \theta$, $\arcsin x$, $\arctan x$.

Add-on compatibility makes it possible to expand into a powerful computing system that will branch, loop, do sub-routines, make decisions and manipulate arrays. *There is nothing comparable, anywhere.*

For complete information, write or call:

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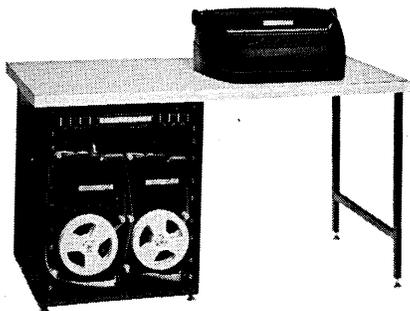
In Major Cities, Tel:

(201) 241-0250	(215) 642-4321	(313) 278-4744	(412) 366-1906	(514) 482-0737	(702) 735-5802
(203) 666-9433	(216) 333-6611	(314) 727-0256	(415) 454-4140	(518) 463-8877	(713) 668-0275
(205) 245-6057	(301) 588-3711	(317) 631-0909	(416) 364-0327	(601) 234-7631	(714) 234-5651
(206) 622-2466	(301) 821-8212	(319) 365-2966	(504) 729-6858	(612) 881-5324	(717) 381-5440
(212) 682-5921	(303) 364-7361	(402) 341-6463	(505) 255-9042	(614) 488-9753	(717) 397-3212
(213) 278-3232	(305) 841-3691	(404) 457-6441	(512) 454-4324	(617) 851-7311	(816) 421-0890
(214) 361-4351	(312) 456-1542	(405) 842-7882	(513) 531-2729	(702) 322-4692	(817) 834-1433
					(919) 288-1695

CIRCLE NO. 71 ON INQUIRY CARD

INVAC

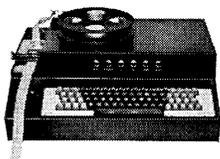
PERFORATED TAPE INPUT/OUTPUT SYSTEMS



INVAC Tapemaker Systems range from comprehensive I/O Typewriter-Punch-Reader Consoles to relatively simple desk-top units. Typical applications include check-out systems, computer programming, and data logging; machine control, data processing, and tape duplication.

- ... Many Standard Options Available
- ... Customized for Specific Applications
- ... Full Operational Mode Flexibility
- ... Complete Code Compatibility
- ... On Line or Off Line Capability

MODEL PKP-200
Keyboard-Punch
Tapemaker is a tape
preparation system
designed for machine
composition in the
typographic industry.
Readily customized
for all tape making
applications.



Write for Data.

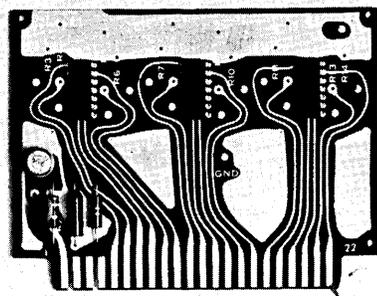
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CORPORATION

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Systems Incorporating
TAPE PUNCHES READERS AND HANDLERS
PHOTOELECTRIC KEYBOARD
I/O TYPEWRITERS AND PRINTERS

CIRCLE NO. 72 ON INQUIRY CARD

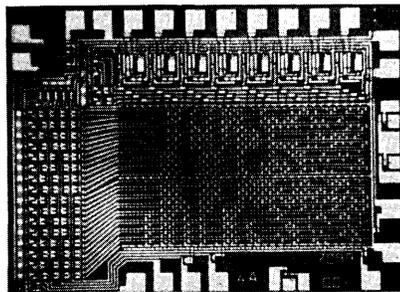
NEW PRODUCTS



MHTL INTEGRATED CIRCUIT LOGIC CARDS

Integrated circuit logic cards, series 400, utilizing MHTL (Motorola High Threshold Logic) packaging for highest noise immunity, will include complete voltage decoupling on each card through use of an emitter follower driven by a highly regulated power supply and provision for pull-up resistors directly on the printed circuit logic card. Higher noise immunity, typically 5.0 volts, is achieved with high threshold logic. Datascan, Clifton, N.Y.

Circle Number 231 on Inquiry Card.



MOS-LSI CHIP

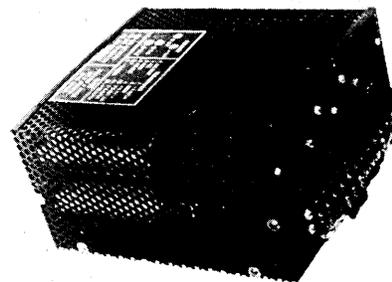
1,024-bit read-only permanent-memory MOS-LSI array, designated PM1024 is available as both a custom and a standard product. The chip contains 1340 MOS transistors, which provides an average packing density of about 180,000 MOS transistors per-square-inch with a peak packing density of well over 500,000 MOS transistors per square inch within the main memory portion.

The chip contains 60 logic gates with an average of about 22 MOS transistors per gate. Several gates contain as many as 133 MOS transistors. Due to the matrix approach

used throughout the chip, the interconnection problem is said to be much less severe than encountered on chips of considerably less complexity and device count.

The 1024-bit read only memory is organized into 128 eight-bit words and can be organized into 256 four-bit words. The memory pattern, specified by the customer, is "written" into the chip by using a specially programmed metal mask. Philco-Ford, Philadelphia, Pennsylvania.

Circle Number 204 on Inquiry Card.



MULTIPLE OUTPUT POWER SUPPLY

Low cost all silicon solid-state power supply with multiple outputs features switching regulators in two of the outputs resulting in high efficiency and an excellent size to output power ratio. Particularly designed for computer applications, the new supply also features output voltage protection, output voltage sequencing, and is short circuit proof. Power Systems, Venice, California.

Circle Number 206 on Inquiry Card.



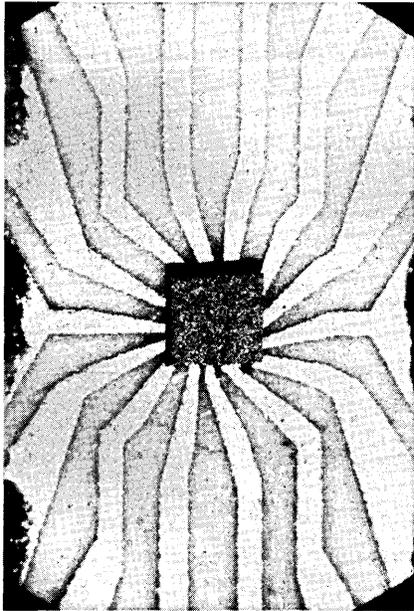
LOW-COST STORED PROGRAM CONTROLLER

Compact, high-speed, general-purpose store-program controller, designated the SPC-12 is designed for control, communication and data processing applications. The controller can function as a general-purpose computer or in the decentralized portion of a centralized-decentralized system.

The SPC-12 is all solid state, us-

ing silicon monolithic integrated circuits. It is a binary, parallel, single-address processor with 4,096 to 16,384 words (8-bit bytes) of core memory with a cycle time of 2.16 microseconds. The processor has ten programmable hardware registers. Four registers can function as accumulators, three as hardware index registers. The processor has an instruction repertoire which includes over 400 commands. Memory may be addressed directly or indirectly, indexed or not indexed. Indexing is possible before, after, or both before and after indirect addressing; and since indexing is performed by means of hardware index registers in the central processing unit (as opposed to pseudo-index registers stored in memory), no additional time is required for indexing. Automation Products, Orange, California.

Circle Number 208 on Inquiry Card.



TTL PACKAGE

Fairchild Semiconductor's line of TTL microcircuit products is now available in Fairpak®, the dual-in-line package which is claimed to improve IC reliability by means of a face-down bonded die. Of ceramic construction, Fairpak achieves a high-degree of hermeticity, and has excellent heat-transfer characteristics. The low profile package (0.125 inches) is less than half the weight of conventional plastic and epoxy DIPs, for which it is a plug-in replacement, pin for pin. Fairchild Semiconductor, Mountain View, California.

Circle Number 216 on Inquiry Card.

ZERO T.C.

S/N

SERIAL
MEMORY

20,000
BITS

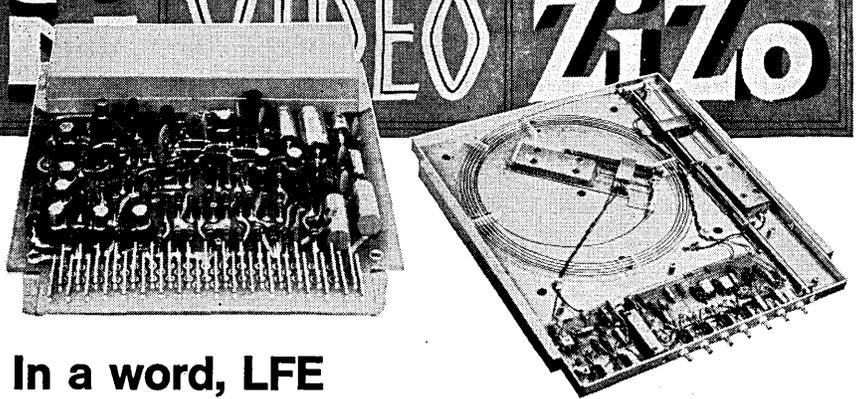
TORSIONAL DELAY

UNITY
GAIN

BI-POLAR

R
VIDEO

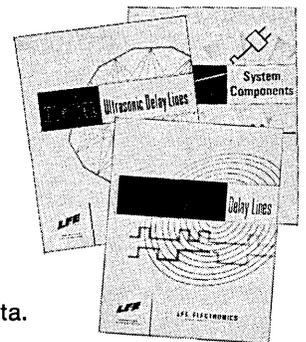
ZiZo



**In a word, LFE
for glass and magnetostrictive
delay lines for digital applications**

These are just a sampling of the performance features of LFE's glass and magnetostrictive delay lines. We can supply you with standard delay lines or serial memories with the capacity, bit rate, mode, delay and other parameters you need . . . or, you can specify custom delay lines, with or without associated electronics, to meet your special design requirements.

For the complete story write for technical data.



ELECTRONICS DIVISION

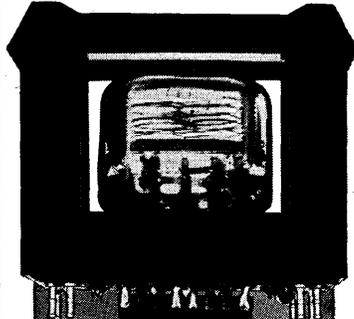
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WALTHAM, MASSACHUSETTS 02154
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CIRCLE NO. 73 ON INQUIRY CARD

New Shorter READOUTS

We also make indicators, switches, keyboards, panel displays, in-line displays and CRT displays.

Actual size



NEED THIS SPACE?

Specify TNR-70A Digital
Readout for I-C or
Discrete Circuitry

IT COSTS NO MORE!

Handles the job in $\frac{1}{3}$ the depth. How? With this monolithic silicon circuit. Complete decoder/driver package, with NIXIE[®] tube and bezel, is only $\frac{1}{8}$ " deep. Accepts 1-2-4-8 binary coded decimal inputs and produces 10 mutually exclusive outputs. Here's your answer where space is a critical factor. Prices as low as \$22.75 without tube in 100-299 quantities. Write for complete information.



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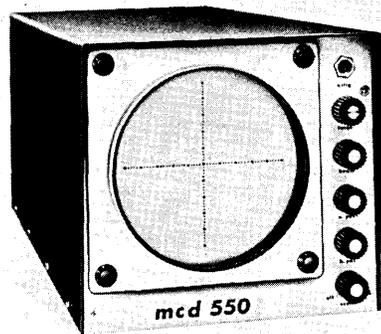
For complete information, contact your local TEC-Rep, or write direct.



INFORMATION DISPLAY AND CONTROL DEVICES
TRANSISTOR ELECTRONICS CORPORATION
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Minneapolis, Minnesota 55424
Phone (612) 941-1100

CIRCLE NO. 74 ON INQUIRY CARD

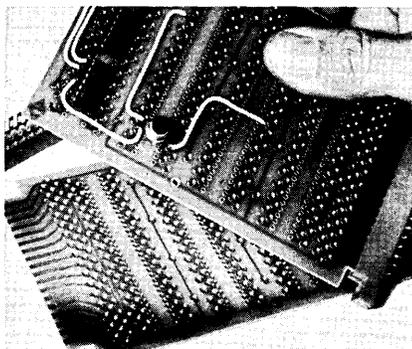
NEW PRODUCTS



X-Y MONITORS

Two solid-state X-Y Monitors have been developed for low-budgeted industrial applications requiring a small, easily-operated instrument capable of functioning in difficult environments and withstanding rough handling over a long period of time. Model 550 is rated at 20 foot lumens and requires only 50 VA (115/230 VAC), while the Model 560 is designed for where a brighter screen is needed and is rated at 80 foot lumens, utilizing a 100 VA power source. Measurement Control Devices, Philadelphia, Pa.

Circle Number 245 on Inquiry Card.



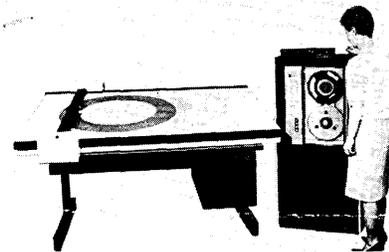
IC PROTOBOARDS

Series 2000 universal circuit board mounts any of the standard D.I.P. or T05 integrated circuits, and has a card-edge connector with one or two-sided capability, with 18 to 44 contacts. The boards feature spring-loaded grip-type terminations. Two sizes are provided: 0.050" diameter for IC leads or pins, an 0.070" diameter for circuit wiring and other component leads.

Rows of IC terminals are pro-

vided, each double row containing up to 78 terminals for the IC's; each IC terminal is matched by a wiring terminal connected with a printed circuit path. Gridcraft, Inc., Fort Wayne, Indiana.

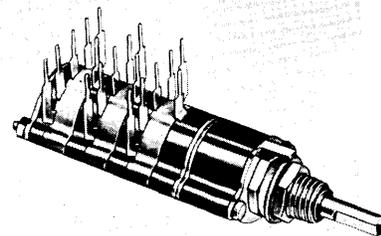
Circle Number 242 on Inquiry Card.



DELTA PLOTTER

Low-cost, high-speed, all digital delta plotter capable of straight line drawing at .001" increments with replaceable printed circuit boards and all-solid-state circuitry utilizing silicon integrated circuits operates either as an off-line system with input from punch cards, paper tape, or magnetic tape, or as an on-line system at speeds up to ten inches-per-second. Each coordinate with its sign is displayed in five digit configuration, along with the operation being performed and the internal function position of the program director, on the front panel. Auto-trol, Arvada, Colorado.

Circle Number 237 on Inquiry Card.



PC ROTARY SWITCH

Printed circuit mounting of a rotary switch is said to be accomplished easily and efficiently with a new style of rotary switch. The terminal design permits insertion directly into a printed circuit board. Conventional wave soldering techniques can then be used to complete the circuitry. Gold plated printed circuit terminals facilitate soldering. The switch will make and break the following loads: $\frac{1}{4}$ amp., 115 VAC resistive; $\frac{1}{4}$ amp., 6 to 28 VDC; 50 ma., 115 VAC in-

ductive; 20 ma., 28 VDC inductive; or carry 4 amps. continuously. Initially insulation resistance is 50,000 megohms and voltage breakdown is 1,000 VAC. Life expectancy is about 100,000 cycles of operation, depending on conditions. Grayhill, Inc., La Grange, Illinois.

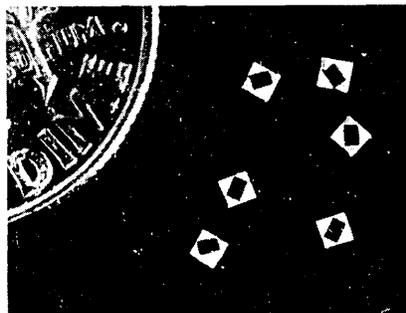
Circle Number 244 on Inquiry Card.

HIGH RESOLUTION TRIMMERS

High resolution trimmers packaged in RT11 and RT12 type packages with pins or leads are available in standard resistance values between 10 ohms and 50K ohms; and in semi-standard resistance values between 75K ohms and 175K ohms.

The producer claims advanced construction techniques and the use of a longer element give higher resolution for given wire size and type. With fewer parts, fewer electrical connections, these trimmers are said to feature longer life with less noise and better performance under extreme environmental conditions. All units automatically undergo dynamic and static tests which exceed MIL-R-27208B Group A inspection levels. Fairchild Controls, Hicksville, N.Y.

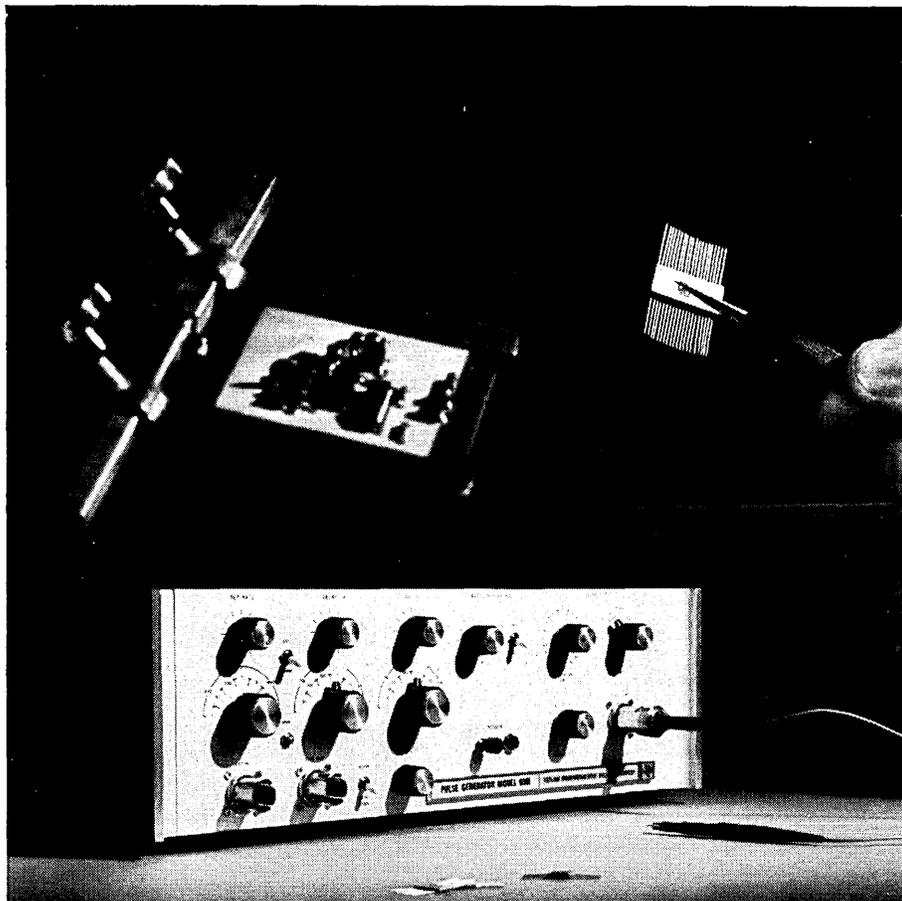
Circle Number 236 on Inquiry Card.



THICK FILM RESISTOR CHIP

Thick film resistor, Style GC-50, is designed to replace silicon chip resistors in the production of integrated circuits and hybrids. Physical dimensions of the resistor are 0.050" x 0.050" x 0.010", with a resistance range from 50 ohms to 100K. Wattage rating is 0.050 watts at 125 deg. C. Temperature coefficient of the GS-50 resistor chip is 200 ppm/degree C, from -65 C to +150 C. Mepco, Inc., Morristown, N.J.

Circle Number 243 on Inquiry Card.



Why You Need a Special Pulse Generator for State of the Art Circuit Design

With high speeds and critical design parameters, you need the best test instruments to be sure your designs will be optimum. The TI Model 6901 Pulse Generator gives outputs from 1 KHz to 0.1 GHz; independent amplitude and baseline controls; jitter less than 0.1% of period + 50 psec; and count-down synchronization output.

The 6901 makes your designing simpler, too. Because the pulse amplitude of the generator can be changed without affecting DC offset, you can use the offset instead of an external bias supply for your circuit.

For additional information, contact your TI Field Office, or the Industrial Products Division, Texas Instruments Incorporated, P. O. Box 66027, Houston, Texas 77006.

TEXAS INSTRUMENTS

INCORPORATED

CIRCLE NO. 75 ON INQUIRY CARD

827A



With so many extras, we couldn't call our Minuteman Static Inverter anything but an Extravert. It's the best you can buy for critical applications such as computers and process instrument AC interruptible power.

- The extras:
- Extra reliability
 - Extra protection
 - Extra overload capacity
 - Extra KVA at low PF
 - Extra power quality
 - Extra-low harmonics
 - Extra-high efficiency
 - Extra-easy maintenance
 - Extra-experience
 - Extra-ordinary service

Available 1KVA to 100-plus KVA.

If you're an introvert, write for more information about this remarkable product.

If you're an extrovert, phone.



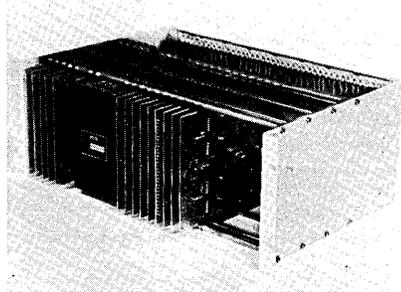
Think initially of TRW

TRW Equipment Group
Telephone (216) 383-3435
Dept. 0855, 23555 Euclid Ave.
Cleveland, Ohio 44117

TRW

CIRCLE NO. 76 ON INQUIRY CARD

NEW PRODUCTS



1.5 μ s IC MEMORY

The random access Model CE-150 has full cycle time of 1.5 μ sec, an access time of 750 nanoseconds, and is available in capacities of 4096, 8192 and 16,384 words with word lengths variable in 4 bit increments from 8 to 36 bits. The system is designed for applications as a memory in small computers or as a buffer in data systems where memory speeds faster than 1.5 μ sec are not required. Lockheed Electronics, Los Angeles, California.

Circle Number 247 on Inquiry Card.

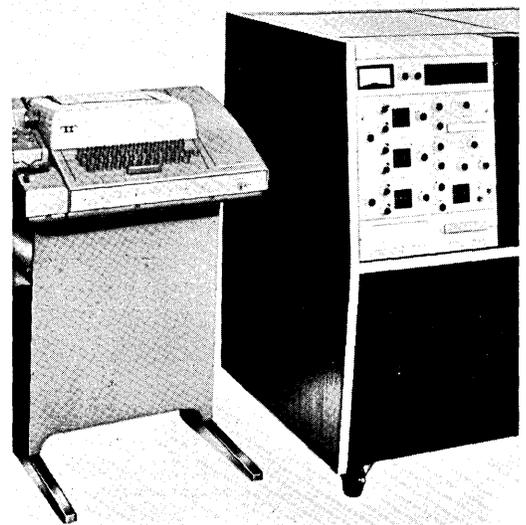


MULTIPLE-STATION PUSHBUTTON SWITCH

The series 6500, DW Multi-Switch switch is available in configurations of up to 18 stations in a single row, depending on switch functions. Maximum switching per station is 2-C (DPDT). Each station on the DW switch utilizes specially designed switching modules that consist of a switch housing, push-button actuator, terminal board assembly and switching contractors.

Series 65000 switches are said to be designed to meet the performance requirements of sophisticated equipment such as; analog and digital computers, analyzers, transmitters and receivers, intercoms, numerical control, ground support systems, scientific instruments, or any other control panel application where cost and reliability are prime engineering parameters. Switchcraft, Chicago, Illinois.

Circle Number 239 on Inquiry Card.



COMPUTERIZED SPECTROMETER

Two-hundred-sample automatic liquid scintillation spectrometer, with pre-programmed data reduction capabilities, using a built-in digital computer. Designated model SL-40, the system provides direct on-line readout of the disintegration rates (dpm) in variably quenched single or dual-isotope samples. Sample activity is computed either through the channels' ratio method or the external standard ratio method, at the operator's option. An alternate operating mode allows variably quenched carbon-14 and more energetic isotopes to be counted at constant efficiency. Intertechnique Instruments, Dover, New Jersey.

Circle Number 241 on Inquiry Card.



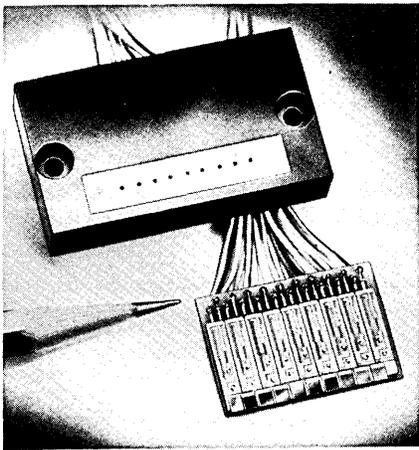
TAPEMAKER-PRINTER SYSTEMS

Series TMP-200 tapemaker-printer system for on-line and off-line applications includes an I/O typewriter, tape punch, and tape reader (each with handler), plus a complete set of electronic controls for

the specific functions requested by the customer. The system utilizes any to 8 level data code and can be interfaced with telephone transmission equipment and computers.

Typical applications include check-out systems, code conversion, computer input-output, programming, communications reception and transmission, data handling or logging, data processing, digital recording, numerical machine control, off-line data preparation, tape duplication, and X-Y co-ordinate plotting. Data speeds may range from zero to 125 characters per second or higher. Invac Corp., Waltham, Mass.

Circle Number 248 on Inquiry Card.

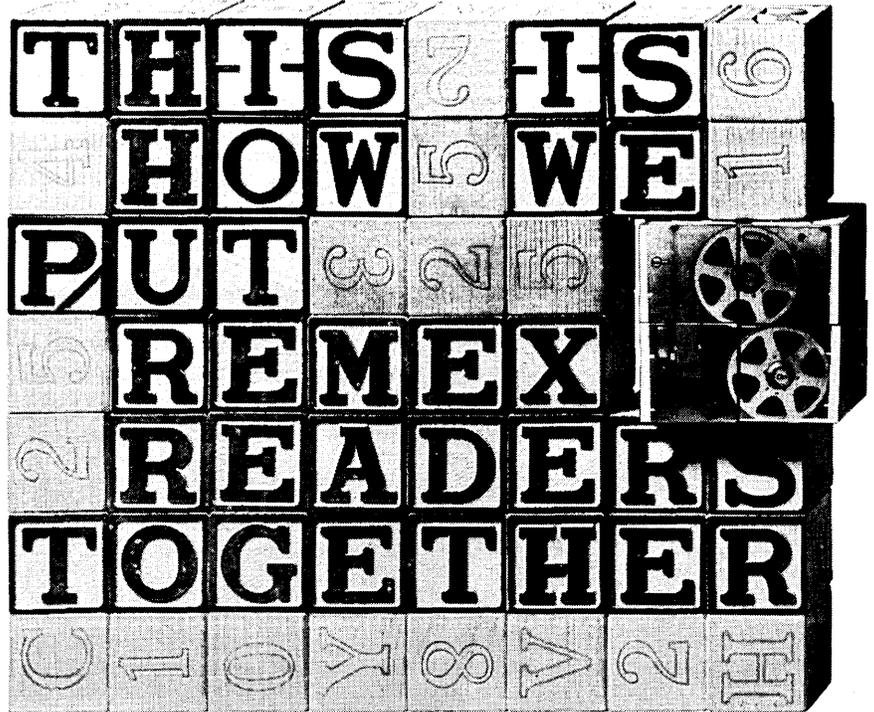


PHOTOVOLTAIC/THIN FILM HYBRID READOUT

Miniaturized photovoltaic/thin film hybrid readout assemblies, designed with initial amplifiers configured to interface directly with standard DTL or TTL logic elements and standard housings for use in 8-level tape readers as well as 12-level card readers, are said to be the first to offer the system designer a new and heretofore unavailable capability in the area of light sensitive arrays, combining the concept of common substrate construction of light sensitive devices with all associated amplification circuitry.

A typical readout assembly, consisting of 12 individual 2 channel amplifiers, is packaged in a housing only 3.5" long, 1.2" wide by 0.38" thick. Voltages compatible with computer logic levels are available with field effect transistors and standard silicon transistors, as required by light conditions. Sensor Technology, Van Nuys, Calif.

Circle Number 240 on Inquiry Card.



Whether you ask for a standard reader or a specially designed system, we go at it in the same tried-and-true way, with the same basic components. "Building block" construction makes our readers rugged and reliable.

So do the photocells and the solid state circuits. Manufacturers of numerically controlled systems, automatic test machinery and computers

have told us that Remex equipment performs far better than anybody else's. Which may explain why we sell more readers, year in, year out. See for yourself. Call us at

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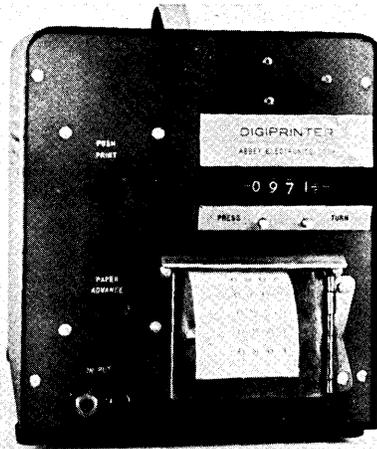
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CIRCLE NO. 92 ON INQUIRY CARD

NEW PRODUCTS



DIGITAL RECORDING VOLTMETER

The digital recording voltmeter is said to cost less than half the price of existing digital recording voltmeters. The new instrument can be furnished in portable or panel mounted configurations.

The device is a self-contained unit that provides a continuous digital readout and a printout on command on 2 1/4 inch adding machine tape. The standard model has a range of 100 millivolts for a full scale count of 1000. Over-ranging is 10%. Other single and multi-ranges can be furnished.

Accuracy is $\pm 0.1\%$ f.s. ± 1 count. Resolution is 0.05%. Input impedance is 1 megohm off null, virtually infinite at null. Slewing speed is 8 seconds, printing speed 2 seconds. Abbey Electronics, Westbury, New York.

Circle Number 238 on Inquiry Card.

1/20 WATT PRECISION RESISTOR

A molded precision metal film resistor, 0.050" diameter by 0.130" long, featuring end cap construction, is now available for use in miniature circuit assemblies. Type MRE-1/20 resistor conforms to all the applicable requirements of RN45 (proposed) of MIL-R-10509F and offers tolerances to $\pm 0.1\%$ and temperature coefficients as low as 0 ± 25 ppm/ $^{\circ}$ C. American Components, Conshohocken, Pennsylvania.

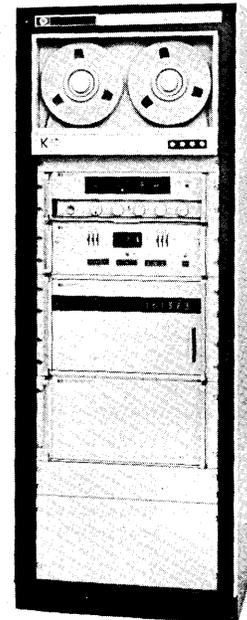
Circle Number 200 on Inquiry Card.

DUAL BINARY CIRCUITS

Seven new dual binary circuits have been added to Signetics' Designer's-Choice Logic (DCL) series. Three of the circuits feature 70 MHz toggle rates.

All seven binaries offer both synchronous and asynchronous capabilities. All DCL elements are available in two temperature ranges: -55 degrees C to $+125$ degrees C and 0 degrees C to $+70$ degrees C and in three packages: 14-lead flat and DIP and the new B-package, a 16-lead silicone DIP. Signetics, Sunnyvale, California.

Circle Number 209 on Inquiry Card.



NOISE-IMMUNE DATA ACQUISITION SYSTEMS

Data acquisition systems series is said to combine higher speed and better resolution with excellent noise immunity at a reasonable price. Over fourteen channels per second can be scanned and recorded with 5-digit resolution plus sixth-digit overrange and with 152 dB suppression of 60-Hz common mode interference.

Although the maximum recording rate is achieved on magnetic tape, other versions of the systems record data with commensurate speed on either punched or printed tape, punched cards, or typewritten pages (8 channels/sec on printed tape, 10 characters/sec on typewriter, 16 characters/sec on punched cards, 120 characters/sec on punched tape). Hewlett Packard, Palo Alto, Calif.

Circle Number 246 on Inquiry Card.

INCREASE COMPUTER THROUGHPUT

Brochure describes the COPE 0.45 (Communications Oriented Processing Equipment) remote-data communications terminal system consisting of a remote controller, operator's console, teletypewriter, high-speed printer (1250 lpm), card reader (1500 cpm) and communications line interface. Features include full duplex communications (both directions concurrently), self-sufficient operating system software, a basic cycle time of 1.5 μ sec. per word, plus the extra speed provided by unique cycle-steal-interrupt capabilities.

Compared with any other terminal using voice-grade lines, the COPE is said to be 3-to-6 times faster, with up to 12 times more efficiency of throughput. The terminal is claimed to be especially designed for heavy production loads typical of large-scale FORTRAN and COBOL users, with dramatic economies in communications/modem costs, operator hours, and overall installation requirements. Computer Industries, Dallas, Texas.

Circle Number 331 on Inquiry Card.

THUMBWHEEL SWITCHES

The evolution, design, construction, and broadly varied applications of thumbwheel switches are described in a new, illustrated 10-page brochure by The Digitran Company, Pasadena, Calif.

Titled "An Introduction to Thumbwheel Switches", the brochure provides a brief history of thumbwheel switch technology, and describes the construction of a typical Digiswitch.

Two pages are devoted to the broad range of commercial, industrial, military, and aerospace applications of thumbwheel switches, among which are instruments for timing and measuring; test or checkout equipment; process control, computer control and data handling equipment.

In its final section, the brochure provides a ready-reference review of key features and operating characteristics of the company's switch line, including a special quick-check tabular chart comparing features and options available in the various Digiswitch/Miniswitch series. Digitran Company, Pasadena, Calif.

Circle Number 330 on Inquiry Card.



Have you noticed which disc memories your competitors use now?

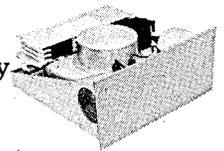
Five computer manufacturers and six data systems builders have adopted Data Disc memories as a standard rapid-access peripheral storage.

They've discovered that Data Disc memories cost about 35% less than any other head-per-track disc memory of equal storage capacity. Complete machines, including electronics, sell for 1/10¢ per bit in quantities of ten.

Perhaps you wonder how a top-quality machine can cost so little. Well, cost per disc, per track, per head or per drive is no less than any other reliable memory. But cost per bit stored is far less—simply because our "in-contact" recording technique stores twice as many bits per inch as older "floating head" techniques.

"In-contact" recording—in which heads ride in gentle contact with a highly polished disc—is five years old now. It has proven its long-

term reliability in hundreds of Data Disc memories now operating across the nation. We guarantee an error rate less than 1 part in 10^{10} , and tests by our customers show typical error rates 1000 times better.



An F-Series head-per-track system

Our F-Series head-per-track system comes with storage capacities of 0.8, 1.6, 3.2 and 6.4 million bits. It has an average access time of 16.7 ms, and stores 100,000 bits on each track—enough to fill the core memory of a small computer. And the whole system fits in 8 $\frac{3}{4}$ " of rack space.

For complete information contact Data Disc, Inc., 1275 California Avenue, Palo Alto, California 94304, Phone (415) 326-7602.



DATA DISC

CIRCLE NO. 78 ON INQUIRY CARD



Micro Zener Diodes

Data sheets on the full CODI line of micro zener diodes include full performance and mechanical specifications on 120 devices. The sheets include information on the following lines: The MLV Series micro low voltage Zener diodes which can replace JAN types IN 4370A through IN 4373A; the MGLA Series micro general purpose low voltage avalanche diodes for use at 2.8 to 10.0 volts; the MLLA Series micro low leakage low voltage avalanche diodes for use at 2.8 to 10.0 volts; the MHLA Series micro high temperature low voltage avalanche diodes for use at 2.8 to 10.0 volts; and the MTC Series micro temperature compensated Zener diodes which can replace

JAN types IN 821 through IN 827A and IN 935 through IN 946B. Computer Diode, Fair Lawn, New Jersey.

Circle Number 300 on Inquiry Card.

Guaranteed IC Performance

Series Se/NE8000 designer's-choice-logic integrated circuits feature guaranteed performance limits covering worst-case d-c noise margins, worst-case a-c and d-c loading, minimum-maximum propagation delay limits, power consumption-per-gate limits and absolute maximum ratings. The Series 8000 DCL integrated circuits include high-speed TTL circuits, slower TTL circuits with low power and good a-c noise immunity, low power DTL circuits with high d-c noise margins and

functional arrays for counting and storage applications.

Complete information is given in Bulletin No. 25700A, which contains schematic diagrams for each series, plus complete electrical characteristics in tabular form for easy interpretation. Performance curves are supplied in the areas of pair delay, turn-on and turn-off delays, clocked more switching and holding levels and toggle rates. Sprague Electric, North Adams, Massachusetts.

Circle Number 301 on Inquiry Card.

Hardware Capabilities

Twelve-page illustrated quick-reference catalog provides a complete review of the producer's computer peripheral hardware product line. A briefer catalog, four pages, is also available, as well as new technical data sheets that give performance specifications for particular items of equipment. Computer-related devices, including strip-chart, film, and large-area digitizing systems, incremental plotting systems, high-speed high-accuracy drafting systems, flatbed D/A plotting systems, and cathode ray tube microfilm printers and plotters are described. The new brochures present an overall view of the company's hardware capabilities and the individual data sheets are available for a requirement of more detailed information. Computer Industries, Van Nuys, California.

Circle Number 302 on Inquiry Card.

Long Life Push-Button Switch

Six-page two color folder offers specifications on momentary and push-pull switches for military and commercial application. Standard and moistureproof switch lines are shown with dimensional drawings for standard mounting adapters. Electrical, mechanical, and material specifications for these 10-ampere (115 vac or 28 vdc) switches with a 250,000-cycle mechanical life rat-

amnesia (am nē'zhə or am nē'zhiə)
loss of memory due to a 10% voltage swing. *n.*

Raytheon Computer's 300 memory keeps right on reading and writing data reliably even when operating voltage and drive currents vary as much as $\pm 10\%$. And over a full temperature range of 0°C to 50°C. The 300 is a 2½D 900 nano-second core memory for general data systems use. ■ If your definition of memory is: high performance, high reliability, high capacity, and delivery in 60-90 days, see us. Raytheon Computer, 2700 So. Fairview St., Santa Ana, Calif. 92704. (714) 546-7160.



CIRCLE NO. 79 ON INQUIRY CARD

ing include available contact arrangements, button colors and sizes, seven types of mounting adapters, and a table for converting MIL Standard push-button switch specification number to the manufacturer's equivalents. Nexus, Stamford, Connecticut.

Circle Number 303 on Inquiry Card.

Sub-min Connectors

Illustrated 12-page catalog describes a wide range of sub-miniature "established-reliability" electronic and electrical connectors designed for a wide spectrum of applications in the fields of oceanography, aerospace, computers and industrial electronics. Included in catalog SMI-B are special hermetic types, particularly suited for high-humidity environments. Bathtub-type protective shells are available for most of the units described, in draw-pull and screwlock versions. U.S. Components, Bronx, New York.

Circle Number 304 on Inquiry Card.

DC Power Supplies

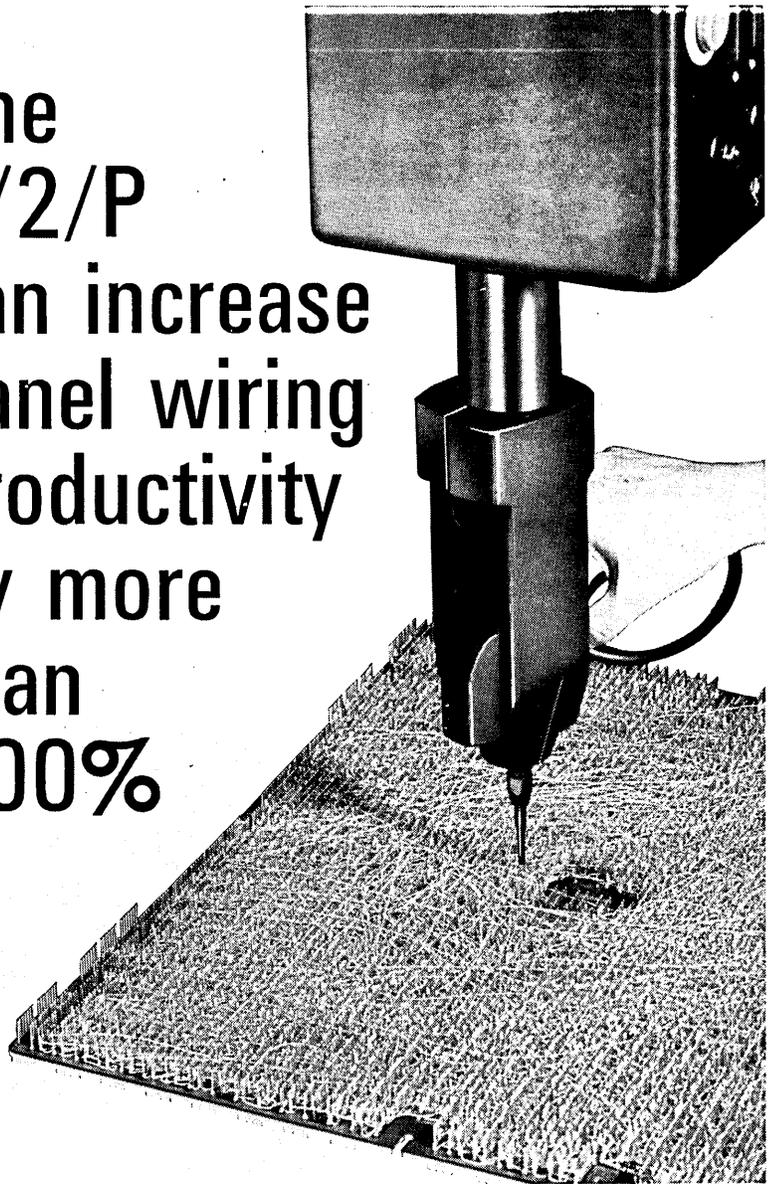
Short-form catalog (68A) covering DC power supplies and AC line regulators includes information on the manufacturers' newer power supplies such as the QRD Series, which are high-speed programmable units suitable for automated testing of integrated circuits, and AEC nuclear instrument module power supplies. A line of high voltage DC supplies is also listed. AC line regulators in the catalog include a series with silicon controlled rectifiers and a series using magnetic amplifiers. A series of frequency changers is listed, as is a line of neon lamp supplies. Raytheon Company, Sorensen Operation, Norwalk, Connecticut.

Circle Number 305 on Inquiry Card.

Flat-Ribbon Cable

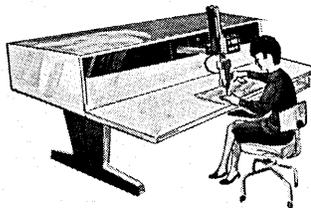
Twelve-page capabilities brochure and short-form product catalog describes flat-ribbon cable and related products. The new bulletin discusses the manufacturer's approach to flat-ribbon cable made with round conductors, touching on its advantages and briefly mentioning stripping, terminating, connectors and other wiring and cable handling procedures. Spectra-Strip Cor-

The
P/2/P
can increase
panel wiring
productivity
by more
than
500%



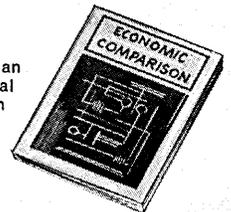
The P/2/P Wiring System combines numerical control, automatic indexing, and a human operator to form a highly efficient production facility for wire wrap or clip on termination wiring.

It provides the advantages of total automation (automatic travel and positioning of the tool) while eliminating the problems of hand wiring (slow production rates and human errors). The result—flawless panel assembly at less than $\frac{1}{3}$ the hand wrap cost, and at $\frac{1}{8}$ the initial investment required for a fully automatic system.



Write, wire, or call to arrange for a demonstration of the P/2/P Wiring System, and see these benefits for yourself.

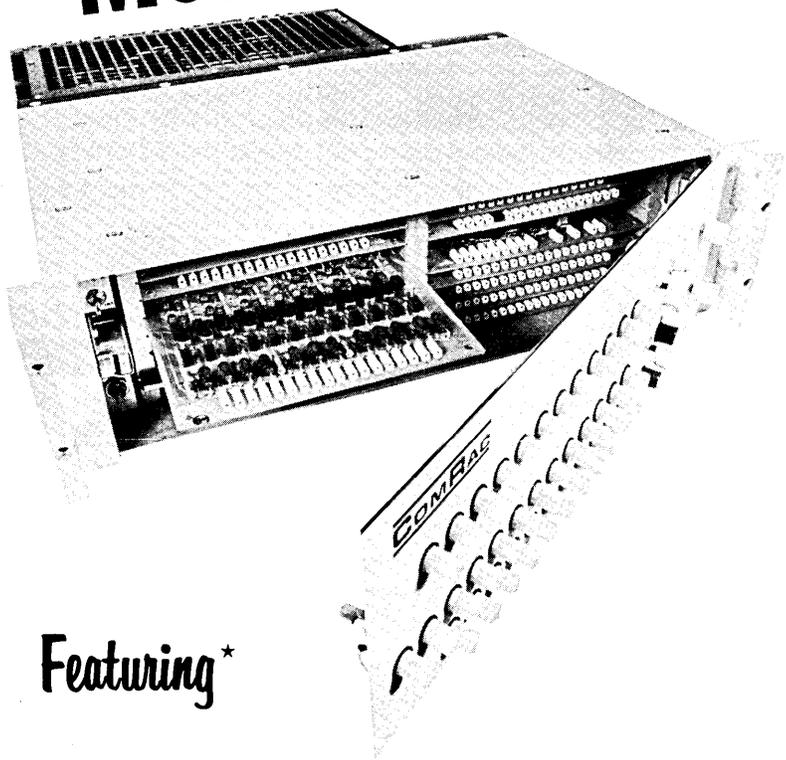
"Economic Comparison", an objective survey of several wiring methods now in use, is yours on request.



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- ★ 5¼" Rack-Mounted Chassis Including Power Supply
- ★ DTL And TTL Compatible Interface
- ★ Operating Modes: Read/Restore, Clear/Write, Buffer Read, Buffer Write, Read/Modify/Write
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poration, Garden Grove, California.
Circle Number 306 on Inquiry Card.

Thick-Film Hybrids

Twelve-page illustrated brochure describes the maker's thick-film hybrid microcircuits for high-reliability applications and offers hybrid circuits to users without in-house capability. The booklet shows step-by-step how the circuits are made and points out advantages at each stage. Starting with an alumina substrate, a typical circuit is taken through the manufacturing process. Photographs illustrate how the company's production techniques help to assure accurate, high-density circuits. The brochure lists standard circuits available off-the-shelf. Custom circuits are also offered. Tele-Dynamics, Philadelphia, Pennsylvania.

Circle Number 307 on Inquiry Card.

Servicing Digital Computers

More and more digital devices are being used in business and industry, opening a new servicing field for the enterprising electronics serviceman. Although factory representatives generally service the large computers, there are many digital computers and devices that a competent serviceman can service.

"Servicing Digital Devices," by Jim Kyle, teaches the reader how to troubleshoot computers and associated digital equipment. The book tells what test equipment is needed, explains the basic principles of logic and switching circuits, and gives a brief survey of the types of digital equipment the serviceman is likely to encounter. Logic symbols, counters, registers, adders, and comparators are explained. Price \$3.25. Howard Sams & Company, Indianapolis, Indiana.

Circle Number 308 on Inquiry Card.

Double-Density D Connectors

Four-page catalog describes contact arrangements, electrical data, accessories, and assembly instructions for double density D rectangular connectors. Packaged in the popular D subminiature shell configuration, the connectors provide double the contact density in the same insert area. In addition to high-density and reliability, these connectors are

said to be lower in cost-per-contact than most comparable lines. They are available in the same five shell sizes as D subminiature connectors but since contacts are on 0.075" centers, can accommodate arrangements of 19, 31, 52, 79 or 100 contacts. Contacts are crimp snap in and are rated at 5 amps each. ITT Cannon Electric, Los Angeles, California.

Circle Number 309 on Inquiry Card.

Relay Catalog

Complete specifications, technical reference data, and ordering information are presented in a 4-page catalog bulletin on Sigma series 4 SPDT relays. A sensitive, multi-purpose DC relay, the series 4 responds to either 20 or 50 milliwatt signals, switches 0.1 to 2.5 amperes at 28 VDC/120 VAC resistive one hundred thousand to one million times depending on contact material and load, and has a mechanical life of eight million operations minimum. Over five hundred individual relay types may be selected among the adjustments, coil resistances, contact materials, and physical types cataloged. Sigma Instruments, Braintree, Massachusetts.

Circle Number 310 on Inquiry Card.

Product Line Brochure

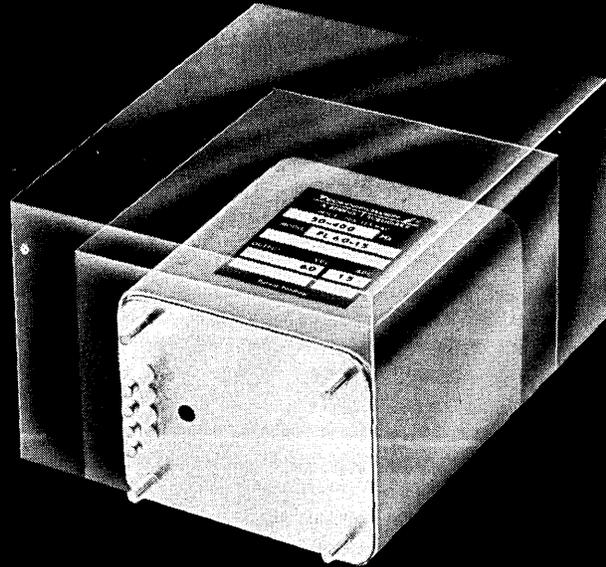
Six-page brochure illustrates and discusses 53 product types offered by the manufacturer. General classifications include mechanical and electro-mechanical products; timing and programming devices; electronic displays and counters; servo packages, assemblies and subsystems; precision measurement instruments; and in-line control modules. Representative products are pictured in these and related categories, along with a range of the operating parameters available. A number of entirely new products include "Logicator" and "Opticator" displays designed for operation from digital computers. Bowmar Instrument Corporation, Fort Wayne, Indiana.

Circle Number 311 on Inquiry Card.

Electronic Measuring Apparatus

A family of measuring apparatus is described in a 50-page illustrated catalog encompassing a broad

smaller-than-ever power modules!



Of particular interest for up-to-the-minute computer and systems applications, Technipower's 1968 lines feature modules up to one half the size of standard competitive equivalents, as a result of unique design concepts. Three new series of ultra-compact, highly efficient modules are available now!

PL-80 Series — Regulated AC-DC Supplies

3.0 to 152 VDC, to 75 watts — Temperature rating 80°C
432 models, featuring 0.05% line and load regulation, 0.002% ripple, up to 20% output adjustment range. Designed to meet MIL environmental specifications.

HF-80 Series — Regulated AC-DC Supplies

2.8 to 1000 VDC, to 375 watts — Temperature rating 80°C
75 models (including models capable of 5 volts @ 50 amperes output), regulation, by high frequency transformation methods, $\pm(0.05\% + 5 \text{ mv})$ line, $\pm(0.10\% + 10 \text{ mv})$ load, 2:1 output adjustment range, series operation permissible. Incorporated EMI suppression components designed to meet MIL-I-6181D.

CD-95 Series — Regulated DC-DC Converters

2.8 to 1000 VDC, to 250 watts — Temperature rating 95°C
84 true converter models, full isolation between input and output for local regulated DC power. Regulation $\pm(0.05\% + 5 \text{ mv})$ line, $\pm(0.10\% + 10 \text{ mv})$ load, ripple 0.2% + 10 mv, 2:1 output adjustment range, series operation permissible. Incorporated EMI suppression components designed to meet MIL-I-6181D. Fully encapsulated, meets MIL environmental requirements.

Write for fully descriptive literature, which includes installation data and prices.



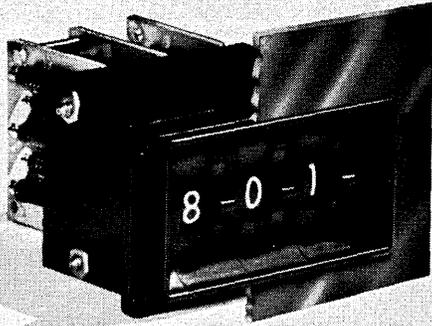
TECHNIPOWER

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CIRCLE NO. 82 ON INQUIRY CARD



precise potentiometer

Dial the exact voltage or resistance setting you need. With Digidecades and Digividiers it takes less time than you needed to read this sentence. If you want to repeat a previous setting, it's yours. For example: an error-free change from 10 ohms to 910 ohms is made with one flick of a finger rather than cranking a knob 360° several times. High reliability combines with low contact resistance thanks to redundant, non-oxidizing contacts. And contact resistance is very stable.

Digidecade resistance decades provide your choice of one, two, or three

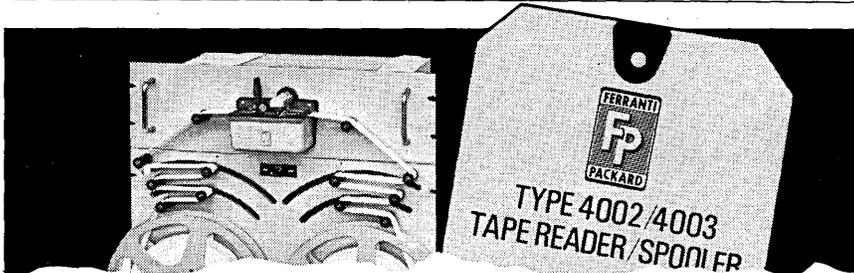
decades per unit. More can be ganged together, with accuracy at 25°C of 1±% of setting, or better.

Digivider voltage dividers, with your choice of Kelvin-Varley or Poggendorf circuits, are available in a wide range of input impedances, and are accurate to 1% of full scale.

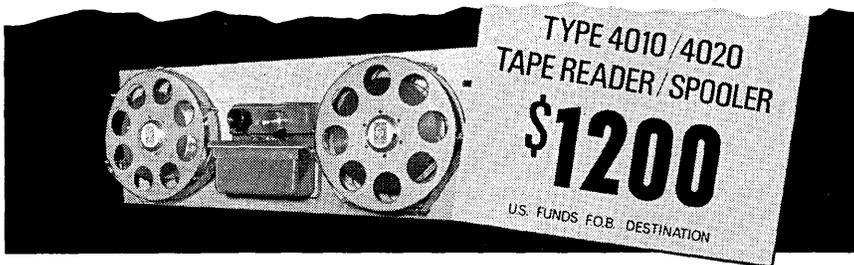
For precise pot data, write Digitran.

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Subsidiary of Becton, Dickinson and Company [BD]
855 S. Arroyo Pkwy./Pasadena, Cal. 91105
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CIRCLE NO. 83 ON INQUIRY CARD



We've taken our 1000 C.P.S. Paper Tape Reader/Spooler, slowed it down to 300 C.P.S., halved the price...



...and come up with a dependable unit that can't be matched in terms of quality, economy and delivery.

Medium speed range — up to 300 characters/second — photoelectric sensing — stops on character at 300 characters/second — bidirectional — silicon logic — tried and tested design concept and components — off the shelf delivery from mid 1968 — low unit price of \$1,200.00. For complete details, write, wire or phone.



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6712

CIRCLE NO. 84 ON INQUIRY CARD

range of oscilloscopes, multimeters, pulse generators, transistor curve tracers, low frequency measuring systems, and instrumentation recorders. Combining solid-state circuitry with the latest advancements plus many exclusive features, this new generation of equipment is said to be designed to provide greatly increased reliability and performance. The catalog is divided into three major product sections. The first section is devoted to the manufacturers' oscilloscope series. The second discusses electronic multimeters. The third covers a family of signal sources which are claimed to provide the newest and most unique low frequency generating measurement systems on the market. Philips Electronic Instruments, Mount Vernon, N.Y.

Circle Number 312 on Inquiry Card.

Magnetic Disk Pack Brochure

Technical folder detailing the characteristics of CM VI (Caelus Memories, six-high) magnetic disk pack is now available. The CM VI is said to be designed and guaranteed to function with IBM 360 and compatible equipment. The folder contains manufacturing, testing and application data along with product specifications. Caelus Memories, San Jose, California.

Circle Number 313 on Inquiry Card.

Conductive Tapes

Electrically conductive tapes are described in an 8-page, four-color brochure listing properties and application data on Scotch brand conductive tapes No. X-1170 and No. X-1181. No. X-1170 is an aluminum foil backed tape with an electrically conductive adhesive. No. X-1181 is a copper foil backed tape, also with an electrically conductive adhesive. Both tapes are designed for EMI/RFI shielding applications. 3M Company, St. Paul, Minnesota.

Circle Number 314 on Inquiry Card.

50 MHz Pulse Generator

110B Pulse Generator featuring 50 MHz rep rates, 4.0 ns linear rise, ± 10V output, 12V baseline adjustment and both synchronous and asynchronous gating is described in Technical Bulletin 110B. Waveform photos are used to illustrate

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SJCC Interviews:
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DEVELOPMENT ENGINEER (CUSTOM MODULAR PRODUCTS) — will have full project responsibility for special, non-catalog digital logic modules. Will involve proposal support, circuit development, product documentation, and fabrication support as well as circuit and product design and interdepartmental liaison activities. 1-5 years experience in circuit design necessary.

DEVELOPMENT ENGINEER (DIGITAL LOGIC MODULES) — to perform product design tasks under supervision of project engineer, with project responsibility on new product development. Will participate heavily in the design and development of complex logic function packages. Should have 1-5 years experience in circuit design with solid understanding of high-speed switching circuits, I/C's and logic functions.

ANALOG DESIGN ENGINEER (SENIOR) — to define requirements for design of high-precision analog circuits, modules and subsystem devices. Previous experience in A-D and D-A device design and in precision current switches and operation amplifiers required.

COMPUTER LOGIC DESIGN ENGINEER — to design computer or related logic systems and contribute to department projects. Will make recommendations for new development projects based on detailed technical analysis, maintain good working knowledge of small computer technology, and aid in general project administration. Reports to department manager, small com-

puter development. 3-6 years experience including central processor logic design.

COMPUTER DESIGN ENGINEER — Challenging opportunities for development engineers who exhibit creative ability in the conception, design and development of new computer hardware to join the team that's responsible for advanced high-speed computer systems design. Requires digital logic design and central processor design experience.

COMPUTER-BASED SYSTEMS ENGINEERS — several challenging opportunities are available for engineers with a background in digital computers and systems. Areas of activity include: display, hardware and software, communication systems, data acquisition control, data reduction, message switching, data concentration, and management information. Levels of involvement range from staff engineers to project management. 3-5 years applicable experience.

For more information about these and other key professional opportunities in our engineering area, call Mr. J. Paul Costello (617) 879-2600. Or, send resume in confidence, with salary information, to Honeywell, Computer Control Division, Old Connecticut Path, Framingham, Massachusetts 01701.

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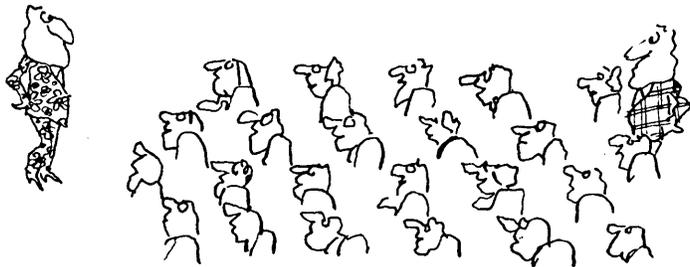
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CIRCLE NO. 905 ON INQUIRY CARD.

capabilities and usefulness of unit. Other photos show detail of interior and front panel. Complete specifications are provided. Available from Datapulse, Inc., Culver City, California.

Circle Number 315 on Inquiry Card.

Submin Capacitors

Twelve-page catalog describes complete line of subminiature ceramic capacitors in a wide choice of values, lead arrangements, lead material, physical and electrical properties. Republic Electronics, Paterson, N.J.

Circle Number 316 on Inquiry Card.

Solid-State X-Y Monitors

Two-page bulletin describes and illustrates two new T-R X-Y monitors developed for use in industrial applications where adverse environments and less-than-careful handling is to be expected. The bulletin explains how the Model 550 and the Model 560 were designed to fill current requirements for compact, low-cost X-Y monitors which are both simple to operate and have the built-in reliability to function properly day-in and day-out under production line conditions.

Both monitors feature complete solid-state construction (except CRT), a 4½" usable screen display, plug-in P.C. boards, identical DC amplifiers and rear-input connectors. Both are operable over a temperature range from 40° to 131°F. Measurement Control Devices, Philadelphia, Pa.

Circle Number 317 on Inquiry Card.

Solid-State AC Regulators

Four-page catalog describes a recently introduced line of solid-state AC regulators. The units described are compact, modular, fast acting sinusoidal designs which are said to be independent of input frequency and regulate against line AC variations as well as eliminating AC transients. The catalog describes model types, provides mechanical and operating data, circuit descriptions and prices. Electronic Research Associates, Cedar Grove, New Jersey.

Circle Number 318 on Inquiry Card.

Were you the one who set up a radio station to blanket the block with Little League propaganda?



Maybe you were the fellow they spotted pulling a wagon-load of electronic gear. Maybe they even kidded you about being the block's mad scientist. But you had your way. With a couple of 12AX7's, a 6L6 and a 12AT7, you blanketed the block on 1405 kc with scores, schedules and appeals for funds. And before long, you were something of a celebrity.

Even then, you had an inquiring mind. You taught yourself theory, used your lunch money for parts and were fixing the family radio while others were just starting to play with batteries and bulbs.

And basically, you haven't changed. You still get the same uninhibited kick out of seeing your ideas proven out and put to work. But maybe you find that the fields you're working in (or the state of the art you're working at) are already well-travelled. And you feel like the day you "discovered" Doppler radar in high school—a decade-and-a-half too late.

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tems for high performance and supersonic aircraft, are all pushing state-of-the-art frontiers with concepts like solid-state rate sensors that replace gyro systems, laser rangefinders, sophisticated computerized stabilization systems for space vehicles... and a host of others. More examples? Monolithic IC's with densities up to 2,000 active elements per chip. Computer-controlled weight and moment equalization systems with applications on orbital vehicles. Optimizing designs for analog and digital flight control and fly-by-wire systems ranging from VTOL to SST. And many more.

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nology on the campus of the State University of New York at Binghamton—a mile away from the General Electric facility.)

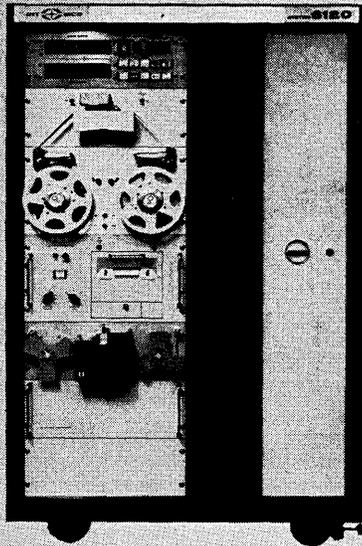
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CIRCLE NO. 85 ON INQUIRY CARD

Professional Development Seminars

Catalog covering the spring offerings of the Association for Computing Machinery Professional Development Seminars describes a total of nine different seminars scheduled for thirty-five cities during April, May, and June. ACM Professional Development, New York, N.Y.

Circle Number 319 on Inquiry Card.

Counting, Recording, Controlling Devices

Representative products of precision counting, recording, and controlling devices are presented in a new catalog illustrating the variety of applications for these instrument-type devices and assemblies, virtually all of which are custom made for commercial and military use. Veeder-Root, Hartford, Connecticut.

Circle Number 320 on Inquiry Card.

MIL-C-26500 Circular Connectors

Twelve-page catalog describes and illustrates in detail a line of circu-

lar connectors that conform to MIL-C-26500. Described and shown are types for various mounting applications; each style is available with threaded or bayonet-type coupling. Shell sizes are from 8 to 24. The contacts are the crimp, removable type per MIL-C-26636 and are available in size #12, #16, or #20.

The catalog also provides information on peripheral equipment such as dust caps, potting sleeves and assembly tools. Also provided is a part number cross reference of competitor connectors. Elco Corp., Willow Grove, Pa.

Circle Number 321 on Inquiry Card.

Flexible Printed Circuitry

Electrical characteristics, design information and a variety of applications of Flexprint® circuitry, which is said to permit greater design flexibility and increased circuit reliability, are described in a 14-page handbook available from the Flexprint Division of Sanders Associates, Inc.

The handbook includes current

applications, a table of insulation material characteristics for vinyl, mylar, aclar, FEP teflon, and kapton (H-film), and a conductor design chart which compares electrical characteristics of flat conductors with AWG round wire sizes. Methods of attaching Flexprint circuitry to various types of connectors are described along with instructions for low-cost design. The handbook also features standard specifications and tolerances for commonly used insulation materials. Sanders Associates, Manchester, N.H.

Circle Number 322 on Inquiry Card.

SPDT Thermostat

Bulletin outlines and illustrates single-pole double-throw No. 3700 thermostat, a miniature, snap-acting bi-metal disc thermostat designed for use wherever switching action is to be reversed instantly, from one terminal to the other (a third terminal is common). Often used to turn off current and actuate an overheat warning signal simultaneously, the No. 3700 is said to be suitable for computers, airborne



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Wire, Cable, Tubing

Two-color brochure lists product line and specifications of the producer's products in three groups: wire-cable-tubing, electronic hardware and switches, and radio-TV accessories and components. The 4-page folder gives a military switch cross reference, military and commercial specification charts for tubing products, hardware and wire and cable. In addition a chart gives the Underwriters Laboratories and C.S.A. specifications. Birnbach Company, New York, New York.

Circle Number 324 on Inquiry Card.

Ribbon Cable

Eighty-page handbook on the fundamentals and applications of flat-ribbon cable in the design and manufacture of electronic equipment, titled "Round Conductor Ribbon Cable Handbook," describes the advantages of round-conductor flat-ribbon cable, the mechanical and electrical/electronic characteristics of ribbon cables, and termination and interconnection techniques.

Other chapters cover nomenclature and terminology; and the wide range of cables and harnesses that can be fabricated with round conductor ribbon cable; ultra-flexible ribbon cable; ribbon cable for low capacitance or for high temperature applications; ribbon cables utilizing coaxial cable and other special purpose cables and harnesses. The Handbook is liberally illustrated with drawings, tables and photos. Price \$5.00. Spectra-Strip, Garden Grove, California.

Circle Number 325 on Inquiry Card.

Mass Memory

Specifications, functional block diagram and general description of the 20-million-bit Ampex Model RM mass core memory are contained in 6-page, two-color brochure C038. Ampex, Culver City, California.

Circle Number 326 on Inquiry Card.

Signal Wire and Tubing

Eight-page Catalog AP-B-1R1 is a guide to the manufacturers line of instrument tubing, thermocouple extension wire, and instrument wire and cable. The new bulletin includes the latest photos, selection parameters, and installation recommendations for a wide selection of instrument tubing. Included are plastic-jacketed metal tubing and bundles, plastic tubing and bundles, metal-armored bundles, fire-resistant bundles, and compact heat-traced packages.

Thermocouple extension wire and cable descriptions cover shielded and unshielded constructions, including armored and special high-temperature designs. Instrument wire and cable constructions for maximum rejection of electromagnetic noise are also presented. Samuel Moore & Company, Mantua, Ohio.

Circle Number 327 on Inquiry Card.

Hybrid Simulation Systems

Twelve-page brochure describes the capabilities that enable Scientific Data Systems to develop and produce hybrid simulation systems. SDS hybrid simulation systems are built around Sigma computers, which interface to any customer-furnished analog computer through custom-designed hardware and software. Basic hybrid interface hardware includes A-to-D and D-to-A conversion systems and memory interface, interrupt control, logic control, analog control, and frequency control units. Functions of these units, as well as a central processor, peripheral equipment and typical applications are described in the brochure. Scientific Data Systems, Santa Monica, California.

Circle Number 328 on Inquiry Card.

Modular Circuit Card Elements

Four-page data folder on interchangeable modular circuit card elements contains information on four basic card patterns: 8 and 10-pin T.O. 5, and 14 and 16-pin dual-in-line. In addition, specifications are included for other elements which may be used in the package. Elgin Electronics, Erie, Pennsylvania.

Circle Number 332 on Inquiry Card.

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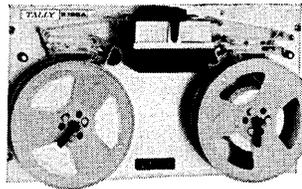
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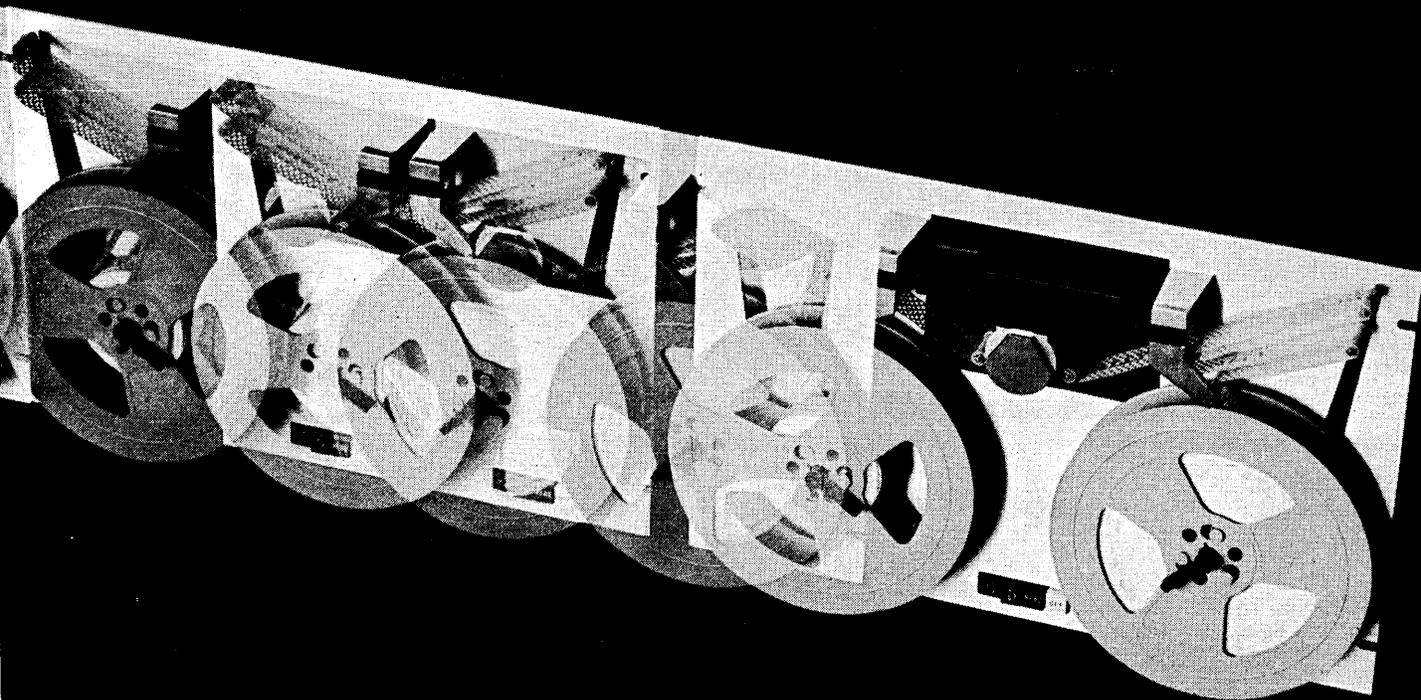


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