# XCELL

THE NEWSLETTER FOR XILINX PROGRAMMABLE GATE ARRAY USERS

Issue 1 Fourth Quarter 1988

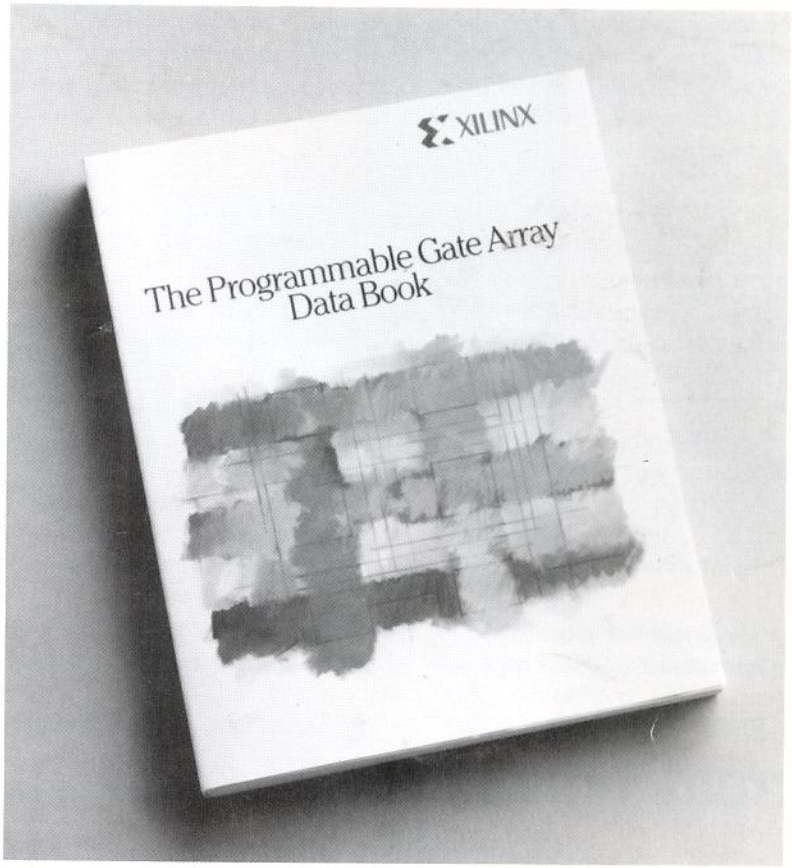

*Welcome to* XCELL, *the new Xilinx customer newsletter. By sending us your development system registration card you automatically became a charter subscriber to this quarterly publication. It is our intent to make this an informative, easy to read, responsive and—hopefully—interactive newsletter. We want to supply you with early and correct information, tell you about the status of our products and about our plans, about bugs and their workarounds, give you applications ideas and convey to you some of the enthusiasm that we feel for our Programmable Gate Arrays.*

*If you have questions or suggestions, please send them to me. "Letters to the Editor" make a newsletter more lively.*

Peter Alfke, Editor

## Table of Contents






# New Xilinx Data Book Is Available

The new Data Book contains the complete data sheets for our devices, the XC2064, XC2018, XC3020, XC3030, XC3042, XC3064, XC3090 and the XC1736, as well as military data sheets for the XC2000 family.

We explain Quality, Reliability and Testing issues, and give you an overview of the design flow and the development systems.

Twenty-five Application Briefs give details on LCA performance parameters, on metastability, and on methods to estimate size and performance. We show you many innovative design ideas from adders to code converters and state machines, and complete designs, like a FIFO controller, a 40 MHz presettable counter and an 8-digit Frequency Counter.

Ask your local Xilinx sales representative for a copy of this 320-page book, or drop us a note.

This Data Book has an ambitious goal. We want to prove to you that Xilinx is THE Programmable Gate Array Company, ready, willing and able to provide you with all the information and support you need to design with LCAs.

We want this to be the best Data Book in our industry. Only you can judge whether we have succeeded. Please tell us how we can improve it.

# Component Availability (OCTOBER 1988)

| | | 48 PIN | | 68 PIN | | 84 PIN | | 132 PIN | 175 PIN | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | PLASTIC DIP | CERAMIC DIP | PLASTIC PLCC | CERAMIC PGA | PLASTIC PLCC | CERAMIC PGA | CERAMIC PGA | CERAMIC PGA | |
| | | -PD 48 | -CD 48 | -PC 68 | -PG 68 | -PC 84 | -PG 84 | -PG 132 | -PG 175 | Mil-Std-883 Class B |
| XC2064 | -33 | C | I M | C I | C I M | | | | | |
| | -50 | C | I | C I | C I M | | | | | |
| | -70 | | | C | C | | | | | |
| XC2018 | -33 | | | C I | | C I | C I M | | | B: 4Q88 |
| | -50 | | | C I | | C I | C I M | | | B: 4Q88 |
| | -70 | | | C | | C | C | | | |
| XC3020 | -50 | | | C I | | C I | C I M | | | B: 4Q88 |
| | -70 | | | C I | | C I | C I | | | |
| XC3030 | -50 | | | | | Dec.'88* | Dec.'88 | | | B: 2Q89 |
| | -70 | | | | | Dec.'88* | Dec.'88 | | | |
| XC3042 | -50 | | | | | Dec.'88* | Dec.'88 | 4Q88 | | B: 1Q89 |
| | -70 | | | | | Dec.'88* | Dec.'88 | 4Q88 | | |
| XC3064 | -50 | | | | | | | 1Q89 | | B: 3Q89 |
| | -70 | | | | | | | 1Q89 | | |
| XC3090 | -50 | | | | | | | | C I M | B: 1Q89 |
| | -70 | | | | | | | | C | |

LCA Package and Temperature Options

| | |
|---|---|
| C = Commercial | 0°C To 70°C |
| I = Industrial | -40°C To 85°C |
| M = Military | -55°C To 125°C |
| B = Military | MIL-STD-883, Class B |

* Engineering Samples Now
Shaded Areas: Not Meaningful

XC1736 PD8C (Plastic 8-Pin Mini-DIP, -40°C to +85°C)
XC1736 CD8C (Ceramic 8-Pin Mini-DIP, -55°C to +125°C)

# Current Software List

The following is a list of the current software revision levels for each of Xilinx's development system products currently being shipped (Oct 1988). Make sure that you have up-to-date versions of this software.

**DS21 XACT ver. 2.12:**
XACT ver. 2.12 (3 disks)
XC3090ES Update (3 disks)
DOS 16/M Loader ver. 2.49 (1 disk)
XC3030/XC3042 die files (2 disks)

**DS22 P-SILOS ver. 2.01**
P-SILOS ver. 2C.5 rev 2 (2 disks)
XNF/LCA intrfce ver. 2.11 (2 disks)
XNF2SILO ver 2.01

**DS23 ADI ver. 2.10**
APR ver. 2.13 ( 2 disks)
XNF/lca intrfce ver. 2.11 (2 disks)
Logic Synthesis ver. 1.00 (1 disk)

**DS28 XACTOR ver. 2.10**
XACTOR 2.10 (1 disk)

**DS31 FutureNet DASH ver. 2.01**
FutureNet interface and library
PIN2XNF ver.2.01 (5 disks)

**DS40 FutureNet TTL Library**
ver. 1.0 (1 disk)

**DS33 Daisy Interface (DNIX)**
ver. 1.04 (6 disks)

**DS51 ver. 2.11**
DS52 ver. 2.10
DS21 XACT ver. 2.11

**DS52 ver. 2.10**
Schema II ver. 2.03 (4 disks)
Xilinx/Schema intrface ver. 2.01
DS23 ADI ver. 2.10

**DS53 ver.2.12**
DS54 ver. 2.10
DS21 XACT ver. 2.12

**DS54 ver. 2.10**
DASH-LCA ver. 4.02r (2 disks)
PIN2XNF ver.2.01(5 disks)
DS23 ADI ver. 2.13

**DS81 Ser. Config PROM Programmer**
SCP Programmer ver. 2.00 (1 disk)
XPROM ver. 2.00

# Fast Bidirectional Counters for Robotics

The position of a robotics arm is usually determined by three shaft encoders in the form of up/down pulse generators and counters. At a maximum speed of 5 meters per second and a resolution of 1 micron, these counters must resolve 0.2 µs pulses and should have a capacity of at least 2 million steps. The counters must have an easy interface to the microprocessor so that the count value can be read on-the-fly, without ambiguity.

The established microprocessor peripheral counters have severe limitations. They usually are too short (16-bit), lack up/down control or quadrature clock inputs, and cannot be read easily.

Now Xilinx suggests a design that packs three 22-bit counters into one LCA, the XC 3020. Max count rate is 8 MHz, and the count values can easily be read on-the-fly. The counter architecture is somewhat unconventional. Each counter consists of two parts:

1. A conventional up/down 4-bit Grey-code counter with a capacity from -8 to +7. This counter is asynchronous to the system clock, affected only by the incoming count signals.

2. A 20-bit up/down counter in the form of a 20-bit recirculating shift register, a serial adder/subtractor, and a carry/borrow flip-flop. This shift register forms the most significant part of the counter. Synchronous with the LCA clock, it is easily synchronized to the microprocessor clock. At a 20 MHz clock rate it recirculates once, and can be incremented, decremented, or read, once per microsecond.

Communication between these two parts of the counter is through a carefully controlled mailbox. Whenever the 4-bit up/down counter reaches plus or minus 8, it sets a carry or a borrow flip-flop. The shift register counter accepts these inputs synchronously with a max delay of 1 µs.

When the microprocessor wants to read the counter, it first disables the interaction between the two parts of the counter. Then the two parts of the counter are transferred into 24 output registers and their interaction is enabled again. This mechanism insures reliable read-out, even if the counter is oscillating around certain critical values.

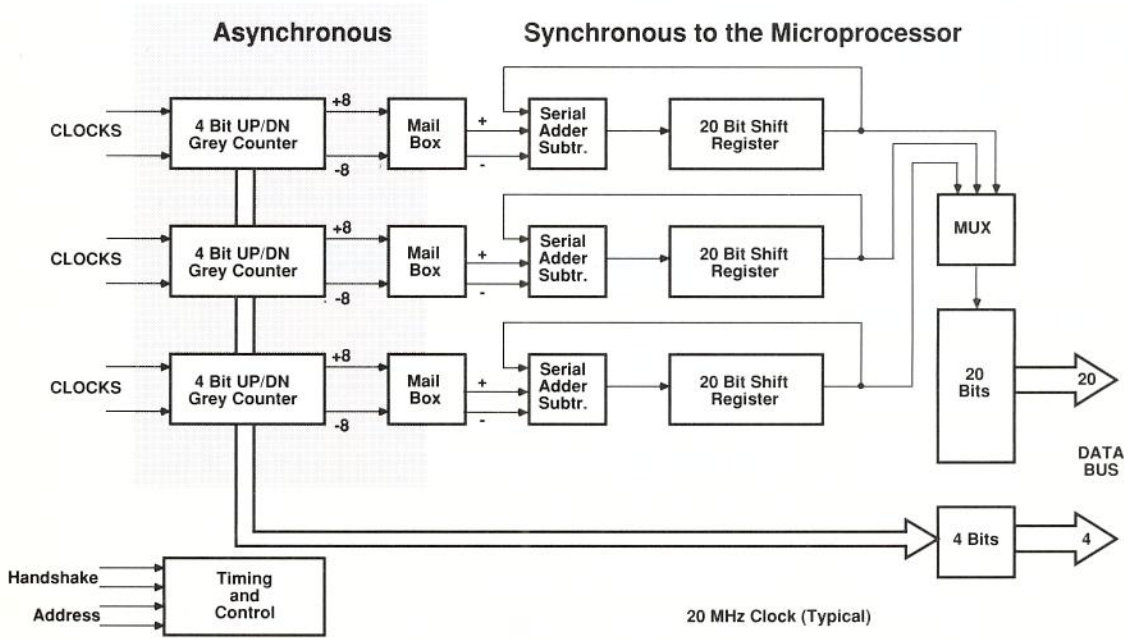
The problem of a traditional up/down counter is that it, worst case, can oscillate between two values where all (or most) counter bits change at the incoming count rate. This makes a reliable microprocessor interface virtually impossible.

In this design the most significant 20 bits of the counter do not have this problem, and the least significant 4 bits count in a Grey code, where only one bit changes on any clock transition. Such counters can safely be read on-the-fly. This safe and compact design puts one additional burden on the microprocessor: The two parts of the counter must be added in software, since they have independent sign bits. Considering the other advantages, that seems like a small price to pay.

Possible variations:

Speed can be increased to 20 MHz by changing the partitioning from 4/20 bits to 8/16 bits. The up/down count control can be implemented in several ways.

Please note that this design has not been built. We welcome responses from our readers about real-life requirements for such a circuit. **P.A.**




**Triple 22-Bit Up/Down Counter (Plus Sign with Microprocessor Interface**

# How to Run XACT in EGA or VGA Mode

The XACT and XACTOR programs can display graphics in CGA, EGA, or VGA mode. The graphics mode used by XACT or XACTOR is always fixed for a complete session. You may change the graphics mode from session to session.

The default graphics mode is CGA since it is simplest. Xilinx recommends that you use EGA or VGA, as their resolution is far superior to CGA (CGA: 320 x 200 pixels, EGA 640 x 350 pixels, VGA: 640 x 480 pixels).

If you want to use CGA, there is nothing that you need to do or set up to indicate this to XACT and XACTOR. To choose the EGA or VGA graphics mode you must set an environment variable, GRMODE, in your AUTOEXEC.BAT file as follows:

```
SET  GRMODE=EGA   or
SET   GRMODE=VGA
```

You may also set the GRMODE variable to CGA :

```
SET   GRMODE=CGA
```

if you want to always be explicit about which graphics mode should be used. The XACT and XACTOR programs will read this environment variable when they are invoked and will then display graphics in the selected mode.

Without an EGA or VGA display card in your PC, you should not set the GRMODE variable to EGA or VGA. If you do, the screen will go blank after you invoke the XACT or XACTOR program. The programs simply assume that you have the correct hardware for the indicated graphics mode.

Whether or not you already have the GRMODE environment variable set, you may set it again or set it with a different value, when the normal DOS prompt is displayed. To do this you just type the command:

```
SET  GRMODE=EGA   or
SET   GRMODE=VGA
```

and then press the "enter" key. If you then type "set" and press the "enter" key, you will see all the environment variables that are set and whether the GRMODE variable is set correctly. If it is not set correctly, just re-type the "SET GRMODE=" command with the correct value. You must do this BEFORE invoking the XACT or XACTOR programs. You may NOT change the graphics mode in the middle of an XACT or XACTOR session.

## *A Short History of XACT*

The 1.3 release supported the 2000 family only. It used bank-switched EMS memory to overcome the 640K limitation of the PC.

The 2.01 release in late '87 supports both the 2000 and the 3000 families. For performance reasons it abandons bank switching and uses the '286 in protected mode with **extended** memory, managed by DOS/16M.

The 2.10 release in May of '88 fixes some bugs and improves the performance, a significant factor in XC3090 support.

The 2.11 and 2.12 release each fix bugs that affected the capability of XACT to unroute and then re-route a design.

## Fast Counters

We just finished the design of a 40 MHz presettable counter described in the new Data Book. We also built a 100 MHz, 8 digit Frequency Counter with LED readout, using an inexpensive watch crystal as time base. The logic fits in one XC3020.

In this newsletter we explain an idea for a triple 22-bit (plus sign) 8 MHz counter with a convenient and safe microprocessor interface.

## Colorblind? Use Cyan / Magenta

Many men, but surprisingly few women are yellow-green colorblind. Normally, this may be just a minor inconvenience. For a design engineer using the Xilinx Design Editor, however, this is a horse of a different color.

XACT uses Red, Yellow, and Green with a Black background. If you are color blind it is very difficult to distinguish between Green and Yellow.

Now there is a software solution to this problem. In the XACT Program Executive (the first graphics screen which appears after you invoke XACT) there is a new command in the PROFILE menu. It is called PALETTE, with two options: "GREEN/RED/YELLOW" and "CYAN/MAGENTA/WHITE." Thus, if you are yellow-green colorblind, you can select the "CMW" palette.

*Remember to save your profile after you have changed the palette.*

## Four "Ones" Added to Configuration Bit Stream

The 2.11 and later releases of XACT changed the bit-stream by adding four more dummy "ones" to the beginning of the header and increasing the length count by four. This change was made in order to simplify the software and make different software packages consistent.

This small change makes the configuration bit file, when read as bytes, completely different, virtually unrecognizable from the older version.

DOWNLOAD will, however, work with either version of the .BIT file, and MAKEPROM and XACTOR can use either version of .BIT files, or even a mixture of them.

There was no change in the silicon—the chip still only requires four leading "ones" minimum.

The new Sept. '88 Data Book lists the new code, but also mentions that the chip only requires four leading "Ones."

# Why Is There A Clone Compatibility Issue?

XACT is a large, demanding program, using interactive graphics, requiring megabytes of RAM. This pushes the IBM-PC into uncharted waters.

The '286, in REAL mode, can only address 640 K bytes, obviously not enough. Bank-switching is a well-known trick to increase the apparent addressing range, but it is unacceptable since it would degrade performance dramatically.

Our only choice is, therefore, to run XACT in PROTECTED mode where the '286 can address 16 megabytes of extended memory.

In PROTECTED mode the '286 has no access to its BIOS, keyboard or mouse. These are only available in REAL mode, so our program must toggle very often (many times per second) between REAL and PROTECTED MODE.

We use an application development tool from Rational Systems Inc., Natick, MA, called DOS/16M. This program allows applications written in C (as is all Xilinx software) to run in PROTECTED mode on '286 and '386 microprocessors. DOS/16M acts as an interface between the application and DOS, intercepting interrupts and switching from PROTECTED to REAL mode as necessary before resignaling or handling the interrupt.

Now we get to the problem: Intel gave the '286 an instruction to switch from REAL to PROTECTED mode, but, unfortunately, no instruction to switch back from PROTECTED to REAL mode. Pulling RESET is the only way.

IBM then implemented this "Return to real mode" in—of all places—the keyboard controller! Perhaps they found some unused code space and just stuck it in. So the switch from PROTECTED to REAL mode is done in a very clumsy way. It works predictably in the IBM AT, but not in all clones.

For legal reasons, clone manufacturers have to use a BIOS that is a functional emulation, not a direct copy of the IBM BIOS. The creators of some clone BIOS took liberties with the seemingly uncritical control of the keyboard.

So they tend to behave differently, and that is the reason for most of our compatibility problems. Until recently, very few popular software packages used PROTECTED mode, and these idiosyncracies have, therefore, gone unnoticed.

DOS/16M has implemented a wide variety of workarounds to accomodate the different BIOS and keyboard controller flavors. It also suggests several different switchmode settings to avoid problems that defy the general solution.

Note that these problems are fundamentally caused by a "flaw" in the '286. The '386 can switch back to real mode. It may mean the end of most compatibility problems on '386 based machines.

The following computers do run Xilinx software without problems. Since Xilinx has these computers in-house, if any software problems should show up, Xilinx will supply a solution.

IBM PC/AT
IBM PS/2 Models 60 or 80
Compaq 286 or 386
Compaq Portable 286 or 386
Compaq Portable II or III
HP Vectra ES or ES/12
AST Premium 286 with BIOS 3.03 or higher.

Xilinx Applications runs four Proteus 386 (16 MHz, 6 Mbytes of RAM) without any problems. We chose them for the best "bang for the buck" in the summer of '88, but this is a fast-changing world...

The following computers are known to have problems running Xilinx software.

Comcen 286 AT (mouse)
CSS Computer (keyboard)
FORTRON 386 (keyboard)
Leading Edge
MEK 386
NCR PC 916
OPC AT
PC Limited 286
Tandon PCA
Trigem AT

You can test the compatibility of your PC by running PMTEST.

Before making any PC buying decision, please ask Xilinx Applications for a more complete list of PC compatibility issues.

## All DOS Are Not Created Equal

Some clone manufacturers supply their own version of DOS which may differ from the real, true blue DOS sold by IBM.

In case of mysterious unresolvable software problems on clones using non-IBM DOS, we suggest changing, if not to the IBM hardware, at least to the IBM DOS.

## Don't Be Longwinded

Names longer than 22 characters cause a nasty interrupt (000D) in APR. No serious problem in English, but some Germanic languages allow unlimited concatenation of nouns, like:

Speicheradressendekodierschaltung
Mikroprozessorversorgungsspannung
Doppelfehlerkorrekturalgorithmus
Kylvattennivåövervakningssignalingång

Our German and Scandinavian users should avoid such names.

## North-East Sales Office Moved to Nashua, NH

The new address for the Xilinx sales office covering the New England states, New York, New Jersey, and Canada is:

**61 Spit Brook Road,**
**Fourth Floor**
**Nashua, NH 03060**
**Phone: (603) 891-1096**
**Fax: (603) 891-0890**

## Beware of the Power of an In-Circuit-Emulator

When a microprocessor emulator is hooked into a system, proper sequencing of the two power supplies—Emulator and System—is very important. Improper sequencing can blow up devices.

A powered-up emulator with (typically) 74240-type outputs driving a logic High into non-powered up system, can cause severe damage.

The logic High input on a device that has Vcc = 0V (or very low) will forward-bias the input protection diode (ESD protection) and can route large amounts of current into this pin and out of the Vcc lead, if Vcc is not free to float High. In a large system with many MOS and bipolar devices, as well as decoupling and supply storage capacitors connected to the Vcc bus, this bus (or plane) can be considered an almost unlimited current sink once it has reached +1V.

The current source capability of a 74LS240-type output that is logically High, but clamped down to 1 or 2 V can be as much as 200 mA per output!

Many outputs of an emulator can thus together drive several Amperes into the Vcc bus of the target systems, and this current will take the route of the best (lowest drop) protection diode. CMOS output drivers have a very good diode to Vcc, it is the p-channel output transistor's drain acting as a diode. This large diode is likely to take most of the current coming from the emulator, and this current can easily blow the Vcc bonding wires within milliseconds.

The problem can only be avoided by proper supply sequencing (turn the system on first, the emulator last, reverse sequence for turn-off), or by other means of limiting the current being driven across the interface, especially the current into the Vcc leads of the target CMOS devices.

Even if the current is low, there is another problem: The clamp current from a powered input might sustain a degenerate Vcc level, which might prevent proper initialization when Vcc is re-applied.

# DIN Hold Time Poses No Problem

Cautious designers have pointed out an inconsistency in the original specification for the XC3000-series CLB timing parameters:

DIN has a hold time requirement of 4ns (-70 part), while the clock to output delay is specified as 8ns max, no minimum value is given. This has raised the concern that a fast part might have an output delay shorter than the hold time requirement, which would make the DIN input useless. This problem does not exist in reality, because all delays on a given chip track very well, even with temperature and supply voltage variations.

The new Sept. 88 Xilinx Data Book states clearly in a note to the CLB timing specifications on page 2-41:

"The CLB K to Q output delay of any CLB, plus the shortest possible interconnect delay, is always longer than the DIN hold time requirement."

The applications section (page 6-18) discusses this problem more generally:

"All delays track very well over temperature, supply voltage and processing variations, never deviating more than 30% from each other's normalized value."

If two parameters are specified with a 2:1 ratio, the most extreme variations of this ratio are:

$(2+30\%) \div (1-30\%) = 2.6 \div 0.7 = 3.7$

$(2-30\%) \div (1+30\%) = 1.4 \div 1.3 = 1.1$

In other words, the parameter specified as 8 ns will *always* be larger than the one specified as 4 ns.

While we are on the subject: A battle has raged for 20 years whether to specify set-up and hold-time requirements in the maximum or the minimum column. It is a purely semantic problem: a minimum for the device is a maximum for the system, and vice versa. Rather than add confusion and open old wounds, let's say that every reader is entitled to move set-up and hold-time numbers to the column of choice.

A similar confusion rages around the clock frequency. Is it: clock frequency = 70 MHz (max) or is it: max clock frequency = 70 MHz (min)? Both methods are correct, but the first one has room for a zero (min) specification to indicate static operation.

**Latch-up** is a totally different phenomenon. It can occur when a CMOS output is forced higher than Vcc, while Vcc is capable of sourcing substantial current.

Under these circumstances the CMOS structure looks like a Silicon-Controlled-Rectifier, i.e. once triggered it will stay conducting and can conduct almost unlimited current, thus potentially self-destructing.

Modern CMOS output structures have been made resistant to this problem. It takes several hundred milliamps to trigger the SCR, and the trigger must be sustained for milliseconds to cause the latching feedback SCR action.

The required high trigger current and long duration make Xilinx LCA outputs extremely latch-up resistant.

## Typographical Error in the New Data Book

The table of XC3000, "General LCA Switching Characteristics," on page 2-44 lists the timing units as nanoseconds. They really are microseconds (values between 0 and 7 µs). The equivalent parameters for the XC2000 family are labeled correctly on page 2-87.

The XC1736 pin assignment drawing on page 2-113 shows an erroneous overbar over RESET.

These are the only misleading errors that we have found so far.

## Outputs Can Switch Simultaneously

When many outputs drive capacitive loads simultaneously in the same direction, the resulting current spikes cause significant voltage drops on the supply bonding wires inside the package. This has been called "ground bounce," and Xilinx designers were very much aware of this problem. The Xilinx devices, therefore, have a very effective supply distribution grid on the chip, and have multiple supply pins (two Vcc/ground pin pairs on the 68 and 84 pin packages, eight Vcc/ground pin pairs on the 132- and 175- pin packages).

As a result, we allow the simultaneous, fast mode, same direction, switching of a total combined load of 1000 pF for the 84-pin and smaller packages, of 4000 pF for the 132-pin and larger packages (See the note below the IOB switching table on page 41 of the 3000 family data sheet, and page 2-43 of the new Data Book). In slow mode this capacitance can be four times larger.

See also the first lines of page 2-26 in the new Data Book: "Slew-limited outputs maintain their DC drive capability, but generate less external reflections and internal noise. More than 32 fast outputs should not be switching in the same direction exactly simultaneously. A few ns of deliberate routing skew can alleviate this problem of "ground-bounce."

P.S. The unloaded output slew rate has been measured as 3 volts per nanosecond(!) in fast mode. It is approximately 0.5 volts per nanosecond in slow mode, which should be the standard mode for all outputs that are not very speed-critical. Slow mode is, therefore, the default mode. Note that slow mode has **no reduction** in dc drive capability. See pages 6-14 and 15 of the new Data Book for more information on "Additional Electrical Parameters."

## XC1736-Vpp Must Be Tied To Vcc

When using the programmed 1736, Vpp must be tied to Vcc. Failure to do this will result in unpredictable access times and thus in unpredictable, temperature-dependent operation.

We state this requirement clearly in the data sheet pin description, but some users ignored it and they are in for a long search, trying to find the bug in a design that worked "most of the time."

Also, don't forget to tie the unused PWRDWN input of an LCA to Vcc.

## New Speeds File

XACT 2.12 includes corrected XC 3020 SPEEDS.XCT file coefficients.

Since these coefficients are shared with other software, this file must be duplicated and named as shown below:

1. Locate the SPEEDS.XCT file in the XACT directory.

2. Duplicate this file two times by typing the following commands:

```
Copy SPEEDS.XCT SPEEDS.APR
Copy SPEEDS.XCT SPEEDS.L2X
```

## PLCC Sockets Share The PGA Footprint, But Have Different Pin-Out

If you want to use a socketed PLCC on a PGA-based PC board, you are in for a surprise and a rather complex rats nest of an adapter. Look carefully at our pin-out descriptions, they show you the difference. This problem indicates a lack of standardization in our industry.

## Strange Output Levels

A properly configured and properly used LCA will always have $V_{OL}$ below 0.3V and VOH above 4 V.

If the user ever measures a static output voltage between these two values, something is seriously wrong. We have seen two possibilities:

- Contention between two outputs as a result of wrong interface design. An LCA output fighting an LS-TTL output can generate 1.5 or 2.5 V. Since the output current can be as high as 50 mA, this situation should not be allowed to persist for more than a few seconds.
- Wrong configuration. If the LCA has read erroneous configuration data, it might create internal contention which might even generate strange output levels. This situation must also be cured immediately.

## *If All Else Fails, Read the Instruction Manual...*

We know that reading manuals is no fun. It has also been said that "power users do not read manuals..." In spite of this we want to encourage our users to read the manuals. There is a lot of useful and important information in those binders, and many of your questions are already answered there.

We just mailed you the first application notes from our series of User's Guides, easy-to-read, practical explanations of sometimes confusing issues like:

**Configuring LCAs**
**Designing LCAs with Boolean Equations**
**Simulating Bidirectional I/O's**
**Dev. System Hardware Requirements**

This series will be continued.

Our new Data Book is a well-organized treasure trove of information. It even has an index, starting on page 8-1. You see, we are trying very hard to make the information accessible and easy to find.

So, before you get frustrated and grab the phone:

*PLEASE READ THE MANUAL!*

We, in turn, promise to make the manuals more readable and the software more user-friendly.

## FALL 88

# Seminar Series

*Xilinx will give technical seminars in the cities listed to the right. These seminars emphasize designing with the XC3000 family and the newer development systems. If you have not yet designed with the XC3000 family, we recommend that you attend. If you are already familiar with the XC3000 family, you might recommend this seminar to a friend.*

## Agenda

- Programmable Gate Arrays, a Technical Description
- Performance / Density / Cost
- Design Methodology
- Development Systems
- Applications Examples
- Live Demonstration of a Complete
- Design, from Schematic Capture to Working Prototype

### USA & Canada

| | |
|---|---|
| Sacramento, CA | 9-16 |
| Milpitas, CA; Chicago, IL | 9-20 |
| Detroit, MI | 9-21 |
| Seattle, WA | 9-28 |
| Portland, OR | 9-29 |
| King of Prussia, PA | 10-3 |
| Rochester, NY; Tyson's Corner, VA | 10-4 |
| Toronto,ONT Atlanta, GA | 10-5 |
| Ottawa,QUE Huntsville, AL | 10-6 |
| Montreal, QUE | 10-7 |
| Col.Springs,CO; Marlboro, MA | 10-11 |
| Boulder, CO Boston, MA | 10-12 |
| Salt Lake City, UT; Waterbury, CT | 10-13 |
| Phoenix, AZ | 10-14 |
| Chatsworth, CA | 10-18 |
| Irvine, CA | 10-19 |
| San Diego, CA | 10-20 |

### Europe

| | |
|---|---|
| København | 12.Oct |
| Malmö | 13.Oct |
| Oslo | 14.Oct |
| Stockholm | 17.Oct |
| Helsinki | 18.Oct |
| Wien | 20.Oct |
| Madrid | 25.Oct |
| Bruxelles | 26.Oct |
| Utrecht | 27.Oct |
| Bracknell | 31.Oct |
| Cambridge | 1.Nov |
| Manchester | 2.Nov |
| Livingston | 3.Nov |
| Milano | 4.Nov |
| München | 21.Nov |
| Karlsruhe | 22.Nov |
| Hamburg | 24.Nov |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