WD33C93B

Enhanced SCSI Bus

Interface Controller

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 DESCRIPTION

The 33C93B, a MOS/VLSI device implemented in Western Digital's CMOS process, operates from a single 5 volt supply and is available in either a 44-pin PLCC or a 40-pin dual-in-line (DIP) package. All inputs and outputs are TTL compatible.

The 33C93B is intended for use in systems which interface to the Small Computer System Interface (SCSI) Bus. The 33C93B can operate in both the initiator (typically, a host computer system) and the target (typically, a peripheral device) SCSI bus roles.

When used in the host system, the 33C93B interfaces to both the host bus and the SCSI bus. To perform a SCSI operation, the host processor issues a command to the 33C93B to select the desired target. The 33C93B then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a device with higher priority, it continues trying and notifies the host when it has succeeded by generating an interrupt. At this point, the 33C93B is operating in the initiator role. When the peripheral requests a SCSI command from the host, the 33C93B receives the request and generates another interrupt to the host. The host responds to this interrupt by issuing a "Transfer Info" command and supplying SCSI command bytes to the 33C93B. The 33C93B transfers the SCSI command to the peripheral and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The 33C93B also offers high-level Select-and-Transfer commands which eliminate the interrupt handling otherwise required between each SCSI bus phase.

When the 33C93B is used in a peripheral system, the 33C93B operates primarily in a target role. It interfaces with a local processor and the SCSI bus in this environment just as it does when used in a host adapter. The target-role command set enables the 33C93B to request each SCSI bus phase individually or to sequence the SCSI bus phases automatically through the use of combination commands.

The 33C93B has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-free mode for standard SCSI applications.

1.2 FEATURES

- Implements full SCSI bus features: arbitration, disconnect, reconnect, parity generation and checking on both data ports, soft reset, and synchronous data transfers.
- Includes 48 mA drivers for direct connection to the SCSI bus.
- Operates in both initiator and target roles.
- Synchronous offset selectable from one to twelve bytes.
- Programmable timeout for selection and reselection.
- Support for SCSI-2 features:
  - Synchronous transfer rates up to 10 Mbytes/s for Fast SCSI transfers; up to 5 Mbyte/s for standard SCSI transfers.
  - Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive commands provide support for queue tag messages and target routine identify messages.
- Special "Translate Address" command performs the Logical-to-Physical address mapping.
- "Combination" commands greatly reduce interrupt-handling responsibilities.
- Compatible with most microprocessors through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature.
- Burst data transfers up to 4096 bytes.
- Data transfer options include programmed I/O, single-byte DMA, burst (multibyte) DMA, or direct bus access (WD bus) transfers.
- Single +5 V supply.
- Available in 44-pin PLCC or 40-pin DIP.
- Low-power CMOS design.

1.3 DIFFERENCES BETWEEN THE 33C93A AND 33C93B

The 33C93B delivers the same functionality as the 33C93A as well as additional features to support SCSI-2 and improve system performance. Unless the device is configured with the RAF bit in the OWN ID register set, the 33C93B is completely backward compatible to the 33C93A; consequently, in most applications, it may replace the 33C93A with no modification to the hardware or the firmware.

The 33C93B has grouped several recently added features of the 33C93A with two 33C93B-only enhancements into a mode enabled by configuring the device with the RAF bit set. Section 4.3.1 describes this new mode. The first two features---the loading of the microcode revision on a soft reset condition and the aborting of a target Receive command upon the detection of the SCSI Attention condition or of a parity error---existed in the 33C93A design. The 33C93B design has added to this mode the ability to detect possible data corruption and unexpected disconnects from the SCSI bus when operating as a target.

To support SCSI-2, the combination commands Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive optionally send or receive Queue-tag messages at appropriate points in the SCSI bus sequence. The host via two bits in the Destination ID Register and the newly added Queue Tag Register provides information which the first two commands use to generate and check these messages. Wait-for-Select-and-Receive, through the same locations, relays information to the host regarding the type of Queue-tag message received, including whether the initiator sent a message or not, and the actual queue tag.

These commands also support the LUNTAR bit in the Identify message. By setting the corresponding bit in the Target LUN Register, the host enables the Select-and-Transfer and Reselect-and-Transfer commands to send an Identify message for a target routine. In the case of Select-and-Transfer, setting this bit also enables the 33C93B to accept automatically an Identify message with the LUNTAR bit set. The host also has the option to let the Wait-for-Select-and-Receive command receive a target routine Identify message and proceed to the next phase or to interrupt the host so that it may reject the message when the application does not support target routines.

The last new feature pertaining to SCSI-2 relates to Fast SCSI. When the 33C93B has an input clock between 16 MHz and 20 MHz, by controlling the Fast SCSI Select (FSS) bit in the Synchronous Transfer Register, the host can select between normal synchronous transfers which reach a maximum transfer rate of 5 MB/s and Fast synchronous transfers with a peak rate of 10 MB/s on both the SCSI and host DMA interfaces.

The final addition to the 33C93B is the FIFO Full/Empty (FFE) bit in the Auxiliary Status Register to be used primarily during polled I/O transfers. As its name suggests, this bit reflects the full or empty state of the FIFO depending on the direction of the transfer. If the host is writing data to the FIFO, the 33C93B sets this bit when the FIFO is empty, indicating that the host may write up to twelve bytes to the FIFO without having to poll the DBR bit before writing each byte. Similarly, when the host is reading data from the FIFO, the 33C93B sets this bit when the FIFO is full, indicating that the host may read the Data Register twelve times without polling DBR before each read. Some restrictions do apply when using this bit, and they are described in Section 3.1.22.

2.0 PIN DESCRIPTIONS

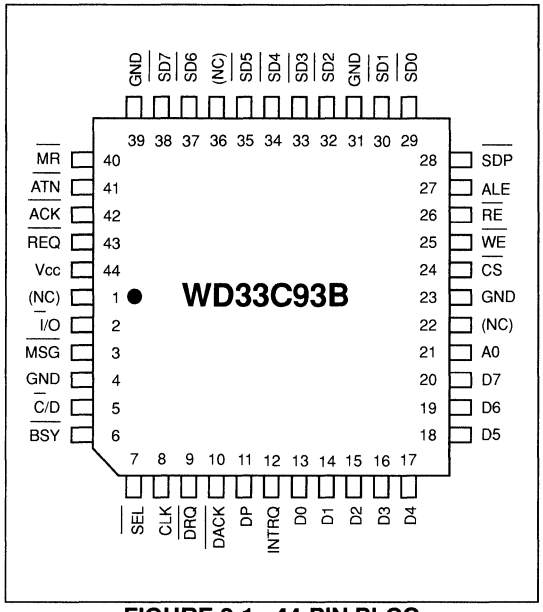


FIGURE 2-1. 44-PIN PLCC

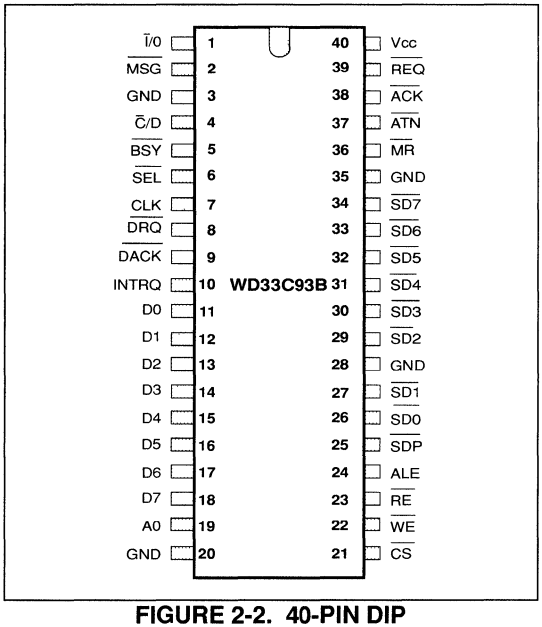


FIGURE 2-2. 40-PIN DIP

2.1 PROCESSOR/DMA INTERFACE

NAME	I/O	DESCRIPTION
CLK	I	8-20 MHz square wave clock
MR	I	Reset is an active-low input which forces the 33C93B into an idle state and forces all SCSI signals to the negated state.
INTRQ	O	Interrupt Request to the external microprocessor indicates a command completion/termination or a need to service the SCSI interface. Reading the SCSI Status Register clears this bit.
RE	I/O	Read Enable is an active-low input used with CS to read a register or with DACK to access the DATA register in DMA mode. In WD Bus mode, it is used as an output to read data from a sector buffer. (Tri-state).
WE-	I/O	Write Enable is an active-low input used with CS to write a register or with DACK to access the Data Register in DMA mode. In WD Bus mode, it is used as an output to write data to a sector buffer. (Tri-state)
CS	I	Chip Select is an active-low input which qualified RE and WE when access sign a register. This signal must be inactive during a DMA cycle (DACK active in DMA and Burst DMA mode or DRQ active in WD Bus mode).
A0	I	Address Pin A0 is used to access the internal registers for non-multiplexed address/data busses (i.e.; the ALE pin is grounded). The address of the desired register is loaded into the address register during a write cycle with A0=0. The selected register is then accessed when A0=1.

TABLE 2-1. SIGNAL DESCRIPTIONS

NAME	I/O	DESCRIPTION
ALE	I	Address Latch Enable is used for multiplexed address/data busses to load the address of the desired 33C93B register from the data bus. For indirect addressing, the ALE pin should be grounded. See the description of the Address Register for a complete discussion of direct and indirect addressing.
$\overline{\text{DACK}}$ ($\overline{\text{RCS}}$)	I/O	DMA Acknowledge is an active-low input used for interfacing to an external DMA controller (e.g. 8237). When $\overline{\text{DACK}}$ is low, all bus transfers are to or from the DATA register regardless of the contents of the Address Register. In WD Bus mode this pin, an open-drain output, functions as a RAM Chip Select to the sector buffer. $\overline{\text{RE}}$ and $\overline{\text{WE}}$ are outputs when $\overline{\text{RCS}}$ is active. Regardless of the host DMA mode selected, this pin should be pulled via external circuitry (e.g. a pullup resistor) to an inactive state and should not be left floating.
$\overline{\text{DRQ}}$	I/O	Data Request is an active-low output when used for interfacing to an external DMA controller and an active-high input when in WD Bus mode. In the first application, $\overline{\text{DRQ}}$ and $\overline{\text{DACK}}$ form the handshake for the DMA data transfers. In Burst mode, $\overline{\text{DRQ}}$ remains low so long as there is data to transfer; in Single-byte DMA mode, $\overline{\text{DRQ}}$ toggles for each byte. Since this pin is an open drain output, a pullup resistor may be required when operating in these modes. In WD Bus mode, this pin becomes the DRQ input. A high level on this pin enables the 33C93B to perform burst transfers; a low level inhibits transfers by deasserting $\overline{\text{RCS}}$ and disabling the $\overline{\text{RE}}$ and $\overline{\text{WE}}$ outputs.
D7 - D0	I/O	Processor data bus.
DP	I/O	Data Parity is used only for checking and generating parity during data transfers.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

2.2 SCSI INTERFACE

NAME	I/O	DESCRIPTION
$\overline{ATN}$	I/O	$\overline{ATN}$ is an output in the initiator role and an input in the target role. Its assertion indicates the ATTENTION condition.
$\overline{REQ}$	I/O	$\overline{REQ}$ is an input in the initiator role and an output in the target role. It indicates a request for a data transfer.
$\overline{ACK}$	I/O	$\overline{ACK}$ is an output in the initiator role and an input in the target role. It indicates an acknowledgement of a data transfer.
$\overline{MSG}$	I/O	$\overline{MSG}$ is an input in the initiator role and an output in the target role. The target asserts this signal when requesting message information.
$\overline{C/D}$	I/O	$\overline{C/D}$ is an input in the initiator role and an output in the target role. It specifies whether control or data information is on the SCSI data bus.
$\overline{I/O}$	I/O	$\overline{I/O}$ is an input in the initiator role and an output in the target role. It controls the direction of data movement on the SCSI data bus with respect to an initiator.
$\overline{SD7}$	I/O	SCSI data bus.
$\overline{SD0}$	I/O	SCSI data bus.
$\overline{SDP}$	I/O	SCSI data bus parity signal.
$\overline{BSY}$	I/O	$\overline{BSY}$ is asserted when the 33C93B is attempting to arbitrate for the SCSI bus or when connected as a target.
$\overline{SEL}$	I/O	$\overline{SEL}$ is asserted when the 33C93B is attempting to select or reselect another SCSI device.

NOTE: All pins have open-drain output drivers.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

24

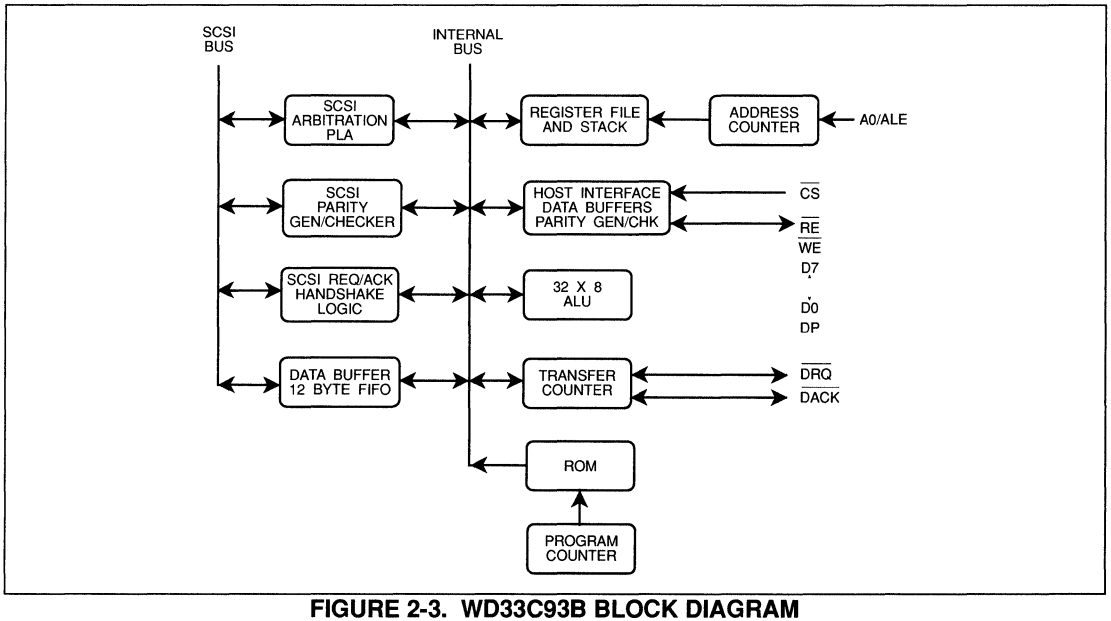


FIGURE 2-3. WD33C93B BLOCK DIAGRAM

3.0 WD33C93B REGISTERS

A0	R/W	REGISTER ACCESSED		ADDRESS (HEX)
0	R	Auxiliary Status Register		XX
0	W	Address Register		XX
1	R/W	Own ID Register	/CDB Size	00
1	R/W	Control Register		01
1	R/W	Timeout Period Register		02
1	R/W	Total Sectors Register	/CDB 1st	03
1	R/W	Total Heads Register	/CDB 2nd	04
1	R/W	Total Cylinders Register (MSB)	/CDB 3rd	05
1	R/W	Total Cylinders Register (LSB)	/CDB 4th	06
1	R/W	Logical Address (MSB)	/CDB 5th	07
1	R/W	Logical Address (2nd)	/CDB 6th	08
1	R/W	Logical Address (3rd)	/CDB 7th	09
1	R/W	Logical Address (LSB)	/CDB 8th	0A
1	R/W	Sector Number Register	/CDB 9th	0B
1	R/W	Head Number Register	/CDB 10th	0C
1	R/W	Cylinder Number (MSB) Register	/CDB 11th	0D
1	R/W	Cylinder Number (MSB) Register	/CDB 12th	0E
1	R/W	Target LUN Register		0F
1	R/W	Command Phase Register		10
1	R/W	Synchronous Transfer Register		11
1	R/W	Transfer Count Register (MSB)		12
1	R/W	Transfer Count Register (2nd Byte)		13
1	R/W	Transfer Count Register (LSB)		14
1	R/W	Destination ID Register		15
1	R/W	Source ID Register		16
1	R	SCSI Status Register		17
1	R/W	Command Register		18
1	R/W	Data Register		19
1	R/W	Queue Tag Register		1A

NOTE: 1. All unused bits of a defined register are reserved and must be zero.
2. Reading an undefined or unavailable register results in an all-ones data bus output.
3. Register addresses are determined by the Address Register bits AR7 through AR0.
4. When using a multiplexed address/data bus with ALE, the A0 pin is ignored, and the Address Register is loaded with ALE. In this mode, the Auxiliary Status Register is mapped at 1F hex.
5. See Section 3.2 for a description of how reset affects the internal registers.

TABLE 3-1. REGISTER MAP

3.1 REGISTER DESCRIPTIONS

3.1.1 Auxiliary Status Register

The Auxiliary Status Register, a read-only register, contains general status information not directly associated with the interrupt condition. The host may access the Auxiliary Status Register at any time except during DMA accesses. (DACK asserted in DMA/Burst mode or RCS asserted in WD bus mode).

7	6	5	4	3	2	1	0
INT	LCI	BSY	CIP	O	FFE	PE	DBR

Bit 0DBR-DATA BUFFER READY

Data Buffer Ready indicates to the processor whether or not the Data Register is available for reading or writing. During a Send command or a Transfer Info command which transmits data over the SCSI bus, the 33C93B sets this bit when ready to take a byte from the host; it resets this bit when the processor writes the byte to the DATA register. During a Receive command or a Transfer Info command which receives data over the SCSI bus, the 33C93B sets DBR when it receives a byte and resets DBR when the processor reads the byte from the DATA register.

Bit 1PE-PARITY ERROR

Parity Error status indicates that the 33C93B received a byte with even parity during a transfer. SCSI parity checking is always enabled; host parity checking is enabled via the EHP bit in the OWN ID register Detection of a parity error will set the PE status bit regardless of the state of the HHP or HSP bits in the CONTRO register. Issuing a command clears the PE bit.

Bit 2FFE -FIFO FULL/EMPTY

FIFO Full/Empty indicates when the FIFO is full or empty depending on the direction of the transfer. (see Section 3.1.22)

Bit 4CIP -COMMAND IN PROGRESS

Command In Progress indicates that the 33C93B is interpreting the last command entered into the Command Register which is therefore unavailable.

Bit 5BSY-BUSY

Busy indicates that a Level II command is currently executing, so the host may only access the Command Register (when CIP = 0),the Data Register, and the Auxiliary Status Register. When this bit is set, the host should not issue a Level II command.

Bit 6 LCI -LAST COMMAND IGNORED

Last Command Ignored indicates that the 33C93B ignored a command because the host issued it just prior to or concurrent with a pending interrupt.

Bit 7 INT-INTERRUPT PENDING

Interrupt Pending reflects the state of the INTRQ pin. When set, the host should read the SCSI Status Register to clear INTRQ prior to issuing any commands.

3.1.2 Address Register

The Address Register, a write-only register, holds the address of the register to be accessed. Registers in the 33C93B may be accessed in one of two ways:

- Direct addressing (multiplexed address/data busses). In this mode, the falling edge of the ALE signal latches the contents of the host data bus into the ADDRESS register. The CS and WE or RE signals typically follow to access the selected register. When using direct addressing, the A0 pin should be connected to ground, and the Auxiliary Status Register is located at address 1F hex.
- Indirect addressing (separate address/data busses). This method, enabled by tying ALE to ground, requires two separate cycles for a register access. The first cycle loads the desired address into the Address Register by writing (CS and WE asserted) to the 33C93B with A0=0.The second cycle, with A0=1, then reads (CS and RE asserted) or writes (CS and WE asserted) the selected register. Every cycle with A0=1 increments the ADDRESS register except when accessing the Data or Command Registers. In indirect addressing, the Auxiliary Status Register is accessed by performing a read (CS and RE asserted) with A0=0.

3.1.3 Own ID/CDB Size Register

The Own ID/CDB Size Register, in its first mode, contains information which the Soft Reset command uses to configure the device. Following a hardware reset, the host, before issuing any other command, must initialize this register and issue the Reset command to set the clock divisor and the SCSI bus ID of the device and to enable various sets of features and host bus parity checking.

In the second mode, bits 3-0 of this register specify the SCSI CDB size if the command group is unknown (i.e. not a group 0, group 1, or group 5 SCSI command) to the 33C93B during the Select-and-Transfer and Wait-for-Select commands. This mode is enabled only when advanced features (see Section 4.3.1) have been selected.

7	6	5	4	3	2	1	0
FS1	FS0	RAF	EHP	EAF	ID2	ID1	ID0

Bit 0-2IDn- SCSI ID BITS

SCSI ID Bits 0-2 set the SCSI bus ID that the 33C93B uses during arbitration and selection.

Bit 3EAF-ENABLE ADVANCED FEATURES

Enable Advanced Features, when set, enables functions described in section 4.3.1.

Bit 4 EHP-ENABLE HOST PARITY

Enable Host Parity enables odd parity checking on the host bus. The PE bit in the Auxiliary Status Register will then also indicate parity errors detected on the host bus, and the HHP bit in the Control Register will have effect during transfers. When host parity is disabled, the PE bit is not set when a parity error occurs on the host bus,and the HHP bit must be set to zero. Note: Parity is always generated on the host data parity bit (DP), regardless of the state of this bit.

Bit 5 RAF-REALLY ADVANCED FEATURES

Really Advanced Features, when set, enables features described in section 4.3.1.

Bit 6-7 FSn-FREQUENCY SELECT

Frequency Select 0-1 select the divisor that is applied to the input clock. The divided clock is used for data transfer timing and for SCSI bus arbitration timing. The table below shows input clock frequency ranges and their corresponding divisors. An incorrect divisor for the input clock may result in violation of SCSI bus timing specifications.

INPUT CLOCK FREQUENCY (MHz)	FS1	FS0	RESULTING DIVISOR
8-10	0	0	2
12-15	0	1	3
16-20	1	0	4
XX	1	1	Undefined

Note that a clock rate between 10 MHz and 12 MHz should not be used, as the resulting SCSI bus clear delay may violate SCSI specifications. The formula for computing the maximum SCSI data transfer rate is given in Section 6.

3.1.4 Control Register

The Control Register consists of option bits which affect response to parity errors and to the SCSI attention condition, suppress interrupts, allow command chaining, and select the mode of DMA transfer.

7	6	5	4	3	2	1	0
DM2	DM1	DM0	HHP	EDI	IDI	HA	HSP

Bit 0 HSP-HALT on SCSI PARITY ERROR

The Halt on SCSI Parity Error bit enables the 33C93B to terminate a Receive or Transfer Info command if a parity error occurs on an incoming SCSI data byte. Asynchronous transfers check parity on every byte; synchronous data transfers check parity on 4096-byte boundaries in most cases. In the initiator role, the 33C93B responds to a SCSI parity error by leaving the ACK pin asserted to inhibit any additional data transfers (REQs) by the target and to facilitate error handling with the target. If Immediate Halts are enabled, a SCSI parity error during a synchronous Receive or Reselect-and-Receive command will abort the transfer before the 4096-byte boundary.

Bit 1 HA-HALT on ATTENTION

The Halt on Attention bit (target mode only) enables the 33C93B to terminate a Send or Receive command if the initiator asserts ATN. The 33C93B normally tests for the ATN condition before the start of a data transfer, on 4096 byte boundaries, and after the end of the transfer. If the Immediate Halt feature is enabled, an Abort command will be issued upon recognition of the ATN condition. These rules apply to both synchronous and asynchronous transfers.

Bit 2 IDI-INTERMEDIATE DISCONNECT INTERRUPT

The Intermediate Disconnect Interrupt bit, when set in the initiator role, causes the 33C93B to terminate a Select-and-Transfer command and generate an 85 hex interrupt upon a proper target disconnect. When this bit is reset, a valid disconnect will not cause the 33C93B to generate an interrupt, and command execution proceeds. This feature, when used with the Resume SAT command, provides support for overlapped SCSI operations. In the target role, the IDI bit selects combination command execution options. Refer to Section 4 for more details.

Bit 3EDI-ENDING DISCONNECT INTERRUPT

The Ending Disconnect Interrupt bit, when set, delays the 16 hex interrupt which normally follows receipt of the Command-Complete message during a Select-and-Transfer command until after the target disconnects, replacing the 85 hex interrupt. This bit also enables chaining between certain target-role combination commands to reduce host system overhead. Refer to Section 4 for more details.

Bit 4HHP-HALT on HOST PARITY ERROR

The Halt on Host Parity Error bit allows the 33C93B to terminate a Send or Transfer command if a parity error occurs on an incoming host data byte. The 33C93B checks for host parity errors according to the sames rules it uses when checking for SCSI parity errors. However, a host parity error will not leave the ACK signal asserted.

Bit 5-7 DMx-DMA MODE SELECT

The DMA Mode Select bits 2-0 select the host bus transfer mode to be used during a Data phase. The following table describes the different DMA modes and specifies the state of these bits to select each mode:

DM2	DM1	DM0	DMA MODE SELECTED
0	0	0	Polled I/O Mode or no DMA enabled. The host must poll for DBR in the Auxiliary Status Register and then, depending on the direction of the transfer, read or write the DATA register.
0	0	1	Burst Mode or demand-mode DMA. In this mode, the DRQ signal will remain active so long as data or space exists in the internal FIFO to allow the transfer to continue. The DMA controller responds by asserting DACK and pulsing RE or WE to transfer the data.
0	1	0	WD-Bus Mode or Direct Buffer Access (DBA) mode. In this mode, the 33C93B acts as a bus master, and all data access signals reverse their directions. The DRQ pin becomes the DRQ input, which when high, enables the 33C93B to drive the buffer control signals. The DACK pin becomes the RCS output and serves as a chip select for the buffer. The RE and WE pins become outputs which drive the read and write functions of the RAM buffer. Transfers will continue in a burst manner until the transfer is complete or until the external buffer logic pauses the transfer by negating the DRQ signal. One transfer may occur after DRQ drops and then the DACK, RE, and WE signals will tri-state.
1	0	0	DMA MODE or Single-byte DMA. In this mode,a DRQ/DACK handshake occurs for each byte.The DMA controller transfers the byte by asserting WE or RE while asserting DACK.

3.1.5 Timeout Period Register

The Timeout Period Register stores a user-selected, 8-bit value which determines the timeout period for selection and reselection attempts. The timeout period specifies how long the 33C93B will wait for a response (i.e. assertion of the BSY signal) after it has begun the Selection phase (asserted SEL and negated BSY) before terminating the command. Loading this register with zero disables the timeout feature. For a desired timeout period, the register value depends upon the input clock frequency, as shown in the following equation:

$$\text{register value} = \frac{\text{Tper} * \text{Ficlk}}{80}$$

where Tper = the desired timeout period in milliseconds; Ficlk = the input clock frequency at the MCK pin in megahertz (with no divisor applied).

The constant '80' scales the units of the equation, as it is based on the internal timeout cycle time. The user should round the resulting 'register value' up to the next integral value to ensure that the minimum timeout requirement is met.

3.1.6 Command Descriptor Block Registers

The Command Descriptor Block Registers hold the SCSI command bytes to be sent during Command phase of a Select-and-Transfer command and the command bytes received during the Command phase of a Wait-for-Select-and-Receive command.

The Send-Status-and-Command-Complete command uses the contents of the CDB11 register as the returned status and determines the type of the Command-Complete message to send from the contents of the CDB12 register. Bit 0 of CDB12 selects whether the command sends a simple Command-Complete message bit 0=0) or a Linked-Command-Complete message (bit 0=1). In the latter case, bit 1 of CDB12, the FLAG bit, specifies whether a 0A hex (FLAG=0) or a 0B hex (FLAG=1) message is sent.

3.1.7 Total Sectors Register

The Total Sectors Register stores an 8-bit value specifying the total number of sectors per track for the Translate Address command.

3.1.8 Total Heads Register

The Total Heads Register stores an 8-bit value specifying the total number of heads for the Translate Address command.

3.1.9 Total Cylinders Register

The Total Cylinders Register stores a 16-bit value specifying the total number of cylinders for the Translate Address command.

3.1.10 Logical Address Register

The Logical Address Register stores the 32-bit logical address to be translated by the Translate Address command.

3.1.11 Sector Number Register

The Sector Number Register will contain the resulting physical sector number following a Translate Address command.

3.1.12 Head Number Register

The Head Number Register contains the resulting head number following a Translate Address command.

If the host desires the 33C93B to compensate for spare sectors on the disk, this register should contain the number of spare sectors per cylinder prior to issuing the Translate Address command. A value of zero indicates no compensation. With compensation, the maximum number of cylinders allowed is 4096, and the maximum number of heads is 15.

3.1.13 Cylinder Number Register

The Cylinder Number Register contains a 16-bit value specifying the resulting cylinder number following a Translate Address command.

If the host desires the 33C93B to compensate for spare sectors on the disk, the Translate Address command expects this register to contain the number of sectors per cylinder after allowing for the spares, i.e. (sectors/track * heads - spares/cylinders).

3.1.14 Target LUN Register

The Target LUN Register holds the Logical Unit Number (LUN) and other target status information during various 33C93B commands and sequences.

The Select-and-Transfer commands use the contents of this register and the Source ID Register to generate and check Identify messages. In addition, these commands also store the returned status byte from the target in this register. For proper operation of the Select-and-Transfer commands, the host should not set the TLV bit in this register.

In advanced mode, the Select-and-Transfer commands, in the event of an unexpected reselection, place the logical unit number (TRN=0) or the target routine number (TRN=1) of a reselecting target in this register. The TLV and DOK bits will be zero.

The Wait-for-Select-and-Receive command places a copy of a received Identify message in this register. If the TLV bit is zero, the initiator did not send a valid Identify message. If the TLV bit is one, the initiator sent a valid Identify message, and the DOK bit will then indicate whether or not the initiator has enabled disconnects. The Wait-for-Select-and-Receive command will accept an Identify message with the TRN bit set only if the host issues the command with the SBT bit in the Command Register set.

The Reselect-and-Transfer commands use only the LUN portion and the TRN bit of this register to generate the Identify message. The TLV and DOK bits are not used.

7	6	5	4	3	2	1	0
TLV	DOK	TRN	0	0	TL2	TL1	TL0

3.1.15 Command Phase Register

The Command Phase Register indicates which phases of a combination command have completed. Thus, if the command has terminated abnormally, the processor can read this register to determine the cause of the termination and decide how to respond to it.

When resuming a combination command, the contents of this register specify from which point to restart the command. Refer to the description of the specific commands for details regarding the various command phases and resume values.

7	6	5	4	3	2	1	0
0	CP6	CP5	CP4	CP3	CP2	CP1	CP0

3.1.16 Synchronous Transfer Register

The contents of the Synchronous Transfer Register specify the maximum transfer rate and the transfer mode for a SCSI data phase.

For information phases other than a Data phase or when the selected offset is zero (OF3=OF2=OF1=OF0=0), the 33C93B performs asynchronous transfers. A non-zero offset value, which should be twelve or less, selects synchronous data transfers and determines the effective FIFO depth. This value is typically determined through negotiation (as defined in the SCSI standard) with the other SCSI device.

The Transfer Period control bits select the minimum transfer period for both synchronous and asynchronous SCSI data transfers and, in WD-Bus mode, the transfer period and the width of the RE/WE strobes for host transfers; for non-data transfers, the transfer period defaults to six periods. The period is defined in terms of the internal clock cycle time, which depends upon the input clock, the divisor selected in the Own ID Register, and the setting of the FSS bit.

The FSS bit has effect only when operating with an input clock frequency of 16-20 MHz, i.e. the divisor set to 4. Setting this bit enables Fast SCSI transfers, doubling the maximum transfer rate for synchronous transfers. For example, with a 20 MHz input clock and a transfer period of 2, the normal maximum transfer rate (FSS=0) would be 5 MB/s; the Fast SCSI transfer rate (FSS=1) would be twice this value or 10 MB/s. The FSS bit does not affect the rate of asynchronous transfers.

7	6	5	4	3	2	1	0
FSS	TP2	TP1	TP0	OF3	OF2	OF1	OF0

Bit 0-3 OFx - OFFSET

The OFFSET bits specifies the desired offset according to the following table:

3	2	1	0	SELECTED OFFSET
0	0	0	0	0 *
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	Undefined
1	1	1	X	Undefined

* Asynchronous data phase transfers.

6	5	4	SCSI/WD-BUS TRANSFER PERIOD	(SCSI REQ/ACK Synchronous Pulse Width and WD-BUS RE/WE Pulse Width
0	0	X	8 cycles	(4 cycles)
0	1	0	2 cycles	(1 cycle)
0	1	1	3 cycles	(1 cycle)
1	0	0	4 cycles	(2 cycles)
1	0	1	5 cycles	(3 cycles)
1	1	0	6 cycles	(4 cycles)
1	1	1	7 cycles	(4 cycles)

The 'cycle' referred to above is the period of the internal data transfer clock. For asynchronous transfers or for synchronous transfer when the input clock frequency is less than 16 MHz, it is calculated as follows:

$$\text{CYCLE } (\mu s) = \frac{\text{DIVISOR (from OWN ID)}}{2 * \text{INPUT CLOCK FREQUENCY (MHz)}}$$

For synchronous transfers when the input clock frequency is 16 MHz or greater, the cycle time is calculated as follows:

$$\text{CYCLE } (\mu s) = \frac{2}{(\text{FSS}+1) * \text{INPUT CLOCK FREQUENCY (MHz)}}$$

24

Bit 4-6TPx - TRANSFER PERIOD

The Transfer Period bits select the desired desired transfer period according to the following table:

Bit 7 FSS - FAST SCSI SELECT

The Fast SCSI Select bit under the conditions mentioned above enables the doubling of the internal clock frequency resulting in a synchronous transfer rate up to 10 MB/s.

3.1.17 Transfer Count Register

The Transfer Count Register, a 24-bit register, stores a preset value for the internal transfer counter. A Send, Receive, or Transfer Info command causes the 33C93B to load this preset value into the internal transfer counter, which then decrements as each data byte is transferred over the SCSI bus and causes a "successful completion" interrupt when it reaches zero.

Loading the Transfer Count Register with zeros prior to issuing these command or issuing the command with the Single-byte Transfer bit set in the Command Register disables the counter function. If the counter is disabled, the Send, Receive, or Transfer Info command will complete when a single byte has been transferred.

In combination commands, this register specifies the number of bytes to be transferred during a Data phase. A zero value indicates the lack of a Data phase.

After the completion of any successful transfer, including commands issued in Single Byte Transfer mode, the Transfer Count Register will be zero.

When a transfer halts because of an error condition, a SCSI bus phase change, or an abort, the Transfer Count Register will contain the number of bytes NOT successfully transferred over the SCSI bus, including any bytes present in the FIFO at the time of the interruption. The FIFO clearing process may cause the Transfer Count Register to differ with the host DMA controller count, because some bytes may have been transferred into the FIFO but not to the SCSI bus.

3.1.18 Destination ID Register

The Destination ID Register stores the encoded SCSI bus ID of the device to be selected or reselected when a Select or Reselect command is issued. This register also contains control bits that affect the operation of certain combination commands.

7	6	5	4	3	2	1	0
SCC	DPD	DF	TG1	TG0	DI2	DI1	DI0

Bit 2-0DIx - DESTINATION ID

Destination ID bits 2-0 specify which SCSI device to select or reselect.

Bit 3-4TGx - TAG MESSAGE

The Tag Message bits select which tag message code to send during Select-and-Transfer and identify which tag message code was received by the Wait-for-Select-and-Receive command. In addition, the Reselect-and-Transfer commands send a Simple-Queue Tag message following the Identify message if either of these bits are set.

4	3	MESSAGE RECEIVED OR SENT
0	0	No Message
0	1	Simple Queue Tag (20H)
1	0	Head Of Queue Tag (21H)
1	1	Ordered Queue Tag (22H)

Bit 5DF -DISABLE FEATURE

Disable Feature, when set, disables Data phase direction checking in advanced mode and inhibits the normally automatic link from Send-Status-and-Command-Complete to the command fetch portion of Wait-for-Select-and-Receive when a Linked-Command-Complete message is sent.

Bit 6 DPD - DATA PHASE DIRECTION

Data Phase Direction, when advanced features are enabled (see Section 4.3.1), specifies the expected direction of the SCSI Data phase of a Select-and-Transfer command. When this bit is zero, the expected direction is out (to the target), and when this bit is one, the expected direction is in (from the target). An unexpected data phase error will occur if the actual direction does not match the setting of this bit.

Bit 7 SCC - SELECT COMMAND CHAIN

Select Command Chain selects which command will follow a Reselect-and-Transfer command when chaining is enabled (EDI=1). When this bit is zero, a Send-Status-and-Command-Complete command will follow; when this bit is one, a Send-Disconnect-Message command follows.

3.1.19 Source ID Register

The SOURCE ID register is used to report the SCSI bus ID of the device that has selected or reselected the 33C93B. It also contains bits that enable and control response to selection and reselection.

7	6	5	4	3	2	1	0
ER	ES	DSP	0	SIV	SI2	SI1	SI0

Bit 2-0SIx - SOURCE ID

Source ID Bits 2-0, valid only if the SIV bit is set, indicate the SCSI bus ID of the device that selected or reselected the 33C93B.

Bit 3SIV - SOURCE ID VALID

Source ID Valid is set to one when the 33C93B is selected or reselected and the other SCSI bus device asserted its own bus ID bit during the Selection/Reselection phase. This bit is zero if only the bus ID bit of the 33C93B was asserted.

Bit 5DSP DISABLE SELECT PARITY

Disable Select Parity, when set, causes the 33C93B to ignore the bus parity when responding to selection or reselection.

Bit 6 ES - ENABLE SELECTION

Enable Selection, when set, allows the 33C93B to respond to selection by another device on the SCSI bus.

Bit 7ER - ENABLE RESELECTION

Enable Reselection, when set, allows the 33C93B to respond to re-selection by another device on the SCSI bus.

3.1.20 SCSI Status Register

The SCSI Status Register, a read-only register, holds a value which indicates the cause of the most recent INTRQ assertion. The 33C93B asserts INTRQ whenever a condition occurs that requires intervention by the host. For example,

- the 33C93B has been reset;
- the command completed successfully;
- the bus phase changed;
- an error occurred.

After assertion of INTRQ, the contents of this register will not change until the host reads the register or until the 33C93B has been reset.

7	6	5	4	3	2	1	0
SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Bit 0-3SSx - SCSI STATUS

SCSI Status bits 0-3 are status qualifiers with meanings that depend upon the upper (4-7) status bits.

Bit 4-7SSx - SCSI STATUS

SCSI Status bits 4-7 define the type of interrupt that occurred. The following table describes the various types:

STATUS	CODE	GROUP MEANING
0000	xxxx	The 33C93B is in a reset state.
0001	xxxx	A 33C93B command has completed successfully.
0010	xxxx	A 33C93B command has paused or was aborted.
0100	xxxx	A 33C93B command has been terminated prematurely due to an error or other unexpected condition.
1000	xxxx	An event on the SCSI bus requires service.

All other Status Code groups are currently not used and are reserved for future use.

In the following tables, the 'STATE' column indicates the state---Disconnected, Target, or Initiator---from which the Status Code can occur. The MCI field refers to the signals that define a SCSI bus information transfer phase: MSG, C/D, and I/O. A bit set to one indicates that the signal is asserted on the SCSI bus; a zero indicates negation. Whenever one of these Status Codes occurs, the REQ signal is asserted on the SCSI bus. The table on the right summarizes the meaning of the MCI field:

MCI CODE	MEANING
000	Data Out phase
001	Data In phase
010	Command phase
011	Status phase
100	Unspecified Info Out phase
101	Unspecified Info In phase
110	Message Out phase
111	Message In phase

STATUS	CODE	STATE	SPECIFIC MEANING
0000	0000	DTI	33C93 Reset. The device has been hard reset, or a Reset command has executed successfully with no advanced features enabled. The new state of the 33C93B is disconnected.
0000	0001	DTI	33C93B Reset. The device has successfully completed a Reset command with advanced features enabled. The new state of the 33C93B is disconnected.

TABLE 3-2. RESET STATE INTERRUPTS

STATUS	CODE	STATE	SPECIFIC MEANING
0001	0000	D	A Reselect command completed successfully. The new state of the 33C93B is connected as a target.
0001	0001	D	A Select command completed successfully. The new state of the 33C93B is connected as an initiator.
0001	0010	-	Reserved for future use.
0001	0011	T	A Receive, Send, Reselect-and-Transfer, Wait- for-Select-and-Receive, Send-Status-and-Command-Complete, or Send-Disconnect-Message command completed successfully (ATN is not asserted).
0001	0100	T	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, or Send-Status-and-Command-Complete command completed successfully (ATN is asserted).
0001	0101	DT	A Translate Address command completed successfully.
0001	0110	I	A Select-and-Transfer command completed successfully.
0001	0111	-	Reserved for future use.
0001	1MCI	I	A Transfer Info (non-Message-In phase) command completed successfully. MCI defines the new information type (SCSI bus phase) requested.

TABLE 3-3. SUCCESSFUL COMPLETION INTERRUPTS

STATUS	CODE	STATE	SPECIFIC MEANING
0010	0000	I	A Transfer Info (Message In phase) command has paused with ACK asserted, giving the host the opportunity to reject the message.
0010	0001	I	A Save-Data-Pointer message was received during a Select-and-Transfer command. The host should save its current data buffer pointer.
0010	0010	D	A Select, Reselect, or Wait-for-Select-and-Receive command aborted.
0010	0011	T	A Receive or Send command aborted, or a Wait-for-Select-and-Receive detected an error in the Identify message. (ATN is not asserted).
0010	0100	T	A command aborted or halted due to assertion of ATN, or a Wait-for-Select-and-Receive detected an error in the Identify message. (ATN is asserted).
0010	0101	T	A transfer has aborted because of a violation of the data transfer protocol, possibly corrupting the data.
0010	0110	I	An I/O process with a queue tag which does not match the value in the Queue Tag Register reselected the 33C93B. ACK has been left asserted.
0010	0111	I	A target whose SCSI bus ID does not match the ID in the Destination ID Register reselected the 33C93B or the following Identify message did not match the LUN in the Target LUN Register. ACK has been left asserted following the Identify message, and the bus ID and LUN of the reselecting target are available in the Source ID and Target LUN Registers. This status only occurs when executing a Select-and-Transfer in advanced mode.
0010	1MCI	-	Reserved for future use.

TABLE 3-4. PAUSED OR ABORTED INTERRUPTS

STATUS	CODE	STATE	SPECIFIC MEANING
0100	0000	DTI	An invalid command was issued.
0100	0001	TI	An unexpected disconnect occurred. The new state of the 33C93B is disconnected.
0100	0010	D	A timeout occurred during a Select or Reselect command. The state of the 33C93B is disconnected.
0100	0011	TI	A parity error caused a command to terminate ($\overline{ATN}$ is not asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0100	T	A parity error caused a command to terminate ($\overline{ATN}$ is asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0101	DT	A Translate Address command did not complete successfully. The Logical Address exceeded the disk boundaries.
0100	0110	I	A target whose SCSI bus device ID does not match the bus ID set in the Destination ID Register has reselected the 33C93B during a Select-and-Transfer command. This interrupt occurs when the 33C93B is not in advanced mode. The state of the 33C93B is connected as an initiator.
0100	0111	I	A status byte with a parity error was received during Select-and-Transfer.
0100	1MCI	I	An unexpected information phase was requested. MCI defines the SCSI bus phase requested. This interrupt typically occurs when the phase changes before the Transfer Count reaches zero during a Transfer Info command or when an unexpected phase sequence occurs during a Select-and-Transfer command.

TABLE 3-5. TERMINATED INTERRUPTS

STATUS	CODE	STATE	SPECIFIC MEANING
1000	0000	D	The 33C93B has been reselected. The new state of the 33C93B is connected as an initiator.
1000	0001	D	The 33C93B has been reselected in advanced mode. The Identify message from the target must be read from the DATA register. The ACK signal is asserted. The new state of the 33C93B is connected as an initiator.
1000	0010	D	The 33C93B has been selected ($\overline{ATN}$ was not asserted). The new state of the 33C93B is connected as a target.
1000	0011	D	The 33C93B has been selected ($\overline{ATN}$ was asserted). The new state of the 33C93B is connected as a target.
1000	0100	T	The ATN- signal has been asserted.
1000	0101	TI	The target has disconnected. The new state of the 33C93B is disconnected.
1000	0110	-	Reserved for future use.
1000	0111	T	The Wait-for-Select-and-Receive command has paused because the first byte of the incoming CDB is not of a known command group. The host can examine the CDB1 register to determine from the opcode the number of command bytes expected. The new state of the 33C93B is connected as a target. (Advanced mode only)
1000	1MCI	I	The REQ signal has been asserted while the 33C93B was in an idle initiator state. The information phase type should be examined. MCI defines the information phase (SCSI bus phase) requested.

TABLE 3-6. SERVICE REQUIRED INTERRUPTS

24

3.1.21 Command Register

The Command Register is used to issue the 33C93B commands. The host should never write to this register when the CIP or INT bits (in auxiliary status) are set and should never issue a Level II command when the BSY bit is set.

The Single-byte Transfer (SBT) bit in the Command Register affects the information transfer commands by disabling the Transfer Count Register and specifying that only one byte is to be transferred. The previous contents of the Transfer Count Register are not preserved.

The SBT bit also affects the Wait-for-Select-and-Receive command. Normally, this command does not accept as valid an Identify message with the LUNTAR bit (bit 5) set, which occurs when the initiator wishes to communicate with a target routine. Issuing the command with the SBT bit set allows it to accept an Identify message for a target routine.

Refer to the Commands section for a description of the commands and their corresponding command codes.

7	6	5	4	3	2	1	0
SBT	CC6	CC5	CC4	CC3	CC2	CC1	CC0

3.1.22 Data Register

The Data Register provides an interface between the internal twelve byte FIFO and the host. During any type of information phase, the host may access this register with the processor, and during a SCSI Data phase, the host may also access this register through the DMA/WD interface.

The processor, except in one case, should only access the Data Register when the DBR bit in the Auxiliary Status Register is true. The exception occurs when the 33C93B is reselected while operating in advanced mode: the processor must retrieve the Identify message from the target by reading the Data Register.

The FFE bit in the Auxiliary Status Register enables the host to avoid polling DBR in some cases. This bit, when the host writes to the FIFO, acts as a FIFO empty indicator; thus, when set, the host can safely write up to eleven bytes to the FIFO without polling for DBR between each write. Similarly, when the transfer direction is to the host, the FFE bit indicates the FIFO full condition, and the processor can safely read twelve bytes from the FIFO without checking for DBR before each read. In both cases, the host should consider the FFE bit valid only when DBR is set.

Two exceptions do exist, however, both when writing to the Data Register. First, after the initial setting of the FFE and DBR bits in response to a Transfer Info or Send command, the host may write twelve bytes to the FIFO without causing a FIFO overrun. Second, because the 33C93B splits a Transfer Info command into two separate transfers when responding to a message out phase, the host must not write the last message byte to the Data Register until the 33C93B specifically requests that byte. For instance, if the host wishes to send a (five-byte) Synchronous Data Transfer Request message, the first set of writes should contain only the first four bytes of the message. The host must then poll for DBR before writing the final byte.

The processor normally should not access the Data Register during a Data phase unless the host has selected polled I/O mode by setting all of the DMA Mode Select bits in the Control Register to zero. In exceptional cases, such as aborting a transfer, the host may wish to switch to polled I/O accesses. In this case, the processor may access the DATA register but must guarantee that the DMA interface is inactive, i.e. DACK inactive in the DMA and Burst DMA modes and RCS deasserted in WD Bus mode.

3.1.23 Queue Tag Register

The Queue Tag Register holds the second byte of the Tag messages associated with the Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive commands.

The Select-and-Transfer and Reselect-and-Transfer commands send the contents of this register as the second byte of the Tag message during the Tag message out phase.

The Select-and-Transfer and Wait-for-Select-and-Receive commands place the received queue tag byte into this register during the Tag message in phase. The Select-and-Transfer commands, furthermore, compare the received byte with the previous contents of the register and generate an interrupt in the case of a mismatch.

3.2 RESET CONDITIONS

3.2.1 Hardware Reset

A hard reset, caused by assertion of the $\overline{MR}$ signal, will result in the following conditions:

- The Auxiliary Status Register is reset to zero. The INT bit (and the INTRQ pin) is set to one when the hardware reset completes.
- The Own ID Register is reset to zero.
- Advanced mode is disabled.
- The ES, ER, and DSP bits in the SOURCE ID register are reset to zero.
- The SCSI Status Register is reset to zero.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The internal clock divider circuit is set to divide by two.

The hard reset does NOT affect the following host accessible registers:

- Registers 01 hex through 15 hex;
- Source ID (16 hex) Register bits 0-3;
- Command Register (18 hex);

Note: The SCSI Soft Reset may be implemented by using the SCSI bus reset signal to reset the 33C93B (for example, OR the host power on reset signal with the received SCSI bus reset ($\overline{RST}$) signal). The host may examine the registers that are not affected by the $\overline{MR}$ signal to recover from the SCSI reset condition.

3.2.2 Software Reset

A soft reset, caused by executing the Reset command, will result in the following conditions:

- The DBR bit in the Auxiliary Status Register is reset to zero. The INT bit (and INTRQ pin) is set to one when the Reset command is complete.
- All SCSI bus signals are reset to the negated state.
- The internal FIFO, internal transfer counter (not the Host Accessible Register), offsets, and state machines are cleared.
- The Own ID Register is interpreted and the clock divisor, host parity, and operating mode are configured.
- Registers 01 hex through 16 hex are reset to zero. The Command Register (18 hex) is also reset to zero.
- The SCSI Status Register is set as commanded by the EAF bit in the Own ID Register.

4.0 COMMANDS

4.1 COMMAND LIST

COMMAND CODE (HEX)	COMMAND	VALID	LEVEL
00	Reset	D, T, I	I
01	Abort	D, T	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	T, I	I
05	Reselect	D	II
06	Select-with-ATN	D	II
07	Select-without-ATN	D	II
08	Select-with-ATN-and-Transfer	D, I	II
09	Select-without-ATN-and-Transfer	D, I	II
0A	Reselect-and-Receive-Data	D, T	II
0B	Reselect-and-Send-Data	D, T	II
0C	Wait-for-Select-and-Receive	D, T	II
0D	Send-Status-and-Command-Complete	T	II
0E	Send-Disconnect-Message	T	II
0F	Set IDI	D, T, I	I
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
18	Translate Address	D, T	II
20	Transfer Info	I	II

33C93B States:
D = Disconnected
T = Connected as a target
I = Connected as an initiator

Command Levels:
I = Level I command
II = Level II command

TABLE 4-1. COMMAND LIST

4.2 33C93B COMMAND TYPES

The 33C93B command set consists of two types of commands: Level I and Level II commands. Level I commands, except for the Reset and Abort commands, do not generate interrupts upon their completion; Level II commands always terminate with an interrupt. The host may issue a Level I command while a Level II command is executing. Issuing a Level II command while another Level II command is executing will cause unpredictable behavior of thepart.

The 33C93B operates in one of three "states" at any one time: disconnected, connected as a target, or connected as an initiator. In each state, the 33C93B recognizes only certain commands as valid, as indicated in the command list above. An attempt to issue a Level II command invalid for the present 33C93B state will cause an "invalid command" interrupt. Level I commands issued in invalid states will be ignored.

There are two types of Level II commands. 'Simple' Level II commands perform a single operation (e.g. selection) or single phase (e.g. Command phase). 'Combination' Level II commands combine multiple phases into a single 33C93B command to minimize interrupt overhead.

The initiator combination commands expect the target to follow common SCSI bus phase sequences. Any deviation causes an interrupt.

The EDI and IDI bits in the Control Register and the SCC bit in the Destination ID Register enable and control chaining of target combinations command. Linking commands further decreases interrupt overhead by creating longer phase sequences. When using command chaining, the host must initialize all commands in the chain prior to starting the sequence.

4.3 33C93B SPECIFIC FEATURES

The 33C93B incorporates two sets of features, both of which cause it to be incompatible with the original 33C93 design and one which causes it to be incompatible with the 33C93A device. Both the 33C93A and 33C93B implement the 'advanced mode' features. Both devices, moreover, implement two features included in the 'really advanced' set of functions; however, in this mode, the 33C93B also generates additional interrupts, described below, making it incompatible with the 33C93A.

Upon completion of a hardware reset, both sets of features are disabled. The host enables them by soft resetting the 33C93B with the EAF and RAF bits in the Own ID Register set appropriately. An advanced mode reset results in a 01 hex being loaded into the SCSI Status Register instead of the 00 hex which normally results from a reset. This difference gives the host a method to deduce that a 33C93B is installed as opposed to a 33C93.

4.3.1 Advanced Mode Features

Unexpected Reselection:
When in normal (33C93) mode, a reselection when idle (ER=1) or a reselection during a Select-and-Transfer command by an target whose ID does not match the one in the Destination ID Register causes an interrupt immediately after the reselection handshake finishes. In advanced mode, the 33C93B will continue to the Message In phase to fetch the Identify message. If the 33C93B was idle, the SCSI Status Register will be set to 81 hex, and the Identify message will be in the Data Register. If the 33C93B was executing a Select-and-Transfer command, the SCSI Status Register will be set to 27 hex, and the logical unit number will be in the Target LUN Register. In both cases, the SOURCE ID register will contain the SCSI bus ID of the reselecting target, and the ACK signal remains asserted so that the Identify message may be rejected if desired.

Any message other than a valid Identify message will result in an unexpected message in phase interrupt. If the unexpected reselection occurs during a Select-and-Transfer command, a parity error will cause an unexpected message in phase interrupt only if the halt-on-SCSI-parity-error feature is enabled. If reselected from an idle state, the 33C93B will halt on a parity error regardless of the setting of the HSP bit. The host can retrieve the byte with the Transfer Info command.

Unknown SCSI Command Groups:
The length of a SCSI Command Descriptor Block is determined by the group code, found in bits 7-5 of the first command byte. The SCSI standard (X3.131-1986) defines Group 0 (opcodes 00 to 1F hex), group 1 (opcodes 20 to 3F hex), and group 5 (opcodes A0 to BF hex) commands respectively as six, ten, and twelve byte commands. All other command groups are undefined by that standard. In normal mode, the 33C93B assumes a length of six bytes for these undefined groups when executing a Select-and-Transfer or Wait-for-Select-and-

Receive command. In advanced mode, the 33C93B behaves as follows:

- Select-and-Transfer: When sending a command from an unknown group, the host must load the expected command length into the CDB Size Register before issuing the Select-and-Transfer. The 33C93B uses this value to make sure the correct number of bytes are transferred in the Command phase.
- Wait-for-Select-and-Receive: When receiving the CDB from the initiator, the 33C93B examines the first CDB byte to determine the command group. An undefined group results in an interrupt with the SCSI Status Register set to 87 hex and the Command Phase Register set to 31 hex. The host may examine the byte, available in the CDB 1st Register, to determine the total command length, which it then places into the CDB Size Register, before resuming the Wait-for-Select-and-Receive command.

  After this interrupt, the 33C93B will only accept a Resume Wait-for-Select-and-Receive, Abort, Disconnect, or Reset command. All other commands are invalid. While the host processes the interrupt, the 33C93B continues to transfer the first six bytes of the SCSI command into its internal FIFO.

Data Phase Direction:
Normally during a Select-and-Transfer command, the target solely determines the direction of the Data phase. The 33C93B will not detect a mismatch between this direction and the one expected by the host and will proceed with the transfer. In advanced mode, the 33C93B compares the DPD bit in the Destination ID Register with the state of the I/O- signal on the SCSI bus. If the expected and actual directions do not match, an interrupt will occur with an 'unexpected phase' status in the SCSI Status Register. Setting the DF bit in the Destination ID Register disables this feature.

Microcode Revision:
The 33C93B will load the revision number of the microcode into the CDB1 register during the reset sequence when really advanced features are enabled.

Immediate Halt:
The 33C93B normally checks for parity errors during a synchronous transfer and for the attention condition during both asynchronous and synchronous transfer on 4096-byte boundaries. With really advanced features enabled, the 33C93B continuously checks for these conditions and upon detecting one issues an Abort command.

Protocol Error:
The 33C93B, if it detects a possible transfer corruption caused by noise on the REQ and ACK signals, will abort a Send or Receive command and generate a 25 hex interrupt. The detection scheme can not catch all possible failures due to the nature of the SCSI transfer protocols; however, this feature does provide some protection against data integrity faults.

Unexpected Bus Free Interrupts:
The 33C93B will generate either an 85 hex interrupt or a 41 hex interrupt in the event that a glitch on the SEL signal causes the device to disconnect from the SCSI bus.

4.4 LEVEL I COMMANDS

4.4.1 Reset (00 hex)

The Reset command initializes the 33C93B according to the contents of the Own ID Register and as described in the Reset Conditions section. The host may issue the Reset command while in any state, forcing the 33C93B into a disconnected state; any command executing at that time will terminate. Upon completion of the Reset command, the 33C93B will generate an interrupt with the SCSI Status Register containing a 00 hex or a 01 hex depending upon the contents of the Own ID Register at the time of the reset.

4.4.2 Abort (01 hex)

The Abort command is valid in the disconnected and connected-as-a-target states. The Abort command has different effects depending on the current state and the command that is currently executing, as described below:

- Disconnected State: In this state, the Abort command will halt a selection or reselection attempt of a Select, Select-and-Transfer, Reselect, or Reselect-and-Transfer command or will halt the Wait-for-Select-and-Receive command before selection. Aborting a selection or reselection attempt before the 33C93B has won arbitration immediately returns the 33C93B to an idle state and generates a "paused/aborted" interrupt. If the 33C93B has already won arbitration, the Abort command causes the 33C93B to remove the Bus ID bits from the SCSI bus while maintaining assertion of SEL. If the target does not respond within at least 200 µs by asserting BSY-, the 33C93B will go to a Bus Free condition and generate a "paused/ aborted" interrupt. If the target does respond within this time period, a "successful completion" interrupt will result instead.

  The Abort command, in addition, will terminate a Select- and-Transfer command if the target has disconnected from the bus. The 33C93B will generate an 85 hex interrupt and will be in the Disconnected state. If the target is still connected at the time the Abort command is recognized, the command will be ignored.

- Target State: In this state, the Abort command will terminate a Receive or Send command or the Data phase portion of a Reselect-and-Transfer command. The following rules apply when issuing an Abort:

  - During a Send or Reselect-and-Send command, the 33C93B removes the data request (DRQ, DBR, etc.) at an arbitrary time during the abort procedure. The host must NOT service any data request once it has written the Abort command to the Command Register until the 33C93B generates an interrupt. Abort processing will not complete until the contents of the FIFO are flushed to the SCSI bus.
  - During a Receive or Reselect-and-Receive command, the host must continue to service any data request from the 33C93B. Abort processing will not complete until the contents of the FIFO are flushed to the host.

    After completion of the Abort command, the Transfer Count Register contains the number of bytes that were not transferred across the SCSI bus. The 33C93B remains in the connected-as-a-target state and will accept any target mode command, including a resume of the aborted command.

4.4.3 Disconnect (04 hex)

The Disconnect command, valid in the initiator and target states, immediately terminates an active Level II command, causes the immediate release of all bus signals, and returns the 33C93B to a disconnected state. In the target role, the Disconnect command is the normal procedure for disconnecting from the SCSI bus following the information transfer phase. In the initiator role, this command can be used to release the bus following a timeout condition.

4.4.4 Assert ATN (02 hex)

The Assert ATN command, valid only when connected as an initiator, allows the initiator to inform the target that it has a message pending. The target should respond with a Message Out Phase. ATN is automatically negated:

- before the last byte of a Transfer Info command issued in response to the Message Out phase;
- when the Identify message out is transferred to the target during a Select-and-Transfer command;
- when a SCSI Bus Free phase occurs.

The Select-with-ATN and Select-with-ATN-and-Transfer commands will cause the 33C93B to assert ATN automatically prior to the release of SEL.

4.4.5 Negate ACK (03 hex)

The Negate ACK command causes the 33C93B to release ACK which for some reason it has held active. Holding ACK active allows the host to respond to information it has just received before the target continues the current phase or proceeds to the next one. The 33C93B, therefore, does not negate ACK before generating an interrupt in the following cases:

- after successful completion of a Message-In Transfer Info command;

- after detection of a parity error on any received SCSI information when the Halt on SCSI Parity Error (HSP) bit is set;
- after unexpected reselection in advanced mode;
- after reception of a save-data-pointer message during a Select-and-Transfer command;
- after reselection by a process with a queue tag which differs from the contents of the Queue Tag Register; and
- after reception of a status byte with a parity error during a Select-and-Transfer command.

ACK negates automatically for all initiator transfers other than Message In transfers. Host parity errors, moreover, do not affect the ACK signal.

Before completing a Message In phase, the initiator, upon examining the message, may decide to reject it and send a "MESSAGE REJECT" message to the target or, upon detecting a parity error in the message, may decide to send a "MESSAGE PARITY ERROR" message to the target. Similarly, if a parity error causes a transfer command to terminate, the initiator may wish to send an "INITIATOR DETECTED ERROR" message to the target. In all cases, the initiator signals its intent to send a message by asserting ATN before issuing the Negate ACK command.

4.4.6 Set IDI (0F hex)

The Set IDI command provides support for overlapped SCSI operations in the initiator role. The host may start a SCSI operation with the IDI bit reset, allowing the 33C93B to handle target disconnects and reconnects and thus minimizing the interrupt handling overhead. When it wishes to start a second operation, the host issues the Set IDI command so that if the current target disconnects and releases the SCSI bus, the 33C93B will produce an interrupt. The host may now start the second operation without having had to wait for the first operation to complete.

4.5 SIMPLE LEVEL II COMMANDS

4.5.1 Select-with-ATN (06 hex)

Select-with-ATN, valid only in the disconnected state, instructs the 33C93B to select a target. Before issuing this command, the host should write the SCSI Bus ID of the target device into the Destination ID Register. The Select-with-ATN command causes the 33C93B to begin bus arbitration. If another device selects or reselects the 33C93B during arbitration, the Select-with-ATN command aborts and a "service required" interrupt (8x hex) will occur.

Should the 33C93B win the arbitration, it asserts SEL and ATN, places the target and initiator Bus IDs on the SCSI data bus, and then deasserts BSY. At this time, a timeout sequence begins, its length determined by the value in the Timeout Period Register. If the target does not respond with bsy within the allotted time, the 33C93B begins a selection abort sequence as described in the Abort command description. If the target has not responded by the end of this sequence, the Select-with-ATN command terminates. If the target responds before the timeout period has elapsed or before the selection abort sequence completes, the 33C93B negates the SEL signal, enters the connected-as-an-initiator state, and generates a "successful completion" interrupt.

A successful abort of Select-with-ATN, either through a timeout or through the Abort command, leaves the 33C93B disconnected from the SCSI bus and results in a "paused/aborted" interrupt.

4.5.2 Select-without-ATN (07 hex)

The Select-without-ATN command is identical to the Select-with- ATN command except that ATN is not set during the Selection Phase.

4.5.3 Reselect (05 hex)

The Reselect command is identical to the Select-without-ATN command except that the I/O- signal is asserted upon completion of the Arbitration Phase. Successful completion of the Reselect command results in the 33C93B being connected as a target.

4.5.4 Receive (10-13 hex)

The four Receive commands---Receive Command, Receive Data, Receive Message Out, and Receive Unspecified Info Out---differ from each other only by the state of the C/D and MSG pins and the type of data that is transferred. These commands, valid only in the target role, correspond to those SCSI information phases where the I/O pins is not asserted; the type of the Receive command selected determines the state of the C/D and MSG outputs according to the following chart (1=asserted):

RECEIVE	COMMAND TYPE	OP-CODE	MSG	C/D	I/O
Receive	Command	10	0	1	0
Receive	Data	11	0	0	0
Receive	Message Out	12	1	1	0
Receive	Unspecified Info Out	13	1	0	0

A Receive command will complete or terminate under any of the following conditions:

- The host has read the specified number of bytes from the Data Register;
- The 33C93B detects a parity error on one of the received data bytes when Halt-on-SCSI-Parity is enabled;
- The 33C93B detects $\overline{ATN}$ when Halt-on-ATN is enabled;
- The 33C93B detects a transfer protocol error;
- The host aborts the Receive command;
- The host issues a Disconnect command; or
- The 33C93B resets because of a Reset command or assertion of MR.

Any conclusion of a Receive command, except those due to a Disconnect command or a Reset, leaves the 33C93B in a connected-as-a-target state and the number of bytes not yet transferred in the Transfer Count Register.

In the case of a Receive Data command, the 33C93B evaluates the contents of the Synchronous Transfer Register. Any offset other than zero selects synchronous transfers. The minimum transfer period applies to both synchronous and asynchronous transfers. The 33C93B also examines the Control Register to determine what mode of data transfer will occur on the host interface.

In all other cases, asynchronous transfers occur on the SCSI bus, and polled I/O transfers occur on the host interface.

4.5.5 Send (14-17 hex)

The four Send commands---Send Status, Send Data, Send Message, and Send Unspecified Info---like the four Receive commands, differ from each other only by the state of the C/D and MSG pins and the type of data that is transferred. These commands, valid only in the connected-as-a-target state, correspond to those SCSI phases where the I/O- pin is asserted; the type of Send command selected determines the state of the C/D and MSG outputs according to the following chart (1=asserted):

SEND	COMMAND TYPE	OP-CODE	MSG	C/D	I/O
Send	Status	14	0	1	1
Send	Data	15	0	0	1
Send	Message In	16	1	1	1
Send	Unspecified Info Out	17	1	0	1

A Send command will complete or terminate under any of the following conditions:

- The initiator has acknowledged receipt of the specified number of bytes;
- The 33C93B detects a parity error on one of the received data bytes when Halt-on-Host-Parity is enabled;
- The 33C93B detects $\overline{ATN}$ when Halt-on-ATN is enabled;
- The 33C93B detects a transfer protocol error;
- The host aborts the Receive command;
- The host issues a Disconnect command; or
- The 33C93B resets because of a Reset command or assertion of MR.

Any conclusion of a Send command, except those due to a Disconnect command or a Reset, leaves the 33C93B in a connected-as-a-target state and

24

the number of bytes not yet transferred in the Transfer Count Register.

In the case of the Send Data command, the 33C93B evaluates the contents of the Synchronous Transfer Register. Any offset other than zero selects synchronous transfers. The minimum transfer period applies to both synchronous and asynchronous transfers. The 33C93B also examines the Control Register to determine what mode of data transfer will occur on the host interface.

In all other cases, asynchronous transfers occur on the SCSI bus, and polled I/O transfers occur on the host interface.

4.5.6 Transfer Info (20 hex)

The Transfer Info command allows the host to send and receive data, command, status, and message information when operating in the connected-as-an-initiator state.

The first $\overline{REQ}$ assertion following connection as an initiator results in a "service required" interrupt. The processor should examine the SCSI Status Register to determine the type and direction of information transfer requested by the target, and then issue a Transfer Info command in response. The 33C93B will also generate an interrupt each time the target device requests a new type of information transfer phase.

The processor either should initialize the Transfer Count Register prior to issuing this command or issue the command with the SBT bit in the Command Register set. Also, if responding to a request for a Data phase, the processor should set the DMA mode select bits in the Control Register and specify the offset and transfer period in the Synchronous Transfer Register before issuing the Transfer Info command.

Behavior of the DBR status bit during Transfer Info depends upon the direction of the transfer. When the bytes move from the initiator to the target, i.e. an out phase, the DBR bit is set whenever the FIFO can accept additional data from the host. When the transfer proceeds in the opposite direction, DBR set indicates that the FIFO contains data available for the host to read.

The Transfer Info command normally terminates or pauses after the specified number of bytes has been sent or received. For a non- Message-In transfer, the 33C93B will generate a "successful completion" interrupt after the target asserts $\overline{REQ}$ to begin a new phase. For a message-in transfer, the 33C93B does not wait for the next phase but instead leaves $\overline{ACK}$ asserted and generates a "paused/aborted" interrupt. The processor can then assert $\overline{ATN}$ if it intends to reject the message before negating $\overline{ACK}$.

The Transfer Info command may terminate for a number of different reasons which are listed below:

- The host issues a Disconnect command;
- The 33C93B resets in response to the assertion of MR or the Reset command;
- The target negates the $\overline{BSY}$ signal;
- The target unexpectedly changes phase, i.e. before the specified number of bytes have been transferred; or
- The incoming data has a parity error and the corresponding halt-on-parity-error bit is set.

The Disconnect command, the hard and soft resets, and the negation of $\overline{BSY}$ will leave the 33C93B in a idle, disconnected state, and in these cases, the value in the Transfer Count Register will not accurately reflect the number of bytes that did not transfer across the SCSI interface. Except for the issuance of the Disconnect command, these occurrences will result in an interrupt.

The 33C93B checks for a parity error on each byte it receives; however, for synchronous transfers, the internal microcontroller will not recognize an error until the transfer reaches a 4096- byte boundary. The response to the parity error, furthermore, depends upon the direction of the transfer. If the parity error occurs on received SCSI data, the 33C93B will halt the SCSI interface, leaving $\overline{ACK}$ asserted to halt the target, and generate a "terminated" interrupt once the host has flushed any remaining bytes from the FIFO. Similarly, if the error occurs on data received on the host interface, the 33C93B will halt the host interface and generate a "terminated" interrupt after any bytes remaining in the FIFO are flushed to the SCSI bus; the $\overline{ACK}$ signal, however, will not remain asserted. In both cases, the Transfer Count Register will indicate the number of bytes that did not successfully transfer to or from the target.

If it detects a parity error but the appropriate halt-on-parity-error bit is not set, the 33C93B will indicate the error by setting the Parity Error bit in the Auxiliary Status Register but will not terminate the Transfer Info command.

An unexpected phase change will cause a "terminated" interrupt, and as in the case of a parity error, the Transfer Count Register contains the number of bytes yet to be transferred. If an unexpected phase change occurs during a SCSI synchronous transfer, the host should test the Parity Error bit in the Auxiliary Status Register, as the phase change most likely occurred before the internal microcontroller recognized the parity error. In the asynchronous case, the 33C93B stops on the byte with the error; therefore, it will always detect a parity error before a phase change in this mode.

4.5.7 Translate Address (18 hex)

The Translate Address Command performs a logical-address to physical-address translation to facilitate processing of certain SCSI commands involving logical addresses up to 32 bits in length. To perform this mapping, the processor first loads the logical address into the Logical Address Register, the disk parameters into the Total Cylinder Number, Total Head Number, and Total Sector Number Registers, and zeros into the Head Number and Cylinder Number Registers. It then issues the Translate Address command, and upon receiving a "successful completion" interrupt, reads the Cylinder Number, Head Number, and Sector Number Registers to obtain the logical address.

The Translate Address command can also compensate for spare sectors. To use this feature, the host, instead of zeroing the Head Number and Cylinder Number Registers, should load the number of spare sectors per cylinder into the Head Number Register and the logical number of sectors per cylinder into the Cylinder Number Register prior to issuing the command.

An overflow during any calculation will result in a "terminated" interrupt.

4.6 COMBINATION LEVEL II COMMANDS

4.6.1 Select-and-Transfer (08 and 09 hex)

The Select-and-Transfer commands greatly reduce the host or local processor interrupt-handling burden by enabling the 33C93B's internal microprocessor to manage the low-level SCSI protocol. Use of these command may result in as few as one interrupt per SCSI operation. Select-and-Transfer commands, used when in an initiator role, typically consist of at least the following SCSI phases: an Arbitration phase, a Selection phase, a Command phase, a Status phase, and a Command-Complete Message phase. These commands optionally include Data and additional Message In phases.

The Select-and-Transfer commands expect the target to follow a certain sequence of SCSI bus phases, and any deviation from this expected protocol results in a "terminated" interrupt. As the different phases complete, the 33C93B updates the Command Phase Register, so upon termination of the command, the host processor may examine this register to identify the cause of the termination and the state of the SCSI operation.

The two Select-and-Transfer commands differ from each other only by whether or not the 33C93B asserts ATN pin during the Selection phase. The ability to assert ATN during Selection supports the SCSI message protocol which calls for an Identify Message Out phase following the selection. When executing a Select-with-ATN-and-Transfer command, the 33C93B expects the target to request a Message Out phase immediately following selection, whereas for a Select-without-ATN-and-Transfer command, it expects the target to begin the Command phase once selection completes.

The 33C93B begins the Select-and-Transfer command by arbitrating for the bus and selecting a target just as during a Select command. If the target does not respond before a timeout occurs, the Select-and-Transfer command halts and generates an interrupt. Failure to complete the Selection phase is also indicated by the fact that the Command Phase Register contains all zeros. If the selection is successful, no interrupt is generated, and the Command Phase Register will be set to a 10 hex.

After completing the Selection phase, the 33C93B begins a Message Out phase if ATN has been asserted or a Command phase if not. When the

target requests a Message Out phase, the 33C93B responds by automatically sending an Identify message byte, which it generates by exclusive-ORing the contents of the Target LUN Register with 80 hex if the Enable Reselection bit in the Source ID Register is reset or with C0 hex if the bit is set. After it has sent the Identify message, the 33C93B will set the Command Phase Register to 20 hex.

Normally, bit 6 of the Identify message mirrors the state of the Enable Reselection bit; however, the host may occasionally wish to allow the 33C93B to respond to a reselection attempt but not enable target disconnects during another SCSI operation. Setting both the Enable Reselection bit and the DOK bit of the Target LUN Register allows the 33C93B to respond to reselection but results in an Identify message byte which does not enable target disconnects.

Following the Identify message out, if bits 3 or 4 of the Destination ID Register specify a tag message and if ATN is asserted, the 33C93B expects the target to request the first byte of a tag message. It responds to this request by sending the selected tag message code and incrementing the Command Phase Register. The 33C93B now expects the target to ask for the second byte and services this request by sending the contents of the Queue Tag Register and incrementing the Command Phase Register to 22 hex.

The 33C93B expects a Command phase to follow the Message Out phase or, if ATN is not asserted during selection, the Selection phase. The 33C93B obtains the SCSI command from the internal Command Descriptor Block Registers and sends either six, ten, or twelve bytes of command information depending on the first byte of the SCSI command. The Select-and-Transfer commands support Group 0 (6-byte CDB), Group 1 (10-byte CDB), and Group 5 (12-byte CDB) SCSI commands. The length of any other command defaults to six bytes unless advanced mode is enabled. The Command Phase Register, set to 30 hex before the first Command byte is sent, increments with each byte transferred, so for a twelve-byte CDB command, the Command Phase Register will contain 3C hex when all bytes of the CDB have been transferred.

After the Command phase, the 33C93B anticipates a Data phase if the Transfer Count Register contains a non-zero value, a Status phase if this register contains zero, or, in either case, a Message In phase if the Enable Reselection bit is set and the DOK bit is not. The 33C93B assumes a pending disconnection if the target requests a Message In phase. Thus, when enabled, the 33C93B expects to receive either a Save-Data-Pointer message (02 hex) or a Disconnect message (04 hex). If a message byte has a parity error and the HSP bit is set or if the target sends an unsupported message, the 33C93B will generate a "terminated" interrupt, alerting the processor of this fact and allowing it to retrieve the message byte via the Transfer Info command.

Reception of a correct Save-Data-Pointer message results in a "paused/aborted" interrupt, terminating the Select-and-Transfer command with the Command Phase Register set to 41 hex. The processor can then save the SCSI data pointer before resuming the Select-and-Transfer command.

A Disconnect message, on the other hand, will not cause an interrupt; instead, command execution continues with the Command Phase Register set to 42 hex and with Bus Free as the next expected phase. The 33C93B updates the Command Phase Register to 43 hex when the target actually disconnects and, if the IDI bit is set, suspends the Select-and-Transfer command with an 85 hex interrupt. If, however, the IDI bit is reset, the 33C93B sits in an idle state, waiting for the target to reconnect. Reselection by the original target generates no interrupt and increments the Command Phase Register to 44 hex; reselection by a different target will cause a "terminated" interrupt. In advanced mode, this interrupt will not occur until the 33C93B has also received the Identify message from the target and placed the logical unit number in the Target LUN Register.

Following the original target reselection, the 33C93B expects an Identify Message In phase from the target. This single-byte message should be of the binary form: 10r00ttt, where r and ttt match the corresponding bits in the Target LUN Register. Successful completion of this phase results in the Command Phase register being updated to 45 hex or 70 hex depending upon whether or not the 33C93B expects a tag message, deduced from the settings of the TG0 and TG1 bits of the Destination ID Register.

The target, in the latter case, should send a Simple Queue tag message immediately after the Identify message. Upon receiving and validating the message byte, the 33C93B increments the Command Phase Register and awaits the second message

byte from the target. When it receives this byte, the 33C93B sets the Command Phase to 45 hex and then compares the byte to the contents of the Queue Tag Register. If the two values match, command execution proceeds; if the two values differ, the 33C93B stores the received byte in the Queue Tag Register, generates a "Different Process Reselected" interrupt (26 hex) and terminates the Select-and-Transfer command.

The 33C93B anticipates a data phase immediately after the Command phase or after successfully receiving the proper messages after reselection. To handle the Data phase, the Select-and-Transfer command effectively performs a Transfer Info command. The contents of the Transfer Count Register determines the number of bytes to transfer; the value in the Synchronous Transfer Register specifies the type and minimum period of the transfers on the SCSI interface; and the DMA mode select bits in the Control Register specify the protocol to follow on the host interface.

Any number of disconnection/reconnection cycles may occur during the data transfer so long as the target follows the defined message protocol. The Command Phase Register will cycle through the disconnect phases (41-45,70,71) with each disconnection and subsequent reconnection until all of the data has been transferred, at which point it is set to 46 hex. During the data transfer, a disconnection will cause an interrupt regardless of the setting of the IDI bit to allow the host to reinitialize the external DMA controller.

The start of the Status phase, assuming the transfer count has reached zero, advances the Command Phase Register to 47 hex. If the status byte has no parity error or if the HSP bit is not set, the internal microcontroller places the byte in the Target LUN Register and updates the Command Phase Register to 50 hex. If the byte contains an error, a 27 hex interrupt will occur, and the command will terminate with ACK asserted.

The 33C93B expects the target to send a Command-Complete message (00 hex) to indicate that the SCSI operation has completed. Upon receiving this message, the 33C93B sets the Command Phase Register to 60 hex, and if the EDI bit is reset, generates "successful completion" interrupt. The processor should then read the Target LUN Register to examine the target status. Another interrupt will occur when the SCSI bus goes to the Bus Free state or when the target again asserts REQ to begin a new information transfer phase (as in SCSI linked commands). Setting the EDI bit suppresses the "successful completion" interrupt until the target disconnects from the SCSI bus.

The following table summarizes the possible values that the Command Phase Register can assume during the Select-and-Transfer commands and their meanings relative to command termination:

COMMAND PHASE	MEANING
00	No SCSI bus device has been selected. The 33C93B is in the disconnected state.
10	The target has been selected. The 33C93B is now in the connected-as-an-initiator state.
20	An Identify message has been sent to the target.
21	The Tag message code has been sent to the target.
22	The Queue tag has been sent to the target.
30	Command phase has started, no bytes transferred.
3X	Command phase, x bytes have been transferred.
41	Save-Data-Pointer message received.
42	Disconnect message received, bus not free.
43	Target has disconnected (SCSI Bus Free) following a successful transfer of a Disconnect message. The 33C93B is now in the disconnected state.
44	The 33C93B has been reselected by the target with a SCSI bus ID which matches the value in the Destination ID Register. The 33C93B is now in the connected as an initiator state.
45	The 33C93B has received an matching Identify message and, if expected, a matching Tag message from the target.
46	The number of bytes specified in the Transfer Count Register have been transferred to or from the target during the Data phase.
47	The target has begun a Receive Status phase.
50	The 33C93B has successfully received a Status byte from the target and stored it in the Target LUN Register.
60	The 33C93B has successfully received a Command-Complete message from the target.
70	The 33C93B has received an Identify message from the target, and the Logical Unit Number matches the value in the Target LUN Register. A tag message is expected.
71	The 33C93B has received a Simple-Queue Tag message.

TABLE 4-2. SELECT-AND-TRANSFER COMMANDS

The host processor may resume a Select-and-Transfer sequence by issuing the command when the 33C93B is in the Connect-as-an-initiator state. When resuming the Select-and-Transfer, the 33C93B examines the Command Phase Register to determine where to restart execution of the command. This feature, in conjunction with the Intermediate Disconnect Interrupt enabled, supports multi-threaded or overlapped I/O on the SCSI bus.

The following table briefly describes the valid settings of the Command Phase Register when resuming a Select-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after target selection is complete.
20	Resume after Identify message out. Command or message phases are expected; an implied Negate ACK occurs.
22	Resume after Tag message out. Command phase is expected; an implied Negate ACK occcurs.
30	Resume when Command phase has begun ($\overline{REQ}$ asserted).
41	Resume after Command phase or after a Save-Data-Pointer message. Data, Status, or Message In phases are expected. An implied Negate ACK occurs.
42	Resume to complete Disconnect Message In; an implied Negate ACK occurs.
44	Resume after reselection by a target. An Identify Message In expected.
45	Resume to transfer more data in a data transfer phase. May expect Status or Message In as well. An implied Negate ACK occurs.
46	Resume after the Data phase has completed, expecting Status phase or a Save-Data-Pointer/Disconnect Message In phase. An implied Negate ACK does NOT occur.
50	Resume to complete a Status phase; an implied Negate ACK occurs.
60	Resume to complete a Command Complete message from the target; an implied Negate ACK occurs.
70	Resume to receive a Simple-Queue Tag message. An implied Negate ACK occurs.

TABLE 4-3. SELECT-AND-TRANSFER COMMANDS

4.6.2 Reselect-and-Transfer (0A and 0B hex)

The Reselect-and-Transfer commands consist of the Reselect-and- Receive-Data and the Reselect-and-Send-Data commands. These commands cause the 33C93B to execute certain common SCSI bus phase sequences as a target following a Reselection phase. These phases, determined by which command is sent and the setting of the EDI bit in the Control Register and the SCC bit in the Destination ID Register, are summarized below. Refer to the descriptions of the Send-Status-and-Command-Complete and Send- Disconnect-Message commands for details on those sequences.

- Reselect-and-Receive command, EDI=0, and SCC=don't care:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Completion interrupt.
- Reselect-and-Send command, EDI=0, and SCC=don't care:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;
  - Completion interrupt.
- Reselect-and-Receive command, EDI=1, and SCC=0:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Chain to Send-Status-and-Command-Complete
- Reselect-and-Send command, EDI=1, and SCC=0:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;
  - Chain to Send-Status-and-Command-Complete;
- Reselect-and-Receive command, EDI=1, and SCC=1:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Chain to Send-Disconnect-Message;
- Reselect-and-Send command, EDI=1, and SCC=1:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;
  - Chain to Send-Disconnect-Message;

The Message In phase consists of an Identify message and, if bits 3 and 4 in the Destination ID Register are not both zero, a Simple-Queue Tag message. The commands send the contents of the Queue Tag Register as the second byte of the Tag message.

If the reselection attempt times out during a Reselect-and-Transfer command, if $\overline{ATN}$ is asserted and HA=1, or if a parity error is detected on a incoming data byte (and HSP=1 or HHP=1, depending on data direction), the command will terminate with the appropriate status. In this case, the Command Phase Register will indicate the last successfully completed phase. If these conditions do not occur and all phases complete normally, the command will end with a "successful completion" interrupt at this point if EDI=0. However, if EDI=1, no interrupt is generated and command chaining occurs (as described above).

The following table summarizes the possible values that the Command Phase Register can assume during the Reselect-and-Transfer commands and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No SCSI bus device has been reselected. The 33C93B is in the disconnected state.
10	The 33C93B has successfully reselected the initiator. The 33C93B is now in the connected as a target state.
20	The Identify message has been successfully sent to the initiator.
46	The requested data transfer has been completed.

TABLE 4-4. RESELECT-AND-TRANSFER COMMANDS

The host processor may resume a Reselect-and-Transfer sequence by issuing the command when the 33C93B is operating in the connected-as-a-target state. When resuming, the 33C93B examines the Command Phase Register to determine where to restart the Reselect-and-Transfer command. This feature in conjunction with the capability to chain to other combination commands allows longer SCSI bus sequences to be performed by a single command.

The following table briefly describes the meaning of the Command Phase Register when resuming a Reselect-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after initiator reselection is complete; start with Identify Message Out.
20	Resume after Identify message out; start with data transfer phase. If Transfer Count is zero, no data transfer phase occurs. In either case, a chain to another combination command can occur if enabled.

TABLE 4-5. RESELECT-AND-TRANSFER COMMANDS

4.6.3 Wait-for-Select-and-Receive (0C hex)

The Wait-for-Select-and-Receive causes the 33C93B to idle until it is selected by an initiator, at which time the 33C93B will enter the target mode and automatically request message and command information. Optionally, the 33C93B will then disconnect if it receives a SCSI read command. Use of this command therefore eliminates the interrupts which normally occur after selection and after each subsequent SCSI bus phase and minimizes bus-connect time during SCSI read commands.

If the initiator asserts $\overline{ATN}$ during the Selection phase, the 33C93B first executes an implied "Receive Message Out" command to get the Identify message and the Tag message, if any, from theinitiator. The 33C93B stores the Identify message byte in the Target LUN Register; it encodes the Tag message code into bits 3 and 4 of the Destination ID Register and places the queue tag into the Queue Tag Register. Normally, the Wait-for-Select-and-Receive command rejects an Identify message with the LUNTAR bit (bit 5) set; however, issuing this command with the SBT bit in the Command Register set allows the 33C93B to accept an Identify message for a target routine.

The 33C93B executes an implied "Receive Command" following the Selection phase or Identify Message In phase and stores the SCSI command information in the CDB registers. It determines the number of command bytes to request from the SCSI group code in the first byte of the CDB.

At this point, a "successful completion" interrupt normally will occur to allow the local processor to interpret the SCSI CDB. However, by setting the EDI bit prior to issuing a Wait-for-Select-and-Receive command, the host enables the 33C93B to perform an automatic disconnect when it receives a SCSI read command. Thus, when EDI=1 and the 1st CDB byte received contains a six, ten, or twelve byte read command code, the 33C93B will suppress the interrupt and chain to the Send-Disconnect-Message command. Completion of this sequence causes an interrupt and normally indicates a transition to the bus free condition. Refer to the Send-Disconnect-Message command description for more details.

If the message or command information received from the initiator is invalid, the Wait-for-Select-and-Receive command will be terminated and the appropriate status reported. As usual, the Command Phase Register will indicate which phases of the command completed before the error condition occurred.

The following table summarizes the possible values that the Command Phase Register can assume during the Wait-for-Select-and-Receive command and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	The 33C93B has not been selected. The 33C93B is in the disconnected state.
10	The 33C93B has been successfully selected by the initiator. The 33C93B is now in the connected-as-a- target state.
20	The 33C93B has received a message byte (Identify) from the initiator. The Target LUN register holds the byte.
21	The 33C93B has received a message byte (Tag code) from the initiator. The Queue Tag Register contains the byte.
22	The 33C93B has received a message byte (Queue Tag) from the initiator. The Queue Tag Register contains the byte.
30	The 33C93B is ready to begin Command phase. The SCSI bus phase lines and REQ have not been asserted.
31	The 33C93B has transferred one command byte from the initiator. The SCSI Status may indicate the need for the host to load the command size into the Own ID Register.
3x	The 33C93B has transferred x command bytes from the initiator.

TABLE 4-6. WAIT-FOR-SELECT-AND-RECEIVE COMMANDS

A "paused/aborted" interrupt in conjunction with command phases 20 and 21 indicate that the respective message byte was not valid. A parity error in the Identify message results in the appropriate interrupt and the Command Phase Register set to 10 hex. This combination allows the host to retry the transfer by merely reissuing the command to resume the operation from the proper phase. A parity error in the other two message bytes results in a command phase of 21 or 22, indicating which byte contained the error.

The host processor may resume the Wait-for-Select-and-Receive command by issuing the command when the 33C93B is operating in the connected-as-a-target state. When resuming this command, the 33C93B examines the Command Phase Register to determine where to restart the Wait-for-Select-and-Receive command. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the Command Phase Register when resuming a Wait-for-Select-and-Receive command:

COMMAND PHASE	MEANING
10	Resume after selection by the initiator is complete. Start with Identify Message Out if ATN is asserted; otherwise, start with Command phase.
20	Resume after a Message Out; check the received message in the Target LUN Register for a valid Identify message.
21	Resume after Identify message verified. Start with Tag Message Out if ATN is asserted; otherwise, start with Command phase.
30	Resume after Identify Message Out. Start with Command phase.
31	Resume after the 33C93B has transferred one command byte from the initiator. This resume point is used only when an unknown group code has been detected in advanced mode and the command size has been loaded into the Own ID Register.

TABLE 4-7. WAIT-FOR-SELECT-AND-RECEIVE COMMANDS

4.6.4 Send-Status-and-Command-Complete (0D hex)

The Send-Status-and-Command-Complete command, valid in the target role, combines the Status and the Command-Complete Message phases used to complete a SCSI operation into one command. This command also supports linked SCSI operations by optionally sending a Linked-Command-Complete message after the transferring the status byte. Bits in the CDB12 register corresponding to the standard linked command control bits in the CDB control the choice of Linked-Command-Complete messages.

Before issuing this command, the host loads the status byte into the CDB11 register and the link control bits from the current CDB into the CDB12 register. Note that the bits used by the 33C93B are identical in meaning to the SCSI standard link control bits. Consequently, the host processor may simply load the control byte from the current SCSI command into CDB12 to obtain the correct function. As the command execution progresses, the Command Phase Register will update to indicate the last phase completed.

The possible sequences caused by this command are as follows:

- CDB12 bit0=0, bit1=don't care: The status byte in CDB11 is sent, followed by a Command Complete message (00 hex), followed by a transition to bus free. A "successful completion" interrupt now occurs.
- CDB12 bit0=1, bit1=0: The status byte in CDB11 is sent, followed by a Linked-Command-Complete message (0A hex). If the DF bit in the Destination ID Register is not set, a chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to obtain the next CDB from the initiator. 33C93B command execution proceeds as described for that command.
- CDB12 bit0=1, bit1=1: The status byte in CDB11 is sent, followed by a Linked-Command-Complete-with-Flag message (0B hex). If the DF bit in the Destination ID Register is not set, a chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to obtain the next CDB from the initiator. 33C93B command execution proceeds as described for that command.

Assertion of $\overline{ATN}$ when HA=1, assertion of $\overline{MR}$, or execution of a Disconnect or Reset command will terminate this command.

The following table summarizes the possible values that the Command Phase Register can assume during the Send-Status-and-Command-Complete command and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, $\overline{\text{ATN}}$ was found to be asserted.
50	Status phase transfer completed.
60	Command Complete message transfer completed.
61	Linked Command Complete message transfer completed.

TABLE 4-8. SEND-STATUS-AND-COMMAND-COMPLETE COMMANDS

The host processor may resume the Send-Status-and-Command-Complete command by loading the appropriate value into the Command Phase Register prior to issuing the command. This feature, in conjunction with the capability to chain to other combination commands, allows for a single command to invoke longer SCSI bus sequences.

The following table briefly describes the meaning of the Command Phase Register when resuming a Send-Status-and-Command-Complete command:

COMMAND PHASE	MEANING
50	Resume after status phase. Start with command complete message. May chain to command fetch if selected to do so.

TABLE 4-9. SEND-STATUS-AND-COMMAND-COMPLETE COMMANDS

4.6.5 Send-Disconnect-Message (0E hex)

The Send-Disconnect-Message command, a target-mode command, instructs the 33C93B to send a Disconnect message and then to deassert the BSY signal, causing a logical disconnection of the device from the SCSI bus. Also, a Save-Data-Pointer message will precede the Disconnect message if the host sets the IDI bit prior to issuing this command.

Assertion of ATN when HA=1, assertion of MR, or execution of a Disconnect or Reset command will terminate this command. The following table summarizes the possible values that the Command Phase Register can assume during the Send-Disconnect-Message and their meanings relative to command termination.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN was found to be asserted.
41	The Save-Data-Pointer message was transferred.
42	The Disconnect message was transferred.
43	The bus free state occurred after the Disconnect message was transferred. The 33C93B is now in the disconnected state.

TABLE 4-10. SEND-TO-DISCONNECT-MESSAGE COMMANDS

5.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to GND . . . . . -0.5 V to +7.0 V
Operating temperature . . . . . 0° to 70° C
Storage temperature . . . . . -55° to +125° C
Power dissipation . . . . . 500 mW
Input Static Discharge Protection . . . . . 1200 V pin to pin

DC OPERATING CHARACTERISTICS . . . . . Ta = 0° to 70° C,
. . . . . VCC = +5 V ± - 0.25 V, GND = 0 V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
IIL	Input Leakage		10	uA	VIN = .4 to VCC
IOL1	SCSI Output Leakage (Inactive)		50	uA	VOUT = .5 to VCC
IOL2	Output Leakage (Tri-state)		10	uA	VOUT = .4 to VCC
VIH	Input High Voltage	2.0	5.0	V	
VIL	Input Low Voltage	-.25	0.8	V	
VIHYS	Schmitt Trigger Input Hysteresis (All SCSI Pins)	0.3		V	
VOH	Output High Voltage	2.4		V	IO = -400 uA
VOL1	SCSI Output Low Voltage (1)		0.5	V	IO = 48.0 mA
VOL2	Output Low Voltage (All Others)		0.4	V	IO = 4.0 mA
ICC	Supply Current		36	mA	Ta = +25° C

(1) $\overline{\text{REQ}}$ and $\overline{\text{ACK}}$ will sink 57 mA at 0.5 volts.

6.0 TIMING CHARACTERISTICS

Timing characteristics are valid over the entire operating temperature (0° to 70° C) and voltage (4.75 to 5.25 volts) ranges, and are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts. All outputs are assumed to have a load capacitance of 50 picofarads. Additionally, open-drain outputs DRQ and DACK are tested with 10 mA current source pull-ups as loads.

The SCSI asynchronous timings, furthermore, assume that the minimum assertion and deassertion times specified for the chosen transfer period have been met. For example, with a transfer period of four, the 33C93B, acting as a target, will assert REQ for at least 200 ns. If the initiator takes more than 200 ns from the leading edge of REQ to assert ACK, then the 33C93B will release REQ within 175 ns. However, if the initiator responds with ACK within 200 ns of REQ, the 33C93B may not meet the 175 ns maximum.

These timings, moreover, apply only during a burst and assume that the FIFO has space or data available to allow the burst to continue. For instance, the time from the REQ in low to ACK out low for the first byte of a new phase or of a 4096-byte burst will depend on the time needed by the 33C93B and possibly the host microprocessor to respond to the new phase or to set up for the next 4096-byte block. Clearly, the 33C93B can not meet the175 ns timing in these situations. In addition, the internal microcontroller controls the handshaking of messages bytes, like the Identify and Disconnect messages, during execution of the combination commands, and again, in these cases, the 33C93B will not meet the asynchronous transfer timings given in the following tables.

Many of the timing parameters that follow are defined in terms of an internal clock cycle time Tcyc. The cycle time depends upon the input clock frequency, the clock divisor selected, and, for synchronous transfers and if the input clock frequency is 16 MHz or greater, the setting of the FSS bit in the Synchronous Transfer Register. Section 6.2.16 provides the details on calculating Tcyc for a given set of these parameters. For normal SCSI transfers, the resulting clock has a frequency from 4 MHz to 5 MHz; for fast SCSI transfers, the frequency falls in the range from 8 MHz to 10 MHz. For non-transfer timings, such as those pertaining to arbitration and bus release, Tcyc corresponds to the value for normal SCSI transfers.

6.1 PROCESSOR/DMA INTERFACE

6.1.1 CLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tcp	Clock Period	50	125	ns
tch	Clock High	20		ns
tcl	Clock Low	20		ns

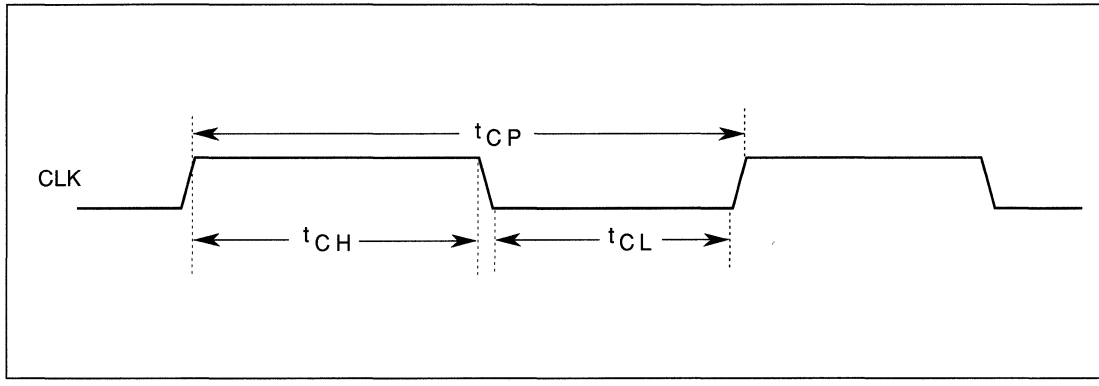


FIGURE 6-1. CLOCK TIMING

6.1.2 $\overline{MR}$

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tmr	$\overline{MR}$ PULSE WIDTH	1		us

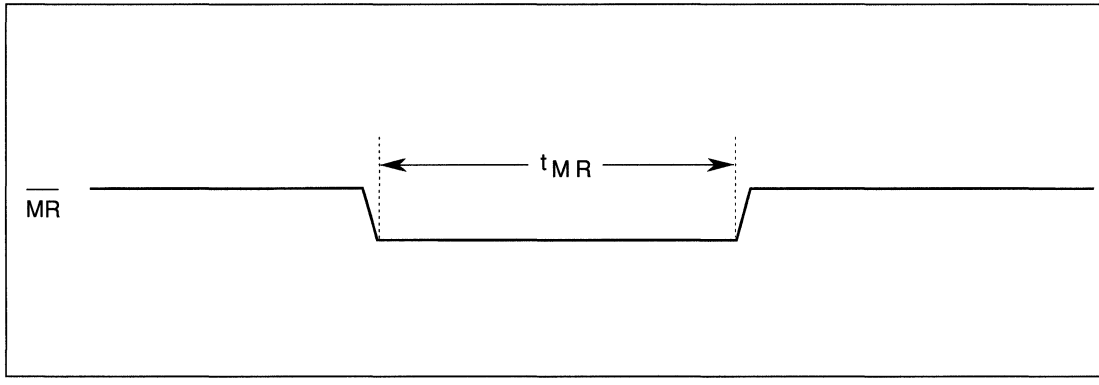


FIGURE 6-2. MR- TIMING

6.1.3 Processor Write (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavwl	A0 Valid to $\overline{WE}$ Low	0		ns
tclwl	$\overline{CS}$ Low to $\overline{WE}$ Low	0		ns
twe	$\overline{CS}$ Low, $\overline{WE}$ Low Time	120		ns
tdvwh	Data Valid to $\overline{WE}$ High	70		ns
twhai	$\overline{WE}$ High to $\overline{A0}$ Invalid	0		ns
twhch	$\overline{WE}$ High to $\overline{CS}$ High	-5		ns
twhdi	$\overline{WE}$ High to Data Invalid	0		ns
twhw1	$\overline{WE}$ High to $\overline{WE}$ or $\overline{RE}$ Low	100		ns

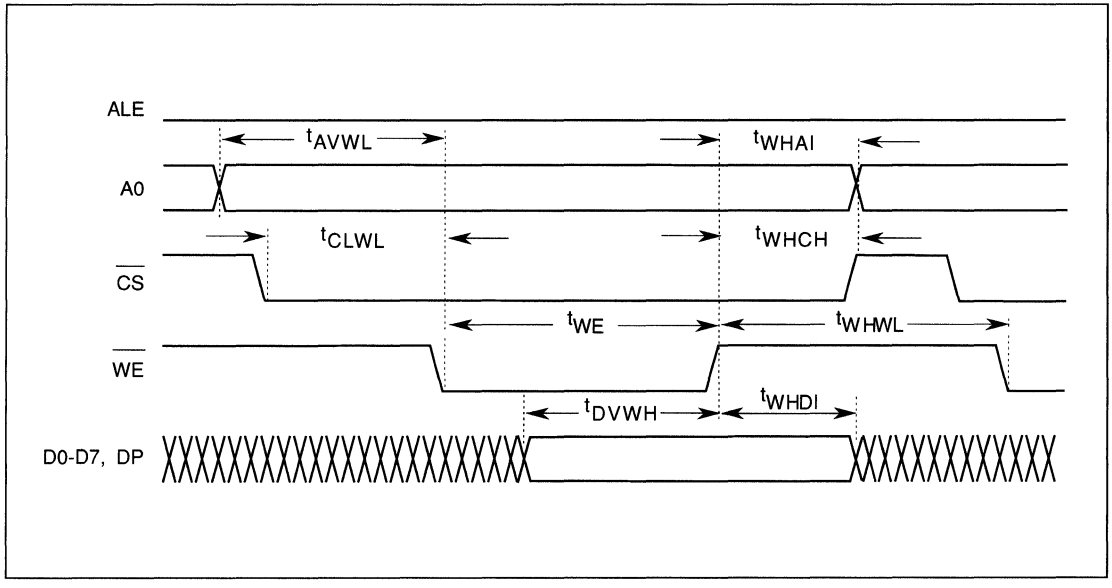


FIGURE 6-3. PROCESSOR WRITE TIMING

6.1.4 Processor Read (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavrl	A0 Valid to $\overline{RE}$ Low	0		ns
tclrl	$\overline{CS}$ Low to $\overline{RE}$ Low	0		ns
tre	$\overline{CS}$ Low, $\overline{RE}$ Low Time	180	10000	ns
trldv	$\overline{RE}$ Low to Data Valid		162	ns
trhch	$\overline{RE}$ High to $\overline{CS}$ High	-5		ns
trhdi	$\overline{RE}$ High to Data Invalid	5	40	ns
trhrl	$\overline{RE}$ High to $\overline{RE}$ or $\overline{WE}$ Low	100		ns
trhai	$\overline{RE}$ High to A0 Invalid	0		ns

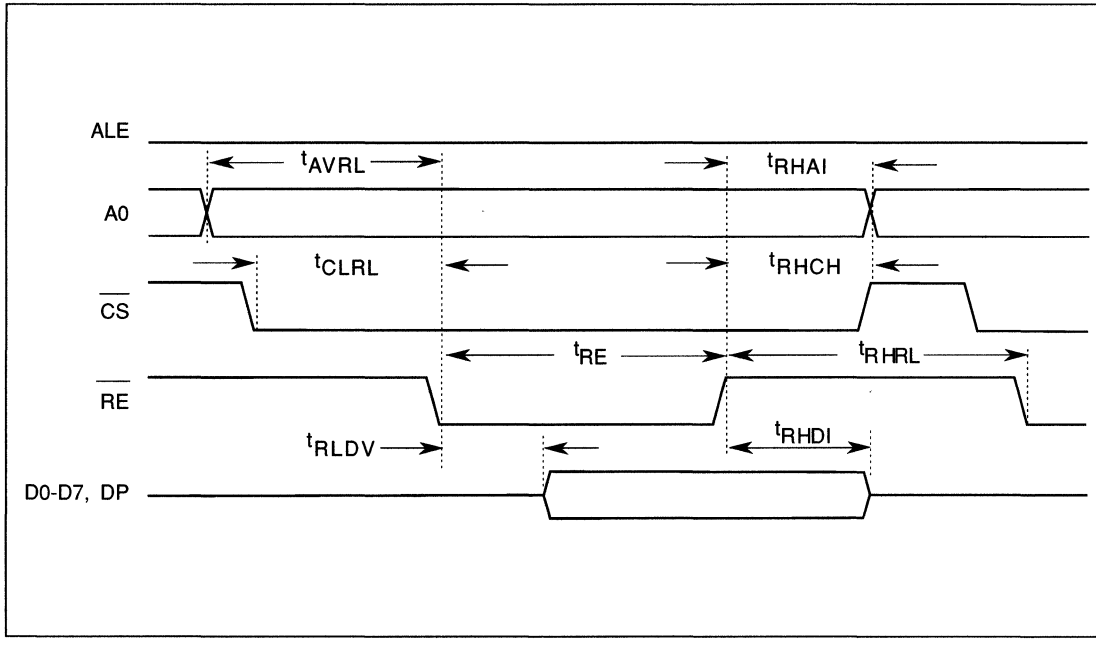


FIGURE 6-4. PROCESSOR READ TIMING

6.1.5 Processor Write (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR Value to ALE Low	40		ns
talai	ALE Low to ADDR Invalid	0		ns
talwl	ALE Low to $\overline{WE}$ Low	90		ns
tclwl	$\overline{CS}$ Low to $\overline{WE}$ Low	0		ns
twe	$\overline{CS}$ Low, to $\overline{WE}$ Low Time	120		ns
tdvwh	Data Valid to $\overline{WE}$ High	70		ns
twhch	$\overline{WE}$ High to $\overline{CS}$ High	-5		ns
twhdi	$\overline{WE}$ High to Data Invalid	0		ns
twhwl	$\overline{WE}$ High to $\overline{WE}$ or $\overline{RE}$ Low	100		ns
tahal	ALE High to ALE Low	40	1000	ns

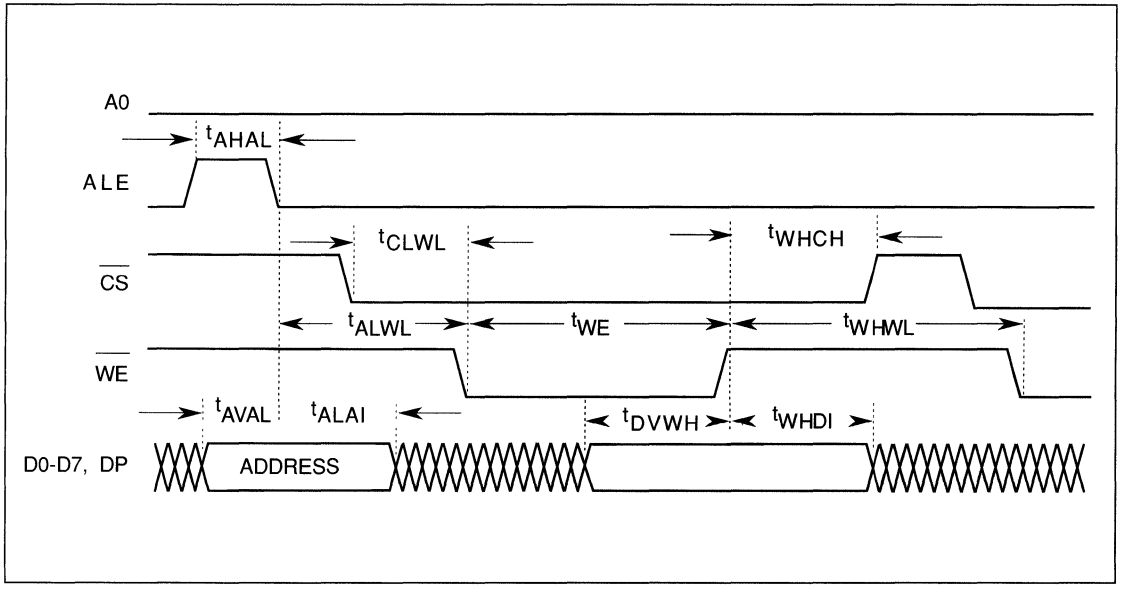


FIGURE 6-5. PROCESSOR WRITE (DIRECT) TIMING

6.1.6 Processor Read (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR Valid to ALE Low	40		ns
talai	ALE Low to ADDR Invalid	0		ns
talrl	ALE Low to $\overline{RE}$ Low	30		ns
tclrl	$\overline{CS}$ Low to $\overline{RE}$ Low	0		ns
tre	$\overline{CS}$ Low, $\overline{RE}$ Low Time	180	10000	ns
trldv	$\overline{RE}$ Low to Data Valid		162	ns
trhch	$\overline{RE}$ High to $\overline{CS}$ High	-5		ns
trhdi	$\overline{RE}$ High to Data Invalid	5	40	ns
trhrl	$\overline{RE}$ High to $\overline{RE}$ or $\overline{WE}$ Low	100		ns
tahal	ALE High to ALE Low	40	1000	ns

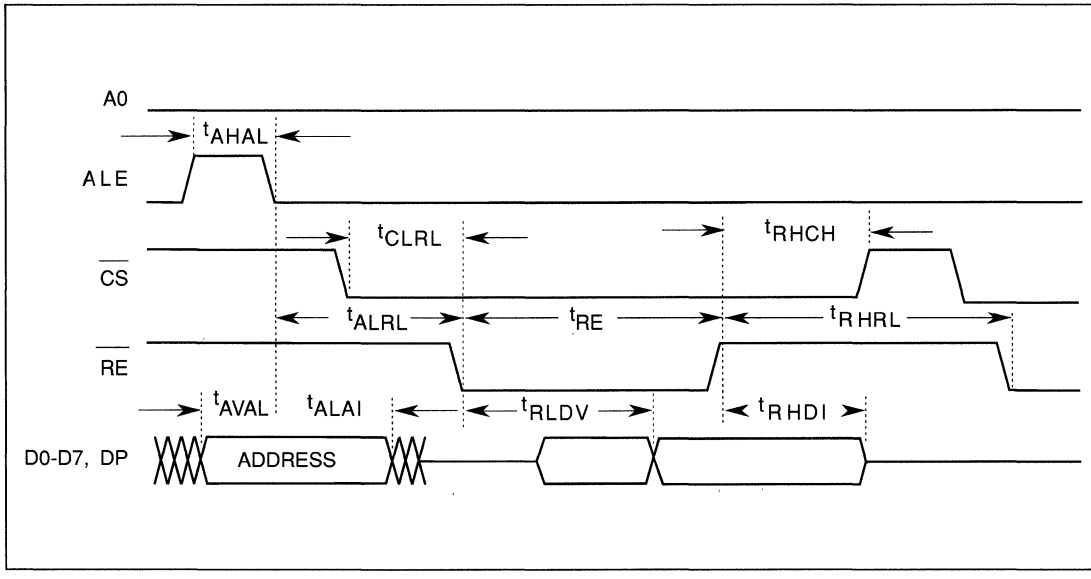


FIGURE 6-6. PROCESSOR READ (DIRECT) TIMING

6.1.7 DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	$\overline{DACK}$ Low to $\overline{WE}$ Low	0		ns
tdlqh	$\overline{DACK}$ Low to $\overline{DRQ}$ High		75	ns
twr	$\overline{WE}$ Pulse Width	50		ns
twhwl	$\overline{WE}$ High to $\overline{WE}$ Low	100		ns
tdvwh	Data Valid to $\overline{WE}$ High	25		ns
twhdh	$\overline{WE}$ High to $\overline{DACK}$ High	0		ns
twhdi	$\overline{WE}$ High to Data Invalid	0		ns
tdhql	$\overline{DACK}$ High to $\overline{DRQ}$ Low	0		ns

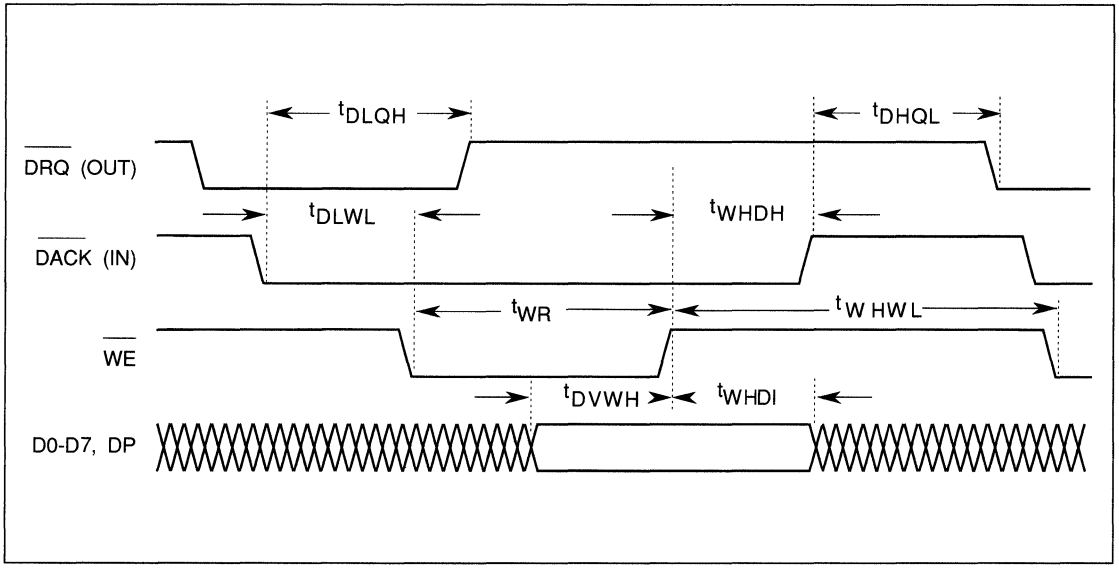


FIGURE 6-7. DMA WRITE TIMING

6.1.8 DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	$\overline{DACK}$ Low to $\overline{RE}$ Low	0		ns
tdlqh	$\overline{DACK}$ Low to $\overline{DRQ}$ High		75	ns
trd	$\overline{RE}$ Pulse Width	80		ns
trhrl	$\overline{RE}$ High to $\overline{RE}$ Low	100		ns
trldv	$\overline{RE}$ Low to Data Valid		70	ns
trhdh	$\overline{RE}$ High to $\overline{DACK}$ High	0		ns
trhdi	$\overline{RE}$ High To Data Invalid	5	40	ns
tdhql	$\overline{DACK}$ High to $\overline{DRQ}$ Low	0		ns

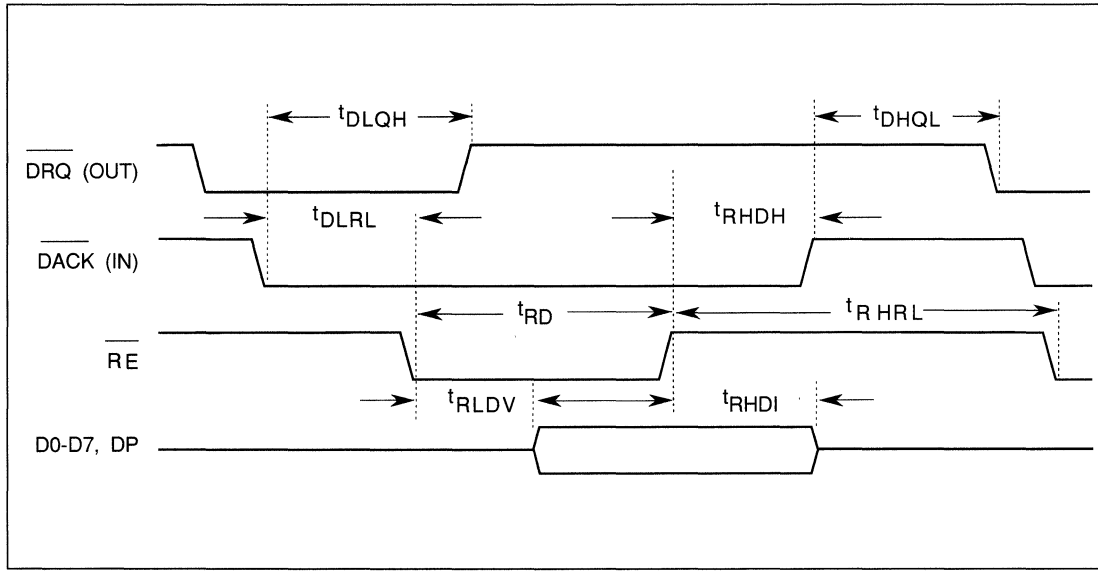


FIGURE 6-8. DMA READ TIMING

6.1.9 WD-BUS Buffer Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ High to $\overline{RCS}$ Low	0	40	ns
tslwv	$\overline{RCS}$ Low to $\overline{WE}$ Valid	-5	20	ns
two	$\overline{WE}$ Pulse Width (1)	1-10 ns		Tcyc
twhwl	$\overline{WE}$ High to $\overline{WE}$ Low (A)	1-10 ns		Tcyc
twldv	$\overline{WE}$ Low to Data Valid		20	ns
twhdi	$\overline{WE}$ High to Data Invalid	1-		ns
tqlsh	DRQ Low to $\overline{RCS}$ Tri-state	8	10	Tcyc
tshwi	$\overline{RCS}$ Tri-state to $\overline{WE}$ Invalid		100	ns
twhsh	$\overline{WE}$ High to $\overline{RCS}$ Tri-state	0		ns
tslwl	$\overline{RCS}$ Low to $\overline{WE}$ Low	60		ns
twlql	$\overline{WE}$ Low to DRQ Low (2)		55	ns
tslql	$\overline{RCS}$ Low to DRQ Low (3)		75	ns

(1) Two + Twhwl = 2*Tcyc
(2) Guarantees that only one more byte will be transferred.
(3) Guarantees that only one byte will be transferred.

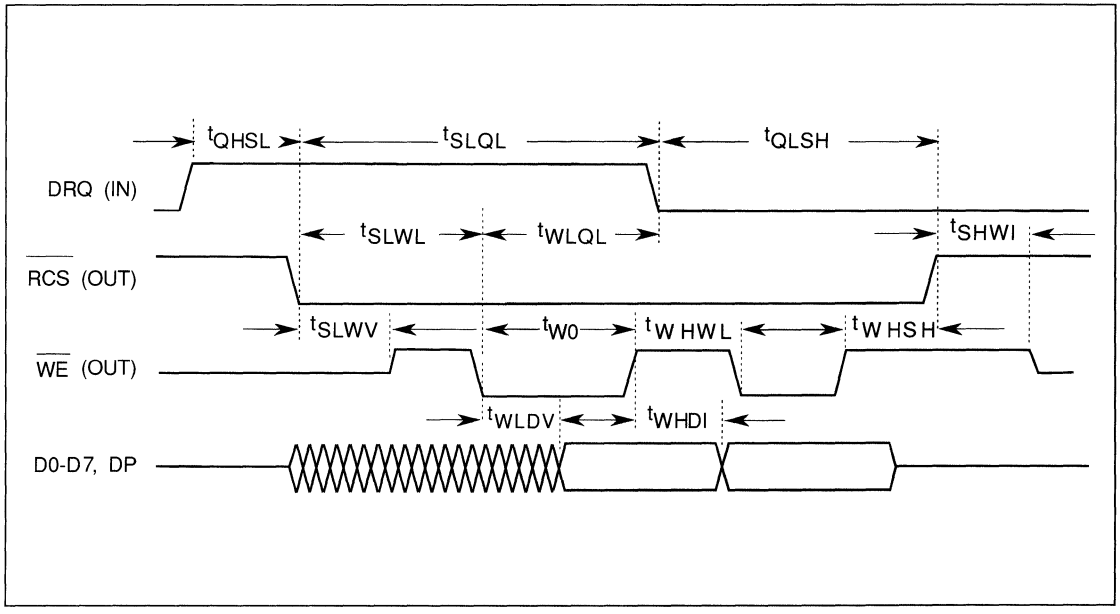


FIGURE 6-9. WD BUS BUFFER WRITE TIMING

6.1.10 WD-BUS Buffer Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ High to $\overline{RCS}$ Low	0	40	ns
tslrv	$\overline{RCS}$ Low to $\overline{RE}$ Valid	-5	20	ns
tro	$\overline{RE}$ Pulse Width (1)	1-10 ns		Tcyc
trhrl	$\overline{RE}$ High to $\overline{RE}$ Low (1)	1-10 ns		Tcyc
tdvrh	Data Valid to $\overline{RE}$ High	20		ns
trhdi	$\overline{RE}$ High to Data Invalid	0		ns
tqlsh	DRQ Low to $\overline{RCS}$ Tri-state	8	10	Tcyc
tshri	$\overline{RCS}$ Tri-state to $\overline{RE}$ Invalid		100	ns
trhsh	$\overline{RE}$ High to $\overline{RCS}$ Tri-state	0		ns
tslrl	$\overline{RCS}$ Low to $\overline{RE}$ Low	60		ns
trlql	$\overline{RE}$ Low to DRQ Low (2)		55	ns
tslql	$\overline{RCS}$ Low to DRQ Low (3)		75	ns

(1) Tro + Trhrl = 2*Tcyc
(2) Guarantees that only one more byte will be transferred.
(3) Guarantees that only one byte will be transferred.

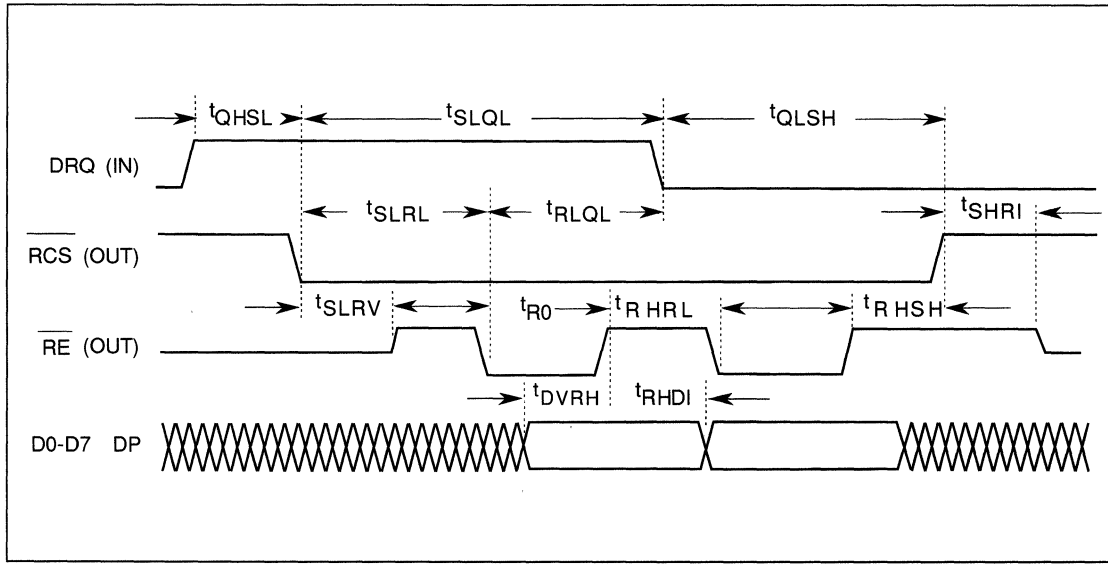


FIGURE 6-10. WD BUS BUFFER READ TIMING

6.1.11 Burst DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	$\overline{DACK}$ Low to $\overline{WE}$ Low	0		ns
twlqh	$\overline{WE}$ Low to $\overline{DRQ}$ High		50	ns
twr	$\overline{WE}$ Pulse Width	30		ns
twhwl	$\overline{WE}$ High to $\overline{WE}$ Low	30		ns
tdvwh	Data Valid to $\overline{WE}$ High	18		ns
twhdh	$\overline{WE}$ High to $\overline{DACK}$ High	0		ns
twhdi	$\overline{WE}$ High to Data Invalid	0		ns
tdhql	$\overline{DACK}$ High to $\overline{DRQ}$ Low	0		ns

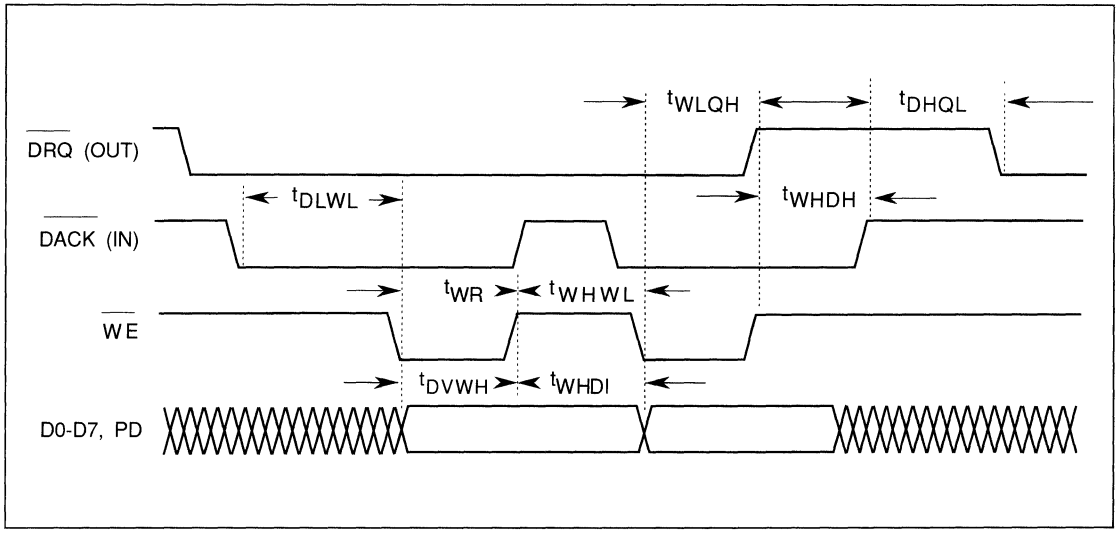


FIGURE 6-11. BURST DMA WRITE TIMING

6.1.12 Burst DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	$\overline{DACK}$ Low to $\overline{RE}$ Low	0		ns
tdldv	$\overline{DACK}$ Low to Data Valid	50		ns
trlqh	$\overline{RE}$ Low to $\overline{DRQ}$ High		60	ns
trd	$\overline{RE}$ Pulse Width	30		ns
trhrl	$\overline{RE}$ High to $\overline{RE}$ Low	30		ns
trhdv	$\overline{RE}$ High to Data Valid		80	ns
trhdh	$\overline{RE}$ High to $\overline{DACK}$ High	0		ns
trhdi	$\overline{RE}$ High to Data Invalid	5	40	ns
tdhql	$\overline{DACK}$ High to $\overline{DRQ}$ Low	0		ns

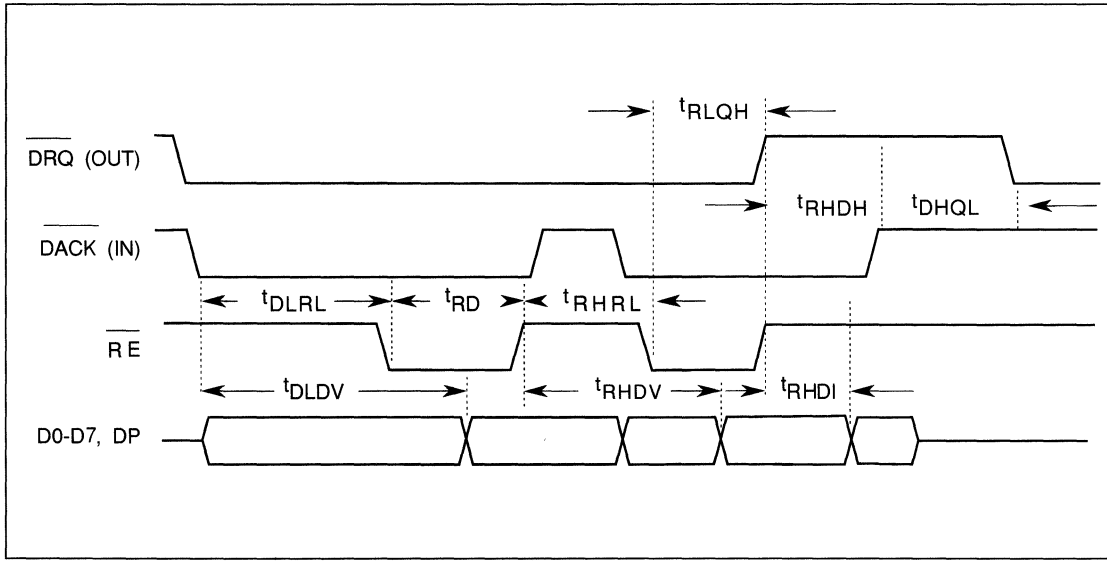


FIGURE 6-12. BURST DMA READ TIMING

6.1.13 INTRQ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tihrl	INTRQ High to $\overline{RE}$ Low	0		ns
tri	$\overline{RE}$ Pulse Width	180		ns
trhil	$\overline{RE}$ High to INTRQ Low	0	100	ns
tilih	INTRQ Low to INTRQ High	100		ns

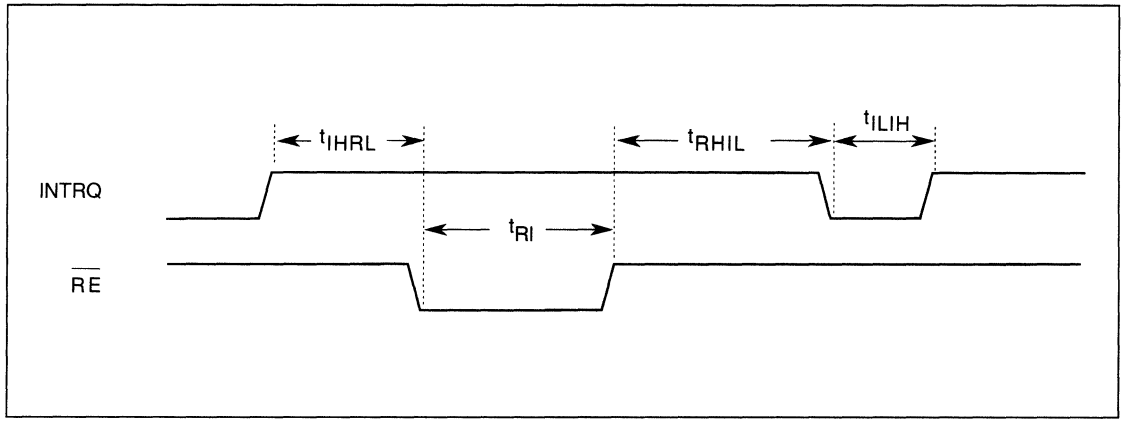


FIGURE 6-13. INTRQ TIMING

6.2 SCSI INTERFACE

6.2.1 Arbitration

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tbhbl	$\overline{BSY}$, $\overline{SEL}$ In High to $\overline{BSY}$ Out Low	12	16	cyc
tblio	$\overline{BSY}$ Out Low to BUS ID Out	-50	50	ns
tblsl	$\overline{BSY}$ Out Low to $\overline{SEL}$ Out Low	2.2		us

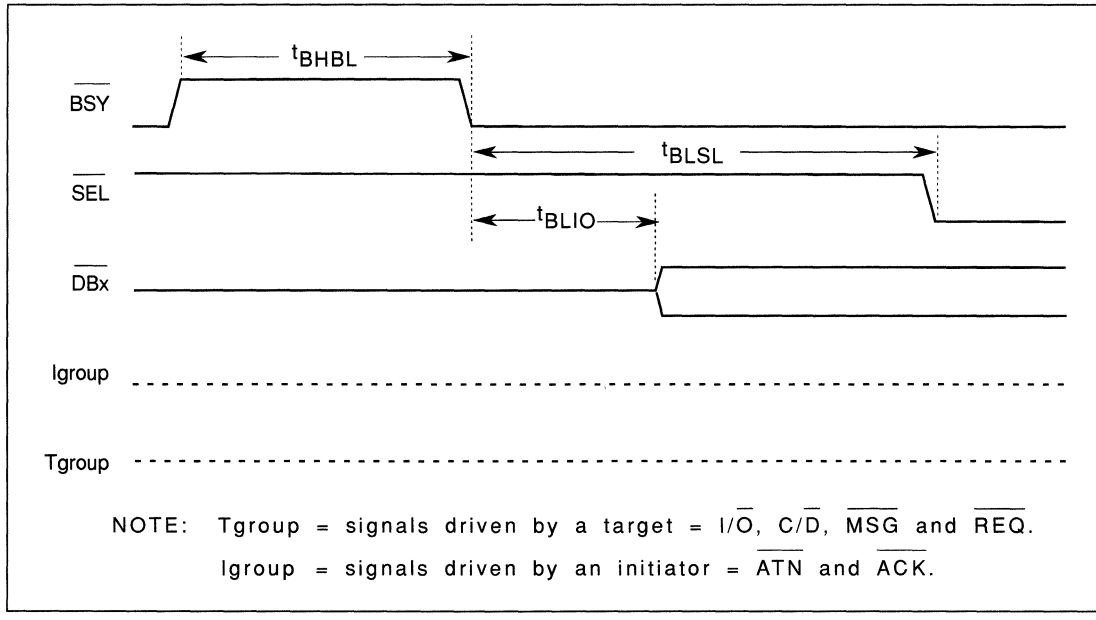


FIGURE 6-14. ARBITRATION TIMING

6.2.2 Selecting A Target (As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tsloo	$\overline{SEL}$ Out Low to "OR-ED" ID Out	1.2		us
tovao	"OR-ED" ID Out Valid To $\overline{ACK}$, $\overline{ATN}$ Out	100		ns
taobh	$\overline{ACK}$, $\overline{ATN}$ Out Valid To $\overline{BSY}$ Out High	100		ns
tbhbv	$\overline{BSY}$ Out High To $\overline{BSY}$ In Low Valid	400		ns
tblsh	$\overline{BSY}$ In Low to $\overline{SEL}$ Out High	100		ns

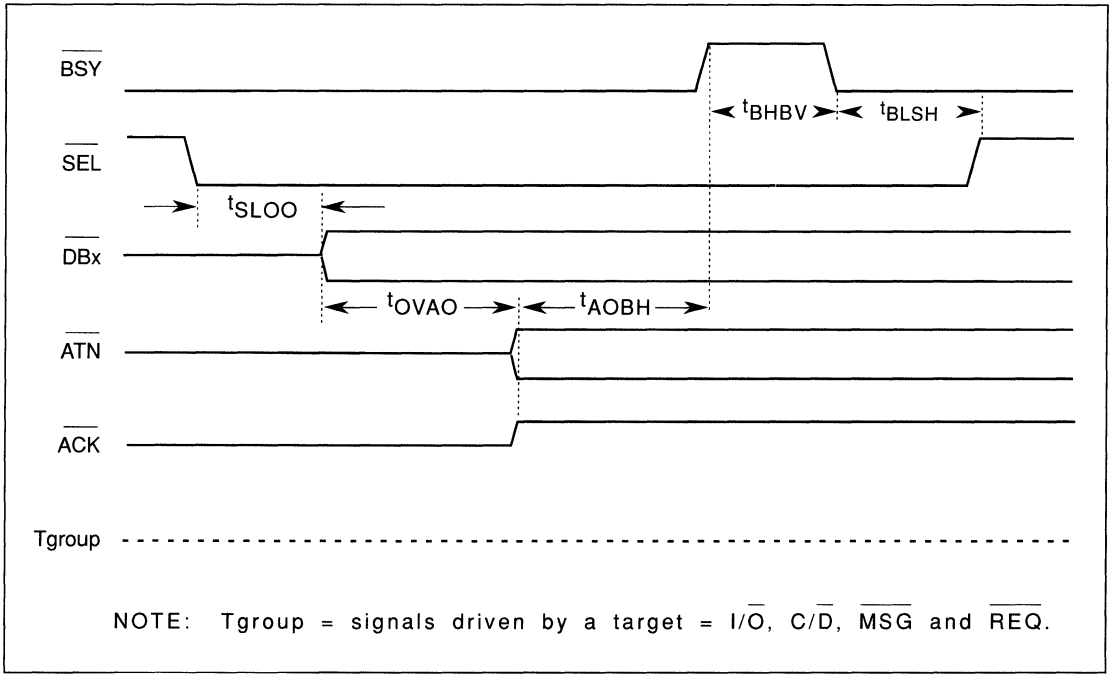


FIGURE 6-15. TIMING-INITIATOR SELECTING A TARGET

6.2.3 Response To Selection (As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslbh	$\overline{SEL}$ In Low to $\overline{BSY}$ In High	0		ns
tivbh	"OR-ED" ID Valid In To $\overline{BSY}$ In High	0		ns
tbhbl	$\overline{SEL}$ Low, ID Valid, $\overline{BSY}$ High To $\overline{BSY}$ Out Low	0.4	200	us
tbloi	$\overline{BSY}$ Out Low To "OR-ED" ID Invalid In	0		ns
tblsh	$\overline{BSY}$ Out Low to $\overline{SEL}$ In High	0		ns
tavsh	$\overline{ATN}$ Valid In to $\overline{SEL}$ In High	0		ns
tshio	$\overline{SEL}$ In High to Tgroup Out	100		ns

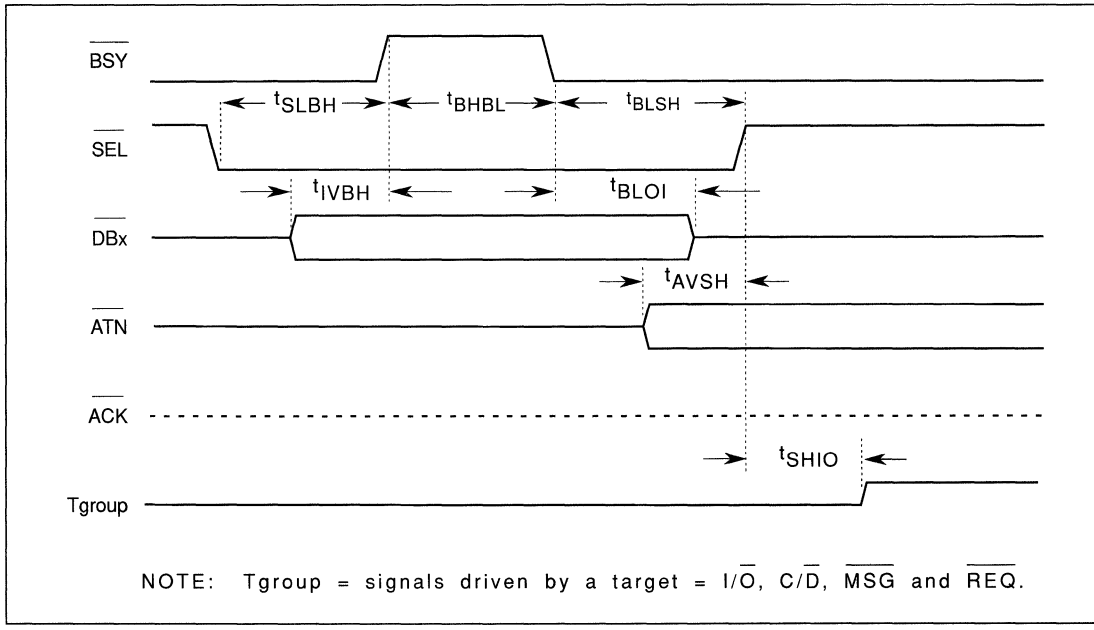


FIGURE 6-16. TIMING-TARGET RESPONSE

6.2.4 Reselecting An Initiator (As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tsloo	$\overline{SEL}$ Out Low to "OR-ED" ID Out	1.2		us
tovio	"OR-ED" ID Out Valid To I/O and Tgroup Out Valid	100		ns
tiobh	I/O and Tgroup Out Valid To $\overline{BSY}$ Out High	100		ns
tbhbv	$\overline{BSY}$ Out High To $\overline{BSY}$ In Low Valid	400		ns
tblsh	$\overline{BSY}$ In Low to $\overline{SEL}$ Out High	100		ns

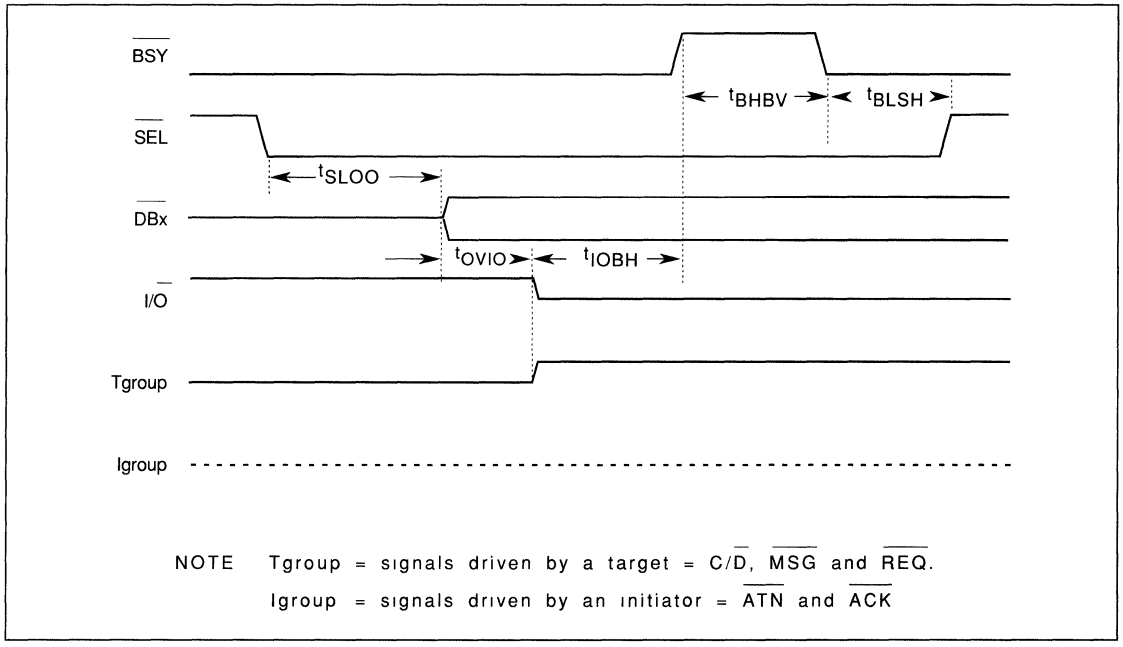
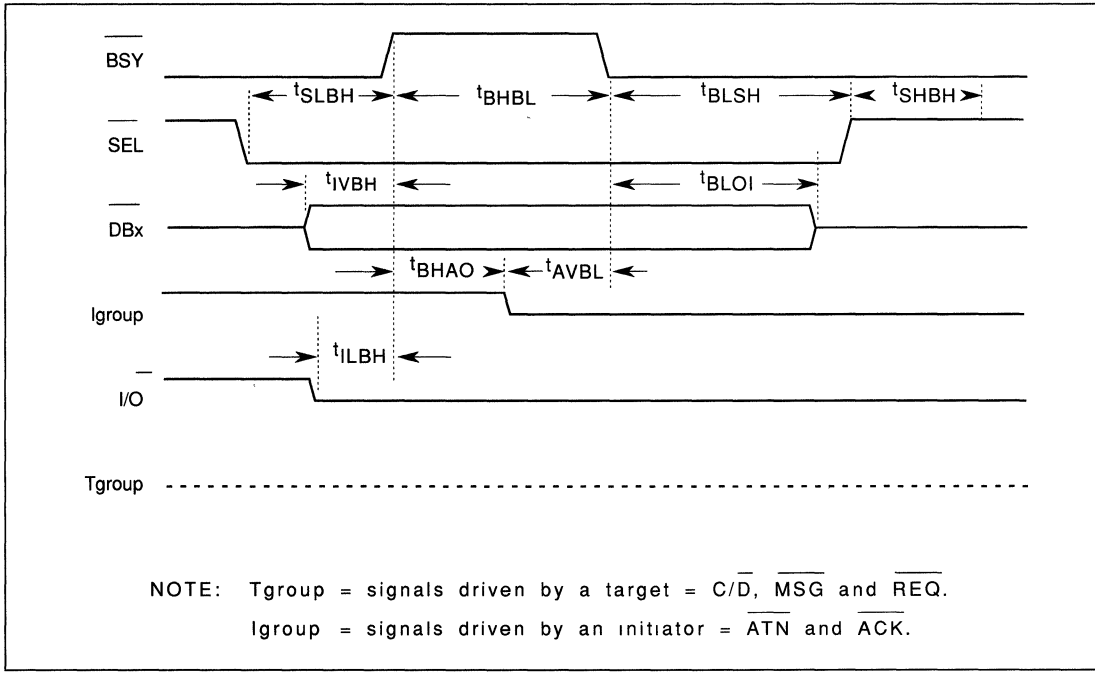


FIGURE 6-17. TIMING-RESELECTING A TARGET

6.2.5 Response To Reselection (As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslbh	$\overline{SEL}$ In Low to $\overline{BSY}$ In High	0		ns
tivbh	"OR-ED" ID Valid In To $\overline{BSY}$ In High	0		ns
tilbh	I/I- In Low to $\overline{BSY}$ In High	0		ns
tbhao	$\overline{SEL}$ Low, ID Valid, $\overline{BSY}$ High To Igroup Out	100		ns
tavbl	Igroup Valid Out to $\overline{BSY}$ Out Low	100		ns
tbhbl	$\overline{BSY}$ In High to $\overline{BSY}$ Out Low	0.4	200	ns
tbloi	$\overline{BSY}$ Out Low To "OR-ED" ID Invalid In	0		ns
tblsh	$\overline{BSY}$ Out Low to $\overline{SEL}$ In High	0		ns
tshbh	$\overline{SEL}$ In High to $\overline{BSY}$ Out High	0		ns

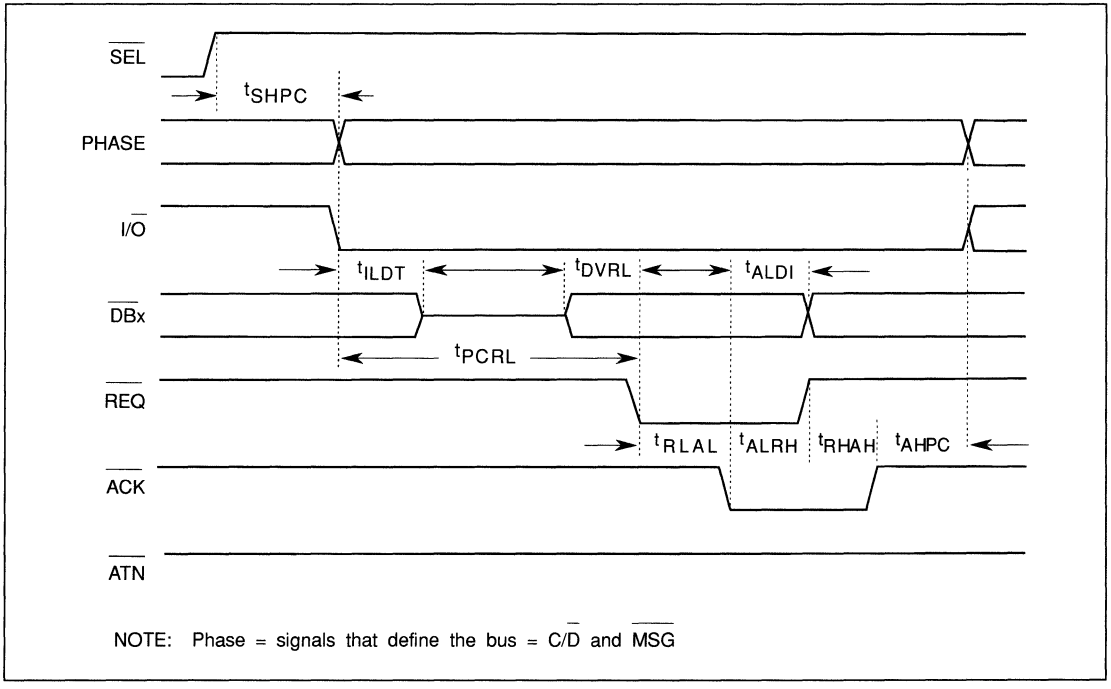


NOTE: Tgroup = signals driven by a target = C/D, MSG and REQ.
Igroup = signals driven by an initiator = ATN and ACK.

FIGURE 6-18. TIMING-RESELECTION AS INITIATOR

6.2.6 Receive Asynchronous Information Transfer In (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	$\overline{SEL}$ In High To Phase Change In	0		ns
tildt	$\overline{I/O}$ In Low To Data Bus Tri-state	0	125	ns
tpcrl	Phase Change In To $\overline{REQ}$ In Low	400		ns
tdvrl	Data Valid In To $\overline{REQ}$ In Low	0		ns
trlal	$\overline{REQ}$ In Low To $\overline{ACK}$ Out Low	0	175	ns
tadli	$\overline{ACK}$ Out Low To Data Invalid In	0		ns
talrh	$\overline{ACK}$ Out Low To $\overline{REQ}$ In High	0		ns
trhah	$\overline{REQ}$ In High To $\overline{ACK}$ Out High	0	175	ns
tahpc	$\overline{ACK}$ Out High To Phase Change In	0		ns

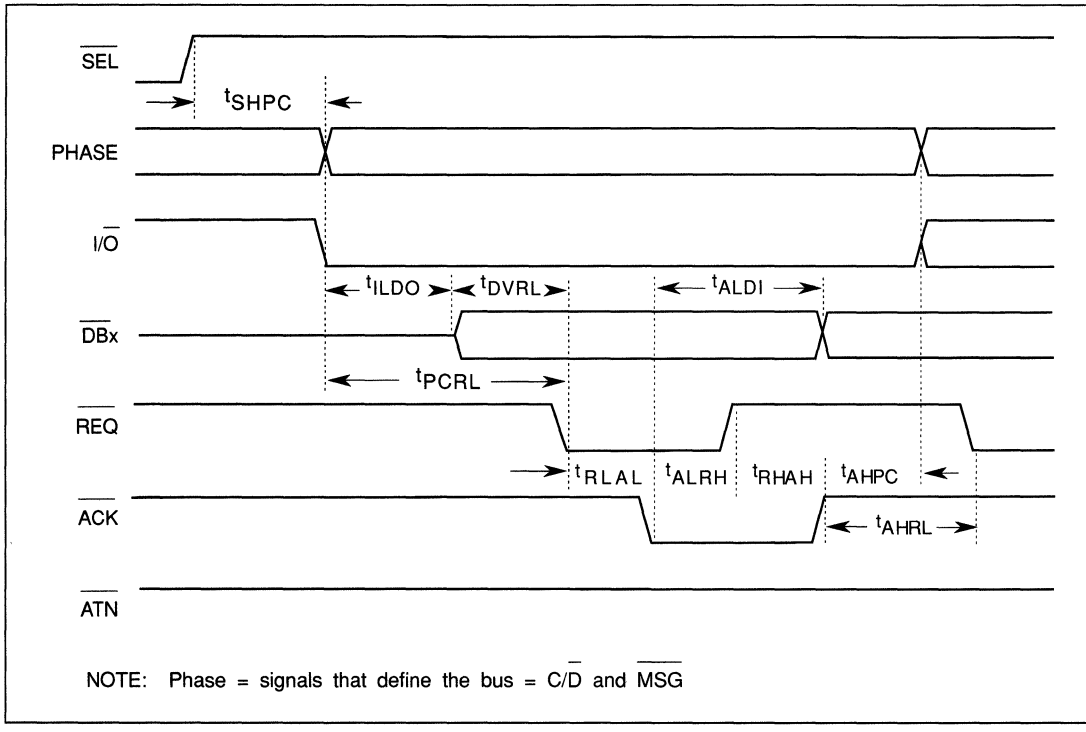


NOTE: Phase = signals that define the bus = C/D and MSG

FIGURE 6-19. TIMING-ASYNCHRONOUS TRANSFER IN AS INITIATOR

6.2.7 Send Asynchronous Information Transfer In (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	$\overline{SEL}$ In High To Phase Change Out	100		ns
tildo	$\overline{I/O}$ Out Low To Data Out	800		ns
tdvrl	Data Out Valid To $\overline{REQ}$ Out Low	55		ns
tpcrl	Phase Change Out To $\overline{REQ}$ Out Low	500		ns
trlal	$\overline{REQ}$ Out Low To $\overline{ACK}$ In Low	0		ns
talrh	$\overline{ACK}$ In Low To $\overline{REQ}$ Out High	0	175	ns
taldi	$\overline{ACK}$ In Low To Data Out Invalid	0		ns
trhah	$\overline{REQ}$ Out High To $\overline{ACK}$ In High	0		ns
tahpc	$\overline{ACK}$ In High To Phase Change Out	100		ns
tahrl	$\overline{ACK}$ In High To $\overline{REQ}$ Out Low	0	175	ns



NOTE: Phase = signals that define the bus = $\overline{C/D}$ and $\overline{MSG}$

FIGURE 6-20. TIMING-ASYNCHRONOUS TRANSFER IN AS TARGET

6.2.8 Send Asynchronous Information Transfer Out (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	$\overline{SEL}$ In High To Phase Change In	0		ns
tihdo	$\overline{I/O}$ In High To Data Out	0		ns
tpcrl	Phase Change In To $\overline{REQ}$ In Low	400		ns
trlal	$\overline{REQ}$ In Low To $\overline{ACK}$ Out Low	0	175	ns
tdval	Data Out Valid To $\overline{ACK}$ Out Low	55		ns
talrh	$\overline{ACK}$ Out Low To $\overline{REQ}$ In High	0		ns
trhah	$\overline{REQ}$ In High To $\overline{ACK}$ Out High	0	175	ns
trhdi	$\overline{REQ}$ In High To Data Out Invalid	0		ns
tahpc	$\overline{ACK}$ Out High To Phase In Change	0		ns

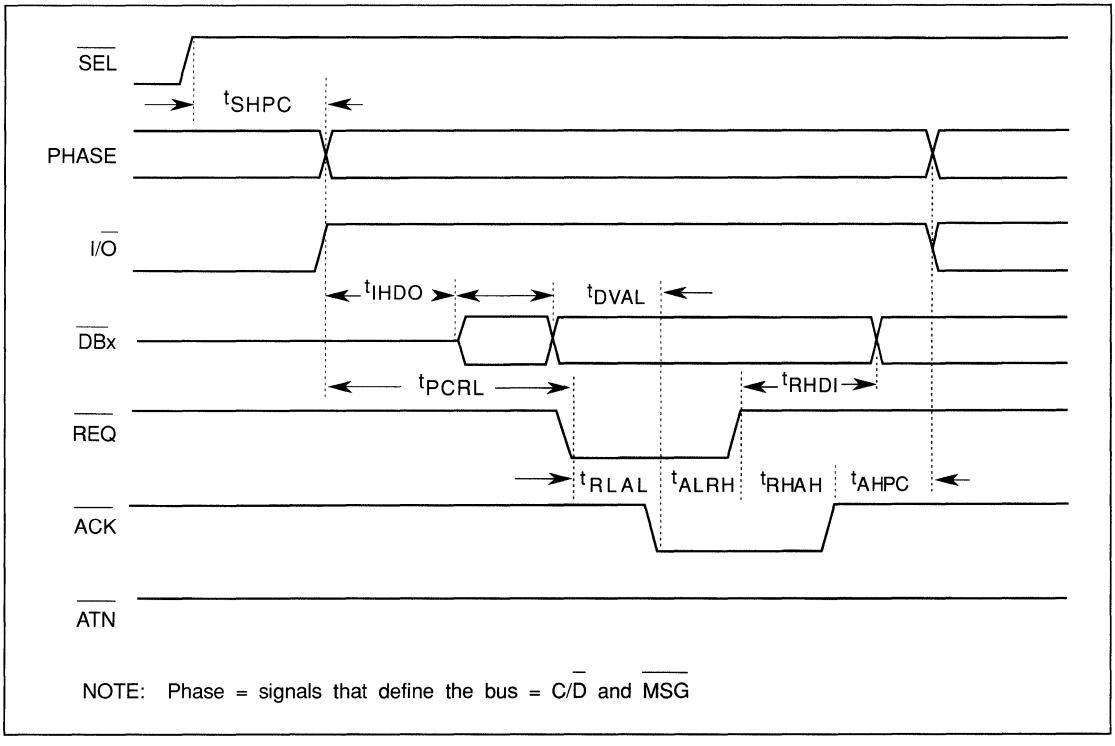
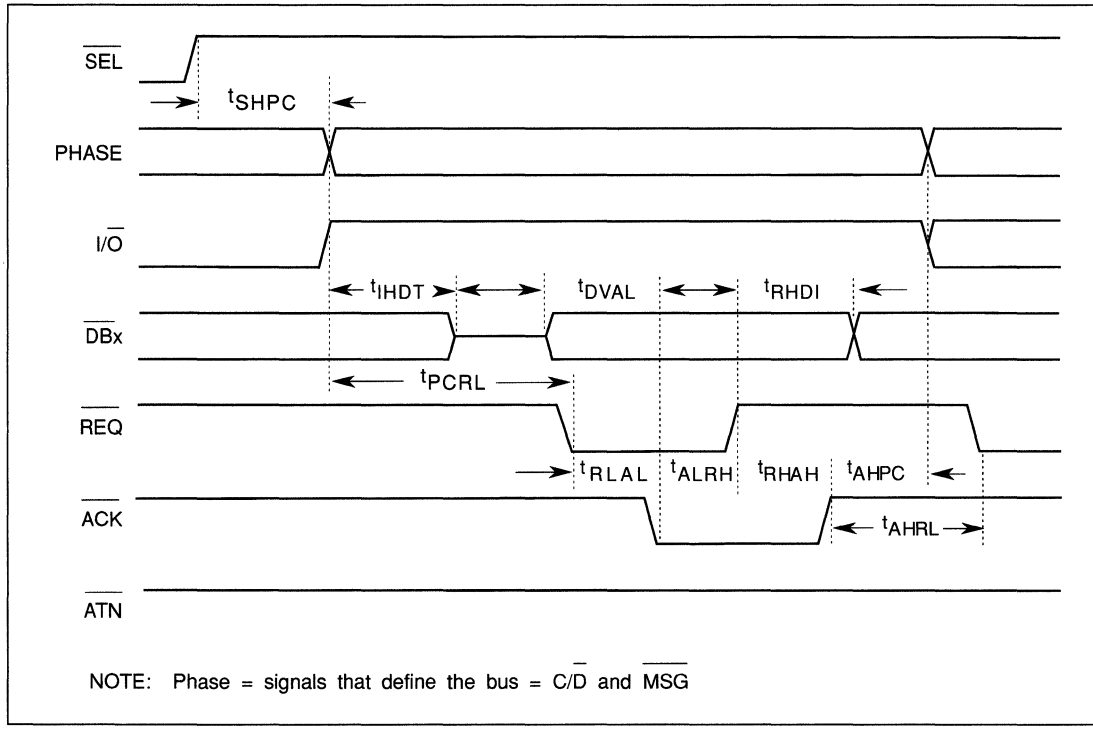


FIGURE 6-21. TIMING-ASYNCHRONOUS TRANSFER OUT AS INITIATOR

6.2.9 Receive Asynchronous Information Transfer Out (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	$\overline{SEL}$ In High To Phase Change Out	100		ns
tihdt	$\overline{I/O}$ Out High To Data Bus Tri-state		0	ns
tpcrl	Phase Change To $\overline{REQ}$ Out Low	500		ns
trlal	$\overline{REQ}$ Out Low To $\overline{ACK}$ In Low	0		ns
tdval	Data In Valid To $\overline{ACK}$ In Low	0		ns
talrh	$\overline{ACK}$ In Low To $\overline{REQ}$ Out High	0	175	ns
trhdi	$\overline{REQ}$ Out High To Data In Invalid	0		ns
trhah	$\overline{REQ}$ Out High To $\overline{ACK}$ In High	0		ns
tahpc	$\overline{ACK}$ In High To Phase Change Out	0		ns
tahrl	$\overline{ACK}$ In High To $\overline{REQ}$ Out Low	0	175	ns



NOTE: Phase = signals that define the bus = C/D and MSG

FIG.6-22. TIMING-RECEIVE ASYNCHRONOUS TRANSFER OUT AS TARGET

6.2.10 Receive Synchronous Information Transfer In (5 and 10 Mb/s) (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrl	Data Valid In To $\overline{REQ}$ In Low	0		ns
trldi	$\overline{REQ}$ In Low To Data Invalid	30		ns
trcyc	$\overline{REQ}$ In Cycle Time	100		ns
trlrh	$\overline{REQ}$ In Low To $\overline{REQ}$ In High	30		ns
trhrl	$\overline{REQ}$ In High To $\overline{REQ}$ In Low	30		ns
talah	$\overline{ACK}$ Out Low To $\overline{ACK}$ Out High (1)	1-10 ns		Tcyc
tahal	$\overline{ACK}$ Out High To $\overline{ACK}$ Out Low (1)	1-10 ns		Tcyc
tahpc	$\overline{ACK}$ Out High To Phase Change	0		ns

Parameters tshpc, tildt, and tpcrl are also applicable and are identical to those in 6.2.6.
(1) Tahal + Talah = 2*Tcyc

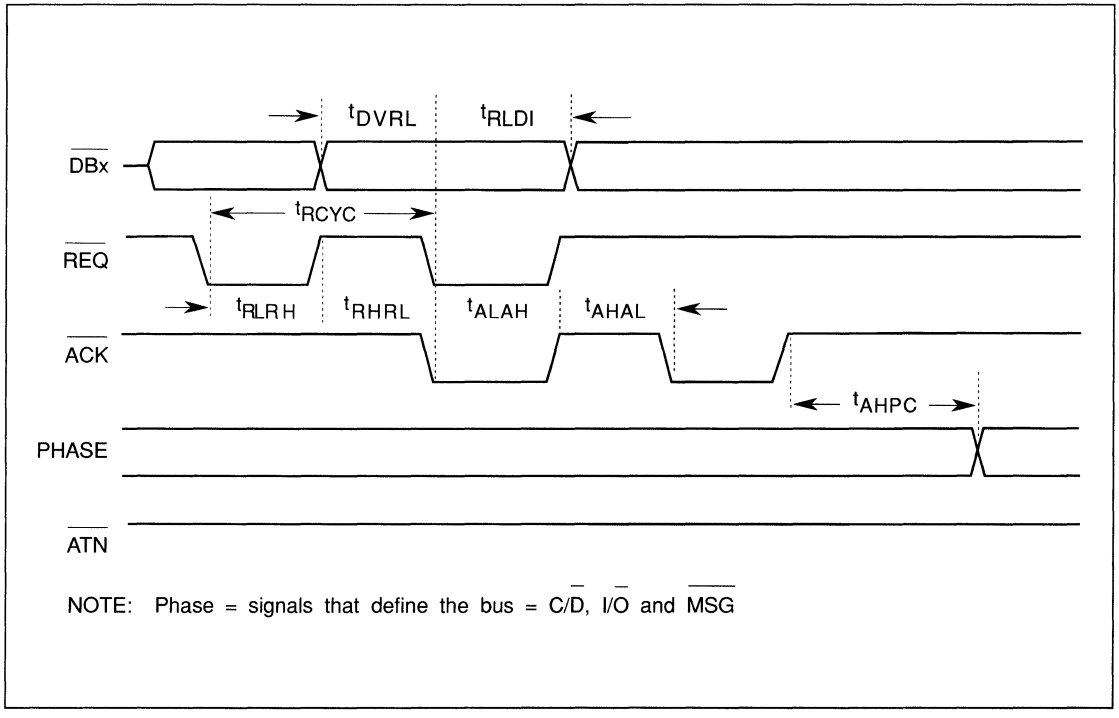


FIG.6-23.TIMING-RECEIVE SYNCHRONOUS TRANSFER IS AN INITIATOR

6.2.11 Send Synchronous Information Transfer In (5 Mb/s) (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrl	Data Valid Out To $\overline{REQ}$ Out Low	55		ns
trldi	$\overline{REQ}$ Out Low To Data Invalid	100		ns
trlrh	$\overline{REQ}$ Out Low To $\overline{REQ}$ Out High (1)	1-10 ns		Tcyc
trhrl	$\overline{REQ}$ Out High To $\overline{REQ}$ Out Low (1)	1-10 ns		Tcyc
tacyc	$\overline{ACK}$ In Cycle Time	200		ns
talah	$\overline{ACK}$ In Low To $\overline{ACK}$ In High	50		ns
tahal	$\overline{ACK}$ In High To $\overline{ACK}$ In Low	50		ns
tahpc	$\overline{ACK}$ In High To Phase Change Out	0		ns

Parameters tshpc, tildo, and tpcrl are also applicable and are identical to those in 6.2.7.
(1) Trhrl + Trlrh = 2*Tcyc

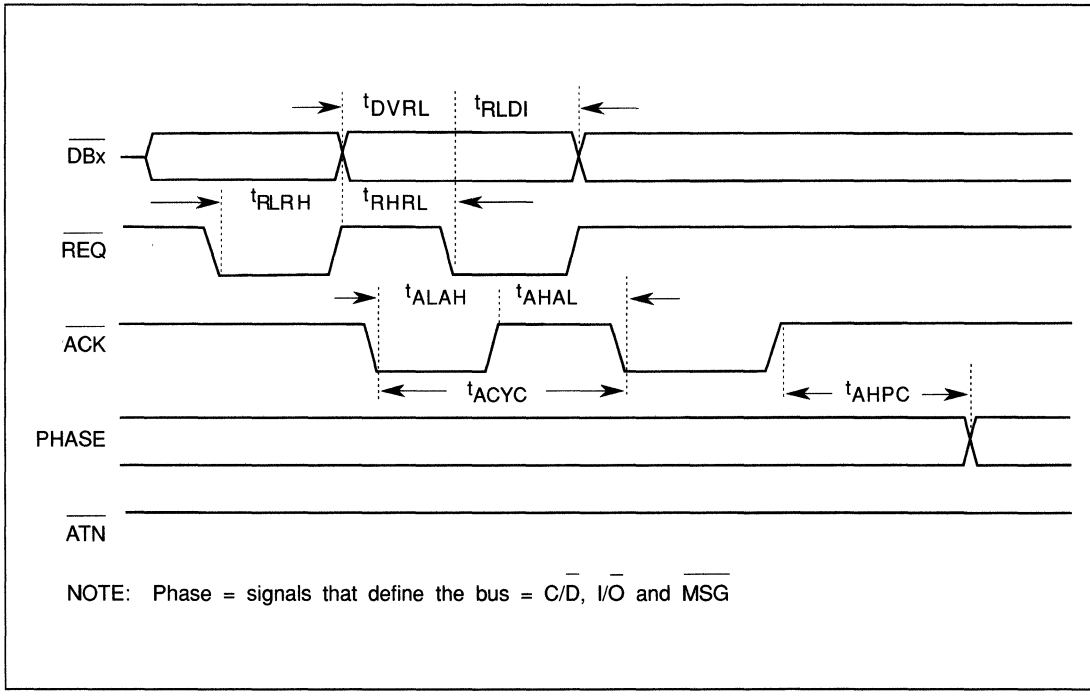


FIGURE 6-24. TIMING-SEND SYNCHRONOUS TRANSFER IN AS TARGET

6.2.12 Send Synchronous Information Transfer In (10 Mb/s) (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrl	Data Valid Out To $\overline{REQ}$ Out Low	25		ns
rtrldi	$\overline{REQ}$ Out Low To Data Invalid	35		ns
trlrh	$\overline{REQ}$ Out Low To $\overline{REQ}$ Out High (1)	1-10 ns		Tcyc
trhrl	$\overline{REQ}$ Out High To $\overline{REQ}$ Out Low (1)	1-10 ns		Tcyc
tacyc	$\overline{ACK}$ In Cycle Time	100		ns
talah	$\overline{ACK}$ In Low To $\overline{ACK}$ In High	30		ns
tahal	$\overline{ACK}$ In High To $\overline{ACK}$ In Low	30		ns
tahpc	$\overline{ACK}$ In High To Phase Change Out	0		ns

Parameters tshpc, tildo, and tpcrl are also applicable and are identical to those in 6.2.7.
(1) Trhrl + Trlrh = 2*Tcyc

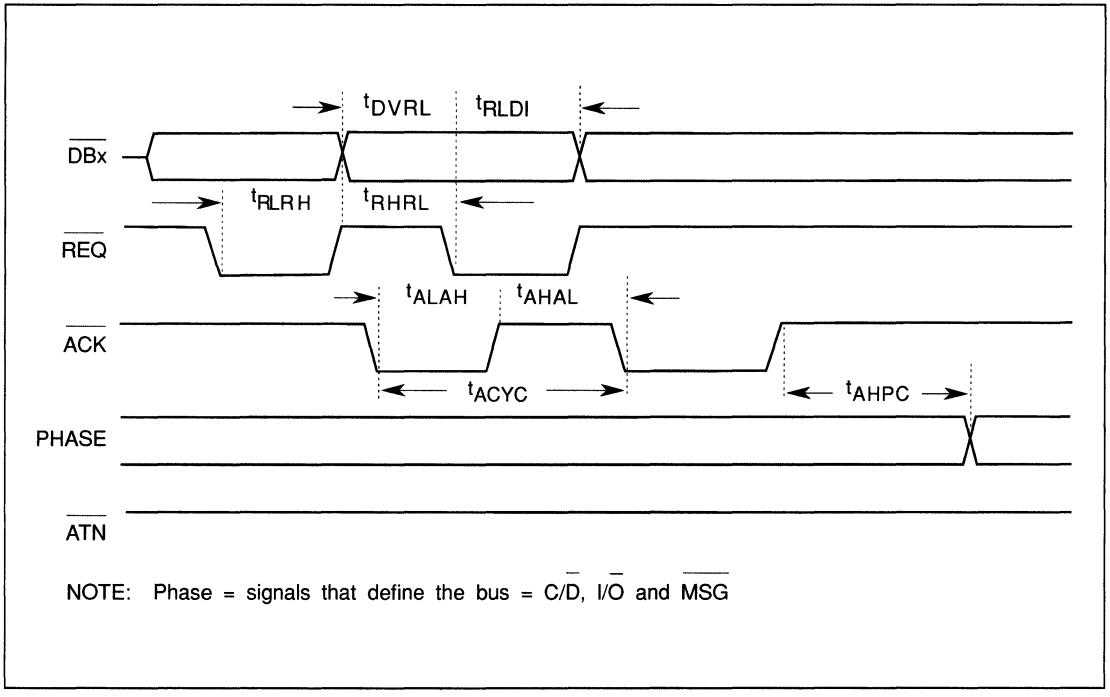


FIGURE 6-25. TIMING-SEND SYNCHRONOUS TRANSFER IN AS TARGET

6.2.13 Send Synchronous Information Transfer Out (5 Mb/s) (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdval	Data Valid Out To $\overline{ACK}$ Out Low	55		ns
taldi	$\overline{ACK}$ Out Low To Data Invalid	100		ns
trcyc	$\overline{REQ}$ In Cycle Time	200		ns
trlrh	$\overline{REQ}$ In Low To $\overline{REQ}$ In High	50		ns
trhrl	$\overline{REQ}$ In High To $\overline{REQ}$ In Low	50		ns
talah	$\overline{ACK}$ Out Low To $\overline{ACK}$ Out High (1)	1-10 ns		Tcyc
tahal	$\overline{ACK}$ Out High To $\overline{ACK}$ Out Low (1)	1-10 ns		Tcyc
tahpc	$\overline{ACK}$ Out High To Phase Change In	0		ns

Parameters tshpc, tihdo, and tpcrl are also applicable and are identical to those in 6.2.8.
(1) Tahal + Talah = 2*Tcyc

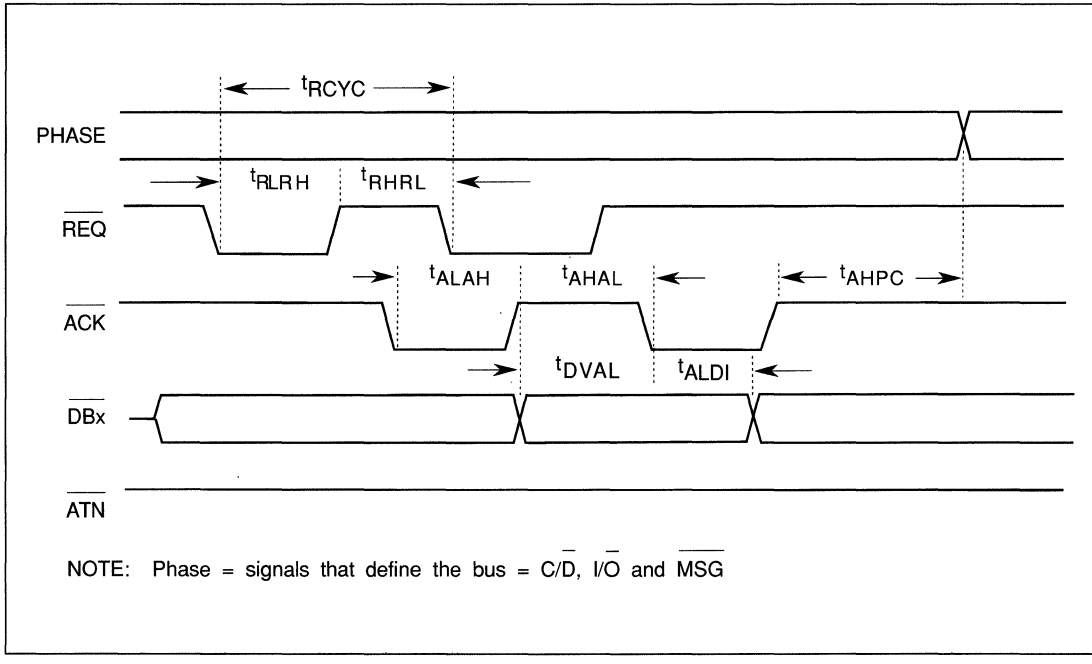


FIG. 6-26. TIMING-SEND SYNCHRONOUS TRANSFER OUT AS INITIATOR

6.2.14 Send Synchronous Information Transfer Out (10 Mb/s) (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdval	Data Valid Out To $\overline{ACK}$ Out Low	25		ns
taldi	$\overline{ACK}$ Out Low To Data Invalid	35		ns
trcyc	$\overline{REQ}$ In Cycle Time	100		ns
trlrh	$\overline{REQ}$ In Low To $\overline{REQ}$ In High	30		ns
trhrl	$\overline{REQ}$ In High To $\overline{REQ}$ In Low	30		ns
talah	$\overline{ACK}$ Out Low To $\overline{ACK}$ Out High (1)	1-10 ns		Tcyc
tahal	$\overline{ACK}$ Out High To $\overline{ACK}$ Out Low (1)	1-10 ns		Tcyc
tahpc	$\overline{ACK}$ Out High To Phase Change In	0		ns

Parameters tshpc, tihdo, and tpcrl are also applicable and are identical to those in 6.2.8.
(1) Tahal + Talah = 2*Tcyc

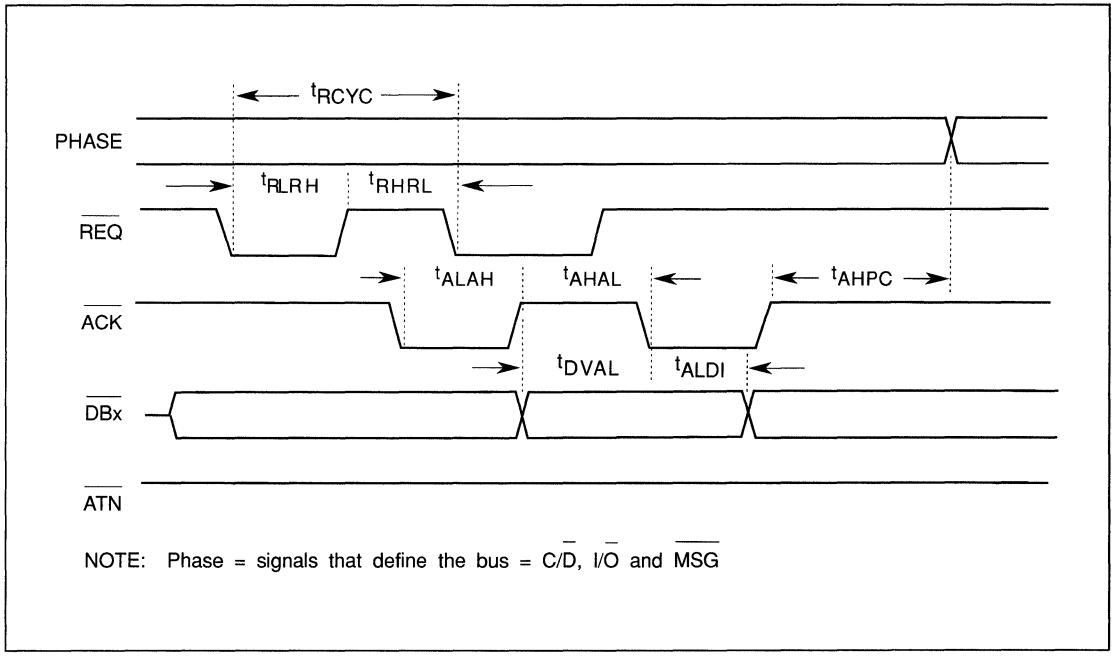


FIG. 6-27. TIMING-SEND SYNCHRONOUS TRANSFER OUT AS INITIATOR

6.2.15 Receive Synchronous Information Transfer Out (5 and 10 Mb/s) (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdval	Data Valid In To $\overline{ACK}$ In Low	0		ns
taldi	$\overline{ACK}$ In Low To Data Invalid	30		ns
trlrh	$\overline{REQ}$ Out Low To $\overline{REQ}$ Out High (1)	1-10 ns		Tcyc
trhrl	$\overline{REQ}$ Out High To $\overline{REQ}$ Out Low (1)	1-10 ns		Tcyc
tacyc	$\overline{ACK}$ In Cycle Time	100		ns
talah	$\overline{ACK}$ In Low To $\overline{ACK}$ In High	30		ns
tahal	$\overline{ACK}$ In High To $\overline{ACK}$ In Low	30		ns
tahpc	$\overline{ACK}$ In High To Phase Change Out	0		ns

Parameters tshpc, tihdt, and tpcrl are also applicable and are identical to those in 6.2.9.
(1) Trhrl + Trlrh = 2*Tcyc

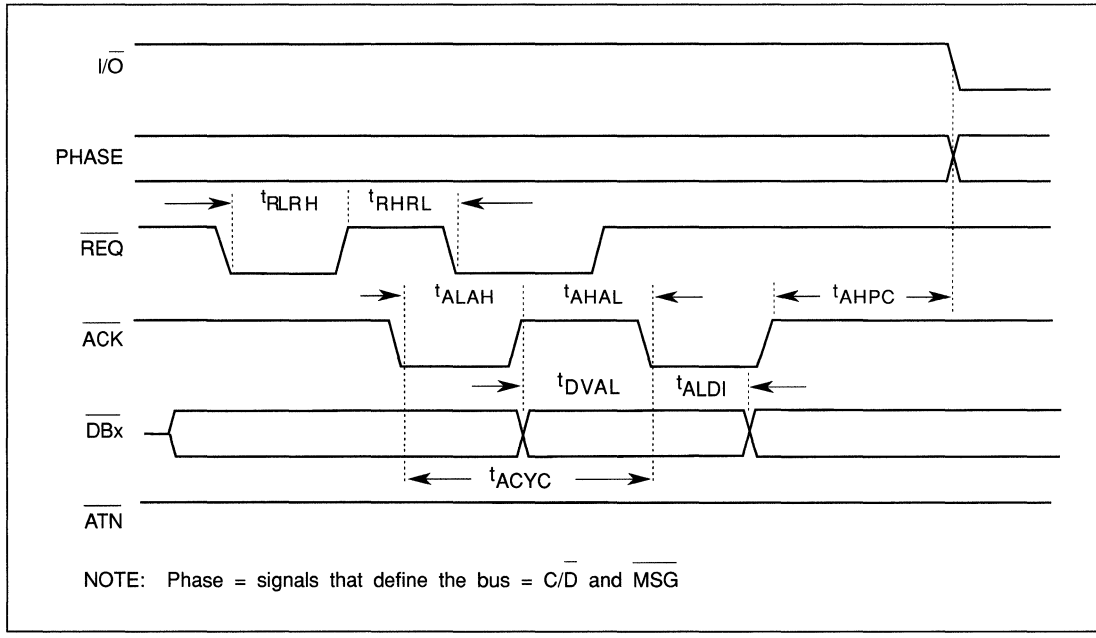


FIG. 6-28. TIMING-RECEIVE SYNCHRONOUS TRANSFER OUT AS TARGET

6.2.16 Arbitration To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslbh	$\overline{SEL}$ In Low To $\overline{BSY}$ High, Data Tri-state		6+50 ns	Tcyc

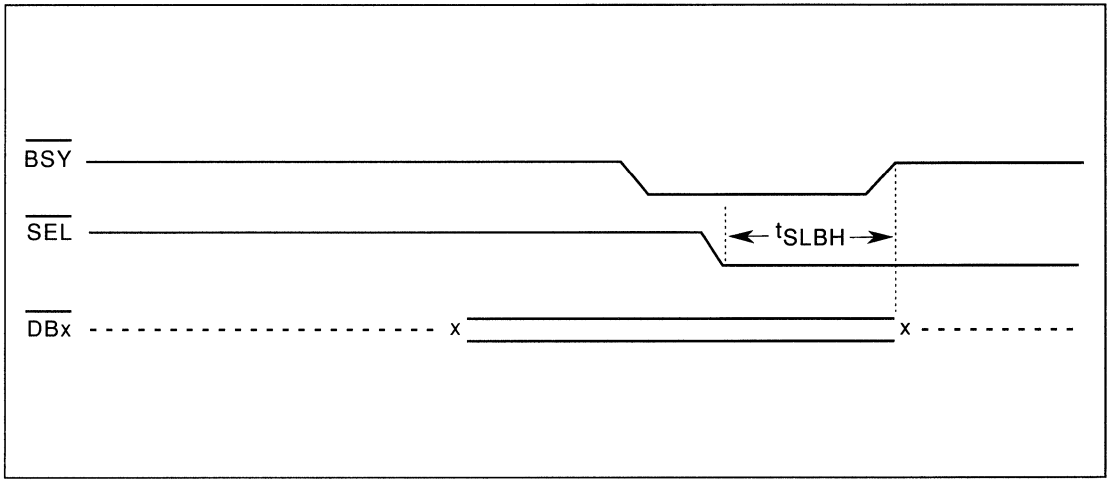


FIGURE 6-29. ARBITRATION TO BUS FREE TIMING

6.2.17 Selection (As An Initiator) Or Reselection (As A Target) To Bus Free (Selection Timeout)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
ttadc	Timeout Or Abort To Data Bus Cleared	0		ns
tdcsh	Data BUS Cleared To $\overline{SEL}$ Out High	201		us
tshdt	$\overline{SEL}$ Out High To Data Bus Tri-state		800	ns
tshih	$\overline{SEL}$ Out High To cntl Tri-state		800	ns

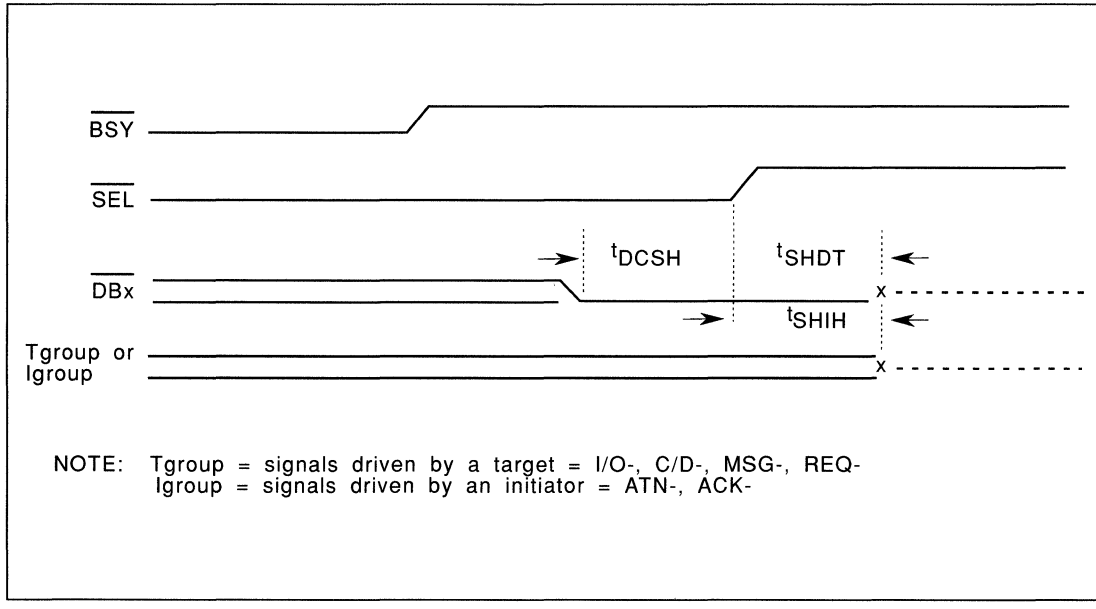


FIGURE 6-30. TIMING-SELECTION TO BUS FREE

6.2.18 Connected-As-An-Initiator To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tbhdt	$\overline{BSY}$ In High To Data Bus Tri-state		8+75 ns	Tcyc
tbhgt	$\overline{BSY}$ In High To Igroup Tri-state		8+75 ns	Tcyc

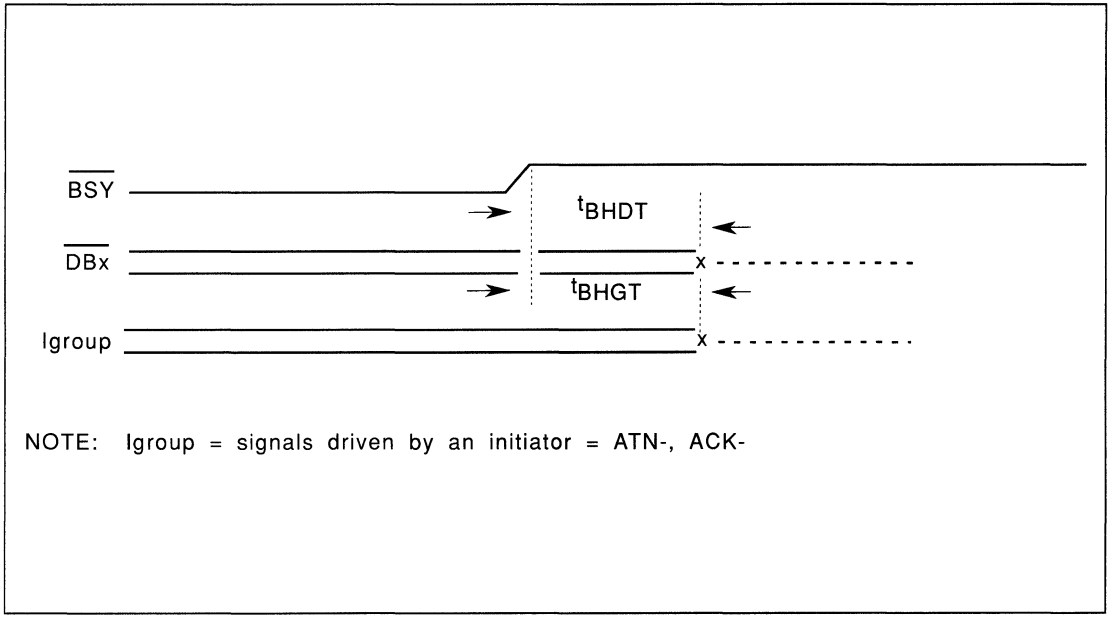


FIGURE 6-31. TIMING-INITIATOR TO BUS FREE

6.2.19 Connected-As-A-Target To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tbhdt	$\overline{\text{BSY}}$ Out High To Data Bus Tri-state		8+75 ns	Tcyc
tbhgt	$\overline{\text{BSY}}$ Out High To Tgroup Tri-state		8+75 ns	Tcyc

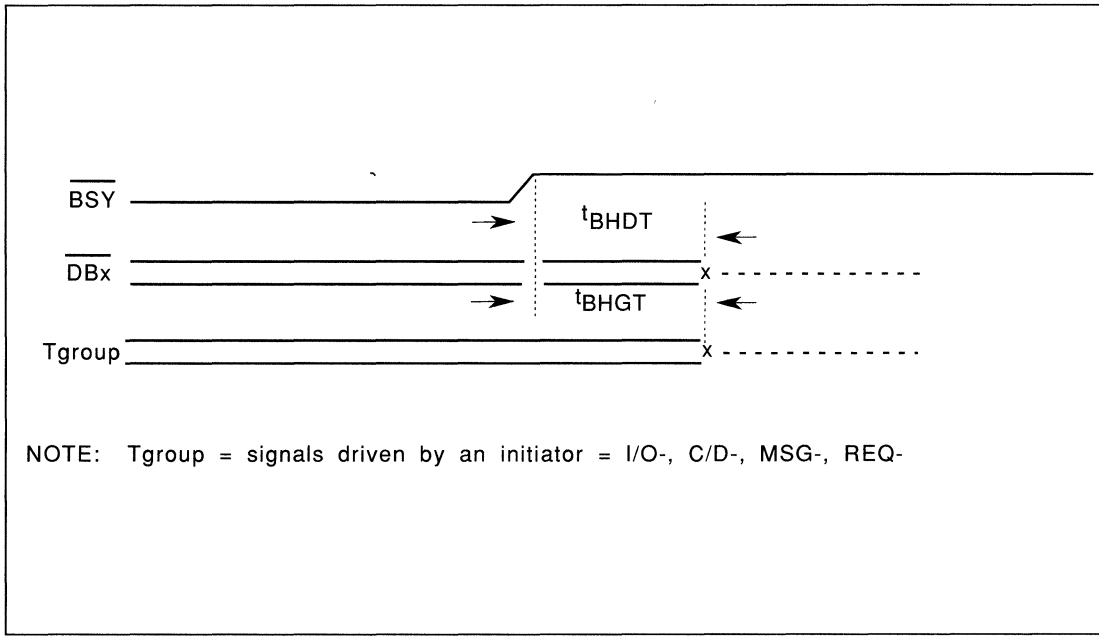


FIGURE 6-32. TIMING-TARGET TO BUS FREE