ICS90C64

Dual Video/Memory

Clock Generator

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

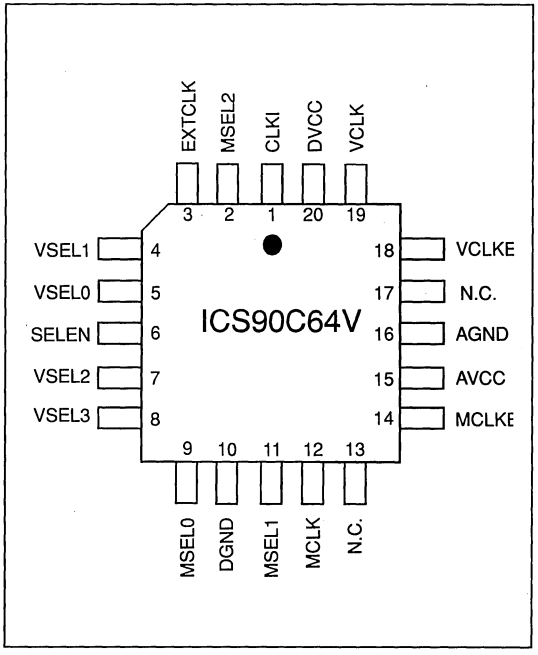
PREFACE

The Integrated Circuit Systems ICS90C64 dual video/memory clock generator was designed exclusively to work with Western Digital video graphics chips.

Because you get optimum video subsystem performance when you use this video/memory clock generator with the Western Digital video graphics chips, we have included the ICS90C64 in our databook.

You can contact Integrated Circuit Systems at the following address:

Integrated Circuit Systems, Inc.
Valley Forge Corporate Center
2626 Van Buren Ave., P.O. Box 968
Valley Forge, PA 19482
Phone: (215) 666-1900
Fax: (215) 666-1099



20-PIN PLCC DIAGRAM

1.0 INTRODUCTION

The Integrated Circuit Systems ICS90C64 is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

1.1 DESCRIPTION

The Integrated Circuit Systems Video Graphics Array Clock Generator (ICS90C64) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of 15 internally generated frequencies or one external input. The selection of the video dot clock frequency is done through four inputs.

- VSEL0
- VSEL1
- VSEL2
- VSEL3

VSEL0 and VSEL1 are latched by the SELEN signal. VSEL2 and VSEL3 are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

11

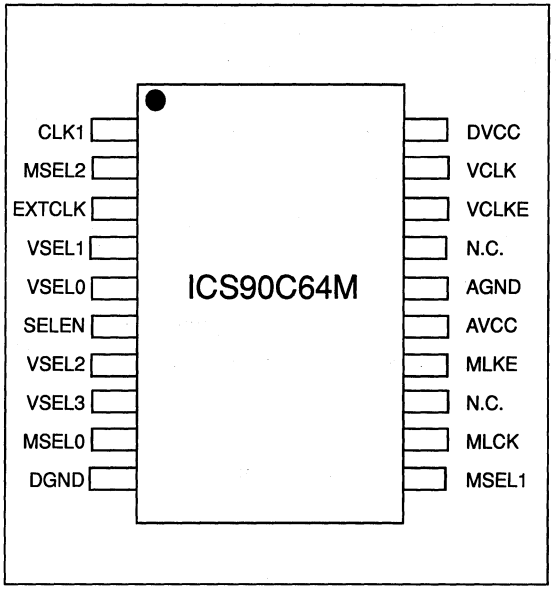
The input and truth table have been designed to allow a direct connection to one of the many Western Digital VGA controllers or 8514/A chip sets.

The MCLK output is one of eight internally generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz Input frequency.

The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

1.2 FEATURES

- Dual Clock generator for the IBM compatible Western Digital Video Graphics Array (VGA) LSI devices, and 8514/A chip sets.
- Integral loop filter components. Reduces cost and phase jitter.
- Generates 15 video clock frequencies (including 25.175 and 28.322 MHz) derived from a 14.318 MHz system clock reference frequency.
- On-chip generation of eight memory clock frequencies.
- Video clock is selectable among the 15 internally generated clocks and one external clock.
- CMOS technology.



20-PIN S.O.DIAGRAM

- Backward compatibility to the WD90C63 and WD90C61 device.
- Available in a 20-pin PLCC, S.O., and DIP packages.

Ordering Information

ICS90C64V (PLCC Package)
ICS90C64M (S.O. Package)
ICS90C64N (DIP Package)

Note: ICS90C64N (DIP) pinout is identical to ICS90C64M (S.O.) pinout.

2.0 ICS90C64 VGA INTERFACE

The ICS90C64 has two system interfaces: System Bus and VGA Controller, as well as analog filters and seven user programmable inputs. Figure 2-1 shows how the Integrated Circuit Systems VGA Clock ICS90C64 is connected to a VGA controller. Western Digital VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs VCLK1 and VCLK2 to outputs. These outputs are used to select the required video frequency.

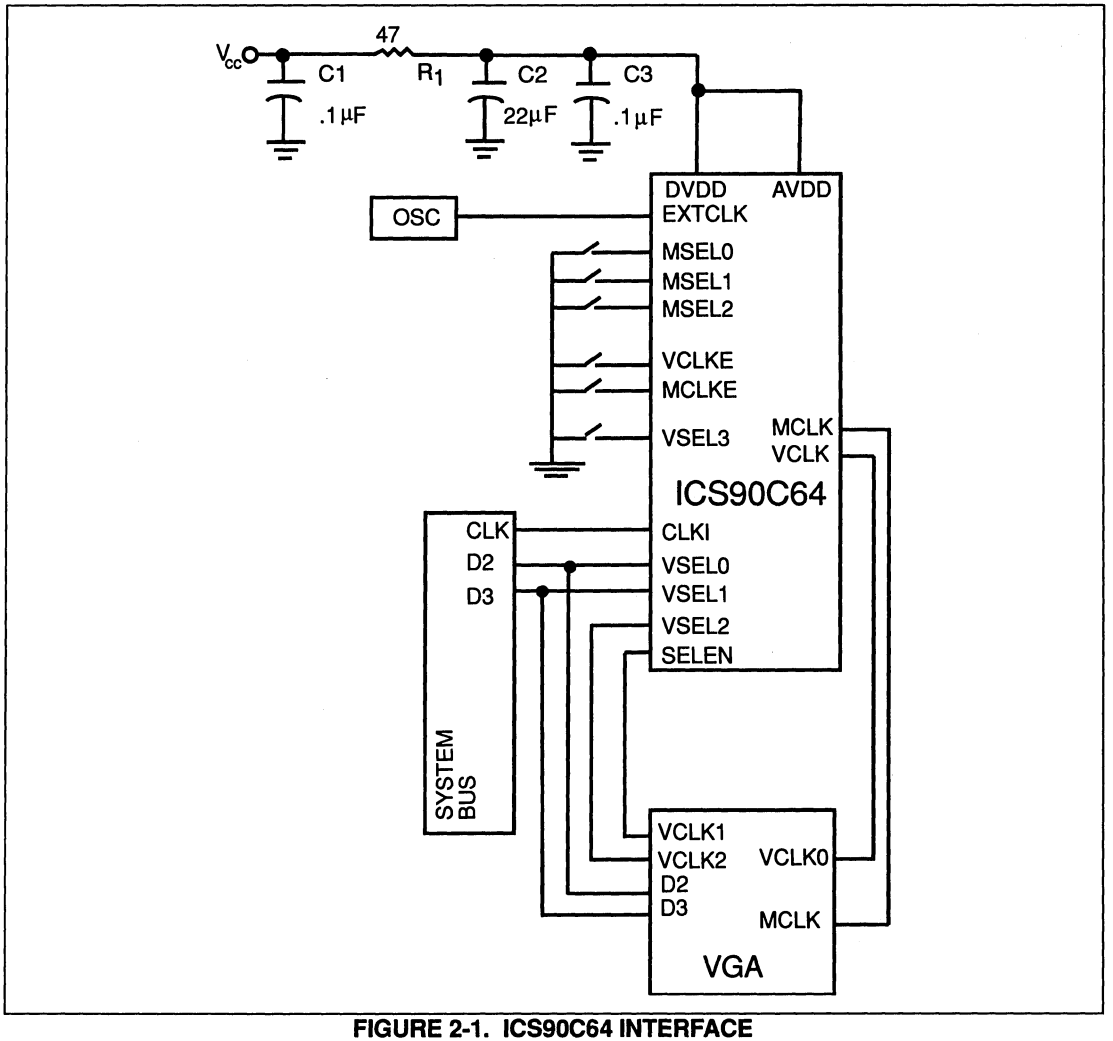


FIGURE 2-1. ICS90C64 INTERFACE

Note:
C_3 should be placed as close as possible to the ICS90C64 AVDD pin

2.1 SYSTEM BUS INPUTS

The system bus inputs are:

- CLK1
- VSEL0
- VSEL1

The ICS90C64 uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

2.2 INPUTS FROM VGA CONTROLLER

The VGA controller input the the ICS90C64 is:

- SELEN

The ICS90C64 is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, VSEL2, and VSEL3. The signals VSEL2 and VSEL3 may be supplied by the VGA controller as is the case in Western Digital VGA controllers. The inputs VSEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital VGA controllers during I/O writes to internal register 3C2h.

Note: Only VSEL0 and VSEL1 are latched with signal SELEN.

2.3 OUTPUTS TO VGA CONTROLLER

The outputs from the ICS90C64 to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

2.4 ANALOG FILTERS

The analog filters are integral to the ICS90C64 device. No external components are required. This feature reduces PC board space requirements and component costs. Phase jitter is reduced as externally generated noise cannot easily influence the phase locked loop filter.

2.5 USER DEFINABLE INPUTS

The user definable inputs are:

- EXTCLK
- VCLKE, MCLKE
- MSEL0-2
- VSEL2, VSEL3

EXTCLK is an additional input that may be internally routed to the VCLK output. This additional input is useful for supporting modes that require frequencies not provided by the ICS90C64.

VCLKE and MCLKE are the output enable signals for VCLK and MCLK. When low the respective output is tristated.

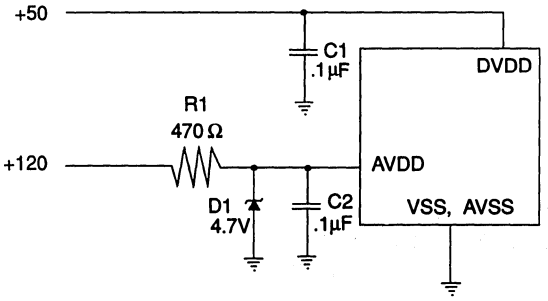
MSEL0-2 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pullup resistors.

VSEL2 and VSEL3 are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

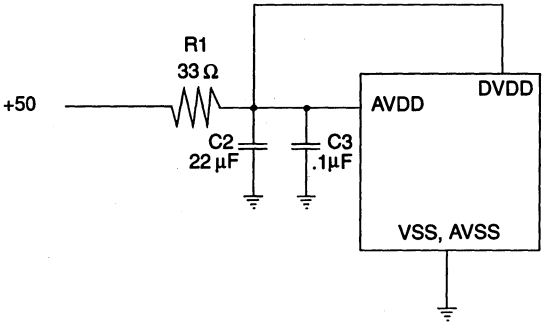
VSEL2 and VSEL3 have internal pullups.

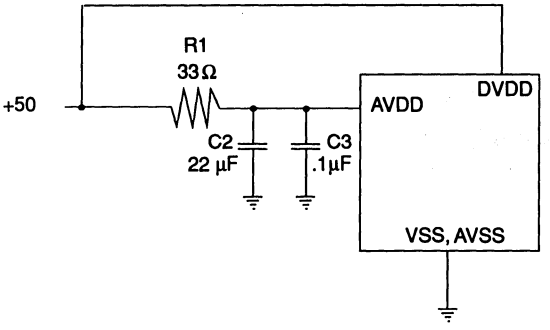
2.6 POWER CONSIDERATIONS

The **ICS90C64** product requires an Avdd supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 volt power quality is not only dependent on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 volts by deriving it from the +12 volt supply by using a Zener diode and dropping resistor. A 470 ohm resistor and 5.1 volt Zener diode is the least costly way to accomplish this. A 0.047 to 0.1 microfarad bypass capacitor tied from Avdd to Avss insures good high frequency decoupling of this point.



Laptop and notebook computers have entirely different problems with power. Typically they have no +12 volt supply, however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise generating components. Most systems provide power that is clean enough to allow for jitter free Dual Video/Memory Clock performance if the +5 volt supply is decoupled with a 33 ohm resistor and 22 microfarad Tantalum capacitor. Avdd is not particularly sensitive to supply voltage and will work fine at 4.1 volts over the full frequency range of the ICS90C64, so drop across the decoupling resistor is not a problem. Digital inputs that are desired to be held at a static logical high level should not be tied to +5 volts as this will result in excessive current drain through the ESD protection diode. The internal pullup resistors will adequately keep these inputs high.





11

VSEL				
3	2	1	0	VCLK FREQUENCY (MHz)
0	0	0	0	30.0
0	0	0	1	77.25
0	0	1	0	EXTCLK
0	0	1	1	80.0
0	1	0	0	31.5
0	1	0	1	36.0
0	1	1	0	75.0
0	1	1	1	50.0
1	0	0	0	40.0
1	0	0	1	50.0
1	0	1	0	32.0
1	0	1	1	44.9
1	1	0	0	25.175
1	1	0	1	28.322
1	1	1	0	65.0
1	1	1	1	36.0

TABLE 1-1. VCLK SELECTION

MSEL			
2	1	0	MCLK FREQUENCIES (MHz)
0	0	0	33.0
0	0	1	49.218
0	1	0	60.0
0	1	1	30.5
1	0	0	41.612
1	0	1	37.5
1	1	0	36.0
1	1	1	44.296

TABLE 1-2. MCLK SELECTION

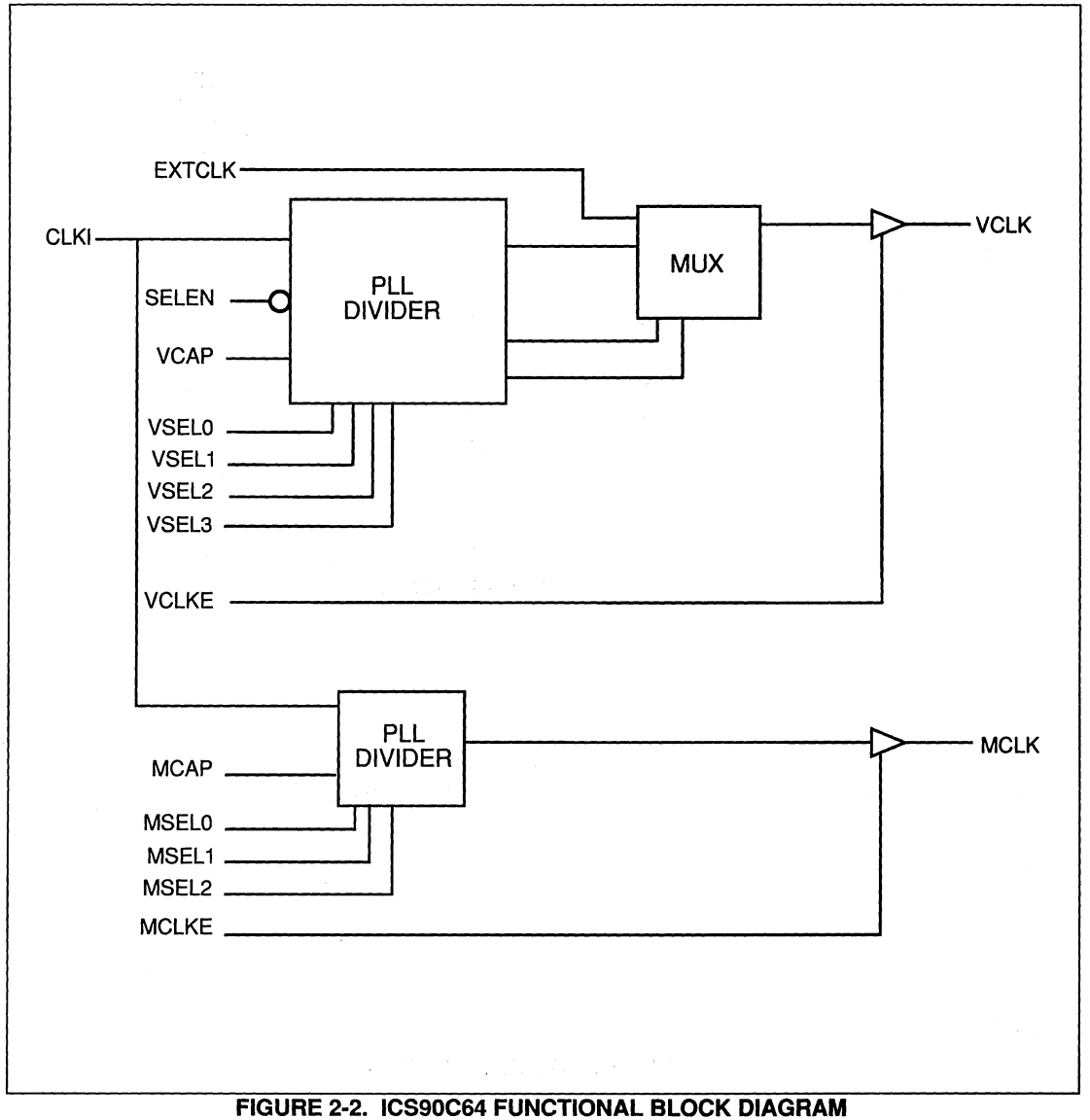


FIGURE 2-2. ICS90C64 FUNCTIONAL BLOCK DIAGRAM

3.0 PIN DESCRIPTIONS

The following table provides the pin definitions for the 20-pin ICS90C64 package.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	CLK1	IN	Reference input clock from system
2	MSEL2	IN	Select input for MCLK selection
3	EXTCLK	IN	External clock input for an additional frequency
4	VSEL1	IN	Control input for VCLK selection
5	VSEL0	IN	Control input for VCLK selection
6	SELEN	IN	Strobe for latching VSEL (0,1)(*Low enable*)
7	VSEL2	IN	Control input for VCLK selection
8	VSEL3	IN	Control input for VCLK selection
9	MSEL0	IN	Select input for MCLK selection
10	DGND	--	Ground for Digital Circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock Output
13	N.C.	--	No connection
14	MCLKE	IN	Enable input for MCLK output (*high enables output*)
15	AVCC	--	Power supply for analog circuit
16	AGND	--	Ground for analog circuit
17	N.C.	--	No connection
18	VCLKE	IN	Enable input for VCLK output (*high enables output*)
19	VCLK	OUT	Video Clock Output
20	DVCC	--	Power supply for Digital Circuit

TABLE 3-1. PIN DESCRIPTIONS

Note:
CLKI, EXTCLK, VSEL0, VSEL1, VSEL2, VSEL3
SELEN, MSEL0, MSEL1, MSEL2, VCLKE, & MCLKE - input pins have internal pullup resistors.

4.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias	0°C to 70°C
Storage temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to VSS	0.5 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

4.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to VSS (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0°C to 70°C
Power Supply Voltage	4.75 to 5.25 Volts

4.2 D. C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{ss}	0.8	V	V_{CC} = 5V
V_{IH}	Input High Voltage	2.0	V_{CC}	V	V_{CC} = 5V
I_{IH}	Input Leakage Current	---	20	µA	V_{in} = V_{CC}
V_{OL}	Output Low Voltage	---	0.4	V	I_{OL} = 8.0mA
V_{OH}	Output High Voltage	2.4	---	V	I_{OH} = 4.0mA
I_{CC}	Supply Current	---	30	mA	V_{CC} = 5V
R_{UP}	Internal Pullup Resistors	25	---	Kohm	V_{CC} = 5V
C_{in}	Input Pin Capacitance	---	8	pF	Fc = 1MHz
C_{out}	Output Pin Capacitance	---	12	pF	Fc = 1MHz

TABLE 4-1. D.C. CHARACTERISTICS

11

5.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section.

1. REFCLK = 14.318 MHz
2. tc = 1/fc
3. All units are in nanoseconds (ns).
4. Maximum jitter within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC.
6. Output pin loading = 25 pF.
7. Duty cycle measured at 1.4V.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	SELEN TIMING			
t_{pwen}	Enable Pulse Width	20	---	
t_{suen}	Setup Time Data to Enable	20	---	
t_{hden}	Hold Time Data to Enable	10	---	
	Reference Input Clock			
t_r	Rise Time	---	10	Phase Jitter 1 ns max.
t_f	Fall Time	---	10	Duty Cycle 42.5% min. to 57.5% max.
	MCLK and VCLK TIMINGS			
t_r	Rise Time	---	3	Phase Jitter 3 ns max.
t_f	Fall Time	---	3	Duty Cycle 40% min. to 60% max.
---	Frequency Error		0.5	%
---	Maximum Frequency		80	MHz
---	Propagation Delay for Pass Through Frequency	---	20	ns
---	Output Enable to tristate (into and out of) time	---	15	ns

TABLE 5-1. AC TIMING CHARACTERISTICS

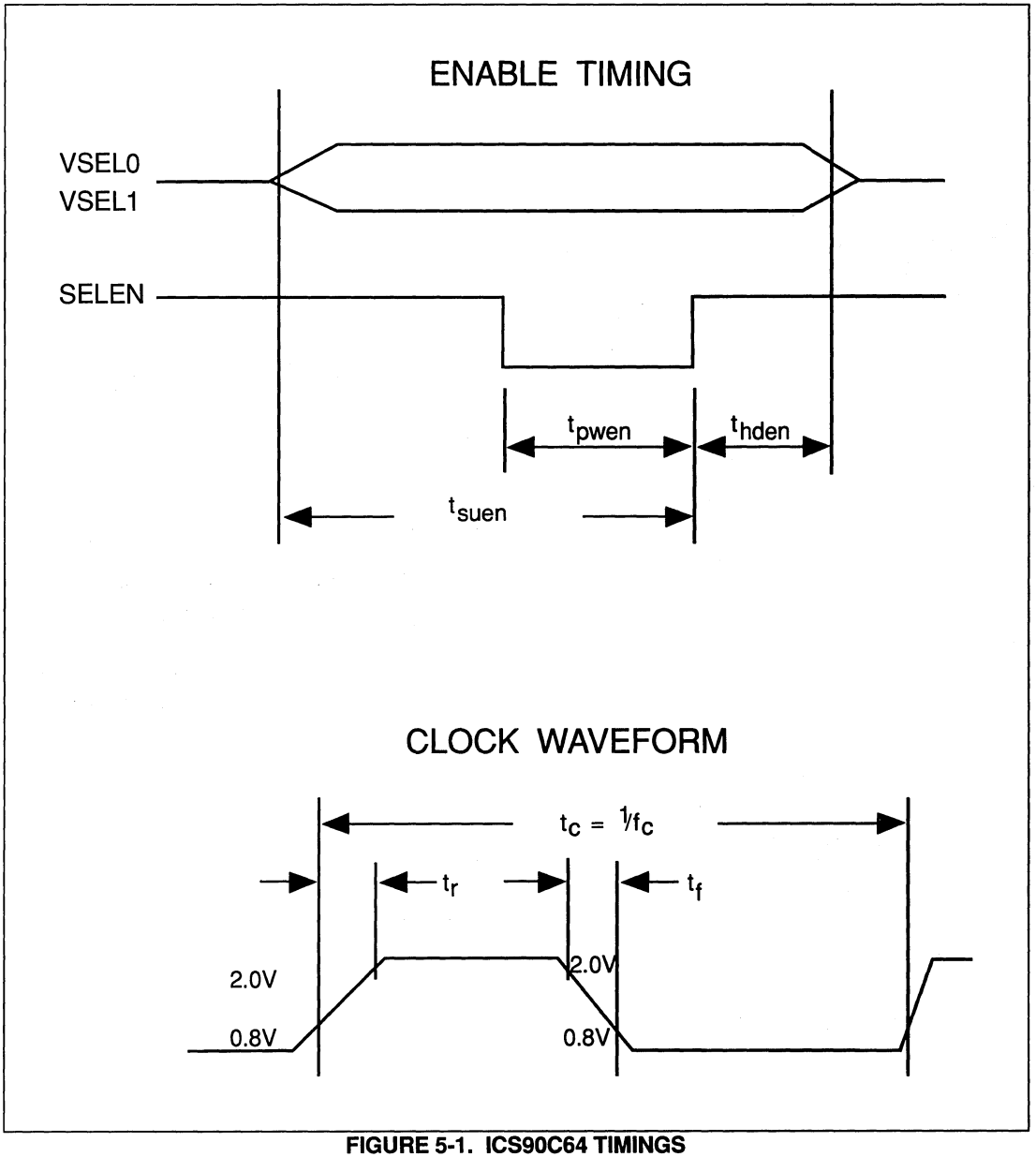


FIGURE 5-1. ICS90C64 TIMINGS

6.0 PACKAGING INFORMATION

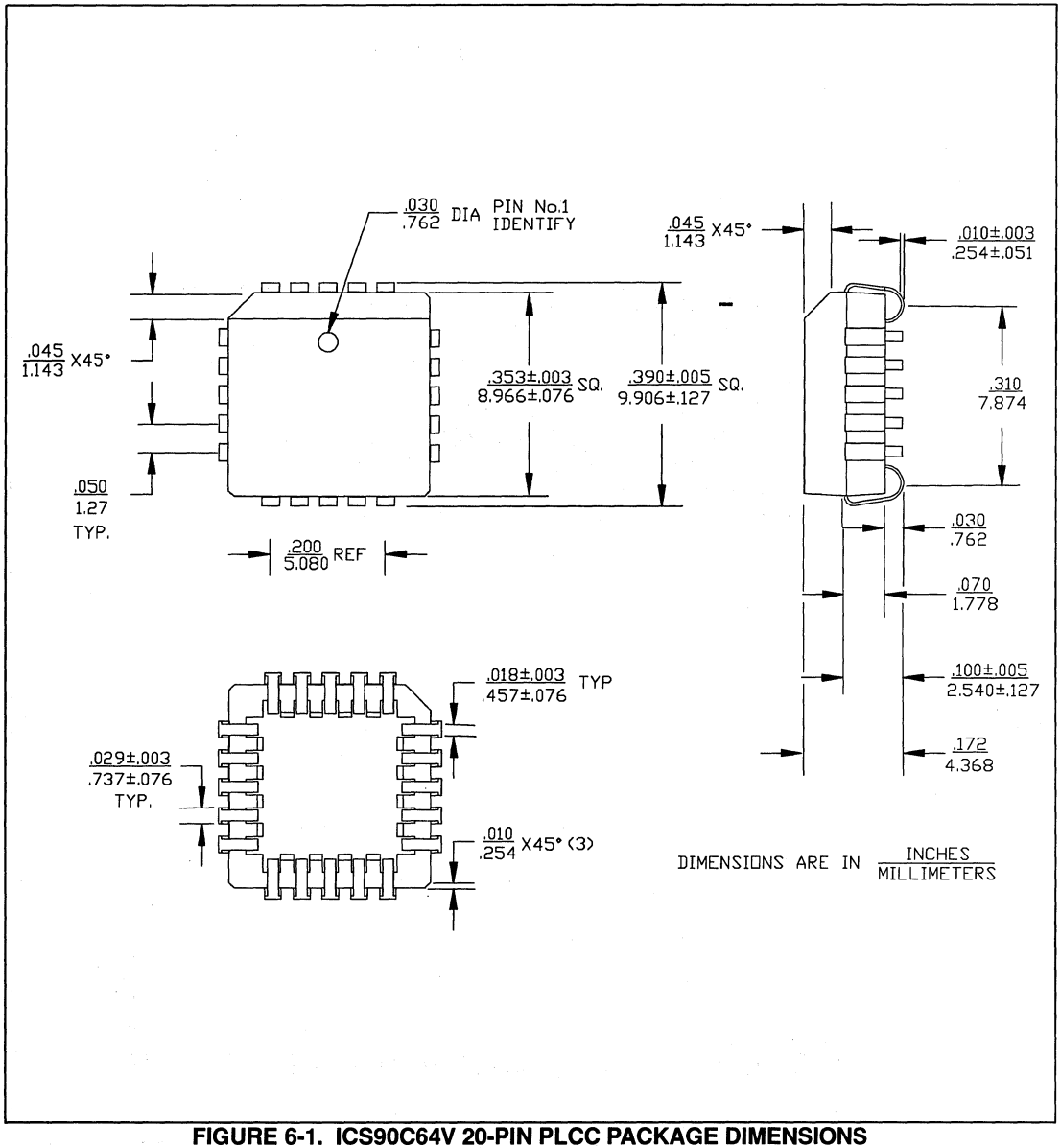


FIGURE 6-1. ICS90C64V 20-PIN PLCC PACKAGE DIMENSIONS

Contact Integrated Circuit Systems for other package diagrams at the following address:

Integrated Circuit Systems, Inc.
Valley Forge Corporate Center
2626 Van Buren Ave., P.O. Box 968
Valley Forge, PA 19482
Phone: (215) 666-1900
Fax: (215) 666-1099

FIGURE 6-2. OTHER ICS PACKAGE DIMENSIONS