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FE3021

Address Buffer and

Memory Controller

WESTERN DIGITAL

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1.0 DESCRIPTION

The FE3021 is a 16 MHz AT address buffer and memory controller in a 132-pin JEDEC package. Chip count is significantly reduced by integrating the memory controller, AT bus address buffers, and I/O into one chip. The memory controller is a high performance design, with programmable modes of operation. It controls page mode DRAM or static column DRAM. A maximum of 4 banks of DRAM can be controlled allowing a maximum of 8 MB of memory to be controlled by the FE3021. The DRAM bank locations are programmable on 128K byte boundries. One memory bank allows split addressing, so that one portion may be placed in conventional memory with the remainder in extended memory.

Additional features of the FE3600B chip set include EMS 4.0 support, on-chip address and control signal buffers for directly driving the AT bus, zero wait state access at 16 MHz using 100 ns DRAM with page mode access, generation of chip selects for floppy controller, 8042, 80287, and NMI, and mapping main and EGA BIOS into one physical PROM.

1.1 FEATURES

❏ Page mode DRAM access with interleaved memory banks

❏ Controls up to 4 banks (up to 8 MBytes) of memory

❏ On- chip RAS and CAS drivers for DRAM chips

❏ On- chip DRAM address multiplexer

❏ LIM standard EMS expanded memory hardware (supports EMS 4.0 multi-tasking)

❏ On- chip address and control signal buffers for directly driving AT bus

❏ Zero wait state access at 16 MHz using 100 ns DRAM with page mode access

❏ Generates chip selects for floppy controller, 8042, 80287, and NMI

❏ Generates programmable chip selects for four additional devices

❏ Maps system BIOS and EGA BIOS into one physical PROM

❏ "Hot" reset generation for quick 80286 switch from protected to real mode

❏ Fast Alternate Gate A20 generation

❏ 132 pin JEDEC plastic flat package
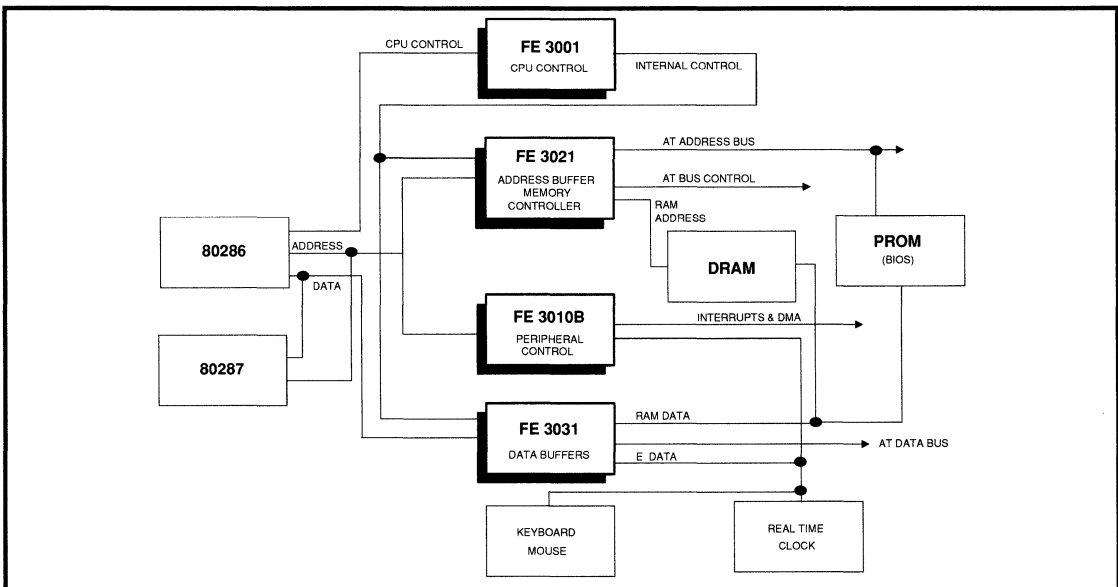
Figure 1. FE3600B Chip Set Functional Block Diagram

Figure 2. FE3021 Functional Block Diagram

MASTER

PROCESSOR
ADDRESS
A23-A0

A20GT

ADR0

BHE

ALE

ADSTB

LATCH

LATCH

LATCH

AT BUS
SA19 - SA0

AT BUS

AT BUS
LA23 - LA17

YIOR

YIOW

AT BUS
IOR
IOW

PROGRAMMABLE
AND FIXED
CHIP SELECTS

WAIT STATE CTRL

CS8042, CSNMI, CS0, CS1,
CS2, CS3, CSF, CS287

FAST RESET

READY

PROCESSOR STATUS

S0, S1, M/ IO

REFR

BANK SELECTS

BANK 0 L
BANK 0 H
1
2
3

PAGE MODE:

DRAM CTRL

RAS0 - RAS3

CASL0 - CASL3

CASH0 - CASH3

DLE, , LOWMEG, ONBD

DRAM

64K, 256K, 1M

(ANY COMBINATION)

DELAY LINE

RAS

TAP1-
TAP2

EMS
MAPPER

2 X 36 X 11
EMS REGISTERS

MEM ADDRESS
DECODER

ROW HIT/MISS

BIOS ROM
MAPPER

MA9 - MA0

SELDAT

CSPROM

EDATA BUS
D3 - D0

AT BUS

1.2   INTRODUCTION

The FE3021 device is designed to reduce chip count, increase flexibility, and provide improved operating speed and functionality when used with the FE3001, FE3010B, and FE3031 devices to implement a low cost, high performance AT compatible computer.

Chip count is reduced by integrating the memory controller, AT bus address buffers, and I/O Management functions into one chip.

The memory controller is a high performance design, with programmable modes of operation. It controls page mode DRAM or static column DRAM.

Up to 4 banks of DRAM may be controlled. The DRAM bank locations are programmable on 128K byte boundaries. One memory bank allows split addressing, so that one portion may be placed in conventional memory, with the remainder in extended memory, with an additional mode to allow copying BIOS code from ROM to RAM for faster execution.

A major function of the FE3021 is to generate chip select decodes for peripheral chips on the system board; for instance, the floppy controller, hard disk controller, serial, and parallel port chips. The floppy and hard disk chip selects may be disabled or may be enabled for either the primary or secondary address decode, as defined 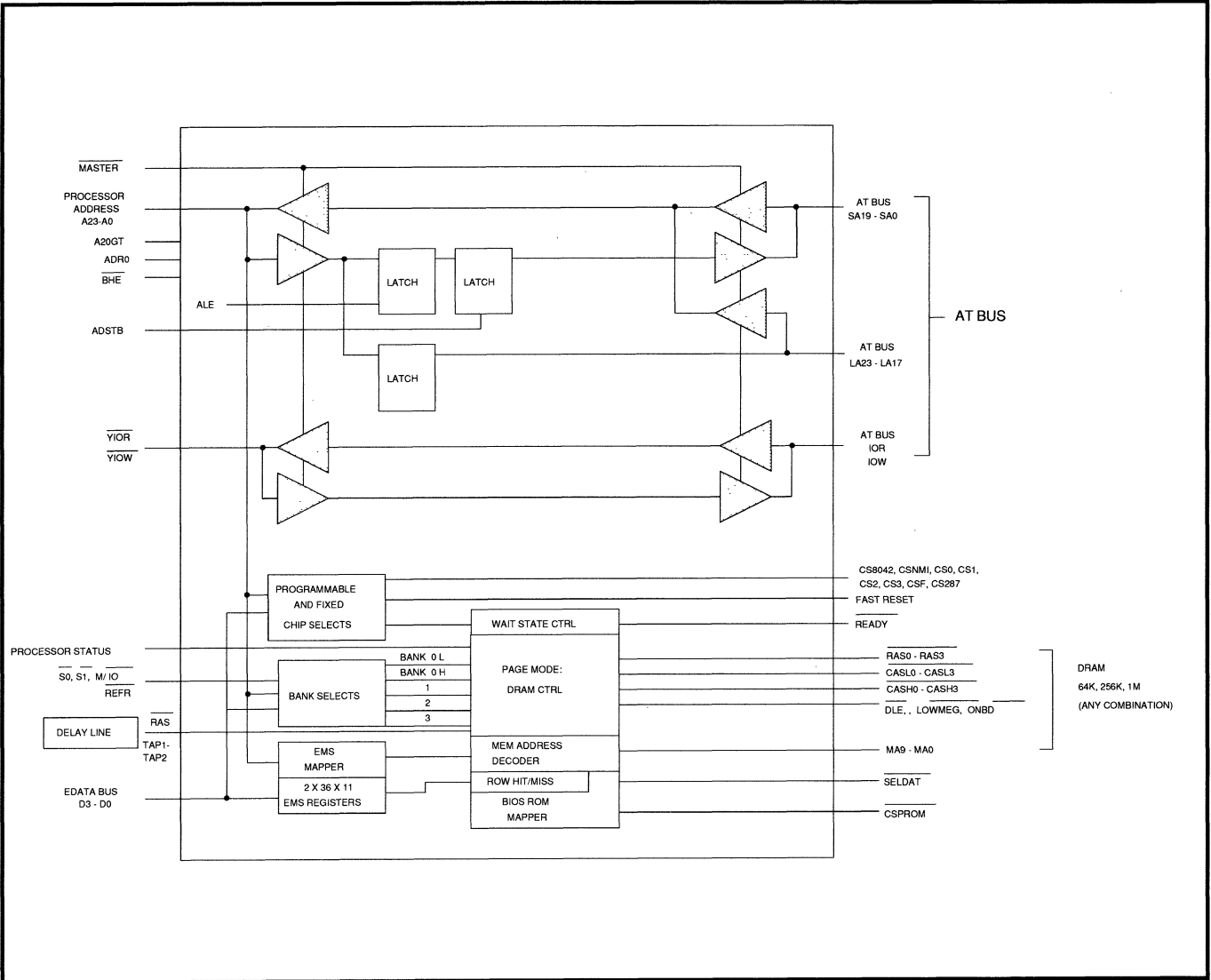by IBM. Four programmable chip selects are available, for supporting serial, parallel, mouse, or other types of ports. Refer to Figure 2 for Pin assignment information and locations.

To reduce chip count and improve performance, particularly when an EGA or VGA graphics controller is placed on the system board, separate blocks of ROM may be mapped into a single physical ROM. For instance, the EGA BIOS and standard BIOS may be placed into the same pair of ROM chips or into a single 8-bit wide ROM. Besides reducing chip count, EGA operating speed will be improved, since EGA BIOS will be accessed 16 bits at a time. To improve BIOS performance, ROM code may be copied into RAM, and the BIOS ROM mapped out and replaced by RAM.

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2.0 80286 INTERFACE

This interface port connects with the 80286 address lines and the 80286 bus status lines. By connecting directly to the 80286 and by duplicating a portion of the bus controller logic, early determination of memory or I/O accesses may be made, as well as whether the access will be 8 bits or 16 bits. Pins A23-A0 are normally inputs, receiving addresses from the 80286. When MASTER is asserted, these pins become outputs.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
74	A23	I/O	80286 Address Line
78	A22	I/O	" "
79	A21	I/O	" "
80	A20	I/O	" "
81	A19	I/O	" "
82	A18	I/O	" "
83	A17	I/O	" "
84	A16	I/O	" "
85	A15	I/O	" "
86	A14	I/O	" "
87	A13	I/O	" "
88	A12	I/O	" "
89	A11	I/O	" "
90	A10	I/O	" "
109	A9	I/O	" "
110	A8	I/O	" "
111	A7	I/O	" "
112	A6	I/O	" "
113	A5	I/O	" "
114	A4	I/O	" "
115	A3	I/O	" "
116	A2	I/O	" "
117	A1	I/O	" "
118	A0	I/O	" "
119	$\overline{S0}$	I	80286 Status Line
120	$\overline{S1}$	I	80286 Status Line
121	$\overline{M/IO}$	I	80286 Status Line
122	CPUCLK	I	80286 Clock
123	HLDA	I	80286 Hold Acknowledge Line
21	$\overline{BHE}$	I	80286 Byte High Enable

Table 1. 80286 Interface Pin Functions

3.0   DATA BUS INTERFACE

The data bus port is 4 bits wide, which should connect to the EDATA local data bus, and is used to access the internal FE3021 control registers. The upper 4 bits should be ignored when reading the control registers. Refer to Table 2 for pin assignments.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
17	EDATA3	I/O	Control Register Data Line
16	EDATA2	I/O	" "
15	EDATA1	I/O	" "
14	EDATA0	I/O	Control Register Data Line

Table 2. Data Bus Interface Pin Assignments

4.0 I/O CHIP SELECTS

This logic section generates chip selects for standard system board functions such as the 8042 keyboard controller, 80287 math coprocessor, floppy controller, and hard disk controller. It also generates chip selects for up to 4 additional I/O ports which may have programmable addresses and wait state characteristics. Refer to Table 3 for pin assignments.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
48	CS0	O	Programmable Chip Select 0
47	CS1	O	Programmable Chip Select 1
46	CS2	O	Programmable Chip Select 2
45	CS3	O	Programmable Chip Select 3 Or H. D. Control Chipselect
49	CSF	O	Floppy Disk Controller Chip Select Or Operation Or Configuration Register Select
60	CS8042	O	8042 Keyboard Control Select
56	CS287	O	80287 Coprocessor Select
20	CSNMI	O	NMI Logic Chip Select
22	CSPTB	O	Memory Parityand I/o Check Control Chip Select

Table 3. I/O Chip Selects Pin Assignments

5.0 I/O CONTROL

This logic section contains control logic for the I/O bus.

The IORDY signal will go low when generating wait states. For 12 MHz systems, this signal may be tied directly to the bus signal IOCHRDY. For 16 MHz or 20 MHz systems, this signal should be sent to the FE3001 directly. The IOCHRDY bus signal should be buffered through an open collector driver and wire-OR'ed with the IORDY signal. The IORDY pin will normally be at a high impedance state. When generating wait states, it will go low. When going from a low to a high state, the IORDY pin will be actively driven high for one processor clock time, then the output will tri-state. An external pullup resistor should be used to keep the IORDY signal high when the IORDY pin is at a high impedance state. The state of IORDY is sampled at the rising edge of RESET ; if IORDY is low at this time, the FE3021 will fetch data and instructions from the BIOS ROM 8 bits at a time over the EDATA bus, otherwise a 16 bit wide ROM on the MDATA bus is assumed.

Table 4 lists the data word size, I/O addresses, and chip selects generated for each variable port type.

The PORT 0, PORT 1, PORT 2, and PORT 3 addresses are fully programmable, with the choice of either using nine I/O addresses for decode, or masking the A8 address bit (for instance, for decoding dual serial ports). The LSB (A0) address is always ignored. The lower 2, 3, or 4 bits of the address may also be ignored so that 2, 4, 8, or 16 bytes may be allocated for the port.

All FE3021 control registers, except those used for EMS page mapping, are accessed by first writing eight times to address FFF00 (in an area allocated for ROM BIOS). Any memory access outside of the ROM BIOS address space, either data access or instruction fetch, will abort the unlocking process. Once unlocked, memory accesses outside of the ROM BIOS area may be made without affecting the unlocked state. When unlocked, the address space from FFF01 to FFFFE becomes register controls for the FE3021 device. The controls are locked again by reading location FFFFF. This access method guarantees that all control register changes will be made through the BIOS.

PIN NUMBER	PIN NAME	I/O	FUNCTION
127	IORDY	I/O	Ready Line, modified Open Drain, Input At Reset Time For 8-Bit ROM Sizing
40	SELDAT	O	Direction Of Data Tranceiver Data To EDATA Bus
8	IOR	I/O	System I/O Read Command Signal, Drives Expansion Bus. An Input In Master Mode.
9	IOW	I/O	System I/o Write Command Signal, Drives Expansion Bus. An Input In Master Mode.
10	YMEMR	I	Ungated System Memory Read Command Signal From FE3001
11	YMEMW	I	Ungated System Memory Write Command Signal From FE3001

Table 4. I/O Control Pin Functions

PIN NUMBER	MNEMONIC	I/O	FUNCTION
53	ADSTB	I	Address Strobe From FE3001 And FE3010B.
12	$\overline{\text{YIOR}}$	I/O	Ungated I/O Read Strobe From FE3001, An Output In Master Mode.
13	$\overline{\text{YIOW}}$	I/O	Ungated I/O Write Strobe From FE3001, output In Master Mode.
19	$\overline{\text{FRES}}$	I/O	"HOT" Reset Output
25	$\overline{\text{LOMEG}}$	O	To FE3031 Memory Strobe Gating
28	$\overline{\text{RESET}}$	I	Master Reset For FE3021
52	$\overline{\text{MASTER}}$	I	Bus Master Signal From AT Bus
54	A20GT	I	From 8042. When High, A20 Is Ungated
57	$\overline{\text{ONBD}}$	O	To FE3001. Indicates High Speed On-Board Access
59	ADDR19	O	AT Bus SA19
61	ADDR 18	O	AT Bus SA18
62	ADDR 17	O	AT Bus SA17
64	ADDR 16	I/O	AT Bus SA16
65	ADDR 15	I/O	AT Bus SA15
66	ADDR 14	I/O	AT Bus SA14
68	ADDR 13	I/O	AT Bus SA13
69	ADDR 12	I/O	AT Bus SA12
72	ADDR 11	I/O	AT Bus SA11
73	ADDR 10	I/O	AT Bus SA10
75	ADDR 9	I/O	AT Bus SA 9
94	ADDR8	I/O	AT Bus SA8
96	ADDR7	I/O	AT Bus SA7
97	ADDR6	I/O	AT Bus SA6
98	ADDR5	I/O	AT Bus SA5
100	ADDR4	I/O	AT Bus SA4
101	ADDR3	I/O	AT Bus SA3
104	ADDR2	I/O	AT Bus SA2
106	ADDR1	I/O	AT Bus SA1
105	ADDR0	I/O	AT Bus SA0
63	LA23	I/O	AT Bus LA23
70	LA22	I/O	AT Bus LA22
71	LA21	I/O	AT Bus LA21
93	LA20	I/O	AT Bus LA20
95	LA19	I/O	AT Bus LA19
102	LA18	I/O	AT Bus LA18
103	LA17	I/O	AT Bus LA17

Table 4. I/O Control Pin Functions (Continued)

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A Version Number register provides information on the version of the FE3021 chip. It also contains a bit which toggles between '0' and '1' when the register is read, which provides indication that the register set has been unlocked.

VERSION NUMBER

| FFF01	X	X	X	X	VER			T
	7	6	5	4	3	2	1	0
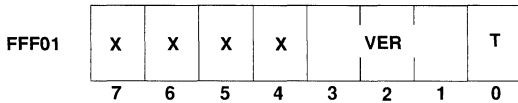
T : toggles between 0 and 1 with every read access of the Version Number register.

VER : 000 when T=0
101 when T=1 for Early Production Version
100 when T=1 for Production Version

System board devices may be located on the EDATA bus rather than on the I/O expansion slot DATA bus. The $\overline{\text{SELDAT}}$ signal which controls the DATA to EDATA bus direction is affected by the two port location registers. This option is available for peripheral devices which cannot directly drive the high current I/O slot DATA bus. Note, however, that DMA transfers cannot be made to devices on the EDATA bus.

 The $\overline{\text{SELDAT}}$ signal is active (low) when $\overline{\text{IOR}}$ is active and address bits A8 and A9 are low, or the PORTS LOCATION register indicates that an addressed port is on the EDATA bus. The $\overline{\text{SELDAT}}$ signal is also low when $\overline{\text{MEMR}}$ is active and the **8-bit** BIOS is being accessed.

PORTS LOCATION REGISTER

FFF06	X	X	X	X	A	B	C	D
	7	6	5	4	3	2	1	0
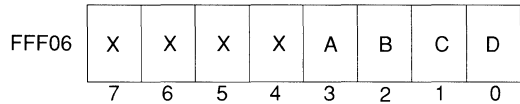
A = 0	Port 0 On DATA Bus
A = 1	Port 0 On EDATA Bus
B = 0	Port 1 On DATA Bus
B = 1	Port 1 On EDATA Bus
C = 0	Port 2 On DATA Bus
C = 1	Port 2 On EDATA Bus
D = 0	Port 3 On DATA Bus
D = 1	Port 3 On EDATA Bus

THE PORTS LOCATION REGISTER IS CLEARED BY A MASTER RESET.

HOT RESET REGISTER

FFF07	X	X	X	X	0/1	DA	A	H
	7	6	5	4	3	2	1	0
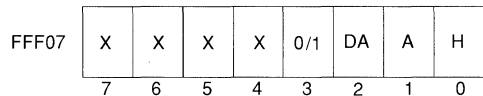
THE HOT RESET REGISTER IS CLEARED BY A MASTER RESET.

Register FFF07 is used to generate a hot reset to the processor or to generate an alternate A20 gate. The state of the A bit is OR'ed with the A20GT pin. If either the A bit is set or the A20GT pin is high, the A20 line is undisturbed. If both are low, then the A20 line is gated low. If the DA bit is set, then a CPU reset generated by the keyboard controller will reset the A bit; the A bit will not be reset by a hot reset generated by the FE3021. A hot reset is generated by changing the H bit from a '0' to a '1'. 131 clocks after the trailing edge of the $\overline{\text{MEMW}}$ strobe, the $\overline{\text{FRES}}$ pin will be pulled low. The reset pulse lasts for 32 clocks, then the $\overline{\text{FRES}}$ pin is actively pulled high for one clock cycle, then is tri-stated. If the $\overline{\text{FRES}}$ pin is pulled low externally (e.g. if wire-OR'ed with the 8042 CPU reset line), then the internal FE3021 registers will relock. If the $\overline{\text{FRES}}$ pin is not used, then it should be pulled up externally or the FE3021 registers will not unlock.

Bit 3 is a writeable bit which is not currently used.

ENABLE PORTS REGISTER

FFF10	X	X	X	X	EN3	EN2	EN1	EN0
	7	6	5	4	3	2	1	0
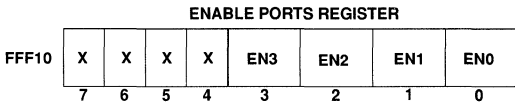
THE ENABLE PORTS REGISTER IS CLEARED BY A MASTER RESET.

The programmable PORT 0, PORT 1, PORT 2, and PORT 3 chip selects are enabled with the Enable Ports register. If the Enable bit is 0, the port chip select bit will always be at an inactive (high) state. All four ports are disabled after master reset. EN3 enables $\overline{CS3}$ only when $\overline{CS3}$ is a programmed chip select. When $\overline{CS3}$ is a HDC chip select, $\overline{CS3}$ is enabled by register FFF49, bit 1.

For ports 0, 1, and 2, the access will have the default wait states: 1 wait state for 16 bit accesses and 4 wait states for 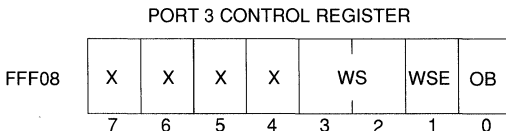8 bit accesses, with the wait states set from the FE3001. The selected chip must generate $\overline{IOCS16}$ if it is a 16 bit peripheral.

PORT 3 CONTROL REGISTER

FFF08	X	X	X	X	WS	WSE	OB
	7	6	5	4	3 2	1	0

THE PORT 3 CONTROL REGISTER IS CLEARED BY A MASTER RESET.

WS	HDC DATA PORT HIGH SPEED WAIT STATES
00	1
01	2
10	3
11	4

OB	$\overline{CS3}$ WAIT STATES
0	Default (slow)
1	High Speed Hard Disk Controller

WSE:	HIGH SPEED HDC WAIT STATE ENABLE
0:	High Speed HDC Wait States Set By FE3001
1:	High Speed HDC Wait States Set By WS Field

For port 3, the access will normally have the default wait states but may also be programmed to have high speed wait state timing when $\overline{CS3}$ is programmed as a hard disk chip select and the on-board 16-bit hard disk controller is capable of high speed access. When the high speed disk controller configuration is used, the WSE and OB fields should be set to '1', and the WS field will set the number of high speed wait states, timed from the CPUCLK, rather than from SYSCLK. The other disk controller ports will always be accessed at low speed.

When 0B is set to a 1, the FE3021 will generate the ONBD signal to the FE3001 during HDC accesses through port 3. The FE3001 will provide the same number of wait states it does for on-board memory. If it is desired, the number of wait states for the HDC can be extended using the WS and WSE fields.

When implementing a high speed disk controller port, it is necessary to provide a separate address path for the hard disk controller. The HDC receives ungated I/O read and write strobes at the full CPU speed. The following schematic illustrates the required connections.

4
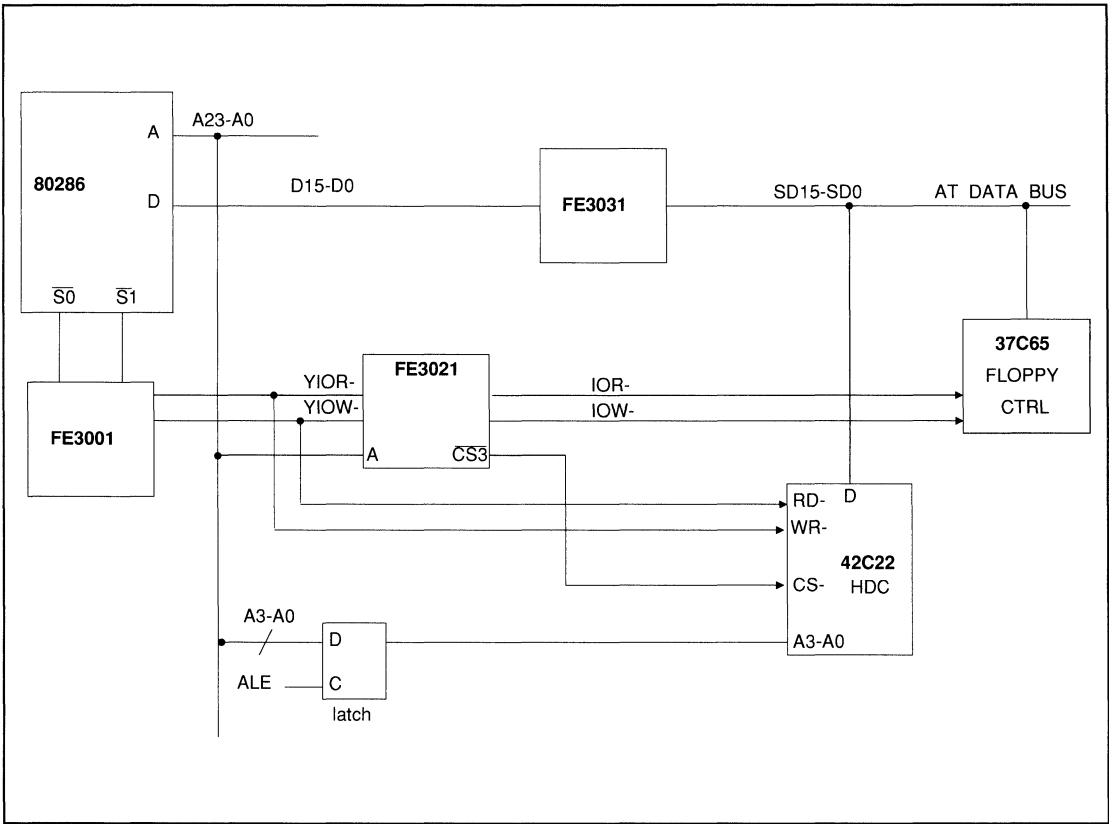
Figure 3. High Speed HDC Configuration

FFF09
FFF11
FFF19
FFF21

X	X	X	X	O	U	LMASK	
7	6	5	4	3	2	1	0

LMASK	ADDRESS BITS COMPARED
00	A9 A8 A7 A6 A5 A4 A3 A2 A1 X
01	A9 A8 A7 A6 A5 A4 A3 A2 X X
10	A9 A8 A7 A6 A5 A4 A3 X X X
11	A9 A8 A7 A6 A5 A4 X X X X

U = 0 : INCLUDE A8 IN ADDRESS COMPARISON

LMASK	ADDRESS BITS COMPARED
00	A9 X A7 A6 A5 A4 A3 A2 A1 X
01	A9 X A7 A6 A5 A4 A3 A2 X X
10	A9 X A7 A6 A5 A4 A3 X X X
11	A9 X A7 A6 A5 A4 X X X X

U = 1 : IGNORE A8 IN ADDRESS COMPARISON

THE PORT ADDRESS MASK REGISTER IS CLEARED BY A MASTER RESET.

PORT	PORT CONTROL REGISTER ADDRESS
0	FFF09
1	FFF11
2	FFF19
3	FFF21

NOTE: Bit 3 is not writeable and is always '0'.

PORT ADDR - LOWER MSB

FFF0A
FFF12
FFF1A
FFF22

X	X	X	X	X	X	A9	A8
7	6	5	4	3	2	1	0

PORT ADDR - UPPER LSB

FFF0B
FFF13
FFF1B
FFF23

X	X	X	X	A7	A6	A5	A4
7	6	5	4	3	2	1	0

PORT ADDR - LOWER LSB

FFF0C
FFF14
FFF1C
FFF24

X	X	X	X	A3	A2	A1	0
7	6	5	4	3	2	1	0

PORT	PORT I/O ADDRESS REGISTERS		
	A9-A8	A7-A4	A3-A0
0	FFF0A	FFF0B	FFF0C
1	FFF12	FFF13	FFF14
2	FFF1A	FFF1B	FFF1C
3	FFF22	FFF23	FFF24

The PORT I/O ADDRESS registers for all four ports are set to all zeros by a master reset.

The following tables list the I/O addresses and chip selects generated for each fixed port type. The chip selects are not gated with IOR or IOW. The CSNMI signal is decoded for both even and odd addresses, so that access may be made to the FE3001 control register at address 073.

The floppy controller operations register select, configuration register select, and floppy disk controller chip select may be generated from the CSF pin and the ADDR2 and ADDR1 lines.

	ADDR2	ADDR1	CSF
OPERATIONS REGISTER ACCESS	0	X	1
CONFIG REGISTER ACCESS	1	1	1
FLOPPY CHIP SELECT ACTIVE	X	0	1

PORT	BIT SIZE	I/O ADDRESS	ACTIVE PIN	FUNCTION
FLOPPY	8	3F2 372	CSF	FDC Operation Select. 3F2 Is Primary Address, 372 Is Secondary
	8	3F4-3F5 374-375	CSF	3F4-3F5 Are Primary Addresses, 374-375 Are Secondary.
	8	3F6 376	$\overline{CS3}$*	Hard Disk Controller Chip Select. 3F6 Is Primary Address, 376 Is Secondary.
	8	3F7 377	CSF $\overline{CS3}$*	$\overline{CS3}$ And CSF Pins Will Be Asserted. 3F7 Is Primary Address, 377 Is Secondary.
80287	8	0E0-0FF	$\overline{CS287}$	80287 Chip Select.
8042	8	060-06E (EVEN)	$\overline{CS8042}$	8042 Chip Select.
NMI LOGIC	8	070-07F	$\overline{CSNMI}$	Real Time Clock And NMI Logic Select
PARITY CHECK	8	061-06F (ODD)	$\overline{CSPTB}$	Parity Check Select And Port B Decode . External Logic Must Separate The Signals.
HARD DISK	16	1F0 170	$\overline{CS3}$ *	HDC Chip Select - Data Port Access. 1F0 Is Primary Address, 170 Is Secondary
	8	1F1-1F7 171-177	$\overline{CS3}$	HDC Chip Select - TASK FILE. 1F1-1F7 Are Primary Addresses, 171-177 Are Secondary.

Table 5. I/O Addresses/Chip Selects for Fixed Ports

* WHEN $\overline{CS3}$ PIN IS PROGRAMMED AS HDC CHIP SELECT .

PRIMARY / SECONDARY PORT FUNCTION SELECT

FFF49

X	X	X	X	DH	PS	H	F
7	6	5	4	3	2	1	0

DH=0: $\overline{CS3}$ pin will respond to address programmed by FFF22-FFF24
DH=1: $\overline{CS3}$ pin will respond to hard disk addresses
PS=0: Primary hard disk and floppy disk address
PS=1: Secondary hard disk and floppy disk address
H=0:   On-board hard disk controller enabled
H=1:   Disable on-board hard disk controller
F=0:   On-board floppy disk controller enabled
F=1:   Disable on-board floppy disk controller

DH, PS, H, AND F ARE CLEARED TO '0' BY MASTER RESET

NOTE: For early production version (ID Register = 0000, 1011) bits 2 - 0 had different definitions:

Bit 2 = 0: Enable CSF Output
Bit 1 = 0: Primary Hard Disk Address
Bit 0 = 0: Primary Floppy Disk Address

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6.0   MEMORY CONTROL

Four RAS pins are available for controlling up to four 16 bit wide banks of system board RAM. Eight CAS pins control the low and high bytes of each bank. During a refresh cycle, all RAS signals will be active (ignoring the RAM configuration register FFF57) and CAS signals will stay inactive.

The RAS and CAS lines drive the DRAM array directly.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
128	RAS0	O	RAS Signal For DRAM Memory Bank 0
129	RAS1	O	RAS Signal For DRAM Memory Bank 1
130	RAS2	O	RAS Signal For DRAM Memory Bank 2
132	RAS3	O	RAS Signal For DRAM Memory Bank 3
125	CASL0	O	CAS Signal For DRAM Memory Bank 0, Low Byte
126	CASL1	O	CAS Signal For DRAM Memory Bank 1, Low Byte
2	CASL2	O	CAS Signal For DRAM Memory Bank 2, Low Byte
3	CASL3	O	CAS Signal For DRAM Memory Bank 3, Low Byte
4	CASH0	O	CAS Signal For DRAM Memory Bank 0, High Byte
5	CASH1	O	CAS Signal For DRAM Memory Bank 1, High Byte
6	CASH2	O	CAS Signal For DRAM Memory Bank 2, High Byte
131	CASH3	O	CAS Signal For DRAM Memory Bank 3, High Byte
18	REFR	I	Memory Refresh Signal
43	CSPROM	O	BIOS PROM Select
26	TAP2	I	Second Tap Output Of RAS Delay Line
44	TAP1	I	First Tap Output Of RAS Delay Line
58	RAS	O	To RAS Delay Line Input
23	DBLE	O	To FE3031 Memory Data Bus Latch Enable
24	ADR0	I	From FE3001 Byte Conversion

Table 6. Memory Control Pin Information

7.0 MEMORY ADDRESS MULTIPLEXER

The memory address multiplexer generates the row and column addresses for the DRAM. The memory address multiplexer outputs should be buffered by external drivers when driving the memory array.

The memory address multiplexer supports three sizes of DRAM: 64K, 256K, and 1 MB. The three sizes of DRAM's may be intermixed in any order.

The memory address multiplexer is designed so that SIMM mounted DRAM's of the three different sizes may be inserted into SIMM sockets without the need to change board jumpers.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
31	RA0	O	Memory Address Multiplexer Output Bit 0 (LSB)
32	RA1	O	Memory Address Multiplexer Output Bit 1
33	RA2	O	Memory Address Multiplexer Output Bit 2
34	RA3	O	Memory Address Multiplexer Output Bit 3
35	RA4	O	Memory Address Multiplexer Output Bit 4
36	RA5	O	Memory Address Multiplexer Output Bit 5
37	RA6	O	Memory Address Multiplexer Output Bit 6
38	RA7	O	Memory Address Multiplexer Output Bit 7
39	RA8	O	Memory Address Multiplexer Output Bit 8
41	RA9	O	Memory Address Multiplexer Output Bit 9 (MSB)

Table 7. Memory Address Multiplexer Outputs

64K DRAM ADDRESS MULTIPLEXER CONFIGURATION											
Memory Mode		MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Independent	RAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
Non Page Mode	CAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A9
Independent	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A9
Page Mode	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
2 Way Intlv	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A17
Page Mode	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
4 Way Intlv	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A18	A17
Page Mode	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
256K DRAM ADDRESS MULTIPLEXER CONFIGURATION											
Independent	RAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
Non Page Mode	CAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A10	A17
Independent	RAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A10	A17
Page Mode	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
2 Way Intlv	RAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A19	A17
Page Mode	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 Way Intlv	RAS	(A20)	A18	A16	A15	A14	A13	A12	A20	A19	A17
Page Mode	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1

Table 8. Address Multiplexer Configurations

1 MBIT DRAM ADDRESS MULTIPLEXER CONFIGURATION										
Independent	RAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
Non Page Mode	CAS	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
Independent	RAS	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
Page Mode	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
2 Way Intlv	RAS	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
Page Mode	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 Way Intlv	RAS	A20	A18	A16	A15	A14	A13	A22	A21	A19	A17
Page Mode	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
REFRESH ADDRESS - ALL DRAM SIZES										
		A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Table 8. Address Multiplexer Configurations (Continued)

NOTE: Addresses in parentheses not used by DRAM.

SYSTEM BOARD ROM WAIT STATE
CONTROL REGISTER

FFF50	X	X	X	X	RWS	0	RWSE
	7	6	5	4	3 2	1	0

RWS	HIGH SPEED WAIT STATE
00 *	1
01	2
10	3
11	4

RWSE=1: Enables RWS, otherwise on-board ROM and RAM Wait States will be set by FE3001.

THIS REGISTER IS CLEARED TO ZERO BY MASTER RESET.

The FE3021 can extend the number of processor wait states for an on-board BIOS access by setting the RWSE bit to a '1'. The number of wait states will then be determined by the value of the RWS field. If the RWSE bit is set to a '0', the number of wait states for an on-board BIOS access is controlled by the FE3001.

The ability to add wait states for BIOS accesses is important for a 16-bit BIOS because the on-board memory read wait states programmed into the FE3001 apply to both on-board BIOS and on-board DRAM. That value will be programmed to optimize DRAM access time (typically zero wait states for page mode operations). This very fast access time will likely be too quick for BIOS ROMs and can therefore be extended for BIOS accesses by setting the RWSE bit.

Bit 1 is used for diagnostic purposes and should remain '0'.

The system BIOS address space may be from F0000 to FFFFF or E0000 to FFFFF. If the EGA BIOS is to be mapped, then the BIOS ROM chip select is also active when the region from C0000 to C3FFF or C0000 to C7FFF is addressed. The address output onto the expansion bus will be automatically translated. The BIOS PROM size and number of wait states will then apply to both the system BIOS region F0000-FFFFF and C0000-C3FFF.

The BIOS EPROM size may either be 8 bits or 16 bits. The EPROM size is determined at reset time, and is signaled by the IORDY line. If the IORDY line is high at the trailing edge of master reset, then the EPROM size is set to 16 bits. If the IORDY line is low at the trailing edge of master reset, then the EPROM size is set to 8 bits. No external logic is required for the 16 bit EPROM size. To select the 8 bit EPROM size, the IORDY line should be pulled low by a master reset. The MDATA bus is used for 16 bit EPROM's while the EDATA bus is used for 8 bit EPROM's.

The $\overline{\text{CSPROM}}$ signal is only active when $\overline{\text{MEMR}}$ is active.

MEMORY ADDRESS RANGE FOR ACTIVE CSPROM	FUNCTION
0F0000-0FFFFF FF0000-FFFFFF	BIOS SIZE = 64K (DEFAULT)
0E0000-0FFFFF FE0000-FFFFFF	BIOS SIZE = 128K
0C0000-0C3FFF	16K EGA BIOS Mapping Enabled Addresses Translated To 0F8000-0FBFFF Or 0F0000 - 0F3FFF
0C0000-0C7FFF	32K EGA BIOS Mapping Enabled Addresses Translated To 0F8000-0FFFFF Or 0F0000 - 0F7FFF * A16 is ignored in early production version (0000, 1011)

EPROM / RAM MAP CONTROL REGISTER

FFF51	X	X	X	X	EGA	MS	PS
	7	6	5	4	3 2	1	0

FFF52	X	X	X	X	XLA	'0'	MLA	FAD
	7	6	5	4	3	2	1	0
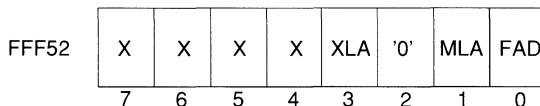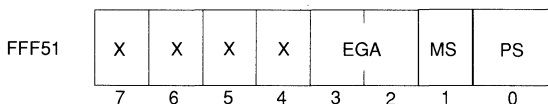
EGA=00 MS=X: No EGA mapping.
EGA=01 MS=0: 16K EGA map. C0000 - C3FFF
                  mapped to F8000 - FBFFF
        MS=1: 16K EGA map. C0000 - C3FFF
                  mapped to F0000 - F3FFF
EGA=10 MS=0: 32K VGA map. C0000 - C7FFF
                  mapped to F8000 - FFFFF
        MS=1: 32K VGA map. C0000 - C7FFF
                  mapped to F0000 - F7FFF
PS = 0: PROM chip select will be active
             when address is 0F0000-0FFFFF
             or FF0000-FFFFFF, for 64K
             of BIOS.
             Default case after master reset.
      1: PROM chip select will be active
             when address is 0E0000-0FFFFF
             or FE0000-FFFFFF, for
             128K of BIOS.

THIS REGISTER IS CLEARED TO ZERO BY A MASTER RESET.

ALL BITS ARE CLEARED BY MASTER RESET

XLA=0: LA23 - LA17 low speed timing
XLA=1: LA23 - LA17 high speed timing

MLA=0: LA23 - LA17 latches are transparent
           during refresh cycles
MLA=1: LA23 - LA17 gated to '0' during refresh
           cycles

FAD=0: 3 wait state EMS misses
FAD=1: 2 wait state EMS misses

Register FFF52 controls logic for various speed enhancement and diagnostic modes. The XLA bit controls the timing of the LA23 - LA17 signals. Use of this bit can affect compatibility of plug-in bus cards.

When XLA=0, LA23 - LA17 signals are generated by latching the processor addresses by active S̄0̄ or S̄1̄. The LA23 - LA17 latches become transparent when a M̄ĒM̄R̄, M̄ĒM̄W̄, Ī̄ŌR̄, or Ī̄ŌW̄ strobe occurs. This bit should be 0 when running at 8 MHz, when the FE3001 is using the low speed clock.

When XLA=1, LA23 - LA17 signals are latched by active $\overline{S0}$ or $\overline{S1}$, but do not become transparent again until two CPU clocks after $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, or $\overline{IOW}$. This delay provides proper 8 MHz bus emulation of the LA23 - LA17 signals when the processor is running at 16 MHz.

The MLA bit is provided for diagnostic purposes. Bit 2 of register FFF52 is reserved and must be '0'.

The FAD bit can be used to enhance EMS performance for lower speed systems. EMS misses are normally three wait states, which are necessary for 16/20 MHz operation. At 12 MHz and below, EMS misses only need to be two wait states. This bit can be used for the non-page or page mode 2 operation at 12 MHz or below. This bit should remain 0 for page mode 3 or 16/20 MHz operation.

A single contiguous block of memory may be write protected, so that when BIOS ROM is copied into RAM, the RAM copy will not be inadvertently altered. Write protection is accomplished by not asserting CAS when MEMW is active.

Master reset clears the upper address boundary registers and presets the lower address boundary registers, which disables write protection. Write protection is enabled on the address range where the RAM address is less than or equal to the upper address boundary as well as greater than or equal to the lower address boundary.

RAM WRITE PROTECT
UPPER ADDRESS BOUNDARY

FFF53	X	X	X	X	'1'	A18	A17	A16
	7	6	5	4	3	2	1	0

THIS REGISTER IS CLEARED BY MASTER RESET

RAM WRITE PROTECT
LOWER ADDRESS BOUNDARY

FFF55	X	X	X	X	'1'	A18	A17	A16
	7	6	5	4	3	2	1	0

THIS REGISTER IS PRESET TO ALL '1' BY MASTER RESET

Write protection is programmable on 64K boundaries, and the write protection boundaries must be equal to or above 80000H and equal to or below FFFFFH. Write protection will not affect EMS writing even if the EMS window address range is covered by write protection boundaries. This allows protection of BIOS code copied into RAM without affecting operation of EMS.

The memory banks may be programmed to various sizes on 128K boundaries, except the upper split of bank 0, which is programmable on 64K boundaries.

A pair of window registers determines the address range for each memory bank. This allows the banks to be positioned at varying points and in different order than the bank number. If one bank of memory is defective, it can be disabled and the other banks can be programmed to replace it.

NOTE: For the early production version of the FE3021 (version reg=0000, 1011), bank 0 has three pairs of window registers to allow split addressing. The bottom split could be used for conventional memory from 8000 to 9FFFF. The top split could be used for extended memory or could be used to copy main BIOS from ROM to RAM in the address range E0000 or F0000 to FFFFF. A middle split was available for copying user and video BIOS from ROM to RAM. This middle split had boundaries programmable between C0000 to DFFFF in 16K address increments. One limitation was that if the middle split were used, unused memory between the splits could not be translated and used for extended memory.

For the production version of the FE3021 (version reg=0000, 1001), the middle split of Bank 0 was removed. Video BIOS is shadowed instead by mapping the EGA/VGA BIOS to F0000 or F8000 and then shadowing the F0000 - FFFFF BIOS area. This method also allows a ROM resident setup program to reside at F0000 in ROM, which can be replaced with EGA/VGA BIOS by shadowing. This method allows a 512K bank to be allocated as 128K of conventional memory, 64K of shadowed VGA and system BIOS, and 320K of extended or EMS memory.

4

BANK 0 - LOWER SPLIT

UPPER ADDRESS BOUNDARY

FFF57	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

UPPER BOUNDARY MUST BE 0FXXXX OR BELOW

LOWER ADDRESS BOUNDARY

FFF59	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

LOWER BOUNDARY MUST BE 0FXXXX OR BELOW

UPPER ADDRESS BOUNDARY = 09XXXX (HEX) BY MASTER RESET

LOWER ADDRESS BOUNDARY = 08XXXX (HEX) BY MASTER RESET

BANK 0 - UPPER SPLIT

UPPER ADDRESS BOUNDARY - MSD

FFF5A	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

BANK 0 - UPPER SPLIT

UPPER ADDRESS BOUNDARY - LSD

FFF5B	X	X	X	X	A19	A18	A17	$\overline{A16}$**
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - MSD

FFF5C	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - LSD

FFF5D	X	X	X	X	A19	A18	A17	A16**
	7	6	5	4	3	2	1	0

UPPER ADDRESS BOUNDARY = 00XXXX (HEX) BY MASTER RESET

LOWER ADDRESS BOUNDARY = FFXXXX (HEX) BY MASTER RESET
(UPPER SPLIT DISABLED)

* Don't care
** A16 is ignored in early production version (0000, 1011)

BANK 0 - MIDDLE SPLIT

UPPER ADDRESS BOUNDARY - MSD

FFF5E	X	X	X	X	'1'	'1'	'0'	A16
	7	6	5	4	3	2	1	0

(ONLY IN EARLY PRODUCTION VERSION)

UPPER ADDRESS BOUNDARY - LSD
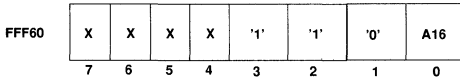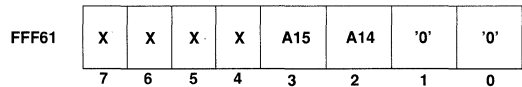
FFF5F	X	X	X	X	A15	A14	'0'	'0'
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - MSD

FFF60	X	X	X	X	'1'	'1'	'0'	A16
	7	6	5	4	3	2	1	0

UPPER ADDRESS BOUNDARY = 00XXXX (HEX) BY MASTER RESET

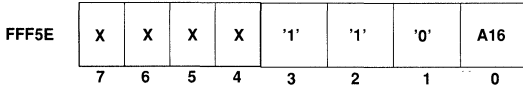LOWER ADDRESS BOUNDARY = FFXXXX (HEX) BY MASTER RESET
(MIDDLE SPLIT DISABLED)
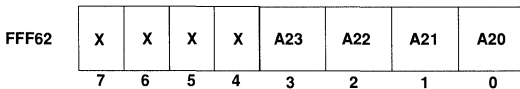
LOWER ADDRESS BOUNDARY - LSD

FFF61	X	X	X	X	A15	A14	'0'	'0'
	7	6	5	4	3	2	1	0

BANK 1

UPPER ADDRESS BOUNDARY - MSD

FFF62	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

BANK 1

UPPER ADDRESS BOUNDARY - LSD

FFF63	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0
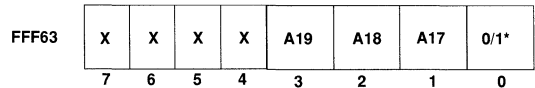
LOWER ADDRESS BOUNDARY - MSD
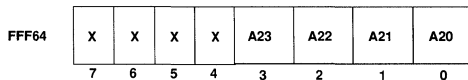
FFF64	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0
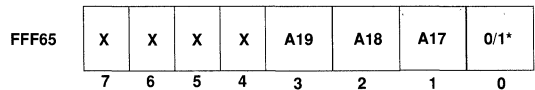
UPPER ADDRESS BOUNDARY = 07XXXX (HEX) BY MASTER RESET
LOWER ADDRESS BOUNDARY = 00XXXX (HEX) BY MASTER RESET

LOWER ADDRESS BOUNDARY - LSD

FFF65	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

* Don't care

4

BANK 2

UPPER ADDRESS BOUNDARY - MSD

FFF66	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

THESE REGISTERS ARE CLEARED BY MASTER RESET

BANK 2

UPPER ADDRESS BOUNDARY - LSD

FFF67	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - MSD

FFF68	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

THESE REGISTERS ARE PRESET TO ALL '1' BY MASTER RESET

(BANK 2 DISABLED BY MASTER RESET)

LOWER ADDRESS BOUNDARY - LSD

FFF69	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

BANK 3

UPPER ADDRESS BOUNDARY - MSD

FFF6A	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

THESE REGISTERS ARE CLEARED BY MASTER RESET

BANK 3

UPPER ADDRESS BOUNDARY - LSD

FFF6B	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - MSD

FFF6C	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

THESE REGISTERS ARE PRESET TO ALL '1' BY MASTER RESET

(BANK 3 DISABLED BY MASTER RESET)

LOWER ADDRESS BOUNDARY - LSD

FFF6D	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

* Don't care

The RAM banks may be either independent or two-way or four-way page interleaved. DRAM banks which are interleaved must be the same DRAM size.

This register is not used in non-page mode.

When the memory system operates in page mode, the banks of memory may operate independently or may be interleaved. Interleaving may decrease the average number of wait states, thus increasing performance, but interleaving may only be done if the memory banks to be interleaved are the same size.
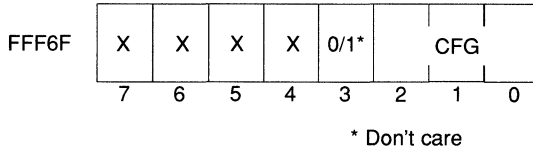
CFG	FUNCTION
000*	All banks are independent
011	Bank 2 paired with Bank 3, Banks 0 and 1 are independent
101	Bank 0 paired with Bank 1, Banks 2 and 3 are independent
111	Bank 0 paired with Bank 1, Bank 2 paired with Bank 3
110	All four banks are interleaved

* : Default after Master Reset

FFF6F	X	X	X	X	0/1*	CFG	
	7	6	5	4	3	2	1 0

* Don't care

2 WAY INTERLEAVE

3	
2	
3	
2	BANKS 2 + 3
3	
0	
1	
0	BANKS 0 + 1
1	
0	

2047
1024
1023
0

ADDRESS

4 WAY INTERLEAVE

3
2
1
0
3
0
3
2
1
0
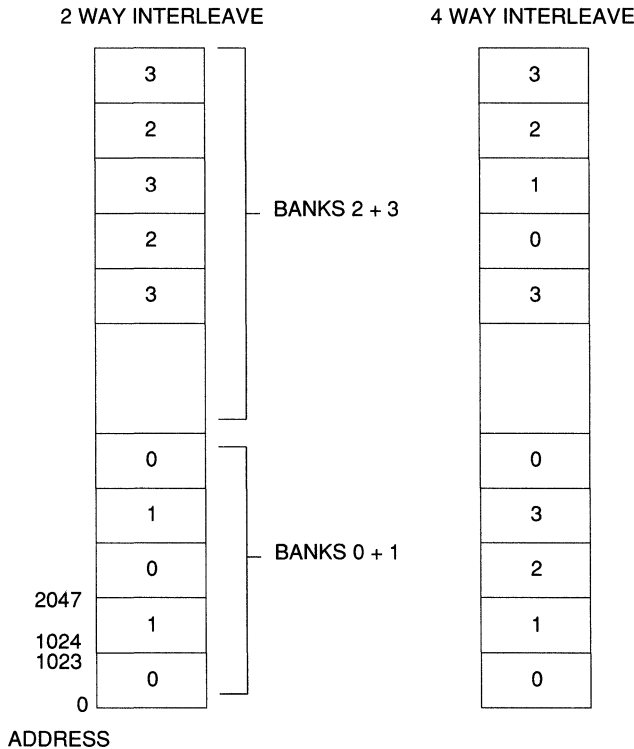
When the memory system operates in page mode, accesses to DRAM in the same page are made with zero wait states. An access to a different page, or the first access to a page after a refresh, DMA, or master cycle will be made either with two wait states for memory mode 2, or three wait states for memory mode 3. The actual page size is variable, depending on the DRAM size.

DRAM SIZE	PAGE SIZE
64K	512 bytes
256K	1024 bytes
1M	2048 bytes

Multiple banks of memory operating in page mode may operate independently or may be interleaved. Interleaving may decrease the average number of wait states, thus increasing performance, but interleaving may only be done if the memory banks to be interleaved are the same size. Only banks 0 and 1 or banks 2 and 3 may be interleaved together when implementing 2-way interleave. When banks 0 and 1 are interleaved, bank 1 boundary registers should be programmed so that the bank is disabled and the bank 0 boundaries should be programmed as if bank 0 were twice the normal size. As an example, for a system with 2 banks of 256K DRAM operating independently, the banks could be programmed as shown in the upper diagram below.

When the banks are interleaved, the banks would be programmed as shown in the lower diagram below.
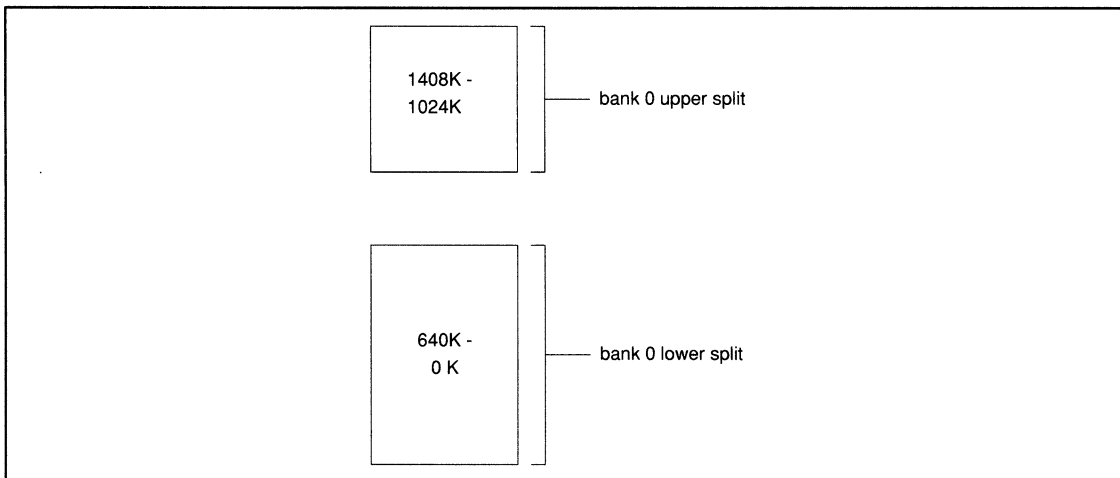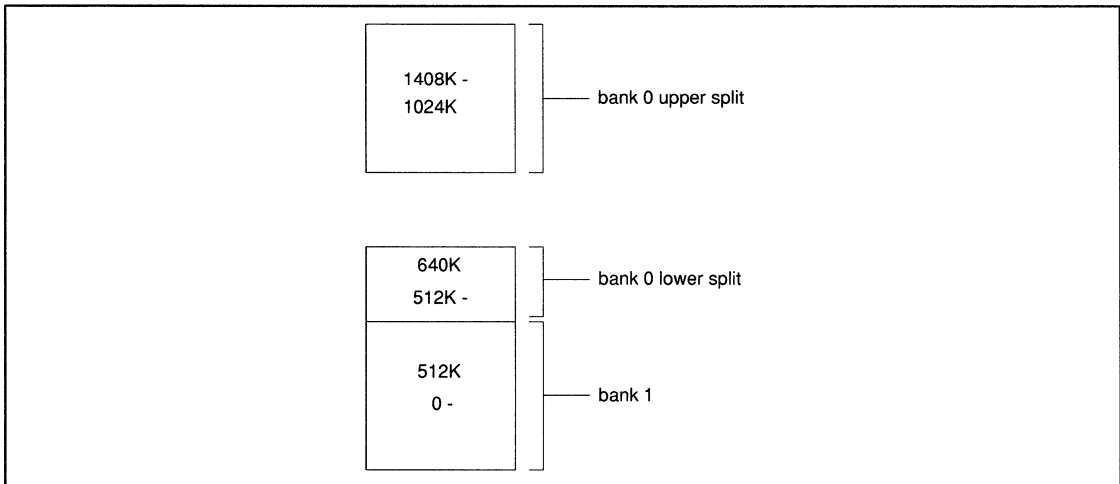
The following tables illustrate memory system characteristics with various configurations of memory and processor speed, both for page mode and non-page mode DRAM access.

For a page mode hit, the read and write accesses may have different performance. For a page mode miss or the first access to a page, the read and write accesses have the same performance. In a page mode miss, $\overline{RAS}$ starts out low and must be brought high for a RAS precharge time before the memory can be accessed.

NON-PAGE MODE	CPU FREQUENCY	WAIT STATES			DRAM SPEED
		READ	WRITE	EMS MISS	
MODE 4	8 MHz	0	0	2	120 ns
MODE 0	16 MHz	1	1	3	80 ns
MODE 4	12.5 MHz	1	1	2	120 ns

PAGE MODE	CPU FREQUENCY	WAIT STATES				DRAM SPEED
		READ	WRITE	NON-EMS MISS	EMS MISS	
MODE 2	12.5 MHz	0	1	2	3	120 ns
MODE 3	20 MHz	0	1	3	3	80 ns
MODE 3	16 MHz	0	1	3	3	100 ns
MODE 3	12.5 MHz	0	1	3	3	120 ns

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```
RAM SIZE CONFIGURATION REGISTER - BANK 1 AND 0

                ┌───────┬───────┐        SZ = 00 *: 256K
FFF70           │ BNK 1 │ BNK 0 │             01  : 1M
                │  SZ   │  SZ   │             10  : RESERVED
                └───────┴───────┘             11  : 64K
                  3   2   1   0


        RAM SIZE CONFIGURATION REGISTER - BANK 3 AND 2

                ┌───────┬───────┐        SZ = 00 *: 256K
FFF71           │ BNK 3 │ BNK 2 │             01  : 1M
                │  SZ   │  SZ   │             10  : RESERVED
                └───────┴───────┘             11  : 64K
                  3   2   1   0
```
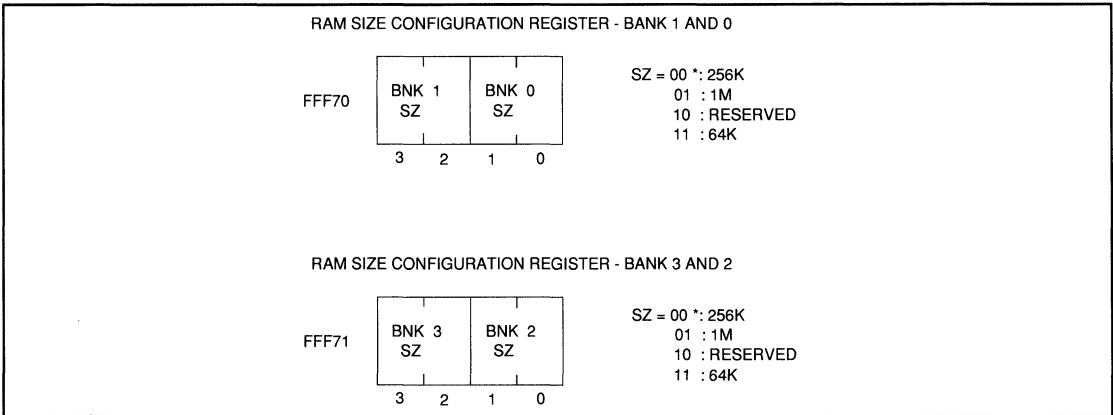
The DRAM timing is set by an external delay line for DMA or master mode transfers. The RAS leading edge becomes active from the active level of the MEMR or MEMW signals.

The DRAM timing modes are programmed by writing into register FFF72. The DRAM timing mode is actually switched during a processor hold state caused by a refresh, DMA, or bus master cycle. The Present DRAM Timing Mode register contains the current timing mode. Registers FFF72 and FFF73 will thus disagree until after a processor hold state occurs; typically, a refresh cycle will occur in 10 to 15 microseconds.
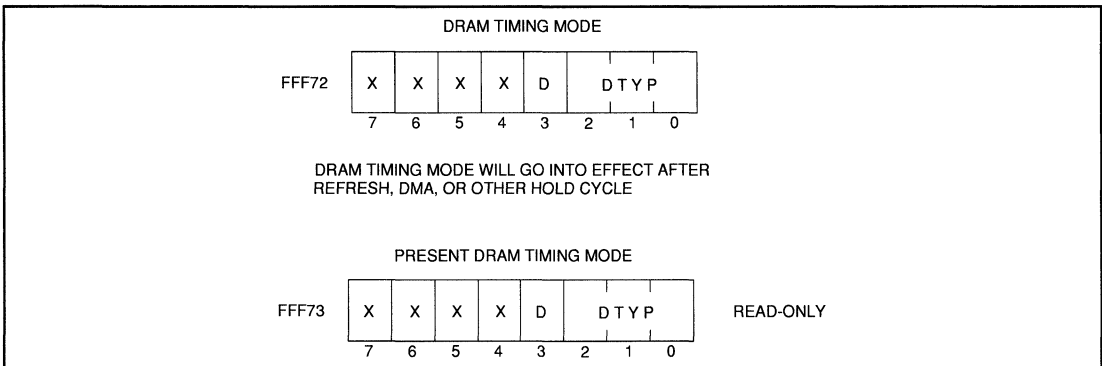
```
                        DRAM TIMING MODE

                ┌───┬───┬───┬───┬───┬───────────┐
FFF72           │ X │ X │ X │ X │ D │  D T Y P  │
                └───┴───┴───┴───┴───┴───────────┘
                  7   6   5   4   3   2   1   0

        DRAM TIMING MODE WILL GO INTO EFFECT AFTER
        REFRESH, DMA, OR OTHER HOLD CYCLE


                  PRESENT DRAM TIMING MODE

                ┌───┬───┬───┬───┬───┬───────────┐
FFF73           │ X │ X │ X │ X │ D │  D T Y P  │    READ-ONLY
                └───┴───┴───┴───┴───┴───────────┘
                  7   6   5   4   3   2   1   0
```

DTYP	DRAM MODE	
000*	Non-Page	(MODE 0)
001	Zero Wait State Read, One Wait State Write	(MODE 1)
010	Page Mode DRAM At 12.5 MHz CPU rate	(MODE 2)
011	Standard Page Mode for 8-20 MHz CPU rate	(MODE 3)
100	Identical to Mode 0, but RAS delayed one-half CPU clock	(MODE 4)
101	Non-Page for 8-12 MHz CPU rate,with 0 Wait States, RAS pulse width is 2 CPU clocks	(MODE 5)

* :   Default after Master Reset
D = 0: Normal operation (default)
1 :   Reversed for diagnostics;
        disables DRAM Page Mode Hit/Miss logic

8.0 EMS MEMORY

RAM memory above 1024K may be used both for expanded or extended memory. EMS memory may be as small as 128K bytes or as large as 7168K bytes. The EMS memory is accessed by two sets of EMS Page Registers, which reside in user I/O space. Each set of EMS Page Registers points to 36 blocks of memory, each block 16K bytes in size, which make up the EMS Page Frame. Four of the blocks are located above 640K, with the other 32 blocks located between 128K and 640K.

Each EMS Page Register is associated with one page of the EMS Page Frame, and consists of an enable bit and a 10 bit page number. When enabled, a 24 bit real address is formed by taking the 10 bit page number and appending the 14 bit address referencing the byte or word in the EMS page. The 24 bit address is then used to access the DRAM memory controlled by the FE3021.

In either page mode or non-page mode, if the DRAM row address does not change, then no additional wait states are required for EMS translation. This will allow EMS access without additional wait states if accesses are made to the same 512, 1024, or 2048 byte page, depending on DRAM size.

The EMS hardware must first be configured by programming the EMS control registers located in the FFF00-FFFFF register space, which is unlocked by writing to memory location FFF00 eight times. The I/O port locations of the EMS Page Registers are in user I/O space and their locations are selected with EMS Configuration Registers FFF75 and FFF78.

EMS Configuration Register FFF79 is used to completely enable or disable EMS, as well as to switch between the two sets of EMS Page registers. When the 'E' bit is '0', EMS operation is disabled and the EMS registers in user I/O space are inaccessible. When this is '0', it is as if the EMS hardware had been "unplugged" from the bus. When the 'E' bit is a '1', the EMS registers in the user I/O space become accessible. Registers FFF75 and FFF78 (which determine the I/O port addresses for the EMS logic), should be programmed prior to setting the 'E' bit to '1'.

4

EMS CONFIGURATION REGISTER N

FFF75 | N

| 3 | 2 | 1 | 0 |
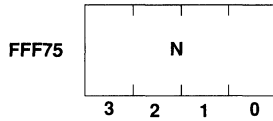
THIS REGISTER IS LOADED WITH '0110' BY MASTER RESET

EMS CONFIGURATION REGISTER M

FFF78 | M

| 3 | 2 | 1 | 0 |
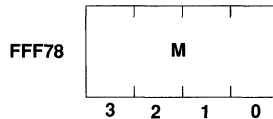
THIS REGISTER IS LOADED WITH '1000' BY MASTER RESET

EMS CONFIGURATION REGISTER

FFF79 | E | '0' | P F A
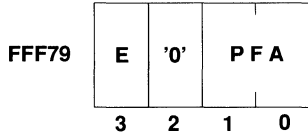
E=1: MASTER ENABLE FOR EMS
BIT 2 RESERVED, '0'

| 3 | 2 | 1 | 0 |

PFA = 00 : EMS PAGE FRAME C4000-D3FFF
PFA = 01 : EMS PAGE FRAME C8000-D7FFF
PFA = 10 : EMS PAGE FRAME CC000-DBFFF
PFA = 11 : EMS PAGE FRAME D0000-DFFFF
THIS REGISTER IS CLEARED BY MASTER RESET

	MSD						LSD		
FFF76	A23	A22	A21	A20	FFF77	A19	A18	A17	0/1*
	3	2	1	0		3	2	1	0

LOWER EMS BOUNDARY

THESE REGISTERS ARE SET TO '1111' BY MASTER RESET   * Don't care

Registers FFF76 and FFF77 are used to allocate memory for EMS, on 128K byte boundaries. Memory with addresses below the EMS boundary is accessed normally, as convenitioanl or extended memory.

On-board memory with addresses above the EMS boundary is reserved for use only as EMS memory. DRAM memory accesses to addresses above the EMS boundary are made to the expansion bus. This allows EMS, off-board, and on-board extended memory to be used simultaneously.

```
          EMS REGISTER              CPU ADDRESS

          ┌──────────────┐      ┌──────────────┐
          │      0       │      │   080FFF     │
          └──────────────┘      └──────────────┘
                    ╲              ╱
                     ╲            ╱

                 ┌────────────┬────────────┐
  RESULT 1:      │     0      │    0FFF     │
                 └────────────┴────────────┘
                 23        14  13          0

                 ┌──────────┐
                 │    10    │    EMS LOWER ADDRESS BOUNDARY
                 └──────────┘
                 23        16

                 ┌─────────────────────────┐
  RESULT 2:      │   1    0    0    FFF     │    GENERATED ADDRESS
                 └─────────────────────────┘
```
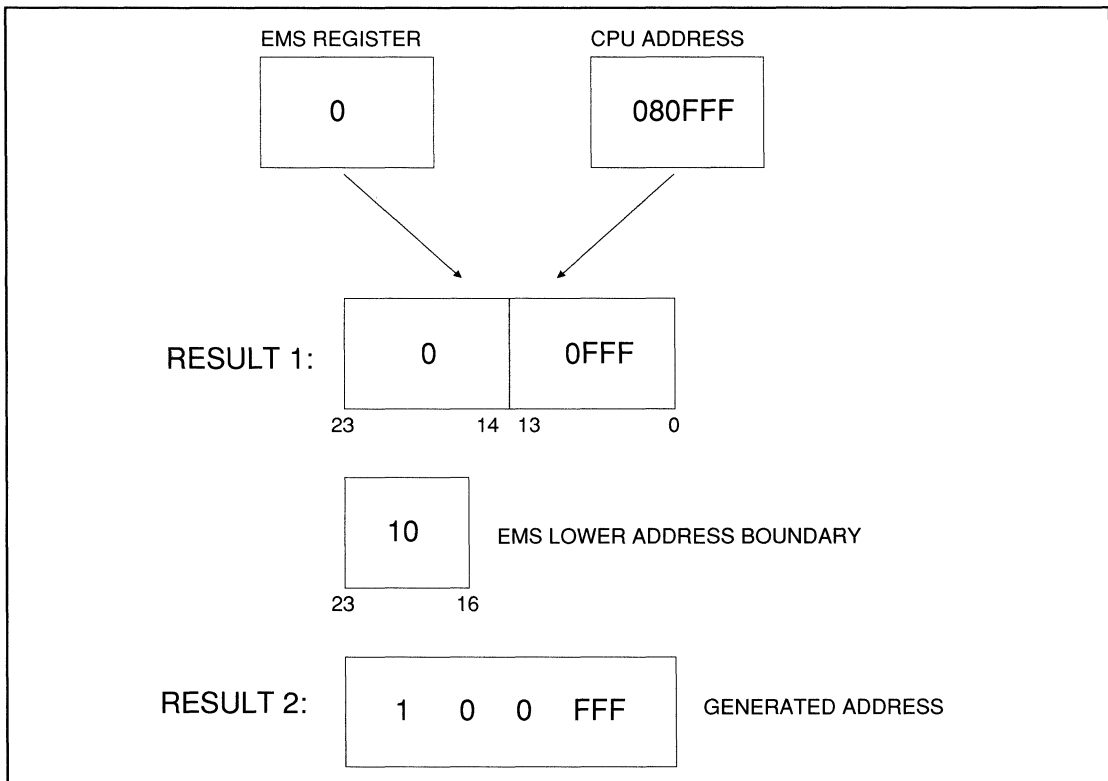
Any CPU address above 1 MB (the EMS lower address boundary), is assumed to reference memory on the expansion bus, rather than on-board memory, which prevents extended memory references from affecting on-board EMS memory.

EMS DMA Control Register FFF7A is used to control the selected EMS map register set during DMA or master transfers. This allows DMA transfers to be made to a particular EMS task, whether or not it is the currently selected task.

On-board memory may be allocated either to extended or to EMS memory in 128K byte blocks. EMS memory is allocated from the top of on-board memory down to the desired limit.

As an example, if the system contained 2 MB of DRAM, the memory map (without EMS) might look similar to figure 5a on the following page. The system would contain 640K of conventional memory and 1,280K of extended memory. The 1,280K of extended memory is composed of two parts: the original 1,024K and 256K of memory relocated from 0A0000 - 0E0000. The 128K area from 0E0000 - 0F0000 could also be relocated but in this example, it is not.

Figure 5b illustrates the memory map after EMS has been installed. The EMS boundary registers have been programmed so that on-board memory above 1,152K is reserved for EMS. 128K of on-board extended memory remains between 100000 - 120000. Additional extended memory could be added on the expansion bus, starting at 120000. Two EMS areas are shown, one 64K area at 0D0000 - 0E0000, and the other at 020000 - 0A0000.

Figure 5c shows the possible EMS page numbers ranging from 0 - 4F for the 1,280K of memory available for EMS paging.

Figure 4. EMS/Memory Map Configurations

a) 2 MB Memory Map before EMS installed

Index	Region	Size
23 22 21 20	256K	2304K / 2048K
11 10	EXTENDED	1024K
0F	64K FOR MAIN & VIDEO BIOS	
0E 0D 0C 0B 0A	ADAPTER FUNCTIONS	640K
09 08 07 06 05 04 03 02 01 00	CONVENTIONAL	0

b) EMS Installed

Index	Region	Size
	1152K REMOVED FOR EMS	2304K
11 10	128K EXTENDED	1152K / 1024K
0F		
0E		
0D	64K EMS	
0C 0B 0A	ADAPTER FUNCTIONS	640K
09 08 07 06 05 04 03 02	512K EMS	
01	128K	128K
00	CONVENTIONAL	0

c) Available EMS Memory

EMS PAGE #
(ADJUST ON, BIT 2 = 0)

47 ... 0	1152K
N/A ... N/A	0 K

72 PAGES TOTAL
= 1152K EMS

The EMS Control Register and EMS Page Registers are addressed in the user I/O port address space, I/O ports 100 (hex) through 3FF (hex). The EMS Control Registers and EMS Page Registers are selected when the I/O port address bits 9 - 6 match the value 'M' programmed by register FFF78 and the I/O port address bits 5 - 2 match the value 'N' programmed by register FFF75.

The EMS I/O Control Port is used to enable or disable EMS translation. When EMS translation is disabled, the EMS I/O control port and EMS page registers may still be accessed, but EMS page swapping will not occur.

The EMS I/O Control Port is also used to select the active page register set. When the processor accesses EMS memory, it always uses the register set specified by the TK bit. Normally, when DMA accesses EMS memory, it also uses the register set specified by the TK bit. Alternatively, the DMA transfer may be made using a particular register set, independently of the register set currently being used by the processor. This allows a DMA operation to start, continue, and finish while the processor is time-slicing and swapping back and forth between two programs.

The P and W fields for each page register are specified in the following table. Each EMS Page register is composed of a one bit enable bit (E) and a 10-bit page number (Q9-Q0). EMS translation for the EMS page is enabled when the E bit is a '1'.

EMS CONTROL REGISTER

EMS I/O CONTROL PORT	EMS	TK	DTK	DEN
	3	2	1	0

EMS = 1:   EMS TRANSLATION ENABLED

DEN = 0 :   DMA TRANSFERS MADE TO MAP REGISTER SET SPECIFIED BY "TK" BIT

DEN = 1 :   DMA TRANSFERS MADE TO MAP REGISTER SET SPECIFIED BY "DTK" BIT

EMS CONTROL REGISTER ADDRESS LOCATION

I/O PORT ADDRESS	X	X	X	X	1	1	M			N			X	X
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

EMS PAGE REGISTER - MSD

I/O PORT ADDRESS	P		1	0	M		N		W				E	O	Q9-Q8
	15 14 13 12	11	10 9	8 7	6 5	4 3 2	1 0						D3	D2	D1 D0

I/O PORT ADDRESS	P		0	1	M		N		W				Q7-Q4
	15 14 13 12	11	10 9	8 7	6 5	4 3 2	1 0						D3 D2 D1 D0

EMS PAGE REGISTER - LSD

I/O PORT ADDRESS	P		0	0	M		N		W				Q3-Q0
	15 14 13 12	11	10 9	8 7	6 5	4 3 2	1 0						D3 D2 D1 D0

9.0   TEST MODE

All output pins will become tristated if $\overline{\text{YMEMR}}$ and $\overline{\text{YMEMW}}$ are active simultaneously while $\overline{\text{MR}}$ is active. The outputs will remain tristated if $\overline{\text{MR}}$ is brought inactive while $\overline{\text{YMEMR}}$ and $\overline{\text{YMEMW}}$ are both active. The outputs will become active drivers again when $\overline{\text{MR}}$ is brought low without both $\overline{\text{YMEMR}}$ and $\overline{\text{YMEMW}}$ active. This "all output tristate" mode allows an in-circuit board tester to drive the FE3021 output pins.

P	W	EMS PAGE			
		PFA=00	PFA=01	PFA=10	PFA=11
0000	11	D0000-D3FFF	D4000-D7FFF	D8000-DBFFF	DC000-DFFFF
0000	10	CC000-CFFFF	D0000-D3FFF	D4000-D7FFF	D8000-DBFFF
0000	01	C8000-CBFFF	CC000-CFFFF	D0000-D3FFF	D4000-D7FFF
0000	00	C4000-C7FFF	C8000-CBFFF	CC000-CFFFF	D0000-D3FFF
1001	11	9C000-9FFFF	624K TO 640K		
1001	10	98000-9BFFF	608K TO 624K		
1001	01	94000-97FFF	592K TO 608K		
1001	00	90000-93FFF	576K TO 592K		
1000	11	8C000-8FFFF	560K TO 576K		
1000	10	88000-8BFFF	544K TO 560K		
1000	01	84000-87FFF	528K TO 544K		
1000	00	80000-83FFF	512K TO 528K		
0111	11	7C000-7FFFF	496K TO 512K		
0111	10	78000-7BFFF	480K TO 496K		
0111	01	74000-77FFF	464K TO 480K		
0111	00	70000-73FFF	448K TO 464K		
0110	11	6C000-6FFFF	432K TO 448K		
0110	10	68000-6BFFF	416K TO 432K		
0110	01	64000-67FFF	400K TO 416K		
0110	00	60000-63FFF	384K TO 400K		
0101	11	5C000-5FFFF	368K TO 384K		
0101	10	58000-5BFFF	352K TO 368K		
0101	01	54000-57FFF	336K TO 352K		
0101	00	50000-53FFF	320K TO 336K		
0100	11	4C000-4FFFF	304K TO 320K		
0100	10	48000-4BFFF	288K TO 304K		
0100	01	44000-47FFF	272K TO 288K		
0100	00	40000-43FFF	256K TO 272K		
0011	11	3C000-3FFFF	240K TO 256K		
0011	10	38000-3BFFF	224K TO 240K		
0011	01	34000-37FFF	208K TO 224K		
0011	00	30000-33FFF	192K TO 208K		
0010	11	2C000-2FFFF	176K TO 192K		
0010	10	28000-2BFFF	160K TO 176K		
0010	01	24000-27FFF	144K TO 160K		
0010	00	20000-23FFF	128K TO 144K		

Table 9. EMS Page Register Information

10.0 FE3021 PINOUT

As illustrated in Figure 5, the FE3021 is pack-
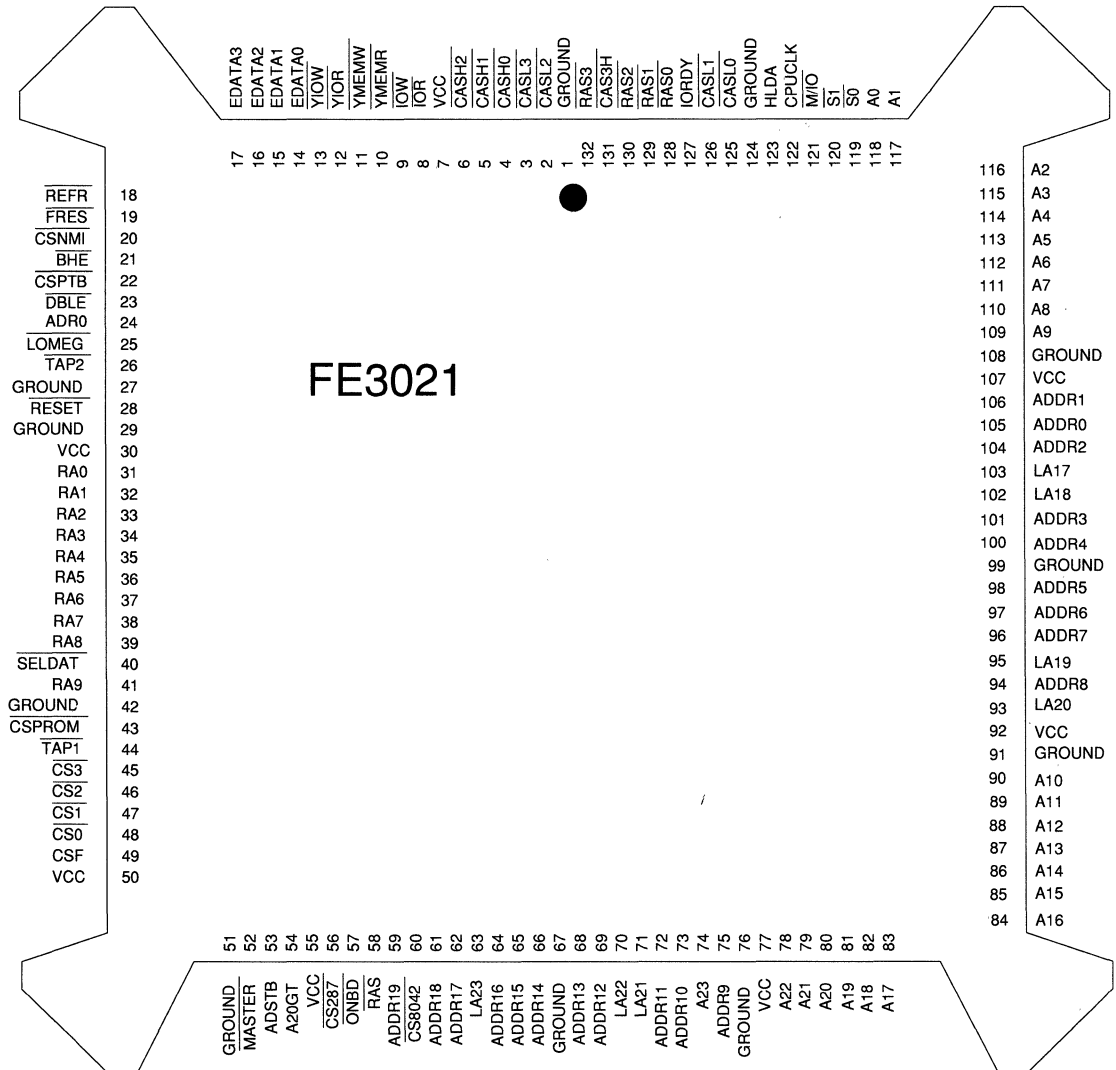aged in a 132-pin plastic flat pack. Table 10
groups the pins by function.

Figure 5. FE3021 Pin Assignment

AT BUS	
LA23	63
LA22	70
LA21	71
LA20	93
LA19	95
LA18	102
LA17	103
ADDR19	59
ADDR18	61
ADDR17	62
ADDR16	64
ADDR15	65
ADDR14	66
ADDR13	68
ADDR12	69
ADDR11	72
ADDR10	73
ADDR9	75
ADDR8	94
ADDR7	96
ADDR6	97
ADDR5	98
ADDR4	100
ADDR3	101
ADDR2	104
ADDR1	106
ADDR0	105
MASTER	52

GROUND	POWER
1	7
27	30
29	50
42	55
51	77
67	92
76	107
91	
99	
108	
124	

DATA BUS	
EDATA3	17
EDATA2	16
EDATA1	15
EDATA0	14

CHIP SELECTS AND CONTROL	
CS0	48
CS1	47
CS2	46
CS3	45
CSF	49
CS8042	60
CS287	56
CSNMI	20
CSPTB	22
ADSTB	53
SELDAT	40
YMEMR	10
YMEMW	11
YIOR	12
YIOW	13
IOR	8
IOW	9

MEMORY ADDRESS MUX	
RA9	41
RA8	39
RA7	38
RA6	37
RA5	36
RA4	35
RA3	34
RA2	33
RA1	32
RA0	31
RAS	58

80286 INTERFACE	
A23	74
A22	78
A21	79
A20	80
A19	81
A18	82
A17	83
A16	84
A15	85
A14	86
A13	87
A12	88
A11	89
A10	90
A9	109
A8	110
A7	111
A6	112
A5	113
A4	114
A3	115
A2	116
A1	117
A0	118
S0	119
S1	120
M/IO	121
CPUCLK	122
HLDA	123
IORDY	127

MEMORY CONTROL	
RAS0	128
RAS1	129
RAS2	130
RAS3	132
CASL0	125
CASL1	126
CASL2	2
CASL3	3
CASH0	4
CASH1	5
CASH2	6
CASH3	131
REFR	18
CSPROM	43
ONBD	57
BHE	21
DBLE	23
ADR0	24
LOMEG	25
A20GT	54

RESET	
RESET	28
FRES	19

Table 10.   FE3021 Pins Grouped By Function

11.0 DC OPERATING CHARACTERISTICS

T_a = 0˚ to 70˚ C,   Vcc = 5 V ± .25 V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
IIL	Input Leakage		±10	UA	VIN=.4 TO VCC
IOZ	Tri-State And Open Drain Output Leakage		±10	UA	VOUT=.4 TO VCC
VIH	Input High Voltage	2.0		V	
VIL	Input Lowvoltage		.8	V	
VILC	CPU Clock Input High Voltage	.6		V	
VILC	CPU Clock Input Low Voltage		.6	V	
ICC	Supply Current		50	mA	All Outputs Open, Inputs At 2.0V, CPUCLK = 16 MHz

For outputs: $\overline{\text{YIOR}}$, $\overline{\text{YIOW}}$, RA9-RA0, $\overline{\text{ONBD}}$, $\overline{\text{LOMEG}}$, A23-A0, CSF, $\overline{\text{CS0}}$, $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$, $\overline{\text{CS8042}}$, $\overline{\text{CS287}}$, $\overline{\text{CSNMI}}$, $\overline{\text{CSPTB}}$, $\overline{\text{RAS}}$, $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{RAS2}}$, $\overline{\text{RAS3}}$, CASL0, CASL1, CASL2, CASL3, CASH0, CASH1, CASH2, CASH3, CSPROM, $\overline{\text{DBLE}}$, $\overline{\text{FRES}}$, SELDAT, AND EDATA3-EDATA0

For outputs: ADDR19-ADDR0, LA23-LA17, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, IORDY

* 10 mA for $\overline{\text{IOR}}$, $\overline{\text{IOW}}$.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT=-1 mA
VOL	Output Low Voltage		.4	V	IOUT=1 mA

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT=-3 mA
VOL	Output Low Voltage		.4	V	IOUT=12 mA*

12.0 AC TIMING CHARACTERISTICS

load capacitance =   50 pF for outputs: CSF, $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CS8042}$, $\overline{CS287}$, $\overline{CSNMI}$, $\overline{CSPTB}$, $\overline{SELDAT}$, RA0-RA9, $\overline{ONBD}$, $\overline{LOMEG}$, DBLE, RAS, CSPROM, $\overline{YIOR}$, $\overline{YIOW}$, $\overline{FRES}$

load capacitance =   100 pF for output: IORDY, A19-A0, EDATA3-EDATA0

load capacitance =   200 pF for outputs: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, $\overline{CASL0}$, $\overline{CASL1}$, $\overline{CASL2}$, $\overline{CASL3}$, $\overline{CASH0}$, $\overline{CASH1}$, $\overline{CASH2}$, $\overline{CASH3}$, LA23-LA17, ADDR19-ADDR0, $\overline{IOR}$, $\overline{IOW}$

4

13.0 SYSTEM TIMING

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T1	CPUCLK Cycle	40		31		25	
T2	CPUCLK High Pulse	13		12			
T3	CPUCLK Low Pulse	11		10			
T4	A23-A0, MIO Setup To $\overline{S0}$ OR $\overline{S1}$ Falling	22		22			
T5	A23-A0, MIO To $\overline{ONBD}$		38		34		
T6	$\overline{S0}$, $\overline{S1}$ Setup To CPUCLK Falling	20		11		9	
T7	$\overline{S0}$, $\overline{S1}$ Hold From CPUCLK Falling	3		2		1	
T10	MIO, A23..A0 To LA23..LA17		50		45		45
T13	$\overline{YMEMR}$ To $\overline{CSPROM}$		45		38		30
T14	ADSTB To $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CSPTB}$, $\overline{CSF}$, $\overline{CS287}$, $\overline{CSNMI}$, $\overline{CS8042}$		45		35		35
T17a	$\overline{YIOR}$ To $\overline{IOR}$		40		35		35
T17	$\overline{YIOW}$ To $\overline{IOW}$		40		35		35
T18	ADSTB To ADDR19..ADDR1		50		45		45
T19	ADR0 To ADDR0		45		40		40
T20	Data Valid From $\overline{YMEMR}$ Or $\overline{YIOR}$ Active		180		150		150
T22	LA23..LA17 From CPUCLK Falling		50		45		45
T24	DATA Setup To $\overline{YMEMW}$ Or $\overline{YIOW}$ Inactive		180	150		150	
T25	Data Hold From $\overline{YMEMW}$ Or $\overline{YIOW}$ Inactive	10		10		10	
T26	$\overline{YIOR}$ Or $\overline{YMEMR}$ To $\overline{SELDAT}$		50		45		45
T27	$\overline{IOR}$ To $\overline{SELDAT}$, Master Mode Cycle		50		45		45
T28	ADSTB To Row Address; DMA Cycle, Non-EMS		50		42		35
T28a	ADSTB To Row Address; DMA Cycle, EMS		180		145		145

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T29	$\overline{YMEMR}$ To $\overline{RAS}$, $\overline{RAS3}$: $\overline{RAS0}$; Refresh Cycle		35		30		30
T30	$\overline{YMEMR}$ Or $\overline{YMEMW}$ To $\overline{RAS}$; DMA Cycle		35		30		30
T31	$\overline{TAP1}$ Falling To Column Address		45		37		30
T32	$\overline{YMEMR}$ Or YMEMW To $\overline{RAS3}..\overline{RAS0}$; DMA Cycle		35		30		30
T33	$\overline{TAP2}$ Falling To $\overline{CASL3}..\overline{CASL0}$, $\overline{CASH0}$; DMA Cycle		30		26		25
T34	$\overline{YMEMR}$ Or $\overline{YMEMW}$ Rising To $\overline{CASL3}...\overline{CASL0}$ Or $\overline{CASH3}..\overline{CASH0}$ Inactive		35		28		27
T35	$\overline{YMEMR}$ Active To $\overline{DLE}$ Active; DMA Or Master Mode		40		32		30
T36	$\overline{YMEMR}$ inactive To $\overline{DLE}$ inactive: DMA Or Master Mode		40		32		30
T37	$\overline{BHE}$ Or ADR0 Setup To CPUCLK Falling		25	20		20	
T38a	ADR0 Setup To CPUCLK Falling		25	20		20	
T38b	$\overline{BHE}$ Setup To CPUCLK Falling		25	20		20	
T39	A23..A1 To RA9..RA0 Row Address; Mode 0, 1, 4, 5		45		37		30
T40	$\overline{TAP1}$ Falling To RA9. . RA0 Column Address; Mode 0, 1, 4, 5		45		37		30
T41	RA9..RA0 Row Address Valid From CPUCLK At End Of CAS		50		39		
T43	CPUCLK Falling To $\overline{RAS}$; Mode 0, 1, & 5		35		30		30
T44	CPUCLK Falling To $\overline{RAS3}$; $\overline{RAS0}$; Mode 0 & 1 & 5		35		30		30
T45	CPUCLK Rising To $\overline{RAS}$; Mode 4		35		30		30
T46	CPUCLK Rising To $\overline{RAS3}..\overline{RAS0}$; Mode 4		35		30		30

4

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T47	$\overline{TAP2}$ Falling To $\overline{CASL3}$.. $\overline{CASL0}$; Or $\overline{CASH3}$..$\overline{CASH0}$ Active; Mode 0, 1, &4 & 5		35		25		25
T48	CPUCLK Falling To CASL3.. $\overline{CASL0}$ Or $\overline{CASH3}$.. $\overline{CASH0}$ Inactive; Mode 0, 1, & 4 & 5		35		27		27
T49	Row ADDR From $\overline{S0}$ Or $\overline{S1}$ Inactive; Mode 2		50		44		
T50	$\overline{TAP2}$ Falling To $\overline{DLE}$ Active; Mode 0, 1, 4, & 5		35		30		30
T51	CPUCLK Falling To $\overline{DLE}$ Inactive; Mode 0, 1, 4, & 5		35		30		30
T52	Ready Low From $\overline{S0}$ OR $\overline{S1}$ low		35		30		30
T53	Ready High From CPUCLK Falling		35		30		
T54	Column ADDR From CPUCLK Falling; Mode 2		40		34		
T56	$\overline{RAS3}$..$\overline{RAS0}$ Active From CPUCLK Falling; Mode 2		35		30		
T57	$\overline{CASL3}$..$\overline{CASL0}$ Or $\overline{CASH3}$.. $\overline{CASH0}$ Active From CPUCLK Rising; Mode 2		30		23		
T58	$\overline{CASL3}$ ..$\overline{CASL0}$ Or $\overline{CASH3}$ .. $\overline{CASH0}$ Inactive From CPUCLK Rising		30		23		
T5857	Difference Of CAS Inactive And Active Time (T58-T57)		4		4		
T59	$\overline{DLE}$ From CPUCLK		35		26		
T60	Row Address Valid From CPUCLK Falling; Mode 3		40		34		
T61	$\overline{RAS3}$ ..$\overline{RAS0}$ Inactive From $\overline{S0}$ Or $\overline{S1}$ Active		35		30		
T62	$\overline{RAS3}$ ..$\overline{RAS0}$ Inactive From HLDA Active		40		35		
T63	Column Address Hold From End Of CAS	1		1		1	
T64	Column Address From CPUCLK; MODE 2 & 3		50		44		

4

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T65	Column Address From A23-A1		45		37		
T66	$\overline{RAS3}$ .. $\overline{RAS0}$ Active From CPUCLK Rising; Mode 3		35		30		
T67	$\overline{CASL3}$ .. $\overline{CASL0}$ Or $\overline{CASH3}$ .. $\overline{CASH0}$ Active From CPUCLK;Mode 3		28		23		
T68	$\overline{CASL3}$ .. $\overline{CASL0}$ Or $\overline{CASH3}$ .. $\overline{CASH0}$ Inactive From CPUCLK Rising; Mode 3		28		23		
T6867	Difference Of CAS Inactive And Active Time (T68-T67)		4		4		
T69	$\overline{REFR}$ To $\overline{ONBD}$		40		35		35
T70	Refresh Address Valid From $\overline{REFR}$		50		39		35
T72	$\overline{MASTER}$ Active To LA[23:17], ADDR[16:0] High Impedance		45		45		45
T73	$\overline{MASTER}$ Inactive To LA[23:17], ADDR [16:0] Low Impedance		45		45		45
T74	ADDR[9:0] To Chip Selects				65		65
T75	$\overline{MASTER}$ Active To A[23:0], ADR0 Low Impedance		45		45		45
T76	$\overline{MASTER}$ Inactive To A[23:0], ADR0 High Impedance		45		45		45
T77	LA[23:17], ADDR[16:1] To RA[9:0]		45		40		40
T78	$\overline{MASTER}$ Active To $\overline{YIOR}$, $\overline{YIOW}$ Low Impedance		45		45		45
T79	$\overline{MASTER}$ Inactive To $\overline{YIOR}$, YIOW High Impedance		45		45		45
T80	$\overline{MASTER}$ Active To $\overline{IOR}$, $\overline{IOW}$ High Impedance		45		45		45
T81	$\overline{MASTER}$ Inactive To $\overline{IOR}$, $\overline{IOW}$ Low impedance		45		45		45
T82a	$\overline{IOR}$ To $\overline{YIOR}$		30		25		25
T82b	$\overline{IOW}$ To $\overline{YIOW}$		30		25		25
T83	LA[23:17], ADDR[16:0] To A[23:0], ADRO		40		35		35

NOTE 1 : LA23 - LA17 LATCHED AT MIDDLE OF Ts UNTIL MEMORY OR I/O STROBE

Figure 6. Basic Timing

4

CPUCLK

A23-A0,
MIO

$\overline{S0}$, $\overline{S1}$

LA23-LA17

$\overline{IOR}$, $\overline{IOW}$,
$\overline{MEMR}$, $\overline{MEMW}$

Ts   Tc   Tw   Tw   Tw   Tw

t 22

(NOTE 2)

NOTE 2: FOR OFF-BOARD CYCLES, LA23 - LA17 LATCHED AT MIDDLE OF Ts UNTIL
         2 CPUCLK's AFTER MEMORY OR I/O STROBE
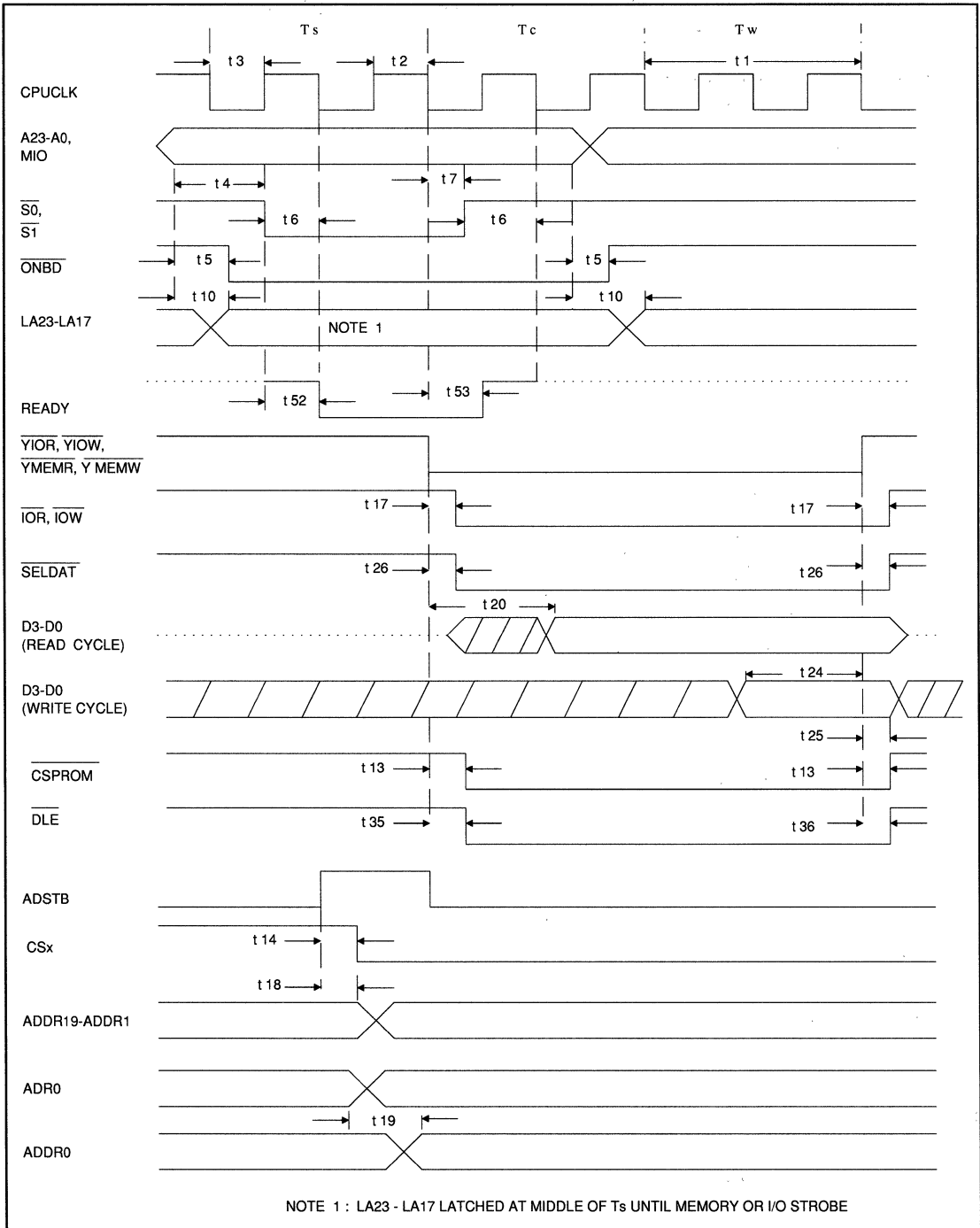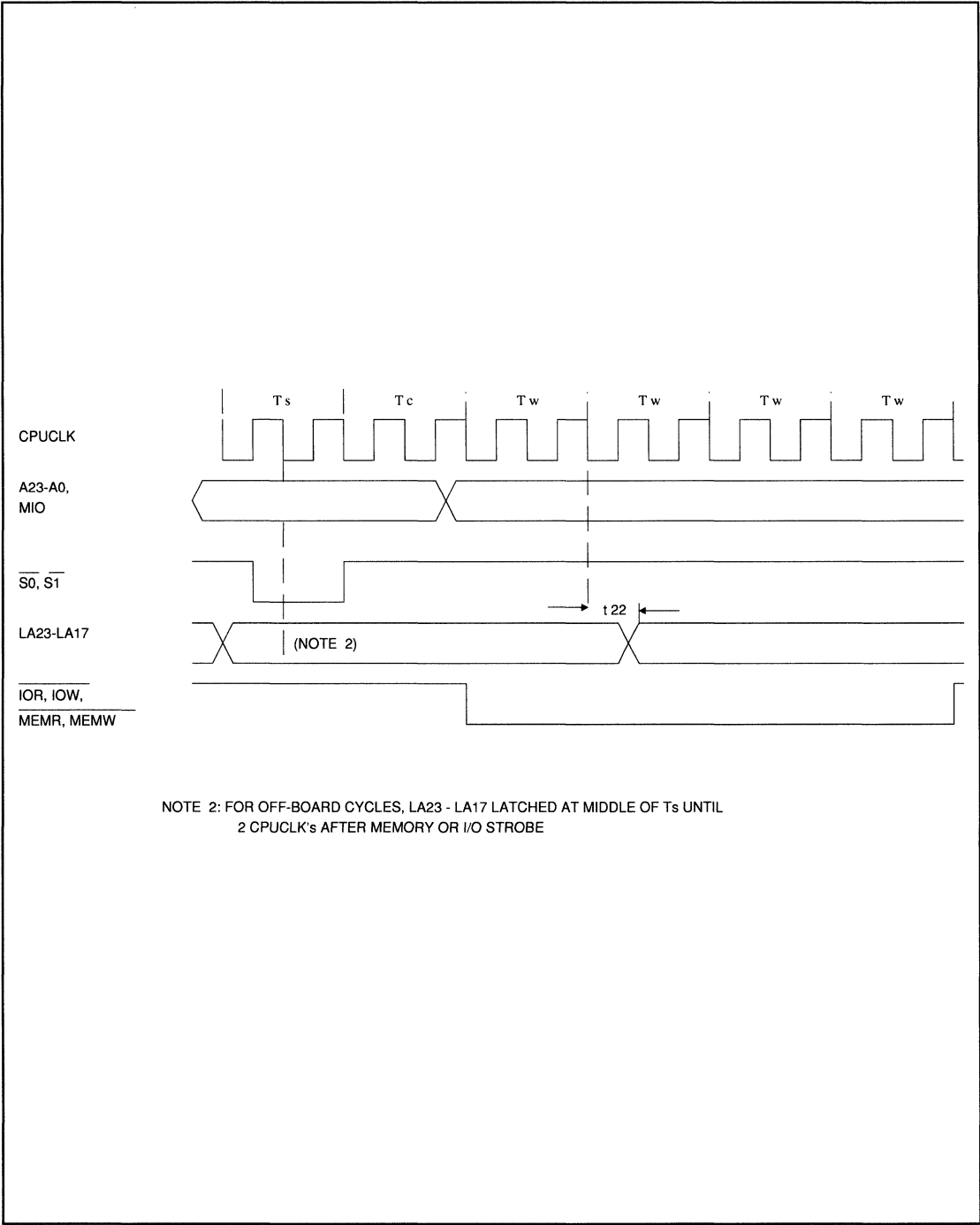
Figure 7. High Speed Mode LA23-LA17 Timing
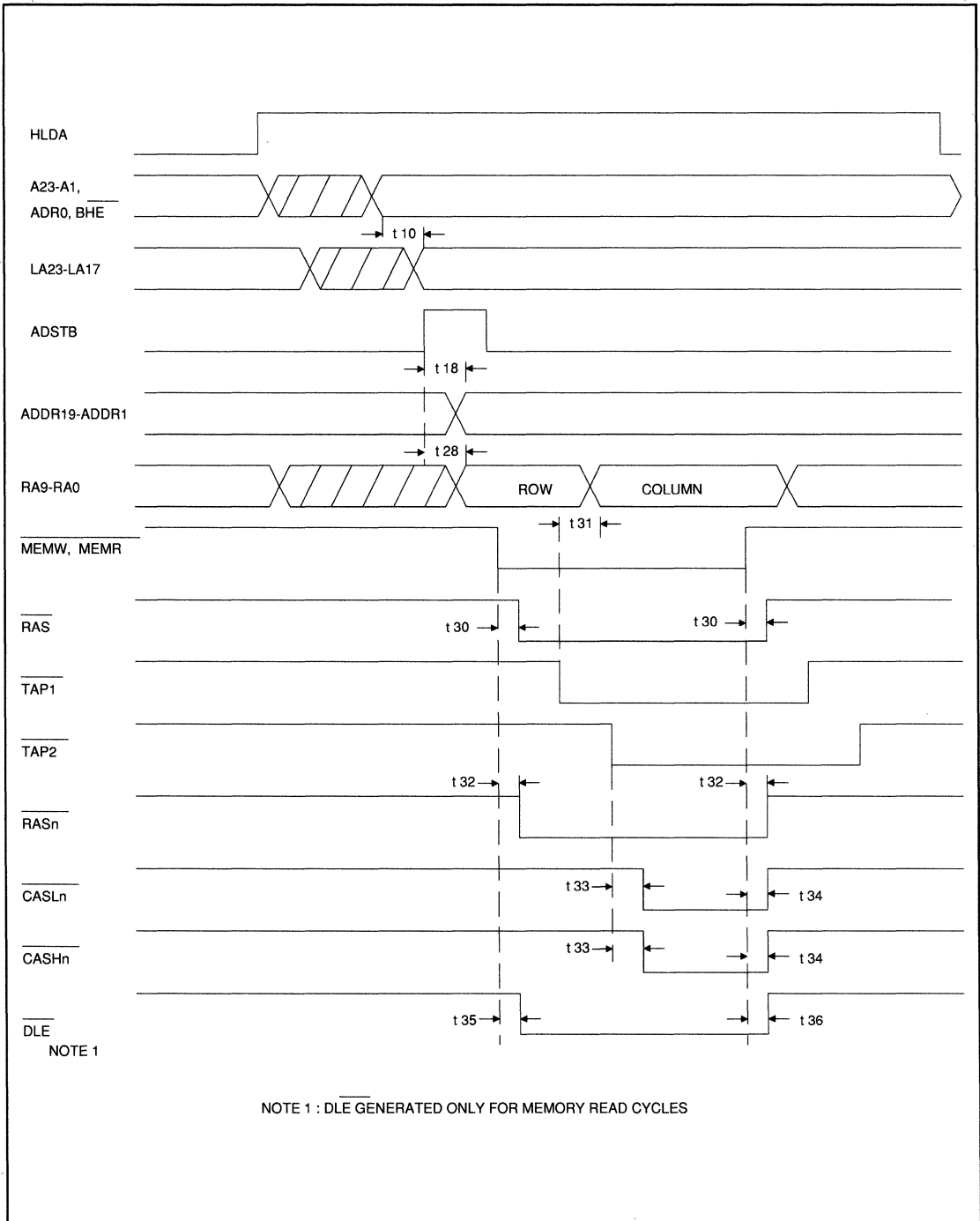
Figure 8. DMA Memory Cycle

4

NOTE 1: DLE GENERATED ONLY FOR MEMORY READ CYCLES
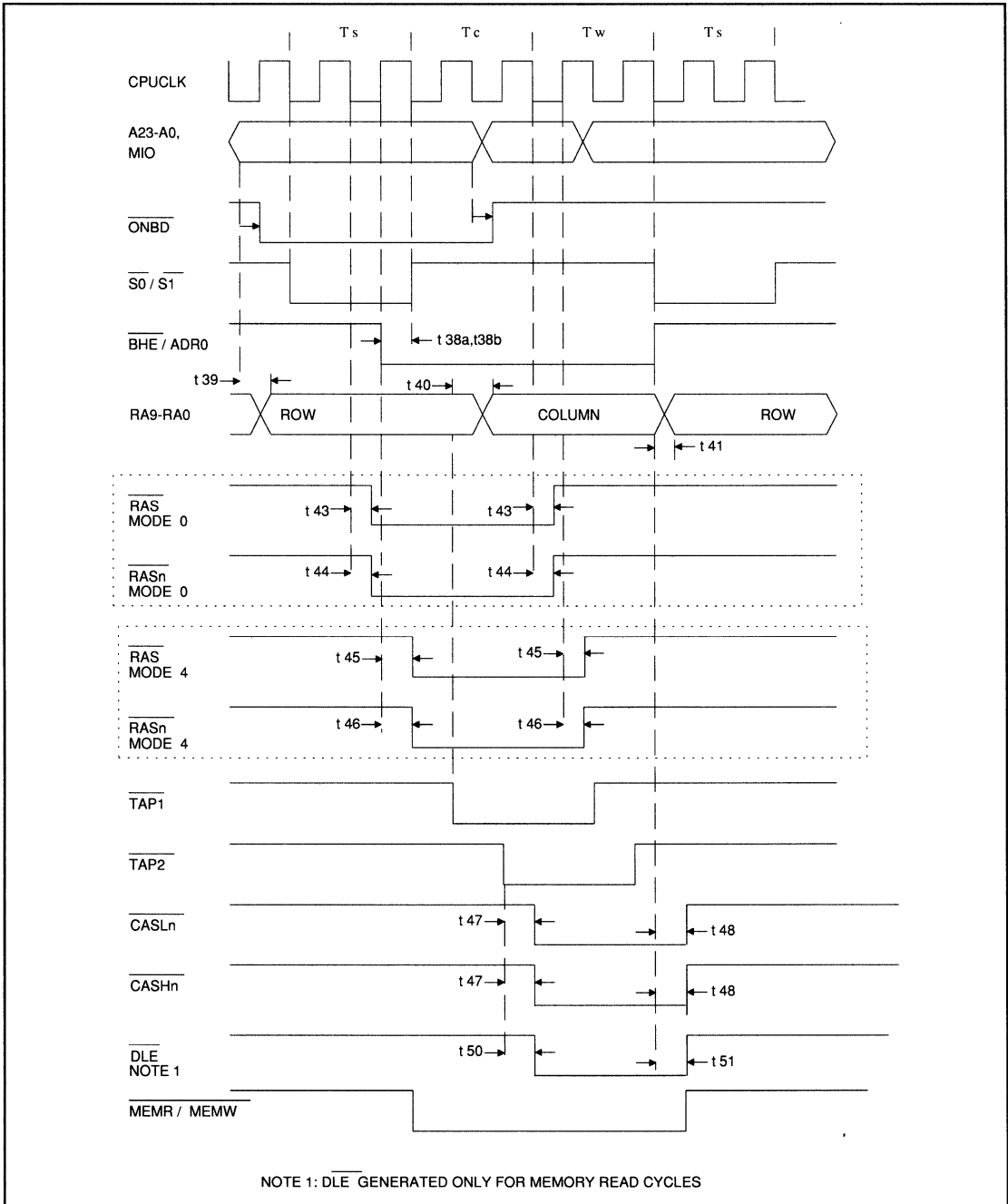
Figure 9. Memory Modes 0 & 4 (Non-page Mode)
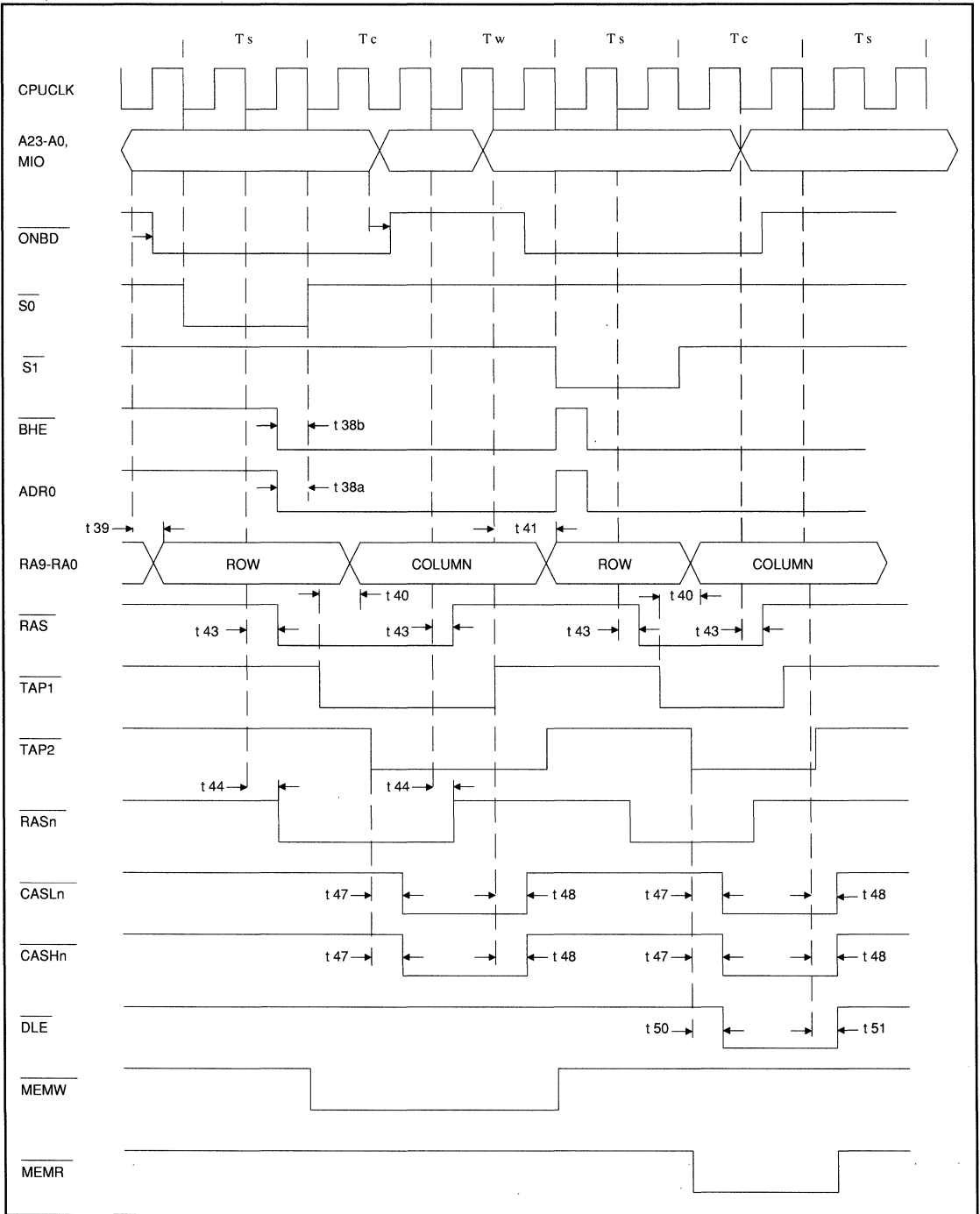
Figure 10. Memory Mode 1 (Non-Page 0 WS Read/1 WS Write)

4
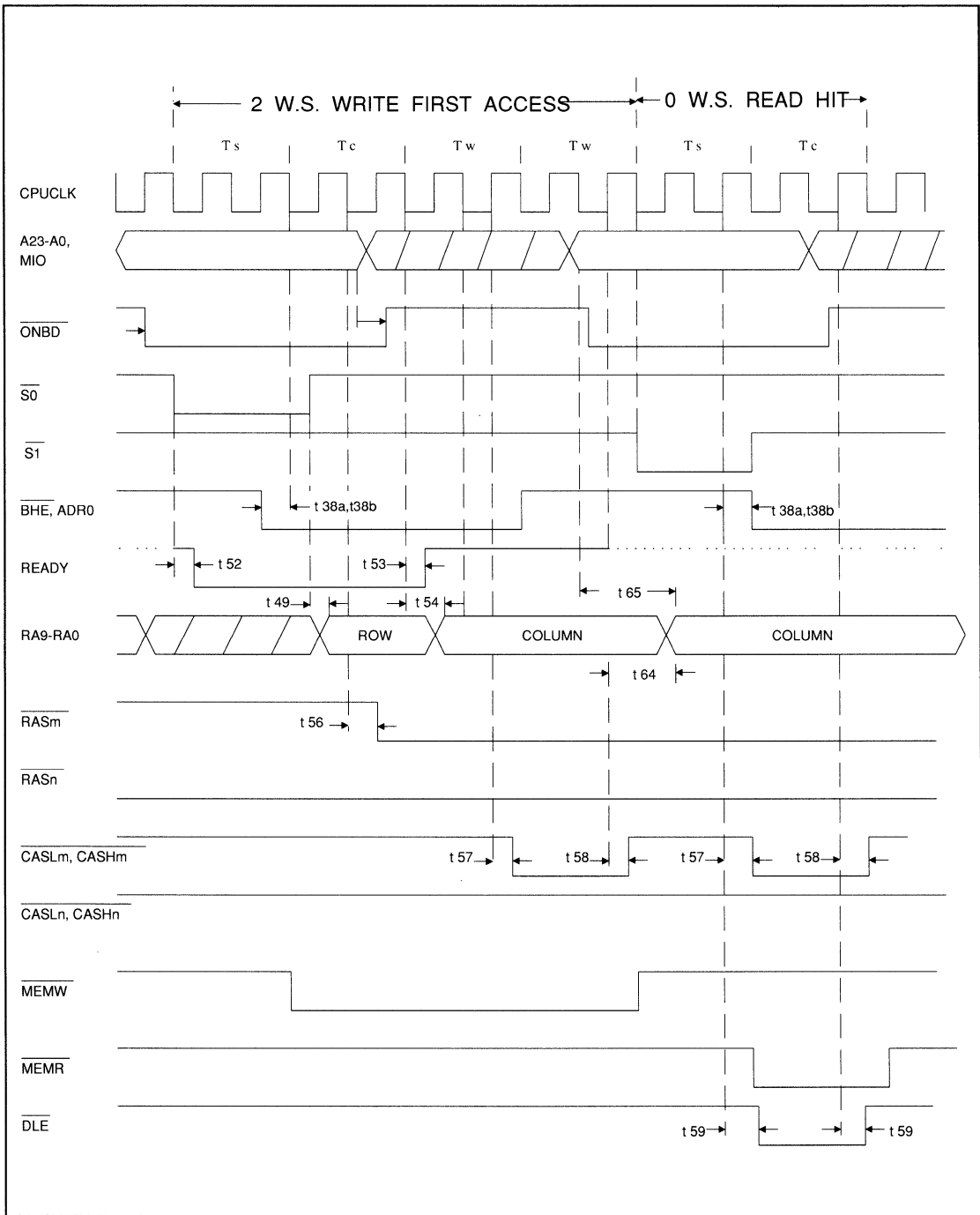
Figure 11. Memory Mode 2 (PAGE) 1 0F 2
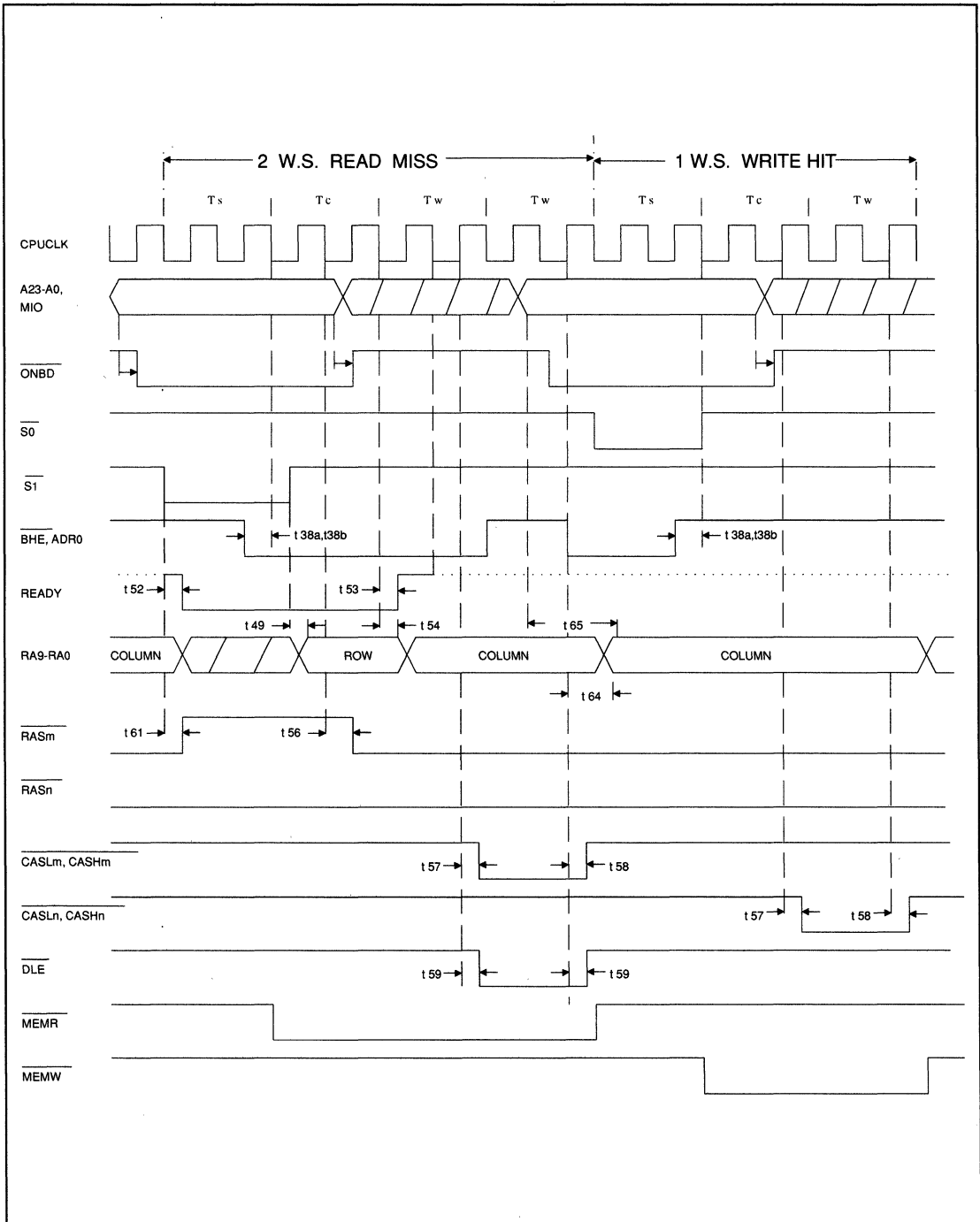
Figure 12. Memory Mode 2 (PAGE) 2 OF 2

4
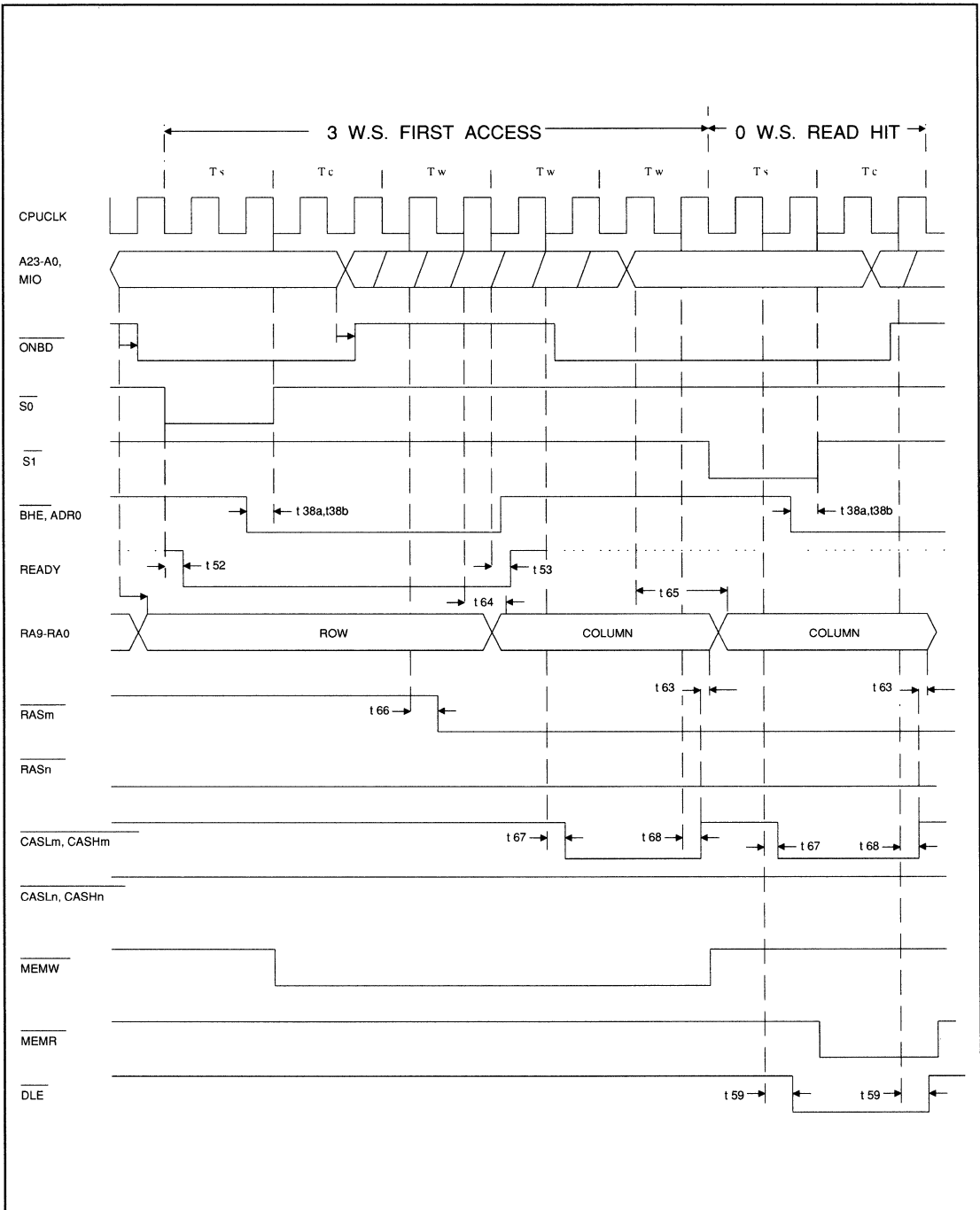
Figure 13. Memory Mode 3 (PAGE) 1 OF 2
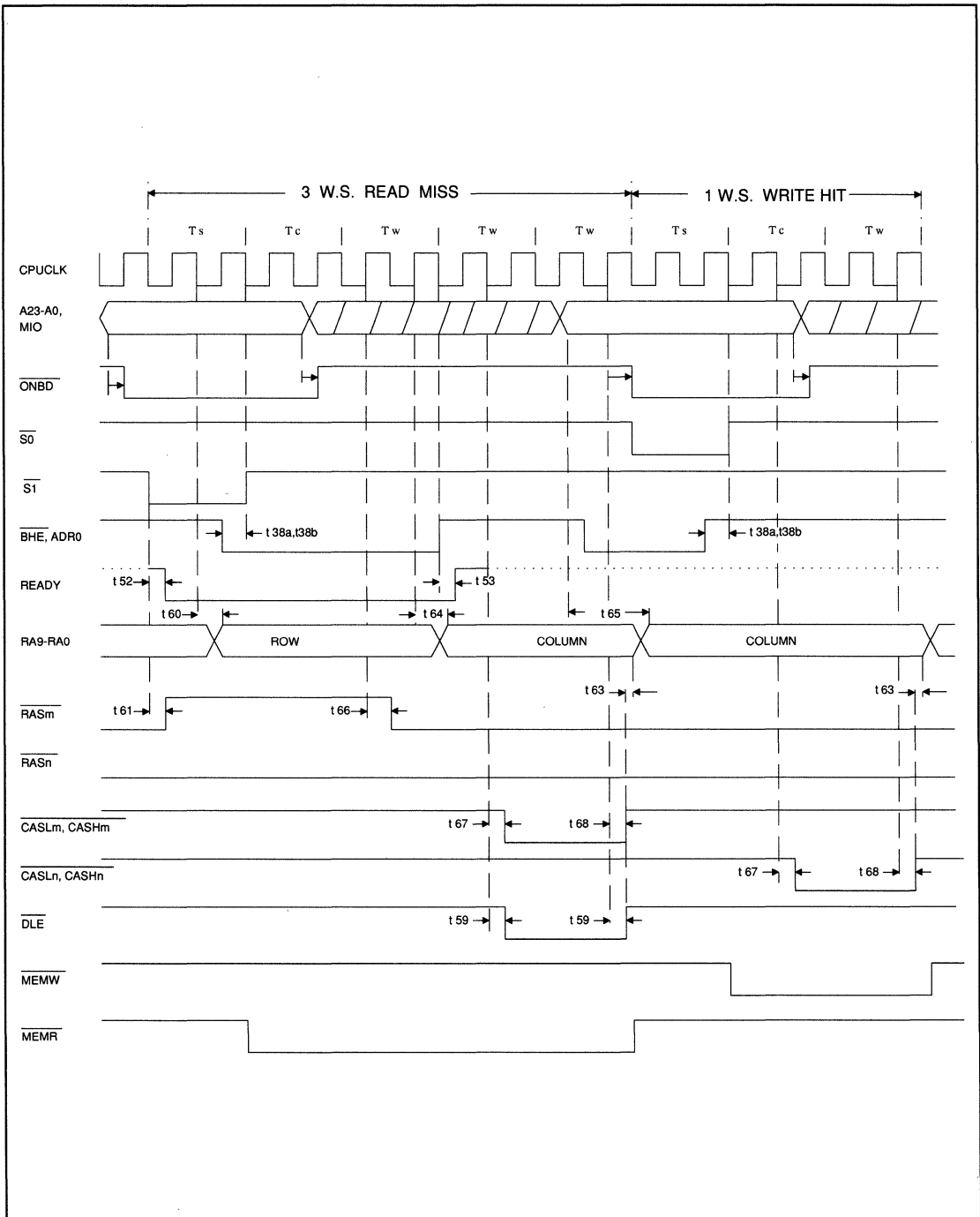
Figure 14. Memory Mode 3 (PAGE) 2 OF 2
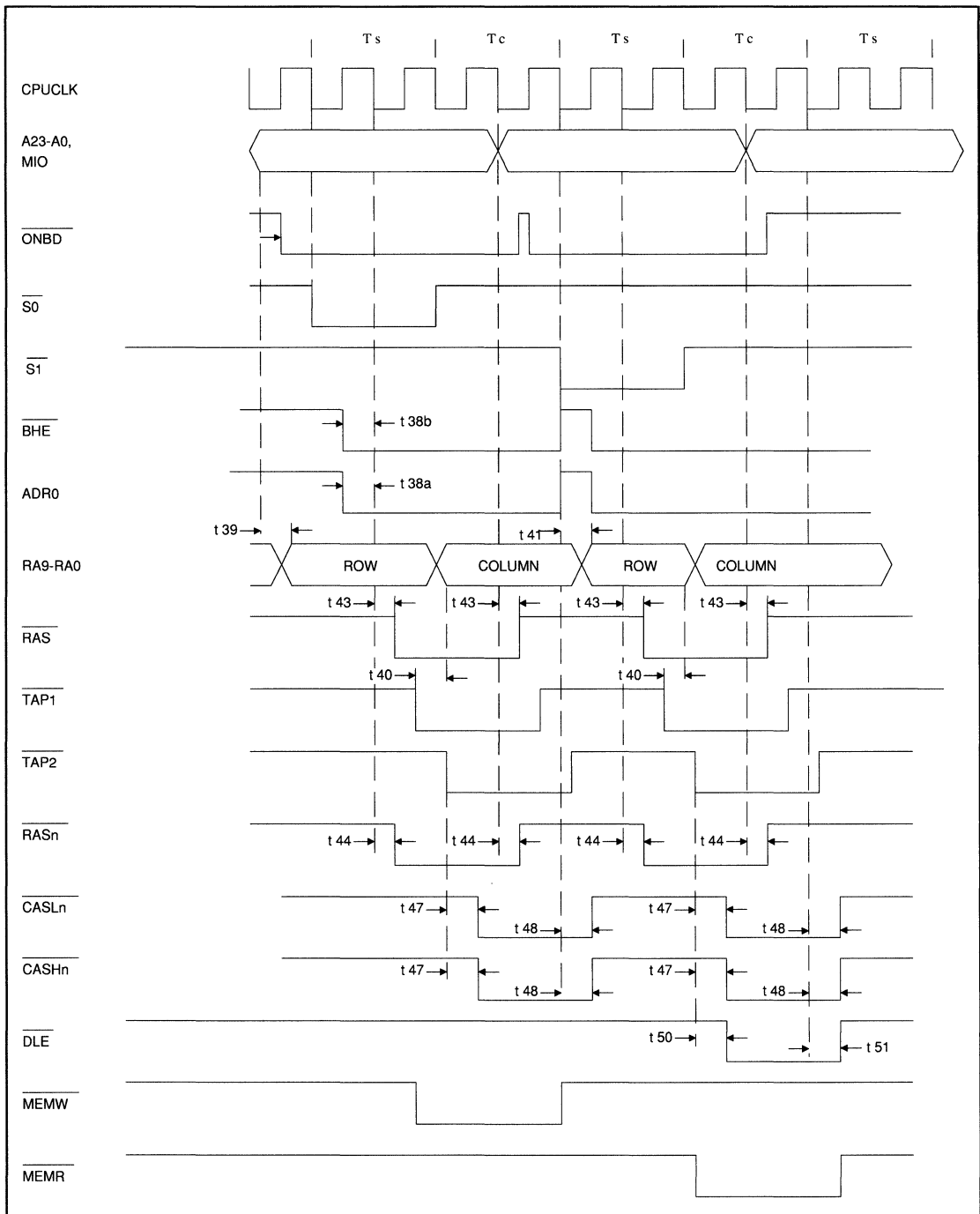
Figure 15. Memory Mode 5 (Non-Page) 0 WS Read & Write

Figure 16. Refresh Cycle

4
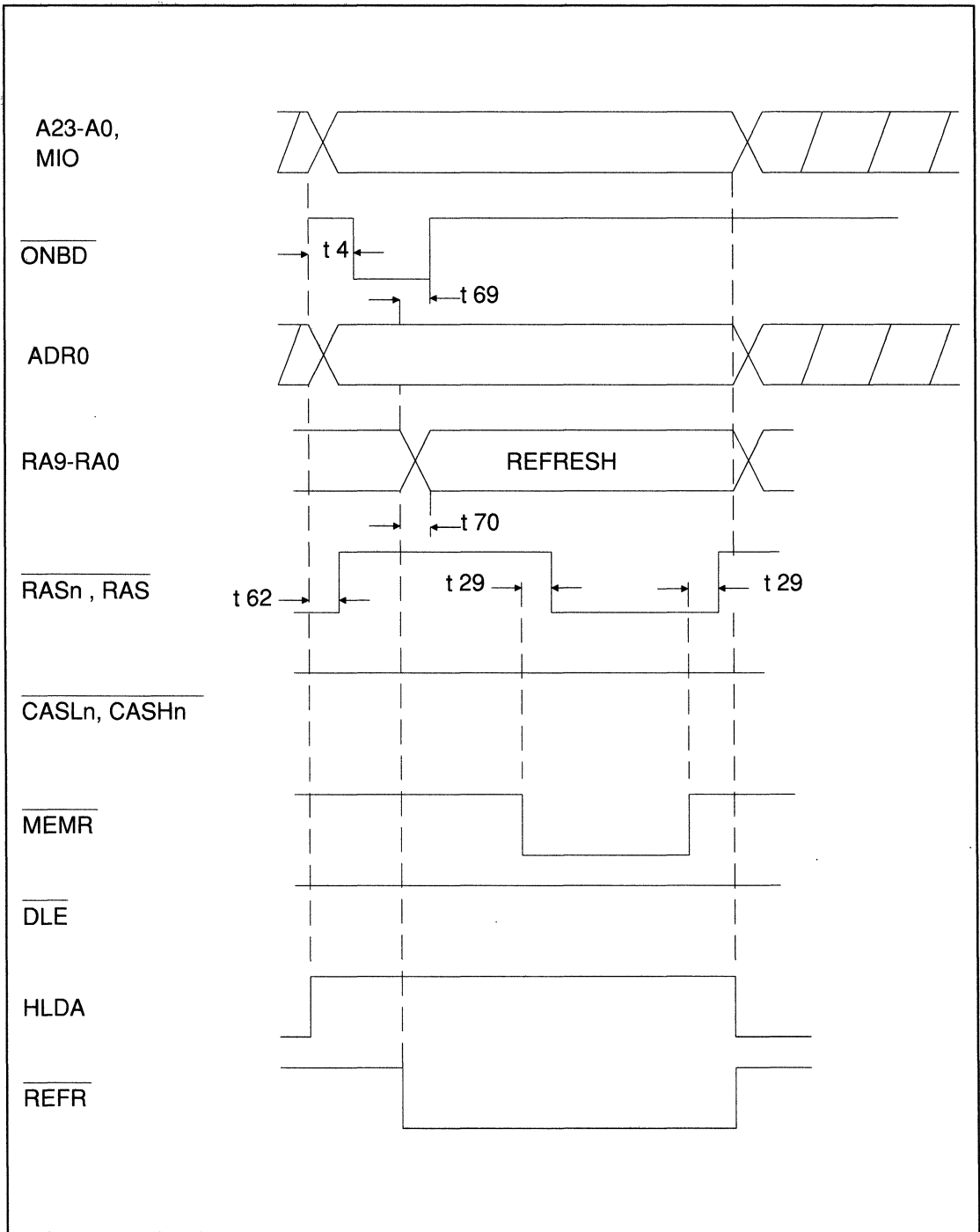
NOTE 1 : DLE GENERATED ONLY FOR MEMORY READ CYCLES
NOTE 2 : EARLY PRODUCTION FE3021 REQUIRES ADSTB HIGH DURING MASTER CYCLE
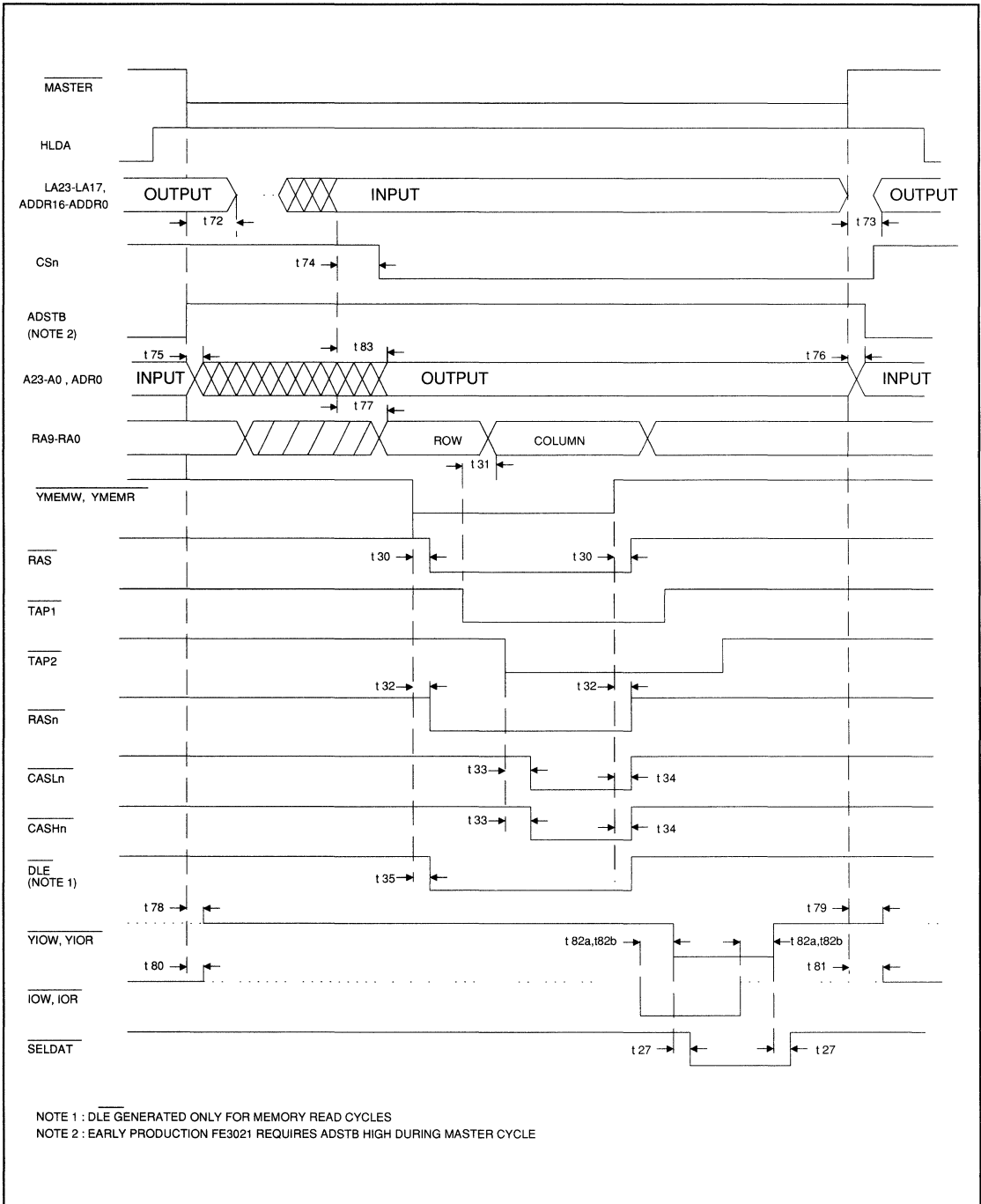
Figure 17. Bus Master Cycle

14.0 PACKAGE DIAGRAMS
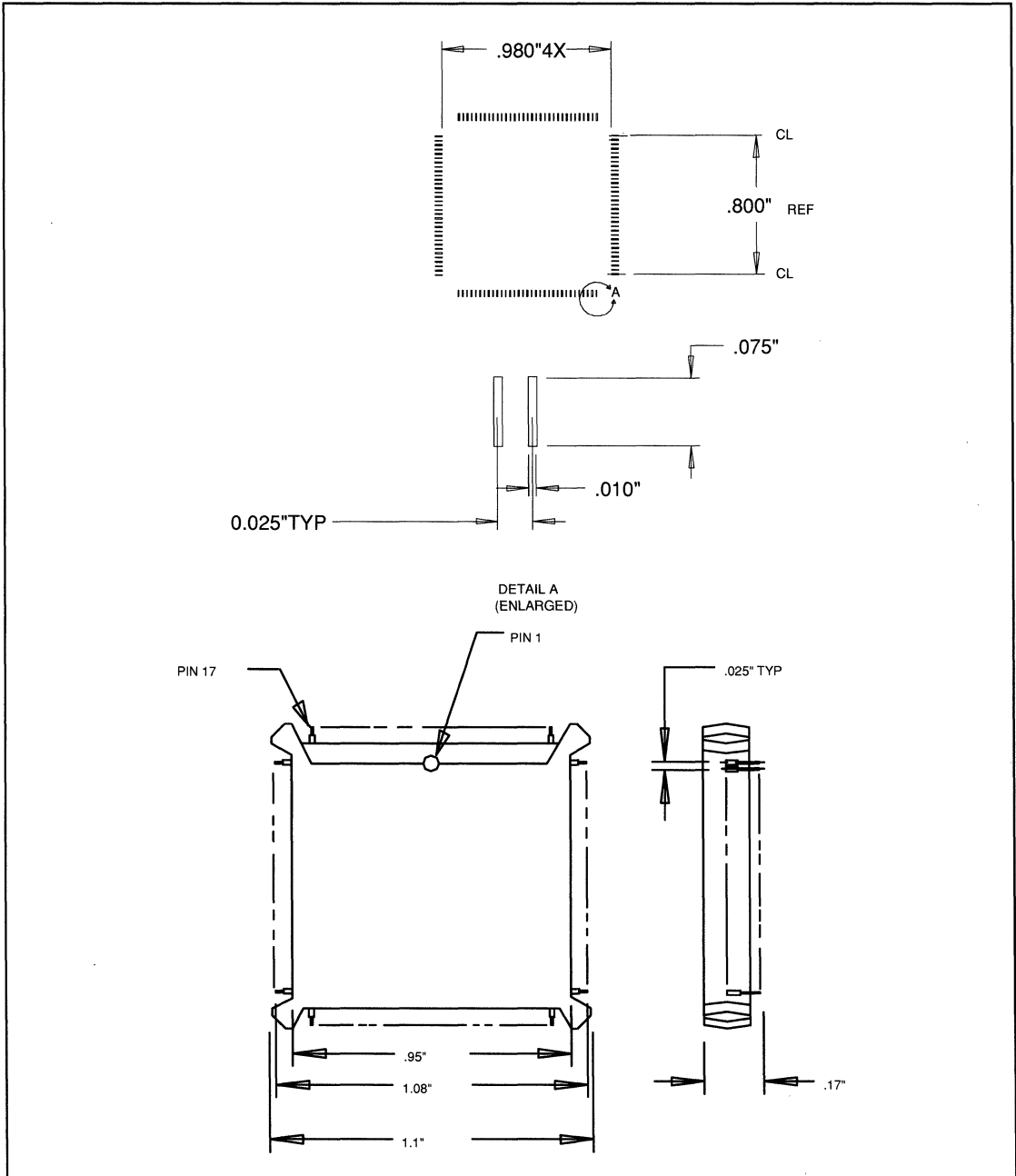
Figure 18. 132-Pin JEDEC Flat Pack Packaging Diagram
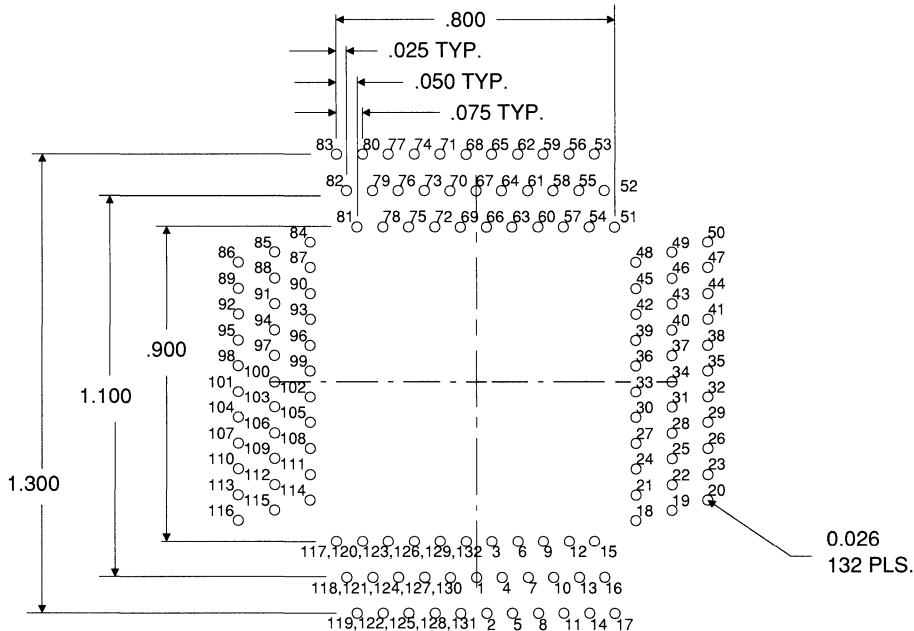
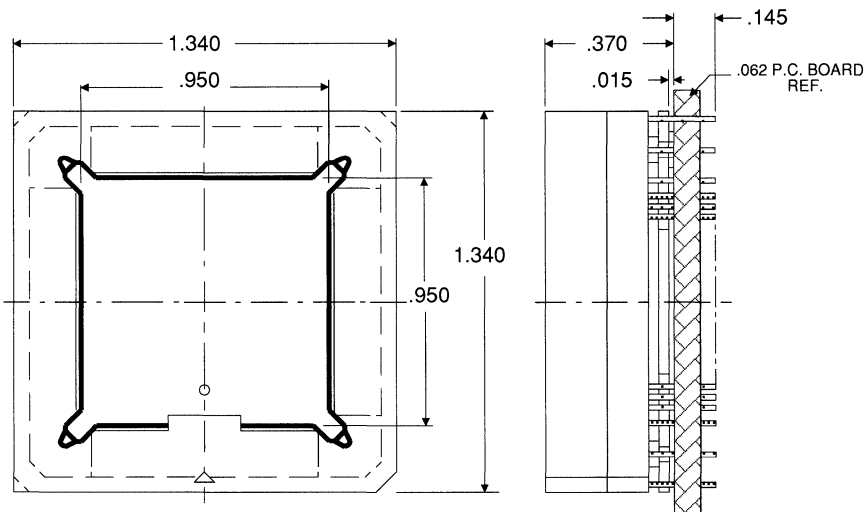RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-5

Figure 19. Socket Diagram