TOSHIBA AMERICA, INC.

MOS
MEMORY

MOS
MEMORY

April 1987

TOSHIBA

MOS MEMORY PRODUCTS

DATA BOOK

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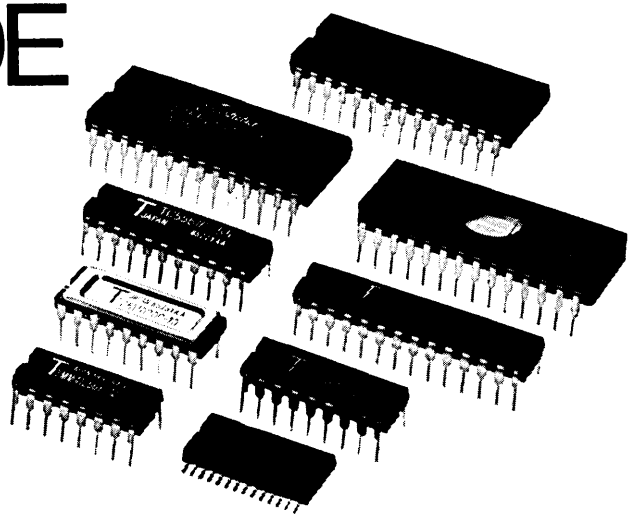
MEMORY PRODUCT GUIDE



1. Dynamic RAM

Capacity	Type No.	Organi-zation	Access Time, Max(ns)		Cycle Time Min.(ns)	Process	Power Dissipation, Max.(mW)		Pins	Operating Mode
			t_{RAC}	t_{CAC}			Active	Standby		
256K Bit	TMM41256P/T-12	262,144×1	120	60	220	NMOS	330	28	16/18	Page
	TMM41256P/T-15		150	75	260		275			
	*TMM41256AP/AT/AZ-10	262,144×1	100	50	190	NMOS	440	28	16/18/16	Page
	*TMM41256AP/AT/AZ-12		120	60	220		396			
	*TMM41256AP/AT/AZ-15		150	75	260		358			
	TMM41257P/T-12	262,144×1	120	60	220	NMOS	385	28	16/18	Nibble
	TMM41257P/T-15		150	75	260		330			
	*TMM41257AP/AT/AZ-10	262,144×1	100	50	190	NMOS	440	28	16/18/16	Nibble
	*TMM41257AP/AT/AZ-12		120	60	220		396			
	*TMM41257AP/AT/AZ-15		150	75	260		358			
	TMM41464P-12	65,536×4	120	60	220	NMOS	385	28	18	Page
	TMM41464P-15		150	75	260		330			
1M Bit	TC511000P/J/Z-85	1,048,576×1	85	25	165	CMOS	385	5.5	18/26/20	Fast Page
	TC511000P/J/Z-10		100	25	190		330			
	TC511000P/J/Z-12		120	30	220		275			
	TC511001P/J/Z-85	1,048,576×1	85	30	165	CMOS	385	5.5	18/26/20	Nibble
	TC511001P/J/Z-10		100	35	190		330			
	TC511001P/J/Z-12		120	40	220		275			
	TC511002P/J/Z-85	1,048,576×1	85	25	165	CMOS	385	5.5	18/26/20	Static Column
	TC511002P/J/Z-10		100	25	190		330			
	TC511002P/J/Z-12		120	30	220		275			
	TC514256P/J/Z-85	262,144×4	85	30	165	CMOS	413	5.5	20/26/20	Fast Page
	TC514256P/J/Z-10		100	30	190		358			
	TC514256P/J/Z-12		120	35	220		303			
	TC514258P/J/Z-85	262,144×4	85	30	165	CMOS	413	5.5	20/26/20	Static Column
	TC514258P/J/Z-10		100	30	190		358			
	TC514258P/J/Z-12		120	35	220		303			

NOTE: PACKAGE TYPE P: PLASTIC DIP T: PLCC J: SOJ Z: ZIP *NEW PRODUCT

2. Dynamic RAM HYBRID MODULE

Capacity	Type No.	Organi-zation	Access Time, Max(ns)		Cycle Time Min.(ns)	Dram Units	Power Dissipation, Max.(mW)		Pins	Module
			t_{RAC}	t_{CAC}			Active	Standby		
8M Bit	*THM81000S-10	1,048,576×8	100	25	190	TC511000J	2,640	44	30	SIMM
	*THM81000S-12		120	30	220		2,200			
	*THM81000L-10	1,048,576×8	100	25	190	TC511000J	2,640	44	30	SIP
	*THM81000L-12		120	30	220		2,200			
9M Bit	*THM91000S-10	1,048,576×9	100	25	190	TC511000J	2,970	49.5	30	SIMM
	*THM91000S-12		120	30	220		2,475			
	*THM91000L-10	1,048,576×9	100	25	190	TC511000J	2,970	49.5	30	SIP
	*THM91000L-12		120	30	220		2,475			

3. STANDARD APPLICATION Static RAM

Capacity	Type No.	Organi-zation	Access Time Max.(ns)	Cycle Time Min.(ns)	Process	Power Dissipation Max.(mW)		Pins	Package Width (inch)
						Active	Standby		
16K Bit	TMM2015BP-90	2,048×8	90	90	NMOS	275	27.5	24	0.3
	TMM2015BP-10		100	100					
	TMM2015BP-12		120	120					
	TMM2015BP-15		150	150					
	TMM2016BP-90	2,048×8	90	90	NMOS	275	27.5	24	0.6
	TMM2016BP-10		100	100					
	TMM2016BP-12		120	120					
	TMM2016BP-15		150	150					
	TC5517CP/CF-15	2,048×8	150	150	CMOS	27.5	0.165	24	0.6(P) 0.45(F)
	TC5517CP/CF-20		200	200					
	TC5517CPL/CFL-15		150	150			0.005		
	TC5517CPL/CFL-20		200	200					
	TC5518CP/CF-15	2,048×8	150	150	CMOS	27.5	0.165	24	
	TC5518CP/CF-20		200	200					
	TC5518CPL/CFL-15		150	150			0.005		
	TC5518CPL/CFL-20		200	200					
64K Bit	TMM2063P-10	8,192×8	100	100	NMOS	440	55	28	0.3
	TMM2063P-12		120	120					
	TMM2063P-15		150	150					
	TMM2064P-10	8,192×8	100	100	NMOS	440	55	28	0.6
	TMM2064P-12		120	120					
	TMM2064P-15		150	150					
	TC5563APL-10	8,192×8	100	100	CMOS	27.5	0.55	28	0.3
	TC5563APL-12		120	120					
	TC5563APL-15		150	150					
	TC5563APL-10L		100	100			0.165		
	TC5563APL-12L		120	120					
	TC5563APL-15L		150	150					
	TC5565APL/AFL-10	8,192×8	100	100	CMOS	27.5	0.55	28	0.6(P) 0.45(F)
	TC5565APL/AFL-12		120	120					
	TC5565APL/AFL-15		150	150					
	TC5565APL/AFL-10L		100	100			0.165		
	TC5565APL/AFL-12L		120	120					
	TC5565APL/AFL-15L		150	150					
	*TC5564APL/AFL-12	8,192×8	120	120	CMOS	27.5	0.005	28	0.6(P) 0.45(F)
	*TC5565APL/AFP-15		150	150					
256K Bit	TC55257P-10	32,768×8	100	100	CMOS	27.5	5.5	28	0.6
	TC55257P-12		120	120					
	TC55257PL-85		85	85			0.55		
	TC55257PL-10		100	100					
	TC55257PL-12		120	120					
	*TC55257AP/AF-10	32,768×8	100	100	CMOS	27.5	5.5	28	0.6(P) 0.45(F)
	*TC55257AP/AF-12		120	120					
	*TC55257APL/AFL-10		100	100			0.55		
	*TC55257APL/AFL-12		120	120					

PSEUDO-STATIC RAM

256K Bit	TC51832P-85	32,768×8	85	135	CMOS	303	5.5	28	.6
	TC51832P-10		100	160		248			
	TC51832P-12		120	190		220			

NOTE: PACKAGE TYPE P: PLASTIC DIP F: FLAT PACKAGE (SOP) *NEW PRODUCT

4. HIGH SPEED Static RAM

Capacity	Type No.	Organi-zation	Access Time Max.(ns)	Cycle Time Min.(ns)	Process	Power Dissipation Max.(mW)		Pins	Package Width (inch)
						Active	Standby		
16K Bit	*TMM2018AD/AP-25	2,048×8	25	25	NMOS	660	110	24	0.3
	*TMM2018AD/AP-35		35	35		550			
	*TMM2018AD/AP-45		45	45		440			
	*TMM2068AD/AP-25	4,096×4	25	25	NMOS	660	110	20	0.3
	*TMM2068AD/AP-35		35	35		550			
	*TMM2068AD/AP-45		45	45		440			
	*TMM2078AD-25	4,096×4	25	25	NMOS	660	110	22	0.3
	*TMM2078AD-35		35	35		550			
	*TMM2078AD-45		45	45		440			
64K Bit	*TMM2088P-35	8,192×8	35	35	NMOS	660	55	28	0.3
	*TMM2088P-45		45	45					
	*TMM2088P-55		55	55					
72K Bit	*TMM2089C-35	8,192×9	35	35	NMOS	660	55	28	0.3
	*TMM2089C-45		45	45					
	*TMM2089C-55		55	55					
64K Bit	TC5561P-55	65,536×1	55	55	CMOS	550	0.55	22	0.3
	TC5561P-70		70	70					
	TC5562P-45	65,536×1	45	45	CMOS	550	11	22	
	TC5562P-55		55	55					
	*TC55416P-35	16,384×4	35	35	CMOS	440	55	22	0.3
	*TC55416P-45		45	45		330			
	*TC55417P-35	16,384×4	35	35	CMOS	440	55	24	0.3
	*TC55417P-45		45	45		330			

NOTE: PACKAGE MATERIAL D: CERDIP C: CERAMIC DIP P: PLASTIC DIP *NEW PRODUCT

5. EPROM

Capacity	Type No.	Organi-zation & Process	Access Time Max.(ns)	Cycle Time Min.(ns)	Power Supply (V)	Temperature Range (°C)	Power Dissipation Max.(mW)		Pins	Programming Algorithm
							Active	Standby		
64K Bit	TMM2764AD-15	8,192×8 NMOS	150	150	5V±5%	0~70	525	158	28	I or II
	TMM2764AD-20		200	200						
	TMM2764ADI-15		150	150		−40~85	630	184		
	TMM2764ADI-20		200	200						
	TMM2764AD-150		150	150	5V±10%	0~70	660	193		
	TMM2764AD-200		200	200						
128K Bit	TMM27128AD-15	16,384×8 NMOS	150	150	5V±5%	0~70	525	158	28	I or II
	TMM27128AD-20		200	200						
	TMM27128ADI-15		150	150		−40~85	630	184		
	TMM27128ADI-20		200	200						
	TMM27128AD-150		150	150	5V±10%	0~70	660	193		
	TMM27128AD-200		200	200						
256K Bit	TMM27256AD-15	32,768×8 NMOS	150	150	5V±5%	0~70	525	158	28	I or II
	TMM27256AD-20		200	200						
	TMM27256ADI-15		150	150		−40~85	630	184		
	TMM27256ADI-20		200	200						
	TMM27256AD-150		150	150	5V±10%	0~70	660	193		
	TMM27256AD-200		200	200						
	TC57256D-20	32,768×8 CMOS	200	200	5V±5%	21.0	158	0.525	28	I or II
	TC57256D-25		250	250						
	*TC57256AD-15		150	150	5V±5%	12.5				
	*TC57256AD-20		200	200						
512K Bit	TMM27512D-20	65,536×8 NMOS	200	200	5V±5%	0~70	630	184	28	I or II
	TMM27512D-25		250	250						
	TMM27512DI-20		200	200		−40~85	683	210		
	TMM27512DI-25		250	250						
	TMM27512D-200		200	200	5V±10%	0~70	715	220		
	TMM27512D-250		250	250						
1M Bit	*TC571000D-15	131,072×8 CMOS	150	150	5V±5%	−40~85	158	0.525	32	II
	*TC571000D-20		200	200						
	*TC571001D-15		150	150						
	*TC571001D-20		200	200						

NOTE: PACKAGE MATERIAL D: CERDIP

*NEW PRODUCT

6. ONE TIME PROM

Capacity	Type No.	Organi-zation & Process	Access Time Max.(ns)	Cycle Time Min.(ns)	Power Supply (V)	Temperature Range (°C)	Power Dissipation Max.(mW)		Pins	Programming Algorithm
							Active	Standby		
64K Bit	TMM2464AP/AF	8,192×8 NMOS	200	200	5V+5%	−40~85°C	525	158	28	I or II
128K Bit	TMM24128AP/AF	16,384×8 NMOS	200	200	5V+5%	−40~85°C	525	158	28	I or II
256K Bit	TMM24256AP/AF	32,768×8 NMOS	200	200	5V+5%	−40~85°C	525	158	28	I or II
	*TC54256AP/AF	32,768×8 CMOS	200	200	5V±5%		158	0.525	28	I or II
512K Bit	TMM24512P/F	65,536×8 NMOS	250	250	5V±5%	−40~85°C	630	184	28	I or II

NOTE: PACKAGE TYPE P: PLASTIC DIP F: FLAT PACKAGE (SOP) *NEW PRODUCT

7. Mask ROM

Capacity	Type No.	Organi-zation	Access Time Max.(ns)	Cycle Time Min.(ns)	Process	Power Dissipation Max.(mW)		Pins
						Active	Standby	
256K Bit	TC53257P/F	32,768×8	200	200	CMOS	138	0.11	28
1M Bit	TC531000AP/AF	131,072×8	200	200	CMOS	138	0.11	28
2M Bit	TC532000P	262,144×8	200	200	CMOS	220	0.11	32
4M Bit	*TC534000P	524,288×8	250	250	CMOS	220	0.11	32

NOTE: PACKAGE TYPE P: PLASTIC DIP F: FLAT PACKAGE *NEW PRODUCT

1. 256K Bit Dynamic RAM

Organization	256K×1 (page mode)	256K×1 (nibble mode)	64K×4 (page mode)
TOSHIBA	TMM41256AP/AT/AZ	TMM41257AP/AT/AZ	TMM41464AP/AT/AZ
Fujitsu	MB81256	MB81257	MB81464
Hitachi	HM50256	HM50257	HM50464
Mitsubishi	M5M4256	M5M4257	M5M4464
NEC	μPD41256	μPD41257	μPD41464
Oki	MSM41256	MSM41257	MSM41464
TI	TMS4256	TMS4257	TMS4464

2. 1M×1 Dynamic RAM

Organization	1MB×1 (Fast page mode)		1MB×1 (Nibble mode)		1MB×1 (Static column mode)	
SUPPLIER	PART#	PROCESS	PART#	PROCESS	PART#	PROCESS
TOSHIBA	TC511000	CMOS	TC511001	CMOS	TC511002	CMOS
FUJITSU	MB81C1000	CMOS	MB81C1001	CMOS	MB81C1002	CMOS
HITACHI	HM511000	CMOS	HM511001	CMOS	HM511002	CMOS
MITSUBISHI	M5M4C1000	CMOS	M5M4C1001	CMOS	M5M4C1002	CMOS
NEC	μPD421000	CMOS	μPD421001	CMOS	μPD421002	CMOS
TI	TMS4C1024	CMOS	TMS4C1025	CMOS	TMS4C1027	CMOS
AT&T	M411024PP	CMOS	—		M411024PK	CMOS
NMB	AAA1M101	CMOS	AAA1M102	CMOS	AAA1M100	CMOS
SAMSUNG	KM41C1000	CMOS	KM41C1001	CMOS	KM41C1002	CMOS

3. 256K×4 Dynamic RAM

Organization	256K×4 (Fast page mode)		256K×4 (Static column mode)	
SUPPLIER	PART#	PROCESS	PART#	PROCESS
TOSHIBA	TC514256	CMOS	TC514258	CMOS
FUJITSU	MB81C4256	CMOS	—	
HITACHI	HM514256	CMOS	HM514258	CMOS
MITSUBISHI	M5M44C256	CMOS	M5M44C258	CMOS
NEC	μPD424256	CMOS	μPD424258	CMOS
TI	TMS44C256	CMOS	TMS44C257	CMOS
SHARP	LH64257	CMOS	LH64256	CMOS

4. DRAM HYBRID MODULE

ORGANIZATION	1M×8	1M×9
TOSHIBA	THM81000S/L	THM91000S/L
HITACHI	HB56A18	HB56A19
MITSUBISHI		MH1M09J

5. 16K Bit Static RAM
1) NMOS

Organization	2K×8			4K×4
Package Width	0.6 inch	0.3 inch		
TOSHIBA	TMM2016BP	TMM2015BP	TMM2018AD/AP	TMM2068AD/AP
Fujitsu	MB8128			MB8168
Hitachi	HM6116	HM6116AS		HM6168
Inmos				IMS1420/1421
Mitsubishi	M58725			M5M2168
Motorola	MCM6116		MCM2016H/18	MCM6168
NEC	μPD4016	μPD4016CX		
Oki	MSM2128			
AMD		AM9128	AM9128	AM2168

2) CMOS

Organization	2K×8	
TOSHIBA	TC5517CP/CF	TC5518CP/CF
Fujitsu	MB8416	MB8417/8418
Hitachi	HM6116	HM6117
NEC	μPD446	μPD449
Oki	MSM5128	MSM5129
Mitsubishi	M5M5117	M5M5116/5118
Sharp	LH5117	LH5118

6. 64K/72K Bit Static RAM

Organization	8K×8						8K×9	64K×1
NMOS/CMOS	NMOS	CMOS			NMOS			CMOS
Package Width	0.3 inch	0.6 inch			0.3 inch			0.3 inch
TOSHIBA	TMM2063P	TMM2064P	TC5564AP/AF	TC5565APL/AFL	TC5563AP	TMM2088P	TMM2089C	TC5562P
Fujitsu		MB8464		MB8464		MB81C78	MB81C79	HB81C71A
Hitachi	HM6264AS	HM6264		HM6264	HM6264ASP			HM6287
Mitsubishi			M5M5164	M5M5165		M5M5178	M5M5179	M5M5187
NEC			μPD4464	μPD4364				μPD4361
Oki		MSM5165	MSM5164	MSM5165				
Inmos								IMS1600/1
Motorola						MCM6164		MCM6287
IDT				IDT7164				IDT7187

7. 256K Bit Static RAM/Pseudo Static RAM

Organization	32K×8	
TYPE	SRAM	PSRAM
NMOS/CMOS	CMOS	CMOS
Package Width	0.6 inch	0.6 inch
TOSHIBA	TC55257	TC51832P/PL
Fujitsu	HB84256	
Hitachi	HM62256	HM65256
Mitsubishi	M5M5256	
NEC	μPD43256	μPD42832
Sony	CXK58256	
SMOS	SRM20256	
Sharp	LH52256	LH62258

8. 64K/128K Bit NMOS EPROM/OTP

Organization	8K×8		16K×8	
EPROM/OTP	EPROM	OTP	EPROM	OTP
Pins	28	28	28	28
TOSHIBA	TMM2764AD	TMM2464AP/AF	TMM27128AD	TMM24128AP/AF
AMD	Am2764A		Am27128A	
Fujitsu	MBM2764		MBM27128A	
Hitachi	HN482764	HN482764	HM4827128G	HN4827128
Intel	i2764A	P2764A	i27128A	P27128A
Mitsubishi	M5L2764K	M5M2764P	M5L27128K	M5M27128P
Mostek				
Motorola	—			
NEC	μPD2764	μPD2764C	μPD27128	μPD27128C
Oki	MSM2764		MSM27218	
TI	TMS2764			

9. 256K/512K/1MBIT EPROM/OTP

Organization	32K×8				64K×8		128K×8	
EPROM/OTP	EPROM		OTP		EPROM	OTP	EPROM	
	NMOS	CMOS	NMOS	CMOS	NMOS		CMOS	
TOSHIBA	TMM27256AD	TC57256D TC57256AD	TMM24256AP/AF	TC54256AP/AF	TMM27512D	TMM24512P/F	TC571000D	TC571001D
AMD	Am27256	AM27C256			Am27512			
Fujitsu	MBM27256	MBM27C256			—	—	MBM27C1000	MBM27C1001
Hitachi	HN27256G	HN27C256G	HN4827256P		HN27512G		HN27C101	HN27C301
Intel	i27256	i27C256	P27256A	P27C256	i27512	P27512	27010	—
Mitsubishi	M5L27256K	M5M27C256	M5M27256P	M5M27C256P	M5L27512		M5M27C100	M5M27C101
NEC	μPD27256	μPD27C256A	μPD27256C	μPD27256C		—	μPD27C100	μPD27C101
Oki	MSM27256	MSM27C256			MSM27512		MSM271000	
NSC	—	NMC27C256	—		NMC27C512		NMC27C1023	
TI	—	TMS27C256			TMS27C512			

10. 256K/1MBIT/2MBIT/4MBIT MROM

Organization	32K×8	128K×8	256K×8	512K×8
	CMOS	CMOS		
TOSHIBA	TC53257P/F	TC531000AP/AF	TC532000P	TC534000P
TI	TMS47C256	TMS47C1024		
Fujitsu	MB83256	MB831124	MB832000	
Hitachi	HN613256P	HN62301	HN62302	
Motorola	MCM65256A			
Mitsubishi	—	M5M23C100	—	M5M23C400
NEC	μPD23C256	μPD23C1000	μPD23C2000	
Oki	MSM53256	MSM531000		
RCA	CDM53256			

MEMORY SELECTION GUIDE (1) — ACCESS TIME VS. CAPACITY.

*Preliminary

	16K Bit	64K Bit	72K Bit	128K Bit	256K Bit	512K Bit	1M Bit	2M Bit	4M Bit
250					TC57256-25	TMM27512-25 TMM27512-250 TMM24512	TC571000/1-25		TC534000
200	TC5517C-20 TC5518C-20	TMM2764A-20 TMM2764A-200 TMM2464A		TMM27128A-20 TM27128A-200 TMM24128A	TC57256A-20 TMM27256A-20 TMM27256A-200 TC57256-20 TMM24256A TC54256A TC53257	TMM27512-20 TMM27512-200	TC571000/1-20	TC532000	
150	TMM2015B-12/15 TMM2016B-12/15 TC5517C-15 TC5518C-15	TMM2063-12/15 TMM2064-12/15 TC5563A-12/15 TC5564A-12/15 TC5565A-12/15 TMM2764A-15 TMM2764A-150		TMM27128A-15 TMM27128A-150	TMM41256-12/15 TMM41257-12/15 TMM41464-12/15 TMM41256A-12/15 TMM41257A-12/15 TC55257-12 TC55257A-12 TC51832-12 TMM27256A-15 TMM27256A-150		TC511000-12 TC511001-12 TC511002-12 TC514256-12 TC514258-12 TC531000A		
100	TMM2015B-90/10 TMM2016B-90/10	TMM2063-10 TMM2064-10 TMM2064-70 TC5563A-10 TC5565A-10 TC5561-55/70			TMM41256A-10 TMM41257A-10 TC55257-85/10 TC55257A-85/10 TC51832-85/10		TC511000-85/10 TC511001-85/10 TC511002-85/10 TC514256-85/10 TC514258-85/10		
55	TMM2018A-25/35/45 TMM2068A-25/35/45 TMM2078A-25/35/45	TMM2088-35/45/55 TC5562-45/55 TC55416-35/45/55 TC55417-35/45/55	TMM2089-35/45/55						

MEMORY SELECTION GUIDE (2) — TYPE OF MEMORY VS. CAPACITY

*Preliminary

Memory	Type	Memory Capacity								
		16K Bit	64K Bit	72K Bit	128K Bit	256K Bit	512K Bit	1M Bit	2M Bit	4M Bit
RAM	NMOS Dynamic RAM					TMM41256P/T TMM41257P/T TMM41464P TMM41256AP/AT/AZ TMM41257AP/AT/AZ				
	CMOS Dynamic RAM							TC511000P/JZ TC511001P/JZ TC511002P/JZ TC514256P/JZ TC514258P/JZ		
	NMOS Static RAM	TMM2015BP TMM2016BP TMM2018AD/AP TMM2068AD/AP TMM2078AD	TMM2063P TMM2064P TMM2088P	TMM2089C/P						
	CMOS Static RAM	TC5517CP/CF TC5518CP/CF	TC5564APL/FL TC5563APL TC5565APL/AFL TC5561P TC5562P TC55416P TC55417P			TC55257P TC55257AP/AF TC51832P/PL				
ROM	NMOS EPROM		TMM2764AD/ADI		TMM27128AD/ADI	TMM27256AD/ADI	TMM27512D/DI			
	CMOS EPROM					TC57256D/AD		TC571000/ID		
	CMOS Mask ROM					TC53257P/F		TC531000AP/AF	TC532000P	TC534000P
	NMOS OTP		TMM2464AP/AF		TMM24128AP/AF	TMM24256AP/AF	TMM24512P/F			
	CMOS OTP					TC54256AP/AF				

MEMORY SELECTION GUIDE (3) — WORD BY BIT

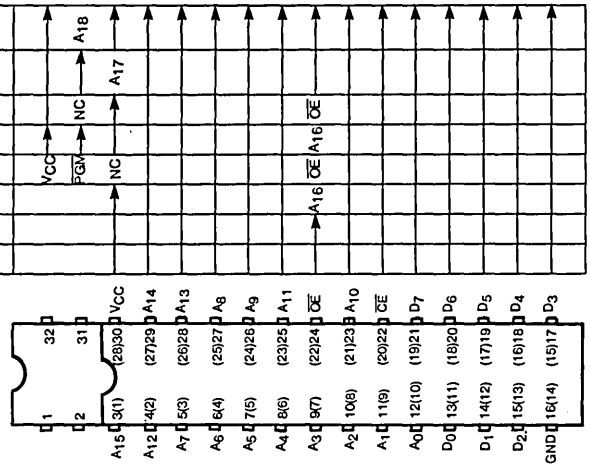
Word \ Bit	1	4	8	9
2K			TMM2015BP TMM2016BP TMM2018AD TMM2018AP TC5517CP/CF TC5518CP/CF	
4K		TMM2068AD/AP TMM2078AD		
8K			TMM2063P TMM2064P TC5564APL/AFL TC5563APL TC5565APL/AFL TMM2088P TMM2464AP/AF TMM2764AD/ADI	TMM2089C/P
16K		TC55416P TC55417P	TMM24128AP/AF TMM27128AD/ADI	
32K			TC55257P TC55257AP/AF TC51832P/PL TC54256AP/AF TMM24256AP/AF TMM27256AD/ADI TC53257P/F T57256D/AD	
64K	TC5561P TC5562P	TMM41464P	TMM24512P/F TMM27512D/DI	
128K			TC531000AP/AF TC571000/ID	
256K	TMM41256P/T TMM41257P/T TMM41256AP/AT/AZ TMM41257AP/AT/AZ	TC514256P/J/Z TC514258P/J/Z	TC532000P	
512K			TC534000P	
1M	TC511000P/J/Z TC511001P/J/Z TC511002P/J/Z		THM81000S/L	THM91000S/L

MEMORY SELECTION GUIDE (4) — HIGH DENSITY PACKAGE

PACKAGE		PLCC	SOJ	ZIP		SIP/SIMM	SOG	
PIN		18	26/20	16	20/19	30	24	28
Dynamic RAM	256K	TMM41256T TMM41257T TMM41256AT TMM41257AT		TMM41256AZ TMM41257AZ				
	1M		TC511000J TC511001J TC511002J TC514256J TC514258J		TC511000Z TC511001Z TC511002Z TC514256Z TC514258Z			
	8M/9M					THM81000S/L THM91000S/L		
Static RAM	16K						TC5517CF TC5518CF	
	64K							TC5564AFL TC5565AFL
	256K							TC55257AF
Mask ROM	256K							TC53257F
	1M							TC531000AF
OTP	64K							TMM2464AF
	128K							TMM24128AF
	256K							TMM24256AF TC54256AF
	512K							TMM24512F

TOSHIBA BYTE-WIDE MEMORY PIN OUT FOR 28/32 PIN DEVICES

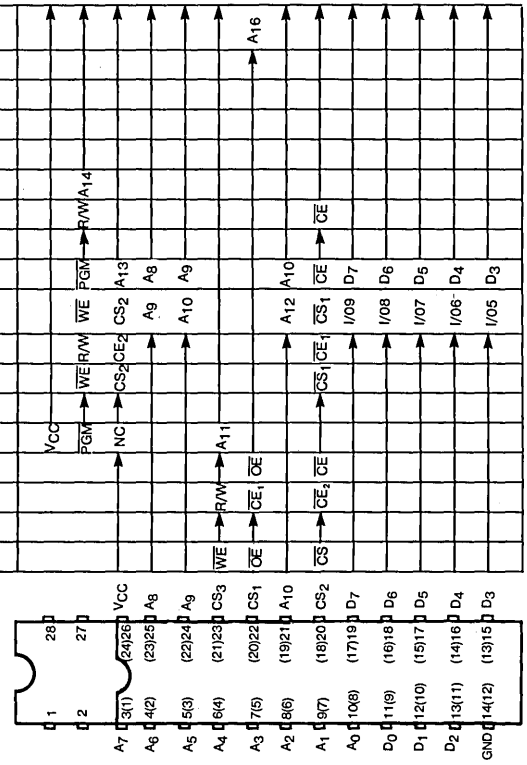
4M BIT	MROM	TC534000
2M BIT	MROM	TC532000
1M BIT	MROM	TC531001
	EPROM	TC571001
		TC571000
	MROM	TC531000
512K BIT	OTP	TMM24512
	EPROM	TMM27512



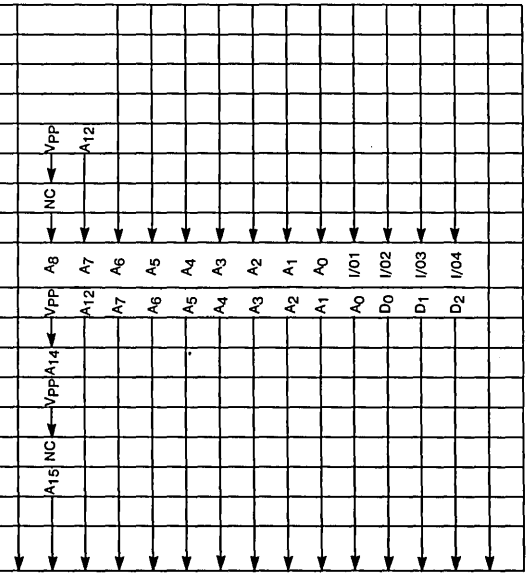
512K BIT	EPROM	TMM27512
	OTP	TMM24512
1M BIT	MROM	TC531000
	EPROM	TC571000
		TC571001
	MROM	TC531001
2M BIT	MROM	TC532000
4M BIT	MROM	TC534000

TOSHIBA BYTE-WIDE MEMORY PIN OUT FOR 24/28 PIN DEVICES

1M BIT	MROM	TC531000
512K BIT	OTP	TMM27512
	EPROM	TMM24512
256K BIT	MROM	TC53257
	OTP	TC54256/TMM24256
	EPROM	TC57256/TMM27256
	CRAM	TC55257
128K BIT	OTP	TMM24128A
	ERPOM	TMM27128A
72K BIT	H.S. SRAM	TMM2089
64K BIT	CRAM	TC5564/65
	SRAM	TMM2063/64/88
	OTP	TMM2464A
	EPROM	TMM2764A
16K BIT	CRAM	TC5517
		TC5516/18
	H.S. SRAM	TMM2018
	SRAM	TMM2015/16



16K BIT	SRAM	TMM2015/16
	H.S. SRAM	TMM2018
	CRAM	TC5516/18
		TC5517
64K BIT	EPROM	TMM2764A
	OTP	TMM2464A
	SRAM	TMM2063/64/88
	CRAM	TC5564/65
72K BIT	H.S. SRAM	TMM2089C
128K BIT	EPROM	TMM27128A
	OTP	TMM24128A
256K BIT	CRAM	TC55257
	EPROM	TC57256/TMM27256
	OTP	TC54256/TMM24256
	MROM	TC53257
512K BIT	EPROM	TMM27512
	OTP	TMM24512
1M BIT	MROM	TC531000



Dynamic RAMs

TOSHIBA MOS MEMORY PRODUCT

262,144 WORD × 1 BIT DYNAMIC RAM
N-CHANNEL SILICON GATE MOS

TMM41256P/T-12
TMM41256P/T-15

DESCRIPTION

The TMM41256P/T is the new generation dynamic RAM organized 262,144 words by 1 bit, it is successor to the industry standard TMM4164AP.

The TMM41256P/T utilizes TOSHIBA's N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM-41256P/T to be packaged in a standard 16 pin plastic DIP and 18 pin plastic leaded chip carrier. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

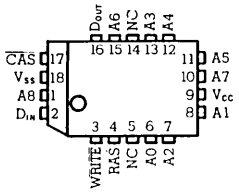
- 262,144 words by 1 bit organization
- Fast access time and cycle time

DEVICE	t_{RAC}	t_{CAC}	t_{RC}
TMM41256P/T-12	120 ns	60 ns	220 ns
TMM41256P/T-15	150 ns	75 ns	260 ns

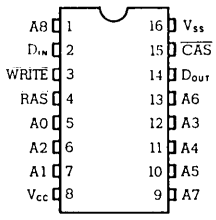
- Single power supply of 5V ±10% with a built-in V_{BB} generator
- Low Power:
  330mW Operating (MAX.) (TMM41256P/T-12)
  275mW Operating (MAX.) (TMM41256P/T-15)
  28mW Stand by (MAX.)
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh, and Page Mode capability.
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  Plastic DIP : TMM41256P
  Plastic Leaded Chip Carrier : TMM41256T

PIN CONNECTION (TOP VIEW)

• Plastic LCC



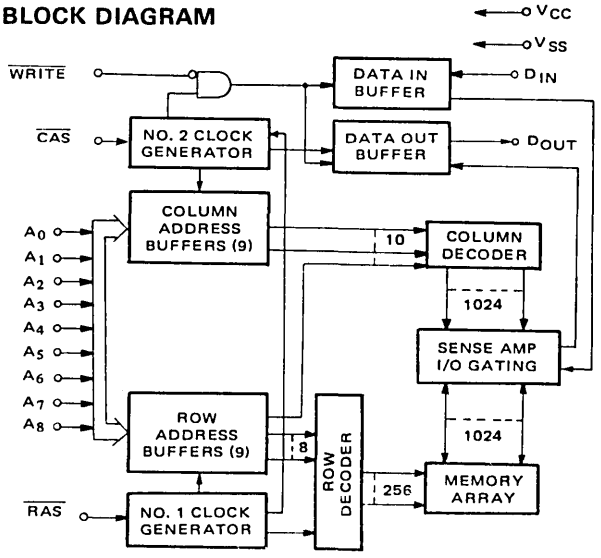
• Plastic DIP



PIN NAMES

$A_0 \sim A_8$	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM MATIGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITDONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TMM41256P T-12	–	60	mA	3, 4
		TMM41256P T-15	–	50		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	5	mA	
I_{CC3}	REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN.)	TMM41256P T-12	–	45	mA	3
		TMM41256P T-15	–	40		
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling : t_{PC} = t_{PC} MIN.)	TMM41256P T-12	–	45	mA	3, 4
		TMM41256P T-15	–	40		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = OV)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV ≦ V_{OUT} ≦ +5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRIAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70 C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41256P-12		TMM41256P-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	220	—	260	—	ns	
t_{RWC}	Read-Write Cycle Time	240	—	285	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	260	—	310	—	ns	
t_{PC}	Page Mode Cycle Time	120	—	145	—	ns	
t_{PRWC}	Page Mode Read-Write Cycle Time	140	—	170	—	ns	
t_{PRMW}	Page Mode Read-Modify-Write Cycle Time	160	—	195	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	120	—	150	ns	8,10
t_{CAC}	Access Time from $\overline{CAS}$	—	60	—	75	ns	9,10
t_{OFF}	Output Buffer Turn-Off Delay	0	35	0	40	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	6
t_{RP}	$\overline{RAS}$ Precharge Time	90	—	100	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	60	—	75	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120	—	150	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	25	—	25	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	50	—	60	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	25	—	30	—	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	95	—	120	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	—	0	—	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	15	—	20	—	ns	12
t_{WCH}	Write Command Hold Time	35	—	45	—	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	95	—	120	—	ns	
t_{WP}	Write Command Pulse Width	35	—	45	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35	—	45	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35	—	45	—	ns	
t_{DS}	Data-In Set-Up Time	0	—	0	—	ns	14
t_{DH}	Data-In Hold Time	35	—	45	—	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	95	—	120	—	ns	
t_{REF}	Refresh Period	—	4	—	4	ms	
t_{WCS}	Write Command Set-Up Time	−10	—	−10	—	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	40	—	50	—	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	100	—	125	—	ns	15

CAPACITANCE

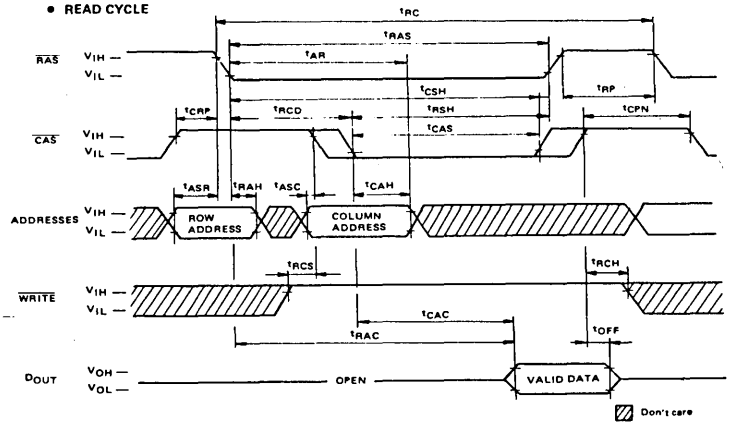
(V_{CC} = 5V ±10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance ($A_0 \sim A_8$, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	pF
C_O	Output Capacitance (D_{OUT})	–	7	pF

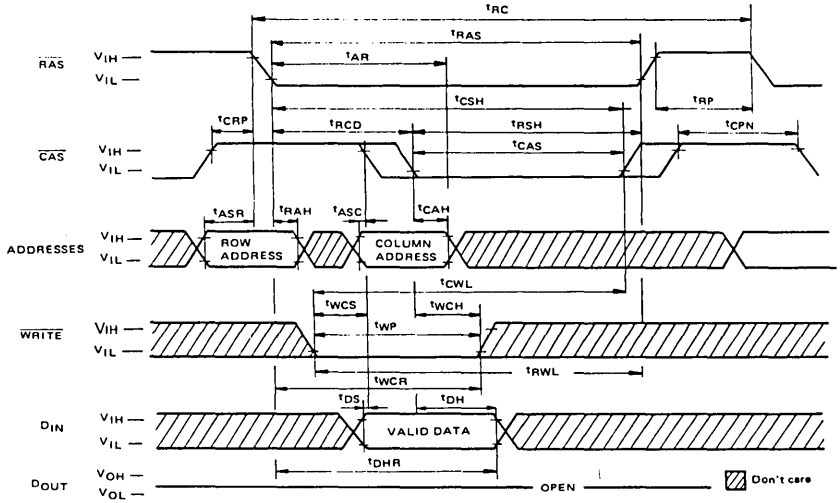
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5 ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.)
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

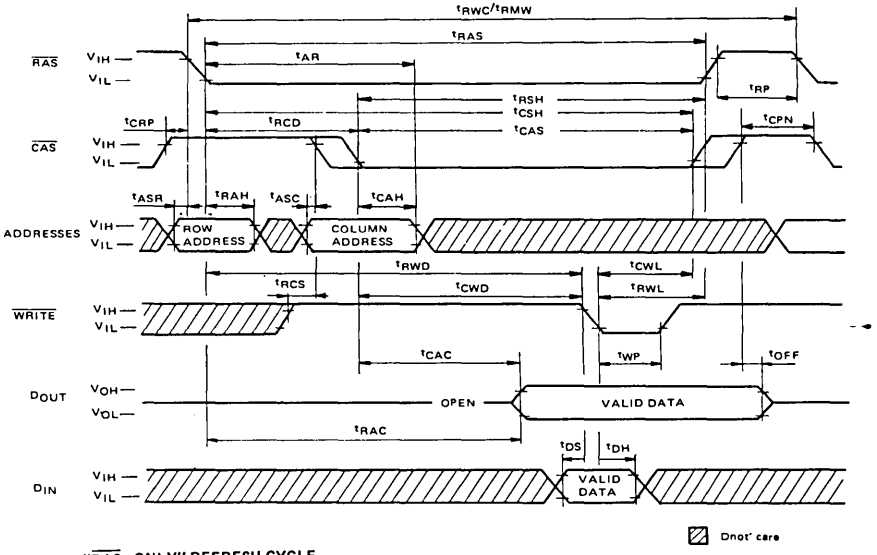
TIMING WAVEFORMS



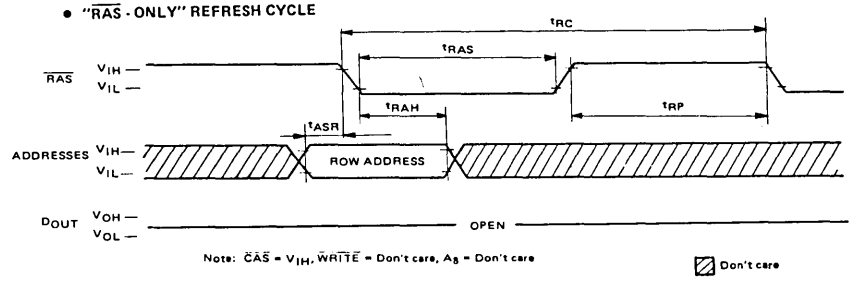
• WRITE CYCLE (EARLY WRITE)



•READ-WRITE/READ-MODIFY-WRITE CYCLE



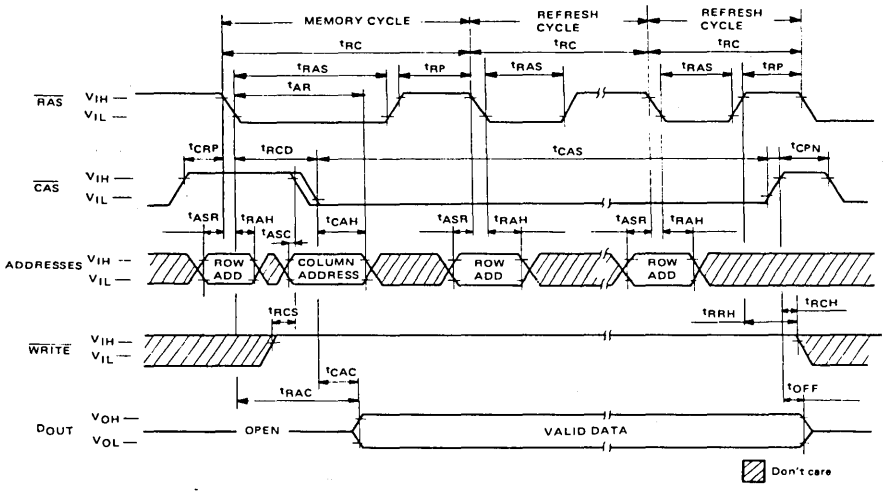
• "$\overline{RAS}$-ONLY" REFRESH CYCLE



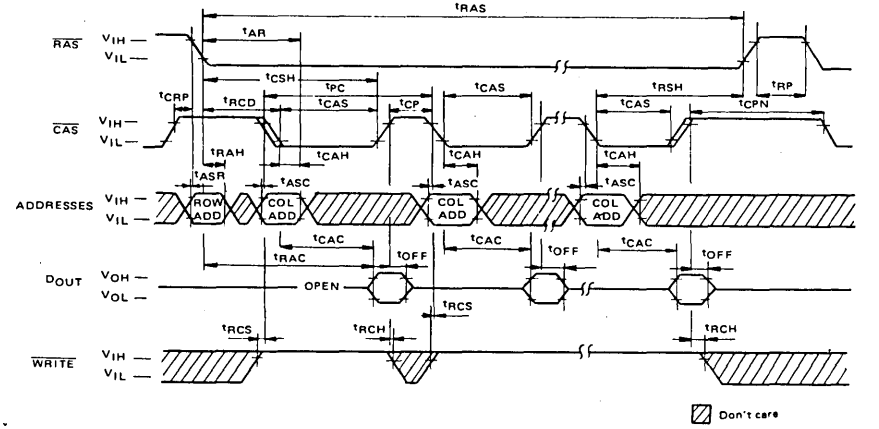
Note: $\overline{CAS}$ = V_{IH}, $\overline{WRITE}$ = Don't care, A_8 = Don't care

Don't care

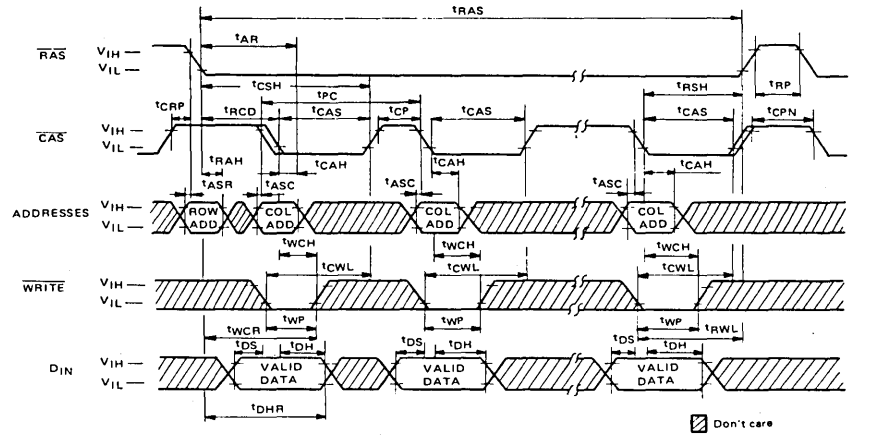
• HIDDEN REFRESH CYCLE



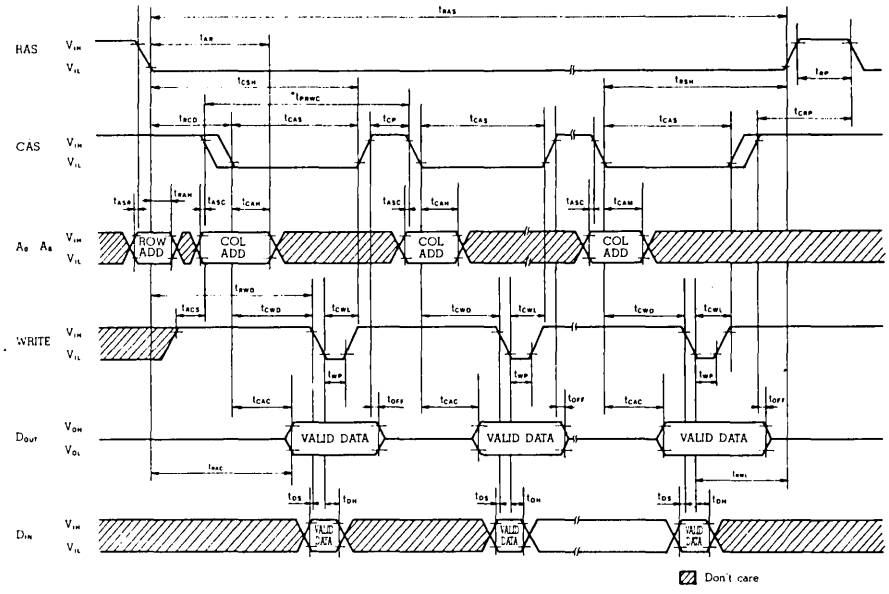
• PAGE MODE READ CYCLE



• PAGE MODE WRITE CYCLE



● PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256P/T are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41256P/T is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

PAGE MODE

The "Page-Mode" feature of the TMM41256P/T allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($A_0 \sim A_7$) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this funciton is most easily accomplished with "$\overline{RAS}$ - only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

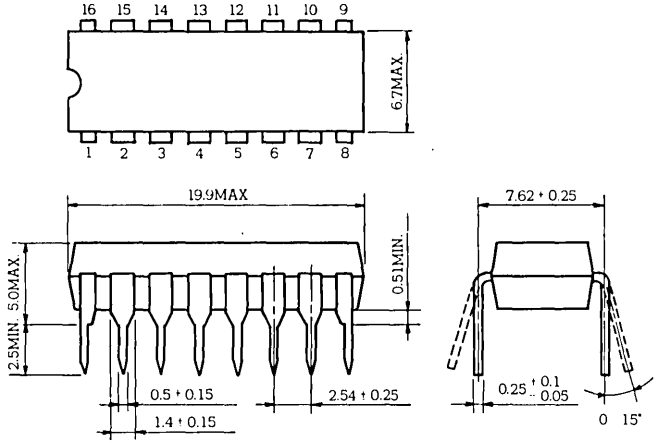
HIDDEN REFRESH

An optional feature of the TMM41256P/T is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$ - only" refresh cycle, but with $\overline{CAS}$ held low

OUTLINE DRAWINGS

● Plastic DIP

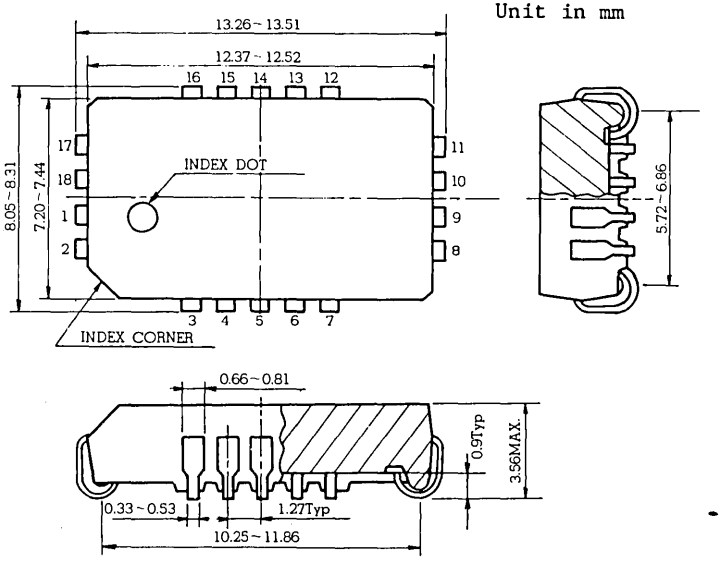
Unit in mm



Note : Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

● Plastic LCC

Unit in mm



Note : Each lead pitch is 1.27mm.

TOSHIBA MOS MEMORY PRODUCT

TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12
TMM41256AP/AT/AZ-15

DESCRIPTION

The TMM41256AP/AT/AZ is the N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41256AP/AT/AZ to be packaged in a standard 16 pin plastic DIP, 18 pin PLCC and 16 pin ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41256AP/AT/AZ high speed operation. Also, the advanced circuit techniques have realized low power dissipation. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as schottky TTL. In addition to the $\overline{RAS}$ only refresh mode, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is available. Another special feature of TMM41256AP/AT/AZ is page mode, allowing the user to access at a high data rate.

FEATURES

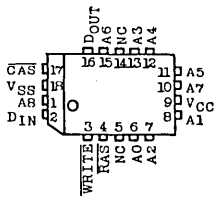
- 262,144 words by 1 bit organization
- Fast access time and cycle time

	TMM41256AP/AT/AZ-10/-12/-15
$\overline{RAS}$ Access Time	100ns/120ns/150ns
$\overline{CAS}$ Access Time	50ns/ 60ns/ 75ns
Cycle Time	190ns/220ns/260ns

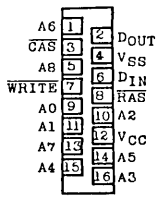
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power:
  - 440mW MAX. Operating (TMM41256AP/AT/AZ-10)
  - 385mW MAX. Operating (TMM41256AP/AT/AZ-12)
  - 330mW MAX. Operating (TMM41256AP/AT/AZ-15)
  - 28mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Page Mode capability
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  - Plastic DIP : TMM41256AP
  - Plastic Leaded Chip Carrier: TMM41256AT
  - Plastic ZIP : TMM41256AZ

PIN CONNECTION (TOP VIEW)

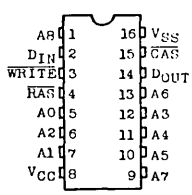
- Plastic LCC



- Plastic ZIP



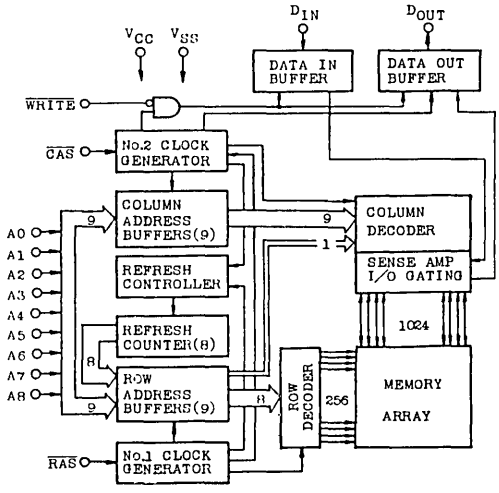
- Plastic DIP



PIN NAMES

A0 ∿ A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	
Operating Temperature	T_{OPR}	0 ∿ 70	°C	
Storage Temperature	T_{STG}	-55 ∿ 150	°C	
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	
Power Dissipation	P_D	600	mW	
Short Circuit Output Current	I_{OUT}	50	mA	

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	TMM41256AP/AT/AZ-10	-	80	mA	3,4
		TMM41256AP/AT/AZ-12	-	72	mA	
		TMM41256AP/AT/AZ-15	-	65	mA	
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		-	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$: $t_{RC}=t_{RC}$ MIN.)	TMM41256AP/AT/AZ-10	-	70	mA	3
		TMM41256AP/AT/AZ-12	-	62	mA	
		TMM41256AP/AT/AZ-15	-	55	mA	
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Cycling: $t_{PC}=t_{PC}$ MIN.)	TMM41256AP/AT/AZ-10	-	60	mA	3,4
		TMM41256AP/AT/AZ-12	-	55	mA	
		TMM41256AP/AT/AZ-15	-	50	mA	
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: $t_{RC}=t_{RC}$ MIN.)	TMM41256AP/AT/AZ-10	-	70	mA	3
		TMM41256AP/AT/AZ-12	-	62	mA	
		TMM41256AP/AT/AZ-15	-	55	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, ALL Other Pins Not Under Test = 0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ +5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM41256AP/AT/AZ-10		TMM41256AP/AT/AZ-12		TMM41256AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190	-	220	-	260	-	ns	
t_{RWC}	Read-Write Cycle Time	200	-	240	-	265	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	220	-	260	-	310	-	ns	
t_{PC}	Page Mode Cycle Time	100	-	120	-	145	-	ns	
t_{PRWC}	Page Mode Read-Write Cycle Time	110	-	140	-	170	-	ns	
t_{PRMW}	Page Mode Read-Modify Write Cycle Time	130	-	160	-	195	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	100	-	120	-	150	ns	8,10
t_{CAC}	Access Time from $\overline{CAS}$	-	50	-	60	-	75	ns	9,10
t_{OFF}	Output Buffer Turn-Off Delay	5	25	5	30	5	35	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80	-	90	-	100	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	50	-	60	-	75	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100	-	120	-	150	-	ns	
t_{CAS}	$\overline{CAS}$ Puls	50	10,000	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	50	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	20	-	25	-	ns	
t_{CP}	Page Mode $\overline{CAS}$ Precharge Time	40	-	50	-	60	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	25	-	30	-	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	70	-	85	-	105	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	-	0	-	0	-	ns	
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	10	-	15	-	20	-	ns	
t_{WCH}	Write Command Hold Time	20	-	25	-	30	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TMM41526AP/AT/AZ-10		TMM41526AP/AT/AZ-12		TMM41526AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	70	-	85	-	105	-	ns	
t_{WP}	Write Command Pulse Width	20	-	25	-	30	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	-	35	-	45	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	-	35	-	45	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	14
t_{DH}	Data-In Hold Time	20	-	25	-	30	-	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	70	-	85	-	105	-	ns	
t_{REF}	Refresh Period	-	4	-	4	-	4	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	30	-	40	-	50	-	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	80	-	100	-	125	-	ns	15
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	40	-	50	-	60	-	ns	

CAPACITANCE (T_{CC}=5V±10%, f=1MHz, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A_0 ~ A_8, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	
C_O	Output Capacitance (D_{OUT})	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS Before RAS initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurement assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Assumes that $t_{RCD} \leqq t_{RCD}$(max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

9. Assume that $t_{RCD} \geqq t_{RCD}$(max.)

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

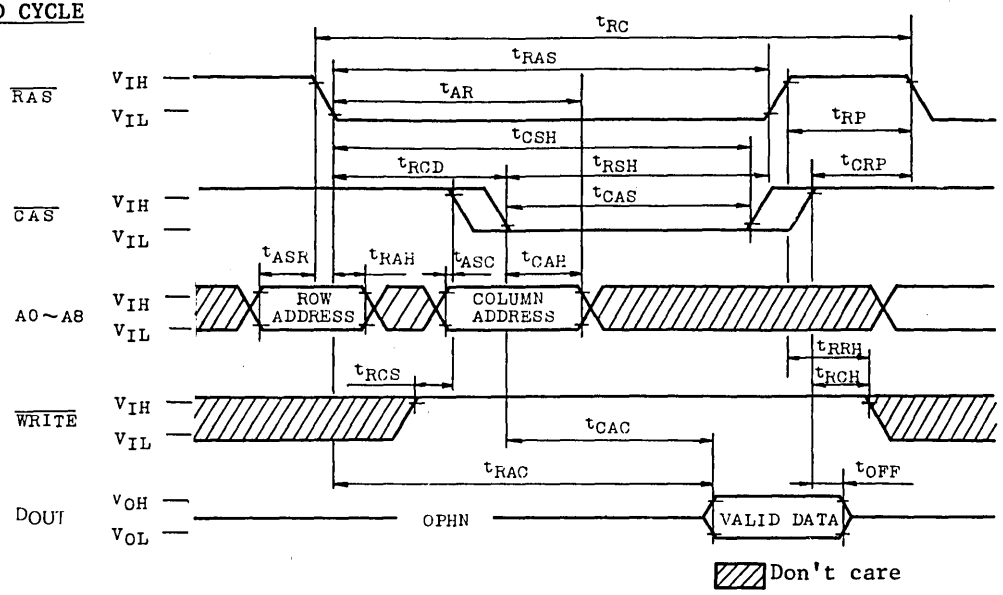
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled exclusively by t_{CAC}.

14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.

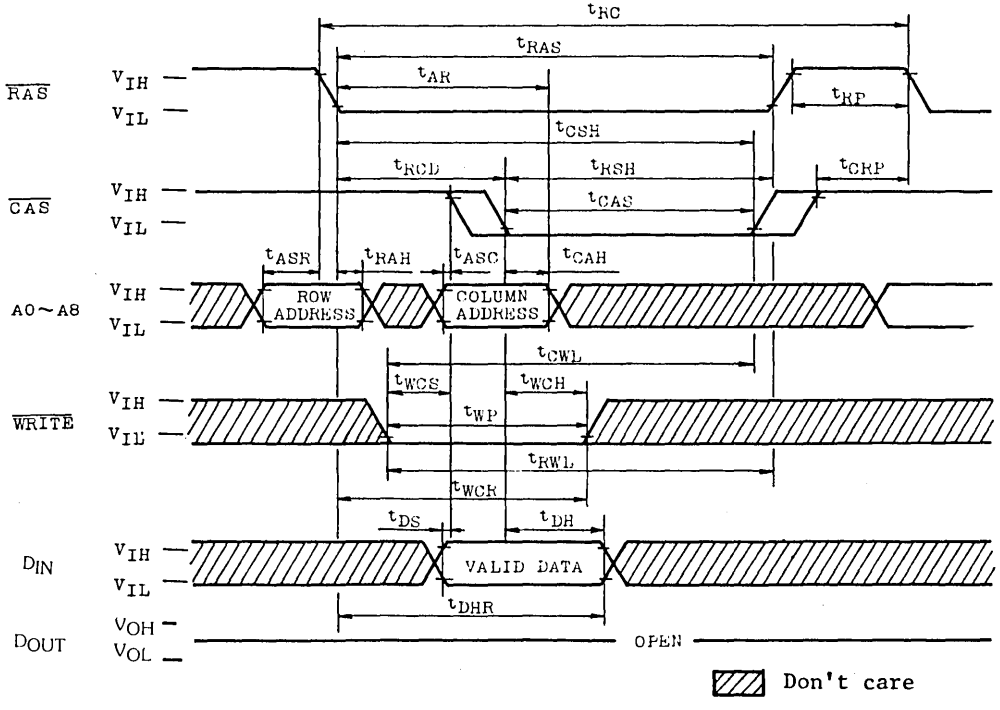
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$(min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

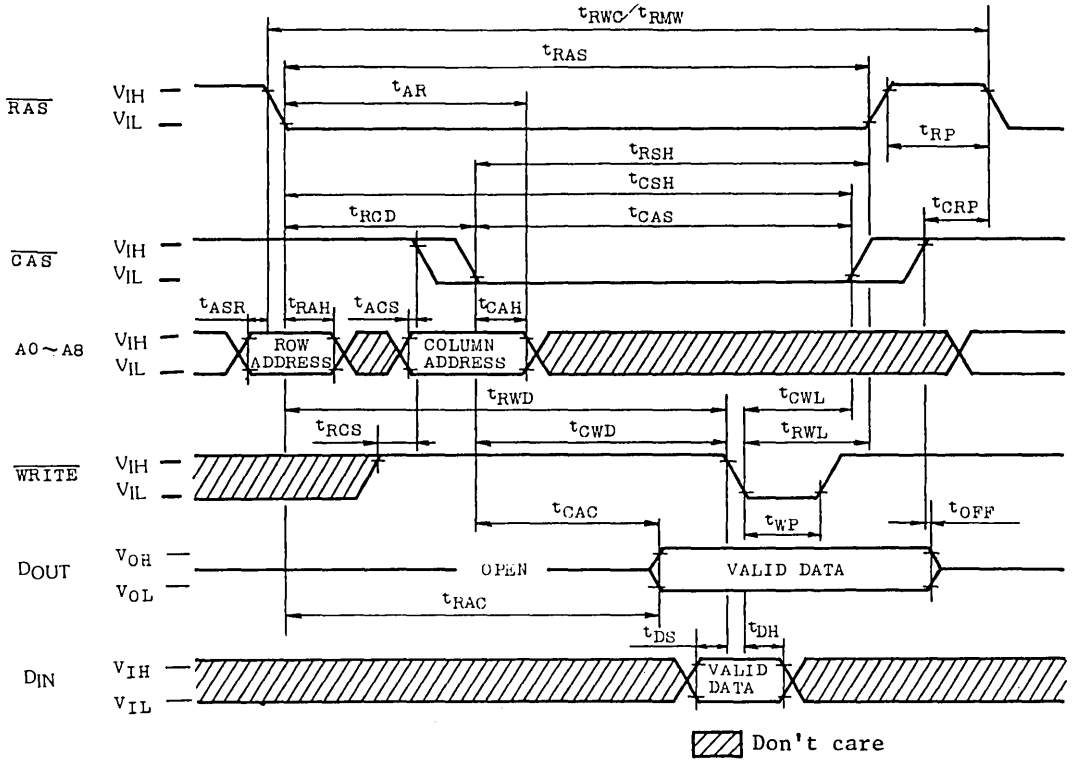
READ CYCLE



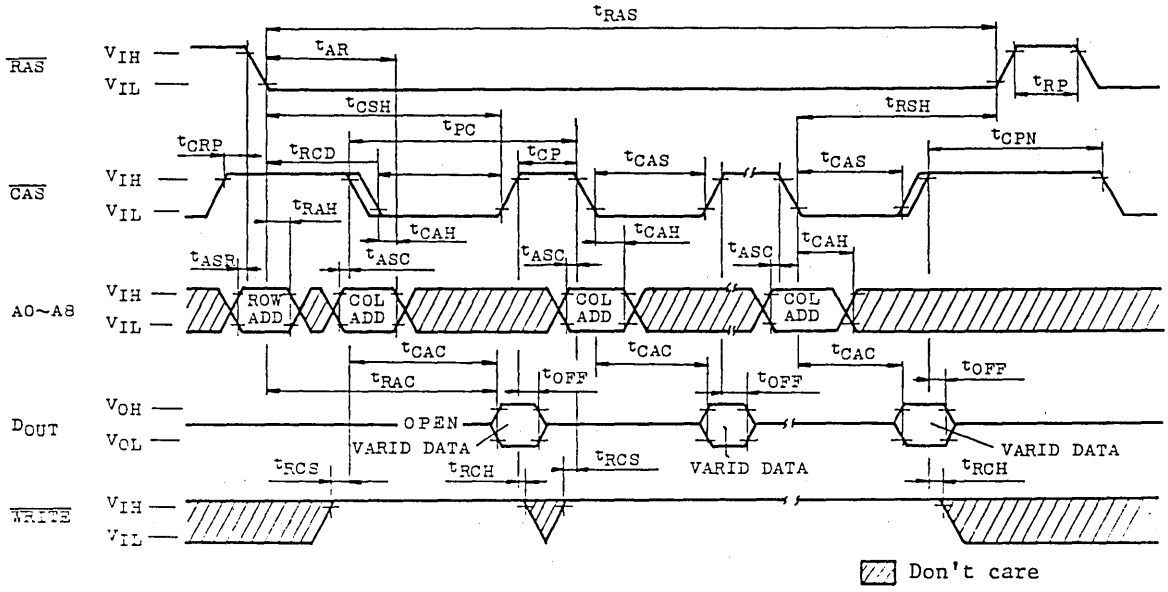
WRITE CYCLE (EARLY WRITE)



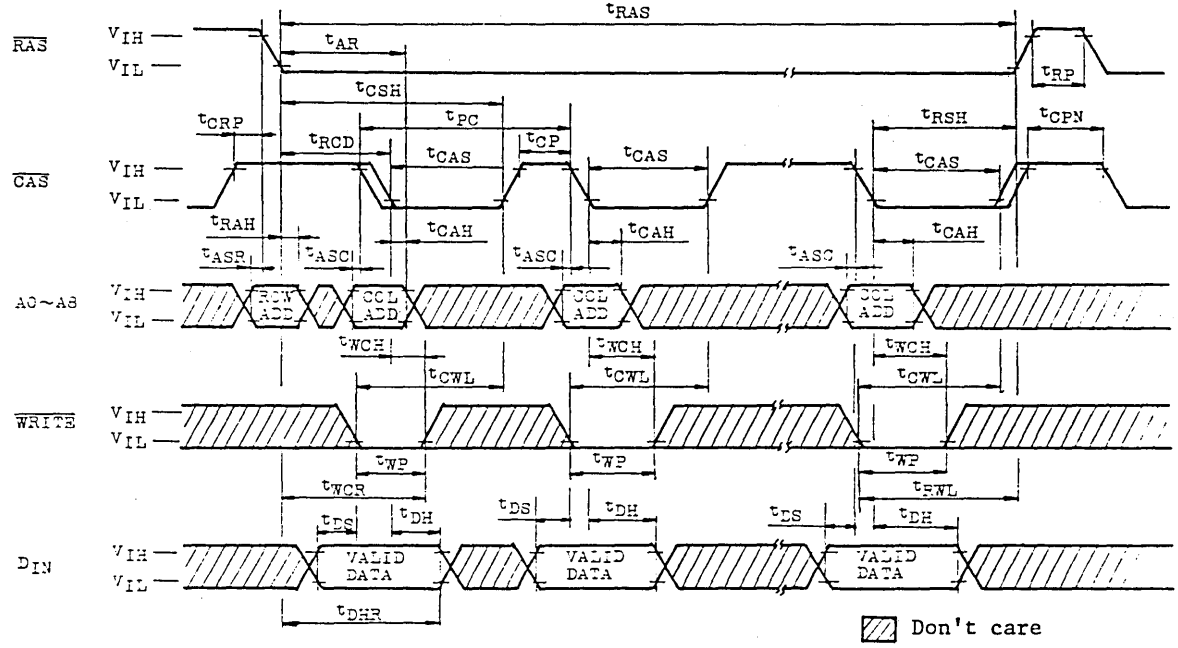
READ-WRITE/READ-MODIFY-WRITE CYCLE



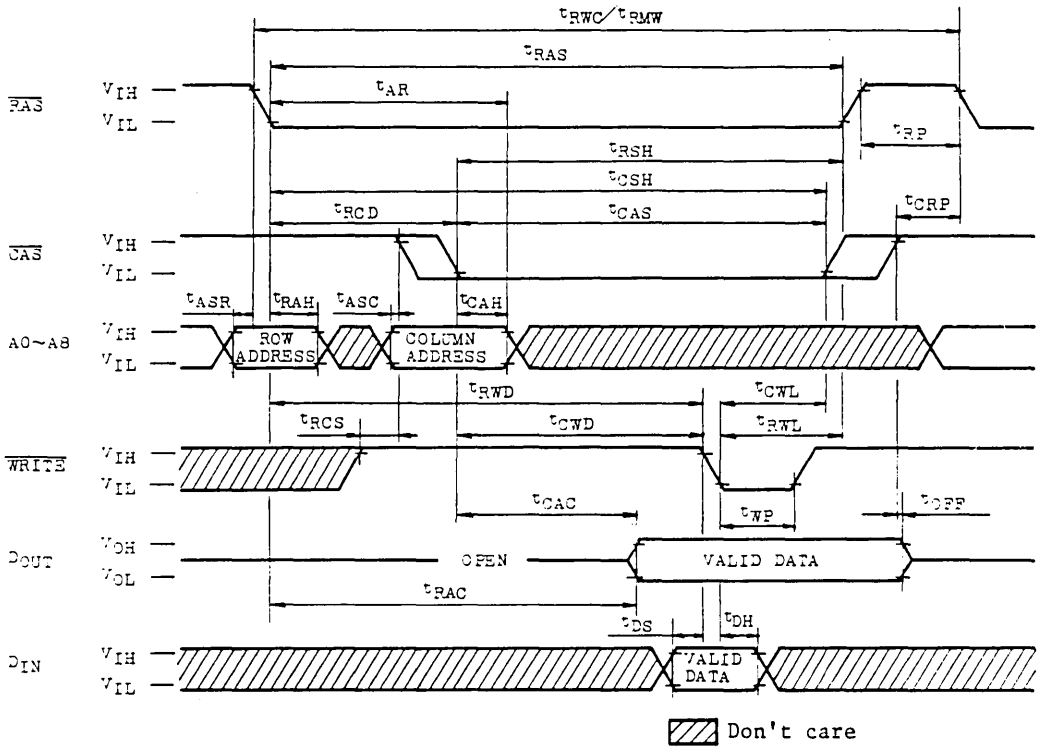
PAGE MODE READ CYCLE



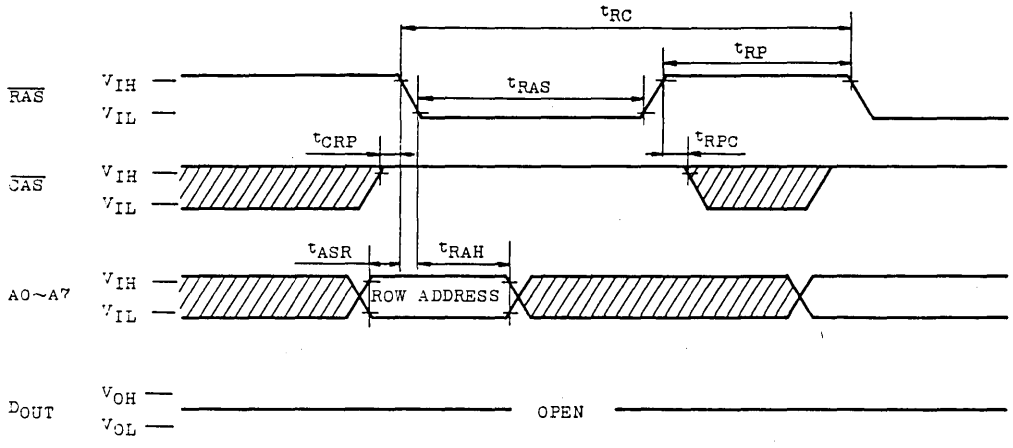
PAGE MODE WRITE CYCLE (EARLY WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE

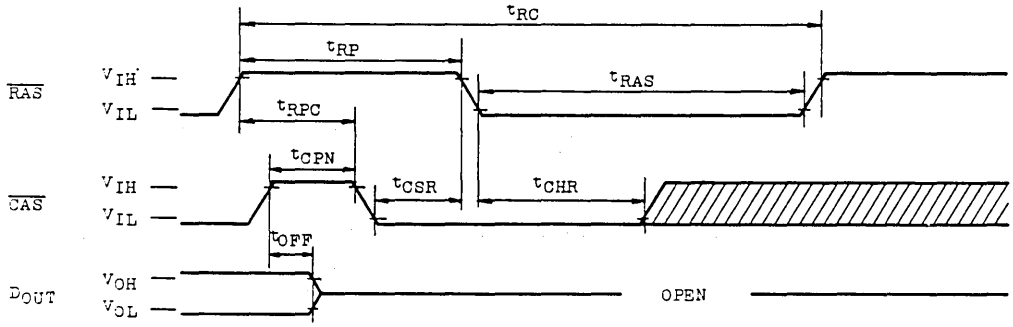


$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$=Don't care, A8=Don't care Don't care

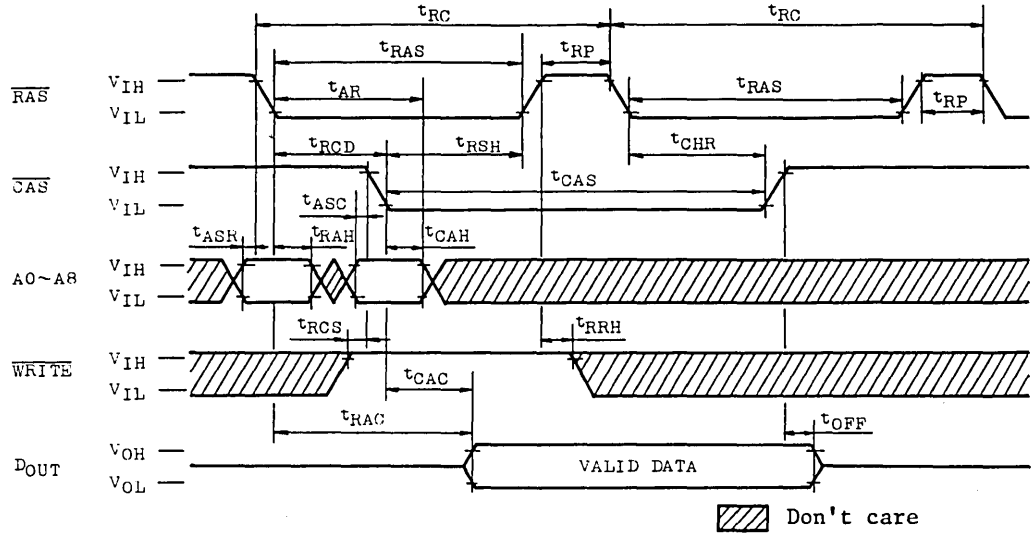
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



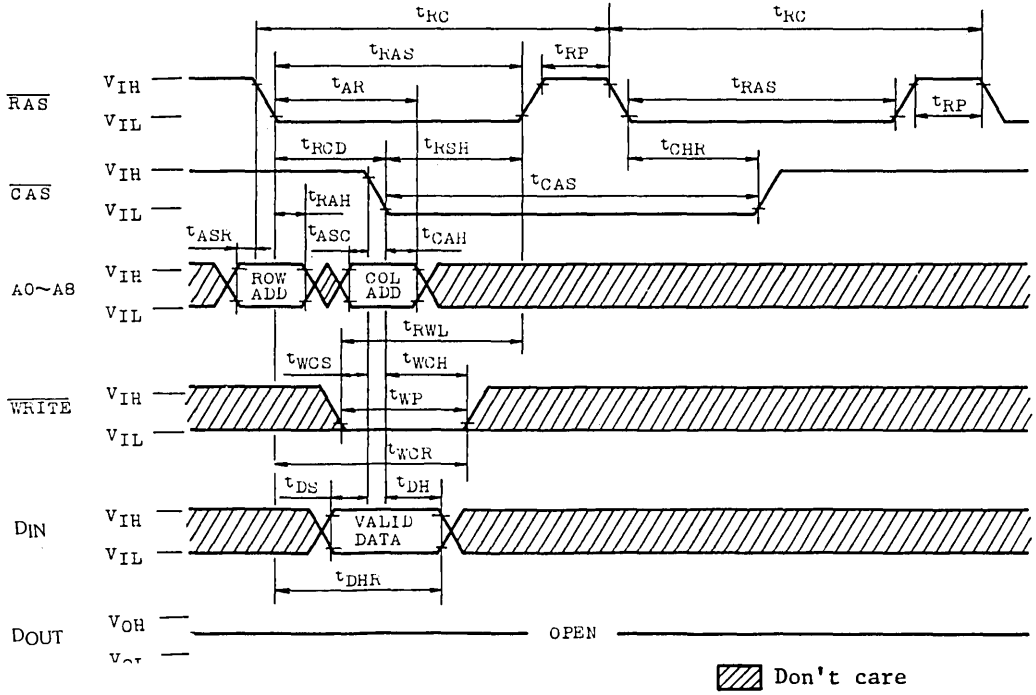
Note: $\overline{WRITE}$=Don't care, A0 ∿ A8=Don't care

Don't care

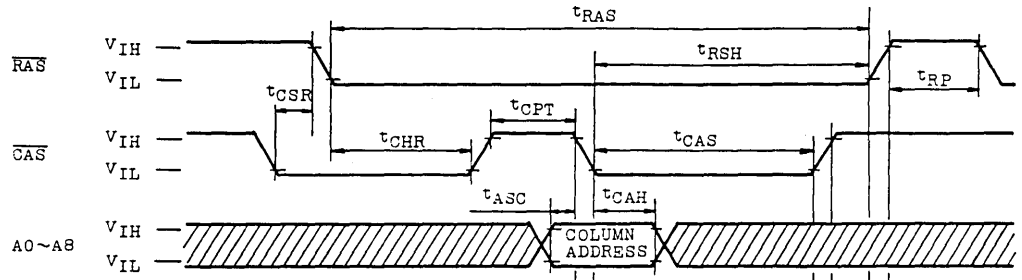
HIDDEN REFRESH CYCLE (READ)



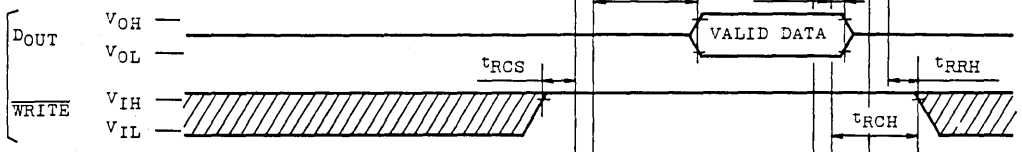
HIDDEN REFRESH CYCLE (WRITE)



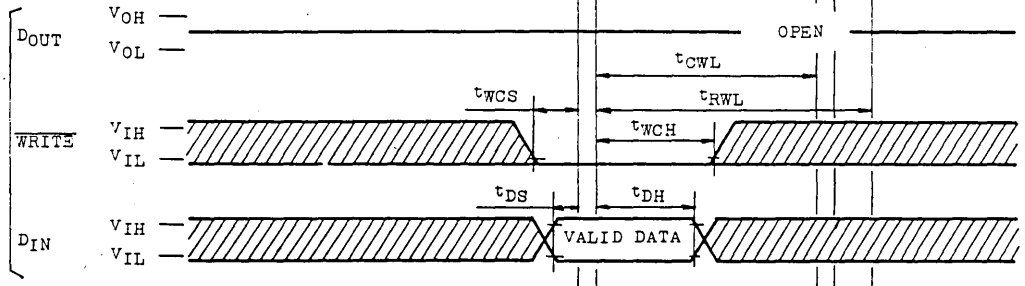
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



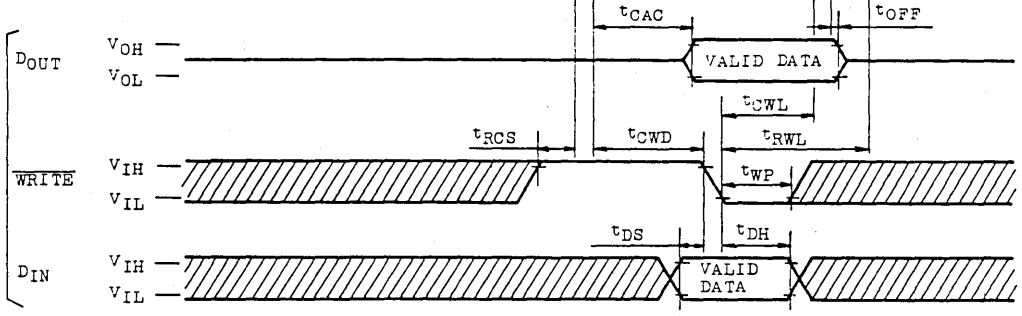
READ CYCLE



WRITE CYCLE



READ-WRITE/READ-MODIFY-WRITE CYCLE



Don't care

APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256AP/AT/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41256AP/AT/AZ is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid form access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

PAGE MODE

The "Page-Mode" feature of the TMM41256AP/AT/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

RAS ONLY REFRESH

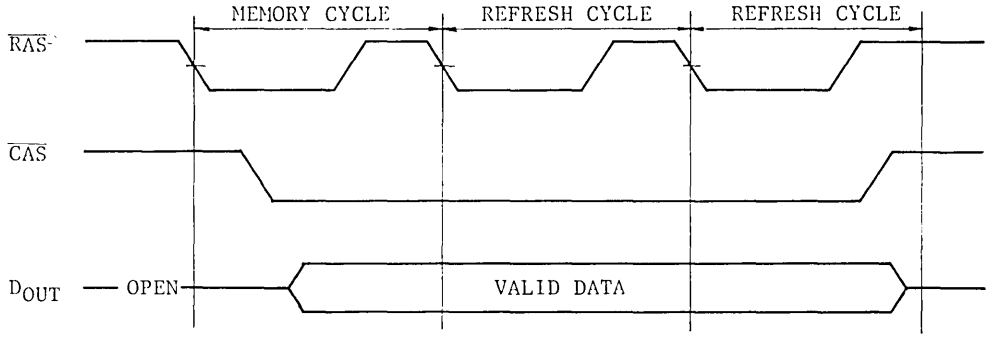
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A0 ∿ A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TMM41256AP/AT/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TMM41256AP/AT/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41256AP/AT/AZ can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST.
Repeat this operation 256 times.

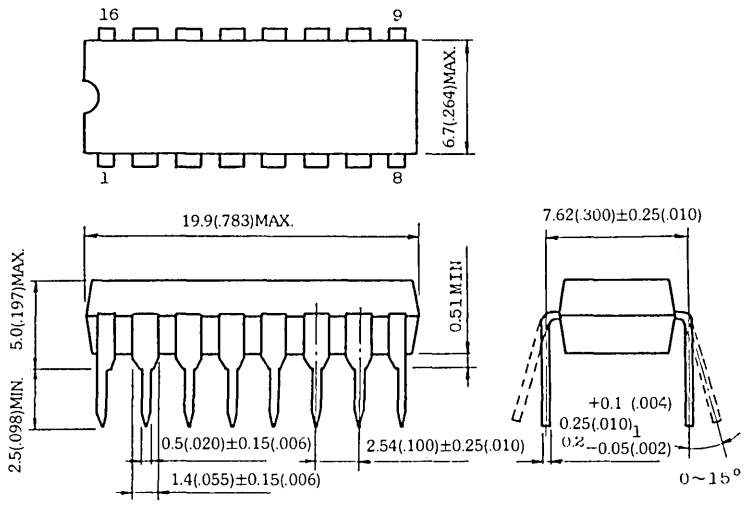
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS

• Plastic DIP

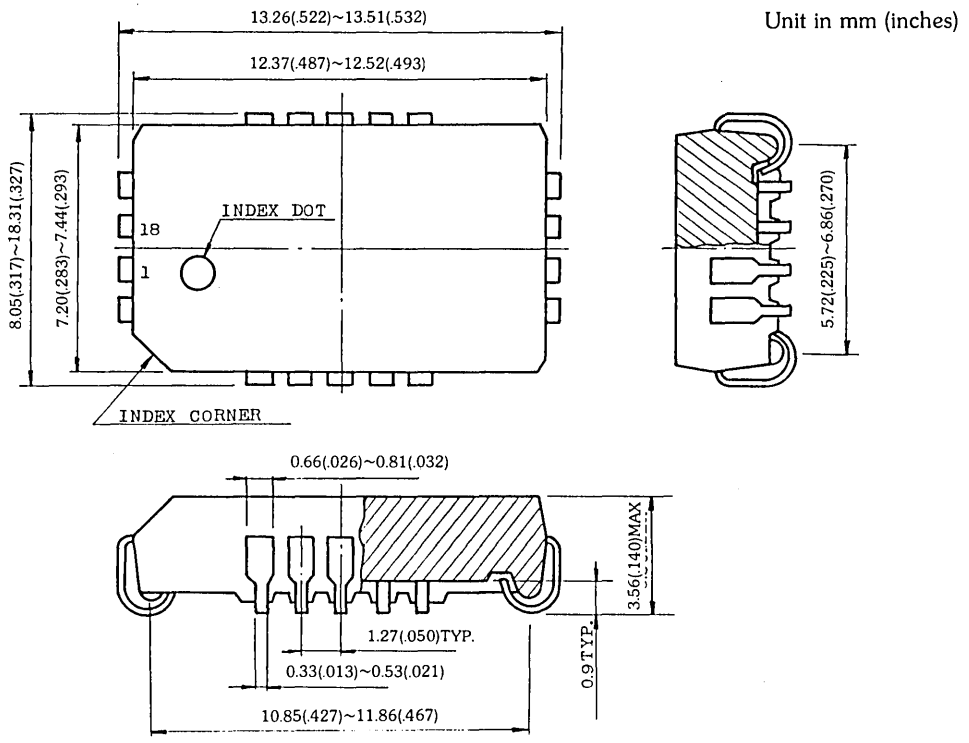
Unit in mm (inches)



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.16 leads. All dimensions are in millimeters.

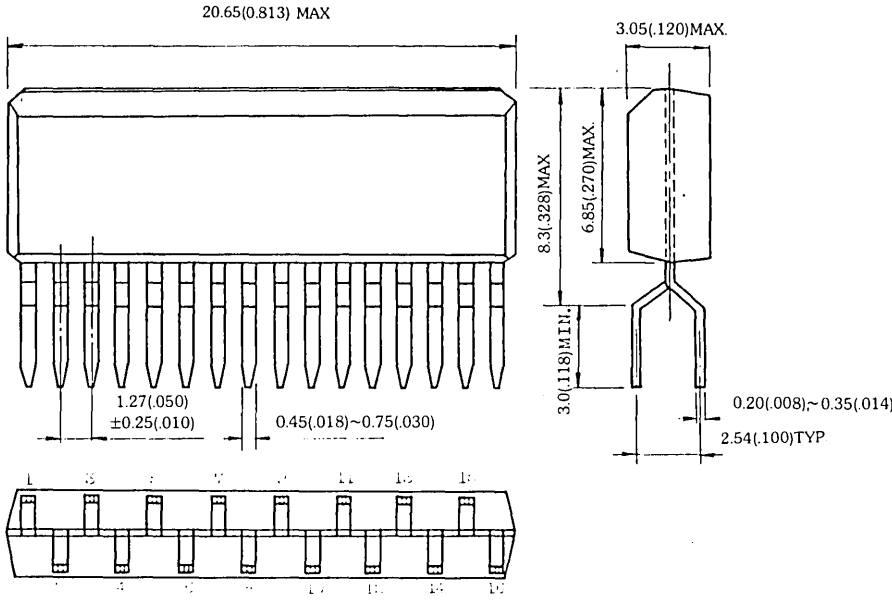
• Plastic LCC

Unit in mm (inches)



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

Unit in mm (inches)



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCT

262,144 WORD × 1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41257P/T-12
TMM41257P/T-15

DESCRIPTION

The TMM41257P/T is the N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41257P/T to be packaged in a standard 16 pin plastic DIP and 18 pin plastic leaded chip carrier. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41257P/T high speed operation. Also, the advanced circuit techniques have realized low power dissipation. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as schottky TTL. In addition to the $\overline{RAS}$ only refresh mode, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is available. Another special feature of TMM41257P/T is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

FEATURES

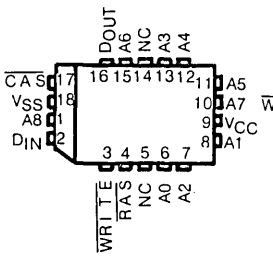
- 262,144 words by 1 bit organization
- Fast access time and cycle time

	TMM41257P/T-12	TMM41257P/T-15
$\overline{RAS}$ Access Time	120ns	150ns
$\overline{CAS}$ Access Time	60ns	75ns
Cycle Time	220ns	260ns
Nibble Mode Access Time	30ns	40ns
Nibble Mode Cycle Time	55ns	70ns

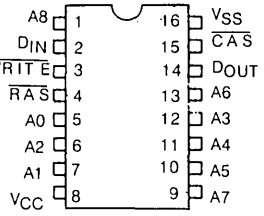
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power:
  385mW MAX. Operating (TMM41257P/T-12)
  330mW MAX. Operating (TMM41257P/T-15)
  28mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Nibble Mode capability
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  Plastic DIP :TMM41257P
  Plastic Leaded Chip Carrier :TMM41257T

PIN CONNECTION (TOP VIEW)

- Plastic LCC



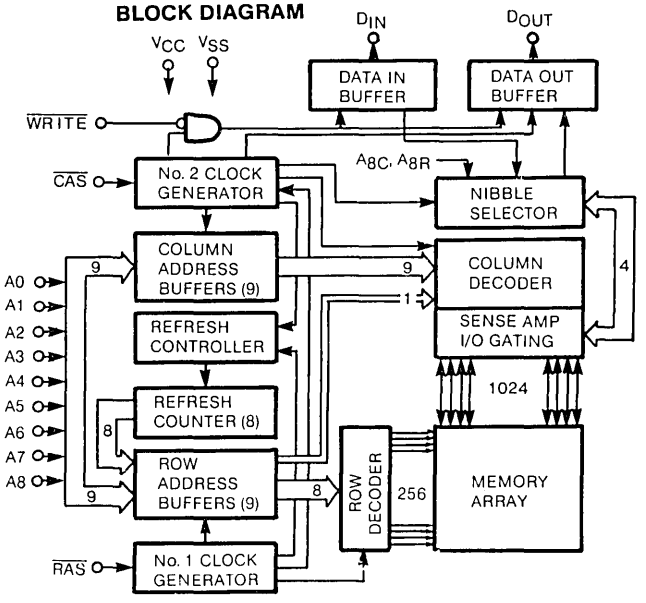
- Plastic DIP



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	−1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TMM41257P/T-12	-	70	mA	3,4
		TMM41257P/T-15	-	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TMM41257P/T-12	-	60	mA	3
		TMM41257P/T-15	-	50		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{NC}=t_{NC} MIN.)	TMM41257P/T-12	-	40	mA	3,4
		TMM41257P/T-15	-	30		
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: t_{RC}=t_{RC} MIN.)	TMM41257P/T-12	-	60	mA	3
		TMM41257P/T-15	-	50		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≦V_{IN}≦6.5V, All Other Pins Not Under Test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV≦V_{OUT}≦+5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=−5mA)		2.4		V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)			0.4	V	

ELECTRIAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41257P/T-12		TMM41257P/T-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	220	—	260	—	ns	
t_{RWC}	Read-Write Cycle Time	240	—	285	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	260	—	310	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	120	—	150	ns	8,10
t_{CAC}	Access Time from $\overline{CAS}$	—	60	—	75	ns	9,10
t_{OFF}	Output Buffer Turn-Off Delay	5	30	5	35	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	90	—	100	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	60	—	75	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120	—	150	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	20	—	25	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	25	—	30	—	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	85	—	105	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	—	0	—	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	15	—	20	—	ns	12
t_{WCH}	Write Command Hold Time	25	—	30	—	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	85	—	105	—	ns	
t_{WP}	Write Command Pulse Width	25	—	30	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35	—	45	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35	—	45	—	ns	
t_{DS}	Data-In Set-Up Time	0	—	0	—	ns	14
t_{DH}	Data-In Hold Time	25	—	30	—	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	85	—	105	—	ns	
t_{REF}	Refresh Period	—	4	—	4	ms	
t_{WCS}	Write Command Set-Up Time	0	—	0	—	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	40	—	50	—	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	100	—	125	—	ns	15
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	—	30	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	—	0	—	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	50	—	60	—	ns	
t_{NC}	Nibble Mode Cycle Time	55	—	70	—	ns	
t_{NRWC}	Nibble Mode Read-Write/ Read-Modify-Write Cycle Time	85	—	105	—	ns	
t_{NCAC}	Nibble Mode Access Time	—	30	—	40	ns	10
t_{NCAS}	Nibble Mode Pulse Width	30	—	40	—	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	15	—	20	—	ns	
t_{NRRSH}	Nibble Mode $\overline{RAS}$ Hold Time (Read)	25	—	30	—	ns	
t_{NWRSH}	Nibble Mode $\overline{RAS}$ Hold Time (Write)	45	—	50	—	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	30	—	40	—	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Read Time	25	—	30	—	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

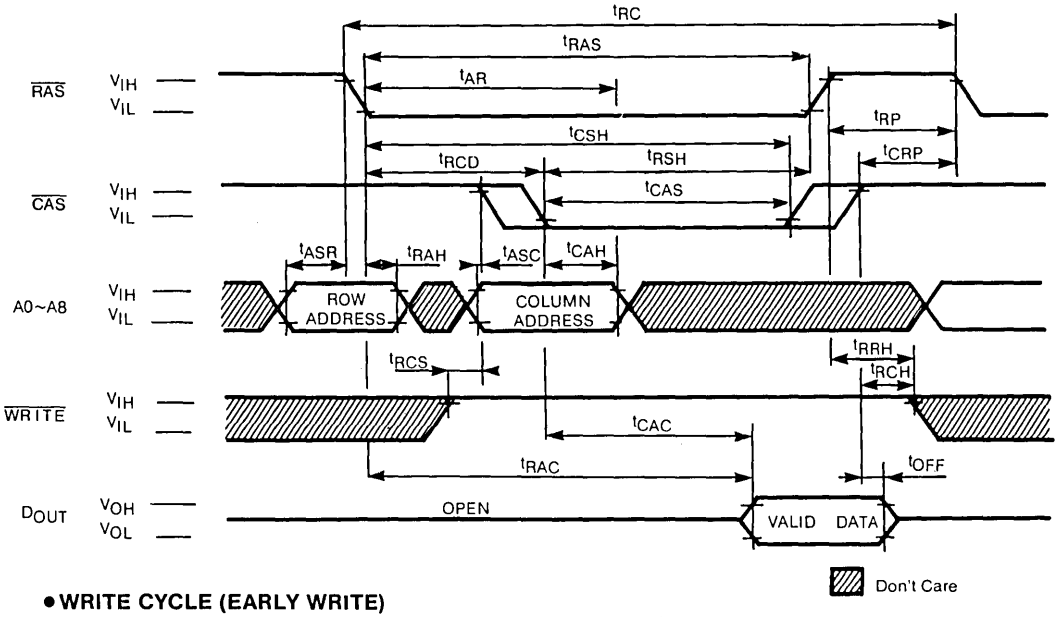
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A_0~A_8, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

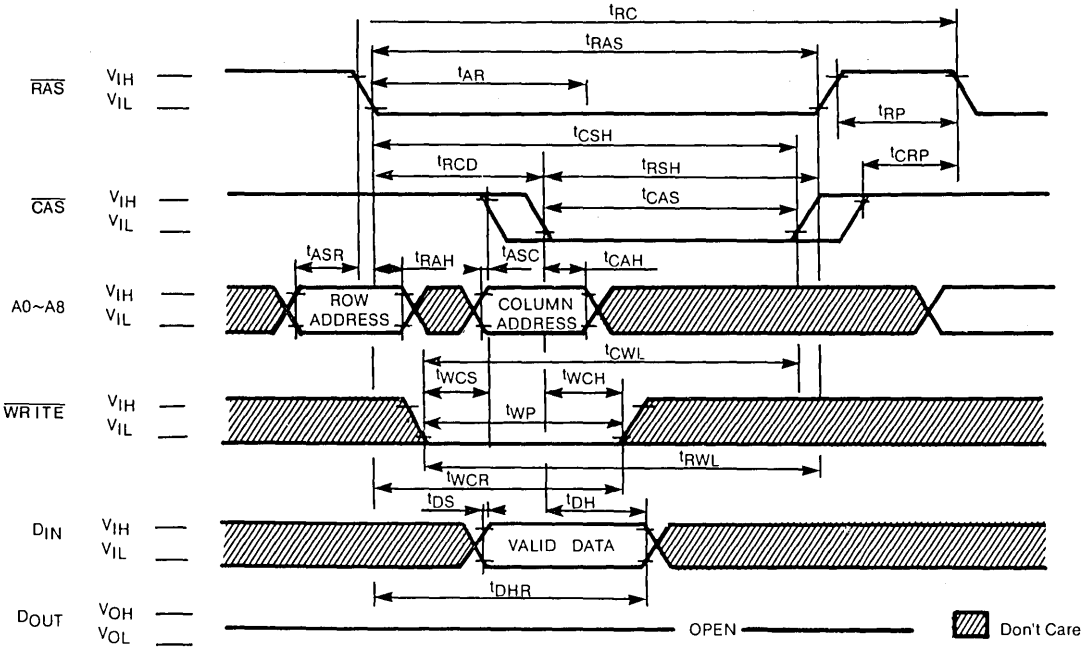
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$(min.) and $t_{RWD} \geqq t_{RWD}$(min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

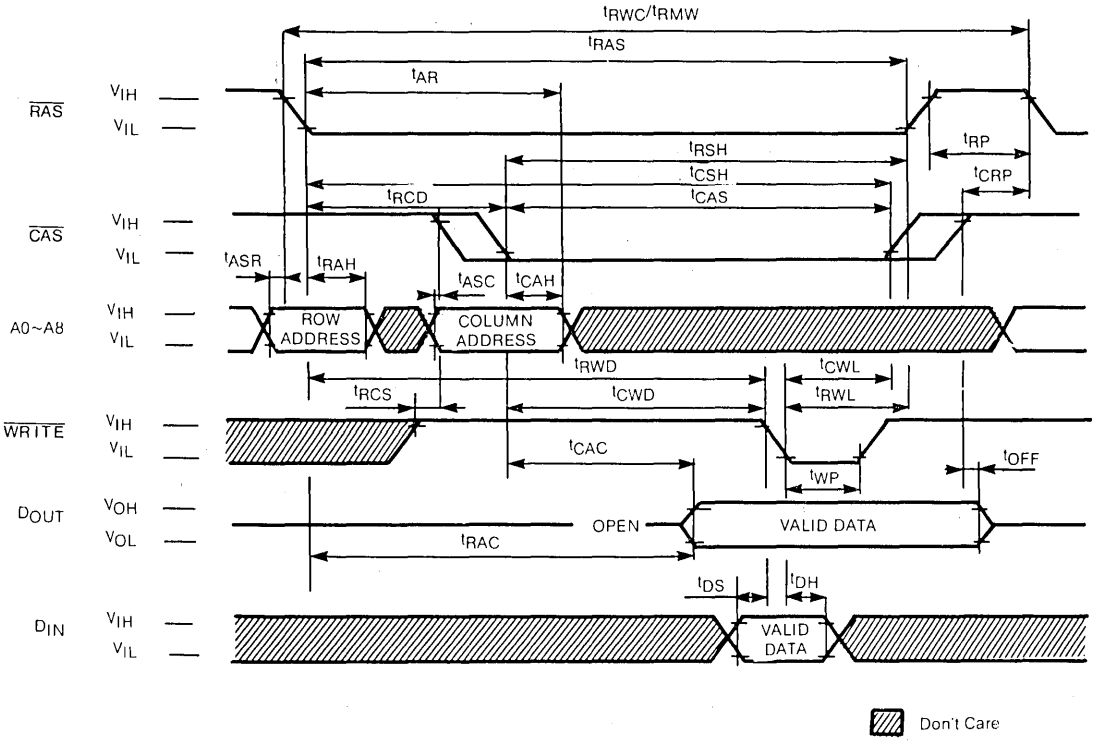
• READ CYCLE



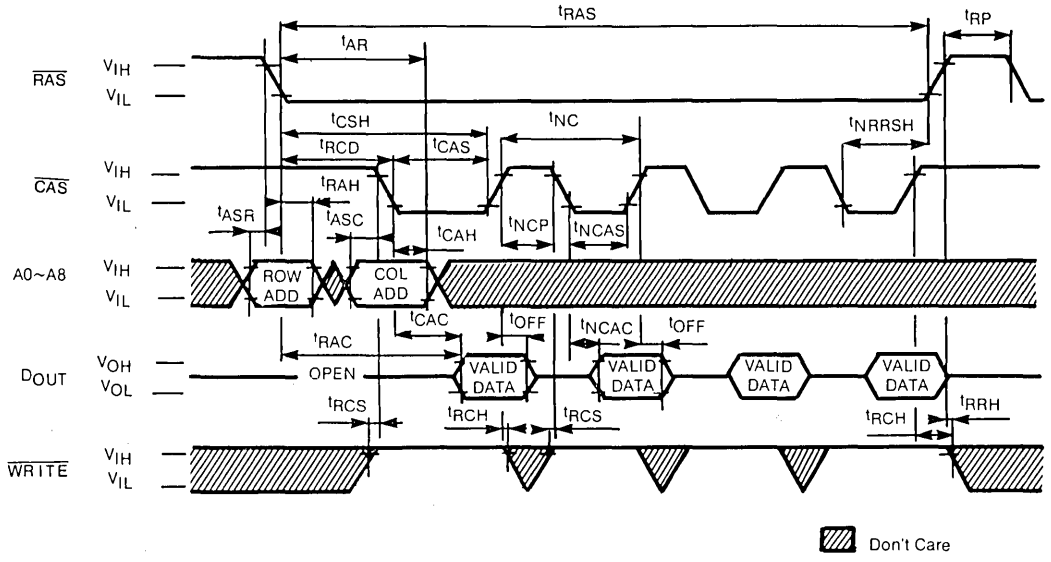
• WRITE CYCLE (EARLY WRITE)



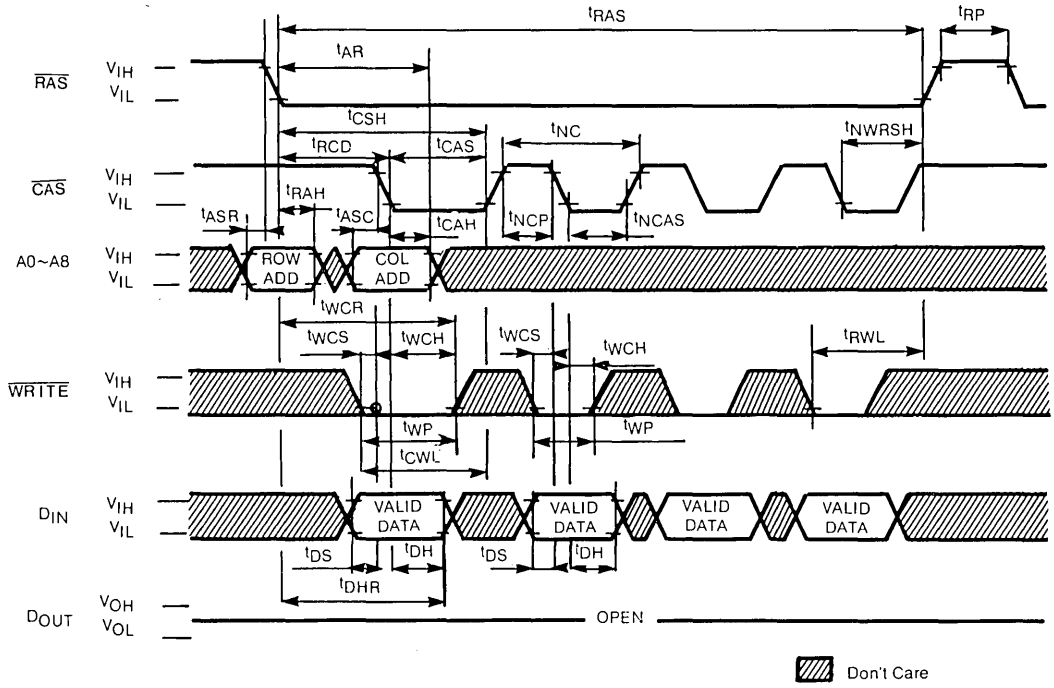
• READ-WRITE/READ-MODIFY-WRITE CYCLE



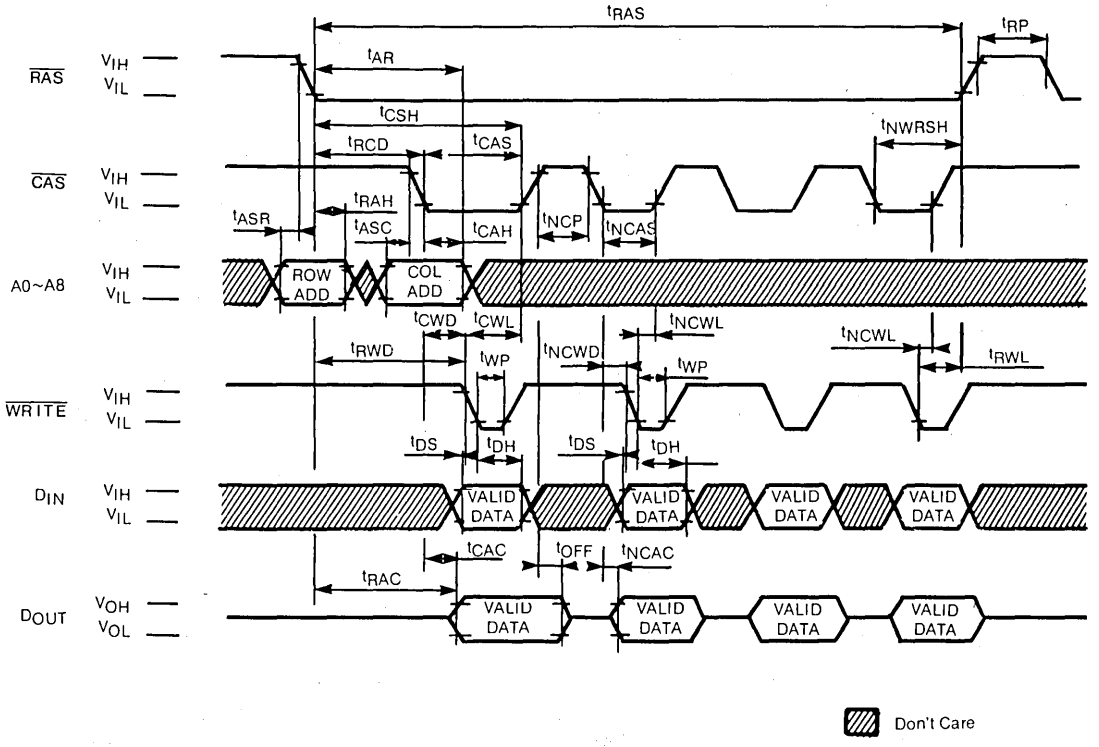
• NIBBLE MODE READ CYCLE



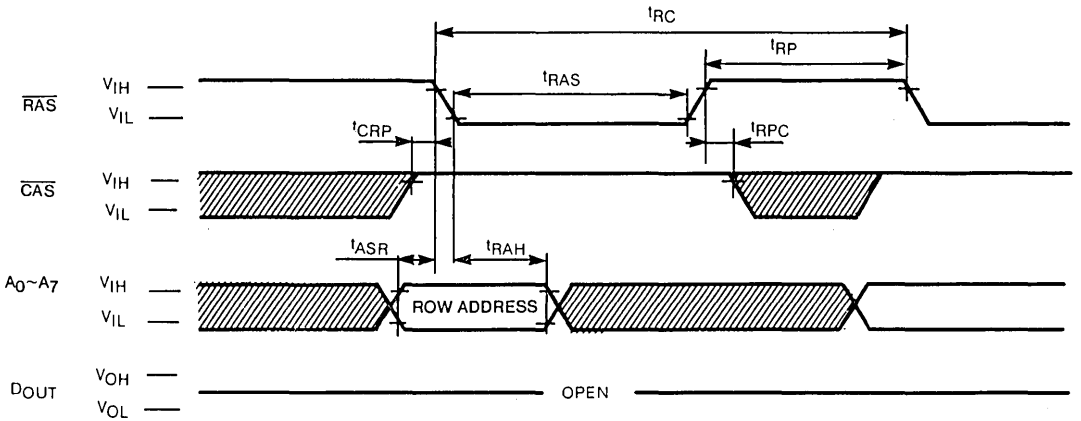
• NIBBLE MODE WRITE CYCLE



• NIBBLE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



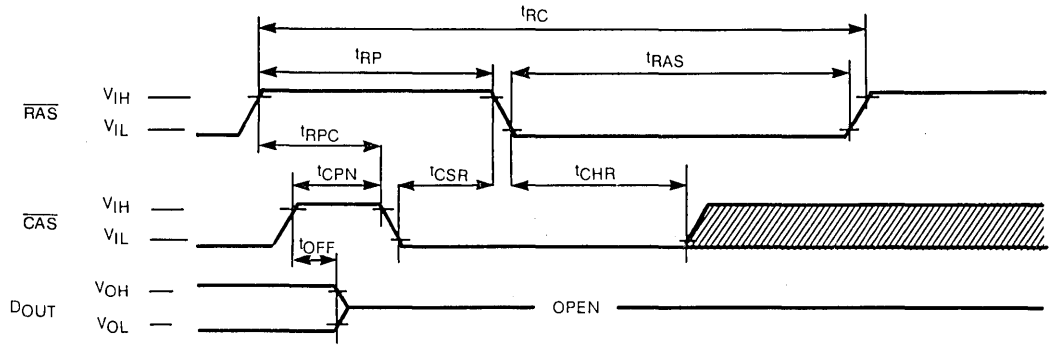
• $\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$ =Don't Care, A8=Don't Care

Don't Care

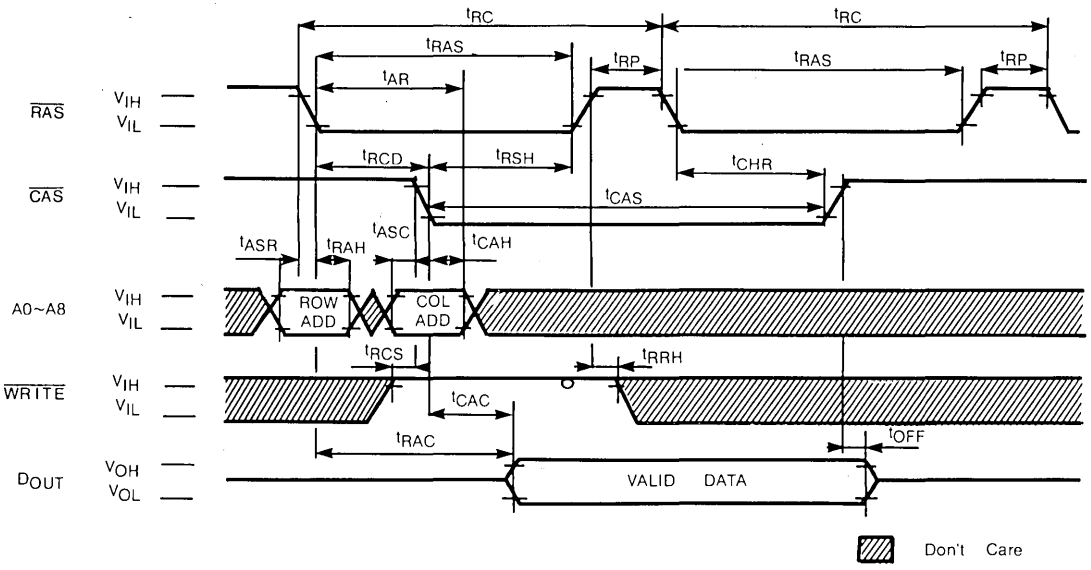
• $\overline{CAS}$ BEFORE $\overline{RAS}$ CYCLE



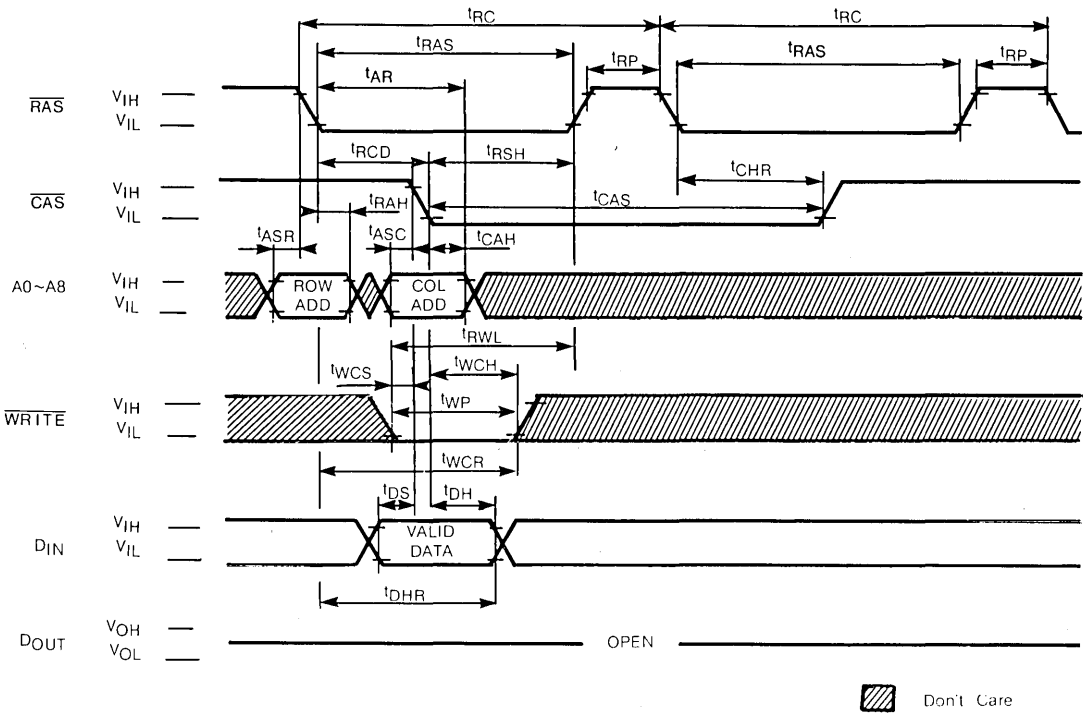
Note: $\overline{WRITE}$ =Don't Care, A0~A8=Don't Care

Don't Care

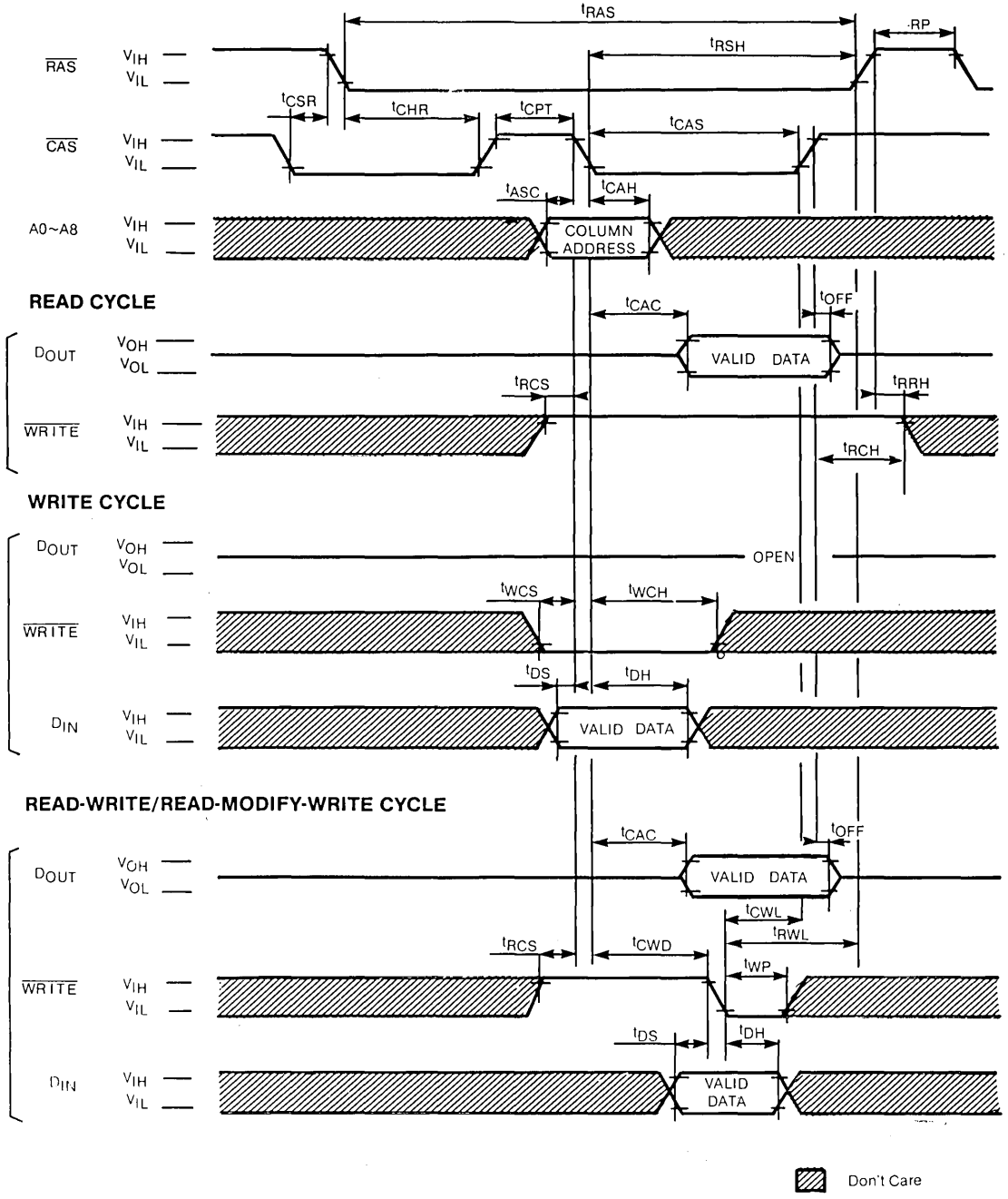
• HIDDEN REFRESH CYCLE (READ)



• HIDDEN REFRESH CYCLE (WRITE)



• $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41257P/T are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$ " feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

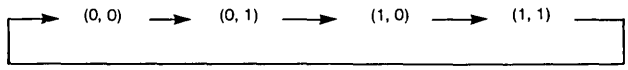
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41257P/T is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at a high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin one (A_8) determines the starting point of the circular 4 bits nibble. Row A_8 and column A_8 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A_8 row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

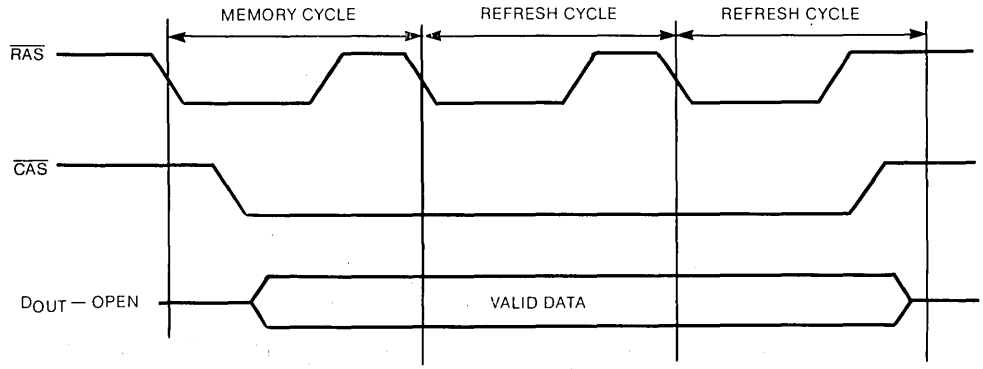
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A_0~A_7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results is a substantial reduction in operating power This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TMM41257P/T offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TMM41257P/T is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41257P/T can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as intialization cycles. The test procedure is as follows.

(1) Write "0" into all the memory cells at normal write mode.

(2) Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.

(3) Check "1" out of 256 bits at normal read mode, which was written at (2).

(4) Using the same column as (2), read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 256 times.

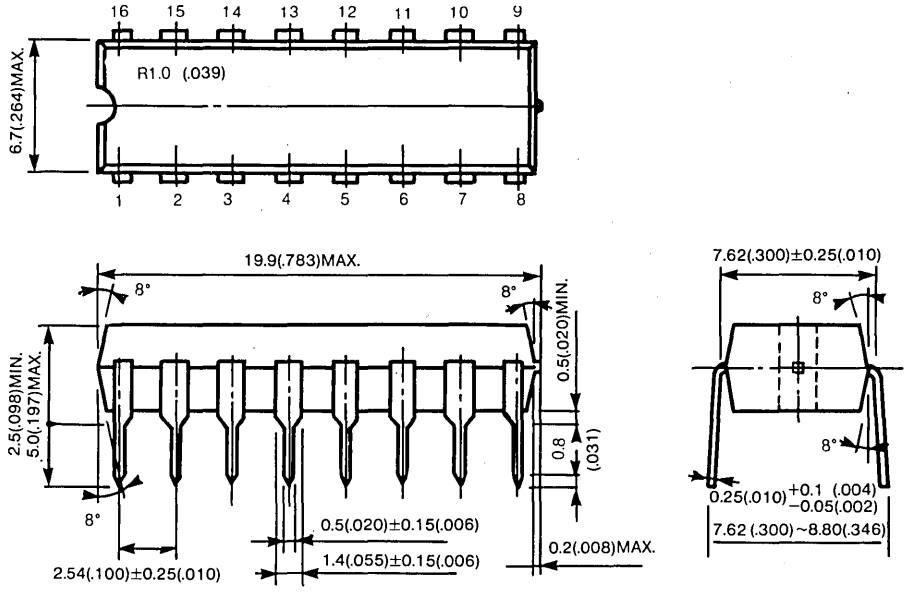
(5) Check "0" out of 256 bits at normal read mode, which was written at (4).

(6) Perform the above (1) to (5) with the complement data.

OUTLINE DRAWINGS

- **Plastic Dip**

Unit in mm (inches)

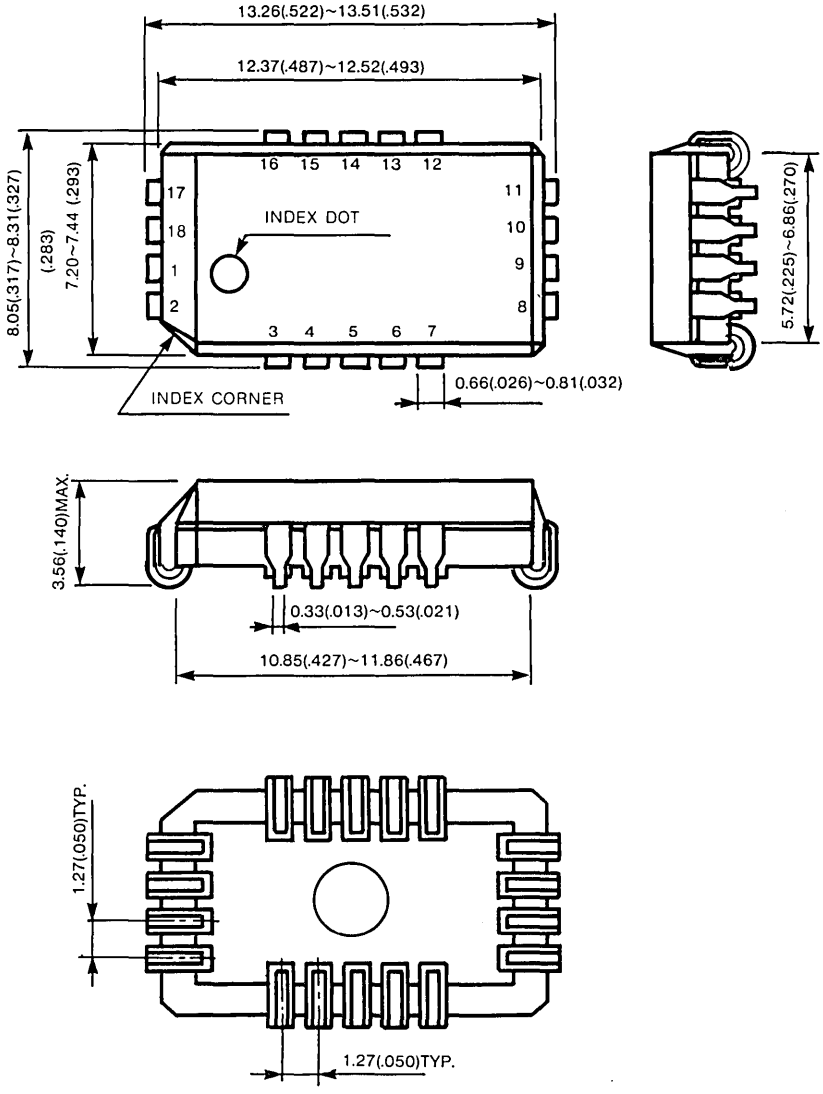


Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.16 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

- **Plastic LCC**

Unit in mm (inches)



TOSHIBA MOS MEMORY PRODUCT

262,144 WORD × 1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE CMOS

TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12
TMM41257AP/AT/AZ-15

*This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TMM41257AP/AT/AZ is an N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41257AP/AT/AZ to be packaged in a standard 16 pin plastic DIP, 18 pin PLCC and 16 pin ZIP. The package size allows for high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41257AP/AT/AZ high speed operation. Also, the advanced circuit techniques have achieved low power dissipation. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as schottky TTL. In addition to the $\overline{RAS}$-only refresh mode, a $\overline{CAS}$-before-$\overline{RAS}$ automatic refresh is available. Another special feature of the TMM41257AP/AT/AZ is nibble mode which allows the user to serially access 4 bits of data at a high data rate.

FEATURES

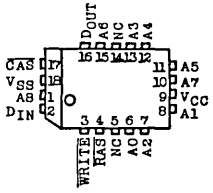
- 262,144 words by 1 bit organization
- Fast access time and cycle time

	TMM41257AP/AT/AZ-10/-12/-15
$\overline{RAS}$ Access Time	100ns/120ns/150ns
$\overline{CAS}$ Access Time	50ns/ 60ns/ 75ns
Cycle Time	190ns/220ns/260ns
Nibble Mode Access Time	25ns/ 30ns/ 40ns
Nibble Mode Cycle Time	50ns/ 60ns/ 70ns

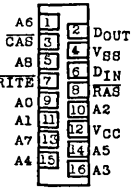
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power:
  440mW MAX. Operating (TMM41257AP/AT/AZ-10)
  396mW MAX. Operating (TMM41257AP/AT/AZ-12)
  358mW MAX. Operating (TMM41257AP/AT/AZ-15)
  28mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Nibble Mode capability
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  Plastic DIP : TMM41257AP
  Plastic Leaded Chip Carrier : TMM41257AT
  Plastic ZIP : TMM41257AZ

PIN CONNECTION (TOP VIEW)

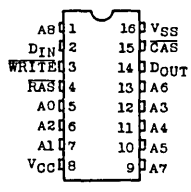
- Plastic LCC



- Plastic ZIP



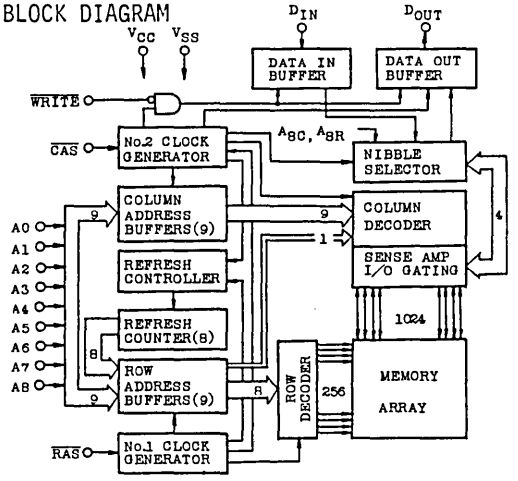
- Plastic DIP



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TMM41257AP/AT/AZ-10	-	80	mA	3, 4
		TMM41257AP/AT/AZ-12	-	72		
		TMM41257AP/AT/AZ-15	-	65		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TMM41257AP/AT/AZ-10	-	70	mA	3
		TMM41257AP/AT/AZ-12	-	62		
		TMM41257AP/AT/AZ-15	-	55		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{NC}=t_{NC} MIN.)	TMM41257AP/AT/AZ-10	-	50	mA	3, 4
		TMM41257AP/AT/AZ-12	-	45		
		TMM41257AP/AT/AZ-15	-	40		
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: t_{RC}=t_{RC} MIN.)	TMM41257AP/AT/AZ-10	-	70	mA	3
		TMM41257AP/AT/AZ-12	-	62		
		TMM41257AP/AT/AZ-15	-	55		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ +5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41257AP/AT/AZ-10		TMM41257AP/AT/AZ-12		TMM41257AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190	-	220	-	260	-	ns	
t_{RWC}	Read-Write Cycle Time	200	-	240	-	285	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	220	-	260	-	310	-	ns	
t_{NC}	Nibble Mode Cycle Time	50	-	60	-	70	-	ns	
t_{NRWC}	Nibble Mode Read-Write / Read-Modify-Write Cycle Time	75	-	90	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	100	-	120	-	150	ns	8,10
t_{CAC}	Access Time from $\overline{CAS}$	-	50	-	60	-	75	ns	9,10
t_{NCAC}	Nibble Mode Access Time	-	25	-	30	-	40	ns	10
t_{OFF}	Output Buffer Turn-Off Delay	5	25	5	30	5	35	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80	-	90	-	100	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	50	-	60	-	75	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100	-	120	-	150	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	50	10,000	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	50	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	20	-	25	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	25	-	30	-	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	70	-	85	-	105	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	-	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	10	-	15	-	20	-	ns	12
t_{WCH}	Write Command Hold Time	20	-	25	-	30	-	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	70	-	85	-	105	-	ns	
t_{WP}	Write Command Pulse Width	20	-	25	-	30	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	-	35	-	45	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	-	35	-	45	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TMM41527AP/AT/AZ-10		TMM41527AP/AT/AZ-12		TMM41527AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	14
t_{DH}	Data-In Hold Time	20	-	25	-	30	-	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	70	-	85	-	105	-	ns	
t_{REF}	Refresh Period	-	4	-	4	-	4	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	30	-	40	-	50	-	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80	-	100	-	125	-	ns	15
t_{NCAS}	Nibble Mode $\overline{CAS}$ Pulse Width	25	-	30	-	40	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	15	-	20	-	20	-	ns	
t_{NRRSH}	Nibble Mode $\overline{RAS}$ Hold Time (Read)	20	-	25	-	30	-	ns	
t_{NWRSH}	Nibble Mode $\overline{RAS}$ Hold Time (Write)	40	-	45	-	50	-	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	25	-	30	-	40	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	40	-	50	-	60	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A_0∿A_8, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Assumes that $t_{RCD} \leqq t_{RCD}$(max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

9. Assumes that $t_{RCD} \geqq t_{RCD}$(max.)

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

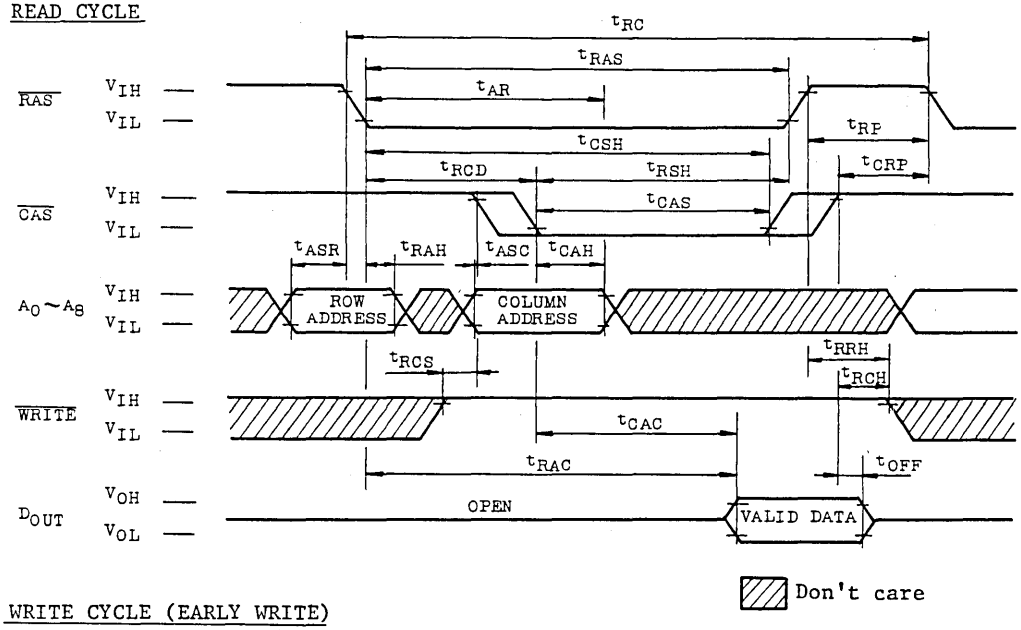
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled exclusively by t_{CAC}.

14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.

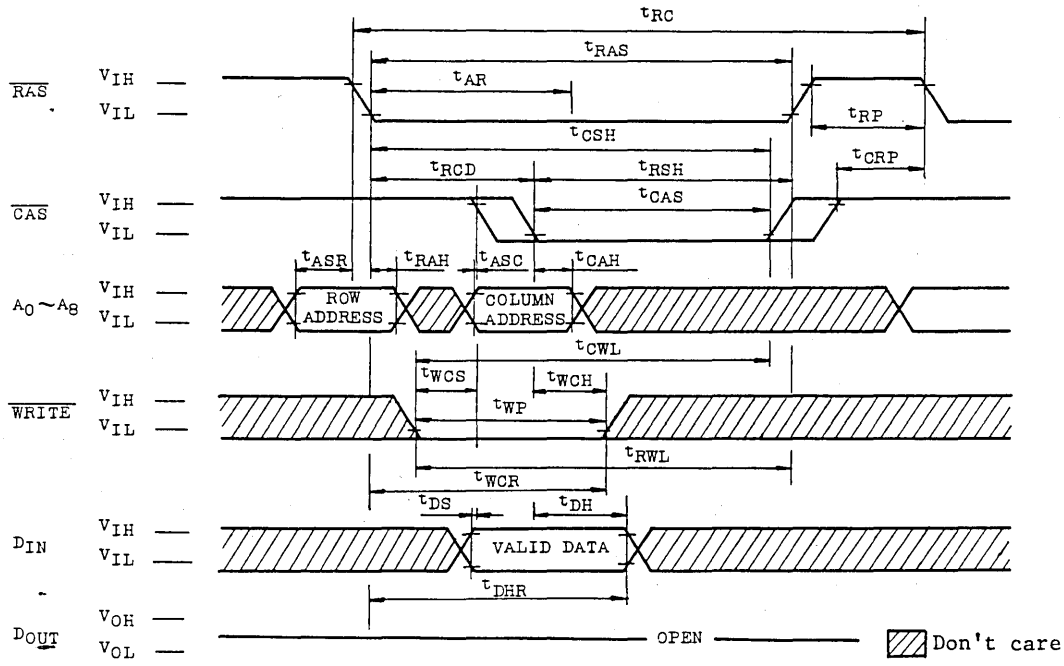
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$(min.) and $t_{RWD} \geqq t_{RWD}$(min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

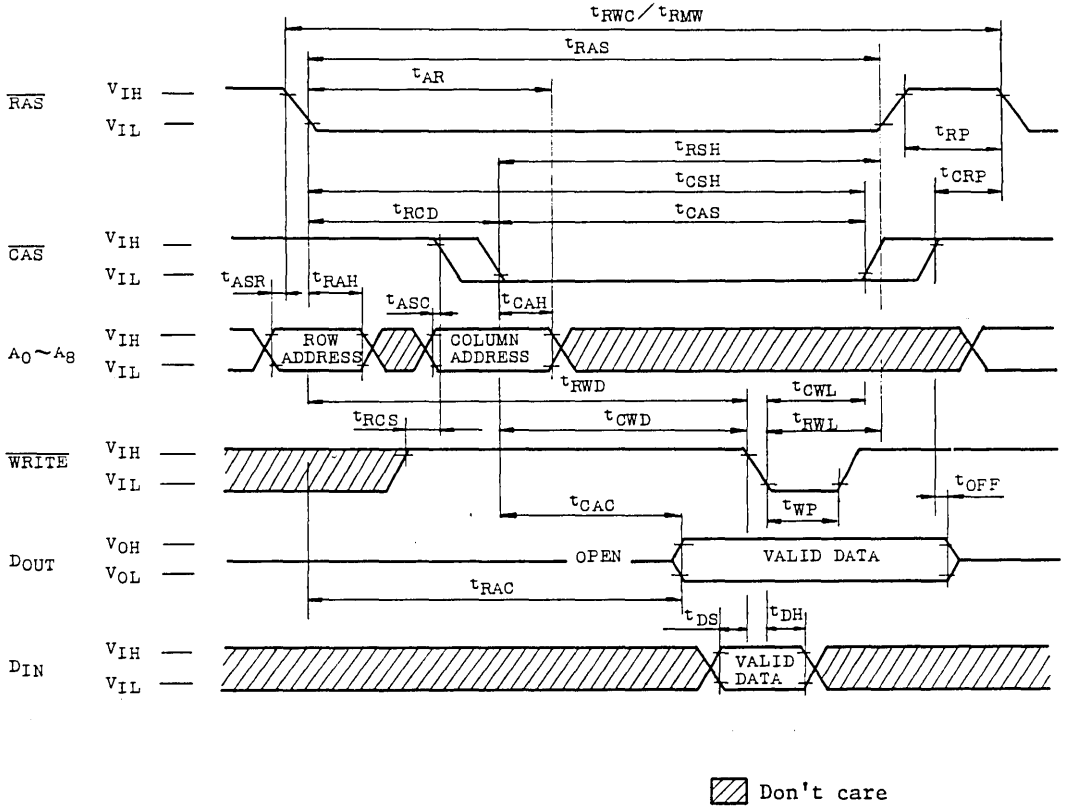
READ CYCLE



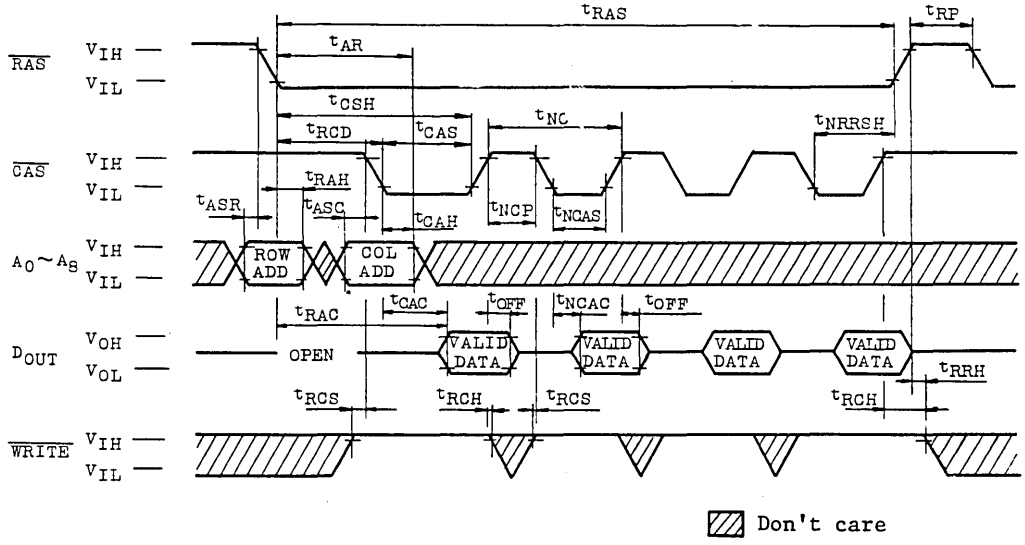
WRITE CYCLE (EARLY WRITE)



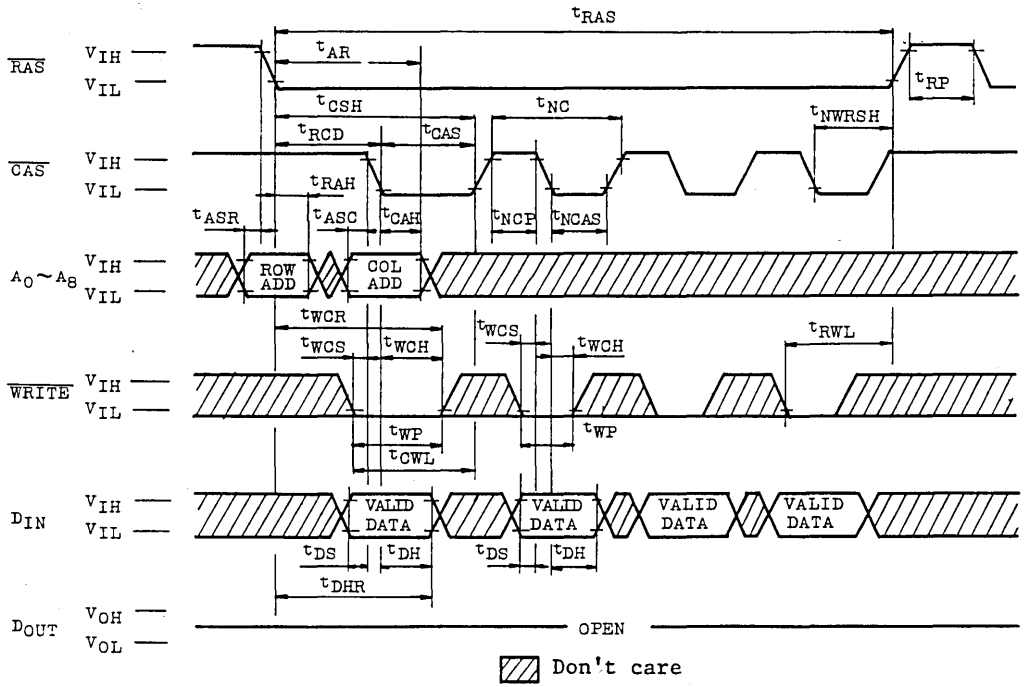
READ-WRITE/READ-MODIFY-WRITE CYCLE



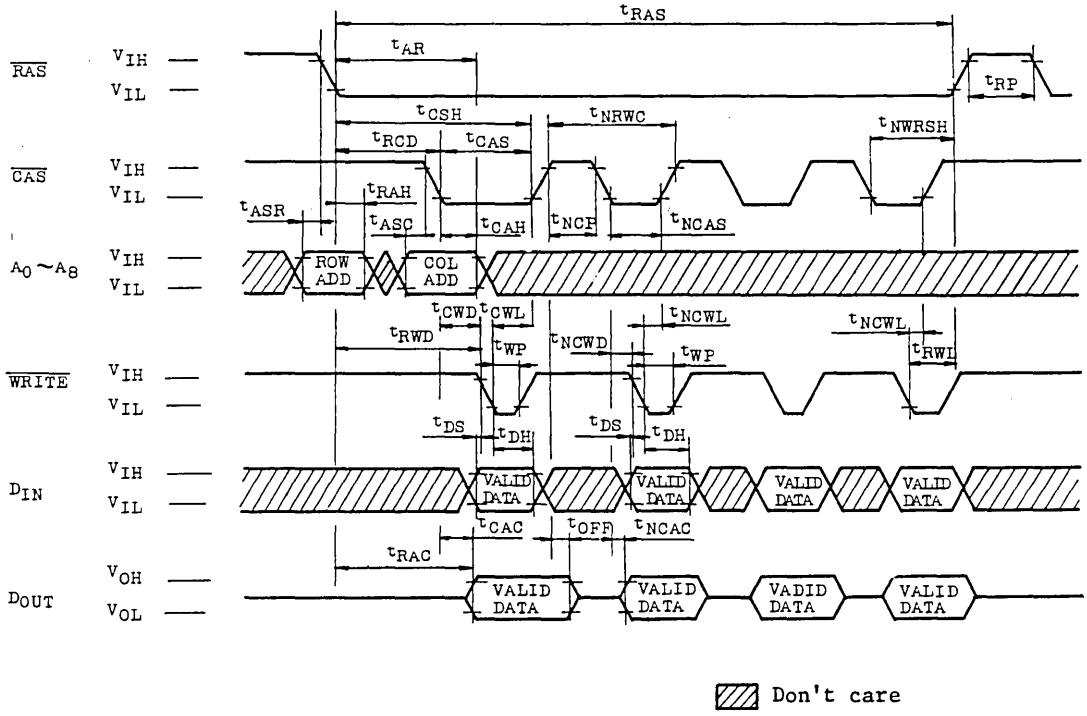
NIBBLE MODE READ CYCLE



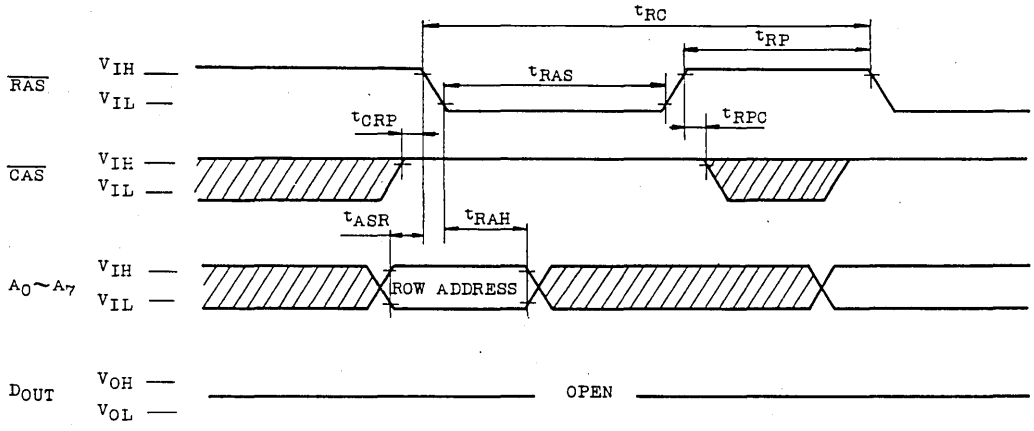
NIBBLE MODE WRITE CYCLE (EARLY WRITE)



NIBBLE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



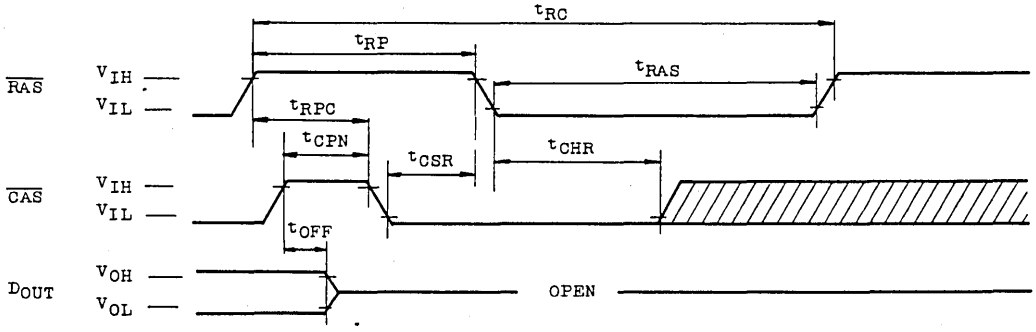
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$=Don't care, A8=Don't care

Don't care

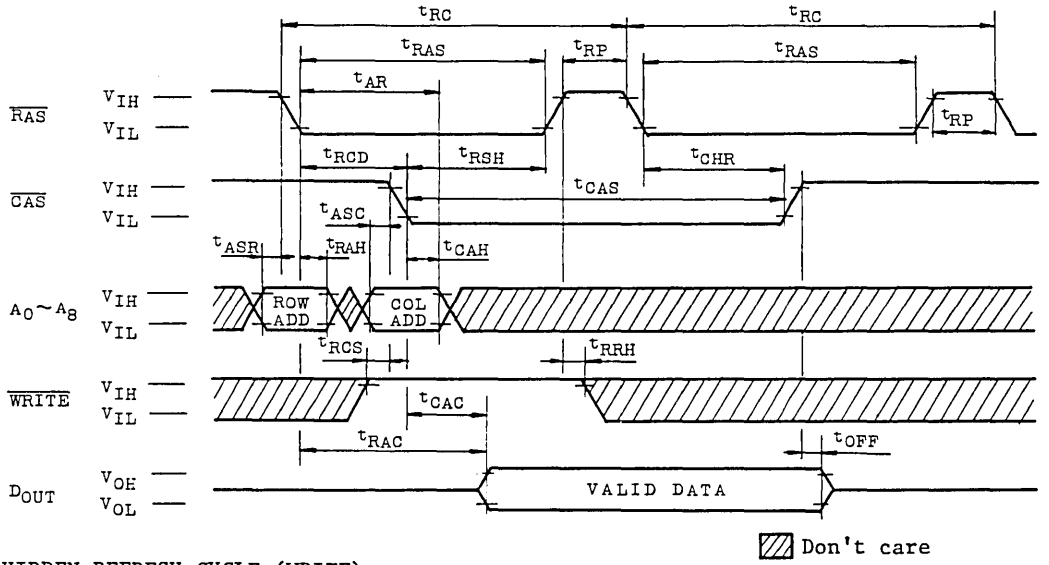
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



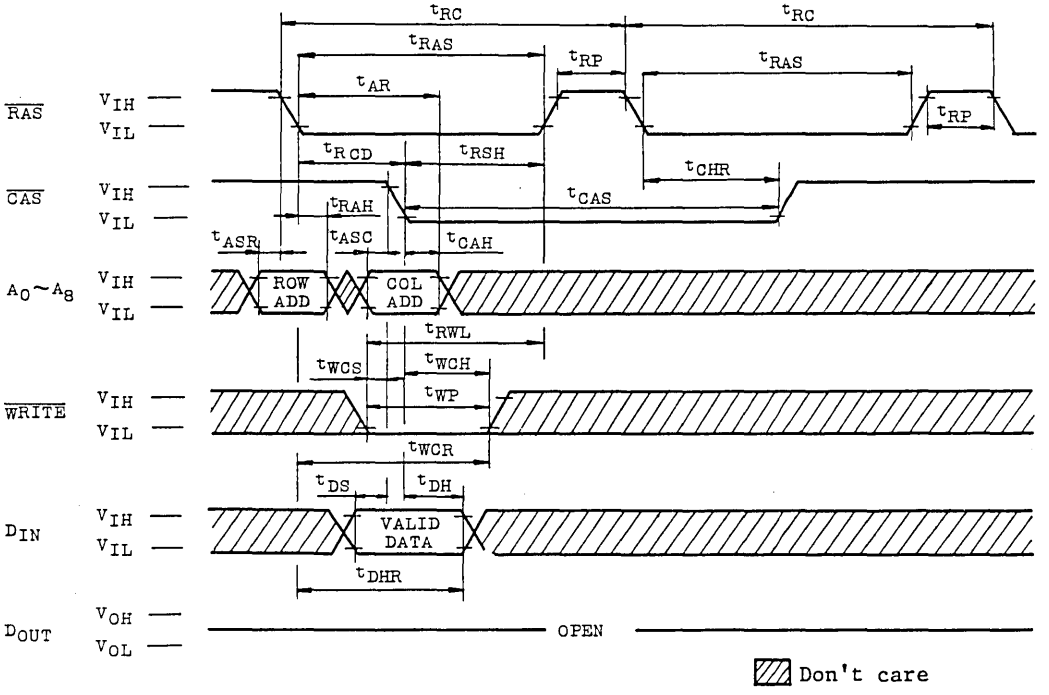
Note: $\overline{WRITE}$=Don't care, A0 ∿ A8=Don't care

Don't care

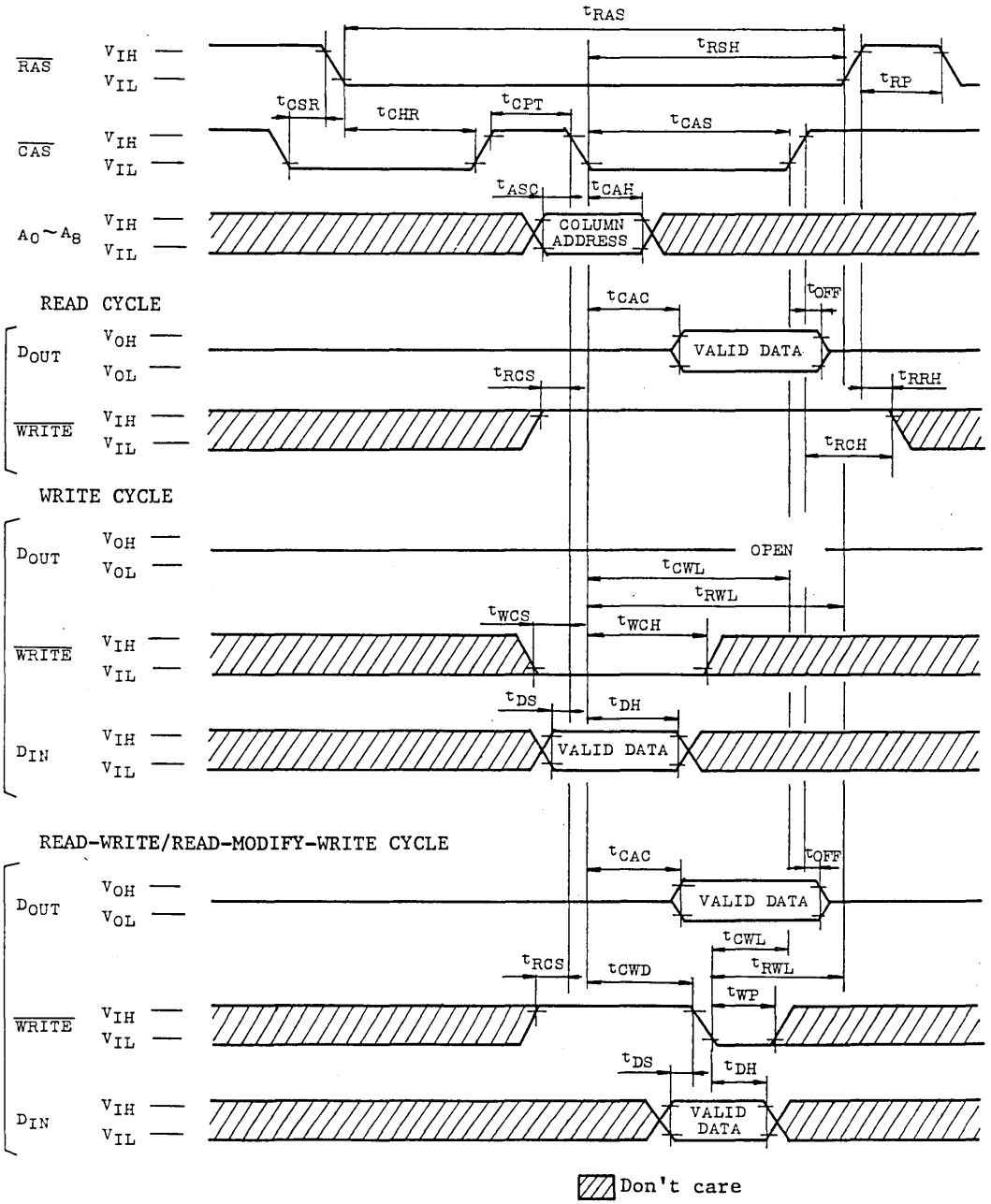
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41257AP/AT/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

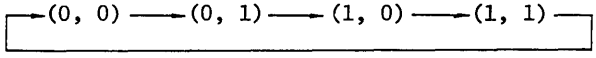
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be avialable at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41257AP/AT/AZ is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin one (A_8) determines the starting point of the circular 4 bits nibble. Row A_8 and column A_8 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion: 00 → 01 → 10 → 11 with A_8 row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

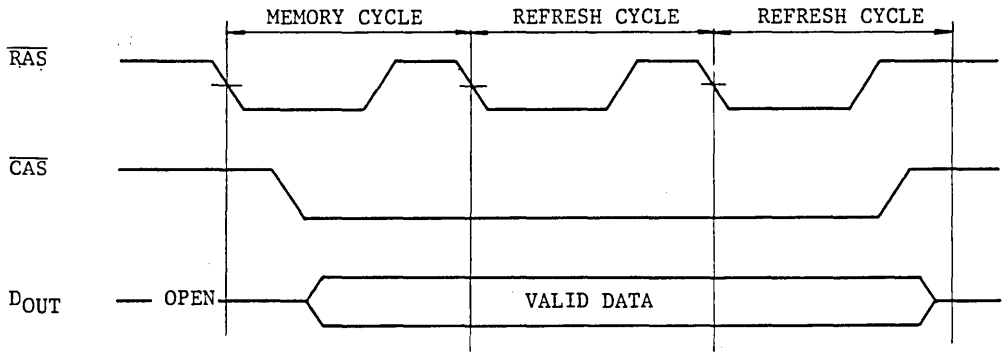
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($A_0 \sim A_7$) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TMM41257AP/AT/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TMM41257AP/AT/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41257AP/AT/AZ can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST.
Repeat this operation 256 times.

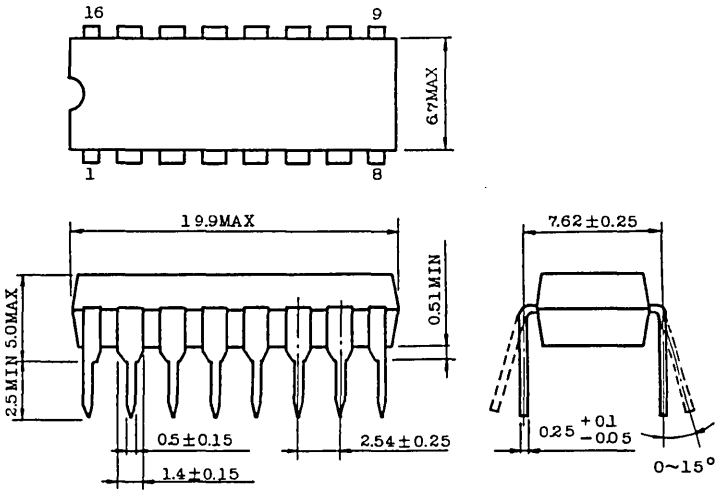
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS

• Plastic DIP

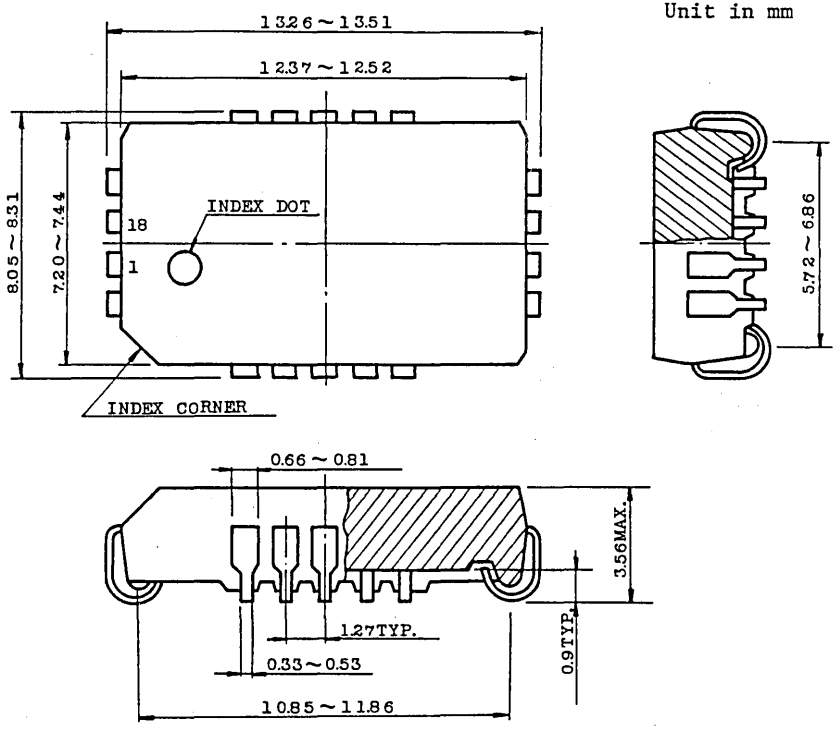
Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.16 leads. All dimensions are in millimeters.

• Plastic LCC

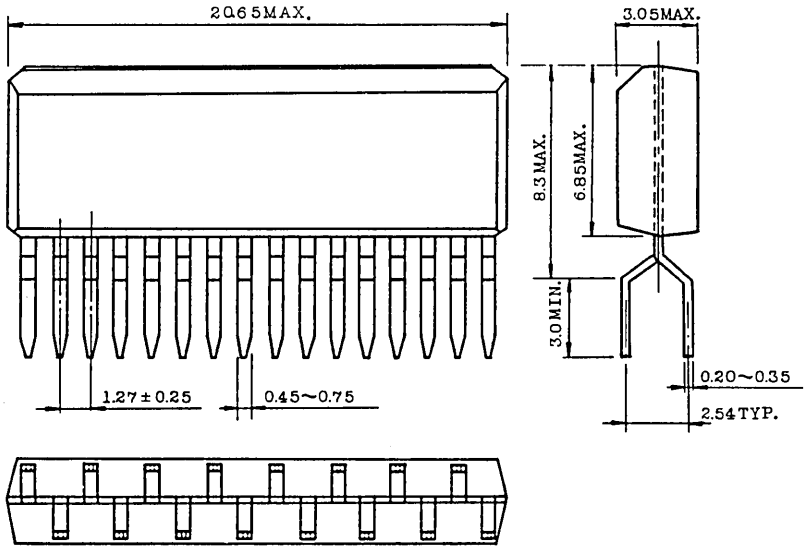
Unit in mm



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCT

65,536 WORD × 4 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41464P-12
TMM41464P-15

DESCRIPTION

The TMM41464P is the new generation dynamic RAM organized 65,536 word by 4 bit, it is successor to the industry standard TMM4164AP.

The TMM41464P utilizes TOSHIBA's N-channel/ Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM 41464P to be packaged in a standard 18 pin plastic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as schottky TTL.

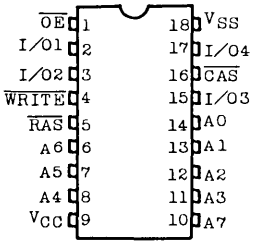
FEATURES

- 65,536 words by 4 bit organization
- Fast access Time and cycle time

DEVICE	t_{RAC}	t_{CAC}	t_{RC}
TMM41464P-12	120ns	60ns	220ns
TMM41464P-15	150ns	75ns	260ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low power:
  385mW Operating (MAX.) (TMM41464-12)
  330mW Operating (MAX.) (TMM41464-15)
  28mW Standby (MAX.)
- Industory standard 18 pin plastic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{RAS}$ only refresh, Hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, and Page Mode capability.
- All inputs and outputs TTL compatible
- 256 refresh cycles/4ms

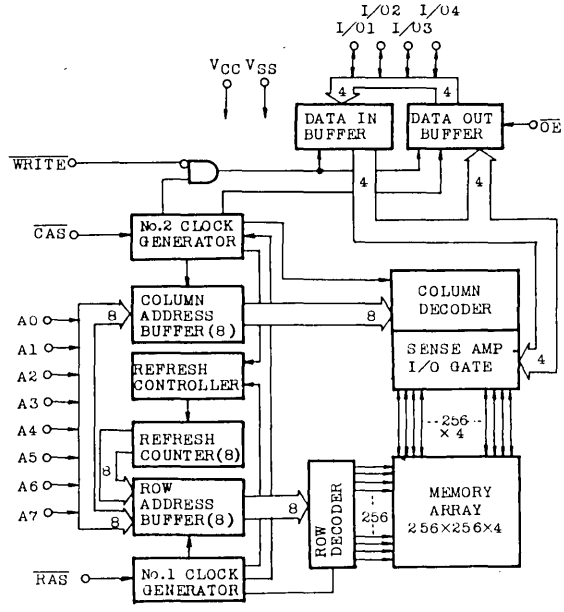
PIN CONNECTION



PIN NAMES

A_0~A_7	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/O_1~I/O_4	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature·Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	—	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling : t_{RC}=t_{RC} MIN.)	TMM41464P-12	—	70	mA	3,4
		TMM41464P-15	—	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		—	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH} : t_{RC}=t_{RC} MIN.)	TMM41464P-12	—	60	mA	3
		TMM41464P-15	—	50		
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling : t_{PC}=t_{PC} MIN.)	TMM41464P-12	—	60	mA	3,4
		TMM41464P-15	—	50		
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: t_{RC}=t_{RC} MIN.)	TMM41464P-12	—	60	mA	3
		TMM41464P-15	—	50		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≦V_{IN}≦6.5V, All Other Pins Not Under Test =0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V≦V_{OUT}≦+5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=−5mA)		2.4		V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)			0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41464P-12		TMM41464P-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	220	—	260	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	295	—	355	—	ns	
t_{PC}	Page Mode Cycle Time	120	—	145	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	120	—	150	ns	8,10
t_{CAC}	Access Time from $\overline{CAS}$	—	60	—	75	ns	9,10
t_{OFF}	Output Buffer Turn-Off Delay	0	35	0	40	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	90	—	100	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	60	—	75	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120	—	150	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	20	—	25	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	50	—	60	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	25	—	35	—	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	85	—	110	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	—	0	—	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	15	—	20	—	ns	12
t_{WCH}	Write Command Hold Time	35	—	45	—	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	95	—	120	—	ns	
t_{WP}	Write Command Pulse Width	35	—	45	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35	—	45	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35	—	45	—	ns	
t_{DS}	Data-In Set-Up Time	0	—	0	—	ns	14
t_{DH}	Data-In Hold Time	35	—	45	—	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	95	—	120	—	ns	
t_{REF}	Refresh Period	—	4	—	4	ms	
t_{WCS}	Write Command Set-Up Time	0	—	0	—	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	100	—	120	—	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	160	—	195	—	ns	15
t_{OEA}	$\overline{OE}$ Access time	—	30	—	40	ns	
t_{OED}	$\overline{OE}$ to Data Delay	30	—	40	—	ns	
t_{OEZ}	Output Buffer Turn-Off Delay Time from $\overline{OE}$	0	30	0	40	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	30	—	40	—	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Refereuco to $\overline{OE}$	0	—	0	—	ns	

SYMBOL	PARAMETER	TMM41464P-12		TMM41464P-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX		
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	30	—	30		ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	10	—	10		ns	
t_{RPC}	$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	0	—	0		ns	
t_{CPT}	$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	50	—	60		ns	

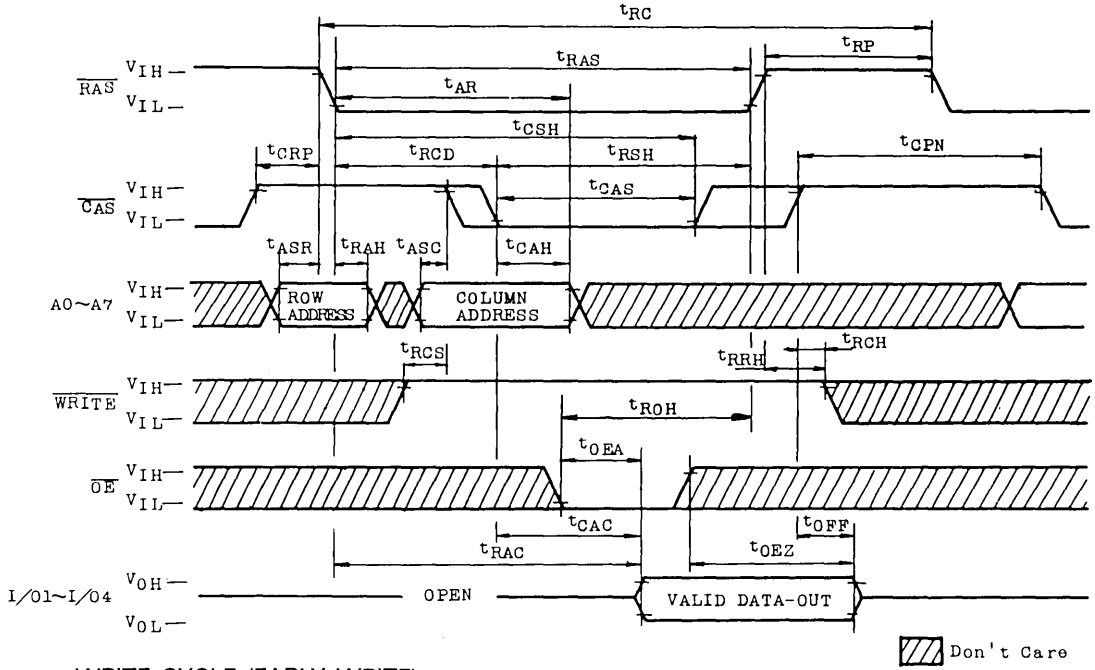
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A_0 ~ A_7)		5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)		7	pF
C_O	Input/Output Capacitance ($I/O1$ ~ $I/O4$)		7	pF

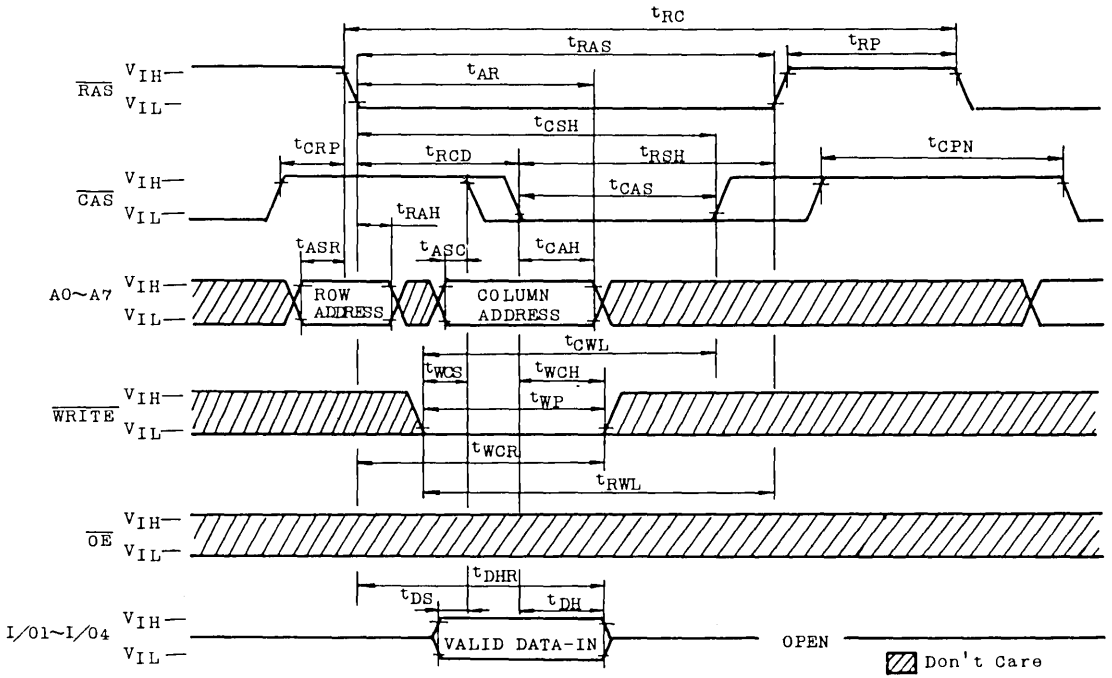
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are refrenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimun of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycle are required.
6. AC measurements assume t_T = 5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
10. Measured with a load equivalent to 2 TLL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These paramenters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the input/output pin will remain open circuits (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$(min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell.

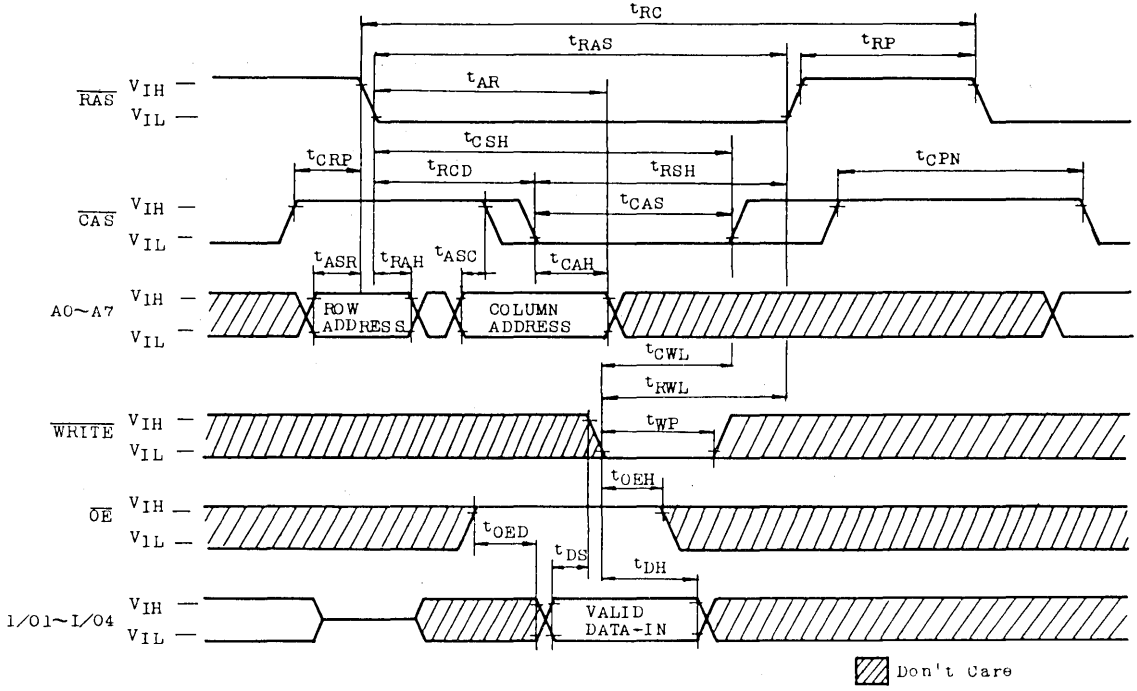
● READ CYCLE



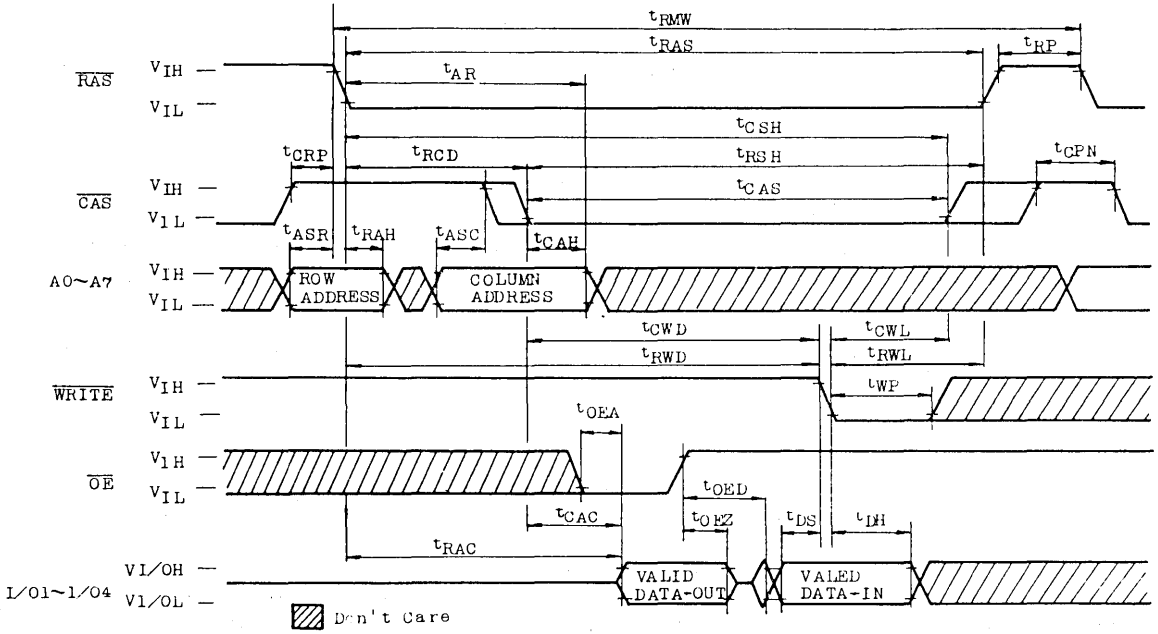
○ WRITE CYCLE (EARLY WRITE)



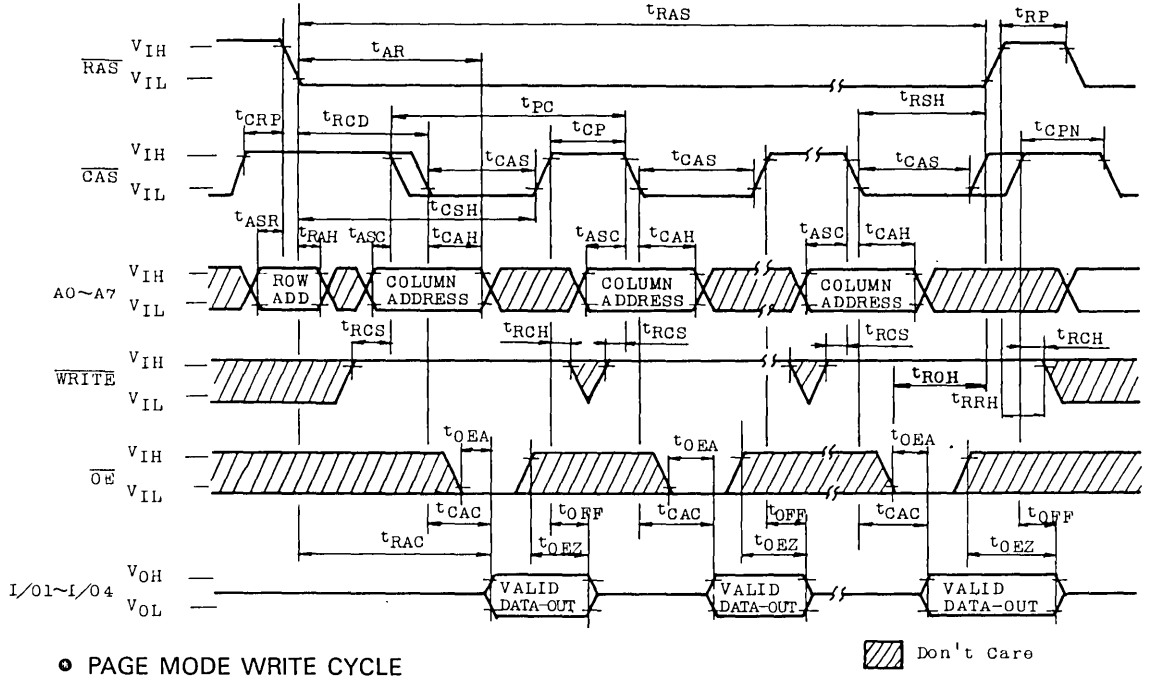
- WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



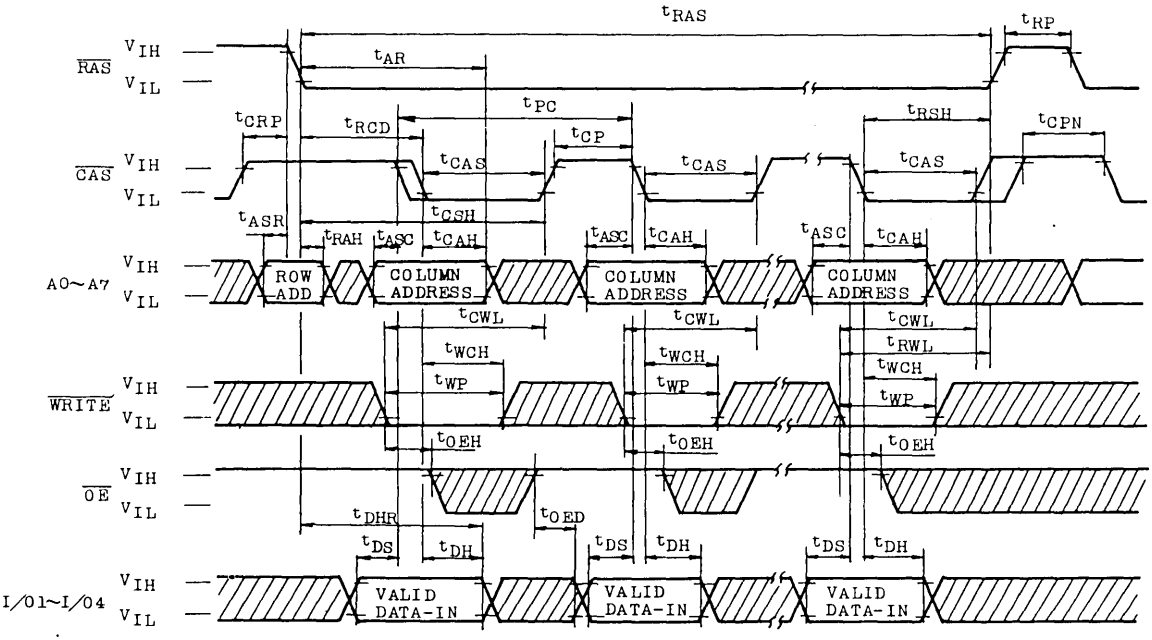
- READ-WRITE/READ-MODIFY-WRITE CYCLE



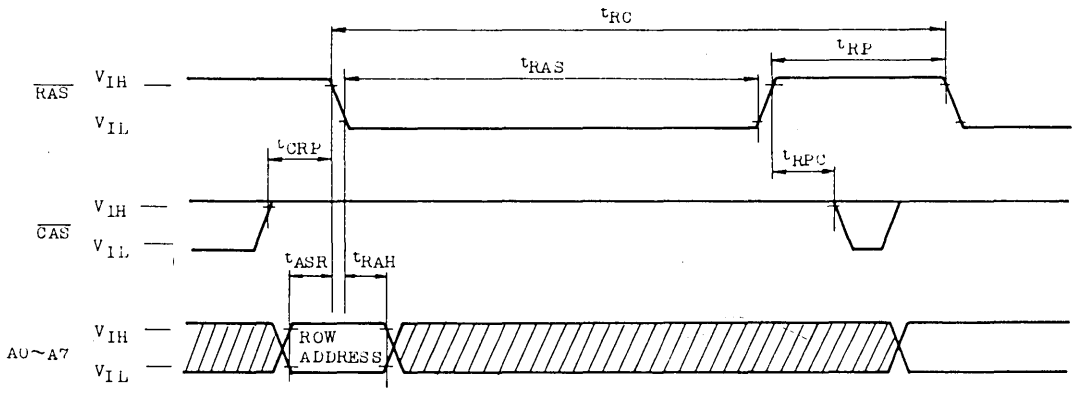
● PAGE MODE READ CYCLE



● PAGE MODE WRITE CYCLE

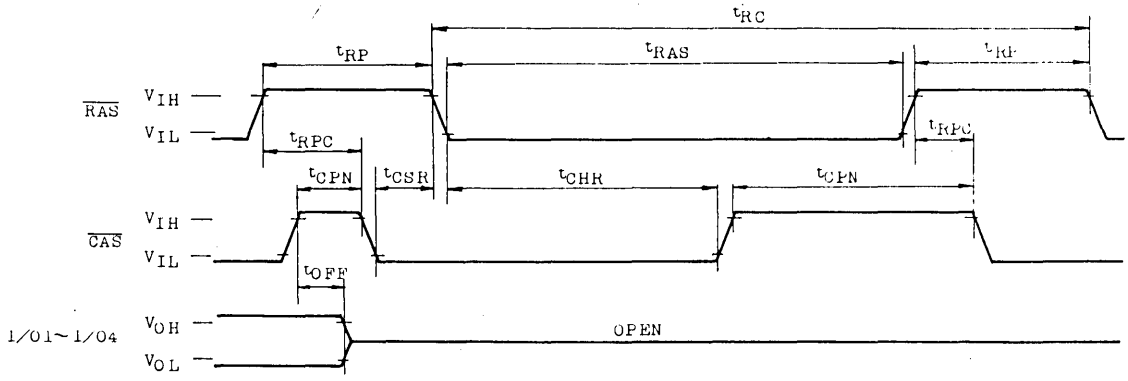


- $\overline{RAS}$ ONLY REFRESH CYCLE



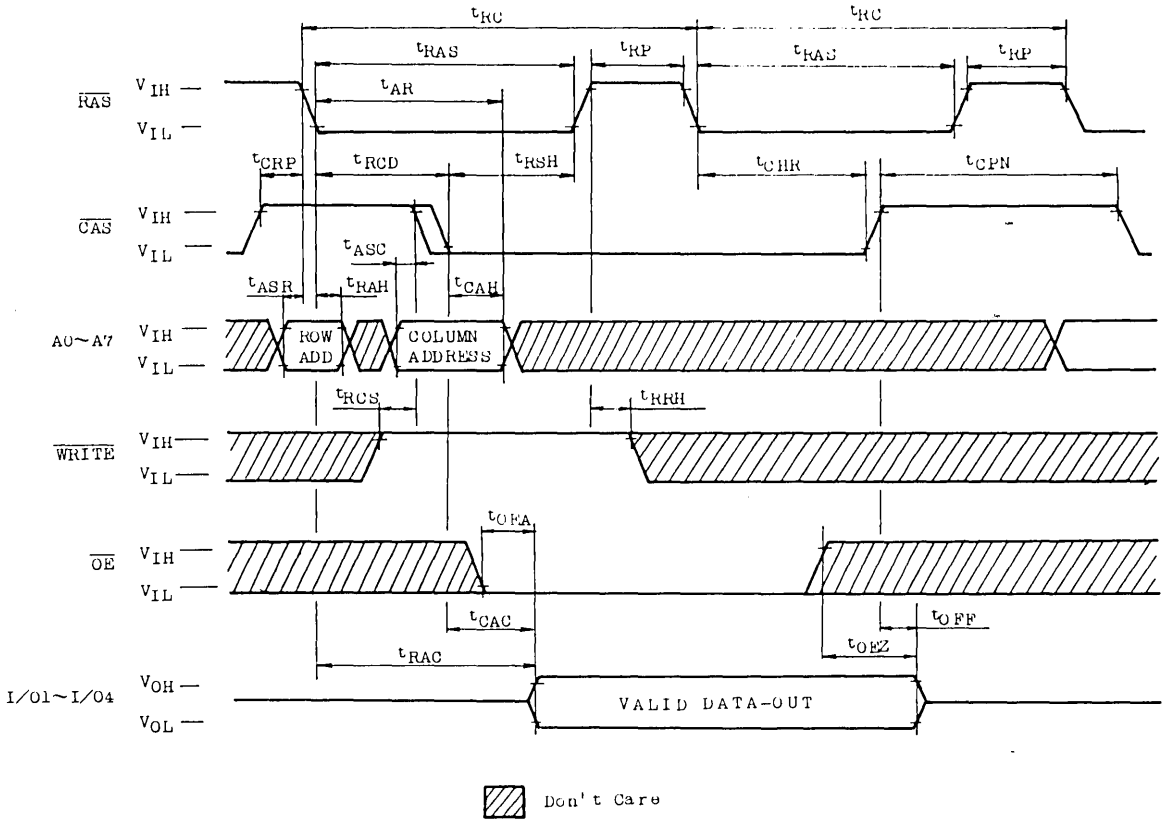
Notes: $\overline{WRITE}$, $\overline{OE}$=Don't Care

- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

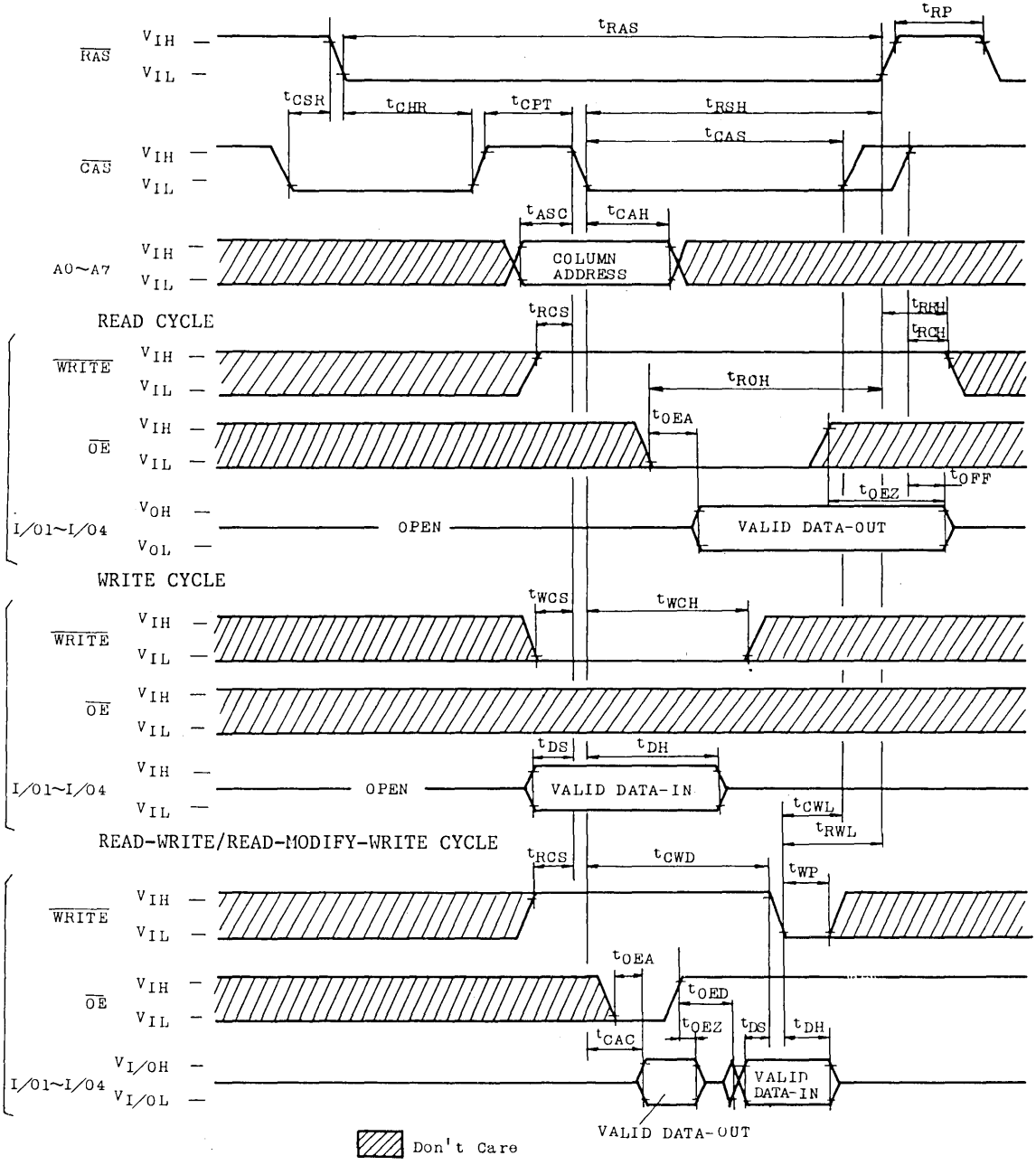


Note: $\overline{WRITE}$, $\overline{OE}$, A0 ∿ A7=Don't Care

- HIDDEN REFRESH CYCLE



- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TMM41464P are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

Data is written during write or read-modify-write cycle.

The falling edge of $\overline{CAS}$ or $\overline{WRITE}$ strobes data into the on-chip data latches.

In an early-write cycle, $\overline{WRITE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WRITE}$ with setup and hold time referenced to this signal.

In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed -write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state

When the $\overline{OE}$ input is brought to a logic low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A_0-A_7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TMM41464P offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation .

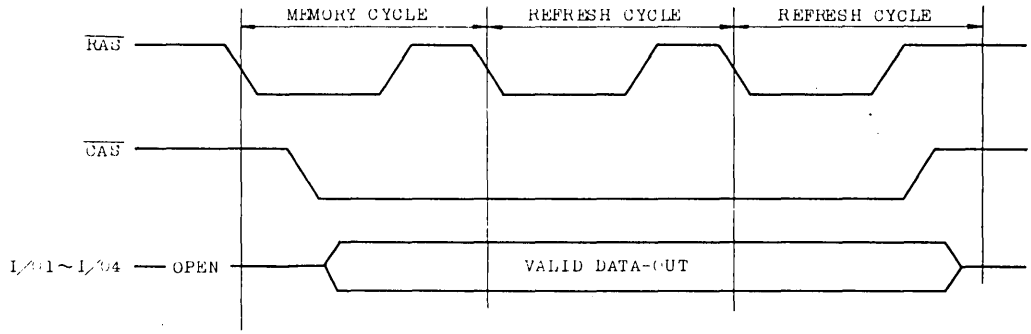
PAGE MODE

The "Page-Mode" feature of the TMM41464P allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative

going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TMM41464P is that refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

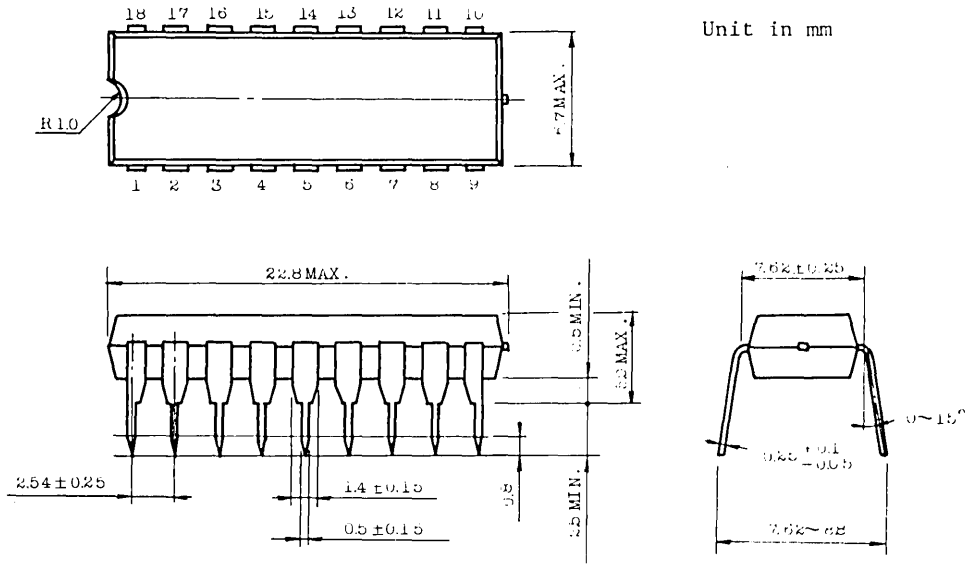
The internal refresh operation of TMM41464P can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.
② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE).
Repeat this operation 256 times.
③ Check "1" out of 256 bits at normal read mode, which was written at ②.
④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. Repeat this operation 256 times.
⑤ Check"0" out of 256 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ to the complement data.

OUTLINE DRAWINGS

Unit in mm



NOTES : Each lead pitch is 2.54mrn. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads. Alldimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 1 BIT DYNAMIC RAM
SILICON GATE CMOS

TC511000P/J/Z-85, TC511000P/J/Z-10
TC511000P/J/Z-12

DESCRIPTION

The TC511000P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. "Test Mode" function is implemented from Revision C.

FEATURES

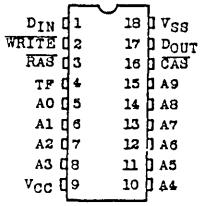
- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

		TC511000P/J/Z-85-10-12		
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

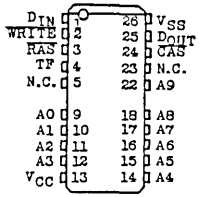
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  385mW MAX. Operating(TC511000P/J/Z-85)
  330mW MAX. Operating(TC511000P/J/Z-10)
  275mW MAX. Operating(TC511000P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511000P
  Plastic SOJ: TC511000J
  Plastic ZIP: TC511000Z

PIN CONNECTION (TOP VIEW)

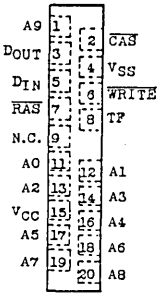
Plastic DIP



Plastic SOJ



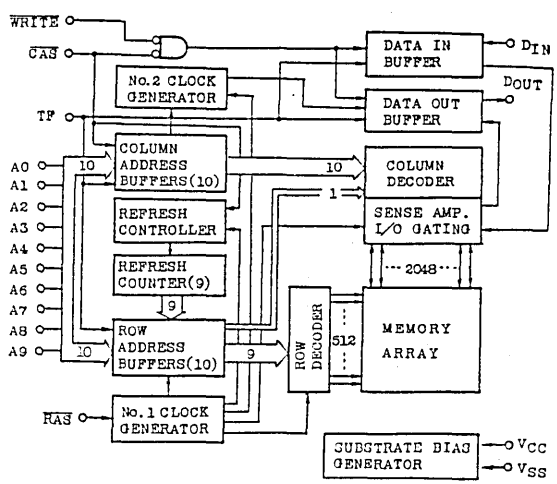
Plastic ZIP



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	-1 ∿ 10.5	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC}+4.5	-	10.5	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511000P/J/Z-85 TC511000P/J/Z-10 TC511000P/J/Z-12	- - -	70 60 50	mA	3,4
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511000P/J/Z-85 TC511000P/J/Z-10 TC511000P/J/Z-12	- - -	70 60 50	mA	3
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC511000P/J/Z-85 TC511000P/J/Z-10 TC511000P/J/Z-12	- - -	50 40 30	mA	3,4
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC511000P/J/Z-85 TC511000P/J/Z-10 TC511000P/J/Z-12	- - -	70 60 50	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≦ $V_{IN(TF)}$ ≦ 0.8V, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	µA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC}+4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		-	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511000P/J/Z-85		TC511000P/J/Z-10		TC511000P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{RWC}	Read-Write Cycle Time	190	-	220	-	255	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	55	-	70	-	ns	
t_{PRWC}	Fast Page Mode Read-Write Cycle Time	75	-	85	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	50	-	65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511000P/J/Z-85		TC511000P/J/Z-10		TC511000P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	25	-	25	-	30	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	100	-	120	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	45	-	50	-	60	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEH}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

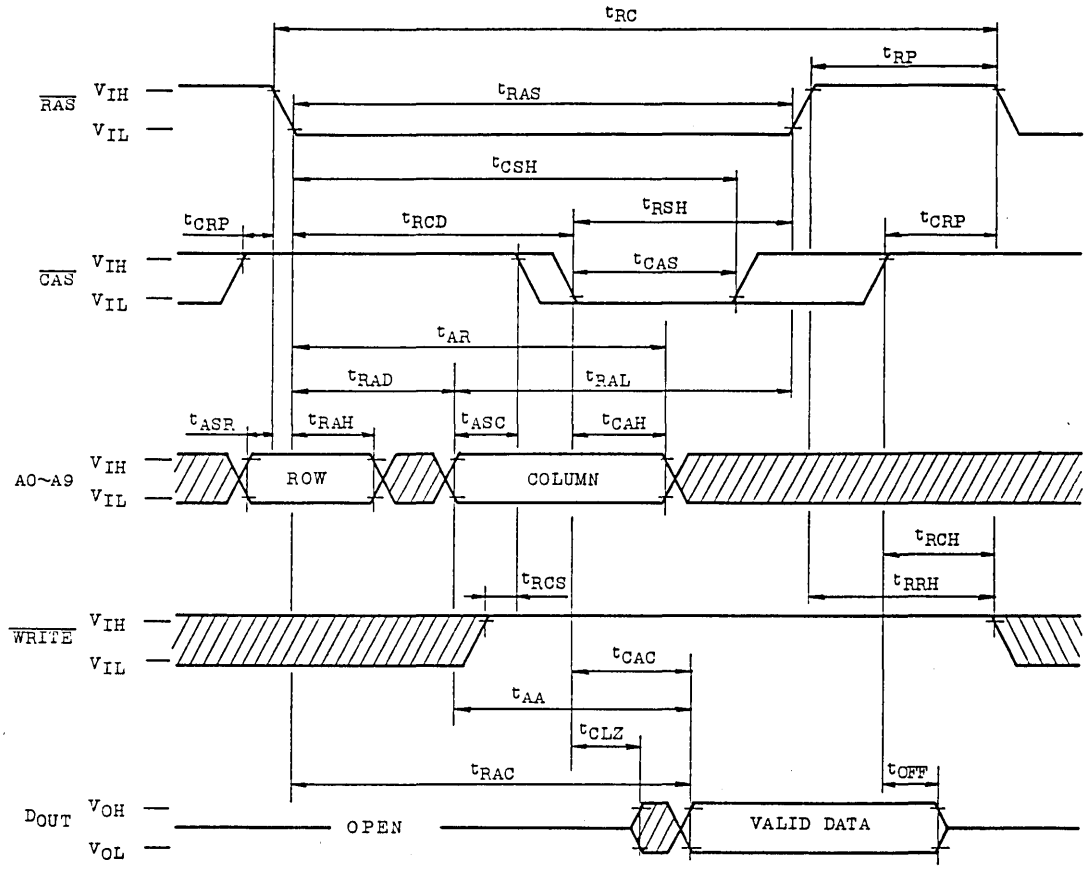
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	-	7	
C_O	Output Capacitance (D_{OUT})	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater then the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

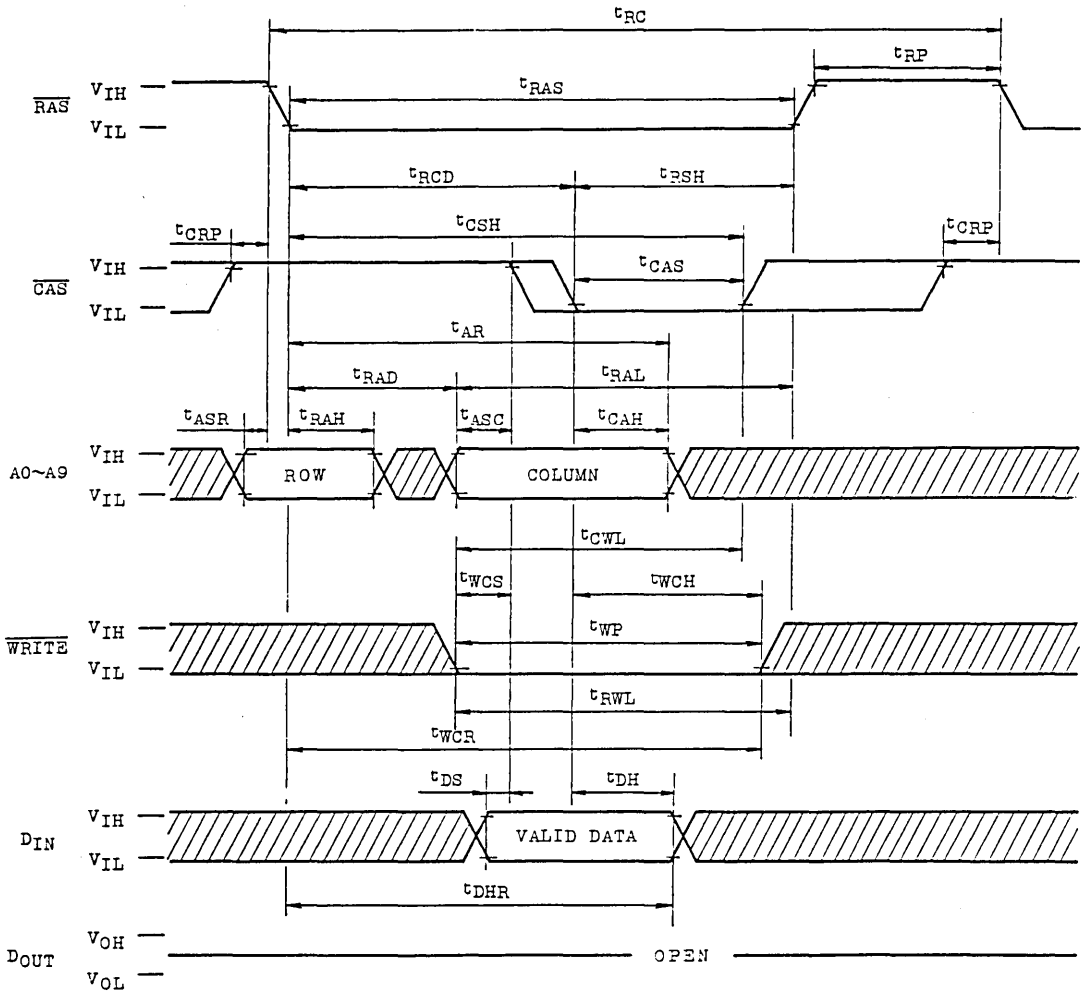
READ CYCLE



: "H" or "L"

NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

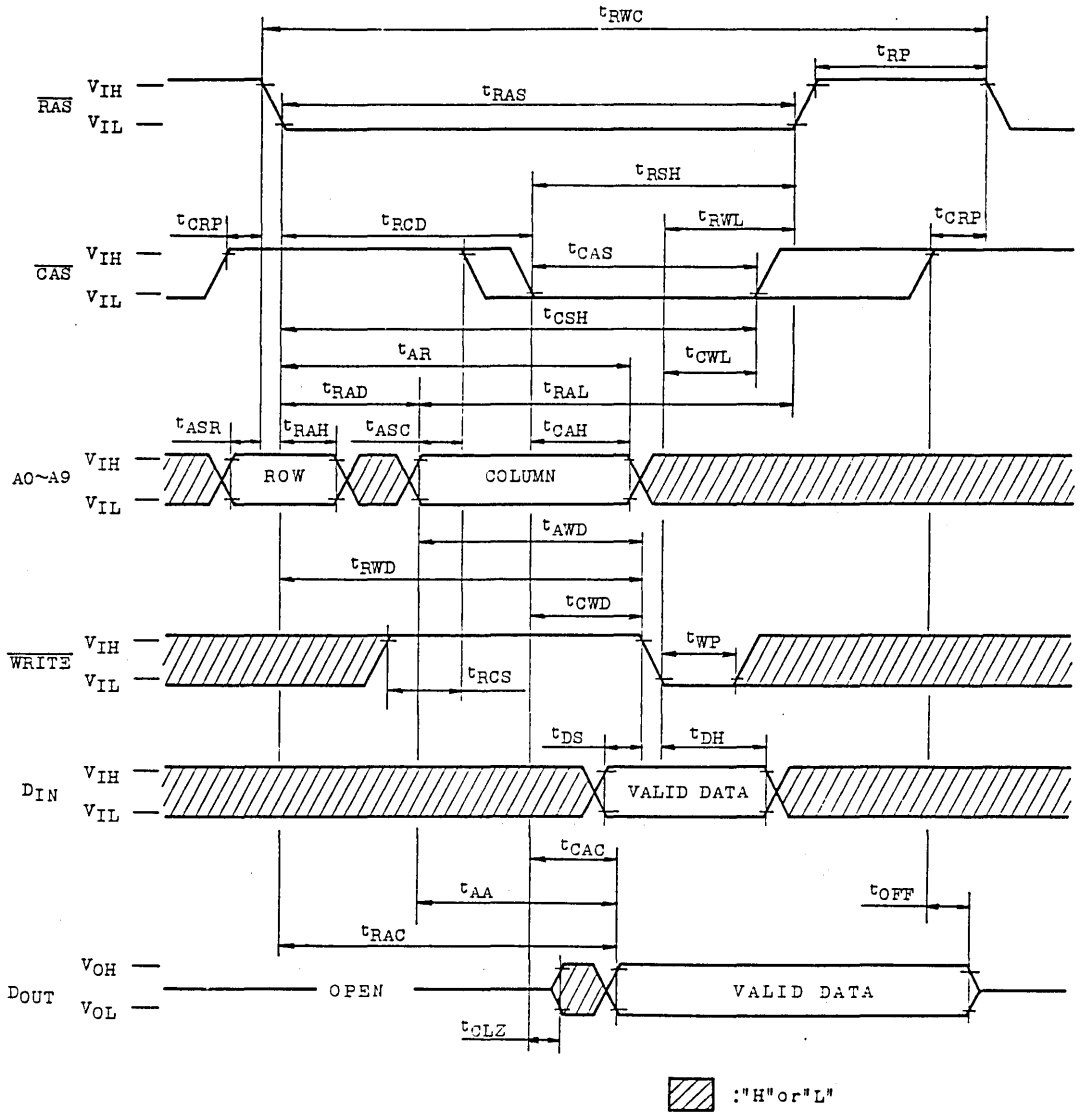
WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

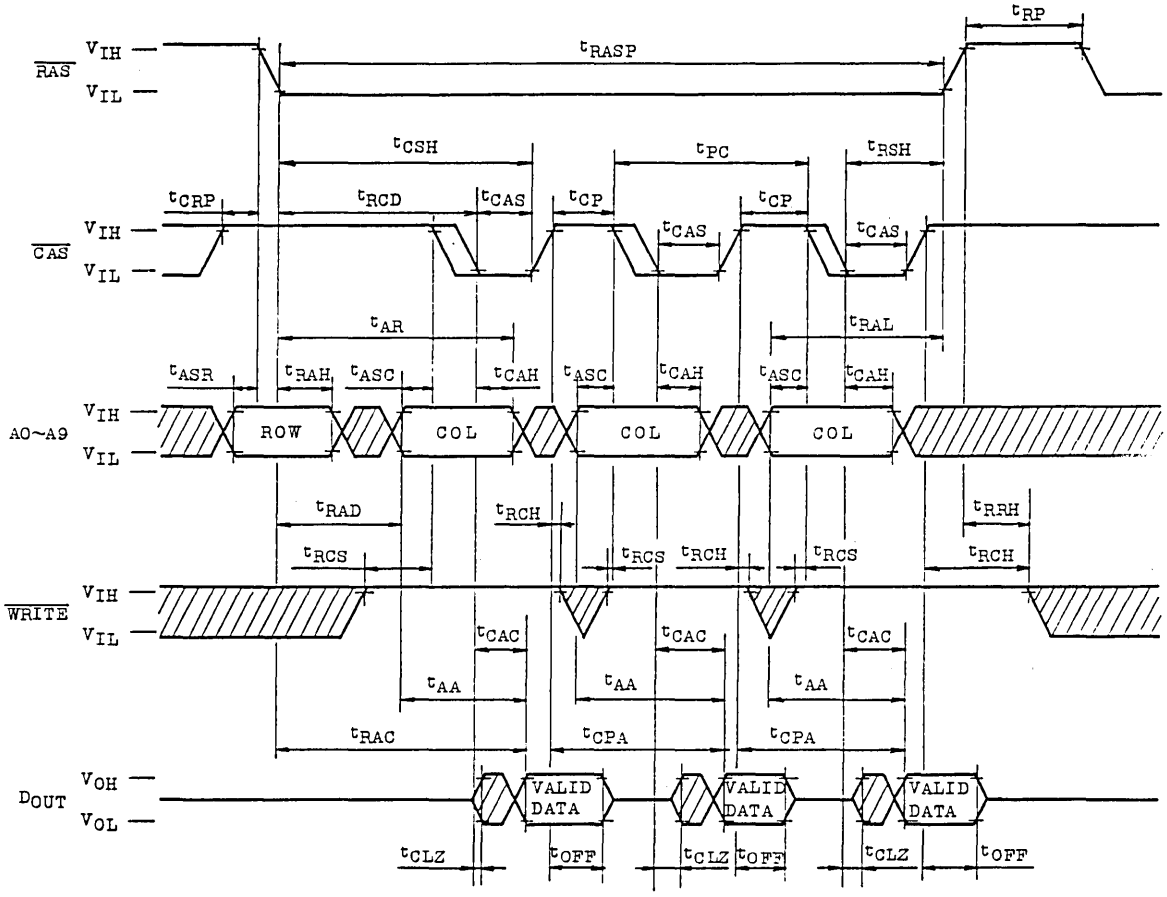
NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

READ-WRITE CYCLE



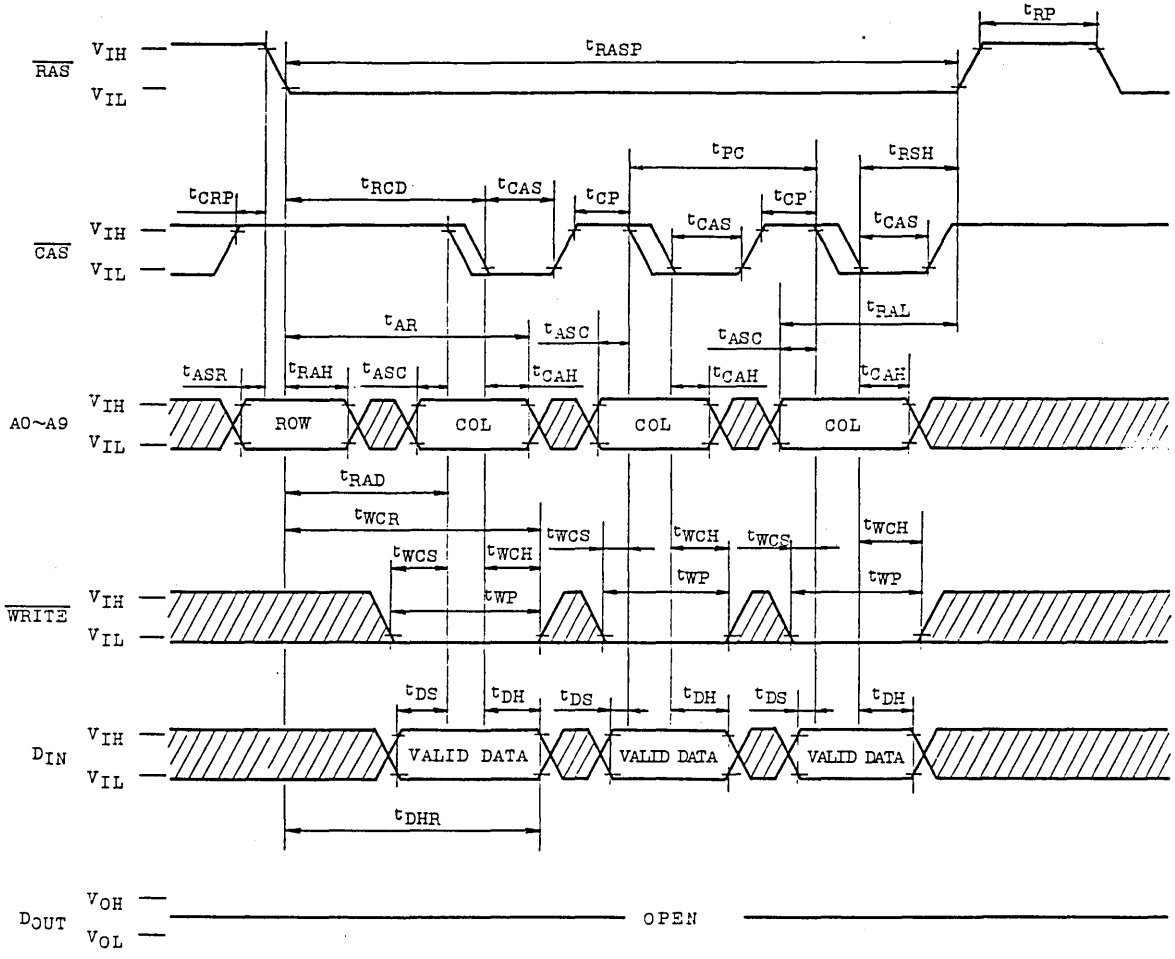
NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

FAST PAGE MODE READ CYCLE



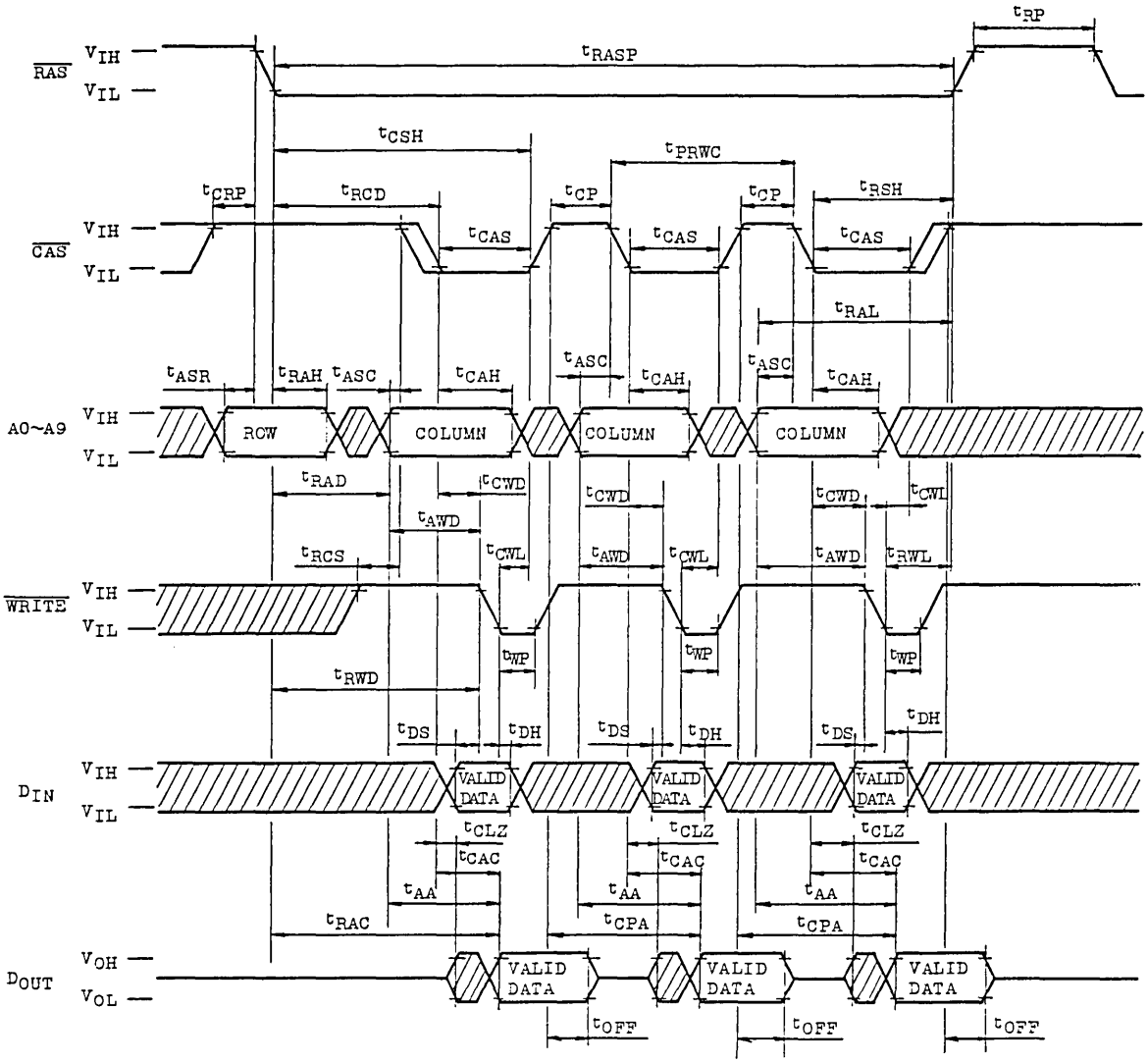
NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



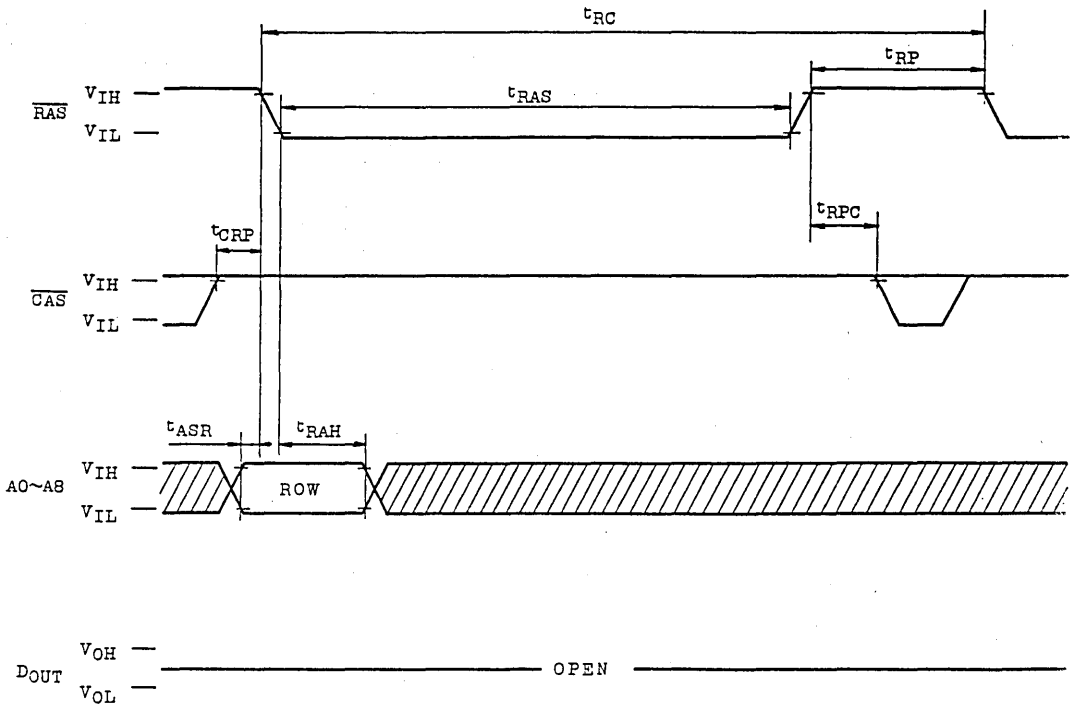
NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

FAST PAGE MODE READ-WRITE CYCLE



NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE

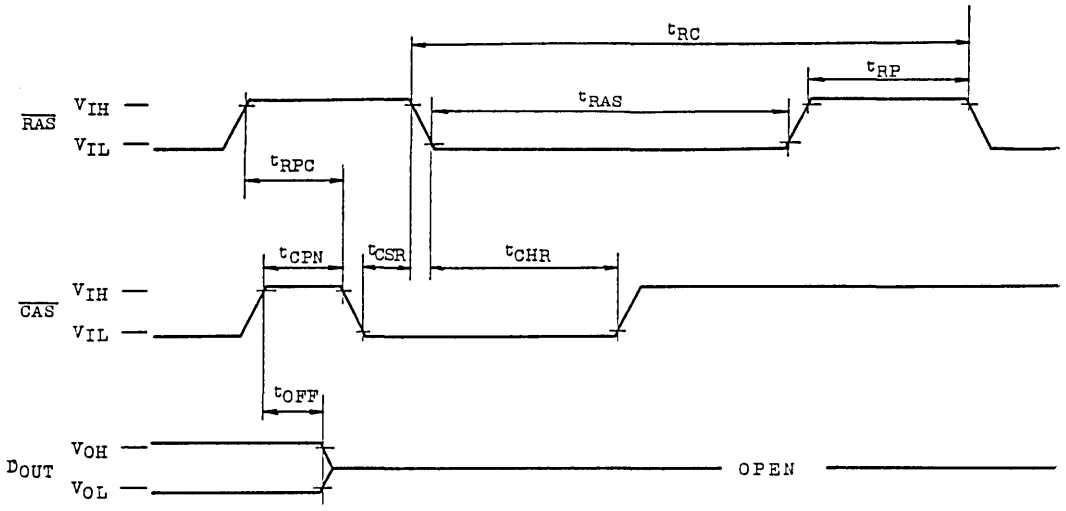


▨ : "H" or "L"

NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L"

"TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

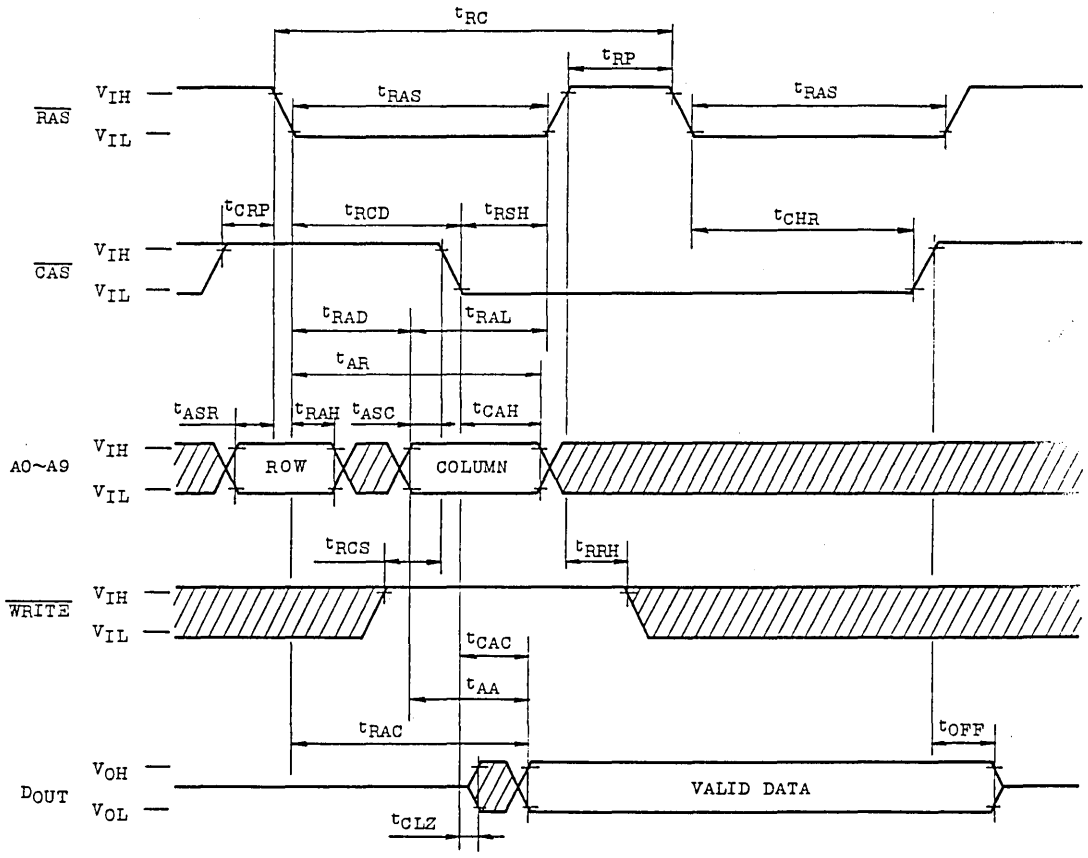


▨: "H" or "L"

NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

"TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

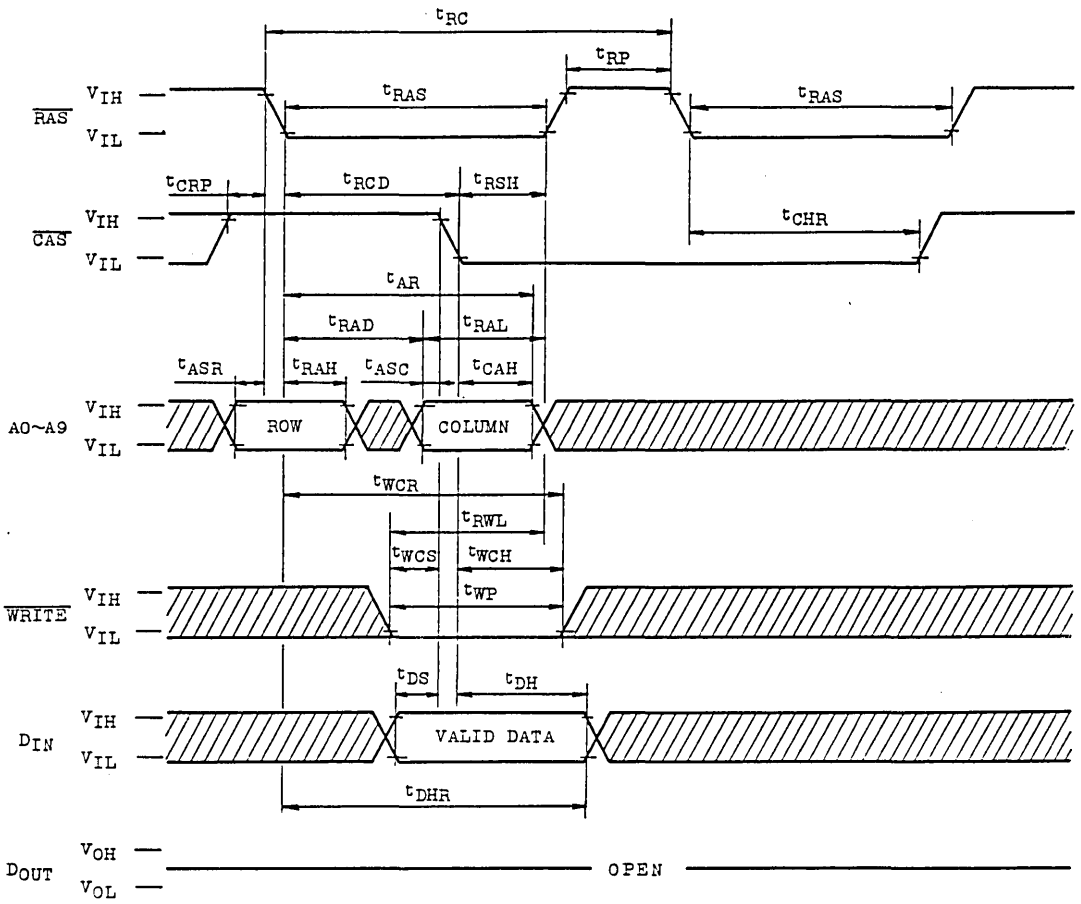
HIDDEN REFRESH CYCLE (READ)



▨ : "H" or "L"

NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

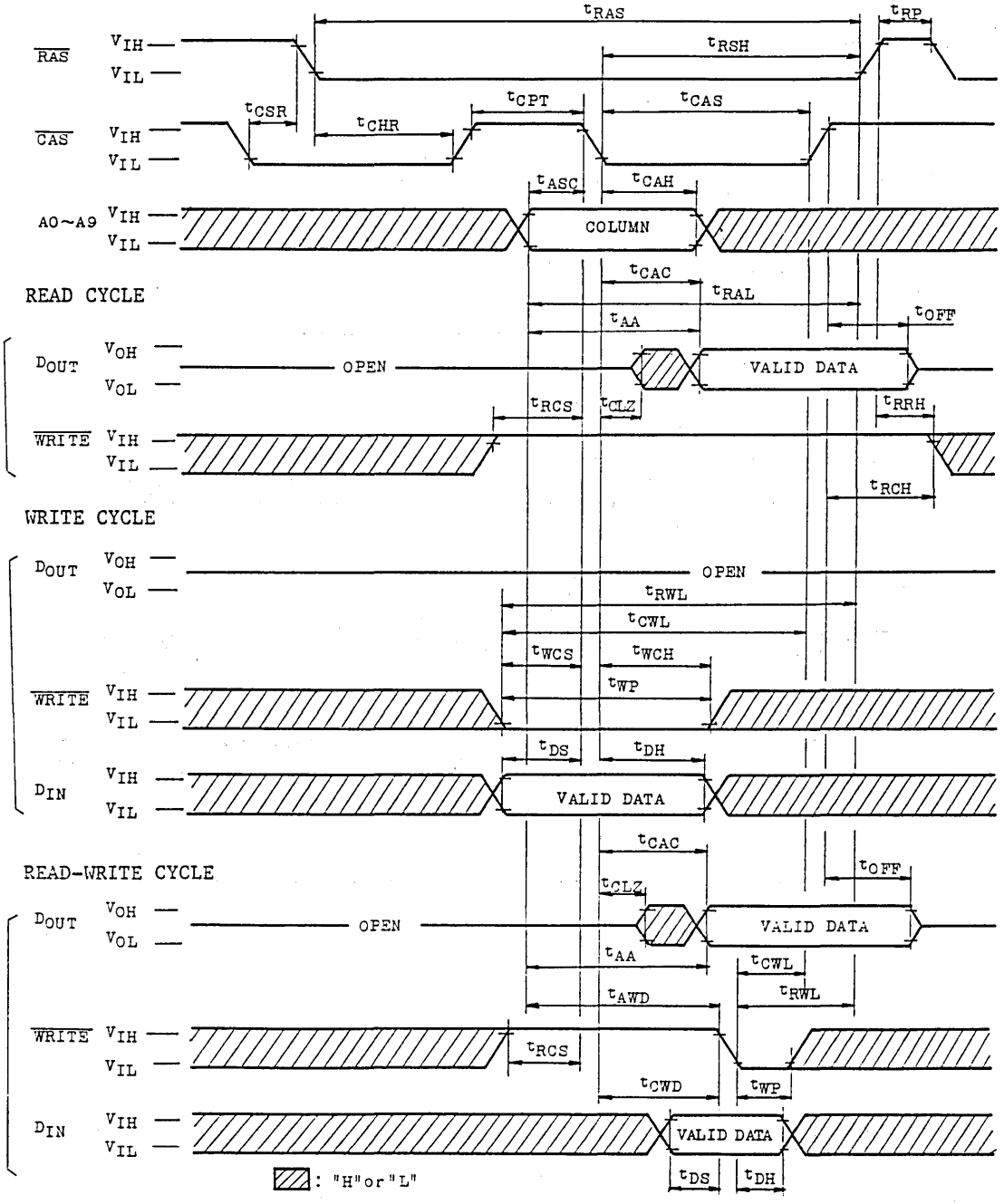
HIDDEN REFRESH CYCLE (WRITE)



▨ : "H" or "L"

NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE: "TF" pin should be connected V_{IL} level or open, if "Test Mode" is not used.

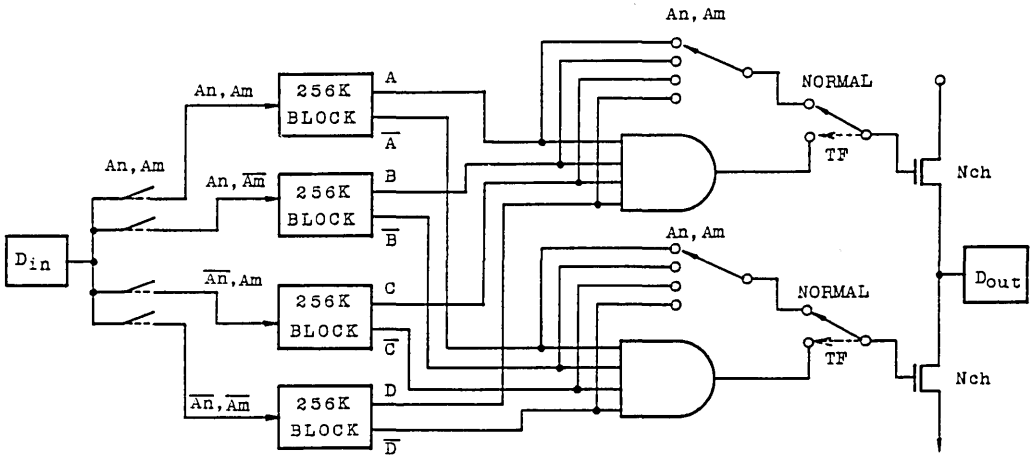
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- o For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- o For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = Low level or Hi-Z; Normal

Truth Table in Test mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
otherwise				Hi-Z

Fig. 1

DESCRIPTION OF THE TEST MODE FOR 1M DRAMS (CONTINUED)

The "Test Mode" function is enabled by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period (tTES and tTEH as shown in figure 2). It can be used while operating in any mode, including static column mode. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode".

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

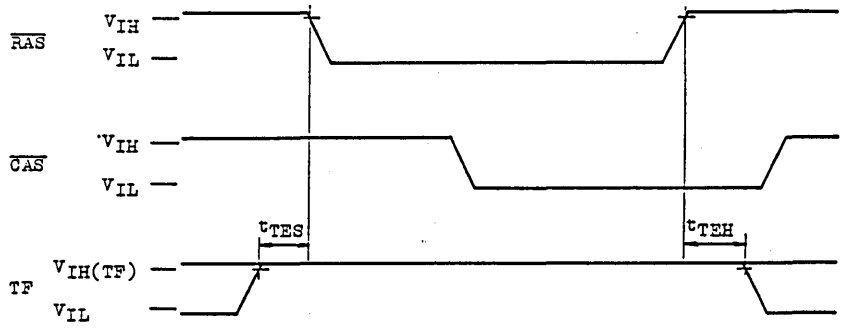
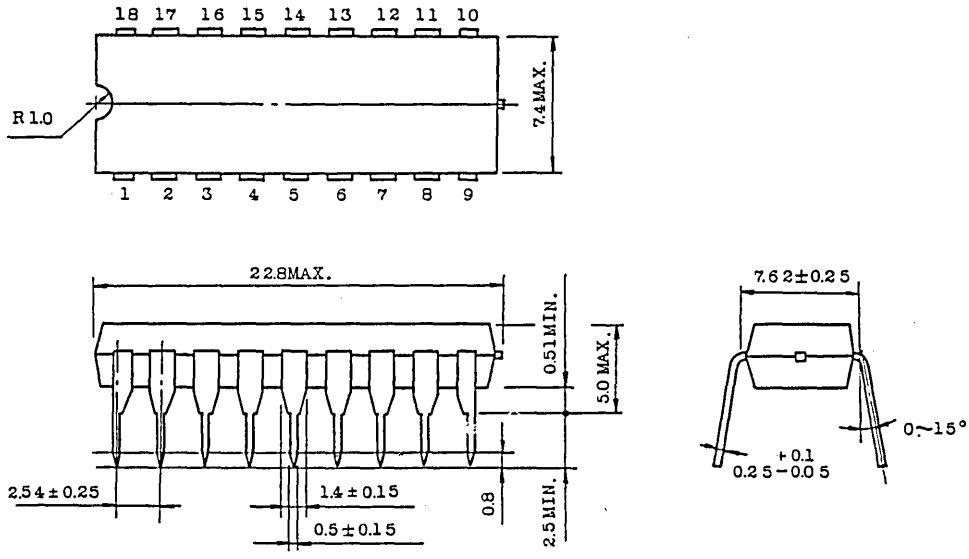


Fig.2 Test Mode Cycle

• Plastic DIP

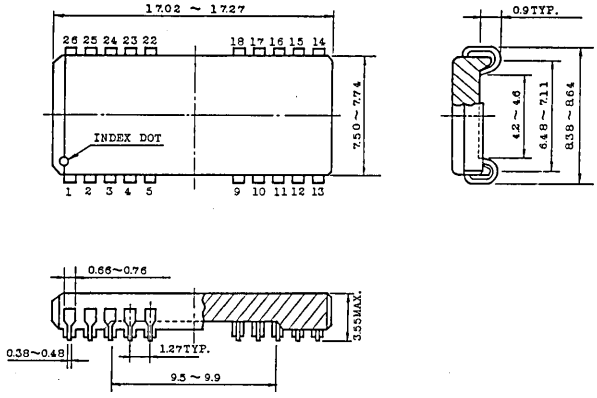
Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads.
All dimensions are in millimeters.

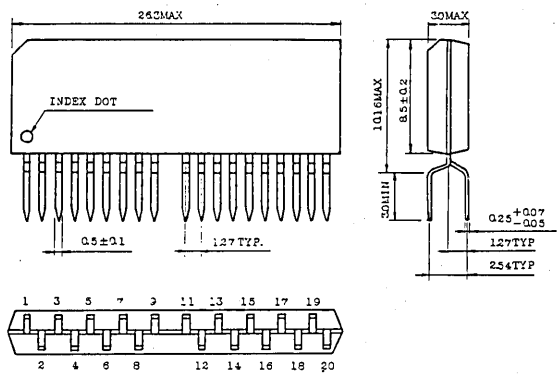
• Plastic SOJ

Unit in mm



• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 1 BIT DYNAMIC RAM
SILICON GATE CMOS

TC511001P/J/Z-85, TC511001P/J/Z-10
TC511001P/J/Z-12

DESCRIPTION

The TC511001P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511001P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511001P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The special feature of TC511001P/J/Z is nibble mode, allowing the user to serially access 4 bits of data at a high data rate. "Test Mode" function is implemented from Revision C.

FEATURES

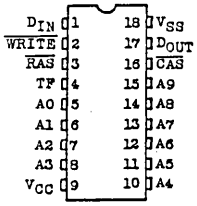
- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

		TC511001P/J/Z-85-10-12		
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns	40ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{NCAC}	Nibble Mode Access Time	20ns	20ns	25ns
t_{NC}	Nibble Mode Cycle Time	40ns	40ns	50ns

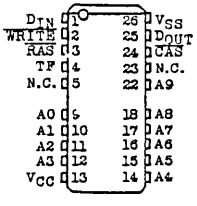
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power:
  385mW MAX. Operating (TC511001P/J/Z-85)
  330mW MAX. Operating (TC511001P/J/Z-10)
  275mW MAX. Operating (TC511001P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Nibble Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511001P
  Plastic SOJ: TC511001J
  Plastic ZIP: TC511001Z

PIN CONNECTION (TOP VIEW)

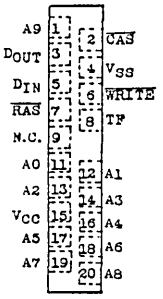
Plastic DIP



Plastic SOJ



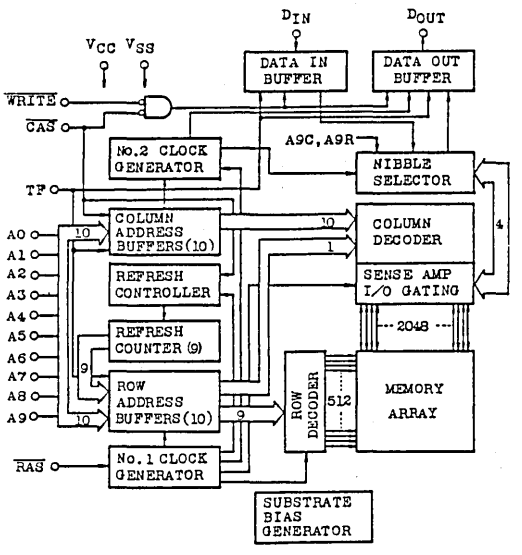
Plastic ZIP



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Test Mode Input Voltage	$V_{IN(TF)}$	-1 ∿ 10.5	V	1
Output Temperature	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC}+4.5	-	10.5	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5±10%, T_a=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511001P/J/Z-85 TC511001P/J/Z-10 TC511001P/J/Z-12	- - -	70 60 50	mA mA mA	3,4
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	3
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511001P/J/Z-85 TC511001P/J/Z-10 TC511001P/J/Z-12	- - -	70 60 50	mA mA mA	3
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{NC}=t_{NC} MIN.)	TC511001P/J/Z-85 TC511001P/J/Z-10 TC511001P/J/Z-12	- - -	50 40 30	mA mA mA	3,4
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFERSH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC511001P/J/Z-85 TC511001P/J/Z-10 TC511001P/J/Z-12	- - -	70 60 50	mA mA mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V≦V_{IN}≦6.5V, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≦ $V_{IN(TF)}$ ≦ 0.8V, All Other Pins Not Under Test = 0V)		-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ +5.5V)		-10	10	µA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC}+4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		-	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511001P/J/Z-85		TC511001P/J/Z-10		TC511001P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{RWC}	Read-Write Cycle Time	190	-	220	-	255	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	40	-	50	-	ns	
t_{NRMW}	Nibble Mode Read-Write Cycle Time	65	-	65	-	80	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	30	-	35	-	40	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{NCAC}	Nibble Mode Access Time	-	20	-	20	-	25	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	-	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	65	25	80	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511001P/J/Z-85		TC511001P/J/Z-10		TC511001P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time reference to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	30	-	35	-	40	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	100	-	120	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	45	-	50	-	60	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	-	20	-	25	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	20	-	25	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEH}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.

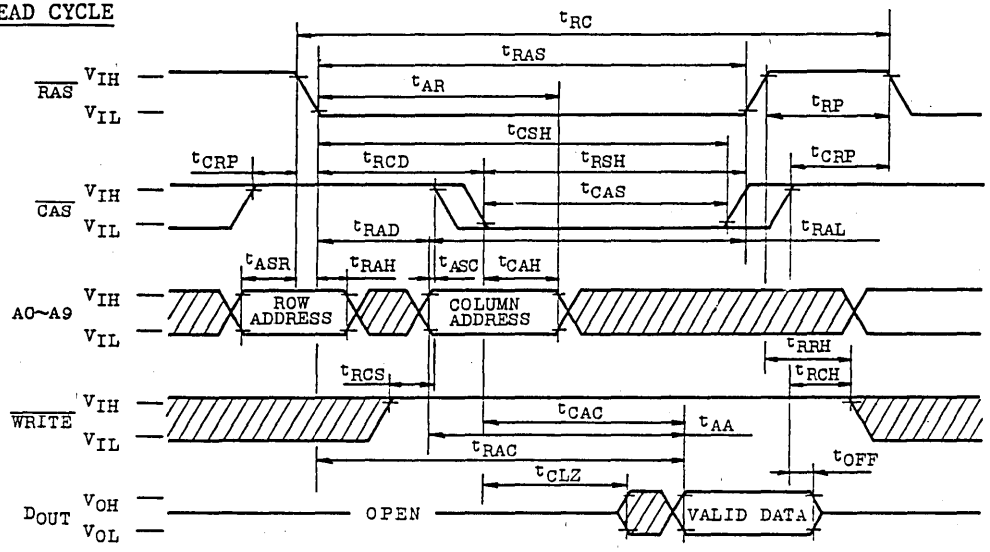
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

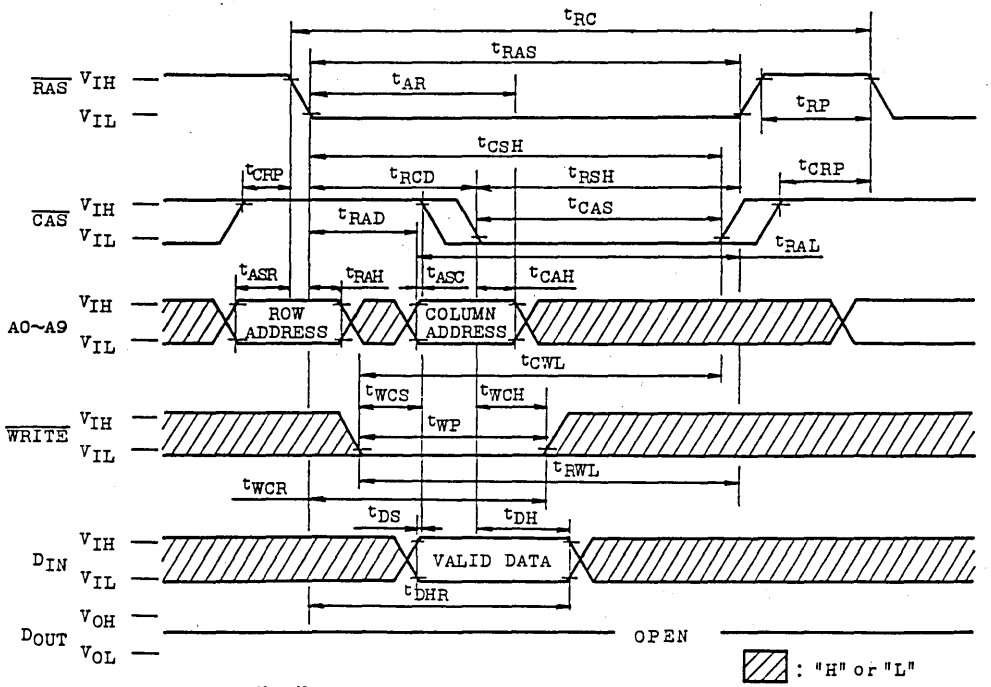
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

READ CYCLE

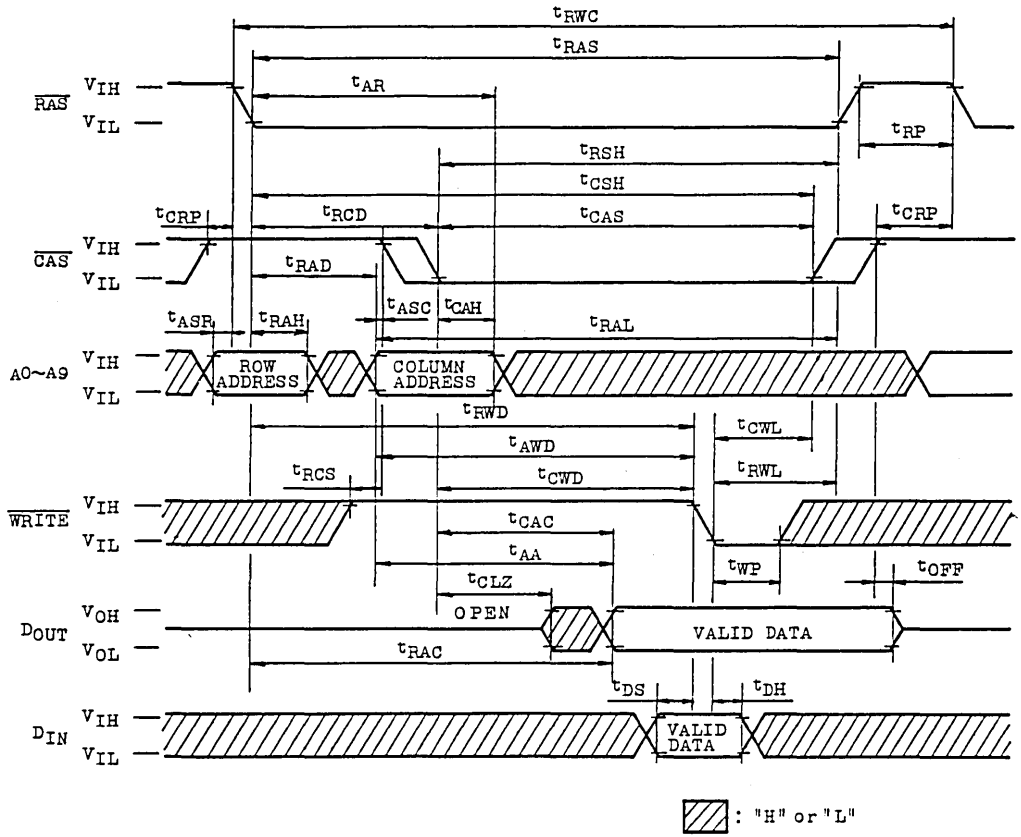


WRITE CYCLE (EARLY WRITE)



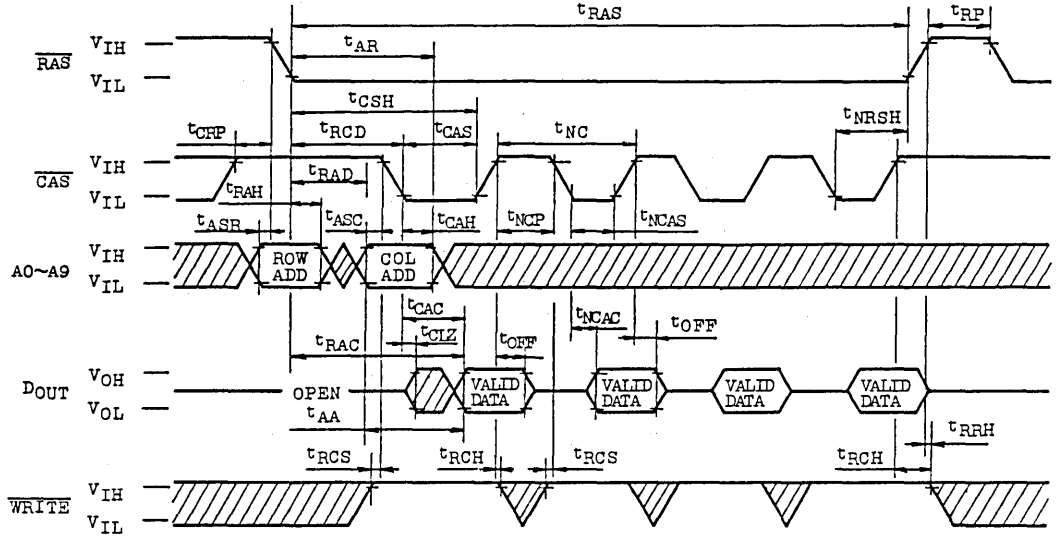
NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

READ-WRITE CYCLE

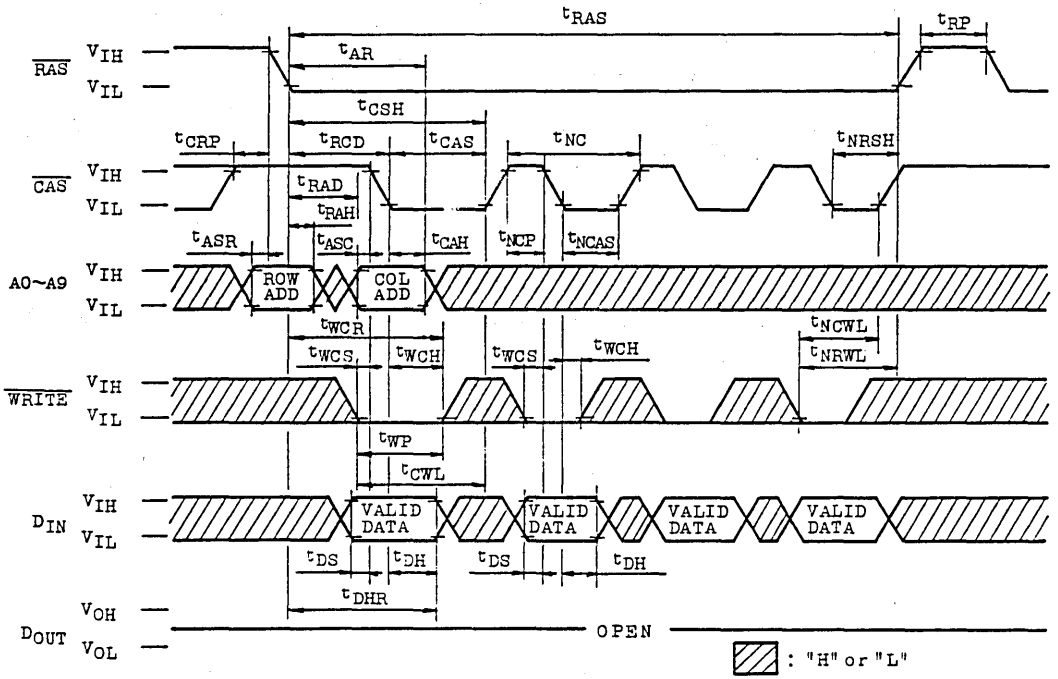


NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

NIBBLE MODE READ CYCLE

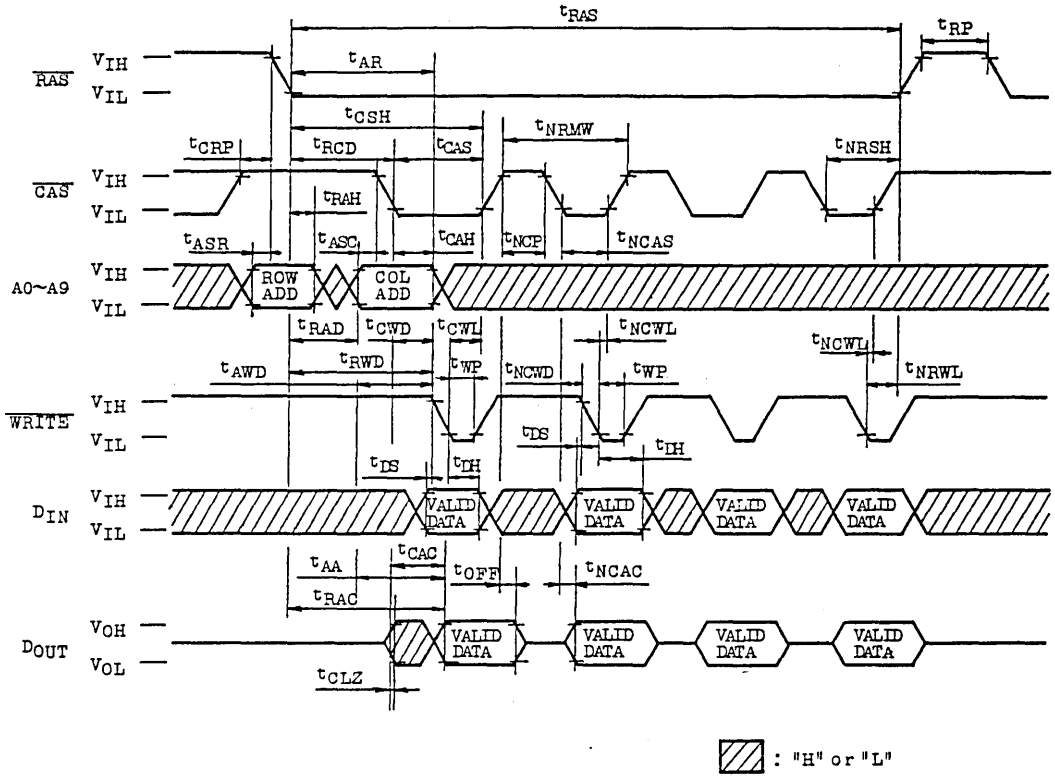


NIBBLE MODE WRITE CYCLE (EARLY WRITE)



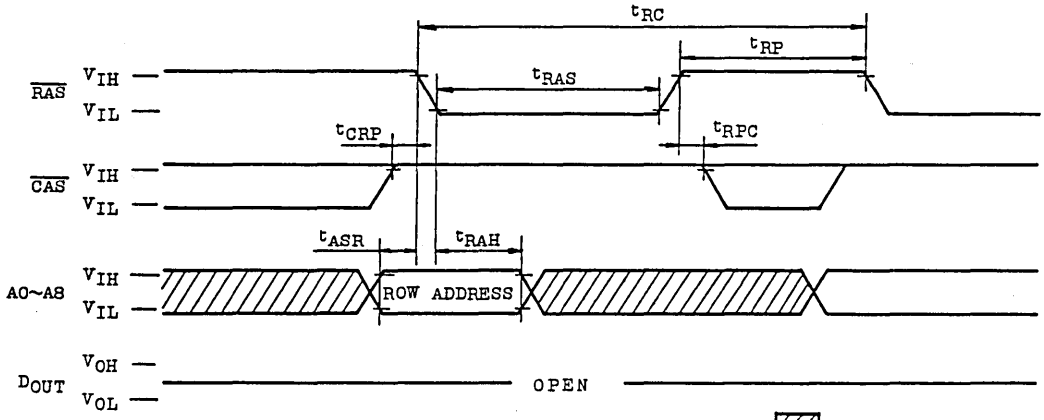
NOTE: "TF" pin should be connected to V_{IL} level or open.

NIBBLE MODE READ-WRITE CYCLE



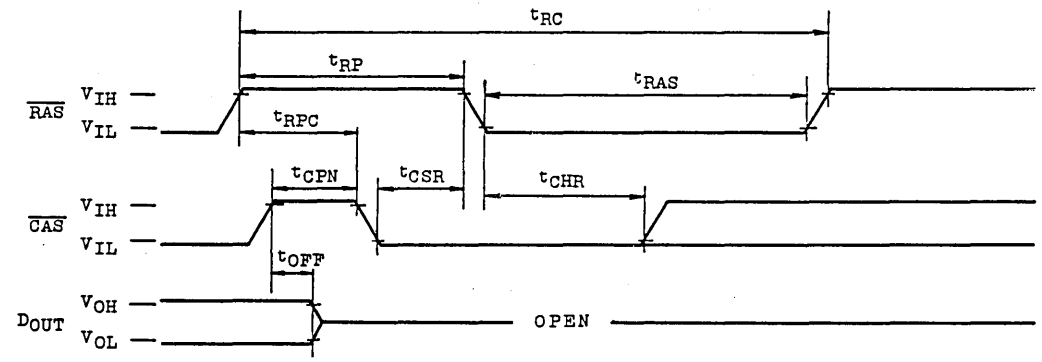
NOTE: "TF" pin should be connected to V_{IL} level or open.

$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L" ▨ : "H" or "L"

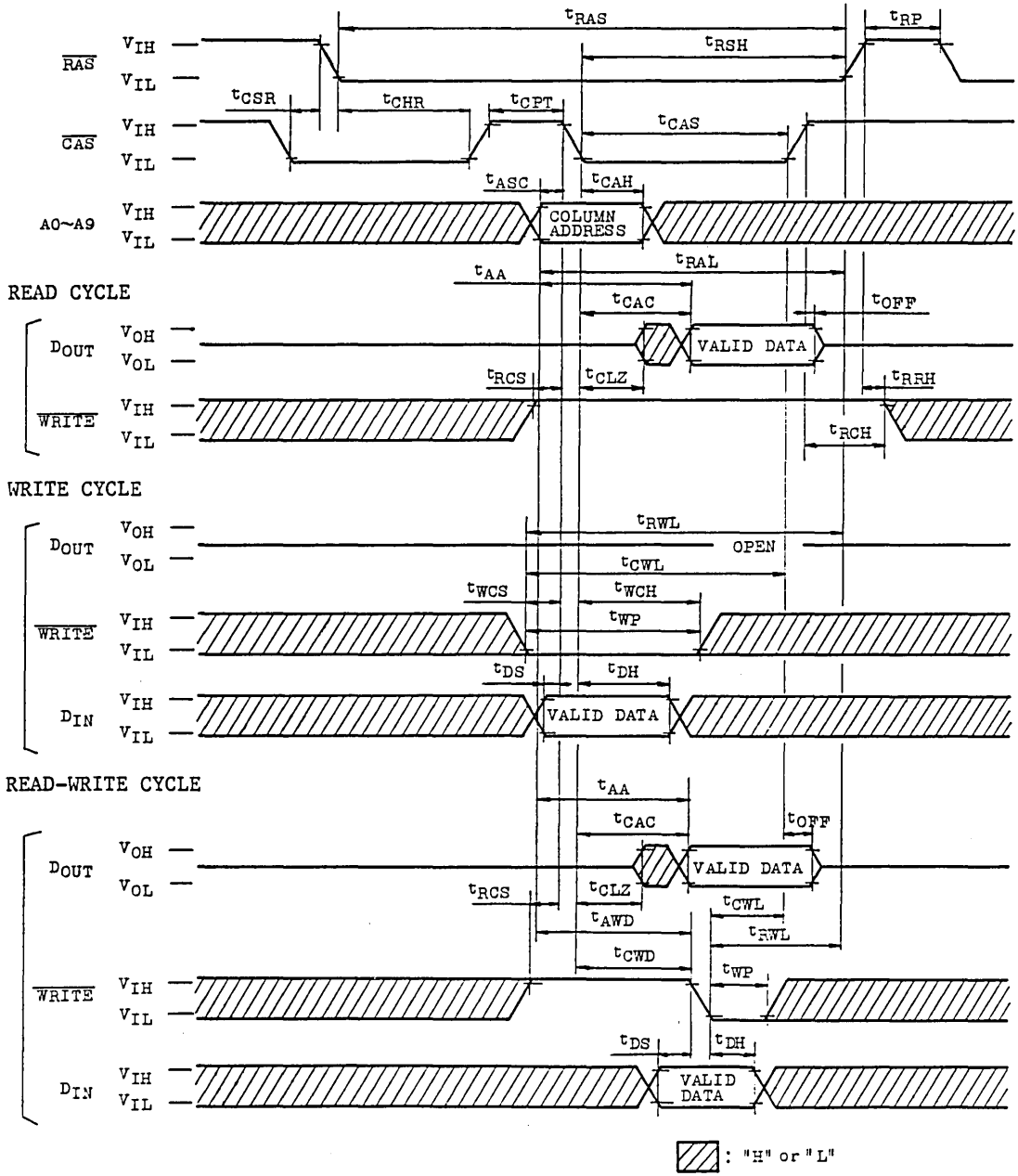
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

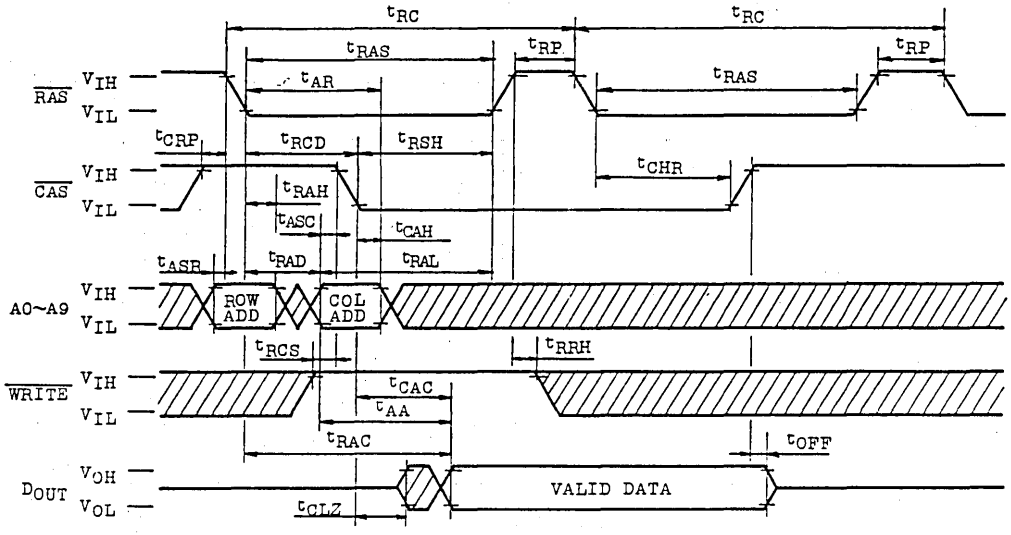
"TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

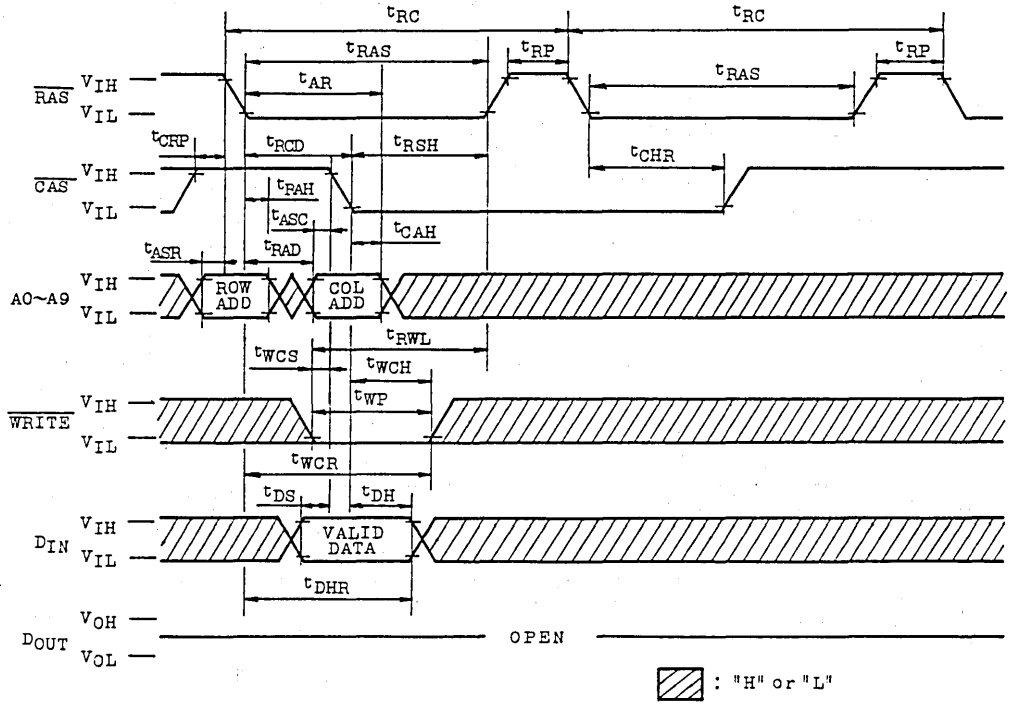


NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC511001P/J/Z are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In(D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low(active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made is negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

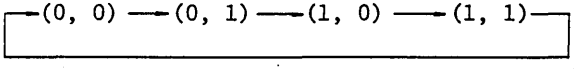
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active(low). Data read from the selected cell will be avialable at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC511001P/J/Z is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A9 determines the starting point of the circular 4 bits nibble. Row A9 and column A9 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A9 row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any conbinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

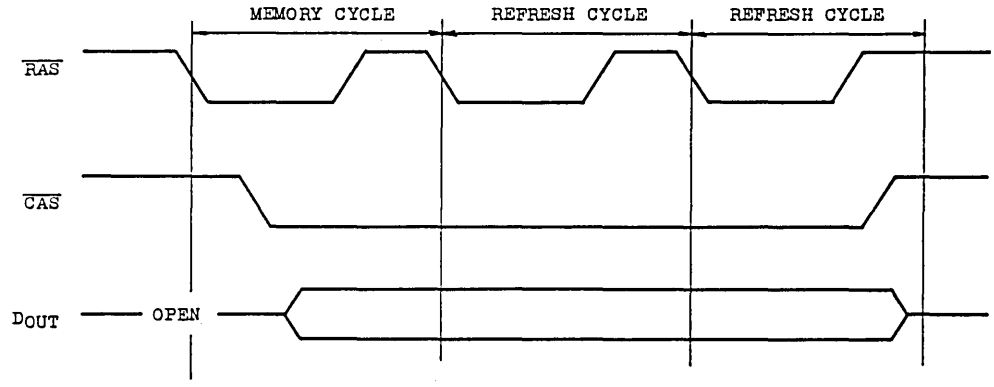
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0 ∿ A8) within each 8 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511001P/J/Z offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in perparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC511001P/J/Z is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511001P/J/Z can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one cartain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE).
Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST.
Repeat this operation 512 times.

⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

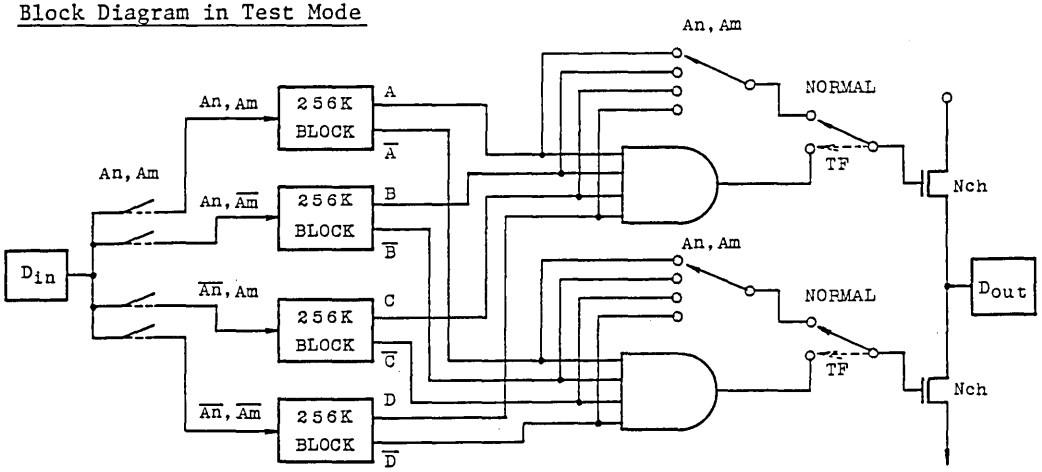
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin = Super Voltage; Test Mode

TF Pin = Low Level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

DESCRIPTION OF THE TEST MODE FOR 1M DRAMS (CONTINUED)

The "Test Mode" function is enabled by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period (tTES and tTEH as shown in figure 2) It can be used while operating in any mode, including static column mode. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode"

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

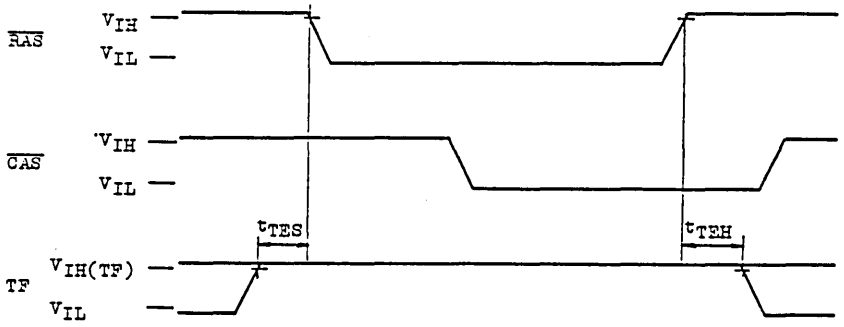
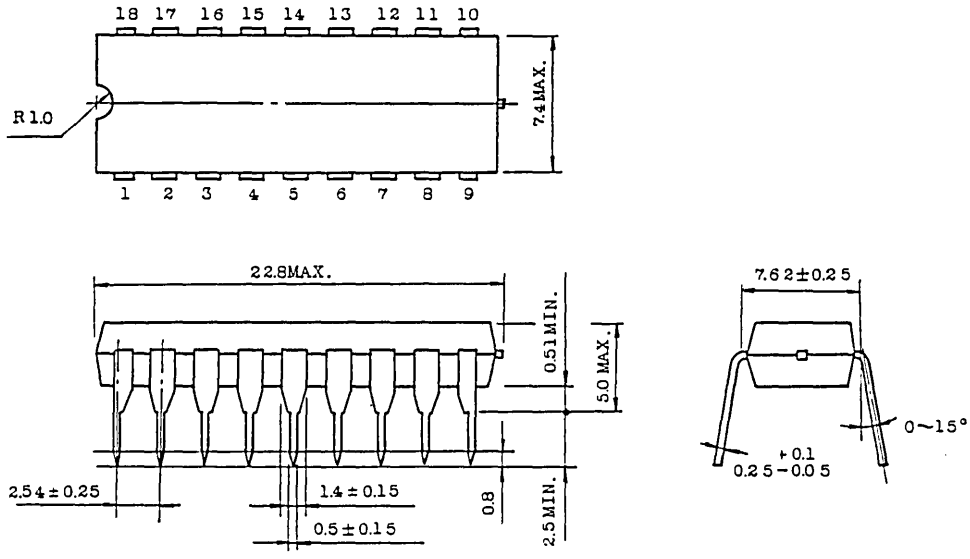


Fig.2 Test Mode Cycle

OUTLINE DRAWINGS

• Plastic DIP

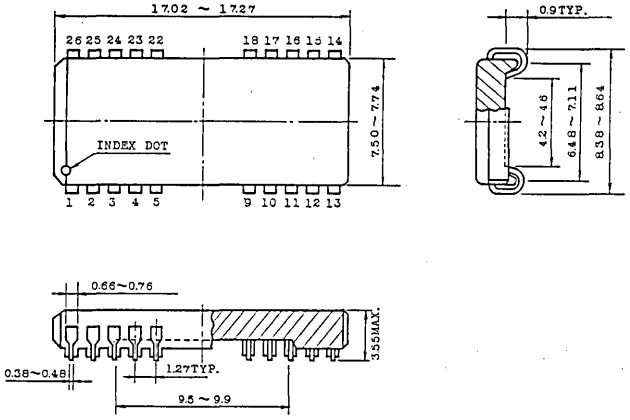
Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads.
All dimensions are in millimeters.

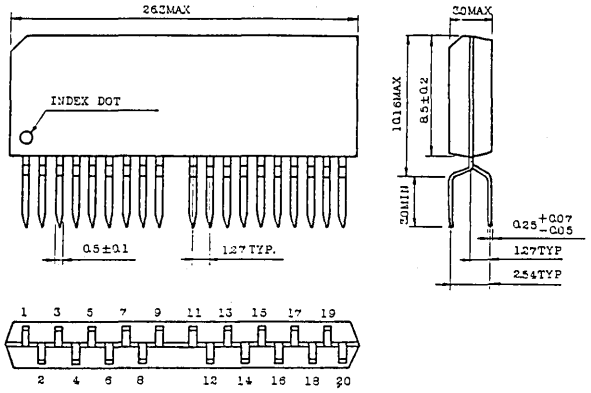
Plastic SOJ

Unit in mm



Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 1 BIT DYNAMIC RAM
SILICON GATE CMOS

TC511002P/J/Z-85, TC511002P/J/Z-10
TC511002P/J/Z-12

DESCRIPTION

The TC511002P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511002P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511002P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. "Test Mode" function is implemented from Revision C.

FEATURES

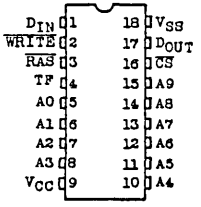
- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

		TC511002P/J/Z-85-10-12		
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	50ns	55ns	65ns

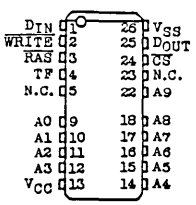
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  385mW MAX. Operating (TC511002P/J/Z-85)
  330mW MAX. Operating (TC511002P/J/Z-10)
  275mW MAX. Operating (TC511002P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability.
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511002P
  Plastic SOJ: TC511002J
  Plastic ZIP: TC511002Z

PIN CONNECTION (TOP VIEW)

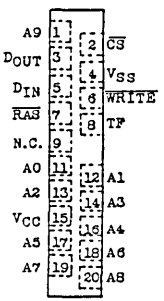
Plastic DIP



Plastic SOJ



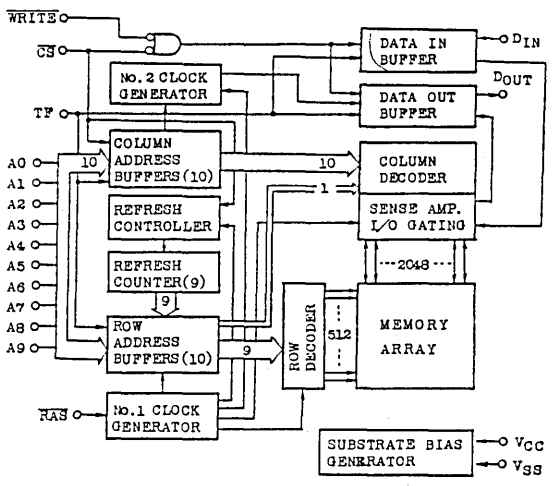
Plastic ZIP



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CS}$	Chip Select Input
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	-1 ∿ 10.5	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC}+4.5	-	10.5	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5±10%, T_a=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511002P/J/Z-85	-	70	mA	3,4
		TC511002P/J/Z-10	-	60	mA	
		TC511002P/J/Z-12	-	50	mA	
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC}, MIN.)	TC511002P/J/Z-85	-	70	mA	3
		TC511002P/J/Z-10	-	60	mA	
		TC511002P/J/Z-12	-	50	mA	
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	TC511002P/J/Z-85	-	50	mA	3,4
		TC511002P/J/Z-10	-	40	mA	
		TC511002P/J/Z-12	-	30	mA	
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC511002P/J/Z-85	-	70	mA	3
		TC511002P/J/Z-10	-	60	mA	
		TC511002P/J/Z-12	-	50	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V≦V_{IH}≦6.5V, All Other Pins Not Under Test = 0V)		-10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V≦$V_{IN(TF)}$≦0.8V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V≦V_{OUT}≦+5.5V)		-10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC}+4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		-	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511002P/J/Z-85		TC511002P/J/Z-10		TC511002P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{RWC}	Read-Write Cycle Time	190	-	220	-	255	-	ns	
t_{SC}	Static Column Mode Cycle Time	50	-	55	-	65	-	ns	
t_{SRWC}	Static Column Mode Read Write Cycle Time	90	-	100	-	120	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{ALW}	Access Time from Last Write	-	85	-	95	-	115	ns	8,15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	30	-	30	-	35	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	0	-	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	100	-	115	-	140	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (continued)

SYMBOL	PARAMETER	TC511002P/J/Z-85		TC511002P/J/Z-10		TC511002P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	10	-	10	-	15	-	ns	16
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	25	-	30	-	ns	
t_{LWAD}	Last Write to Column Address Delay Time	25	40	25	45	30	55	ns	15
t_{AHLW}	Last Write to Column Address Hold Time	85	-	95	-	115	-	ns	
t_{RCS}	Read Command Set-Up Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{WI}	Write Command Inactive Time	10	-	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WS}	Write Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	25	-	25	-	30	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	85	-	100	-	120	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	45	-	50	-	60	-	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEH}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	

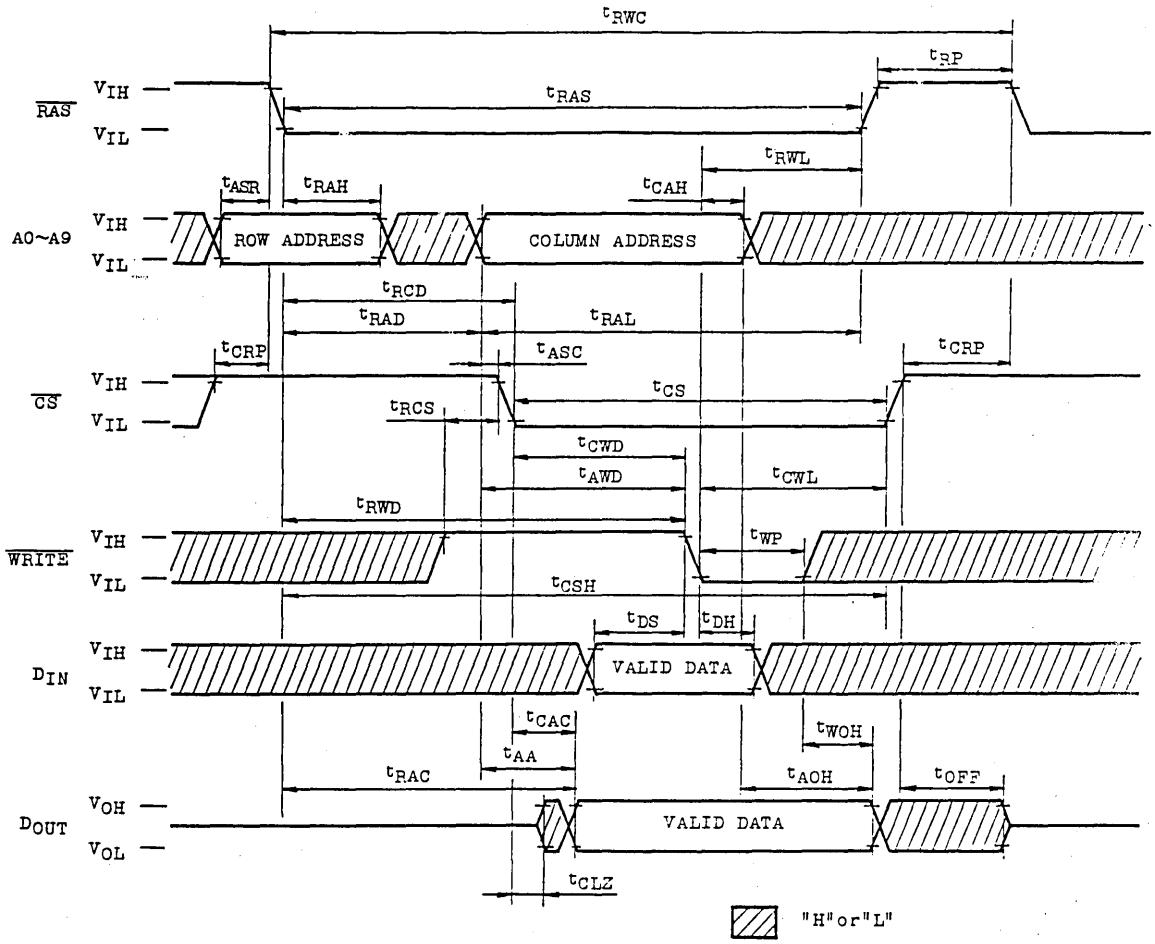
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, TF)	-	7	
C_O	Output Capacitance (D_{OUT})	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
   In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ intialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
12. t_{WS}, t_{WH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electeical characteristics only. If $t_{WS} \geq t_{WS}$(min.) and $t_{WH} \geq t_{WH}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither or the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specilied t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD} (max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

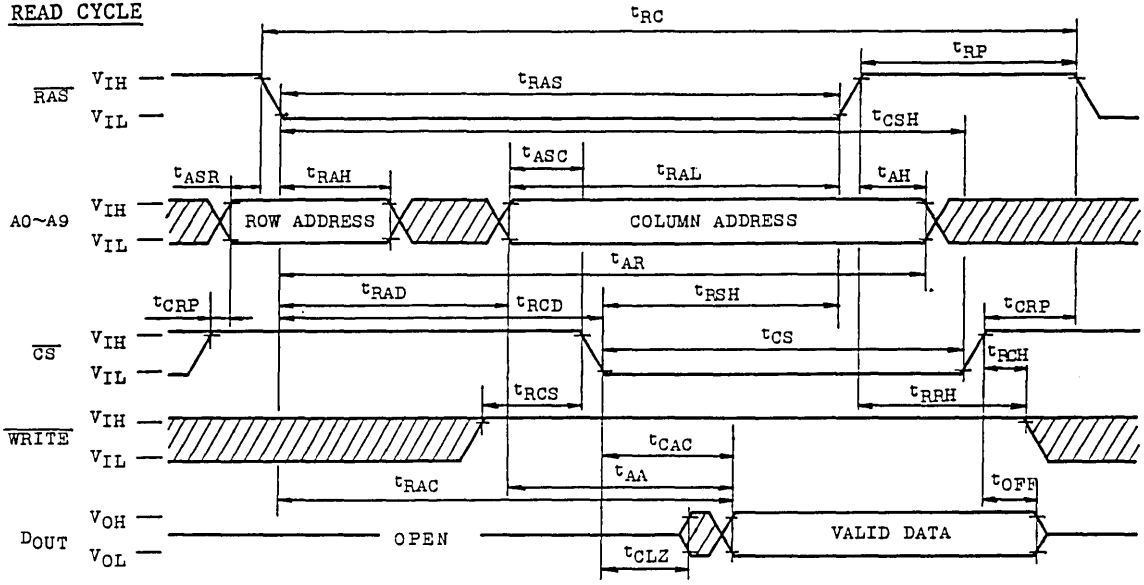
READ-WRITE CYCLE



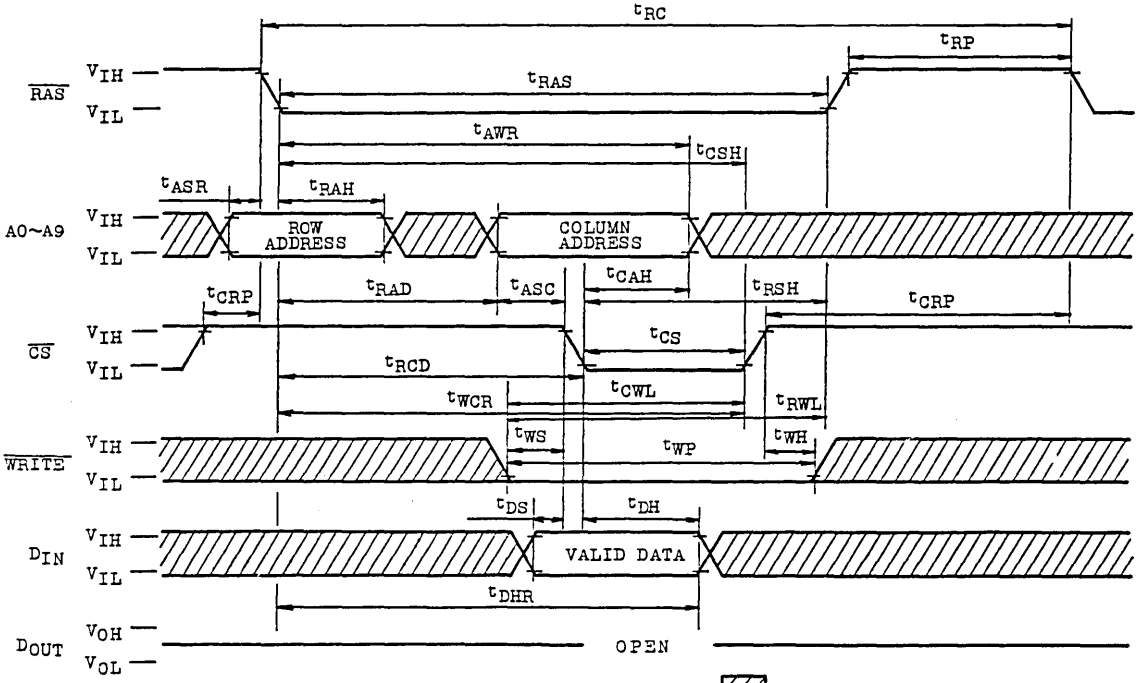
NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

TIMING WAVEFORMS

READ CYCLE

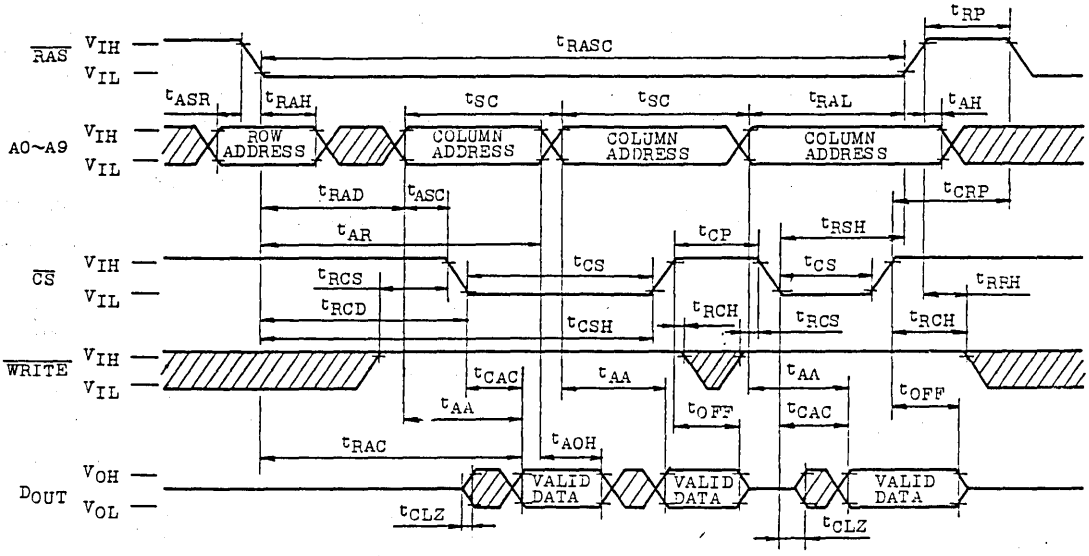


WRITE CYCLE (EARLY WRITE)

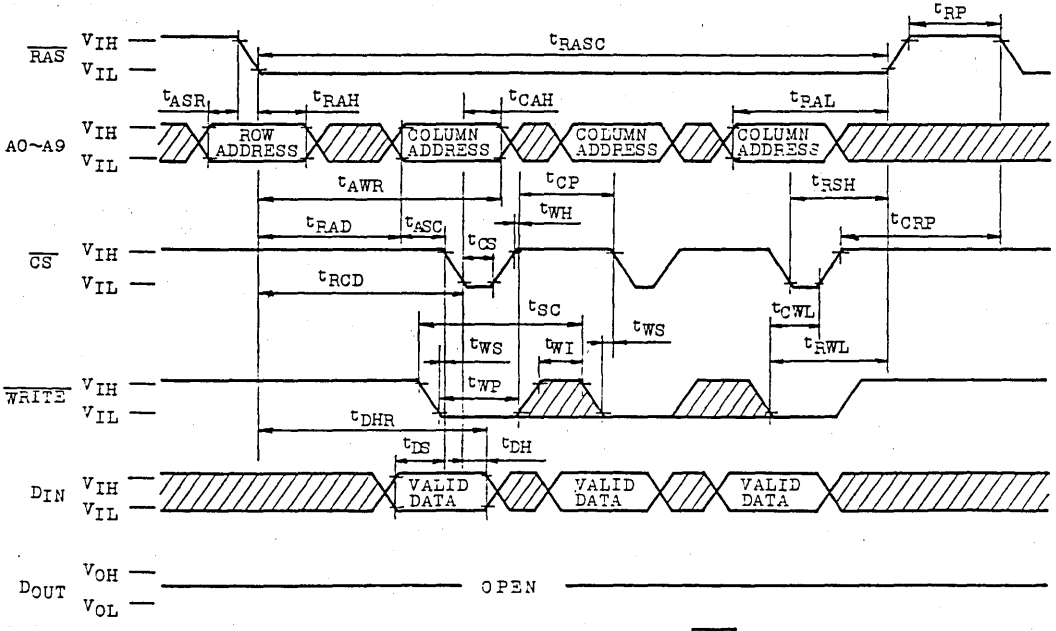


NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ CYCLE

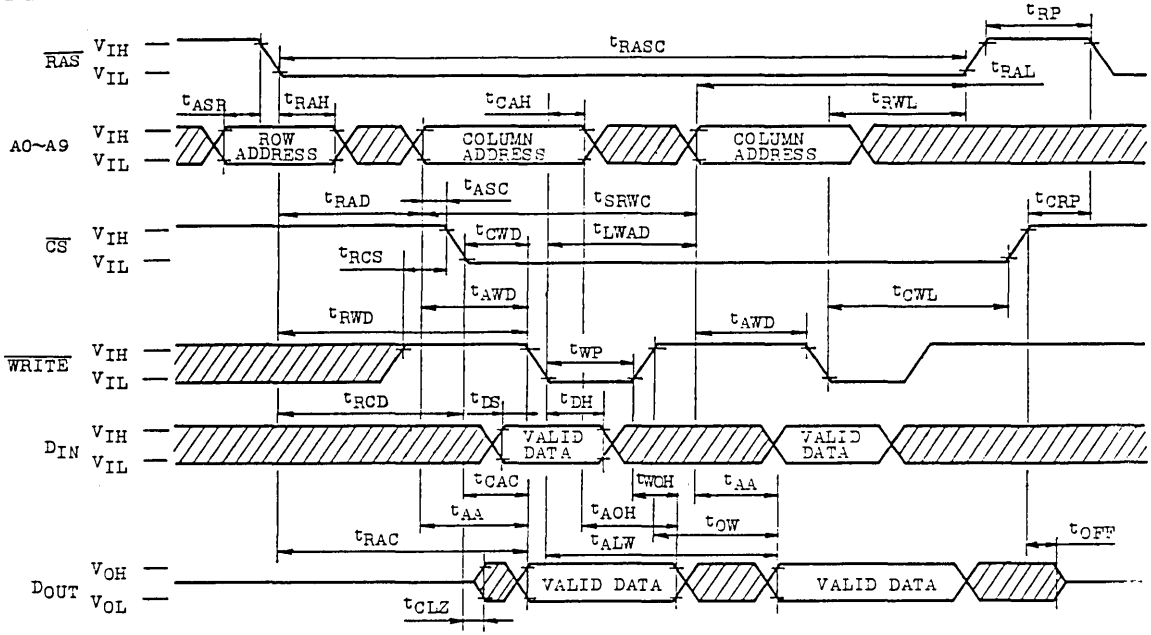


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

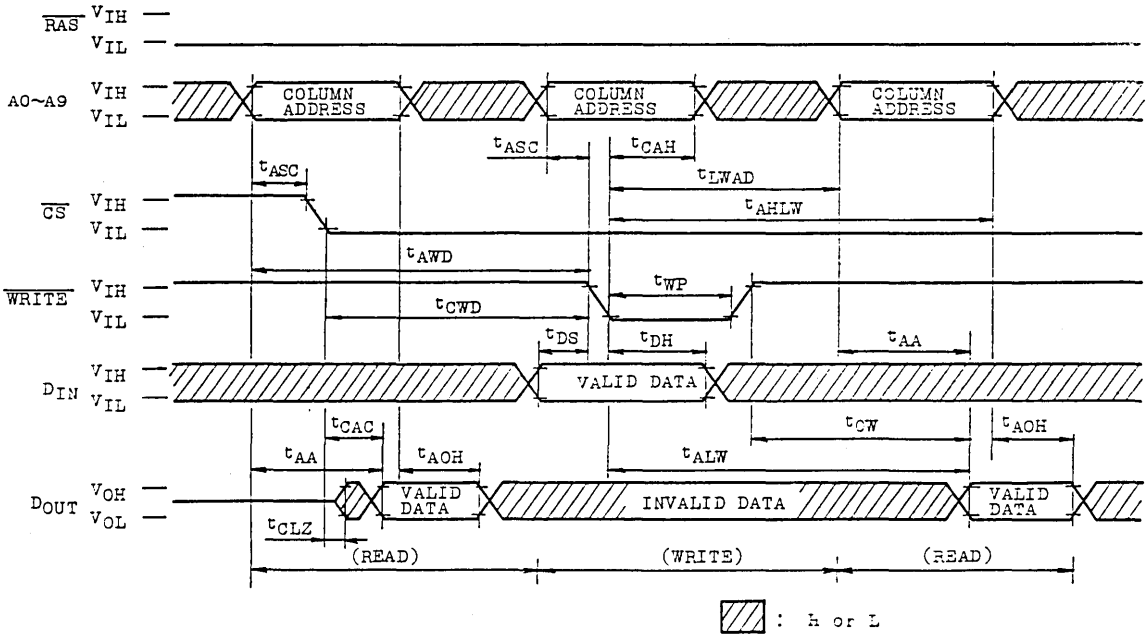


NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ-WRITE CYCLE

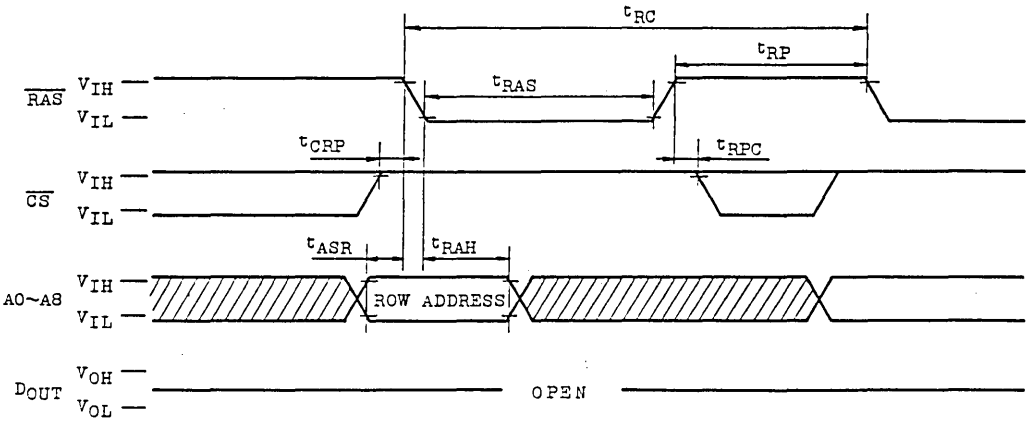


STATIC COLUMN MODE READ/WRITE MIXED CYCLE



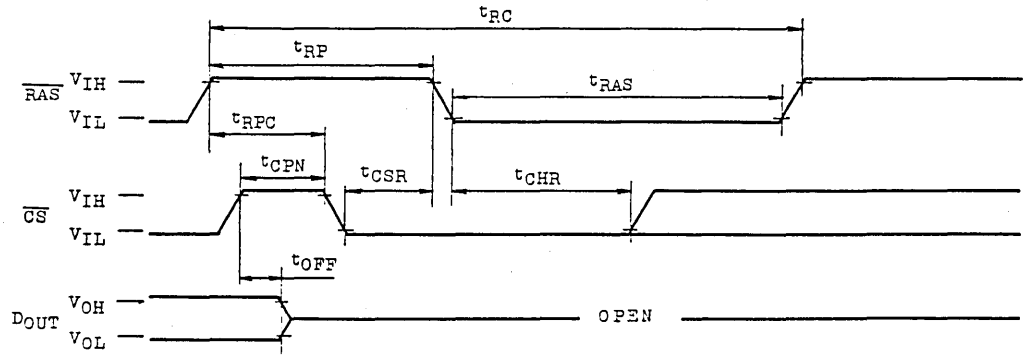
NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L" ▨ : "H"or"L"

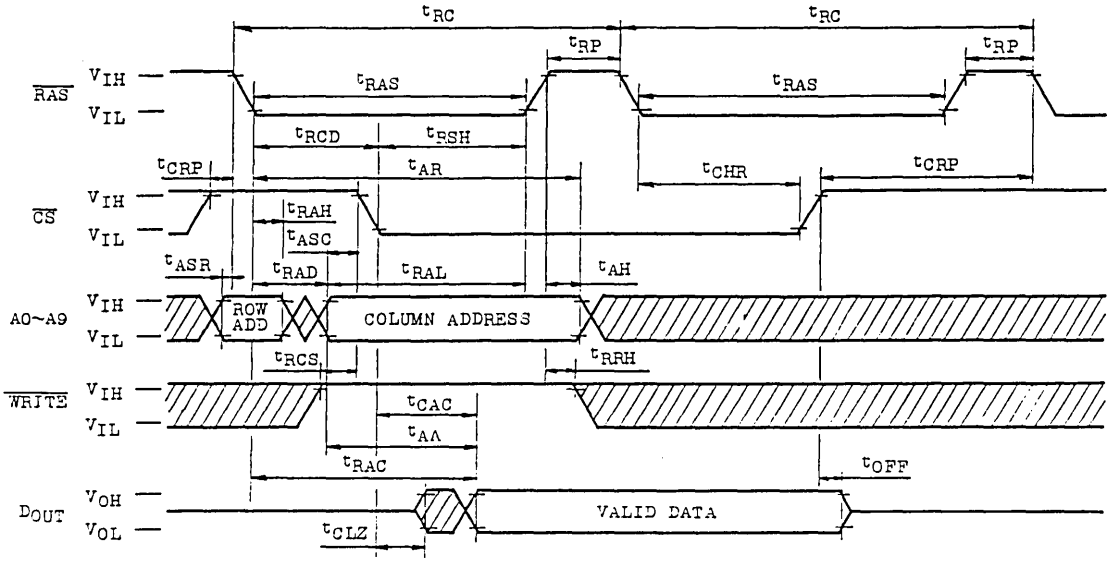
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



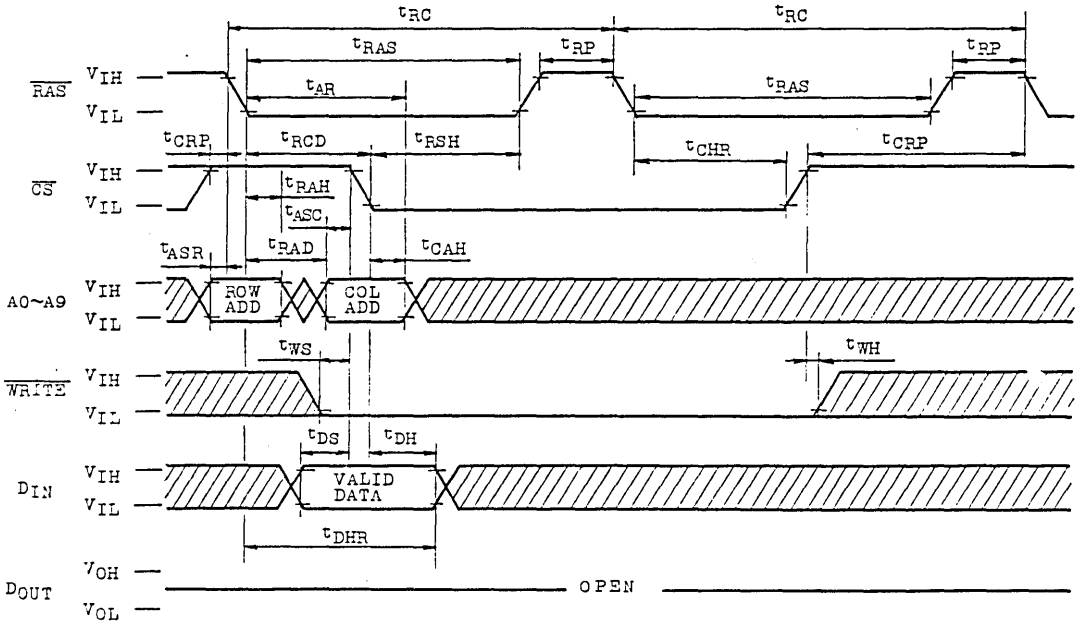
NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

"TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)

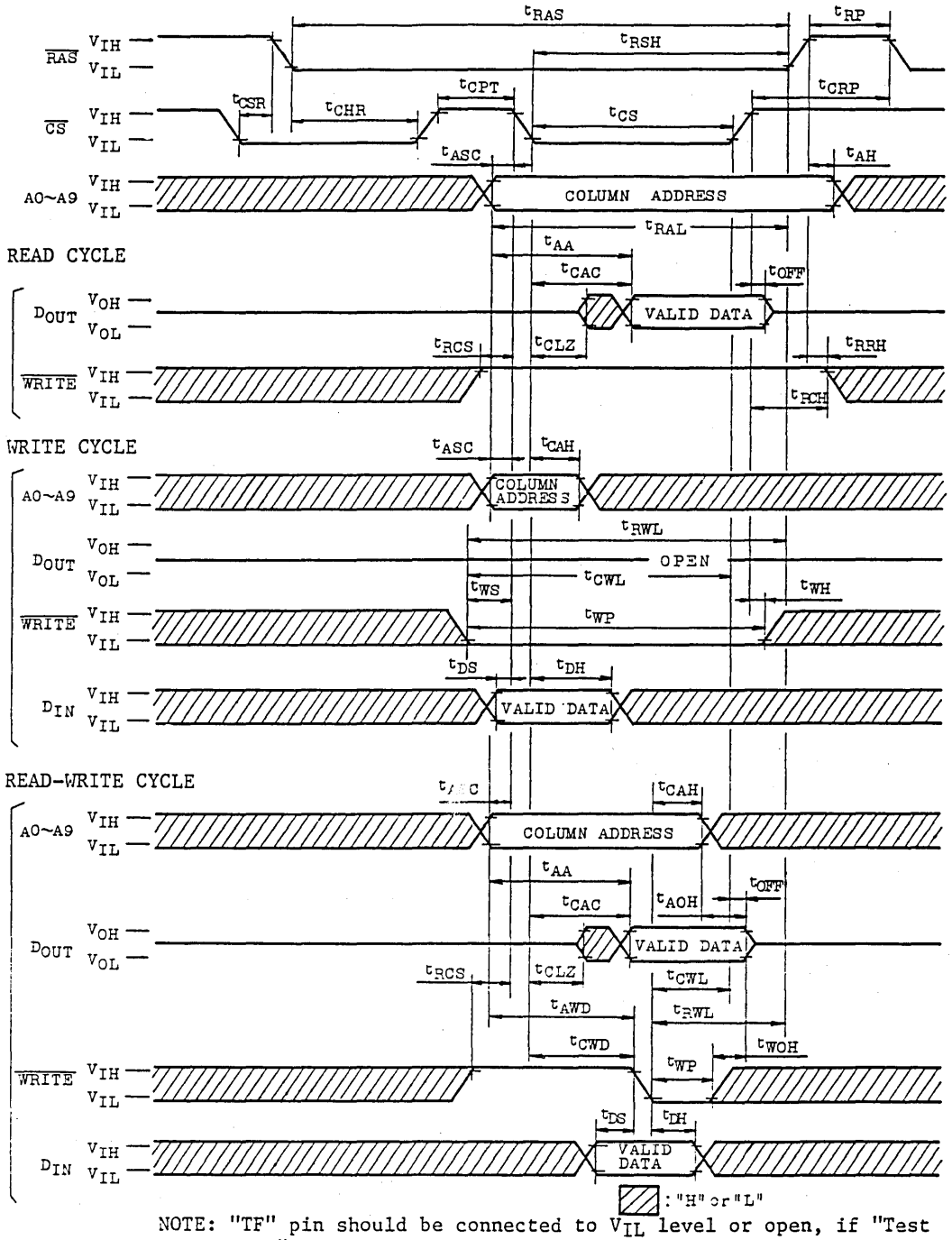


HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

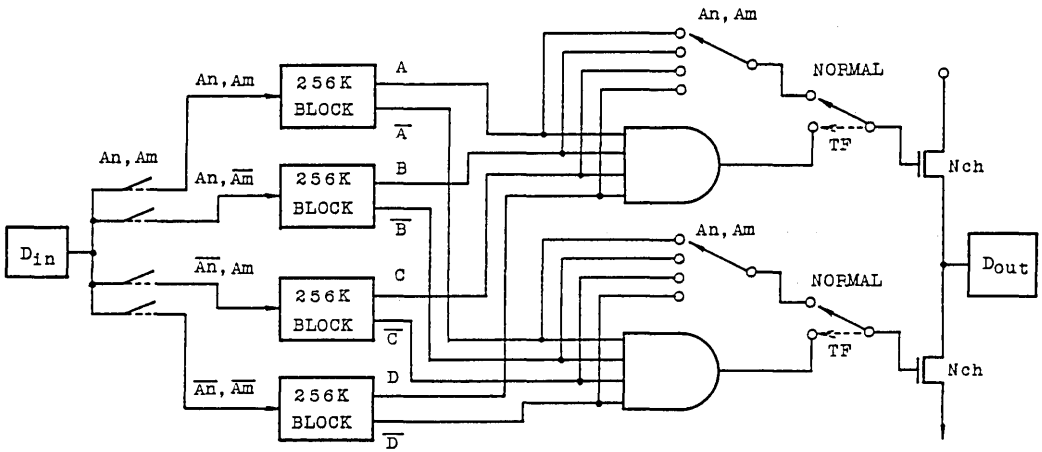
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- o For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- o For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode

TF Pin = Low level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

DESCRIPTION OF THE TEST MODE FOR 1M DRAMS (CONTINUED)

The "Test Mode" function is enabled by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period (tTES and tTEH as shown in figure 2). It can be used while operating in any mode, including static column mode. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode"

During normal operation or when the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

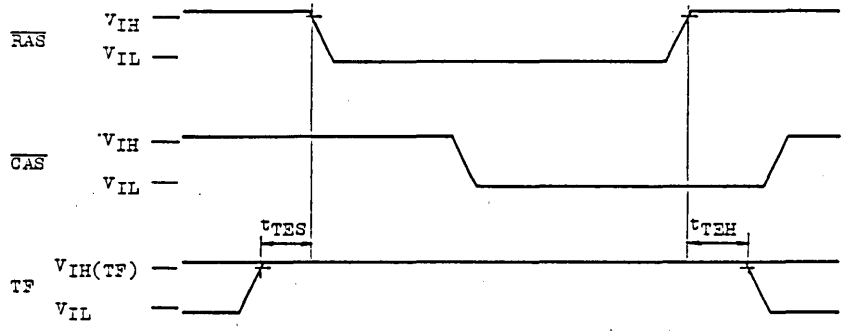
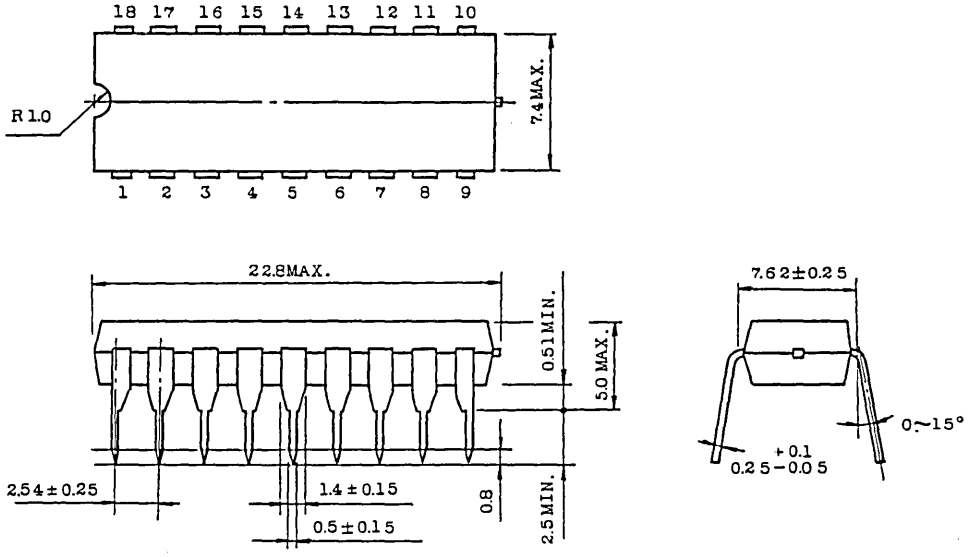


Fig.2 Test Mode Cycle

OUTLINE DRAWINGS

Plastic DIP

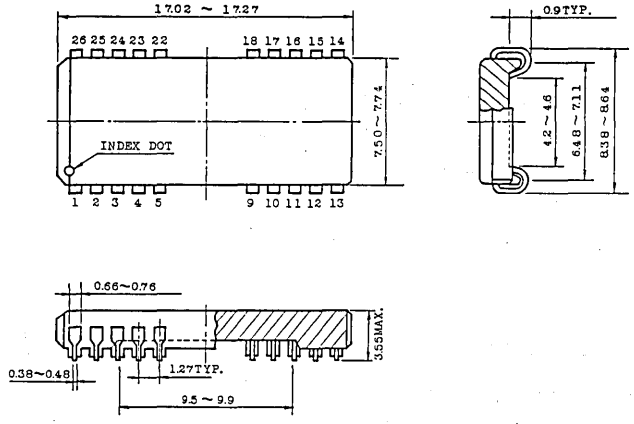
Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads. All dimensions are in millimeters.

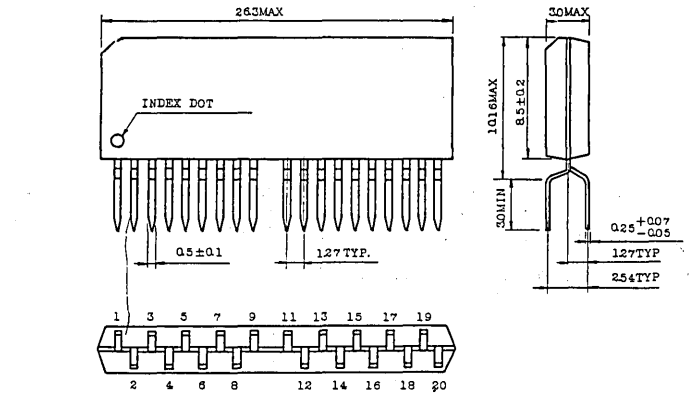
Plastic SOJ

Unit in mm



Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCT

262,144 WORDS × 4 BIT DYNAMIC RAM
SILICON GATE CMOS

TC514256P/J/Z-85, TC514256P/J/Z-10
TC514256P/J/Z-12

DESCRIPTION

The TC514256P/J/Z is the new generation dynamic RAM organized 262,144 words by 4 bit. The TC514256P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514256P/J/Z to be packaged in a standard 20 pin plastic DIP and 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

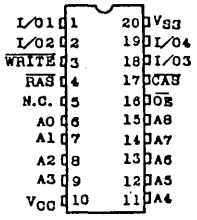
- 262,144 words by 4 bit organization
- Fast access time and cycle time

		TC514256P/J/Z-85-10-12		
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	30ns	35ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

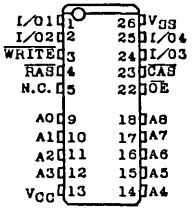
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  413mW MAX. Operating(TC514256P/J/Z-85)
  358mW MAX. Operating(TC514256P/J/Z-10)
  303mW MAX. Operating(TC514256P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, RAS-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC514256P
  Plastic SOJ: TC514256J
  Plastic ZIP: TC514256Z

PIN CONNECTION (TOP VIEW)

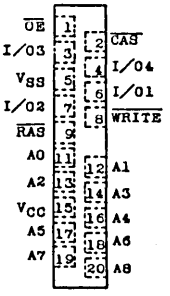
Plastic DIP



Plastic SOJ



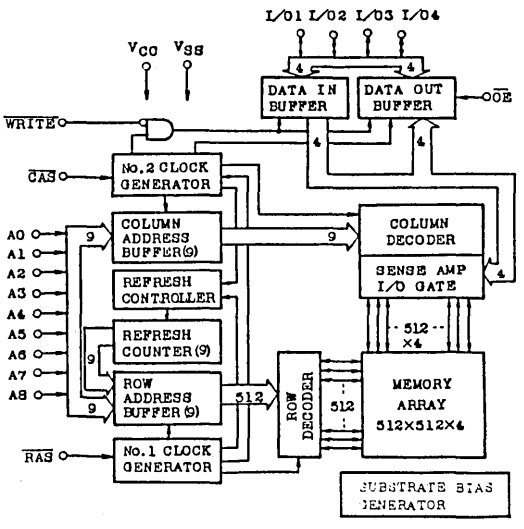
Plastic ZIP



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514256P/J/Z-85	-	75	mA	3,4
		TC514256P/J/Z-10	-	65		
		TC514256P/J/Z-12	-	55		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514256P/J/Z-85	-	75	mA	3
		TC514256P/J/Z-10	-	65		
		TC514256P/J/Z-12	-	55		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=VIL,$\overline{CAS}$,Address Cycling: t_{PC}=P_C MIN.)	TC514256P/J/Z-85	-	55	mA	3,4
		TC514256P/J/Z-10	-	45		
		TC514256P/J/Z-12	-	35		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=R_C MIN.)	TC514256P/J/Z-85	-	75	mA	3
		TC514256P/J/Z-10	-	65		
		TC514256P/J/Z-12	-	55		
$I_I(L)$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≦V_{IN}≦6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_O(L)$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ V_{CC})		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level VOLTAGE (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level VOLTAGE (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514256P/J/Z -85		TC514256P/J/Z -10		TC514256P/J/Z -12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	225	-	255	-	295	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	55	-	70	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	110	-	115	-	140	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	30	-	30	-	35	ns	8,13
t_{AA}	Access Tire from Column Address	-	45	-	50	-	60	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	50		65	ns	8,14
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	5	-	5	-	5	-	ns	5
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	-	30	-	35	-	ns	
t_{RSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	30	10,000	35	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	70	25	85	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20		25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	10
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10

SYMBOL	PARAMETER	TC514256P/J/Z -85		TC514256P/J/Z -10		TC514256P/J/Z -12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	65	-	65	-	75	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	120	-	135	-	160	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	80	-	85	-	100	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	50	-	60	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	20	-	20	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	25	-	25	-	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	-	25	-	30	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	25	0	25	0	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	-	25	-	30	-	ns	

CAPACITANCE (V_{CC} = 5V±10%, f=1MHz, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A_0 - A_8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Output Capacitance (I/O_1 - I/O_4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" May cause permanent damage to the device.

2. All voltage are reference to V_{SS}.

3. Icc1, Icc3, Icc4, Icc6 depend on cycle rate.

4. Icc1, Icc4 depend on output loading. Specified value are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measurement with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

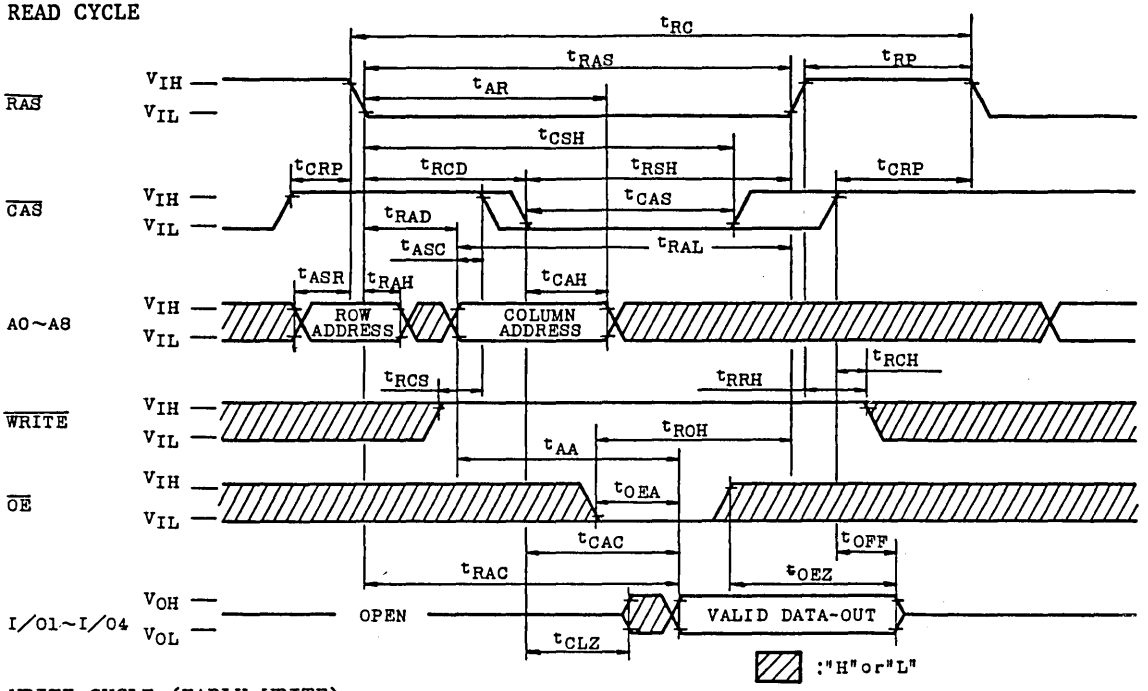
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.

12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

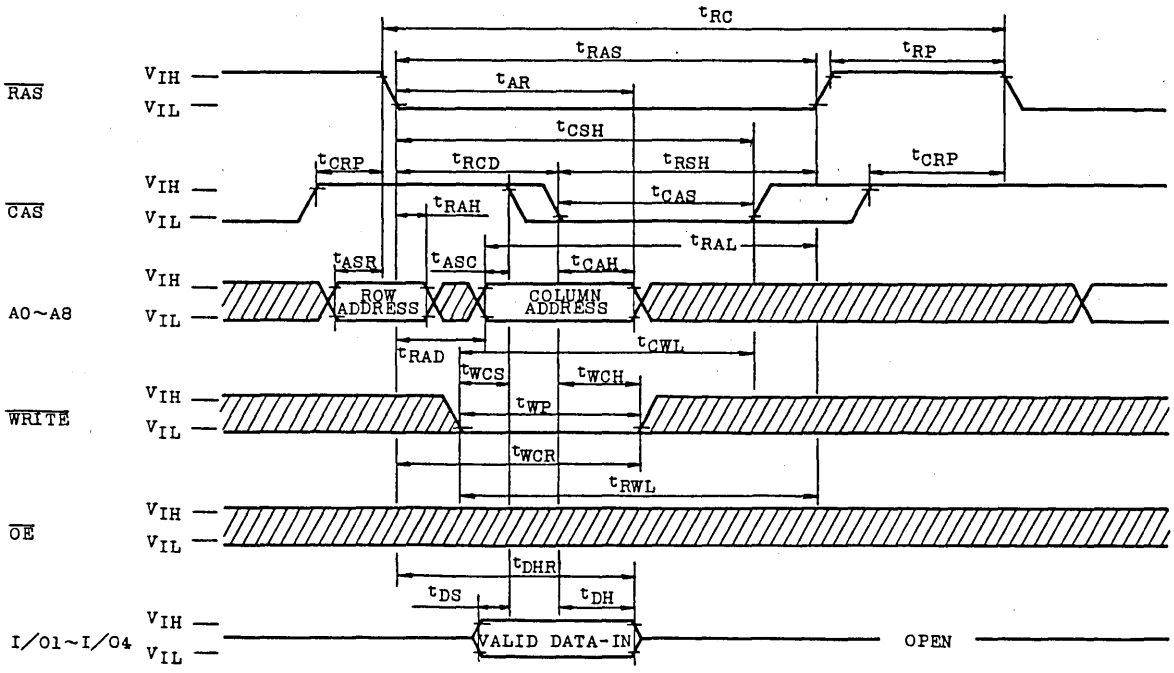
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

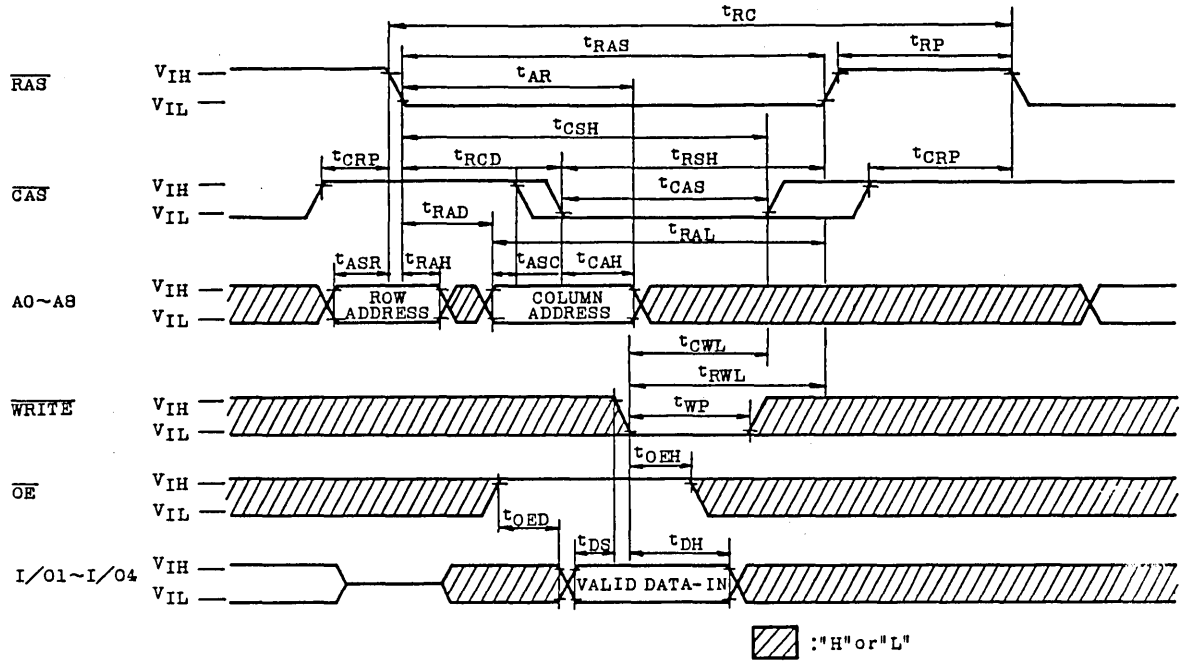
READ CYCLE



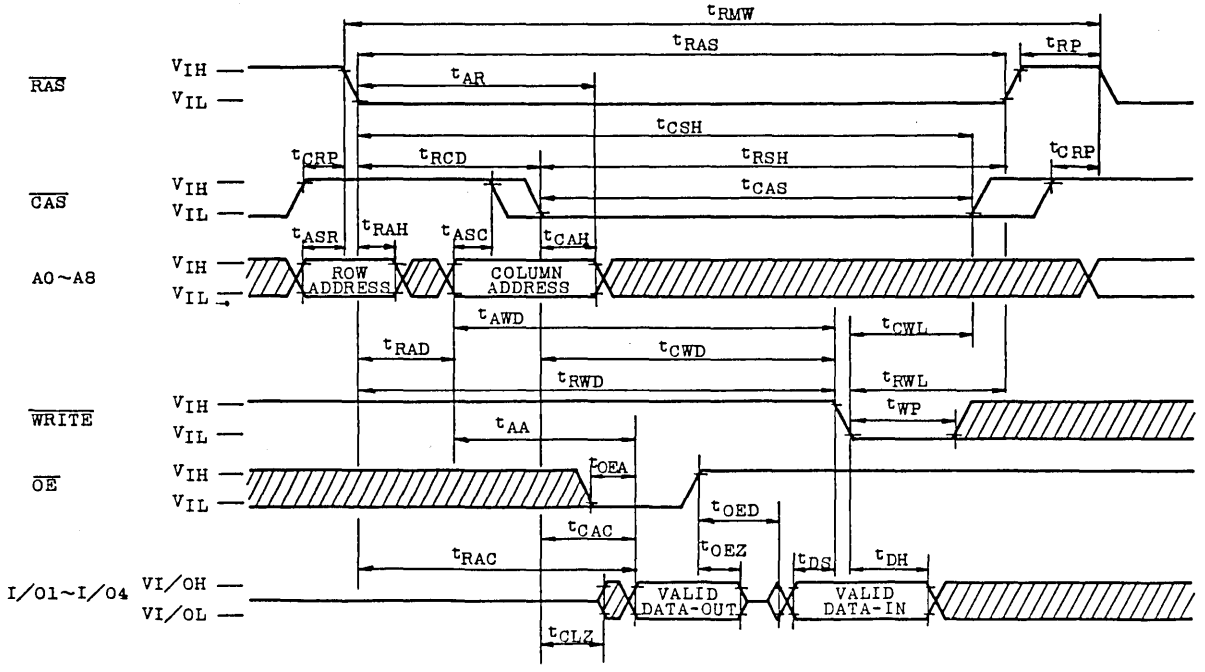
WRITE CYCLE (EARLY WRITE)



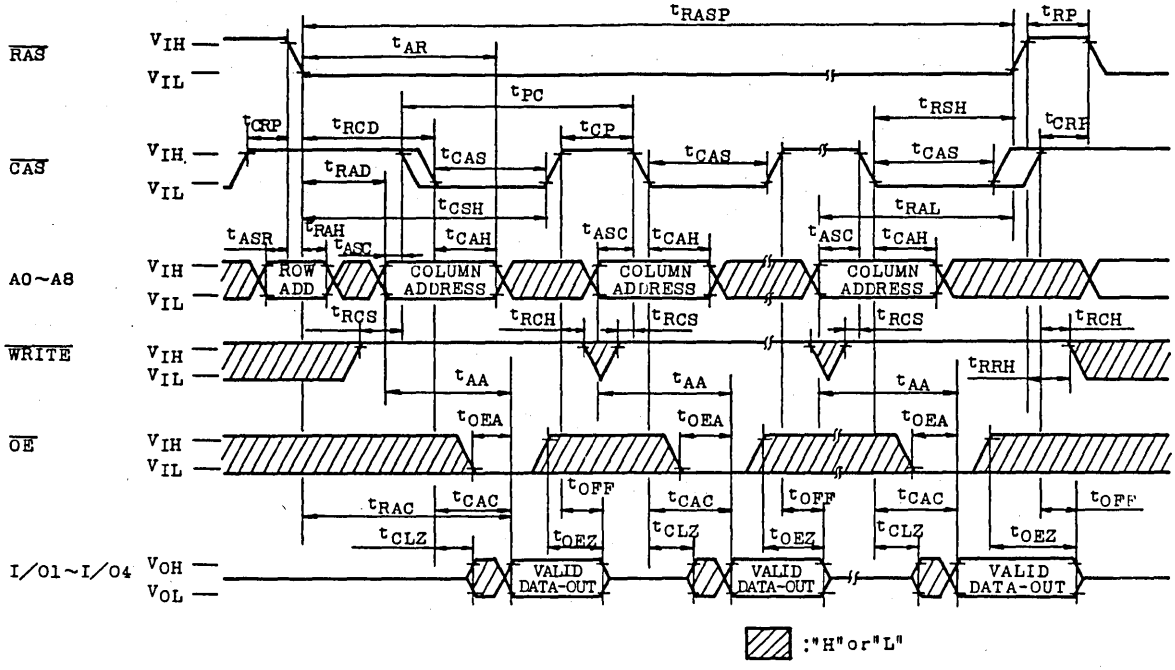
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



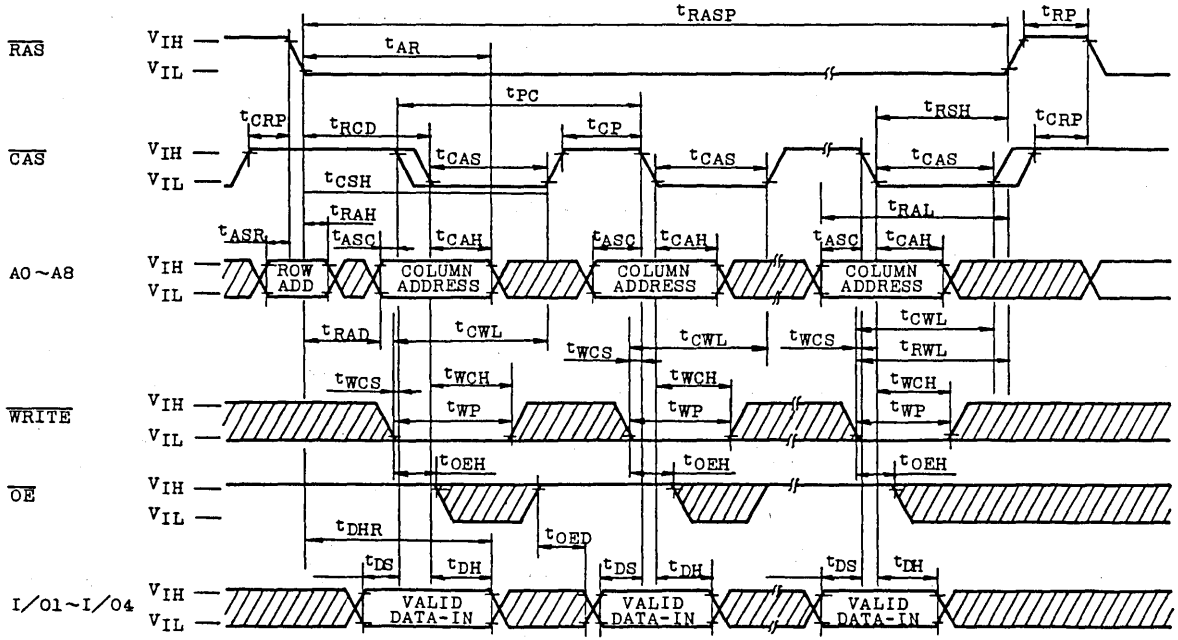
READ-MODIFY-WRITE CYCLE



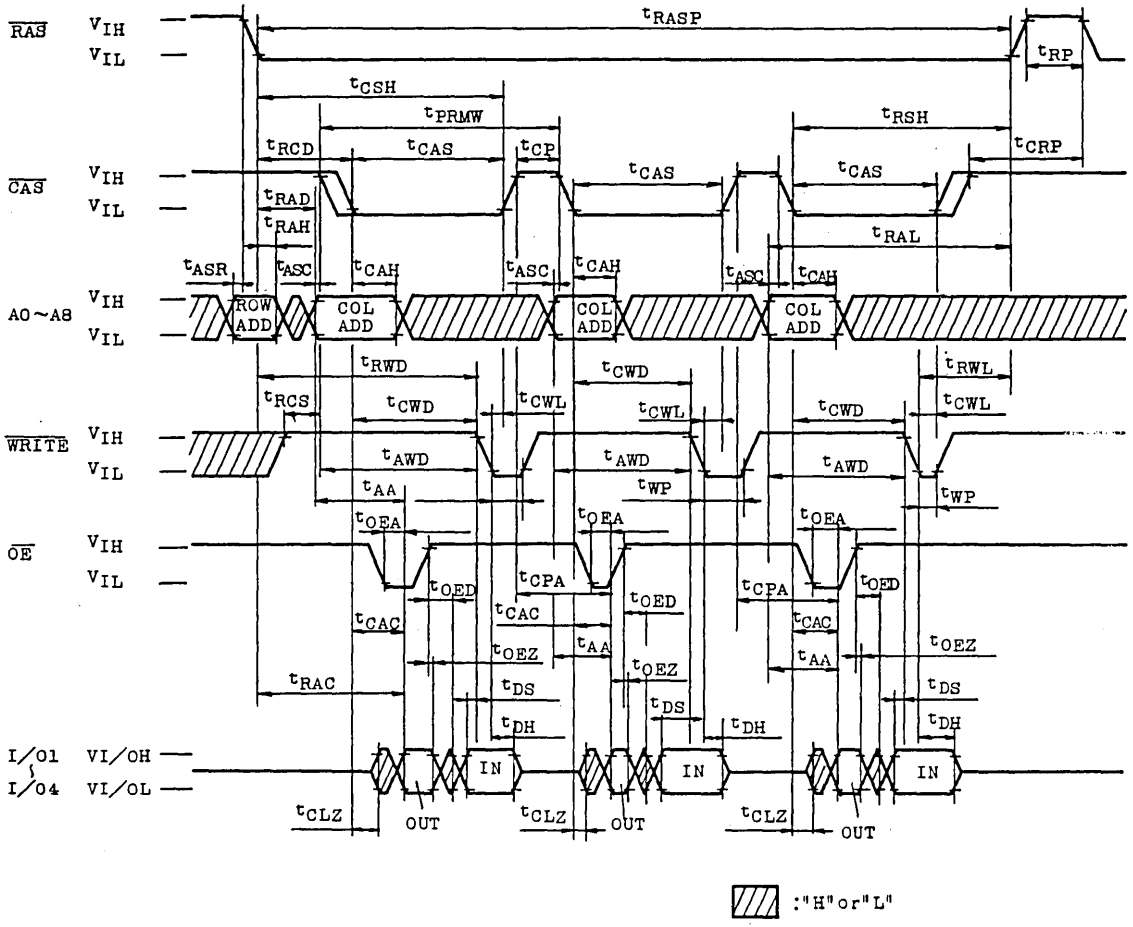
FAST PAGE MODE READ CYCLE



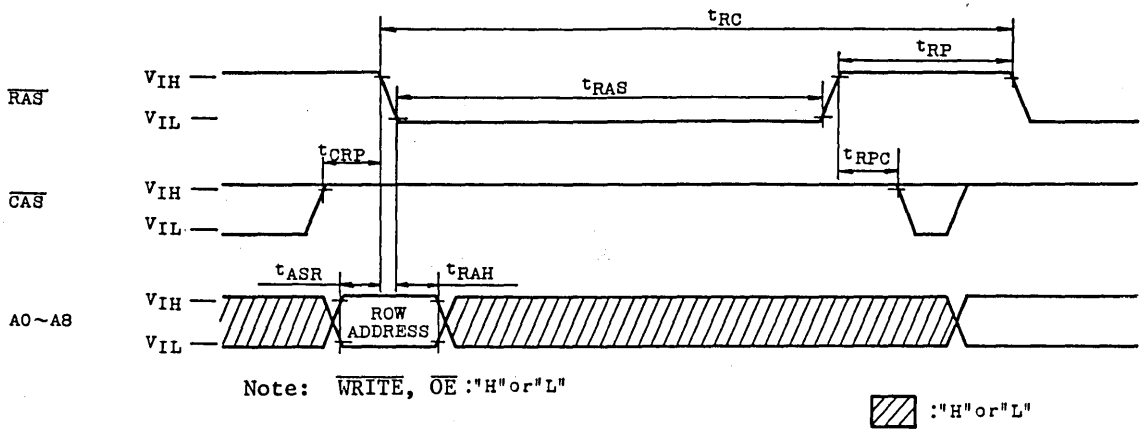
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



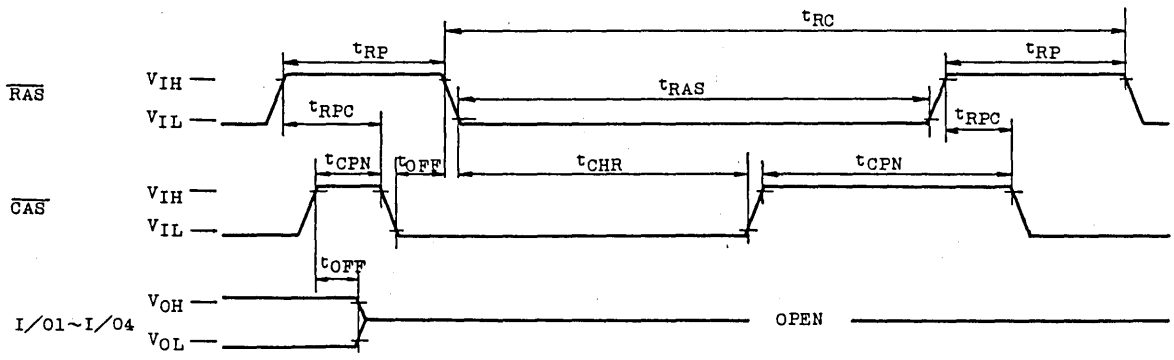
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$:"H"or"L"

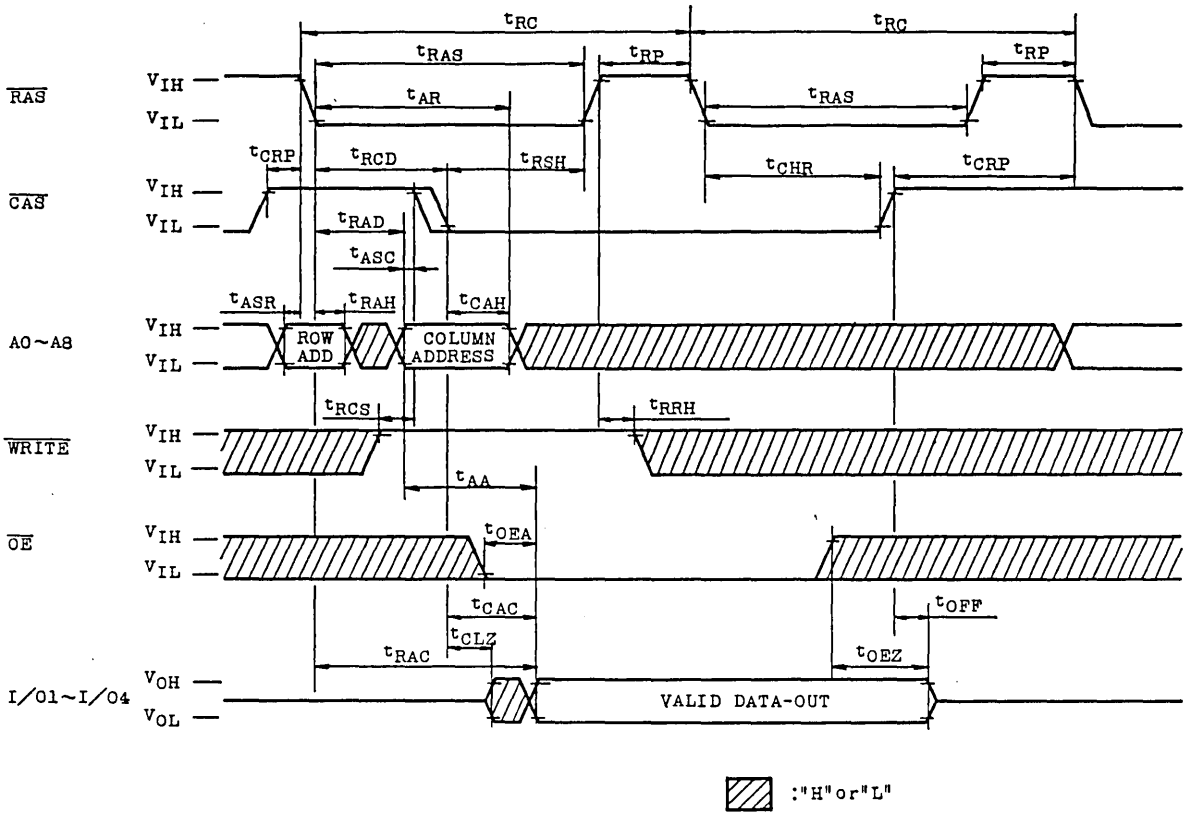
:"H"or"L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

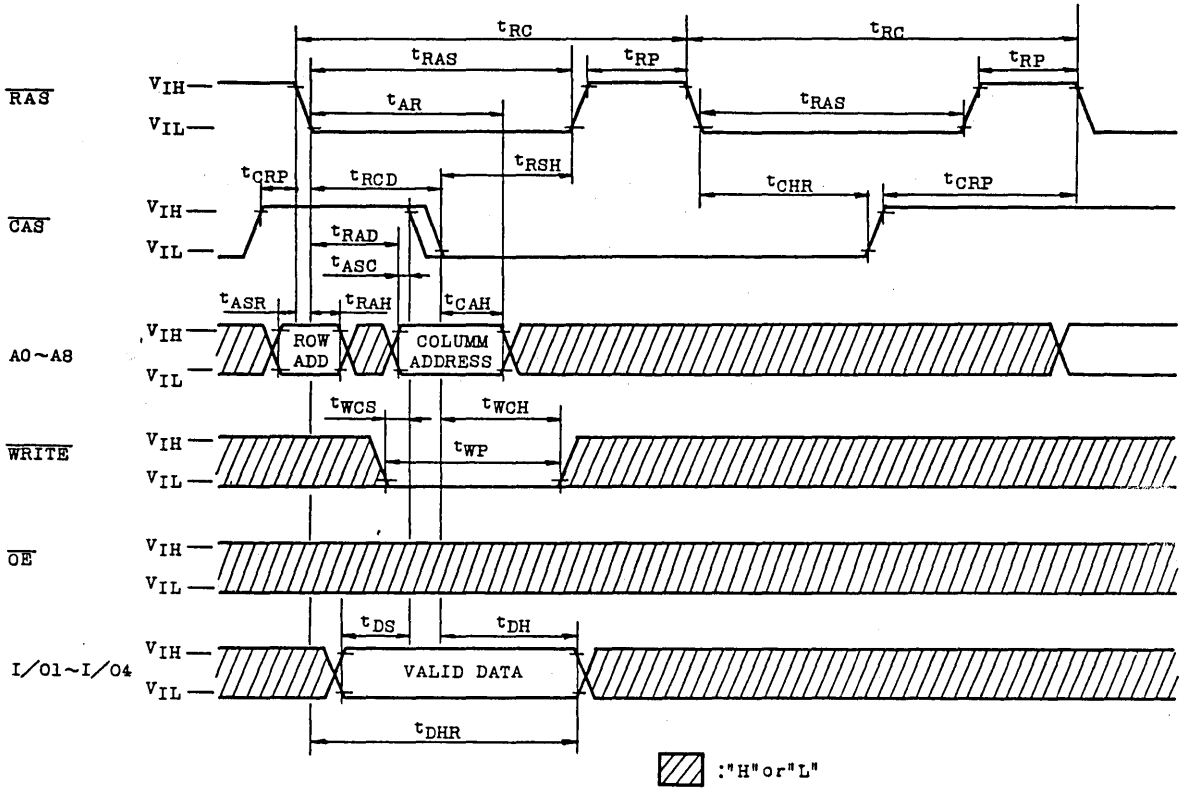


Note: $\overline{WRITE}$, $\overline{OE}$, A0 ∿ A8 :"H"or"L"

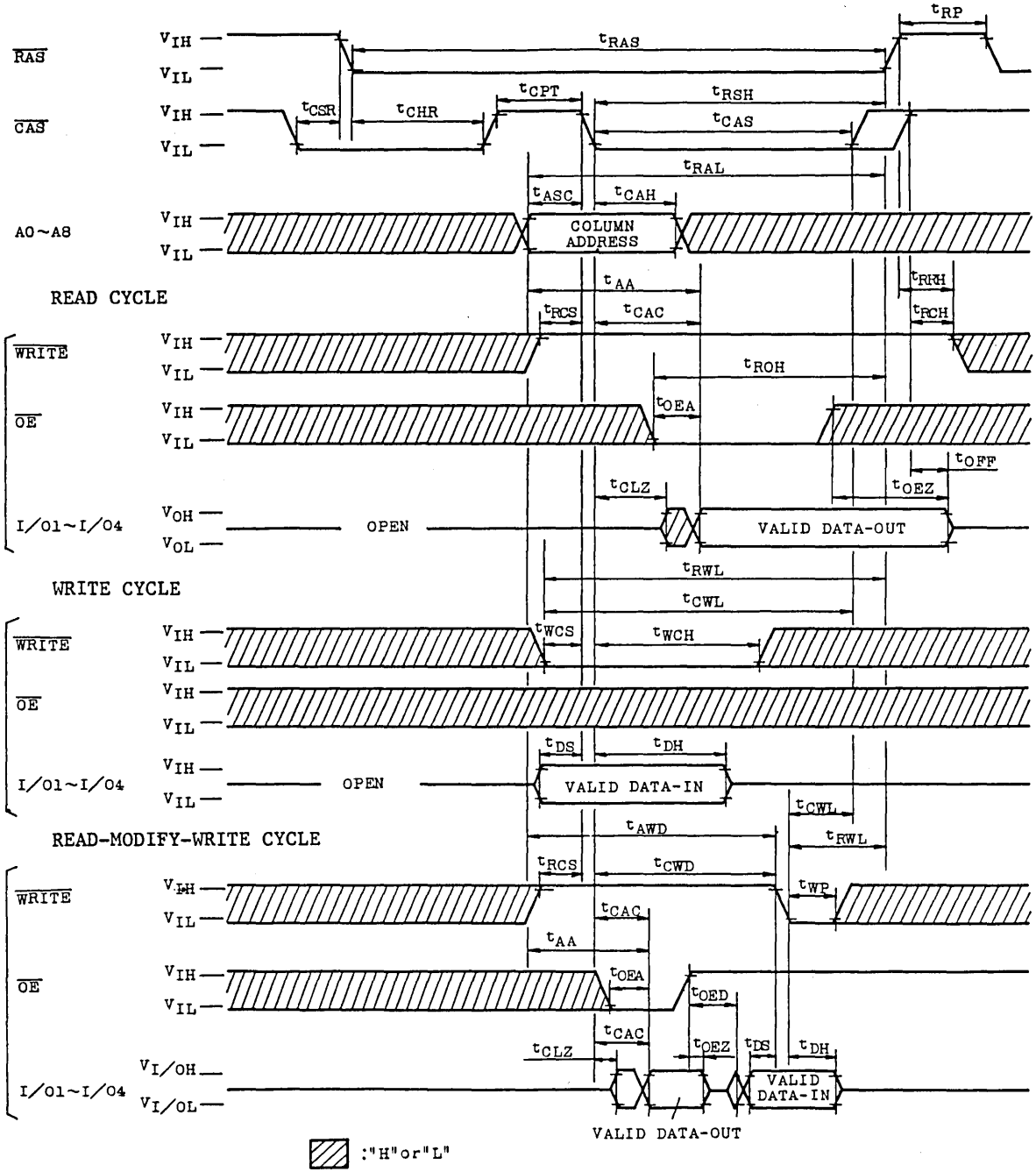
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



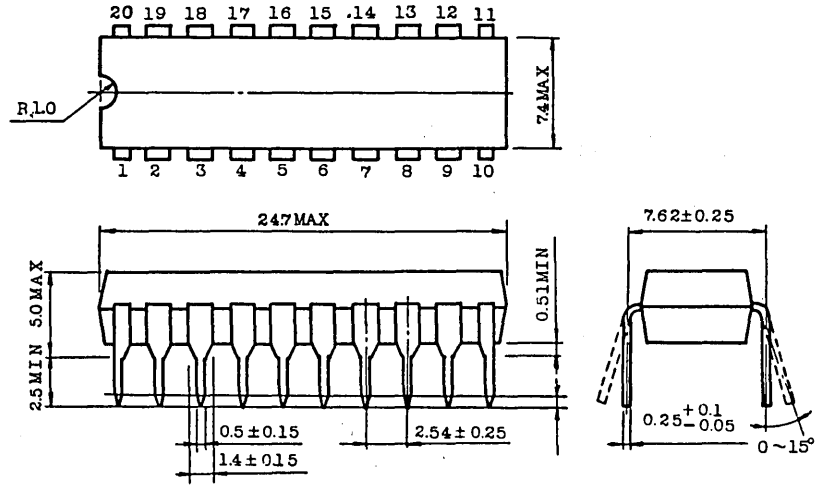
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OUTLINE DRAWINGS

• Plastic DIP

Unit in mm

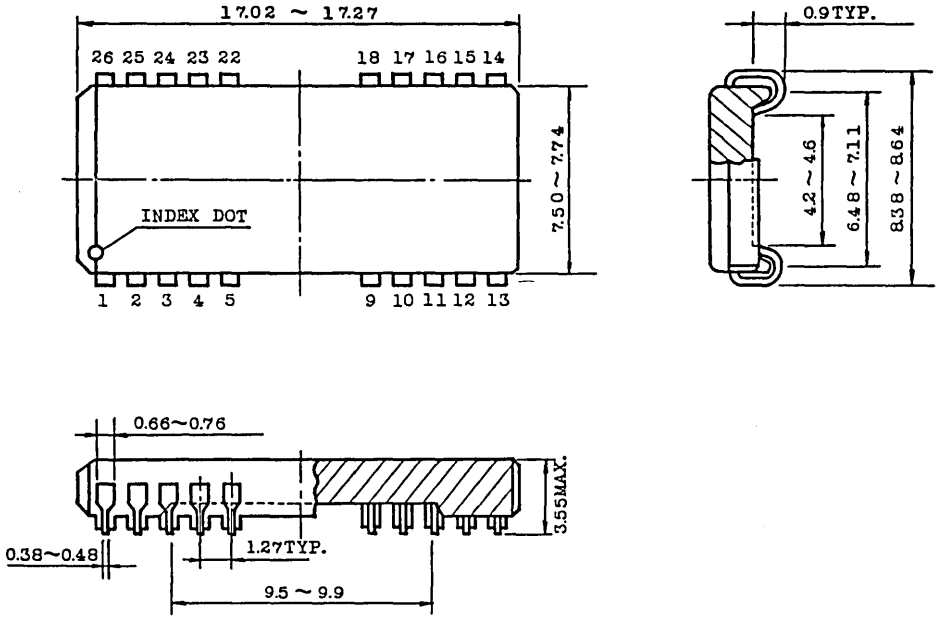


Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.20 leads.

All dimensions are in millimeters.

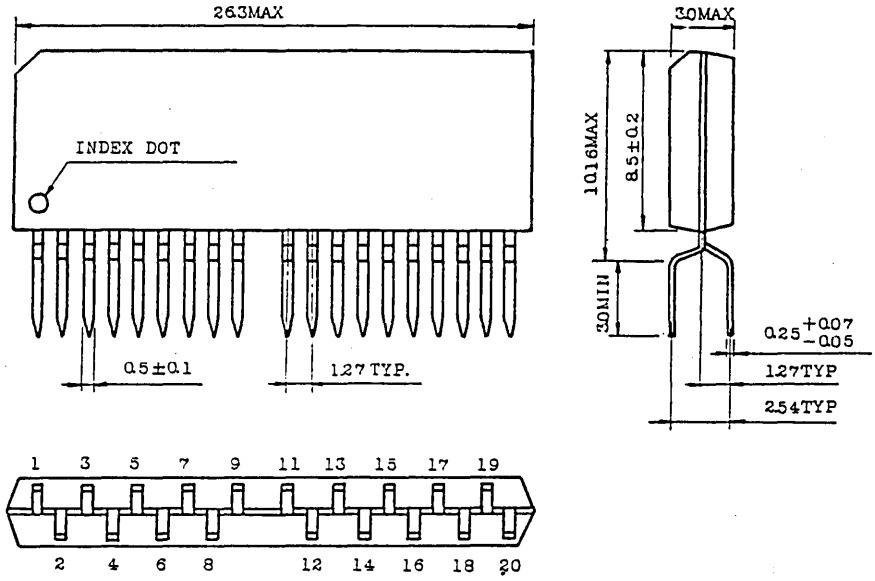
• Plastic SOJ



Note: Each lead pitch 1.27mm.
All dimensions are in millimeters.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCT

262,144 WORDS × 4 BIT DYNAMIC RAM
SILICON GATE CMOS

TC514258P/J/Z-85, TC514258P/J/Z-10
TC514258P/J/Z-12

DESCRIPTION

The TC514258P/J/Z is the new generation dynamic RAM organized 262,144 words by 4 bit. The TC514258P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514258P/J/Z to be packaged in a standard 20 pin plastic DIP and 20/26 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

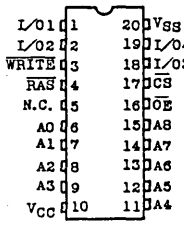
- 262,144 words by 4 bit organization
- Fast access time and cycle time

		TC514258P/J/Z-85-10-12		
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	30ns	30ns	35ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	50ns	55ns	65ns

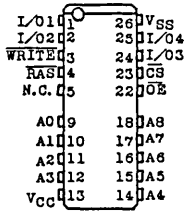
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  413mW MAX. Operating (TC514258P/J/Z-85)
  358mW MAX. Operating (TC514258P/J/Z-10)
  303mW MAX. Operating (TC514258P/J/Z-12)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Static Column Mode capability
- All inputs and outputs TTL complatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC514258P
  Plastic SOJ: TC514258J
  Plastic ZIP: TC514258Z

PIN CONNECTION (TOP VIEW)

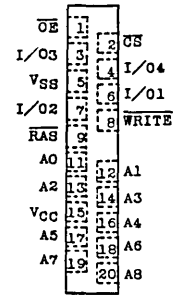
• Plastic DIP



• Plastic SOJ



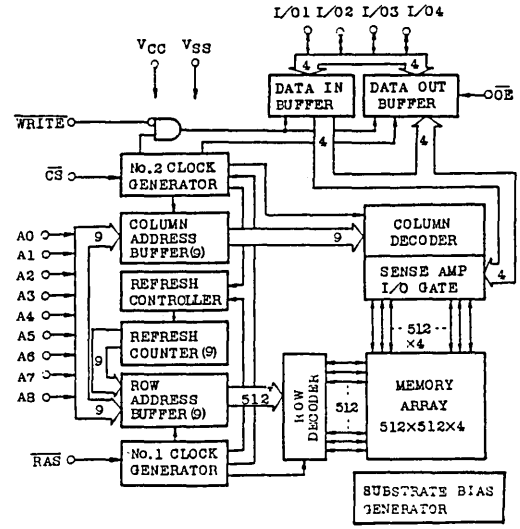
• Plastic ZIP



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	UNIT	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514258P/J/Z-85	-	75	mA	3,4
		TC514258P/J/Z-10	-	65		
		TC514258P/J/Z-12	-	55		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514258P/J/Z-85	-	75	mA	3
		TC514258P/J/Z-10	-	65		
		TC514258P/J/Z-12	-	55		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	TC514258P/J/Z-85	-	75	mA	3,4
		TC514258P/J/Z-10	-	65		
		TC514258P/J/Z-12	-	55		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514258P/J/Z-85	-	75	mA	3
		TC514258P/J/Z-10	-	65		
		TC514258P/J/Z-12	-	55		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≦V_{IN}≦6.5V, All Other Pins Not Under Test = 0V		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disable, 0V ≦ V_{OUT} ≦ 5.5V		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514258P/J/Z-85		TC514258P/J/Z-10		TC514258P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	225	-	255	-	295	-	ns	
t_{SC}	Static Column Mode Cycle Time	50	-	55	-	65	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	110	-	115	-	135	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CS}$	-	30	-	30	-	35	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{ALW}	Access Time from Last Write	-	85	-	95	-	115	ns	8,15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	30	-	30	-	35	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	30	-	30	-	35	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	30	10,000	30	10,000	35	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	30	100,000	30	100,000	35	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	55	25	70	25	85	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold TIme	20	-	20	-	25	-	ns	
t_{AWR}	Write Address Hold Time Referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	100	-	115	-	140	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{AH}	Column Address Hold Time Referenced to $\overline{RAS}$ Rise	10	-	10	-	15	-	ns	16
t_{LWAD}	Last Write to Column Address Delay Time	25	40	25	45	30	55	ns	17

SYMBOL	PARAMETER	TC514258P/J/Z-85		TC514258P/J/Z-10		TC514258P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AHLW}	Last Write to Column Address Hold Time	85	-	95	-	115	-	ns	
t_{RCS}	Read Command Set-up Time Referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	$\overline{WRITE}$ Pulse Width	20	-	20	-	25	-	ns	
t_{WI}	$\overline{WRITE}$ Inactive Time	10	-	10	-	15	-	ns	
t_{RWL}	$\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	$\overline{WRITE}$ Command to $\overline{CS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WS}	$\overline{WRITE}$ Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	65	-	65	-	75	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	120	-	135	-	160	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	80	-	85	-	100	-	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ counter Test Cycle)	50	-	50	-	60	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	20	-	20	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	30	-	35	-	45	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	-	25	-	30	-	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	25	0	25	0	30	ns	9
t_{OEH}	$\overline{OE}$ Command Hold Time	25	-	25	-	30	-	ns	

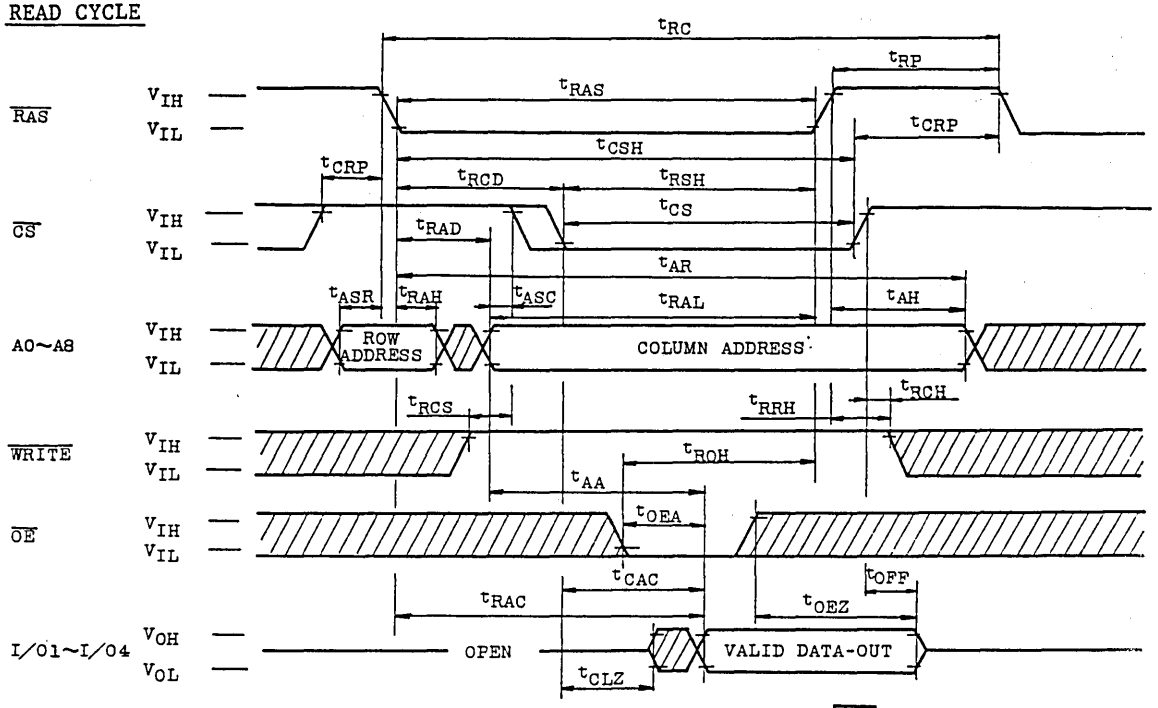
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A_0 ∿ A_8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	
C_O	Output Capacitance (I/O_1 ∿ I/O_4)	-	7	

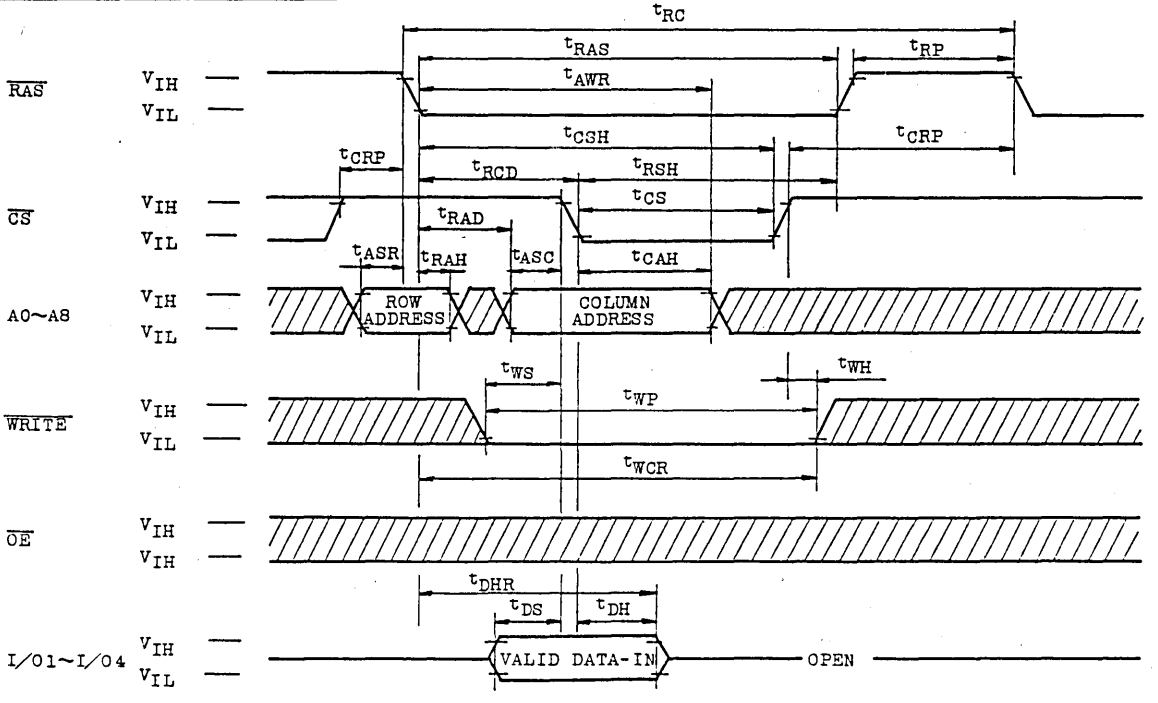
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. Icc1, Icc3, Icc4, Icc6 depend on cycle rate.
4. Icc1, Icc4 depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
12. t_{WS}, t_{WH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WS} \geq t_{WS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD} (max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

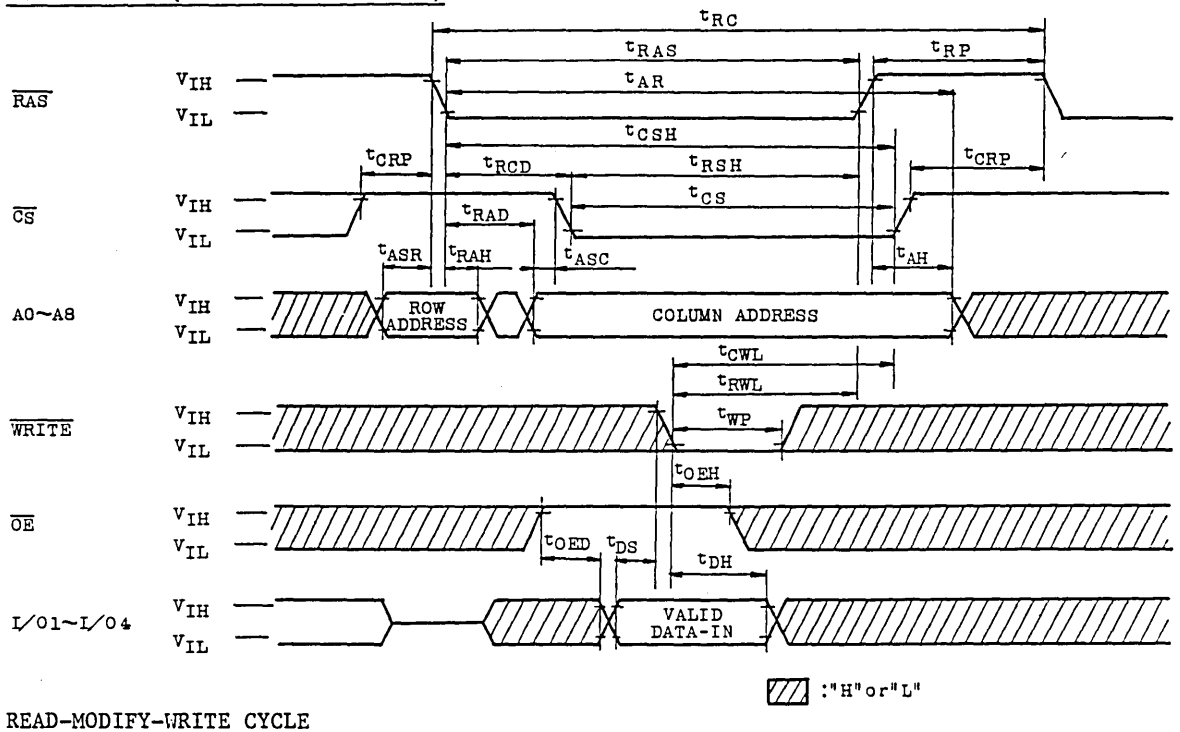
READ CYCLE



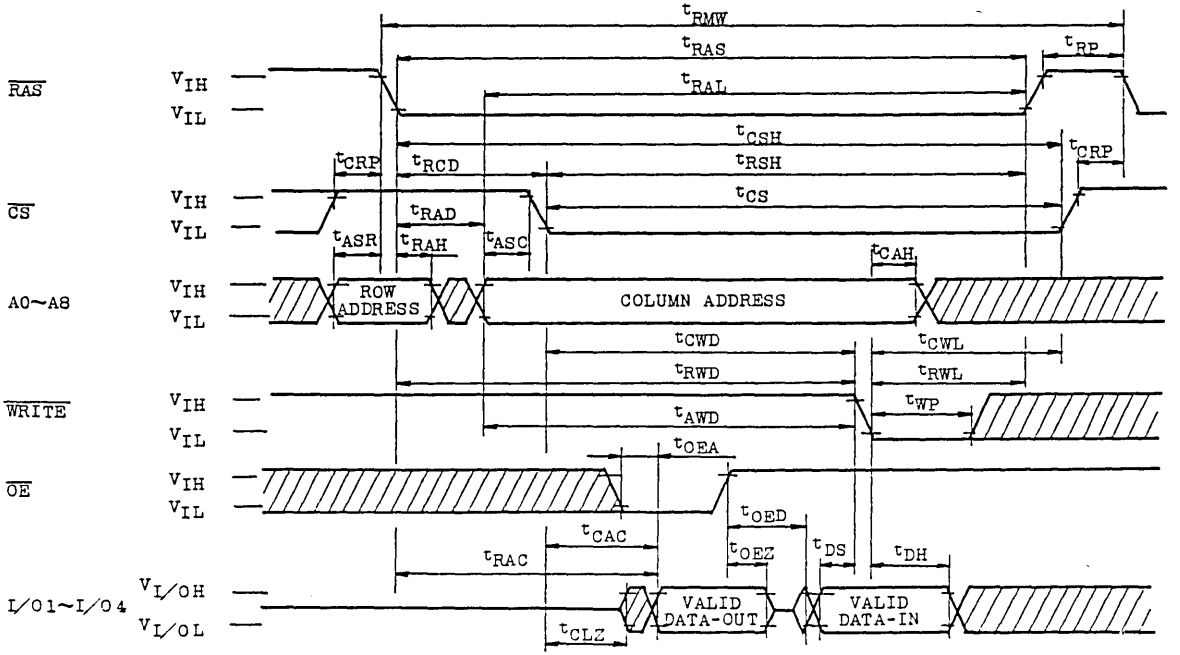
WRITE CYCLE (EARLY WRITE)



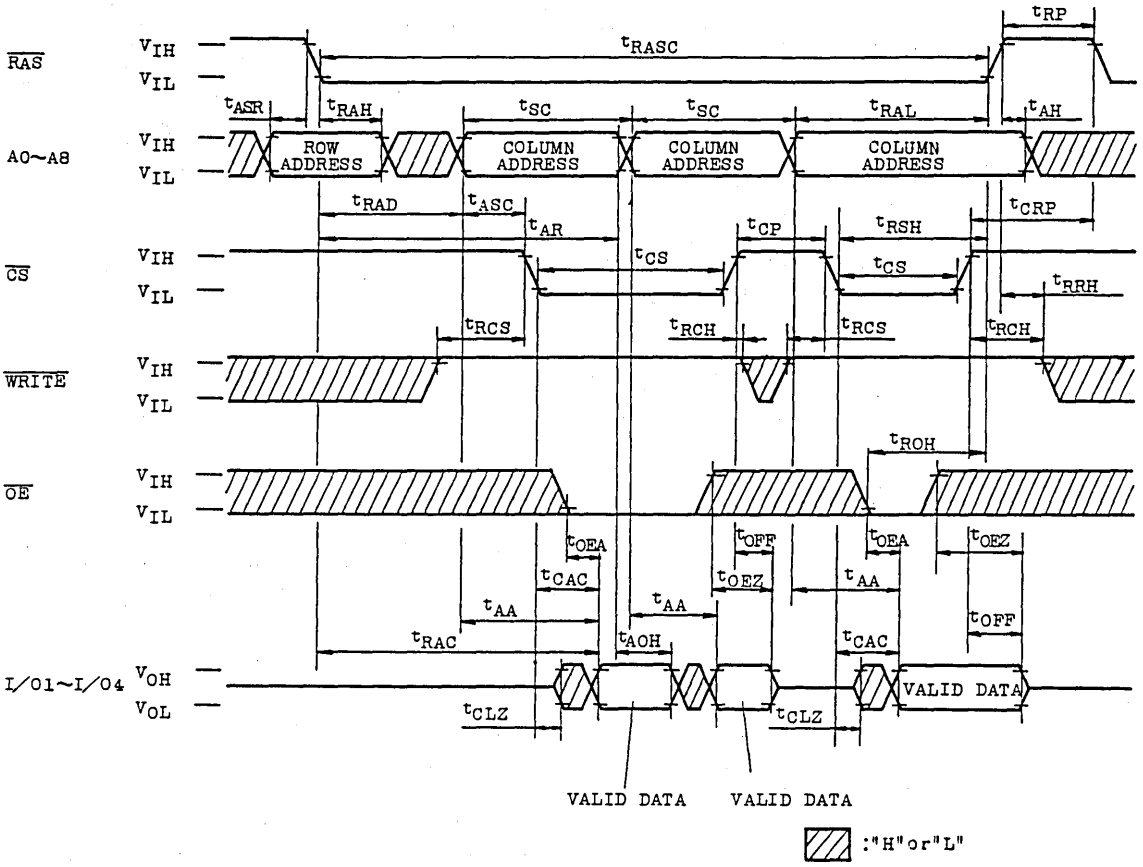
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



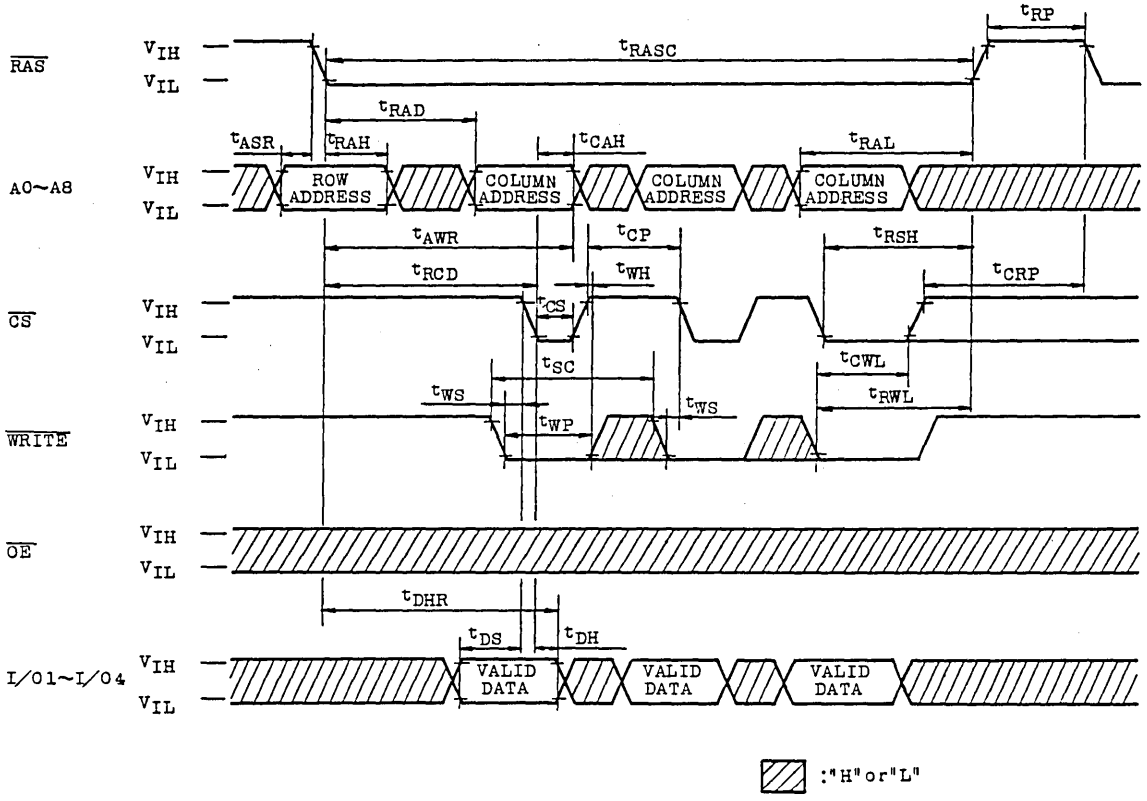
READ-MODIFY-WRITE CYCLE



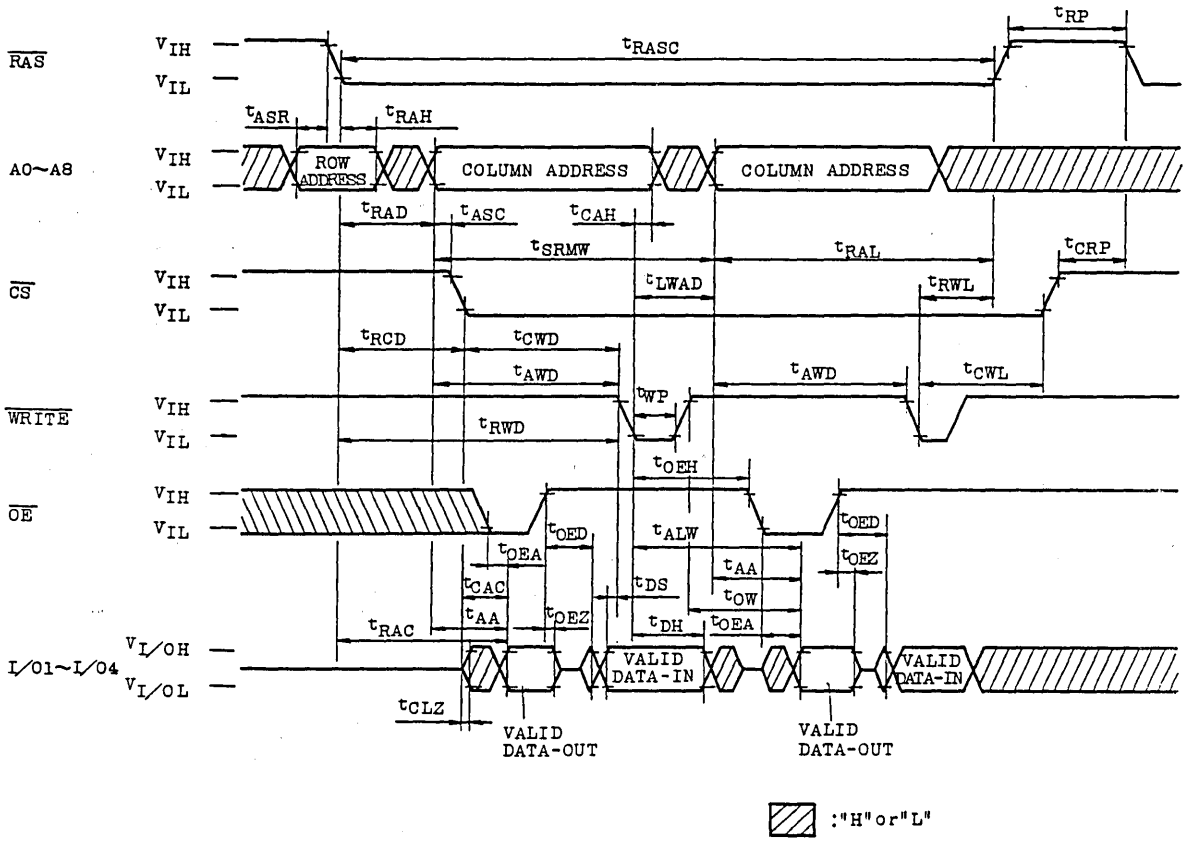
STATIC COLUMN MODE READ CYCLE



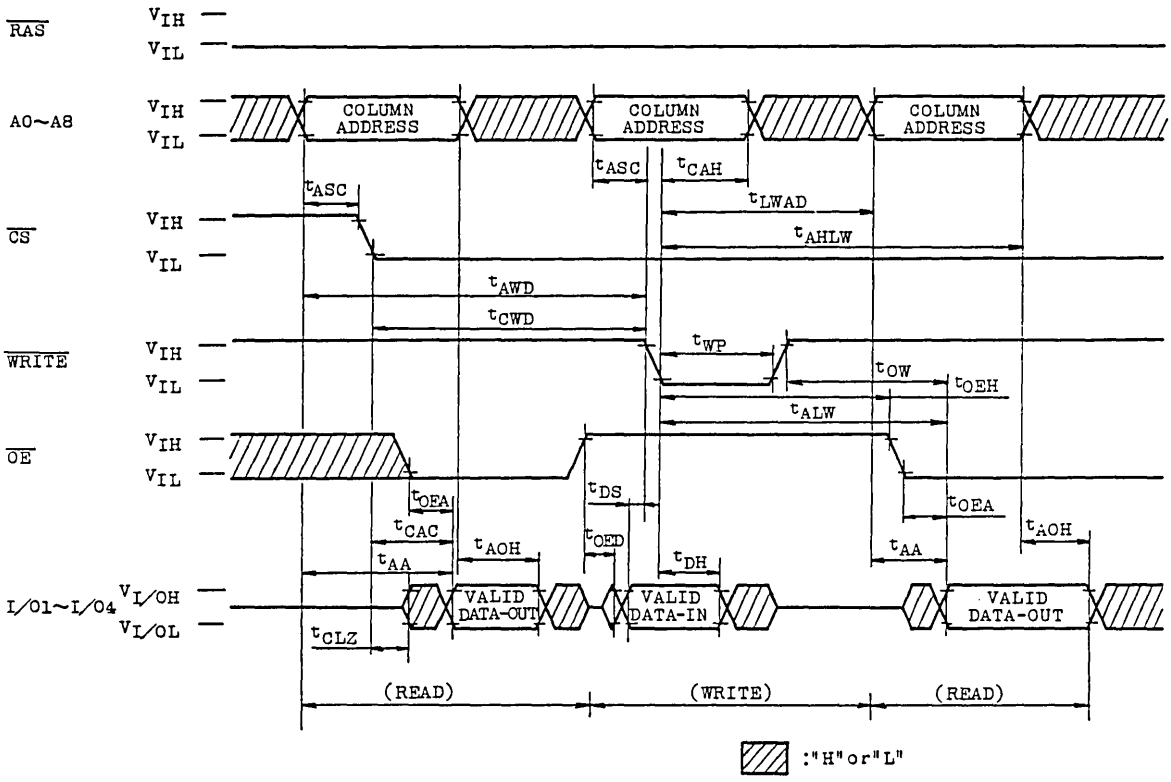
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



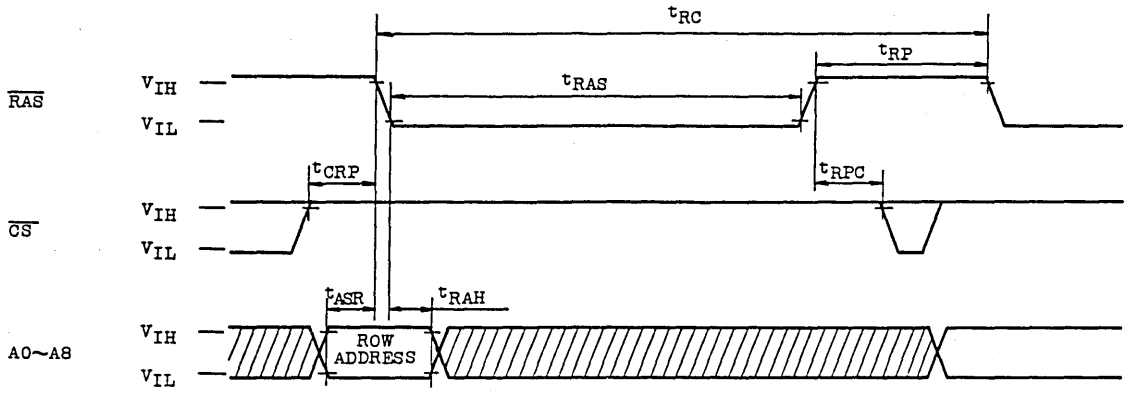
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE



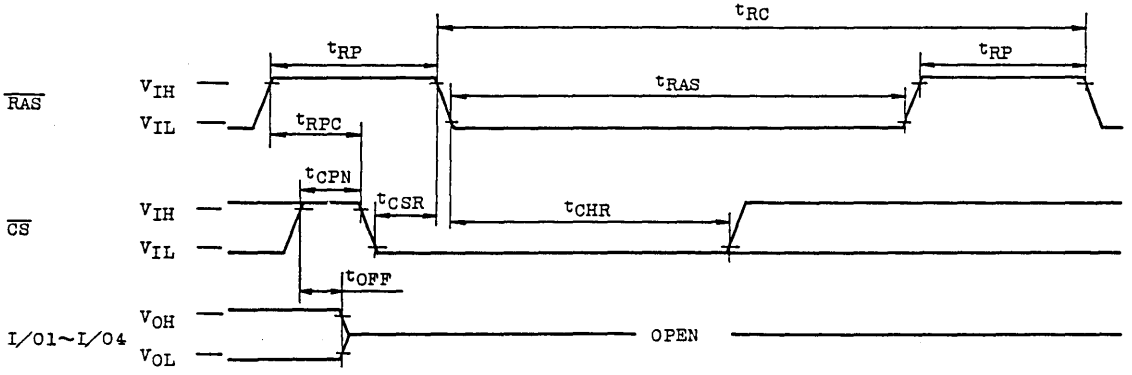
$\overline{RAS}$ ONLY REFRESH CYCLE



Notes: $\overline{WRITE}$, $\overline{OE}$:"H"or"L"

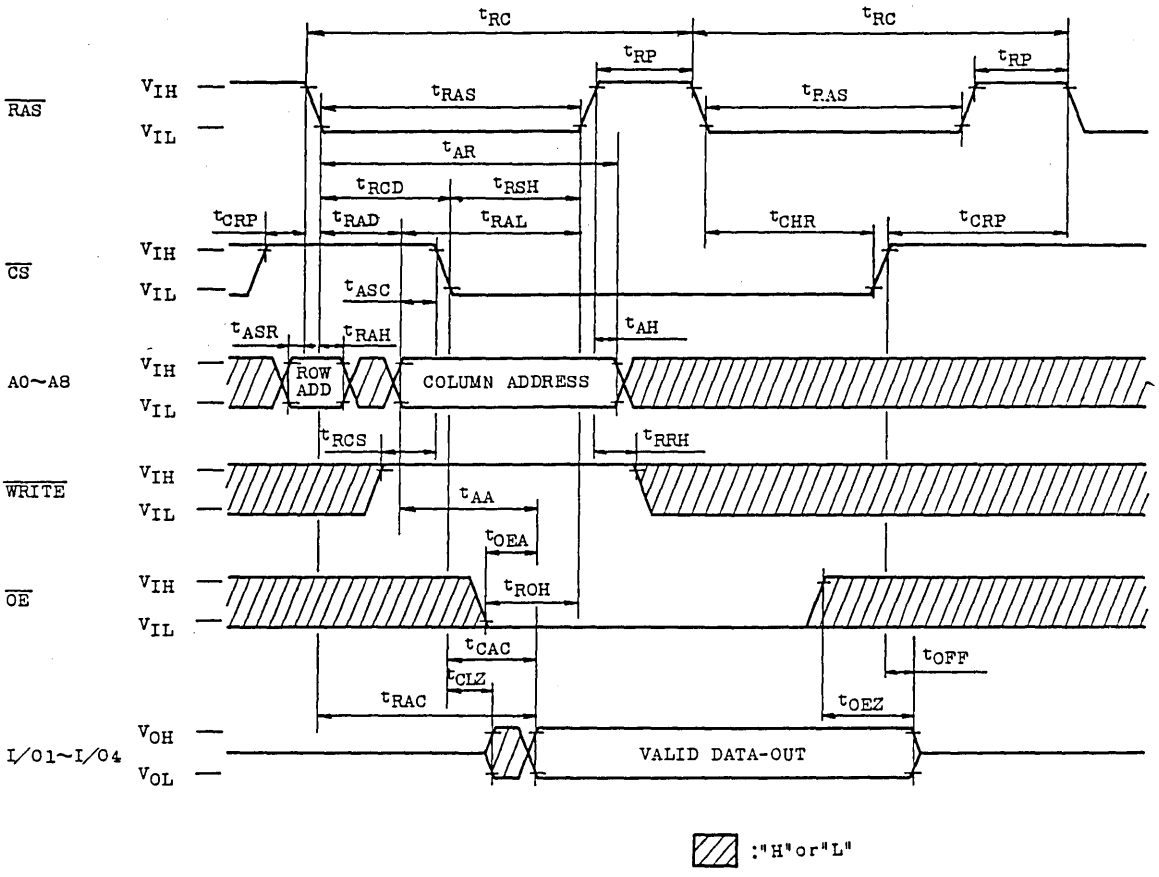
:"H"or"L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

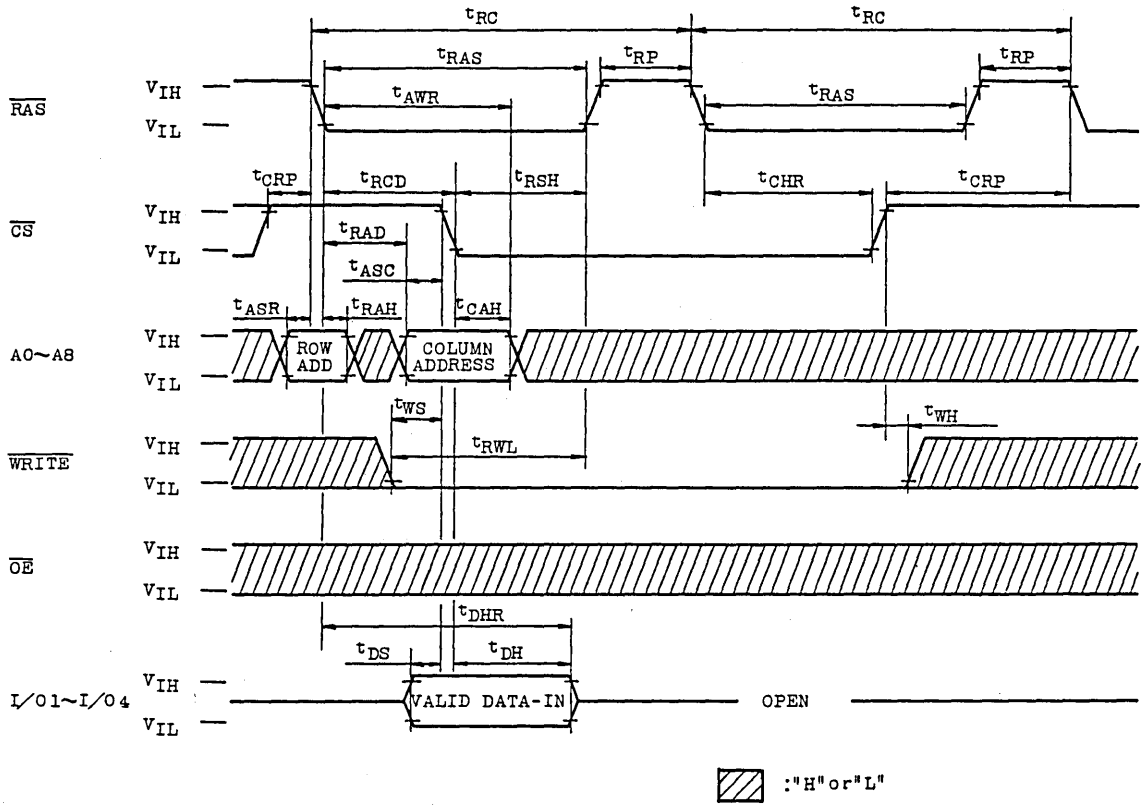


Note: $\overline{WRITE}$, $\overline{OE}$, A0 ∿ A8 :"H"or"L"

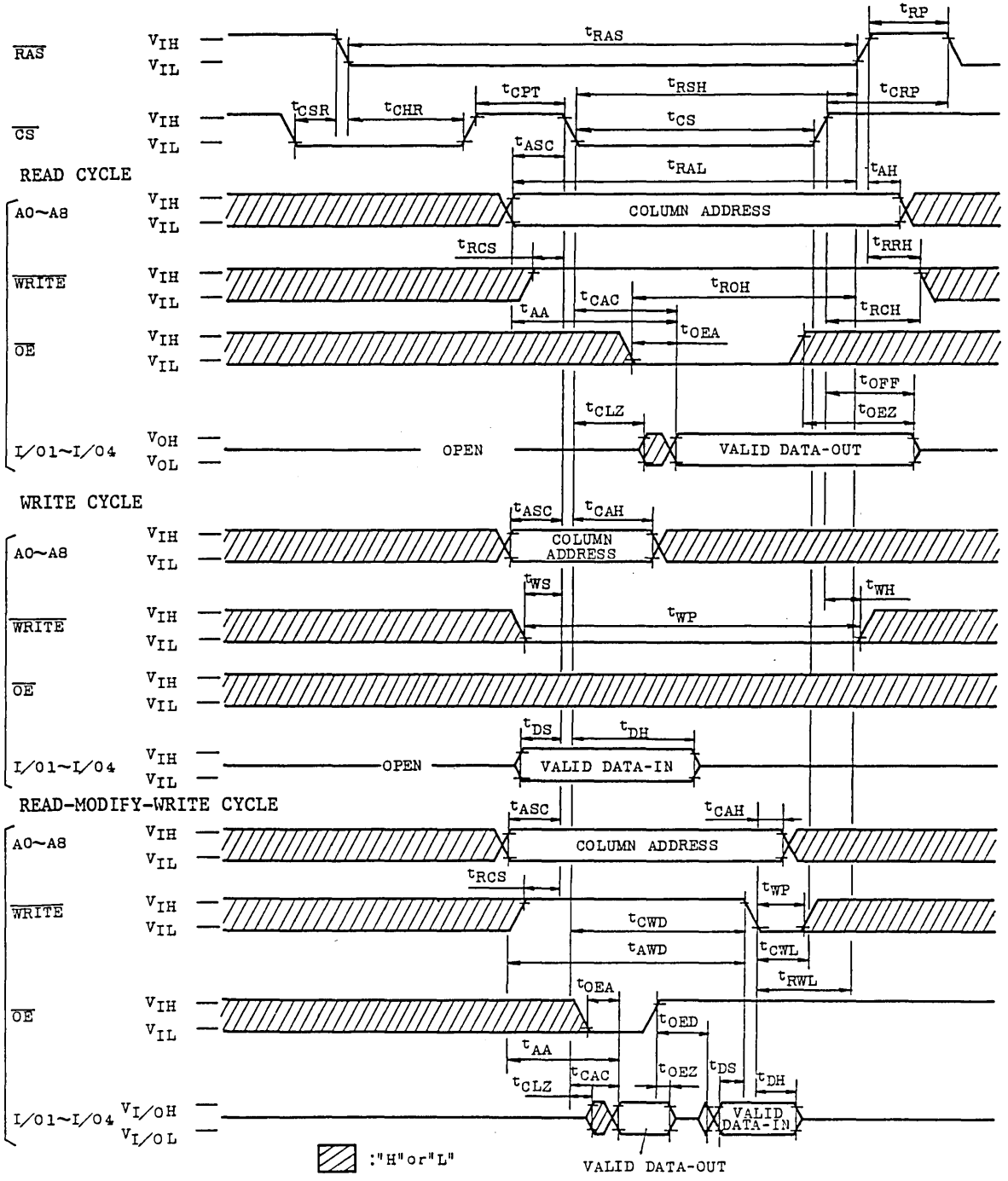
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



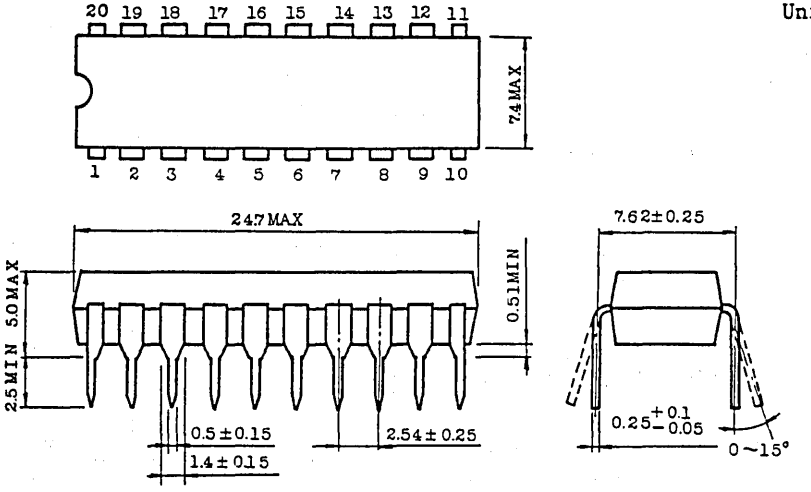
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OUTLINE DRAWINGS

• Plastic DIP

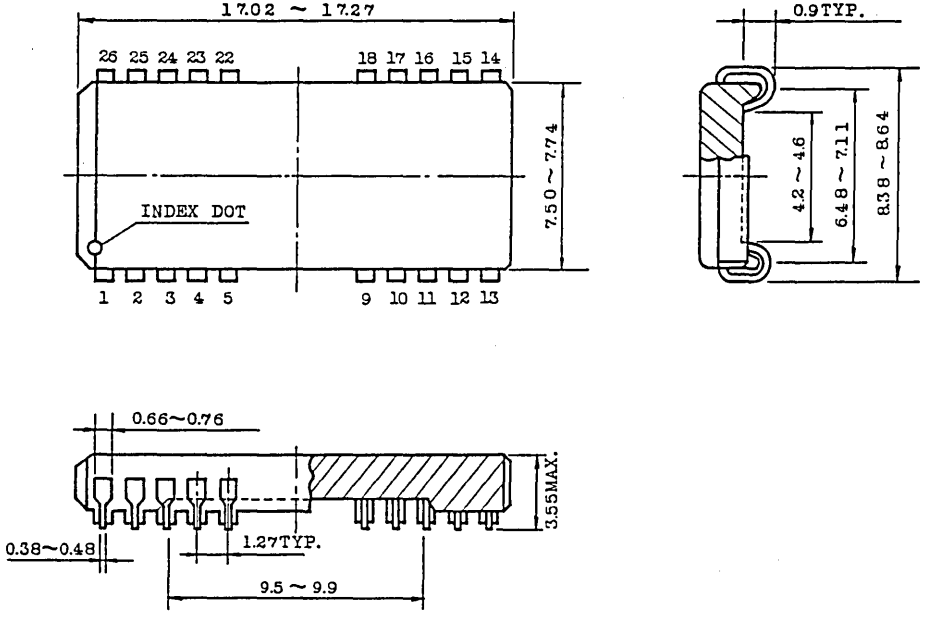
Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.20 leads.
All dimensions are in millimeters.

• Plastic SOJ

Unit in mm

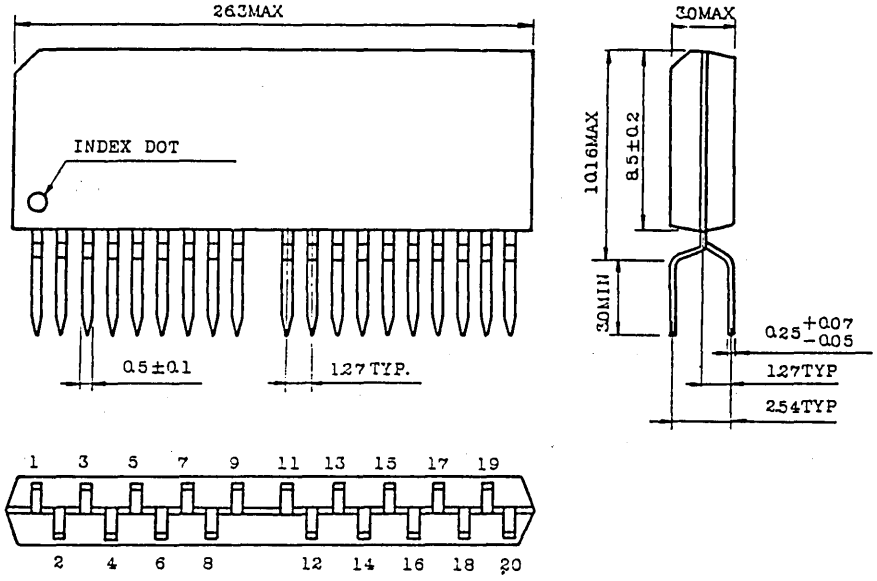


Note: Each lead pitch 1.27mm. All dimensions are in millimeters.

Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 8 BIT
DYNAMIC RAM MODULE

THM81000S/L-10/12

DESCRIPTION

The THM81000S/L is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511000J on the printed circuit board.

The THM81000S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

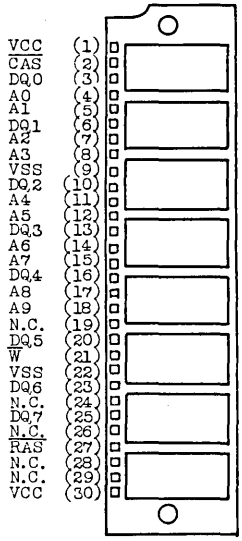
- 1,048,576 words by 8 bits organization
- Fast access time

		THM81000S/L-10	THM81000S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	35ns	45ns
t_{RC}	Cycle Time	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	55ns	70ns

- Single power supply of 5V±10%
- Low power
  2,640mW MAX. Operating (THM81000S/L-10)
  2,200mW MAX. Operating (THM81000S/L-12)
  44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

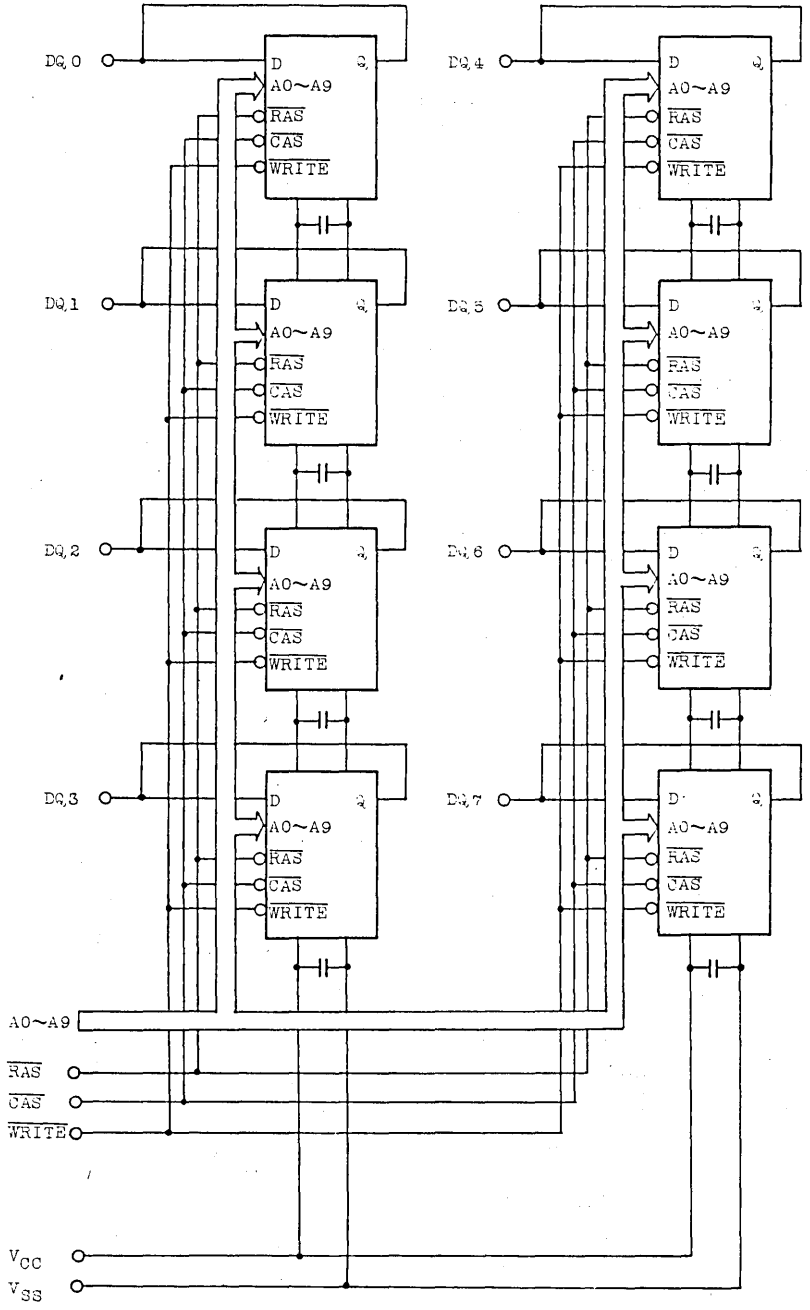
(TOP VIEW)



PIN NAMES

A0 ∿ 9	Address Inputs
DQ0 ∿ 7	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature . Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	-1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM81000S/L-10	-	480	mA	3, 4
		THM81000S/L-12	-	400		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM81000S/L-10	-	480	mA	3
		THM81000S/L-12	-	400		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC}=t_{PC} MIN.)	THM81000S/L-10	-	320	mA	3, 4
		THM81000S/L-12	-	240		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM81000S/L-10	-	480	mA	3
		THM81000S/L-12	-	400		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81000S/L-10		THM81000S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190		220		ns	
t_{PC}	Fast Page Mode Cycle Time	55		70		ns	
t_{RAC}	Access Time from $\overline{RAS}$		100		120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$		35		45	ns	8, 13
t_{AA}	Access Time from Column Address		50		60	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		50		65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5		5		ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80		90		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	35		45		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100		120		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	35		45		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	65	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		15		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	20		25		ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	50		60		ns	
t_{RCS}	Read Command Set-Up Time	0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		ns	10

ELECTRICAL CHARACTERISTIC AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM81000S/L-10		THM81000S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0		ns	10
t_{WCH}	Write Command Hold Time	20		25		ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{WP}	Write Command Pulse Width	20		25		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25		30		ns	
t_{DS}	Data Set-Up Time	0		0		ns	11
t_{DH}	Data Hold Time	20		25		ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{REF}	Refresh Period		8		8	ms	
t_{WCS}	Write Command Set-Up Time	0		0		ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30		30		ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50		60		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15		20		ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)		60	pF
C_{DQ}	I/O Capacitance (DQ0 ∿ DQ7)		15	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

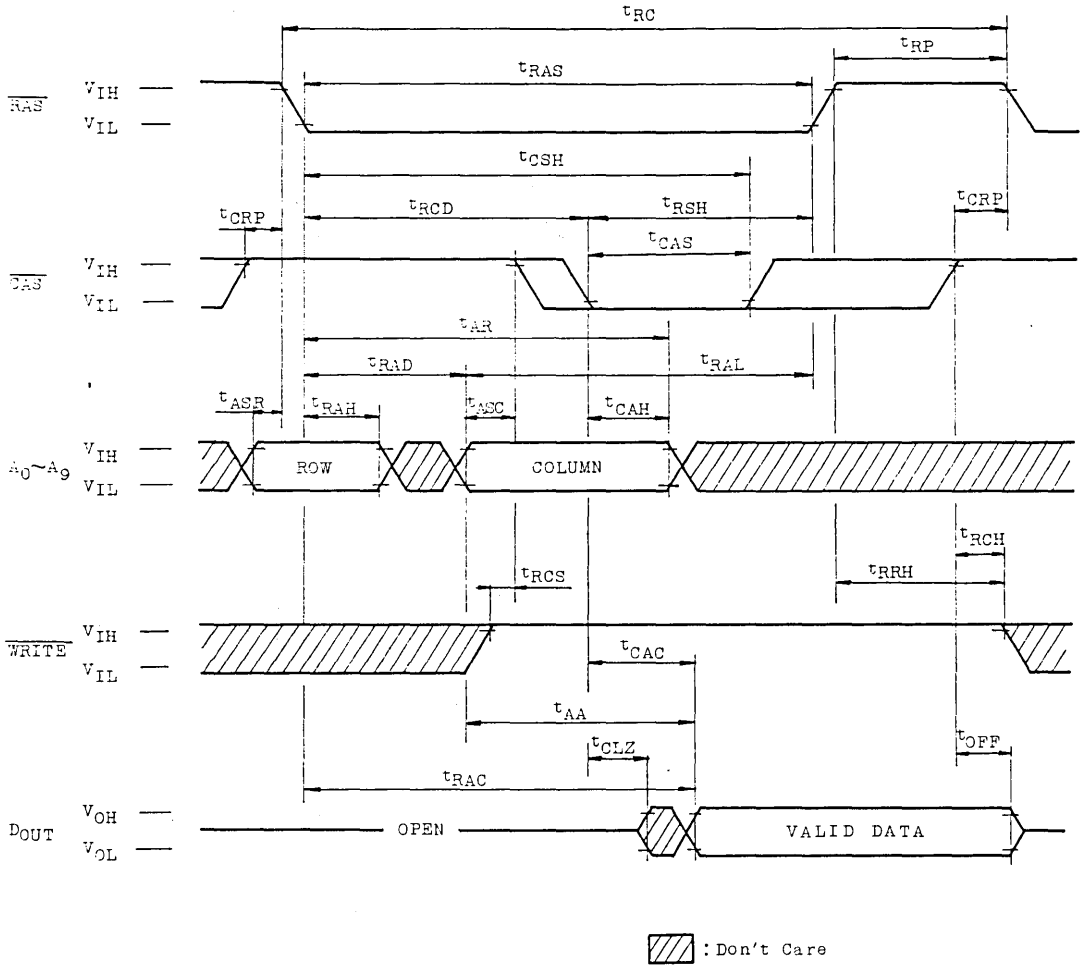
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.

12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

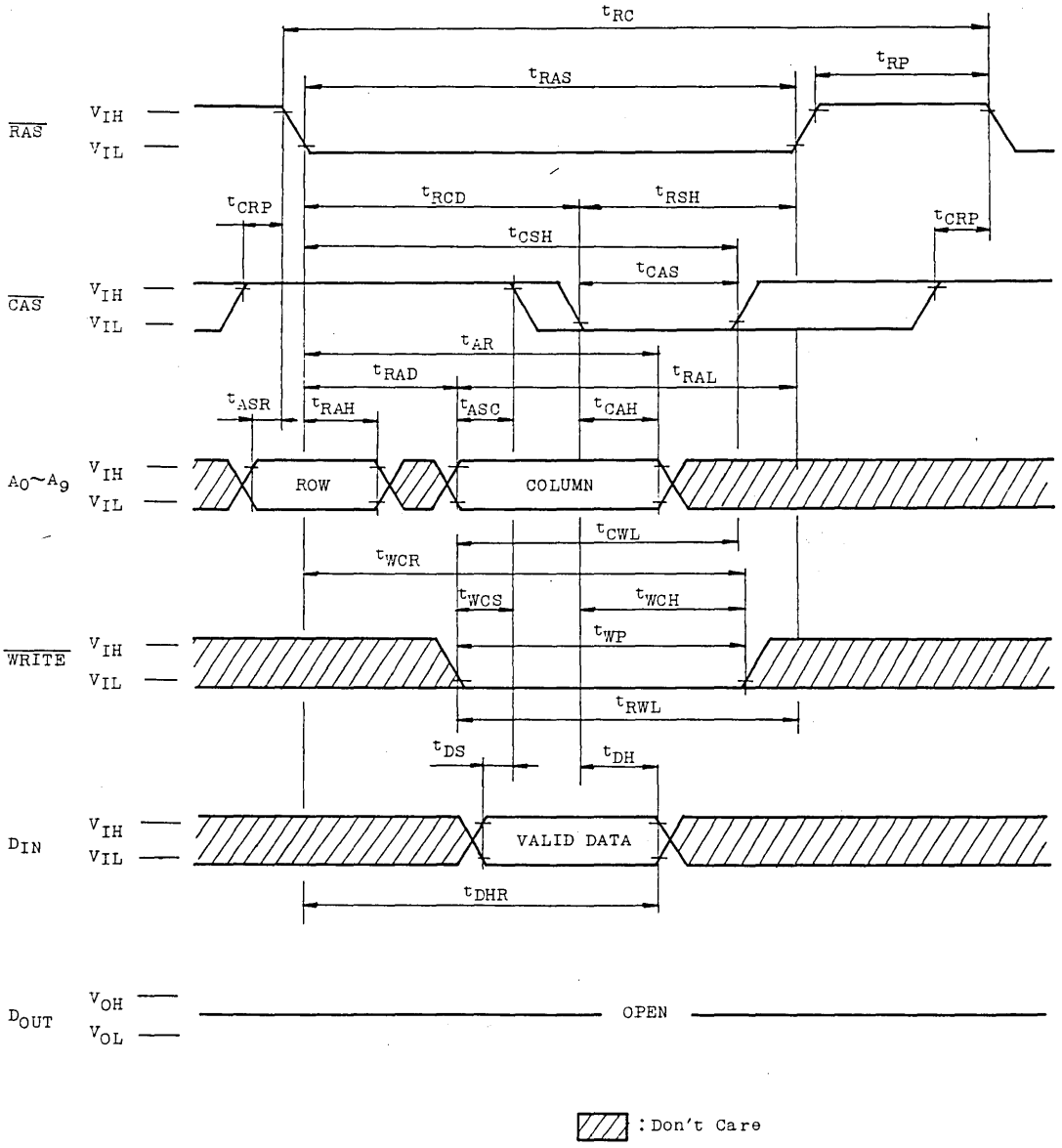
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

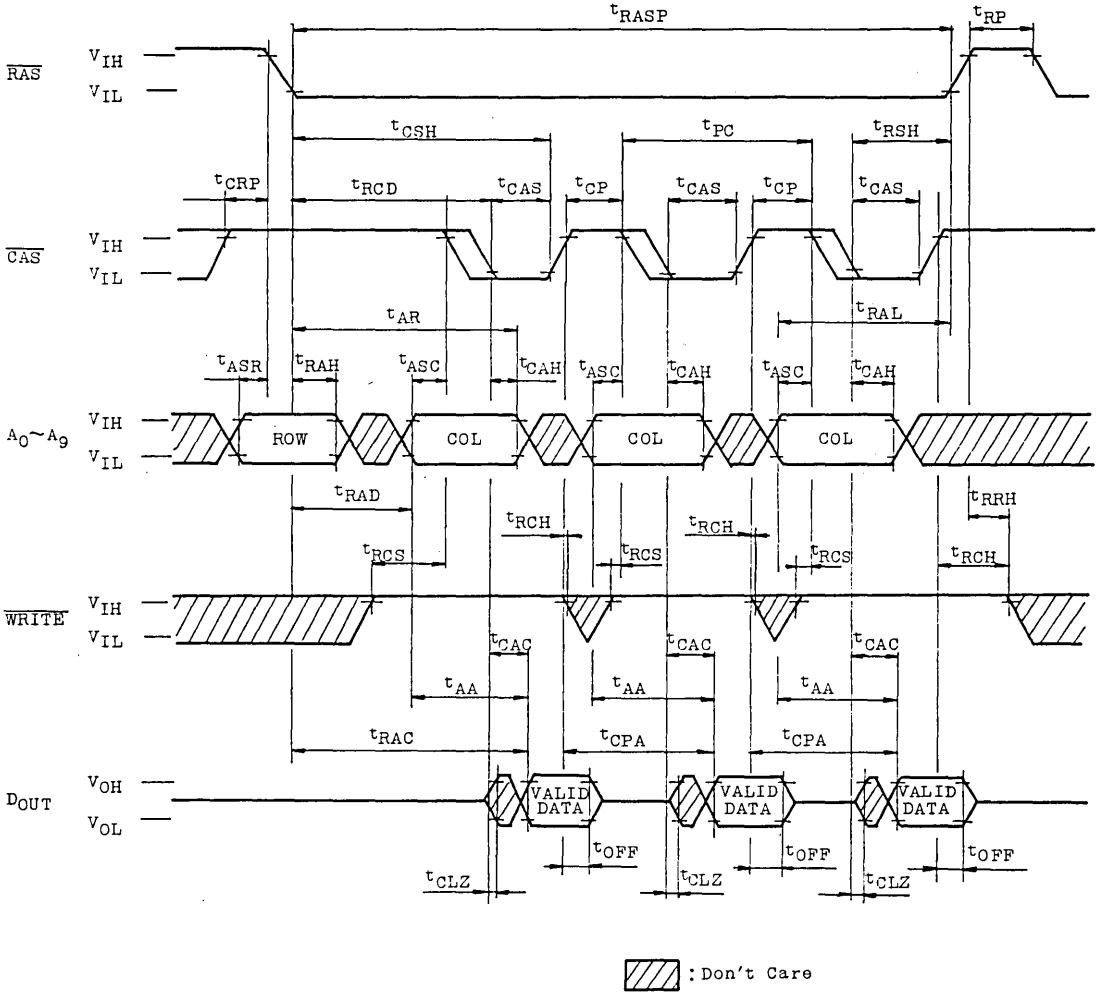
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
VIH
VIL
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
VIH
VIL
tCAC
tAA
tOFF
tCLZ
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: Don't Care

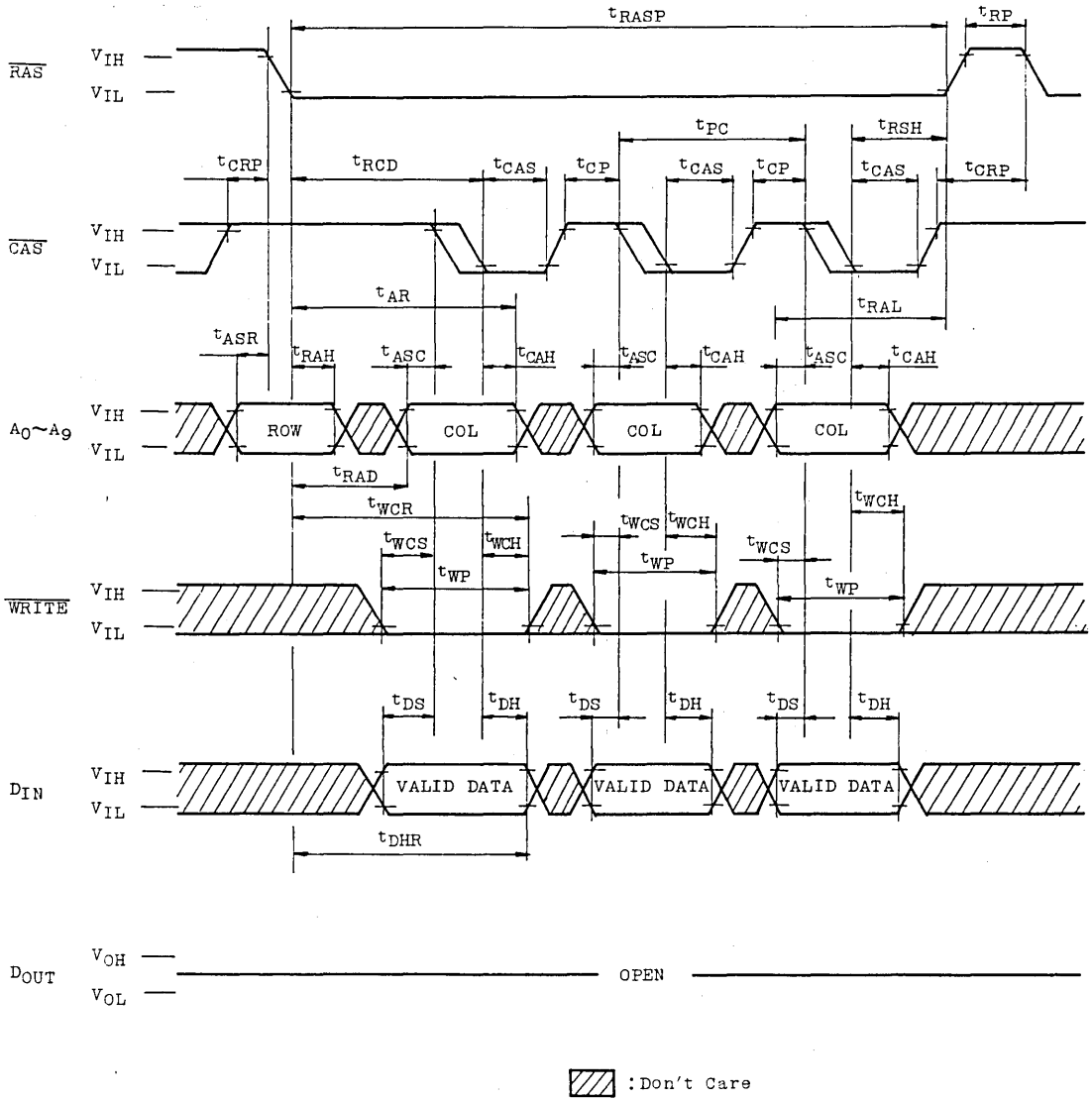
EARLY WRITE CYCLE



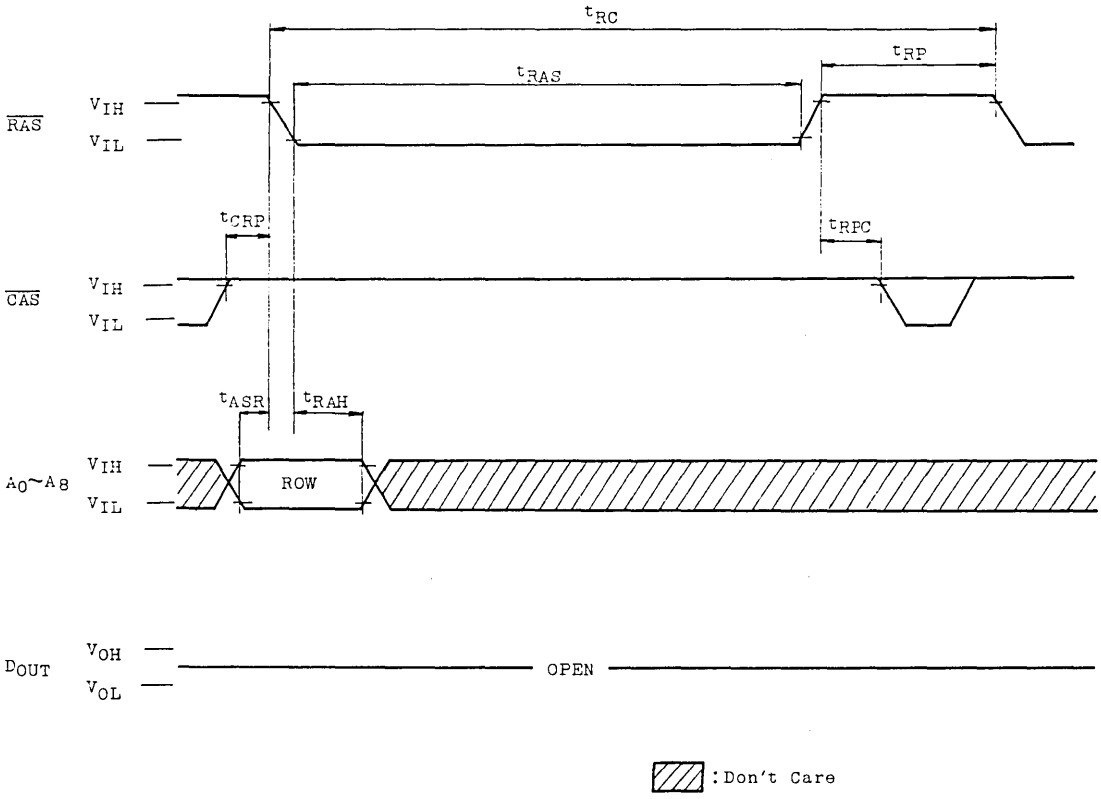
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

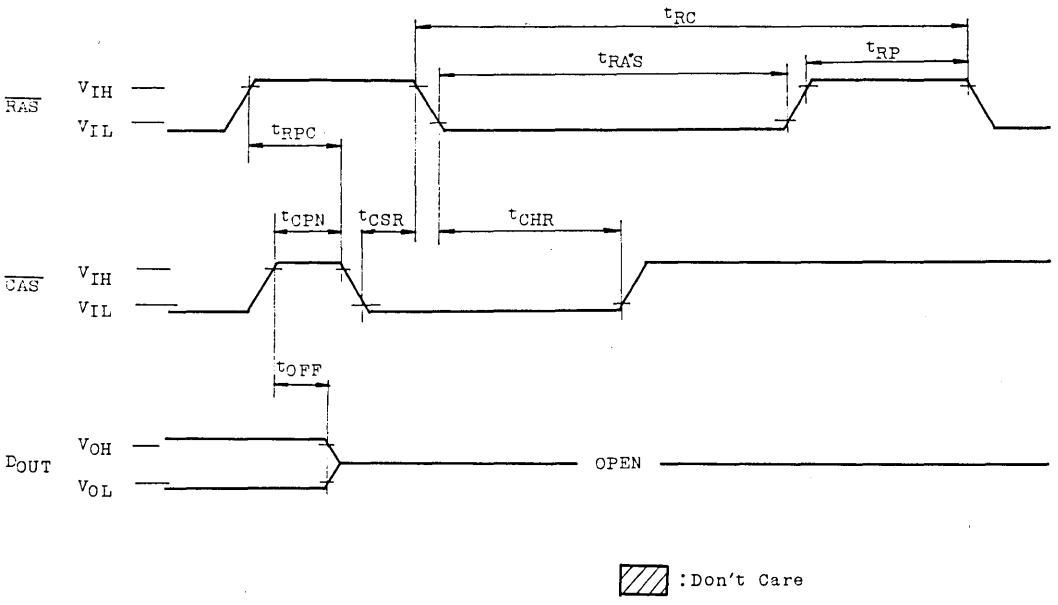


$\overline{RAS}$ ONLY REFRESH CYCLE



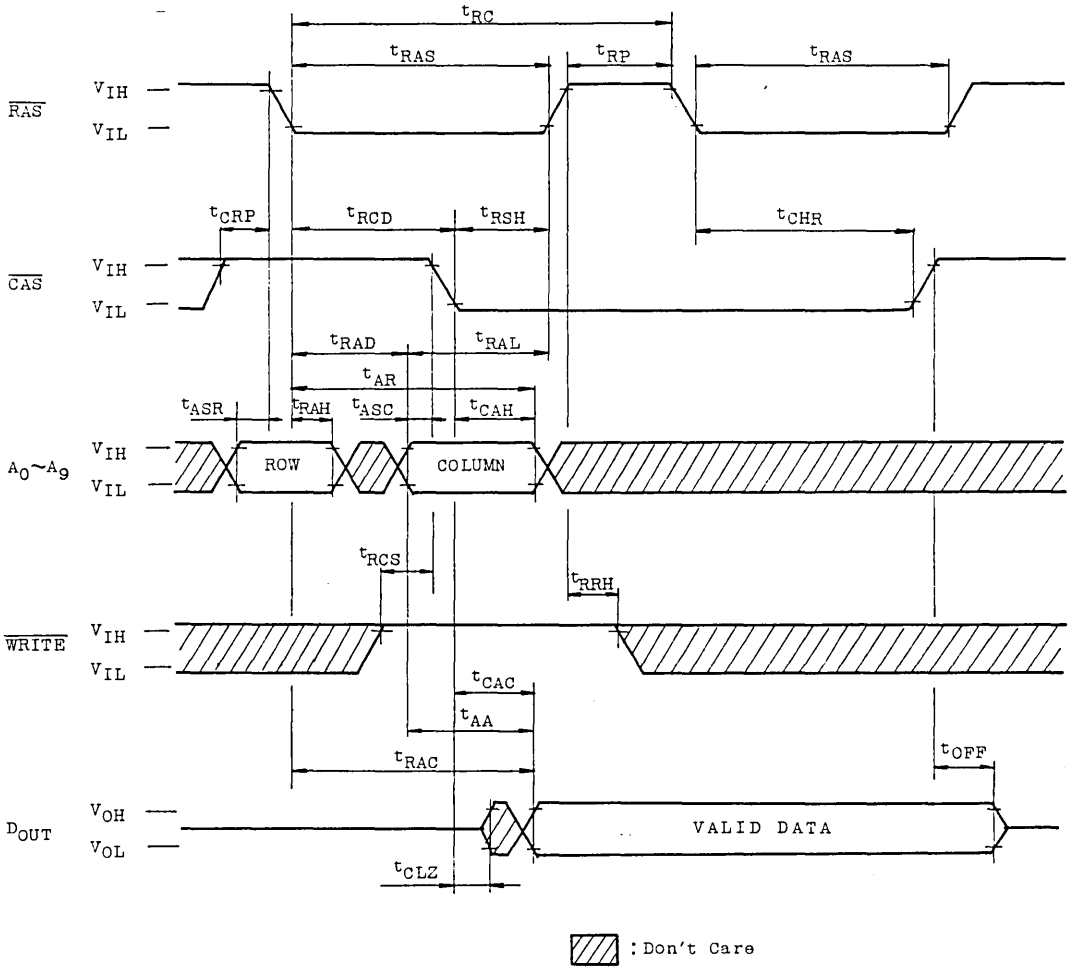
Note: $\overline{WRITE}$=Don't care, A9=Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

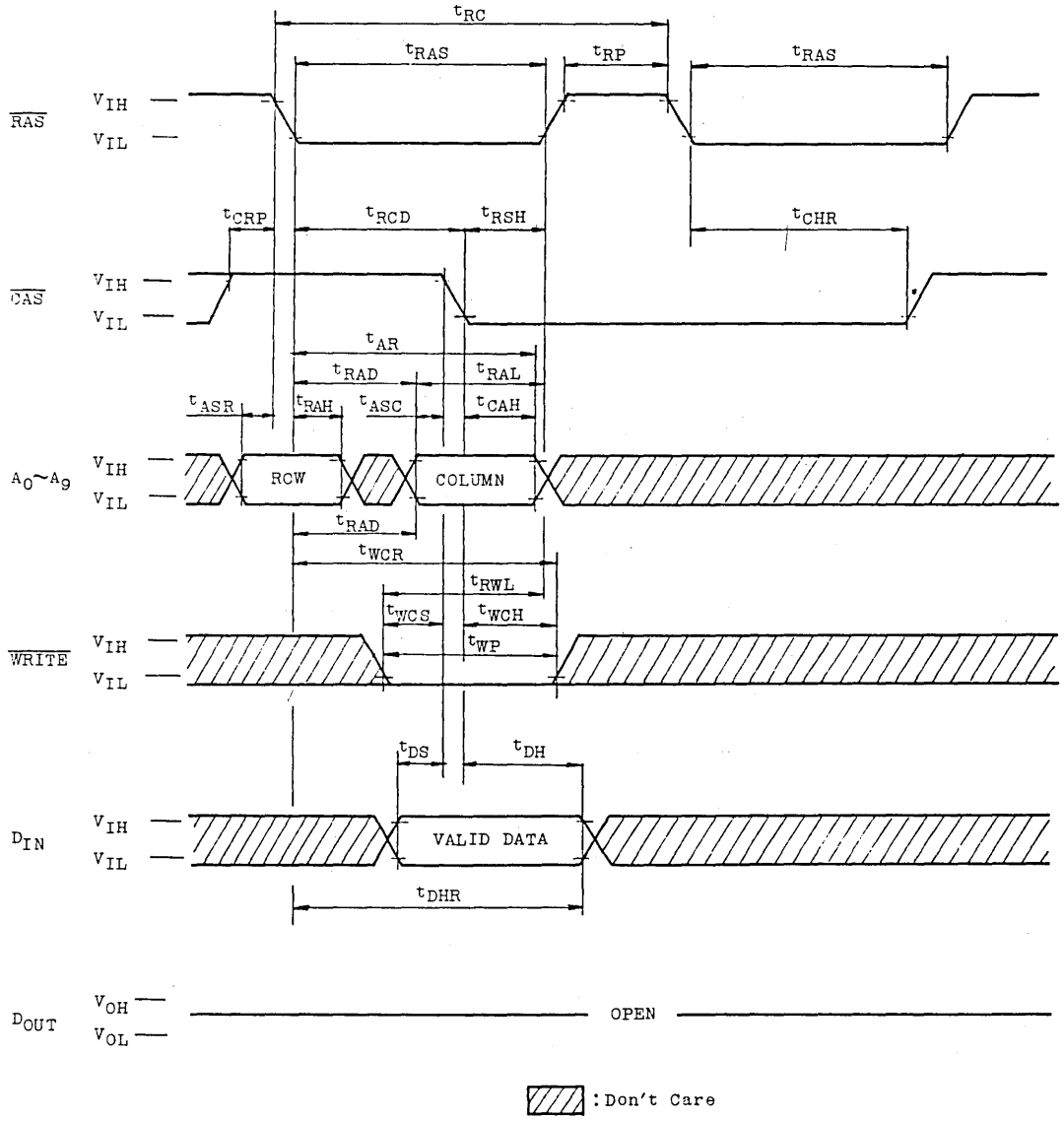


Note: $\overline{WRITE}$=Don't care, A0 ∿ A9=Don't care

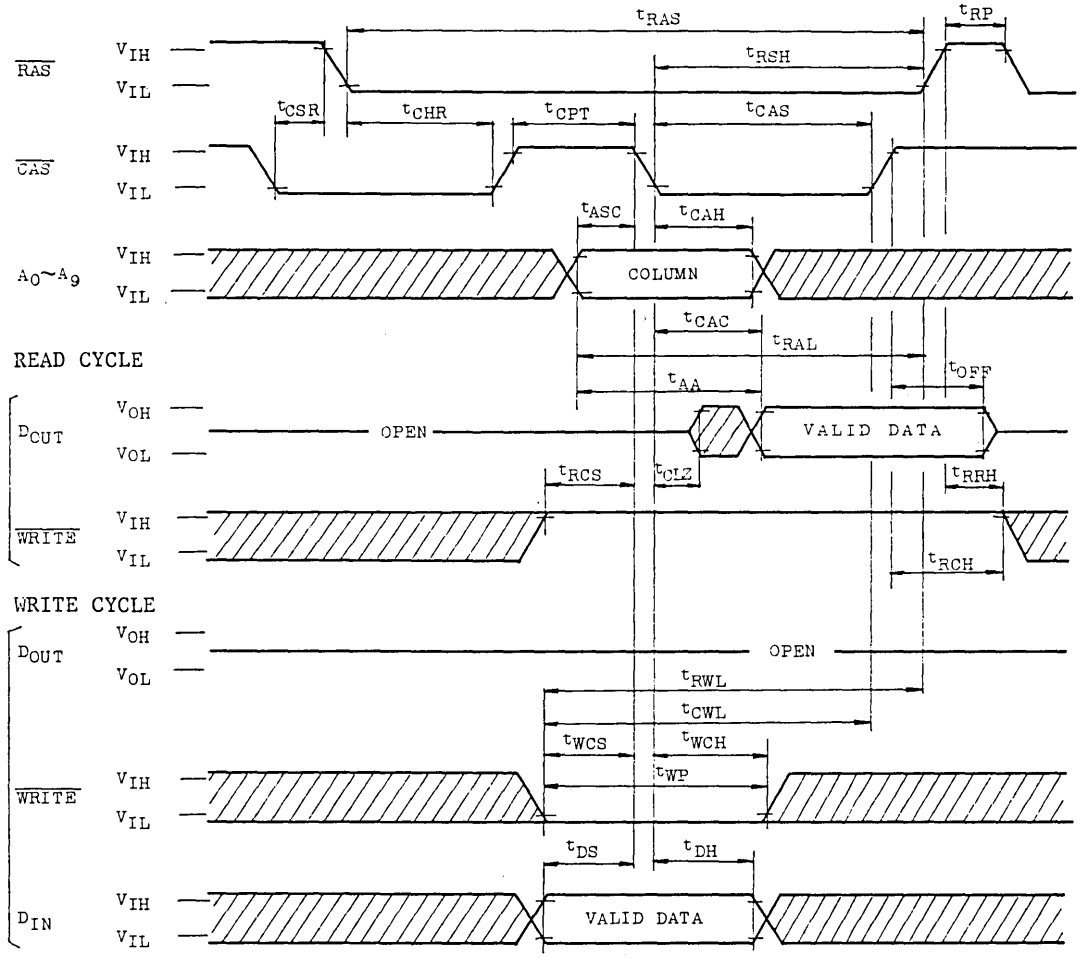
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



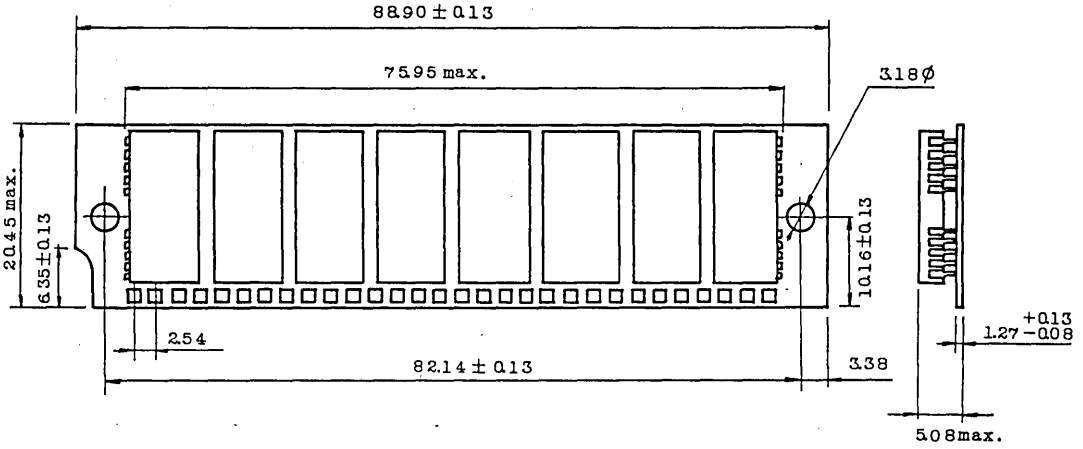
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



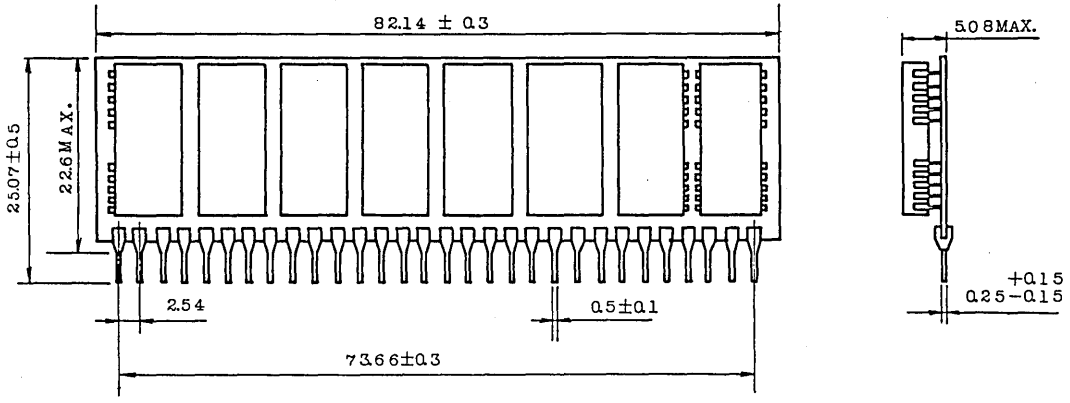
OUTLINE DRAWINGS

• THM81000S

Unit in mm



• THM81000L



TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 9 BIT
DYNAMIC RAM MODULE

THM91000S/L-10/12

DESCRIPTION

The THM91000S/L is a 1,048,576 words by 9 bits dynamic RAM module which assembled 9 pcs of TC511000J on the printed circuit board.

The THM91000S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

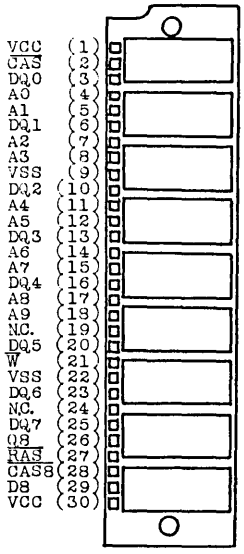
- 1,048,576 words by 9 bits organization
- Fast access time

		THM91000S/L-10	THM91000S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	35ns	45ns
t_{RC}	Cycle Time	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	55ns	70ns

- Single power supply of 5V±10%
- Low power
  2,970 mW MAX. Operating (THM91000S/L-10)
  2,475 mW MAX. Operating (THM91000S/L-12)
  49.5 mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

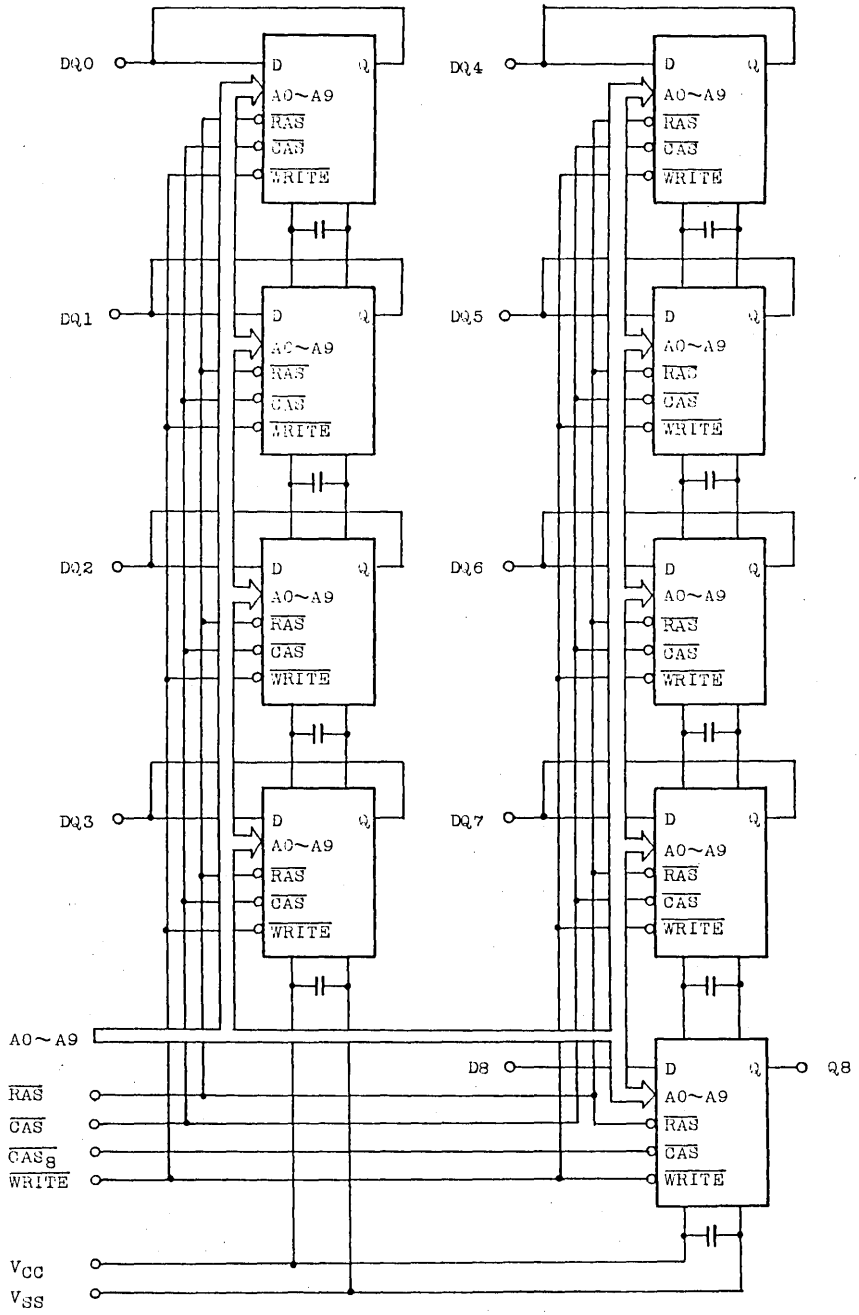
(TOP VIEW)



PIN NAMES

A0 ∿ 9	Address Inputs
DQ0 ∿ 7	Data Input/Outputs
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	-1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM91000S/L-10	-	540	mA	3, 4
		THM91000S/L-12	-	450		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM91000S/L-10	-	540	mA	3
		THM91000S/L-12	-	450		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC}=t_{PC} MIN.)	THM91000S/L-10	-	360	mA	3, 4
		THM91000S/L-12	-	270		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM91000S/L-10	-	540	mA	3
		THM91000S/L-12	-	450		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM91000S/L-10		THM91000S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190		220		ns	
t_{PC}	Fast Page Mode Cycle Time	55		70		ns	
t_{RAC}	Access Time from $\overline{RAS}$		100		120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$		35		45	ns	8, 13
t_{AA}	Access Time from Column Address		50		60	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		50		65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5		5		ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80		90		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	35		45		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100		120		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	35		45		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	65	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		15		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	20		25		ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	50		60		ns	
t_{RCS}	Read Command Set-Up Time	0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0		ns	10

ELECTRICAL CHARACTERISTIC AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM91000S/L-10		THM91000S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WCH}	Write Command Hold Time	20		25		ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{WP}	Write Command Pulse Width	20		25		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25		30		ns	
t_{DS}	Data Set-Up Time	0		0		ns	11
t_{DH}	Data Hold Time	20		25		ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{REF}	Refresh Period		8		8	ms	
t_{WCS}	Write Command Set-Up Time	0		0		ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30		30		ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50		60		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15		20		ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)		60	pF
C_{I2}	Input Capacitance (D8, $\overline{CAS8}$)		7	pF
C_{DQ}	I/O Capacitance (DQ0 ∿ DQ7)		15	pF
C_{Q}	Output Capacitance (Q8)		10	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

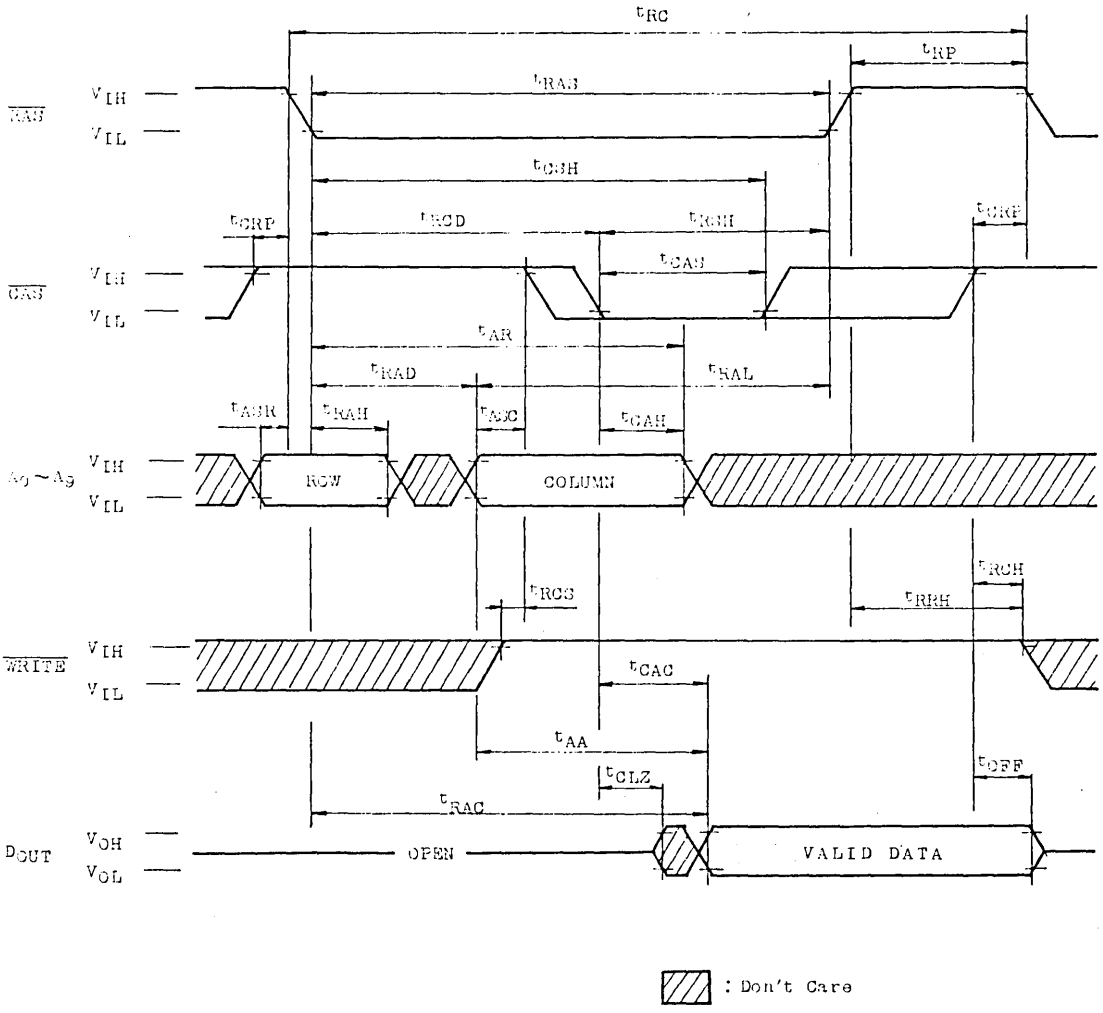
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.

12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

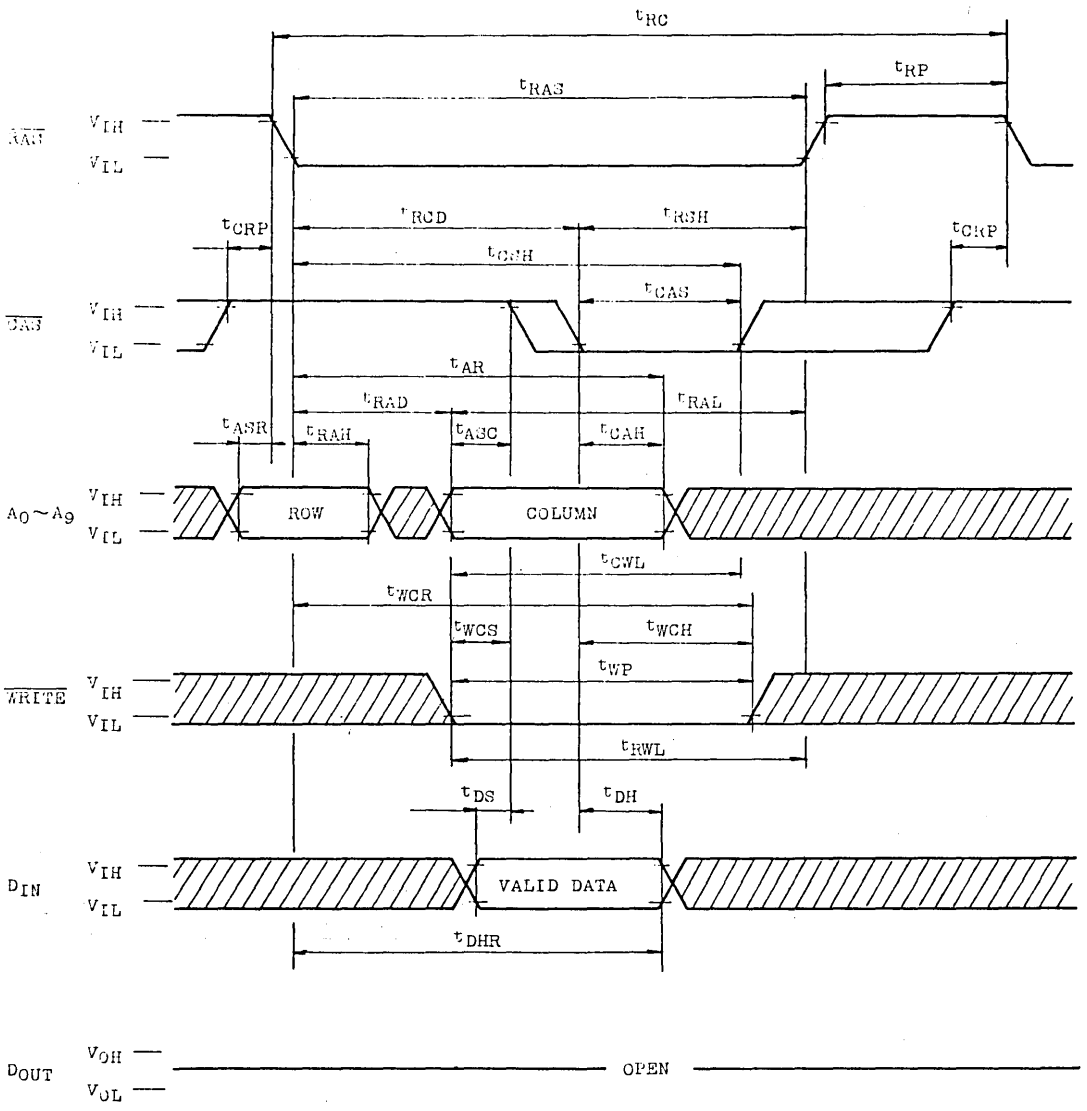
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

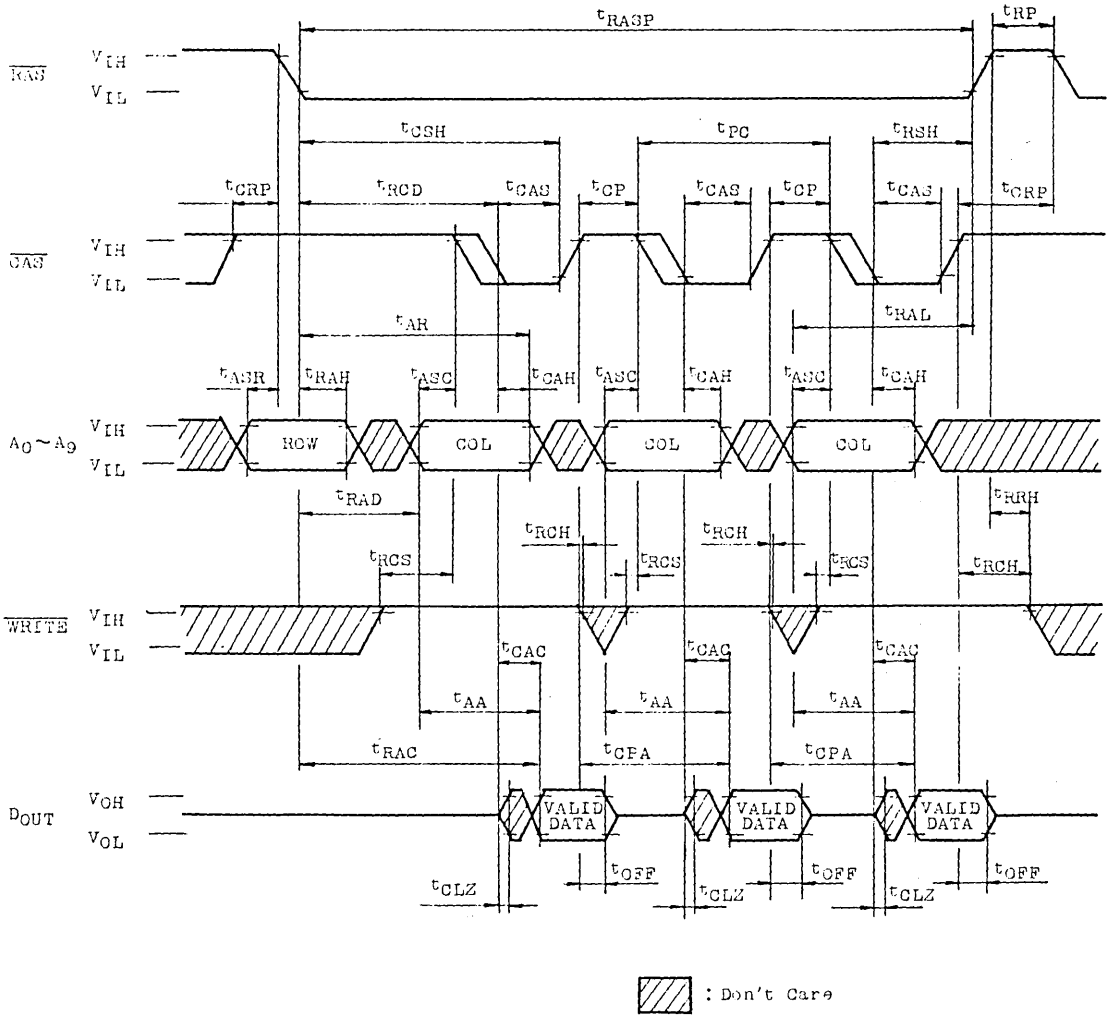
READ CYCLE


tRC
tRP
tRAS
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
ROW
COLUMN
tRCS
tRCH
tRRH
tCAC
tAA
tCLZ
tOFF
tRAC
OPEN
VALID DATA
RAS
CAS
WRITE
A0 ~ A9
DOUT
VIH
VIL
VOH
VOL
: Don't Care

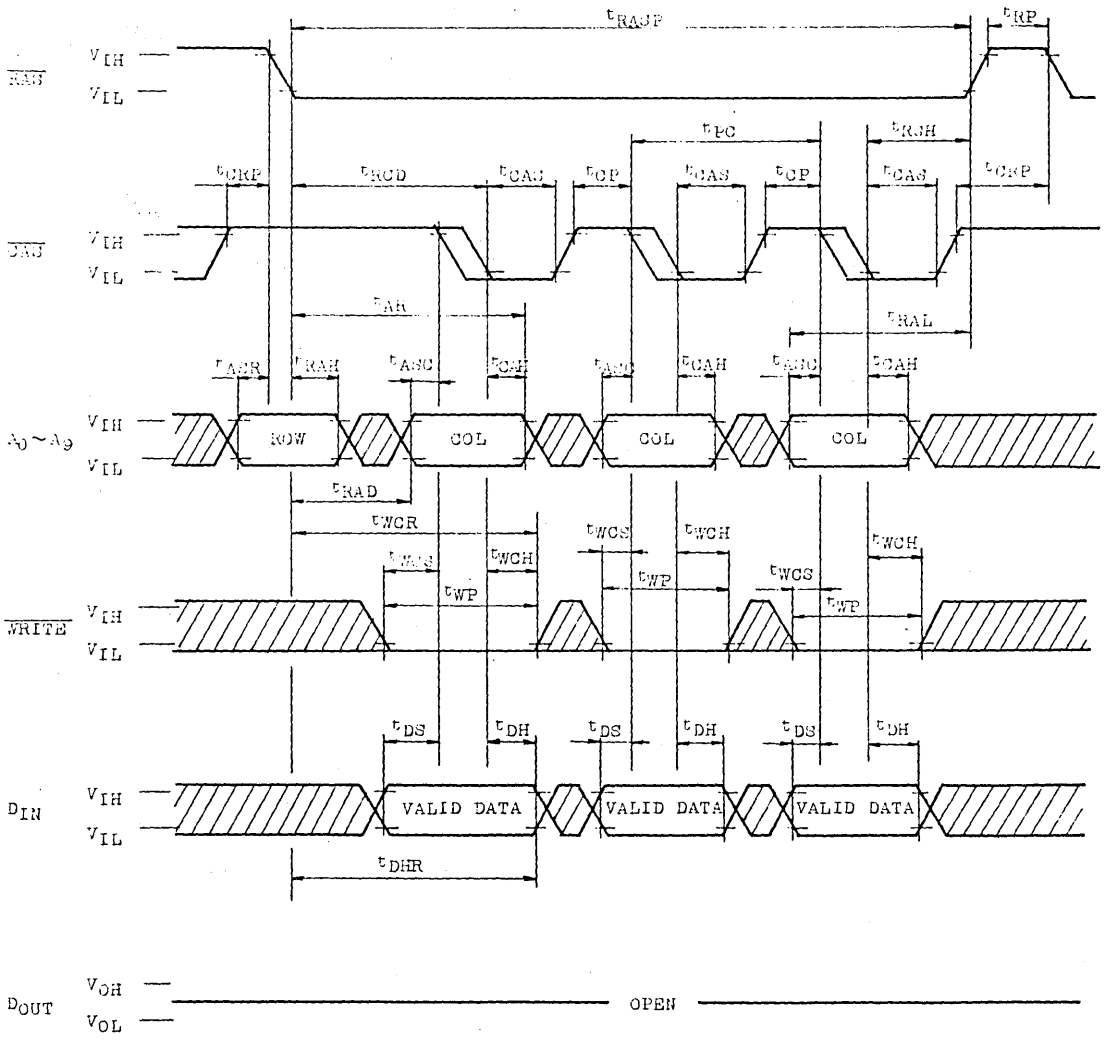
EARLY WRITE CYCLE



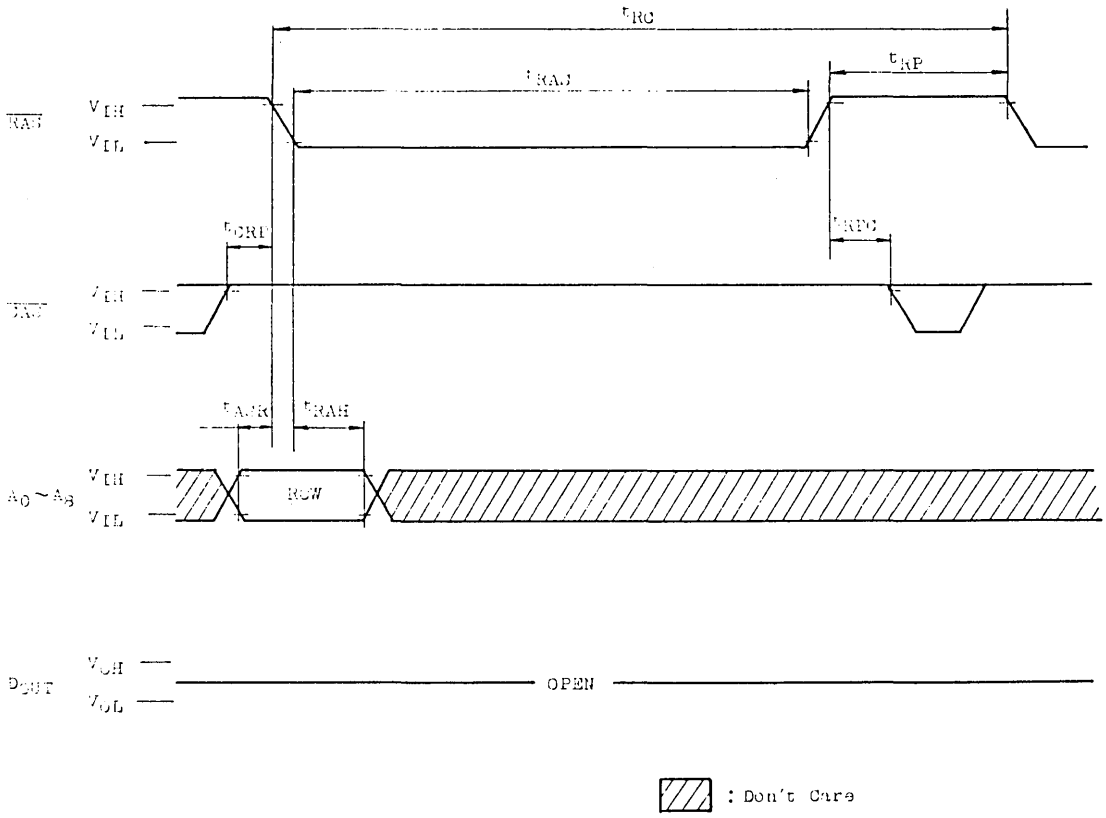
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

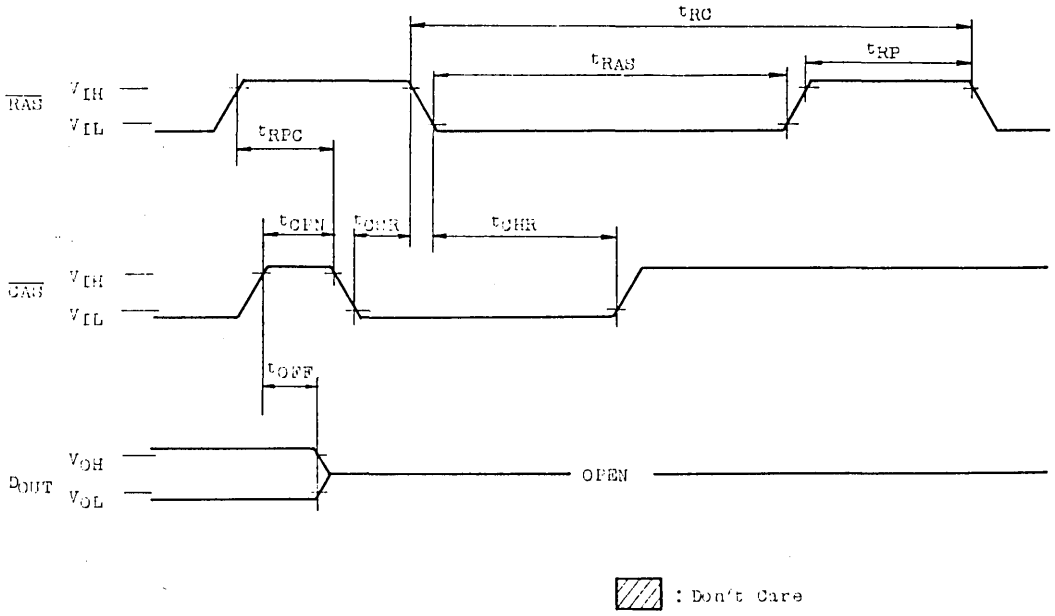


$\overline{RAS}$ ONLY REFRESH CYCLE



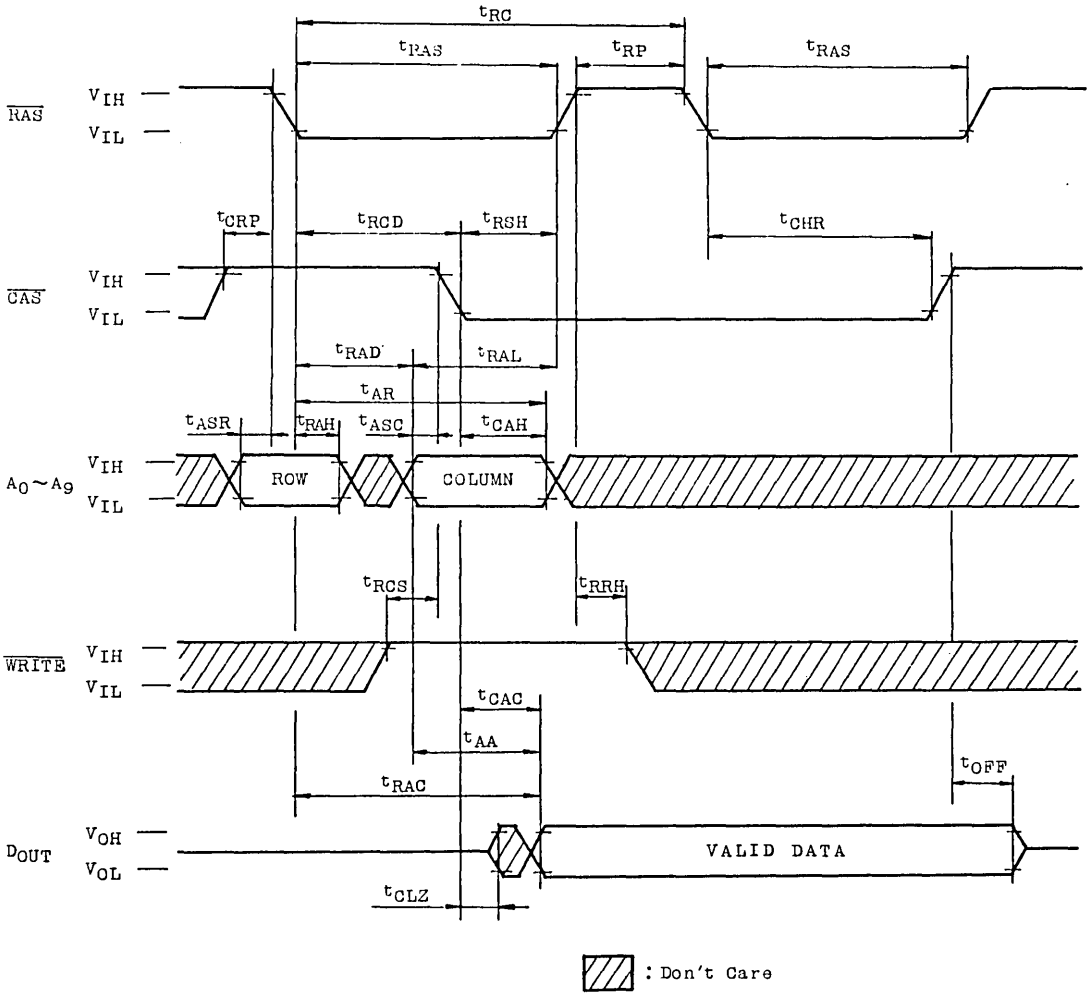
Note: $\overline{WRITE}$=Don't care, A9=Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

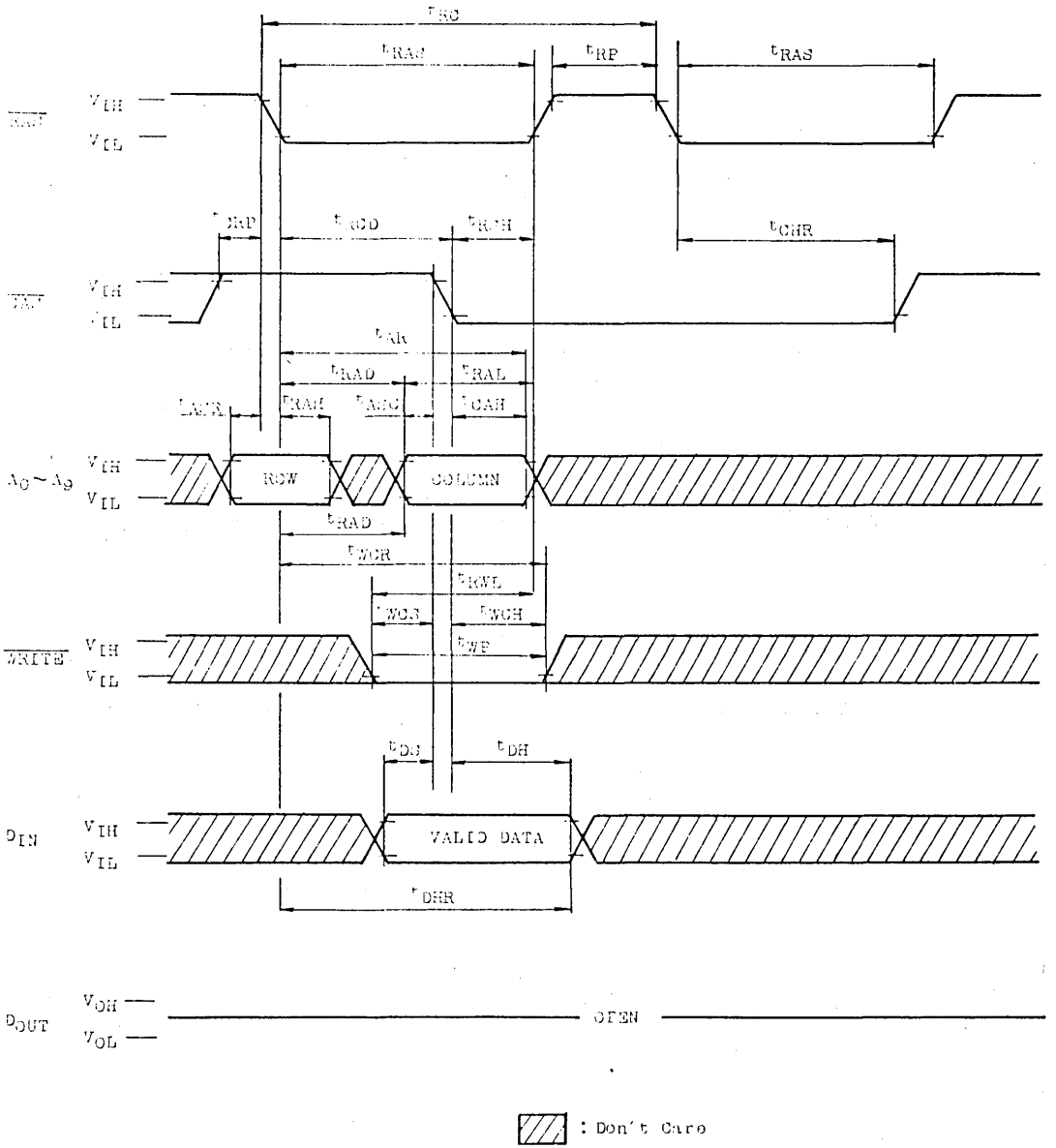


Note: $\overline{WRITE}$=Don't care, A0 ∿ A9=Don't care

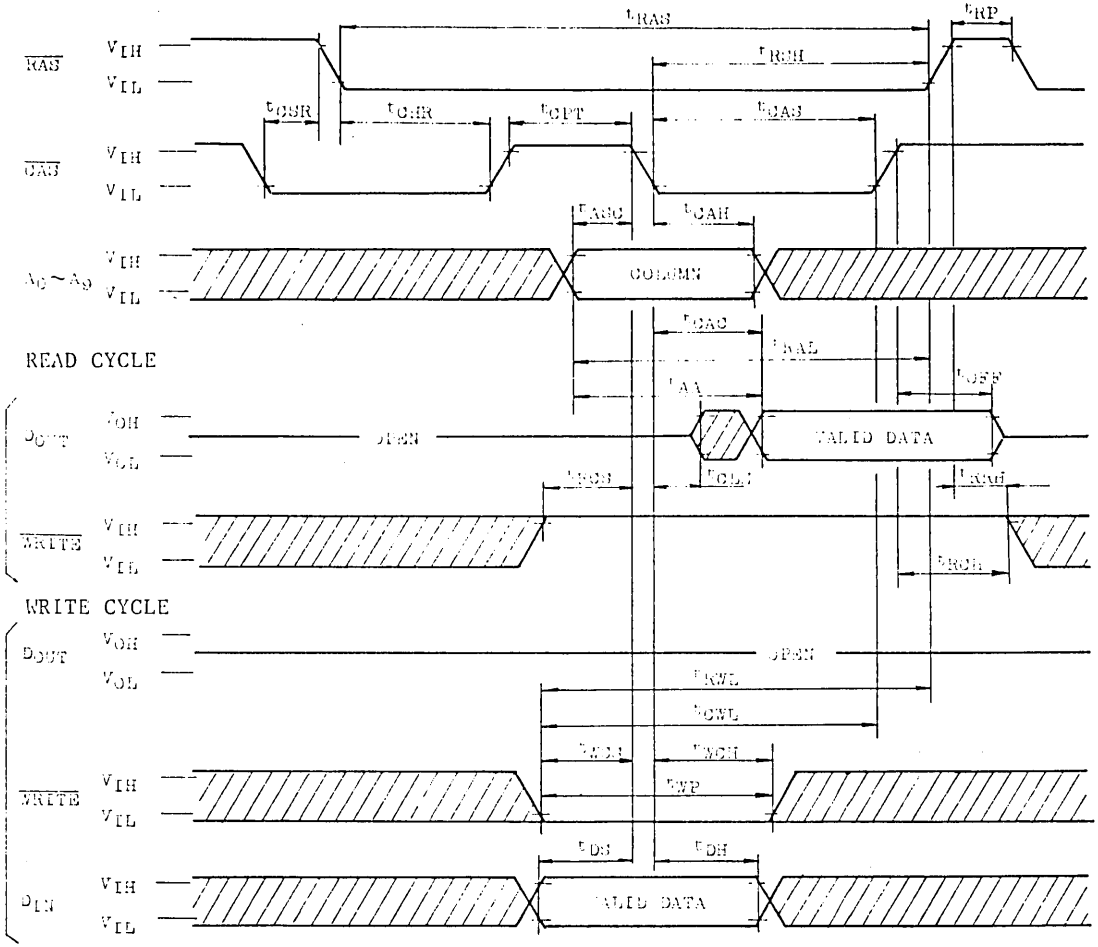
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



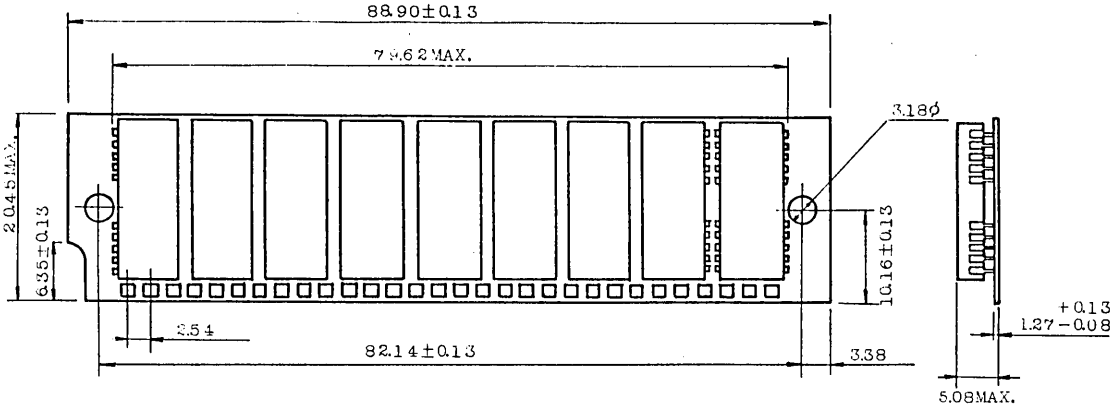
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



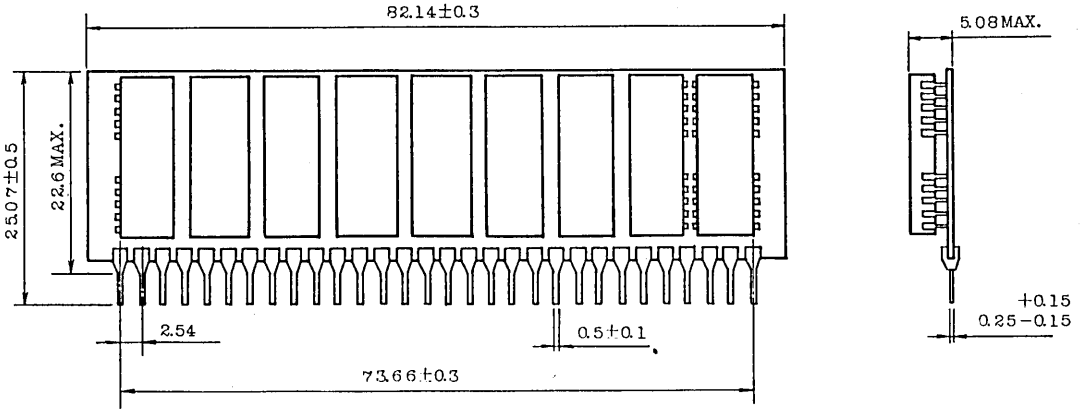
OUTLINE DRAWINGS

• THM91000S

Unit in mm



• THM91000L



Standard Application Static RAMs

TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2015BP-90, TMM2015BP-12
TMM2015BP-10, TMM2015BP-15

DESCRIPTION

The TMM2015BP is a 16, 384 bits high speed and low power static random access memory organized as 2, 048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 50mA. When $\overline{CS}$ is a logical high, the device is placed in a low power standby mode in which maximum standby current is 5mA. Thus the TMM2015BP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2015BP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability

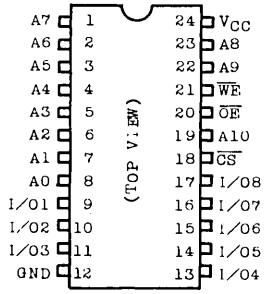
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2015BP-90	90ns	50mA	5mA
TMM2015BP-10	100ns	50mA	5mA
TMM2015BP-12	120ns	50mA	5mA
TMM2015BP-15	150ns	50mA	5mA

- High Density Assembly Capability
  0.3 inch width package (24pin plastic DIP)
- Single 5V power Supply
- Fully Static Operation
- Power Down Feature: $\overline{CS}$
- Output Buffer Control: $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

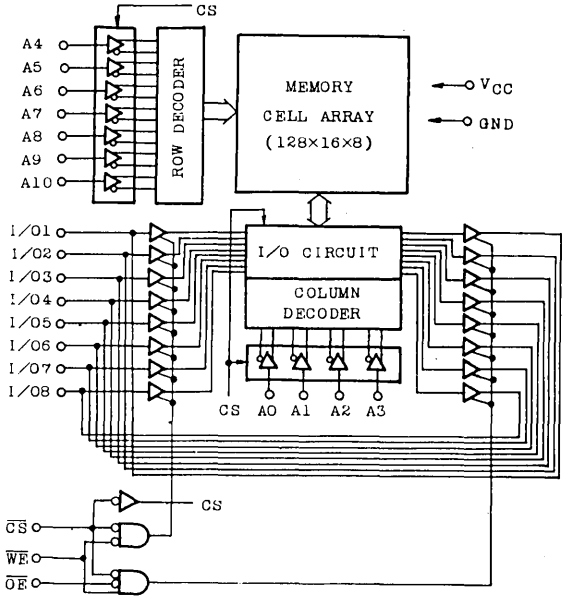
PIN CONNENCTION



PIN NAMES

$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_{10}$	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Terperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation(Ta=70°C)	0.7	W

* −3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Vovtage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=4.0mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, I_{OUT}=0mA	—	—	10	mA
I_{SB}	Standby Current	$\overline{CS}$=V_{IH} , I_{OUT}=0mA	—	—	5	mA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}, I_{OUT}=0mA	—	—	50	mA

CAPACITANCE*** (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=OV	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=OV	10	pF

*** Note : This paramenter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2015BP-90		TMM2015BP-10		TMM2015BP-12		TMM2015BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	90	—	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	90	—	100	—	120	—	150	
t_{CO}	Chip Select Access Time	—	90	—	100	—	120	—	150	
t_{OE}	Output Enable Time	—	35	—	35	—	50	—	55	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	15	—	15	—	15	—	15	—	
t_{CHZ}	$\overline{CS}$ to Output in High-Z	—	40	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	35	—	50	
t_{PU}	Chip Selection to power Up Time	0	—	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	50	—	60	—	60	

Write Cycle

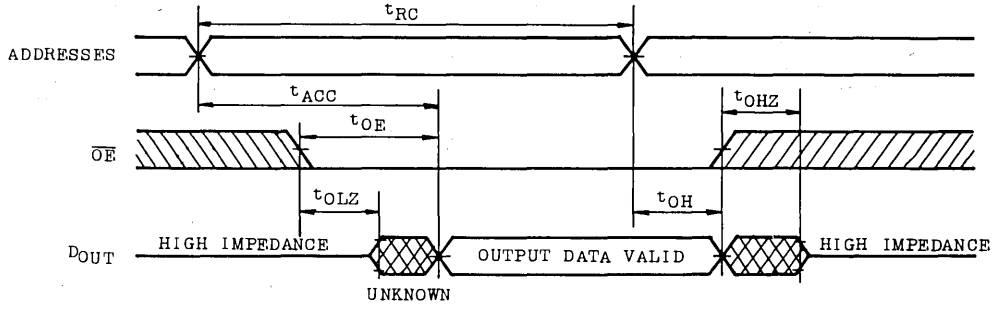
SYMBOL	PARAMETER	TMM2015BP-90		TMM2015BP-10		TMM2015BP-12		TMM2015BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	90	—	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	60	—	70	—	85	—	100	—	
t_{AS}	Address Set Up Time	20	—	20	—	20	—	20	—	
t_{WP}	Write Pulse Width	55	—	65	—	80	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	30	—	35	—	45	—	50	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	25	—	30	—	35	—	50	

A. C. TEST CONDITIONS

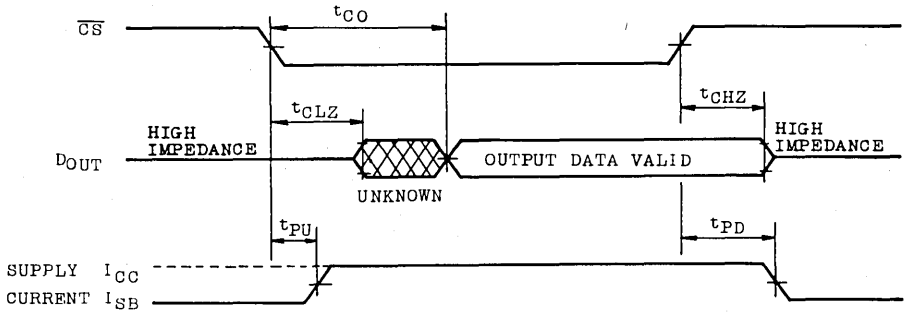
Input Pulse Levels	0~3.5V
Input Rise and Fall Time	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate & C_L=100pF

TIMING WAVEFORMS

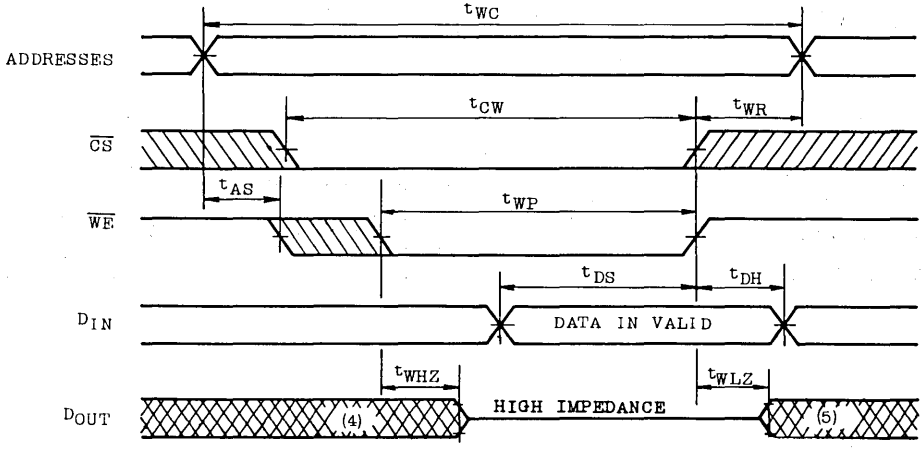
- (A) READ CYCLE [1] (1)



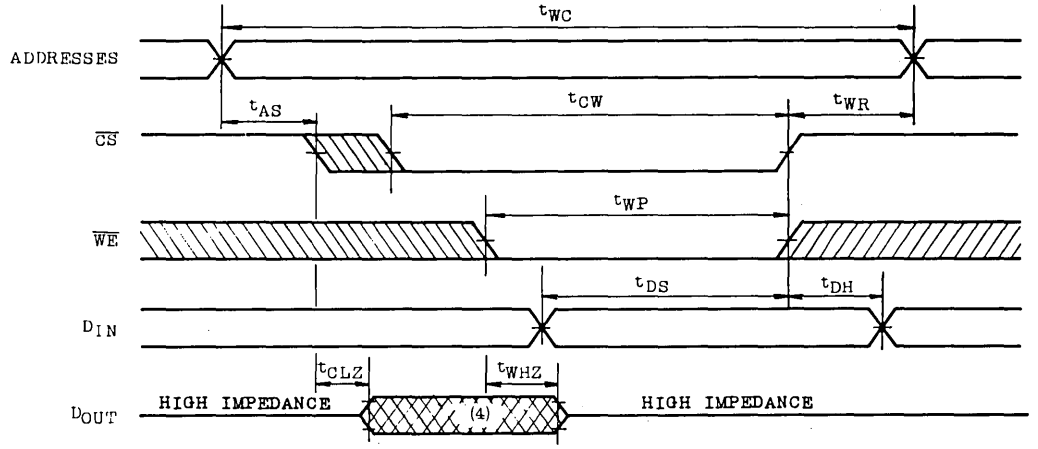
- (B) READ CYCLE [2] (1), (2)



- (C) WRITE CYCLE [1] (3)



- (D) WRITE CYCLE (2) (3)



NOTES:

(1) The $\overline{WE}$ is high for read cycle.
Device is continuously selected, $\overline{CS}$ = V_{IL} in read cycle (1)

(2) All addresses are valid perior to or simultaneously with $\overline{CS}$ transitions.

(3) A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.
The t_{cw} is specified as the time from the chip selection to end of write in write cycle, and the t_{wp} is specified as the overlap time of low $\overline{CS}$ and low $\overline{WE}$.
$\overline{OE}$ is allowed to be low or high level in write cycle.
If the $\overline{OE}$ is high, the output buffers remain in a high impedance state in this period.

(4) If the $\overline{CS}$ low transition occurs simultaneously with or latter to the $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

(5) If the $\overline{CS}$ high transition occurs simultaneously with $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time

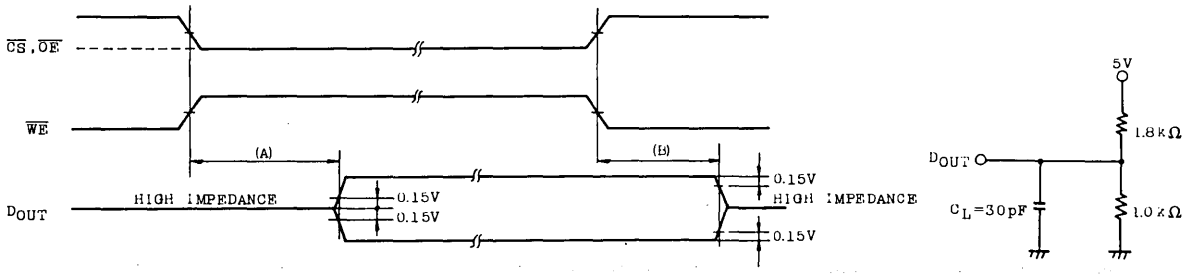
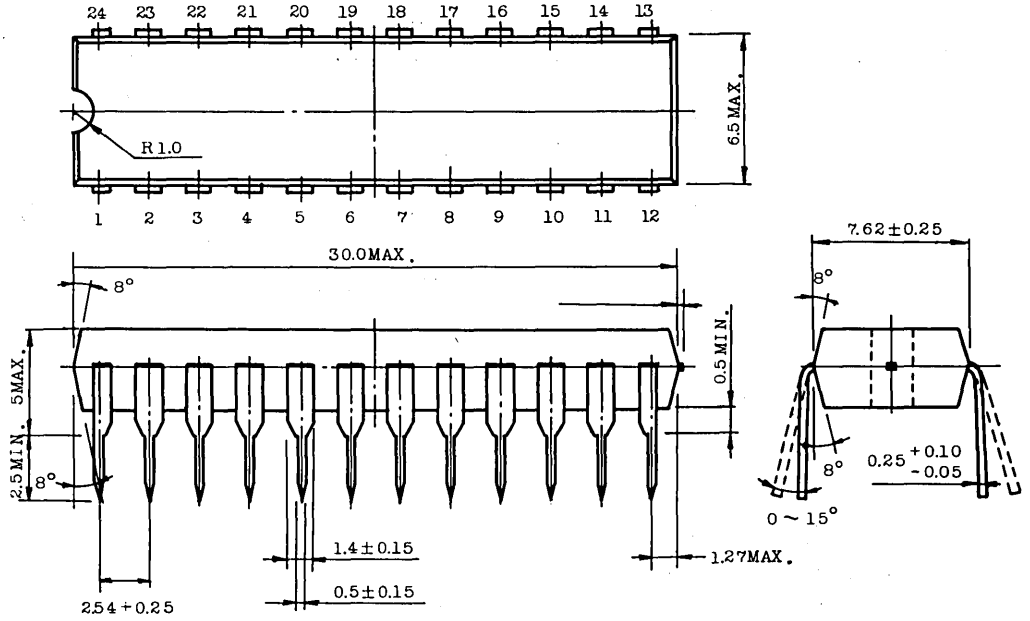


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT STATIC RAM **TMM2016BP-90, TMM2016BP-12**
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS **TMM2016BP-10, TMM2016BP-15**

DESCRIPTION

The TMM2016BP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns /120ns/150ns and maximum operating current of 50mA. When $\overline{CS}$ is logical high, the device is placed in a low power standby mode in which maximum standby current is 5mA. Thus the TMM2016BP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2016BP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability

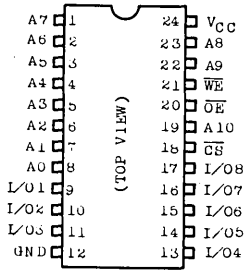
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2016BP-90	90ns	50mA	5mA
TMM2016BP-10	100ns	50mA	5mA
TMM2016BP-12	120ns	50mA	5mA
TMM2016BP-15	150ns	50mA	5mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature $\overline{CS}$
- Output Buffer Control $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge

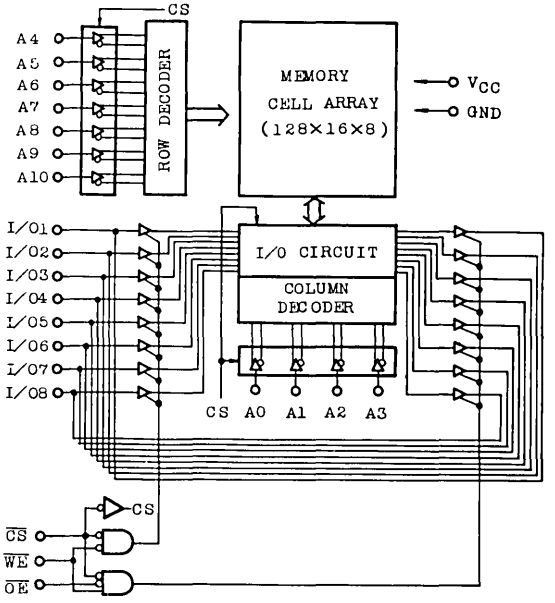
PIN CONNECTION



PIN NAMES

A_0~A_3	Column Address Inputs
A_4~A_{10}	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
I/O_1~I/O_8	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Terperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation(Ta=70°C)	1.0	W

* −3.0V at Pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX.	UNIT
V_{IH}	Input High Vovtage	2 0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0 5**	—	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=4.0mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC} I_{OUT}=0mA	—	—	10	mA
I_{SB}	Standby Current	$\overline{CS}$=V_{IH} I_{OUT}=0mA	—	—	5	mA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL} I_{OUT}=0mA	—	—	50	mA

CAPACITANCE*** (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

*** Note : This paramenter is periodically sampled and is not 100% tested

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2016BP-90		TMM2016BP-10		TMM2016BP-12		TMM2016BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	90	—	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	90	—	100	—	120	—	150	
t_{CO}	Chip Select Access Time	—	90	—	100	—	120	—	150	
t_{OE}	Output Enable Time	—	35	—	35	—	50	—	55	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	15	—	15	—	15	—	15	—	
t_{CHZ}	$\overline{CS}$ to Output in High-Z	—	40	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	35	—	50	
t_{PU}	Chip Selection to power Up Time	0	—	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	50	—	60	—	60	

Write Cycle

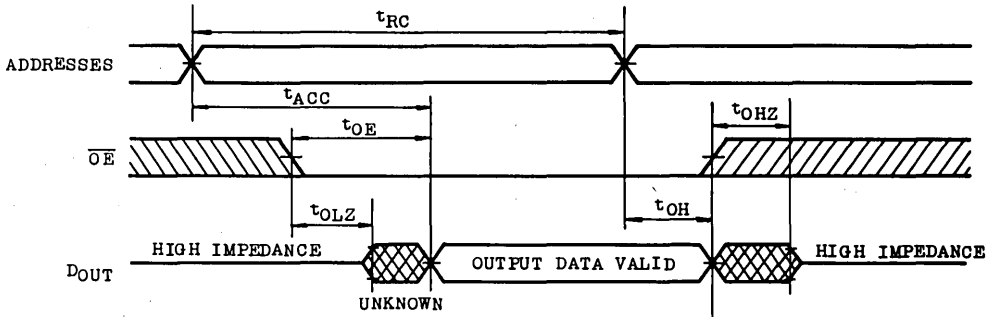
SYMBOL	PARAMETER	TMM2016BP-90		TMM2016BP-10		TMM2016BP-12		TMM2016BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	90	—	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	60	—	70	—	85	—	100	—	
t_{AS}	Address Set Up Time	20	—	20	—	20	—	20	—	
t_{WP}	Write Pulse Width	55	—	65	—	80	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	30	—	35	—	45	—	50	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	25	—	30	—	35	—	50	

A. C. TEST CONDITIONS

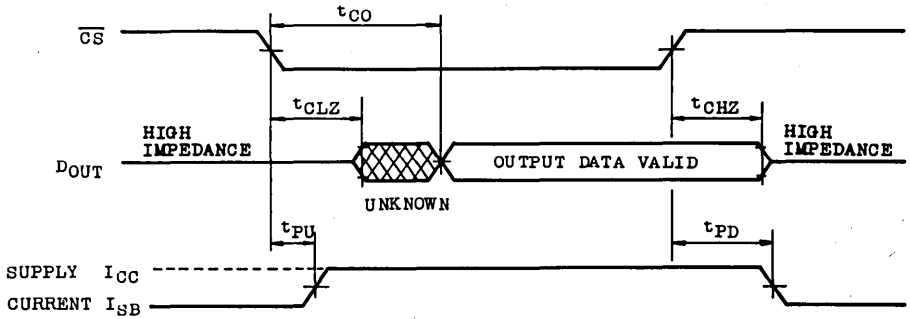
Input Pulse Levels	0~3.5V
Input Rise and Fall Time	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate & C_L=100pF

TIMING WAVEFORMS

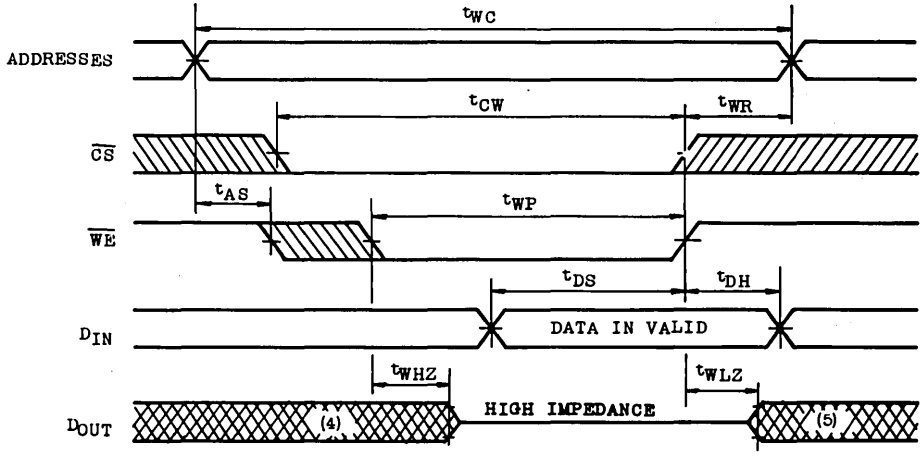
- (A) READ CYCLE [1] (1)



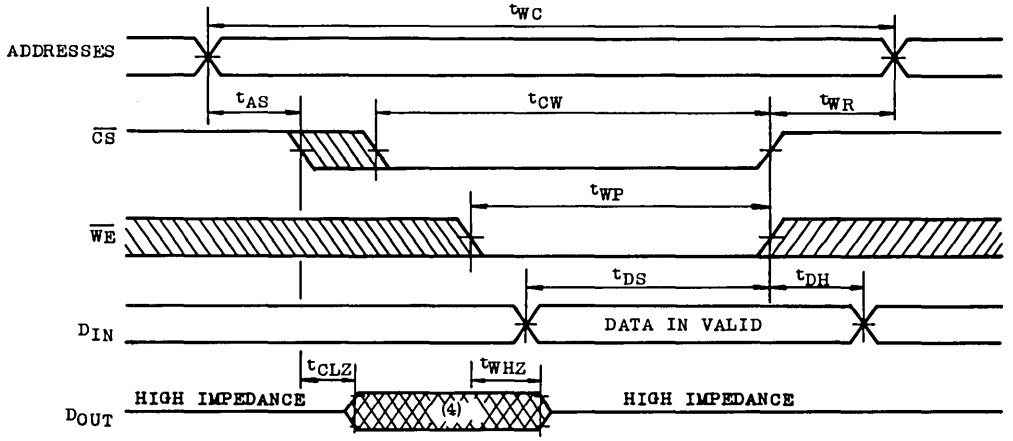
- (B) READ CYCLE [2] (1), (2)



- (C) WRITE CYCLE [1] (3)



- (D) WRITE CYCLE (2) (3)



NOTES:

(1) The $\overline{WE}$ is high for read cycle.
Device is continuously selected, $\overline{CS}=V_{IL}$ in read cycle (1)

(2) All adresses are valid perior to or simultaneously with $\overline{CS}$ transitions.

(3) A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.
The t_{cw} is specified as the time from the chip selection to end of write in write cycle , and the t_{wp} is specified as the overlap time of low $\overline{CS}$ and low $\overline{WE}$.
$\overline{OE}$ is allowed to be low or high level in write cycle.
If the $\overline{OE}$ is high , the output buffers remain in a high impedance state in this period.

(4) If the $\overline{CS}$ low transition occurs simultaneously with or latter to the $\overline{WE}$ low transition, the output buuffers remain in a high impedance state in this period.

(5) If the $\overline{CS}$ high transition occurs simultaeously with $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.

Thease parameters are specified as follows and measured by using the load shown in Fig. 1

(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time

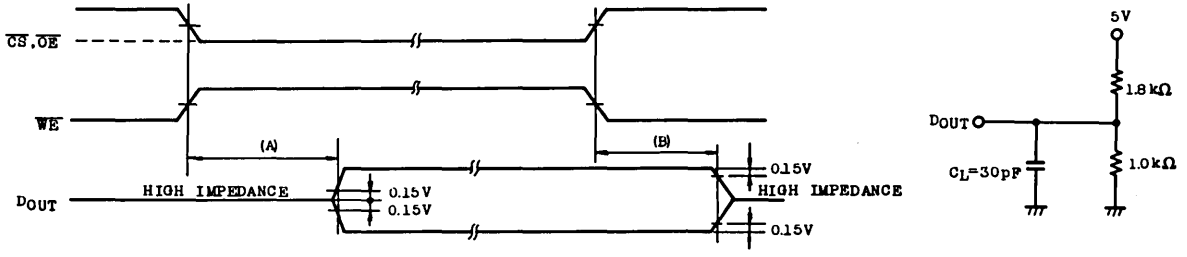
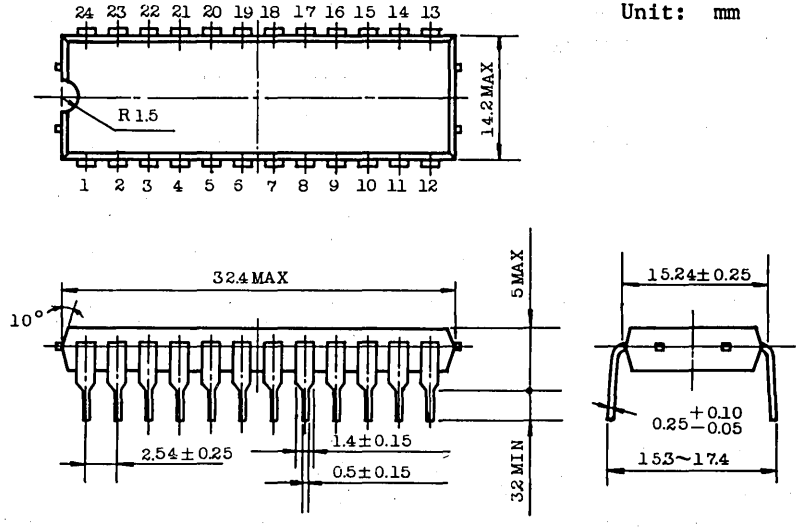


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS



Unit: mm

NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

TOSHIBA MOS MEMORY PRODUCT

2,048 WORD × 8 BIT CMOS STATIC RAM

TC5517CP-15/CPL-15/CP-20/CPL-20
TC5517CF-15/CFL-15/CF-20/CFL-20

DESCRIPTION

The TC5517CP/CF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply. The TC5517CP/CF has a output enable inputs, $\overline{OE}$ for fast memory access and output control and chip enable enable input $\overline{CE}$, which is used for device selection and can be used in order to achieve minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 150ns, 200ns and maximum operating current is 5mA/MHz are achieved. Thus the TC5517CP/CF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5517CPL/CFL guaranteed a standby current epual to or less than 1μA at 60°C ambient temperature available. And the TC5517CP/CPL is pin compatible with 2716 type EPROM. This means that the TC5517CP/CPL and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

FEATURES

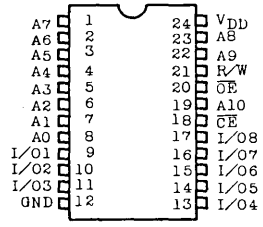
- Low Power Dissipation
  5mA/MHz (Max.) Operating
  0.2μA(MAX.) at Ta=25°C Standby
  1.0μA(MAX.) at Ta=60°C Standby
- 5V Single Power Supply
- Low Voltage Operation : V_{DD}=3V
  t_{CO}=1μs(MAX.) Ta=60°C
- Wide Temperature Operation
  Ta=−40~85°C
- Fully Static Operation
- Data Retention Voltage : 2.0V~5.5V
- Output Buffer Control : $\overline{OE}$

- Access Time

	TC5517CP-15/CPL-15 TC5517CF-15/CFL-15	TC5517CP-20/CPL-20 TC5517CF-20/CFL-20
Address Access Time (MAX.)	150ns	200ns
$\overline{CE}$ Access Time (MAX.)	150ns	200ns
$\overline{OE}$ Access Time (MAX.)	70ns	100ns

- Directly TTL Compatible : All Inputs and Outputs
- 24 Pin Standard Plastic Package : TC5517CP
- 24 Pin Flat Package : TC5517CF

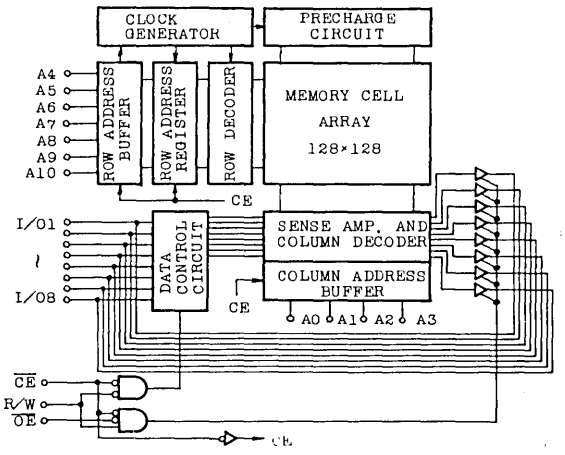
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{10}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	$A_0 \sim A_{10}$	$I/O_1 \sim I/O_8$	POWER
Read	L	L	H	Stable	Data Out	I_{DDO}
Write	L	*	L	Stable	Data In	I_{DDO}
Output Deselect	L	H	H	*	High Impedance	I_{DDO}
** Standby	H	*	*	*	High Impedance	I_{DDS}

Note : * : H or L ** : DataRetention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3~7.0V
V_{IN}	Input Voltage	−0.3V~V_{DD}+0.3V
$V_{I/O}$	Input/Output Voltage	−0.3V~V_{DD}+0.3V
P_D	Power Dissipation(Ta=85°C)	0.8W(0.45W)*
T_{STG}	Storage Temperature	−55°C~150°C
T_{OPR}	Operating Temperature	−40°C~85°C
T_{SOLDER}	Soldering Temperature·Time	260°C·10sec.

*Plastic FP=0.45W

RECOMMENDED D. C. OPERATING CONDITIONS (Ta=−40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DH}	Data Retention Voltage	2.0	—	5.5	V

D. C. CHARACTERISTICS (Ta=−40~85°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS			TC5517CP-15 CF-15 MIN.	TC5517CP-15 CF-15 MAX.	TC5517CP-20 CF-20 MIN.	TC5517CP-20 CF-20 MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			—	±1.0		±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE}=V_{IH}$, $OV \leqq V_{I/O} \leqq V_{DD}$			—	±5.0		±5.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			−1.0	—	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			2.0	—	2.0	—	mA
I_{DDS1}	Standby Current	$\overline{CE2}$=2.2V			—	3.0	—	3.0	mA
I_{DDS2}	Standby Current	$\overline{CE} \geqq V_{DD}-0.5V$	TC5517CPL/CFL	Ta=25°C	—	0.2	—	0.2	μA
				Ta=60°C	—	1.0	—	1.0	
			TC5517CP/CF	Ta=25°C	—	1.0	—	1.0	
				Ta=60°C	—	5.0	—	5.0	
				Ta=85°C	—	30	—	30	
I_{DDO1}	Operating Current	t_{cycle}=Min. cycle, $\overline{CE}$=OV, I_{OUT}=0mA		$V_{IN}=V_{IH}/V_{IL}$	—	45		30	mA
I_{DDO2}				$V_{IN}=V_{DD}/GND$	—	40		25	
I_{DDO3}		t_{cycle}=1μs, $\overline{CE}$=OV, I_{OUT}=0mA		$V_{IN}=V_{IH}/V_{IL}$	—	10	—	10	
I_{DDO4}				$V_{IN}=V_{DD}/GND$	—	5	—	5	

Note : Typical values are at Ta=25°C, V_{DD}=5V.

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	—	5	10	pF
$C_{I/O}$	Input/Output Capacitance	—	5	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC5517CP-15/CPL-15 TC5517CF-15/CFL-15		TC5517CP-20/CPL-20 TC5517CF-20/CFL-20		UNITS
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	—	200	—	ns
t_{ACC}	Address Time	—	150	—	200	
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	100	
t_{CO}	$\overline{CE}$ to Output Valid	—	150	—	200	
t_{COE}	$\overline{CE}$ or $\overline{OE}$ to Output Active	10	—	10	—	
t_{OD}	Output High-Z from Deselection	—	50	—	60	
t_{OH}	Output Hold from Address Change	15	—	20	—	

Write Cycle

SYMBOL	PARAMETER	TC5517CP-15/CPL-15 TC5517CF-15/CFL-15		TC5517CP-20/CPL-20 TC5517CF-20/CFL-20		UNITS
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	200	—	ns
t_{WP}	Write Pulse Width	120	—	150	—	
t_{AW}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{ODW}	Output High-Z from R/W	—	50	—	60	ns
t_{OEW}	Output Active from R/W	10	—	10	—	
t_{DS}	Data Set up Time	60	—	80	—	
t_{DH}	Data Hold Time	0	—	0	—	

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Input Pulse Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

Input Pulse Rise and Fall Times : 10ns

3V OPERATE SPECIFICATION

D. C. RECOMMENDED OPERATING CONDITIONS (Ta = −10~60°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V
V_{IH}	Input High Voltage	V_{DD}−0.2	—	V_{DD}	V
V_{IL}	Input Low Voltage	0	—	0.2	V

D.C. CHARACTERISTICS

(Ta = −10~60°C)

SYMBOL	PARAMETER CONDIOIONS	MIN.			TYP.	MAX.	UNIT	
I_{IL}	Input Leakage Current	$0V \leqq V_{IN} \leqq V_{DD}$			—	—	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			—	—	±5.0	μA
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.2V$			−100	—	—	μA
I_{OL}	Output Low Current	$V_{OL} = 0.2V$			100	—	—	μA
I_{DDS}	Standby Current	$\overline{CE} = V_{IH}$	TC5517CPL/CFL	Ta=25°C	—	—	0.2	μA
				Ta=60°C	—	—	1.0	
			TC5517CP/CF	Ta=25°C	—	—	1.0	
				Ta=60°C	—	—	5.0	
I_{DDO}	Operating Current	$\overline{CE} = 0V$, $I_{OUT} = 0mA$, t_r, $t_f \leqq 20nsec$	$t_{cycle} = 1\mu sec$		—	2.0	3.0	mA
			$t_{cycle} = 10\mu sec$		—	0.3	0.5	

- All voltage is measured from GND.

A. C. CHARACTERISTICS

(Ta = −10~60°C, V_{DD} = 3V ± 10%)

Read CYCLE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	1000	—	—	ns
t_{ACC}	Address Access Time	—	250	1000	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	80	200	ns
t_{CO}	$\overline{CE}$ to Output Valid	—	250	1000	ns
t_{COE}	$\overline{CE}$ or $\overline{OE}$ Output Active	10	—		ns
t_{OD}	Output High-Z Deselection	—	—	200	ns
t_{OH}	Output Hold from Address Change	20	—	—	ns

WRITE CYCLE

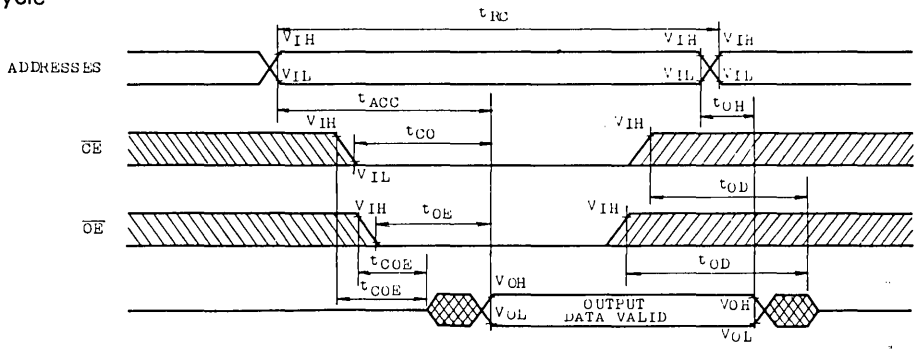
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{WC}	Write Cycle Time	1000	—	—	ns
t_{WP}	Write Pulse Width	500	—	—	ns
t_{AW}	Address Set up Time	100	—	—	ns
t_{WR}	Write Recovery Time	100	—	—	ns
t_{ODW}	Output High-Z from R/W	—	—	200	ns
t_{OEW}	Output Active from R/W	10	—	—	ns
t_{DS}	Data Set up Time	400	—	—	ns
t_{DH}	Data Hold Time	50	—	—	ns

A. C. TEST CONDITIONS

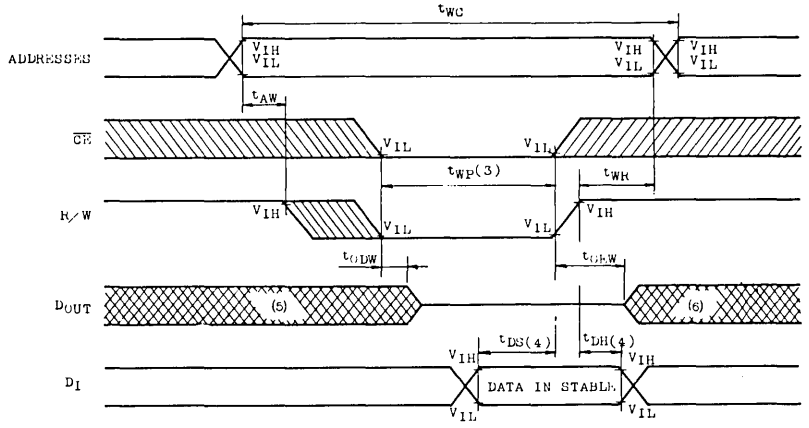
- Output Load : 100pF (Include Jig)
- Input Pulse Levels : 0.2V, V_{DD}−0.2V
- Timing Measurement Level Input : 1.5V , 1.5V
- Output : 1.5V , 1.5V
- Input Pulse Rise and Fall Times : ≦20ns

TIMING WAVEFORMS

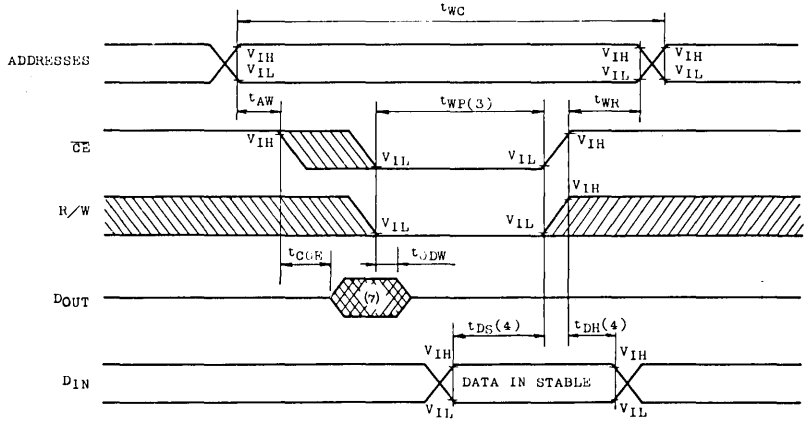
- Read Cycle



- Write Cycle 1 (2)



- Write Cycle 2 (2)



: UNKNOWN

Note:

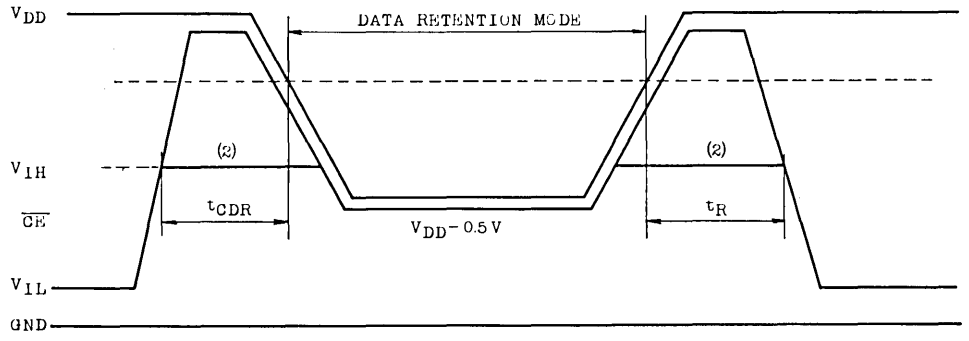
1. R/W is high for a Read Cycle.
2. $\overline{OE}$=V_{IH} or V_{IL}. If, $\overline{OE}$=V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specfied as the logical "AND" of $\overline{CE}$ and R/W.
   t_{WP} is measured from the latter of $\overline{CE}$ or R/W going low to the earlier of $\overline{CE}$ or R/W going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or R/W going high.
5. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
6. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS (Ta=−40~85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Power Supply Voltage			2.0	—	5.5	V
I_{DDS2}	Standby Current	TC5517CPL/CFL	Ta=25°C	—	0.005	0.2	μA
			Ta=60°C	—	—	1.0	
		TC5517CP/CF	Ta=25°C	—	0.05	1.0	
			Ta=60°C	—	—	5.0	
			Ta=85°C	—	—	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	—	—	ns
t_R	Recovery Time			t_{RC}(1)	—	—	

Note :

1. t_{RC} : Read Cycle Time

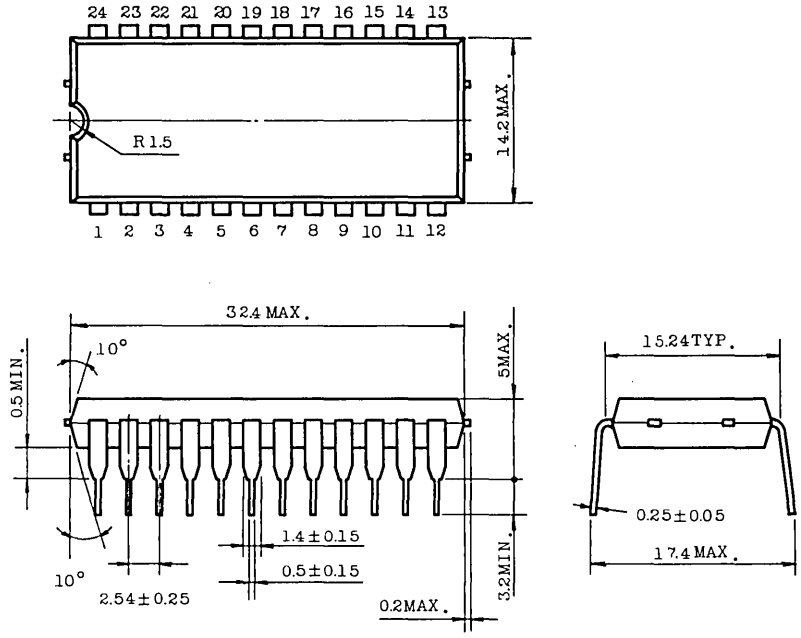


Note :

2. If the V_{IH} level of $\overline{CE}$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V I_{DDS1} current flows.

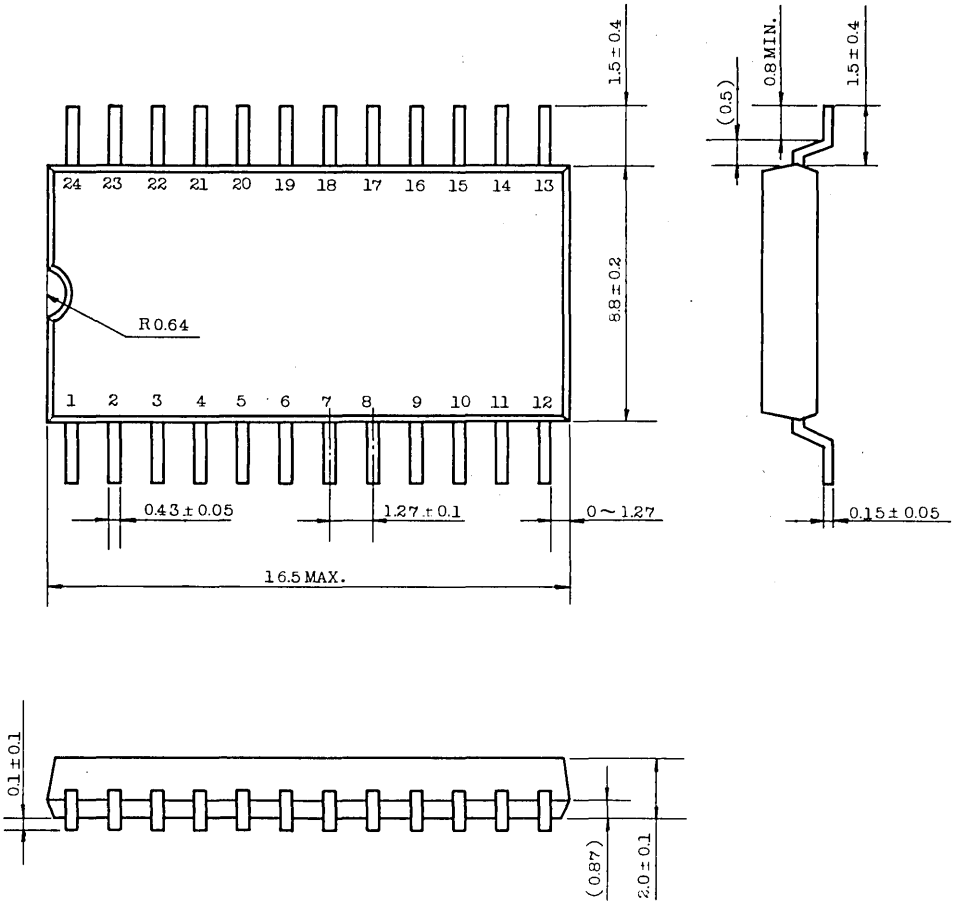
OUTLINE DRAWINGS

- Plastic DIP



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

- Plastic FP



Note : Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

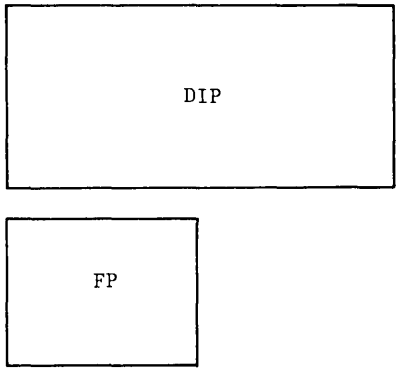
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

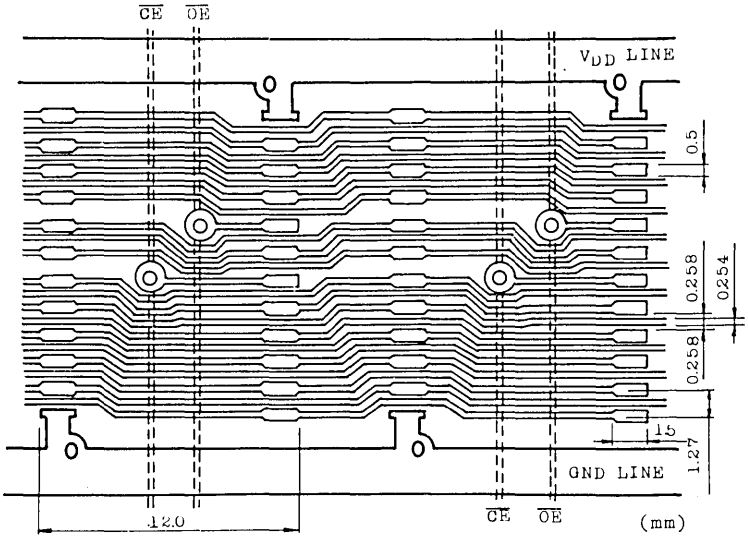
	Flat pacpage	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2. Comparison in occupied space.



3. Advantage of this package
   Small dimensions
   Capability of High Density Assembly
   Capability of thin Assembly——Capability of Assembly on both side of PC board.

4. PC pattern layout example.



TOSHIBA MOS MEMORY PRODUCT

2,048 WORD × 8 BIT CMOS STATIC RAM

TC5518CP-15/CPL-15/CP-20/CPL-20
TC5518CF-15/CFL-15/CF-20/CFL-20

DESCRIPTION

The TC5518CP/CF is a 16384-bit high speed and low power sully static random access memory organized as 2048 words by a 8 bits using CMOS technology, and operates from a single 5 volt supply. The $\overline{CE1}$ and $\overline{CE2}$, which are used for device selection and can be used in order to achieve minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 150ns, 200ns and maximum operating current is 5mA/MHz are achieved.

Thus the TC5518CP/CF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5518CPL/CFL guaranteed a standby current epual to or less than 1μA at 60°C ambient temperature available. And the TC5518CP/CPL is pin compatible with 2716 type EPROM. This means that the TC5518CP/CPL and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

FEATURES

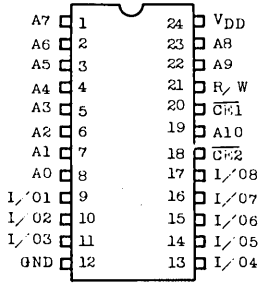
- Low Power Dissipation
  5mA/Max. Operating
  0.2μA(MAX.) at Ta=25°C Standby
  1.0μA(MAX.) at Ta=60°C Standby
- 5V Single PowerSupply
- Low Voltage Operation : V_{DD}=3V
  $t_{CO1, 2}$=1μs(MAX.) Ta=60°C
- Wide Temperature Operation
  Ta=−40~85°C
- Fully Static Operation
- Data Retention Voltage : 2.0V~5.5V
- Two Chip Enables ($\overline{CE1}$, $\overline{CE2}$)
  Simple Memory Expansion and Battery Back Up

- Access Time

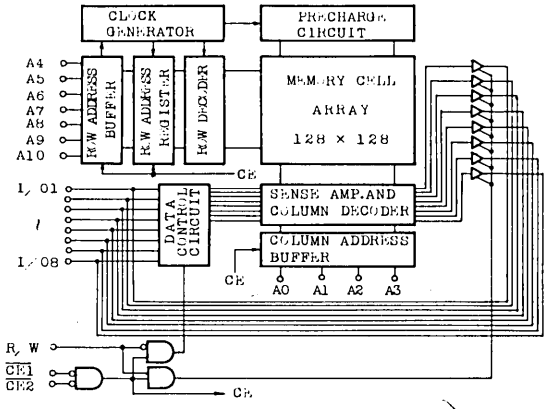
	TC5518CP-15/CPL-15 TC5518CF-15/CFL-15	TC5518CP-20/CPL-20 TC5518CF-20/CFL-20
Address Access Time (MAX.)	150ns	200ns
$\overline{CE1}$ Access Time (MAX.)	150ns	200ns
$\overline{CE2}$ Access Time (MAX.)	150ns	200ns

- Directly TTL Compatible : All Inputs and Outputs
- 24 Pin Standard Plastic Package : TC5518CP
- 24 Pin Flat Package : TC5518CF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{10}	Address Inputs
R/W	Read/Write Control Input
$\overline{CE_1}$, $\overline{CE_2}$	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

OPERATION MODE

MODE	$\overline{CE_2}$	$\overline{CE_1}$	R/W	A_0~A_{10}	I/O_1~I/O_8	POWER
Read	L	L	H	Stable	Data Out	I_{DDO}
Write	L	L	L	Stable	Data In	I_{DDO}
** Standby 1	*	H	*	*	High Impedance	I_{DDS}
** Standby 2	H	*	*	*	High Impedance	I_{DDS}

Note : * : H or L ** : Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3~7.0V
V_{IN}	Input Voltage	−0.3V~V_{DD}+0.3V
$V_{I/O}$	Input/Output Voltage	−0.3V~V_{DD}+0.3V
P_D	Power Dissipation(Ta=85°C)	0.8W(0.45W)*
T_{STG}	Storage Temperature	−55°C~150°C
T_{OPR}	Operating Temperature	−40°C~85°C
T_{SOLDER}	Soldering Temperature·Time	260°C·10sec.

*Plastic FP=0.45W

RECOMMENDED D. C. OPERATING CONDITIONS (Ta=−40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DH}	Data Retention Voltage	2.0	—	5.5	V

D. C. CHARACTERISTICS (Ta=−40~85°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS			TC5518CP-15 CF-15 MIN.	TC5518CP-15 CF-15 MAX.	TC5518CP-20 CF-20 MIN.	TC5518CP-20 CF-20 MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			—	±1.0	—	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE_2}=V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			—	±5.0		±5.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			−1.0	—	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			2.0	—	2.0	—	mA
I_{DDS1}	Standby Current	$\overline{CE_2}$=2.2V or $\overline{CE_1}$=2.2V			—	3.0	—	3.0	mA
I_{DDS2}	Standby Current	$\overline{CE_2}$=V_{DD}−0.5V or $\overline{CE_1}$=V_{DD}−0.5V V_{DD}=2~5.5V	TC5518CPL/CFL	Ta=25°C	—	0.2	—	0.2	μA
				Ta=60°C	—	1.0	—	1.0	
			TC5518CP/CF	Ta=25°C	—	1.0	—	1.0	
				Ta=60°C	—	5.0	—	5.0	
				Ta=85°C	—	30	—	30	
I_{DDO1}	Operating Current	t_{cycle}=Min. cycle, $\overline{CE_1}$=$\overline{CE_2}$=0V, I_{OUT}=0mA		V_{IN}=V_{IH}/V_{IL}	—	45		30	mA
I_{DDO2}				V_{IN}=V_{DD}/GND	—	40		25	
I_{DDO3}		t_{cycle}=1μs, $\overline{CE_1}$=		V_{IN}=V_{IH}/V_{IL}	—	10	—	10	
I_{DDO4}		$\overline{CE_2}$=0V, I_{OUT}=0mA		V_{IN}=V_{DD}/GND	—	5	—	5	

Note : Typical values are at Ta=25°C, V_{DD}=5V.

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	—	5	10	pF
C_{OUT}	Input/Output Capacitance	—	5	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS ($Ta = -40 \sim 85°C$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC5518CP-15/CPL-15 TC5518CF-15/CFL-15		TC5518CP-20/CPL-20 TC5518CF-20/CFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	—	200	—	ns
t_{ACC}	Address Access Time	—	150	—	200	
t_{CO1}	$\overline{CE_1}$ to Output Valid	—	150	—	200	
t_{CO2}	$\overline{CE_2}$ to Output Valid	—	150	—	200	
t_{COE}	$\overline{CE_1}$ or $\overline{CE_2}$ to Output Active	10	—	10	—	
t_{OD}	Output High-Z Deselection	—	50	—	60	
t_{OH}	Output Hold from Address Change	15	—	20	—	

SYMBOL	PARAMETER	TC5518CP-15/CPL-15 TC5518CF-15/CFL-15		TC5518CP-20/CPL-20 TC5518CF-20/CFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	150	—	200	—	ns
t_{WP}	Write Pulse Width	120	—	150	—	
t_{AW}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	Output High-Z from R/W	—	50	—	60	
t_{OEW}	Output Active from R/W	10	—	10	—	
t_{DS}	Data Set up Time	60	—	80	—	
t_{DH}	Data Hold Time	0	—	0	—	

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate
Input Pulse Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10ns

3V OPERATE SPECIFICATION

D. C. RECOMMENDED OPERATING CONDITIONS ($Ta = -10 \sim 60°C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V
V_{IH}	Input High Voltage	$V_{DD}-0.2$	—	V_{DD}	V
V_{IL}	Input Low Voltage	0	—	0.2	V

D.C. CHARACTERISTICS (Ta=−10~60°C)

SYMBOL	PARAMETER CONDIOIONS	MIN.			TYP.	MAX.	UNIT	
I_{IL}	Input Leakage Current	$0V \leqq V_{IH} \leqq V_{DD}$			—	—	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE1}$, $2=V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			—	—	±5.0	μA
I_{OH}	Output High Current	$V_{OH}=V_{DD}-0.2V$			−100	—	—	μA
I_{OL}	Output Low Current	$V_{OL}=0.2V$			100	—	—	μA
I_{DDS}	Standby Current	$\overline{CE1}=\overline{CE2}=V_{IH}$	TC5518CPL/CFL	Ta=25°C	—	—	0.2	μA
				Ta=60°C	—	—	1.0	
			TC5518CP/CF	Ta=25°C	—	—	1.0	
				Ta=60°C	—	—	5.0	
I_{DDO}	Operating Current	$\overline{CE1}$, $2=0V$, $I_{OUT}=0mA$, t_r, $t_f \leqq 20nsec$	$t_{cycle}=1\mu sec$		—	2.0	3.0	mA
			$t_{cycle}=10\mu sec$		—	0.3	0.5	

● All voltage is measured from GND.

A. C. CHARACTERISTICS (Ta=−10~60°C, V_{DD}=3V±10%)

Read CYCLE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	1000	—	—	ns
t_{ACC}	Address Access Time	—	250	1000	ns
t_{CO1}	$\overline{CE1}$ to Output Valid	—	250	1000	ns
t_{CO2}	$\overline{CE2}$ to Output Valid	—	250	1000	ns
t_{COE}	$\overline{CE1}$ or $\overline{CE2}$ Output Active	10	—	—	ns
t_{OD}	Output High-Z Deselection	—	—	200	ns
t_{OH}	Output Hold from Address Change	20	—	—	ns

WRITE CYCLE

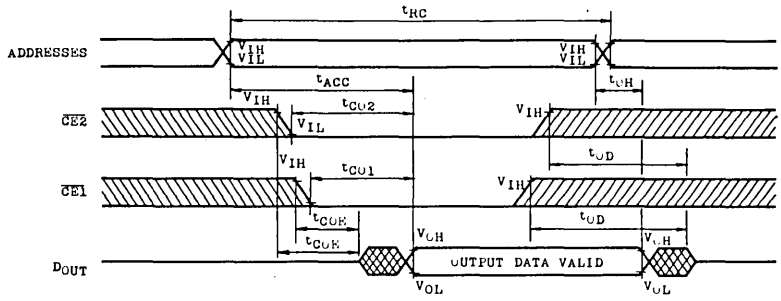
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{WC}	Write Cycle Time	1000	—	—	ns
t_{WP}	Write Pulse Width	500	—	—	ns
t_{AW}	Address Set up Time	100	—	—	ns
t_{WR}	Write Recovery Time	100	—	—	ns
t_{ODW}	Output High-Z from R/W	—	—	200	ns
t_{OEW}	Output Active from R/W	10	—	—	ns
t_{DS}	Data Set up Time	400	—	—	ns
t_{DH}	Data Hold Time	50	—	—	ns

A. C. TEST CONDITIONS

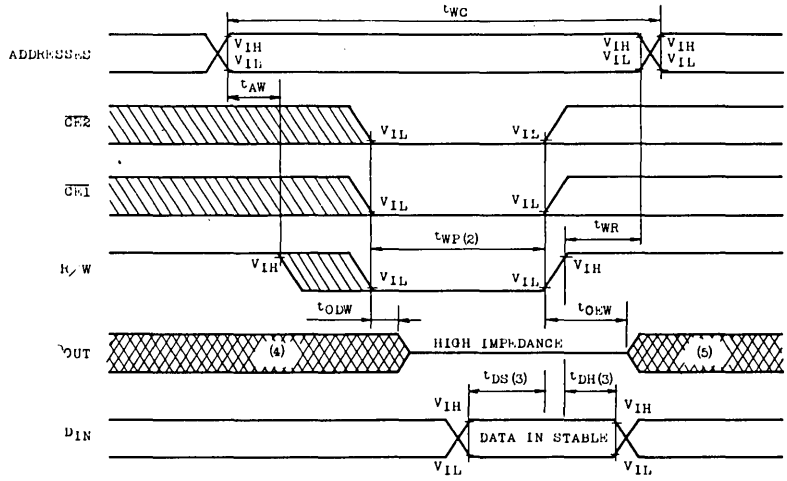
Output Load : 100pF (Include Jig)
Input Pulse Levels : 0.2V, V_{DD}−0.2V
Timing Measurement Level Input : 1.5V , 1.5V
Output : 1.5V , 1.5V
Input Pulse Rise and Fall Times : ≦20ns

TIMING WAVEFORMS

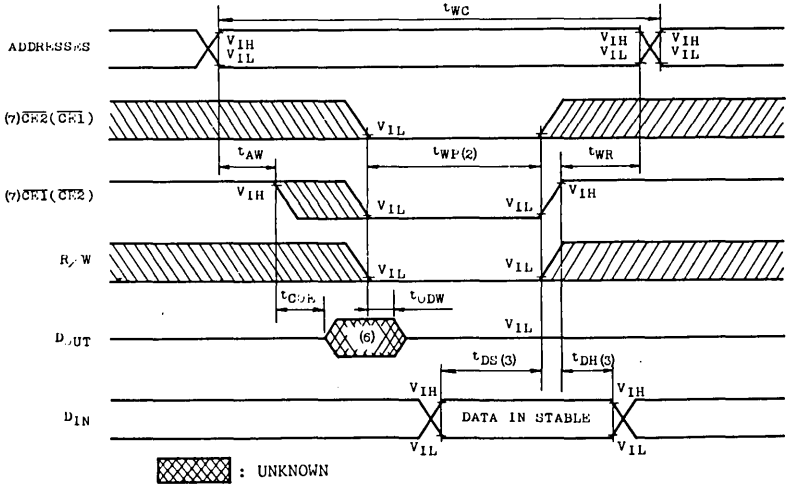
- Read Cycle



- Write Cycle 1 (2)



- Write Cycle 2 (2)



Note :

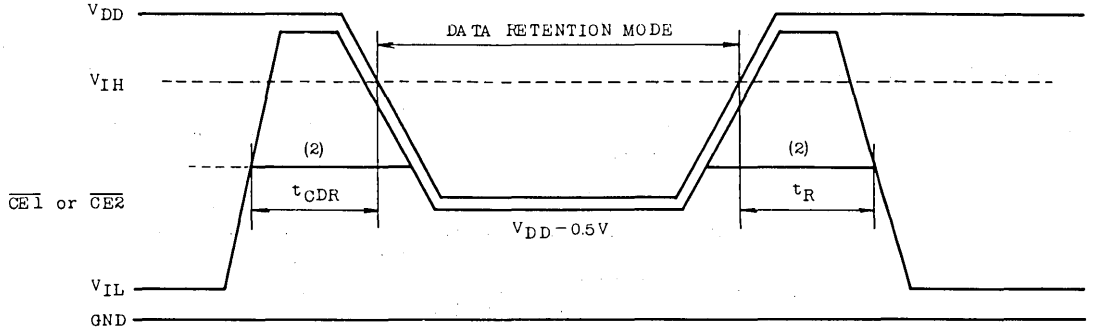
1. R/W is high for a read Cycle.
2. t_{WP} is specified as logical "AND" of $\overline{CE_1}$, $\overline{CE_2}$ and R/W.
   t_{WP} is measured from the latter of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going low to the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going high.
3. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going high.
4. If the $\overline{CE_1}$ or $\overline{CE_2}$ low transition occurs simultaneously or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
5. If the $\overline{CE_1}$ or $\overline{CE_2}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
6. If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE_1}$ or $\overline{CE_2}$ low transition, the output buffers remain in a high impedance state in this peried.
7. A write occurs during the overlap of a low $\overline{CE_1}$, low $\overline{CE_2}$ and low R/W.
   In write cycle 2, write is controlled by either $\overline{CE_1}$ or $\overline{CE_2}$.

DATA RETENTION CHARACTERISTICS (Ta = −40~85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Power Supply Voltage			2.0	—	5.5	V
I_{DDS2}	Standby Current	TC5518CPL/CFL	Ta=25°C	—	0.005	0.2	μA
			Ta=60°C	—	—	1.0	
		TC5518CP/CF	Ta=25°C	—	0.05	1.0	
			Ta=60°C	—	—	5.0	
			Ta=85°C	—	—	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	—	—	μs
t_R	Recovery Time			t_{RC}(1)	—	—	ns

Note :

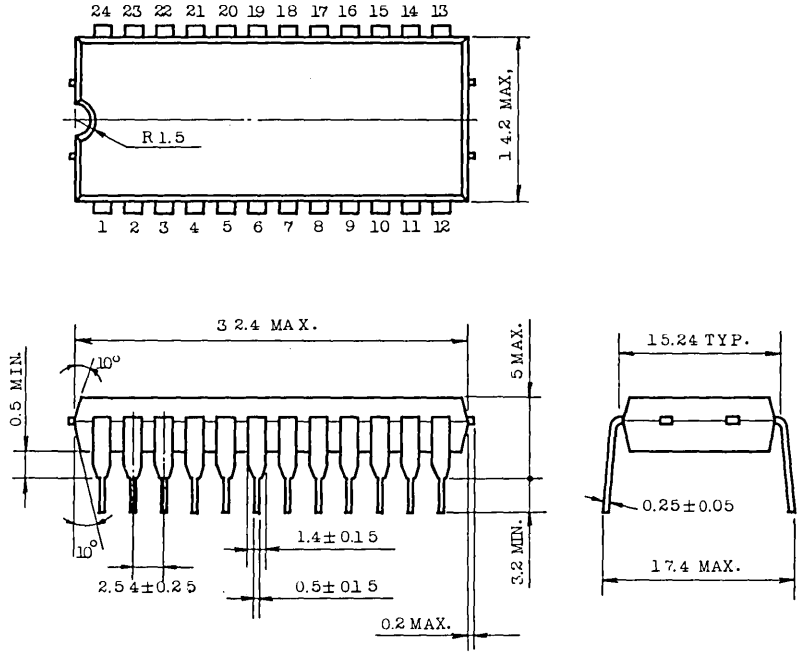
1. t_{RC} : Read Cycle Time



2. If the V_{IH} level of $\overline{CE_2}$ ($\overline{CE_1}$) is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

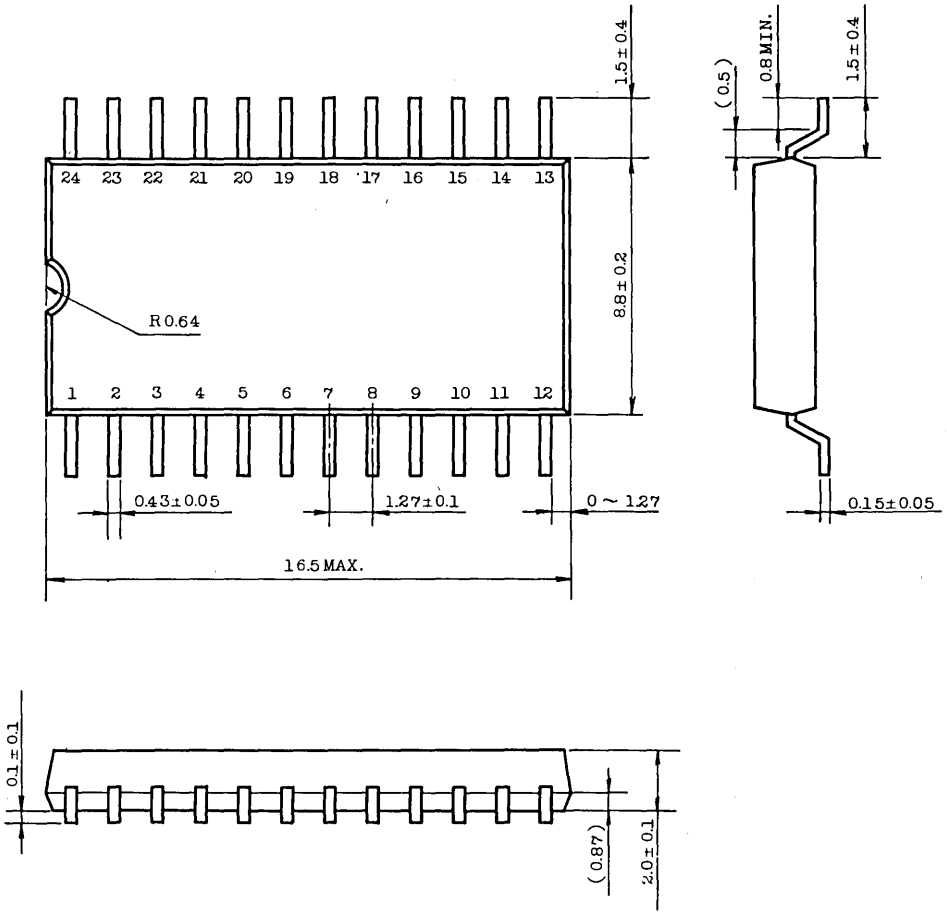
OUTLINE DRAWINGS

- Plastic DIP



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

- Plastic FP



Note : Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

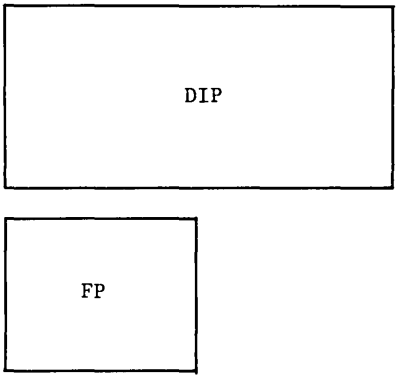
This new flat package is a very small and this compared with conventional standard dual-in-line package. Differences as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

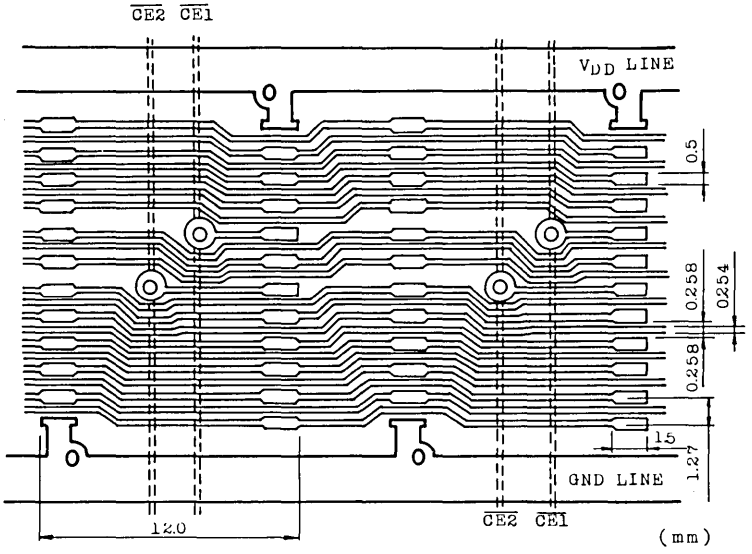
	Flat pacpage	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2, Comparison in occupied space



3. Advantage of this package
   Small dimensions
   Capability of High Density Assembly
   Capability of thin Assembly ——
   Capability of Assembly on both side of PC board

4. PC pattern layout example



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2063P-10, TMM2063P-12 TMM2063P-15

DESCRIPTION

The TMM2063P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When $\overline{CS_1}$ is a logical high or CS_2 is a logical low, the device is placed in a low power standby mode in which maximum standby current is 10mA. Thus the TMM2063P is most suitable for use in microcomputer peripheral memory where the low power applications are required, moreover, suitable for use in high density assembly as 0.3 inch width package is use for. The TMM2063P is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

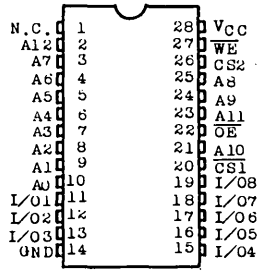
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2063P-10	100ns	80mA	10mA
TMM2063P-12	120ns	80mA	10mA
TMM2063P-15	150ns	80mA	10mA

- High Density Assembly Capability : 0.3 inch width package (28 pin plastic DIP)
- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature : $\overline{CS_1}$, CS_2
- Output Buffer Control : $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Inputs Protected : All inputs have protection against static charge

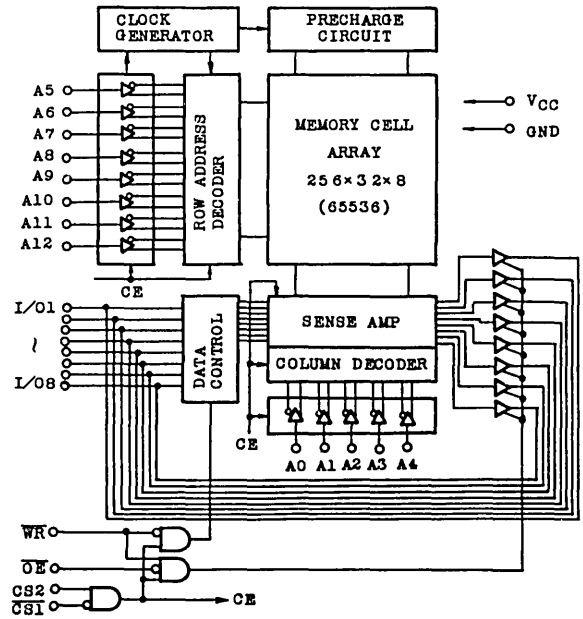
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
A_0~A_4	Column Address Inputs
A_5~A_{12}	Row Address Inputs
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
I/O_1~I/O_8	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	0.8	W

* −3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=2.1mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS_1}$=V_{CC}, CS_2=0V I_{OUT}=0mA	—	—	20	mA
I_{SB}	Standby Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}, I_{OUT}=0mA	—	—	10	mA
I_{CC}	Operating Current	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, I_{OUT}=0mA	—	—	80	mA

CAPACITANCE*** (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

*** Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2063P-10		TMM2063P-12		TMM2063P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CS_1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CS_2 Access Time	—	100	—	120	—	150	
t_{OE}	$\overline{OE}$ Access Time	—	40	—	50	—	60	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS_1}$ or CS_2 to Output in Low-Z	10	—	10	—	10	—	
t_{CHZ}	$\overline{CS_1}$ or CS_2 to Output in High-Z	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	50	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	60	—	60	

Write Cycle

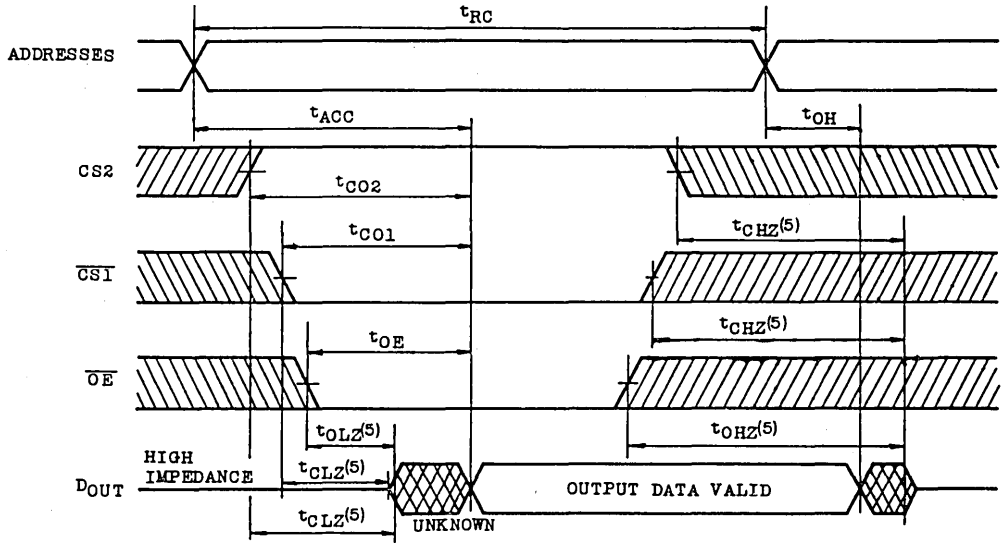
SYMBOL	PARAMETER	TMM2063P-10		TMM2063P-12		TMM2063P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	80	—	100	—	120	—	
t_{AS}	Address Set Up Time	10	—	10	—	10	—	
t_{WP}	Write Pulse Width	70	—	85	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	30	—	35	—	40	

A. C. TEST CONDITIONS

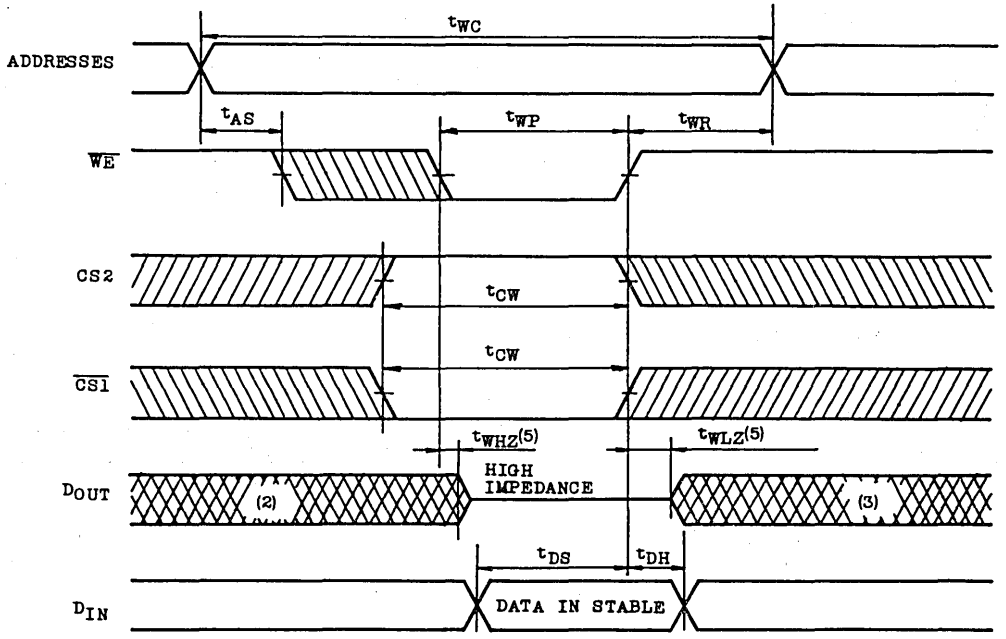
Input Pulse Levels	V_{IH}=2.2V, V_{IL}=0.6V
Input Rise and Fall Time	10ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & C_L=100pF

TIMING WAVEFORMS

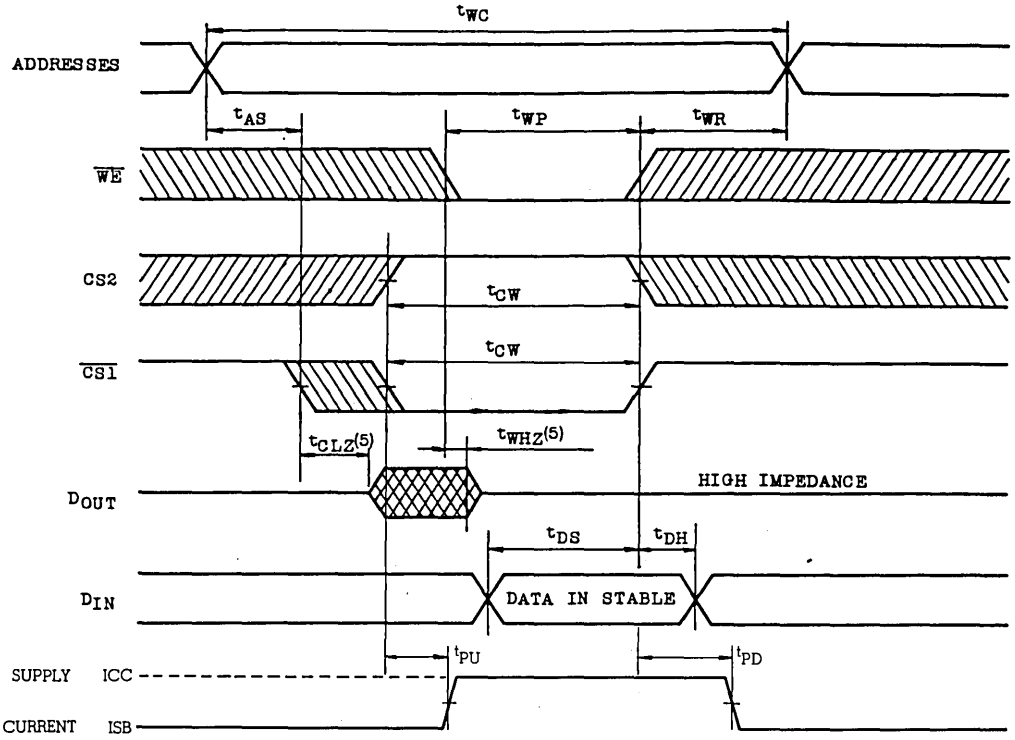
- READ CYCLE (1)



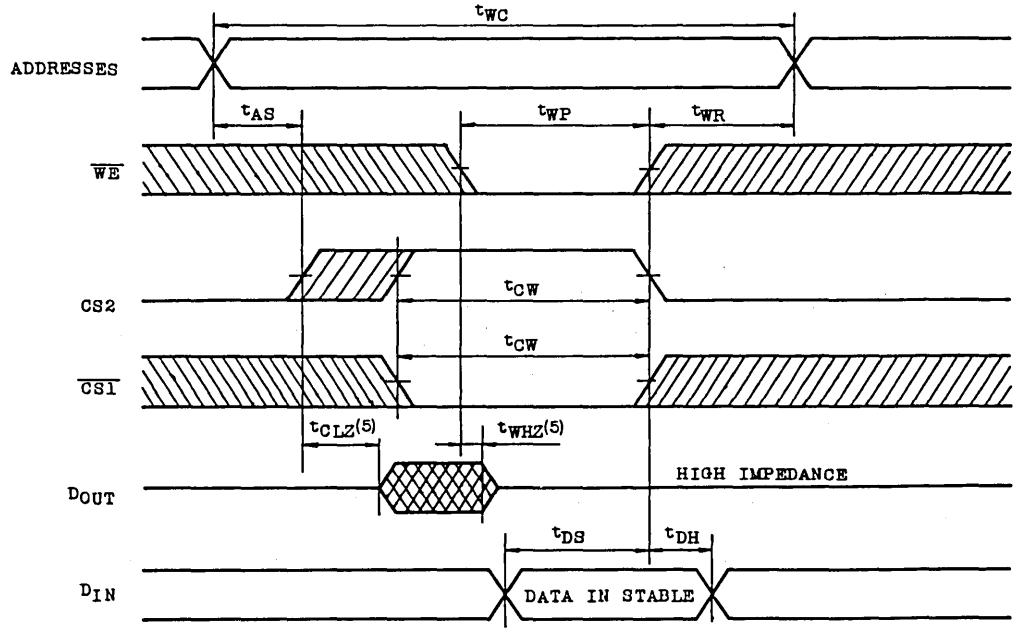
- WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



- WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS_1}$ Low transition or CS_2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS_1}$ High transition or CS_2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{CLZ}, t_{OLZ}, t_{WLZ}·····Output Enable Time
   (B) t_{CHZ}, t_{OHZ}, t_{WHZ}·····Output Disable Time

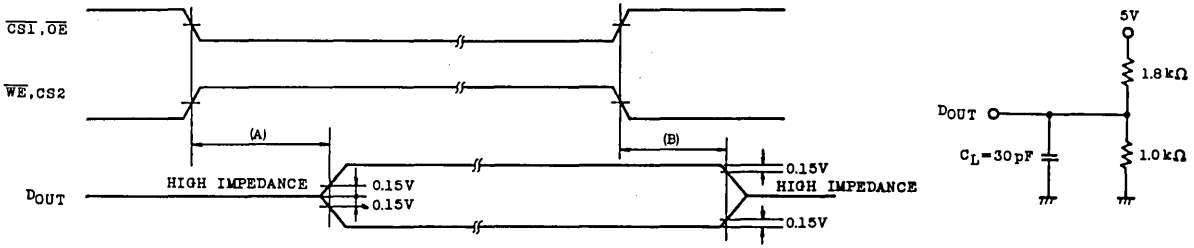
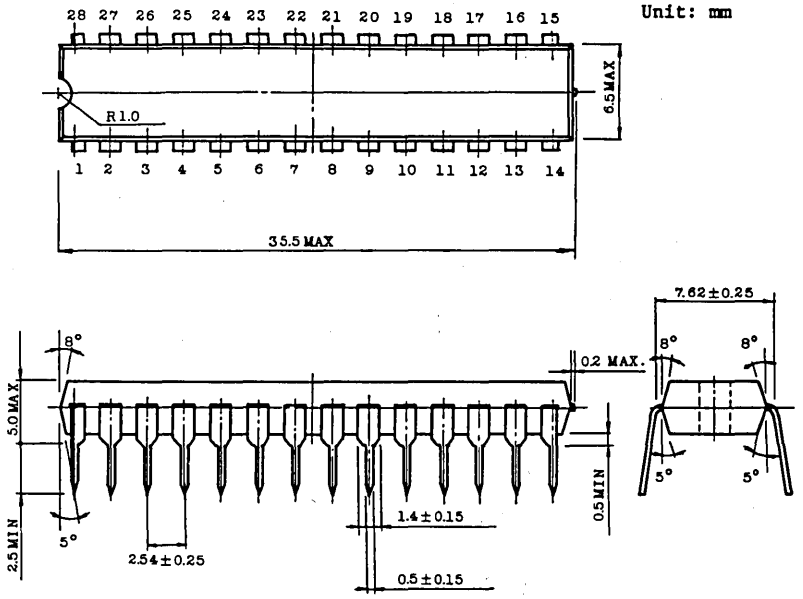


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2064P-10, TMM2064P-12 TMM2064P-15

DESCRIPTION

The TMM2064P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When $\overline{CS_1}$ is a logical high or CS_2 is a logical low, the deivce is placed in a low power standby mode in which maximum standby current is 10mA. Thus the TMM2064P is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2064P is fabricated with ion implanted N channel silicon gate MOS technology for high perfomance and high reliability.

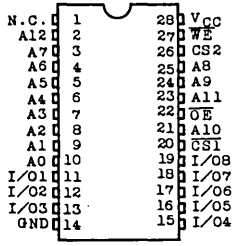
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2064P-10	100ns	80mA	10mA
TMM2064P-12	120ns	80mA	10mA
TMM2064P-15	150ns	80mA	10mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature : $\overline{CS_1}$ CS_2
- Output Buffer Control : $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Inputs Protected : All inputs have protection against static charge.

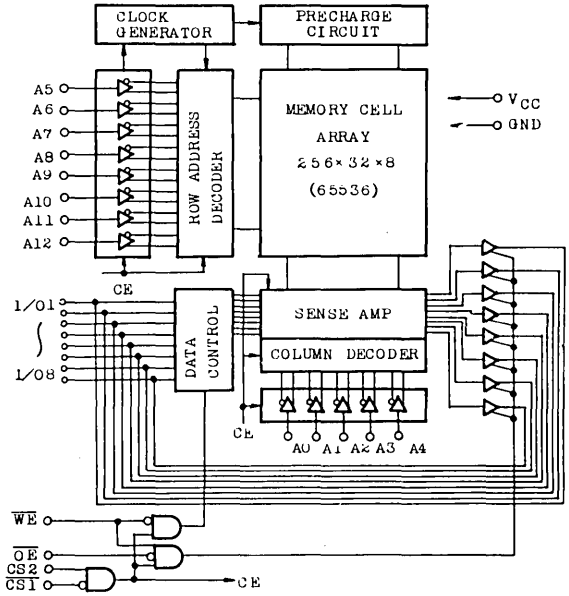
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
A_0~A_4	Column Address Inputs
A_5~A_{12}	Row Address Inputs
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
I/O_1~I/O_8	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

* −3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=2.1mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS_1}$=V_{CC}, CS_2=0V I_{OUT}=0mA	—	—	20	mA
I_{SB}	Standby Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}, I_{OUT}=0mA	—	—	10	mA
I_{CC}	Operating Current	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, I_{OUT}=0mA	—	—	80	mA

CAPACITANCE*** (Ta=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

*** Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

(T_a=0~70°C, V_{CC}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2064P-10		TMM2064P-12		TMM2064P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CS_1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CS_2 Access Time	—	100	—	120	—	150	
t_{OE}	$\overline{OE}$ Access Time	—	40	—	50	—	60	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS_1}$ or CS_2 to Output in Low-Z	10	—	10	—	10	—	
t_{CHZ}	$\overline{CS_1}$ or CS_2 to Output in High-Z	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	50	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	60	—	60	

Write Cycle

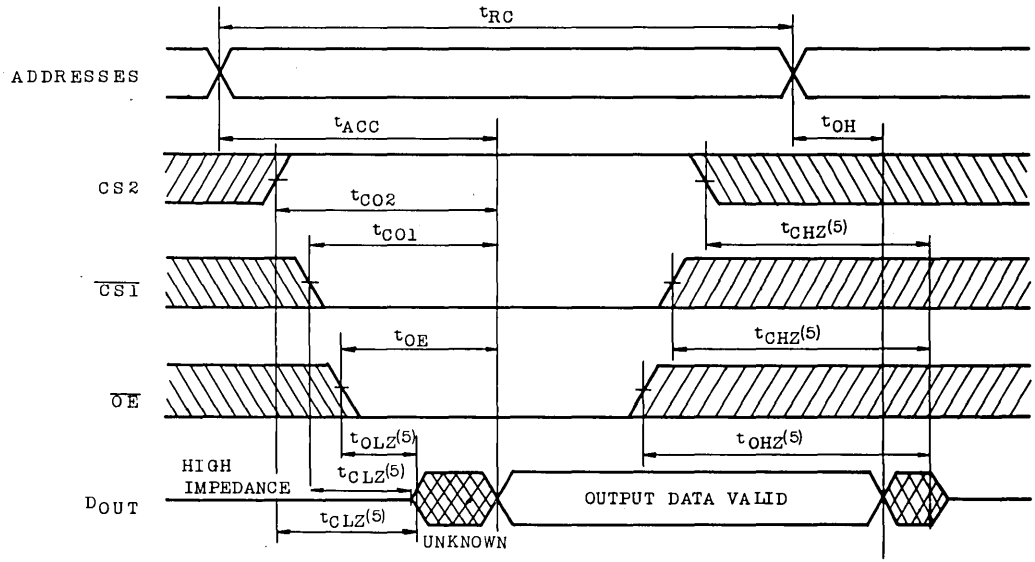
SYMBOL	PARAMETER	TMM2064P-10		TMM2064P-12		TMM2064P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	80	—	100	—	120	—	
t_{AS}	Address Set Up Time	10	—	10	—	10	—	
t_{WP}	Write Pulse Width	70	—	85	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	30	—	35	—	40	

A. C. TEST CONDITIONS

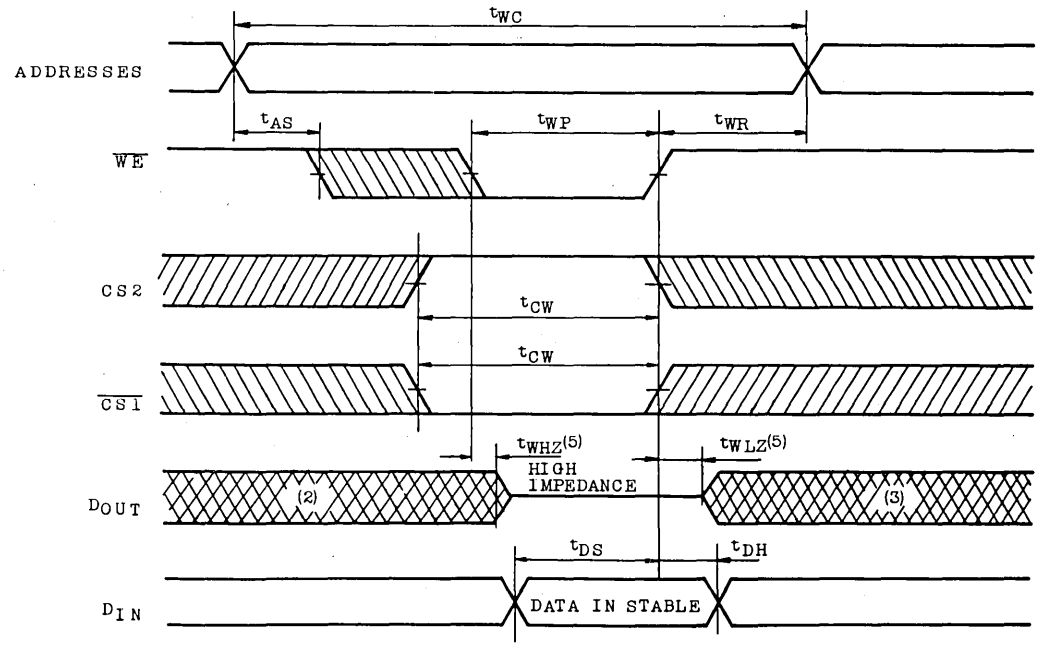
Input Pulse Levels	V_{IH}=2.2V, V_{IL}=0.6V
Input Rise and Fall Time	10ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & C_L=100pF

TIMING WAVEFORMS

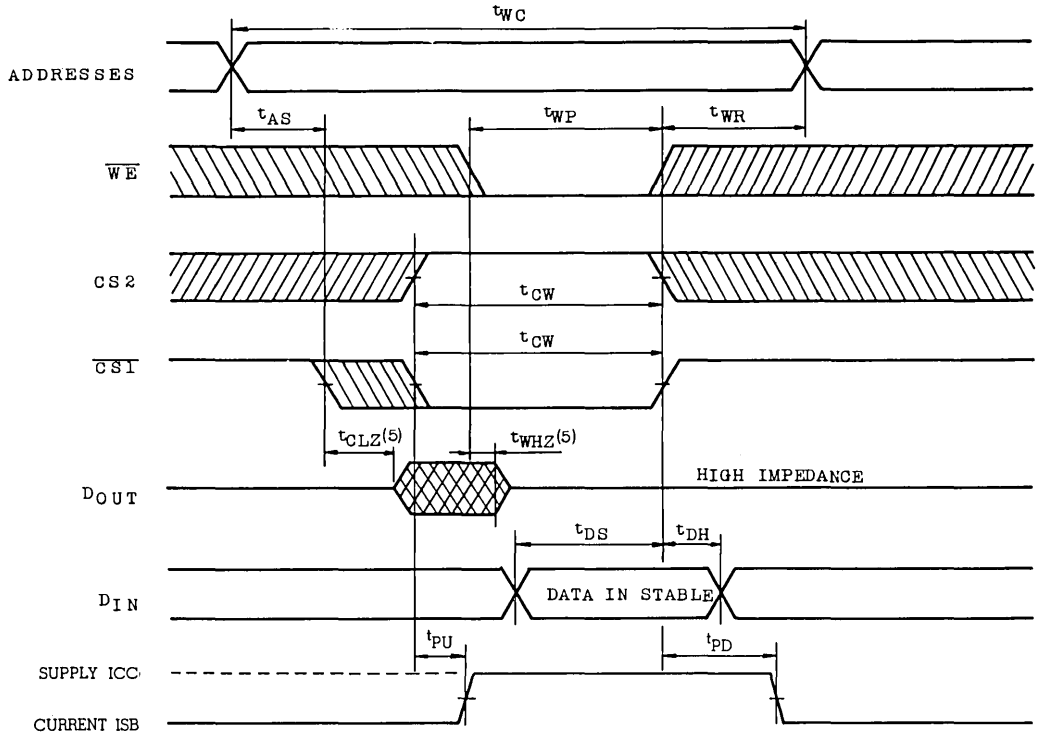
- READ CYCLE (1)



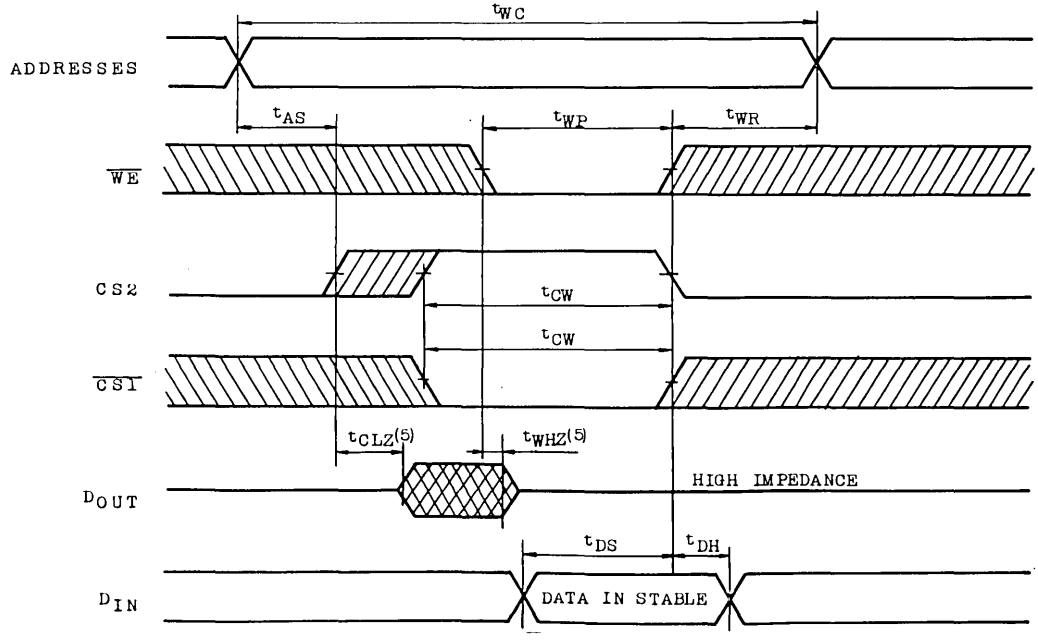
- WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



- WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS_1}$ Low transition or CS_2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS_1}$ High transition or CS_2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{CLZ}, t_{OLZ}, t_{WLZ}·····Output Enable Time
   (B) t_{CHZ}, t_{OHZ}, t_{WHZ}·····Output Disable Time

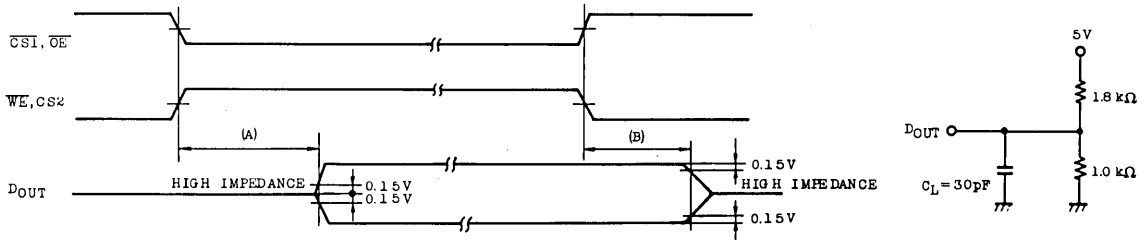
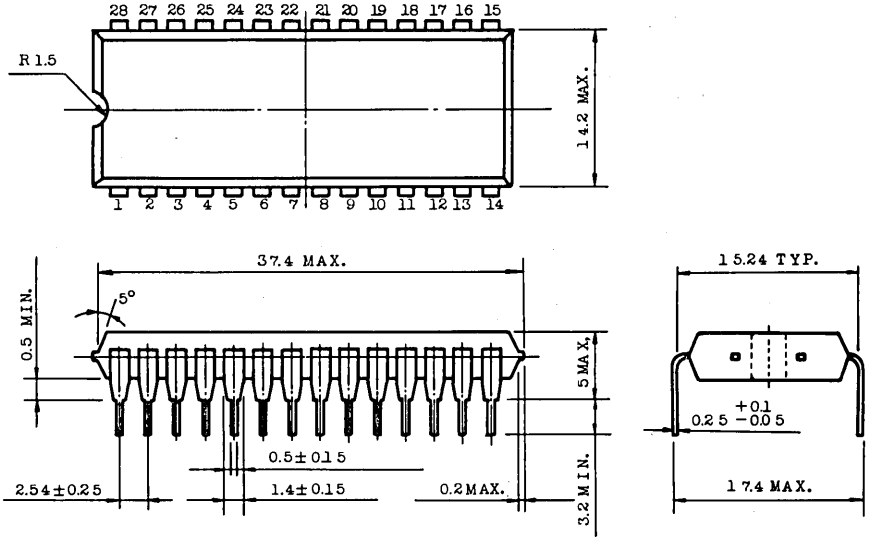


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5563APL-10, TC5563APL-12
TC5563APL-15

PRELIMINARY

DESCRIPTION

The TC5563APL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE_2 is a logical low or $\overline{CE_1}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5563APL has three control inputs. Two chip enables ($\overline{CE_1}$, CE_2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5563APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5563APL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5563APL is offered in a dual-in-line 28 pin 0.3 inch width plastic package.

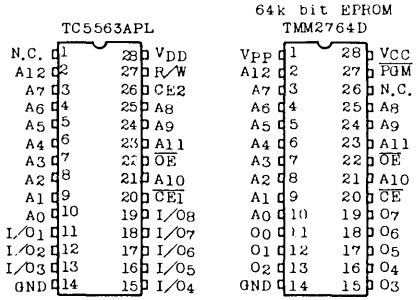
FEATURES

- Low Power Dissipation
  27.5mW/MHz (MAx.) Operating
- Standby Current : 100μA (Max.) Ta=70°C
- Access Time
  TC5563APL-10 : 100ns (Max.)
  TC5563APL-12 : 120ns (Max.)
  TC5563APL-15 : 150ns (Max.)
- 5V Single Power Supply
- Power Down Features : CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package(SOP)	*TC5565AFL

*) See TC5565APL Technical Date.

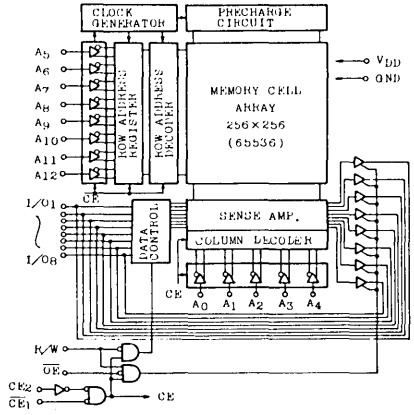
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



TC5563APL-10, TC5563APL-12
TC5563APL-15

OPERATION MODE

OPERATION MODE	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	0.8	W
T_{SOLDER}	Soldering Temperature	260·10	°C·Sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

* : −3.0V at Pulse width 50ns

D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3*	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

* : −3.0V at Pulse width 50ns

D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}		—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V		−1.0	—	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		4.0	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL} or R/W=V_{IL} or $\overline{OE}$=V_{IH} V_{OUT}=0~V_{DD}		—	—	±1.0	μA
I_{DDO1}	Operating Current	V_{DD}=5.5V Iout=0mA $\overline{CE_1}$=V_{IL} CE_2=V_{IH} Other Input =V_{IH}/V_{IL}	t_{CYCLE}=1μs	—	—	10	mA
			t_{CYCLE}= Min. cycle	—	—	45	mA
I_{DDO2}	Operating Current	V_{DD}=5.5V $\overline{CE_1}$=0.2V CE_2=V_{DD}−0.2V Other Input Iout=0mA =V_{DD}−0.2V/0.2V	t_{CYCLE}=1μs	—	—	5	mA
			t_{CYCLE}= Min. cycle	—	—	40	mA
I_{DDS1}	Standby Current	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL}		—	—	3	mA
*I_{DDS2}	Standby Current	$\overline{CE_1}$=V_{DD}−0.2V or CE_2=0.2V V_{DD}=2.0~5.5V		—	2	100	μA

* : In standby mode with $\overline{CE_1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE_2 \geqq V_{DD}-0.2V$ or $CE_2 \leqq 0.2V$.

CAPACITANCE (Ta = 25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	ns
t_{CO1}	$\overline{CE1}$ Access Time	—	100	—	120	—	150	ns
t_{CO2}	CE2 Access Time	—	100	—	120	—	150	ns
t_{OE}	Output Enable to Output Valid	—	50	—	60	—	70	ns
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	—	10	—	15	—	ns
t_{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	ns
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	—	35	—	40	—	50	ns
t_{ODO}	Output Enable to Output in High-Z	—	35	—	40	—	50	ns
t_{OH}	Output Data Hold Time	20	—	20	—	20	—	ns

Write Cycle

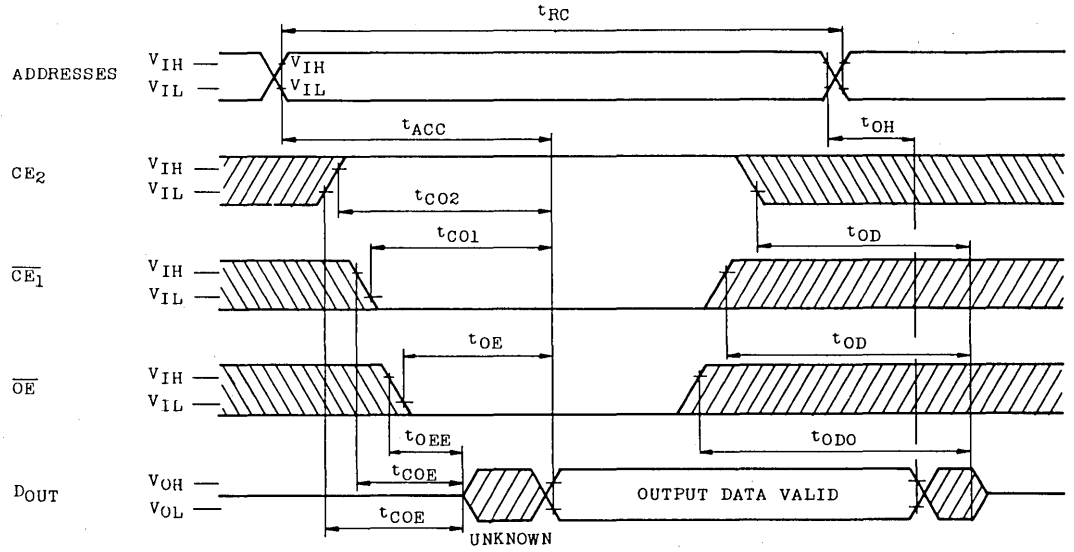
SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{WP}	Write Pulse Width	60	—	70	—	90	—	ns
t_{CW}	Chip Selection to End of Write	80	—	85	—	100	—	ns
t_{AS}	Address Set up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{ODW}	R/W to Output in High-Z	—	35	—	40	—	50	ns
t_{OEW}	R/W to Output in Low-Z	5	—	5	—	10	—	ns
t_{DS}	Data Set Up Time	40	—	50	—	60	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns

A. C. TEST CONDITIONS

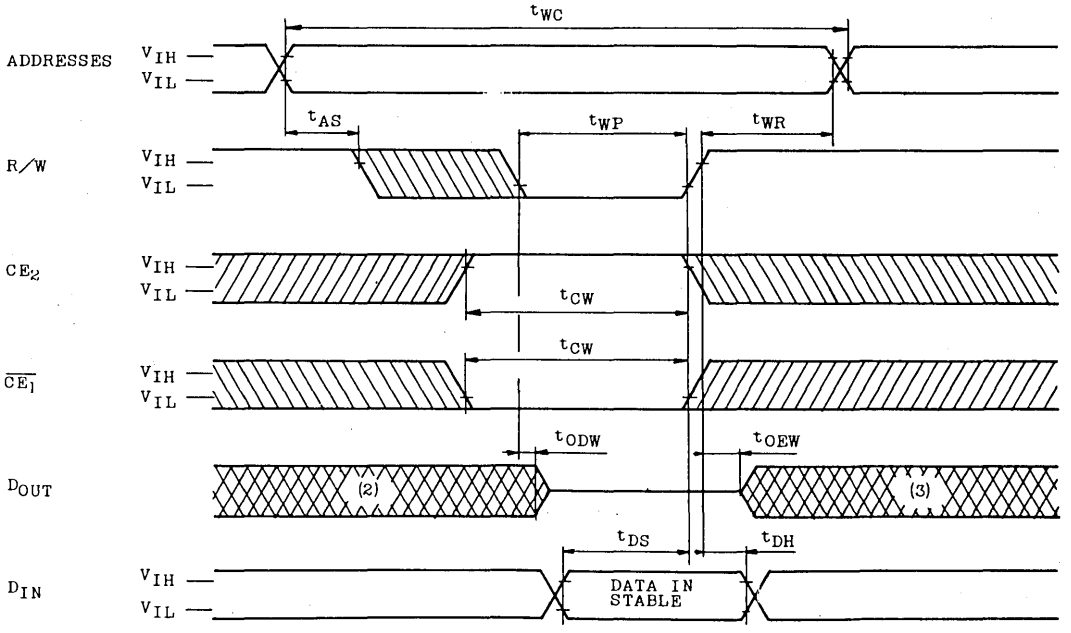
Output Load		: 100pF + 1 TTL Gate
Input Pulse Level		: 0.6V, 2.4V
Timing Measurement	V_{IN}	: 0.8V, 2.2V
Reference Level	V_{OUT}	: 0.8V, 2.2V
		: 5ns

TIMING WAVEFORMS

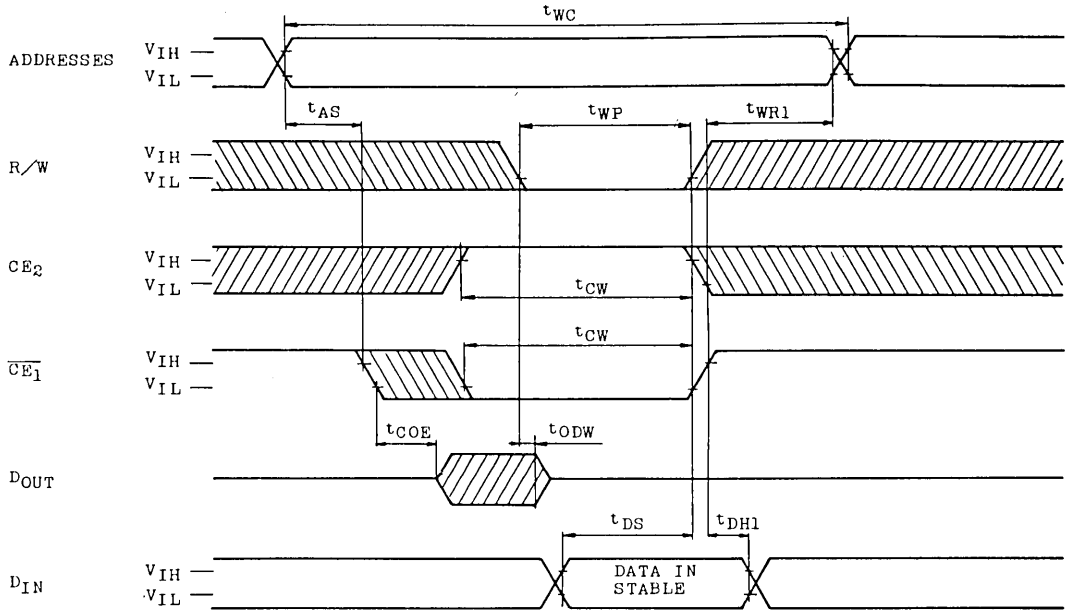
- READ CYCLE (1)



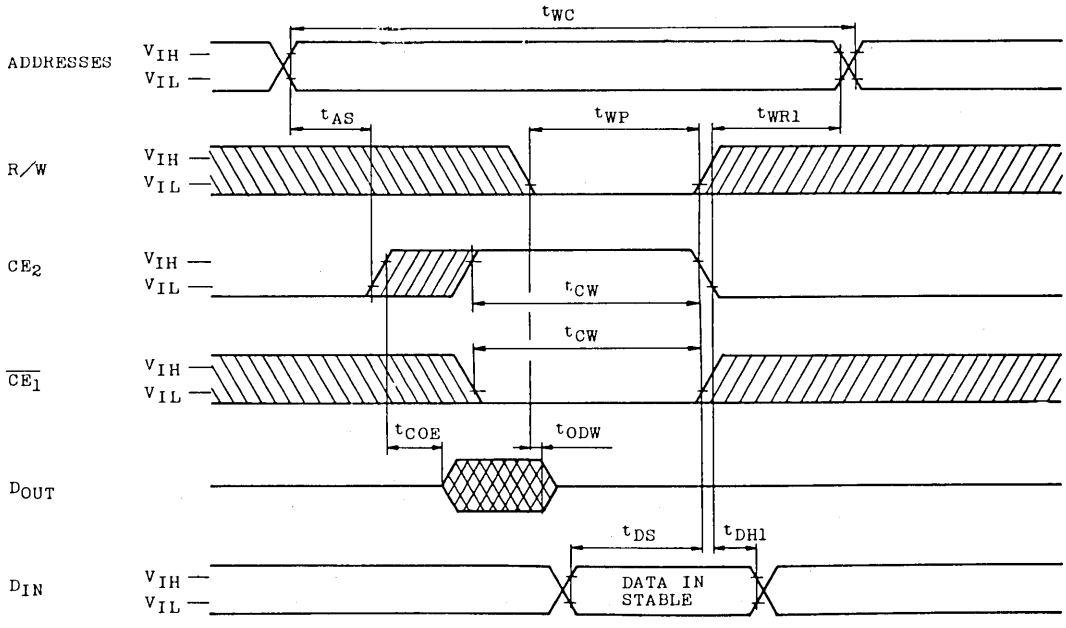
- WRITE CYCLE 1 (4) (R/W Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



- WRITE CYCLE 3 (4) (CE2 Controlled Write)



Note :

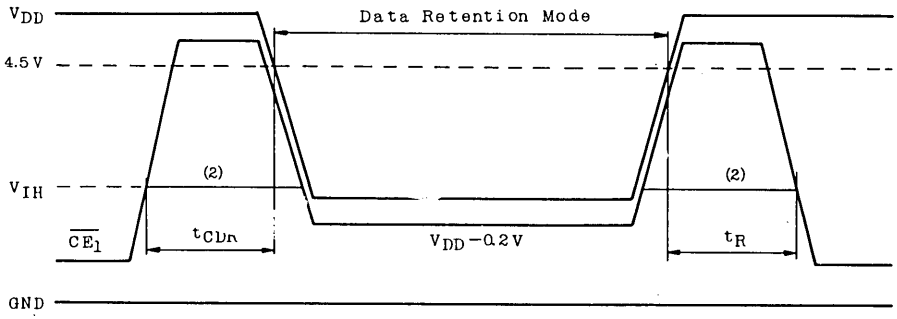
1. R/W is High for Read cycle,
2. Assuming that $\overline{CE_1}$ low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE_1}$ High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

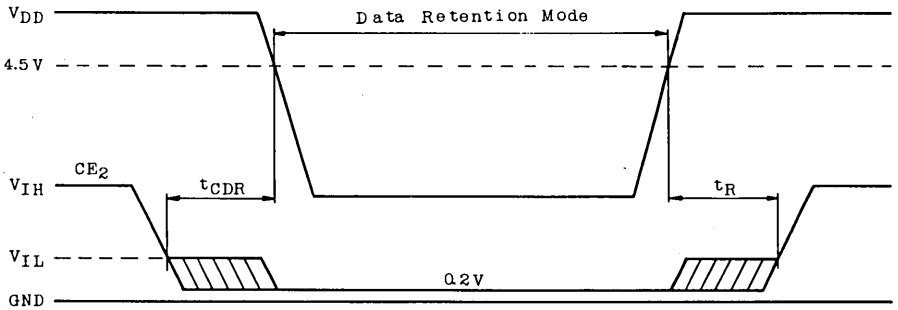
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Standby Supply Current	V_{DD}=3.0V	—	—	50	μA
		V_{DD}=5.5V	—	—	100	μA
t_{CDR}	Chip Deselection to Data Retntion Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}*	—	—	ns

* : Read cycle time.

● $\overline{CE1}$ Controlled Data Retention Mode (1)



● CE2 Controlled Data Retention Mode (3)



Note :

1. In $\overline{CE_1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE_1}$ is 2.2V in operation, I_{DDS_1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
3. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5563APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF. decoupling capacitor for every device is recommended to eliminate such noise.

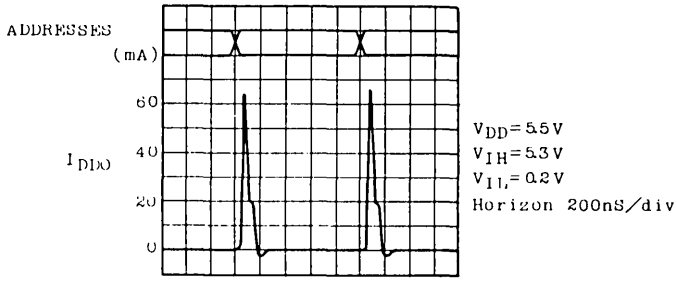
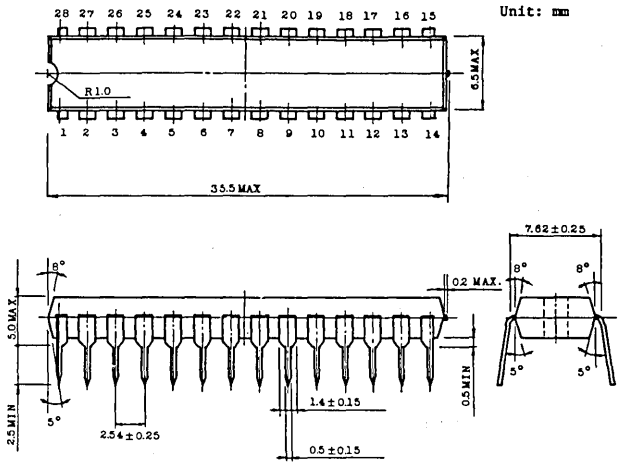


Fig. TYPICAL CURRENT WAVEFORMS

OUTLINE DRAWINGS

- DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT
CMOS STATIC RAM
SILICON GATE CMOS

TC5563APL-10L, TC5563APL-12L
TC5563APL-15L

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DESCRIPTION

The TC5563APL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns. When CE_2 is a logical low or $\overline{CE_1}$ is a logical high, the device is placed in low power standby mode in which standby current is 0.6μA typically. The TC5563APL has three control inputs. Two chip enables ($\overline{CE_1}$, CE_2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5563APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

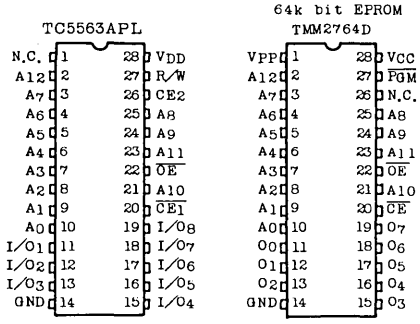
The TC5563APL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5563APL is offered in a dual-in-line 28 pin 0.3 inch width plastic package.

FEATURES

- Low Power Dissipation
  27.5mW/MHz (MAx.) Operating
- Standby Current : 1μA (Max.) Ta=25°C
- Access Time
  TC5563APL-10L : 100ns (Max.)
  TC5563APL-12L : 120ns (Max.)
  TC5563APL-15L : 150ns (Max.)
- 5V Single Power Supply
- Power Down Features : CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

PIN CONNECTION (TOP VIEW)



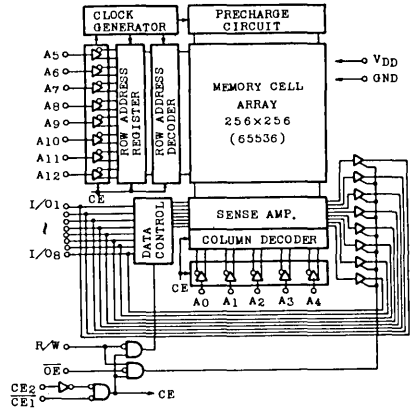
PIN NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package(SOP)	*TC5565AFL.

* : See TC5565APL/AFL Technical Date.

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	0.8	W
T_{SOLDER}	Soldering Temperature	260·10	°C·Sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

* : −3.0V at Pulse width 50ns

D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3*	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

* : −3.0V at Pulse width 50ns

D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}		—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V		−1.0	—	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		4.0	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL} or R/W=V_{IL} or $\overline{OE}$=V_{IH} V_{OUT}=0~V_{DD}		—	—	±1.0	μA
I_{DDO1}	operating Current	V_{DD}=5.5V Iout=0mA $\overline{CE_1}$=V_{IL} CE_2=V_{IH} Other Input=V_{IH}/V_{IL}	t_{CYCLE}=1μs	—	—	10	mA
			t_{CYCLE}=Min. cycle	—	—	45	
I_{DDO2}	Operating Current	V_{DD}=5.5V $\overline{CE_1}$=0.2V CE_2=V_{DD}−0.2V Other Input =V_{DD}−0.2V/0.2V	t_{CYCLE}=1μs	—	—	5	mA
		Iout=0mA	t_{CYCLE}=Min. cycle	—	—	40	
I_{DDS1}	Standby Current	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL}		—	—	3	mA
*I_{DDS2}	Standby Current	$\overline{CE_1}$=V_{DD}−0.2V or CE_2=0.2V	Ta=25°C	—	0.6	1.0	μA
			Ta=0~70°C	—	—	30	

* : In standby mode with $\overline{CE_1}$≧V_{DD}−0.2V, these specification limits are guaranteed under the condition of CE_2≧V_{DD}−0.2V or CE_2≦0.2V

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC5563APL-10L		TC5563APL-12L		TC5563APL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CE1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CE2 Access Time	—	100	—	120	—	150	
t_{OE}	Output Enable to Output Valid	—	50	—	60	—	70	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	—	10	—	15	—	
t_{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	—	35	—	40	—	50	
t_{ODO}	Output Enable to Output in High-Z	—	35	—	40	—	50	
t_{OH}	Output Data Hold Time	20	—	20	—	20	—	

Write Cycle

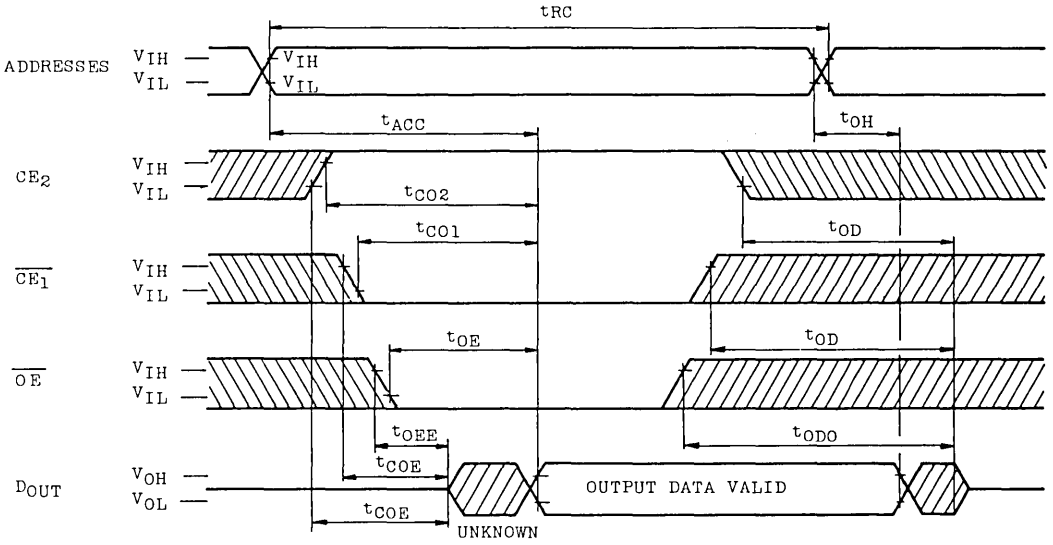
SYMBOL	PARAMETER	TC5563APL-10L		TC5563APL-12L		TC5563APL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{WP}	Write Pulse Width	60	—	70	—	90	—	
t_{CW}	Chip Selection to End of Write	80	—	85	—	100	—	
t_{AS}	Address Set up Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{ODW}	R/W to Output in High-Z	—	35	—	40	—	50	
t_{OEW}	R/W to Output in Low-Z	5	—	5	—	10	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

A. C. TEST CONDITIONS

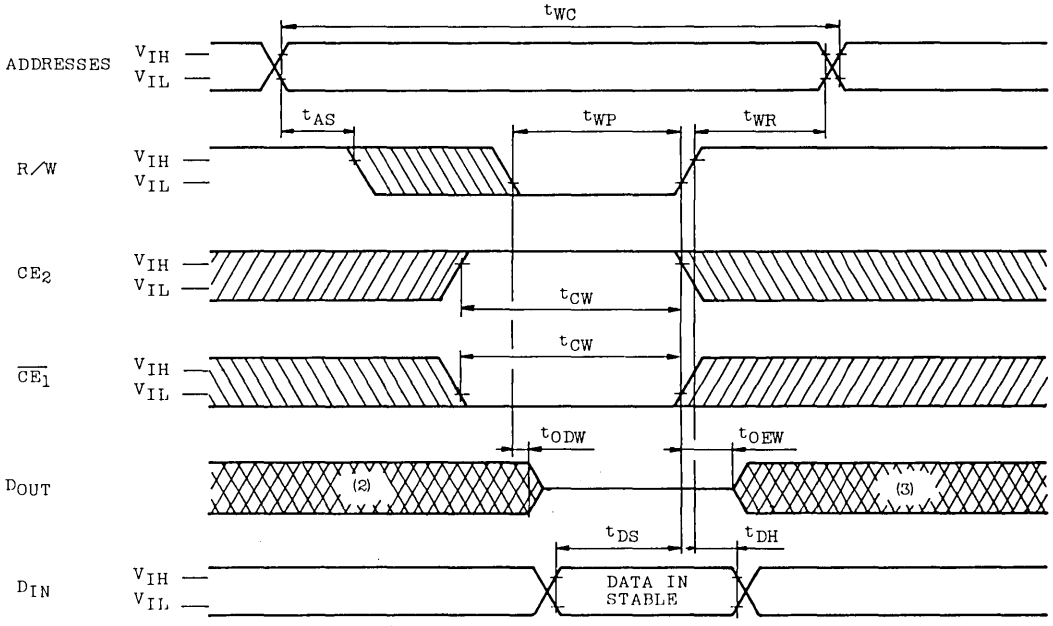
Output Load	: 100pF+1 TTL Gate
Input Pulse Level	: 0.6V, 2.4V
Timing Measurement Reference Level	V_{IN} : 0.8V, 2.2V V_{OUT} : 0.8V, 2.2V
t_r, t_f	: 5ns

TIMING WAVEFORMS

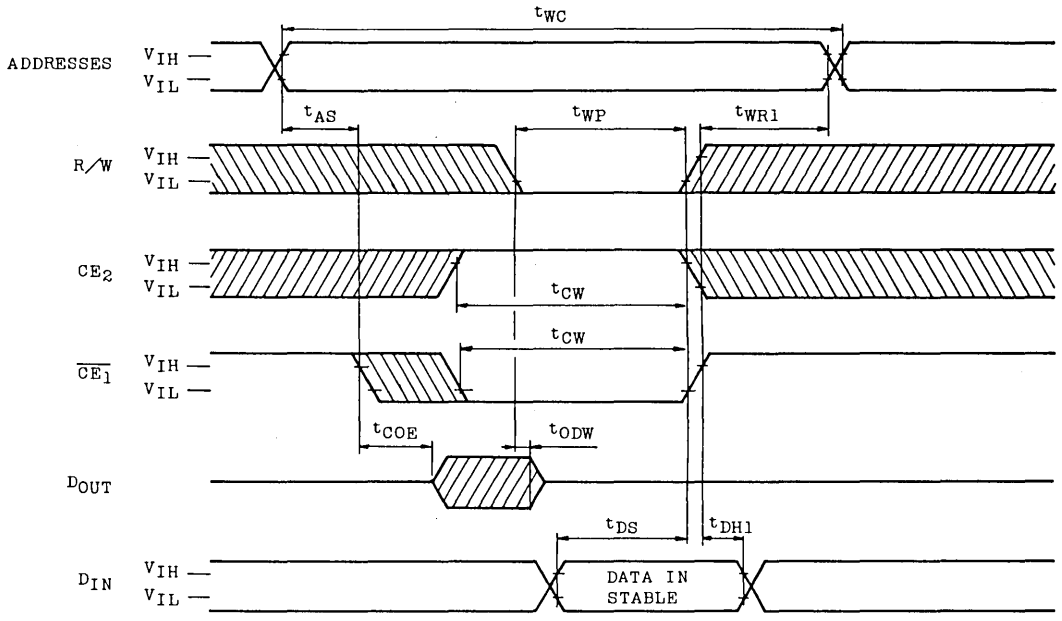
- READ CYCLE (1)



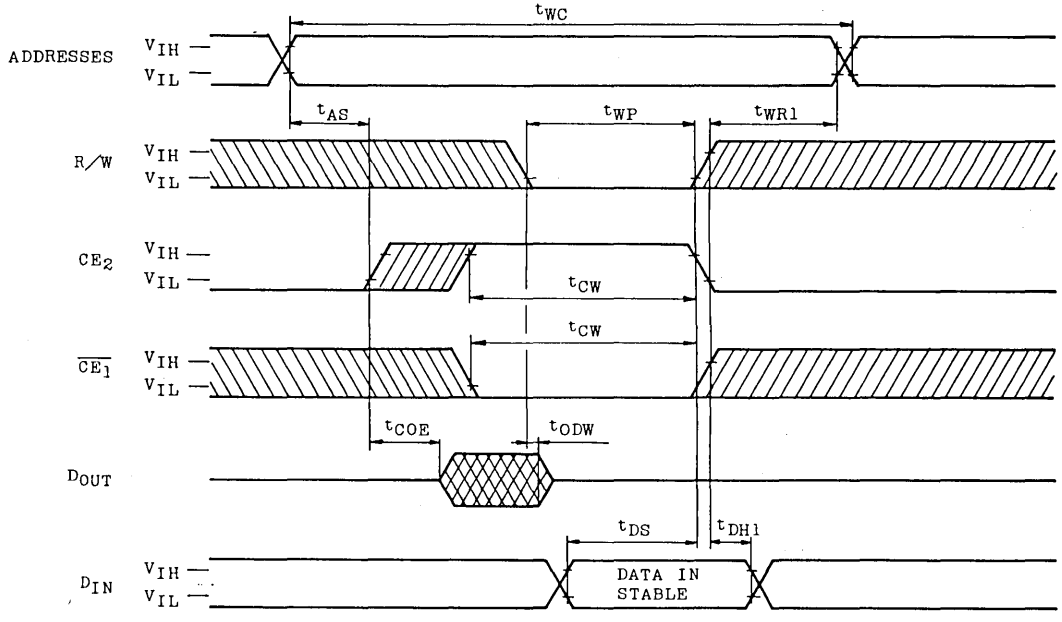
- WRITE CYCLE 1 (4) (R/W Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



- WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note :

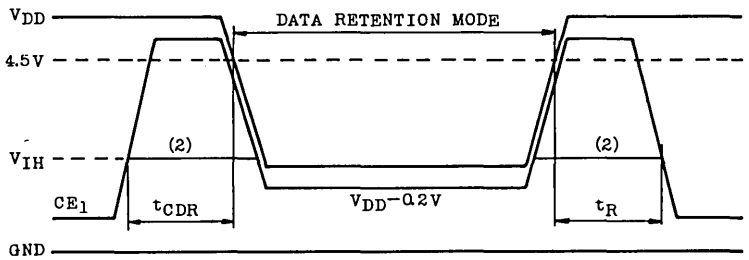
1. R/W is High for Read Cycle.
2. Assuming that $\overline{CE_1}$ Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE_1}$ High transition or CE_2 Low transition occures coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

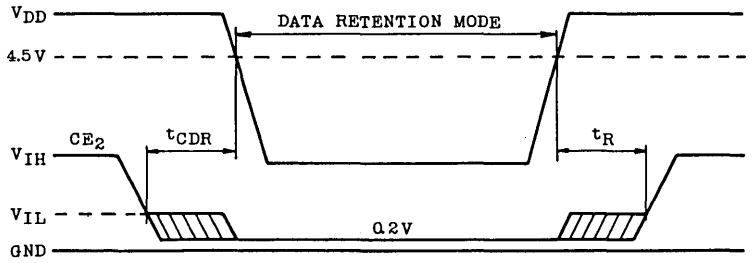
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Stand by Supply Current	V_{DD}=3.0V	—	—	15	μA
		V_{DD}=5.5V	—	—	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}*	—	—	ns

* : Read cycle time.

● $\overline{CE1}$ Controlled Data Retention Mode (1)



● CE2 Controlled Data Retention Mode (3)



Note :

1. In $\overline{CE_1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE_1}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
3. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5563APL/F is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

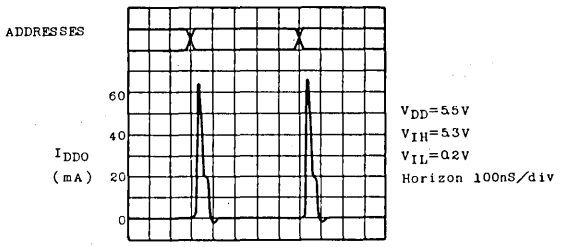
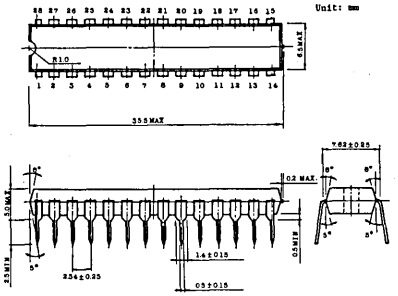


Fig. TYPICAL CURRENT WAVEFORMS

- DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

TC5565APL-10, TC5565APL-12, TC5565APL-15
TC5565AFL-10, TC5565AFL-12, TC5565AFL-15

DESCRIPTION

The TC5565APL/AFL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE2 is a logical low or $\overline{CE1}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5565APL/AFL has three control inputs. Two chip enable ($\overline{CE1}$, CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5565APL also features pin compatibility with the 64K bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems. The TC5565APL is offered in a dual-in-line 28 pin standard plastic package. The TC5565AFL is offered in 28 pin mini Flat Package.

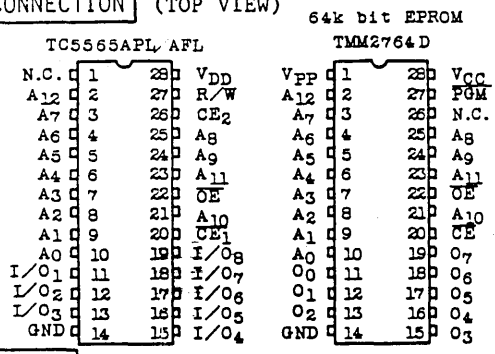
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current : 100μA(Max.) Ta=70°C
- Access Time
  TC5565APL/AFL-10 : 100ns(Max.)
  TC5565APL/AFL-12 : 120ns(Max.)
  TC5565APL/AFL-15 : 150ns(Max.)
- 5V Single Power Supply
- Power Down Features: CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage: 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	TC5565APL
300 mil DIP (Slim Package)	*TC5563APL
Flat Package (SOP)	TC5565AFL

*) See TC5563APL Technical Data.

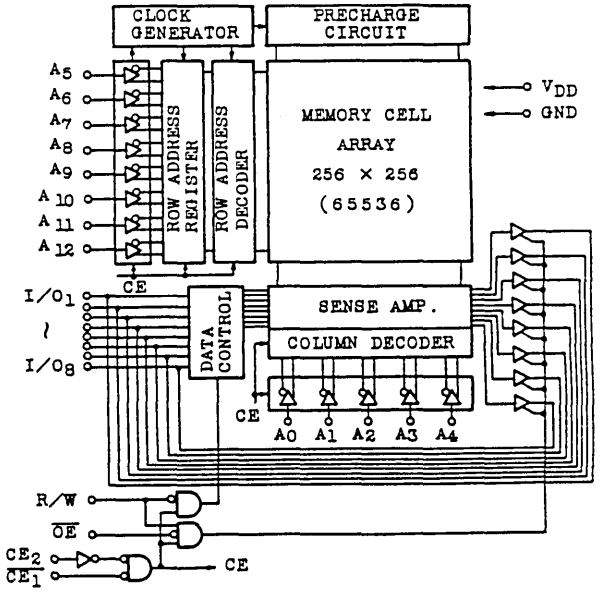
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A12	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1~I/O8	Data Input/Output
VDD	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}_1$	CE_2	$\overline{OE}$	R/W	I/O_1~I/O_8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3~7.0	V
V_{IN}	Input Voltage	*-0.3~7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{solder}	Soldering Temperature	260·10	°C·sec
T_{stg}	Storage Temperature	-55~150	°C
T_{opr}	Operating Temperature	0~70	°C

* -3.0V at pulse width 50ns MAX. ** Flat package

D.C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

D.C and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}			-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			-1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}_1$=V_{IH} or CE_2=V_{OL} or R/W=V_{IL} or $\overline{OE}$=V_{IH} V_{OUT}=0~V_{DD}			-	-	±1.0	μA
I_{DDO1}	Operating Current	V_{DD}=5.5V $\overline{CE}_1$=V_{IL} CE_2=V_{IH} Other input= V_{IH}/V_{IL}	t_{cycle}=1.0μs		-	-	10	mA
			TC5565APL-10 TC5565AFL-10	t_{cycle} =100ns	-	-	45	mA
			TC5565APL-12 TC5565AFL-12	t_{cycle} =120ns	-	-	40	mA
			TC5565APL-15 TC5565AFL-15	t_{cycle} =150ns	-	-	35	mA
I_{DDO2}		V_{DD}=5.5V $\overline{CE}_1$=0.2V CE_2=V_{DD}-0.2V Other input= V_{DD}-0.2V/0.2V	t_{cycle}=1.0μs		-	-	5	mA
			TC5565APL-10 TC5565AFL-10	t_{cycle} =100ns	-	-	40	mA
			TC5565APL-12 TC5565AFL-12	t_{cycle} =120ns	-	-	35	mA
			TC5565APL-15 TC5565AFL-15	t_{cycle} =150ns	-	-	30	mA
I_{DDS1}	Standby Current	$\overline{CE}_1$=V_{IH} or CE_2=V_{IL}			-	-	3	mA
*I_{DDS2}		$\overline{CE}_1$=V_{DD}-0.2V or CE_2=0.2V		V_{DD}=5.5V	-	2	100	μA
				V_{DD}=3.0V	-	1	50	μA

Note * : In standby mode with $\overline{CE}_1 \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE_2 \geqq V_{DD}-0.2V$ or $CE_2 \leqq 0.2V$.

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	-	-	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	-	-	10	pF

Note : This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0∿70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	120	-	150	-	ns
t_{ACC}	Address Access Time	-	100	-	120	-	150	ns
t_{CO1}	$\overline{CE}_1$ Access Time	-	100	-	120	-	150	ns
t_{CO2}	CE_2 Access Time	-	100	-	120	-	150	ns
t_{OE}	Output Enable to Output Valid	-	50	-	60	-	70	ns
t_{COE}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in Low-Z	10	-	10	-	15	-	ns
t_{OEE}	Output Enable to Output in Low-Z	5	-	5	-	5	-	ns
t_{OD}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in High-Z	-	35	-	40	-	50	ns
t_{ODO}	Output Enable to Output in High-Z	-	35	-	40	-	50	ns
t_{OH}	Output Data Hold Time	20	-	20	-	20	-	ns

Write Cycle

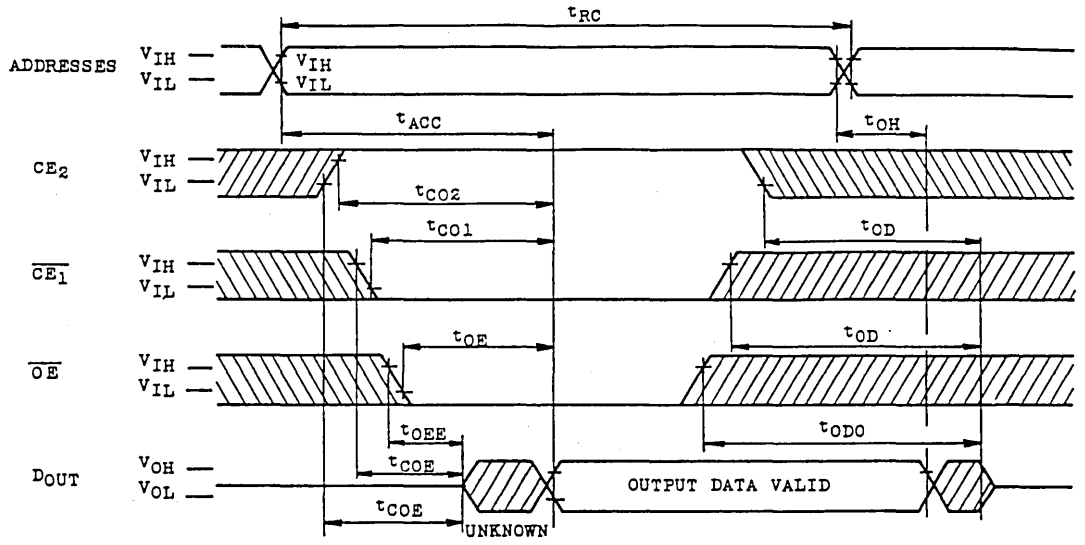
SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	120	-	150	-	ns
t_{WP}	Write Pulse Width	60	-	70	-	90	-	ns
t_{CW}	Chip Selection to End of Write	80	-	85	-	100	-	ns
t_{AS}	Address Set up Time	0	-	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{ODW}	R/W to Output High-Z	-	35	0	40	-	50	ns
t_{OEW}	R/W to Output Low-Z	5	-	5	-	10	-	ns
t_{DS}	Data Set up Time	40	-	50	-	60	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns

A.C. TEST CONDITION

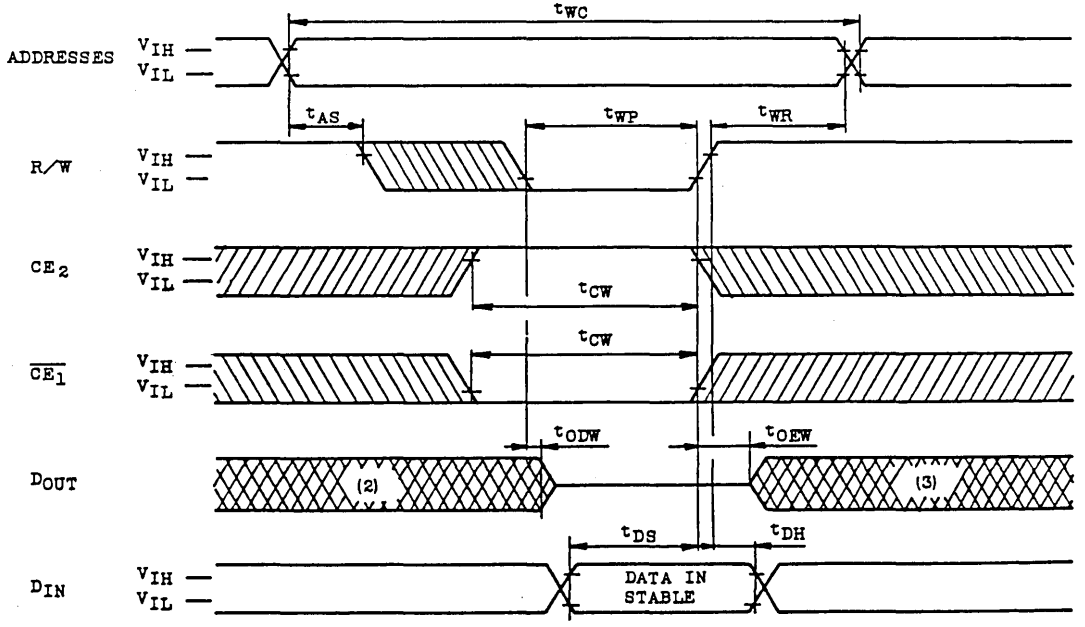
Output Load		: 100pF + 1 TTL Gate
Input Pulse Level		: 0.6V, 2.4V
Timing Measurement	V_{IN}	: 0.8V, 2.2V
Reference Level	V_{OUT}	: 0.8V, 2.2V
t_r, t_f		: 5ns

TIMING WAVEFORMS

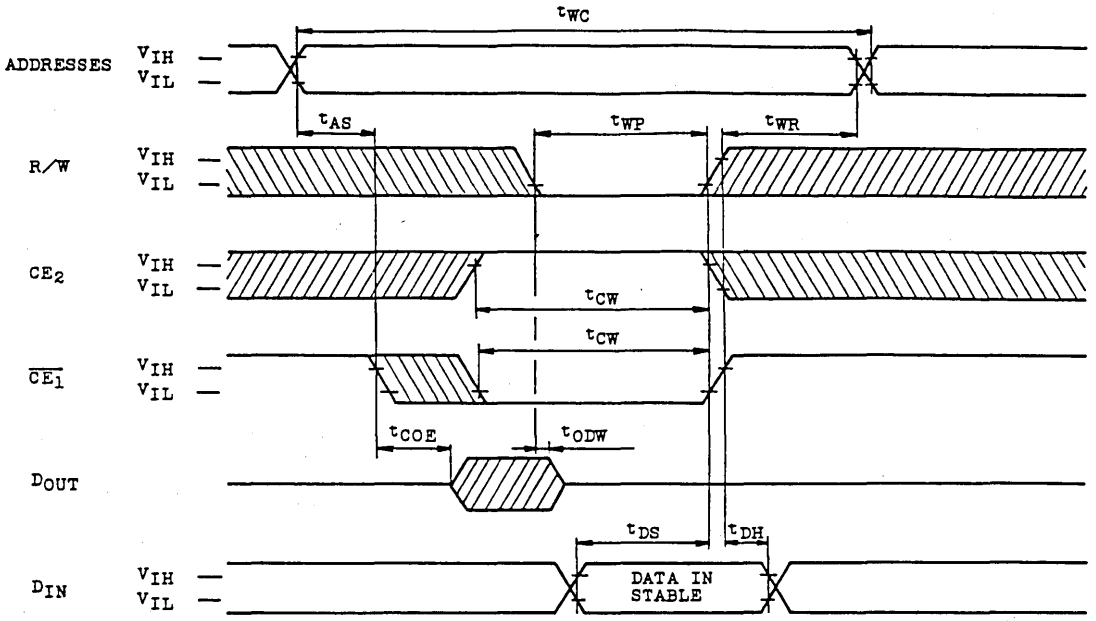
READ CYCLE (1)



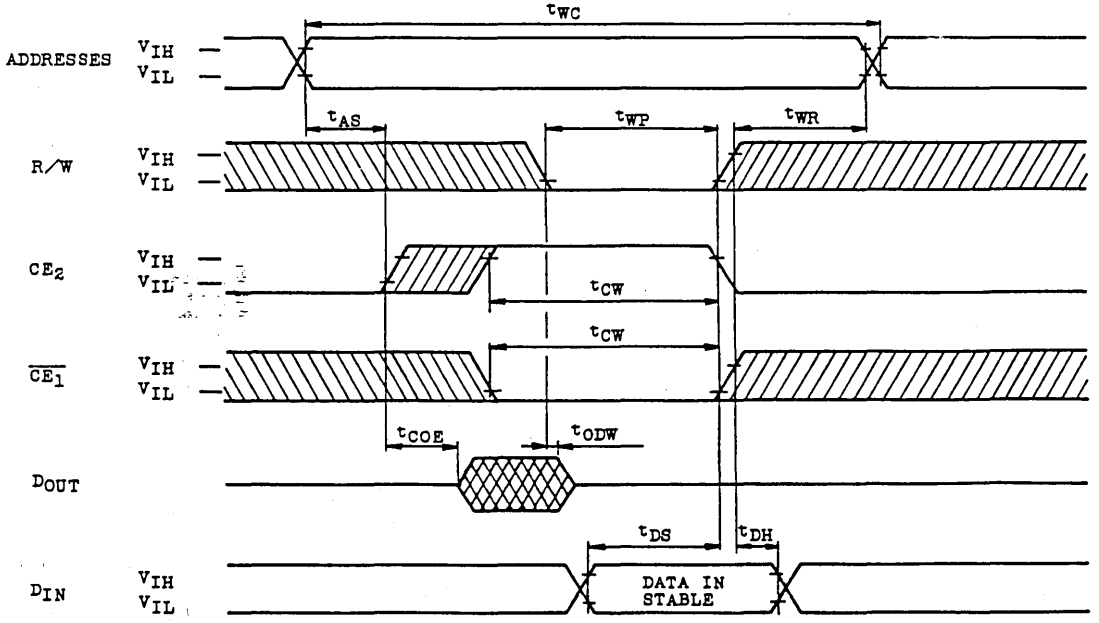
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE_1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}_1$ Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}_1$ High transition or CE_2 Low transition occure coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

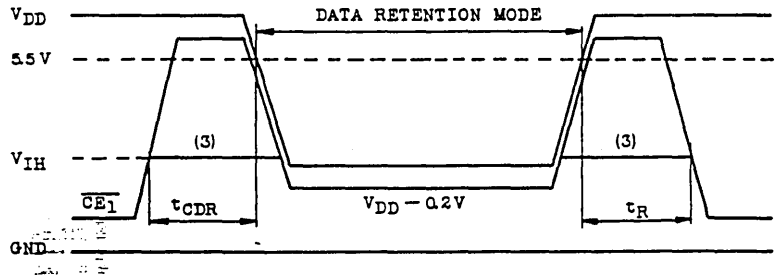
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

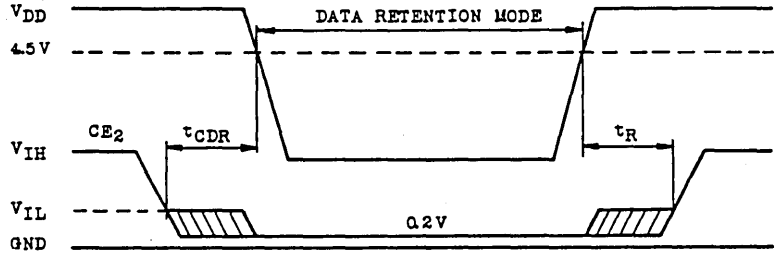
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Stand by Supply Current	V_{DD}=3.0V	-	-	50	μA
		V_{DD}=5.5V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μs
t_R	Recovery Time		t_{RC}(1)	-	-	μs

Note (1) : Read cycle time.

$\overline{CE}_1$ Controlled Data Retention Mode (2)



CE_2 Controlled Data Retention Mode (4)



Note 2 : In $\overline{CE}_1$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD}-0.2V$.

3 : If the V_{IH} of $\overline{CE}_1$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

4 : In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5565APL/AFL is an synchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

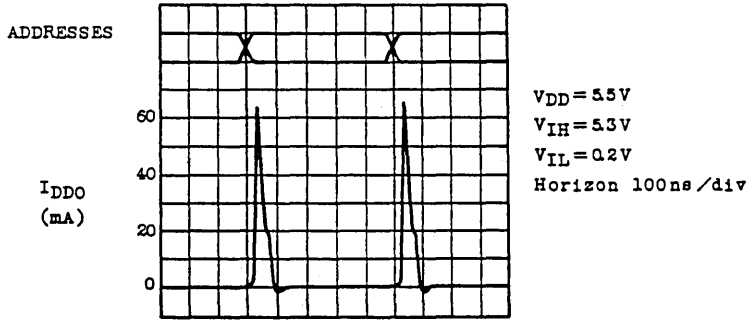
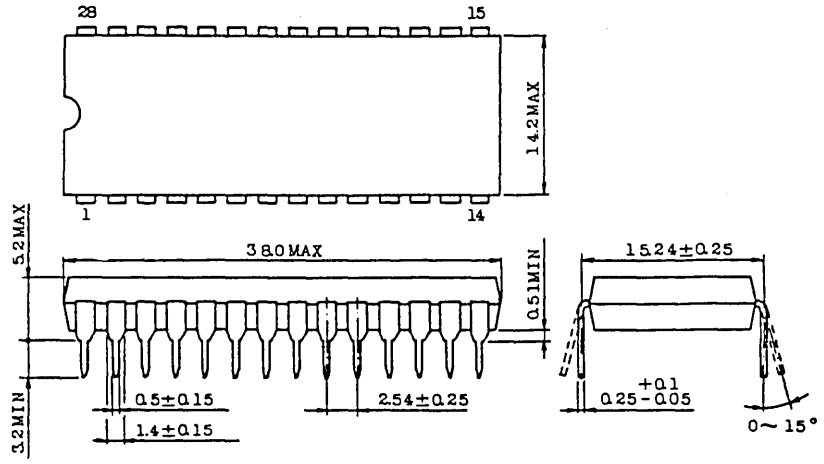


Fig. TYPICAL CURRENT WAVEFORMS

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

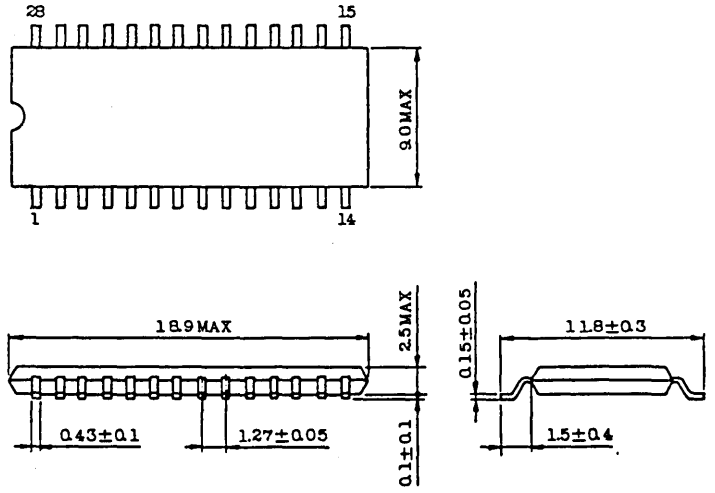
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

MFP 28 PIN OUTLINE DRAWING (F28GC-P)

Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5565APL-10L, TC5565APL-12L, TC5565APL-15L
TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L

DESCRIPTION

The TC5565APL/AFL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns. When CE_2 is a logical low or $\overline{CE_1}$ is a logical high, the device is placed in low power standby mode in which standby current is 0.6μA typically. The TC5565APL/AFL has three control inputs. Two chip enables ($\overline{CE_1}$, CE_2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5565APL/AFL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5565APL/AFL is offered in a dual-in-line 28 pin standard plastic package.

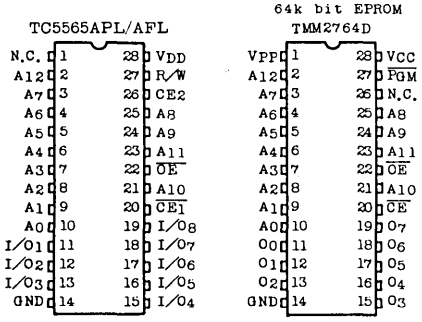
FEATURES

- Low Power Dissipation
  27.5mW/MHz (MAx.) Operating
- Standby Current : 1μA (Max.) Ta=25°C
- Access Time
  TC5565APL/AFL-10L : 100ns (Max.)
  TC5565APL/AFL-12L : 120ns (Max.)
  TC5565APL/AFL-15L : 150ns (Max.)
- 5V Single Power Supply
- Power Down Features : CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	TC5565APL
300 mil DIP (Slim Package)	*TC5563APL
Flat Package(SOP)	TC5565AFL

* : See TC5563APL Technical Date.

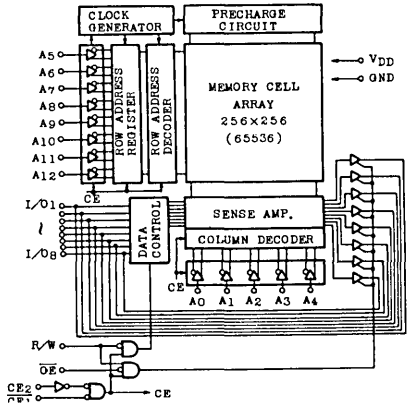
PIN CONNECTION (TOP VIEW)



NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature	260·10	°C·Sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

* : −3.0V at Pulse width 50ns
** : Flat package

D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3*	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

* : −3.0V at Pulse width 50ns

D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}		—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V		−1.0	—	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		4.0	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL} or R/W=V_{IL} or $\overline{OE}$=V_{IH} V_{OUT}=0~V_{DD}		—	—	±1.0	μA
I_{DDO1}	operating Current	V_{DD}=5.5V Iout=0mA $\overline{CE_1}$=V_{IL} CE_2=V_{IH} Other Input=V_{IH}/V_{IL}	t_{CYCLE}=1μs	—	—	10	mA
			t_{CYCLE}=Min. cycle	—	—	45	
I_{DDO2}	Operating Current	V_{DD}=5.5V $\overline{CE_1}$=0.2V CE_2=V_{DD}−0.2V Other Input Iout=0mA =V_{DD}−0.2V/0.2V	t_{CYCLE}=1μs	—	—	5	mA
			t_{CYCLE}=Min. cycle	—	—	40	
I_{DDS1}	Standby Current	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL}		—	—	3	mA
*I_{DDS2}	Standby Current	$\overline{CE_1}$=V_{DD}−0.2V or CE_2=0.2V	Ta=25°C	—	0.6	1.0	μA
			Ta=0~70°C	—	—	30	

* : In standby mode with $\overline{CE_1}$≧V_{DD}−0.2V, these specification limits are guaranteed under the condition of CE_2≧V_{DD}−0.2V or CE_2≦0.2V.

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS

(Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5565APL-10L TC5565AFL-10L		TC5565APL-12L TC5565AFL-12L		TC5565APL-15L TC5565AFL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CE1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CE2 Access Time	—	100	—	120	—	150	
t_{OE}	Output Enable to Output Valid	—	50	—	60	—	70	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	—	10	—	15	—	
t_{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	—	35	—	40	—	50	
t_{ODO}	Output Enable to Output in High-Z	—	35	—	40	—	50	
t_{OH}	Output Data Hold Time	20	—	20	—	20	—	

Write Cycle

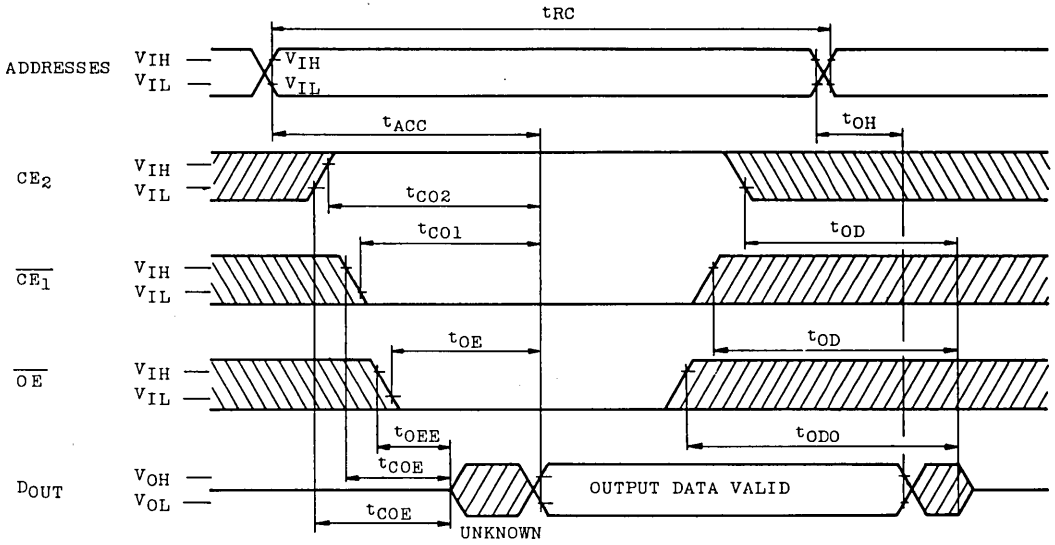
SYMBOL	PARAMETER	TC5565APL-10L TC5565AFL-10L		TC5565APL-12L TC5565AFL-12L		TC5565APL-15L TC5565AFL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{WP}	Write Pulse Width	60	—	70	—	90	—	
t_{CW}	Chip Selection to End of Write	80	—	85	—	100	—	
t_{AS}	Address Set up Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{ODW}	R/W to Output in High-Z	—	35	—	40	—	50	
t_{OEW}	R/W to Output in Low-Z	5	—	5	—	10	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

A. C. TEST CONDITIONS

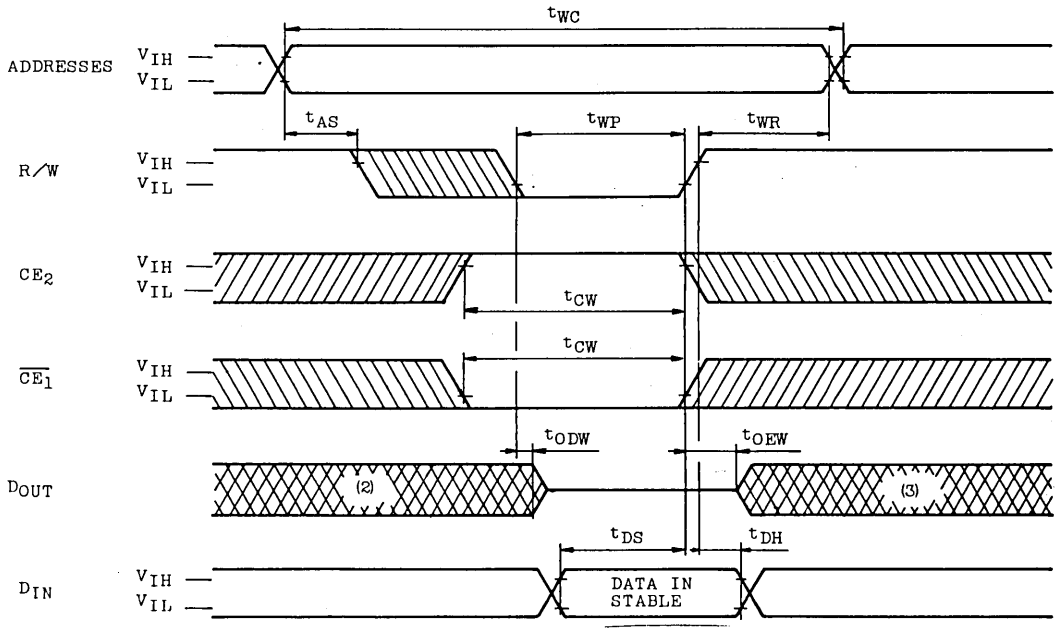
Output Load	: 100pF+1 TTL Gate
Input Pulse Level	: 0.6V, 2.4V
Timing Measurement Reference Level	V_{IN} : 0.8V, 2.2V V_{OUT} : 0.8V, 2.2V
t_r, t_f	: 5ns

TIMING WAVEFORMS

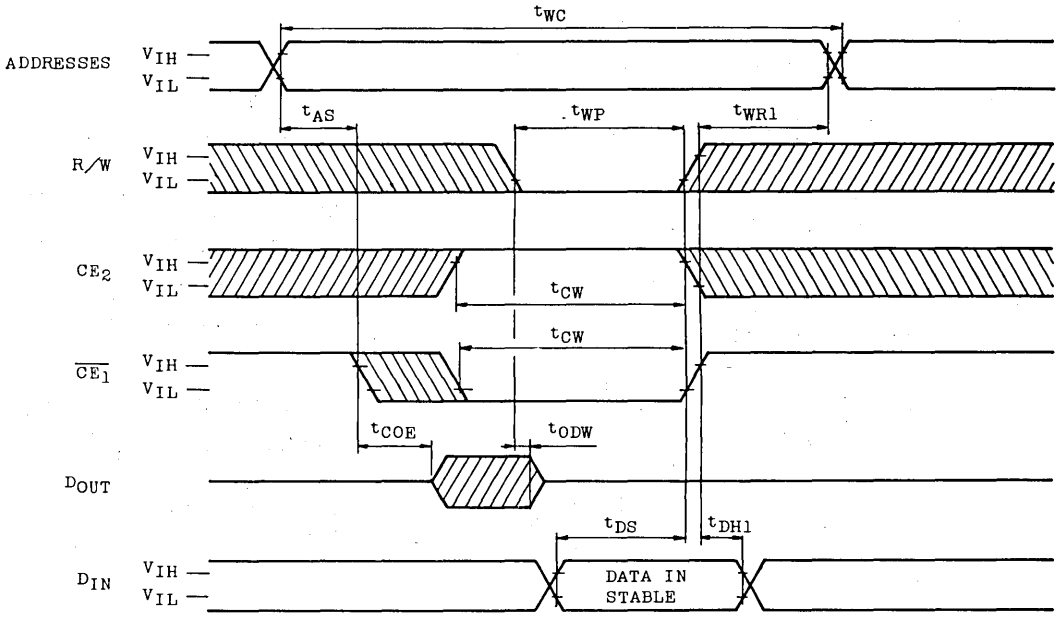
- READ CYCLE (1)



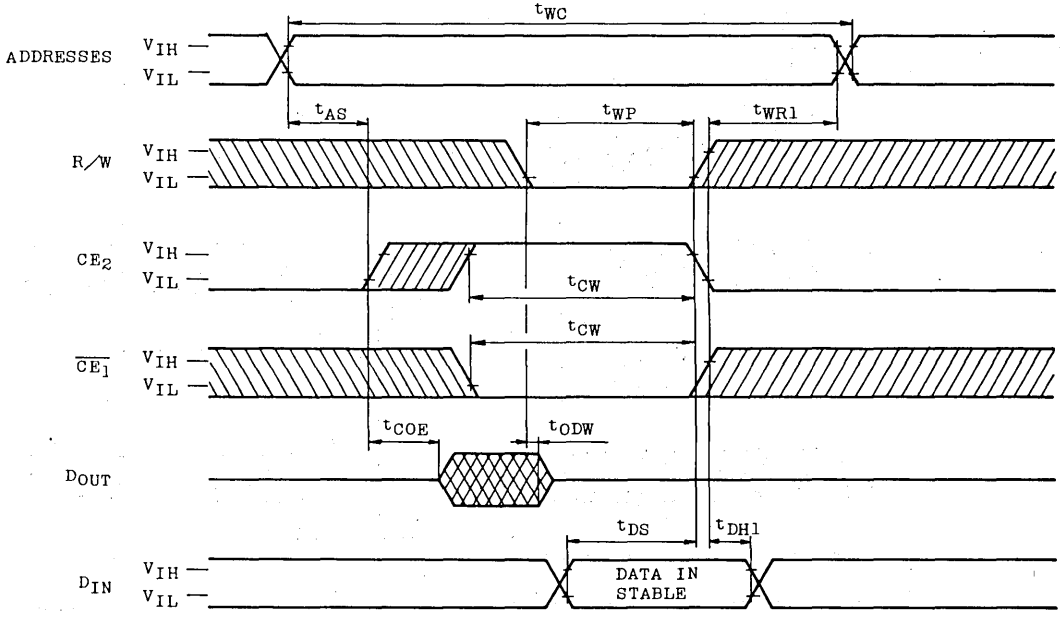
- WRITE CYCLE 1 (4) (R/W Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



- WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note :

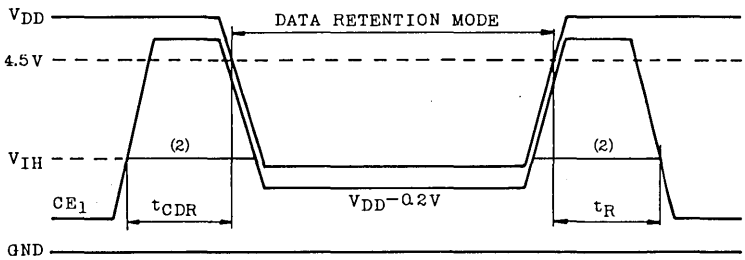
1. R/W is High for Read Cycle.
2. Assuming that $\overline{CE_1}$ Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE_1}$ High transition or CE_2 Low transition occure coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

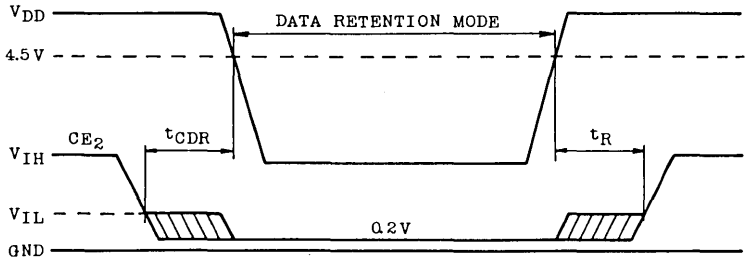
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Stand by Supply Current	V_{DD}=3.0V	—	—	15	μA
		V_{DD}=5.5V	—	—	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}*	—	—	ns

* : Read cycle time.

- $\overline{CE_1}$ Controlled Data Retention Mode (1)



- CE_2 Controlled Data Retention Mode (3)



Note :

1. In $\overline{CE_1}$ controlled data retention mode. minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE_1}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
3. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5565APL/AFL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

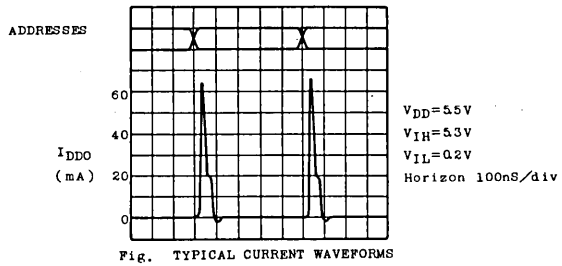
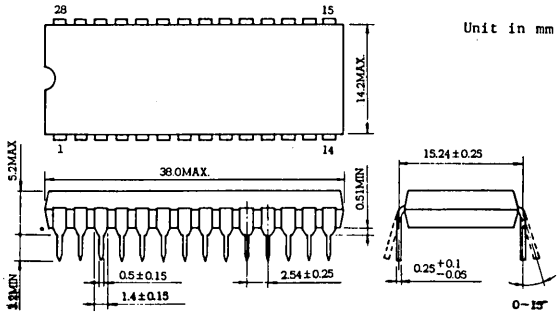


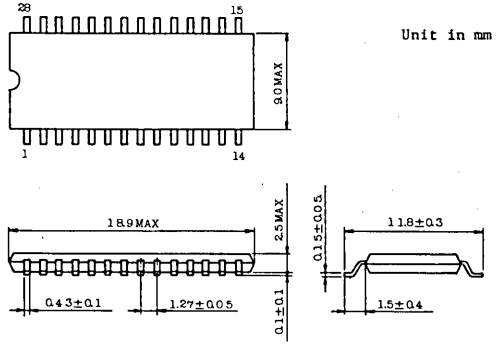
Fig. TYPICAL CURRENT WAVEFORMS

● DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

● MFP 28 PIN OUTLINE DRAWING (F28GC-P)



Note : Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT CMOS STATIC RAM

TC5564APL-12,TC5564APL-15
TC5564AFL-12,TC5564AFL-15

DESCRIPTION

TC5564APL is 65536 bits static random access memory organized as 8192 words by 8 bits using CMOS technology, and operates with a single 5V power supply.

Advanced circuit techniques provides low power feature with a maximum operating of 5mA/MHz. Operation current depends on cycle time.

TC5564APL has three control inputs. Two chip enables ($\overline{CE1}$, CE2) allow for device selection and data retention control. Output enable ($\overline{OE}$) input provides fast memory access. When device is placed in standby mode with chip off state, standby current is typically 0.01μA. So the TC5564APL is suitable for use in various microprocessor application systems where low power and battery back up are required. Ultra low standby power allow not only battery but capacitance backup.

Pin assignment of TC5564APL is pin-compatible with the 64K bits EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

TC5564APL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

FEATURES

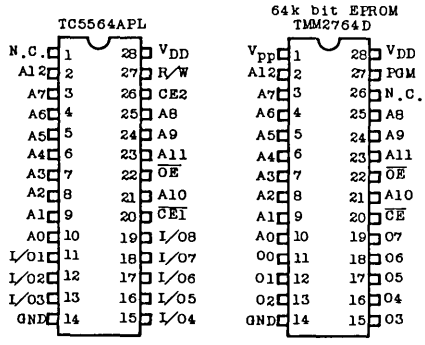
- Low Power Dissipation
  5mA/MHz (MAX.) Operating
  0.2μA (MAX.) at Ta=25°C Standby
  1.0μA (MAX.) at Ta=60°C Standby
- 5V Single Power Supply
- Low Voltage Operation : V_{DD}=3V
  T_{CO}=1μs (MAX.) Ta=60°C
- Fully Static Operation
- Data Retention Voltage : 2.0~5.5V
- Plastic DIP and Plastic FP Package
- Pin Compatible with 2764 type EPROM

- Access Time

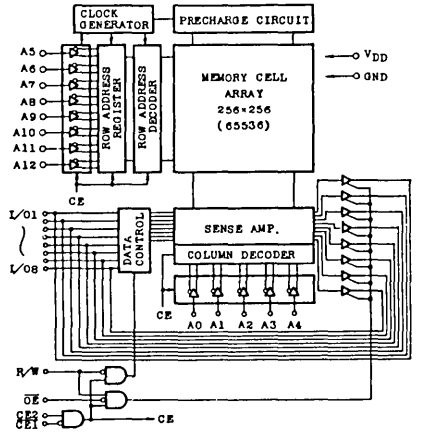
	TC5564APL-12 TC5564AFL-12	TC5564APL-15 TC5564AFL-15
Address Access Time (MAX.)	120ns	150ns
$\overline{CE1}$ Access Time (MAX.)	120ns	150ns
CE2 Access Time (MAX.)	120ns	150ns
Output Enable Time (MAX.)	60ns	70ns

- Directly TTL Compatible : All Inputs and Outputs
- Wide Temperature Operation : −40~85°C

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1~I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

OPERATING MODE

Operation Mode	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1~I/O8	Power
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	
Output Deselect	*	*	H	*	High-Z	
Standby	H	*	*	*	"	I_{DDS}
	*	L	*	*	"	I_{DDS}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
*V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3**~V_{DD}	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0(0.6)***	W
T_{solder}	Soldering Temperature	260·10	°C·sec
T_{stg}	Storage Temperature	−55~150	°C
T_{opr}	Operating Temperature	−40~85	°C

* 8.5V at 100ns
** −3.0V Pulse width 50ns
*** SOP

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = −40~85°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3*	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

* −3.0V Pulse width 50ns

D. C and OPERATING CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V±10% Unless other wise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IN}	Input Leakage Current	V_{IN} = 0~V_{DD}	—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	—	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	4.0	—	—	mA
V_{OH}	Output High Voltage	I_{OH} = −20μA	V_{DD}−0.1	—	—	V
V_{OL}	Output Low Voltage	I_{OL} = 20μA	—	—	0.1	V
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}	—	—	±1.0	μA

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP	MAX	UNIT
I_{DDO1}	Operating Current	$\overline{CE1}=V_{IL}$ and CE2 = V_{IH} Other Input = V_{IH}/V_{IL} I_{OUT}=0mA	$t_{cycle}=1\mu s$		—	—	10	mA
			MIN CYCLE	TC5564APL-12 TC5564AFL-12	—	—	45	
			MIN CYCLE	TC5564APL-15 TC5564AFL-15	—	—	40	
I_{DDO2}	Operating Current	$\overline{CE1}$=0.2V and CE2=V_{DD}−0.2V, Other Input =V_{DD}−0.2V/0.2V I_{OUT}=0mA	$t_{cycle}=1\mu s$		—	—	5	mA
			MIN CYCLE	TC5564APL-12 TC5564AFL-12	—	—	40	
			MIN CYCLE	TC5564APL-15 TC5564AFL-15	—	—	35	
I_{DDS1}	Standby Current	$\overline{CE1}=V_{IH}$ or CE2=V_{IL}			—	—	2	mA
I_{DDS2}	Standby Current	$\overline{CE_1}=V_{DD}-0.2V$ or CE2=0.2V V_{DD}=2.0~5.5V		Ta=25°C	—	0.01	0.2	μA
				Ta=60°C	—	—	1.0	

Note : (1) In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of CE2 $\geqq V_{DD}-0.2V$ or CE2 $\leqq$ 0.2V.
(2) All voltage is measured from GND.

CAPACITANCE (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

READ CYCLE

SYMBOL	PARAMETER	TC5564APL-12 TC5564AFL-12		TC5564APL-15 TC5564AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	120	—	150	—	ns
t_{ACC}	Address Access Time	—	120	—	150	
t_{CO1}	$\overline{CE1}$ Access Time	—	120	—	150	
t_{CO2}	CE2 Access Time	—	120	—	150	
t_{OE}	Output Enable to Output in Valid	—	60	—	70	
t_{COE}	Chip Enable to ($\overline{CE1}$, CE2) Output in Low-Z	10	—	10	—	
t_{OEE}	Output Enable to Output Low-Z	5	—	5	—	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) Output in High-Z	—	60	—	70	
t_{ODO}	Output Enable to Output High-Z	—	50	—	60	
t_{OH}	Output Data Hold Time	20	—	20	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC5564APL-12 TC5564AFL-12		TC5564APL-15 TC5564AFL-15		UNIT
		MIN	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	120	—	150	—	ns
t_{WP}	Write Pulse Width	80	—	100	—	
t_{CW}	Chip Selection to End of Write	100	—	120	—	
t_{AS}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W to Output High-Z	—	60	—	70	
t_{OEW}	R/W to Output Low-Z	10	—	10	—	
t_{DS}	Data Set Up Time	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	

A.C. TEST CONDITIONS

- Input Pulse Levels : 2.4V/0.6V
- Timing Measurement Reference Levels : 2.2V/0.8V
- Output Reference Levels : 2.2V/0.8V
- Input Pulse Rise and Fall Times : 5ns
- Output Load : See Fig.1

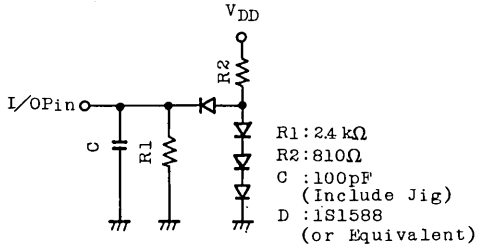


Fig.1 Output Lood

3V OPERATE SPECIFICATION

D. C RECOMMENDED OPERATING CONDITIONS (Ta = −10~60°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V
V_{IH}	Input High Voltage	$V_{DD}-0.2$	—	V_{DD}	V
V_{IL}	Input Low Voltage	0	—	0.2	V

D. C and OPERATING CHARACTERISTICS (Ta = −10~60°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IN}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$		—	—	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE1}=V_{IH}$ or $CE2=V_{IL}$ or $R/\overline{W}=V_{IL}$ or $\overline{OE}=V_{IH}$ $V_{OUT}=0\sim V_{DD}$		—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=V_{DD}-0.2V$		−100	—	—	μA
I_{OL}	Output Low Current	$V_{OL}=0.2V$		100	—	—	μA
V_{OH}	Output High Voltage	$I_{OH}=-20\mu A$		$V_{DD}-0.1$	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=20\mu A$		—	—	0.1	V
I_{DDO}*	operating Current	$\overline{CE1}=V_{IL}$ and $CE2=V_{IH}$ Other input= $V_{DD}-0.2V/0.2V$ I_{OUT}=0mA, duty 100%	$t_{cycle}=1\mu s$	—	2.0	3.0	mA
			$t_{cycle}=10\mu s$	—	—	0.5	
I_{DDS}	Standby Current Current	$\overline{CE1}=V_{IL}$ and $CE2=V_{IH}$ or $CE2=V_{IL}$	Ta=25°C	—	0.01	0.2	μA
			Ta=60°C	—	—	1.0	

- All voltage is measured from BND

* I_{DDO} is nlightly depending on input pulse t_r, t_f. If long t_r, t_f pulse is applied, there are some transient current at input stage. These specification is garanteed with t_r, $t_f \leqq 20ns$

3V OPERATE SPECIFICATION

A. C. CHARACTERISTICS (Ta = −10~60°C, V_{DD} 3V±10%)

READ CYCLE

SYMBOL	PARAMETER	MIN.	TYP.*	MAX.	UNIT
t_{RC}	Read Cycle Time	1000	—	—	ns
t_{ACC}	Address Access Time	—	300	1000	
t_{CO1}	$\overline{CE1}$ Access Time	—	300	1000	
t_{CO2}	CE2 Access Time	—	300	1000	
t_{OE}	Output Enable to Output Valid	—	100	200	
t_{OH}	Output Data Hold Time	20	—	—	
t_{COE}	Chip Enable to Output in Low Z	10	—	—	
t_{OEE}	Output Enable to Output in Low Z	5	—	—	
t_{OD}	Chip Enable to Output in High Z	—	—	200	
t_{ODO}	Output Enable to Output in High Z	—	—	150	

WRITE CYCLE

SYMBOL	PARAMETER	MIN.	TYP.*	MAX.	UNIT
t_{WC}	Write Cycle Time	1000	—	—	ns
t_{WP}	Write Pulse Width	500	—	—	
t_{CW}	Chip Selection to End of Write	800	—	—	
t_{AS}	Address Set Up Time	100	—	—	
t_{WR}	Write Recovery Time	100	—	—	
t_{DS}	Data Set Up Time	400	—	—	
t_{DH}	Data Hold Time	50	—	—	
t_{ODW}	R/W to Output High Z	—	—	200	
t_{OEW}	R/W to Output Low Z	10	—	—	

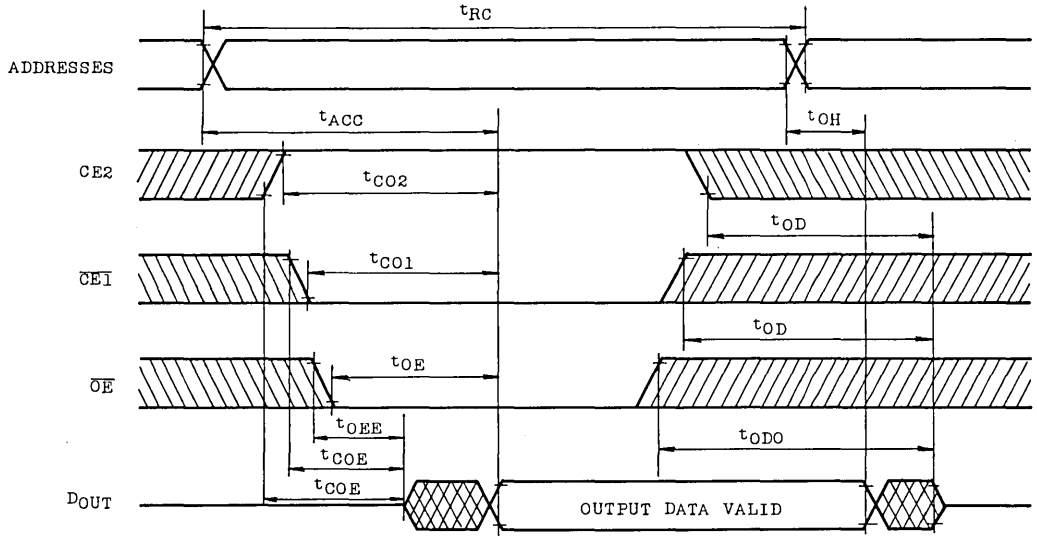
* Typ. condition is Ta=25°C, V_{DD}=3V

A. C. TEST CONDITIONS

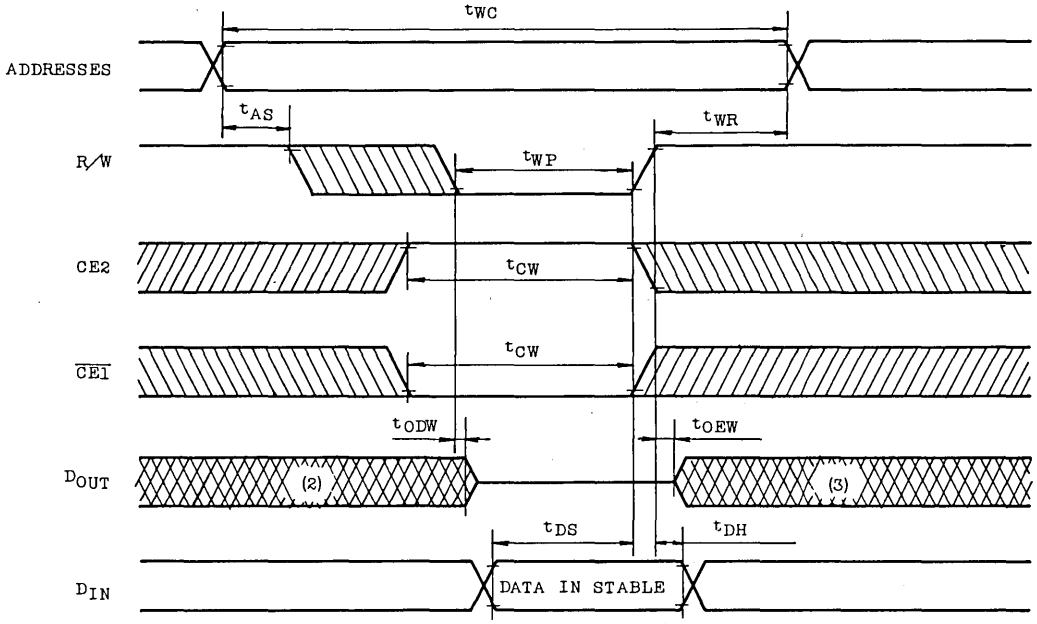
- $V_{IN}=V_{DD}-0.2V/0.2V$
- Output Reference Level : 1.5V/1.5V
- Timing Measurement Level : 1.5V/1.5V
- Input Rise and Fall Time : ≦20ns
- Output Load : 100pF (Include Jig)

TIMING WAVEFORMS

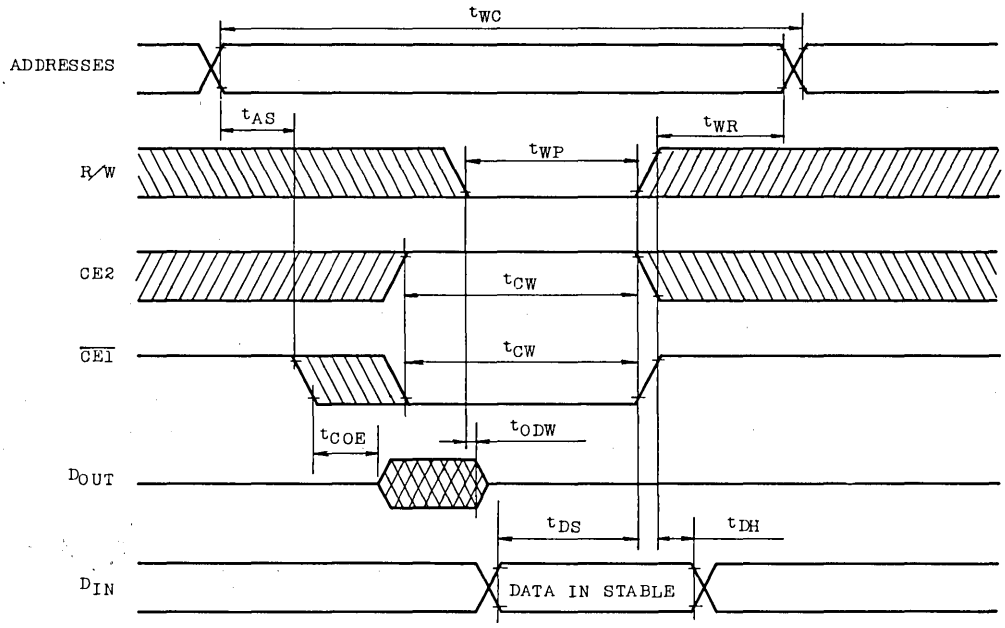
READ CYCLE (1)



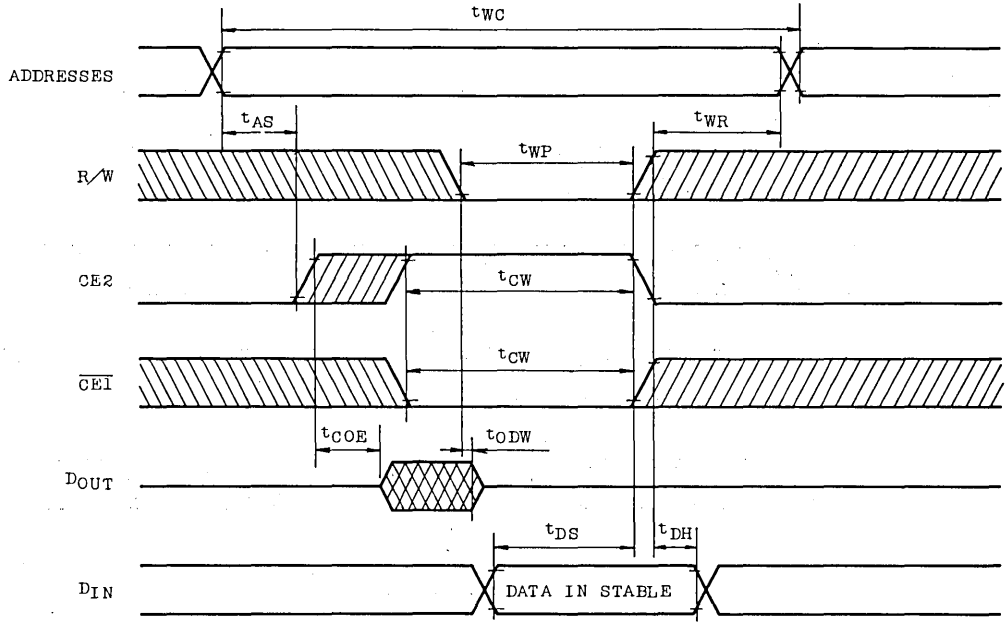
WRITE CYCLE (R/E Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)

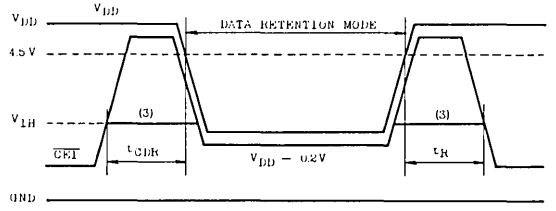


Note : (1) R/W is High for Read Cycle. (2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W low transition, Outputs remain in a high impedance state. (3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state. (4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

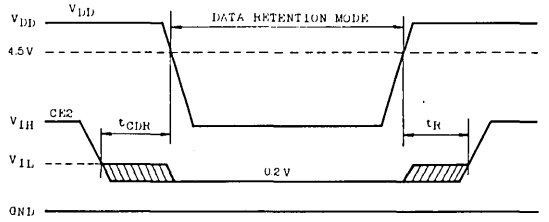
DATA RETENTION CHARACTERISTICS (Ta = −40~85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Standby Current	Ta=25°C	—	0.01	0.2	μA
		Ta=60°C	—	—	1.0	
t_{CDR}	Chip Deselection to Data Retention Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}(1)	—	—	ns

$\overline{CE1}$ Controlled Data Retention Mode (2)



CE2 Controlled Data Retention Mode (4)



Note : (1) T_{RC} : Read Cycle Time (2) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2≦0.2V or CE2≧V_{DD}−02V. (3) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} Voltage is going down from 4.5 to 2.4V, I_{DDS1} current flows. (4) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2≦0.2V.

DEVICE INFORMATION

The TC5564APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation executed by internal pulse generated from row address transient. Therefore the peak current flows after only row address change, as is shown in the following figure.

This peak current may induce the noise on V_{DD}/GND line. Thus the use of about 0.1μF decoupling capacitor every device is recommended to eliminate such noise.

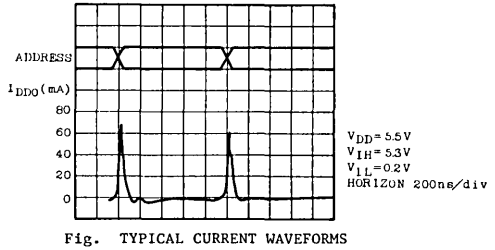
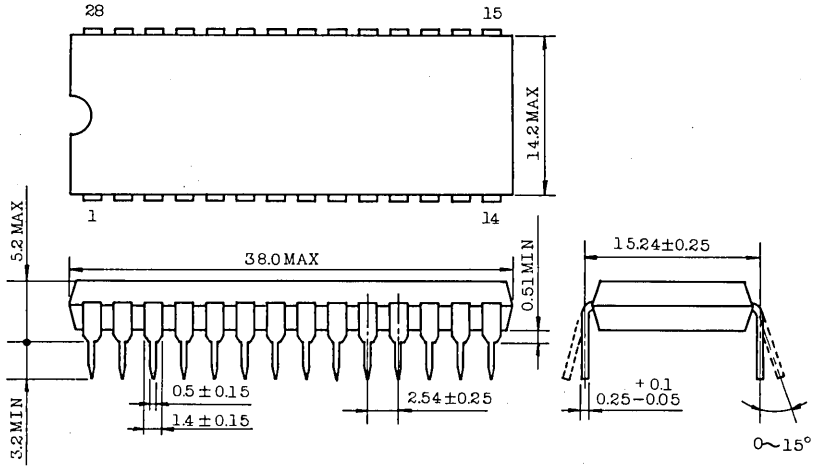


Fig. TYPICAL CURRENT WAVEFORMS

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

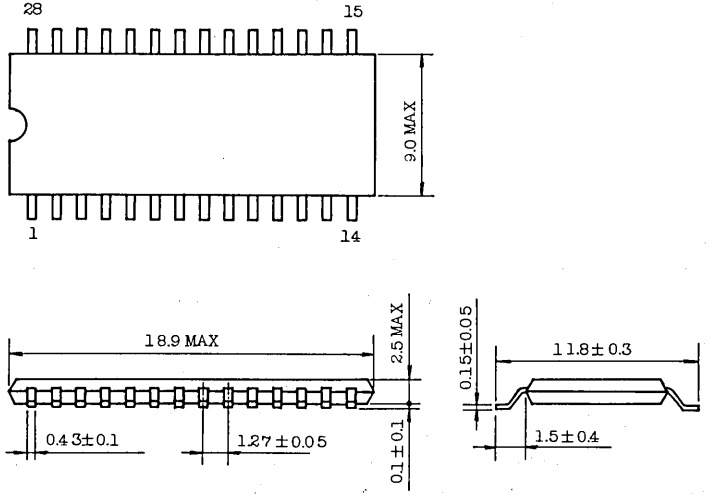
Unit in mm



Note : Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center or each lead that is obtained on the basis of No.1 and No.28 leads.

MFP 28 PIN OUTLINE DRAWINGS (F28GA-P)

Unit in mm



Note : Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

32,768 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC55257PL-85, TC55257P-10/PL-10
TC55257P-12/PL-12

DESCRIPTION

The TC55257P is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a operating current of 5mA/MHz(Typ.) and minimum cycle time of 85ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC55257P has two control inputs. Chip enable ($\overline{CE}$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257P is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257P is offered in a dual-in-line 28 pin standard plastic package.

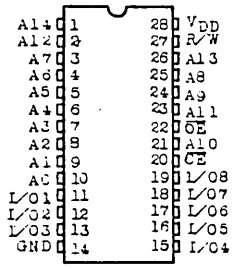
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current
  100uA(Max.): TC55257PL-85/PL-10/PL-12
  1mA(Max.): TC55257P-10/P-12
- 5V Single Power Supply
- Power Down Feature: $\overline{CE}$
- Data Retention Supply Voltage: 2.0 ∿ 5.5V
- Access Time

	TC55257PL-85	TC55257P-10 TC55257PL-10	TC55257P-12 TC55257PL-12
Access Time (Max.)	85ns	100ns	120ns
CE Access Time (Max.)	85ns	100ns	120ns
Output Enable Time(Max.)	40ns	50ns	60ns

- Directly TTL Compatible: All Inputs and Outputs
- Standard 28 pin DIP

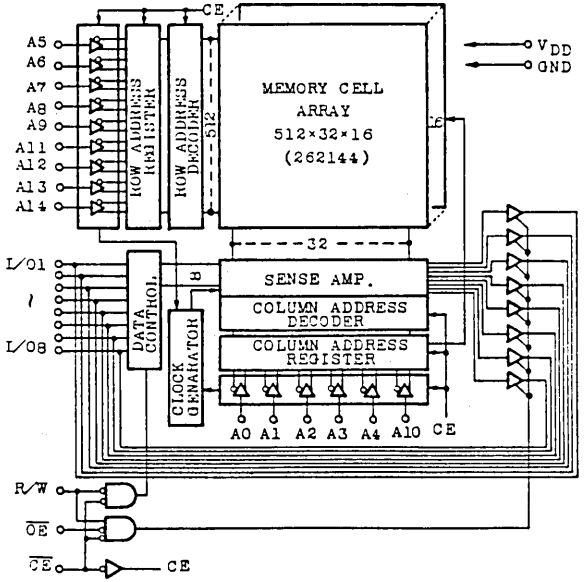
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*) H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3*~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature	260 • 10	°C•sec
T_{strg}	Storage Temperature	-55 ~ 150	°C
T_{opr}	Operating Temperature	0 ~ 70	°C

* ..... -3.0V at pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

D.C. and OPERATING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$		-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$		4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $R/W=V_{IL}$ or $\overline{OE}=V_{IH}$ $V_{OUT}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{DDO1}	Operating Current (Read Cycle)*	$V_{DD}=5.5V$ $\overline{CE}=V_{IL}$, $R/W=V_{IH}$ Other Input $=V_{IH}/V_{IL}$ $I_{OUT}=0mA$	t_{cycle}=1μs	-	-	10	mA
			t_{cycle}= Min. cycle	-	-	70	
I_{DDO2}		$V_{DD}=5.5V$ $\overline{CE}=0.2V$, $R/W=V_{DD}-0.2V$ Other Input $=V_{DD}-0.2V/0.2V$ $I_{OUT}=0mA$	t_{cycle}=1μs	-	-	5	mA
			t_{cycle}= Min. cycle	-	-	60	
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$		-	-	3	mA
I_{DDS2}	Standby Current	$\overline{CE}=V_{DD}-0.2V$ $V_{DD}=2.0 \sim 5.5V$	TC55257PL	-	2	100	μA
			TC55257P	-	-	1.0	mA

* Assuming that R/W is Low for Write Cycle, the current consumption is twice as much as that when R/W is High for Write Cycle.

CAPACITANCE ($Ta=25°C$, $f=1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ~ 70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257PL-85		TC55257P-10 /PL-10		TC55257P-12 /PL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	V_{IN}=2.4V/0.6V V_{IH}=2.2V V_{IL}=0.8V t_r, t_f≦5ns V_{OH}=2.2V V_{OL}=0.8V Output Load: C_L(100pF) and 1 TTL Gate	85	-	100	-	120	-	ns
t_{ACC}	Address Access Time		-	85	-	100	-	120	
t_{CO}	$\overline{CE}$ Access Time		-	85	-	100	-	120	
t_{OE}	Output Enable to Output in Valid		-	40	-	50	-	60	
t_{COE}	Chip Enable($\overline{CE}$)to Output in Low-Z		10	-	10	-	10	-	
t_{OEE}	Output Enable to Output in Low-Z		5	-	5	-	5	-	
t_{OD}	Chip Enable($\overline{CE}$)to Output in High-Z		-	30	-	50	-	60	
t_{ODO}	Output Enable to Output in High-Z		-	30	-	40	-	50	
t_{OH}	Output Data Hold Time		5	-	10	-	10	-	

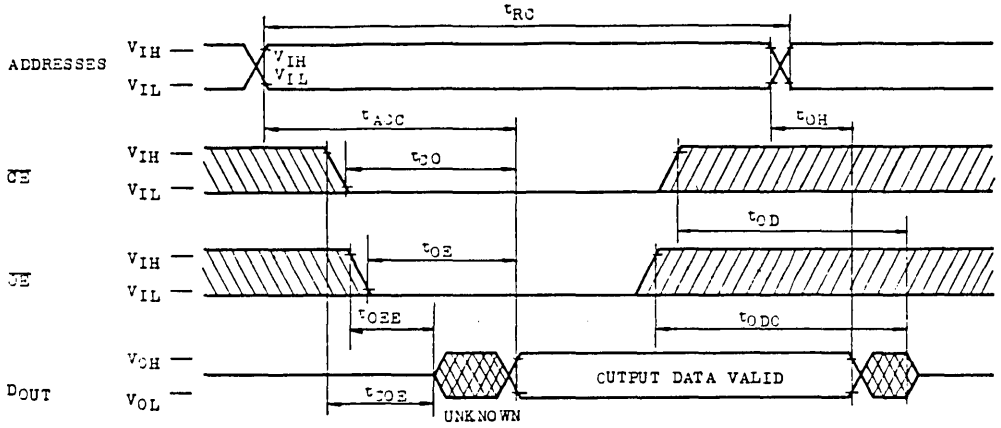
Write Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257PL-85		TC55257P-10 /PL-10		TC55257P-12 /PL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	V_{IN}=2.4V/0.6V V_{IH}=2.2V V_{IL}=0.8V t_r, t_f≦5ns	85	-	100	-	120	-	ns
t_{WP}	Write Pulse Width		60	-	70	-	80	-	
t_{CW}	Chip Selection to End of Write		65	-	90	-	100	-	
t_{AS}	Address Set up Time		0	-	0	-	0	-	
t_{WR}	Write Recovery Time		10	-	10	-	10	-	
t_{ODW}	R/W to Output High-Z		-	30	-	50	-	60	
t_{OEW}	R/W to Output Low-Z		10	-	10	-	10	-	
t_{DS}	Data Set up Time		40	-	40	-	50	-	
t_{DH}	Data Hold Time		0	-	0	-	0	-	

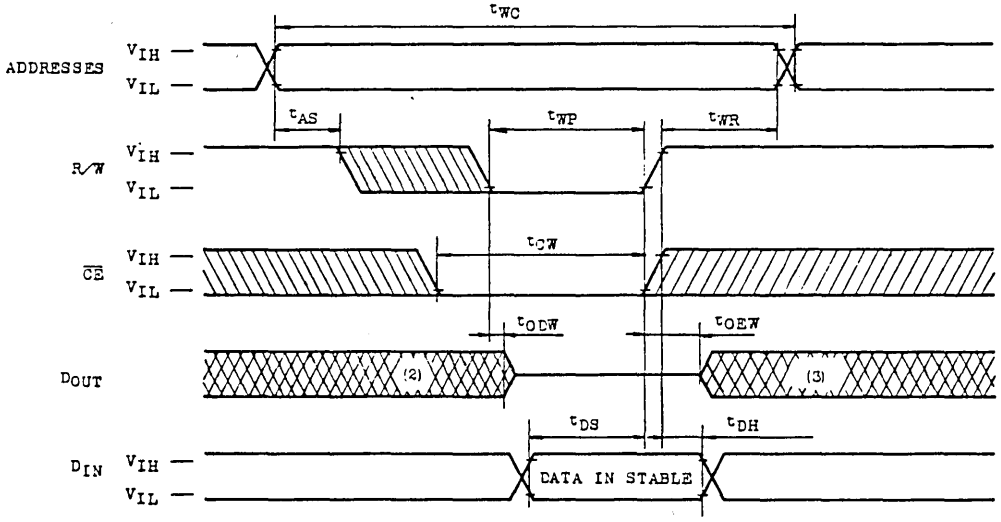
Note: Input pulse levels=V_{IN}
Timing Measurement Reference levels=V_{IH}, V_{IL}

TIMING WAVEFORMS

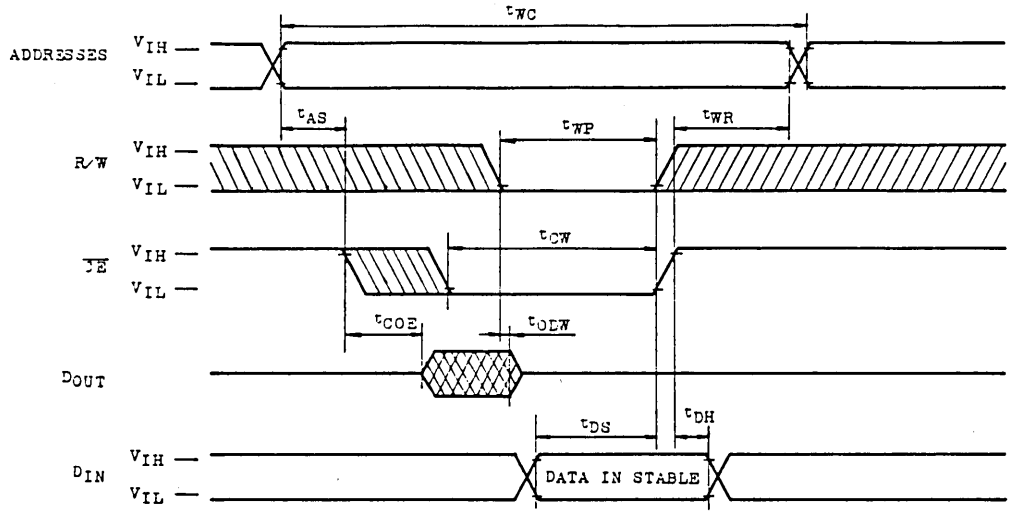
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



Note: 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

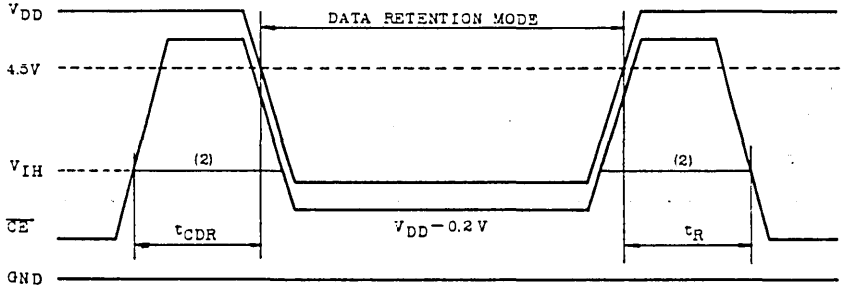
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage			2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	TC55257PL	V_{DD}=3.0V	-	-	50	μA
			V_{DD}=5.5V	-	-	100	
		TC55257P		-	-	1.0	mA
t_{CDR}	Chip Deselection to Data Retention Mode			0	-	-	μs
t_R	Recovery Time			t_{RC}(1)	-	-	

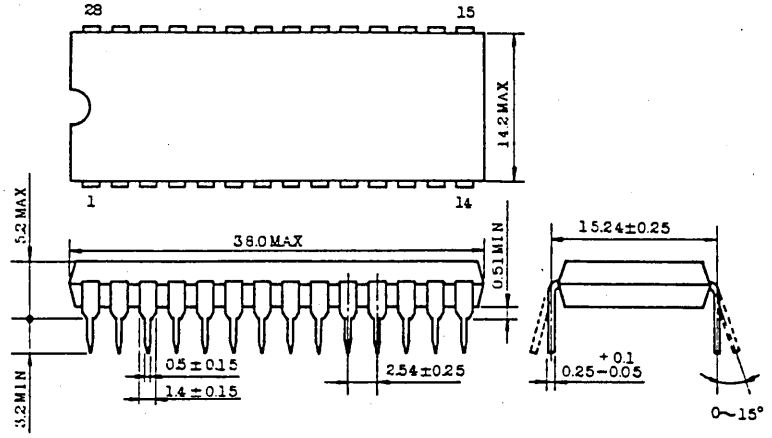
Note (1): Read cycle time

$\overline{CE}$ Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{CE}$ is 2.4V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

DIP 28 PIN OUTLINE DRAWING (6D28A-P) Unit in mm



Note: Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

32,768 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS
PRELIMINARY

TC55257AP-10/APL-10/AP-12/APL-12
TC55257AF-10/AFL-10/AF-12/AFL-12

DESCRIPTION

The TC55257AP is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and minimum cycle time of 100ns/120ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC55257AP has two control inputs. Chip enable (CE) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257AP is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

TC55257AP is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

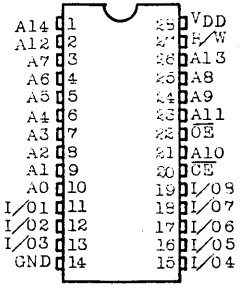
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current
  100μA(Max.): TC55257APL-10/APL-12
  /AFL-10/AFL-12
  1mA(Max.): TC55257AP-10/AP-12
  /AF-10/AF-12
- 5V Single Power Supply
- Power Down Feature: $\overline{CE}$
- Data Retention Supply Voltage:
  2.0 ∿ 5.5V
- Access Time

	TC55257AP-10/APL-10 AF-10/AFL-10	TC55257AP-12/APL-12 AF-12/AFL-12
Access Time(MAX.)	100ns	120ns
CE Access Time(MAX.)	100ns	120ns
Output Enable Time (MAX.)	50ns	60ns

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP and Plastic FP Package

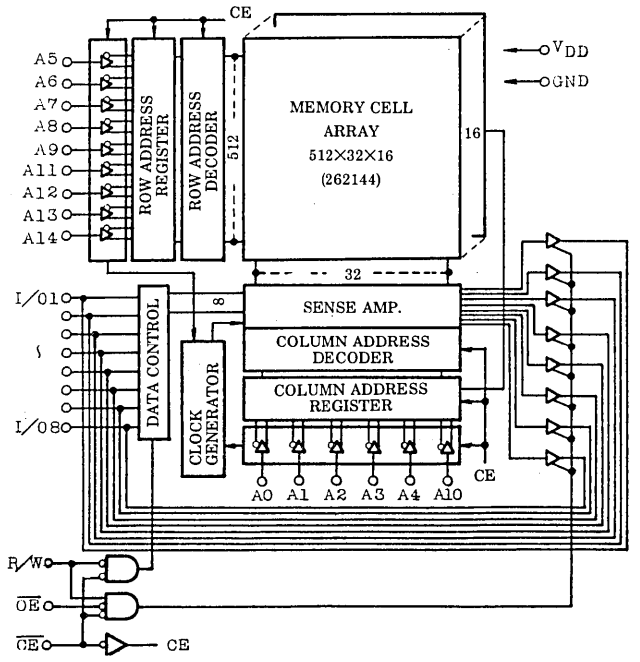
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ∿ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ∿ I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*) H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ∿ 7.0	V
V_{IN}	Input Voltage	-0.3* ∿ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ∿ V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature	260 • 10	°C • sec
T_{strg}	Storage Temperature	-55 ∿ 150	°C
T_{opr}	Operating Temperature	0 ∿ 70	°C

* ..... -3.0V at pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

D.C. and OPERATING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$		-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$		4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $R/\overline{W}=V_{IL}$ or $\overline{OE}=V_{IH}$ $V_{OUT}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{DDO1}	Operating Current (Read Cycle)*	$V_{DD}=5.5V$ $\overline{CE}=V_{IL}$, $R/\overline{W}=V_{IH}$ Other Input $=V_{IH}/V_{IL}$ $I_{OUT}=0mA$	$t_{cycle}=1\mu s$	-	-	10	mA
			$t_{cycle}=$ Min. cycle	-	-	45	
I_{DDO2}		$V_{DD}=5.5V$ $\overline{CE}=0.2V$, $R/\overline{W}=V_{DD}-0.2V$ Other Input $=V_{DD}-0.2V/0.2V$ $I_{OUT}=0mA$	$t_{cycle}=1\mu s$	-	-	5	mA
			$t_{cycle}=$ Min. cycle	-	-	40	
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$		-	-	3	mA
I_{DDS2}	Standby Current	$\overline{CE}=V_{DD}-0.2V$ $V_{DD}=2.0 \sim 5.5V$	TC55257APL/AFL	-	2	100	μA
			TC55257AP/AF	-	-	1.0	mA

* Assuming that R/W is Low for Write Cycle, the current consumption is twice as much as that when R/W is High for Write Cycle

CAPACITANCE ($Ta=25°C$, $f=1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT}=GND$	10	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257AP-10/APL-10 AF-10/AFL-10		TC55257AP-12/APL-12 AF-12/AFL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	$V_{IN}=2.4V/0.6V$	100	-	120	-	ns
t_{ACC}	Address Access Time	$V_{IH}=2.2V$	-	100	-	120	
t_{CO}	$\overline{CE}$ Access Time	$V_{IL}=0.8V$	-	100	-	120	
t_{OE}	Output Enable to Output in Valid	t_r, $t_f \leqq 5ns$	-	50	-	60	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	$V_{OH}=2.2V$ $V_{OL}=0.8V$	10	-	10	-	
t_{OEE}	Output Enable to Output in Low-Z	Output Load: C_L(100pF) and 1 TTL Gate	5	-	5	-	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z		-	50	-	60	
t_{ODO}	Output Enable to Output in High-Z		-	40	-	50	
t_{OH}	Output Data Hold Time		10	-	10	-	

Write Cycle

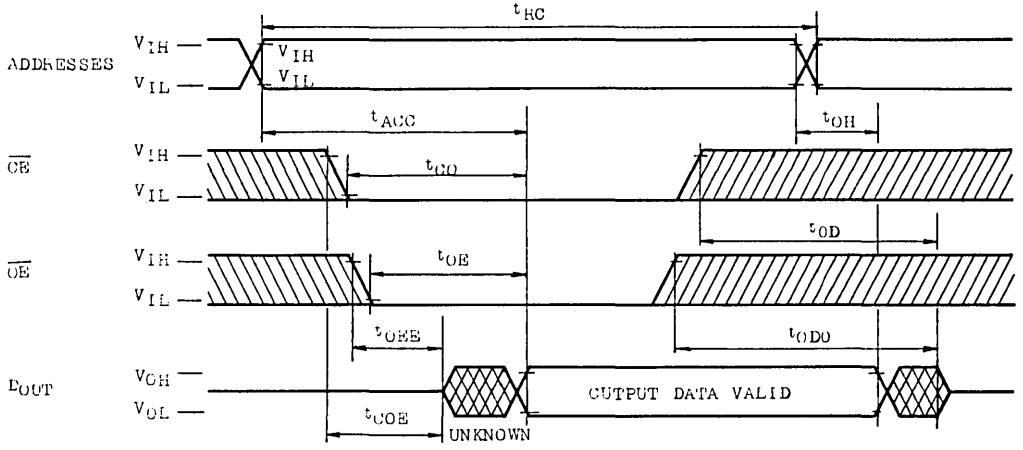
SYMBOL	PARAMETER	TEST CONDITION	TC55257AP-10/APL-10 AF-10/AFL-10		TC55257AP-12/APL-12 AF-12/AFL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	$V_{IN}=2.4V/0.6V$	100	-	120	-	ns
t_{WP}	Write Pulse Width	$V_{IH}=2.2V$	70	-	80	-	
t_{CW}	Chip Selection to End of Write	$V_{IL}=0.8V$	90	-	100	-	
t_{AS}	Address Set up Time	t_r, $t_f \leqq 5ns$	0	-	0	-	
t_{WR}	Write Recovery Time		10	-	10	-	
t_{ODW}	R/W to Output High-Z		-	50	-	60	
t_{OEW}	R/W to Output Low-Z		10	-	10	-	
t_{DS}	Data Set up Time		40	-	50	-	
t_{DH}	Data Hold Time		0	-	0	-	

Note: Input pulse levels=V_{IN}

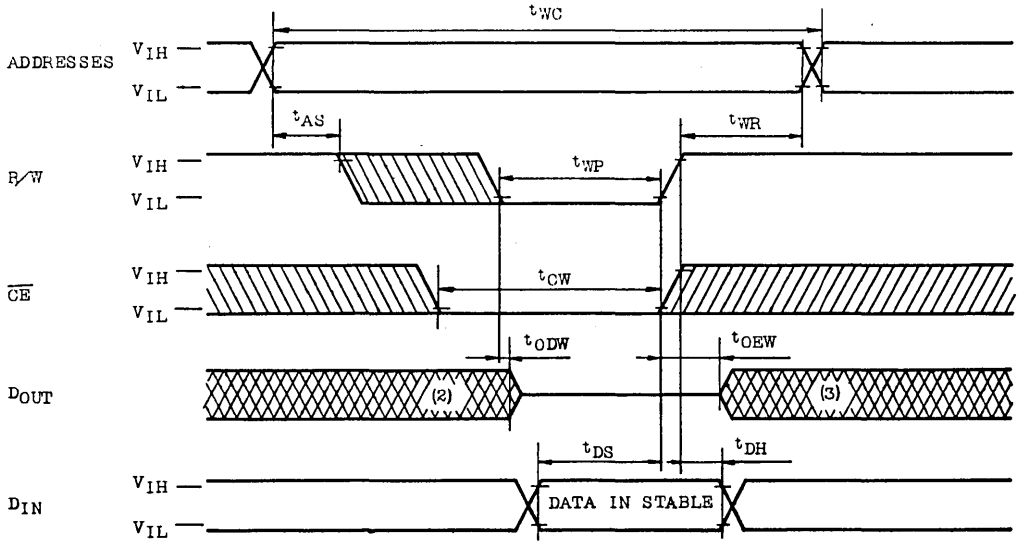
Timing Measurement Reference Levels=V_{IH}, V_{IL}

TIMING WAVEFORMS

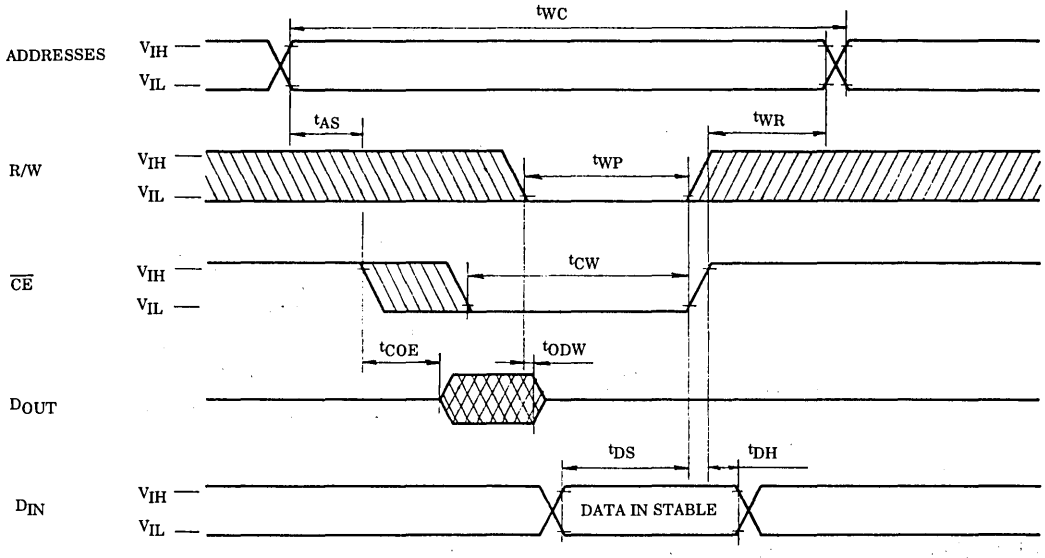
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



Note: 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

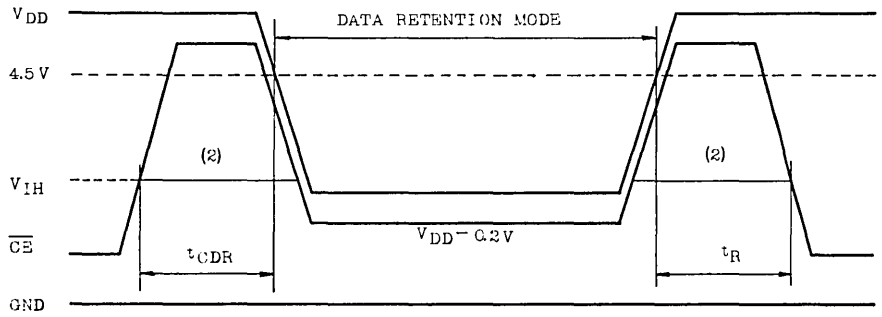
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage			2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	TC55257APL /AFL	V_{DD}=3.0V	-	-	50	µA
			V_{DD}=5.5V	-	-	100	
		TC55257AP/AF		-	-	1.0	mA
t_{CDR}	Chip Deselection to Data Retention Mode			0	-	-	µs
t_R	Recovery Time			t_{RC}(1)	-	-	

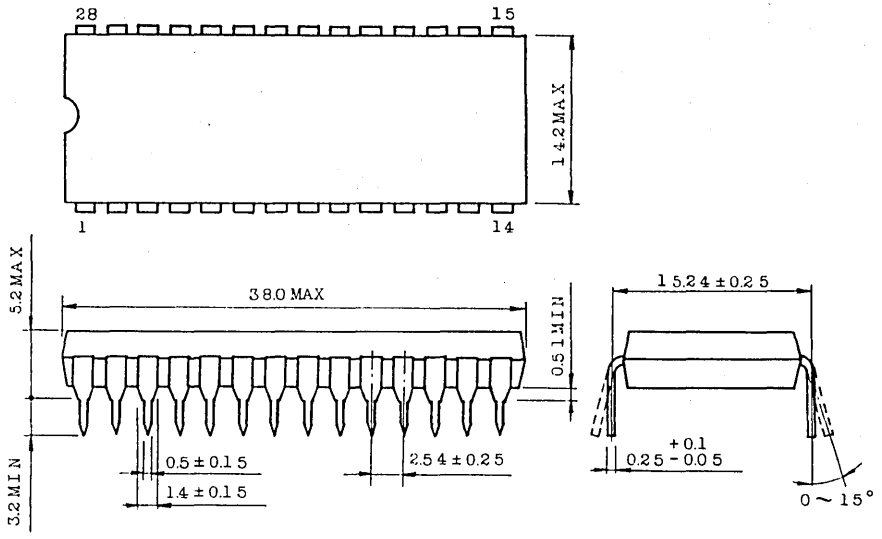
Note (1): Read Cycle Time

$\overline{CE}$ Controlled Data Retention Mode



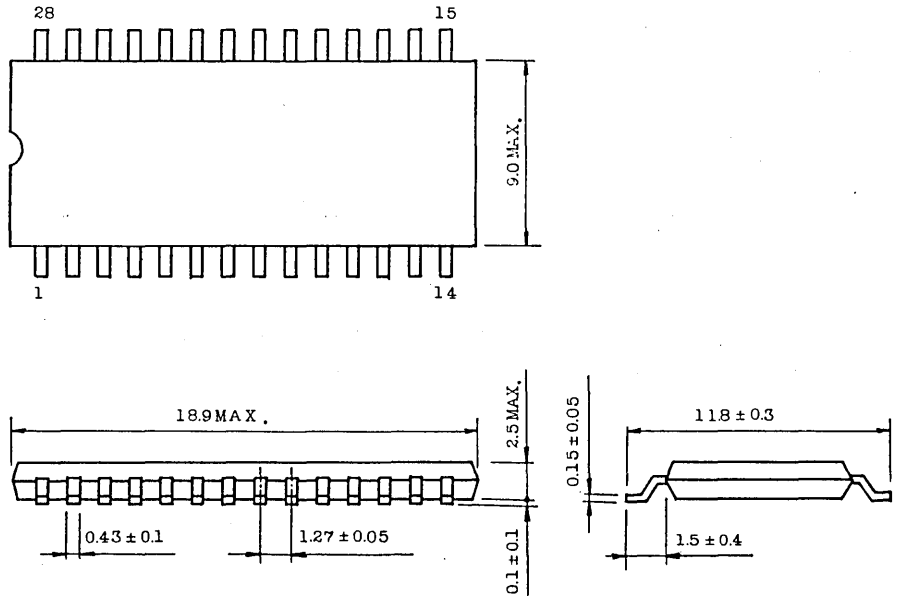
Note (2): If the V_{IH} of $\overline{CE}$ is 2.4V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

DIP 28 PIN OUTLINE DRAWING (6D28A-P) Unit in mm



Note: Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

MFP 28 PIN OUTLINE DRAWINGS (F28GA-P) Unit in mm



Note: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

32,768 WORD × 8 CMOS PSEUDO STATIC RAM
SILICON MONOLITHIC
SILICON GATE CMOS

TC51832P-85, TC51832P-10
TC51832P-12

DESCRIPTION

The TC51832P is a 256K bit high speed CMOS pseudo static RAM organized as 32,768 words by 8 bits. The TC51832P utilized one transistor dynamic memory cell with CMOS peripheral circuit to provide large capacity, high speed and low power features. System oriented features include single power supply of 5V±10% torelance. The $\overline{OE}/\overline{RFSH}$ input allows two types of refresh operation —— auto refresh and self refresh. The TC51832P also features static RAM like write function that the input data is written into the memory cell at the rising edge of R/W, thus being easy to interface with microprocessor. The TC51832P is a pin-compatible with 256K bit CMOS static RAM - TC55257P and is moulded a standard 0.6 inch width plastic DIP.

FEATURES

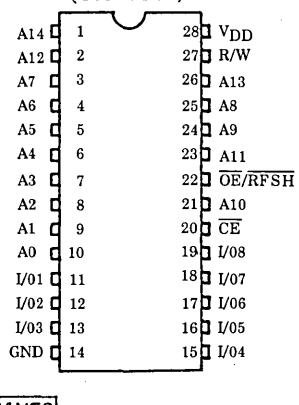
- Organization: 32,768 word × 8 bit
- Fast Access Time and Cycle Time

	TC51832P-85	TC51832P-10	TC51832P-12
t_{CEA} $\overline{CE}$ Access Time	85ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	135ns	160ns	190ns

- Single Power Supply: 5V±10%
- Static RAM like Write Function
- All inputs and outputs: TTL Compatible
- Low Power Dissipation
  - Operating : 303mW(TC51832P-85)
    248mW(TC51832P-10)
    220mW(TC51832P-12)
  - Standby : 5.5mW
  - Self Refresh: 5.5mW
- Two types of Refresh Operation Capability
  - Auto Refresh
  - Self Refresh
- Pin Compatible with 256K bit CMOS Static RAM TC55257P

PIN CONNECTION

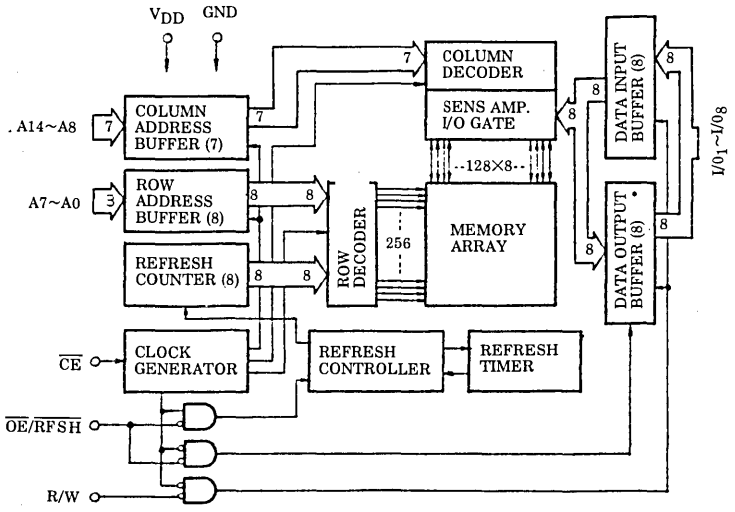
(TOP VIEW)



PIN NAMES

A0 ∿ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable/Refresh Input
$\overline{CE}$	Chip Enable Input
I/01 ∿ I/08	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTES
V_{IN}	Input Voltage	-1.0 ∿ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ∿ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ∿ 7.0	V	
T_{OPR}	Operating Temperature	0 ∿ 70	°C	
T_{STG}	Storage Temperature	-55 ∿ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	
V_{IL}	Input low Voltage	-1.0	-	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{DDO}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{CE}$, Address Cycleling: t_{RC}=t_{RC} MIN)	TC51832P-85	-	55	mA	3,4
		TC51832P-10	-	45		
		TC51832P-12	-	40		
I_{DDS1}	STANDBY CURRENT 1 Power Supply Standby Current, TTL Level Input ($\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{IH})		-	1	mA	
I_{DDF}	SELF REFRESH CURRENT Average Power Supply Self Refresh Current ($\overline{CE}$=V_{DD}-0.2V, $\overline{OE}$/$\overline{RFSH}$=0.2V)		-	1	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ V_{DD}, All Other Inputs not under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disable, 0V ≦ V_{OUT} ≦ V_{DD})		-10	10	uA	
V_{OH}	OUTPUT HIGH LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LOW LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD}=5V±10%, Ta=0 ~ 70°C) (Notes 5, 6, 7, 8, 9)

SYMBOL	PARAMETER	TC51832P-85		TC51832P-10		TC51832P-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	-	160	-	190	-	ns	
t_{RMW}	Read Write Cycle Time	200	-	240	-	280	-	ns	
t_{CE}	$\overline{CE}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{P}	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	$\overline{CE}$ Access Time	-	85	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	10	-	10	-	10	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	R/W to Output in Low-Z	0	-	0	-	0	-	ns	
t_{CHZ}	$\overline{CE}$ to Output in High-Z	0	20	0	30	0	30	ns	10
t_{OHZ}	$\overline{OE}$ to Output in High-Z	0	20	0	30	0	30	ns	10
t_{WHZ}	R/W to Output in High-Z	0	20	0	30	0	30	ns	10
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	-	70	-	85	-	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	-	70	-	85	-	ns	
t_{DSW}	Data Set-Up Time Referenced to R/W	35	-	40	-	50	-	ns	11
t_{DSC}	Data Set-Up Time Referenced to $\overline{CE}$	35	-	40	-	50	-	ns	11
t_{DHW}	Data Hold Time Referenced to R/W	0	-	0	-	0	-	ns	11
t_{DHC}	Data Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	11
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	12
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	12
t_{FC}	Auto Refresh Cycle Time	135	-	160	-	190	-	ns	
t_{RFD}	$\overline{CE}$ to $\overline{RFSH}$ Delay Time	40	-	50	-	60	-	ns	

(Continued)

SYMBOL	PARAMETER	TC51832P-85		TC51832P-10		TC51832P-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh Cycle)	80	8,000	80	8,000	80	8,000	ns	13
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	13
t_{FCE}	$\overline{RFSH}$ Active to $\overline{CE}$ Delay Time	160	-	190	-	225	-	ns	13
t_{FSR}	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Auto Refresh Cycle)	65	-	80	-	95	-	ns	13
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh Cycle)	8,000	-	8,000	-	8,000	-	ns	13
t_{FRS}	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Self Refresh Cycle)	160	-	190	-	225	-	ns	13
t_{FST}	$\overline{RFSH}$ Set-Up Time (Refresh Counter Test Cycle)	10	30	10	30	10	30	ns	
t_{FHT}	$\overline{RFSH}$ Hold Time (Refresh Counter Test Cycle)	65	8,000	65	8,000	65	8,000	ns	
t_{REF}	Refresh Period	-	4	-	4	-	4	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

CAPACITANCE (V_{DD}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0 ∿ A14)	-	5	pF
CI2	Input Capacitance ($\overline{CE}$, $\overline{OE}/\overline{RFSH}$, R/W)	-	7	pF
CIO	Input/Output Capacitance (I/O1 ∿ I/O8)	-	7	pF

NOTES:

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2) All voltages are reference to GND.

3) I_{DDO} depend on cycle rate.

4) I_{DDO} depend on output loading. Specified value are obtained with the output open.

5) An initial pause of 1ms with high $\overline{CE}$ and high $\overline{OE}/\overline{RFSH}$ is required after power-up before proper device operation is achieved.

6) AC measurements assume t_T=5ns.

7) V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) The $\overline{OE}/\overline{RFSH}$ input operates as the output enable input($\overline{OE}$) and refresh control input(RFSH) under the condition of that $\overline{CE}$=V_{IL} and $\overline{CE}$=V_{IH}, respectively.

10) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

11) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time(t_{DSW}, t_{DSC}) and hold time(t_{DHW}, t_{DHC}).

12) All address are latched at the falling edge of $\overline{CE}$. Therefore must be valid during t_{ASC} and t_{AHC}.

13) Two refresh operation - auto refresh and self refresh are determind by the $\overline{OE}/\overline{RFSH}$ pulse width under the condition of $\overline{CE}$=V_{IH}.

    Auto refresh: $\overline{OE}/\overline{RFSH}$ pulse width $\leqq t_{FAP}$(max.)

    Self refresh: $\overline{OE}/\overline{RFSH}$ pulse width $\geqq t_{FAS}$(min.)

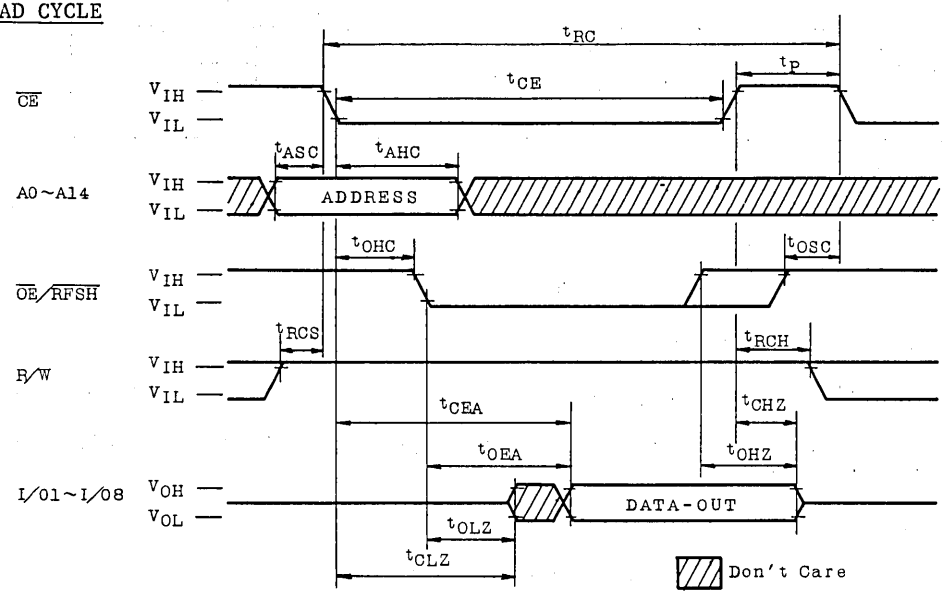
    The following timing parameter must be kept before device proper operation is achieved after refresh.

    Auto refresh: t_{FCE} and t_{FSR}

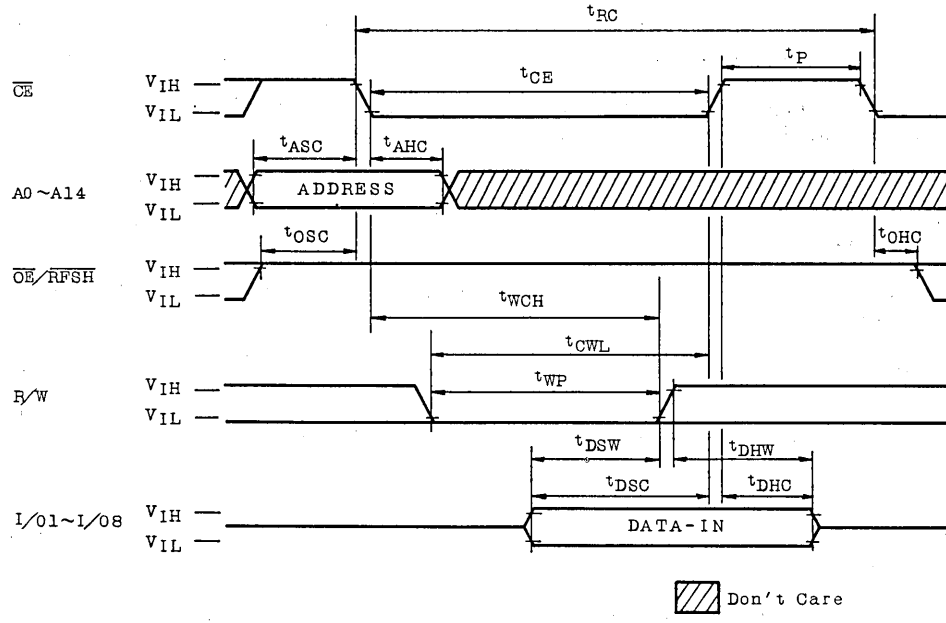
    Self refresh: t_{FRS}

TIMING CHART

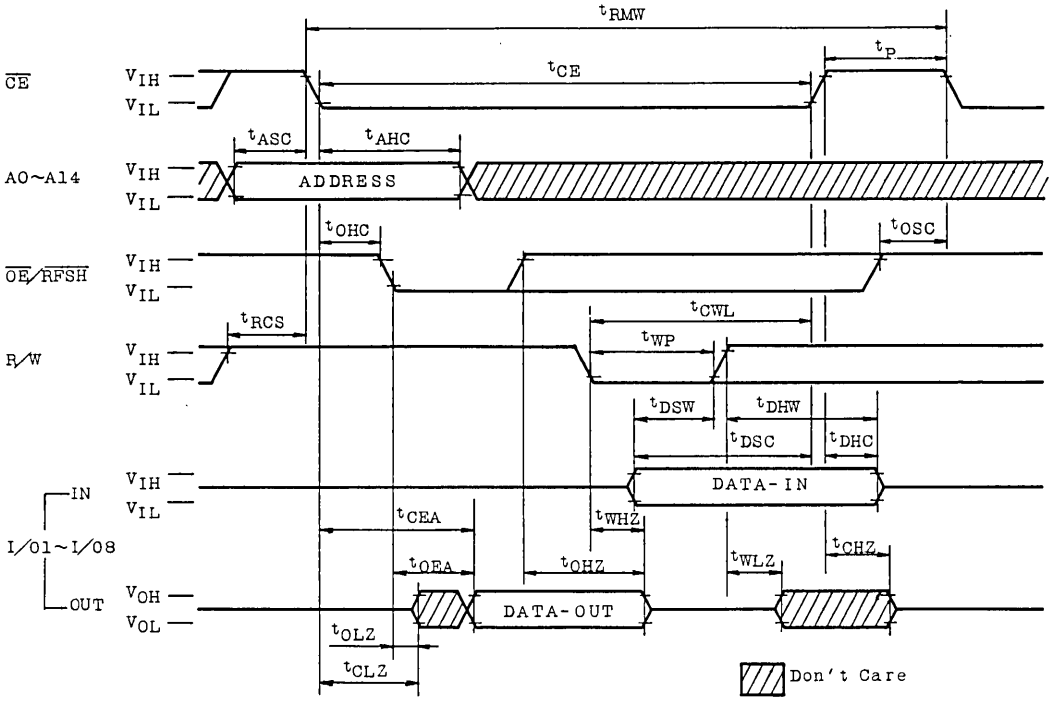
READ CYCLE



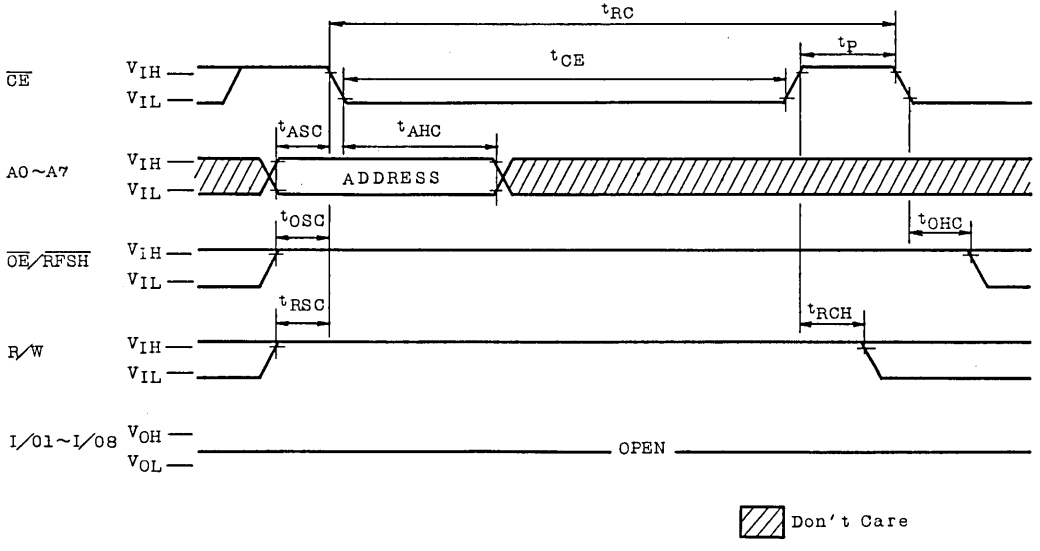
WRITE CYCLE



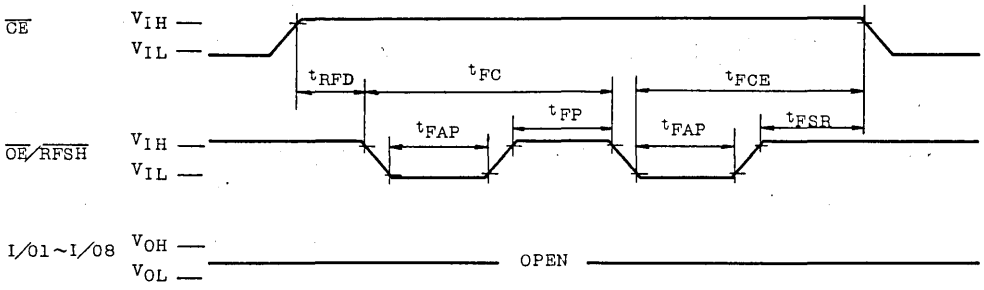
READ WRITE CYCLE



$\overline{CE}$ ONLY REFRESH CYCLE

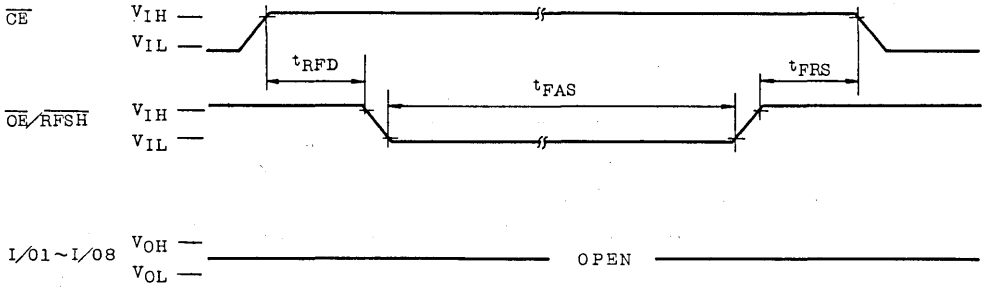


AUTO REFRESH CYCLE



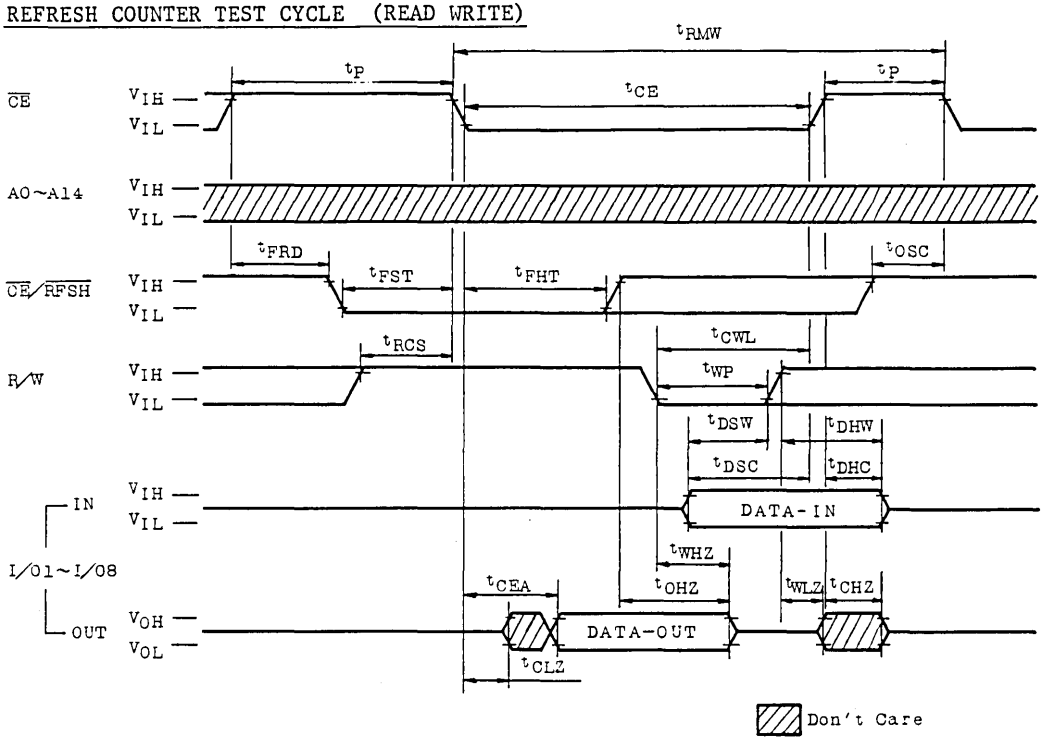
Note) A0~A14, R/$\overline{W}$ = Don't Care

SELF REFRESH CYCLE



Note) A0~A14, R/$\overline{W}$ = Don't Care

REFRESH COUNTER TEST CYCLE (READ WRITE)



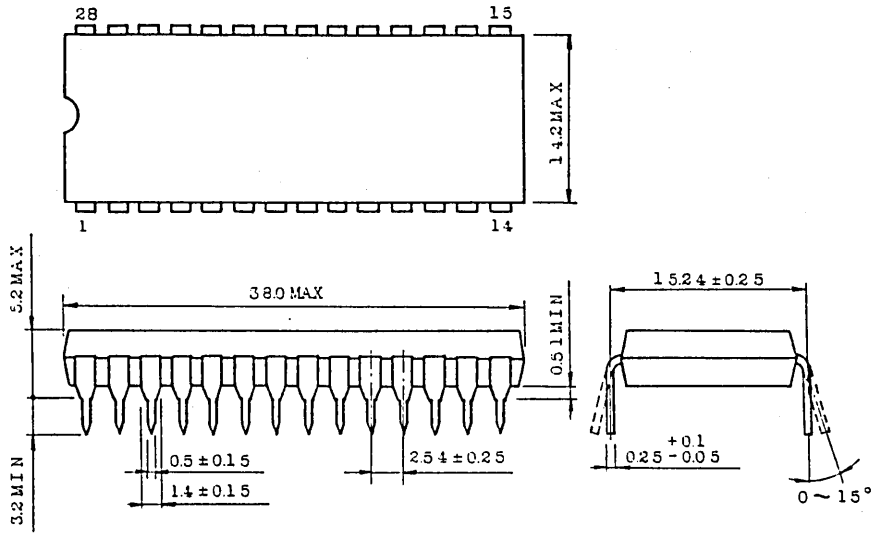
REFRESH COUNTER TEST

The internal refresh operation of TC51832P can be tested by REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and fixed zero as column address.
The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.
② Read "0" out and write "1" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.
③ Check "1" out of 256 bits at normal read mode, which was written at ②
④ Read "1" out and write "0" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④
⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS (6D28A-P)

Unit in mm



NOTES: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCT

32,768 WORD × 8 CMOS PSEUDO STATIC RAM
SILICON MONOLITHIC
SILICON GATE CMOS

TC51832PL-85, TC51832PL-10
TC51832PL-12

DESCRIPTION

The TC51832PL is a 256K bit high speed CMOS pseudo static RAM organized as 32,768 words by 8 bits. The TC51832PL utilized one transistor dynamic memory cell with CMOS peripheral circuit to provide large capacity, high speed and low power features. System oriented features include single power supply of 5V±10% torelance. The $\overline{OE}/\overline{RFSH}$ input allows two types of refresh operation — auto refresh and self refresh. The TC51832PL also features static RAM like write function that the input data iswritten into the memory cell at the rising edge of R/W, thus being easy to interface with microprocessor. The TC51832PL is a pin-compatible with 256K bit CMOS static RAM - TC55257P and is moulded a standard 0.6 inch width plastic DIP.

FEATURES

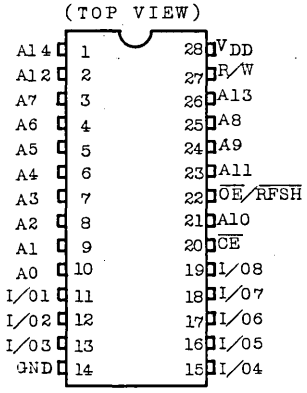
- Organization: 32,768 word 8 bit
- Fast Access Time and Cycle Time

	TC51832PL-85	TC51832PL-10	TC51832PL-12
t_{CEA} $\overline{CE}$ Access Time	85ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	135ns	160ns	190ns

- Single Power Supply: 5V±10%
- Static RAM like Write Function
- All inputs and outputs: TTL Compatible
- Low Power Dissipation
  - Operating : 303mW(TC51832PL-85)
    248mW(TC51832PL-10)
    220mW(TC51832PL-12)
  - Standby : 1.1mW
  - Self Refresh: 1.1mW
- Two types of Refresh Operation Capability
  - Auto Refresh
  - Self Refresh
- Pin compatible with 256K bit CMOS Static TAM TC55257P

PIN CONNECTION

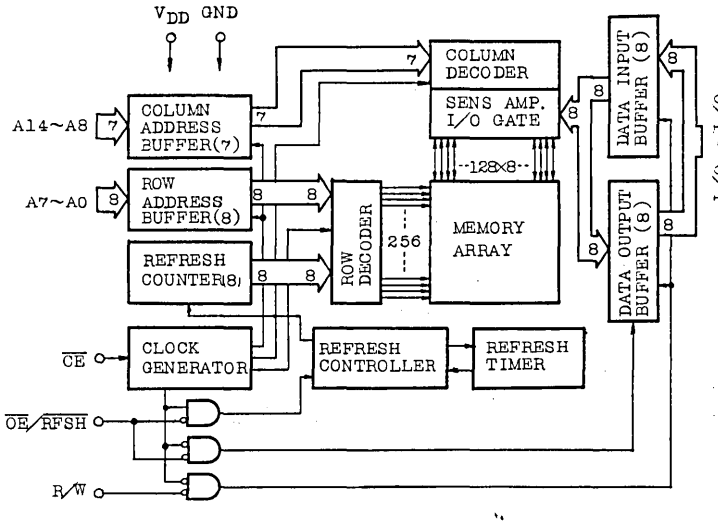
(TOP VIEW)



PIN NAMES

A0 ∿ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable/Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1 ∿ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTES
V_{IN}	Input Voltage	-1.0 ∿ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ∿ 7.0	V	1
V_{DD}	Power Supply Voltage	-1.0 ∿ 7.0	V	1
T_{OPR}	Operating Temperature	0 ∿ 70	°C	1
T_{STG}	Storage Temperature	-55 ∿ 150	°C	1
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec	1
P_D	Power Dissipation	600	mW	1
I_{OUR}	Short Circuit Output Current	50	mA	1

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{DD}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{DDO}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{CE}$, Address Cycling: t_{RC}=t_{RC} MIN)	TC51832PL-85	-	55	mA	3, 4
		TC51832PL-10	-	45		
		TC51832PL-12	-	40		
I_{DDS1}	STANDBY CURRENT 1 Power Supply Standby Current, TTL Level Input ($\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{IH})		-	1	mA	
I_{DDS2}	STANDBY CURRENT 2 Power Supply Standby Current, CMOS Level Input ($\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{DD}-0.2V)		-	0.2	mA	
I_{DDF}	SELF REFRESH CURRENT Average Power Supply Self Refresh Current ($\overline{CE}$=V_{DD}-0.2V, $\overline{OE}$/$\overline{RFSH}$=0.2V)		-	0.2	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ V_{DD}, All Other Inputs not under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disable, 0V ≦ V_{OUT} ≦ V_{DD})		-10	10	μA	
V_{OH}	OUTPUT HIGH LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LOW LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7, 8, 9)

SYMBOL	PARAMETER	TC51832PL-85		TC51832PL-10		TC51832PL-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	-	160	-	190	-	ns	
t_{RMW}	Read Write Cycle Time	200	-	240	-	280	-	ns	
t_{CE}	$\overline{CE}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{P}	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	$\overline{CE}$ Access Time	-	85	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	10	-	10	-	10	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	R/W to Output in Low-Z	0	-	0	-	0	-	ns	
t_{CHZ}	$\overline{CE}$ to Output in High-Z	0	20	0	30	0	30	ns	10
t_{OHZ}	$\overline{OE}$ to Output in High-Z	0	20	0	30	0	30	ns	10
t_{WHZ}	R/W to Output in High-Z	0	20	0	30	0	30	ns	10
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	-	70	-	85	-	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	-	70	-	85	-	ns	
t_{DSW}	Data Set-Up Time Referenced to R/W	35	-	40	-	50	-	ns	11
t_{DSC}	Data Set-Up Time Referenced to $\overline{CE}$	35	-	40	-	50	-	ns	11
t_{DHW}	Data Hold Time Referenced to R/W	0	-	0	-	0	-	ns	11
t_{DHC}	Data Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	11
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	12
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	12
t_{FC}	Auto Refresh Cycle Time	135	-	160	-	190	-	ns	
t_{RFD}	$\overline{CE}$ to $\overline{RFSH}$ Delay Time	40	-	50	-	60	-	ns	

(Continued)

SYMBOL	PARAMETER	TC51832PL-85		TC51832PL-10		TC51832PL-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh Cycle)	80	8,000	80	8,000	80	8,000	ns	13
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	13
t_{FCE}	$\overline{RFSH}$ Active to $\overline{CE}$ Delay Time	160	-	190	-	225	-	ns	13
t_{FSR}	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time(Auto Refresh Cycle)	65	-	80	-	95	-	ns	13
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh Cycle)	8,000	-	8,000	-	8,000	-	ns	13
t_{FRS}	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Self Refresh Cycle)	160	-	190	-	225	-	ns	13
t_{FST}	$\overline{RFSH}$ Set-Up Time (Refresh Counter Test Cycle)	10	30	10	30	10	30	ns	
t_{FHT}	$\overline{RFSH}$ Hold Time (Refresh Counter Test Cycle)	65	8,000	65	8,000	65	8,000	ns	
t_{REF}	Refresh Period	-	4	-	4	-	4	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

CAPACITANCE (V_{DD}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0 ∿ A14)	-	5	pF
CI2	Input Capacitance ($\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$, R/W)	-	7	pF
CIO	Input/Output Capacitance (I/O1 ∿ I/O8)	-	7	pF

NOTES:

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2) All voltages are reference to GND.

3) I_{DDO} depend on cycle rate.

4) I_{DDO} depend on output loading. Specified value are obtained with the output open.

5) An initial pause of 1ms with high $\overline{CE}$ and high $\overline{OE}/\overline{RESH}$ is required after power-up before proper device operation is achieved.

6) AC measurements assume t_T=5ns.

7) V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) The $\overline{OE}/\overline{RFSH}$ input operates as the output enable input($\overline{OE}$) and refresh control input(RFSH) under the condition of that $\overline{CE}$=V_{IL} and $\overline{CE}$=V_{IH}, respectively.

10) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

11) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW}, t_{DSC}) and hold time (t_{DHW}, t_{DHC}).

12) All address are latched at the falling edge of $\overline{CE}$. Therefore must be valid during t_{ASC} and t_{AHC}.

13) Two refresh operation - auto refresh and self refresh are determind by the $\overline{OE}/\overline{RFSH}$ pulse width under the condition of $\overline{CE}$=V_{IH}.

    Auto refresh: $\overline{OE}/\overline{RFSH}$ pulse width $\leqq t_{FAP}$(max.)

    Self refresh: $\overline{OE}/\overline{RFSH}$ pulse width $\geqq t_{FAS}$(min.)

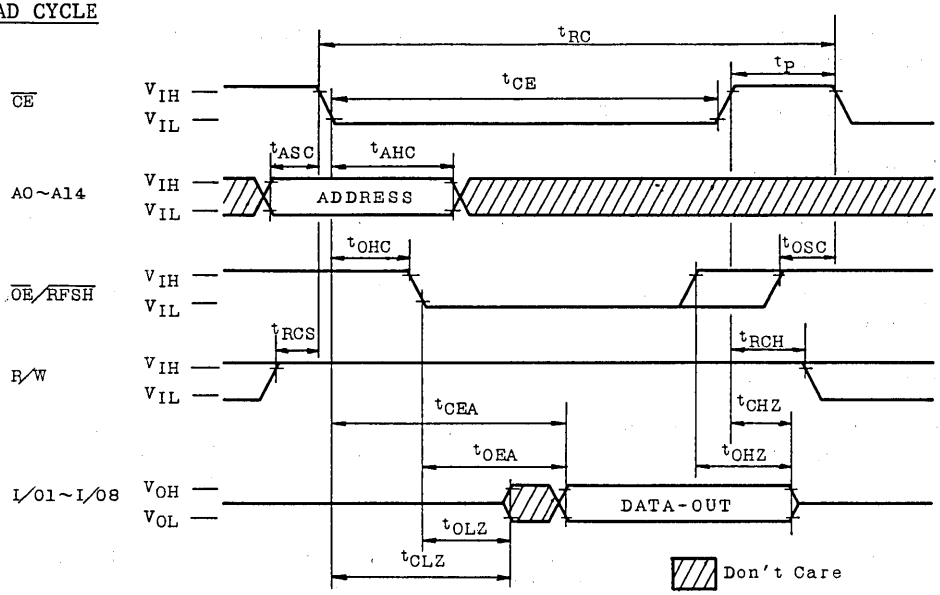
    The following timing parameter must be kept before device proper operatio is achieved after refresh.

    Auto refresh: t_{FCE} and t_{FSR}

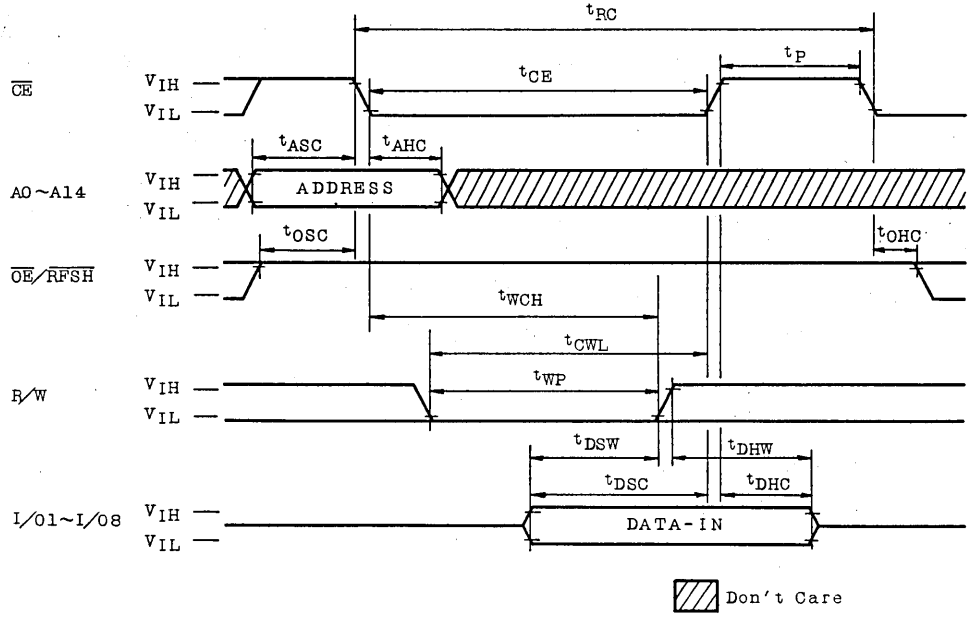
    Self refresh: t_{FRS}

TIMING CHART

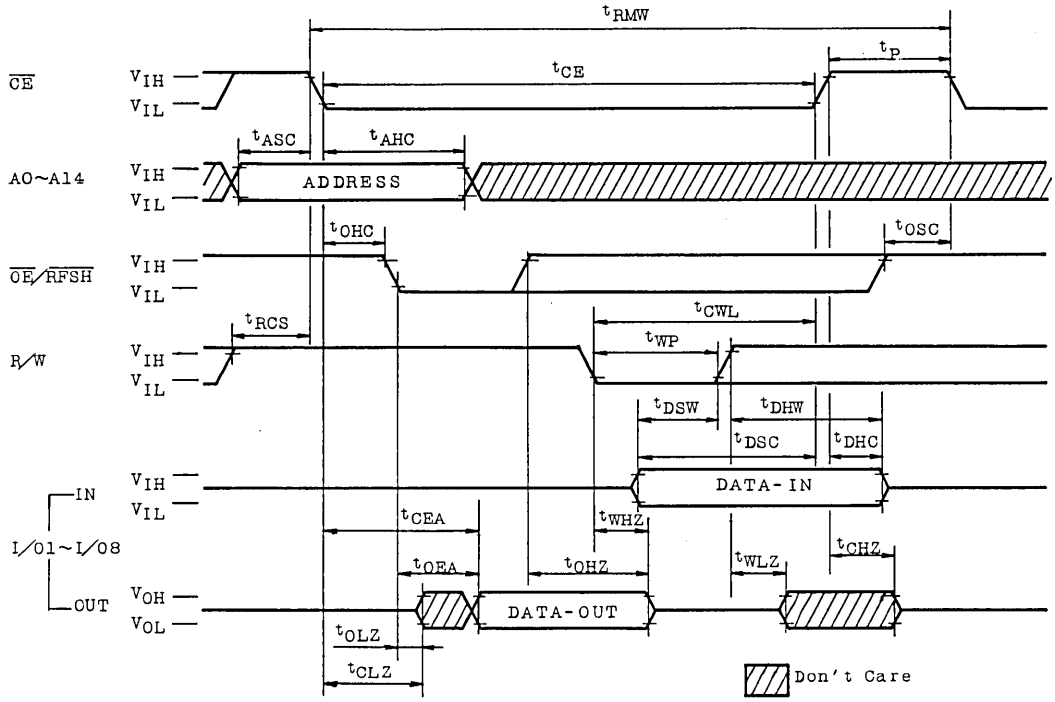
READ CYCLE



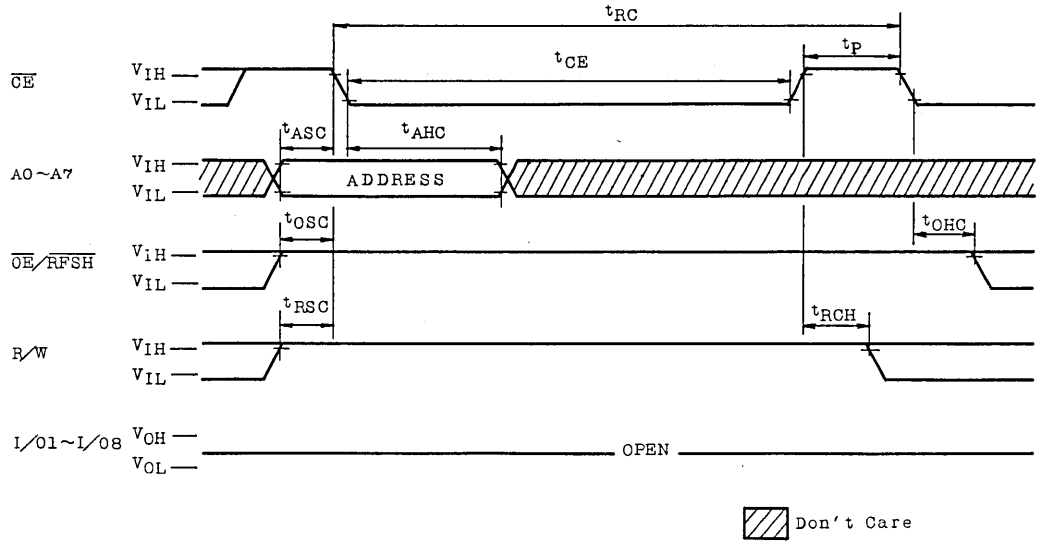
WRITE CYCLE



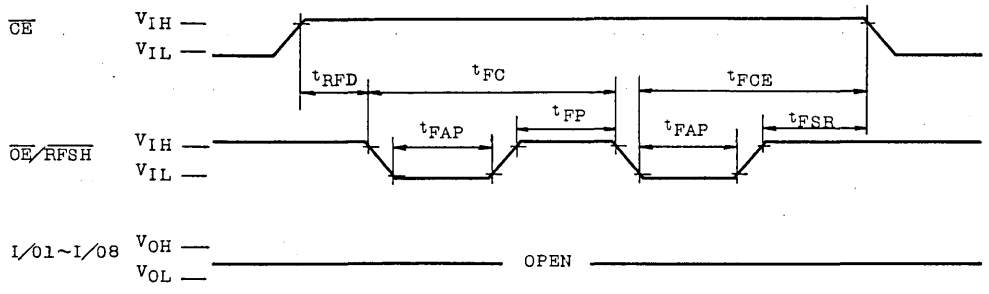
READ WRITE CYCLE



$\overline{CE}$ ONLY REFRESH CYCLE

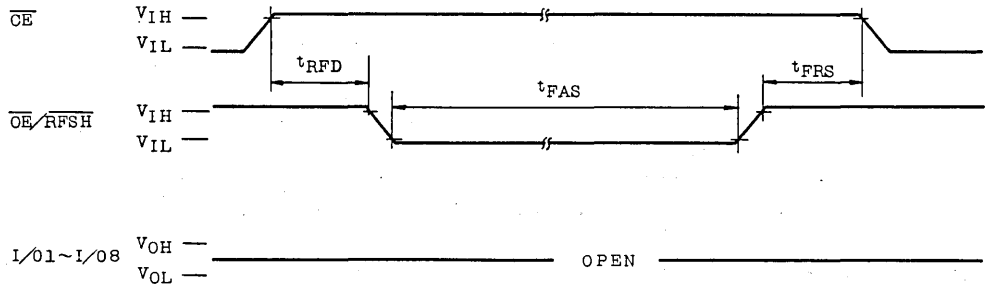


AUTO REFRESH CYCLE



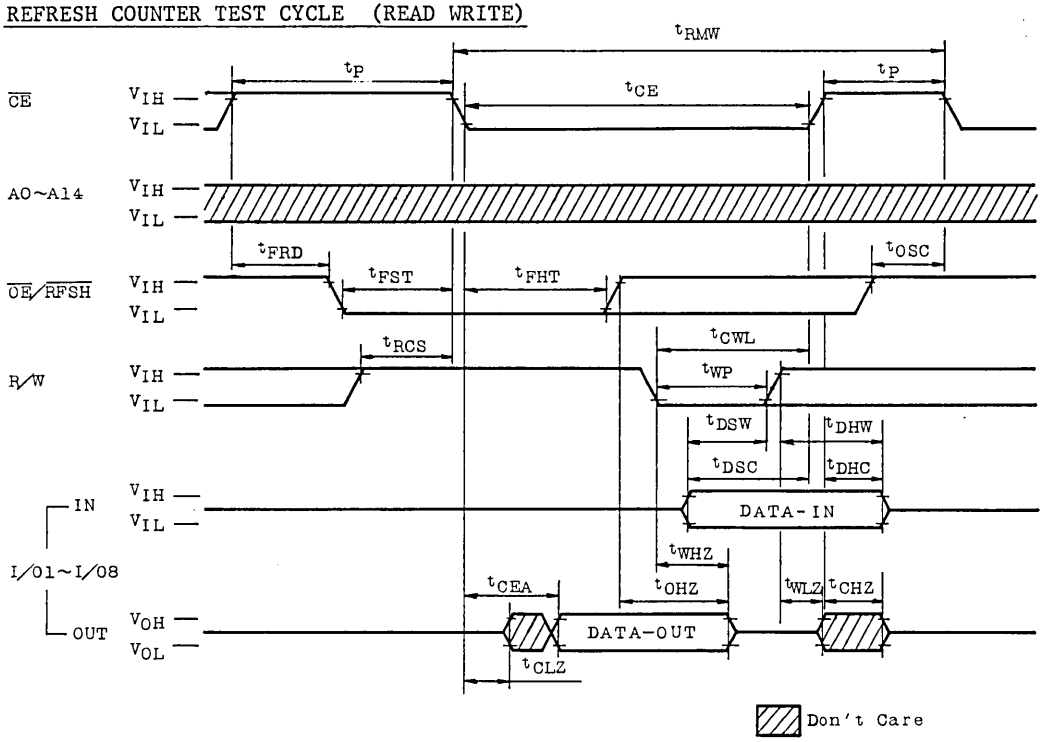
Note) A0~A14, R/$\overline{W}$=Don't Care

SELF REFRESH CYCLE



Note) A0~A14, R/$\overline{W}$=Don't Care

REFRESH COUNTER TEST CYCLE (READ WRITE)



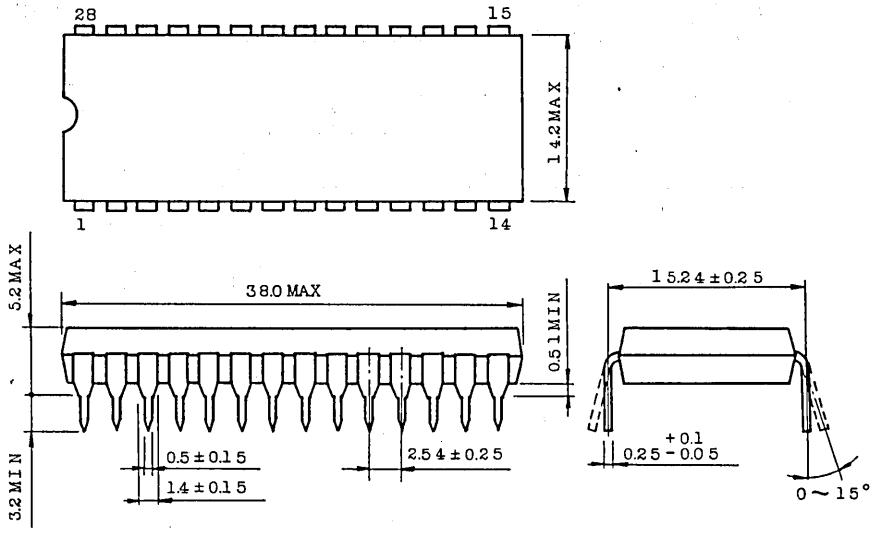
REFRESH COUNTER TEST

The internal refresh operation of TC51832PL can be tested by REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and fixed zero as column address.
The test procedure is as follows.

① Write "0" into all the memory cells at normal wirte mode.
② Read "0" out and write "1" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.
③ Check "1" out of 256 bits at normal read mode, which was written at ②.
④ Read "1" out and write "0" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS (6D28A-P)

Unit in mm



NOTES: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads. All dimensions are in millimeters.

High Speed Static RAMs

TOSHIBA MOS MEMORY PRODUCT

2,048 WORD × 8 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2018AD-25, TMM2018AD-35
TMM2018AD-45

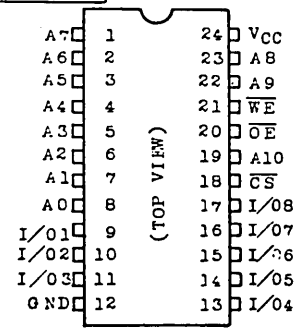
DESCRIPTION

The TMM2018AD is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 150mA/135mA/135mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.
Thus the TMM2018AD is most suitable for use in cache memory and high speed storage.
The TMM2018AD is offered in a 24 pin standard cerdip package with 0.3 inch width for high density assembly.
The TMM2018AD is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time
  - t_{ACC}=25ns: TMM2018AD-25
  - t_{ACC}=35ns: TMM2018AD-35
  - t_{ACC}=45ns: TMM2018AD-45
- Low power dissipation
  - I_{CC}=150mA: TMM2018AD-25
  - I_{CC}=135mA: TMM2018AD-35
  - I_{CC}=135mA: TMM2018AD-45
  - I_{SB}=20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs Directly TTL Compatible
- Power down feature: $\overline{CS}$=V_{IH}
- Output buffer control: $\overline{OE}$
- Three state outputs
- Inputs protected: All inputs protection against static charge.
- Package: 24 pins standard cerdip package, 0.3 inch width

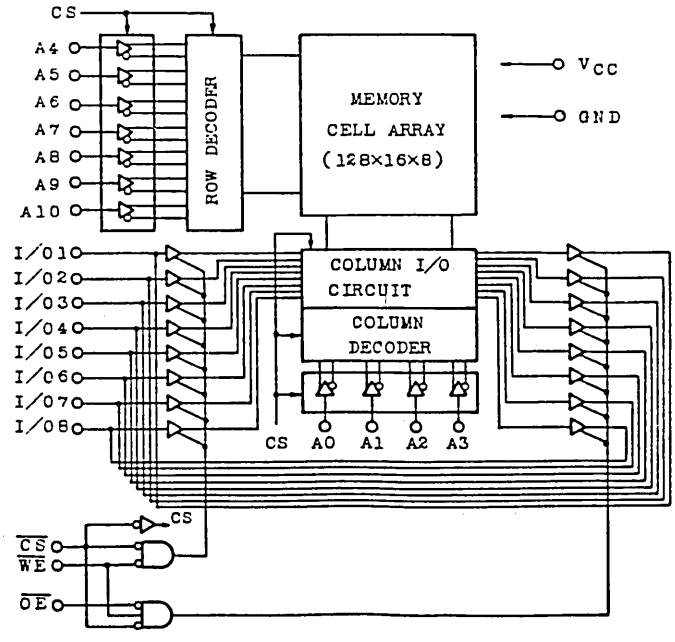
PIN CONNECTION



PIN NAMES

A_0-A_{10}	Address Inputs
I/O_1-I/O_8	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5-7.0	V
V_{IN}	Input Voltage	-3.5-7.0	V
$V_{I/O}$	Input/Output Voltage	-3.5-7.0	V
T_{opr}	Operating Temperature	0-70	°C
T_{stg}	Storage Temperature	-55-150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation	0.9	W
I_{OUT}	D.C. Output Current	20	mA

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V(MIN.)

D.C. CHARACTERISTICS (Ta=0-70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{IL}	Input Current	V_{IN}=0-V_{CC}		-	±1.0	μA
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4	-	V
V_{OL}	Output Low Voltage	I_{OL}=8.0mA		-	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0-V_{CC}, $\overline{CS}$=V_{IH}		-	±1.0	μA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}	-25	-	150	mA
			-35	-	135	
			-45	-	135	
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}		-	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, V_{CC}=0-5.5V		-	40	mA

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0-70°C, V_{CC}=5V±10%)

READ CYCLE

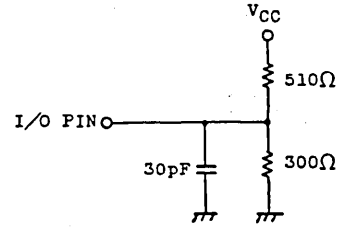
SYMBOL	PARAMETER	TMM2018AD-25		TMM2018AD-35		TMM2018AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	45	-	ns
t_{ACC}	Address Access Time	-	25	-	35	-	45	
t_{CO}	Chip Select Access Time	-	25	-	35	-	45	
t_{OE}	Output Enable to Output Valid	-	15	-	20	-	20	
t_{CLZ}	Chip Selection to Output in Low-Z	0	-	0	-	0	-	
t_{CHZ}	Chip Deselection to Output in High-Z	-	15	-	20	-	20	
t_{OLZ}	Output Enable to Output in Low-Z	0	-	0	-	0	-	
t_{OHZ}	Output Disable to Output in High-Z	-	12	-	15	-	15	
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	20	-	30	-	30	

WRITE CYCLE

SYMBOL	PARAMETER	TMM2018AD-25		TMM2018AD-35		TMM2018AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	45	-	ns
t_{CW}	Chip Selection to End of Write	20	-	30	-	40	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	20	-	30	-	35	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	-	12	-	15	-	15	
t_{DS}	Data Set Up Time	12	-	15	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

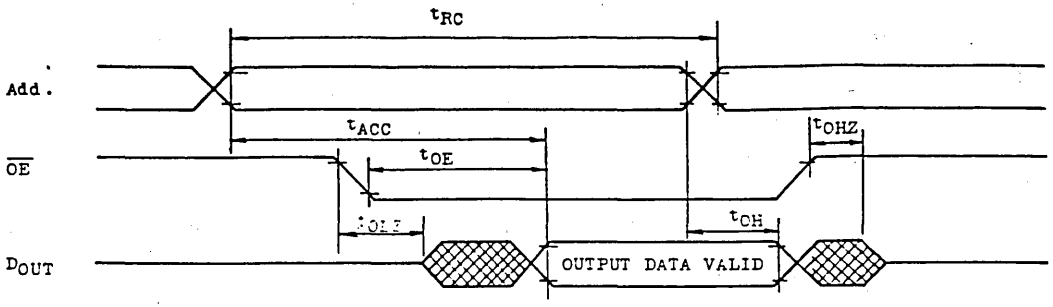
A.C. TEST CONDITONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

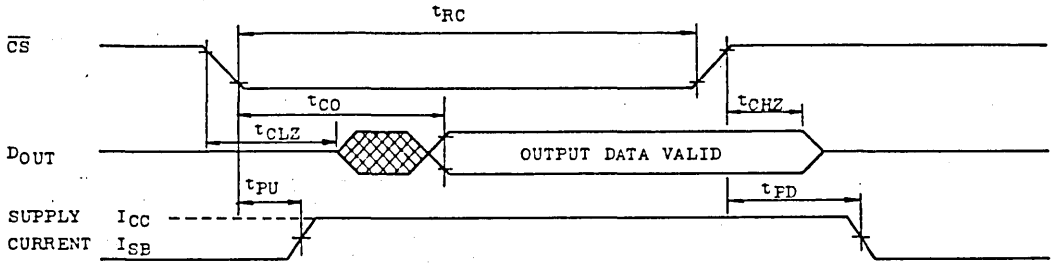


TIMING WAVEFORMS

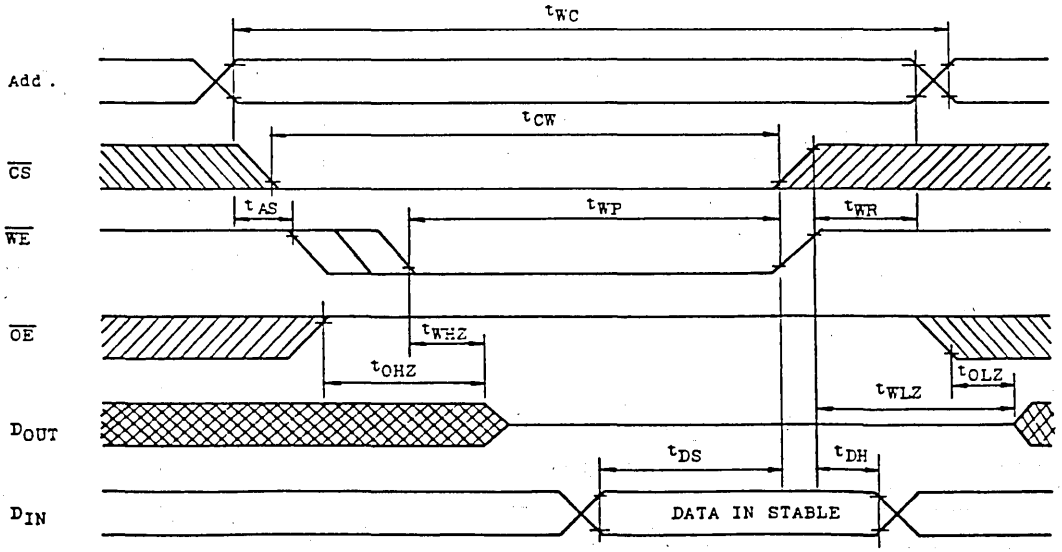
READ CYCLE 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})



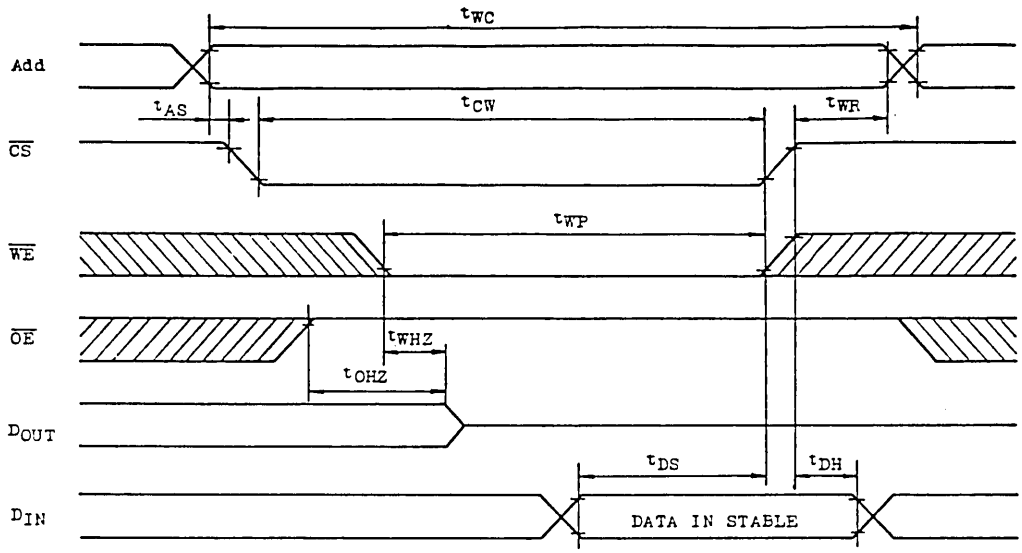
READ CYCLE 2. ($\overline{WE}$=V_{IH}, $\overline{OE}$=V_{IL})



WRITE CYCLE 1.



WRITE CYCLE 2.



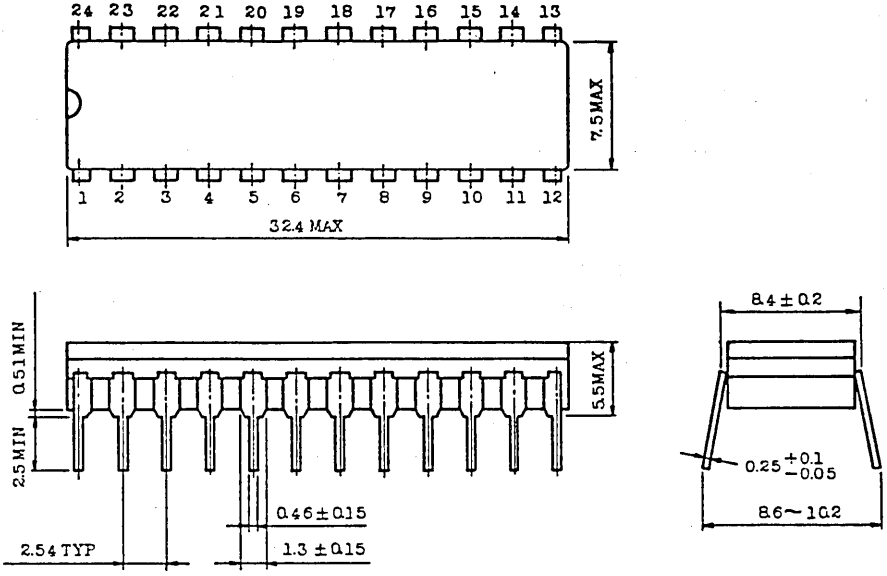
Note:

1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.

2. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.

TOSHIBA MOS MEMORY PRODUCT

2,048 WORD × 8 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2018AP-25, TMM2018AP-35
TMM2018AP-45

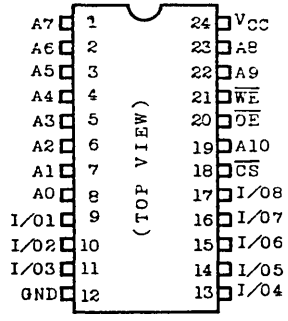
DESCRIPTION

The TMM2018AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply.
Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 150mA/135mA/135mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.
Thus the TMM2018AP is most suitable for use in cache memory and high speed storage.
The TMM2018AP is offered in a 24 pin standard plastic package with 0.3 inch width for high density assembly.
The TMM2018AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time
  - t_{ACC}=25ns: TMM2018AP-25
  - t_{ACC}=35ns: TMM2018AP-35
  - t_{ACC}=45ns: TMM2018AP-45
- Low power dissipation
  - I_{CC}=150mA: TMM2018AP-25
  - I_{CC}=135mA: TMM2018AP-35
  - ICC=135mA: TMM2018AP-45
  - I_{SB}=20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs: Directly TTL compatible
- Power down feature: $\overline{CS}$=V_{IH}
- Output buffer control: $\overline{OE}$
- Three state outputs
- Inputs protected: All inputs protection against static charge.
- Package: 24 pin standard plastic package, 0.3 inch width.

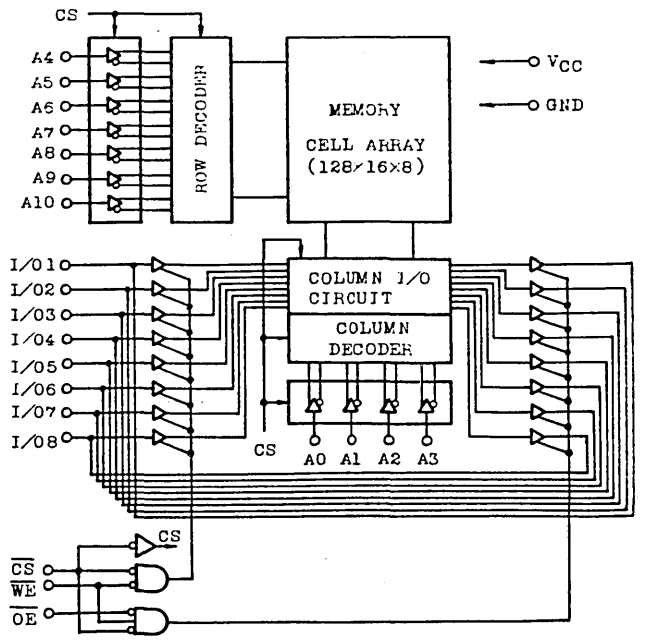
PIN CONNECTION



PIN NAMES

A0 ∿ A10	Address Inputs
I/01 ∿ I/08	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5 ∿ 7.0	V
V_{IN}	Input Voltage	-3.5 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-3.5 ∿ 7.0	V
T_{opr}	Operating Temperature	0 ∿ 70	°C
T_{stg}	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature • Time	260 • 10	°C•sec
P_D	Power Dissipation	0.9	W
I_{OUT}	D.C. Output Current	20	mA

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	

* Pulse Width: 10ns, DC: -0.5V (MIN.)

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{IL}	Input Current	V_{IN}=0 ∿ V_{CC}		-	±1.0	μA
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4	-	V
V_{OL}	Output Low Voltage	I_{OL}=8.0mA		-	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0 ∿ V_{CC}, $\overline{CS}$=V_{IH}		-	±1.0	μA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}	-25	-	150	mA
			-35	-	135	
			-45	-	135	
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}		-	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, V_{CC}=0 ∿ 5.5V		-	40	

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{CC}=5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TMM2018AP-25		TMM2018AP-35		TMM2018AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	45	-	ns
t_{ACC}	Address Access Time	-	25	-	35	-	45	
t_{CO}	Chip Select Access Time	-	25	-	35	-	45	
t_{OE}	Output Enable to Output Valid	-	15	-	20	-	20	
t_{CLZ}	Chip Selection to Output in Low-Z	0	-	0	-	0	-	
t_{CHZ}	Chip Deselection to Output in High-Z	-	15	-	20	-	20	
t_{OLZ}	Output Enable to Output in Low-Z	0	-	0	-	0	-	
t_{OHZ}	Output Disable to Output in High-Z	-	12	-	15	-	15	
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	20	-	30	-	30	

Write Cycle

SYMBOL	PARAMETER	TMM2018AP-25		TMM2018AP-35		TMM2018AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	45	-	ns
t_{CW}	Chip Selection to End of Write	20	-	30	-	40	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	20	-	30	-	35	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	-	12	-	15	-	15	
t_{DS}	Data Set Up Time	12	-	15	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

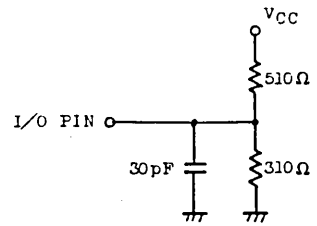
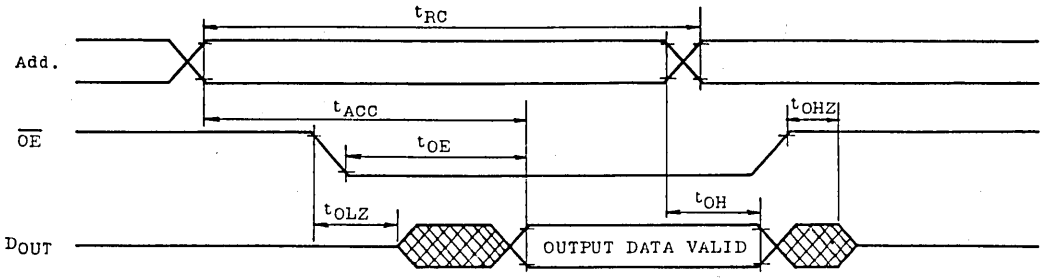


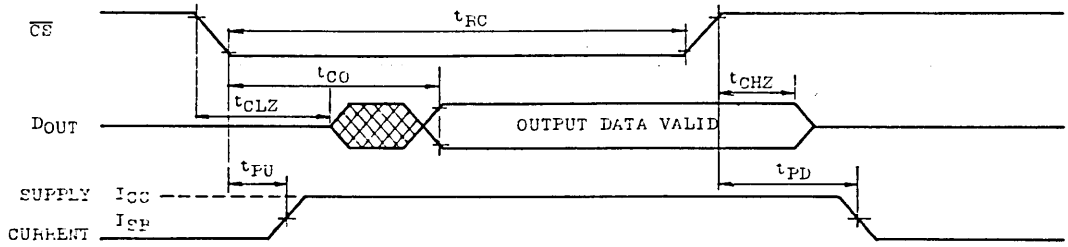
Fig.1 OUTPUT LOAD

TIMING WAVEFORMS

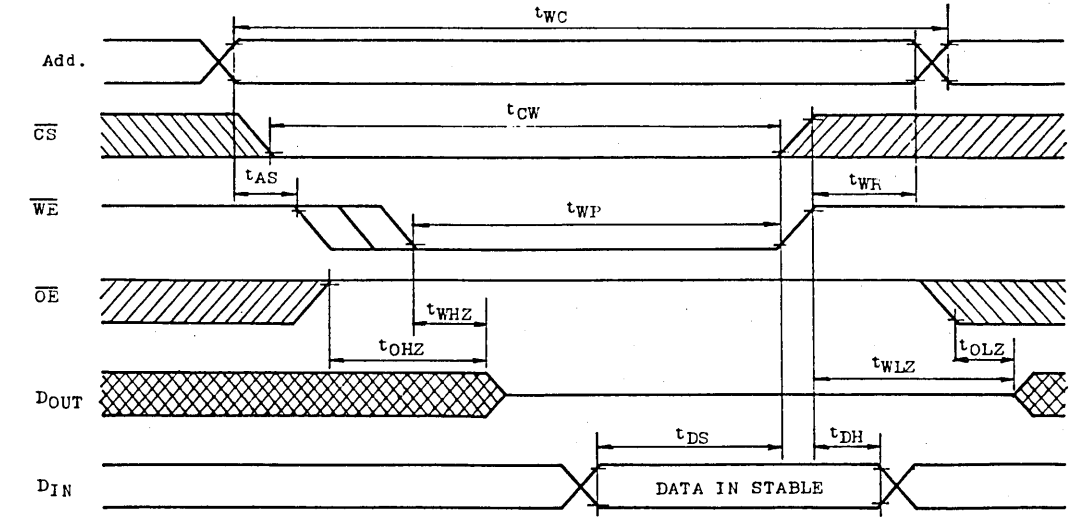
READ CYCLE 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})



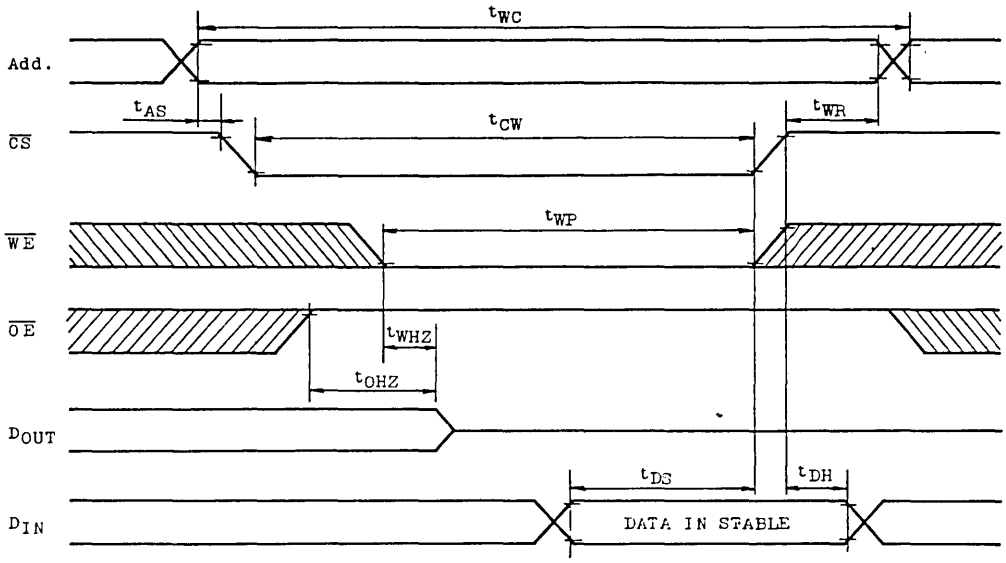
READ CYCLE 2. ($\overline{WE}$=V_{IH}, $\overline{OE}$=V_{IL})



WRITE CYCLE 1.



WRITE CYCLE 2.

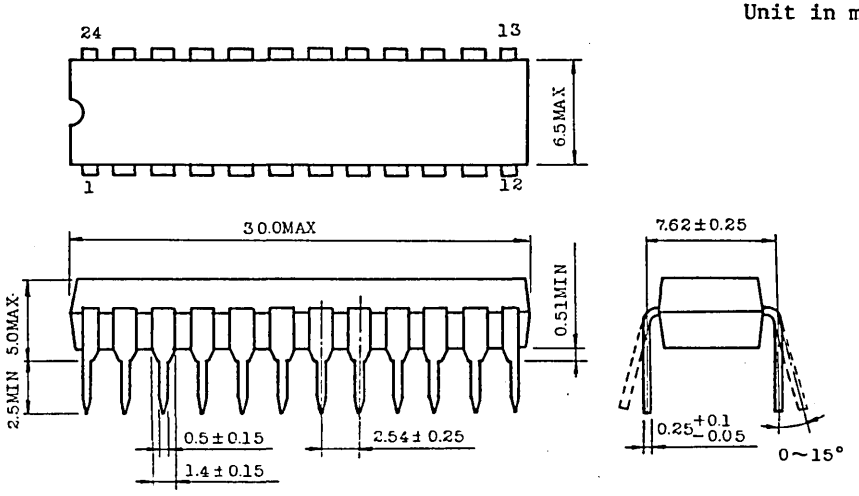


Note: 1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.

2. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.

TOSHIBA MOS MEMORY PRODUCT

4,096 WORD × 4 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2068AD-25, TMM2068AD-35
TMM2068AD-45

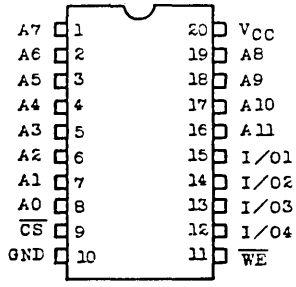
DESCRIPTION

The TMM2068AD is a 16,384 bits high speed and low power static random access memory organized as 4,096 words by 4 bits and operates from a single 5V supply.
Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 135/120/120mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.
Thus the TMM2068AD is most suitable for us in cache memory and high speed storage
The TMM2068AD is offered in a 20 pin standard cerdip package with 0.3 inch width for high density assembly.
The TMM2068AD is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

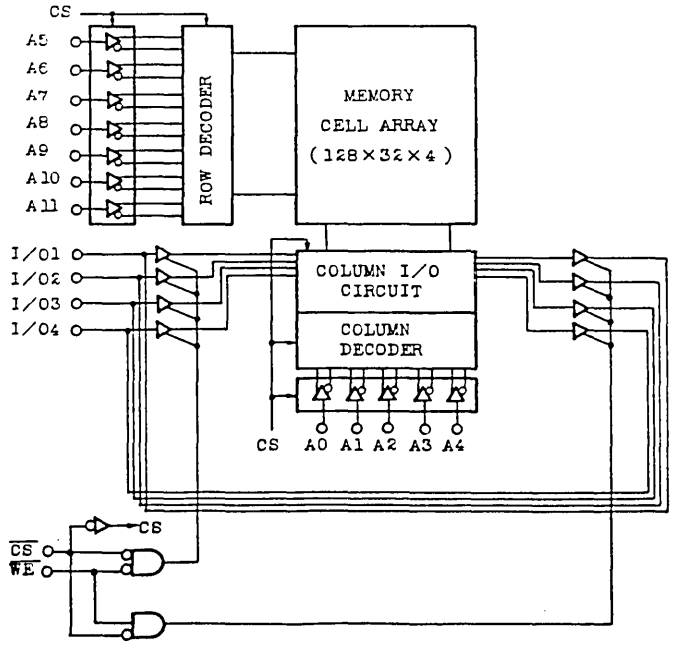
- Fast access time
  - t_{ACC}=25ns: TMM2068AD-25
  - t_{ACC}=35ns: TMM2068AD-35
  - t_{ACC}=45ns: TMM2068AD-45
- Low power dissipation
  - I_{CC}=135mA: TMM2068AD-25
  - I_{CC}=120mA: TMM2068AD-35
  - I_{CC}=120mA: TMM2068AD-45
  - I_{SB}=20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs: Directly TTL compatible
- Power down feature : $\overline{CS}$=V_{IH}
- Three state outputs
- Inputs protected: All inputs protection against static charge.
- Package: 20 pins standard cerdip package, 0.3 inch width.

PIN CONNECTION



(TOP VIEW)

BLOCK DIAGRAM



PIN NAMES

A0~A11	Address Inputs
I/O_1~I/O_4	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5~7.0	V
V_{IN}	Input Voltage	-3.5~7.0	V
$V_{I/O}$	Input/Output Voltage	-3.5~7.0	V
T_{opr}	Operating Temperature	0~70	°C
T_{stg}	Storage Temperature	-55~150	°C
T_{solder}	Soldering Temperature·Time	260·10	°C·sec
P_D	Power Dissipation	1.0	W
I_{OUT}	D.C. Output Current	20	mA

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V (Min.)

D.C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{IL}	Input Current	V_{IN}=0~V_{CC}		-	±1.0	μA
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4	-	V
V_{OL}	Output Low Voltage	I_{OL}=8.0mA		-	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0~V_{CC}, $\overline{CS}$=V_{IH}		-	±1.0	μA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}	-25	-	135	mA
			-35	-	120	
			-45	-	120	
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}		-	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, V_{CC}=0~5.5V		-	40	mA

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	8	

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

Read Cycle

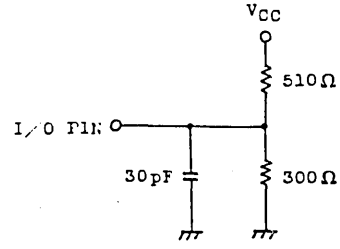
SYMBOL	PARAMETER	TMM2068AD-25		TMM2068AD-35		TMM2068AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	45	-	ns
t_{ACC}	Address Access Time	-	25	-	35	-	45	
t_{CO}	Chip Select Access Time	-	25	-	35	-	45	
t_{CLZ}	Chip Selection to Output in Low-Z	5	-	5	-	5	-	
t_{CHZ}	Chip Deselection to Output in High-Z	0	15	0	20	0	20	
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	20	-	30	-	30	

Write Cycle

SYMBOL	PARAMETER	TMM2068AD-25		TMM2068AD-35		TMM2068AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	45	-	ns
t_{CW}	Chip Selection to End of Write	20	-	30	-	40	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	20	-	30	-	35	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	0	10	0	15	0	15	
t_{DS}	Data Set Up Time	10	-	15	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

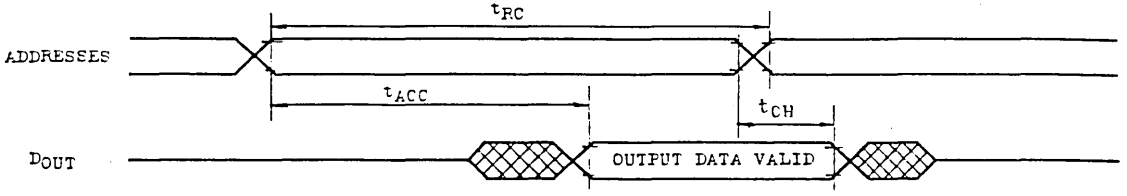
A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

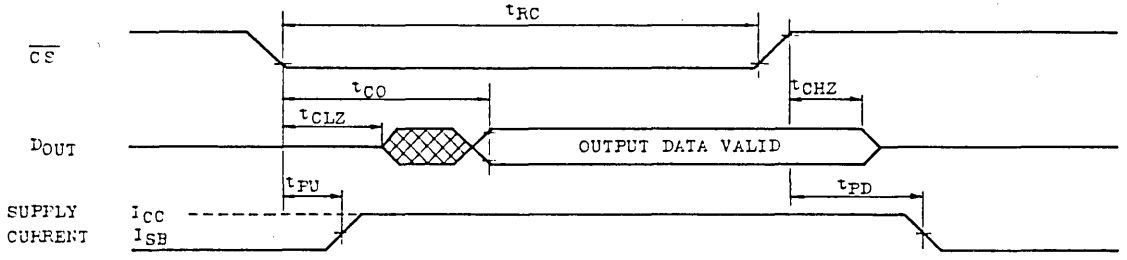


TIMING WAVEFORMS

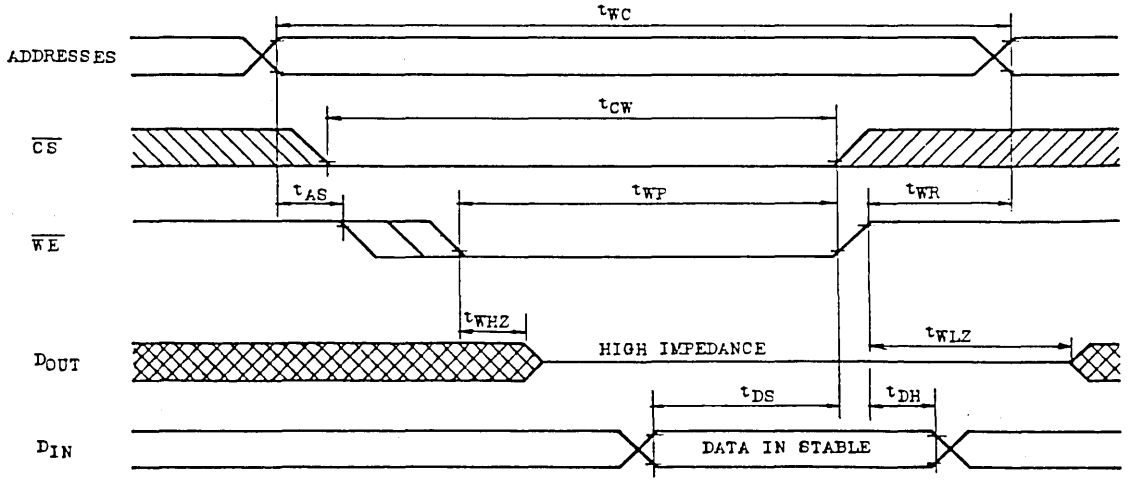
READ CYCLE 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})



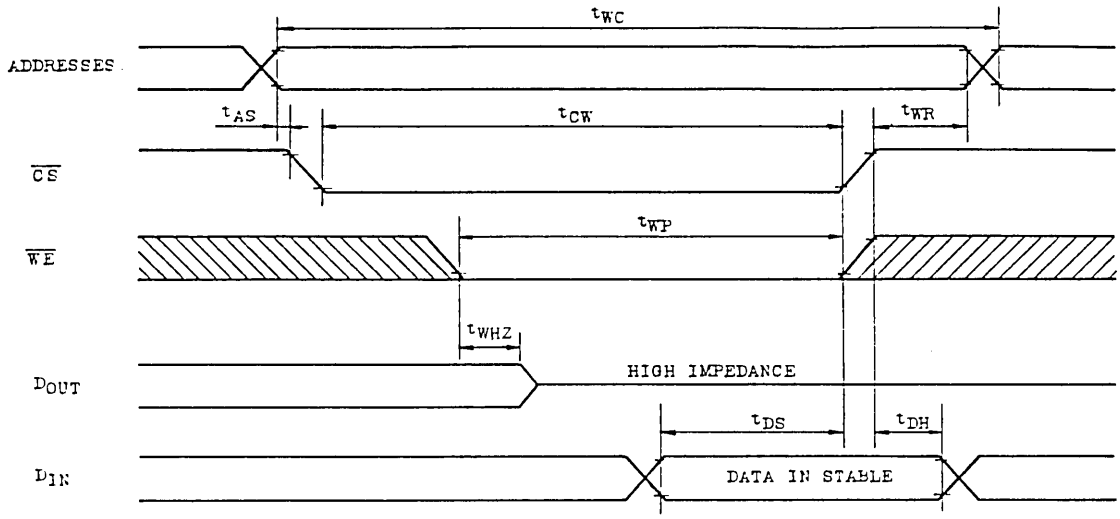
READ CYCLE 2. ($\overline{WE}$=V_{IH})



WRITE CYCLE 1.



WRITE CYCLE 2.

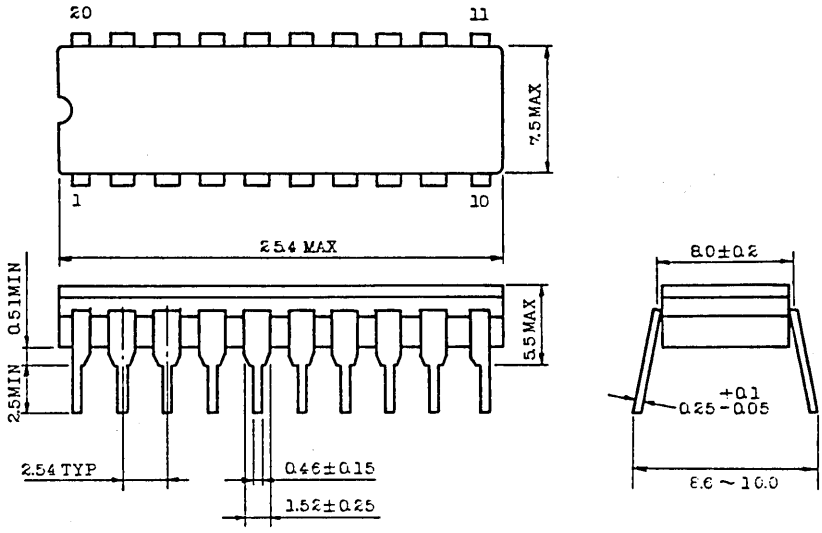


Note 1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.

2. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.20 leads.

4,096 WORD × 4 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2068AP-25, TMM2068AP-35 TMM2068AP-45

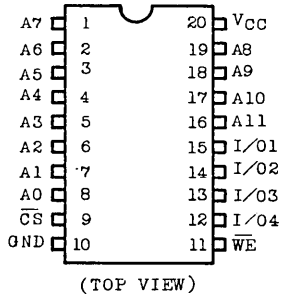
DESCRIPTION

The TMM2068AP is a 16,384 bits high speed and low power static random access memory organized as 4,096 words by 4 bits and operates from a single 5V supply.
Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 135/120/120mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.
Thus the TMM2068AP is most suitable for us in cache memory and high speed storage.
The TMM2068AP is offered in a 20 pin standard plastic package with 0.3 inch width for high density assembly.
The TMM2068AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time
  t_{ACC}=25ns: TMM2068AP-25
  t_{ACC}=35ns: TMM2068AP-35
  t_{ACC}=45ns: TMM2068AP-45
- Low power dissipation
  I_{CC}=135mA: TMM2068AP-25
  I_{CC}=120mA: TMM2068AP-35
  I_{CC}=120mA: TMM2068AP-45
  I_{SB}=20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs: Directly TTL compatible
- Power down feature : $\overline{CS}$=V_{IH}
- Three state outputs
- Inputs protected: All inputs protection aganist static charge.
- Package: 20 pins standard plastic package, 0.3 inch width.

PIN CONNECTION

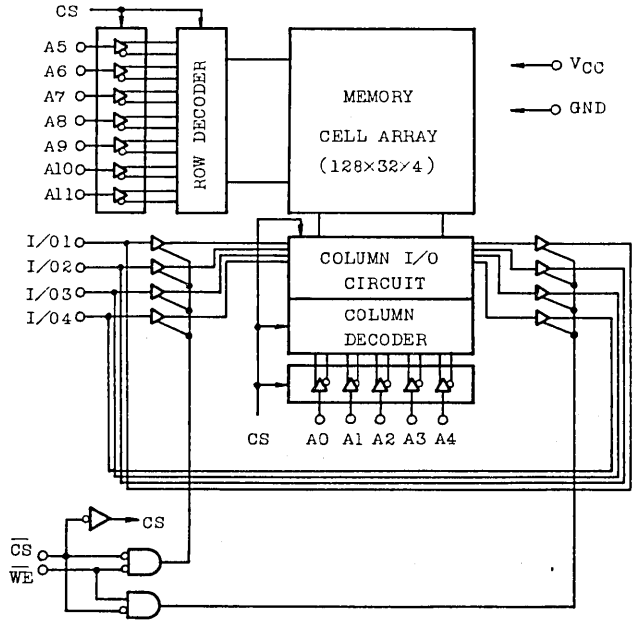


(TOP VIEW)

PIN NAMES

A0 ∿ A11	Address Inputs
I/O1 ∿ I/O4	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5 ∿ 7.0	V
V_{IN}	Input Voltage	-3.5 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-3.5 ∿ 7.0	V
T_{opr}	Operating Temperature	0 ∿ 70	°C
T_{stg}	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation	1.0	W
I_{OUT}	D.C. Output Current	20	mA

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V (Min.)

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	MAX.	UNIT
I_{IL}	Input Current	V_{IN}=0 ∿ V_{CC}		-	±1.0	μA
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4	-	V
V_{OL}	Output Low Voltage	I_{OL}=8.0mA		-	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0 ∿ V_{CC}, $\overline{CS}$=V_{IH}		-	±1.0	μA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}	-25	-	135	mA
			-35	-	120	
			-45	-	120	
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}		-	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, V_{CC}=0 ∿ 5.5V		-	40	mA

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	8	

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2068AP-25		TMM2068AP-35		TMM2068AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	45	-	ns
t_{ACC}	Address Access Time	-	25	-	35	-	45	
t_{CO}	Chip Select Access Time	-	25	-	35	-	45	
t_{CLZ}	Chip Selection to Output in Low-Z	5	-	5	-	5	-	
t_{CHZ}	Chip Deselection to Output in High-Z	0	15	0	20	-	20	
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	20	-	30	-	30	

Write Cycle

SYMBOL	PARAMETER	TMM2068AP-25		TMM2068AP-35		TMM2068AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	45	-	ns
t_{CW}	Chip Selection to End of Write	20	-	30	-	40	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	20	-	30	-	35	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	0	10	0	15	0	15	
t_{DS}	Data Set Up Time	10	-	15	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

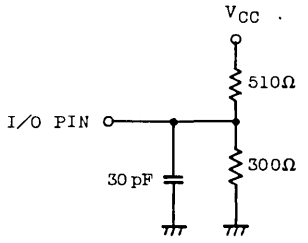
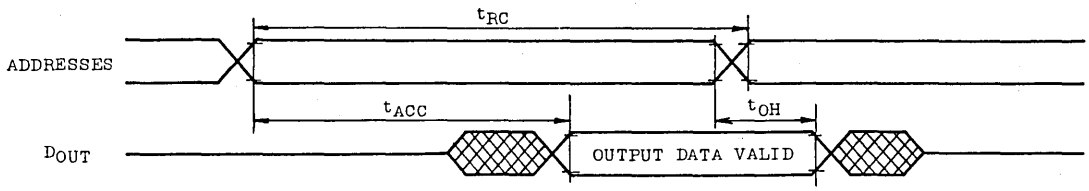


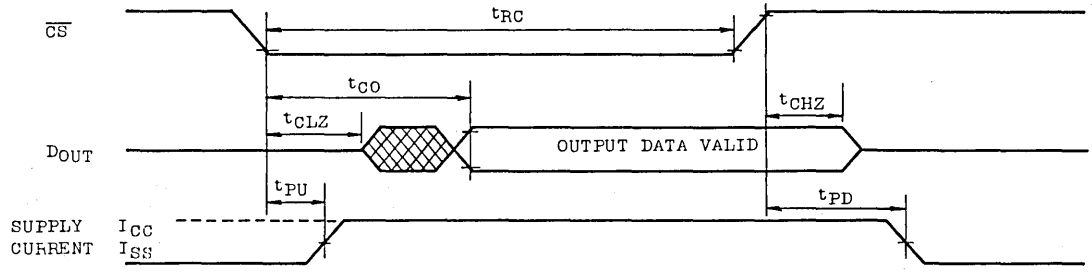
Fig.1 OUTPUT LOAD

TIMING WAVEFORMS

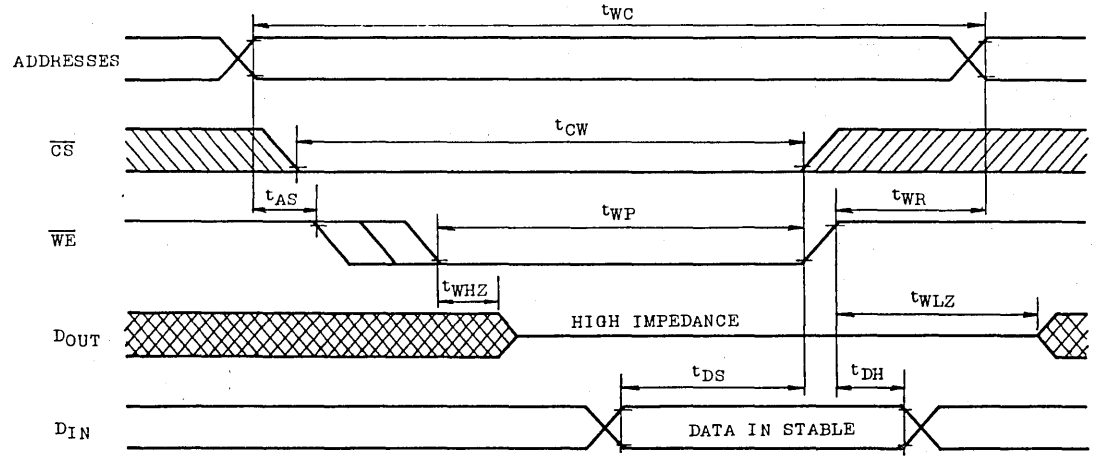
READ CYCLE 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})



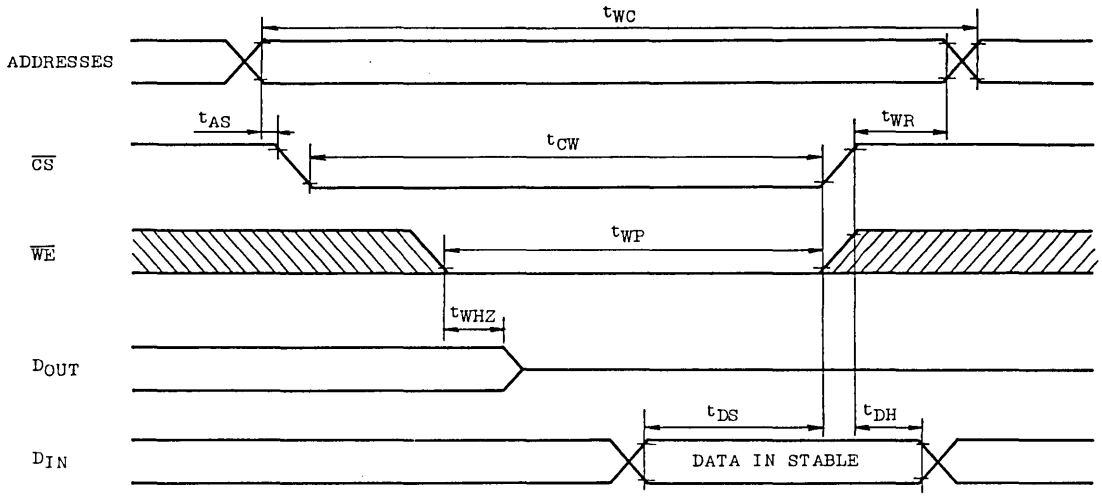
READ CYCLE 2. ($\overline{WE}$=V_{IH})



WRITE CYCLE 1.



WRITE CYCLE 2.

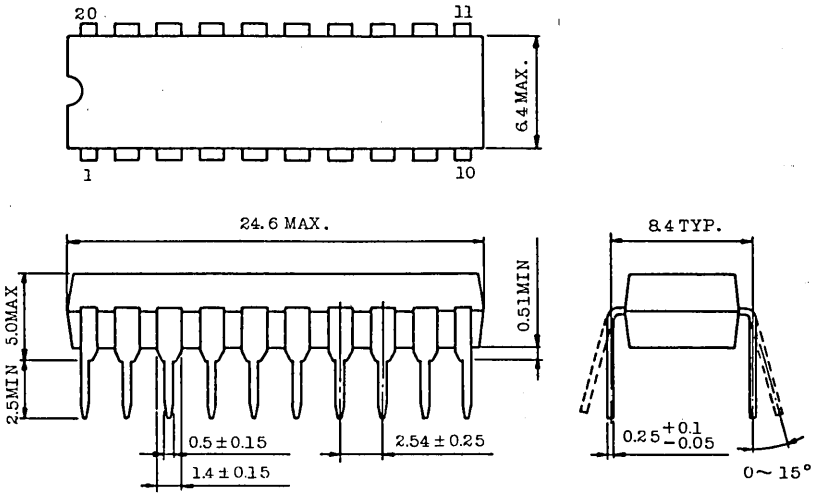


Note 1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.

2. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.20 leads.

TOSHIBA MOS MEMORY PRODUCT

4,096 WORD × 4 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2078AD-25, TMM2078AD-35
TMM2078AD-45

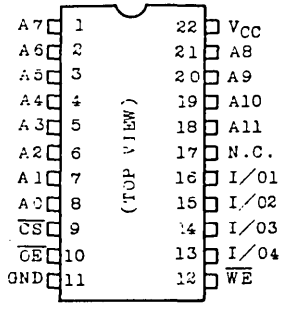
DESCRIPTION

The TMM2078AD is a 16,384 bits high speed and low power static random access memory organized as 4,096 words by 4 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 135mA/120mA/120mA When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.
Thus the TMM2078AD is most suitable for use in cache memory and high speed storage.
The TMM2078AD is offered in a 22 pin standard cerdip package with 0.3 inch width for high density assembly.
The TMM2078AD is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time
  - t_{ACC}=25ns: TMM2078AD-25
  - t_{ACC}=35ns: TMM2078AD-35
  - t_{ACC}=45ns: TMM2078AD-45
- Low power dissipation
  - I_{CC}=135mA: TMM2078AD-25
  - I_{CC}=120mA: TMM2078AD-35
  - I_{CC}=120mA: TMM2078AD-45
  - I_{SB}=20mA
- Single 5V power supply
- Fully static operaion
- All inputs and outputs
  Directly TTL Compatible
- Power down feature: $\overline{CS}$=V_{IH}
- Output buffer control: $\overline{OE}$
- Three state outputs
- Inputs protected: All inputs protection against static charge.
- Package: 22 pins standard cerdip package, 0.3 inch width

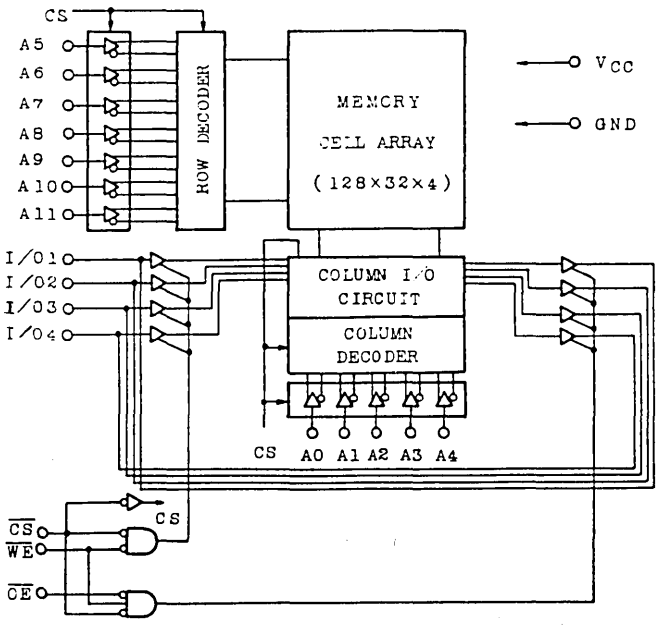
PIN CONNECTION



PIN NAMES

A_0-A_{11}	Address Inputs
I/O_1-I/O_4	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5-7.0	V
V_{IN}	Input Voltage	-3.5-7.0	V
$V_{I/O}$	Input/Output Voltage	-3.5-7.0	V
T_{opr}	Operating Temperature	0-70	°C
T_{stg}	Storage Temperature	-55-150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation	0.9	W
I_{OUT}	D.C. Output Current	20	mA

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V(MIN.)

D.C. CHARACTERISTICS (Ta=0-70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{IL}	Input Current	V_{IN}=0-V_{CC}		-	±1.0	μA
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4	-	V
V_{OL}	Output Low Voltage	I_{OL}=8.0mA		-	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0-V_{CC}, $\overline{CS}$=V_{IH}		-	±1.0	μA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}	-25	-	135	mA
			-35	-	120	
			-45	-	120	
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}		-	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, V_{CC}=0-5.5V		-	40	mA

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	8	

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (T_a=0-70°C, V_{CC}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2078AD-25		TMM2078AD-35		TMM2078AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	45	-	ns
t_{ACC}	Address Access Time	-	25	-	35	-	45	
t_{CO}	Chip Select Access Time	-	25	-	35	-	45	
t_{OE}	Output Enable to Output Valid	-	15	-	20	-	20	
t_{CLZ}	Chip Selection to Output in Low-Z	0	-	0	-	5	-	
t_{CHZ}	Chip Deselection to Output in High-Z	-	15	-	20	-	20	
t_{OLZ}	Output Enable to Output in Low-Z	0	-	0	-	0	-	
t_{OHZ}	Output Disable to Output in High-Z	-	10	-	15	-	15	
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	20	-	30	-	30	

WRITE CYCLE

SYMBOL	PARAMETER	TMM2078AD-25		TMM2078AD-35		TMM2078AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	45	-	ns
t_{CW}	Chip Selection to End of Write	20	-	30	-	40	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	20	-	30	-	35	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	-	10	-	15	-	15	
t_{DS}	Data Set Up Time	10	-	15	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

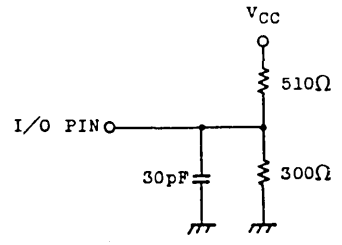
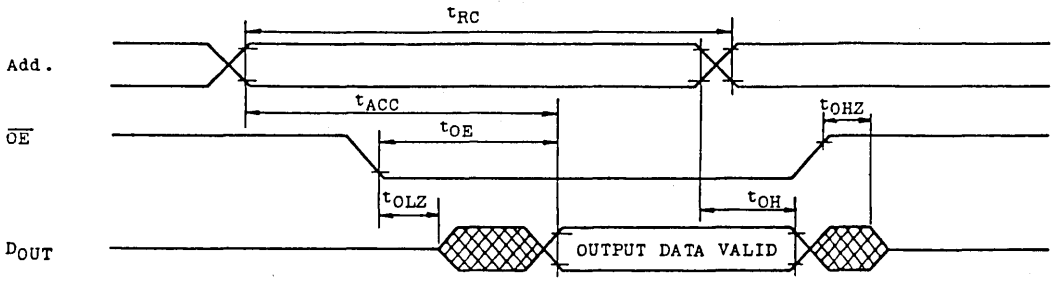


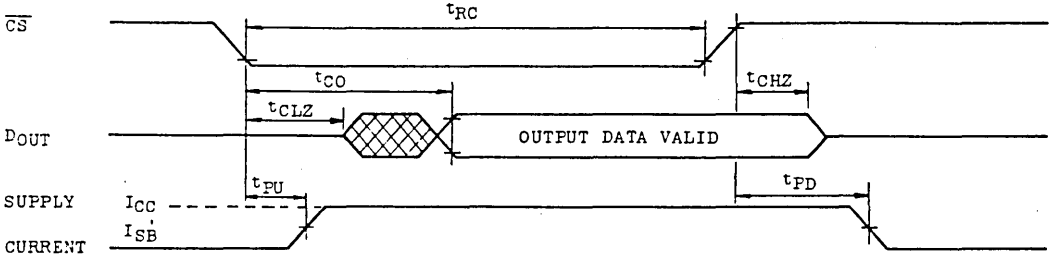
Fig.1 Output Load

TIMING WAVEFORMS

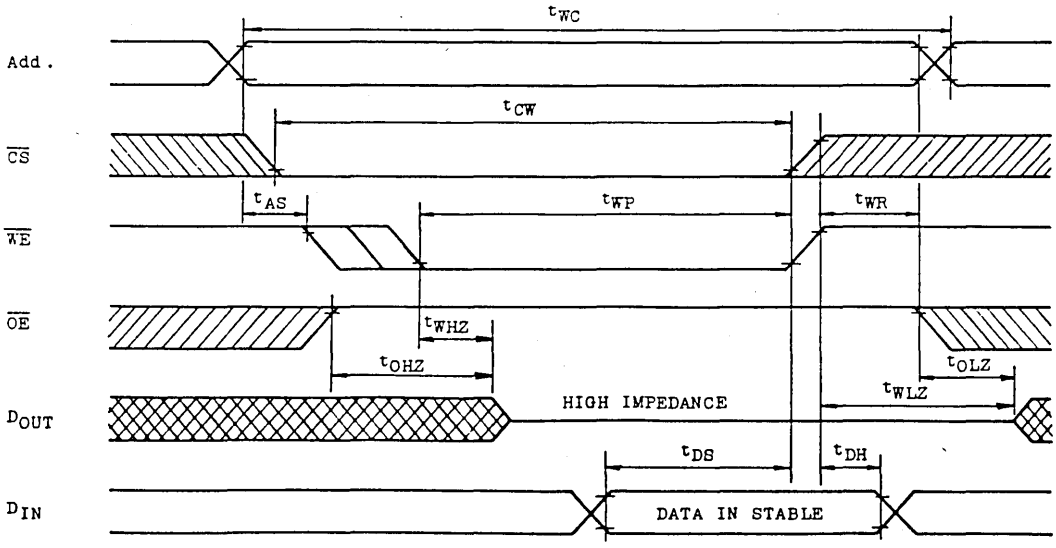
READ CYCLE 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})



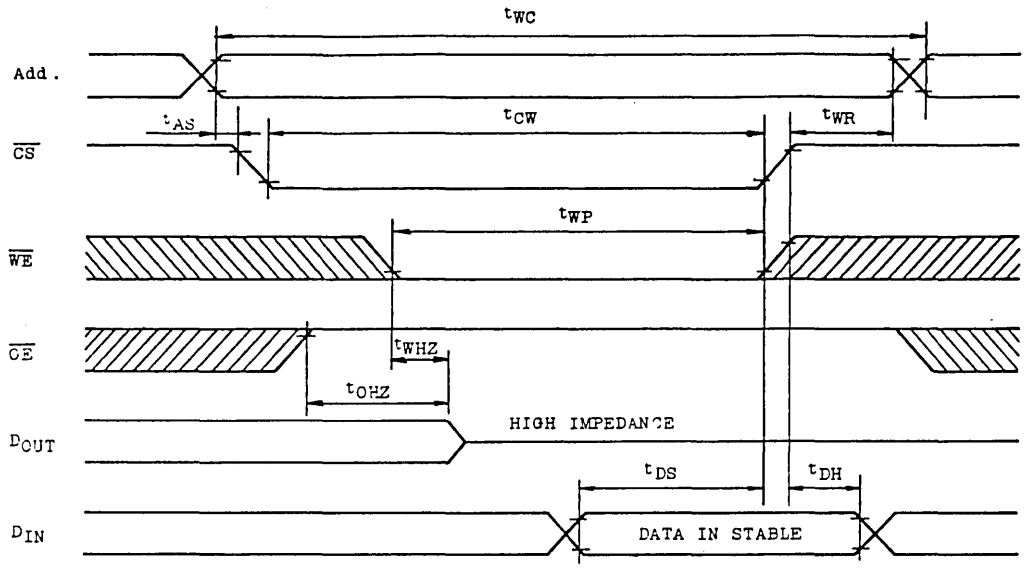
READ CYCLE 2. ($\overline{WE}$=V_{IH}, $\overline{OE}$=V_{IL})



WRITE CYCLE 1.



WRITE CYCLE 2.



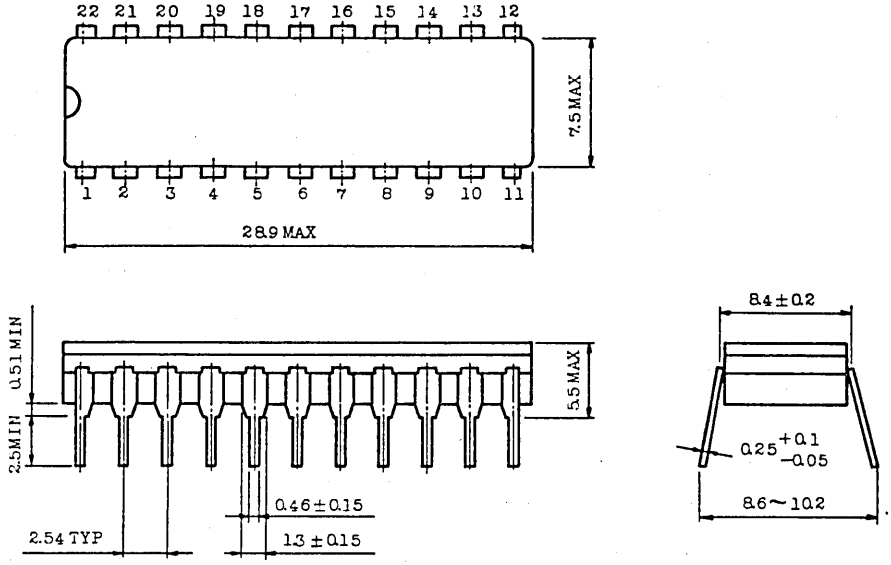
Note:

1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.

2. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.22 leads.

TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2088P-35, TMM2088P-45
TMM2088P-55

DESCRIPTION

The TMM2088P is a 65,536 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 8 bits and operates from a single 5-volt supply. The TMM2088P is features an automatic stand-by mode when deselect by $\overline{CS1}$ signal. Thus the TMM2088P is suitable for use in cache memory and high speed storage. The TMM2088P is offered in a 28 pin standard plastic dual in-line package with 0.3 inch width for high density assembly.

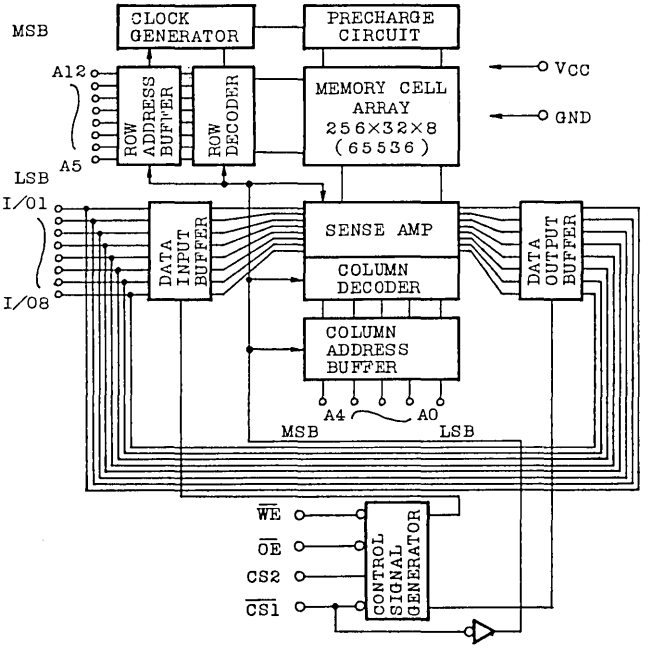
FEATURES

- Access Time and Current

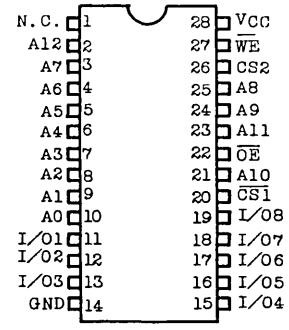
Parameter / Part Number	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2088P-35	35ns	135mA	15mA
TMM2088P-45	45ns	135mA	15mA
TMM2088P-55	55ns	135mA	15mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: ($\overline{CS1}$)
- Output Buffer Control: ($\overline{OE}$)
- Three State Outputs
- All Inputs and Outputs: (Directly TTL Compatible)
- Inputs Protected: (All inputs have Protection against static charge.)

BLOCK DIAGRAM



PIN CONNECTION



PIN NAMES

A0 ∿ A12	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS1}$, CS2	Chip Select Inputs
I/O1 ∿ I/O8	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground
N.C.	No Connection

OPERATION MODE

MODE	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O1 ∿ 8	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5 ∿ 7.0	V
V_{IN}, V_{OUT}	Input Output Voltage	-3.5 ∿ 7.0	V
$T_{opr.}$	Operating Temperature	0 ∿ 70	°C
$T_{stg.}$	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature • Time	260 • 10	°C•sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V (Min.)

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V ∿ 5.5V	-1.0	1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	-4.0	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	8.0	-	mA
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V∿5.5V	-1.0	1.0	μA
I_{SBP}	Peak Power-on Current	$\overline{CS1}$=V_{CC}, CS2=0V, I_{OUT}=0mA	-	30	mA
I_{SB}	Standby Current	$\overline{CS1}$=V_{IH}, I_{OUT}=0mA	-	15	mA
I_{CC}	Operating Current	$\overline{CS1}$=V_{IL}, I_{OUT}=0mA	-	135	mA

CAPACITANCE* (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2088P-35		TMM2088P-45		TMM2088P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	-	45	-	55	-	ns
t_{ACC}	Address Access Time	-	35	-	45	-	55	
t_{CO1}	$\overline{CS1}$ Access Time	-	35	-	45	-	45	
t_{CO2}	CS2 Access Time	-	25	-	25	-	30	
t_{OE}	$\overline{OE}$ Access Time	-	20	-	20	-	25	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	
t_{CLZ}	Output Enable Time from $\overline{CS1}$ or CS2	0	-	5	-	5	-	
t_{CHZ}	Output Disable Time from $\overline{CS1}$ or CS2	-	20	-	20	-	20	
t_{OLZ}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	
t_{OHZ}	Output Disable Time from $\overline{OE}$	-	15	-	15	-	20	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to POwer Down Time	-	30	-	30	-	30	

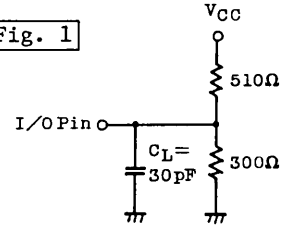
WRITE CYCLE

SYMBOL	PARAMETER	TMM2088P-35		TMM2088P-45		TMM2088P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	-	45	-	55	-	ns
t_{CW}	Chip Selection to End of Write	30	-	40	-	50	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	25	-	35	-	45	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{DS}	Data Set Up Time	15	-	20	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	
t_{WLZ}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	
t_{WHZ}	Output Disable Time from $\overline{WE}$	-	15	-	15	-	20	

A.C. TEST CONDITIONS

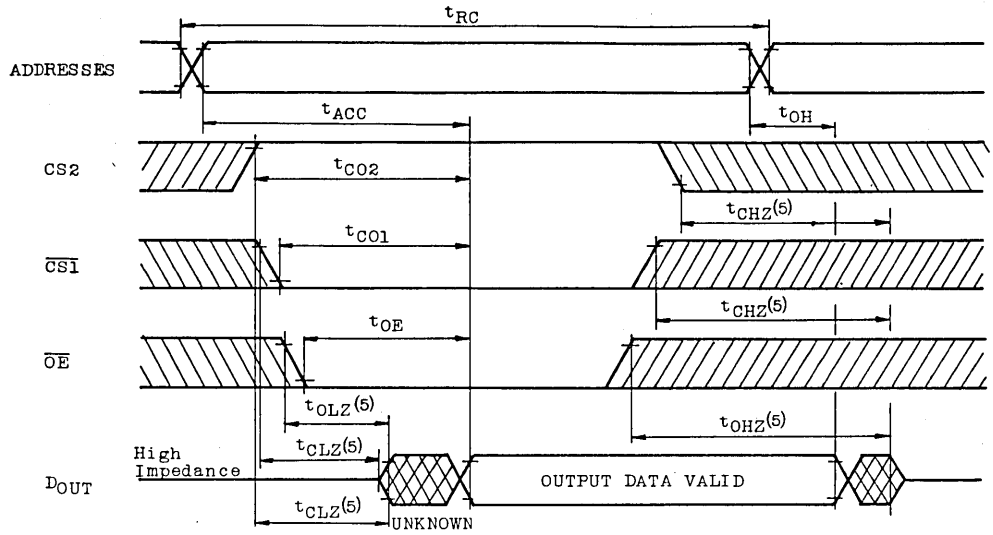
Input Pulse Levels	0.0 ∿ 3.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig. 1

Fig. 1

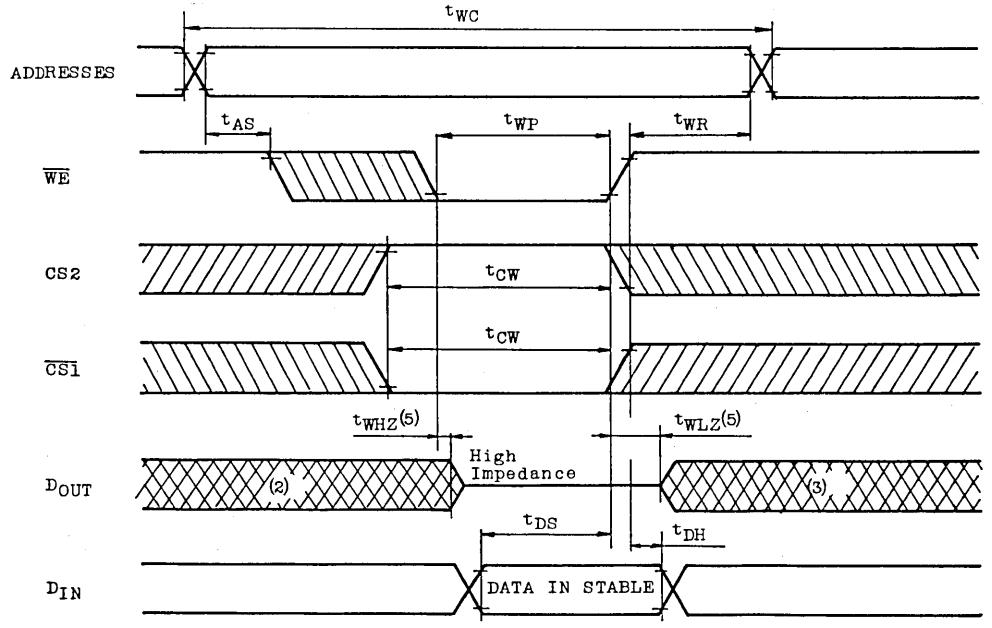


TIMING WAVEFORMS

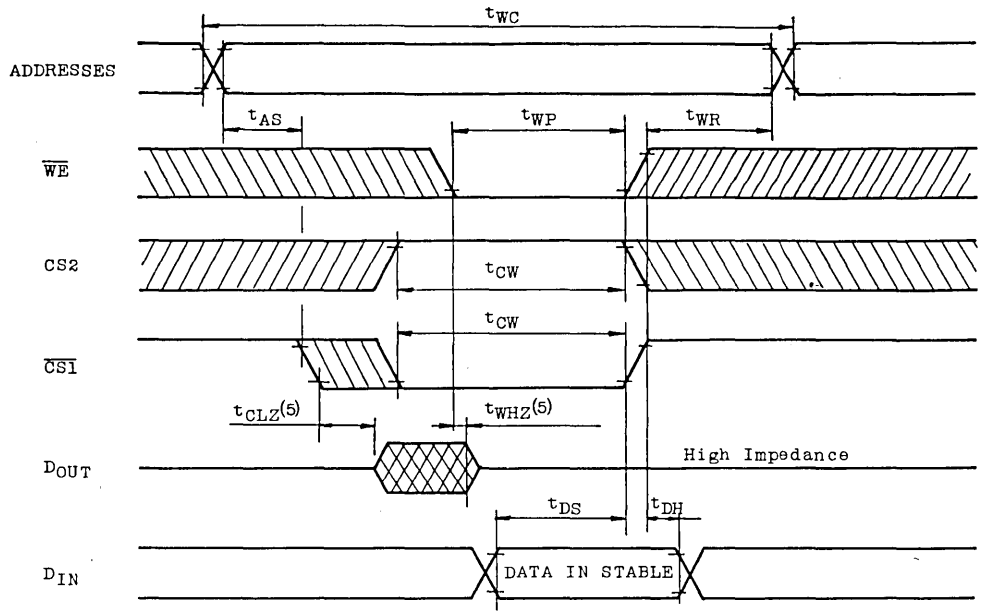
READ CYCLE (1)



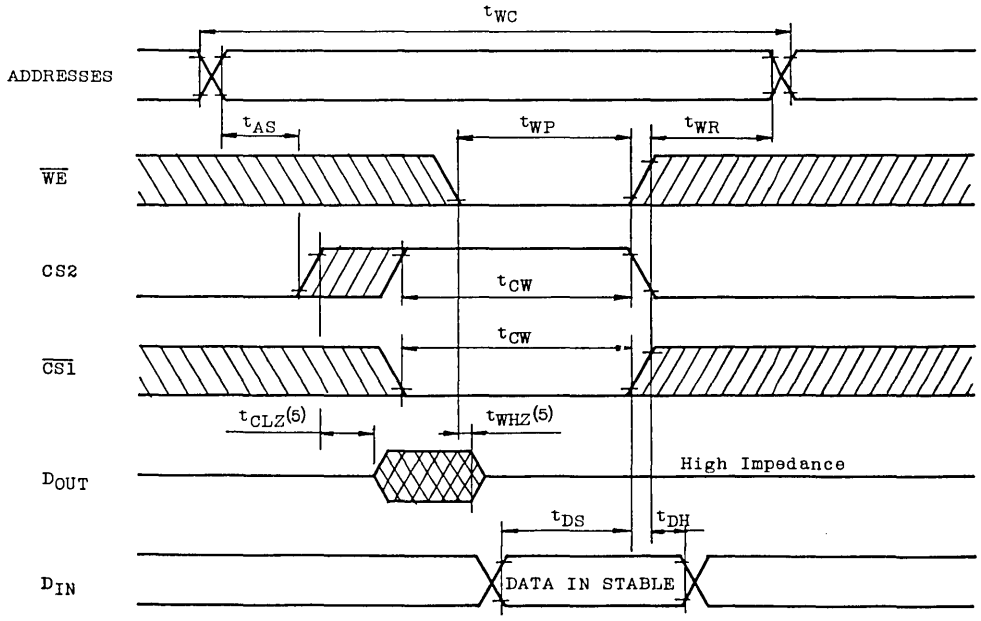
WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

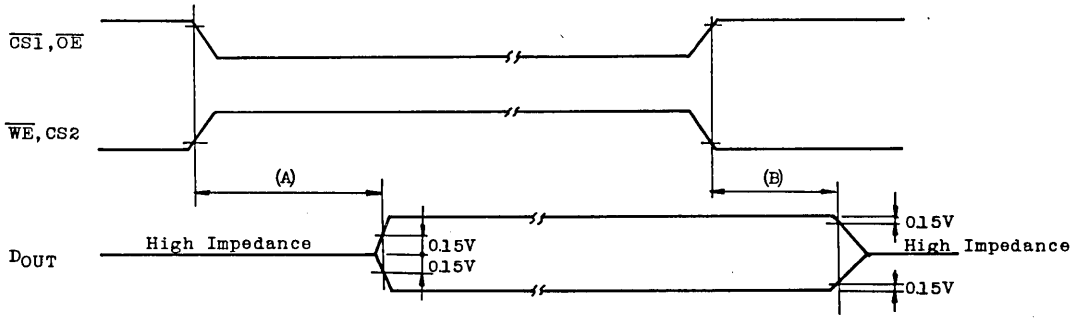
3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

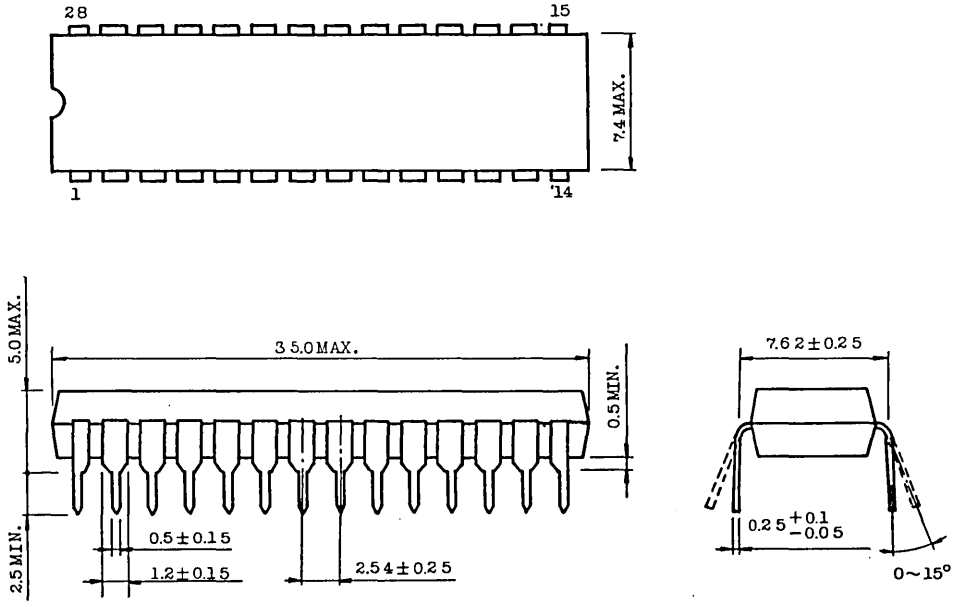
(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time



DIP 28 PIN OUTLINE DRAWING

Unit in mm



Note: Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 9 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2089C-35
TMM2089C-45
TMM2089C-55

PRELIMINARY

DESCRIPTION

The TMM2089C is a 73,728 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 9 bits and operates from a single 5-volt supply. The TMM2089C is features an automatic stand-by mode when deselect by $\overline{CS1}$ signal. Thus the TMM2089C is suitable for use in cache memory and high speed storage. The TMM2089C has nine I/O terminals, therefore it is most suitable for MEMORY SYSTEM with Parity bit. The TMM2089C is offered is a 28 pin standard ceramic dual in-line package with 0.3 inch width for high density assembly.

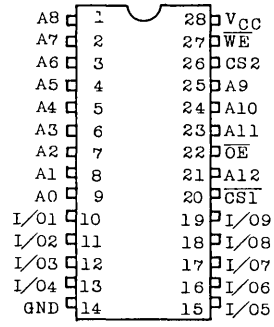
FEATURES

- Access Time and Current

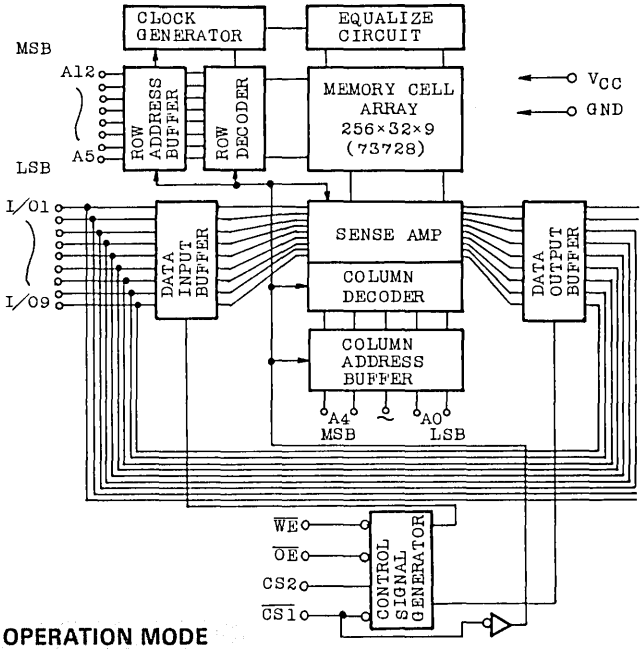
Part Number \ Parameter	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2089C-35	35ns	135mA	15mA
TMM2089C-45	45ns	135mA	15mA
TMM2089C-55	55ns	135mA	15mA

- Single 5V Power Supply
- Fully static Operation
- Power Down Feature : ($\overline{CS1}$)
- Output Buffer Control : ($\overline{OE}$)
- Three State Outputs
- All Inputs and Outputs: (Directly TTL Corpatible)
- Inputs Protected : (All inputs have protection against static charge.)

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
I/O1~I/O9	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground

OPERATION MODE

MODE	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O1~9	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−3.5~7.0	V
V_{IN}, V_{OUT}	Input Output Voltage	−3.5~7.0	V
$T_{opr.}$	Operating Temperature	0~70	°C
$T_{stg.}$	Storage Temperature	−55~150	°C
T_{nolder}	Soldering Temperature.·Time	260·10	°C·sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−3.0	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V

* Pulse width : 10ns, DC : −0.5V (Min.)

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−1.0	1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	−4.0	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	8.0	—	mA
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−1.0	1.0	μA
I_{SBP}	Peak Power-on Current	$\overline{CS1}$=V_{CC}, CS2=0V, I_{OUT}=0mA	—	30	mA
I_{SB}	Standby Current	$\overline{CS1}$=V_{IH}, I_{OUT}=0mA	—	15	mA
I_{CC}	Operating Current	$\overline{CS1}$=V_{IL}, I_{OUT}=0mA	—	135	mA

CAPACITANCE * (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

* Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2089C-35		TMM2089C-45		TMM2089C-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{ACC}	Address Access Time	—	35	—	45	—	55	
t_{CO1}	$\overline{CS1}$ Access Time	—	35	—	45	—	45	
t_{CO2}	CS2 Access Time	—	25	—	25	—	30	
t_{OE}	$\overline{OE}$ Access Time	—	20	—	20	—	25	
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	
t_{CLZ}	Output Enable Time from $\overline{CS1}$ or CS2	0	—	5	—	5	—	
t_{CHZ}	Output Disable Time from $\overline{CS1}$ or CS2	—	20	—	20	—	20	
t_{OLZ}	Output Enable Time from $\overline{OE}$	0	—	0	—	0	—	
t_{OHZ}	Output Disable Time from $\overline{OE}$	—	10	—	10	—	15	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Dowen Time	—	30	—	30	—	30	

WRITE CYCLE

SYMBOL	PARAMETER	TMM2089C-35		TMM2089C-45		TMM2089C-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{CW}	Chip Selection to End of Write	30	—	40	—	50	—	
t_{AS}	Address Set Up Time	0	—	0	—	0	—	
t_{WP}	Write Pulse Width	25	—	35	—	45	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Set UP Time	15	—	20	—	20	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{WLZ}	Output Enable Time from $\overline{WE}$	0	—	0	—	0	—	
t_{WHZ}	Output Disable Time from $\overline{WE}$	—	10	—	10	—	15	

A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig.1

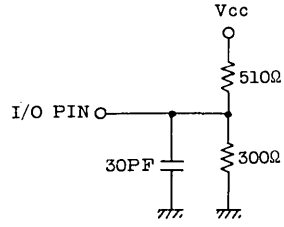
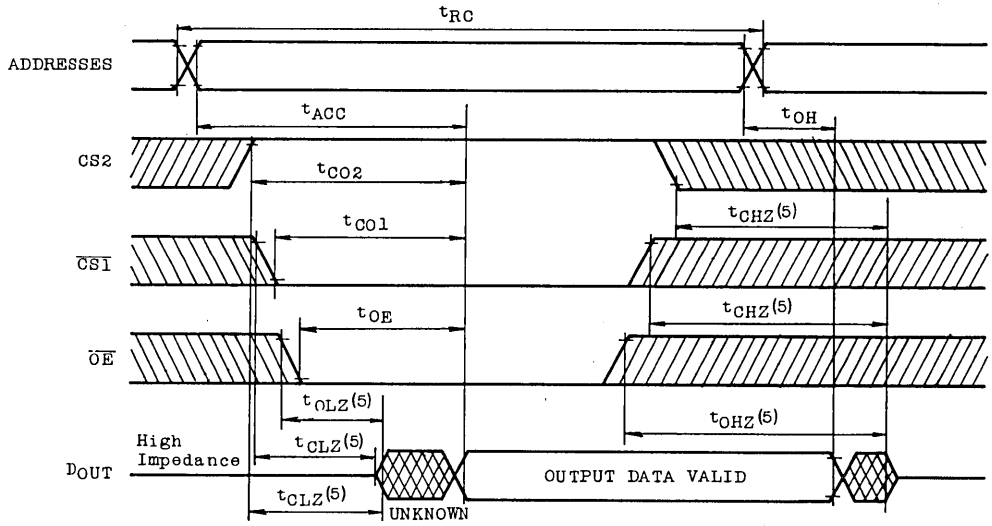


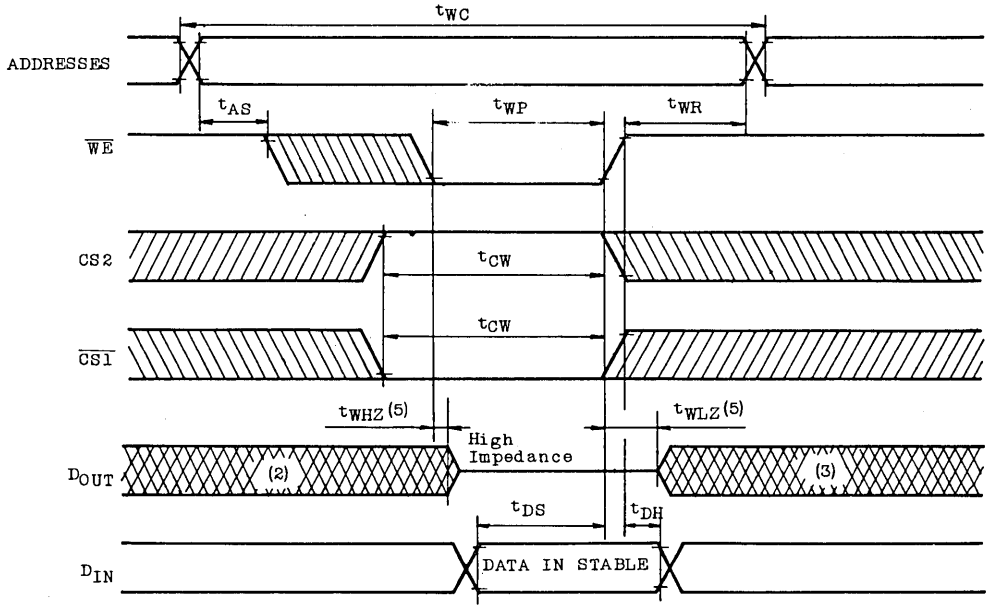
Fig.1 Output Load

TIMING WAVEFORMS

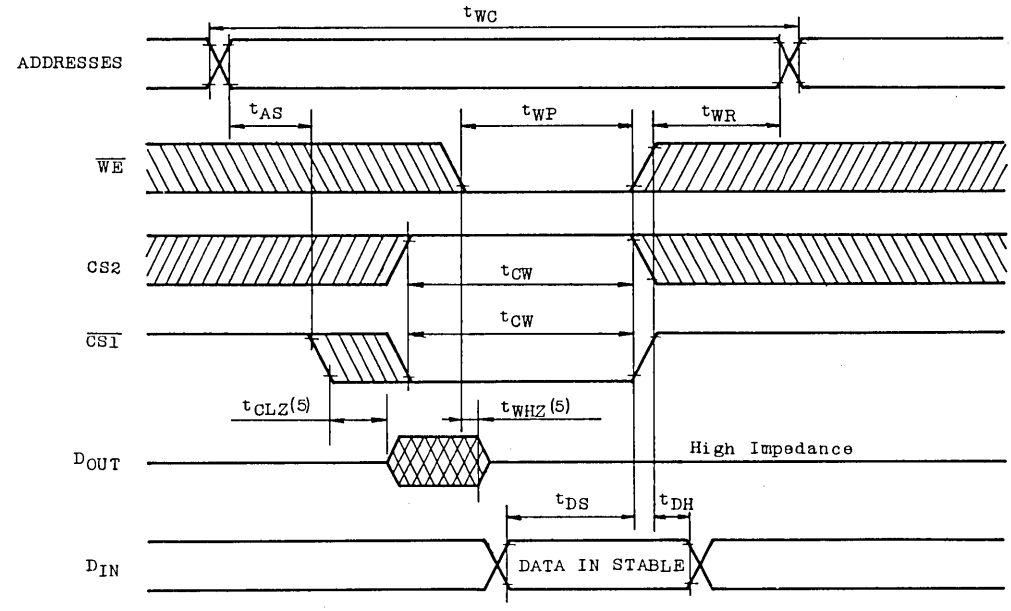
- READ CYCLE (1)



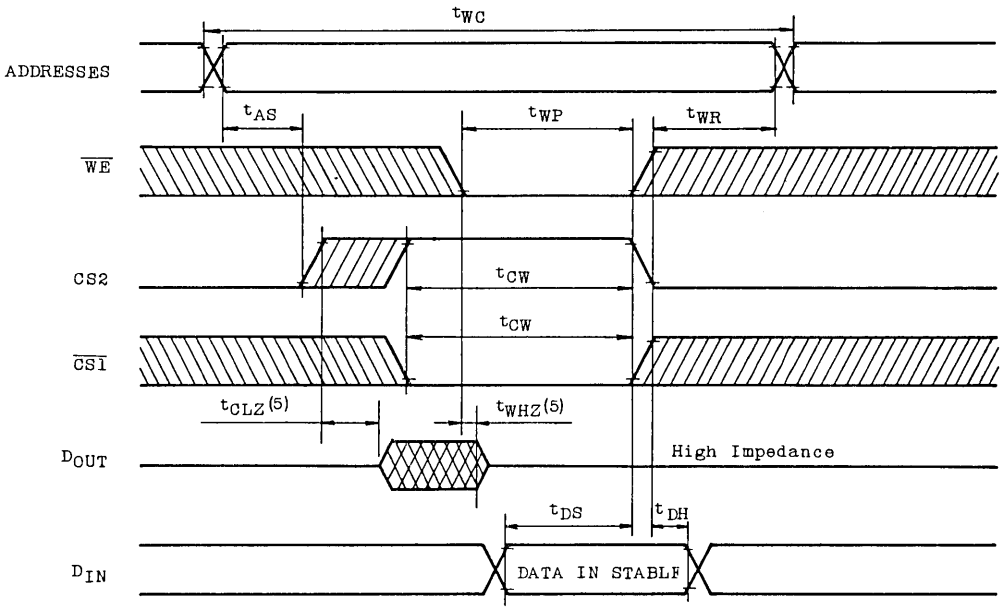
- WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



● WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



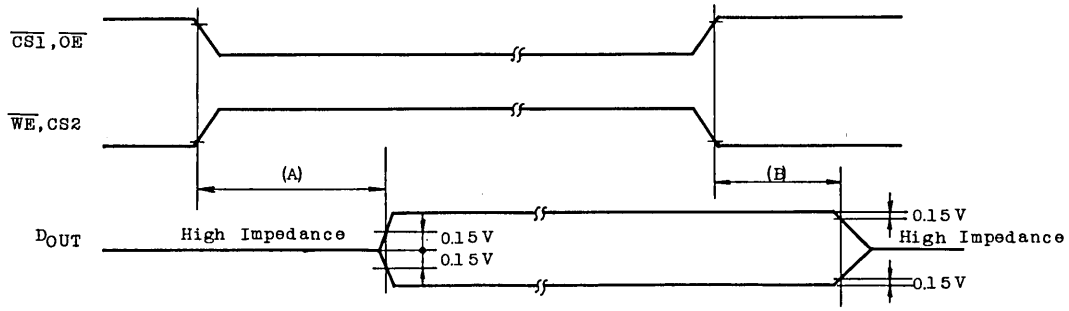
● WRITE CYCLE 3 (4) ($\overline{CS2}$ Controlled Write)



NOTE :

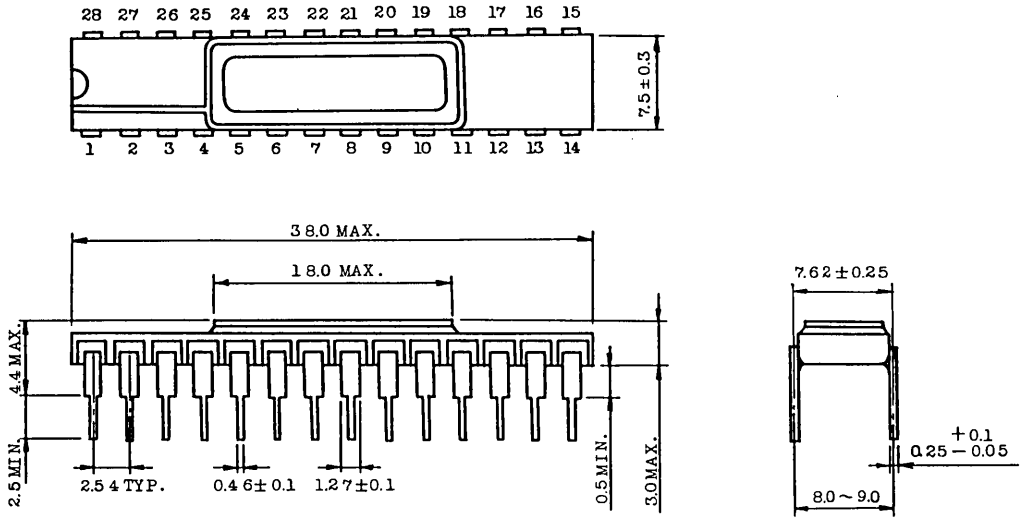
1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS1}$ Hight transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain is a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ}·····Output Enable Time
(B) t_{CHZ}, t_{OHZ}, t_{WHZ}·····Output Disable Time



OUTLINE DRAWINGS

Unit: mm



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 9 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2089P-35, TMM2089P-45
TMM2089P-55

DESCRIPTION

The TMM2089P is a 73,728 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 9 bits and operates from a single 5-volt supply. The TMM2089P is features an automatic stand-by mode when deselect by $\overline{CS1}$ signal. Thus the TMM2089P is suitable for use in cache memory and high speed storage. TheTMM2089P has nine I/O terminals, therefore it is most suitable for MEMORY SYSTEM with Parity bit. The TMM2089P is offered in a 28 pin standard plastic dual in-line package with 0.3 inch width for high density assembly.

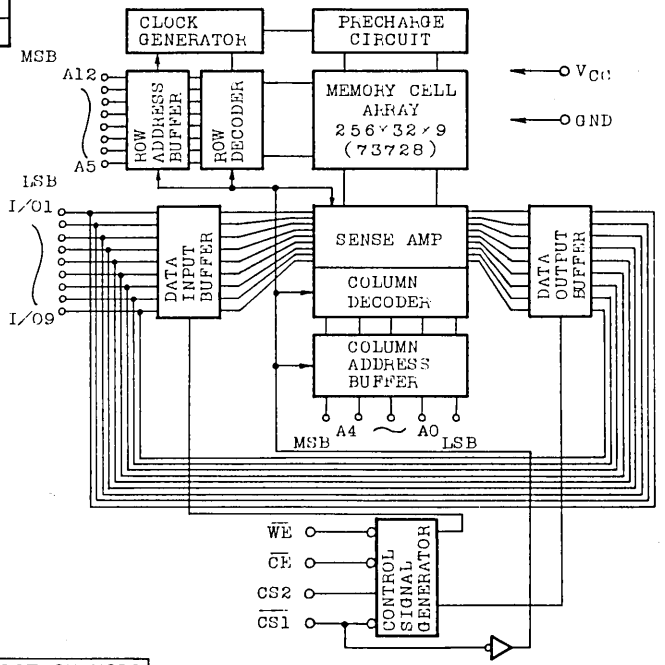
FEATURES

- Access Time and Current

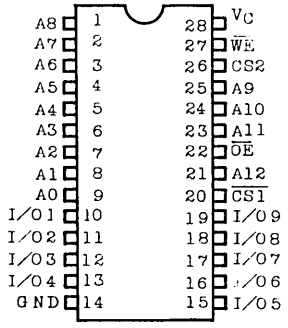
Part Number \ Parameter	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2089P-35	35ns	135mA	15mA
TMM2089P-45	45ns	135mA	15mA
TMM2089P-55	55ns	135mA	15mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: ($\overline{CS1}$)
- Output Buffer Control: ($\overline{OE}$)
- Three State Outputs
- All Inputs and Outputs: (Directly TTL Compatible)
- Inputs Protected: (All inputs have protection against static charge.)

BLOCK DIAGRAM



PIN CONNECTION



PIN NAMES

A0 ∿ A12	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS1}$, CS2	Chip Select Inputs
I/O1 ∿ I/O9	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

OPERATION MODE

MODE	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O1 ∿ 9	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5 ∿ 7.0	V
V_{IN}, V_{OUT}	Input Output Voltage	-3.5 ∿ 7.0	V
$T_{opr.}$	Operating Temperature	0 ∿ 70	°C
$T_{stg.}$	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V(Min.)

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V ∿ 5.5V	-1.0	1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	-4.0	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	8.0	-	mA
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V ∿ 5.5V	-1.0	1.0	μA
I_{SBP}	Peak Power-on Current	$\overline{CS1}$=V_{CC}, CS2=0V, I_{OUT}=0mA	-	30	mA
I_{SB}	Standby Current	$\overline{CS1}$=V_{IH}, I_{OUT}=0mA	-	15	mA
I_{CC}	Operating Current	$\overline{CS1}$=V_{IL}, I_{OUT}=0mA	-	135	mA

CAPACITANCE* (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	

* Note: This parameter is periodically smapled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2080P-35		TMM2089P-45		TMM2089P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	-	45	-	55	-	ns
t_{ACC}	Address Access Time	-	35	-	45	-	55	
t_{CO1}	$\overline{CS1}$ Access Time	-	35	-	45	-	45	
t_{CO2}	CS2 Access Time	-	25	-	25	-	30	
t_{OE}	$\overline{OE}$ Access Time	-	20	-	20	-	25	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	
t_{CLZ}	Output Enable Time from $\overline{CS1}$ or CS2	0	-	5	-	5	-	
t_{CHZ}	Output Disable Time from $\overline{CS1}$ or CS2	-	20	-	20	-	20	
t_{OLZ}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	
t_{OHZ}	Output Disable Time from $\overline{OE}$	-	15	-	15	-	20	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	30	-	30	-	30	

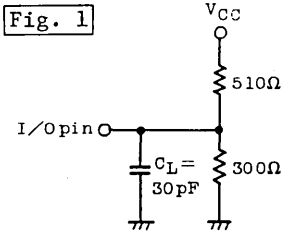
WRITE CYCLE

SYMBOL	PARAMETER	TMM2089P-35		TMM2089P-45		TMM2089P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	-	45	-	55	-	ns
t_{CS}	Chip Selection to End of Write	30	-	40	-	50	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	25	-	35	-	45	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{DS}	Data Set Up Time	15	-	20	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	
t_{WLZ}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	
t_{WHZ}	Output Disable Timf from $\overline{WE}$	-	15	-	15	-	20	

A.C. TEST CONDITIONS

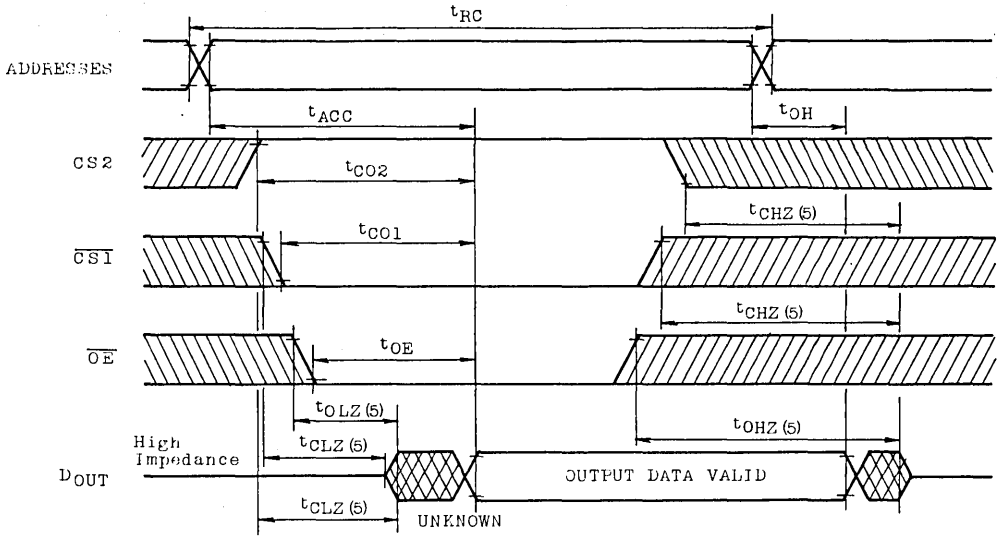
Input Pulse Levels	0.0V/3.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levles	2.0V/0.8V
Output Load	Fig. 1

Fig. 1

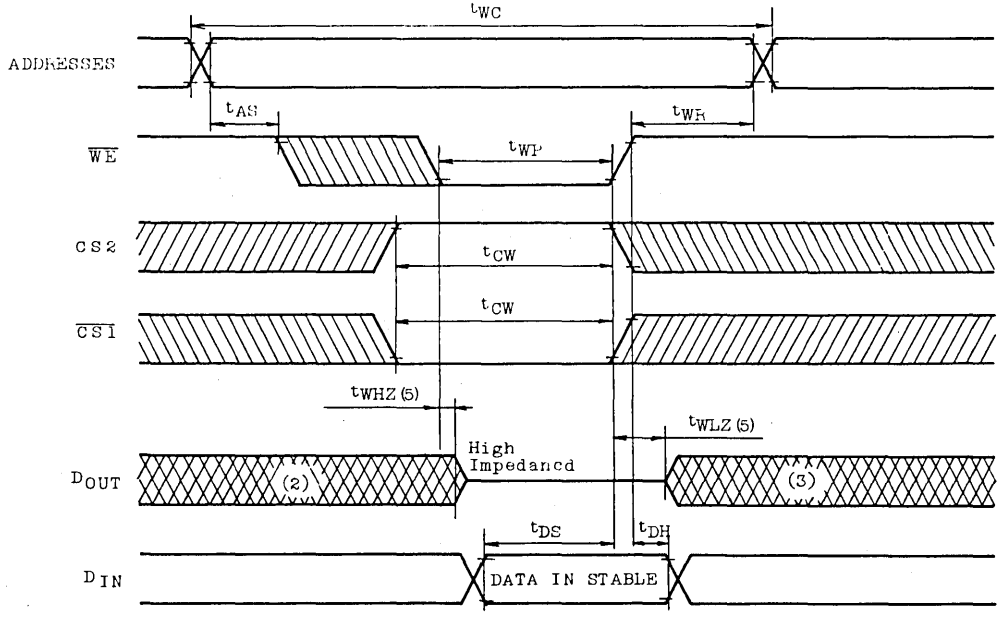


TIMING WAVEFORMS

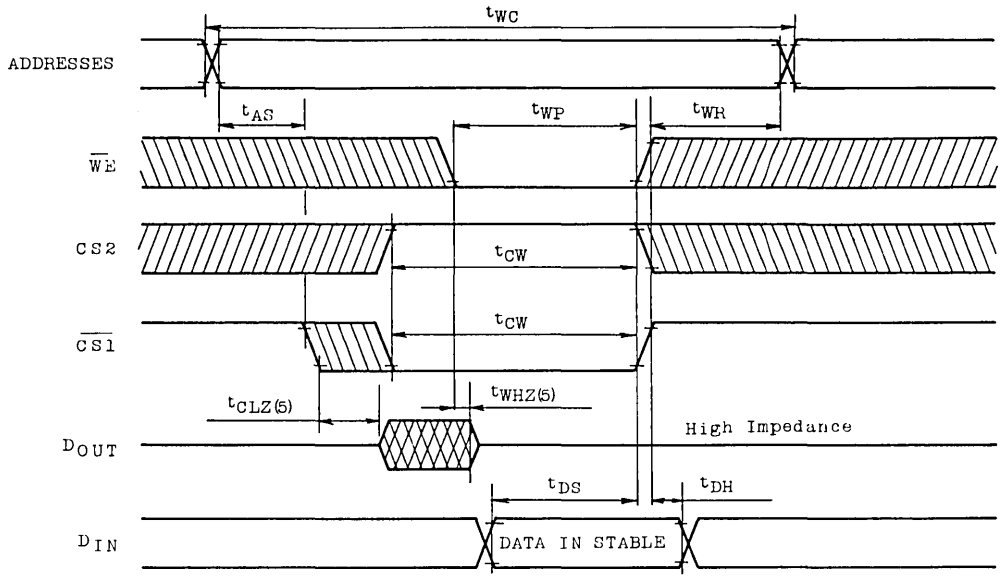
READ CYCLE (1)



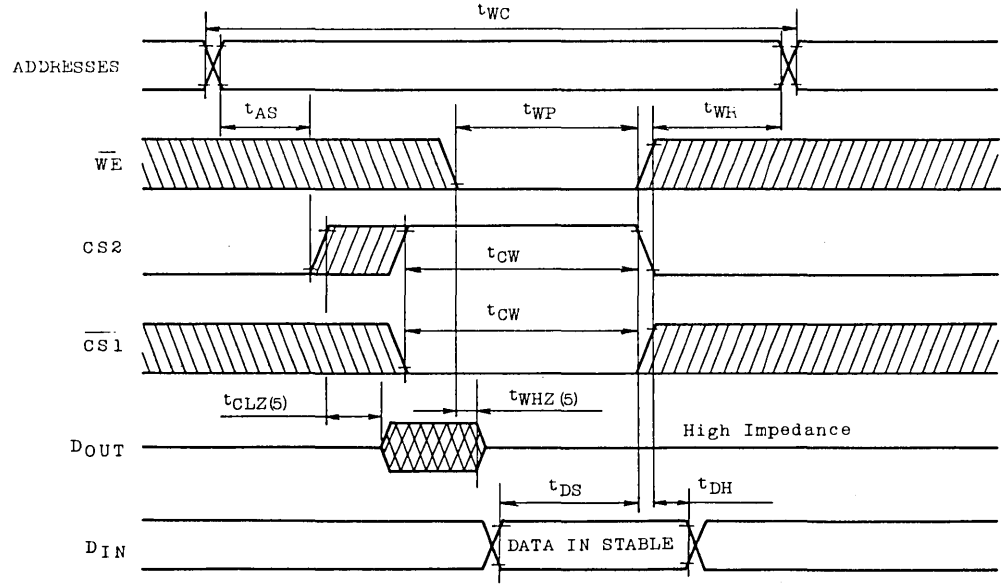
WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

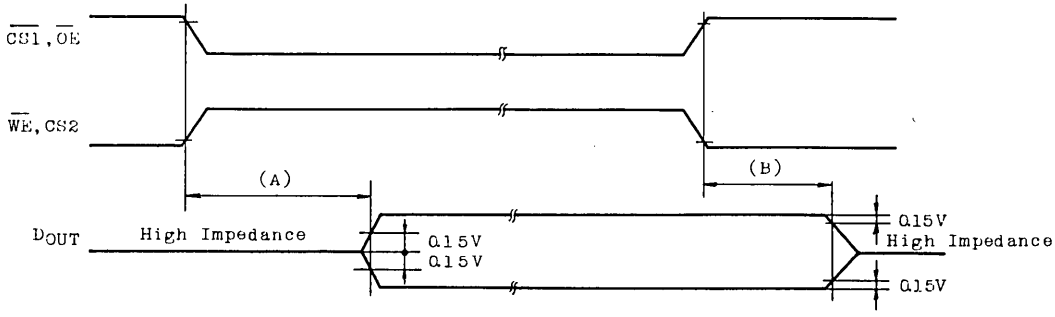
3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

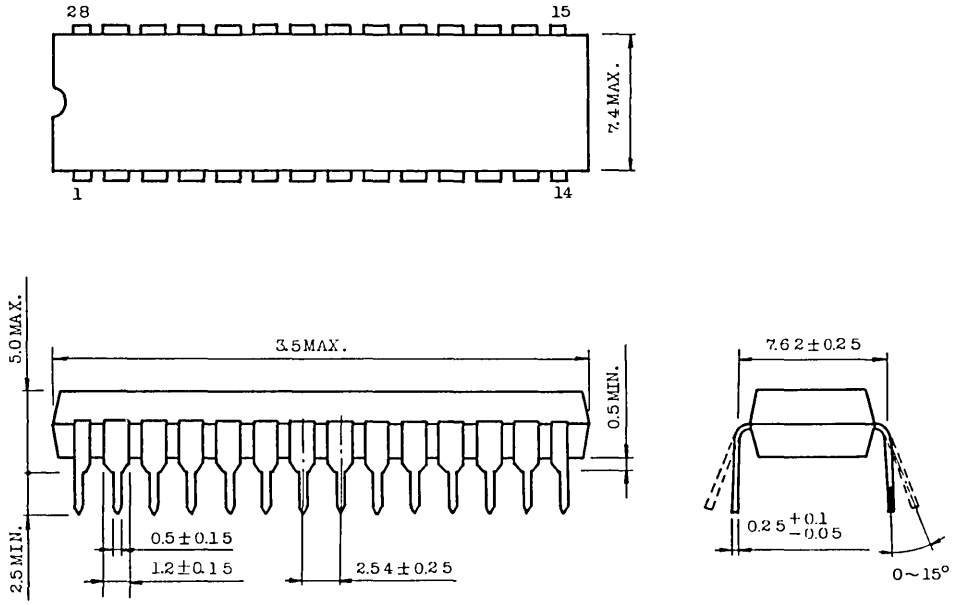
(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time



DIP 28 PIN OUTLINE DRAWING

Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

65,536 WORD × 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5561P-55
TC5561P-70

DESCRIPTION

The TC5561P is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and Operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 55ns/70ns and maximum operating current of 100mA at minimum cycle time.

The TC5561P also features an automatic stand-by mode. When deselected by Chip Enable (CE), the operating current is reduced from 100mA to 100μA.

The TC5561P is suitable for use in main memory of high speed computer and pattern memory, where high speed/low power/high density are required.

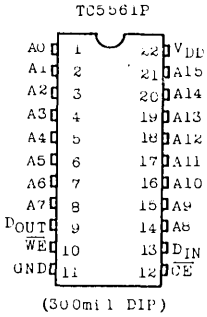
The TC5561P is moulded in a 22 pin standard plastic package with 0.3 inch width for high density assembly.

The TC5561P is fabricated with ion implanted COMS silicon gate MOS technology for high performance and high reliability.

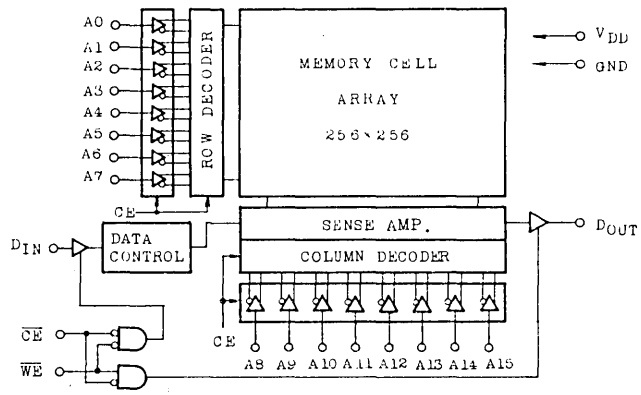
FEATURES

- Fast access time : TC5561P-55 55ns(MAX.)
  TC5561P-70 70ns(MAX.)
- Low power dissipation : Operation100mA(MAX.)
  Standby100μA(MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package, 300mil width

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{15}	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{SOLDER}	Soldering Temperature	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−3.0	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}	—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	−8	—	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	8	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=0~V_{DD}	—	—	±1.0	μA
I_{DDO}	Operating Current	V_{DD}=5.5V, t_{cycle}=Min cycle, $\overline{CE}$=V_{IL} Other Input=V_{IH}/V_{IL}	—	—	100	mA
I_{DDS1}	Standby Current	$\overline{CE}$=V_{IH}	—	—	2	mA
I_{DDS2}		$\overline{CE}$=V_{DD}−0.2V	—	—	100	μA

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5561P-55		TC5561P-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{ACC}	Address Access Time	—	55	—	70	
t_{CO}	Chip Enable Access Time	—	55	—	70	
t_{COE}	Chip Enable to Output in Low-Z	5	—	5	—	
t_{COD}	Chip Disable to Output in High-Z	—	30	—	30	
t_{OH}	Output Data Hold Time	5	—	5	—	

Write Cycle

SYMBOL	PARAMETER	TC5561P-55		TC5561P-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	35	—	
t_{CW}	Chip Enable to End of Write	35	—	35	—	
t_{AS}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{OEW}	$\overline{WE}$ to Output Low-Z	0	—	0	—	
t_{ODW}	$\overline{WE}$ to Output High-Z	—	30	—	30	
t_{DS}	Data Set up Time	35	—	35	—	
t_{DH}	Data Hold Time	0	—	0	—	

A. C. TEST CONDITIONS

Input Pulse Levels	2.4V/0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig.1

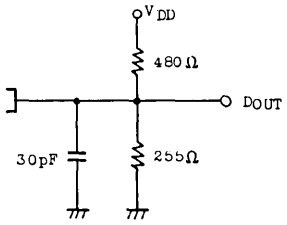
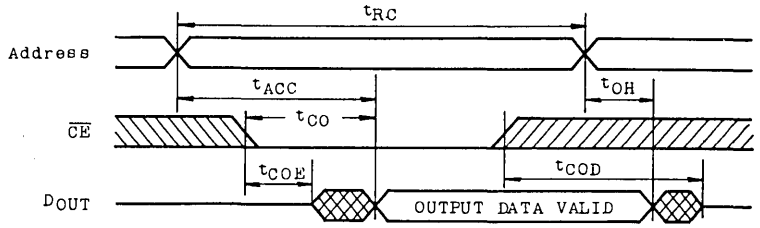


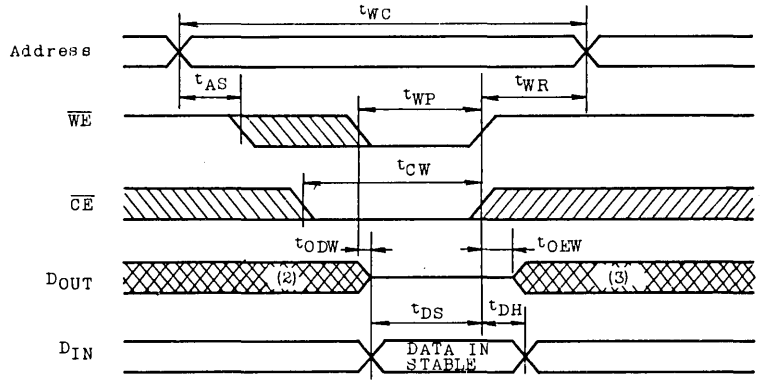
Fig.1 Output Load

TIMING WAVEFORMS

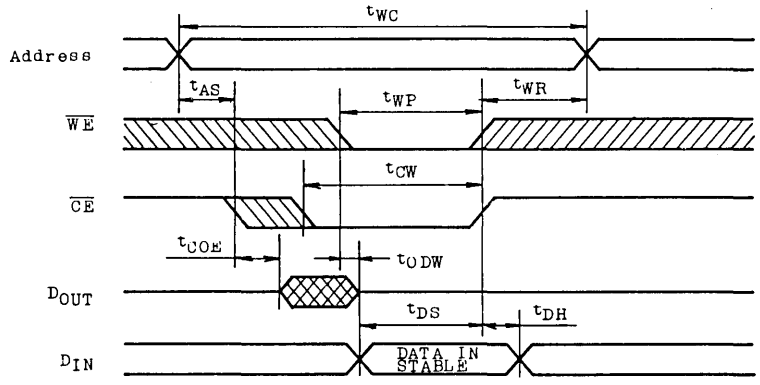
- READ CYCLE (1)



- WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

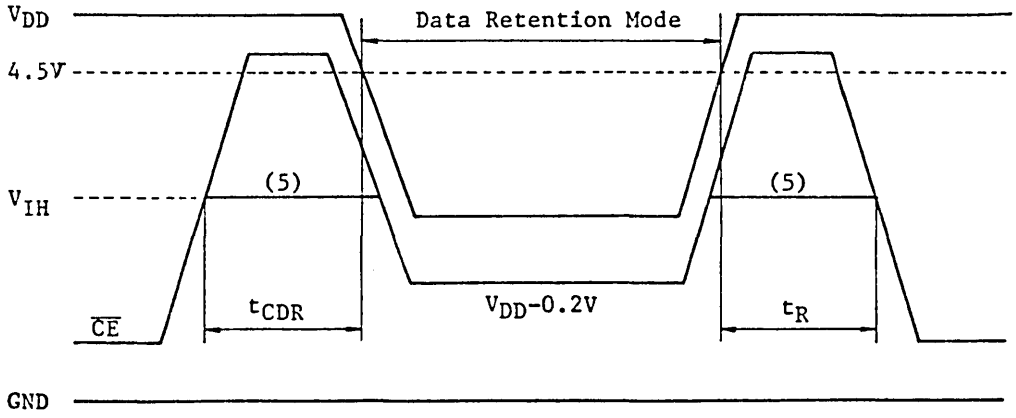


Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The operating temperature(Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

DATA RETENTION CHARACTERISTICS (Ta=−40~50°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Standby Supply Current	V_{DD}=3.0V	—	—	50	μA
		V_{DD}=5.5V	—	—	100	μA
t_{CDH}	Chip Deselection to Data Retntion Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}(1)	—	—	μs

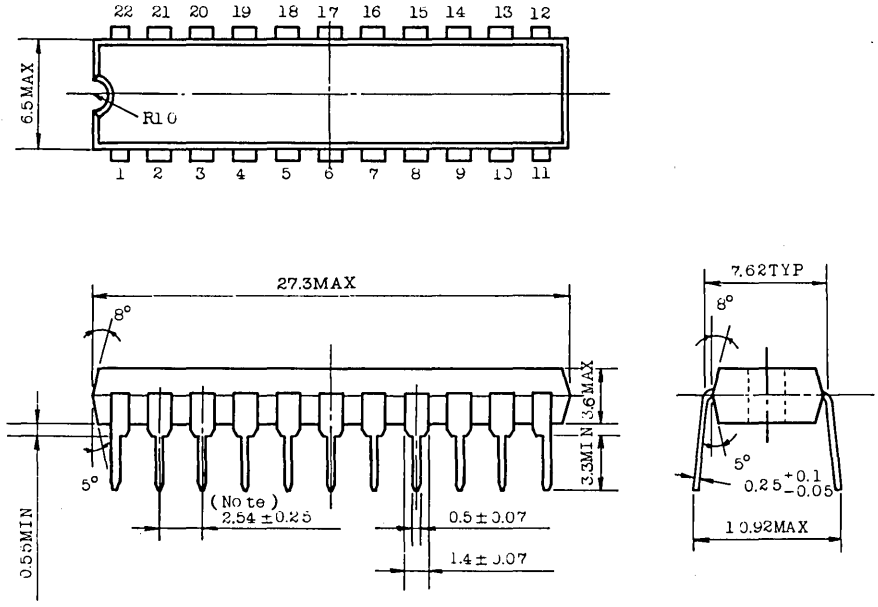


5. If the V_{IH} of $\overline{CE}$, is 2.2V in operation, I_{DDS1} current flows the period that V_{DD} voltage is going down from 4.5V to 2.5V.

TC5561P-55
TC5561P-70

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

TOSHIBA MOS MEMORY PRODUCT

65,536 WORD × 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5562P-45
TC5562P-55

DESCRIPTION

The TC5562P is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 45ns/55ns and maximum operating current of 100mA at minimum cycle time.

The TC5562P also features and automatic stand-by mode. When deselected by chip Enable($\overline{CE}$), the operating current is reduced from 100mA to 20mA.

The TC5562P is suitable for use in main memory of high speed/high density are required.

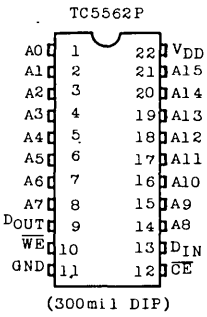
The TC5562P is moulded in a 22 pin standard plastic package with 0.3 inch width for high density assembly.

The TC5562P is fabricated with ion implanted COMS silicon gate MOS technology for high performance and high reliability.

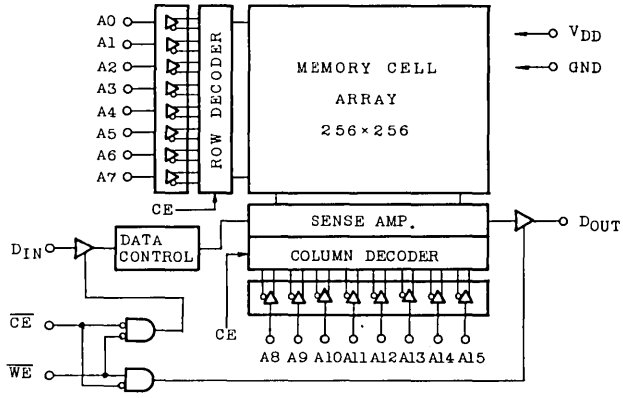
FEATURES

- Fast access time : TC5562P-45 45ns(MAX.)
  TC5562P-55 55ns(MAX.)
- Low power dissipation : Operation 100mA(MAX.)
  Standby 20mA(MAX.)
- 5V single power supply
- Fully Static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package, 300mil width

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{15}	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{SOLDER}	Soldering Temperature	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−3.0	—	0.8	V

D. C and OPERATING CHARACTERISTICS

($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$	—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$	−8	—	—	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$	8	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0\sim V_{DD}$	—	—	±1.0	μA
I_{DDO}	Operating Current	$V_{DD}=5.5V$, tcycle=Min cycle, $\overline{CE}=V_{IL}$ Other Input=V_{IH}/V_{IL}	—	—	100	mA
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$	—	—	20	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$ Other Input=$V_{DD}-0.2V$ or 0.2V	—	—	2	

CAPACITANCE

($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT}=GND$	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC5562P-45		TC5562P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	45	—	55	—	ns
t_{ACC}	Address Access Time	—	45	—	55	
t_{CO}	Chip Enable Access Time	—	45	—	55	
t_{COE}	Chip Enable to Output in Low-Z	5	—	5	—	
t_{COD}	Chip Disable to Output in High-Z	—	25	—	30	
t_{OH}	Output Data Hold Time	5	—	5	—	

Write Cycle

SYMBOL	PARAMETER	TC5562P-45		TC5562P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	45	—	55	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	
t_{CW}	Chip Enable to End of Write	30	—	35	—	
t_{AS}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{OEW}	$\overline{WE}$ to Output Low-Z	0	—	0	—	
t_{ODW}	$\overline{WE}$ to Output High-Z	—	25	—	30	
t_{DS}	Data Set up Time	30	—	35	—	
t_{DH}	Data Hold Time	0	—	0	—	

A. C. TEST CONDITIONS

Input Pulse Levels	2.4V/0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

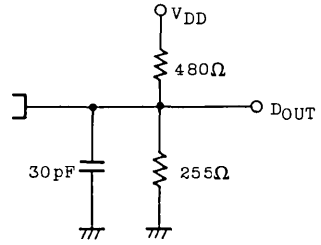
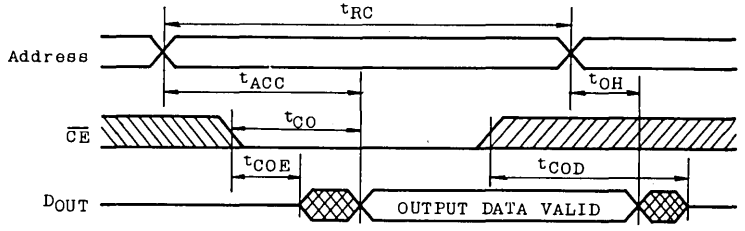


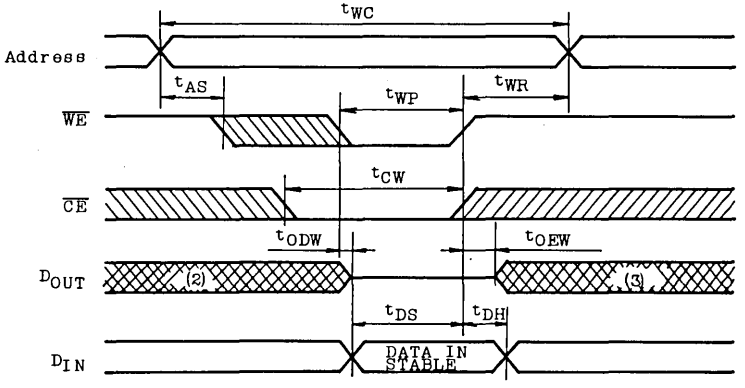
Fig.1 Output Load

TIMING WAVEFORMS

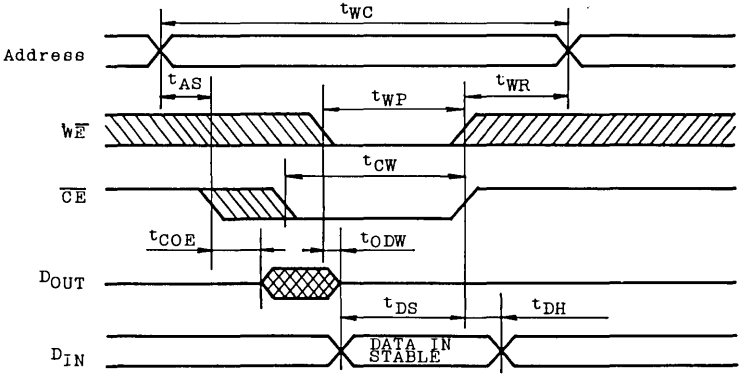
- READ CYCLE (1)



- WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

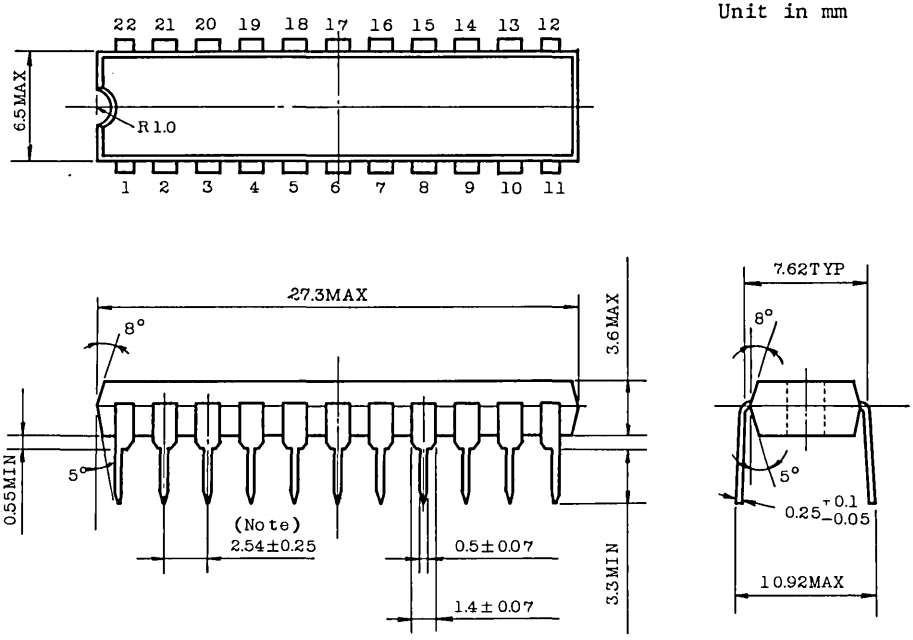


Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The operating temperature(Ta) in guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

16,384 WORD × 4 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC55416P-35
TC55416P-45

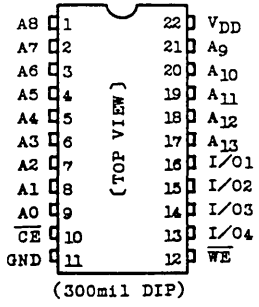
DESCRIPTION

The TC55416P is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns and maximum operating current of 80mA/60mA at minimum cycle time.
The TC55416P also features an automatic stand-by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 10mA.
The TC55416P is suitable for use in cache memory and high speed storage, where high speed/high density are required.
The TC55416P is molded in a 22 pin standard plastic package with 0.3 inch width for high density assembly.
The TC55416P is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

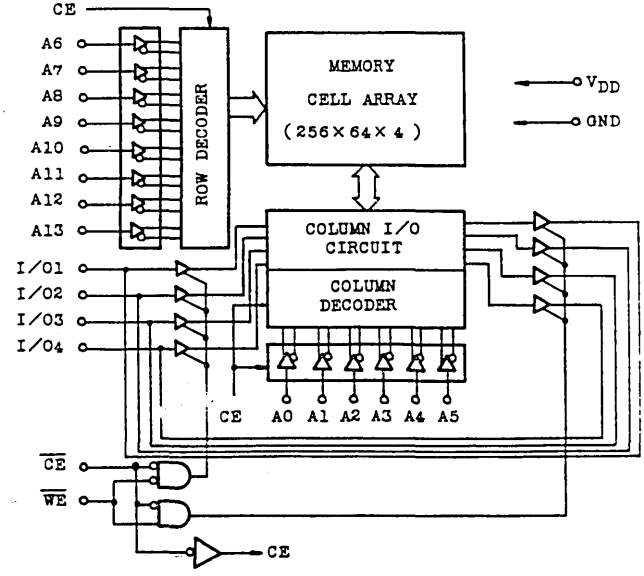
FEATURES

- Fast access time : TC55416P-35 35ns (Max.)
  TC55416P-45 45ns (Max.)
- Low power dissipation : Operation TC55416P-35 80mA (Max.)
  TC55416P-45 60mA (Max.)
  Standby 10mA (Max.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible : All Input and Output
- Package : 22 pins standard plastic package, 300 mil width.

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A13	Address Inputs
I/O1~I/O4	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
V_{OUT}	Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{solder}	Soldering Temperature	260·10	°C·sec
T_{stg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	0~70	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

D.C. and OPERATING CHARACTERISTICS (T_a=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}		-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V		-4	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=0~V_{DD}		-	-	±1.0	μA
I_{DDO}	Operating Current	V_{DD}=5.5V t_{cycle}=Min cycle $\overline{CE}$=V_{IL} Other Input=V_{IH}/V_{IL}	-35	-	-	80	mA
			-45	-	-	60	
I_{DDS1}	Standby Current	V_{DD}=5.5V, t_{cycle}=Min cycle $\overline{CE}$=V_{IH}, Other Input=V_{IH}/V_{IL}		-	-	20	mA
I_{DDS2}		$\overline{CE}$=V_{DD}-0.2V Other Input=V_{DD}-0.2V or 0.2V		-	-	1	

CAPACITANCE (T_a=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55416P-35		TC55416P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	-	45	-	ns
t_{ACC}	Address Access Time	-	35	-	45	ns
t_{CO}	Chip Enable Access Time	-	35	-	45	ns
t_{COE}	Chip Enable to Output in Low-Z	0	-	0	-	ns
t_{COD}	Chip Enable to Output in High-Z	-	15	-	20	ns
t_{OH}	Output Data Hold Time	5	-	5	-	ns

Write Cycle

SYMBOL	PARAMETER	TC55416P-35		TC55416P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	-	45	-	ns
t_{WP}	Write Pulse Width	30	-	35	-	ns
t_{CW}	Chip Enable to End of Write	30	-	35	-	ns
t_{AS}	Address Set Up Time	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{ODW}	$\overline{WE}$ to Output High-Z	-	15	-	15	ns
t_{OEW}	$\overline{WE}$ to Output Low-Z	0	-	0	-	ns
t_{DS}	Data Set Up Time	15	-	20	-	ns
t_{DH}	Data Hold Time	0	-	0	-	ns

A.C. TEST CONDITIONS

Input Pulse Levels	0.6V, 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.8V, 2.0V
Output Load	See Fig.1

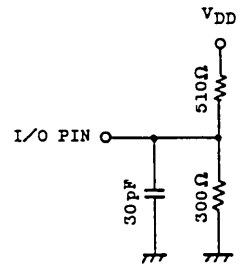
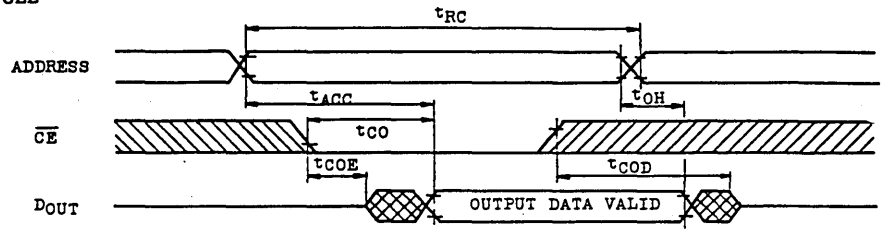


Fig.1 OUTPUT LOAD

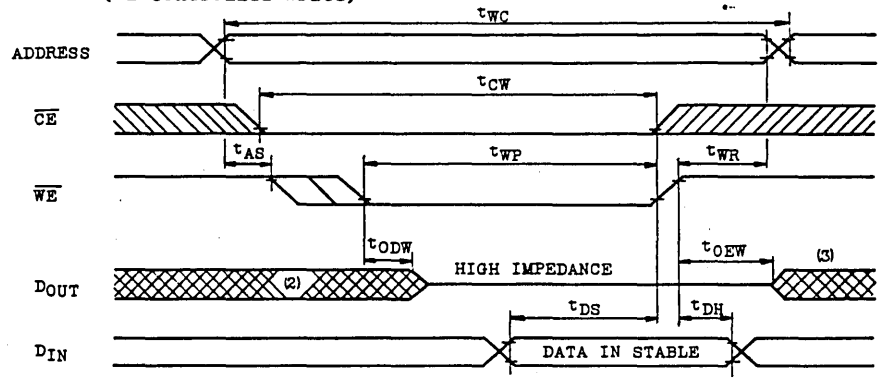
Note: In all condition, t_{COD} max is less than t_{COE} min both for a given device and from device to device.

TIMING WAVEFORMS

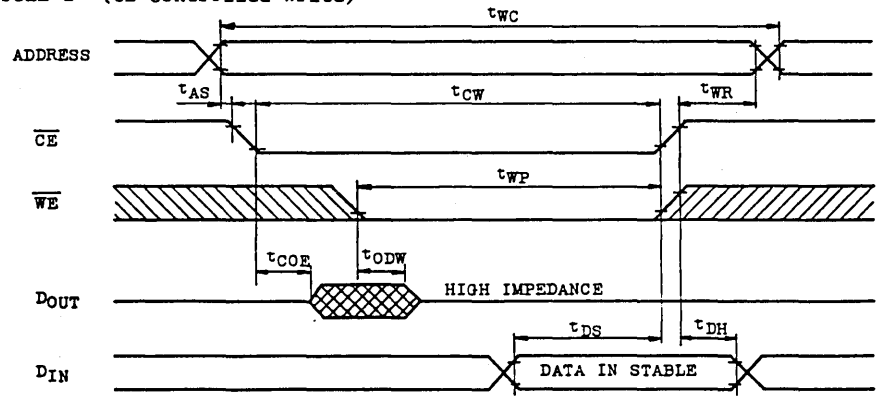
READ CYCLE(1)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



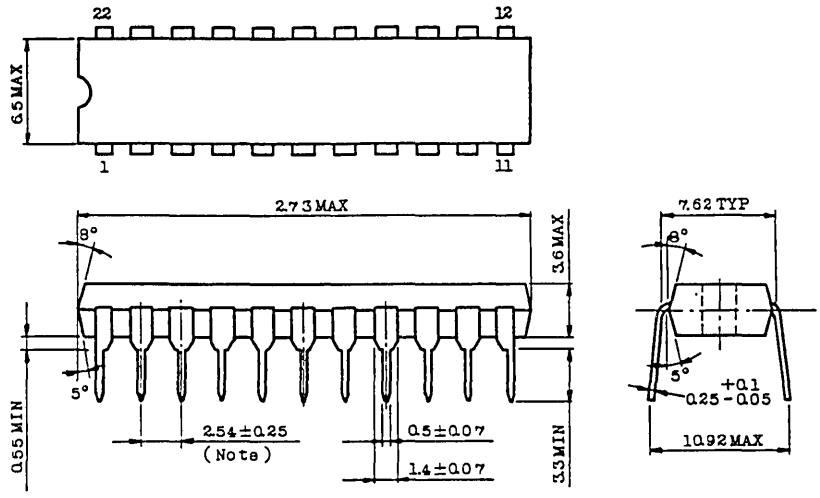
WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

TOSHIBA MOS MEMORY PRODUCT

16,384 WORD × 4 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC55417P-35
TC55417P-45

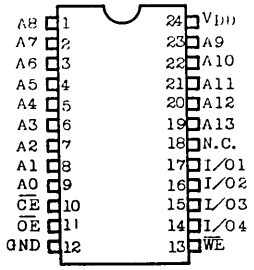
DESCRIPTION

The TC55417P is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns and maximum operating current of 80mA/60mA at minimum cycle time. The TC55417P also features an automatic stand-by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 10mA. The TC55417P is suitable for use in cache memory and high speed storage, where high speed/high density are required. The TC55417P is molded in a 24 pin standard plastic package with 0.3 inch width for high density assembly. The TC55417P is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time : TC55417P-35 35ns (Max.)
  TC55417P-45 45ns (Max.)
- Low power dissipation: Operation TC55417P-35 80mA (Max.)
  TC55417P-45 60mA (Max.)
  Standby 10mA (Max.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible: All Input and Output
- Output buffer control : $\overline{OE}$
- Package : 24 pins standard plastic package, 300 mil width.

PIN CONNECTION

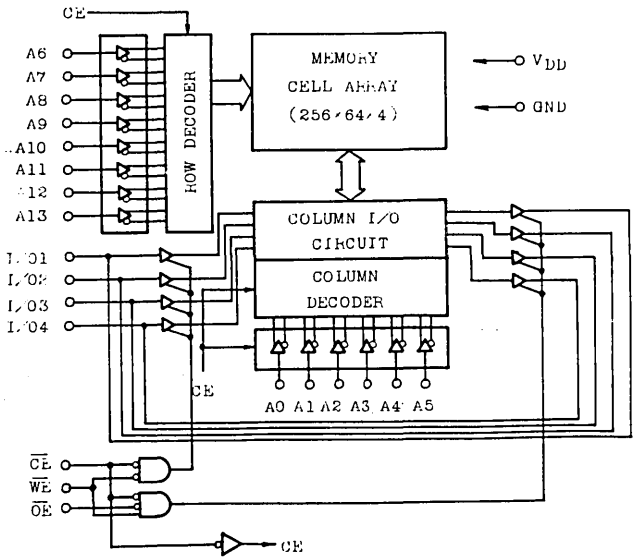


(300mil DIP)

PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ∿ 7.0	V
V_{IN}	Input Voltage	-2.0 ∿ 7.0	V
V_{OUT}	Output Voltage	-0.5 ∿ V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
T_{stg}	Storage Temperature	-65 ∿ 150	°C
T_{opr}	Operating Temperature	0 ∿ 70	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta=0 ∿ 70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0 ∿ V_{DD}		-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V		-4	-	-	mA
I_{OL}	Output low Current	V_{OL}=0.4V		8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=0 ∿ V_{DD}		-	-	±1.0	μA
I_{DDO}	Operating Current	V_{DD}=5.5V tcycle=Min cycle $\overline{CE}$=V_{IL} Other Input=V_{IH}/V_{IL}	-35	-	-	80	mA
			-45	-	-	60	
I_{DDS1}	Standby Current	V_{DD}=5.5V, t_{cycle}=Min cycle $\overline{CE}$=V_{IH}, Other Input=V_{IH}/V_{IL}		-	-	20	mA
I_{DDS2}		$\overline{CE}$=V_{DD}-0.2V Other Input=V_{DD}-0.2V or 0.2V		-	-	1	

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55417P-35		TC55417P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	-	45	-	ns
t_{ACC}	Address Access Time	-	35	-	45	ns
t_{CO}	Chip Enable Access Time	-	35	-	45	ns
t_{OE}	Output Enable to Output Valid	-	20	-	20	ns
t_{COE}	Chip Enable to Output in Low-Z	0	-	0	-	ns
t_{COD}	Chip Enable to Output in High-Z	-	15	-	20	ns
t_{OEE}	Output Enable to Output in Low-Z	0	-	0	-	ns
t_{ODO}	Output Disable to Output in High-Z	-	15	-	15	ns
t_{OH}	Output Data Hold Time	5	-	5	-	ns

Write Cycle

SYMBOL	PARAMETER	TC55417P-35		TC55417P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	-	45	-	ns
t_{WP}	Write Pulse Width	30	-	35	-	ns
t_{CW}	Chip Enable to End of Write	30	-	35	-	ns
t_{AS}	Address Set Up Time	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{ODW}	$\overline{WE}$ to Output High-Z	-	15	-	15	ns
t_{OEW}	$\overline{WE}$ to Output Low-Z	0	-	0	-	ns
t_{DS}	Data Set Up Time	15	-	20	-	ns
t_{DH}	Data Hold Time	0	-	0	-	ns

A.C. TEST CONDITIONS

Input Pulse Levels	0.6V, 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.8V, 2.0V
Output Load	See Fig. 1

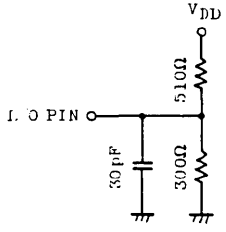
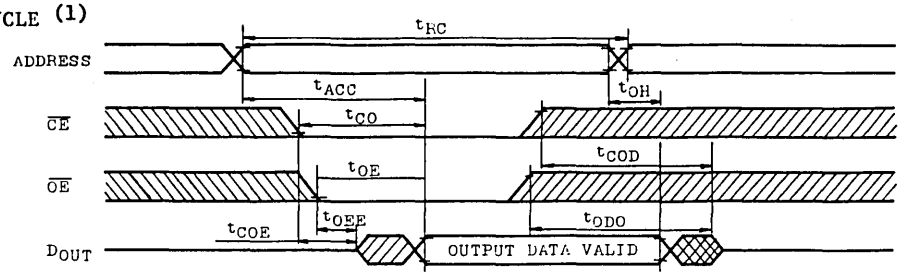


Fig. 1 OUTPUT LOAD

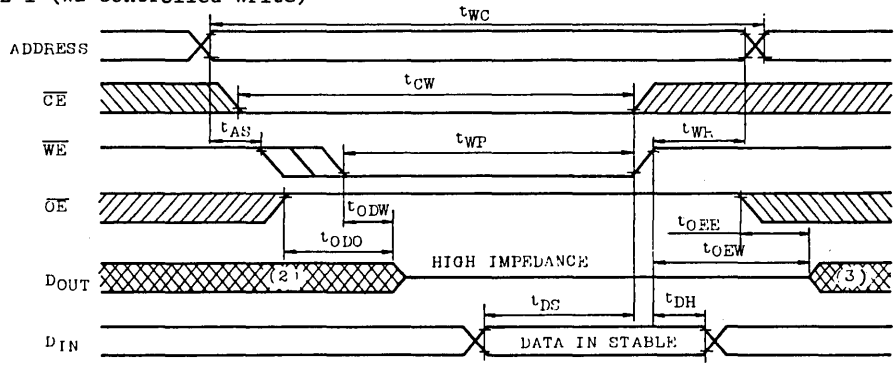
Note: In all condition, t_{COD} max is less than t_{COE} min both for a given device and from device to device.

TIMING WAVEFORMS

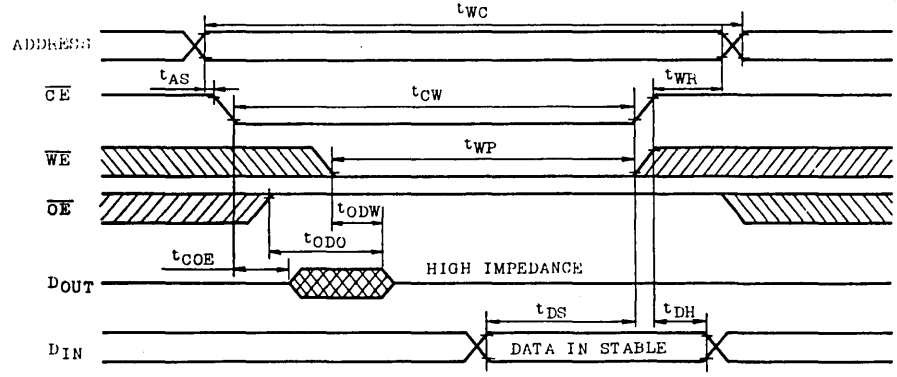
READ CYCLE (1)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



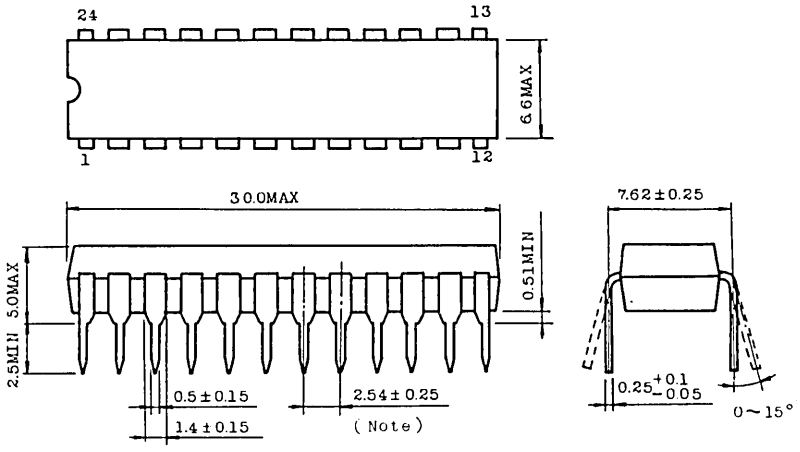
WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)



Note: 1. $\overline{WE}$ is High for Read cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.24 leads.

Erasable/Programmable Read Only Memories

HIGH SPEED PROGRAMMING MODE

FEATURES

The High Speed Programming I or High Speed Programming II Algorithms may be used to program 64K through 512K devices. The 1MEGABIT devices may be programmed using the High Speed Programming II Algorithm.

The High Speed Programming I Algorithm uses 1ms programming pulse and the flow chart is shown in Figure 1.

The High Speed Programming II Algorithm uses 0.1ms programming pulse and the flow chart is shown in Figure 2.

APPLICABLE DEVICES

Device Name		Theoretical Programming Time	
EPROM	One Time PROM	I	II
TMM2764AD/ADI	TMM2464AP/AF	33 sec	0.8 sec
TMM27128AD/ADI	TMM24128AP/AF	66 sec	1.7 sec
TMM27256AD/ADI	TMM24256AP/AF	131 sec	3.3 sec
TC57256AD	TC54256AP/AF	131 sec	3.3 sec
TMM27512D/DI	TMM24512P	262 sec	7.0 sec
TC571000D	TC541000P	N/A	14 sec
TC571001D	TC541001P	N/A	14 sec

IDENTIFICATION MODE

The identification mode allows the reading of an electrical signature from the device that will identify the manufacturer and device type. The identification mode is activated using the following conditions:

1. For the Manufacturer Code:
   Set A9=12V±0.5V, Aϕ=ViL, Other Addresses=ViL
   Note: The manufacturer code is consistent with the E.I.A. standard.
2. For the Device Code:
   Set A9=12V±0.5V, Aϕ=ViH, Other Addresses=ViL.
   Note: The Device Code is manufacturer dependent.

The following table shows the Electrical Signatures of Toshiba devices.

ELECTRICAL DEVICES

Device Name		Signature	
EPROM	One Time PROM	Manufacture Code	Device Code
TMM2764AD/ADI	TMM2464AP/AF	98	52
TMM27128AD/ADI	TMM24128AP/AF	98	D3
TMM27256AD/ADI	TMM24256AP/AF	98	54
TC57256AD	TC54256AP/AF	98	C4
TMM27512D/DI	TMM24512P	98	15
TC571000D	TC541000P	98	86
TC571001D	TC541001P	98	07

Figure 1

HIGH SPEED PROGRAM I FLOW CHART

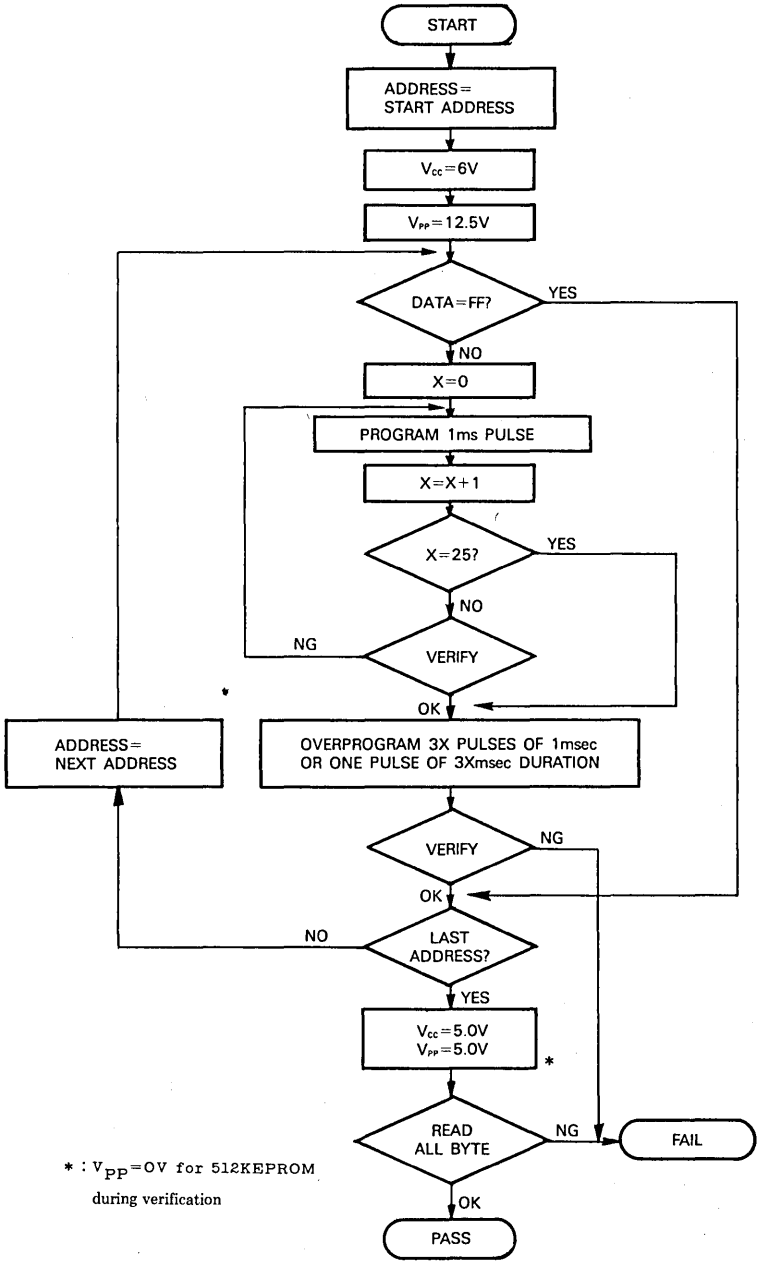
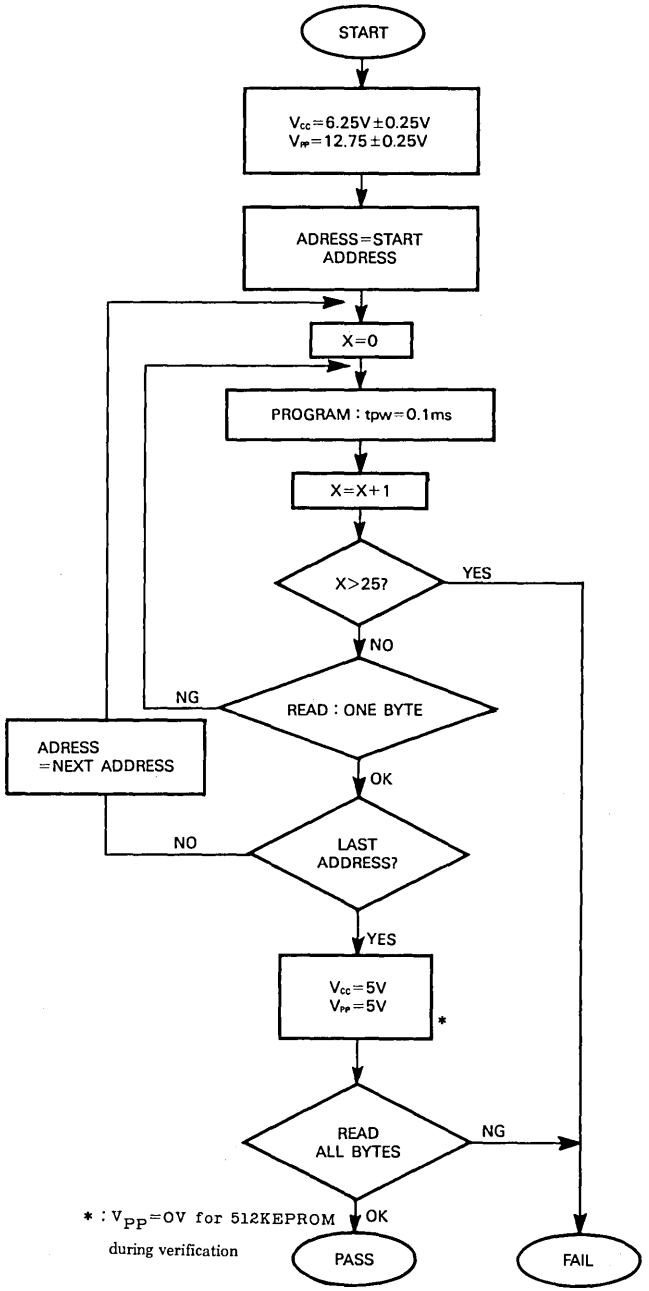


Figure 2

HIGH SPEED PROGRAM II FLOW CHART



TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

TMM2764AD-15, TMM2764AD-150
TMM2764AD-20, TMM2764AD-200

DESCRIPTION

The TMM2764AD is a 8192 word×8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764AD's access time is 150ns/200ns, and the TMM2764AD operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.
For program operation, the programming is achieved by using the high speed programming mode.

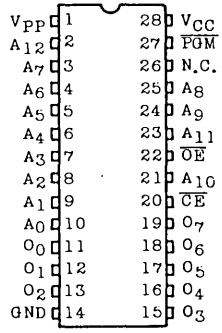
The TMM2764AD is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

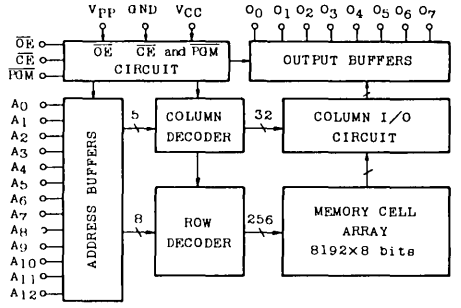
	−15	−20	−150	−200
V_{CC}	5V±5%		5V±10%	
t_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA		120mA	
I_{CC1}	30mA		35mA	

- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764 A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N. C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	PGM (27)	CE (20)	OE (22)	VPP (1)	VCC (28)	O0~O7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG.}$	Storage Temperature	−65~125	°C
$T_{OPR.}$	Operating Temperature	0~70	°C

READ OPERATION

D. C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM2764AD-15/20	TMM2764AD-150/200
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}±0.6V	2.0~V_{CC}+0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}		—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	−15/20	—	—	30	mA
			−150/200	—	—	35	
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	−15/20	—	—	100	mA
			−150/200	—	—	120	
V_{IH}	Input High Voltage	—		2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—		−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA		2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6		—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM2764AD-15/150		TMM2764AD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

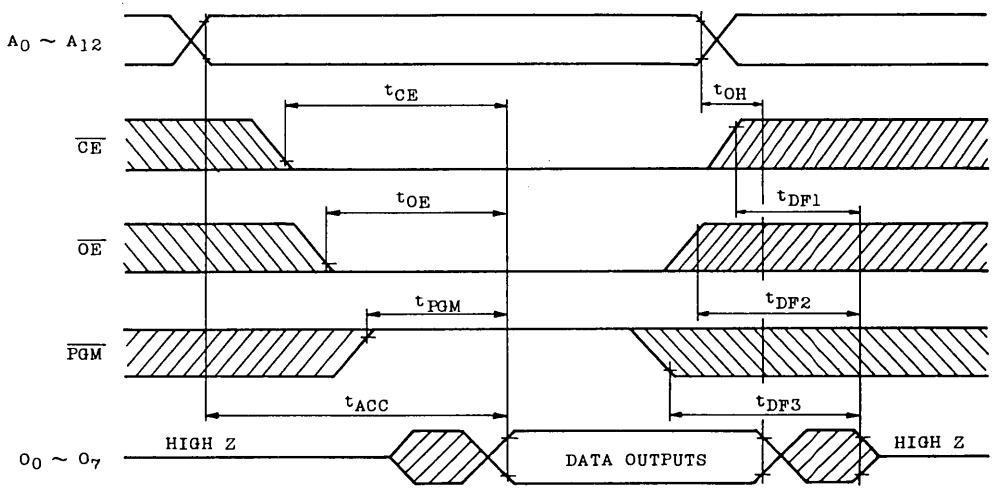
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25C°, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=OV.	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=OV	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

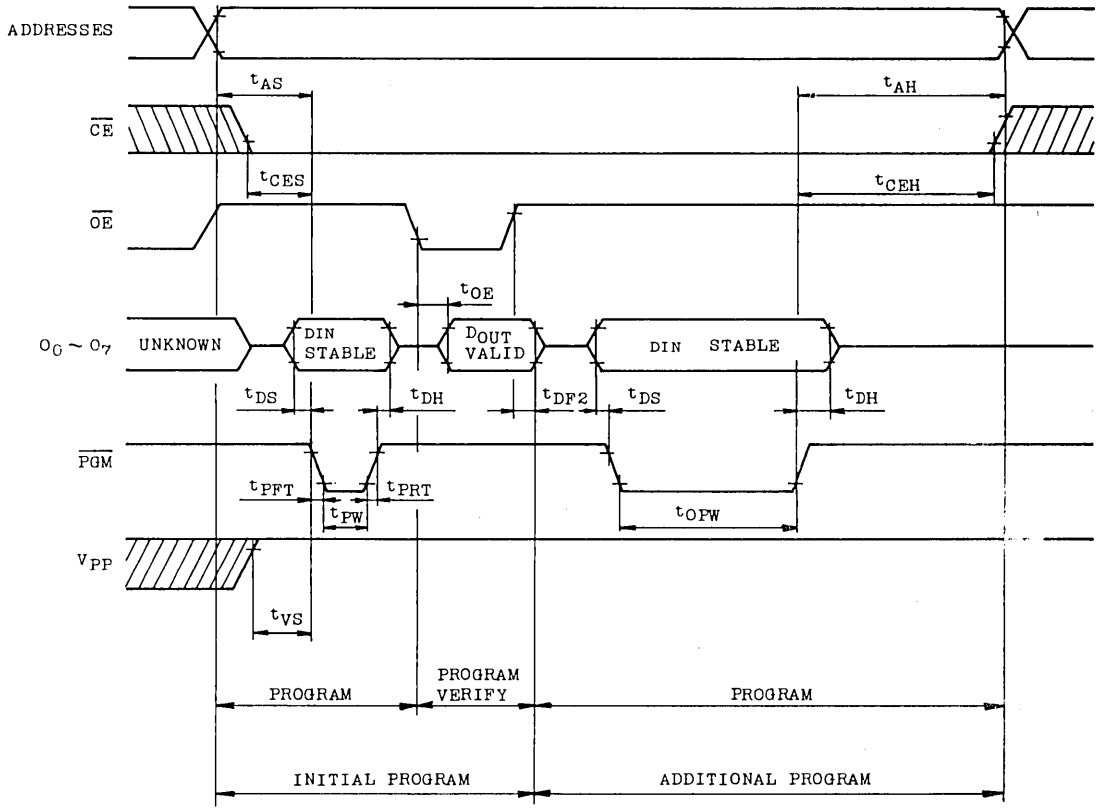
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	—	78.75	ms
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. Test Conditions

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45 to 2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

Note : 1. t_{opw} depeds on the program pulse width which is required in the initial Program.

TIMING WAVEFORMS (PROGRAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM2764AD's erasure is achieved by applying shortwave ultraviolet light which has a wave length of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (Ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM2764AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM2764AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL

		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IL}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM2764AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM2764AD can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2764AD has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM2764AD is placed in the standby mode which reduce 70% of the operating current and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764AD are in the "1" state which is erased state.

Therefore the program operation is to introduce "Os" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL.

The TMM2764AD can be programmed any location at anytime——either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2764AD from being programmed.

Programming of two or more TMM2764AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage(+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$ = V_{IH}.

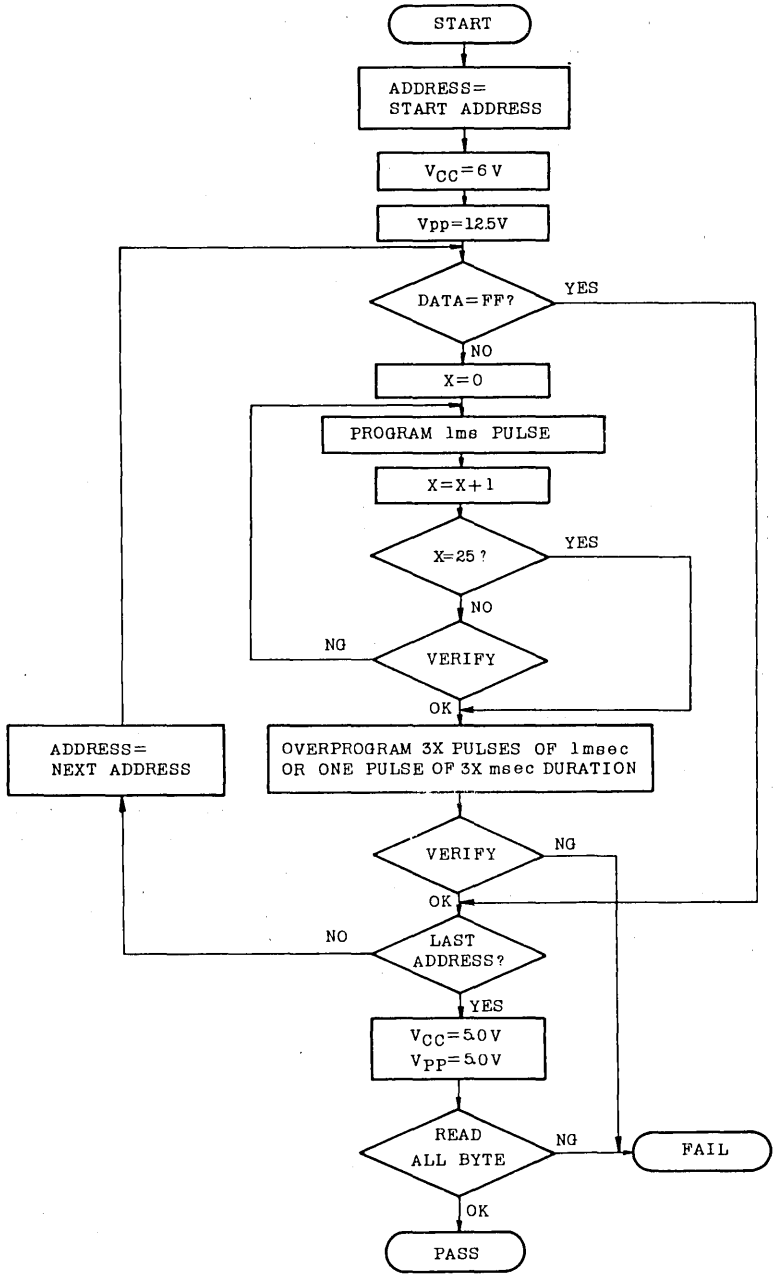
The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max.25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP} =5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM2764AD which identifies its manufacture and device type.

The programming equipent may read out manufacurer code and device code from TMM2764AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

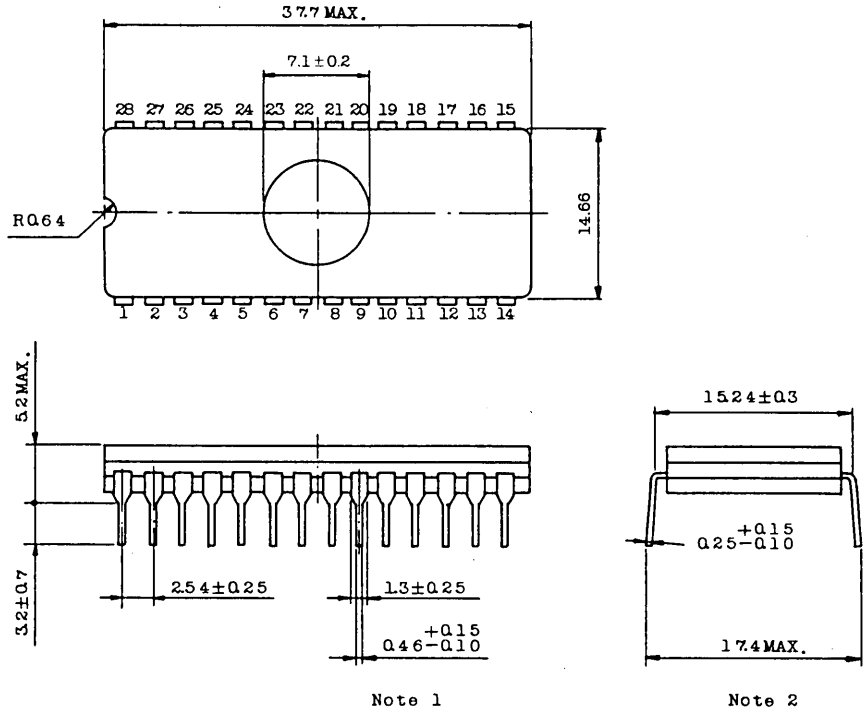
The following table shows electric signature of TMM2764AD.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	0	1	0	52

Notes : A9 = 12V±0.5V
$\overline{A1}$~$\overline{A8}$, A10~A12, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT UV ERASABLE AND
ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

TMM2764ADI-15
TMM2764ADI-20

DESCRIPTION

The TMM2764ADI is a 8192 word × 8bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764AD's access time is 150/200ns and the TMM2764ADI operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the programming is achieved by using the high speed programming mode.

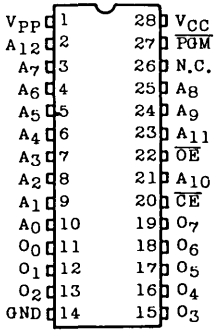
The TMM2764ADI is fabricated with the Nchannel silicon double layer gate MOS technology.

FEATURES

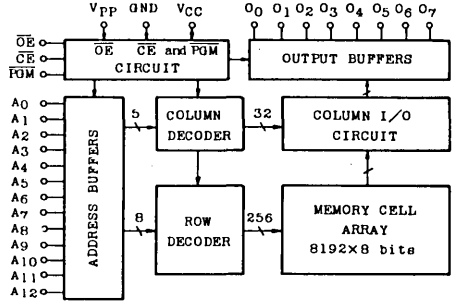
	−15	−20
V_{CC}	5V±5%	
t_{ACC}	150ns	200ns
I_{CC2}	100mA	
I_{CC1}	30mA	

- Wide operating temparature range −40~85°C
- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764 A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N. C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG.}$	Storage Temperature	−65~125	°C
$T_{OPR.}$	Operating Temperature	−40~85	°C

READ OPERATION

D. C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM2764ADI-15/20
Ta	Operating Temperature	−40~85°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%
V_{PP}	V_{PP} Power Supply Voltage	2.2~V_{CC}±0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	—	—	+10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	35	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	120	mA
V_{IH}	Input High Voltage	—	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—	−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM2764ADI-15		TMM2764ADI-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

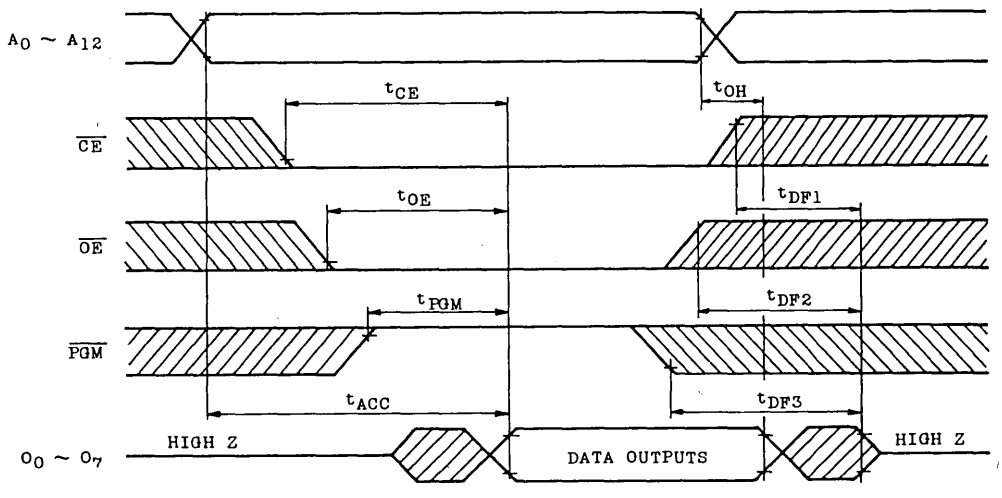
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta = 25C°, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$.	—	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

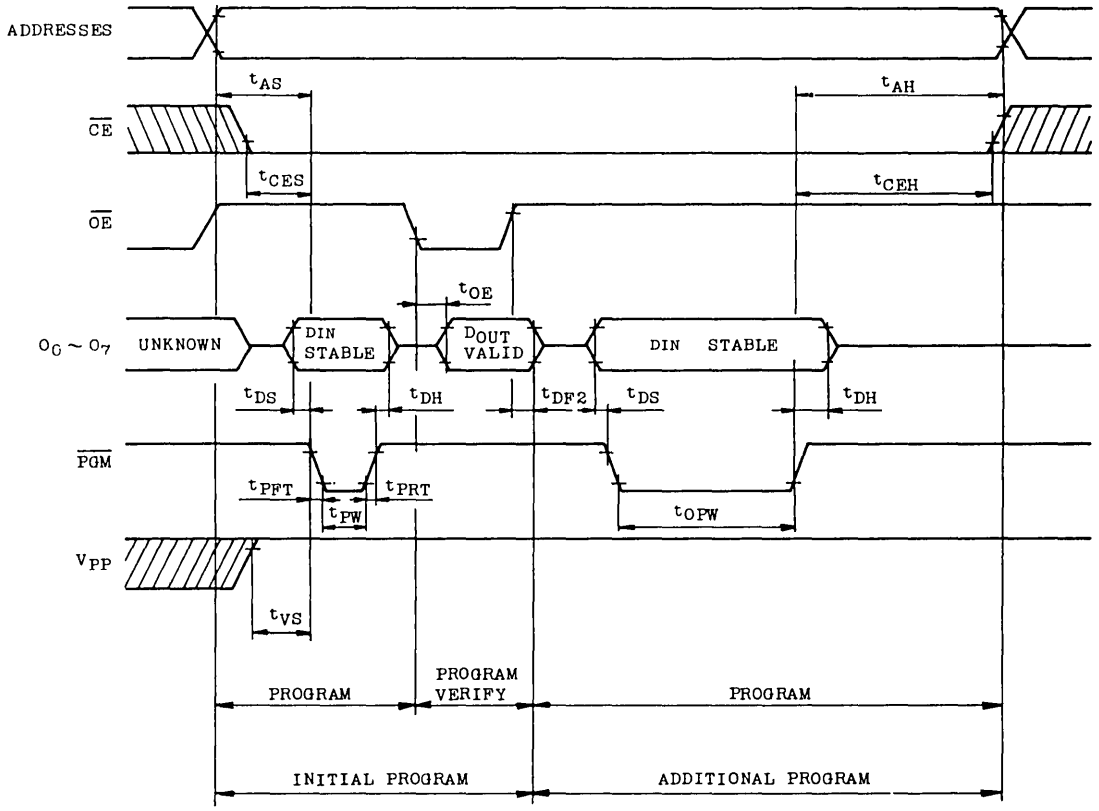
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	—	78.75	ms
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. Test Conditions

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

Note : 1. t_{opw} depeds on the program pulse width which is required in the initial Program

TIMING WAVEFORMS (PROGRAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V

ERASURE CHARACTERISTICS

The TMM2764ADI's erasure is achieved by applying shortwave ultraviolet light which has a wave length of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (Ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM2764ADI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM 2764ADI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES (NOMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=−40~85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IL}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM2764ADI has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM2764ADI can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2764ADI has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM2764ADI is placed in the standby mode which reduce 70% of the operating current and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764ADI are in the "1" state which is erased state. The programming operation is introduces "Os" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL.

The TMM2764ADI can be programmed any location at anytime — either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2764ADI from being programmed.

Programming of two or more TMM2764ADI's in parallel with different data is easlly accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage(+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$ =V_{IH}.

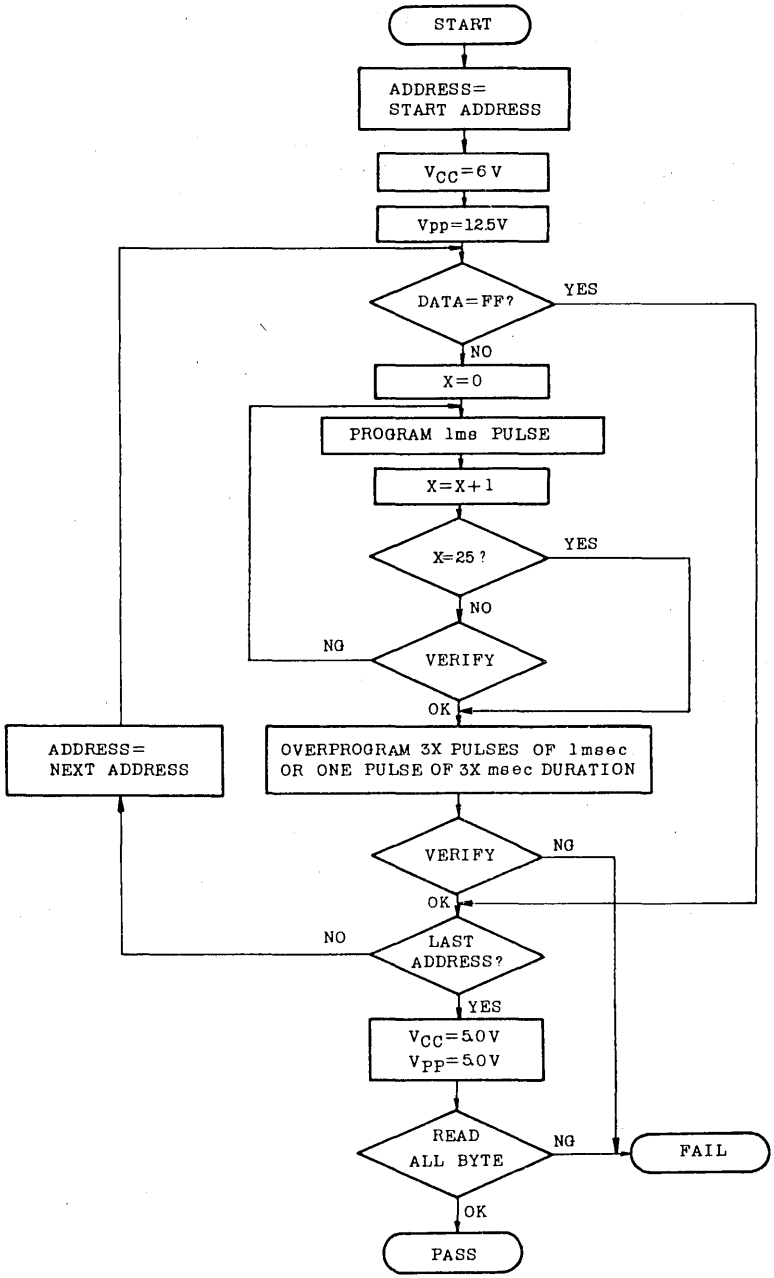
The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max.25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP} =5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM2764ADI which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM2764ADI by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output under these conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

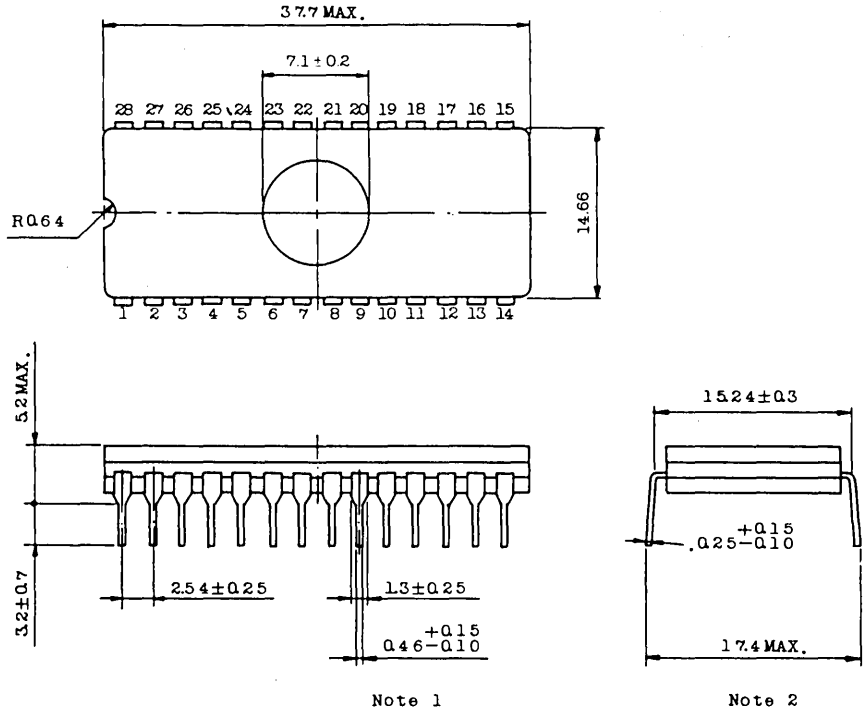
The following table shows electric signature of the TMM2764ADI.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	0	1	0	52

Notes : A9 = 12V±0.5V
A1~A8, A10~A12, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCT

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

TMM27128AD-15, TMM27128AD-150
TMM27128AD 20, TMM27128AD-200

DESCRIPTION

The TMM27128AD is a 16,384 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM 27128AD's access time is 150ns/200ns, and the TMM27128AD operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the program is achieved by using the high speed programming mode.

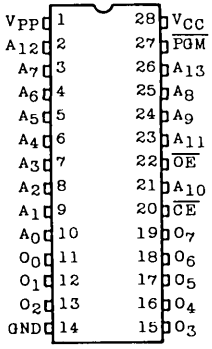
The TMM27128AD is fabricated with the N-channel silicon double layer gate MOS technolgy.

FEATURES

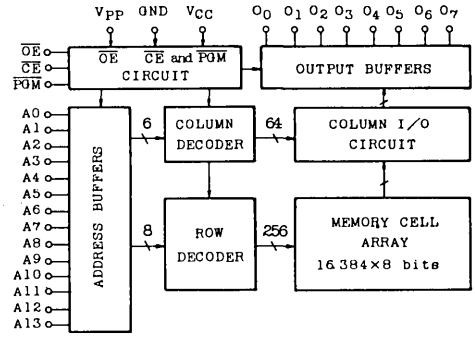
	−15	−20	−150	−200
V_{CC}	5V±5%		5V±10%	
t_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA		120mA	
I_{CC1}	30mA		35mA	

- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{13}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STRG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27128AD-15/20	TMM27128AD-150/200
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}±0.6V	2.0~V_{CC}+0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}		—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	−15/20	—	—	30	mA
			−150/200	—	—	35	
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	−15/20	—	—	100	mA
			−150/200	—	—	120	
V_{IH}	Input High Voltage	—		2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—		−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA		2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6		—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27128AD-15/150		TMM27128AD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

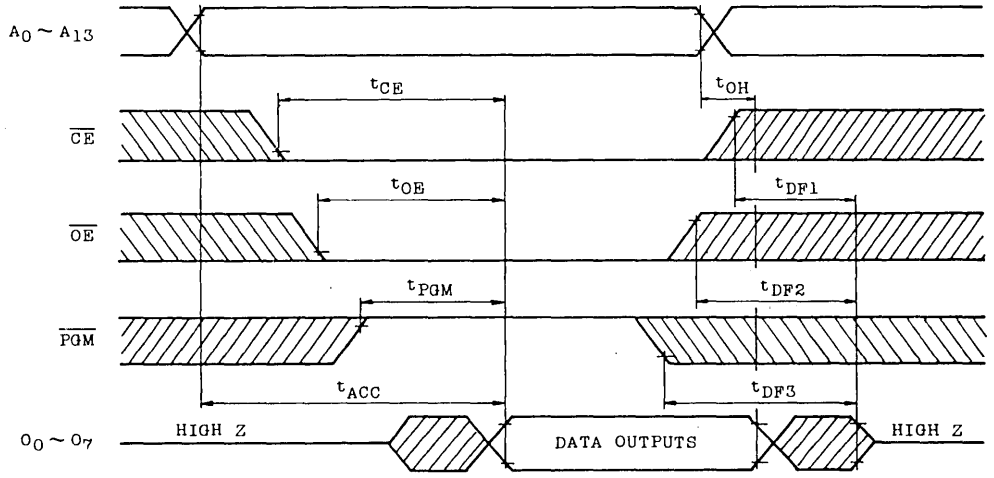
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=0V$	—	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	—	8	12	pF

* This paramater is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Outpu Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

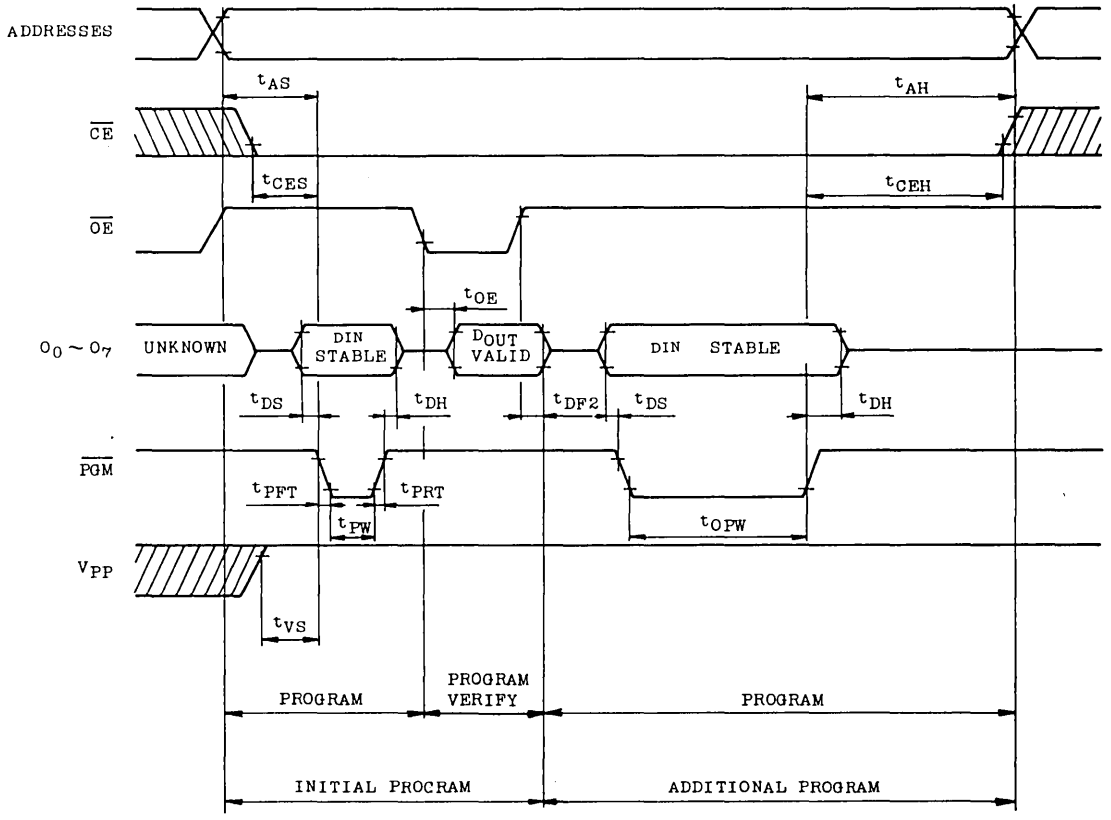
A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3	78.75	ms
t_{PRT}	Program pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output is High-Z	$\overline{CE}$=V_{IL}	—	—	90	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

TIMING WAVEFORMS (READ)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM27128AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) through the chips transparent window.

The integrated dose (ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W.sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27128AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27128AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES (NUMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27128AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in high impedance state.

Thus, two or more TMM27128AD's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27128AD has a low power standby mode conntrolled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM27128AD is placed in the standby mode which reduces 70% of operating current. The outputs are in a high impedence state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128AD are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The levels required for all inputs are TTL.

The TMM27128AD can be programmed at any location, anytime — either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM27128AD from being programmed.

Programming of two or more TMM27128AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$=V_{IH}.

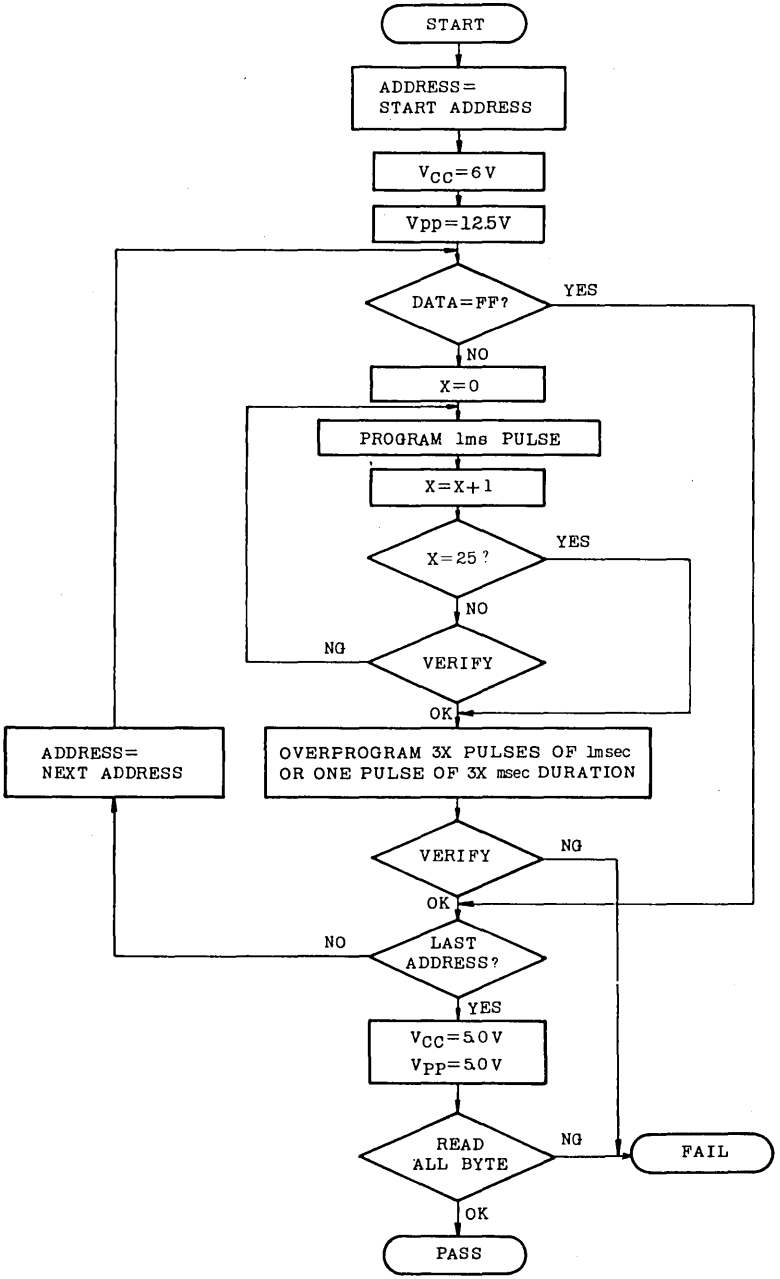
The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27128AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM2764AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output is this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

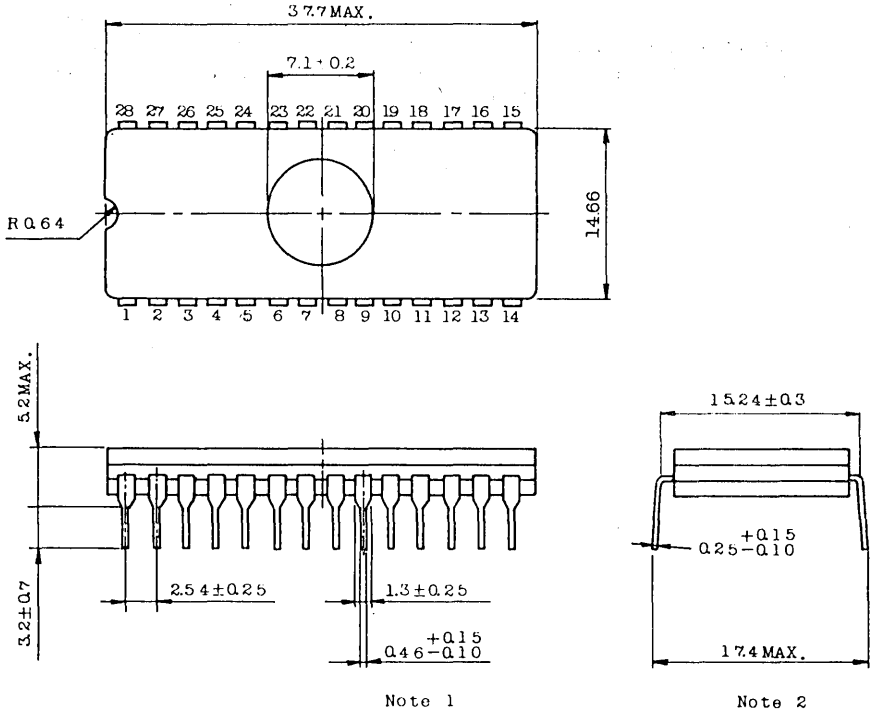
The following table shows electric signature of the TMM27128AD.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	1	0	0	1	1	D3

Notes : A9 = 12V±0.5V
A1~A8, A10~A13, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note 1 Note 2

Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

TOSHIBA MOS MEMORY PRODUCT

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

TMM27128ADI-15
TMM27128ADI-20

DESCRIPTION

The TMM27128ADI is a 16,384 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM 27128ADI's access time is 150ns/200ns, and the TMM27128ADI operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the program is achieved by using the high speed programming mode.

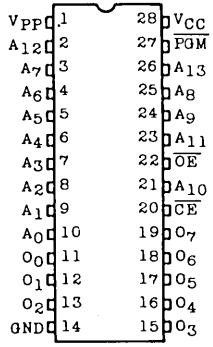
The TMM27128ADI is fabricated with the N-channel silicon double layer gate MOS technolgy.

FEATURES

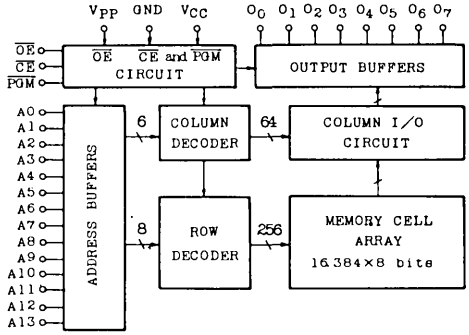
	−15	−20
V_{CC}	5V±5%	
t_{ACC}	150ns	200ns
I_{CC2}	100mA	
I_{CC1}	30mA	

- Wide operating temparature range −40~85°C
- Full static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{13}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STRG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	−40~85	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27128ADI-15/20
Ta	Operating Temperature	−40~85°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}±0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	35	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	120	mA
V_{IH}	Input High Voltage	—	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—	−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27128ADI-15		TMM27128ADI-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

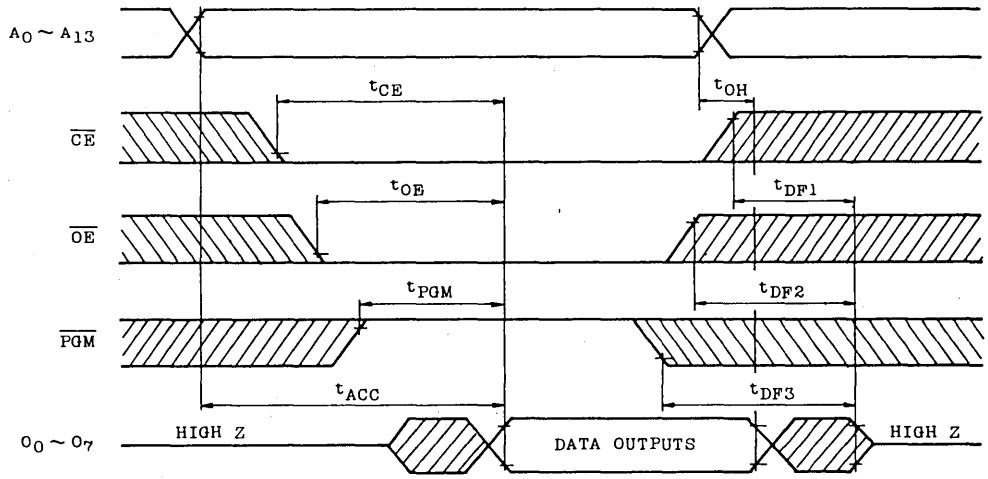
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	—	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	—	8	12	pF

* This paramater is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

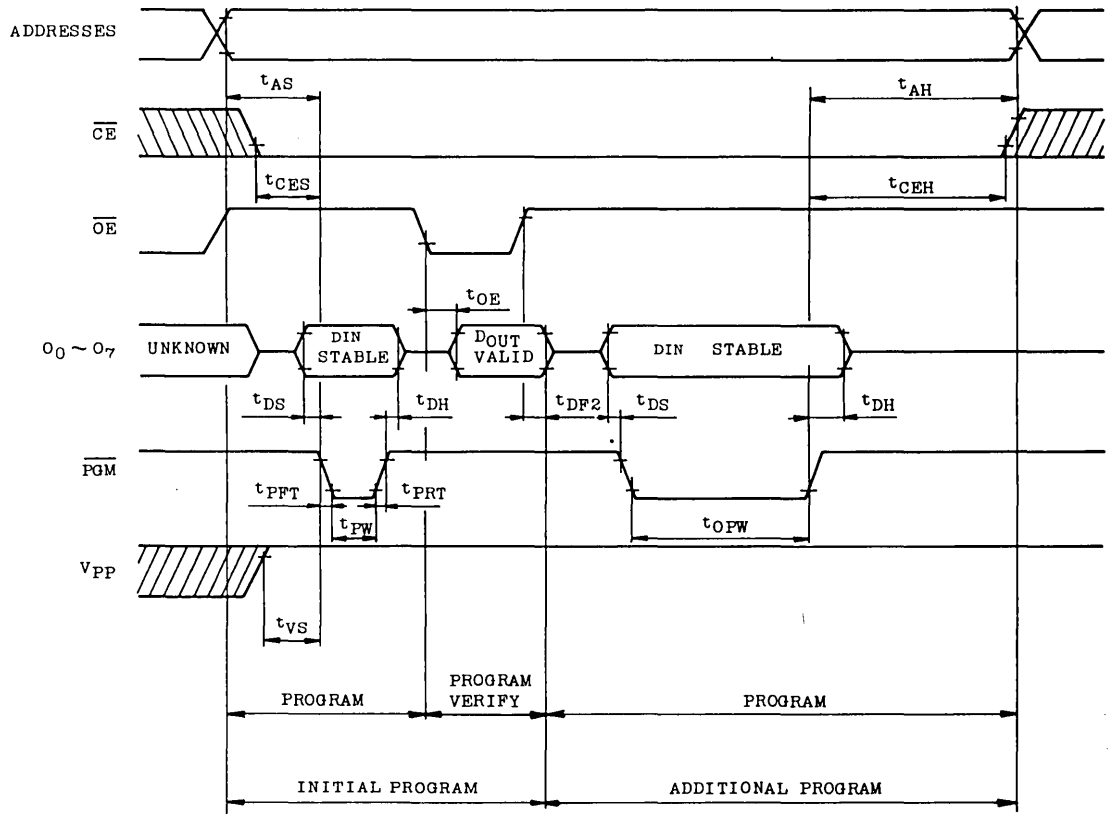
($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3	78.75	ms
t_{PRT}	Program pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output is High-Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

TIMING WAVEFORMS (READ)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM27128ADI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) of the chip through the transparent window.

The integrated dose (ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W.sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27128ADI's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27128ADI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAME (MODE)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=−40~85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IH}, L : : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27128ADI has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in high impedance state.

So two or more TMM27128ADI's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27128ADI has a low power standby mode conntrolled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM27128ADI is placed in the standby mode which reduces 70% of operating current. The outputs are then in a high impedence state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128ADI are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The levels required for all inputs are TTL.

The TMM27128ADI can be programmed at any location, anytime — either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM27128ADI from being programmed.

Programming of two or more TMM27128ADI's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$ and $\overline{PGM}=V_{IH}$.

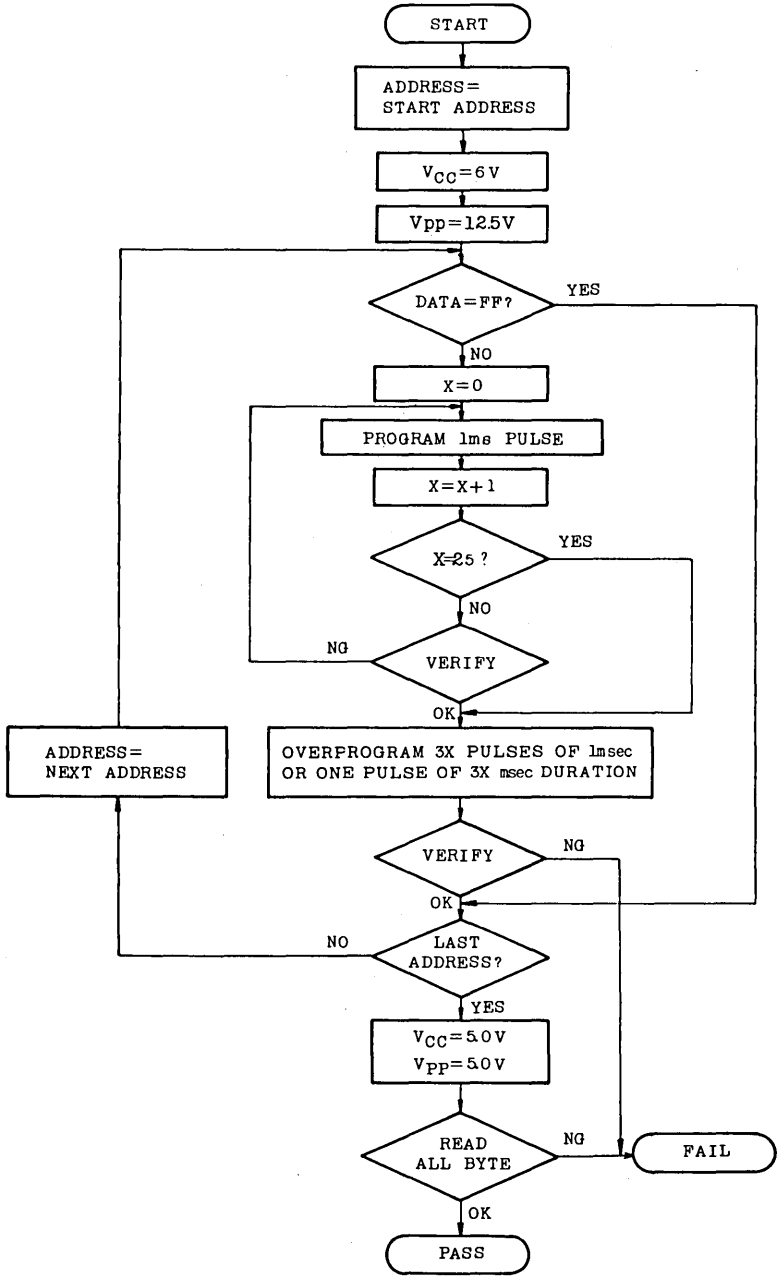
The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27128ADI which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM27128ADI by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output is this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

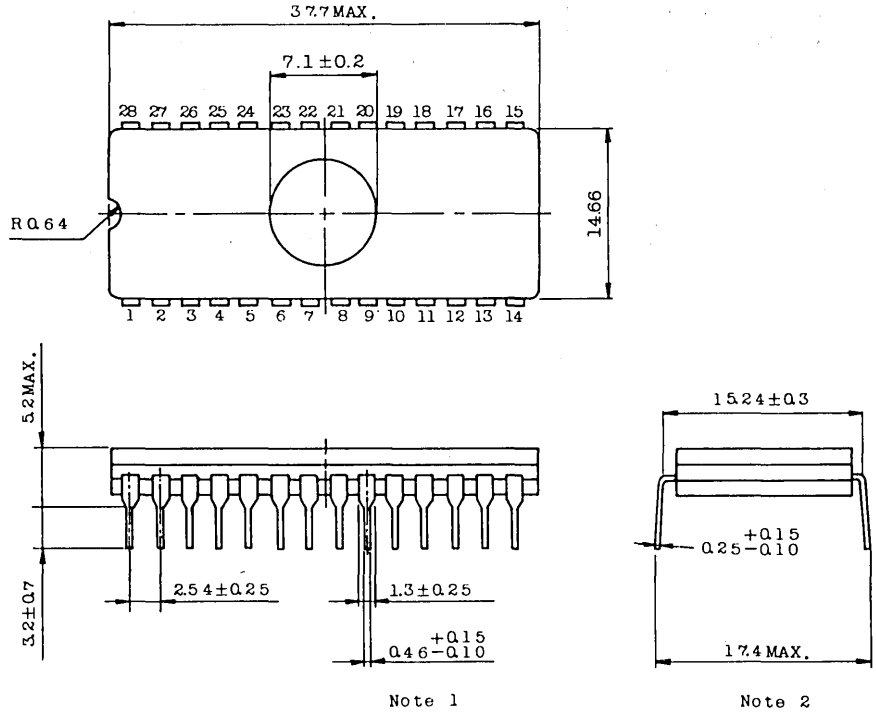
The following table shows electric signature of TMM27128ADI.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	1	0	0	1	1	D3

Notes : A9 = 12V±0.5V
A1 ~ A8, A10 ~ A13, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

TOSHIBA MOS MEMORY PRODUCT

32,768 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM27256AD-15, TMM27256AD-150
TMM27256AD-20, TMM27256AD-200

DESCRIPTION

The TMM27256AD is a 32,768 word × 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27256AD's access time is 150ns/200ns, and the TMM27256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the programming is achieved by using the high speed programming mode.

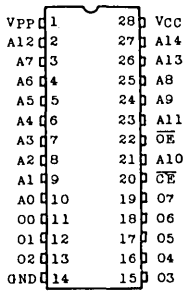
The TMM27256AD is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

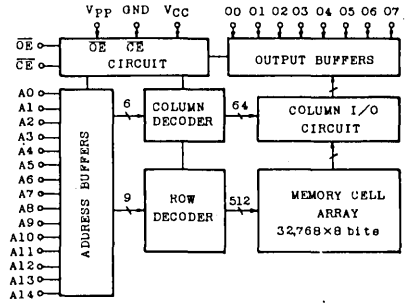
	−15	−20	−150	−200
V_{CC}	5V±5%		5V±10%	
t_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA		120mA	
I_{CC1}	30mA		35mA	

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i 27256
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	*			High Impedance	
Program Verify	*	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27256AD-15/20	TMM27256AD-150/200
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}±0.6V	2.0~V_{CC}+0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}		—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	−15/20	—	—	30	mA
			−150/200	—	—	35	
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	−15/20	—	—	100	mA
			−150/200	—	—	120	
V_{IH}	Input High Voltage	—		2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—		−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA		2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6		—	—	±10	μA

A.C. CHARACTERISTICS

(Ta=0~70°C, V_{CC}=5V±5%, V_{PP}=2.0V~V_{CC}+0.6V)

	PARAMETER	TEST CONDITION	TMM27256AD-15/150		TMM27256AD-20/200		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	0	—	ns

A. C. Test Conditions

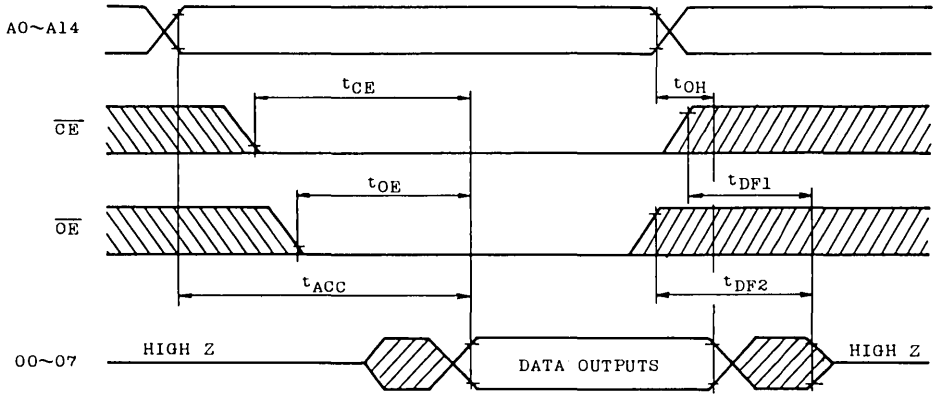
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	—	—	50	mA

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	ns
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $OE=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	—	—	150	ns
t_{DFF}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	—	—	130	ns

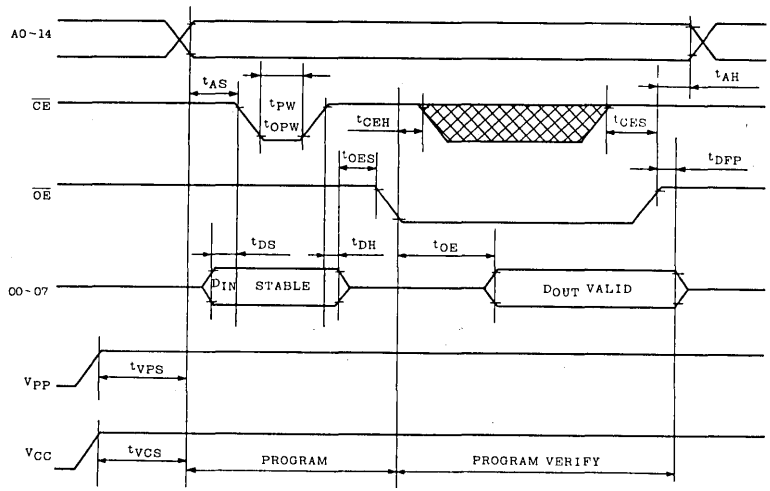
A C Test Conditions

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM27256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) through the chips transparent window.

The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27256AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5 V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	*	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27256AD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$.the outputs will be in a high impedance state.

So two or more TMM27256AD's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27256AD has a low power standby mode conntrolled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27256AD is placed in standby mode which reduces the operating current by 70%. The outputs are then in a high impedence state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256AD are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The TMM27256AD is in the programming mode when the V input is at 12.5V and $\overline{CE}$ is at TTL-Low with $\overline{OE}=V_{IH}$.

The TMM27256AD can be programmed at any location, anytime — either individually, sequentially or at randomly.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ of V_{IL} and $\overline{CE}$ V_{IH} or V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TMM27256AD from being programmed.

Programming of two or more TMM27256ADs in parallel with different data is easily accomplished. That is , all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

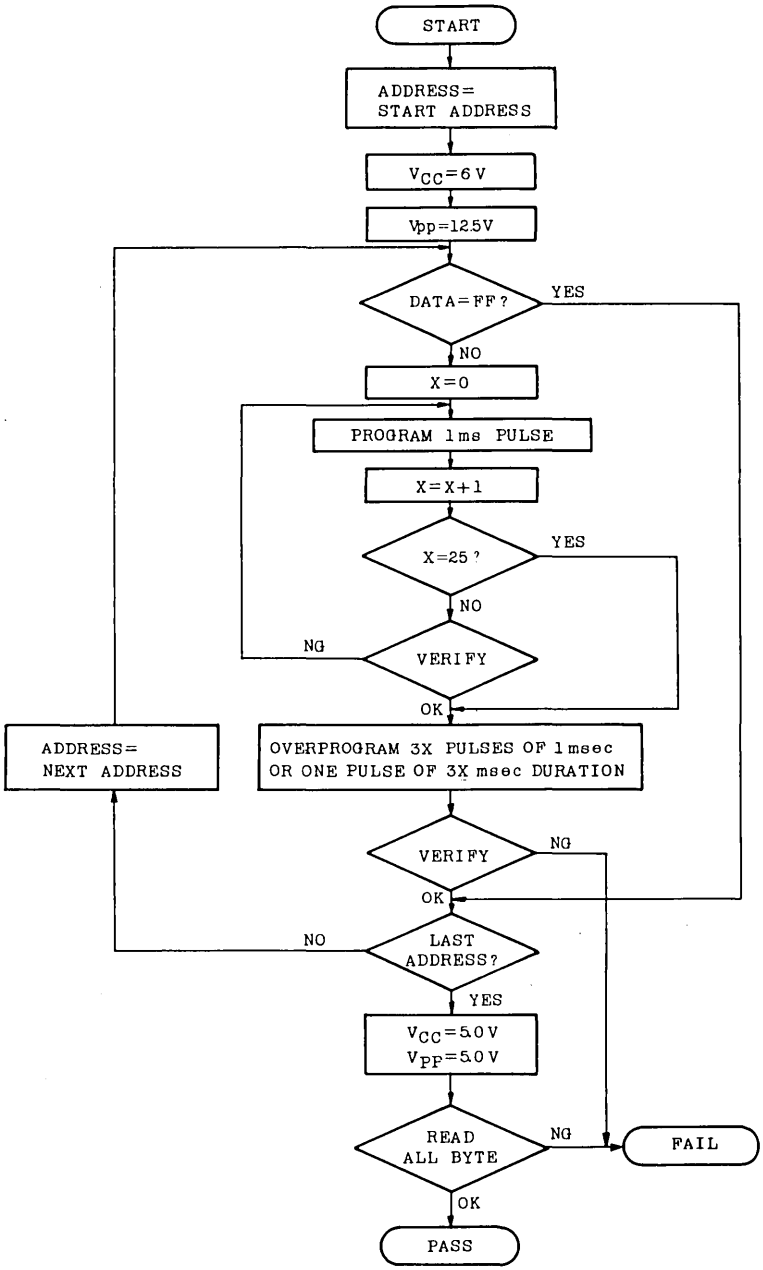
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27256AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM27256AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

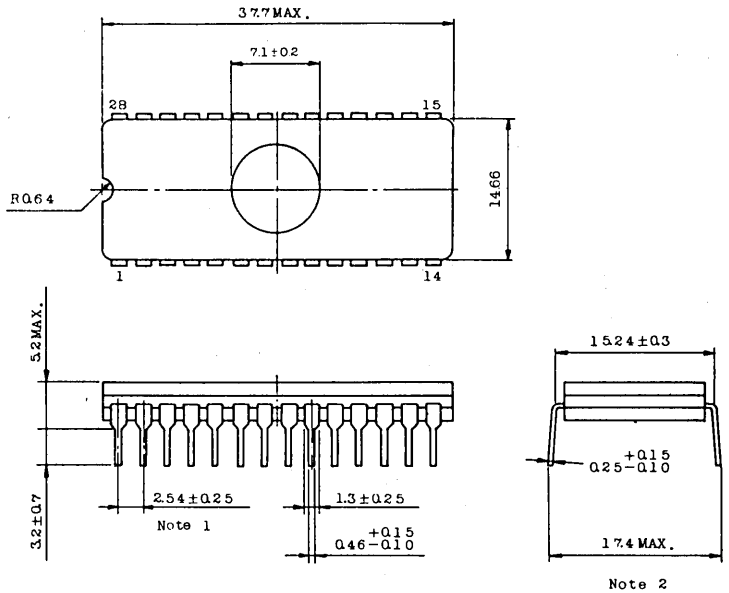
The following table shows electric signature of the TMM27256AD.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

Notes : $A_9 = 12V \pm 0.5V$
A_1-A_8, A_{10}-A_{14}, $\overline{CE}$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCT

32,768 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM27256ADI-15
TMM27256ADI-20

DESCRIPTION

The TMM27256ADI is a 32,768 word × 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, The TMM27256ADI's access time is 150ns/200ns, and the TMM27256ADI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the programming is achieved by using the high speed programming mode.

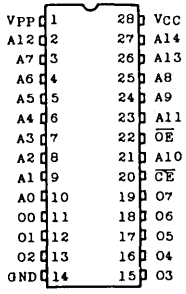
The TMM27256ADI is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

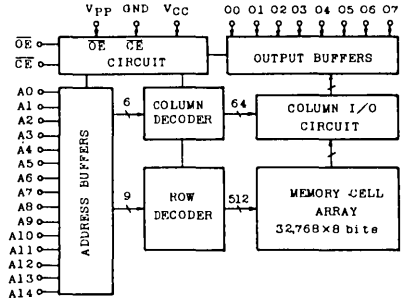
	−15	−20
V_{CC}	5V±5%	
t_{ACC}	150ns	200ns
I_{CC2}	100mA	
I_{CC1}	30mA	

- Wide operating temparature range −40~85°C
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27256
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	*			High Impedance	
Program Verify	*	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	−40~85°C	°C

READ OPERATION

D. C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27256ADI-15/20
Ta	Operating Temperature	−40~85°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%
V_{PP}	V_{PP} Power Supply Voltage	2.2~V_{CC}±0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	35	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	120	mA
V_{IH}	Input High Voltage	—	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—	−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	—	—	±10	μA

A.C. CHARACTERISTICS

($Ta=-40\sim85°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=2.0V\sim V_{CC}+0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	TMM27256AD-15		TMM27256AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$ = $\overline{OE}$=V_{IL}	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	0	—	ns

A C Test Conditions

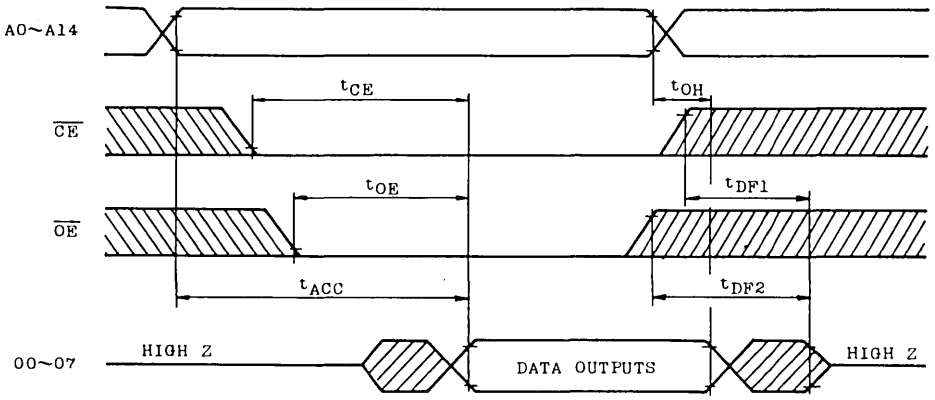
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	—	—	50	mA

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	ns
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $OE=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	—	—	150	ns
t_{DFF}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	—	—	130	ns

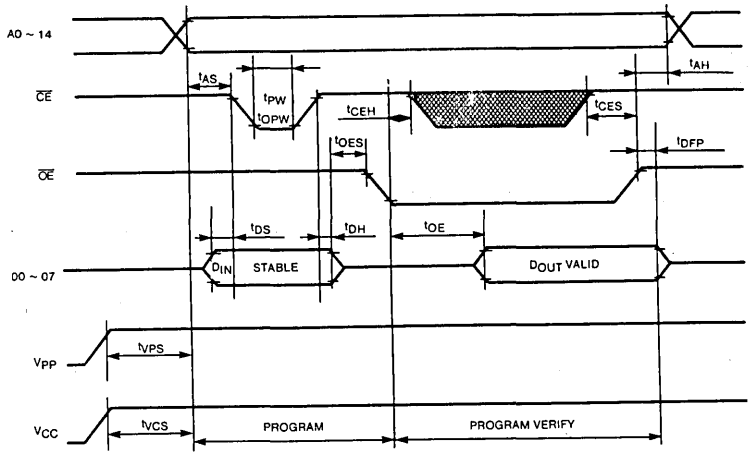
A C Test Conditions

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V

ERASURE CHARACTERISTICS

The TMM27256ADI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) of the chip through the transparent window.

The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps with an ultraviolet light intensity of 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27256ADI's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Both Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27256ADI's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read Operation (Ta=−40~85°C)	Read	L	L	5 V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	*	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27256ADI has two control functions.

The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after the address access time from stabilizing of all addressess.

The $\overline{CE}$ to output valid (t_{CE}) time is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{CE}$.

OUTPUT DESELECT MODE

With $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, outputs will be in high impedance state.

Therefore two or more TMM27256ADI's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27256ADI has a low power standby mode conntrolled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27256ADI is placed in the standby mode which reduces 70% of operating current by applying TTL-high level (V_{CC}). The outputs are in a high impedence state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256ADI are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The TMM27256ADI is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$.

The TMM27256ADI can be programmed at any location, anytime — either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ of V_{IL} and $\overline{CE}$ V_{IH} or V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TMM27256ADI from being programmed.

Programming of two or more TMM27256ADI's in parallel with different data is easily accomplished. That is , all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

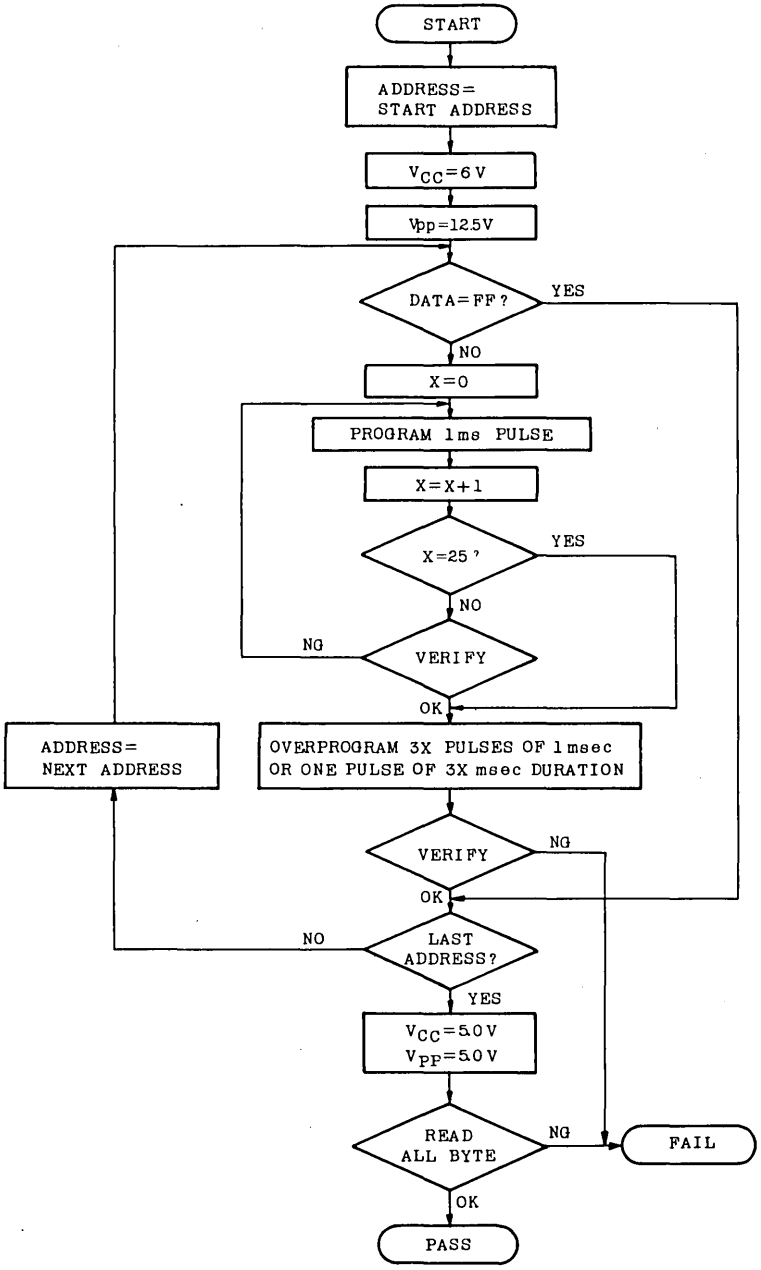
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27256ADI which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM27256ADI by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

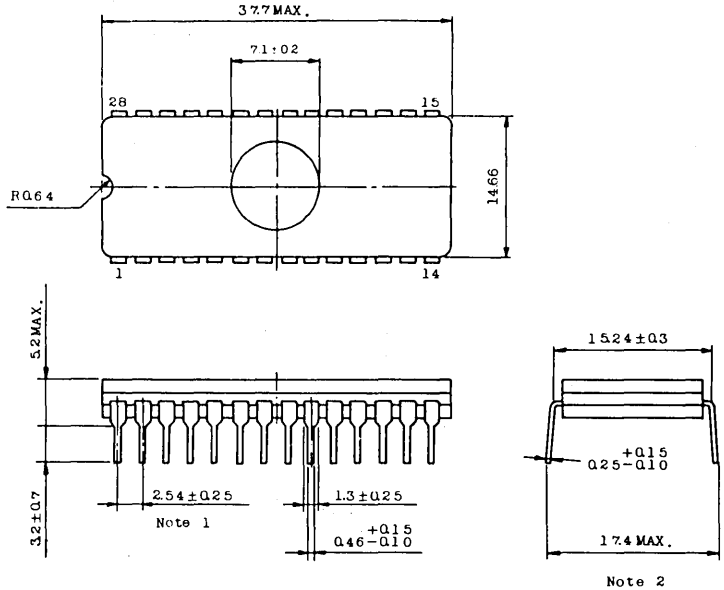
The following table shows electric signature of the TMM27256ADI.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

Notes : $A_9 = 12V \pm 0.5V$
A_1-A_8, A_{10}-A_{14}, $\overline{CE}$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCT

32,768 WORD X 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABEL READ ONLY MEMORY

TC57256D-20
TC57256D-25

SILICON STACKED GATE MOS

DESCRIPTION

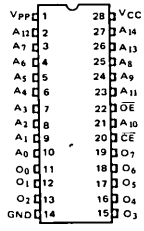
The TC57256D is a 32,768 word ×8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256D's access time is 200ns, and the TC57256D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30 mA/5MHz and standby current to 100μA.

For program operation, the programming is achieved by using the high speed programming mode. Program supply voltage is 21V. The programming of the TC57256D is accomplished within one and a half minutes (typ.) TC57256D is fabricated using CMOS technology and N-channel silicon double layer gate MOS technology.

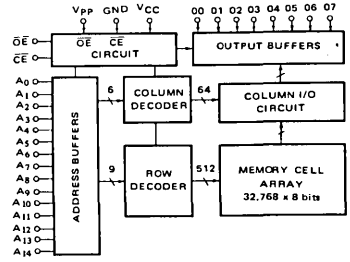
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  30mA/5MHZ (active)
  100μA (standby)
- Fast access time TC57256D-20 200 ns
  TC57256D-25 250 ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROMS TC53257P, TMM23256P and EPROM i27256
- Standard 28 pin DIP cerdip Package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H		5V	High Impedance	
Standby	H	*		5V	High Impedance	Standby
Program	L	H	21V	6V	Data In	Active
Program Inhibit	H	*			High Impedance	
Program Verify	L	L			Data Out	

* * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	−0.6 ~ 22.0	V
V_{IN}	Input Voltage	−0.6 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6 ~ V_{CC} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	−65 ~ 125	°C
T_{OPR}	Operating Temperature	−40 ~ 85	°C

READ OPERATION
D.C. RECOMMENDED OPERATING CONDITONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	−	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	−	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC} + 0.3	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input current	V_{IN} = 0 ~ V_{CC}		−	−	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$ = 0	f = 5MHz	−	−	30	mA
I_{CC02}			f = 1MHz	−	−	10	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}		−	−	1	mA
I_{CCS2}		$\overline{CE}$ = V_{CC} −0.2V		−	−	100	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA		2.4	−	−	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		−	−	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = 0 ~ V_{CC} + 0.3V		−	−	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V ~ V_{CC}		−	−	±10	μA

A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{CC} = 5V ±5%, V_{PP} = 2.0V ~ V_{CC} + 0.3V)

SYMBOL	PARAMETER	TEST CONDITION	TC57256D-20		TC57256D-25		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	−	200	−	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}	−	200	−	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IL}	−	70	−	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}	0	60	0	90	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	−	0	−	ns

A.C. TEST CONDITONS

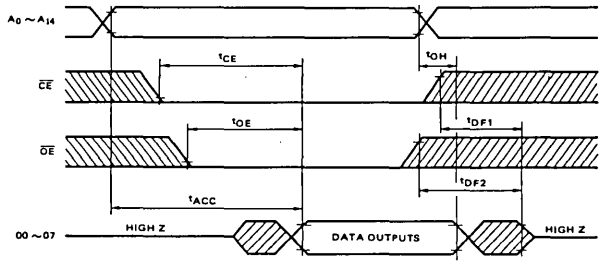
Output Load : 1 TTL Gate and C_L = 100pF
Input Pulse Rise and Fall Times : 10 ns Max.
Input Pulse Levels : 0.45 ~ 2.4V
Timing Mesurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = OV	–	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = OV	–	8	12	pF

*This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION
D.C. RECOMMENDED OPERATING CONDITONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 25 ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 21V ±0.5)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0 ~ V_{CC}	–	–	±10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 21.5V	–	–	30	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta = 25 ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 21V ±0.5)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs
t_{OEH}	$\overline{OE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	0.95	1	21	ms
t_{DV}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}	–	–	1	μs
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}	–	–	150	ns

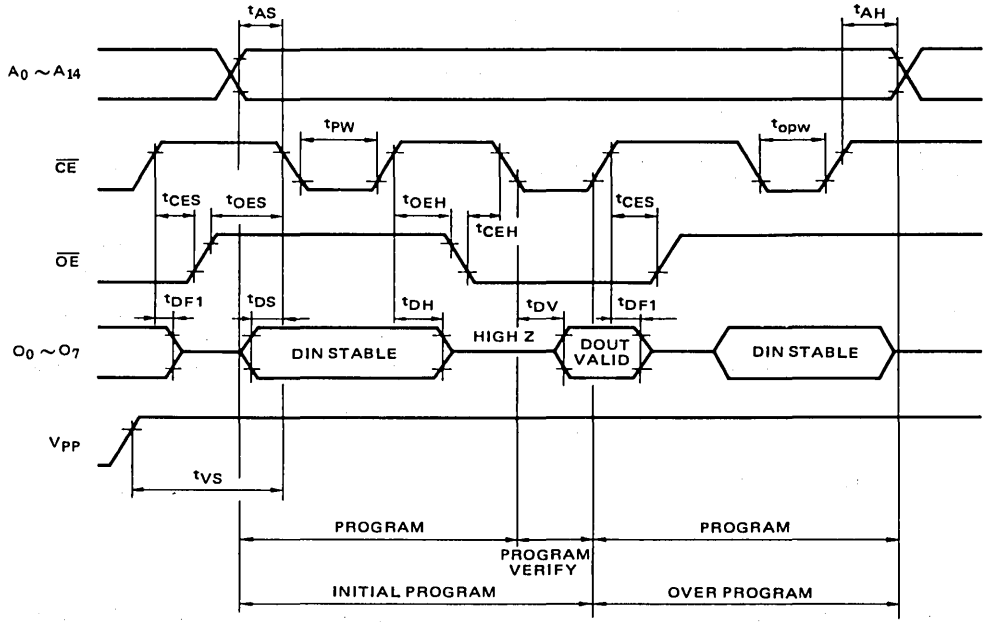
A.C. TEST CONDITIONS

Output Load	:	1 TTL Gate and C_L (100pF)
Input Pulse Rise and Fall Times	:	10 ns Max.
Input Pulse Levels	:	0.45 ~ 2.4V
Timing Measurement Reference Level	:	Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC} = 6V ±0.25V, V_{PP} = 21V ± 0.5V)



Note: (1) V_{CC} must be applied simultaneously with or before V_{PP} and cut off simultaneously with or after V_{PP}.
(2) Removing the device from socket and setting the device in socket with V_{PP}=21V may cause permanent damage to the device.
(3) The V_{PP} supply voltage is permitted up to 22V for program operation; voltages over 22V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not exceed 22V.

ERASURE CHARACTERISTICS

The TC57256D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) through the chips transparent window.

The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps with an ultraviolet light intensity of 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TC57256D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Both sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TC57256D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read Operation (Ta = −40 ~ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta = 25 ±5°C)	Program	L	H	21V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	L	L			Data Out	Active

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC57256D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after the address access time from stabilizing of all addressess.

The $\overline{CE}$ to output valid (t_{CE}) time is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{CE}$.

OUTPUT DESELECT MODE

With $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in high impedance state.
Therefore two or more TC57256D's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256D has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC57256D is placed in the standby mode which reduces the operating current to 100μA. The outputs will be in a high impedence state, independent of the $\overline{OE}$inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256D are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The TC57256D is in the programming mode when the V_{PP} input is at 21V and $\overline{CE}$ is at TTL-Low $\overline{OE}=V_{IH}$.

The TC57256D can be programmed at any location, anytime — either individually, sequentially or at randomly.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC57256D from being programmed.

Programming two or more TC57256D's in parallel with different data is easily accomplished: All inputs except for $\overline{CE}$ may be commonly connected, a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only, and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using a high speed programming mode. The device is set up in the high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

Programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified in the Program Verify Mode.

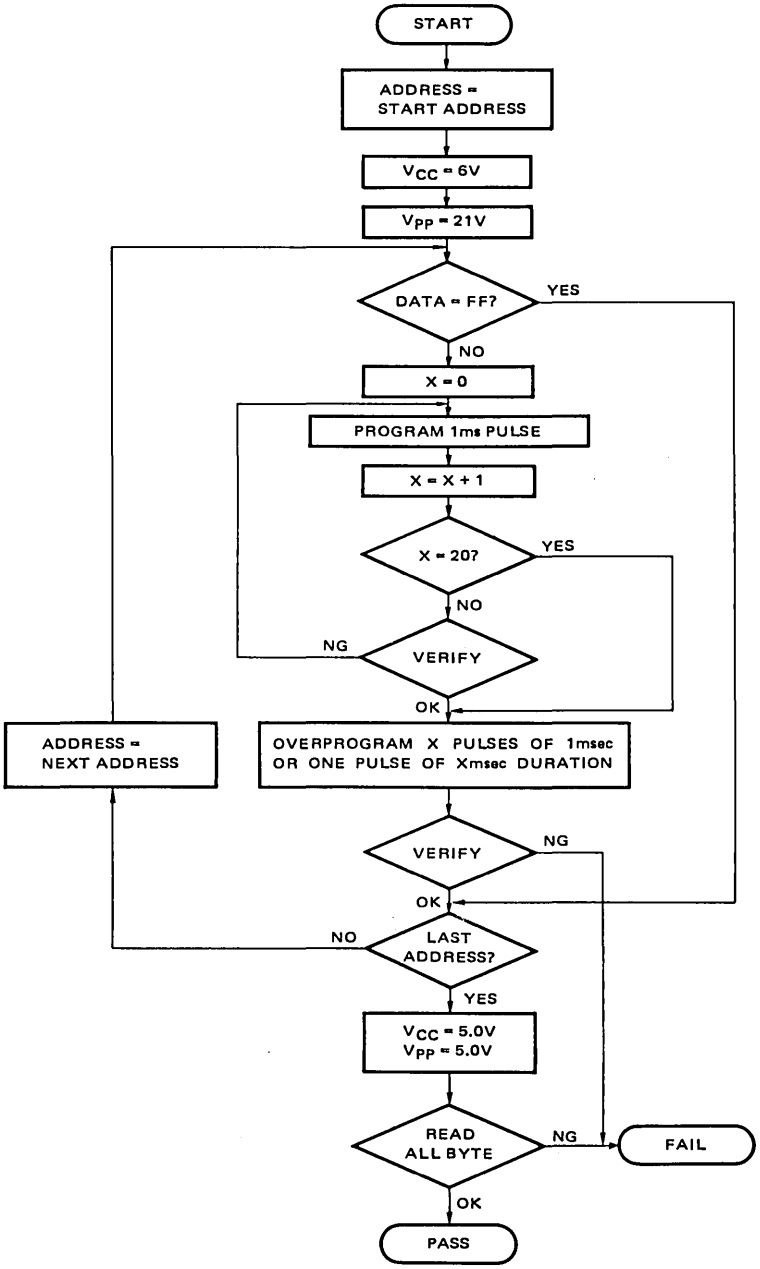
If the programmed data is not correct, another program pulse of 1ms is applied and the programmed data is verified. This should be repeated until the program operates correctly (max. 20 times).

After correctly programming the selected address, an additional program pulse with a width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

This high speed program algorithm allows the programming of the TC57256D to be accomplished within one and a half minutes (typ.)

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TC57256D which identifies its manufacture and device type.

The programming equipment may be used to read the manufacturer code and device code from the TC57256D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

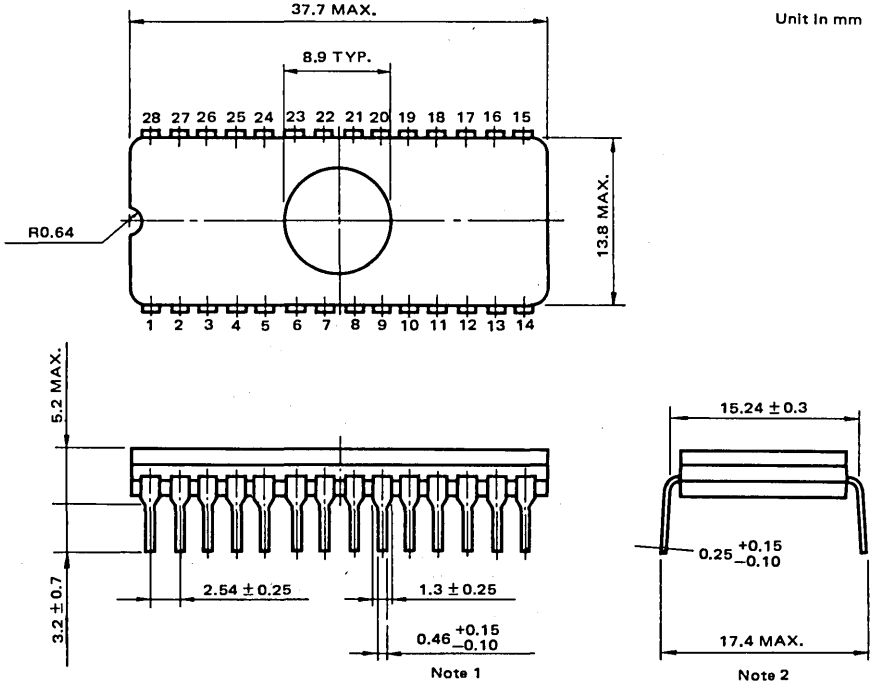
Electric Signature mode is set up when 12V is applied to address line A_9 and the rest of address lines are set to V_{IL} in read operation. Data output under these conditions is the manufacturer code. Device code is identified when address A_0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O_7).

The following table shows electric signature of TC57256D.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

Notes: $A_9 = 12V \pm 0.5V$
$A_1 - A_8$, $A_{10} - A_{14}$, $\overline{CE}$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS



Note: (1) Each lead pitch 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.
(2) This value is measured at the end of leads.
(3) The dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCT

TC57256AD-15
TC57256AD-20

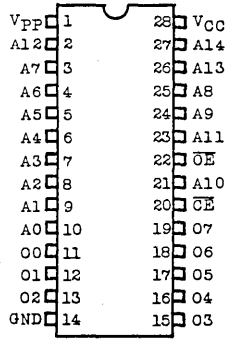
DESCRIPTION

The TC57256AD is a 32,768 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256AD's access time is 150ns. The TC57256AD operates from a single 5-volt power supply and has a low power standby mode which reduces power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 40mA/6.7MHz and the standby current to 100μA. For program operation, the programming is achieved by using the high speed prgramming mode. The TC57256AD is fabricated using CMOS technology and N-channel silicon double layer gate MOS technology.

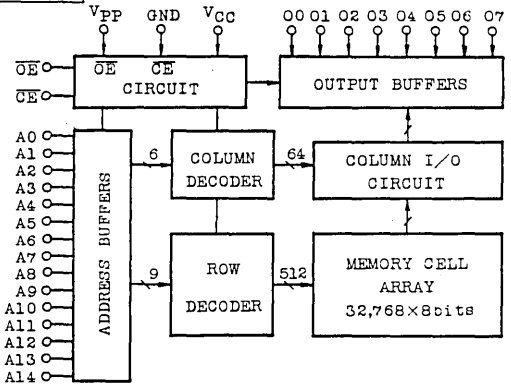
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  Active : 40mA/6.7MHz
  Standby: 100μA
- Fast access time:
  TC57256AD-15 150ns
  TC57256AD-20 200ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROMs TC53257P and TMM23256P, TMM27256AD and TC57256AD
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A14	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	

D.C. and OPERATING CHARACTERISTICS (Ta=-40 ∿ 85°C, V_{CC}=5V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0V ∿ V_{CC}		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$=0V	f=6.7MHz	-	-	40	mA
I_{CC02}		I_{OUT}=0mA	f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{CC} Current	V_{PP}=V_{CC} ± 0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ∿ V_{CC}		-	-	±10	μA

A.C. CHARACTERISTICS (Ta=-40∼85°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	TC57256AD-15		TC57256AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	150	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	70	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	0	60	
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	0	-	

A.C. TEST CONDITIONS

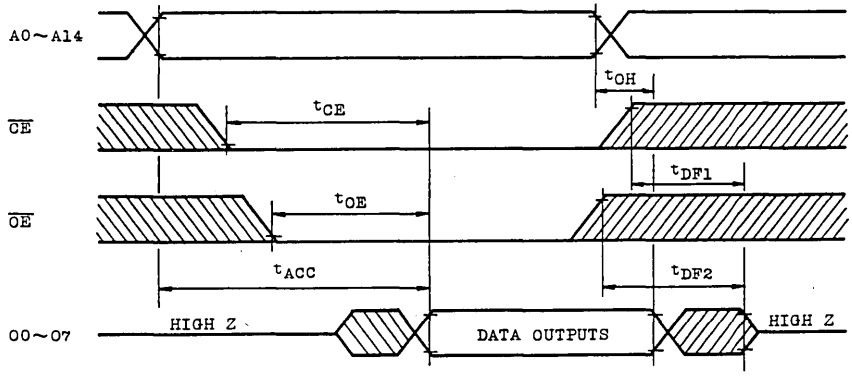
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V∼2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS ($Ta=25 \pm 5°C$, $V_{CC}=6V \pm 0.25V$, $V_{PP}=12.5V \pm 0.5V$)

SYMBOL	PARAMETER	TESTCONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS ($Ta=25 \pm 5°C$, $V_{CC}=6V \pm 0.25V$, $V_{PP}=12.5V \pm 0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

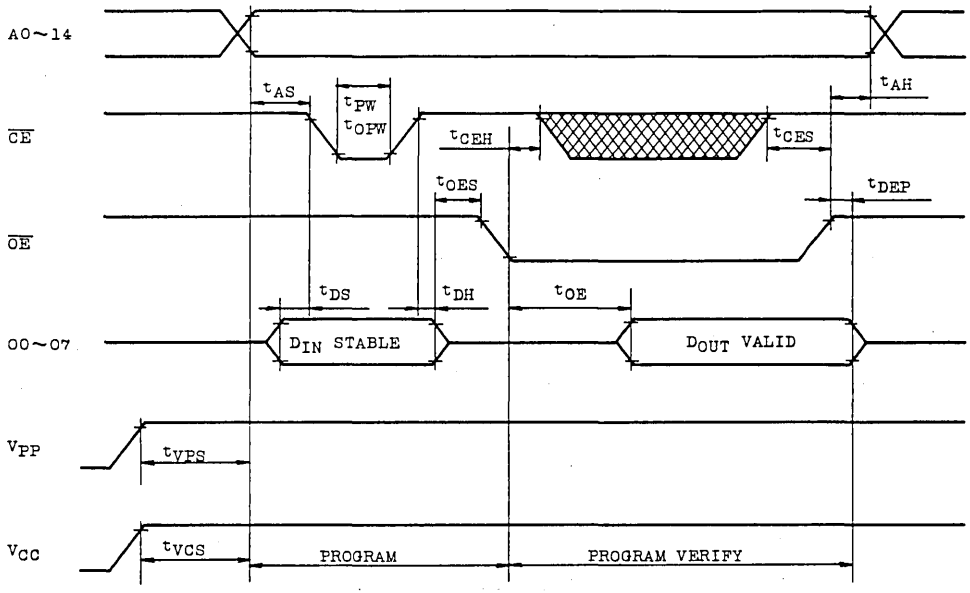
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : $0.45V \sim 2\ 4V$
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note: (1) V_{CC} must be applied simultaneously with or before V_{PP} and cut off simultaneously with or after V_{PP}.

(2) Removing the device from the socket or placing the device in the socket with V_{PP}=12.5V may cause permanent damage to the device.

(3) The V_{PP} supply voltage is permitted up to 14V for program operation; voltages over 14V should not be applied to the V_{PP} terminal. When a switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of the pulse should not exceed 14V.

ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light with a wavelength of 2537Å (Angstroms) through the transparent window of the chip.

The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w · sec/cm²].

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1 cm from the lamp surface, erasure will be achieved within 60 minutes.

Using a commercial lamp with an ultraviolet light intensity of 12000 [μw/cm²] reduces the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w · sec/cm²].)

The TC57256AD's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Both sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TC57256AD's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=-40 ∿ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25 ± 5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC57256AD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addressess.

The $\overline{CE}$ to output valid (t_{CE}) time is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

With $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, outputs will be in high impedance state so two or more TC57256AD's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256AD has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC57256AD is placed in the standby mode which reduces the operating current to 100μA. The outputs are in a high impedence state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "1" state, which is the erased state. The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The TC57256AD is in the programming mode when the Vpp input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$.

The TC57256AD can be programmed at any location, anytime, either individually, sequentially or randomly.

PROGRAM VERIFY MODE

The verify mode verifies that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to Vpp terminal, a high level $\overline{CE}$ input inhibits the TC57256AD from being programmed.

Programming of two or more TC57256AD's in parallel with different data is easily accomplished: all inputs except for $\overline{CE}$ and $\overline{OE}$ are commonly connected, a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only, and TTL high level signals are applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly reduced by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the Vpp terminal with $V_{CC}=6V$.

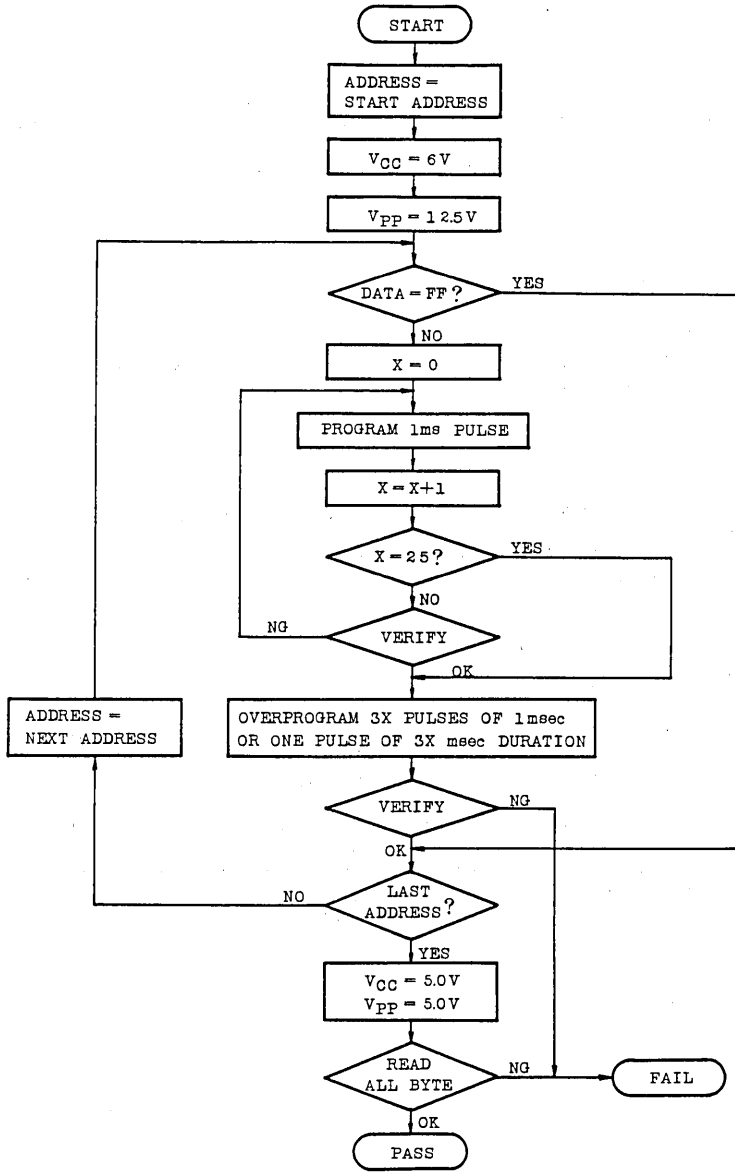
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. The programmed data is then verified by using the Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and the programmed data is verified. This should be repeated until the programmed data is correct. (max. 25 times)

After correctly programming the selected addresses, an additional program pulse with a width of 3 times more than that needed for initial programming is applied.

When programming has been completed. Data in all addresses should be verified with $V_{CC}=Vpp=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TC57256AD which identifies its manufacture and device type.

The programming equipment may be used to read the manufacturer code and device code from the TC57256AD by using this mode before program operation, and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output under these conditions is the manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O_7).

The following table shows the electric signature of the TC57256AD.

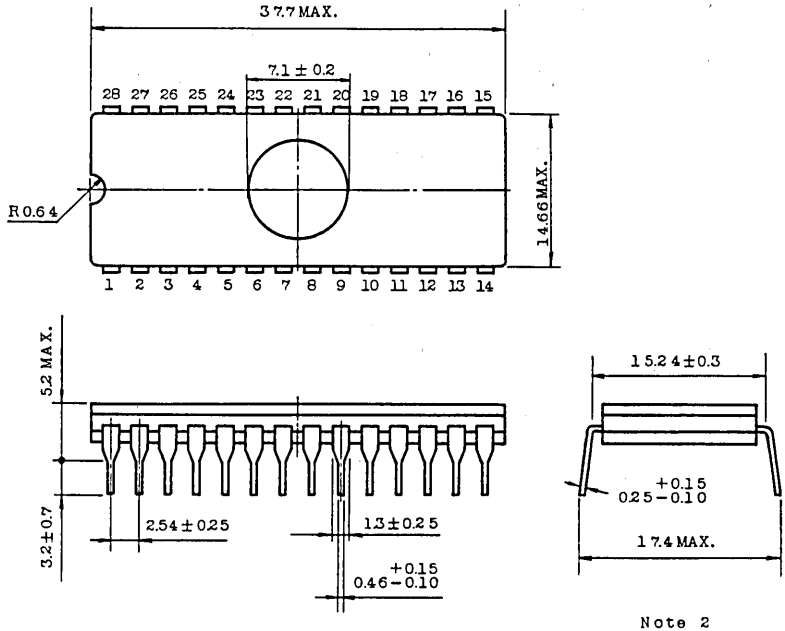
PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}$=V_{IL}

OUTLINE DRAWINGS

Unit in mm



Note 1

Note 2

Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCT

65,536 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
PRELIMINARY

TMM27512D-20,TMM27512D-200
TMM27512D-25,TMM27512D-250

DESCRIPTION

The TMM27512D is a 65,536 word × 8 bit ultraviolet light erasable and electrically programmable read memory.

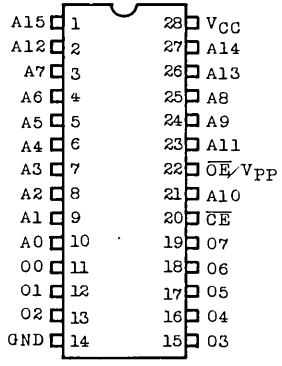
For read operation, the TMM27512D's access time is 200ns/250ns. The TMM27512D operates from a single 5-volt power supply and has a low power standby mode which reduces power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. For program operation, the programming is achieved by using the high speed prgramming mode. The TMM27512D is fabricated with N-channel silicon double layer gate MOS technology.

FEATURES

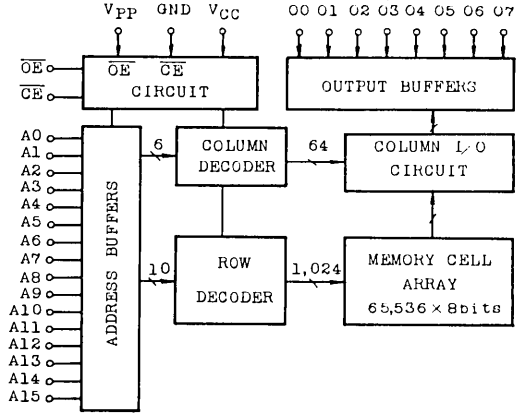
	−20	−25	−200	−250
V_{CC}	5V±5%		5V±10%	
t_{ACC}	200ns	250ns	200ns	250ns
I_{CC2}	120mA		130mA	
I_{CC1}	35mA		40mA	

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27512
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{15}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	V_{PP}	6V	Data In	Active
Program Inhibit	H	V_{PP}		High Impedance	
Program Verify	L	L		Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. AND RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27512D-20/25	TMM27512D-200/250
Ta	Operating Tamperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}		—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	−20/25	—	—	35	mA
			−200/250	—	—	40	
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	−20/25	—	—	120	mA
			−20/250	—	—	130	
V_{IH}	Input High Voltage	—		2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—		−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA		2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6		—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27512D-20/200		TMM27512D-25/250		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	200	—	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	90	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

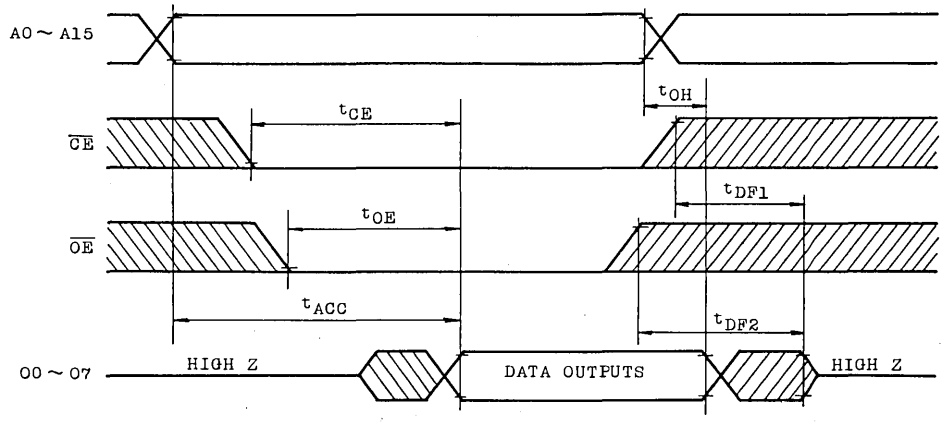
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN}=0V$	—	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN}=0V$	—	50	60	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	130	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	—	2	—	—	μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	—	2	—	—	μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time	—	50	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}/V_{PP}=V_{PP}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	—	—	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	—	—	130	ns

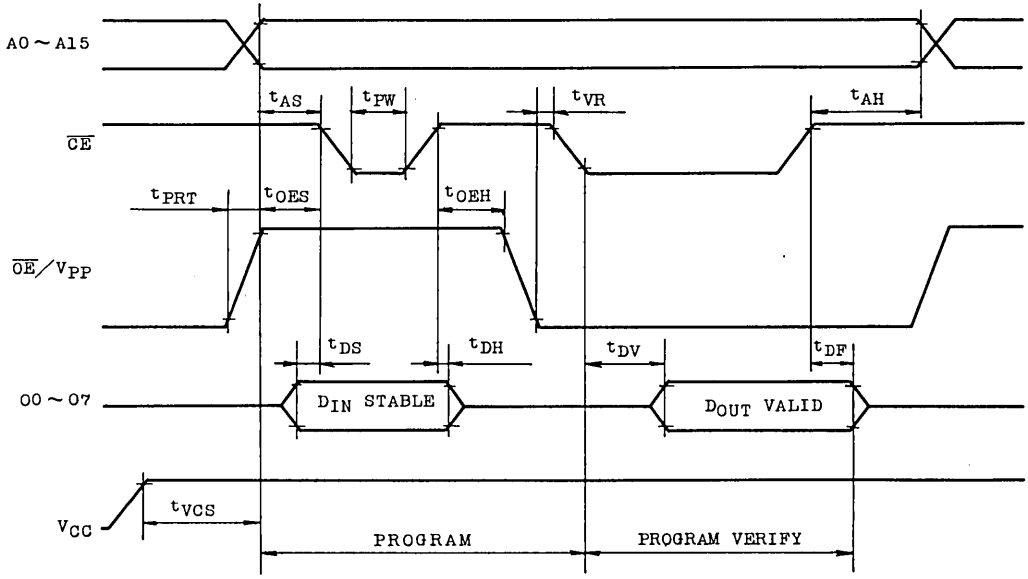
A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note: (1) V_{CC} must be applied simultaneously with or before V_{PP} and cut off simultaneously with or after V_{PP}.
(2) Removing the device from the socket and setting the device in the socket with V_{PP}=12.5V may cause permanent damage to the device.
(3) The V_{PP} supply voltage is permitted up to 14V for program operation; Voltages over 14V should be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not exceed 14V.

ERASURE CHARACTERISTICS

The TMM27512D's erasure is achieved by applying shortwave ultraviolet light with a wavelength of 2537Å (Angstroms) through the transparent window of the chip.

The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²].

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1cm from the lamp surface, erasure will be achieved within 60 minutes.

Using a commercial lamp with an ultraviolet light intensity of 12000 [μw/cm²] reduces the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (10×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27512D's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Sunlight and flourescent lamps both include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27512D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	Active
	Standby	H	*		High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	V_{PP}	6V	Data In	Active
	Program Inhibit	H	V_{PP}		High Impedance	Active
	Program Verify	L	L		Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM27512D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addressess.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL}, and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

With $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, outputs will be in a high impedance state, so two or more TMM27512D's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27512D has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27512D is placed in the standby mode which reduces 70% of the operating current. The outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27512D are in the "1" state which is the erased state. The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The TMM27512D is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-Low level

The TMM27512D can be programmed at any location, anytime, either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode verifies that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}/V_{PP}$ at V_{IL} and at $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM27512D from being programmed.

Programming of two or more TMM27512D's in parallel with different data is easily accomplished: all inputs except for $\overline{CE}$ are commonly connected, a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only, and TTL high level signals are applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

This high speed programming mode is performed at V_{CC}=6.0V and $\overline{OE}/V_{PP}$=12.5V

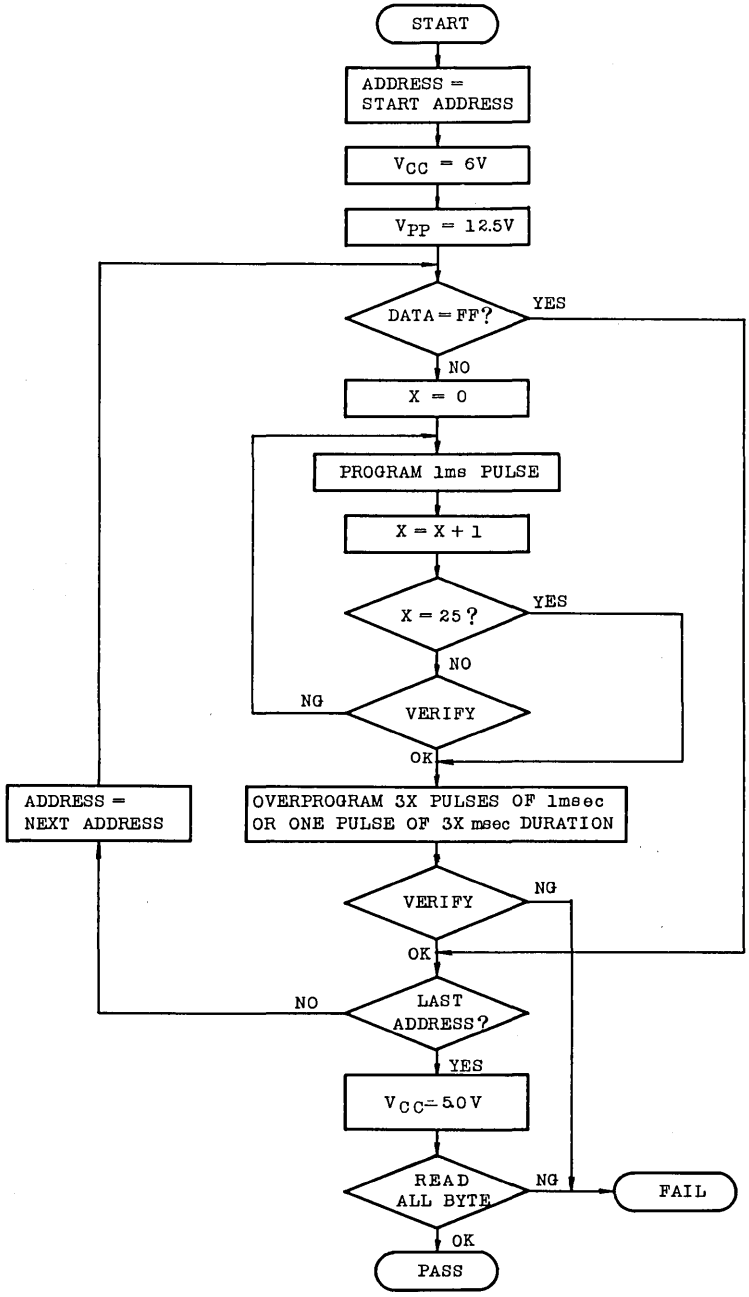
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. The programmed data is then verified by using the Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and the programmed data is reverified. This should be repeated until the programmed data is correct. (max. 25 times)

After correctly programming the selected address, an additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27512D which identifies its manufacture and device type.

The programming equipment may be used to read out the manufacturer code and device code from the TMM27512D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output under these conditions is the manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07).

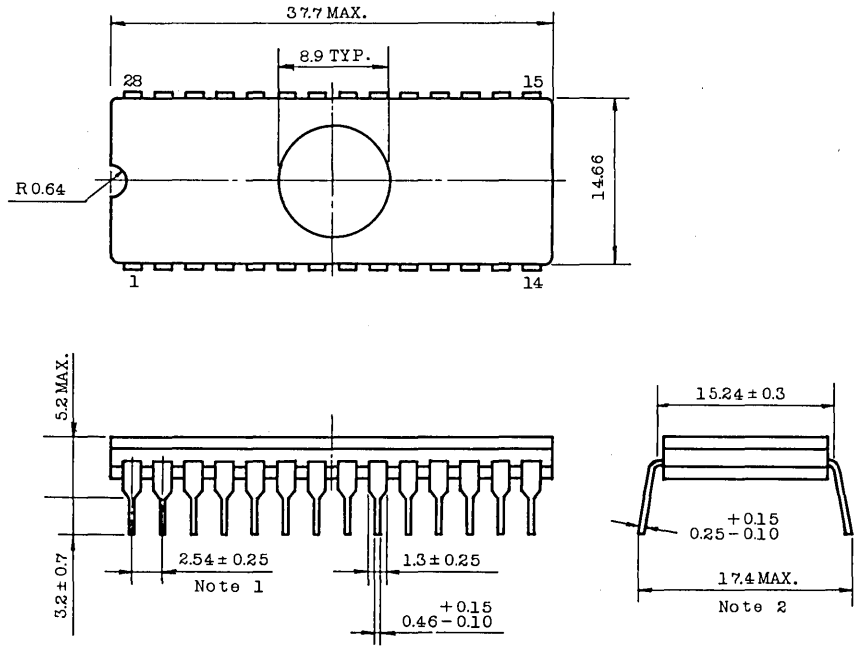
The following table shows electric signature of the TMM27512D.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	1	0	1	0	1	15

Notes : A9 = 12V±0.5V
A1~A8, A10~A15, $\overline{CE}$, $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

TOSHIBA MOS MEMORY PRODUCT

65,536 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
PRELIMINARY

TMM27512DI-20
TMM27512DI-25

DESCRIPTION

The TMM27512DI is a 65,536 word × 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27512DI's access time is 200ns/250ns. The TMM27512DI operates from a single 5-volt power supply and has a low power standby mode which reduces power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

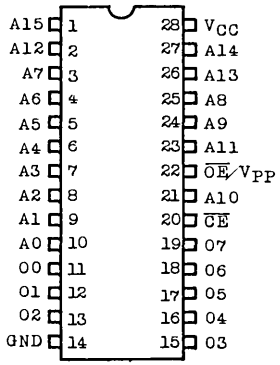
For program operation, the programming is achieved by using the high speed prgramming mode. TMM27512DI is fabricated with N-channel silicon double layer gate MOS technology.

FEATURES

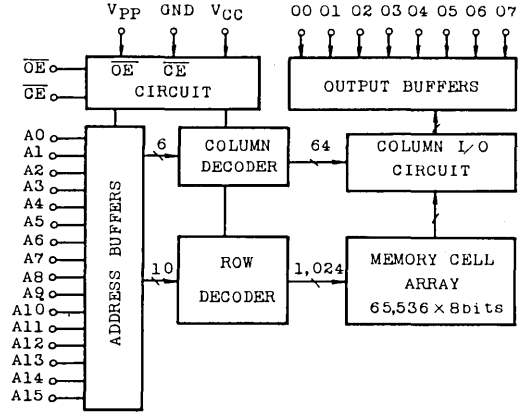
	−15	−20
V_{CC}	5V±5%	
t_{ACC}	150ns	200ns
I_{CC2}	120mA	
I_{CC1}	35mA	

- Wide operating temparature range −40~85°C
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27512
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{15}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$/V_{PP}	Output Enable Input / Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$/V_{PP} (22)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	V_{PP}	6V	Data In	Active
Program Inhibit	H	V_{PP}		High Impedance	
Program Verify	L	L		Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	−40~85	°C

READ OPERATION

D. C. AND RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27512DI-20/25
Ta	Operating Temperature	−40~85°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4\sim V_{CC}$	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{IH}$	—	—	40	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}=V_{IL}$	—	—	130	mA
V_{IH}	Input High Voltage	—	2.2	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	—	−0.3	—	0.8	V
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=0\sim V_{CC}+0.6$	—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27512DI-20		TMM27512DI-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	200	—	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	90	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

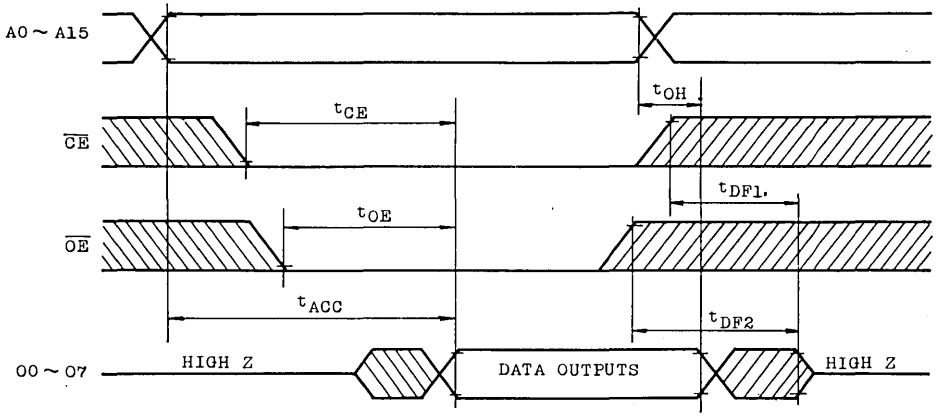
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN}=0V$	—	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN}=0V$	—	50	60	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	130	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	—	2	—	—	μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	—	2	—	—	μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time	—	50	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}/V_{PP}=V_{PP}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	—	—	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	—	—	130	ns

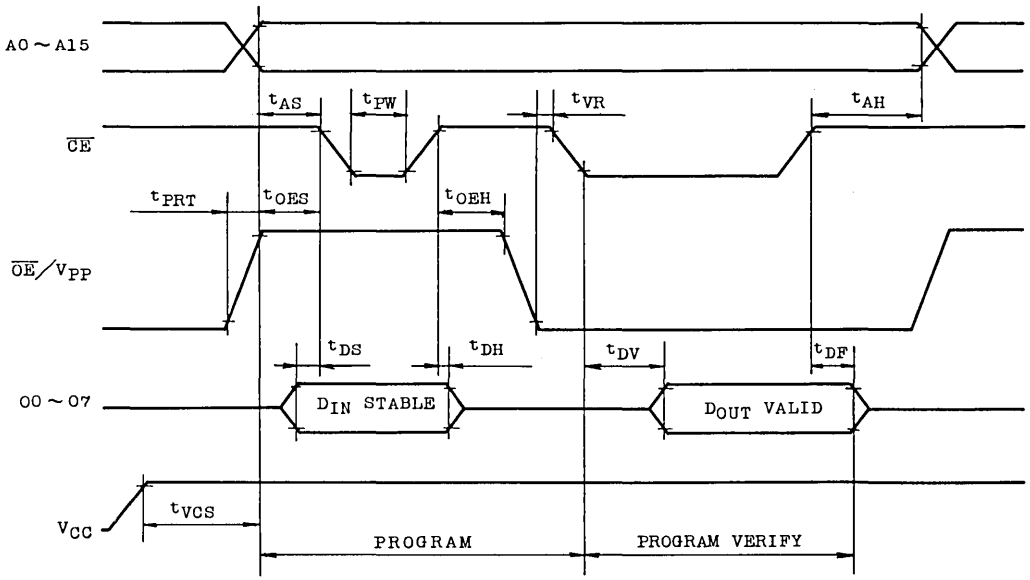
A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should be aplied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM27512DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelegth of 2537Å (Angstroms) to the Chip through the transparent window. Then integrated dose (ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] ×(10×60) [sec] ≅15 [w·sec/cm²] .)

The TMM27512DI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wevelength components. Therefore when used under such lighting for extended periods of time, the opeque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM27512DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read Operation (Ta=−40~85°C)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	Active
	Standby	H	*		High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	V_{PP}	6V	Data In	Active
	Program Inhibit	H	V_{PP}		High Impedance	Active
	Program Verify	L	L		Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM27512DI has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM27512DI's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27512DI has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27512DI is placed in the standby mode which reduce 70% of the operating current by applying TTL-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27512DI are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TMM27512DI is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-Low level.

The TMM27512DI can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}/V_{PP}$ at V_{IL} and $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM27512DI from being programmed.

Programming of two or more TMM27512DI's is parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

This high speed programing mode is performed at $V_{CC}=6.0V$ and $\overline{OE}/V_{PP}=12.5V$

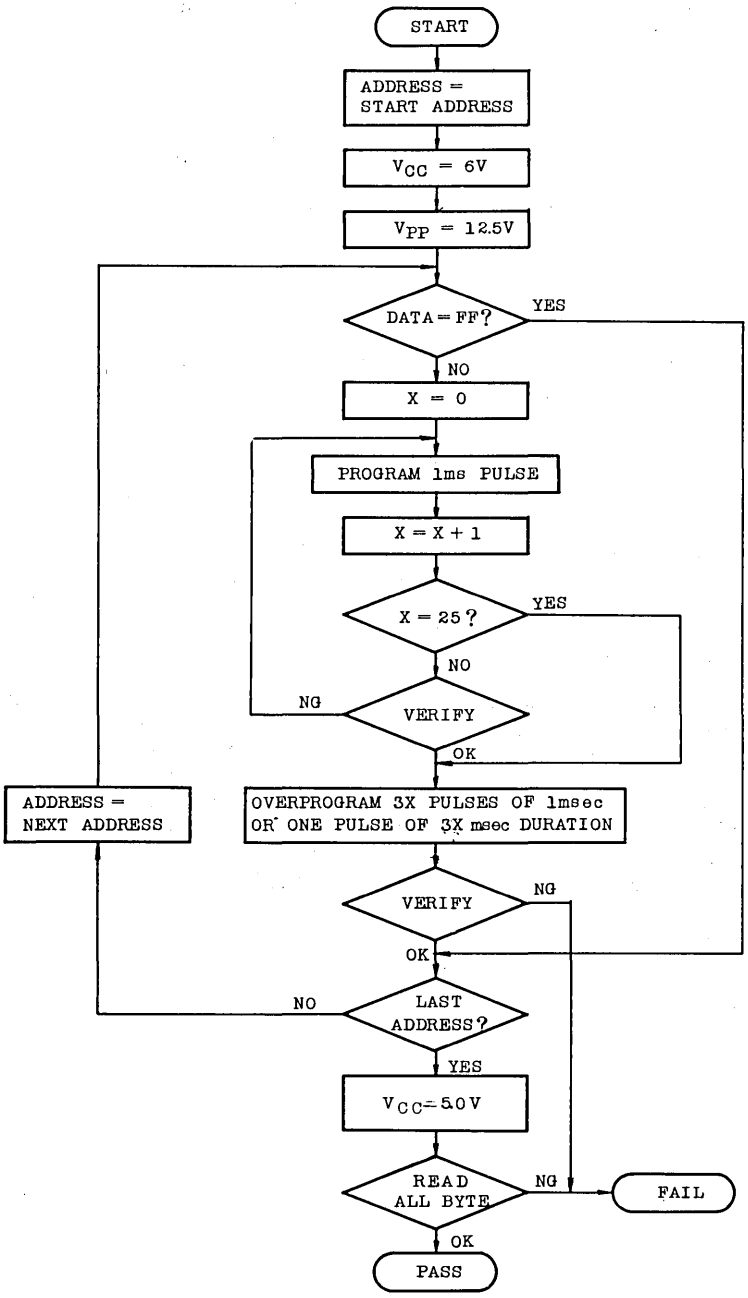
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completd, the data in all addresses should be verified with $V_{CC}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM27512DI which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM27512DI by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07).

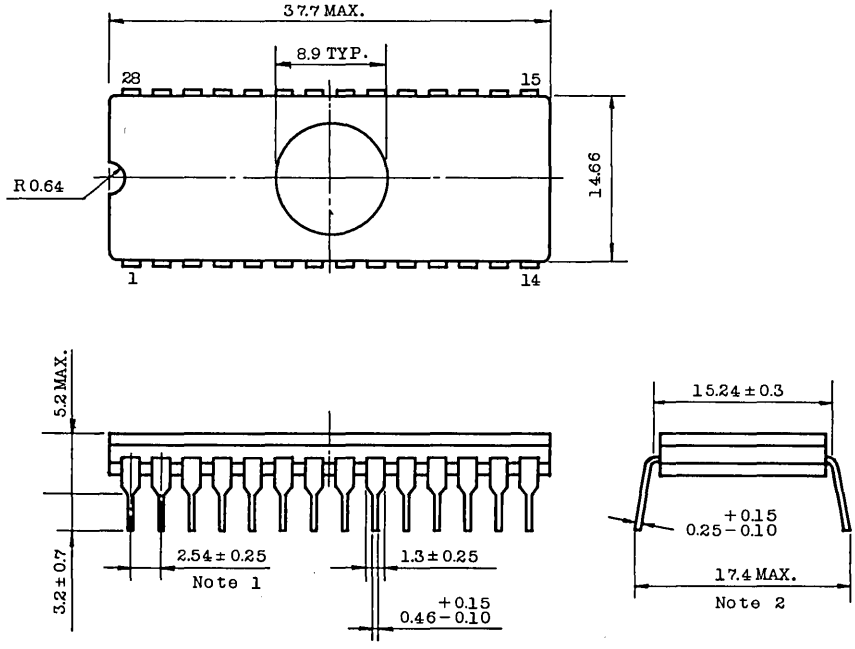
The following table shows electric signature of TMM27512DI.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	1	0	1	0	1	15

Notes : A9 = 12V$\pm$0.5V
A1~A8, A10~A15, $\overline{CE}$, $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

TOSHIBA MOS MEMORY PRODUCT

1 MEGA BIT (131,072 WORD × 8 BIT)
SILICON STACKED GATE MOS
CMOS U.V. Erasable & Electrically
Programmable Read Only Memory

TC571000D-20, TC571000D-25
TC571001D-20, TC571001D-25

DESCRIPTION

The TC571000D/TC571001D is a 131,072 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571000D is JEDEC standard pin configuration and the TC571001D is compatible with 28 pin 1M bit Mask ROM. Both products are packed in 32 pin standard cerdip package.

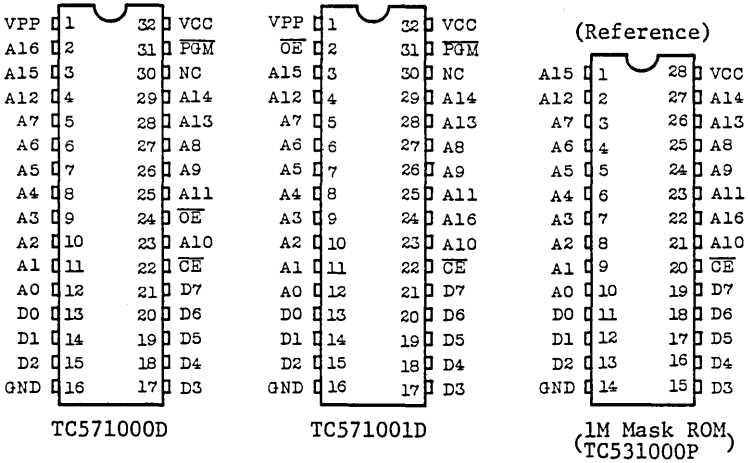
TC571000D/TC571001D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 30mA/5.0MHz and access time of 200ns/250ns.

The programming times of the TC571000D/TC571001D except overhead times of EPROM programmer is only 14 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Fast access Time
  TC571000D-20/TC571001D-20: 200ns
  TC571000D-25/TC571001D-25: 250ns
- Low power dissipation
  Active : 30mA/5.0MHz
  Standby: 100μA (Ta=85°C)
- Single 5V power supply
- Wide operating temperature range: -40 ∿ 85°C
- Full static operation
- High speed programming operation: t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin: TC571000D
- 1M MROM compatible : TC571001D
- Standard 32 pin DIP cerdip package

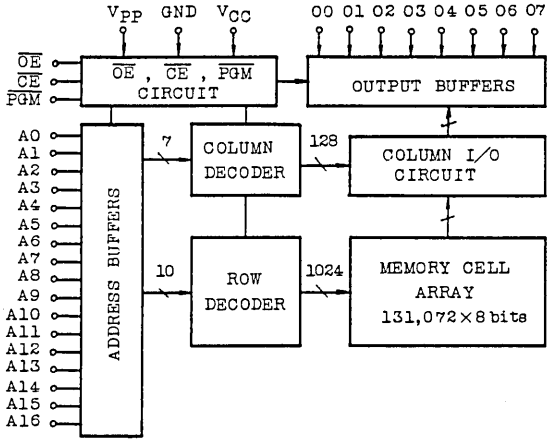
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A16	Address Inputs
D0 ∿ D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	00 ∿ 07	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* : H or L.

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 • 10	°C• sec
T_{STRG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	

D.C. and OPERATING CHARACTERISTICS ($Ta=-40 \sim 85°C$, $V_{CC}=5V \pm 5\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$		-	-	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}$=0V	f=5.0MHz	-	-	30	mA
I_{CCO2}		I_{out}=0mA	f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}=V_{IH}$		-	-	1	mA
I_{CCS2}		$\overline{CE}=V_{CC}-0.2V$		-	-	100	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$		2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$		-	-	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=V_{CC} \pm 0.6V$		-	-	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4V \sim V_{CC}$		-	-	10	μA

A.C. CHARACTERISTICS ($Ta=-40 \sim 85°C$, $V_{CC}=5V \pm 5\%$, $V_{PP}=V_{CC} \pm 0.6V$)

SYMBOL	PARAMETER	TC571000D-20/TC571001D-20		TC571000D-25/TC571001D-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	200	-	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	200	-	250	
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	100	
t_{PGM}	$\overline{PGM}$ to Output Valid	-	70	-	100	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	90	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	90	
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	90	
t_{OH}	Output Data Hold Time	0	-	0	-	

A.C. TEST CONDITIONS

Output Load : 1 TTL Gate and C_L=100pF

Input Pulse Rise and Fall Times : 10ns Max.

Input Pulse Levels : 0.45V to 2.4V

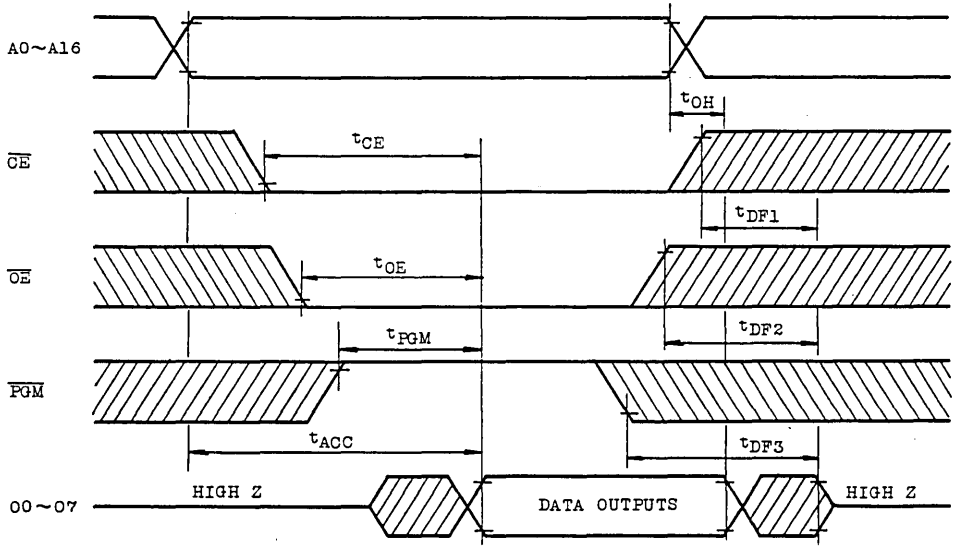
Timing Measurement Reference Level : Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	10	12	

* This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

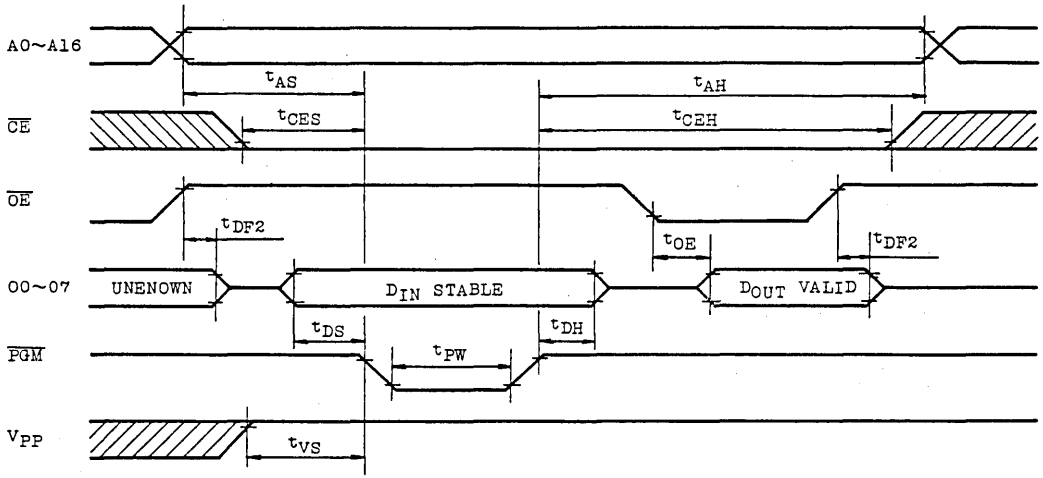
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	-	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	-	-	-	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after Vpp.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC571000D/571001D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [W/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [W. sec/cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1 cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm^2] × (20 × 60) [sec] ≅ 15 [W• sec/cm^2].)

The TC571000D/TC571001D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000∿4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opeque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC571000D/TC571001D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

		$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O_0∿O_7	POWER
READ OPERATION (Ta=-40∿85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC571000D/TC571001D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.
Assuming in that $\overline{CE}$=$\overline{OE}$=V_{IL} and $\overline{PGM}$=V_{IH}, the output data is valid at the output after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL}, $\overline{PGM}$=V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.
And assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two or more ROMs can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC571000D/TC571001D has a low power standby mode controlled by the $\overline{CE}$ signal.
By applying a high level to the $\overline{CE}$ input, the TC571000D/TC571001D is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC571000D/TC571001D are in the "1" state which is erased state.
Threrefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The levels required for all inputs are TTL. The TC571000D/TC571001D can be programmed any location at anytime ——— either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

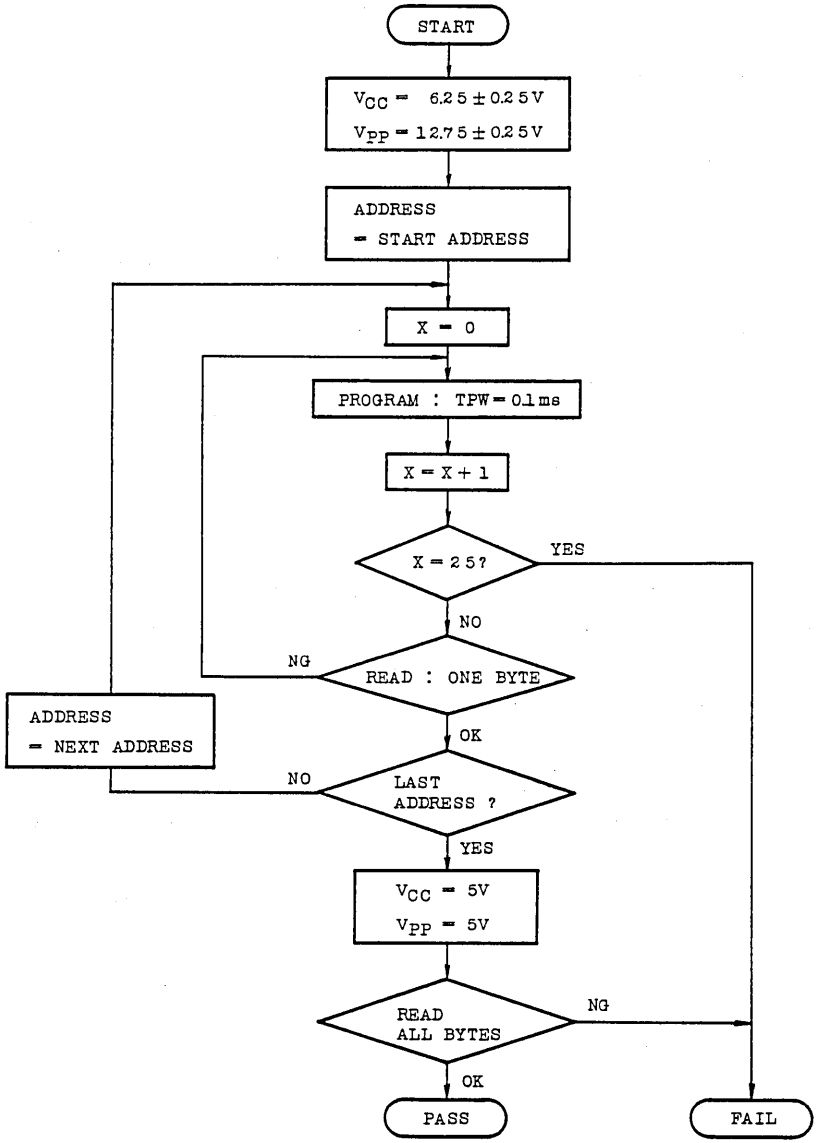
Under the condition that the program voltage (+12.75V) is applied to Vpp terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC571000D/TC571001D from being programmed. Programming of two or more EPROMS in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC}=6.25V and $\overline{PGM}$=V_{IH}.
The programming is achieved by applying a single TTL low level 0.1 ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC571000D/TC571001D which identifies it's manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC571000D/TC571001D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TC571000D/TC571001D.

SIGNATURE \ PINS		A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	HEX. DATA
Manufacture Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC571000D	V_{IH}	1	0	0	0	0	1	1	0	86
	TC571001D		0	0	0	0	0	1	1	1	07

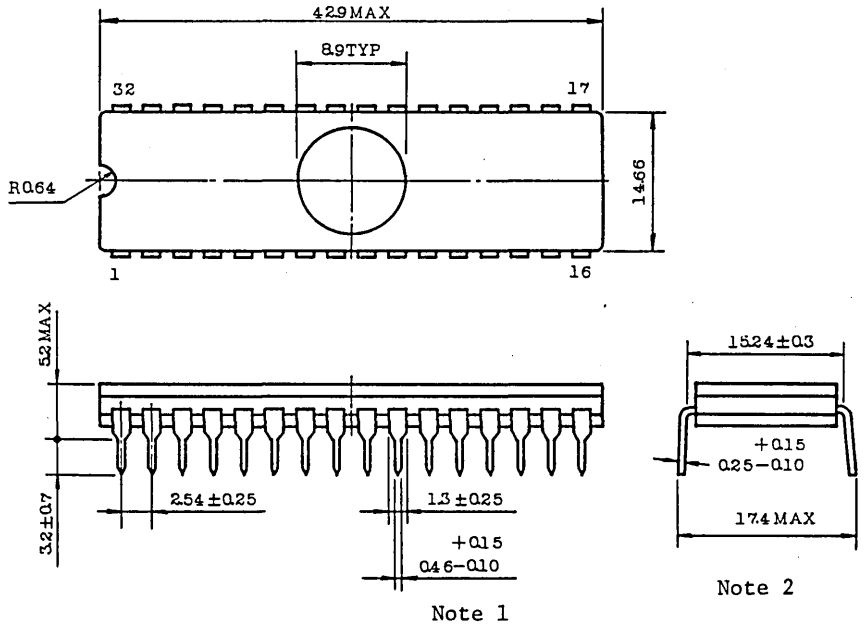
Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A16, $\overline{CE}$, $\overline{OE}$=V_{IL}

$\overline{PGM}$=V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note 1

Note 2

Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect NO.1 and No.32 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

One Time Programmable Read Only Memories

HIGH SPEED PROGRAMMING MODE

FEATURES

The High Speed Programming I or High Speed Programming II Algorithms may be used to program 64K through 512K devices. The 1MEGABIT devices may be programmed using the High Speed Programming II Algorithm.

The High Speed Programming I Algorithm uses 1ms programming pulse and the flow chart is shown in Figure 1.

The High Speed Programming II Algorithm uses 0.1ms programming pulse and the flow chart is shown in Figure 2.

APPLICABLE DEVICES

Device Name		Theoretical Programming Time	
EPROM	One Time PROM	I	II
TMM2764AD/ADI	TMM2464AP/AF	33 sec	0.8 sec
TMM27128AD/ADI	TMM24128AP/AF	66 sec	1.7 sec
TMM27256AD/ADI	TMM24256AP/AF	131 sec	3.3 sec
TC57256AD	TC54256AP/AF	131 sec	3.3 sec
TMM27512D/DI	TMM24512P	262 sec	7.0 sec
TC571000D	TC541000P	N/A	14 sec
TC571001D	TC541001P	N/A	14 sec

IDENTIFICATION MODE

The identification mode allows the reading of an electrical signature from the device that will identify the manufacturer and device type. The identification mode is activated using the following conditions:

1. For the Manufacturer Code:
   Set A9=12V±0.5V, Aϕ=ViL, Other Addresses=ViL
   Note: The manufacturer code is consistent with the E.I.A. standard.
2. For the Device Code:
   Set A9=12V±0.5V, Aϕ=ViH, Other Addresses=ViL.
   Note: The Device Code is manufacturer dependent.

The following table shows the Electrical Signatures of Toshiba devices.

ELECTRICAL DEVICES

Device Name		Signature	
EPROM	One Time PROM	Manufacture Code	Device Code
TMM2764AD/ADI	TMM2464AP/AF	98	52
TMM27128AD/ADI	TMM24128AP/AF	98	D3
TMM27256AD/ADI	TMM24256AP/AF	98	54
TC57256AD	TC54256AP/AF	98	C4
TMM27512D/DI	TMM24512P	98	15
TC571000D	TC541000P	98	86
TC571001D	TC541001P	98	07

Figure 1

HIGH SPEED PROGRAM I FLOW CHART

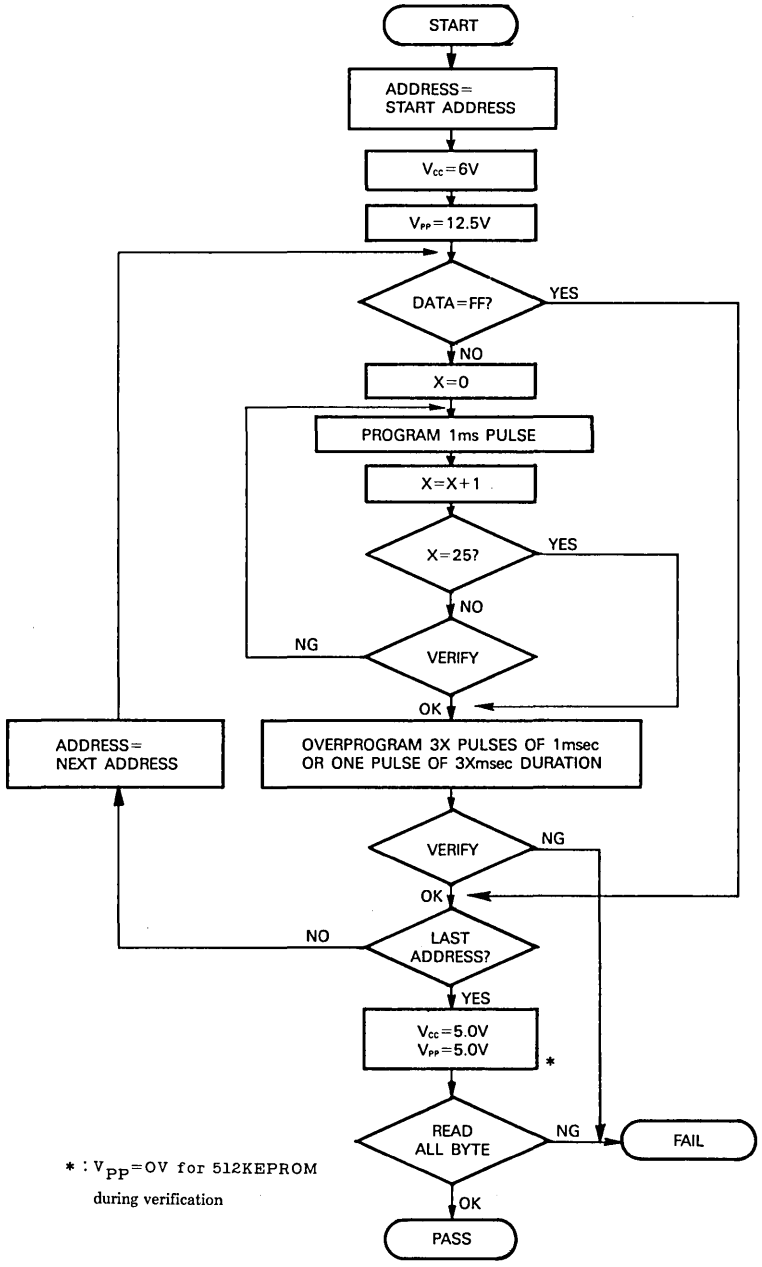
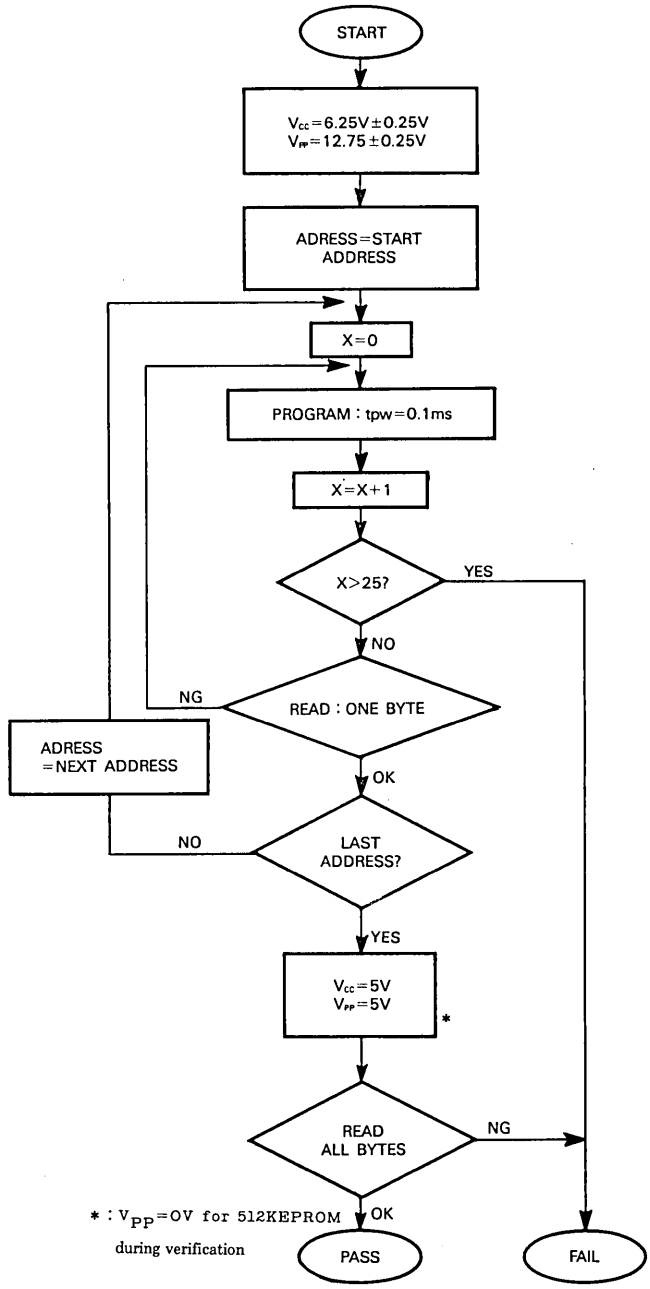


Figure 2

HIGH SPEED PROGRAM II FLOW CHART



TOSHIBA MOS MEMORY PRODUCT

TMM2464AP/AF 8,192 WORD × 8 BIT
ONE TIME PROGRAMMABLE READ ONLY MEMORY
N CHANNEL SILICON STACKED GATE MOS

TMM2464AP/AF

DESCRIPTION

The TMM2464AP/AF is a 8,192 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic DIP.

The TMM2464AP/AF's access time is 200ns, and has low power standby mode which reduces the power dissipation without increasing access time.

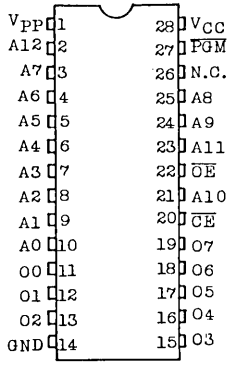
The electrical characteristics and programming method are the same as U. V. EPROM TMM-2764AD's.

Once programed, the TMM2464AP/AF can not be erased because of using plastic DIP without transparent window.

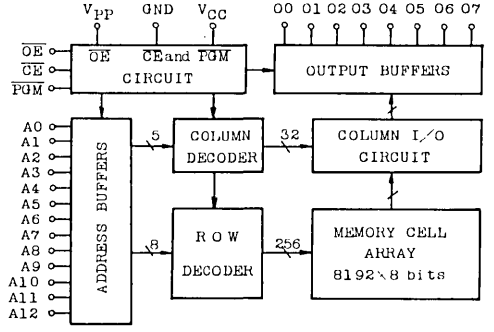
FEATURES

- Single 5 volt power supply
- Fast access time: 200ns (Max.)
- Power dissipation : 100mA(active current) Max.
  : 30mA(standby current) Max.
- Low power standby mode : $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Full static operation
- High speed programming mode
- Three state outputs
- Inputs and outputs TTL compatible
- Compatible with TMM2764AD and ROM TMM2365P, TC5365P.
- 28 PIN standard plastic package: TMM2464AP
- 28 PIN flat package : TMM2464AF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N.C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG.}$	Storage Temperature	−55~150	°C
$T_{OPR.}$	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	−	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	−	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	V_{PP} Power Supply Voltage	2.2	V_{CC}	V_{CC}+0.6	

D. C. and OPERATING CHARACTERISTICS

($Ta=0\sim70°C$, $V_{CC}=5V\pm5\%$, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	−	−	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{IH}$	−	−	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}=V_{IL}$	−	−	100	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	−	−	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	−	−	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=0\sim V_{CC}+0.6V$	−	−	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4V\sim V_{CC}$	−	−	±10	μA

A. C. CHARACTERISTICS

($Ta = 0 \sim 70$ C, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 2.0V \sim V_{CC} + 0.6V$, Unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	–	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	–	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	ns
t_{OH}	Output Data Hold Time	0	–	ns

A. C. TEST CONDITIONS

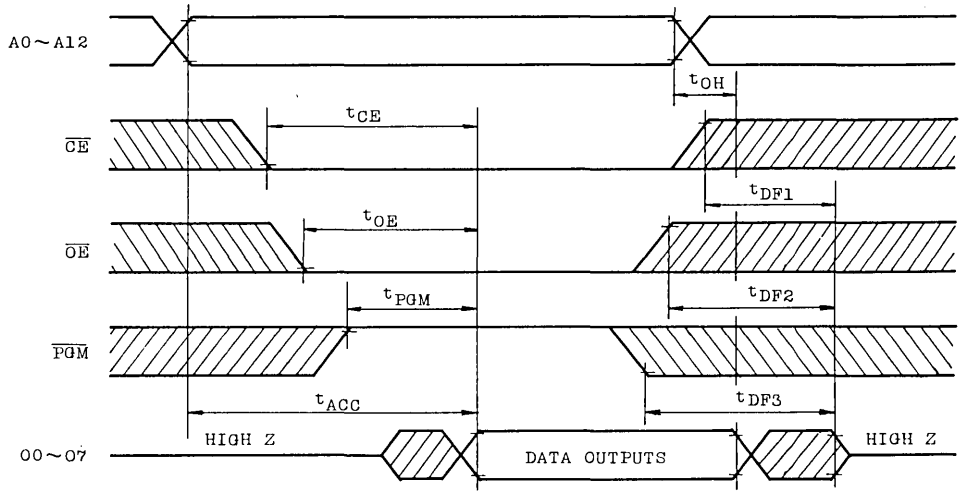
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	–	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	–	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA

A. C. PROGRAMMING CHARACTERISTICS ($Ta=25\pm5$ C, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

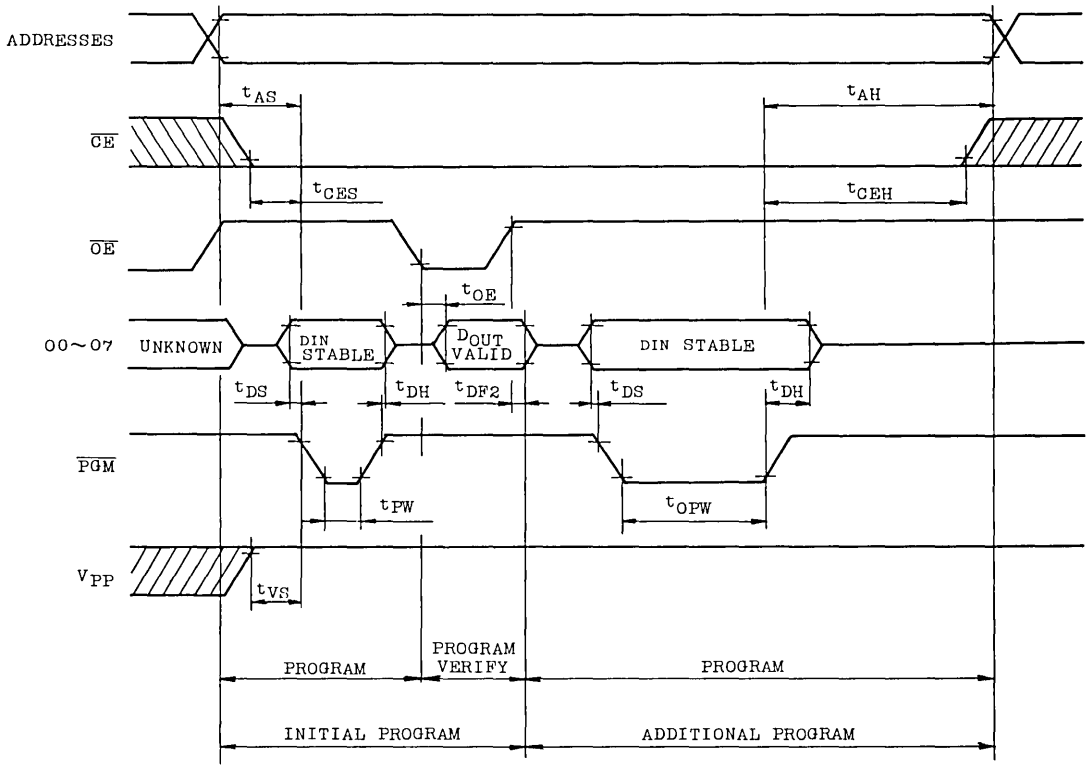
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. t_{OPW} depend on the program pulse width which is reguired in the initial program.

TIMING WAVEFORMS (HIGH SPEED PROGRAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM2464AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs. In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES(NUMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM2464AP/AF has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the outpus after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TMM2464AP/AF can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2464AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a TTL high level to the $\overline{CE}$ input, the TMM2464AP/AF is placed in the standby mode which reduce the operating current from 100mA to 30mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2464AP/AF from being programmed. Programming of two or more TMM2464AP/AF in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGMAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$=V_{IH}. The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM2464AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM2464AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

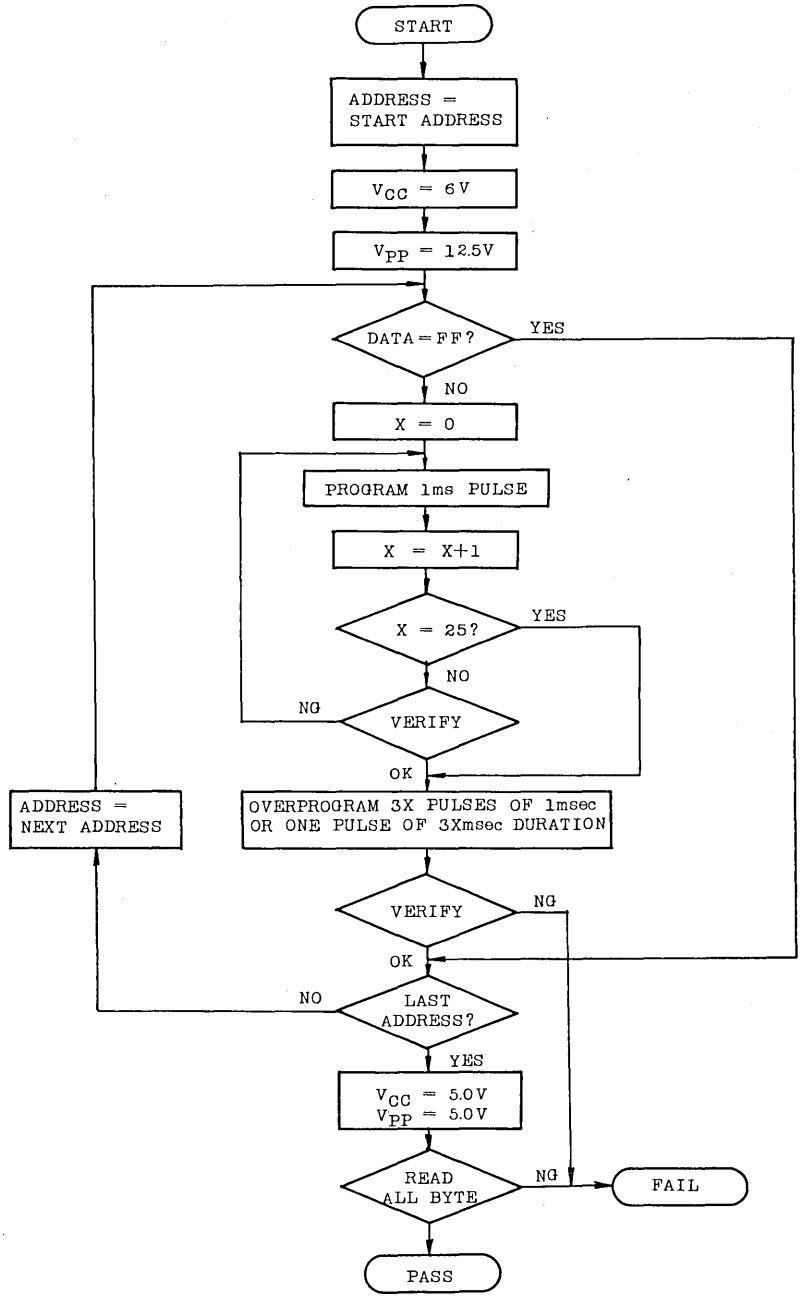
Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM2464AP/AF

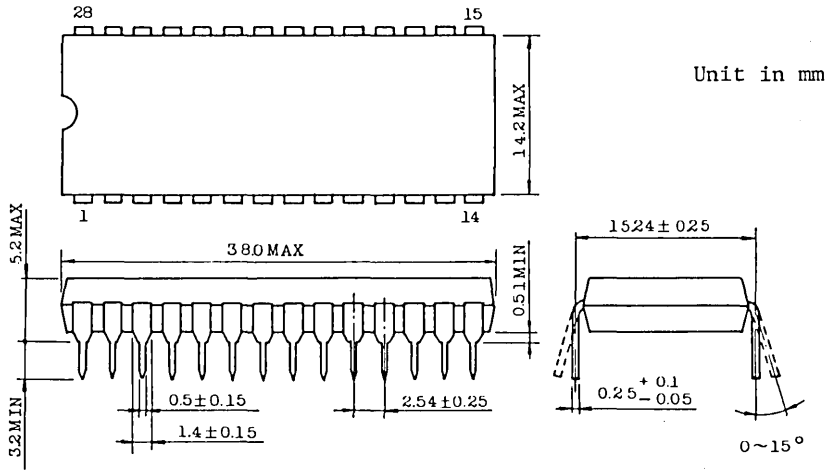
PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	0	1	0	52

Notes: A9=12V±0.5V
A1~A8, A10~A12, $\overline{CE}$, $\overline{OE}$=V_{IL} $\overline{PGM}$=V_{IH}

HIGH SPEED PROGRAM MODE FLOW CHART

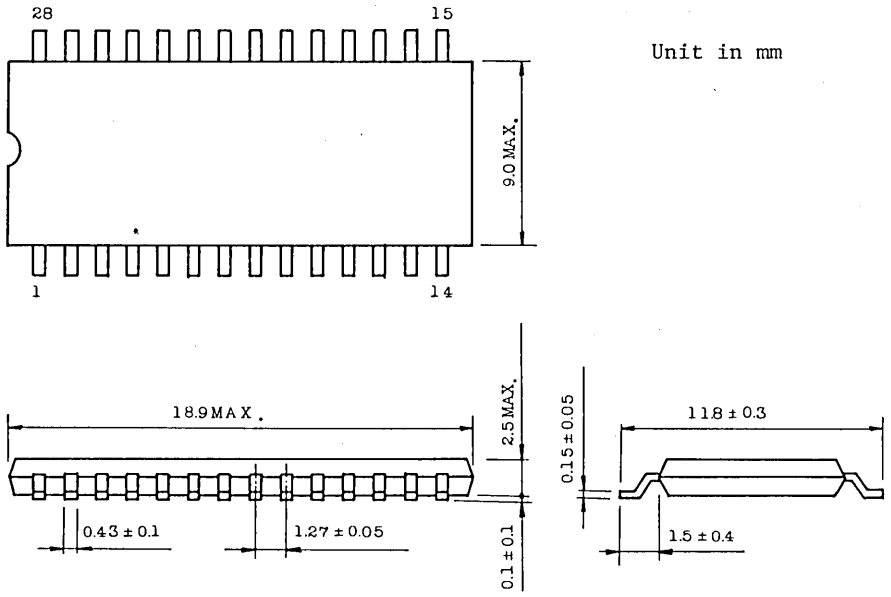


OUTLINE DRAWINGS (TMM2464AP)



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal positson with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM2464AF)



Note : Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

TMM24128AP/AF 16,384 WORD × 8 BIT
ONE TIME PROGRAMMABLE READ ONLY MEMORY
N CHANNEL SILICON STACKED GATE MOS

TMM24128AP/AF

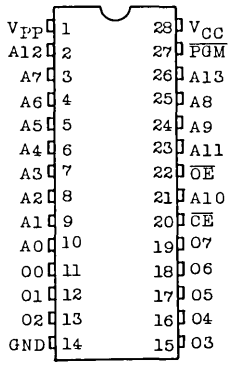
DESCRIPTION

The TMM24128AP/AF is a 16,384 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic DIP. TMM24128AP/AF's access time is 200ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TMM27128AD's. Once programed, the TMM24128AP/AF can not be erased because of using plastic DIP without transparent window.

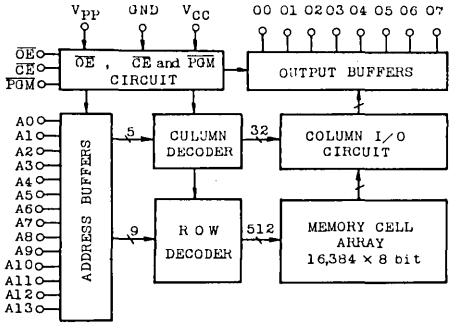
FEATURES

- Single 5 volt power supply
- Fast access time : 200ns(Max.)
- Power dissipation : 100mA(active current) Max.
  30mA(standby current) Max.
- Low power standby mode : $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Full static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Compatible with TMM27128AD and MASK ROM TMM23128P
- 28 PIN standard plastic package: TMM24128AP
- 28 PIN flat package : TMM24128AF

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{13}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG.}$	Storage Temperature	−55~150	°C
$T_{OPR.}$	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	−	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	−	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS

(Ta=0~70°C, V_{CC}=5V±5%, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	100	mA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6V	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V~V_{CC}	—	—	±10	μA

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 2.0V \sim V_{CC} + 0.6V$, Unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	–	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	–	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	ns
t_{OH}	Output Data Hold Time	0	–	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

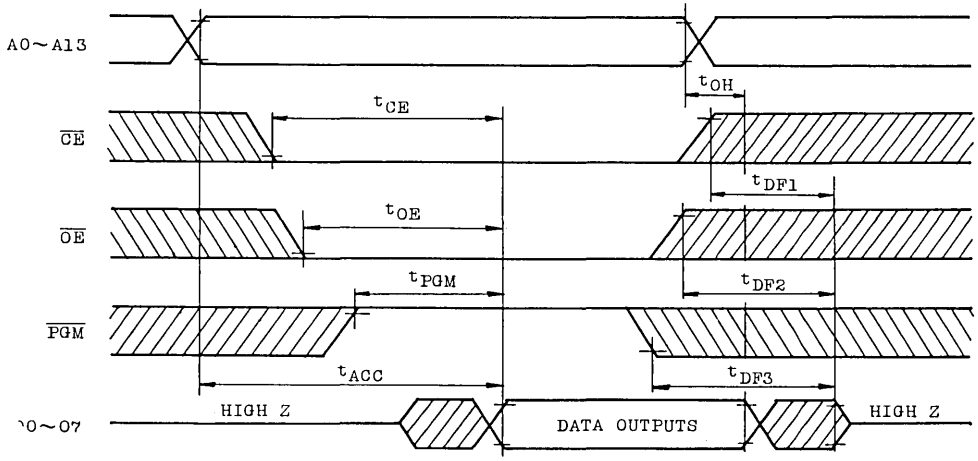
CAPACITANCE

* ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	–	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	–	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

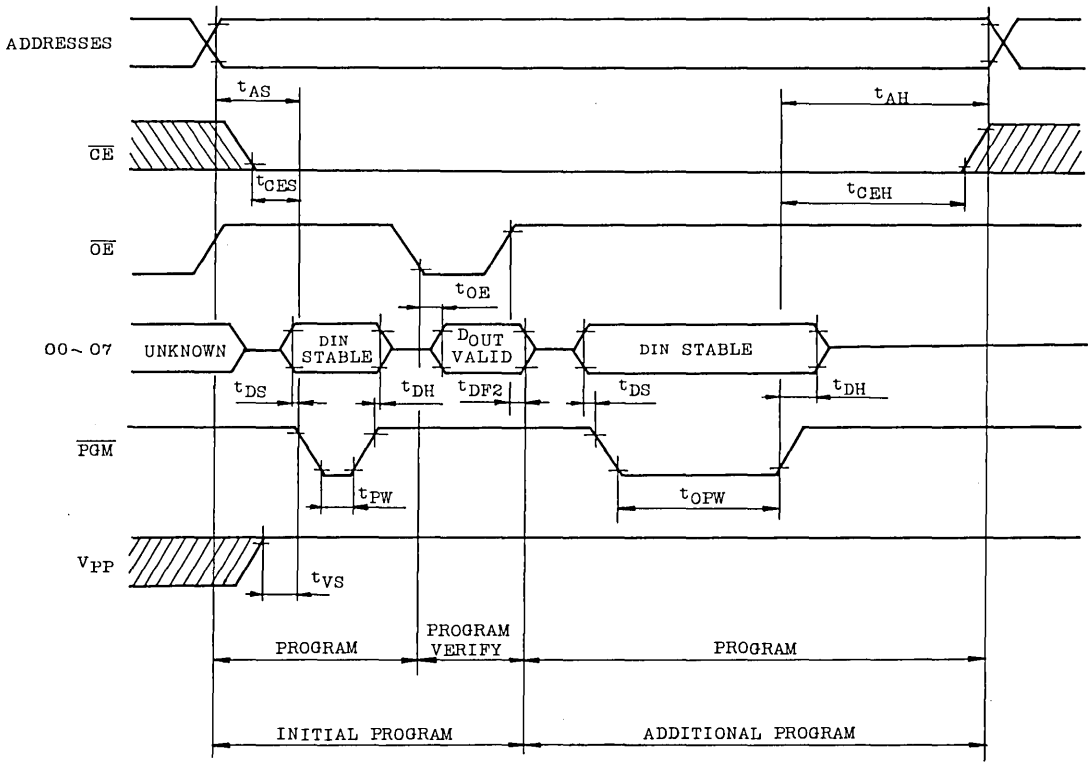
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. t_{OPW} depend on the program pulse width which is reguired in the initial program.

TIMING WAVEFORMS (HIGH SPEED PROGMAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM24128AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES(NUMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM24128AP/AF has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{LL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{LL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TMM24128AP/AF can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM24128AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying TTL high level to the $\overline{CE}$ input, the TMM24128AP/AF is placed in the standby mode which reduce the operating current from 100mA to 30mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM24128AP/AF from being programmed. Programming of two or more TMM24128AP/AF in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGMAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$=V_{IH}. The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24128AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24128AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

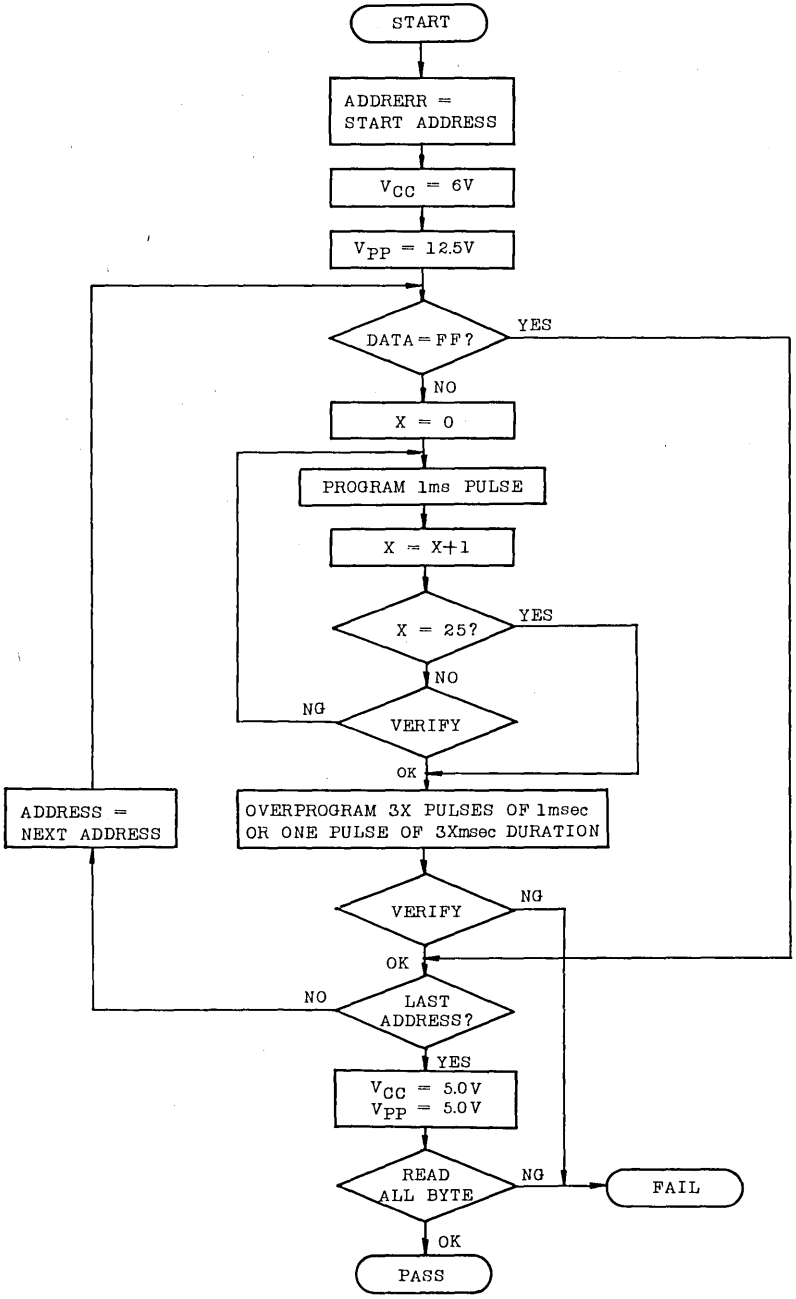
Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM24128AP/AF.

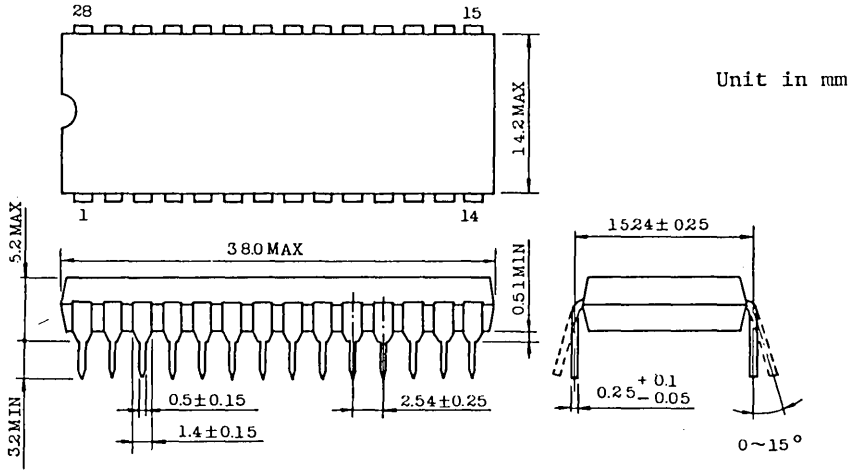
PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	1	0	0	1	1	D3

Notes: A9=12V±0.5V
A1~A8, A10~A13, $\overline{CE}$, $\overline{OE}$=V_{IL} $\overline{PGM}$=V_{IH}

HIGH SPEED PROGRAM MODE FLOW CHART

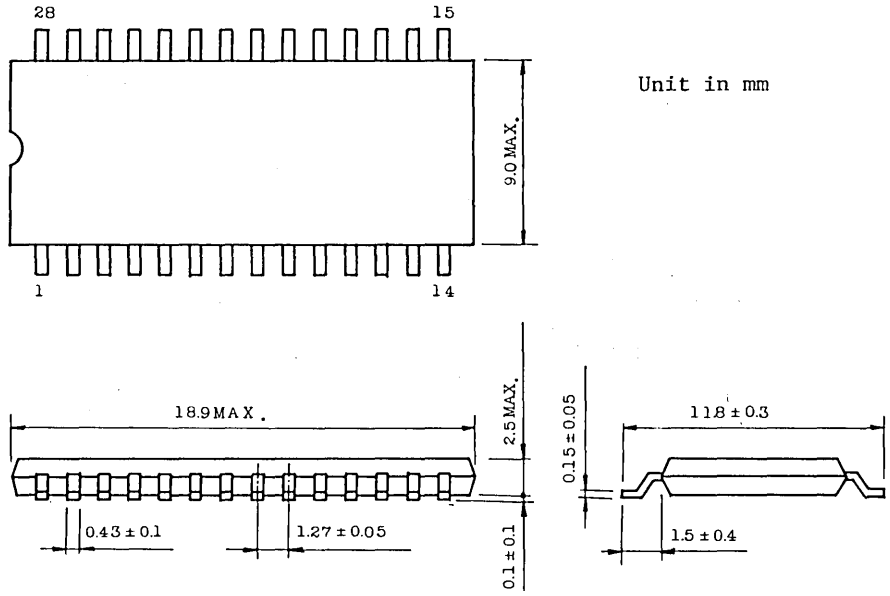


OUTLINE DRAWINGS (TMM24128AP)



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM24128AF)



Note: Lead picth is 1.27 and tolerance is±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

TMM24256AP/AF 32,763 WORD × 8 BIT
ONE TIME PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM24256AP/AF

DESCRIPTION

The TMM24256AP/AF is a 32,768 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic Package.

The TMM24256AP/AF's access time is 200ns and has low power standby mode which reduces the power dissipation without increasing access time.

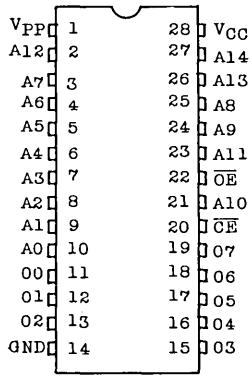
The electrical characteristics and programming method are the same as U.V. EPROM TMM27256AD's.

Once programed, the TMM24128AP/AF can not be erased because of using plastic DIP without transparent window.

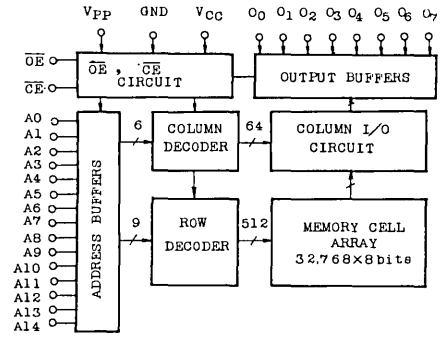
FEATURES

- Fast access time : 200ns
- Low power dissipation
  Active : 100mA
  Standby : 30mA
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD and TC57256D
- Standard 28 pin DIP plastic package : TMM24256AP
- Plastic Flat Package : TMM24256AF

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STG.}$	Storage Temperature	−55~150	°C
$T_{OPR.}$	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	−	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	−	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	100	mA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6V	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V~V_{CC}	—	—	±10	μA

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%, V_{PP}=2.0V~V_{CC}+0.6V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	–	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	–	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	–	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	–	ns

A. C. TEST CONDITIONS

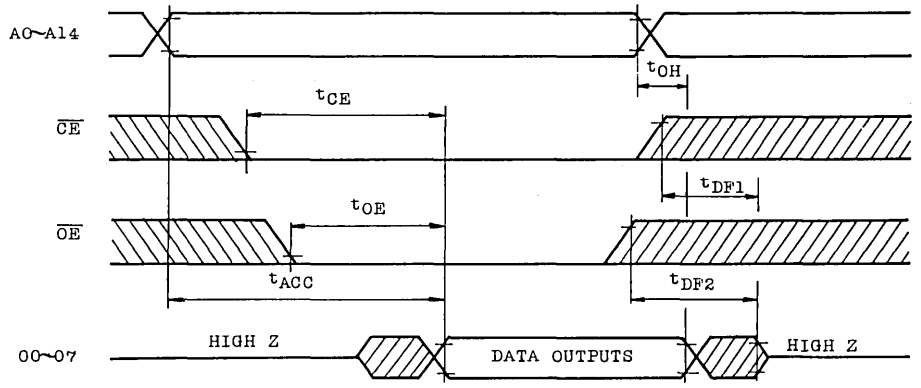
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	—	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



High speed PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A_9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	ns
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	—	—	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	—	—	130	ns

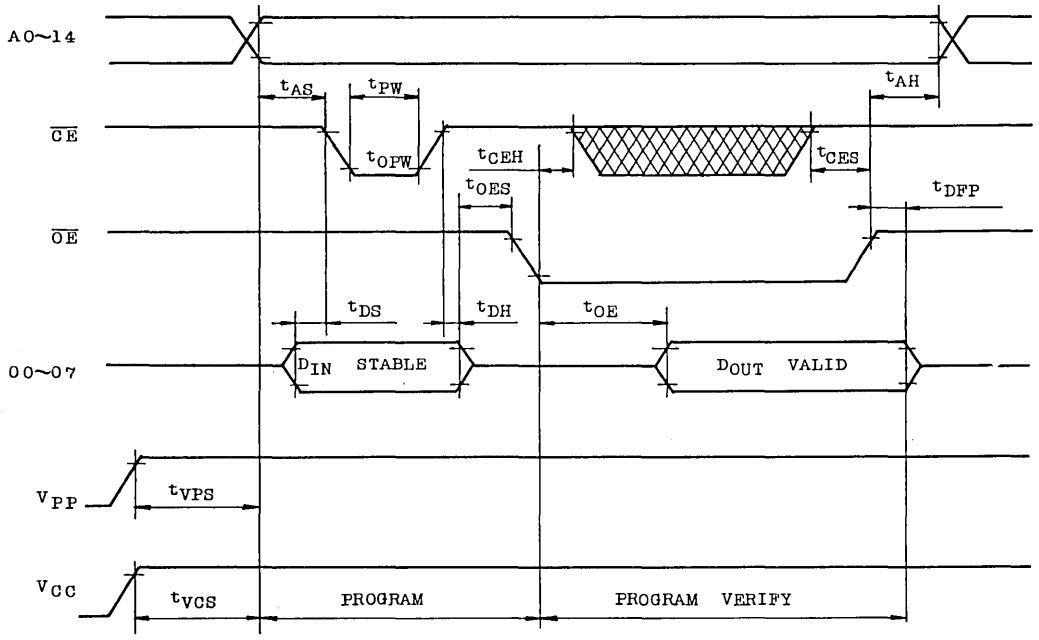
A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1 : The length of the overprogram pulse may very as a fumction of the counter value X.

TIMING WAVEFORMS(PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM24256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	Active
	Program Verify	*	L			Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM24256AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection.

Assuming the $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TMM24256AP/AF's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM24256AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TMM24256AP/AF is placed in the standby mode which reduce the operating current to 30mA from 100mA (about 70% reduction) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM24256AP/AF from being programmed.

Programming of two or more TMM24256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGMAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24256AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

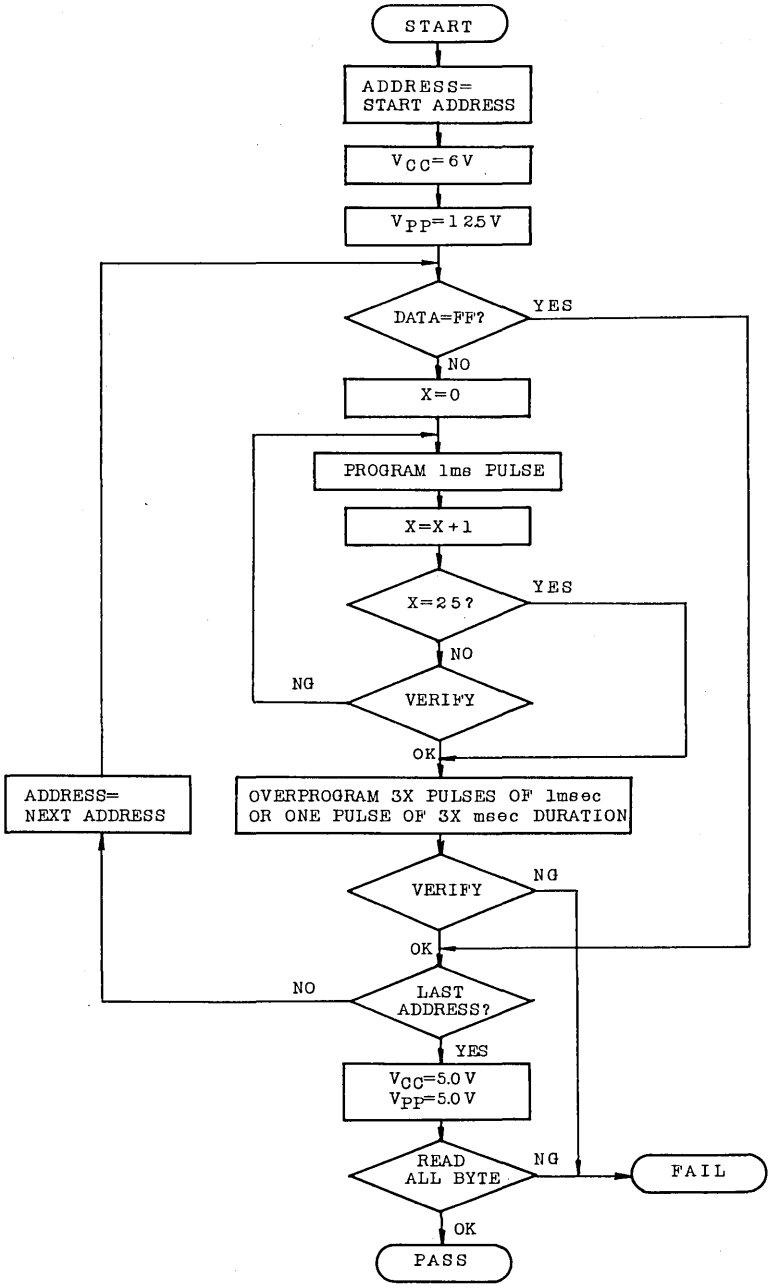
The following table shows electric signature of TMM24256AP/AF.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

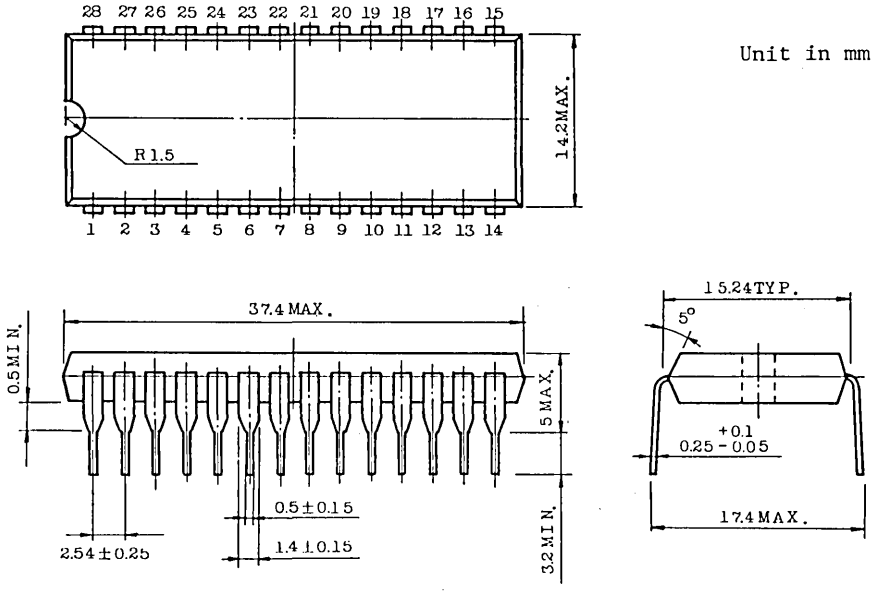
Notes: A9=12V±0.5V

A1~A8, A10~A14, $\overline{CE}$, $\overline{OE}$=V_{IL}

HIGH SPEED PROGRAM MODE FLOW CHART



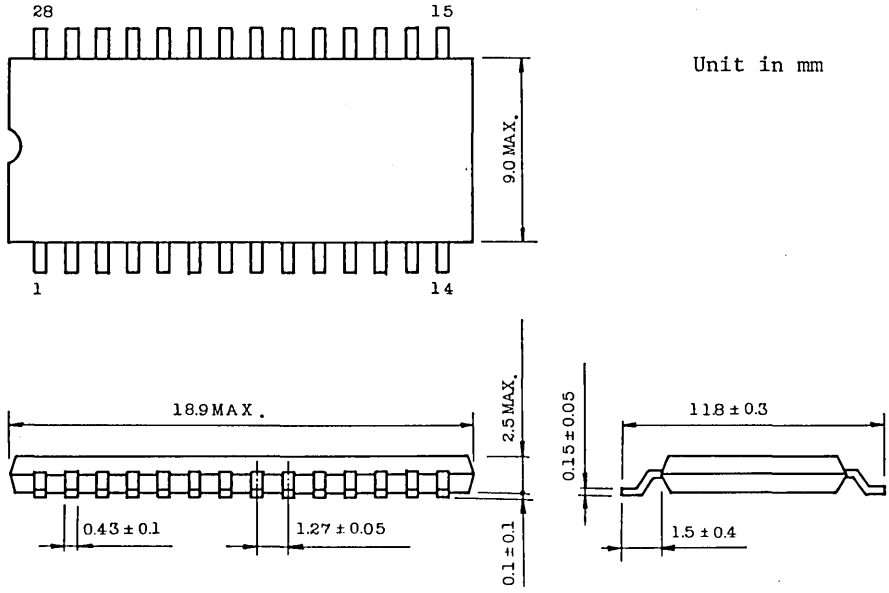
OUTLINE DRAWINGS (TMM24256AP)



Unit in mm

Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM24256AF)



Note: Lead picth is 1.27 and tolerance is±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

TC54256AP/AF

32.768 WORD x 8 BIT COMS ONE TIME PROGRAMMABLE READ ONLY MEMORY

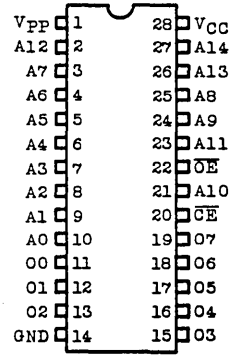
DESCRIPTION

The TC54256AP/AF is a 32,768 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic package. The TC54256AP/AF's access time is 200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC57256AD's. Once programed, the TC54256AP/AF can not be erased because of using plastic DIP without transparent window.

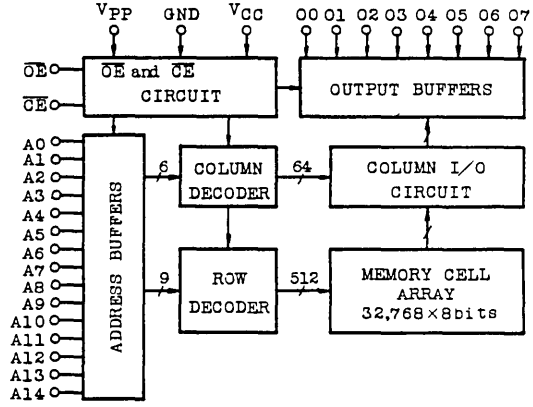
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  Active : 40mA/6.7MHz
  Standby: 100μA
- Fast access time: 200ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, TC57256D/AD, One time PROM TMM24256P/AP and TC54256P
- Standard 28 pin DIP plastic package: TC54256AP
- Plastic Flat Package : TC54256AF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A14	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	$-0.6 \sim 7.0$	V
V_{PP}	Program Supply Voltage	$-0.6 \sim 14.0$	V
V_{IN}	Input Voltage	$-0.6 \sim 7.0$	V
$V_{I/O}$	Input/Output Voltage	$-0.6 \sim V_{CC}+0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	$-65 \sim 125$	°C
T_{OPR}	Operating Temperature	$-40 \sim 85$	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	Vpp Power Supply Voltage	$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	

D.C. and OPERATING CHARACTERISTICS (Ta=$-40 \sim 85$°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0V $\sim V_{CC}$		-	-	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}$=0V	f=6.7MHz	-	-	40	mA
I_{CCO2}			f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}=V_{IH}$		-	-	1	mA
I_{CCS2}		$\overline{CE}=V_{CC}-0.2V$		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	Vpp Current	$V_{PP}=V_{CC}$±0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V $\sim V_{CC}$		-	-	±10	μA

A.C. CHARACTERISTICS (Ta=-40 ∿ 85°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	
t_{OH}	Output Data in Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	

A.C. TEST CONDITIONS

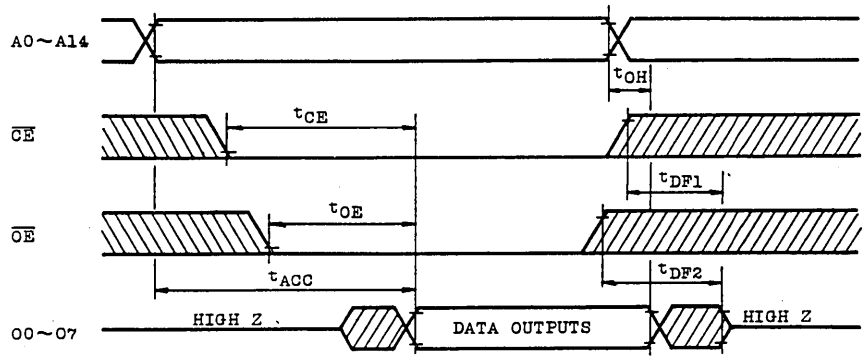
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	130	ns

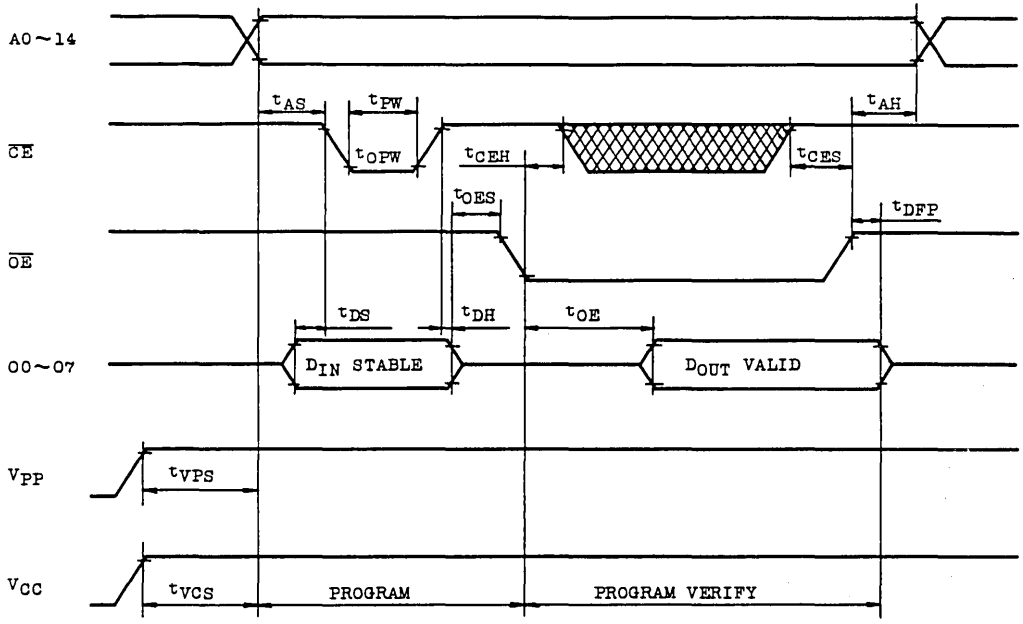
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC54256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=-40 ∿ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC54256AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TC54256AP/AF's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54256AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC54256AP/AF is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54256AP/AF are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TC54256AP/AF is in the programming mode when the Vpp input is at 12.5V and $\overline{CE}$ is at TTL-Low level under $\overline{OE}=V_{IH}$.
The TC54256AP/AF can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL}.

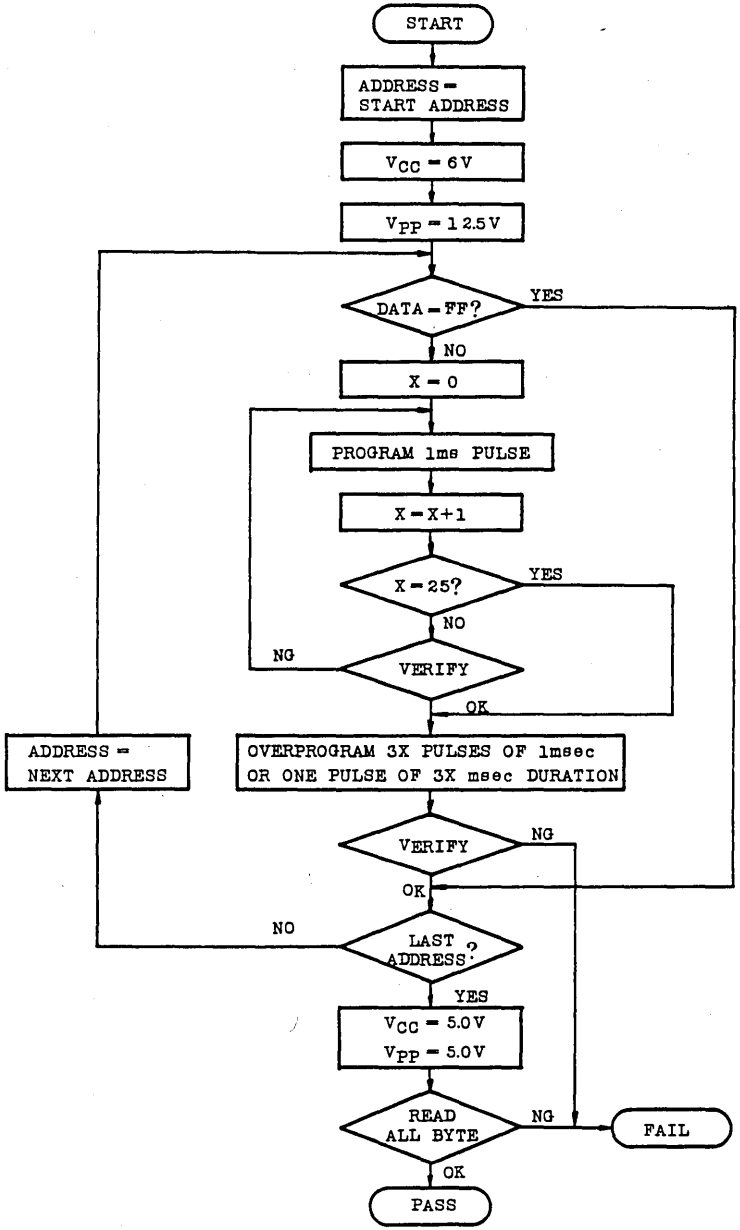
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to Vpp terminal, a TTL high level $\overline{CE}$ input inhibits the TC54256AP/AF from being programmed. Programming of two or more TC54256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the Vpp terminal with $V_{CC}=6V$.
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with $V_{CC}=Vpp=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54256AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7). The following table shows electric signature of TC54256AP/AF.

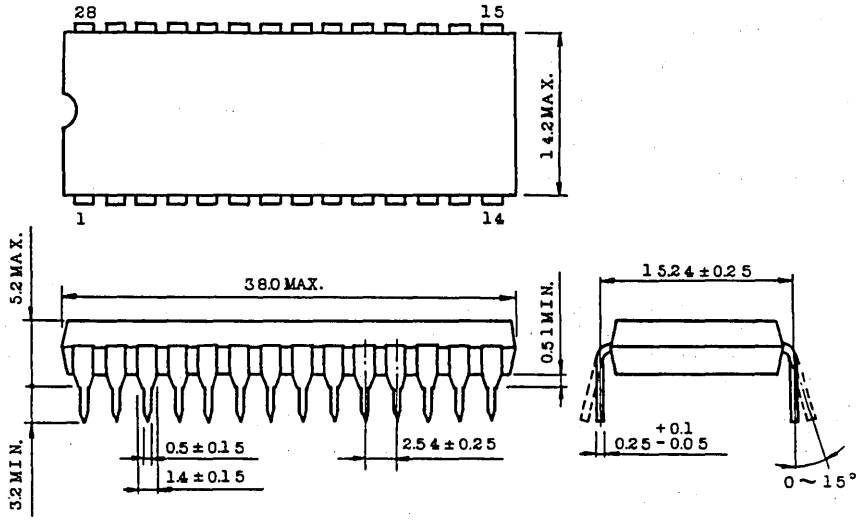
PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS (TC54256AP)

Unit in mm



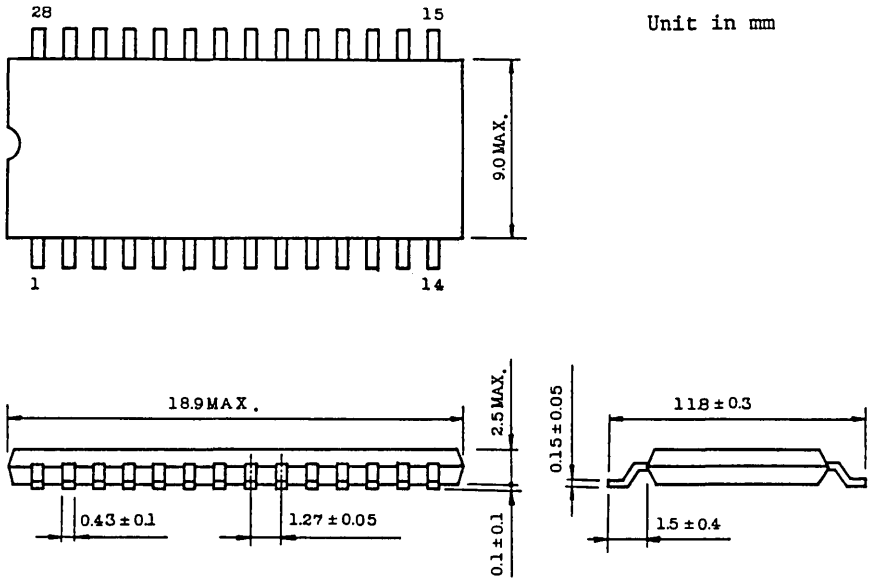
Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TC54256AF)

Unit in mm



Note: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TMM24512P/F

TMM24512P/F 65,536 WORD x 8 BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY

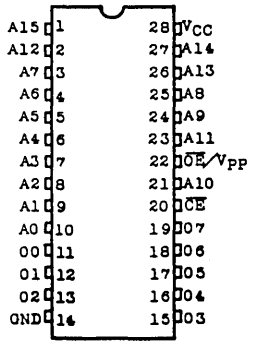
DESCRIPTION

The TMM24512P/F is a 65,536 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic package. The TMM24512P/F's access time is 250ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TMM27512D's. Once programed, the TMM24512P/F can not be erased because of using plastic DIP without transparent window.

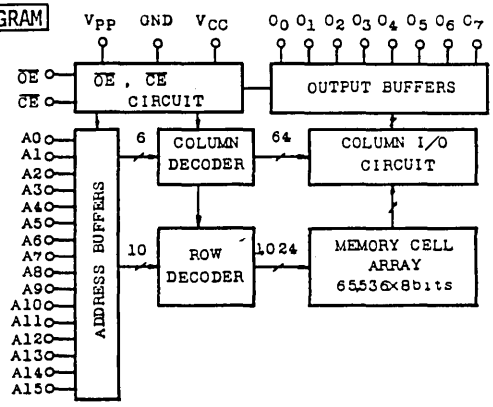
FEATURES

- Fast access time: 250ns
- Low power dissipation
  - Active : 120mA
  - Standby: 35mA
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with TMM27512D
- Standard 28 pin DIP plastic package: TMM24512P
- Plastic Flat Package : TMM24512F

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A15	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	V_{PP}	6V	Data In	Active
Program Inhibit	H	V_{PP}		High Impedance	
Program Verify	L	L		Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ 7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature	260 • 10	°C•sec
T_{STG}	Storage Temperature	-55 ∿ 150	°C
T_{OPR}	Operating Temperature	0 ∿ 70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	

D.C. and OPERATING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{CC}=5V \pm 5\%$)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{IH}$	-	-	35	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}=V_{IL}$	-	-	120	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=0 \sim V_{CC}+0.6V$	-	-	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4V \sim V_{CC}$	-	-	±10	μA

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{CC}=5V \pm 5\%$, $V_{PP}=2.0V \sim V_{CC}+0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	UNIT
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	250	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	100	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	90	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	90	
t_{OH}	Output Data in Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	

A.C. TEST CONDITIONS

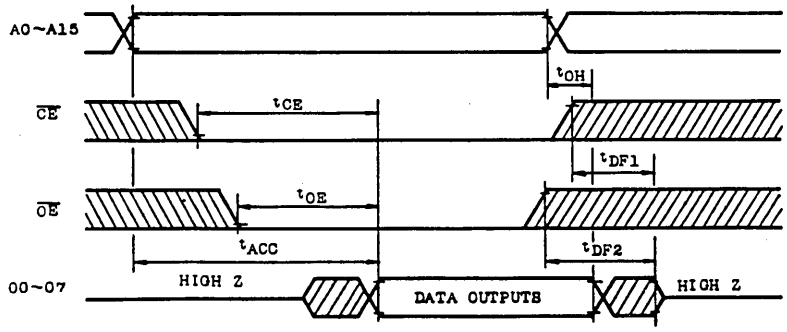
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : $0.45V \sim 2.4V$
- Timing Measurement Reference Level: Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * ($Ta=25°C$, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN}=0V$	-	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN}=0V$	-	50	60	
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	-	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	130	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}$/V_{PP} Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}$/V_{PP} Hold Time	-	2	-	-	μs
t_{PRT}	$\overline{OE}$/V_{PP} Pulse Rise Time	-	50	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VR}	$\overline{OE}$/V_{PP} Recovery Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$/V_{PP}=V_{PP}	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}$/V_{PP}=V_{IL}	-	-	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$/V_{PP}=V_{IL}	-	-	130	ns

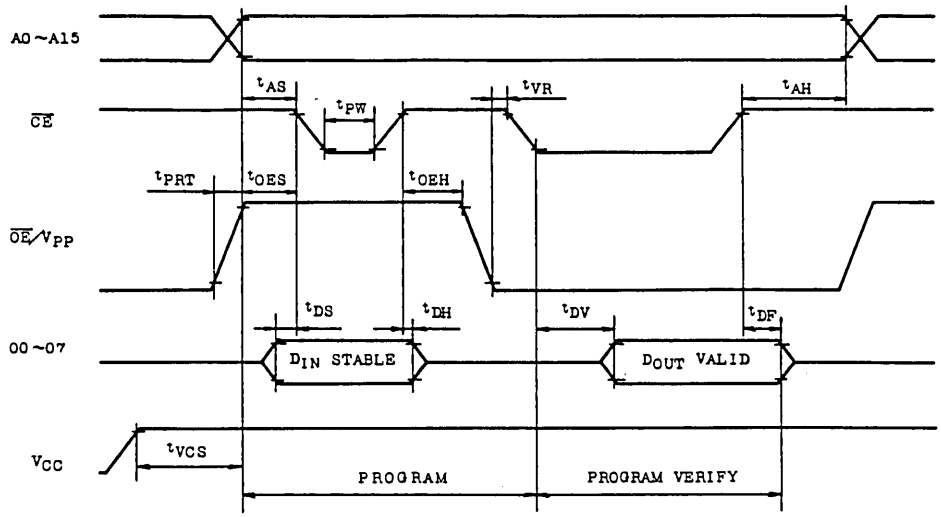
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.

2. Removing the device from socket and setting the device in socket with Vpp=12.5V may cause permanent damage to the device.

3. The Vpp supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM24512P/F's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	$O_0 \sim O_7$ (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=0 ∿ 70°C)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	
	Standby	H	*		High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	V_{PP}	6V	Data In	Active
	Program Inhibit	H	V_{PP}		High Impedance	
	Program Verify	L	L		Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TMM24512P/F has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming the $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TMM24512P/F's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM24512P/F has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TMM24512P/F is placed in the standby mode which reduce the operating current to 35mA from 120mA (about 70% reduction) by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM24512P/F are in the "1" state which is erased state. Therefore the program operation is to introduce "0" data into the desired bit locations by electrically programming. The TMM24512P/F is in the programming mode when the $\overline{OE}$/Vpp input is at 12.5V and $\overline{CE}$ is at TTL-Low level. The TMM24512P/F can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{CE}$ at V_{IL} and $\overline{OE}$/Vpp at V_{IL}.

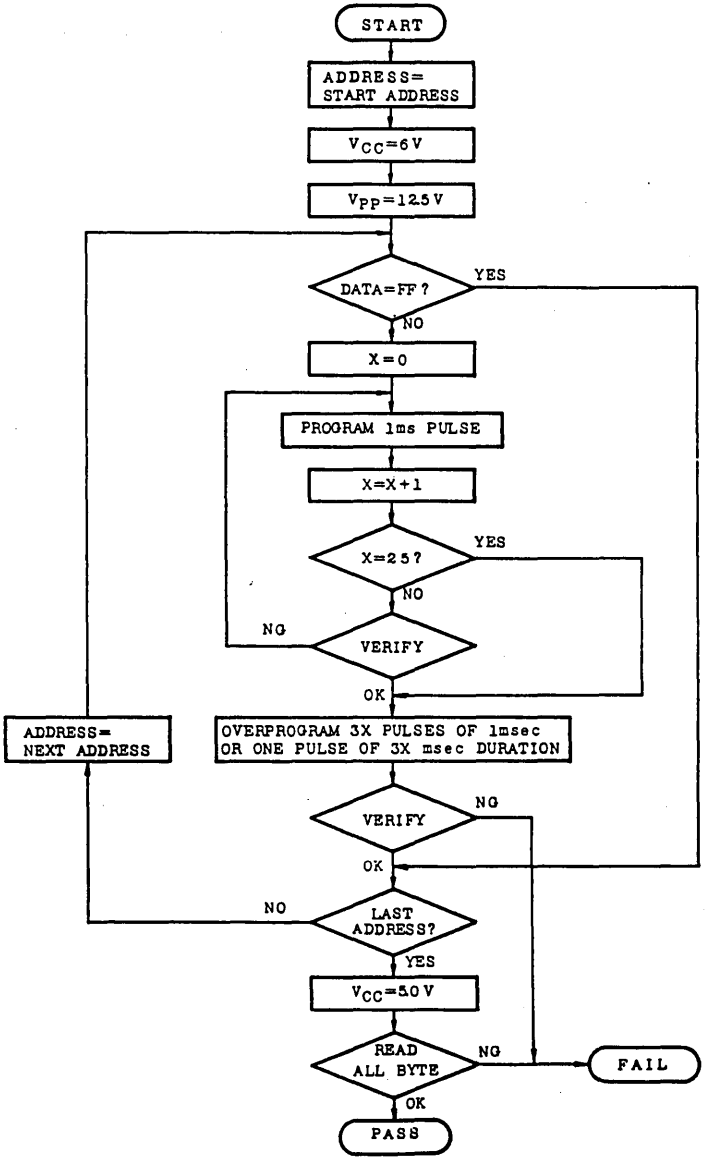
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to Vpp terminal, a TTL high level $\overline{CE}$ input inhibits the TMM24512P/F from being programmed. Programming of two or more TMM24512P/F's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the Vpp terminal with V_{CC}=6V. The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with V_{CC}=5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24512P/F which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24512P/F by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

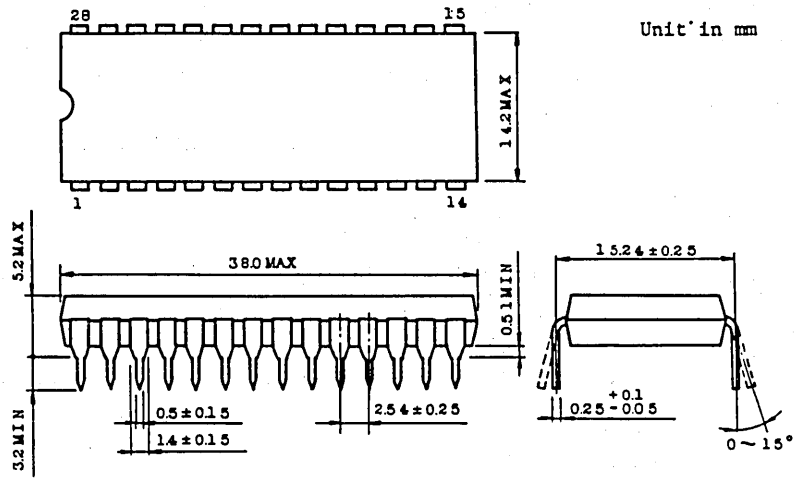
The following table shows electric signature of TMM24512P/F.

PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	1	0	1	0	1	15

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A15, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS (TMM24512P)

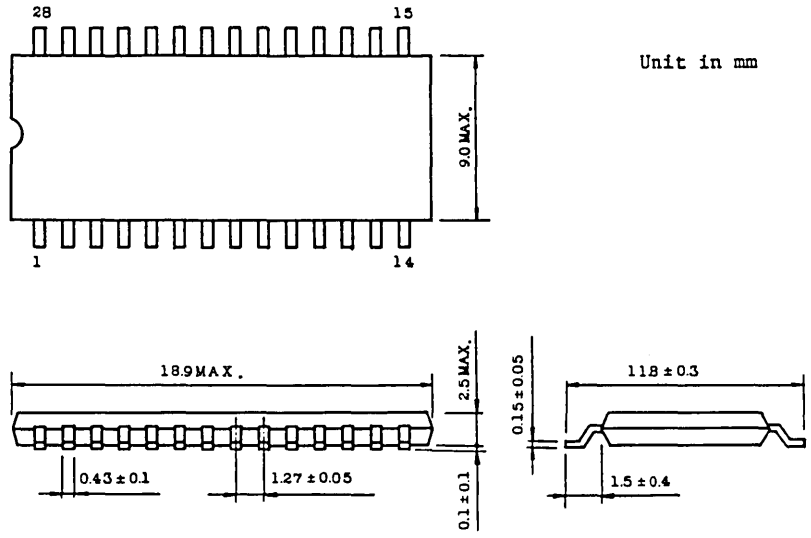


Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM24512F)



Unit in mm

Note: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

Read Only Memories

256K BIT (32K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE MOS

TC53257P
TC53257F

DESCRIPTION

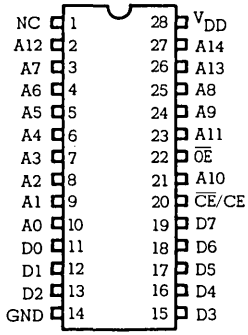
The TC53257P/F is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, this being suitable for use in program memory of microprocessor, and in character generator. The TC53257P/F using CMOS technology is most suitable for low power applications where battery operation is required.

The TC53257P/F has one programmable chip enable input $\overline{CE}$/CE, for device selection and one output enable input ($\overline{OE}$) for fast memory access and output control.

FEATURES

- Single 5V Power Supply
- Access Time : 200ns(Max.)
- Power Dissipation
  Operating Current : 25mA(Max.)
  Standby Current : 20μA(Max.)
- Pin Compatible with 256K EPROM TC57256D
- Full Static Operation
- Programmable Chip Enable
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Package
  Plastic DIP : TC53257P
  Plastic FP : TC53257F

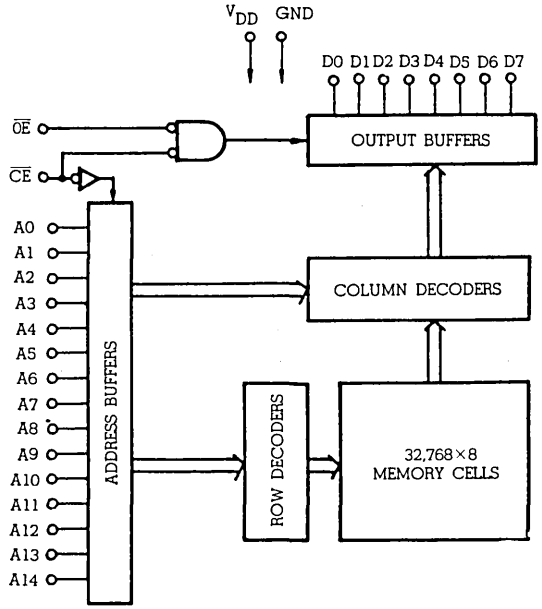
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{14}	Address Inputs
D_0~D_7	Data Outputs
NC	No connection
$\overline{CE}$/CE	Chip enable input
$\overline{OE}$	Output enable input
V_{DD}	Power supply
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−0.5~7.0	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0 0.6*	W
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	−40~85	°C
T_{SOLDER}	Soldering Temperature·Time	260·10	°C·sec

Note : *Plastic FP

D. C. OPERATING CONDITINS (Ta = −40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V

D. C. and OPERATING CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0V~V_{DD}	—	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} V_{OUT} = 0V~V_{DD}	—	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	3.2	—	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} CE = V_{IL}	—	2	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} − 0.2V, CE = 0.2V	—	20	μA
I_{DDO1}	Operating Current	V_{IH} = $V_{IH\ VIL}$, t_{CYCLE} = 200ns	—	40	mA
I_{DDO2}		V_{IN} = V_{DD} − 0.2V/0.2V, t_{CYCLE} = 200ns	—	25	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	—	8	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	—	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

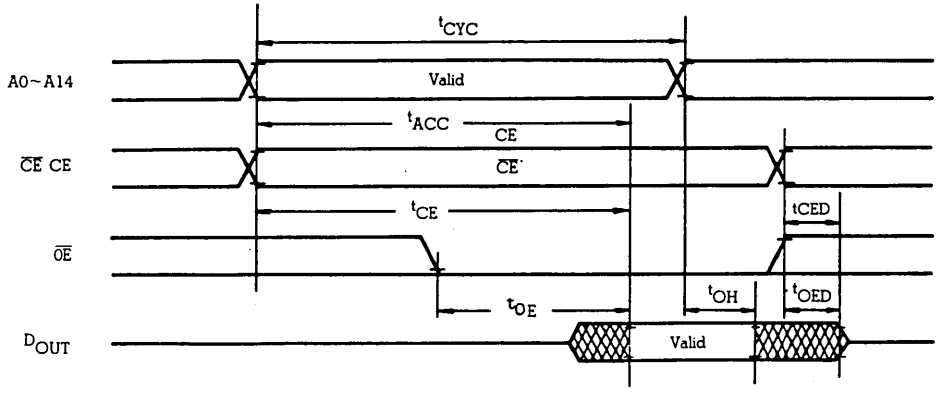
A. C. CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	200	—	ns
t_{ACC}	Access Time	—	200	ns
t_{CE}	Chip Enable Access Time from CE/$\overline{CE}$	—	200	ns
t_{OE}	Output Enable Access Time from $\overline{OE}$	—	70	ns
t_{CED}, t_{OED}	Output Disable Time from CE/$\overline{CE}$, $\overline{OE}$	0	60	ns
t_{OH}	Output Hold Time	0	—	ns

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL
Input Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V, 2.2V
Output : 0.8V, 2.2V
Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



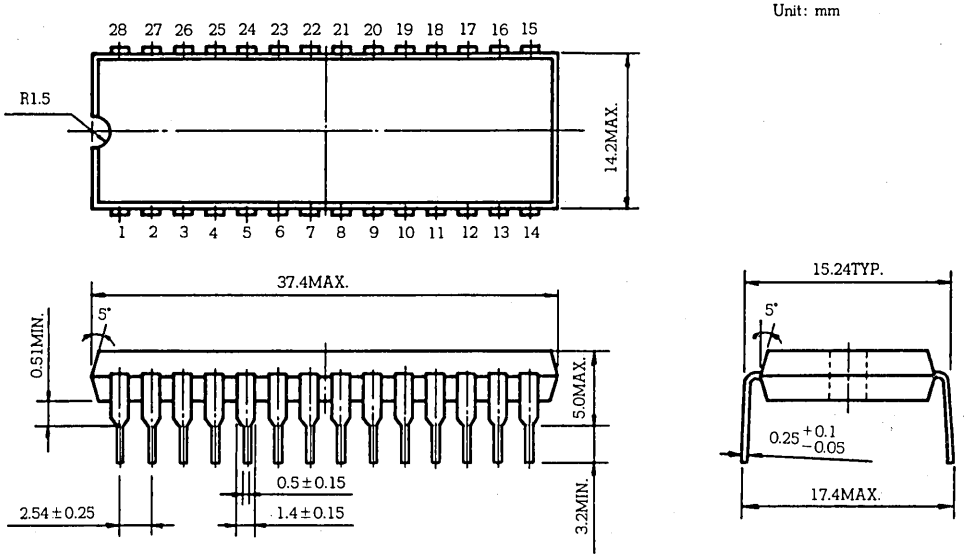
OPERATION MODE H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

MODE	$\overline{CE}$(CE)	$\overline{OE}$	$A_{0\sim14}$	Outputs	Power
Read	L(H)	L	Valid	Data out	Operating
Output Deselect	L(H)	H	*	High-Z	Operating
	H(L)	*	*		Standby

OUTLINE DRAWINGS

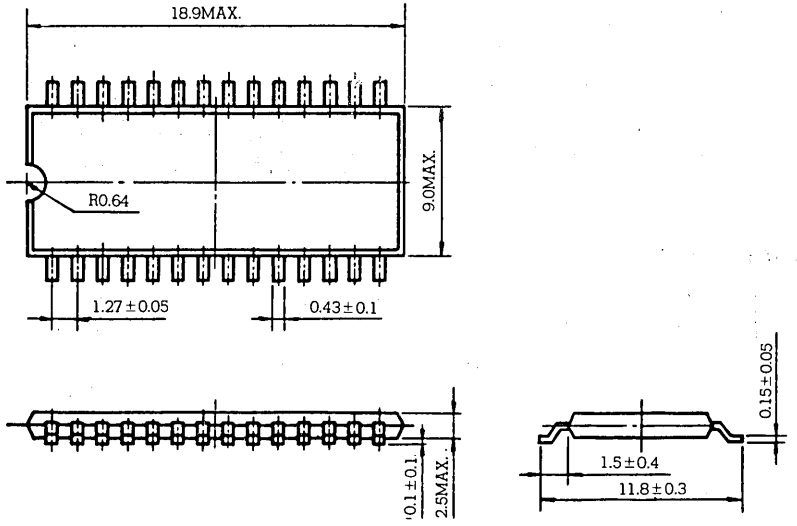
● Plastic DIP

Unit: mm



NOTE : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

● Plastic FP



NOTE : Each lead pitch is 1.27mm.
All leads are located within 0.12mm of their true longitudinal position with respect to No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

1M BIT (128K WORD × 8 BIT)
CMOS MASK ROM
SILICON GATE CMOS

TC531000AP
TC531000AF

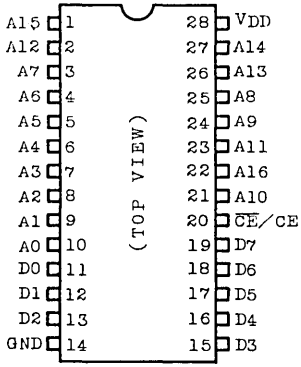
DESCRIPTION

The TC531000AP/AF is a 1,048,576 bits read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, especially character generator. The TC531000AP/AF using CMOS technology is most suitable for low power applications where battery operation are required. The TC531000AP/AF has one chip enable input $\overline{CE}$/CE, programmable for device selection.

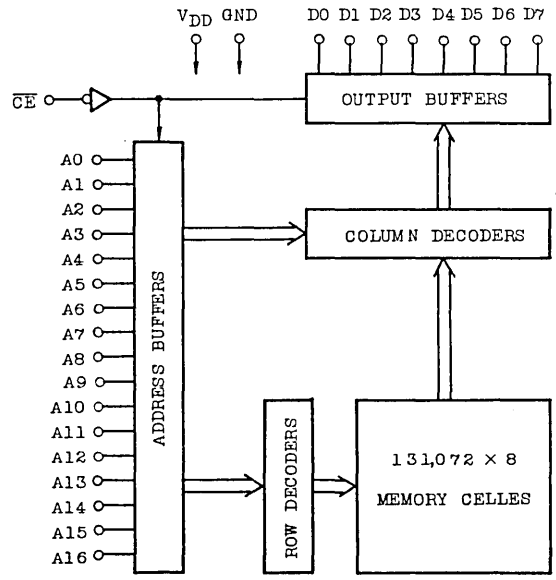
FEATURES

- Single 5V Power Supply
- Access Time: 150ns (Max.)
- Power Dissipation
  - Operating Current: 40mA (Max.)
  - Standby Current : 20μA (Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- Package Plastic DIP: TC531000AP
  Plastic FP : TC531000AF

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A16	Address Inputs
D0 ∿ D7	Data Outputs
$\overline{CE}$/CE	Chip Enable Input
V_{DD}	Power Supply
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ∿ 7.0	V
V_{IN}	Input Voltage	-0.5 ∿ V_{DD}	V
V_{OUT}	Output Voltage	0 ∿ V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	-55 ∿ 150	°C
T_{OPR}	Operating Temperature	-40 ∿ 70	°C
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C•sec

Note: * Plastic FP

D.C. OPERATING CONDITIONS (Ta=-40 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta=-40 ∿ 70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0 ∿ V_{DD}	-	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH}, V_{OUT}=0 ∿ V_{DD}	-	±5.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	-1.0	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	2.0	-	mA
I_{DDS1}	Standby Current	$\overline{CE}$=V_{IH}	-	2	mA
I_{DDS2}	Standby Current	$\overline{CE}$=V_{DD} and V_{IN}=0V (V_{DD})	-	20	μA
I_{DDO1}	Operating Current	V_{IN}=V_{IH}/V_{IL}, t_{cycle}=150ns	-	50	mA
I_{DDO2}		V_{IN}=V_{DD}/0V, t_{cycle}=150ns	-	40	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f=1MHz, Ta=25°C	-	10	pF
C_{OUT}	Output Capacitance	f=1MHz, Ta=25°C	-	10	

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (V_{DD}=5V±10%, Ta=-40 ∿ 70°C)

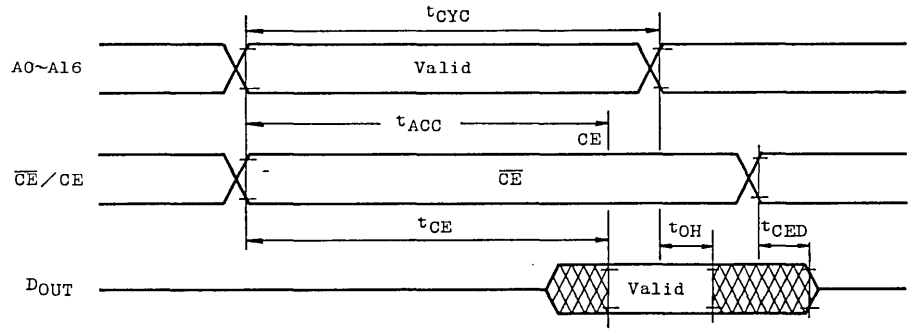
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	-	ns
t_{ACC}	Access Time	-	150	ns
t_{CE}	Chip Enable Access Time	-	150	ns
t_{CED}	Output Disable Time	-	50	ns
t_{OH}	Output Hold Time	0	-	ns

AC TEST CONDITIONS

- Output Load : 100pF + 1TTL
- Input Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels

  Input : 0.8V, 2.2V
  Output: 0.8V, 2.0V
- Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATION MODE

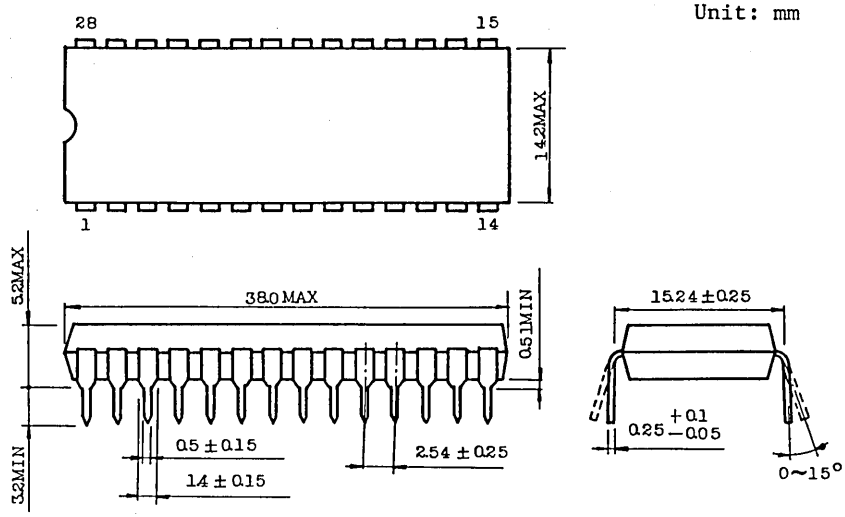
MODE	$\overline{CE}$(CE)	A0 ∿ 16	Outputs	Power
Read	L(H)	Valid	Data Out	Operating
Output Deselect	H(L)	*	High-Z	Standby

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWINGS

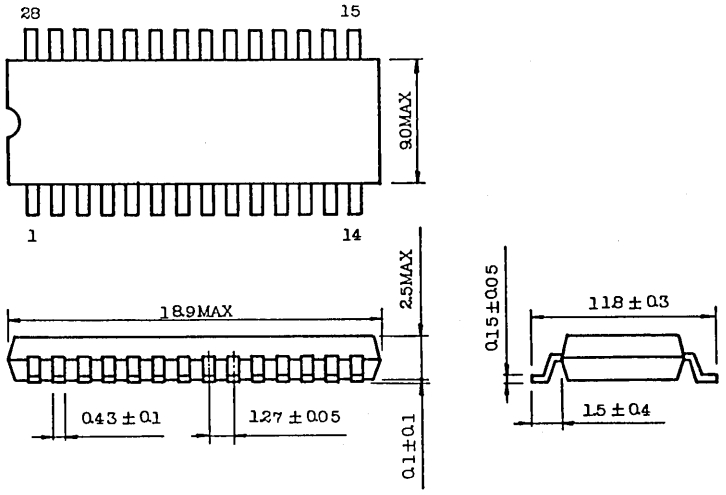
Plastic DIP

Unit: mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

Plastic FP



Note: Each lead pitch is 1.27mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCT

2M BIT (256K WORD×8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC532000P

DESCRIPTION

The TC532000P is a 2,097, 152 bits read only memory organized as 262, 144 words by 8 bits with a low bit cost thus being suitable for use in program memory of microprocessor, especially character generator. The TC532000P using CMOS technoloby is most suitable for low power applications where battery operation is required.

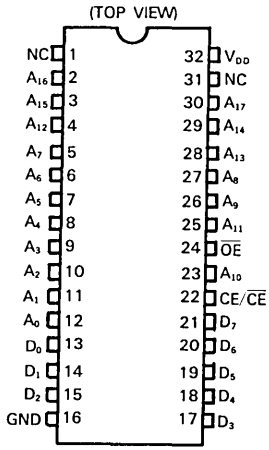
The TC532000P has one programmable chip enable input $\overline{CE}$/CE for device selection, and one output enable input $\overline{OE}$ for fast memory access and output control.

The TC532000P is moulded in a 32 pin standard plastic package, 0.6 inch in width.

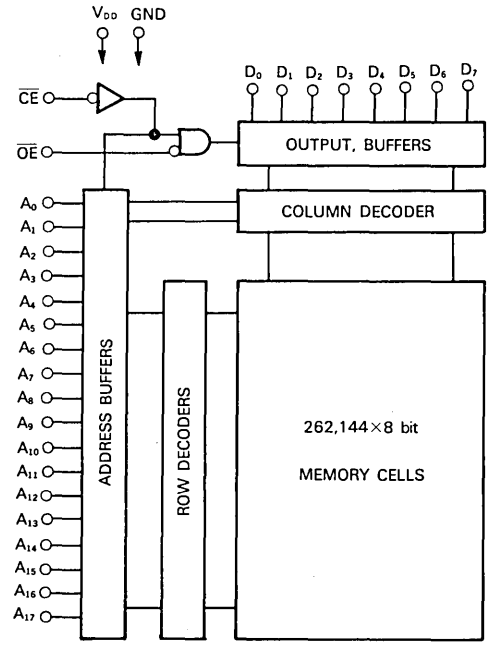
FEATURES

- Single 5V Power Supply
- Access Time: 200ns(Max.)
- Power Dissipetion
  - Operating Current : 30mA(Max.)
  - Standby Current : 20uA(Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 32pin 600mil width Plastic DIP
- Fully Static Operation
- Programmable Chip Enable

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A_0~A_{17}	Address inputs
D_0~D_7	Data outputs
$\overline{OE}$	Output Enable input
$\overline{CE}$/CE	Chip enable input
N.C.	No Conuection
V_{DD}	Power supply
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0	W
T_{STG}	Storage Temperature	−55~150	°C
T_{ORR}	Operating Temperature	−40~85	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note: *Plastic FP

D.C. OPERATING CONDITIONS

(Ta = −40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V

D.C. and OPERATING CHARACTERISTICS

(Ta = −40~85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	—	±1.0	uA
I_{LO}	Output Leakage Cunnent	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, V_{OUT} = OV~V_{DD}	—	±5.0	uA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	—	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	—	5	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} and V_{IN} = OV (V_{DD})	—	20	uA
I_{DDO1}	Operating Current	V_{IN} = V_{IH}/V_{IL}, t_{cycle} = 200ns, I_{OUT} = 0mA	—	40	mA
I_{DDO2}		V_{IN} = V_{DD}/OV, t_{cycle} = 200ns, I_{OUT} = 0mA	—	30	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	—	8	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	—	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

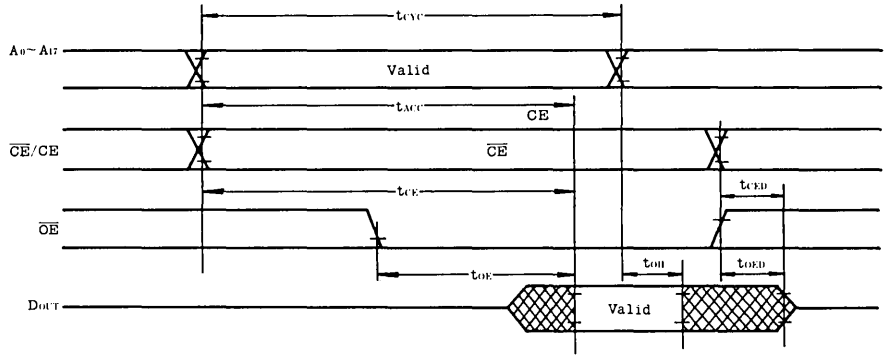
($Ta = -40 \sim 85°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	200	—	ns
t_{ACC}	Access Time	—	200	ns
t_{CE}	Chip Enable Access Time	—	200	ns
t_{OE}	Output Enable Access Time	—	70	ns
t_{CED}, t_{OED}	Output Disable Time	0	60	ns
t_{OH}	Output Hold Time	0	—	ns

AC TEST CONDITIONS

Output Load : 100pF+1TTL
Input Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V, 2.2V
Output : 0.8V, 2.0V
Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



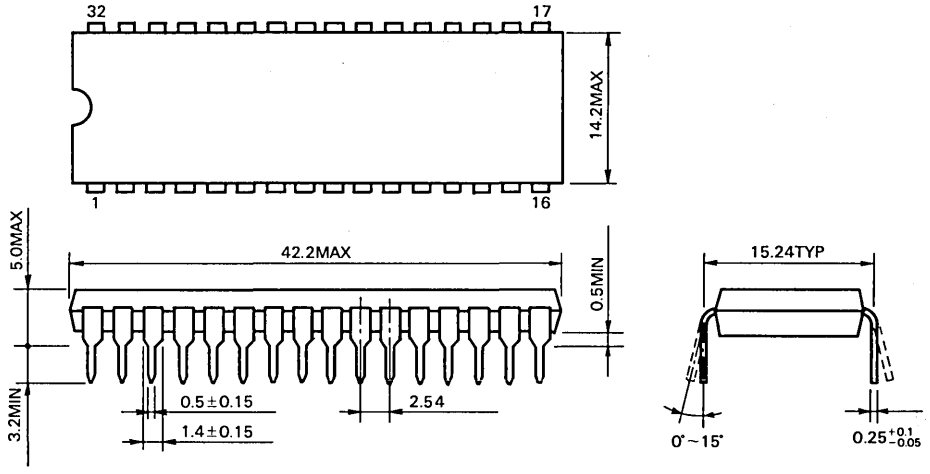
OPERATION MODE

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A_0-A_{17}	Outputs	Power
Read	L(H)	L	Valid	Data out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWINGS

Unit : mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.32 leads.

4M BIT (512K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC534000P

DESCRIPTION

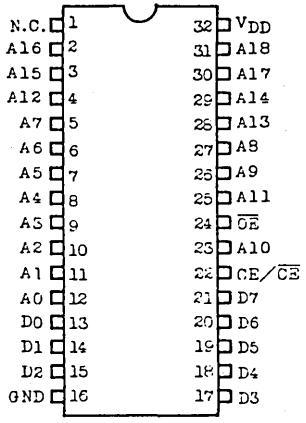
The TC534000P is a 4,194,304 bits read only memory organized as 524,288 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, and data memory, especially character generator. The TC534000P using CMOS technology is most suitable for low power applications where battery operations are required.
The TC534000P has one programmable chip enable input $\overline{CE}$/CE for device selection.
The TC534000P is moulded in a 32 pin standard plastic package, 0.6 inch in width.

FEATURES

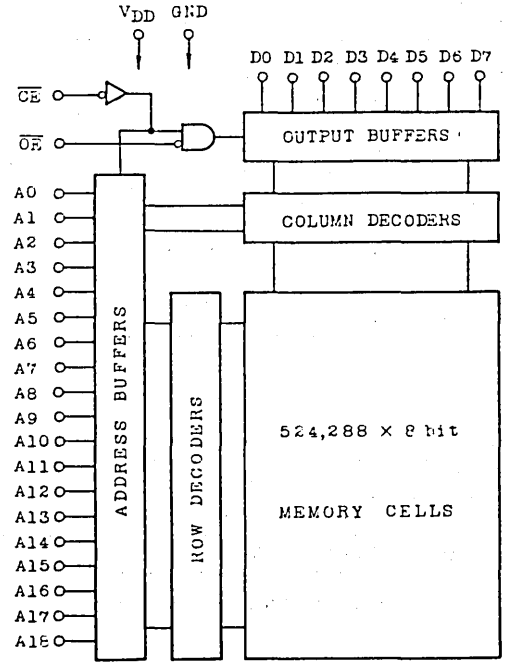
- Single 5V Power Supply
- Access Time: 250ns (Max.)
- Power Dissipation

  Operating Current: 30mA (Max.)
  Standby Current : 20μA (Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 32 pin 600 mil width Plastic DIP
- Fully Static Operation
- Programmable Chip Enable

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A18	Address Inputs
D0 ∿ D7	Data Outputs
$\overline{OE}$	Output Enable Input
CE/$\overline{CE}$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	$-0.5 \sim 7.0$	V
V_{IN}	Input Voltage	$-0.5 \sim V_{DD}$	V
V_{OUT}	Output Voltage	$0 \sim V_{DD}$	V
P_D	Power Dissipation	1.0	W
T_{STG}	Storage Temperature	$-55 \sim 150$	°C
T_{OPR}	Operating Temperature	$-40 \sim 85$	°C
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C•sec

D.C. OPERATING CONDITIONS (Ta=$-40 \sim 85$°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	
V_{IL}	Input Low Voltage	-0.3	-	0.8	

D.C. and OPERATING CHARACTERISTICS (Ta=$-40 \sim 85$°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$	-	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$, $V_{OUT}=0V \sim V_{DD}$	-	±5.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	-1.0	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	2.0	-	mA
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$	-	2	mA
I_{DDS2}	Standby Current	$\overline{CE}=V_{DD}$ and V_{IN}=0V(V_{DD})	-	20	μA
I_{DDO1}	Operating Current	$V_{IN}=V_{IH}/V_{IL}$, t_{cycle}=250ns	-	40	mA
I_{DDO2}		$V_{IN}=V_{DD}/0V$, t_{cycle}=250ns	-	30	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f=1MHz, Ta=25°C	-	8	pF
C_{OUT}	Output Capacitance	f=1MHz, Ta=25°C	-	10	

Note: This parameter is periodically sampled and is not 100% tested.

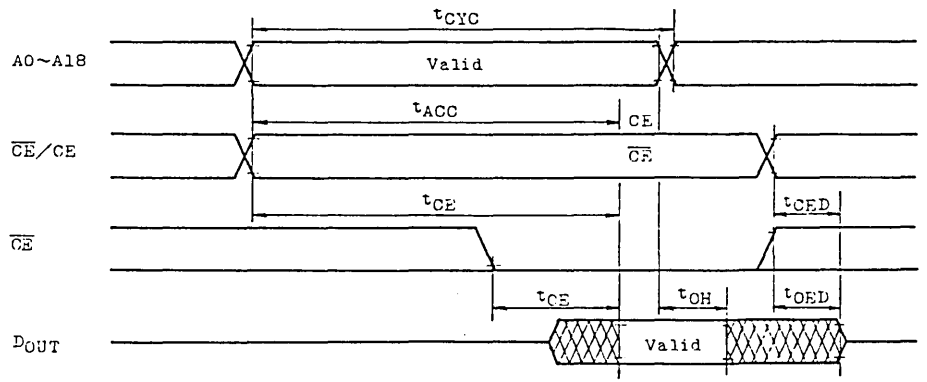
A.C. CHARACTERISTICS (Ta=-40 ∿ 85°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	250	-	ns
t_{ACC}	Access Time	-	250	
t_{CE}	Chip Enable Access Time	-	250	
t_{OE}	Output Enable Access Time	-	100	
t_{CED}	Output Disable Time	0	80	
t_{OED}	Output Disable Time from $\overline{OE}$	-	80	
t_{OH}	Output Hold Time	20	-	

AC TEST CONDITIONS

Output Load	:	100pF + 1TTL
Input Levels	:	0.6V, 2.4V
Timing Measurement Reference Levels	Input :	0.8V, 2.2V
	Output:	0.8V, 2.0V
Input Rise and Fall Time	:	5ns

TIMING WAVEFORMS



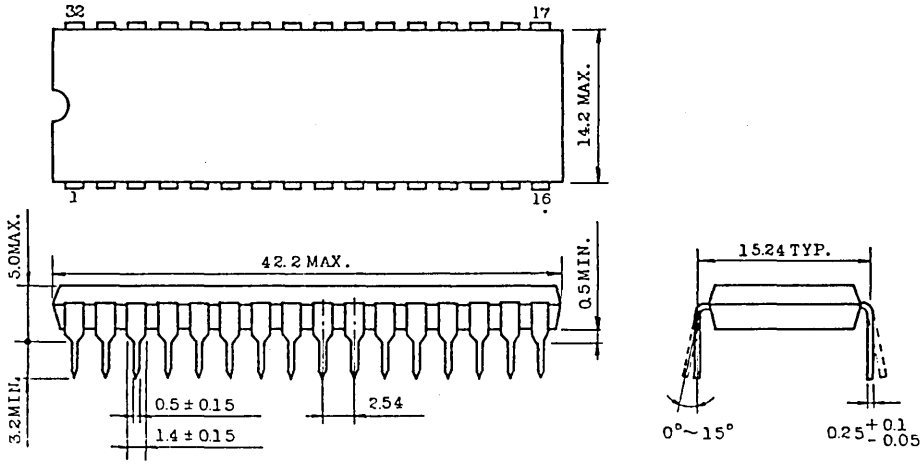
OPERATION MODE

MODE	$\overline{CE}$(CE)	$\overline{OE}$	A0 ∿ 18	Outputs	Power
Read	L(H)	L	Valid	Data Out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWINGS

Unit: mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.32 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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