Series 54/74 Circuits

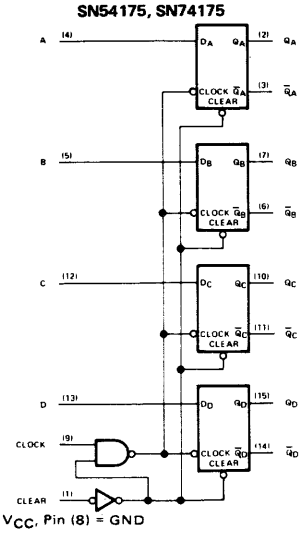
New TTL/MSI Now Available

SN54/74175 Quad and SN54/74174 HEX D-Type Flip-Flops With Direct Clear

- Replace latch circuits with clocked operation
- Reduce F-F Package count by 50 to 66
- Fully buffered inputs/outputs
- Economical for use as:
  - Buffer registers
  - Shift registers
  - Shift-register generators
  - Pattern generators
  - Scratch-pad memories

LOGIC

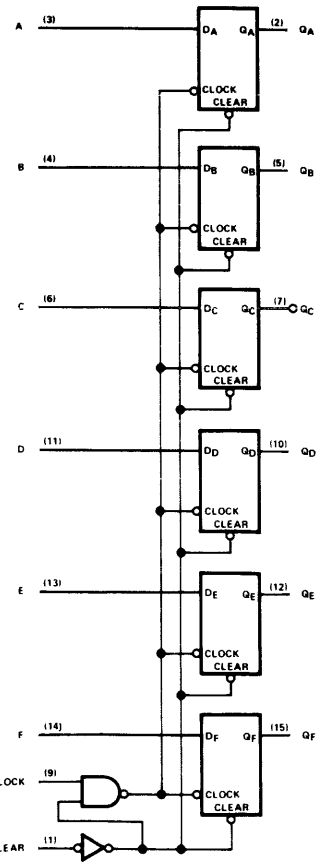
SN54175, SN74175



Pin (16) = V_{CC}, Pin (8) = GND

LOGIC

SN54174, SN74174



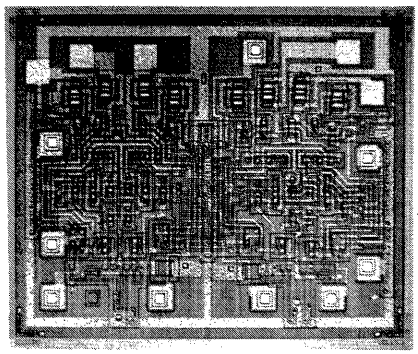
Pin (16) = V_{CC}, Pin (8) = GND

Available in 16-pin
J, N, and W packages

HIGH-SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS

description

TYPICAL DUAL FLIP-FLOP CIRCUIT BAR



Series 54/74 integrated circuits are designed and characterized for high-speed, general-purpose digital applications where high d-c noise margin and relatively low power dissipation are important system considerations. This logic series includes the basic gates, flip-flop elements, and complex logic and storage elements needed to perform all functions of general-purpose digital systems. Series 54 and 74 are completely compatible with Series 54H/74H, 54L/74L, and 54S/74S TTL logic families. Compatibility of these four TTL families permits improved systems design as the logician is permitted the flexibility of selecting component switching speed or circuit power dissipation with respect to system requirements. Series 54H/74H or 54S/74S high-speed TTL circuits can be selectively used to perform those functions requiring minimal propagation delay times. Series 54L/74L low-power TTL circuits can be used to reduce total power requirements. All four TTL families are designed to operate at the same supply voltages and compatible logic levels. In addition, high d-c noise margins characteristic of TTL circuits are maintained.

Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C for Series 54 circuits, and over the temperature range of 0°C to 70°C for Series 74 circuits.

features

LOW SYSTEM COST

- **choice of packages — ceramic flat package**
  — economical dual-in-line plastic package
  — ceramic dual-in-line package
- **broad selection of SSI and MSI functions — reduces package count**

OPTIMUM CIRCUIT PERFORMANCE

- **high speed — typical gate propagation delay time of 10 ns**
- **high d-c noise margin — typically one volt**
- **low output impedance provides low a-c noise susceptibility**
- **diode-clamped inputs simplify system design**
- **low power dissipation — 10 mW per gate at 50% duty cycle**
- **full fan-out —10 Series 54/74L loads**
  — 40 Series 54L/74L loads
  — 8 Series 54S/74S or 54H/74H loads
- **compatible for use with other current-sinking logic families — DTL, other TTL**
- **all inputs are diode clamped to minimize transmission-line effects**

SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES*			SEC.-PAGE
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR/AND/OR GATES AND BUFFERS						
Quadruple 2-Input Positive NAND Gates	SN5400	SN7400	J	N	W	6-5
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5401	SN7401	J	N	W	6-6
Quadruple 2-Input Positive NOR Gates	SN5402	SN7402	J	N	W	6-9
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5403	SN7403	J	N		6-10
Hex Inverters	SN5404	SN7404	J	N	W	6-11
Hex Inverters (with Open-Collector Output)	SN5405	SN7405	J	N	W	6-12
Hex Inverter Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5406	SN7406	J	N	W	6-13
Hex Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5407	SN7407	J	N	W	6-15
Quadruple 2-Input Positive AND Gates	SN5408	SN7408	J	N	W	6-17
Quadruple 2-Input Positive AND Gates	SN5409	SN7409	J	N	W	6-17
Triple 3-Input Positive NAND Gates	SN5410	SN7410	J	N	W	6-20
Triple 3-Input Positive NAND Gates (with Open-Collector Output)	SN5412	SN7412	J	N	W	6-21
Dual NAND Schmitt Triggers	SN5413	SN7413	J	N	W	6-22
Hex Inverter Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5416	SN7416	J	N	W	6-13
Hex Buffers/Drivers (with Open-Collector High-Voltage Output)	SN5417	SN7417	J	N	W	6-15
Dual 4-Input Positive NAND Gates	SN5420	SN7420	J	N	W	6-26
Expandable Dual 4-Input Positive NOR Gates (with Strobe)	SN5423	SN7423	J	N	W	6-27
Dual 4-Input Positive NOR Gates	SN5425	SN7425	J	N	W	6-27
Quadruple 2-Input High-Voltage Interface NAND Gates	SN5426	SN7426	J	N		6-30
Triple 3-Input Positive NOR Gates	SN5427	SN7427	J	N	W	6-32
8-Input Positive NAND Gates	SN5430	SN7430	J	N	W	6-34
Quadruple 2-Input Positive OR Gates	SN5432	SN7432	J	N	W	6-35
Quadruple 2-Input Positive NAND Buffers	SN5437	SN7437	J	N	W	6-37
Quadruple 2-Input Positive NAND Buffers (with Open-Collector Output)	SN5438	SN7438	J	N	W	6-37
Dual 4-Input Positive NAND Buffers	SN5440	SN7440	J	N	W	6-39

SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

TEXAS INSTRUMENTS
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SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
AND-OR-INVERT GATES						
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5450	SN7450	J	N	W	6-40
Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5451	SN7451	J	N	W	6-40
Expandable 4-Wide 2-Input AND-OR-INVERT Gates	SN5453	SN7453	J	N	W	6-42
4-Wide 2-Input AND-OR-INVERT Gates	SN5454	SN7454	J	N	W	6-42
EXPANDERS						
Dual 4-Input Expander	SN5460		J	N	W	6-44
Dual 4-Input Expander		SN7460	J	N	W	6-45
FLIP-FLOPS						
Positive Edge-Triggered J-K Flip-Flops (AND Inputs)	SN5470	SN7470	J	N	W	6-46
J-K Master-Slave Flip-Flops (AND Inputs)	SN5472	SN7472	J	N	W	6-49
Dual J-K Master-Slave Flip-Flops	SN5473	SN7473	J	N	W	6-52
Dual D-Type Edge-Triggered Flip-Flops	SN5474	SN7474	J	N	W	6-55
Dual-J-K Master-Slave Flip-Flops with Preset and Clear	SN5476	SN7476	J	N	W	6-58
Gated J-K Master-Slave Flip-Flops	SN54104	SN74104	J	N	W	6-61
Gated J-K Master-Slave Flip-Flops	SN54105	SN74105	J	N	W	6-61
Dual J-K Master-Slave Flip-Flops (V_{CC}-14, Gnd-7)	SN54107	SN74107	J	N		6-52
Gated J-K Master-Slave Flip-Flops with Data Lockout	SN54110	SN74110	J	N	W	6-66
Dual J-K Master-Slave Flip-Flops with Data Lockout	SN54111	SN74111	J	N	W	6-69
Monostable Multivibrators	SN54121	SN74121	J	N	W	6-72
Retriggerable Monostable Multivibrators with Clear	SN54122	SN74122	J	N	W	6-79
Dual Retriggerable Monostable Multivibrators with Clear	SN54123	SN74123	J	N	W	6-79

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SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Note 1)	5.5 V
Interemitter Voltage (See Note 2)	5.5 V
Resistor Node Voltage, SN54121, SN74121 (See Note 1)	−5.5 V to 7 V
Operating Free-Air Temperature Range: Series 54 Circuits	−55°C to 125°C
Series 74 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

logic definition

Series 54/74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

HIGH VOLTAGE = LOGICAL 1

LOW VOLTAGE = LOGICAL 0

input clamping diodes

Although not shown on all schematic diagrams, all of these SSI circuits incorporate input diodes. Each clamping diode is capable of limiting negative excursions at the input to a maximum of 1.5 volts below ground, even if −12 mA of current is drawn.

unused inputs of NAND/AND gates

6

For optimum switching times and minimum noise susceptibility, unused inputs should be maintained at a positive voltage greater than 2.4 V but not exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.4 V and 3.5 V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load in the logical 1 state to the driving output.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

input-current requirements

Input-current requirements reflect worst-case conditions over the specified recommended operating free-air temperature and V_{CC} ranges. Each input, of the multiple emitter input transistors which have a 4-kΩ base resistor, requires that no more than −1.6 mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −1.6 mA maximum. Each input requires current into the input at a logical 1 voltage level. This current is 40 μA maximum for each emitter of input transistors with the 4-kΩ base resistor. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

fan-out capability

Fan-out reflects the ability of an output to sink current from a number of loads (N) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate is capable of sinking current or supplying current to 30 loads (N = 30). Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

Series 54/74 circuits are well suited for driving Series 54H/74H and 54S/74S high-speed TTL and Series 54L/74L low-power TTL circuits. As examples, a Series 54/74 output, rated for a fan-out of ten (N=10), will drive eight 54H/74H loads or forty 54/74L loads.

TEXAS INSTRUMENTS
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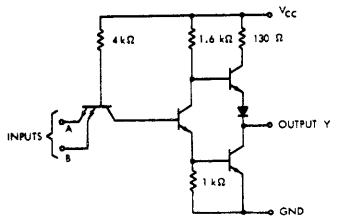
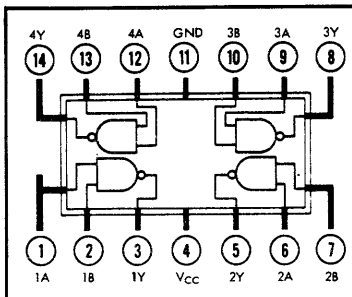
schematic (each gate)

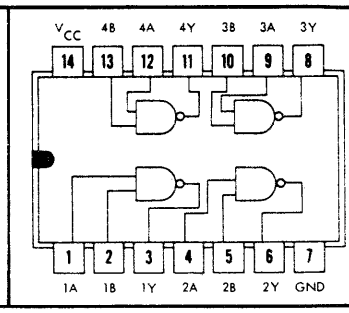


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5400 Circuits	4.5	5	5.5	V
SN7400 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5400 Circuits	−55	25	125	°C
SN7400 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5400	−20		−55	mA
				SN7400	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		11	22	ns

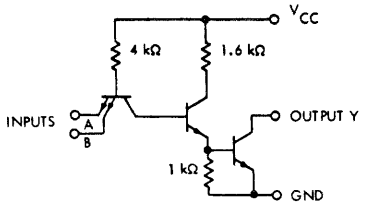
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

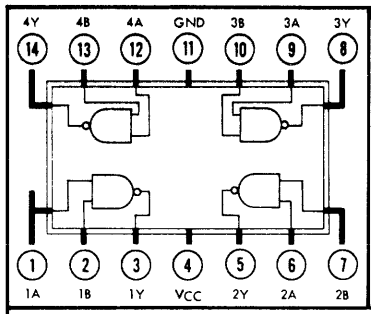
CIRCUIT TYPES SN5401, SN7401
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)

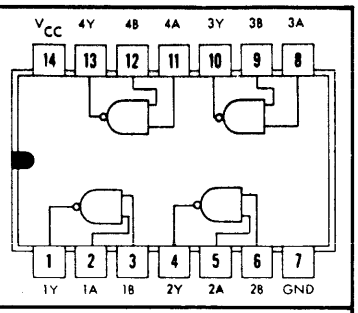


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5401 Circuits	4.5	5	5.5	V
SN7401 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5401 Circuits	−55	25	125	°C
SN7401 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7					0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, $V_{out(1)}$ = 5.5 V	V_{in} = 0.8 V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX,	V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX,	V_{in} = 0		4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), can be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54 TTL loads. When no other open-collector gates are paralleled, this gate can be used to drive ten TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available during a logical 1 level at output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

In both conditions (logical 0 and logical 1) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where: V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

logical 1 (off level) circuit calculations (see figure F)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the $V_{out(1)}$ level required at the load:

$$V_{RL} = V_{CC} - V_{out(1)\ required}$$

The total current through the load resistor (I_{RL} is the sum of the load currents ($I_{in(1)}$) and off-level reverse currents ($I_{out(1)}$ through each of the wire-AND connected outputs:

$$I_{RL} = \eta \cdot I_{out(1)} + N \cdot I_{in(1)} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ required}}{\eta \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

where: η = number of gates wire-AND connected, and N = number of TTL loads.

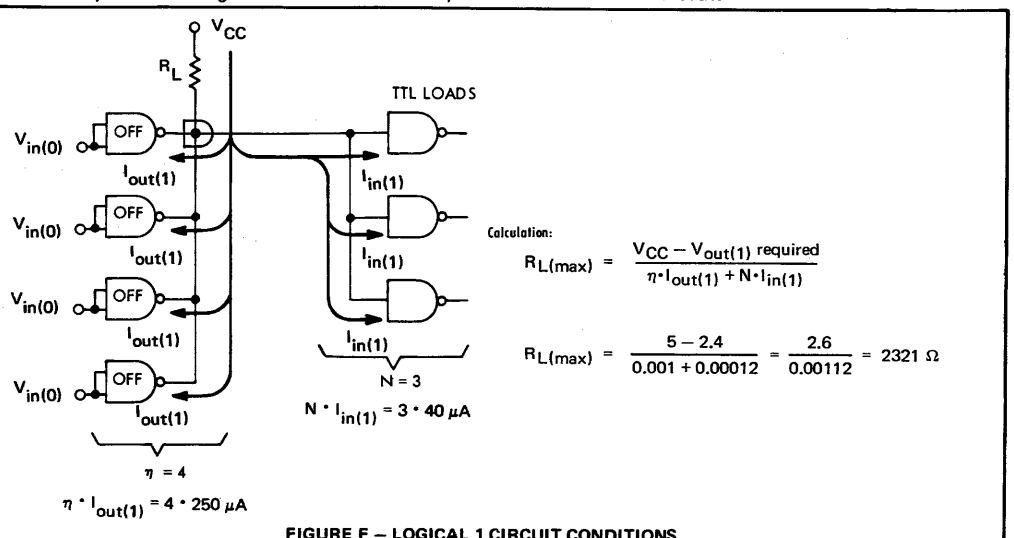


FIGURE F – LOGICAL 1 CIRCUIT CONDITIONS

APPLICATION DATA

logical 0 (on level) circuit calculations (see figure G)

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 16 mA, the maximum current which will ensure a logical 0 maximum of 0.4 volts.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L is:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)\ required}}{I_{sink\ capability} - I_{sink\ from\ TTL\ loads}}$$

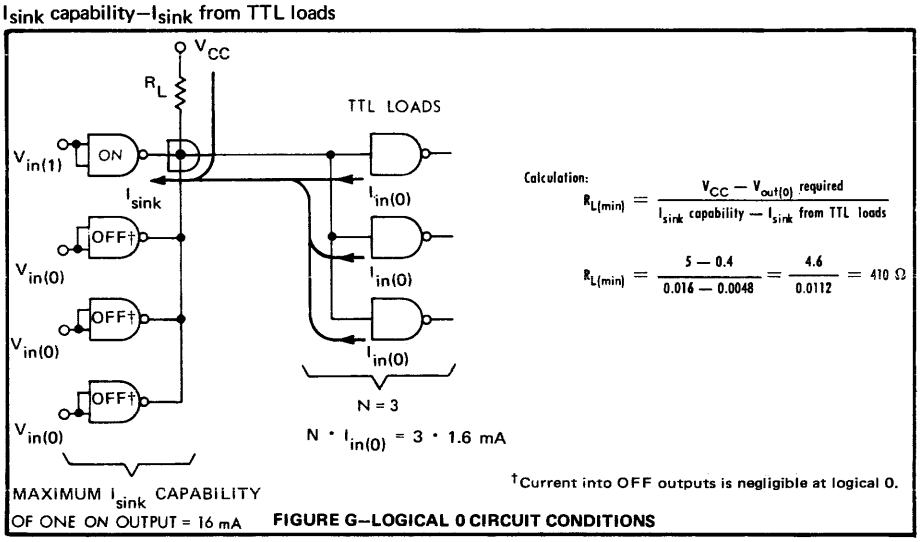


FIGURE G–LOGICAL 0 CIRCUIT CONDITIONS

driving TTL loads and combining outputs

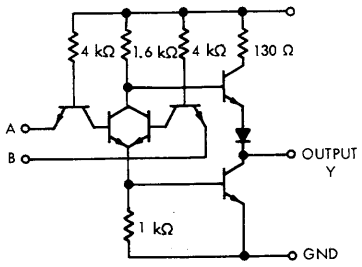
Table I provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten TTL loads and wire-AND connecting two to seven parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or fewer if a valid minimum and maximum R_L is possible. When fanning-out to ten TTL loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 4 kΩ resistor in this case will satisfy the logical 1 condition and limit the logical 0 level to less than 0.43 V.

FAN-OUT TO TTL LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000§
	MAXIMUM							MIN

TABLE 1–LOAD RESISTOR VALUE IN OHMS

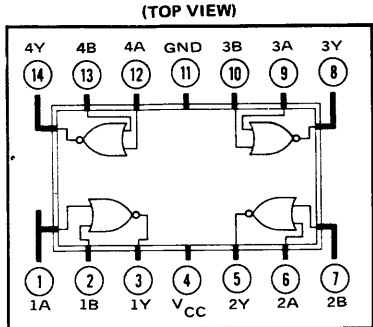
‡ All values shown in the table are based on:
Logical 1 conditions: V_{CC} = 5 V, $V_{out(1)}$ required = 2.4 V
Logical 0 conditions: V_{CC} = 5 V, $V_{out(0)}$ required = 0.4 V
§ – The theoretical value is ∞. See explanation in text.
X – Not recommended or not possible.

schematic (each gate)

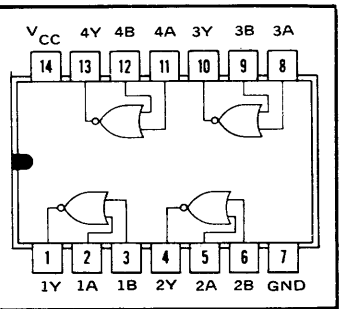


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N-DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A + B}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5402 Circuits	4.5	5	5.5	V
	SN7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5402 Circuits	−55	25	125	°C
	SN7402 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	8			2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	9					0.8	V
$V_{out(1)}$	Logical 1 output voltage	9	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	10	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	11	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	12	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	13	V_{CC} = MAX	SN5402	−20		−55	mA
				SN7402	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	14	V_{CC} = MAX, V_{in} = 5 V			14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	14	V_{CC} = MAX, V_{in} = 0			8	16	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		12	22	ns

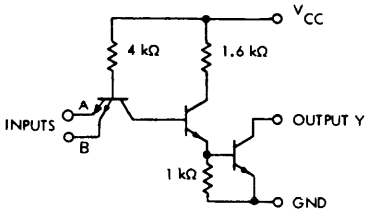
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

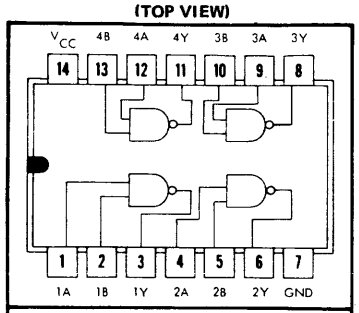
CIRCUIT TYPES SN5403, SN7403
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5403 Circuits	4.5	5	5.5	V
SN7403 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)			10	
Operating Free-Air Temperature Range, T_A: SN5403 Circuits	−55	25	125	°C
SN7403 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output)	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7				0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		4	8	mA

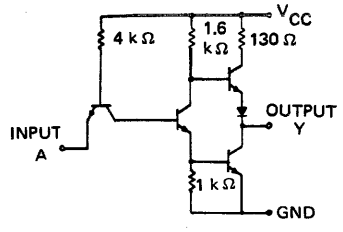
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

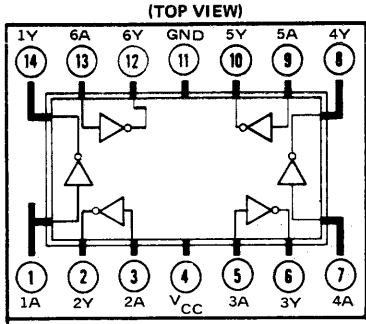
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each inverter)

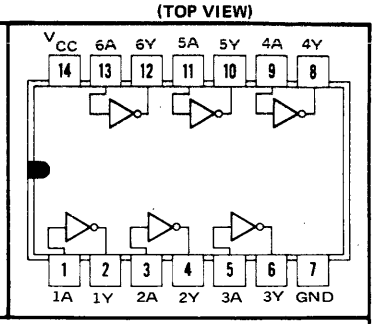


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \bar{A}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5404 Circuits	4.5	5	5.5	V
	SN7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5404 Circuits	−55	25	125	°C
	SN7404 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	15			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	16					0.8	V
$V_{out(1)}$	Logical 1 output voltage	16	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current	18	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current	18	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	19	V_{CC} = MAX	SN5404	−20		−55	mA
				SN7404	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	20	V_{CC} = MAX, V_{in} = 5 V			18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	20	V_{CC} = MAX, V_{in} = 0			6	12	mA

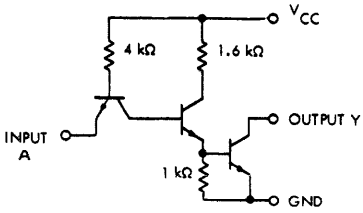
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

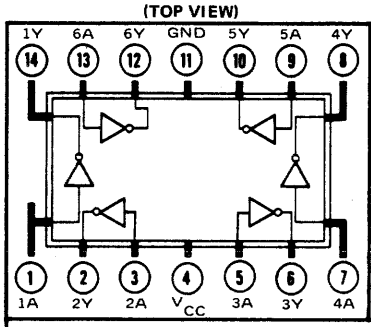
CIRCUIT TYPES SN5405, SN7405
HEX INVERTERS (WITH OPEN-COLLECTOR OUTPUT)

schematic (each inverter)

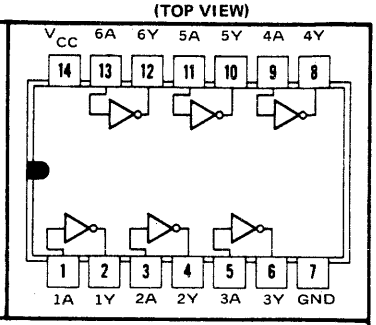


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5405 Circuits	4.5	5	5.5	V
SN7405 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)			10	
Operating Free-Air Temperature Range, T_A: SN5405 Circuits	−55	25	125	°C
SN7405 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

6

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	15		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	17				0.8	V
$I_{out(1)}$	Output reverse current	17	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	15	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current	18	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current	18	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	20	V_{CC} = MAX, V_{in} = 5 V, T_A = 25°C		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	20	V_{CC} = MAX, V_{in} = 0, T_A = 25°C		6	12	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		40	55	ns

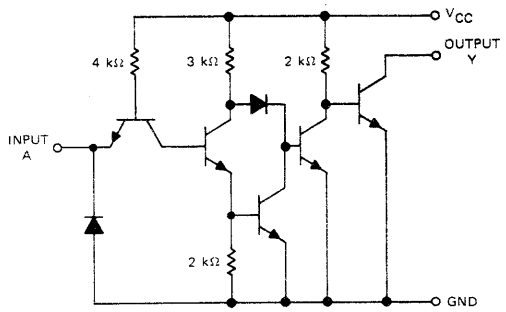
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ These typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN5406, SN5416, SN7406, SN7416
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

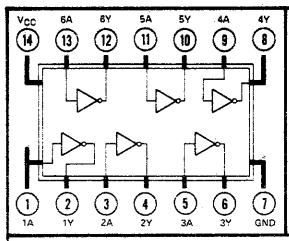
FOR INTERFACING WITH HIGH-LEVEL CIRCUITS
OR FOR DRIVING HIGH-CURRENT LOADS

schematic (each inverter)

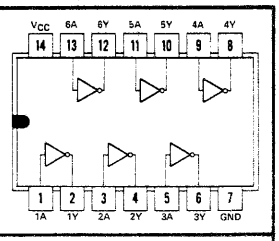


NOTE: Component values shown are nominal.

W
FLAT PACKAGE
(TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A}$

- **Converts TTL voltage levels to MOS levels**
- **High sink-current capability**
- **Input clamping diodes simplify system design**
- **Typical propagation delay time: 15 ns**
- **Open-collector driver for indicator lamps and relays**
- **Inputs fully compatible with most TTL and DTL circuits**
- **Typical power dissipation: 105 mW**

6

description

These monolithic TTL hex inverter buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as inverter buffers for driving TTL inputs. For increased fan-out, several inverters in a single package may be paralleled. The SN5406 and SN7406 have minimum breakdown voltages of 30 volts and the SN5416 and SN7416 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5406 and SN5416, and 40 milliamperes for the SN7406 and SN7416.

These circuits are completely compatible with most TTL or DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 150 milliwatts and average propagation delay time is 15 nanoseconds. The SN5406 and SN5416 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7406 and SN7416 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Output voltage (see Notes 1 and 2):	SN5406, SN7406 Circuits	30 V
	SN5416, SN7416 Circuits	15 V
Operating free-air temperature range:	SN5406, SN5416 Circuits	−55°C to 125°C
	SN7406, SN7416 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN5406, SN5416			SN7406, SN7416			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	SN5406, SN7406			30			30	V
	SN5416, SN7416			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	74		2			V
V_{IL}	Low-level input voltage	75				0.8	V
I_{OH}	High-level output current	75	V_{CC} = MIN, V_I = 0.8 V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	74	V_{CC} = MIN, V_I = 2 V, I_{OL} = MAX			0.7	V
			V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current (each input)	76	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	77	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	78	V_{CC} = MAX, V_I = 0		30	42	mA
I_{CCL}	Supply current, low-level output	78	V_{CC} = MAX, V_I = 5 V		27	38	mA

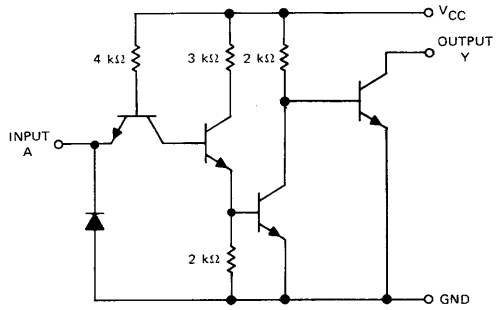
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	79	C_L = 15 pF, R_L = 110 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output	79	C_L = 15 pF, R_L = 110 Ω		15	23	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

FOR INTERFACING WITH HIGH-LEVEL CIRCUITS
OR FOR DRIVING HIGH-CURRENT LOADS

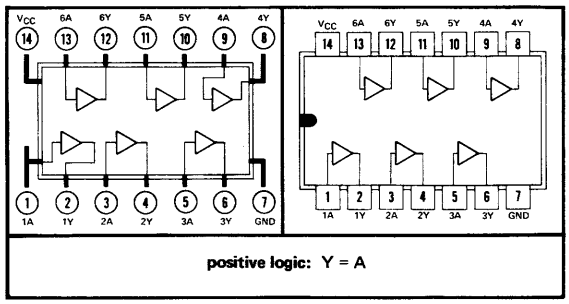
schematic (each buffer/driver)



NOTE: Component values shown are nominal.

W
FLAT PACKAGE
(TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



- Converts TTL voltage levels to MOS levels
- High sink-current capability
- Input clamping diodes simplify system design
- Typical propagation delay time: 14 ns
- Open-collector driver for indicator lamps and relays
- Inputs fully compatible with most TTL and DTL circuits
- Typical power dissipation: 145 mW

6

description

These monolithic TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as buffers for driving TTL inputs. For increased fan-out, several buffers in a single package may be paralleled. The SN5407 and SN7407 have minimum breakdown voltages of 30 volts and the SN5417 and SN7417 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5407 and SN5417, and 40 milliamperes for the SN7407 and SN7417.

These circuits are completely compatible with most TTL and DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 145 milliwatts and average propagation delay time is 14 nanoseconds. The SN5407 and SN5417 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7407 and SN7417 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Output voltage (see Notes 1 and 2):	SN5407, SN7407 Circuits	30 V
	SN5417, SN7417 Circuits	15 V
Operating free-air temperature range:	SN5407, SN5417 Circuits	−55°C to 125°C
	SN7407, SN7417 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN5407, SN5417			SN7407, SN7417			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	SN5407, SN7407			30			30	V
	SN5417, SN7417			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	80		2			V
V_{IL}	Low-level input voltage	81				0.8	V
I_{OH}	High-level output current	80	V_{CC} = MIN, V_I = 2 V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	81	V_{CC} = MIN, V_I = 0.8 V, I_{OL} = MAX			0.7	V
			V_{CC} = MIN, V_I = 0.8 V, I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current (each input)	82	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	83	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	84	V_{CC} = MAX, V_I = 5 V		29	41	mA
I_{CCL}	Supply current, low-level output	84	V_{CC} = MAX, V_I = 0		21	30	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

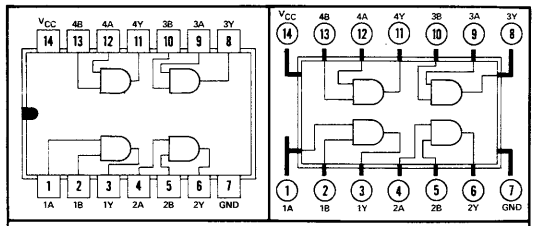
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	85	C_L = 15 pF, R_L = 110 Ω		6	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output	85	C_L = 15 pF, R_L = 110 Ω		20	30	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

Choice of Totem-Pole Outputs (SN5408/SN7408) or Open-Collector Outputs (SN5409/SN7409)

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

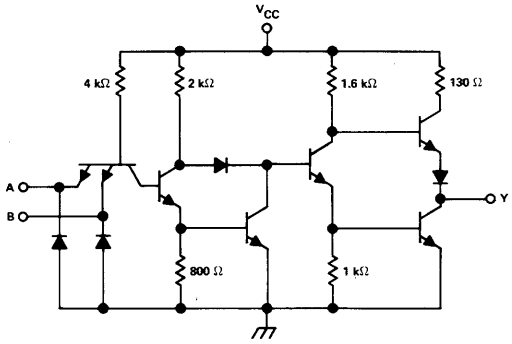
W
FLAT PACKAGE
(TOP VIEW)



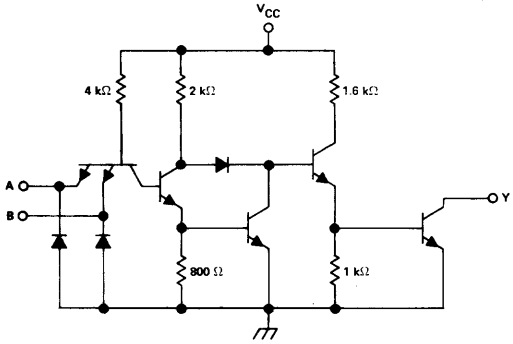
positive logic: Y = AB

schematics (each gate)

SN5408, SN7408



SN5409, SN7409



Component values shown are nominal.

6

description

These Series 54/74 TTL gates provide the system designer with direct implementation of the positive AND or negative OR functions.

The SN5408/SN7408, with totem-pole outputs, drives 10 normalized Series 54/74 loads at the low output level and 20 loads at the high output level. The SN5409/SN7409, with open-collector output, provides additional logic flexibility, as the outputs may be wire-AND connected to extend the AND function. The SN5409/SN7409 will sink sufficient current to drive 10 normalized Series 54/74 loads at the low output level.

The SN5408 and SN5409 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7408 and SN7409 are characterized for operation from 0°C to 70°C.

SN5408, SN7408

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range, T_A: SN5408 Circuits . . . . . −55°C to 125°C
SN7408 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	SN5408			SN7408			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN5408, SN7408			UNIT
					MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	86			2			V
V_{IL}	Low-level input voltage	88					0.8	V
V_{OH}	High-level output voltage	86	V_{CC} = MIN, I_{OH} = −800 μA	V_{IH} = 2 V,	2.4			V
V_{OL}	Low-level output voltage	88	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_{IH}	High-level input current (each input)	89	V_{CC} = MAX,	V_I = 2.4 V			40	μA
			V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	90	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	91	V_{CC} = MAX	SN5408	−20		−55	mA
				SN7408	−18		−55	
I_{CCH}	Supply current, high-level output	92	V_{CC} = MAX,	V_I = 5 V		11	21	mA
I_{CCL}	Supply current, low-level output	92	V_{CC} = MAX,	V_I = 0		20	33	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5408, SN7408			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	93	C_L = 15 pF, R_L = 400 Ω		17.5	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	19	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

SN5409, SN7409

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Output voltage (see Notes 1 and 3) . . . . . 5.5 V
Operating free-air temperature range: SN5409 Circuits . . . . . −55°C to 125°C
SN7409 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5409			SN7409			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	SN5409, SN7409			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	87		2			V
V_{IL}	Low-level input voltage	88				0.8	V
I_{OH}	High-level output current	87	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	88	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_{IH}	High-level input current (each input)	89	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	90	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	92	V_{CC} = MAX, V_I = 5 V		11	21	mA
I_{CCL}	Supply current, low-level output	92	V_{CC} = MAX, V_I = 0		20	33	mA

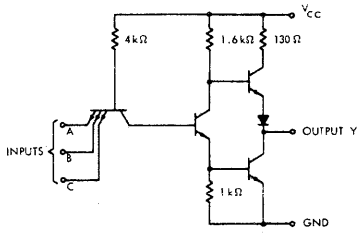
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5409, SN7409			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	93	C_L = 15 pF, R_L = 400 Ω		21	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output				16	24	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

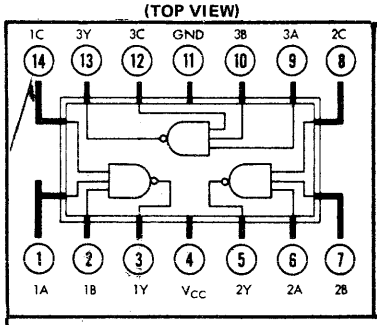
CIRCUIT TYPES SN5410, SN7410
TRIPLE 3-INPUT POSITIVE NAND GATES

schematic (each gate)

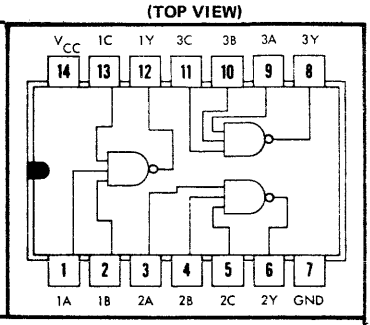


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5410 Circuits	4.5	5	5.5	V
	SN7410 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5410 Circuits	−55	25	125	°C
	SN7410 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short circuit output current§	5	V_{CC} = 5.5 V	SN5410	−20		−55	mA
				SN7410	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			3	6	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

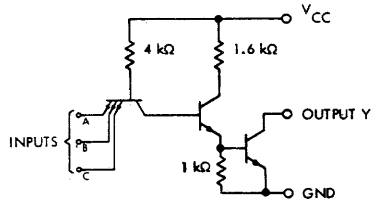
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		11	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

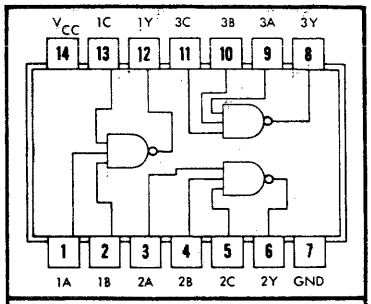
§ Not more than one output should be shorted at a time.

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5412 Circuits	4.5	5	5.5	V
SN7412 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5412 Circuits	−55	25	125	°C
SN7412 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7				0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V		9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		3	6	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

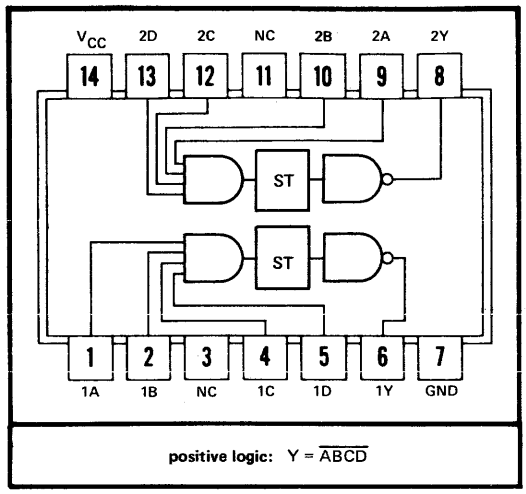
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating condionts for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN5413,SN7413
DUAL NAND SCHMITT TRIGGERS

- Operation from Very Slow Edges
- Temperature-Compensated Threshold Levels
- Temperature-Compensated Hysteresis, Typically 0.8 V
- High Noise Immunity

J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)†



NC—No internal connection.
†Pin assignments for these circuits are the same for all packages.

description

6

The SN5413 and SN7413 dual Schmitt triggers consist of two identical Schmitt-trigger circuits in monolithic integrated circuit form. Logically, each circuit functions as a four-input NAND gate, but because of the Schmitt action, the gate has different input threshold levels for positive- and negative-going signals. The hysteresis, or backlash, which is the difference between the two threshold levels, is typically 800 mV.

An important design feature is the built-in temperature compensation which ensures very high stability of the threshold levels and the hysteresis over a very wide temperature range. Typically, the hysteresis changes by 3% over the temperature range of −55°C to 125°C and the upper threshold changes by 1% over the same range. The SN5413/SN7413 can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. It can also be triggered from straight d-c levels.

These circuits are fully compatible with most other TTL, DTL, or MSI circuits. The SN5413 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN7413 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5413 Circuits	−55°C to 125°C
SN7413 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		SN5413			SN7413			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	0	125	0	25	70	°C
Maximum input rise and fall times		No restriction			No restriction			

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage	94	V_{CC} = 5 V	1.5	1.7	2	V
V_{T-}	Negative-going threshold voltage	95	V_{CC} = 5 V	0.6	0.9	1.1	V
$V_{T+}-V_{T-}$	Hysteresis	94 & 95	V_{CC} = 5 V	0.4	0.8		V
V_I	Input clamp voltage	97	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	95	V_{CC} = MIN, V_I = 0.6 V, I_{OH} = −800 μA	2.4	3.3		V
V_{OL}	Low-level output voltage	94	V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA		0.22	0.4	V
I_{T+}	Input current at positive-going threshold	94	V_{CC} = 5 V, V_I = V_{T+}		−0.65		mA
I_{T-}	Input current at negative-going threshold	95	V_{CC} = 5 V, V_I = V_{T-}		−0.85		mA
I_I	Input current at maximum input voltage	96	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	96	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	97	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current§	98	V_{CC} = MAX	−18		−55	mA
I_{CCH}	Supply current, high-level output	99	V_{CC} = MAX, V_I = 0		14	23	mA
I_{CCL}	Supply current, low-level output	99	V_{CC} = MAX, V_I = 4.5 V		20	32	mA

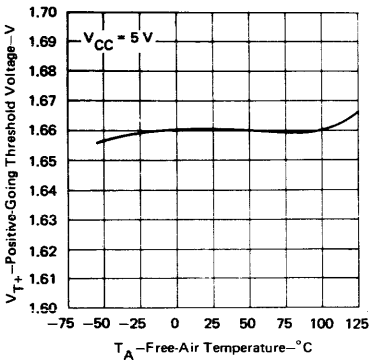
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

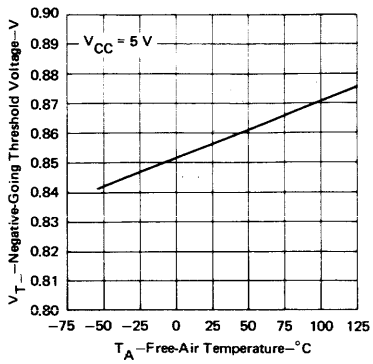
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	100	C_L = 15 pF, R_L = 400 Ω		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output	100	C_L = 15 pF, R_L = 400 Ω		15	22	ns

TYPICAL CHARACTERISTICS

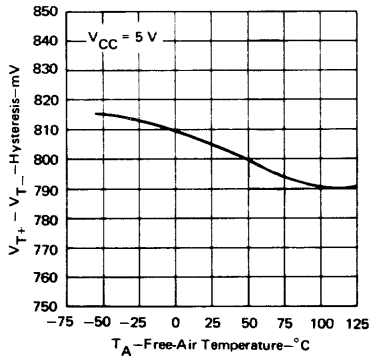
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



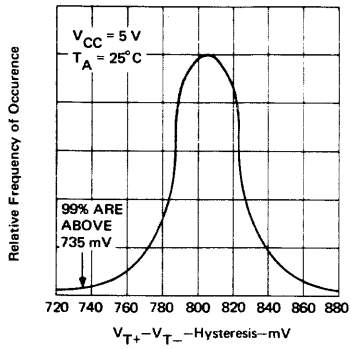
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



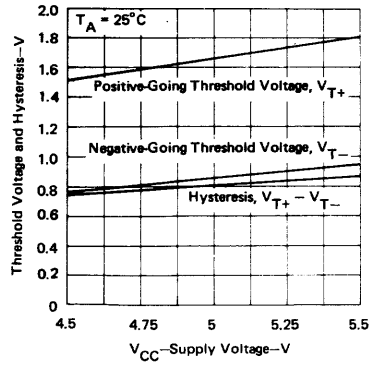
HYSTERESIS
vs
FREE-AIR TEMPERATURE



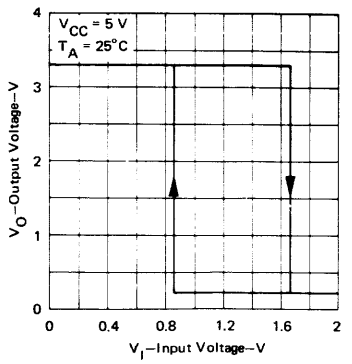
DISTRIBUTION OF UNITS
FOR HYSTERESIS



THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE



OUTPUT VOLTAGE
vs
INPUT VOLTAGE



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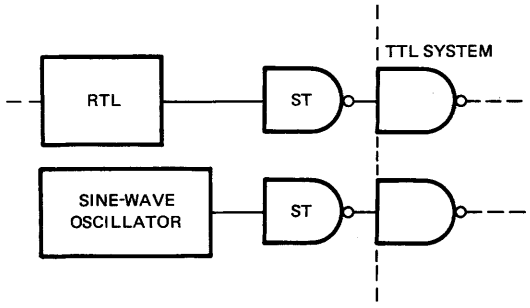
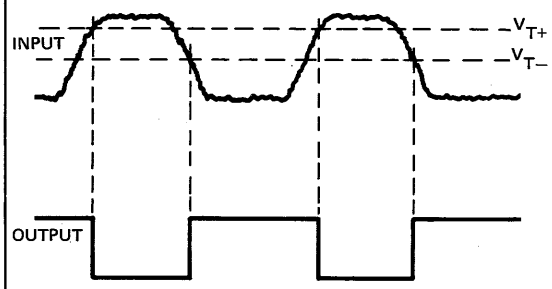
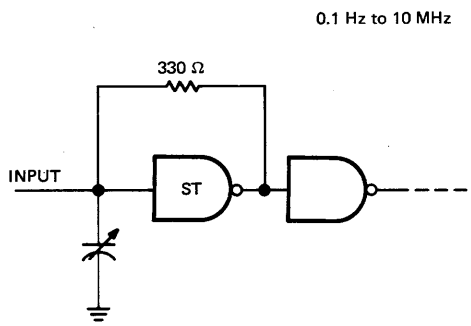
TYPICAL APPLICATION DATA



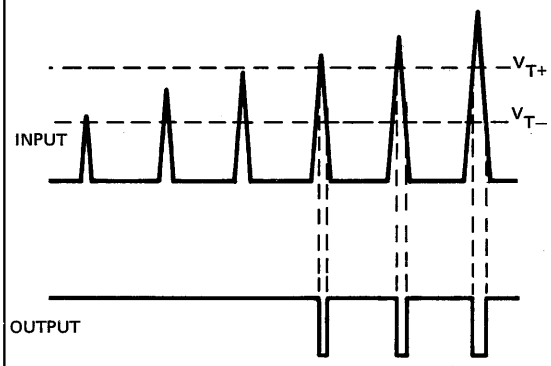
TTL SYSTEM INTERFACE
FOR SLOW INPUT WAVEFORMS



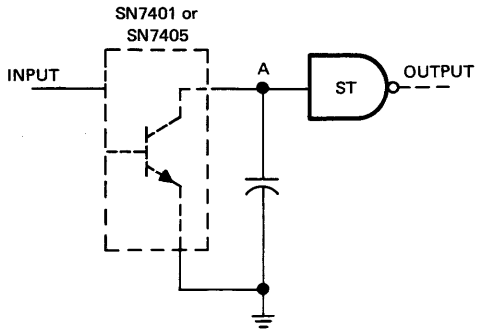
PULSE SHAPER

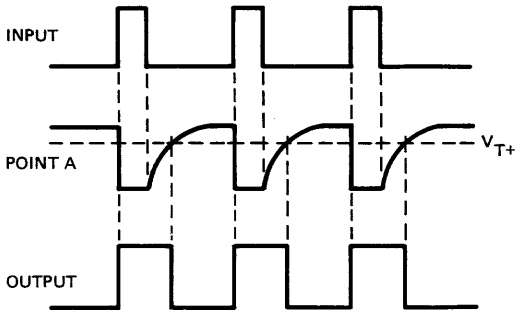


MULTIVIBRATOR



THRESHOLD DETECTOR



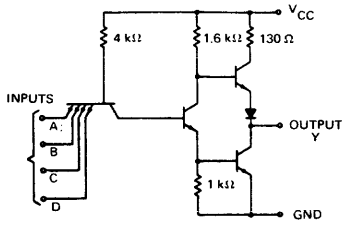


PULSE STRETCHER

6

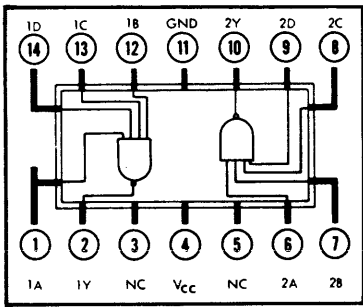
CIRCUIT TYPES SN5420, SN7420
DUAL 4-INPUT POSITIVE NAND GATES

schematic (each gate)

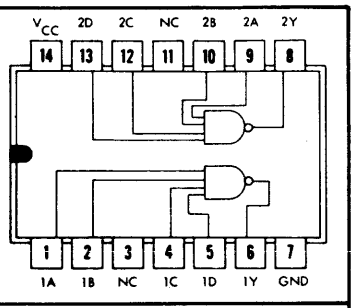


Component values shown are nominal.
NC—No Internal Connection

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5420 Circuits	4.5	5	5.5	V
	SN7420 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5420 Circuits	−55	25	125	°C
	SN7420 Circuits	0	25	70	°C

6

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

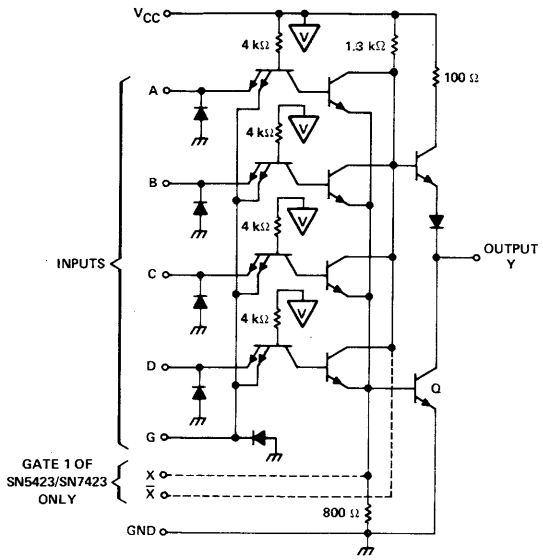
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5420	−20		−55	mA
				SN7420	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			6	11	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			2	4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

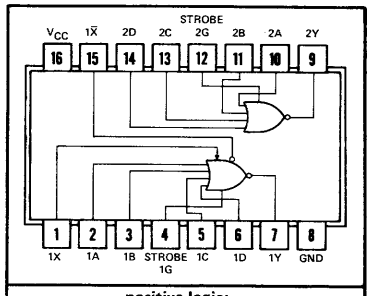
schematic (each gate)



NOTES: A. Component values shown are nominal.
B. Both expander inputs are used simultaneously for expanding.
C. If expander is not used leave X and $\overline{X}$ open.
D. A total of four expander gates can be connected to the expander inputs.

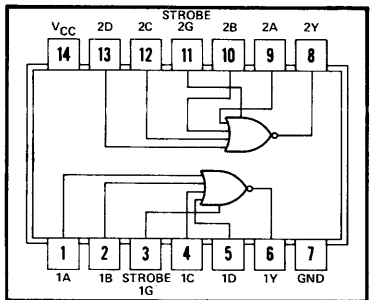
▽ = V_{CC} bus

SN5423, SN7423
J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)†



positive logic:
$1Y = \overline{1G(1A+1B+1C+1D)+X}$
$2Y = \overline{2G(2A+2B+2C+2D)}$
X = output of SN5460/SN7460

SN5425, SN7425
J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)†



positive logic:
$Y = \overline{G(A+B+C+D)}$

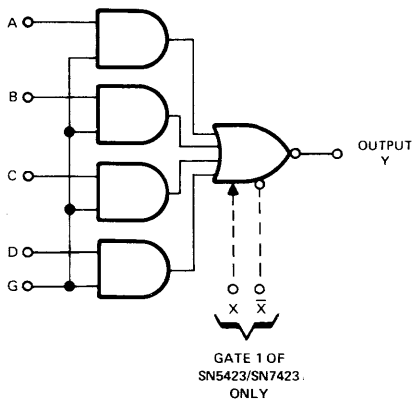
†Pin assignments for these circuits are the same for all packages.

logic and functional block diagram (each gate)

TRUTH TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

Expander inputs are open.
H = high level, L = low level, X = irrelevant



6

CIRCUIT TYPES SN5423, SN5425, SN7423, SN7425
DUAL 4-INPUT NOR GATES WITH STROBE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5423, SN5425 Circuits . . . . . −55°C to 125°C
SN7423, SN7425 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		SN5423, SN5425			SN7423, SN7425			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −800 μA	V_{IL} = 0.8 V,	2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,		0.22	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4 V			40	μA
		strobe inputs					160	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		strobe inputs					−6.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−55	mA
I_{CCH}	Supply current, high-level output		V_{CC} = MAX,	All inputs at 0 V		8	16	mA
I_{CCL}	Supply current, low-level output		V_{CC} = MAX,	All inputs at 5 V		10	19	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

electrical characteristics (SN5423 circuits) using expander inputs, V_{CC} = 4.5 V, T_A = −55°C

PARAMETER		TEST FIGURE¶	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{OL} = 16 mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{OL} = 16 mA, I_1 = 0.41 mA, R_1 = 0			1	V
V_{OH}	High-level output voltage	30	I_{OH} = −400 μA, I_1 = 0.15 mA, I_2 = −0.15 mA	2.4	3.3		V
V_{OL}	Low-level output voltage	29	I_{OL} = 16 mA, I_1 = 0.3 mA, R_1 = 138 Ω		0.22	0.4	V

electrical characteristics (SN7423 circuits) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE¶	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{OL} = 16 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{OL} = 16 mA, I_1 = 0.62 mA, R_1 = 0			1	V
V_{OH}	High-level output voltage	30	I_{OH} = −400 μA, I_1 = 270 μA, I_2 = −270 μA	2.4	3.3		V
V_{OL}	Low-level output voltage	29	I_{OL} = 16 mA, I_1 = 0.43 mA, R_1 = 130 Ω		0.22	0.4	V

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Referenced test figures appear on page 2-49 of TTL Integrated Circuits Catalog (CC201).

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, (see note 3)

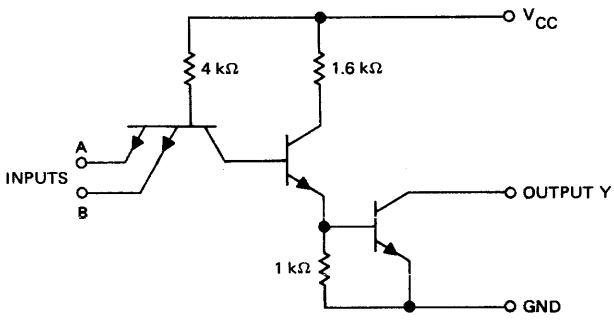
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω		13	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 400 Ω		8	15	ns

NOTE 3: Switching characteristics of the SN5423 and SN7424 are tested with the expander pins open.

CIRCUIT TYPES SN5426, SN7426
QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE NAND GATES

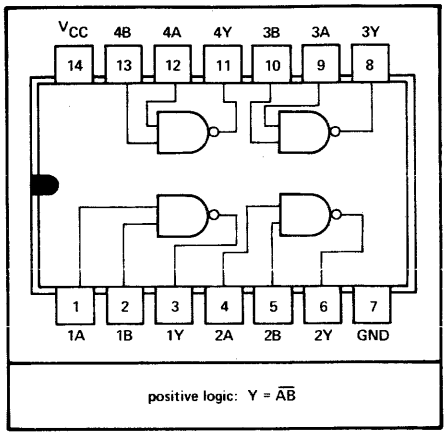
FOR DRIVING LOW-THRESHOLD-VOLTAGE MOS INPUTS

schematic (each gate)



Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

description

These open-collector NAND gates feature high output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12-volt systems. Although the output is rated to withstand 15 volts, the V_{CC} terminal is connected to the standard 5-volt source. The output transistor will sink 16 milliamperes while maintaining a low-level output voltage of 0.4 volt maximum thus providing a high-fan-out driver with the nominal power dissipation of standard Series 54/74 gates.

The SN5426 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN7426 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Output voltage (see Notes 1 and 2) . . . . . 15 V
Operating free-air temperature range: SN5426 Circuits . . . . . −55°C to 125°C
SN7426 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5426			SN7426			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage	4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}			15			15	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	101		2			V
V_{IL}	Low-level input voltage	102				0.8	V
V_{OH}	High-level output voltage	102	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = 1 mA	15			V
I_{OH}	High-level output current	102	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 12 V			50	μA
V_{OL}	Low-level output voltage	101	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA			0.4	V
I_{IH}	High-level input current (each input)	103	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	104	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	105	V_{CC} = MAX, V_I = 0		4	8	mA
I_{CCL}	Supply current, low-level output	105	V_{CC} = MAX, V_I = 5 V		12	22	mA

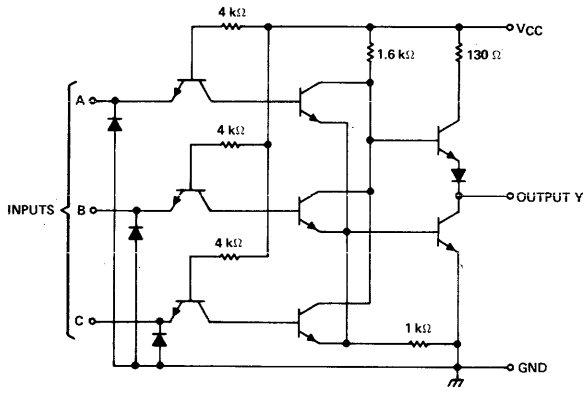
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	106	C_L = 15 pF, R_L = 1 kΩ		16	24	ns
t_{PHL}	Propagation delay time, high-to-low-level output	106	C_L = 15 pF, R_L = 1 kΩ		11	17	ns

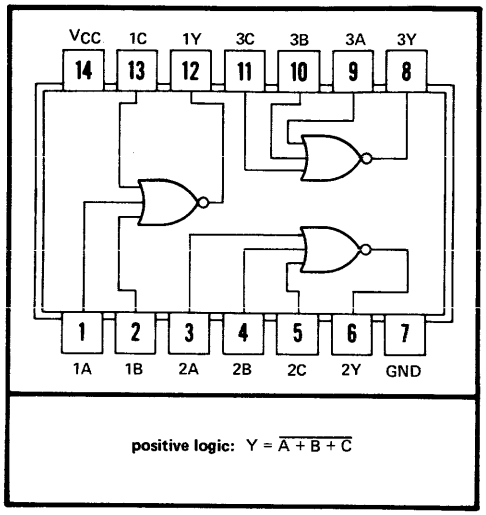
CIRCUIT TYPES SN5427, SN7427
TRIPLE 3-INPUT POSITIVE-NOR GATES

schematic (each gate)



Component values shown are nominal.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5427 Circuits . . . . . −55°C to 125°C
SN7427 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5427			SN7427			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA			0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN5427	−20		−55	mA
			SN7427	−18		−55	
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	See Note 2		10	16	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	See Note 3		16	26	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 2. I_{CCH} is measured with all inputs grounded, and outputs open.
3. I_{CCL} is measured with one input of each gate at 4.5 V, the remaining inputs grounded, and outputs open.

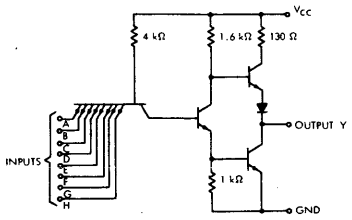
6

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 400 Ω		10	15	ns
t_{PLH}	Propagation delay time, low-to-high-level output			7	11	ns

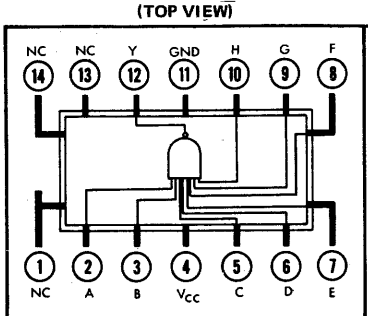
CIRCUIT TYPES SN5430, SN7430
8-INPUT POSITIVE NAND GATES

schematic

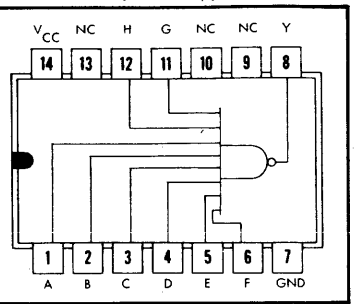


Component values shown are nominal.
NC—No Internal Connection

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCDEFGH}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5430 Circuits	4.5	5	5.5	V
	SN7430 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5430 Circuits	−55	25	125	°C
	SN7430 Circuits	0	25	70	°C

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electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

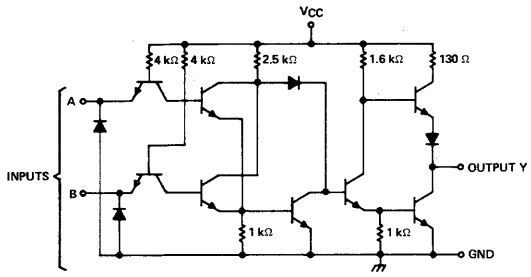
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5430	−20		−55	mA
				SN7430	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			3	6	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			1	2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

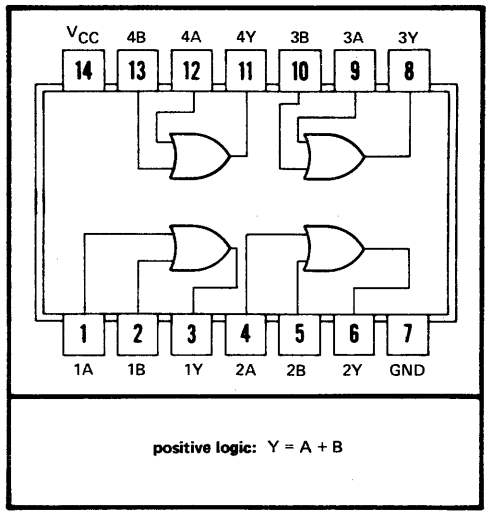
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		13	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

schematic (each gate)



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5432 Circuits . . . . . −55°C to 125°C
SN7432 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5432			SN7432			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA	V_{IH} = 2 V,	2.4	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,		0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX.	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN5432	−20		−55	mA
			SN7432	−18		−55	
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	See Note 2		15	22	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	See Note 3		23	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTES: 2. I_{CCH} is measured with one input of each gate at 4.5 V, the remaining inputs grounded, and outputs open.
3. I_{CCL} is measured with both inputs of all gates grounded, and outputs open.

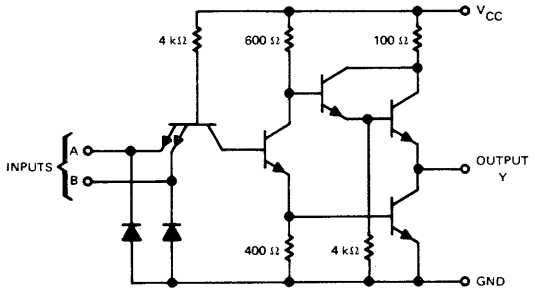
6

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

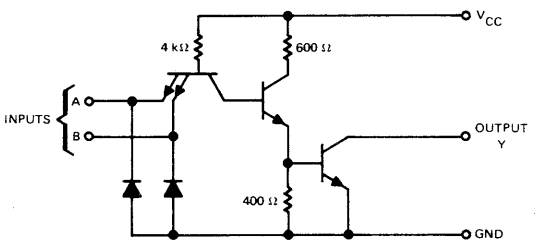
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 400 Ω		14	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output			10	15	ns

schematics (each buffer)

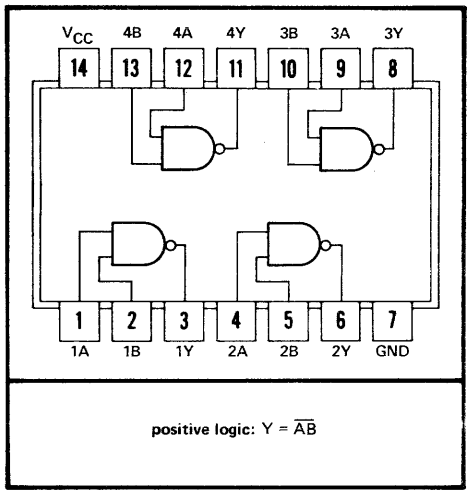
SN5437, SN7437 (TOTEM-POLE OUTPUT)



SN5438, SN7438 (OPEN-COLLECTOR OUTPUT)



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Output voltage (see Notes 1 and 3): SN5438, SN7438 Circuits . . . . . 5.5 V
Operating free-air temperature range: SN5437, SN5438 Circuits . . . . . −55°C to 125°C
SN7437, SN7438 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5437, SN5438			SN7437, SN7438			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			30			30	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN5437, SN7437			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −1.2 mA	V_{IL} = 0.8 V,	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 48 mA	V_{IH} = 2 V,		0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	V_I = 0	−20		−70	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	All inputs at 0 V		9	15.5	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	All inputs at 5 V		34	54	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN5438, SN7438			UNIT
					MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN,	V_{IL} = 0.8 V,	V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 48 mA		0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	All inputs at 0 V			5	8.5	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	All inputs at 5 V			34	54	mA

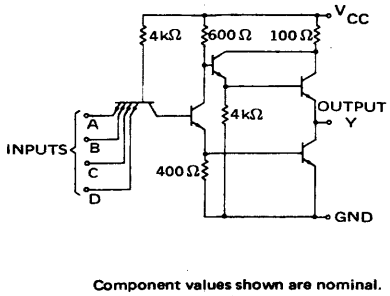
6

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

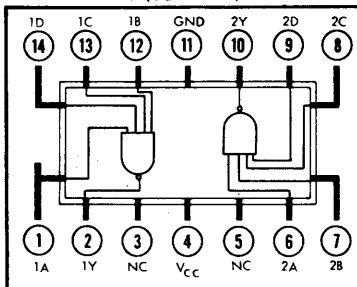
PARAMETER		TEST CONDITIONS	SN5437, SN7437			SN5438, SN7438			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 133 Ω		13	22		14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	15		11	18	ns

schematic (each gate)

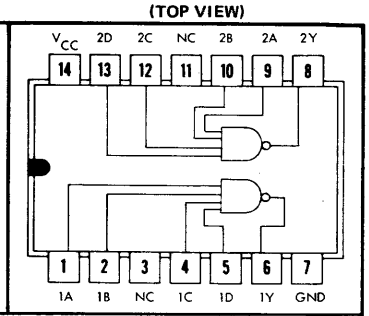


Component values shown are nominal.
NC—No Internal Connection

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5440 Circuits	4.5	5	5.5	V
	SN7440 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N				30	
Operating Free-Air Temperature Range, T_A:	SN5440 Circuits	−55	25	125	°C
	SN7440 Circuits	0	25	70	°C

electrical characteristics (over recommended free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −1.2 mA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 48 mA			0.28	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current §	5	V_{CC} = MAX	SN5440	−20		−70	mA
				SN7440	−18		−70	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			17	27	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			4	8	mA

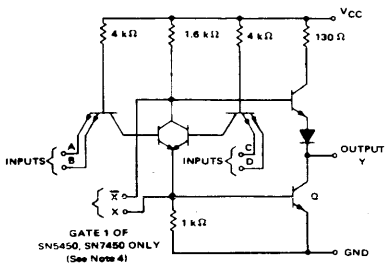
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 133 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 133 Ω		13	22	ns

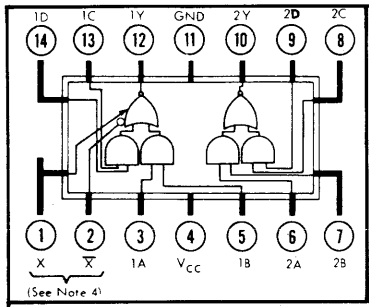
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

CIRCUIT TYPES SN5450, SN5451, SN7450, SN7451
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

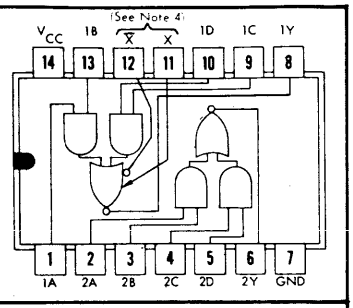
schematic (each gate)



W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (X)}$
X = Output of SN5460/SN7460

NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Make no external connection to X and $\overline{X}$ pins of the SN5451 and SN7451.
5. A total of four expander gates can be connected to the expander inputs.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5450, SN5451 Circuits	4.5	5	5.5	V
SN7450, SN7451 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5450, SN5451 Circuits	−55	25	125	°C
SN7450, SN7451 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	21			2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	22					0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	21	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	23	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	24	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	25	V_{CC} = MAX	SN5450, SN5451	−20		−55	mA
				SN7450, SN7451	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	26	V_{CC} = MAX, V_{in} = 5 V			7.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	27	V_{CC} = MAX, V_{in} = 0			4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

electrical characteristics (SN5450 circuits) using expander inputs, V_{CC} = 4.5 V, T_A = –55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.41 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 0.15 mA, I_2 = –0.15 mA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.3 mA, R_1 = 138 Ω		0.22	0.4	V

electrical characteristics (SN7450 circuits) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.62 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 270 μA, I_2 = –270 μA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.43 mA, R_1 = 130 Ω		0.22	0.4	V

6

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

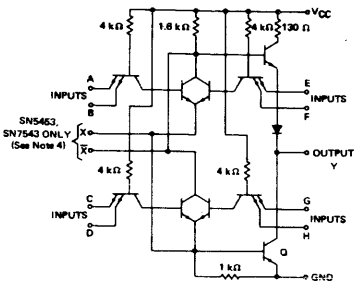
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		13	22	ns

†Expander pins X and $\overline{X}$ are open.

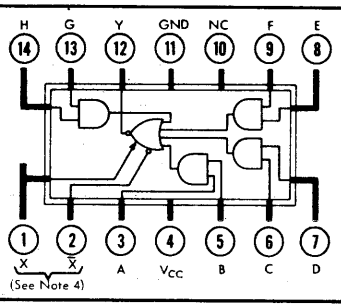
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

CIRCUIT TYPES SN5453, SN5454, SN7453, SN7454
EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATES

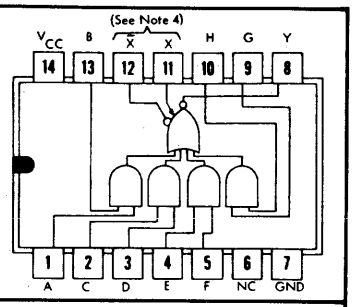
schematic



W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (EF) + (GH) + (X)}$
X = Output of SN5460/SN7460

NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Make no external connection to X and $\overline{X}$ pins of the SN5454 and SN7454.
5. A total of four expander gates can be connected to the expander inputs.
6. NC—No Internal Connection

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5453, SN5454 Circuits	4.5	5	5.5	V
SN7453, SN7454 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5453, SN5454 Circuits	−55	25	125	°C
SN7453, SN7454 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of one AND section to ensure logical 0 level at output	21			2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 level at output	22					0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	21	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	23	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	24	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	25	V_{CC} = 5.5 V	SN5453, SN5454	−20		−55	mA
				SN7453, SN7454	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	26	V_{CC} = MAX, V_{in} = 5 V			5.1	9.5	mA
$I_{CC(1)}$	Logical 1 level supply current	27	V_{CC} = MAX, V_{in} = 0			4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

electrical characteristics (SN5453 circuits) using expander inputs, V_{CC} = 4.5 V, T_A = –55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.41 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 0.15 mA, I_2 = –0.15 mA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.3 mA, R_1 = 138 Ω		0.22	0.4	V

electrical characteristics (SN7453 circuits) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.62 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 270 μA, I_2 = –270 μA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.43 mA, R_1 = 130 Ω		0.22	0.4	V

6

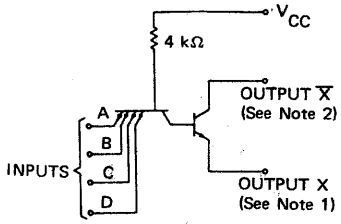
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		13	22	ns

† Expander inputs X and $\overline{X}$ are open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

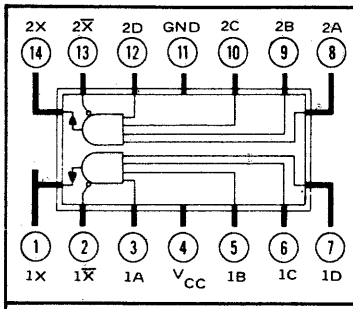
CIRCUIT TYPE SN5460
DUAL 4-INPUT EXPANDER

schematic (each expander)

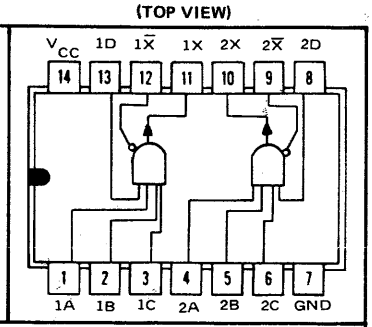


NOTES: 1. Connect to X input of SN5450 or SN5453 circuit.
2. Connect to $\overline{X}$ input of SN5450 or SN5453 circuit.
3. Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: X=ABCD
when connected to X and $\overline{X}$ pins of SN5450 or SN5453 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN5450 or one SN5453 circuit 4

electrical characteristics (unless otherwise noted T_A = –55°C to 125°C)

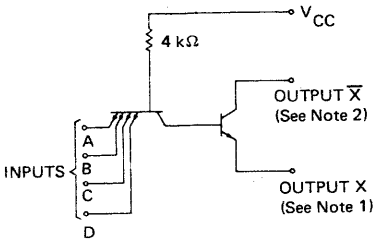
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	31		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	32				0.8	V
V_{on}	On-state output voltage	31	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, R = 1.1 kΩ, T_A = –55°C			0.4	V
I_{off}	Off-state output current	32	V_{CC} = 4.5 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 1.2 kΩ, T_A = –55°C			150	μA
I_{on}	On-state output current	33	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, T_A = –55°C	–0.3			mA
$I_{in(0)}$	Logical 0 level input current (each input)	32	V_{CC} = 5.5 V, V_{in} = 0.4 V			–1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	34	V_{CC} = 5.5 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply curren·	35	V_{CC} = 5.5 V, V_{in} = 5 V, V_1 = 0.85 V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	35	V_{CC} = 5.5 V, V_{in} = 0, V_1 = 0.85 V		2	4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

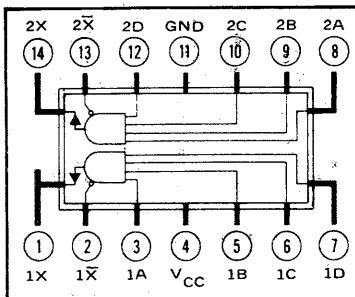
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through SN5450 or SN5453 circuit)	66	C_L = 15 pF, R_L = 400 Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through SN5450 or SN5453 circuit)	66	C_L = 15 pF, R_L = 400 Ω		15	30	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

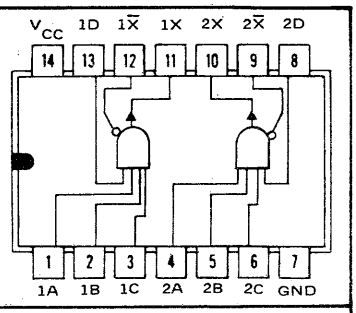
schematic (each expander)



W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: X=ABCD
when connected to X and $\overline{X}$ pins of SN7450 or SN7453 circuit.

NOTES: 1. Connect to X input of SN7450 or SN7453 circuit.
2. Connect to $\overline{X}$ input of SN7450 or SN7453 circuit.
3. Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Maximum number of expanders that may be fanned-in to one SN7450 or one SN7453 Circuit 4

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals is in the on state	31		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal is in the off state	32				0.8	V
V_{on}	On-state output voltage	31	V_{CC} = 4.75 V, V_{in} = 2 V, V_1 = 1 V, R = 1.1 kΩ, T_A = 0°C			0.4	V
I_{off}	Off-state output current	32	V_{CC} = 4.75 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 1.2 kΩ T_A = 0°C			270	μA
I_{on}	On-state output current	33	V_{CC} = 4.75 V, V_{in} = 2 V, V_1 = 1 V	−0.43			mA
$I_{in(0)}$	Logical 0 level input current (each input)	32	V_{CC} = 5.25 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	34	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	35	V_{CC} = 5.25 V, V_{in} = 5 V, V_1 = 0.85 V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	35	V_{CC} = 5.25 V, V_{in} = 0, V_1 = 0.85 V		2	4	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through SN7450 or SN7453)	66	C_L = 15 pF, R_L = 400 Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through SN7450 or SN7453)	66	C_L = 15 pF, R_L = 400 Ω		15	30	ns

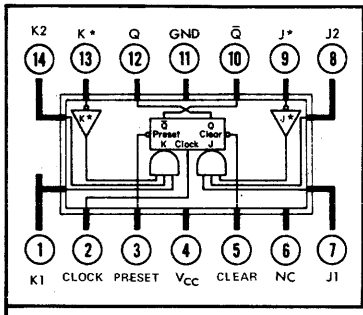
CIRCUIT TYPES SN5470, SN7470
EDGE-TRIGGERED J-K FLIP-FLOPS

logic

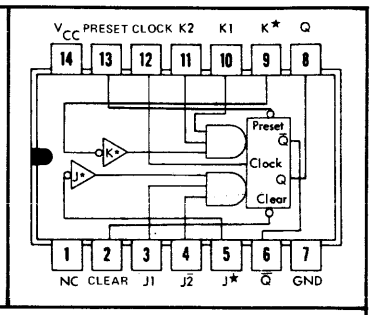
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \cdot J2 \cdot \overline{J^*}$.
2. $K = K1 \cdot K2 \cdot \overline{K^*}$.
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. If inputs J* or K* are not used they must be grounded.
6. NC - No Internal Connection

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

description

These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are ideally suited for medium- to high-speed applications and can result in a significant saving in system power dissipation and package count where input gating is required.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5470 Circuits	4.5	5	5.5	V
SN7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5470 Circuits	−55	25	125	°C
SN7470 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$ (See Figure 68)	5		150	ns
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 68)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 67)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 67)	25			ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

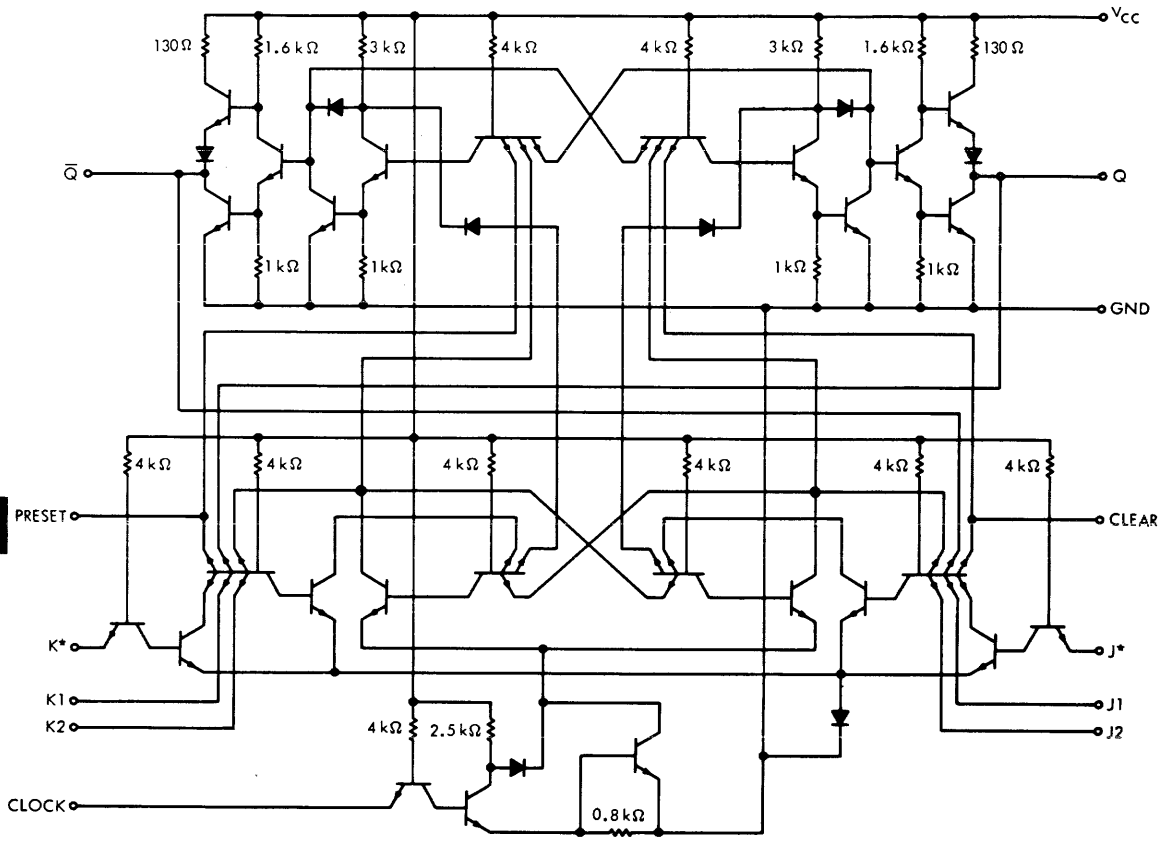
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	36 and 37			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	36 and 37					0.8	V
$V_{out(1)}$	Logical 1 output voltage	36	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	37	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J*, K1, K2, K*, or clock	38	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	38	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J*, K1, K2, K*, or clock	39	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	39	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	40	V_{CC} = MAX, V_{in} = 0	SN5470	−20		−57	mA
				SN7470	−18		−57	
I_{CC}	Supply current	39	V_{CC} = MAX, V_{in} = 5 V			13	26	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	68	C_L = 15 pF, R_L = 400 Ω	20	35		MHz
t_{setup}	Minimum input setup time	68	C_L = 15 pF, R_L = 400 Ω		10	20	ns
t_{hold}	Minimum input hold time	68	C_L = 15 pF, R_L = 400 Ω		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	67	C_L = 15 pF, R_L = 400 Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	67	C_L = 15 pF, R_L = 400 Ω			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	68	C_L = 15 pF, R_L = 400 Ω	10	27	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	68	C_L = 15 pF, R_L = 400 Ω	10	18	50	ns

schematic



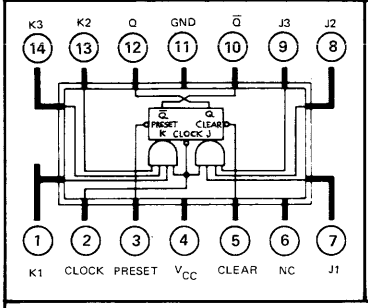
NOTE: Component values shown are nominal.

logic

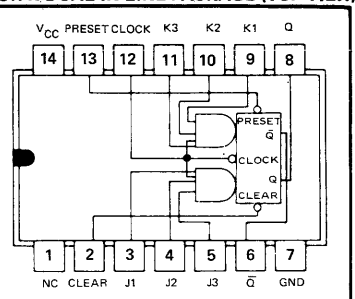
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC = No Internal Connection.

W FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

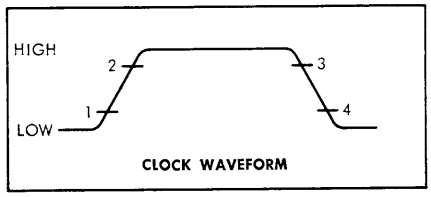


positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



CLOCK WAVEFORM

6

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5472 Circuits	4.5	5	5.5	V
SN7472 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5472 Circuits	−55	25	125	°C
SN7472 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 69)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 70)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 70)	25			ns
Input Setup Time, t_{setup} (See figure 69)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	41 and 42				2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	41 and 42						0.8	V
$V_{out(1)}$	Logical 1 output voltage	41	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	42	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	43	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	43	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	44	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	44	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	45	V_{CC} = MAX,	V_{in} = 0	SN5472	−20		−57	mA
					SN7472	−18		−57	
I_{CC}	Supply current	44	V_{CC} = MAX,	V_{in} = 5 V			10	20	mA

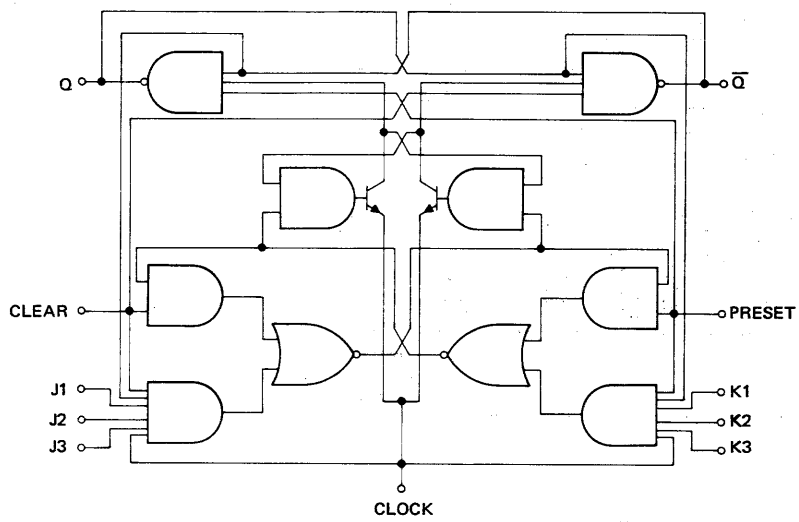
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

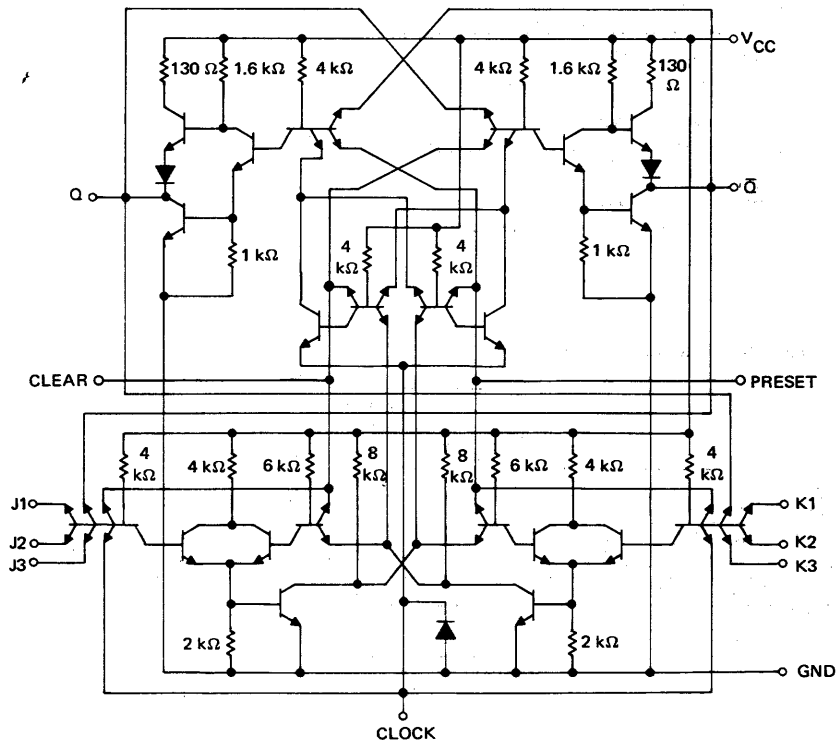
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	69	C_L = 15 pF,	R_L = 400 Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	70	C_L = 15 pF,	R_L = 400 Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	70	C_L = 15 pF,	R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	25	40	ns

6

functional block diagram



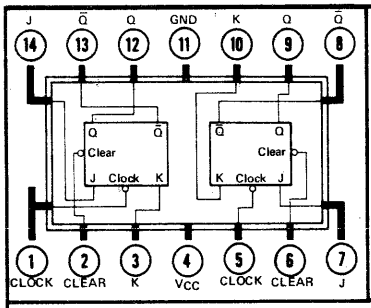
schematic



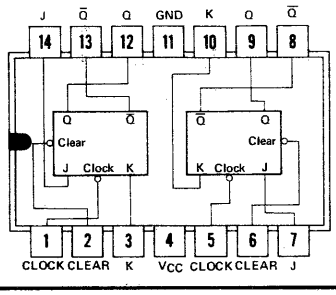
Component values shown are nominal.

CIRCUIT TYPES SN5473, SN54107, SN7473, SN74107
DUAL J-K MASTER-SLAVE FLIPS-FLOPS

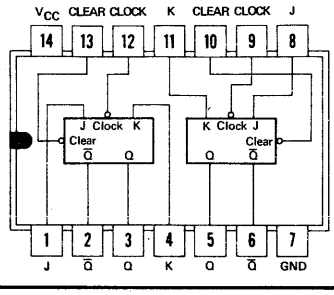
SN5473, SN7473
W FLAT PACKAGE
(TOP VIEW)



SN5473, SN7473
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN54107, SN74107
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic:
Low input to clear sets Q to logical 0.
Clear is independent of clock.

description

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: (See waveform on page 2-26)

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

recommended operating conditions

	SN5473 SN54107			SN7473 SN74107			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 69)	20			20			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 70)	25			25			ns
Input setup time, t_{setup} (See Figure 69)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input hold time, t_{hold}	0			0			
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	46 and 47				2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	46 and 47						0.8	V
$V_{out(1)}$	Logical 1 output voltage	46	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	47	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	48	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	48	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	49	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	49	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	50	V_{CC} = MAX,	V_{in} = 0	SN5473, SN54107	−20		−57	mA
					SN7473, SN74107	−18		−57	
I_{CC}	Supply current	49	V_{CC} = MAX				20	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

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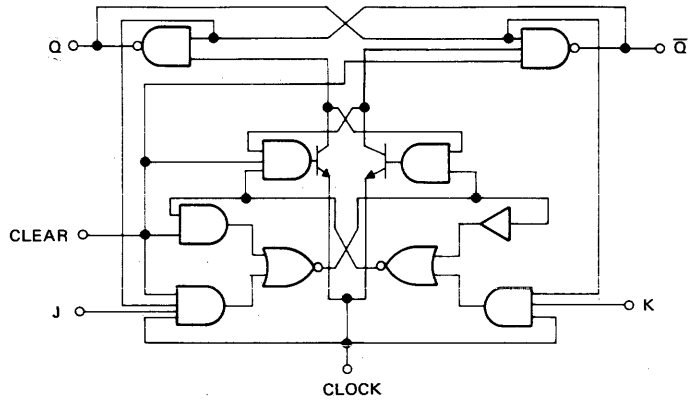
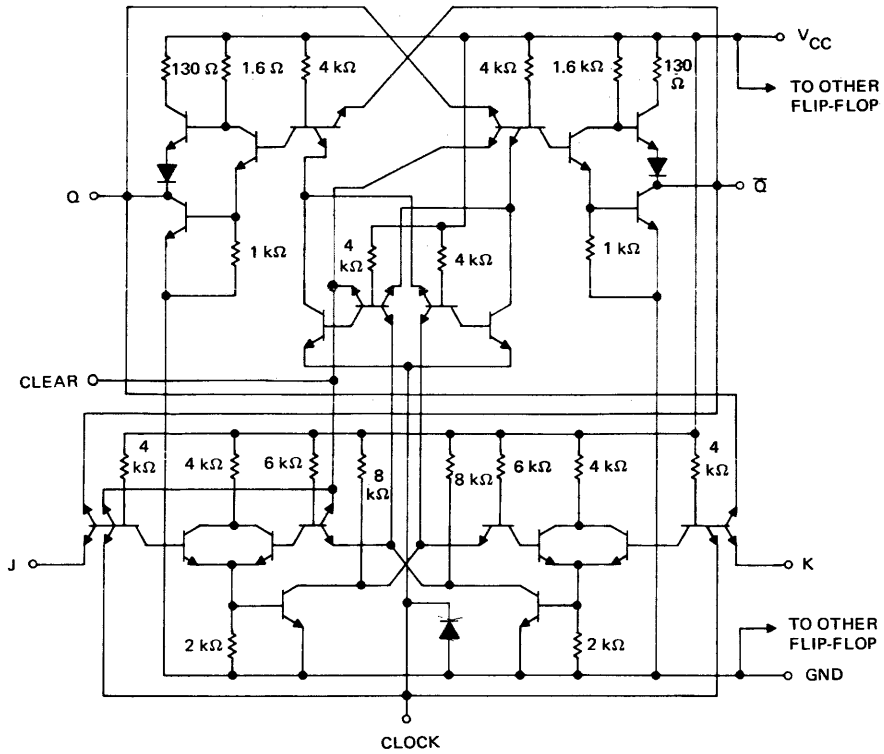
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	69	C_L = 15 pF,	R_L = 400 Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	70	C_L = 15 pF,	R_L = 400 Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	70	C_L = 15 pF,	R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	25	40	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

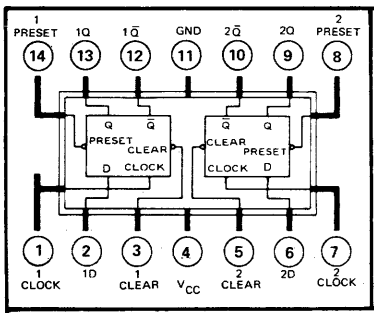
logic

TRUTH TABLE (Each Flip-Flop)

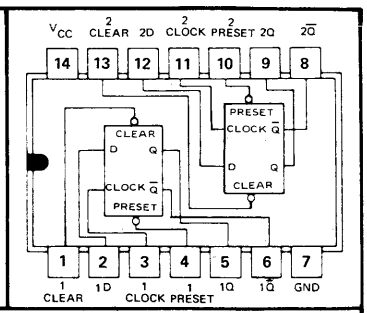
t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These monolithic, dual, D-type, edge-triggered flip-flops feature direct clear and preset inputs and complementary Q and $\bar{Q}$ outputs. Input information is transferrred to the outputs on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

These dual flip-flops have the same clocking characteristics as the SN5470/SN7470 gated (edge-triggered) flip-flop circuits, and both are ideally suited for medium- to-high-speed applications. They can result in a significant saving in system power dissipation and package count in applications where input gating is not required.

recommended operating conditions

	SN5474			SN7474			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 71)	30			30			ns
Width of preset pulse, $t_{p(preset)}$ (See Figure 67)	30			30			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 67)	30			30			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	52 and 53				2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	52 and 53						0.8	V
$V_{out(1)}$	Logical 1 output voltage	52	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	53	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	54	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	54	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	55	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	55	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear	55	V_{CC} = MAX,	V_{in} = 2.4 V				120	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	56	V_{CC} = MAX,	V_{in} = 0	SN5474	−20		−57	mA
					SN7474	−18		−57	
I_{CC}	Supply current	55	V_{CC} = MAX				17	30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

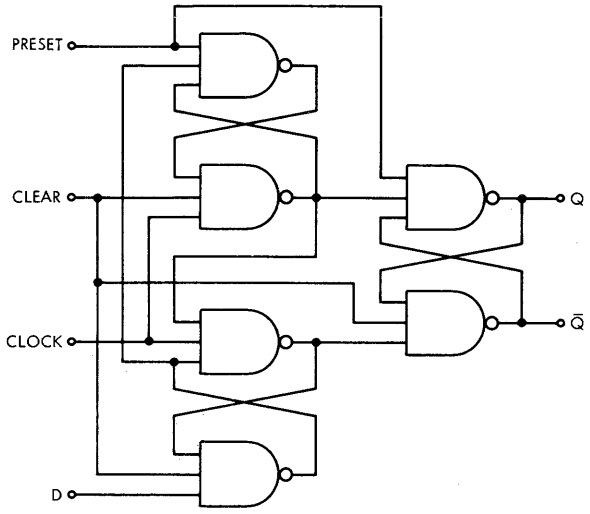
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

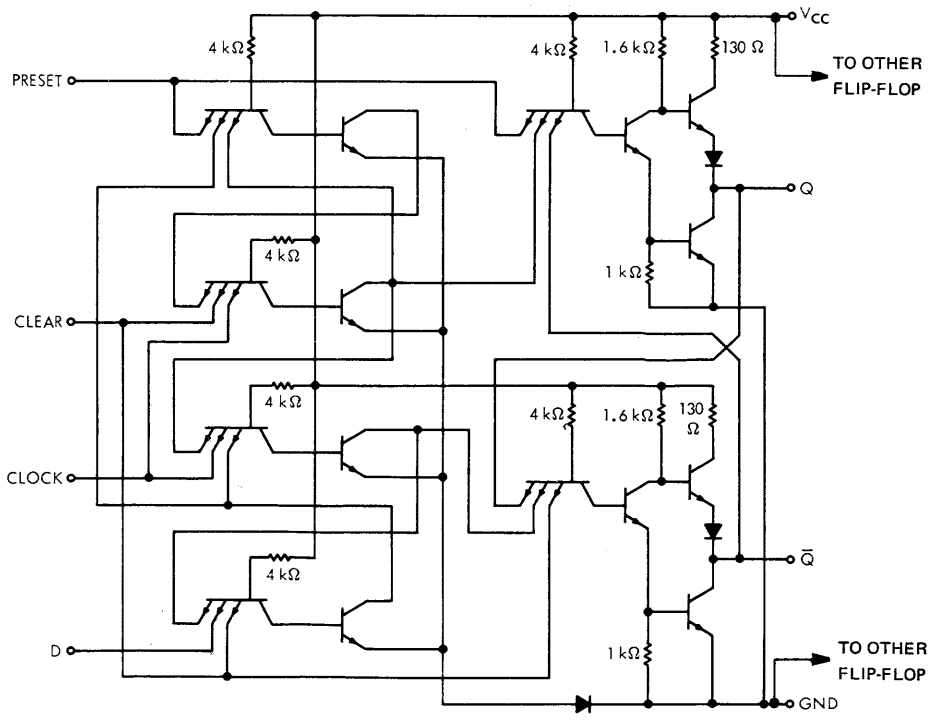
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	71	C_L = 15 pF,	R_L = 400 Ω	15	25		MHz
t_{setup}	Minimum input setup time	71	C_L = 15 pF,	R_L = 400 Ω		15	20	ns
t_{hold}	Minimum input hold time	71	C_L = 15 pF,	R_L = 400 Ω		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	67	C_L = 15 pF,	R_L = 400 Ω			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	67	C_L = 15 pF,	R_L = 400 Ω			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	71	C_L = 15 pF,	R_L = 400 Ω	10	14	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	71	C_L = 15 pF,	R_L = 400 Ω	10	20	40	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

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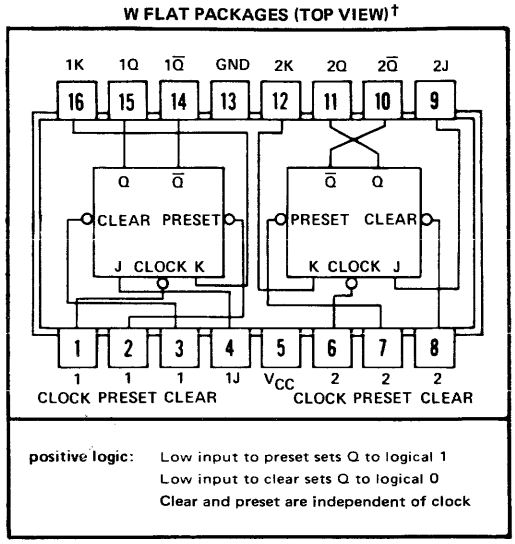
CIRCUIT TYPES SN5476, SN7476
DUAL J-K MASTER-SLAVE FLIP-FLOPS
WITH PRESET AND CLEAR

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)†



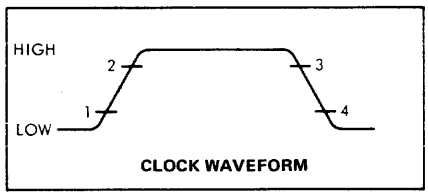
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent of clock

†Pin assignments for these circuits are the same for all packages.

description

The SN7476 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5476 Circuits	4.5	5	5.5	V
SN7476 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5476 Circuits	−55	25	125	°C
SN7476 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 69)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 70)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 70)	25			ns
Input Setup Time, t_{setup} (See figure 69)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

electrical characteristics, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	46 and 47			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	46 and 47					0.8	V
$V_{out(1)}$	Logical 1 output voltage	46	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	47	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	48	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear, preset, or clock	48	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	49	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear, preset, or clock	49	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	51	V_{CC} = MAX, V_{in} = 0	SN5476	−20		−57	mA
				SN7476	−18		−57	
I_{CC}	Supply current (each flip-flop)	49	V_{CC} = MAX			20	40	mA

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	69	C_L = 15 pF, R_L = 400 Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 0 level from clear or preset to output	70	C_L = 15 pF, R_L = 400 Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 1 level from clear or preset to output	70	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF, R_L = 400 Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF, R_L = 400 Ω	10	25	40	ns

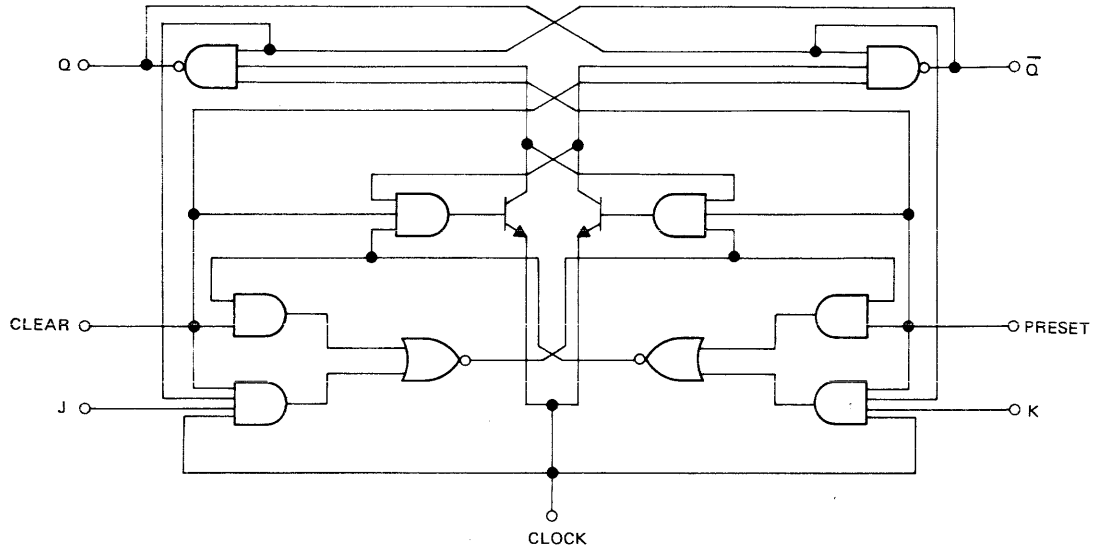
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

CIRCUIT TYPES SN5476, SN7476
DUAL J-K MASTER-SLAVE FLIP-FLOPS
WITH PRESET AND CLEAR

functional block diagram (each flip-flop)



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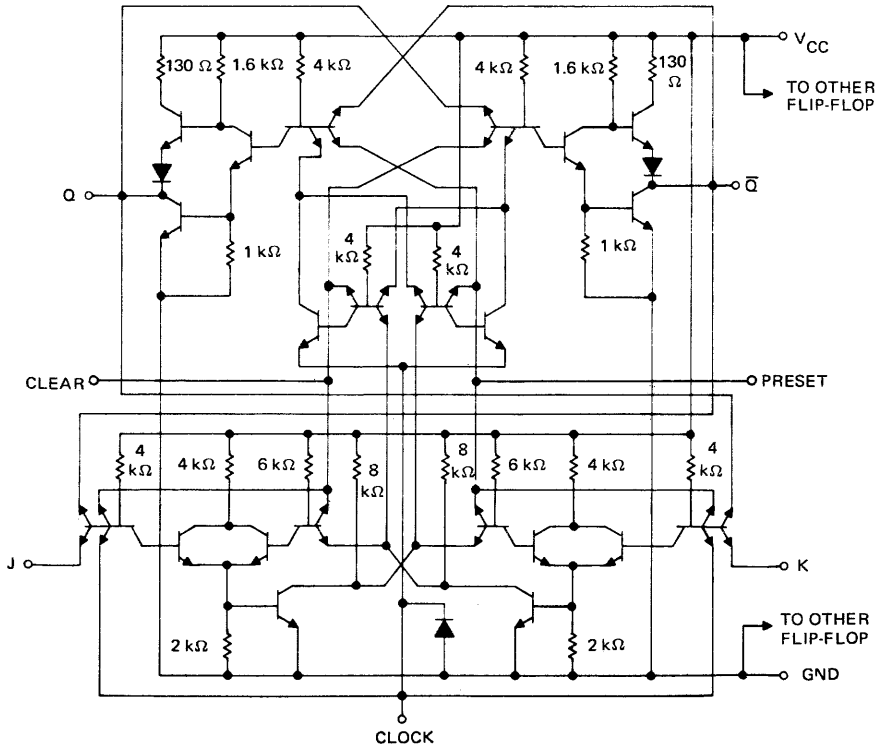
schematic (each flip-flop)



NOTE: Component values shown are nominal.

CIRCUIT TYPES SN54104, SN54105, SN74104, SN74105
GATED J-K MASTER-SLAVE FLIP-FLOPS

featuring

- Buffered Clock Input
- Direct Preset and Clear
- Common JK Gate Input

logic

TRUTH TABLE

INPUTS AT t_n			OUTPUTS AT t_{n+1}	
JK	J†	K†	Q	$\overline{Q}$
L‡	X	X	Q_n	$\overline{Q}_n$
H	L‡	L‡	Q_n	$\overline{Q}_n$
H	L	H	L	H
H	H	L	H	L
H	H	H	$\overline{Q}_n$	Q_n

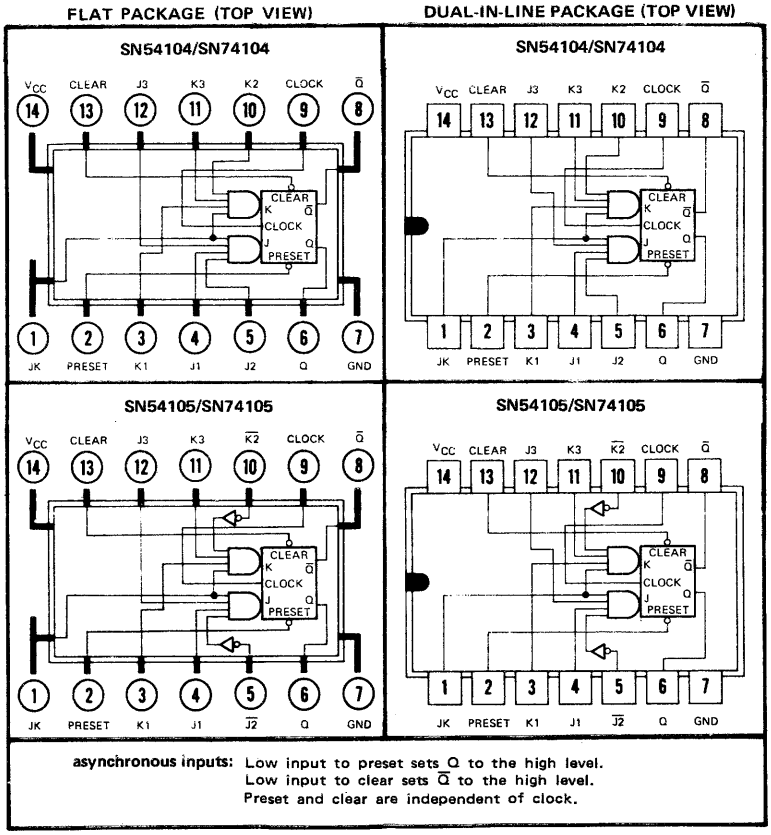
† SN54104/SN74104: J = J1 · J2 · J3,
K = K1 · K2 · K3
SN54105/SN74105: J = J1 · $\overline{J2}$ · J3,
K = K1 · $\overline{K2}$ · K3

‡ These low levels must be maintained while the clock is low

NOTES:
A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.
C. H = high, L = low, X = irrelevant.

W
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



asynchronous inputs: Low input to preset sets Q to the high level.
Low input to clear sets $\overline{Q}$ to the high level.
Preset and clear are independent of clock.

description

These J-K master-slave flip-flops feature a buffered clock input, direct preset and clear, gated J and K inputs, and a common JK input. The clock buffer offers typical TTL high noise immunity, low clock-line loading, and, in most cases, eliminates the need for stringent control of system-clock rise and fall times. When activated, the direct preset and clear inputs control the state of both the master and slave flip-flops independent of the clock and synchronous-input states. Gated inputs may be used to perform a wide variety of control functions without the need for external gates, and the common JK input simplifies hardware design for applications utilizing a single gate-control source.

Due to the internal clock buffer, the JK input gates accept data when the clock line is low, and transfer of data from the master to the slave occurs during the clock-line transition from the low state to the high state. When the clock line is high, the data inputs are inhibited.

The SN54104/SN74104 includes internal capacitive loading on the J and K input gates and, as the input setup and hold times are lengthened, this circuit displays improved performance in systems where appreciable clock skew is anticipated.

The SN54105/SN74105 offers an inverting data input to each of the J and K input gates for additional control flexibility. As the input setup and hold times are not lengthened, this circuit permits operation at higher toggle rates than the SN54104/SN74104.

These TTL circuits feature one-volt typical d-c noise margins and are compatible for use with most TTL and DTL families. Full fan-out to 10 normalized Series 54/74 loads is available from the outputs. The SN54104 and SN54105 circuits are characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74104 and SN74105 circuits are characterized for operation from 0°C to 70°C.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (See Note 1) . . . . . 8 V
Input voltage (See Note 1) . . . . . −1.5 V to 5.5 V
Voltage applied to any output (See Note 2) . . . . . −0.5 V to V_{CC}
Operating free-air temperature range: SN54104, SN54105 Circuits . . . . . −55°C to 125°C
SN74104, SN74105 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage V_{CC} (See Note 1)	SN54104, SN54105		4.5	5	5.5	V
	SN74104, SN74105		4.75	5	5.25	
Operating free-air temperature range	SN54104, SN54105		−55	25	125	°C
	SN74104, SN74105		0	25	70	
Width of low-level clock pulse, $t_{w(clock)}$ (See Figure 112)			15†			ns
Width of preset and clear pulse, $t_{w(preset)}$ and $t_{w(clear)}$			20†			ns
Input release time for low-level data, $t_{release(L)}$ (See Note 3 and Figure 113)	SN54104, SN74104				10†	ns
	SN54105, SN74105				1†	
Input setup time for high-level data, $t_{setup(H)}$ (See Note 4 and Figure 113)	SN54104, SN74104		35†			ns
	SN54105, SN74105		10†			

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This rating applied at the Q output with preset held low and at the $\overline{Q}$ output with clear held low.
3. Release time for low-level data is an interval between the release of low-level data and the positive-going edge of the clock pulse; this interval being sufficiently short to ensure recognition of the low-level data.
4. Setup time for high-level data is an interval between the arrival of the high-level data and the positive-going edge of the clock pulse; this interval being sufficiently long to ensure recognition of the high-level data.

†These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	107 and 108		T_A = MIN	2			V
				T_A = 25°C	1.7			
				T_A = MAX	1.4			
V_{IL}	Low-level input voltage	107 and 108		T_A = MIN			0.8	V
				T_A = 25°C			0.9	
				T_A = MAX			0.8	
V_{OH}	High-level output voltage	107	V_{CC} = MIN, I_{OH} = −1 mA		2.4	2.7		V
V_{OL}	Low-level output voltage	108	V_{CC} = MAX, I_{OL} = 17.7 mA			0.2	0.4	V
			V_{CC} = MIN, I_{OL} = 16 mA			0.2	0.4	
I_{IH}	High-level input current into any input except JK, preset, or clear	109	V_{CC} = MAX, V_I = 4.5 V	T_A = 25°C		2	40	μA
				T_A = MAX			40	
I_{IH}	High-level input current into JK	109	V_{CC} = MAX, V_I = 4.5 V	T_A = 25°C		4	80	μA
				T_A = MAX			80	
I_{IH}	High-level input current into preset or clear	109	V_{CC} = MAX, V_I = 4.5 V	T_A = 25°C		8	120	μA
				T_A = MAX			120	
I_{IL}	Low-level input current into any input except JK, preset, or clear	110	V_{CC} = MAX, V_I = 0.4 V			−1.1	−1.6	mA
			V_{CC} = MIN, V_I = 0.4 V			−0.9	−1.45	
I_{IL}	Low-level input current into JK	110	V_{CC} = MAX, V_I = 0.4 V			−2.2	−3.2	mA
			V_{CC} = MIN, V_I = 0.4 V			−1.8	−2.9	
I_{IL}	Low-level input current into preset or clear	110	V_{CC} = MAX, V_I = 0.4 V			−3	−4.75	mA
			V_{CC} = MIN, V_I = 0.4 V			−2.5	−3.9	
I_{CC}	Supply current	111	V_{CC} = 5 V	SN54104, SN74104		15	24	mA
				SN54105, SN74105		17	28	

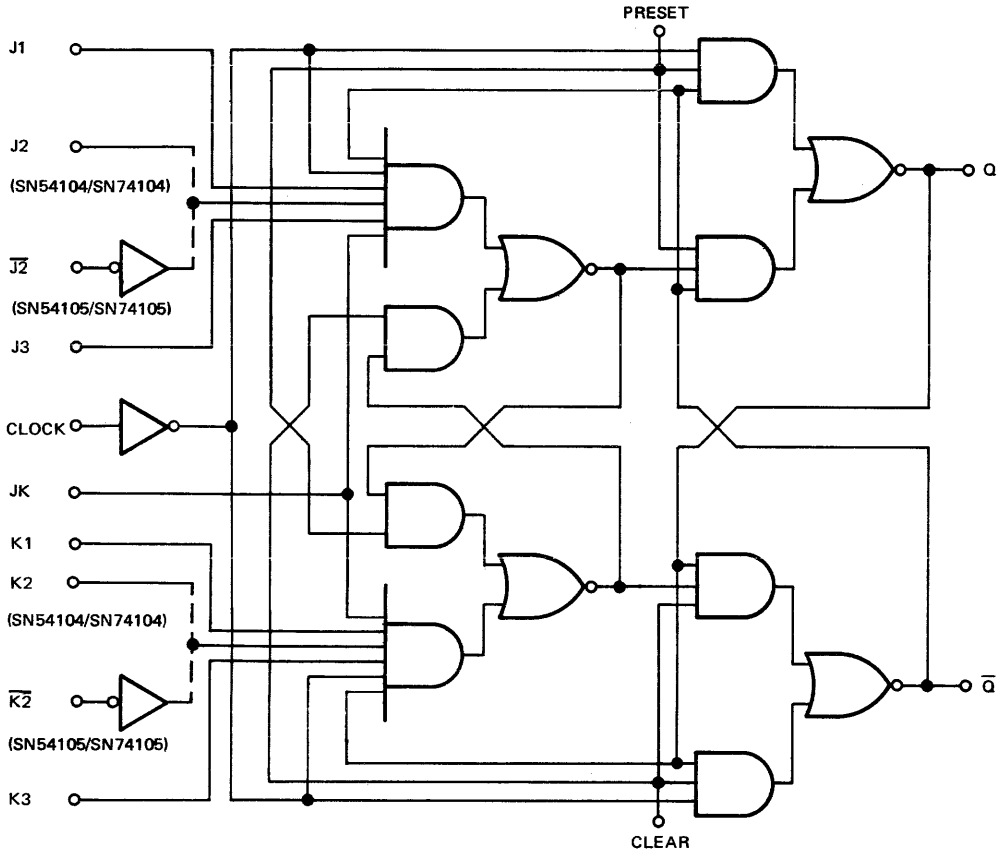
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from clock	112	C_L = 15 pF, R_L = 400 Ω		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock	112	C_L = 15 pF, R_L = 400 Ω		16	25	ns

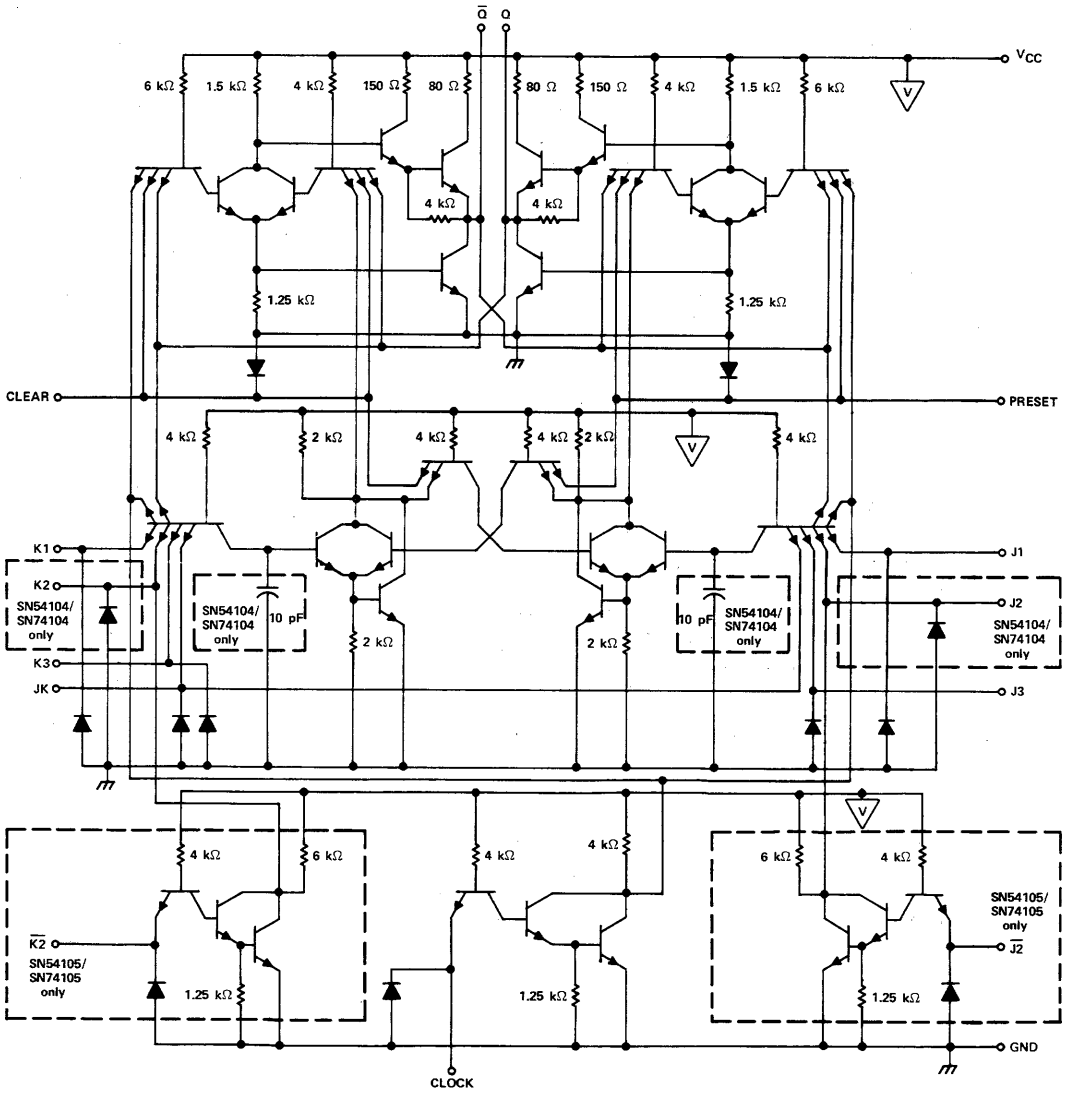
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

functional block diagram



schematic



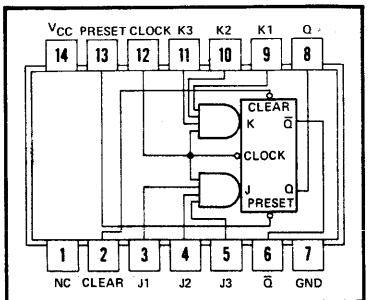
Component values shown are nominal.

▽ . . . V_{CC} bus

CIRCUIT TYPES SN54110, SN74110
GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

- Data Lockout Solves Clock-Skew Problems
- Improved Immunity to Noise
- Input-Clamping Diodes Simplify System Design
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL, DTL, and MSI Circuits
- Typical Maximum Input Clock Frequency . . . 25 MHz

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

†Pin assignments for these circuits are the same for all packages.
NC—No internal connection.

description

The SN54110 and SN74110 are d-c coupled, variable-skew, J-K flip-flops which utilize TTL circuitry to obtain 25-MHz performance typically. They are termed "variable-skew" because they allow the maximum clock skew in a system to be a direct function of the clock pulse width. The J and K inputs are enabled only during a short period (20 nanoseconds maximum setup time plus 5 nanoseconds maximum hold time) on the rising edge of the clock pulse as shown in the timing diagram, Figure 1. After this, inputs may be changed while the clock is at the high level without affecting the state of the master. On the threshold level of the falling edge of the clock pulse, the data stored in the master during the rising edge will be transferred to the output. The effective allowable clock skew then is minimum propagation delay time minus hold time, plus clock pulse width. This means that the system designer can set the maximum allowable clock skew needed by varying the clock pulse width. Thus system design is made easier and the requirements for sophisticated clock distribution systems are minimized or, in some cases, entirely eliminated. These flip-flops have an additional feature—the synchronous input has reduced sensitivity to data change while the clock is high because the data need be present for only a short period of time and the system's susceptability to noise is thereby effectively reduced.

The SN54110/SN74110 has the same functional advantage as the SN5472/SN7472 in that three-input AND logic is provided for both the J and K data functions. Preset and clear inputs, which are completely independent of the state of the clock, are also provided. The SN54110 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74110 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

INPUTS AT t_n		OUTPUT AT t_{n+1}
J‡	K‡	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

H = high level, L = low level
NOTES: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.
‡ J = J1 • J2 • J3
K = K1 • K2 • K3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54110 Circuits . . . . . −55°C to 125°C
SN74110 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the J input with respect to clear and clock, and to the K input with respect to preset and clock.

recommended operating conditions

		SN54110			SN74110			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}		0		20†	0		20†	MHz
Width of clock pulse, $t_{w(clock)}$		25†			25†			ns
Width of preset pulse, $t_{w(preset)}$		25†			25†			ns
Width of clear pulse, $t_{w(clear)}$		25†			25†			ns
Input setup time, high-level or low-level data, t_{setup} (see Note 3 and Figure 114)		20†			20†			ns
Input hold time, high-level or low-level data, t_{hold} (see Note 4)		5†			5†			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

4. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to insure its recognition.

†These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡	MIN	TYP§	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −800 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	J, K, or clock input	V_{CC} = MAX, V_I = 2.4 V			40	μA
		preset or clear input				160	
I_{IL}	Low-level input current	J, K, or clock input	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
		preset or clear input				−3.2	
I_{OS}	Short-circuit output current¶		V_{CC} = MAX	−20		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 5		20	34	mA

NOTE 5: With J and K inputs grounded, the clock input at 4.5 V, and the outputs open, I_{CC} is tested first with clear at 4.5 V and preset grounded, then with clear grounded and preset at 4.5 V.

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§All typical values are at V_{CC} = 5 V, T_A = 25°C.

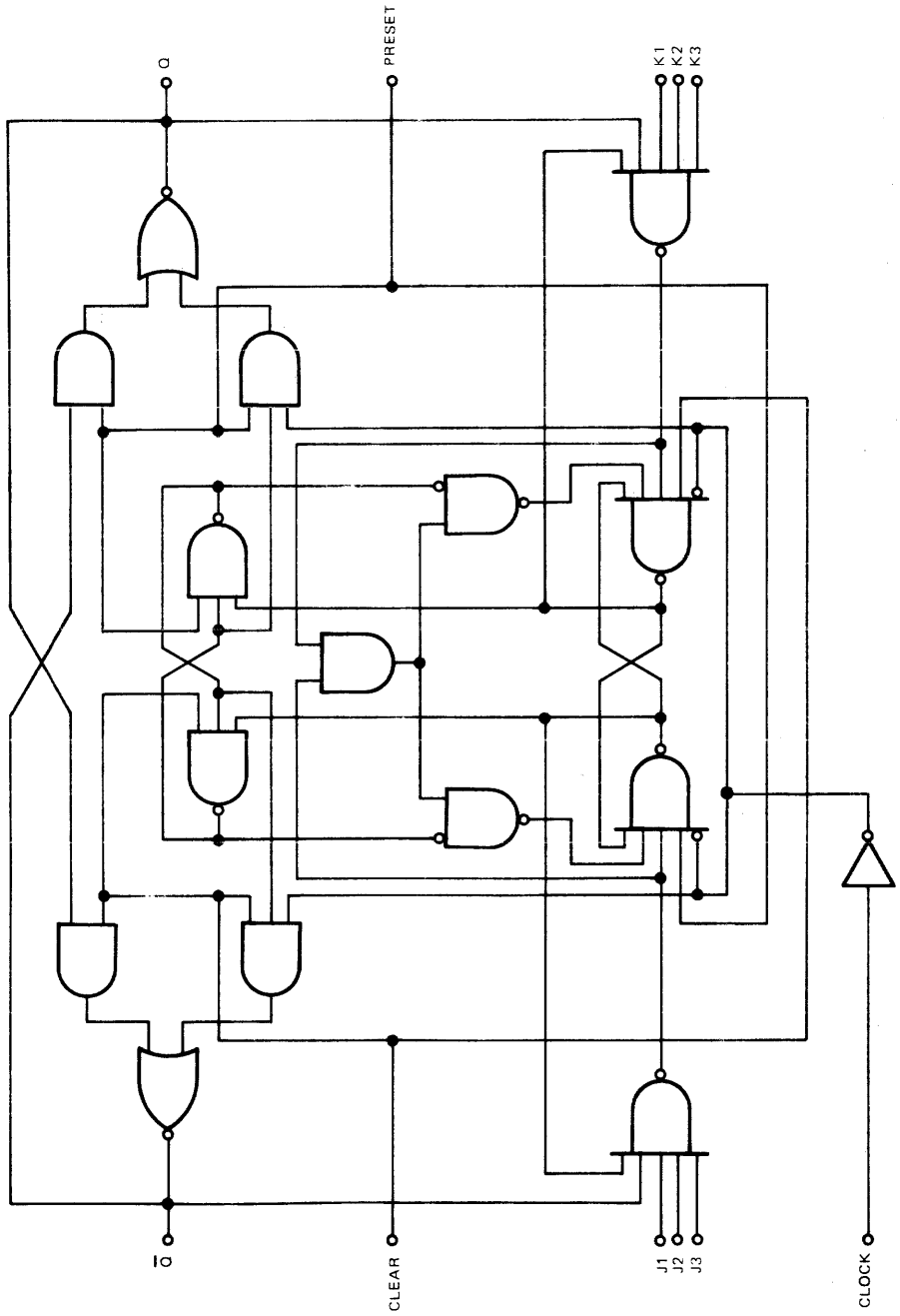
¶Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 114	20	25		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			18	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		10	20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		6	13	20	ns

6

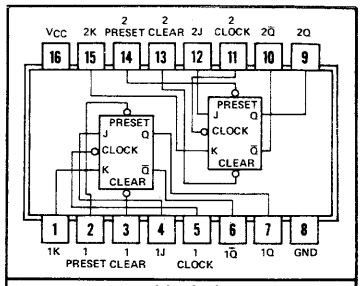
functional block diagram



CIRCUIT TYPES SN54111, SN74111
DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

- Data Lockout Solves Clock-Skew Problems
- Improved Immunity to Noise
- Input-Clamping Diodes Simplify System Design
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL, DTL, and MSI Circuits
- Typical Maximum Input Clock Frequency . . . 25 MHz

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

†Pin assignments for these circuits are the same for all packages.

description

The SN54111 and SN74111 are d-c coupled, variable-skew, J-K flip-flops which utilize TTL circuitry to obtain 25-MHz performance typically. They are termed "variable-skew" because they allow the maximum clock skew in a system to be a direct function of the clock pulse width. The J and K inputs are enabled to accept data only during a short period (30 nanoseconds maximum hold time) starting with, and immediately following, the rising edge of the clock pulse as shown in the timing diagram, Figure 1. After this, inputs may be changed while the clock is at the high level without affecting the state of the master. At the threshold level of the falling edge of the clock pulse, the data stored in the master will be transferred to the output. The effective allowable clock skew then is minimum propagation delay time minus hold time, plus clock pulse width. This means that the system designer can set the maximum allowable clock skew needed by varying the clock pulse width. Thus system design is made easier and the requirements for sophisticated clock distribution systems are minimized or, in some cases, entirely eliminated. These flip-flops have an additional feature—the synchronous input has reduced sensitivity to data change while the clock is high because the data need be present for only a short period of time and the system's susceptibility to noise is thereby effectively reduced.

The SN54111 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74111 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

INPUTS AT t_n		OUTPUT AT t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

H = high level, L = low level
NOTES: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54111 Circuits	−55°C to 125°C
SN74111 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the J input with respect to clear and clock, and to the K input with respect to preset and clock.

recommended operating conditions

		SN54111			SN74111			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of preset pulse, $t_{w(preset)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		25			25			ns
Input setup time, high-level or low-level data, t_{setup} (see Figure 115)		0			0			ns
Input hold time, high-level or low-level data, t_{hold} (see Figure 115)		30			30			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −800 μA	V_{IH} = 2 V,	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	J or K input	V_{CC} = MAX,	V_I = 2.4 V			40	μA
		Clear or Preset input					80	
		Clock input					120	
I_{IL}	Low-level input current	J or K input	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		Clear or Preset input					−3.2	
		Clock input					−4.8	
I_{OS}	Short-circuit output current §		V_{CC} = MAX	SN54111	−20		−57	mA
				SN74111	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3		28	41	mA

NOTE 3: With J and K inputs grounded, the clock input at 4.5 V, and the outputs open, I_{CC} is tested first with clear at 4.5 V and preset grounded, then with clear grounded and preset at 4.5 V.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

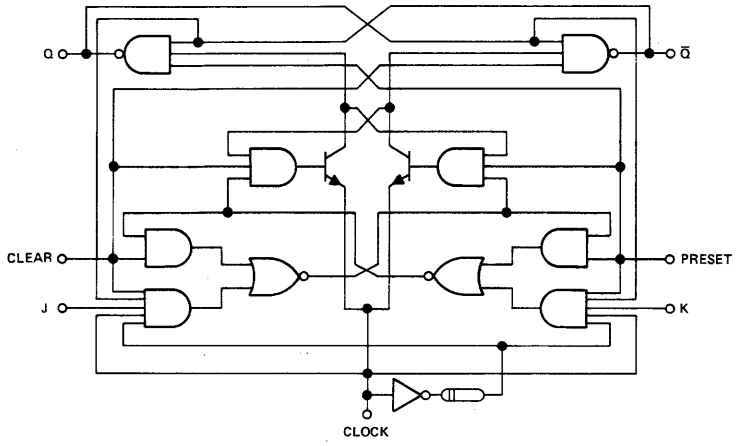
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, See Figure 115	R_L = 400 Ω,	20	25		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset				12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset				21	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			6	12	17	ns
t_{PHL}	Propaagtion delay time, high-to-low-level output from clock			10	20	30	ns

functional block diagram (each flip-flop)



CIRCUIT TYPES SN54121, SN74121
MONOSTABLE MULTIVIBRATORS

logic

TRUTH TABLE (See Notes 1 thru 3)

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

$1 = V_{in(1)} \geq 2\ V$

$0 = V_{in(0)} \leq 0.8\ V$

NOTES: 1. t_n = time before input transition.

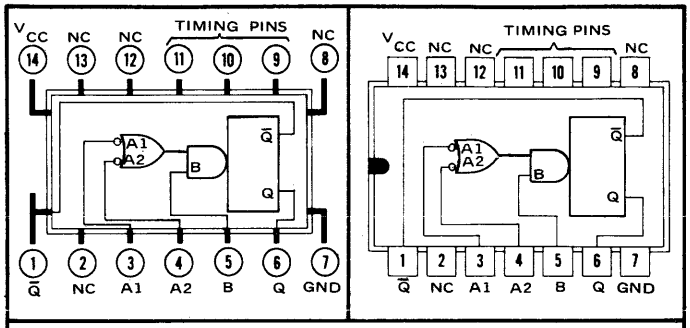
2. t_{n+1} = time after input transition.

3. X indicates that either a logical 0 or 1 may be present.

4. NC = No Internal Connection.

W FLAT PACKAGE
(TOP VIEW)
(See Notes 6 thru 9)

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)
(See Notes 6 thru 9)



positive logic: see truth table and notes 5 and 6

5. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
6. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
7. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of typically 30 ns is obtained.
8. To use the internal timing resistor (2 kΩ nominal), connect pin (9) to pin (14).
9. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
10. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.

description

This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL compatible and featuring temperature-independent backlash, See Figure L) for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i.e., pin (9) connected to pin (14), pins (10), (11) open) an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

description (continued)

Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 40 kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwatts at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwatts.

Duty cycles as high as 90% are achieved when using R_T = 40 kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54121 Circuits	4.5	5	5.5	V
SN74121 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Input Pulse Rise/Fall Time: Schmitt Input (B)			1	V/s
Logic Inputs (A1, A2)			1	V/μs
Input Pulse Width	50			ns
External Timing Resistance Between Pins (11) and (14) (Pin (9) open)	1.4			kΩ
External Timing Resistance: SN54121			30	kΩ
SN74121			40	kΩ
Timing Capacitance	0		1000	μF
Output Pulse Width			40	s
Duty Cycle: R_T = 2 kΩ			67%	
R_T = 30 kΩ (SN54121) or R_T = 40 kΩ (SN74121)			90%	

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electrical characteristics over operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNITS
V_{T+}	Positive-going threshold voltage at A input	57	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	57	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	57	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	57	V_{CC} = MIN		0.8	1.35		V
$V_{out(0)}$	Logical 0 output voltage	57	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$V_{out(1)}$	Logical 1 output voltage	57	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.3		V
$I_{in(0)}$	Logical 0 level input current at A1 or A2	58	V_{CC} = MAX, V_{in} = 0.4 V			−1	−1.6	mA
$I_{in(0)}$	Logical 0 level input current at B	59	V_{CC} = MAX, V_{in} = 0.4 V			−2	−3.2	mA
$I_{in(1)}$	Logical 1 level input current at A1 or A2	60	V_{CC} = MAX, V_{in} = 2.4 V			2	40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			0.05	1	mA
$I_{in(1)}$	Logical 1 level input current at B	61	V_{CC} = MAX, V_{in} = 2.4 V			4	80	μA
			V_{CC} = MAX, V_{in} = 5.5 V			0.05	1	mA
I_{OS}	Short circuit output current at Q or $\overline{Q}$§	62 and 63	V_{CC} = MAX	SN54121	−20	−25	−55	mA
				SN74121	−18	−25	−55	
I_{CC}	Power supply current in quiescent (unfired) state	64	V_{CC} = MAX			13	25	mA
I_{CC}	Power supply current in fired state	64	V_{CC} = MAX			23	40	mA

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†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logical 1 level from B input to Q output	72	C_L = 15 pF,	C_T = 80 pF	15	35	55	ns
t_{pd1}	Propagation delay time to logical 1 level from A1/A2 inputs to Q output				25	45	70	ns
t_{pd0}	Propagation delay time to logical 0 level from B input to $\overline{Q}$ output	72	C_L = 15 pF,	C_T = 80 pF	20	40	65	ns
t_{pd0}	Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{Q}$ output				30	50	80	ns
$t_{p(out)}$	Pulse width obtained using internal timing resistor	73	C_L = 15 pF, R_T = Open,	C_T = 80 pF, Pin ⑨ to V_{CC}	70	110	150	ns
$t_{p(out)}$	Pulse width obtained with zero timing capacitance	73	C_L = 15 pF, R_T = Open,	C_T = 0, Pin ⑨ to V_{CC}	20	30	50	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	73	C_L = 15 pF, R_T = 10 kΩ,	C_T = 100 pF, Pin ⑨ Open	600	700	800	ns
			C_L = 15 pF, R_T = 10 kΩ,	C_T = 1 μF, Pin ⑨ Open	6	7	8	ms
t_{hold}	Minimum duration of trigger pulse	73	C_L = 15 pF, R_T = Open,	C_T = 80 pF, Pin ⑨ to V_{CC}		30	50	ns

TYPICAL CHARACTERISTICS§

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

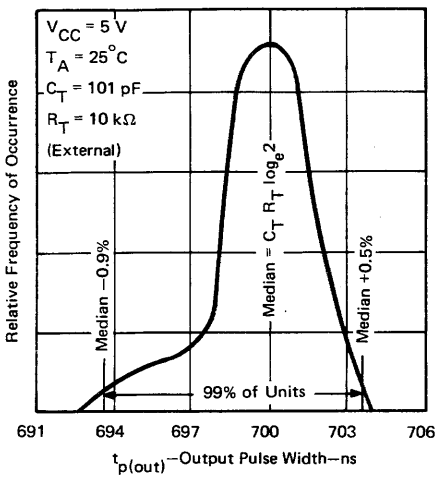


FIGURE H

VARIATION IN INTERNAL TIMING RESISTOR VALUE
vs
FREE-AIR TEMPERATURE

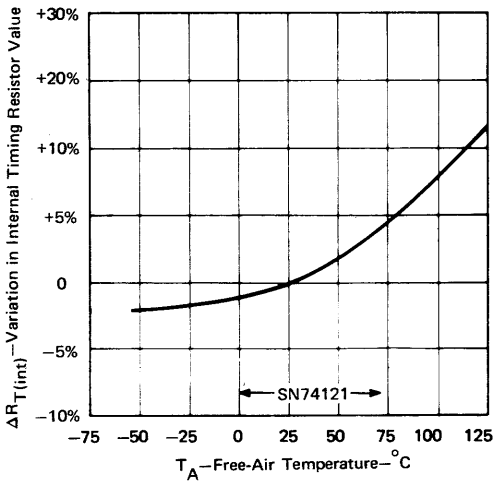


FIGURE I

6

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

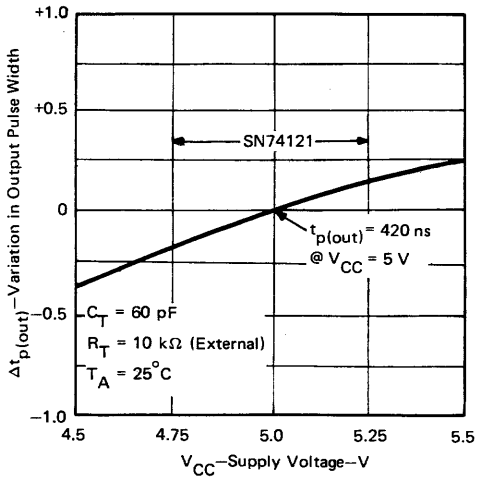


FIGURE J

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

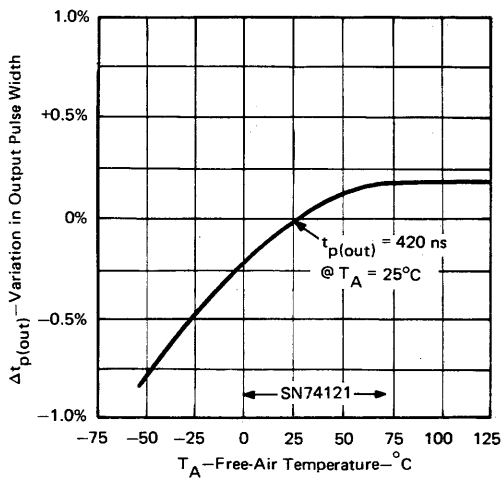


FIGURE K

§ Unless otherwise noted data is applicable for SN54121 and SN74121.

TYPICAL CHARACTERISTICS§

SCHMITT TRIGGER THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

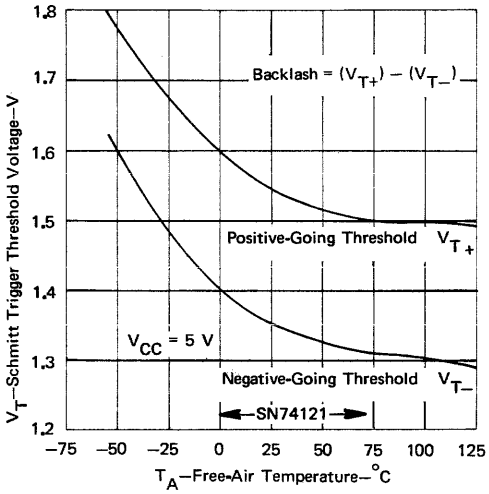


FIGURE L

6

PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL
(B INPUT TO Q OUTPUT)
vs
FREE-AIR TEMPERATURE

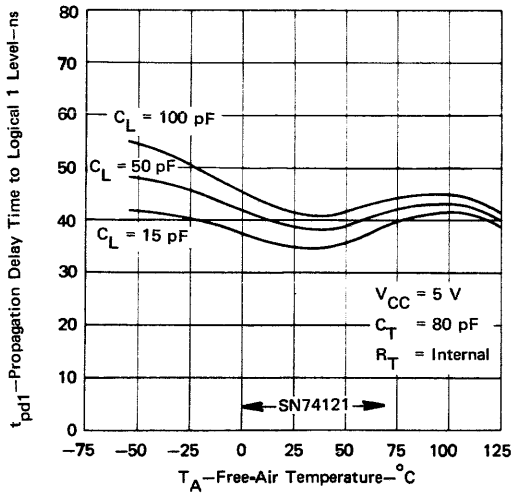


FIGURE M

PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL
(B INPUT TO $\overline{Q}$ OUTPUT)
vs
FREE-AIR TEMPERATURE

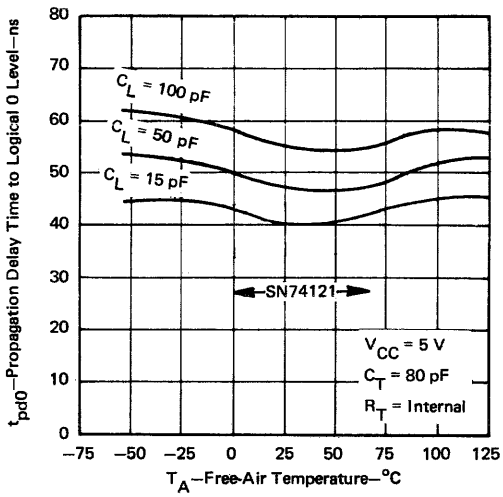


FIGURE N

§Unless otherwise noted data is applicable for SN54121 and SN74121.

TYPICAL CHARACTERISTICS §

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

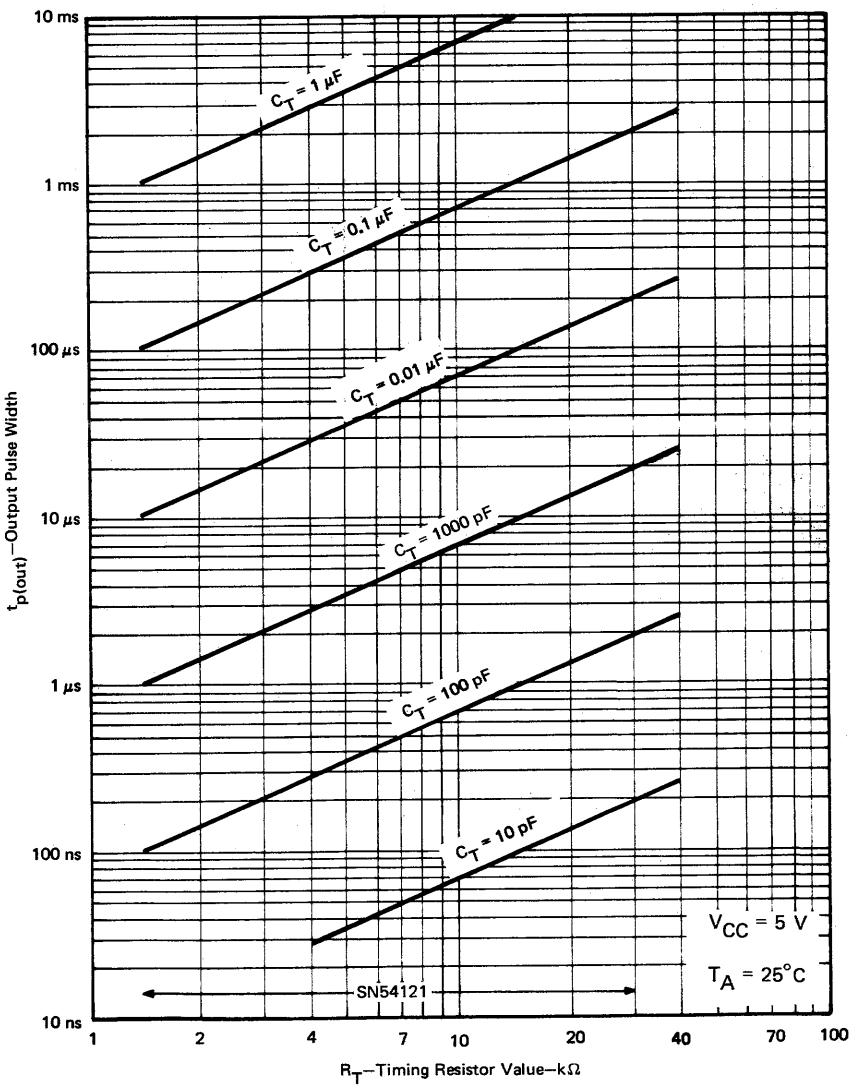


FIGURE O

§Unless otherwise noted data is applicable for SN54121 and SN74121.

6

TYPICAL CHARACTERISTICS §

OUTPUT PULSE WIDTH
vs
EXTERNAL CAPACITANCE

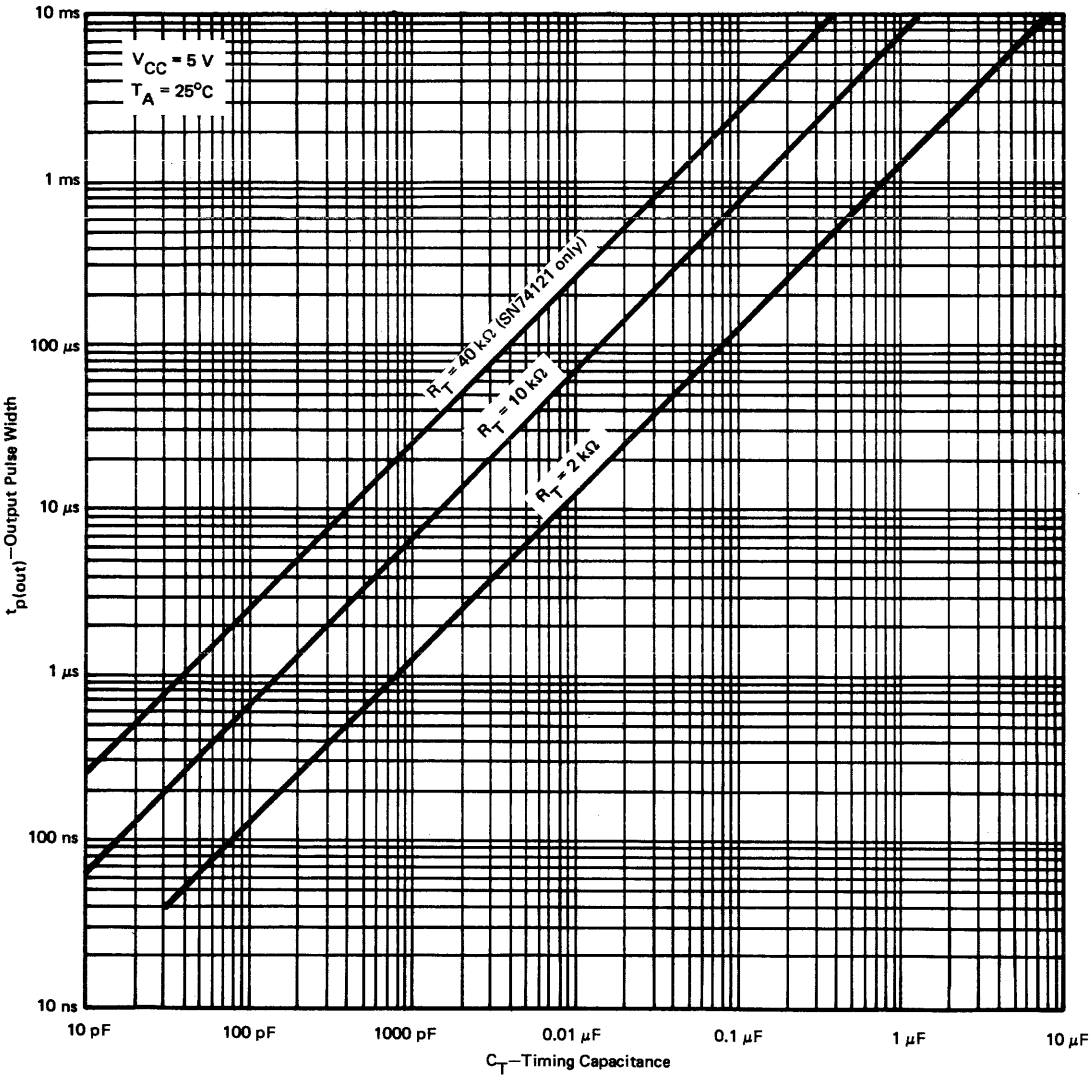


FIGURE P

§ Unless otherwise noted data is applicable for SN54121 and SN74121.

CIRCUIT TYPES SN54122, SN54123, SN74122, SN74123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

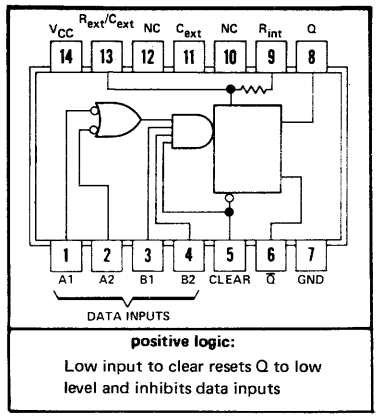
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Diode-Clamped Inputs
- D-C Triggered from High- or Low-Level Gated Logic Inputs
- Compatible for Use with TTL or DTL
- Typical Average Propagation Delay to Output Q . . . 21 ns

logic

SN54122, SN74122
TRUTH TABLE
(See Note A)

INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎏
L	X	H	↑	⎍	⎏
X	L	H	H	L	H
X	L	↑	H	⎍	⎏
X	L	H	↑	⎍	⎏
H	↓	H	H	⎍	⎏
↓	↓	H	H	⎍	⎏
↓	H	H	H	⎍	⎏

SN54122, SN74122
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†
(SEE NOTES B THRU D)

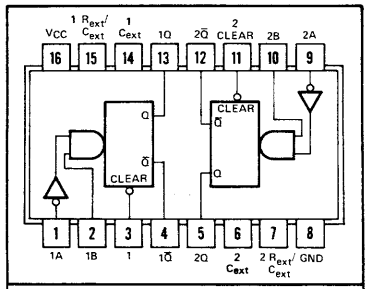


positive logic:
Low input to clear resets Q to low level and inhibits data inputs

SN54123, SN74123
TRUTH TABLE
(See Note A)

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎏
↓	H	⎍	⎏

SN54123, SN74123
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†
(SEE NOTE D)



positive logic:
Low input to clear resets Q to low level and inhibits data inputs

†Pin assignments for these circuits are the same for all packages.

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎏ = one low-level pulse, X = irrelevant (any input, including transitions).
B. NC = No internal connection.
C. To use the internal timing resistor of SN54122/SN74122 (10 kΩ nominal), connect R_{int} to V_{CC}.
D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

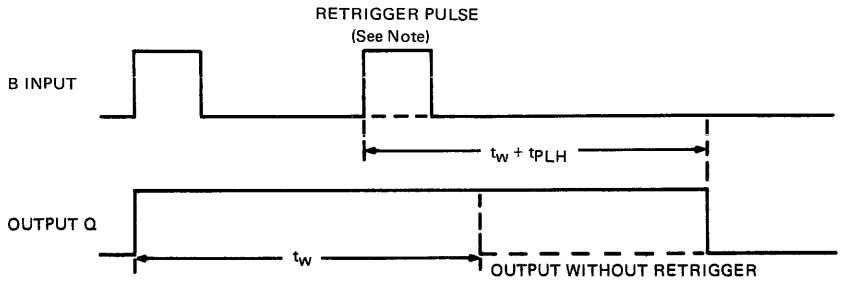
6

CIRCUIT TYPES SN54122, SN54123, SN74122, SN74123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

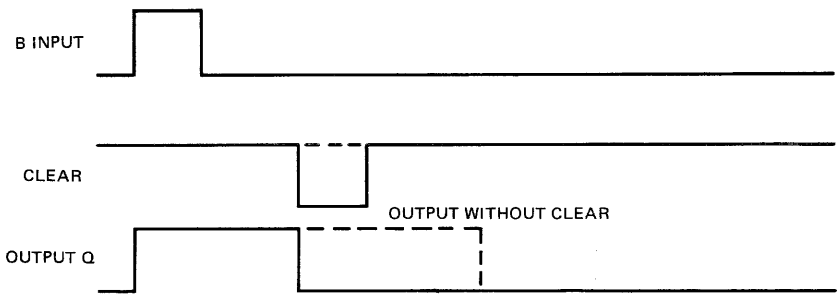
description

These monolithic TTL retriggerable monostable multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs at the low logic level, and in the high-level state, a fan-out of 20 is available. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

Figure A below illustrates triggering the one-shot with the high-level-active (B) inputs.



OUTPUT PULSE CONTROL USING RETRIGGER PULSE



OUTPUT PULSE CONTROL USING CLEAR INPUT

FIGURE A—TYPICAL INPUT/OUTPUT PULSES

NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

description (continued)

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. SN54122/SN74122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with SN54121/SN74121.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = 0.32\ R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

R_T is in kΩ (either internal or external timing resistor)
C_{ext} is in pF
t_w is in ns

For pulse widths when $C_{ext} \leqslant 1000$ pF, see Figure 3.

These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per one shot is 115 milliwatts; typical average propagation delay time to the Q output is 21 nanoseconds. The SN54122 and SN54123 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74122 and SN74123 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage, SN54122, SN74122 Circuits only (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54122, SN54123 Circuits . . . . . −55°C to 125°C
SN74122, SN74123 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54122, SN54123			SN74122, SN74123			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input data setup time, t_{setup} (see Note 3 and Figure 116)		40†			40†			ns
Input data hold time, t_{hold} (see Note 4 and Figure 116)		40†			40†			ns
Width of clear pulse, $t_{w(clear)}$		40†			40†			ns
External timing resistance		5		25	5		50	kΩ
External capacitance		No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal				50			50	pF
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

†These conditions are recommended for use at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the SN54122/SN74122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, See Note 5	I_{OH} = −800 μA,	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, See Note 5	I_{OL} = 16 mA,		0.22	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4 V			40	μA
		clear input					80	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		clear input					−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	See Note 5	−10		−40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 6 and 7	SN54122, SN74122		23	28	mA
				SN54123, SN74123		46	66	

†For conditions shown as MIN or MAX, use the value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of SN54122/SN74122 is open.
7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of SN54122/SN74122 is open.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either A input	C_{ext} = 0, C_L = 15 pF, See Figure 116	R_{ext} = 5 kΩ, R_L = 400 Ω,		22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either B input				19	28	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either A input				30	40	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either B input				27	36	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output, from clear input				18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output, from clear input				30	40	ns
$t_{w(min)}$	Minimum width of Q output pulse				45	65	ns
t_w	Width of Q output pulse	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 400 Ω	3.08	3.42	3.76	μs

TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

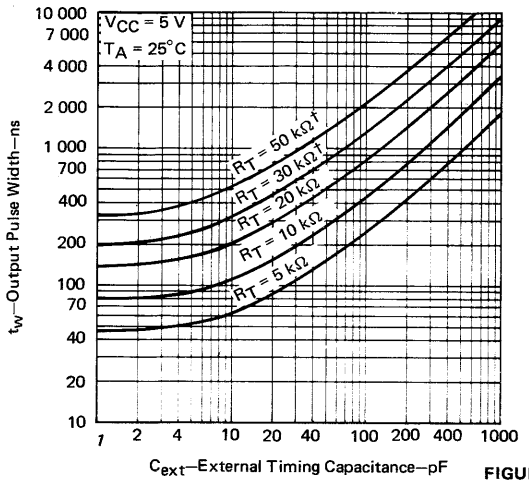
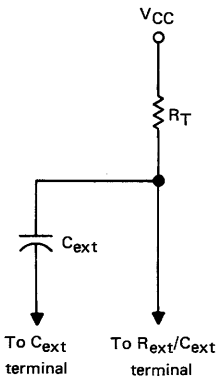


FIGURE B

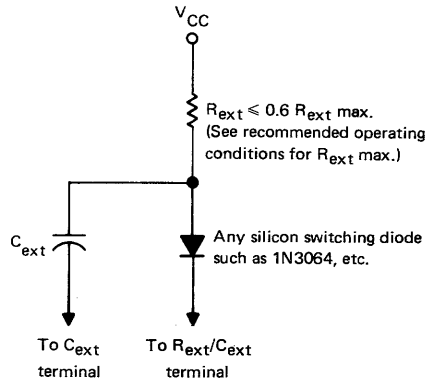
†These values of resistance exceed the maximums recommended for use over the full temperature range of the SN54122 and SN54123.

TYPICAL APPLICATION DATA



TIMING COMPONENT CONNECTIONS WHEN $C_{ext} \leq$ 1000 pF

FIGURE C



TIMING COMPONENT CONNECTIONS WHEN C_{ext} > 1000 pF AND CLEAR IS USED

FIGURE D

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure D be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

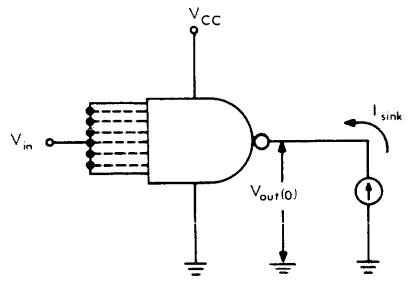
$$t_w = 0.28\ R_{ext}C_{ext}\left(1 + \frac{0.7}{R_{ext}}\right)$$

where

R_{ext} is in kΩ
C_{ext} is in pF
t_w is in ns

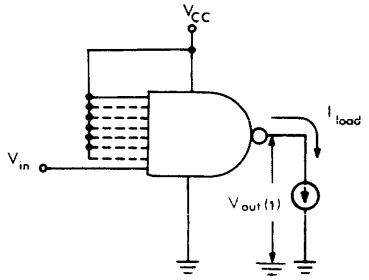
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



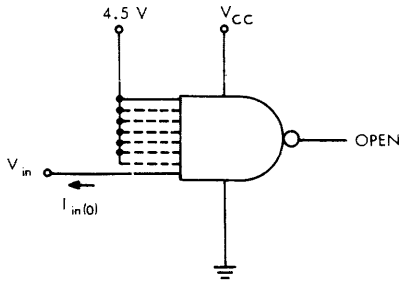
1. All inputs are tested simultaneously.

FIGURE 1



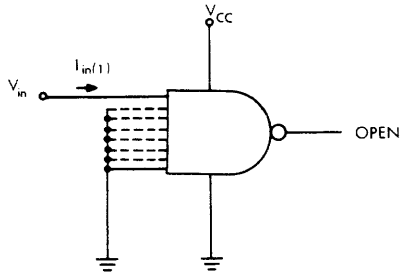
1. Each input is tested separately.

FIGURE 2



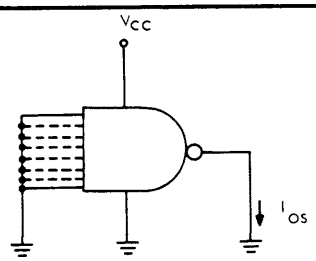
1. Each input is tested separately.

FIGURE 3



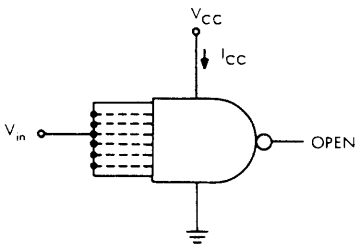
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



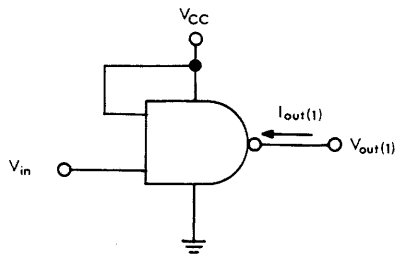
1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

FIGURE 6

§ Arrows indicate actual direction of current flow.

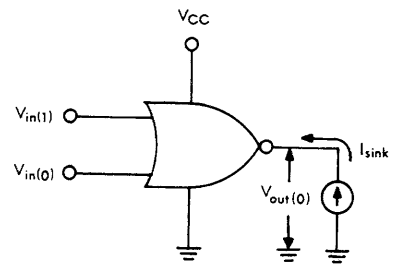
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



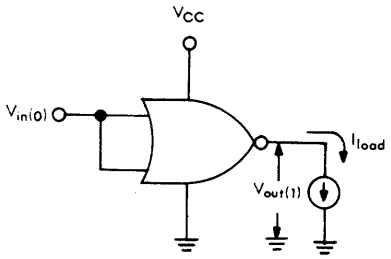
1. Each input is tested separately.

FIGURE 7



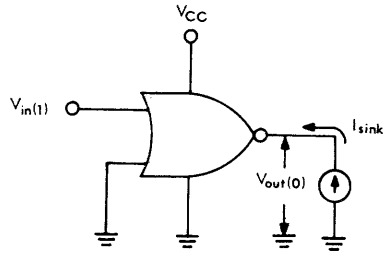
1. Each input is tested separately.

FIGURE 8



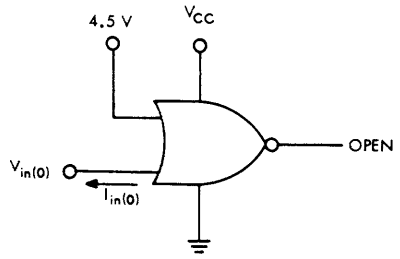
1. Both inputs are tested simultaneously.

FIGURE 9



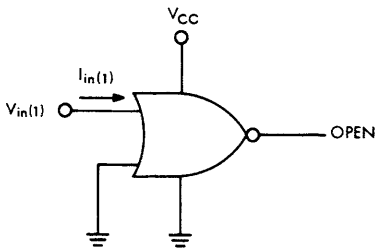
1. Each input is tested separately.

FIGURE 10



1. Each input is tested separately.

FIGURE 11



1. Each input is tested separately.

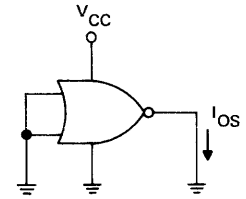
FIGURE 12

§Arrows indicate actual direction of current flow.

6

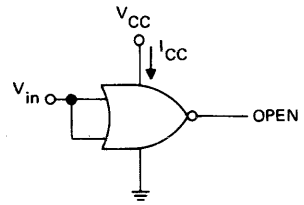
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each gate is tested separately.

FIGURE 13



1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

FIGURE 14

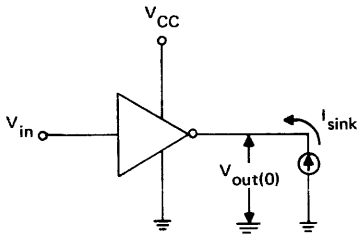


FIGURE 15

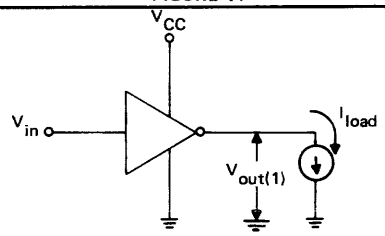


FIGURE 16

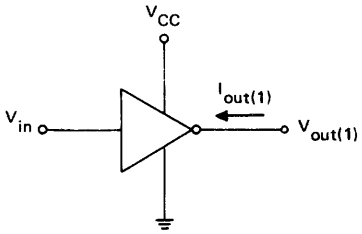


FIGURE 17

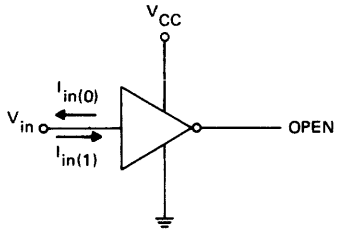
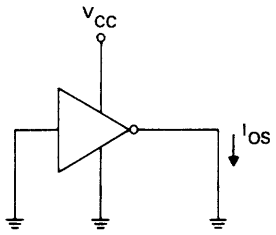
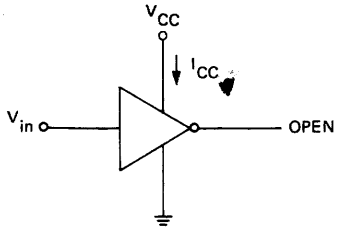


FIGURE 18



1. Each inverter is tested separately.

FIGURE 19



1. All inverters are tested simultaneously.

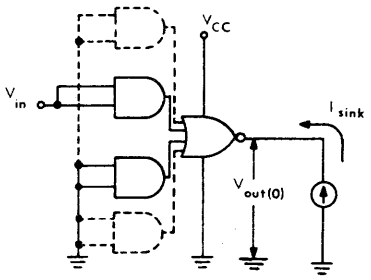
FIGURE 20

§ Arrows indicate actual direction of current flow

6

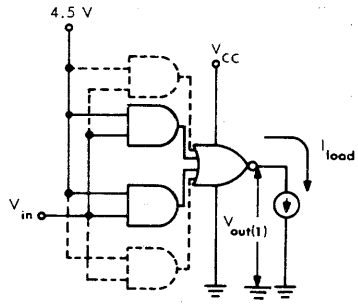
PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)



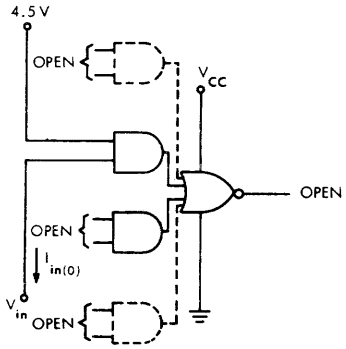
1. Each AND section is tested separately.

FIGURE 21



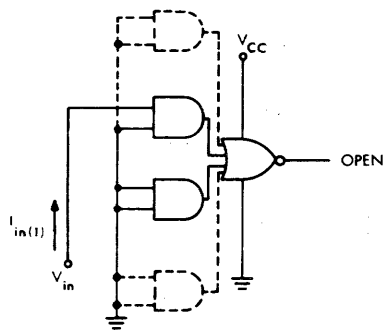
1. Each pair of inputs is tested separately.

FIGURE 22



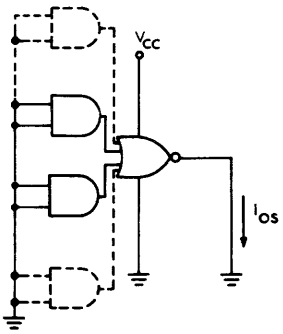
1. Each input is tested separately.

FIGURE 23



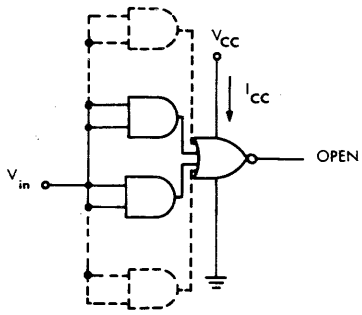
1. Each input is tested separately.

FIGURE 24



1. Each gate is tested separately.

FIGURE 25



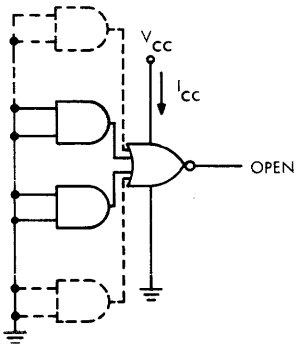
1. All gates are tested simultaneously.

FIGURE 26

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)



1. All gates are tested simultaneously.

FIGURE 27

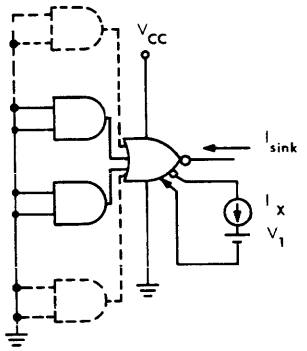


FIGURE 28

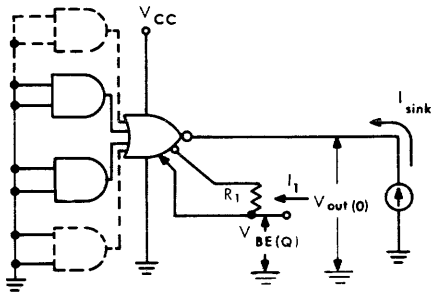


FIGURE 29

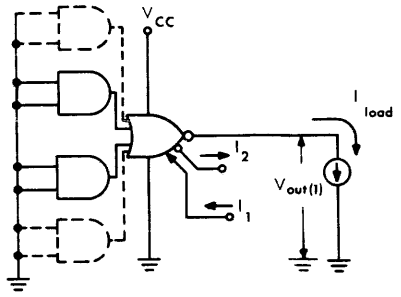
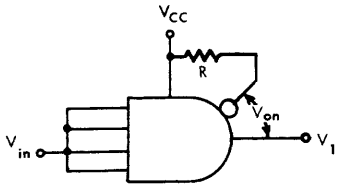
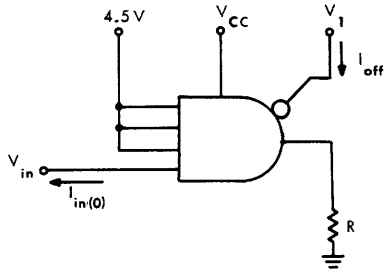


FIGURE 30



1. All inputs are tested simultaneously.

FIGURE 31



1. Each input is tested separately.

FIGURE 32

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

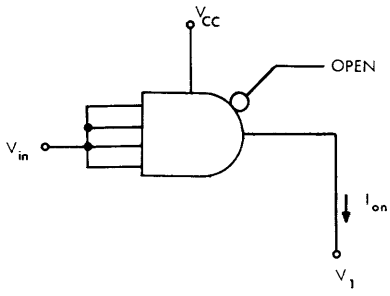
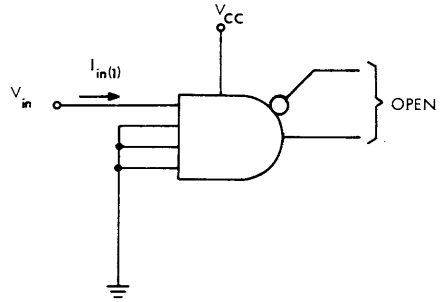
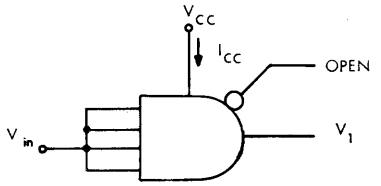


FIGURE 33



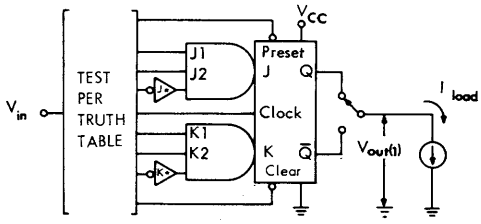
1. Each input is tested separately.

FIGURE 34



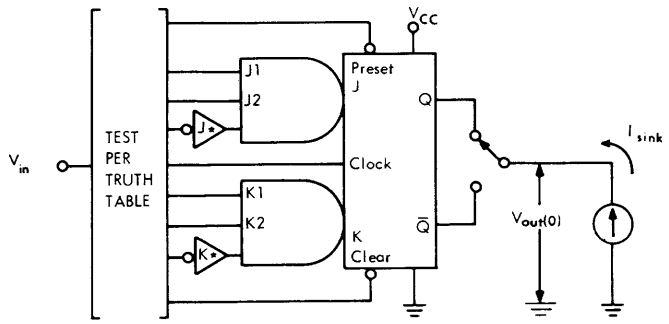
1. "On" and "off" conditions are tested separately.
2. All gates are tested simultaneously.

FIGURE 35



1. Each output is tested separately.
2. Preset and clear are tested with $V_{in(clock)} = 0$.

FIGURE 36



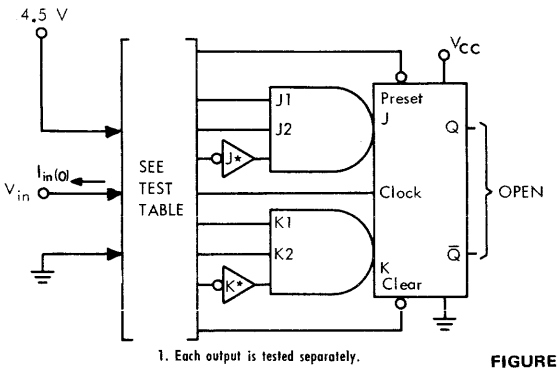
1. Each output is tested separately.

FIGURE 37

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

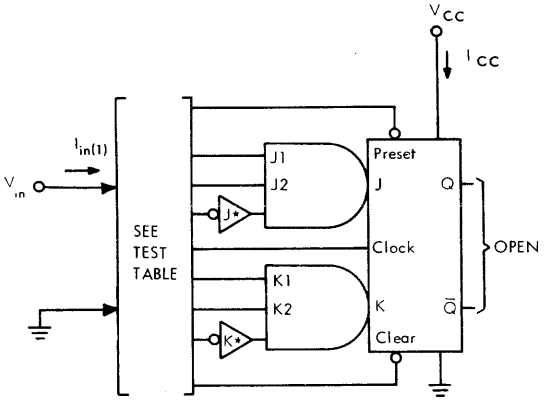
d-c test circuits § (continued)



1. Each output is tested separately.

TEST TABLE			
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Ground	Apply Momentary GND, then 4.5 V
J2	J1	J★	Clear
J1	J2	J★	Clear
J★	None	None	None
K2	K1	K★	Preset
K1	K2	K★	Preset
K★	None	None	None
Clock	None	None	None
Preset	K1 and K2	K★	None
Clear	J1 and J2	J★	None

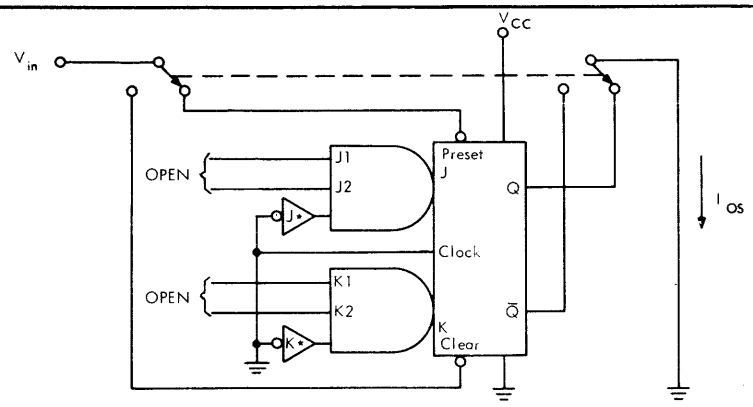
FIGURE 38



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply 4.5 V
J2	J1 and Clear	J★
J1	J2 and Clear	J★
J★	None	None
K2	K1 and Preset	K★
K1	K2 and Preset	K★
K★	None	None
Clock	None	None
Preset	K1 and K2	K★
Clear	J1 and J2	J★

1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

FIGURE 39



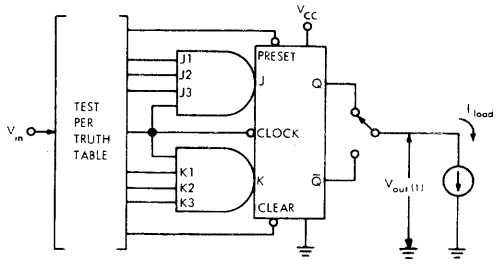
1. Each output is tested separately.

FIGURE 40

§ Arrows indicate actual direction of current flow.

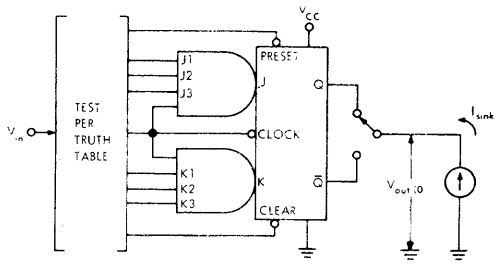
PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)



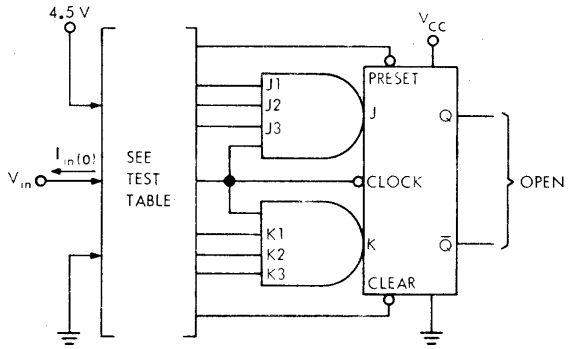
1. Each output is tested separately.

FIGURE 41



1. Each output is tested separately.

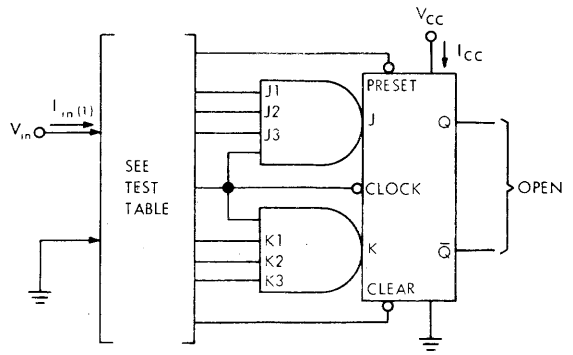
FIGURE 42



1. Each input is tested separately.

TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

FIGURE 43



1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

FIGURE 44

§Arrows indicate actual direction of current flow.

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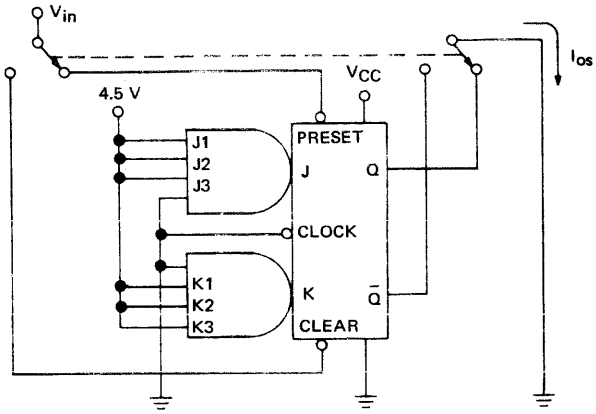
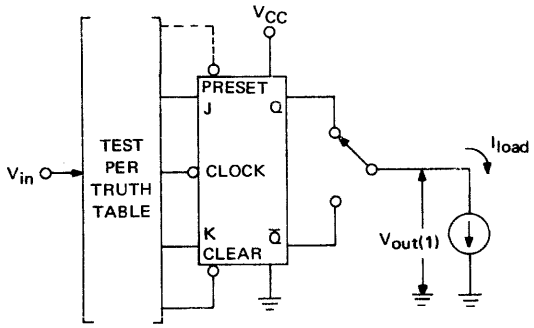
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



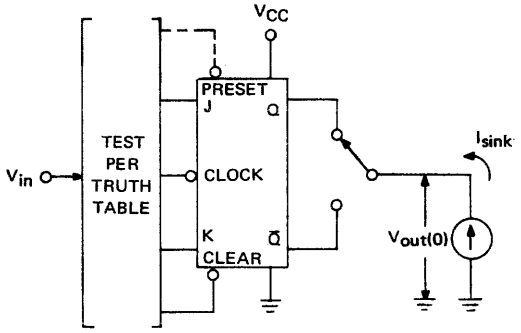
1. Each output is tested separately.

FIGURE 45



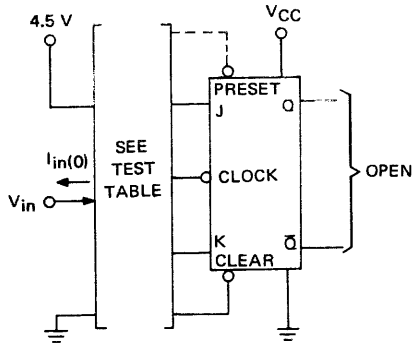
1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 46



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 47



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\bar{Q}$ (See Note 3)	Clock and Clear

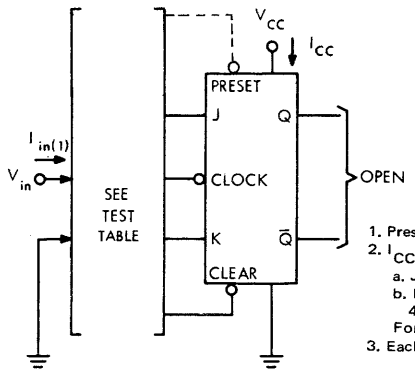
1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3 After application of momentary ground, Q and $\bar{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is applicable for SN5476/SN7476 circuits only.

FIGURE 48

§ Arrows indicate actual direction of current flow

PARAMETER MEASUREMENT INFORMATION

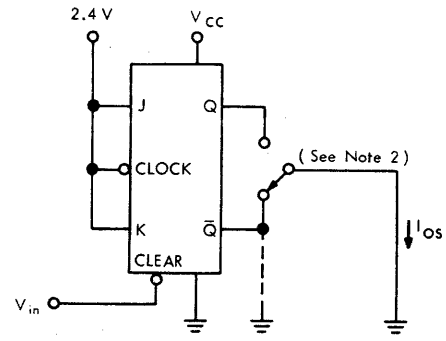
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

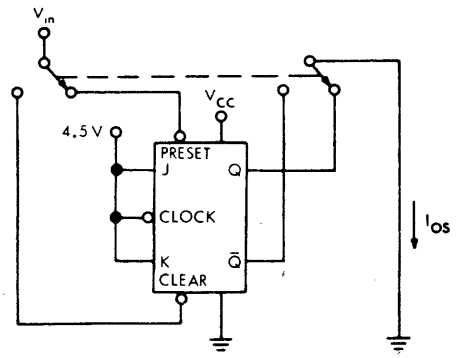
1. Preset is applicable for SN5476/SN7476 circuits only.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = GND. For SN5476/SN7476: Preset = 4.5 V.
   b. For SN5473/SN7473: J = Clear = 4.5 V, K = GND, and apply momentary 4.5 V, then GND to Clock.
   For SN5476/SN7476: J = K = Clock = Preset = GND, and Clear = 4.5 V.
3. Each flip-flop is tested separately for $I_{in(1)}$.

FIGURE 49



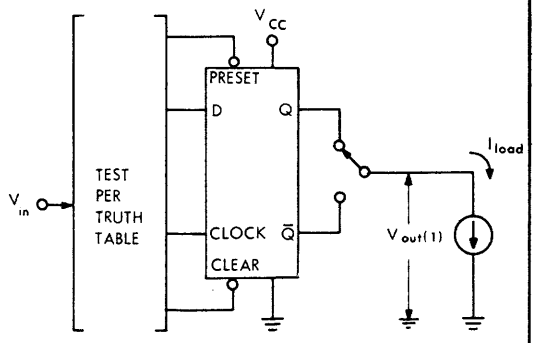
1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\bar{Q}$. When testing Q, apply 2.4 V to Clear, ground $\bar{Q}$, and limit duration of test to 100 ms.

FIGURE 50



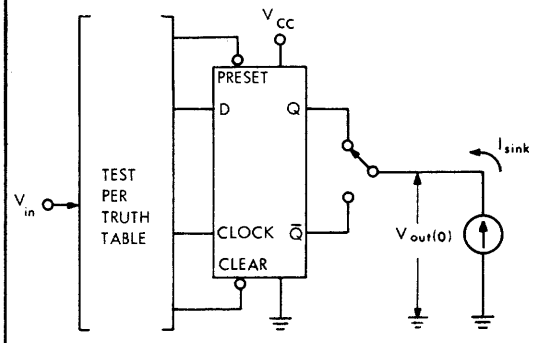
1. Each flip-flop is tested separately.

FIGURE 51



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 52



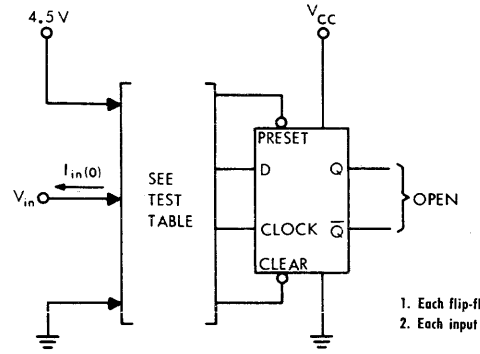
1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 53

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

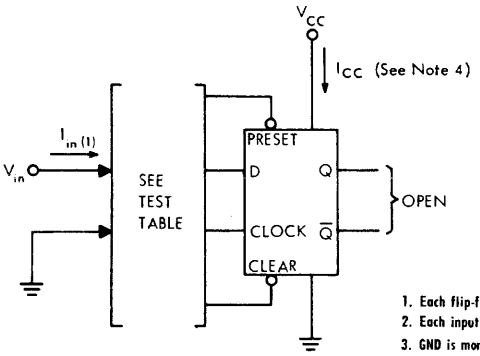


TEST TABLE

APPLY V_{in} (TEST $I_{in(0)}$)	APPLY 4.5 V	APPLY GND
Clock	Clear	Preset and D
Preset	Clear	Clock and D
Clear	Clock, D, and Preset	None
D	Clear and Clock	Preset

1. Each flip-flop is tested separately.
2. Each input is tested separately.

FIGURE 54

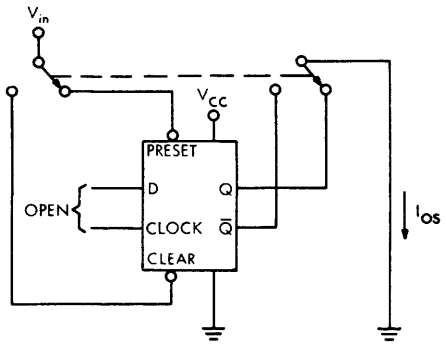


TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	APPLY 4.5 V	APPLY GND
Clock	Clear and D	Preset
Clock	Preset and D	Clear
Preset	Clear and D	Clock (See Note B)
Clear	Preset	Clock, D, and Q
Clear	Preset	D and Clock (See Note B)
D	Preset and Clock	Clear

1. Each flip-flop is tested separately.
2. Each input is tested separately.
3. GND is momentarily applied to clock, then 4.5 V.
4. I_{CC} is measured with D, clock, and preset at GND, then with D, clock, and clear at GND.

FIGURE 55



1. Each output is tested separately.

FIGURE 56

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

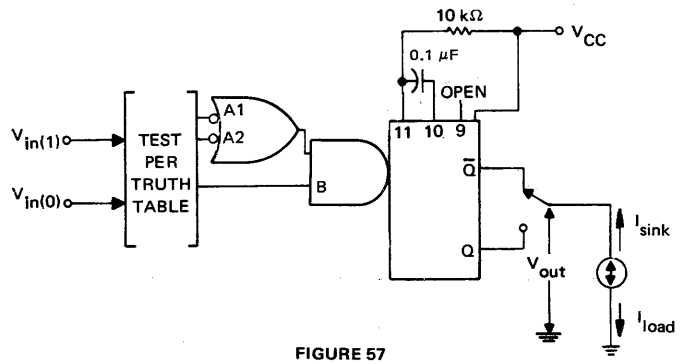
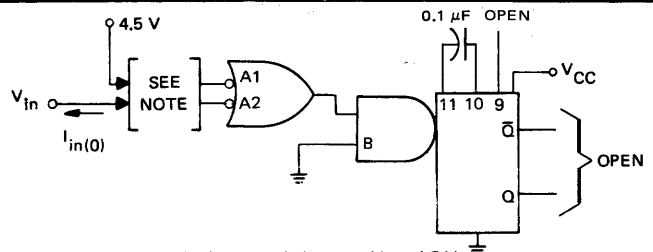


FIGURE 57



1. Each input is tested separately. Input not being tested is at 4.5 V.

FIGURE 58

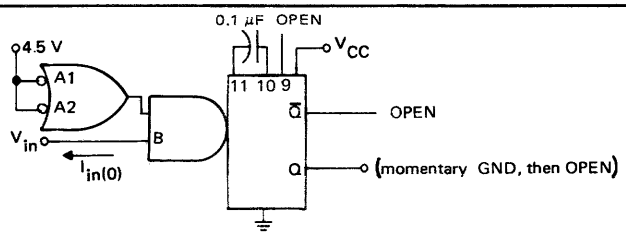
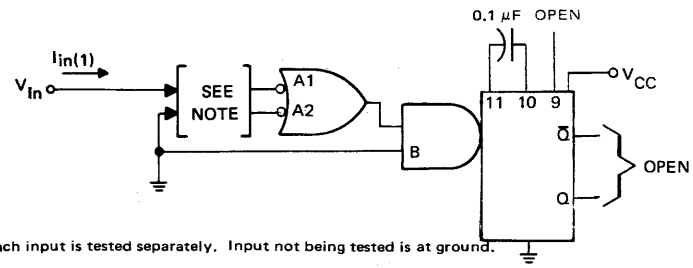


FIGURE 59



1. Each input is tested separately. Input not being tested is at ground.

FIGURE 60

§ Arrows indicate actual direction of current flow.

6

d-c test circuits § (continued) PARAMETER MEASUREMENT INFORMATION

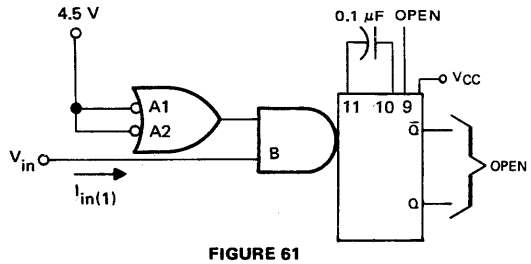
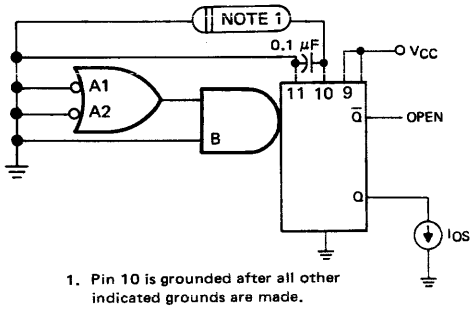


FIGURE 61



1. Pin 10 is grounded after all other indicated grounds are made.

FIGURE 62

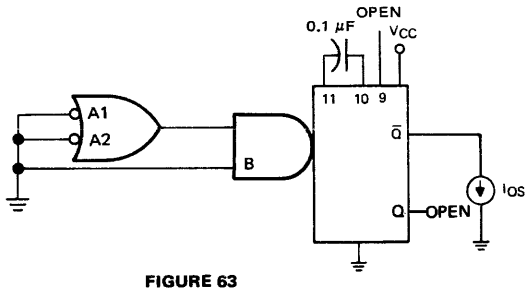
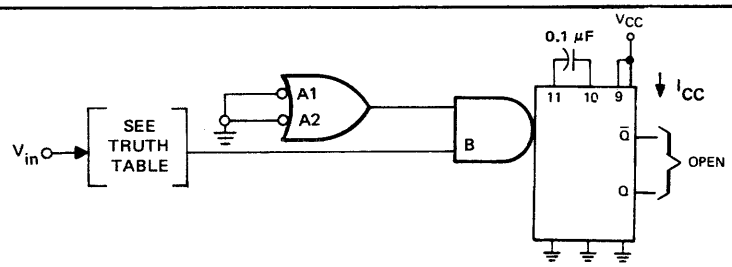


FIGURE 63



1. Quiescent and fired conditions are tested.

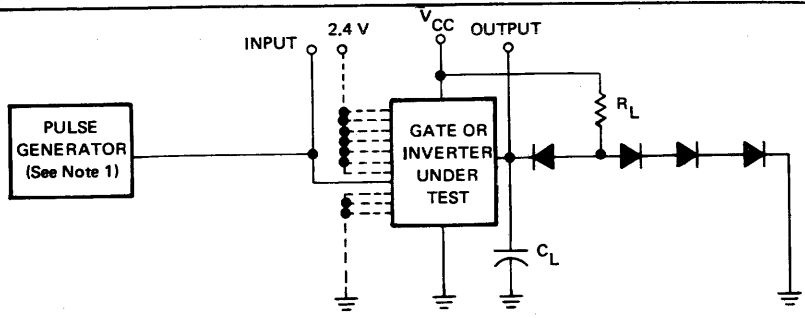
FIGURE 64

§ Arrows indicate actual direction of current flow.

6

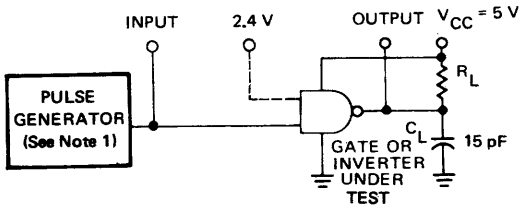
PARAMETER MEASUREMENT INFORMATION

switching characteristics

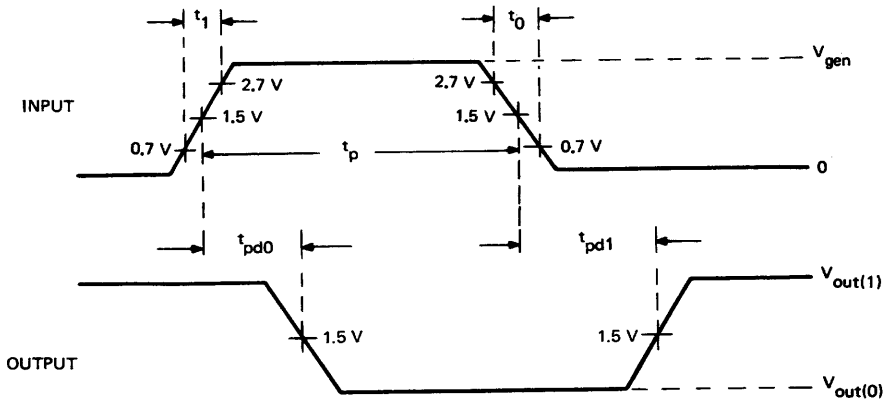


(See Note 5)

TEST CIRCUIT FOR SN5400, SN5402, SN5404, SN5410, SN5420, SN5430, SN5440, SN5450, SN5451, SN5453, SN5454, SN7400, SN7402, SN7404, SN7410, SN7420, SN7430, SN7440, SN7450, SN7451, SN7453, AND SN7454



TEST CIRCUIT FOR SN5401, SN5403, SN5405, SN7401, SN7403, SN7405



VOLTAGE WAVEFORMS

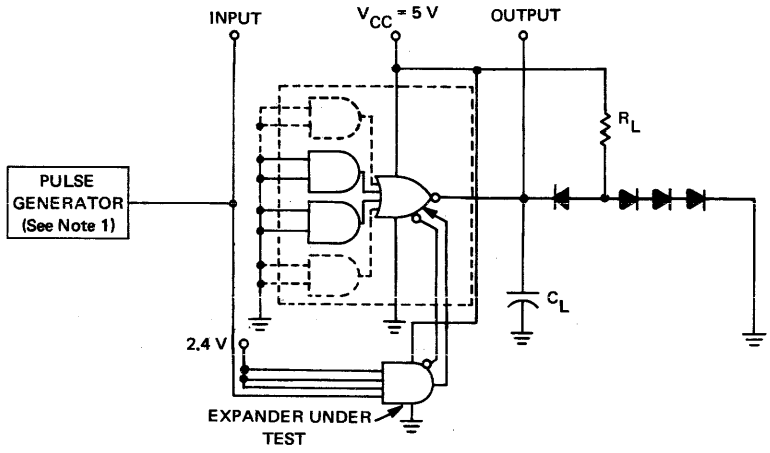
NOTES: 1. The generator has the following charactertistic: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.
5. When testing the SN5400/SN7400 through SN5440/SN7440 (except SN5402/SN7402) connect all unused inputs to 2.4 V. When testing the SN5402/SN7402 or SN5450/SN7450 through SN5454/SN7454, apply the input pulse to one input of one AND section and 2.4 V to all unused inputs of that AND section. All inputs of unused AND sections are grounded.

FIGURE 65-GATE PROPAGATION DELAY TIMES

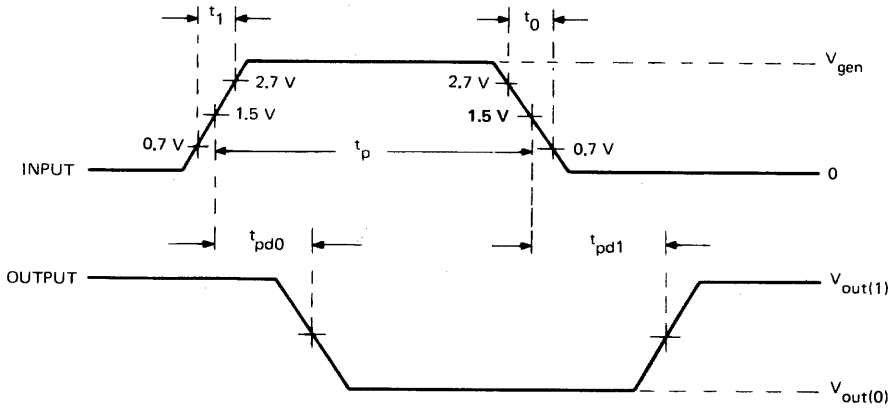
6

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



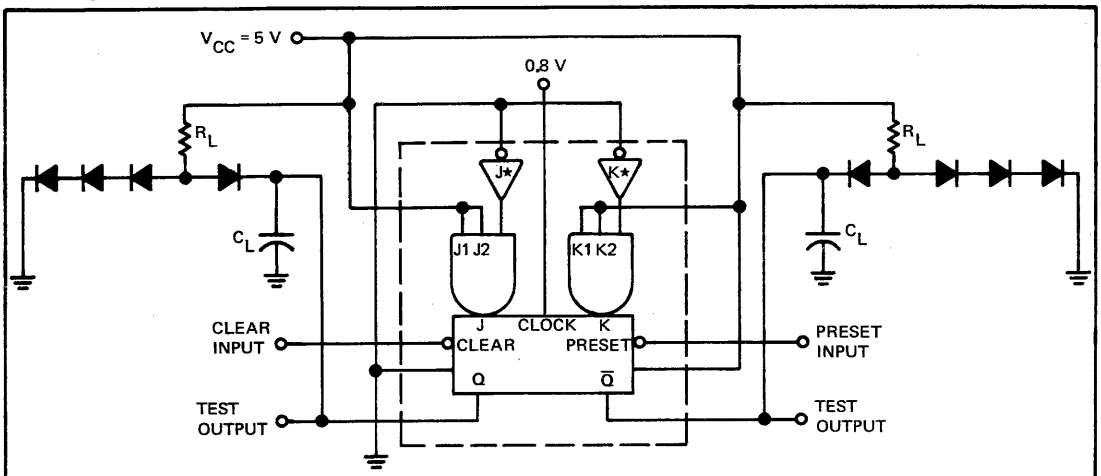
VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.

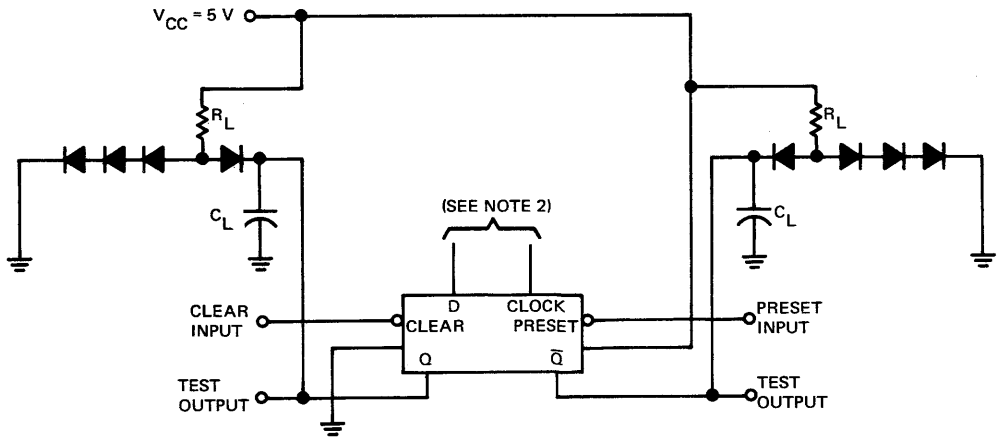
FIGURE 66–EXPANDER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



SN5470/SN7470 TEST CIRCUIT



SN5474/SN7474 TEST CIRCUIT

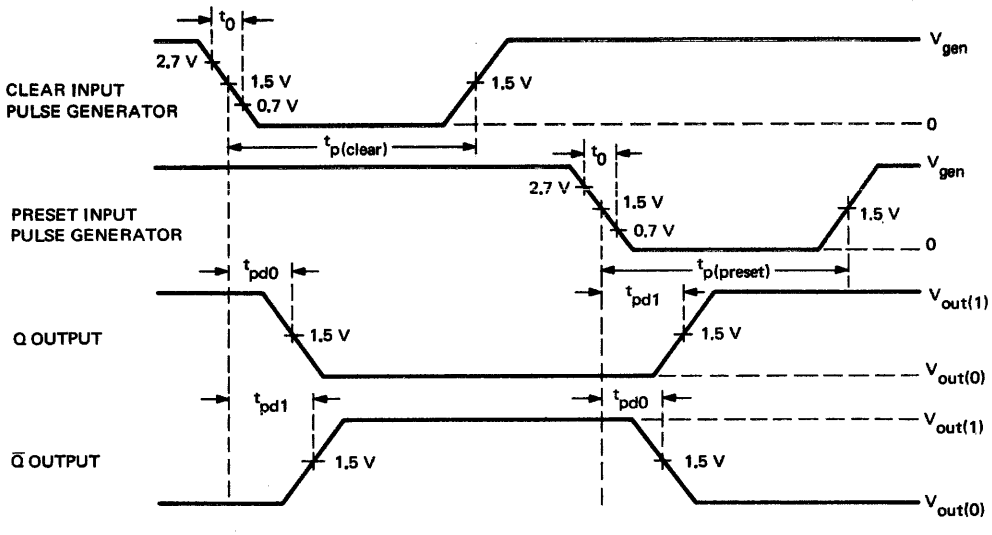
NOTES: 1. Preset or clear function of the SN5470/SN7470 can occur only when clock input is low. Gated inputs are inhibited.
2. Clear and preset inputs of the SN5474/SN7474 dominate regardless of the state of clock or D inputs.
3. All diodes are 1N3064.
4. C_L includes probe and jig capacitance.

FIGURE 67–SN5470/SN7470 AND SN5474/SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 1 OF 2)

6

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



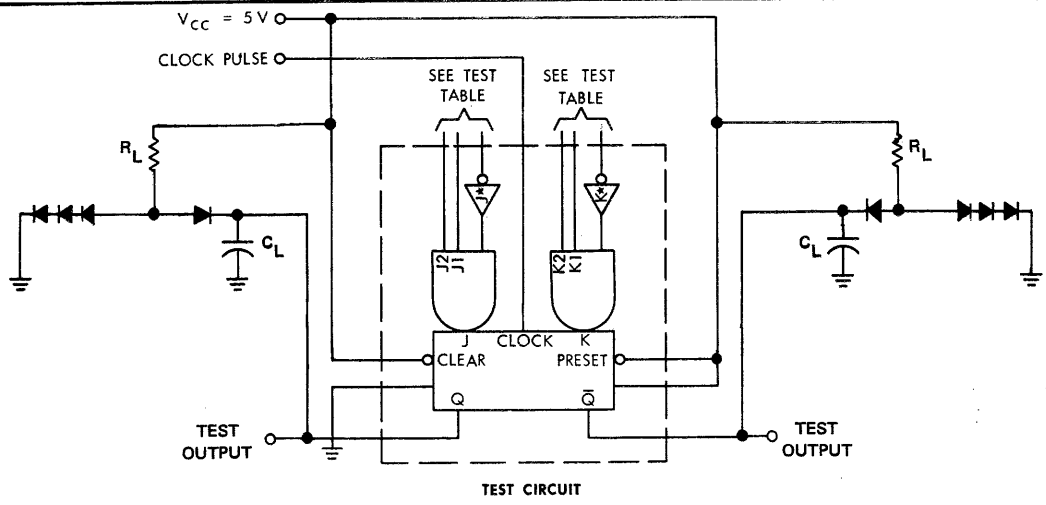
VOLTAGE WAVEFORMS

NOTE 6: Clear or preset input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_p = 25 ns for the SN5470/SN7470, and t_p = 30 ns for SN5474/SN7474.

FIGURE 67—SN5470/SN7470 AND SN5474/SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 2 OF 2)

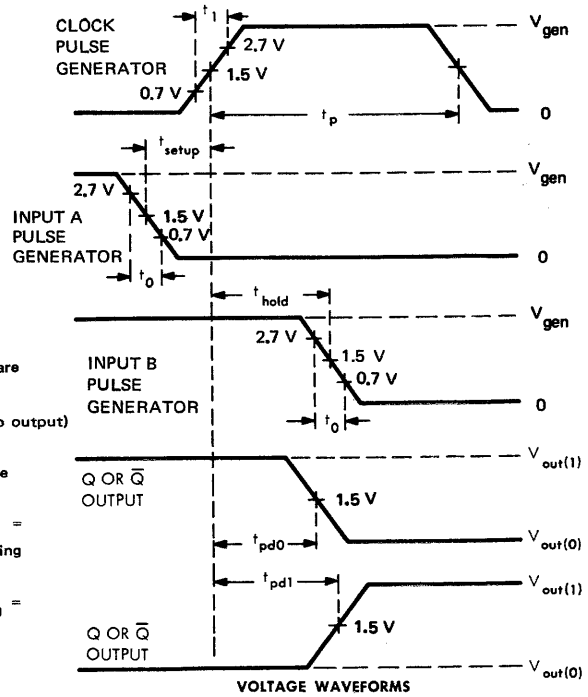
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT

TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	APPLY 2.4 V	GND
1	t_{setup} at J★	J★	None	J1, J2, K1, K2	K★
2	t_{hold} at J1, J2	None	J1, J2	K1, K2	J★ and K★
3	t_{setup} at K★	K★	None	J1, J2, K1, K2	J★
4	t_{hold} at K1, K2	None	K1, K2	J1, J2	J★ and K★



VOLTAGE WAVEFORMS

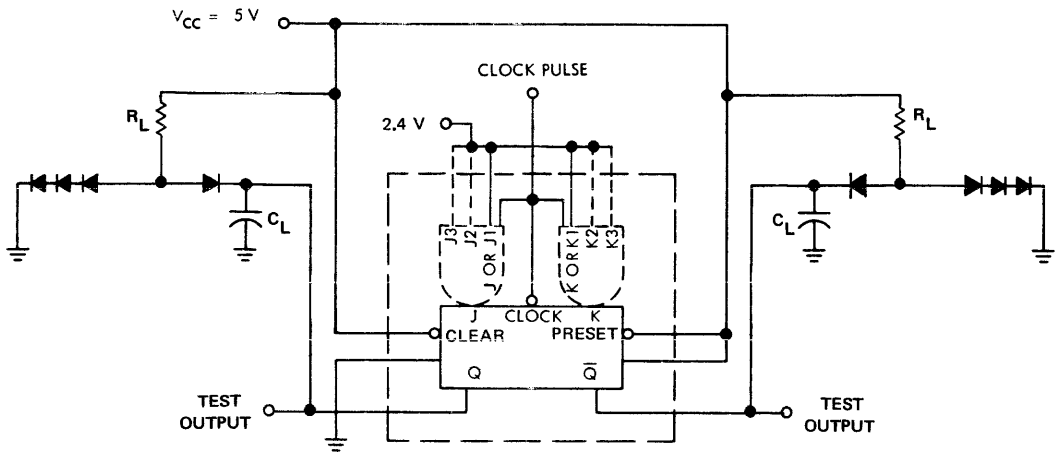
NOTES: 1. Clock pulse (see note 3), input A, and input B are used to measure t_{setup} and t_{hold}.
2. Clock frequency, t_{pd1}, and t_{pd0} (from clock to output) are measured in the toggle mode. Hold J = K = Logical 1 per truth table and apply clock pulse (see note 3).
3. Clock pulse characteristics: V_{gen} = 3.5 V, t_1 = 10 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.
4. Input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns.
5. All diodes are 1N3064.
6. C_L includes probe and jig capacitance.

FIGURE 68–SN5470/SN7470 FLIP-FLOP SWITCHING TIMES

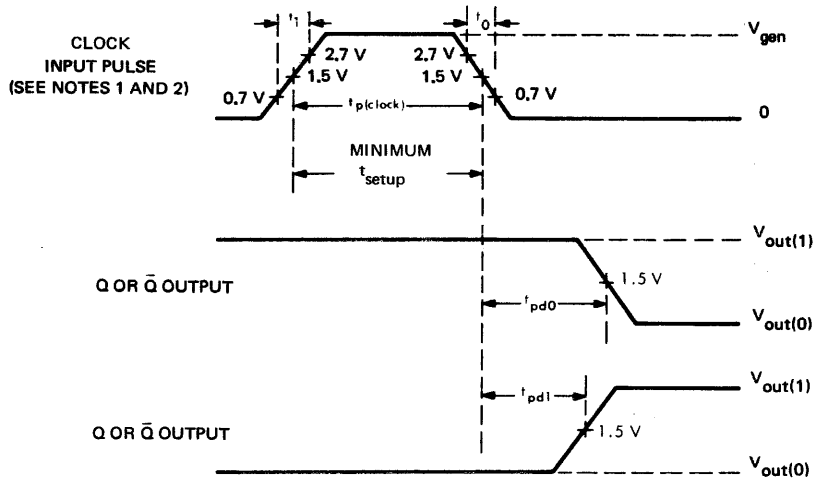
6

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

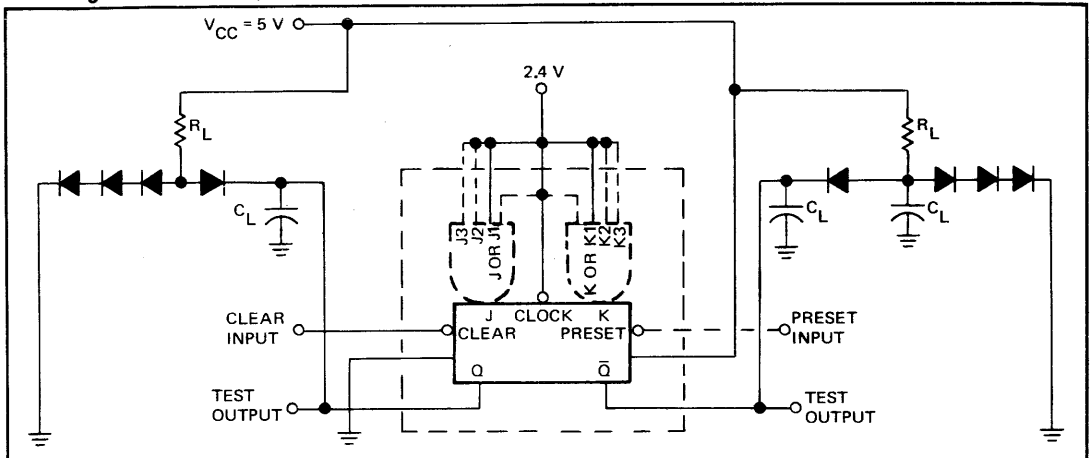
NOTES: 1. Clock, J, and K input pulse characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.

2. For the SN5472/SN7472, J = J1 • J2 • J3; and K = K1 • K2 • K3.
3. Gated inputs (shown with dotted lines) are for the SN5472/SN7472 only. The SN5473/SN7473, SN54107/SN74107 and SN5476/SN7476. Dual Flip-Flops have direct J and K inputs, and preset is not available on the SN5473/SN7473 and SN54107/SN74107.
4. All diodes are 1N3064.
5. C_L includes probe and jig capacitance.

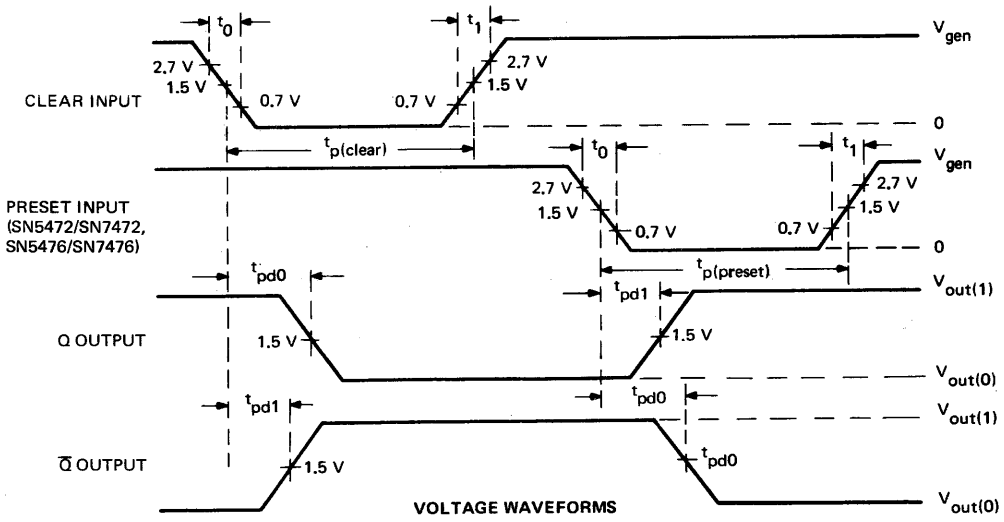
FIGURE 69–SN5472/SN7472, SN5473/SN7473, SN5476/SN7476, SN54107/SN74107 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

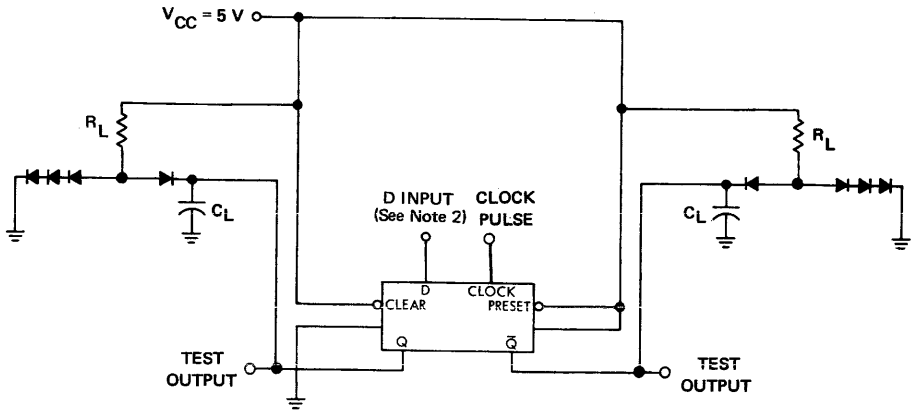
1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: V_{CC} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, $t_{p(clear)} = t_{p(preset)}$ = 25 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
3. Gates inputs (shown with dotted lines) are for the SN5472/SN7472 only. The SN5473/SN7473, SN5476/SN7476, and SN54107/SN74107 Dual Flip-Flops have direct J and K inputs, and preset is not available on the SN5473/SN7473 or SN54107/SN74107.
4. All diodes are 1N3064.
5. C_L includes probe and jig capacitance.

FIGURE 70–SN5472/SN7472, SN5473/SN7473, SN5476/SN7476, SN54107/SN74107 PRESET/CLEAR PROPAGATION DELAY TIMES

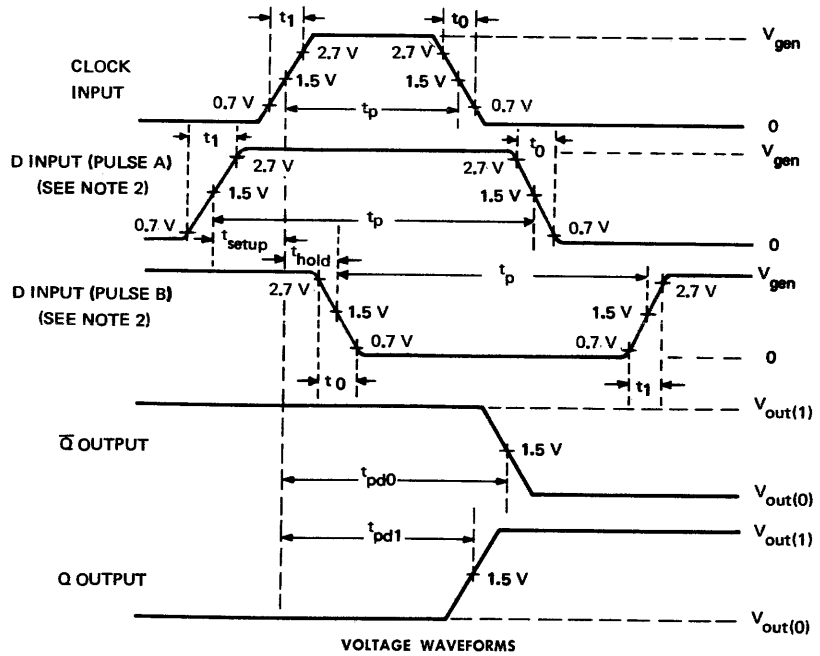
6

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



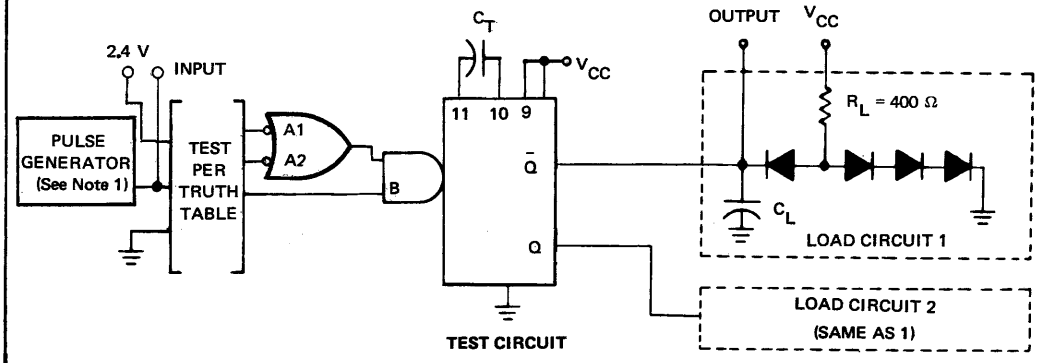
VOLTAGE WAVEFORMS

NOTES:
1. Clock input pulse has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_p = 30 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.
2. D input (pulse A) has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_{setup} = 20 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_{hold} = 5 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064.
4. C_L includes probe and jig capacitance.

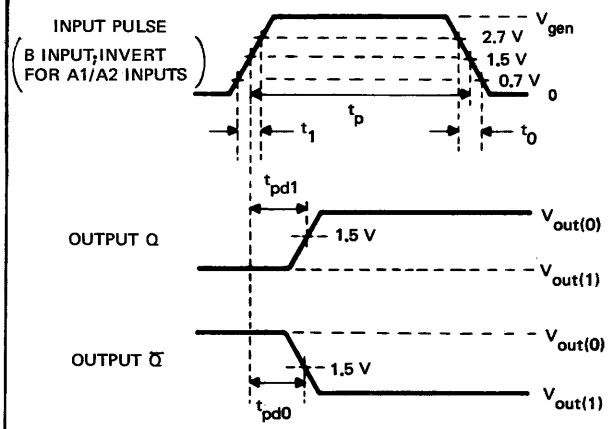
FIGURE 71–SN5474/SN7474 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

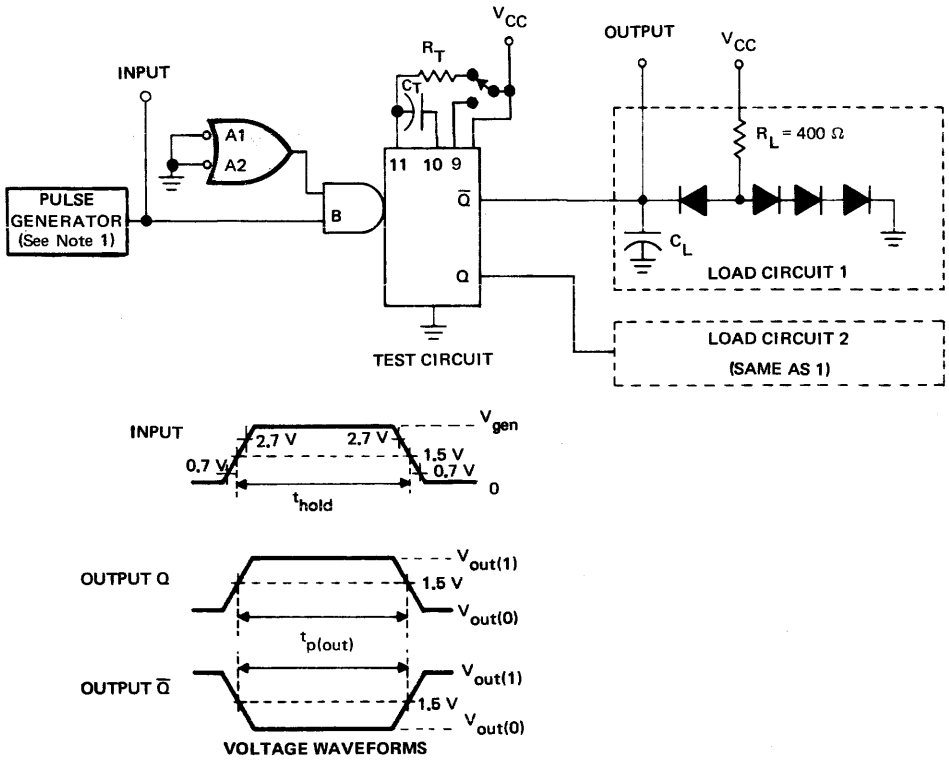
1. The pulse generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, $t_p \geq 50$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.

FIGURE 72–SN54121/SN74121 SWITCHING TIMES

6

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



1. The pulse generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 50 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.

FIGURE 73–$t_{p(out)}$ (internal/minimum), t_{hold}

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§

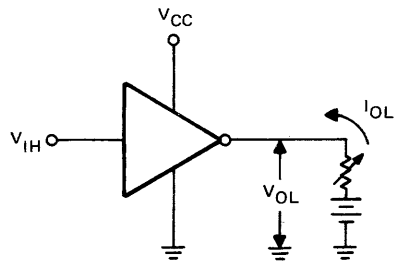


FIGURE 74–V_{IH}, V_{OL}

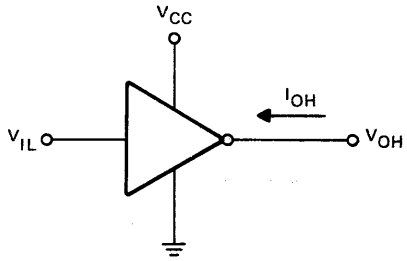


FIGURE 75–V_{IL}, I_{OH}

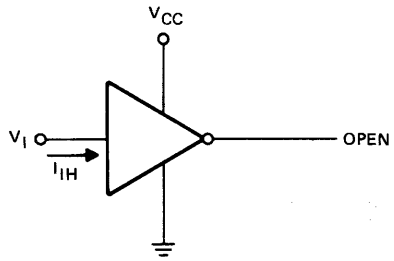


FIGURE 76–I_{IH}

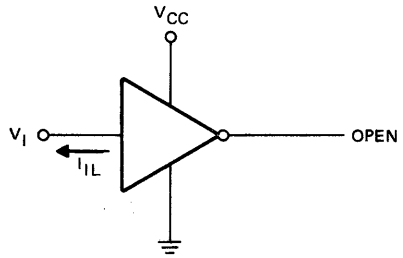
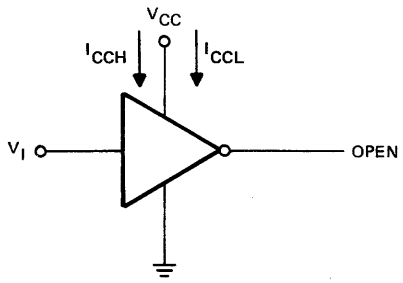


FIGURE 77–I_{IL}



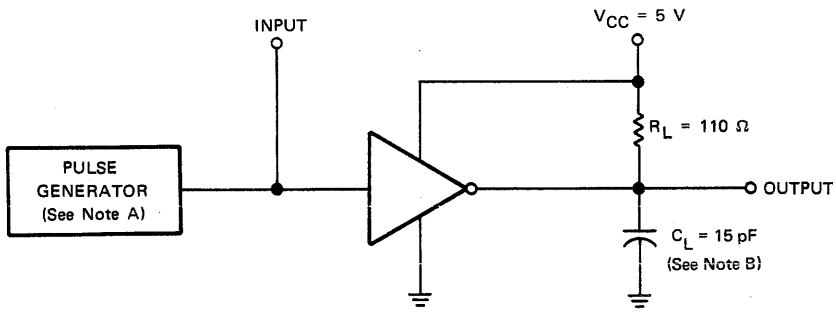
All inverters are tested simultaneously.

FIGURE 78–I_{CCH}, I_{CCL}

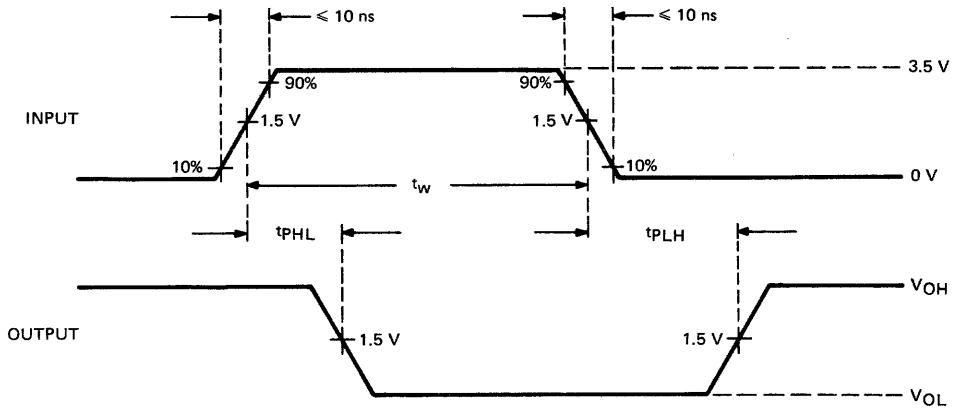
§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 79–PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§

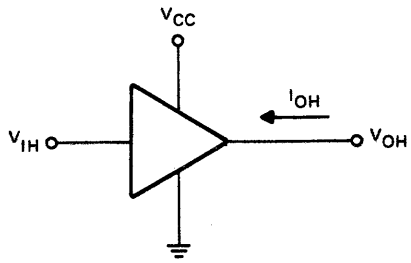


FIGURE 80–V_{IH}, I_{OH}

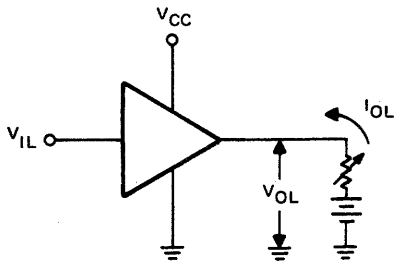


FIGURE 81–V_{IL}, V_{OL}

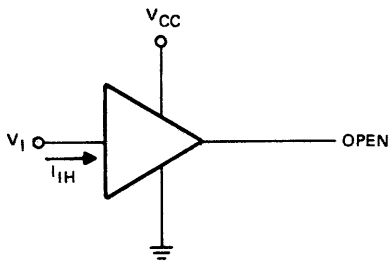


FIGURE 82–I_{IH}

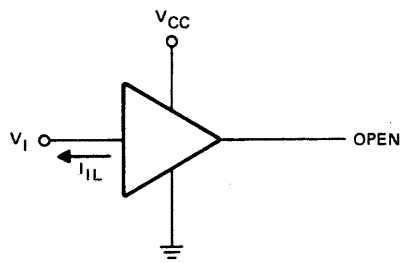
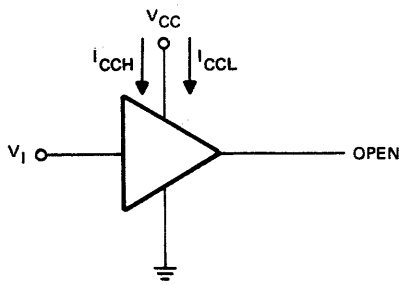


FIGURE 83–I_{IL}



All buffers/drivers are tested simultaneously.

FIGURE 84–I_{CCH}, I_{CCL}

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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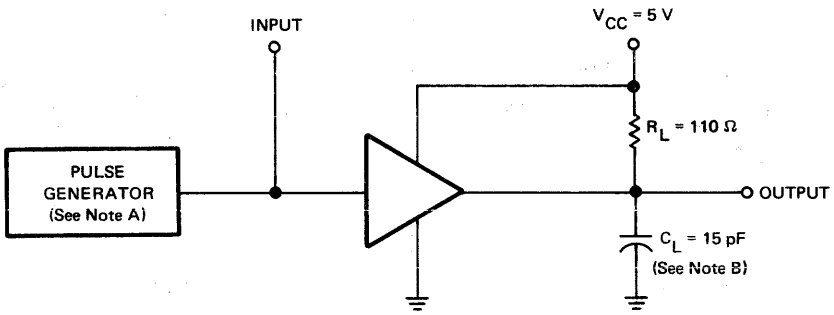
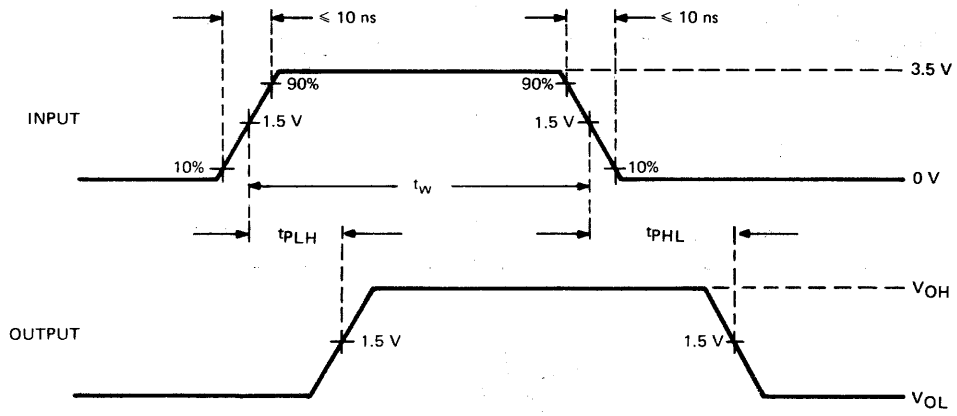
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



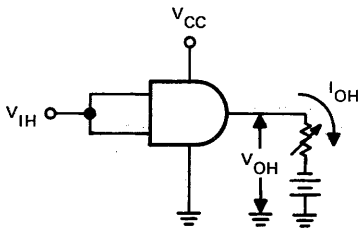
VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 85–PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



Both inputs are tested simultaneously.

FIGURE 86–V_{IH}, V_{OH}

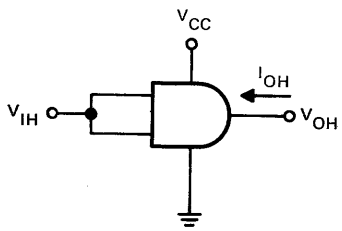
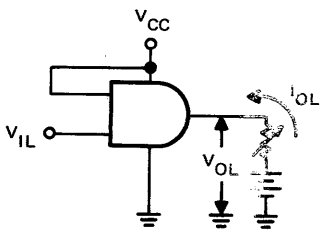
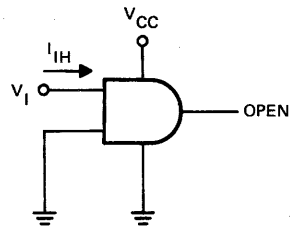


FIGURE 87–V_{IH}, I_{OH}



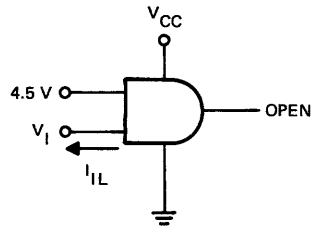
Each input is tested separately.

FIGURE 88–V_{IL}, V_{OL}



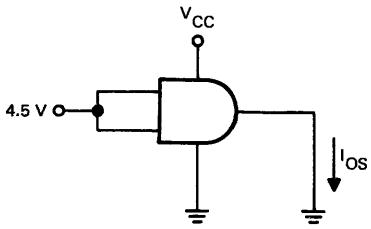
Each input is tested separately.

FIGUER 89–I_{IH}



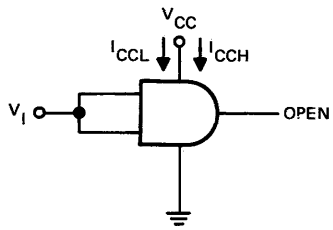
Each input is tested separately.

FIGURE 90–I_{IL}



Each gate is tested separately.

FIGURE 91–I_{OS}



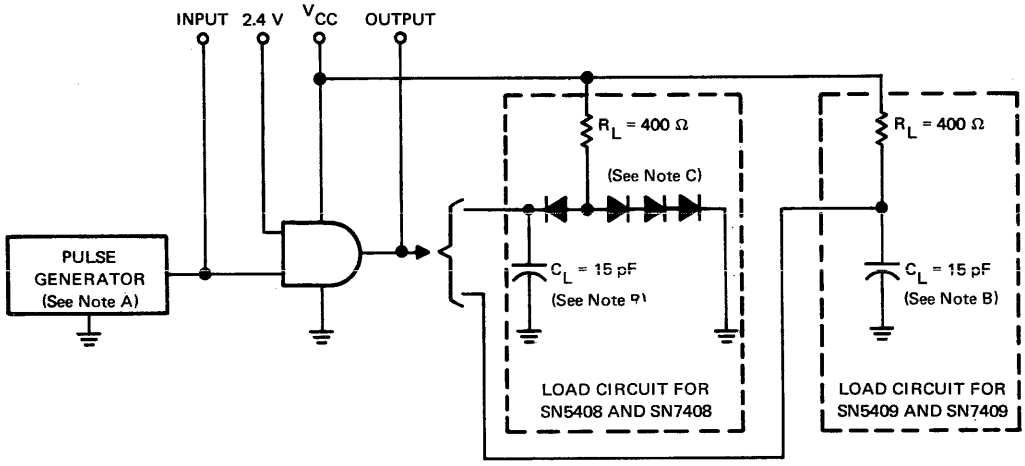
A. High-level and low-level conditions are tested.
B. All gates are tested simultaneously.

FIGURE 92–I_{CCH}, I_{CCL}

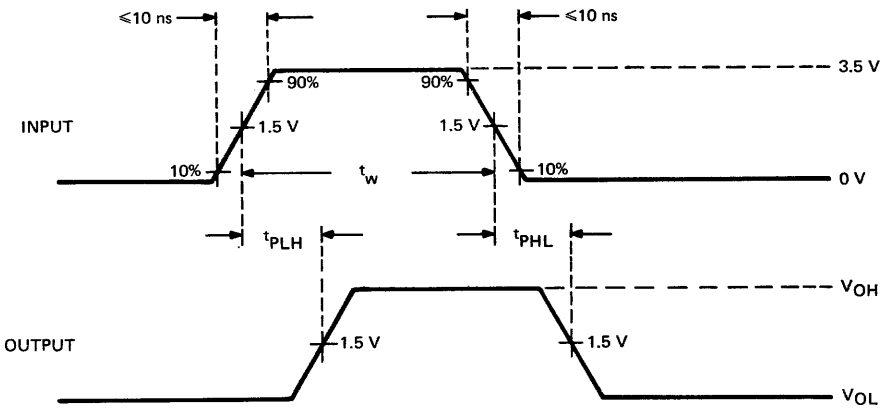
¶ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristic



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 93—PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§

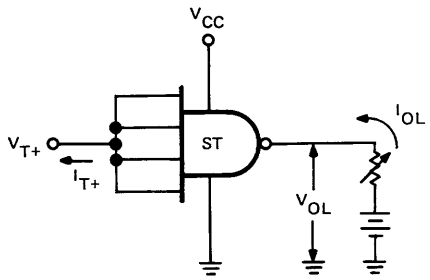


FIGURE 94–V_{T+}, I_{T+}, V_{OL}

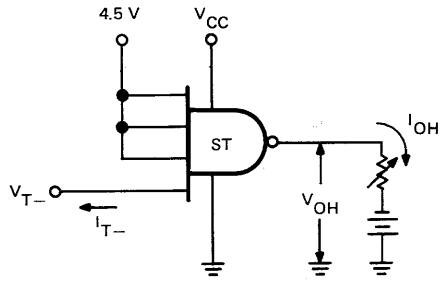
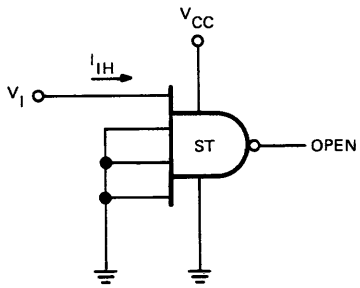
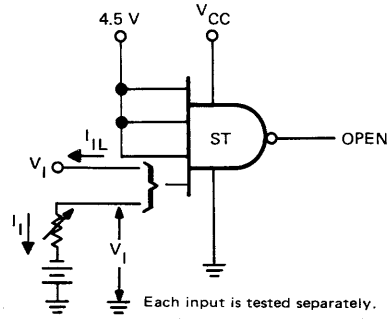


FIGURE 95–V_{T-}, I_{T-}, V_{OH}



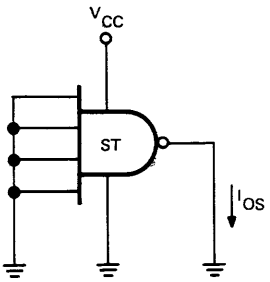
Each input is tested separately.

FIGURE 96–I_{IH}



Each input is tested separately.

FIGURE 97–V_I, I_{IL}



Each gate is tested separately.

FIGURE 98–I_{OS}

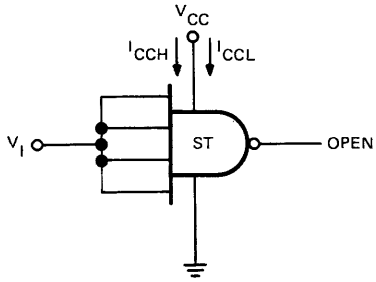


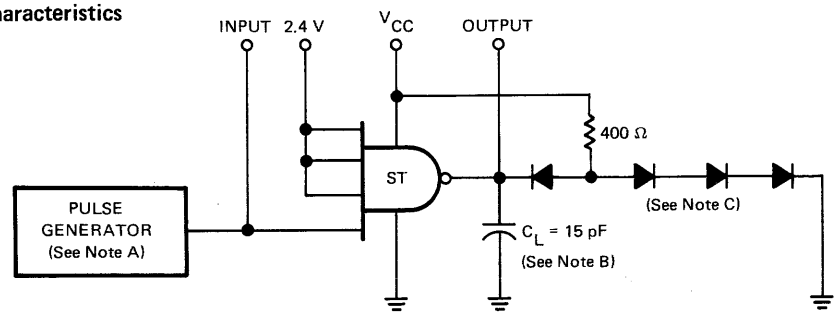
FIGURE 99–I_{CCH}, I_{CCL}

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

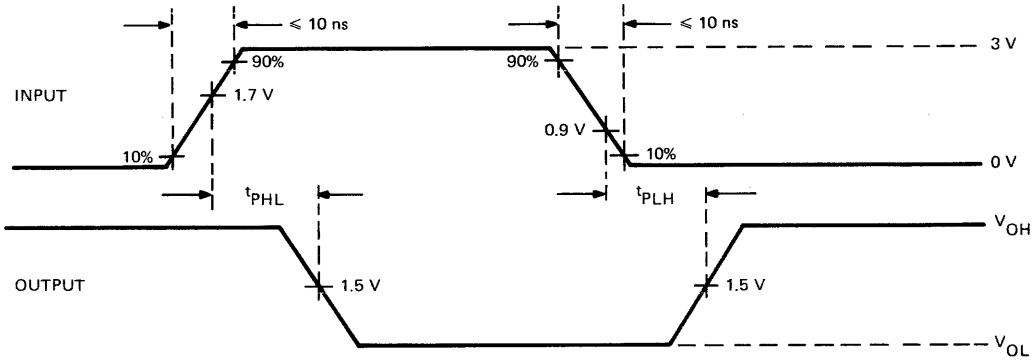
6

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



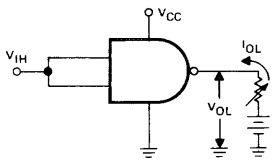
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 100–PROPAGATION DELAY TIMES

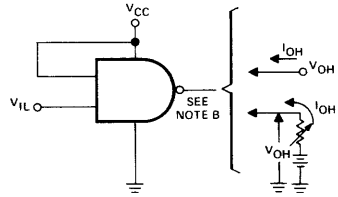
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



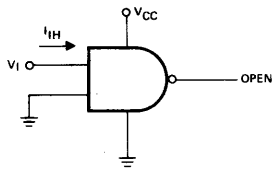
Both inputs are tested simultaneously.

FIGURE 101–V_{IH}, V_{OL}



A. Each input is tested separately.
B. I_{OH} is tested at V_{OH} = 12 V and V_{OH} is tested at I_{OH} = 1 mA.

FIGURE 102–V_{IL}, V_{OH}, I_{OH}



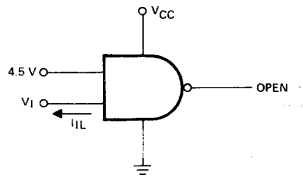
Each input is tested separately.

FIGURE 103–I_{IH}

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

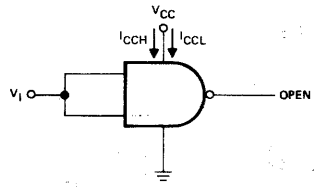
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



Each input is tested separately.

FIGURE 104–I_{IL}

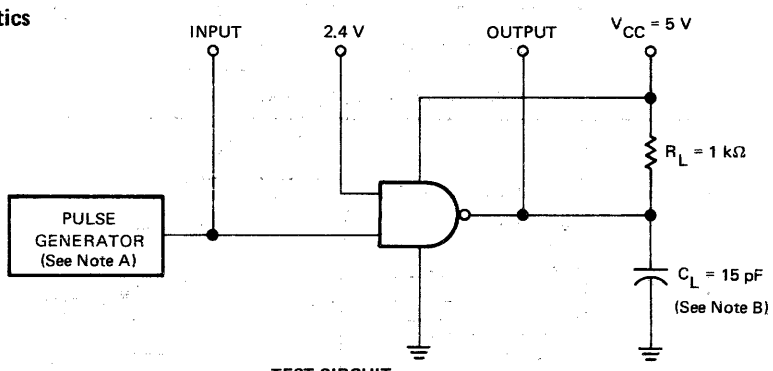


High-level and low-level output conditions are tested.

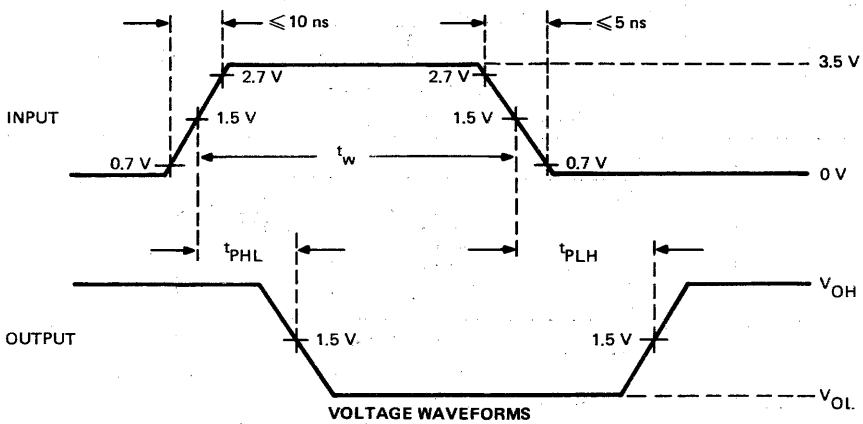
FIGURE 105–I_{CCH}, I_{CCL}

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

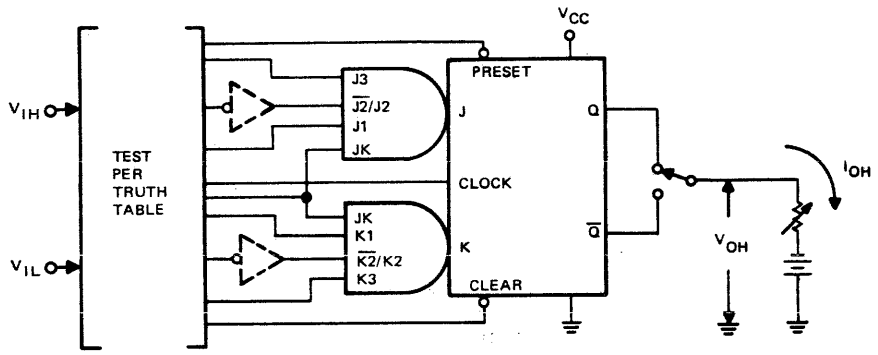
NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 106–PROPAGATION DELAY TIMES

6

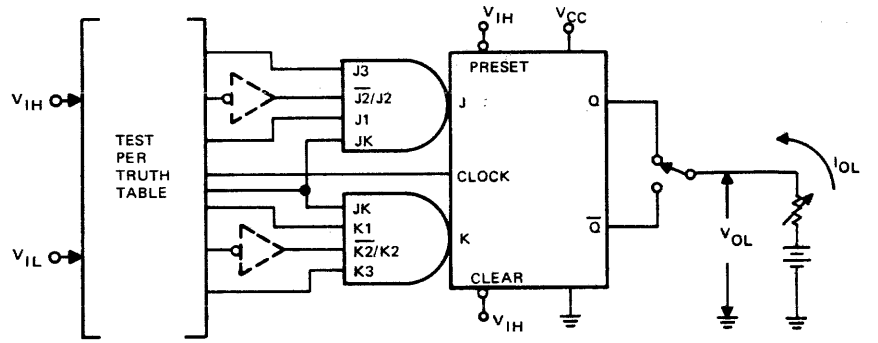
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



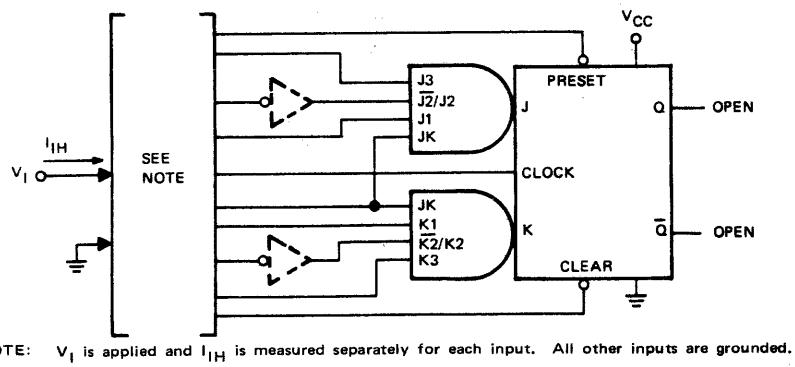
NOTES: A. Each output is tested separately.
B. V_{OH} is also tested using clear and preset inputs.

FIGURE 107 – V_{IH}, V_{IL}, V_{OH}



NOTE: Each output is tested separately.

FIGURE 108 – V_{IH}, V_{IL}, V_{OL}



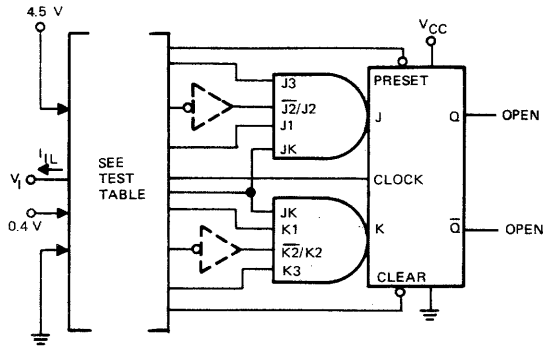
NOTE: V_I is applied and I_{IH} is measured separately for each input. All other inputs are grounded.

FIGURE 109 – I_{IH}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTES: A. Each input is tested separately.
B. V_I is applied and I_{IL} is measured separately for each input.
C. All unspecified inputs are at 4.5 V.

TEST TABLE

APPLY V_I TEST I_{IL}	CONDITIONS ON OTHER INPUTS	
	APPLY 0.4 V	APPLY GND
CLOCK	NONE	NONE
PRESET	CLEAR	CLOCK
CLEAR	PRESET	CLOCK
J1	$\overline{J2}$ (OR 4.5 V TO J2)	CLOCK, CLEAR
$\overline{J2}$ (OR J2)	NONE	CLOCK, CLEAR
J3	$\overline{J2}$ (OR 4.5 V TO J2)	CLOCK, CLEAR
JK	$\overline{J2}$, $\overline{K2}$ (OR 4.5 V TO J2, K2)	CLOCK, CLEAR
JK	$\overline{J2}$, $\overline{K2}$ (OR 4.5 V TO J2, K2)	CLOCK, PRESET
K1	$\overline{K2}$ (OR 4.5 V TO K2)	CLOCK, PRESET
$\overline{K2}$ (OR K2)	NONE	CLOCK, PRESET
K3	$\overline{K2}$ (OR 4.5 V TO K2)	CLOCK, PRESET

FIGURE 110– I_{IL}

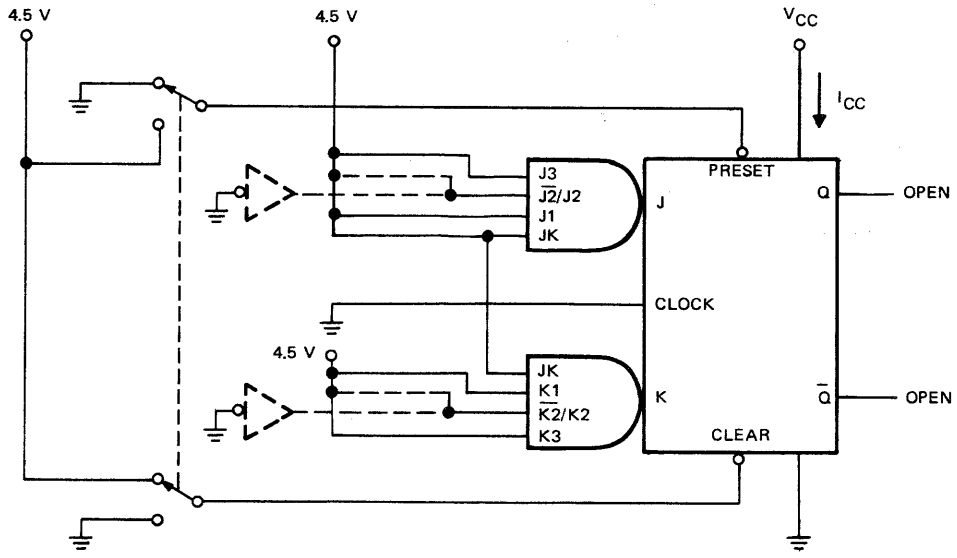
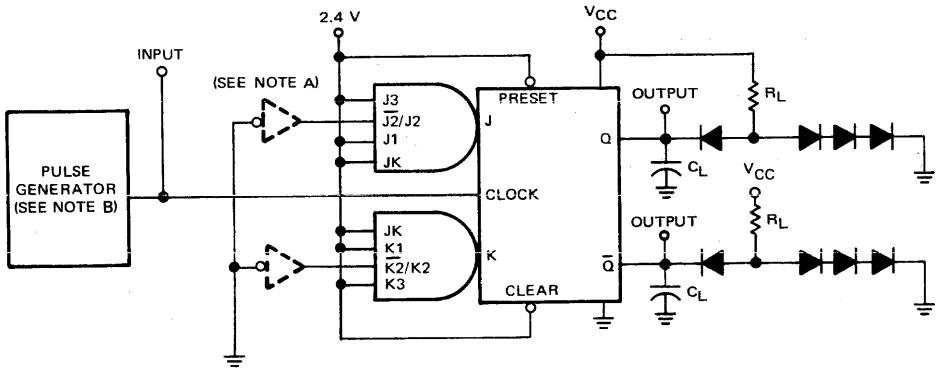


FIGURE 111– I_{CC}

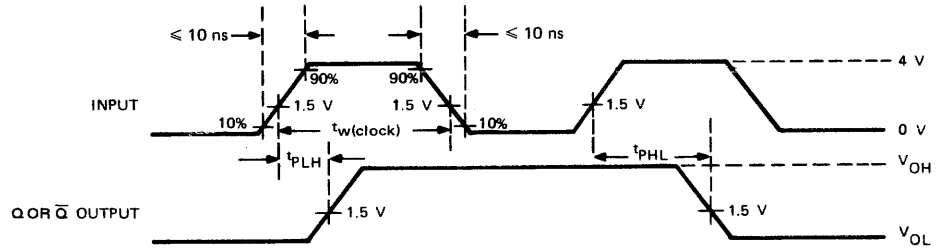
† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



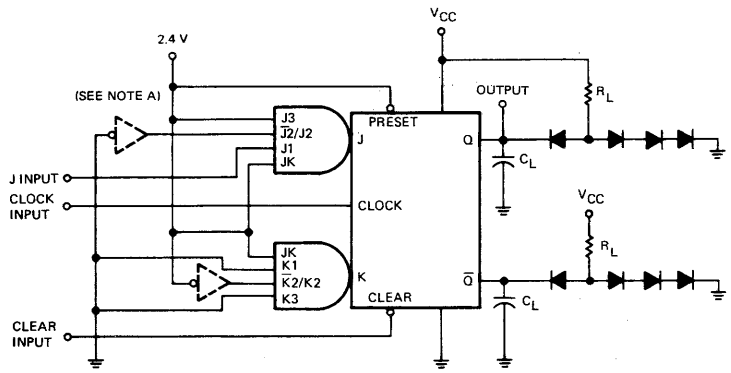
VOLTAGE WAVEFORMS

NOTES: A. Test circuit shown is for the SN54105/SN74105. When testing SN54104/SN74104, the J2 and K2 inputs are connected in parallel with the other J and K inputs.
B. The pulse generator has the following characteristics: $t_{w(clock)}$ = 250 ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

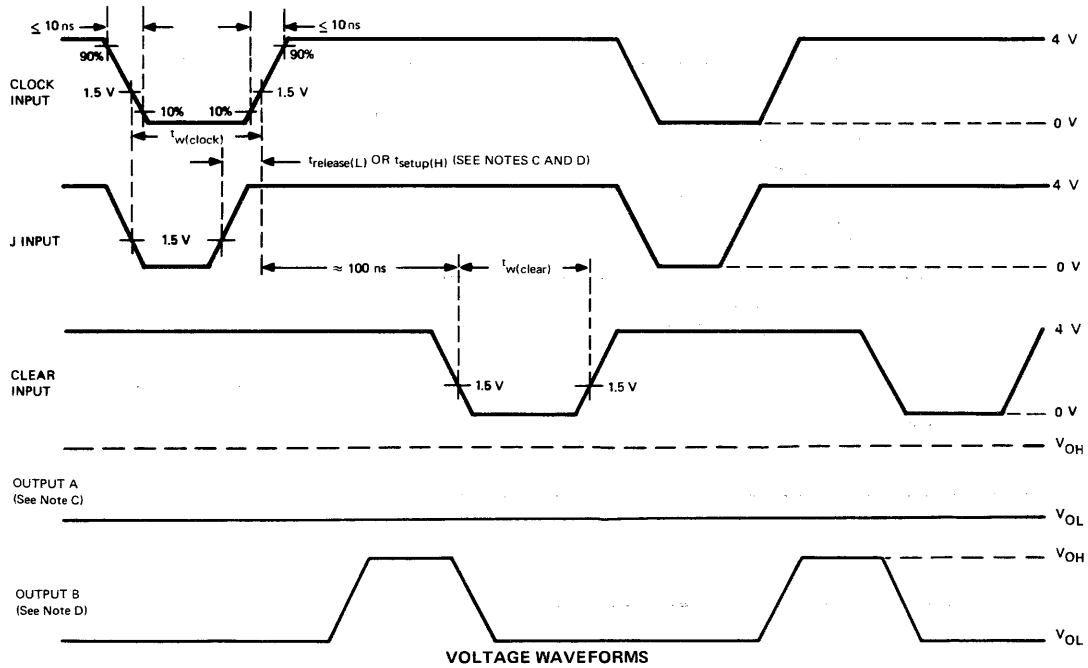
FIGURE 112– PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Test circuit shown is for the SN54105/SN74105. When testing SN54104/SN74104, the J2 input is connected in parallel with the other J inputs and K2 is grounded.

B. The input pulses have the following characteristics: PRR = 1 MHz, $t_{w(clock)}$ = 100 ns, and $t_{w(clear)}$ = 100 ns. For duration of the J-input pulse, see Notes C and D.

C. Output A is valid for: SN54104/SN74104, $t_{release(L)} \leqslant 10$ ns; SN54105/SN74105, $t_{release(L)} \leqslant 1$ ns.

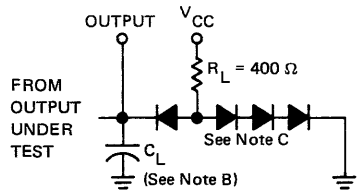
D. Output B is valid for: SN54104/SN74104, $t_{setup(H)} \geqslant 35$ ns; SN54105/SN74105, $t_{setup(H)} \geqslant 10$ ns.

E. C_L includes probe and jig capacitance.

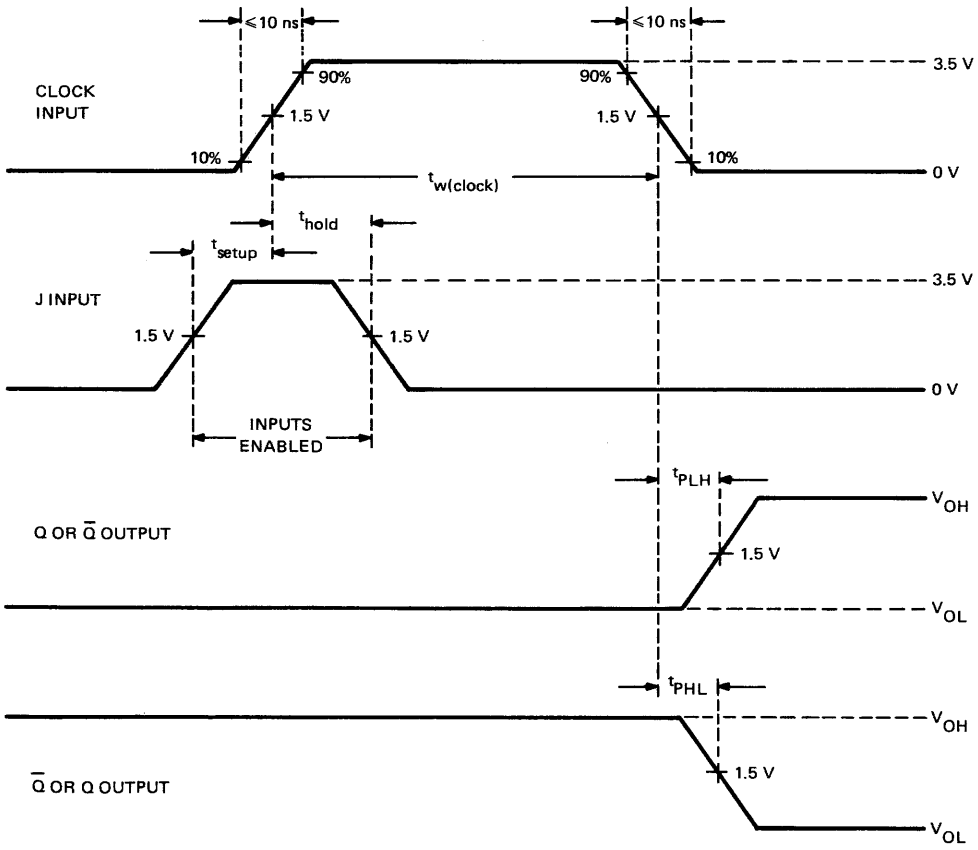
F. All diodes are 1N3064.

FIGURE 113 – INPUT SETUP/RELEASE TIMES

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

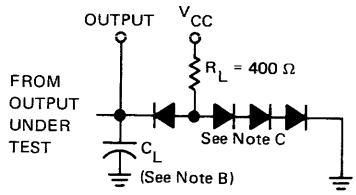


VOLTAGE WAVEFORMS

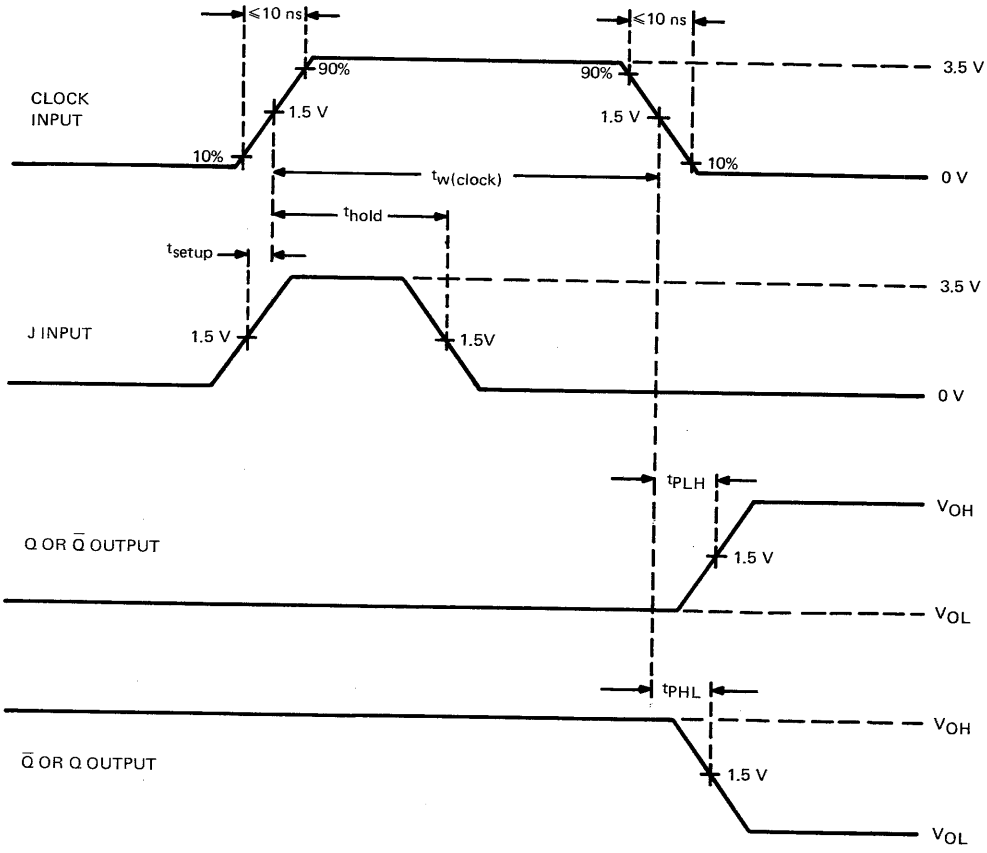
NOTES: A. Both input pulses are supplied by generators with the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$. Clock duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 114

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. Both input pulses are supplied by generators with the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, clock duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 115

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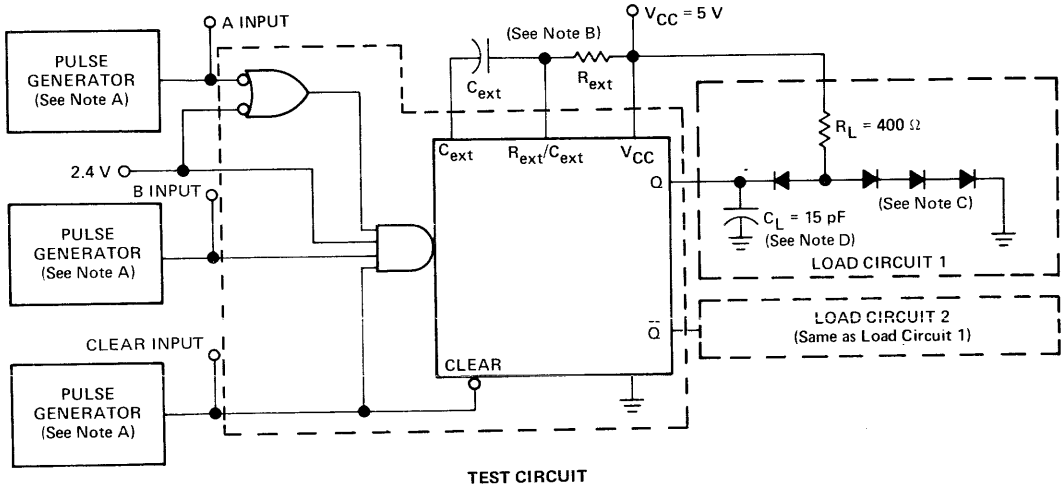
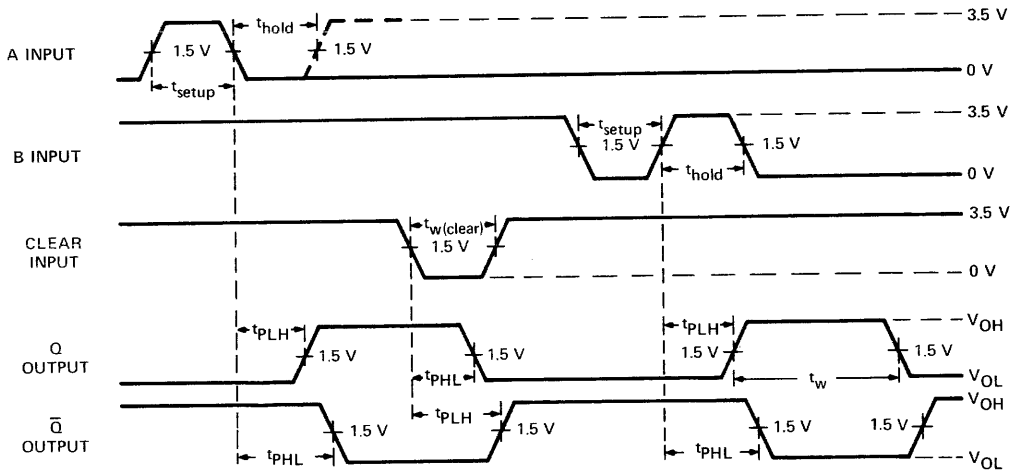
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



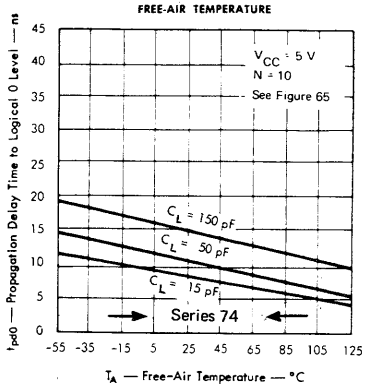
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $t_r \leq 10$ ns (10% to 90% level), $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.
B. See Test Conditions, switching characteristics table, page 3, for values of R_{ext} and C_{ext}.
C. All diodes are 1N3064.
D. C_L includes probe and jig capacitance.

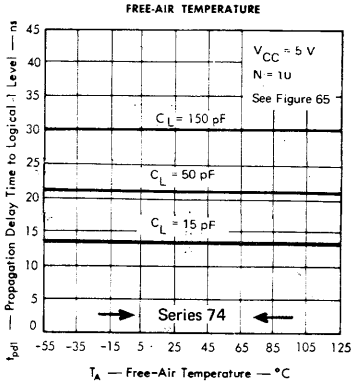
FIGURE 116–SWITCHING TIMES

TYPICAL CHARACTERISTICS §

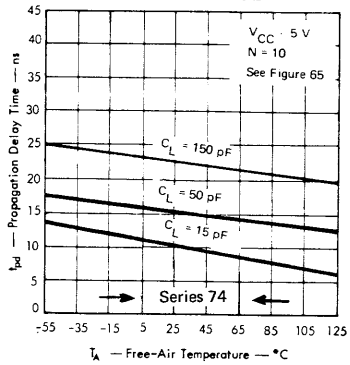
PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL
vs
FREE-AIR TEMPERATURE



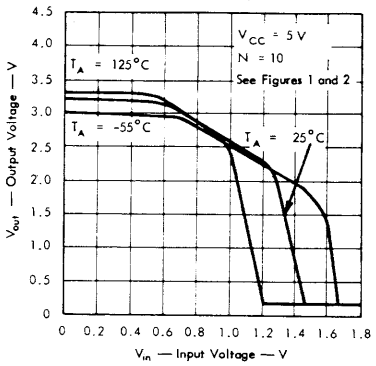
PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL
vs
FREE-AIR TEMPERATURE



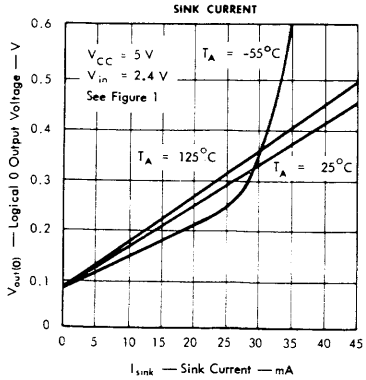
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE



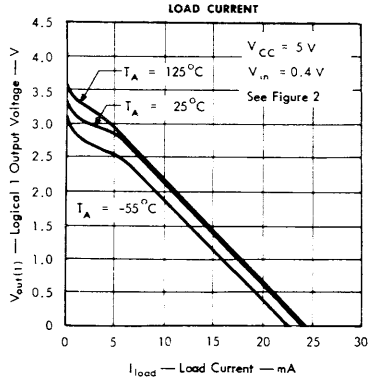
OUTPUT VOLTAGE
vs
INPUT VOLTAGE



LOGICAL 0 OUTPUT VOLTAGE
vs
SINK CURRENT



LOGICAL 1 OUTPUT VOLTAGE
vs
LOAD CURRENT



§ Unless otherwise noted, data as shown is applicable for: SN5400, SN5402, SN5404, SN5410, SN5420, SN5430, SN5450, SN5451, SN5453, SN5454, SN7400, SN7402, SN7404, SN7410, SN7420, SN7430, SN7450, SN7451, SN7453, SN7454.

TEXAS INSTRUMENTS
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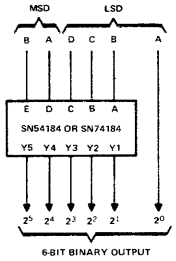
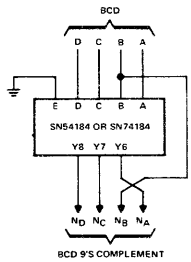
SN54184 and SN74184 BCD-to-binary converters (continued)

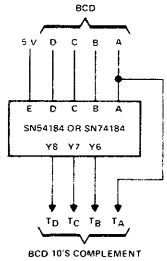
6-BIT CONVERTER



BCD 9'S COMPLEMENT CONVERTER



BCD 10'S COMPLEMENT CONVERTER



TRUTH TABLE
BCD-TO-BINARY CONVERTER

BCD WORDS	INPUTS (See Note A)						OUTPUTS (See Note B)				
	E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	L	L	L	L	L
2-3	L	L	L	L	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	L	L	L	H	L
6-7	L	L	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	L	L	H	L	L
10-11	L	H	L	L	L	L	L	L	H	L	H
12-13	L	H	L	L	H	L	L	L	H	H	L
14-15	L	H	L	H	L	L	L	L	H	H	H
16-17	L	H	L	H	H	L	L	H	L	L	L
18-19	L	H	H	L	L	L	L	H	L	L	H
20-21	H	L	L	L	L	L	L	H	L	H	L
22-23	H	L	L	L	H	L	L	H	L	H	H
24-25	H	L	L	H	L	L	L	H	H	L	L
26-27	H	L	L	H	H	L	L	H	H	L	H
28-29	H	L	H	L	L	L	L	H	H	H	L
30-31	H	H	L	L	L	L	L	H	H	H	H
32-33	H	H	L	L	H	L	H	L	L	L	L
34-35	H	H	L	H	L	L	H	L	L	L	H
36-37	H	H	L	H	H	L	H	L	L	H	L
38-39	H	H	H	L	L	L	H	L	L	H	H
ANY	X	X	X	X	X	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: A. Input conditions other than those shown produce highs at outputs Y1 through Y5.

B. Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

In addition to BCD-to-binary conversion, the SN54184 and SN74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the truth table (above, right) when the devices are connected as shown above the truth table.

TRUTH TABLE
BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

BCD WORD	INPUTS (See Note C)						OUTPUTS (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: C. Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

D. Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

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