Texas Instruments TMS320C30 DSP Preview Bulletin

OVERVIEW

The TMS320C30 Digital Signal Processor (DSP) is a CMOS 32-bit third-generation microprocessor in the industry-standard TMS320 family. The TMS320 family's high-speed number-crunching capability, powerful instruction sets, and innovative architectures have made this high-performance family of processors ideal for DSP applications.

The TMS320C30's 60-ns cycle time allows it to execute more than 33 million floating-point operations per second (MFLOPS). It approaches performance previously available only on a supercomputer. Even higher performance is gained through its large on-chip memories, concurrent DMA controller, and instruction cache.

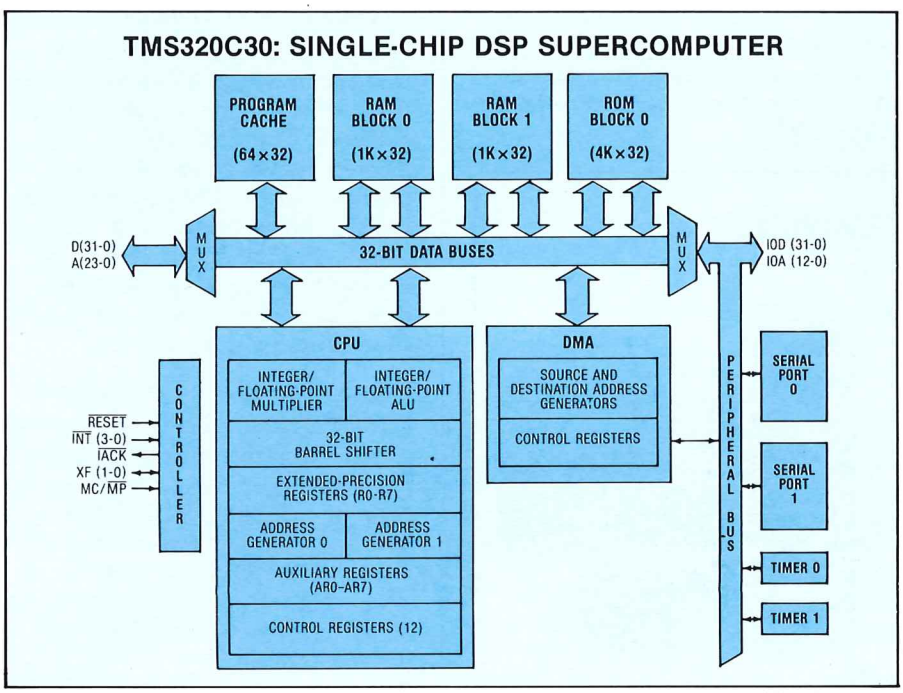
High-density one-micron CMOS technology allows numerous on-chip features which minimize the total system cost. These include an instruction cache, large memories, full floating-point multiplier and ALU, DMA controller, serial ports, and timers.

Since the TMS320C30 is a floating-point DSP, numbers no longer must be scaled, thereby making code development much easier. Software development is accelerated by tools such as a C compiler and a translator that converts existing TMS320 programs to TMS320C30 code.

DEVELOPMENT SUPPORT

Texas Instruments also provides an extensive catalog of development tools and support including:

- □ Software and hardware development tools
- □ Application software
- □ Training workshops
- □ Third-party hardware and software
- □ Local technical support and hotline

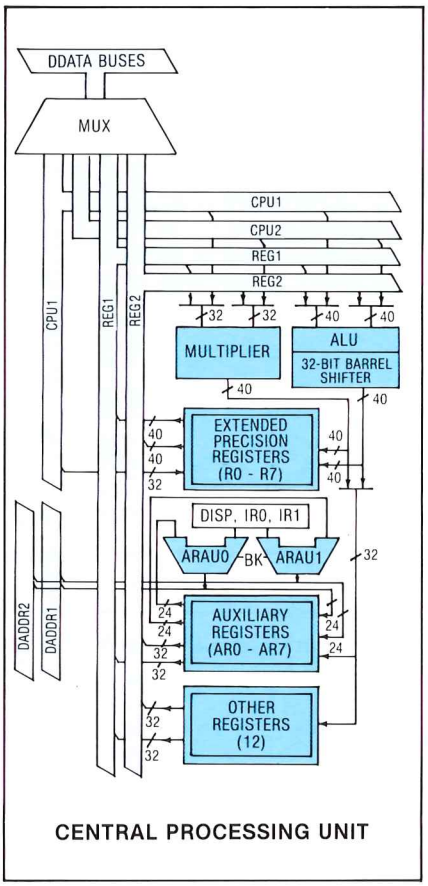


FEATURES	BENEFITS
□ 60-ns single-cycle execution time (more than 33 MFLOPS) □ 2K×32-bit dual-access RAM □ 4K×32-bit dual-access ROM □ 64×32-bit instruction cache □ Single-cycle floating-point multiply/accumulate □ On-chip DMA controller □ Zero-overhead loops and single-cycle branches	□ High performance for realtime digital signal processing
□ Floating-point, integer, and logical 32/40-bit ALU □ Flexible, general-purpose instruction set and addressing modes □ 16-megaword memory space □ Register-based CPU □ Complete line of support tools □ High-level language supported	□ Ease of use
□ On-chip serial ports and timers □ Large on-chip memories, instruction cache, and DMA controller □ Peripheral bus for customization	□ Minimum number of chips for reduced cost, space, and power consumption

IMPORTANT NOTICE:
This document contains advance information on products in the sampling or pre-production stage.

ARCHITECTURE

The architecture of the TMS320C30 allows floating-point operations to be performed at fixed-point speeds. This is achieved through its 60-ns instruction cycle and a high degree of parallelism. The accuracy and precision of its floating-point units relieve the designer of many integer operation problems such as overflow or operand alignment. Its on-chip DMA controller supporting concurrent I/O, along with its general-purpose features and register-based architecture also enhance performance of the TMS320C30.



CENTRAL PROCESSING UNIT

The CPU

The CPU consists of a multiplier, ALU, 32-bit barrel shifter, auxiliary register arithmetic units, supporting register file, and associated buses. The multiplier performs single-cycle integer and floating-point multiplications. Inputs to the multiplier are 32-bit floating-point or 24-bit integer values. The ALU performs single-cycle 32-bit integer, 32-bit logical, and 40-bit floating-point operations, including single-cycle integer and floating-point conversions. Results of the multiplier and the ALU are always maintained in 32-bit integer and 40-bit floating-point formats. The barrel shifter can shift up to 32 bits left or right in a single cycle. The internal buses, CPU1/CPU2 and REG1/REG2, carry two operands from memory and two operands from the register file. This makes it possible for the CPU to perform parallel multiplies and adds (subtracts) on four integer or floating-point operands in a single cycle.

Floating-Point Operations

Floating-point operations provide convenient and trouble-free computations while maintaining accuracy and precision. The TMS320C30 implementation of floating-point arithmetic allows for floating-point operations at integer speeds. The floating-point capability can prevent problems with overflow, operand alignment, and other burdensome tasks common to integer operations.

Register-Based CPU Architecture

The TMS320C30 has a register-based CPU architecture built around 28 registers. These may be operated upon by the multiplier and ALU. The first eight registers (R0-R7) are the extended-precision registers. These registers support operations on 40-bit floating-point numbers and 32-bit integers.

The next eight registers (AR0-AR7) are the auxiliary registers, whose primary function is the generation of the 24-bit addresses. However, they also may be used as general-purpose 32-bit registers. Two auxiliary register arithmetic units (ARAU0 and ARAU1) can generate two addresses in a single cycle. The ARAUs operate in parallel with the multiplier and ALU. They support displacements and indexes for linear, circular, and bit-reversed addressing.

The remaining registers support a variety of system functions: addressing, stack management, processor status, block repeat, and interrupts.

Data Organization

Two integer formats are supported on the TMS320C30:

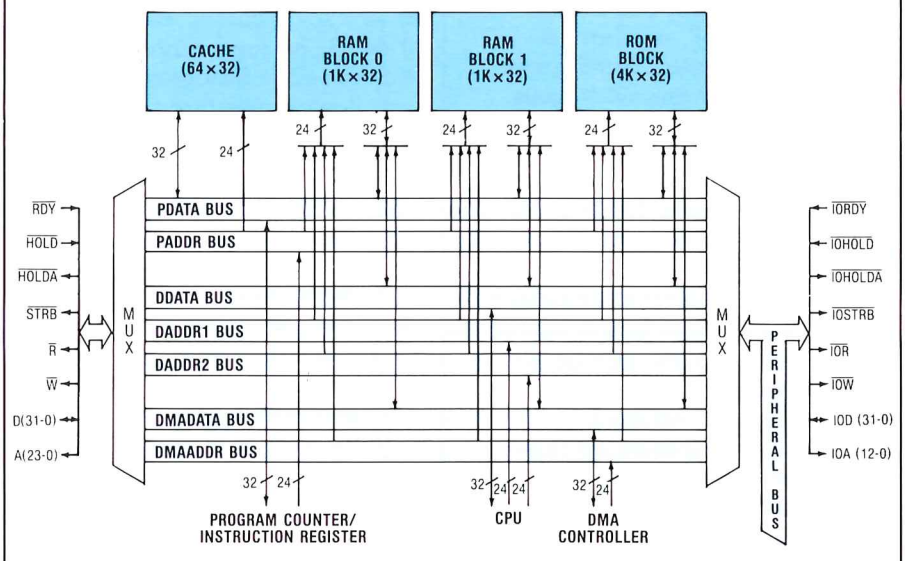
- 16-bit format used for immediate signed or unsigned integer operands
- 32-bit single-precision signed or unsigned integers

Three floating-point formats are available on the TMS320C30:

- 16-bit short floating-point format for immediate floating-point operands
- 32-bit single-precision format
- 40-bit extended-precision format

Large Memory Space

All addressing is performed by a 32-bit machine word. Program, data, and I/O space are contained within a single logical 16M-word memory space allowing tables, coefficients, program code, or data to be stored in either RAM or ROM. This single logical memory space allows the user



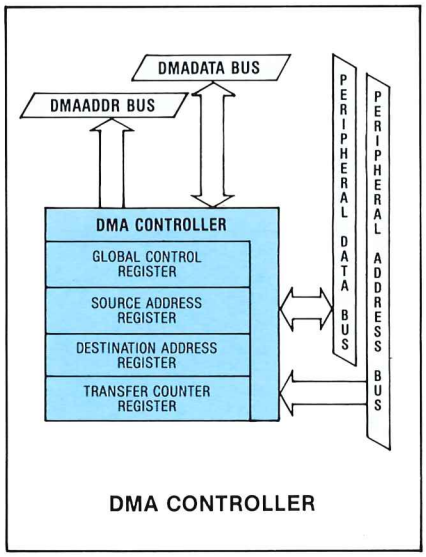
MEMORY ORGANIZATION

to maximize memory usage and to allocate the memory space as required.

RAM blocks 0 and 1 are each 1K×32 bits. The ROM block is 4K×32 bits. Each RAM or ROM block is capable of supporting two accesses in a single cycle. The separate program, data, and DMA buses allow for parallel program fetches, data reads and writes, and DMA operations. In a single cycle, the CPU can access two data values in one RAM block and perform an external program fetch in parallel with the DMA loading another RAM block. Management of memory resources and busing is handled by the memory controller.

Instruction Cache

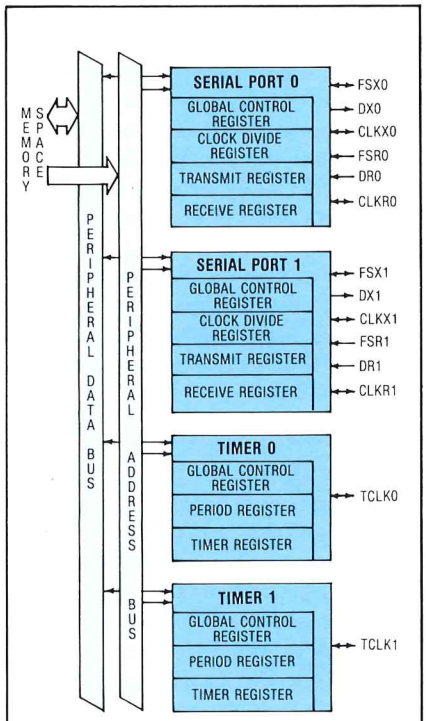
A 64×32-bit instruction cache allows for maximum system performance with minimal system cost. The instruction cache holds often repeated sections of code to greatly reduce the number of off-chip accesses necessary. This allows for code to be stored off-chip in slower, low-cost memories. Also, the external buses are freed for use by the DMA, external memory fetches, or other devices in the system.



DMA CONTROLLER

DMA

The TMS320C30 contains an on-chip Direct Memory Access (DMA) controller. The DMA controller can read from and write to any location in the memory map without interfering with the CPU. Therefore, it is possible to interface the TMS320C30 to slow external memories and peripherals (A/Ds, serial ports, etc.) without reducing the throughput of the CPU. The result is improved system performance and decreased system cost.



PERIPHERAL MODULES

The DMA controller contains its own address generators, source and destination registers, and transfer counter. Dedicated DMA address and data buses prevent conflicts between the CPU and the DMA controller. A DMA operation can be a block or single word transfer to or from memory.

The DMA controller can respond to interrupts in much the same way as the CPU. This ability allows the DMA to transfer data based upon the interrupts received. Thus I/O transfers normally performed by the CPU can instead be performed by the DMA. Again, the CPU may continue processing data while the DMA brings in or sends out data.

Peripherals

All peripheral modules are manipulated through memory-mapped registers located on a dedicated peripheral bus. This peripheral bus allows for the straightforward addition, removal, and creation of peripheral modules.

Timers/Counters

The two timer modules are general-purpose 32-bit timer/event counters, with two signaling modes and internal or external clocking. Available to each timer is an I/O pin that can be used as an input clock to the timer, or as an output signal driven by the timer. The pin may also be configured as a general-purpose I/O pin.

Serial Ports

The two serial ports are modular and totally independent. The zero-glue interface to codecs allows for a minimum chip solution. Each serial port can be configured to transfer 8, 16, 24, or 32 bits of data per frame. The clock for each serial port can originate either internally or externally. An internally generated divide-down clock is provided. The maximum speed of the serial ports is greater than 8 megabits per second. The pins of the serial ports are configurable as general-purpose I/O pins. A special handshake mode allows TMS320C30s to communicate over their serial ports with guaranteed synchronization. Also, the serial ports may be configured to operate as timers.

External Interfaces

The TMS320C30 provides two external interfaces: the parallel interface and the I/O interface. The parallel interface consists of a 32-bit data bus, a 24-bit address bus, and a set of control signals. The I/O interface consists of a 32-bit data bus, a 13-bit address bus, and a set of control signals. Both ports support an external ready signal for wait-state generation and the use of software-controlled wait states. The TMS320C30 has sufficient internal and external busing to achieve the full performance benefit of the machine and to execute programs at full speed. There are effectively four internal buses to perform two independent date fetches, a program fetch, and a DMA fetch—all concurrently in a single cycle. Two external buses are available for simultaneous program, data, and DMA fetches.

The TMS320C30 supports four external interrupts, a number of internal interrupts, and a nonmaskable external reset signal. Two external I/O flags, XF0 and XF1, may be configured as input or output pins under software control. These pins are also used by the interlocked instructions to support multiprocessor communication.

ADDRESSING MODES

The TMS320C30 supports six powerful addressing modes that allow the user to access data from memory or registers: register mode, direct mode, indirect mode, short-immediate mode, long-immediate mode, and PC-relative mode. In a single cycle, two independent addresses can be generated and two independent data fetches can occur.

POWERFUL INSTRUCTION SET

The TMS320C30 instruction set is exceptionally well suited to digital signal processing and other numerically intensive applications. All instructions are a single machine word long. In addition to multiply and accumulate instructions, the TMS320C30 possesses a full complement of general-purpose instructions.

Instruction Set Groups

- □ Load and store
- □ Two-operand arithmetic/logical
- □ Three-operand arithmetic/logical
- □ Parallel-operation
- □ Arithmetic/logical operations with store
- □ Program control
- □ Interlocked-operations

Included in the load and store instructions is the ability to load a register conditionally. This operation is particularly useful for locating the maximum and minimum of a set of data.

The two-operand arithmetic and logical instructions consist of a complete set of arithmetic instructions. This includes floating-point, integer, and logical operations, support of multiprecision arithmetic, and 32-bit arithmetic and logical shifts.

The three-operand arithmetic and logical instructions are a subset of the two-operand arithmetic and logical instructions. These instructions provide for the reading of two operands from memory and/or the CPU register file in a single cycle.

The parallel-operation instructions allow for a high degree of parallelism. These instructions support very flexible, parallel floating-point and integer multiplies and adds. They also include the ability to load two registers in parallel.

The arithmetic/logical operations with store instructions also support a high degree of parallelism and thus complement the parallel-operation instructions. They permit extremely rapid operations on blocks of memory.

The program-control instructions consist of all those operations that affect the program flow. These fall into two main types: repeat modes and branching.

Block Repeat Instructions

For many algorithms, there is an inner kernel of code where most of the execution time is spent. The repeat modes of the TMS320C30 allow for the implementation of zero-overhead looping. When using the repeat modes, these time-critical sections of code can be executed in the shortest possible time. The instructions supporting the repeat modes are RPTS (repeat a single instruction) and RPTB (repeat a block of code). The block size is unlimited and can be interrupted during execution.

Single-Cycle Branch Instruction

The branching capabilities of the TMS320C30 include two main subsets: standard and delayed branches. Standard branches execute in four cycles and include calls and returns. Delayed branches execute in a single cycle. There are multiple conditions to branch on for both the standard and delayed branches.

Multiprocessor Support

The interlocked-operations instructions support multiprocessor communication. Through the use of external signals, these instructions allow for powerful synchronization mechanisms, such as semaphores, to be implemented.

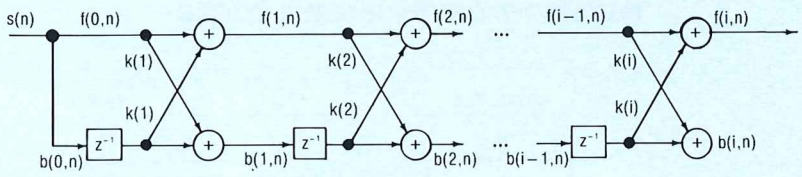
APPLICATIONS

The TMS320C30 opens doors to new applications with its ability to perform floating-point operations at fixed-point speeds.

Lattice Implementation of an LPC Filter

Speech is being used in many applications such as telecom equipment, consumer toys, automobiles and computer voice systems. In a wide variety of speech systems, the LPC (Linear Predictive Coding) filter is considered to be the fundamental building block. A common algorithm to implement LPC is the lattice filter. The lattice filter algorithm requires only three cycles per filter tap. Note that the code includes a floating-point multiply and add in parallel (MPYF3 and ADDF3), as well as a floating-point add in parallel with a store of a result to memory (ADDF3 and STF). Furthermore, the algorithm is joined together with the repeat block (RPTB) instruction to allow for zero-overhead looping when the filter is implemented. This illustrates the

```
;=============================================
;LATTICE FILTER (LPC INVERSE FILTER - ANALYSIS)
;
;EQUATIONS: F(i,n) = f(i-1,n) + k(i) * b(i-1,n-1)
;           b(i,n) = b(i-1,n-1) + k(i) * f(i-1,n)
;=============================================
;
        RPTB    LOOP
        MPYF3   *AR0, *AR1, R0      ; k(i) * b(i-1,n-1) -> R0
||      ADDF3   R2, R0, R2          ; f(i-1-1,n) + k(i-1) * b(i-1-1,n-1)
;                                   ; = f(i-1,n) -> R2
;
;                                   ; b(i-1-,n-1) + k(i-1) * f(i-1-1,n)
        ADDF3   *-AR1(1), R1, R3    ; = b(i-1,n) -> R3
||      STF     R3, *AR1++(IR0)     ; b(i-1-1,n) -> b(i-1-1,n-1)
;
LOOP    MPYF3   *AR0==(1), R2, R1   ; k(i) * f(i-1,n) -> R1
```



A set of 'k' parameters, used to describe the speech, is illustrated in the signal flowgraph for the lattice implementation of the LPC filter.

TMS320C30's ability to perform floating-point operations, two memory accesses per cycle, parallel operations, and zero-overhead looping.

The TMS320C30 can efficiently utilize its internal peripheral modules as illustrated by its two independent serial ports allowing for zero-glue interconnection to the codecs. Since the serial ports are independent, they may run asynchronous with respect to each other.

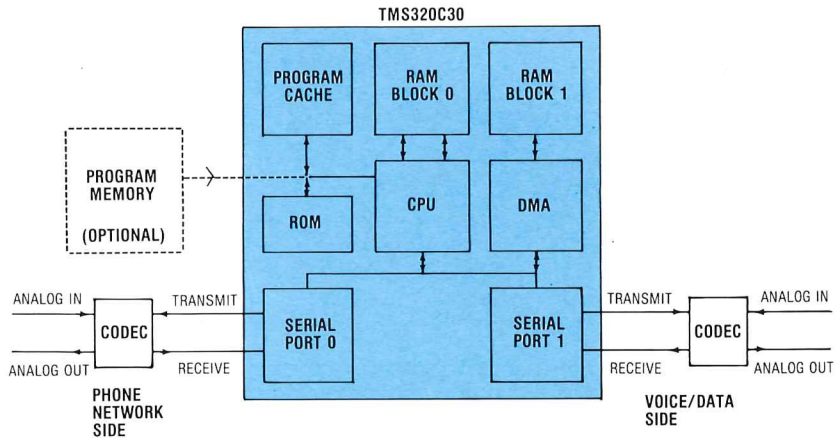
The DMA can read from both serial ports and transfer data into RAM block 1 which contains the next frames of data to be processed. While the DMA is moving data onto the chip, the CPU is processing data in RAM block 0. The program is initially fetched from off-chip memory, which may be a slow, inexpensive memory. This code is then stored in the instruction cache, where it can be fetched in a single cycle to utilize the speed of the CPU. Alternately, the program may be stored in on-chip ROM.

For example, the lattice filter code shown is only 4 words long and easily fits into the 64-word instruction cache. After the current frames are processed, the DMA can use RAM block 0 for the next incoming frames while the CPU processes data in RAM block 1.

The result is a very low chip count system that provides an unprecedented level of performance.

TMS320C30 Benchmarks

Benchmark	Performance
FIR filter tap with data shift	60 ns
256-tap FIR sample rate	>60 kHz
LMS adaptive FIR filter tap and data shift	180 ns
256-tap adaptive FIR filter sample rate	>20 kHz
Cascaded IIR biquad filter element (five coefficients)	360 ns
Echo canceller (single chip)	>64 ms
Lattice filter tap	180 ns
Vector dot product (per element)	60 ns



This TMS320C30 hardware system is appropriate for a number of applications including voice and data compression/expansion, echo cancellation, data encryption, speech synthesis, and speech recognition.

DEVELOPMENT AND SUPPORT TOOLS

Digital signal processors are essentially application-specific microprocessors or microcomputers. Like any other microprocessor, no matter how impressive the performance of the processor or the ease of interfacing, without good development tools and technical support, it is difficult to design it into a system. The TMS320C30 has a wide range of development tools for software and hardware designers.

Assembler/Linker

The assembler/linker is available on PC MS-DOS and VAX VMS for users to develop their TMS320C30 DSP algorithms. The macro assembler converts TMS320C30 source code into TMS320C30 executable object code. This package also supports TMS320C1x and TMS320C2x source code translation to TMS320C30 source code. The linker permits a program to be designed and implemented in separate modules that will later be linked together to form a complete program. An archiver is also included to compress the size of object files.

C Compiler

The C compiler is a full implementation of the standard Kernighan and Ritchie C. The compiler outputs assembly language source code which can then be fed directly into the assembler. The compiler also supports the insertion of assembly language code into the C source code. The user may write functions in assembly language and then call these functions from the C source. Similarly, C functions may be called from assembly language. Variables defined in the C source may be accessed in assembly language modules and vice versa. The result is a compiler that allows the user to tailor the amount of high-level programming versus the amount of assembly language according to the application.

Simulator

The simulator is a software program that simulates operations of the device for program verification. It also enables the user to monitor the state of the simulated TMS320C30 while the program is executing. The simulator uses the object code pro-

duced by the macro assembler/linker and is available on PC MS-DOS and VAX VMS.

Software Development System (SWDS)

The Software Development System is a PC-resident tool that executes code on a TMS320C30. The SWDS offers the user the system interface necessary to write, assemble/link, load, and debug the TMS320C30 code on a PC workstation.

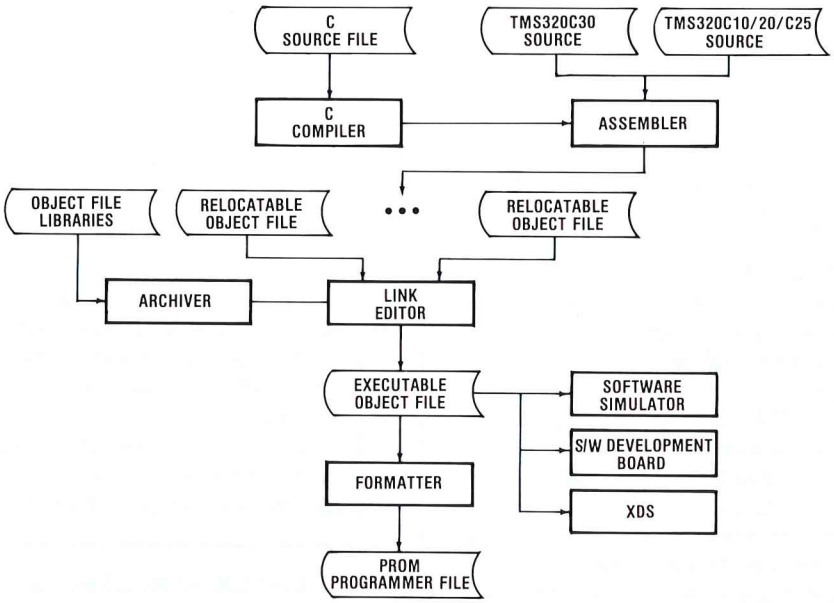
Emulator (XDS)

The XDS is a powerful, full-speed in-circuit emulator with realtime hardware breakpoint/trace and program execution capability from target memory. The XDS allows integration of the hardware and software modules in the debug mode.

Other Development Support

Other development support includes a growing library of textbooks and reference guides as well as a technical support hotline (713-TRY-A-320 or 713-879-2320) and bulletin board service. TI's Regional Technology Centers (RTCs) provide hands-on workshops and design services. Many third parties with DSP expertise can provide assistance in various application areas.

TMS320C30 DEVELOPMENT TOOLS



The TMS320C30 has a complete line of hardware and software development tools to accelerate your time to market and ease development.

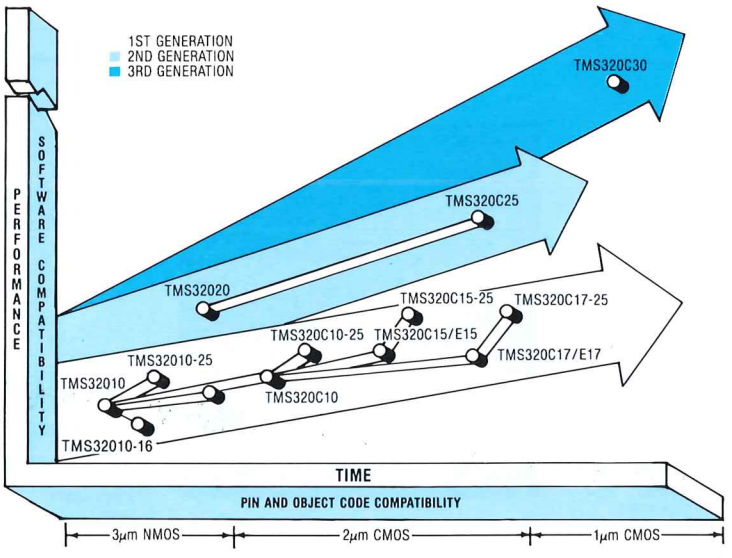
Availability

The TMS320C30 Assembler/Linker and Simulator are available now. The C Compiler, SWDS, and XDS will be available in early 1988.

To receive additional literature on the TMS320C30 as it becomes available, fill out the attached response card.

THE GROWING TMS320 FAMILY

Texas Instruments TMS320 Digital Signal Processor (DSP) Family provides a wide range of devices for your cost/performance needs. With three generations of compatible devices, you can choose a DSP from $5.00 to 33 MFLOPS (million floating-point operations per second). TI can provide your DSP solution.



TMS320 FAMILY GROWTH PROTECTS CUSTOMER INVESTMENT

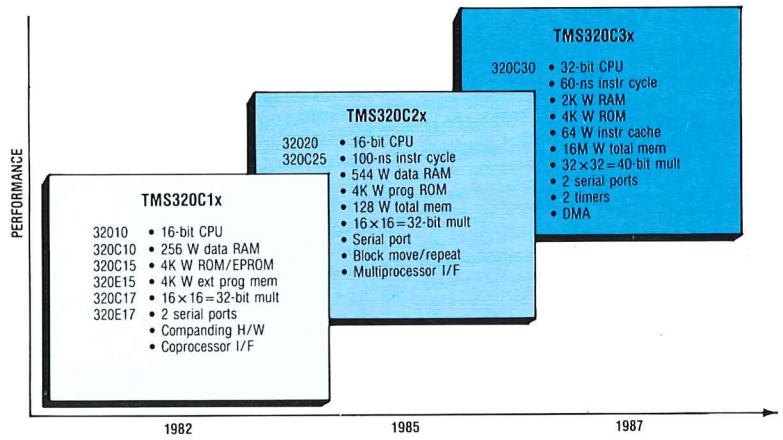
THREE GENERATIONS TO MEET YOUR DSP PERFORMANCE NEEDS

The TMS32010, introduced in 1982, was the first digital signal processor in the TMS320 family. Since then, Texas Instruments has demonstrated its dedication to the advancement of digital signal processing by expanding the family to include enhancements of earlier generations as well as more powerful new generations of digital signal processors.

The three generations of the TMS320 Digital Signal Processors are:

- TMS320C1x — 1st generation
- TMS320C2x — 2nd generation
- TMS320C3x — 3rd generation

For additional information on any of the TMS320 products, contact your local field sales office.



The three generations of compatible TMS320 Digital Signal Processors offer features tailored to your performance needs.

TMS320 FAMILY COMPARISON

GENERATION	DEVICE	TECHNOLOGY	CYCLE TIME (ns)	TYPICAL POWER (W)	DATA TYPE	ON-CHIP MEMORY				TOTAL MEMORY SPACE	I/O				HIGH-LEVEL LANGUAGE	MILITARY VERSIONS
						RAM	ROM	EPROM	CACHE		PARALLEL	SERIAL	DMA	TIMERS		
1ST	TMS32010	NMOS	200	.9	16-bit integer	144	1.5K	–	–	4K	8	–	–	–	3rd party	Now
	TMS32010-16	NMOS	320	.9	16-bit integer	144	1.5K	–	–	4K	8	–	–	–	3rd party	–
	TMS32010-25	NMOS	160	.9	16-bit integer	144	1.5K	–	–	4K	8	–	–	–	3rd party	–
	TMS320C10	CMOS	200	.165	16-bit integer	144	1.5K	–	–	4K	8	–	–	–	3rd party	Planned
	TMS320C10-25	CMOS	160	.2	16-bit integer	144	1.5K	–	–	4K	8	–	–	–	3rd party	–
	TMS320E15	CMOS	200	.3	16-bit integer	256	–	4K	–	4K	8	–	–	–	3rd party	Planned
	TMS320C15	CMOS	200	.225	16-bit integer	256	4K	–	–	4K	8	–	–	–	3rd party	Planned
	TMS320C15-25	CMOS	160	.25	16-bit integer	256	4K	–	–	4K	8	–	–	–	3rd party	–
	TMS320E17	CMOS	200	.325	16-bit integer	256	–	4K	–	4K	6	2	–	1	3rd party	–
	TMS320C17	CMOS	200	.25	16-bit integer	256	4K	–	–	4K	6	2	–	1	3rd party	–
	TMS320C17-25	CMOS	160	.275	16-bit integer	256	4K	–	–	4K	6	2	–	1	3rd party	–
2ND	TMS32020	NMOS	200	1.5	16-bit integer	544	–	–	–	128K	16	1	†	1	C compiler	Planned
	TMS320C25	CMOS	100	1.0	16-bit integer	544	4K	–	–	128K	16	1	†	1	C compiler	Planned
3RD	TMS320C30	CMOS	60	1.0	32-bit F/I*	2K	4K	–	64	16M	**	2	‡	2	C compiler	Planned

* Floating-Point/Integer
** Unlimited
† External DMA
‡ Internal/External DMA

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