

TEXAS INSTRUMENTS
FIELD PROGRAMMABLE LOGIC DEPARTMENT
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY T1BPAL16XX-10
DEVICES T1BPAL16R4-10, T1BPAL16R6-10, T1BPAL16R8-10, and
INCLUDED T1BPAL16L8-10

PROGRAMMING PROCEDURE:

Array fuses are programmed by executing the following programming sequence. Each fuse can be opened by selecting the appropriate (1 of 32) Input Line and (1 of 8) Product Line. The levels for selecting Input Lines and Product Lines are shown in Tables 1-2 and 1-3.

- Step 1: Raise PGM ENABLE to V_{IH} .
- Step 2: Select an Input Line by applying appropriate levels to PI pins.
- Step 3: Select a Product Line group by applying appropriate logic levels to PA pins. The actual product line selected will be determined by the PO pin (described in step 5).
- Step 4: Raise /OE to V_{IH} .
- Step 5: Raise the selected PO pin to V_{IHH} .
- Step 6: Program the fuse by pulsing V_{CC} to V_{IHH} .
- Step 7: Remove the output voltage.
- Step 8: Lower /OE to V_{IL} to enable device.
- Step 9: Pulse PGM VER pin to V_{IH} .
- Step 10: Verify the blowing of fuse by checking for a V_{OL} at the selected PO pin.

If the fuse is still intact, steps 1 thru 10 may be repeated until the fuse is successfully blown, not to exceed 4 retries. Do not apply additional pulses to a fuse once it is correctly programmed. Verification is possible only with the Security fuse intact.

A single security fuse is provided on each device to discourage the unauthorized copying of fuse patterns. To program the security fuse, follow the steps above omitting steps 5 and 10. Verification is achieved by verifying the entire fuse array. If the security fuse is blown, all other fuses will appear to be unblown.

For Input and Product Line selection, see Tables 1-2 and 1-3.

For programming waveforms, see Figure 1-1.

PREPARED BY B. Cole PAL20Y-1.DWG	DATE 12/04/85	TEXAS INSTRUMENTS		
CHECKED BY <i>[Signature]</i>	DATE 6/30/88	TITLE: ALGORITHM SPECIFICATION T1BPAL16XX-10		
ENGINEER Joel Skellie	DATE 12/04/85			
APPROVED BY <i>[Signature]</i>	DATE 06/30/88	REVISION D	A SIZE	PAL20003
RELEASED BY /	DATE / /	LETTER	SIZE	SHEET 1 10

PIN ASSIGNMENTS IN PROGRAMMING MODE

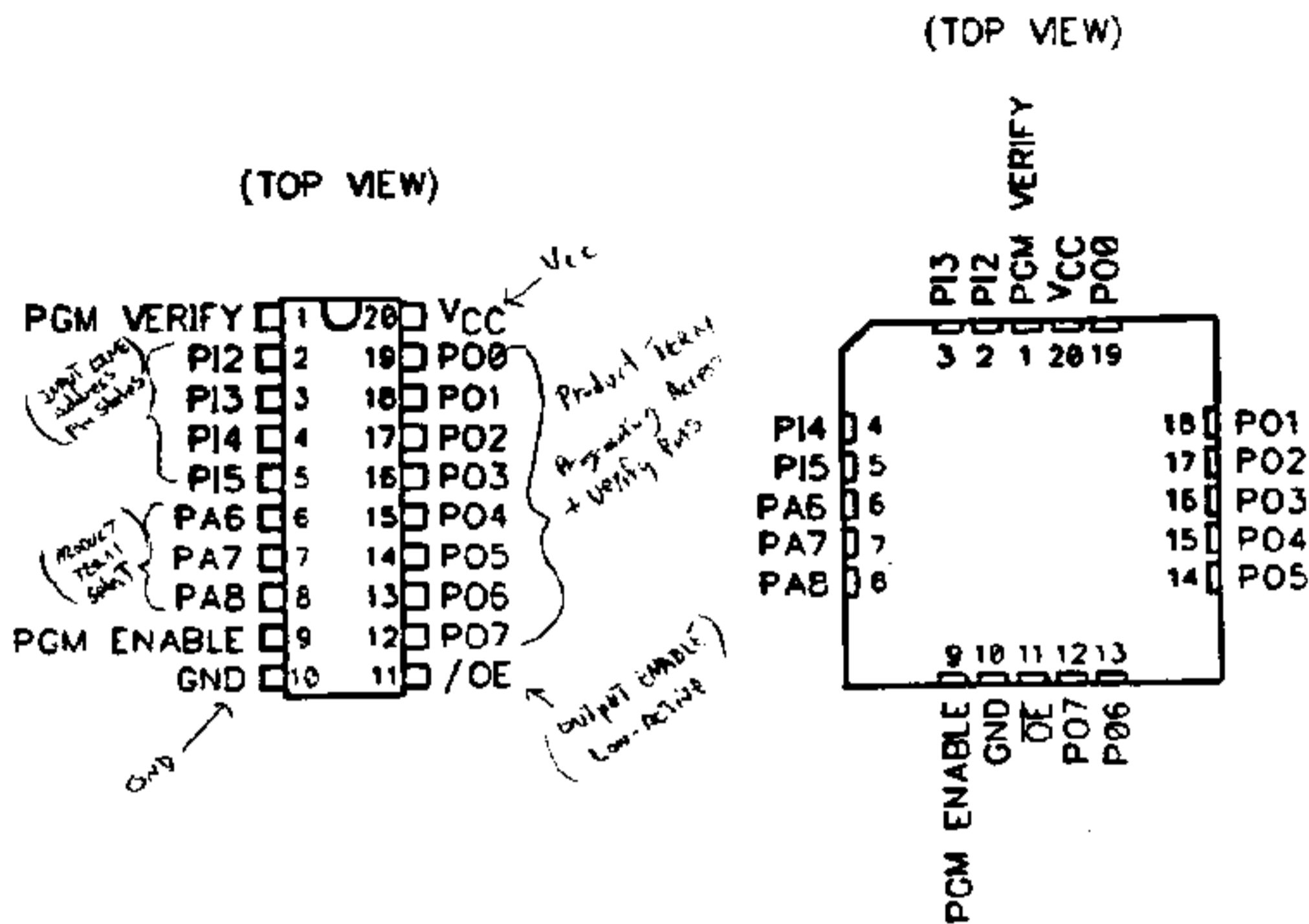


TABLE 1-1. PROGRAMMING PARAMETERS, TA = 25°C

PARAM	DESCRIPTION	MIN	NOM	MAX	UNIT
VCC	Verify-level supply voltage	5.25	5.50	5.75	V
V _{IH}	High-Level input voltage	2.40		5.50	V
V _{IL}	Low-level input voltage			0.50	V
V _{IHH}	Program-pulse voltage	10.25	10.50	10.75	V
	PO	10.25	10.50	10.75	V
	PGM ENA	10.25	10.50	10.75	V
	PI, PA	10.25	10.50	10.75	V
	VCC	9.5	9.75	10	V
I _{IHH}	Program-pulse current		20	40	ma
	PO		5	15	ma
	PGM ENA		2	10	ma
	PI, PA			450	ma
	I _{CC}			50	ma
t _{w1}	Program-pulse duration at VCC	10			us
t _{w2}	Pulse duration of PGM VERIFY	100			ns
t _{su}	Set-up time	100			ns
t _h	Hold time	100			ns
t _{d1}	Delay time from /OE low to PGM VERIFY high.	100			ns
t _{d2}	Delay time from PGM VERIFY high to valid output.	100			ns

TABLE 1-2, INPUT LINE SELECT

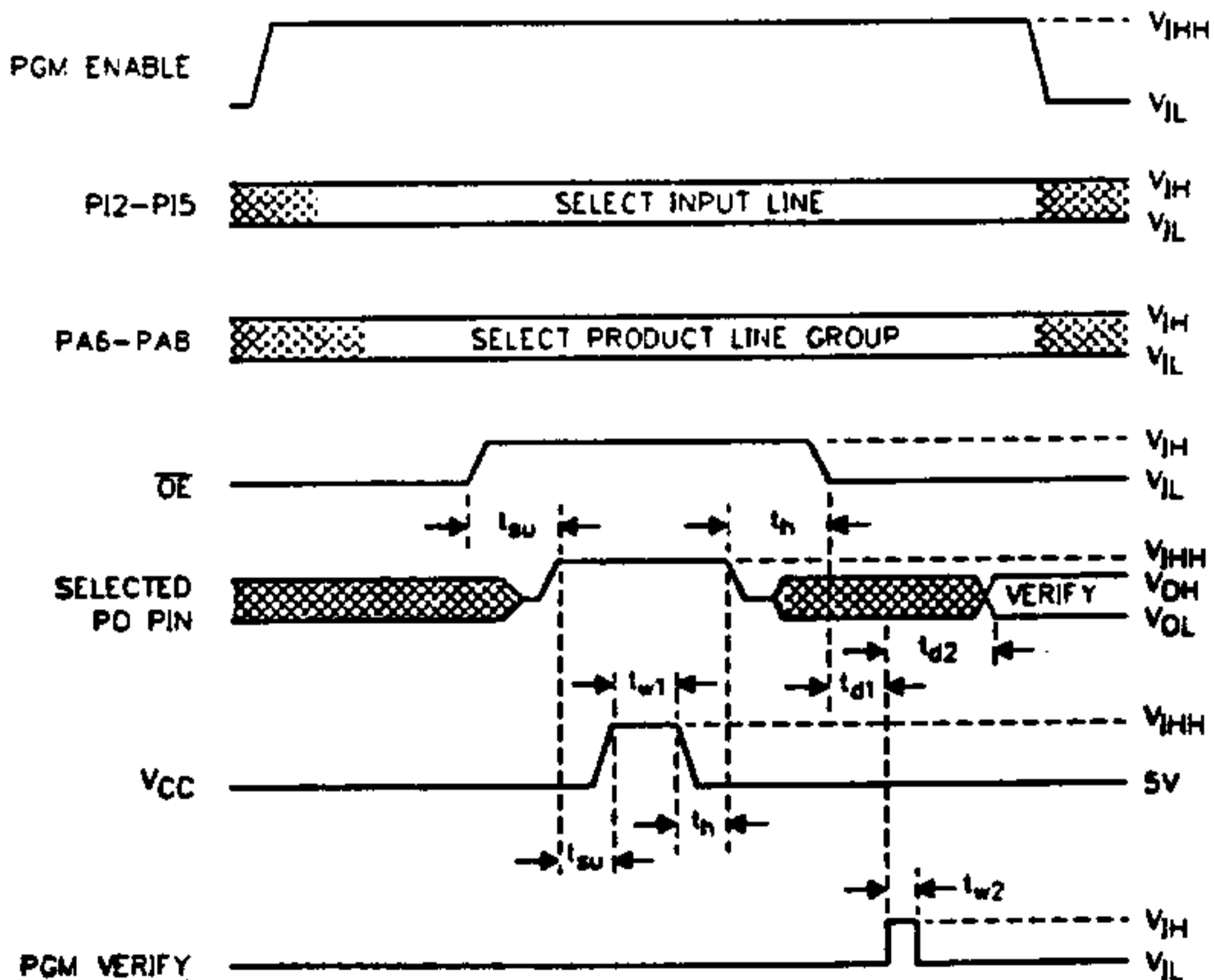
Input Line Number	Input Line Number-Address Pin States			
	P15	P14	P13	P12
00	L	L	L	L
01	L	L	L	L
02	L	L	L	L
03	L	L	L	L
04	L	L	L	L
05	L	L	L	L
06	L	L	L	L
07	L	L	L	L
08	L	L	L	L
09	L	L	L	L
10	L	L	L	L
11	L	L	L	L
12	L	L	L	L
13	L	L	L	L
14	L	L	L	L
15	L	L	L	L
16	L	L	L	L
17	L	L	L	L
18	L	L	L	L
19	L	L	L	L
20	L	L	L	L
21	L	L	L	L
22	L	L	L	L
23	L	L	L	L
24	L	L	L	L
25	L	L	L	L
26	L	L	L	L
27	L	L	L	L
28	L	L	L	L
29	L	L	L	L
30	L	L	L	L
31	L	L	L	L

TABLE 1-3. PRODUCT TERM ADDRESSING

PRODUCT TERM								Product Term Select Address Pin States		
								PAB	PA7	PA6
0	8	16	24	32	40	48	56	L	L	L
1	9	17	25	33	41	49	57	L	L	H
2	10	18	26	34	42	50	58	L	H	L
3	11	19	27	35	43	51	59	L	H	H
4	12	20	28	36	44	52	60	H	L	L
5	13	21	29	37	45	53	61	H	L	H
6	14	22	30	38	46	54	62	H	H	L
7	15	23	31	39	47	55	63	H	H	H
SF →	--	--	--	--	--	--	--	X	X	HH
P00	P01	P02	P03	P04	P05	P06	P07	L = V _{IL} , HH = V _{IHH} H = V _{IH}		
Programming Access and Verify Pin										

SF - Security Fuse (Does not require voltage to the P0 pin)

FIGURE 1-1. PROGRAMMING WAVEFORMS

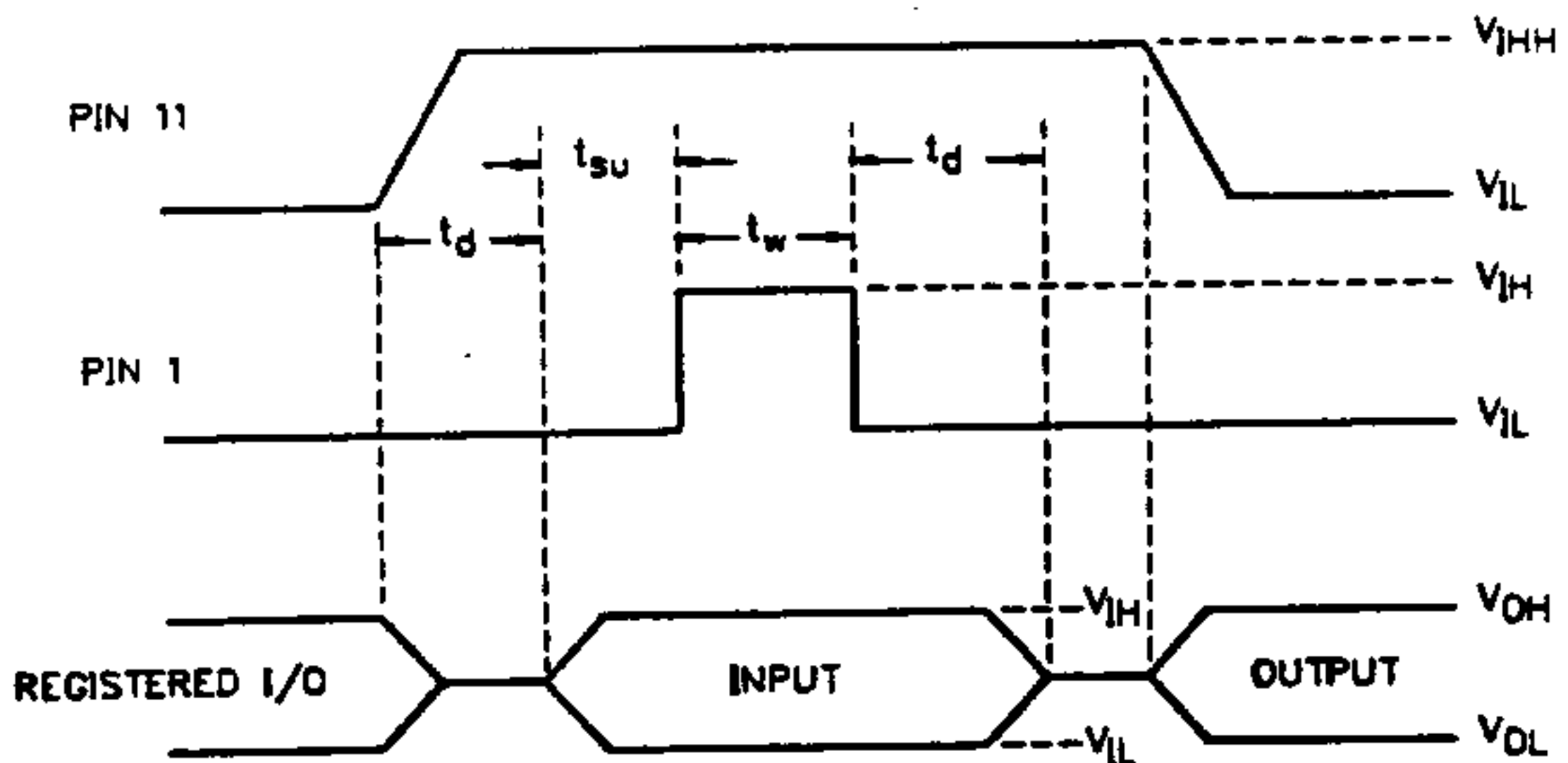


Preload procedure for registered outputs (See Note 2)

The output registers of the TBPAL16XX-10 can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 volts and pin 1 at V_{IL} , raise pin 11 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower pin 11 to V_{IL} .
Preload can be verified by observing the voltage level at the output pin.

Preload waveforms (See Notes 2 and 3)



Notes: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

3. $t_d = t_{su} = t_w = 100$ ns to 1000 ns.
 $V_{IHH} = 10.25$ V to 10.75 V.

PROGRAMMING ALGORITHM TEMPLATE

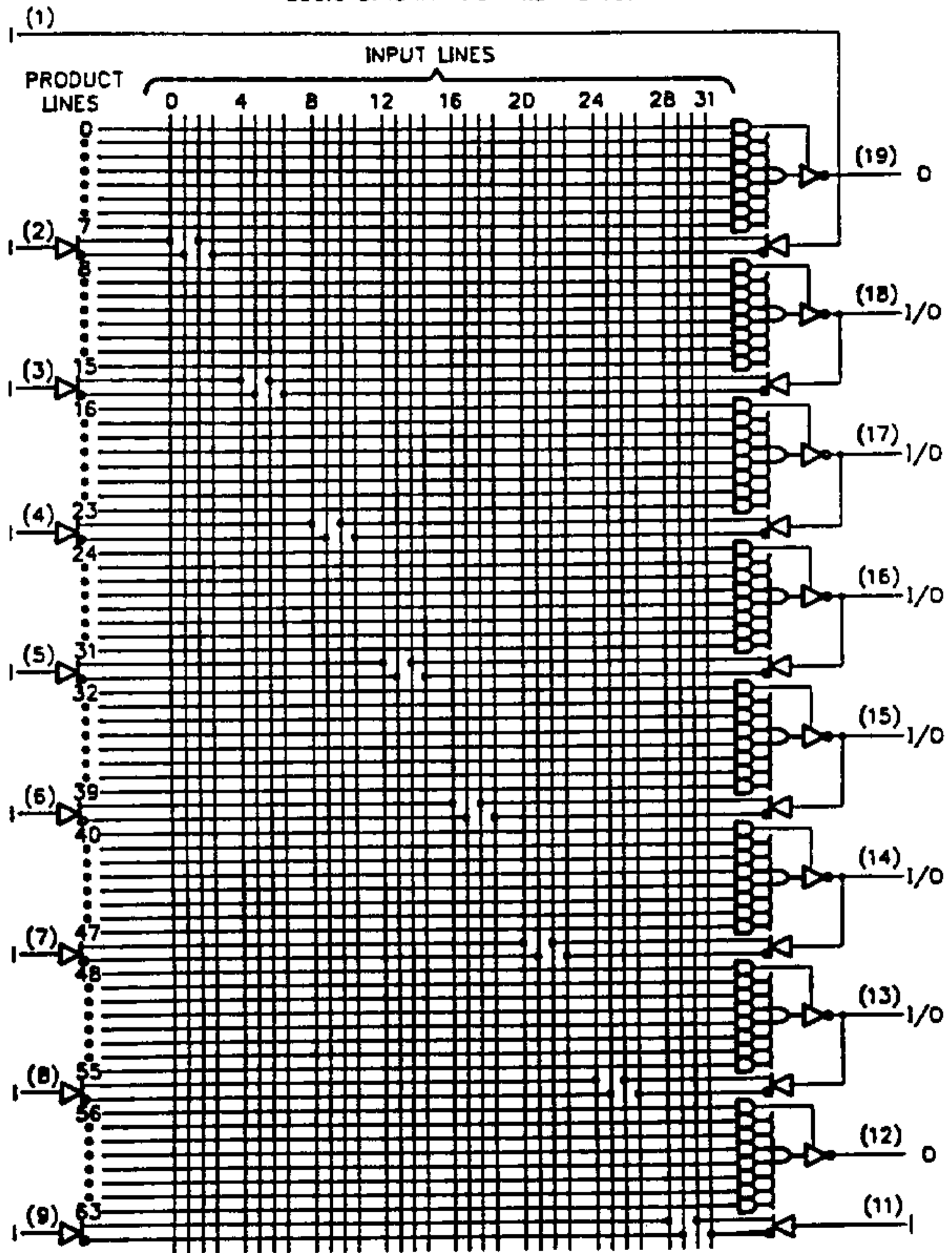
SPECIFICATION NUMBER	PAL20003
DEVICE FAMILY	TIBPAL16XX-10
INCLUDED DEVICES	TIBPAL16L8-10, TIBPAL16R4-10, TIBPAL16R6-10, TIBPAL16R8-10

PROGRAMMER INFO:

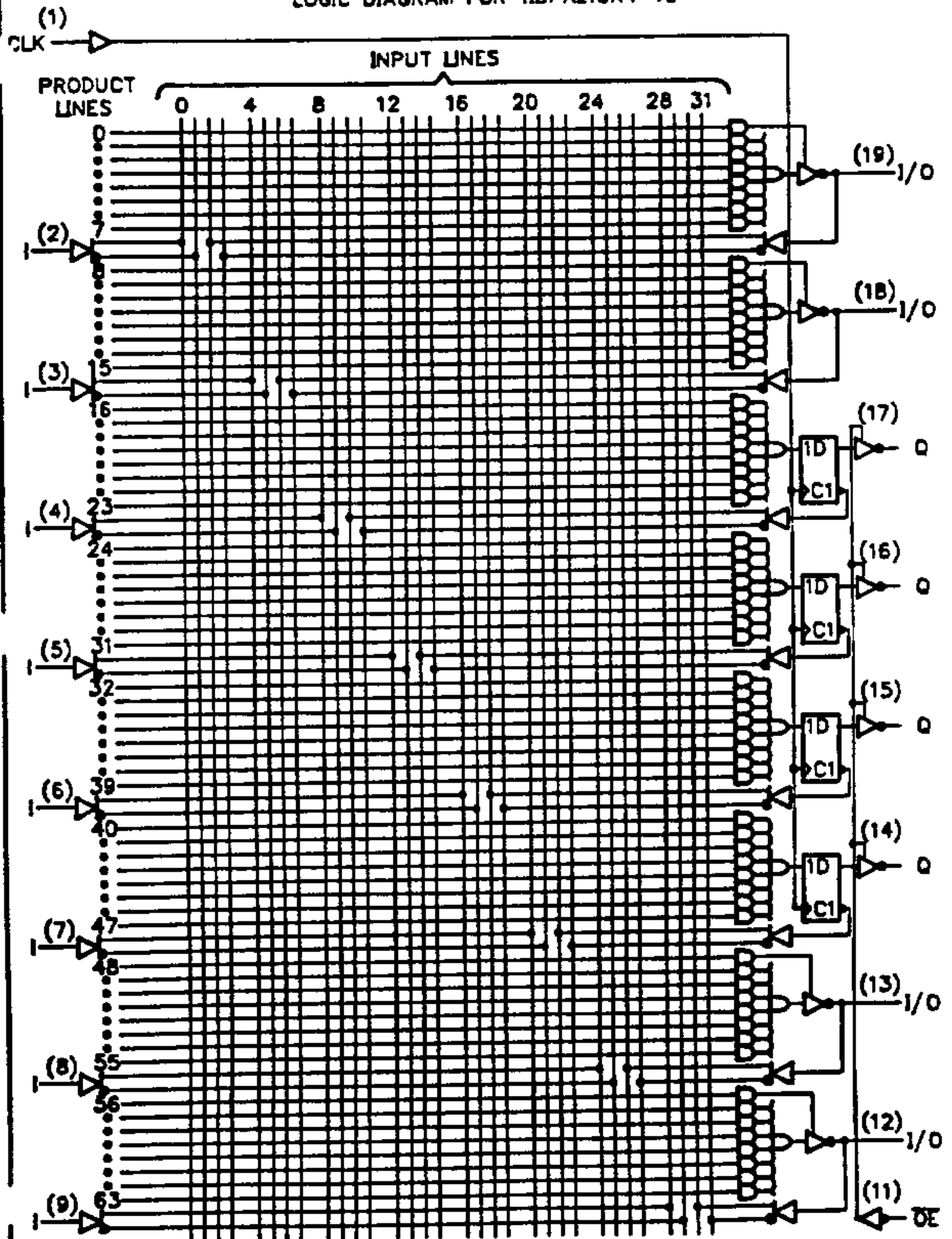
MANUFACTURER :	MODEL:	ADAPTER #:
UPDATE VERSION :	FW/SW P/N:	

! PARAMETER	! MIN	! NOM	! MAX	! UNITS	! ACTUAL
! VCC - VERIFY LEVEL SUPPLY VOLTAGE	! 5.25	! 5.5	! 5.75	! V	!
! VIH - HIGH LEVEL INPUT VOLTAGE	! 2.4	!	! 5.5	! V	!
! VIL - LOW LEVEL INPUT VOLTAGE	!	!	! 0.5	! V	!
! VIHh - PROGRAM-PULSE VOLTAGE (PO PINS)	! 10.25	! 10.5	! 10.75	! V	!
! VIHh - PROGRAM-PULSE VOLTAGE (PGM ENA)	! 10.25	! 10.5	! 10.75	! V	!
! VIHh - PROGRAM-PULSE VOLTAGE (PI,PA)	! 10.25	! 10.5	! 10.75	! V	!
! VIHh - PROGRAM-PULSE VOLTAGE (VCC)	! 9.5	! 9.75	! 10.00	! V	!
! tw1 - PROGRAM PULSE WIDTH AT VCC	! 10	!	! 50	! us	!
! tw2 - PGM VERIFY PULSE WIDTH	! 100	!	!	! ns	!
! t _{su} - SET UP TIME (/OE-PO)	! 100	!	!	! ns	!
! t _{su} - SET UP TIME (PO-VCC)	! 100	!	!	! ns	!
! t _h - HOLD TIME (/OE-PO)	! 100	!	!	! ns	!
! t _h - HOLD TIME (PO-VCC)	! 100	!	!	! ns	!
! t _{d1} - DELAY TIME (SEE WAVEFORMS)	! 100	!	!	! ns	!

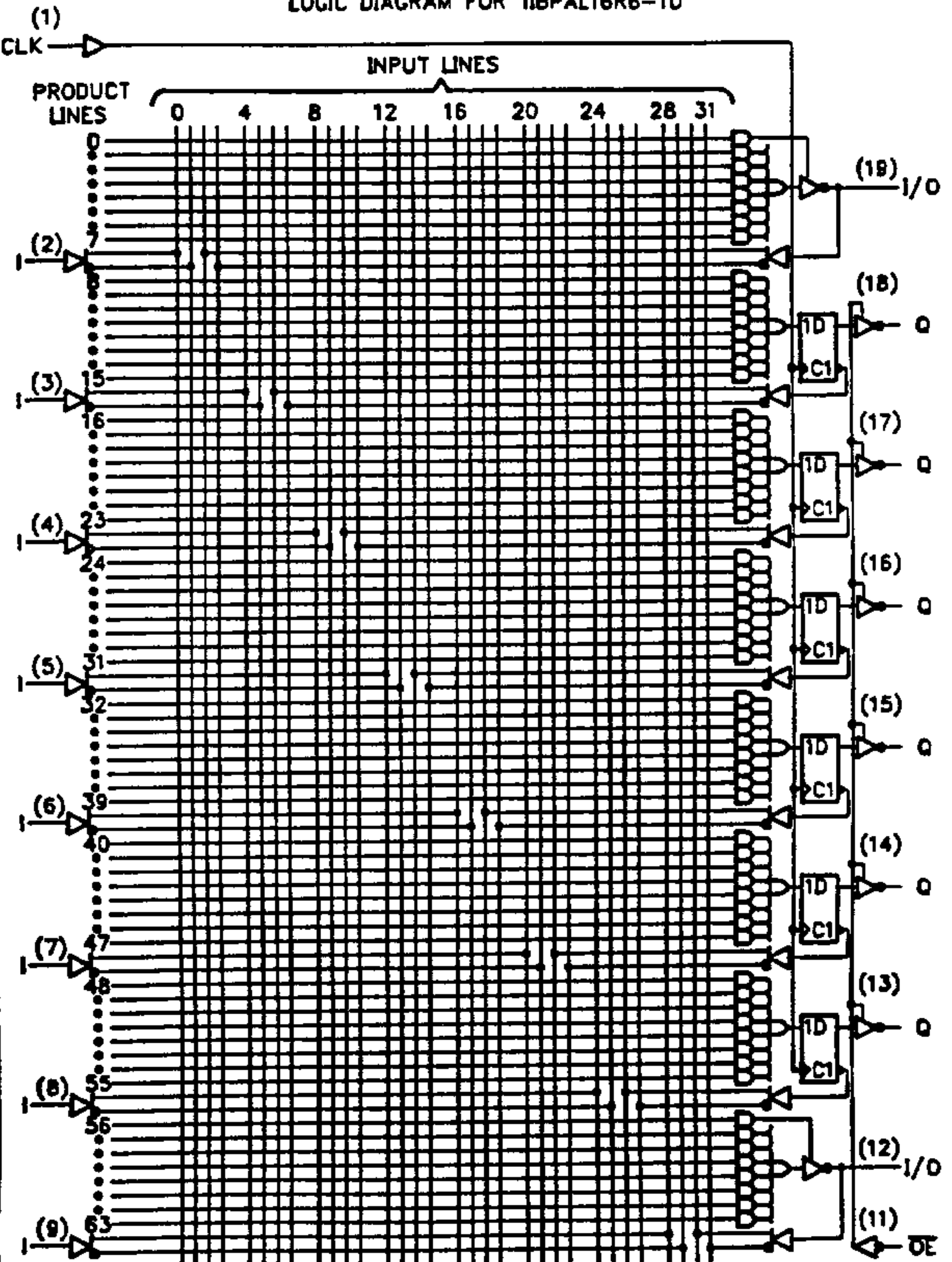
LOGIC DIAGRAM FOR TIBPAL16LB-10



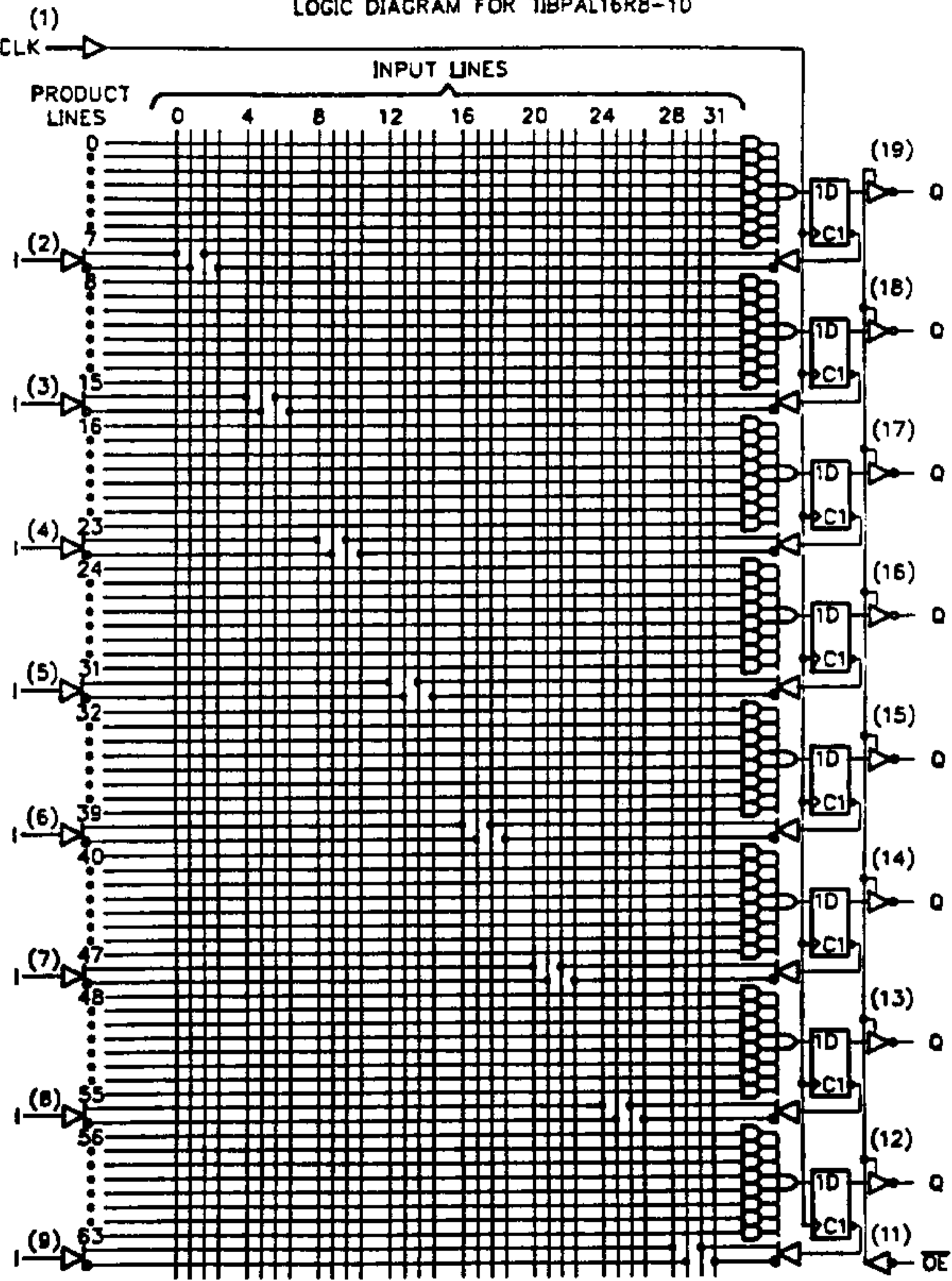
LOGIC DIAGRAM FOR TIBPAL16R4-10



LOGIC DIAGRAM FOR T1BPAL16R6-10



LOGIC DIAGRAM FOR TIBPAL16R8-10



REVISION HISTORY

REVISION LTR.	DATE	ENGINEER	DESCRIPTION OF CHANGES
A	06-87	Thomas	Sheet 1 of 9. Changed Security Fuse Programming Procedure. Table 1-3. Deleted the requirement for PO0 pulse during security fuse programming.
B	12-87	Thomas	Changed V _{CC} to Min = 5.25 V, Nom = 5.50 V, Max = 5.75 V.
C	03-88	Thomas	Added PLCC Pinout. Chg. PO to V _{CC} for t _{w1} . Chg. units from us to ns for t _{w2} . Chg. PI0-PI4 to PI2-PI5 and PA0-PA3 to PA6-PA8, Sht. 4.
D	06-88	Thomas	Sht. 2 - changed t _{d2} units from us to ns