Synertek Cell Library 1984

Cell Library.

Data Book 1984

Synertek.

Cell Library.

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Addendums:

Please note there will be two addendums to this data book featuring the available new cells. Addendum A will be published in July 1984. Addendum B will be published in October, 1984. Use the response card in front of this book to order both.

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Numerical Index

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BAM00001	Inverter/Buffer	1.6K	2.5 C_L + 2	2-3
BAM00002	Inverter/Buffer	3.2K	0.4 C_L + 1	2-3
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BAM00013	5-Input NAND	3.2K	20 C_L + 5	3-8
BAM00020	2-Input NOR	1.6K	10 C_L + 2	4-2
BAM00021	3-Input NOR	2.1K	7 C_L + 1	4-3
BAM00022	4-Input NOR	2.7K	7 C_L + 1	4-4
BAM00023	5-Input NOR	3.7K	7 C_L + 1	4-6
BAM00030	2-Input AND	2.1K	7 C_L + 4	5-2
BAM00031	3-Input AND	2.7K	7 C_L + 4	5-3
BAM00032	4-Input AND	3.2K	7 C_L + 4	5-4
BAM00033	5-Input AND	3.7K	7 C_L + 4	5-6
BAM00040	2-Input OR	2.2K	8 C_L + 6	6-2
BAM00041	3-Input OR	2.7K	9 C_L + 8	6-4
BAM00042	4-Input OR	3.2K	10 C_L + 9	6-6
BAM00043	5-Input OR	4.3K	11 C_L + 9	6-8
BAM00050	Exclusive-OR	2.7K	11 C_L + 2	7-2
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BAM00055	p-channel Pull-up Transistor	1.1K	NA	14-11
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BAM00061	2,1 AND-NOR	2.1K	11 C_L + 2	8-4
BAM00062	2,2 OR-NAND	2.7K	11 C_L + 2	8-6
BAM00063	2,1 OR-NAND	2.1K	11 C_L + 2	8-8
BAM00070	Transmission Gate	2.1K	10 C_L + 2	14-13
BAM00071	Transmission Gate with Enable Inverter	2.1K	10 C_L + 3	14-14
BAM00072	2-to-1 Multiplexer	2.7K	7 C_L + 2	9-2
BAM00073	4-to-1 Multiplexer	2.7K	4 C_L + 2	9-3
BAM00074	8-to-1 Multiplexer	27.3K	3 C_L + 3	9-4
BAM00076	MUX Driver for BAM00072	2.1K	2N + 3	9-5
BAM00077	2-to-4 MUX Decoder/Driver for BAM00073	20.3K	0.7N + 6	9-6
BAM00078	3-to-8 MUX Decoder/Driver for BAM00074	52K	1.5N + 10	9-7
BAM00080	D-Latch without Reset	3.7K	50 MHz	10-2
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BAM00082	D Flip-Flop with Reset	13.9K	50 MHz	10-6
BAM00083	D Flip-Flop with Reset	8.5K	50 MHz	10-6
BAM00084	D Flip-Flop with Set/Reset	9.1K	50 MHz	10-10
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BAM00092	Set/Reset Latch	2.7K	10 C_L + 3	10-26
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BAM00097	D-Latch with 3-State Output and Data Select	22.4K	25 nsec	10-14
BAM00098	D-Latch with 3-State Output and Data Select	12.8K	25 nsec	10-14
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BAM00104	D Flip-Flop with Reset	8.5K	50 nsec	10-17
BAM00105	Binary Adder	16.0K	data sheet	12-6
BAM00200	Power-On-Reset Generator	14.4K	NA	14-8
BAM00210	Resistor Pull-up Load	1.6K	NA	14-9
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BAM00800	V_{SS} PAD	44.3K	NA	11-2
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BAM00810	V_{DD} PAD	44.3K	NA	11-4
BAM00811	V_{DD} PAD	73K	NA	11-5
BAM00820	TTL/CMOS Output Driver	153K	0.84 C_L + 5	11-6
BAM00822	TTL/CMOS Output Driver	76.4K	0.08 C_L + 4	11-8
BAM00823	TTL/CMOS Output Driver	113K	0.08 C_L + 4	11-10
BAM00824	Versatile Output PAD Driver	136K	0.03 C_L + 5.0	11-11
BAM00830	TTL/CMOS 3-State Output Driver	153K	0.04 C_L + 5	11-13
BAM00832	TTL/CMOS 3-State Output Driver	129K	0.04 C_L + 5	11-15
BAM00840	Open-Drain Output Driver	93K	0.04 C_L + 5	11-16
BAM00841	Open-Drain Output Driver	73K	0.05 C_L + 4	11-18
BAM00845	Open-Drain Output Driver — Less Drive	50K	0.5 C_L + 0.7	11-19
BAM00846	Open-Drain Output Driver — Less Drive	73K	0.5 C_L + 0.7	11-20
BAM00850	TTL-Compatible Input Buffer	77K	5 C_L + 3	11-21
BAM00851	TTL-Compatible Input Buffer	73K	5 C_L + 3	11-22
BAM00860	Schmitt Trigger Input Buffer	101K	5 C_L + 3	11-23
BAM00861	Schmitt Trigger Input Buffer	96K	5 C_L + 3	11-25
BAM00870	Fast TTL-Compatible Input Latch	89K	data sheet	11-26
BAM00880	Input PAD with Protection Device	75K	0	11-28
BAM00881	Input PAD with Protection Device	73K	0	11-29
BAM00890	Open-Drain Output with Resistor Pull-up	137K	0	11-30
BAM00891	LED Driver	239K	0.015 (C_L) + 6	11-32
BAM00910	I/O PAD with Open-Drain Output	79K	0.60 C_L + 0.7	11-34
BAM00911	I/O PAD with Open-Drain Output	136K	0.02 C_L + 0.04	11-35
BAM00920	Output Driver PAD for Clock Oscillator	109K	0.2 C_L + 0.7	11-36
BAM00921	Crystal Oscillator with PADs	143K	NA	11-38
BAM00923	Output Driver PAD for Clock Oscillator	126.2K	0.2 C_L + 0.7	11-39
BAM00930	I/O PAD with 3-State Output	185K	0.04 C_L + 6	11-40
BAM00932	I/O PAD with 3-State Output	144.4K	0.04 C_L + 6	11-42
BAM02001	High Speed Inverter/Buffer	1.6K	2.5 (C_L) + 1.5	2-5
BAM02002	High Speed Inverter/Buffer	3.2K	0.4 (C_L) + 1.0	2-6
BAM02003	High Speed Inverter/Buffer	9.1K	0.10 (C_L) + 0.5	2-7
BAM02004	High Speed 3-State Inverter/Buffer	2.1K	3.5 (C_L) + 1.5	2-9
BAM02007	High Speed 3-State Inverter/Buffer	4.3K	3.5 (C_L) + 1.5	2-14
BAM02008	High Speed 3-State Inverter/Buffer	2.1K	3.5 (C_L) + 1.5	2-14
BAM02010	Fast 2 Input NAND (High Speed)	2.1K	2.5 (C_L) + 1	3-3
BAM02011	Fast 3-Input NAND	2.7K	2.5 (C_L) + 1	3-6
BAM02012	Fast 4-Input NAND	5.4K	2 (C_L) + 2	3-7
BAM02013	High Speed 5-Input NAND	TBD	3.0 (C_L) + 1.0	3-9
BAM02014	High Speed 6-Input NAND	4.3K	3.0 (C_L) + 1.0	3-10
BAM02022	High Speed 4-Input NOR	3.2K	1.5 (C_L) + 1.0	4-5
BAM02023	High Speed 5-Input NOR	5.9K	2.0 (C_L) + 2.5	4-7
BAM02032	Fast 4-Input AND	5.9K	2 (C_L) + 2	5-5
BAM02040	Fast 2-Input OR	4.3K	2 (C_L) + 2	6-3

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Cell I.D.	Description	Area (sq. μm)	Propagation Delay or Clock Frequency	Page No.
BAM02041	High Speed 3-Input OR	6.4K	1.5 C_L + 2	6-5
BAM02042	High Speed 4-Input OR	8.0K	1.5 (C_L) + 2	6-7
BAM02060	Fast 2,2 AND-NOR	3.2K	5.0 (C_L) + 1.5	8-3
BAM02061	Fast 2,1 AND-NOR	2.7K	5.0 (C_L) + 1.7	8-5
BAM02062	Fast 2,2 OR-NAND	3.2K	5.0 (C_L) + 1.7	8-7
BAM02063	Fast 2,1 OR-NAND	2.7K	4.7 (C_L) + 1.5	8-9
BAM02080	Fast Transparent D-Latch	5.4K	2 (C_L) + 2.0	10-3
BAM02082	High Speed D-Type Flip-Flop	17.1K	80 MHz	10-8
BAM02083	High Speed D-Type Flip-Flop	11.7K	80 MHz	10-8
BAM02092	High Speed Set/Reset Latch	3.7K	8.0 (C_L) + 3.0	10-25
BAM06010	8 x 8 Static RAM	380K	4 (C_L) + 20	13-2
BAM06140	64 x 4 Static ROM	227K	35 nsec	13-6
BAM06141	64 x 8 Static ROM	278K	35 nsec	13-9
BAM06142	64 x 12 Static ROM	325K	35 nsec	13-12

TTL Cross Reference

TTL Equivalent	Cell Identifier	Function	Comment	Page No.
7400	BAM00010	2-Input NAND		3-2
7400	BAM02010	Fast 2-Input NAND		3-3
7402	BAM00020	2-Input NOR		4-2
7404	BAM00000	Inverter		2-2
7404	BAM00001-3	Inverter/Buffer	Functional Equivalent	2-3
7404	BAM00006	TTL-Compatible Buffer	Functional Equivalent	2-11
7408	BAM00030	2-Input AND		5-2
7410	BAM00011	3-Input NAND		3-4
7410	BAM02011	Fast 3-Input NAND		3-5
7411	BAM00031	3-Input AND		5-3
7420	BAM00012	4-Input NAND		3-6
7421	BAM00032	4-Input AND		5-4
7425	BAM00022	4-Input NOR		4-4
7427	BAM00021	3-Input NOR		4-3
7432	BAM00040	2-Input OR		6-2
7451	BAM00060	2,2 AND-NOR		8-2
7474	BAM00084	D Flip-Flop with Set/Reset		10-10
7483	BAM00105	Binary Adder		12-6
7486	BAM00050	Exclusive-OR		7-2
7496	BAM00093/94	Parallel-Load Shift Register	Cell without Clear	10-27 10-29
74107	BAM00090/91	J-K Flip-Flop with Set/Reset		10-23
74125	BAM00004,7,8	3-State Inverter/Buffer		2-8, 2-12
74138	BAM00078	3-to-8 Line Decoder	Cell without Enable	9-7
74152	BAM00074+78	8-to-1 Multiplexer		9-4
74153	BAM00073+77	4-to-1 Multiplexer	Cell without Strobe	9-3
74155	BAM00077	2-to-4 Line Decoder	Cell without Strobe	9-6
74157	BAM00072+76	2-to-1 Multiplexer	Cell without Strobe	9-2
74163	BAM00099/100	Look-Ahead Carry Counter	Cell without Count Enable	12-2
74193	BAM00101/102	Look-Ahead Up/Down Counter		12-4
74260	BAM00023	5-Input NOR		4-6
74266	BAM00051	Exclusive-NOR		7-3
74279	BAM00092	Set-Reset Latch		10-26
74363	BAM00095/96	Transparent D-Latch with 3-State		10-12
74373	BAM00080	D-Latch without Reset	Cell without 3-State and Enable	10-2
74373	BAM02080	Fast D-Type Flip-Flop	Cell without 3-State and Enable	10-3

CMOS Cross Reference

CMOS Equivalent	Cell Identifier	Function	Comment	Page No.
4001	BAM00020	2-Input NOR		4-2
4002	BAM00022	4-Input NOR		4-4
4008	BAM00105	Binary Adder		12-6
4011	BAM00010	2-Input NAND		3-2
4011	BAM02010	Fast 2-Input NAND	Functional Equivalent	3-3
4012	BAM00012	4-Input NAND		3-6
4013	BAM00084	D Flip-Flop with Set/Reset		10-10
4020	BAM00086/87	T Flip-Flop with Reset		10-19
4021	BAM00093/94	Parallel-Load Shift Register		10-27
4023	BAM00011	3-Input NAND		3-4
4023	BAM02011	Fast 3-Input NAND	Functional Equivalent	3-5
4025	BAM00021	3-Input NOR		4-3
4027	BAM00090/91	J-K Flip-Flop with Set/Reset		10-23
4029	BAM00101/102	Look-Ahead Up/Down Counter	Cell has only Binary-Count	12-4
4042	BAM00080	D-Latch without Reset	Cell without Clock Polarity Select	10-2
4042	BAM02080	D-Latch, Transparent, HIgh Speed	Cell without Clock Polarity Select	10-3
4044	BAM00092	Set-Reset Latch	Cell without 3-State	10-25
4049	BAM00001-3	Inverter/Buffer		2-3
4049	BAM00006	TTL-Compatible Buffer		2-11
4051	BAM00074+75	8-to-1 Multiplexer	Cell without Inhibit	9-4
4052	BAM00073+77	4-to-1 Multiplexer	Cell without Inhibit	9-3
4053	BAM00072+76	2-to-1 Multiplexer	Cell without Inhibit	9-2
4069	BAM00000	Inverter		2-2
4070	BAM00050	Exclusive-OR		7-2
4071	BAM00040	2-Input OR		6-2
4072	BAM00042	4-Input OR		6-6
4073	BAM00031	3-Input AND		5-3
4075	BAM00041	3-Input OR		6-4
4077	BAM00051	Exclusive-NOR		7-3
4081	BAM00030	2-Input AND		5-2
4082	BAM00032	4-Input AND		5-4
4085	BAM00060	2,2 AND-NOR	Cell without Inhibit	8-2
4502	BAM00004,7,8	3-State Inverter/Buffer	Cell without Inhibit	2-8, 2-12
4555	BAM00077	2-to-4 Line Decoder	Cell without Enable	9-6
40161	BAM00099/100	Look-Ahead Carry Counter		12-2
40174	BAM00082/83	D Flip-Flop with Reset		10-6

I. General Description

The Synertek Cell Library combines the dense layout characteristics of the HCMOS process technology with the automation achieved by standard cell system design. The cells adhere to a well-defined set of design and layout structure rules, thereby relieving the chip designer of the burden of electrical and physical considerations and permitting a focus on system and logic design efforts.

In general, the cells utilize a constant height and a variable width and allow for placement adjacent to each other in the horizontal direction. The structure rules are compatible with standard CAD interactive layout software by including feedthroughs on all inputs and outputs, and by accounting for power connections by cell abutment. Interactive layout systems can utilize the supplied physical outlines for each cell to minimize layout data. In some cases, individual cells may have a non-standard height or may not have feedthroughs for all inputs and outputs in order to achieve a higher level of packing density.

The HCMOS Cell Library incorporates this structured approach to provide fundamental logic functions for high speed, low power applications.

II. Electrical Requirements

A. Absolute Maximum Ratings:

Parameter	Value
Power Supply (V_{DD})	+6 V
Input Voltage	−0.3 V to V_{DD} + 0.3 V
Output Voltage	−0.3 V to V_{DD} + 0.3 V
Temperature	−55 to +150° C

B. Maximum Operating Conditions:

Parameter	Value
Power Supply (V_{DD})	2.0 V to 6.0 V
Input Voltage	0 V to V_{DD}
Output Voltage	0 V to V_{DD}
Temperature	−55 to +125° C

C. Recommended Operating Conditions:

Parameter	Value
Power Supply (V_{DD})	5.0 V ± 10%
Temperature	−55 to +125° C

D. Nominal Conditions:

Parameter	Value
Power Supply (V_{DD})	5.0 V
Temperature	25° C

III. Physical Specifications

A. Cell Height: 69, 139, and 208 μm (with some special exceptions).

B. Cell Width: Increments of 7.7 μm.

C. Power: 5.6 μm metal lines horizontally routed through each cell.

D. Metal Interconnections: 2.8 μm width, 3.5 μm spacing.

E. Polysilicon Interconnections: 2.1 μm width, 2.5 μm spacing.

IV. Electrical Specifications for Individual Cells

A. Propagation Delay

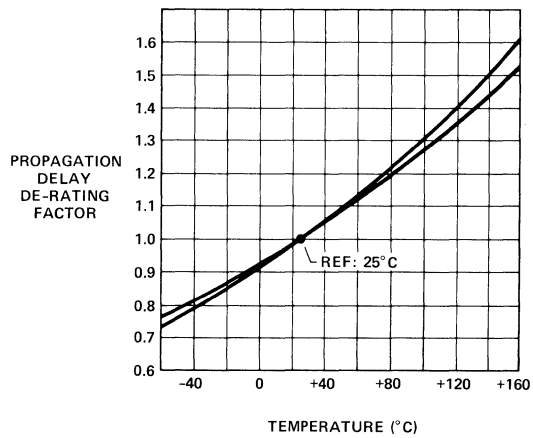
The output propagation delay for each cell is indicated in the individual cell data sheet. Both low-to-high and high-to-low transitions are specified. Delays are consistently measured at the 50% points. Individual cell propagation delays are specified as a function of the cell output load capacitance, C_L, in pF. Further, the equation is valid at nominal conditions, only (V_{DD} = 5.0 V, T = 25° C, nominal process). Actual delays at other than nominal conditions are determined by utilizing derating factors, as shown below:

(t_{PD}) actual = (t_{PD}) nominal • (X_1) • (X_2) • (X_3)

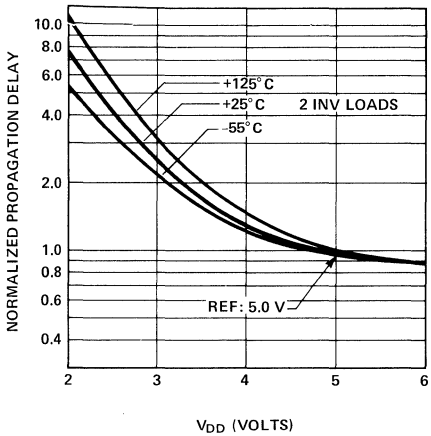
X_1 = derating factor for temperature.
X_2 = derating factor for V_{DD}.
X_3 = derating factor for process variations.

The derating factors for temperature and V_{DD} level are taken from the following curves:

PROPAGATION DELAY DE-RATING FACTOR VS. TEMPERATURE



PROPAGATION DELAY VS. V_{DD}



The derating factor for process variation is taken from the following table:

Process	Derating Factor
Worst Cast	1.50
Nominal	1.00
Best Case	0.65

B. Power Dissipation

There are two components of power dissipation in the HCMOS Cell Library cells. The first component is the static or DC power and consists of three effects:

- Internal leakage paths between V_{DD} and V_{SS}. In most cases, the currents are less than 1 nA, but sometimes they can be as high as 1 μA.
- Output loads. Output loads (resistive elements with a current path to ground) require substantial currents when they are driven.
- TTL input level effects. Inputs to the TTL-compatible Input Buffer cell may cause significant power drain. This results from both the pull-up and the pull-down devices being simultaneously conducting when an input level below V_{DD} and above V_{SS} is applied. The data sheet for this cell shows this effect quantitatively.

The second component of power dissipation is the transient or AC power and consists of three parts:

- Internal capacitance charging. Whenever internal levels change state from low to high levels, energy is required to charge the node capacitance. This occurs only at the time of transition and is a function of the amount of node capacitance and the V_{DD} level.
- Output load capacitance. When external levels change state from low to high, energy is also required for charging. In this case, however, node capacitance is typically orders of magnitude higher than internal nodes and consequently, power dissipation effects can be quite substantial.
- Transitional push/pull currents. Internal cells will experience current paths between V_{DD} and V_{SS} when undergoing a high-to-low or low-to-high transition. This occurs for very short periods when both the p-channel and n-channel transistors simultaneously conduct.

The data sheets for each cell indicate the cell power dissipation for internal node capacitance charging and for transitional push/pull currents. Output loads, TTL input level effects, and output load capacitance must be accounted for additionally. Internal leakage paths will not exceed 1 μA in total and hence, can usually be neglected.

Cell data sheets indicate power dissipation at fixed loading (usually 0.050 pF) and at nominal operating conditions. Note that the power is given in units of μW/MHz. In this way, the frequency of edge transitions directly effects power and can be readily calculated.

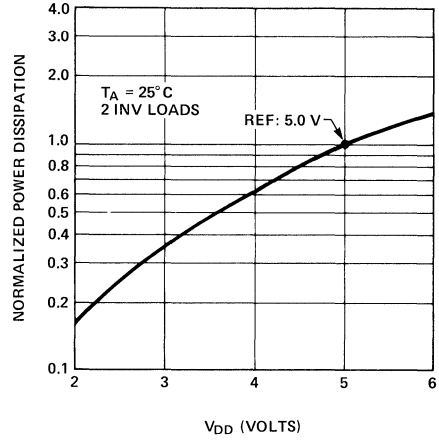
In a like fashion, additional loading (greater than 0.050 pF) increases power dissipation according to the following relation:

$$P_{DISS} = P_{DISS}\ \text{nominal} + 25\ (C_L - 0.050)$$

where,

P_{DISS} nominal = Nominal Power Dissipation (from data sheet)
C_L = Load Capacitance on Node (pF)

POWER DISSIPATION VS. V_{DD}



By this relation, power dissipation at any particular loading condition may be calculated. Further, the effect of V_{DD} on power dissipation needs to be determined for situations that call for V_{DD} levels other than nominal (V_{DD} = 5.0 V). For this, the above curve is used.

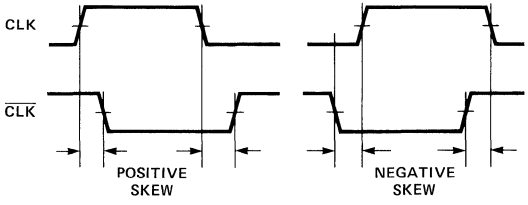
Finally, it should be noted that temperature and process variations have no substantial effects on power dissipation.

C. Other Timings

There are other timing parameters sometimes specified besides propagation delay. Some examples are pulse widths, clock rates, set-up and hold times, and three-state turn-on and turn-off delays. For these parameters, the same derating factors are used as for propagation delays, unless otherwise noted.

D. Clock Skews

Many cells require complementary clock input signals. Some examples are latches, flip-flops, and shift registers. For these cells, some degree of clock skew is permitted, as shown below:



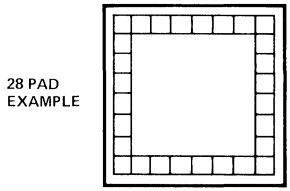
The maximum tolerable clock skew at nominal conditions (V_{DD} = 5.0 V, T = 25°C, nominal process parameters) is ± 10 nsec. Skew effects get worse as V_{DD} goes higher, T goes lower, and as the process parameters increase the speed of the MOS transistors. In short, unless otherwise indicated, maximum tolerable clock skew at the worst-case conditions may not exceed ± 5 nsec. This is not as bad as it seems, however, since clock drivers get faster as the conditions for worst-case skew are approached, a self-compensating situation. Thus, if the nominal condition is met (± 10 nsec), then the worst-case condition will be met as well.

V. Die Size Estimating

The approximate die size may be estimated by following a simple step-by-step procedure, as follows:

1. Pad Layout Analysis

Estimate the minimum possible die size by laying out a simple chip plan with pad cells only. For example, the following sketch shows a pads-only layout for a 28-pad chip.



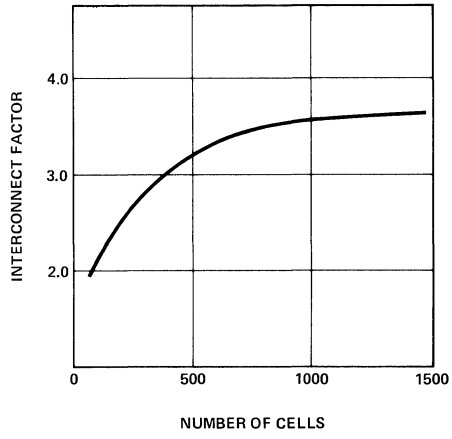
The width of the average pad cell is about 15 mils (400 μm). (If the actual pad cells to be used are known, a more accurate estimate may be obtained with a modest amount of additional effort). Using 15 mils, a side dimension of 8 x 15 = 120 mils results. This is the resultant die size if the useable internal area is enough for the required logic active area, which is to be calculated in the next section.

2. Active Area

The Active area (inside the pads) consists of the area of the cells used and the amount of interconnection area needed. The interconnection area can be thought of as a multiple of the cell area. Although the value of this multiple varies with the application, it is generally about 3.0 to 4.0. In this way, if the cells are itemized and their total area is calculated, then this can be multiplied by the Interconnect Factor to arrive at the total active area. The following expression summarizes this calculation:

Total Active Area	=	Inter-connect Factor	x	Total Cell Area

INTERCONNECT FACTOR VS. NO. OF CELLS



Experience has shown that the Interconnect Factor is larger when more cells are used. As a general guideline, the above graph can be used to derive an approximate value for the Interconnect Factor.

The calculated value of the total active area (in. sq. μm) must be converted to mils sq., as follows:

$$\text{Side Dimension (Mils)} = 0.04 \sqrt{\text{Total Active Area (sq. } \mu\text{m)}}$$

If this active area fits inside the pad layout derived earlier, then the chip is said to be "pad-limited" and the side dimension derived in step 1 is the actual chip dimension. On the other hand, if the active area is too large, then the chip is not pad-limited and the pad periphery must be added to the side dimension of the active area to arrive at the final die size.

Example: Calculate the die size for a circuit utilizing ten 2-input NAND gates, eight 2-input NOR gates, fifteen inverters, five D-type flip-flops, eight inputs, ten outputs, V_{DD}, and V_{SS}.

a. Find area for each cell in data sheet and multiply the area by the number of devices.

Type	Cell Area (sq. μm)		Qty.		Area (sq. μm)
2-input NAND	2.2K	x	10	=	22K
2-input NOR	1.6K	x	8	=	12.8K
Inverter	1.1K	x	15	=	16.5K
D-type Flip-Flop	13.9K	x	5	=	69.5K
					120.8K

b. Calculate Total Active Area

$$\text{Total Active Area} = 2 \times 120.8\text{K} = 241.6\text{K sq. } \mu\text{m}$$

c. Convert Total Active Area to mils

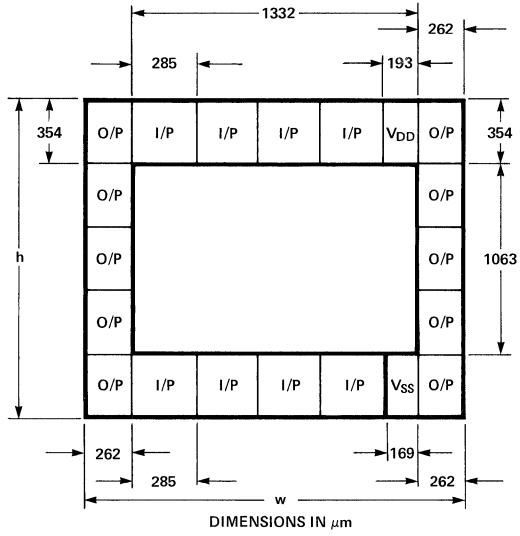
$$\text{Side Dimension (mils)} = 0.04 \sqrt{241.6\text{K sq. } \mu\text{m}} = 19.66 \text{ mils}$$

d. Lay out the pad cells to estimate the minimum possible die size.

The area available in the example is 1063 μm (354 x 3) high and 1332 μm ([258 x 4] + 193) wide, ie., 42.5 mils x 53.28 mils.

Since the active area required for our circuit is smaller (19.66 mils/side) than the smallest dimension inside the pads (42.5 mils), the die size will be 42.5 x 53.28 mils. This is a pad-limited design.

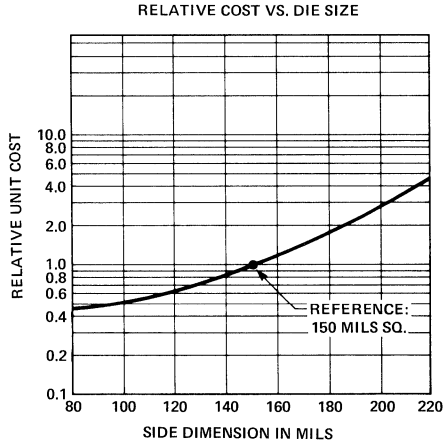
If the active area (including interconnect) were larger than 42.5 mils on either side, the pads would have to be separated to accommodate the larger cell active area, thus increasing the overall size of the die.



DIMENSIONS IN μm

VI. Relative Unit Cost Estimates

From the die size estimate performed previously, it is possible to get formal unit price quotations from Synertek by contacting the appropriate marketing organization. In addition, relative costs may be estimated, based upon the resulting die size estimate. These relative costs can be used to compare the economics of several different partitioning schemes, for example. Although absolute costs and prices cannot be found this way, it is at least possible to evaluate the impact of additional circuitry on the cost of a chip. The following graph illustrates relative unit costs for the case of a 28-lead dual-in-line product versus die size.

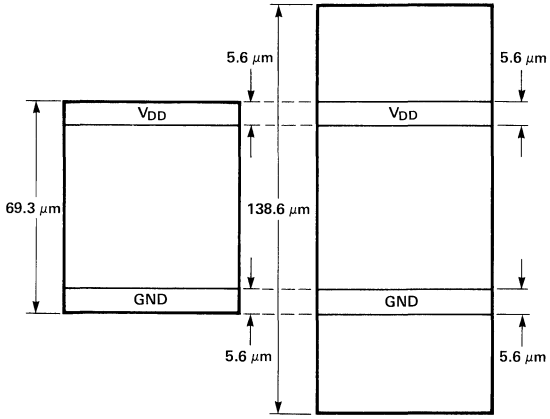


VII. Cell Structures

A. Power and Ground Connections Through Cells

V_{DD} and GND connections are routed through rows of cells by means of cell abutment. Both V_{DD} and GND (V_{SS}) are bussed through the cells in the horizontal direction by 5.6 μm wide metal lines. The following diagram illustrates the bussing for both 69.3 and 138.6 μm high cells.

V_{DD} AND GND ROUTING THROUGH CELLS

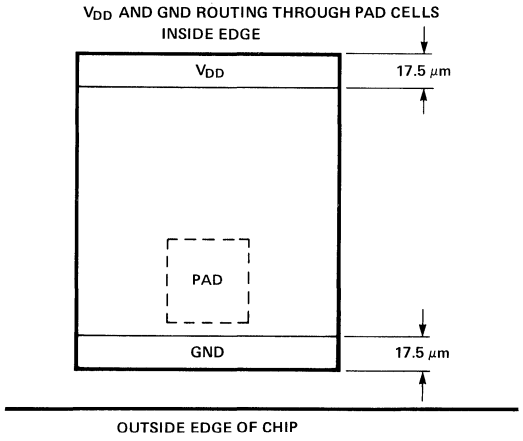


Note that the busses will be routed through a row of cells, even when cell heights are mixed, providing that the cells are centered the same. Connections to V_{DD} and GND can be made at the ends of the cell rows. This may be done either automatically (if the router software is capable) or by manual edits.

B. Power and Ground Connections in Pad Cells

The same principle applies for pad cells as for internal cells, as diagrammed below.

V_{DD} AND GND ROUTING THROUGH PAD CELLS

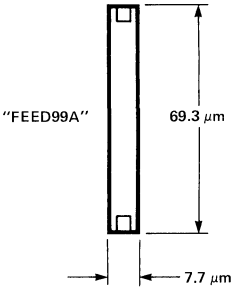


Connections between adjacent cells for V_{DD} and GND are made by means of cell abutment. However, one difference exists for pad cells. That difference is that pad cells with different heights still have V_{DD} and GND busses on the top and bottom of the cell. This means that, if cells of different heights are used, a gap must be provided between the cells and the V_{DD} and GND busses must be entered manually. In addition, the V_{DD} and GND busses have standard widths of 17.5 μm (5.6 μm is the bus width for internal cells).

C. Feedthrough Cell

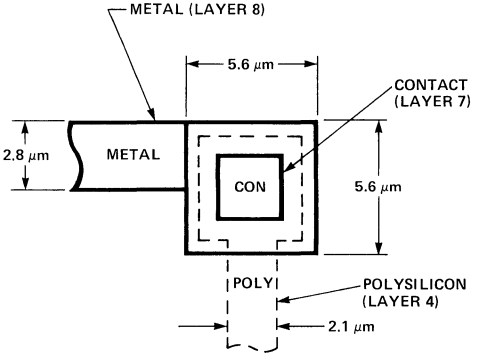
A feedthrough cell is required by most router software packages to permit routing a connection through a row of contiguous cells to some point beyond. To achieve this, a feedthrough cell is used, whose outline drawing is shown below.

FEEDTHROUGH CELL



D. Contacts

Connections between metal and polysilicon lines are achieved by means of contacts. The following figure illustrates the required dimensions of the contact.



The polysilicon stripes (lines) are 2.1 microns wide and the metal lines are 2.8 microns wide. The size of both the metal and polysilicon contact coverage is 5.6 x 5.6 microns. The contact opening is 2.8 x 2.8 microns. The layer numbers are indicated on the figure.

Systems Engineers into I.C. Designers

I. Introduction

Much has been said about the economics of standard cell design methodologies. Clearly, there is an economic niche for standard cell ICs between the gate array and the full custom approaches.

A more significant point, however, is that standard cell design techniques very closely resemble those used by system designers and this resemblance permits a dramatic change in the nature of future IC design. It is intended to point out the similarities between standard cell IC design technologies and conventional system design technologies by discussing the standard cell design process.

II. Standard Cell Design Concept

The basic concept of standard cell IC design is centered around the use of pre-designed circuit elements (or cells). These cells are generally very basic logic function cells and have been carefully designed to be as compact as possible. Further, complete characterization ensures that the electrical characteristics of each cell are well defined and fully documented. The design of a chip, then, is reduced to the selection of the desired cells to be used and the necessary physical layout and interconnection to achieve the chip realization of the circuit. In this way, the chip design activity closely resembles the procedure used to design and layout a conventional printed circuit board.

III. Reasons for the Evolution of Standard Cell Design

The observer may naturally wonder why standard cell IC design has suddenly become such a useful methodology. Although it hasn't happened overnight, it certainly seems as though standard cell methods have been only a recent development. In fact, standard cell techniques have been in use for over 10 years, although the refinements of the last 2-3 years have really made the methodology of far greater usefulness.

The first reason for the recent popularity of standard cell IC design methodology has been the maturity of CMOS process technology. Although standard cell techniques are fundamentally process-independent, they are far easier to apply to CMOS than to NMOS. The reason is associated with the basic operation of CMOS logic circuits. CMOS logic gates have very high input impedances and consequently do not require significant driving from output stages. In addition to this, the voltage levels of CMOS internal signals are typically rail-to-rail; that is, they swing from GND to V_{DD} levels and intermediate levels are not encountered. The result of these two factors is that CMOS cells are very easy to design with. It is not necessary to account for loading effects, except for the way they impact operating speeds of the circuits. With other process technologies, it is necessary to consider DC limitations of fanout and loading effects on logic levels.

CMOS technology also offers advantages in the area of greatly reduced power dissipation. However, the reason that this is an important issue is not always understood. Although it is pretty obvious that reduced power consumption in electronic systems is a good thing, a second, more important issue is less obvious. This issue arises as a result of the tremendous advances in the circuit densities of modern ICs. When thousands and even tens of thousands of gates are put on a single silicon substrate, the power dissipation quickly becomes prohibitive for even the most sophisticated NMOS or Bipolar processes. With CMOS, on the other hand, there is no real problem with this. In effect, the number of gates that can be realistically put onto a single chip is limited by power considerations for NMOS and Bipolar technologies, but this limit is pushed out much further with CMOS and this permits continued advances in chip packing densities.

Not to be overlooked as an important and necessary reason for the recent blooming of standard cell design methodology, is the continued advance of CAD tools, without which it would be extremely difficult to perform the physical layout of ICs. Although it is possible to manually arrange the placement of standard cells on a physical plane and to interconnect them, this would offer only marginally economic benefits. With modern software tools, it is possible to perform completely automatic cell placement and connection routing with little or no manual design effort. The automatic layout of ICs is only one area where CAD tools have had an impact. Another area is the availability of simulation software, that allows accurate testing of designs (both for logic function and for operating speeds) prior to actual silicon implementation. Test generation is another design aid that has benefited from new CAD developments, although fully automatic test generation still is some time away.

There are other reasons, as well, that standard cell IC design has suddenly burst upon the scene, but it is hard to compare them in significance with the inherent advantages of CMOS and the coming of age of CAD tools.

IV. Logic Design with Standard Cells

Performing the basic logic design of an electronic system with standard cells is very similar to designing with SSI/MSI logic blocks. This is perhaps best demonstrated by starting with a brief look at what standard cell documentation looks like. Figure 1 illustrates a typical data sheet for a Synertek standard cell (from the Cell Library). The data sheet shown is for a simple 3-input NOR gate. It should be immediately noticed that

the data sheet bears a rather close resemblance to a typical TTL or 4000 series CMOS data sheet. This is no accident, but is purposely done in order to make it easy for system designers to use the Cell Library.

The basic function of the cell is described in the data sheet, as well as its operating characteristics. All the information needed by the designer is available from the data sheet. Propagation delays, power dissipation, input load capacitance, and physical size are all tabulated. The data sheet is the basic reference for the logic designer.

V. The Synertek Cell Library

The Synertek Cell Library currently contains approximately 150 cells. These consist of gates, inverters, multiplexers, flip-flops, shift registers, counters, adders, I/O circuits (pad cells), and even some LSI type functions, such as RAMs, ROMs, and PLAs. Furthermore, some basic analog functions are provided to permit direct interfacing to analog signal environments (OP AMPs, Comparators, etc.) Finally, a complete set of high-speed cells is also available for those applications that need faster operation (at the expense of somewhat larger cells). With this library of cells to select from, nearly any conceivable circuit may be constructed and designed in a very quick and low cost fashion.

Future enhancements and expansions of the Cell Library illustrate the Synertek commitment to this design methodology. Advanced cells will be added, like microprocessor cores (6502), microprocessor peripheral control functions (UART, Timers), and more analog cells (D/A).

VI. CAD Tools for Standard Cell Designs

Although the logic design phase of standard cell IC design closely resembles the logic design of full systems, the extensive use of CAD software and hardware tools is quite different. At first this sounds like it might be a big catch to the whole process, but actually the design tools are quite simple to use and very effective in their operation.

The Synertek philosophy toward the use of CAD is straightforward and consists of a uniform approach to the use of commercially available tools. No major software or hardware is developed by Synertek. Rather, all necessary items are purchased for use by Synertek. In this way, no particular dependence toward any given approach results, since it is very easy to change the particular software/hardware if a better version is developed. Of more importance, especially to the independent systems designer who is designing ICs with the Synertek Cell Library, there is no dependence on Synertek with this approach. If Synertek were to abandon the standard cell business, for example, the user of the Cell Library is not left stranded, but can still get full support for the CAD tools directly from the supplier. In addition to this, any designs with the Cell Library will be manufacturable by any number of IC producers, since the process design rules are fairly standard and will become even more so as time progresses.

VII. Synertek CAD Hardware

The Synertek CAD hardware facilities are not the only possible configuration, but serve to demonstrate at least one approach. Synertek is equipped with several DEC VAX 11/780 series of super-minicomputers. Schematic capture and automatic cell placement and routing is performed with the use of GENISCO black and white graphics terminals. Tektronix color terminals are also used, but the additional value of color in standard cell designs is not a significant feature. An independent system designer could use a hardware configuration like this, but in many cases, this might be more than is affordable. In that case, Synertek often recommends to its customers to use some commercially available engineering workstations.

The details of the individual cell layouts are kept on Synertek's CALMA graphic design systems (GDS-II). These systems are used to perform the final operations on the chip designs. This consists of inserting the complete cells into the partial layout generated by the place and route system, performing design layout checks (DRCs ERCs and NCCs), and adding some necessary manufacturing marks to the finished layout.

VIII. Synertek CAD Software

The Synertek software tools are centered around the basic software package offered by Silvar-Lisco for standard cell design, the SDS schematic capture programs and the CAL-MP automatic place and route software. In addition to these (and their associated interface programs), Synertek uses the HILO logic simulator (offered by GENRAD) and SPICE for circuit simulation. Design rule checking is done with Phoenix Data Systems programs for DRC, ERC, and NCC checks.

IX. Design Procedure

The typical design steps of a standard cell approach are outlined here. Speed and simplicity of design are achieved by the use of state-of-the-art tools.

The first step in the design is to partition the logic into manageable units. In the case of standard cell IC design, this is required to ensure that packaging constraints are met. For example, common dual-in-line packages have 18, 22, 24, 40, or 48 pins. Thus, the number of inputs and outputs for a circuit is constrained. If the packaging of the IC is not a problem, the next step can be taken.

The second step in the design is to convert any peculiar system logic implementations into equivalent standard cell logic. This usually consists of building equivalent functions for MSI logic blocks out of cells available in the library.

Next, the complete schematic is entered into the system. For the case of Synertek, this means using the Silvar-Lisco Schematic Capture software package to load the logic network. In addition to this, several post-processing programs need to be run to flatten the hierarchical schematic and to extract a cell connection netlist in preparation for automatic chip layout.

At this point in the design sequence, optional testing of the design may be undertaken. This consists of logic simulation to verify that the system functions properly and to generate test patterns to be used later, as well as circuit simulation to determine the speed performance of the chip, if necessary. These jobs are not always required, depending upon the level of experience of the individual designer and the nature of the design. For instance, designs that operate at slow clock rates, well within the range of the cells to be used, do not need circuit simulation tests.

When the logic entry portion of the design has been checked by the simulations outlined above, the layout of the chip may begin. The first step to be taken here is to determine the placements of the pad connections for the chip. Often, in the case of chips with relatively low gate counts (say, less than 500), pad limited layouts may result. In these cases, the chip size is determined by the pad arrangement and not by the internal connections of the cells.

Once the pads are placed, this placement can be entered as a layout constraint for the automatic Place and Route software. When this software is run, the cell connection netlist is used to place the cells and to route the interconnections automatically. It is possible for the designer to do some simple interactive controlling of the cell placements to optimize the resulting layout for size (and ultimately, manufacturing cost).

The final placement is the end result of the logic designer's job. From there on, the tooling (masks) are generated by CAD operators (on CALMA equipment at Synertek) and tooling suppliers (vendors to Synertek). Prototype wafer runs are made and sample packages assembled for evaluation by the logic designer.

X. Summary and Conclusions

In summary, the design steps undertaken by the chip designer require little or no IC expertise. The major effort is focused on the actual logic design and simulation. The design steps are well automated and require only a short period of training before the engineer can start his design program.

Standard cell design methodology greatly simplifies the task of converting system logic into an IC. The use of the Synertek Cell Library, combined with modern CAD tools, creates a systematic chip design approach that is easily performed by system design technologists. The future promises that this methodology will result in a proliferation of IC applications in many systems previously not practical.

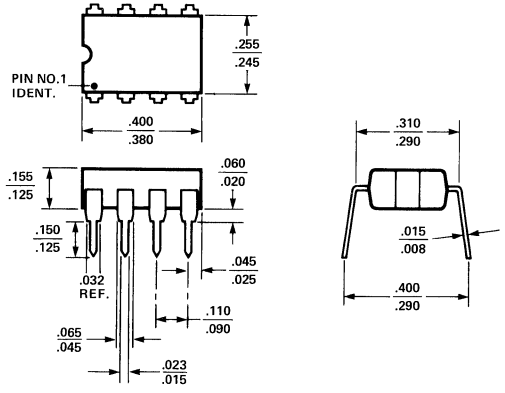
Packaging Information

Maximum Die Size for Given Pin Count and Package Type

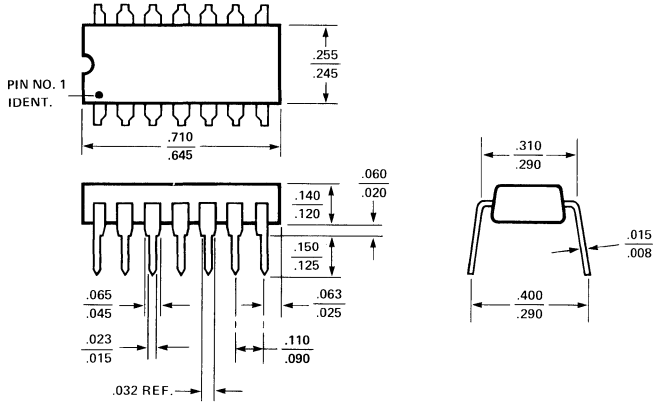
Number of Pins	Plastic	Cerdip	Ceramic
8	0.140 x 0.200	—	0.135 x 0.180
14	0.130 x 0.210	—	0.135 x 0.220
16	0.130 x 0.210	0.120 x 0.210	0.135 x 0.200
18	0.140 x 0.230	0.130 x 0.280	0.134 x 0.225
20	0.140 x 0.210	—	0.135 x 0.220
22	0.200 x 0.210	—	0.180 x 0.210
24	0.230 x 0.250	0.210 x 0.210	0.270 x 0.270
28	0.240 x 0.240	0.225 x 0.275	0.260 x 0.260
40	0.280 x 0.280	0.250 x 0.325	0.270 x 0.270
48	0.330 x 0.330	—	0.310 x 0.310
64	0.300 x 0.300	—	0.360 x 0.360

All dimensions in inches.

Plastic Dual In-Line — 8 Leads

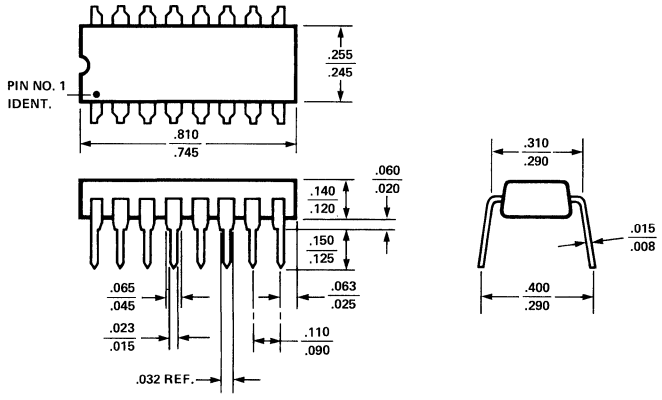


Plastic Dual In-Line — 14 Leads

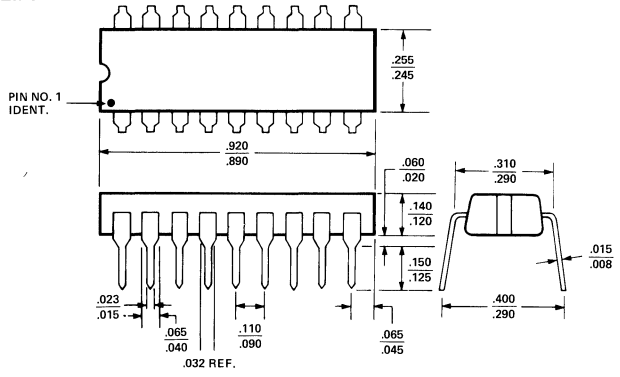


Packaging Information

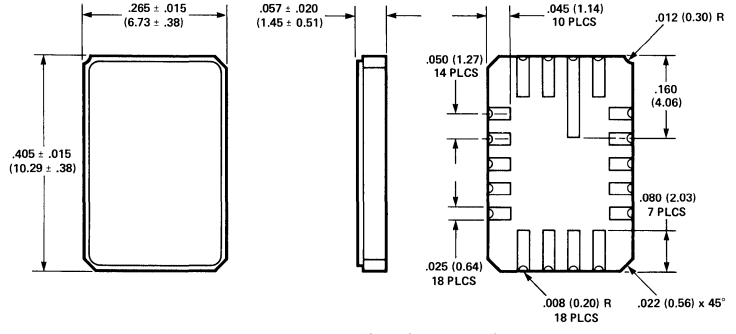
Plastic Dual In-Line— 16 Leads



Plastic Dual In-Line— 18 Leads



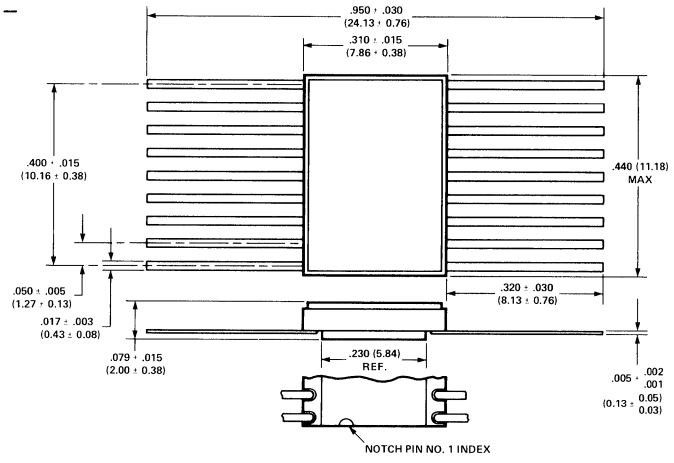
Chip Carrier — 18 Leads



DIMENSIONS IN INCHES AND (MILLIMETERS).

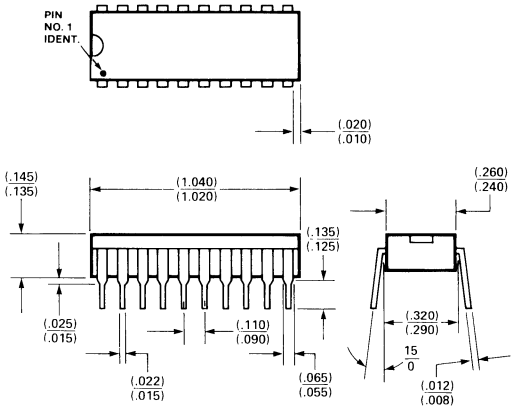
Packaging Information

Flat Package — 18 Leads

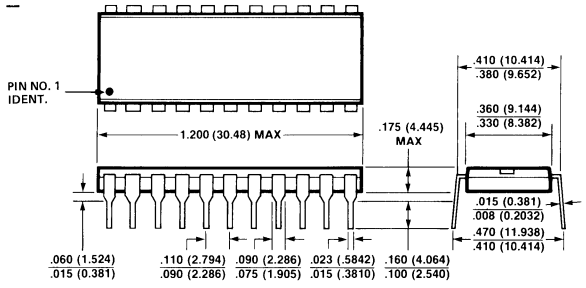


DIMENSIONS IN INCHES AND (MILLIMETERS).

Plastic Dual In-Line— 20 Leads

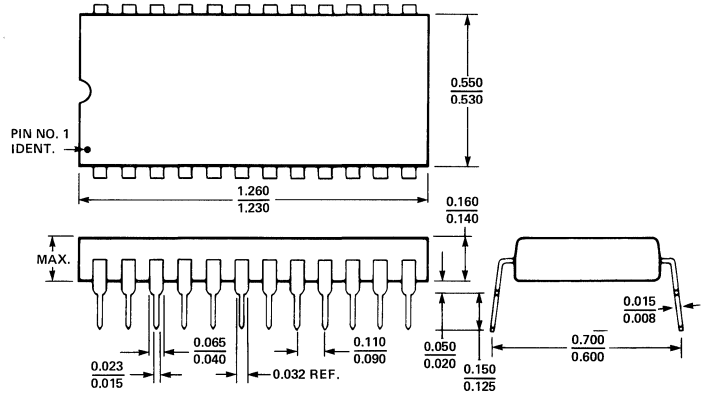


Plastic Dual In-Line — 22 Leads

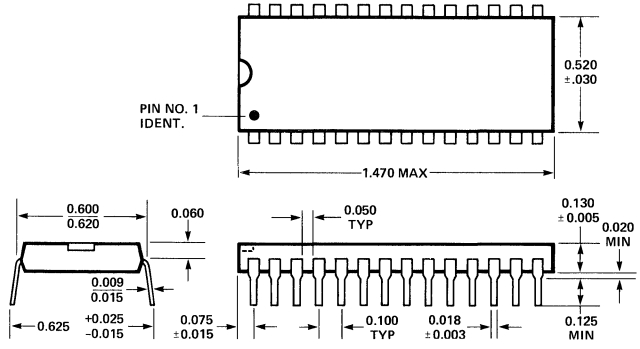


Packaging Information

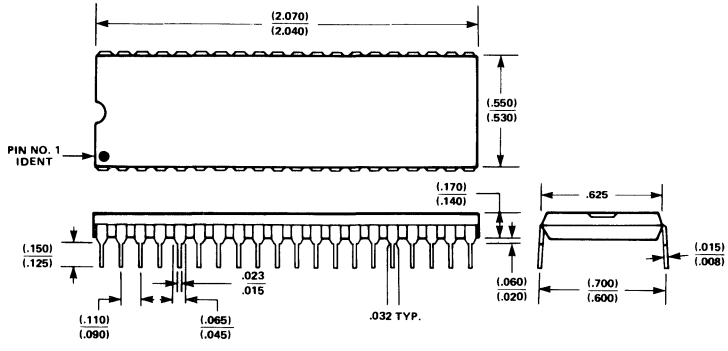
Plastic Dual In-Line — 24 Leads



Plastic Dual In-Line — 28 Leads

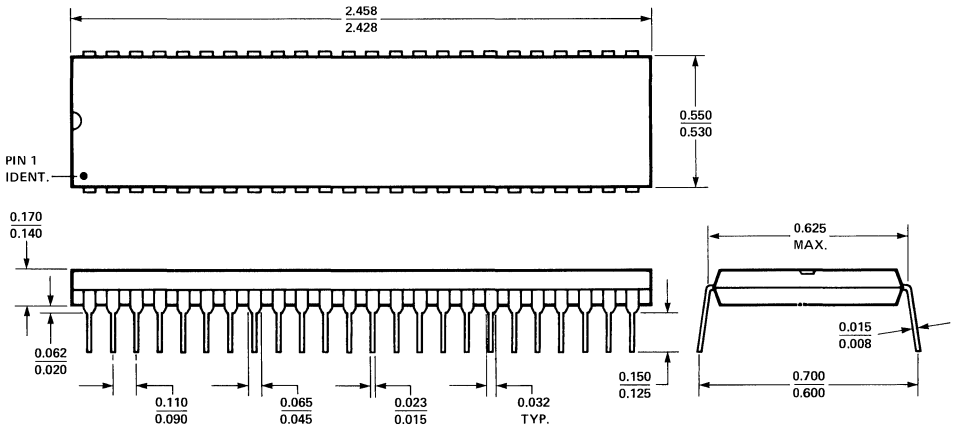


Plastic Dual In-Line — 40 Leads

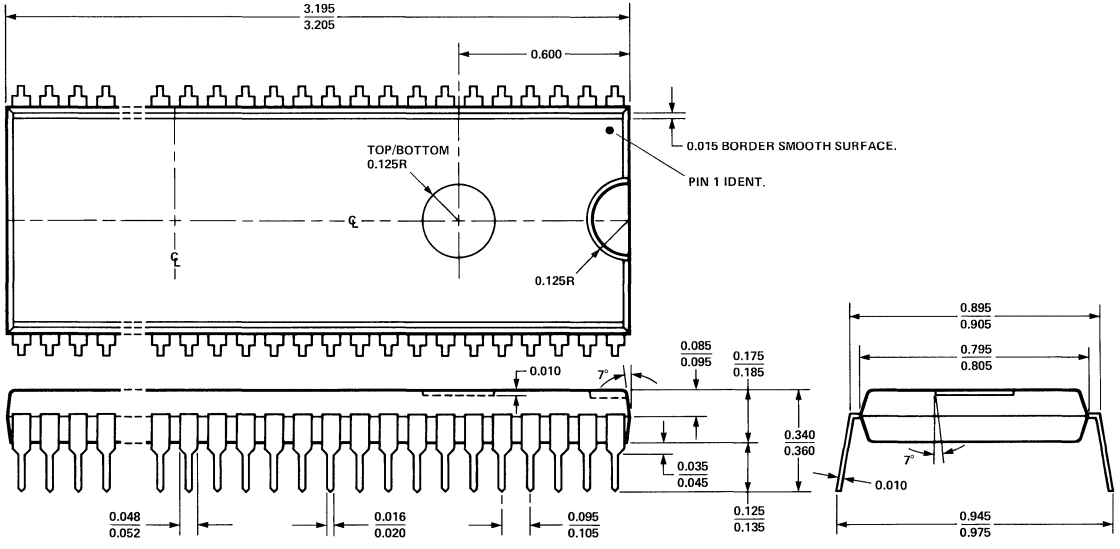


Packaging Information

Plastic Dual In-Line —
48 Leads



Plastic Dual In-Line —
64 Leads



Inverters/ Inverting Buffers

2

Synertek.

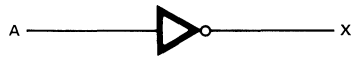
Inverter

BAM00000

Description

The BAM00000 is an HCMOS cell that performs the function of a standard logic inverter.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	15.4	μm
Cell Height	69.3	μm
Cell Area	1.1K	Sq. μm
Average Power Dissipation*	3.0	μW/MHz
Input Capacitance	0.040	pF

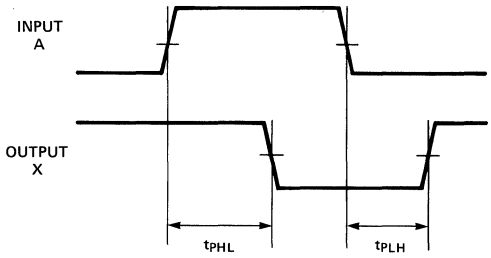
*V_{DD} = 5.0V, T_A = 25° C, CL = 0.050 pF.

Function Table

Inputs	Output
A	X
H	L
L	H

H = High level.
L = Low level.

Dynamic Characteristics



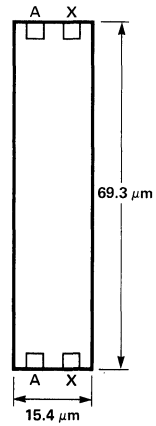
Propagation Delays (in nsec):

$t_{PHL} = 7 (C_L) + 1$

$t_{PLH} = 30 (C_L) + 3.5$

(C_L in pF)

Outline Drawing



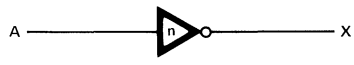
Inverting Buffers

BAM00001/BAM00002/BAM00003

Description

The BAM00001, BAM00002, and BAM00003 are HCMOS cells used for high output drive applications. Typical uses are for data bus drivers and internal clock buffers.

Logic Symbol



n	Cell I.D.
2	BAM00001
3	BAM00002
4	BAM00003

Function Table

Input A	Output X
H	L
L	H

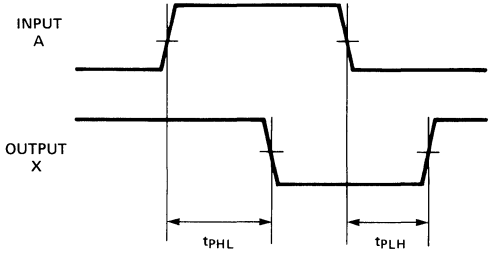
H = High level.
L = Low level.

Cell Parameters

Parameter	BAM00001	BAM00002	BAM00003	Unit
Cell Width	23.1	46.2	130.9	μm
Cell Height	69.3	69.3	69.3	μm
Cell Area	1.6K	3.2K	9.1K	sq. μm
Average Power Dissipation*	8	40	375	μW/MHz
Input Capacitance	0.120	0.550	2.50	pF

*V_{DD} = 5.0 V, T_A = 25° C, C_L in pF.

Dynamic Characteristics



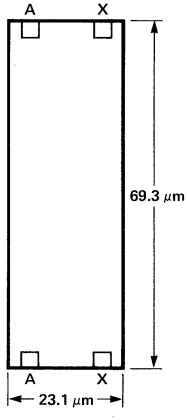
Propagation Delays (in nsec):

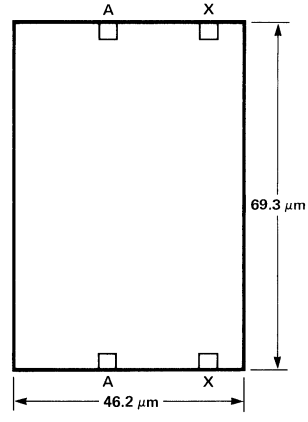
BAM00001
$t_{PHL} = 2.5 (C_L) + 2$
$t_{PLH} = 2.0 (C_L) + 2$

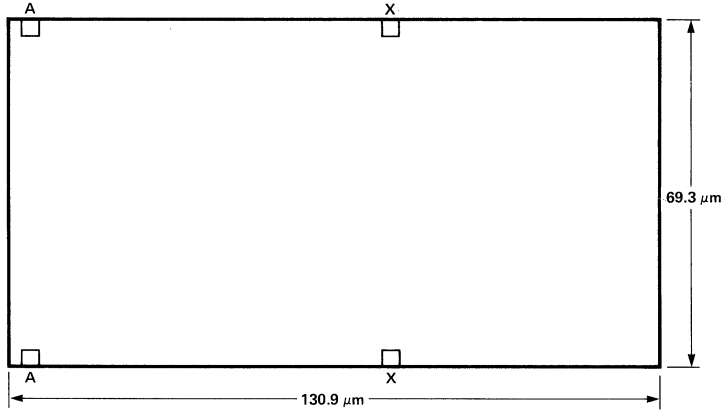
BAM00002
$t_{PHL} = 0.4 (C_L) + 1$
$t_{PLH} = 0.4 (C_L) + 1$

BAM00003
$t_{PHL} = 0.1 (C_L) + 0.5$
$t_{PLH} = 0.1 (C_L) + 0.5$

Outline Drawings







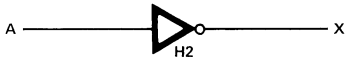
High Speed Inverter/Buffer

BAM02001

Description

The BAM02001 is a high speed inverter buffer which is used for general logic functions, as well as for clock drive.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	23.1	μm
Cell Height	69.3	μm
Cell Area	1.6K	Sq. μm
Average Power Dissipation*	8	μW/MHz
Input Capacitance	0.120	pF

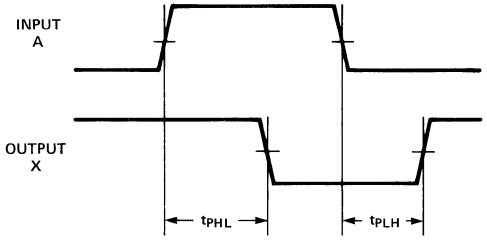
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Input A	Output X
H	L
L	H

H = High level.
L = Low level.

Dynamic Characteristics



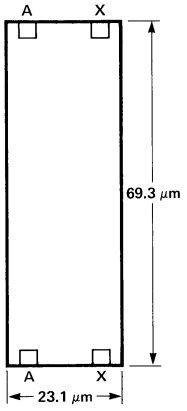
Propagation Delays (in nsec):

$t_{PHL} = 2.5\ (C_L) + 1.5$

$t_{PLH} = 2.0\ (C_L) + 1.5$

(C_L in pF)

Outline Drawing



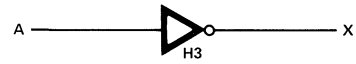
High Speed Inverter/Buffer

BAM02002

Description

The BAM02002 is a high speed inverter buffer which is used for general logic functions, as well as for clock drive.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	46.2	μm
Cell Height	69.3	μm
Cell Area	3.2K	Sq. μm
Average Power Dissipation*	40	μW/MHz
Input Capacitance	0.550	pF

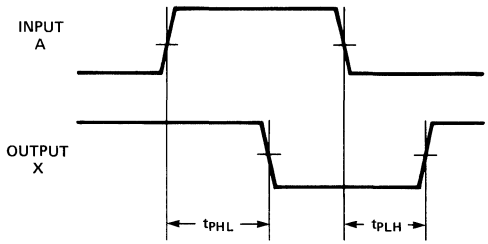
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Input A	Output X
H	L
L	H

H = High level.
L = Low level.

Dynamic Characteristics



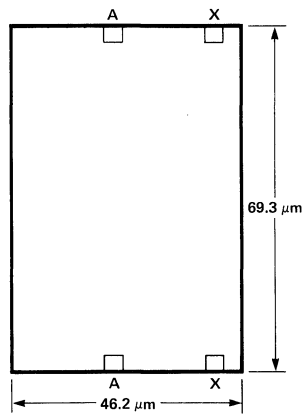
Propagation Delays (in nsec):

$t_{PHL} = 0.4\ (C_L) + 1.0$

$t_{PLH} = 0.4\ (C_L) + 1.0$

(C_L in pF)

Outline Drawing



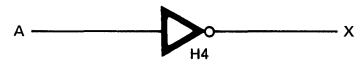
High Speed Inverter/Buffer

BAM02003

Description

The BAM02003 is a high speed inverter buffer which is used for general logic functions, as well as for clock drive.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	131	μm
Cell Height	69.3	μm
Cell Area	9.1K	Sq. μm
Average Power Dissipation*	375	μW/MHz
Input Capacitance	2.50	pF

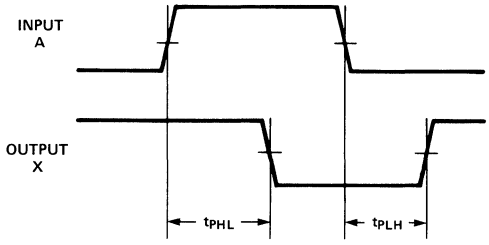
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Input A	Output X
H	L
L	H

H = High Level
L = Low Level

Dynamic Characteristics



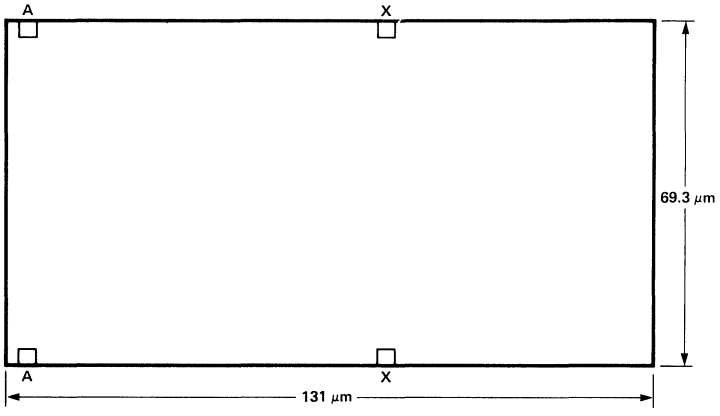
Propagation Delay (in nsec):

$t_{PHL} = 0.10\ (C_L) + 0.5$

$t_{PLH} = 0.10\ (C_L) + 0.5$

(C_L in pF)

Outline Drawing



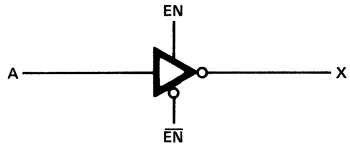
High Speed Three-State Inverter/Buffer

BAM00004

Description

The BAM00004 is an HCMOS cell that is used as a three-state driver for internal bus-connected circuits. When the output stage is enabled, the cell functions as a push/pull inverter. When disabled, the output is de-activated to its high impedance state.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	Sq. μm
Average Power Dissipation*	4.0	μW/MHz
Input Capacitance (A)	0.120	pF
Input Capacitance (EN, $\overline{EN}$)	0.098	pF
Output Capacitance (X)	0.042	pF

*V_{DD} = 5.0V, T_A = 25° C, CL = 0.050 pF.

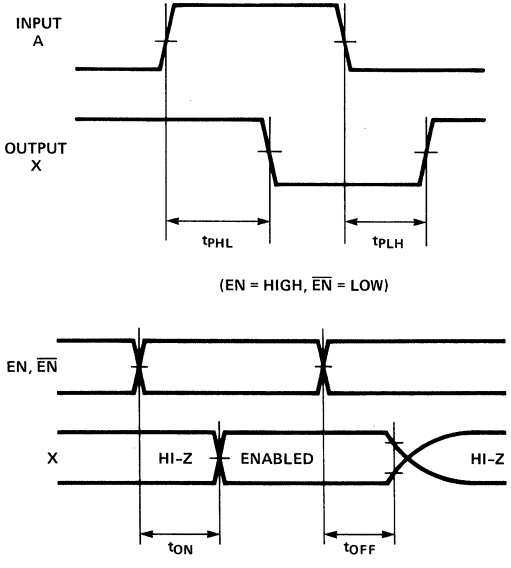
Function Table

Inputs			Output
EN	$\overline{EN}$	A	X
L	H	X	Hi-Z
H	L	H	L
H	L	L	H

H = High level.
L = Low level.
X = "Don't care."

Note: Other combinations are not permitted.

Dynamic Characteristics



Propagation Delays (in nsec):

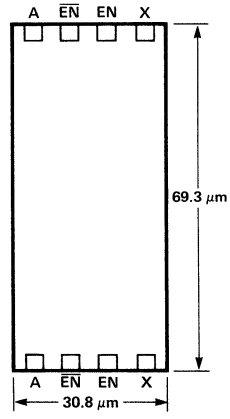
$t_{PHL} = 3.5 (C_L) + 2$

$t_{PLH} = 3.5 (C_L) + 2$

$t_{OFF} = 1.5$

$t_{ON} = 1.5$

Outline Drawing



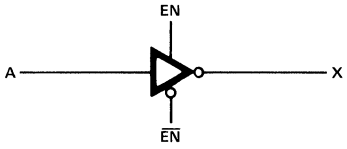
High-Speed Three-State Inverter/Buffer

BAM02004

Description

The BAM02004 is a high-speed three-state bus driver used for internal bus-connected circuits. When the output stage is enabled, the cell functions as a push/pull inverter. When disabled, the output is de-activated to its high impedance state.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	Sq. μm
Average Power Dissipation*	4.0	μW/MHz
Input Capacitance (A)	0.120	pF
Input Capacitance (EN, $\overline{EN}$)	0.098	pF
Output Capacitance (X)	0.042	pF

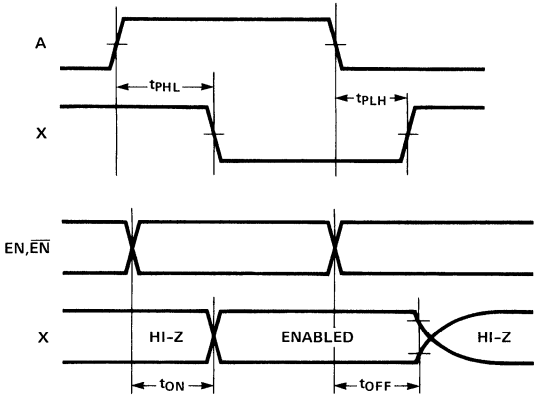
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Output
EN	$\overline{EN}$	A	X
L	H	X	High-Z
H	L	H	L
H	L	L	H

H = High level.
L = Low level.

Dynamic Characteristics



Propagation Delays:

$t_{PHL} = 3.5 (C_L) + 1.5$

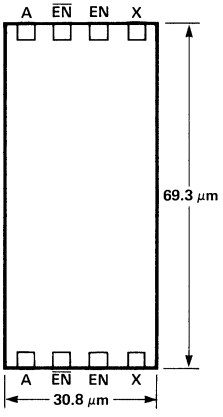
$t_{PLH} = 3.5 (C_L) + 1.5$

$t_{ON} = 1.5$

$t_{OFF} = 1.5$

(C_L) in pF)

Outline Drawing



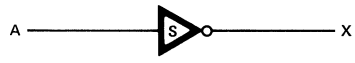
Slow Inverter for Pulse Generation

BAM00005

Description

The BAM00005 is a special inverter cell that has a slow low-to-high output transition. In this way, it is possible to implement rudimentary pulse generator circuits. The typical pulse width which may be achieved is about 1 μsec.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	46.2	μm
Cell Height	69.3	μm
Cell Area	3.2K	Sq. μm
Average Power Dissipation*	8.0	μW/MHz
Input Capacitance	0.280	pF

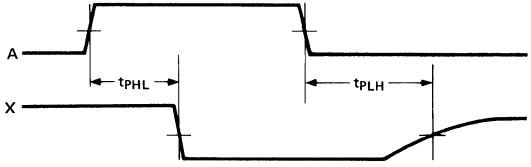
*V_{DD} = 5.0V, T_A = 25° C, CL = 0.050 pF.

Function Table

Inputs	Output
A	X
H	L
L	H

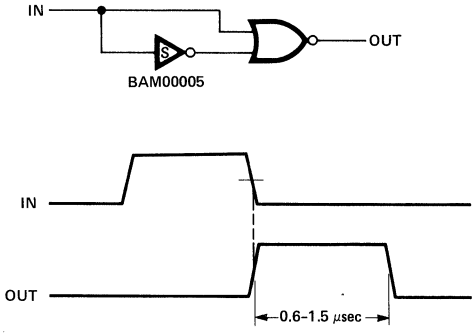
H = High level.
L = Low level.

Dynamic Characteristics

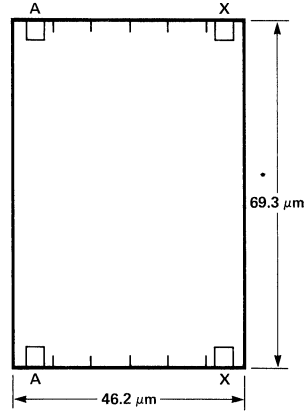


Propagation Delays (in nsec):
$t_{PHL} = 3.5 (C_L) + 3$
$t_{PLH} = 1000 (C_L) + 800$
(C in pF)

Typical Application
(Pulse Generator)



Outline Drawing



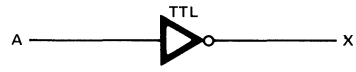
TTL-Compatible Inverter/Buffer

BAM00006

Description

The BAM00006 is an HCMOS cell that functions as a TTL-compatible input buffer. It is not a pad cell, so its use is mainly intended to be with I/O cells having no integral input buffer, such as the BAM00930.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	46.2	μm
Cell Height	69.3	μm
Cell Area	3.2K	Sq. μm
Average Power Dissipation	*	μW/MHz
Input Capacitance	0.550	pF

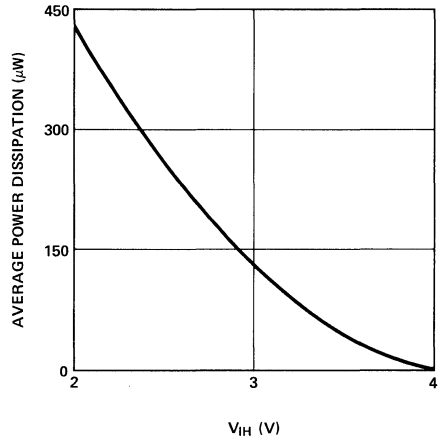
*V_{DD} = 5.0V, T_A = 25° C, 50% duty cycle.

Function Table

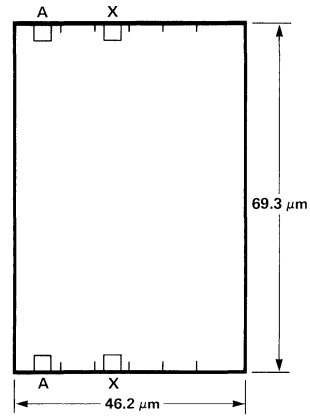
Inputs	Output
A	**X**
H	L
L	H

H = High level.
L = Low level.

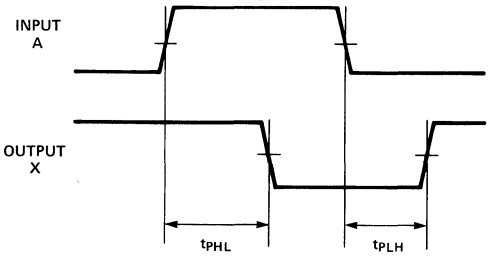
The following graph shows the relationship between input V_{IH} level and power dissipation for the above conditions.



Outline Drawing



Dynamic Characteristics



Propagation Delays (in nsec):

$t_{PHL} = 3.5\ (C_L) + 3$

$t_{PLH} = 3.5\ (C_L) + 2$

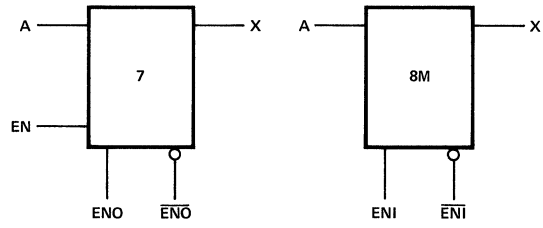
High Speed Three-State Inverter/Buffer

BAM00007/8

Description

The BAM00007/8 are HCMOS cells which are used as three-state drivers for internal bus connections. They are identical to the BAM00004, except that they have a common Enable control. The BAM00007 is the first stage and contains the EN and $\overline{EN}$ circuits. The BAM00008 is a slave stage and uses the EN and $\overline{EN}$ from the BAM00007, routed by means of cell abutment.

Logic Symbols

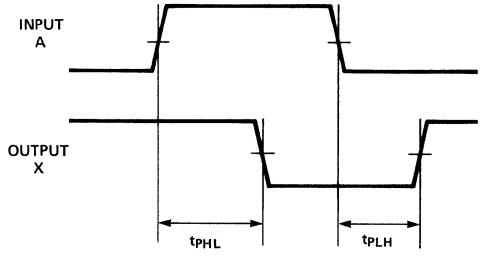


Cell Parameters

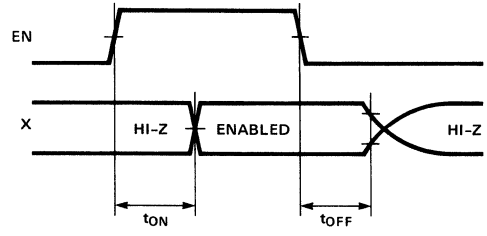
Parameter	BAM00007	BAM00008	Unit
Cell Width	61.6	30.8	μm
Cell Height	69.3	69.3	μm
Cell Area	4.3K	2.1K	Sq. μm
Average Power Dissipation*	2.0	4.0	μW/MHz
Input Capacitance ($\overline{EN}$)	0.220	—	pF
Input Capacitance (A)	0.130	0.130	pF
Output Capacitance (X)	0.042	0.042	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Dynamic Characteristics



(EN = HIGH LEVEL)



Propagation Delays (in nsec):

$t_{PHL} = 3.5\ (C_L) + 2$

$t_{PLH} = 3.5\ (C_L) + 2$

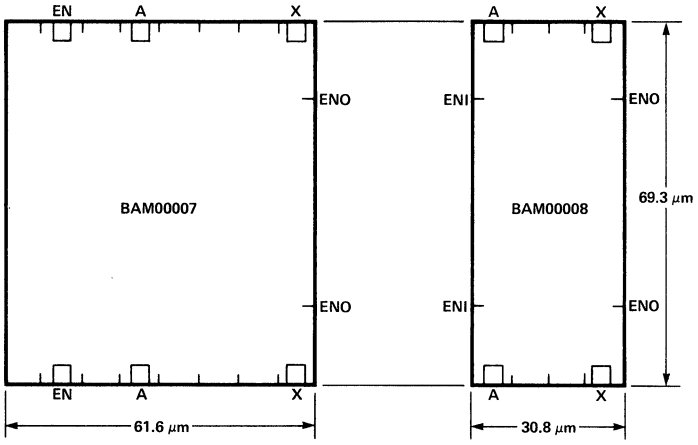
(C_L in pF)

$t_{OFF} = 0.3\ (N_L) + 3$

$t_{ON} = 0.3\ (N_L) + 3$

(N = Number of BAM00008 stages)

Outline Drawings



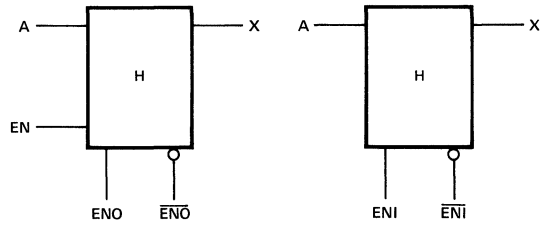
High-Speed Three-State Inverter/Buffer

BAM02007/8

Description

The BAM02007/8 are high-speed three-state drivers and are used for internal bus connections. They are identical to the BAM02004, except that they have a common Enable control. The BAM02007 is the first stage and contains the EN and $\overline{EN}$ circuits. The BAM02008 is a slave stage and uses the EN and $\overline{EN}$ from the BAM02007, routed by means of cell abutment.

Logic Symbols

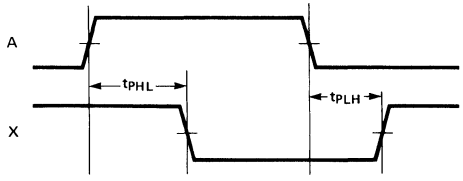


Cell Parameters

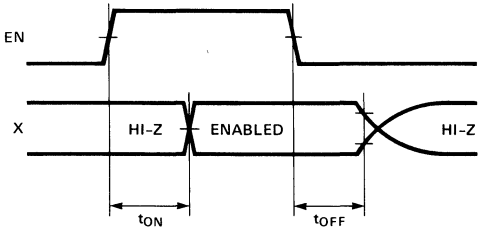
Parameter	BAM02007	BAM02008	Unit
Cell Width	61.6	30.8	μm
Cell Height	69.3	69.3	μm
Cell Area	4.3K	2.1K	Sq. μm
Average Power Dissipation*	20.0	4.0	μW/MHz
Input Capacitance (EN)	0.220	—	pF
Input Capacitance (A)	0.130	0.130	pF
Output Capacitance (X)	0.040	0.040	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Dynamic Characteristics



(EN = HIGH)



Propagation Delays (in nsec):

$t_{PHL} = 3.5\ (C_L) + 1.5$

$t_{PLH} = 3.5\ (C_L) + 1.5$

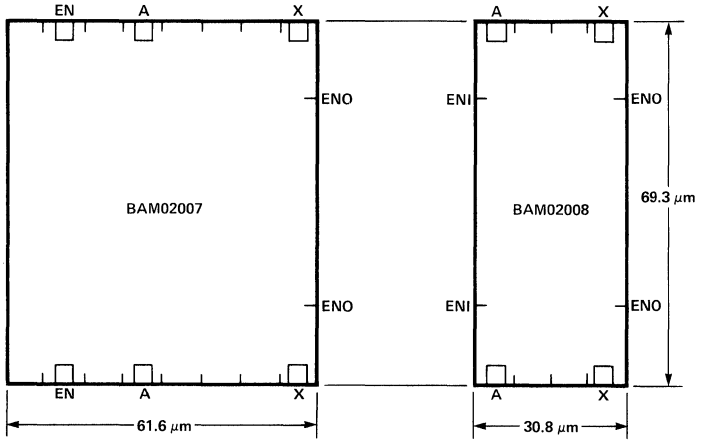
(C_L in pF)

$t_{OFF} = 0.3\ (N) + 3$

$t_{ON} = 0.3\ (N) + 3$

(N = Number of BAM02008 stages)

Outline Drawings



NAND Gates

3

Synertek

2-Input NAND Gate

BAM00010

Description

The BAM00010 is an HCMOS cell that performs the logic function of a 2-input NAND gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	23.1	μm
Cell Height	69.3	μm
Cell Area	1.6K	Sq. μm
Average Power Dissipation*	3.8	μW/MHz
Input Capacitance	0.040	pF

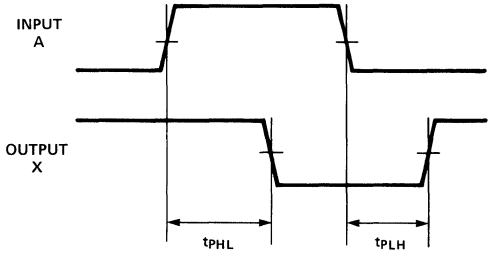
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs		Output
A	B	X
L	X	H
X	L	H
H	H	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUT B = HIGH LEVEL)

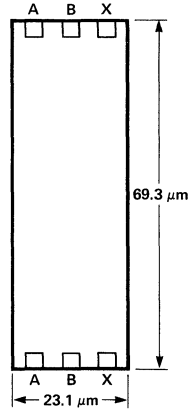
Propagation Delays (in nsec):

$t_{PHL} = 11\ (C_L) + 2$

$t_{PLH} = 22\ (C_L) + 2$

(C_L in pF)

Outline Drawing



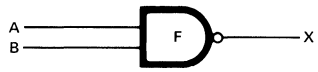
Fast 2-Input NAND Gate

BAM02010

Description

The BAM02010 is a high-speed version of the BAM00010 2-input NAND gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	Sq. μm
Average Power Dissipation*	9.0	μW/MHz
Input Capacitance	0.180	pF

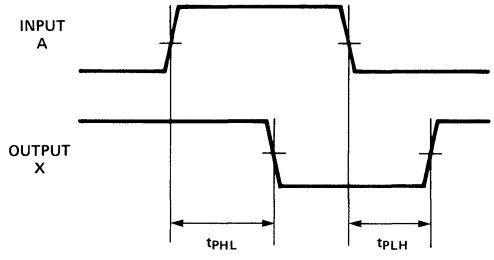
*V_{DD} = 5.0 V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs		Output
A	B	X
L	X	H
X	L	H
H	H	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



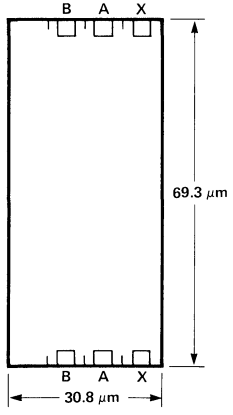
(INPUT B = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 2.5 (C_L) + 1$

$t_{PLH} = 3.0 (C_L) + 1$

Outline Drawing



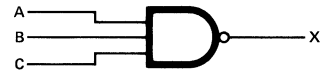
3-Input NAND Gate

BAM00011

Description

The BAM00011 is an HCMOS cell that performs the logic function of a 3-input NAND gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	Sq. μm
Average Power Dissipation*	4.0	μW/MHz
Input Capacitance	0.040	pF

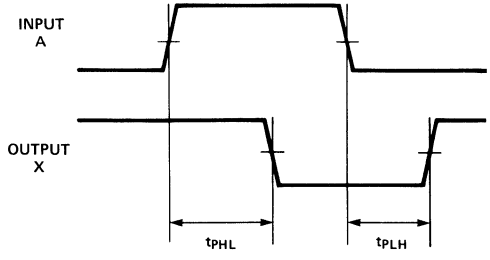
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Output
A	B	C	X
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



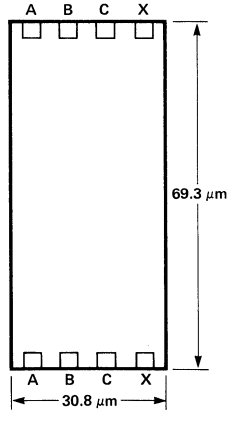
(INPUTS B, C = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 15 (C_L) + 2$

$t_{PLH} = 22 (C_L) + 3$

Outline Drawing



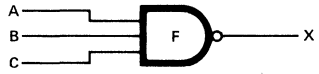
Fast 3-Input NAND Gate

BAM02011

Description

The BAM02011 is a high-speed version of the BAM00011 3-input NAND gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	Sq. μm
Average Power Dissipation*	11.0	μW/MHz
Input Capacitance	0.200	pF

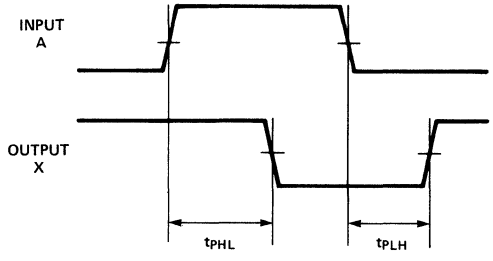
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Output
A	B	C	X
L	X	X	H
X	L	X	H
H	H	H	L

H = High level.
L = Low level.

Dynamic Characteristics



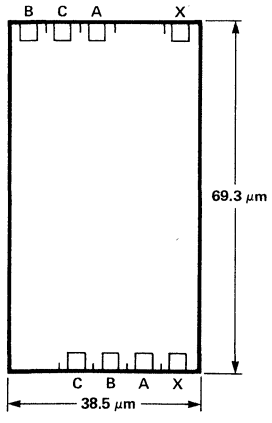
(INPUTS B, C = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 2.5 (C_L) + 1$

$t_{PLH} = 3.0 (C_L) + 1$

Outline Drawing



4-Input NAND Gate

BAM00012

Description

The BAM00012 is an HCMOS cell that performs the logic function of a 4-input NAND gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	Sq. μm
Average Power Dissipation*	4.0	μW/MHz
Input Capacitance	0.040	pF

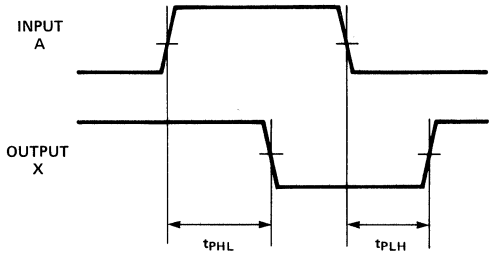
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Output
A	B	C	D	X
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



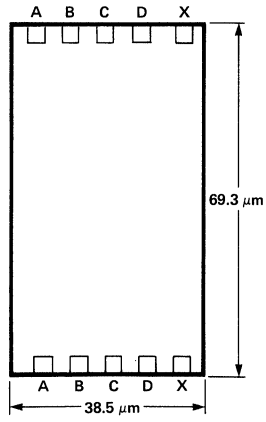
(INPUTS B, C, D = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 20 (C_L) + 3$

$t_{PLH} = 22 (C_L) + 4$

Outline Drawing



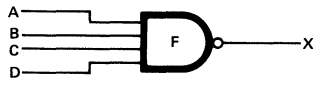
Fast 4-Input NAND Gate

BAM02012

Description

The BAM02012 is a high speed HCMOS cell which performs the function of a 4-input NAND.

Logic Symbol



Cell Parameters

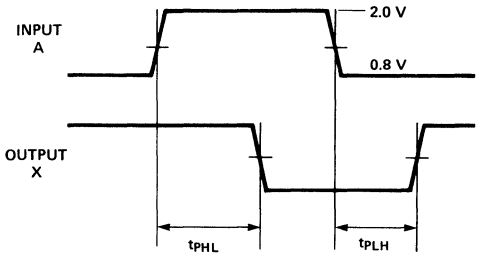
Parameter	Value	Unit
Cell Width	77	μm
Cell Height	69.3	μm
Cell Area	5.4K	Sq. μm
Average Power Dissipation*	11.0	μW/MHz
Input Capacitance	0.200	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Output
A	B	C	D	X
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Dynamic Characteristics



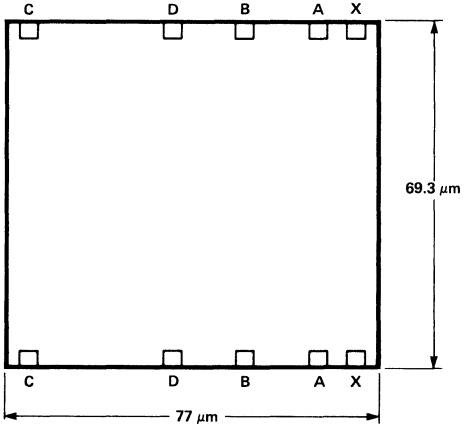
(B, C, D = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 2\,(C_L) + 2$

$t_{PLH} = 2\,(C_L) + 2$

Outline Drawing



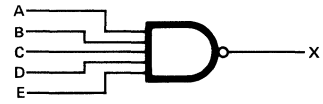
5-Input NAND Gate

BAM00013

Description

The BAM00013 is an HCMOS cell that performs the logic function of a 5-input NAND gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	46.2	μm
Cell Height	69.3	μm
Cell Area	3.2K	Sq. μm
Average Power Dissipation*	4.0	μW/MHz
Input Capacitance	0.040	pF

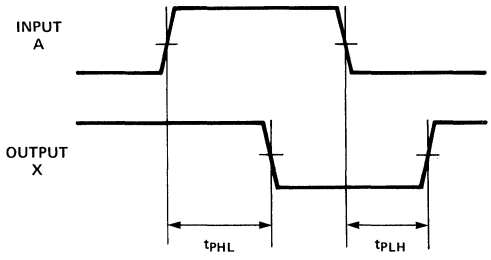
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs					Output
A	B	C	D	E	X
H	H	H	H	H	L
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



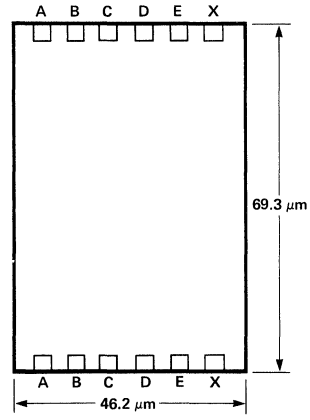
(INPUT B, C, D, E = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 20\ (C_L) + 5$

$t_{PLH} = 25\ (C_L) + 6$

Outline Drawing



High-Speed 5-Input NAND Gate

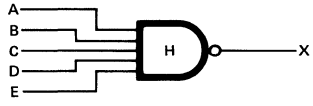
PRELIMINARY

BAM02013

Description

The BAM02013 is a high-speed HCMOS cell which performs the function of a 5-input NAND.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	TBD	μm
Cell Height	69.3	μm
Cell Area	TBD	Sq. μm
Average Power Dissipation*	11	μW/MHz
Input Capacitance	0.130	pF

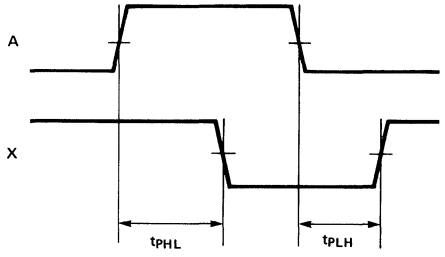
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs					Output
A	B	C	D	E	X
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = High level.
L = Low level.

Dynamic Characteristics



(B, C, D, E = HIGH LEVEL.)

Propagation Delays (in nsec):

$t_{PHL} = 3.0\ (C_L) + 1.0$

$t_{PLH} = 4.0\ (C_L) + 2.0$

(C_L in pF)

High Speed 6-Input NAND Gate

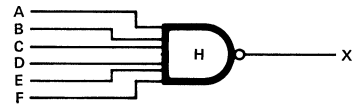
PRELIMINARY

BAM02014

Description

The BAM02014 is a high speed HCMOS cell which performs the function of a 6-input NAND.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	61.6	μm
Cell Height	69.3	μm
Cell Area	4.3K	Sq. μm
Average Power Dissipation*	11	μW/MHz
Input Capacitance	0.154	pF

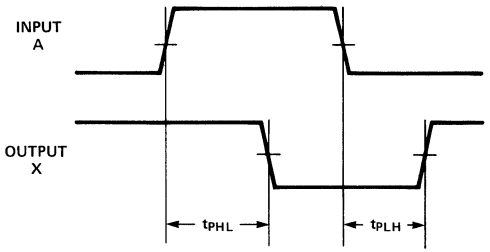
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs						Output
A	B	C	D	E	F	X
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

H = High Level
L = Low Level

Dynamic Characteristics



(B, C, D, E, F = HIGH LEVEL.)

Propagation Delays (in nsec):

$t_{PHL} = 3.0\ (C_L) + 1.0$

$t_{PLH} = 4.0\ (C_L) + 2.0$

(C_L in pF)

NOR Gates

4

Synertek.

2-Input NOR Gate

BAM00020

Description

The BAM00020 is an HCMOS cell that performs the logic function of a 2-input NOR gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	23.1	μm
Cell Height	69.3	μm
Cell Area	1.6K	Sq. μm
Average Power Dissipation*	2.5	μW/MHz
Input Capacitance	0.040	pF

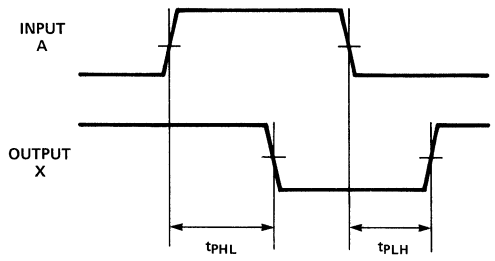
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs		Output
A	B	X
L	L	H
H	X	L
X	H	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUT B = LOW LEVEL)

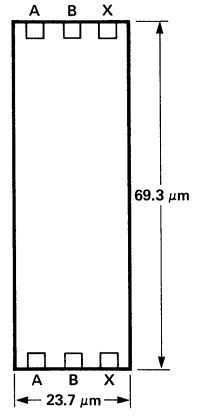
Propagation Delays (in nsec):

$t_{PHL} = 10 (C_L) + 2$

$t_{PLH} = 44 (C_L) + 6.7$

(C_L in pF)

Outline Drawing



3-Input NOR Gate

BAM00021

Description

The BAM00021 is an HCMOS cell that performs the logic function of a 3-input NOR gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	Sq. μm
Average Power Dissipation*	2.5	μW/MHz
Input Capacitance	0.040	pF

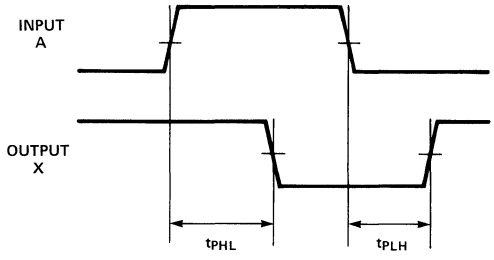
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Output
A	B	C	X
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUT B, C = LOW LEVEL)

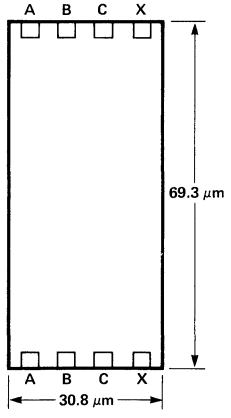
Propagation Delays (in nsec):

$t_{PHL} = 7 (C_L) + 1$

$t_{PLH} = 67 (C_L) + 6$

(C_L in pF)

Outline Drawing



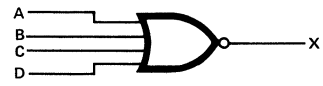
4-Input NOR Gate

BAM00022

Description

The BAM00022 is an HCMOS cell that performs the logic function of a 4-input NOR gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	Sq. μm
Average Power Dissipation*	2.5	μW/MHz
Input Capacitance	0.040	pF

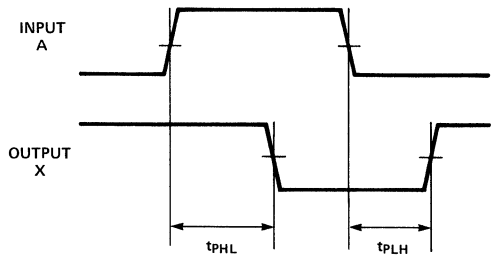
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Output
A	B	C	D	X
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUTS B, C, D = LOW LEVEL)

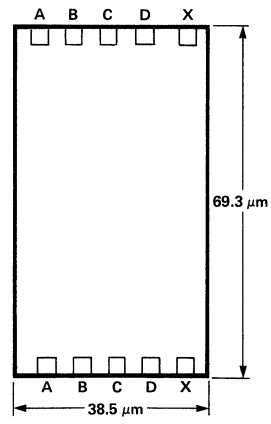
Propagation Delays (in nsec):

$t_{PHL} = 7 (C_L) + 1$

$t_{PLH} = 92 (C_L) + 9$

(C_L in pF)

Outline Drawing



High Speed 4-Input NOR Gate

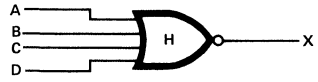
PRELIMINARY

BAM02022

Description

The BAM02022 is a high-speed version of the BAM00022 4-input NOR Gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	46.2	μm
Cell Height	69.3	μm
Cell Area	3.2K	Sq. μm
Average Power Dissipation*	6.0	μW/MHz
Input Capacitance	0.300	pF

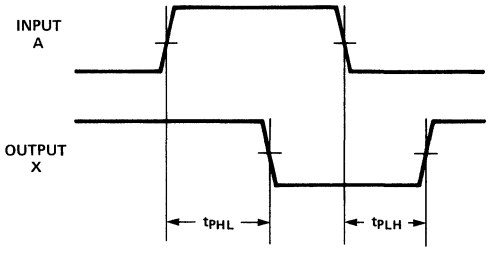
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Output
A	B	C	D	X
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

H = High level.
L = Low level.

Dynamic Characteristics



(INPUTS B, C, D = LOW)

Propagation Delays (in nsec):

$t_{PHL} = 1.5 (C_L) + 1.0$

$t_{PLH} = 1.5 (C_L) + 1.0$

(C_L in pF)

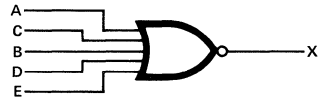
5-Input NOR Gate

BAM00023

Description

The BAM00023 is an HCMOS cell that performs the logic function of a 5-input NOR gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	53.9	μm
Cell Height	69.3	μm
Cell Area	3.7K	Sq. μm
Average Power Dissipation*	2.5	μW/MHz
Input Capacitance	0.040	pF

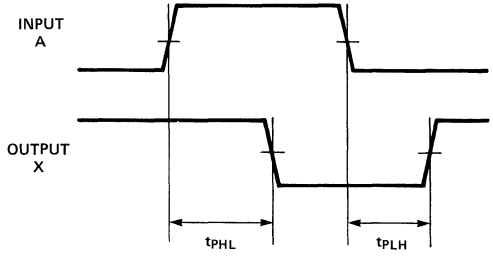
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs					Output
A	B	C	D	E	X
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUTS B, C, D, E = LOW LEVEL)

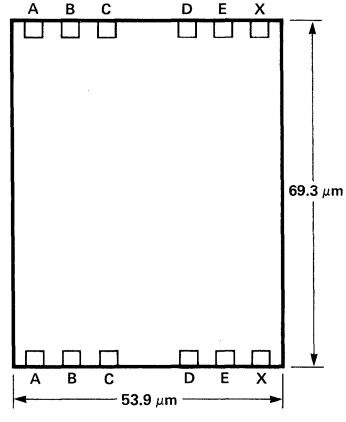
Propagation Delays (in nsec):

$t_{PHL} = 7\ (C_L) + 1$

$t_{PLH} = 118\ (C_L) + 17$

(C_L in pF)

Outline Drawing



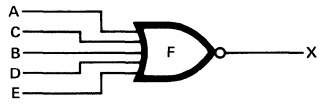
High-Speed 5-Input NOR Gate

BAM02023

Description

The BAM02023 is a high-speed version of the BAM00023 5-input NOR gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	84.7	μm
Cell Height	69.3	μm
Cell Area	5.9K	Sq. μm
Average Power Dissipation*	34	μW/MHz
Input Capacitance	0.310	pF

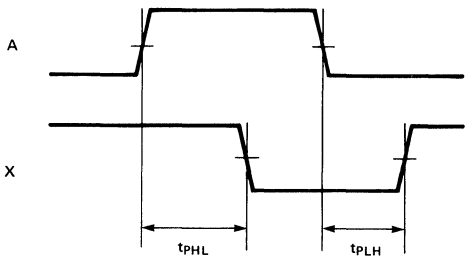
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs					Output
A	B	C	D	E	X
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUTS B, C, D, E = LOW LEVEL)

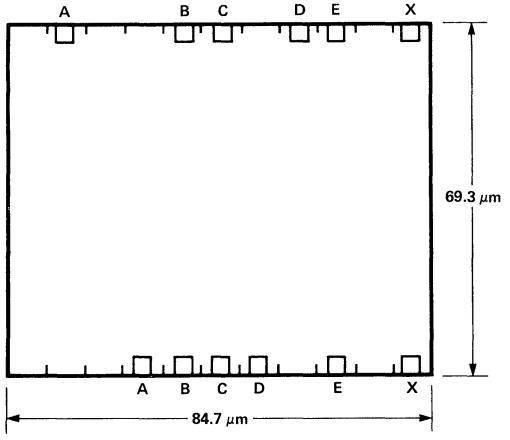
Propagation Delays (in nsec):

$t_{PHL} = 2.0\ (C_L) + 2.5$

$t_{PLH} = 2.7\ (C_L) + 3.0$

(C_L in pF).

Outline Drawing



AND Gates

5

Synertek.

2-Input AND Gate

BAM00030

Description

The BAM00030 is an HCMOS cell that performs the logic function of a 2-input AND gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	Sq. μm
Average Power Dissipation*	3.5	μW/MHz
Input Capacitance	0.040	pF

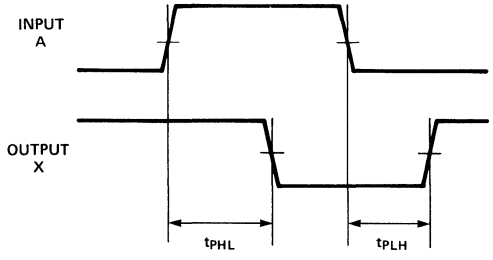
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs		Output
A	B	X
L	X	L
X	L	L
H	H	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



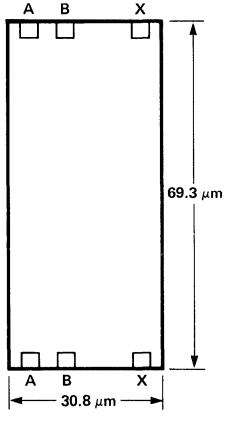
(INPUT B = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 7 (C_L) + 4$

$t_{PLH} = 22 (C_L) + 4$

Outline Drawing



3-Input AND Gate

BAM00031

Description

The BAM00031 is an HCMOS cell that performs the logic function of a 3-input AND gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	Sq. μm
Average Power Dissipation*	3.5	μW/MHz
Input Capacitance	0.040	pF

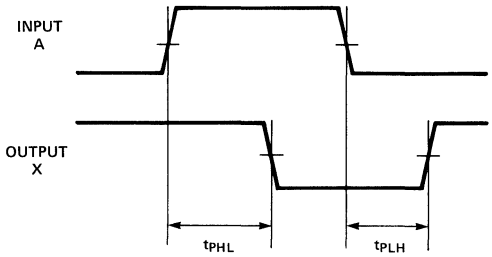
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Output
A	B	C	X
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



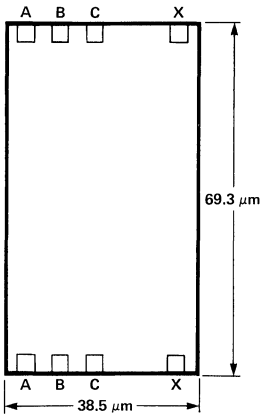
(INPUTS B, C = HIGH LEVEL)

Propagation Delays: (in nsec):

$t_{PHL} = 7 (C_L) + 4$

$t_{PLH} = 23 (C_L) + 4$

Outline Drawing



AND GATES

4-Input AND Gate

BAM00032

Description

The BAM00032 is an HCMOS cell that performs the logic function of a 4-input AND gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	46.2	μm
Cell Height	69.3	μm
Cell Area	3.2K	Sq. μm
Average Power Dissipation*	3.5	μW/MHz
Input Capacitance	0.040	pF

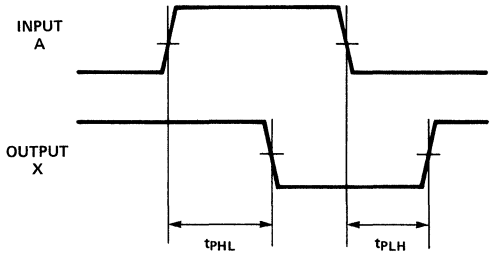
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Output
A	B	C	D	X
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUTS B, C, D = HIGH LEVEL)

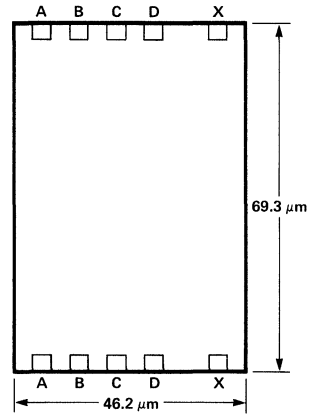
Propagation Delays (in nsec):

$t_{PHL} = 7 (C_L) + 4$

$t_{PLH} = 23 (C_L) + 6$

(C_L in pF)

Outline Drawing



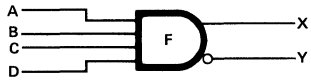
Fast 4-Input AND Gate

BAM02032

Description

The BAM02032 is a high-speed HCMOS cell which performs the function of a 4-input AND. For convenience, the intermediate NAND function is also available as an output.

Logic Symbol



Cell Parameters

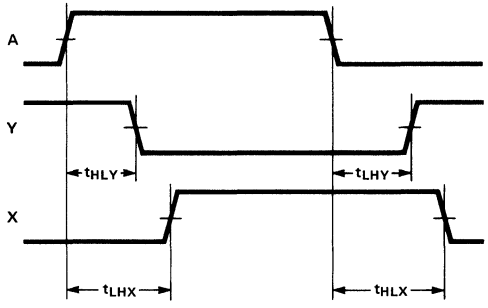
Parameter	Value	Unit
Cell Width	85	μm
Cell Height	69.3	μm
Cell Area	5.9K	Sq. μm
Average Power Dissipation*	15	μW/MHz
Input Capacitance	0.200	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Outputs	
A	B	C	D	X	Y
L	X	X	X	L	H
X	L	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
H	H	H	H	H	L

Dynamic Characteristics



(B, C, D = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{HLY} = 2 (C_L) + 2$

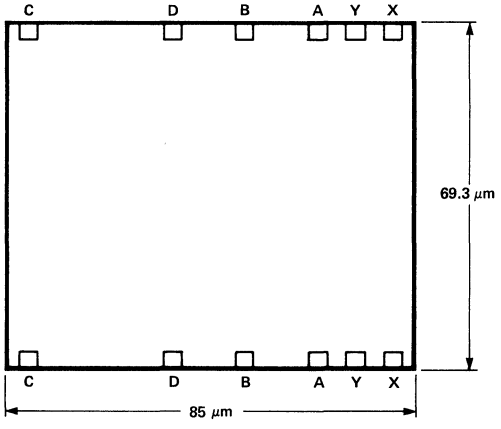
$t_{LHY} = 2 (C_L) + 2$

$t_{HLX} = 7 (C_L) + 2$

$t_{LHX} = 7 (C_L) + 2$

(C_L in pF)

Outline Drawing



AND GATES

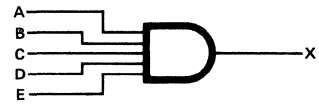
5-Input AND Gate

BAM00033

Description

The BAM00033 is an HCMOS cell that performs the logic function of a 5-input AND gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	53.9	μm
Cell Height	69.3	μm
Cell Area	3.7K	Sq. μm
Average Power Dissipation*	3.5	μW/MHz
Input Capacitance	0.040	pF

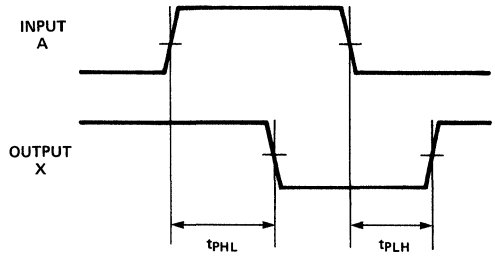
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs					Output
A	B	C	D	E	X
L	X	X	X	X	L
X	L	X	X	X	L
X	X	L	X	X	L
X	X	X	L	X	L
X	X	X	X	L	L
H	H	H	H	H	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



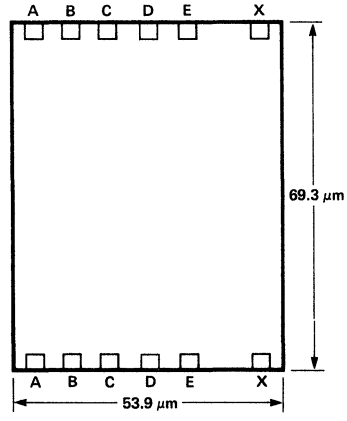
(INPUTS B, C, D, E = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 7\ (C_L) + 4$

$t_{PLH} = 23\ (C_L) + 6$

Outline Drawing



OR Gates

6

Synertek.

2-Input OR Gate

BAM00040

Description

The BAM00040 is an HCMOS cell that performs the logic function of a 2-input OR gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.2K	Sq. μm
Average Power Dissipation*	3.5	μW/MHz
Input Capacitance	0.040	pF

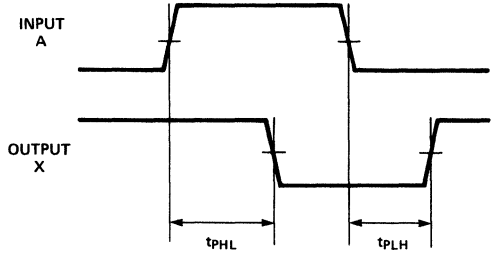
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs		Output
A	B	X
H	X	H
X	H	H
L	L	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



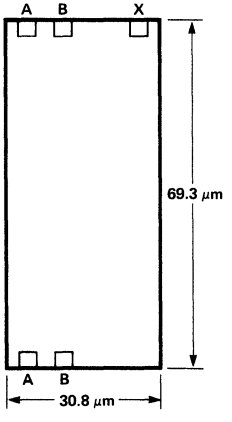
(INPUT B = LOW LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 8 (C_L) + 6$

$t_{PLH} = 23 (C_L) + 3$

Outline Drawing



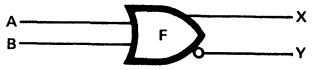
Fast 2-Input OR Gate

BAM02040

Description

The BAM02040 is a high speed HCMOS cell which performs the function of a 2-input OR gate. For convenience, the intermediate NOR function is also available as an output.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	61.6	μm
Cell Height	69.3	μm
Cell Area	4.3K	Sq. μm
Average Power Dissipation*	10.0	μW/MHz
Input Capacitance	0.165	pF

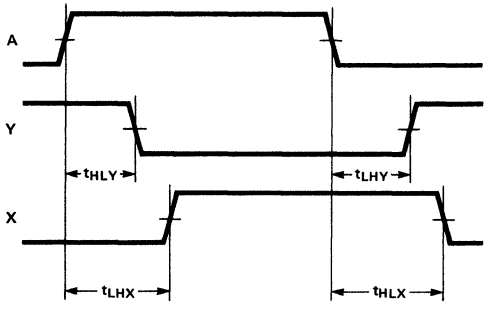
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs		Outputs	
A	B	X	Y
X	H	H	L
H	X	H	L
L	L	L	H

H = High level.
L = Low level.

Dynamic Characteristics



(B, C, D = HIGH LEVEL)

Propagation Delays (in nsec):

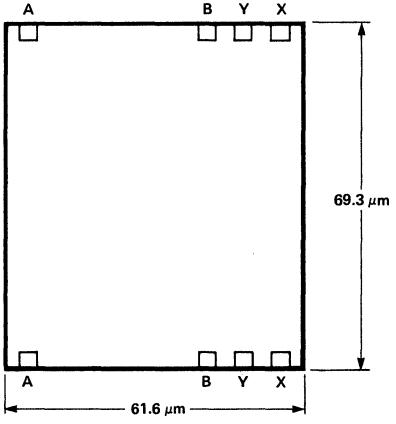
$t_{HLY} = 2 (C_L) + 2$

$t_{LHY} = 3 (C_L) + 2$

$t_{HLX} = 5 (C_L) + 2$

$t_{LHX} = 5 (C_L) + 2$

Outline Drawing



3-Input OR Gate

BAM00041

Description

The BAM00041 is an HCMOS cell that performs the logic function of a 3-input OR gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	Sq. μm
Average Power Dissipation*	3.5	μW/MHz
Input Capacitance	0.040	pF

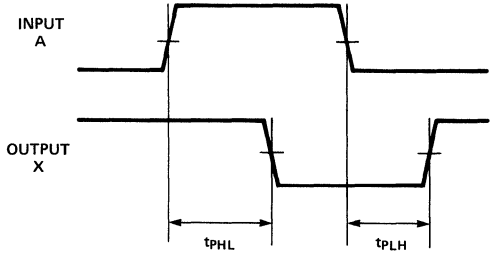
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Output
A	B	C	X
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



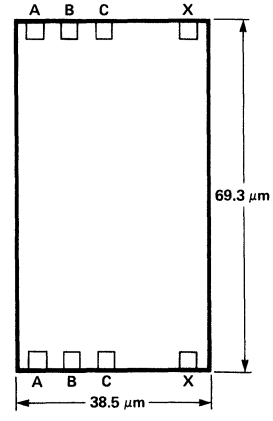
(INPUTS B, C = LOW LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 9\ (C_L) + 8$

$t_{PLH} = 23\ (C_L) + 3$

Outline Drawing



High-Speed 3-Input OR Gate

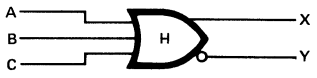
PRELIMINARY

BAM02041

Description

The BAM02041 is a high speed HCMOS cell which performs the function of a 3-input OR gate. For convenience, the intermediate NOR function is also available as an output.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	92.4	μm
Cell Height	69.3	μm
Cell Area	6.4K	Sq. μm
Average Power Dissipation*	10	μW/MHz
Input Capacitance	0.250	pF

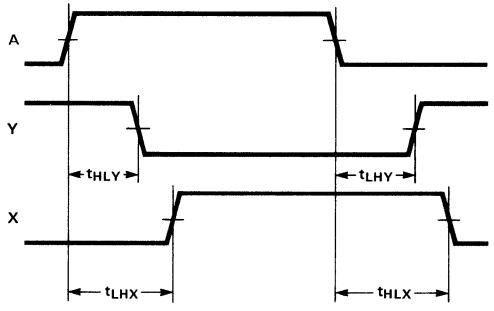
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Outputs	
A	B	C	X	Y
H	X	X	H	L
X	H	X	H	L
X	X	H	H	L
L	L	L	L	H

H = High level.
L = Low level.

Dynamic Characteristics



(B, C = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{HLY} = 1.5\ (C_L) + 2$

$t_{LHY} = 1.5\ (C_L) + 2$

$t_{HLX} = 6\ (C_L) + 1.0$

$t_{LHX} = 4\ (C_L) + 1.5$

(C_L in pF)

4-Input OR Gate

BAM00042

Description

The BAM00042 is an HCMOS cell that performs the logic function of a 4-input OR gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	46.2	μm
Cell Height	69.3	μm
Cell Area	3.2K	Sq. μm
Average Power Dissipation*	3.5	μW/MHz
Input Capacitance	0.040	pF

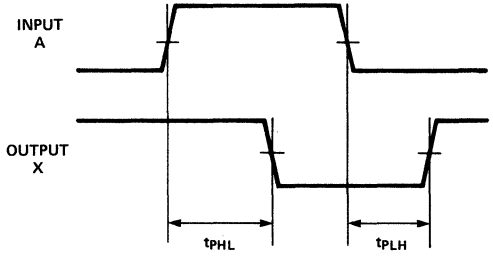
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Output
A	B	C	D	X
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H
L	L	L	L	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



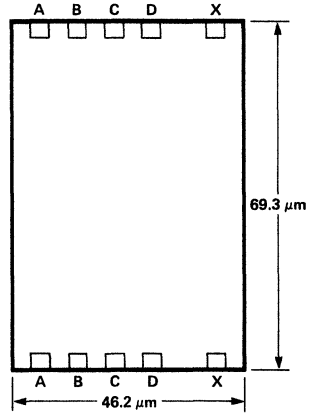
(INPUTS B, C, D = LOW LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 10\ (C_L) + 9$

$t_{PLH} = 23\ (C_L) + 3$

Outline Drawing



High Speed 4-Input OR Gate

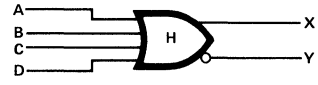
PRELIMINARY

BAM02042

Description

The BAM02042 is a high speed HCMOS cell which performs the function of a 4-input OR gate. For convenience, the intermediate NOR function is also available as an output.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	115.5	μm
Cell Height	69.3	μm
Cell Area	8.0K	Sq. μm
Average Power Dissipation*	10.0	μW/MHz
Input Capacitance	0.300	pF

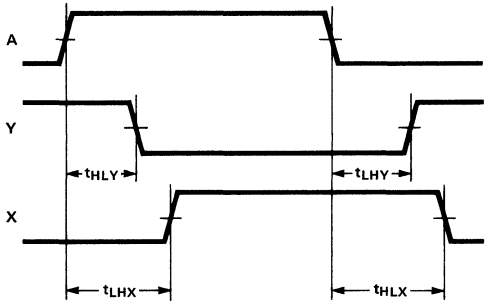
*V_{DD} = 5.0V, T_A = 25° C, CL = 0.050 pF.

Function Table

Inputs				Output	
A	B	C	D	X	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	L	H

H = High level.
L = Low level.

Dynamic Characteristics



(B, C, D = HIGH LEVEL)

Propagation Delays (in nsec):

$t_{HLY} = 1.5 (C_L) + 2$

$t_{LHY} = 2.0 (C_L) + 2$

$t_{HLX} = 6 (C_L) + 2$

$t_{LHX} = 2 (C_L) + 2$

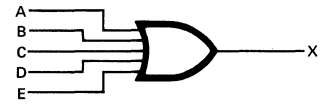
5-Input OR Gate

BAM00043

Description

The BAM00043 is an HCMOS cell that performs the logic function of a 5-input OR gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	61.6	μm
Cell Height	69.3	μm
Cell Area	4.3K	Sq. μm
Average Power Dissipation*	3.5	μW/MHz
Input Capacitance	0.040	pF

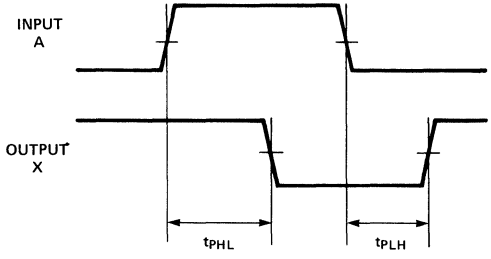
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs					Output
A	B	C	D	E	X
H	X	X	X	X	H
X	H	X	X	X	H
X	X	H	X	X	H
X	X	X	H	X	H
X	X	X	X	H	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



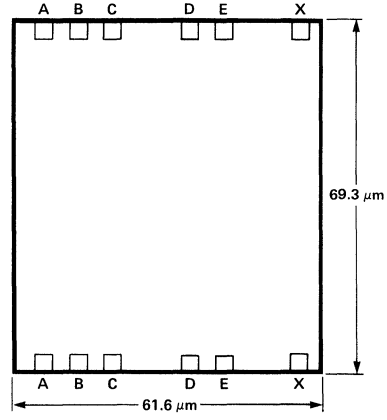
(INPUTS B, C, D, E = LOW LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 11\ (C_L) + 9$

$t_{PLH} = 23\ (C_L) + 3$

Outline Drawing



XOR Gates

7

Synertek.

Description

The BAM00050 is an HCMOS cell that performs the logic function of an exclusive-OR gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	Sq. μm
Average Power Dissipation*	3.0	μW/MHz
Input Capacitance	0.080	pF

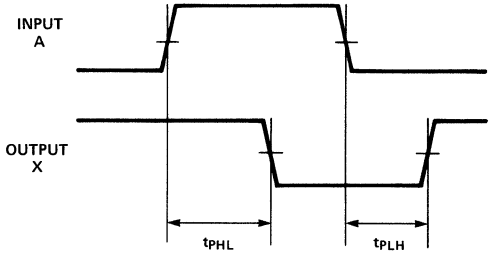
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs		Output
A	B	X
L	L	L
L	H	H
H	L	H
H	H	L

H = High level.
L = Low level.

Dynamic Characteristics

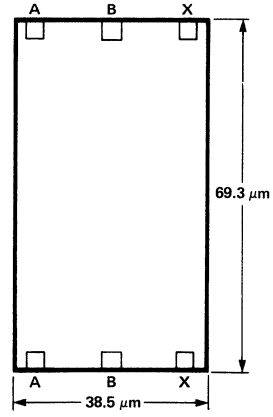


Propagation Delays (in nsec):

$t_{PHL} = 11 (C_L) + 2$

$t_{PLH} = 46 (C_L) + 6$

Outline Drawing



Exclusive-NOR

BAM00051

Description

The BAM00051 is an HCMOS cell that performs the logic function of an exclusive-NOR gate.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	Sq. μm
Average Power Dissipation*	3.0	μW/MHz
Input Capacitance	0.080	pF

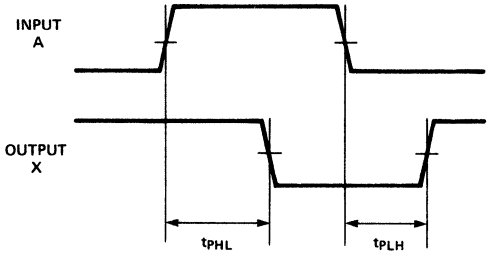
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs		Output
A	B	X
L	L	H
H	L	L
L	H	L
H	H	H

H = High level.
L = Low level.

Dynamic Characteristics



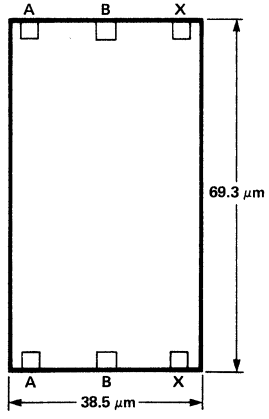
(INPUT B = LOW LEVEL)

Propagation Delays (in nsec):

$t_{PHL} = 11 (C_L) + 5$

$t_{PLH} = 45 (C_L) + 7$

Outline Drawing



XOR GATES

AND-NOR/ OR-NAND Gates

8

Synertek.

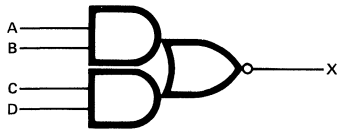
2,2 AND-NOR Gate

BAM00060

Description

The BAM00060 is an HCMOS cell that performs the logic function of a 2-by-2 AND-NOR gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	Sq. μm
Average Power Dissipation*	4.0	μW/MHz
Input Capacitance	0.040	pF

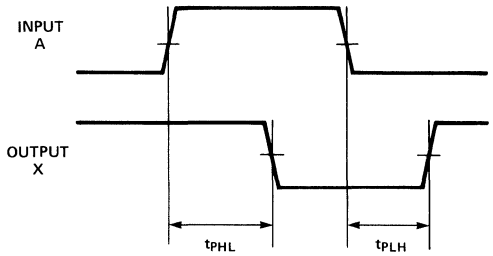
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Output
A	B	C	D	X
H	H	X	X	L
X	X	H	H	L
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUT B = HIGH, INPUTS C, D = LOW)

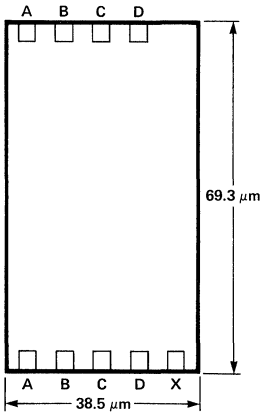
Propagation Delays (in nsec):

$t_{PHL} = 11\ (C_L) + 2$

$t_{PLH} = 35.5\ (C_L) + 6$

(C_L in pF)

Outline Drawing



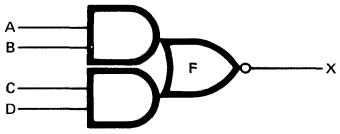
Fast 2, 2 AND-NOR Gate

BAM02060

Description

The BAM02060 is a high speed version of the BAM00060 cell, a 2-by-2 AND-NOR gate.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	46.2	μm
Cell Height	69.3	μm
Cell Area	3.2K	Sq. μm
Average Power Dissipation*	5.5	μW/MHz
Input Capacitance	0.112	pF

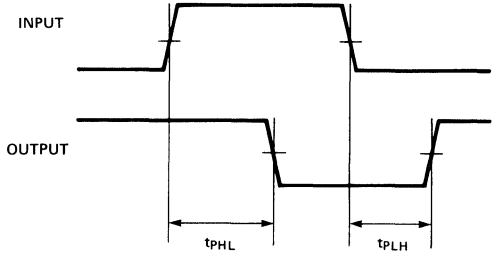
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Output
A	B	C	D	X
H	H	X	X	L
X	X	H	H	L
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUT B = HIGH, INPUTS C, D = LOW)

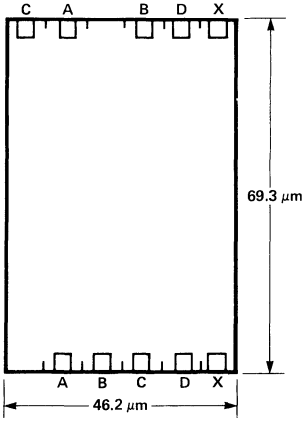
Propagation Delays (in nsec):

$t_{PHL} = 5.0\ (C_L) + 1.5$

$t_{PLH} = 6.0\ (C_L) + 2.0$

(C_L in pF).

Outline Drawing



2,1 AND-NOR Gate

BAM00061

Description

The BAM00061 is an HCMOS cell that performs the logic function of a 2-by-1 AND-NOR gate.

Logic Symbol

Positive Logic Equation:

$X = \overline{(A \cdot B) + C}$

Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	sq. μm
Average Power Dissipation*	4.0	μW/MHz
Input Capacitance	0.040	pF

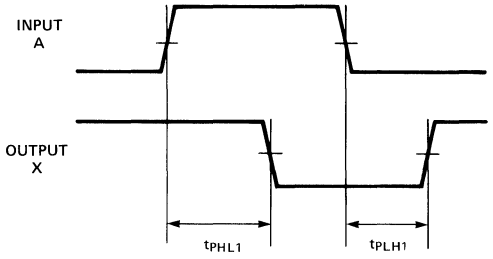
*V_{DD} = 5.0 V, T_A = 25° C, C_L = 0.050 pF.

Function Table

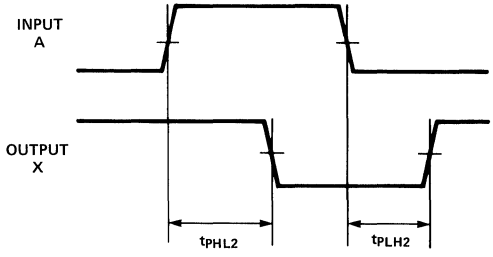
Inputs			Output
A	B	C	X
H	H	X	L
X	X	H	L
L	X	L	H
X	L	L	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUT B = HIGH, INPUT C = LOW)



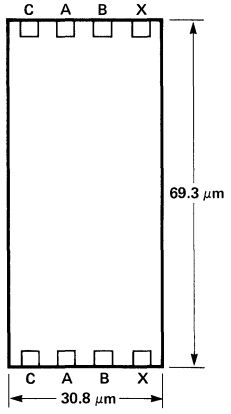
(INPUTS A, B = LOW)

Propagation Delays (in nsec):

$t_{PHL1} = 11\ (C_L) + 2$ $\quad t_{PHL2} = 7\ (C_L) + 1$

$t_{PLH1} = 46\ (C_L) + 6$ $\quad t_{PLH2} = 47\ (C_L) + 4$

Outline Drawing



Fast 2, 1 AND-NOR Gate

BAM02061

Description

The BAM02061 is a high speed version of the BAM00061 cell, a 2-by-1 AND-NOR gate.

Logic Symbol

Positive Logic Equation:

$X = \overline{(A \cdot B) + C}$

Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	sq. μm
Average Power Dissipation*	5.5	μW/MHz
Input Capacitance	0.110	pF

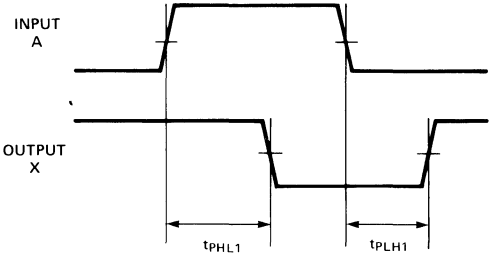
*V_{DD} = 5.0 V, T_A = 25°C, C_L = 0.050 pF.

Function Table

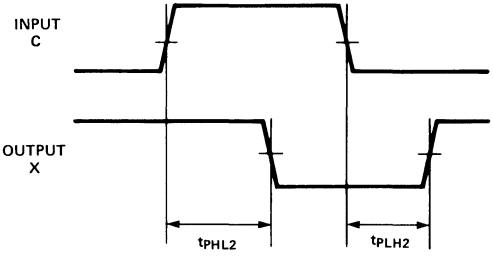
Inputs			Output
A	B	C	X
H	H	X	L
X	X	H	L
L	X	L	H
L	X	X	H
X	L	L	H

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUT B = HIGH, INPUT C = LOW)



(INPUTS A, B = LOW)

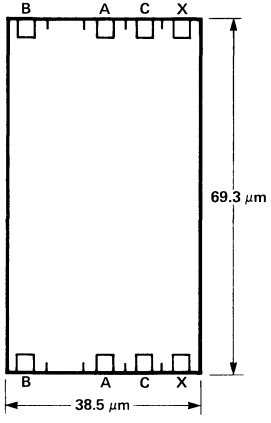
Propagation Delays (in nsec):

$t_{PLH1} = 5.7\ (C_L) + 0.7$ $t_{PHL2} = 3.5\ (C_L) + 0.7$

$t_{PHL1} = 5.0\ (C_L) + 1.7$ (C_L in pF).

$t_{PLH2} = 6.5\ (C_L) + 1.7$

Outline Drawing



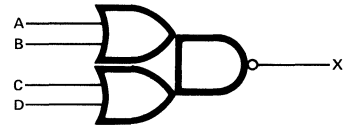
2,2 OR-NAND Gate

BAM00062

Description

The BAM00062 is an HCMOS cell that performs the logic function of a 2-by-2 OR-NAND gate.

Logic Symbol



Positive Logic Equation:

$X = \overline{(A + B) \cdot (C + D)}$

Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	sq. μm
Average Power Dissipation*	4.0	μW/MHz
Input Capacitance	0.040	pF

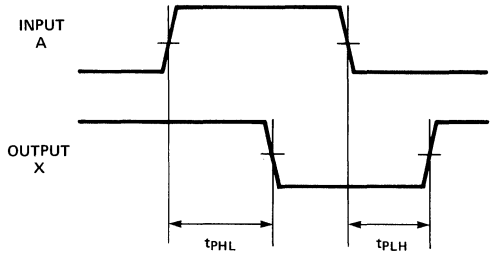
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Output
A	B	C	D	X
L	L	X	X	H
X	X	L	L	H
H	X	H	X	L
H	X	X	H	L
X	H	H	X	L
X	H	X	H	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



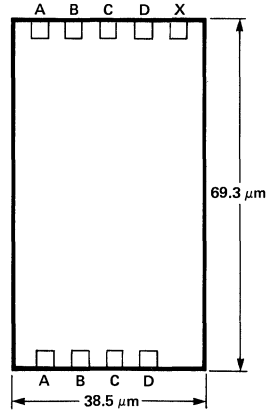
(INPUT B = LOW, INPUTS C, D = HIGH)

Propagation Delays (in nsec):

$t_{PHL} = 11 (C_L) + 2$

$t_{PLH} = 46 (C_L) + 5$

Outline Drawing



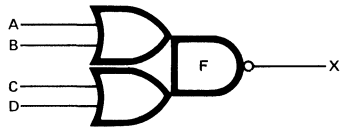
Fast 2, 2 OR-NAND Gate

BAM02062

Description

The BAM02062 is a high speed version of the BAM00062 cell, a 2-by-2 OR-NAND gate.

Logic Symbol



Positive Logic Equation:

$X = \overline{(A + B) \cdot (C + D)}$

Cell Parameters

Parameter	Value	Unit
Cell Width	46.2	μm
Cell Height	69.3	μm
Cell Area	3.2K	sq. μm
Average Power Dissipation*	5.5	μW/MHz
Input Capacitance	0.110	pF

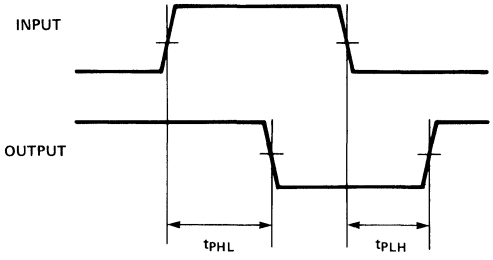
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Output
A	B	C	D	X
L	L	X	X	H
X	X	L	L	H
H	X	H	X	L
H	X	X	H	L
X	H	H	X	L
X	H	X	H	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUT B = LOW, INPUTS C, D = HIGH)

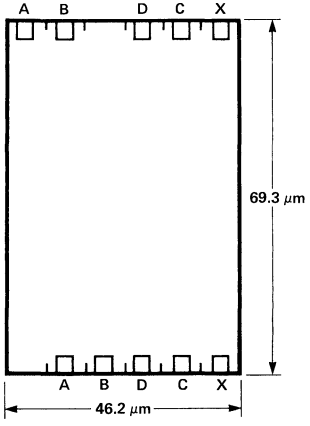
Propagation Delays (in nsec):

$t_{PHL} = 5.0\ (C_L) + 1.7$

$t_{PLH} = 6.0\ (C_L) + 2.0$

(C_L in pF).

Outline Drawing



2,1 OR-NAND Gate

BAM00063

Description

The BAM00063 is an HCMOS cell that performs the logic function of a 2-by-1 OR-NAND gate.

Logic Symbol

Positive Logic Equation:

$X = \overline{(A + B) \cdot C}$

Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	sq. μm
Average Power Dissipation*	4.0	μW/MHz
Input Capacitance	0.040	pF

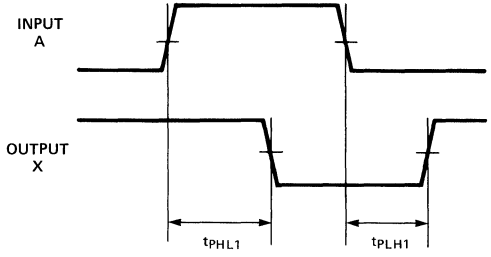
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

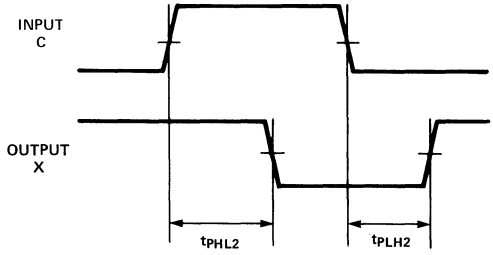
Inputs			Output
A	B	C	X
L	L	X	H
X	X	L	H
H	X	H	L
X	H	H	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



(INPUT B = LOW, INPUT C = HIGH)



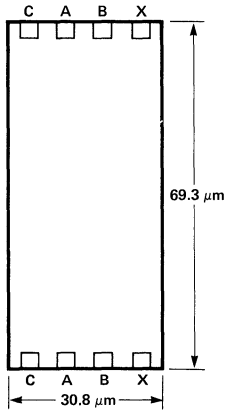
(INPUTS A, C = HIGH)

Propagation Delays (in nsec):

$t_{PHL1} = 11\ (C_L) + 2$ $\quad t_{PHL2} = 11\ (C_L) + 2$

$t_{PLH1} = 46\ (C_L) + 6$ $\quad t_{PLH2} = 23\ (C_L) + 3$

Outline Drawing



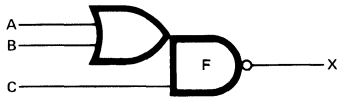
Fast 2, 1 OR-NAND Gate

BAM02063

Description

The BAM02063 is a high speed version of the BAM00063 cell, a 2-by-1 OR-NAND gate.

Logic Symbol



Positive Logic Equation:

$X = \overline{(A + B) \cdot C}$

Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	sq. μm
Average Power Dissipation*	5.5	μW/MHz
Input Capacitance	0.120	pF

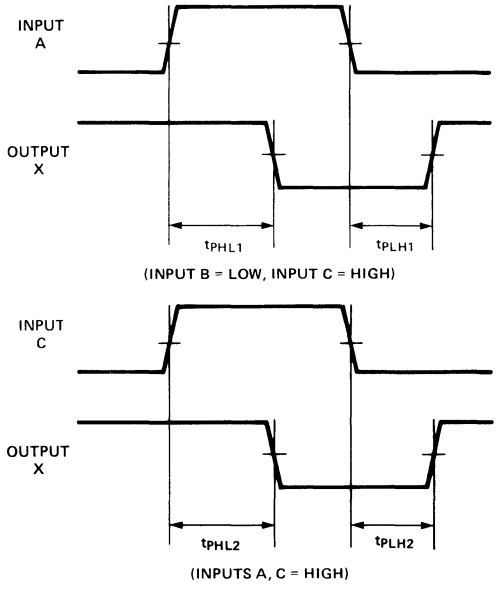
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Output
A	B	C	X
L	L	X	H
X	X	L	H
H	X	H	L
X	H	H	L

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



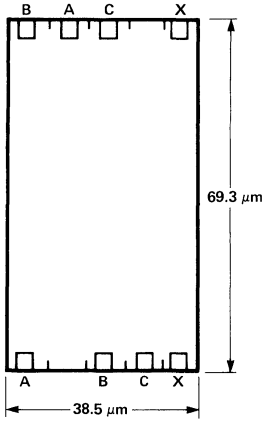
Propagation Delays (in nsec):

$t_{PLH1} = 4.7\ (C_L) + 1.5$ $t_{PHL2} = 4.7\ (C_L) + 2.0$

$t_{PHL1} = 5.0\ (C_L) + 1.0$ (C_L in pF)

$t_{PLH2} = 3.7\ (C_L) + 1.0$

Outline Drawing



Multiplexers/ Decoder Drivers

9

Synertek.

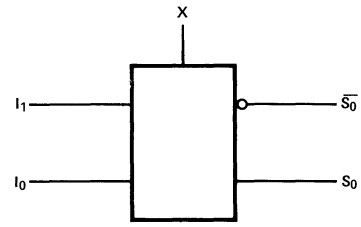
2-to-1 Multiplexer

BAM00072

Description

The BAM00072 is an HCMOS cell that performs the function of a 2-to-1 multiplexer. One of two identical inputs may be gated (low impedance feedthrough path) to a common output by means of the control signals, S_0 and $\overline{S_0}$. This cell may only be used by abutment to the mux driver cell, BAM00076.

Logic Symbol



Cell Parameters

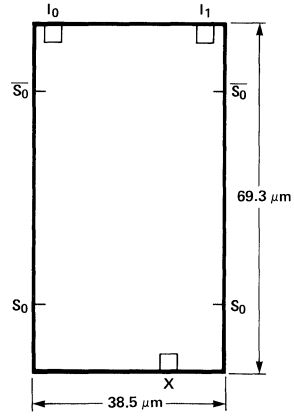
Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	Sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance (I_0, I_1)	0.070	pF
Input Capacitance (S_0, $\overline{S_0}$)	0.110	pF
"ON" Resistance (Typ.)	6K	Ω

Function Table

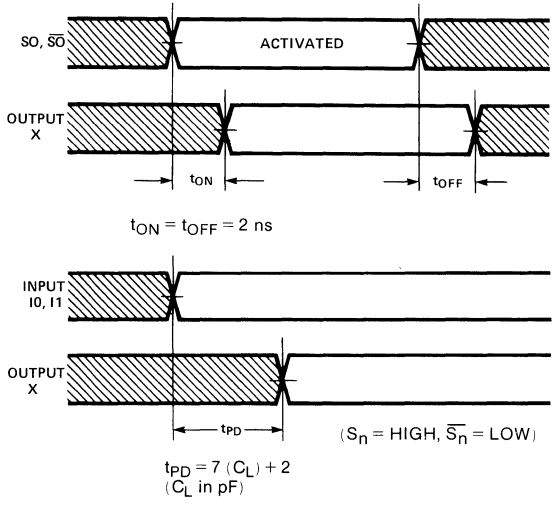
Controls Inputs		Low Impedance Input to Output Path
S_0	$\overline{S_0}$	
H	L	I_0
L	H	I_1
L	L	Undefined
H	H	Undefined

H = High level.
L = Low level.

Outline Drawing



Dynamic Characteristics



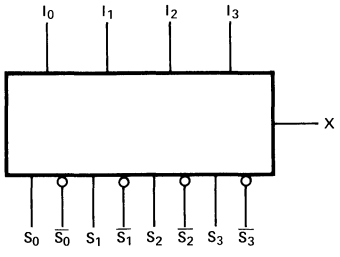
4-to-1 Multiplexer

BAM00073

Description

The BAM00073 is an HCMOS cell that performs the function of a 4-to-1 multiplexer. One of four identical inputs may be gated to a common output by activating the appropriate pair of select lines. Each pair of select lines consists of a positive-true and a negative-true control. The positive-true line must be high and the negative-true line must be low to select that particular input. The opposite condition of both control lines is the unselected case. Only one of four inputs may be selected at any one time. This cell may only be used by abutment to the mux driver cell, BAM00077.

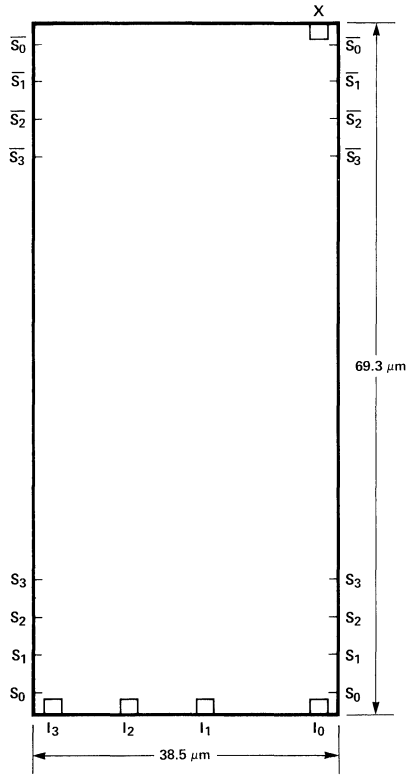
Logic Symbol



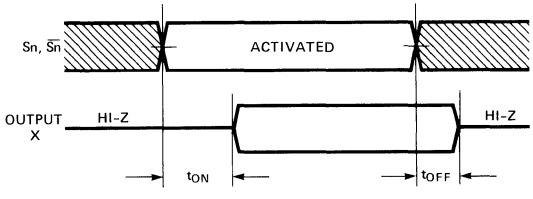
Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	Sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance (S_N, $\overline{S_N}$)	0.120	pF
"ON" Resistance (Typ.)	3.4K	Ω

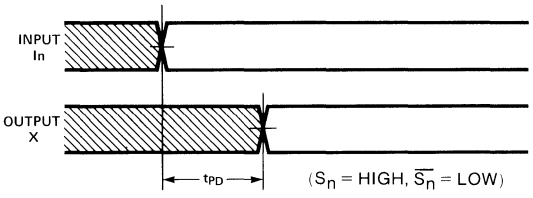
Outline Drawing



Dynamic Characteristics



$t_{ON} = t_{OFF} = 2$ ns



$t_{PD} = 4\ (C_L) + 2$
(C_L in pF)

8-to-1 Multiplexer

BAM00074

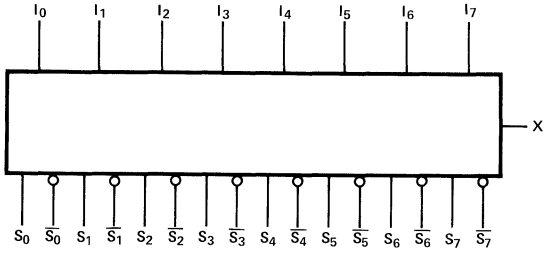
Description

The BAM00074 is an HCMOS cell that performs the function of a 8-to-1 multiplexer. One of eight identical inputs may be gated to a common output by activating the appropriate pair of select lines. Each pair of select lines consists of a positive-true and a negative-true control. The positive-true line must be high and the negative-true line must be low to select that particular input. The opposite condition of both control lines is the unselected case. Only one of eight inputs may be selected at any one time. This cell may only be used by abutement to the mux driver cell, BAM00078.

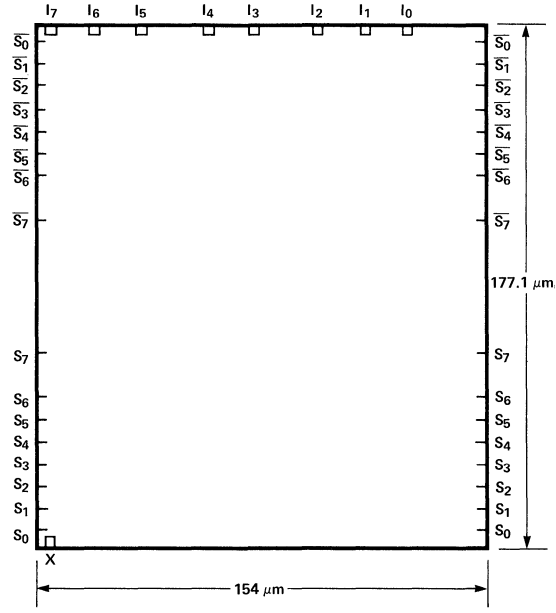
Cell Parameters

Parameter	Value	Unit
Cell Width	154	μm
Cell Height	177.1	μm
Cell Area	27.3K	Sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance (I_N)	0.050	pF
Input Capacitance (S_N, $\overline{S_N}$)	0.250	pF
"ON" Resistance (Typ.)	1.4K	Ω

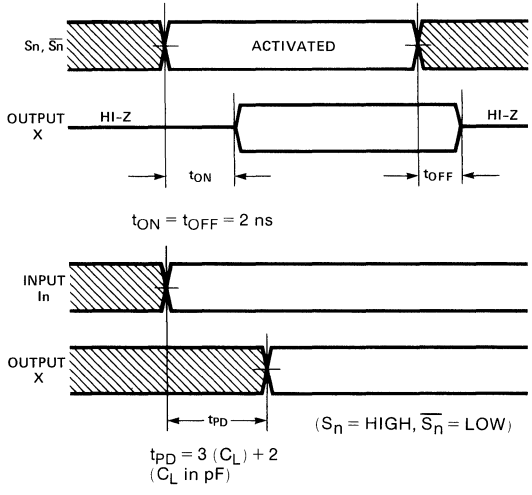
Logic Symbol



Outline Drawing



Dynamic Characteristics



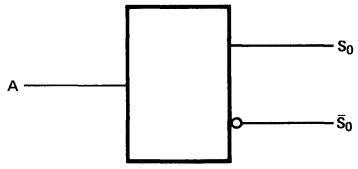
Mux Driver

BAM00076

Description

The BAM00076 is an HCMOS cell that is used as a driver for the BAM00072 Multiplexer cell. Input A is used to select the desired output pair which, in turn, selects one of two analog inputs in the mux cell. The cell layout is designed to be located directly adjacent to the mux cell so that no external connections are required.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	sq. μm
Average Power Dissipation*	6.0	μW/MHz
Input Capacitance	0.070	pF

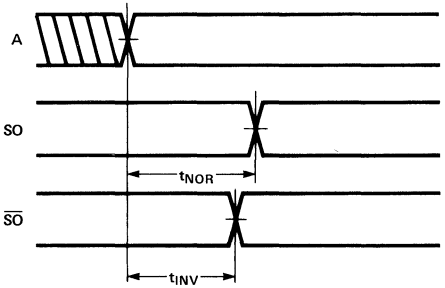
*V_{DD} = 5.0V, T_A = 25° C, C_L = BAM00072.

Function Table

Input	Outputs	
A	S_0	$\overline{S_0}$
H	H	L
L	L	H

H = High level.
L = Low level.

Dynamic Characteristics



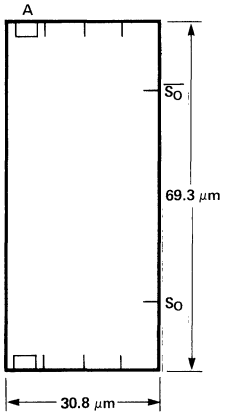
Propagation Delays (in nsec):

$t_{NOR} = 3 + 2N$

$t_{INV} = 2 + 1N$

(N = Number of BAM00072 stages to be driven)

Outline Drawing



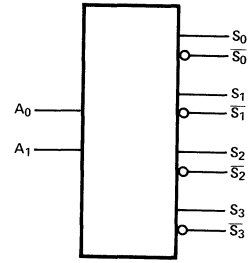
2-to-4 Mux Decoder/Driver

BAM00077

Description

The BAM00077 is an HCMOS cell that is used as a decoder/driver for the BAM00073 Multiplexer cell. It decodes 2 input selects into a 1-of-4 output pair activation. Each output pair consists of a positive-true and a negative-true signal. Only one of the 4 output pairs is active at any time. The cell layout is designed to be located directly adjacent to the mux cell so that no external connections are required.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	146.3	μm
Cell Height	138.6	μm
Cell Area	20.3K	sq. μm
Average Power Dissipation*	65	μW/MHz
Input Capacitance	0.350	pF

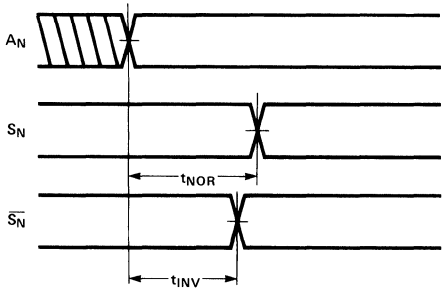
*V_{DD} = 5.0V, T_A = 25° C, C_L = BAM00073.

Function Table

Inputs		Active Output Pair
A_1	A_0	
L	L	S_0
L	H	S_1
H	L	S_2
H	H	S_3

H = High level.
L = Low level.

Dynamic Characteristics



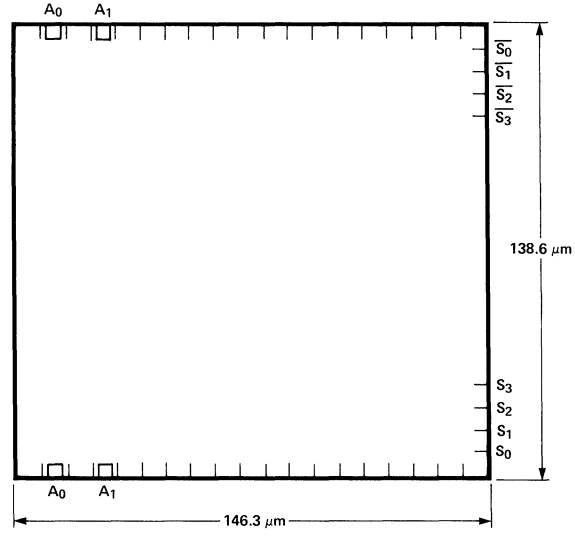
Propagation Delays (in nsec):

$t_{NOR} = 6 + 0.7N$

$t_{INV} = 6 + 0.3N$

(N = Number of BAM00073 stages to be driven)

Outline Drawing



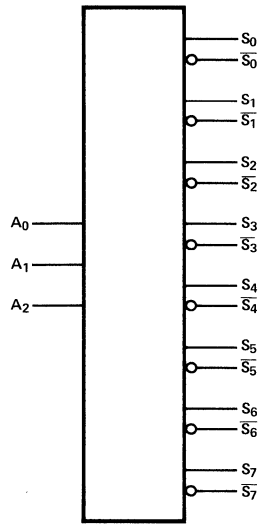
3-To-8 MUX Decoder/Driver

BAM00078

Description

The BAM00078 is an HCMOS cell that is used as a decoder/driver for the BAM00074 Multiplexer cell. It decodes 3 input selects into a 1-of-8 output pair activation. Each output pair consists of a positive-true and a negative-true signal. Only one of the 8 output pairs is active at any time. The cell layout is designed to be located directly adjacent to the mux cell so that no external connections are required.

Logic Symbol

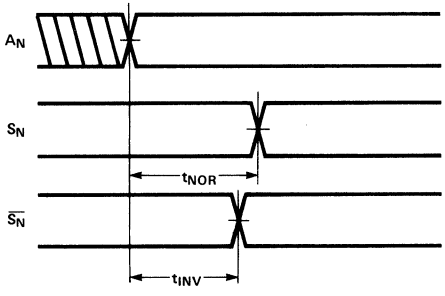


Cell Parameters

Parameter	Value	Unit
Cell Width	293	μm
Cell Height	177	μm
Cell Area	52K	sq. μm
Average Power Dissipation*	140	μW/MHz
Input Capacitance	1.0	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = BAM00074.

Dynamic Characteristics



Propagation Delays (in nsec):

$t_{NOR} = 10 + 1.5N$

$t_{INV} = 7 + 0.7N$

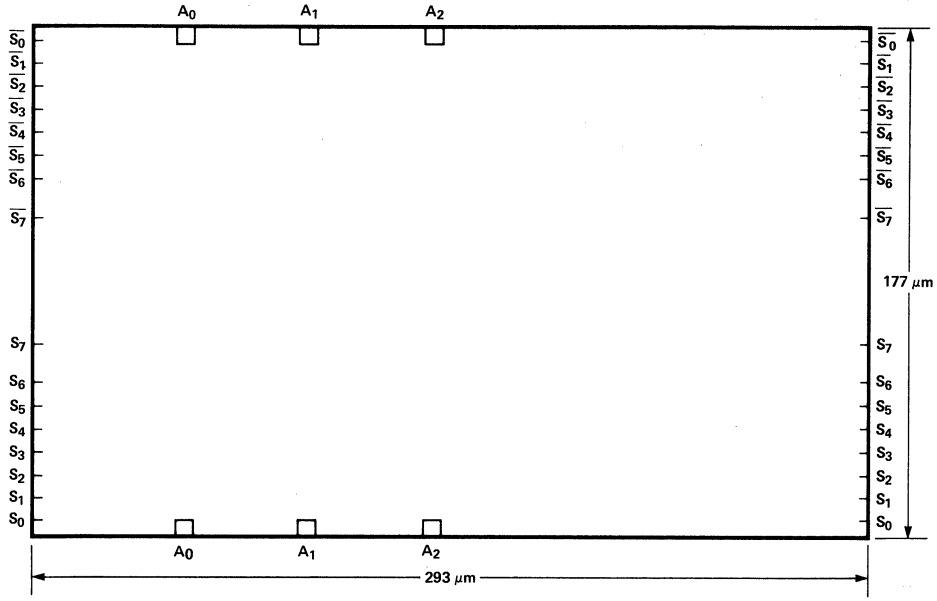
(N = Number of BAM00074 stages to be driven).

Function Table

Inputs			Active Output Pair
A_2	A_1	A_0	
L	L	L	S_0
L	L	H	S_1
L	H	L	S_2
L	H	H	S_3
H	L	L	S_4
H	L	H	S_5
H	H	L	S_6
H	H	H	S_7

H = High level.
L = Low level.

Outline Drawing



Flip-Flops/ Latches/Registers

10

Synertek.

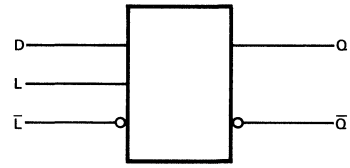
D-Latch Without Reset

BAM00080

Description

The BAM00080 is an HCMOS cell which performs the function of a D-type flip-flop. The L and $\overline{L}$ complementary inputs are the latch controls. When L is high and $\overline{L}$ is low, the Q output follows the D input. When L goes low and $\overline{L}$ goes high, Q latches to its current state, independent of D. $\overline{Q}$ is the complement of Q.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	53.9	μm
Cell Height	69.3	μm
Cell Area	3.7K	sq. μm
Average Power Dissipation*	4.5	μW/MHz
Input Capacitance (L, $\overline{L}$)	0.050	pF
Input Capacitance (D)	0.040	pF

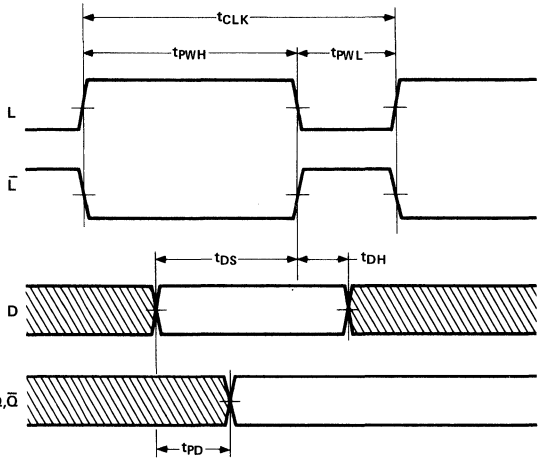
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Outputs	
L	$\overline{L}$	D	Q	$\overline{Q}$
H	L	H	H	L
H	L	L	L	H
L	H	X	Q_0	$\overline{Q_0}$

H = High level.
L = Low level.
X = "Don't care".
Q_0 = The level of Q output prior to L and $\overline{L}$ changing state.

Dynamic Characteristics



Mimimum Pulse Widths:

t_{PWH} = 10 nsec

t_{PWL} = 10 nsec

Minimum Set-Up and Hold Times:

t_{DS} = 10 nsec

t_{DH} = 0 nsec

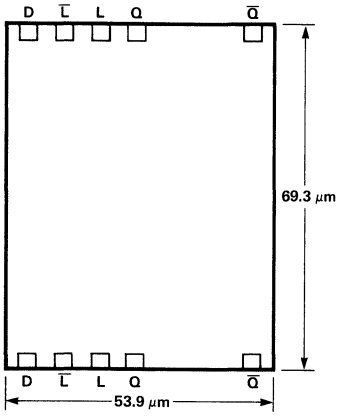
Maximum Propagation Delays:

t_{PD} = 15 (C_L) + 7 nsec

Maximum Clock Rate:

$f_{CLK} = \frac{1}{t_{CLK}} = 50$ MHz

Outline Drawing



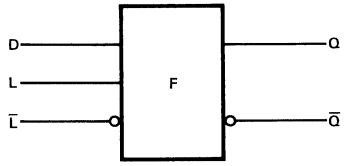
Fast Transparent D-Latch

BAM02080

Description

The BAM02080 is a high speed version of the BAM00080 cell. It performs the function of a transparent D-Latch. When L and $\overline{L}$ are asserted, the Q output follows the D input. When L and $\overline{L}$ are de-asserted, the Q and $\overline{Q}$ retain their state independent of the D input.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	77	μm
Cell Height	69.3	μm
Cell Area	5.4K	Sq. μm
Average Power Dissipation*	14.0	μW/MHz
Input Capacitance (D)	0.055	pF
Input Capacitance (L, $\overline{L}$)	0.100	pF

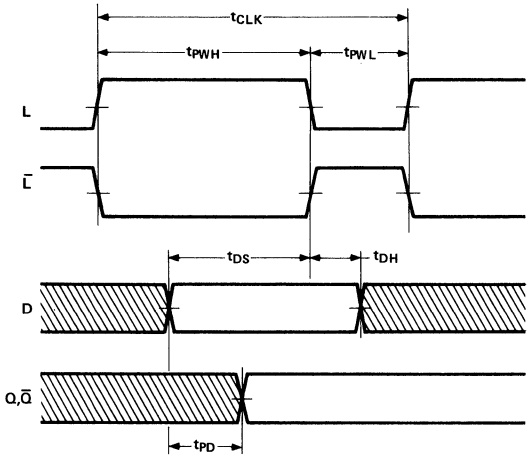
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Outputs	
L	$\overline{L}$	D	Q	$\overline{Q}$
H	L	H	H	L
H	L	L	L	H
L	H	X	Q_o	$\overline{Q_o}$

H = High level.
L = Low level.
X = "Don't Care".
Q_o = The level on Q output prior de-asserting.

Dynamic Characteristics



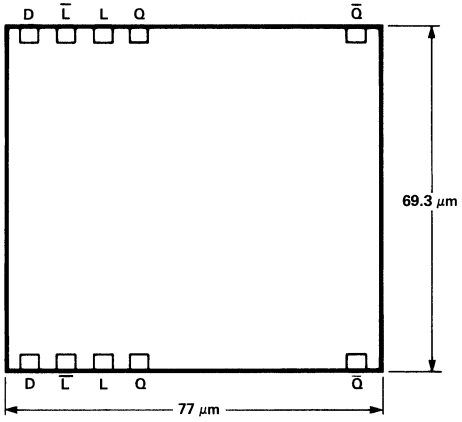
Minimum Pulse Widths:
t_{PWH} = 5.5 nsec
t_{PWL} = 5.5 nsec

Minimum Set-up and Hold Times:
t_{DS} = 4 nsec
t_{DH} = 0 nsec

Maximum Propagation Delays:
t_{PD} = 2 (C_L) + 2 nsec

Maximum Clock Rate:
t_{CLK} = 60 MHz

Outline Drawing



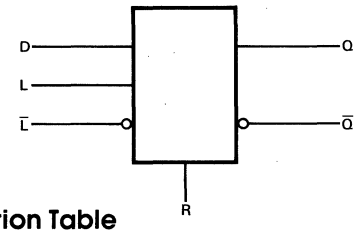
D-Latch with Reset

BAM00081

Description

The BAM00081 is an HCMOS cell which performs the function of a D-type flip-flop with a positive-true reset control. The L and $\overline{L}$ complementary inputs are the latch controls. When L and $\overline{L}$ are logic true levels, the Q output follows the D input. When L and $\overline{L}$ go to their logic false levels, Q retains the current state. $\overline{Q}$ is the complement of Q.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	61.6	μm
Cell Height	69.3	μm
Cell Area	4.3K	sq. μm
Average Power Dissipation*	5.5	μW/MHz
Input Capacitance (D, R)	0.040	pF
Input Capacitance (L, $\overline{L}$)	0.050	pF

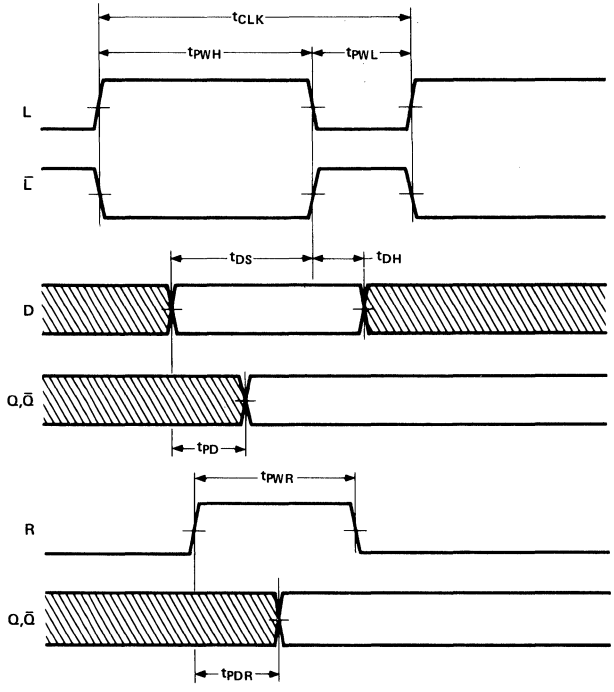
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Outputs	
R	L	$\overline{L}$	D	Q	$\overline{Q}$
H	X	X	X	L	X
L	H	L	H	H	L
L	H	L	L	L	H
L	L	H	X	Q_0	$\overline{Q}_0$

H = High level.
L = Low level.
X = "Don't care".
Q_0 = The level of Q output prior to L and $\overline{L}$ changing state.

Dynamic Characteristics



Minimum Set-up and Hold Times:

t_{DS} = 10 nsec

t_{DH} = 0 nsec

Minimum Pulse Widths:

t_{PWH} = 10 nsec

t_{PWL} = 10 nsec

t_{PWR} = 10 nsec

Maximum Propagation Delays:

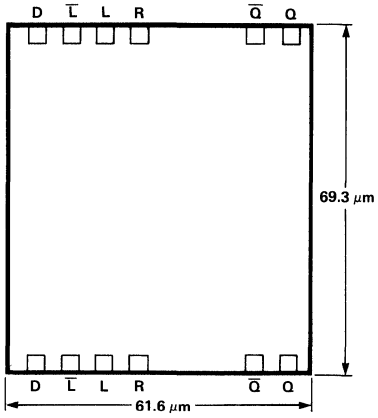
$t_{PD} = 15\ (C_L) + 7$ nsec

$t_{PDR} = 15\ (C_L) + 5$ nsec

Maximum Clock Rate:

$f_{CLK} = \frac{1}{t_{CLK}} = 50$ MHz

Outline Drawing



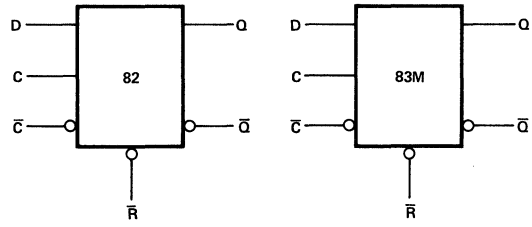
D Flip-Flop with Reset

BAM00082/83

Description

The BAM00082/83 cells are HCMOS cells which perform the function of a D-type flip-flop with negative-true reset control. The two cells are identical in their electrical function and characteristics and differ only in their physical layouts. The BAM00082 is intended for use as the first stage in a shift register. As such, all inputs and outputs are accessible. The BAM00083, on the other hand, is intended for use as a subsequent stage in a shift register and thus, only the Q and $\overline{Q}$ outputs are accessible. When the cells are abutted, the Q output of the first stage becomes the D input to the second, thus providing for shift register function.

Logic Symbol



Cell Parameters

Parameter	Value BAM00082	Value BAM00083	Unit
Cell Width	100.1	61.6	μm
Cell Height	138.6	138.6	μm
Cell Area	13.9K	8.5K	sq. μm
Average Power Dissipation*	9.0	9.0	μW/MHz
Input Capacitance (D)	0.050	0.050	pF
Input Capacitance (C, $\overline{C}$)	0.110	0.110	pF
Input Capacitance ($\overline{R}$)	0.140	0.140	pF

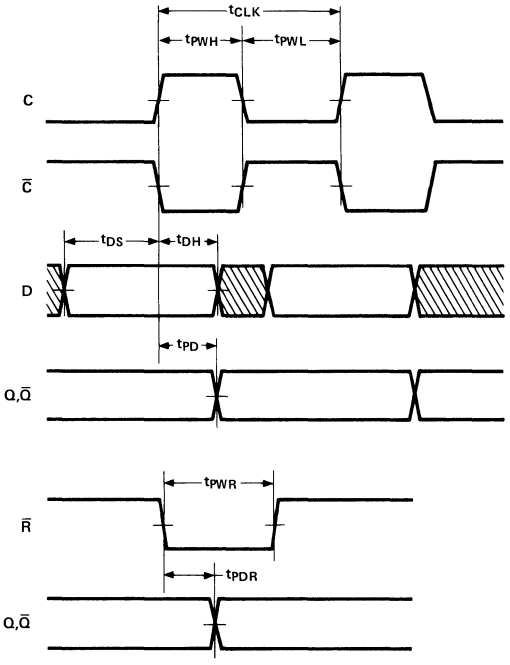
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Outputs	
$\overline{R}$	D	C	$\overline{C}$	Q	$\overline{Q}$
L	X	X	X	L	H
H	H	⌐	¬	⌐	¬
H	L	⌐	¬	¬	⌐

H = High level.
L = Low level.
X = "Don't care".
⌐ = Low-to-high transition.
¬ = High-to-low transition.

Dynamic Characteristics



Minimum Pulse Widths:

t_{PWH} = 10 nsec

t_{PWL} = 10 nsec

t_{PWR} = 10 nsec

Minimum Set-up and Hold Times:

t_{DS} = 10 nsec

t_{DH} = 0 nsec

Maximum Propagation Delays:

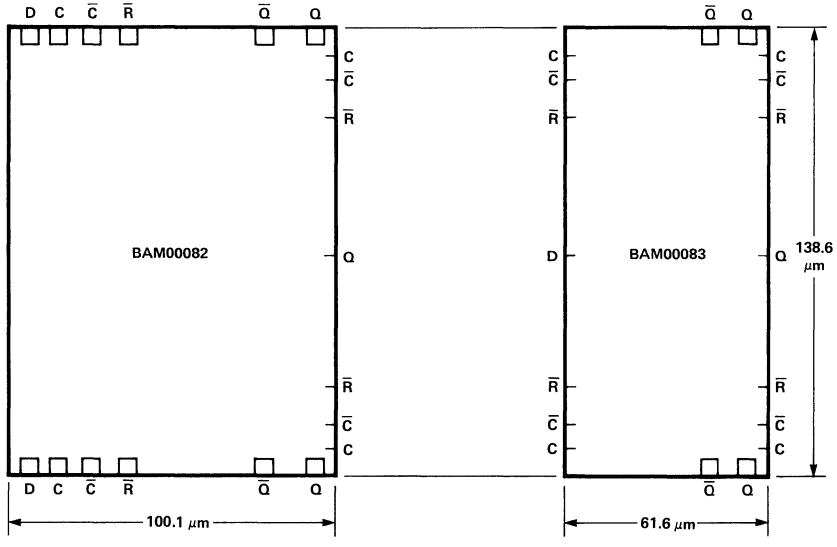
$t_{PD} = 15\ (C_L) + 7$ nsec

$t_{PDR} = 15\ (C_L) + 5$ nsec

Maximum Clock Rate:

$f_{CLK} = \frac{1}{t_{CLK}} = 50$ MHz

Outline Drawings



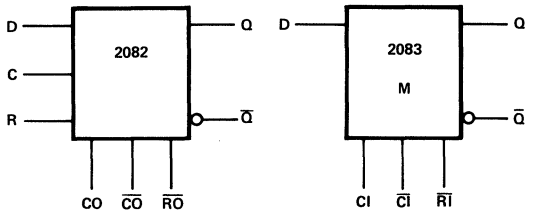
High-Speed D-Type Flip-Flop

BAM02082/2083

Description

The BAM02082/83 are high-speed D-type flip-flops with positive-true Clock and Reset signals. The BAM02082 is the first stage flip-flop and contains buffers for both Clock and Reset inputs. The BAM02083 is used as a subsequent stage in a chain and may only be used by abutment to the BAM02082. In this way, it is possible to chain stages together to form shift registers or latching registers of any desired length with a minimum of external interconnect.

Logic Symbols

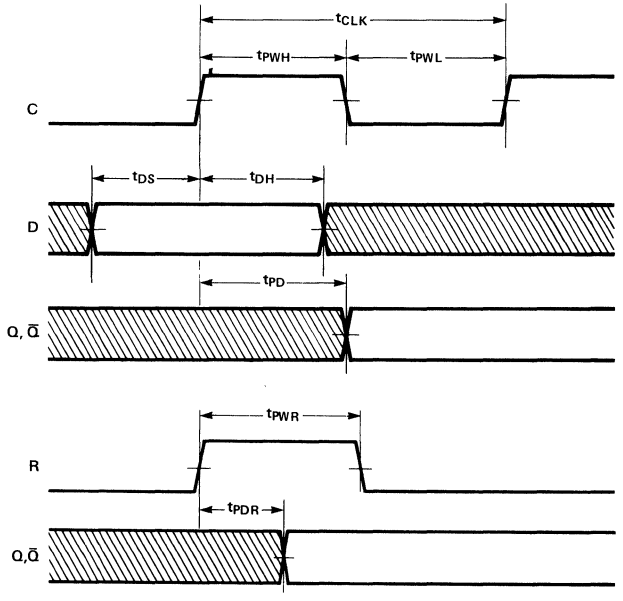


Cell Parameters

Parameter	Value BAM02082	Value BAM02083	Unit
Cell Width	123.2	84.7	μm
Cell Height	138.6	138.6	μm
Cell Area	17.1K	11.7K	Sq. μm
Average Power Dissipation*			μW/MHz
Input Capacitance (C)	0.220	—	pF
Input Capacitance (R)	0.140	—	pF
Input Capacitance (D)	0.070	0.070	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Dynamic Characteristics



Propagation Delays:

t_{PD} (Q) = 2.0(C_L) + 3.5

t_{PD} ($\overline{Q}$) = 4.0(C_L) + 4.0

t_{PDR} (Q) = 5.0(C_L) + 7.0

t_{PDR} ($\overline{Q}$) = 2.0(C_L) + 4.0

Minimum Pulse Widths:

t_{PWH} = 6.0

t_{PWL} = 6.0

t_{PWR} = 6.0

Minimum Set-up Times:

t_{DS} = 6.0

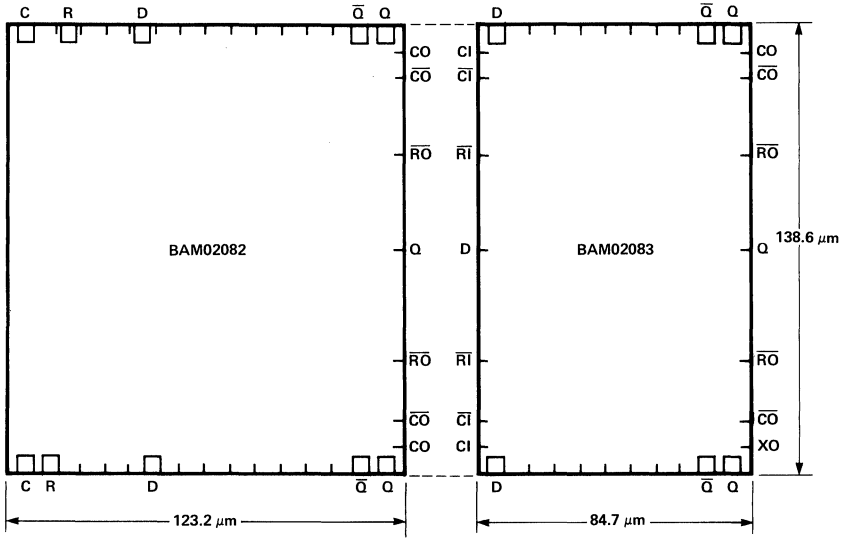
t_{DH} = 0.0

Maximum Clock Rate:

$f_{CLK} = \frac{1}{t_{CLK}} = 80$ MHz

(Times in nsec, C_L in pF)

Outline Drawings



D-Type Flip-Flop with Set and Reset

BAM00084

Description

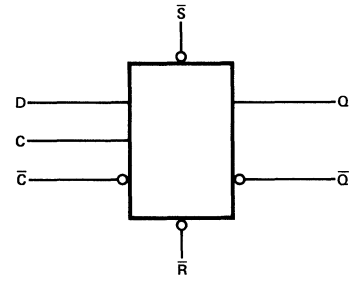
The BAM00084 is an HCMOS cell which performs the function of a standard D-type flip-flop with negative-true set and reset controls. It is used to implement a variety of logic functions, such as storage registers, counters, and shift registers.

Cell Parameters

Parameter	Value	Unit
Cell Width	130.9	μm
Cell Height	69.3	μm
Cell Area	9.1K	sq. μm
Average Power Dissipation*	11.0	μW/MHz
Input Capacitance (C, $\overline{C}$)	0.090	pF
Input Capacitance ($\overline{S}$, $\overline{R}$)	0.110	pF
Input Capacitance (D)	0.025	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Logic Symbol

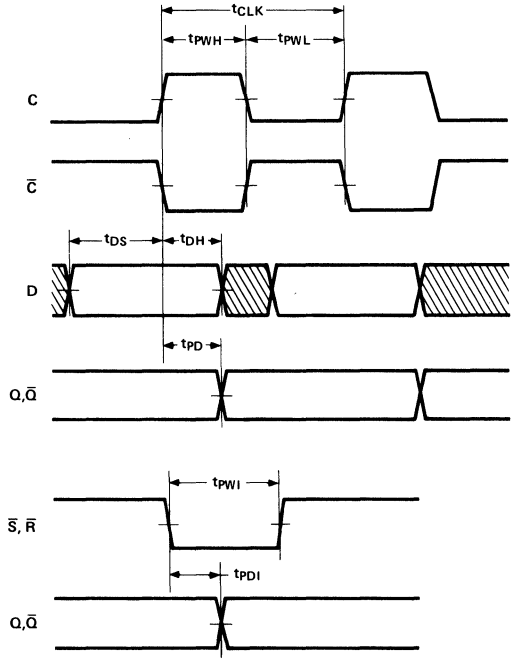


Function Table

Inputs					Outputs	
$\overline{S}$	$\overline{R}$	C	$\overline{C}$	D	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
H	H	⌐	⌙	H	⌐	⌙
H	H	⌐	⌙	L	⌙	⌐

X = "Don't care".
H = High level.
L = Low level.
⌐ = Low-to-High Transition.
⌙ = High-to-Low Transition.

Dynamic Characteristics



Maximum Propagation Delays:

$t_{PDI} = 15\ (C_L) + 5$

$t_{PD} = 15\ (C_L) + 7$

Minimum Pulse Widths:

t_{PWI} = 10 nsec

t_{PWH} = 10 nsec

t_{PWL} = 10 nsec

Minimum Set-up and Hold Times:

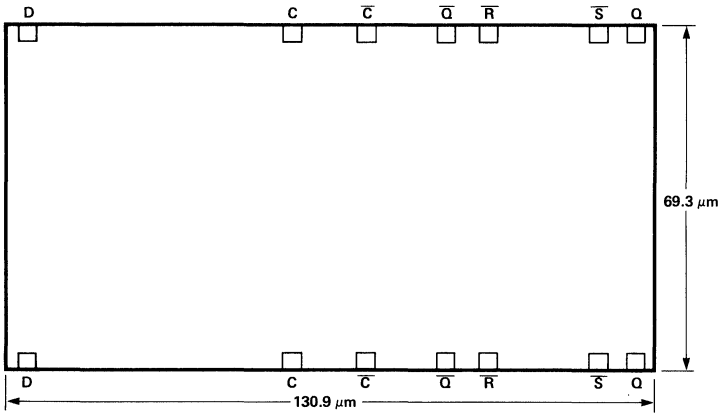
t_{DS} = 10 nsec

t_{DH} = 0 nsec

Maximum Clock Rate:

$f_{CLK} = \frac{1}{t_{CLK}} = 50$ MHz

Outline Drawing



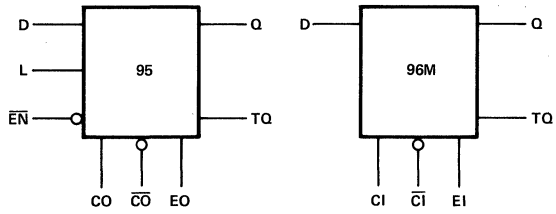
Transparent D-Latch with Three-State Output

BAM00095/96

Description

The BAM00095/96 are HCMOS cells which perform the function of a transparent D-type latch. They are very similar to the BAM00080 except that they have a three-state Q output in addition to the normal Q output. The BAM00095 is intended as the first stage in a group of latches with common Clock and Output Enables and the BAM00096 is used as a subsequent stage.

Logic Symbols

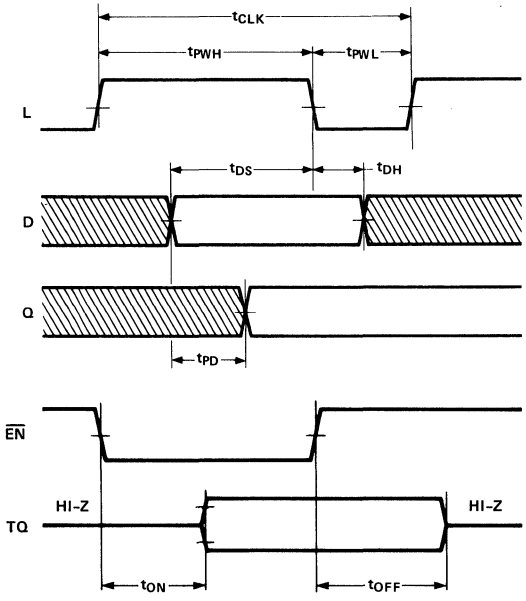


Cell Parameters

Parameter	Value BAM00095	Value BAM00096	Unit
Cell Width	84.7	53.9	μm
Cell Height	138.6	138.6	μm
Cell Area	11.7K	7.5K	sq. μm
Average Power Dissipation*	**	11.0	μW/MHz
Input Capacitance (L, $\overline{EN}$)	0.130	—	pF
Input Capacitance (D)	0.040	0.040	pF
Output Capacitance (TQ)	0.070	0.070	pF

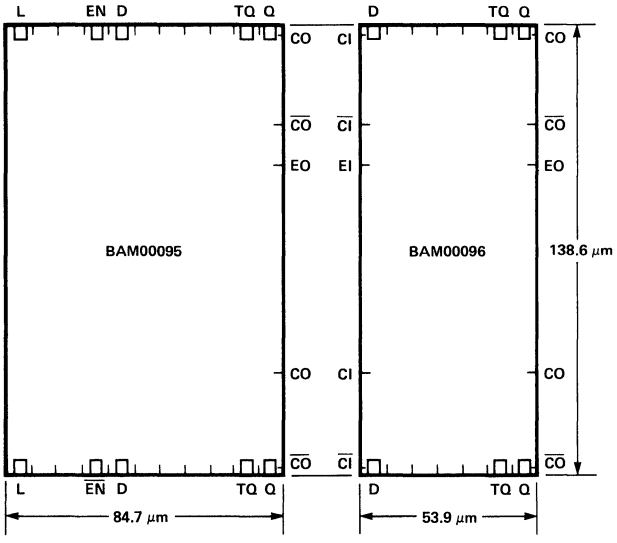
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.
**PDISS = 30 + 3.5n μW/MHz, where n = number of BAM00096 stages.

Dynamic Characteristics



Minimum Pulse Widths:
t_{PWH} = 20 nsec
t_{PWL} = 20 nsec
Minimum Set-up and Hold Times:
t_{DS} = 10 nsec
t_{DH} = 0 nsec
Maximum Propagation Delays (in nsec):
t_{PD} = 15 (C_L) + 7 nsec
t_{ON} = 2.0 nsec
t_{OFF} = 2.0 nsec
Maximum Clock Rate:
$f_{CLK} = \frac{1}{t_{CLK}}$ = 25 nsec

Outline Drawings



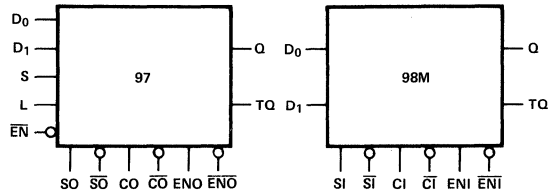
D-Latch with Three-State Output and Data Select

BAM00097/98

Description

The BAM00097/98 are HCMOS cells which perform the function of a transparent D-type Latch. They are very similar to the BAM00095/96 except that they have a selectable D data input. The BAM00097 is intended as the first stage in a group of latches with common Clock, Output Enable, and Data Select and the BAM00098 is used as a subsequent stage.

Logic Symbol



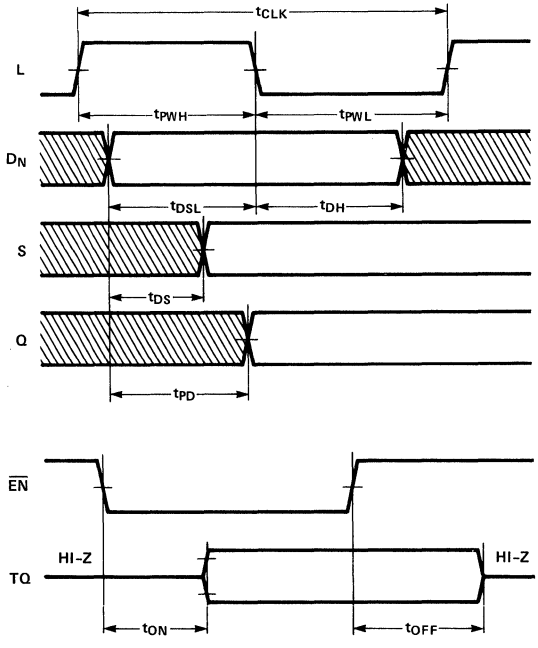
Cell Parameters

Parameter	BAM00097	BAM00098	Unit
Cell Width	161.7	92.4	μm
Cell Height	138.6	138.6	μm
Cell Area	22.4K	12.8K	Sq. μm
Average Power Dissipation*	**	11.0	μW/MHz
Input Capacitance (L, $\overline{EN}$, S)	0.130	—	pF
Input Capacitance (D_n)	0.070	0.070	pF
Output Capacitance (TQ)	0.070	0.070	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

**P_{DISS} = 30 + 3.5n μW/MHz, where n = number of BAM00098 stages.

Dynamic Characteristics



Data Select Logic

Select Input (S)	Active Data Input
L	D_1
H	D_0

H = High level.
L = Low level.

Minimum Pulse Widths:
t_{PWH} = 20 nsec
t_{PWL} = 20 nsec

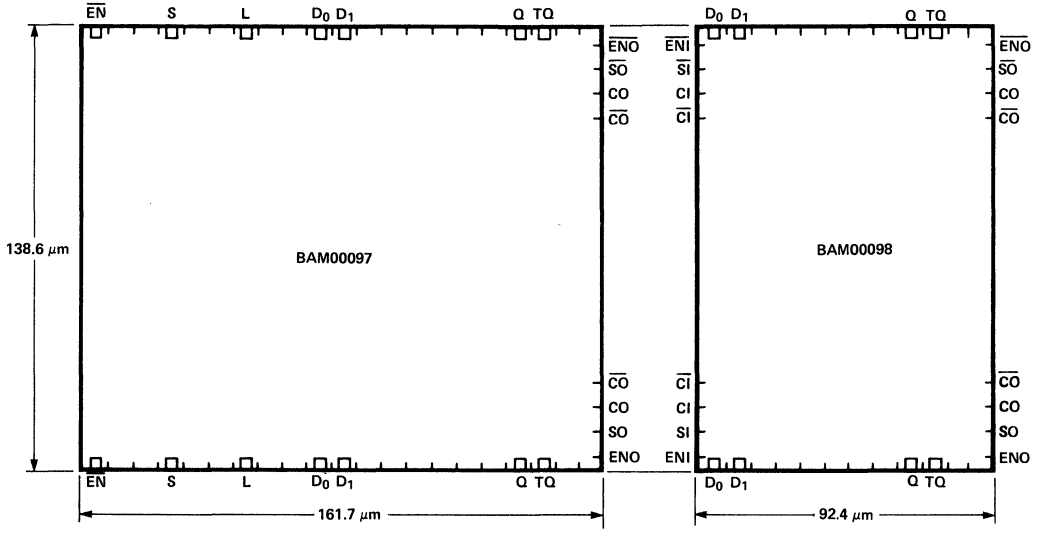
Minimum Set-up and Hold Times:
t_{DSL} = 10 nsec
t_{DSS} = 5 nsec
t_{DH} = 0 nsec

Maximum Propagation Delays:
t_{PD} = 15 (C_L) + 7 nsec (C_L in pF)
t_{ON} = 2.0 nsec
t_{OFF} = 2.0 nsec

Maximum Clock Rate:

$$f_{CLK} = \frac{1}{t_{CLK}} = 25\,\text{MHz}$$

Outline Drawing



D Flip-Flop without Set or Reset

BAM00103

Description

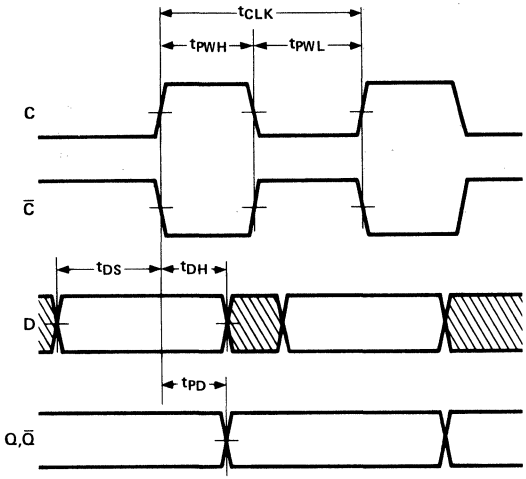
The BAM00103 is a D-type Flip-Flop without set or reset. It is similar to the BAM00084 cell function and, like that cell, it is 99 μm high.

Cell Parameters

Parameter	Value	Unit
Cell Width	92.4	μm
Cell Height	69.3	μm
Cell Area	6.4K	Sq. μm
Average Power Dissipation*	11.0	μW/MHz
Input Capacitance (C, $\overline{C}$)	0.090	pF
Input Capacitance (D)	0.025	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Dynamic Characteristics



Maximum Propagation Delays (in nsec):

t_{PD} = 15 (C_L) + 7 nsec

Minimum Pulse Widths:

t_{PWI} = 10 nsec

t_{PWH} = 10 nsec

t_{PWL} = 10 nsec

Minimum Set-up and Hold Times:

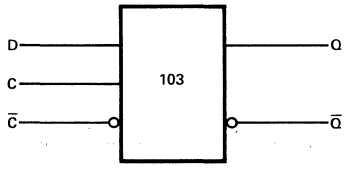
t_{DS} = 10 nsec

t_{DH} = 0 nsec

Maximum Clock Rate:

$f_{CLK} = \frac{1}{t_{CLK}} = 50$ nsec

Logic Symbol

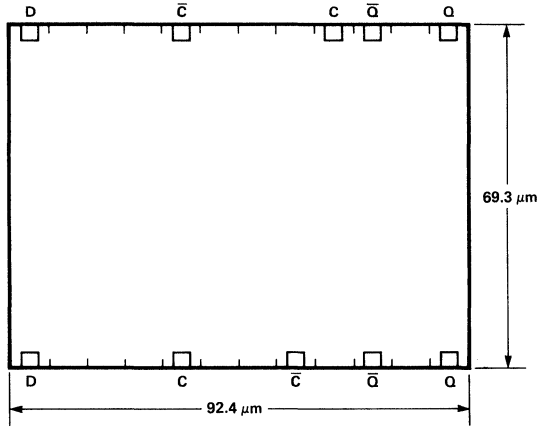


Function Table

Inputs			Outputs	
C	$\overline{C}$	D	Q	$\overline{Q}$
X	X	X	H	L
X	X	X	L	H
⌐	¬	H	⌐	¬
⌐	¬	L	¬	⌐

X = "Don't care".
H = High level.
L = Low level.
⌐ = Low-to-high transition.
¬ = High-to-low transition.

Outline Drawing



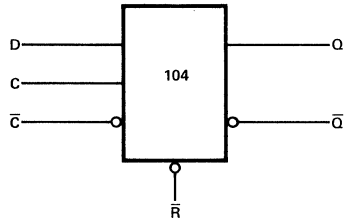
D Flip-Flop with Reset

BAM00104

Description

The BAM00104 is a D-type Flip-Flop with reset. It is similar to the BAM00084 cell in its function and, like that cell, it is 99 μm high.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	123.2	μm
Cell Height	69.3	μm
Cell Area	8.5K	sq. μm
Average Power Dissipation*	11.0	μW/MHz
Input Capacitance (C, $\overline{C}$)	0.090	pF
Input Capacitance (R)	0.120	pF
Input Capacitance (D)	0.025	pF

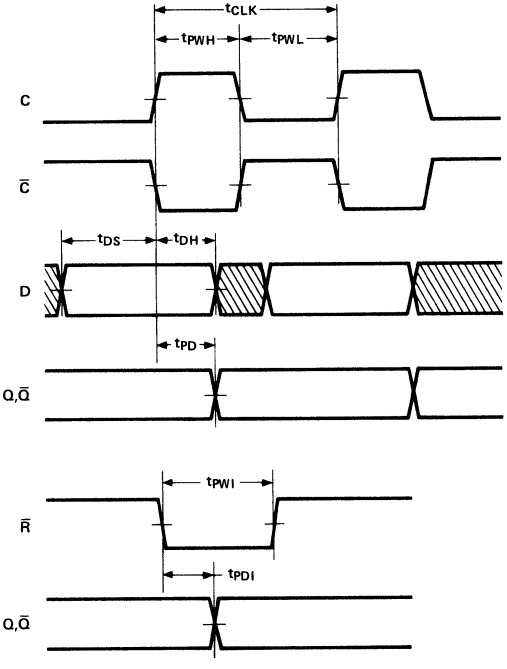
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs				Outputs	
$\overline{R}$	C	$\overline{C}$	D	Q	$\overline{Q}$
H	X	X	X	H	L
L	X	X	X	L	H
H	↑	↓	H	↑	↓
H	↑	↓	L	↓	↑

X = "Don't care".
H = High level.
L = Low level.
↑ = Low-to-high transition.
↓ = High -to-low transition.

Dynamic Characteristics



Maximum Propagation Delays (in nsec):

$t_{PDI} = 15\ (C_L) + 5$nsec

$t_{PD} = 15\ (C_L) + 7$ nsec

Minimum Pulse Widths:

$t_{PWI} = 10$ nsec

$t_{PWH} = 10$ nsec

$t_{PWL} = 10$ nsec

Minimum Set-up and Hold Times:

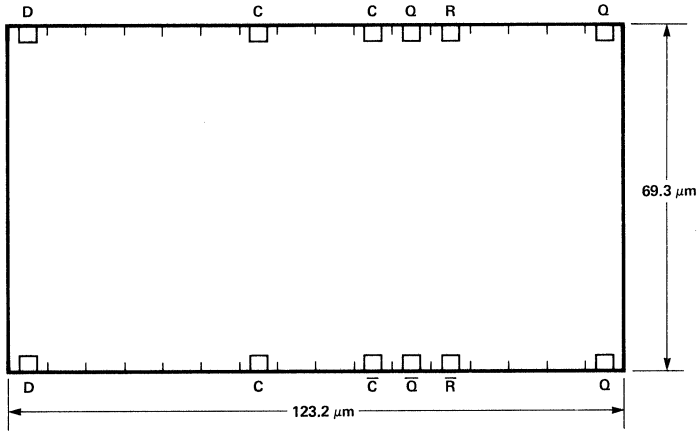
$t_{DS} = 10$ nsec

$t_{DH} = 0$ nsec

Maximum Clock Rate:

$$f_{CLK} = \frac{1}{t_{CLK}} = 50 \text{ nsec}$$

Outline Drawing



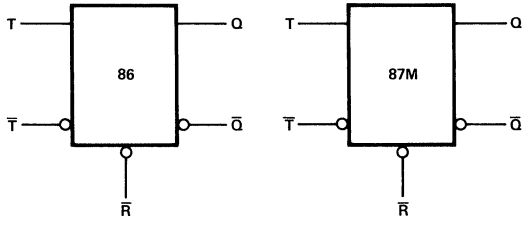
T Flip-Flop with Reset

BAM00086/87

Description

The BAM00086/87 are HCMOS cells which perform the function of a toggle flip-flop with negative-true reset control. The two cells are identical in their electrical function and characteristics and differ only in their physical layouts. The BAM00086 is intended for use as the first stage of a counter chain and, as such, all inputs and outputs are accessible. The BAM00087, on the other hand, is intended for use as a subsequent stage in a counter chain. Thus, only its Q and $\overline{Q}$ outputs are accessible. Clocks and Reset are internally common to all stages and are accessible only in the first stage of the counter.

Logic Symbol

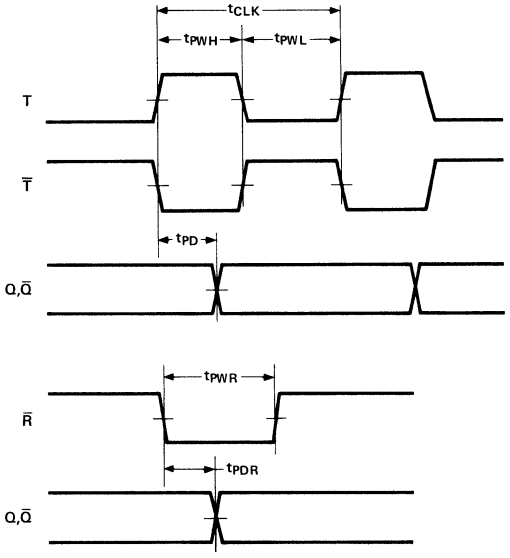


Cell Parameters

Parameter	Value BAM00086	Value BAM00087	Unit
Cell Width	92.4	61.6	μm
Cell Height	138.6	138.6	μm
Cell Area	12.8K	8.5K	sq. μm
Average Power Dissipation*	9.0	9.0	μW/MHz
Input Capacitance (T, $\overline{T}$)	0.120	0.120	pF
Input Capacitance ($\overline{R}$)	0.150	0.150	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Dynamic Characteristics



Function Table

Inputs R̄	Inputs T	Inputs T̄	Outputs Q	Outputs Q̄
L	X	X	L	H
H	↑	↓	$\overline{Q}_O$	Q_O

H = High level.
L = Low level.
X = "Don't care".
Q_O = The level of Q output prior to T, $\overline{T}$ transitions.

Minimum Pulse Widths:

t_{PWH} = 10 nsec

t_{PWL} = 10 nsec

t_{PWR} = 10 nsec

Maximum Propagation Delays:

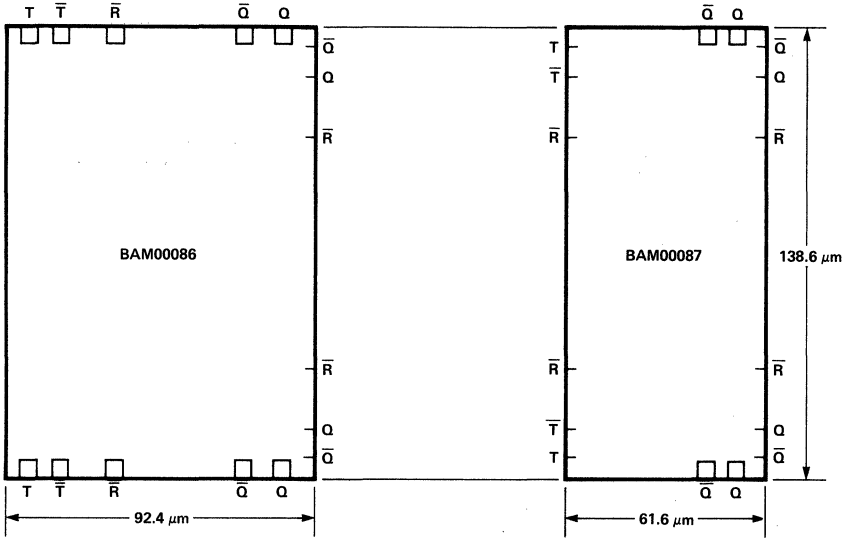
$t_{PD} = 15\ (C_L) + 7$ nsec

$t_{PDR} = 15\ (C_L) + 5$ nsec

Maximum Clock Rate:

$f_{CLK} = \frac{1}{t_{CLK}} = 50$ MHz

Outline Drawings



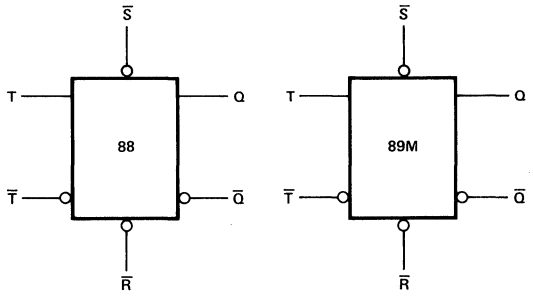
T Flip-Flop with Set and Reset

BAM00088/89

Description

The BAM00088/89 are HCMOS cells which perform the function of a toggle flip-flop with negative-true set and reset controls. The two cells are identical in their electrical function and characteristics and differ only in their physical layouts. The BAM00088 is intended for use as the first stage of a counter chain and, as such, all inputs and outputs are accessible. The BAM00089, on the other hand, is intended for subsequent stages and only the $\overline{S}$, $\overline{R}$, Q, and $\overline{Q}$ functions are accessible. Q and $\overline{Q}$ outputs are automatically connected to T and $\overline{T}$ inputs of the following stage when cells are abutted.

Logic Symbol

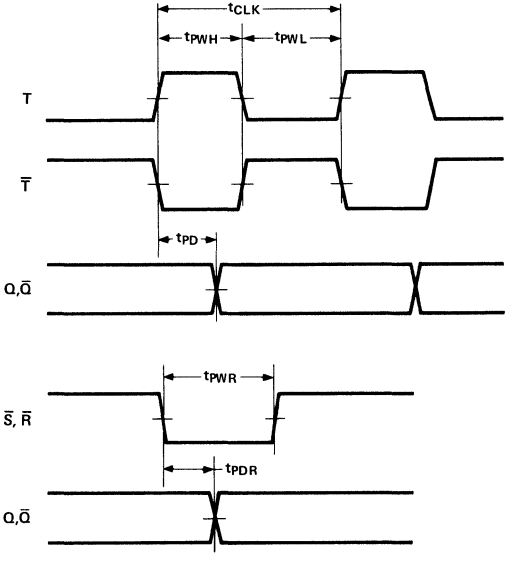


Cell Parameters

Parameter	Value BAM00088	BAM00089	Unit
Cell Width	84.7	69.3	μm
Cell Height	138.6	138.6	μm
Cell Area	11.7K	9.6K	sq. μm
Average Power Dissipation*	11.0	11.0	μW/MHz
Input Capacitance (T, $\overline{T}$)	0.120	0.120	pF
Input Capacitance ($\overline{S}$, $\overline{R}$)	0.130	0.130	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Dynamic Characteristics



Function Table

Inputs $\overline{S}$	$\overline{R}$	T	$\overline{T}$	Outputs Q	$\overline{Q}$
L	H	X	X	L	H
H	L	X	X	H	L
H	H	↓	↑	$\overline{Q}_O$	Q_O

H = High level.
L = Low level.
X = "Don't care".
Q_O = The level of Q output prior to T, $\overline{T}$ transitions.

Minimum Pulse Widths:

t_{PWH} = 10 nsec

t_{PWL} = 10 nsec

t_{PWR} = 10 nsec

Maximum Propagation Delays:

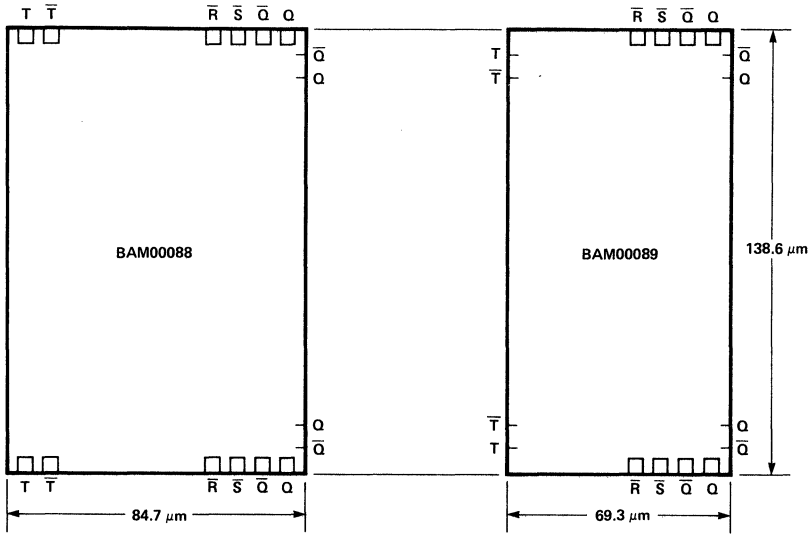
$t_{PD} = 15\ (C_L) + 5$ nsec

$t_{PDR} = 15\ (C_L) + 7$ nsec

Maximum Clock Rate:

$$f_{CLK} = \frac{1}{t_{CLK}} = 50 \text{ MHz}$$

Outline Drawings



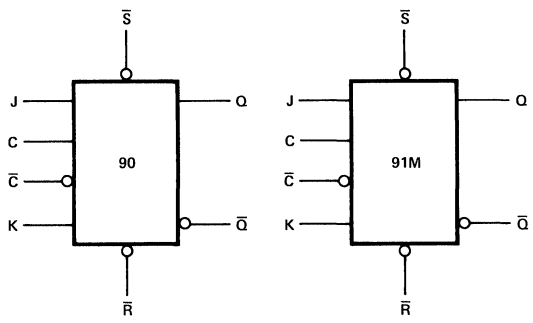
J-K Flip-Flop with Set and Reset

BAM00090/91

Description

The BAM00090/91 cells are HCMOS cells which perform the function of standard J-K flip-flops with negative-true set and reset controls. The two cells are identical in their electrical functions and characteristics and differ only in their physical layouts. The BAM00090 is intended as the first stage of a counter chain and has all inputs and outputs accessible. The BAM00091, on the other hand, is intended for use as a following stage and only $\overline{S}$, $\overline{R}$, Q, and $\overline{Q}$ are accessible. Clocks are internally common to all stages and are connected to following stages when the cells are abutted.

Logic Symbol



Cell Parameters

Parameter	Value BAM00090	Value BAM00091	Unit
Cell Width	123.2	107.8	μm
Cell Height	138.6	138.6	μm
Cell Area	17.1K	14.9K	sq. μm
Average Power Dissipation*	26.0	26.0	μW/MHz
Input Capacitance (C, $\overline{C}$)	0.160	0.160	pF
Input Capacitance ($\overline{S}$, $\overline{R}$)	0.190	0.190	pF
Input Capacitance (J, K)	0.110	0.110	pF

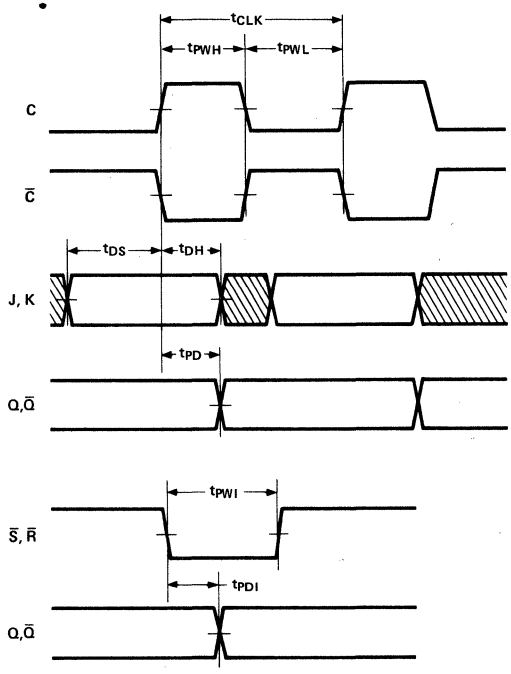
*V_{DD} = 5.0V, T_A = 25°C, C_L = 0.050 pF.

Function Table

Inputs						Outputs	
$\overline{S}$	$\overline{R}$	C	$\overline{C}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	X	H	L
H	L	X	X	X	X	L	H
L	L	X	X	X	X	H	L
H	H	⌐	⌙	L	L	Q_O	$\overline{Q_O}$
H	H	⌐	⌙	L	H	L	H
H	H	⌐	⌙	H	L	H	L
H	H	⌐	⌙	H	H	$\overline{Q_O}$	Q_O

H = High level.
L = Low level.
X = "Don't care".
Q_O = The level of Q output just prior to low-to-high C transition.
⌐ = Low-to-high transition.
⌙ = High-to-low transition.

Dynamic Characteristics



Maximum Propagation Delays (in nsec):

$t_{PDI} = 10\ (C_L) + 5$ nsec

$t_{PD} = 10\ (C_L) + 7$ nsec

Minimum Pulse Widths:

$t_{PWI} = 10$ nsec

$t_{PWH} = 10$ nsec

$t_{PWL} = 10$ nsec

Minimum Set-up and Hold Times:

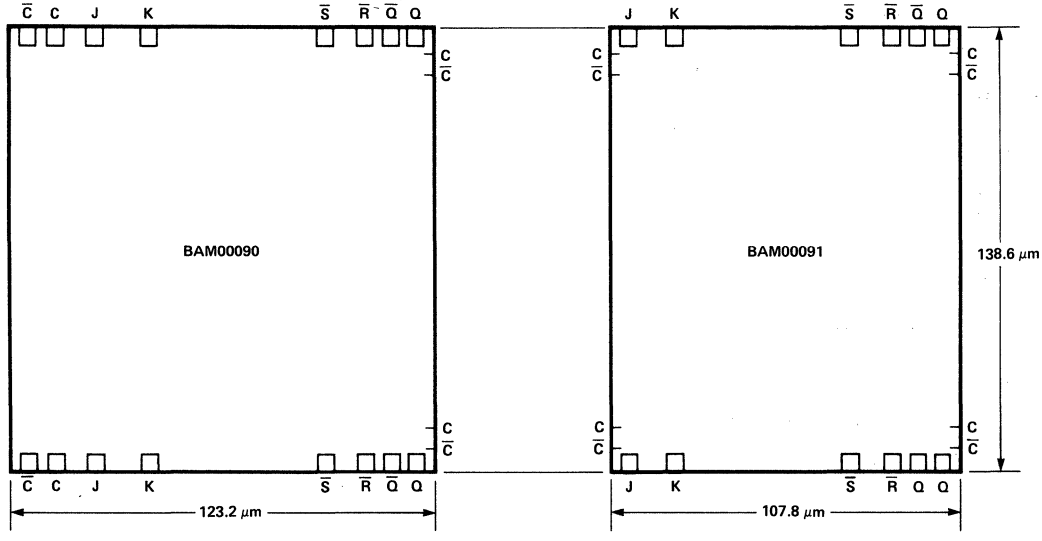
$t_{DS} = 10$ nsec

$t_{DH} = 0$ nsec

Maximum Clock Rate:

$f_{CLK} = \frac{1}{t_{CLK}} = 50$ MHz

Outline Drawings



S-R Latch

BAM00092

Description

The BAM00092 is an HCMOS cell which performs the function of a set-reset latch.

Function Table

Inputs		Outputs	
$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
H	L	H	L
L	H	L	H
H	H	Q_O	$\overline{Q}_O$
L	L	H	H

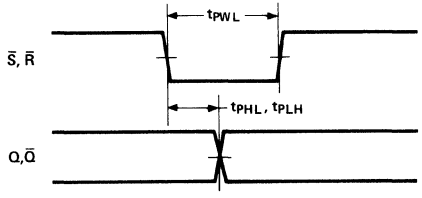
H = High level.
L = Low level.
x = "Don't care".
Q_O = The level of Q output just prior to $\overline{S}$ or $\overline{R}$ going from low to high.

Cell Parameters

Parameter	Value	Unit
Cell Width	38.5	μm
Cell Height	69.3	μm
Cell Area	2.7K	sq. μm
Average Power Dissipation*	7.0	μW/MHz
Input Capacitance	0.050	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Dynamic Characteristics



Minimum Pulse Width:

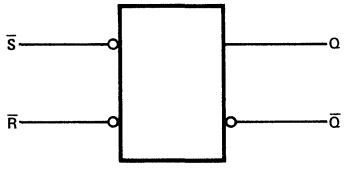
t_{PWL} = 15 nsec

Maximum Propagation Delays:

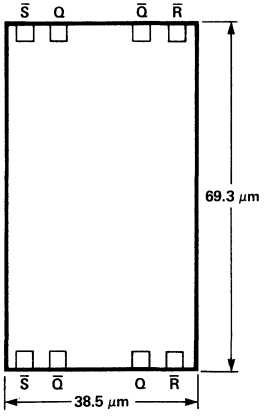
t_{PHL} = 10 (C_L) + 3 nsec

t_{PLH} = 20 (C_L) + 7 nsec

Logic Symbol



Outline Drawing



High-Speed Set-Reset Latch

BAM02092

Description

The BAM02092 is a high-speed version of the BAM00092 S-R Latch.

Function Table

Inputs		Outputs	
$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
H	L	H	L
L	H	L	H
H	H	Q_O	$\overline{Q}_O$
L	L	H	H

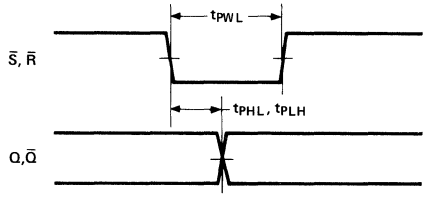
H = High level.
L = Low level.
x = "Don't care".
Q_O = The level of Q output just prior to $\overline{S}$ or $\overline{R}$ going from low to high.

Cell Parameters

Parameter	Value	Unit
Cell Width	53.9	μm
Cell Height	69.3	μm
Cell Area	3.7K	sq. μm
Average Power Dissipation*	15	μW/MHz
Input Capacitance	0.140	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Dynamic Characteristics



Minimum Pulse Width:

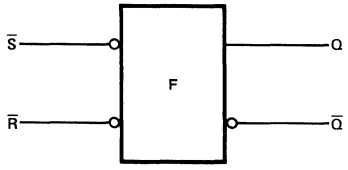
t_{PWL} = 10 nsec

Maximum Propagation Delays (in nsec):

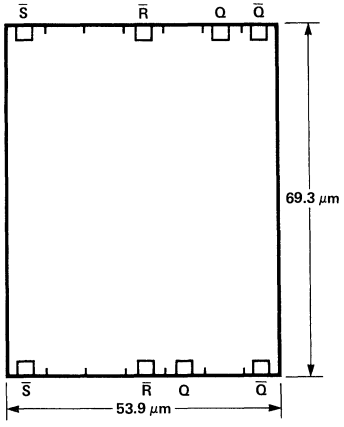
$t_{PHL} = 8.0\ (C_L) + 3.0$

$t_{PLH} = 3.0\ (C_L) + 1.5$

Logic Symbol



Outline Drawing



Parallel Load Shift Register Front End

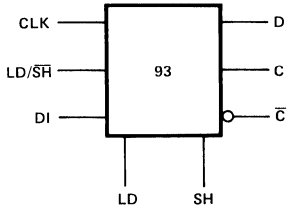
BAM00093

Description

The BAM00093 is an HCMOS cell which provides the front end logic required for a parallel load shift register (BAM00094 Shift Register cells). It is used to generate clock signals (C and $\overline{C}$), shift and load controls (SH and LD), and input data (D) for the first stage of the shift register.

The clocks (C and $\overline{C}$) are generated from the CLK input and provide for high drive output capability (needed to drive a multiple-stage shift register). The LD/$\overline{SH}$ input selects either Load (LD/$\overline{SH}$ = High) or Shift (LD/$\overline{SH}$ = Low) mode. LD and SH are both positive-true outputs. Further, when Load mode is selected, C and $\overline{C}$ are asserted to allow for proper operation of parallel loading. Finally, the D output follows the DI input directly.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	61.6	μm
Cell Height	138.6	μm
Cell Area	8.5K	sq. μm
Average Power Dissipation*	26.0	μW/MHz
Input Capacitance (CLK)	0.270	pF
Input Capacitance (LD/SH)**	0.300	pF
Input Capacitance (DI)**	0.050	pF

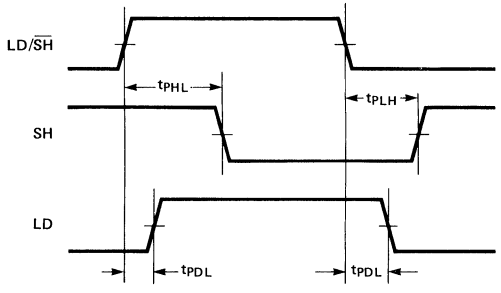
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

**Internal to this cell, only. Output load capacitance must be added to give total input capacitance.

Function Table

(See BAM00094 data sheet for full functional description).

Dynamic Characteristics



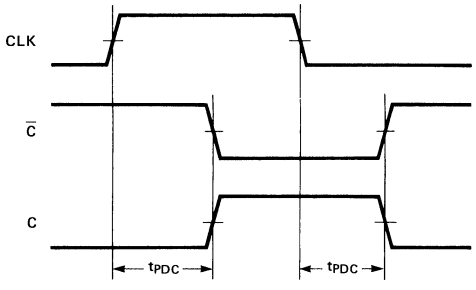
Propagation Delays (in nsec):

t_{PHL} = 3 + 1.5N

t_{PLH} = 2 + 0.3N

t_{PDL} = 0

(N = Number of shift register stages to be driven).

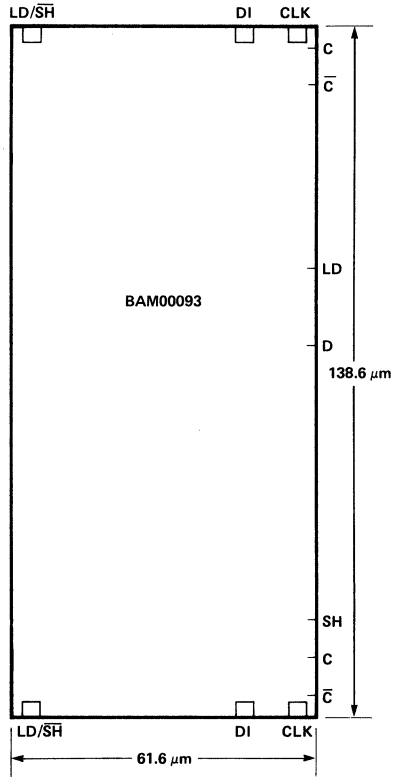


Propagation Delays (in nsec):

t_{PDC} = 2 + 0.2N

(N = Number of shift register stages to be driven).

Outline Drawing



Parallel Load Shift Register — Shift Stage

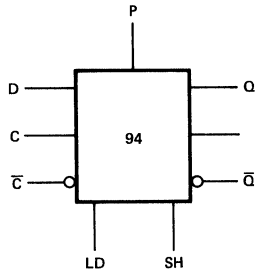
BAM00094

Description

The BAM00094 is an HCMOS cell which performs the function of a parallel load shift register. It is a single bit and can be cascaded with identical cells by abutted placement. The first stage of a cascaded series of cells is driven by the BAM00093 Front End Cell which contains the necessary control elements and has adequate drive capability.

Each shift register cell has clock inputs (C and $\overline{C}$), shift and load controls (SH and LD), and the serial data input (D). These functions are all abutted inputs. The abutted outputs are clocks, shift and load controls, and the serial data output (Q). In addition, there are three connections which are accessible at non-abutted contacts. They are Q and $\overline{Q}$ outputs and the parallel data input (P).

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	92.4	μm
Cell Height	138.6	μm
Cell Area	12.8K	sq. μm
Average Power Dissipation*	11.0	μW/MHz
Input Capacitance (C, $\overline{C}$)**	0.110	pF
Input Capacitance (LD, SH)**	0.080	pF
Input Capacitance (D)	0.050	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.
**Internal to this cell, only. Output load capacitance must be added to give total effective input capacitance, since inputs feed through to outputs.

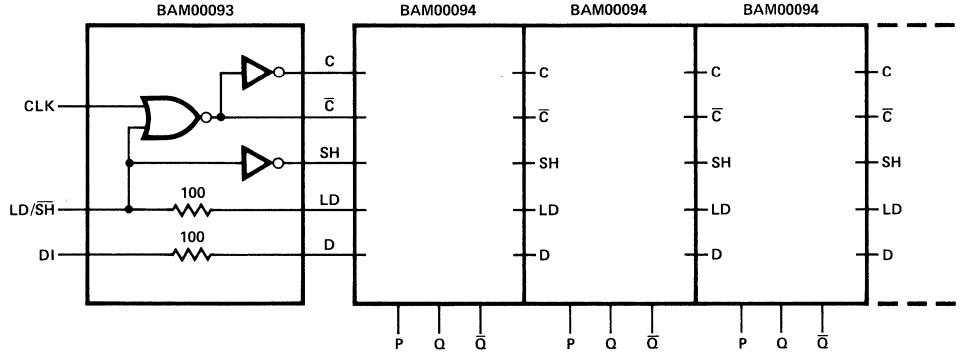
Pin Functions

C, $\overline{C}$
Free-running complementary clock inputs.

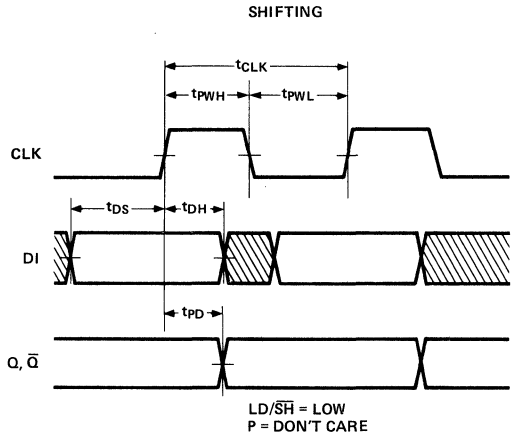
SH, LD
Positive-true shift and load control inputs. When SH is high, normal shifting of D data occurs on positive edge of C input (LD must be low when SH is high). When LD is high (SH must be low), data on P is loaded into cells and latched on negative edge of LD. Note that the C and $\overline{C}$ are both asserted by the BAM00093 cell when LD is selected, a requirement for cells to load.

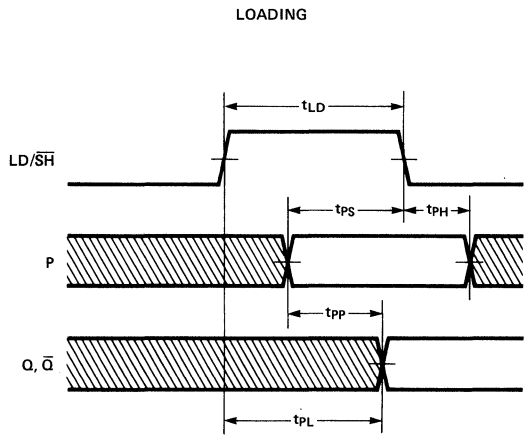
P, D
Parallel and serial data inputs, respectively.

Q, $\overline{Q}$
Complementary data outputs.



Dynamic Characteristics





$f_{CLK} = \frac{1}{t_{CLK}} = 50$ MHz (max)

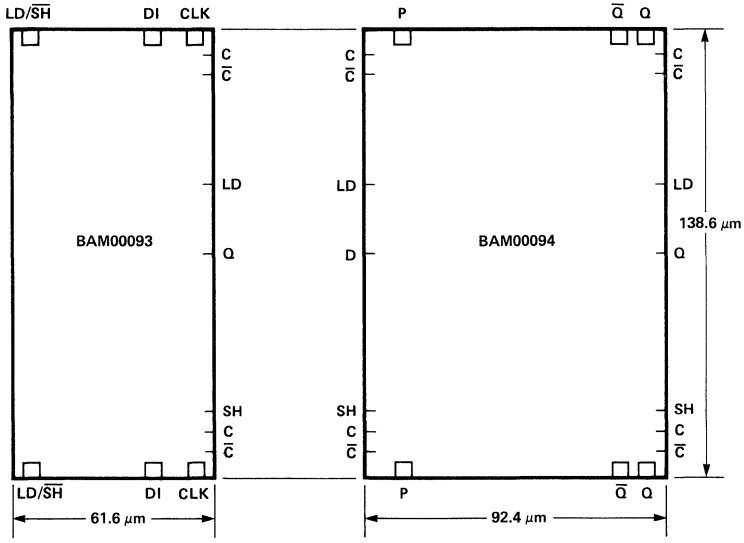
$t_{PWH} = t_{PWL} = 10$ nsec (min)
$t_{DS} = 10$ nsec (min)
$t_{DH} = 0$ nsec (min)
$t_{PD} = 15\ (C_L) + 7$ nsec (max)

$t_{LD} = 20$ nsec (min)
$t_{PS} = 20$ nsec (min)
$t_{PH} = 0$ nsec (min)

$t_{PL} = 20$ nsec (max)
$t_{PP} = 20$ nsec (max)

Both must occur.

Outline Drawings



I/O Drivers/ Output Drivers/ Input Pads

11

Synertek.

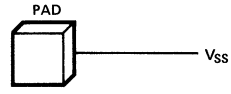
V_{SS} Pad

BAM00800

Description

The BAM00800 is a pad cell used for the connection to circuit ground (V_{SS}).

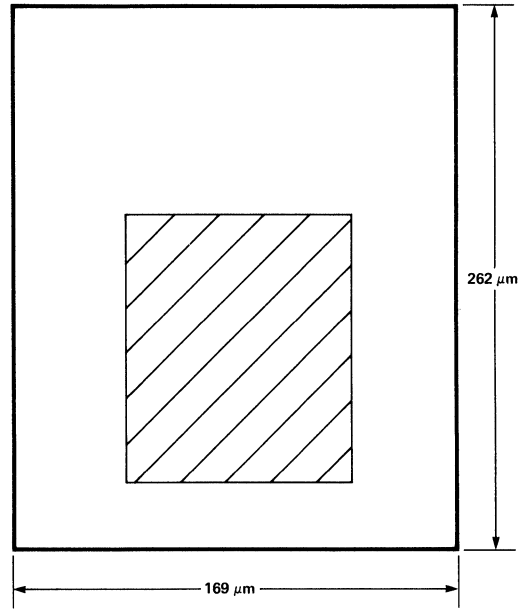
Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	169	μm
Cell Height	262	μm
Cell Area	44.3K	sq. μm
Average Power Dissipation	0	μW/MHz
Pad Capacitance	1.0	pF

Outline Drawing



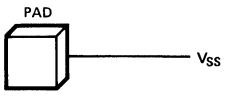
V_{SS} Pad

BAM00801

Description

The BAM00801 is a pad cell that is used for the connection to circuit ground (V_{SS}). It is identical to the BAM00800, except for the cell height.

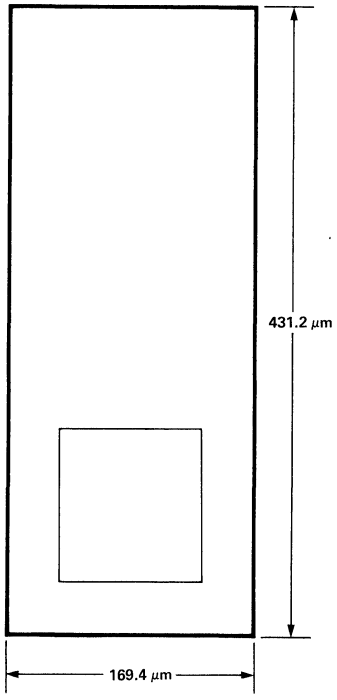
Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	169.4	μm
Cell Height	431.2	μm
Cell Area	73K	Sq. μm
Average Power Dissipation	0	μW/MHz
Pad Capacitance	1.4	pF

Outline Drawing



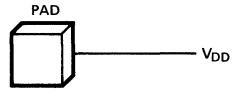
V_{DD} Pad

BAM00810

Description

The BAM00810 is a pad cell which is used for the connection to circuit power (V_{DD}).

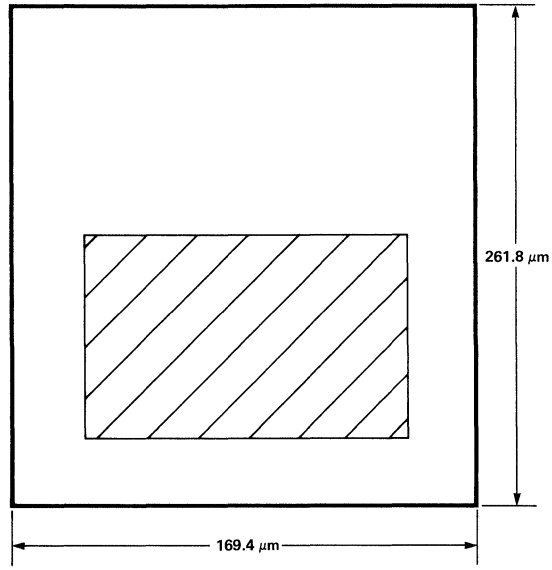
Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	169.4	μm
Cell Height	261.8	μm
Cell Area	44.3K	sq. μm
Average Power Dissipation	0	μW/MHz
Pad Capacitance	1.0	pF

Outline Drawing



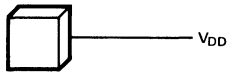
V_{DD} Pad

BAM00811

Description

The BAM00811 is a pad cell that is used for the connection to circuit power (V_{DD}). It is identical to the BAM00810, except for the cell height.

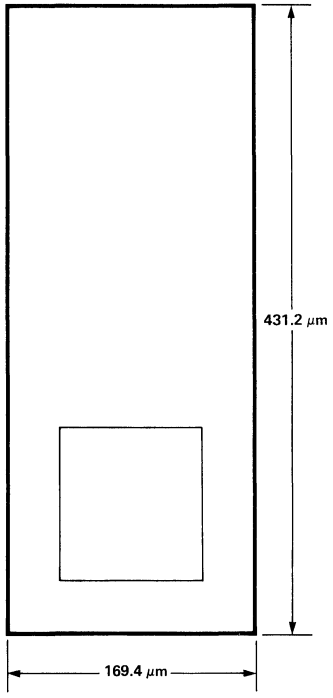
Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	169.4	μm
Cell Height	431.2	μm
Cell Area	73K	Sq. μm
Average Power Dissipation	0	μW/MHz
Pad Capacitance	1.0	pF

Outline Drawing



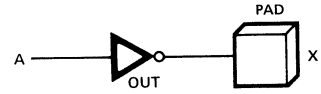
TTL/CMOS Output Driver

BAM00820

Description

The BAM00820 is an output driver cell for externally connected TTL or CMOS circuits. It consists of three successive push/pull inverter stages, each with progressively higher drive capability than the preceding stage.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	585	μm
Cell Height	262	μm
Cell Area	153K	sq. μm
Average Power Dissipation*	450 + 25 (C)	μW/MHz
Input Capacitance	0.320	pF

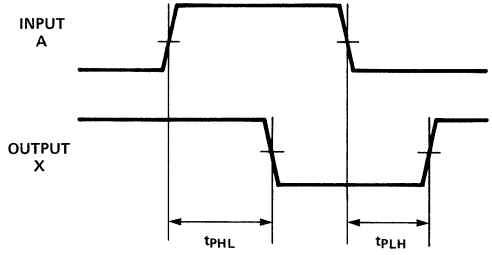
*V_{DD} = 5.0V, T_A = 25° C, C_L in pF.

Function Table

Input A	Output A
L	H
H	L

H = High level.
L = Low level.

Dynamic Characteristics

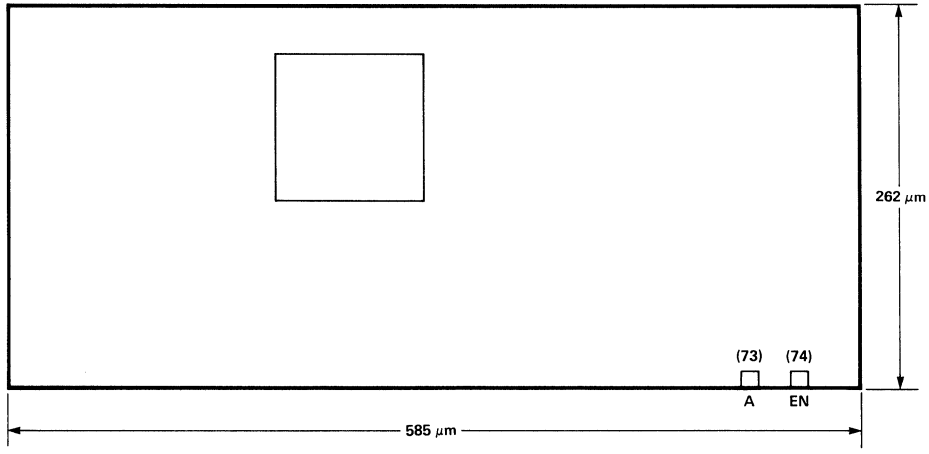


Propagation Delays (in nsec):

$t_{PHL} = 10$
$t_{PLH} = 10$ } 1 TTL Load

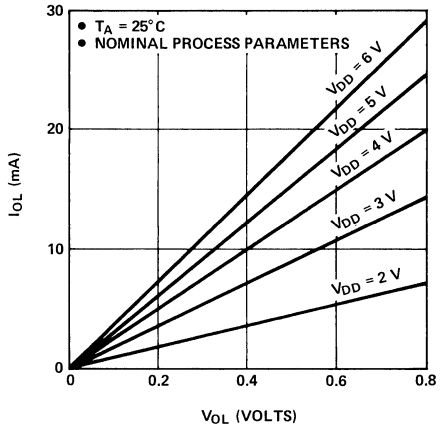
$t_{PHL} = 0.84\ (C_L) + 5$
$t_{PLH} = 0.04\ (C_L) + 5$ } CMOS Load (High-Z)

Outline Drawing

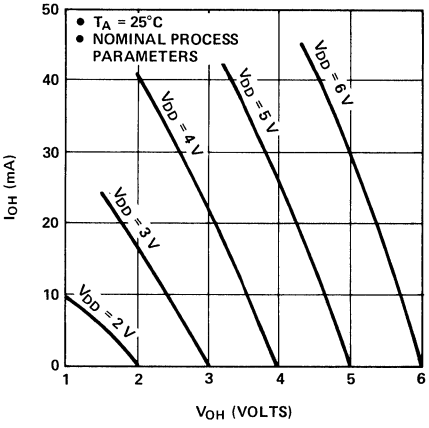


Output Drive Characteristics

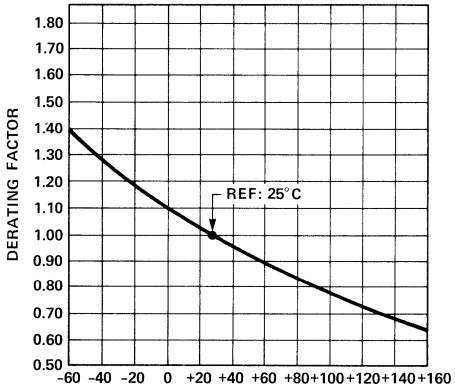
I_{OL} vs. V_{OL}



I_{OH} vs. V_{OH}



I_{OH}/I_{OL} DE-RATING FACTOR VS. TEMPERATURE



Process De-Rating Factors:

Worst-Case = 0.80

Nominal = 1.00

Best-Case = 1.25

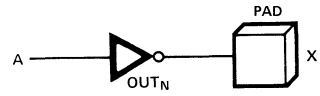
TTL/CMOS Output Driver

BAM00822

Description

The BAM00822 is an output driver cell for externally connected TTL or CMOS circuits. It consists of three successive push/pull inverter stages, each with progressively higher drive capability than the preceding stage.

Logic Symbol



N = 3 for BAM00822

Cell Parameters

Parameter	Value	Unit
Cell Width	177.1	μm
Cell Height	431.2	μm
Cell Area	76.4K	sq. μm
Average Power Dissipation*	150 + 25(C_L)	μW/MHz
Input Capacitance	0.160	pF

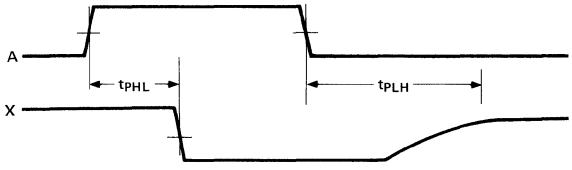
*V_{DD} = 5.0V, T_A = 25° C, C_L in pF.

Function Table

Input A	Output X
L	H
H	L

H = High level.
L = Low level.

Dynamic Characteristics

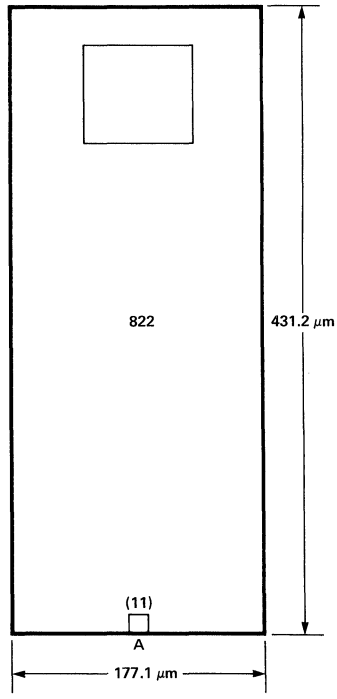


Propagation Delays (in nsec):

t_{PHL} = 8 nsec
t_{PLH} = 12 nsec
} 1 TTL Load

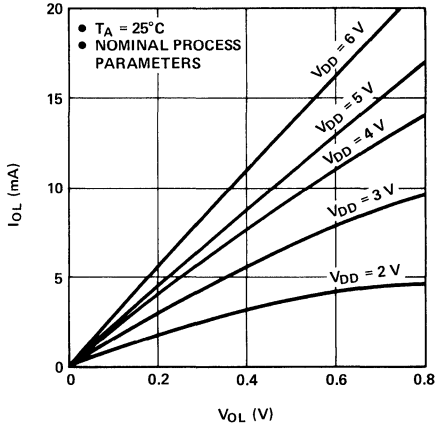
t_{PHL} = 0.08 (C_L) + 4
t_{PLH} = 0.25 (C_L) + 5
} CMOS Load

Outline Drawing

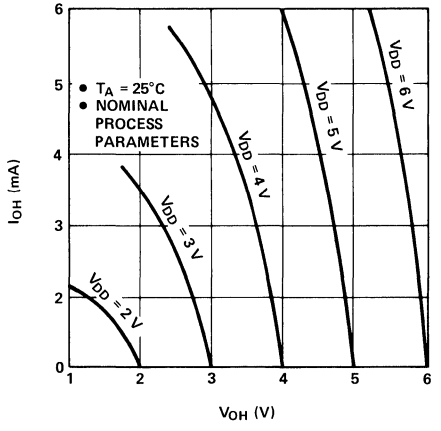


Output Drive Characteristics

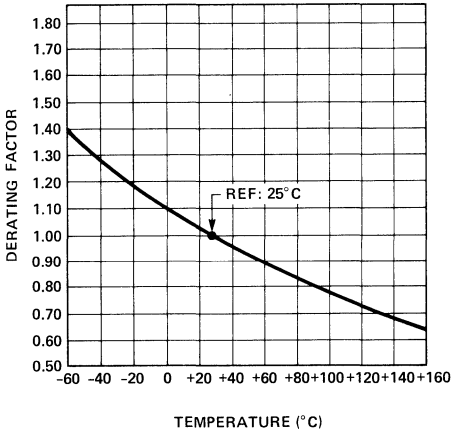
I_{OL} vs. V_{OL}



I_{OH} vs. V_{OH}



I_{OH}/I_{OL} DE-RATING FACTOR VS. TEMPERATURE



Process De-Rating Factors:
Worst-Case = 0.80
Nominal = 1.00
Best-Case = 1.25

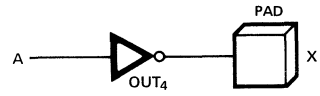
TTL/CMOS Output Driver

BAM00823

Description

The BAM00823 is an output driver pad for externally connected TTL or CMOS circuits. It is electrically identical to the BAM000820 and differs only in its physical shape.

Logic Symbol



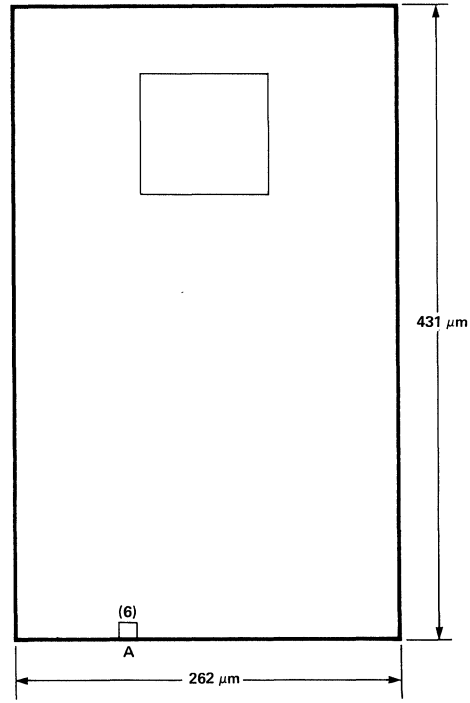
Cell Parameters

Parameter	Value	Unit
Cell Width	262	μm
Cell Height	431	μm
Cell Area	113K	sq. μm
Average Power Dissipation*	450 + 25(C_L)	μW/MHz
Input Capacitance	0.320	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L in pF.

Note: Function Table, Dynamic Characteristics, Schematic, Models, and Output Drive Charts are all identical to BAM00820.

Outline Drawing



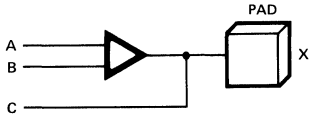
Versatile Output Pad Driver

BAM00824

Description

The BAM00824 is an INPUT/OUTPUT pad cell which only contains the push/pull output transistors. In this way, the cell size is minimized and it may be utilized in a variety of ways (for example, as three-state I/O driver or as push/pull driver).

Logic Symbol

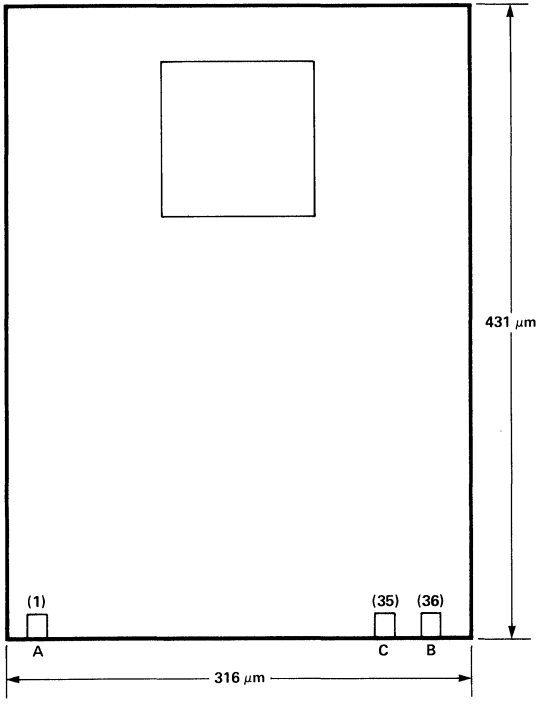


Cell Parameters

Parameter	Value	Unit
Cell Width	316	μm
Cell Height	431	μm
Cell Area	136K	sq. μm
Average Power Dissipation	*	μW/MHz
Input Capacitance (A, B)	8.4	pF
Pad Capacitance	1.0	pF

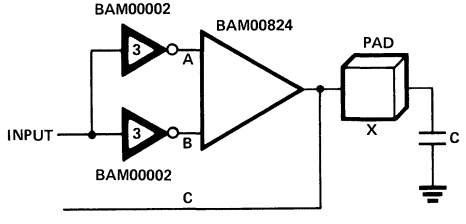
*Depends on application and output load.

Outline Drawing

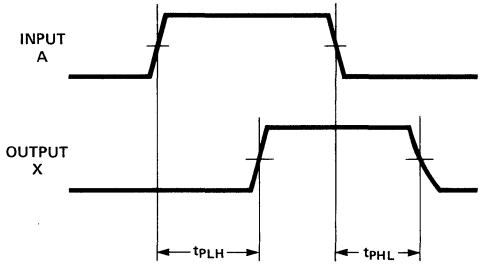


Simulation Example

Circuit



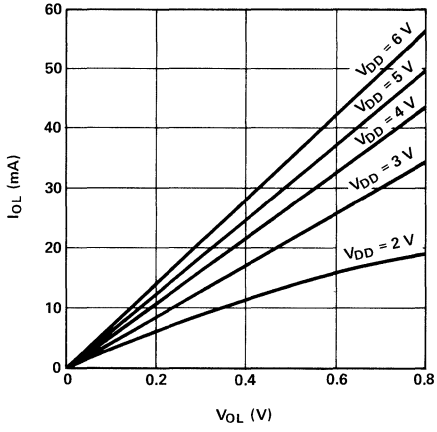
Waveforms



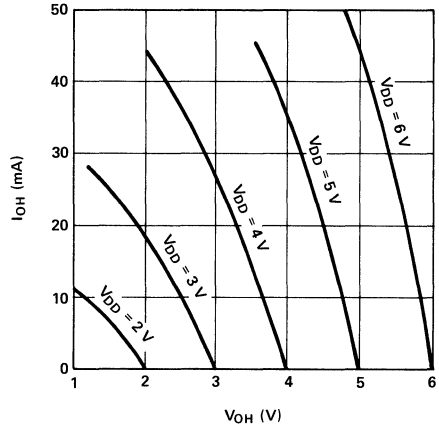
$t_{PLH} = 0.05\ (C_L) + 5.5$
$t_{PHL} = 0.03\ (C_L) + 5.0$
(t_{PXX} in nsec, C_L in pF).

Output Drive Characteristics

I_{OL} vs. V_{OL}



I_{OH} vs. V_{OH}



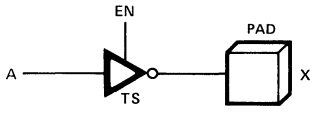
TTL/CMOS Three-State Output Driver

BAM00830

Description

The BAM00830 is an output driver cell for externally connected TTL or CMOS circuits. Additionally, its push/pull output stage may be switched to the high impedance state to facilitate bus connection applications. For I_{OL} and I_{OH} characteristics, refer to BAM00820.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	585	μm
Cell Height	262	μm
Cell Area	153K	sq. μm
Average Power Dissipation*	450 + 25(C_L)	μW/MHz
Input Capacitance (A)	0.500	pF
Input Capacitance (E_N)	0.330	pF

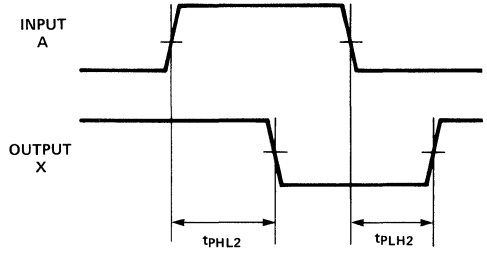
*V_{DD} = 5.0V, T_A = 25° C, C_L in pF.

Function Table

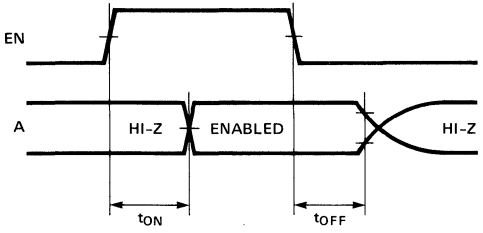
Inputs		Output
EN	A	X
L	X	Hi-Z
H	L	H
H	H	L

H = High level.
L = Low level.
X = "Don't care".
Hi-Z = High impedance state.

Dynamic Characteristics



(EN = HIGH LEVEL)



Propagation Delays: (in nsec):

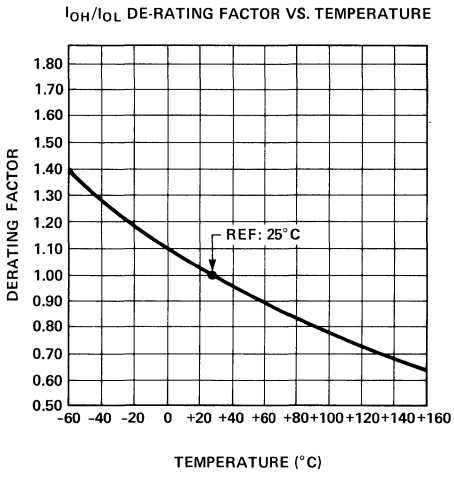
$t_{PHL} = 0.04\ (C_L) + 5$

$t_{PLH} = 0.04\ (C_L) + 5$

$t_{OFF} = 7.0$

$t_{ON} = 4.0$

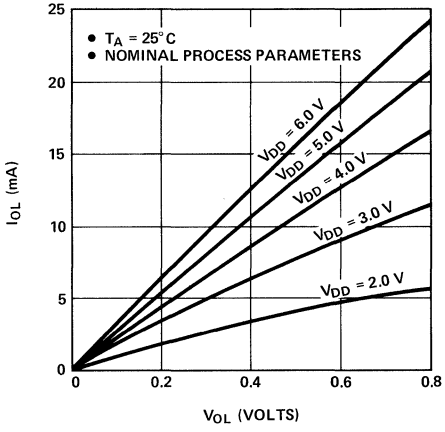
Output Drive Characteristics



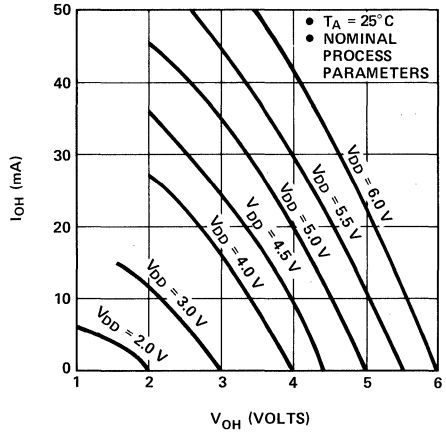
Process De-rating Factors:
Worst-case = 0.80
Nominal = 1.00
Best-case = 1.25

Output Drive Characteristics

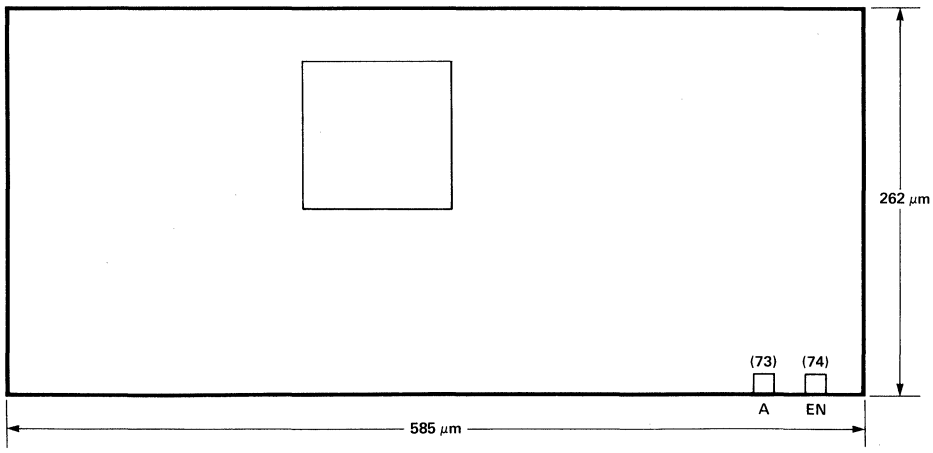
I_{OL} vs. V_{OL}



I_{OH} vs. V_{OH}



Outline Drawing



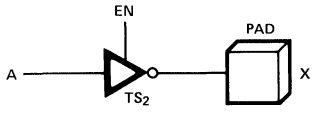
TTL/CMOS Three State Output Driver

BAM00832

Description

The BAM00832 is an output pad driver cell for externally connected circuits. It is a three-state circuit and is electrically identical to the BAM00830 cell. The only difference is the physical shape of the cell.

Logic Symbol

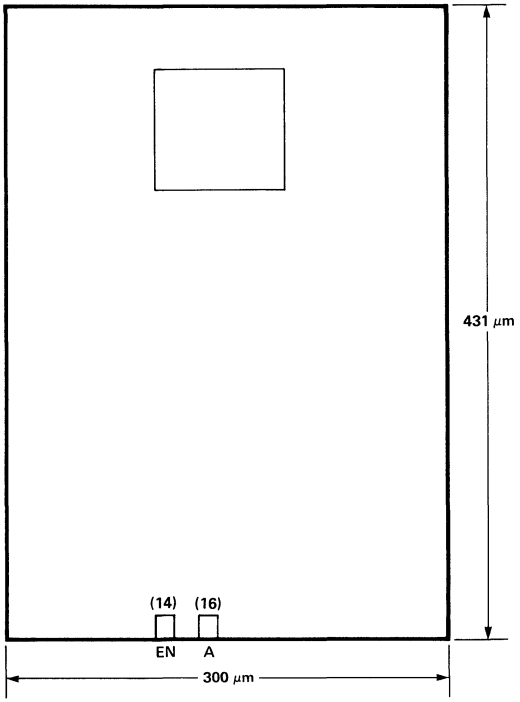


Cell Parameters

Parameter	Value	Unit
Cell Width	300	μm
Cell Height	431	μm
Cell Area	129K	sq. μm
Average Power Dissipation*	825 + 25 (C_L)	μW/MHz
Input Capacitance (A)	0.500	pF
Input Capacitance (E_N)	0.330	pF
Output Leakage	1.0	μA

*V_{DD} = 5.0V, T_A = 25° C, C_L in pF.

Outline Drawing



Note:
For Function Table, Dynamic Characteristics, TEGAS Model, SPICE Model, and Output Characteristics, see BAM00830 data sheet.

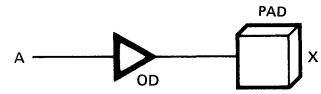
Open-Drain Output Driver

BAM00840

Description

The BAM00840 is an output driver pad cell with open-drain output driver stage which actively pulls to the low level. External pull-up resistors or wire-OR circuit implementations may be handled in this way. For I_{OL} characteristics, refer to BAM00820.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	354	μm
Cell Height	262	μm
Cell Area	93K	sq. μm
Average Power Dissipation*	30	μW/MHz
Input Capacitance	0.150	pF
Maximum Output Leakage (Off)	1.0	μA

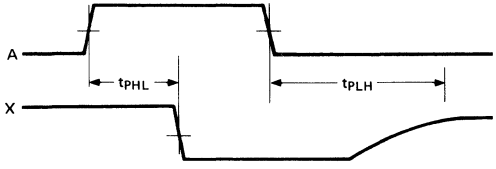
*V_{DD} = 5.0V, T_A = 25° C (Independent of C_L).

Function Table

Input A	Output X
L	High-Z
H	L

H = High level.
L = Low level.
Hi-Z = High impedance state.

Dynamic Characteristics

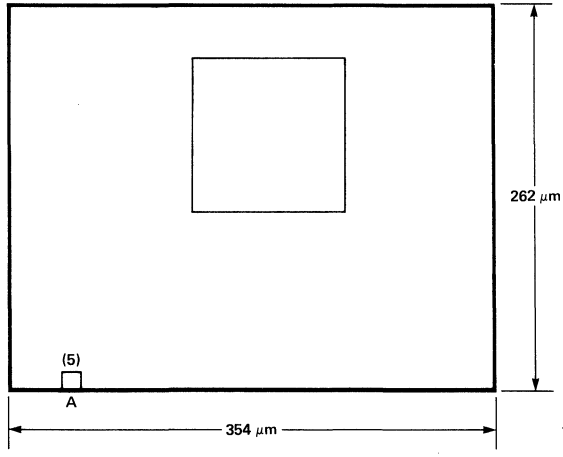


Propagation Delays (in nsec):

$t_{PHL} = 0.04\ (C_L) + 5$

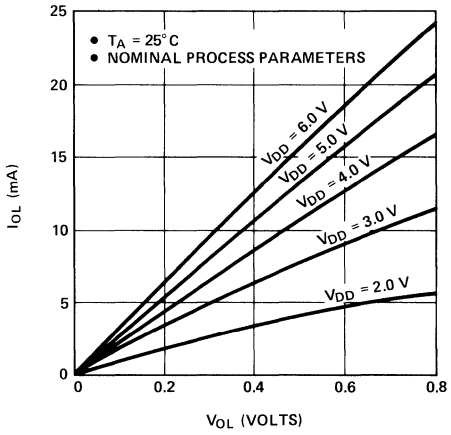
t_{PLH} = Dependent upon pull-up resistor value and output load capacitance ($\tau = RC$).

Outline Drawing

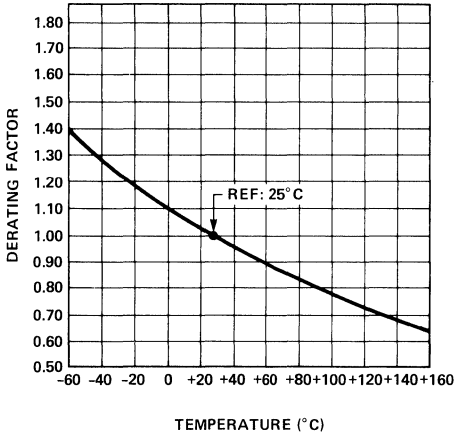


Output Drive Characteristics

I_{OL} vs. V_{OL}



I_{OH}/I_{OL} DE-RATING FACTOR VS. TEMPERATURE



Process De-rating Factors:
Worst-case = 0.80
Nominal = 1.00
Best-case = 1.25

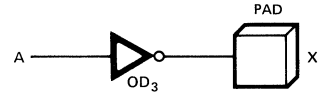
Open-Drain Output Driver

BAM00841

Description

The BAM00841 is an output driver pad cell with open-drain output driver stage which actively pulls to the low level. External pull-up resistors or wire-OR circuit implementations may be handled in this way. For I_{OL} characteristics, refer to BAM00822.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	169	μm
Cell Height	431	μm
Cell Area	73K	sq. μm
Average Power Dissipation*	40	μW/MHz
Input Capacitance	0.180	pF
Maximum Output Leakage (Off)	1.0	μA

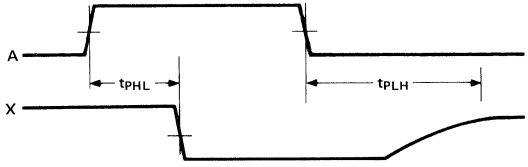
*V_{DD} = 5.0V, T_A = 25° C, (independent of C_L).

Function Table

Input A	Output X
L	Hi-Z
H	L

H = High level.
L = Low level.
Hi-Z = High impedance state.

Dynamic Characteristics

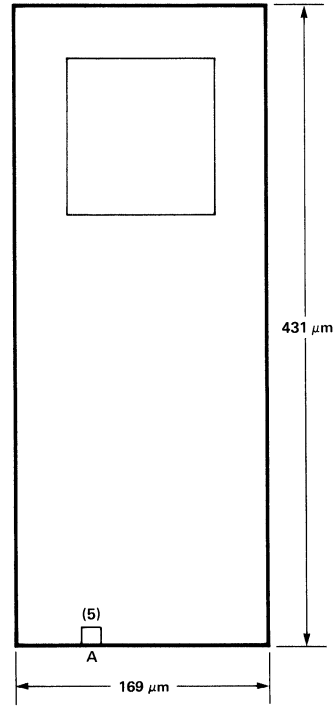


Propagation Delays (in nsec):

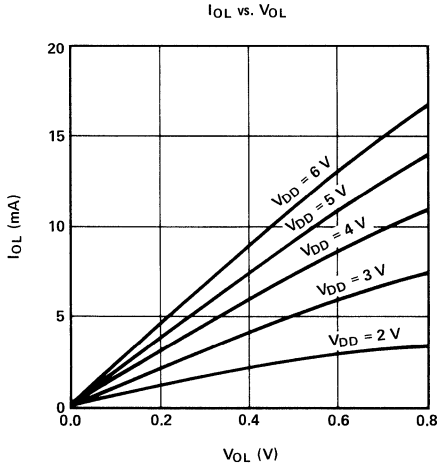
$t_{PHL} = 0.05\ (C_L) + 4$

t_{PLH} = Dependent upon pull-up resistor value and output load capacitance. ($\tau = RC$).

Outline Drawing



Output Drive Characteristics



Note: For temperature and process de-rating factors, refer to BAM00840 data sheet.

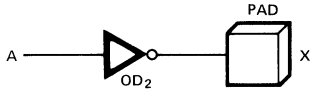
Open Drain Output Driver

BAM00845

Description

The BAM00845 is an open drain output pad cell used to drive externally connected circuits. It is similar to the BAM00840 except that it has less drive capability and is a smaller cell.

Logic Symbol



Cell Parameters

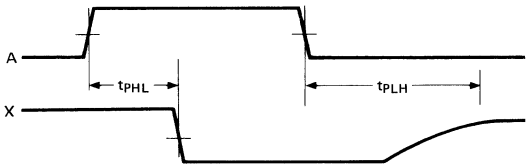
Parameter	Value	Unit
Cell Width	193	μm
Cell Height	262	μm
Cell Area	50K	sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance (A)	0.200	pF
Pad Capacitance (CI)	1.0	pF

Function Table

Input A	Output X
L	Hi-Z
H	L

H = High level.
L = Low level.
Hi-Z = High impedance state.

Dynamic Characteristics

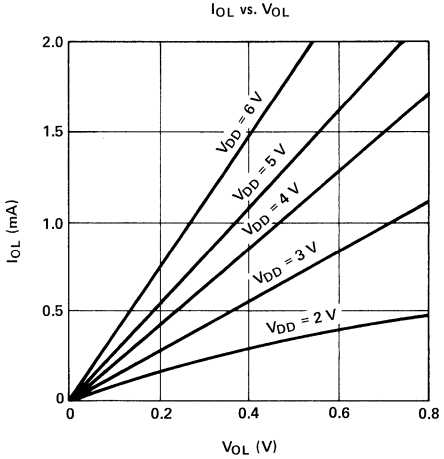


Propagation Delays: (in nsec):

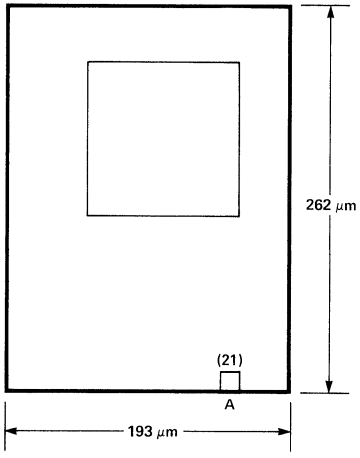
$t_{PHL} = 0.5 (C_L) + 0.7$

t_{PLH} = Dependent upon pull-up resistor value and output load capacitance

Output Drive Characteristics



Outline Drawing



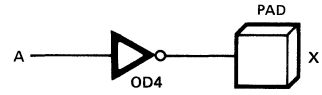
Open Drain Output Driver Pad

BAM00846

Description

The BAM00846 is an open drain output pad cell used to drive externally connected circuits. It is similar to the BAM00845, except for its physical shape.

Logic Symbol



Cell Parameters

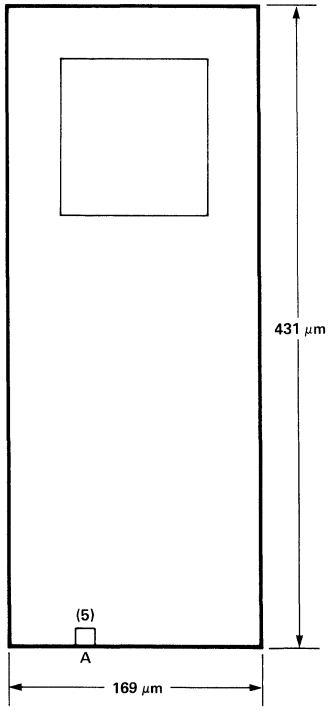
Parameter	Value	Unit
Cell Width	169	μm
Cell Height	431	μm
Cell Area	73K	Sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance (A)	0.200	pF
Pad Capacitance	1.0	pF

Function Table

Input	Output
A	**X**
L	Hi-Z
H	L

H = High level.
L = Low level.
Hi-Z = High impedance state.

Outline Drawing



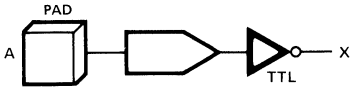
TTL-Compatible Input Buffer

BAM00850

Description

The BAM00850 is an input buffer pad cell used for externally applied TTL-compatible input signals.

Logic Symbol



(Protective device included)

Cell Parameters

Parameter	Value	Unit
Cell Width	293	μm
Cell Height	262	μm
Cell Area	77K	sq. μm
Average Power Dissipation	*	μW/MHz
Input Capacitance	1.0	pF
Minimum V_{IH} at V_{DD} = 5.0 V + 10%	2.0	V
Maximum V_{IL} at V_{DD} = 5.0 V + 10%	0.8	V
Maximum Input Leakage	1.0	μA

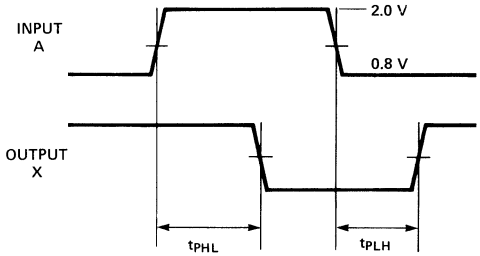
*V_{DD} = 5.0 V, T_A = 25° C, 50% Duty Cycle.

Function Table

Input A	Output X
H	L
L	H

H = High level.
L = Low level.

Dynamic Characteristics

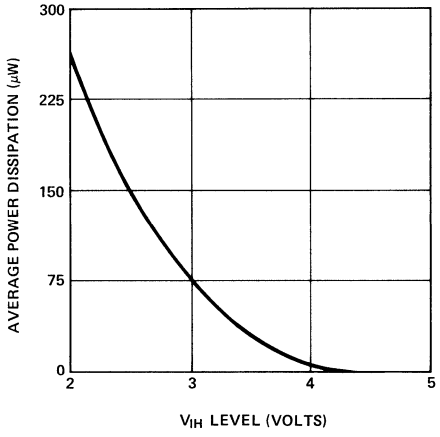


Propagation Delays (in nsec):

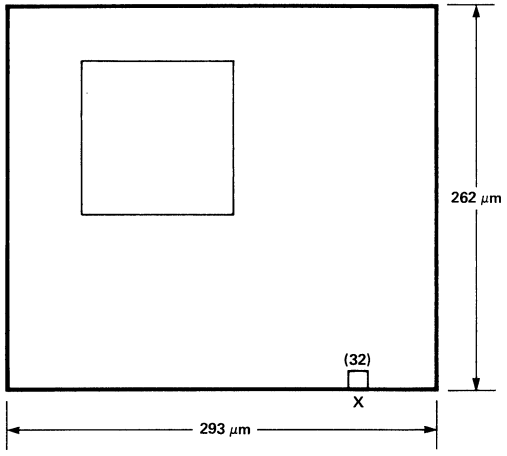
$t_{PHL} = 5\ (C_L) + 3$

$t_{PLH} = 5\ (C_L) + 3$

The following graph shows the relationship between power dissipation and V_{IH} level for the conditions outlined above.



Outline Drawing



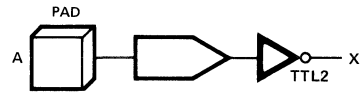
TTL-Compatible Input Buffer

BAM00851

Description

The BAM00851 is an input buffer pad cell used for externally applied TTL-compatible input signals. It is identical to the BAM00850, except for its physical shape.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	169	μm
Cell Height	431	μm
Cell Area	73K	Sq. μm
Average Power Dissipation	*	μW/MHz
Input Capacitance	1.0	pF
Minimum V_{IH} at V_{DD} = 5.0 V + 10%	2.0	V
Maximum V_{IL} at V_{DD} = 5.0 V + 10%	0.8	V
Maximum Input Leakage	1.0	μA

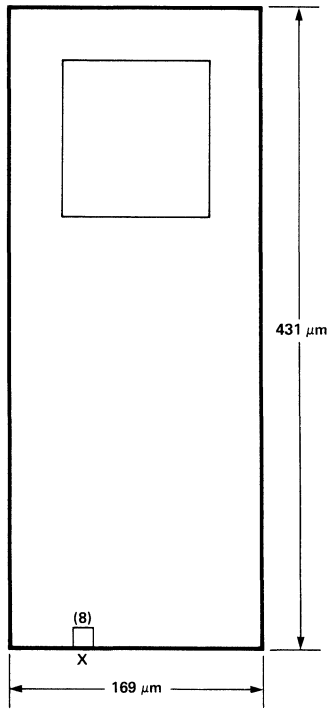
*V_{DD} = 5.0 V, T_A = 25° C, 50% duty cycle.

Function Table

Input	Output
A	**X**
H	L
L	H

H = High level.
L = Low level.

Outline Drawing



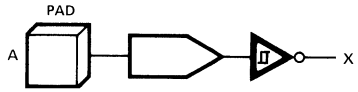
Schmitt Trigger Input Buffer

BAM00860

Description

The BAM00860 is an input pad cell which incorporates input level hysteresis (Schmitt Trigger).

Logic Symbol



(Input Protection Included)

Cell Parameters

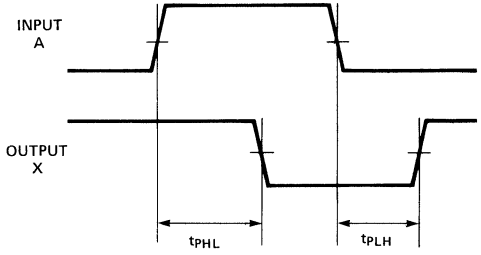
Parameter	Value	Unit
Cell Width	385	μm
Cell Height	262	μm
Cell Area	101K	sq. μm
Average Power Dissipation*	25	μW/MHz
Input Capacitance	1.0	pF
Minimum V_{IH} at V_{DD} = 2.0 - 6.0 V	V_{DD} - 0.5	V
Maximum V_{IL} at V_{DD} = 2.0 - 6.0 V	V_{SS} + 0.5	V
Maximum Input Leakage	1.0	μA

Function Table

Input A	Output X
H	L
L	H

H = High level.
L = Low level.

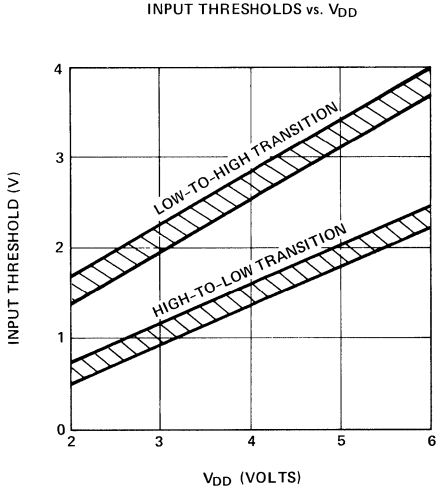
Dynamic Characteristics



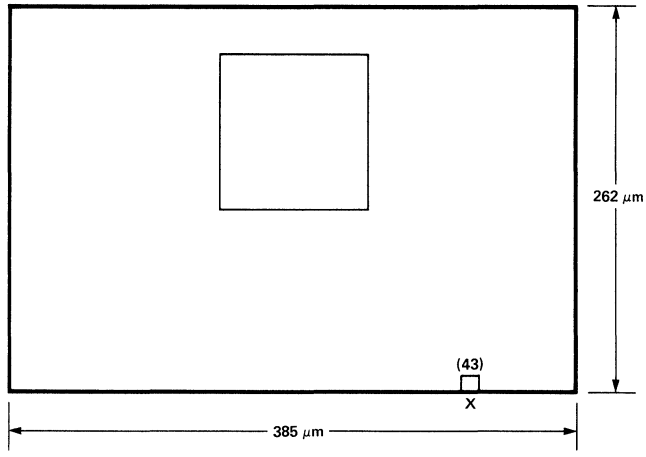
Propagation Delays (in nsec):

$t_{PHL} = 5\,(C_L) + 3$

$t_{PLH} = 5\,(C_L) + 3$



Outline Drawing



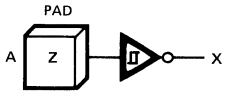
Schmitt Trigger Input Buffer

BAM00861

Description

The BAM00861 is an input pad cell that incorporates input level hysteresis (Schmitt Trigger). It is identical to the BAM00860, except for its physical shape.

Logic Symbol

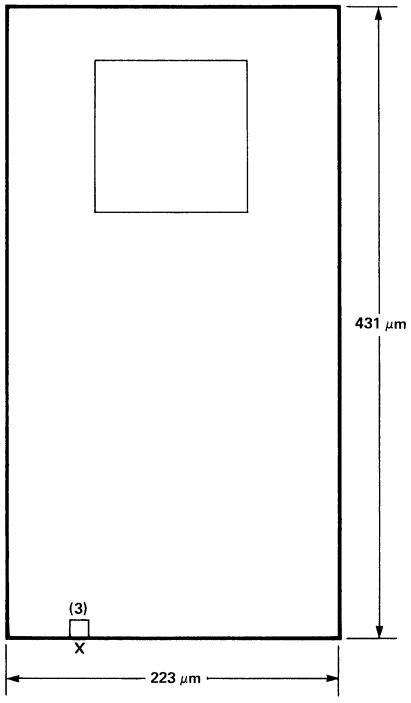


Cell Parameters

Parameter	Value	Unit
Cell Width	223	μm
Cell Height	431	μm
Cell Area	96K	Sq. μm
Average Power Dissipation*	25	μW/MHz
Input Capacitance	1.0	pF
Maximum Input Leakage	1.0	μA

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Outline Drawing



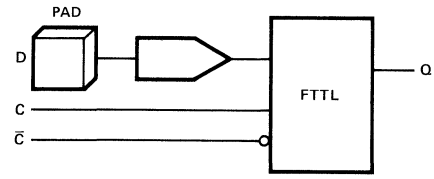
Fast TTL-Compatible Input Latch

BAM00870

Description

The BAM00870 is an input pad cell which contains an integral storage latch and which is intended for high speed operation. When C and $\overline{C}$ are active, the level of the Q output follows D directly. When C and $\overline{C}$ are deactivated, the D to Q feedthrough is disabled and internal latching circuits clamp the level of Q to either V_{DD} or V_{SS}, depending on the logic level of D just prior to C and $\overline{C}$ deactivation.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	339	μm
Cell Height	262	μm
Cell Area	89K	sq. μm
Average Power Dissipation*	15	μW/MHz
Input Capacitance (D)	1.0	pF
Input Capacitance (C, $\overline{C}$)	0.070	pF
Minimum V_{IH} at V_{DD} = 5.0 V + 10%	2.0	V
Maximum V_{IL} at V_{DD} = 5.0 V + 10%	0.8	V
Maximum Input Leakage	1.0	μA

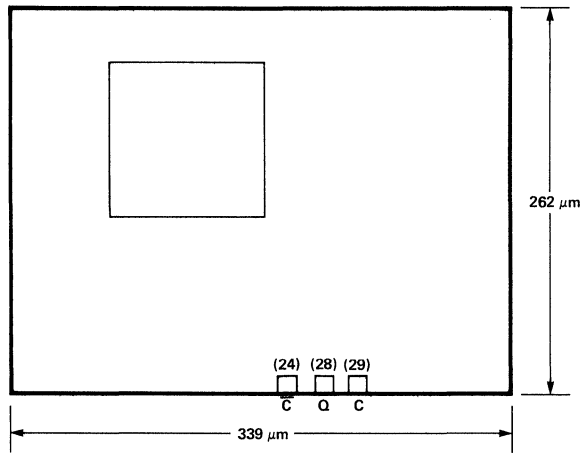
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Output
D	C	$\overline{C}$	Q
H	H	L	H
L	H	L	L
X	L	H	Q_O

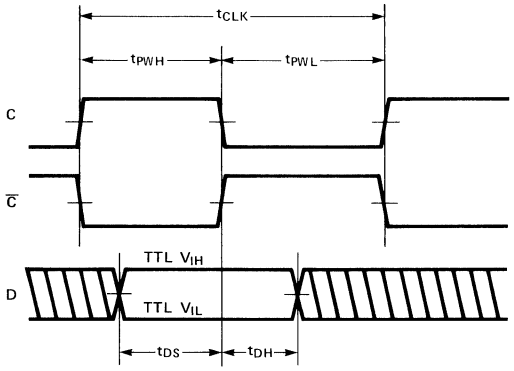
H = High level.
L = Low level.
X = "Don't care".
Q_O = Level on Q just prior to H-L transition of C.

Outline Drawing



Dynamic Characteristics

PULSE WIDTHS AND SET-UP TIMES



Minimum Times:

$t_{PWH} = 3.5$ nsec

$t_{PWL} = 3.5$ nsec

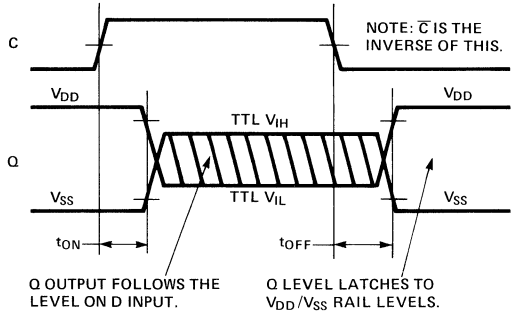
$t_{DS} = 2.0$ nsec

$t_{DH} = 2.0$ nsec

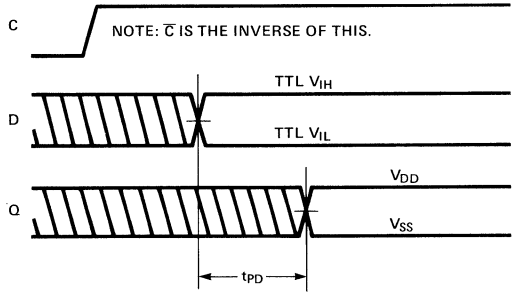
Maximum Clock Rate:

$f_{CLK} = \frac{1}{t_{CLK}} = 100$ MHz

LATCHING DELAYS



TRANSPARENT PROP DELAYS



Maximum Propagation Delays (in nsec):

$t_{ON} = 0.7\ (C_L) + 1.5$

$t_{OFF} = 0.3\ (C_L) + 3.0$

$t_{PD} = 1.5\ (C_L) + 0.4$

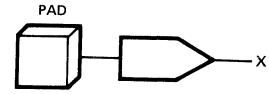
Input Pad with Protection Device

BAM00880

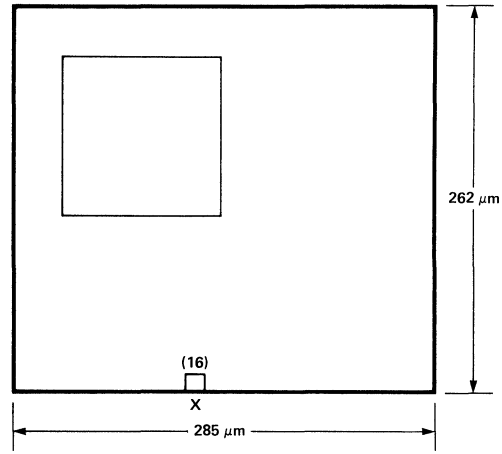
Description

The BAM00880 is an HCMOS cell which is used as a device input bonding pad. Integral to the cell is a protective device which prevents inadvertent damage caused by electrostatic discharges or by excessive applied voltage or current. The protection specifications also apply to other pad cells in the library which have protective devices included.

Logic Symbol



Outline Drawing



Cell Parameters

Parameter	Value	Unit
Cell Width	285	μm
Cell Height	262	μm
Cell Area	75K	Sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance	1.0	pF
Minimum Positive Latch-up Voltage	14	V
Minimum Positive Latch-up Current	10	mA
Minimum Negative Latch-up Voltage	1	V
Minimum Negative Latch-up Current	30	mA
Minimum Electrostatic Discharge	2000	V

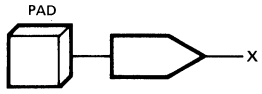
Input Pad with Protection Device

BAM00881

Description

The BAM00881 is an HCMOS cell that is used as a device input bonding pad. Integral to the cell is a protective device that prevents inadvertent damage caused by electrosatic discharges or by excessive applied voltage or current. It is identical to the BAM00880, except for its physical shape.

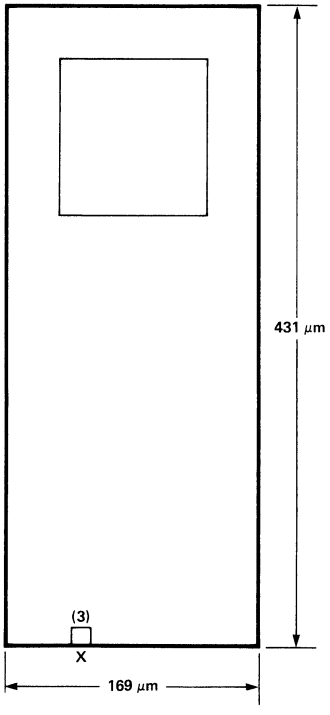
Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	169	μm
Cell Height	431	μm
Cell Area	73K	Sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance	1.0	pF
Minimum Positive Latch-up Voltage	14	V
Minimum Positive Latch-up Current	10	mA
Minimum Negative Latch-up Voltage	1	V
Minimum Negative Latch-up Current	30	mA
Minimum Electrostatic Discharge	2000	V

Outline Drawing



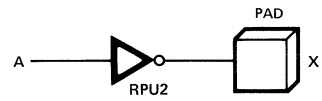
Open Drain Output Driver with Resistor Pull-Up

BAM00890

Description

The BAM00890 is an output pad cell that has an open drain output drive stage with a resistive pull-up device. It is capable of sinking 20 mA of current and is useful for driving LEDs or other high current loads. For I_{OL} characteristics, refer to BAM00824.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	524	μm
Cell Height	262	μm
Cell Area	137K	Sq. μm
Average Power Dissipation*	60	μW/MHz
Input Capacitance	0.130	pF
Minimum Pull-up Resistance	350K	ohm
Maximum Pull-up Resistance	700	ohm

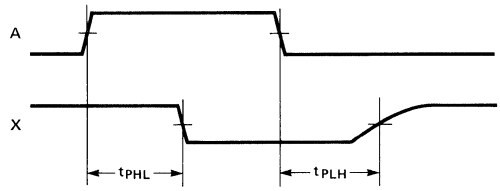
*V_{DD} = 5.0V, T_A = 25° C, 50% Output Duty Cycle.

Function Table

Input A	Output X
H	L
L	H

H = High level.
L = Low level.

Dynamic Characteristics

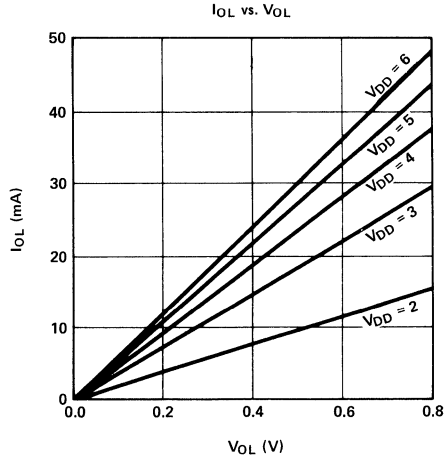


Propagation Delays (in nsec):

$t_{PHL} = 0.07\ (C_L) + 0.3$

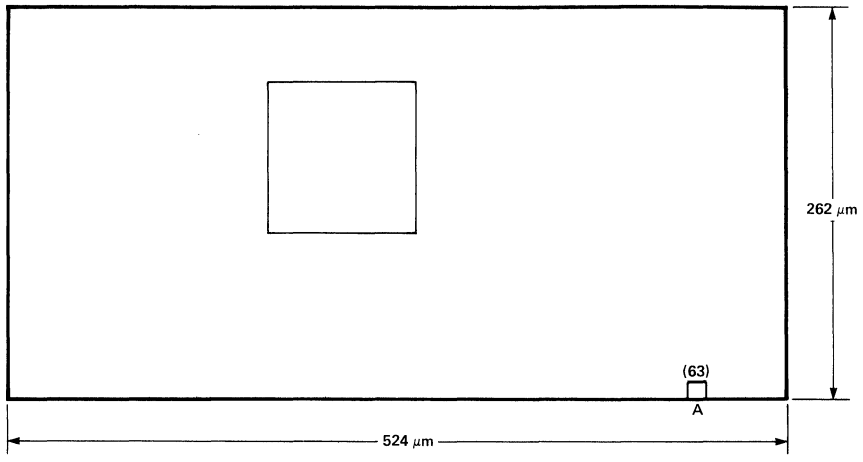
t_{PLH} = Dependent upon output load resistance and capacitance ($\tau = R_C$).

Output Drive Characteristics



Open Drain Output Driver with Resistor Pull-Up

Outline Drawing



LED Driver

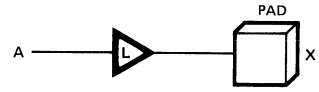
PRELIMINARY

BAM00891

Description

The BAM00891 is an output driver pad cell with open-drain output stage which actively pulls to the high level. The cell has an internal pull-down load of about 10K Ω to ensure that the output discharges when switched off. This cell may be used with other pad cells (like the BAM00840) to implement multiplexed load drive.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	554	μm
Cell Height	431	μm
Cell Area	239K	Sq. μm
Average Power Dissipation*	600	μW/MHz
Input Capacitance	0.20	pF
Maximum Output Leakage	7.0	μA

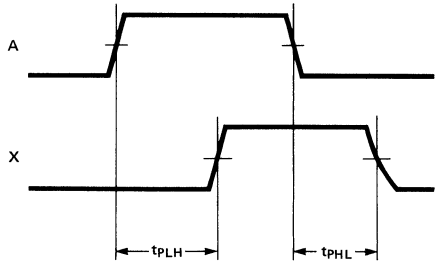
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Input A	Output X
L	Hi-Z
H	H

H = High level.
L = Low level.

Dynamic Characteristics

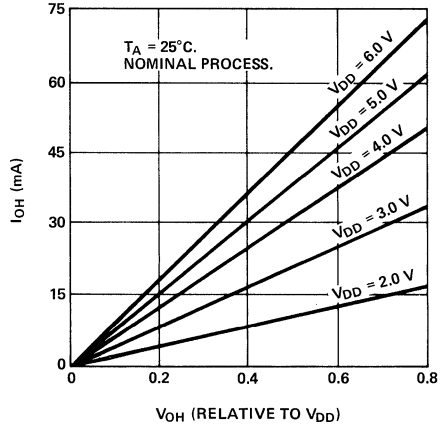


Propagation Delays (in nsec):

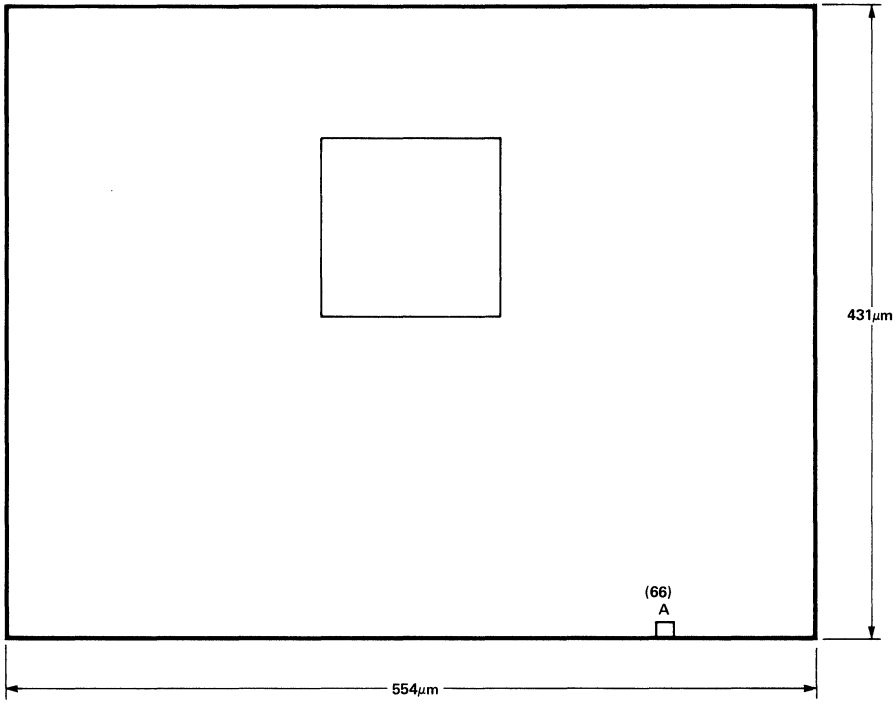
t_{PLH} = 0.015 (C_L) + 6

t_{PHL} = Dependent upon external pull-down resistor value and load capacitance.

Output Drive Characteristics



Outline Drawing



I/O Pad with Open Drain Output

BAM00910

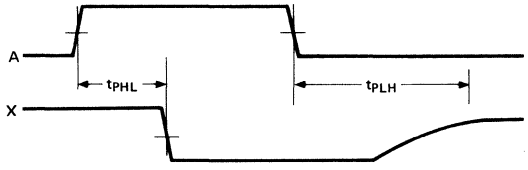
Description

The BAM00910 is an I/O pad cell with an open drain output driver and an input protection device. For I_{OL} characteristics, refer to BAM00845.

Cell Parameters

Parameter	Value	Unit
Cell Width	300	μm
Cell Height	262	μm
Cell Area	79K	sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance (A)	0.200	pF
Pad Capacitance (D_N)	1.0	pF

Dynamic Characteristics

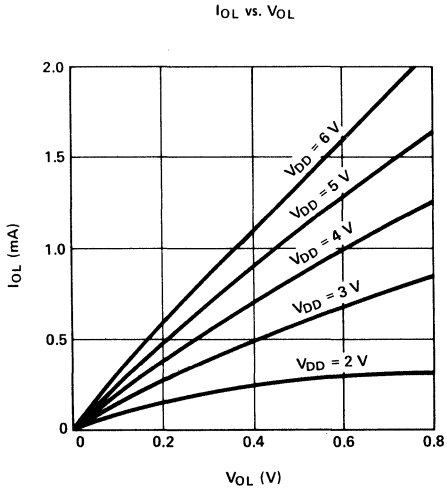


Propagation Delays: (in nsec):

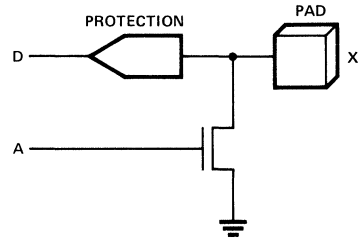
$t_{PHL} = 0.6\ (C_L) + 0.7$

t_{PLH} = Dependent upon pull-up resistor value and output load capacitance.

Output Drive Characteristics



Logic Symbol

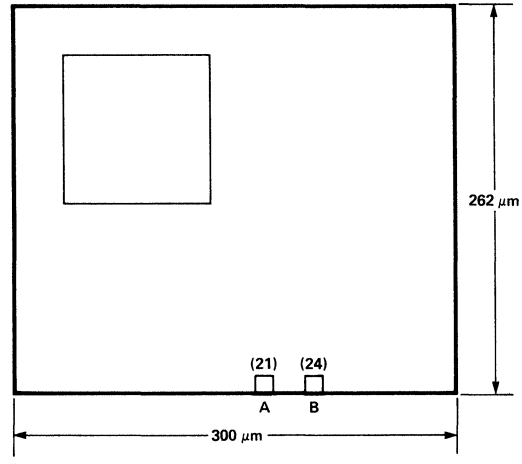


Function Table

Input A	Outputs B, X
L	Hi-Z
H	L

H = High level.
L = Low level.
Hi-Z = High impedance state.

Outline Drawing



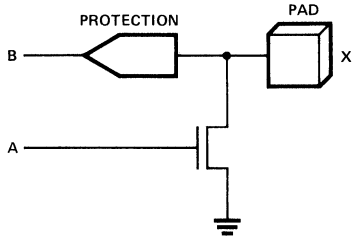
I/O Pad with Open Drain Output

BAM00911

Description

The BAM00911 is an I/O pad cell with an open drain output driver and an input protection device. It is very similar to the BAM00910 except that the output drive capability is substantially increased.

Logic Symbol



Cell Parameters

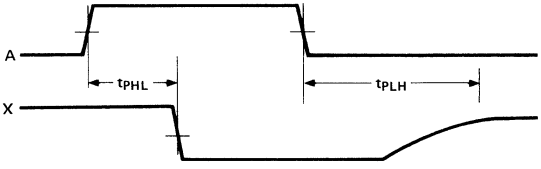
Parameter	Value	Unit
Cell Width	316	μm
Cell Height	431	μm
Cell Area	136K	sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance (A)	0.200	pF
Pad Capacitance	1.0	pF

Function Table

Input A	Outputs B, X
L	Hi-Z
H	L

H = High level.
L = Low level.
Hi-Z = High impedance state.

Dynamic Characteristics

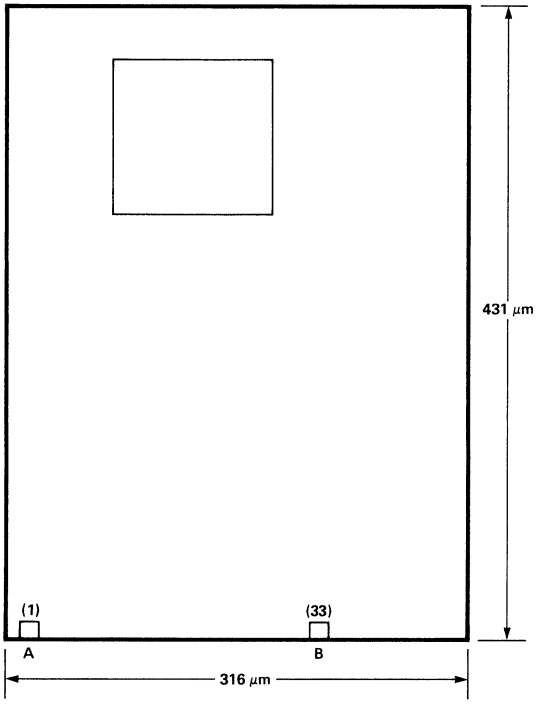


Propagation Delays (in nsec):

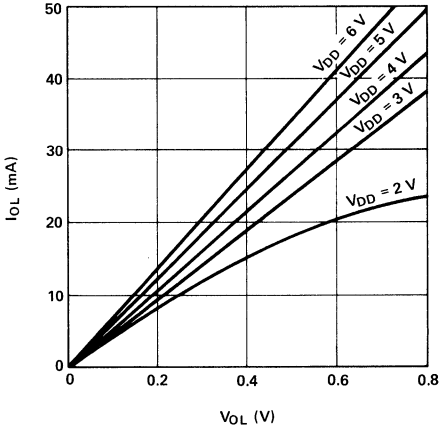
$t_{PHL} = 0.02\ (C_L) + 0.04$

t_{PHL} = Dependent upon pull-up resistor value and output load capacitance.

Outline Drawing



Output Drive Characteristics



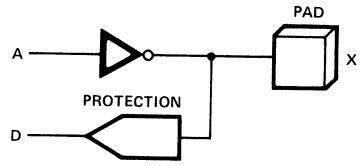
Output Driver Pad for Clock Oscillator

BAM00920

Description

The BAM00920 is an I/O pad cell which is used as an output driver for externally connected circuits. In addition, a protection device permits the pad signal to be routed back on to the chip, so that it may be used as part of and R-C oscillator for clock generation.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	416	μm
Cell Height	262	μm
Cell Area	109K	sq. μm
Average Power Dissipation*	400 + 25(C_L)	μW/MHz
Input Capacitance (A)	3.0	pF
Pad Capacitance	1.0	pF

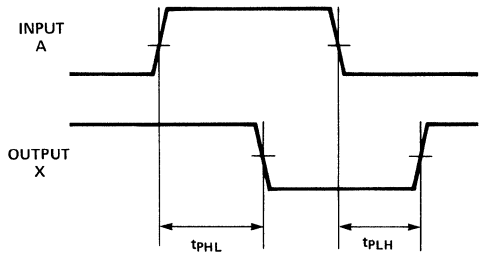
*V_{DD} = 5.0 V, T_A = 25° C, C_L in pF.

Function Table

Input A	Output X
H	L
L	H

H = High level.
L = Low level.

Dynamic Characteristics



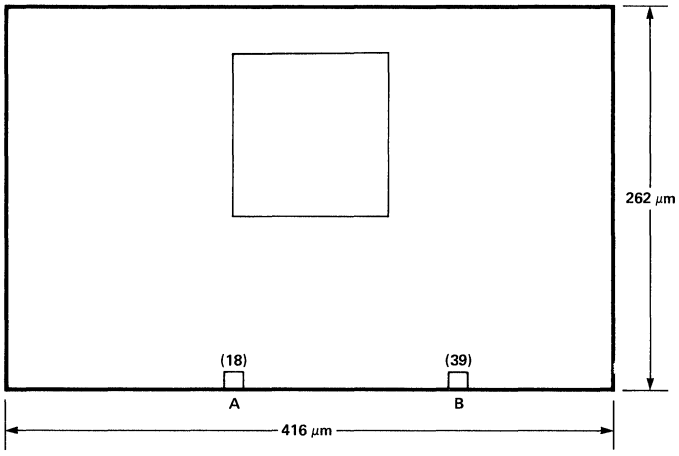
(EN = HIGH LEVEL)

Propagation Delays: (in nsec):

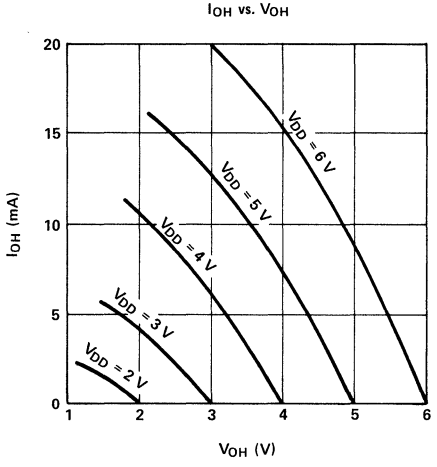
$t_{PHL} = 0.2\ (C_L) + 0.7$

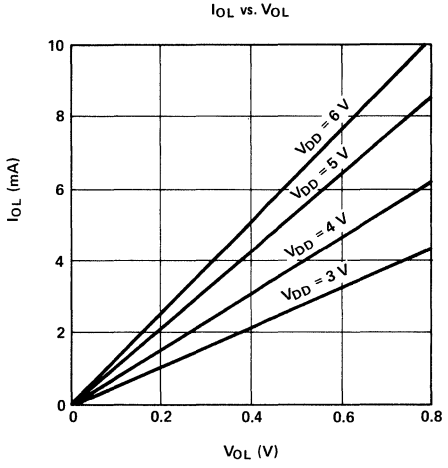
$t_{PLH} = 0.2\ (C_L) + 0.7$

Outline Drawing



Output Drive Characteristics





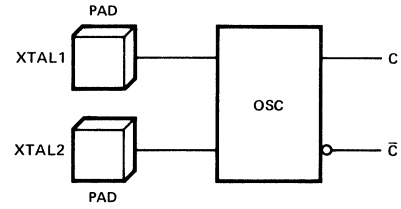
Crystal Oscillator with Pads

BAM00921

Description

The BAM00921 is a crystal oscillator circuit whose center frequency is 16 MHz. The only external components required are the desired crystal and two capacitors. Alternately, it is possible to drive the XTAL1 pin with an externally generated signal, in which case XTAL2 must be unconnected. C and $\overline{C}$ are outputs from the oscillator and are complementary signals.

Logic Symbol

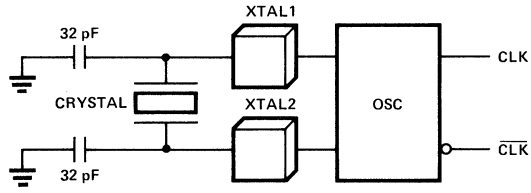


Cell Parameters

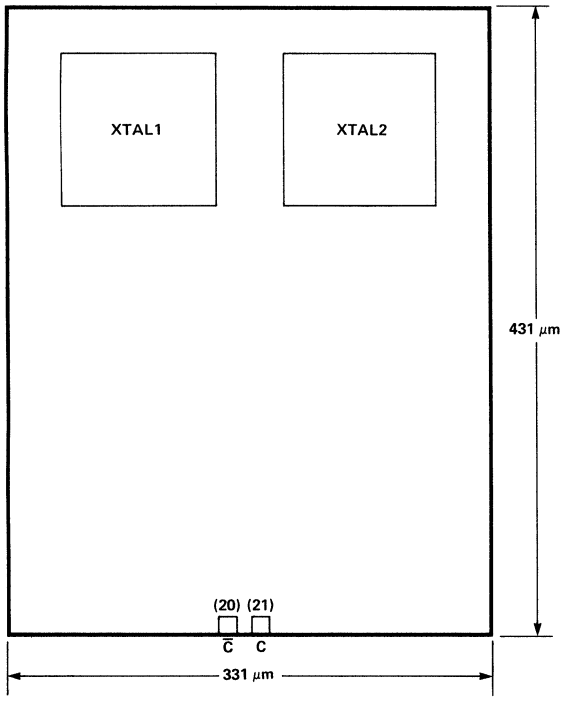
Parameter	Value	Unit
Cell Width	331	μm
Cell Height	431	μm
Cell Area	143K	sq. μm
Average Power Dissipation*	4.0	mW
Minimum Frequency	12	MHz
Maximum Frequency	16	MHz

*V_{DD} = 5.0 V, T_A = 25° C, C_L = 0.050 pF, Frequency = 16 MHz.

Typical Connection



Outline Drawing



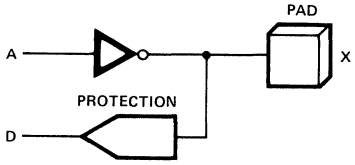
Output Driver Pad for Clock Oscillator

BAM00923

Description

The BAM00923 is an I/O pad cell which is used as an output driver for externally connected circuits. In addition, a protection device permits the pad signal to be routed back on to the chip, so that it may be used as part of an R-C oscillator for clock generation. This cell is identical to the BAM 00920, except for its physical shape.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	293	μm
Cell Height	431	μm
Cell Area	126.2K	sq. μm
Average Power Dissipation*	375 + 25 (C_L)	μW/MHz
Input Capacitance (A)	3.0	pF
Pad Capacitance	1.0	pF

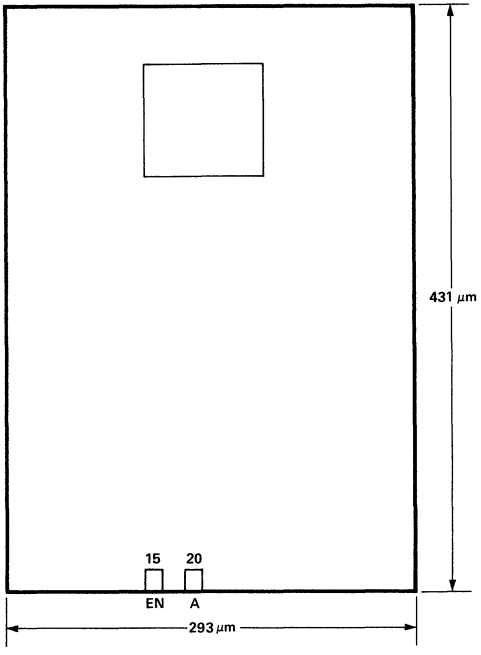
*V_{DD} = 5.0 V, T_A = 25° C, C_L in pF.

Function Table

Input A	Output X
H	L
L	H

H = High level.
L = Low level.

Outline Drawing



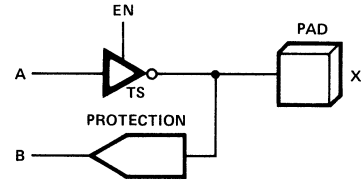
I/O Pad with Three-State Output

BAM00930

Description

The BAM00930 is an I/O pad cell which functions as a three-state driver for externally connected circuits. In addition, the pad connection is routed back to the chip so that external drivers can be inputs, as well. It is identical to the BAM00830 cell, except for the addition of the input with its protection device.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	708	μm
Cell Height	262	μm
Cell Area	185K	sq. μm
Average Power Dissipation*	825 + 25 (C_L)	μW/MHz
Input Capacitance (A)	0.500	pF
Input Capacitance (EN)	0.330	pF
Pad Capacitance	1.0	pF

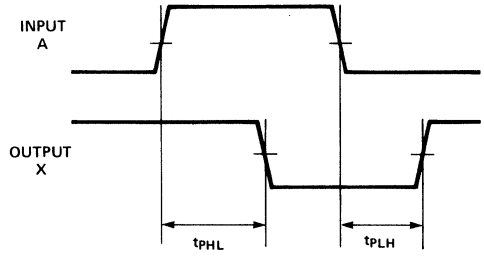
*V_{DD} = 5.0 V, T_A = 25° C.

Function Table

Inputs A	Inputs EN	Output B, X
X	L	Hi-Z
L	H	H
H	H	L

H = High level.
L = Low level.
X = "Don't Care"
Hi-Z = High Impedance State.

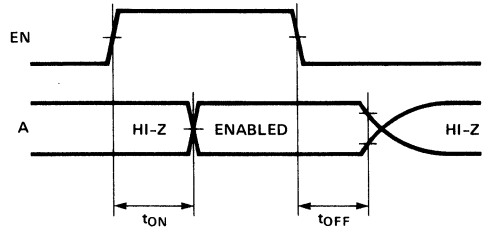
Dynamic Characteristics



(EN = HIGH LEVEL)

$t_{PHL} = 0.04\ (C_L) + 6$

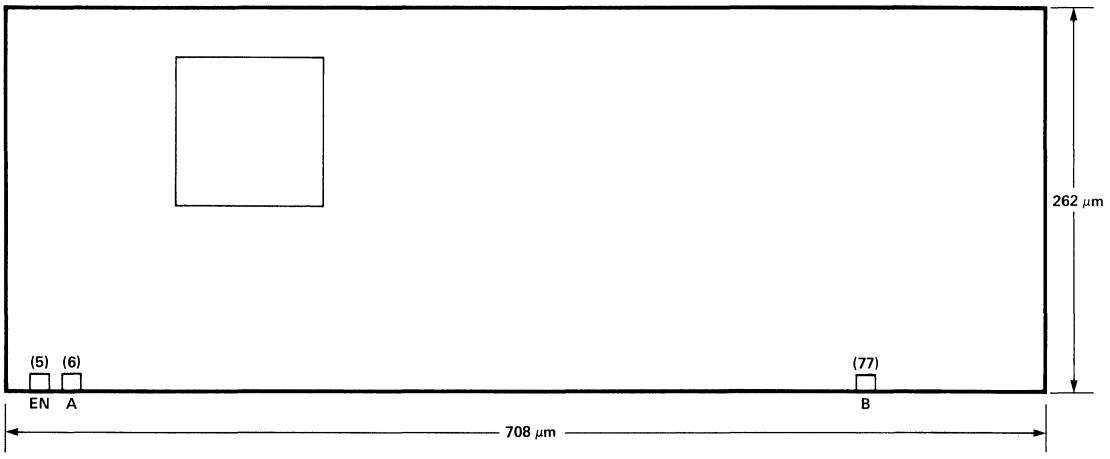
$t_{PLH} = 0.04\ (C_L) + 6$



$t_{OFF} = 7.0$

$t_{ON} = 3.5$

Outline Drawing



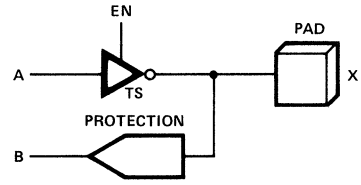
I/O Pad with Three-State Output

BAM00932

Description

The BAM00932 is an I/O pad cell which functions as a three-state driver for externally connected circuits. In addition, the pad connection is routed back to the chip so that external drivers can be inputs, as well. It is similar to the BAM00930, except for its physical shape.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	347	μm
Cell Height	431	μm
Cell Area	149.4K	sq. μm
Average Power Dissipation*	800 + 25(C_L)	μW/MHz
Input Capacitance (A)	0.500	pF
Input Capacitancew (EN)	0.330	pF
Pad Capacitance	1.0	pF

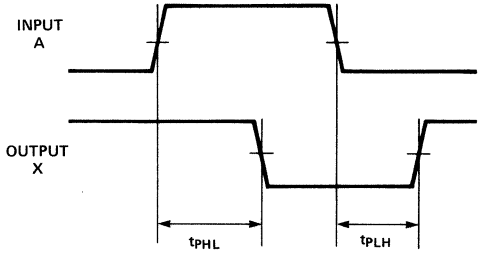
*V_{DD} = 5.0 V, T_A = 25° C.

Function Table

Inputs A	Inputs EN	Output B, X
X	L	Hi-Z
L	H	H
H	H	L

H = High level.
L = Low level.
X = "Don't Care"
Hi-Z = High Impedance State.

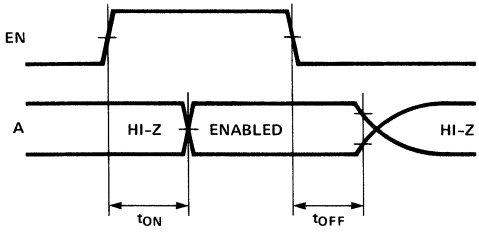
Dynamic Characteristics



$t_{PHL} = 0.04\ (C_L) + 6$

$t_{PLH} = 0.04\ (C_L) + 6$

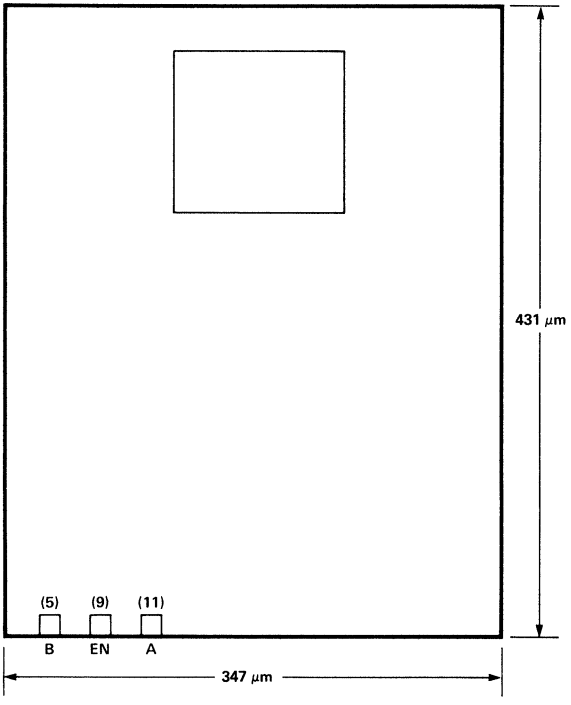
(EN = HIGH LEVEL)



$t_{OFF} = 7.0$

$t_{ON} = 3.5$

Outline Drawing



Counters/ Adders

12

Synertek.

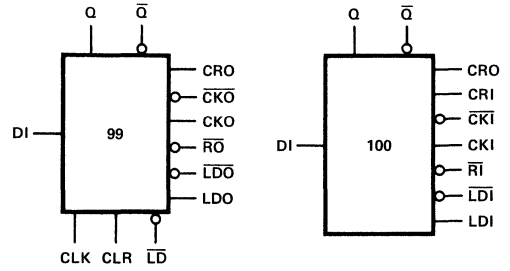
Look-Ahead Carry Counter

BAM00099/100

Description

The BAM00099/100 are HCMOS cells which are used for fast-carry counters. In addition, a data loading capability permits forcing each stage in a count chain to a presettable state. The BAM00099 is used for the first stage of the count chain and has the clock, clear, and common load drivers, as well as the first counter bit. The BAM00100 is used for following stages.

Logic Symbol

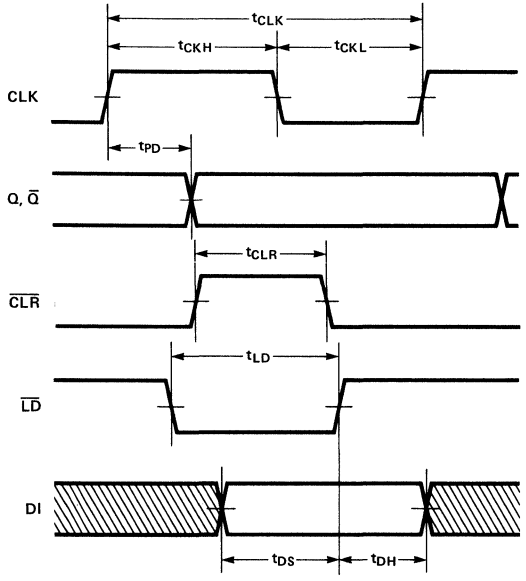


Cell Parameters

Parameter	Value BAM00099	Value BAM00100	Unit
Cell Width	200.2	154	μm
Cell Height	138.6	138.6	μm
Cell Area	27.8K	21.3K	sq. μm
Average Power Dissipation*	49 + 3N	38.0	μW/MHz
Input Capacitance (DI)	0.070	0.070	pF
Input Capacitance (LD, CLR)	0.110	—	pF
Input Capacitance (CLK)	0.070	—	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Dynamic Characteristics

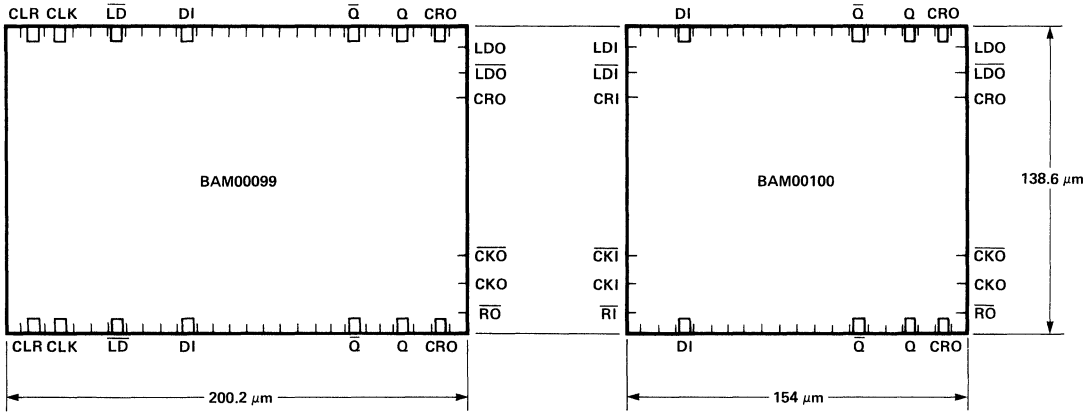


Dynamic Parameters

Parameter	Min.	Max.	Unit
t_{CLK}	20.0	—	ns
t_{CKL}	8.0	—	ns
t_{CKH}	8.0	—	ns
t_{PD}	1.5	4	ns
t_{CLR}	6.7	—	ns
t_{LD}	6.7	—	ns
t_{DS}	3.5	—	ns
t_{DH}	0	—	ns

Note: Use propagation delay de-rating factors for all parameters.

Outline Drawings



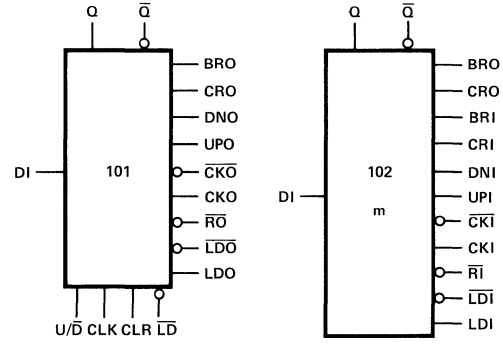
Look-Ahead Carry/Borrow Up/Down Counter

BAM00101/102

Description

The BAM00101/102 are HCMOS cells which are used as fast-carry/borrow up/down counters. In addition, a data loading capability permits forcing each stage in a count chain to a presettable state. The BAM00101 is used for the first stage of the count chain and has the clock, clear, and common load drivers, as well as the first counter bit. The BAM00102 is used for following stages.

Logic Symbols

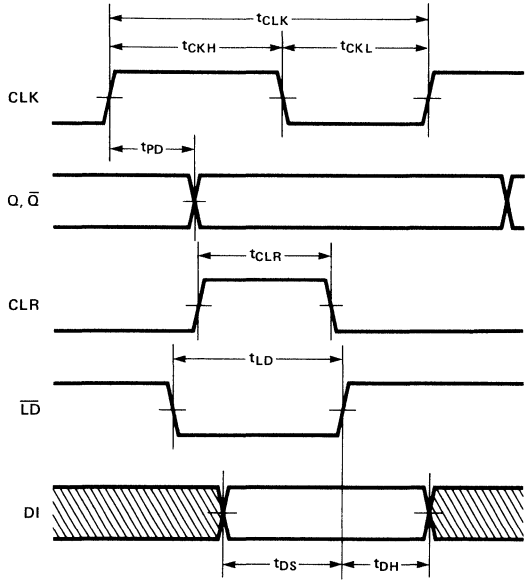


Cell Parameters

Parameter	Value BAM00101	Value BAM00102	Unit
Cell Width	269.5	207.9	μm
Cell Height	138.6	138.6	μm
Cell Area	37.4K	28.8K	sq. μm
Average Power Dissipation*	49.0 + 3N	38.0	μW/MHz
Input Capacitance (DI)	0.070	0.070	pF
Input Capacitance ($\overline{LD}$,CLR, U/$\overline{D}$)	0.110	—	pF
Input Capacitance (CLK)	0.110	—	pF

*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Dynamic Characteristics

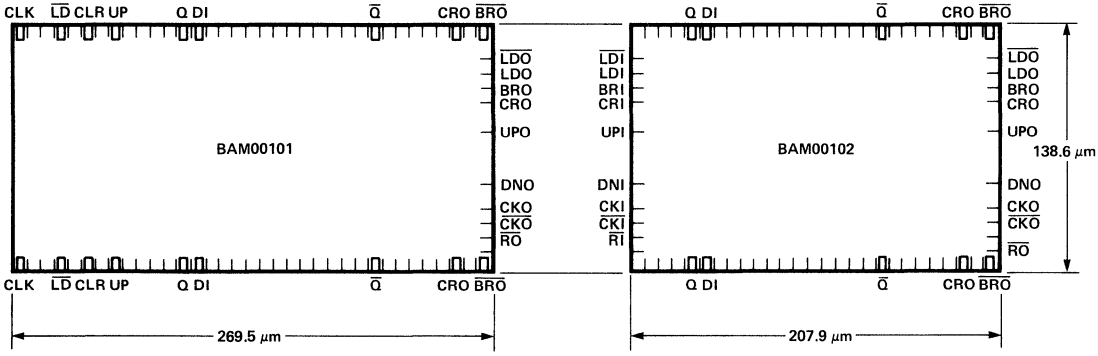


Dynamic Parameters

Parameter	Min.	Max.	Unit
t_{CLK}	30	—	ns
t_{CKL}	12	—	ns
t_{CKH}	12	—	ns
t_{PD}	2	6	ns
t_{CLR}	10	—	ns
t_{LD}	10	—	ns
t_{DS}	5	—	ns
t_{DH}	0	—	ns

Note: Use propagation delay de-rating factors for all parameters.

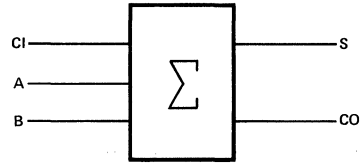
Outline Drawings



Description

The BAM00105 is a binary adder cell which can be combined with other like cells to form multi-bit adders. It consists of two inputs which are the bits to be added (A and B), a carry input (CI), the sum output (S), and the carry output (CO). It is comparable in function to the 7483 TTL device.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	115.5	μm
Cell Height	138.6	μm
Cell Area	16.0K	sq. μm
Average Power Dissipation*	45.0	μW/MHz
Input Capacitance (A, B)	0.080	pF
Input Capacitance (CI)	0.140	pF

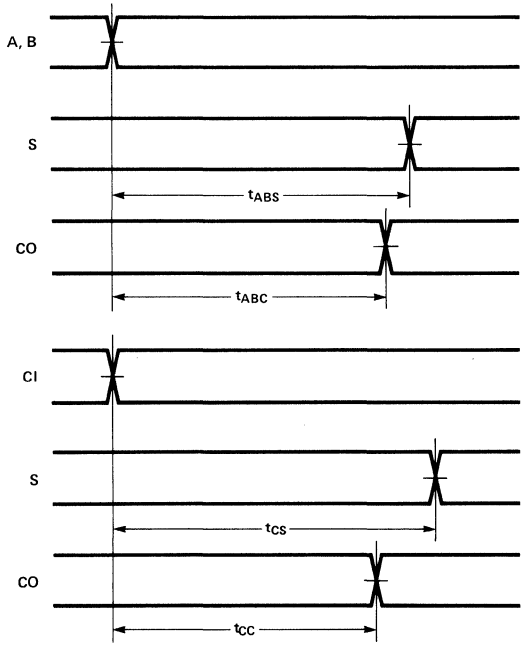
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Outputs	
A	B	CI	S	CO
L	L	L	L	L
H	L	L	H	L
L	H	L	H	L
H	H	L	L	H
L	L	H	H	L
H	L	H	L	H
L	H	H	L	H
H	H	H	H	H

H = High level.
L = Low level.

Dynamic Characteristics



Propagation Delays (in nsec):

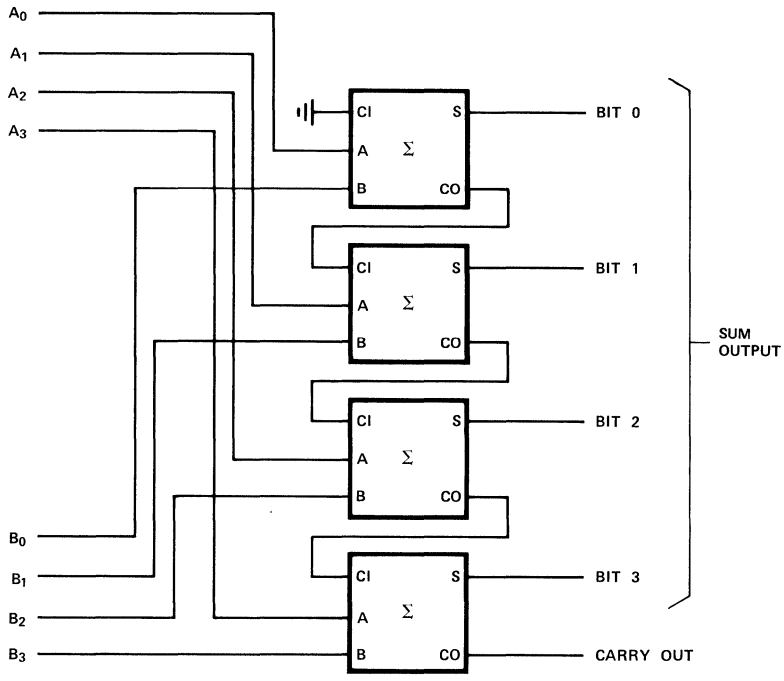
$t_{ABS} = 6\ (C_L) + 10$

$t_{ABC} = 3\ (C_L) + 10$

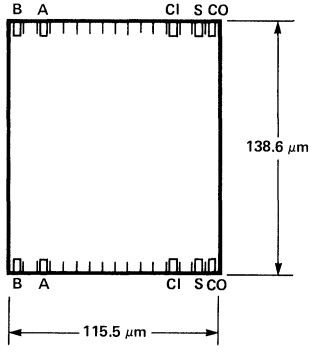
$t_{CS} = 6\ (C_L) + 6$

$t_{CC} = 3\ (C_L) + 3$

Typical Application (4-Bit Adder)



Outline Drawing



Memories

13

Synertek.

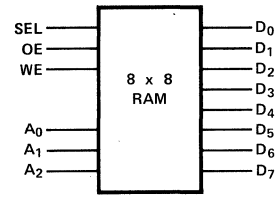
8 x 8 Static RAM

BAM06010

Description

The BAM06010 is a static RAM cell organized 8 words by 8 bits. Its operation is similar to the SY2114 except that all control signals are positive-true. The data bus lines are all bi-directional and are three-state outputs, controlled by OE.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	747	μm
Cell Height	508	μm
Cell Area	380K	sq. μm
Standby Power Dissipation[1]	8	μW
WR Cycle Power Dissipation[1]	250	μW
RD Cycle Power Dissipation[2]	250	μW
Input Capacitance (A_N)	0.250	pF
Input Capacitance (OE, SEL, WE)	0.300	pF
Input Capacitance (D_N)	0.100	pF

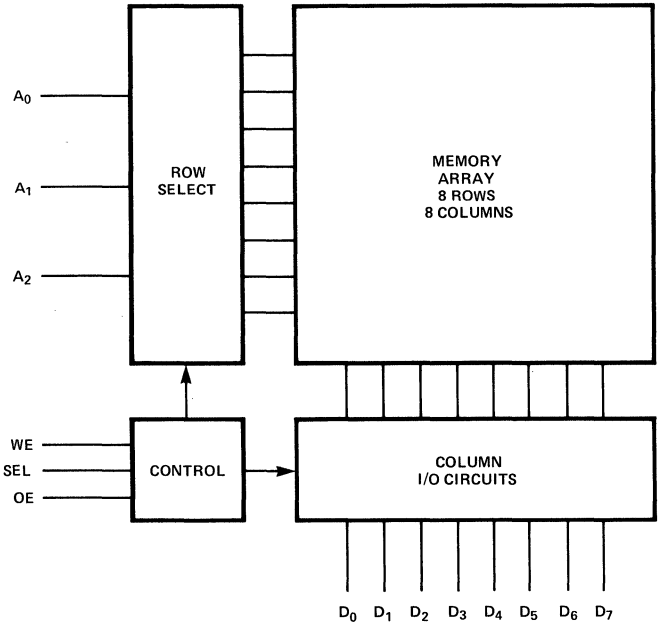
Notes:
1. V_{DD} = 5.0V, T_A = 25° C, independent of C_L.
2. V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Outputs
SEL	WE	OE	D_O-D_7
L	x	x	High-Z
H	L	L	High-Z
H	L	H	Read Data Out
H	H	L	Write Data In

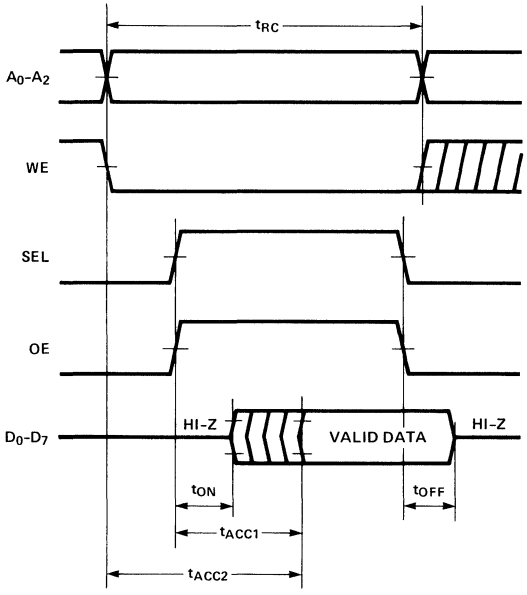
H = High level.
L = Low level.
x = "Don't care".

Block Diagram

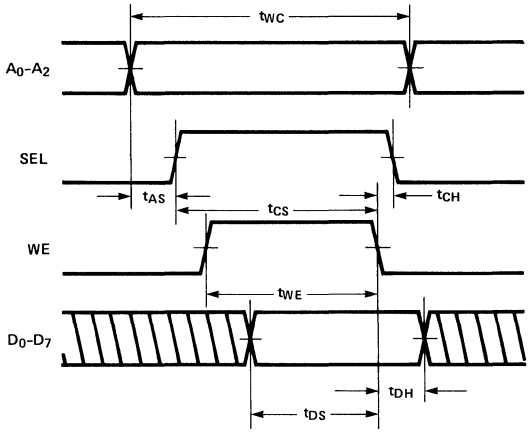


Dynamic Characteristics

READ TIMING



WRITE TIMING



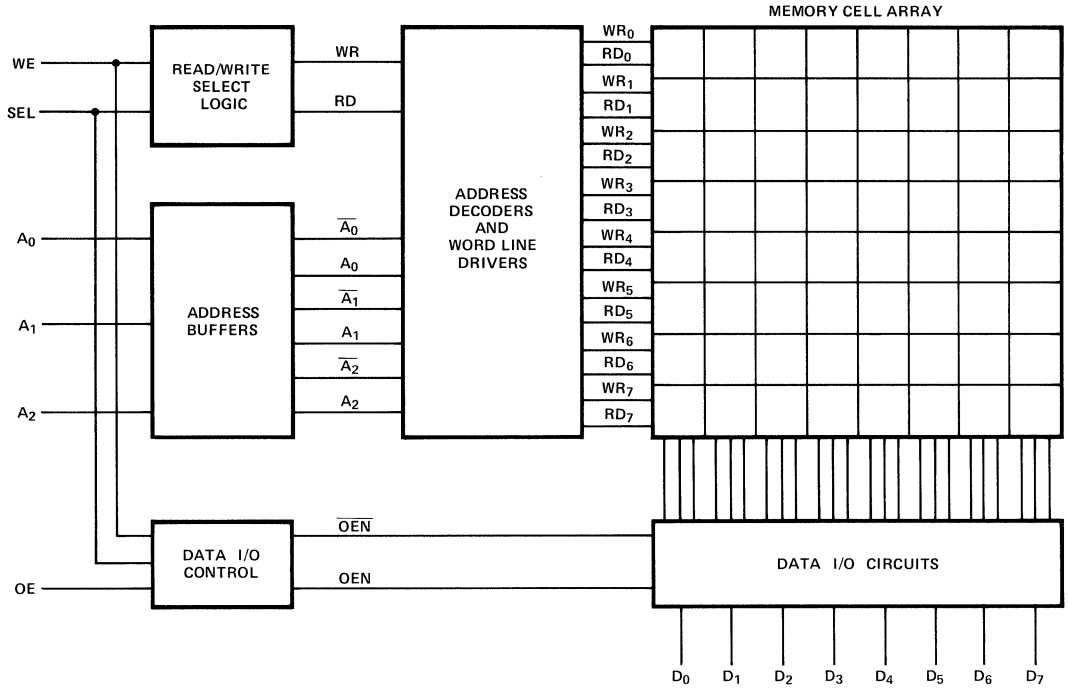
Read Cycle Timings (T_A = 25° C, V_{DD} = 5.0 V)

Parameter	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	35	—	ns
Read Access Time	t_{ACC2}	—	20+4(C_L)	ns
SEL/OE to Valid Output	t_{ACC1}	—	10	ns
Output Turn-On Delay	t_{ON}	—	10	ns
Output Turn-Off Delay	t_{OFF}	—	15	ns

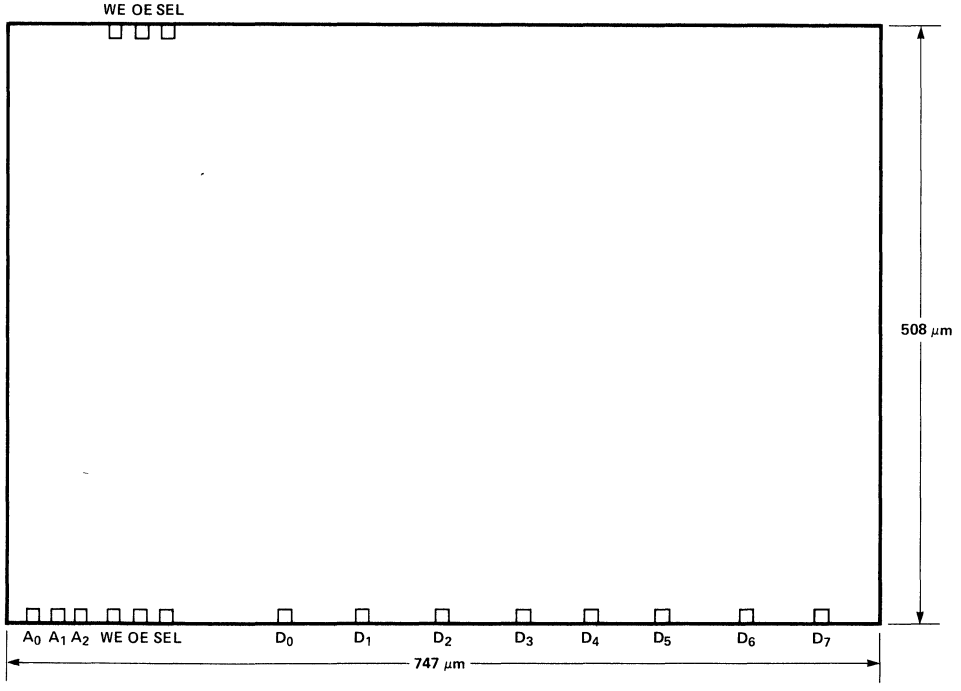
Write Cycle Timings (T_A = 25° C, V_{DD} = 5.0 V)

Parameter	Symbol	Min.	Max.	Unit
Write Cycle Time	t_{WC}	35	—	ns
Address Set Up Time	t_{AS}	10	-	ns
WE Pulse Width	t_{WE}	20	-	ns
Data Set Up Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	15	-	ns
SEL Set Up Time	t_{CS}	20	-	ns
SEL Hold Time	t_{CH}	0	-	ns

Detailed Block Diagram



Outline Drawing



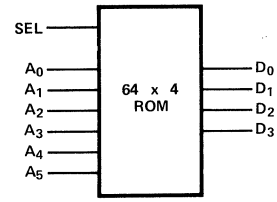
64 x 4 Static ROM

BAM06140

Description

The BAM06140 is a static ROM cell organized 64 words by 4 bits. It is activated by a single SEL input which causes the contents of the applied address to be presented on the cell outputs. When SEL is in its inactive state, the outputs are high impedance.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	447	μm
Cell Height	508	μm
Cell Area	227K	sq. μm
Average Power Dissipation*	8.0	mW
Input Capacitance (SEL, A_N)	0.080	pF
Output Capacitance (D_N)	0.040	pF

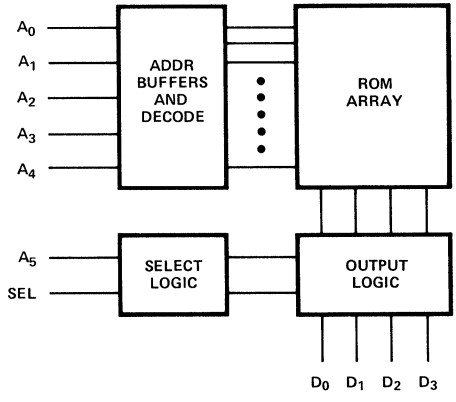
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

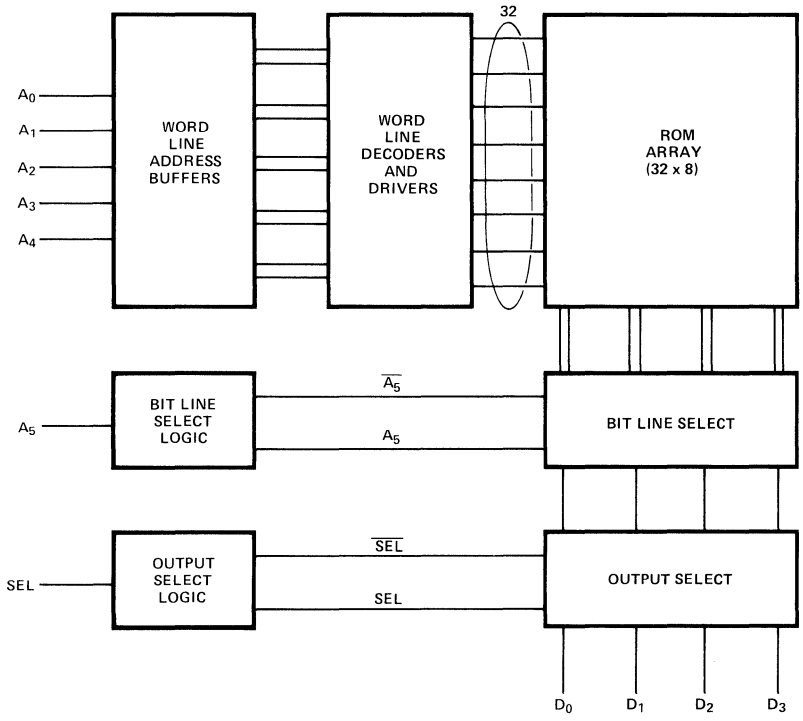
Input SEL	Outputs D_0-D_3
H	Active
L	Hi-Z

H = High level.
L = Low level.
Hi-Z = High impedance state.

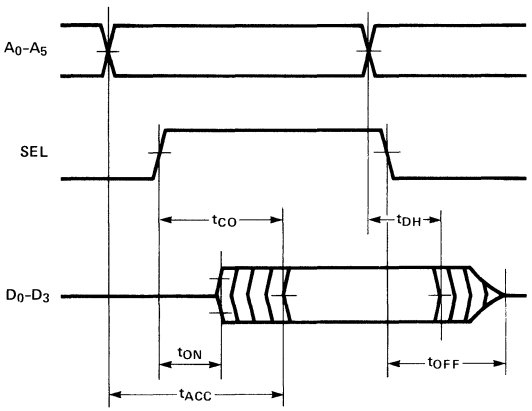
Block Diagram



Detailed Block Diagram



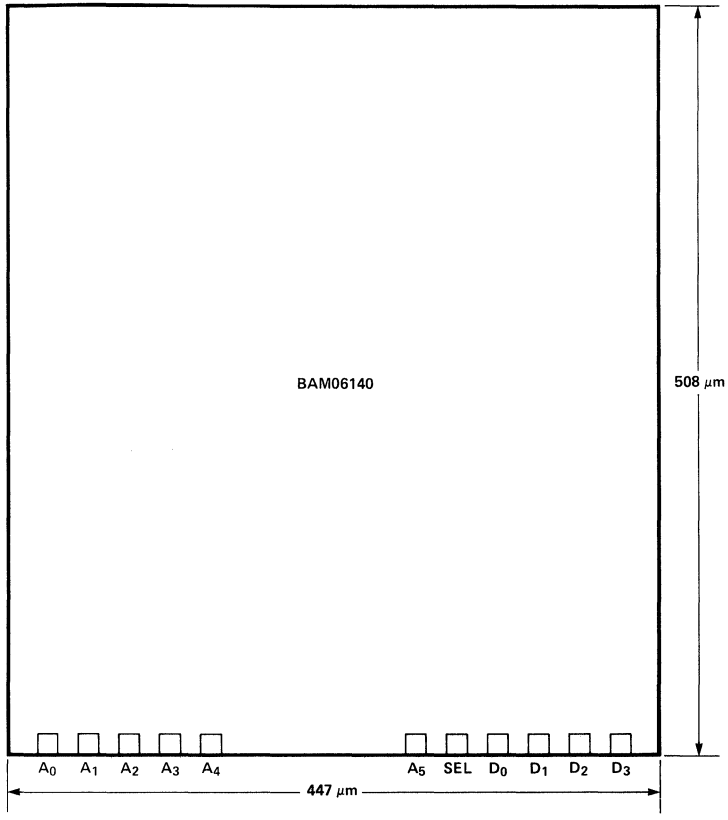
Dynamic Characteristics



Timing Parameters (T_A = 25° C, V_{DD} = 5.0 V)

Parameter	Symbol	Min.	Max.	Unit
ADDR Access Time	t_{ACC}	—	35	nsec
SEL Access Time	t_{CO}	—	10	nsec
Data Hold Time	t_{DH}	30	—	nsec
Driver Turn On Delay	t_{ON}	—	10	nsec
Driver Turn Off Delay	t_{OFF}	—	7	nsec

Outline Drawing



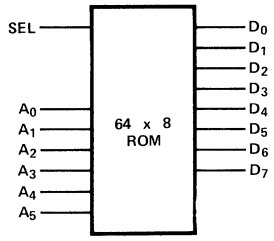
64 x 8 Static ROM

BAM06141

Description

The BAM06141 is a static ROM cell organized 64 words by 8 bits. It is activated by a single SEL input which causes the contents of the applied address to be presented on the cell outputs. When SEL is in its inactive state, the outputs are high impedance.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	547	μm
Cell Height	508	μm
Cell Area	278K	sq. μm
Average Power Dissipation*	8.0	mW
Input Capacitance (SEL, A_N)	0.080	pF
Input Capacitance (D_N)	0.040	pF

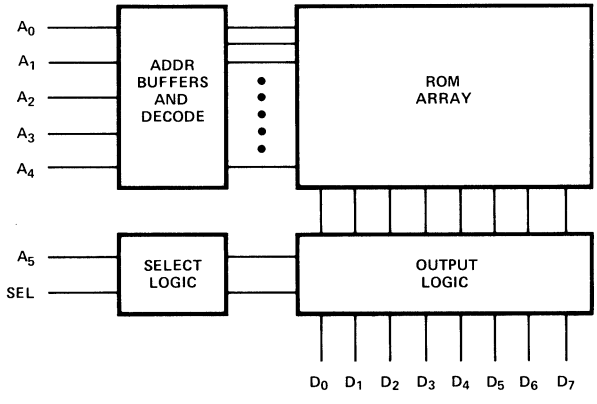
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

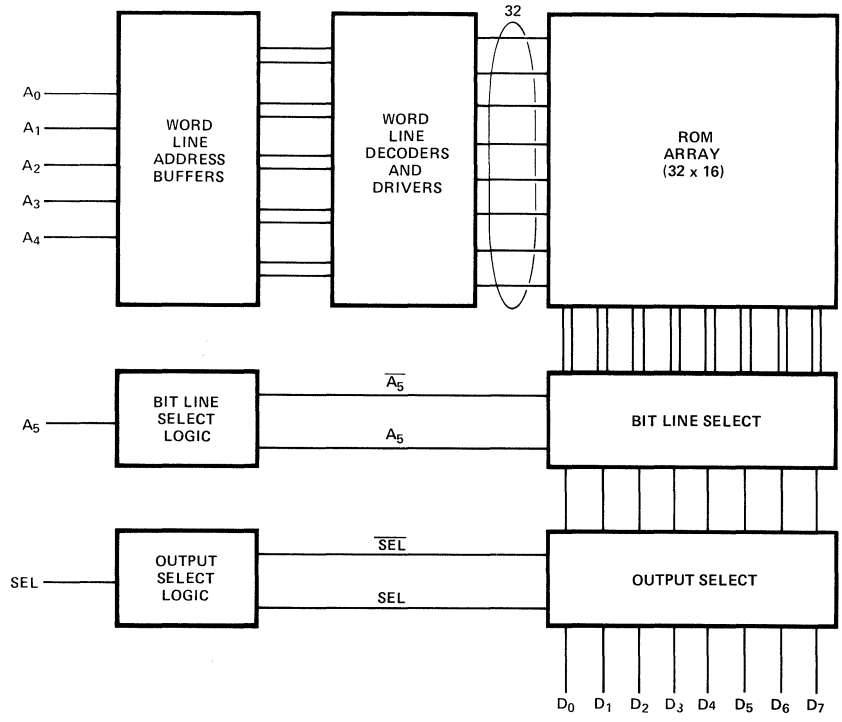
Input SEL	Outputs D_0-D_7
H	Active
L	Hi-Z

H = High level.
L = Low level.
Hi-Z = High impedance state.

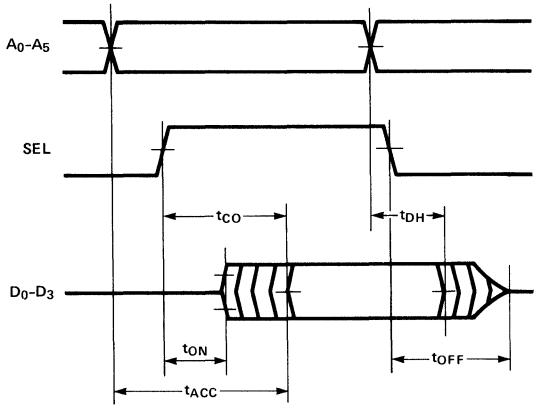
Block Diagram



Detailed Block Diagram



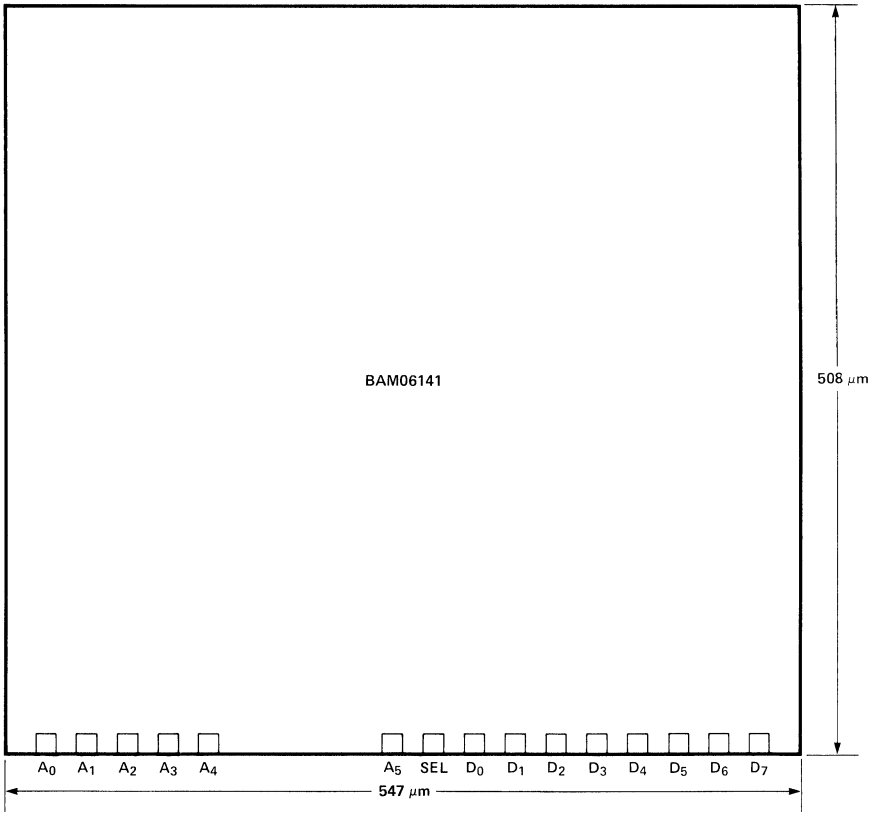
Dynamic Characteristics



Timing Parameters ($T_A = 25°C$, $V_{DD} = 5.0$ V)

Parameter	Symbol	Min.	Max.	Unit
ADDR Access Time	t_{ACC}	—	35	nsec
SEL Access Time	t_{CO}	—	10	nsec
Data Hold Time	t_{DH}	30	—	nsec
Driver Turn On Delay	t_{ON}	—	10	nsec
Driver Turn Off Delay	t_{OFF}	—	7	nsec

Outline Drawing



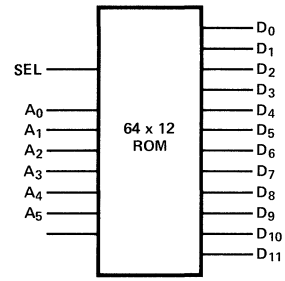
64 x 12 Static ROM

BAM06142

Description

The BAM06142 is a static ROM cell organized 64 words by 12 bits. It is activated by a single SEL input which causes the contents of the applied address to be presented on the cell outputs. When SEL is in its inactive state, the outputs are high impedance.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	639	μm
Cell Height	508	μm
Cell Area	325K	sq. μm
Average Power Dissipation*	8.0	mW
Input Capacitance (SEL, A_N)	0.080	pF
Input Capacitance (D_N)	0.040	pF

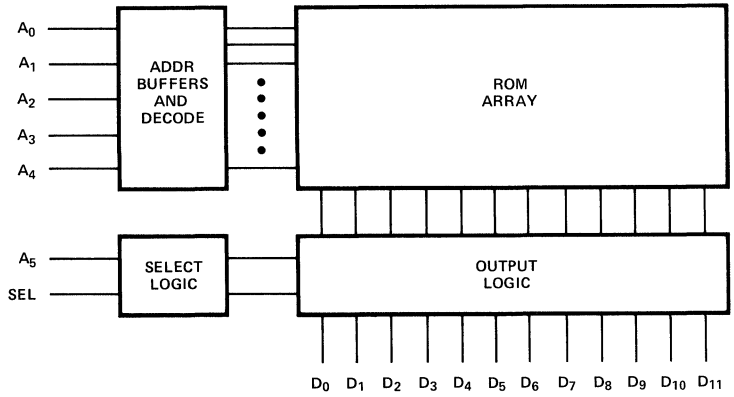
*V_{DD} = 5.0V, T_A = 25°C, C_L = 0.050 pF.

Function Table

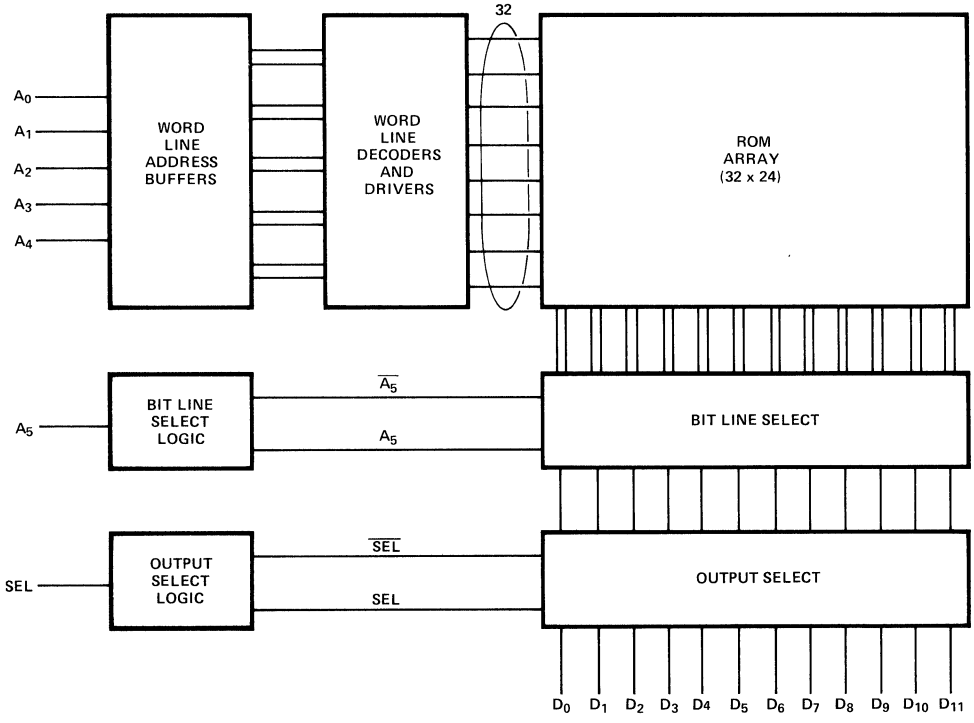
Input SEL	Outputs D_0-D_{11}
H	Active
L	Hi-Z

H = High level.
L = Low level.
Hi-Z = High impedance state.

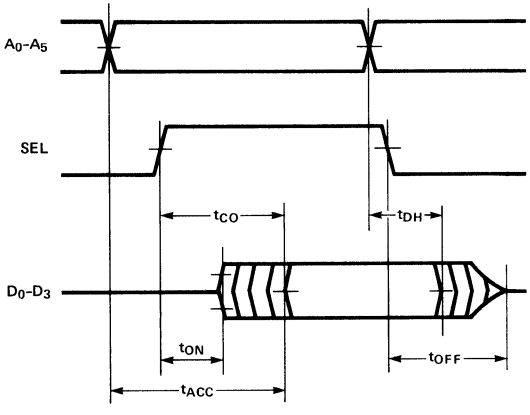
Block Diagram



Detailed Block Diagram



Dynamic Characteristics

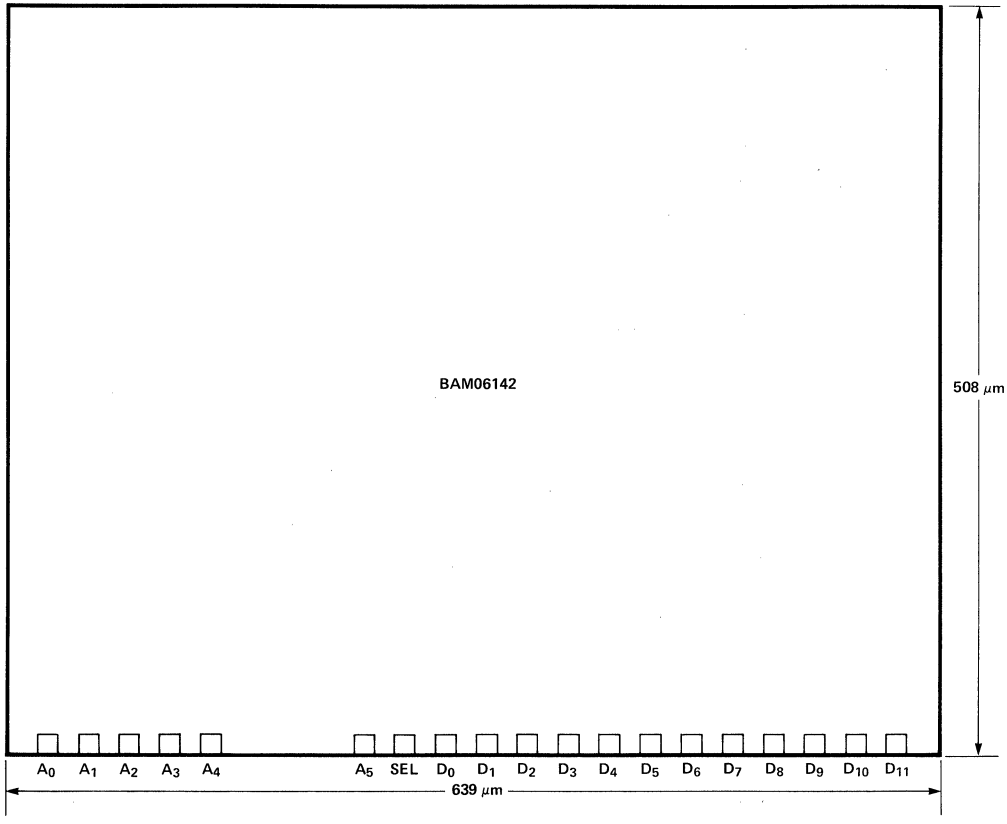


Timing Parameters (T_A = 25° C, V_{DD} = 5.0 V)

Parameter	Symbol	Min.	Max.	Unit
ADDR Access Time	t_{ACC}	—	35	nsec
SEL Access Time	t_{CO}	—	10	nsec
Data Hold Time	t_{DH}	30	—	nsec
Driver Turn On Delay	t_{ON}	—	10	nsec
Driver Turn Off Delay	t_{OFF}	—	7	nsec

MEMORIES

Outline Drawing



Miscellaneous

14

Synertek.

GND Connection Cell

BAMGND

Description

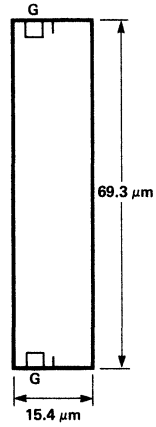
The BAMGND cell is a simple cell which permits connections to the GND bus.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	15.4	μm
Cell Height	69.3	μm
Cell Area	1.1K	Sq. μm

Outline Drawing



V_{DD} Connection Cell

BAMV$_{DD}$

Description

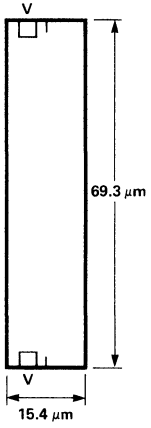
The BAMV$_{DD}$ cell is a simple cell which permits connections to the V_{DD} bus.

Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	15.4	μm
Cell Height	69.3	μm
Cell Area	1.1K	Sq. μm

Outline Drawing



Synchronous Clock Gate

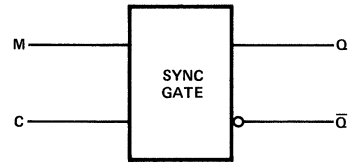
PRELIMINARY

BAM00106

Description

The BAM00106 is a circuit which performs the function of a gate which passes or blocks clock pulses in a synchronous fashion. Clock pulse width and synchronism are preserved after gating. A high level on the M (Mask) input opens the gate and a low level closes the gate. When the gate is open, Q follows the C input. When closed, Q is low. A transitions are synchronous with the low-to-high edge of the C input.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	177.1	μm
Cell Height	69.3	μm
Cell Area	12.3K	Sq. μm
Average Power Dissipation*	27	μW/MHz
Input Capacitance (M)	0.130	pF
Input Capacitance (C)	0.270	pF

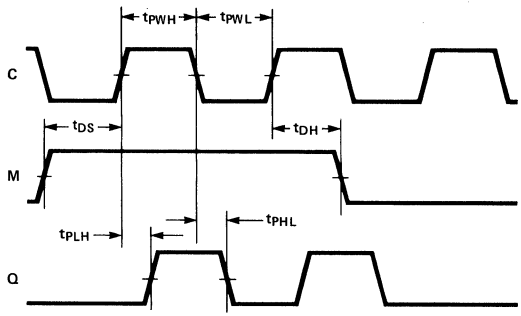
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs		Outputs	
M	C	Q	$\overline{Q}$
L	X	L	H
H	↑	↑	↓
H	↓	↓	↑

H = High level.
L = Low level.
X = "Don't care."

Dynamic Characteristics



($\overline{Q}$ IS THE INVERSE OF Q)

Minimum Pulse Widths:

t_{PWH} = 7 nsec

t_{PWL} = 7 nsec

t_{PWM} = 10 nsec

Minimum Set-up and Hold Times:

t_{DS} = 6 nsec

t_{DH} = 3 nsec

Maximum Propagation Delays:

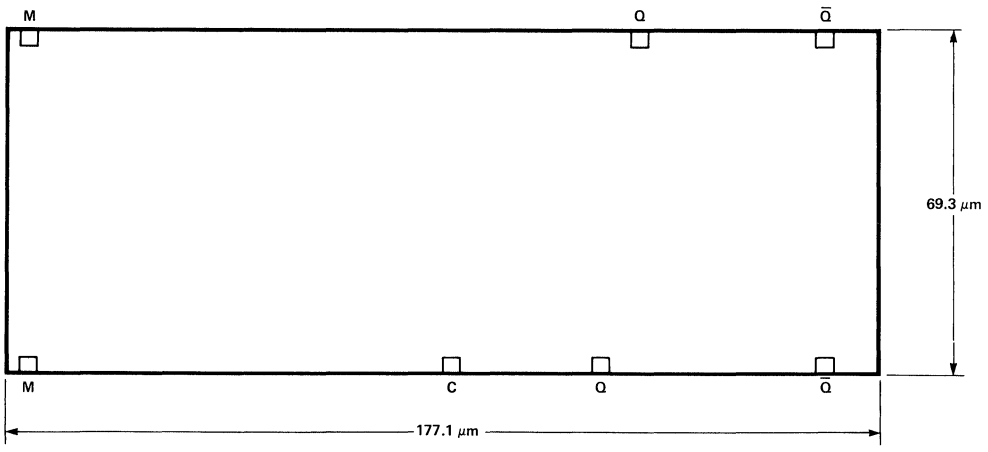
$t_{PHL} = 2 (C_L) + 2$ nsec

$t_{PLH} = 2 (C_L) + 4$ nsec

Maximum Clock Rate:

$$f_{CLK} = \frac{1}{t_{PWH} + t_{PWL}} = 70 \text{ MHz}$$

Outline Drawing



Data Synchronizer

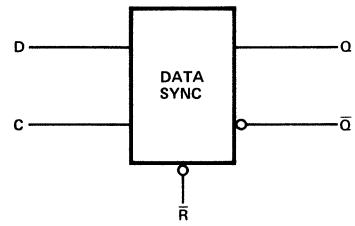
PRELIMINARY

BAM00107

Description

The BAM00107 is a Data Synchronizer circuit which synchronizes incoming data to an internal clock. It consists of a D Flip-Flop followed by a Set-Reset Latch. This combination causes incoming asynchronous data streams to be locked into sync, even when marginal timing conditions exist.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	300.3	μm
Cell Height	69.3	μm
Cell Area	20.8K	Sq. μm
Average Power Dissipation*	35	μW/MHz
Input Capacitance (D)	0.040	pF
Input Capacitance (C, C̄)	0.230	pF
Input Capacitance (R̄)	0.200	pF

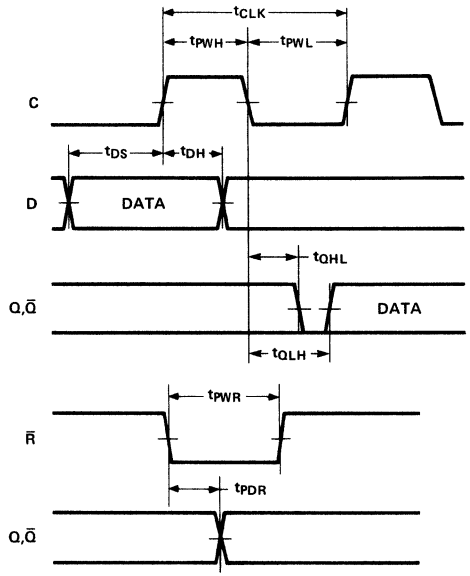
*V_{DD} = 5.0V, T_A = 25° C, C_L = 0.050 pF.

Function Table

Inputs			Outputs	
R̄	D	C	Q	Q̄
L	X	X	L	H
H	H	↑	↑	↓
H	L	↓	↓	↑

H = High level.
L = Low level.

Dynamic Characteristics



Minimum Pulse Widths:

t_{PWH} = 7 nsec

t_{PWL} = 7 nsec

t_{PWR} = 7 nsec

Maximum Propagation Delays:

$t_{QHL} = 2.5\ (C_L) + 5$ nsec

$t_{QLH} = 2.5\ (C_L) + 6$ nsec

$t_{PDR} = 2.5\ (C_L) + 9$ nsec

Minimum Set-up/Hold Times:

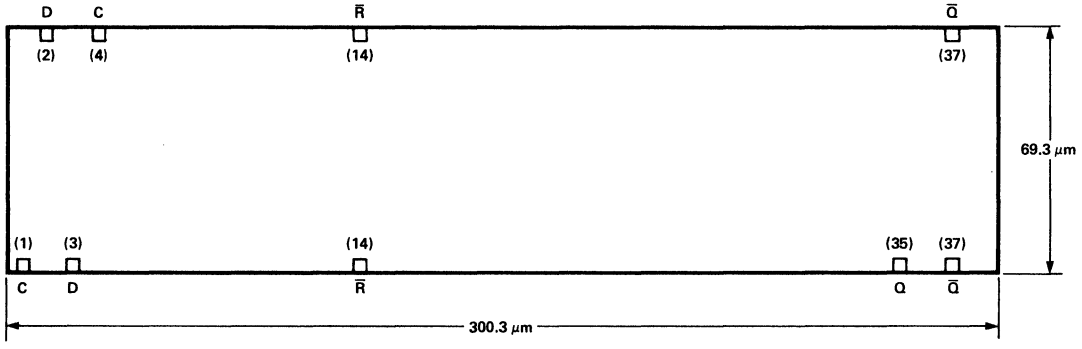
t_{DS} = 7 nsec

t_{DH} = 0 nsec

Maximum Clock Rates:

$$f_{CLK} = \frac{1}{t_{CLK}} = 70 \text{ MHz}$$

Outline Drawing



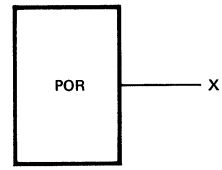
Power-On-Reset Generator

BAM00200

Description

The BAM00200 is a cell that generates a system reset signal when V_{DD} power is applied.

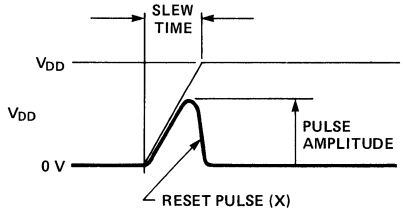
Logic Symbol

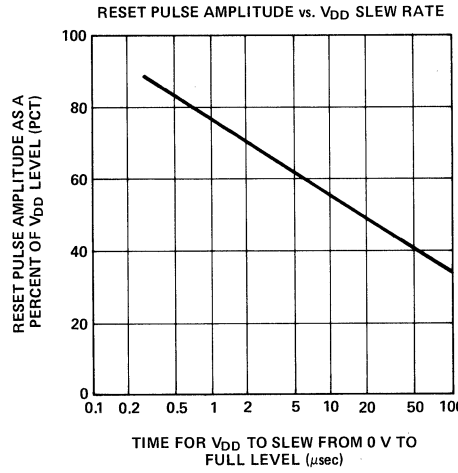


Cell Parameters

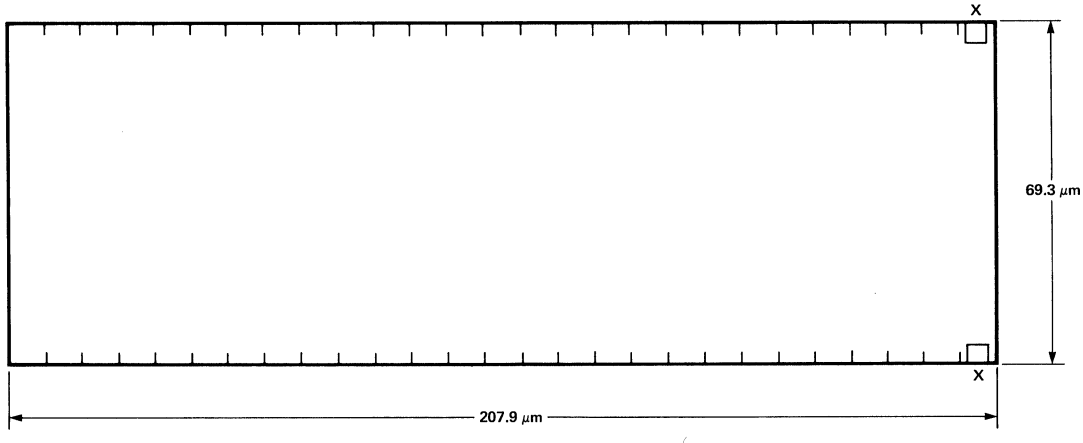
Parameter	Value	Unit
Cell Width	207.9	μm
Cell Height	69.3	μm
Cell Area	14.4K	Sq. μm
Average Power Dissipation	0	μW/MHz

Dynamic Characteristics





Outline Drawing



Resistor Pull-Up Load

BAM00210

Description

The BAM00210 is a cell whose function is that of a passive pull-up resistor. It is implemented by the use of a single n-channel transistor whose "on" impedance is relatively high.

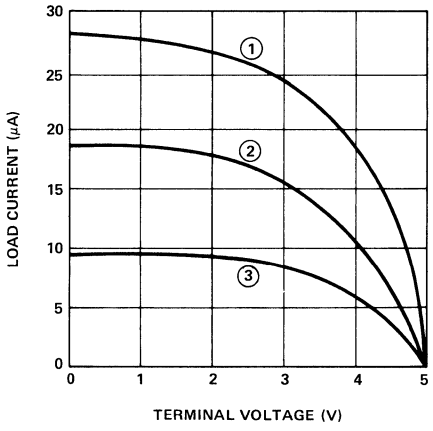
Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	23.1	μm
Cell Height	69.3	μm
Cell Area	1.6K	Sq. μm
Average Power Dissipation*	26.0	μW
Input Capacitance	0.025	pF
Typical Resistance**	250K	ohm

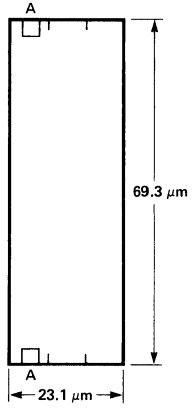
*V_{DD} = 5.0V, T_A = 25°C, 50% duty cycle.
**See graph for details.

CURRENT vs. VOLTAGE



(1) = 0°C, WORST-CASE PROCESS.
(2) = 25°C, NOMINAL PROCESS.
(3) = 70°C, WORST-CASE PROCESS.

Outline Drawing



MISCELLANEOUS

Resistor Pull-Down Load

BAM00220

Description

The BAM00220 is a cell whose function is that of a passive pull-down resistor. It is implemented by the use of a single p-channel transistor whose "on" impedance is relatively high.

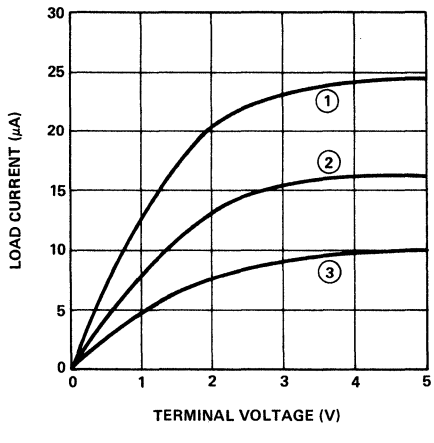
Logic Symbol

Cell Parameters

Parameter	Value	Unit
Cell Width	23.1	μm
Cell Height	69.3	μm
Cell Area	1.6K	Sq. μm
Average Power Dissipation*	26.0	μW
Input Capacitance	0.025	pF
Typical Resistance**	250K	ohm

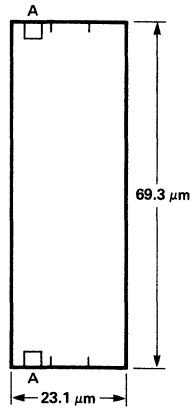
*V_{DD} = 5.0V, T_A = 25°C, 50% duty cycle.
**See graph for details.

CURRENT vs. VOLTAGE



① = 0°C, WORST-CASE PROCESS.
② = 25°C, NOMINAL PROCESS.
③ = 70°C, WORST-CASE PROCESS.

Outline Drawing



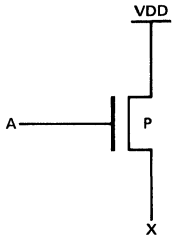
p-Channel Pull-up Transistor

BAM00055

Description

The BAM00055 is an HCMOS cell containing a single p-channel MOS transistor whose source is connected to V_{DD} and whose gate and drain are the available connections. The primary application is for precharging internal bus lines and selected nodes.

Logic Symbol



Cell Parameters

Parameter	Value	Unit
Cell Width	15.4	μm
Cell Height	69.3	μm
Cell Area	1.1K	Sq. μm
Average Power Dissipation*	0	μW/MHz
Input Capacitance	0.030	pF

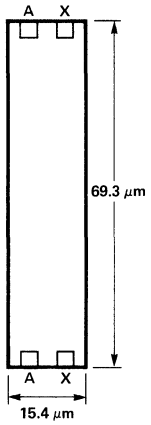
*Strictly load capacitance charging currents.

Function Table

Inputs	Output
A	X
L	V_{DD}
H	Hi-Z

H = High level.
L = Low level.

Outline Drawing



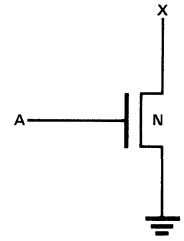
n-Channel Pull-down Transistor

BAM00056

Description

The BAM00056 is an HCMOS cell containing a single n-channel MOS transistor whose source is connected to V_{SS} and whose gate and drain are the available connections. The primary application is for discharging internal bus lines and selected nodes.

Logic Symbol



Cell Parameters

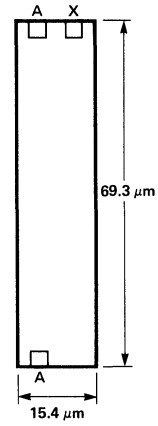
Parameter	Value	Unit
Cell Width	15.4	μm
Cell Height	69.3	μm
Cell Area	1.1K	Sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance	0.030	pF

Function Table

Inputs A	Output B
L	Hi-Z
H	V_{SS}

H = High level.
L = Low level.

Outline Drawing



Transmission Gate

BAM00070

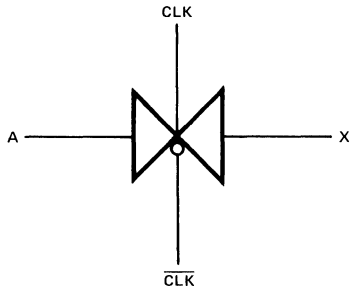
Description

The BAM00070 is an HCMOS cell that performs the logic function of a feedthrough transmission gate.

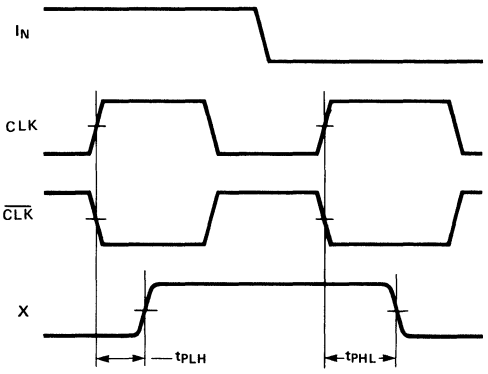
Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	Sq. μm
Average Power Dissipation	0	μW/MHz
Input Capacitance (CLK, $\overline{CLK}$)	0.040	pF
Input Capacitance (A)	0.025	pF
"ON" Resistance (Typ.)	6.7K	Ω

Logic Symbol



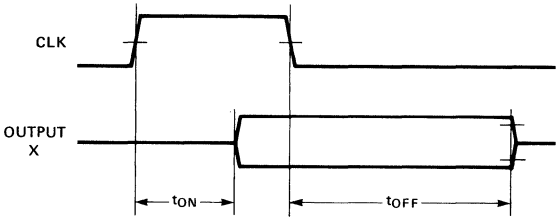
Dynamic Characteristics



Propagation Delays: (in nsec):

$t_{PHL} = 10\ (C_L) + 2$

$t_{PLH} = 12\ (C_L) + 2$



Switching Delays (in nsec):

$t_{ON} = t_{OFF} = 2.0$ nsec

Output Ramp Times:

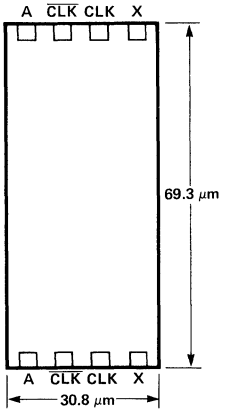
Dependent upon the driving source at the transfer gate input. A direct connection to V_{DD} or V_{SS} will result in a ramp time having a time constant of RC, where R is the "ON" resistance of the gate and C_L is the load capacitance.

Function Table

Inputs		Transfer Impedance
CLK	$\overline{CLK}$	
H	L	Low (ON)
L	H	High (OFF)
L	L	Undefined
H	H	Undefined

H = High level.
L = Low level.

Outline Drawing



MISCELLANEOUS

Transmission Gate with Enable Inverter

BAM00071

Description

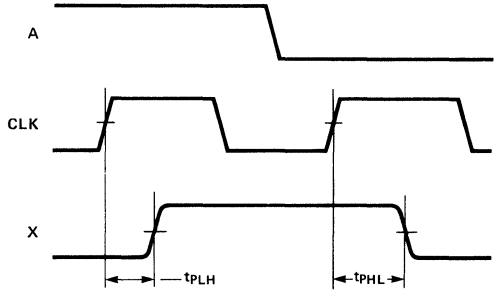
The BAM00071 is an HCMOS cell that performs the function of a feedthrough transmission gate. A positive-true clock enable signal activates the gate.

Cell Parameters

Parameter	Value	Unit
Cell Width	30.8	μm
Cell Height	69.3	μm
Cell Area	2.1K	sq. μm
Average Power Dissipation*	3.0	μW/MHz
Input Capacitance (A)	0.250	pF
Input Capacitance (CLK)	0.070	pF

*V_{DD} = 5.0V, T_A = 25° C.
(Independent of output capacitance).

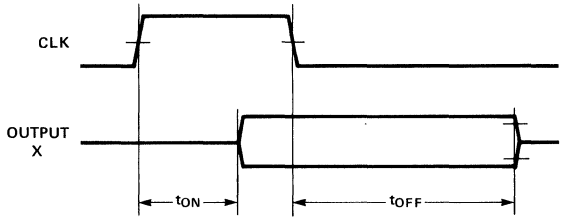
Dynamic Characteristics



Propagation Delays (in nsec):

t_{PHL} = 10 (C_L) + 3

t_{PLH} = 12 (C_L) + 3



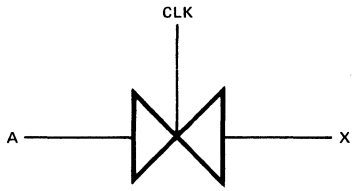
Switching Delays (in nsec):

t_{ON} = t_{OFF} = 5.0 nsec

Output Ramp Times:

Dependent upon the driving source at the transfer gate input. A direct connection to V_{DD} or V_{SS} will result in a ramp time having a time constant of RC, where R is the "ON" resistance of the gate and C_L is the load capacitance.

Logic Symbol

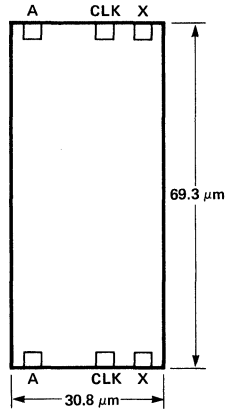


Function Table

CLK Input	Transmission Impedance (A-X)
L	High (OFF)
H	Low (ON)

H = High level.
L = Low level.

Outline Drawing



Life Support Policy:

Synertek products are not authorized for use as critical components in life support devices or systems without the express written approval of Synertek. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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