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Introduction

Synertek, founded in 1973, has developed a broad line of MOS/LSI circuits. Today, these devices include Shift Registers, "N" MOS Static RAMs, "C" MOS Static RAMs, ROMs, EPROMs, a full complement of Systems, an expanding family of Microprocessors, timekeeping circuits, and finally a unique capability for custom MOS circuits. Synertek's fabrication capability includes advanced "N" channel, "P" channel, CMOS depletion load and HMOS Silicon Gate processes.

Synertek, a recognized leader in ROM capability, can handle many different types of customer inputs with turn-around times for prototypes of less than 2 to 3 weeks. Assembly capacity is located both here in the U.S. as well as in offshore facilities.

Custom MOS circuit design and production are an integral part of Synertek's present and future business plans. Whether the circuit design project starts at the feasibility stage or at the point where our customers provide tooling (reticles, tapes, etc.), Synertek is organized to quickly and efficiently handle the most difficult custom design.

This catalog provides complete technical information on our expanding line of Synertek Memories, Microprocessors, Timekeeping Circuits, Systems, and Custom capability. Additional information may be obtained by contacting your local Synertek Representative or Distributor, or by contacting Product Marketing in Santa Clara, California at (408) 988-5600.



Synertek[®], Inc.
1979 Data Catalog

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*Numerical Index, Functional Index
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Product Replacement Guide

Synertek
INCORPORATED

Random Access Memory (RAM)

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AMD		AM9111EPC	SYP21H11-2	21L02AP	SYP21L02-1
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AM9114BDC	SYC2114	P2112	SYP2112	21L02BP	SYP21L02B
AM91L14BPC	SYP2114L	C2112	SYC2112	21L02AP	SYP21L02-1
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AM9114CPC	SYP2114-3	AM9112ADC	SYC2112-1	21L02BP	SYP21L02B
AM9114CDC	SYC2114-3	AM9112BPC	SYP2112A	21L02BD	SYC21L02B
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AM91L14CDC	SYC2114L-3	AM9112DPC	SYP2112A-2	MB8114N	SYP2114-3
AM9114EPC	SYP2114-2	AM9112DPC	SYC2112A-2	MB8114NL	SYP2114L-3
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AM91L42-3BPC	SYP2142L-3	EMM		UB8112N	SYP2112A-4
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AM9142-2BPC	SYP2142-2	2114UCA	SYC2114	Hitachi	
AM9142-2BDC	SYC2142-2	2114UCE	SYD2114	HM472114-4	SYC2114L
AM91L42-2BPC	SYP2142L-2	L2114UCB	SYP2114L	HM435101-1	SYC5101L-1
AM91L42-2BDC	SYC2142L-2	L2114UCA	SYC2114L	HM435101	SYC5101L
AM9102APC	SYP2102-1	L2114UCA	SYC2114L	Intel	
AM9102ADC	SYC2102-1	L2114UCE	SYD2114L	P2114	SYP2114
AM9102DPC	SYP2102A-2	2114-3CB	SYP2114-3	C2114	SYC2114
AM9102DDC	SYC2102A-2	2114-3CA	SYC2114-3	D2114	SYD2114
AM9102EPC	SYP21H02-2	2114-3CE	SYD2114-3	P2114L	SYP2114L
AM9102EDC	SYC21H02-2	L2114-3CB	SYP2114L-3	C2114L	SYC2114L
AM91L02APC	SYP21L02-1	L2114-3CA	SYC2114L-3	D2114L	SYD2114L
AM91L02ADC	SYC21L02-1	L2114-3CE	SYD2114L-3	P2114-3	SYP2114-3
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AM9101DPC	SYP2101A-2	Fairchild		C2114-2	SYC2114-2
AM9101DDC	SYC2101A-2	2102P	SYP2102	D2114-2	SYC2114-2
AM9101EPC	SYP21H01-2	2102D	SYC2102	P2114L-2	SYP2114L-2
AM9101EDC	SYC21H01-2	2102-2P	SYP2102-1	C2114L-2	SYC2114L-2
P2111	SYP2111	2102-2D	SYC2102-1	D2114L-2	SYD2114L-2
C2111	SYC2111	2102-1P	SYP2102A-4	P2142	SYP2142
AM9111APC	SYP2111-1	2102-1D	SYC2102A-4	C2142	SYC2142
AM9111ADC	SYC2111-1	2102FP	SYP2102A-2	2142L	SYP2142L
AM9111BPC	SYP2111A	2102FD	SYC2102A-2	C2142L	SYC2142L
AM9111BDC	SYC2111A			P2142-3	SYP2142-3
AM9111DPC	SYP2111A-2				
AM9111DDC	SYC2111A-2				

PART NUMBER	REPLACE WITH	PART NUMBER	REPLACE WITH	PART NUMBER	REPLACE WITH
C2142-3	SYC2142-3	P21143	SYP2114-3	2102A-2B	SYP2102A-2
P2142L-3	SYP2142L-3	D21143	SYD2114-3	2102A-2IJA	SYC2102A-2
C2142L-3	SYC2142L-3	P2114L3	SYP2114L-3	21L02B	SYP21L02
P2142-2	SYP2142-2	D2114L3	SYD2114L-3	21L02IJA	SYC21L02
C2142-2	SYC2142-2	P21142	SYP2114-2	21L02-1B	SYP21L02-1
P2142L-2	SYP2142L-2	D21142	SYC2114-2	21L02-1IJA	SYC21L02-1
C2142L-2	SYC2142L-2	P2114L2	SYP2114L-2	21F02B	SYP21L02B
P2102A-4	SYP2102A-4	D2114L2	SYD2114L-2	21F02IJA	SYC21L02B
C2102A-4	SYC2102A-4	<i>Motorola</i>		2102AB	SYP21L02A
D2102A-4	SYD2102A-4	MCM2114P-45	SYP2114	2102AIJA	SYC21L02A
P2102A-2	SYP2102A-2	MCM2114C-45	SYC2114	2102AL-4B	SYP21L02BL
C2102A-2	SYC2102A-2	MCM21L14P-45	SYP2114L	2102AL-4IJA	SYC21L02BL
D2102A-2	SYD2102A-2	MCM21L14C-45	SYC2114L	2102ALB	SYP21L02AL
P2102A	SYP21L02B	MCM2114P-30	SYP2114-3	2102ALIJA	SYC21L02AL
C2102A	SYC21L02B	MCM2114C-30	SYC2114-3	2101XC	SYP2101-1
D2102B	SYD21L02B	MCM21L14P-30	SYP2114L-3	2101IMA	SYC2101-1
P2102AL-4	SYP21L02BL	MCM21L14C-30	SYC2114L-3	2101-1XC	SYP2101-1
P2102AL	SYP21L02AL	MCM21L14P-20	SYP2114-2	2101IMA	SYC2101-1
P2101A-4	SYP2101A-4	MCM2114C-20	SYC2114-2	2111XA	SYP2111
C2101A-4	SYC2101A-4	MCM21L14P-20	SYP2114L-2	2111IKA	SYC2111
P2101A	SYP2101A	MCM21L14C-20	SYC2114L-2	2111-1XA	SYP2111-1
C2101A	SYC2101A	<i>National</i>		2111-1IKA	SYC2111-1
P2101A-2	SYP2101A-2	MM2102N	SYP2102	2112B	SYP2112
C2101A-2	SYC2101A-2	MM2102D	SYC2102	2112IJA	SYC2112
P2111A-4	SYP2111A-4	MM2102N	SYP21L02	2112-1B	SYP2112-1
C2111A-4	SYC2111A-4	MM2102D	SYC21L02	2112-1IJA	SYC2112-1
D2111A-4	SYD2111A-4	MM2102-1N	SYP21L02-1	<i>T.I.</i>	
P2111A	SYP2111A	MM2102-1D	SYC21L02-1	TMS4045-45NL	SYP2114
C2111A	SYC2111A	MM2102AN	SYP21L02A	TMS4045-45JL	SYC2114
D2111A	SYD2111A	MM2102AD	SYC21L02A	TMS40L45-45NL	SYP2114L
P2111A-2	SYP2111A-2	MM2102A-4N	SYP21L02B	TMS40L45-45JL	SYC2114L
C2111A-2	SYC2111A-2	MM2102A-4D	SYC21L02B	TMS4045-30NL	SYP2114-3
D2111A-2	SYD2111A-2	MM2101-1N	SYP2101-1	TMS4045-30JL	SYC2114-3
P2112A-4	SYP2112A-4	MM2101-1D	SYC2101-1	TMS40L45-30NL	SYP2114L-3
C2112A-4	SYC2112A-4	MM2111N	SYP2111	TMS40L45-30JL	SYC2114L-3
D2112A-4	SYD2112A-4	MM2111D	SYC2111	TMS4045-20NL	SYP2114-2
P2112A	SYP2112A	MM2111-1N	SYP2111-1	TMS4045-20JL	SYC2114-2
C2112A	SYC2112A	MM2111-1D	SYC2111-1	TMS4035-NL	SYP2102
D2112A	SYD2112A	MM2112N	SYP2112	TMS4035JL	SYC2102
P2112A-2	SYP2112A-2	MM2112D	SYC2112	TMS4033NL	SYP2102A-4
C2112A-2	SYC2112A-2	<i>NEC</i>		TMS4033JL	SYC2102A-4
D2112A-2	SYD2112A-2	MPD5101L-1	SYP5101L-1	TMS4039NL	SYP2101-1
P5101L-1	SYP5101L-1	MPD5101L	SYP5101L	TMS4039JL	SYC2101-1
C5101L-1	SYC5101L-1	<i>Signetics</i>		TMS4039-1NL	SYP2101A-4
P5101L	SYP5101L	2102B	SYP2102	TMS4039-1JL	SYC2101A-4
C5101L	SYC5101L	2102IJA	SYC2102	TMS4042NL	SYP2111
P5101L-3	SYP5101L-3	2102-1B	SYP2102-1	TMS4042JL	SYC2111
C5101L-3	SYC5101L-3	2102-1IJA	SYC2102-1	TMS4042-2NL	SYP2111A-4
<i>Intersil</i>		2102A-4B	SYP2102A-4	TMS4042-2JL	SYC2111A-4
P2114	SYP2114	2102A-4IJA	SYC2102A-4	TMS4043NL	SYP2112
D2114	SYD2114				
P2114L	SYP2114L				
D2114L	SYD2114L				

Read-Only Memory (ROM)

PART NUMBER	REPLACE WITH	PART NUMBER	REPLACE WITH	PART NUMBER	REPLACE WITH
AMD		RO-3-9316C	SYP2316B-3	NEC	
AM9217BPC	SYP2316A	RO-3-9332B	SYP2332	UPD2316A	SYP2316A
AM9217BDC	SYC2316A	<i>Intel</i>		UPD2316E	SYP2316B
AM9218BPC	SYP2316B	P2316A	SYP2316A	UPD2332	SYP2332
AM9218BDC	SYC2316B	C2316A	SYC2316A	<i>Signetics</i>	
AM9218CPC	SYP2316B-3	P2316E	SYP2316B	2616N	SYP2316B
AM9218CDC	SYC2316B-3	C2316E	SYC2316B	2616INC	SYC2316B
AM9232BPC	SYP2332	<i>Motorola</i>		2616-1N	SYP2316B-3
AM9232BDC	SYC2332	MCM68316A	SYP2316A	2616-1INC	SYC2316B-3
AMI		MCM68316E	SYP2316B	2633N	SYP2332
S6831A	SYP2316A	MCM68332	SYP2332	2633INC	SYC2332
S6831B	SYP2316B	<i>National</i>		<i>T.I.</i>	
EA		MM2316A	SYP2316A	TMS4732NL	SYP2332
EA2316A	SYP2316A	MM5258	SYP2316B	TMS4732JL	SYC2332
EA2316E	SYP2316B	MM52116	SYP2316B		
GI		MM52132	SYP2332		
RO-3-9316A	SYP2316A				
RO-3-9316B	SYP2316B				

Shift Registers

PART NUMBER	REPLACE WITH	PART NUMBER	REPLACE WITH	PART NUMBER	REPLACE WITH
AMD		AM2803PC	SYP2803A	MM5027D	SYC2827
AM1402APC	SYP1402A	AM2803HC	SYT2803A	MM5058N	SYP2533
AM1402A	SYC1402A	AM2804PC	SYP2804A	MM5058D	SYC2533
AM1403APC	SYP1403A	AM2804HC	SYT2804A	<i>Signetics</i>	
AM1403A	SYT1403A	<i>Intel</i>		2502B	SYP1402A
AM1404APC	SYP1404A	P2401	SYP2401	2502I	SYC1402A
AM1404A	SYT1404A	C2401	SYC2401	2503V	SYP1403A
AM9401PC	SYP2401	<i>National</i>		2503TA	SYT1403A
AM9401DC	SYC2401	MM1402AN	SYP1402A	2504V	SYP1404A
AM2825PC	SYP2825A	MM1402AD	SYC1402A	2504TA	SYT1404A
AM2825DC	SYC2825A	MM1403AN	SYP1403A	2533V	SYP2533
AM2826PC	SYP2826	MM1403AH	SYT1403A	2502	SYP2802A
AM2826DC	SYC2826	MM1404AN	SYP1404A	2503	SYP2803A
AM2827PC	SYP2827	MM1404AH	SYT1404A	2504	SYP2804A
AM2827DC	SYC2827	MM5025N	SYP2825A		
AM2533V	SYP2533	MM5025D	SYC2825A		
AM2533DC	SYC2533	MM5026N	SYP2826		
AM2833PC	SYP2833	MM5026D	SYC2826		
AM2833DC	SYC2833	MM5027N	SYP2827		
AM2802PC	SYP2802A				
AM2802DC	SYC2802A				

Shift Registers

Shift Registers



1024-Bit Dynamic Shift Registers

Quad, Dual, Single

SY1402A, SY1403A, SY1404A

MEMORY PRODUCTS

- Synertek ion implanted silicon gate process
- 5 MHz data rate—minimum
- 2.5 MHz clock rate
- TTL, DTL compatible
- Reduced clock capacitance, 85 pF
- Reduced power dissipation, 80 μ W/bit at 1.0 MHz

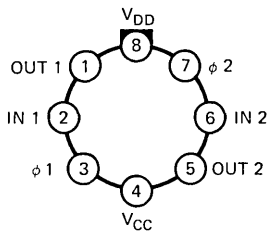
The SY1402A, 1403A and 1404A 2 ϕ dynamic shift registers utilize I/O multiplexing techniques to attain a 5.0 MHz data rate with a clock rate of only 2.5 MHz. The inputs and outputs are bipolar and MOS compatible for ease of implementation in a TTL, DTL and a high- or low-threshold MOS system.

silicon gate design. These savings directly affect the cost of the overhead circuitry (clock drivers, power supplies) for a shift register memory system.

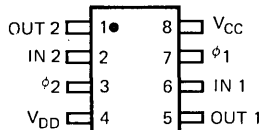
Clock power and V_{DD} current have been significantly reduced due to the advantages inherent in an ion implanted silicon gate design over a conventional

The SY1402A, 1403A and 1404A are used effectively in applications requiring low cost serial memory such as CRT refresh, line and page storage for facsimile transmitters and receivers, and character storage for high speed printers.

PIN CONFIGURATION

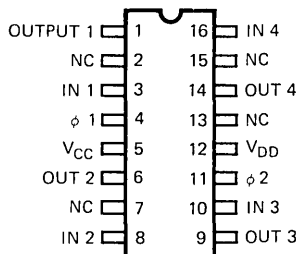


SYM1403A



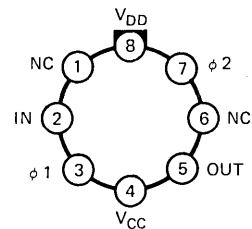
SYP1403A

PIN CONFIGURATION

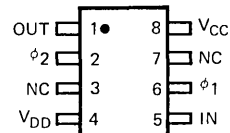


SYP1402A
SYC1402A

PIN CONFIGURATION



SYM1404A



SYP1404A

ORDERING INFORMATION

Order Number	Package Type	Organization	Temperature Range
SYP1404A	Plastic Dip	1024 x 1	0°C to +70°C
SYM1404A	TO Can	1024 x 1	0°C to +70°C
SYP1403A	Plastic Dip	512 x 2	0°C to +70°C
SYM1403A	TO Can	512 x 2	0°C to +70°C
SYP1402A	Plastic Dip	256 x 4	0°C to +70°C
SYC1402A	Ceramic Dip	256 x 4	0°C to +70°C



SHIFT
REGISTERS

ABSOLUTE MAXIMUM RATINGS¹

Temperature Under Bias	0°C to 70°C	Data and Clock Input Voltages	
Storage Temperature	-65°C to +160°C	and Supply Voltages with	
Power Dissipation ⁽²⁾	1 Watt	respect to V _{CC}	+0.5V to -20V

D.C. CHARACTERISTICS

 T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified

V_{DD} = -5V ±5% or -9V ±5%

Symbol	Test	Min.	Typ. ⁽³⁾	Max.	Unit	Conditions
I _{LI}	Input Load Current		<10	500	nA	T _A = 25°C
I _{LO}	Output Leakage Current		<10	1000	nA	V _{OUT} = 0.0V, T _A = 25°C
I _{LC}	Clock Leakage Current		10	1000	nA	Max. V _{IILC} , T _A = 25°C
V _{IL}	Input "Low" Voltage	V _{CC} -10		V _{CC} -4.2	V	
V _{IH}	Input "High" Voltage	V _{CC} -2		V _{CC} +3	V	

V_{DD} = -5V ±5%

I _{DD1}	Power Supply Current		15	20	mA	T _A = 25°C	Output at Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, V _{IILC} = V _{CC} -17V
I _{DD2}	Power Supply Current			22	mA	T _C = 0°C	
V _{IILC}	Clock Input Low Voltage	V _{CC} -17		V _{CC} -15	V		
V _{IHC}	Clock Input High Voltage	V _{CC} -1		V _{CC} +3	V		
V _{OL}	Output Low Voltage		-3	0.5	V	R _{L1} = 3K to V _{DD} , I _{OL} = 1.6 mA	
V _{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R _{L1} = 3K to V _{DD} , I _{OH} = -100 μA	
V _{OH2}	Output High Voltage Driving MOS	V _{CC} -1.6	V _{CC} -1		V	R _{L2} = 4.7K to V _{DD} (See p. 4 for connection)	

V_{DD} = -9V ±5%

I _{DD3}	Power Supply Current		15	20	mA	T _A = 25°C	Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, V _{IILC} = V _{CC} -14.7V
I _{DD4}	Power Supply Current			22	mA	T _C = 0°C	
V _{IILC}	Clock Input Low Voltage	V _{CC} -14.7		V _{CC} -12.6	V		
V _{IHC}	Clock Input High Voltage	V _{CC} -1		V _{CC} +3	V	R _{L1} = 4.7K to V _{DD} , I _{OL} = 1.6 mA	
V _{OL}	Output Low Voltage		-3	0.5	V	R _{L1} = 4.7K to V _{DD} , I _{OL} = 1.6 mA	
V _{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R _{L1} = 4.7K to V _{DD} , I _{OH} = -100 μA	
V _{OH2}	Output High Voltage Driving MOS	V _{CC} -1.9	V _{CC} -1		V	R _{L2} = 6.2K to V _{DD} R _{L3} = 3.9K to V _{CC}	(See p. 4 for connection)

Note 1: Stresses listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The 1 watt dissipation is not to be construed as an operating rating (see note 1). For operating at elevated temperatures the device must be derated based as shown on page 4. When operating at V_{DD} = -5V ±5% the maximum duty cycle is 33% and at V_{DD} = -9V ±5% the maximum duty cycle is 26%. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = [t_{LOW} / (t_{LOW} + t_{HIGH})] x clock rate.

Note 3: Typical values are at T_A = 25°C and at nominal voltages.

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = +5V \pm 5\%$

Symbol	Test	$V_{DD} = -5V \pm 5\%$ (Test Load 1)		$V_{DD} = -9V \pm 5\%$ (Test Load 2)		Unit
		Min.	Max.	Min.	Max.	
Frequency	Clock Rep Rate		2.5		1.5	MHz
Frequency	Data Rep Rate	Note 1	5.0	Note 1	3.0	MHz
$t_{\phi PW}$	Clock Pulse Width	.130	10	.170	10	μsec
$t_{\phi D}$	Clock Pulse Delay	10	Note 1	10	Note 1	nsec
t_R, t_F	Clock Pulse Transition		1000		1000	nsec
t_{DW}	Data Write Time (Set Up)	30		60		nsec
t_{DH}	Data To Clock Hold Time	20		20		nsec
t_{A+}, t_{A-}	Clock To Data Out Delay		90		110	nsec

CAPACITANCE ² $V_{CC} = +5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$ or $-9V \pm 5\%$, $T_A = 25^\circ\text{C}$

Symbol	Test	Typ.	Max.	Conditions
C_{IN}	Input Capacitance	5 pF	10 pF	$V_{IN} = V_{CC}$
C_{OUT}	Output Capacitance	5 pF	10 pF	$V_{OUT} = V_{CC}$
C_{ϕ}	Clock Capacitance	70 pF	85 pF	$V_{\phi} = V_{CC}$
$C_{\phi 1\phi 2}$	Clock to Clock Capacitance	11 pF	16 pF	$V_{\phi} = V_{CC}$

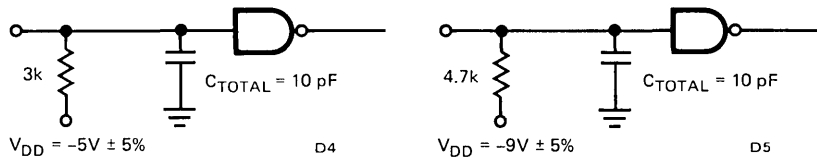
Note 1: See page 4 for guaranteed curve. Note 2: This parameter is periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

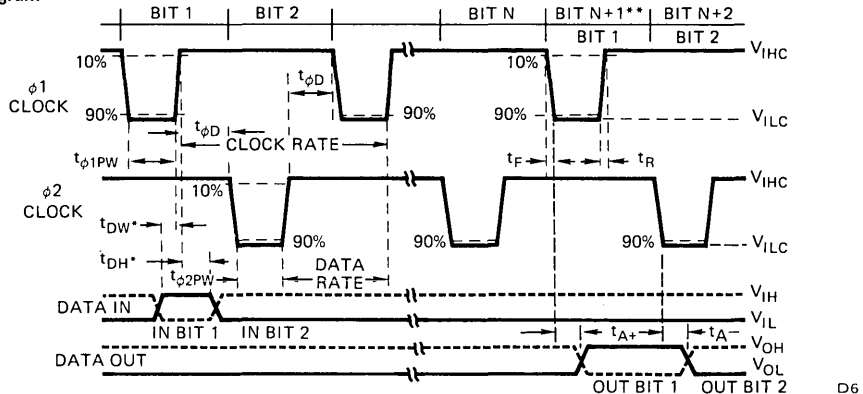
Conditions of Test

Input rise and fall times: 10 nsec

Output Load is 1 TTL gate



Timing Diagram

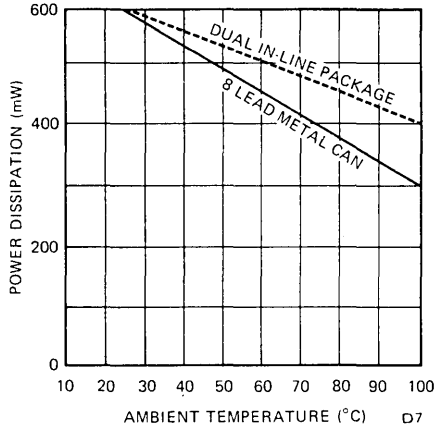


* t_{DW} and t_{DH} same for $t_{\phi 2}$

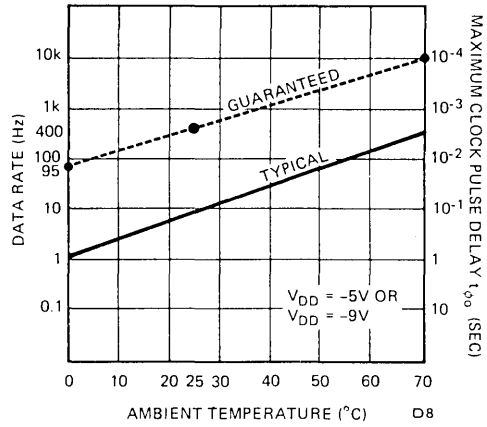
**N: 256 for SY1402A, N=512 for SY1403A, N=1024 for SY1404A



TYPICAL CHARACTERISTICS

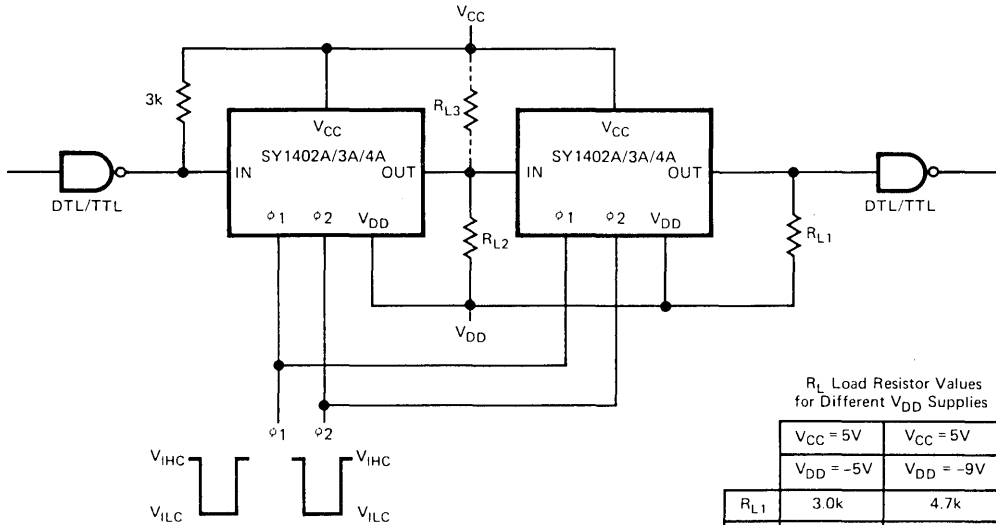


MAXIMUM ALLOWABLE POWER DISSIPATION



MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS. TEMPERATURE

DTL/TTL MOS Interfaces



R_L Load Resistor Values for Different V_{DD} Supplies

	$V_{CC} = 5V$ $V_{DD} = -5V$	$V_{CC} = 5V$ $V_{DD} = -9V$
R_{L1}	3.0k	4.7k
R_{L2}	4.7k	6.2k
R_{L3}	Not required	3.9k

D9



2048-Bit Dynamic Recirculating Shift Registers

SY2401

MEMORY PRODUCTS

SHIFT REGISTERS

- Single Supply Voltage - +5V
- Fully TTL Compatible - Inputs, Outputs and Clock
- Guaranteed 1MHz Operation (SY2401) or 2.5MHz Operation (SY2401-1) With 100pF Load, Over Temperature
- Low Power Dissipation - 150 μ W/Bit Typical at Maximum Clock Rate
- Low Clock Capacitance - 7pF
- Write/Recirculate and Chip Select Logic Incorporated on Chip
- Standard Configuration - Dual 1024 Bit

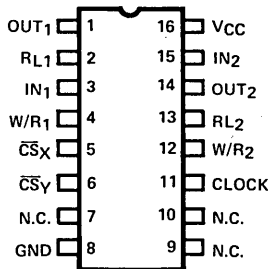
The SY2401 is a 2048-bit dynamic recirculating shift register. It is directly TTL compatible in all respects: inputs, outputs, clock and a single +5V power supply. Write/recirculate controls are provided to eliminate the need for external logic elements when recirculating data.

Two Chip Select inputs have been provided to allow easy selection of an individual package when outputs of several devices have been "OR-tied." A separate

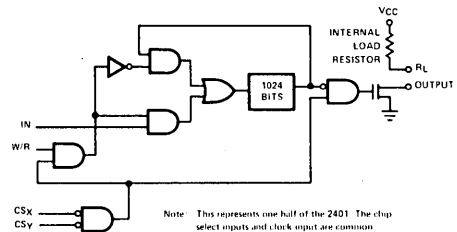
internal "pull-up" resistor (R_L) is provided which can be externally connected to the output pin to achieve full signal swing.

This shift register is fabricated with ion-implanted N-channel silicon gate technology. This technology provides the designer with high performance, easy to use MOS circuits. Only a single +5V Power supply is needed and all devices are directly TTL compatible, including clocks.

PIN CONFIGURATION



LOGIC DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Clock Frequency	Temperature Range
SYP2401	Plastic DIP	1 MHz	0°C to 70°C
SYC2401	Ceramic DIP	1 MHz	0°C to 70°C
SYP2401-1	Plastic DIP	2.5 MHz	0°C to 70°C
SYC2401-1	Ceramic DIP	2.5 MHz	0°C to 70°C

PIN NAMES

IN	Data Input	OUT	Data Output
W/R	Write/Recirculate Control	R_L	Internal Load Resistor
$\overline{CS}_X, \overline{CS}_Y$	Chip Select Input	N.C.	No Connection

TRUTH TABLE

FUNCTION	PIN SYMBOL		
	W/R	\overline{CS}_X	\overline{CS}_Y
WRITE MODE	H	L	L
RECIRCULATE	L	X	X
	X	H	X
	X	X	H
READ MODE	X	L	L

H = Logic High Level L = Logic Low Level

X = Don't Care Condition

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to 150°C
Power Dissipation	1W
Voltage on Any Pin with Respect to Ground	-0.5V to +7V

***COMMENT:**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

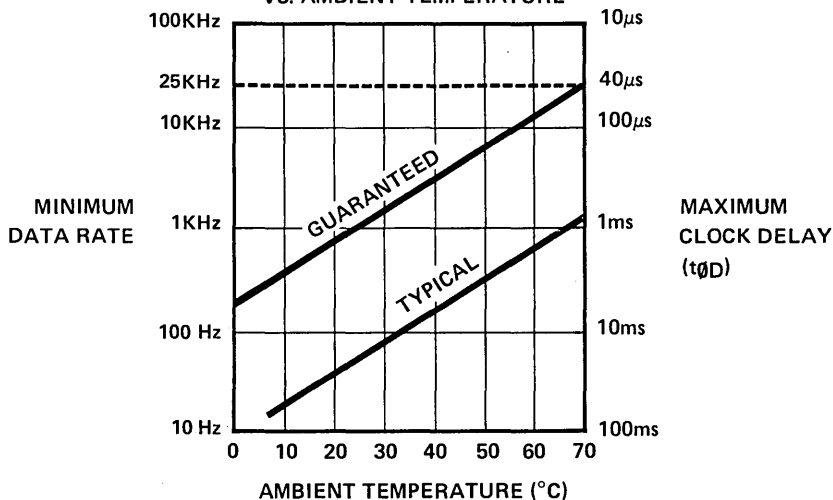
$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	SY2401		SY2401-1	Unit	Test Conditions
		Min.	Typ.(1)	Max.		
I _{LI}	Input Leakage			10	μA	$V_{IN} = 5.25V$ $V_{OUT} = 5.25V$ $T_A = 25^\circ\text{C}$ } $V_{CC} = 5.25V$; $T_A = 0^\circ\text{C}$ } 80% Duty Cycle
I _{LO}	Output Leakage			100	μA	
I _{CC}	Power Supply Current			70	mA	
V _{IH}	Input High Level Voltage (All Inputs)	2.2		5.25	V	$V_{OL} = 0.45V$ $I_{OH} = -1\text{mA}$, R_L Connected $I_{OL} = 1.6\text{mA}$, R_L Connected
V _{IL}	Input Low Level Voltage (All Inputs)	-0.3		0.65	V	
I _{OL}	Output Low Sink Current	6.3	10		mA	
V _{OH}	Output High Level Voltage	2.4		V_{CC}	V	
V _{OL}	Output Low Level Voltage	0		0.45	V	
R _L	Internal Load	0.8	1.3	2.2	$K\Omega$	

NOTE: (1) Typical values are at 25°C and at nominal voltage.

A.C. CHARACTERISTICS

**MINIMUM DATA RATE AND MAXIMUM CLOCK DELAY
VS. AMBIENT TEMPERATURE**





A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

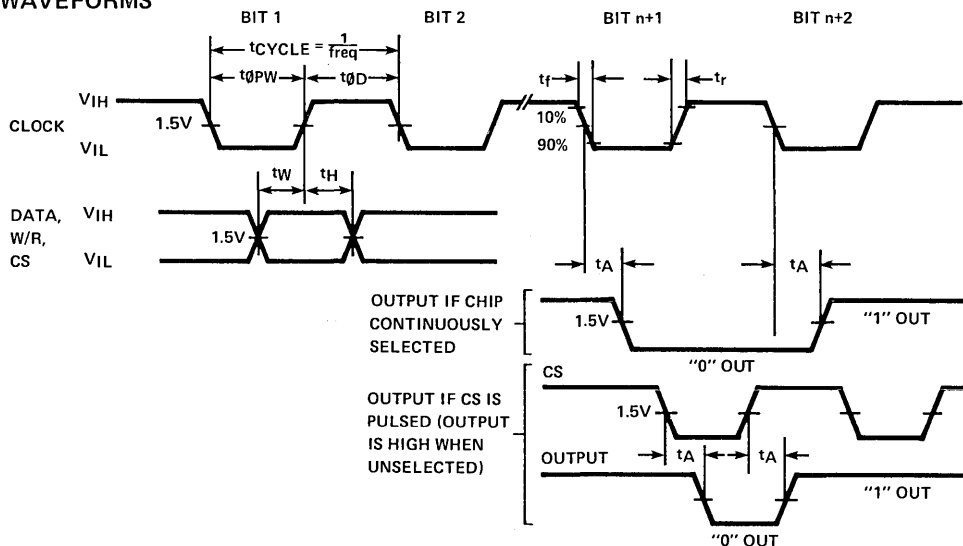
Symbol	Parameter	SY2401		SY2401-1		Units	Test Conditions
		Min	Max	Min	Max		
Freq. Max.	Max. Data Rep. Rate		1		2.5	MHz	T _A = 25°C
Freq. Min.	Min. Data Rep. Rate	1		1		KHz	
		25		25		KHz	T _A = 70°C
t _{φpw}	Clock Pulse Width	0.80	10	0.32	10	μs	T _A = 25°C
t _{φD}	Clock Pulse Delay	0.20	1000	0.08	1000	μs	
		0.20	40	0.08	40	μs	T _A = 70°C
t _r , t _f	Clock Rise and Fall Time		50		50	ns	
t _W	Write Time	200		80		ns	
t _H	Hold Time	150		60		ns	
t _A	Access Time From Clock or Chip Select		500		230	ns	R _L Connected, C _L = 100pF One TTL Load

CAPACITANCE

T_A = 25°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
C _{IN}	Data, W/R & CS Input Capacitance		4	7	pF	All Pins at AC Ground; 250 mV Peak to Peak, 1 MHz
C _{OUT}	Output Capacitance		10	14	pF	
C _φ	Clock Capacitance		4	7	pF	

WAVEFORMS



SHIFT
REGISTERS



1024 Bit Static Shift Registers

SY2533 SY2833/A/B/C

MEMORY PRODUCTS

SHIFT
REGISTERS

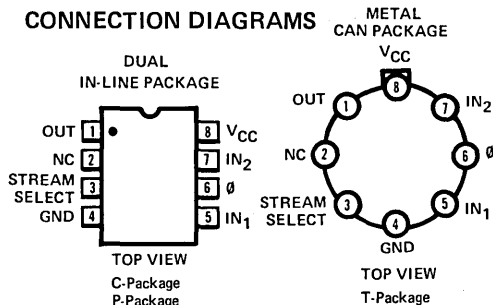
- Single +5V Power Supply
- High Speed Operation – 5.0 MHz
- Totally TTL compatible – inputs, output, clock
- Military temperature range operation
- 400 mvolt noise immunity
- Replaces AMD 2833 Series and Signetics 2533

The SY2533/SY2833 Series of Static Shift Registers, organized 1024x1, are completely TTL compatible and capable of high speed operation. Only a single +5V power supply is needed, and all inputs, clock and outputs operate at TTL voltage levels. On chip logic is provided to accept input data from either of two inputs, allowing simple external system recirculate operation. Data is entered into the register on the positive to negative transition of the clock pulse, and 1023 clock cycles later, is available at the output, a delay time after the positive to negative transition of

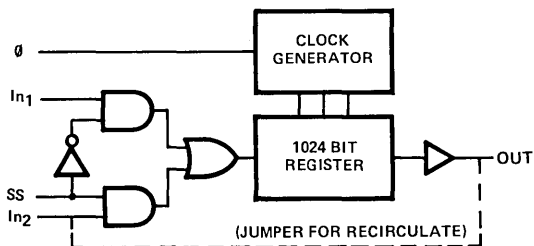
the clock pulse. Since all internal storage is implemented with static, DC logic, the clock input may be held indefinitely at a logic "0" state without loss of data.

The SY2533/SY2833 Static Shift Registers, manufactured with Synertek's ion-implanted silicon gate N-channel MOS technology, are totally compatible, plug in replacements for AMD's 2833 Series as well as Signetics 2533. These devices are intended for serial data storage in systems where single power supply, high speed operation and low system cost are important design parameters.

CONNECTION DIAGRAMS



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Clock Frequency	Temperature Range
SYP2533	Plastic Dip	1.5 MHz	0°C to +70°C
SYT2533	TO-Can	1.5 MHz	0°C to +70°C
SYC2533	Ceramic Dip	1.5 MHz	0°C to +70°C
SYP2833	Plastic Dip	2 MHz	0°C to +70°C
SYT2833	TO-Can	2 MHz	0°C to +70°C
SYC2833	Ceramic Dip	2 MHz	0°C to +70°C
SYP2833A	Plastic Dip	3 MHz	0°C to +70°C
SYT2833A	TO-Can	3 MHz	0°C to +70°C
SYC2833A	Ceramic Dip	3 MHz	0°C to +70°C
SYP2833B	Plastic Dip	4 MHz	0°C to +70°C
SYT2833B	TO-Can	4 MHz	0°C to +70°C
SYC2833B	Ceramic Dip	4 MHz	0°C to +70°C
SYP2833C	Plastic Dip	5 MHz	0°C to +70°C
SYT2833C	TO-Can	5 MHz	0°C to +70°C
SYC2833C	Ceramic Dip	5 MHz	0°C to +70°C
SYMC2833	Ceramic Dip	2 MHz	-55°C to +125°C

TRUTH TABLE

STREAM SELECT	FUNCTION
0	IN 1
1	IN 2

NOTE: "0" = 0V, "1" = +5V

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (SY2533, 2833, 2833A, 2833B, 2833C), -55°C to $+125^\circ\text{C}$ (SYM2833)

$V_{CC} = +5V \pm 5\%$

Parameters	Description	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	$V_{CC} = \text{MIN}, I_{OH} = -100 \mu\text{A}$
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	$V_{CC} = \text{MIN}, I_{OL} = 1.6 \text{ mA}$
V_{IH}	Input HIGH Level	2.0		$V_{CC}+0.3$	Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level	-0.3		0.8	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current			10	μA	$V_{CC} = \text{MAX}, V_{IN} = 0V, T_A = 25^\circ\text{C}$
I_{CC}	V_{CC} Power Supply Current (Note 1)		16	30	mA	f = 1.5 MHz SY2533
			16	35/42		f = 2.0 MHz SY2833/SYM2833
			20	40		f = 3.0 MHz SY2833A
I_{CC}	V_{CC} Power Supply Current (Note 1)		40	60	mA	f = 4.0 MHz SY2833B
			50	75		f = 5.0 MHz SY2833C

Note 1: Power supply currents are with outputs open.

A.C. CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (SY2533, 2833, 2833A), -55°C to $+125^\circ\text{C}$ (SYM2833)

$V_{CC} = +5V \pm 5\%$

Parameters	Description	SY2533			SY2833/SYM2833			SY2833A			Units	Test Conditions
		Min	Typ ¹	Max	Min	Typ ¹	Max	Min	Typ ¹	Max		
f_{max}	Maximum Clock Frequency	1.5	2.0		2.0	3.0		3.0	3.5		MHz	
$t_{\phi\text{pwL}}$	Clock LOW Time	0.250		∞	0.200		∞	0.170		∞	μs	
$t_{\phi\text{pwH}}$	Clock HIGH Time	0.350		100	0.250		100	0.165		100	μs	
t_r, t_f	Clock Rise and Fall Times			1			1			1	μs	
$t_s (I)$	Setup Time, I_0 or I_1 Input			50			50			50	ns	$t_r = t_f \leq 25\text{ns}$
$t_h (I)$	Hold Time, I_0 or I_1 Input			50			50			50	ns	
$t_s (S)$	Setup Time, S Input			80			80			80	ns	
$t_h (S)$	Hold Time, S Input			50			50			50	ns	
t_{pd}	Delay, Clock to Output LOW or HIGH			300			300			200	ns	
$t_{\text{pr}}, t_{\text{pf}}$	Output Rise and Fall Times			150			150			150	ns	10% to 90%
C_{in}	Capacitance, Any Input ²		3	5		3	5		3	5	pF	f = 1 MHz

Note 1: Typical limits are at $V_{CC} = 5.0V$, and $T_A = 25^\circ\text{C}$

Note 2: This parameter is periodically sampled but not 100% tested. It is guaranteed by design.



A.C. CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

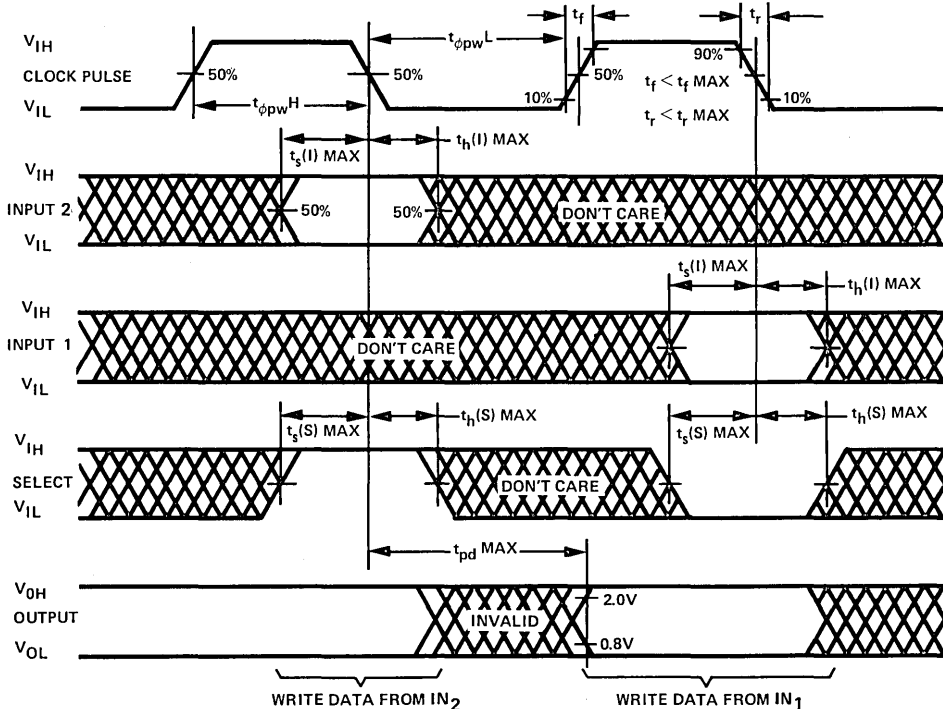
$V_{CC} = +5V \pm 5\%$

Parameters	Description	SY2833B			SY2833C			Units	Test Conditions
		Min	Typ ¹	Max	Min	Typ ¹	Max		
f_{max}	Maximum Clock Frequency	4.0	5.0		5.0	6.0		MHz	
$t_{\phi pwL}$	Clock LOW Time	0.125		∞	0.100		∞	μs	
$t_{\phi pwH}$	Clock HIGH Time	0.125		100	0.100		100	μs	
t_r, t_f	Clock Rise and Fall Times			1			1	μs	
$t_s(I)$	Setup Time, I_0 or I_1 Input			30			30	ns	$t_r = t_f \leq 25\text{ns}$
$t_h(I)$	Hold Time, I_0 or I_1 Input			50			50	ns	
$t_s(S)$	Setup Time, S Input			50			50	ns	
$t_h(S)$	Hold Time, S Input			50			50	ns	
t_{pd}	Delay, Clock to Output LOW or HIGH			150			110	ns	$R_L = 2.9\text{k}, C_L = 20\text{pf}$
t_{pr}, t_{pf}	Output Rise and Fall Times			150			150	ns	10% to 90%
C_{in}	Capacitance, Any Input ²		3	5		3	5	pF	$f = 1\text{ MHz}$

Note 1: Typical limits are at $V_{CC} = 5.0V$, and $T_A = 25^\circ\text{C}$.

Note 2: This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

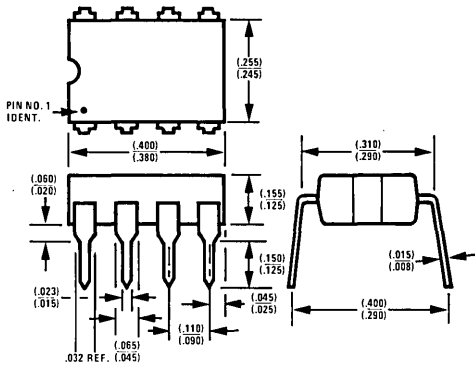
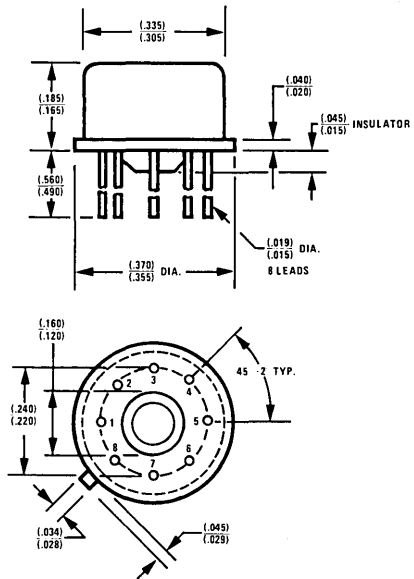
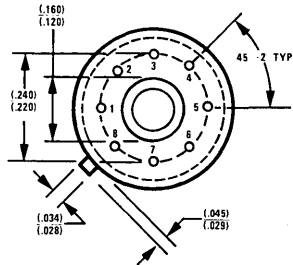
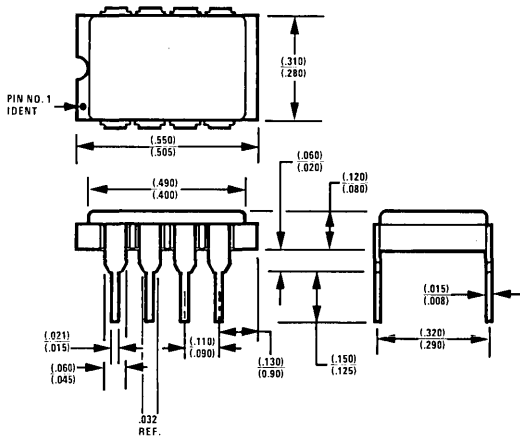
TIMING DIAGRAM



DEFINITION OF TERMS

Static Shift Register. A shift register capable of maintaining stored data without continuously being clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

Setup and Hold Times. The shift register will accept the data present on its input around the time the clock goes from HIGH to LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The setup and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum setup time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

PHYSICAL DIMENSIONS
8 Lead Plastic Dip

8 Lead TO-Can

8 Lead Ceramic Dip




512 Bit and 480 Bit Dual Static Shift Registers

SY2534, SY2535

MEMORY PRODUCTS

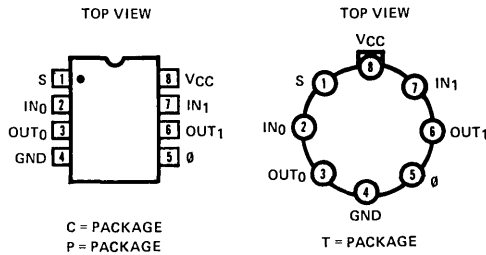
SHIFT
REGISTERS

- +5 Volts Only—No Negative Power Supplies
- Reduce System Cost—Eliminate One Power Supply
- Available to 3.0 MHz
- Double Density Replacement For Signetics 2527/2529
- All Inputs, Outputs and Clocks TTL Compatible

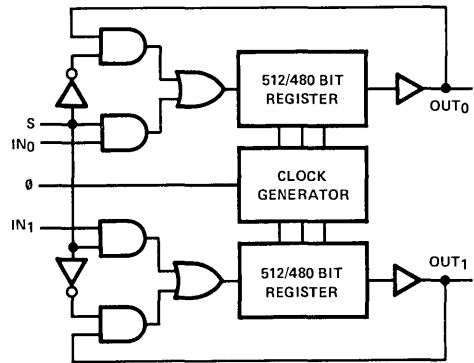
These dual 512-bit and 480-bit static shift registers employ Synertek's ion-implanted silicon gate technology to achieve full TTL compatibility. All inputs and outputs are TTL levels and the only supply necessary is +5 volts. For applications requiring

dynamic storage, these same compatibility features are available on the 2048-bit SY2401. Pinouts are essentially the same as Signetics' 2527/2529, allowing the user to reduce package count by a factor of two with the double density SY2534/SY2535.

CONNECTION DIAGRAMS



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Register Length	Clock Frequency	Temperature Range
SYP2534	Plastic DIP	512	1.5MHz	0°C to +70°C
SYT2534	TO Can	512	1.5MHz	0°C to +70°C
SYP2534A	Plastic DIP	512	3.0MHz	0°C to +70°C
SYT2534A	TO Can	512	3.0MHz	0°C to +70°C
SYP2535	Plastic DIP	480	1.5MHz	0°C to +70°C
SYT2535	TO Can	480	1.5MHz	0°C to +70°C
SYP2535A	Plastic DIP	480	3.0MHz	0°C to +70°C
SYT2535A	TO Can	480	3.0MHz	0°C to +70°C

TRUTH TABLE

S	Function
0	Recirculate
1	Write

Note: "0" = OV. "1" = +5V

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	0.6W

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGE: $V_{CC} = +5.0V \pm 5\%$; 0° to $70^\circ C$
ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{MIN}, I_{OH} = -100\mu A$	2.4	3.5		Volts
V_{OL}	Output LOW Voltage	$V_{CC} = \text{MIN}, I_{OL} = 1.6\text{mA}$		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			$V_{CC} + 0.3$	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	-0.3		0.8	Volts
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX}, V_{IN} = 0V,$ $T_A = 25^\circ C$			10	μA
I_{CC}	V_{CC} Power Supply Current (Note 1)	$f = 1.5 \text{ MHz SY2534/2535}$ $f = 3.0 \text{ MHz SY2534A/2535A}$		16	35	mA
				25	45	mA

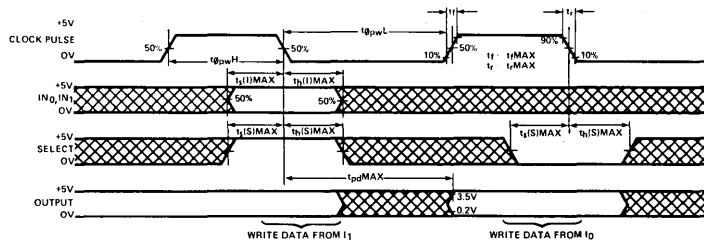
Note 1: Power Supply currents are with inputs and outputs open.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameters	Description	Test Conditions	SY2534, SY2535			SY2534A, SY2535A			Units
			Min	Typ ¹	Max	Min	Typ ¹	Max	
f_{max}	Maximum Clock Frequency		1.5	2.0		3.0	3.5		MHz
$t_{\phi\text{pwL}}$	Clock LOW Time		0.250		∞	0.170		∞	μS
$t_{\phi\text{pwH}}$	Clock HIGH Time		0.350		100	0.165		100	μS
t_r, t_f	Clock Rise and Fall Times				1			1	μS
$t_s(I)$	Setup Time I_0 or I_1 Input	$t_r = t_f \leq 25\text{ns}$			50			50	ns
$t_h(I)$	Hold Time I_0 or I_1 Input	$t_r = t_f \leq 25\text{ns}$			50			50	ns
$t_s(S)$	Setup Time, S Input	$t_r = t_f \leq 25\text{ns}$			80			80	ns
$t_h(S)$	Hold Time, S Input	$t_r = t_f \leq 25\text{ns}$			50			50	ns
t_{pd}	Delay Clock to Output LOW or HIGH	$R_L = 2.9K, C_L = 20\text{pF}$			300			200	ns
$t_{\text{pr}}, t_{\text{pf}}$	Output Rise and Fall Times	10% to 90%			150			150	ns
C_{in}	Capacitance, Any Input ²	$f = 1 \text{ MHz}$		3	5		3	5	pF

 Note 1: Typical limits are at $V_{CC} = 5.0V$, and $T_A = 25^\circ C$.

Note 2: This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

TIMING DIAGRAM

DEFINITION OF TERMS

Static Shift Register. A shift register capable of maintaining stored data without continuously being clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

Setup and Hold Times. The shift register will accept the data present on its input around the time the clock goes from HIGH to LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The setup and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum setup time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.



1024-Bit Dynamic Shift Registers

Quad, Dual, Single

SY2802A, SY2803A, SY2804A

MEMORY PRODUCTS

SHIFT
REGISTERS

- Synertek ion implanted silicon gate process
- 10 MHz data rate—minimum
- 5 MHz clock rate
- TTL, DTL compatible
- Reduced clock capacitance, 85pF
- Reduced power dissipation, 80 μ W/bit at 1.0 MHz

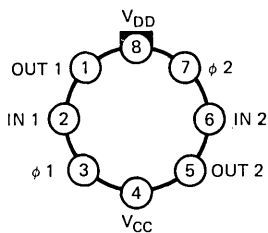
The SY2802A, 2803A and 2804A 2 ϕ dynamic shift registers utilize I/O multiplexing techniques to attain a 10 MHz data rate with a clock rate of only 5 MHz. The inputs and outputs are bipolar and MOS compatible for ease of implementation in a TTL, DTL and a high- or low-threshold MOS system.

silicon gate design. These savings directly affect the cost of the overhead circuitry (clock drivers, power supplies) for a shift register memory system.

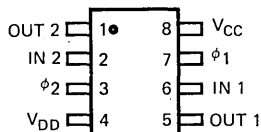
Clock power and V_{DD} current have been significantly reduced due to the advantages inherent in an ion implanted silicon gate design over a conventional

The SY2802A, 2803A and 2804A are used effectively in applications requiring low cost serial memory such as CRT refresh, line and page storage for facsimile transmitters and receivers, and character storage for high speed printers.

PIN CONFIGURATION

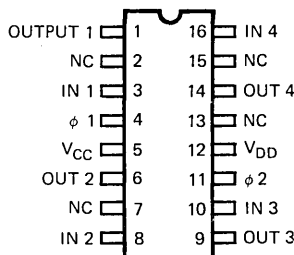


SYM2803A



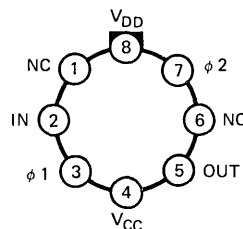
SYP2803A

PIN CONFIGURATION

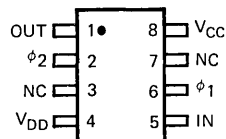


SYP2802A
SYC2802A

PIN CONFIGURATION



SYM2804A



SYP2804A

ORDERING INFORMATION

Order Number	Package Type	Organization	Temperature Range
SYP2804A	Plastic Dip	1024 x 1	0°C to +70°C
SYM2804A	TO Can	1024 x 1	0°C to +70°C
SYP2803A	Plastic Dip	512 x 2	0°C to +70°C
SYM2803A	TO Can	512 x 2	0°C to +70°C
SYP2802A	Plastic Dip	256 x 4	0°C to +70°C
SYC2802A	Ceramic Dip	256 x 4	0°C to +70°C

SHIFT
REGISTERS**ABSOLUTE MAXIMUM RATINGS**¹

Temperature Under Bias	0°C to 70°C	Data and Clock Input Voltages	
Storage Temperature	-65°C to +160°C	and Supply Voltages with	
Power Dissipation ⁽²⁾	1 Watt	respect to V _{CC}	+0.5V to -20V

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specifiedV_{DD} = -5V ±5%

Symbol	Test	Min.	Typ. ⁽³⁾	Max.	Unit	Conditions
I _{LI}	Input Load Current		< 10	500	nA	T _A = 25°C
I _{LO}	Output Leakage Current		< 10	1000	nA	V _{OUT} = 0.0V, T _A = 25°C
I _{LC}	Clock Leakage Current		10	1000	nA	Max. V _{ILC} , T _A = 25°C
V _{IL}	Input "Low" Voltage	V _{CC} -10		V _{CC} -4.2	V	
V _{IH}	Input "High" Voltage	V _{CC} -2		V _{CC} +3	V	

V_{DD} = -5V ±5%

I _{DD1}	Power Supply Current		35	40	mA	T _A = 25°C	Output at Logic "0", 10 MHz Data Rate, 40% Duty Cycle, Continuous Operation, V _{ILC} = V _{CC} - 17V
I _{DD2}	Power Supply Current			45	mA	T _C = 0°C	
V _{ILC}	Clock Input Low Voltage	V _{CC} -17		V _{CC} -15	V		
V _{IHC}	Clock Input High Voltage	V _{CC} -1		V _{CC} +3	V		
V _{OL}	Output Low Voltage		-3	0.5	V	R _{L1} = 3K to V _{DD} , I _{OL} = 1.6 mA	
V _{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R _{L1} = 3K to V _{DD} , I _{OH} = -100μA	
V _{OH2}	Output High Voltage Driving MOS	V _{CC} -1.6	V _{CC} -1		V	R _{L2} = 4.7K to V _{DD} (See p. 4 for connection)	

A.C. CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = +5V ±5%

Symbol	Test	V _{DD} = -5V ±5%		Unit
Frequency	Clock Rep Rate		5.0	MHz
Frequency	Data Rep Rate	Note 1	10.0	MHz
t _{φPW}	Clock Pulse Width	.07	10	μsec
t _{φD}	Clock Pulse Delay	10	Note 1	nsec
t _R , t _F	Clock Pulse Transition		1000	nsec
t _{DW}	Data Write Time (Set Up)		30	nsec
t _{DH}	Data To Clock Hold Time		20	nsec
t _{A+} , t _{A-}	Clock To Data Out Delay		90	nsec

Note 1: Stresses listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The 1 watt dissipation is not to be construed as an operating rating (see note 1). For operating at elevated temperatures the device must be derated based as shown on page 4. When operating at V_{DD} = -5V ±5% the maximum duty cycle is 40%. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = [t_{φPW} + 1/2 (t_R + t_F)] × clock rate.

Note 3: Typical values are at T_A = 25°C and at nominal voltages.



CAPACITANCE ² $V_{CC} = +5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$, $T_A = 25^\circ C$

Symbol	Test	Typ.	Max.	Conditions
C_{IN}	Input Capacitance	5 pF	10 pF	} $f = 1 \text{ MHz}$ $V_{IN} = V_{CC}$ $V_{OUT} = V_{CC}$ $V_\phi = V_{CC}$
C_{OUT}	Output Capacitance	5 pF	10 pF	
C_ϕ	Clock Capacitance	70 pF	85 pF	
$C_{\phi1\phi2}$	Clock to Clock Capacitance	11 pF	16 pF	

Note 1: See page 4 for guaranteed curve.

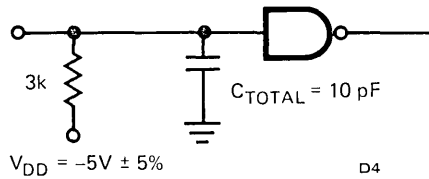
Note 2: This parameter is periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

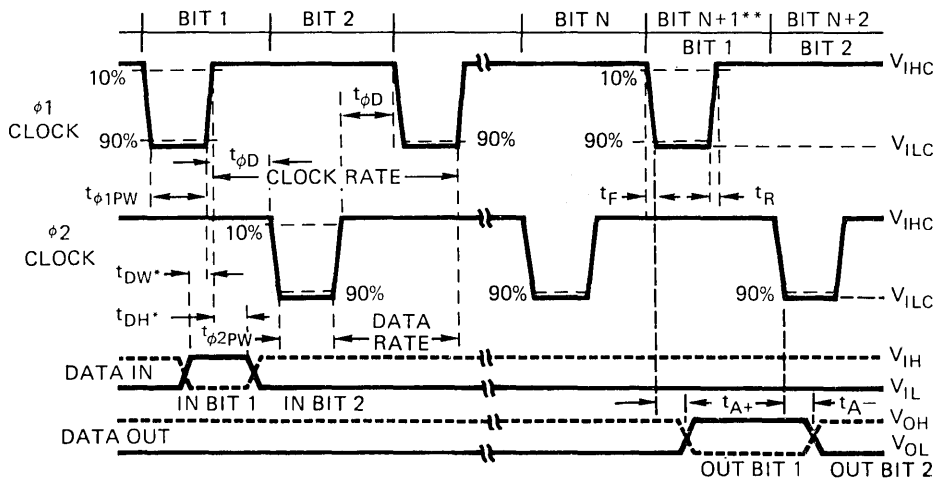
Conditions of Test

Input rise and fall times: 10 nsec

Output Load is 1 TTL gate



Timing Diagram



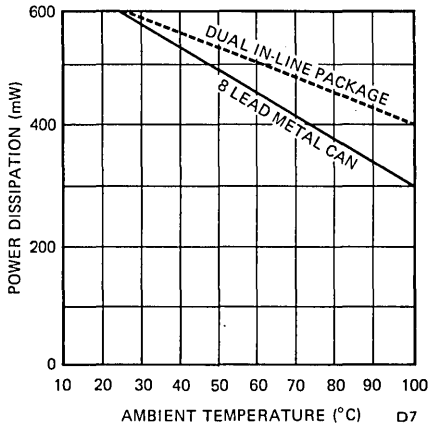
* t_{DW} and t_{DH} same for $t_{\phi2}$

** $N = 256$ for SY2802A, $N = 512$ for SY2803A, $N = 1024$ for SY2804A

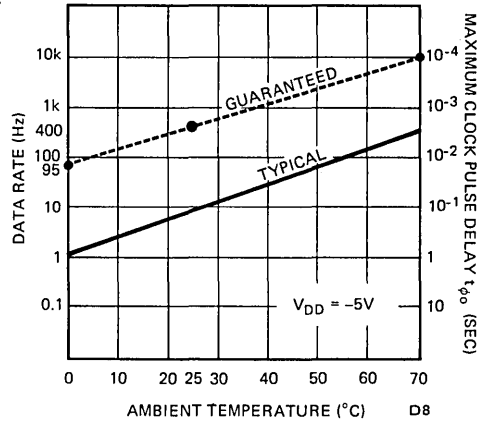
D6



TYPICAL CHARACTERISTICS

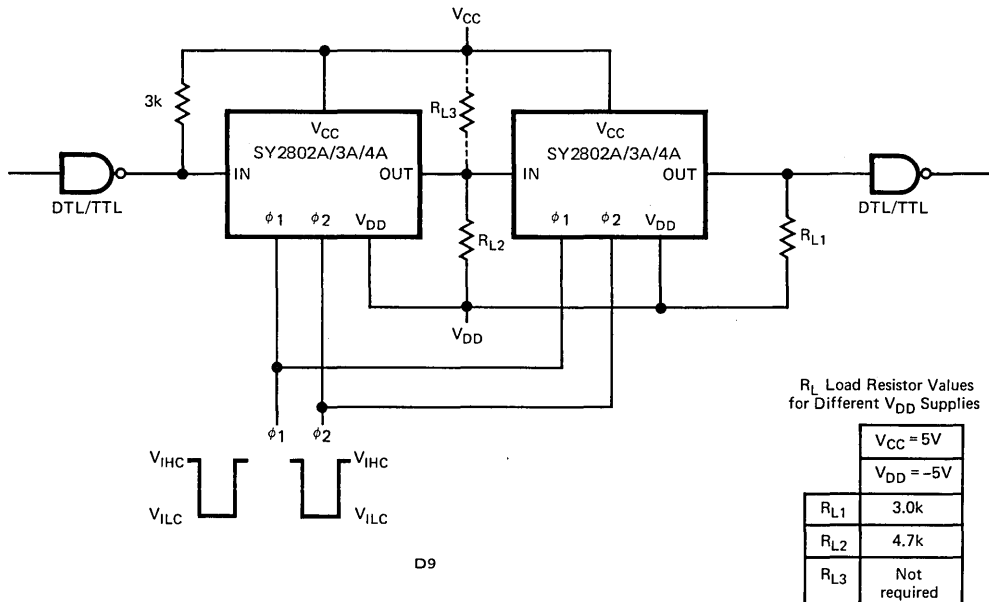


**MAXIMUM ALLOWABLE
POWER DISSIPATION**



**MINIMUM OPERATING DATA RATE
OR MAXIMUM CLOCK PULSE DELAY
VS. TEMPERATURE**

DTL/TTL MOS Interfaces





2048-Bit Dynamic Shift Registers

**SY2825A,
SY2826/7**

**MEMORY
PRODUCTS**

SHIFT
REGISTERS

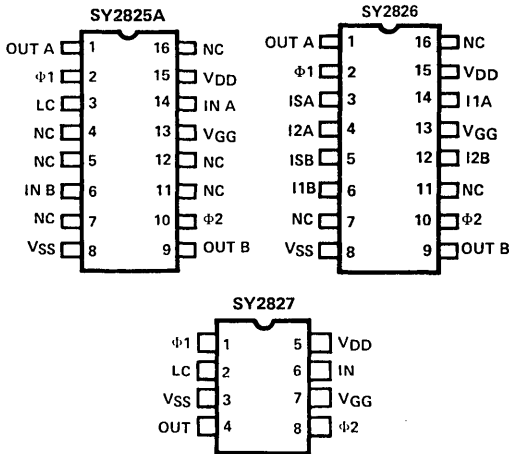
- 6 MHz Data Rate

- Recirculate Gates On Chip

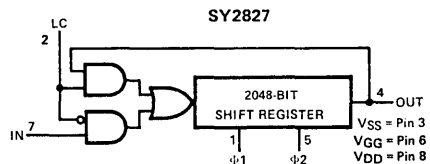
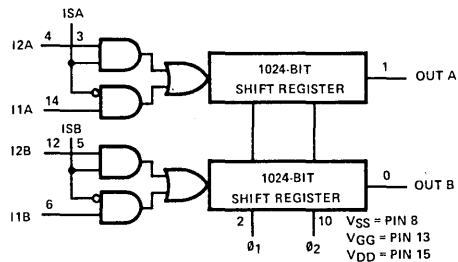
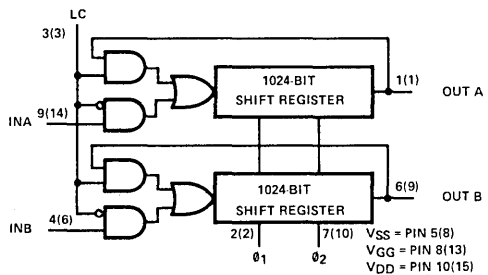
The SY2825/26/27 are 2048-bit dynamic shift registers designed with Synertek's ion-implanted silicon gate technology. The 2825 is a dual 1024-bit device with on-chip recirculate and a load control (LC) common to both registers. When LC is HIGH, the two registers recirculate data; when LC is LOW new data is entered through the data inputs. The SY2826 is similar, but each register has two data inputs selected by separate input select (IS) signals. The SY2827 is

a single 2048-bit register with on-chip recirculate and a load control. All the devices can drive one standard TTL load. The select, load command, and data inputs may be driven by TTL signals. Two high-voltage clock signals, $\phi 1$ and $\phi 2$, are required. Internally, each shift register consists of two multiplexed registers so that a data shift occurs on each $\phi 1$ or $\phi 2$ clock pulse. The data rate, therefore is double the frequency of either clock signal.

CONNECTION DIAGRAMS



BLOCK DIAGRAMS



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SYP2825A	Plastic DIP	0°C to 70°C
SYC2825A	Ceramic DIP	0°C to 70°C
SYP2826	Plastic DIP	0°C to 70°C
SYC2826	Ceramic DIP	0°C to 70°C
SYP2827	Plastic DIP	0°C to 70°C
SYC2827	Ceramic DIP	0°C to 70°C



ABSOLUTE MAXIMUM RATINGS*

Storage Temperature -65°C to +150°C
Temperature (Ambient)
Under Bias 0°C to +70°C
DC Input Voltage
with Respect to V_{SS} -20V to +0.3V

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

OPERATING RANGE

V_{SS} = +5.0V ±5%, V_{GG} = -10.0V to -11.0V, T_A = 0°C to +70°C.

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V _{OH}	Output High Voltage	I _{OH} = -0.5mA		2.4		V _{SS}	Volts
V _{OL}	Output Low Voltage	I _{OL} = 1.6mA		0.0		0.4	Volts
V _{IH}	Input High Level	Guaranteed input logical High Voltage for all inputs except clocks		V _{SS} -1.0		V _{SS} +0.3	Volts
V _{IL}	Input Low Level	Guaranteed input logical Low Voltage for all inputs except clocks		V _{SS} -10		V _{SS} -4.2	Volts
I _I	Input Leakage Current	V _{IN} = -10V, T _A = 25°C			10	500	nA
I _φ	Clock Input Leakage Current	V _φ = -15V, T _A = 25°C			50	1000	nA
V _{φH}	Clock High Level			V _{SS} -1.0		V _{SS} +0.3	Volts
V _{φL}	Clock Low Level			V _{GG} -0.3		V _{GG} +0.8	Volts
I _{GG}	V _{GG} Current	T _A = 25°C V _{SS} = 5.25V V _{GG} = -11.0V	.01MHz < f _φ < 0.1MHz		2.5	5	
			f _φ = 1.0MHz		2.5	5	mA
			f _φ = 3.0MHz		2.5	5	
I _{DD}	V _{DD} Current	V _{φL} = -11.0V t _{φpw} = 115ns Data = 11110000...	.01MHz < f _φ < 0.1MHz		3	4	
			f _φ = 1.0MHz		15	20	mA
			f _φ = 3.0MHz		30	40	

Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = -10.5V and 25°C ambient.

SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS OVER OPERATING RANGE

Parameters	Definition	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
f _D	Data Rate (Note 2)		0.02		6.0	MHz
f _φ	Clock Frequency		0.01		3.0	MHz
t _{φd}	Delay Between Clocks (Note 3)		10			ns
t _{φpw}	Clock Low Time	t _{φt} = 20ns	0.115		10	μs
t _{φt}	Clock Rise and Fall Times	10% to 90%			0.5	μs
t _s	Set-Up Time, Data and Select Inputs (See Definitions)				40	ns
t _h	Hold Time, Data and Select Inputs (See Definitions)				20	ns
t _{pd}	Delay, Clock to Data Out	C _L = 15pF			80	ns
C(D)	Capacitance, Data Input				5	pF
C(S)	Capacitance, Select Input or L _C	f = 1 MHz, V _{IN} = 0V			7	pF
C(φ)	Capacitance, Clock Input	All other pins at GND		80	110	pF

Note: 2. The Data Rate is twice the frequency of either clock phase.

DEFINITION OF TERMS

Dynamic Shift Register A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

ϕ_1, ϕ_2 The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at V_{SS} . Data is accepted into the master of each bit during one phase and is transferred to the slave of each bit during the other phase.

$t_{\phi d}$ Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-to-LOW transition of the other clock input. During $t_{\phi d}$ both clocks are HIGH and all data is stored on capacitive nodes.

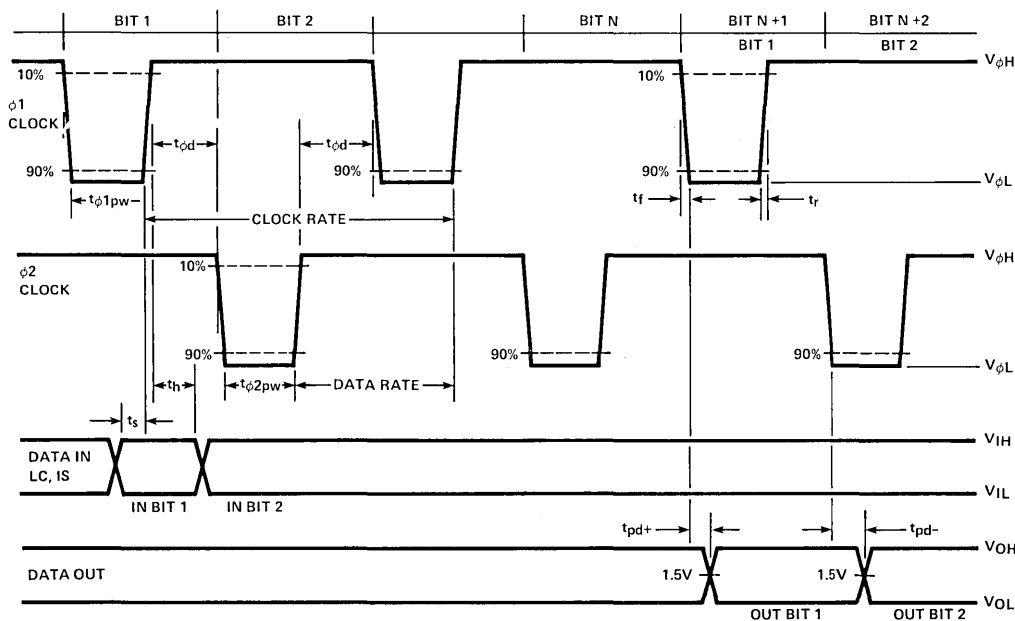
$t_{\phi pw}$ Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and the data transfer between master and slave or slave and master occurs.

$t_{\Phi t}$ Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occurring.

$t_s(D)$ Data set-up time. The time prior to the LOW-to-HIGH transition of Φ during which the data on the data input must be steady to be correctly written into the memory.

$t_h(D)$ Data hold time. The time following the LOW-to-HIGH transition of Φ during which the data must be steady. To correctly write data into the register, the data must be applied by $t_s(D)$ before this transition and must not be changed until $t_h(D)$ after this transition.

t_{pd} The delay from a HIGH-to-LOW clock transition to correct data present at the register output.

SWITCHING WAVEFORMS


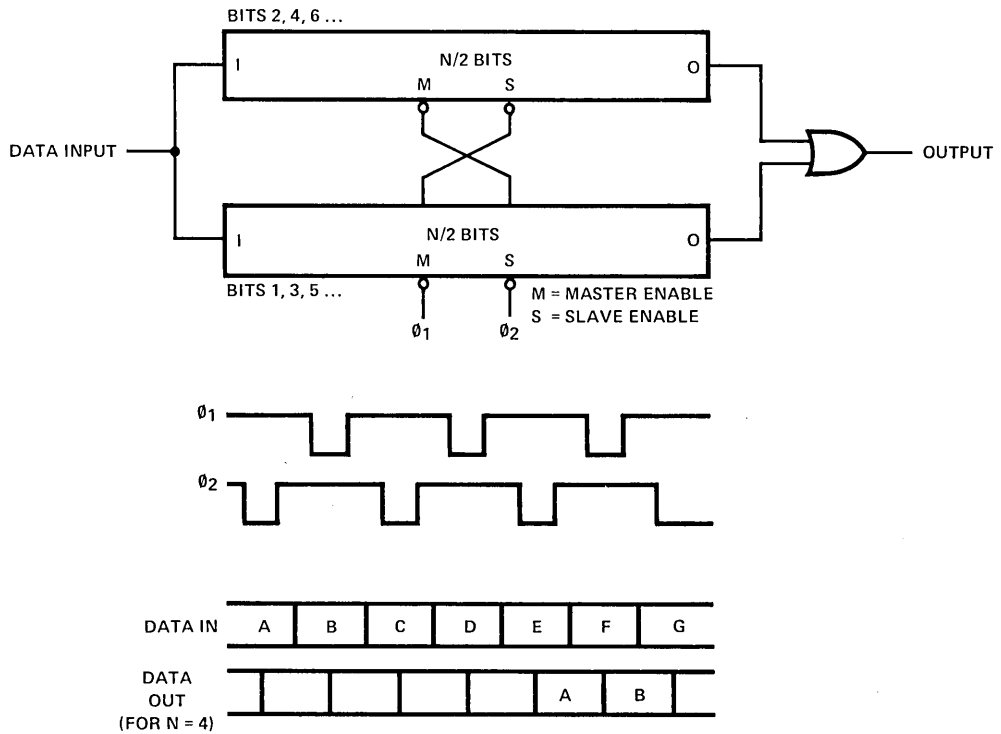
Clock Rise Time 20ns
 Clock Fall Time 20ns
 Output Load 1 TTL Load

TRUTH TABLES
SY2825A and 2827

LC	IN	OUT	DATA ENTERED
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

SY2826

IS	INPUT1	INPUT2	DATA ENTERED
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

FUNCTIONAL EQUIVALENT OF EACH REGISTER


Since the two registers shift on opposite clock pulses, a new data bit is entered on both ϕ_1 and ϕ_2 . Data entering the register on ϕ_1 will appear at the output on ϕ_1 (from the negative edge of ϕ_1 to the negative edge of ϕ_2).

Random Access Memories

Random Access Memories



256 x 4 Static Random Access Memory

SY2101

MEMORY PRODUCTS

RAMS

- 256x4 Organization to Meet Needs For Small System Memories
- Access Time — 250/350/450/500/ns
- Single +5V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required
- Simple Memory Expansion — Two Chip Enable Inputs
- Inputs Protected — All Inputs Have Protection Against Static Charge
- Low Cost Packaging — 22 Pin Plastic Dual-In-Line Configuration
- Low Power — Typically 150 mW
- Three-State Output — OR-Tie Capability
- Output Disable Provided For Ease of Use in Common Data Bus Systems

The SY2101 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The SY2101 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

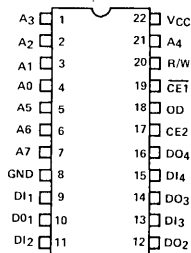
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two Chip Enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided

so that data inputs and outputs can be tied for common I/O systems. Output disable is then used to eliminate any bi-directional logic.

The SY2101 is fabricated with N-channel ion implanted silicon gate technology. This technology allows the design and production of high-performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's ion implanted silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

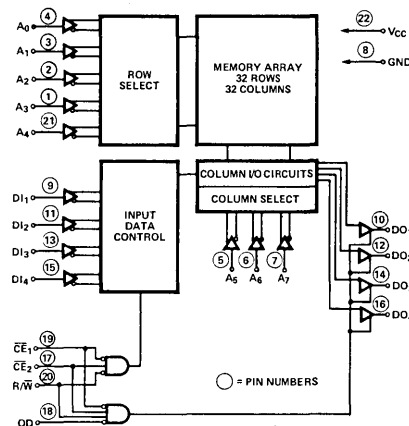
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP2101-1	Plastic DIP	500 ns	0°C to 70°C
SYC2101-1	Ceramic DIP	500 ns	0°C to 70°C
SYP2101A-2	Plastic DIP	250 ns	0°C to 70°C
SYC2101A-2	Ceramic DIP	250 ns	0°C to 70°C
SYP2101A	Plastic DIP	350 ns	0°C to 70°C
SYC2101A	Ceramic DIP	350 ns	0°C to 70°C
SYP2101A-4	Plastic DIP	450 ns	0°C to 70°C
SYC2101A-4	Ceramic DIP	450 ns	0°C to 70°C

BLOCK DIAGRAM



DIN	DATA INPUT	OD	OUTPUT DISABLE
A0-A7	ADDRESS INPUTS	DOUT	DATA OUTPUT
R/W	READ/WRITE INPUT	VCC	POWER (+5V)
CE1, CE2	CHIP ENABLE		



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	2101-1			2101A-2 2101A, 2101A-4			Unit	Test Conditions
		Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.		
I _{LI}	Input Current			10			10	μA	V _{IN} = 0 to 5.25V
I _{LOH}	I/O Leakage Current(2)			15			10	μA	C _E = 2.2V, V _{OUT} = 4.0V
I _{LOL}	I/O Leakage Current(2)			-50			-10	μA	C _E = 2.2V, V _{OUT} = 0.45V
I _{CC1}	Power Supply Current		30	60		30	50	mA	V _{IN} = 5.25V, I _O = 0mA T _A = 25°C
I _{CC2}	Power Supply Current			70			55	mA	V _{IN} = 5.25V, I _O = 0mA T _A = 0°C
V _{IL}	Input Low Voltage	-0.5		+0.65	-0.5		+0.8	V	
V _{IH}	Input High Voltage	2.2		V _{CC}	2.0		V _{CC}	V	
V _{OL}	Output Low Voltage			+0.45			+0.4	V	I _{OL} = 3.2mA (I _{OL} = 2.0mA 2101-1)
V _{OH}	Output High Voltage	2.2			2.4			V	I _{OH} = -150μA

NOTE: 1. Typical Values are for T_A = 25°C and nominal supply voltage.
2. Input and Output tied together.

A.C. CHARACTERISTICS – SY2101-1

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t _{RCY}	Read Cycle	500		ns
t _A	Access Time		500	ns
t _{CO}	Chip Enable To Output		350	ns
t _{OD}	Output Disable To Output		300	ns
t _{DF} [1]	Data Output to High Z State	0	150	ns
t _{OH}	Previous Data Read Valid after change of Address	0		ns
WRITE CYCLE				
t _{WCY}	Write Cycle	500		ns
t _{AW}	Write Delay	100		ns
t _{CW}	Chip Enable To Write	400		ns
t _{DW}	Data Setup	280		ns
t _{DH}	Data Hold	100		ns
t _{WP}	Write Pulse	300		ns
t _{WR}	Write Recovery	50		ns



**A.C. CHARACTERISTICS – SY2101A-2**T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t _{RCY}	Read Cycle	250		ns
t _A	Access Time		250	ns
t _{CO}	Chip Enable To Output		180	ns
t _{OD}	Output Disable To Output		130	ns
t _{DF} [1]	Data Output to High Z State	0	180	ns
t _{OH}	Previous Data Read Valid after change of Address	40		ns
WRITE CYCLE				
t _{WCY}	Write Cycle	250		ns
t _{AW}	Write Delay	20		ns
t _{CW}	Chip Enable To Write	150		ns
t _{DW}	Data Setup	150		ns
t _{DH}	Data Hold	0		ns
t _{WP}	Write Pulse	150		ns
t _{WR}	Write Recovery	0		ns
t _{DS}	Output Disable Setup	20		ns

A.C. CHARACTERISTICS – SY2101AT_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t _{RCY}	Read Cycle	350		ns
t _A	Access Time		350	ns
t _{CO}	Chip Enable To Output		240	ns
t _{OD}	Output Disable To Output		180	ns
t _{DF} [1]	Data Output to High Z State	0	150	ns
t _{OH}	Previous Data Read Valid after change of Address	40		ns
WRITE CYCLE				
t _{WCY}	Write Cycle	350		ns
t _{AW}	Write Delay	20		ns
t _{CW}	Chip Enable To Write	200		ns
t _{DW}	Data Setup	200		ns
t _{DH}	Data Hold	0		ns
t _{WP}	Write Pulse	200		ns
t _{WR}	Write Recovery	0		ns
t _{DS}	Output Disable Setup	20		ns

NOTE: 1 t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.



A.C. CHARACTERISTICS – SY2101A-4

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t _{RCY}	Read Cycle	450		ns
t _A	Access Time		450	ns
t _{CO}	Chip Enable To Output		310	ns
t _{OD}	Output Disable To Output		250	ns
t _{DF} ^[1]	Data Output to High Z State	0	200	ns
t _{OH}	Previous Data Read Valid after change of Address	40		ns
WRITE CYCLE				
t _{WCY}	Write Cycle	450		ns
t _{AW}	Write Delay	20		ns
t _{CW}	Chip Enable To Write	250		ns
t _{DW}	Data Setup	250		ns
t _{DH}	Data Hold	0		ns
t _{WP}	Write Pulse	250		ns
t _{WR}	Write Recovery	0		ns
t _{DS}	Output Disable Setup	20		ns

A.C. CONDITIONS OF TEST

2101A-2 2101A 2101A-4

2101-1

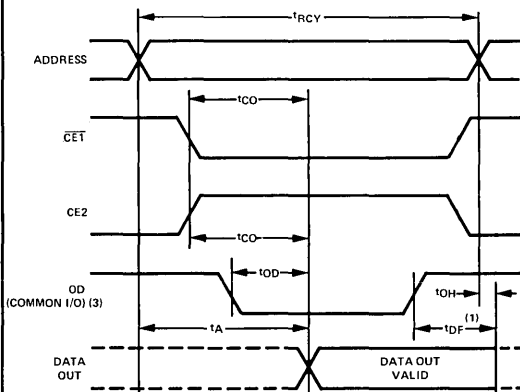
Input Pulse Levels: +0.8V to 2.0V +0.65V to 2.2V
 Input Pulse Rise & Fall Times: 10ns 10ns
 Timing Measurement Reference Level: Inputs: 1.5V 1.5V
 Outputs: 0.8V & 2.0V 0.8V & 2.0V
 Output Load: 1 TTL Gate & C_L = 100pF 1 TTL Gate & C_L = 100pF

CAPACITANCE T_A = 25°C, f = 1MHz

Symbol	Test	Typ.	Max.	Unit
C _{IN}	Input Capacitance (All Input Pins) V _{IN} = 0V	4	8	pF
C _{OUT}	Output Capacitance V _{OUT} = 0V	8	12	pF

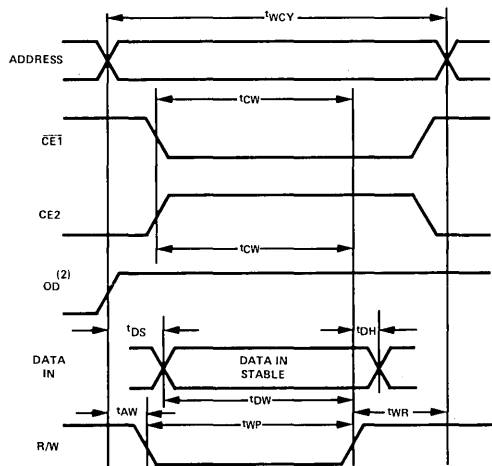
TIMING DIAGRAMS

READ CYCLE



- NOTES:
- t_{DF} is with respect to the trailing edge of CE1, CE2, or OD, whichever occurs first.
 - During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
 - OD should be tied low for separate I/O operation.

WRITE CYCLE



RAMs



256 x 4 Static Random Access Memory

SY21H01

MEMORY PRODUCTS

RAMS

- 256x4 Organization to Meet Needs for Small System Memories
- Access Time – 175/200 ns
- Single +5V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Simple Memory Expansion – Two Chip Enable Inputs
- Inputs Protected – All Inputs Have Protection Against Static Charge
- Low Cost Packaging – 22 Pin Plastic Dual-In-Line Configuration
- Three-State Output – OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

The SY21H01 is a 256-word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The SY21H01 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

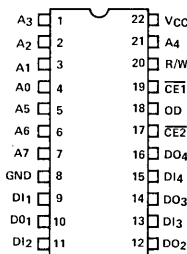
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two Chip Enables allow easy selection of an individual package when

outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. Output disable is then used to eliminate any bi-directional logic.

The SY21H01 is fabricated with N-channel ion implanted silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's ion implanted silicon gate technology also provides excellent protection against contamination. This permits the use of low cost packaging.

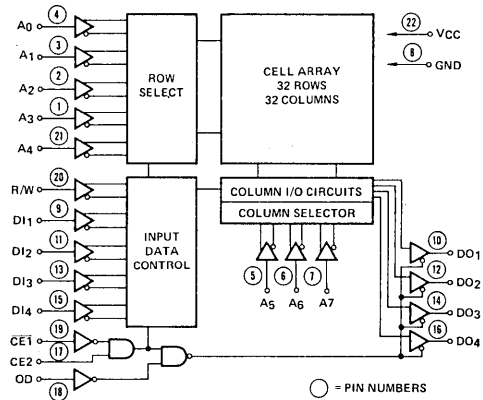
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP21H01	Plastic DIP	175 ns	0°C to 55°C
SYC21H01	Ceramic DIP	175 ns	0°C to 55°C
SYP21H01-2	Plastic DIP	200 ns	0°C to 55°C
SYC21H01-2	Ceramic DIP	200 ns	0°C to 55°C

BLOCK DIAGRAM



PIN NAMES

DIN	DATA INPUT	OD	OUTPUT DISABLE
A0-A7	ADDRESS INPUTS	DOUT	DATA OUTPUT
R/W	READ/WRITE INPUT	VCC	POWER (+5V)
CE1, CE2	CHIP ENABLE		

**ABSOLUTE MAXIMUM RATINGS**

Ambient Temperature Under Bias	0°C to 55°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to $+55^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$ (Unless Otherwise Specified)

Symbol	Parameter	Min	Typ ⁽¹⁾	Max	Units	Test Conditions
I_{LI}	Input Current			10	μA	$V_{IN} = 0$ to $5.25V$
I_{LOH}	I/O Leakage Current [2]			15	μA	$\overline{CE} = 2.2V$, $V_{OUT} = 4.0V$
I_{LOL}	I/O Leakage Current [2]			-50	μA	$\overline{CE} = 2.2V$, $V_{OUT} = 0.45V$
I_{CC1}	Power Supply Current		50	80	mA	$V_{IN} = 5.25V$, $I_O = 0mA$ $T_A = 25^\circ\text{C}$
I_{CC2}	Power Supply Current			90	mA	$V_{IN} = 5.25V$, $I_O = 0mA$ $T_A = 0^\circ\text{C}$
V_{IL}	Input "Low" Voltage	-0.5		+0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.4	V	$I_{OL} = 3.2mA$
V_{OH}	Output "High" Voltage	2.4			V	$I_{OH} = -150\mu\text{A}$

- NOTES: 1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.
2. Input and Output tied together.

A.C. CHARACTERISTICS – SY21H01

$T_A = 0^\circ\text{C}$ to 55°C , $V_{CC} = 5V \pm 5\%$ unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
READ CYCLE					
t_{RCY}	Read Cycle		175		ns
t_A	Access Time			175	ns
t_{CO}	Chip Enable to Output			110	ns
t_{OD}	Output Disable to Output			90	ns
$t_{DF} [1]$	Data Output to High Z State	0		70	ns
t_{OH}	Previous Data Read Valid after change of Address	0			ns
WRITE CYCLE					
t_{WCY}	Write Cycle		175		ns
t_{AW}	Write Delay	0			ns
t_{CW}	Chip Enable to Write		100		ns
t_{DW}	Data Setup		100		ns
t_{DH}	Data Hold		0		ns
t_{WP}	Write Pulse		150		ns
t_{WR}	Write Recovery		0		ns

- NOTES: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, $CE2$, or OD , whichever occurs first.

A.C. CHARACTERISTICS – SY21H01-2

$T_A = 0^\circ\text{C}$ to $+55^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
READ CYCLE					
t_{RCY}	Read Cycle	200			ns
t_A	Access Time			200	ns
t_{CO}	Chip Enable to Output			120	ns
t_{OD}	Output Disable to Output			100	ns
$t_{DF(1)}$	Data Output to High Z State	0		80	ns
t_{OH}	Previous Data Read Valid after change of Address	0			ns
WRITE CYCLE					
t_{WCY}	Write Cycle	200			ns
t_{AW}	Write Delay	0			ns
t_{CW}	Chip Enable to Write	120			ns
t_{DW}	Data Setup	120			ns
t_{DH}	Data Hold	0			ns
t_{WP}	Write Pulse	170			ns
t_{WR}	Write Recovery	0			ns

NOTE: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, $CE2$, or OD , whichever occurs first.

A.C. CONDITIONS OF TEST

Input Pulse Levels: +0.8V to 2.0V

Input Pulse Rise & Fall Times: 10 ns

Timing Measurement Input: 1.5V

Reference Level Output: 0.8V & 2.0V

Output Load: 1 TTL Gate & $C_L = 100$ pF

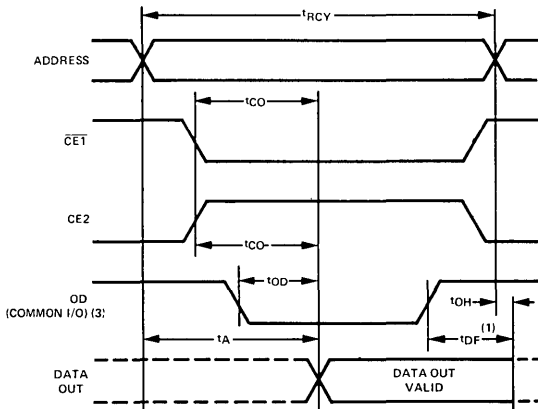
CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$

Symbol	Test	Typ	Max	Units
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0\text{V}$	4	8	pF
C_{OUT}	Output Capacitance $V_{OUT} = 0\text{V}$	8	12	pF

NOTE: This parameter is periodically sampled and not 100% tested.

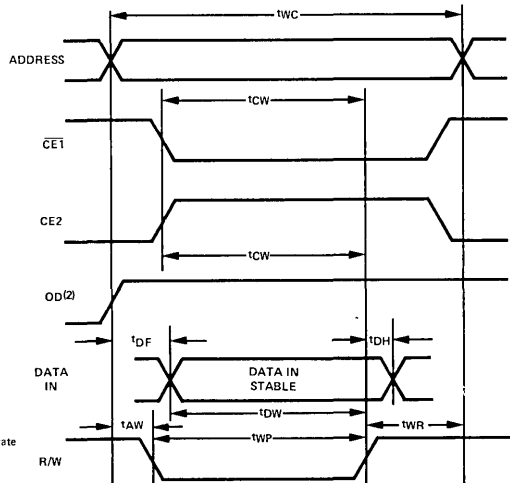
TIMING DIAGRAMS

READ CYCLE



- NOTES:
- t_{DF} is with respect to the trailing edge of $\overline{CE1}$, $CE2$, or OD , whichever occurs first.
 - During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
 - OD should be tied low for separate I/O operation.

WRITE CYCLE

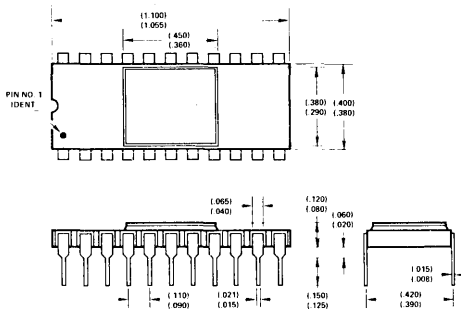




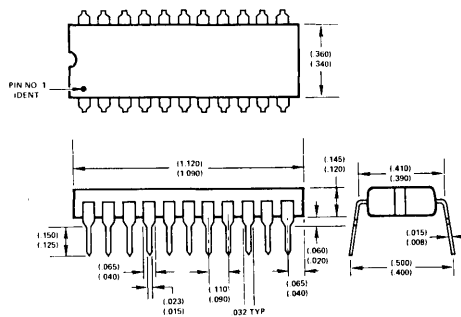
RAMs

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE





1024 x 1 Static Random Access Memory

SY2102

MEMORY PRODUCTS

RAMS

- Single +5 Volt Operation
- 3-State Outputs
- Directly TTL Compatible
- Low Power Dissipation
- Standby Power Mode

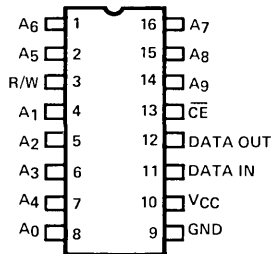
The 2102 family is a series of 1024 word by one bit static random access memory devices fabricated using Synertek's silicon gate technology. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102 family is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

A low standby power version is also available. It has all the same operating characteristics of the 2102-1 with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.

The family is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable (\overline{CE}) lead allows easy selection of an individual package when outputs are OR-tied.

PIN CONFIGURATION



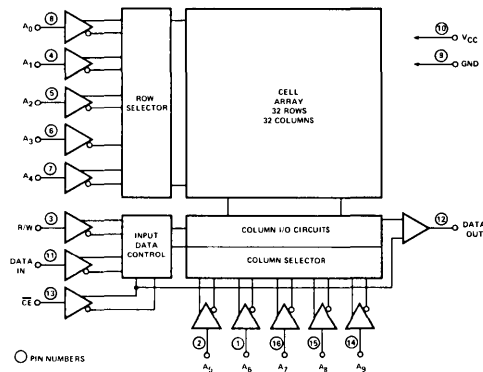
PIN NAMES

DIN	Data Input	\overline{CE}	Chip Enable
A ₀ -A ₉	Address Inputs	DOUT	Data Output
R/W	Read/Write Input	VCC	Power (+5V)

ORDERING INFORMATION

Order Number	Package Type	Access Time	Standby	Temperature Range
SYP2102A-2	Plastic DIP	250nsec	No	0°C to 70°C
SYC2102A-2	Ceramic DIP	250nsec	No	0°C to 70°C
SYP2102A-4	Plastic DIP	450nsec	No	0°C to 70°C
SYC2102A-4	Ceramic DIP	450nsec	No	0°C to 70°C
SYP2102-1	Plastic DIP	500nsec	No	0°C to 70°C
SYC2102-1	Ceramic DIP	500nsec	No	0°C to 70°C
SYP2102-1L	Plastic DIP	500nsec	Yes	0°C to 70°C
SYC2102-1L	Ceramic DIP	500nsec	Yes	0°C to 70°C
SYP2102-6	Plastic DIP	650nsec	No	0°C to 70°C

BLOCK DIAGRAM



TRUTH TABLE

\overline{CE}	R/W	DIN	DOUT	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	DOUT	READ

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	-10°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin	
With Respect To Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

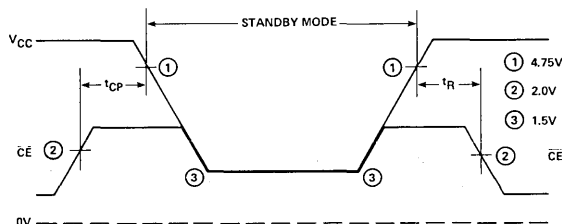
$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

Symbol	Parameter	2102A-4 Limits			2102A-2 Limits			2102-1, 2102-1L 2102A-6 Limits			Unit	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{LI}	Input Load Current	1	10	1	10	1	10	μA	$V_{IN} = 0$ to 5.25V			
I_{LOH}	Output Leakage Current	1	5	1	5	1	5	μA	$\overline{CE} = 2.0\text{V}$, $V_{OUT} = V_{OH}$			
I_{LOL}	Output Leakage Current	-1	-10	-1	-10	-1	-10	μA	$\overline{CE} = 2.0\text{V}$, $V_{OUT} = 0.4\text{V}$			
I_{CC}	Power Supply Current	33	55	45	65	33	55	mA	All Inputs = 5.25V , Data Out Open, $T_A = 0^\circ\text{C}$			
V_{IL}	Input Low Voltage	-0.5	0.8	-0.5	0.8	-0.5	0.65	V				
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}	2.2	V_{CC}	V				
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	$I_{OL} = 2.1\text{mA}$			
V_{OH}	Output High Voltage	2.4		2.4		2.2		V	$I_{OH} = 100\mu\text{A}$			

STANDBY CHARACTERISTICS – 2102-1L

$T_A = 0^\circ\text{C}$ to 70°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{PD}	V_{CC} in Standby	1.5			V	$2.0\text{V} \leq V_{PD} \leq V_{CC} \text{ Max}$ $1.5\text{V} \leq V_{PD} < 2.0\text{V}$
$V_{CES(1)}$	\overline{CE} Bias in Standby	2.0			V	
		V_{PD}			V	
I_{PD1}	Standby Current		15	23	mA	All Inputs = $V_{PD1} = 1.5\text{V}$ All Inputs = $V_{PD2} = 2.0\text{V}$
I_{PD2}	Standby Current		20	30	mA	
t_{CP}	Chip Deselect to Standby Time	0			ns	
$t_{R(2)}$	Standby Recovery Time	t_{RC}			ns	

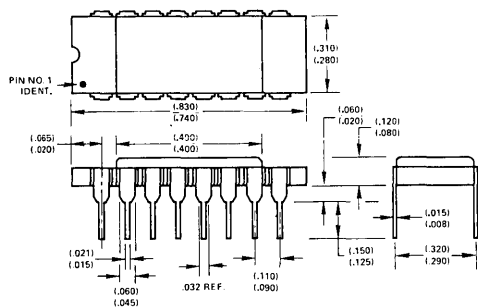
STANDBY WAVEFORMS

NOTES:

1. Consider the test conditions as shown: if the standby voltage (V_{PD}) is between 5.25V ($V_{CC} \text{ Max.}$) and 2.0V , then \overline{CE} must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V ($V_{PD} \text{ Min.}$), then \overline{CE} and standby voltage must be at least the same value or, if they are different, \overline{CE} must be the more positive of the two.

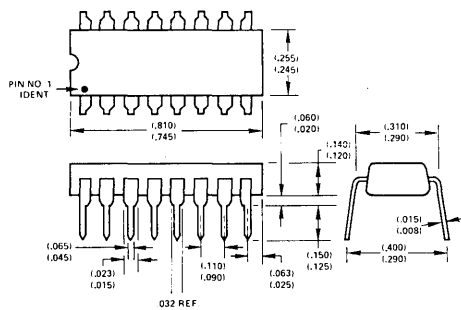
2. $t_R = t_{RC}$ (READ CYCLE TIME).

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE





1024 x 1 Static Random Access Memory

SY21H02

MEMORY PRODUCTS

RAMS

- 175/200 nsec Maximum Access Times
- Maximum Times Apply over Temperature Range and Supply Voltage Variation

PIN CONFIGURATION

BLOCK DIAGRAM

ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP21H02	Plastic DIP	175 ns	0°C to +55°C
SYC21H02	Ceramic DIP	175 ns	0°C to +55°C
SYP21H02-2	Plastic DIP	200 ns	0°C to +55°C
SYC21H02-2	Ceramic DIP	200 ns	0°C to +55°C

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-0.5V to +7V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+55^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ. (1)	Max.		
I _{LI}	Input Load Current (All Input Pins)			10	μA	V _{IN} = 0 to 5.25V
I _{LOH}	Output Leakage Current			5	μA	$\overline{CE} = 2.0V$, V _{OUT} = 2.4 to V _{CC}
I _{LOL}	Output Leakage Current			-10	μA	$\overline{CE} = 2.0V$, V _{OUT} = 0.4V
I _{CC1}	Power Supply Current		50	80	mA	All Inputs = 5.25V, Data Out Open, T _A = 25°C
I _{CC2}	Power Supply Current			90	mA	All Inputs = 5.25V, Data Out Open, T _A = 0°C
V _{IL}	Input "Low" Voltage	-0.5		0.8	V	
V _{IH}	Input "High" Voltage	2.0		V _{CC}	V	
V _{OL}	Output "Low" Voltage			0.4	V	I _{OL} = 2.1mA
V _{OH}	Output "High" Voltage	2.4			V	I _{OH} = -100μA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.



1024 x 1 Static Random Access Memory

SY21L02

MEMORY PRODUCTS

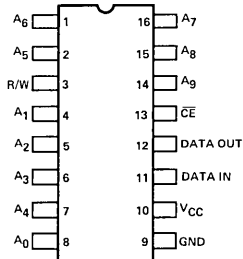
RAMS

- Low Power Maximum $I_{CC} = 15\text{mA}$ (SY21L02)
- Directly TTL Compatible
- 200mV Noise Immunity
- Single +5V Supply
- Standby Power Mode – 23mW

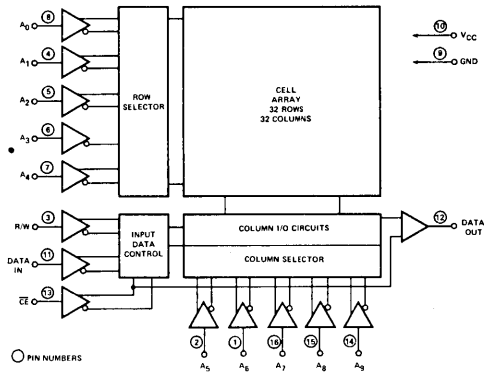
The Synertek SY21L02 is a 1024 word by one bit static random access memory element using N-channel depletion mode silicon gate devices. It uses fully stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The SY21L02 is designed for memory applications where very low power dissipation is required in the operating and standby modes. It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable (\overline{CE}) lead allows easy selection of an individual package when outputs are OR-tied.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP21L02	Plastic DIP	1μsec	0°C to 70°C
SYC21L02	Ceramic DIP	1μsec	0°C to 70°C
SYP21L02-1	Plastic DIP	500nsec	0°C to 70°C
SYC21L02-1	Ceramic DIP	500nsec	0°C to 70°C
SYP21L02A	Plastic DIP	350nsec	0°C to 70°C
SYC21L02A	Ceramic DIP	350nsec	0°C to 70°C
SYP21L02B	Plastic DIP	400nsec	0°C to 70°C
SYC21L02B	Ceramic DIP	400nsec	0°C to 70°C

21L02 PIN NAMES

DIN	DATA INPUT
A0-A9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
CE	CHIP ENABLE
DOUT	DATA OUTPUT
VCC	POWER (+5V)

NOTE: An "L" suffix (SYP21L02L, SYC21L02BL, etc.) indicates standby operation.



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

*COMMENTS

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC AND OPERATING CHARACTERISTICS (SY21L02)

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified

Symbol	Parameter	Min.	Typ. ⁽¹⁾	Max.	Unit	Test Conditions
I_{LI}	Input Load Current (All Input Pins)			10	μA	$V_{IN} = 0$ to 5.25V
I_{LOH}	Output Leakage Current			10	μA	$\overline{CE} = 2.2\text{V}$, $V_{OUT} = 4.0\text{V}$
I_{LOL}	Output Leakage Current			-100	μA	$\overline{CE} = 2.2\text{V}$, $V_{OUT} = 0.45\text{V}$
I_{CC1}	Power Supply Current		11	14	mA	All Inputs = 5.25V Data Out Open $T_A = 25^\circ\text{C}$
I_{CC2}	Power Supply Current		12	15	mA	All Inputs = 5.25V Data Out Open $T_A = 0^\circ\text{C}$
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	$I_{OL} = 1.9\text{mA}$
V_{OH}	Output "High" Voltage	2.4			V	$I_{OH} = -100\mu\text{A}$

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

DC AND OPERATING CHARACTERISTICS (SY21L02-1, SY21L02A, SY21L02B)

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.(1)	Max.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	$V_{IN} = 0$ to 5.25V
I_{LOH}	Output Leakage Current			5	μA	$\overline{CE} = 2.0\text{V}$, $V_{OUT} = 2.4$ to V_{CC}
I_{LOL}	Output Leakage Current			-10	μA	$\overline{CE} = 2.0\text{V}$, $V_{OUT} = 0.4\text{V}$
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	$I_{OL} = 3.2\text{mA}$
V_{OH}	Output "High" Voltage	2.4			V	$I_{OH} = -100\mu\text{A}$
I_{CC1}	Power Supply Current: SY21L02B		20	26	mA	All Inputs = 5.25V , Data Out Open, $T_A = 25^\circ\text{C}$
	SY21L02A		22	26	mA	
	SY21L02-1		24	34	mA	
I_{CC2}	Power Supply Current: SY21L02B			30	mA	All Inputs = 5.25V , Data Out Open, $T_A = 0^\circ\text{C}$
	SY21L02A			30	mA	
	SY21L02-1			40	mA	

NOTE: 1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.



RAMS

STANDBY CHARACTERISTICS (SY21L02L, SY21L02-1L, SY21L02AL, SY21L02BL)

$T_A = 0^\circ\text{C}$ to 70°C

Symbol	Parameter	Min.	Typ. ⁽¹⁾	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	1.5			V	
$V_{CES(2)}$	\overline{CE} Bias in Standby	2.0			V	$2.0\text{V} \leq V_{PD} \leq V_{CC}$ Max. $1.5\text{V} \leq V_{PD} < 2.0\text{V}$
		V_{PD}			V	
I_{PD1}	Standby Current Drain		9	10	mA	All Inputs = $V_{PD1} = 1.5\text{V}$
I_{PD2}	Standby Current Drain		11	12	mA	All Inputs = $V_{PD2} = 2.0\text{V}$
t_{CP}	Chip Deselect to Standby Time	0			ns	
$t_R(3)$	Standby Recovery Time	t_{RC}			ns	

NOTE 1: Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

NOTE 2: Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then \overline{CE} must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min.), then \overline{CE} and standby voltage must be at least the same value or, if they are different, \overline{CE} must be the more positive of the two.

NOTE 3: $t_R = t_{RC}$ (READ CYCLE TIME).

AC CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified

Symbol	Parameter	SY21L02		SY21L02-1		SY21L02A		SY21L02B		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	

READ CYCLE

t_{RC}	Read Cycle	1000		500		350		400		nsec
t_A	Access Time		1000		500		350		400	nsec
t_{CO}	Chip Enable to Output Time		500		350		180		150	nsec
t_{OH1}	Previous Read Data Valid with Respect to Address	50		50		40		40		nsec
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0		nsec

WRITE CYCLE

t_{WC}	Write Cycle	1000		500		350		400		nsec
t_{AW}	Address to Write Setup Time	200		150		20		20		nsec
t_{WP}	Write Pulse Width	750		300		250		150		nsec
t_{WR}	Write Recovery Time	50		50		0		0		nsec
t_{DW}	Data Setup Time	800		330		250		125		nsec
t_{DH}	Data Hold Time	100		100		0		0		nsec
t_{CW}	Chip Enable to Write Setup Time	900		400		250		150		nsec

CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$

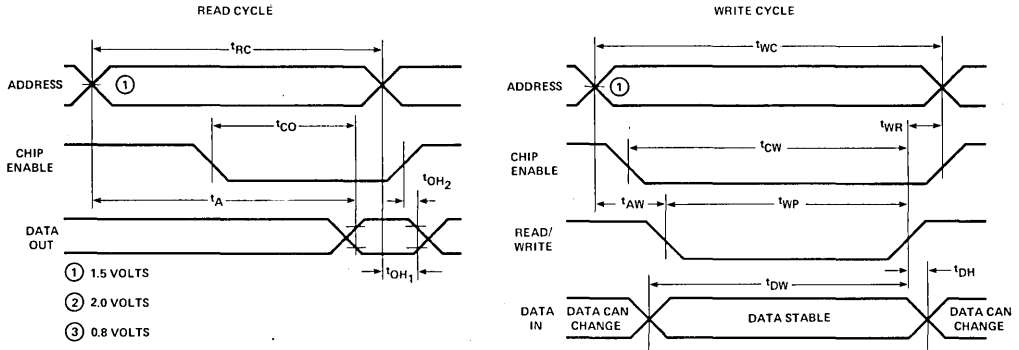
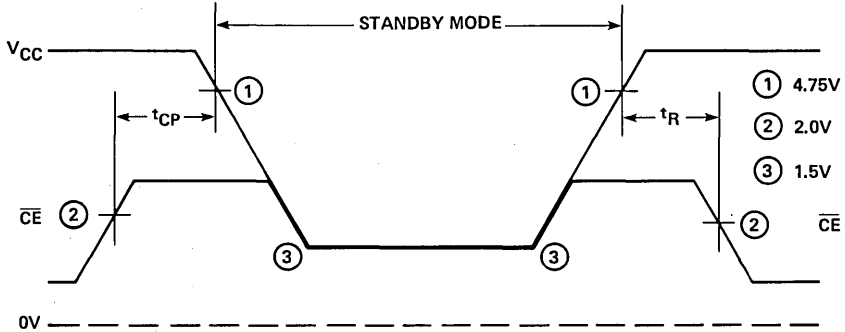
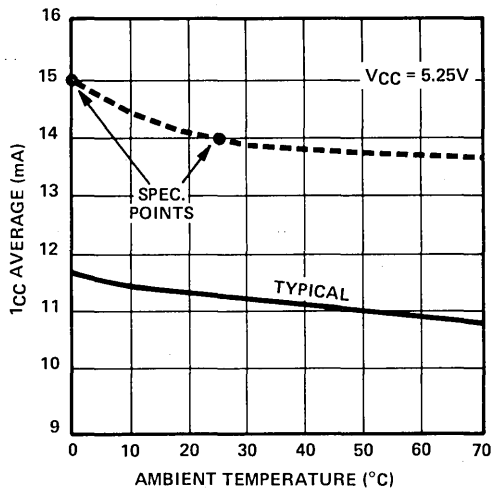
Symbol	Test	Typ.	Max.	Units
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0\text{V}$	3	5	pF
C_{OUT}	Output Capacitance $V_{OUT} = 0\text{V}$	7	10	pF

NOTE: This parameter is periodically sampled and is not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels: +0.65 Volt to 2.2 Volt
 Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt
 Output Load: 1 TTL Gate and $C_L = 100\text{pF}$

TIMING DIAGRAMS

STANDBY WAVEFORMS

TYPICAL DC CHARACTERISTICS
POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE




256x4 Static Random Access Memory

SY2111

MEMORY PRODUCTS

RAMS

- Organization 256 Words By 4 Bits
- Common Data Input And Output
- Single +5V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Access Time – 250/350/450/500ns
- Simple Memory Expansion – 2 Chip Enable Inputs
- Fully Decoded – On-Chip Address Decode
- Inputs Protected – All Inputs have Protection Against Static Charge
- Low Cost Packaging – 18 Pin Plastic Dual-In-Line Configuration
- Low Power – Typically 150mW
- Three - State Output – OR - Tie Capability

The SY2111 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The SY2111 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

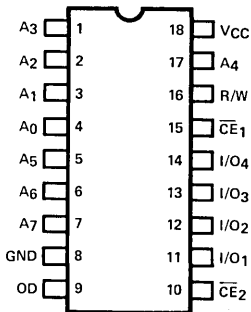
It is directly TTL compatible in all respects: inputs,

outputs, and a single +5V supply. Separate Chip Enable leads allow easy selection of an individual package when outputs are OR-tied.

The SY2111 is fabricated with N-channel ion-implanted silicon gate technology, which allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

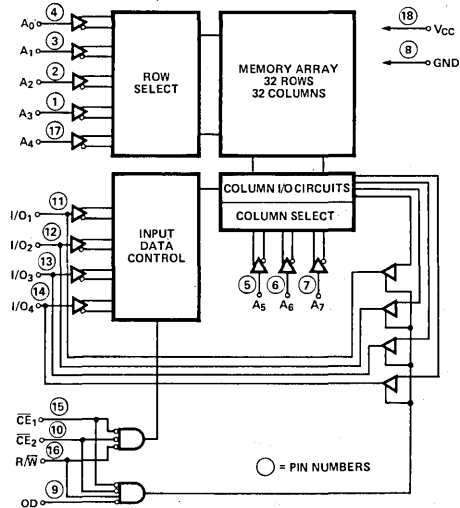
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP2111-1	Plastic DIP	500 ns	0°C to 70°C
SYC2111-1	Ceramic DIP	500 ns	0°C to 70°C
SYP2111A-2	Plastic DIP	250 ns	0°C to 70°C
SYC2111A-2	Ceramic DIP	250 ns	0°C to 70°C
SYP2111A	Plastic DIP	350 ns	0°C to 70°C
SYC2111A	Ceramic DIP	350 ns	0°C to 70°C
SYP2111A-4	Plastic DIP	450 ns	0°C to 70°C
SYC2111A-4	Ceramic DIP	450 ns	0°C to 70°C

BLOCK DIAGRAM



PIN NAMES

A ₀ -A ₇	ADDRESS INPUTS	CE ₁	CHIP ENABLE 1
OD	OUTPUT DISABLE	CE ₂	CHIP ENABLE 2
R/W	READ/WRITE INPUT	I/O ₁ -I/O ₄	DATA INPUT/OUTPUT

**ABSOLUTE MAXIMUM RATINGS**

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	2111-1			2111A			Unit	Test Conditions
		Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.		
I _{LI}	Input Load Current			10			10	μA	V _{IN} = 0 to 5.25V
I _{LOH}	I/O Leakage Current			15			10	μA	CE = 2.2V, V _{I/O} = 4.0V
I _{LOL}	I/O Leakage Current			-50			-10	μA	CE = 2.2V, V _{I/O} = 0.45V
I _{CC1}	Power Supply Current		30	60		30	50	mA	V _{IN} = 5.25V I _{I/O} = 0mA, T _A = 25°C
I _{CC2}	Power Supply Current			70			55	mA	V _{IN} = 5.25V I _{I/O} = 0mA, T _A = 0°C
V _{IL}	Input Low Voltage	-0.5		+0.65	-0.5		+0.8	V	
V _{IH}	Input High Voltage	2.2		V _{CC}	2.0		V _{CC}	V	
V _{OL}	Output Low Voltage			0.45			0.4	V	I _{OL} = 3.2mA (I _{OL} = 2.0mA - 2111-1)
V _{OH}	Output High Voltage	2.2			2.4			V	I _{OH} = -150μA

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS – SY2111-1

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
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READ CYCLE

t _{RCY}	Read Cycle	500		ns
t _A	Access Time		500	ns
t _{CO}	Chip Enable To Output		350	ns
t _{OD}	Output Disable To Output		300	ns
t _{DF} [1]	Data Output To High Z State	0	150	ns
t _{OH}	Previous Data Read Valid After Change Of Address	0		ns

WRITE CYCLE

t _{WCY}	Write Cycle	500		ns
t _{AW}	Write Delay	100		ns
t _{CW}	Chip Enable To Write	400		ns
t _{DW}	Data Setup	280		ns
t _{DH}	Data Hold	100		ns
t _{WP}	Write Pulse	300		ns
t _{WR}	Write Recovery	50		ns
t _{DS}	Output Disable Setup	20		ns

NOTE: 1. t_{DF} is with respect to the trailing edge of CE1, CE2, or OD, whichever comes first.

A.C. CHARACTERISTICS – SY2111A-2

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	250		ns
t_A	Access Time		250	ns
t_{CO}	Chip Enable To Output		180	ns
t_{OD}	Output Disable To Output		130	ns
$t_{DF}[1]$	Data Output To High Z State	0	180	ns
t_{OH}	Previous Data Read Valid After Change Of Address	40		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	250		ns
t_{AW}	Write Delay	20		ns
t_{CW}	Chip Enable To Write	150		ns
t_{DW}	Data Setup	150		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	150		ns
t_{WR}	Write Recovery	0		ns
t_{DS}	Output Disable Setup	20		ns

A.C. CHARACTERISTICS – SY2111A

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	350		ns
t_A	Access Time		350	ns
t_{CO}	Chip Enable To Output		240	ns
t_{OD}	Output Disable To Output		180	ns
$t_{DF}[1]$	Data Output To High Z State	0	150	ns
t_{OH}	Previous Data Read Valid After Change Of Address	40		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	350		ns
t_{AW}	Write Delay	20		ns
t_{CW}	Chip Enable To Write	200		ns
t_{DW}	Data Setup	200		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	200		ns
t_{WR}	Write Recovery	0		ns
t_{DS}	Output Disable Setup	20		ns

NOTE: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, $\overline{CE2}$, or OD, whichever comes first.



256 x 4 Static Random Access Memory

SY21H11

MEMORY PRODUCTS

RAMS

- Organization – 256 Words By 4 Bits
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Access Time – 175/200 ns
- Fully Decoded – On-Chip Address Decode
- Inputs Protected – All Inputs Have Protection Against Static Charge
- Low Cost Packaging – 18 Pin Plastic Dual-In-Line Configuration
- Three-State Output – OR-Tie Capability
- Simple Memory Expansion – 2 Chip Enable Inputs

The SY21H11 is a 256-word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The SY21H11 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

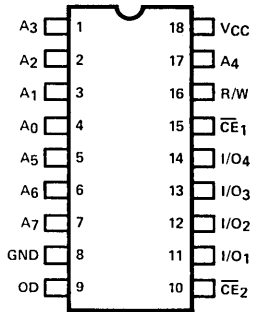
It is directly TTL compatible in all respects: inputs,

outputs, and a single +5V supply. Separate Chip Enable leads allow easy selection of an individual package when outputs are OR-tied.

The SY21H11 is fabricated with N-channel ion-implanted silicon gate technology, which allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost packaging.

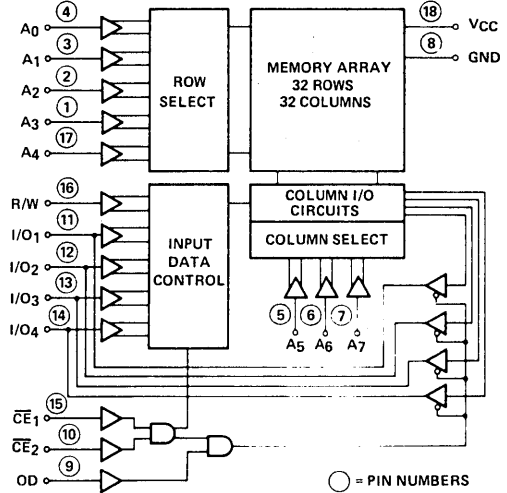
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP21H11	Plastic DIP	175 ns	0°C to 55°C
SYC21H11	Ceramic DIP	175 ns	0°C to 55°C
SYP21H11-2	Plastic DIP	200 ns	0°C to 55°C
SYC21H11-2	Ceramic DIP	200 ns	0°C to 55°C

BLOCK DIAGRAM



PIN NAMES

A0-A7	ADDRESS INPUTS	CE1	CHIP ENABLE 1
OD	OUTPUT DISABLE	CE2	CHIP ENABLE 2
R/W	READ/WRITE INPUT	I/O1-I/O4	DATA INPUT/OUTPUT

**ABSOLUTE MAXIMUM RATINGS**

Ambient Temperature Under Bias	0°C to 55°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to 55°C , $V_{CC} = 5\text{V} \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min	Typ.(1)	Max	Unit	Test Conditions
I_{LI}	Input Load Current			10	μA	$V_{IN} = 0$ to 5.25V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE} = 2.2\text{V}$, $V_{I/O} = 4.0\text{V}$
I_{LOL}	I/O Leakage Current			-50	μA	$\overline{CE} = 2.2\text{V}$, $V_{I/O} = 0.45\text{V}$
I_{CC1}	Power Supply Current		50	80	mA	$V_{IN} = 5.25\text{V}$ $I_{I/O} = 0\text{mA}$, $T_A = 25^\circ\text{C}$
I_{CC2}	Power Supply Current			90	mA	$V_{IN} = 5.25\text{V}$ $I_{I/O} = 0\text{mA}$, $T_A = 0^\circ\text{C}$
V_{IL}	Input Low Voltage	-0.5		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 3.2\text{mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -150\mu\text{A}$

NOTES: 1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

A.C. CHARACTERISTICS – SY21H11

READ CYCLE $T_A = 0^\circ\text{C}$ to 55°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RCY}	Read Cycle	175			ns
t_A	Access Time			175	ns
t_{CO}	Chip Enable to Output			100	ns
t_{OD}	Output Disable to Output			90	ns
$t_{DF}^{[1]}$	Data Output to High Z State	0		70	ns
t_{OH}	Previous Data Read Valid After Change of Address	0			ns

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WCY}	Write Cycle	175			ns
t_{AW}	Write Delay	0			ns
t_{CW}	Chip Enable to Write	100			ns
t_{DW}	Data Setup	100			ns
t_{DH}	Data Hold	0			ns
t_{WP}	Write Pulse	150			ns
t_{WR}	Write Recovery	0			ns

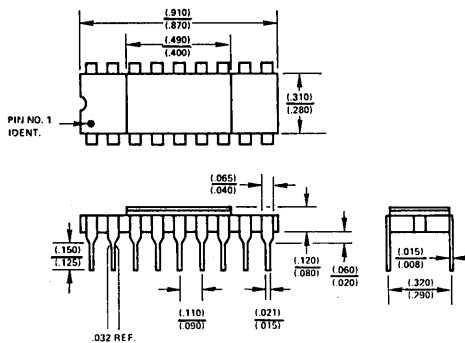
NOTE: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, $\overline{CE2}$, or OD, whichever comes first.

RAMS

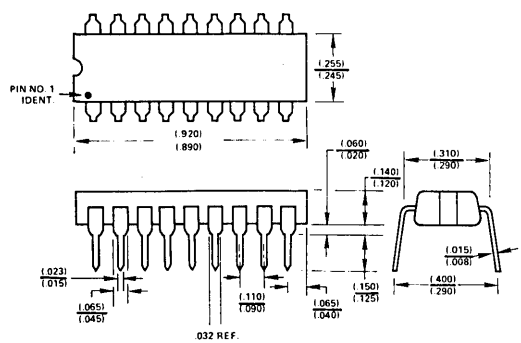
RAMS

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE





256 x 4 Static Random Access Memory

SY2112

MEMORY PRODUCTS

RAMS

- Organization 256 Words by 4 Bits
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible - All Inputs and Outputs
- Static MOS - No Clocks or Refreshing Required
- Access Time - 250/350/450/500 ns
- Simple Memory Expansion - Chip Enable Input
- Fully Decoded - On-Chip Address Decode
- Inputs Protected - All Inputs Have Protection Against Static Charge
- Low Cost Packaging - 16 Pin Plastic Dual-In-Line Configuration
- Low Power - Typically 150 mW
- Three-State Output - OR-tie Capability

The SY2112 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

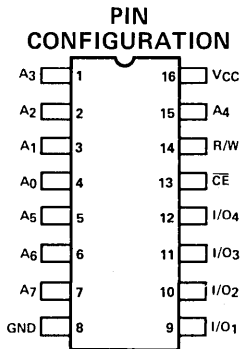
The SY2112 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip

Enable lead allows easy selection of an individual package when outputs are OR-tied.

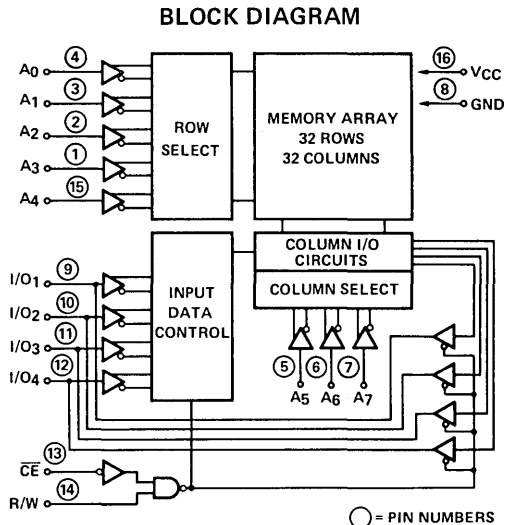
The SY2112 is fabricated with ion implanted N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's ion implanted silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP2112A-2	Plastic DIP	250nsec	0°C to 70°C
SYC2112A-2	Ceramic DIP	250nsec	0°C to 70°C
SYP2112A	Plastic DIP	350nsec	0°C to 70°C
SYC2112A	Ceramic DIP	350nsec	0°C to 70°C
SYP2112A-4	Plastic DIP	450nsec	0°C to 70°C
SYC2112A-4	Ceramic DIP	450nsec	0°C to 70°C
SYP2112-1	Plastic DIP	500nsec	0°C to 70°C
SYC2112-1	Ceramic DIP	500nsec	0°C to 70°C



PIN NAMES

A ₀ -A ₇	ADDRESS INPUTS
R/W	READ/WRITE INPUT
CE	CHIP ENABLE INPUT
I/O ₁ -I/O ₄	DATA INPUT/OUTPUT
V _{CC}	POWER (+5V)

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

***COMMENT**

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. AND OPERATING CHARACTERISTICS – SY2112A, SY2112A-2, SY2112A-4

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit	Test Conditions
I _{LI}	Input Current			10	μA	$V_{IN} = 0$ to 5.25V
I _{LOH}	I/O Leakage Current			10	μA	$\overline{CE} = 2.2\text{V}$, $V_{I/O} = 4.0\text{V}$
I _{LOL}	I/O Leakage Current			-10	μA	$\overline{CE} = 2.2\text{V}$, $V_{I/O} = 0.45\text{V}$
I _{CC1}	Power Supply Current		30	50	mA	$V_{IN} = 5.25\text{V}$, $I_{I/O} = 0\text{mA}$ $T_A = 25^\circ\text{C}$
I _{CC2}	Power Supply Current			55	mA	$V_{IN} = 5.25\text{V}$, $I_{I/O} = 0\text{mA}$ $T_A = 0^\circ\text{C}$
V _{IL}	Input "Low" Voltage	-0.5		+0.8	V	
V _{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V _{OL}	Output "Low" Voltage			+0.4	V	$I_{OL} = 3.2\text{mA}$
V _{OH}	Output "High" Voltage	2.4			V	$I_{OH} = -150\mu\text{A}$

NOTES: 1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

D. C. AND OPERATING CHARACTERISTICS – SY2112-1

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit	Test Conditions
I _{LI}	Input Current			10	μA	$V_{IN} = 0$ to 5.25V
I _{LOH}	I/O Leakage Current			15	μA	$\overline{CE} = 2.2\text{V}$, $V_{I/O} = 4.0\text{V}$
I _{LOL}	I/O Leakage Current			-50	μA	$\overline{CE} = 2.2\text{V}$, $V_{I/O} = 0.45\text{V}$
I _{CC1}	Power Supply Current		30	60	mA	$V_{IN} = 5.25\text{V}$, $I_{I/O} = 0\text{mA}$ $T_A = 25^\circ\text{C}$
I _{CC2}	Power Supply Current			70	mA	$V_{IN} = 5.25\text{V}$, $I_{I/O} = 0\text{mA}$ $T_A = 0^\circ\text{C}$
V _{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V _{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V _{OL}	Output "Low" Voltage			+0.45	V	$I_{OL} = 2\text{mA}$
V _{OH}	Output "High" Voltage	2.2			V	$I_{OH} = -150\mu\text{A}$

NOTES: 1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

A. C. CHARACTERISTICS – SY2112A-2

READ CYCLE $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
tRCY	Read Cycle	250		ns
tA	Access Time		250	ns
tCO	Chip Enable to Output Time		180	ns
tCD	Chip Enable to Output Disable Time	0	120	ns
tOH	Previous Read Data Valid After Change of Address	40		ns

WRITE CYCLE NO. 1 $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
tWCY1	Write Cycle	250		ns
tAW1	Address to Write Setup Time	20		ns
tDW1	Write Setup Time	180		ns
tWP1	Write Pulse Width	180		ns
tCS1	Chip Enable Setup Time	0	100	ns
tCH1	Chip Enable Hold Time	0		ns
tWR1	Write Recovery Time	0		ns
tDH1	Data Hold Time	0		ns
tCW1	Chip Enable to Write Setup Time	180		ns

WRITE CYCLE NO. 2 $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
tWCY2	Write Cycle	250		ns
tAW2	Address to Write Setup Time	20		ns
tDW2	Write Setup Time	180		ns
tWD2	Write To Output Disable Time	120	100	ns
tCS2	Chip Enable Setup Time	0		ns
tCH2	Chip Enable Hold Time	0		ns
tWR2	Write Recovery Time	0		ns
tDH2	Data Hold Time	0		ns

A. C. CHARACTERISTICS – SY2112A

READ CYCLE $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
tRCY	Read Cycle	350		ns
tA	Access Time		350	ns
tCO	Chip Enable to Output Time		240	ns
tCD	Chip Enable to Output Disable Time	0	200	ns
tOH	Previous Read Data Valid After Change of Address	40		ns

A. C. CHARACTERISTICS – SY2112A (Cont.)

WRITE CYCLE NO. 1 $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
tWCY1	Write Cycle	350		ns
tAW1	Address to Write Setup Time	20		ns
tDW1	Write Setup Time	250		ns
tWP1	Write Pulse Width	250		ns
tCS1	Chip Enable Setup Time	0	100	ns
tCH1	Chip Enable Hold Time	0		ns
tWR1	Write Recovery Time	0		ns
tDH1	Data Hold Time	0		ns
tCW1	Chip Enable to Write Setup Time	250		ns

WRITE CYCLE NO. 2 $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
tWCY2	Write Cycle	350		ns
tAW2	Address to Write Setup Time	20		ns
tDW2	Write Setup Time	250		ns
tWD2	Write To Output Disable Time	200	130	ns
tCS2	Chip Enable Setup Time	0		ns
tCH2	Chip Enable Hold Time	0		ns
tWR2	Write Recovery Time	0		ns
tDH2	Data Hold Time	0		ns

A. C. CHARACTERISTICS – SY2112A-4

READ CYCLE $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
tRCY	Read Cycle	450		ns
tA	Access Time		450	ns
tCO	Chip Enable to Output Time		200	ns
tCD	Chip Enable to Output Disable Time	0	260	ns
tOH	Previous Read Data Valid After Change of Address	40		ns

WRITE CYCLE NO. 1 $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
tWCY1	Write Cycle	450		ns
tAW1	Address to Write Setup Time	20		ns
tDW1	Write Setup Time	300		ns
tWP1	Write Pulse Width	300		ns
tCS1	Chip Enable Setup Time	0	100	ns
tCH1	Chip Enable Hold Time	0		ns
tWR1	Write Recovery Time	0		ns
tDH1	Data Hold Time	0		ns
tCW1	Chip Enable to Write Setup Time	300		ns

A. C. CHARACTERISTICS – SY2112A-4 (Cont.)

WRITE CYCLE NO. 2 $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
tWCY2	Write Cycle	450		ns
tAW2	Address to Write Setup Time	20		ns
tDW2	Write Setup Time	300		ns
tWD2	Write To Output Disable Time	260	150	ns
tCS2	Chip Enable Setup Time	0		ns
tCH2	Chip Enable Hold Time	0		ns
tWR2	Write Recovery Time	0		ns
tDH2	Data Hold Time	0		ns

A. C. CHARACTERISTICS – SY2112-1

READ CYCLE $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
trCY	Read Cycle	500		ns	$t_r, t_f \leq 20\text{ns}$
tA	Access Time		500	ns	$0.65V \geq V_{IN} \geq 2.2V$
tCO	Chip Enable To Output Time		350	ns	Timing Reference = 1.5V
tCD	Chip Enable To Output Disable Time	0	150	ns	Load = 1 TTL Gate
tOH	Previous Read Data Valid After Change of Address	0		ns	$C_L = 100\text{pF}$

WRITE CYCLE NO. 1 $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
tWCY1	Write Cycle	500		ns	$t_r, t_f \leq 20\text{ns}$
tAW1	Address To Write Setup Time	100		ns	$0.65V \geq V_{IN} \geq 2.2V$
tDW1	Write Setup Time	200		ns	Timing Reference = 1.5V
tWP1	Write Pulse Width	300		ns	Load = 1 TTL Gate
tCS1	Chip Enable Setup Time	0	100	ns	$C_L = 100\text{pF}$
tCH1	Chip Enable Hold Time	0		ns	
tWR1	Write Recovery Time	50		ns	
tDH1	Data Hold Time	100		ns	
tCW1	Chip Enable to Write Setup Time	200		ns	

WRITE CYCLE NO. 2 $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
tWCY2	Write Cycle	500		ns	$t_r, t_f \leq 20\text{ns}$
tAW2	Address To Write Setup Time	100		ns	$0.65V \geq V_{IN} \geq 2.2V$
tDW2	Write Setup Time	200		ns	Timing Reference = 1.5V
tWD2	Write To Output Disable Time	100		ns	Load = 1 TTL Gate
tCS2	Chip Enable Setup Time	0		ns	$C_L = 100\text{pF}$
tCH2	Chip Enable Hold Time	0		ns	
tWR2	Write Recovery Time	50		ns	
tDH2	Data Hold Time	100		ns	



256 x 4 Static Random Access Memory

SY21H12

MEMORY PRODUCTS

- Organization-256 Words By 4 Bits
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible - All Inputs and Outputs
- Access Time - 175/200 ns
- Simple Memory Expansion - Chip Enable Input

- Fully Decoded - On-Chip Address Decode
- Inputs Protected - All Inputs Have Protection Against Static Charge
- Low Cost Packaging - 16 Pin Plastic Dual-In-Line Configuration
- Three-State Output - OR-Tie Capability

The SY21H12 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The SY21H12 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

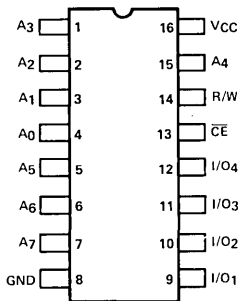
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip

Enable lead allows easy selection of an individual package when outputs are OR-tied.

The SY21H12 is fabricated with ion implanted N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's ion implanted silicon gate technology also provides excellent protection against contamination. This permits the use of low cost packaging.

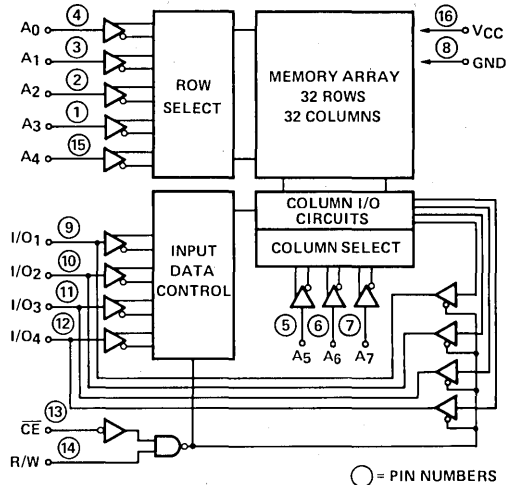
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP21H12	Plastic DIP	175nsec	0°C to 55°C
SYC21H12	Ceramic DIP	175nsec	0°C to 55°C
SYP21H12-2	Plastic DIP	200nsec	0°C to 55°C
SYC21H12-2	Ceramic DIP	200nsec	0°C to 55°C

BLOCK DIAGRAM



PIN NAMES

A ₀ -A ₇	ADDRESS INPUTS
R/W	READ/WRITE INPUT
CE	CHIP ENABLE INPUT
I/O ₁ -I/O ₄	DATA INPUT/OUTPUT
V _{CC}	POWER (+5V)

**ABSOLUTE MAXIMUM RATINGS***

Ambient Temperature Under Bias	0°C to 55°C
Storage Temperature	-65°C to 150°C
Voltage On Any Pin	
With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

***COMMENTS**

Stresses above those listed under "Absolute Maximum Ratings" may cause damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. AND OPERATING CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to 55°C , $V_{CC} = 5\text{V} \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	$V_{IN} = 0$ to 5.25V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE} = 2.2\text{V}$, $V_{I/O} = 4.0\text{V}$
I_{LOL}	I/O Leakage Current			-50	μA	$\overline{CE} = 2.2\text{V}$, $V_{I/O} = 0.45\text{V}$
I_{CC1}	Power Supply Current		50	80	mA	$V_{IN} = 5.25\text{V}$, $I_{I/O} = 0\text{mA}$ $T_A = 25^\circ\text{C}$
I_{CC2}	Power Supply Current			90	mA	$V_{IN} = 5.25\text{V}$, $I_{I/O} = 0\text{mA}$ $T_A = 0^\circ\text{C}$
V_{IL}	Input "Low" Voltage	-0.5		+0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.4	V	$I_{OL} = 3.2\text{mA}$
V_{OH}	Output "High" Voltage	2.4			V	$I_{OH} = -150\mu\text{A}$

NOTE: 1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

A. C. CHARACTERISTICS – SY21H12

READ CYCLE $T_A = 0^\circ\text{C}$ to 55°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified

Symbol	Parameter	Min.	Max.	Unit
t_{RCY}	Read Cycle		175	ns
t_A	Access Time		175	ns
t_{CO}	Chip Enable to Output Time		110	ns
t_{CD}	Chip Enable to Output Disable Time	0	70	ns
t_{OH}	Previous Read Data Valid After Change of Address	0		ns

WRITE CYCLE NO. 1 $T_A = 0^\circ\text{C}$ to 55°C , $V_{CC} = 5\text{V} \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
t_{WCY1}	Write Cycle		175	ns
t_{AW1}	Address to Write Setup Time	0		ns
t_{DW1}	Write Setup Time	100		ns
t_{WP1}	Write Pulse Width	150		ns
t_{CS1}	Chip Enable Setup Time	0	50	ns
t_{CH1}	Chip Enable Hold Time	0		ns
t_{WR1}	Write Recovery Time	0		ns
t_{DH1}	Data Hold Time	0		ns
t_{CW1}	Chip Enable to Write Setup Time	100		ns

WRITE CYCLE NO. 2 $T_A = 0^{\circ}\text{C}$ to 55°C , $V_{CC} = 5\text{V} \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
tWCY2	Write Cycle	175		ns
tAW2	Address to Write Setup Time	0		ns
tDW2	Write Setup Time	100		ns
tWD2	Write to Output Disable Time		70	ns
tCS2	Chip Enable Setup Time	0		ns
tCH2	Chip Enable Hold Time	0		ns
tWR2	Write Recovery Time	0		ns
tDH2	Data Hold Time	0		ns

A. C. CHARACTERISTICS – SY21H12-2
READ CYCLE $T_A = 0^{\circ}\text{C}$ to 55°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified

Symbol	Parameter	Min.	Max.	Unit
tRCY	Read Cycle	200		ns
tA	Access Time		200	ns
tCO	Chip Enable to Output Time		120	ns
tCD	Chip Enable to Output Disable Time	0	80	ns
tOH	Previous Read Data Valid After Change of Address	0		ns

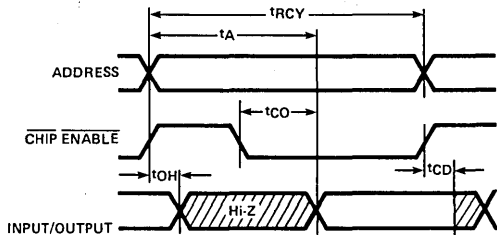
WRITE CYCLE NO. 1 $T_A = 0^{\circ}\text{C}$ to 55°C , $V_{CC} = 5\text{V} \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
tWCY1	Write Cycle	200		ns
tAW1	Address to Write Setup Time	0		ns
tDW1	Write Setup Time	120		ns
tWP1	Write Pulse Width	170		ns
tCS1	Chip Enable Setup Time	0	50	ns
tCH1	Chip Enable Hold Time	0		ns
tWR1	Write Recovery Time	0		ns
tDH1	Data Hold Time	0		ns
tCW1	Chip Enable to Write Setup Time	120		ns

WRITE CYCLE NO. 2 $T_A = 0^{\circ}\text{C}$ to 55°C , $V_{CC} = 5\text{V} \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
tWCY2	Write Cycle	200		ns
tAW2	Address to Write Setup Time	0		ns
tDW2	Write Setup Time	120		ns
tWD2	Write to Output Disable Time		80	ns
tCS2	Chip Enable Setup Time	0		ns
tCH2	Chip Enable Hold Time	0		ns
tWR2	Write Recovery Time	0		ns
tDH2	Data Hold Time	0		ns

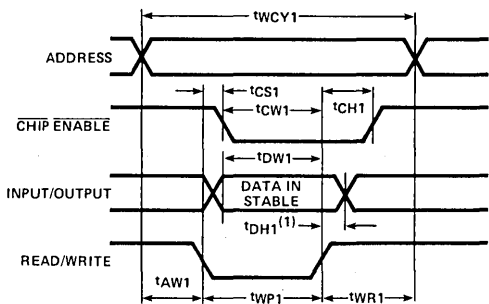
READ CYCLE WAVEFORMS



CAPACITANCE

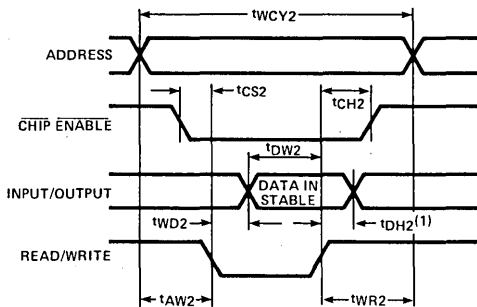
Symbol	Test	Limits (pF)	
		Typ.	Max.
C _{IN}	Input Capacitance (All Input Pins) V _{IN} = 0V	4	8
C _{I/O}	I/O Capacitance V _{I/O} = 0V	10	18

WRITE CYCLE #1



NOTE 1. Data Hold Time. (t_{DH}) is reference to the trailing edge of CHIP ENABLE (CE) or READ/WRITE (R/W) whichever comes first.

WRITE CYCLE #2



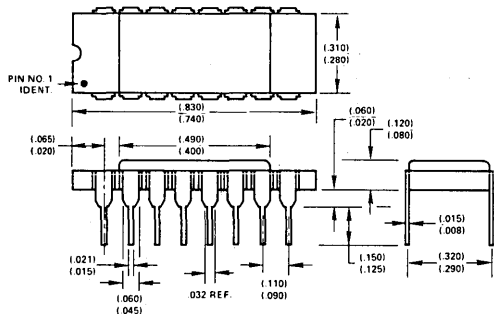
$$T_A = 0^{\circ}\text{C to } 55^{\circ}\text{C, } V_{CC} = 5\text{V} \pm 5\%$$

A.C. CONDITIONS OF TEST

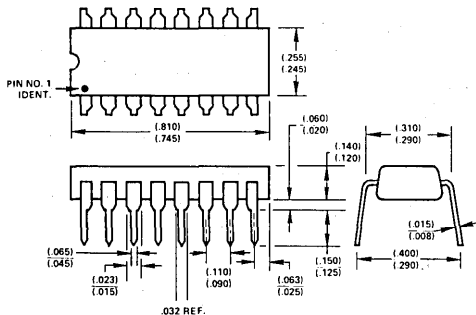
Input Pulse Levels	+0.8 Volt to 2.0 Volt
Input Rise and Fall Times	10 nsec
Timing Measurement Reference Levels:	
Input	1.5 Volt
Output	0.8 and 2.0 Volt
Output Load	.1 TTL Gate and C _L = 100 pF

PACKAGE DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE





1024x4 Static Random Access Memory

SY2114

MEMORY PRODUCTS

RAMS

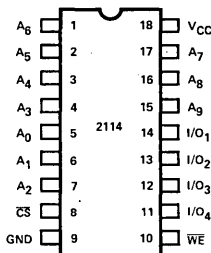
- 200 ns Maximum Access
- Low Operating Power Dissipation
0.1 mW/Bit
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible:
All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

The SY2114 is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 1 TTL load.

The SY2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select (CS) input allows easy selection of an individual device when outputs are or-tied.

The SY2114 is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology — a technology providing excellent performance characteristics as well as improved protection against contamination.

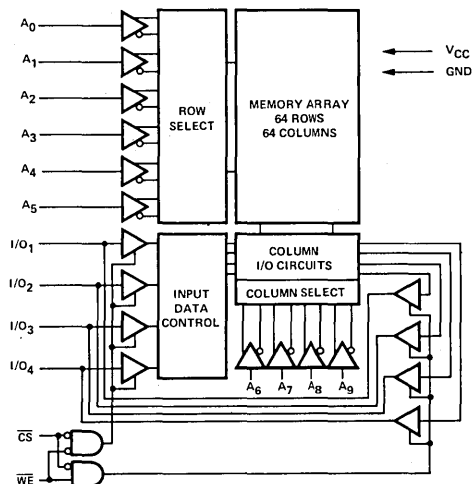
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYC2114	Ceramic	450nsec	100mA	0°C to 70°C
SYP2114	Molded	450nsec	100mA	0°C to 70°C
SYC2114-3	Ceramic	300nsec	100mA	0°C to 70°C
SYP2114-3	Molded	300nsec	100mA	0°C to 70°C
SYC2114L	Ceramic	450nsec	70mA	0°C to 70°C
SYP2114L	Molded	450nsec	70mA	0°C to 70°C
SYC2114L-3	Ceramic	300nsec	70mA	0°C to 70°C
SYP2114L-3	Molded	300nsec	70mA	0°C to 70°C
SYC2114-2	Ceramic	200nsec	100mA	0°C to 70°C
SYP2114-2	Molded	200nsec	100mA	0°C to 70°C
SYC2114L-2	Ceramic	200nsec	70mA	0°C to 70°C
SYP2114L-2	Molded	200nsec	70mA	0°C to 70°C

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-0.5V to +7 V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ (Unless otherwise specified)

Symbol	Parameter	2114-2 2114-3,2114		2114L-2 2114L,2114L-3		Unit	Conditions
		Min	Max	Min	Max		
I _{LI}	Input Load Current (All input pins)		10		10	μA	V _{IN} = 0 to 5.25V
I _{LO}	I/O Leakage Current		10		10	μA	$\overline{\text{CS}} = 2.0\text{V}$, V _{I/O} = 0.4V to V _{CC}
I _{CC1}	Power Supply Current		95		65	mA	V _{CC} = 5.25V, I _{I/O} = 0 mA, T _A = 25°C
I _{CC2}	Power Supply Current		100		70	mA	V _{CC} = 5.25V, I _{I/O} = 0 mA, T _A = 0°C
V _{IL}	Input Low Voltage	-0.5	0.8	-0.5	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC}	2.0	V _{CC}	V	
V _{OL}	Output Low Voltage		0.4		0.4	V	I _{OL} = 3.2 mA
V _{OH}	Output High Voltage	2.4	V _{CC}	2.4	V _{CC}	V	I _{OH} = -1.0 mA

CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$

Symbol	Test	Typ	Max	Units
C _{I/O}	Input/Output Capacitance		5	pF
C _{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ (Unless Otherwise Specified)

Symbol	Parameter	2114-2,2114L-2		2114-3,2114L-3		2114,2114L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{RC}	Read Cycle Time	200		300		450		nsec
t _A	Access Time		200		300		450	nsec
t _{CO}	Chip Select to Output Valid		70		100		120	nsec
t _{CX}	Chip Select to Output Enabled	20		20		20		nsec
t _{OTD}	Chip Deselect to Output Off	0	60	0	80	0	100	nsec
t _{OHA}	Output Hold From Address Change	50		50		50		nsec
Write Cycle								
t _{WC}	Write Cycle Time	200		300		450		nsec
t _{AW}	Address to Write Setup Time	0		0		0		nsec
t _W	Write Pulse Width	120		150		200		nsec
t _{WR}	Write Release Time	0		0		0		nsec
t _{OTW}	Write to Output Off	0	60	0	80	0	100	nsec
t _{DW}	Data to Write Overlap	120		150		200		nsec
t _{DH}	Data Hold	0		0		0		nsec

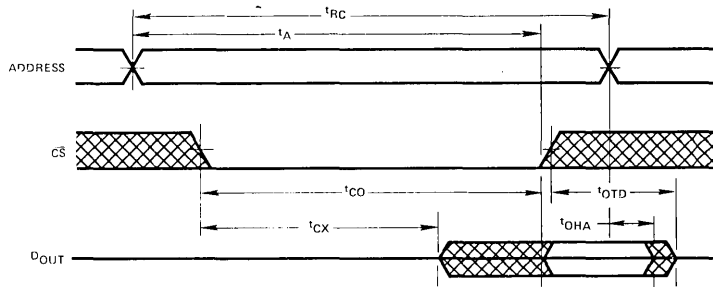
A.C. Test Conditions

Input Pulse Levels 0.8V to 2.0V
 Input Rise and Fall Time 10 n sec
 Timing Measurement Levels: Input 1.5V
 Output 0.8 and 2.0V
 Output Load 1TTL Gate and 100pF

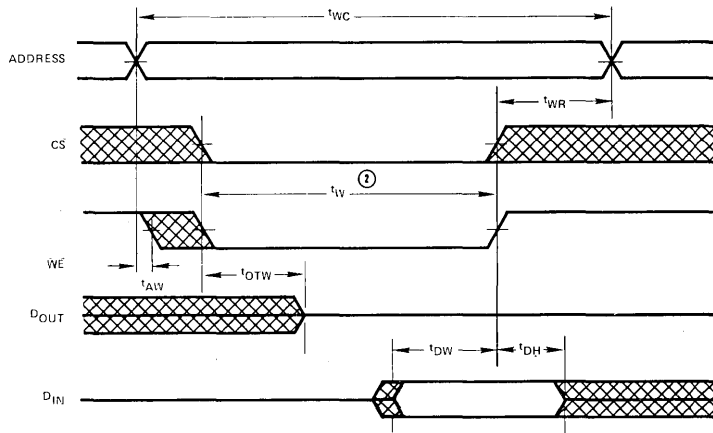
RAMs

TIMING DIAGRAMS

Read Cycle ①



Write Cycle



NOTES:

 ① \overline{WE} is high for a Read Cycle

 ② t_W is measured from the latter of \overline{CS} or \overline{WE} going low to the earlier of \overline{CS} or \overline{WE} going high.

DATA STORAGE

When \overline{WE} is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as \overline{WE} remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

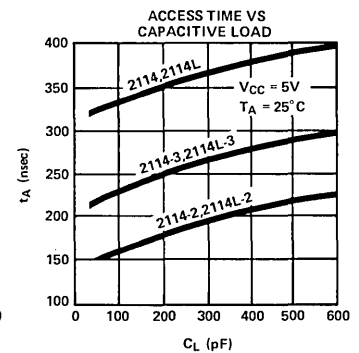
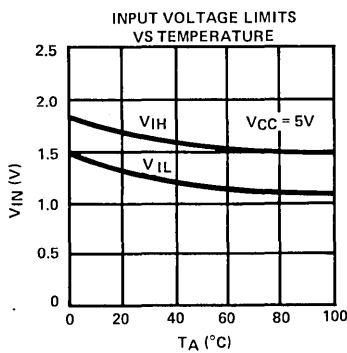
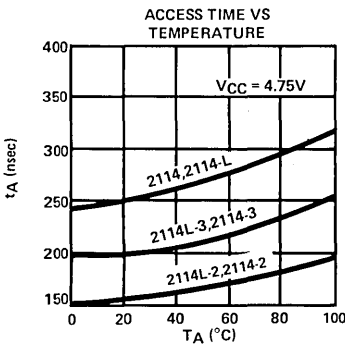
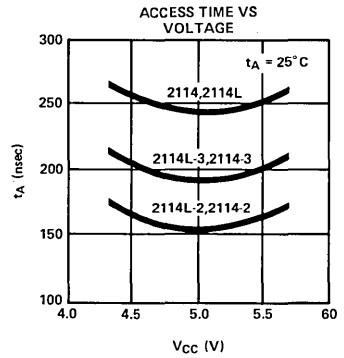
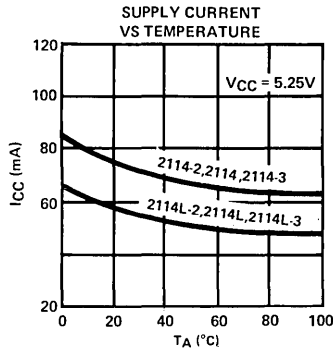
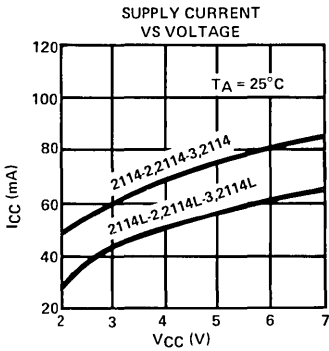
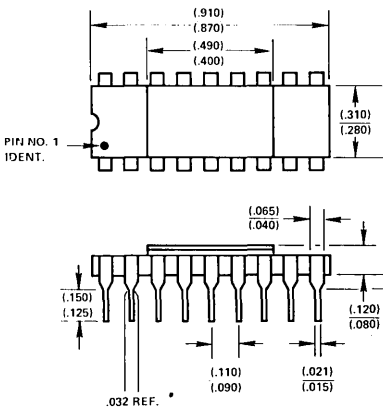
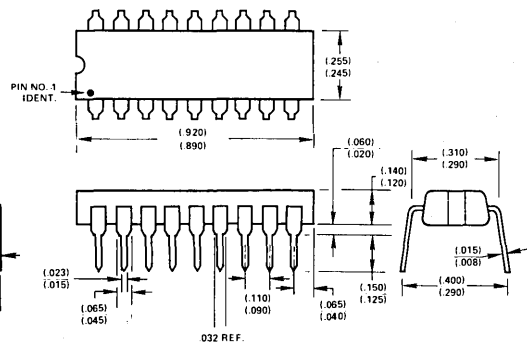
Data storage also cannot be affected by \overline{WE} ; Addresses, or the I/O ports as long as \overline{CS} is high. Either \overline{CS} or \overline{WE} or both can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during Write time — defined as the overlap of \overline{CS} low and

\overline{WE} low. The addresses must be properly established during the entire Write time plus t_{WR} .

Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.

RAMS

TYPICAL CHARACTERISTICS

PACKAGE DIAGRAM
CERAMIC PACKAGE

MOLDED PACKAGE




Military 1024x4 Static Random Access Memory

Extended Temperature Range (-55°C to +125°C)

SYM2114

MEMORY PRODUCTS

RAMS

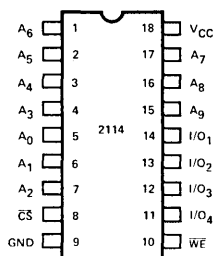
- 300 ns Maximum Access
- Low Operating Power Dissipation
0.1 mW/Bit
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible:
All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package
- Operation over full military temperature range. (-55°C to +125°C)

The SYM2114 is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 1 TTL load.

The SYM2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select (CS) input allows easy selection of an individual device when outputs are or-tied.

The SYM2114 is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology — a technology providing excellent performance characteristics as well as improved protection against contamination.

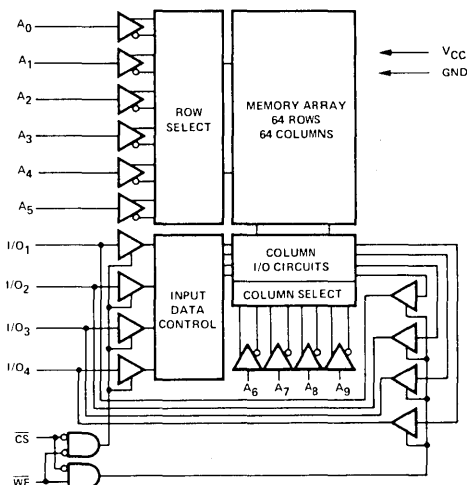
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYM2114	Ceramic	450nsec	100mA	-55°C to 125°C
SYM2114-3	Ceramic	300nsec	100mA	-55°C to 125°C

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-0.5V to +7 V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$ (Unless Otherwise Specified)

Symbol	Parameter	2114-3, 2114		Unit	Conditions
		Min	Max		
I _{LI}	Input Load Current (All input pins)		10	µA	V _{IN} = 0 to 5.5V
I _{LO}	I/O Leakage Current		10	µA	$\overline{CS} = 2.0V$, V _{I/O} = 0.4V to V _{CC}
I _{CC1}	Power Supply Current		70	mA	V _{CC} 5.5V, I _{I/O} = 0 mA, T _A = 25°C
I _{CC2}	Power Supply Current		100	mA	V _{CC} = 5.5V, I _{I/O} = 0 mA, T _A = -55°C
V _{IL}	Input Low Voltage	-0.5	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC}	V	
V _{OL}	Output Low Voltage		0.4	V	I _{OL} = 2.0 mA
V _{OH}	Output High Voltage	2.4	V _{CC}	V	I _{OH} = 200µA

CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$

Symbol	Test	Typ	Max	Units
C _{I/O}	Input/Output Capacitance		5	pF
C _{IN}	Input Capacitance		5	pF

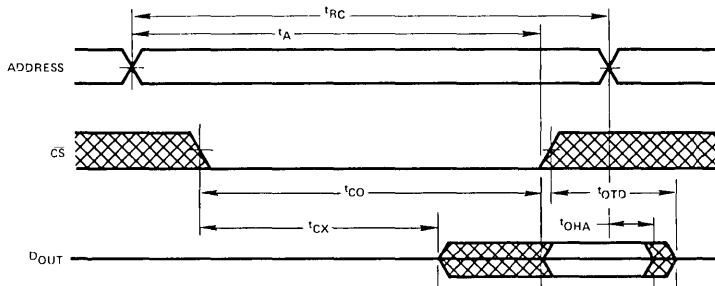
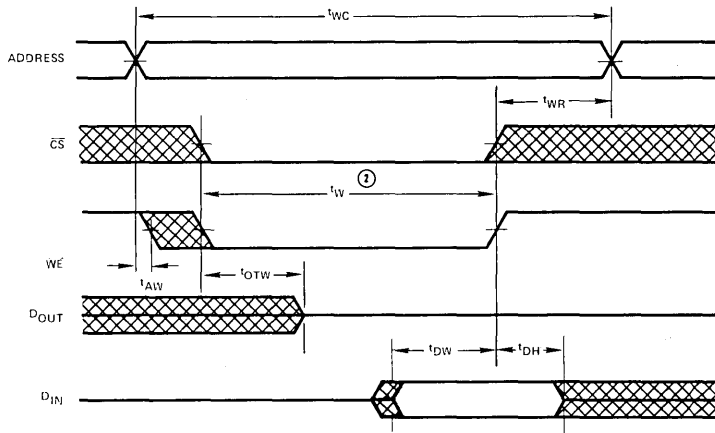
NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$ (Unless Otherwise Specified)

SYMBOL	PARAMETER	2114-3		2114		UNIT
		MIN	MAX	MIN	MAX	
READ CYCLE						
t _{RC}	Read Cycle Time	300		450		nsec
t _A	Access Time		300		450	nsec
t _{CO}	Chip Select to Output Valid		100		120	nsec
t _{CX}	Chip Select to Output Enabled	20		20		nsec
t _{OTD}	Chip Deselect to Output Off	0	80	0	100	nsec
t _{OHA}	Output Hold From Address Change	50		50		nsec
WRITE CYCLE						
t _{WC}	Write Cycle Time	300		450		nsec
t _{AW}	Address to Write Setup Time	0		0		nsec
t _W	Write Pulse Width	150		200		nsec
t _{WR}	Write Release Time	0		0		nsec
t _{OTW}	Write to Output Off	0	80	0	100	nsec
t _{DW}	Data to Write Overlap	150		200		nsec
t _{DH}	Data Hold	0		0		nsec

A.C. Test Conditions

Input Pulse Levels	0.8V to 2.0V
Input Rise and Fall Time	10 n sec
Timing Measurement Levels: Input	1.5V
Output	0.8 and 2.0V
Output Load	1TTL Gate and 100pF

TIMING DIAGRAMS
Read Cycle ^①

Write Cycle

NOTES:

- ① \overline{WE} is high for a Read Cycle
- ② t_W is measured from the latter of \overline{CS} or \overline{WE} going low to the earlier of \overline{CS} or \overline{WE} going high.

DATA STORAGE

When \overline{WE} is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as \overline{WE} remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

Data storage also cannot be affected by \overline{WE} , Addresses, or the I/O ports as long as \overline{CS} is high. Either \overline{CS} or \overline{WE} or both can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during Write time — defined as the overlap of \overline{CS} low and

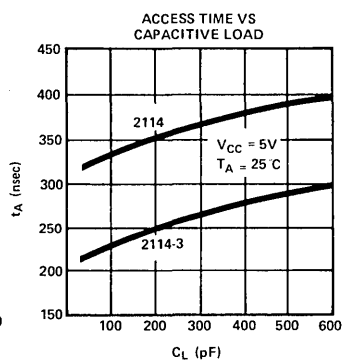
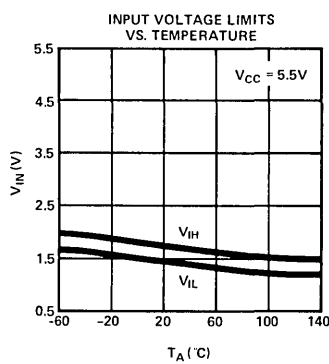
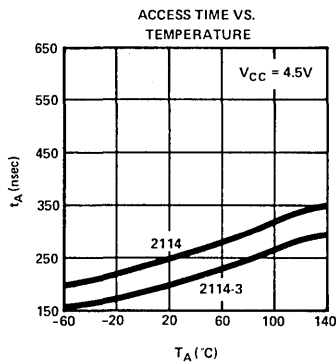
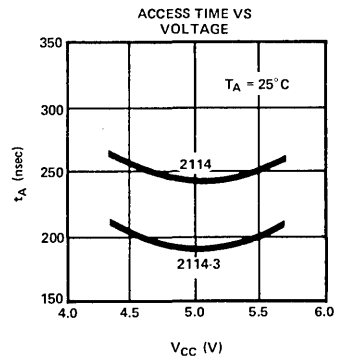
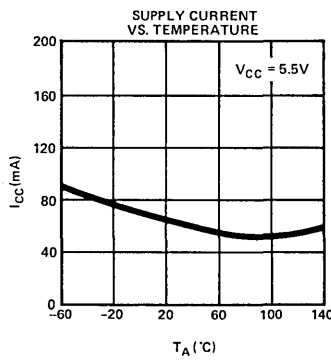
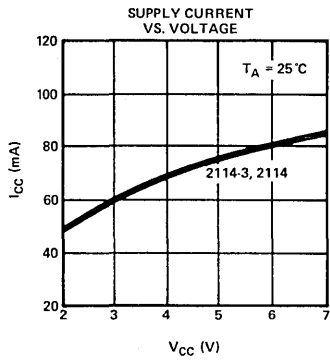
\overline{WE} low. The addresses must be properly established during the entire Write time plus t_{WR} .

Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.

RAMS

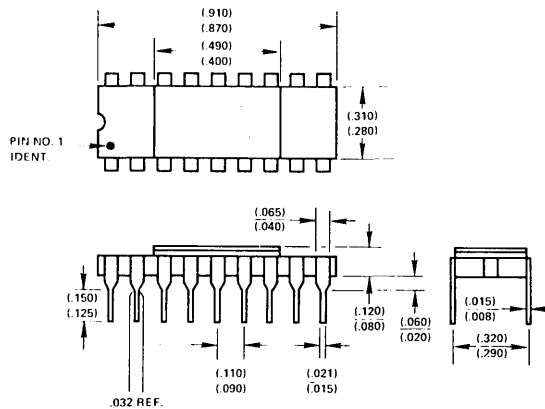


TYPICAL CHARACTERISTICS



PACKAGE DIAGRAM

CERAMIC PACKAGE





1024x4 Static Random Access Memory

Low Power Standby

SY2114LV

MEMORY PRODUCTS

RAMS

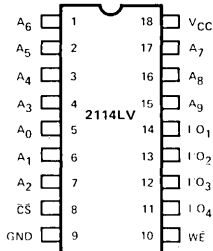
- 200 ns Maximum Access
- Low Power: 0.1 mW/Bit Operating
0.03 mW/Bit Standby
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single Supply: +5V Operating
+2.5V Standby
- Totally TTL Compatible:
All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

The SY2114LV is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. These advanced processing techniques allow the SY2114LV to maintain memory with V_{CC} reduced to 2.5V. This reduces standby power by 60% and simplifies the design of battery back-up systems. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 2 TTL loads.

The SY2114LV is designed for memory applications where high performance, low power, large bit storage and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select (CS) input allows easy selection of an individual device when outputs are or-tied.

The SY2114LV is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology — a technology providing excellent performance characteristics as well as improved protection against contamination.

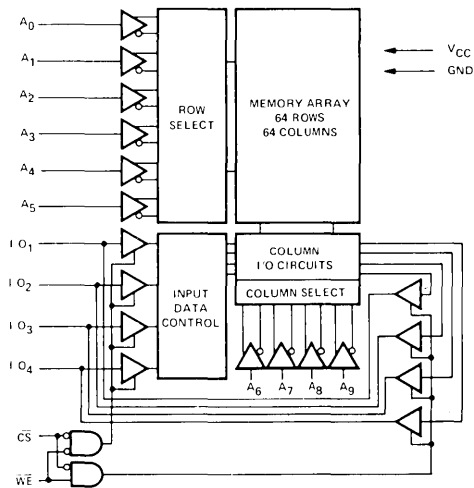
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYC2114LV	Ceramic	450nsec	70mA	0°C to +70°C
SYP2114LV	Molded	450nsec	70mA	0°C to +70°C
SYC2114LV-3	Ceramic	300nsec	70mA	0°C to +70°C
SYP2114LV-3	Molded	300nsec	70mA	0°C to +70°C
SYC2114LV-2	Ceramic	200nsec	70mA	0°C to +70°C
SYP2114LV-2	Molded	200nsec	70mA	0°C to +70°C

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-0.5V to +7V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS TA = 0°C to +70°C, VCC = 5V ± 5% (Unless otherwise specified)

Symbol	Parameter	2114LV-2, 2114LV-3, 2114LV		Unit	Conditions
		Min	Max		
ILI	Input Load Current (All input pins)		10	μA	VIN = 0 to 5.25V
ILO	I/O Leakage Current		10	μA	CS̄ = 2.0V, VI/O = 0.4V to VCC
ICC1	Power Supply Current		65	mA	VCC = 5.25V, I1/O = 0 mA, TA = 25°C
ICC2	Power Supply Current		70	mA	VCC = 5.25V, I1/O = 0 mA, TA = 0°C
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	V	
VOL	Output Low Voltage	2.4	0.4	V	IOL = 3.2 mA
VOH	Output High Voltage		VCC	V	IOH = -1.0 mA

CAPACITANCE TA = 25°C, f = 1.0 MHz

Symbol	Test	Typ	Max	Units
CI/O	Input/Output Capacitance		5	pF
CIN	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 5% (Unless Otherwise Specified)

Symbol	Parameter	2114LV-2		2114LV-3		2114LV		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	200		300		450		nsec
tA	Access Time		200		300		450	nsec
tCO	Chip Select to Output Valid		70		100		120	nsec
tCX	Chip Select to Output Enabled	20		20		20		nsec
tOTD	Chip Deselect to Output Off	0	60	0	80	0	100	nsec
tOHA	Output Hold From Address Change	50		50		50		nsec
Write Cycle								
tWC	Write Cycle Time	200		300		450		nsec
tAW	Address to Write Setup Time	0		0		0		nsec
tW	Write Pulse Width	120		150		200		nsec
tWR	Write Release Time	0		0		0		nsec
tOTW	Write to Output Off	0	60	0	80	0	100	nsec
tDW	Data to Write Overlap	120		150		200		nsec
tDH	Data Hold	0		0		0		nsec

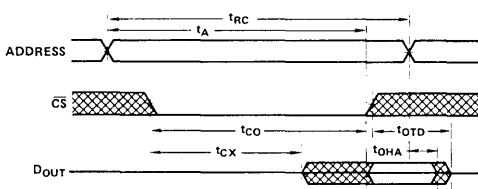
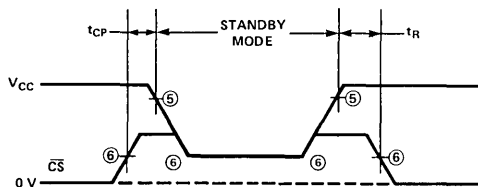
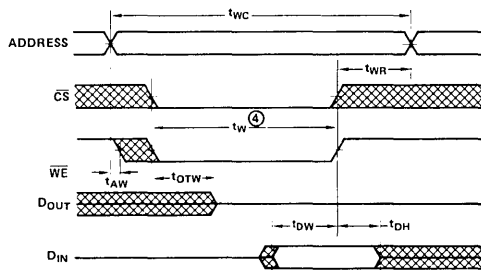
A.C. Test Conditions

Input Pulse Levels	0.8V to 2.0V
Input Rise and Fall Time	10 nsec
Timing Measurement Levels: Input	1.5V
Output	0.8 and 2.0V
Output Load	1TTL Gate and 100pF

RAMs

STANDBY CHARACTERISTICS
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	2.5		V	$2.5\text{V} \leq V_{PD} \leq V_{CC}$ Max. All Inputs = $V_{PD} = 2.5\text{V}$
$V_{CSS(2)}$	\overline{CS} Bias in Standby	2.5		V	
I_{PD}	Standby Current Drain		50	mA	
t_{CP}	Chip Deselect to Standby Time	0		ns	
t_R	Standby Recovery Time	500		ns	

TIMING DIAGRAMS
Read Cycle⁽³⁾

Standby Operation

Write Cycle

NOTES

1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.5V, then \overline{CS} must be held at 2.5V Min.
3. \overline{WE} is high for a Read Cycle.
4. t_W is measured from the latter of \overline{CS} or \overline{WE} going low to the earlier of \overline{CS} or \overline{WE} going high.
5. 4.75 Volts
6. 2.5 Volts

DATA STORAGE

When \overline{WE} is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as \overline{WE} remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

Data storage also cannot be affected by \overline{WE} , Addresses, or the I/O ports as long as \overline{CS} is high. Either \overline{CS} or \overline{WE} or both can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during Write time – defined as the overlap of \overline{CS} low and

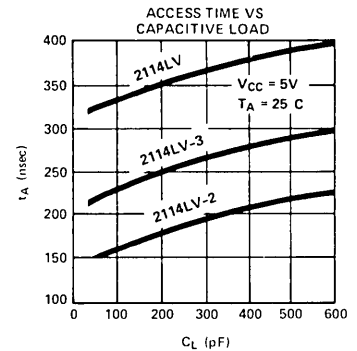
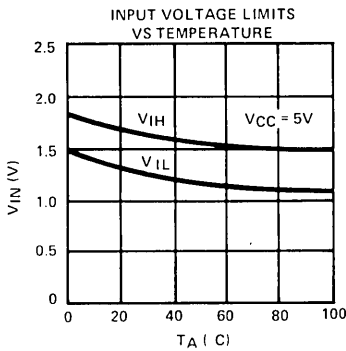
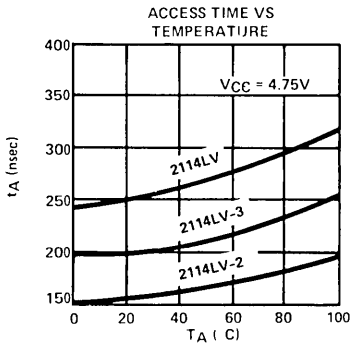
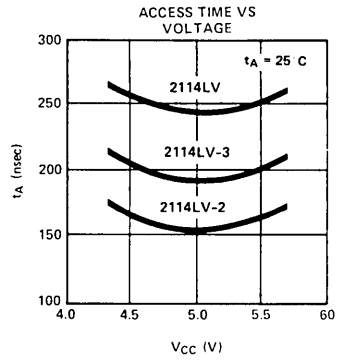
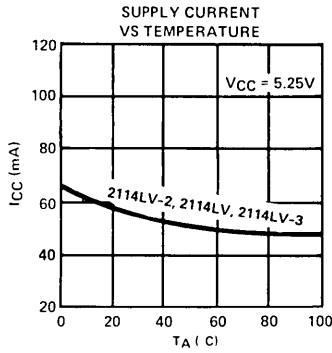
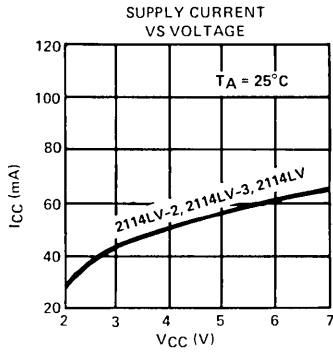
\overline{WE} low. The addresses must be properly established during the entire Write time plus t_{WR} .

Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.



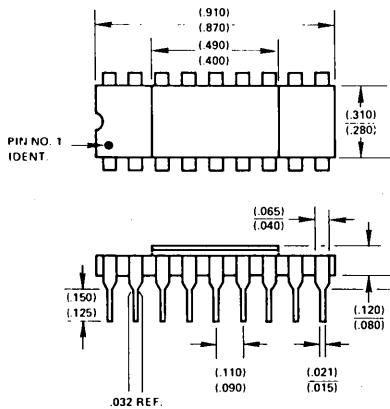
RAMs

TYPICAL CHARACTERISTICS

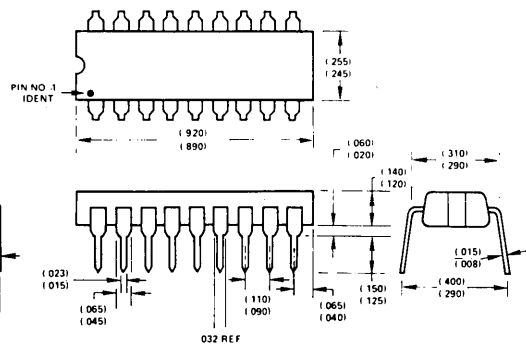


PACKAGE DIAGRAM

CERAMIC PACKAGE



MOLDED PACKAGE





1024x4 Static Random Access Memory

SY2142

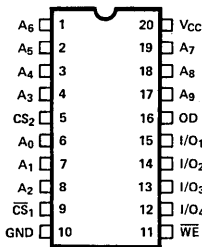
MEMORY PRODUCTS

RAMS

- 200ns Maximum Access
- Low Operating Power Dissipation
0.1mW/Bit
- No Clocks or Strokes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible:
All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400mv Noise Immunity
- High Density 20 Pin Package
- Two Chip Selects and Output Disable
Functions Simplify Memory Expansion

The 2142 is a 4096-bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of bus oriented systems, and the outputs can drive 2 TTL loads.

PIN CONFIGURATION



ORDERING INFORMATION

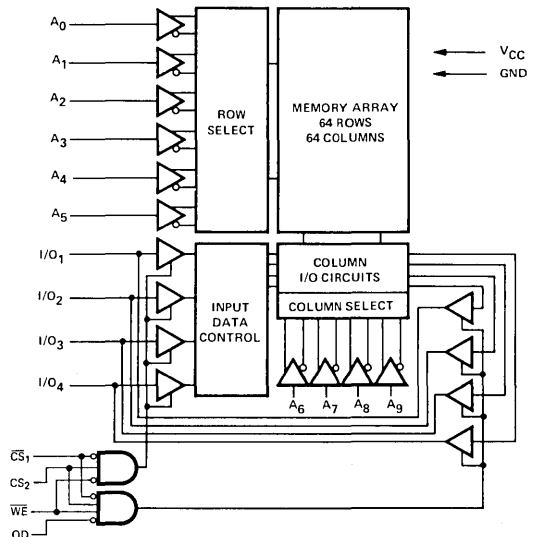
Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYC2142	Ceramic	450nsec	100mAmp	0°C to 70°C
SYP2142	Molded	450nsec	100mAmp	0°C to 70°C
SYC2142-3	Ceramic	300nsec	100mAmp	0°C to 70°C
SYP2142-3	Molded	300nsec	100mAmp	0°C to 70°C
SYC2142L	Ceramic	450nsec	70mAmp	0°C to 70°C
SYP2142L	Molded	450nsec	70mAmp	0°C to 70°C
SYC2142L-3	Ceramic	300nsec	70mAmp	0°C to 70°C
SYP2142L-3	Molded	300nsec	70mAmp	0°C to 70°C
SYC2142-2	Ceramic	200nsec	100mAmp	0°C to 70°C
SYP2142-2	Molded	200nsec	100mAmp	0°C to 70°C
SYC2142L-2	Ceramic	200nsec	70mAmp	0°C to 70°C
SYP2142L-2	Molded	200nsec	70mAmp	0°C to 70°C

The SY2142 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply.

Two Chip Selects (\overline{CS}_1 and CS_2) are provided to simplify systems where memory expansion is implemented by OR-tying several 2142's. Also an Output Disable directly controls the output stages.

The SY2142 is packaged in a 20-pin DIP and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology — a technology providing excellent performance characteristics as well as protection against contamination allowing the use of low cost packaging techniques.

BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-0.5V to +7V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$ (Unless Otherwise Specified)

Symbol	Parameter	2142, 2142-2 2142-3		2142L, 2142L-2 2142L-3		Unit	Conditions
		Min	Max	Min	Max		
I _{LI}	Input Load Current (All input pins)		10		10	μA	V _{IN} = 0 to 5.25V
I _{LO}	I/O Leakage Current		10		10	μA	$\overline{CS} = 2.0V$, V _{I/O} = 0.4V to V _{CC}
I _{CC1}	Power Supply Current		95		65	mA	V _{CC} = 5.25V, I _{I/O} = 0 mA, T _A = 25°C
I _{CC2}	Power Supply Current		100		70	mA	V _{CC} = 5.25V, I _{I/O} = 0 mA, T _A = 0°C
V _{IL}	Input Low Voltage	-0.5	0.8	-0.5	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC}	2.0	V _{CC}	V	
V _{OL}	Output Low Voltage		0.4		0.4	V	I _{OL} = 3.2 mA
V _{OH}	Output High Voltage	2.4	V _{CC}	2.4	V _{CC}	V	I _{OH} = -1.0 mA

CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$

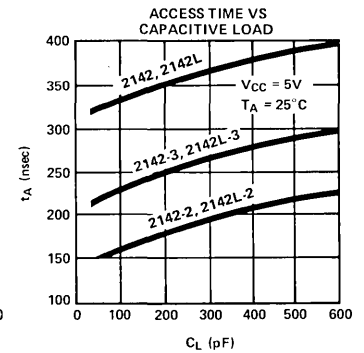
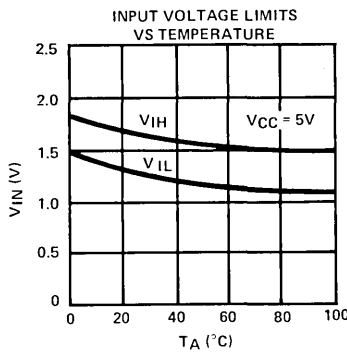
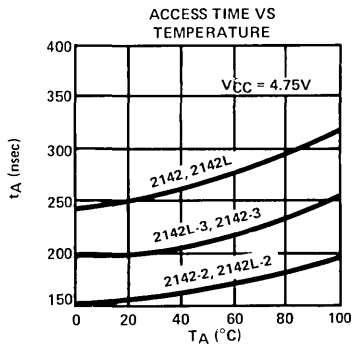
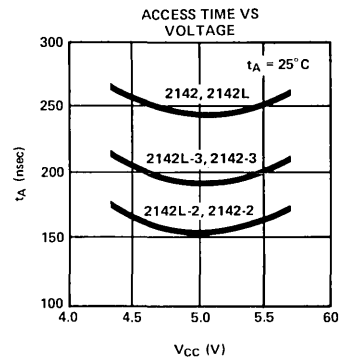
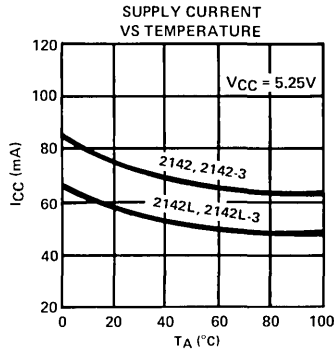
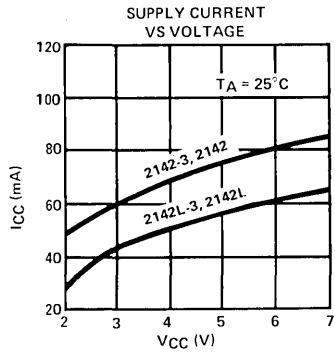
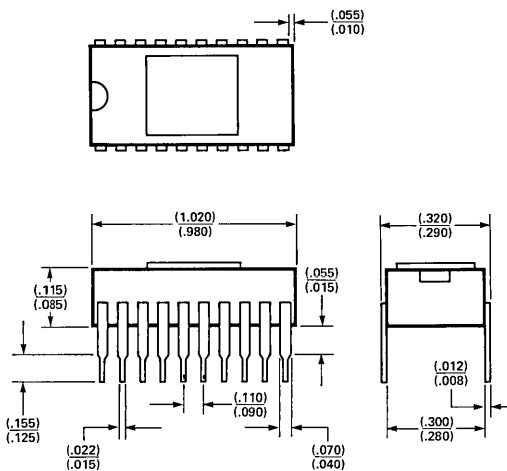
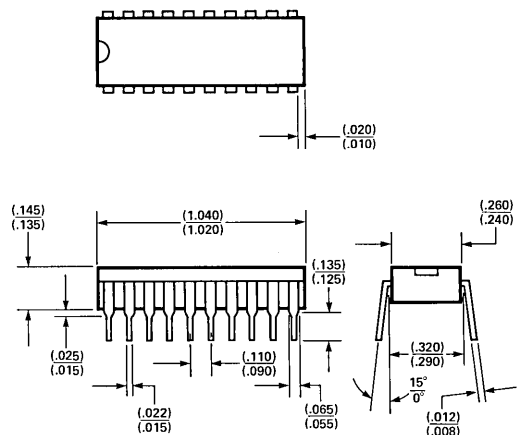
Symbol	Test	Typ	Max	Units
C _{I/O}	Input/Output Capacitance		5	pF
C _{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$ (Unless Otherwise Specified)

Symbol	Parameter	2142-2, 2142L-2		2142-3, 2142L-3		2142, 2142L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	200		300		450		ns
t _A	Access Time		200		300		450	ns
t _{OD}	Output Enable to Output Valid		70		100		120	ns
t _{ODX}	Output Enable to Output Active	20		20		20		ns
t _{CO}	Chip Selection to Output Valid		70		100		120	ns
t _{CX}	Chip Selection to Output Active	20		20		20		ns
t _{OTD}	Output 3-state from Disable	0	60	0	80	0	100	ns
t _{OHA}	Output Hold from Address Change	50		50		50		ns
WRITE CYCLE								
t _{WC}	Write Cycle Time	200		300		450		ns
t _{AW}	Address to Write Setup Time	0		0		0		ns
t _W	Write Pulse Width	120		150		200		ns
t _{WR}	Write Release Time	0		0		0		ns
t _{OTD}	Output 3-state from Disable	0	60		80		100	ns
t _{DW}	Data to Write Time Overlap	120		150		200		ns
t _{DH}	Data Hold from Write Time	0		0		0		ns

See following page for A.C. Test Conditions

TYPICAL CHARACTERISTICS

PACKAGE DIAGRAMS
20 PIN CERAMIC DIP

20 PIN MOLDED DIP




1024x4 Static Random Access Memory

Low Power Standby

SY2142LV

MEMORY PRODUCTS

- 200 ns Maximum Access
- Low Power: 0.1 mW/Bit Operating
0.03 mW/Bit Standby
- No Clocks or Strokes Required
- Identical Cycle and Access Times
- Single Supply: +5V Operating
+2.5V Standby
- Totally TTL Compatible:
All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package
- Two Chip Selects and Output Disable
Functions Simplify Memory Expansion

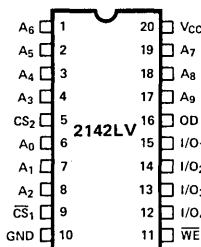
The SY2142LV is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. These advanced processing techniques allow the SY2142LV to maintain memory with V_{CC} reduced to 2.5V. This reduces standby power by 60% and simplifies the design of battery back-up systems. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 2 TTL loads.

The SY2142LV is designed for memory applications where high performance, low power, large bit storage and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply.

Two Chip Selects (\overline{CS}_1 and CS_2) are provided to simplify systems where memory expansion is implemented by OR-tying several 2142LVs. Also an Output Disable directly controls the output stages.

The SY2142LV is packaged in a 20-pin DIP and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology — a technology providing excellent performance characteristics as well as protection against contamination allowing the use of low cost packaging techniques.

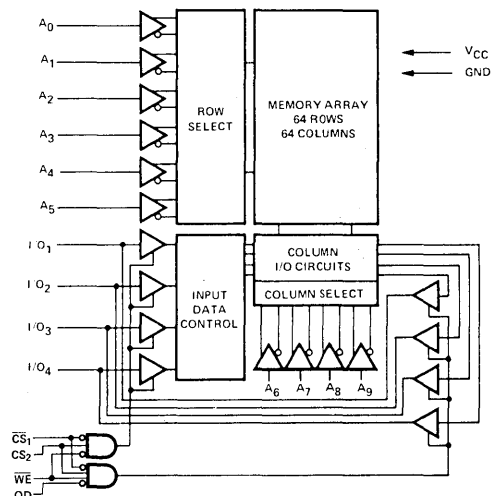
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYC2142LV	Ceramic	450nsec	70mA	0°C to +70°C
SYP2142LV	Plastic	450nsec	70mA	0°C to +70°C
SYC2142LV-3	Ceramic	300nsec	70mA	0°C to +70°C
SYP2142LV-3	Plastic	300nsec	70mA	0°C to +70°C
SYC2142LV-2	Ceramic	200nsec	70mA	0°C to +70°C
SYP2142LV-2	Plastic	200nsec	70mA	0°C to +70°C

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-0.5V to +7 V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS TA = 0°C to +70°C, VCC = 5V ± 5% (Unless otherwise specified)

Symbol	Parameter	2142LV-2 2142LV-3, 2142LV		Unit	Conditions
		Min	Max		
ILI	Input Load Current (All input pins)		10	μA	VIN = 0 to 5.25V
ILO	I/O Leakage Current		10	μA	CS = 2.0V, V1/O = 0.4V to VCC
ICC1	Power Supply Current		65	mA	VCC = 5.25V, I1/O = 0 mA, TA = 25°C
ICC2	Power Supply Current		70	mA	VCC = 5.25V, I1/O = 0 mA, TA = 0°C
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	V	
VOL	Output Low Voltage	2.4	0.4	V	IOL = 3.2 mA
VOH	Output High Voltage		VCC	V	IOH = -1.0 mA

CAPACITANCE TA = 25°C, f = 1.0 MHz

Symbol	Test	Typ	Max	Units
C1/O	Input/Output Capacitance		5	pF
CIN	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ±5% (Unless Otherwise Specified)

Symbol	Parameter	2142LV-2		2142LV-3		2142LV		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	200		300		450		nsec
tA	Access Time		200		300		450	nsec
tOD	Output Enable to Output Valid		70		100		120	nsec
tODX	Output Enable to Output Active	20		20		20		nsec
tCO	Chip Select to Output Valid		70		100		120	nsec
tCX	Chip Select to Output Enabled	20		20		20		nsec
tOTD	Chip Deselect to Output Off	0	60	0	80	0	100	nsec
tOHA	Output Hold From Address Change	50		50		50		nsec
Write Cycle								
tWC	Write Cycle Time	200		300		450		nsec
tAW	Address to Write Setup Time	0		0		0		nsec
tW	Write Pulse Width	120		150		200		nsec
tWR	Write Release Time	0		0		0		nsec
tOTW	Write to Output Off	0	60	0	80	0	100	nsec
tDW	Data to Write Overlap	120		150		200		nsec
tDH	Data Hold	0		0		0		nsec

A.C. Test Conditions

Input Pulse Levels 0.8V to 2.0V
Input Rise and Fall Time 10 n sec

Timing Measurement Levels: Input 1.5V
Output . . . 0.8 and 2.0V
Output Load 1TTL Gate and 100pF

RAMs



RAMS

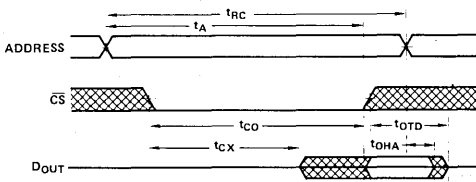
STANDBY CHARACTERISTICS

T_A = 0°C to 70°C

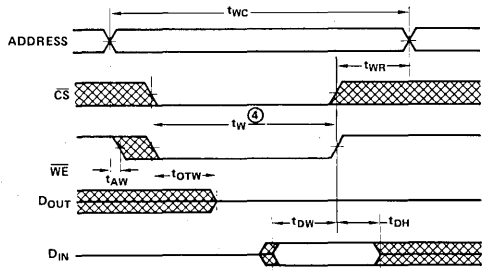
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V _{PD}	V _{CC} in Standby	2.5		V	
V _{CSS(2)}	\overline{CS} Bias in Standby	2.5		V	2.5V ≤ V _{PD} ≤ V _{CC} Max.
I _{PD}	Standby Current Drain		50	mA	All Inputs = V _{PD} = 2.5V
t _{CP}	Chip Deselect to Standby Time	0		ns	
t _R	Standby Recovery Time	500		ns	

TIMING DIAGRAMS

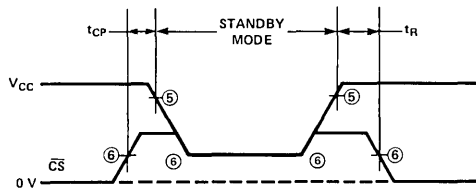
Read Cycle⁽³⁾



Write Cycle



Standby Operation



NOTES

1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.5V, then \overline{CS} must be held at 2.5V Min.
3. \overline{WE} is high for a Read Cycle.
4. t_W is measured from the latter of \overline{CS} or \overline{WE} going low to the earlier of \overline{CS} or \overline{WE} going high.
5. 4.75 Volts
6. 2.5 Volts

DATA STORAGE

When \overline{WE} is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as \overline{WE} remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

Data storage also cannot be affected by \overline{WE} , Addresses, or the I/O ports as long as \overline{CS} is high. Either \overline{CS} or \overline{WE} or both can prevent extraneous writing due to signal transitions.

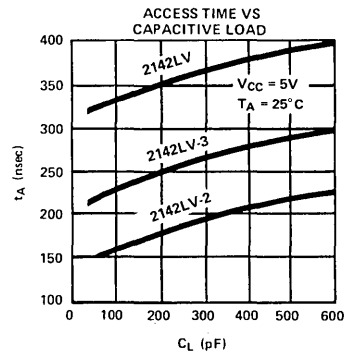
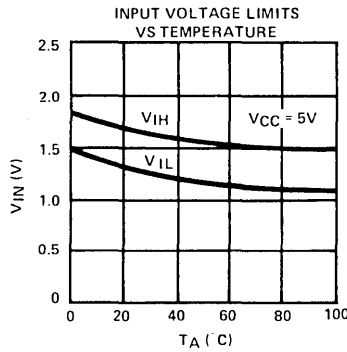
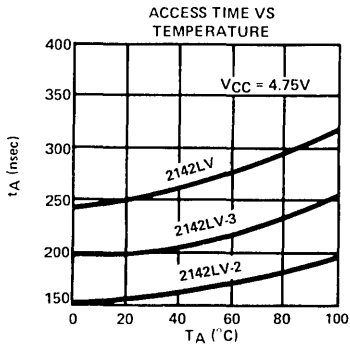
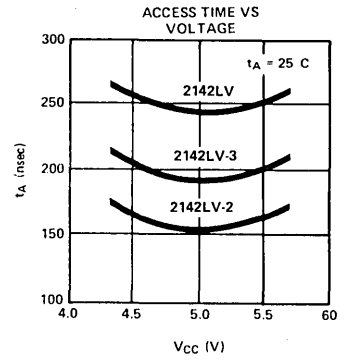
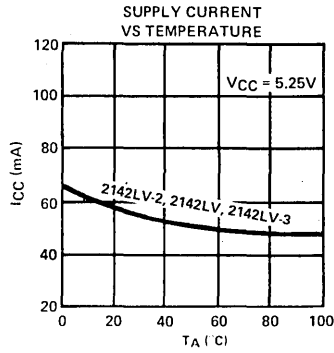
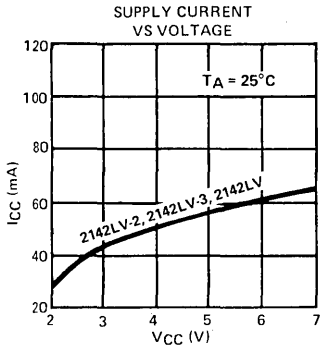
Data within the array can only be changed during Write time – defined as the overlap of \overline{CS} low and

\overline{WE} low. The addresses must be properly established during the entire Write time plus t_{WR}.

Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.



TYPICAL CHARACTERISTICS





4096 x 1 Static Random Access Memory

SY2147

MEMORY PRODUCTS

Preliminary

RAMS

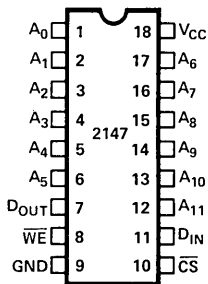
- 55 ns Maximum Access
- No Clocks or Strobes Required
- Automatic \overline{CS} Power Down
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible
All Inputs and Outputs
- Separate Data Input and Output
- High Density 18-Pin Package
- Three-State Output

The Synertek SY2147 is a 4096-Bit Static Random Access Memory organized 4096 words by 1-bit and is fabricated using Synertek's new N-Channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock on refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

The SY2147 offers an automatic power down feature. Power down is controlled by the Chip Select input. When Chip Select (\overline{CS}) goes high, thus de-selecting the SY2147, the device will automatically power down and remain in a standby power mode as long as \overline{CS} remain high. This unique feature provides system level power savings as much as 80%.

The SY2147 is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

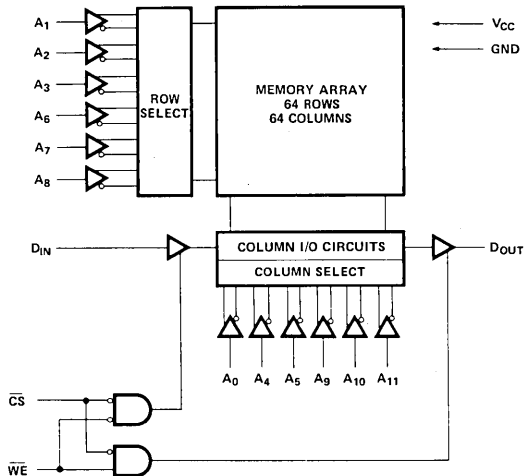
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Supply Current (Max)	Standby Current (Max)
SYC2147-3	Ceramic	55nsec	180mA	30mA
SYC2147	Ceramic	70nsec	160mA	20mA
SYC2147L	Ceramic	70nsec	140mA	10mA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias -10°C to 80°C
 Storage Temperature -65°C to 150°C
 Voltage on Any Pin with
 Respect to Ground -0.5V to +7V
 Power Dissipation 1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$ (Unless otherwise specified)

Symbol	Parameter	2147-3		2147		2147L		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{LI}	Input Load Current (All input pins)		10		10		10	μA	$V_{CC} = \text{Max}$, $V_{IN} = \text{Gnd to } V_{CC}$
I _{LO}	Output Leakage Current		50		50		50	μA	$\overline{CS} = V_{IH}$, $V_{CC} = \text{Max}$ $V_{OUT} = \text{Gnd to } 4.5\text{V}$
I _{CC}	Power Supply Current		170 180		150 160		135 140	mA mA	$T_A = 25^\circ\text{C}$ $V_{CC} = \text{Max}$, $\overline{CS} = V_{IL}$ $T_A = 0^\circ\text{C}$ Outputs Open
I _{SB}	Standby Current		30		20		10	mA	$V_{CC} = \text{Min to Max}$, $\overline{CS} = V_{IH}$
I _{PO}	Peak Power-on Current		70		50		30	mA	$V_{CC} = \text{Gnd to } V_{CC} \text{ Min}$ $\overline{CS} = \text{Lower of } V_{CC} \text{ or } V_{IH} \text{ Min}$
V _{IL}	Input Low Voltage	-0.3	0.8	-0.3	0.8	-0.3	0.8	V	
V _{IH}	Input High Voltage	2.0	6.0	2.0	6.0	2.0	6.0	V	
V _{OL}	Output Low Voltage		0.4		0.4		0.4	V	I _{OL} = 8mA
V _{OH}	Output High Voltage	2.4		2.4		2.4		V	I _{OH} = -4.0mA

CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$

Symbol	Test	Typ.	Max.	Unit
C _{OUT}	Output Capacitance		7	pF
C _{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$ (Unless otherwise specified)

READ CYCLE

Symbol	Parameter	2147-3		2147,2147L		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
t _{RC}	Read Cycle Time	55		70		ns	
t _{AA}	Address Access Time		55		70	ns	
t _{ACS1}	Chip Select Access Time		55		70	ns	Note 1
t _{ACS2}	Chip Select Access Time		65		80	ns	Note 2
t _{OH}	Output Hold from Address Change	5		5		ns	
t _{LZ}	Chip Selection to Output in Low Z	10		10		ns	
t _{HZ}	Chip Deselection to Output in High Z	0	40	0	40	ns	
t _{PU}	Chip Selection to Power Up Time	0		0		ns	
t _{PD}	Chip Deselection to Power Down Time		30		30	ns	

WRITE CYCLE

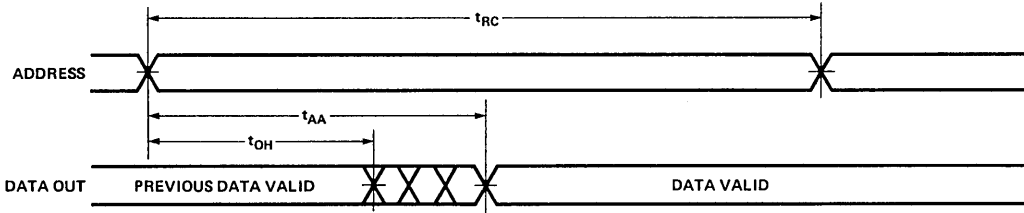
t _{WC}	Write Cycle Time	55		70		ns	
t _{CW}	Chip Selection to End of Write	45		55		ns	
t _{AW}	Address Valid to End of Write	45		55		ns	
t _{AS}	Address Setup Time	0		0		ns	
t _{WP}	Write Pulse Width	35		40		ns	
t _{WR}	Write Recovery Time	10		15		ns	
t _{DW}	Data Valid to End of Write	25		30		ns	
t _{DH}	Data Hold Time	10		10		ns	
t _{WZ}	Write Enabled to Output in High Z	0	30	0	35	ns	
t _{OW}	Output Active from End of Write	0		0		ns	

(See following page for notes)

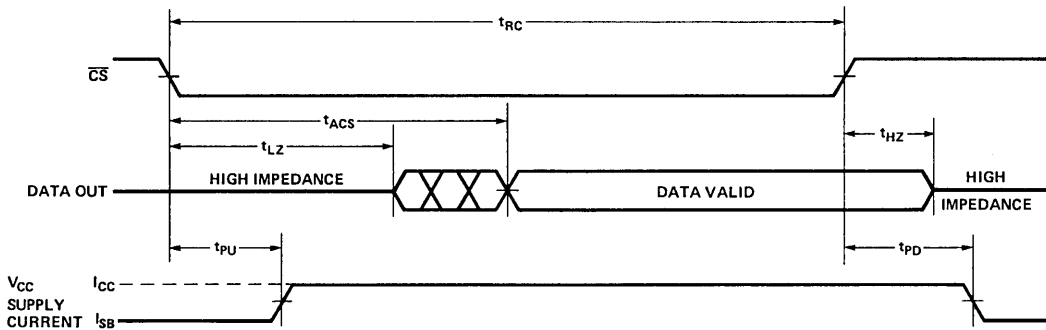


TIMING DIAGRAMS

READ CYCLE NO. 1 [3,4]

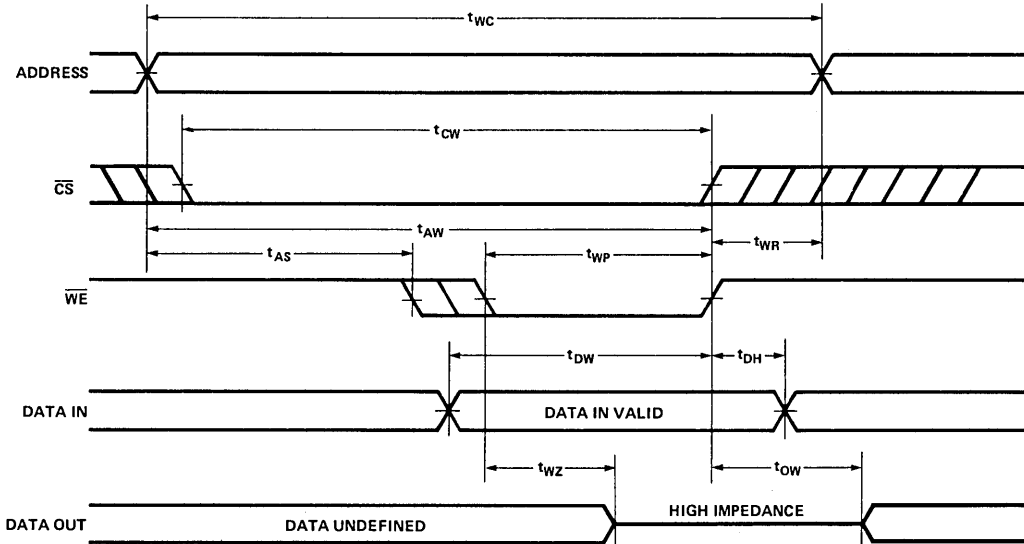


READ CYCLE NO. 2 [3,5]



- NOTES:
1. Chip deselected for greater than 55ns prior to selection.
 2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
 3. WE is high for Read Cycles.
 4. Device is continuously selected, CS-bar = V_{IL}.
 5. Addresses valid prior to or coincident with CS-bar transition low.

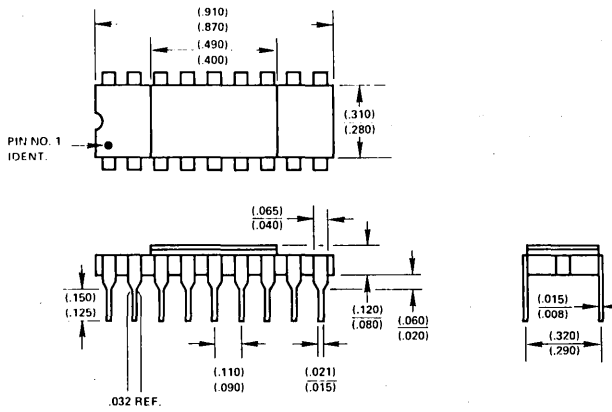
WRITE CYCLE



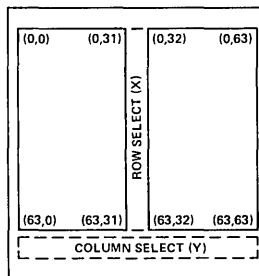


PACKAGE DIAGRAM

CERAMIC PACKAGE



BIT MAPPING INFORMATION (X,Y)



ROW ADDRESSES							
MSB							LSB
X ₅	X ₄	X ₃	X ₂	X ₁	X ₀		
A ₃	A ₂	A ₁	A ₆	A ₇	A ₈		

COLUMN ADDRESSES							
MSB							LSB
Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀		
A ₁₀	A ₀	A ₄	A ₉	A ₅	A ₁₁		



CMOS 256 x 4 Static Random Access Memory

SY5101

MEMORY PRODUCTS

RAMS

- Very Low Power — 100mW operating
— 50µW standby
- Pin compatible with SY2101 RAM—operates in same sockets
- Standby operation whenever chip is not selected
- Single +5V power supply
- Power Down (2 volt) memory retention
- Totally TTL compatible—inputs and outputs
- 3-state output

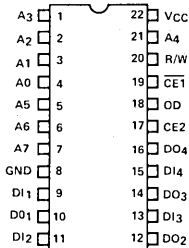
The SY5101, a 256 word x 4 bit CMOS static RAM is a low power pin-for-pin replacement for the industry standard 2101. The device is fabricated with Synertek's silicon gate, ion implanted CMOS process which allows production of very low power, high performance memories.

The 5101 is a completely static design, requiring no refresh or clocks. Low standby power can be achieved without external power down circuits—whenever the device is not enabled (CE2= Logic 0) minimum standby current is drawn from the +5 volt supply. To simplify design of systems using battery backup for non volatility, the SY5101L will also maintain memory storage at supply voltages as low as 2.0 volts.

An output disable input controls the 3-state output to make construction of large memory systems simple. Write and Read cycles are selected by applying the appropriate logic signal to the R/W input with VCC at +5 volts.

The 5101 is intended for use in memory systems using battery backup and/or power down techniques in order to reduce standby power dissipation and in battery powered systems where low operating power is needed. The 5101 will extend battery life in an existing 2101 design and will also permit the elimination of expensive power down circuits.

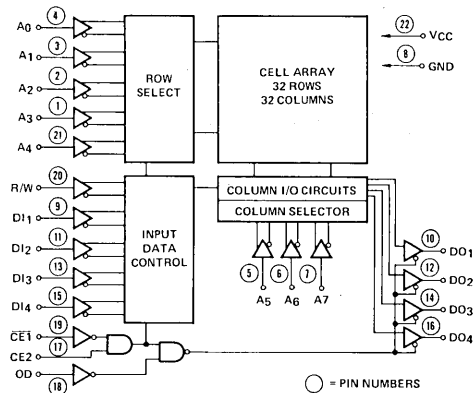
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Access Time	Standby Current µA/Device	2.0 Volt Memory Retention
SYP5101L-3	650nsec	200	Yes
SYC5101L-3	650nsec	200	Yes
SYP5101L	650nsec	10	Yes
SYC5101L	650nsec	10	Yes
SYP5101L-1	450nsec	10	Yes
SYC5101L-1	450nsec	10	Yes
SYP5101-8	800nsec	500	No
SYC5101-8	800nsec	500	No

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias 0°C to 70°C
 Storage Temperature -65°C to +150°C
 *Voltage on Any Pin
 With Respect to Ground -0.3V to V_{CC}+0.3V
 Maximum Power Supply Voltage +7.0V
 Power Dissipation 1 Watt

*Note: During application of power care must be taken to assure that the input voltage on any pin (V_{IN}) is constrained as follows: -0.3V ≤ V_{IN} ≤ V_{CC}+0.3V

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

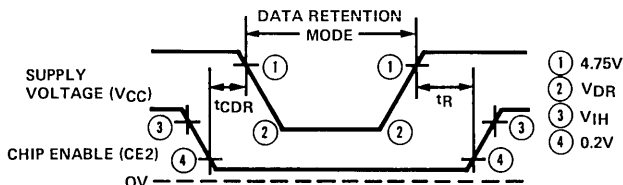
Symbol	Parameter	5101L and 5101L-1 Limits		5101L-3 Limits		5101-8 Limits		Units	Test Conditions
		Min.	Typ.[1] Max.	Min.	Typ.[1] Max.	Min.	Typ.[1] Max.		
I _{L2} [2]	Input Current	.005	1	.005	1	.005	1	μA	V _{IN} = 0.0V to V _{CC}
I _{LO} [2]	Output Leakage Current		1		1		2	μA	$\overline{CE1} = 2.2V, V_{OUT} = 0$ to V _{CC}
I _{CC1}	Operating Current	8	22	8	22	10	25	mA	V _{IN} = V _{CC} , Except $\overline{CE1} \leq 0.65V$, Outputs, Open
I _{CC2}	Operating Current	11	27	11	27	13	30	mA	V _{IN} = 2.2V, Except $\overline{CE1} \leq 0.65V$, Outputs Open
I _{CCL} [2]	Standby Current		10		200		500	μA	CE2 ≤ 0.2V, T _A = 70°C
V _{IL}	Input Low Voltage	-0.3	0.65	-0.3	0.65	-0.3	0.65	V	
V _{IH}	Input High Voltage	2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V	
V _{OL}	Output Low Voltage		0.4		0.4		0.4	V	I _{OL} = 2.0 mA
V _{OH}	Output High Voltage	2.4		2.4		2.4		V	I _{OH} = -1.0 mA

Low V_{CC} Data Retention Characteristics (For 5101L, 5101L-1 and 5101L-3) T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions
V _{DR}	V _{CC} for Data Retention	2.0			V	CE2 ≤ 0.2V V _{DR} = 2.0V, T _A = 70°C V _{DR} = 2.0V, T _A = 70°C
I _{CCDR1}	5101L or 5101L-1 Data Retention Current		0.14	10	μA	
I _{CCDR2}	5101L-3 Data Retention Current		0.70	200	μA	
t _{CDR}	Chip Deselect to Data Retention Time	0			ns	
t _R	Operation Recovery Time	t _{RC} [3]			ns	

NOTES:

- Typical values are T_A = 25°C and nominal supply voltage.
- Current through all inputs and outputs included in I_{CCL} measurement.
- t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform




A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

READ CYCLE

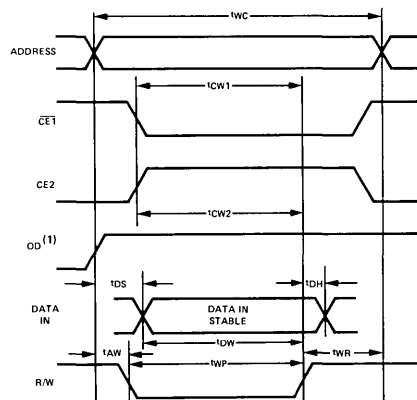
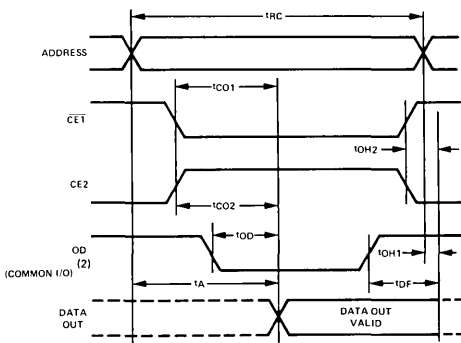
Symbol	Parameter	5101L-1 Limits (ns)		5101L and 5101L-3 Limits (ns)		5101-8 Limits (ns)	
		Min.	Max.	Min.	Max.	Min.	Max.
t_{RC}	Read Cycle	450		650		800	
t_A	Access Time		450		650		800
t_{CO1}	Chip Enable (CE 1) to Output		500		600		800
t_{CO2}	Chip Enable (CE 2) to Output		500		700		850
t_{OD}	Output Disable to Output		250		350		450
t_{DF}	Data Output to High Z State	0	130	0	150	0	200
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0		0		0	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0	

WRITE CYCLE

t_{WC}	Write Cycle	450		650		800
t_{AW}	Write Delay	130		150		200
t_{CW1}	Chip Enable (CE 1) to Write	350		550		650
t_{CW2}	Chip Enable (CE 2) to Write	350		550		650
t_{DW}	Data Setup	250		400		450
t_{DH}	Data Hold	50		100		100
t_{WP}	Write Pulse	250		400		450
t_{WR}	Write Recovery	50		50		100
t_{DS}	Output Disable Setup	130		150		200

READ CYCLE

TIMING DIAGRAMS



NOTES:

1. During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
2. OD may be tied low for separate I/O operation.

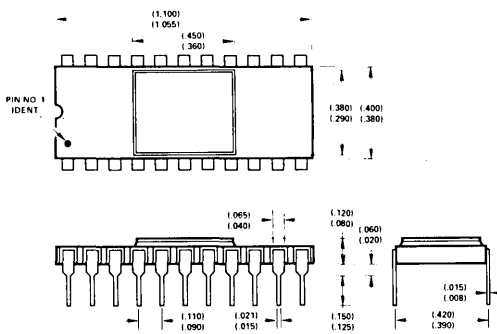
CAPACITANCE³ $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8	pF
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	8	12	pF

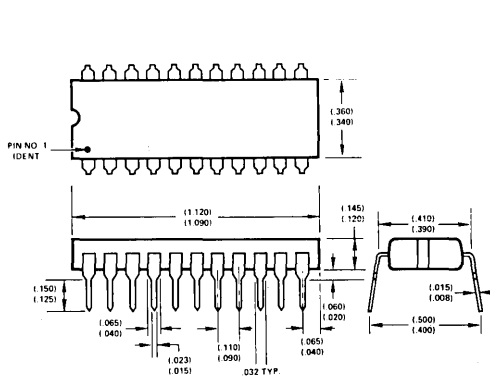
Note 3: This Parameter is periodically sampled and is not 100% tested.

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



Read Only Memories and EPROMs

Read Only Memories and EPROMs



2048 x 8 Static Read Only Memory

SY2316A/B

MEMORY PRODUCTS

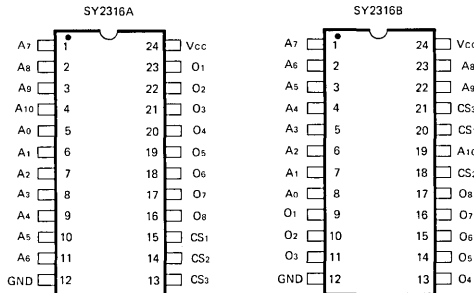
- 2048x8 Bit Organization
- Single +5 Volt Supply
- Metal Mask Programming
- Two Week Prototype Turnaround
- Access Time—550ns /450ns (max.)
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316A — Replacement for Intel 2316A
- SY2316B — Pin Compatible with 2708 EPROM
— Replacement for Two 2708s

The SY2316A and SY2316B high performance read only memories are organized 2048 words by 8 bits with access times of less than 550 ns and 450 ns. These ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

The SY2316A/B operate totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

Designed to replace two 2708 8K EPROMs, the SY2316B can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATION

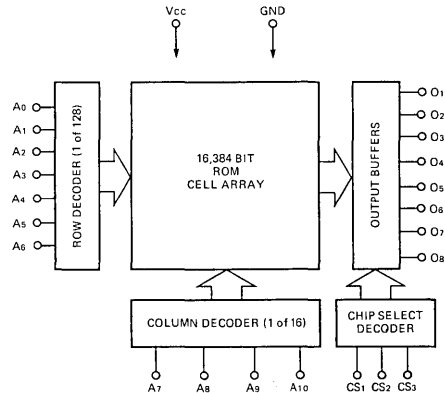


ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC2316A	Ceramic	550ns	0°C to +70°C
SYP2316A	Plastic	550ns	0°C to +70°C
SYC2316B	Ceramic	450ns	0°C to +70°C
SYP2316B	Plastic	450ns	0°C to +70°C

A custom number will be assigned by Synertek.

BLOCK DIAGRAM



ROMs
EPROMs



ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	0° to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

TA = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
VOH	Output HIGH Voltage	2.4	Vcc	Volts	Vcc = 4.75V, IOH = -200 µA
VOL	Output LOW Voltage		0.4	Volts	Vcc = 4.75V, IOL = 2.1 mA
VIH	Input HIGH Voltage	2.0	Vcc	Volts	
VIL	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
IIL	Input Load Current		10	µA	Vcc = 5.25V, 0V ≤ Vin ≤ 5.25V
ILO	Output Leakage Current		10	µA	Chip Deselected
Icc	Power Supply Current		98	mA	Vout = +0.4V to Vcc Output Unloaded Vcc = 5.25V, Vin = Vcc

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

TA = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	SY2316B		SY2316A		Units	Test Conditions
		Min.	Max.	Min.	Max.		
tACC	Address Access Time		450		550	ns	Output load: 1 TTL load and 100 pf Input transition time: 20ns Timing reference levels: Input: 1.5V Output: 0.8V and 2.2V
tCO	Chip Select Delay		250		300	ns	
tDF	Chip Deselect Delay		150		150	ns	
tOH	Previous Data Valid After Address Change Delay	20		20		ns	

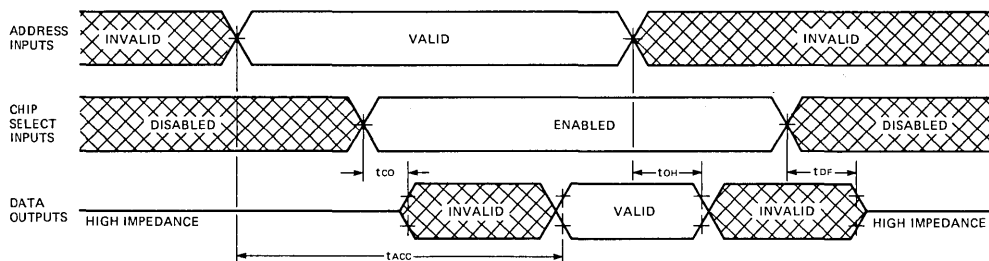
CAPACITANCE

tA = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
CI	Input Capacitance		7	pF	All pins except pin under test tied to AC ground
CO	Output Capacitance		10	pF	

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



ROMs
EPROMs



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards; a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

Table with 3 columns: COLUMN, INFORMATION, and card type (First Card, Second Card, Third Card, Fourth Card). It lists fields like Customer name, part number, contact info, and logic level settings.

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O8) is the MSB, and Output 1 (O1) is the LSB.

Table with 3 columns: COLUMN, INFORMATION, and Data Cards. It maps column ranges to decimal addresses and octal equivalents of output data.

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O8) is the MSB and Output 1 (O1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

Table with 3 columns: COLUMN, INFORMATION, and Data Cards. It maps column ranges to 5-digit decimal equivalents and output data for initial input addresses.

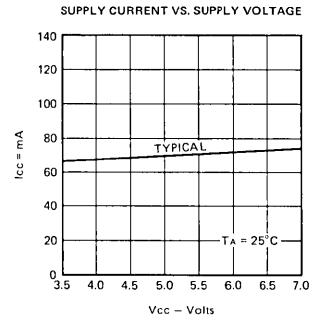
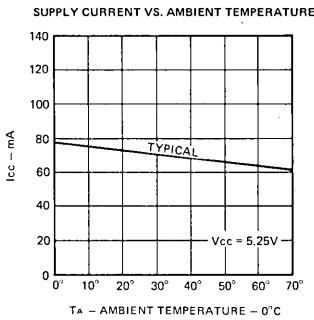
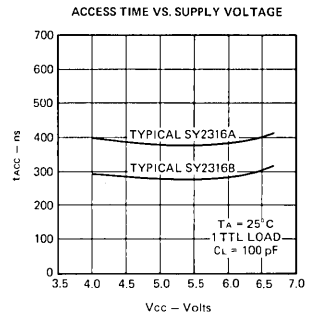
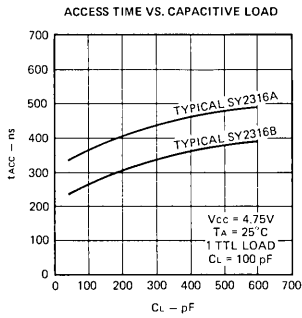
Send bit pattern data to the following special address:

Synertek - ROM
P.O. Box 552
Santa Clara, CA 95052

ROMS
EPROMs

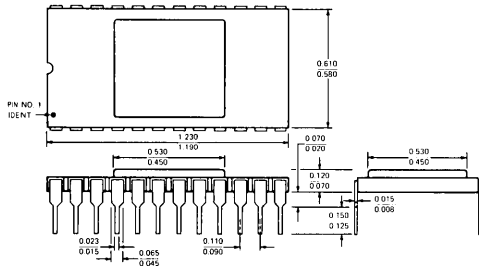


TYPICAL CHARACTERISTICS

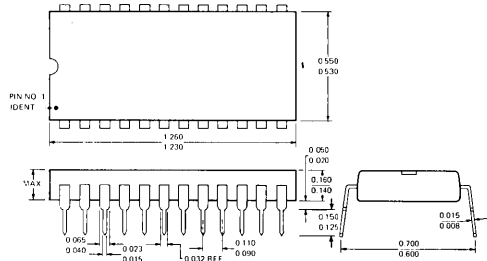


PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



ROMs EPROMs



2048x8 Static Read Only Memory

SY2316B-3

MEMORY PRODUCTS

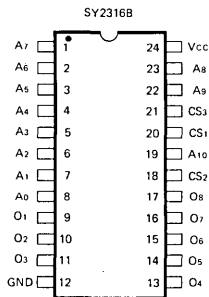
- Access Time—300ns (max.)
- 2048x8 Bit Organization
- Single +5 Volt Supply
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316B — Pin Compatible with 2708 EPROM
— Replacement for Two 2708s

The SY2316B-3 high performance Read Only Memory is organized 2048 words by 8 bits with an access time of less than 300 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

The SY2316B-3 operates totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. The device offers three-state output buffers for memory expansion.

Designed to replace two 2708 8K EPROMs, the SY2316B-3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATION

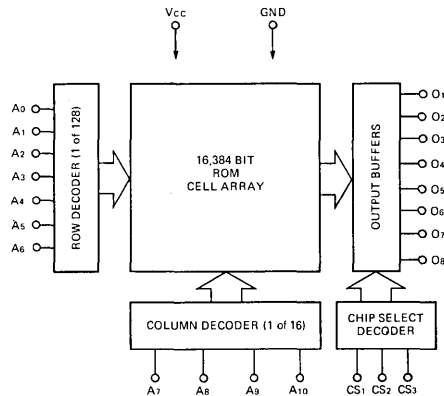


ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC2316B-3	Ceramic	300ns	0°C to +70°C
SYP2316B-3	Plastic	300ns	0°C to +70°C

A custom number will be assigned by Synertek.

BLOCK DIAGRAM



ROMS
EPROMS



ROMs
EPROMs

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	0° to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V _{OH}	Output HIGH Voltage	2.4	V _{CC}	Volts	V _{CC} = 4.75V, I _{OH} = -200 μA
V _{OL}	Output LOW Voltage		0.4	Volts	V _{CC} = 4.75V, I _{OL} = 2.1 mA
V _{IH}	Input HIGH Voltage		V _{CC}	Volts	
V _{IL}	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
I _{LI}	Input Load Current		10	μA	V _{CC} = 5.25V, 0V ≤ V _{in} ≤ 5.25V
I _{LO}	Output Leakage Current		10	μA	Chip Deselected
I _{CC}	Power Supply Current		98	mA	V _{out} = +0.4V to V _{CC} Output Unloaded V _{CC} = 5.25V, V _{in} = V _{CC}

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t _{ACC}	Address Access Time		300	ns	Output load: 1 TTL load and 100 pF
t _{CO}	Chip Select Delay		130	ns	
t _{DF}	Chip Deselect Delay		130	ns	Input transition time: 20ns
t _{OH}	Previous Data Valid After Address Change Delay	20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

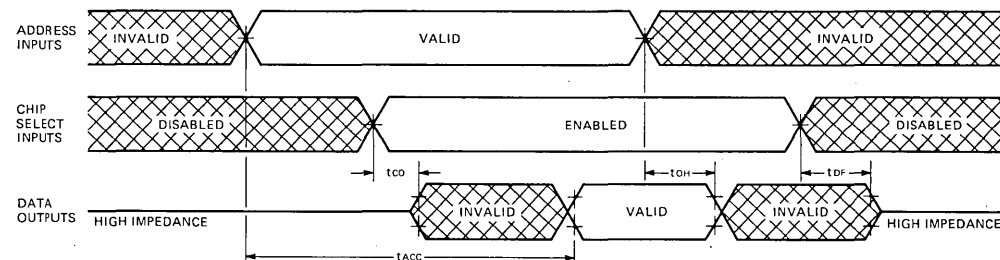
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C _I	Input Capacitance		7	pF	All pins except pin under test tied to AC ground
C _O	Output Capacitance		10	pF	

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM





PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1-30	Customer name
	31-50	Customer part number
	60-72	Synertek part number (punch "2316B-3")
Second Card	1-30	Customer contact (name)
	31-50	Customer telephone number
Third Card	1-6	Leave blank -- pattern number to be assigned by Synertek
	30	CS ₃ /CS ₃ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
	31	CS ₂ /CS ₂ chip select logic level.
Fourth Card	32	CS ₁ /CS ₁ chip select logic level.
	1-8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15-28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35-57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O₈) is the MSB, and Output 1 (O₁) is the LSB.

	COLUMN	INFORMATION
Data Cards	1-4	Decimal address
	6-13	Output (MSB-LSB)
	15-17	Octal equivalent of output data
	22-25	Decimal address
	27-34	Output (MSB-LSB)
	36-38	Octal equivalent of output data
	43-46	Decimal address
	48-55	Output (MSB-LSB)
	57-59	Octal equivalent of output data
	64-67	Decimal address
	69-76	Output (MSB-LSB)
	78-80	Octal equivalent of output data

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O₈) is the MSB and Output 1 (O₁) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

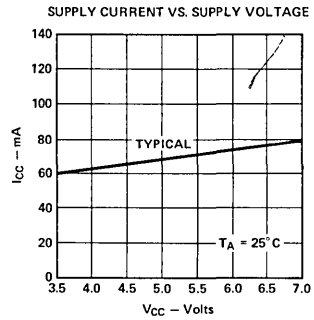
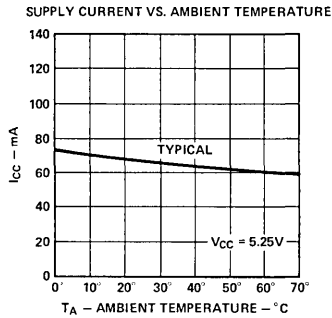
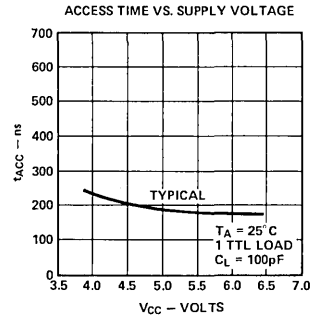
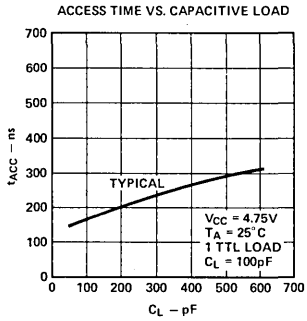
	COLUMN	INFORMATION
Data Cards	1-5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7-14	Output data (MSB-LSB) for initial input address.
	16-23	Output data for initial input address +1
	25-32	Output data for initial input address +2
	34-41	Output data for initial input address +3
	43-50	Output data for initial input address +4
	52-59	Output data for initial input address +5
	61-68	Output data for initial input address +6
	70-77	Output data for initial input address +7
	79-80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:

Synertek — ROM
P.O. Box 552
Santa Clara, CA 95052

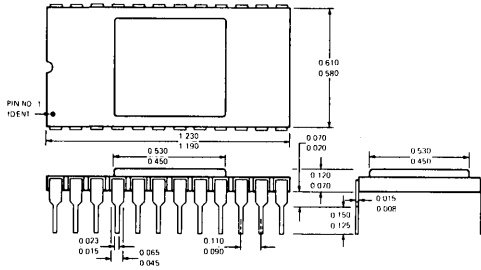


TYPICAL CHARACTERISTICS

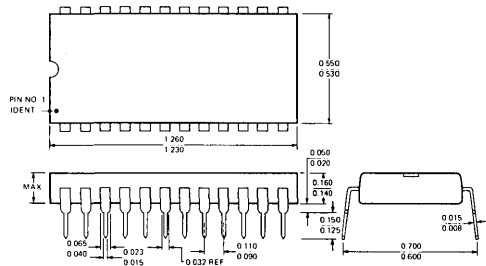


PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



ROMs
EPROMs



4096 x 8 Static Read Only Memory

SY2332/33

MEMORY PRODUCTS

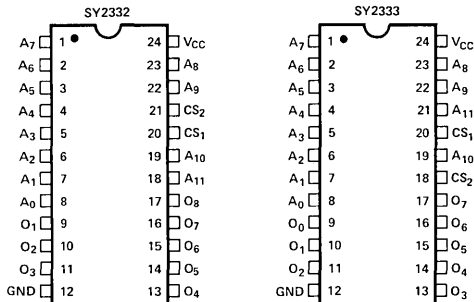
- SY2333-2732 EPROM Pin Compatible
- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time—450ns (max)
- Totally Static Operation
- Completely TTL Compatible
- SY2332-2716 EPROM Pin Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- 2708/2716/2732 EPROMs Accepted as Program Data Inputs

The SY2332/3 high performance read only memory is organized 4096 words by 8 bits with access times of less than 450 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

The SY2332/3 operates totally asynchronously. No clock input is required. The two programmable Chip Select inputs allow four 32K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

Designed to replace 2716 or 2732 32K EPROMs, the SY2332/3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATION

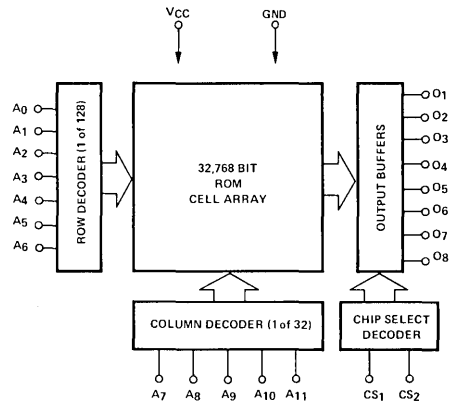


ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC2333	Ceramic	450ns	0°C to +70°C
SYP2333	Plastic	450ns	0°C to +70°C
SYC2332	Ceramic	450ns	0°C to +70°C
SYP2332	Plastic	450ns	0°C to +70°C

A custom number will be assigned by Synertek.

BLOCK DIAGRAM



ROMS
EPROMs



ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V _{OH}	Output HIGH Voltage	2.4	V _{CC}	Volts	V _{CC} = 4.75V, I _{OH} = -200μA
V _{OL}	Output LOW Voltage	0.4	V _{CC}	Volts	V _{CC} = 4.75V, I _{OL} = 2.1 mA
V _{IH}	Input HIGH Voltage	2.0	V _{CC}	Volts	
V _{IL}	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
I _{LI}	Input Load Current		10	μA	V _{CC} = 5.25V, 0V ≤ V _{IN} ≤ 5.25V
I _{LO}	Output Leakage Current		10	μA	Chip Deselected
I _{CC}	Power Supply Current		100	mA	V _{OUT} = +0.4 V to V _{CC} Output Unloaded, Chip Enabled V _{CC} = 5.25V, V _{IN} = V _{CC}

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	SY2332		Units	Test Conditions
		Min.	Max.		
t _{ACC}	Address Access Time		450	ns	Output load: 1 TTL load and 100pF
t _{CO}	Chip Select Delay		150	ns	
t _{DF}	Chip Deselect Delay		150	ns	Input transition time: 20ns
t _{OH}	Previous Data Valid After Address Change Delay	20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

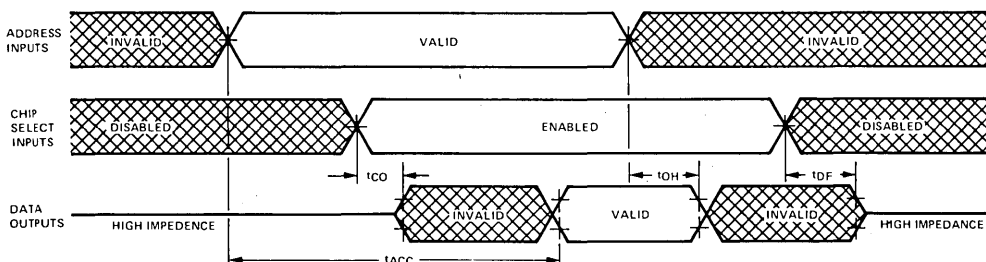
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C _I	Input Capacitance		7	pF	
C _O	Output Capacitance		10	pF	All pins except pin under test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



ROMs
EPROMs



ROMs
 EPROMs

PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards or 1" wide paper tape.

CARD FORMAT

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMs. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMs. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1-30	Customer name
	31-50	Customer part number
	60-72	Synertek part number (punch 2333 or 2332)
Second Card	1-30	Customer contact (name)
	31-50	Customer telephone number
Third Card	1-6	Leave blank — pattern number to be assigned by Synertek
	30	CS ₂ /CS ₂ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"; if DON'T CARE, punch "2")
	31	CS ₁ /CS ₁ chip select logic level.
Fourth Card	1-8	Data Format. Punch "Intel" starting in column one.
	15-28	Logic Format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35-37	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH and an "N" is defined as a LOW. Output 8 (O₈ or O₇) is the MSB and Output 1 (O₁ or O₀) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

	COLUMN	INFORMATION
Data Cards	1-5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7-14	Output data (MSB-LSB) for initial input address.
	16-23	Output data for initial input address +1
	25-32	Output data for initial input address +2

34-41	Output data for initial input address +3
43-50	Output data for initial input address +4
52-59	Output data for initial input address +5
61-68	Output data for initial input address +6
70-77	Output data for initial input address +7
79-80	ROM pattern number (may be left blank)

INTEL PAPER TAPE FORMAT

The paper tape which should be used is 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces.

BPNF Format

The format requirements are as follows:

- All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
- Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F for the N x 8 organization.
NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high tape level output, and an N results in a low level output.
- Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
- Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
- Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
- MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

HEXADECIMAL PROGRAM TAPE FORMAT

The hexadecimal tape format used by the INTELLEC 8 system is a modified memory image, blocked into discrete records. Each record contains record length, record type, memory address, and checksum information in addition to data. A frame by frame description is as follows:

Frame 0	Record mark. Signals the start of a record. The ASCII character colon (":") (HEX 3A) is used as the record mark.
Frames 1, 2 (0-9, A-F)	Record length. Two ASCII characters representing a hexadecimal number in the range 0 to 'FF' (0 to 255). This is the count of the actual data bytes in the record type or checksum. A record length of 0 indicates end of file.
Frames 3 to 6	Load Address. Four ASCII characters that represent the initial memory will be loaded. The first data byte is stored in the location pointed to by the load address, succeeding data bytes are loaded into ascending addresses.

Frames 7, 8

Record type. Two ASCII characters. Currently all records are type 0, this field is reserved for future expansion. Data. Each 8 bit memory word is represented by two frames containing the ASCII characters (0 to 9, A to F) to represent a hexadecimal value 0 to 'FF' (0 to 255).

Frames 9 to 9+2*
(Record Length) -1

Frames 9+2*
(Record Length) to
9+2* (Record
Length) +1

Checksum. The checksum is the negative of the sum of all 8 bit bytes in the record since the record mark (":") evaluated modulus 256. That is, if you add together all the 8 bit bytes, ignor-

ing all carries out of an 8-bit sum, then add the checksum, the result is zero.

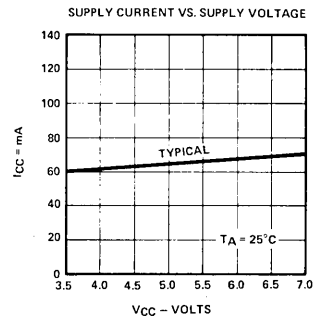
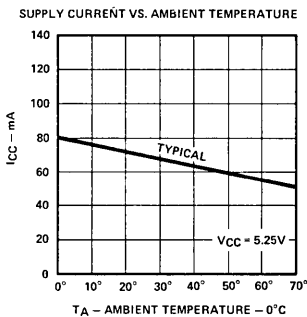
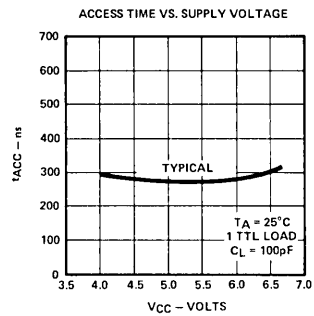
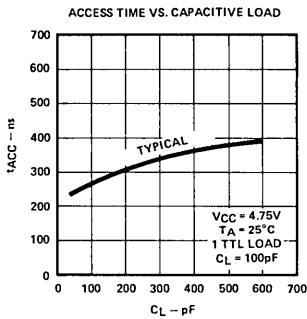
Example: If memory locations 1 through 3 contain 53F8EC, the format of the hex file produced when these locations are punched is:

:0300010053F8ECC5

Send bit pattern data to the following special address:

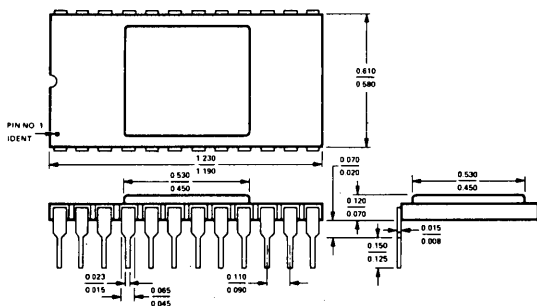
Synertek - ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

TYPICAL CHARACTERISTICS

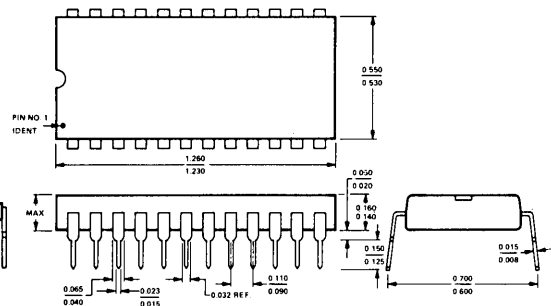


PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE





8192 x 8 Static Read Only Memory

SY2364

MEMORY PRODUCTS

PRELIMINARY

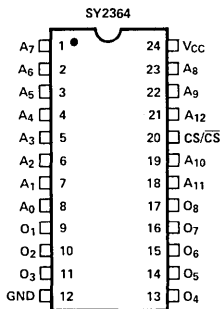
- SY2716–2732 EPROM Pin Compatible
- 8192 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time—450ns (max)
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Programmable Chip Select
- 2708/2716/2732 EPROMs Accepted as Program Data Inputs
- SY2316–SY2332 ROM Pin Compatible

The SY2364 high performance Read Only Memory is organized 8192 words by 8 bits with access times of less than 450 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

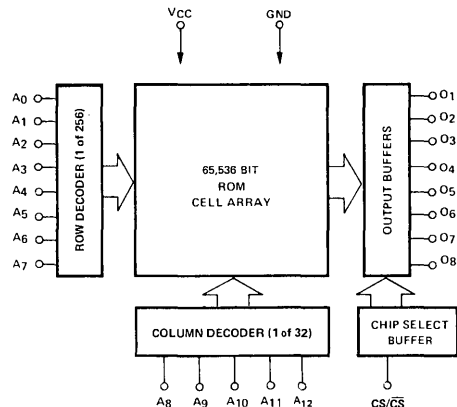
The SY2364 operates totally asynchronously. No clock input is required. The programmable Chip Select input allows two 64K ROMs to be OR-tied without external decoding. The SY2364 offers three-state output buffers for memory expansion.

Designed to replace 2716 or 2732 EPROMs, the SY2364 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC2364	Ceramic	450ns	0°C to +70°C
SYP2364	Plastic	450ns	0°C to +70°C

A custom number will be assigned by Synertek.

ROMS
EPROMs

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS
 $T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = 5.0\text{V} \pm 5\%$ (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	Volts	$V_{CC} = 4.75\text{V}, I_{OH} = -200\mu\text{A}$
V_{OL}	Output LOW Voltage	0.4	0.4	Volts	$V_{CC} = 4.75\text{V}, I_{OL} = 2.1\text{mA}$
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	μA	$V_{CC} = 5.25\text{V}, 0\text{V} \leq V_{IN} \leq 5.25\text{V}$
I_{LO}	Output Leakage Current		10	μA	Chip Deselected
I_{CC}	Power Supply Current		120	mA	$V_{OUT} = +0.4\text{V to } V_{CC}$ Output Unloaded, Chip Enabled $V_{CC} = 5.25\text{V}, V_{IN} = V_{CC}$

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

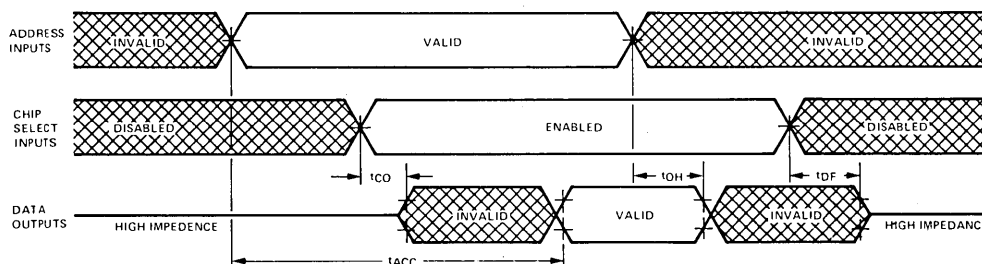
A.C. CHARACTERISTICS
 $T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = 5.0\text{V} \pm 5\%$ (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		450	ns	Output load: 1 TTL load and 100pF Input transition time: 20ns Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V
t_{CO}	Chip Select Delay		150	ns	
t_{DF}	Chip Deselect Delay		150	ns	
t_{OH}	Previous Data Valid After Address Change Delay	20		ns	

CAPACITANCE
 $T_A = 25^\circ\text{C}, f = 1.0\text{MHz}$, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under test tied to AC ground
C_O	Output Capacitance		10	pF	

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM




ROMS
EPROMS

PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards or 1" wide paper tape.

CARD FORMAT

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMs. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMs. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1-30	Customer name
	31-50	Customer part number
	60-72	Synertek part number (punch 2364)
Second Card	1-30	Customer contact (name)
	31-50	Customer telephone number
Third Card	1-6	Leave blank - pattern number to be assigned by Synertek
	30	CS/CS chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
Fourth Card	1-8	Data Format. Punch "Intel" starting in column one.
	15-28	Logic Format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35-37	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH and an "N" is defined as a LOW. Output 8 (O₈ or O₇) is the MSB and Output 1 (O₁ or O₀) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

	COLUMN	INFORMATION
Data Cards	1-5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7-14	Output data (MSB-LSB) for initial input address.
	16-23	Output data for initial input address +1
	25-32	Output data for initial input address +2

34-41	Output data for initial input address +3
43-50	Output data for initial input address +4
52-59	Output data for initial input address +5
61-68	Output data for initial input address +6
70-77	Output data for initial input address +7
79-80	ROM pattern number (may be left blank)

INTEL PAPER TAPE FORMAT

The paper tape which should be used is 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces.

BPNF Format

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F for the N x 8 organization.
NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high tape level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

HEXADECIMAL PROGRAM TAPE FORMAT

The hexadecimal tape format used by the INTELLEC 8 system is a modified memory image, blocked into discrete records. Each record contains record length, record type, memory address, and checksum information in addition to data. A frame by frame description is as follows:

Frame 0	Record mark. Signals the start of a record. The ASCII character colon (":") HEX 3A) is used as the record mark.
Frames 1, 2 (0-9, A-F)	Record length. Two ASCII characters representing a hexadecimal number in the range 0 to 'FF' (0 to 255). This is the count of the actual data bytes in the record type or checksum. A record length of 0 indicates end of file.
Frames 3 to 6	Load Address. Four ASCII characters that represent the initial memory will be loaded. The first data byte is stored in the location pointed to by the load address, succeeding data bytes are loaded into ascending addresses.

Frames 7, 8 Record type. Two ASCII characters. Currently all records are type 0, this field is reserved for future expansion.

Frames 9 to 9+2* (Record Length) -1 Data. Each 8 bit memory word is represented by two frames containing the ASCII characters (0 to 9, A to F) to represent a hexadecimal value 0 to 'FF' (0 to 255).

Frames 9+2* (Record Length) to 9+2* (Record Length) +1 Checksum. The checksum is the negative of the sum of all 8 bit bytes in the record since the record mark (":") evaluated modulus 256. That is, if you add together all the 8 bit bytes, ignor-

ing all carries out of an 8-bit sum, then add the checksum, the result is zero.

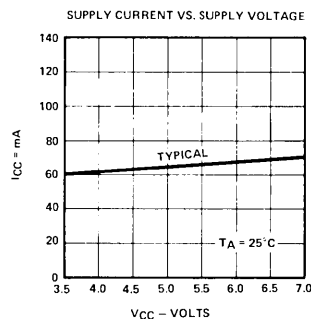
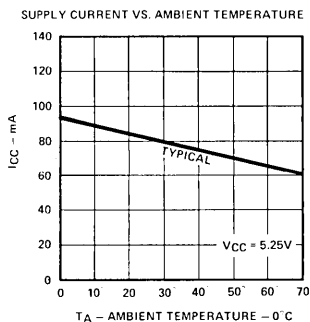
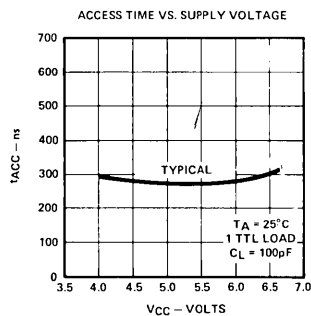
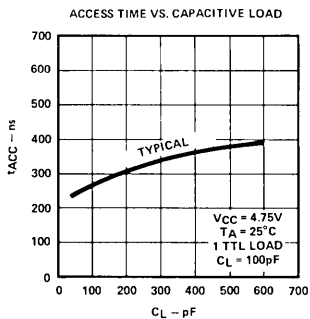
Example: If memory locations 1 through 3 contain 53F8EC, the format of the hex file produced when these locations are punched is:

```
:0300010053F8ECC5
```

Send bit pattern data to the following special address:

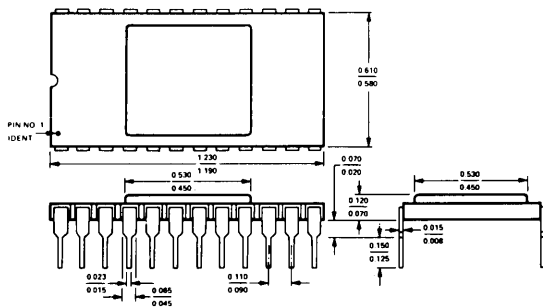
Synertek — ROM
P.O. Box 552 MS/34-A
3045 Stender Way
Santa Clara, CA 95052

TYPICAL CHARACTERISTICS

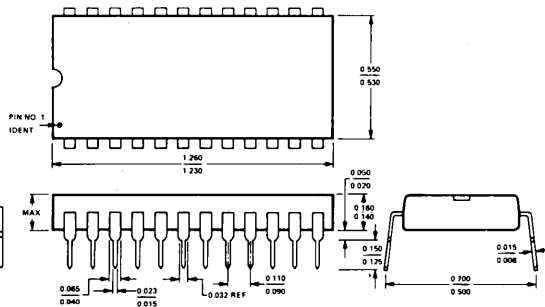


PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



ROMs
EPROMs



2048 x 8 EPROM

UV Erasable

SY2716

MEMORY PRODUCTS

Preliminary

ROMs
EPROMs

- Single +5 Volt Power Supply
- Low Power Dissipation
-525 mW Maximum
132 mW Standby
- Access Time - 350nsec to 450nsec
- Totally Static Operation

- Pin Compatible With SY2316B, and SY2333 Mask Programmable ROMs
- Single Address Programming with 50msec Pulse
- TTL Compatible - Read and Program On All Inputs and Outputs

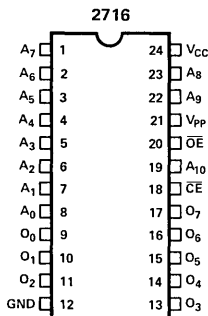
The SY2716 is a 16384-Bit electrically programmable, ultra-violet erasable, read-only memory. Organized 2048 words by 8 bits, the SY2716 operates from a single 5 volt power supply and is completely static in operation, requiring no clocks. In addition, a Chip Enabled controlled standby mode reduces the active power dissipation of 525 milliwatts to 132 milliwatts in standby, a 75% power savings.

The SY2716 is pin compatible with the existing 16K and 32K ROMs (SY2316B, SY2332), permitting simple conversion from EPROM prototype systems to mask programmable ROM production systems.

Programming the SY2716 is completely TTL compatible and requires no high voltage pulses. The SY2716 therefore can easily be programmed on PC boards in the system. In addition, each word can be individually programmed with the SY2716's single address programming. Total programming time for all 16384 bits is less than two minutes.

The high speed operation of the SY2716 (350nsec to 450nsec) makes this device ideal for use with high performance microprocessor systems now in production.

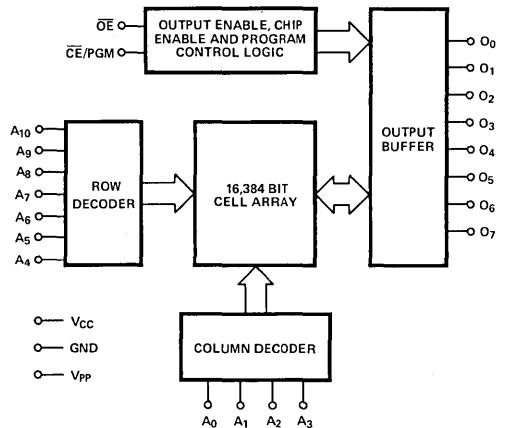
PIN CONFIGURATION



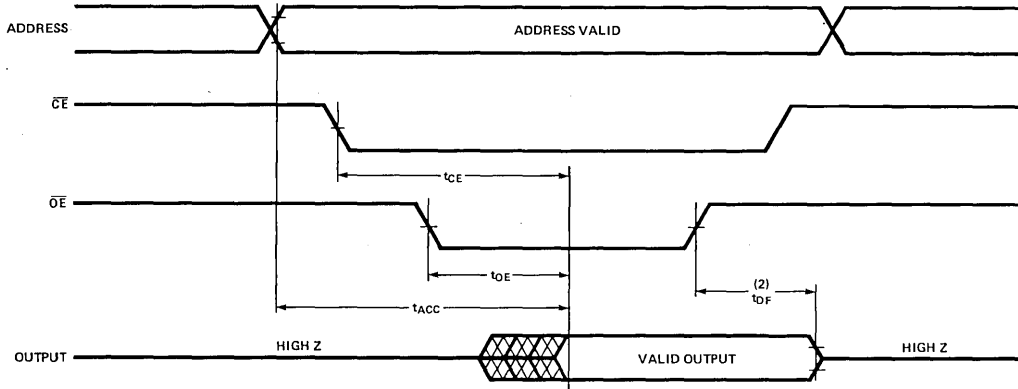
ORDERING INFORMATION

Order Number	Access Time	Temperature Range
SYC2716	450nsec	0°C to +70°C
SYC2716-1	350nsec	0°C to +70°C
SYC2716-2	390nsec	0°C to +70°C

BLOCK DIAGRAM



READ TIMING DIAGRAM



NOTE 2: t_{DF} IS SPECIFIED FROM \overline{OE} OR \overline{CE} , WHICHEVER OCCURS FIRST.

PROGRAMMING D.C. CHARACTERISTICS

$T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$; $V_{CC} = 5\text{V} \pm 5\%$; $V_{PP} = 25\text{V} \pm 1\text{V}$

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Current (for any input)			10	μA	$V_{IN} = 5.25\text{V}/0.45$
I_{PP1}	V_{PP} Supply Current			5	mA	$\overline{CE}/\text{PGM} = V_{IL}$
I_{PP2}	V_{PP} Supply Current During Programming Pulse			30	mA	$\overline{CE}/\text{PGM} = V_{IH}$
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	-0.1		0.8	V	
V_{IH}	Input High Level	2.0		$V_{CC}+1$	V	

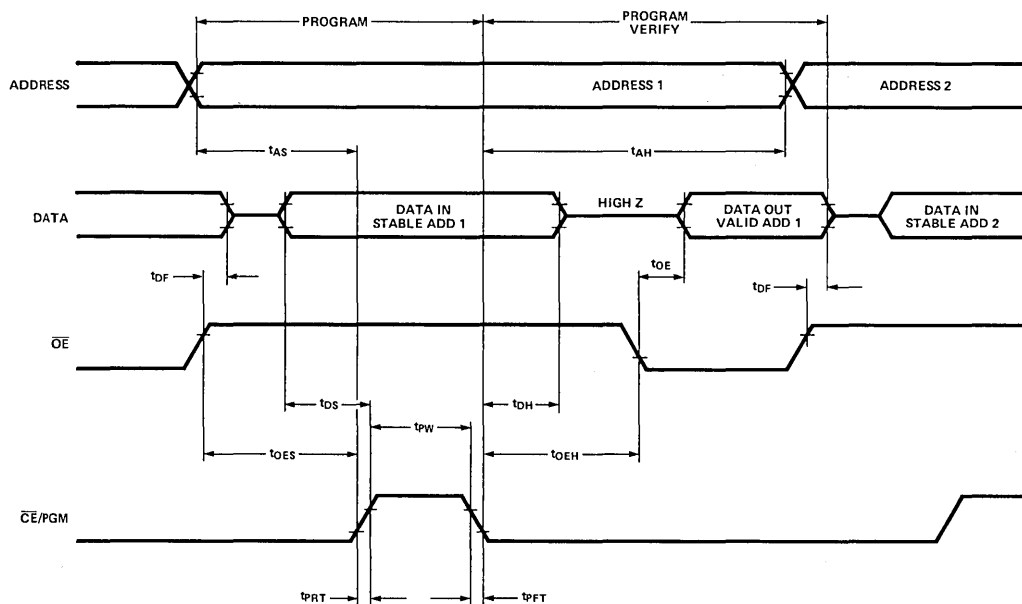
NOTE: During programming care must be taken to avoid V_{pp} transients exceeding the +26 volt maximum.

PROGRAMMING A.C. CHARACTERISTICS

$T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$; $V_{CC} = 5\text{V} \pm 5\%$; $V_{PP} = 25\text{V} \pm 1\text{V}$

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t_{AS}	Address Setup Time	2			μs	
t_{OES}	\overline{OE} Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	\overline{OE} Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Output Enable to Output Float Delay	0		120	ns	$\overline{CE}/\text{PGM} = V_{IL}$
t_{OE}	Output Enable to Output Delay			120	ns	$\overline{CE}/\text{PGM} = V_{IL}$
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTE: During application of power, care must be taken to assure that V_{CC} is applied before or simultaneously with V_{pp} . V_{pp} must be removed before or simultaneously with V_{CC} . The maximum allowable voltage during programming which may be applied to the V_{pp} with respect to ground is +26V. Care must be taken when switching the V_{pp} supply to prevent overshoot exceeding the 26V maximum specification. For convenience in programming, the 2716 may be verified with the V_{pp} supply at $25\text{V} \pm 1\text{V}$. During normal read operation, however, V_{pp} must be at V_{CC} .

PROGRAMMING TIMING DIAGRAM

ERASURE

Erasure of the SY2716 begins to occur when exposed to light with wavelengths shorter than 4000 angstroms. Certain types of ambient light contain wavelengths in this range. Although exposure to sunlight or fluorescent light for a relatively long time is required to cause erasure, care should be taken to avoid exposure to this type of light for extended periods.

Erasing the SY2716 is accomplished by exposing the device to ultra violet light with a wavelength of 2537 angstroms. The minimum dose (integrated) required for erasure is 15 W-sec/cm² (intensity at the device x exposure time). A 12 mW/cm² lamp (without filter) placed one inch from the device will require about 20 minutes for complete erasure. After erasure, all bits are in the logic "1" state.

A.C. CONDITIONS OF TEST:

V_{CC}	5V \pm 5%
V_{PP}	25V \pm 1V
Input Rise and Fall Times (10% to 90%)	20 ns
Input Pulse Levels	0.8V to 2.2V
Input Timing Reference Level	1V and 2V
Output Timing Reference Level	0.8V and 2V



OPERATIONAL DESCRIPTION

MODE \ PINS	\overline{CE}/PGM	\overline{OE}	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

1. Programming

Initially, at delivery, all bits of the SY2716 have been erased, and, therefore, are in the logic "1" state. Data is programmed into each memory word by introducing logic "0"s at each desired bit. The 2716 programming mode is selected by applying +25 volts to the V_{PP} power pin and holding the \overline{OE} Input in a logic "1" state. The data to be programmed is applied in an 8 bit parallel format to the Data Output pins. Addresses, as well as the data applied to the output pins, are completely TTL compatible. A 50 millisecond TTL level programming pulse is then applied to the \overline{CE}/PGM input to complete programming.

A TTL level Program pulse must be applied for each address location to be programmed. However, address locations may be selected at random, either individually or sequentially.

Because of this simple programming procedure, multiple 2716s can easily be programmed in parallel. Inputs of each of the devices are simply connected together and then common Data, Address and Program signals are applied to all devices simultaneously.

2. Program Inhibit

Because programming of the SY2716 is totally controlled by the \overline{CE}/PGM input, multiple 2716s can be simply programmed in parallel with different data. Addresses and Data Output pins of each device are connected in common to the desired data source. The specific 2716 to be programmed is then selected by applying a TTL logic "1" voltage level to the \overline{CE}/PGM pin of the desired device. Programming of all other devices connected in parallel is inhibited with a TTL logic "0" input on the \overline{CE}/PGM input.

3. Program Verify

Immediately following the programming of an SY2716 EPROM, each of the data words should be read to assure accurate programming. This verify may be performed with V_{PP} held at +25 volts by applying a low level TTL logic signal ("0") to the \overline{OE} Input. Except during the verify and programming operations, V_{PP} should be held at +5 volts (V_{CC}).

4. Read Mode

The read mode is selected by holding both \overline{CE}/PGM and \overline{OE} Inputs at a TTL logic "0" level while applying 5.0V power to both V_{CC} and V_{PP} inputs. Appropriate data previously programmed into the selected address then appears in the Data Output pins. Chip Enable (\overline{CE}) is the power control, and must be used to select the device. Output Enable (\overline{OE}) controls only the output stages and must be used to gate data to the Output pins independently of device selection.

5. Standby Mode

Power dissipation of the SY2716 is controlled by the \overline{CE} input and can be reduced to standby power level (132 milliwatts max) simply by applying a TTL logic "1" signal to the \overline{CE} Input. Whenever \overline{CE} is in the logic "1" state, Outputs are in a high impedance state, independent of the \overline{OE} input status.

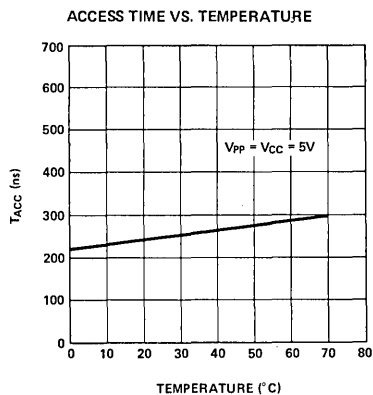
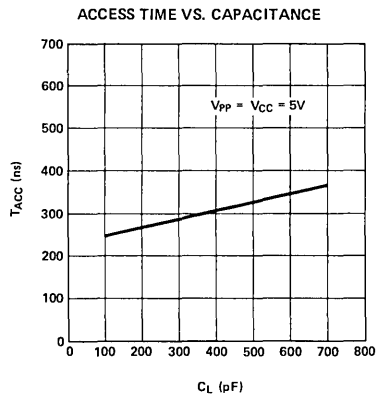
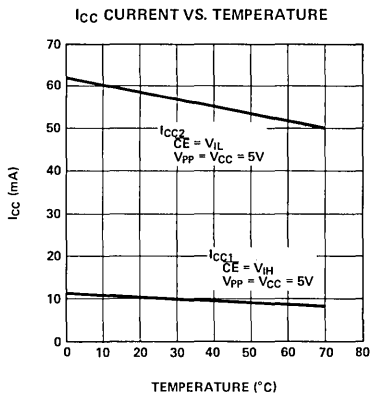
6. Output Control

The outputs of multiple SY2716s may be or-tied to provide memory expansion. Since these outputs will be tied in common to the same data bus, only one SY2716 should be selected (\overline{OE} Logic "0" level) to prevent data bus contention between SY2716s or other memory circuits connected to the bus. The output of the desired SY2716 is enabled simply by providing a TTL logic "0" signal to the \overline{OE} Input. Conversely, outputs of other 2716s are deselected by applying a logic "1" signal to their \overline{OE} Inputs.

PROGRAMMING

The SY2716 is programmed by selectively programming logic "0"s in the memory matrix set initially in the all logic "1" state by erasure. Only logic "0"s can be programmed electrically; logic "1"s can only be obtained by UV erasure. Programming is accomplished by applying a 50msec TTL pulse to the \overline{CE}/PGM pulse with $25V \pm 1V$ applied to V_{PP} and a TTL logic "1" applied to the \overline{OE} input. The specific word to be programmed is selected with the address inputs, and the data to be programmed is applied to the data output pins.

TYPICAL CHARACTERISTICS



PACKAGE DIAGRAM

ROMs
EPROMs



2048 x 8 Static Read Only Memory

SY4600

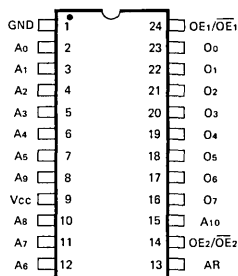
MEMORY PRODUCTS

- 2048x8 or 4096x4 Bit Organizations
- Single +5 Volt Supply
- Two Week Prototype Turnaround
- Access Time – 550 ns. (max.)
- Totally Static Operation
- Synchronous or Asynchronous Operation
- Completely TTL Compatible
- Two Programmable Output Enables
- Three-State Outputs for Wire-OR Expansion
- On-Chip Address Registers
- Low Power Dissipation – 31 μ W/Bit (max.)
- Pin-for-Pin Replacement for EA4600

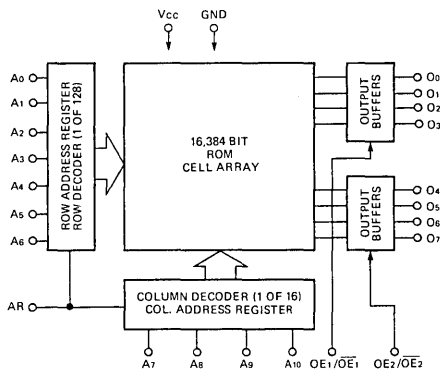
The SY4600 is a high performance 16,384 bit static read only memory organized 2048 words by 8 bits or 4096 words by 4 bits. The device is designed to be compatible with all microprocessor and similar applications where large bit storage and simple interfacing are important design considerations. Synertek's N-channel ion-implanted silicon gate process produces a +5 Volt TTL compatible ROM with a minimum noise immunity of 0.4 Volt.

Synchronous or asynchronous operation offers maximum design flexibility. Clocking the Address Read (AR) input stores the applied address information. The outputs appear and remain stable until a new address is read. With the AR input HIGH, output data asynchronously appear 550ns after the application of a new address. Two programmable Output Enables control four outputs each permitting 4 bit or 8 bit operation.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC4600	Ceramic	550ns	0°C to +70°C
SYP4600	Plastic	550ns	0°C to +70°C

A custom number will be assigned by Synertek.

ROMs
EPROMs

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0° to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V _{OH}	Output HIGH Voltage	2.4	V _{CC}	Volts	V _{CC} = 4.75V, I _{OH} = -200 μA
V _{OL}	Output LOW Voltage		0.4	Volts	V _{CC} = 4.75V, I _{OH} = 2.4 mA
V _{IH}	Input HIGH Voltage	2.0	V _{CC}	Volts	
V _{IL}	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
I _{LI}	Input Load Current		10	μA	V _{CC} = 5.25V, 0V ≤ V _{in} ≤ 5.25V
I _{LO}	Output Leakage Current		10	μA	Chip Deselected
I _{CC}	Power Supply Current		98	mA	V _{out} = +0.4V to V _{CC} Output Unloaded V _{CC} = 5.25V, V _{in} = V _{CC}

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

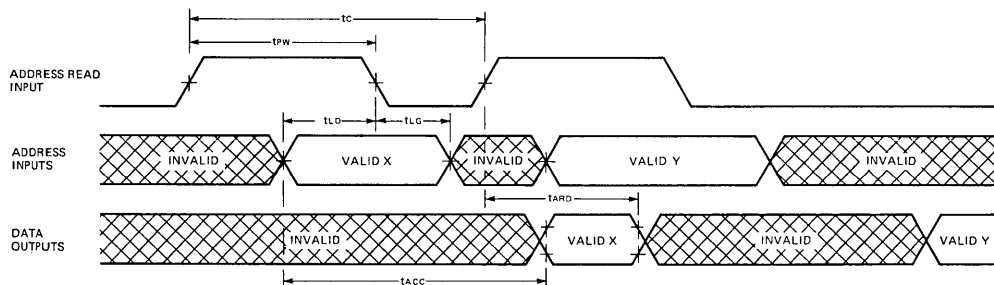
A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 5% (unless otherwise specified)

CLOCKED MODE TIMING SPECIFICATIONS (See Figure 1)

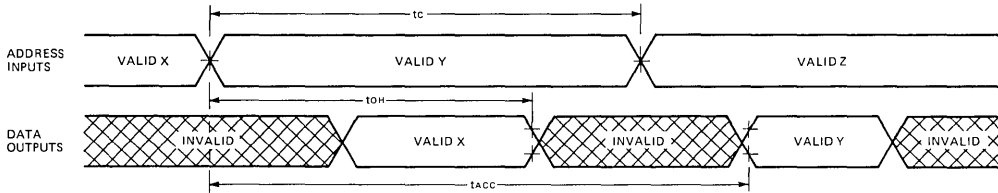
Symbol	Parameter	Min.	Max.	Units	Test Conditions
t _c	Cycle Time	500		ns	Output load: 1 TTL load and 100 pf
t _{ACC}	Address to Output Delay Time		550	ns	Input transition time: 20 ns
t _{PW}	Address Read Pulse Width	300		ns	Timing reference levels:
t _{LD}	Address Lead Time	100		ns	Input: 1.5V
t _{LG}	Address Lag Time	150		ns	Output: 0.8V and 2.2 V
t _{ARD}	AR Input to Output Disturb Delay	75		ns	

FIGURE 1 – CLOCKED MODE TIMING DIAGRAM

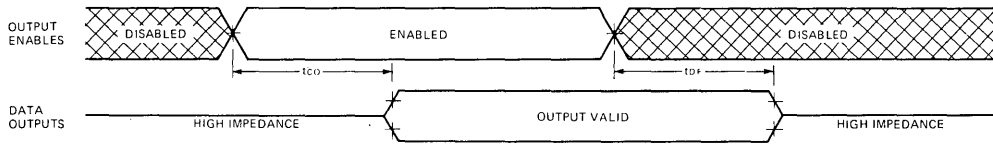


UNCLOCKED MODE TIMING SPECIFICATIONS (See Figure 2)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_c	Cycle Time	500		ns	$AR = V_{cc}$
t_{ACC}	Address Access Time		550	ns	See clocked mode timing specifications
t_{OH}	Previous Data Valid After Address Change Delay	75		ns	

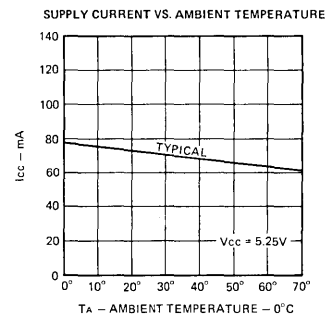
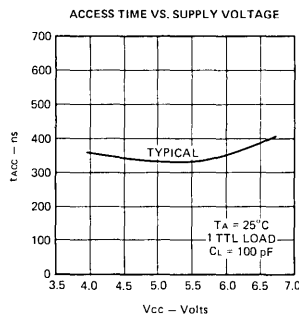
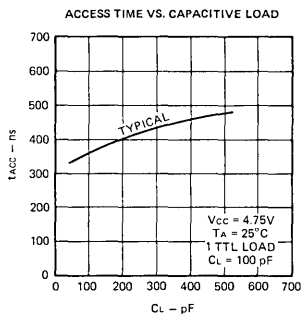
FIGURE 2 – UNLOCKED MODE TIMING DIAGRAM (AR = V_{cc})

OUTPUT ENABLE TIMING SPECIFICATIONS (CLOCKED OR UNLOCKED) (See Figure 3)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{CO}	Output Enable Delay		300	ns	See clocked mode timing specifications
t_{DF}	Output Disable Delay		300	ns	

FIGURE 3 – OUTPUT ENABLE TIMING DIAGRAM (CLOCKED OR UNLOCKED MODES)

CAPACITANCE
 $t_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_i	Input Capacitance		7	pF	All pins except pin under test tied to AC ground
C_o	Output Capacitance		10	pF	

Note 2: This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS


PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1-30	Customer name
	31-50	Customer part number
	60-72	Synertek part number (punch "4600")
Second Card	1-30	Customer contact (name)
	31-50	Customer telephone number
Third Card	1-6	Leave blank — pattern number to be assigned by Synertek
	31	OE ₂ /OE ₂ output enable logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
Fourth Card	32	OE ₁ /OE ₁ output enable logic level.
	1-8	Data Format. Synertek, or Electronic Arrays data card format may be used. Specify format by punching "Synertek" or "EA" starting in column one.
	15-28	Logic format: punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35-37	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck).

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 7 (O₇) is the MSB, and Output 0 (O₀) is the LSB.

	COLUMN	INFORMATION
Data Cards	1-4	Decimal address
	6-13	Output (MSB-LSB)
	15-17	Octal equivalent of output data
	22-25	Decimal address
	27-34	Output (MSB-LSB)
	36-38	Octal equivalent of output data
	43-46	Decimal address
	48-55	Output (MSB-LSB)
	57-59	Octal equivalent of output data
	64-67	Decimal address
	69-76	Output (MSB-LSB)
	78-80	Octal equivalent of output data

ELECTRONIC ARRAYS DATA CARD FORMAT

All addresses are coded in octal form (address 0 = 0000, address 2047 = 3777, A₁₀ = MSB and A₀ = LSB). All output words are also coded in octal. Output 7 (O₇) is the MSB, and Output 0 (O₀) is the LSB. The four Title Cards discussed above must accompany the EA card deck.

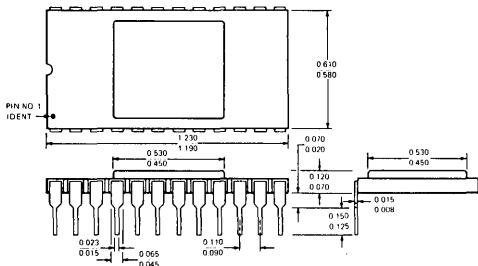
	COLUMN	INFORMATION
Data Cards	1-4	Octal equivalent of initial input address.
	5-7	Octal equivalent of output data for initial input address.
	8-10	Octal equivalent of output data for initial input address +1.
	11-13	Octal equivalent of output data for initial address +2
	⋮	⋮
	⋮	⋮
	⋮	⋮
	50-52	Octal equivalent of output data for initial address +15.
69-80	ROM pattern number (may be left blank).	

Send bit pattern data to the following special address:

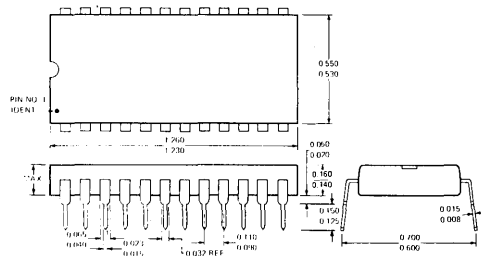
Synertek — ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



ROMs
EPROMs

Microprocessors

Microprocessors



8-Bit Microprocessor Family

SY6500

MICROPROCESSOR PRODUCTS

- Single 5 V $\pm 5\%$ power supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- Bi-directional Data Bus
- Instruction decoding and control
- Addressable memory range of up to 65 K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1 MHz, 2 MHz, and 3 MHz operation
- On-chip clock options
 - * External single clock input
 - * Crystal time base input
- 40 and 28 pin package versions
- Pipeline architecture

The SY6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the SY6500 family are software compatible within the group and are bus compatible with the MC6800 product offering.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs or crystals provide the time base. The external clock versions are geared for the multi-processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz, 2 MHz, and 3 MHz maximum operating frequencies.

MEMBERS OF THE FAMILY

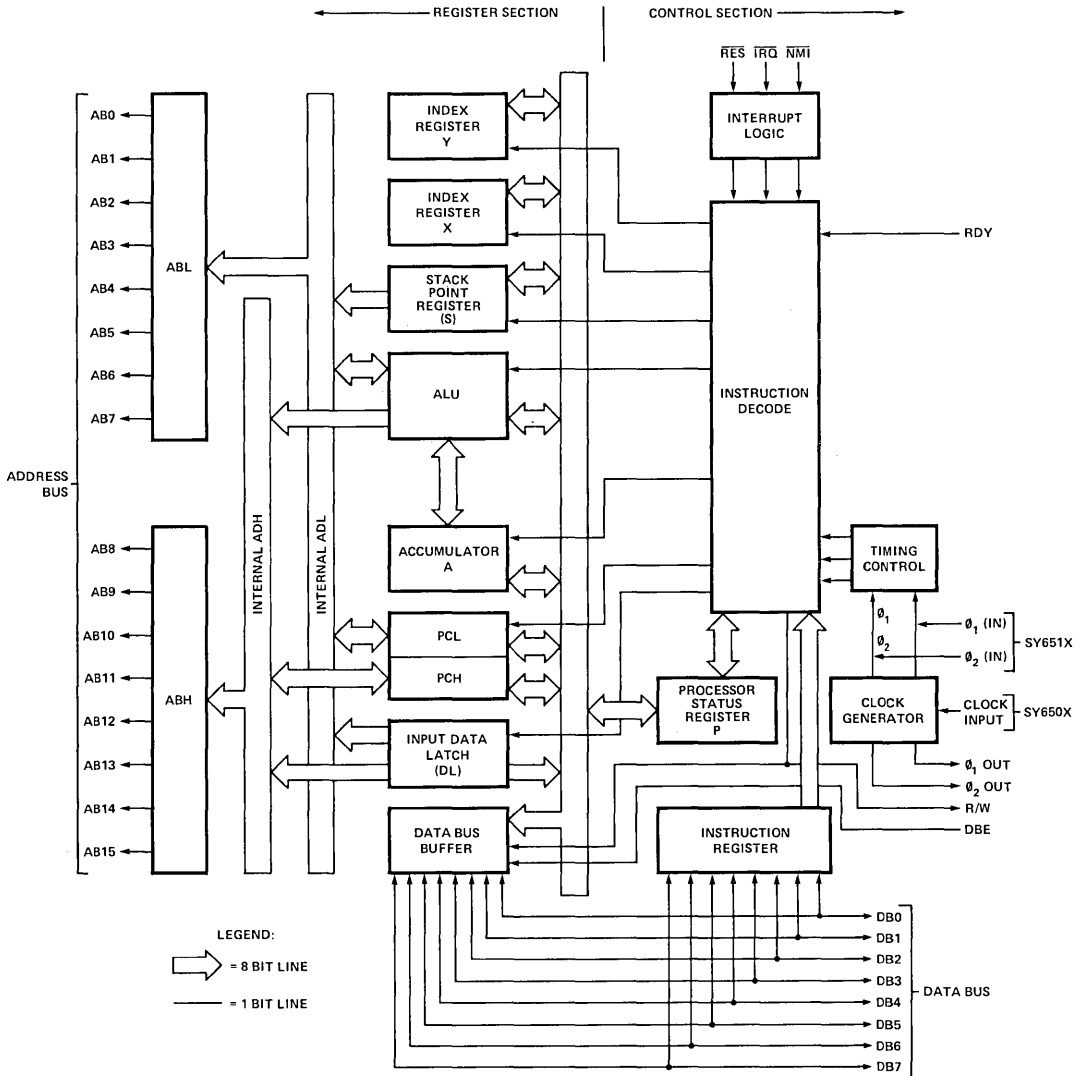
PART NUMBERS		CLOCKS	PINS	\overline{IRQ}	\overline{NMI}	RDY	ADDRESSING
Plastic	Ceramic						
SYP6502	SYC6502	On-Chip	40	✓	✓	✓	16 (64 K)
SYP6503	SYC6503	"	28	✓	✓		12 (4 K)
SYP6504	SYC6504	"	28	✓			13 (8 K)
SYP6505	SYC6505	"	28	✓		✓	12 (4 K)
SYP6506	SYC6506	"	28	✓			12 (4 K)
SYP6507	SYC6507	"	28			✓	13 (8 K)
SYP6512	SYC6512	External	40	✓	✓	✓	16 (64 K)
SYP6513	SYC6513	"	28	✓	✓		12 (4 K)
SYP6514	SYC6514	"	28	✓			13 (8 K)
SYP6515	SYC6515	"	28	✓		✓	12 (4 K)



COMMENTS ON THE DATA SHEET

The data sheet is constructed to review first the basic "Common Characteristics" – those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

SY6500 INTERNAL ARCHITECTURE



NOTE:
 1. CLOCK GENERATOR IS NOT INCLUDED ON SY651X.
 2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE SY6500 PRODUCTS.





D.C. CHARACTERISTICS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{in}	-0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

COMMENT

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0-70^\circ C$)

(\emptyset_1, \emptyset_2 applies to SY651X, \emptyset_o (in) applies to SY650X)

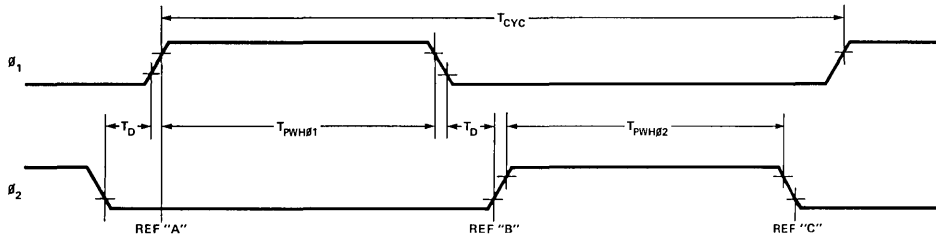
Symbol	Characteristic	Min.	Max.	Unit	
V_{IH}	Input High Voltage				
	Logic, \emptyset_o (in) (650X) \emptyset_1, \emptyset_2 (651X)	+2.4 $V_{CC} - 0.5$	V_{CC} $V_{CC} + 0.25$	V	
V_{IL}	Input Low Voltage				
	Logic, \emptyset_o (in) (650X) \emptyset_1, \emptyset_2 (651X)	-0.3 -0.3	+0.4 +0.2	V	
I_{IL}	Input Loading ($V_{in} = 0V, V_{CC} = 5.25V$) RDY, S.O.	-10	-300	μA	
I_{in}	Input Leakage Current ($V_{in} = 0$ to 5.25 V, $V_{CC} = 0$)				
	Logic (Excl. RDY, S.O.)	-	2.5	μA	
	\emptyset_1, \emptyset_2 (651X)	-	100	μA	
	\emptyset_o (in) (650X)	-	10.0	μA	
I_{TSI}	Three-State (Off State) Input Current ($V_{in} = 0.4$ to 2.4 V, $V_{CC} = 5.25V$) DB0-DB7	-	10	μA	
V_{OH}	Output High Voltage ($I_{LOAD} = -100\mu A_{dc}, V_{CC} = 4.75V$) SYNC, DB0-DB7, A0-A15, R/W	2.4	-	V	
V_{OL}	Output Low Voltage ($I_{LOAD} = 1.6mA_{dc}, V_{CC} = 4.75V$) SYNC, DB0-DB7, A0-A15, R/W	-	0.4	V	
P_D	Power Dissipation				
	1 MHz and 2 MHz 3 MHz	- -	700 800	mW mW	
C	Capacitance ($V_{in} = 0, T_A = 25^\circ C, f = 1MHz$)				
	C_{in}	RES, NMI, RDY, IRQ, S.O., DBE DB0-DB7	- -	10 15	pF
	C_{out}	A0-A15, R/W, SYNC	-	12	
	C_{\emptyset_o (in)	\emptyset_o (in) (650X)	-	15	
	C_{\emptyset_1}	\emptyset_1 (651X)	-	50	
	C_{\emptyset_2}	\emptyset_2 (651X)	-	80	

Note: IRQ and NMI require 3 K pull-up resistors.

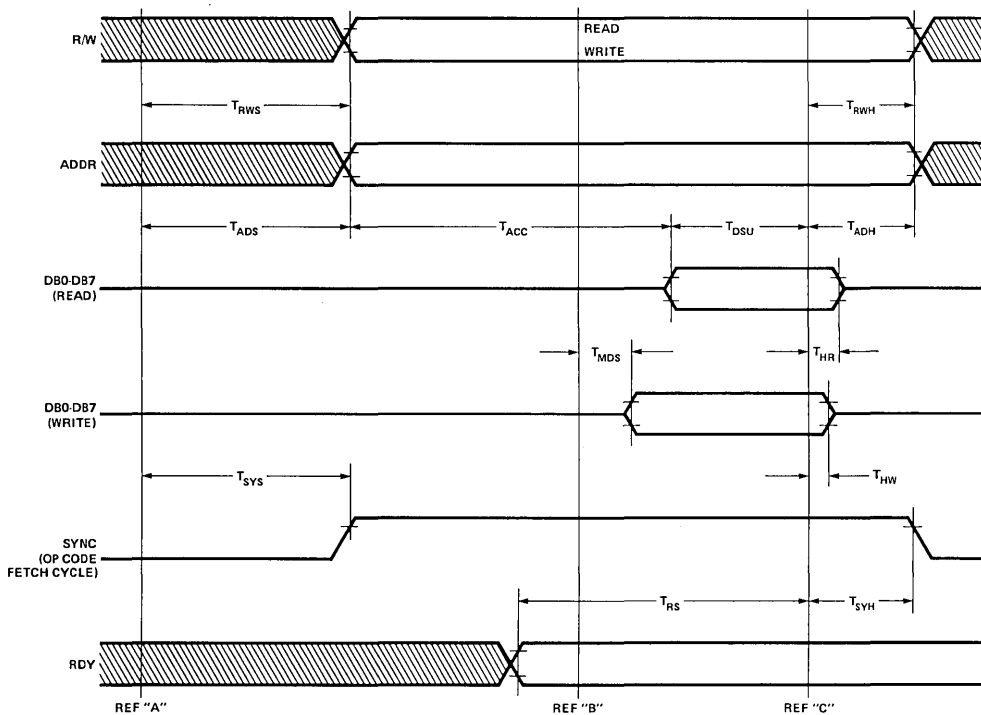
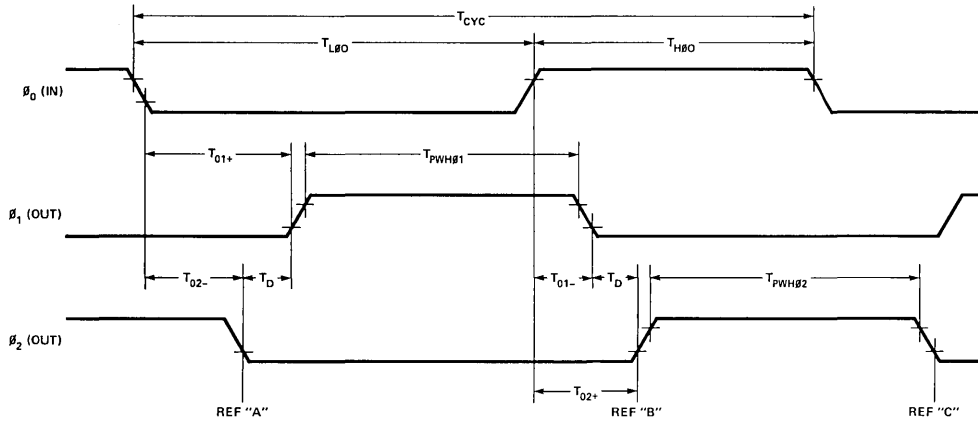


TIMING DEFINITIONS

SY651X INPUT CLOCK TIMING



SY650X INPUT CLOCK TIMING



MICRO-PROCESSORS



DYNAMIC OPERATING CHARACTERISTICS

 $(V_{CC} = 5.0 \pm 5\%, T_A = 0^\circ \text{ to } 70^\circ\text{C})$

Device Type	Parameter	Note	Symbol	1 MHz		2 MHz ^⑥		3 MHz ^⑦		Unit	
				Min.	Max.	Min.	Max.	Min.	Max.		
651X	Cycle Time		T_{CYC}	1.00	40	0.50	40	0.33	40	μs	
	θ_1 Pulse Width		$T_{PWH\theta_1}$	430	—	215	—	150	—	ns	
	θ_2 Pulse Width		$T_{PWH\theta_2}$	470	—	235	—	160	—	ns	
	Delay Between θ_1 and θ_2		T_D	0	—	0	—	0	—	ns	
	θ_1 and θ_2 Rise and Fall Times	①	T_R, T_F	0	25	0	20	0	15	ns	
650X	Cycle Time		T_{CYC}	1.00	40	0.50	40	0.33	40	μs	
	θ_0 (IN) Low Time	②	$T_{L\theta_0}$	480	—	240	—	160	—	ns	
	θ_0 (IN) High Time	②	$T_{H\theta_0}$	460	—	240	—	160	—	ns	
	θ_0 Neg to θ_1 Pos Delay	⑤	T_{01+}	10	70	10	70	10	70	ns	
	θ_0 Neg to θ_2 Neg Delay	⑤	T_{02-}	5	65	5	65	5	65	ns	
	θ_0 Pos to θ_1 Neg Delay	⑤	T_{01-}	5	65	5	65	5	65	ns	
	θ_0 Pos to θ_2 Pos Delay	⑤	T_{02+}	15	75	15	75	15	75	ns	
	θ_0 (IN) Rise and Fall Time	①	T_{RO}, T_{FO}	0	10	0	10	0	10	ns	
	θ_1 (OUT) Pulse Width		$T_{PWH\theta_1}$	$T_{L\theta_0}^{-20}$	$T_{L\theta_0}^{-10}$	$T_{L\theta_0}^{-20}$	$T_{L\theta_0}^{-10}$	$T_{L\theta_0}^{-20}$	$T_{L\theta_0}^{-10}$	$T_{L\theta_0}^{-10}$	ns
	θ_2 (OUT) Pulse Width		$T_{PWH\theta_2}$	$T_{L\theta_0}^{-40}$	$T_{L\theta_0}^{-10}$	$T_{L\theta_0}^{-40}$	$T_{L\theta_0}^{-10}$	$T_{L\theta_0}^{-40}$	$T_{L\theta_0}^{-10}$	ns	
	Delay Between θ_1 and θ_2		T_D	5	—	5	—	5	—	ns	
	θ_1 and θ_2 Rise and Fall Times	① ③	T_R, T_F	—	25	—	25	—	15	ns	
650X 651X	R/W Setup Time		T_{RWS}	—	225	—	140	—	110	ns	
	R/W Hold Time		T_{RWH}	30	—	30	—	15	—	ns	
	Address Setup Time		T_{ADS}	—	225	—	140	—	110	ns	
	Address Hold Time		T_{ADH}	30	—	30	—	15	—	ns	
	Read Access Time		T_{ACC}	—	650	—	310	—	170	ns	
	Read Data Setup Time		T_{DSU}	100	—	50	—	50	—	ns	
	Read Data Hold Time		T_{HR}	10	—	10	—	10	—	ns	
	Write Data Setup Time		T_{MDS}	—	175	—	100	—	75	ns	
	Write Data Hold Time		T_{HW}	60	—	60	—	30	—	ns	
	Sync Setup Time		T_{SYS}	—	350	—	175	—	100	ns	
	Sync Hold Time		T_{SYH}	30	—	30	—	15	—	ns	
	RDY Setup Time	④	T_{RS}	200	—	200	—	150	—	ns	

NOTES:

- ① Measured between 10% and 90% points on waveform.
- ② Measured at 50% points.
- ③ Load = 1 TTL load +30 pF.
- ④ RDY must never switch states within T_{RS} to end of θ_2 .

- ⑤ Load = 100 pF.
- ⑥ The 2 MHz devices are identified by an "A" suffix.
- ⑦ The 3 MHz devices are identified by a "B" suffix.

PIN FUNCTIONS

Clocks (Φ_1, Φ_2)

The SY651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The SY650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Clock generator circuits are shown elsewhere in this data sheet.

Address Bus (A_0 - A_{15}) (See sections on each micro for respective address lines on those devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (DB_0 - DB_7)

Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the three-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (Φ_2) clock, thus allowing data output from microprocessor only during Φ_2 . During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low. This signal is available on the SY6512, only.

Ready (RDY)

This input signal allows the user to halt the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (Φ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (Φ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If ready is low during a write cycle, it is ignored until the following read operation. Ready transitions must not be permitted during Φ_2 time.

Interrupt Request (\overline{IRQ})

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K Ω external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt (\overline{NMI})

A negative going transition on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

\overline{NMI} is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for \overline{IRQ} will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

\overline{NMI} also requires an external 3K Ω resistor to V_{CC} for proper wire-OR operations.

Inputs \overline{IRQ} and \overline{NMI} are hardware interrupts lines that are sampled during Φ_2 (phase 2) and will begin the appropriate interrupt routine on the Φ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of Φ_1 .

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during Φ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the Φ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset (\overline{RES})

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and SYNC signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Read/Write (R/W)

This output signal is used to control the direction of data transfers between the processor and other circuits on the data bus. A high level on R/W signifies data into the processor; a low is for data transfer out of the processor.

PROGRAMMING CHARACTERISTICS

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry	DEC	Decrement Memory by One	PHA	Push Accumulator on Stack
AND	"AND" Memory with Accumulator	DEX	Decrement Index X by One	PHP	Push Processor Status on Stack
ASL	Shift left One Bit (Memory or Accumulator)	DEY	Decrement Index Y by One	PLA	Pull Accumulator from Stack
				PLP	Pull Processor Status from Stack
BCC	Branch on Carry Clear	EOR	"Exclusive-or" Memory with Accumulator	ROL	Rotate One Bit Left (Memory or Accumulator)
BCS	Branch on Carry Set			ROR	Rotate One Bit Right (Memory or Accumulator)
BEQ	Branch on Result Zero	INC	Increment Memory by One	RTI	Return from Interrupt
BIT	Test Bits in Memory with Accumulator	INX	Increment Index X by One	RTS	Return from Subroutine
BMI	Branch on Result Minus	INY	Increment Index Y by One		
BNE	Branch on Result not Zero			SBC	Subtract Memory from Accumulator with Borrow
BPL	Branch on Result Plus	JMP	Jump to New Location	SEC	Set Carry Flag
BRK	Force Break	JSR	Jump to New Location Saving Return Address	SED	Set Decimal Mode
BVC	Branch on Overflow Clear	LDA	Load Accumulator with Memory	SEI	Set Interrupt Disable Status
BVS	Branch on Overflow Set	LDX	Load Index X with Memory	STA	Store Accumulator in Memory
		LDY	Load Index Y with Memory	STX	Store Index X in Memory
CLC	Clear Carry Flag	LSR	Shift One Bit Right (Memory or Accumulator)	STY	Store Index Y in Memory
CLD	Clear Decimal Mode				
CLI	Clear Interrupt Disable Bit	NOP	No Operation	TAX	Transfer Accumulator to Index X
CLV	Clear Overflow Flag	ORA	"OR" Memory with Accumulator	TAY	Transfer Accumulator to Index Y
CMP	Compare Memory and Accumulator			TSX	Transfer Stack Pointer to Index X
CPX	Compare Memory and Index X			TXA	Transfer Index X to Accumulator
CPY	Compare Memory and Index Y			TXS	Transfer Index X to Stack Pointer
				TYA	Transfer Index Y to Accumulator

ADDRESSING MODES

Accumulator Addressing

This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing

In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

Absolute Addressing

In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

Zero Page Addressing

The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

Indexed Zero Page Addressing – (X, Y indexing)

This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing – (X, Y indexing)

This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Implied Addressing

In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Relative Addressing

Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

Indexed Indirect Addressing

In indexed indirect addressing (referred to as (Indirect,X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Indirect Indexed Addressing

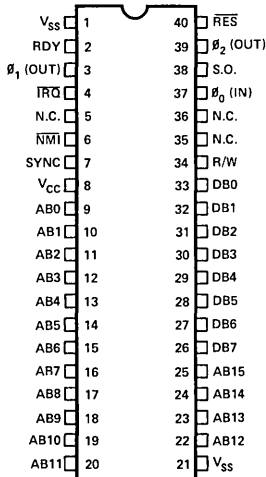
In indirect indexed addressing (referred to as (Indirect,Y)), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Absolute Indirect

The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.



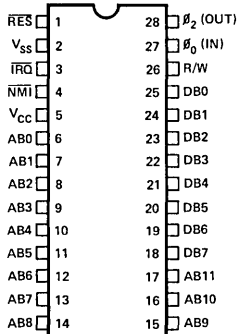
SY6502 – 40 Pin Package



Features

- 65K Addressable Bytes of Memory
- IRQ Interrupt
- NMI Interrupt
- On-the-chip Clock
 - ✓ TTL Level Single Phase Input
 - ✓ Crystal Time Base Input
- SYNC Signal (can be used for single instruction execution)
- RDY Signal (can be used for single cycle execution)
- Two Phase Output Clock for Timing of Support Chips

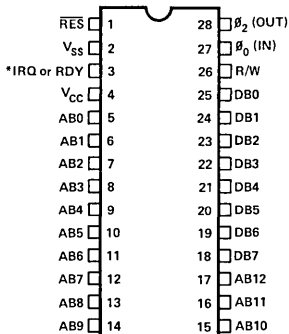
SY6503 – 28 Pin Package



Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bi-Directional Data Bus

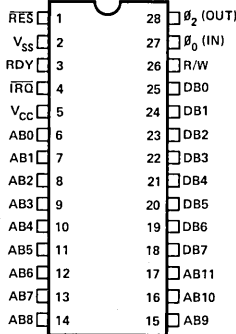
SY6504 & SY6507 – 28 Pin Package



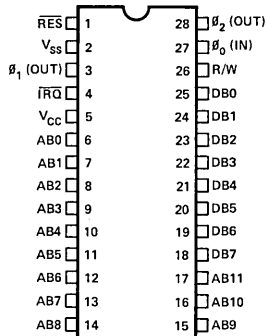
Features

- IRQ Interrupt (6504 only)
- RDY Signal (6507 only)
- 8K Addressable Bytes of Memory (AB00-AB12)
- On-the-chip Clock
- 8 Bit Bi-Directional Data Bus

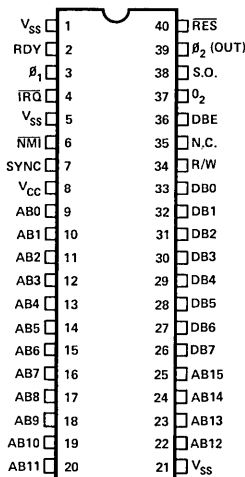
MICRO-PROCESSORS

SY6505 – 28 Pin Package

Features

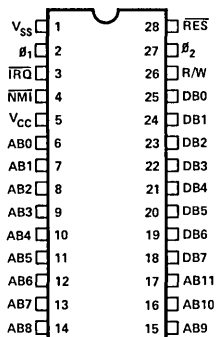
- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- $\overline{\text{IRQ}}$ Interrupt
- RDY Signal
- 8 Bit Bi-Directional Data Bus

SY6506 – 28 Pin Package

Features

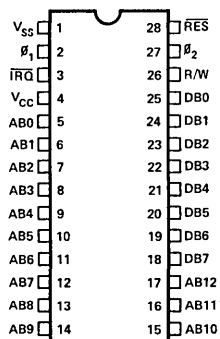
- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- $\overline{\text{IRQ}}$ Interrupt
- Two phases off
- 8 Bit Bi-Directional Data Bus

SY6512 – 40 Pin Package

Features

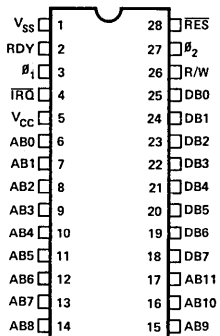
- 65K Addressable Bytes of Memory
- $\overline{\text{IRQ}}$ Interrupt
- $\overline{\text{NMI}}$ Interrupt
- RDY Signal
- 8 Bit Bi-Directional Data Bus
- SYNC Signal
- Two phase input
- Data Bus Enable

SY6513 – 28 Pin Package

Features

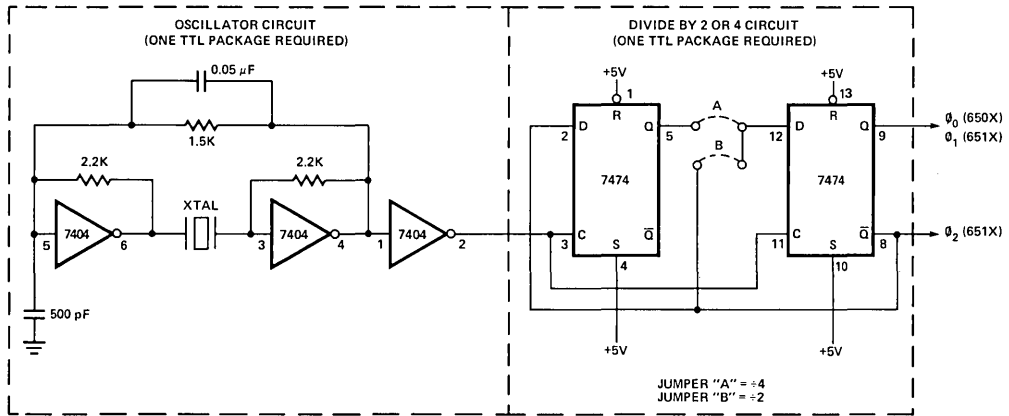
- 4K Addressable Bytes of Memory (AB00-AB11)
- Two phase clock input
- \overline{IRQ} Interrupt
- \overline{NMI} Interrupt
- 8 Bit Bi-Directional Data Bus

SY6514 – 28 Pin Package

Features

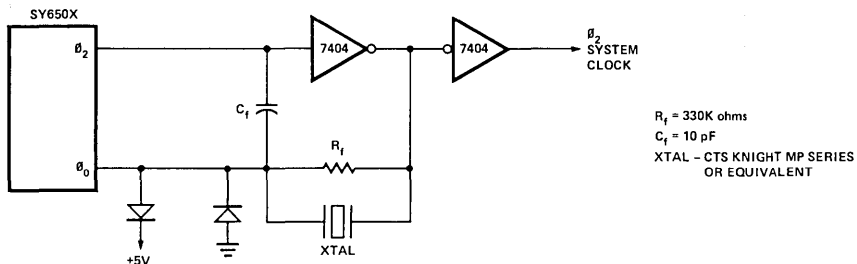
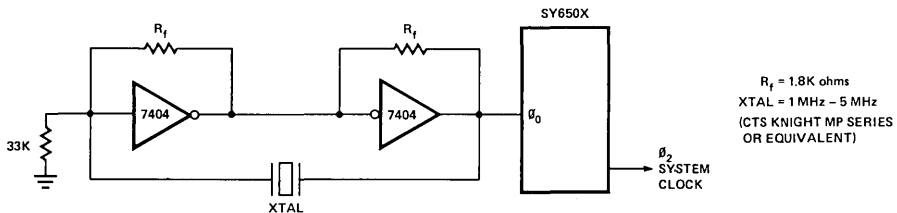
- 8K Addressable Bytes of Memory (AB00-AB12)
- Two phase clock input
- \overline{IRQ} Interrupt
- 8 Bit Bi-Directional Data Bus

SY6515 – 28 Pin Package

Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- Two phase clock input
- \overline{IRQ} Interrupt
- 8 Bit Bi-Directional Data Bus

CLOCK GENERATION CIRCUITS


CRYSTAL FREQUENCY	OUTPUT FREQUENCY	
	÷2	÷4
3.579545 MHz	1.7897 MHz	0.894886 MHz
4.194304 MHz	2.097152 MHz	1.048576 MHz


MICRO-PROCESSORS

- Single +5 volt ($\pm 5\%$) power supply.
- Separate +5 volt power pin for RAM, providing very low standby power.
- 2048 bytes of ROM.
- 64 bytes of RAM.
- 32 bi-directional I/O lines.
- 16-bit programmable interval timer/event counter.
- Five Interrupts
- Software-compatible to SY6502.
- Pipeline architecture for high-performance.
- Thirteen address modes with true indexing capability.
- Variable length stack.
- Two index registers
- 40-pin dual in-line package.
- 64-pin emulator device available for system and program development.

The SY6500/1 is a completely self-contained microcomputer system fabricated on a single chip. Included in the SY6500/1 are 2048 bytes of mask-programmable ROM, 64 bytes of RAM, 32 I/O lines, a 16-bit timer/counter, and an on-chip clock oscillator. The internal processor architecture is identical to the SY6502 to provide software compatibility and to assure high-performance operation.

PRODUCT SUPPORT

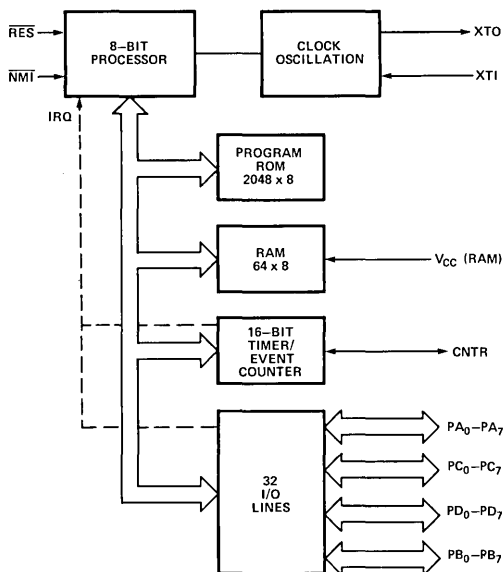
To allow prototype circuit development Synertek offers a 64 pin Emulator device. This device provides all 6500/1 interface lines plus routing the address bus, data bus, and all control lines off-chip to external memory.

Extensive hardware and software development support is available with our versatile System 65, and our personality module allows complete in-circuit user emulation of the 6500/1 microcomputer.

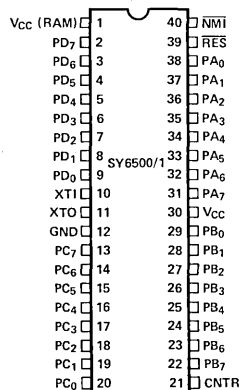
Support products available:

- System 65 Microcomputer Development System: SYS65-101
- 1 MHz personality board: M65-081
- 2 MHz personality board: M65-082
- 1 MHz Emulator Device: SYC6500/1E
- 2 MHz Emulator Device: SYC6500/1EA

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package	Frequency	Temp. Range
SY6500/1	Plastic	1 MHz	0°-70° C
SY6500/1A	Plastic	2 MHz	0°-70° C
SYC6500/1	Ceramic	1 MHz	0°-70° C
SYC6500/1A	Ceramic	2 MHz	0°-70° C

MAXIMUM RATINGS

Rating	Symbol	Allowable Range	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	V
Input/Output Voltage	V _{IN}	-0.3 to +7.0	V
Operating Temp.	T _{OP}	0 to 70	°C
Storage Temp.	T _{STG}	-55 to +150	°C

All inputs contain protection circuitry to prevent damage due to static discharge. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±5%, T_A = 0-70°C, unless otherwise noted)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{IH}	Input High Voltage	2.0	—	V _{CC}	V
V _{IL}	Input Low Voltage	-0.3	—	0.8	V
V _{IHXT}	Input High Voltage (XTL1)	2.4	—	V _{CC}	V
V _{ILXT}	Input Low Voltage (XTL1)	-0.3	—	0.4	V
I _{IN}	Input Leakage (\overline{RES} , \overline{NMI})	—	—	2.5	μA
I _{TSI}	Three-State Input Leakage (PA ₀ -PA ₇ , PB ₀ -PB ₇ , PC ₀ -PC ₇ , PD ₀ -PD ₇ , CNTR), V _{IN} = 0.4 to 2.4V	—	—	10.0	μA
V _{OH}	Output High Voltage, I _{LOAD} = 100μA	2.4	—	—	V
V _{OL}	Output Low Voltage, I _{LOAD} = 1.6mA	—	—	0.4	V
P _D	Power Dissipation	—	500	—	mW
I _{RR}	Standby Current (RAM only)	—	10	—	mA
C _{IN}	Input Capacitance (\overline{RES} , \overline{NMI})	—	—	10.0	pF
C _{TSI}	Three-State Input Capacitance (PA ₀ -PA ₇ , PB ₀ -PB ₇ , PC ₀ -PC ₇ , PD ₀ -PD ₇ , CNTR)	—	—	10.0	pF
C _{INX}	Input Capacitance (XTL1)	—	—	50.0	pF
C _{OUT}	Output Capacitance: V _{IN} = 0V, T _A = 25°C, f = 1.0 MHz	—	—	10.0	pF

ARCHITECTURE

Index Registers

There are two 8-bit index registers X and Y. They may be used to count program steps or to provide an index value, which is added to a base address to generate an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Indexing simplifies many types of programs, especially when data tables are referenced.

Stack Pointer

The Stack Pointer is an 8-bit register used to control the addressing of the Stack Memory. It is automatically decremented and incremented by the CPU whenever the Stack is accessed.

The Stack is used automatically by the CPU for interrupt processing and subroutine calling and may also be used by the programmer for other storage functions.

Arithmetic and Logic Unit (ALU)

All arithmetic and logical operations are done in the ALU. The ALU has no internal memory and is used only to perform momentary numerical operations.

Accumulator

The Accumulator is an 8-bit register which is used to hold the results of most arithmetic and logical operations.

Program Counter

The 16-bit Program Counter provides the addresses which step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher byte of the Program Counter (PCH) is placed on the high-order 8 bits. The Counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the internal data bus. These instructions are latched into the instruction register then decoded along with timing and interrupt signals to generate control signals for the various registers.

Timing Control

The Timing Control Unit keeps track of the specific instruction cycle being executed. This unit is set to T_0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

Interrupt Logic

The interrupt logic controls the processor interface to the interrupt inputs to assure proper timing, enabling and sequencing of the interrupt signals which the processor recognizes and services.

Clock Oscillator

The Clock Oscillator provides all the timing signals used by the CPU. A 2MHz crystal must be used with the 1MHz SY6500/1 and a 4MHz crystal for the 2MHz SY6500/1A.

2K x 8 ROM

The 2048 byte Read Only Memory (ROM) usually contains the program instructions and other fixed constants. These program instructions and constants are permanently stored in the ROM by metal mask programming during fabrication of the SY6500/1.

64 x 8 RAM

The 64-byte Random Access Memory (RAM) contains the user program stack and is used for scratchpad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic re-

fresh. A standby power pin allows RAM memory to be maintained at a reduced operating power. In the event that power is lost and execution stops, this standby power retains RAM data until execution resumes.

Status/Control Register

The 8-bit status/control register controls and reports the status of eight signals — five control signals and three status signals.

Counter/Latch

The counter/latch consists of a 16-bit counter and a 16-bit latch register. The counter contains either a count of $\phi 2$ clock periods or a selected external event, depending on the counter mode selected in the status control register. The latch contains the counter initialization value.

Input/Output (I/O) Ports

The SY6500/1 provides four 8-bit I/O ports — PA, PB, PC, PD. The 32 I/O lines of the I/O ports are completely bidirectional; all signals may be used for either input or output. (See page 7 "Hardware Details" for further details and mask options).

INSTRUCTION SET

The SY6500/1 can execute a wide range of instructions. The instructions can be divided into the following groups:

- Transfer and Load
- Arithmetic and Logic
- Rotate and Shift
- Stack Manipulation
- Bit Manipulation (set, reset, test)
- Jumps, Calls and Returns

The following tables summarize the various instructions and their functions, by group:


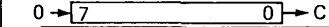
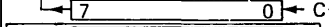
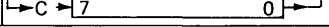
TRANSFER AND LOAD GROUP

Operation	Mnemonic	Function
Load Accumulator with Memory	LDA	M → A
Load Index X with Memory	LDX	M → X
Load Index Y with Memory	LDY	M → Y
Store Accumulator in Memory	STA	A → M
Store Index X in Memory	STX	X → M
Store Index Y in Memory	STY	Y → M
Transfer Accumulator to Index X	TAX	A → X
Transfer Accumulator to Index Y	TAY	A → Y
Transfer Stack Pointer to Index X	TSX	S → X
Transfer Index X to Accumulator	TXA	X → A
Transfer Index Y to Accumulator	TYA	Y → X
Transfer Index X to Stack Register	TXS	X → S

ARITHMETIC AND LOGIC GROUP

Operation	Mnemonic	Function
Add Memory to Accumulator with Carry	ADC	$A+M+C \rightarrow A$
AND Memory with Accumulator	AND	$A \wedge M \rightarrow A$
Compare Memory and Accumulator	CMP	$A-M$
Compare Memory and Index X	CMX	$X-M$
Compare Memory and Index Y	CMY	$Y-M$
Decrement Memory by One	DEC	$M-1 \rightarrow M$
Decrement Index X by One	DEX	$X-1 \rightarrow X$
Decrement Index Y by One	DEY	$Y-1 \rightarrow Y$
Exclusive-Or Memory with Accumulator	EOR	$A \vee M \rightarrow A$
Increment Memory by One	INC	$M+1 \rightarrow M$
Increment Index X by One	INX	$X+1 \rightarrow X$
Increment Index Y by One	INY	$Y+1 \rightarrow Y$

ROTATE AND SHIFT GROUP

Operation	Mnemonic	Function
Shift Left One Bit (Memory or Accumulator)	ASL	
Shift Right One Bit (Memory or Accumulator)	LSR	
Rotate One Bit Left (Memory or Accumulator)	ROL	
Rotate One Bit Right (Memory or Accumulator)	ROR	

STACK MANIPULATION GROUP

Operation	Mnemonic	Function
Push Accumulator on Stack	PHA	$A \rightarrow Ms, S-1 \rightarrow S$
Push Processor Status on Stack	PHP	$P \rightarrow Ms, S-1 \rightarrow S$
Pull Accumulator from Stack	PLA	$S+1 \rightarrow S, Ms \rightarrow A$
Pull Processor Status from Stack	PLP	$S+1 \rightarrow S, Ms \rightarrow P$

BIT MANIPULATION GROUP

Operation	Mnemonic
Branch on Carry Clear	BCC
Branch on Carry Set	BCS
Branch on Result Zero	BEQ
Test Bits in Memory with Accumulator	BIT
Branch on Result Minus	BMI
Branch on Result not Zero	BNE
Branch on Result Plus	BPL
Branch on Overflow Clear	BVC
Branch on Overflow Set	BVS
Clear Carry Flag	CLC
Clear Decimal Mode	CLD
Clear Interrupt Disable Bit	CLI
Clear Overflow Flag	CLV
Set Carry Flag	SEC
Set Decimal Mode	SED
Set Interrupt Disable Status	SEI

JUMPS, CALLS, RETURNS GROUP

Operation	Mnemonic	Function
Force Break	BRK	
Jump to New Location	JMP	
Jump to New Location Saving Return Address	JSR	Jump to subroutine
Return from Interrupt	RTI	
Return from Subroutine	RTS	

ADDRESSING MODES

Accumulator Addressing

This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing

In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

Absolute Addressing

In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

Zero Page Addressing

The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

Indexed Zero Page Addressing (X, Y Indexing)

This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing (X, Y Indexing)

This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Implied Addressing

In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Relative Addressing

Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

Indexed Indirect Addressing

In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Indirect Indexed Addressing

In indirect indexed addressing [referred to as ((Indirect, Y))], the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Absolute Indirect

The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

EXPLANATION OF SYMBOLS

Legend	Meaning
A	Accumulator
X, Y	Index Registers
M	Memory
P	Processor Status Register
S	Stack Pointer
+	Add
^	Logical AND
-	Subtract
⊕	Logical Exclusive OR
→, ←	Transfer to

HARDWARE DETAILS
Memory Address Map

Figure 1 indicates the internal memory address assignments for the SY6500/1.

Peripheral I/O Ports (PA, PB, PC, PD)

These four 8-bit ports can be used for either input or output functions. There are no direction registers associated with any of these ports so care must be used to always leave the pins which are to be used as inputs in the off (high) state. Each port consists of an active transistor to V_{SS} and a "passive" pull-up transistor to +5.

NOTE: These pull-up devices may be deleted as a mask option in 8-bit groups for dedicated input functions or cases in which the pull-up is to be located external to the SY6500/1.

Each output pin on the four ports is capable of sinking 1 TTL load (1.6 ma. at $V_O = 0.4$ volts max). When an output is "off", it is pulled high (to +5 volts) by a "load resistor" (pull-up transistor) of approximately 6 - 8K ohms.

All four ports are located in the processor's "zero-page" memory area and thus may be serviced very quickly with simple two-byte instructions.

The two lower bits of the PA port (PA1 and PA0) also serve as edge sensing inputs for generating IRQ interrupt.

Edge Detect Capability (PA0, PA1)

The two LSB's of the PA port, PA1 and PA0, function as edge detecting inputs in addition to their normal input/output functions. The minimum pulse width that can be detected at these inputs is twice the period of the $\phi 2$ clock. For example, with $\phi 2 = 1$ MHz, the input pulse should be 2 microseconds or longer.

PA0 will detect an asynchronous rising edge and set bit 6 in the I/O status register. This bit can be cleared by attempting to write any data to the CLEAR INTO Address (89 hex).

PA1 will detect an asynchronous falling edge and set bit 5 in the I/O status register. This bit can be cleared by attempting to write any data to the CLEAR INT1 Address (8A hex).

Non-Maskable Interrupt (\overline{NMI})

This input is identical to the similarly named pin in the SY6502. It provides fast falling edge sensitive interrupt service for high priority events such as power fail. NMI vector location is FFA and FFB.

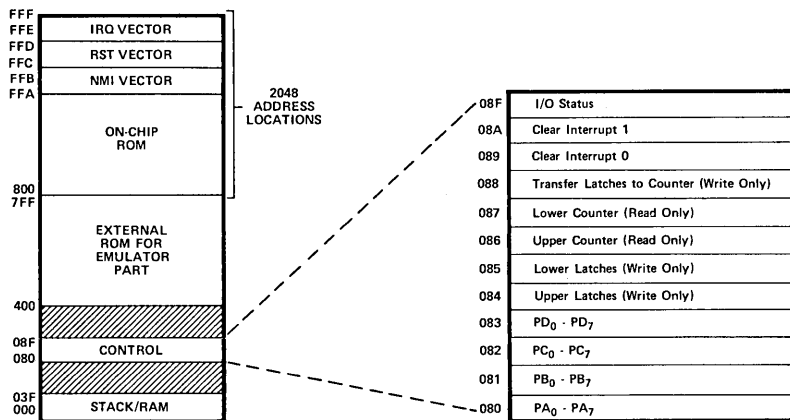


Figure 1. Memory Map

MICRO-PROCESSORS

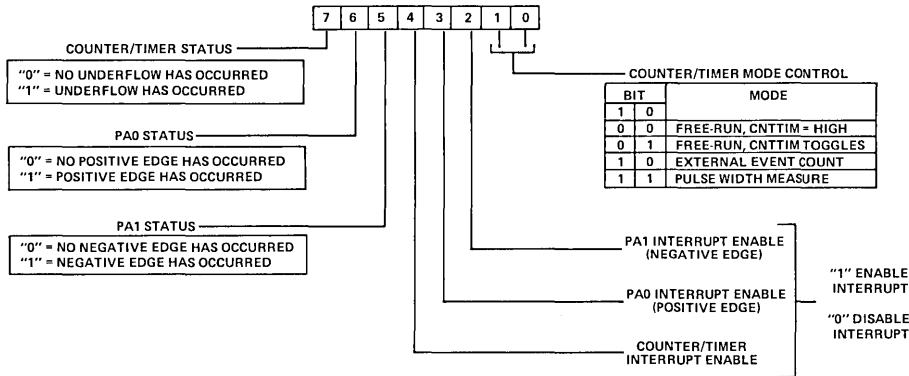


Figure 2. I/O Status Register

I/O STATUS REGISTER

The I/O STATUS REGISTER is the zero page memory byte located at address 8F (hex). This register consists of timer underflow status (bit 7), edge detect input status (bits 6 and 5), interrupt enables (bits 4, 3 and 2), and timer mode controls (bits 1 and 0).

The timer underflow bit will be set each time the counter underflows in any of the four possible modes. This bit is cleared to a logic '0' at reset (power on). However, since the counter and latch are not initialized by \overline{RES} , this bit could be at a logic '1' state very quickly after \overline{RES} goes to a logic '1'.

Status register bits 5 and 6 reflect the history on the edge detecting inputs (PA1 and PA0). Bit 5 will be set any time a falling edge occurs on PA1 and bit 6 will be set by a rising edge on PA0. Note that this condition can also be a result of these parts being used as outputs, since the edge detecting circuitry is sensitive to any activity on this pin regardless of the source.

The interrupt enable bits (4, 3, and 2) can be set to '1' to enable any of the three possible interrupt sources or cleared to '0' to mask the associated interrupt activity.

The two mode bits (1 and 0) control the timer counter operating modes; they are both initialized to '0' at power on. The counter timer modes are more fully explained in a later paragraph.

IRQ Generation

An IRQ request can be initiated by any or all of three potential sources. These sources are all software maskable via the use of the appropriate interrupt enable bits in the I/O status register.

One of the interrupt sources is the counter/timer underflow indicator. Whenever the underflow status bit is set due to an underflow condition in the counter register

(transition from 0000 → FFFF), an internal IRQ Request will be made if appropriate interrupt enable bit (bit 4) in the I/O status register has been set.

The other two interrupt sources are the edge detecting inputs (PA1 and PA0). If a rising (PA0) or falling (PA1) edge is detected at either of these inputs, and their associated interrupt enable bit has been set (bit 3 for PA0 or bit 2 for PA1) an internal IRQ Request will be generated.

In all three cases, the IRQ Request is a result of logical 'OR' function of the logical 'AND' of each of the potential interrupting sources and their respective interrupt enable bits. Multiple simultaneous interrupts will cause the IRQ Request to remain active until all interrupting conditions have been serviced and cleared. IRQ vector location FFE and FFF.

Counter-Timer

The counter-timer consists of a 16-bit counter and a 16-bit latch. The two 8-bit halves of the counter (UC, LC) are loaded only via a download from the dual 8-bit latch (UL, LL). The latches are two zero page "write-only" locations and the counter consists of two "read-only" zero page locations.

1. Free Run Modes (Modes 00 and 01)

There are two free-run timer modes. In both of these modes the counter decrements by 1 for each internal $\phi 2$ clock cycle. In mode 00 the counter timer I/O pin (CNTR) is in the high state continuously (output disabled). Power-on reset (\overline{RES} low) forces the counter timer status bits into this mode.

Mode 01 will cause the CNTR I/O port to toggle on each counter underflow; it will also toggle each time a write to address 88 occurs (A → UL; UL, LL → UC, LC). This mode can be used to generate symmetric or asymmetric output waveforms. A one-shot mode can

also be synthesized by changing from mode 01 (output enabled) to mode 00 (output high) after only one occurrence of the output toggle condition.

2. External Event Count Mode (Mode 10)

Mode 10 causes the counter to decrement each time a rising edge is detected on the CNTR pin. The maximum rate at which these edges can be detected is one-half the internal $\phi 2$ clock rate.

3. Pulse Width Measurement Mode (Mode 11)

This mode (11) enables the measurement of negative pulses. The counter will count internal $\phi 2$ clocks as long as the CNTR pin is in the low state (<0.8V). If the CNTR pin is left unconnected, this mode may be used to stop the counter since the internal pull-up device will cause the input to be in the high (>2.0V) state.

In all of the counter/timer modes, the counter is automatically reloaded with the contents of the latch after each counter underflow from 0000, i.e., the counter will go from 0000 to UL, LL (not FFFF). The most significant bit (7) of the I/O status register will be set each time the counter/timer underflows. This bit can be cleared by either reading the lower eight bits of the counter/timer or by loading the upper eight bits of the latch with address 88 (hex). Accessing this address also causes the latch to download to the counter.

Power-On Reset Considerations

The occurrence of $\overline{\text{RES}}$ going from low to high will cause the SY6500/1 to set the interrupt mask bit in the processor status register and will initiate a reset vector fetch to begin program execution. All of the peripheral I/O ports (PA, PB, PC, PD) and CNTR I/O will be set to the off (high) state. The I/O status register will be cleared to 00 (hex), thus selecting timer mode 00, and resetting all interrupt enable bits. (Reset vector location is FFC and FFD).

NOTE: Neither the latch nor counter are initialized with RESET.

SY6500/1E Emulator Version (64 Pin Device)

The SY6500/1E is provided to permit simplified software development and construction of prototype systems. All capabilities of the 40-pin SY6500/1 are also retained in the SY6500/1E, except there is no mask-programmable ROM in the latter. Instead, the internal Address Bus (A0-A11), Data Bus (DB0-DB7), and Control Bus ($\phi 2$, R/W, RDY, SYNC) are provided so that external 2708/2716 EPROM or other PROM's for the 2 MHz version of the emulator, may be used for development.

A typical prototype system may require as few as two components — the SY6500/1E and 2716 or 2708. The electrical characteristics of the I/O lines are identical to the final 40-pin device, ensuring a smooth transition from prototype to production. Software characteristics

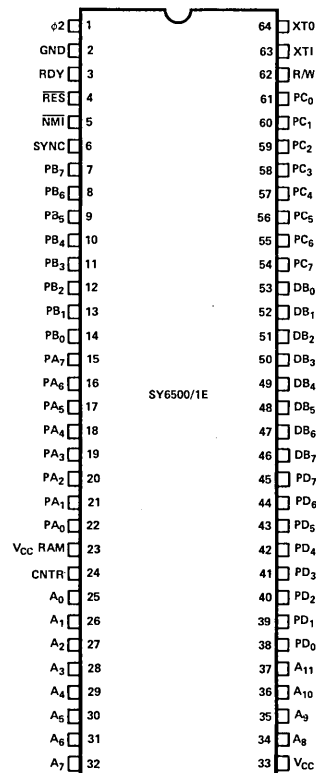
are also identical, except for the fact that the program memory is external in the prototype system. All timing, addressing, and program commands are identical.

Since the Address Bus (12 lines) is available on the SY6500/1E, this permits using up to 3K bytes of program storage (400-FFF in hex) available for prototyping. Thus, a large program may be utilized for system check-out and a reduced version for the production system. This would permit a gradual reduction or compression of the program during the development phase.

The remaining addresses, 000-3FF, contain four pages of memory (each page being 256 bytes). It is possible to use part of this address space for additional program storage, as long as the page zero addresses used for I/O and RAM are not utilized. Processor read operations from page zero addresses are internal to the SY6500/1E and do not use the Data Bus at all. This ensures proper I/O and RAM functioning, independent of the external configuration.

SY6500/1E Pin-Outs

The pin assignments for the 64-pin emulator device are shown below:





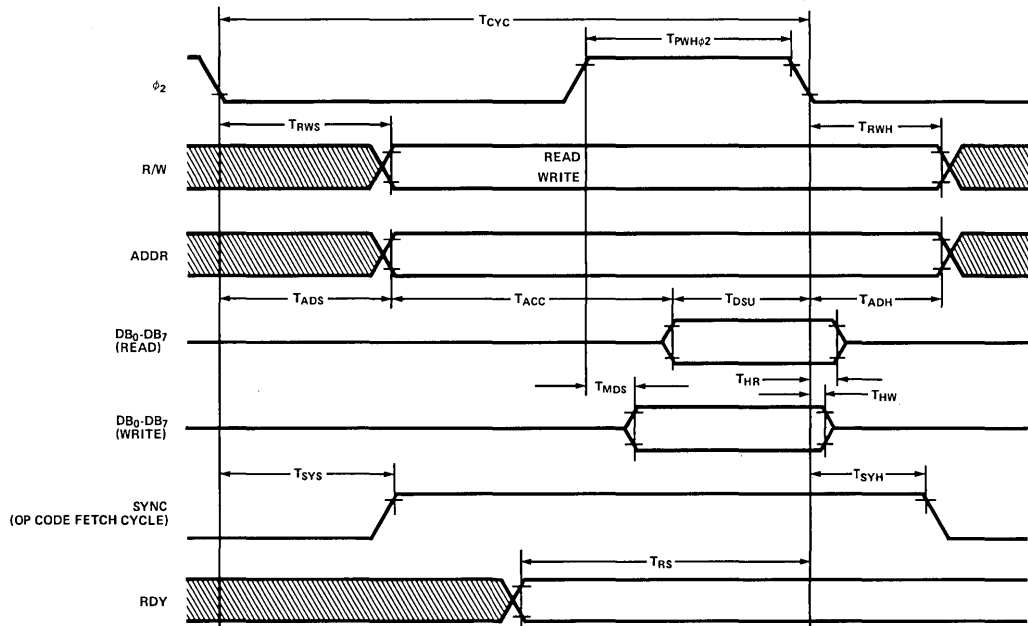
SY6500/1E – EMULATOR TIMING CHARACTERISTICS

(V_{CC} = 5.0 ± 5%, T_A = 0-70°C)

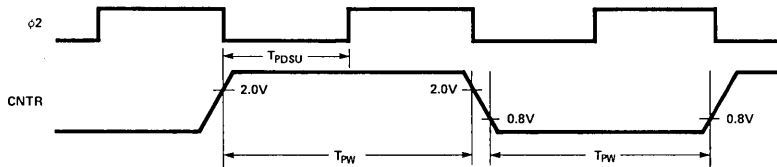
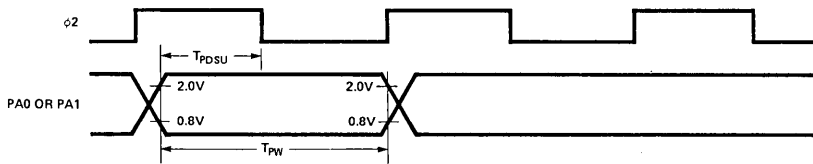
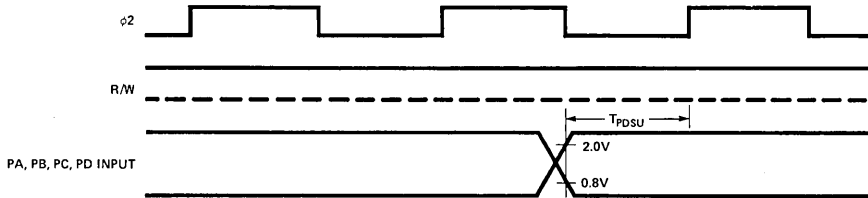
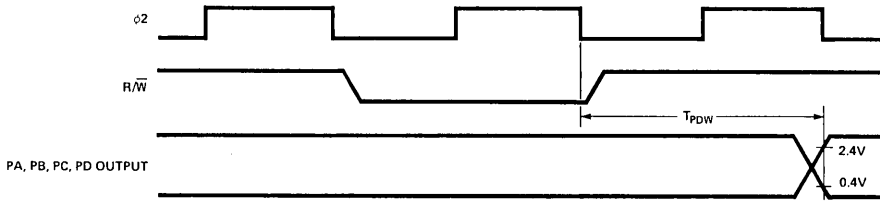
Symbol	Parameter	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
T _{CYC}	Cycle Time	1.00	40	0.50	40	μs
T _{PWHφ2}	φ2 Pulse Width	470	—	235	—	ns
T _R , T _F	φ2 Rise and Fall Times ^[1]	—	25	—	25	ns
T _{RWS}	R/W Setup Time	—	300	—	150	ns
T _{RWH}	R/W Hold Time	30	—	30	—	ns
T _{ADS}	Address Setup Time	—	300	—	150	ns
T _{ADH}	Address Hold Time	30	—	30	—	ns
T _{ACC}	Read Access Time	—	575	—	300	ns
T _{DSU}	Read Data Setup Time	100	—	50	—	ns
T _{HR}	Read Data Hold Time	10	—	10	—	ns
T _{MDS}	Write Data Setup Time	—	200	—	100	ns
T _{HW}	Write Data Hold Time	30	—	30	—	ns
T _{SYS}	Sync Setup Time	—	350	—	175	ns
T _{SYH}	Sync Hold Time	30	—	30	—	ns
T _{RS}	RDY Setup Time ^[2]	200	—	200	—	ns

- NOTES: 1. Measured between 10% and 90% points on waveform
 2. RDY must never switch states within T_{RS} of end of φ2.

SY6500/1E – READ/WRITE TIMING



MICRO-PROCESSORS

TIMING CHARACTERISTICS (PORTS AND COUNTER)

TIMING CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$

Symbol	Parameter	1MHz		2MHz		Unit
		Min.	Max.	Min.	Max.	
T_{CYC}	XTL1 Input Clock Cycle Time	0.500	5.0	0.250	5.0	μsec
T_{PDW}	Internal Write to Peripheral Data Valid	1.0	—	0.5	—	μsec
T_{PDSU}	Peripheral Data Setup Time	400	—	200	—	nsec
T_{PW}	Count and Edge Detect Pulse Width	1.0	—	0.5	—	μsec

MICRO-PROCESSORS

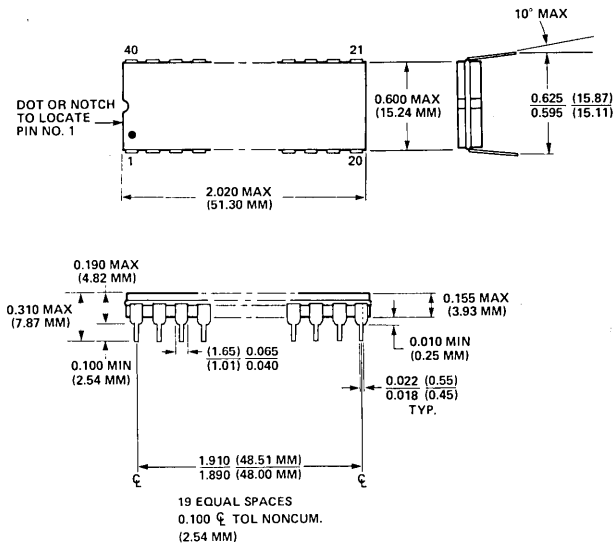
SY6500/1 Mask ROM Input Format

The Synertek SY6500/1 one-chip microcomputer provides 2048 x 8 bits of mask programmable ROM. Synertek uses computer-aided techniques to generate and test the ROM bit patterns. The customer patterns can be provided on every media including: 80-column punched cards, paper tape, 2708/2716 EPROMs, as well as a System 65 Floppy Diskette.

Details on these formats can be found in Synertek Technical Note SY6500/1 ROM Programming Input Formats. Copies of this Technical Note are available from Synertek on request.

Acceptable Formats are:

- System 65 Assembler Output on mini-floppy diskette
- Synertek Data Card Format
- Intel Data Card Format
- Intel Hex
- AMI ASCII Hex Format
- EA Data Card Format
- MOS Technology Hex Interface File Format
- Intel BPNF
- ASCII BPNF
- Binary Format

PACKAGING DIAGRAM


NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation.

40 LEAD PLASTIC DUAL IN-LINE PACKAGE

MICRO-PROCESSORS

SY6500/1 Customer Specification Form

1. Date: _____
2. Customer Name: _____
3. Customer Part No. (maximum 10 digits) _____
4. Synertek "C" Number _____
5. Customer Contact: _____
6. Customer Phone Number: _____
7. ROM Start and Stop Address in Submitted Media (Tapes, Cards, Diskette).
ROM Data Start Address is: _____ (min = 800)
(Three hexadecimal digits)
ROM Data Stop Address is: _____ (max = FFF)
(Three hexadecimal digits)
8. External Frequency Reference is: _____

C = Crystal or Clock
 R = RC Network
9. Specify I/O Port Internal Pullup Resistance Option
 - a. I/O Port A Internal Pullups are to be deleted _____ (Y or N)
 - b. I/O Port B Internal Pullups are to be deleted _____ (Y or N)
 - c. I/O Port C Internal Pullups are to be deleted _____ (Y or N)
 - d. I/O Port D Internal Pullups are to be deleted _____ (Y or N)
10. Customer's Input

<input type="checkbox"/> Punched Cards	<input type="checkbox"/> 2716 EPROM
<input type="checkbox"/> Punched Tape	<input type="checkbox"/> System 65 Mini-floppy
<input type="checkbox"/> 2708 EPROM	<input type="checkbox"/> Other (specify) _____
11. Fill code to be used for unused ROM locations is: _____
(Two hexadecimal digits)
12. Data Format

<input type="checkbox"/> Synertek Data Card	13. Logic Format
<input type="checkbox"/> Intel Hex	<input type="checkbox"/> Positive
<input type="checkbox"/> BPNF	<input type="checkbox"/> Negative
<input type="checkbox"/> Binary	
<input type="checkbox"/> System 65 Assembler	14. Verification Status
<input type="checkbox"/> MOS Technology	<input type="checkbox"/> Hold
<input type="checkbox"/> AMI ASCII Hex	<input type="checkbox"/> Not Required
<input type="checkbox"/> EA Data Card	
<input type="checkbox"/> ASCII BPNF	
<input type="checkbox"/> Intel Data Card	



Peripheral Interface Adapter (PIA)

SY6520 SY6520A

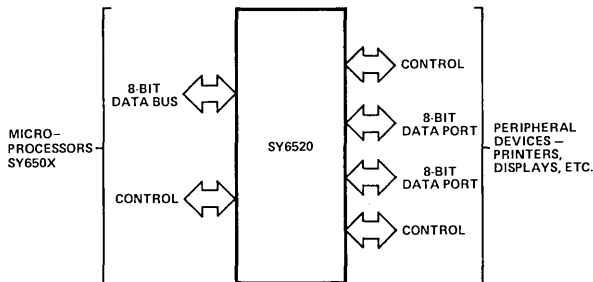
MICROPROCESSOR PRODUCTS

- Direct Replacement for MC6820
- Single +5V Power Supply
- Two 8-bit Bi-directional I/O Ports with Individual Data Direction Control
- CMOS-Compatible Peripheral Control Lines
- Automatic "Handshake" Control of Data Transfers
- Programmable Interrupt Capability
- Automatic Initialization on Power Up
- 1 and 2 MHz Versions

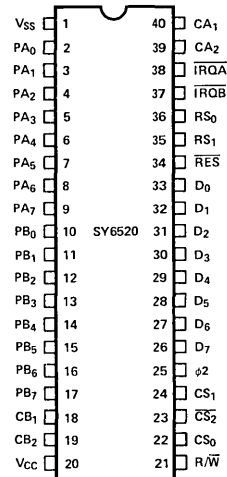
The SY6520 Peripheral Interface Adapter (PIA) is designed to provide a broad range of peripheral control to microcomputer systems. Control of peripheral devices is accomplished through two 8-bit bi-directional

I/O ports. Each I/O line may be programmed to be either an input or an output. In addition, four peripheral control lines are provided to perform "handshaking" during data transfers.

BASIC SY6520 INTERFACE DIAGRAM



PIN ASSIGNMENTS



ORDERING INFORMATION

Part Number	Package	Speed
SYC6520	Ceramic	1 MHz
SYP6520	Plastic	1 MHz
SYC6520A	Ceramic	2 MHz
SYP6520A	Plastic	2 MHz

MICRO PROCESSORS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{in}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0$, $T_A = 0-70^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	+2.0	V_{CC}	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Input Leakage Current ($V_{IN} = 0$ to 5.0 V R/W, Reset, RS_0 , RS_1 , CS_0 , CS_1 , $\overline{CS_2}$, CA_1 , CB_1 , ϕ_2)	I_{IN}	-	± 2.5	μA
Three-State (Off State Input Current) ($V_{IN} = 0.4$ to 2.4 V, $V_{CC} = \text{max}$), D_0 - D_7 , PB_0 - PB_7 , CB_2)	I_{TSI}	-	± 10	μA
Input High Current ($V_{IH} = 2.4$ V), PA_0 - PA_7 , CA_2)	I_{IH}	100	-	μA
Input Low Current ($V_{IL} = 0.4$ V), PA_0 - PA_7 , CA_2)	I_{IL}	-	-1.6	mA
Output High Voltage ($V_{CC} = \text{min}$, $I_{OH} = -100 \mu\text{A}$)	V_{OH}	2.4	-	V
Output Low Voltage ($V_{CC} = \text{min}$, $I_{OL} = -1.6\text{mA}$)	V_{OL}	-	+0.4	V
Output High Current (Sourcing) ($V_{OH} = 2.4$ V) ($V_O = 1.5$ V, the current for driving other than TTL, e.g., Darlington Base), PB_0 - PB_7 , CB_2)	I_{OH}	-100	-	μA
		-1.0	-10	mA
Output Low Current (Sinking) ($V_{OL} = 0.4$ V)	I_{OL}	1.6	-	mA
Output Leakage Current (Off-State), \overline{IRQA} , \overline{IRQB}	I_{OFF}	-	10	μA
Power Dissipation	P_D	-	500	mW
Input Capacitance ($V_{IN} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz) D_0 - D_7 , PA_0 - PA_7 , PB_0 - PB_7 , CA_2 , CB_2 R/W, Reset, RS_0 , RS_1 , CS_0 , CS_1 , CS_2 , CA_1 , CB_1 , ϕ_2)	C_{IN}	-	10	pF
		-	7.0	
		-	20	
Output Capacitance ($V_{IN} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz)	C_{OUT}	-	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

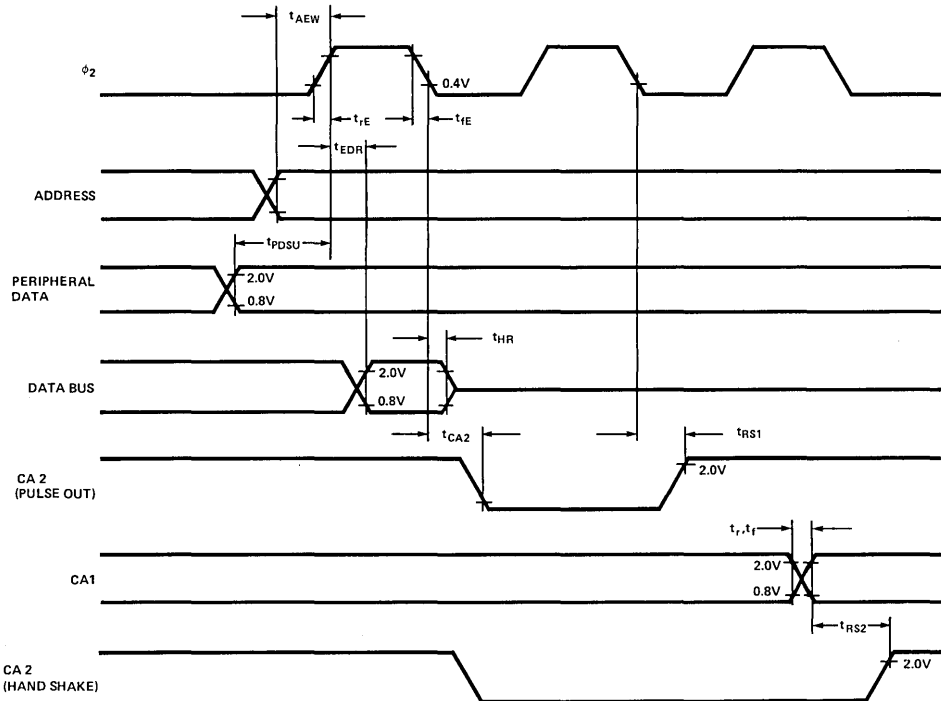


Figure 1. Read Timing Characteristics

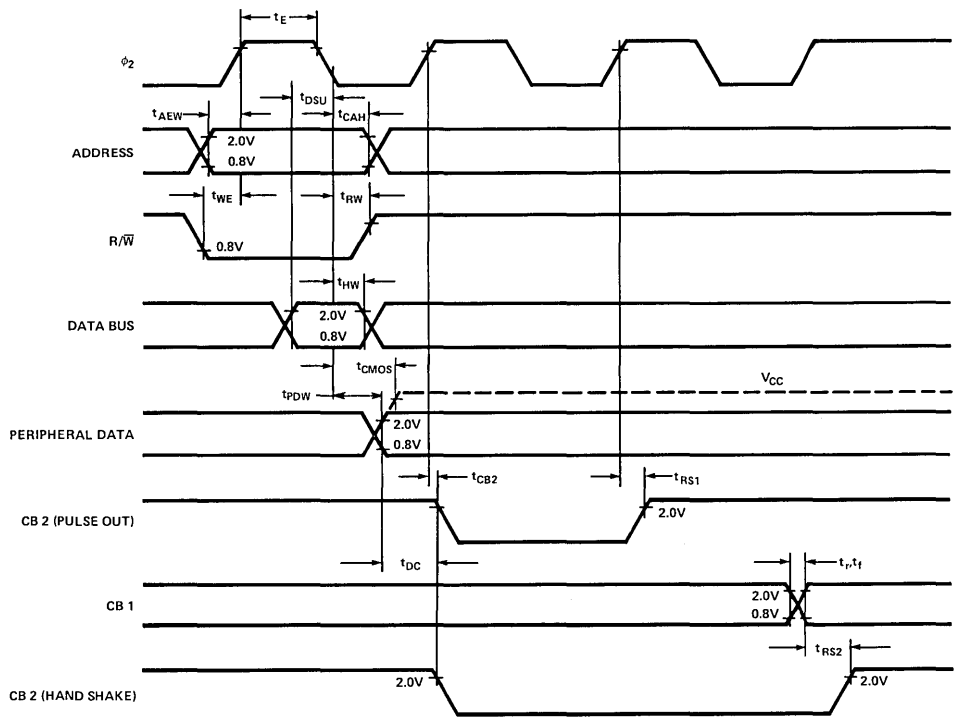


Figure 2. Write Timing Characteristics

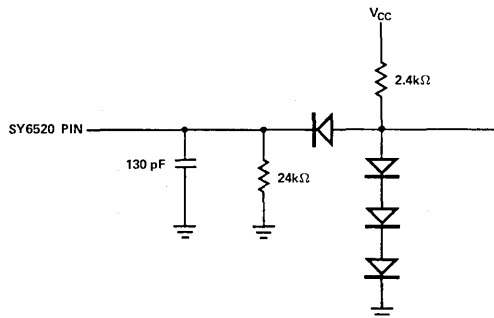
MICRO-PROCESSORS



SWITCHING CHARACTERISTICS ($V_{CC} = +5V \pm 5\%$, $T_A = 0-70^\circ C$, unless otherwise noted)

Characteristic	Symbol	SY6520 (1 MHz)		SY6520A (2 MHz)		Unit
		Min.	Max.	Min.	Max.	
READ TIMING CHARACTERISTICS						
Delay Time, Address Valid to ϕ_2 Positive Transition	T_{AEW}	180	—	90	—	ns
Delay Time, ϕ_2 Positive Transition to Data Valid on Bus	T_{EDR}	—	395	—	190	ns
Peripheral Data Setup Time	T_{PDSU}	300	—	150	—	ns
Data Bus Hold Time	T_{HR}	10	—	10	—	ns
Delay Time, ϕ_2 Negative Transition to CA2 Negative Transition	T_{CA2}	—	1.0	—	0.5	μs
Delay Time, ϕ_2 Negative Transition to CA2 Positive Transition	T_{RS1}	—	1.0	—	0.5	μs
Rise and Fall Time for CA1 and CA2 Input Signals	t_r, t_f	—	1.0	—	0.5	μs
Delay Time from CA1 Active Transition to CA2 Positive Transition	T_{RS2}	—	2.0	—	1.0	μs
Rise and Fall Time for ϕ_2 Input	t_{rE}, t_{fE}	—	25	—	25	ns
WRITE TIMING CHARACTERISTICS						
ϕ_2 Pulse Width	T_E	0.470	25	0.235	25	μs
Delay Time, Address Valid to ϕ_2 Positive Transition	T_{AEW}	180	—	90	—	ns
Delay Time, Data Valid to ϕ_2 Negative Transition	T_{DSU}	300	—	150	—	ns
Delay Time, Read/Write Negative Transition to ϕ_2 Positive Transition	T_{WE}	130	—	65	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Delay Time, ϕ_2 Negative Transition to Peripheral Data Valid	T_{PDW}	—	1.0	—	0.5	μs
Delay Time, ϕ_2 Negative Transition to Peripheral Data Valid CMOS ($V_{CC} - 30\%$) PA0-PA7, CA2	T_{CMOS}	—	2.0	—	1.0	μs
Delay Time, ϕ_2 Positive Transition to CB2 Negative Transition	T_{CB2}	—	1.0	—	0.5	μs
Delay Time, Peripheral Data Valid to CB2 Negative Transition	T_{DC}	0	1.5	0	0.75	μs
Delay Time, ϕ_2 Positive Transition CB2 Positive Transition	T_{RS1}	—	1.0	—	0.5	μs
Rise and Fall Time for CB1 and CB2 Input Signals	t_r, t_f	—	1.0	—	0.5	μs
Delay Time, CB1 Active Transition to CB2 Positive Transition	T_{RS2}	—	2.0	—	1.0	μs
Delay Time, ϕ_2 Negative Transition to Read/Write Positive Transition	T_{RW}	50	—	25	—	ns

TEST LOAD



MICRO-PROCESSORS



INTERFACE SIGNAL DESCRIPTION

RES (Reset)

This signal is used to initialize the PIA. A low signal on the RES input causes all internal registers to be cleared.

φ₂ (Input Clock)

This input is the system φ₂ clock and is used to trigger all data transfers between the microprocessor and the PIA.

R/W (Read/Write)

This signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/W signal permits the processor to read data supplied by the PIA; a low on the R/W signal permits the processor to Write into the PIA.

IRQA, IRQB (Interrupt Requests)

IRQA and IRQB are interrupt lines generated by the PIA for ports A and B respectively. These signals are active low signals and have open-drain outputs, thus allowing multiple IRQ signals from multiple PIA's to be wire-ORed together before connecting to the processor IRQ signal input.

D₀-D₇ (Data Bus)

These eight data bus lines are used to transfer data information between the processor and the PIA. These signals are bi-directional and are normally high-impedance except when selected for a read operation.

CS1, CS2, CS3 (Chip Selects)

The PIA is selected when CS1 and CS2 are high and CS3 is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits.

RS0, RS1 (Register Selects)

These two signals are used to select the various registers inside the PIA.

INTERNAL ARCHITECTURE

The SY6520 is organized into two independent sections referred to as the "A Side" and the "B Side." Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control and the buffers necessary to drive the Peripheral Interface buses. Figure 3 is a block diagram of the SY6520.

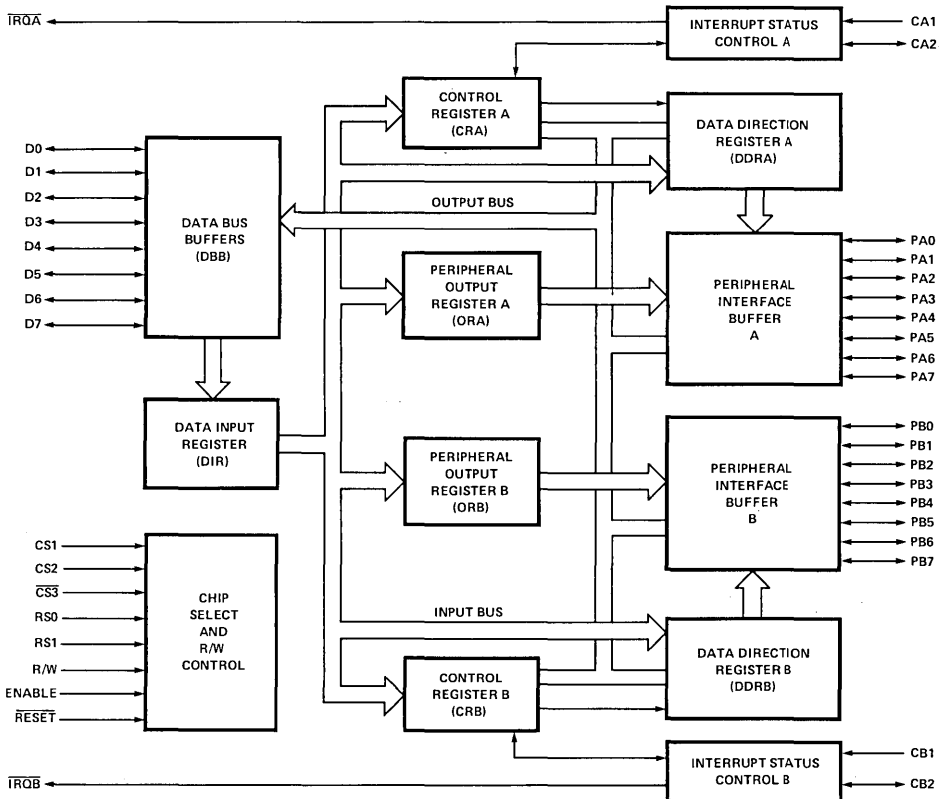


Figure 3. SY6520 Block Diagram

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	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
	7	6	5	4	3	2	1	0
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB2 Control	

Figure 4. Control Registers

Data Input Register

When the microprocessor writes data into the SY6520, the data which appears on the data bus during the Phase Two clock pulse is latched into the Data Input Register. It is then transferred into one of six internal registers of the SY6520 after the trailing edge of Phase Two. This assures that the data on the peripheral output lines will make smooth transitions from high to low or from low to high and the voltage will remain stable except when it is going to the opposite polarity.

Control Registers (CRA and CRB)

Figure 4 illustrates the bit designation and functions in the Control Registers. The Control Registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) are provided in each control register to indicate the status of the interrupt input lines (CA1, CA2, CB1, CB2). These interrupt status bits (IRQA1, IRQB1) are normally interrogated by the microprocessor during the interrupt service routine to determine the source of an active interrupt. These are the interrupt lines which drive the interrupt input (\overline{IRQ} , \overline{NMI}) of the microprocessor.

Data Direction Registers (DDRA, DDRB)

The Data Direction Registers allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A

port and each bit in DDRB controls the corresponding line in the Peripheral B port. Placing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Peripheral Output Registers (ORA, ORB)

The Peripheral Output Registers store the output data which appears on the Peripheral I/O port. Writing a "0" into a bit in ORA causes the corresponding line on the Peripheral A port to go low ($< 0.4V$) if that line is programmed to act as an output. A "1" causes the corresponding output to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

Interrupt Status Control

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register, detects active transitions on the interrupt inputs and performs those operations necessary to assure proper operation of these four peripheral interface lines.

Peripheral Interface Buffers (A, B) and Data Bus Buffers (DBB)

These Buffers provide the necessary current and voltage drive on the peripheral I/O ports and data bus to assure proper system operation and to meet the device specifications.



FUNCTIONAL DESCRIPTION

Bit 2 (DDR) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1", a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0", a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1) selects the various internal registers as shown in Figure 5.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

Register Select Lines (RS0), (RS1)

These two register select lines are used to select the various registers inside the SY6520. These input lines are used in conjunction with internal control registers to select a particular register that is to be accessed by the microprocessor. These lines are normally connected to microprocessor address output lines. These lines operate in conjunction with the chip-select inputs to allow the microprocessor to address a single 8-bit register within the microprocessor address space. This register may be an internal register (CRA, ORA, etc.) or it may be a Peripheral I/O port.

The processor may write directly into the Control Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are discussed separately below.

Reading the Peripheral A I/O Port

The Peripheral A I/O port consists of 8 lines which can be programmed to act as inputs or outputs. When programmed to act as outputs, each line reflects the contents of the corresponding bit in the Peripheral Output Register. When programmed to act as inputs, these lines will go high or low depending on the input data. The Peripheral Output Register (ORA) has no effect on those lines programmed to act as inputs. The eight lines of the Peripheral A I/O port therefore contain either input or output data depending on whether the line is programmed to act as an input or an output.

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines into the processor (via the data bus). This will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read into the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

Reading the Peripheral B I/O Port

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for

Register Select Pin		Data Direction Register Access Control Bit		Register Selected
RS1	RS0	CRA-2	CRB-2	
0	0	1	—	Peripheral Interface A
0	0	0	—	Data Direction Register A
0	1	—	—	Control Register A
1	0	—	1	Peripheral Interface B
1	0	—	0	Data Direction Register B
1	1	—	—	Control Register B

Figure 5. Register Addressing

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those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back into the processor on a Read operation.

Interrupt Request Lines (\overline{IRQA} , \overline{IRQB})

The active low Interrupt Request lines (\overline{IRQA} and \overline{IRQB}) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are "open drain" and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a "wired-OR" configuration. The "A" and "B" in the titles of these lines correspond to the "A" peripheral port and the "B" peripheral port. Hence each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers. These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2).

The four interrupt flags are set by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

Control of \overline{IRQA}

Control Register A bit 7 is always set by an active transition of the CA1 interrupt input signal. Interrupting from this flag can be disabled by setting bit 0 in the Control Register A (CRA) to a logic 0. Likewise, Control Register A bit 6 can be set by an active transition of the CA2 interrupt input signal. Interrupting from this flag can be disabled by setting bit 3 in the Control Register to a logic 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the proper chip-select and register-select signals are provided to allow the processor to read the Peripheral A I/O port.

Control of \overline{IRQB}

Control of \overline{IRQB} is performed in exactly the same manner as that described above for \overline{IRQA} . Bit 7 in CRB is set by an active transition on CB1; interrupting from this flag is controlled by CRB bit 0. Likewise, bit 6 in CRB is set by an active transition on CB2; interrupting from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 are reset by a "Read Peripheral B Output Register" operation.

SUMMARY:

\overline{IRQA} goes low when CRA-7 = 1 and CRA-0 = 1 or
when CRA-6 = 1 and CRA-3 = 1

\overline{IRQB} goes low when CRB-7 = 1 and CRB-0 = 1 or
when CRB-6 = 1 and CRB-3 = 1

It should be stressed at this point that the flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

Interface Between SY6520 and Peripheral Devices

The SY6520 provides two 8-bit bi-directional ports and 4 interrupt/control lines for interfacing to peripheral devices. These ports and the associated interrupt/control lines are referred to as the "A" side and the "B" side. Each side has its own unique characteristics and will therefore be discussed separately below.

Peripheral I/O Ports

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by loading data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Peripheral A I/O Port (PA0-PA7)

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a "1" in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A "0" in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-ups as shown in Figure 6. These pull-up devices are resistive in nature and therefore allow the output voltage to go to V_{CC} for a logic 1. The switches can sink a full 1.6mA, making these buffers capable of driving one standard TTL load.

In the input mode, the pull-up devices shown in Figure 6 are still connected to the I/O pin and still supply current to this pin. For this reason, these lines represent one standard TTL load in the input mode.

Peripheral B I/O Port (PB0-PB7)

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an out-



put has been discussed previously. Likewise, the effect of reading or writing this port has been discussed. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

The Peripheral B I/O port buffers are push-pull devices as shown in Figure 7. The pull-up devices are switched "OFF" in the "0" state and "ON" for a logic 1. Since these pull-ups are active devices, the logic "1" voltage is not guaranteed to go higher than +2.4V. They are TTL compatible but are not CMOS compatible.

However, the active pull-up devices can source up to

1mA at 1.5V. This current drive capability is provided to allow direct connection to Darlington transistor switches. This allows very simple control of relays, lamps, etc.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic which is a function of the Peripheral B push-pull buffers is the high-impedance input state. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

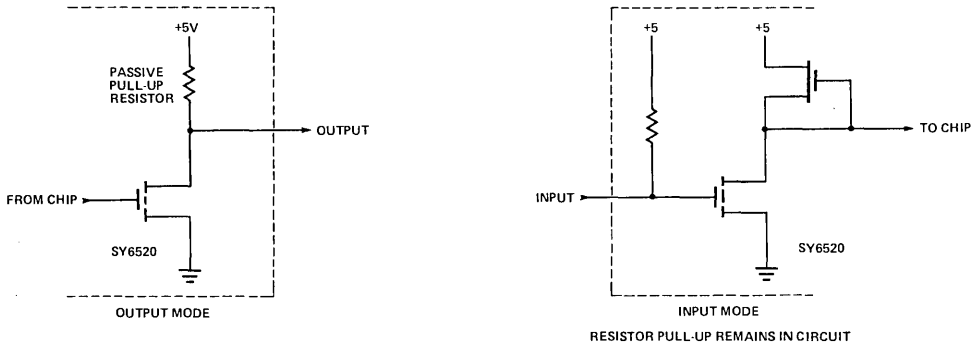


Figure 6. Port A Buffer Circuit (PA₀-PA₇)

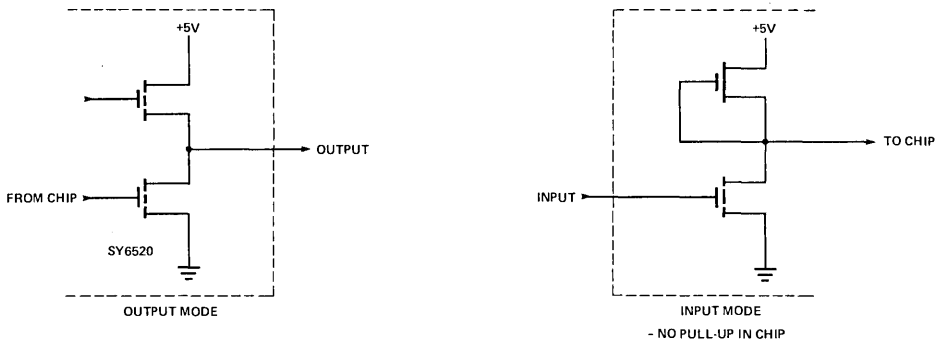


Figure 7. Port B Buffer Circuit (PB₀-PB₇)

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Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 8 summarizes the operation of these control lines.

Peripheral A Interrupt Input/Peripheral Control Lines (CA1, CA2)

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

NOTE: A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

Setting the interrupt flag will interrupt the processor through \overline{IRQA} if bit 0 of CRA is a 1 as described previously.

CA2 can act as a totally independent interrupt input or as a peripheral control output. As an input (CRA, bit 5=0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupts.

In the Output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a "0" and CRA, bit 3 to a "1". This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

Peripheral B Interrupt Input/Peripheral Control Lines (CB1, CB2)

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

CA1/CB1 CONTROL

CRA (CRB)		Active Transition of Input Signal*	IRQA (IROB) Interrupt Outputs
Bit 1	Bit 0		
0	0	Negative	Disable – remain high
0	1	Negative	Enable – goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable – remain high
1	1	Positive	Enable – as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB)			Active Transition of Input Signal*	IRQA (IROB) Interrupt Outputs
Bit 5	Bit 4	Bit 3		
0	0	0	Negative	Disable – remains high
0	0	1	Negative	Enable – goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable – remains high
0	1	1	Positive	Enable – as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

CRA			Mode	Description
Bit 5	Bit 4	Bit 3		
1	0	0	“Handshake” on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor “Read A Data” operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a “Read A Data” operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

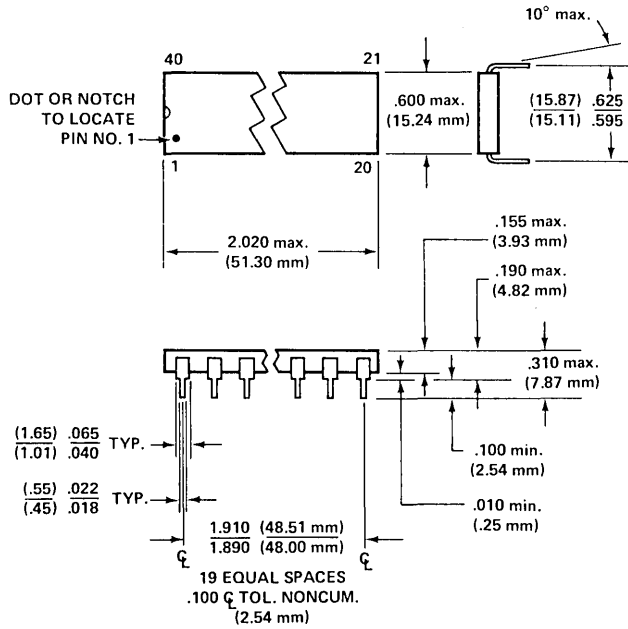
CB2 OUTPUT MODES

CRB			Mode	Description
Bit 5	Bit 4	Bit 3		
1	0	0	“Handshake” on Write	CB2 is set low on microprocessor “Write B Data” operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor “Write B Data” operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

Figure 8. Summary of Operation of Control Lines



PACKAGE OUTLINE



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

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- Two 8-Bit Bidirectional I/O Ports
- Two 16-Bit Programmable Timer/Counters
- Serial Data Port
- Single +5V Power Supply
- TTL Compatible
- CMOS Compatible Peripheral Control Lines
- Expanded "Handshake" Capability Allows Positive Control of Data Transfers Between Processor and Peripheral Devices
- Latched Output and Input Registers
- 1 MHz and 2 MHz Operation

The SY6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can

be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

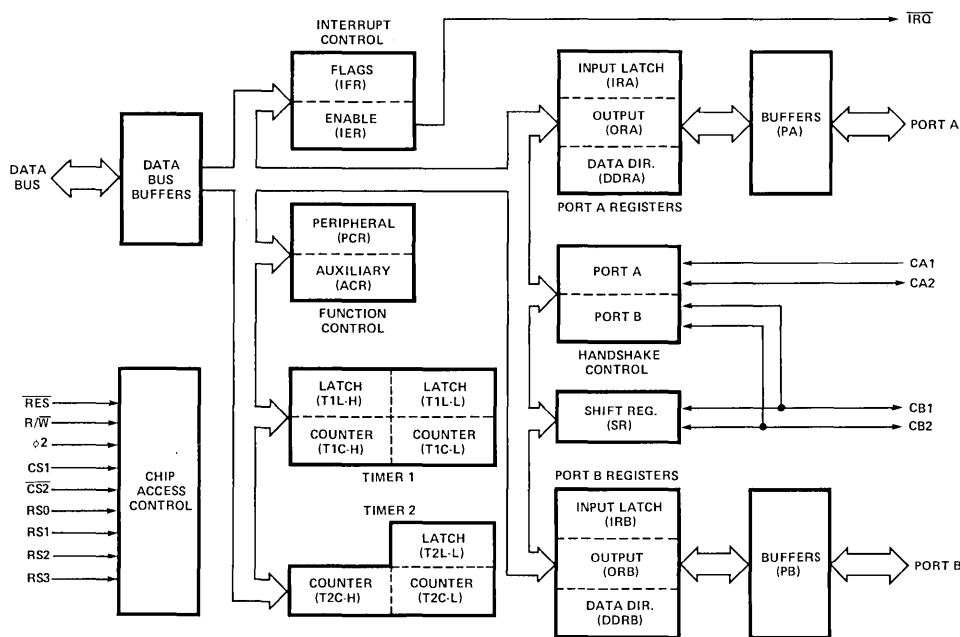


Figure 1. SY6522 Block Diagram





ABSOLUTE MAXIMUM RATINGS

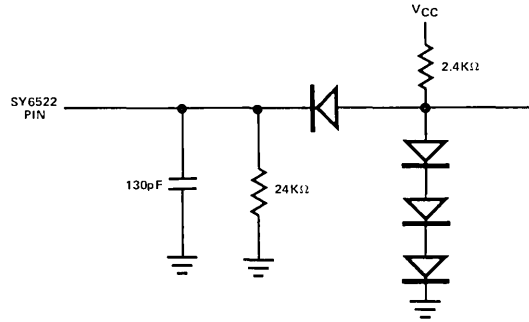
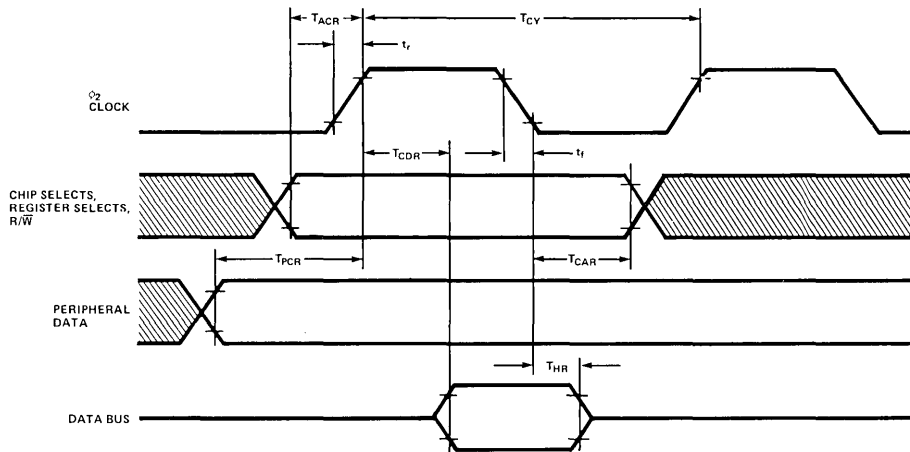
Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	V
Input Voltage	V _{IN}	-0.3 to +7.0	V
Operating Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0-70°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V _{IH}	Input High Voltage (all except $\phi 2$)	2.4	V _{CC}	V
V _{CH}	Clock High Voltage	2.4	V _{CC}	V
V _{IL}	Input Low Voltage	-0.3	0.4	V
I _{IN}	Input Leakage Current - V _{IN} = 0 to 5 Vdc R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2, CA1, $\phi 2$	-	±2.5	μA
I _{TSI}	Off-state Input Current - V _{IN} = .4 to 2.4V V _{CC} = Max, D0 to D7	-	±10	μA
I _{IH}	Input High Current - V _{IH} = 2.4V PA0-PA7, CA2, PB0-PB7, CB1, CB2	-100	-	μA
I _{IL}	Input Low Current - V _{IL} = 0.4 Vdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	-	-1.6	mA
V _{OH}	Output High Voltage V _{CC} = min, I _{load} = -100 μAdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	2.4	-	V
V _{OL}	Output Low Voltage V _{CC} = min, I _{load} = 1.6 mAdc	-	0.4	V
I _{OH}	Output High Current (Sourcing) V _{OH} = 2.4V V _{OH} = 1.5V (PB0-PB7)	-100 -1.0	-	μA mA
I _{OL}	Output Low Current (Sinking) V _{OL} = 0.4 Vdc	1.6	-	mA
I _{OFF}	Output Leakage Current (Off state) \overline{IRQ}	-	10	μA
C _{IN}	Input Capacitance - T _A = 25°C, f = 1 MHz (R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2, D0-D7, PA0-PA7, CA1, CA2, PB0-PB7) (CB1, CB2) ($\phi 2$ Input)	-	7.0 10 20	pF pF pF
C _{OUT}	Output Capacitance - T _A = 25°C, f = 1 MHz	-	10	pF
P _D	Power Dissipation	-	700	mW

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Figure 2. Test Load (for all Dynamic Parameters)

Figure 3. Read Timing Characteristics
READ TIMING CHARACTERISTICS (FIGURE 3)

Symbol	Parameter	SY6522		SY6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	—	90	—	ns
T_{CAR}	Address Hold Time	0	—	0	—	ns
T_{PCR}	Peripheral Data Set-Up Time	300	—	300	—	ns
T_{CDR}	Data Bus Delay Time	—	395	—	200	ns
T_{THR}	Data Bus Hold Time	10	—	10	—	ns

 NOTE: $t_r, t_f = 10$ to 30 ns.

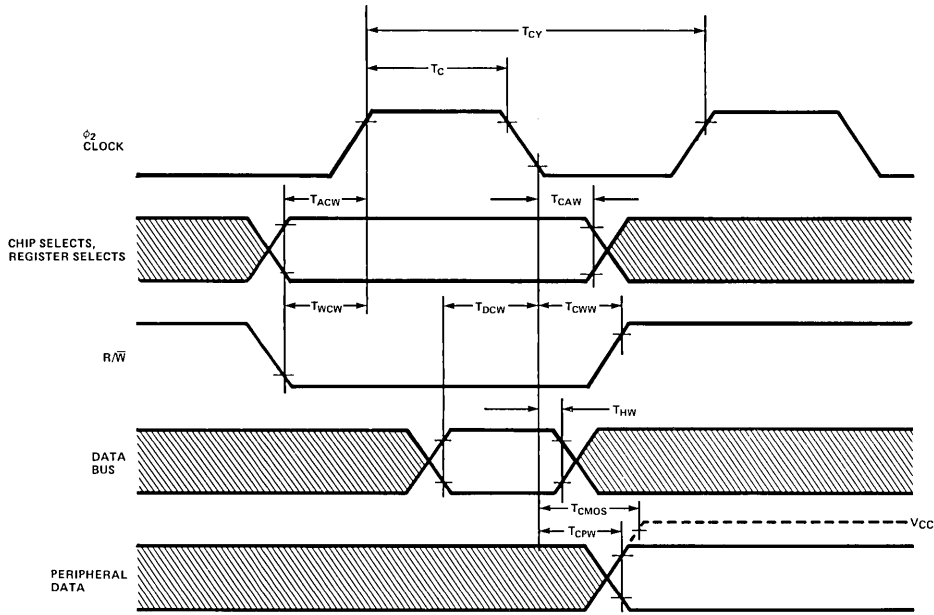


Figure 4. Write Timing Characteristics

WRITE TIMING CHARACTERISTICS (FIGURE 4)

Symbol	Parameter	SY6522		SY6522A		Unit
		Min.	Max.	Min.	Max.	
T _{CY}	Cycle Time	1	50	0.50	50	μs
T _C	φ2 Pulse Width	0.47	25	0.25	25	μs
T _{ACW}	Address Set-Up Time	180	—	90	—	ns
T _{CAW}	Address Hold Time	0	—	0	—	ns
T _{WCW}	R/ \bar{W} Set-Up Time	180	—	90	—	ns
T _{CWW}	R/ \bar{W} Hold Time	0	—	0	—	ns
T _{DCW}	Data Bus Set-Up Time	300	—	150	—	ns
T _{HW}	Data Bus Hold Time	10	—	10	—	ns
T _{CPW}	Peripheral Data Delay Time	—	1.0	—	1.0	μs
T _{CMOS}	Peripheral Data Delay Time to CMOS Levels	—	2.0	—	2.0	μs

NOTE: tr, tf = 10 to 30ns.

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PERIPHERAL INTERFACE CHARACTERISTICS

Symbol	Characteristic	Min.	Max.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2, and CB2 Input Signals	—	1.0	μs	—
T_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	—	1.0	μs	5a, 5b
T_{RS1}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	—	1.0	μs	5a
T_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	—	2.0	μs	5b
T_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	—	1.0	μs	5c, 5d
T_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0	1.5	μs	5c, 5d
T_{RS3}	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	—	1.0	μs	5c
T_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	—	2.0	μs	5d
T_{IL}	Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	—	ns	5e
T_{SR1}	Shift-Out Delay Time — Time from ϕ_2 Falling Edge to CB2 Data Out	—	300	ns	5f
T_{SR2}	Shift-In Setup Time — Time from CB2 Data In to ϕ_2 Rising Edge	300	—	ns	5g
T_{IPW}	Pulse Width — PB6 Input Pulse	2	—	μs	5i
T_{ICW}	Pulse Width — CB1 Input Clock	2	—	μs	5h
I_{IPS}	Pulse Spacing — PB6 Input Pulse	2	—	μs	5i
I_{ICS}	Pulse Spacing — CB1 Input Pulse	2	—	μs	5h

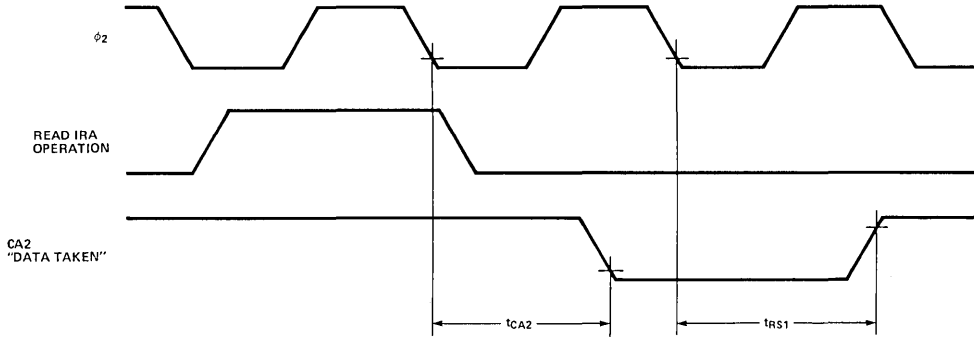


Figure 5a. CA2 Timing for Read Handshake, Pulse Mode

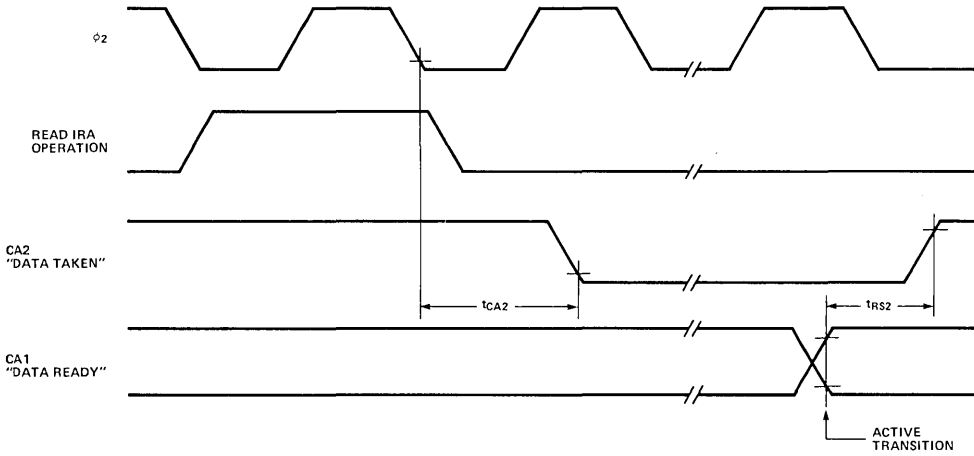


Figure 5b. CA2 Timing for Read Handshake, Handshake Mode

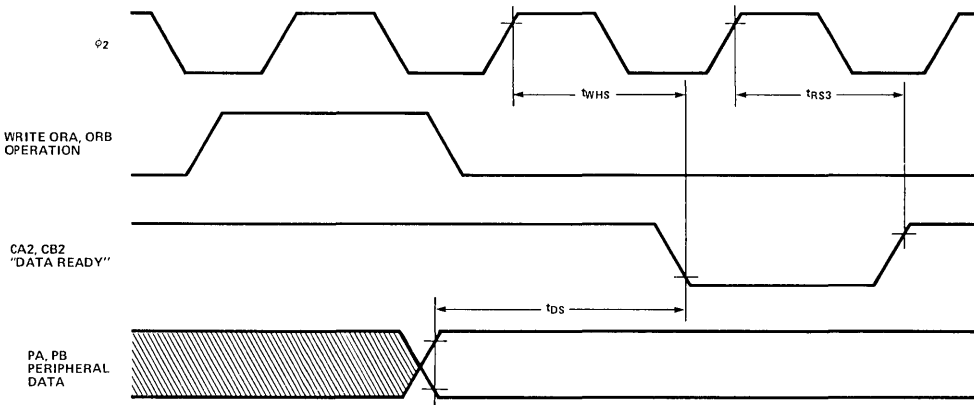


Figure 5c. CA2, CB2 Timing for Write Handshake, Pulse Mode

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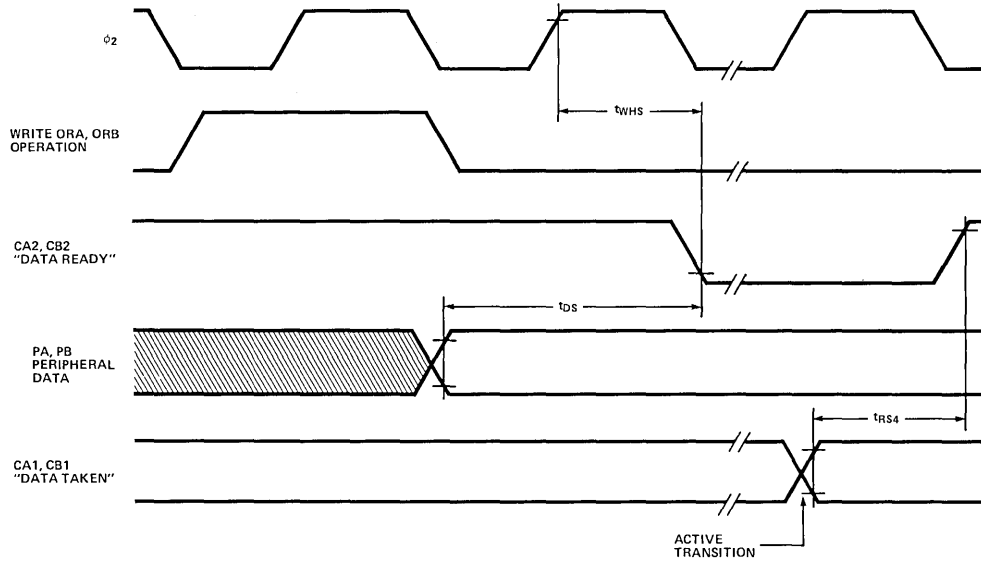


Figure 5d. CA2, CB2 Timing for Write Handshake, Handshake Mode

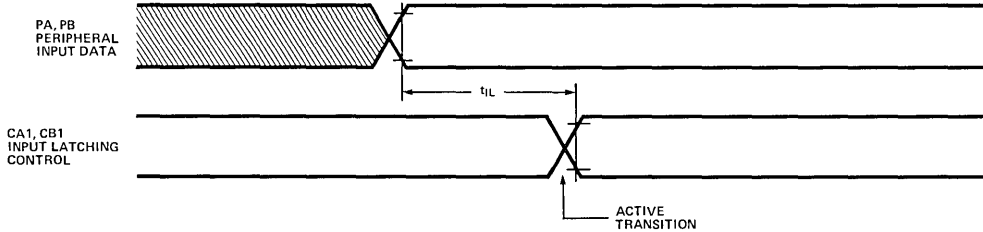


Figure 5e. Peripheral Data Input Latching Timing

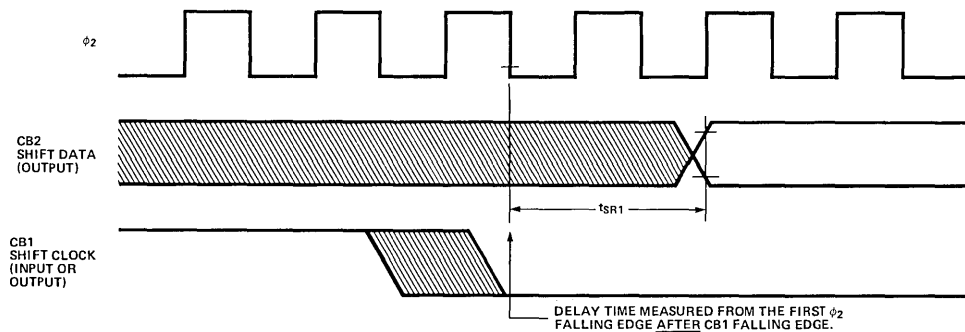


Figure 5f. Timing for Shift Out with Internal or External Shift Clocking

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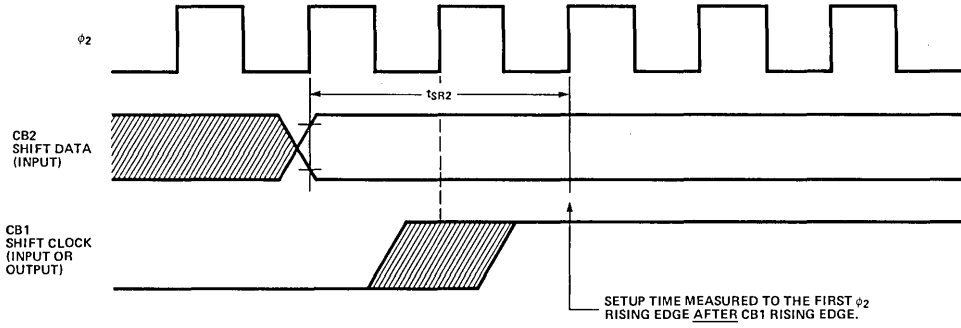


Figure 5g. Timing for Shift In with Internal or External Shift Clocking

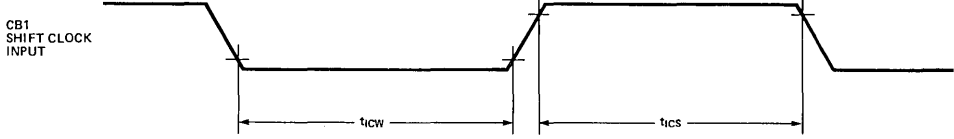


Figure 5h. External Shift Clock Timing

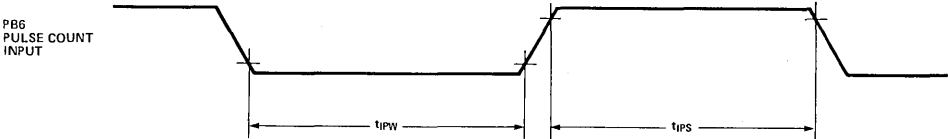


Figure 5i. Pulse Count Input Timing

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PIN DESCRIPTIONS
RES (Reset)

The reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

φ2 (Input Clock)

The input clock is the system φ2 clock and is used to trigger all data transfers between the system processor and the SY6522.

R/W (Read/Write)

The direction of the data transfers between the SY6522 and the system processor is controlled by the R/W line. If R/W is low, data will be transferred out of the processor into the selected SY6522 register (write operation). If R/W is high and the chip is selected, data will be transferred out of the SY6522 (read operation).

DB0-DB7 (Data Bus)

The eight bi-directional data bus lines are used to transfer data between the SY6522 and the system processor. During read cycles, the contents of the selected SY6522 register are placed on the data bus lines and transferred into the processor. During write cycles, these lines are high-impedance inputs and data is transferred from the processor into the selected register. When the SY6522 is unselected, the data bus lines are high-impedance.

CS1, CS2 (Chip Selects)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected SY6522 register will be accessed when CS1 is high and CS2 is low.

RS0-RS3 (Register Selects)

The four Register Select inputs permit the system processor to select one of the 16 internal registers of the SY6522, as shown in Figure 6.

Register Number	RS Coding				Register Desig.	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No "Handshake"	

Figure 6. SY6522 Internal Register Summary

IRQ (Interrupt Request)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is "open-drain" to allow the interrupt request signal to be "wire-or'ed" with other equivalent signals in the system.

PA0-PA7 (Peripheral A Port)

The Peripheral A port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 7 illustrates the output circuit.

CA1, CA2 (Peripheral A Control Lines)

The two Peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A port input lines. CA1 is a high-impedance input only while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

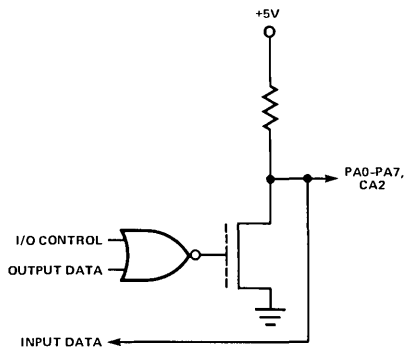


Figure 7. Peripheral A Port Output Circuit

PB0-PB7 (Peripheral B Port)

The Peripheral B port consists of eight bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the

PA port. In addition, the polarity of the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Peripheral B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0mA at 1.5VDC in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 8 is the circuit schematic.

CB1, CB2 (Peripheral B Control Lines)

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Unlike PB0-PB7, CB1 and CB2 cannot drive Darlington transistor circuits.

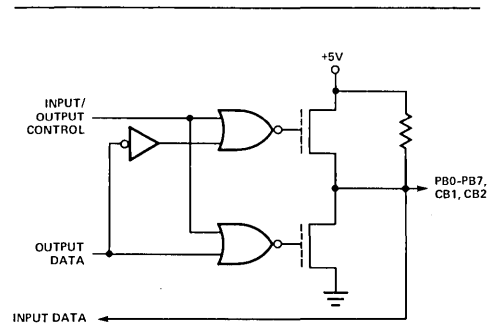


Figure 8. Peripheral B Port Output Circuit

FUNCTIONAL DESCRIPTION

Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and an Input Register (IRA, IRB). When the pin is programmed as an output, the voltage on the pin is controlled by the cor-

responding bit of the Output Register. A 1 in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled, IRA will reflect the levels on the PA pins at the time the latching occurred (via CA1).

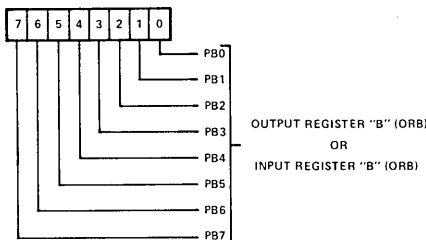
The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the level on the pin determines whether a 0 or a 1 is sensed. When reading IRB, however, the bit stored in the output register, ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 9, 10, and 11 illustrate the formats of the port registers. In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 16.)

Handshake Control of Data Transfers

The SY6522 allows positive control of data transfers between the system processor and peripheral devices

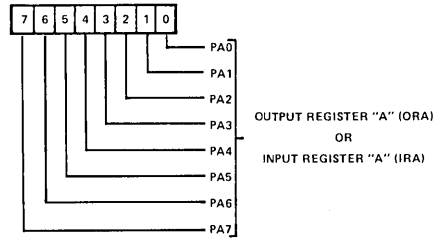
REG 0 – ORB/IRB



Pin Data Direction Selection	WRITE	READ
DDRB = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin level has no effect.
DDRB = "0" (INPUT) (Input latching disabled)	MPU writes into ORB, but no effect on pin level, until DDRB changed.	MPU reads input level on PB pin.
DDRB = "0" (INPUT) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 9. Output Register B (ORB), Input Register B (IRB)

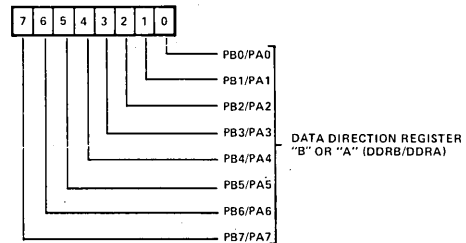
REG 1 – ORA/IRA



Pin Data Direction Selection	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin.
DDRA = "1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 10. Output Register A (ORA), Input Register A (IRA)

REG 2 (DDRB) AND REG 3 (DDRA)



- "0" ASSOCIATED PB/PA PIN IS AN INPUT (HIGH-IMPEDANCE)
- "1" ASSOCIATED PB/PA PIN IS AN OUTPUT, WHOSE LEVEL IS DETERMINED BY ORB/ORA REGISTER BIT.

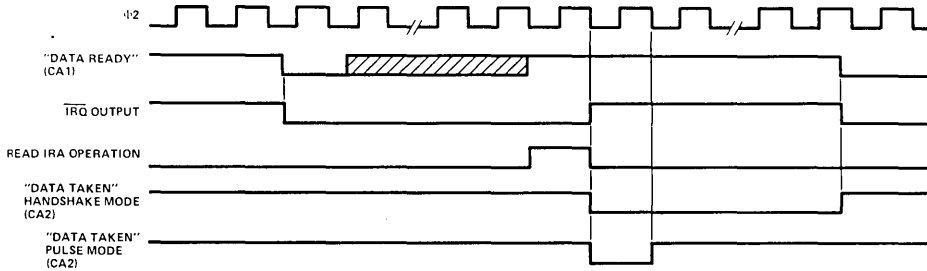
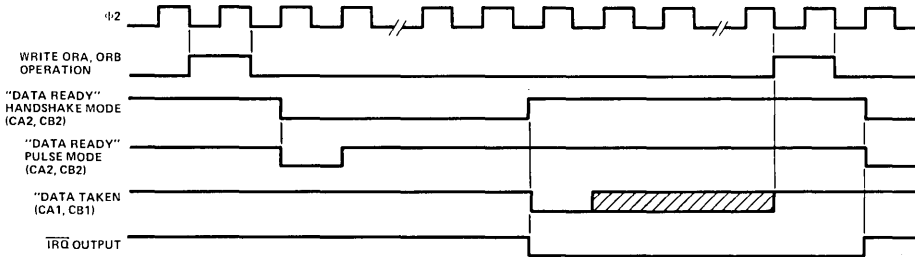
Figure 11. Data Direction Registers (DDRB, DDRA)

through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

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Figure 12. Read Handshake Timing (Port A, Only)

Figure 13. Write Handshake Timing

In the SY6522, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 12 which illustrates the normal Read Handshaking sequence.

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the SY6522 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the SY6522. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and cleaning the "Data Ready" output. This sequence is shown in Figure 13.

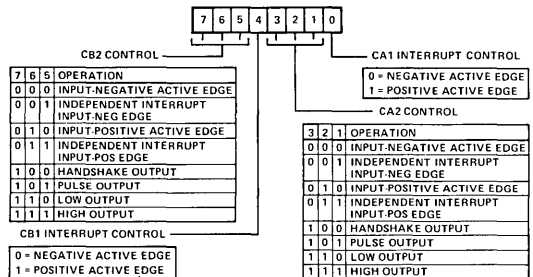
Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 14).

Timer Operation

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at $\phi 2$ clock rate. Upon reaching zero, an interrupt flag will be set, and \overline{TRQ} will go low if the interrupt is enabled. The timer will then disable any further interrupts, or will automatically transfer the contents of the latches into the counter and will continue to decrement. In addition, the timer may be programmed to invert the output signal on a peripheral pin each time it "times-out". Each of these modes is discussed separately below.

The T1 counter is depicted in Figure 15 and the latches in Figure 16.

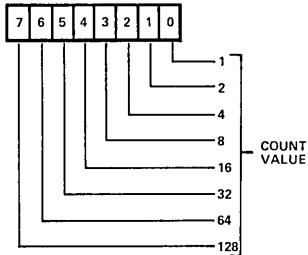
REG 12 - PERIPHERAL CONTROL REGISTER


Figure 14. CA1, CA2, CB1, CB2 Control

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 oper-

ating modes. The four possible modes are depicted in Figure 17.

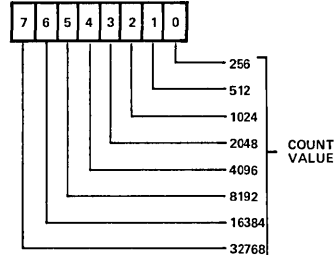
REG 4 – TIMER 1 LOW-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).

READ – 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

REG 5 – TIMER 1 HIGH-ORDER COUNTER

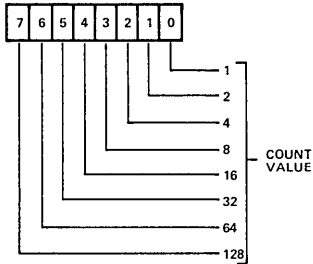


WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER. T1 INTERRUPT FLAG ALSO IS RESET.

READ – 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 15. T1 Counter Registers

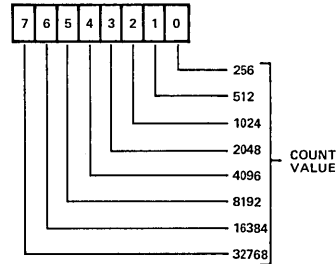
REG 6 – TIMER 1 LOW-ORDER LATCHES



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAT A WRITE INTO REG 4.

READ – 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG.

REG 7 – TIMER 1 HIGH-ORDER LATCHES



WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ – 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

Figure 16. T1 Latch Registers

REG 11 – AUXILIARY CONTROL REGISTER

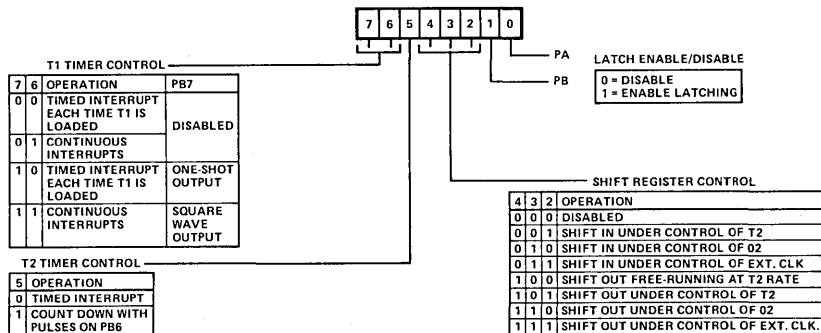


Figure 17. Auxiliary Control Register

Note: The processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

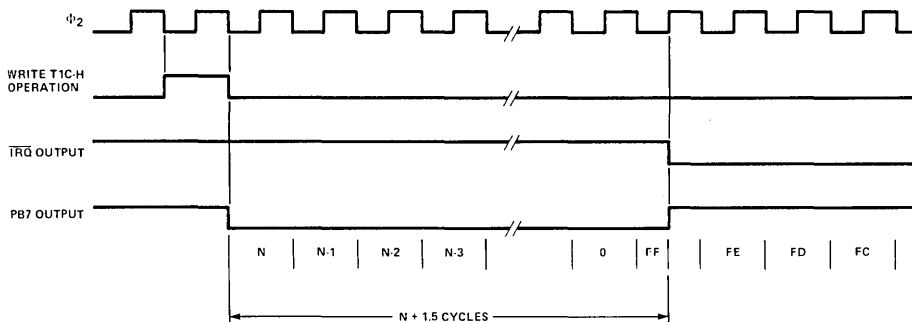


Figure 18. Timer 1 and Timer 2 One-Shot Mode Timing

Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7=1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

In the one-shot mode, writing into the high order latch has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter, the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the phase two following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{\text{TRQ}}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

Timing for the SY6522 interval timer one-shot modes is shown in Figure 18.

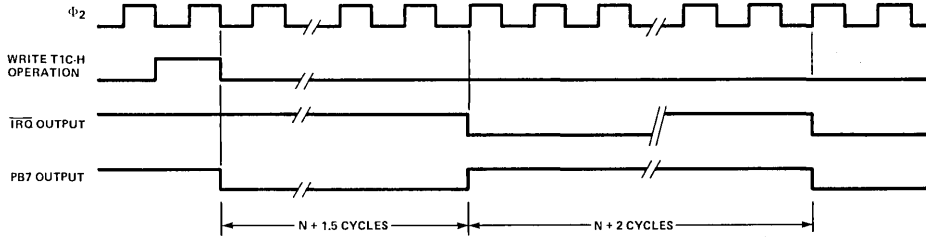
Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous

series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H, by reading T1C-L, or by writing directly into the flag as described later. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the SY6522 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated. Timing for the free-running mode is shown in Figure 19.



Note: A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If one is 1 and the other is 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

Figure 19. Timer 1 Free-Run Mode Timing

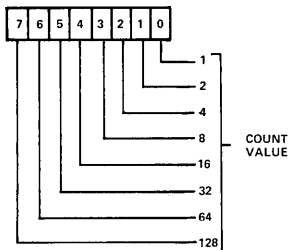
Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-slot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high order counter. The counter registers act as a 16-bit counter which decrements at $\Phi 2$ rate. Figure 20 illustrates the T2 Counter Registers.

Timer 2 One-Shot Mode

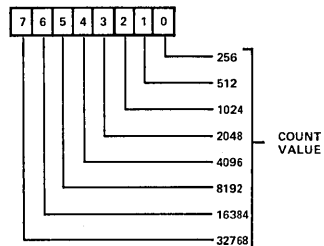
As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

REG 8 – TIMER 2 LOW-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T2 LOW-ORDER LATCHES.
 READ – 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

REG 9 – TIMER 2 HIGH-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T2 HIGH-ORDER COUNTER. ALSO, LOW-ORDER LATCHES TRANSFERRED TO LOW-ORDER COUNTER. IN ADDITION, T2 INTERRUPT FLAG IS RESET.
 READ – 8 BITS FROM T2 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 20. T2 Counter Registers

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on subsequent down-counting operations. Timing for this mode is shown in Figure 21. The pulse must be low on the leading edge of Φ_2 .

Shift Register Operation

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 22 illustrates the configuration of the SR data bits and the SR control bits of the ACR.

Figures 23 and 24 illustrate the operation of the various shift register modes.

Interrupt Operation

Controlling interrupts within the SY6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output (\overline{IRQ}) will go low. \overline{IRQ} is an "open-collector" output which can be "wire-or'ed" with other devices in the system to interrupt the processor.

In the SY6522, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

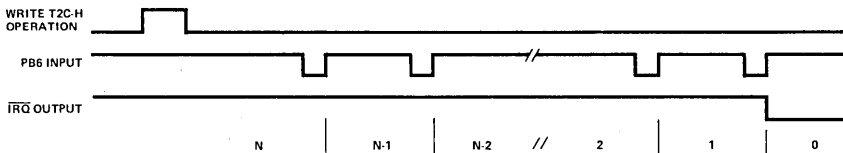
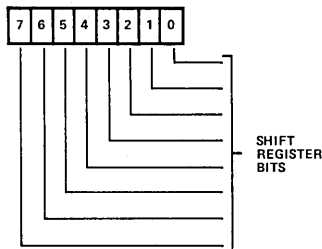


Figure 21. Timer 2 Pulse Counting Mode

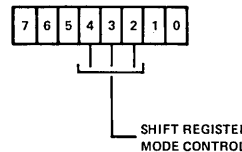
REG 10 — SHIFT REGISTER



NOTES:

1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

REG 11 — AUXILIARY CONTROL REGISTER



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF Φ_2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF Φ_2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 22. SR and ACR Control Bits

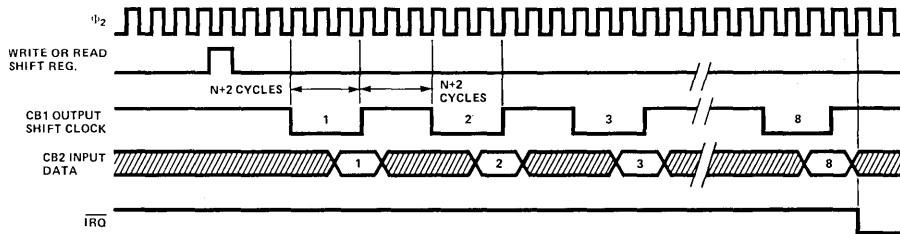
SR Disabled (000)

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operation is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic 0).

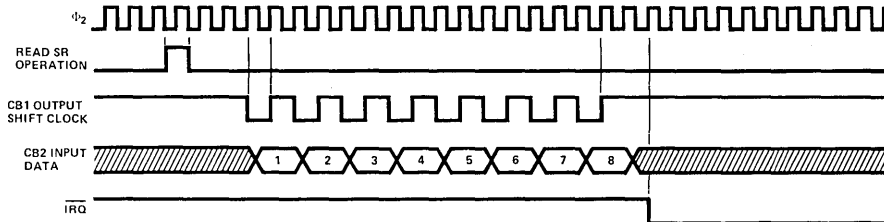
Shift in Under Control of T2 (001)

In the 001 mode the shifting rate is controlled by the low order 8 bits of T2. Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the ϕ_2 clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will be set and \overline{IRQ} will go low.


Shift in Under Control of ϕ_2 (010)

In mode 010 the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each ϕ_2 clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.


Shift in Under Control of External CB1 Clock (011)

In mode 011 CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

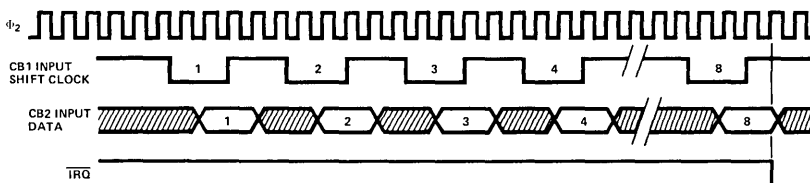
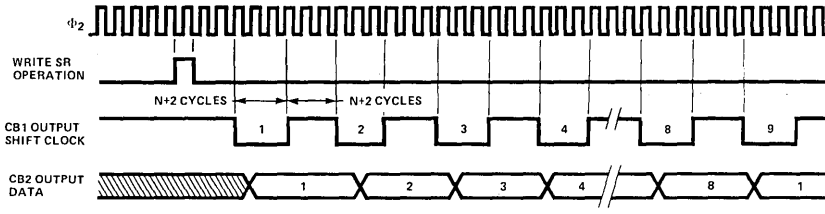


Figure 23. Shift Register Input Modes



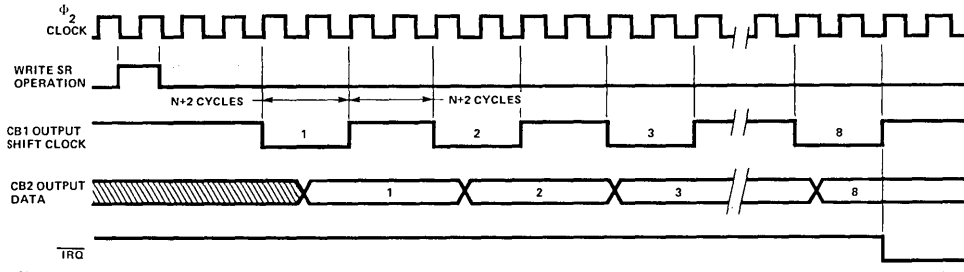
Shift Out Free-Running at T2 Rate (100)

Mode 100 is very similar to mode 101 in which the shifting rate is set by T2. However, in mode 100 the SR Counter does not stop the shifting operation. Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.



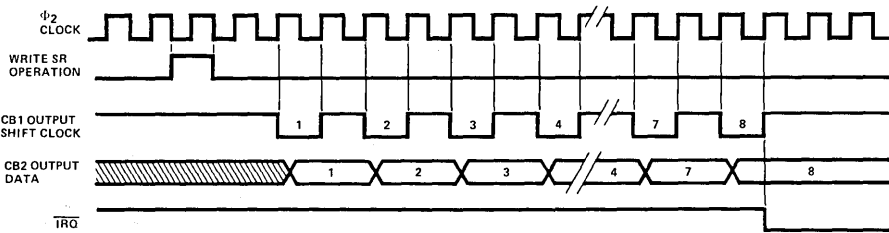
Shift Out Under Control of T2 (101)

In mode 101 the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.



Shift Out Under Control of ϕ_2 (110)

In mode 110, the shift rate is controlled by the ϕ_2 system clock.



Shift Out Under Control of External CB1 Clock (111)

In mode 111 shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

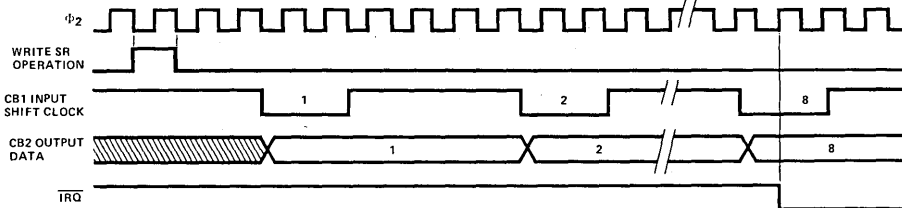


Figure 24. Shift Register Output Modes

MICRO-PROCESSORS

The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) are depicted in Figures 25 and 26, respectively.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the IRQ output. This bit corresponds to the logic function: $IRQ = IFR6 \times IER6 + IFR5 \times IER5 + IFR4 \times IER4 + IFR3 \times IER3 + IFR2 \times IER2 + IFR1 \times IER1 + IFR0 \times IER0$. Note: X = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

REG 13 – INTERRUPT FLAG REGISTER

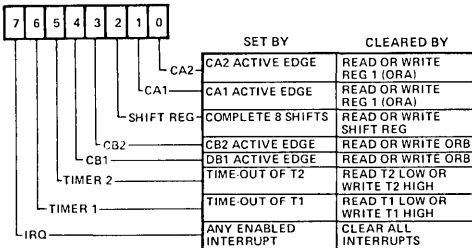


Figure 25. Interrupt Flag Register (IFR)

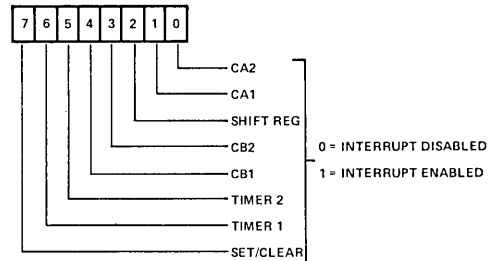
For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register. The system processor can set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to

address 1110 (IER address). If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/W line high. Bit 7 will be read as a logic 0.

REG 14 – INTERRUPT ENABLE REGISTER

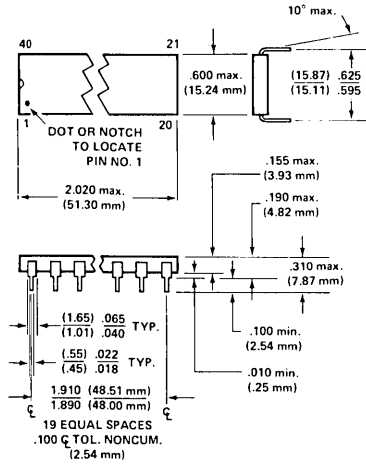


- NOTES:
- IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT.
 - IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT.
 - IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "0" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

Figure 26. Interrupt Enable Register (IER)

MICRO-PROCESSORS

PACKAGE OUTLINE

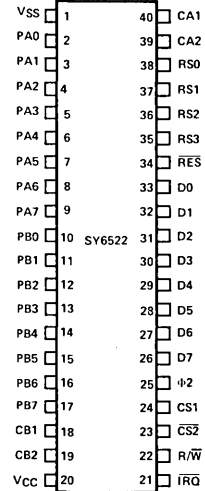


NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

ORDERING INFORMATION

Order Number	Package Type	Frequency Option
SYP 6522	Plastic	1 MHz
SYP 6522A	Plastic	2 MHz
SYC 6522	Ceramic	1 MHz
SYC 6522A	Ceramic	2 MHz

PIN CONFIGURATION





Memory, I/O, Timer Array

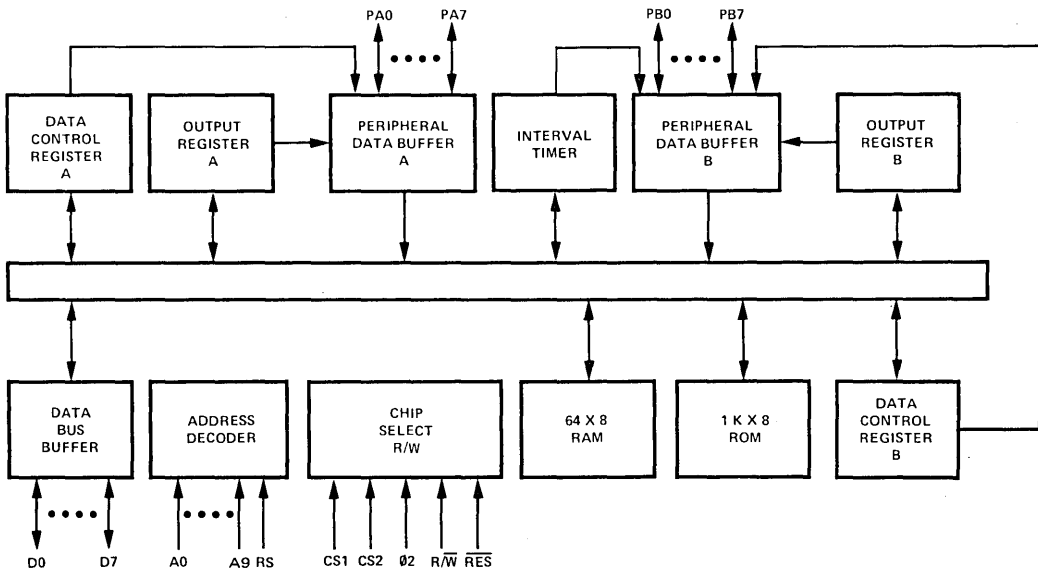
SY6530

MICROPROCESSOR
PRODUCTS

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- 1024 x 8 ROM
- 64 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins
- Allows up to 7K contiguous bytes of ROM with no external decoding

The SY6530 is designed to operate in conjunction with the SY6500 microprocessor Family. It is comprised of a mask programmable 1024 x 8 ROM, a 64 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods.

FIGURE 1. SY6530 BLOCK DIAGRAM



MICRO-PROCESSORS

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (V_{CC}) -3 to +7.0V
 Input/Output Voltage (V_{IN}) -3 to +7.0V
 Operating Temperature (T_{OP}) 0 to 70°C
 Storage Temperature Range (T_{STG}) -55 to +150°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$)

	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.4		V_{CC}	V
Input Low Voltage	V_{IL}	-0.3		0.4	V
Input Leakage Current; $V_{IN} = V_{SS} + 5V$ A0-A9, RS, R/W, RES, 02, PB6*, PB5*	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); $V_{IN} = .4V$ to 2.4V; D0-D7	I_{TSI}		± 1.0	± 10.0	μA
Input High Current; $V_{IN} = 2.4V$ PA0-PA7, PB0-PB7	I_{IH}	-100.	-300.		μA
Low Input Current; $V_{IN} = .4V$ PA0-PA7, PB0-PB7	I_{IL}		-1.0	-1.6	mA
Output High Voltage $V_{CC} = MIN$, $I_{LOAD} \leq -100\mu A$ (PA0-PA7, PB0-PB7, D0-D7) $I_{LOAD} \leq -3mA$ (PA0, PB0)	V_{OH}	2.4 1.5			V
Output Low Voltage $V_{CC} = MIN$, $I_{LOAD} \leq 1.6mA$	V_{OL}			0.4	V
Output High Current (Sourcing); $V_{OH} \geq 2.4V$ (PA0-PA7, PB0-PB7, D0-D7) $\geq 1.5V$ Available for other than TTL (Darlington) (PA0, PB0)	I_{OH}	-100 -3.0	-1000 -5.0		μA mA
Output Low Current (Sinking); $V_{OL} \leq .4V$	I_{OL}	1.6			mA
Clock Input Capacitance	C_{CLK}			30	pF
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF
Power Dissipation	P_D		500	700	mW

*When Programmed as address pins All values are D.C. readings

WRITE TIMING CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Period	T_{CYC}	1		10	μs
Rise & Fall Times	T_R, T_F			25	ns
Clock Pulse Width	T_C	470			ns
R/W valid before positive transition of clock	T_{WCW}	180			ns
Address valid before positive transition of clock	T_{ACW}	180			ns
Data bus valid before negative transition of clock	T_{DCW}	300			ns
Data Bus Hold Time	T_{HW}	10			ns
Peripheral data valid after negative transition of clock	T_{CPW}			1	μs
Peripheral data valid after negative transition of clock driving CMOS (Level = $V_{CC} - 30\%$)	T_{CMOS}			2	μs
R/W hold time after negative clock transition	T_{CWW}	0			ns
Address hold time	T_{CAH}	0			ns



READ TIMING CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
R/ \bar{W} valid before positive transition of clock	T _{WCR}	180			ns
Address valid before positive transition of clock	T _{ACR}	180			ns
Peripheral data valid before positive transition of clock	T _{PCR}	300			ns
Data bus valid after positive transition of clock	T _{CDR}			395	ns
Data Bus Hold Time	T _{HR}	10			ns
$\bar{I}RQ$ (Interval Timer Interrupt) valid before positive transition of clock	T _{IC}	200			ns
R/ \bar{W} hold time after negative clock transition	T _{CWR}	0			ns
Address hold time	T _{CAH}	0			ns

Loading = 30 pF + 1 TTL load for PA0-PA7, PB0-PB7
 = 130 pF + 1 TTL load for D0-D7

INTERFACE SIGNAL DESCRIPTION

Reset (\bar{RES})

During system initialization a low ($\leq 0.4V$) on the \bar{RES} input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during reset. Interrupt capability is disabled with the \bar{RES} signal. The \bar{RES} signal must be held low for at least one clock period when reset is required.

Input Clock (ϕ_2)

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4, V_{IH} > 2.4$ or high level clock $V_{IL} < 0.2, V_{IH} = V_{CC}^{+3}_{-2}$).

Read/Write (R/\bar{W})

The R/\bar{W} is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the SY6530. A high on the R/\bar{W} pin allows the processor to read (with proper addressing) the data supplied by the SY6530. A low on the R/\bar{W} pin allows a write (with proper addressing) to the SY6530.

Interrupt Request ($\bar{I}RQ$)

The $\bar{I}RQ$ pin is an interrupt pin from the interval timer. This same pin, if not used as an interrupt, can be used as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the data direction register. The pin will be normally high with a low indicating an interrupt from the SY6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pullup may be omitted with a mask option.

Data Bus (D0-D7)

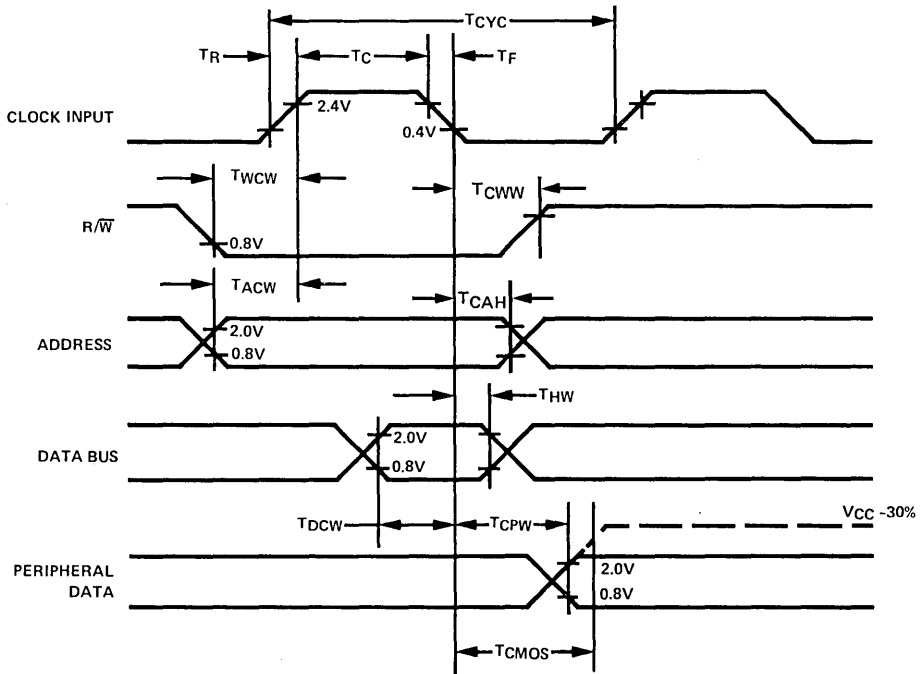
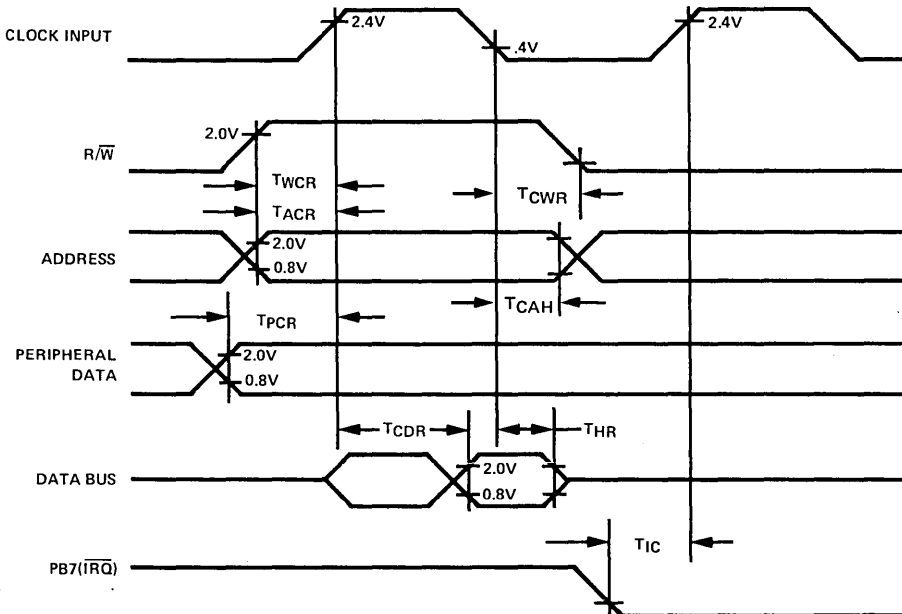
The SY6530 has eight bi-directional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports (PA0-PA7, PB0-PB7)

The SY6530 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into 2 8-bit ports, PA0-PA7 and PB0-PB7. PB5, PB6 and PB7 also have other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the SY6530 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volts for a "0" as the peripheral pins are all TTL compatible. Pins PA0 and PB0 are also capable of sourcing 3 ma at 1.5V, thus making them capable of direct transistor drive.

Address Lines (A0-A9)

There are 10 address pins. In addition to these 10, there is the ROM SELECT (RS) pin. The above pins, A0-A9 and ROM SELECT, are always used as addressing pins. There are 2 additional pins which are mask programmable and can be used either individually or together as CHIP SELECTS. They are pins PB5 and PB6. When used as peripheral data pins they cannot be used as chip selects.

FIGURE 2. WRITE TIMING CHARACTERISTICS

FIGURE 3. READ TIMING CHARACTERISTICS

MICRO-PROCESSORS

INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The SY6530 is divided into four basic sections, RAM, ROM, I/O and TIMER. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of 2 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O Register.

ROM 1 K Byte (8 K Bits)

The 8K ROM is in a 1024 x 8 configuration. Address lines A0-A9, as well as RS are needed to address the entire ROM. With the addition of CS1 and CS2, seven SY6530's may be addressed, giving 7168 x 8 bits of contiguous ROM.

RAM - 64 Bytes (512 Bits)

A 64 x 8 static RAM is contained on the SY6530. It is addressed by A0-A5 (Byte Select), RS, A6, A7, A8, A9, and, depending on the number of chips in the system, CS1 and CS2.

Internal Peripheral Registers

There are four internal registers, two data direction registers and two peripheral I/O data registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral buffer pin as an output. Therefore, anything then written into the I/O Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data to or from the I/O Register. For example, a "1" loaded into data direction A, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and remain in the high state. The two data I/O registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor array.

During a read operation the microprocessor is not reading the I/O Registers but in fact is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the I/O Register. The only way the I/O Register data can be changed is by a microprocessor Write operation. The I/O Register is not affected by a Read of the data on the peripheral pins.

Interval Timer

The Timer section of the SY6530 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 4.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written into the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A3 = 1 enables \overline{IRQ} on PB7, A3 = 0 disables \overline{IRQ} on PB7. When PB7 is used as an interrupt flag with the interval timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

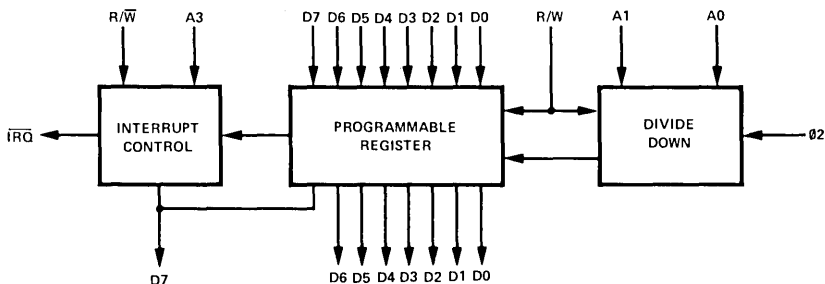
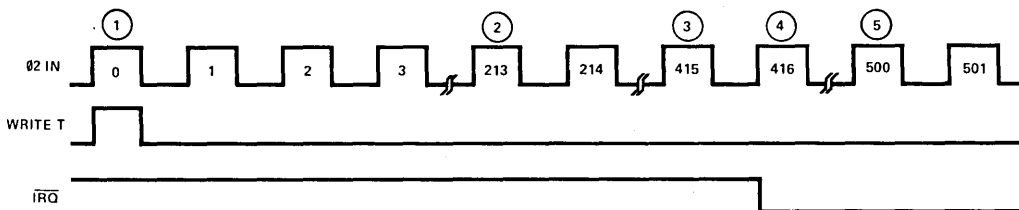
When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 1 1 is read, the time since interrupt is 28T. The value read is in two's complement.

```
Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
ADD 1      = 0 0 0 1 1 1 0 0 = 28.
```

Thus to arrive at the total elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 5 illustrates an example of interrupt.

FIGURE 4. BASIC ELEMENTS OF INTERVAL TIMER

FIGURE 5. TIMER INTERRUPT TIMING


1. Data written into Interval timer is $00110100 = 52_{10}$

2. Data in Interval timer is $00011001 = 25_{10}$

$$52 - \frac{213}{8} - 1 = 52 - 26 - 1 = 25$$

3. Data in Interval timer is $00000000 = 0_{10}$

$$52 - \frac{415}{8} - 1 = 52 - 51 - 1 = 0$$

4. Interrupt has occurred at ϕ_2 pulse #416

Data in Interval timer = 11111111

5. Data in Interval timer is 10101100

two's complement is $01010100 = 84_{10}$

$$84 + (52 \times 8) = 500_{10}$$

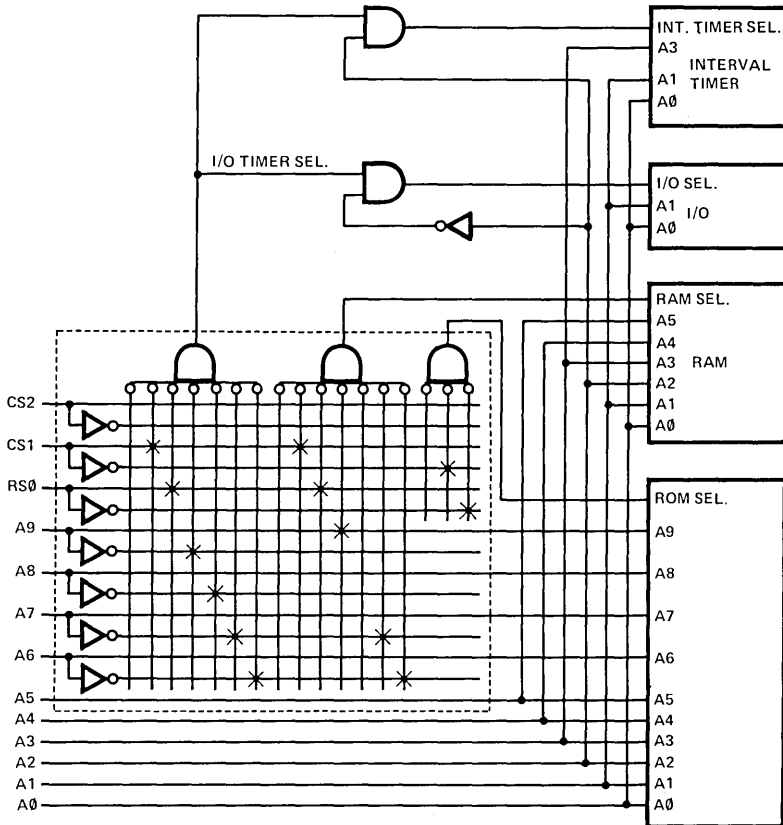
When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{\text{IRQ}}$ pin. This is done so as to avoid future interrupts until another Write timer operation.

ADDRESSING

Addressing of the SY6530 offers many variations to the user for greater flexibility. The system may be configured with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0-A9). In addition there is the possibility of 3 additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are CS1 and CS2. The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering the part. Both pins act independently of each other in that either or both pins may be designated as chip-select. The third additional address line is RS. In a 2-chip system, RS would be used to distinguish between ROM and non-ROM sections of the SY6530. With the addressing pins available, a total of 7K contiguous ROM may be addressed with no external decode. Below is an example of a 1-chip and a 7-chip SY6530 addressing scheme.

One-Chip Addressing

Figure 6 illustrates a 1-chip system for the SY6530.

FIGURE 6. SY6530 ONE CHIP ADDRESS ENCODING DIAGRAM


- A. X indicates mask programming
i.e. ROM select = $CS1 \cdot RSO$
RAM select = $CS1 \cdot RSO \cdot \overline{A9} \cdot A7 \cdot A6$
I/O TIMER SELECT = $CS1 \cdot RSO \cdot A9 \cdot A8 \cdot A7 \cdot A6$
- B. Notice that A8 is a don't care for RAM select
- C. The CS2/PB5 pin functions as PB5 in this example.

Seven-Chip Addressing

In the 7-chip system the objective would be to have 7K of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,535 and 1024. For this case, assume A13, A14, and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between addresses 65,535 and 58,367. The 2 pins designated as chip-select or I/O would be mask programmed as chip-select pins. Pin RS would be connected to address line A10. Pins CS1 and CS2 would be connected to address lines A11 and A12 respectively. See Figure 7.

The two examples shown would allow addressing of the ROM and RAM; however, once the I/O or timer has been addressed, further decoding is necessary to select which of the I/O registers is desired, as well as the coding of the interval timer.

I/O Register - Timer Addressing

Figure 8 illustrates the address decoding for the internal elements and timer programming. Address lines A2 distinguishes I/O registers from the timer. When A2 is high and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the divide by matrix. This decoding is defined in Figure 8. In addition, address A3 is used to enable the interrupt flag to PB7.



The addressing of the ROM select, RAM select and I/O timer select lines would be as follows:

FIGURE 7. SY6530 SEVEN CHIP ADDRESSING SCHEME

		CS2	CS1	RS0	A9	A8	A7	A6
		A12	A11	A10				
SY6530 #1,	ROM SELECT	0	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	0
	I/O TIMER	0	0	0	1	0	0	0
SY6530 #2,	ROM SELECT	0	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	1
	I/O TIMER	0	0	0	1	0	0	1
SY6530 #3,	ROM SELECT	0	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	0
	I/O TIMER	0	0	0	1	0	1	0
SY6530 #4,	ROM SELECT	1	0	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	1
	I/O TIMER	0	0	0	1	0	1	1
SY6530 #5,	ROM SELECT	1	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	0
	I/O TIMER	0	0	0	1	1	0	0
SY6530 #6,	ROM SELECT	1	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	1
	I/O TIMER	0	0	0	1	1	0	1
SY6530 #7,	ROM SELECT	1	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	1	0
	I/O TIMER	0	0	0	1	1	1	0

* RAM select for SY6530 #5 would read = $\overline{A12} \cdot \overline{A11} \cdot \overline{A10} \cdot \overline{A9} \cdot A8 \cdot \overline{A7} \cdot \overline{A6}$

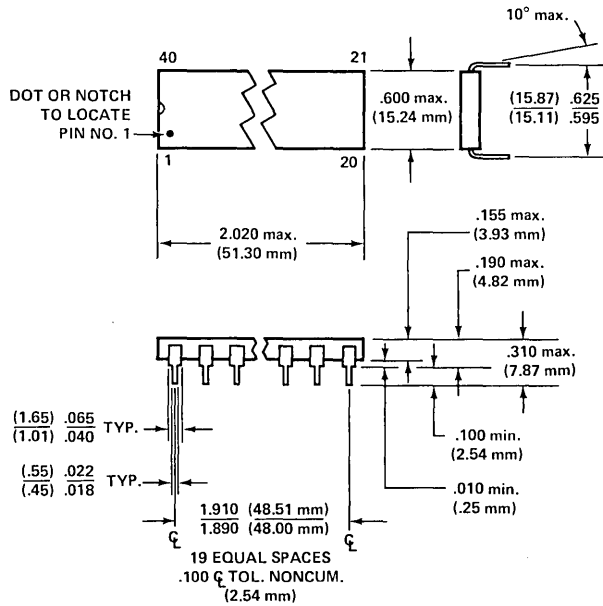
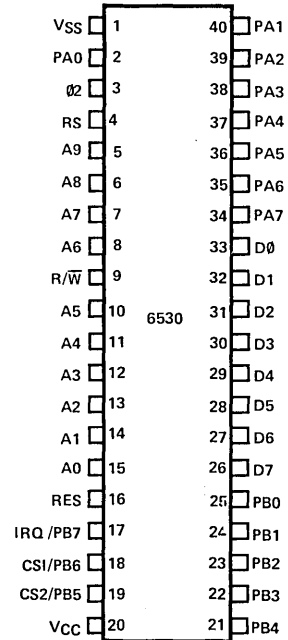
FIGURE 8. ADDRESSING DECODE FOR I/O REGISTER AND TIMER
ADDRESSING DECODE

	ROM SELECT	RAM SELECT	I/O TIMER SELECT	R/W	A3	A2	A1	A0
READ ROM	1	0	0	1	-	-	-	-
WRITE RAM	0	1	0	0	-	-	-	-
READ RAM	0	1	0	1	-	-	-	-
WRITE DDRA	0	0	1	0	-	0	0	1
READ DDRA	0	0	1	1	-	0	0	1
WRITE DDRB	0	0	1	0	-	0	1	1
READ DDRB	0	0	1	1	-	0	1	1
WRITE PER. REG. A	0	0	1	0	-	0	0	0
READ PER. REG. A	0	0	1	1	-	0	0	0
WRITE PER. REG. B	0	0	1	0	-	0	1	0
READ PER. REG. B	0	0	1	1	-	0	1	0
WRITE TIMER								
÷ 1T	0	0	1	0	X	1	0	0
÷ 8T	0	0	1	0	X	1	0	1
÷ 64T	0	0	1	0	X	1	1	0
÷ 1024T	0	0	1	0	X	1	1	1
READ TIMER	0	0	1	1	X	1	-	0
READ INTERRUPT FLAG	0	0	1	1	-	1	-	1

- = Don't care condition

X A3 = 1 Enables IRQ to PB7

A3 = 0 Disables IRQ to PB7


PACKAGE OUTLINE

PIN DESIGNATION

PROGRAMMING INSTRUCTIONS

The SY6530 utilizes computer aided techniques to manufacture and test custom ROM patterns. The pattern and address coding is supplied to Synertek in any of several formats.

- 1) 2708-type EPROMs.
- 2) Synertek data card formats.
- 3) Other input formats, providing they can be translated into one of the above.

Synertek Data Card Format

A. The format for the first and all succeeding records, except for the last record, in a file is as follows:

;N₁N₀ A₃A₂A₁A₀ (D₁D₀)₁ (D₁D₀)₂ X₃X₂X₁X₀

where:

1. All characters (N,A,D,X) are the ASCII characters 0 through F, each representing a hexadecimal digit.
2. ; is a record mark indicating the start of a record.
3. N₁N₀ = the number of bytes of data in this record (in hexadecimal). Each pair of hexadecimal characters (D₁D₀) represents a single byte in the record.
4. A₃A₂A₁A₀ = the hexadecimal starting address for the record. A₃ represents address bits 15 through 12, etc. The 8-bit byte represented by (D₁D₀)₁ is stored in address A₃A₂A₁A₀; (D₁D₀)₂ is stored in (A₃A₂A₁A₀) + 1, etc.
5. (D₁D₀) = two hexadecimal digits representing an 8-bit byte of data. (D₁ = high order 4 binary bits and D₀ = low-order 4 bits). A maximum of 18 (Hex) or 24 (decimal) bytes of data per record is permitted.
6. X₃X₂X₁X₀ = record check sum. This is the hexadecimal sum of all characters in the record, including N₁N₀ and A₃A₂A₁A₀ but excluding the record mark and the check sum characters. To generate the check sum, each byte of data (represented by two ASCII characters), is treated as 8 binary bits. The binary sum of these 8-bit bytes is truncated to 16 binary bits (4 hexadecimal digits) and is then represented in the record as four ASCII characters (X₃X₂X₁X₀).



B. The format for the last record in a file is as follows:

; 00 C3C2C1C0 X3X2X1X0

1. 00 = zero bytes of data in this record. This identifies this as the final record in a file.
2. C3C2C1C0 = the total number of records (in hexadecimal) in this file, including the last record.
3. X3X2X1X0 = check sum for this record.

C. Example

The following example illustrates the exact format of the hex interface file in both listing and punched paper tape form.

```

;18F000CA86004C00F0FDF9212D21FF292DBF2161F5F7FF657D677D0D40
;18F018E564672DFD7575E5000CF4112F800925198D200539192F20C98
;18F03008DB02880810DE12D894189AC2830E9800FBB6232F087F650AA5
;18F048036E20EF2FA58D4465E8FDF93DE775EF257FB520ED64657C0DEB
;18F0607F11D05A1EDF0250B0DAFE009252909912DB108A0298DE080C0D
;18F078D95058DF82D2D79A00ED65E68724EE05212764A5F5BDA9050E2C
;18F090EC20FF652525246933213F20FF31293B7E18D65042DE40500A92
;18F0A81E5E5B02534A53DE4A9B189259969F589E5E92DF52DE9E9A0CA2
;18F0C000B3268D2400EF6765E7A0B5606725217D20AF35EDF5202F0C08
;18F0D8692525342B35256CDF12F2785FFF547FD2E2D6525BDF5A720D26
;10F0F012DB020F1A1ABF86D2DA9ADAC8DECA1B0A12
;00000B000B

```

ADDITIONAL PATTERN INFORMATION

In addition to the ROM data patterns, it is necessary to provide the information outlined below.

- CUSTOMER NAME
- CUSTOMER PART NO.
- CUSTOMER CONTACT (NAME)
- CUSTOMER TELEPHONE NO.
- CS1/PB6 (ENTER "CS1" OR "PB6")
- CS2/PB5 (ENTER "CS2" OR "PB5")
- PULL-UP RESISTOR ON PB7 ("YES" OR "NO")
- LOGIC FORMAT ("POS" OR "NEG")

DEVICE ADDRESSING (Enter "H" for High, "L" for Low, or "N" for don't care)

	RS	CS1	CS2	A9	A8	A7	A6
ROM SELECT							
RAM SELECT							
I/O TIMER SELECT							

Send Information To:

Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

MICRO-PROCESSORS

SY6530 CUSTOMER SPECIFICATION FORM

1. Date.
2. Customer name.
3. Customer part no.
(maximum 10 digits)
4. Synertek "C" number.
5. Customer Contact.
6. Customer phone number
7. Chip Select Code
(Check one square in each block)

CS1	
PB6	

CS2	
PB5	

PULL UP	YES	
ON PB7	NO	

8. ROM/RAM/I-O SELECTS (Specify H or L or N (don't care) in each box.)

	RS	CS1	CS2	A9	A8	A7	A6
ROM SELECT				N	N	N	N
RAM SELECT							
I/O SELECT							

9. Customer's Input

- Punched Cards
- Punched Tape

10. Data Format

- MOS Technology
- Intel Hex
- Intel BPNF
- Binary

11. Logic Format

- Positive
- Negative

12. Verification Status

- Hold
- Not Required

MICRO-PROCESSORS



RAM, I/O, Timer Array

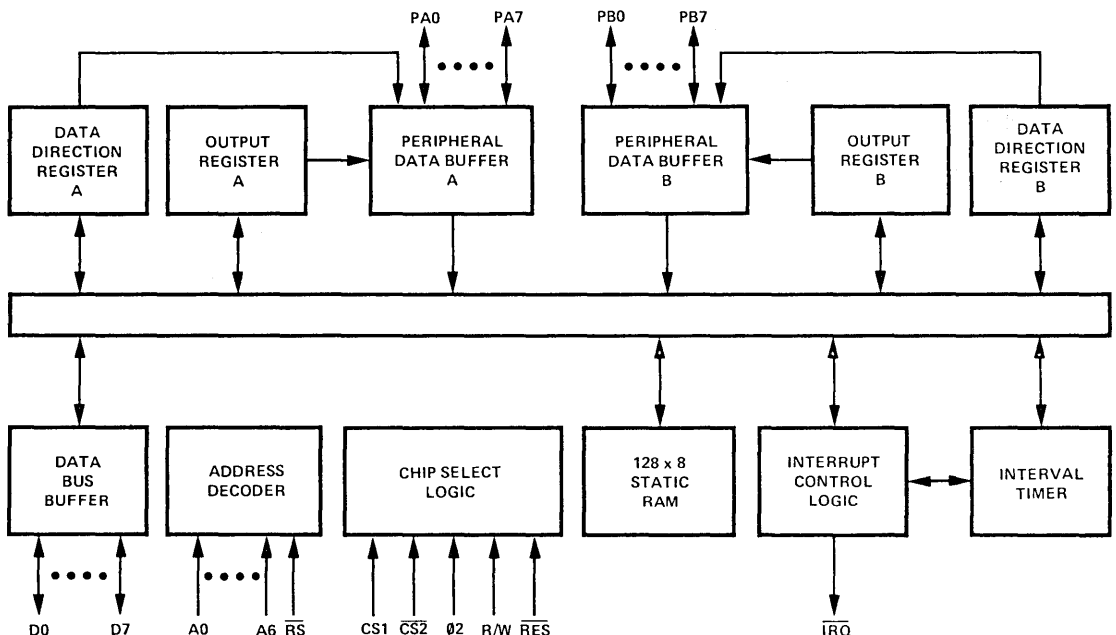
SY6532

MICROPROCESSOR PRODUCTS

The SY6532 is designed to operate in conjunction with the SY6500 Microprocessor Family. It is comprised of a 128 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, a software programmable interval timer with interrupt capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect interrupt circuit.

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- Programmable edge-sensitive interrupt
- 128 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins

Figure 1. 6532 BLOCK DIAGRAM



MICRO-PROCESSORS

MAXIMUM RATINGS

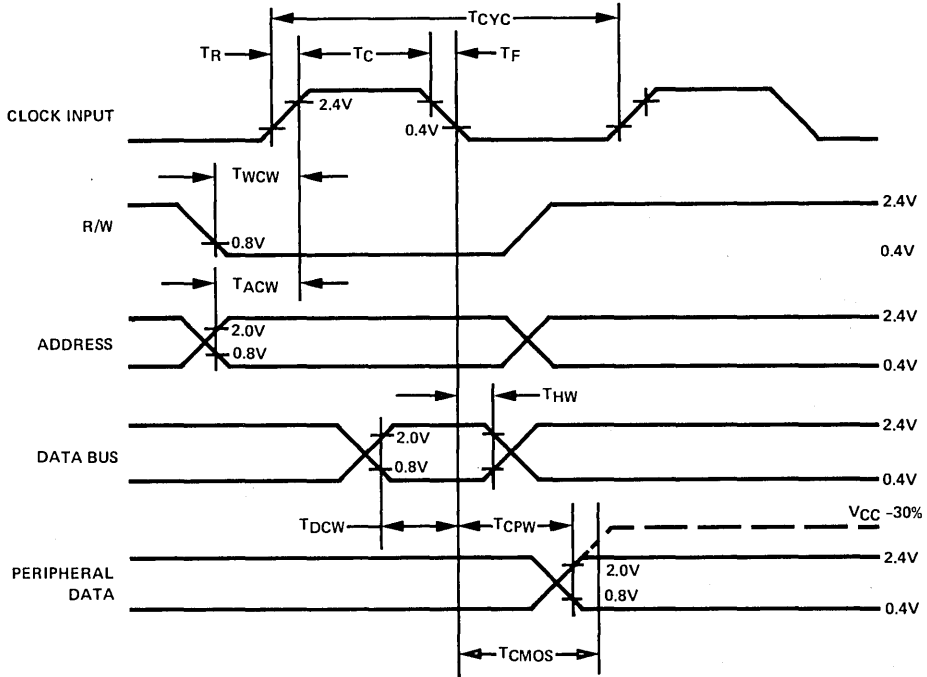
RATING	SYMBOL	VOLTAGE	UNIT
Supply Voltage	V _{CC}	-.3 to +7.0	V
Input/Output Voltage	V _{IN}	-.3 to +7.0	V
Operating Temperature Range	T _{OP}	0 to 70	°C
Storage Temperature Range	T _{STG}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = 25° C)

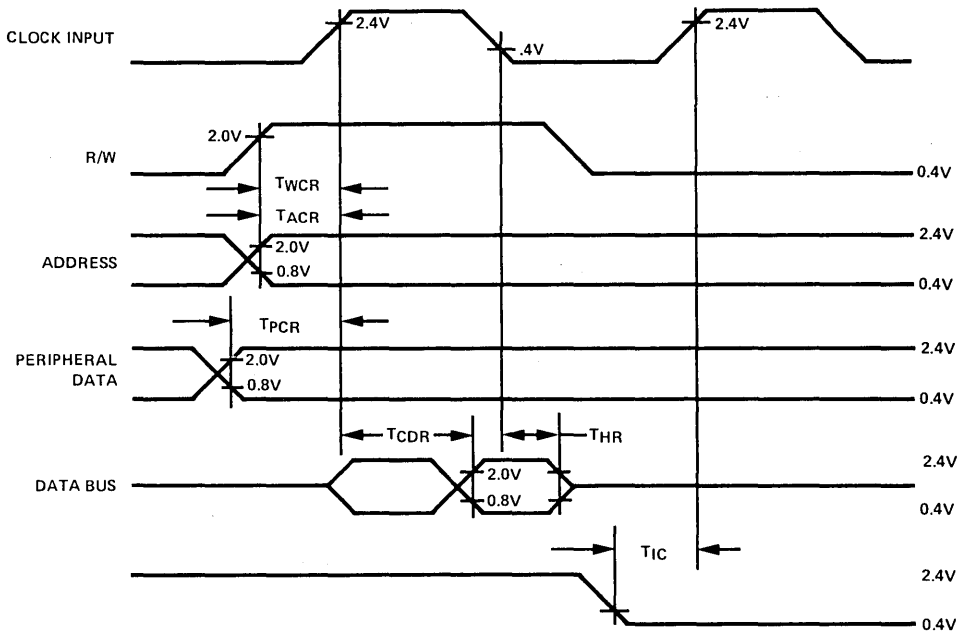
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V _{IH}	V _{SS} + 2.4		V _{CC}	V
Input Low Voltage	V _{IL}	V _{SS} - .3		V _{SS} + .4	V
Input Leakage Current; V _{IN} = V _{SS} + 5V A ϕ -A6, RS, R/W, RES, ϕ 2, CS1, CS2	I _{IN}		1.0	2.5	μ A
Input Leakage Current for High Impedance State (Three State); V _{IN} = .4V to 2.4V; D ϕ -D7	I _{TSI}		±1.0	±10.0	μ A
Input High Current; V _{IN} = 2.4V PA ϕ -PA7, PB ϕ -PB7	I _{IH}	-100.	-300.		μ A
Input Low Current; V _{IN} = .4V PA ϕ -PA7, PB ϕ -PB7	I _{IL}		-1.0	-1.6	MA
Output High Voltage V _{CC} = MIN, I _{LOAD} ≤ -100 μ A (PA ϕ -PA7, PB ϕ -PB7, D ϕ -D7) I _{LOAD} ≤ 3 MA (PB ϕ -PB7)	V _{OH}	V _{SS} + 2.4 V _{SS} + 1.5			V
Output Low Voltage V _{CC} = MIN, I _{LOAD} ≤ 1.6MA	V _{OL}			V _{SS} + .4	V
Output High Current (Sourcing); V _{OH} ≥ 2.4V (PA ϕ -PA7, PB ϕ -PB7, D ϕ -D7) ≥ 1.5V Available for direct transistor drive (PB ϕ -PB7)	I _{OH}	-100 3.0	-1000 5.0		μ A MA
Output Low Current (Sinking); V _{OL} ≤ .4V	I _{OIL}	1.6			MA
Clock Input Capacitance	C _{Clk}			30	pf
Input Capacitance	C _{IN}			10	pf
Output Capacitance	C _{OUT}			10	pf
Power Dissipation	I _{CC}		100	125	mA

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

WRITE TIMING CHARACTERISTICS



READ TIMING CHARACTERISTICS



WRITE TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Period	TCYC	1			μ S
Rise & Fall Times	TR, TF			25	NS
Clock Pulse Width	TC	470			NS
R/W valid before positive transition of clock	TWCW	180			NS
Address valid before positive transition of clock	TACW	180			NS
Data Bus valid before negative transition of clock	TDCW	300			NS
Data Bus Hold Time	THW	10			NS
Peripheral data valid after negative transition of clock	TCPW			1	μ S
Peripheral data valid after negative transition of clock driving CMOS (Level = $V_{CC} = 30\%$)	TCMOS			2	μ S

READ TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
R/W valid after positive transition of clock	TWCR	180			NS
Address valid before positive transition of clock	TACR	180			NS
Peripheral data valid before positive transition of clock	TPCR	300			NS
Data Bus valid after positive transition of clock	TCDR			395	NS
Data Bus Hold Time	THR	10			NS
\overline{IRQ} (Interval Timer Interrupt) valid before positive transition of clock	TIC	200			NS

Loading = 30 pf + 1 TTL load for PA \emptyset -PA7, PB \emptyset -PB7
 = 130 pf + 1 TTL load for D \emptyset -D7

INTERFACE SIGNAL DESCRIPTION

Reset (\overline{RES})

During system initialization a Logic "0" on the \overline{RES} input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the \overline{RES} signal. The \overline{RES} signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or high level clock ($V_{IL} < 0.2$, $V_{IH} = V_{CC} \begin{smallmatrix} +.3 \\ -.2 \end{smallmatrix}$).

Read/Write (R/W)

The R/W signal is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the SY6532. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the SY6532. A low on the R/W pin allows a write (with proper addressing) to the SY6532.

Interrupt Request (\overline{IRQ})

The \overline{IRQ} pin is an interrupt pin from the interrupt control logic. It will be normally high with a low indicating an interrupt from the SY6532. \overline{IRQ} is an open-drain output, permitting several units to be wire-or'ed to the common \overline{IRQ} microprocessor input pin. The \overline{IRQ} pin may be activated by a transition on PA7 or timeout of the interval timer.

Data Bus (D0-D7)

The SY6532 has eight bi-directional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports

The SY6532 has 16 pins available for peripheral I/O operations. Each pin is individually programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0-PA7 and PB0-PB7. PA7 may also function as an interrupt input pin. This feature is described in another section. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the SY6532 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.4 volts for a "1" and less than 0.4 volts for a "0" as the peripheral pins are all TTL compatible. Pins PB0-PB7 are also capable of sourcing 3 ma at 1.5 v thus making them capable of direct transistor drive.

Address Lines (A0-A6)

There are 7 address pins. In addition to these, there is the \overline{RS} pin. The above pins, A0-A6 and \overline{RS} , are always used as addressing pins. There are 2 additional pins which are used as CHIP SELECTS. They are pins CS1 and $\overline{CS2}$.

INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The SY6532 is divided into four basic sections: RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O register.

RAM 128 Bytes (1024 Bits)

A 128 x 8 static RAM is contained on the SY6532. It is addressed by A0-A6 (Byte Select), \overline{RS} , CS1, and $\overline{CS2}$.

Internal Peripheral Registers

There are four 8-bit internal registers: two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of data into and out of the peripheral I/O pins. A logic zero in a bit of the data direction register (DDRA and DDRB) causes the corresponding pin of the I/O port to act as an input. A logic one causes the corresponding pin to act as an output. The voltage on any pin programmed as an output is determined by the corresponding bit in the output register (ORA and ORB).

Data is read directly from the PA pins during a peripheral read operation. Thus, for a PA pin programmed as an output, the data transferred into the processor will be the same as the data in the ORA only if the voltage on the pin is allowed to be ≥ 2.4 volts for a logic one and ≤ 0.4 volts for a zero. If the loading on the pin does not allow this, then the data resulting from the read operation may not match the contents of ORA.

The output buffers for the PB pins are somewhat different from the PA buffers. The PB buffers are push-pull devices which are capable of sourcing 3ma at 1.5 volts. This allows for these pins to directly drive transistor circuits. To assure that the processor will read the proper data when performing a peripheral read operation, logic is provided in the peripheral B port to permit the processor to read the contents of ORB, instead of the PB pins as is the case for the PA port.

Interval Timer

The timer section of the SY6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 2.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, and interrupt flag is set to a logic "1." After the interrupt flag is set the internal clock begins counting down to a maximum of $-255T$. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

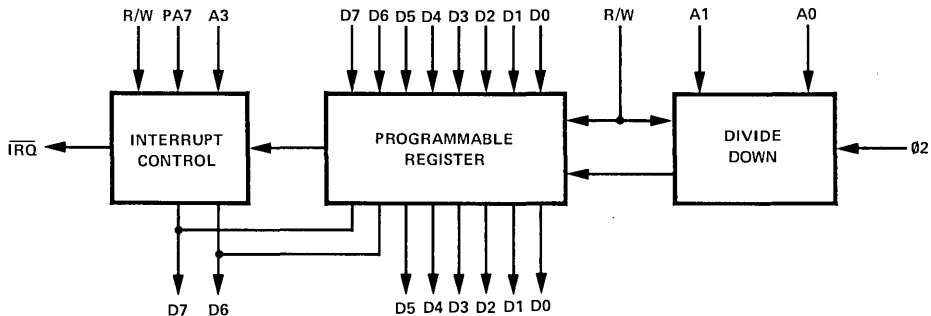
The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of \overline{IRQ} , i.e., A3 = 1 enables \overline{IRQ} , A3 = 0 disables \overline{IRQ} . In either case, when timeout occurs, bit 7 of the Interrupt Flag Register is set. This flag is cleared when the Timer register is either read from or written to by the processor. If \overline{IRQ} is enabled by A3 and an interrupt occurs \overline{IRQ} will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the timer has counted down to 00000000 on the next count time an interrupt will occur and the counter will read 11111111. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 11100100 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read	= 11100100
Complement	= 00011011
Add 1	= 00011100 = 28.

Figure 2. BASIC ELEMENTS OF INTERVAL TIMER

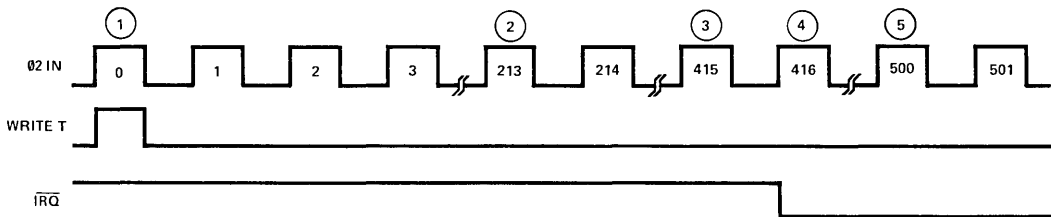


Thus, to arrive at the total elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 00110100 (=52). With a divide by 8, total time to interrupt is $(52 \times 8) + 1 = 417T$. Total elapsed time would be $416T + 28T = 444T$, assuming the value read after interrupt was 11100100.

After interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 3 illustrates an example of interrupt.

Figure 3. TIMER INTERRUPT TIMING



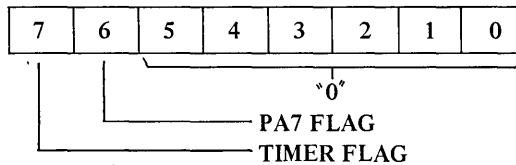
1. Data written into interval timers is $00110100 = 52_{10}$
2. Data in Interval timer is $00011001 = 25_{10}$
 $52 - \frac{213}{8} - 1 = 52 - 26 - 1 = 25$
3. Data in Interval timer is $00000000 = 0_{10}$
 $52 - \frac{415}{8} - 1 = 52 - 51 - 1 = 0$
4. Interrupt has occurred at $\Phi 2$ pulse #416
 Data in Interval timer = 11111111
5. Data in Interval timer is 10101100
 two's complement is $01010100 = 84_{10}$
 $84 + (52 \times 8) = 500_{10}$

When reading the timer after an interrupt, A3 should be low so as to disable the \overline{IRQ} pin. This is done so as to avoid future interrupts until after another Write operation.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits: the timer interrupt flag and the PA7 interrupt flag. When a read operation is performed on the Interrupt Flag Register, the bits are transferred to the processor on the data bus, as the diagram below, indicates.

Figure 4. INTERRUPT FLAG REGISTER



The PA7 flag is cleared when the Interrupt Flag Register is read. The timer flag is cleared when the timer register is either written or read.

ADDRESSING

Addressing of the SY6532 is accomplished by the 7 addressing pins, the \overline{RS} pin and the two chip select pins CS1 and $\overline{CS2}$. To address the RAM, CS1 must be high with $\overline{CS2}$ and \overline{RS} low. To address the I/O and Interval timer CS1 and \overline{RS} must be high with $\overline{CS2}$ low. As can be seen to access the chip CS1 is high and $\overline{CS2}$ is low. To distinguish between RAM or I/O Timer the \overline{RS} pin is used. When this pin is low the RAM is addressed, when high the I/O Interval timer section is addressed. To distinguish between timer and I/O address line A2 is utilized. When A2 is high the interval timer is accessed. When A2 is low the I/O section is addressed. Table 1 illustrates the chip addressing.

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, the PA7 pin can function as an edge sensitive input. In this mode, an active transition on PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, and providing the PA7 interrupt is enabled, the \overline{IRQ} output will go low.

Control of the PA7 edge detecting logic is accomplished by performing a write operation to one of four addresses. The data lines for this operation are "don't care" and the addresses to be used are found in Figure 4.

The setting of the internal interrupt flag by an active transition on PA7 is always enabled, no matter whether PA7 is set up as an input or an output.

The \overline{RES} signal disables the PA7 interrupt and sets the active transition to the negative edge-detect state. During the reset operation, the interrupt flag may be set by a negative transition. It may, therefore, be necessary to clear the flag before its normal use as an edge detecting input is enabled. This can be achieved by reading the Interrupt Flag Register, as defined by Figure 4 immediately after reset.

I/O Register - Timer Addressing

Table 1 illustrates the address decoding for the internal elements and timer programming. Address line A2 distinguishes I/O registers from the timer. When A2 is low and \overline{RS} is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

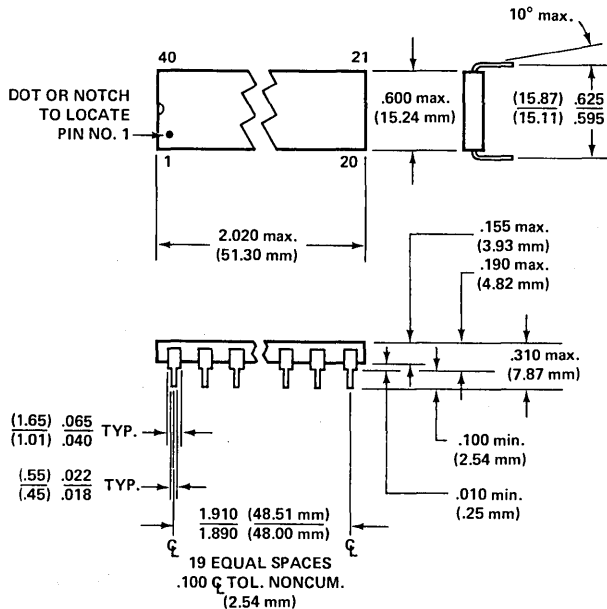
When the timer is selected A1 and A0 decode the "divide-by" matrix. This decoding is defined in Table 1. In addition, Address A3 is used to enable the interrupt flag to \overline{IRQ} .

Table 1 ADDRESSING DECODE

OPERATION	\overline{RS}	R/W	A4	A3	A2	A1	A0
Write RAM	0	0	—	—	—	—	—
Read RAM	0	1	—	—	—	—	—
Write DDRA	1	0	—	—	0	0	1
Read DDRA	1	1	—	—	0	0	1
Write DDRB	1	0	—	—	0	1	1
Read DDRB	1	1	—	—	0	1	1
Write Output Reg A	1	0	—	—	0	0	0
Read Output Reg A	1	1	—	—	0	0	0
Write Output Reg B	1	0	—	—	0	1	0
Read Output Reg B	1	1	—	—	0	1	0
Write Timer							
÷ 1T	1	0	1	(a)	1	0	0
÷ 8T	1	0	1	(a)	1	0	1
÷ 64T	1	0	1	(a)	1	1	0
÷ 1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	—	(a)	1	—	0
Read Interrupt Flag	1	1	—	—	1	—	1
Write Edge Detect Control	1	0	0	—	1	(b)	(c)

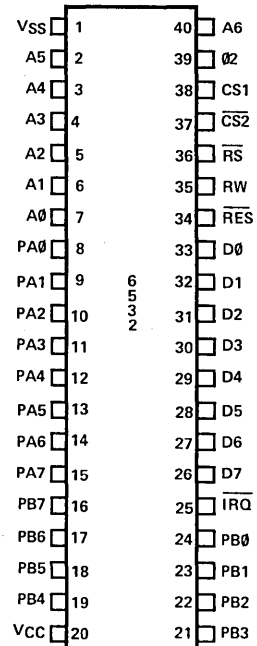
- NOTES: — = Don't Care, "1" = High level ($\geq 2.4V$), "0" = Low level ($\leq 0.4V$)
- (a) A3 = 0 to disable interrupt from timer to \overline{IRQ}
 A3 = 1 to enable interrupt from timer to \overline{IRQ}
 - (b) A1 = 0 to disable interrupt from PA7 to \overline{IRQ}
 A1 = 1 to enable interrupt from PA7 to \overline{IRQ}
 - (c) A0 = 0 for negative edge-detect
 A0 = 1 for positive edge-detect

PACKAGE OUTLINE



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

PIN DESIGNATION



MICRO-PROCESSORS



CRT Controller

SY6545

MICROPROCESSOR PRODUCTS

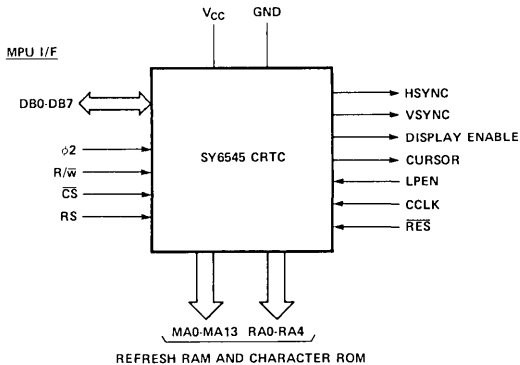
PRELIMINARY

- Single +5 volt ($\pm 5\%$) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character refresh RAM.
- No DMA required.
- Pin-compatible with MC6845.
- Row/Column or straight-binary addressing for refresh RAM.
- Refresh RAM may be configured as part of microprocessor memory field or independently slaved to 6545.
- Internal 8-bit status register.
- CRTC-controlled memory update modes: Interleaved and during blanking

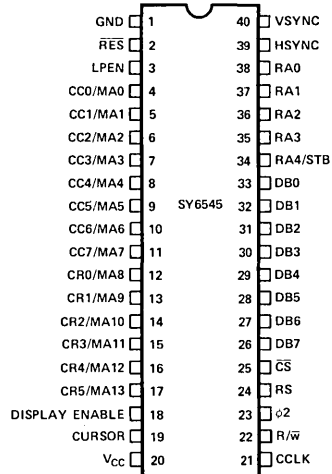
The SY6545 is a CRT Controller intended to provide capability for interfacing the 6500/6800 microprocessor families to CRT or TV-type raster scan displays. A unique

feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

INTERFACE DIAGRAM



PIN DESIGNATION



MICRO-PROCESSORS

MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.3V to +7.0V
Input/Output Voltage, V_{IN}	-0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	-55°C to 150°C

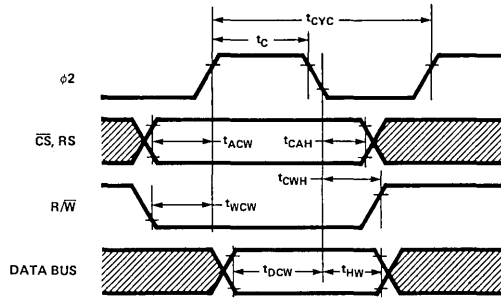
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $T_A = 25^\circ C$, unless otherwise noted)

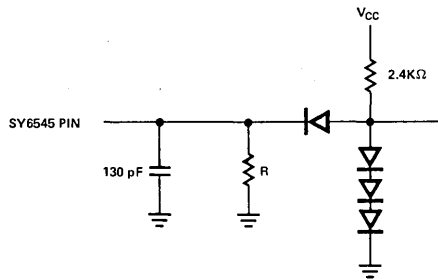
Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage	2.0	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	0.8	V
I_{IN}	Input Leakage ($\phi 2$, R/\bar{w} , \overline{RES} , \overline{CS} , RS, LPEN, CCLK)	—	2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) $V_{IN} = 0.4$ to $2.4V$	—	10.0	μA
V_{OH}	Output High Voltage $I_{LOAD} = 205\mu A$ (DB0-DB7) $I_{LOAD} = 100\mu A$ (all others)	2.4	—	V
V_{OL}	Output Low Voltage $I_{LOAD} = 1.6mA$	—	0.4	V
P_D	Power Dissipation	—	700	mW
C_{IN}	Input Capacitance $\phi 2$, R/\bar{w} , \overline{RES} , \overline{CS} , RS, LPEN, CCLK DB0-DB7	—	10.0	pF
		—	12.5	pF
C_{OUT}	Output Capacitance	—	10.0	pF

WRITE TIMING CHARACTERISTICS


($V_{CC} = 5.0V \pm 5\%$, $T_A = 0$ to $70^\circ C$, unless otherwise noted)

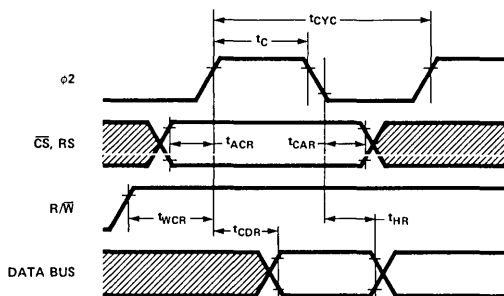
Symbol	Characteristic	SY6545		SY6545A		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	40	0.5	40	μs
t_c	$\phi 2$ Pulse Width	470	—	235	—	ns
t_{ACW}	Address Set-Up Time	180	—	90	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/\bar{W} Set-Up Time	180	—	90	—	ns
t_{CWH}	R/\bar{W} Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	300	—	150	—	ns
t_{HW}	Data Bus Hold Time	10	—	10	—	ns

(t_r and $t_f = 10$ to 30 ns)

TEST LOAD


R = 11K Ω FOR DB₀-DB₇
 = 24K Ω FOR ALL OTHER OUTPUTS

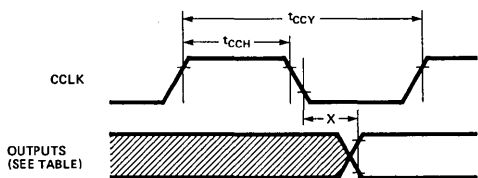
MICRO-PROCESSORS

READ TIMING CHARACTERISTICS


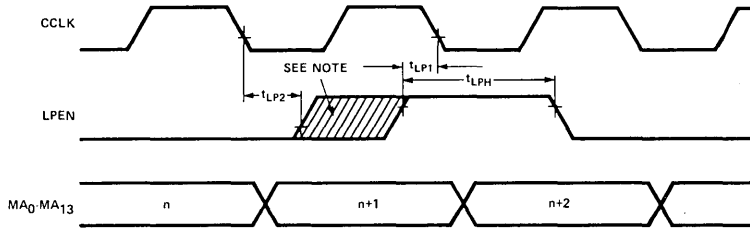
($V_{CC} = 5.0V \pm 5\%$, $T_A = 0$ to $70^\circ C$, unless otherwise noted)

Symbol	Characteristic	SY6545		SY6545A		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	40	0.5	40	μs
t_c	$\phi 2$ Pulse Width	470	—	235	—	ns
t_{ACR}	Address Set-Up Time	180	—	90	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/w Set-Up Time	180	—	90	—	ns
t_{CDR}	Read Access Time	—	395	—	200	ns
t_{HR}	Read Hold Time	10	—	10	—	ns

(t_r and $t_f = 10$ to 30 ns)

SYSTEM TIMING DEFINITIONS


Output	Parameter
MA0-MA13	t_{MAD}
RA0-RA4	t_{RAD}
DISPLAY-ENABLE	t_{DTD}
HSYNC	t_{HSD}
VSYNC	t_{VSD}
CURSOR	t_{CDD}

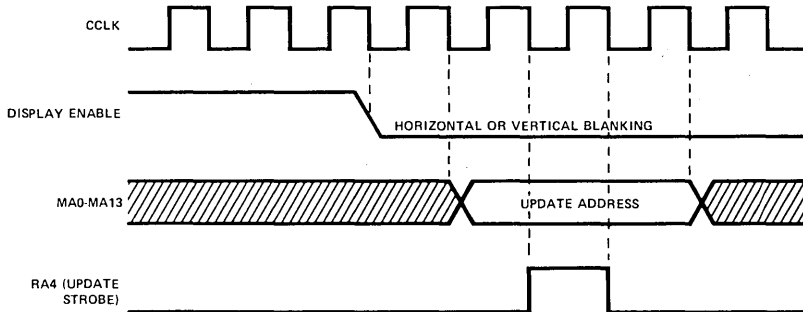
LIGHT PEN STROBE TIMING DEFINITIONS


NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register.
 t_{LP2} and t_{LP1} are time positions causing uncertain results.

SYSTEM TIMING PARAMETERS ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0$ to $70^\circ C$, unless otherwise noted)

Symbol	Characteristics	SY6545		SY6545A		Unit
		Min.	Max.	Min.	Max.	
t_{CCY}	Character Clock Cycle Time	400	—	400	—	ns
t_{CCH}	Character Clock Pulse Width	200	—	200	—	ns
t_{MAD}	MA0-MA13 Propagation Delay	—	160	—	160	ns
t_{RAD}	RA0-RA4 Propagation Delay	—	160	—	160	ns
t_{DTD}	DISPLAY ENABLE Propagation Delay	—	300	—	300	ns
t_{HSD}	HSYNC Propagation Delay	—	300	—	300	ns
t_{VSD}	VSYSN Propagation Delay	—	300	—	300	ns
t_{CDD}	CURSOR Propagation Delay	—	300	—	300	ns
t_{LPH}	LPEN Strobe Width	100	—	100	—	ns
t_{LP1}	LPEN to CCLK Delay	120	—	120	—	ns
t_{LP2}	CCLK to LPEN Delay	0	—	—	—	ns

$t_r, t_f = 20$ ns (max)

LOGICAL TIMING FOR UPDATE STROBE


MPU INTERFACE SIGNAL DESCRIPTION

$\phi 2$ (Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system microprocessor and the SY6545.

R/\bar{w} (Read/Write)

The R/\bar{w} signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/\bar{w} pin allows the processor to read the data supplied by the SY6545; a low on the R/\bar{w} pin allows a write to the SY6545.

\bar{CS} (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The SY6545 is selected when \bar{CS} is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0 - DB_7 (Data Bus)

The DB_0 - DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6545. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the SY6545 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. Display Enable can be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable.

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

\bar{RES}

The \bar{RES} signal is an active-low input used to initialize all internal scan counter circuits. When \bar{RES} is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. \bar{RES} must stay low for at least one CCLK period. All scan timing is initiated when \bar{RES} goes high. In this way, \bar{RES} can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0-MA13 (Refresh RAM Address Lines)

These signals are active-high outputs and are used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode, characters are stored in successive memory locations. Thus, the software must be designed so that row and column character co-ordinates are translated into sequentially-numbered addresses. In the row/column mode MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.



RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

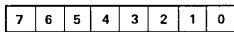
The high-order line, RA4, is unique in that it can also function as a strobe output pin when the SY6545 is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Refresh RAM update address is gated on to the address lines, MA0-MA13. In this way, updates and readouts of the Refresh RAM can be made under control of the SY6545 with only a small amount of external circuitry.

Address Register

This is a 5-bit register which is used as a "pointer" to direct CRT/MPU data transfers within the CRT. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This 3-bit register is used to monitor the status of the CRT, as follows:



- NOT USED
- VERTICAL RE-TRACE
"0" Scan currently not in vertical re-trace portion of its timing.
"1" Scan currently is in its vertical re-trace time.
- LPEN REGISTER FULL
"0" This bit goes to "0" whenever either register R16 or R17 is read by the MPU.
"1" This bit goes to "1" whenever a LPEN strobe occurs.
- UPDATE READY
"0" This bit goes to "0" when register R31 has been either read or written by the MPU.
"1" This bit goes to "1" when an Update Strobe occurs.

Note: The Status Register takes the state,

1	0	1	-	-	-	-	-
---	---	---	---	---	---	---	---

, immediately after power (V_{CC}) turn-on.

Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

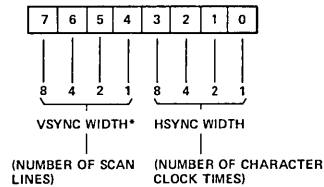
This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the horizontal SYNC on the horizontal line, in terms of the character location number on the line.

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Vertical Total (R4) and Vertical Total Adjust (R5)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame. The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan. These two registers together determine the overall frame frequency and, consequently, the frequency of the VSYNC pulse.

Vertical Displayed (R6)

This 7-bit register contains the number of displayed character rows in each frame.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the vertical SYNC pulse is desired to occur.

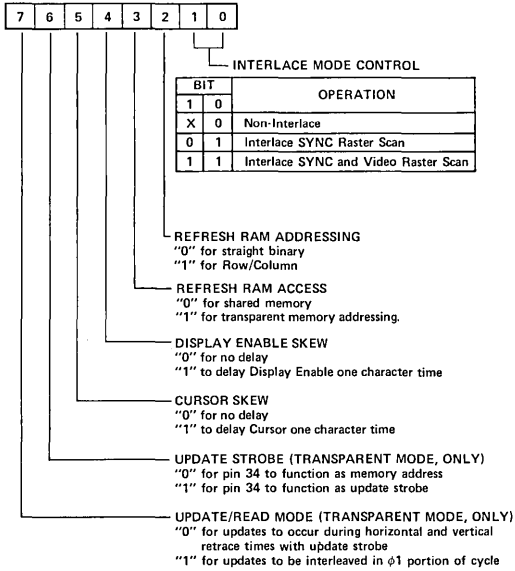
INTERNAL REGISTER DESCRIPTION

CS	RS	Address Reg.					Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit										
		4	3	2	1	0						7	6	5	4	3	2	1	0			
1	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X
0	0	X	X	X	X	X	X	Address Reg.	Reg. No.		√	X	X	X	X	4	3	2	1	0		
0	0	X	X	X	X	X	X	Status Reg.		√		7	6	5	X	X	X	X	X			
0	1	0	0	0	0	0	0	R0 Horiz. Total	# Charac.		√	7	6	5	4	3	2	1	0			
0	1	0	0	0	0	0	1	R1 Horiz. Displayed	# Charac.		√	7	6	5	4	3	2	1	0			
0	1	0	0	0	0	1	0	R2 Horiz. Sync Position	# Charac.		√	7	6	5	4	3	2	1	0			
0	1	0	0	0	1	1		R3 VSYNC, HSYNC Widths	# Scan Lines/ # Char.		√	7	6	5	4	3	2	1	0			
0	1	0	0	1	0	0		R4 Vert. Total	# Charac. Row		√	X	6	5	4	3	2	1	0			
0	1	0	0	1	0	1		R5 Vert. Total Adjust	# Scan Lines		√	X	X	X	4	3	2	1	0			
0	1	0	0	1	1	0		R6 Vert. Displayed	# Charac. Rows		√	X	6	5	4	3	2	1	0			
0	1	0	0	1	1	1		R7 Vert. Sync Position	# Charac. Rows		√	X	6	5	4	3	2	1	0			
0	1	0	1	0	0	0		R8 Mode Control			√	7	6	5	4	3	2	1	0			
0	1	0	1	0	0	1		R9 Scan Line	# Scan Lines		√	X	X	X	4	3	2	1	0			
0	1	0	1	0	1	0		R10 Cursor Start	Scan Line No.		√	X	B	P	4	3	2	1	0			
0	1	0	1	0	1	1		R11 Cursor End	Scan Line No.		√	X	X	X	4	3	2	1	0			
0	1	0	1	1	0	0		R12 Display Start Addr (H)			√	X	X	5	4	3	2	1	0			
0	1	0	1	1	0	1		R13 Display Start Addr (L)			√	7	6	5	4	3	2	1	0			
0	1	0	1	1	1	0		R14 Cursor Position (H)		√	√	X	X	5	4	3	2	1	0			
0	1	0	1	1	1	1		R15 Cursor Position (L)		√	√	7	6	5	4	3	2	1	0			
0	1	1	0	0	0	0		R16 Light Pen Reg (H)		√		X	X	5	4	3	2	1	0			
0	1	1	0	0	0	1		R17 Light Pen Reg (L)		√		7	6	5	4	3	2	1	0			
0	1	1	0	0	1	0		R18 Update Location (H)			√	X	X	5	4	3	2	1	0			
0	1	1	0	0	1	1		R19 Update Location (L)			√	7	6	5	4	3	2	1	0			
0	1	1	1	1	1	1		R31 Dummy Location				X	X	X	X	X	X	X	X	X	X	X

Table 1. Overall Register Structure and Addressing

Mode Control (R8)

This register is used to select the operating modes of the CRTC and is outlined, as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as described later in this document.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the address of the first character of the displayed scan.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the current position of the cursor.

Light Pen High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position. When the LPEN signal makes a transition from high to low, the contents of the internal scan counter is gated into the light pen register.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register whose contents is the refresh RAM address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not exist, but is required to detect when Refresh RAM updates occur. This is necessary for the "transparent" addressing only, and is used to increment the Update Address Register and to set the Update Ready bit in the status register.

Register Formats

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

DESCRIPTION OF OPERATION

Refresh RAM Addressing

There are two modes of addressing for the refresh RAM (or character storage RAM):

1. Shared Memory

In this mode the memory is shared between the MPU address bus and the CRTC address bus. For this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the CRTC must have access to the refresh RAM and the contention circuits must resolve this multiple access requirement.

2. Transparent Memory

For this mode, the refresh RAM is not directly accessible by the MPU, but is controlled entirely by the CRTC. All MPU accesses are made via the CRTC and a small amount of external circuits.

Detailed examples of how each of these modes is implemented are described later in this spec.

In addition, there are two addressing organizations selectable:

1. Row/Column

In this mode, the CRTC address lines (MA0-MA13) are generated as 8 column (MA0-MA7) and 6 row (MA8-MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM.

2. Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity is increased since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential.

Cursor Operation

The Cursor Start (R10) and End (R11) Registers permit a variable number of scan lines for the cursor output signal. In addition, 5 and 6 of register R10 select blinking modes, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 1/16 field rate
1	1	Blink at 1/32 field rate

Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field. Cursor can be delayed by one character time by setting bit 5 of R8 to a "1".

Interlace Modes

There are three raster-scan display modes (see Figure 1).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields

alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace-Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields and results in enhanced readability.

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields.

Some restrictions on interlace mode operation are:

a) The Horizontal Total Character count (register R0) must be odd, in order to represent an even number of character times.

b) For Interlaced Sync and Video mode, only, the following registers must be programmed in a non-standard fashion:

- R4 (Vertical Total) must be programmed to one-half the actual number desired, minus one. For example, for a total of 24 characters high, R4 must contain 11 (decimal).

- R6 (Vertical Displayed) must be programmed to one-half the actual number desired. For example, for 16 displayed characters high, R6 must contain 8 (decimal).

- R7 (Vertical Sync Position) must be programmed to one-half the actual number desired, identical to R6.

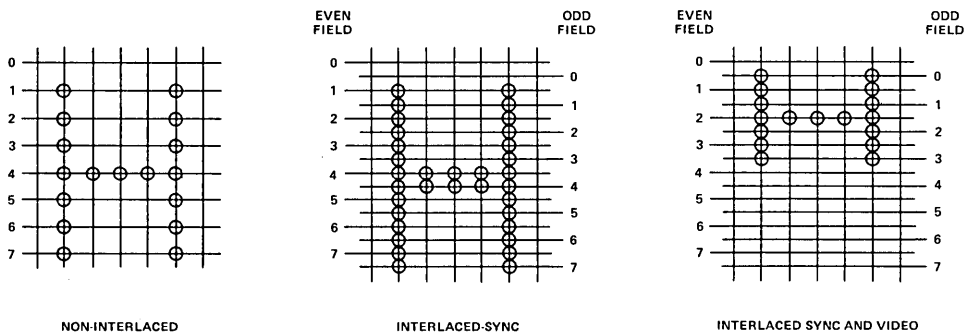


Figure 1. Illustration of the various scan modes for the example of the letter "H" in a 5x7 font.

REFRESH RAM ADDRESSING

Shared Memory Mode

In this mode, the Refresh RAM address lines (MA0-MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the MPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0-MA7 become character column addresses (CC0-CC7) and MA8-MA13 become character row addresses (CR0-CR5).

Transparent Memory Mode

In this mode, the RAM address lines (MA0-MA13) switch between the internal refresh scan counter and the update register, based on the update/read mode selected (register R8).

- a) No update strobe (register R8, bit 6 a "0"). In this case, package pin 34 functions as RA4, not as update strobe. This selection should be made only when one of the following modes is used:
1. "SHARED" memory mode.
 2. "TRANSPARENT" memory mode requiring 16 Scan lines/character using interleaved updating of refresh RAM, so control can be external to CRTC. For this case, then MA0-MA13 reflect the update register during $\phi 1$ time and the scan counter during $\phi 2$.
- b) Interleaved Updates (register R8, bit 7 a "1"). In this case the address lines reflect the update register during $\phi 1$ time and the scan counter during $\phi 2$.
- c) Horizontal and Vertical Retrace updates (R8, bit 7 a "0"). In this case, the update strobe is used to indicate when the update address is present on the address lines. This will occur during the first available re-trace time and the strobe is used to enable external circuits to write or read the Refresh RAM. The CRTC is alerted that data has been latched into the external circuits by a write into register R31. Although data is not stored in the CRTC, the CRTC now operates to enable the update. When the update occurs (strobe and address), the status register indicates this (bit 7 becomes a "1") and subsequent writes into R31 cause the process to repeat (each time, the update counter advances). Reading the Refresh RAM is accomplished in a like manner.



Asynchronous Communication Interface Adapter

SY6551

MICROPROCESSOR PRODUCTS

Preliminary

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud).
- Programmable interrupt and status register to simplify software design.
- Single +5 volt power supply.
- Serial echo mode.
- False start bit detection.
- 8-bit bi-directional data bus for direct communication with the microprocessor.
- External 16x clock input for non-standard baud rates (up to 125 Kbaud).
- Programmable: word lengths; number of stop bits; and parity bit generation and detection.
- Data set and modem control signals provided.
- Parity: (odd, even, none, mark, space).
- Full-duplex or half-duplex operation.
- 5, 6, 7, 8 and 9 bit transmission.

The SY6551 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication

data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

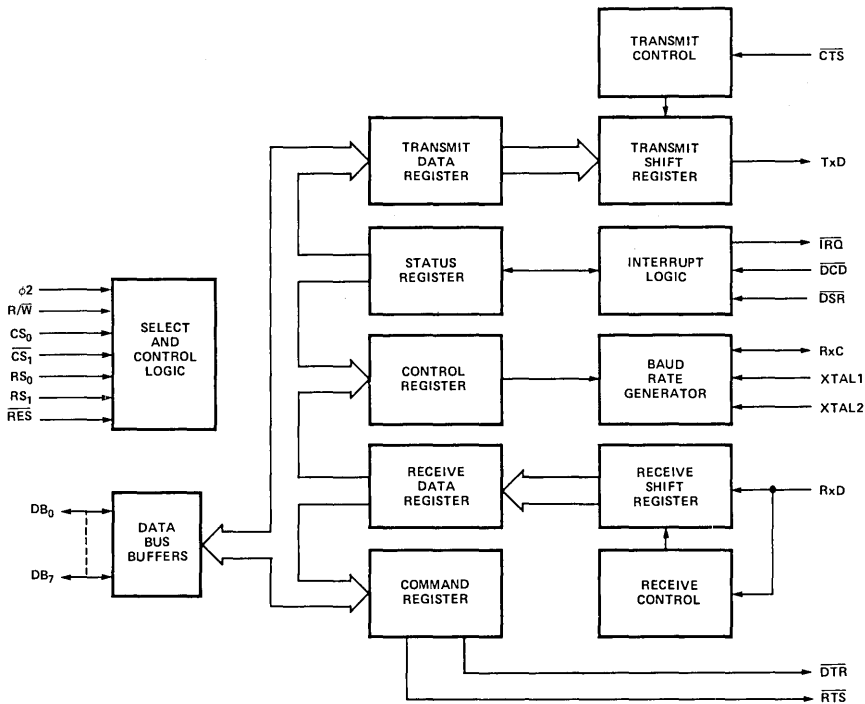


Figure 1. Block Diagram

MICRO-PROCESSORS



ABSOLUTE MAXIMUM RATINGS

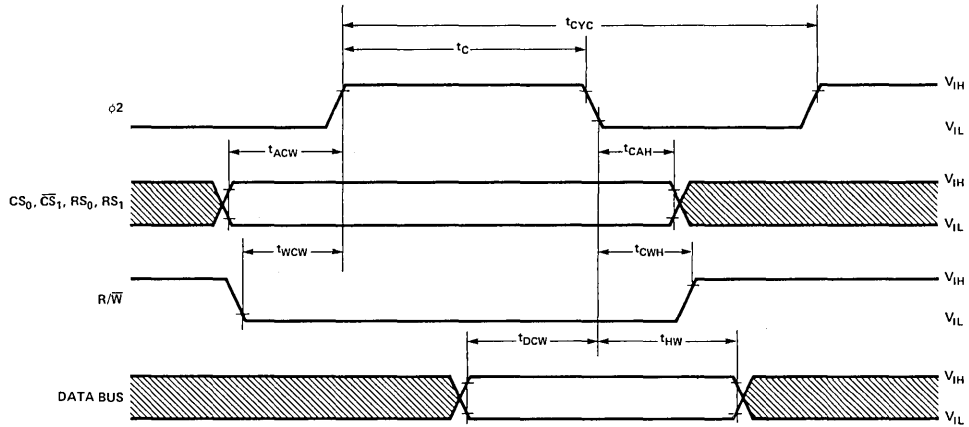
Rating	Symbol	Allowable Range
Supply Voltage	V_{CC}	-0.3V to +7.0V
Input/Output Voltage	V_{IN}	-0.3V to +7.0V
Operating Temperature	T_{OP}	0°C to 70°C
Storage Temperature	T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

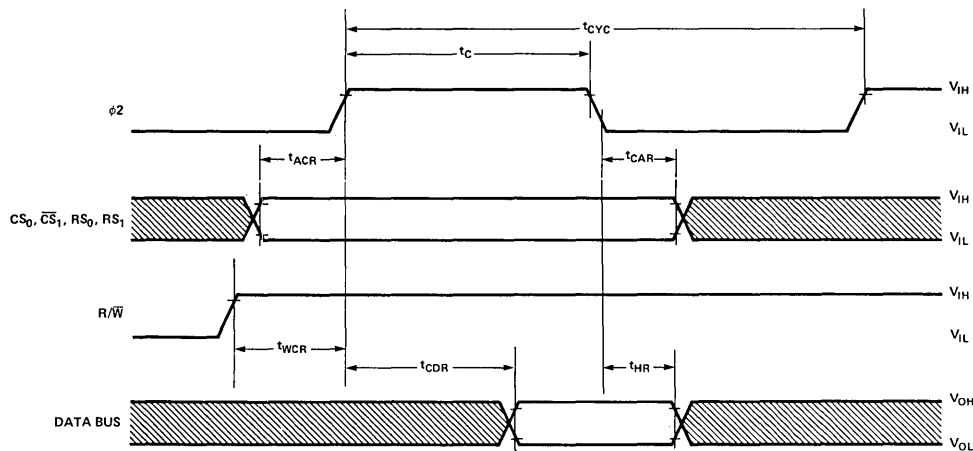
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $T_A = 25^\circ C$, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V
Input Leakage Current: $V_{IN}=0$ to 5V. ($\phi 2$, $\overline{R/W}$, \overline{RES} , CS_0 , $\overline{CS_1}$, RS_0 , RS_1 , \overline{CTS} , RxD , \overline{DCD} , \overline{DSR})	I_{IN}	—	± 1.0	± 2.5	μA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	—	± 2.0	± 10.0	μA
Output High Voltage: $I_{LOAD}=-100\mu A$	V_{OH}	2.4	—	—	V
Output Low Voltage: $I_{LOAD}=1.6mA$ ($\overline{DB_0-DB_7}$, TxD , RxC , \overline{RTS} , \overline{DTR} , \overline{IRQ})	V_{OL}	—	—	0.4	V
Output High Current (Sourcing): $V_{OH}=2.4V$	I_{OH}	-100	-1000	—	μA
Output Low Current (Sinking): $V_{OL}=0.4V$	I_{OL}	1.6	—	—	μA
Output Leakage Current (off state): $V_{OUT}=5V$ (\overline{IRQ})	I_{OFF}	—	1.0	10.0	μA
Clock Capacitance ($\phi 2$)	C_{CLK}	—	—	20	pF
Input Capacitance (except XTAL1 and XTAL2)	C_{IN}	—	—	10	pF
Output Capacitance	C_{OUT}	—	—	10	pF
Power Dissipation	P_D	—	350	500	mw


Figure 2. Write Timing Characteristics
WRITE CYCLE ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0$ to $70^\circ C$, unless otherwise noted)

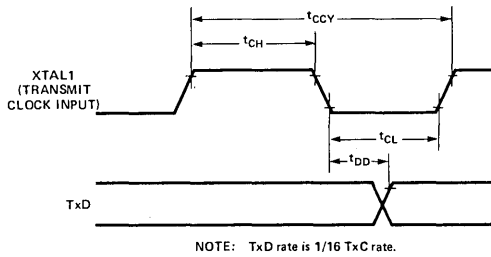
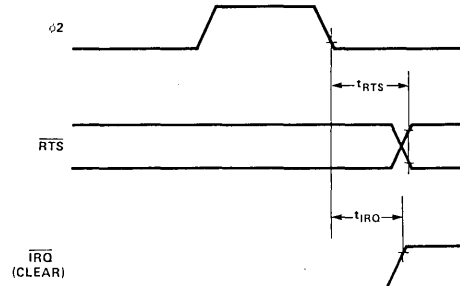
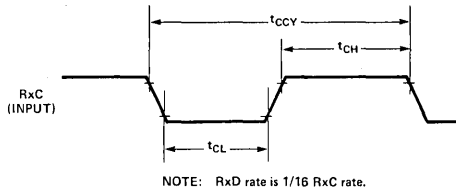
Characteristic	Symbol	SY6551		SY6551A		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	μs
$\phi 2$ Pulse Width	t_C	470	—	235	—	ns
Address Set-Up Time	t_{ACW}	180	—	90	—	ns
Address Hold Time	t_{CAH}	0	—	0	—	ns
R/\overline{W} Set-Up Time	t_{WCW}	180	—	90	—	ns
R/\overline{W} Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	300	—	150	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	ns

 (t_r and $t_f = 10$ to 30 ns)


Figure 3. Read Timing Characteristics
READ CYCLE ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0$ to $70^\circ C$, unless otherwise noted)

Characteristic	Symbol	SY6551		SY6551A		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	μs
Pulse Width ($\phi 2$)	t_C	470	—	235	—	ns
Address Set-Up Time	t_{ACR}	180	—	90	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	ns
R/ \overline{W} Set-Up Time	t_{WCR}	180	—	90	—	ns
Read Access Time	t_{CDR}	—	395	—	200	ns
Read Hold Time	t_{HR}	10	—	10	—	ns

 (t_r and $t_f = 10$ to 30 ns)


Figure 4a. Transmit Timing with External Clock

Figure 4b. Interrupt and RTS Timing

Figure 4c. Receive External Clock Timing
TRANSMIT/RECEIVE CHARACTERISTICS

Characteristic	Symbol	SY6551		SY6551A		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	0.5*	—	0.5*	—	μs
Transmit/Receive Clock High Time	t_{CH}	235	—	235	—	ns
Transmit/Receive Clock Low Time	t_{CL}	235	—	235	—	ns
XTAL1 to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
\overline{RTS} Propagation Delay	t_{RTS}	—	500	—	500	ns
\overline{iRQ} Propagation Delay (Clear)	t_{iRQ}	—	500	—	500	ns

($t_r, t_f = 10$ to 30 nsec)

*The baud rate with external clocking is:
$$\text{Baud Rate} = \frac{1}{16 \times T_{CCY}}$$

INTERFACE SIGNAL DESCRIPTION
 \overline{RES} (Reset)

During system initialization a low on the \overline{RES} input will cause internal registers to be cleared.

 $\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system microprocessor and the SY6551.

 R/\overline{W} (Read/Write)

The R/\overline{W} is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/\overline{W} pin allows the processor to read the data supplied by the SY6551. A low on the R/\overline{W} pin allows a write to the SY6551.

 \overline{iRQ} (Interrupt Request)

The \overline{iRQ} pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common \overline{iRQ} microprocessor input. Normally a high level, \overline{iRQ} goes low when an interrupt occurs.

DB₀ - DB₇ (Data Bus)

The DB₀-DB₇ pins are the eight data lines used for transfer of data between the processor and the SY6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS₀, \overline{CS}_1 (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The SY6551 is selected when CS₀ is high and \overline{CS}_1 is low.

RS₀, RS₁ (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various SY6551 internal registers. The following table indicates the internal register select coding:

RS ₁	RS ₀	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the SY6551 registers. The Programmed Reset is slightly different from the Hardware Reset (\overline{RES}) and these differences are described in the individual register definitions.

ACIA/MODEM INTERFACE SIGNAL DESCRIPTION
XTAL1, XTAL2 (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float. XTAL1 is the input pin for the transmit clock.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

RTS (Request to Send)

The RTS output pin is used to control the modem from the processor. The state of the RTS pin is determined by the contents of the Command Register.

CTS (Clear to Send)

The CTS input pin is used to control the transmitter operation. The enable state is with CTS low. The transmitter is automatically disabled if CTS is high.

DTR (Data Terminal Ready)

This output pin is used to indicate the status of the SY6551 to the modem. A low on DTR indicates the SY6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

DSR (Data Set Ready)

The DSR input pin is used to indicate to the SY6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready".

DCD (Data Carrier Detect)

The DCD input pin is used to indicate to the SY6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

INTERNAL ORGANIZATION

The Transmitter/Receiver sections of the SY6551 are depicted by the block diagram in Figure 5.

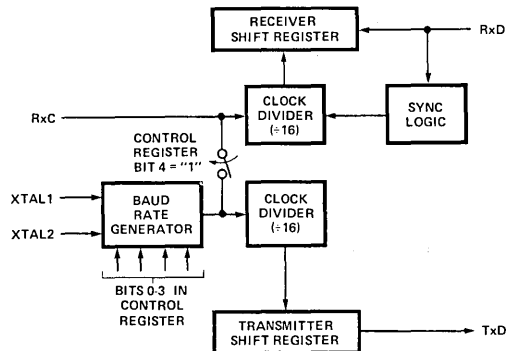
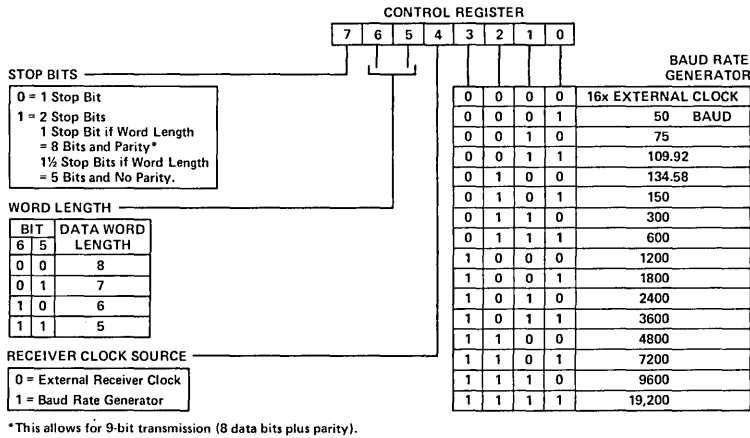


Figure 5. Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the SY6551.

CONTROL REGISTER

The Control Register is used to select the desired mode for the SY6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

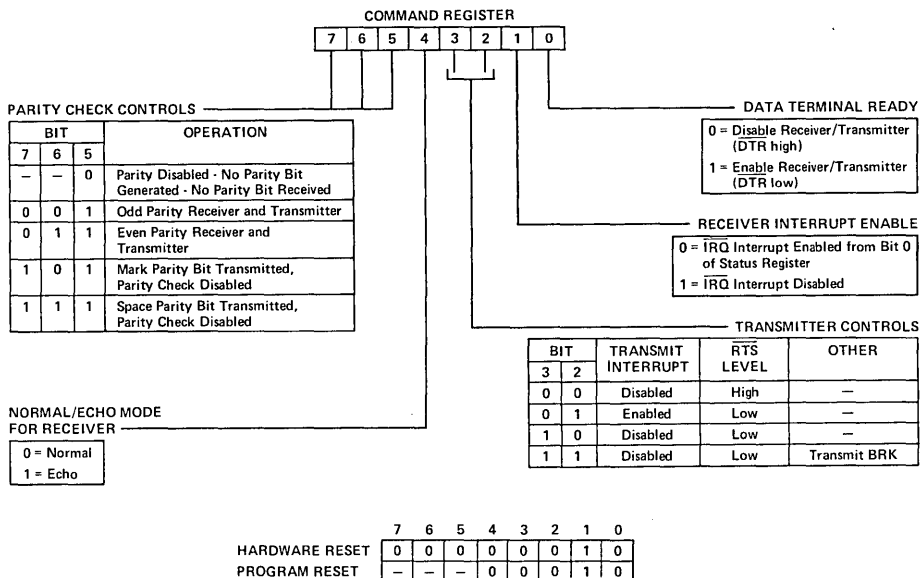


	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	-	-	-	-	-	-	-	-

Figure 6. Control Register Format

COMMAND REGISTER

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.



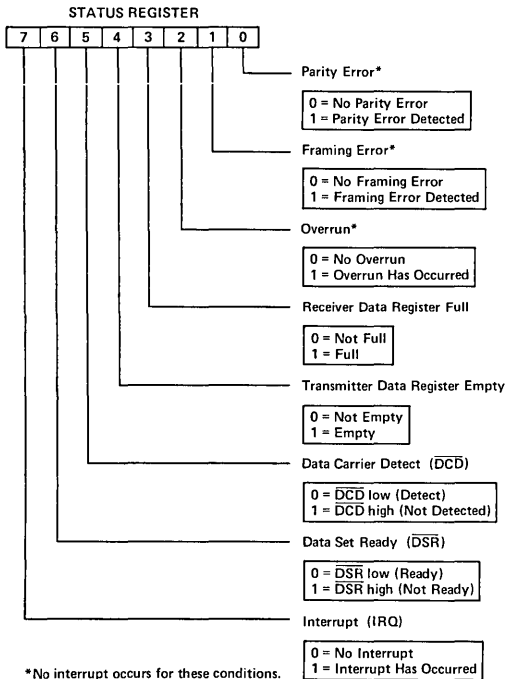
	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	1
PROGRAM RESET	-	-	-	0	0	0	1	0

Figure 7. Command Register Format

MICRO-PROCESSORS

STATUS REGISTER

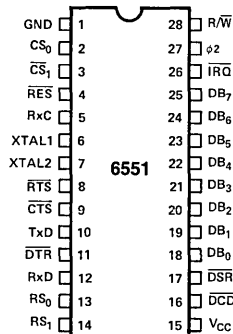
The Status Register is used to indicate to the processor the status of various SY6551 functions and is outlined in Figure 8.



HARDWARE RESET	7	6	5	4	3	2	1	0
PROGRAM RESET	0	-	-	1	0	0	0	0
	-	-	-	-	-	0	-	-

Figure 8. Status Register Format

PIN CONFIGURATION



TRANSMIT AND RECEIVE DATA REGISTERS

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

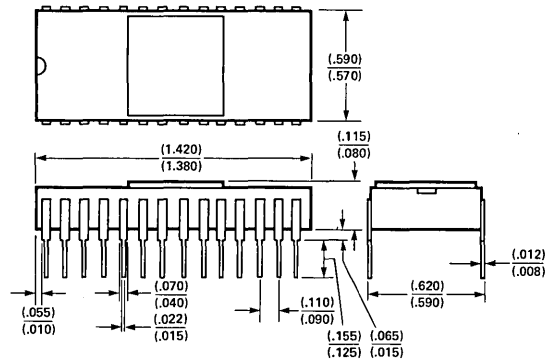
- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

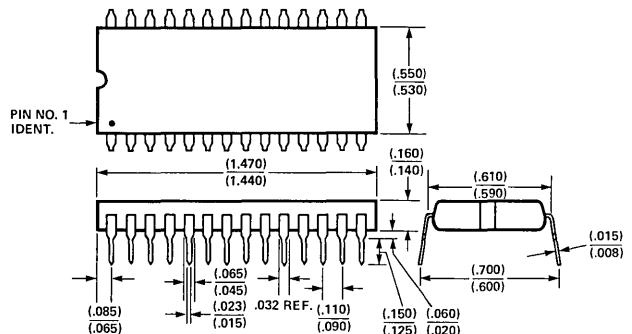
- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

PACKAGE OUTLINES

28 LEAD CERAMIC



28 LEAD PLASTIC





System 65 Microcomputer Development System

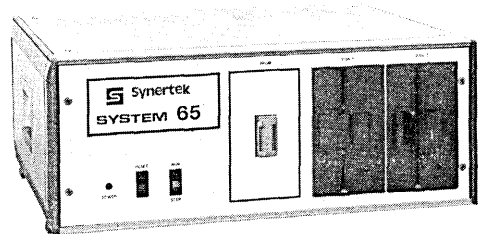
SYSTEM 65, the fully integrated microcomputer development system, built for expansion. **START WITH IT, GROW WITH IT, STAY WITH IT.**

SYSTEM 65

SYSTEM 65 is a new, easy to use, powerful, complete development system for the 6500 family of microcomputers. The basic configuration includes two **built-in mini-floppy disc drives**, 16K bytes of user memory and 16K bytes of resident operating system. Monitor commands are self-prompting whenever memory, peripheral, or disk file assignment is required. Text editor provides line, string, and character editing functions. A resident two-pass assembler and dynamic debug package complete the operating system. Both source and object code may be maintained in memory for fast editing, assembling, and checkout. Since the total monitor, editor debugger and assembler are resident in ROM, 100% of the disk storage and drive utilization is available to the user. The mini-floppy diskettes may be used as storage for source and object code and documentation. Each diskette has the capacity for 78K bytes of information in a maximum of 60 files.

SYSTEM 65 supports a variety of terminals with serial data from 110 baud to 9600 baud. Connectors are provided for both RS-232C and current loop interfacing. Reader ON/OFF signals and RTS/CTS control signals are standard. Included is a parallel port providing automatic control to high speed printers, such as Diablo, Centronics, and Tally.

FUTURE GROWTH is the key to the **SYSTEM 65** architecture and design philosophy. **SYNERTEK** realizes that requirements change and therefore we want the System to grow with you. That is why the System has been incorporated with extra card slots for systems expansion.



GROWTH IS IN THE CARDS. In coming months the following new optional printed circuit cards will become available: PROM Memory Module, PROM Programmer, ADD-ON Memory, System Evaluator Module and Card Extenders.

SYNERTEK is aware that major enhancements will be provided by the users themselves in the form of user-generated software. That's why **SYNERTEK** has provided the flexible and versatile tools necessary to promote efficiency and productivity. Our **DEBUG** Monitor provides eight (8) software breakpoints, one hardware breakpoint with Scope Sync, a single-step feature, and a versatile **TRACE** output with OP Code mnemonics and Symbolic names. Other **DEBUGGER** features include Execution Path History, Register and memory display, as well as memory write protect. The System 65 resident text editor will provide the users with facilitated control at their fingertips.

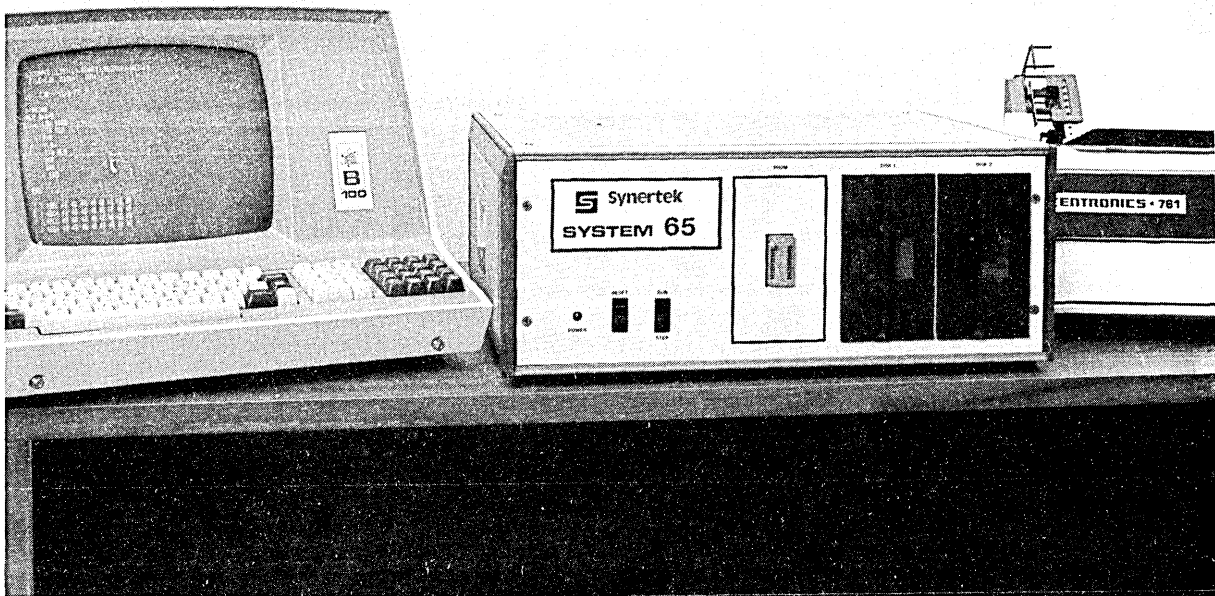
The resident two-pass Assembler provides the programmer with powerful software tools. The Assembler gives the user control of the output which may optionally be spooled to the diskettes or print out only error messages or list the entire program. Errors in listings are "chained" together and highlighted by arrows. The user may optionally relocate the code to another location. A powerful link capability is also provided which will allow multiple files on different media to be treated as a single assembler.

STANDARD PERIPHERAL INTERFACES

The System 65 offers the user the option to incorporate his own set of standard peripheral interfaces. The user then has the ability to place units of their own choosing and familiarity onto the system. The RS-232 port provides the capability for the placement of most Keyboard Printers or Display Terminals onto the System 65. If a high speed printer is required the parallel port connector located on the rear panel of the unit provides that interface flexibility.

EASE OF USE is a major feature of the System 65. The front panel controls are minimal consisting of a RESET Switch, RUN/SINGLE-STEP Switch and a "power on" indicator. System operation is straight forward with the majority of command functions being entered from the terminal. A PROM socket conveniently located on the front panel allows programming of 2708/2716 erasable PROMS.

MICRO-
PROCESSORS



System 65

Timekeeping Products

Timekeeping Products



Multi-Function, Six Digit LCD Watch Circuit With Alarm, Three Stopwatch Modes, and Event Counter

SY5009A

WATCH PRODUCTS

BASIC FUNCTIONS

- Six Digit LCD display (2 alphanumerics)
- Low power (one 1.5V battery operation)
- On chip voltage doubler and tripler
- Hours/minutes/seconds
- Month/date/day
- 100 year calendar
 - Automatic leap year update
- 12 and/or 24 hour operation
- Complete stopwatch functions
 - Time accumulation (start/stop, start/stop . . .)
 - Standard split
 - Taylor split
 - Seconds/100 or minutes/100 resolution
- Event counter
- Alarm
 - Hours/minutes - 24 hour alarm
 - 7 minutes snooze control
 - Momentary warning of pending alarm
 - Alarm output for either coil or ceramic resonator
- User adjustable frequency correction
- Single step and fast roll in set modes

The SY5009A is a six digit LCD drive chip containing the complete circuitry required for time display, chronograph/stop watch, event count and alarm functions. Additional functional flexibility is obtained by mask options allowing the customer to define a pro-

duct most suitable for his unique requirements. The circuit is fabricated with Synertek's high density Silicon Gate CMOS process resulting in a reliable and cost effective product.

ADDITIONAL FEATURES

The following items may be programmed by a mask option:

- Order and number of set modes
- Crystal frequency
- European date option
- Stopwatch resolution (sec/100 or min/100)
- User selectable or mask preset 12/24 hour operation
- Month/date/day or promotional display
- Alarm output polarity
- Alarm frequency: The SY5009A is now available in two versions: The SY5009A-02 with a 2.048 Khz frequency alarm output for a piezo-electric alarm, and the SY5009A-04 with a 4.096 Khz frequency alarm output for a speaker alarm or a piezo-electric alarm.
- Positive or negative case
- Additional segment identifiers
 - Stopwatch mode indicator
 - Alarm indicator
 - Month/date/day or promotional indicator
- Leading zero suppression on hours, month and date display
- No rollover in set mode
- Debounce protection on all button inputs

Five basic watches may be obtained by using only certain combinations of the four buttons available as follows:

FEATURES

Time + Date
 Time + Date + Stopwatch (no split)
 Time + Date + Alarm
 Time + Date + Stopwatch (with split)
 Time + Date + Alarm + Stopwatch (with split)

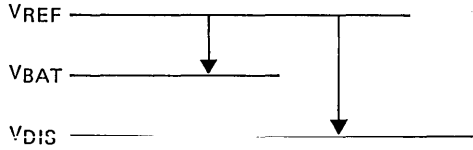
BUTTONS REQUIRED

Time (T), Set (S)
 Time (T), Set (S), Start/Stop (S/S)
 Time (T), Set (S), Split (C)
 Time (T), Set (S), Split (C), Start/Stop (S/S)
 Time (T), Set (S), Split (C), Start/Stop (S/S)

TIMEKEEPING PRODUCTS

ELECTRICAL AND OPERATING CHARACTERISTICS

SUPPLY VOLTAGE DEFINITION



VREF: Reference Voltage - positive battery terminal
 VBAT: Negative battery terminal
 VDIS: Negative display operating voltage

ABSOLUTE MAXIMUM RATINGS*

Input and Output Voltages +3 to -5V
 Supply Voltages +3 to -5V
 Storage Temperature -55°C to 100°C

* Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions not specified in section 3.0 is not implied. Extended periods of exposure to absolute maximum ratings may affect device reliability.

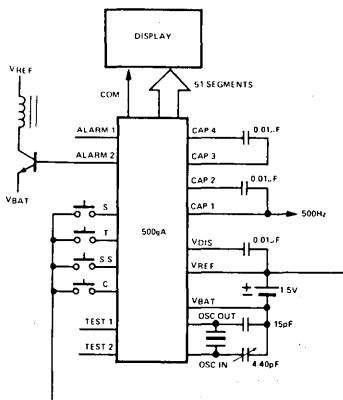
TA = 25°C, VBAT = VREF - 1.5V, VDIS = VREF - 3.0V unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
VBAT	Battery operating voltage	-1.35	-1.5	-1.6	V	
IBAT	Supply current		-3.0	-5.0	μA	Oscillator running at 32768 Hz. All inputs and outputs floating.
VDIS	Display operating voltage	-2.2	-3.0	-5.0	V	
IDIS	On chip display current		-1.0		μA	VDIS = -4.5V
IL, OL	Inputs/outputs leakage			1.0	μA	
IC	Input pull-up current		1.0		μA	Inputs activated
VD	Doubler voltage		-3.0		V	
VT	Tripler voltage		-4.5		V	
VA	Alarm output voltage		1.0		V	
IA	Alarm output current		1.0		mA	VA = 1.0V

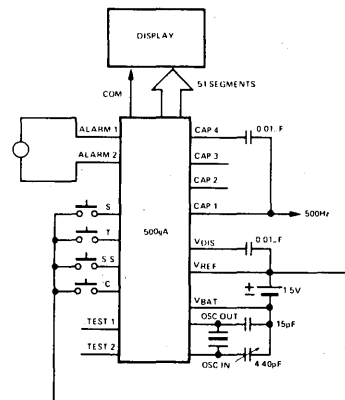
TIMEKEEPING PRODUCTS

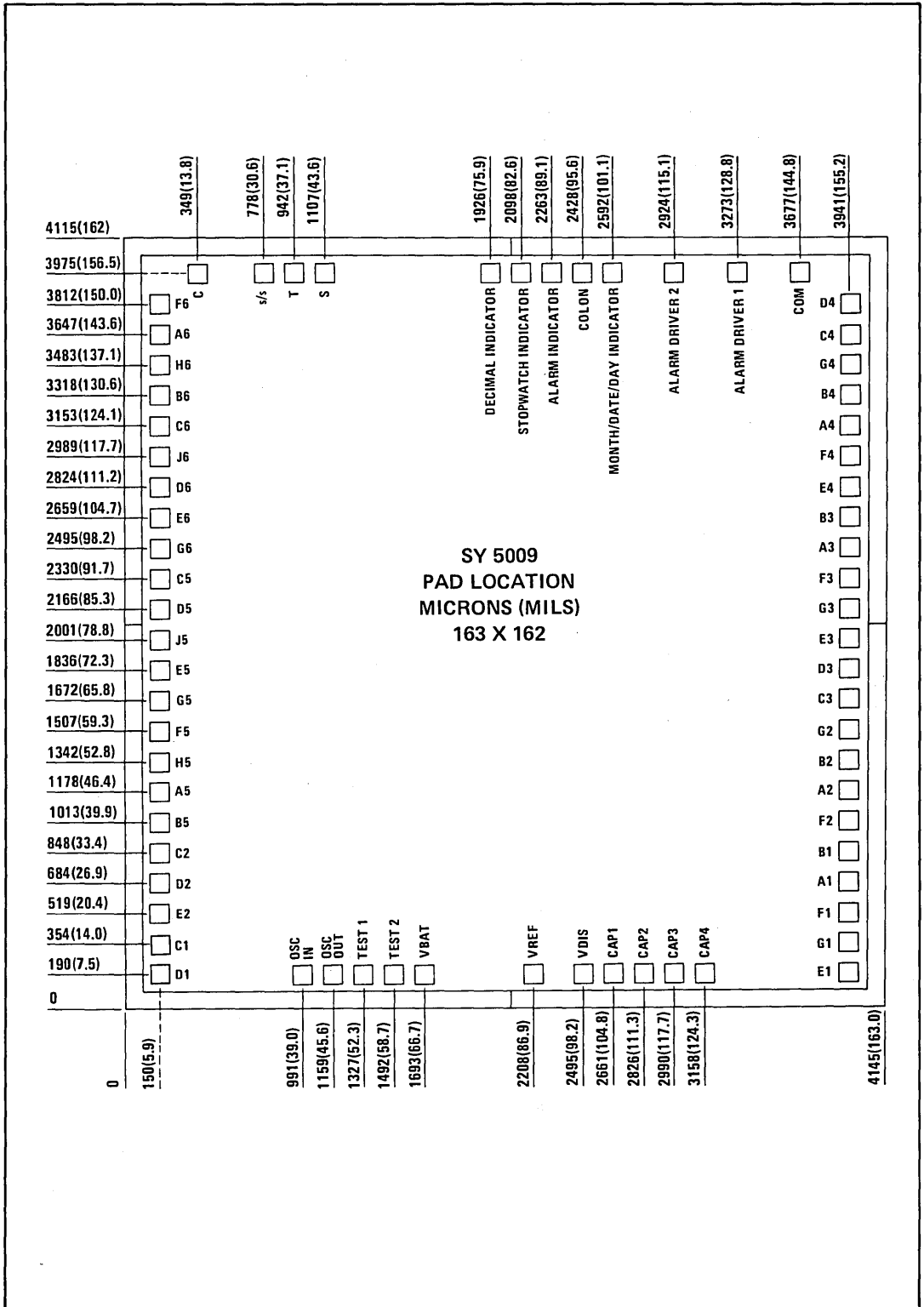
SYSTEM CONNECTIONS

VOLTAGE TRIPLER AND COIL ALARM



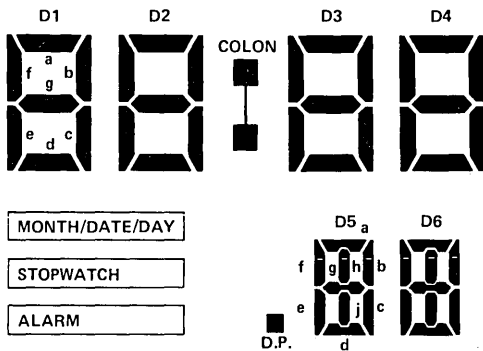
VOLTAGE DOUBLER AND CERAMIC RESONATOR ALARM





TIMEKEEPING
PRODUCTS

DISPLAY DEFINITION



FUNCTIONAL DESCRIPTION

Basic Time Functions

- (1) Continuous display of hours, minutes, seconds, and colon. Alarm indicator will be shown only when buzzer is armed (see: Alarm Functions).
- ↓ T
- (2) For as long as T is held, continuous display of month, date, weekday and month/date/weekday identifier. Alarm identifier will be shown only when alarm is armed. As soon as T is released, the display will revert to (1).

Alarm Functions:

- (3) Continuous time display
Push T button twice and hold
Continuous display of alarm set time in hours and minutes, AM/PM or HR indicator (on digits 5 and 6), and colon. Alarm indicator is flashing regardless of whether or not the buzzer is armed.
As soon as T is released, the display will revert to (3).
- ↓ T-T
- (4) As soon as T is released, the display will revert to (3).

Arming and Disarming the Buzzer

- (5) During the display mode, if the alarm indicator is on the alarm mechanism (coil or piezoelectric disk) is armed and alarm will sound when preset time is reached.
↓ C
Push C button once

- (6) Alarm indicator is turned off and buzzer is disarmed. Alarm will not go off at the preset time.
↓ C
Push C button once
- (7) Alarm indicator is on again. Buzzer is armed and alarm will sound at preset time. Continuous pushes of button "C" will toggle the watch between states (6) and (7).

At the preset time, and with buzzer armed, the alarm will sound in the following manner:

- 1 second beep - a warning that alarm is about to go off
 - 7 seconds silence - allowing the user to turn off the alarm before it goes off
 - If alarm was not turned off during the 7 seconds interval
 - 1 second on
 - 1 second off
 - 1 second on
 - 1 second off
 - 1 second on
 - 1 second off
 - 1 second on
 - 1 second off
 - 1 second on
- } 60 seconds
- } For a total of 52 seconds

At any time after the first beep is heard, the user has three courses of action:

1. Push button T once This will activate snooze control. The alarm sound will stop and the alarm sequence will repeat 7 minutes later. This snooze sequence can be repeated every 7 minutes for as many times as desired.
2. Push button C once Alarm sequence is terminated and the buzzer is disarmed.

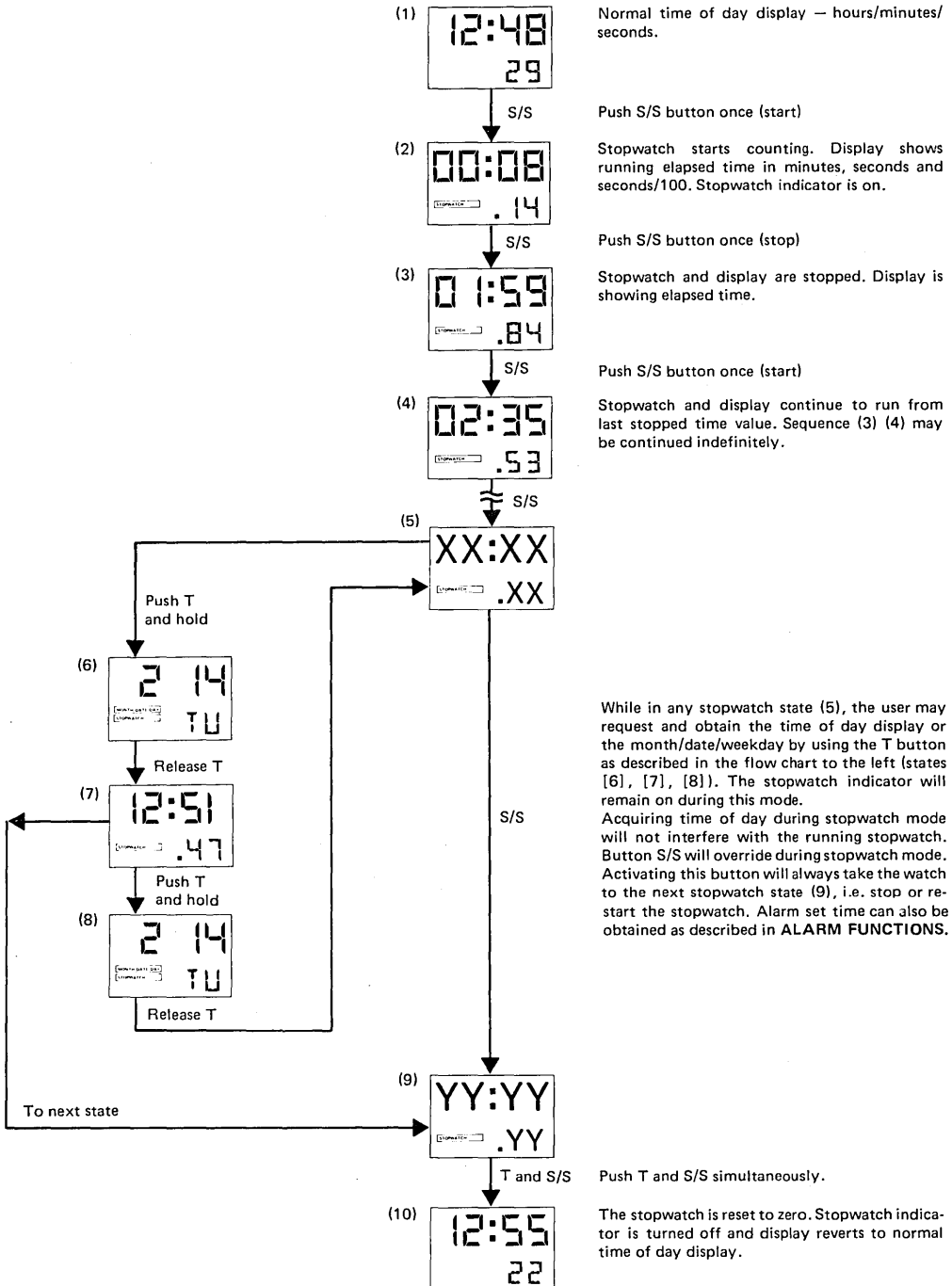
then
Push button C again Buzzer rearmed. Alarm will resound 24 hours later.
3. No action The alarm mechanism will complete the 60 seconds sequence and will then turn itself off. Next alarm sequence will sound 24 hours later, or at a newly preset alarm time.

TIMEKEEPING PRODUCTS

STOPWATCH FUNCTIONS


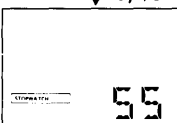
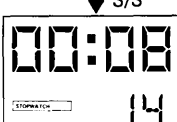
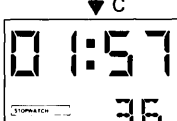
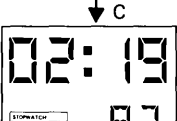
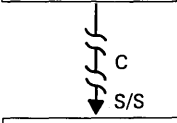
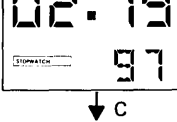
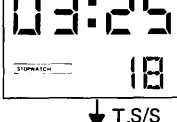
Basic Stopwatch Mode

Basic stopwatch (no split) capability is achieved through addition of the start/stop (S/S) button.



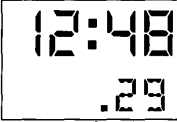
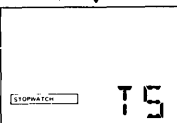
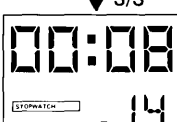
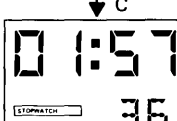
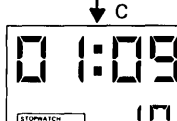
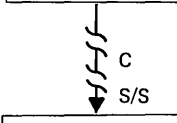
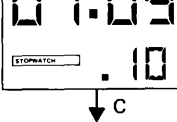
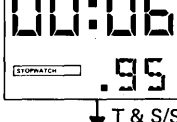
TIMEKEEPING PRODUCTS

STOPWATCH — STANDARD SPLIT MODE

- (1)  Normal time of day display hours/minutes/seconds. Hold button "C" down and push button S/S once.
- ↓ C,S/S
- (2)  The stopwatch is now in the standard split mode. No counting started. Stopwatch indicator is on and digits 5 and 6 show the display indicating standard split.
- ↓ S/S
- (3)  Push S/S button once (start). The stopwatch starts counting. Display shows running time in minutes, seconds and seconds /100.
- ↓ C
- (4)  Push "C" button once (capture). The display will stop at the captured time while the stopwatch keeps running.
- ↓ C
- (5)  Push "C" button once (capture). A new captured time value will be displayed. The stopwatch keeps running uninterrupted.
- ↕ C
- ↕ S/S
- (6)  Any time "C" is pushed, a new captured time will be displayed. This can be repeated indefinitely. Push S/S once. Stopwatch stops running. Display still retains the previous captured time (5).
- ↓ C
- (7)  Push C button once (recall). The display will show the stopped time. Thus, the user may record two events which are very close together by sequences 6 and 7.
- ↓ T,S/S
-  Push T and S/S button simultaneously. Stopwatch is reset to zero. The display reverts to the normal time of day display.

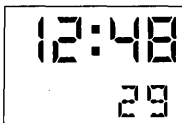
While in this stopwatch mode (anywhere in states 2 through 7), the time of day can be displayed using the T button in the manner shown in the flow chart of the basic stopwatch, states 5,6, and 7. This acquisition of time will not interfere with the stopwatch operation, but will erase the last captured time.

STOPWATCH — TAYLOR SPLIT MODE

-  Normal time of day display — hours/minutes/seconds. Hold down button "C" and push button S/S twice.
- C & S/S ↓ -S/S
-  The display will indicate (TS on digits 5 and 6) that the watch is in Taylor Split Mode. Stopwatch indicator is on.
- ↓ S/S
-  Push button S/S once (start). The stopwatch starts counting. The display is showing the running time in minutes, seconds, and seconds/100.
- ↓ C
-  Push button "C" once (capture). The display will show captured time. The stopwatch is reset to zero and counting from zero again.
- ↓ C
-  Push button "C" once (capture). Again captured time is displayed indicating the time difference between this capture and the previous capture. The stopwatch again is reset to zero and counting up.
- ↕ C
- ↕ S/S
-  Any time "C" is pushed, a new capture time will be displayed showing the difference between the latest capture and the one preceding it. Push S/S once (stop). Stopwatch stops running. The display still shows last captured time.
- ↓ C
-  Push C once. The display will show the difference between the stopped time and last captured time.
- ↓ T & S/S
-  Push T and S/S simultaneously (reset). Stopwatch is reset to zero. The display reverts to the normal time of day.

As in the other stopwatch modes, the time of day display and month/date/weekday display can be obtained by using button T without interfering with the stopwatch operation. (see description: states 6,7, and 8 - basic stopwatch model). Although the last captured time will be erased.

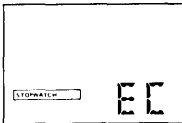
EVENT COUNT MODE



Normal time of day display—hours/minutes/seconds.

Hold down button "C" and push button S/S three times.

C & S/S ↓, S/S, S/S



The display will indicate EC on digits 5 and 6 for "Event Count". Stopwatch indicator will be on.

↓ S/S

Push button S/S once.



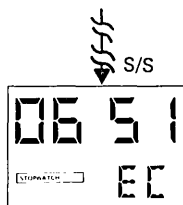
The display will indicate "1" count.

Push button S/S once.

↓ S/S



The display will indicate the count of 2.



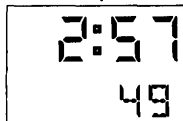
↓ S/S

Push S/S any number of times.

Each subsequent push of S/S will increase the count by one to a maximum of 5999.

↓ T & S/S

Push buttons T and S/S simultaneously.



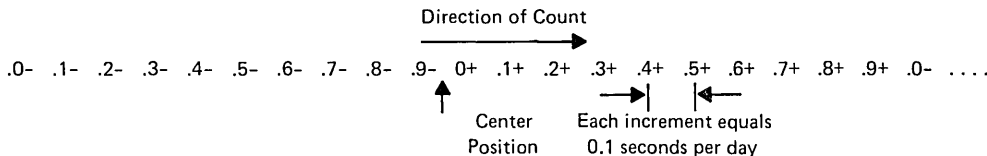
The event counter is reset to zero and the display will revert to the normal time of day.

As in the previous stopwatch modes, here too, the time of day display may be obtained using button T in the manner described in states 6, 7, and 8 of the basic stopwatch mode. Doing so will not interfere with the event counter.

FREQUENCY CORRECTION

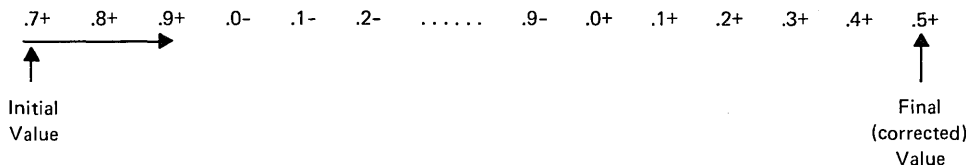
During the Frequency correction set mode, the user may choose to speed up or slow down the watch to compensate for an inaccurate time keeping. The correction range is plus or minus 1 second per day and it is achieved as follows:

Each digit increment in this set mode will speed up the watch by 0.1 seconds per day. Each digit decrement will slow down the watch by the same amount.



Example

The user finds out that his watch is fast by 1 second in 5 days (or 0.2 seconds per day). When getting into the set mode the display indicates .7+; to slow down the watch by 0.2 seconds he must subtract two (2) increments from the display shown or change the setting to .5+. The user holds down button T for the following count and releases T when desired display is reached.



TIMEKEEPING PRODUCTS

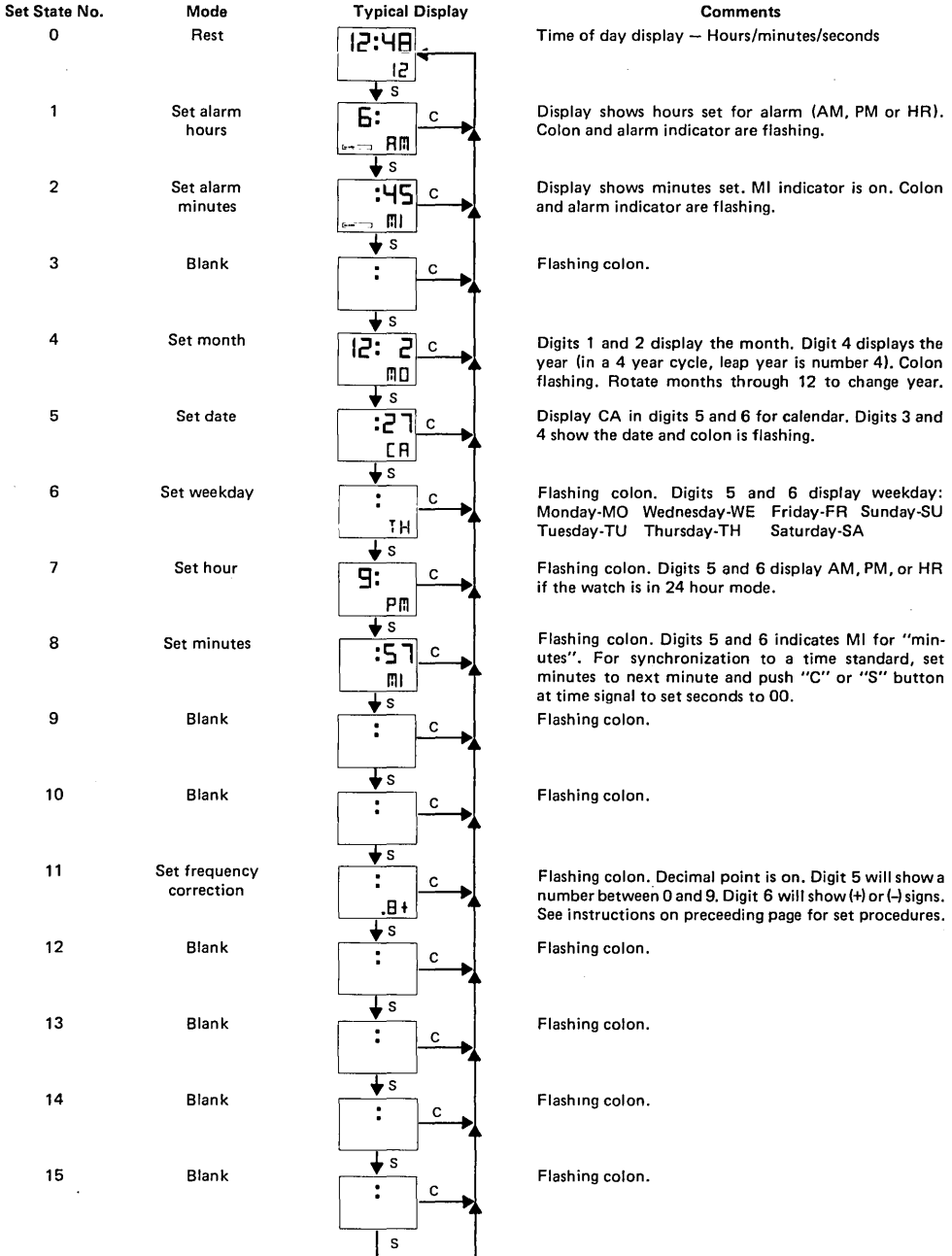


SET MODES

General

Entering the set mode is achieved by using the set (S) button (normally recessed).

The SY5009 has 16 set states (not all being used). Since the order of the set states is programmable, the customer may place blank states anywhere in the sequence as well as determine the last set state at which the watch will return to the rest mode, i.e. time of day display. Modification of the set information is done by button T in either single step or fast roll manner (2HZ rate when T is held down). At any time during the set mode, a push on the "C" button will return the watch to the rest mode (time of day display) even if the set sequence was not completed. A typical set sequence is shown in the flow chart below:



TIMEKEEPING PRODUCTS

Custom Capabilities

Custom Capabilities



Custom MOS/LSI

Since the inception of the company, Synertek has played a very active role in the CUSTOM MOS marketplace. We have found that by maintaining a leadership position in high-technology standard products, we are able to offer our custom product customers the most competitive design/process solutions available in the industry. Our standard products employ the latest in design and process techniques in the P-Channel, N-Channel and CMOS silicon gate technologies including the use of ion implanted, depletion-mode devices and on-chip substrate bias generators. These same techniques allow the design of the most competitive custom circuits which in turn gives the desired overall result for our customer..... an advantage in his marketplace.

The use of custom MOS and CMOS circuits has been so pervasive that it is impossible to discuss the full range of potential applications. A sampling of Synertek's experience illustrates the extremes:

- Two different 16-bit microprocessors: one program's purpose was to reduce the cost of a top line Minicomputer, and the other for use in a Distributed Process Control System.
- A printer and keyboard controller in a microprocessor-based Word Processing System.
- All the digital logic for an electric utility two-way Load Management System.
- The CMOS logic for a Pocket Paging System.
- The analog and digital circuitry for a Tire Pressure Sensing System.
- The digital circuitry for a Bell-system approved Touch-Tone Receiver and Repertory Dialer.

This list could go on but the point is that CUSTOM MOS is being used in almost every sector of the electronics market and the applications are steadily advancing into the electromechanical and mechanical strongholds as well. If the production volume is sufficient, the lower cost and higher reliability of a custom MOS solution cannot be ignored.

There are several possible levels of interface between Synertek and our Customers in the design of a custom product. Some companies prefer that Synertek design the entire electronic subsystem so that they are free to concentrate on system design. Other companies

have in-house MOS design groups and they prefer to provide us with working plates and test tapes. We prefer to work closely with each customer to evolve the best interface for a specific program at a specific point in time. The best interface point depends on many factors including (a) technical difficulty and performance requirements of the chip, (b) anticipated production volume, (c) availability of customer's design engineers when the program must begin, and so on. Synertek has the ability to work at any of the interface levels and indeed that is the first topic of discussion on any program. The flow chart on the next page shows the activities that must be executed promptly and accurately for a successful program. The amount of time required for each task depends on the complexity of the circuit; a realistic range is shown next to each activity. Before a program is begun, however, our customer knows the exact schedule for his particular circuit.

A. CONCEPT REVIEW

The initial step in the development of a custom circuit is a concept review meeting which consists of detailed discussions reviewing system requirements. The purpose of this meeting is to assure that Synertek's MOS-LSI Design Engineers fully understand all pertinent system requirements such as:

- Functional Operation.
- Subsystem, or chip, interface requirements, especially those that may determine which process (P, N, or CMOS), must be used.
- Environmental or packaging requirements.

B. SYSTEM DEFINITION

The block diagrams/flow charts and electrical specifications are established in this phase. These are a result of contributions by both Synertek and the customer.

C. LOGIC DESIGN

Conversion of the system functions to MOS logic implementation is done entirely by Synertek Design Engineers. This logic is optimized for the particular process and application involved and will differ substantially from any prior (e.g. TTL) implementation.

D. CIRCUIT DESIGN

During this phase the individual transistors are designed to implement the logic, to have the proper I/O characteristics, and to execute the intended function at the proper speed. Particular attention is paid to critical speed paths in this phase as well as in composite design.

E. COMPOSITE DESIGN

This is the most time-consuming phase since the overall chip size directly affects the cost of the final device. The composite is designed, usually at 1000X, "by hand" as opposed to using a computer aided placement and wiring program. Creative layout designers are still far superior to computers and the smaller chips result in very real production savings. Composite design and circuit design overlap somewhat, especially in the area of critical speed paths.

F. MASK FABRICATION

This phase actually consists of three separate critical activities.

Digitizing - As sections of the circuit become complete they are digitized on Synertek's Calma system. The digitized information is then used to generate check plots which then are compared to the original section of the composite to assure no errors. This is an iterative procedure which usually requires several interactions before the data base tape is approved for the entire composite.

Pattern Generation - All Synertek circuits are, and always have been, produced without the use of rubilith (rubies). We go directly from digitizing to reticle generation, or pattern generation. The reticle is usually manufactured at 10X. Photographic "blowbacks" are then compared, once again, to the original composite as one last check to assure that the tooling is correct.

Working Plate Manufacture - The approved reticle is then used to step-and-repeat a master plate which is ultimately used for generation of the working plates.

G. WAFER FABRICATION

Fabrication of wafers will be performed in one of Synertek's modern manufacturing areas. Exactly which area will be used for a particular device is determined mainly by the process technology involved. During the fabrication phase, numerous

quality and electrical inspections are performed on each wafer to assure that each wafer run is within the allowable bounds of Synertek's manufacturing process.

H. TEST AND ASSEMBLY

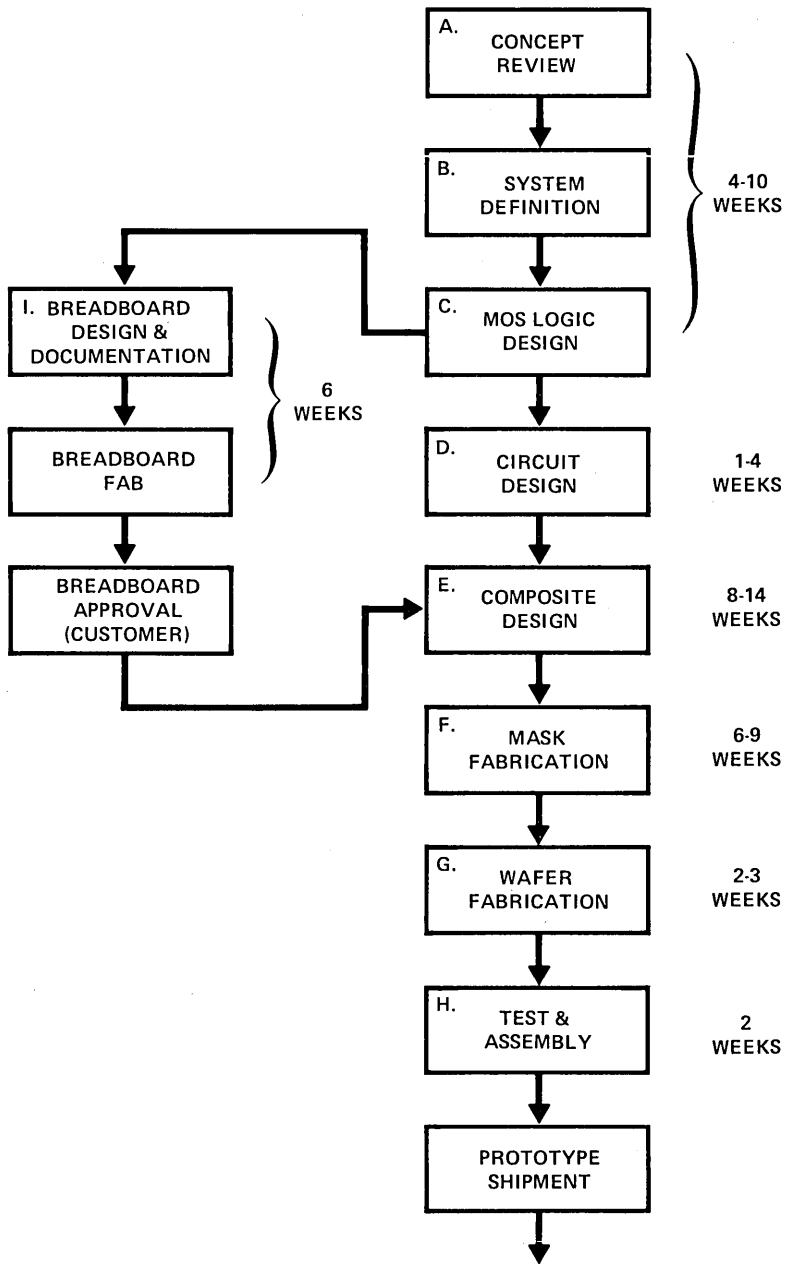
Following the fabrication of devices, wafers are then tested using computer controlled state-of-the-art LSI testers. Each of these machines contains its own mini-computer and, after being properly programmed, is capable of doing both functional and parametric tests. Initial prototype devices will then be assembled in Santa Clara and subjected to a complete final test prior to shipment.

I. BREADBOARD

Since many of our custom circuits contain on the order of 4,000 gates, a great deal of attention is required to assure that these chips work right the first time out. The checking required in composite design and mask fabrication was touched on above. We have found, however, that computer-aided programs for checking logic and circuit design are not adequate in verifying proper operation of the entire chip.

In parallel with the logic and circuit design, Synertek constructs a breadboard which is essentially a transistor-for-transistor duplicate of the circuit being designed. The breadboard is checked out by Synertek and then given to the customer for approval. The breadboard can be wired into the customer's system, for example, and the whole system can be checked out for proper performance. Perhaps features are added or deleted at this point, since the customer's engineering and marketing people get their first "hands on" exposure to this new product. After approval, the breadboard is then used by Synertek's Test Program Development group to generate and debug the test program prior to the time wafers are available.

To determine if your application is technically and/or economically a realistic candidate for Custom MOS implementation, Synertek can perform a preliminary analysis in approximately one week. Such items as functional specifications, logic diagrams if the equipment is already in production using standard components, and/or block diagrams improve the accuracy of the preliminary analysis. If the analysis is promising, Synertek will then issue a firm quotation.

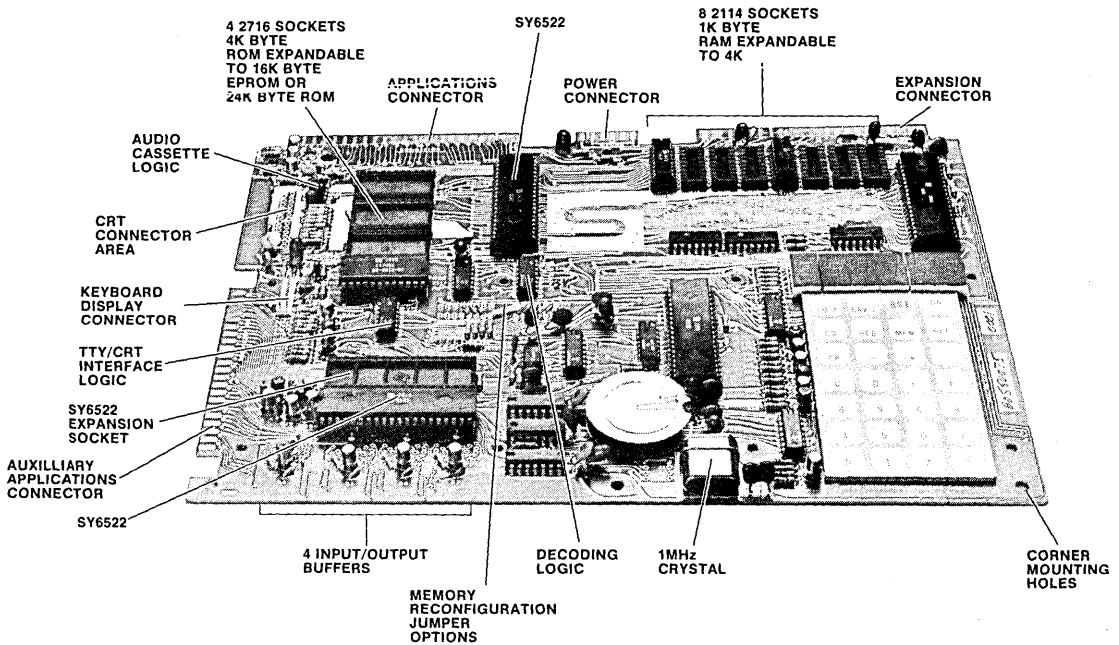


CUSTOM

Systems

Systems

SYM-1 Microcomputer Development Board



Microprocessor Applications

- Experimentation/Training/Engineering/Prototyping/ Instrumentation/Testing

SYM-1 Features Include:

- Ready to use because it's fully assembled, tested and completely integrated as soon as you open the shipping container.
- 51 total I/O lines, expandable to 71.
- The powerful SY6502 8-bit microprocessor with advanced architectural features which make it one of the largest selling "micros" on the market today.
- Five on-board programmable interval timers available to the user for timing loops, watchdog functions, and real-time communications protocols.
- 4K-byte ROM SUPER-MON resident monitor and user expandable.
- Single 5-volt power capability is all that is required.
- 1K-bytes of static RAM on-board with sockets provided for immediate expansion to 4K bytes on-board, with total memory addressability to 65,536 bytes.
- User PROM/ROM — the system is equipped with 4 PROM/ROM expansion sockets for SY2316/SY2332 ROMs or 2716/2732 EPROMs, up to 28K bytes.
- Standard interfaces: digital audio cassette recorder interface with remote control; full duplex 20mA teletype interface; system expansion bus interface; TV/KB controller board interface; RS232 compatible interface; four strappable relay drivers or input buffers; and a 32-character single line oscilloscope display interface.
- Application port — 15 bidirectional TTL lines for user applications with expansion capability for added lines.
- Expansion port for add-on modules (51 I/O lines in basic system)
- Separate power supply connector for easy disconnect of the DC power.
- Uses same hardware interface busses as KIM-1 (MOS Technology)

Expansion Features Include:

- TV/CRT Keyboard Terminal Module KTM-2
- Resident 8K BASIC Interpreter BAS-1
- Port expansion kit PEX-1
- RAM expansion kit SRM-1, SRM-3

On-Board Expansion

The printed circuit board includes in its layout the capability to add additional ROM, PROM, RAM or peripheral ports when you require them. SYM-1 doesn't require you to build up wire-wrap boards to use these options. SYM-1 options are merely plugged into the basic unit to give you the added capability you require. The system is neatly configured and you won't have to have a "rat's nest of wires" hanging off the basic board. We've also maintained KIM hardware compatibility. Our SYM-1 plugs into any KIM motherboard and card cage.

Super Software

Our standard SYM-1 system can be programmed either in machine language for those users wishing to gain an in-depth understanding of microprocessor operations, or it can be loaded with object code developed on a cross-assembler resident in another system. Those users wishing to use a higher level language can purchase our BAS-1 BASIC, a nominally priced option. Machine status is easily accessible, and our SUPER-MON monitor gives the user the same full functional capability of the TTY. Other software enhancements include:

- Write protect of selectable memory areas.
- Byte search capability
- Break function to halt program
- Enhanced Programmable DEBUG Control
- Block Move and Memory Fill functions
- User definable vector branches, and more

Versatility Unlimited

Future growth and expansion is a key requirement in any system. Both are designed into SYM-1. Unlike any other system which you "discard" once you've mastered it, SYM-1 grows with your needs.

You can store your programs in the 1K Static RAM and debug by simply using the single-step feature of the monitor. User static RAM is easily expandable to 4K bytes on board the basic unit. The 51 I/O lines which are available to control your custom applications can be expanded via an additional socket provided for Synertek's Versatile Interface Adapter — SY6522 to a total of 71 I/O lines. Our TV/KB interface board includes an ASCII keyboard which enables any home TV (connected through a standard RF adapter) or CRT monitor to be turned into a versatile video terminal.

Applications Unlimited

A Stand-Alone Microcomputer. With the addition of a user-provided 5-volt power supply, the SYM-1 becomes a functional stand-alone microcomputer development system. In this configuration, the user can select any memory addresses; read/modify data; and execute or single-step programs.

Audio Tape Cassette. By providing the power supply required together with any audio cassette, the user will have enhanced his system to include low-cost file capability and external memory store. The SYM-1 user can create files and block data into records on tape from SYM-1 memory (with error detection) choosing either the (KIM compatible) 8 characters/sec or SYM-1's 185 characters/sec mode.

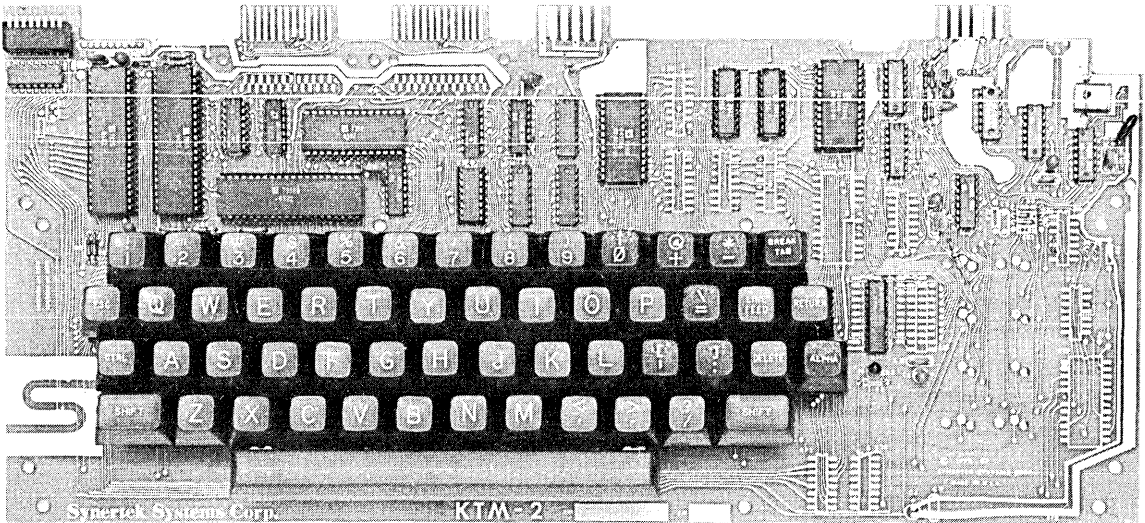
Teletypewriter Interface. The standard 20mA teletypewriter interface which is on-board SYM-1 allows for the easy installation of a Model 33 Teletype, or RS232 Terminal. Once interfaced, the user can list programs and maintain permanent data records. The use of the full Alpha-Numeric keyboard expands the character set available to the user. The paper tape reader/punch options allow the user alternative methods for storing programs and data. The SYM-1 automatically adjusts for a variety of baud rates.

TV/CRT Interface. With the addition of our KTM-2 option board and a standard RF adapter, the SYM-1 becomes a complete computer system with your TV or CRT monitor. The full Alpha-Numeric keyboard on the KTM-2 interface card has the same capability found in larger and more expensive computer systems.

Reliability Unlimited

SYM-1 incorporates the tried and tested SY6502 8-bit microprocessor. This "micro" — with its powerful architecture — has been incorporated into a multitude of system designs. It has been used extensively in TV games where reliability is a must. The powerful COMBO's and VIA's (SY6532 and SY6522), RAM (SY2114) and ROM (SY2332) also have been extensively used and proven in the field.

KTM-2 KEYBOARD TERMINAL MODULE



Description

The KTM-2 provides keyboard/display capability to support any mini or microcomputer terminal requirement. The keyboard is full ASCII with cursor control functions keys. The display interface provides composite video for an external user provided monitor or RF modulator for standard T.V.'s. The screen format is 24 lines x 40 characters.

The KTM-2 hardware is designed to provide flexibility over screen and character size as well as user functions. The design is economical using several Synertek components with custom programming only, i.e. without hardware modifications.

Features

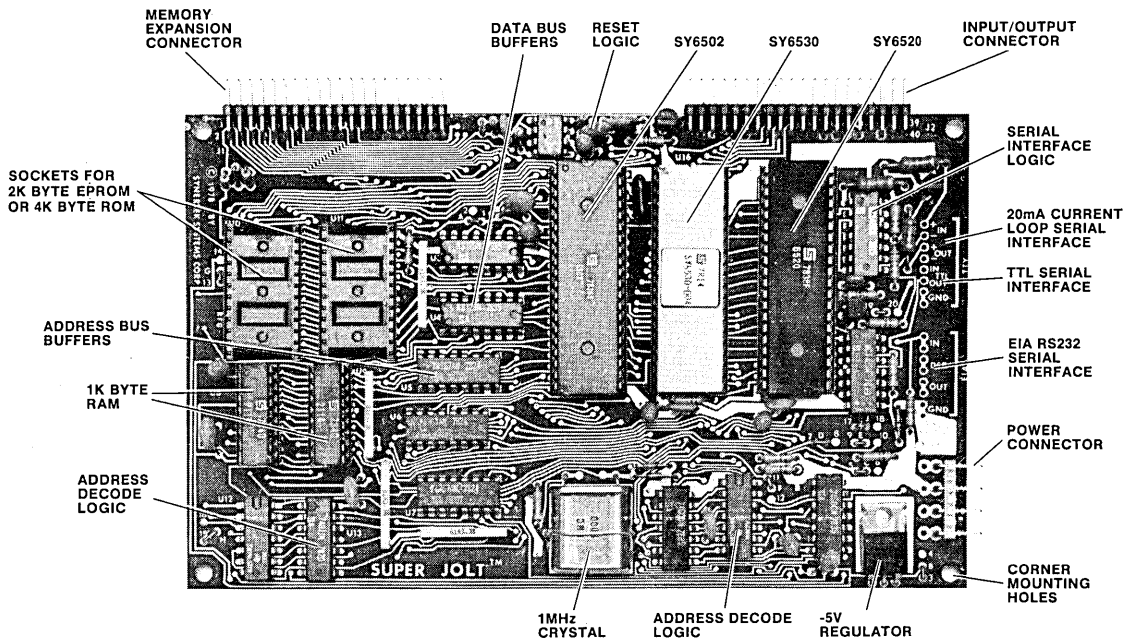
- Screen Size: 24 lines x 40 characters
- Alpha Character Set — Upper and Lower
- Numeric Character Set
- Graphic Characters, 128 Characters (256 with reverse video)
- Control/Special Characters
- 6x7 dot matrix character size; 8x8 matrix field size
- Full Cursor Control
- Addressable Cursor and Data (absolute and relative)

- Operating Mode
 - Conversational (character operations)
- Transmission Mode—Half/Full Duplex
- Scrolling (top-to-bottom then scroll up)
- Keyboard
 - Standard TTY layout
 - Typamatic (auto repeat after 1 second)
 - Tab control
- Communication-programmable baud rates 75-9600
- Editing
 - Erase screen/line
- Auxiliary I/O Port (RS232)
- Interlaced screen (switch selectable)
- European version available

User Interface

The KTM-2 operates as a standard terminal with full ASCII keyboard and cursor/edit control pad. Characters are transmitted as they are typed. The character set available consists of 96 alphanumeric characters, 32 control characters, and 128 graphics characters. Any combination of characters may occupy the screen simultaneously.

CP110 Super Jolt Single Board Computer



General

The CP110 SUPER JOLT CPU board is the most versatile microcomputer on a single PC board. Connected to a terminal, the CPU card provides everything necessary to begin writing, debugging, assembling and executing microcomputer programs. Stand-alone, the CP110 is a single board OEM microcomputer suited to a wide range of dedicated applications.

Measuring a mere 4-1/4" x 7", SUPER JOLT is the most compact single board computer available. Consider these features:

- A Synertek SY6502 NMOS 8-bit microprocessor
- 1,024 bytes of static program RAM memory
- 64 bytes of interrupt vector RAM
- 28 bidirectional and programmable I/O lines
- A 1 MHz crystal controlled clock
- An interval timer
- Four interrupts, including a timer interrupt and a non-maskable interrupt
- Three serial interfaces — 20mA current loop, RS232 and TTL

- Buffered address and data lines
- 1,024 bytes of resident ROM program memory containing DEMON, a powerful Debug Monitor program
- Optional 4,096 bytes of resident ROM program memory that includes a complete single pass Resident Assembler Program and a resident TINY BASIC interpretive language designed especially for SUPER JOLT systems. Our incredible SUPER JOLT, with its Resident Assembler Program (RAP) ROM, functions as a single board development system permitting assemblies to be made with only a single pass of a source program from a terminal or via a TTY paper tape reader. Following assembly, the programs can be debugged using the debugging facilities of the DEMON Debug Monitor program.

For those preferring a higher level language, TINY BASIC (a subset of Dartmouth BASIC) is available in ROMs to plug on-board (SW101) and permits immediate entry and execution of TINY BASIC

SYSTEMS

language programs. The ROM software has been designed so that most any I/O device can be used. By removing the RAP and TINY BASIC ROM, the CP110 SUPER JOLT board becomes a compact general purpose microcomputer suitable for any dedicated application. The vacated ROM sockets may be used for the user's programmed ROMs or for the user's programmed 2708 type PROMs.

CPU

The heart of the CP110 SUPER JOLT is an SY6502 CPU chip, a parallel 8-bit NMOS microprocessor with 16 address lines. The 8-bit data bus (D0-D7) is bidirectional and will drive one TTL (1.6mA, 130pf) load directly. The 64K byte address space is used to address program memory and to select I/O devices for communications with the CPU. Each address line will also drive one TTL load directly. The chip's internal oscillator is stabilized using an on-board 1 MHz crystal.

There are 1,024 bytes of program RAM provided on the CPU board. The program RAM is hard-wire addressed as the first 1,024 bytes of the CPU's 64K of memory address space.

Programmable I/O

The programmable I/O lines available from the CPU board are provided by an SY6520 Peripheral Interface Adapter (PIA) and an SY6530 I/O chip.

The PIA has two 8-bit ports with two interrupt-causing control lines each. Two jumpers are provided on the board which connect one or both PIA interrupt outputs to the CPU IRQ interrupt line. A Data Direction Register for each port determines whether each I/O line is an input or an output.

The SY6530 ROM chip provides 10 additional I/O lines that may also be specified as input or output lines under program control. These I/O lines may be used in conjunction with DEMON for interfacing a high speed paper tape reader to the CPU board.

Interfacing

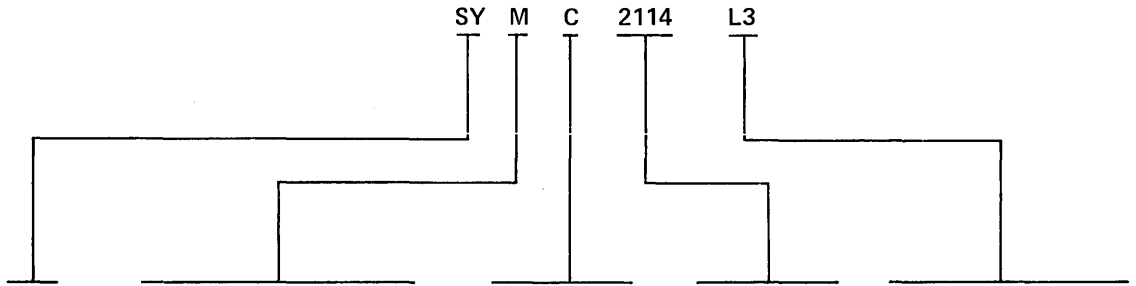
The CP110 SUPER JOLT CPU board provides direct interfacing via RS232, 20mA current loop and TTL. The 20mA current loop requires +5V and -10V whereas the RS232 interface requires +12V and -10V. All interfaces are wired in parallel on the input and output, thereby allowing any combination of interfaces to be used simultaneously.

The CP110 SUPER JOLT is available only as an assembled board with or without the RAP and TINY BASIC mask ROM. Other SUPER JOLT Family support boards are available, including a 4K static RAM board, MM100. A prototyping board is now available (AS200) — it has .1 inch centers and accepts wire wrap sockets.

General Information

General Information

Ordering Information

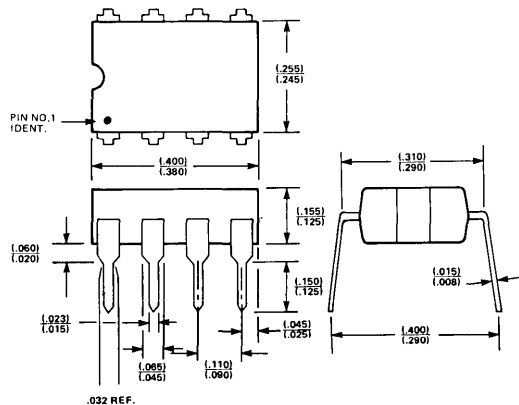


Prefix	Temperature Range No Designator — 0°C to 70°C M — -55°C to +125°C X — Special	Package Type C - Ceramic P - Molded D - Cerdip X - Dice F - Flat Pac T - TO Can	4 Digit Device Code	3 Digit Performance or Processing Designator
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For specially programmed devices (ROM's, 6530 Combo, etc.) Synertek will assign a special custom number. This number must be used when ordering these devices.

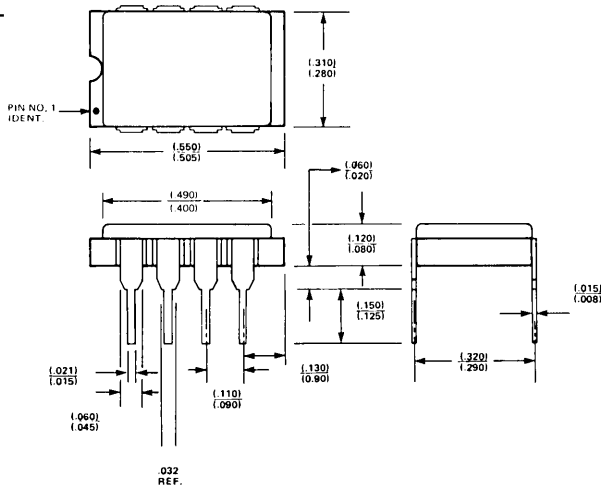
EXAMPLE: SYP 2316B, C28000: 2048 x 8 Read Only Memory, plastic 24 pin Dip, 0°C to +70°C, bit pattern as defined by C28000.

Plastic Dual In-Line — 8 Leads

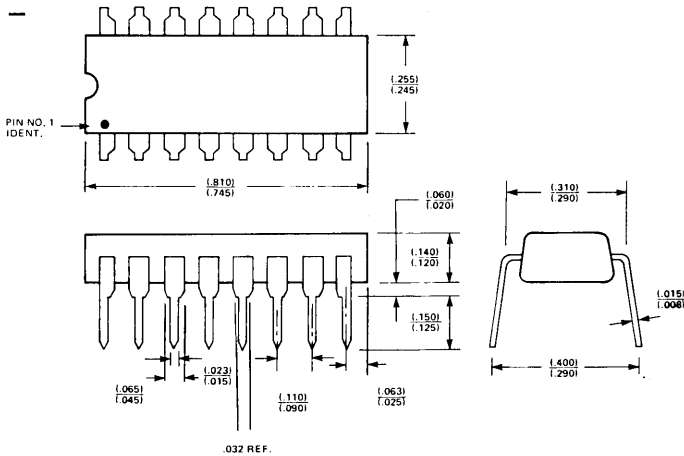


Packaging Information

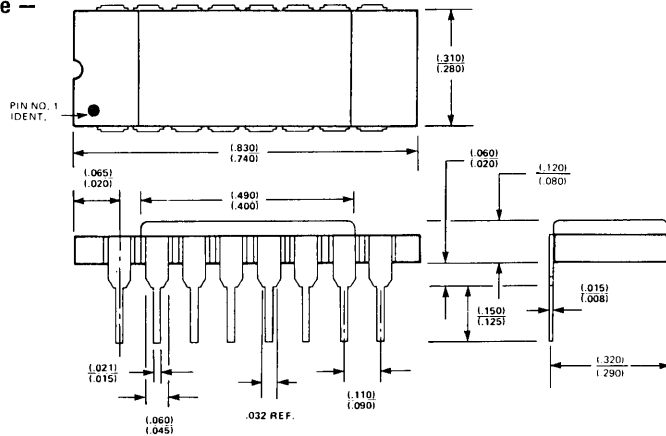
Ceramic Dual In-Line – 8 Leads



Plastic Dual In-Line – 16 Leads

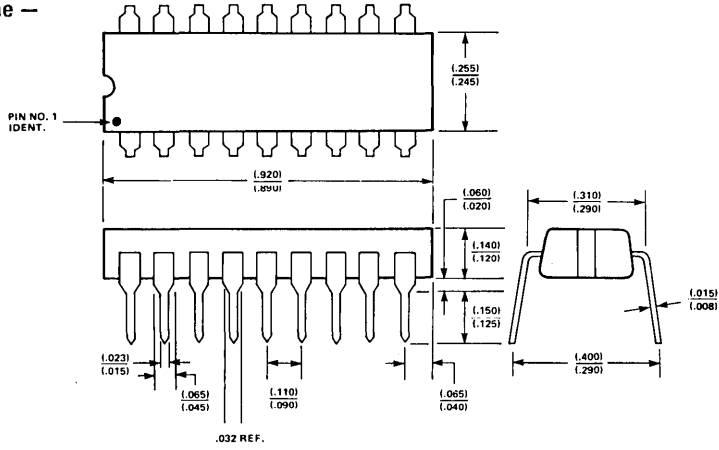


Ceramic Dual In-Line – 16 Leads

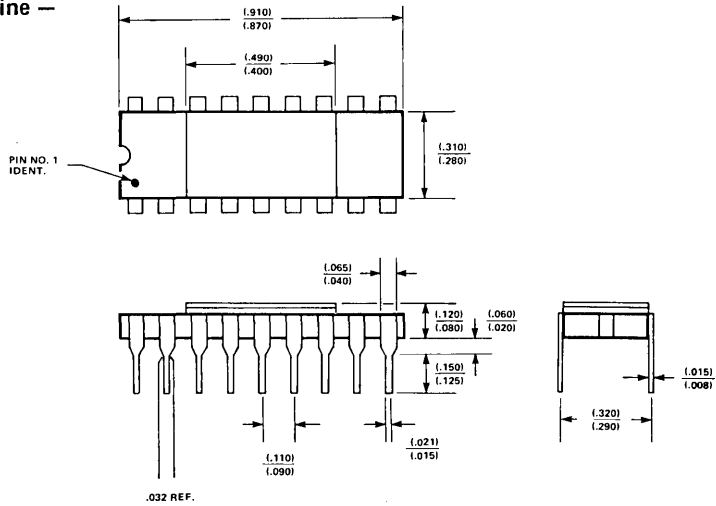


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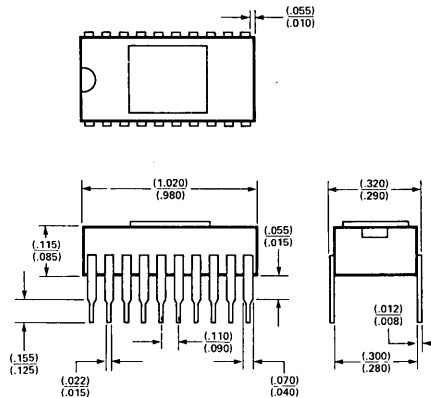
Plastic Dual In-Line – 18 Leads



Ceramic Dual In-Line – 18 Leads

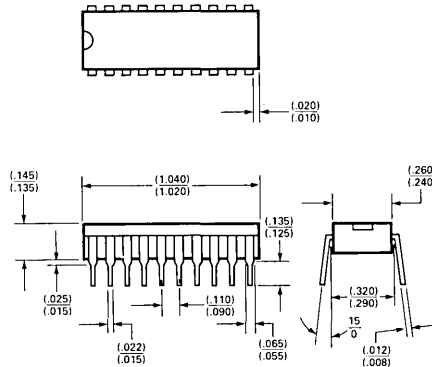


Ceramic Dual In-Line – 20 Leads

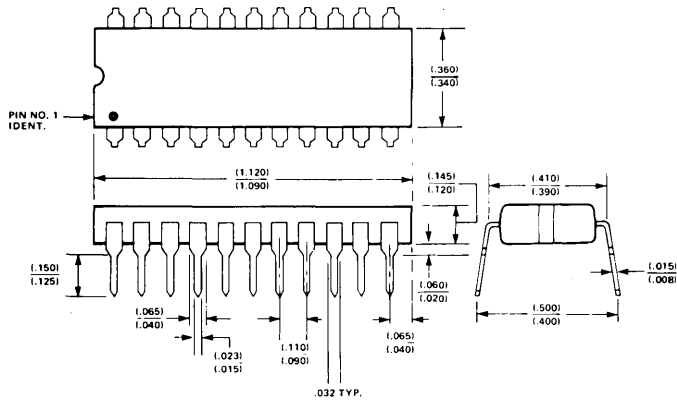


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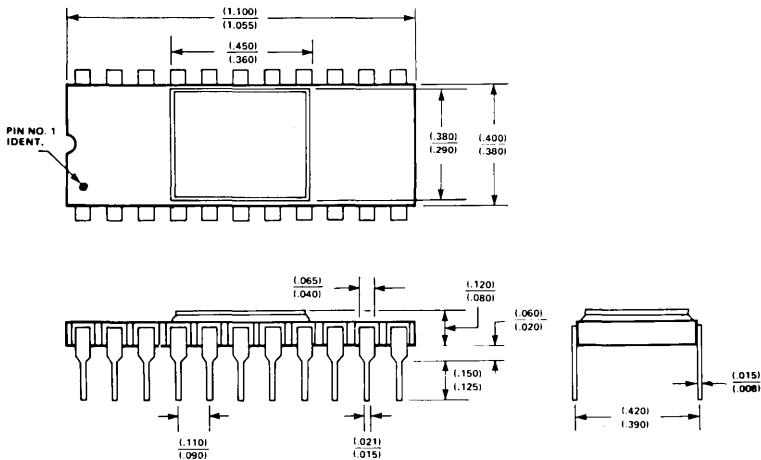
Molded Dual In-Line — 20 Leads



Plastic Dual In-Line — 22 Leads

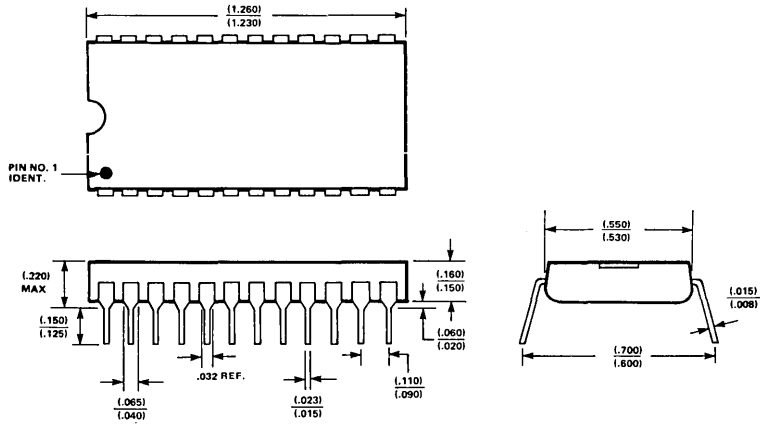


Ceramic Dual In-Line — 22 Leads

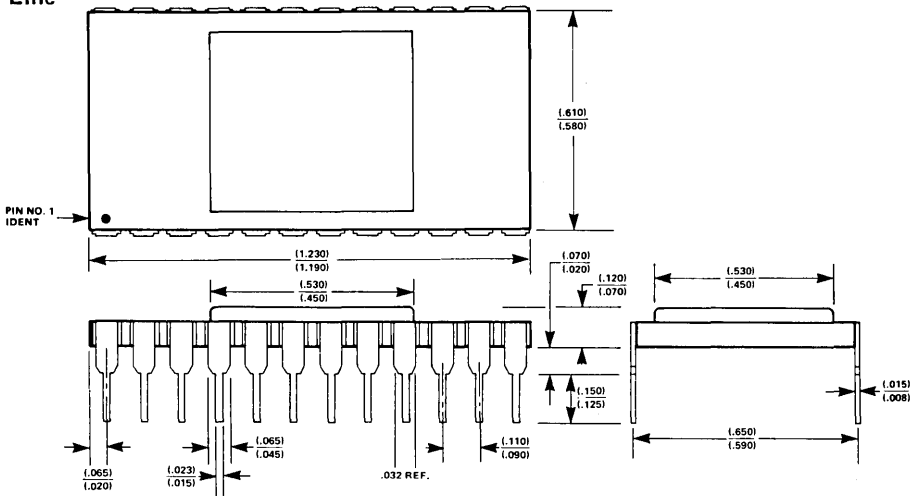


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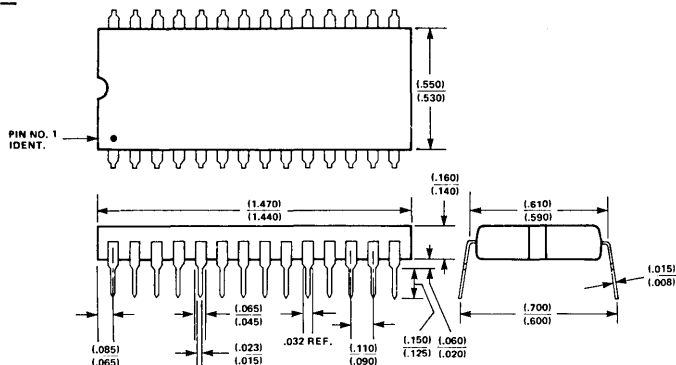
Plastic Dual In-Line – 24 Leads



Ceramic Dual In-Line – 24 Leads

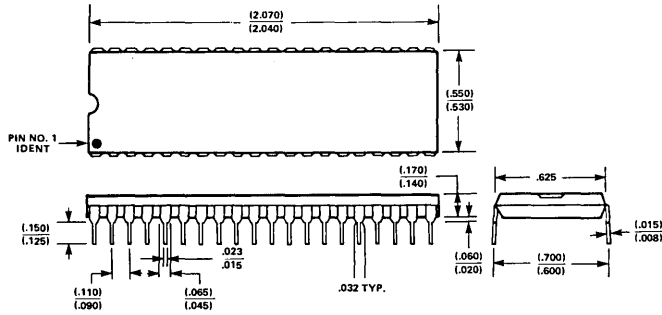


Plastic Dual In-Line – 28 Leads

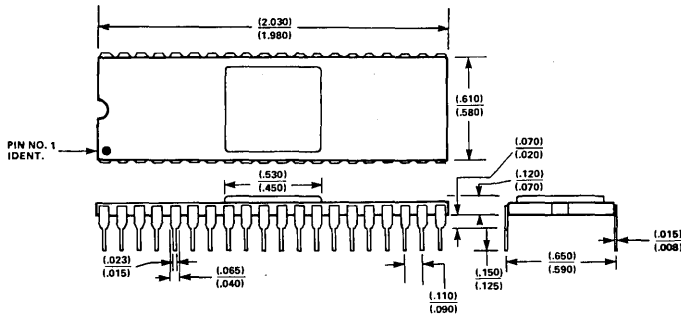


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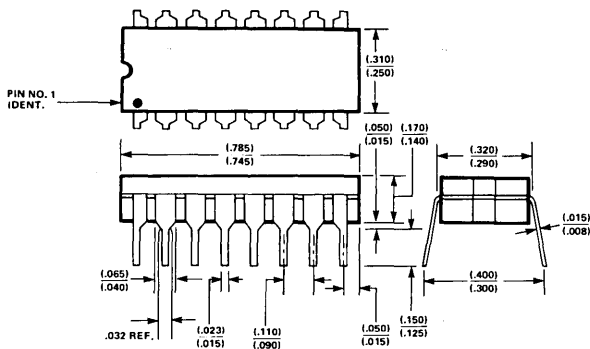
Plastic Dual In-Line — 40 Leads



Ceramic Dual In-Line — 40 Leads

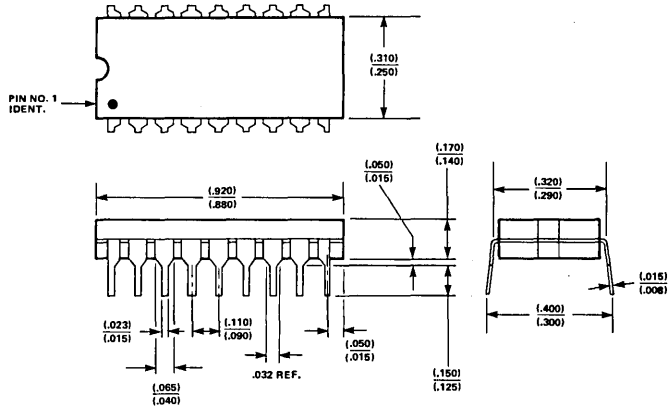


CerDIP Dual In-Line — 16 Leads

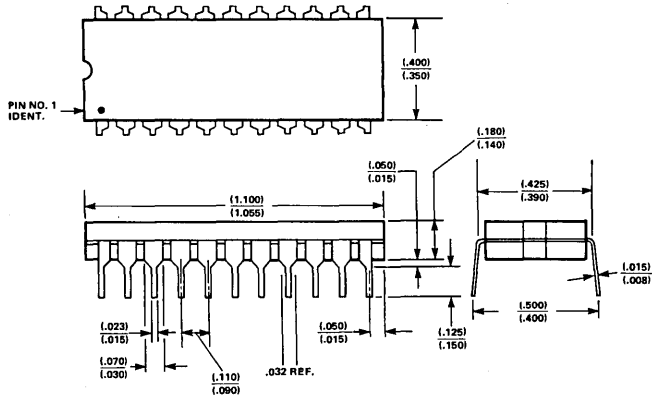


Packaging Information

CerDIP Dual In-Line – 18 Leads



CerDIP Dual In-Line – 22 Leads



Metal Can – 8 Leads

