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STANDARD
MICROSYSTEMS
CORPORATION

LPC47S42x

Enhanced Super I/O with LPC Interface for Server Applications

FEATURES

- 3.3 Volt Operation (5V Tolerant)
- Floppy Disk Controller (Supports Two FDCs)
- Multi-Mode Parallel Port
- Two UARTs
- 8042 Keyboard Controller
- SMBus Controller
- X-Bus Interface
- Programmable Wakeup Event Interface (nIO_PME Pin)
- SMI Support (nIO_SMI Pin)
- GPIOs (39)
- Fan Speed Control Output
- Fan Tachometer Input
- ISA IRQ to Serial IRQ Conversion
- XNOR Chain
- PC99 and ACPI 1.0 Compliant
- ISA Plug-and-Play Compatible Register Set
- Intelligent Auto Power Management
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM® Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - 480 Address, up to 15 IRQ and Three DMA Options
- Enhanced Digital Data Separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Keyboard Controller
  - 8042 Software Compatible
  - 8-Bit Microcomputer
  - 2k Bytes of Program ROM
  - 256 Bytes of Data RAM
  - Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 8-Bit Counter Timer
  - Port 92 Support
  - Fast Gate A20 and KRESET Outputs
- Serial Ports
  - Two Full Function Serial Ports
  - High Speed NS16C550 Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
  - IrDA 1.0, HP-SIR, ASK IR Support

- Multi-Mode Parallel Port with ChiProtect™
  - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 480 Address, up to 15 IRQ and 3 DMA Options
  - Multiplexed Command, Address and Data Bus
  - 8-Bit I/O Transfers
  - 8-Bit DMA Transfers
  - 16-Bit Address Qualification
  - Serial IRQ Interface Compatible with *Serialized IRQ Support for PCI Systems*
  - Power Management Event (PME) Interface Pin
- 100 Pin QFP Package

GENERAL DESCRIPTION

The LPC47S42x* is a 3.3V PC99 compliant Super I/O controller. The LPC47S42x implements the LPC interface, a pin reduced ISA interface which provides the same or better performance as the ISA/X-bus with a substantial savings in pins used. The part provides 39 GPIO pins, an SMBus controller, a fan speed control output, a fan tachometer input, four ISA IRQs that can be routed to any of the serial IRQs, and an X-Bus interface.

The LPC47S42x incorporates a keyboard interface, SMSC's true CMOS 765B floppy disk controller, advanced digital data separator, two 16C550 compatible UARTs, one Multi-Mode parallel port which includes ChiProtect circuitry plus EPP and ECP, and Intelligent Power Management. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use. The on-chip UARTs are compatible with the NS16C550. The parallel port is compatible with IBM PC/AT architecture, as well as IEEE 1284 EPP and ECP. The LPC47S42x incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The LPC47S42x supports the ISA Plug-and-Play Standard (Version 1.0a) and provides the recommended functionality to support Windows '95/'98 and PC99. The I/O Address, DMA Channel and Hardware IRQ of each logical device in the LPC47S42x may be reprogrammed through the internal configuration registers. There are 480 I/O address location options, a Serialized IRQ interface, and three DMA channels.

*The “x” in the part number is a designator that changes depending upon the particular BIOS used inside the specific chip. “2” denotes AMI Keyboard BIOS and “7” denotes Phoenix 42i Keyboard BIOS.

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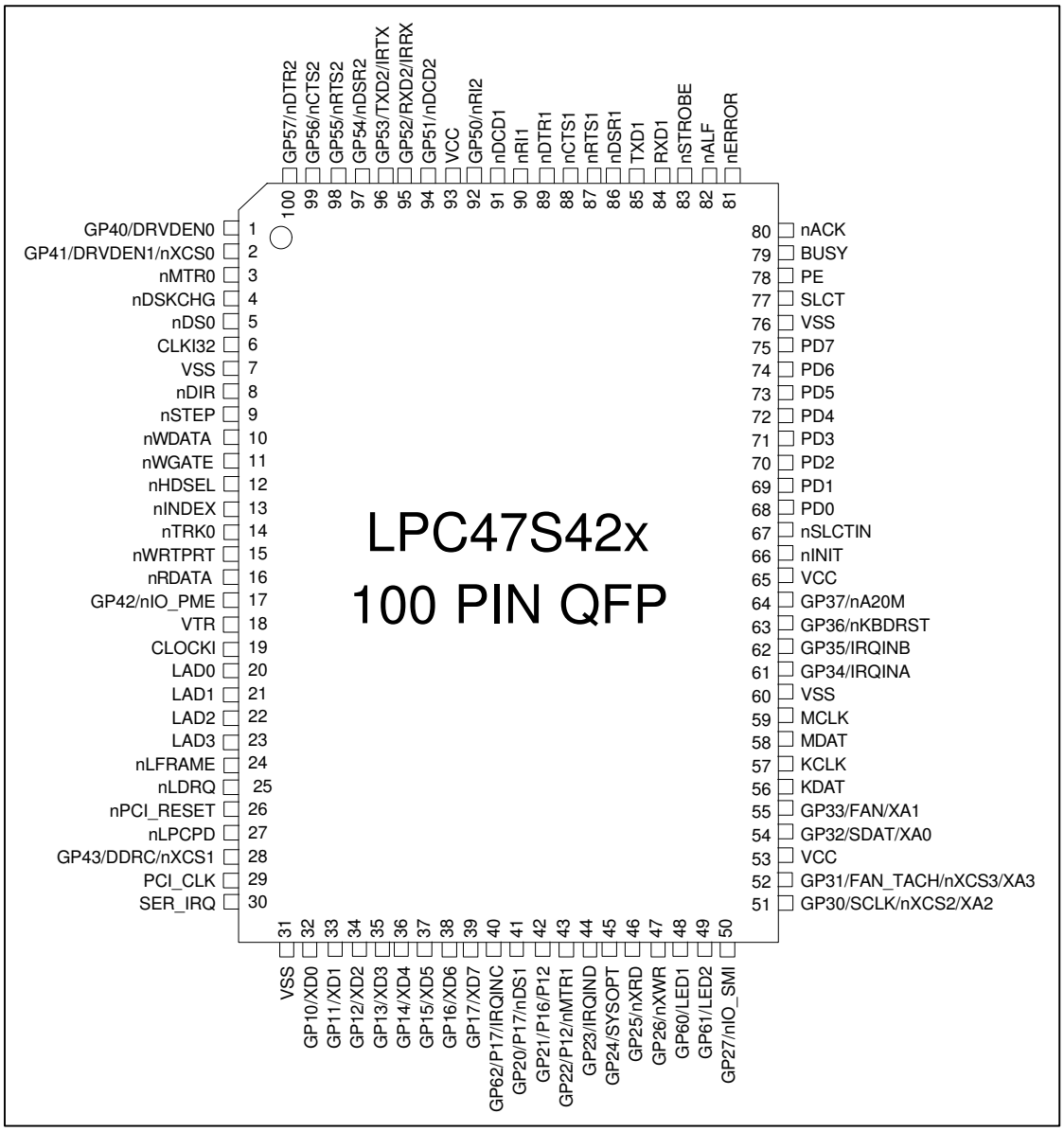
PIN CONFIGURATION



DESCRIPTION OF PIN FUNCTIONS

Note: There are no internal pullups on any of the pins in the LPC47S42x.

PIN #	NAME	FUNCTION	BUFFER TYPE	BUFFER TYPE PER FUNCTION (NOTE 1)
		FDD INTERFACE		
1	GP40/DRVDEN0	General Purpose I/O/Drive Density Select 0	IO12	(I/O12/OD12)/ (O12/OD12)
2	GP41/DRVDEN1/ nXCS0	General Purpose I/O/Drive Density Select 1/X-Bus Chip Select 0	IO12	(I/O12/OD12)/ (O12/OD12)/O12
3	nMTR0	Motor On 0	O12	(O12/OD12)
4	nDSKCHG	Disk Change	IS	IS
5	nDS0	Drive Select 0	O12	(O12/OD12)
8	nDIR	Step Direction	O12	(O12/OD12)
9	nSTEP	Step Pulse	O12	(O12/OD12)
10	nWDATA	Write Disk Data	O12	(O12/OD12)
11	nWGATE	Write Gate	O12	(O12/OD12)
12	nHDSEL	Head Select	O12	(O12/OD12)
13	nINDEX	Index Pulse Input	IS	IS
14	nTRK0	Track 0	IS	IS
15	nWRTPRT	Write Protected	IS	IS
16	nRDATA	Read Disk Data	IS	IS
		LPC INTERFACE		
20	LAD0	Multiplexed Command Address and Data 0	PCI_IO	PCI_IO
21	LAD1	Multiplexed Command Address and Data 1	PCI_IO	PCI_IO
22	LAD2	Multiplexed Command Address and Data 2	PCI_IO	PCI_IO
23	LAD3	Multiplexed Command Address and Data 3	PCI_IO	PCI_IO
24	nLFRAME	Frame	PCI_I	PCI_I
25	nLDRQ	Encoded DMA Request	PCI_O	PCI_O
26	nPCI_RESET	PCI Reset	PCI_I	PCI_I
27	nLPCPD	Power Down (Note 2)	PCI_I	PCI_I
29	PCI_CLK	PCI Clock	PCI_ICLK	PCI_ICLK
30	SER_IRQ	Serial IRQ	PCI_IO	PCI_IO
		GENERAL PURPOSE I/O PINS		
17	GP42/nIO_PME	General Purpose I/O/Power Management Event Output	IO12	(I/O12/OD12)/ (O12/OD12)
28	GP43/DDRC/nXCS1	General Purpose I/O/Device Disable Reg. Control/X-Bus Chip Select 1	IO8	(I/O8/OD8)/I/O8
32	GP10/XD0	General Purpose I/O/X-Bus Data Bit 0	IO8	(I/O8/OD8)/IO8

PIN #	NAME	FUNCTION	BUFFER TYPE	BUFFER TYPE PER FUNCTION (NOTE 1)
33	GP11/XD1	General Purpose I/O/X-Bus Data Bit 1	IO8	(I/O8/OD8)/IO8
34	GP12/XD2	General Purpose I/O/X-Bus Data Bit 2	IO8	(I/O8/OD8)/IO8
35	GP13/XD3	General Purpose I/O/X-Bus Data Bit 3	IO8	(I/O8/OD8)/IO8
36	GP14/XD4	General Purpose I/O/X-Bus Data Bit 4	IO8	(I/O8/OD8)/IO8
37	GP15/XD5	General Purpose I/O/X-Bus Data Bit 5	IO8	(I/O8/OD8)/IO8
38	GP16/XD6	General Purpose I/O/X-Bus Data Bit 6	IO8	(I/O8/OD8)/IO8
39	GP17/XD7	General Purpose I/O/X-Bus Data Bit 7	IO8	(I/O8/OD8)/IO8
40	GP62/P17/IRQINC	General Purpose I/O/P17/ IRQ Input C	IO8	(I/O8/OD8)/IO8/I
41	GP20/P17/nDS1	General Purpose I/O/P17 /Drive Select 1	IO12	(I/O12/OD12)/ IO12/(O12/OD12)
42	GP21/P16/P12	General Purpose I/O/P16/P12	IO8	(I/O8/OD8)/IO8/ IO8
43	GP22/P12/nMTR1	General Purpose I/O/P12/Motor On 1	IO12	(I/O12/OD12)/ IO12/(O12/OD12)
44	GP23/IRQIND	General Purpose I/O/IRQ Input D	IO8	(I/O8/OD8)/I
45	GP24/SYSOPT	General Purpose I/O/System Option (Note 7)	IO8	(I/O8/OD8)
46	GP25/nXRD	General Purpose I/O/X-Bus Read Strobe (Note 10)	IO8	(I/O8/OD8)/O8
47	GP26/nXWR	General Purpose I/O/X-Bus Write Strobe (Note 10)	IO8	(I/O8/OD8)/O8
48	GP60/LED1	General Purpose I/O/LED1 (Note 9)	IO12	(I/O12/OD12)/ (O12/OD12)
49	GP61/LED2	General Purpose I/O/LED2 (Note 9)	IO12	(I/O12/OD12)/ (O12/OD12)
50	GP27/nIO_SMI	General Purpose I/O/nIO_SMI	IO12	(I/O12/OD12)/ (O12/OD12)
61	GP34/IRQINA	General Purpose I/O/IRQ Input A	IO12	(I/O21/OD12)/I
62	GP35/IRQINB	General Purpose I/O/IRQ Input B	IO12	(I/O12/OD12)/I

PIN #	NAME	FUNCTION	BUFFER TYPE	BUFFER TYPE PER FUNCTION (NOTE 1)
		SMBUS PINS		
51	GP30/SCLK/ nXCS2/XA2	General Purpose I/O/SMBus Clock/X-Bus Chip Select 2/X-Bus Address 2	IO12	(I/O12/OD12)/ IOD12/O12/O12
54	GP32/SDAT/XA0	General Purpose I/O/SMBus Data/X-Bus Address 0	IO12	(I/O12/OD12)/ IOD12/O12
		FAN CONTROL PINS		
52	GP31/FAN_TACH/ nXCS3/XA3	General Purpose I/O/Fan Tachometer Input/X-Bus Chip Select 3/X-Bus Address 3	IO8	(I/O8/OD8)/I/O8/ O8
55	GP33 /FAN/XA1	General Purpose I/O /Fan Control/X-Bus Address 1 (Note 4)	IO12	(I/O12/OD12)/ (O12/OD12)/O12
		KEYBOARD/MOUSE		
56	KDAT	Keyboard Data	IOD16	IOD16
57	KCLK	Keyboard Clock	IOD16	IOD16
58	MDAT	Mouse Data	IOD16	IOD16
59	MCLK	Mouse Clock	IOD16	IOD16
63	GP36/nKBDRST	General Purpose I/O /Keyboard Reset (Note 8)	IO8	(I/O8/OD8)/O8
64	GP37/A20M	General Purpose I/O /Gate A20 (Note 8)	IO8	(I/O8/OD8)/O8
		PARALLEL PORT INTERFACE		
66	nINIT/nDIR	Initiate Output/FDC Direction Control	OP14	(OD14/OP14)/ OD14
67	nSLCTIN/nSTEP	Printer Select Input/FDC Step Pulse	OP14	(OD14/OP14)/ OD14
68	PD0/nINDEX	Port Data 0/FDC Index	IS/OP14	IOP14/IS
69	PD1/nTRK0	Port Data 1/FDC Track 0	IS/OP14	IOP14/IS
70	PD2/nWRTPRT	Port Data 2/FDC Write Protected	IS/OP14	IOP14/IS
71	PD3/nRDATA	Port Data 3/FDC Read Disk Data	IS/OP14	IOP14/IS
72	PD4/nDSKCHG	Port Data 4/FDC Disk Change	IS/OP14	IOP14/IS
73	PD5	Port Data 5	IOP14	IOP14
74	PD6/nMTR0	Port Data 6/FDC Motor On 0	IOP14	IOP14/OD14
75	PD7	Port Data 7	IOP14	IOP14
77	SLCT/nWGATE	Printer Selected Status/FDC Write Gate	IO12	I/OD12
78	PE/nWDATA	Paper End/FDC Write Data	IO12	I/OD12
79	BUSY/nMTR1	Busy/FDC Motor On	IO12	I/OD12
80	nACK/nDS1	Acknowledge/FDC Drive Select 1	IO12	I/OD12
81	nERROR/nHDSEL	Error/FDC Head Select	IO12	I/OD12
82	nALF/nDRVDEN0	Autofeed Output/FDC Density Select	OP14	(OD14/OP14)/ OD14

PIN #	NAME	FUNCTION	BUFFER TYPE	BUFFER TYPE PER FUNCTION (NOTE 1)
83	nSTROBE/nDS0	Strobe Output/FDC Drive Select	OP14	(OD14/OP14)/ OD14
SERIAL PORT 1 INTERFACE				
84	RXD1	Receive Data 1	IS	IS
85	TXD1	Transmit Data 1	O12	O12
86	nDSR1	Data Set Ready 1	I	I
87	nRTS1	Request to Send 1	O8	O8
88	nCTS1	Clear to Send 1	I	I
89	nDTR1	Data Terminal Ready 1	O6	O6
90	nRI1	Ring Indicator 1	I	I
91	nDCD1	Data Carrier Detect 1	I	I
SERIAL PORT 2 INTERFACE				
92	GP50/nRI2	General Purpose I/O/Ring Indicator 2	IO8	(I/O8/OD8)/I
94	GP51/nDCD2	General Purpose I/O/Data Carrier Detect 2	IO8	(I/O8/OD8)/I
95	GP52/RXD2/IRRX	General Purpose I/O/Receive Data 2/IRRX	IS/O8	(IS/O8/OD8)/IS/IS
96	GP53/TXD2/IRTX	General Purpose I/O/Transmit Data 2/IRTX (Note 5, 6)	IO12	(I/O12/OD12)/O12/ O12
97	GP54/nDSR2	General Purpose I/O/Data Set Ready 2	IO8	(I/O8/OD8)/I
98	GP55/nRTS2	General Purpose I/O/Request to Send 2	IO8	(I/O8/OD8)/O8
99	GP56/nCTS2	General Purpose I/O/Clear to Send 2	IO8	(I/O8/OD8)/I
100	GP57/nDTR2	General Purpose I/O/Data Terminal Ready 2	IO8	(I/O8/OD8)/O8
POWER PINS				
53, 65, 93	VCC	+3.3 Volt Supply Voltage		
18	VTR	+3.3 Volt Standby Supply Voltage (Note 6)		
7, 31, 60, 76	VSS	Ground		
CLOCK PINS				
6	CLKI32	32.768kHz Standby Clock Input (Note 3)	IS	IS
19	CLOCKI	14.318MHz Clock Input	IS	IS

Note: The "n" as the first letter of a signal name indicates an "Active Low" signal.

Note 1: Buffer types per function on multiplexed pins are separated by a slash “/”. Buffer types in parenthesis represent multiple buffer types for a single pin function.

Note 2: The nLPCPD pin may be tied high. The LPC interface will function properly if the nPCI_RESET signal follows the protocol defined for the nLRESET signal in the “Low Pin Count Interface Specification”.

Note 3: If the 32kHz input clock is not used the CLKI32 pin must be grounded. There is a bit in the configuration register at 0xF0 in Logical Device A that indicates whether or not the 32KHz clock is connected. This bit determines the clock source for the fan tachometer, LED and “wake on specific key” logic. Set this bit to ‘1’ if the clock is not connected.

Note 4: The fan control pin (FAN) comes up as output and low following a VCC POR and Hard Reset. This pin reverts to its non-inverting General Purpose I/O output function when VCC is removed from the part.

Note 5: The GP53/TXD2/IRTX pin is an output and low when the part is under VTR power (VCC=0). The pin comes up as output and low following a VCC POR and Hard Reset.

Note 6: VTR can be connected to VCC if no wakeup functionality is required.

Note 7: The GP24/SYSOPT pin requires an external pulldown resistor to put the base I/O address for configuration at 0x02E. An external pullup resistor is required to move the base I/O address for configuration to 0x04E.

Note 8: External pullups must be placed on the nKBDRST and A20M pins. These pins are General Purpose I/Os that are inputs after an initial power-up (VTR POR). If the nKBDRST and A20M functions are to be used, the system must ensure that these pins are high. See Section “Pins That Require External Pullup Resistor”.

Note 9: The LED pins are powered by VTR so that the LEDs can be controlled when the part is under VTR power. The GP61 pin defaults to the LED function active (blinking at a 1Hz rate, 50% duty cycle) on initial power up (as long as the 32 kHz clock input is active).

Note 10: External pullups are required on the nXRD and nXWR pins.

Buffer Type Descriptions

IO12	Input/Output, 12mA sink, 6mA source.
IS/O12	Input with Schmitt Trigger/Output, 12mA sink, 6mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Open Drain Output, 12mA sink.
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD8	Open Drain Output, 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.
IS/O8	Input with Schmitt Trigger/Output, 8mA sink, 4mA source.
OD14	Open Drain Output, 14mA sink.
OP14	Output, 14mA sink, 14mA source.
IOP14	Input/Output, 14mA sink, 14mA source. Backdrive protected.
IOD16	Input/Output (Open Drain), 16mA sink.
O4	Output, 4mA sink, 2mA source.
I	Input TTL Compatible.
IS	Input with Schmitt Trigger.
PCI_IO	Input/Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_O	Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_OD	Open Drain Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_I	Input. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_ICLK	Clock Input. These pins meet the PCI 3.3V AC and DC Characteristics and timing. (Note 2)

Note 1. See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2.
Note 2. See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2. and 4.2.3.

Pins That Require External Pullup Resistors

The following pins require external pullup resistors:

- KDAT
- KCLK
- MDAT
- MCLK
- GP36/KBDRST if KBDRST function is used
- GP37/A20M if A20M function is used
- GP20/P17/nDS1 If P17 function is used
- GP21/P16/P12 if P16 or P12 function is used
- GP22/P12/nMTR1 if P12 function is used
- GP27/nIO_SMI if nIO_SMI function is used as Open Collector Output
- GP42/nIO_PME if nIO_PME function is used as Open Collector Output
- SER_IRQ
- GP40/DRVDEN0 if DRVDEN0 function is used as Open Collector Output
- GP41/DRVDEN1/XCS0 if DRVDEN1 function is used as Open Collector Output
- GP23, GP 34, GP35 and GP62 if IRQINx function is used
- nMTR0 if used as Open Collector Output
- nDS0 if used as Open Collector Output
- nDIR if used as Open Collector Output
- nSTEP if used as Open Collector Output
- nWDATA if used as Open Collector Output
- nWGATE if used as Open Collector Output
- nHDSEL if used as Open Collector Output
- nINDEX
- nTRK0
- nWRTPRT
- nRDATA
- nDSKCHG
- nXRD
- nXWR

3.3 VOLT OPERATION / 5 VOLT TOLERANCE

The LPC47S42x is a 3.3 Volt part. It is intended solely for 3.3V applications. Non-LPC bus pins are 5V tolerant; that is, the input voltage is 5.5V max, and the I/O buffer output pads are backdrive protected.

The LPC interface pins are 3.3 V only. These signals meet PCI DC specifications for 3.3V signaling. These pins are:

- LAD[3:0]
- nLFRAME
- nLDRQ
- nLPCPD

The input voltage for all other pins is 5.5V max. These pins include all non-LPC Bus pins and the following pins:

- nPCI_RESET
- PCI_CLK
- SER_IRQ
- nIO_PME

POWER FUNCTIONALITY

The LPC47S42x has two power planes: VCC and VTR.

VCC Power

The LPC47S42x is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). See the Operational Description Section and the Maximum Current Values subsection.

VTR Support

The LPC47S42x requires a trickle supply (V_{TR}) to provide sleep current for the programmable wake-up events in the PME interface when V_{CC} is removed. The VTR supply is 3.3 Volts (nominal). See the Operational Description Section. The maximum VTR current that is required depends on the functions that are used in the part. See Trickle Power Functionality subsection and the Maximum Current Values subsection. If the LPC47S42x is not intended to provide wake-up capabilities on standby current, V_{TR} can be connected to V_{CC}. The V_{TR} pin generates a V_{TR} Power-on-Reset signal to initialize these components.

Note: If V_{TR} is to be used for programmable wake-up events when V_{CC} is removed, V_{TR} must be at its full minimum potential at least 10 µs before V_{CC} begins a power-on cycle. When V_{TR} and V_{CC} are fully powered, the potential difference between the two supplies must not exceed 500mV.

Internal PWRGOOD

An internal PWRGOOD logical control is included to minimize the effects of pin-state uncertainty in the host interface as V_{CC} cycles on and off. When the internal PWRGOOD signal is "1" (active), V_{CC} > 2.3V (nominal), and the LPC47S42x host interface is active. When the internal PWRGOOD signal is "0" (inactive), $V_{CC} \leq$ 2.3V (nominal), and the LPC47S42x host interface is inactive; that is, LPC bus reads and writes will not be decoded.

The LPC47S42x device pins nIO_PME, CLOCKI32, KDAT, MDAT, IRRX, nRI1, nRI2, RXD2 and most GPIOs (as input) are part of the PME interface and remain active when the internal PWRGOOD signal has gone inactive, provided V_{TR} is powered. The GP53/TXD2/IRTX, GP60/LED1 and GP61/LED2 pins also remain active when the internal PWRGOOD signal has gone inactive, provided V_{TR} is powered. See Trickle Power Functionality section.

32.768 kHz Trickle Clock Input

The LPC47S42x utilizes a 32.768 kHz trickle clock input to supply a clock signal for the fan tachometer logic, WDT, LED blink and wake on specific key function. See the following section for more information.

Indication of 32kHz Clock

There is a bit to indicate whether or not the 32kHz clock input is connected to the LPC47S42x. This bit is located at bit 0 of the CLOCKI32 register at 0xF0 in Logical Device A. This register is powered by VTR and reset on a VTR POR.

Bit[0] (CLK32_PRSN) is defined as follows:
0=32kHz clock is connected to the CLKI32 pin (default)
1=32kHz clock is not connected to the CLKI32 pin (pin is grounded).

Bit 0 controls the source of the 32kHz (nominal) clock for the CIR wakeup, fan tachometer logic, the LED blink logic, the WDT and the "wake on specific key" logic. When the external 32kHz clock is connected, that will be the source for the fan tachometer, LED, WDT and "wake on specific key" logic. When the external 32kHz clock is not connected, an internal 32kHz clock source will be derived from the 14MHz clock for the fan tachometer, LED, WDT and "wake on specific key" logic.

The following functions will not work under VTR power (VCC removed) if the external 32kHz clock is not connected. These functions will work under VCC power even if the external 32kHz clock is not connected.

- Fan tachometer
- Wake on specific key
- LED blink
- WDT

Trickle Power Functionality

When the LPC47S42x is running under VTR only, the PME wakeup events are active and (if enabled) able to assert the nIO_PME pin active low. The following lists the wakeup events:

- UART 1 Ring Indicator
- UART 2 Ring Indicator
- Keyboard data
- Mouse data
- Wake on Specific Key Logic
- Fan Tachometer (Note)
- GPIOs for wakeup. See below.

Note. The Fan Tachometer can generate a PME when VCC=0. Clear the enable bits for the fan tachometers before removing fan power.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means they will, at a minimum, source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup inputs are GP10-GP17, GP20-GP27, GP30-GP37, GP41, GP43, GP50-GP57, GP60, GP61. These GPIOs function as follows (with the exception of GP53, GP60 and GP61 - see below):

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are for PME wakeup as a GPIO function (or alternate function). Note that GP33 cannot be used for wakeup under VTR power (VCC=0) since this is the fan control pin which comes up as output and low following a VCC POR and Hard Reset. GP53 cannot be used for wakeup under VTR power since this has the IRTX function and comes up as output and low following a VTR POR, a VCC POR and Hard Reset. Also, GP33 reverts to its non-inverting GPIO output function when VCC is removed from the part. GP43 reverts to the basic GPIO function when VCC is removed form the part, but its programmed input/output, invert/non-invert output buffer type is retained.

The other GPIOs function as follows:
GP40, GP62:

- Buffers powered by VCC, but in the absence of VCC they are backdrive protected. These pins do not have input buffers into the wakeup logic that are powered by VTR.

These pins are not used for wakeup.

GP42, GP53, GP60, GP61:

- Buffers powered by VTR.

GP42 is the nIO_PME pin.
GP53 has IRTX as the alternate function and its output buffer is powered by VTR so that the pin is always forced low on VTR POR, VCC POR and Hard Reset. The IRTX pin (GP53/TXD2/IRTX) is powered by VTR so that it is driven low when VCC = 0V with VTR = 3.3V. This pin is driven low on VTR POR, VCC POR and Hard Reset regardless of the selected pin function and regardless of the state of internal PWRGOOD (i.e., when VCC=3.3V and when VCC=0V with VTR=3.3V). The GP53/TXD2/IRTX pin will remain low following a VCC POR until the IRTX function is selected and the serial port is enabled by setting the activate bit, at which time the pin will reflect the state of the IR transmit output of the IR block. If the TXD2 function is selected for the pin, it will remain low following a VCC POR until the serial port is enabled by setting the activate bit, at which time the pin will reflect the state of the transmit output of the serial port. If the GPIO output function is selected, the pin will reflect the state of the data bit.

GP60 and GP61 are used for the LED functions.

See the Table in the GPIO section for more information.

The following list summarizes the blocks, registers and pins that are powered by VTR.

- PME interface block
- Runtime register block (includes all PME, SMI, GPIO and other miscellaneous registers)
- Wake on Specific Key logic
- LED control logic
- Pins for PME Wakeup:
  - GP42/nIO_PME (output, buffer powered by VTR)
  - nRI1 (input)
  - GP50/nRI2 (input)
  - GP52/RXD2/IRRX (input)
  - KDAT (input)
  - MDAT (input)
  - GPIOs (GP10-GP17, GP20-GP27, GP30-GP37, GP41, GP43, GP50-GP57, GP60, GP61) – all input-only except GP53, GP60, GP61. See below.

- Other Pins
  - GP53/TXD2/IRTX (output, buffer powered by VTR)
  - GP60/LED1 (output, buffer powered by VTR)
  - GP61/LED2 (output, buffer powered by VTR)

Maximum Current Values

Refer to the “Operational Description” section for the maximum current values.

The maximum VTR current, I_{TR}, is given with all outputs open (not loaded). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by all pins that are driven by VTR. The pins that are powered by VTR are as follows: GP42/nIO_PME, GP53/TXD2/IRTX, GP60/LED1, GP61/LED2. These pins, if configured as push-pull outputs, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, I_{CC}, is given with all outputs open (not loaded).

Power Management Events (PME/SCI)

The LPC47S42x offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal on pin 17. See the “PME Support” section.

FUNCTIONAL DESCRIPTION

Super I/O Registers

The address map, shown below in Table 1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the FDC, serial and parallel ports, PME register block, Game port and configuration register block can be moved via the configuration registers. Some addresses are used to access more than one register.

Host Processor Interface (LPC)

The host processor communicates with the LPC47S42x through a series of read/write registers via the LPC interface. The port addresses for these registers are shown in Table 1. Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

Table 1 - Super I/O Block Addresses

ADDRESS	BLOCK NAME	LOGICAL DEVICE	NOTES
Base+(0-5) and +(7)	Floppy Disk	0	
Base+(0-7)	Serial Port Com 1	4	
Base+(0-7)	Serial Port Com 2	5	IR Support
 Base+(0-3) Base+(0-7) Base+(0-3), +(400-402) Base+(0-7), +(400-402)	Parallel Port SPP EPP ECP ECP+EPP+SPP	3	
60, 64	KYBD	7	
60 - 67	X-Bus	8	
Base + (0-6C)	Runtime Registers	A	
Base+(0-3)	SMBus	B	
Base + (0-1)	Configuration		

Note 1: Refer to the configuration register descriptions for setting the base address.

LPC Interface
The following sub-sections specify the implementation of the LPC bus.

LPC Interface Signal Definition
The signals required for the LPC bus interface are described in the table below. LPC bus signals use PCI 33MHz electrical signal characteristics.

SIGNAL NAME	TYPE	DESCRIPTION
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
nLFRAME	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
nPCI_RESET	Input	PCI Reset. Used as LPC Interface Reset.
nLDRQ	Output	Encoded DMA/Bus Master request for the LPC interface.
nIO_PME	OD	Power Mgt Event signal. Allows the LPC47S42x to request wakeup.
nLPCPD	Input	Powerdown Signal. Indicates that the LPC47S42x should prepare for power to be shut on the LPC interface.
SER_IRQ	I/O	Serial IRQ.
PCI_CLK	Input	PCI Clock.

LPC Cycles
The following cycle types are supported by the LPC protocol.

CYCLE TYPE	TRANSFER SIZE
I/O Write	1 Byte Transfer
I/O Read	1 Byte Transfer
DMA Write	1 Byte
DMA Read	1 Byte

The LPC47S42x ignores cycles that it does not support.

Field Definitions

The data transfers are based on specific fields that are used in various combinations, depending on the cycle type. These fields are driven onto the LAD[3:0] signal lines to communicate address, control and data information over the LPC bus between the host and the LPC47S42x. See the *Low Pin Count (LPC) Interface Specification* Revision 1.0 from Intel, Section 4.2 for definition of these fields.

nLFRAME Usage

nLFRAME is used by the host to indicate the start of cycles and the termination of cycles due to an abort or time-out condition. This signal is to be used by the LPC47S42x to know when to monitor the bus for a cycle.

This signal is used as a general notification that the LAD[3:0] lines contain information relative to the start or stop of a cycle, and that the LPC47S42x monitors the bus to determine whether the cycle is intended for it. The use of nLFRAME allows the LPC47S42x to enter a lower power state internally. There is no need for the LPC47S42x to monitor the bus when it is inactive, so it can decouple its state machines from the bus, and internally gate its clocks.

When the LPC47S42x samples nLFRAME active, it immediately stops driving the LAD[3:0] signal lines on the next clock and monitor the bus for new cycle information.

The nLFRAME signal functions as described in the Low Pin Count (LPC) Interface Specification Reference.

I/O Read and Write Cycles

The LPC47S42x is the target for I/O cycles. I/O cycles are initiated by the host for register or FIFO accesses, and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1. EPP cycles will depend on the speed of the external device, and may have much longer Sync times.

Data transfers are assumed to be exactly 1-byte. If the CPU requested a 16 or 32-bit transfer, the host will break it up into 8-bit transfers.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 5.2, for the sequence of cycles for the I/O Read and Write cycles.

DMA Read and Write Cycles

DMA read cycles involve the transfer of data from the host (main memory) to the LPC47S42x. DMA write cycles involve the transfer of data from the LPC47S42x to the host (main memory). Data will be coming from or going to a FIFO and will have minimal Sync times. Data transfers to/from the LPC47S42x are 1 byte.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 6.4, for the field definitions and the sequence of the DMA Read and Write cycles.

DMA Protocol

DMA on the LPC bus is handled through the use of the nLDRQ lines from the LPC47S42x and special encodings on LAD[3:0] from the host.

The DMA mechanism for the LPC bus is described in the Low Pin Count (LPC) Interface Specification Reference.

Power Management

CLOCKRUN Protocol

The nCLKRUN pin is not implemented in the LPC47S42x. See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.1.

LPCPD Protocol

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.2.

SYNC Protocol

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 4.2.1.8 for a table of valid SYNC values.

Typical Usage

The SYNC pattern is used to add wait states. For read cycles, the LPC47S42x immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the LPC47S42x needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The LPC47S42x will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value.

The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The LPC47S42x uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. This is provided for EPP cycles, where the number of wait states could be quite large (>1 microsecond). However, the LPC47S42x uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

SYNC Timeout

The SYNC value is driven within 3 clocks. If the host observes 3 consecutive clocks without a valid SYNC pattern, it will abort the cycle.

The LPC47S42x does not assume any particular timeout. When the host is driving SYNC, it may have to insert a very large number of wait states, depending on PCI latencies and retries.

SYNC Patterns and Maximum Number of SYNCS

If the SYNC pattern is 0101, then the host assumes that the maximum number of SYNCs is 8.

If the SYNC pattern is 0110, then no maximum number of SYNCs is assumed. The LPC47S42x has protection mechanisms to complete the cycle. This is used for EPP data transfers and will utilize the same timeout protection that is in EPP.

SYNC Error Indication

The LPC47S42x reports errors via the LAD[3:0] = 1010 SYNC encoding.

If the host was reading data from the LPC47S42x, data will still be transferred in the next two nibbles. This data may be invalid, but it will be transferred by the LPC47S42x. If the host was writing data to the LPC47S42x, the data had already been transferred.

In the case of multiple byte cycles, such as DMA cycles, an error SYNC terminates the cycle. Therefore, if the host is transferring 4 bytes from a device, if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

I/O and DMA START Fields
I/O and DMA cycles use a START field of 0000.

Reset Policy
The following rules govern the reset policy:

1) When nPCI_RESET goes inactive (high), the clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
2) When nPCI_RESET goes active (low):
   a) The host drives the nLFRAME signal high, tristates the LAD[3:0] signals, and ignores the nLDRQ signal.
   b) The LPC47S42x ignores nLFRAME, tristate the LAD[3:0] pins and drive the nLDRQ signal inactive (high).

LPC Transfers

Wait State Requirements

I/O Transfers
The LPC47S42x inserts three wait states for an I/O read and two wait states for an I/O write cycle. A SYNC of 0110 is used for all I/O transfers. The exception to this is for transfers where IOCHRDY would normally be deasserted in an ISA transfer (i.e., EPP) in which case the sync pattern of 0110 is used and a large number of syncs may be inserted (up to 330 which corresponds to a timeout of 10us).

DMA Transfers
The LPC47S42x inserts three wait states for a DMA read and four wait states for a DMA write cycle. A SYNC of 0101 is used for all DMA transfers.

Refer to example timing for the LPC cycles in the “Timing Diagrams” section.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC is compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

FDC Internal Registers

The Floppy Disk Controller contains eight internal registers that facilitate the interfacing between the host microprocessor and the disk drive. Table 2 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the description assumes that the primary addresses have been selected.

Table 2 - Status, Data and Control Registers
(Shown with base addresses of 3F0 and 370)

PRIMARY ADDRESS	SECONDARY ADDRESS	R/W	REGISTER
3F0	370	R	Status Register A (SRA)
3F1	371	R	Status Register B (SRB)
3F2	372	R/W	Digital Output Register (DOR)
3F3	373	R/W	Tape Drive Register (TDR)
3F4	374	R	Main Status Register (MSR)
3F4	374	W	Data Rate Select Register (DSR)
3F5	375	R/W	Data (FIFO)
3F6	376		Reserved
3F7	377	R	Digital Input Register (DIR)
3F7	377	W	Configuration Control Register (CCR)

Status Register A (SRA)

Address 3F0 READ ONLY
This register is read-only and monitors the state of the internal interrupt signal and several disk interface pins in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET COND.	0	1	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION
Active high status indicating the direction of head movement. A logic "1" indicates inward direction; a logic "0" indicates outward direction.

BIT 1 nWRITE PROTECT
Active low status of the WRITE PROTECT disk interface input. A logic "0" indicates that the disk is write protected.

BIT 2 nINDEX
Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT
Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

BIT 4 nTRACK 0
Active low status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the STEP output disk interface output pin.

BIT 6 nDRV2
This function is not supported. This bit is always read as “1”.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 nDIRECTION
Active low status indicating the direction of head movement. A logic "0" indicates inward direction; a logic "1" indicates outward direction.

BIT 1 WRITE PROTECT
Active high status of the WRITE PROTECT disk interface input. A logic "1" indicates that the disk is write protected.

BIT 2 INDEX
Active high status of the INDEX disk interface input.

BIT 3 nHEAD SELECT
Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

BIT 4 TRACK 0
Active high status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST
Active high status of the DMA request pending.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt.

Status Register B (SRB)

Address 3F1 READ ONLY
This register is read-only and monitors the state of several disk interface pins in PS/2 and model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F1.

PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

BIT 0 MOTOR ENABLE 0
Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 1 MOTOR ENABLE 1
Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 2 WRITE GATE
Active high status of the WGATE disk interface output.

BIT 3 READ DATA TOGGLE
Every inactive edge of the RDATA input causes this bit to change state.

BIT 4 WRITE DATA TOGGLE
Every inactive edge of the WDATA input causes this bit to change state.

BIT 5 DRIVE SELECT 0
Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset and it is unaffected by a software reset.

BIT 6 RESERVED
Always read as a logic "1".

BIT 7 RESERVED
Always read as a logic "1".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

BIT 0 nDRIVE SELECT 2
The DS2 disk interface is not supported.

BIT 1 nDRIVE SELECT 3
The DS3 disk interface is not supported.

BIT 2 WRITE GATE
Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

BIT 3 READ DATA
Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

BIT 4 WRITE DATA
Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

BIT 5 nDRIVE SELECT 0
Active low status of the DS0 disk interface output.

BIT 6 nDRIVE SELECT 1
Active low status of the DS1 disk interface output.

BIT 7 nDRV2
Active low status of the DRV2 disk interface input. Note: This function is not supported.
Digital Output Register (DOR)

Address 3F2 READ/WRITE
The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT
These two bits are binary encoded for the drive selects, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET
A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN
PC/AT and Model 30 Mode:
Writing this bit to logic "1" will enable the DMA and interrupt functions. This bit being a logic "0" will disable the DMA and interrupt functions. This bit is a logic "0" after a reset and in these modes.

PS/2 Mode: In this mode the DMA and interrupt functions are always enabled. During a reset, this bit will be cleared to a logic "0".

BIT 4 MOTOR ENABLE 0
This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 5 MOTOR ENABLE 1
This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 6 MOTOR ENABLE 2
The MTR2 disk interface output is not supported.

BIT 7 MOTOR ENABLE 3
The MTR3 disk interface output is not supported.

DRIVE	DOR VALUE
0	1CH
1	2DH

Tape Drive Register (TDR)

Address 3F3 READ/WRITE

The Tape Drive Register (TDR) is included for 82077 software compatibility and allows the user to assign tape support to a particular drive during initialization. Any future references to that drive automatically invokes tape support. The TDR Tape Select bits TDR.[1:0] determine the tape drive number. Table 3 illustrates the Tape Select Bit encoding. Note that drive 0 is the boot device and cannot be assigned tape support. The remaining Tape Drive Register bits TDR.[7:2] are tristated when read. The TDR is unaffected by a software reset.

Table 3 - Tape Select Bits

TAPE SEL1 (TDR.1)	TAPE SEL0 (TDR.0)	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

Table 4 - Internal 2 Drive Decode - Normal

DIGITAL OUTPUT REGISTER				DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	1	0	0	1	0	nBIT 5	nBIT 4
1	X	0	1	0	1	nBIT 5	nBIT 4
0	0	X	X	1	1	nBIT 5	nBIT 4

Table 5 - Internal 2 Drive Decode - Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER				DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	1	0	0	0	1	nBIT 4	nBIT 5
1	X	0	1	1	0	nBIT 4	nBIT 5
0	0	X	X	1	1	nBIT 4	nBIT 5

Normal Floppy Mode

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 - 7 are '0'.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	0	0	0	0	0	0	tape sel1	tape sel0

Enhanced Floppy Mode 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Reserved	Reserved	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

Table 6 - Drive Type ID

DIGITAL OUTPUT REGISTER		REGISTER 3F3 - DRIVE TYPE ID	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	L0-CRF2 - B1	L0-CRF2 - B0
0	1	L0-CRF2 - B3	L0-CRF2 - B2
1	0	L0-CRF2 - B5	L0-CRF2 - B4
1	1	L0-CRF2 - B7	L0-CRF2 - B6

Note: L0-CRF2-Bx = Logical Device 0, Configuration Register F2, Bit x.

Data Rate Select Register (DSR)

Address 3F4 WRITE ONLY

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30 applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

BIT 0 and 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 through 4 PRECOMPENSATION SELECT
These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 7 shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. This starting track number can be changed by the configure command.

BIT 5 UNDEFINED
Should be written as a logic "0".

BIT 6 LOW POWER
A logic "1" written to this bit will put the floppy controller into manual low power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET
This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

Note: The DSR is Shadowed in the Floppy Data Rate Select Shadow Register, located at the offset 0x1F in the runtime register block.

Table 7 - Precompensation Delays

PRECOMP 432	PRECOMPENSATION DELAY (nsec)	
	<2Mbps	2Mbps
111	0.00	0
001	41.67	20.8
010	83.34	41.7
011	125.00	62.5
100	166.67	83.3
101	208.33	104.2
110	250.00	125
000	Default	Default

Default: See Table 10

Table 8 - Data Rates

DRIVE RATE		DATA RATE		DATA RATE		DENSEL	DRATE(1)	
DRT1	DRT0	SEL1	SEL0	MFM	FM		1	0
0	0	1	1	1Meg	---	1	1	1
0	0	0	0	500	250	1	0	0
0	0	0	1	300	150	0	0	1
0	0	1	0	250	125	0	1	0
0	1	1	1	1Meg	---	1	1	1
0	1	0	0	500	250	1	0	0
0	1	0	1	500	250	0	0	1
0	1	1	0	250	125	0	1	0
1	0	1	1	1Meg	---	1	1	1
1	0	0	0	500	250	1	0	0
1	0	0	1	2Meg	---	0	0	1
1	0	1	0	250	125	0	1	0

Drive Rate Table (Recommended) 00 = 360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
01 = 3-Mode Drive
10 = 2 Meg Tape

Note 1: The DRATE and DENSEL values are mapped onto the DRVDEN pins.

Table 9 - DRVDEN Mapping0

DT1	DT0	DRVDEN1 (1)	DRVDEN0 (1)	DRIVE TYPE
0	0	DRATE0	DENSEL	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
1	0	DRATE0	DRATE1	
0	1	DRATE0	nDENSEL	PS/2
1	1	DRATE1	DRATE0	

Table 10 - Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

Main Status Register

Address 3F4 READ ONLY
The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. No delay is required when reading the MSR after a data transfer.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	Reserved	Reserved	DRV1 BUSY	DRV0 BUSY

BIT 0 - 1 DRV x BUSY
These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY
This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

BIT 5 NON-DMA
This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

BIT 6 DIO
Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

BIT 7 RQM
Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

Data Register (FIFO)

Address 3F5 READ/WRITE
All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 11 gives several examples of the delays with a FIFO.

The data is based upon the following formula:

$$\text{Threshold \#} \times \frac{1}{\text{DATA RATE}} \times 8 - 1.5\ \mu s = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters are sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 11 - FIFO Service Delay

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 2 Mbps DATA RATE
1 byte	1 x 4 µs - 1.5 µs = 2.5 µs
2 bytes	2 x 4 µs - 1.5 µs = 6.5 µs
8 bytes	8 x 4 µs - 1.5 µs = 30.5 µs
15 bytes	15 x 4 µs - 1.5 µs = 58.5 µs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE
1 byte	1 x 8 µs - 1.5 µs = 6.5 µs
2 bytes	2 x 8 µs - 1.5 µs = 14.5 µs
8 bytes	8 x 8 µs - 1.5 µs = 62.5 µs
15 bytes	15 x 8 µs - 1.5 µs = 118.5 µs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE
1 byte	1 x 16 µs - 1.5 µs = 14.5 µs
2 bytes	2 x 16 µs - 1.5 µs = 30.5 µs
8 bytes	8 x 16 µs - 1.5 µs = 126.5 µs
15 bytes	15 x 16 µs - 1.5 µs = 238.5 µs

Digital Input Register (DIR)

Address 3F7 READ ONLY
This register is read-only in all modes.

PC-AT Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	0	0	0	0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 - 6 UNDEFINED
The data bus outputs D0 - 6 are read as '0'.

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see Runtime Register at offset 0x1E).

PS/2 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	nHIGH nDENS
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

BIT 0 nHIGH DENS
This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

BITS 1 - 2 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BITS 3 - 6 UNDEFINED
Always read as a logic "1"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see Runtime Register at offset 0x1E).

Model 30 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	0	0	0	0	0	1	0

BITS 0 - 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 NOPREC
This bit reflects the value of NOPREC bit set in the CCR register.

BIT 3 DMAEN
This bit reflects the value of DMAEN bit set in the DOR register bit 3.

BITS 4 - 6 UNDEFINED
Always read as a logic "0"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see Runtime Register at offset 0x1E).

Configuration Control Register (CCR)

Address 3F7 WRITE ONLY
PC/AT and PS/2 Modes

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 8 for the appropriate values.

BIT 2 - 7 RESERVED
Should be set to a logical "0".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	0	0	0	0	0	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 8 for the appropriate values.

BIT 2 NO PRECOMPENSATION
This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

BIT 3 - 7 RESERVED
Should be set to a logical "0"

Table 9 shows the state of the DENSEL pin. The DENSEL pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

Status Register Encoding

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 12 - Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 13 - Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writeable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the nINDEX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

Table 14 - Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: Read Data command - the FDC encountered a deleted data address mark. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 15- Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WRTPRT pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

RESET

There are three sources of system reset on the FDC: the nPCI_RESET pin, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a nPCI_RESET, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

nPCI_RESET Pin (Hardware Reset)
The nPCI_RESET pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset (Software Reset)
These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

MODES OF OPERATION
The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of the Interface Mode bits in LD0-CRF0[3,2].

PC/AT mode
The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is an active high signal.

PS/2 mode
This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the DOR becomes a "don't care". The DMA and interrupt functions are always enabled, and DENSEL is active low.

Model 30 mode
This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is active low.

DMA Transfers
DMA transfers are enabled with the Specify command and are initiated by the FDC by activating a DMA request cycle. DMA read, write and verify cycles are supported. The FDC supports two DMA transfer modes: single Transfer and Burst Transfer. Burst mode is enabled via Logical Device 0-CRF0-Bit[1] (LD0-CRF0[1]).

Controller Phases
For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

Command Phase
After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to Table 16 for the command set descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0" and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the "Invalid Command" condition.

Execution Phase
All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by a read/write or DMA cycle depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode - Transfers from the FIFO to the Host

The interrupt and RQM bit in the Main Status Register are activated when the FIFO contains (16-<threshold>) bytes or the last bytes of a full sector have been placed in the FIFO. The interrupt can be used for interrupt-driven systems, and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The FDC will deactivate the interrupt and RQM bit when the FIFO becomes empty.

Non-DMA Mode - Transfers from the Host to the FIFO

The interrupt and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The interrupt and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The FDC enters the result phase after the last byte is taken by the FDC from the FIFO (i.e. FIFO empty condition).

DMA Mode - Transfers from the FIFO to the Host

The FDC generates a DMA request cycle when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller responds to the request by reading data from the FIFO. The FDC will deactivate the DMA request when the FIFO becomes empty by generating the proper sync for the data transfer.

DMA Mode - Transfers from the Host to the FIFO.

The FDC generates a DMA request cycle when entering the execution phase of the data transfer commands. The DMA controller responds by placing data in the FIFO. The DMA request remains active until the FIFO becomes full. The DMA request cycle is reasserted when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will terminate the DMA cycle after a TC, indicating that no more data is required.

Data Transfer Termination
The FDC supports terminal count explicitly through the TC cycle and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a TC cycle was received. The only difference between these implicit functions and TC cycle is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

Result Phase
The generation of the interrupt determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

Command Set/Descriptions

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 16 for explanations of the various symbols used. Table 17 lists the required parameters and the results associated with each command that the FDC is capable of performing.

Table 16 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
C	Cylinder Address	The currently selected address; 0 to 255.
D	Data Pattern	The pattern to be written in each sector data field during formatting.
D0, D1	Drive Select 0-1	Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.
DIR	Direction Control	If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.
DS0, DS1	Disk Drive Select	DS1 DS0 DRIVE 0 0 Drive 0 0 1 Drive 1
DTL	Special Sector Size	By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EC	Enable Count	When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).
EFIFO	Enable FIFO	This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).
EIS	Enable Implied Seek	When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.
EOT	End of Track	The final sector number of the current track.
GAP		Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap Length	The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head Address	Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head Load Time	The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset". (A reset caused by writing to the appropriate bits of either the DSR or DOR)
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.

Table 16 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive. **N SECTOR SIZE** 00 128 Bytes 01 256 Bytes 02 512 Bytes 03 1024 Bytes … … 07 16K Bytes
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	When set to 1, indicates that the FDC is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the FDC operates in DMA mode.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW id defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set.

Table 16 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

Instruction Set

Table 17 - Instruction Set

READ DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W			C						Sector ID information prior to Command execution.
	W			H						
	W			R						
	W			N						
	W			EOT						
	W			GPL						
	W			DTL						
Execution										Data transfer between the FDD and system.
Result	R			ST0						Status information after Command execution.
	R			ST1						
	R			ST2						
	R			C						Sector ID information after Command execution.
	R			H						
	R			R						
	R			N						

READ DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W			C						Sector ID information prior to Command execution.
	W			H						
	W			R						
	W			N						
	W			EOT						
	W			GPL						
	W			DTL						
Execution										Data transfer between the FDD and system.
Result	R			ST0						Status information after Command execution.
	R			ST1						
	R			ST2						
	R			C						Sector ID information after Command execution.
	R			H						
	R			R						
	R			N						

WRITE DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W			C						Sector ID information prior to Command execution.
	W			H						
	W			R						
	W			N						
	W			EOT						
	W			GPL						
	W			DTL						
Execution										Data transfer between the FDD and system.
Result	R			ST0						Status information after Command execution.
	R			ST1						
	R			ST2						
	R			C						Sector ID information after Command execution.
	R			H						
	R			R						
	R			N						

WRITE DELETED DATA									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERIFY									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL/SC								
Execution										No data transfer takes place.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERSION									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

FORMAT A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W			N						Bytes/Sector
	W			SC						Sectors/Cylinder
	W			GPL						Gap 3
	W			D						Filler Byte
Execution for Each Sector Repeat:	W			C						Input Sector Parameters
	W			H						
	W			R						
	W			N						
										FDC formats an entire cylinder
Result	R			ST0						Status information after Command execution
	R			ST1						
	R			ST2						
	R			Undefined						
	R			Undefined						
	R			Undefined						
	R			Undefined						

RECALIBRATE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R			ST0						Status information at the end of each seek operation.
	R			PCN						

SPECIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W		SRT				HUT			
	W			HLT					ND	

SENSE DRIVE STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	ST3								Status information about FDD

SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	NCN								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	FIFOTHR				
Execution	W	PRETRK								

RELATIVE SEEK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	RCN								

DUMPREG										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT				HUT				
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL	FIFOTHR				
	R	PRETRK								

READ ID									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R			ST0						Status information after Command execution.
	R					ST1				
	R					ST2				
	R					C				
	R					H				
	R					R				
	R					N				

PERPENDICULAR MODE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	Invalid Codes								Invalid Command Codes (NoOp - FDC goes into Stand-by State)
Result	R	ST0								ST0 = 80H

LOCK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

Note: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

Data Transfer Commands
All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it is reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

Read Data
A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of the TC cycle, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see Table 18 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 18 - Sector Sizes

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 19.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. Table 21 describes the effect of the SK bit on the Read Data command execution and results. Except where noted in Table 20, the C or R value of the sector address is automatically incremented (see Table 22).

Table 19 - Effects of MT and N Bits

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

Table 20 - Skip Bit vs Read Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination.
0	Deleted Data	Yes	Yes	Address not incremented. Next sector not searched for.
1	Normal Data	Yes	No	Normal termination.
1	Deleted Data	No	Yes	Normal termination. Sector not read ("skipped").

Read Deleted Data
This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 21 describes the effect of the SK bit on the Read Deleted Data command execution and results.

Except where noted in Table 21, the C or R value of the sector address is automatically incremented (see Table 22).

Table 21 - Skip Bit vs. Read Deleted Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for.
0	Deleted Data	Yes	No	Normal termination.
1	Normal Data	No	Yes	Normal termination. Sector not read ("skipped").
1	Deleted Data	Yes	No	Normal termination.

Read A Track
This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the nINDEX pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a “1” if there no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the nINDEX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 22 - Result Phase

MT	HEAD	FINAL SECTOR TRANSFERRED TO HOST	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

Write Data
After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros. The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

Transfer Capacity
EN (End of Cylinder) bit
ND (No Data) bit
Head Load, Unload Time Interval
ID information when the host terminates the command

Definition of DTL when N = 0 and when N does not = 0

Write Deleted Data
This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

Verify

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, the TC cycle cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to Table 22 and Table 23 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 23 - Verify Command Result Phase

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT ≤ # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

Note: If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

Format A Track

The Format command allows an entire track to be formatted. After a pulse from the nINDEX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the nINDEX pin again and it terminates the command.

Table 24 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a 80x 4E	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		C Y L	H D	S E C	N O	C R C	GAP2 22x 4E	SYNC 12x 00	DATA AM		DATA	C R C	GAP3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a 40x FF	SYNC 6x 00	IAM	GAP1 26x FF	SYNC 6x 00	IDAM	C Y L	H D	S E C	N O	C R C	GAP2 11x FF	SYNC 6x 00	DATA AM	DATA	C R C	GAP3	GAP 4b
		FC			FE								FB or F8				

PERPENDICULAR FORMAT

GAP4a 80x 4E	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		C Y L	H D	S E C	N O	C R C	GAP2 41x 4E	SYNC 12x 00	DATA AM		DATA	C R C	GAP3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

Table 24 - Typical Values for Formatting

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.
GPL2 = suggested GPL value in Format A Track command.
*PC/AT values (typical)
**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.
NOTE: All values except sector size are in hex.

Control Commands

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

Read ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the nINDEX pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

Recalibrate

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the nTRK0 pin from the FDD. As long as the nTRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the nTRK0 pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the nTRK0 pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once. Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

Seek

The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in) and issues step pulses.
PCN > NCN: Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated. During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) Seek command - Step to the proper track
2) Sense Interrupt Status command - Terminate the Seek command
3) Read ID - Verify head is on proper track
4) Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command is issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Track command
   g. Write Deleted Data command
   h. Verify command
2. End of Seek, Relative Seek, or Recalibrate command
3. FDC requires a data transfer during the execution phase in the non-DMA mode

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

Table 25 - Interrupt Identification

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

Sense Drive Status
Sense Drive Status obtains drive status information. It has not execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

Specify
The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in Table 26. The values are the same for MFM and FM.

The choice of DMA or non-DMA operations is made by the ND bit. When this bit is "1", the non-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signaled by the DMA request cycles. Non-DMA mode uses the RQM bit and the interrupt to signal data transfers.

Configure
The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Table 26 - Drive Control Delays (ms)

	HUT					SRT				
	2M	**1M**	**500K**	**300K**	**250K**	**2M**	**1M**	**500K**	**300K**	**250K**
0	64	128	256	426	512	4	8	16	26.7	32
1	4	8	16	26.7	32	3.75	7.5	15	25	30
..	..	..	..	..	..	..	..	..	..	..
E	56	112	224	373	448	0.5	1	2	3.33	4
F	60	120	240	400	480	0.25	0.5	1	1.67	2

	HLT				
	2M	**1M**	**500K**	**300K**	**250K**
00	64	128	256	426	512
01	0.5	1	2	3.3	4
02	1	2	4	6.7	8
..	..	..	..	..	.
7F	63	126	252	420	504
7F	63.5	127	254	423	508

Configure Default Values:

EIS - No Implied Seeks
EFIFO - FIFO Disabled
POLL - Polling Enabled
FIFOTHR - FIFO Threshold Set to 1 Byte
PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

Version
The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

Relative Seek
The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

DIR	ACTION
0	Step Head Out
1	Step Head In

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 79 due to its limitation of issuing a maximum of 80 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

Perpendicular Mode

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 27 describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The format field shown on Page 58 illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, and approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP =0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This enhancement allows data transfers between Conventional and Perpendicular drives without having to issue Perpendicular mode commands between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1. The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
2. The write pre-compensation given to a perpendicular mode drive will be 0ns.
3. For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a "1".If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

1. "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.
2. "Hardware" resets will clear all bits (GAP, WGATE and D0-D3) to "0", i.e all conventional mode.

Table 27 - Effects of WGATE and GAP Bits

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

LOCK

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the nPCI_RESET pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to their default values. A status byte is returned immediately after issuing a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

Enhanced DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

Compatibility
The LPC47S42x was designed with software compatibility in mind. It is a fully backwards- compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system BIOS.

Direct Support for Two Floppy Drives
The nMTR1 function is on pin 43. nMTR1 is the second alternate function on the GP22 pin. Pin 43 has the IO12 buffer type.

The nMTR1 function is selectable as open drain or push pull as nMTR0 is through bit 6 of the FDD Mode Register in CRF0 of LD 0. This overrides the selection of the output type through bit 7 of the GPIO control register. It is also controlled by bit 7 of the FDD Mode Register.

The nDS1 function is on pin 41. nDS1 is the second alternate function on the GP20 pin. Pin 41 has IO12 buffer type.

The nDS1 function is selectable as open drain or push pull as nDS0 is through bit 6 of the FDD Mode Register in CRF0 of LD 0. This overrides the selection of the output type through bit 7 of the GPIO control register. It is also controlled by bit 7 of the FDD Mode register.

See the Runtime Registers section for register information.

Disk Change Support for Second Floppy
Bit[1] in the Force Disk Change register supports the second floppy. Setting either of the Force Disk Change bits active forces the internal FDD nDSKCHG active when the appropriate drive has been selected. The Force Disk Change register is defined in the Runtime Registers section.

Force Write Protect Support for Second Floppy
Bit[0] in the Device Disable register and FDD Option register support floppy write protect.

See the Runtime Registers section for Device Disable register description and the Configuration Registers section for FDD Option register description.

SERIAL PORT (UART)

The LPC47S42x incorporates two full function UARTs. They are compatible with the NS16450, the 16450 ACE registers and the NS16C550A. The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt. The second UART also supports IrDA 1.0, HP-SIR, ASK-IR infrared modes of operation.

Note: The UARTs 1 and 2 may be configured to share an interrupt. Refer to the Configuration section for more information.

Register Description
Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The LPC47S42x contains two serial ports, each of which contain a register set as described below.

Table 28 - Addressing the Serial Port

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

*Note: DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

Receive Buffer Register (RB)

Address Offset = 0H, DLAB = 0, READ ONLY
This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

Transmit Buffer Register (TB)
Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.
Interrupt Enable Register (IER)
Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the LPC47S42x. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0
This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1
This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2
This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3
This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7
These bits are always logic "0".

FIFO Control Register (FCR)
Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported. The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (runtime register at offset 0x20) and UART2 FIFO Control Shadow Register (runtime register at offset 0x1D).

Bit 0
Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1
Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2
Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3
Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Bit 4,5
Reserved

Bit 6,7
These bits are used to set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

Interrupt Identification Register (IIR)
Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:
1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0
This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2
These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bit 3
In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5
These bits of the IIR are always logic "0".

Bits 6 and 7
These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

Table 29 - Interrupt Control

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Line Control Register (LCR)
Address Offset = 3H, DLAB = 0, READ/WRITE

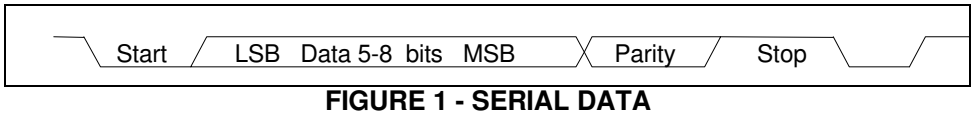


FIGURE 1 - SERIAL DATA

This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1
These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:
The Start, Stop and Parity bits are not included in the word length.

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2
This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3
Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4
Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5
Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 6
Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7
Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

Modem Control Register (MCR)
Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0
This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

Bit 1
This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2
This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3
Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4
This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State (logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7
These bits are permanently set to logic zero.

Line Status Register (LSR)
Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0
Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1
Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrunn error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2
Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3
Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4
Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5
Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6
Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty.

Bit 7
This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

Modem Status Register (MSR)
Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0
Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1
Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2
Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3
Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4
This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

Bit 5
This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6
This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7
This bit is the complement of the Data Carrier
Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

Scratchpad Register (SCR)
Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Programmable Baud Rate Generator (AND Divisor Latches DLH, DLL)
The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal PLL clock by any divisor from 1 to 65535. The internal PLL clock is divided down to generate a 1.8462MHz frequency for Baud Rates less than 38.4k, a 1.8432MHz frequency for 115.2k, a 3.6864MHz frequency for 230.4k and a 7.3728MHz frequency for 460.8k. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

Table 30 shows the baud rates possible.

Effect Of The Reset on Register File
The Reset Function Table (Table 31) details the effect of the Reset input on each of the registers of the Serial Port.

FIFO Interrupt Mode Operation
When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

A. The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
B. The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
D. The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

A. A FIFO timeout interrupt occurs if all the following conditions exist:
   - At least one character is in the FIFO.
   - The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay).
   - The most recent CPU read of the FIFO was longer than 4 continuous character times ago.
   - This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.
B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).
C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

A. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Operation
With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

- Bit 0=1 as long as there is one byte in the RCVR FIFO.
- Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.
- Bit 5 indicates when the XMIT FIFO is empty.
- Bit 6 indicates that both the XMIT FIFO and shift register are empty.
- Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 30 - Baud Rates

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL[1]	HIGH SPEED BIT[2]
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note[1]: The percentage error for all baud rates, except where indicated otherwise, is 0.2%.
Note [2]: The High Speed bit is located in the Device Configuration Space.

Table 31 - Reset Function

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low

Table 32 - Register Summary for an Individual UART Channel

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit
ADDR = 2	FIFO Control Register (Write Only)	FCR (Note 7)	FIFO Enable	RCVR FIFO Reset
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).
Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Table 32 - Register Summary for an Individual UART Channel (continued)

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
Interrupt ID Bit	Interrupt ID Bit (Note 5)	0	0	FIFOs Enabled (Note 5)	FIFOs Enabled (Note 5)
XMIT FIFO Reset	DMA Mode Select (Note 6)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
OUT1 (Note 3)	OUT2 (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	Error in RCVR FIFO (Note 5)
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.
Note 7: The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (runtime register at offset 0x20) and UART2 FIFO Control Shadow Register (runtime register at offset 0x1D).

Notes On Serial Port Operation

FIFO Mode Operation

GENERAL
The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

TX AND RX FIFO Operation
The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. **The UART will prevent loads to the Tx FIFO if it currently holds 16 characters.** Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. **Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have the Tx FIFO empties after this condition, the Tx been loaded into the FIFO, concurrently. When interrupt will be activated without a one character delay.**

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. **To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.**

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

INFRARED INTERFACE

The infrared interface provides a two-way wireless communications port using infrared as a transmission medium. Several IR implementations have been provided for the second UART in this chip (logical device 5), IrDA, and Amplitude Shift Keyed IR. The IR transmission can use the standard UART2 TXD2 and RXD2 pins. These can be selected through the configuration registers.

IrDA 1.0 allows serial communication at baud rates up to 115.2 kbps. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a single IR pulse at the beginning of the serial bit time. A one is signaled by sending no IR pulse during the bit time. Please refer to the AC timing for the parameters of these pulses and the IrDA waveform.

The Amplitude Shift Keyed IR allows asynchronous serial communication at baud rates up to 19.2K Baud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a 500KHz waveform for the duration of the serial bit time. A one is signaled by sending no transmission during the bit time. Please refer to the AC timing for the parameters of the ASK-IR waveform.

If the Half Duplex option is chosen, there is a time-out when the direction of the transmission is changed. This time-out starts at the last bit transferred during a transmission and blocks the receiver input until the timeout expires. If the transmit buffer is loaded with more data before the time-out expires, the timer is restarted after the new byte is transmitted. If data is loaded into the transmit buffer while a character is being received, the transmission will not start until the time-out expires after the last receive bit has been received. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The IR half duplex time-out is programmable via CRF2 in Logical Device 5. This register allows the time-out to be programmed to any value between 0 and 10msec in 100usec increments.

Figure 2 shows the block diagram of the IR components in the LPC47S42x:

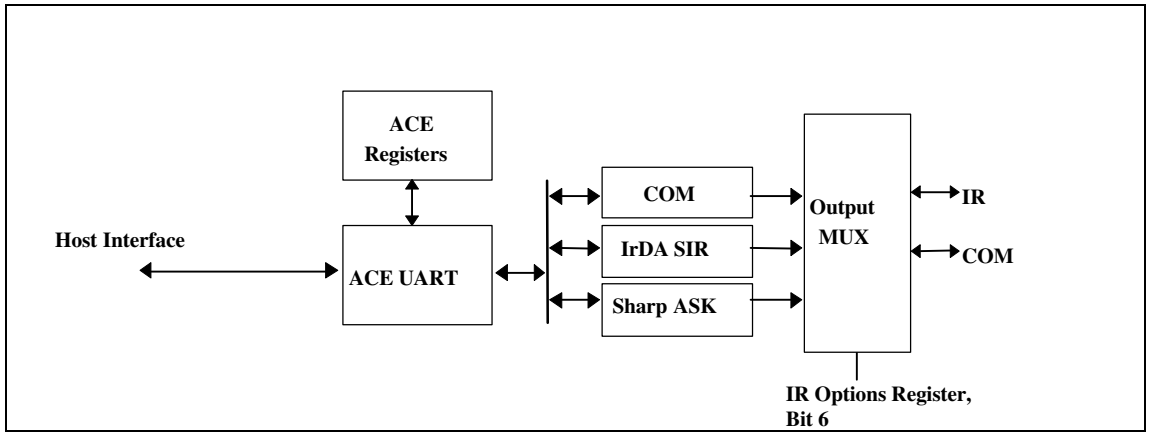


FIGURE 2

IR Transmit Pin
The following description pertains to the IRTX pin of the LPC47S42x.

Following a VTR POR, the IRTX pin will be output and low. It will remain low until one of the following conditions are met:

GP53/TXD2/IRTX Pin. This pin defaults to the GPIO function.

1. This pin will remain low following a VCC POR until the IRTX function is selected for the pin AND serial port 2 is enabled by setting the activate bit, at which time the pin will reflect the state of the IR transmit output of the IR block (if IR is enabled through the IR options Register for Serial Port 2).
2. This pin will remain low following a VCC POR until the TXD2 function is selected for the pin AND serial port 2 is enabled by setting the activate bit, at which the pin will reflect the state of the transmit output of serial port 2.
3. This pin will remain low following a VCC POR until the corresponding GPIO data bit (GP5 register bit 3) is set or the polarity bit in the GP53 control register is set.

PARALLEL PORT

The LPC47S42x incorporates an IBM XT/AT compatible parallel port. This supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Refer to the Configuration Registers for information on disabling, power down, changing the base address of the parallel port, and selecting the mode of operation.

The LPC47S42x also provides a mode for support of the floppy disk controller on the parallel port.

The parallel port also incorporates SMSC's ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports, with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map of the Parallel Port is shown below

DATA PORT	BASE ADDRESS + 00H
STATUS PORT	BASE ADDRESS + 01H
CONTROL PORT	BASE ADDRESS + 02H
EPP ADDR PORT	BASE ADDRESS + 03H
EPP DATA PORT 0	BASE ADDRESS + 04H
EPP DATA PORT 1	BASE ADDRESS + 05H
EPP DATA PORT 2	BASE ADDRESS + 06H
EPP DATA PORT 3	BASE ADDRESS + 07H

The bit map of these registers is:

	D0	D1	D2	D3	D4	D5	D6	D7	Note
DATA PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
STATUS PORT	TMOUT	0	0	nERR	SLCT	PE	nACK	nBUSY	1
CONTROL PORT	STROBE	AUTOFD	nINIT	SLC	IRQE	PCD	0	0	1
EPP ADDR PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 0	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2

Note 1: These registers are available in all modes.
Note 2: These registers are only available in EPP mode.

Table 33 - Parallel Port Connector

HOST CONNECTOR	PIN NUMBER	STANDARD	EPP	ECP
1	83	nSTROBE	nWrite	nStrobe
2-9	68-75	PD<0:7>	PData<0:7>	PData<0:7>
10	80	nACK	Intr	nAck
11	79	BUSY	nWait	Busy, PeriphAck(3)
12	78	PE	(User Defined)	PError, nAckReverse(3)
13	77	SLCT	(User Defined)	Select
14	82	nALF	NDatastb	nAutoFd, HostAck(3)
15	81	nERROR	(User Defined)	nFault(1) nPeriphRequest(3)
16	66	nINIT	nRESET	nInit(1) nReverseRqst(3)
17	67	nSLCTIN	NAddrstrb	nSelectIn(1,3)

(1) = Compatible Mode
(3) = High Speed Mode

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

IBM XT/AT Compatible, Bi-Directional and EPP Modes
Data Port
ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the internal data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

Status Port
ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of a read cycle. The bits of the Status Port are defined as follows:

BIT 0 TMOUT - TIME OUT
This bit is valid in EPP mode only and indicates that a 10 usec time out has occurred on the EPP bus. A logic O means that no time out error has occurred; a logic 1 means that a time out error has been detected. This bit is cleared by a RESET. Writing a one to this bit clears the time out status bit. On a write, this bit is self clearing and does not require a write of a zero. Writing a zero to this bit has no effect.

BITS 1, 2 - are not implemented as register bits, during a read of the Printer Status Register these bits are a low level.

BIT 3 nERR - nERROR
The level on the nERROR input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

BIT 4 SLCT - PRINTER SELECTED STATUS
The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

BIT 5 PE - PAPER END
The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

BIT 6 nACK - nACKNOWLEDGE
The level on the nACK input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

BIT 7 nBUSY - nBUSY
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

Control Port
ADDRESS OFFSET = 02H

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the nAUTOFD output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT
This bit is output onto the nINIT output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT
This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going nACK input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION
Parallel Control Direction is not valid in printer mode. In printer mode, the direction is always out regardless of the state of this bit. In bi-directional, EPP or ECP mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

EPP Address Port
ADDRESS OFFSET = 03H

The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP ADDRESS WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

EPP Data Port 0
ADDRESS OFFSET = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP

DATA WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

EPP Data Port 1
ADDRESS OFFSET = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP Data Port 2
ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP Data Port 3
ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP 1.9 Operation
When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

Software Constraints
Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (i.e., a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

EPP 1.9 Write
The timing for a write operation (address or data) is shown in timing diagram EPP Write Data or Address cycle. The chip inserts wait states into the LPC I/O write cycle until it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

1. If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.

2. If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of operation

1. The host initiates an I/O write cycle to the selected EPP register.
2. If WAIT is not asserted, the chip must wait until WAIT is asserted.
3. The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.
6. a. The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.
   b. The chip latches the data from the internal data bus for the PData bus and drives the sync that indicates that no more wait states are required followed by the TAR to complete the write cycle.
7. Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
8. Chip may modify nWRITE and nPDATA in preparation for the next cycle.

EPP 1.9 Read

The timing for a read operation (data) is shown in timing diagram EPP Read Data cycle. The chip inserts wait states into the LPC I/O read cycle until it has been determined that the read cycle can complete. The read cycle can complete under the following circumstances:

1 If the EPP bus is not ready (nWAIT is active low) when nDATASTB goes active then the read can complete when nWAIT goes inactive high.
2. If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of WRITE or before nDATASTB goes active. The read can complete once nWAIT is determined inactive.

Read Sequence of Operation

1. The host initiates an I/O read cycle to the selected EPP register.
2. If WAIT is not asserted, the chip must wait until WAIT is asserted.
3. The chip tri-states the PData bus and deasserts nWRITE.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
5. Peripheral drives PData bus valid.
6. Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7. a) The chip latches the data from the PData bus for the internal data bus and deasserts nDATASTB or nADDRSTRB. This marks the beginning of the termination phase.
   b) The chip drives the sync that indicates that no more wait states are required and drives valid data onto the LAD[3:0] signals, followed by the TAR to complete the read cycle.
8. Peripheral tri-states the PData bus and asserts nWAIT, indicating to the host that the PData bus is tri-stated.
9. Chip may modify nWRITE, PDIR and nPDATA in preparation for the next cycle.

EPP 1.7 Operation

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle to the end of the cycle. If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

Software Constraints

Before an EPP cycle is executed, the software must ensure that the control register bits D0, D1 and D3 are set to zero. Also, bit D5 (PCD) is a logic "0" for an EPP write or a logic "1" for and EPP read.

EPP 1.7 Write

The timing for a write operation (address or data) is shown in timing diagram EPP 1.7 Write Data or Address cycle. The chip inserts wait states into the I/O write cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The write cycle can complete when nWAIT is inactive high.

Write Sequence of Operation

1. The host sets PDIR bit in the control register to a logic "0". This asserts nWRITE.
2. The host initiates an I/O write cycle to the selected EPP register.
3. The chip places address or data on PData bus.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. If nWAIT is asserted, the chip inserts wait states into I/O write cycle until the peripheral deasserts nWAIT or a time-out occurs.
6. The chip drives the final sync, deasserts nDATASTB or nADDRSTRB and latches the data from the internal data bus for the PData bus.
7. Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

EPP 1.7 Read

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. The chip inserts wait states into the I/O read cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when nWAIT is inactive high.

Read Sequence of Operation

1. The host sets PDIR bit in the control register to a logic "1". This deasserts nWRITE and tri-states the PData bus.
2. The host initiates an I/O read cycle to the selected EPP register.
3. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
4. If nWAIT is asserted, the chip inserts wait states into the I/O read cycle until the peripheral deasserts nWAIT or a time-out occurs.
5. The Peripheral drives PData bus valid.
6. The Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7. The chip drives the final sync and deasserts nDATASTB or nADDRSTRB.
8. Peripheral tri-states the PData bus.
9. Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

Table 34 - EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
nWRITE	nWrite	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP).
WAIT	nWait	I	This signal is active low. It is driven inactive as a positive acknowledgement from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
DATASTB	nData Strobe	O	This signal is active low. It is used to denote data read or write operation.
RESET	nReset	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
ADDRSTB	nAddress Strobe	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
nERR	Error	I	Same as SPP mode.

Note 1: SPP and EPP can use 1 common register.

Note 2: nWrite is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

Extended Capabilities Parallel Port
ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

High performance half-duplex forward and reverse channel Interlocked handshake, for fast reliable transfer Optional single byte RLE compression for improved throughput (64:1) Channel addressing for low-cost peripherals Maintains link and data layer separation Permits the use of active output drivers permits the use of adaptive signal timing Peer-to-peer capability.

Vocabulary
The following terms are used in this document:
assert: When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.
forward: Host to Peripheral communication.
reverse: Peripheral to Host communication
Pword: A port word; equal in size to the width of the LPC interface. For this implementation, PWord is always 8 bits.
1 A high level.
0 A low level.

These terms may be considered synonymous:

PeriphClk, nAck
HostAck, nAutoFd
PeriphAck, Busy
nPeriphRequest, nFault
nReverseRequest, nInit
nAckReverse, PError
Xflag, Select
ECPMode, nSelectIn
HostClk, nStrobe

Reference Document: IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev 1.14, July 14, 1993. This document is available from Microsoft.

The bit map of the Extended Parallel Port registers is:

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Note**
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	nBusy	nAck	PError	Select	nFault	0	0	0	1
dcr	0	0	Direction	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	Parallel Port IRQ			Parallel Port DMA			
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Note 1: These registers are available in all modes.

Note 2: All FIFOs use one common 16 byte FIFO.
Note 3: The ECP Parallel Port Config Reg B reflects the IRQ and DMA channel selected by the Configuration Registers.

ECP Implementation Standard

This specification describes the standard interface to the Extended Capabilities Port (ECP). All LPC devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

Description

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 35 - ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe	O	During write operations nStrobe registers data or address into the slave on the asserting edge (handshakes with Busy).
PData 7:0	I/O	Contains address or data or RLE data.
nAck	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with nStrobe in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with nStrobe. PeriphAck also provides command information in the reverse direction.
PError (nAckReverse)	I	Used to acknowledge a change in the direction the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. It is an "interlocked" handshake with nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with nAck in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data. The host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with nAck. HostAck also provides command information in the forward phase.
nFault (nPeriphRequest)	I	Generates an error interrupt when asserted. This signal provides a mechanism for peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
nInit	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and nSelectIn is high.
nSelectIn	O	Always deasserted in ECP mode.

Register Definitions

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr. The table below lists these dependencies. Operation of the devices in modes other that those specified is undefined.

Table 36 - ECP Register Definitions

NAME	ADDRESS (Note 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.

Note 2: All addresses are qualified with AEN. Refer to the AEN pin definition.

Table 37 - Mode Descriptions

MODE	DESCRIPTION*
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	Reserved
110	Test mode
111	Configuration mode

*Refer to ECR Register Description

Data And ecpAFifo Port
ADDRESS OFFSET = 00H

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.
Mode 011 (ECP FIFO - Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is ony defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet.

Device Status Register (DSR)
ADDRESS OFFSET = 01H
The Status Port is located at an offset of '01H' from the base address. Bits 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

BIT 3 nFault
The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

BIT 4 Select
The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

BIT 5 PError
The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

BIT 6 nAck
The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.
BIT 7 nBusy
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

Device Control Register (DCR)
ADDRESS OFFSET = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the nAUTOFD output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT
This bit is output onto the nINIT output without inversion.

BIT 3 SELECTIN
This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 ackIntEn - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the nACK input. Refer to the description of the interrupt under Operation, Interrupts.

BIT 5 DIRECTION
If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

BITS 6 and 7 during a read are a low level, and cannot be written.

cFifo (Parallel Port Data FIFO)
ADDRESS OFFSET = 400h
Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ecpDFifo (ECP Data FIFO)
ADDRESS OFFSET = 400H
Mode = 011

Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

tFifo (Test FIFO Mode)
ADDRESS OFFSET = 400H
Mode = 110

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

cnfgA (Configuration Register A)
ADDRESS OFFSET = 400H
Mode = 111
This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord = 1 byte)
cnfgB (Configuration Register B)
ADDRESS OFFSET = 401H
Mode = 111

BIT 7 compress
This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression!
BIT 6 intrValue
Returns the value of the interrupt to determine possible conflicts.

BITS [5:3] Parallel Port IRQ (read-only)
Refer to Table 38B.

BITS [2:0] Parallel Port DMA (read-only)
Refer to Table 38C.

ecr (Extended Control Register)
ADDRESS OFFSET = 402H
Mode = all
This register controls the extended ECP parallel port functions.

BITS 7,6,5
These bits are Read/Write and select the Mode.

BIT 4 nErrIntrEn
Read/Write (Valid only in ECP Mode)
1: Disables the interrupt generated on the asserting edge of nFault.
0: Enables an interrupt pulse on the high to low edge of nFault. Note that an interrupt will be generated if nFault is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn
Read/Write
1: Enables DMA (DMA starts when serviceIntr is 0).
0: Disables DMA unconditionally.

BIT 2 serviceIntr
Read/Write
1: Disables DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a 1 by hardware. It must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.
case dmaEn=1:
During DMA (this bit is set to a 1 when terminal count is reached).
case dmaEn=0 direction=0:
This bit shall be set to 1 whenever there are writeIntrThreshold or more bytes free in the FIFO.
case dmaEn=0 direction=1:
This bit shall be set to 1 whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.
BIT 1 full
Read only
1: The FIFO cannot accept another byte or the FIFO is completely full.
0: The FIFO has at least 1 free byte.

BIT 0 empty
Read only
1: The FIFO is completely empty.
0: The FIFO contains at least 1 byte of data.

Table 38A - Extended Control Register

R/W	MODE
000:	Standard Parallel Port Mode . In this mode the FIFO is reset and common collector drivers are used on the control lines (nStrobe, nAutoFd, nInit and nSelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port Mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO Mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register L3-CRF0. All drivers have active pull-ups (push-pull).
101:	Reserved
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

Table 38B

IRQ SELECTED	CONFIG REG B BITS 5:3
15	110
14	101
11	100
10	011
9	010
7	001
5	111
All Others	000

Table 38C

DMA SELECTED	CONFIG REG B BITS 2:0
3	011
2	010
1	001
All Others	000

Operation

Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ecp reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ecp reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert nAutoFd independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

ECP Operation

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:

Set Direction = 0, enabling the drivers.
Set strobe = 0, causing the nStrobe signal to default to the deasserted state.
Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.
Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

Termination from ECP Mode
Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be transitioned into the forward direction.

Command/Data
ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8 bit data or 8 bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8 bit command is transferred when HostAck is low.

The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8 bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 39 -
Forward Channel Commands (HostAck Low)
Reverse Channel Commands (PeripAck Low)

D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

Data Compression
The ECP port supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

Pin Definition
The drivers for nStrobe, nAutoFd, nInit and nSelectIn are open-collector in mode 000 and are push-pull in all other modes.

LPC Connections
The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section). Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

Interrupts
The interrupts are enabled by serviceIntr in the ecr register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

An interrupt is generated when:
1. For DMA transfers: When serviceIntr is 0, dmaEn is 1 and the DMA TC cycle is received.
2. For Programmed I/O:
   a. When serviceIntr is 0, dmaEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.
   b. When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO.
3. When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
4. When ackIntEn is 1 and the nAck signal transitions from a low to a high.

FIFO Operation
The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or DMA cycle depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system. A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

DMA Transfers
DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by encoding the nLDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests a DMA cycle shall not be requested for more than 32 DMA cycles in a row. The FIFO is enabled directly by the host initiating a DMA cycle for the requested channel, and addresses need not be valid. An interrupt is generated when a TC cycle is received. (Note: The only way to properly terminate DMA transfers is with a TC cycle.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

DMA Mode - Transfers from the FIFO to the Host
(Note: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP requests a DMA cycle whenever there is data in the FIFO. The DMA controller responds to the request by reading data from the FIFO. The ECP stop requesting DMA cycles when the FIFO becomes empty or when a TC cycle is received, indicating that no more data is required. If the ECP stops requesting DMA cycles due to the FIFO going empty, then a DMA cycle is requested again as soon as there is one byte in the FIFO. If the ECP stops requesting DMA cycles due to the TC cycle, then a DMA cycle is requested again when there is one byte in the FIFO, and serviceIntr has been re-enabled.

Programmed I/O Mode or Non-DMA Mode
The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and serviceIntr to 0.

The ECP requests programmed I/O transfers from the host by activating the interrupt. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

Programmed I/O - Transfers from the FIFO to the Host
In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntrThreshold bytes may be read from the FIFO in a single burst.

readIntrThreshold =(16-<threshold>) data bytes in FIFO
An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is greater than or equal to (16-<threshold>). (If the threshold = 12, then the interrupt is set whenever there are 4-16 bytes in the FIFO). The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can be completely emptied in a single burst, otherwise a minimum of (16-<threshold>) bytes may be read from the FIFO in a single burst.

Programmed I/O - Transfers from the Host to the FIFO
In the forward direction an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

writeIntrThreshold = (16-<threshold>) free bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.

PARALLEL PORT FLOPPY DISK CONTROLLER
The Floppy Disk Control signals are available optionally on the parallel port pins. When this mode is selected, the parallel port is not available. There are two modes of operation, PPFD1 and PPFD2. These modes can be selected in the Parallel Port Mode Register, as defined in the Parallel Port Mode Register, Logical Device 3, at 0xF1. PPFD1 has only drive 1 on the parallel port pins; PPFD2 has drive 0 and 1 on the parallel port pins.

The following parallel port pins are read as follows by a read of the parallel port register:

1. Data Register (read) = last Data Register (write)
2. Control Register read as "cable not connected" STROBE, AUTOFD and SLC = 0 and nINIT =1
3. Status Register reads: nBUSY = 0, PE = 0, SLCT = 0, nACK = 1, nERR = 1

The following FDC pins are all in the high impedence state when the PPFDC is actually selected by the drive select register:
1. nWDATA, DENSEL, nHDSEL, nWGATE, nDIR, nSTEP, nDS1, nDS0, nMTR0, nMTR1.
2. If PPFDx is selected, then the parallel port can not be used as a parallel port until "Normal" mode is selected.

The FDC signals are muxed onto the Parallel Port pins as shown in Table 41.

For ACPI compliance the FDD pins that are multiplexed onto the Parallel Port function independently of the state of the Parallel Port controller. For example, if the FDC is enabled onto the Parallel Port the multiplexed FDD interface functions normally regardless of the Parallel Port Power control, CR22.3. Table 40 illustrates this functionality.

TABLE 40 - MODIFIED PARALLEL PORT FDD CONTROL

PARALLEL PORT POWER	PARALLEL PORT FDC CONTROL		PARALLEL PORT FDC STATE	PARALLEL PORT STATE
CR22.3	LD3:CRF1.1	LD3:CRF1.0		
1	0	0	OFF	ON
0	0	0	OFF	OFF
X	1	X	ON	OFF
	X	1		(NOTE[1])

NOTE[1]: The Parallel Port Control register reads as "Cable Not Connected" when the Parallel Port FDC is enabled; i.e., STROBE = AUTOFD = SLC = 0 and nINIT = 1.

Table 41 - FDC Parallel Port Pins

CONNECTOR PIN #	QFP CHIP PIN #	SPP MODE	PIN DIRECTION	FDC MODE	PIN DIRECTION
1	83	nSTROBE	I/O	(nDS0)	I/(O) Note1
2	68	PD0	I/O	nINDEX	I
3	69	PD1	I/O	nTRK0	I
4	70	PD2	I/O	nWP	I
5	71	PD3	I/O	nRDATA	I
6	72	PD4	I/O	nDSKCHG	I
7	73	PD5	I/O	-	-
8	74	PD6	I/O	(nMTR0)	I/(O) Note1
9	75	PD7	I/O	-	-
10	80	nACK	I	nDS1	O
11	79	BUSY	I	nMTR1	O
12	78	PE	I	nWDATA	O
13	77	SLCT	I	nWGATE	O
14	82	nALF	I/O	DRVDEN0	O
15	81	nERROR	I	nHDSEL	O
16	66	nINIT	I/O	nDIR	O
17	67	nSLCTIN	I/O	nSTEP	O

Note 1: These pins are outputs in mode PPFD2, inputs in mode PPFD1.

POWER MANAGEMENT

Power management capabilities are provided for the following logical devices: floppy disk, UART 1, UART 2 and the parallel port. For each logical device, two types of power management are provided: direct powerdown and auto powerdown.

FDC Power Management
Direct power management is controlled by CR22. Refer to CR22 for more information.

Auto Power Management is enabled by CR23-B0. When set, this bit allows FDC to enter powerdown when all of the following conditions have been met:

1. The motor enable pins of register 3F2H are inactive (zero).
2. The part must be idle; MSR=80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupts).
3. The head unload timer must have expired.
4. The Auto powerdown timer (10msec) must have timed out.

An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down when all the conditions are met.

Disabling the auto powerdown mode cancels the timer and holds the FDC block out of auto powerdown.

DSR From Powerdown
If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened from DSR powerdown, the auto powerdown will once again become effective.

Wake Up From Auto Powerdown
If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the FDC resumes operation as though it was never in powerdown. Besides activating the nPCI_RESET pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part).
2. A read from the MSR register.
3. A read or write to the Data register.

Once awake, the FDC will reinitiate the auto powerdown timer for 10 ms. The part will powerdown again when all the powerdown conditions are satisfied.

Register Behavior
Table 40 illustrates the AT and PS/2 (including Model 30) configuration registers available and the type of access permitted. In order to maintain software transparency, access to all the registers must be maintained. As Table 40 shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in the FDC description. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed.

Pin Behavior
The LPC47S42x is specifically designed for systems in which power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of the LPC47S42x can be divided into two major categories: system interface and floppy disk drive interface. The floppy disk drive pins are disabled so that no power will be drawn through the part as a result of any voltage applied to the pin within the part's power supply range. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

Table 42 - PC/AT and PS/2 Available Registers

	AVAILABLE REGISTERS		
BASE + ADDRESS	**PC-AT**	**PS/2 (MODEL 30)**	**ACCESS PERMITTED**
Access to these registers DOES NOT wake up the part			
00H	----	SRA	R
01H	----	SRB	R
02H	DOR (1)	DOR (1)	R/W
03H	---	---	---
04H	DSR (1)	DSR (1)	W
06H	---	---	---
07H	DIR	DIR	R
07H	CCR	CCR	W
Access to these registers wakes up the part			
04H	MSR	MSR	R
05H	Data	Data	R/W

Note 1: Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (via DOR or DSR reset bits) will wake up the part.

System Interface Pins
Table 43 gives the state of the interface pins in the powerdown state. Pins unaffected by the powerdown are labeled "Unchanged".

Table 43 – State of System Pins in Auto Powerdown

SYSTEM PINS	STATE IN AUTO POWERDOWN
LAD[3:0]	Unchanged
nLDRQ	Unchanged
nLPCPD	Unchanged
nLFRAME	Unchanged
nPCI_RESET	Unchanged
PCI_CLK	Unchanged
SER_IRQ	Unchanged

FDD Interface Pins
All pins in the FDD interface which can be connected directly to the floppy disk drive itself are either DISABLED or TRISTATED.

Pins used for local logic control or part programming are unaffected. Table 44 depicts the state of the floppy disk drive interface pins in the powerdown state.

Table 44 - State of Floppy Disk Drive Interface Pins in Powerdown

FDD PINS	STATE IN AUTO POWERDOWN
INPUT PINS	
nRDATA	Input
nWRTPRT	Input
nTRK0	Input
nINDEX	Input
nDSKCHG	Input
OUTPUT PINS	
nMTR0	Tristated
nDS0	Tristated
nDIR	Active
nSTEP	Active
nWDATA	Tristated
nWGATE	Tristated
nHDSEL	Active
DRVDEN[0:1]	Active

UART Power Management
Direct power management is controlled by CR22. Refer to CR22 for more information.

Auto Power Management is enabled by CR23-B4 and B5. When set, these bits allow the following auto power management operations:

1. The transmitter enters auto powerdown when the transmit buffer and shift register are empty.
2. The receiver enters powerdown when the following conditions are all met:
   A. Receive FIFO is empty
   B. The receiver is waiting for a start bit.

Note: While in powerdown the Ring Indicator interrupt is still valid and transitions when the RI input changes.

Exit Auto Powerdown
The transmitter exits powerdown on a write to the XMIT buffer. The receiver exits auto powerdown when RXDx changes state.

Parallel Port
Direct power management is controlled by CR22. Refer to CR22 for more information.

Auto Power Management is enabled by CR23-B3. When set, this bit allows the ECP or EPP logical parallel port blocks to be placed into powerdown when not being used.

The EPP logic is in powerdown under any of the following conditions:

1. EPP is not enabled in the configuration registers.
2. EPP is not selected through ecr while in ECP mode.

The ECP logic is in powerdown under any of the following conditions:

1. ECP is not enabled in the configuration registers.
2 SPP, PS/2 Parallel port or EPP mode is selected through ecr while in ECP mode.

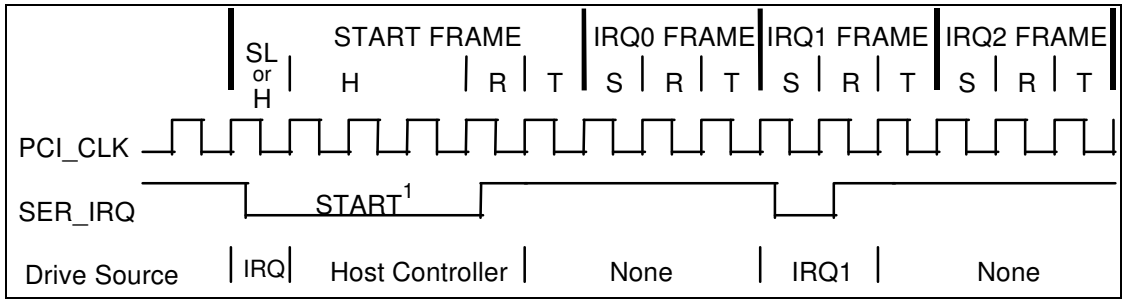
Exit Auto Powerdown
The parallel port logic can change powerdown modes when the ECP mode is changed through the ecr register or when the parallel port mode is changed through the configuration registers.

SERIAL IRQ

The LPC47S42x supports the serial interrupt to transmit interrupt information to the host system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems, Version 6.0.

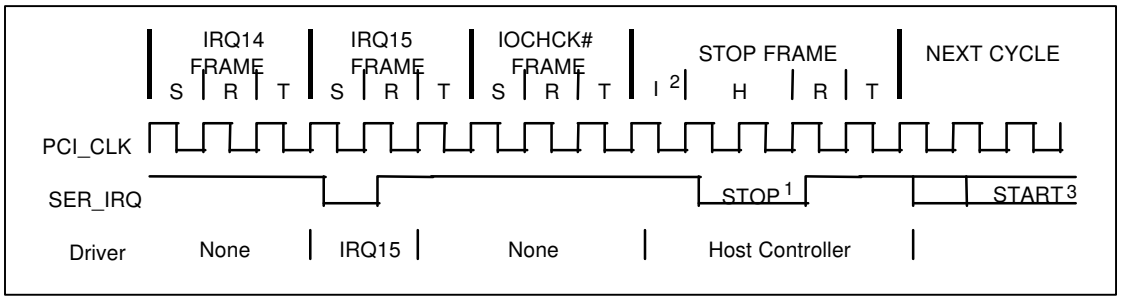
Timing Diagrams for SER_IRQ Cycle

A) Start Frame timing with source sampled a low pulse on IRQ1.



Note: H=Host Control; R=Recovery; T=Turn-Around; SL=Slave Control; S=Sample
Note 1: Start Frame pulse can be 4-8 clocks wide depending on the location of the device in the PCI bridge hierarchy in a synchronous bridge design.

B) Stop Frame Timing with Host using 17 SER_IRQ sampling period.



Note: H=Host Control; R=Recovery; T=Turn-Around; S=Sample; I=Idle
Note 1: Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
Note 2: There may be none, one or more Idle states during the Stop Frame.
Note 3: The next SER_IRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

SER_IRQ Cycle Control

There are two modes of operation for the SER_IRQ Start Frame.

1) **Quiet (Active) Mode**: Any device may initiate a Start Frame by driving the SER_IRQ low for one clock, while the SER_IRQ is Idle. After driving low for one clock the SER_IRQ is immediately tri-stated without at any time driving high. A Start Frame may not be initiated while the SER_IRQ is Active. The SER_IRQ is Idle between Stop and Start Frames. The SER_IRQ is Active between Start and Stop Frames. This mode of operation allows the SER_IRQ to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated the Host Controller will take over driving the SER_IRQ low in the next clock and will continue driving the SER_IRQ low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the Host Controller will drive the SER_IRQ back high for one clock, then tri-state.

Any SER_IRQ Device (i.e., The LPC47S42x) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the Host Controller unless the SER_IRQ is already in an SER_IRQ Cycle and the IRQ/Data transition can be delivered in that SER_IRQ Cycle.

2) **Continuous (Idle) Mode**: Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other SER_IRQ agents become passive and may not initiate a Start Frame. SER_IRQ will be driven low for four to eight clocks by Host Controller. This mode has two functions. It can be used to stop or idle the SER_IRQ or the Host Controller can operate SER_IRQ in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An SER_IRQ mode transition can only occur during the Stop Frame. **Upon reset, SER_IRQ bus is defaulted to continuous mode, therefore only the Host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next SER_IRQ Cycle's mode.**

SER_IRQ Data Frame

Once a Start Frame has been initiated, the LPC47S42x will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase the LPC47S42x drives the SER_IRQ low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, SER_IRQ is left tri-stated. During the Recovery phase the LPC47S42x drives the SER_IRQ high, if and only if, it had driven the SER_IRQ low during the previous Sample Phase. During the Turn-around Phase the LPC47S42x tri-states the SER_IRQ. The LPC47S42x will drive the SER_IRQ line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. (e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, (6 x 3) - 1 = 17th clock after the rising edge of the Start Pulse).

SER_IRQ Sampling Periods

SER_IRQ PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	Not Used	2
2	IRQ1	5
3	nIO_SMI/IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SER_IRQ data frame supports IRQ2 from a logical device on Period 3, which can also be used for the System Management Interrupt (nSMI). When using Period 3 for IRQ2 the user should mask off the SMI via the SMI Enable Register. Likewise, when using Period 3 for nSMI the user should not configure any logical devices as using IRQ2.

SER_IRQ Period 14 is used to transfer IRQ13. Logical devices 0 (FDC), 3 (Par Port), 4 (Ser Port 1), 5 (Ser Port 2) and 7 (KBD) shall have IRQ13 as a choice for their primary interrupt.

The SMI is enabled onto the SMI frame of the Serial IRQ via bit 6 of SMI Enable Register 2 and onto the SMI pin via bit 7 of the SMI Enable Register 2.

Stop Cycle Control
Once all IRQ/Data Frames have completed the Host Controller will terminate SER_IRQ activity by initiating a Stop Frame. Only the Host Controller can initiate the Stop Frame. A Stop Frame is indicated when the SER_IRQ is low for two or three clocks. If the Stop Frame's low time is two clocks then the next SER_IRQ Cycle's sampled mode is the Quiet mode; and any SER_IRQ device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks then the next SER_IRQ Cycle's sampled mode is the Continuos mode; and only the Host Controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

Latency
Latency for IRQ/Data updates over the SER_IRQ bus in bridge-less systems with the minimum Host supported IRQ/Data Frames of seventeen, will range up to 96 clocks (3.84μS with a 25MHz PCI Bus or 2.88uS with a 33MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

EOI/ISR Read Latency

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the SER_IRQ Cycle latency in order to ensure that these events do not occur out of order.

AC/DC Specification Issue

All SER_IRQ agents must drive / sample SER_IRQ synchronously related to the rising edge of PCI bus clock. The SER_IRQ pin uses the electrical specification of PCI bus. Electrical parameters will follow PCI spec. section 4, sustained tri-state.

Reset and Initialization

The SER_IRQ bus uses nPCI_RESET as its reset signal. The SER_IRQ pin is tri-stated by all agents while nPCI_RESET is active. With reset, SER_IRQ Slaves are put into the (continuous) IDLE mode. The Host Controller is responsible for starting the initial SER_IRQ Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent SER_IRQ Cycles. It is Host Controller's responsibility to provide the default values to 8259's and other system logic before the first SER_IRQ Cycle is performed. For SER_IRQ system suspend, insertion, or removal application, the Host controller should be programmed into Continuous (IDLE) mode first. This is to guarantee SER_IRQ bus is in IDLE state before the system configuration changes.

Routable IRQ to Serial IRQ Conversion Capability

IRQINx functions are on pins 61 (IRQINA), 62 (IRQINB), 40 (IRQINC) and 44 (IRQIND) and are muxed onto the GPIO pins as inputs. The IRQINx pin's IRQ time slot in the Serial IRQ stream is selected via a 4-bit control register for each IRQINx function. A value of 0000 disables the IRQ function. These pins are implemented such that internal functions take precedence over the IRQIN pins, i.e. if the IRQIN control register is set to 0x06 and the internal floppy is set to 0x06, the floppy alone will drive the Serial IRQ stream in the IRQ6 time slot. See Configuration registers located at an offset 0xF4 and 0xF5 in Logical Device A.

The internal IRQs that are used for the devices in the part are given precedence over the IRQs on the GPIO pins. That is, if the IRQx is selected for an activated logical device in the part through register 0x70, and it is enabled for use (see description below), then if the same IRQx is programmed on its associated GPIO pin, the external IRQx will be blocked from the serial IRQ frame. If however the IRQx is selected for an activated logical device in the part through register 0x70, and it is NOT enabled for use, then if the same IRQx is programmed on its associated GPIO pin, this external IRQ will go onto the serial IRQ frame. If the logical device is not activated then the IRQx is not considered enabled.

Therefore, if an IRQ is selected for the logical device through register 0x70 and the logical device is activated, then the enable bit for the device, if present, is used to control whether the internal IRQ or the external IRQ on a GPIO is placed onto the serial stream. The following devices have an enable bit: FDC, UART 1, UART2, the parallel port and the SMBus controller. See "Note A. Logical Device IRQ and DMA Operation" in the "Configuration" section..

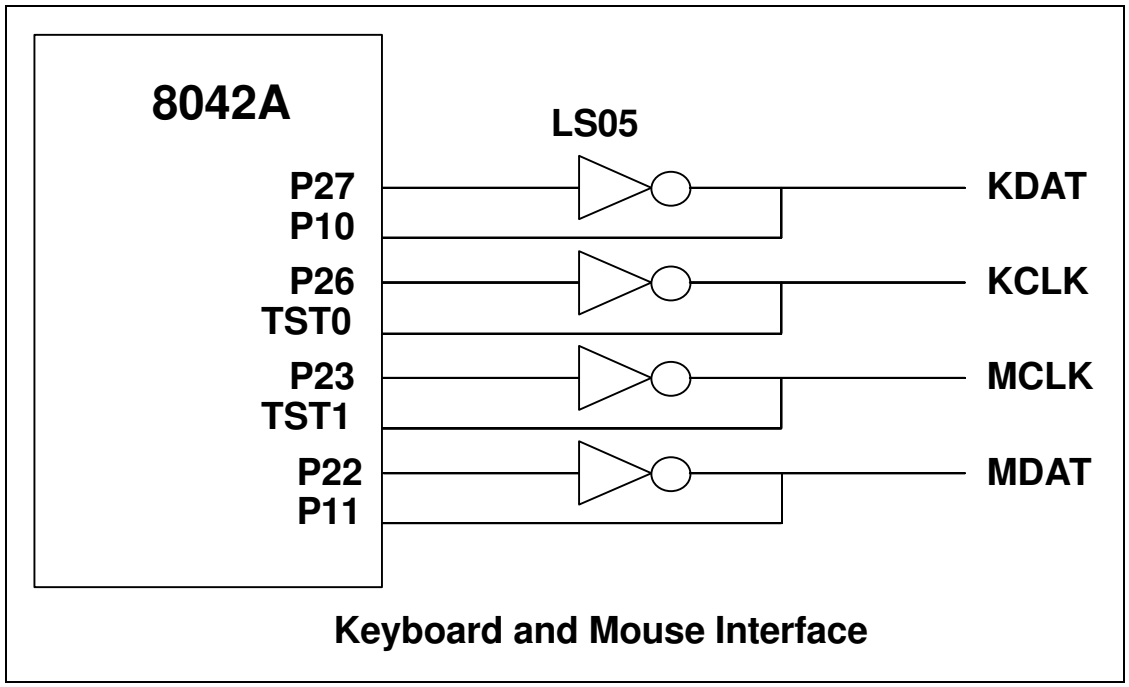
The following devices do not have an enable bit: keyboard, mouse, WDT. For these devices, the interrupt is enabled as follows: programming an IRQ in register 0x70 of logical device 7 enables the keyboard interrupt, programming an IRQ in register 0x72 of logical device 7 enables the mouse interrupt and programming an interrupt in the WDT_CFG register enables the WDT interrupt. Note that the logical device must also be activated for the interrupt to be enabled.

User Note: In order to use the ISA IRQs muxed onto the GPIO pins, the corresponding IRQ must not be used for any of the devices in the LPC47S42x.

8042 KEYBOARD CONTROLLER DESCRIPTION

The LPC47S42x is a Super I/O and Universal Keyboard Controller that is designed for intelligent keyboard management in desktop computer applications.

The Universal Keyboard Controller uses an 8042 microcontroller CPU core. This section concentrates on the LPC47S42x enhancements to the 8042. For general information about the 8042, refer to the "Hardware Description of the 8042" in the 8-Bit Embedded Controller Handbook.



Keyboard and Mouse Interface

KIRQ is the Keyboard IRQ
MIRQ is the Mouse IRQ
Port 21 is used to create a GATEA20 signal from the LPC47S42x.

Keyboard Interface
The LPC47S42x LPC interface is functionally compatible with the 8042 style host interface. It consists of the D0-7 data signals; the read and write signals and the Status register, Input Data register, and Output Data register. Table 45 shows how the interface decodes the control signals. In addition to the above signals, the host interface includes keyboard and mouse IRQs.

Table 45 - I/O Address Map

ADDRESS	COMMAND	BLOCK	FUNCTION (NOTE 1)
0x60	Write	KDATA	Keyboard Data Write (C/D=0)
	Read	KDATA	Keyboard Data Read
0x64	Write	KDCTL	Keyboard Command Write (C/D=1)
	Read	KDCTL	Keyboard Status Read

Note 1: These registers consist of three separate 8 bit registers. Status, Data/Command Write and Data Read.

Keyboard Data Write
This is an 8 bit write only register. When written, the C/D status bit of the status register is cleared to zero and the IBF bit is set.

Keyboard Data Read
This is an 8 bit read only register. If enabled by "ENABLE FLAGS", when read, the KIRQ output is cleared and the OBF flag in the status register is cleared. If not enabled, the KIRQ and/or AUXOBF1 must be cleared in software.

Keyboard Command Write
This is an 8 bit write only register. When written, the C/D status bit of the status register is set to one and the IBF bit is set.

Keyboard Status Read
This is an 8 bit read only register. Refer to the description of the Status Register for more information.

CPU-to-Host Communication
The LPC47S42x CPU can write to the Output Data register via register DBB. A write to this register automatically sets Bit 0 (OBF) in the Status register. See Table 46.

Table 46 - Host Interface Flags

8042 INSTRUCTION	FLAG
OUT DBB	Set OBF, and, if enabled, the KIRQ output signal goes high

Host-to-CPU Communication
The host system can send both commands and data to the Input Data register. The CPU differentiates between commands and data by reading the value of Bit 3 of the Status register. When bit 3 is "1", the CPU interprets the register contents as a command. When bit 3 is "0", the CPU interprets the register contents as data. During a host write operation, bit 3 is set to "1" if SA2 = 1 or reset to "0" if SA2 = 0.

KIRQ
If "EN FLAGS" has been executed and P24 is set to a one: the OBF flag is gated onto KIRQ. The KIRQ signal can be connected to system interrupt to signify that the LPC47S42x CPU has written to the output data register via "OUT DBB,A". If P24 is set to a zero, KIRQ is forced low. On power-up, after a valid RST pulse has been delivered to the device, KIRQ is reset to 0. KIRQ will normally reflects the status of writes "DBB". (KIRQ is normally selected as IRQ1 for keyboard support.)

If "EN FLAGS" has not been executed: KIRQ can be controlled by writing to P24. Writing a zero to P24 forces KIRQ low; a high forces KIRQ high.

MIRQ
If "EN FLAGS" has been executed and P25 is set to a one:; IBF is inverted and gated onto MIRQ. The MIRQ signal can be connected to system interrupt to signify that the LPC47S42x CPU has read the DBB register. If "EN FLAGS" has not been executed, MIRQ is controlled by P25, Writing a zero to P25 forces MIRQ low, a high forces MIRQ high. (MIRQ is normally selected as IRQ12 for mouse support).

Gate A20
A general purpose P21 is used as a software controlled Gate A20 or user defined output.

8042 PINS
The 8042 functions P17, P16 and P12 are implemented as in a true 8042 part. Reference the 8042 spec for all timing. A port signal of 0 drives the output to 0. A port signal of 1 causes the port enable signal to drive the output to 1 within 20-30nsec. After 500nsec (six 8042 clocks) the port enable goes away and the external pull-up maintains the output signal as 1.

In 8042 mode, the pins can be programmed as open drain. When programmed in open drain mode, the port enables do not come into play. If the port signal is 0 the output will be 0. If the port signal is 1, the output tristates: an external pull-up can pull the pin high, and the pin can be shared. In 8042 mode, the pins cannot be programmed as input nor inverted through the GP configuration registers.

External Keyboard and Mouse Interface
Industry-standard PC-AT-compatible keyboards employ a two-wire, bidirectional TTL interface for data transmission. Several sources also supply PS/2 mouse products that employ the same type of interface. To facilitate system expansion, the LPC47S42x provides four signal pins that may be used to implement this interface directly for an external keyboard and mouse.

The LPC47S42x has four high-drive, open-drain output, bidirectional port pins that can be used for external serial interfaces, such as external keyboard and PS/2-type mouse interfaces. They are KCLK, KDAT, MCLK, and MDAT. P26 is inverted and output as KCLK. The KCLK pin is connected to TEST0. P27 is inverted and output as KDAT. The KDAT pin is connected to P10. P23 is inverted and output as MCLK. The MCLK pin is connected to TEST1. P22 is inverted and output as MDAT. The MDAT pin is connected to P11. NOTE: External pull-ups may be required.

Keyboard Power Management
The keyboard provides support for two power-saving modes: soft powerdown mode and hard powerdown mode. In soft powerdown mode, the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode the clock to the 8042 is stopped.

Soft Power Down Mode
This mode is entered by executing a HALT instruction. The execution of program code is halted until either RESET is driven active or a data byte is written to the DBBIN register by a master CPU. If this mode is exited using the interrupt, and the IBF interrupt is enabled, then program execution resumes with a CALL to the interrupt routine, otherwise the next instruction is executed. If it is exited using RESET then a normal reset sequence is initiated and program execution starts from program memory location 0.

Hard Power Down Mode
This mode is entered by executing a STOP instruction. The oscillator is stopped by disabling the oscillator driver cell. When either RESET is driven active or a data byte is written to the DBBIN register by a master CPU, this mode will be exited (as above). However, as the oscillator cell will require an

initialization time, either RESET must be held active for sufficient time to allow the oscillator to stabilize. Program execution will resume as above.

Interrupts
The LPC47S42x provides the two 8042 interrupts: IBF and the Timer/Counter Overflow.

Memory Configurations
The LPC47S42x provides 2K of on-chip ROM and 256 bytes of on-chip RAM.

Register Definitions

Host I/F Data Register
The Input Data register and Output Data register are each 8 bits wide. A write to this 8 bit register will load the Keyboard Data Read Buffer, set the OBF flag and set the KIRQ output if enabled. A read of this register will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag. Refer to the KIRQ and Status register descriptions for more information.

Host I/F Status Register
The Status register is 8 bits wide. Table 47 shows the contents of the Status register.

Table 47 - Status Register

D7	D6	D5	D4	D3	D2	D1	D0
UD	UD	UD	UD	C/D	UD	IBF	OBF

Status Register
This register is cleared on a reset. This register is read-only for the Host and read/write by the LPC47S42x CPU.

UD Writable by LPC47S42x CPU. These bits are user-definable.

C/D (Command Data)-This bit specifies whether the input data register contains data or a command (0 = data, 1 = command). During a host data/command write operation, this bit is set to "1" if SA2 = 1 or reset to "0" if SA2 = 0.

IBF (Input Buffer Full)- This flag is set to 1 whenever the host system writes data into the input data register. Setting this flag activates the LPC47S42x CPU's nIBF (MIRQ) interrupt if enabled. When the LPC47S42x CPU reads the input data register (DBB), this bit is automatically reset and the interrupt is cleared. There is no output pin associated with this internal signal.

OBF (Output Buffer Full) - This flag is set to whenever the LPC47S42x CPU write to the output data register (DBB). When the host system reads the output data register, this bit is automatically reset.

External Clock Signal
The LPC47S42x Keyboard Controller clock source is a 12 MHz clock generated from a 14.318 MHz clock. The reset pulse must last for at least 24 16 MHz clock periods. The pulse-width requirement applies to both internally (VCC POR) and externally generated reset signals. In powerdown mode, the external clock signal is not loaded by the chip.

Default Reset Conditions
The LPC47S42x has one source of hardware reset: an external reset via the nPCI_RESET pin. Refer to Table 48 for the effect of each type of reset on the internal registers.

Table 48 - Resets

DESCRIPTION	HARDWARE RESET (nPCI_RESET)
KCLK	Low
KDAT	Low
MCLK	Low
MDAT	Low
Host I/F Data Reg	N/A
Host I/F Status Reg	00H

N/A: Not Applicable

GATEA20 And Keyboard Reset
The LPC47S42x provides two options for GateA20 and Keyboard Reset: 8042 Software Generated GateA20 and KRESET and Port 92 Fast GateA20 and KRESET.

Port 92 Fast GATEA20 and Keyboard Reset

Port 92 Register
This port can only be read or written if Port 92 has been enabled via bit 2 of the KRST_GA20 Register (Logical Device 7, 0xF0) set to 1.

This register is used to support the alternate reset (nALT_RST) and alternate A20 (ALT_A20) functions.

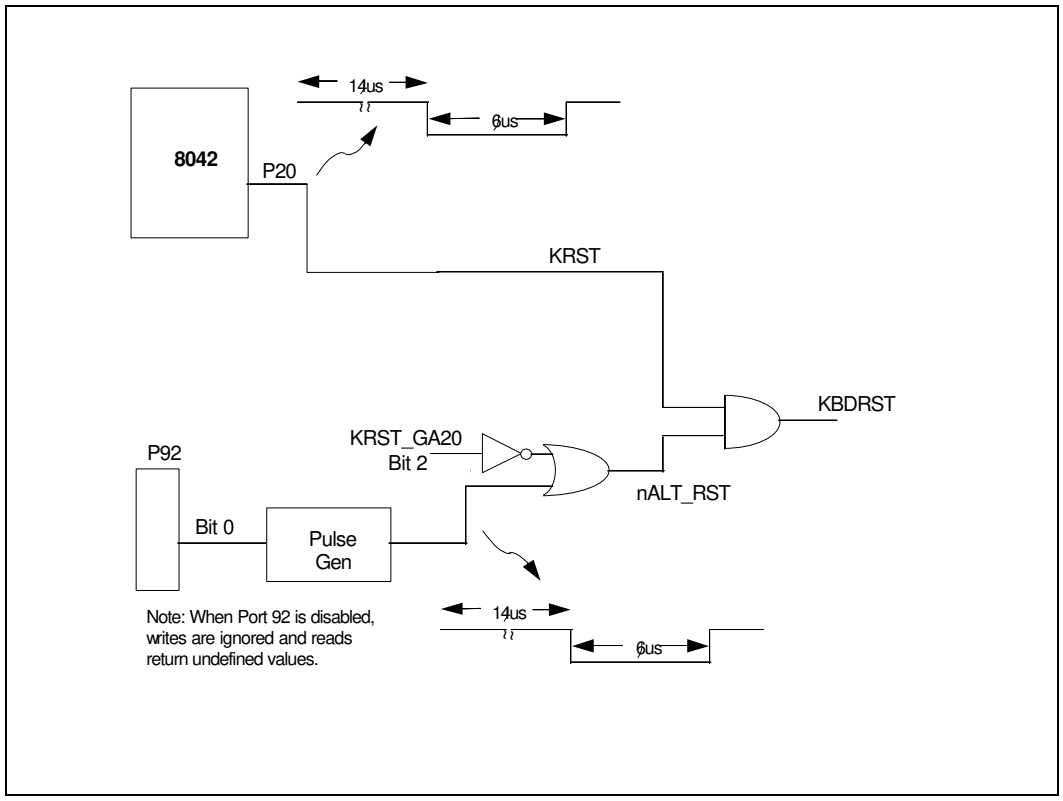
Name	Port 92
Location	92h
Default Value	24h
Attribute	Read/Write
Size	8 bits

Port 92 Register	
BIT	**FUNCTION**
7:6	Reserved. Returns 00 when read
5	Reserved. Returns a 1 when read
4	Reserved. Returns a 0 when read
3	Reserved. Returns a 0 when read
2	Reserved. Returns a 1 when read
1	ALT_A20 Signal control. Writing a 0 to this bit causes the ALT_A20 signal to be driven low. Writing a 1 to this bit causes the ALT_A20 signal to be driven high.
0	Alternate System Reset. This read/write bit provides an alternate system reset function. This function provides an alternate means to reset the system CPU to effect a mode switch from Protected Virtual Address Mode to the Real Address Mode. This provides a faster means of reset than is provided by the Keyboard controller. This bit is set to a 0 by a system reset. Writing a 1 to this bit will cause the nALT_RST signal to pulse active (low) for a minimum of 1 µs after a delay of 500 ns. Before another nALT_RST pulse can be generated, this bit must be written back to a 0.

nGATEA20		
8042 P21	**ALT_A20**	**System nA20M**
0	0	0
0	1	1
1	0	1
1	1	1

Bit 0 of Port 92, which generates the nALT_RST signal, is used to reset the CPU under program control. This signal is AND'ed together externally with the reset signal (nKBDRST) from the keyboard controller to provide a software means of resetting the CPU. This provides a faster means of reset than is provided by the keyboard controller. Writing a 1 to bit 0 in the Port 92 Register causes this signal to pulse low for a minimum of 6µs, after a delay of a minimum of 14µs. Before another nALT_RST pulse can be generated, bit 0 must be set to 0 either by a system reset of a write to Port 92. Upon reset, this signal is driven inactive high (bit 0 in the Port 92 Register is set to 0).

If Port 92 is enabled, i.e., bit 2 of KRST_GA20 is set to 1, then a pulse is generated by writing a 1 to bit 0 of the Port 92 Register and this pulse is AND'ed with the pulse generated from the 8042. This pulse is output on pin KRESET and its polarity is controlled by the GPI/O polarity configuration.



Bit 1 of Port 92, the ALT_A20 signal, is used to force nA20M to the CPU low for support of real mode compatible software. This signal is externally OR'ed with the A20GATE signal from the keyboard controller and CPURST to control the nA20M input of the CPU. Writing a 0 to bit 1 of the Port 92 Register forces ALT_A20 low. ALT_A20 low drives nA20M to the CPU low, if A20GATE from the keyboard controller is also low. Writing a 1 to bit 1 of the Port 92 Register forces ALT_A20 high. ALT_A20 high drives nA20M to the CPU high, regardless of the state of A20GATE from the keyboard controller. Upon reset, this signal is driven low.

Latches On Keyboard and Mouse IRQs
The implementation of the latches on the keyboard and mouse interrupts is shown below.

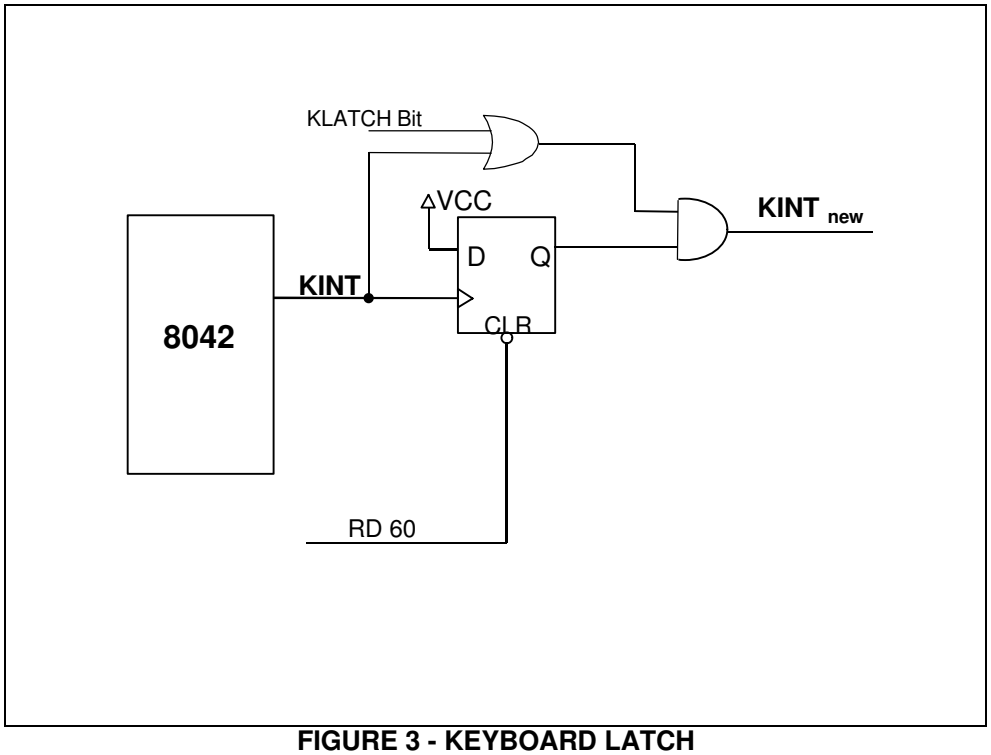


FIGURE 3 - KEYBOARD LATCH

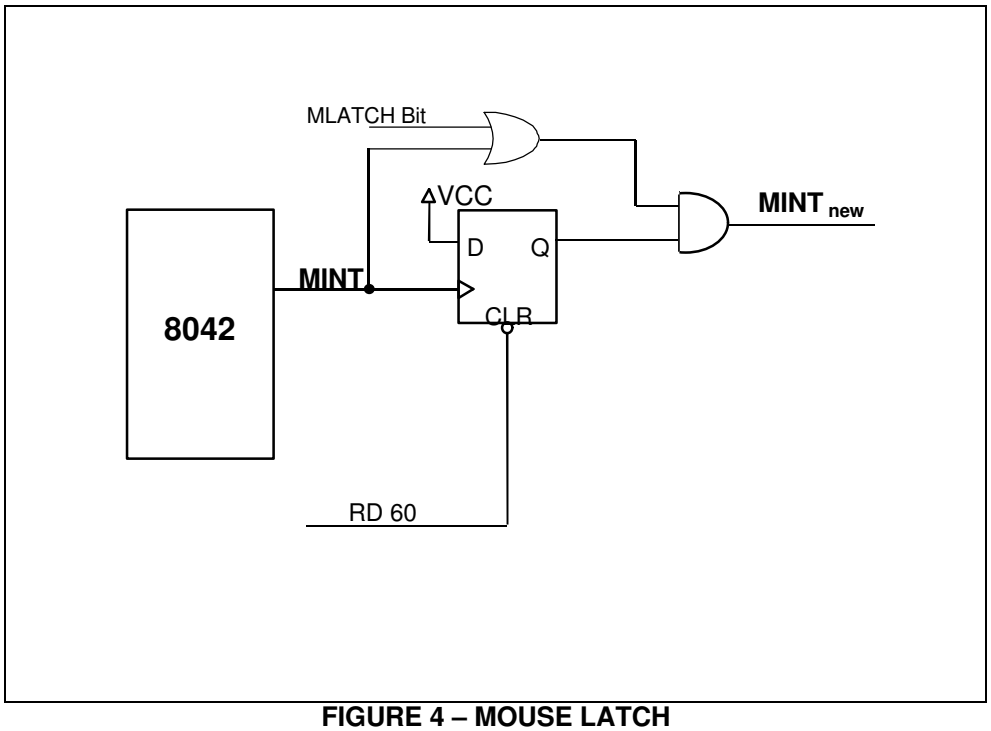


FIGURE 4 – MOUSE LATCH

The KLATCH and MLATCH bits are located in the KRST_GA20 register, in Logical Device 7 at 0xF0. These bits are defined as follows:
Bit[4]: MLATCH – Mouse Interrupt latch control bit. 0=MINT is the 8042 MINT ANDed with Latched MINT (default), 1=MINT is the latched 8042 MINT.
Bit[3]: KLATCH – Keyboard Interrupt latch control bit. 0=KINT is the 8042 KINT ANDed with Latched KINT (default), 1=KINT is the latched 8042 KINT.

See the Configuration section for description on these registers.

Keyboard and Mouse PME Generation

The LPC47S42x sets the associated PME Status bits when the following conditions occur:

- Keyboard Interrupt
- Mouse Interrupt
- Active Edge on Keyboard Data Signal (KDAT)
- Active Edge on Mouse Data Signal (MDAT)

These events can cause a PME to be generated if the associated PME Wake Enable register bit and the global PME_EN bit are set. Refer to the PME Support section for more details on the PME interface logic and refer to the Runtime Register section for details on the PME Status and Enable registers.

The keyboard interrupt and mouse interrupt PMEs can be generated when the part is powered by VCC. The keyboard data and mouse data PMEs can be generated both when the part is powered by VCC, and when the part is powered by VTR (VCC=0).

When using the keyboard and mouse for wakeup, it may be necessary to isolate the keyboard and mouse signals (KCLK, KDAT, MCLK, MDAT) from the 8042 prior to entering certain system sleep states. This is due to the fact that the normal operation of the 8042 can prevent the system from entering or exiting a sleep state, or trigger false PME events. The LPC47S42x has “isolation” bits for the keyboard and mouse signals, which allow the keyboard and mouse data signals to go into the wakeup logic but block the keyboard clock and data signals and the mouse clock and data signals from the 8042. These bits may be used when it is necessary to isolate the 8042 keyboard and mouse signals from the 8042 before entering a system sleep state.

See the SMSC Application Note titled “Using the Enhanced Keyboard and Mouse Wakeup Feature in SMSC Super I/O Parts” for more information.

The bits used to isolate the keyboard and mouse signals from the 8042 are located in Logical Device 7, Register 0xF0 (KRST_GA20) and are defined as follows:
Bit[6] M_ISO. Enables/disables isolation of mouse signals into 8042. Does not affect the MDAT signal to the mouse wakeup (PME) logic.
1=block mouse clock and data signals into 8042
0= do not block mouse clock and data signals into 8042
Bit[5] K_ISO. Enables/disables isolation of keyboard signals into 8042. Does not affect the KDAT signal to the keyboard wakeup (PME) logic.
1= Block keyboard clock and data signals into 8042
0= Do not block keyboard clock and data signals into 8042

When the keyboard and/or mouse isolation bits are used, it may be necessary to reset the 8042 upon exiting the sleep state. If either of the isolation bits is set prior to entering a sleep state where VCC goes inactive (S3-S5), then the 8042 must be reset upon exiting the sleep mode. Write 0x40 to global configuration register 0x2C to reset the 8042. The 8042 must then be taken out of reset by writing 0x00 to register 0x2C since the bit that resets the 8042 is not self-clearing. Caution: Bit 6 of configuration register 0x2C is used to put the 8042 into reset - do not set any of the other bits in register 0x2C, as this may produce undesired results.

It is not necessary to reset the 8042 if the isolation bits are used for a sleep state where VCC does not go inactive (S1, S2).

GENERAL PURPOSE I/O

The LPC47S42x provides a set of flexible Input/Output control functions to the system designer through the 39 dedicated independently programmable General Purpose I/O pins (GPIO). The GPIO pins can perform basic I/O and many of them can be individually enabled to generate an SMI and a PME.

GPIO Pins
The following pins include GPIO functionality. These pins are defined in the table below.

GPIO Pin Functionality

PIN	NAME	POWER WELL	Default on VTR POR	Default on VCC POR	SMI/PME Functionality
1	GP40 /DRVDEN0	VCC	Input	-	nIO_PME
2	GP41 /DRVDEN1/nXCS0	VCC Note 1	Input	-	PME/SMI
17	GP42 /nIO_PME	VTR	Input	-	nIO_PME
28	GP43 /DDRC /nXCS1	VCC Note 1	Input	GPIO Function	PME/SMI
32	GP10 /XD0	VCC Note 1	Input	-	PME/SMI
33	GP11 /XD1	VCC Note 1	Input	-	PME/SMI
34	GP12 /XD2	VCC Note 1	Input	-	PME/SMI
35	GP13 /XD3	VCC Note 1	Input	-	PME/SMI
36	GP14 /XD4	VCC Note 1	Input	-	PME/SMI
37	GP15 /XD5	VCC Note 1	Input	-	PME/SMI
38	GP16 /XD6	VCC Note 1	Input	-	PME/SMI
39	GP17 /XD7	VCC Note 1	Input	-	PME/SMI
41	GP20 /P17 /nDS1	VCC Note 1	Input	-	PME/SMI
40	GP62 /P17 /IRQINC	VCC	Input	-	-
42	GP21 /P16 /IRQ6	VCC Note 1	Input	-	PME/SMI
43	GP22 /P12 / nMTR1	VCC Note 1	Input	-	PME/SMI
44	GP23 /IRQIND	VCC Note 1	Input	-	PME
45	GP24 /SYSOPT	VCC Note 1	Input	-	PME/SMI
46	GP25 /nXRD	VCC Note 1	Input	-	PME/SMI
47	GP26 /nXWR	VCC Note 1	Input	-	PME/SMI
48	GP60 /LED1	VTR Note 1	Input	-	PME/SMI
49	GP61 /LED2	VTR Note 1	Input	-	PME/SMI
50	GP27 /nIO_SMI	VCC Note 1	Input	-	PME/SMI/ nIO_SMI
51	GP30 / SCLK /nXCS2 /XA2	VCC Note 1	Input	-	PME/SMI
52	GP31 /FAN_TACH /nXCS3 /XA3	VCC Note 1	Input	-	PME/SMI
54	GP32 /SDAT /XA0	VCC Note 1	Input	-	PME/SMI
55	GP33 /FAN /XA1	VCC Note 1	Input	Output, low	PME/SMI
61	GP34 /IRQ12 /IRQINA	VCC Note 1	Input	-	PME/SMI
62	GP35 /IRQ14 /IRQINB	VCC Note 1	Input	-	PME/SMI
63	GP36 /nKBDRST	VCC Note 1	Input	-	PME/SMI
64	GP37 /A20M	VCC Note 1	Input	-	PME/SMI
92	GP50 /nRI2	VCC Note 1	Input	-	PME/SMI

PIN	NAME	POWER WELL	Default on VTR POR	Default on VCC POR	SMI/PME Functionality
94	GP51 /nDCD2	VCC Note 1	Input	-	PME/SMI
95	GP52 /RXD2/IRRX	VCC Note 1	Input	-	PME/SMI
96	GP53 /TXD2/IRTX	VTR Note 1	Output, low	Output, low	PME/SMI
97	GP54 /nDSR2	VCC Note 1	Input	-	PME/SMI
98	GP55 /nRTS2	VCC Note 1	Input	-	PME/SMI
99	GP56 /nCTS2	VCC Note 1	Input	-	PME/SMI
100	GP57 /nDTR2	VCC Note 1	Input	-	PME/SMI

Note 1: These pins have input buffers into the wakeup logic that are powered by VTR.

Description

Each GPIO port has a 1-bit data register and an 8-bit configuration control register. The data register for each GPIO port is represented as a bit in one of the 8-bit GPIO DATA Registers, GP1 to GP8. The bits in these registers reflect the value of the associated GPIO pin as follows. Pin is an input: The bit is the value of the GPIO pin. Pin is an output: The value written to the bit goes to the GPIO pin. Latched on read and write. All of the GPIO registers are located in the Runtime Register block; see the Runtime Registers section. The GPIO ports with their alternate functions and configuration state register addresses are listed in the Table on the following page.

General Purpose I/O Port Assignments

PIN NO. /QFP	DEFAULT FUNCTION	ALT. FUNC. 1	ALT FUNC.2	ALT. FUNC. 3	DATA REGISTER[1]	DATA REGISTER BIT NO.	REGISTER OFFSET (HEX)
32	GPIO	X-Bus Data 0			GP1	0	4B
33	GPIO	X-Bus Data 1				1	
34	GPIO	X-Bus Data 2				2	
35	GPIO	X-Bus Data 3				3	
36	GPIO	X-Bus Data 4				4	
37	GPIO	X-Bus Data 5				5	
38	GPIO	X-Bus Data 6				6	
39	GPIO	X-Bus Data 7				7	
41	GPIO	P17	Drive Select 1		GP2	0	4C
42	GPIO	P16	P12	EETI		1	
43	GPIO	P12	Motor On 1	EETI		2	
44	GPIO	IRQ Input D				3	
45	GPIO					4	
46	GPIO	X-Bus Read Strobe				5	
47	GPIO	X-Bus Write Strobe				6	
50	GPIO	nIO_SMI				7	
51	GPIO	SMBus Clock	X-Bus Chip Select 2	X-Bus Address 2	GP3	0	4D
52	GPIO	Fan Tachometer Input	X-Bus Chip Select 3	X-Bus Address 3		1	
54	GPIO	SMBus Data	X-Bus Address 0			2	
55	GPIO	Fan Control	X-Bus Address 1			3	
61	GPIO	IRQ Input A				4	
62	GPIO	IRQ Input B				5	
63	GPIO	Keyboard Reset				6	
64	GPIO	Gate A20				7	
1	GPIO	Drive Density Select 0			GP4	0	4E
2	GPIO	Drive Density Select 1	EETI			1	
17	GPIO	Power Management Event				2	
28	GPIO	Device Disable Reg. Control	X-Bus Chip Select 1	EETI		3	

PIN NO. /QFP	DEFAULT FUNCTION	ALT. FUNC. 1	ALT FUNC.2	ALT. FUNC. 3	DATA REGISTER[1]	DATA REGISTER BIT NO.	REGISTER OFFSET (HEX)
N/A	Reserved					4	
N/A	Reserved					5	
N/A	Reserved					6	
N/A	Reserved					7	
92	GPIO	Ring Indicator 2			GP5	0	4F
94	GPIO	Data Carrier Detect 2				1	
95	GPIO	Receive Serial Data 2	Infrared Receive			2	
96	GPIO	Transmit Serial Data 2	Infrared Transmit			3	
97	GPIO	Data Set Ready 2				4	
98	GPIO	Request to Send 2				5	
99	GPIO	Clear to Send 2				6	
100	GPIO	Date Terminal Ready 2				7	
48	GPIO	LED1	EETI		GP6	0	50
49	GPIO	LED2	EETI			1	
40	GPIO	P17				2	
N/A	Reserved					3	
N/A	Reserved					4	
N/A	Reserved					5	
N/A	Reserved					6	
N/A	Reserved					7	

Note 1: The GPIO Data and Configuration Registers are located in PME block at the offset shown from the RUNTIME REGISTERS BLOCK address.

GPIO Control
Each GPIO port has an 8-bit control register that controls the behavior of the pin. These registers are defined in the "Runtime Registers" section of this specification.

Each GPIO port may be configured as either an input or an output. If the pin is configured as an output, it can be programmed as open-drain or push-pull. Inputs and outputs can be configured as non-inverting or inverting. Bit[0] of each GPIO Configuration Register determines the port direction, bit[1] determines the signal polarity, and bit[7] determines the output driver type select. The GPIO configuration register Output Type select bit[7] applies to GPIO functions and the nSMI Alternate functions.

The Polarity Bit (bit 1) of the GPIO control registers control the GPIO pin when the pin is configured for the GPIO function and when the pin is configured for the alternate function for all pins, with the exception of the DDRC function on GP43 and the either edge triggered interrupts.

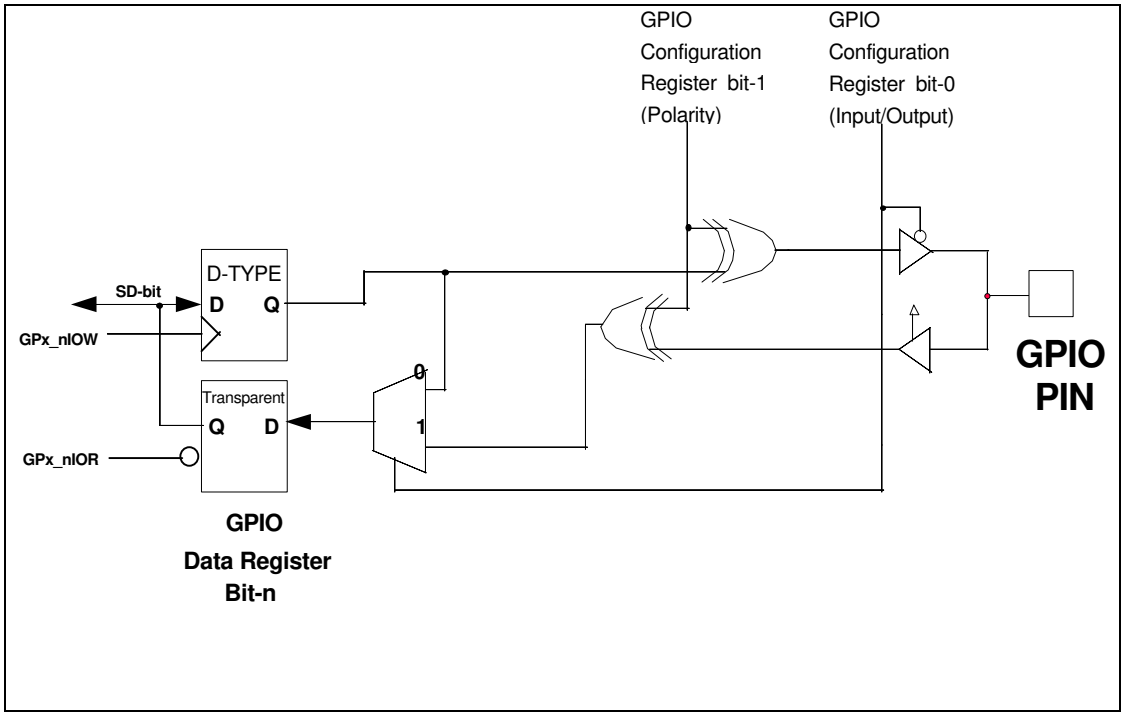
The basic GPIO configuration options are summarized in the following Table.

GPIO Configuration Summary

SELECTED FUNCTION	DIRECTION BIT	POLARITY BIT	DESCRIPTION
	B0	B1	
GPIO	0	0	Pin is a non-inverted output
	0	1	Pin is an inverted output
	1	0	Pin is a non-inverted input
	1	1	Pin is an inverted input

GPIO Operation
The operation of the GPIO ports is illustrated in the Figure below.

Note: The following Figure is for illustration purposes only and in not intended to suggest specific implementation details.



GPIO Function Illustration

Note: When the following functions are selected, the associated GPIO pins have bi-directional functionality: P12, P16, P17.

When a GPIO port is programmed as an input, reading it through the GPIO data register latches either the inverted or non-inverted logic value present at the GPIO pin. Writing to a GPIO port that is programmed as an input has no effect.

When a GPIO port is programmed as an output, the logic value or the inverted logic value that has been written into the GPIO data register is output to the GPIO pin. Reading from a GPIO port that is programmed as an output returns the last value written to the data register.

HOST OPERATION	GPIO INPUT PORT	GPIO OUTPUT PORT
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

GPIO Read/Write Behavior

The LPC47S42x provides 36 GPIOs that can directly generate a PME. See the table in the next section. The polarity bit in the GPIO control registers select the edge on these GPIO pins that will set the associated status bit in the PME_STS2 – PME_STS7 registers. The default is the low-to-high edge. If the corresponding enable bit in the PME_EN 2 – PME_EN7 registers and the PME_EN bit in the PME_EN register is set, a PME will be generated. These registers are located in the Runtime Registers Block, which are located at the address contained in the configuration registers 0x60 and 0x61 in Logical Device A. The PME status bits for the GPIOs are cleared on a write of '1'. In addition, the LPC47S42x provides 35 GPIOs that can directly generate an SMI. See the table in the next section.

GPIO PME and SMI Functionality

The following GPIOs are dedicated wakeup GPIOs with a status and enable bit in the PME status and enable registers:

GP10-GP17
GP20-GP27
GP30-GP37
GP41, GP43
GP50-GP57
GP60, GP61

This following is the list of PME status and enable registers for their corresponding GPIOs:
PME_STS2 and PME_EN2 for GP10-GP17
PME_STS3 and PME_EN3 for GP20-GP27
PME_STS4 and PME_EN4 for GP30-GP33, GP41, GP43, GP60, GP61
PME_STS5 and PME_EN5 for GP50-GP57
PME_STS7 and PME_EN7 for GP34-GP37

The following GPIOs can directly generate an SMI and have a status and enable bit in the SMI status and enable registers.

GP10-GP17
GP20-22, GP24-27
GP30-GP37
GP41, GP43
GP50-GP57
GP60, GP61

The following SMI status and enable registers for these GPIOs:
SMI_STS3 and SMI_EN3 for GP20-22, GP24-27, GP60
SMI_STS4 and SMI_EN4 for GP30-GP33, GP41, GP43, GP61
SMI_STS5 and SMI_EN5 for GP50-GP57
SMI_STS5 and SMI_EN5 for GP10-GP17

SMI_STS7 and SMI_EN7 for GP34-GP37

The following GPIOs have “either edge triggered interrupt” (EETI) input capability. These GPIOs can generate a PME and an SMI on both a high-to-low and a low-to-high edge on the GPIO pin. These GPIOs have a status bit in the MSC_STS status register that is set on both edges. The corresponding bits in the PME and SMI status registers are also set on both edges.

GP21, GP22
GP41, GP43
GP60, GP61

The following table summarizes the PME and SMI functionality for each GPIO. It also shows the Either Edge Triggered Interrupt (EETI) input capability for the GPIOs and the power source for the buffer on the I/O pads.

GPIO	PME	SMI	EETI	Output Buffer Power	Notes
GP10-GP17	Yes	Yes	No	VCC	
GP20-GP26	Yes	Yes	GP21-GP22	VCC	
GP27	Yes	Yes/nIO_SMI	No	VCC	5
GP30-GP37	Yes	Yes	No	VCC	2
GP41	Yes	No	Yes	VCC	1
GP42	nIO_PME	No	No	VTR	
GP43	Yes	Yes	Yes	VCC	3
GP50-GP57	Yes	Yes	No	VCC	4
GP60	Yes	No	Yes	VCC	
GP61	Yes	Yes	Yes	VCC	
GP62	Yes	No	No	VCC	1

Note 1: GP40 and GP62 should not be connected to any VTR powered external circuitry. These pins are not used for wakeup.

Note 2: The GP33 pin cannot be used for wakeup to generate a PME while the part is under VTR power (VCC=0) since GP33 is the FAN pin which comes up as output and low on a VCC POR and hard reset. This pin reverts to its non-inverting GPIO output function when VCC is removed from the part.

Note 3: GP43 defaults to the GPIO function on VCC POR and Hard Reset.

Note 4: GP53 pin cannot be used for wakeup to generate a PME while the part is under VTR power (VCC=0) since GP53 is the IRTX pin which comes up as output and low on a VTR POR, VCC POR and Hard Reset. This pin is a non-inverting GPIO output (low) when VCC is removed from the part.

Note 5: Since GP27 can be used to generate an SMI and as the nIO_SMI output, do not enable GP27 to generate an SMI (by setting bit 7 of the SMI Enable Register 3) if the nIO_SMI function is selected on the GP27 pin. Use GP27 to generate an SMI event only if the SMI output is enabled on the Serial IRQ stream.

EITHER EDGE TRIGGERED INTERRUPTS

Six GPIO pins are implemented such that they allow an interrupt (PME or SMI) to be generated on both a high-to-low and a low-to-high edge transition, instead of one or the other as selected by the polarity bit.

The either edge triggered interrupts (EETI) function as follows: If the EETI function is selected for the GPIO pin, then the bits that control input/output, polarity and open collector/push-pull have no effect on the function of the pin. However, the polarity bit does affect the value of the GP bit (i.e., register GP2, bit 2 for GP22).

A PME or SMI interrupt occurs if the PME or SMI enable bit is set for the corresponding GPIO and the EETI function is selected on the GPIO. The PME or SMI status bits are set when the EETI pin transitions (on either edge) and are cleared on a write of '1'. There are also status bits for the EETIs located in the MSC_STS register, which are also cleared on a write of '1'. The MSC_STS register provides the status of all of the EETI interrupts within one register. The PME, SMI or MSC status is valid whether or not the interrupt is enabled and whether or not the EETI function is selected for the pin.

Miscellaneous Status Register (MSC_STS) is for the either edge triggered interrupt status bits. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding MSC status bits. Status bits are cleared on a write of '1'. See Runtime Register section for more information.

LED FUNCTIONALITY

The LPC47S42x provides LED functionality on two GPIOs, GP60 and GP61. These pins can be configured to turn the LED on and off and blink independent of each other through the LED1 and LED2 runtime registers at offset 0x5D and 0x5E from the base address located in the primary base I/O address in Logical Device A.

The LED pins (GP60 and GP61) are able to control the LED while the part is under VTR power with VCC removed. In order to control a LED while the part is under VTR power, the GPIO pin must be configured for the LED function and either open drain or push-pull buffer type. In the case of open-drain buffer type, the pin is capable of sinking current to control the LED. In the case of push-pull buffer type, the part will source current. The part is also able to blink the LED under VTR power. The LED will not blink under VTR power (VCC removed) if the external 32kHz clock is not connected.

The LED pins can drive a LED when the buffer type is configured to be push-pull and the part is powered by either VCC or VTR, since the buffers for these pins are powered by VTR. This means they will source their specified current from VTR even when VCC is present.

The GP61 pin defaults to the LED function active (blinking at a 1 Hz rate, 50% duty cycle) on initial power up (as long as the 32 kHz clock input is active).

The LED control registers are defined in the "Runtime Register" section.

WATCH DOG TIMER

The LPC47S42x contains a Watch Dog Timer (WDT). The Watch Dog Time-out status bit may be mapped to an interrupt through the WDT_CFG Configuration Register.

The LPC47S42x's WDT has a programmable time-out ranging from 1 to 255 minutes with one minute resolution, or 1 to 255 seconds with 1 second resolution. The units of the WDT timeout value are selected via bit[7] of the WDT_TIMEOUT register (LD8:CRF1.7). The WDT time-out value is set through the WDT_VAL Configuration register. Setting the WDT_VAL register to 0x00 disables the WDT function (this is its power on default). Setting the WDT_VAL to any other non-zero value will cause the WDT to reload and begin counting down from the value loaded. When the WDT count value reaches zero the counter stops and sets the Watchdog time-out status bit in the WDT_CTRL Configuration Register. Note: Regardless of the current state of the WDT, the WDT time-out status bit can be directly set or cleared by the Host CPU.

There are three system events that can reset the WDT. These are a Keyboard Interrupt, a Mouse Interrupt and I/O reads/writes to address 0x201 (an external Joystick Port). The effect on the WDT for each of these system events may be individually enabled or disabled through bits in the WDT_CFG configuration register. When a system event is enabled through the WDT_CFG register, the occurrence of that event will cause the WDT to reload the value stored in WDT_VAL and reset the WDT time-out status bit if set. If all three system events are disabled the WDT will inevitably time out.

The Watch Dog Timer may be configured to generate an interrupt on the rising edge of the Time-out status bit. The WDT interrupt is mapped to an interrupt channel through the WDT_CFG Configuration Register. When mapped to an interrupt the interrupt request pin reflects the value of the WDT time-out status bit.

The host may force a Watch Dog time-out to occur by writing a "1" to bit 2 of the WDT_CTRL (Force WD Time-out) Configuration Register. Writing a "1" to this bit forces the WDT count value to zero and sets bit 0 of the WDT_CTRL (Watch Dog Status). Bit 2 of the WDT_CTRL is self-clearing. See the Runtime Registers section for a description on these registers.

SYSTEM MANAGEMENT INTERRUPT (SMI)

The LPC47S42x implements a “group” nIO_SMI output pin. The System Management Interrupt is a non-maskable interrupt with the highest priority level used for OS transparent power management. The nSMI group interrupt output consists of the enabled interrupts from Super I/O Device Interrupts and many of the GPIOs pins. The GP27/nIO_SMI pin, when selected for the nIO_SMI function, can be programmed to be active high or active low via the polarity bit in the GP27 register. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 of the GP27 register. The nIO_SMI pin function defaults to active low, open-drain output.

The interrupts are enabled onto the group nSMI output via the SMI Enable Registers 1 to 7. The nSMI output is then enabled onto the group nIO_SMI output pin via bit[7] in the SMI Enable Register 2. The SMI output can also be enabled onto the serial IRQ stream (IRQ2) via Bit[6] in the SMI Enable Register 2.

An example logic equation for the nSMI output for SMI registers 1 and 2 is as follows:
nSMI = (EN_PINT and IRQ_PINT) or (EN_U2INT and IRQ_U2INT) or (EN_U1INT and IRQ_U1INT) or (EN_FINT and IRQ_FINT) or (EN_WDT and IRQ_WDT) or (EN_MINT and IRQ_MINT) or (EN_KINT and IRQ_KINT) or (EN_SMBus and IRQ_SMBus) or (EN_RI1 and IRQ_RI1) or (EN_P12 and IRQ_P12) or (EN_RI2 and IRQ_RI2)
Note: The prefixes EN and IRQ are used above to indicate SMI enable bit and SMI status bit respectively.

SMI Registers
The SMI event bits for the GPIOs and the Fan tachometer events are located in the SMI status and Enable registers 3-5. The polarity of the edge used to set the status bit and generate an SMI is controlled by the polarity bit of the control registers. For non-inverted polarity (default) the status bit is set on the low-to-high edge. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding SMI status bit. Status bits for the GPIOs are cleared on a write of '1'.

The SMI logic for these events is implemented such that the output of the status bit for each event is combined with the corresponding enable bit in order to generate an SMI.

The P12 and P16 bits enable an SMI event on single high-to-low edge or on both high-to-low and low-to-high edges. Default is single edge. There is also a polarity select bit for P12 in the Configuration Register 0xF0 in Logical Device 7. The register that selects the edge, Edge Select register, is located at the address programmed in the Base I/O Address register in the Logical Device A at an offset of 21h. Refer also to PME Status and Enable register 2. See the Runtime Registers sections for description on these registers.

If both edges are selected for generating an SMI via P16, then the SMI is asserted on each edge until the P16 SMI status bit is cleared. If both edges are selected for generating an SMI via P12, then a short pulse (20ns) is generated on each edge. However the P12 SMI status bit is set on each edge until cleared. The P12 SMI is not recommended to be used in this mode of operation.

Note that P12 and P16 SMI status bits are cleared by a write of '1'. The SMI generated by P16 is also deasserted when the P16 SMI status bit is written to '1'. However, the SMI generated by P12 is cleared at the source.

The SMI logic for the P16 event is implemented such that the output of the status bit for the event is combined with the corresponding enable bit in order to generate an SMI.

The SMI registers are accessed at an offset from Runtime Registers Block (see Runtime Register section for more information).

The SMI event bits for the super I/O devices are located in the SMI status and enable register 1 and 2. All of these status bits are cleared at the source except for IRINT, which is cleared by a read of the SMI_STS2 register; these status bits are not cleared by a write of '1'. The SMI logic for these events is implemented such that each event is directly combined with the corresponding enable bit in order to generate an SMI.

See the "Runtime Registers" section for the definition of these registers.

ACPI Support Register for SMI Generation
The ACPI PM1 Control register is implemented in the LPC47S42x to allow the generation of an SMI when the SLP_EN bit (PM1_CNTRL2 bit 5) is written to '1'. The SLP_TYPx field (bits[4:2]) is also read/write but has no functionality in the part.

The PM1_CNTRL1 and PM1_CNTRL2 registers implement the ACPI PM1 Control register. These registers are located at the address programmed in the Base I/O address in Logical Device A at the offset of 0x60, 0x61. Software will treat these as a 16-bit register since the two 8-bit registers are adjacent.

Bit[5] in the SMI_STS7 register is the status bit and bit[5] in the SMI_EN7 register is the enable bit for the generation of the SMI when the SLP_EN bit is written to '1'. These registers are located at the address programmed in the Base I/O address in Logical Device A at the offset of 0x64 and 0x66.

See the Runtime Registers section for description on these registers.

PME Support
The LPC47S42x offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events in an ACPI system. A power management event is indicated to the chipset via the assertion of the nIO_PME signal. In the LPC47S42x, the nIO_PME is asserted by active transitions on the ring indicator inputs nRI1 and nRI2, active keyboard-data edges, active mouse-data edges, Wakeup on Specific key, Super I/O Device Interrupts, Watchdog Timer, programmable edges on GPIO pins and fan tachometer event. The GP42/nIO_PME pin, when selected for the nIO_PME function, can be programmed to be active high or active low via the polarity bit in the GP42 register. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 of the GP42 register. The nIO_PME pin function defaults to active low, open-drain output.

PME functionality is controlled by the PME status and enable registers in the runtime registers block, which is located at the address programmed in configuration registers 0x60 and 0x61 in Logical Device A. The PME Enable bit, PME_EN, globally controls PME Wake-up events. When PME_EN is inactive, the nIO_PME signal can not be asserted. When PME_EN is asserted, any wake source whose individual PME Wake Enable register bit, is asserted can cause nIO_PME to become asserted.

The PME Wake Status register indicates that an enabled wake source has occurred and if the PME_EN bit is set, asserted the nIO_PME signal. The PME Status bit is asserted by active transitions of PME Wake sources. PME_STS will become asserted independent of the state of the global PME enable, PME_EN.

The following pertains to the PME status bits for each event:
- The output of the status bit for each event is combined with the corresponding enable bit to set the PME status bit.
- The status bit for any pending events must be cleared in order to clear the PME_STS bit.

For the GPIO events, the polarity of the edge used to set the status bit and generate a PME is controlled by the polarity bit of the GPIO control register. For non-inverted polarity (default) the status bit is set on the low-to-high edge. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding PME status bits. Status bits are cleared on a write of '1'.

The PME Wake registers also include status and enable bits for the fan tachometer input.

See the “Keyboard and Mouse PME Generation” section for information about using the keyboard and mouse signals to generate a PME.

The P12 and P16 bits enable a PME event on single high-to-low edge or on both high-to-low and low-to-high edges. Default is single edge. There is also a polarity select bit in the configuration register at 0xF0 in Logical Device 7. The register that selects the edge, Edge Select register, is located at the address programmed in the Base I/O Address register in the Logical Device A at an offset of 21h. Refer also to PME Status and Enable register 9. See the Runtime Registers sections for description on these registers.

If both edges are selected for generating a PME via P12 or P16, then the PME is asserted on each edge until the corresponding PME status bit is cleared.

Note that P12 and P16 status bits are cleared on by write of ‘1’. The SMI generated by P12 and P16 is deasserted when the associated PME status bit is cleared.

In the LPC47S42x the nIO_PME pin can be programmed to be an open drain, active low, driver. The LPC47S42x nIO_PME pin is fully isolated from other external devices that might pull the nIO_PME signal low; i.e., the nIO_PME signal is capable of being driven high externally by another active device or pullup even when the LPC47S42x Vcc is grounded, providing VTR power is active. The LPC47S42x nIO_PME driver sinks 6mA at .55V max (see section 4.2.1.1 DC Specifications, page 122, in the PCI Local Bus Specification, Revision 2.1).

The PME registers are run-time registers as follows. These registers are located in system I/O space at an offset from Runtime Registers Block, the address programmed in Logical Device A at registers 0x60 and 0x61.

The following registers are for GPIO PME events:
- PME Wake Status 2 (PME_STS2), PME Wake Enable 2 (PME_EN2)
- PME Wake Status 3 (PME_STS3), PME Wake Enable 3 (PME_EN3)
- PME Wake Status 4 (PME_STS4), PME Wake Enable 4 (PME_EN4)
- PME Wake Status 5 (PME_STS5), PME Wake Enable 5 (PME_EN5)
- PME Wake Status 7 (PME_STS7), PME Wake Enable 7 (PME_EN7)

The PME Wake Status 6 (PME_STS6), PME Wake Enable 6 (PME_EN6) registers are for the device interrupt PME events.
The PME Wake Status 1 (PME_STS1), PME Wake Enable 1 (PME_EN1) registers are for pin and internal function PME events.

See PME register description in the Runtime Register Section.

Wake On Specific Key Option

The LPC47S42x has logic to detect a single keyboard scan code for wakeup (PME generation). The scan code is programmed onto the Keyboard Scan Code Register, a runtime register at offset 0x5F from the base address located in the primary base I/O address in Logical Device A. This register is powered by VTR and reset on VTR POR.

The PME status bit for this event is located in the PME_STS1 register at bit 5 and the PME enable bit for this event is located in the PME_EN1 register at bit 5. See the Runtime Register section for a definition of these registers.

Data transmissions from the keyboard consist of an 11-bit serial data stream. A logic 1 is sent at an active high level. The following table shows the functions of the bits.

BIT	FUNCTION
1	Start bit (always 0)
2	Data bit 0 (least significant bit)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (most significant bit)
10	Parity bit (odd parity)
11	Stop Bit (always 1)

The timing for the keyboard clock and data signals are shown in the "Timing Diagrams" section.

The CLK32_PRSN bit (bit 0 of the CLOCKI32 register at 0xF0 in Logical Device A) will determine the clock source for this feature when the part is powered by VCC. If the external 32kHz clock is not connected, the 32kHz internal signal is derived from the 14MHz clock when VCC is active. Use the 32kHz clock for this feature when the part is under trickle power. This feature will not work when the part is under trickle power (VCC removed) if the external 32kHz clock is not connected.

The SPEKEY_EN bit at bit 1 of the CLOCKI32 register at 0xF0 in Logical Device A is used to control this feature. This bit is used to turn the logic for this feature on and off. It will disable the 32kHz clock input to the logic. The logic will draw no power when disabled. The bit is defined as follows:
0= Wake on specific key logic is on (default)
1= Wake on specific key logic is off

Note: The generation of a PME for this event is controlled by the PME enable bit (located in the PME_EN1 register at bit 5) when the logic for feature is turned on.

FAN SPEED CONTROL AND MONITORING

The LPC47S42x implements fan speed control outputs and fan tachometer inputs. The implementation of these features are described in the sections below.

Fan Speed Control

The fan speed control for the LPC47S42x is implemented as pulse width modulators with fan clock speed selection.

Pin 55 is the fan speed control output FAN, muxed with GPIOs. This fan control pin come up as output and is low following a VCC POR and Hard Reset. This pin may not be used for wakeup events under VTR power (VCC=0).

The register is defined in the “Runtime Registers” section.

Fan Speed Control Summary

The following table illustrates the different modes for the fan.

Table 49 – Different Modes for Fan

FAN Clock Control Bit (Note 1)	FAN Clock Multiplier Bit (Note 2)	FAN Clock Source Select Bit (Note 3)	FAN Clock Select Bit (Note 4)	F_{out}	6-Bit Duty Cycle Control bits[6:1] (DCC)	Duty Cycle (%)
0	X	X	X	0Hz – LOW	0	-
0	0	0	0	15.625kHz	1-63	(DCC/64) • 100
0	0	0	1	23.438kHz		
0	0	1	0	40Hz		
0	0	1	1	60Hz		
0	1	0	0	31.25kHz		
0	1	0	1	46.876kHz		
0	1	1	0	80Hz		
0	1	1	1	120Hz		
1	X	X	X	0Hz – HIGH	-	-

Note 1: This is FAN Register Bit 0
Note 2: This is Fan Control Register Bit 2
Note 3: This is Fan Control Register Bit 0
Note 4: This is FAN Register Bit 7

Fan Register
The Fan Register is located at 0x56 from base I/O in Logical Device A. See register description in the Runtime Registers section.

Fan Clock Select, D7
The Fan Clock Select bit in the Fan registers is used with the Fan Clock Source Select and the Fan Clock Multiplier bits in the Fan Control register to determine the fan speed F_{OUT}. See Table 49 above.

Duty Cycle Control, D6 – D1
The Duty Cycle Control (DCC) bits determine the fan duty cycle. The LPC47S42x has ≈1.56% duty cycle resolution.

When DCC = "000000" (min. value), F_{OUT} is always low. When DCC is "111111" (max. value), F_{OUT} is almost always high; i.e., high for $63/64^{th}$ and low for $1/64^{th}$ of the F_{OUT} period.

Generally, the F_{OUT} duty cycle (%) is $(DCC \div 64) \times 100$.

Fan Clock Control, D0
The Fan Clock Control bit D0 is used to override the Duty Cycle Control bits and force F_{OUT} always high.

When D0 = "0", the DCC bits determine the F_{OUT} duty cycle. When D0 = 1, F_{OUT} is always high, regardless of the state of the DCC bits.

Fan Control Register
The Fan Control Register is located at 0x58 from base I/O in Logical Device A. See the register description in the Runtime Registers section.

Fan Count Divisor, D5 – D4
Fan Count Divisor bit in Fan Control Register is used to determine fan tachometer count. The choices for the divisor are 1, 2, 4 and 8. See Fan Tachometer Input section.

Fan Clock Multiplier, D2
The Fan Clock Multiplier bit is used with the Fan Clock Source Select bit in the Fan Control Register and the Fan Clock Select bit in Fan register to determine the F_{OUT}.

When the Fan Clock Multiplier bit = "0", no clock multiplier is used. When the Fan Clock Multiplier bit = "1", the clock speed determined by the Fan Clock Source Select bit is doubled.

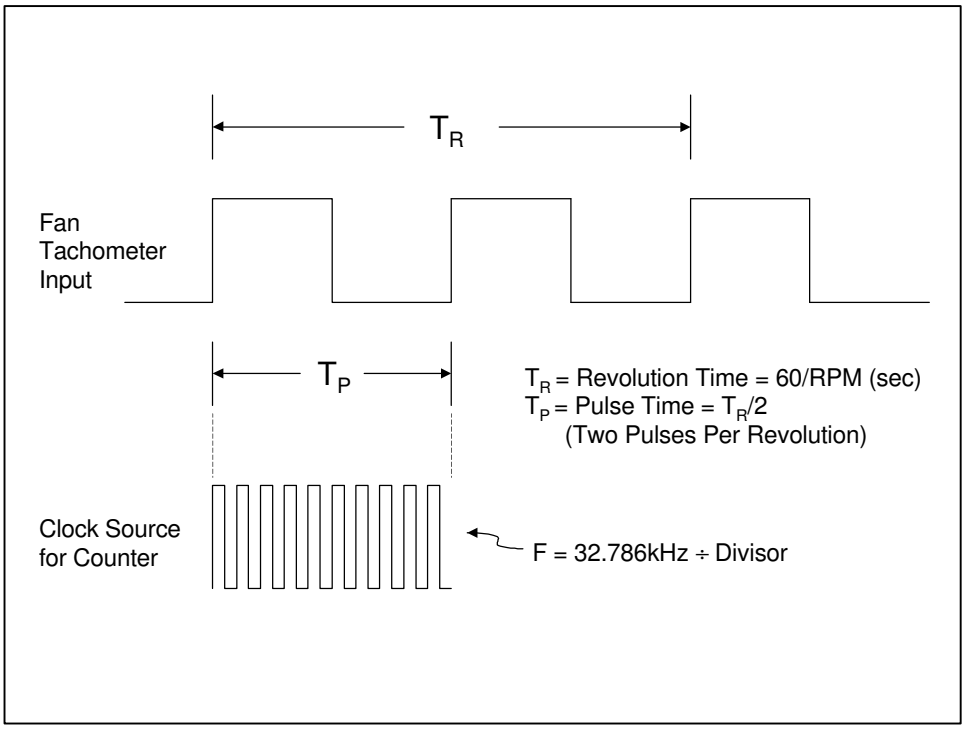
Fan Clock Source Select, D0
The Fan Clock Source Select and the Fan Clock Multiplier bits in the Fan Control register is used with The Fan Clock Select bit in the Fan registers to determine the fan speed F_{OUT}. See Table 49 above.

Fan Tachometer Input
The LPC47S42x implements fan tachometer input for signals from fans equipped with tachometer outputs. The part can generate both a PME and an SMI when the fan speed drops below a predetermined value. See description below.

The clock source for the tachometer count is the 32.768kHz oscillator. The Fan Tachometer Input gate a divided down version of the 32.768kHz oscillator for one period of the Fan signal into an 8-bit counter (maximum count is 255).

The clock source is determined by the CLK32_PRSN bit in the CLOCKI32 register in logical device A. It is either the 32.768kHz clock from the CLKI32 pin or an internal 32.765kHz clock derived from the 14MHz clock.

The fan tachometer input signal and clock source is shown below.



The counter is reset by the rising edge of each pulse (and by writing the preload register). The counter does not wrap; if it reaches 0xFF, it remains at 0xFF until it is reset by the next pulse.

The 2 MSBs of the count are sampled and a PME or SMI is generated (if enabled through the PME_EN1 enable register or the SMI_EN5 enable register - see the “Runtime Registers” section) when these two bits are set. This corresponds to a count value of 192.

The fan count is determined according to the following equation:

$$\text{Count} = \frac{1}{2} \times \underbrace{\frac{1.966 \times 10^6}{\text{RPM} \times \text{Divisor}}}_{\text{(Term 1)}} + \text{Preload} \quad \text{(Equation 1)}$$

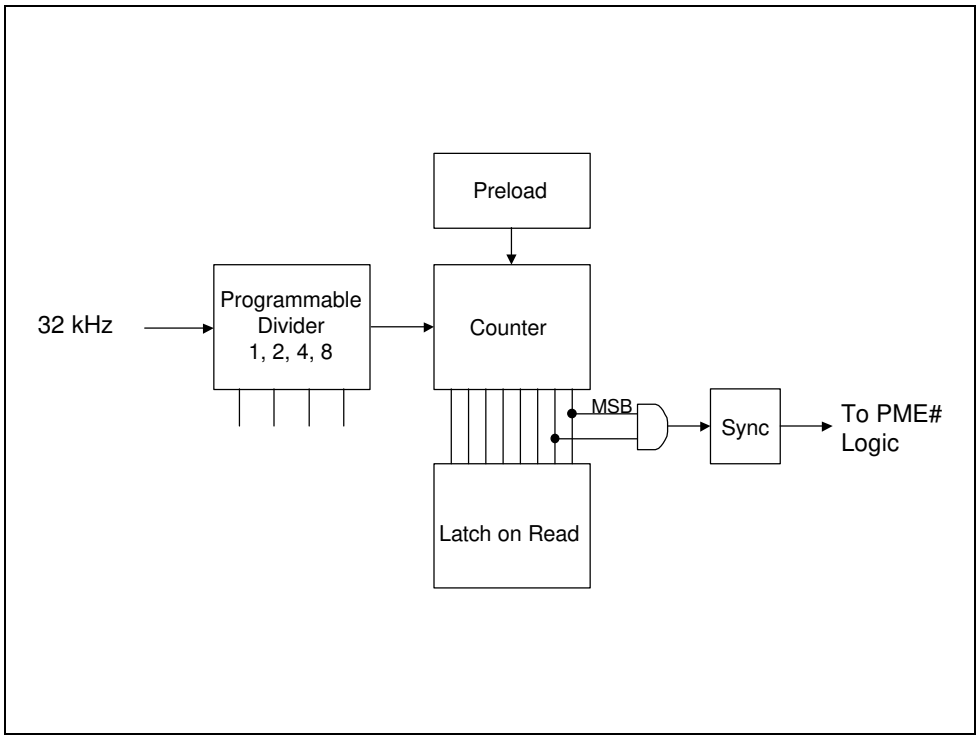
Term 1 in the equation above is determined by multiplying the clock source of 32.768kHz by 60sec/min and dividing by the product of the revolutions per minute times the divisor. The default divisor, located in the Fan Control Register, is 2. This results in a value for Term 1 in Equation 1 of 111 for a 4400 rpm.

The divisor for fan is programmable via the Fan Control Register, Logical Device 8, 0xFA. The choices for the divisor are 1, 2, 4 and 8. The default value is 2. The factor of ½ in Term 1 corresponds to two pulses per revolution.

The preload value is programmable via the FAN Preload Register. The preload is the initial value for the fan count which is used to adjust the count such that the value of 192 corresponds to the “lower limit” of the RPM. By setting the preload value and divisor properly, the PME or SMI will be generated when the RPM reaches the desired percentage of the nominal RPM to indicate a fan failure.

A PME or SMI is generated, if enabled through the PME or SMI enable register, at a count of 192, which corresponds to the “upper limit” for the fan count. This value is made to correspond to the “lower limit” of the RPM for the fan by programming the divisor and preload value accordingly. Typical practice is to consider 70% of normal RPM a fan failure, at which point Term 1 in Equation 1 for the example above will be 160. Therefore, the preload value is chosen to be 32 so that when the count reaches 192, this will correspond to 70% of the normal RPM for the generation of a PME or SMI.

A representation of the logic for the fan tachometer implementation is shown below.



The following tables show examples of the desired functionality. Counts are based on 2 pulses per revolution tachometer outputs with a default divisor of 2.

RPM	Time per Revolution	Term 1 for "Divide by 2" (Default) in Decimal	Preload	Count = (Term 1) + Preload	Comments
4400	13.64 ms	112 counts	32	144	Typical RPM
3080	19.48 ms	160 counts	32	192	70% RPM
2640	22.73 ms	186 counts	32	218	60% RPM
2204	27.22 ms	223 counts	32	255 (maximum count)	50% RPM

Mode Select	Nominal RPM	Time per Revolution	Preload	Counts for the Given Speed in Decimal	70% RPM	Time per Revolution for 70% RPM
Divide by 1	8800	6.82 ms	32	144	6160	9.74 ms
Divide by 2	4400	13.64 ms	32	144	3080	19.48 ms
Divide by 4	2200	27.27 ms	32	144	1540	38.96 ms
Divide by 8	1100	54.54 ms	32	144	770	77.92 ms

Pin 52 is the fan tachometer input FAN_TACH.
The Fan Tachometer Register and Fan Preload Register are defined in the "Runtime Registers" section.

SECURITY FEATURE

The following register describes the functionality to support security in the LPC47S42x.

GPIO Device Disable Register Control
The GPIO pin GP43 is used for the Device Disable Register Control (DDRC) function. Setting bits[3:2] of the GP43 configuration register to '01', selects the DDRC function for the GP43 pin. When bits[3:2]=01 the GP43 pin is an input, with non-inverted polarity. Bits[3:2] cannot be cleared by writing to these bits; they are cleared by VTR POR, VCC POR and Hard Reset. That is, when the DDRC function is selected for this pin, it cannot be changed, except by a VCC POR, hard reset or VTR POR.

When the DDRC function is selected for GP43, the Device Disable register is controlled by the value of the GP43 pin as follows:

- If the GP43 pin is high, the Device Disable Register is Read-Only.
- If the GP43 pin is low, the Device Disable Register is Read/Write.

Device Disable Register
The Device Disable Register is located in the PME register block at offset 0x22 from the RUNTIME REGISTERS BLOCK base I/O address in logical device A. Writes to this register are blocked when the GP43 pin is configured for the Device Disable Register Control function (GP43 configuration register bit 2 =1) and the GP43 pin is high.

The control register for device disable register is defined in the "Runtime Registers" section.

SMBus CONTROLLER

Overview

The LPC47S42x supports SMBus. SMBus is a serial communication protocol between a computer host and its peripheral devices. It provides a simple, uniform and inexpensive way to connect peripheral devices to a single computer port. A single SMBus on a host can accommodate up to 125 peripheral devices.

The SMBus protocol includes a physical layer based on the I^2C^{TM} serial bus developed by Philips, and several software layers. The software layers include the base protocol, the device driver interface, and several specific device protocols.

For a description of the SMBus protocol, please refer to the System Management Bus Specification Revision 1.0, February 15, 1995, available from Intel Corporation.

The SMBus can assert both an nIO_PME and an nIO_SMI event when enabled and following an SMBus interrupt. Refer to registers PME_STS6, PME_EN6, SMI_STS2 and SMI_EN2 in the Runtime Registers section for more information.

The SMBus implementation in the LPC47S42x has the following additions over the I^2C:

(1) Added Timeout Error (TE) Bit, in D6 of the SMBus Status Register.
(2) Added Timeout Interrupt Enable Bit D4 in the SMBus Control register.

Configuration Registers

See the configuration registers section for the SMBus Configuration Registers (Logical Device 0x0B).

Runtime Registers

Overview
The SMBus contains five registers: 1) Control, 2) Status, 3) Own Address, 4) Data, 5) Clock.

The five SMBus registers occupy four addresses in the Host I/O space (Table 50).

The Own Address register and the Clock register are used to initialize the SMBus controller. Normally these registers are written once following device reset.

The other registers are used during actual data transmission/reception. The Data register performs all serial-to-parallel interfacing. The Control/Status register contains status information required for bus access and/or monitoring.

Descriptions of these registers follow in the sections below.

Table 50 – SMBus Runtime Registers

	ISA HOST INTERFACE	
REGISTER NAME	**HOST INDEX**	**HOST TYPE**
Control	SMBus Base Address	W
Status	SMBus Base Address	R
Own Address	SMBus Base Address + 1	R/W
Data	SMBus Base Address + 2	R/W
Clock	SMBus Base Address + 3	R/W

Control Register

Overview
The Control/Status register manages the SMBus operation and provides operational status (Table 51). The Control/Status register is located at the SMBus Base Address.

The Control register is write-only and is located at the SMBus Base Address. The Control register provides register access control and control over SMBus signals.

The read-only component of the SMBus Base Address is the Status register, described in the Status Register section, below.

Table 51 - SMBus Control/Status Register (SMBus/Base Address)

CONTROL	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Type	W	W	W	W	W	W	W	W
Bit Def	PINC	ES0	Reserved	TIE	ENI	STA	STO	ACK
Default	0x00 on VTR POR, VCC POR, HARD RESET or SOFT RESET							
Status	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Type	R	R	R	R	R	R	R	R
Bit Def	PIN	TE	STS	BER	LRB	AAS	LAB	nBB
Default	0x81 on VTR POR, VCC POR, HARD RESET or SOFT RESET							

Bit 7 PINC
Control register bit D7 is the Pending Interrupt Not Control bit. Writing the PINC bit to a logic '1' deasserts all Status register bits except for bit D0 nBB (Bus Busy). NOTE: the PINC bit has no affect on the nBB bit.

The PINC bit is self-clearing. Writing this bit to a logic '0' has no effect.

Bit 6 ESO
Control register bit D6 is the Enable Serial Output control bit. ESO enables or disables the SMBus serial I/O.

When ESO is '1', SMBus serial communication is enabled; communication with serial shift data register is enabled and the bits in the Status register are available for reading.

Bit 5
RESERVED

Bit 4 TIE
The Timeout Interrupt Enable and the ENI bits determine whether or not an interrupt is generated as a result of an SMBus timeout error.

When the TIE bit is '1' and ENI is asserted, SMBus timeout errors will generate an interrupt.

When TIE is '0', SMBus timeout errors will not generate interrupts, regardless of the state of ENI. The TIE bit does not affect the Timeout Error bit TE in the Status register.

Bit 3 ENI
This bit enables the internal SMBus interrupt, nINT, which is generated when the PIN bit is asserted ('0').

Bit 2 and Bit 1 STA and STO
These bits control the generation of the SMBus Start condition and transmission of slave address and R/nW bit, generation of repeated Start condition, and generation of the STOP condition (see Table 52)

Table 52 - Instruction for Serial Bus Control

STA	STO	PRESENT MODE	FUNCTION	OPERATION
1	0	SLV/REC	START	Transmit START+address, remain MST/TRM if R/nW=0; go to MST/REC if R/nW=1.
1	0	MST/TRM	REPEAT START	Same as for SLV/REC
0	1	MST/REC; MST/TRM	STOP READ; STOP WRITE	Transmit STOP go to SLV/REC mode; Note 1
1	1	MST	DATA CHAINING	Send STOP, START and address after last master frame without STOP sent; Note 2
0	0	ANY	NOP	No operation; Note 3

Note 1: In master receiver mode, the last byte is terminated with ACK bit high ('negative acknowledge').
Note 2: If both STA and STO are set high simultaneously in master mode, a STOP condition followed by a START condition + address will be generated. This allows 'chaining' of transmissions without relinquishing bus control.
Note 3: All other STA and STO mode combinations not mentioned in Table 52 are NOPs.

Bit 0 ACK
This bit must be set normally to logic "1". This causes the SMBus to send an acknowledge automatically after each byte (this occurs during the 9th clock pulse). The bit must be reset (to logic "0") when the SMBus controller is operating in master/receiver mode and requires no further data to be sent from the slave transmitter. This causes a negative acknowledge on the SMBus, which halts further transmission from the slave device.

Status Register

Overview
The Status register, the read-only component of the SMBus Base Address, enables access to SMBus operational status information.

Bit 7 PIN
Pending Interrupt Not. This bit is a status flag which is used to synchronize serial communication and is set to logic "0" whenever the chip requires servicing. The PIN bit is normally read in polled applications to determine when an SMBus byte transmission/reception is completed.

When acting as transmitter, PIN is set to logic "1" (inactive) each time the data register is written. In receiver mode, the PIN bit is automatically set to logic "1" each time the data register is read.

After transmission or reception of one byte on the SMBus (nine clock pulses, including acknowledge) the PIN bit will be automatically reset to logic “0” (active) indicating a complete byte transmission/reception. When the PIN bit is subsequently set to logic “1” (inactive) all status bits will be reset to “0” on a BER (bus error) condition.

In polled applications, the PIN bit is tested to determine when a serial transmission/reception has been completed. When the ENI bit (bit 4 of write-only section of the control/status register) is also set to logic “1” the hardware interrupt is enabled. In this case, the PI flag also triggers and internal interrupt (active low) via the nINT output each time PIN is reset to logic “0”.

When acting as a slave transmitter or slave receiver, while PIN = “0”, the chip will suspend SMBus transmission by holding the SCLK line low until the PIN bit is set to logic “1” (inactive). This prevents further data from being transmitted or received until the current data byte in the data register has been read (when acting as slave receiver) or the next data byte is written to the data register (when acting as slave transmitter).

PIN Bit Summary

1. The PIN bit can be used in polled applications to test when a serial transmission has been completed. When the ENI bit is also set, the PIN flag sets the internal interrupt via the nINT output.
2. In transmitter mode, after successful transmission of one byte on the SMBus the PIN bit will be automatically reset to logic "0" (active) indicating a complete byte transmission.
3. In transmitter mode, PIN is set to logic "1" (inactive) each time the data register is written.
4. In receiver mode, PIN is set to logic "0" (inactive) on completion of each received byte.
5. Subsequently, the SCLK line will be held low until PIN is set to logic "1".
6. In receiver mode, when the data register is read, PIN is set to logic "1" (inactive).
7. In slave receiver mode, an SMBus STOP condition will set PIN=0 (active).
8. PIN=0 if a bus error (BER) or a timeout error (TE) occurs while the Timeout Interrupt Enable is asserted (TIE).

Bit 6 TE
When the Timeout Error bit D6 is '1', an SMBus timeout error has occurred (see Section **SMBus Timeout**).

Timeout errors generate an interrupt if the TIE bit is asserted (see Section on Bit 4 TIE). If the TIE bit is asserted, timeout errors will assert the PIN bit.

The TE bit is deasserted '0' whenever the PIN bit is deasserted (see Section on Bit 7 Pin).

Bit 5 STS
When in slave receiver mode, this flag is asserted when an externally generated STOP condition is detected (used only in slave receiver mode).

Bit 4 BER
Bus error; a misplaced START or STOP condition has been detected. Resets nBB (to logic "1"; inactive), sets PIN = "0" (active).

Bit 3 LRB/AD0
Last Received Bit or Address 0 (general call) bit. This status bit serves a dual function, and is valid only while PIN=0:

- LRB holds the value of the last received bit over the SMBus while AAS=0 (not addressed as slave). Normally this will be the value of the slave acknowledgment; thus checking for slave acknowledgment is done via testing of the LRB.
- ADO; when AAS = "1" (Addressed as slave condition) the SMBus controller has been addressed as a slave. Under this condition, this bit becomes the AD0 bit and will be set to logic "1" if the slave address received was the 'general call' (00h) address, or logic "0" if it was the SMBus controller's own slave address.

Bit 2 AAS
Addressed As Slave bit. Valid only when PIN=0. When acting as slave receiver, this flag is set when an incoming address over the SMBus matches the value in own address register (shifted by one bit) or if the SMBus 'general call' address (00h) has been received ('general call' is indicated when AD0 status bit is also set to logic "1").

Bit 1 LAB
Lost Arbitration Bit. This bit is set when, in multi-master operation, arbitration is lost to another master on the SMBus.

Bit 0 nBB
Bus Busy bit. This is a read-only flag indicating when the SMBus is in use. A zero indicates that the bus is busy, and access is not possible. This bit is set/reset (logic "1"/logic "0") by Start/Stop conditions.

Own Address Register
When the chip is addressed as slave, this register must be loaded with the 7-bit SMBus address to which the chip is to respond. During initialization, the own address register must be written to, regardless whether it is later used. The Addressed As Slave (AAS) bit in status register is set when this address is received (the value in the data register is compared with the value in own address register). Note that the data and own address registers are offset by one bit; hence, programming the own address register with a value of 55h will result in the value AAh being recognized as the chip's SMBus slave address.

- After reset, own address register has default address 00h.

Table 53 - SMBus Own Address Register (SMBus Base Address +1)

OWN ADDR	Bit	D7	D6	D5	D4	D3	D2	D1	D0
Default = 0x00 on VTR POR, VCC POR, Hard Reset or Soft Reset	Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit Def	Reserved	Slave Addr 6	Slave Addr 5	Slave Addr 4	Slave Addr 3	Slave Addr 2	Slave Addr 1	Slave Addr 0

Data Shift Register
The Data Register acts as serial shift register and read buffer interfacing to the SMBus. All read and write operations to/from the SMBus are done via this register. SMBus data is always shifted in or out of shift register.

In receiver mode the SMBus data is shifted into the shift register until the acknowledge phase. Further reception of data is inhibited (SCLK pin held low) until the data shift register is read.

In the transmitter mode data is transmitted to the SMBus as soon as it is written to the shift register if the serial I/O is enabled (ESO=1).

Table 54 - SMBus Data Register (SMBus Base Address +2)

Default	DATA	D7	D6	D5	D4	D3	D2	D1	D0
0x00 on VTR POR, VCC POR, Hard Reset or Soft Reset	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Register
Overview
The Clock Register controls the internal SMBus clock generator, the SMBus reset, and the SCLK pin clock frequency (Table 55).

The Clock register is 00H by default.

Table 55 - SMBus Clock Register (SMBus Base Address +3)

	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
TYPE	R/W	R	R	R	R	R/W	R/W	R	0x00 on VTR POR, VCC POR, Hard Reset or Soft Reset
NAME	SMB_RST (NOTE 1)	RESERVED				CLK_DIV	CLK_SEL	RESERVED	

NOTE 1: The SMBus reset bit is not self-clearing.

Bit 7 SMB_RST
The SMBus Reset bit D7 is used to reinitialize all the logic and registers in the SMBus block.

SMB_RST is active high and is not self-clearing. To properly reset the the SMBus block, write the SMB_RST bit to '1' and then re-write the SMB_RST bit to '0'; i.e., the SMB_RST bit must be '0' for normal device operation.

The SMB_RST bit is '0' by default.

Bit 6 – Bit 3
RESERVED

Bit 2 CLK_DIV
The CLK_DIV bit D2 is used to divide the SMBus input clock by two.

When CLK_DIV = '0' (default) the SMBus input clock is not divided; when CLK_DIV = '1', the SMBus input clock, as well as the SMBus output clock SCLK, is divided by two.

Bit 1 CLK_SEL
The CLK_SEL bit D1 is used to enable the SMBus input clock.

When CLK_SEL = '1', the SMBus inout clock is enabled and the SMBus block can operate normally; when CLK_SEL = '0' (default), the input clock is stopped and the SMBus will not run.

The SMBus output clock SCLK frequency is determined by the CLK_SEL and CLK_DIV bits (Table 56).

Table 56 – SMBus Clock Select Encoding

SMBUS CLOCK FREQUENCY CONTROLS		DESCRIPTION
CLK_SEL	CLK_DIV	
0	X	CLOCK OFF
1	0	SCLK = 100kHz
1	1	SCLK = 50kHz

Pin Multiplexing
- SDAT is multiplexed with pin GP32.
- SCLK is multiplexed with pin GP30.

SMBus Timeouts

Overview
The SMBus is designed to provide a predictable communications link between a system and its devices. However some devices, such as a Smart Battery using a microcontroller to support both bus and maintain battery data, may require more time than might normally be expected. The following specifications take such devices into account while maintaining a relatively predictable communications. The following are general comments on the SMBus' timing:
- The bus may be at 0 kHz when idle.
- The F_{SMB} Min is intended to dissuade components from taking too long to complete a transaction.
- An idle bus can be detected by observing that both the clock and data remain high for longer than T_{HIGH} Max.
- Every device must be able to recognize and react to a start condition at F_{SMB} Max.

The SMBus timing is in the Timing Diagrams section.

SMBus Timeout
The SMBus controller will timeout when any clock low (SCLK) exceeds the $T_{TIMEOUT}$ value shown in SMBus timing table above.

Timeout errors are identified using the TE bit in the SMBus Status register (see Status Register section).

Sample Transaction Diagram
The following figure illustrates a data transaction on the SMBus.

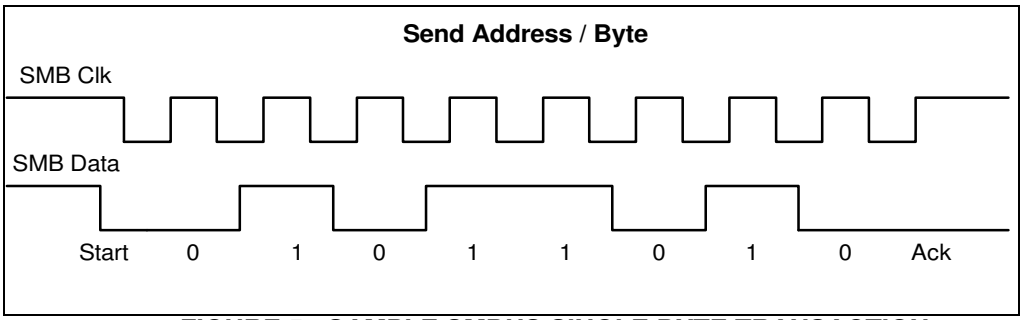


FIGURE 5 - SAMPLE SMBUS SINGLE BYTE TRANSACTION

X-BUS INTERFACE

The X-bus interface allows the LPC47S42x to interface to as many as 4 external components that have an 8 bit data bus and occupy up to 4 contiguous I/O address ports. Depending on the mode of operation, it provides either 4 separate active low chip selects (nXCS0 – nXCS3) and 2 address pins (XA0, XA1) or 2 active low chip selects (nXCS0, nXCS0) and 4 address pins (XA0-XA3). It also provides a read strobe (nXRD), a write strobe (nXWR) and an 8 bit data bus (XD0 – XD7). External pullups are required on the nXRD and nXWR pins.

The chip select outputs are generated by circuitry in the LPC47S42x that compares the LPC I/O address bits with the X-bus base I/O address configuration registers. The mode of operation determines the number of chip selects and address pins that the X-bus interface provides, as well as the number of bits in the base I/O addresses. The mode is chosen via bit 0 of the X-Bus Selection Configuration Register located in Logical Device 8 at 0xF0.

- In X-Bus Mode 1, the X-bus base I/O address configuration registers contain address bits A15 through A8 and A7 through A2, respectively. A1 and A0 pass directly through to XA1 and XA0, respectively. The chip selects only become active (low) for the LPC bus cycle in which the address match occurs.
- In X-Bus Mode 2, the X-bus base I/O address configuration registers contain address bits A15 through A8 and A7 through A4, respectively. A3, A2, A1 and A0 pass directly through to XA3, XA2, XA1 and XA0, respectively. The chip selects only become active (low) for the LPC bus cycle in which the address match occurs.

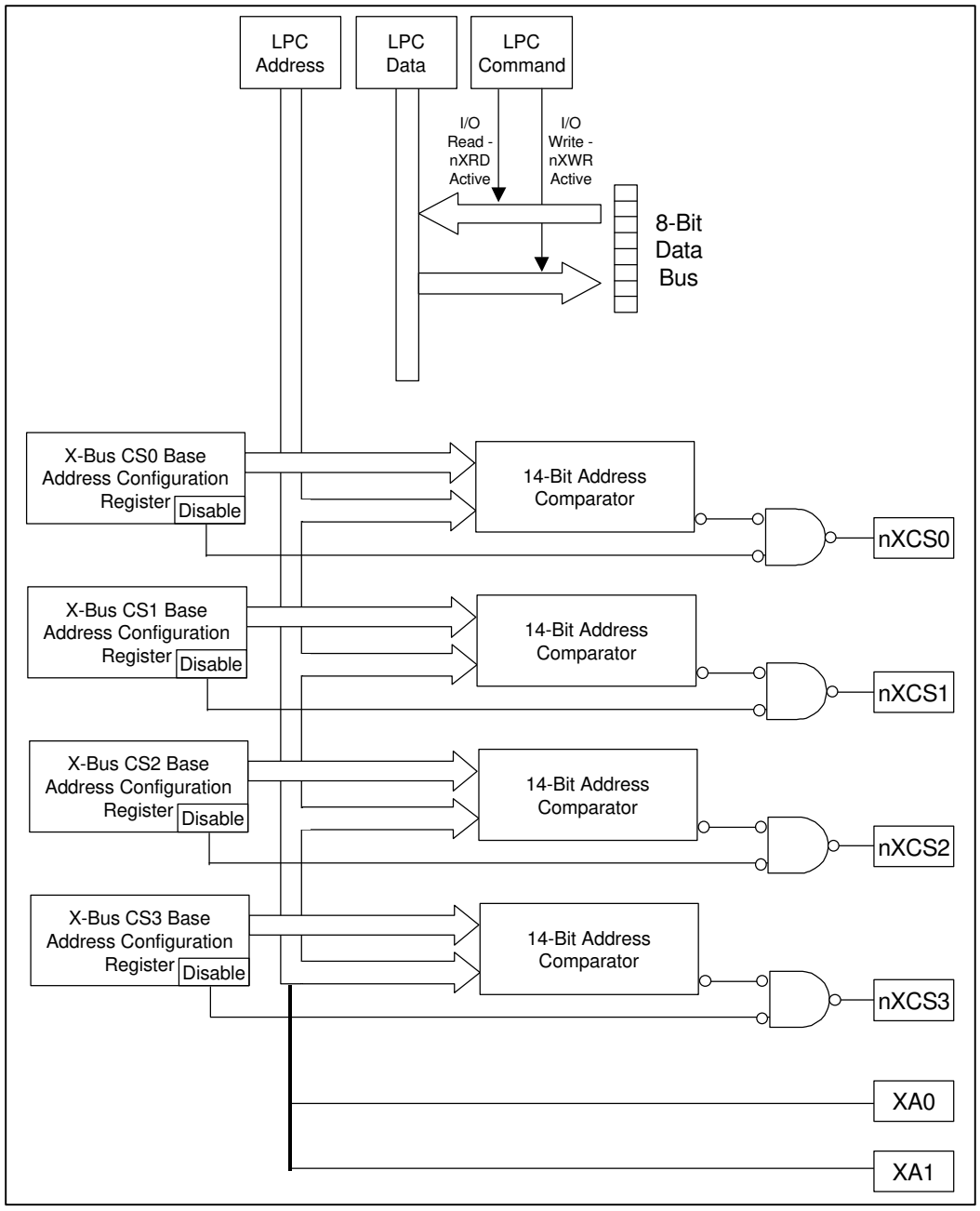
The LPC47S42x performs 16-bit address qualification on the X-Bus base I/O addresses. That is, the upper 4-bits, bits[15:12], must be '0'. Note: Bit 6 of the OSC Global Configuration Register (CR24) must be set to '1' for 16-bit address qualification.

The read and write strobes have address setup and hold times, and pulse widths, that are compatible with X-Bus timing of the Intel PIIX4. See the timing diagrams in the "Timing" section. The strobes will only become active during an LPC cycle in which the LPC address matches the corresponding X-bus address.

Each X-bus chip select has an associated disable bit. This bit allows each chip select to be individually enabled or disabled. This bit is part of the X-bus Low Address Byte Configuration register.

Each X-bus chip select base address register has an associated "write protect" bit that can only be set once, and is reset by VCC POR and hard reset (nPCI_RESET). When this bit is set, it prevents the base address configuration registers (high byte and low byte) for each chip select from being written. This security feature ensures that the base address and disable bit for each chip select can only be set by BIOS and cannot be corrupted by any virus software. This bit is part of the X-bus Low Address Byte Configuration register.

The following figure shows the X-Bus Interface in mode 1.



The following figure shows the X-bus interface in mode 2.

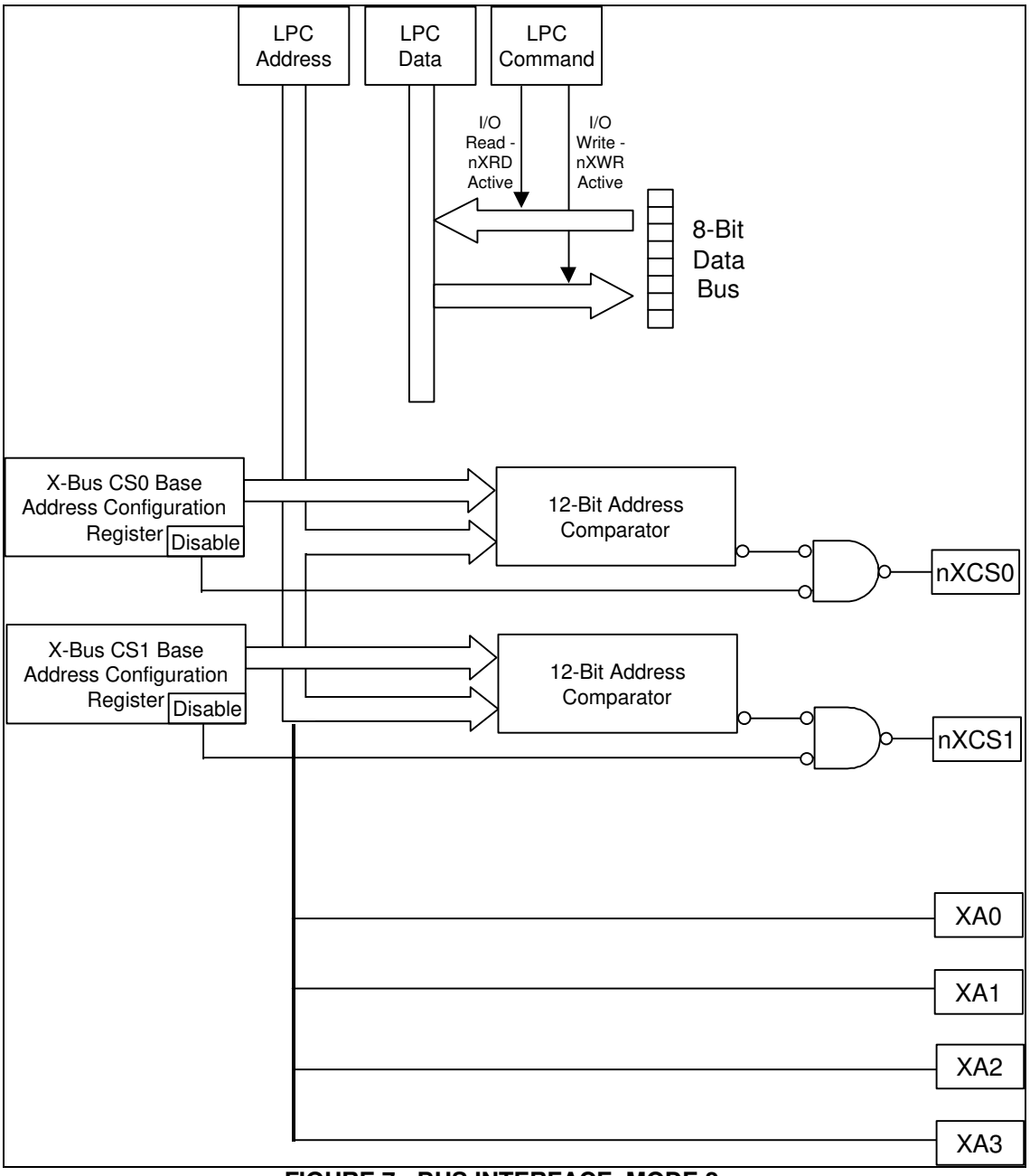


FIGURE 7 - BUS INTERFACE, MODE 2

See the “Timing” section for figures that show “representative” LPC I/O to X-bus cycle timing.

X-Bus Chip Select Base I/O Address Registers
The Base I/O Address Registers for the X-bus are defined in the “Configuration” section.

X-Bus Configuration Register
X-Bus Selection Register is used to select the X-bus mode and the pulse widths of the X-bus read and write strobes. This register is located in Logical Device 8 at an offset of 0xF0. See the Configuration section for register description.

RUNTIME REGISTERS

Runtime Registers Block Summary

The following registers are runtime registers in the LPC47S42x. They are located at the address programmed in the Base I/O Address in Logical Device A (Runtime Registers Block) at the offset shown. These registers are powered by VTR.

Table 57 - Runtime Register Block Summary

OFFSET (hex)	TYPE	HARD RESET	VCC POR	VTR POR	SOFT RESET	REGISTER
00	R/W	-	-	0x00	-	PME_STS
01	R	-	-	-	-	Reserved
02	R/W	-	-	0x00	-	PME_EN
03	R	-	-	-	-	Reserved
04	R/W	-	-	0x00	-	PME_STS1
05	R/W	-	-	0x00	-	PME_STS2
06	R/W	-	-	0x00	-	PME_STS3
07	R/W	-	-	0x00	-	PME_STS4
08	R/W	-	-	0x00	-	PME_STS5
09	R/W	Note 6	Note 6	0x01 Note 6	Note 6	PME_STS6
0A	R/W	-	-	0x00	-	PME_EN1
0B	R/W	-	-	0x00	-	PME_EN2
0C	R/W	-	-	0x00	-	PME_EN3
0D	R/W	-	-	0x00	-	PME_EN4
0E	R/W	-	-	0x00	-	PME_EN5
0F	R/W	-	-	0x00	-	PME_EN6
10	R/W	Note 6	Note 6	0x02 Note 6	Note 6	SMI_STS 1
11	R/W	-	-	0x00	-	SMI_STS 2
12	R/W	-	-	0x00	-	SMI_STS3
13	R/W	-	-	0x00	-	SMI_STS4
14	R/W	-	-	0x00	-	SMI_STS5
15	R/W	-	-	0x00	-	SMI_STS6
16	R/W	-	-	0x00	-	SMI_EN1
17	R/W	-	-	0x00	-	SMI_EN2
18	R/W	-	-	0x00	-	SMI_EN3
19	R/W	-	-	0x00	-	SMI_EN4
1A	R/W	-	-	0x00	-	SMI_EN5
1B	R/W	-	-	0x00	-	SMI_EN6
1C	R/W	-	-	0x00	-	MSC_STS
1D	R	0x00	0x00	0x00	-	UART2 FIFO Control Shadow
1E	R/W	0x03	0x03	-	-	Force Disk Change
1F	R	0x02	0x02	0x02	-	Floppy Data Rate Select Shadow
20	R	0x00	0x00	0x00	-	UART1 FIFO Control Shadow
21	R/W	-	-	0x00	-	Edge Select Register

OFFSET (hex)	TYPE	HARD RESET	VCC POR	VTR POR	SOFT RESET	REGISTER
22	R/W[Note 3]	-	-	0x00	-	Device Disable Register
23	R/W	-	-	0x01	-	GP10
24	R/W	-	-	0x01	-	GP11
25	R/W	-	-	0x01	-	GP12
26	R/W	-	-	0x01	-	GP13
27	R/W	-	-	0x01	-	GP14
28	R/W	-	-	0x01	-	GP15
29	R/W	-	-	0x01	-	GP16
2A	R/W	-	-	0x01	-	GP17
2B	R/W	-	-	0x01	-	GP20
2C	R/W	-	-	0x01	-	GP21
2D	R/W	-	-	0x01	-	GP22
2E	R/W	-	-	0x01	-	GP23
2F	R/W	-	-	0x01	-	GP24
30	R/W	-	-	0x01	-	GP25
31	R/W	-	-	0x01	-	GP26
32	R/W	-	-	0x01	-	GP27
33	R/W	-	-	0x01	-	GP30
34	R/W	-	-	0x01	-	GP31
35	R/W	-	-	0x01	-	GP32
36	R/W	0x00	0x00	0x01	-	GP33
37	R/W	-	-	0x01	-	GP34
38	R/W	-	-	0x01	-	GP35
39	R/W	-	-	0x01	-	GP36
3A	R/W	-	-	0x01	-	GP37
3B	R/W	-	-	0x01	-	GP40
3C	R/W	-	-	0x01	-	GP41
3D	R/W	-	-	0x01	-	GP42
3E	R/W	-[Note 5]	-[Note 5]	0x01	-	GP43
3F	R/W	-	-	0x01	-	GP50
40	R/W	-	-	0x01	-	GP51
41	R/W	-	-	0x01	-	GP52
42	R/W	0x00	0x00	0x00	-	GP53
43	R/W	-	-	0x01	-	GP54
44	R/W	-	-	0x01	-	GP55
45	R/W	-	-	0x01	-	GP56
46	R/W	-	-	0x01	-	GP57
47	R/W	-	-	0x01	-	GP60
48	R/W	-	-	0x04	-	GP61
49	R/W	-	-	0x01	-	GP62
4A	R	-	-	-	-	Reserved – read returns 0
4B	R/W	-	-	0x00	-	GP1
4C	R/W	-	-	0x00	-	GP2
4D	R/W	-[Note 4]	-[Note 4]	0x00	-	GP3

OFFSET (hex)	TYPE	HARD RESET	VCC POR	VTR POR	SOFT RESET	REGISTER
4E	R/W	-	-	0x00	-	GP4
4F	R/W	-	-	0x00	-	GP5
50	R/W	-	-	0x00	-	GP6
51	R	-	-	-	-	Reserved – read returns 0
52	R/W	0x00	0x00	0x00	-	WDT_TIME_OUT
53	R/W	0x00	0x00	0x00	-	WDT_VAL
54	R/W	0x00	0x00	0x00	-	WDT_CFG
55	R/W[Note 1]	0x00 Note 2	0x00	0x00	-	WDT_CTRL
56	R/W	-	-	0x00	-	FAN
57	R/W	-	-	-	-	Reserved – read returns 0
58	R/W	-	-	0x10	-	Fan Control
59	R	-	-	0x00	-	Fan Tachometer
5A	R	-	-	-	-	Reserved – read returns 0
5B	R/W	-	-	0x00	-	Fan Preload
5C	R/W	-	-	-	-	Reserved – read returns 0
5D	R/W	-	-	0x00	-	LED1
5E	R/W	-	-	0x01	-	LED2
5F	R/W	-	-	0x00	-	Keyboard Scan Code
60	R/W	-	-	0x00	-	PM1_CNTRL1
61	R/W	-	-	0x00	-	PM1_CNTRL2
62	R	-	-	-	-	Reserved – read returns 0
63	R	-	-	-	-	Reserved – read returns 0
64	R/W	-	-	0x00	-	SMI_STS7
65	R	-	-	-	-	Reserved – read returns 0
66	R/W	-	-	0x00	-	SMI_EN7
67	R	-	-	-	-	Reserved – read returns 0
68	R/W	-	-	0x00	-	PME_STS7
69	R	-	-	-	-	Reserved – read returns 0
6A	R	-	-	-	-	Reserved – read returns 0
6B	R	-	-	-	-	Reserved – read returns 0
6C	R/W	-	-	0x00	-	PME_EN7
6D-7F	R	-	-	-	-	Reserved – read returns 0

Note. Reserved bits return 0 on read.
Note 1: This register contains some bits that are read or write only.
Note 2: Bit 0 is not cleared by HARD RESET.
Note 3: The Device Disable Register is read-only when GP43 register bit [3:2] = 01 AND the GP43 pin is high, or when bit 1 of the Device Disable Register is '1'.

Note 4: Bit [3] of this register is reset (cleared) on VCC POR and Hard Reset (and VTR POR), for fan output default at power-up.
Note 5: Bits [3:2] of the GP43 register are reset (cleared) on VCC POR and Hard Reset (and VTR POR).
Note 6: The parallel port interrupt defaults to 1 when the parallel port activate bit is cleared. When the parallel port is activated, PINT follows the nACK input.

Runtime Registers Block Description

Table 58 - Runtime Registers Block Description

Note: Reserved bits return 0 on read.

NAME	REG OFFSET (hex)	DESCRIPTION
PME_STS Default = 0x00 on VTR POR	00 (R/W)	Bit[0] PME_Status = 0 (default) = 1 Set when The chip would normally assert the nIO_PME signal, independent of the state of the PME_En bit. Bit[7:1] Reserved PME_Status is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to PME_Status will clear it and cause the The chip to stop asserting nIO_PME, if enabled. Writing a “0” to PME_Status has no effect.
PME_EN Default = 0x00 on VTR POR	02 (R/W)	Bit[0] PME_En = 0 nIO_PME signal assertion is disabled (default) = 1 Enables The chip to assert nIO_PME signal Bit[7:1] Reserved PME_En is not affected by Vcc POR, SOFT RESET or HARD RESET
PME_STS1 Default = 0x00 on VTR POR	04 (R/W)	PME Wake Status Register 1 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] P12 Bit[1] P16 Bit[2] nRI1 Bit[3] KBD Bit[4] MOUSE Bit[5] SPEKEY (Wake on specific key) Bit[6] FAN_TACH Bit[7] nRI2 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.

NAME	REG OFFSET (hex)	DESCRIPTION
PME_STS2 Default = 0x00 on VTR POR	05 (R/W)	PME Wake Status Register 2 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.
PME_STS3 Default = 0x00 on VTR POR	06 (R/W)	PME Wake Status Register 3 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP23 Bit[4] GP24 Bit[5] GP25 Bit[6] GP26 Bit[7] GP27 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.

NAME	REG OFFSET (hex)	DESCRIPTION
PME_STS4 Default = 0x00 on VTR POR	07 (R/W)	PME Wake Status Register 4 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP41 Bit[5] GP43 Bit[6] GP60 Bit[7] GP61 The PME Wake Status register is not affected by VCC POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.
PME_STS5 Default = 0x00 on VTR POR	08 (R/W)	PME Wake Status Register 5 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.

NAME	REG OFFSET (hex)	DESCRIPTION
PME_STS6 Default = 0x01 on VTR POR Bit 0 is set to '1' on VCC POR, VTR POR, HARD RESET and SOFT RESET	09 (R/W)	This register indicates the state of the individual PME sources, independent of the individual source enables or the PME_En bit. If the PME source has asserted an event, the associated PME Status bit will be a "1". Bit[0] PINT The parallel port interrupt defaults to '1' when the parallel port activate bit is cleared. When the parallel port is activated, PINT follows the nACK input. Bit[1] U2INT Bit[2] U1INT Bit[3] FINT Bit[4] MINT Bit[5] KINT Bit[6] WDT Bit[7] SMB The PME Status register is not affected by VCC POR, SOFT RESET or HARD RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Status Register has no effect.
PME_EN1 Default = 0x00 on VTR POR	0A (R/W)	PME Wake Enable Register 1 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_En bit is "1", the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] P12 Bit[1] P16 Bit[2] nRI1 Bit[3] KBD Bit[4] MOUSE Bit[5] SPEKEY (Wake on specific key) Bit[6] FAN_TACH Bit[7] nRI2 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.

NAME	REG OFFSET (hex)	DESCRIPTION
PME_EN2 Default = 0x00 on VTR POR	0B (R/W)	PME Wake Enable Register 2 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.
PME_EN3 Default = 0x00 on VTR POR	0C (R/W)	PME Wake Status Register 3 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP23 Bit[4] GP24 Bit[5] GP25 Bit[6] GP26 Bit[7] GP27 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.

NAME	REG OFFSET (hex)	DESCRIPTION
PME_EN4 Default = 0x00 on VTR POR	0D (R/W)	PME Wake Enable Register 4 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP41 Bit[5] GP43 Bit[6] GP60 Bit[7] GP61 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.
PME_EN5 Default = 0x00 on VTR POR	0E (R/W)	PME Wake Enable Register 5 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.

NAME	REG OFFSET (hex)	DESCRIPTION
PME_EN6 Default = 0x00 on VTR POR	0F (R/W)	PME Enable Register 6 This register enables the individual PME sources onto the PME_ST bus. When the enable bit is '1' and the PME source has asserted a wake event, the PME_ST bus is asserted. The PME_ST bus cannot be asserted if the enable bit is '0'. Bit[0] PINT Bit[1] U2INT Bit[2] U1INT Bit[3] FINT Bit[4] MINT Bit[5] KINT Bit[6] WDT Bit[7] SMB
SMI_STS1 Default = 0x02 on VTR POR Bit 1 is set to '1' on VCC POR, VTR POR, hard reset and soft reset	10 (R/W)	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits must be cleared at their source. Bit[0] Reserved Bit[1] PINT The parallel port interrupt defaults to 1 when the parallel port activate bit is cleared. When the parallel port is activated, PINT follows the nACK input. Bit[2] U2INT Bit[3] U1INT Bit[4] FINT Bit[5] Reserved Bit[6] Reserved Bit[7] WDT
SMI_STS2 Default = 0x00 on VTR POR	11 (R/W)	SMI Status Register 2 This register is used to read the status of the SMI inputs. Bits 2-6 are cleared by a write of 1 to the bit. Bit[0] MINT. Cleared at source. Bit[1] KINT. Cleared at source. Bit[2] SMB Bit[3] nRI1 Bit[4] P12. Status bit is cleared by a write of '1'. The SMI event is cleared at the source. Bit[5] nRI2 Bit[6] Reserved Bit[7] Reserved

NAME	REG OFFSET (hex)	DESCRIPTION
SMI_STS3 Default = 0x00 on VTR POR	12 (R/W)	SMI Status Register 3 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP60 Bit[4] GP24 Bit[5] GP25 Bit[6] GP26 Bit[7] GP27
SMI_STS4 Default = 0x00 on VTR POR	13 (R/W)	SMI Status Register 4 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP41 Bit[5] FAN_TACH Bit[6] GP43 Bit[7] GP61
SMI_STS5 Default = 0x00 on VTR POR	14 (R/W)	SMI Status Register 5 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57

NAME	REG OFFSET (hex)	DESCRIPTION
SMI_STS6 Default = 0x00 on VTR POR	15 (R/W)	SMI Status Register 6 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17
SMI_EN1 Default = 0x00 on VTR POR	16 (R/W)	SMI Enable Register 1 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] Reserved Bit[1] EN_PINT Bit[2] EN_U2INT Bit[3] EN_U1INT Bit[4] EN_FINT Bit[5] Reserved Bit[6] Reserved Bit[7] EN_WDT
SMI_EN2 Default = 0x00 on VTR POR	17 (R/W)	SMI Enable Register 2 This register is used to enable the different interrupt sources onto the group nSMI output, and the group nSMI output onto the nIO_SMI GPI/O pin or the serial IRQ stream. Unless otherwise noted, 1=Enable 0=Disable Bit[0] EN_MINT Bit[1] EN_KINT Bit[2] EN_SMB Bit[3] EN_nRI1 Bit[4] EN_P12 Bit[5] nEN_RI2 Bit[6] EN_SMI_S Bit[7] EN_SMI

NAME	REG OFFSET (hex)	DESCRIPTION
SMI_EN3 Default = 0x00 on VTR POR	18 (R/W)	SMI Enable Register 3 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP60 Bit[4] GP24 Bit[5] GP25 Bit[6] GP26 Bit[7] GP27
SMI_EN4 Default = 0x00 on VTR POR	19 (R/W)	SMI Enable Register 4 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP41 Bit[5] FAN_TACH Bit[6] GP43 Bit[7] GP61
SMI_EN5 Default = 0x00 on VTR POR	1A (R/W)	SMI Enable Register 5 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57

NAME	REG OFFSET (hex)	DESCRIPTION
SMI_EN6 Default = 0x00 on VTR POR	1B (R/W)	SMI Enable Register 6 This register enables the individual SMI sources onto the SMI_ST bus. When the enable bit is '1' and the SMI source has asserted an SMI event, the SMI_ST bus is asserted. The SMI_ST bus cannot be asserted if the enable bit is '0'. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17
MSC_STS Default = 0x00 on VTR POR	1C (R/W)	Miscellaneous Status Register Bits[5:0] can be cleared by writing a 1 to their position (writing a 0 has no effect). Bit[0] Either Edge Triggered Interrupt Input 0 Status. This bit is set when an edge occurs on the GP21 pin. Bit[1] Either Edge Triggered Interrupt Input 1 Status. This bit is set when an edge occurs on the GP22 pin. Bit[2] Either Edge Triggered Interrupt Input 2 Status. This bit is set when an edge occurs on the GP41 pin. Bit[3] Either Edge Triggered Interrupt Input 3 Status. This bit is set when an edge occurs on the GP43 pin. Bit[4] Either Edge Triggered Interrupt Input 4 Status. This bit is set when an edge occurs on the GP60 pin. Bit[5] Either Edge Triggered Interrupt Input 5 Status. This bit is set when an edge occurs on the GP61 pin. Bit[7:6] Reserved. This bit always returns zero.
UART2 FIFO Control Shadow Default = 0x00 on VCC POR, VTR POR and HARD RESET	1D (R)	UART FIFO Control Shadow 2 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)

NAME	REG OFFSET (hex)	DESCRIPTION
Force Disk Change Default = 0x03 on VCC POR and HARD RESET	1E (R/W)	Force Change 1 and Force Change 0 can be written to 1 are not clearable by software. Force Change 1 is cleared on (nSTEP AND nDS1) Force Change 0 is cleared on (nSTEP AND nDS0). DSK CHG (FDC DIR Register, Bit 7) = (nDS0 AND Force Change 0) OR (nDS1 AND Force Change 1) OR nDSKCHG. Setting either of the Force Disk Change bits active (1) forces the FDD nDSKCHG input active when the appropriate drive has been selected. Bit[0] Force Change for FDC0 0=Inactive 1=Active Bit[1] Force Change for FDC1 0=Inactive 1=Active Bit[7:2] Reserved, Reads 0
Floppy Data Rate Select Shadow Default = 0x02 on VCC POR, VTR POR and HARD RESET	1F (R)	Floppy Data Rate Select Shadow Bit[0] Data Rate Select 0 Bit[1] Data Rate Select 1 Bit[2] PRECOMP 0 Bit[3] PRECOMP 1 Bit[4] PRECOMP 2 Bit[5] Reserved Bit[6] Power Down Bit[7] Soft Reset
UART1 FIFO Control Shadow Default = 0x00 on VCC POR, VTR POR and HARD RESET	20 (R)	UART FIFO Control Shadow 1 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)

NAME	REG OFFSET (hex)	DESCRIPTION
Edge Select Register Default = 0x00 on VTR POR	21 (R/W)	Bit[0] EDGE_P12_SMI 0= P12 SMI status bit is set on the high-to-low edge of P1.2 1= P12 SMI status bit is set on both the high-to-low and low-to-high edge of P1.2 Bit[1] EDGE_P16_SMI 0= P16 SMI status bit is set on the high-to-low edge of P1.6 1= P16 SMI status bit is set on both the high-to-low and low-to-high edge of P1.6 Bit[2] EDGE_P12_PME 0= P12 PME status bit is set on the high-to-low edge of P1.2 1= P12 PME status bit is set on both the high-to-low and low-to-high edge of P1.2 Bit[3] EDGE_P16_PME 0= P16 PME status bit is set on the high-to-low edge of P1.6 1= P16 PME status bit is set on both the high-to-low and low-to-high edge of P1.6 Bits[7:4] Reserved

NAME	REG OFFSET (hex)	DESCRIPTION
Device Disable Register Default = 0x00 VTR POR	22 Read/Write when GP43 register bits[3:2] = 01 AND GP43 pin = 0 OR GP43 register bits[3:2] ≠ 01 (Device Disable Register Bit[1] must be 0) READ-ONLY When GP43 register bits[3:2] =01 AND GP43 pin = 1 OR Device Disable Register Bit[1]=1	If “0” (enabled), bits[7:3] have no effect on the devices; devices are controlled by their respective activate bits. If “1” (disabled), bits[7:3] override the activate bits in the configuration registers for each logical block. Bit[0] Floppy Write Protect. 0= No effect: floppy write protection is controlled by the write protect pin or the Forced Write Protect bit (bit 0 of register 0xF1 in Logical Device 0); 1= Write Protected. If set to 1, this bit overrides the write protect pin on the part and the forced write protect bit. nWRTPRT (to the FDC Core) = WP (FDC SRA Register, Bit 1) = (Floppy Write Protect) OR nWRTPRT(from the FDD Interface) OR (nDS0 AND Force Write Protect) OR (nDS1 AND Force Write Protect). Note: The Force Write Protect bit is in the FDD Option Configuration register. Bit[1] Register Lock This bit is cleared on VCC POR and Hard Reset. 0 - No effect (Default) 1 - All of the bits in this register are Read Only until a VCC POR or Hard Reset Bits[2] Reserved. Return 0 on read. Bit[3]: Floppy Enable. 0=No effect: FDC controlled by its activate bit; 1=Floppy Disabled Bit[4] Reserved Bit[5] Serial Port 2 Enable 0=No effect: UART2 controlled by its activate bit; 1=UART2 Disabled Bit[6] Serial Port 1 Enable. 0=No effect: UART1 controlled by its activate bit; 1=UART1 Disabled Bit[7] Parallel Port Enable. 0=No effect: PP controlled by its activate bit; 1=PP Disabled

NAME	REG OFFSET (hex)	DESCRIPTION
GP10 Default = 0x01 on VTR POR	23 (R/W)	General Purpose I/0 bit 1.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=XD0 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP11 Default = 0x01 on VTR POR	24 (R/W)	General Purpose I/0 bit 1.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=XD1 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP12 Default = 0x01 on VTR POR	25 (R/W)	General Purpose I/0 bit 1.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity :=1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=XD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP13 Default = 0x01 on VTR POR	26 (R/W)	General Purpose I/0 bit 1.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=XD3 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP14 Default = 0x01 on VTR POR	27 (R/W)	General Purpose I/0 bit 1.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=XD4 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP15 Default = 0x01 on VTR POR	28 (R/W)	General Purpose I/0 bit 1.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=XD5 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP16 Default = 0x01 on VTR POR	29 (R/W)	General Purpose I/0 bit 1.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=XD6 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP17 Default = 0x01 on VTR POR	2A (R/W)	General Purpose I/0 bit 1.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=XD7 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP20 Default = 0x01 on VTR POR	2B (R/W)	General Purpose I/0 bit 2.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=nDS1 – Floppy Drive select 1 (Note 3) 01=8042 P17 function (User Note 2) 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP21 Default =0x01 on VTR POR	2C (R/W)	General Purpose I/0 bit 2.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=8042 P12 function (Eng. Note 1) (User Note 2) 10=Either Edge Triggered Interrupt Input 0 (Note 1) (Eng. Note 3) 01=8042 P16 function (User Note 2) 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP22 Default =0x01 on VTR POR	2D (R/W)	General Purpose I/0 bit 2.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= nMRT1 – floppy motor select 1 (Note 3) 10= Either Edge Triggered Interrupt Input 1 (Note 1) 01=8042 P12 function (User Note 2) 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP23 Default=0x01 on VTR POR	2E (R/W)	General Purpose I/0 bit 2.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= IRQIND (IRQ Input D) 0= Basic GPIO Function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP24 Default = 0x01 on VTR POR	2F (R/W)	General Purpose I/0 bit 2.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP25 Default = 0x01 on VTR POR	30 (R/W)	General Purpose I/0 bit 2.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= nXRD (X-Bus Read Strobe) 0= Basic GPIO Function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP26 Default = 0x01 on VTR POR	31 (R/W)	General Purpose I/0 bit 2.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= nXWR (X-Bus Write Strobe) 0= Basic GPIO Function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP27 Default = 0x01 on VTR POR	32 (R/W)	General Purpose I/0 bit 2.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nIO_SMI (Note 4) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP30 Default = 0x01 on VTR POR	33 (R/W)	General Purpose I/0 bit 3.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity :=1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= XA2 (X-Bus Address 2) 10= nXCS2 (X-Bus Chip Select 2) 01= SCLK – SMBus CLOCK 00= GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP31 Default = 0x01 on VTR POR	34 (R/W)	General Purpose I/0 bit 3.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= XA3 (X-Bus Address 3) 10= nXCS3 (X-Bus Chip Select 3) 01= FAN_TACH 00= GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP32 Default = 0x01 on VTR POR	35 (R/W)	General Purpose I/0 bit 3.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= Reserved 10= XA0 (X-Bus Address 0) 01= SDAT 00= Basic GPIO Function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP33 Default = 0x01 on VTR POR Default = 0x00 on VCC POR and Hard Reset (Note 2)	36 (R/W)	General Purpose I/0 bit 3.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= Reserved 10= XA1 (X-Bus Address 1) 01=nFAN 00=Basic GPIO Function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP34 Default = 0x01 on VTR POR	37 (R/W)	General Purpose I/0 bit 3.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=IRQINA (IRQ Input A) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP35 Default = 0x01 on VTR POR	38 (R/W)	General Purpose I/0 bit 3.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=IRQINB (IRQ Input B) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP36 Default = 0x01 on VTR POR	39 (R/W)	General Purpose I/0 bit 3.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= nKBDRST 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP37 Default = 0x01 on VTR POR	3A (R/W)	General Purpose I/0 bit 3.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=A20M 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP40 Default =0x01 on VTR POR	3B (R/W)	General Purpose I/0 bit 4.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=DRVDEN0 (Note 3) 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP41 Default =0x01 on VTR POR	3C (R/W)	General Purpose I/0 bit 4.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=nXCS0 (X-Bus Chip Select 0) 10=Either Edge Triggered Interrupt Input 2 01=DRVDEN1 (Note 3) 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP42 Default =0x01 on VTR POR	3D (R/W)	General Purpose I/0 bit 4.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nIO_PME Note: Configuring this pin function as output with non-inverted polarity will give an active low output signal. The output type can be either open drain or push-pull. 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP43 Default = 0x01 on VTR POR Bits[3:2] are reset (cleared) on VCC POR, VTR POR and Hard Reset	3E (R/W)	General Purpose I/0 bit 4.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Either Edge Triggered Interrupt Input 3 10=nXCS1 (X-Bus Chip Select 1) 01=Device Disable Register Control. The GP43 pin is an input, with non-inverted polarity. When bits[3:2]=01, they cannot be changed by writing to these bits; they are cleared by VCC POR, Hard Reset and VTR POR. That is, when the DDRC function is selected for this pin, it cannot be changed, except by a VCC POR, Hard Reset or VTR POR. The Device Disable register is controlled by the value of the GP43 pin as follows: If the GP43 pin is high, the Device Disable Register is Read-Only. If the GP43 pin is low, the Device Disable Register is Read/Write, if bit 1 of the Device Disable Register is cleared (0). 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP50 Default = 0x01 on VTR POR	3F (R/W)	General Purpose I/0 bit 5.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= nRI2 (User Note 1) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP51 Default = 0x01 on VTR POR	40 (R/W)	General Purpose I/0 bit 5.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= nDCD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP52 Default = 0x01 on VTR POR	41 (R/W)	General Purpose I/0 bit 5.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=IRRX (Note 5) 01=RXD2 (Note 5) 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP53 Default = 0x00 on VTR POR, VCC POR and HARD RESET (Note 2)	42 (R/W)	General Purpose I/0 bit 5.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=IRTX (Note 5) 01=TXD2 (Note 5) 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP54 Default = 0x01 on VTR POR	43 (R/W)	General Purpose I/0 bit 5.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= nDSR2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP55 Default = 0x01 on VTR POR	44 (R/W)	General Purpose I/0 bit 5.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= nRTS2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP56 Default = 0x01 on VTR POR	45 (R/W)	General Purpose I/0 bit 5.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= nCTS2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP57 Default = 0x01 on VTR POR	46 (R/W)	General Purpose I/0 bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= nDTR2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP60 Default = 0x01 on VTR POR	47 (R/W)	General Purpose I/0 bit 6.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=Either Edge Triggered Interrupt Input 4 (Note 1) 01=LED1 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP61 Default = 0x04 on VTR POR (Note 6)	48 (R/W)	General Purpose I/0 bit 6.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=Either Edge Triggered Interrupt Input 5 (Note 1) 01=LED2 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP62 Default = 0x01 on VTR POR	49 (R/W)	General Purpose I/0 bit 6.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=IRQINC (IRQ Input C) 01=P17 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP1 Default = 0x00 on VTR POR	4B (R/W)	General Purpose I/0 Data Register 1 Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17

NAME	REG OFFSET (hex)	DESCRIPTION
GP2 Default = 0x00 on VTR POR	4C (R/W)	General Purpose I/0 Data Register 2 Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP23 Bit[4] GP24 Bit[5] GP25 Bit[6] GP26 Bit[7] GP27
GP3 Default = 0x00 on VTR POR Bits 3 is reset on VCC POR, Hard Reset and VTR POR	4D (R/W)	General Purpose I/0 Data Register 3 Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] GP35 Bit[6] GP36 Bit[7] GP37
GP4 Default = 0x00 on VTR POR	4E (R/W)	General Purpose I/0 Data Register 4 Bit[0] GP40 Bit[1] GP41 Bit[2] GP42 Bit[3] GP43 Bit[7:4] Reserved
GP5 Default = 0x00 on VTR POR Bit[3] is reset on VTR POR, VCC POR and HARD RESET	4F (R/W)	General Purpose I/0 Data Register 5 Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57
GP6 Default = 0x00 on VTR POR	50 (R/W)	General Purpose I/0 Data Register 6 Bit[0] GP60 Bit[1] GP61 Bit[2] GP62 Bit[7-3] Reserved
WDT_TIME_OUT Default = 0x00 on VCC POR, VTR POR, VTR POR and Hard Reset	52 (R/W)	Watch-dog Timeout Bit[0] Reserved Bit[1] Reserved Bits[6:2] Reserved, = 00000 Bit[7] WDT Time-out Value Units Select = 0 Minutes (default) = 1 Seconds

NAME	REG OFFSET (hex)	DESCRIPTION
WDT_VAL Default = 0x00 on VCC POR, VTR POR, VTR POR and Hard Reset	53 (R/W)	Watch-dog Timer Time-out Value Binary coded, units = minutes (default) or seconds, selectable via Bit[7] of the WDT_TIME_OUT register. 0x00 Time out disabled 0x01 Time-out = 1 minute (second) ..... 0xFF Time-out = 255 minutes (seconds)
WDT_CFG Default = 0x00 on VCC POR, VTR POR, VTR POR and Hard Reset	54 (R/W)	Watch-dog timer Configuration Bit[0] Joy-Stick Enable =1 WDT is reset upon an I/O read or write of Port 201h =0 WDT is not affected by I/O reads or writes to Port 201h. Bit[1] Keyboard Enable =1 WDT is reset upon a Keyboard interrupt. =0 WDT is not affected by Keyboard interrupts. Bit[2] Mouse Enable =1 WDT is reset upon a Mouse interrupt. =0 WDT is not affected by Mouse interrupts. Bit[3] Reserved Bits[7:4] WDT Interrupt Mapping 1111 = IRQ15 ..... 0011 = IRQ3 0010 = Invalid 0001 = IRQ1 0000 = Disable

NAME	REG OFFSET (hex)	DESCRIPTION
WDT_CTRL Default = 0x00 on VCC POR, VTR POR, VTR POR and Hard Reset	55 (R/W)	Watch-dog timer Control Bit[0] Watch-dog Status Bit, R/W =1 WD timeout occurred =0 WD timer counting Bit[1] Reserved Bit[2] Force Timeout, W =1 Forces WD timeout event; this bit is self-clearing Bit[3] P20 Force Timeout Enable, R/W = 1 Allows rising edge of P20, from the Keyboard Controller, to force the WD timeout event. A WD timeout event may still be forced by setting the Force Timeout Bit, bit 2. = 0 P20 activity does not generate the WD timeout event. Note: The P20 signal will remain high for a minimum of 1us and can remain high indefinitely. Therefore, when P20 forced timeouts are enabled, a self-clearing edge-detect circuit is used to generate a signal which is ORed with the signal generated by the Force Timeout Bit. Bit[7:4] Reserved. Set to 0
FAN Default = 0x00 on VTR POR	56 (R/W)	FAN Register Bit[0] Fan Control 1=FAN pin is high 0=bits[6:1] control the duty cycle of the FAN pin. Bit[6:1] Duty Cycle Control Control the duty cycle of the FAN pin 000000 = pin is low 100000 = 50% duty cycle 111111 = pin is high for 63, low for 1 Bit[7] Fan Clock Select This bit is used with the Fan Clock Source Select and the Fan Clock Multiplier bits in the Fan Control register (0x58) to determine the fan speed F_{OUT}. See Different Modes for Fan table (Table 49) in “Fan Speed Control and Monitoring” section. The fan speed may be doubled through bit 2 of Fan Control Register at 0x58.

NAME	REG OFFSET (hex)	DESCRIPTION
Fan Control Default = 0x10 on VTR POR	58 (R/W)	Fan Control Register Bit[0] Fan Clock Source Select This bit and the Fan Clock Multiplier bit is used with The Fan Clock Select bit in the Fan register (0x56) to determine the fan speed F_{OUT}. See Different Modes for Fan table in “Fan Speed Control and Monitoring” section. Bit[1] Reserved Bit[2] Fan Clock Multiplier 0=No multiplier used 1=Double the fan speed selected by bit 0 of this register and bit 7 of the Fan register Bit[3] Reserved Bit[5:4] FAN Count Divisor. Clock scalar for adjusting the tachometer count. Default = 2. 00: divisor = 1 01: divisor = 2 10: divisor = 4 11: divisor = 8 Bit[7:6] Reserved
Fan Tachometer Register Default = 0x00 on VTR POR	59 (R)	Fan Tachometer Register Bit[7:0] The 8-bit FAN tachometer count. The number of counts of the internal clock per pulse of the fan. The count value is computed from Equation 1 in the Fan section. This value is the final (maximum) count of the previous pulse (latched). The value in this register may not be valid for up to 2 pulses following a write to the preload register.
Fan Preload Register Default = 0x00 on VTR POR	5B (R/W)	Fan Preload Register Bit[7:0] The FAN tachometer preload. This is the initial value used in the computation of the FAN count. Writing this register resets the tachometer count.
LED1 Default = 0x00 on VTR POR	5D (R/W)	Bit[1:0] LED1 Control 00=off 01=Blink at 1Hz rate with a 50% duty cycle (0.5 sec on, 0.5 sec off) 10=Blink at ½ HZ rate with a 25% duty cycle (0.5 sec on, 1.5 sec off) 11=on Bits[7:2] Reserved

NAME	REG OFFSET (hex)	DESCRIPTION
LED2 Default = 0x01 on VTR POR	5E (R/W)	Bit[1:0] LED2 Control 00=off 01=Blink at 1Hz rate with a 50% duty cycle (0.5 sec on, 0.5 sec off) 10=Blink at ½ Hz rate with a 25% duty cycle (0.5 sec on, 1.5 sec off) 11=on Bits[7:2] Reserved
Keyboard Scan Code Default = 0x00 on VTR POR	5F (R/W)	Keyboard Scan Code Bit[0] LSB of Scan Code . . . . Bit[7] MSB of Scan Code
PM1_CNTRL1 Default = 0x00 on VTR POR	60 R/W – Bit[0] Read Only – Bits[7:1]	Bit[0] Read/Write Bits[7:1] Read-Only, reads always return 0
PM1_CNTRL2 Default = 0x00 on VTR POR	61 R/W – Bits[4:2] Read Only – Bits[7,6,1,0] Write Only – Bit[5]	Bits[1:0] Read-Only, reads always return 0 Bits[4:2] Read/Write Bit[5] Write-Only. Reads always return 0; writing a '1' to bit 5 is an SMI event Bits[7:6] Read-Only, reads always return 0
SMI_STS7 Default = 0x00 on VTR POR	64 (R/WC)	SMI Status Register 7 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] GP34 Bit[1] GP35 Bit[2] GP36 Bit[3] GP37 Bit[4] P16 Bit[5] SLP_EN_SMI This bit is the SMI status bit for writing '1' to bit 5 of the PM1_CNTRL2 register. This bit is set upon writing '1' to bit 5 of the PM1_CNTRL2 register. Bit[6] Reserved Bit[7] GP62

NAME	REG OFFSET (hex)	DESCRIPTION
SMI_EN7 Default = 0x00 on VTR POR	66 (R/W)	SMI Enable Register 7 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] GP34 Bit[1] GP35 Bit[2] GP36 Bit[3] GP37 Bit[4] P16 Bit[5] SLP_EN_SMI Bit[6] Reserved Bit[7] GP62
PME_STS7 Default = 0x00 on VTR POR	68 (R/WC)	This register indicates the state of the individual PME sources, independent of the individual source enables or the PME_En bit. If the PME source has asserted an event, the associated PME Status bit will be a “1”. Bit[0] GP34 Bit[1] GP35 Bit[2] GP36 Bit[3] GP37 Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] GP62 The PME Status register is not affected by VCC POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[4:0] will clear it. Writing a “0” to any bit in PME Status Register has no effect.
PME_EN7 Default = 0x00 on VTR POR	6C (R/W)	PME Enable Register 7 When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] GP34 Bit[1] GP35 Bit[2] GP36 Bit[3] GP37 Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] GP62

User Note: When selecting an alternate function for a GPIO pin, all bits in the GPIO register must be properly programmed, including in/out, polarity and output type. The polarity bit does not affect the DDRC function or the either edge triggered interrupt functions.

User Note 1: If this pin is used for Ring Indicator wakeup, either the nRI2 event can be enabled via bit 1 in the PME_EN1 register or the GP50 PME event can be enabled via bit 0 in the PME_EN5 register.

User Note 2: In order to use the P12, P16 and P17 functions, the corresponding GPIO must be programmed for output, non-invert, and push-pull output type.
The P12 function should not be selected on GP21 and GP22 simultaneously. If P12 is selected on GP21 and GP22, simultaneously, then P12 will function on GP22, not on GP21.
The P17 function should not be selected on GP20 and GP62 simultaneously. If P17 is selected on GP20 and GP62, simultaneously, then P17 will function on GP62, not on GP20.

Note 1: If the EETI function is selected for this GPIO then both a high-to-low and a low-to-high edge will set the PME, SMI and MSC status bits.

Note 2: These pins default to an output and LOW on VCC POR and Hard Reset.

Note 3: If the FDC function is selected on this pin (nMTR1, nDS1, DRVDEN0, DRVDEN1) then bit 6 of the FDD Mode Register (Configuration Register 0xF0 in Logical Device 0) will override bit 7 in the GPIO Control Register. Bit 7 of the FDD Mode Register will also affect the pin if the FDC function is selected.

Note 4: The nIO_SMI pin is inactive when the internal group SMI signal is inactive and when the SMI enable bit (EN_SMI, bit 7 of the SMI_EN2 register) is '0'. When the output buffer type is OD, nIO_SMI pin is floating when inactive; when the output buffer type is push-pull, the nIO_SMI pin is high when inactive.

Note 5: If GP52 and GP53 are programmed for RXD2 and TXD2 functions and serial port 2 is programmed for IR operation, then these pins will have IR functionality and when serial port 2 is disabled, the TXD2 pin will TRISTATE. If these pins are programmed for IRRX and IRTX then these pins will have IR functionality and when serial port 2 is disabled, the IRTX pin will go to its inactive state.

Note 6: The GP61 pin defaults to the LED function active (blinking at 1Hz rate, 50y duty cycle) on initial power up (as long as the 32kHz clock input is active).

CONFIGURATION

The Configuration of the LPC47S42x is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components. The LPC47S42x is designed for motherboard applications in which the resources required by their components are known. With its flexible resource allocation architecture, the LPC47S42x allows the BIOS to assign resources at POST.

SYSTEM ELEMENTS

Primary Configuration Address Decoder

After a hard reset (nPCI_RESET pin asserted) or VCC Power On Reset the LPC47S42x is in the Run Mode with all logical devices disabled. The logical devices may be configured through two standard Configuration I/O Ports (INDEX and DATA) by placing the LPC47S42x into Configuration Mode.

The BIOS uses these configuration ports to initialize the logical devices at POST. The INDEX and DATA ports are only valid when the LPC47S42x is in Configuration Mode.

The SYSOPT pin is latched on the falling edge of the nPCI_RESET or on VCC Power On Reset to determine the configuration register's base address. The SYSOPT pin is used to select the CONFIG PORT's I/O address at power-up. Once powered up the configuration port base address can be changed through configuration registers CR26 and CR27. **The SYSOPT pin is a hardware configuration pin which is shared with the GP24 signal on pin 45.**

Note. An external pull-down resistor is required for the base IO address to be 0x02E for configuration. An external pull-up resistor is required to move the base IO address for configuration to 0x04E.

The INDEX and DATA ports are effective only when the chip is in the Configuration State.

PORT NAME	SYSOPT= 0 10k PULL-DOWN RESISTOR	SYSOPT= 1 10K PULL-UP RESISTOR	TYPE
CONFIG PORT (Note 1)	0x02E	0x04E	Write
INDEX PORT (Note 1)	0x02E	0x04E	Read/Write
DATA PORT	INDEX PORT + 1		Read/Write

Note 1: The configuration port base address can be relocated through CR26 and CR27.

Entering the Configuration State

The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0x55>

Exiting the Configuration State

The device exits the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0xAA>

CONFIGURATION SEQUENCE

To program the configuration registers, the following sequence must be followed:

1. Enter Configuration Mode
2. Configure the Configuration Registers
3. Exit Configuration Mode.

Enter Configuration Mode

To place the chip into the Configuration State the Config Key is sent to the chip's CONFIG PORT. The config key consists of 0x55 written to the CONFIG PORT. Once the configuration key is received correctly the chip enters into the Configuration State (The auto Config ports are enabled).

Configuration Mode

The system sets the logical device information and activates desired logical devices through the INDEX and DATA ports. In configuration mode, the INDEX PORT is located at the CONFIG PORT address and the DATA PORT is at INDEX PORT address + 1.

The desired configuration registers are accessed in two steps:

a. Write the index of the Logical Device Number Configuration Register (i.e., 0x07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT.

b. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

Note: If accessing the Global Configuration Registers, step (a) is not required.

Exit Configuration Mode

To exit the Configuration State the system writes 0xAA to the CONFIG PORT. The chip returns to the RUN State.

Note: Only two states are defined (Run and Configuration). In the Run State the chip will always be ready to enter the Configuration State.

Programming Example

The following is an example of a configuration program in Intel 8086 assembly language.

```
;-----------------------------.
; ENTER CONFIGURATION MODE    |
;-----------------------------'
MOV    DX,02EH
MOV    AX,055H
OUT    DX,AL
;-----------------------------.
; CONFIGURE REGISTER CRE0,    |
; LOGICAL DEVICE 8            |
;-----------------------------'
MOV    DX,02EH
MOV    AL,07H
OUT    DX,AL ;Point to LD# Config Reg
MOV    DX,02FH
MOV    AL, 08H
OUT    DX,AL;Point to Logical Device 8
;
MOV    DX,02EH
MOV    AL,E0H
OUT    DX,AL  ; Point to CRE0
MOV    DX,02fH
MOV    AL,02H
OUT    DX,AL  ; Update CRE0
;-----------------------------.
; EXIT CONFIGURATION MODE     |
;-----------------------------'
MOV    DX,02EH
MOV    AX,0AAH
OUT    DX,AL
```

Notes: HARD RESET: nPCI_RESET pin asserted
SOFT RESET: Bit 0 of Configuration Control register set to one
All host accesses are blocked for 500µs after VCC POR (see Power-up Timing Diagram)

Table 59 – LPC47S42x Configuration Registers Summary

INDEX	TYPE	HARD RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
GLOBAL CONFIGURATION REGISTERS						
0x02	W	0x00	0x00	0x00	-	Config Control
0x03	R	-	-	-	-	Reserved – reads return 0
0x07	R/W	0x00	0x00	0x00	0x00	Logical Device Number
0x20	R	0x57	0x57	0x57	0x57	Device ID - hard wired
0x21	R	Current Revision				Device Rev - hard wired
0x22	R/W	0x00	0x00	0x00	0x00	Power Control
0x23	R/W	0x00	0x00	0x00	-	Power Mgmt
0x24	R/W	0x04	0x04	0x04	-	OSC
0x26	R/W	Sysopt=0 : 0x2E Sysopt=1 : 0x4E	Sysopt=0: 0x2E Sysopt=1: 0x4E	-	-	Configuration Port Address Byte 0 (Low Byte)
0x27	R/W	Sysopt=0 : 0x00 Sysopt=1 : 0x00	Sysopt=0: 0x00 Sysopt=1: 0x00	-	-	Configuration Port Address Byte 1 (High Byte)
0x28	R	-	-	-	-	Reserved
0x2A	R/W	-	0x00	0x00	-	TEST 6
0x2B	R/W	-	0x00	0x00	-	TEST 4
0x2C	R/W	-	0x00	0x00	-	TEST 5
0x2D	R/W	-	0x00	0x00	-	TEST 1
0x2E	R/W	-	0x00	0x00	-	TEST 2
0x2F	R/W	-	0x00	0x00	-	TEST 3
LOGICAL DEVICE 0 CONFIGURATION REGISTERS (FDD)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60, 0x61	R/W	0x03, 0xF0	0x03, 0xF0	0x03, 0xF0	0x03, 0xF0	Primary Base I/O Address
0x70	R/W	0x06	0x06	0x06	0x06	Primary Interrupt Select
0x74	R/W	0x02	0x02	0x02	0x02	DMA Channel Select
0xF0	R/W	0x0E	0x0E	0x0E	-	FDD Mode Register
0xF1	R/W	0x00	0x00	0x00	-	FDD Option Register
0xF2	R/W	0xFF	0xFF	0xFF	-	FDD Type Register

INDEX	TYPE	HARD RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
0xF4	R/W	0x00	0x00	0x00	-	FDD0
0xF5	R/W	0x00	0x00	0x00	-	FDD1
LOGICAL DEVICE 1 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 2 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 3 CONFIGURATION REGISTERS (Parallel Port)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0x74	R/W	0x04	0x04	0x04	0x04	DMA Channel Select
0xF0	R/W	0x3C	0x3C	0x3C	-	Parallel Port Mode Register
0xF1	R/W	0x00	0x00	0x00	-	Parallel Port Mode Register 2
LOGICAL DEVICE 4 CONFIGURATION REGISTERS (Serial Port 1)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 1 Mode Register
LOGICAL DEVICE 5 CONFIGURATION REGISTERS (Serial Port 2)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 2 Mode Register
0xF1	R/W	0x02	0x02	0x02	-	IR Options Register
0xF2	R/W	0x03	0x03	0x03	-	IR Half Duplex Timeout
LOGICAL DEVICE 6 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (Keyboard)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select (Keyboard)
0x72	R/W	0x00	0x00	0x00	0x00	Second Interrupt Select (Mouse)

INDEX	TYPE	HARD RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
0xF0	R/W	0x00	0x00	0x00	-	KRESET and GateA20 Select
LOGICAL DEVICE 8 CONFIGURATION REGISTERS (X-Bus)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W[Note1]	0x00	0x00	0x00	0x00	Base I/O Address 0 - High Byte
0x61	R/W [Note1]	0x00	0x00	0x00	0x00[Note 2]	Base I/O Address 0 - Low Byte
0x62	R/W [Note1]	0x00	0x00	0x00	0x00	Base I/O Address 1 - High Byte
0x63	R/W [Note1]	0x00	0x00	0x00	0x00[Note 2]	Base I/O Address 1 - Low Byte
0x64	R/W [Note1]	0x00	0x00	0x00	0x00	Base I/O Address 2 - High Byte
0x65	R/W [Note1]	0x00	0x00	0x00	0x00[Note 2]	Base I/O Address 2 - Low Byte
0x66	R/W [Note1]	0x00	0x00	0x00	0x00	Base I/O Address 3 - High Byte
0x67	R/W [Note1]	0x00	0x00	0x00	0x00[Note 2]	Base I/O Address 3 - Low Byte
0xF0	R/W	[Note 3]	[Note 3]	0x00	-	X-Bus Select
LOGICAL DEVICE 9 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE A CONFIGURATION REGISTERS (Runtime Registers)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	0x00, 0x00	0x00, 0x00	Primary Base I/O Address Runtime Register Block
0XF0	R/W	-	-	0x00	-	CLOCKI32
0xF4	R/W	-	-	0x00	-	IRQIN Routing Register 1
0xF5	R/W	-	-	0x00	-	IRQIN Routing Register 2
LOGICAL DEVICE B CONFIGURATION REGISTERS (SMBus)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	0x00, 0x00	0x00, 0x00	SMBus Primary Base I/O Address Runtime Register Block
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select

Note: Reserved registers are read-only, reads return 0.

Note 1: These registers are read-only if the write protect bit is set in the associated base I/O address low byte register.
Note 2: Bit 1 is reset on VCC POR, VTR POR and HARD RESET only.
Note 3: Bit 7 is reset on VCC POR, VTR POR and HARD RESET.

Chip Level (Global) Control/Configuration Registers[0x00-0x2F]

The chip-level (global) registers lie in the address range [0x00-0x2F]. The design MUST use all 8 bits of the ADDRESS Port for register selection. All unimplemented registers and bits ignore writes and return zero when read.

The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessible only in the Configuration Mode.

Table 60 - Chip Level Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
Chip (Global) Control Registers			
	0x00 - 0x01	Reserved - Writes are ignored, reads return 0.	
Config Control Default = 0x00 on VCC POR , VTR POR and HARD RESET	0x02 W	The hardware automatically clears this bit after the write, there is no need for software to clear the bits. Bit 0 = 1: Soft Reset. Refer to the "Configuration Registers" table for the soft reset value for each register.	C
N/A	0x03 - 0x06	Reserved - Writes are ignored, reads return 0.	
Logical Device # Default = 0x00 on VCC POR, VTR POR, HARD RESET and SOFT RESET	0x07 R/W	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. Note: The Activate command operates only on the selected logical device.	C
Card Level Reserved	0x08 - 0x1F	Reserved - Writes are ignored, reads return 0.	
Chip Level, SMSC Defined			
Device ID Default = 0x57 VCC POR, VTR POR, HARD RESET and SOFT RESET	0x20 R	A read only register which provides device identification. Bits[7:0] = 0x57 when read.	C

Table 60 - Chip Level Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
Device Rev Default = Current Rev VCC POR, VTR POR, HARD RESET and SOFT RESET	0x21 R	A read only register which provides device revision information..	C
PowerControl Default = 0x00. on VCC POR, VTR POR, HARD RESET and SOFT RESET	0x22 R/W	Bit[0] FDC Power Bit[1] Reserved Bit[2] Reserved Bit[3] Parallel Port Power Bit[4] Serial Port 1 Power Bit[5] Serial Port 2 Power Bit[6] Reserved Bit[7] Reserved	C
Power Mgmt Default = 0x00. on VCC POR, VTR POR and HARD RESET	0x23 R/W	Bit[0] FDC Bit[1] Reserved Bit[2] Reserved Bit[3] Parallel Port Bit[4] Serial Port 1 Bit[5] Serial Port 2 Bit[7:6] Reserved (read as 0) For each bit above (except Reserved) = 0 Intelligent Pwr Mgmt off = 1 Intelligent Pwr Mgmt on	C
OSC Default = 0x04, on VCC POR , VTR POR and HARD RESET	0x24 R/W	Bit[0] Reserved Bit [1] PLL Control = 0 PLL is on (backward Compatible) = 1 PLL is off Bits[3:2] OSC = 01 Osc is on, BRG clock is on. = 10 Same as above (01) case. = 00 Osc is on, BRG Clock Enabled. = 11 Osc is off, BRG clock is disabled. Bit [5:4] Reserved, set to zero Bit [6] 16-Bit Address Qualification = 0 12-Bit Address Qualification = 1 16-Bit Address Qualification Note: For normal operation, Bit 6 should be set. Bit[7] Reserved	C

Table 60 - Chip Level Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
Chip Level Vendor Defined	0x25	Reserved - Writes are ignored, reads return 0.	
Configuration Address Byte 0 Default =0x2E (Sysopt=0) =0x4E (Sysopt=1) on VCC POR and HARD RESET	0x26	Bit[7:1] Configuration Address Bits [7:1] Bit[0] = 0 See Note 1	C
Configuration Address Byte 1 Default = 0x00 on VCC POR and HARD RESET	0x27	Bit[7:0] Configuration Address Bits [15:8] See Note 1	C
N/A	0x28	Bits[7:0] Reserved - Writes are ignored, reads return 0.	
Chip Level Vendor Defined	0x29	Reserved - Writes are ignored, reads return 0.	
TEST 6 Default = 0x00, on VCC POR and VTR POR	0x2A R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	
TEST 4 Default = 0x00, on VCC POR and VTR POR	0x2B R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	C
TEST 5 Default = 0x00, on VCC POR and VTR POR	0x2C R/W	Bit[7] Test Mode: Reserved for SMSC. Users should not write to this bit, may produce undesired results. Bit[6] 8042 Reset: 1 = put the 8042 into reset 0 = take the 8042 out of reset Bits[5:0] Test Mode: Reserved for SMSC. Users should not write to this bit, may produce undesired results.	C
TEST 1 Default = 0x00, on VCC POR and VTR POR	0x2D R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	C

Table 60 - Chip Level Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
TEST 2 Default = 0x00, on VCC POR and VTR POR	0x2E R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	C
TEST 3 Default = 0x00, on VCC POR and VTR POR	0x2F R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	C

Note 1: To allow the selection of the configuration address to a user defined location, these Configuration Address Bytes are used. There is no restriction on the address chosen, except that A0 is 0, that is, the address must be on an even byte boundary. As soon as both bytes are changed, the configuration space is moved to the specified location with no delay (Note: Write byte 0, then byte 1; writing CR27 changes the base address).

The configuration address is only reset to its default address upon a Hard Reset or VCC POR.

Note: The default configuration address is either 0x02E or 0x04E, as specified by the SYSOPT pin.

Logical Device Configuration/Control Registers [0x30-0xFF]

Used to access the registers that are assigned to each logical unit. This chip supports eight logical units and has eight sets of logical device registers. The eight logical devices are Floppy, Parallel, Serial 1, Serial 2, Keyboard Controller, SMBus Controller, X-Bus and Runtime Registers. A separate set (bank) of control and configuration registers exists for each logical device and is selected with the Logical Device # Register (0x07).

The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT.

The Logical Device registers are accessible only when the device is in the Configuration State. The logical register addresses are shown in the table below.

Table 61 – Logical Device Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION	STATE
Activate (Note 1) Default = 0x00 on VCC POR , VTR POR, HARD RESET and SOFT RESET	(0x30)	Bits[7:1] Reserved, set to zero. Bit[0] = 1 Activates the logical device currently selected through the Logical Device # register. = 0 Logical device currently selected is inactive	C
Logical Device Control	(0x31-0x37)	Reserved - Writes are ignored, reads return 0.	C
Logical Device Control	(0x38-0x3f)	Vendor Defined - Reserved - Writes are ignored, reads return 0.	C
Memory Base Address	(0x40-0x5F)	Reserved - Writes are ignored, reads return 0.	C
I/O Base Address (Note 2) (see Device Base I/O Address Table) Default = 0x00 on VCC POR, VTR POR, HARD RESET and SOFT RESET	(0x60-0x6F) 0x60,2,... = addr[15:8] 0x61,3,... = addr[7:0]	Registers 0x60 and 0x61 set the base address for the device. If more than one base address is required, the second base address is set by registers 0x62 and 0x63. Refer to Table 62 for the number of base address registers used by each device. Unused registers will ignore writes and return zero when read. See the X-Bus and SMBus Logical Device Configuration registers for a description of their respective Base I/O registers.	C

Table 62 – Logical Device Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION	STATE
Interrupt Select Defaults : 0x70 = 0x00 or 0x06 (Note 3) on VCC POR, VTR POR, HARD RESET and SOFT RESET 0x72 = 0x00, on VCC POR, VTR POR, HARD RESET and SOFT RESET	(0x70,0x72)	0x70 is implemented for each logical device. Refer to Interrupt Configuration Register description. Only the keyboard controller uses Interrupt Select register 0x72. Unused register (0x72) will ignore writes and return zero when read. Interrupts default to edge high (ISA compatible).	C
	(0x71,0x73)	Reserved - not implemented. These register locations ignore writes and return zero when read.	
DMA Channel Select Default = 0x02 or 0x04 (Note 4) on VCC POR, VTR POR, HARD RESET and SOFT RESET	(0x74,0x75)	Only 0x74 is implemented for FDC and Parallel port. 0x75 is not implemented and ignores writes and returns zero when read. Refer to DMA Channel Select Configuration register description.	C
32-Bit Memory Space Configuration	(0x76-0xA8)	Reserved - not implemented. These register locations ignore writes and return zero when read.	
Logical Device	(0xA9-0xDF)	Reserved - not implemented. These register locations ignore writes and return zero when read.	C
Logical Device Configuration	(0xE0-0xFE)	Reserved - Vendor Defined (see SMSC defined Logical Device Configuration Registers).	C
Reserved	0xFF	Reserved	C

Note 1: A logical device will be active and powered up according to the following equation:

DEVICE ON (ACTIVE) = (Activate Bit SET or Pwr/Control Bit SET).
The Logical device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other.

Note 2: If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

Note 3: The default value of the Primary Interrupt Select register for logical device 0 is 0x06.

Note 4: The DMA (0x74) default address for logical device 0 (FDD) is 0x02 and for logical device 3 is 0x04.

Table 63 - I/O Base Address Configuration Register Description

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (Note 1)	FIXED BASE OFFSETS
0x00	FDC	0x60,0x61	[0x0100:0x0FF8] on 8-byte boundaries	+0 : SRA +1 : SRB +2 : DOR +3 : TDR +4 : MSR/DSR +5 : FIFO +7 : DIR/CCR
0x01	Reserved	n/a	n/a	n/a
0x02	Reserved	n/a	n/a	n/a
0x03	Parallel Port	0x60,0x61	[0x0100:0x0FFC] on 4-byte boundaries (EPP Not supported) or [0x0100:0x0FF8] on 8-byte boundaries	+0 : Data/ecpAfifo +1 : Status +2 : Control +400h : cfifo/ecpDfifo/tfifo/cnfgA +401h : cnfgB +402h : ecr
			(all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+3 : EPP Address +4 : EPP Data 0 +5 : EPP Data 1 +6 : EPP Data 2 +7 : EPP Data 3
0x04	Serial Port 1	0x60,0x61	[0x0100:0x0FF8] on 8 byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LCR +6 : MSR +7 : SCR
0x05	Serial Port 2	0x60,0x61	[0x0100:0x0FF8] on 8-byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LCR +6 : MSR +7 : SCR
0x06	Reserved	n/a	n/a	n/a
0x07	KYBD	n/a	Not Relocatable Fixed Base Address: 60,64	+0 : Data Register +4 : Command/Status Reg.

Table 63 - I/O Base Address Configuration Register Description

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (Note 1)	FIXED BASE OFFSETS
0x08	X-Bus	0x60,0x61	Mode 1: [0x0000:0x0FFC] ON 4 BYTE BOUNDARIES Mode 2: [0x0000:0x0FF0] ON 16 BYTE BOUNDARIES	+0: X-bus CS0 Address
		0x62,0x63	Mode 1: [0x0000:0x0FFC] ON 4 BYTE BOUNDARIES Mode 2: [0x0000:0x0FF0] ON 16 BYTE BOUNDARIES	+0: X-bus CS1 Address
		0x64,0x65	Mode 1 Only [0x0000:0x0FFC] ON 4 BYTE BOUNDARIES	+0: X-bus CS2 Address
		0x66,0x67	Mode 1 Only [0x0000:0x0FFC] ON 4 BYTE BOUNDARIES	+0: X-bus CS3 Address
0x09	Reserved	n/a	n/a	n/a
0x0A	Runtime Register Block	0x60,0x61	[0x0000:0x0F80] on 128-byte boundaries	+00 : PME_STS . . . (See Table in “Runtime Registers” section for Full List)
0x0B	SMBus	0x60, 0x61	[0x0100:0x0FF8] on 8-byte boundaries	+0: Control/Data +1: Own Address +2: Data +3: Clock
Config. Port	Config. Port	0x26, 0x27 (Note 2)	0x0100:0x0FFE On 2-byte boundaries	See Configuration Registers in Table 64. Accessed through the index and DATA ports located at the Configuration Port address and the Configuration Port address +1 respectively.

Note 1: This chip uses address bits [A11:A0] to decode the base address of each of its logical devices. Bit 6 of the OSC Global Configuration Register (CR24) must be set to ‘1’ and Address Bits [A15:A12] must be ‘0’ for 16 bit address qualification.

Note 2: The Configuration Port is at either 0x02E or 0x04E (for SYSOPT=0 or SYSOPT=1) at power up and can be relocated via the global configuration registers at 0x26 and 0x27.

Table 64 - Interrupt Select Configuration Register Description

NAME	REG INDEX	DEFINITION	STATE
Primary Interrupt Select Default=0x00 or 0x06 (Note 1) on VCC POR, VTR POR, HARD RESET and SOFT RESET	0x70 (R/W)	Bits[3:0] selects which interrupt level is used for the primary Interrupt. 0x00= no interrupt selected 0x01= IRQ1 0x02= IRQ2/nSMI 0x03= IRQ3 0x04= IRQ4 0x05= IRQ5 0x06= IRQ6 0x07= IRQ7 0x08= IRQ8 0x09= IRQ9 0x0A= IRQ10 0x0B= IRQ11 0x0C= IRQ12 0x0D= IRQ13 0x0E= IRQ14 0x0F= IRQ15 Note: All interrupts are edge high (except ECP/EPP) Note: nSMI is active low	C

Note: An Interrupt is activated by setting the Interrupt Request Level Select 0 register to a non-zero value AND:
For the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
For the PP logical device by setting IRQE, bit D4 of the Control Port and in addition
For the PP logical device in ECP mode by clearing serviceIntr, bit D2 of the ecr.
For the Serial Port logical device by setting any combination of bits D0-D3 in the IER and by setting the OUT2 bit in the UART's Modem Control (MCR) Register.
For the KYBD logical device (refer to the KYBD controller section of this spec).
For the SMBus logical device by setting ENI bit D3 of the Control Register.

Note: IRQs are disabled if not used/selected by any Logical Device. Refer to Note A.

Note: nSMI must be disabled to use IRQ2.

Note: All IRQ's are available in Serial IRQ mode.

Note 1: The default value of the Primary Interrupt Select register for logical device 0 is 0x06.

Table 65 - DMA Channel Select Configuration Register Description

NAME	REG INDEX	DEFINITION	STATE
DMA Channel Select Default=0x02 or 0x04 (Note 1) on VCC POR, VTR POR, HARD RESET and SOFT RESET	0x74 (R/W)	Bits[2:0] select the DMA Channel. 0x00= Reserved 0x01= DMA1 0x02= DMA2 0x03= DMA3 0x04-0x07= No DMA active	C

Note: A DMA channel is activated by setting the DMA Channel Select register to [0x01-0x03] AND:
For the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
For the PP logical device in ECP mode by setting dmaEn, bit D3 of the ecr.

Note: DMA channels are disabled if not used/selected by any Logical Device. Refer to Note A.

Note 1: The default value of the DMA Channel Select register for logical device 0 (FDD) is 0x02 and for logical device 3 and 5 is 0x04.

Note A. Logical Device IRQ and DMA Operation

1. IRQ and DMA Enable and Disable: Any time the IRQ or DMA channel for a logical block is disabled by a register bit in that logical block, the IRQ and/or DMA channel must be disabled. This is in addition to the IRQ and DMA channel disabled by the Configuration Registers (active bit or address not valid).

a. FDC: For the following cases, the IRQ and DMA channel used by the FDC are disabled.
Digital Output Register (Base+2) bit D3 (DMAEN) set to "0".
The FDC is in power down (disabled).

b. Serial Ports:
Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic "0", the serial port interrupt is disabled.

c. Parallel Port:
I. SPP and EPP modes: Control Port (Base+2) bit D4 (IRQE) set to "0", IRQ is disabled.
ii. ECP Mode:
(1) (DMA) dmaEn from ecr register. See table.
(2) IRQ - See table.

MODE (FROM ECR REGISTER)		IRQ CONTROLLED BY	DMA CONTROLLED BY
000	PRINTER	IRQE	dmaEn
001	SPP	IRQE	dmaEn
010	FIFO	(on)	dmaEn
011	ECP	(on)	dmaEn
100	EPP	IRQE	dmaEn
101	RES	IRQE	dmaEn
110	TEST	(on)	dmaEn
111	CONFIG	IRQE	dmaEn

d. Keyboard Controller: Refer to the KBD section of this spec.

e. SMBus Controller:
Control Register Bit D3 (ENI) – When ENI is a logic “0” the SMBus interrupt is disabled.

SMSC Defined Logical Device Configuration Registers

The SMSC Specific Logical Device Configuration Registers reset to their default values only on hard resets generated by VCC or VTR POR (as shown) or the HARD RESET signal. These registers are not affected by soft resets.

Table 66 - Floppy Disk Controller, Logical Device 0 [Logical Device Number = 0x00]

NAME	REG INDEX	DEFINITION	STATE
FDD Mode Register Default = 0x0E on VCC POR , VTR POR and HARD RESET	0xF0 R/W	Bit[0] Floppy Mode = 0 Normal Floppy Mode (default) = 1 Enhanced Floppy Mode 2 (OS2) Bit[1] FDC DMA Mode = 0 Burst Mode is enabled = 1 Non-Burst Mode (default) Bit[3:2] Interface Mode = 11 AT Mode (default) = 10 (Reserved) = 01 PS/2 = 00 Model 30 Bit[4] Reserved Bit[5] Reserved, set to zero Bit[6] FDC Output Type Control = 0 FDC outputs are OD12 open drain (default) = 1 FDC outputs are O12 push-pull Bit[7] FDC Output Control = 0 FDC outputs active (default) = 1 FDC outputs tri-stated Note: Bits 6 & 7 do not affect the parallel port FDC pins.	C

Table 66 - Floppy Disk Controller, Logical Device 0 [Logical Device Number = 0x00]

NAME	REG INDEX	DEFINITION	STATE
FDD Option Register Default = 0x00 on VCC POR, VTR POR and HARD RESET	0xF1 R/W	Bit[0] Forced Write Protect = 0 Inactive (default) = 1 FDD nWRTPRT input is forced active when either of the drives has been selected. Bit[1] Reserved Bits[3:2] Density Select = 00 Normal (default) = 01 Normal (reserved for users) = 10 1 (forced to logic "1") = 11 0 (forced to logic "0") Bit[7:4] Reserved. nWRTPRT (to the FDC Core) = WP (FDC SRA Register, Bit 1) = (Floppy Write Protect) OR nWRTPRT(from the FDD Interface) OR (nDS0 AND Force Write Protect) OR (nDS1 AND Force Write Protect). Note: Floppy Write Protect bit is in the Device Disable register. Note: Boot floppy is always drive 0. Note: the Force Write Protect bits also apply to the Parallel Port FDC.	C
FDD Type Register Default = 0xFF on VCC POR, VTR POR and HARD RESET	0xF2 R/W	Bits[1:0] Floppy Drive A Type Bits[3:2] Floppy Drive B Type Bits[5:4] Reserved (could be used to store Floppy Drive C type) Bits[7:6] Reserved (could be used to store Floppy Drive D type) Note: The LPC47S42x supports two floppy drives	C
	0xF3 R	Reserved, Read as 0 (read only)	C
FDD0 Default = 0x00 on VCC POR, VTR POR and HARD RESET	0xF4 R/W	Bits[1:0] Drive Type Select: DT1, DT0 Bits[2] Read as 0 (read only) Bits[4:3] Data Rate Table Select: DRT1, DRT0 Bits[5] Read as 0 (read only) Bits[6] Precompensation Disable PTS =0 Use Precompensation =1 No Precompensation Bits[7] Read as 0 (read only)	C
FDD1	0xF5 R/W	Refer to definition and default for 0xF4	C

Table 67 - Parallel Port, Logical Device 3 [Logical Device Number = 0x03]

NAME	REG INDEX	DEFINITION	STATE
PP Mode Register Default = 0x3C on VCC POR , VTR POR and HARD RESET	0xF0 R/W	Bits[2:0] Parallel Port Mode = 100 Printer Mode (default) = 000 Standard and Bi-directional (SPP) Mode = 001 EPP-1.9 and SPP Mode = 101 EPP-1.7 and SPP Mode = 010 ECP Mode = 011 ECP and EPP-1.9 Mode = 111 ECP and EPP-1.7 Mode Bit[6:3] ECP FIFO Threshold 0111b (default) Bit[7] PP Interrupt Type **Not valid when the parallel port is in the Printer Mode (100) or the Standard & Bi-directional Mode (000).** = 1 Pulsed Low, released to high-Z. = 0 IRQ follows nACK when parallel port in EPP Mode or [Printer, SPP, EPP] under ECP. IRQ level type when the parallel port is in ECP, TEST, or Centronics FIFO Mode.	C
PP Mode Register 2 Default = 0x00 on VCC POR, VTR POR and HARD RESET	0xF1 R/W	Bits[1:0] PPFDC - muxed PP/FDC control = 00 Normal Parallel Port Mode = 01 PPFD1: Drive 0 is on the FDC pins Drive 1 is on the Parallel port pins = 10 PPFD2: Drive 0 is on the Parallel port pins Drive 1 is on the Parallel port pins Bits[7:2] Reserved. Set to zero.	

Table 68 - Serial Port 1, Logical Device 4 [Logical Device Number = 0x04]

NAME	REG INDEX	DEFINITION	STATE
Serial Port 1 Mode Register Default = 0x00 on VCC POR , VTR POR and HARD RESET	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled(default) = 1 High Speed Enabled Bit[6:2] Reserved, set to zero Bit[7]: Share IRQ =0 UARTS use different IRQs =1 UARTS share a common IRQ See Note 1 below.	C

Note 1: To properly share and IRQ,

1. Configure UART1 (or UART2) to use the desired IRQ pin.
2. Configure UART2 (or UART1) to use No IRQ selected.
3. Set the share IRQ bit.

Note: If both UARTs are configured to use different IRQs and the share IRQ bit is set, then both of the UART IRQs will assert when either UART generates an interrupt.

UART Interrupt Operation Table

Table 69 - Serial Port 2, Logical Device 5 [Logical Device Number = 0x05]

NAME	REG INDEX	DEFINITION	STATE
Serial Port 2 Mode Register Default = 0x00 on VCC POR, VTR POR and HARD RESET	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed disabled(default) = 1 High Speed enabled Bit[7:2] Reserved, set to zero	C

Table 69 - Serial Port 2, Logical Device 5 [Logical Device Number = 0x05]

NAME	REG INDEX	DEFINITION	STATE
IR Option Register Default = 0x02 On VCC POR, VTR POR and HARD RESET	0xF1 R/W	Bit[0] Receive Polarity = 0 Active High (Default) = 1 Active Low Bit[1] Transmit Polarity = 0 Active High = 1 Active Low (Default) Bit[2] Duplex Select = 0 Full Duplex (Default) = 1 Half Duplex Bits[5:3] IR Mode = 000 Standard COM Functionality (Default) = 001 IrDA = 010 ASK-IR = 011 Reserved = 1xx Reserved Bit[6] Reserved, write 0. Bit[7] Reserved, write 0.	C
IR Half Duplex Timeout Default = 0x03 on VCC POR, VTR POR and HARD RSET	0xF2	Bits [7:0] These bits set the half duplex time-out for the IR port. This value is 0 to 10msec in 100usec increments. 0= blank during transmit/receive 1= blank during transmit/receive + 100usec . . .	

Table 70 - KYBD, Logical Device 7 [Logical Device Number = 0x07]

NAME	REG INDEX	DEFINITION	STATE
KRST_GA20 Default = 0x00 on VCC POR, VTR POR and HARD RESET	0xF0 R/W	KRESET and GateA20 Select Bit[7] Polarity Select for P12 = 0 P12 active low (default) = 1 P12 active high Bit[6] M_ISO. Enables/disables isolation of mouse signals into 8042. Does not affect MDAT signal to mouse wakeup (PME) logic. 1=block mouse clock and data signals into 8042 0= do not block mouse clock and data signals into 8042 Bit[5] K_ISO. Enables/disables isolation of keyboard signals into 8042. Does not affect KDAT signal to keyboard wakeup (PME) logic. 1=block keyboard clock and data signals into 8042 0= do not block keyboard clock and data signals into 8042 Bit[4] MLATCH = 0 MINT is the 8042 MINT ANDed with Latched MINT (default) = 1 MINT is the latched 8042 MINT Bit[3] KLATCH = 0 KINT is the 8042 KINT ANDed with Latched KINT (default) = 1 KINT is the latched 8042 KINT Bit[2] Port 92 Select = 0 Port 92 Disabled = 1 Port 92 Enabled Bit[1] Reserved Bit[0] Reserved	
	0xF1 - 0xFF	Reserved - read as ‘0’	

Table 71 – X-Bus, Logical Device 8 [Logical Device Number = 0x08]

NAME	REG INDEX	DEFINITION	STATE
Base I/O Address 0 – High Byte Note 1 Default = 0x00 on VTR POR, VCC POR, Hard Reset and Soft Reset	0x60 R/W, Read-Only when the Base I/O Address 0 – Low Byte Register bit[1]=1.	Register 0x60 sets the high byte of the base I/O address for chip select 0. Bits [7:0] =address[15:8] Note: Bits[15:12] must be '0' since the chip performs 16-bit address qualification on the base I/O addresses.	
Base I/O Address 0 – Low Byte Note 1 Default = 0x00 on VTR POR, VCC POR, Hard Reset and Soft Reset Bit 1 is reset on VCC POR, VTR POR and Hard Reset	0x61 R/W, Read-Only when the Base I/O Address 0 – Low Byte Register bit[1]=1	Register 0x61 sets the low byte of the base I/O address for chip select 0. Bit 1 is the write protect bit for registers 60 and 61. Bit 0 is the disable bit for nXCS0. Bits[7:2] are X-Bus mode dependent as follows: Mode 1: Bits [7:2] =Address[7:2] Mode 2: Bits [7:4] =Address[7:4] Bit[3:2] = Reserved Bit[1] = Register 60, 61 Write Protect. Cleared by VCC POR and Hard Reset only. Cannot be cleared by software writing to this bit. 0=Register 60 and 61 are read/write 1=Register 60 and 61 are read-only Bit[0] = Disable bit for nXCS0. 0=enable chip select 1=disable chip select	
Base I/O Address 1 – High Byte Note 1 Default = 0x00 on VTR POR, VCC POR, Hard Reset and Soft Reset	0x62 R/W, Read-Only when the Base I/O Address 1 – Low Byte Register bit[1]=1	Register 0x62 sets the high byte of the base I/O address for chip select 1. Bits [7:0] =address[15:8] Note: Bits[15:12] must be '0' since the chip performs 16-bit address qualification on the base I/O addresses.	

Table 71 – X-Bus, Logical Device 8 [Logical Device Number = 0x08]

NAME	REG INDEX	DEFINITION	STATE
Base I/O Address 1 – Low Byte Note 1 Default = 0x00 on VTR POR, VCC POR, Hard Reset and Soft Reset Bit 1 is reset on VCC POR, VTR POR and Hard Reset	0x63 R/W, Read-Only when the Base I/O Address 1 – Low Byte Register bit[1]=1	Register 0x63 sets the low byte of the base I/O address for chip select 1. Bit 1 is the write protect bit for registers 62 and 63. Bit 0 is the disable bit for nXCS1. Bits[7:1] are X-Bus mode dependent as follows: Mode 1: Bits [7:2] =address[7:2] Mode 2: Bits [7:4] =address[7:4] Bit[3:2] = Reserved Bit[1] = Register 62, 63 Write Protect. Cleared by VCC POR and Hard Reset only. Cannot be cleared by software writing to this bit. 0=Register 62 and 63 are read/write 1=Register 62 and 63 are read-only Bit[0] = Disable bit for nXCS1. 0=enable chip select 1=disable chip select	
Base I/O Address 2 – High Byte Note 1 Default = 0x00 on VTR POR, VCC POR, Hard Reset and Soft Reset	0x64 R/W, Read-Only when the Base I/O Address 2 – Low Byte Register bit[1]=1	Register 0x64 sets the high byte of the base I/O address for chip select 2. This register is only used in X-Bus Mode 1. Bits [7:0] =address[15:8] Note: Bits[15:12] must be '0' since the chip performs 16-bit address qualification on the base I/O addresses.	
Base I/O Address 2 – Low Byte Note 1 Default = 0x00 on VTR POR, VCC POR, Hard Reset and Soft Reset Bit 1 is reset on VCC POR, VTR POR and Hard Reset	0x65 R/W, Read-Only when the Base I/O Address 2 – Low Byte Register bit[1]=1	Register 0x65 sets the low byte of the base I/O address for chip select 2. Bit 1 is the write protect bit for registers 64 and 65. Bit 0 is the disable bit for nXCS2. This register is only used in X-Bus Mode 1. Bits [7:2] =address[7:2] Bit[1] = Register 64, 65 Write Protect. Cleared by VCC POR and Hard Reset only. Cannot be cleared by software writing to this bit. 0=Register 64 and 65 are read/write 1=Register 64 and 65 are read-only Bit[0] = Disable bit for nXCS2. 0=enable chip select 1=disable chip select	

Table 71 – X-Bus, Logical Device 8 [Logical Device Number = 0x08]

NAME	REG INDEX	DEFINITION	STATE
Base I/O Address 3 – High Byte Note 1 Default = 0x00 on VTR POR, VCC POR, Hard Reset and Soft Reset	0x66 R/W, Read-Only when the Base I/O Address 3 – Low Byte Register bit[1]=1	Register 0x66 sets the high byte of the base I/O address for chip select 3. This register is only used in X-Bus Mode 1. Bits [7:0] =address[15:8] Note: Bits[15:12] must be '0' since the chip performs 16-bit address qualification on the base I/O addresses.	
Base I/O Address 3 – Low Byte Note 1 Default = 0x00 on VTR POR, VCC POR, Hard Reset and Soft Reset Bit 1 is reset on VCC POR, VTR POR and Hard Reset	0x67 R/W, Read-Only when the Base I/O Address 3 – Low Byte Register bit[1]=1	Register 0x67 sets the low byte of the base I/O address for chip select 3. Bit 1 is the write protect bit for registers 66 and 67. Bit 0 is the disable bit for nXCS3. This register is only used in X-Bus Mode 1. Bits [7:2] =address[7:2] Bit[1] = Register 66, 67 Write Protect. Cleared by VCC POR and Hard Reset only. Cannot be cleared by software writing to this bit. 0=Register 66 and 67 are read/write 1=Register 66 and 67 are read-only Bit[0] = Disable bit for nXCS3. 0=enable chip select 1=disable chip select	
X-Bus Selection Default = 0x00 on VTR POR Bit 7 is reset on VCC POR, VTR POR and Hard Reset	0xF0 (R/W)	Bit[0] X-Bus Mode. 0=Mode 1 1=Mode 2 Note that the GPIOs must be configured properly to use the selected mode. The GPIOs are not automatically configured for the mode selected. Bit[1] Reserved Bits[3:2] X-Bus Read/Write Pulse Width Selection. These bits select the pulse width of the X-bus read and write strobes. They extend the LPC cycle accordingly by adding wait states (sync fields) into the cycle. 11=540nsec min 10=420nsec min 01=300nsec min 00=180nsec min (default) Bits[6:4] Reserved Bit[7] Register Write Protect. Cleared by VCC POR, VTR POR and Hard Reset only. Cannot be cleared by software writing this bit. 0=X-Bus selection register is Read/Write. 1=X-Bus Selection register is Read-Only	

Note 1: If the I/O Base Address of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

Table 72 – Runtime Registers, Logical Device A

NAME	REG INDEX	DEFINITION	STATE
CLOCKI32 Default = 0x00 on VTR POR	0xF0 (R/W)	Bit[0] (CLK32_PRSN) 0=32kHz clock is connected to the CLKI32 pin (default) 1=32kHz clock is not connected to the CLKI32 pin (pin is grounded) Bit[1] SPEKEY_EN. This bit is used to turn the logic for the “wake on specific key” feature on and off. It will disable the 32kHz clock input to the logic when turned off. The logic will draw no power when disabled. 0= “Wake on specific key” logic is on (default) 1= “Wake on specific key” logic is off Bits[7:2] are reserved	C
IRQIN Routing Register 1 Default = 0x00 on VTR POR	0xF4 (R/W)	Bits[7:4] IRQINB routing. Selects which serial interrupt is used for IRQINB. See bit mapping below. Bits[3:0] IRQINA routing. Selects which serial interrupt is used for IRQINA. See bit mapping below. Bits[7:4] and bits[3:0] mapping: 0x00= no interrupt selected 0x01= IRQ1 0x02= IRQ2/nIO_SMI 0x03= IRQ3 0x04= IRQ4 0x05= IRQ5 0x06= IRQ6 0x07= IRQ7 0x08= IRQ8 0x09= IRQ9 0x0A= IRQ10 0x0B= IRQ11 0x0C= IRQ12 0x0D= IRQ13 0x0E= IRQ14 0x0F= IRQ15 Note: nIO_SMI must be disabled to use IRQ2 for an interrupt other than SMI.	

Table 72 – Runtime Registers, Logical Device A

NAME	REG INDEX	DEFINITION	STATE
IRQIN Routing Register 2 Default = 0x00 on VTR POR	0xF5	Bits[7:4] IRQIND routing. Selects which serial interrupt is used for IRQIND. See bit mapping below. Bits[3:0] IRQINC routing. Selects which serial interrupt is used for IRQINC. See bit mapping below. Bits[7:4] and bits[3:0] mapping: 0x00= no interrupt selected 0x01= IRQ1 0x02= IRQ2/nIO_SMI 0x03= IRQ3 0x04= IRQ4 0x05= IRQ5 0x06= IRQ6 0x07= IRQ7 0x08= IRQ8 0x09= IRQ9 0x0A= IRQ10 0x0B= IRQ11 0x0C= IRQ12 0x0D= IRQ13 0x0E= IRQ14 0x0F= IRQ15 Note: nIO_SMI must be disabled to use IRQ2 for an interrupt other than SMI.	

Table 73 - SMBus [Logical Device Number = 0x0B]

NAME	REG INDEX	DEFINITION	STATE
SMBus Primary Base Address High Byte Default = 0x00 on VCC POR, VTR POR, HARD RESET and SOFT RESET	0x60 R/W	Bit[0] A8 Bit[1] A9 Bit[2] A10 Bit[3] A11 Bit[4] “0” Bit[5] “0” Bit[6] “0” Bit[7] “0”	C
SMBus Primary Base Address Low Byte (Note 1) Default = 0x00 on VTR POR, VCC POR, HARD RESET and SOFT RESET	0x61 R/W	Bit[0] “0” Bit[1] “0” Bit[2] “0” Bit[3] A3 Bit[4] A4 Bit[5] A5 Bit[6] A6 Bit[7] A7	C

NOTE 1: The valid address range is 0x0100 – 0x0FF8.

OPERATIONAL DESCRIPTION

Maximum Guaranteed Ratings

Operating Temperature Range ..... 0^{o}C to $+70^{o}$C
Storage Temperature Range ..... -55^{o} to $+150^{o}$C
Lead Temperature Range ..... Refer to JEDEC Spec. J-STD-020
Positive Voltage on any pin, with respect to Ground ..... V_{CC}+0.3V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum V_{CC} ..... +7V

Note: Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC Electrical Characteristics

($T_A = 0^{0}C - 70^{0}C$, V_{CC} = +3.3 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		100		mV	
Input Leakage, I and IS Buffers						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	$V_{IN} = V_{CC}$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IO6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -3mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
OD6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
O6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -3mA
IO8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
IOP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
IOD16 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
Backdrive Protect/ChiProtect (All pins excluding LAD[3:0], nLDRQ, nLPCPD, nLFRAME)	I_{IL}			± 10	µA	V_{CC} = 0V V_{IN} = 5.5V Max
5V Tolerant Pins (All pins excluding LAD[3:0], nLDRQ, nLPCPD, nLFRAME) Inputs and Outputs in High Impedance State	I_{IL}			± 10	µA	V_{CC} = 3.3V V_{IN} = 5.5V Max
LPC Bus Pins (LAD[3:0], nLDRQ, nLPCPD, nLFRAME)	I_{IL}			± 10	µA	V_{CC} = 0V and V_{CC} = 3.3V V_{IN} = 3.6V Max
V_{CC} Supply Current Active	I_{CCI}			20[3]	mA	All outputs open, all inputs at a fixed state (i.e., 0V or 3.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Trickle Supply Voltage	V_{TR}	V_{CC} min -.5V[5]		V_{CC} max	V	V_{CC} must not be greater than .5V above V_{TR}
V_{TR} Supply Current Active	I_{TRI}			1[3,4]	mA	All outputs open, all inputs at a fixed state (i.e., 0V or 3.3V)

Note 1: All output leakage's are measured with all pins in high impedance.
Note 2: Output leakage is measured with the low driving output off, either for a high level output or a high impedance state.
Note 3: Contact SMSC for the latest values.
Note 4: Max I_{TRI} with V_{CC} = 3.3V (nominal) is 1mA.
Max I_{TRI} with V_{CC} = 0 is 100µA.
Note 5: The minimum value given for V_{TR} applies when V_{CC} is active. When V_{CC} is 0V, the minimum V_{TR} is 0V.

CAPACITANCE $T_A = 25^0C$; fc = 1MHz; V_{CC} = 3.3V ±10%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

TIMING DIAGRAMS

For the Timing Diagrams shown, the following capacitive loads are used on outputs.

NAME	CAPACITANCE TOTAL (pF)
SER_IRQ	50
nLAD[3:0]	50
nLDRQ	50
nDIR	240
nSTEP	240
nDS0-1	240
nWDATA	240
PD[0:7]	240
nSTROBE	240
nALF	240
nSLCTIN	240
KDAT	240
KCLK	240
MDAT	240
MCLK	240
FAN	50
LEDx	50
TXD1	50
TXD2	50
nXCS[0:3]	50
XA[0:3]	50
XD[0:7]	50
nXRD	50
nXWR	50
SDAT	50
SCLK	50

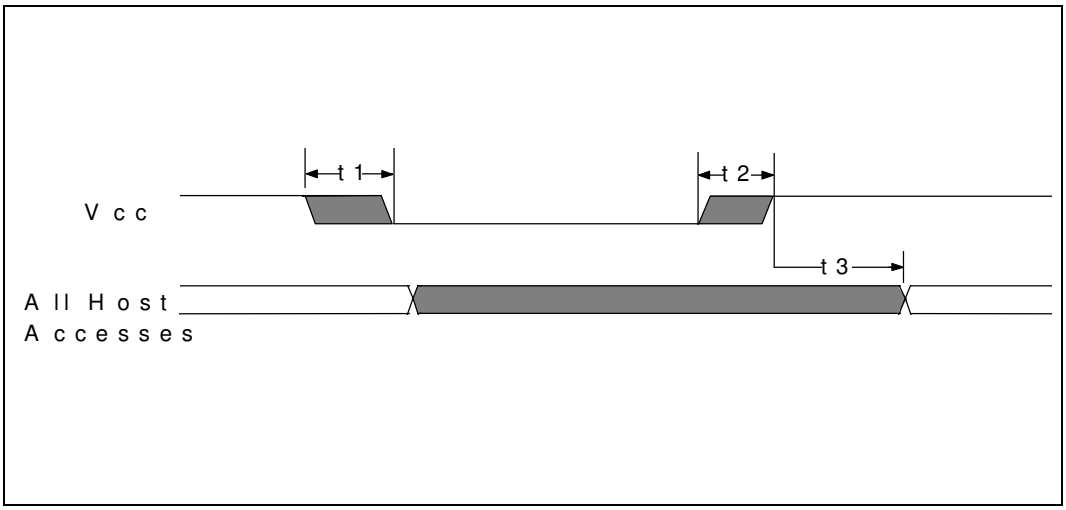


FIGURE 8 - POWER-UP TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Vcc Slew from 2.7V to 0V	300			µs
t2	Vcc Slew from 0V to 2.7V	100			µs
t3	All Host Accesses After Powerup (Note 1)	125		500	µs

Note 1: Internal write-protection period after Vcc passes 2.7 volts on power-up

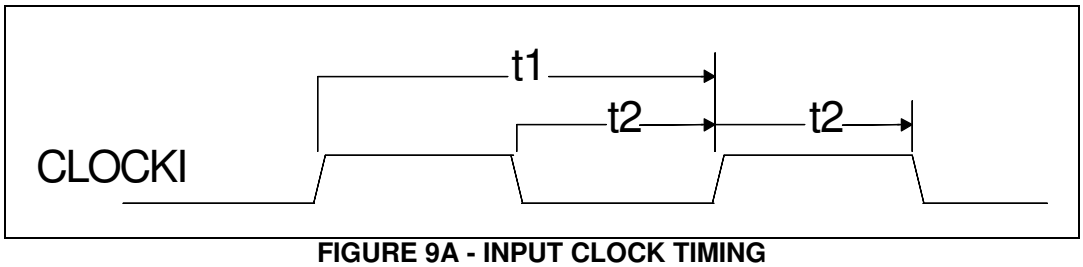


FIGURE 9A - INPUT CLOCK TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318MHz		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
t1	Clock Cycle Time for 32kHz		31.25		µs
t2	Clock High Time/Low Time for 32kHz		16.53		µs
	Clock Rise Time/Fall Time (not shown)			5	ns

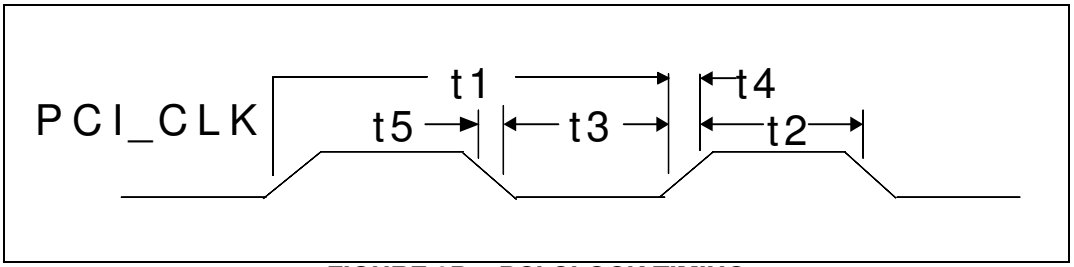


FIGURE 9B – PCI CLOCK TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Period	30		33.3	nsec
t2	High Time	12			nsec
t3	Low Time	12			nsec
t4	Rise Time			3	nsec
t5	Fall Time			3	nsec

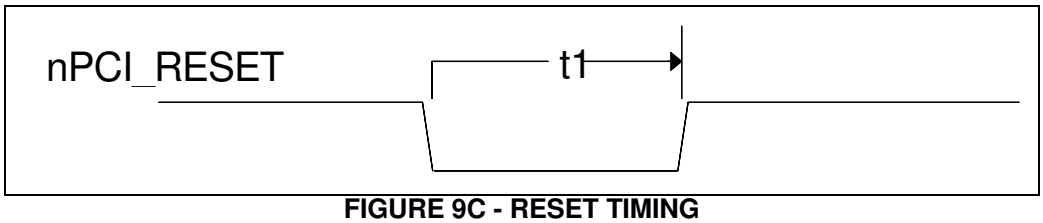


FIGURE 9C - RESET TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nPCI_RESET width	1			ms

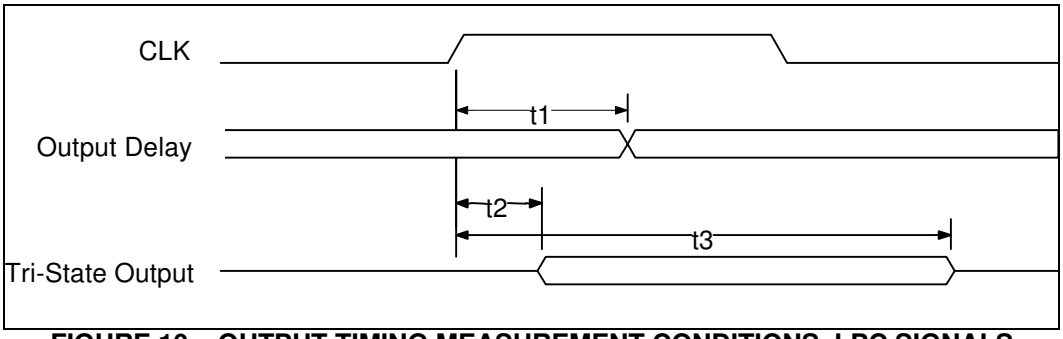


FIGURE 10 – OUTPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	CLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay	2		11	ns
t3	Active to Float Delay			28	ns

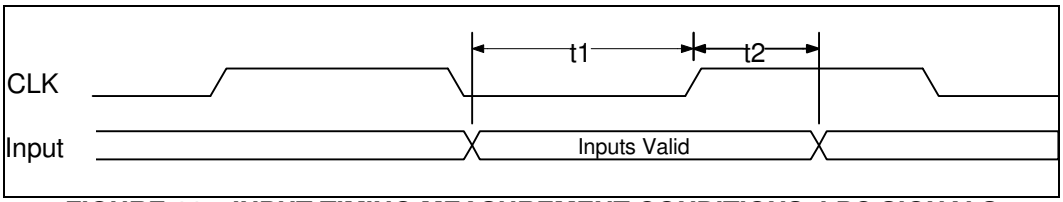
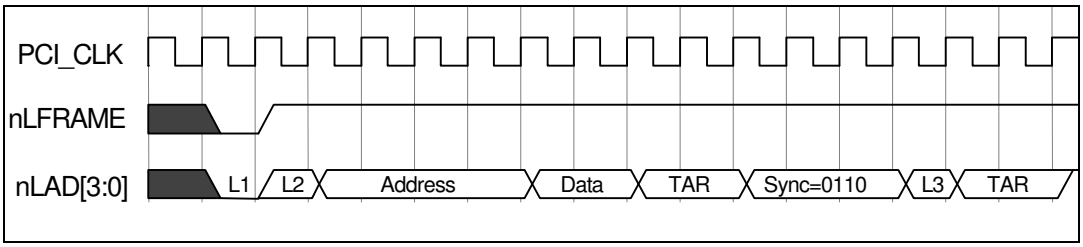


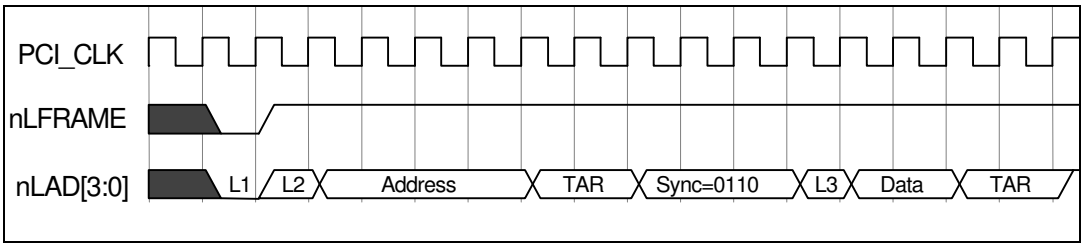
FIGURE 11 – INPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Input Set Up Time to CLK – Bused Signals	7			ns
t2	Input Hold Time from CLK	0			ns



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 12 – I/O WRITE



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 13 – I/O READ

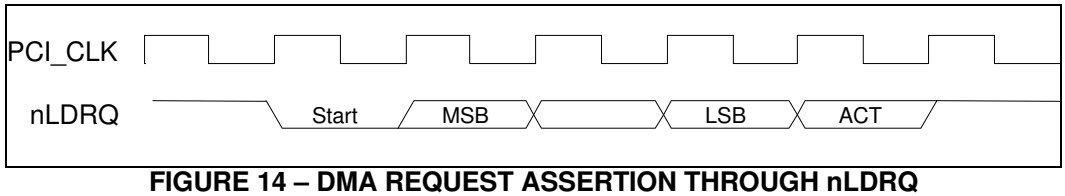
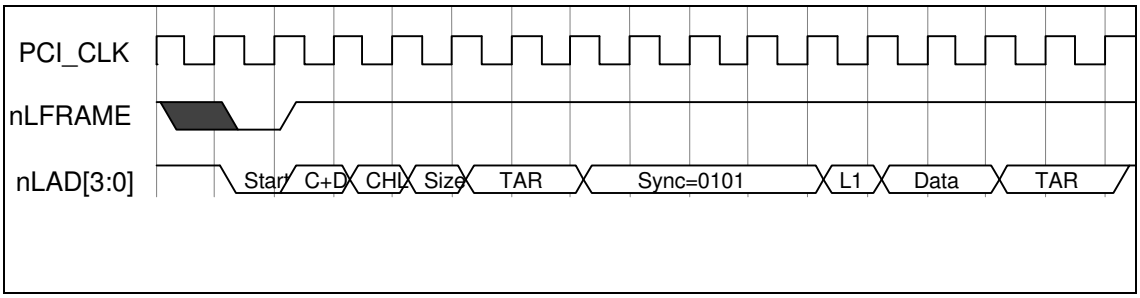
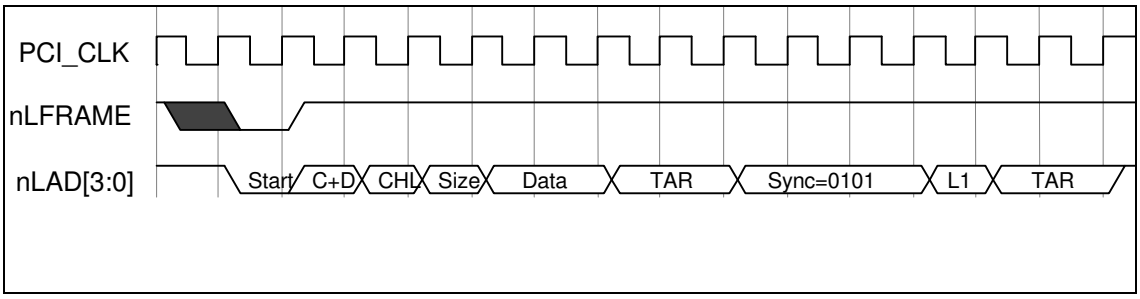


FIGURE 14 – DMA REQUEST ASSERTION THROUGH nLDRQ



Note: L1=Sync of 0000

FIGURE 15 – DMA WRITE (FIRST BYTE)



Note: L1=Sync of 0000

FIGURE 16 – DMA READ (FIRST BYTE)

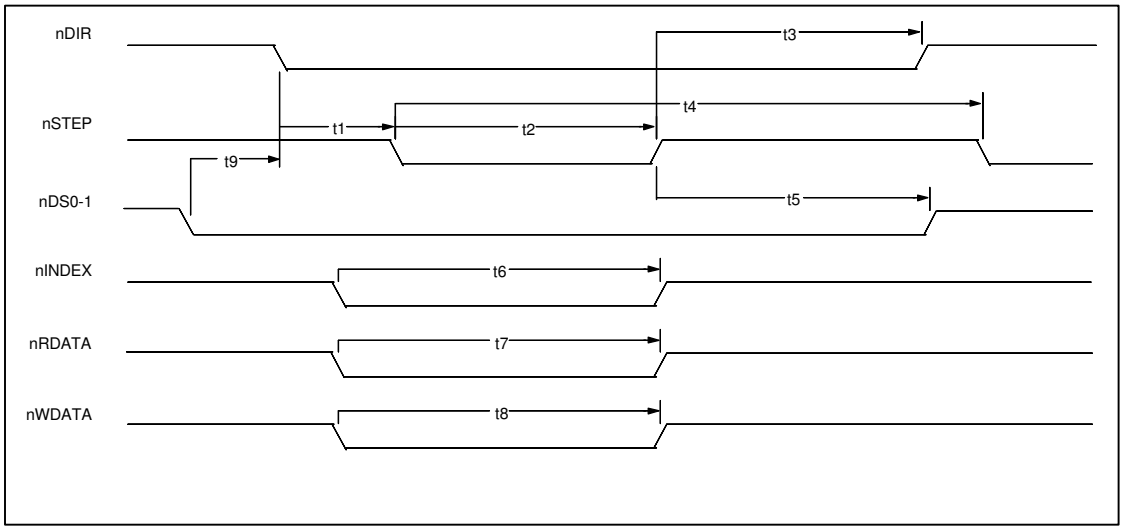


FIGURE 17 – FLOPPY DISK DRIVE TIMING (AT MODE ONLY)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDIR Set Up to STEP Low		4		X*
t2	nSTEP Active Time Low		24		X*
t3	nDIR Hold Time after nSTEP		96		X*
t4	nSTEP Cycle Time		132		X*
t5	nDS0-1 Hold Time from nSTEP Low (Note)		20		X*
t6	nINDEX Pulse Width		2		X*
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y*
t9	nDS0-1, Setup Time nDIR Low (Note)	0			ns

*X specifies one MCLK period and Y specifies one WCLK period.
MCLK = 16 x Data Rate (at 500 kb/s MCLK = 8 MHz)
WCLK = 2 x Data Rate (at 500 kb/s WCLK = 1 MHz)
Note: The nDS0-1 setup and hold times must be met by software.

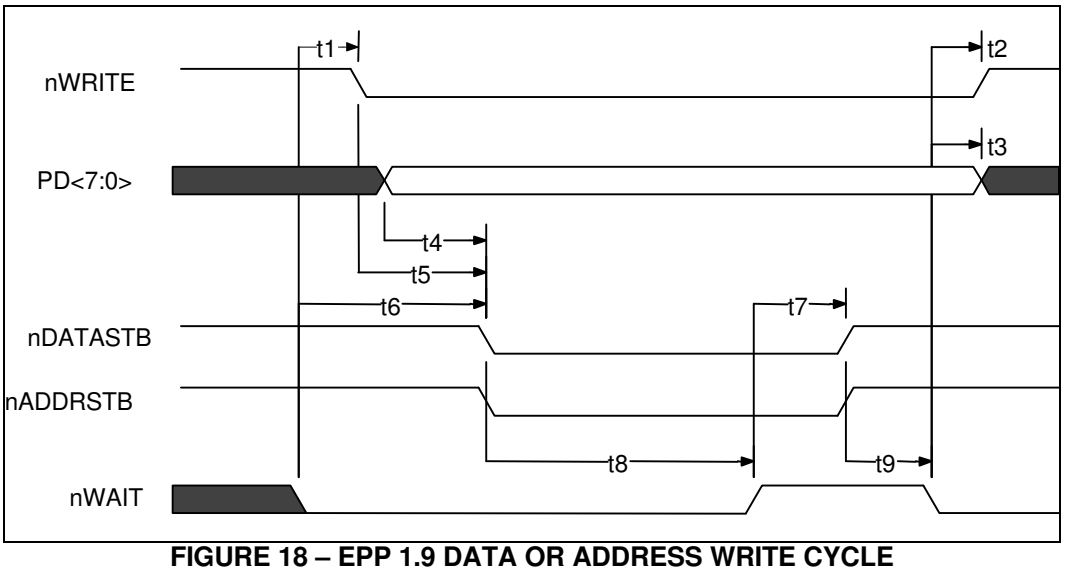


FIGURE 18 – EPP 1.9 DATA OR ADDRESS WRITE CYCLE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWAIT Asserted to nWRITE Asserted (Note 1)	60		185	ns
t2	nWAIT Asserted to nWRITE Change (Note 1)	60		185	ns
t3	nWAIT Asserted to PDATA Invalid (Note 1)	0			ns
t4	PDATA Valid to Command Asserted	10			ns
t5	nWRITE to Command Asserted	5		35	ns
t6	nWAIT Asserted to Command Asserted (Note 1)	60		210	ns
t7	nWAIT Deasserted to Command Deasserted (Note 1)	60		190	ns
t8	Command Asserted to nWAIT Deasserted	0		10	µs
t9	Command Deasserted to nWAIT Asserted	0			ns

Note 1: nWAIT must be filtered to compensate for ringing on the parallel bus cable. WAIT is considered to have settled after it does not transition for a minimum of 50 nsec.

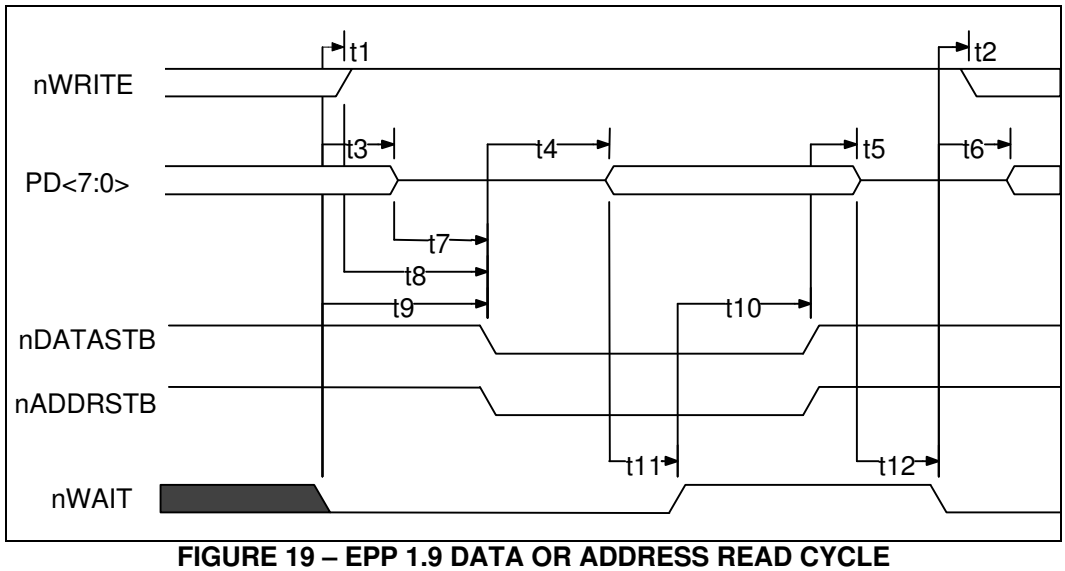


FIGURE 19 – EPP 1.9 DATA OR ADDRESS READ CYCLE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWAIT Asserted to nWRITE Deasserted	0		185	ns
t2	nWAIT Asserted to nWRITE Modified (Notes 1,2)	60		190	ns
t3	nWAIT Asserted to PDATA Hi-Z (Note 1)	60		180	ns
t4	Command Asserted to PDATA Valid	0			ns
t5	Command Deasserted to PDATA Hi-Z	0			ns
t6	nWAIT Asserted to PDATA Driven (Note 1)	60		190	ns
t7	PDATA Hi-Z to Command Asserted	0		30	ns
t8	nWRITE Deasserted to Command	1			ns
t9	nWAIT Asserted to Command Asserted	0		195	ns
t10	nWAIT Deasserted to Command Deasserted (Note 1)	60		180	ns
t11	PDATA Valid to nWAIT Deasserted	0			ns
t12	PDATA Hi-Z to nWAIT Asserted	0			µs

Note 1: nWAIT is considered to have settled after it does not transition for a minimum of 50 ns.
Note 2: When not executing a write cycle, EPP nWRITE is inactive high.

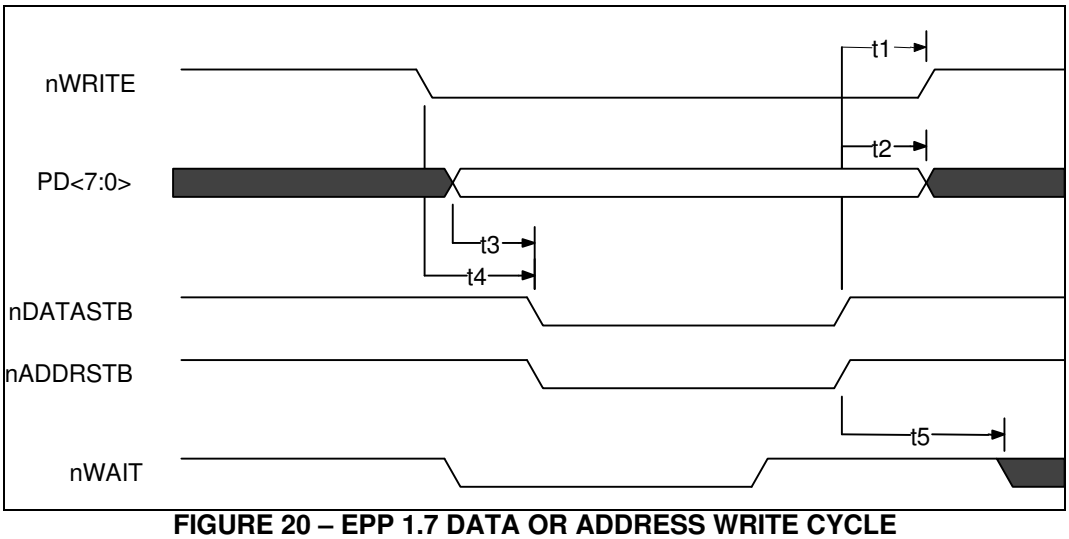


FIGURE 20 – EPP 1.7 DATA OR ADDRESS WRITE CYCLE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Command Deasserted to nWRITE Change	0		40	ns
t2	Command Deasserted to PDATA Invalid	50			ns
t3	PDATA Valid to Command Asserted	10		35	ns
t4	nWRITE to Command	5		35	ns
t5	Command Deasserted to nWAIT Deasserted	0			ns

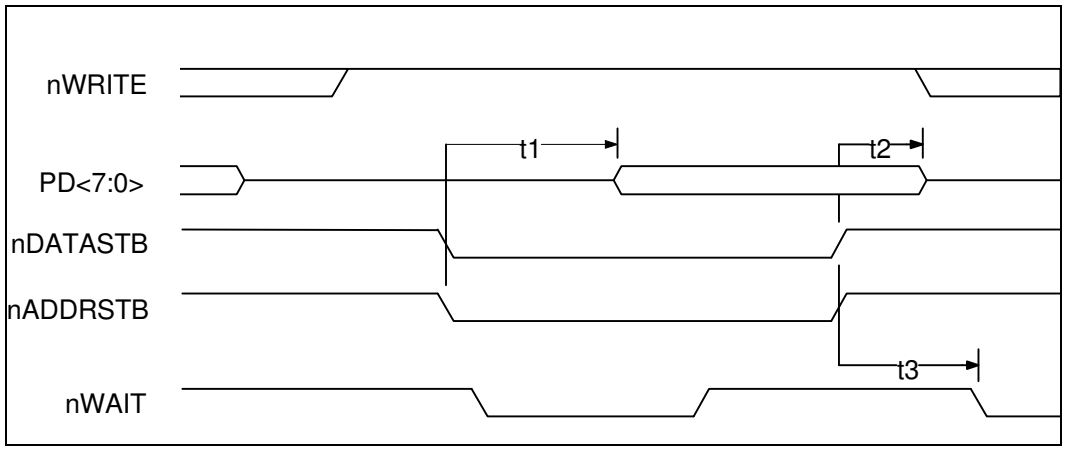


FIGURE 21 – EPP 1.7 DATA OR ADDRESS READ CYCLE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Command Asserted to PDATA Valid	0			ns
t2	Command Deasserted to PDATA Hi-Z	0			ns
t3	Command Deasserted to nWAIT Deasserted	0			ns

ECP Parallel Port Timing

Parallel Port FIFO (Mode 101)

The standard parallel port is run at or near the peak 500KBytes/sec allowed in the forward direction using DMA. The state machine does not examine nACK and begins the next transfer based on Busy. Refer to Figure 22.

ECP Parallel Port Timing

The timing is designed to allow operation at approximately 2.0 Mbytes/sec over a 15ft cable. If a shorter cable is used then the bandwidth will increase.

Forward-Idle

When the host has no data to send it keeps HostClk (nStrobe) high and the peripheral will leave PeriphClk (Busy) low.

Forward Data Transfer Phase

The interface transfers data and commands from the host to the peripheral using an interlocked PeriphAck and HostClk. The peripheral may indicate its desire to send data to the host by asserting nPeriphRequest.

The Forward Data Transfer Phase may be entered from the Forward-Idle Phase. While in the Forward Phase the peripheral may asynchronously assert the nPeriphRequest (nFault) to request that the channel be reversed. When the peripheral is not busy it sets PeriphAck (Busy) low. The host then sets HostClk (nStrobe) low when it is prepared to send data. The data must be stable for the specified setup time prior to the falling edge of HostClk. The peripheral then sets PeriphAck (Busy) high to acknowledge the handshake. The host then sets HostClk (nStrobe) high. The peripheral then accepts the data and sets PeriphAck (Busy) low, completing the transfer. This sequence is shown in Figure 23. The timing is designed to provide 3 cable round-trip times for data setup if Data is driven simultaneously with HostClk (nStrobe).

Reverse-Idle Phase

The peripheral has no data to send and keeps PeriphClk high. The host is idle and keeps HostAck low.

Reverse Data Transfer Phase

The interface transfers data and commands from the peripheral to the host using an interlocked HostAck and PeriphClk. The Reverse Data Transfer Phase may be entered from the Reverse-Idle Phase. After the previous byte has beed accepted the host sets HostAck (nALF) low. The peripheral then sets PeriphClk (nACK) low when it has data to send. The data must be stable for the specified setup time prior to the falling edge of PeriphClk. When the host is ready to accept a byte it sets HostAck (nALF) high to acknowledge the handshake. The peripheral then sets PeriphClk (nACK) high. After the host has accepted the data it sets HostAck (nALF) low, completing the transfer. This sequence is shown in Figure 24.

Output Drivers

To facilitate higher performance data transfer, the use of balanced CMOS active drivers for critical signals (Data, HostAck, HostClk, PeriphAck, PeriphClk) are used in ECP Mode. Because the use of active drivers can present compatibility problems in Compatible Mode (the control signals, by tradition, are specified as open-collector), the drivers are dynamically changed from open-collector to totem-pole. The timing for the dynamic driver change is specified in then IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July 14, 1993, available from Microsoft. The dynamic driver change must be implemented properly to prevent glitching the outputs.

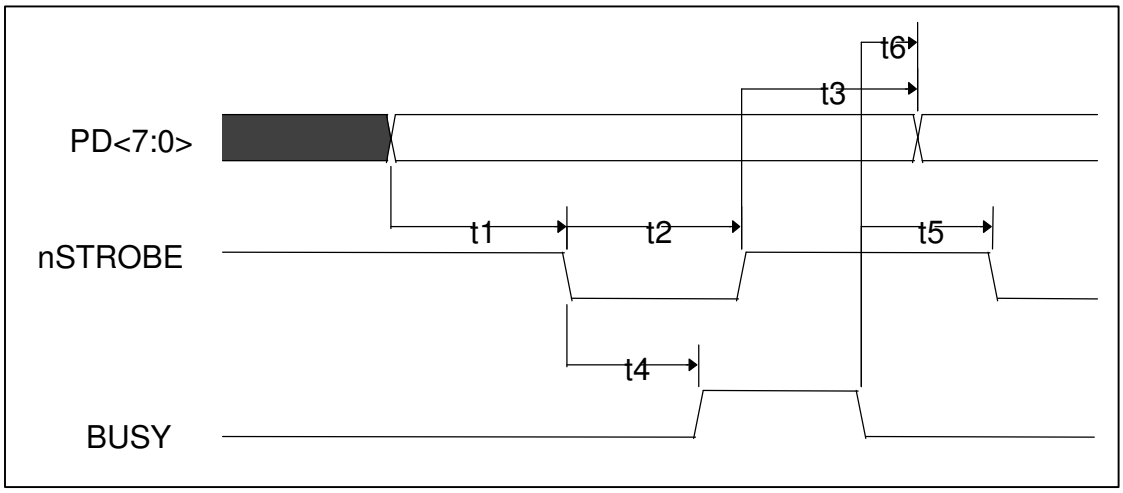


FIGURE 22 - PARALLEL PORT FIFO TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	PDATA Hold from nSTROBE Inactive (Note 1)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (Note 1)	80			ns

Note 1: The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

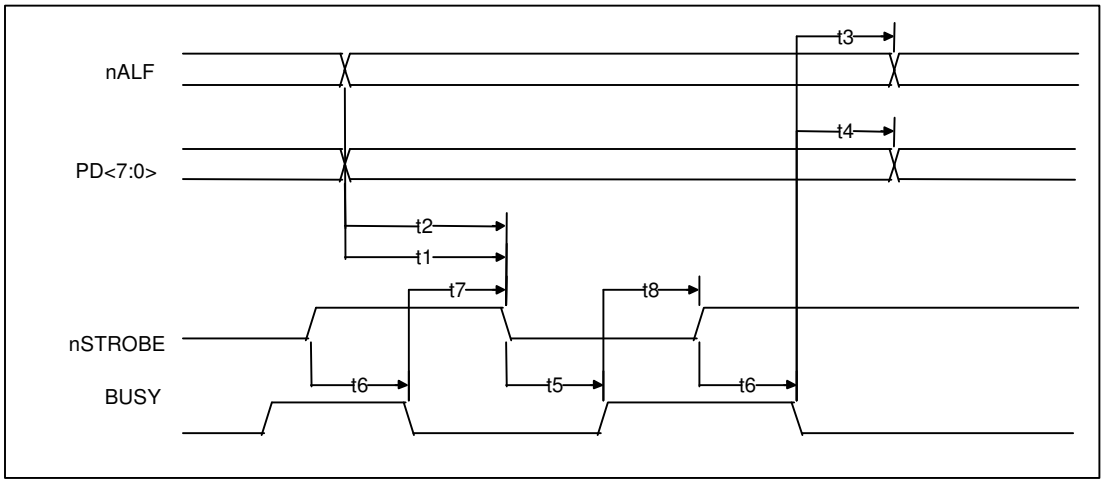


FIGURE 23 - ECP PARALLEL PORT FORWARD TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nALF Valid to nSTROBE Asserted	0		60	ns
t2	PDATA Valid to nSTROBE Asserted	0		60	ns
t3	BUSY Deasserted to nALF Changed (Notes 1,2)	80		180	ns
t4	BUSY Deasserted to PDATA Changed (Notes 1,2)	80		180	ns
t5	nSTROBE Deasserted to Busy Asserted	0			ns
t6	nSTROBE Deasserted to Busy Deasserted	0			ns
t7	BUSY Deasserted to nSTROBE Asserted (Notes 1,2)	80		200	ns
t8	BUSY Asserted to nSTROBE Deasserted (Note 2)	80		180	ns

Note 1: Maximum value only applies if there is data in the FIFO waiting to be written out.
Note 2: BUSY is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

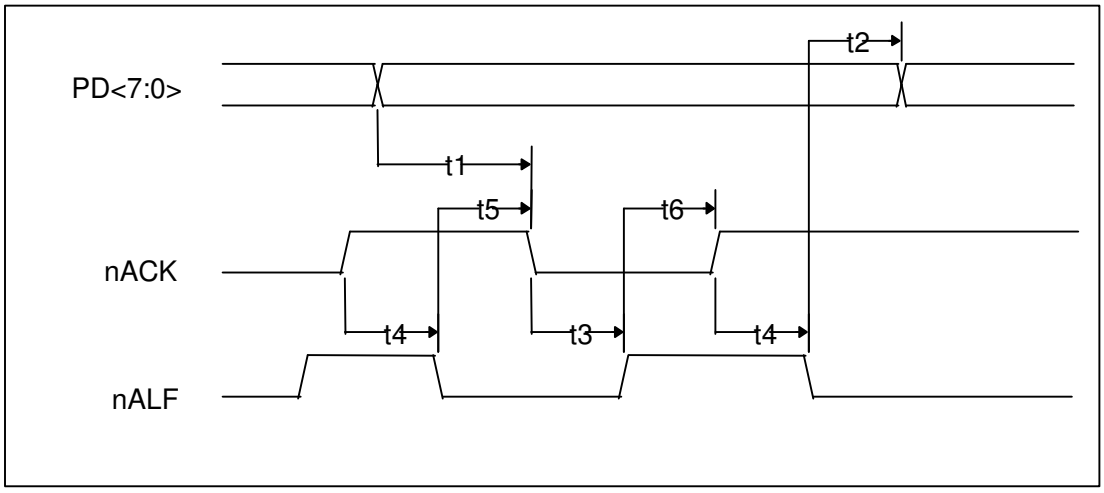
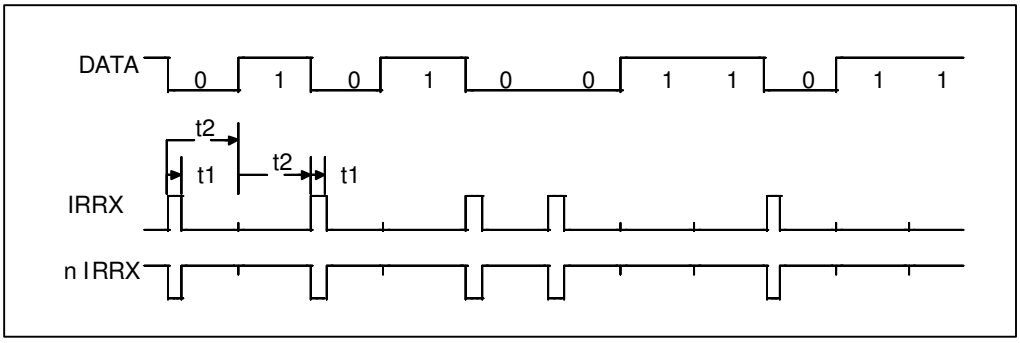


FIGURE 24 - ECP PARALLEL PORT REVERSE TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nACK Asserted	0			ns
t2	nALF Asserted to PDATA Changed	0			ns
t3	nACK Asserted to nALF Deasserted (Notes 1,2)	80		200	ns
t4	nACK Deasserted to nALF Asserted (Note 2)	80		200	ns
t5	nALF Asserted to nACK Asserted	0			ns
t6	nALF Deasserted to nACK Deasserted	0			ns

Note 1: Maximum value only applies if there is room in the FIFO and terminal count has not been received. ECP can stall by keeping nALF low.
Note 2: nACK is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

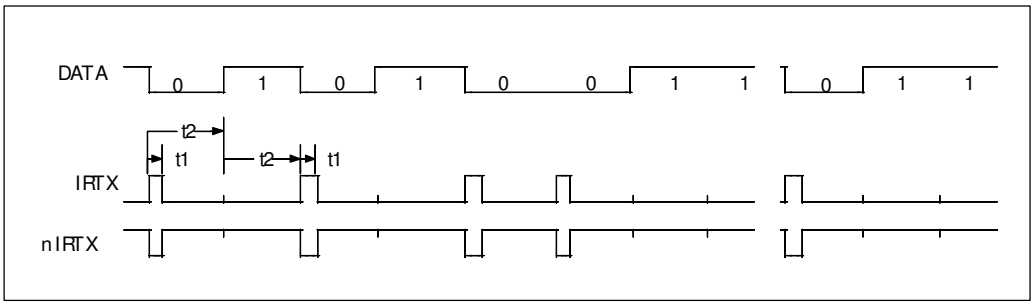


	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:

1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41µs.
2. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)

FIIGURE 25 - IrDA RECEIVE TIMING

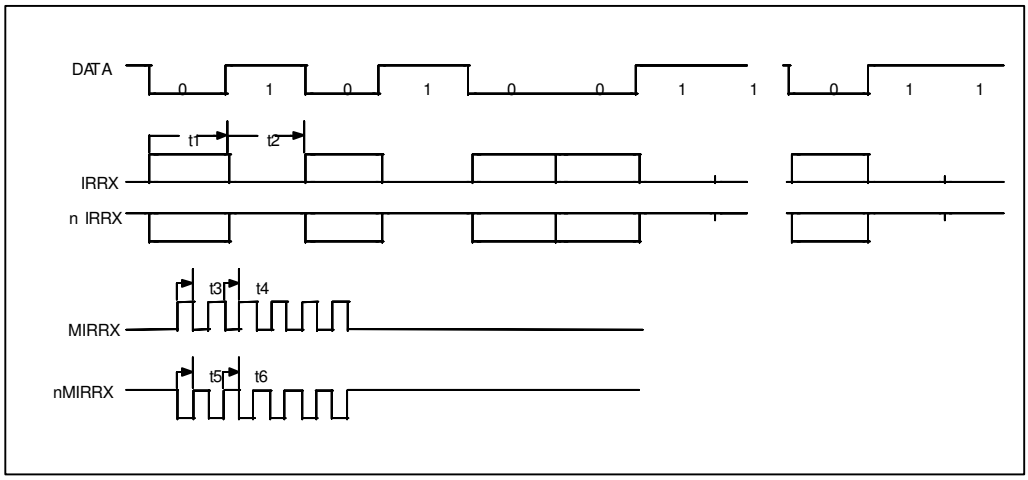


	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.41	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.41	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.41	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.41	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.41	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.41	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.41	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0

FIGURE 26 - IrDA TRANSMIT TIMING

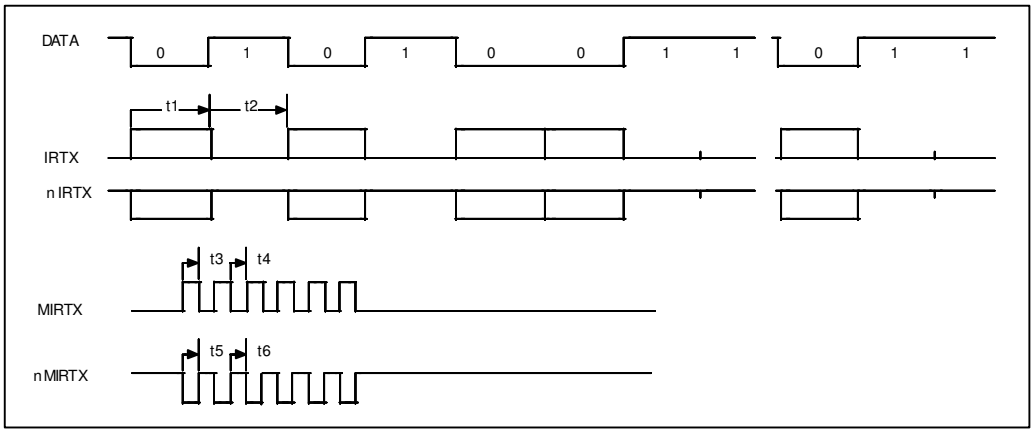


	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)
   MIRRX, nMIRRX are the modulated outputs

FIGURE 27 - AMPLITUDE SHIFT KEYED IR RECEIVE TIMING



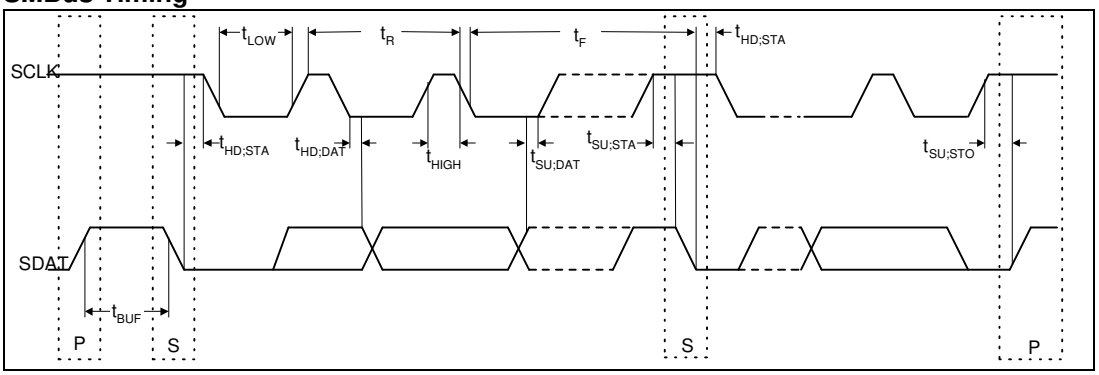
	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0
   MIRTX, nMIRTX are the modulated outputs

FIGURE 28 - AMPLITUDE SHIFT KEYED IR TRANSMIT TIMING

SMBus Timing



SYMBOL	PARAMETER	LIMITS		UNITS	COMMENTS
		MIN	MAX		
FSMB	SMB Operating Frequency	10	100	kHz	
TBUF	Bus free time between Stop and Start Condition	4.7		µs	
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	4.0		µs	
TSU:STA	Repeated Start Condition setup time	4.7		µs	
TSU:STO	Stop Condition setup time	4.0		µs	
THD:DAT	Data hold time	0		ns	
TSU:DAT	Data setup time	250		ns	
TTIMEOUT	Max. Clock low time	25	35	ms	See Note 1
TLOW	Clock low period	4.7		µs	
THIGH	Clock high period	4.0	50	µs	See Note 2
TLOW: SEXT	Cumulative clock low extend time (slave device)		25	ms	
TLOW: MEXT	Cumulative clock low extend time (master device)		10	ms	
TF	Clock/Data Fall Time		300	ns	
TR	Clock/Data Rise Time		1000	ns	

Note 1: A device will timeout when any clock low exceeds this value.
Note 2: Thigh Max provides a simple guaranteed method for devices to detect bus idle conditions.

X-Bus Timing

Note: The following timing values are based on a 33MHz PCI clock. Timing values will vary with variations in the PCI clock frequency.

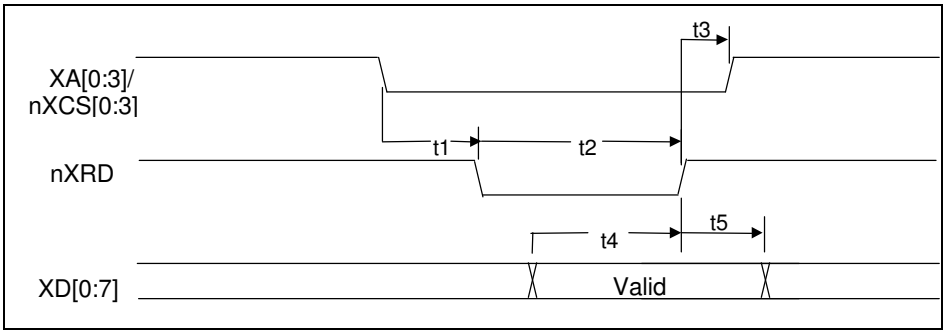


FIGURE 30 - X-BUS READ TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nXCS[0:3] active to nXRD active	100		190	ns
t2	nXRD active to nXRD inactive	A: 180 B: 300 C: 420 D: 540			ns
t3	nXRD inactive to nxCS[0:3] inactive	40			ns
t4	XD[0:7] valid to nXRD inactive	20			ns
t5	nXRD inactive to data invalid	0			ns

Note: Cases A-D for t2 correspond to the different pulse width options for the X-Bus read strobe. See the X-Bus Selection Configuration Register.

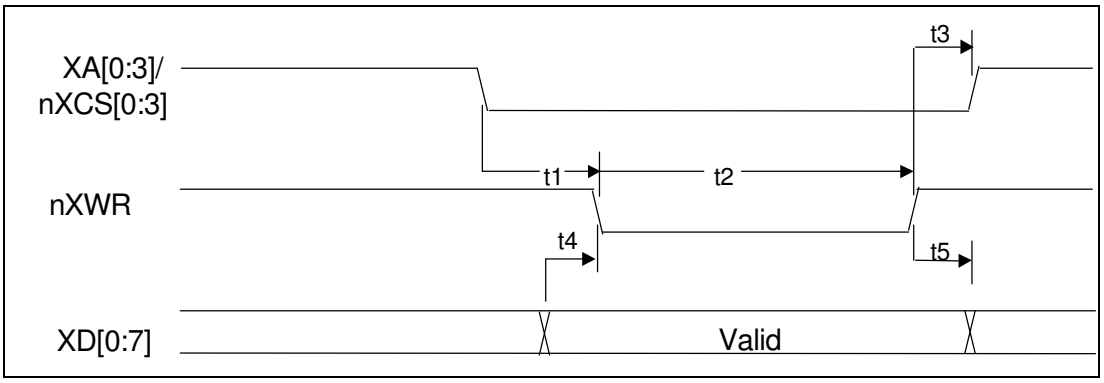


FIGURE 31 - X-BUS WRITE TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nXCS[0:3] active to nXWR active	100		190	ns
t2	nXWR active to nXWR inactive	A: 180 B: 300 C: 420 D: 540			ns
t3	nXWR inactive to nXCS[0:3] inactive	40			ns
t4	XD[0:7] valid to nXWR active	22			ns
t5	nXWR inactive to data invalid	45			ns

Note: Cases A-D for t2 correspond to the different pulse width options for the X-Bus write strobe. See the X-Bus Selection Configuration Register.

Representative LPC I/O Cycle to X-Bus Cycle Timing

X-Bus Read Cycle: LPC I/O Read Cycle – Data from X-Bus Device to Host

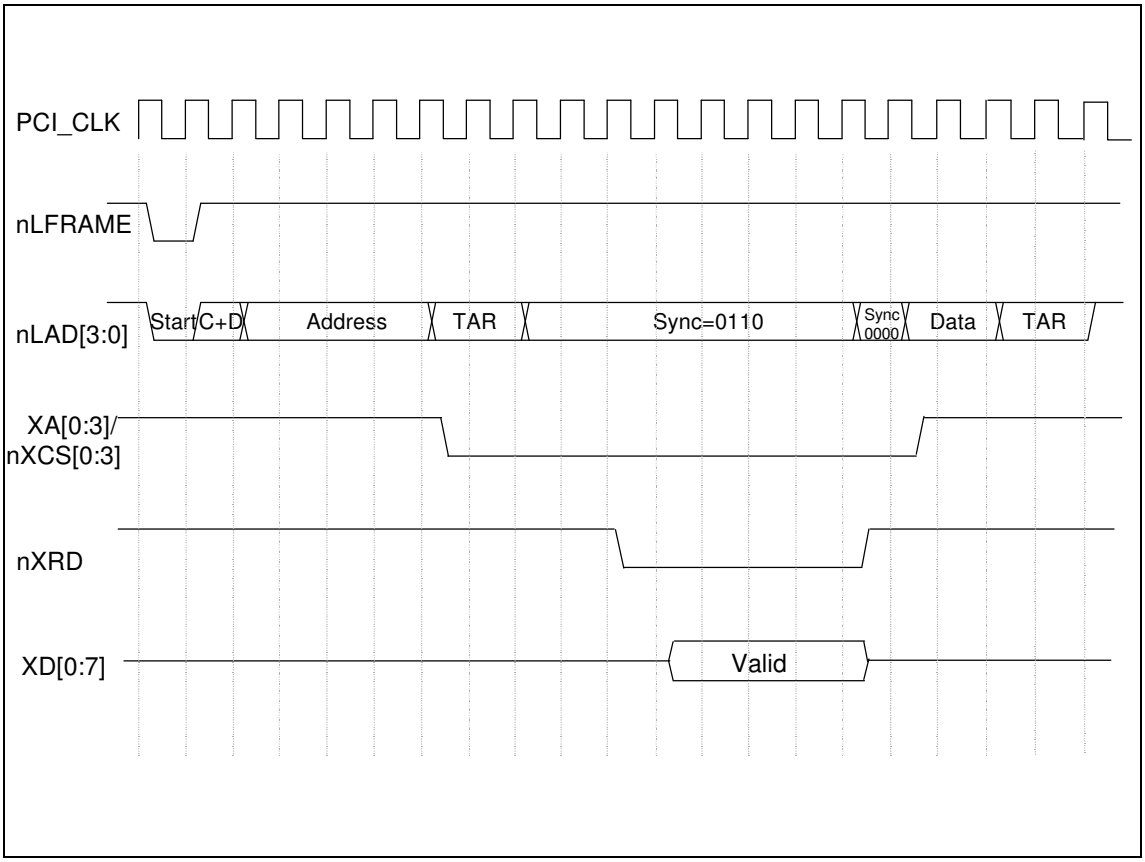


FIGURE 32 - X-BUS AND LPC I/O READ CYCLE

Note: Minimum read pulse width is shown.

X-Bus Write Cycle: LPC I/O Write Cycle - Data from Host to X-Bus Device

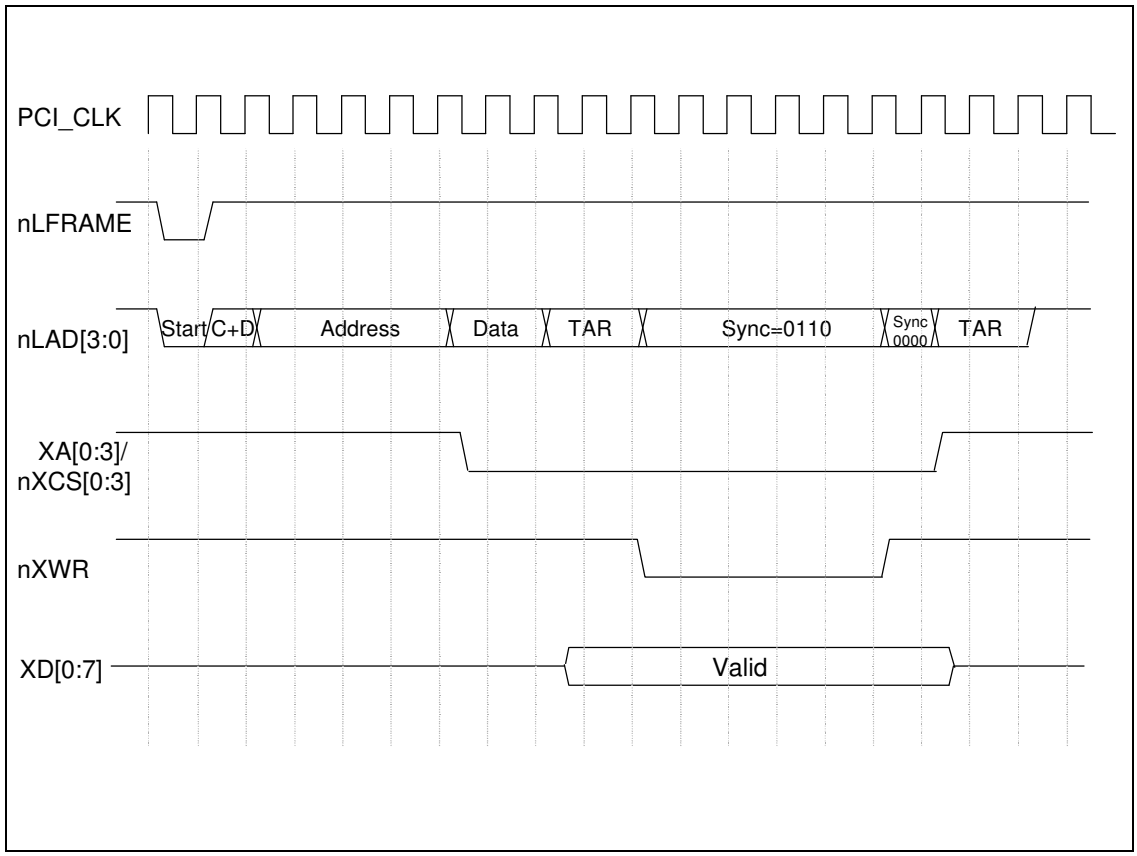


FIGURE 33 - X-BUS AND LPC I/O WRITE CYCLE

Note: Minimum write pulse width is shown.

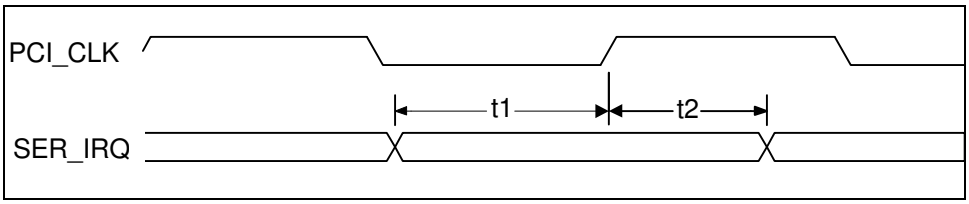


FIGURE 34 – SETUP AND HOLD TIME

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			nsec

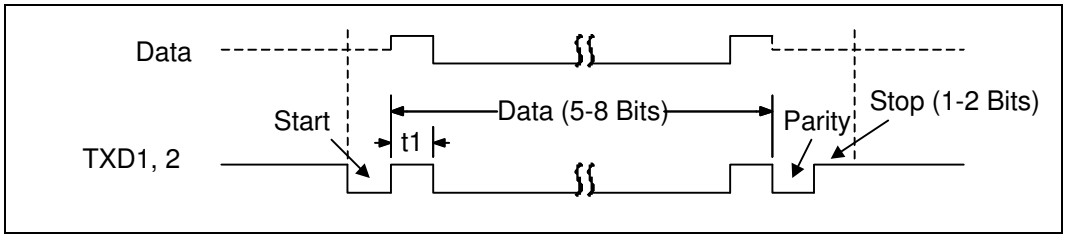


FIGURE 35 – SERIAL PORT DATA

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Serial Port Data Bit Time		t_{BR}[1]		nsec

Note 1: t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the “Baud Rate” table in the “Serial Port” section.

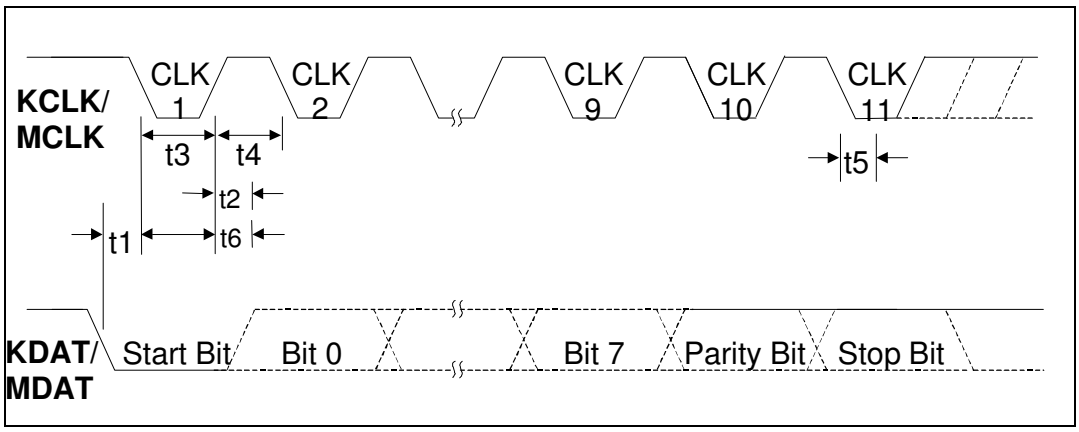


FIGURE 36 – KEYBOARD/MOUSE RECEIVE/SEND DATA TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Time from DATA transition to falling edge of CLOCK (Receive)	5		25	µsec
t2	Time from rising edge of CLOCK to DATA transition (Receive)	5		T4-5	µsec
t3	Duration of CLOCK inactive (Receive/Send)	30		50	µsec
t4	Duration of CLOCK active (Receive/Send)	30		50	µsec
t5	Time to keyboard inhibit after clock 11 to ensure the keyboard does not start another transmission (Receive)	>0		50	µsec
t6	Time from inactive to active CLOCK transition, used to time when the auxiliary device samples DATA (Send)	5		25	µsec

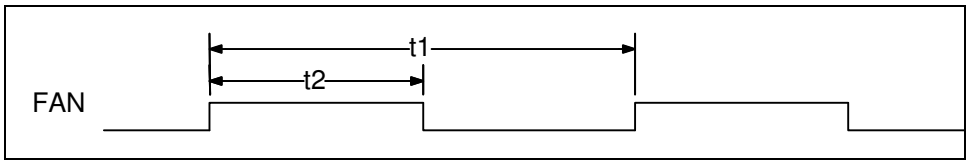


FIGURE 37 – FAN OUTPUT TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PWM Period (Note 1)	0.021		25.8	msec
t2	PWM High Time (Note 2)	0.00033		25.4	msec

Note 1: The period is $1/f_{out}$, where f_{out} is programmed through the FANx and Fan Control registers. The tolerance on f_{out} is +/- 3%.

Note 2: When Bit 0 of the FANx registers is 0, then the duty cycle is programmed through Bits[6:1] of these registers. If Bits[6:1] = "000000" then the FANx pin is low. The duty cycle is programmable through Bits[6:1] to be between 1.56% and 98.44%. When Bit 0 is 1, the FANx pin is high.

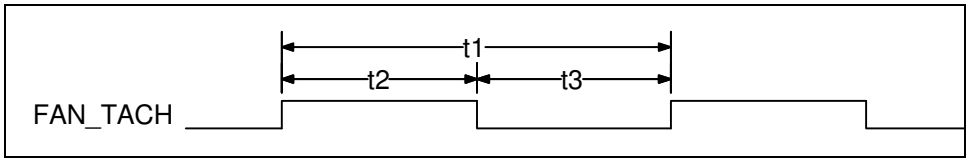


FIGURE 38 – FAN TACHOMETER INPUT TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Pulse Time (1/2 Revolution Time=30/RPM)	$4t_{TACH}$[1]			µsec
t2	Pulse High Time	$3t_{TACH}$[1]			µsec
t3	Pulse Low Time	t_{TACH}			µsec

Note 1: t_{TACH} is the clock used for the tachometer counter. It is 30.52 * DVSR, where the divisor (DVSR) is programmed in the Fan Control register.

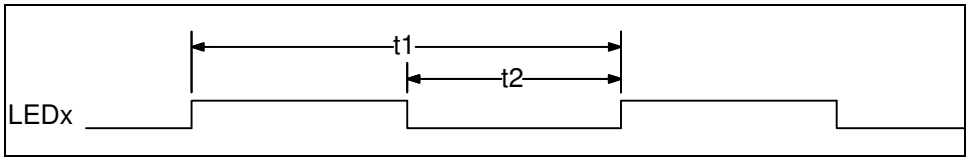
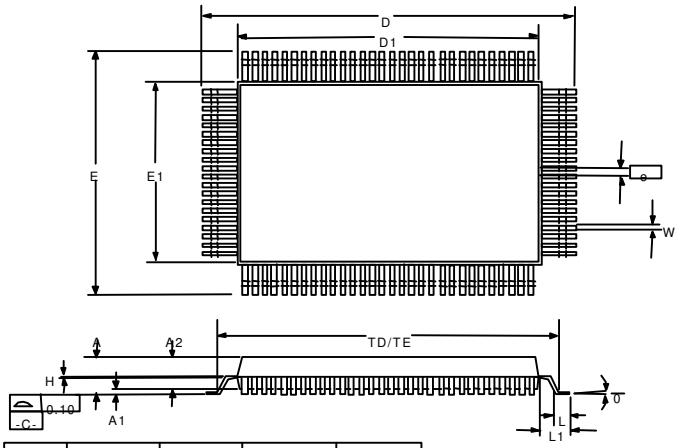


FIGURE 39 – LED OUTPUT TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Period	1		2	sec
t2	Blink ON Time	0		0.5[1]	sec

Note 1: The blink rate is programmed through Bits[1:0] in LEDx register. When Bits[1:0]=00, LED is OFF. Bits[1:0]=01 indicates LED blink at 1Hz rate with a 50% duty cycle (0.5 sec ON, 0.5 sec OFF). Bits[1:0]=10 indicates LED blink at ½ Hz rate with a 25% duty cycle (0.5 sec ON, 1.5 sec OFF). When Bits[1:0]=11, LED is ON.

PACKAGE OUTLINE



DIM	MIN	MAX	MIN	MAX
A	2.80	3.15	.110	.124
A1	0.1	0.45	.004	.018
A2	2.57	2.87	101	113
D	23.4	24.15	.921	.951
D1	19.9	20.1	.783	.791
E	17.4	18.15	.685	.715
E1	13.9	14.1	.547	.555
H	0.1	0.2	.004	.008
L	0.65	0.95	.026	.037
L1	1.8	2.6	.071	.102
e	0.65 BSC		.0256 BSC	
θ	0°	12°	0°	12°
W	.2	.4	.008	.016
TD(1)	21.8	22.2	.858	.874
TE(1)	15.8	16.2	.622	.638
TD(2)	22.21	22.76	.874	.896
TE(2)	16.27	16.82	.641	.662

Notes:

1) Coplanarity is 0.100mm (.004") maximum.
2) Tolerance on the position of the leads is 0.200mm (.008") maximum.
3) Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25mm (.010").
4) Dimensions TD and TE are important for testing by robotic handler. Only above combinations of (1) or (2) are acceptable.
5) Controlling dimension: millimeter. Dimensions in inches for reference only and not necessarily accurate.

FIGURE 40 - 100 PIN QFP PACKAGE OUTLINE

APPENDIX - TEST MODES

Board Test Mode
Board test mode can be entered as follows:
On the rising (deasserting) edge of nPCI_RESET, drive nLFRAME low and drive LAD[0] low.
Exit board test mode as follows:
On the rising (deasserting) edge of nPCI_RESET, drive either nLFRAME or LAD[0] high.

See the “XNOR-Chain Test Mode” section below for a description of this board test mode.

XNOR-Chain Test Mode
XNOR-Chain test structure allows users to confirm that all pins are in contact with the motherboard during assembly and test operations. See Figure 41 below.

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the LPC47S42x pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

The nPCI_RESET pin is not included in the XNOR-Chain. The XNOR-Chain output is on pin 52, GP31/FAN_TACH. See the following sub-sections for more details.

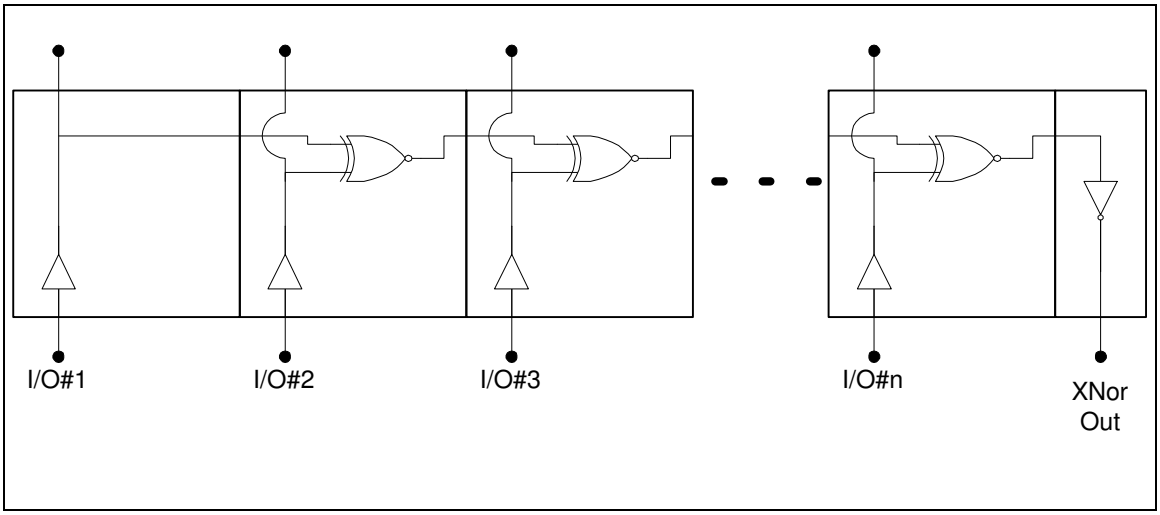


FIGURE 41 – XNOR-CHAIN TEST STRUCTURE

Introduction

The LPC47S42x provides board test capability through the XNOR chain. When the chip is in the XNOR chain test mode, setting the state of any of the input pins to the opposite of its current state will cause the output of the chain to toggle.

All pins on the chip are inputs to the XNOR chain, with the exception of the following:

1. VCC (pins 53, 65 & 93) and VTR (pin 18)
2. VSS (pins 7, 31, 60, & 76)
3. GP31/FAN_TACH (pin 52). This is the chain output.
4. nPCI_RESET (pin 26)

To put the chip in the XNOR chain test mode, tie LAD0 (pin 20) and nLFRAME (pin 24) low. Then toggle nPCI_RESET (pin 26) from a low to a high state. Once the chip is put into XNOR chain test mode, LAD0 (pin 20) and nLFRAME (pin 24) become part of the chain.

To exit the XNOR chain test mode tie LAD0 (pin 20) or nLFRAME (pin 24) high. Then toggle nPCI_RESET (pin 26) from a low to a high state. A VCC POR will also cause the XNOR chain test mode to be exited. To verify the test mode has been exited, observe the output on GP31/FAN_TACH (pin 52). Toggling any of the input pins should not cause its state to change.

Setup

Warning: Ensure power supply is off during setup.

1. Connect VSS (pins 7, 31, 60, & 76) to ground.
2. Connect VCC (pins 53, 65 & 93) and VTR (pin 18) to VCC (3.3V).
3. Connect an oscilloscope or voltmeter to GP31/FAN_TACH (pin 52).
4. All other pins should be tied to ground.

Testing

1. Turn power on.
2. With LAD0 (pin 20) and nLFRAME (pin 24) low, bring nPCI_RESET (pin 26) high. The chip is now in XNOR chain test mode. At this point, all inputs to the XNOR chain are low. The output on GP31/FAN_TACH (pin 52) should also be low. Refer to INITIAL CONFIG on Truth Table 1.
3. Bring pin 100 high. The output on GP31/FAN_TACH (pin 52) should go high. Refer to STEP ONE on Truth Table 1.
4. In descending pin order, bring each input high. The output should switch states each time an input is toggled. Continue until all inputs are high. The output on GP31/FAN_TACH should now be low. Refer to END CONFIG on Truth Table 1.
5. The current state of the chip is now represented by INITIAL CONFIG in Truth Table 2.
6. Each input should now be brought low, starting at pin one and continuing in ascending order. Continue until all inputs are low. The output on GP31/FAN_TACH should now be low. Refer to Truth Table 2.
7. To exit test mode, tie LAD0 (pin 20) or nLFRAME (pin 24) high, and toggle nPCI_RESET from a low to a high state.

TRUTH TABLE 1 - Toggling Inputs in Descending Order

	PIN 100	PIN 99	PIN 98	PIN 97	PIN 96	PIN ...	PIN 1	OUTPUT PIN 52
INITIAL CONFIG	L	L	L	L	L	L	L	L
STEP 1	H	L	L	L	L	L	L	H
STEP 2	H	H	L	L	L	L	L	L
STEP 3	H	H	H	L	L	L	L	H
STEP 4	H	H	H	H	L	L	L	L
STEP 5	H	H	H	H	H	L	L	H
…	…	…	…	…	…	…	…	…
STEP N	H	H	H	H	H	H	L	H
END CONFIG	H	H	H	H	H	H	H	L

TRUTH TABLE 2 - Toggling Inputs in Ascending Order

	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN ...	PIN 100	OUTPUT PIN 52
INITIAL CONFIG	H	H	H	H	H	H	H	L
STEP 1	L	H	H	H	H	H	H	H
STEP 2	L	L	H	H	H	H	H	L
STEP 3	L	L	L	H	H	H	H	H
STEP 4	L	L	L	L	H	H	H	L
STEP 5	L	L	L	L	L	H	H	H
	…	…	…	…	…	…	…	…
STEP N	L	L	L	L	L	L	H	L
END CONFIG	L	L	L	L	L	L	L	L

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