

**RF Signal Processing Servo Amplifier for CD Player**

**Description**

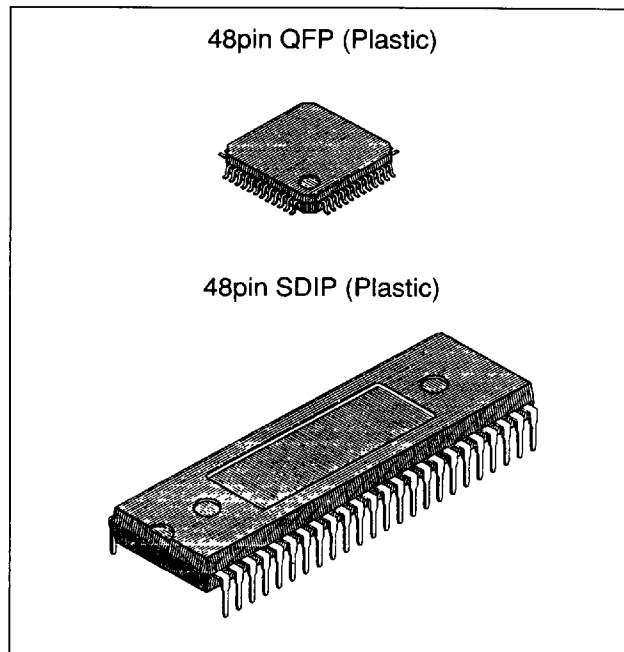
The CXA1372 is a bipolar IC developed for RF signal processing (focus OK, mirror, defect detection, EFM comparator) and servo control.

**Features**

- Single power supply, 5V
- Low power consumption
- Fewer external parts
- Built-in circuit for effective disc defect measures
- Share serial data bus from the microcomputer with CXD2500
- Fully compatible with CXA1182 for microcomputer software

**Functions**

- Auto asymmetry control
- Focus OK detection circuit
- Mirror detection circuit
- Defects detection, counter measures circuit
- EFM comparator
- Focus servo control
- Tracking servo control
- Sled servo control



**Structure**

Silicon monolithic IC

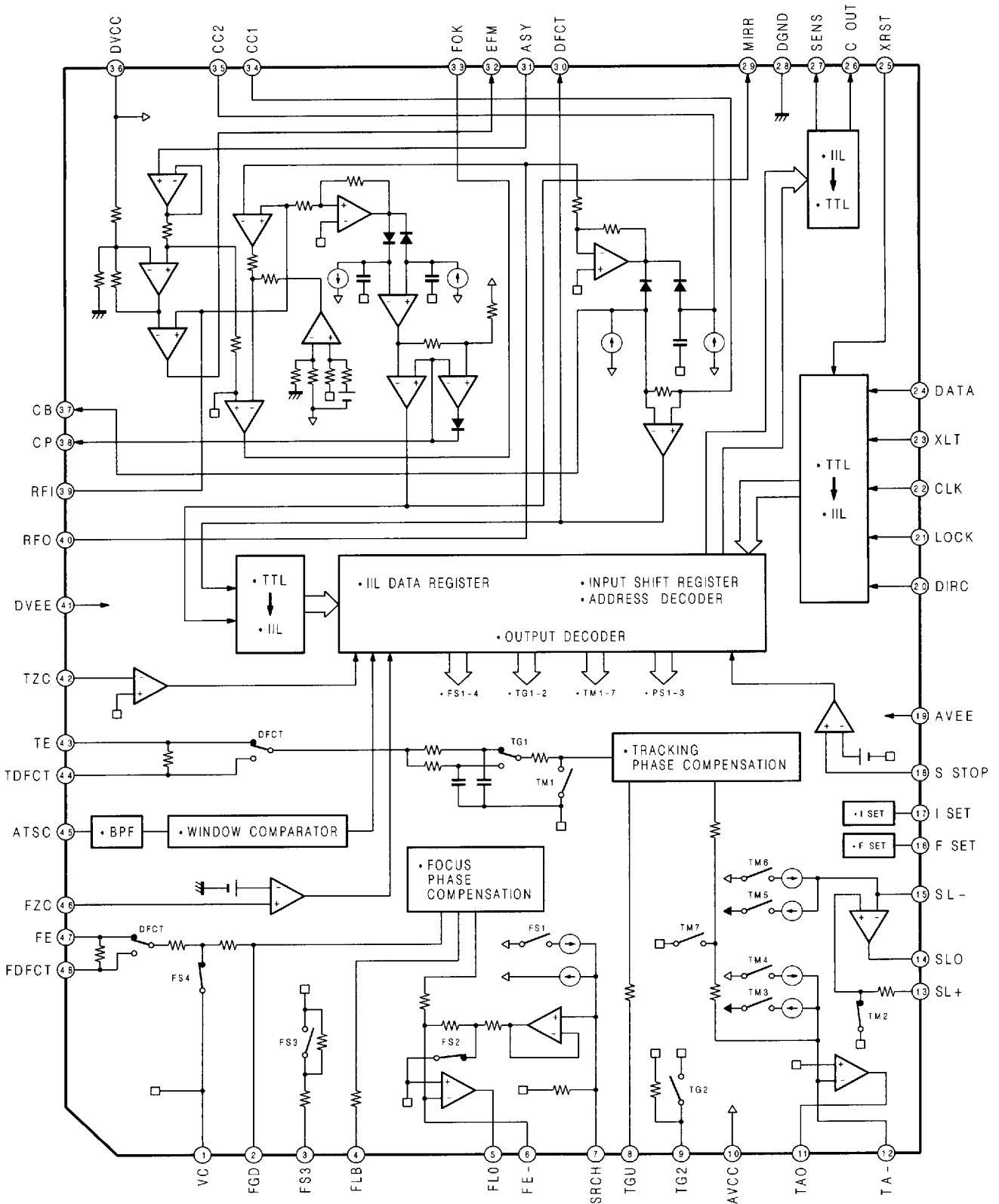
**Absolute Maximum Ratings (Ta = 25°C)**

• Supply voltage	VCC - VEE	12	V
• Operating temperature	Topr	-20 to +75	°C
• Storage temperature	Tstg	-55 to +150	°C
• Allowable power dissipation	PD	CXA1372S	833 mW
		CXA1372Q	457 mW

**Recommended Operating Conditions**

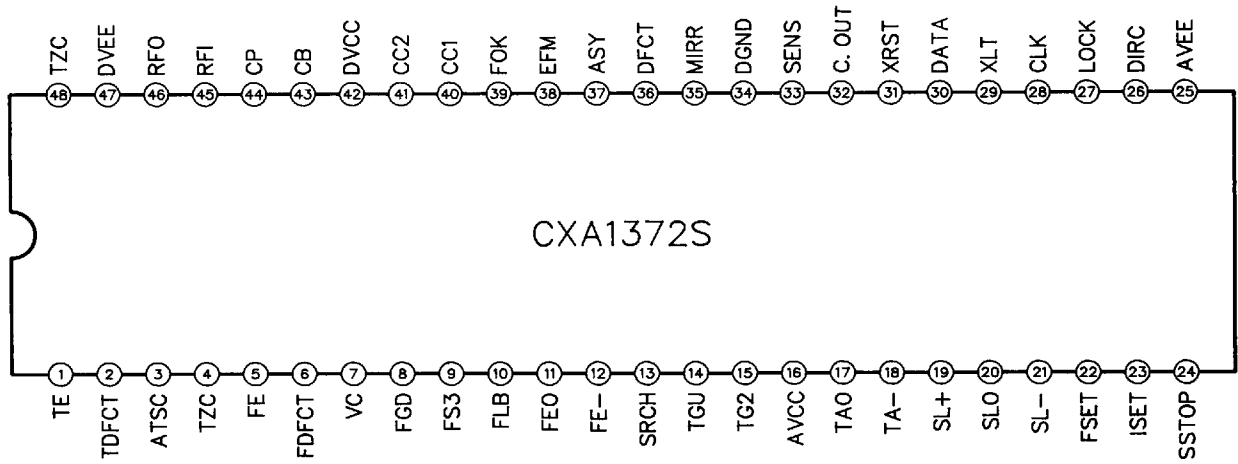
VCC - VEE	3.6 to 11	V
VCC - DGND	3.6 to 5.5	V

CXA1372Q Block Diagram

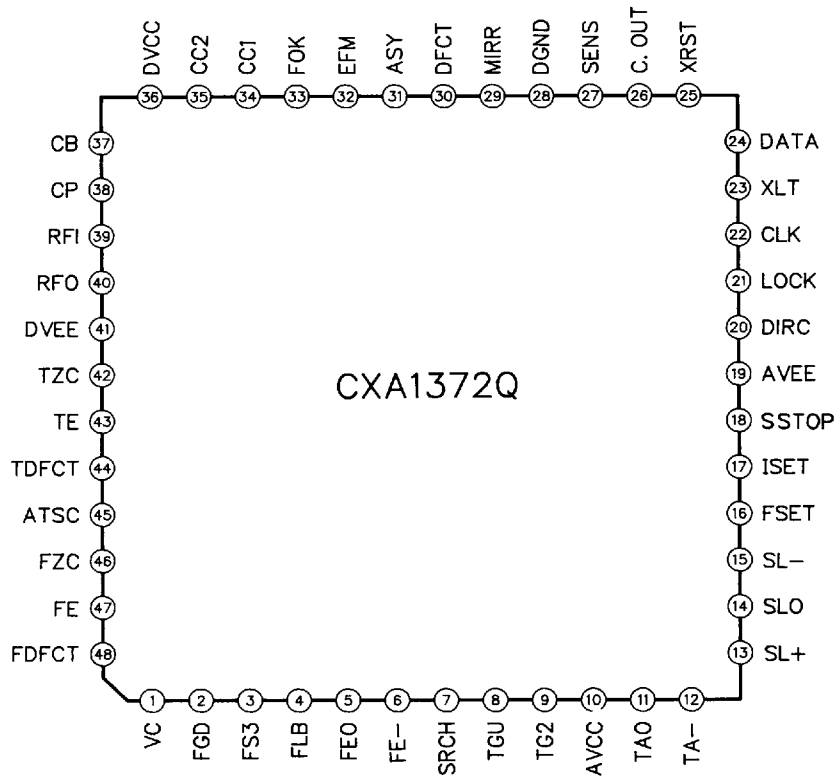


Pin Configuration

CXA1372S



CXA1372Q



Pin Description

Pin No.		Symbol	I/O	Equivalent circuit	Description
Q	S				
1	7	VC	I		Center voltage input pin For dual power: GND For single power supply: $(V_{cc} + GND)/2$
2	8	FGD	I		Connect a capacitor between this pin and pin 3 to reduce high-frequency gain.
3	9	FS3	I		The high-frequency gain of the focus servo is switched through FS3 On and OFF.
4	10	FLB	I		Time constant external pin to raise the low bandwidth of the focus servo.
5	11	FEO	O		Focus drive output.
11	17	TAO	O		Tracking drive output.
14	20	SLO	O		Sled drive output.
6	12	FE-	I		Inverse input pin for focus amplifier.

Pin No.		Symbol	I/O	Equivalent circuit	Description
Q	S				
7	13	SRCH	I		Time constant external pin for the formation of focus search waveforms.
8	14	TGU	I		Time constant external pin for the selection of tracking high band gain.
9	15	TG2	I		Time constant external pin for the selection of tracking high band gain.
12	18	TA-	I		Inverse input pin for tracking amplifier.
13	19	SL+	I		Non-inverse input pin for sled amplifier.
15	21	SL-	I		Inverse input pin for sled amplifier.

Pin No.		Symbol	I/O	Equivalent circuit	Description
Q	S				
16	22	FSET	I		Pin to set peak frequency of focus tracking phase compensation and fo of CLV LPF.
17	23	ISET	I		Current is input to determine focus search, track jump, and sled kick height.
18	24	SSTOP	I		Limit SW ON/OFF signal detection pin for disc inner periphery detection.
20	26	DIRC	I		Pin for one-track jump. Contains a 47kΩ pull-up resistor.
21	27	LOCK	I		At "L" sled runaway prevention circuit operates. Contains a 47kΩ pull-up resistor.
22	28	CLK	I		Serial data transfer clock input from CPU.
23	29	XLT	I		Latch input from CPU.
24	30	DATA	I		Serial data input from CPU.
25	31	XRST	I		Reset input pin, reset at "L".
26	32	SENS	O		Outputs FZC, AS, TZC and SSTOP through command from CPU.
27	33	C. OUT	O		Track number count signal output.

Pin No.		Symbol	I/O	Equivalent circuit	Description
Q	S				
29	35	MIRR	O		MIRR comparator output pin.
38	44	CP	I		Connecting pin of MIRR hold condenser. Non-inverted input pin of MIRR comparator.
34	40	CC1	I		Output pin of DEFECT bottom hold.
35	41	CC2	O		Input pin for the capacitance coupled output of DEFECT bottom hold.
30	36	DFCT	O		Output pin of DEFECT comparator.
37	43	CB	I		Connection pin of DEFECT bottom hold capacitor.
31	37	ASY	I		Input pin of auto asymmetry control.
32	38	EFM	O	<p>Depending on power supply Current source (Vcc to D<sub>GND</sub>)</p>	Output pin of EFM comparator.
33	39	FOK	O		Output pin of FOK comparator.

Pin No.		Symbol	I/O	Equivalent circuit	Description
Q	S				
39	45	RFI	I		Input pin with coupling capacitor where RF summing amplifier output is connected.
40	46	RFO	O		Output pin of RF summing amplifier and check point of eye pattern.
42	48	TZC	I		Input pin of tracking zero-cross comparator.
43	1	TE	I		Input pin of tracking error amplifier.
44	2	TDFCT	I		Capacitor connecting pin for time constant during defects.
45	3	ATSC			Window comparator input pin for ATSC detection.
46	4	FZC	I		Pin for focus zero-cross comparator input.
47	5	FE	I		Input pin of focus error.
48	6	FDFCT	I		Capacitor connecting pin for time constant during defect functions.



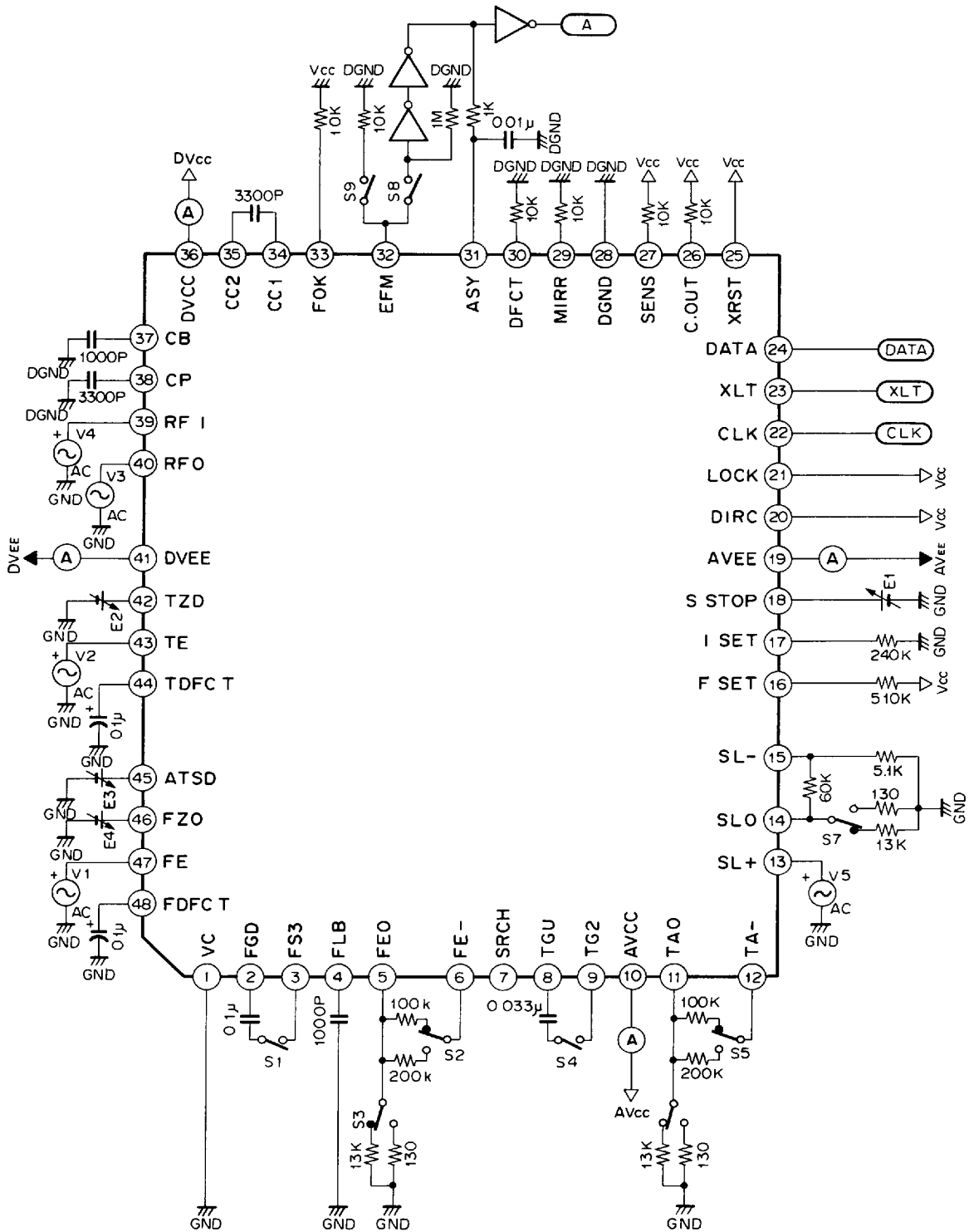
Electrical Characteristics Ta=25°C, Vcc=+2.5V, VEE=-2.5V, D.GND=-2.5V

No.	Item	Symbol	SW condition										Bias condition				Test point	Output waveform and description of test method	Min.	Typ.	Max.	Unit		
			S1	S2	S3	S4	S5	S6	S7	S8	S9	SD	E1	E2	E3	E4								
1	Current consumption	Icc																	8	19	27	mA		
2	Current consumption	IEE																	-8	-16	-22	mA		
3	DC voltage gain	GFE0																00	08	18.0	21.0	24.0	dB	
4	Field through	VFE0F																00	00				-35	dB
5	Max. output voltage	VFE01																08	08	2.0				V
6	Max. output voltage	VFE02																08	08				-2.0	V
7	Max. output voltage	VFE03																08	08	1.2				V
8	Max. output voltage	VFE04																08	08				-1.2	V
9	Search output voltage	VSRCH1																02	02	-640			-360	mV
10	Search output voltage	VSRCH2																03	03	360			640	mV
11	FZC threshold	VZC																00	00	39	50	61		mV
12	DC voltage gain	GTE0																25	25	11.6	14.6	17.6		dB
13	Field through	VTE0F																00	00				-39	dB
14	Max. output voltage	VTE01																25	25	2.0				V
15	Max. output voltage	VTE02																25	25				-2.0	V
16	Max. output voltage	VTE03																25	25	1.2				V
17	Max. output voltage	VTE04																25	25				-1.2	V
18	Jump output voltage	VJUMP1																2C	2C	-640			-360	mV
19	Jump output voltage	VJUMP2																28	28	360			640	mV
20	ATSC threshold	VATSC1																20	20	-45	-26	-7		mV
21	ATSC threshold	VATSC2																20	20	7	26	-45		mV
22	TZC threshold	VTZC																20	20	-20	0	20		mV

No.	Item	Symbol	SW condition										Bias condition				Test point	Output waveform and description of test method	Min.	Typ.	Max.	Unit					
			S1	S2	S3	S4	S5	S6	S7	S8	S9	SD	E1	E2	E3	E4											
23	DC voltage gain	G <sub>sLO</sub>															25					14	V <sub>s</sub> =10Hz, 20mVp-p Open loop gain	50			dB
24	Field through	V <sub>sLOF</sub>															00					14	V <sub>s</sub> =10kHz, 100mVp-p Difference in gain when SD=00 and SD=25			-34	dB
25	Max. output voltage	V <sub>sLO1</sub>															25					14	V <sub>s</sub> =1.0Vdc	2.0			V
26	Max. output voltage	V <sub>sLO2</sub>															25					14	V <sub>s</sub> =-1.0Vdc			-2.0	V
27	Max. output voltage	V <sub>sLO3</sub>											○				25					14	V <sub>s</sub> =1.0Vdc	2.0			V
28	Max. output voltage	V <sub>sLO4</sub>											○				25					14	V <sub>s</sub> =-1.0Vdc			-2.0	V
29	Kick output voltage	V <sub>KICK1</sub>															22					14		-750		-450	mV
30	Kick output voltage	V <sub>KICK2</sub>															23					14		450		750	mV
31	SSTOP threshold	V <sub>SSTOP</sub>															30	*				27	*(V <sub>CC</sub> +DGND)/2=SENS value when E1 is varied.	-40	-25	-10	mV
32	SENS low level	V <sub>SENS</sub>																				27				-2.0	V
33	COOUT low level	V <sub>COOUT</sub>																				26				-2.0	V
34	FOK threshold	V <sub>FOKT</sub>																				33	(V <sub>CC</sub> +DGND)/2 the voltage between Pins 39 and 40 when V4 is varied.	-400	-356	-330	mV
35	High level voltage	V <sub>FOKH</sub>																				33		2.2			V
36	Low level voltage	V <sub>FOKL</sub>																				33	V <sub>A</sub> =1Vp-p - 375mVdc			-1.8	V
37	Max. operating frequency	F <sub>FOK</sub>																				33		45			kHz
38	High level voltage	V <sub>MIRH</sub>																				29		1.8			V
39	Low level voltage	V <sub>MIRL</sub>																				29	V <sub>A</sub> =10kHz 1.0Vp-p - 0.4Vdc			-2.0	V
40	Max. operating frequency	F <sub>MIR</sub>																				29	V <sub>A</sub> =800mVp-p - 0.4Vdc	30			kHz
41	Min. input operating voltage	V <sub>MIR1</sub>																				29				0.3	Vp-p
42	Max. input operating voltage	V <sub>MIR2</sub>																				29	V <sub>A</sub> =10kHz, - 0.4Vdc	1.8			Vp-p

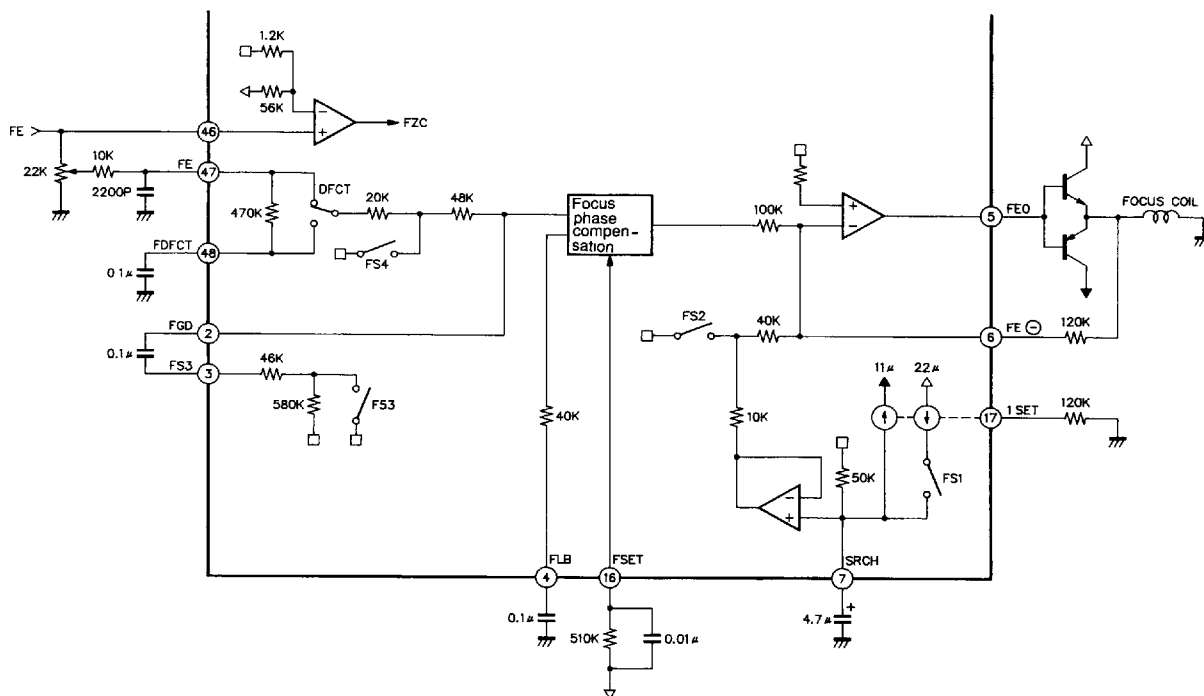
No.	Item	Symbol	SW condition										SD	Bias condition				Test point	Output waveform and description of test method	Min.	Typ.	Max.	Unit																				
			S1	S2	S3	S4	S5	S6	S7	S8	S9	E1		E2	E3	E4																											
43	High level output voltage	V <sub>DFCTH</sub>																						1.8				V															
44	Low level output voltage	V <sub>DFCTL</sub>																										-2.0	V														
45	Min. operating frequency	F <sub>DFCT1</sub>																										1	kHz														
46	Max. operating frequency	F <sub>DFCT2</sub>																												2.5	kHz												
47	Min. input operating voltage	V <sub>DFCT1</sub>																													0.5	Vp-p											
48	Max. input operating voltage	V <sub>DFCT2</sub>																													1.8	Vp-p											
49	Duty 1	D <sub>EM1</sub>																													-50	0	50	mV									
50	Duty 2	D <sub>EM2</sub>																														0	50	100	mV								
51	High level output voltage	V <sub>EFMH</sub>																																		1.2				V			
52	Low level output voltage	V <sub>EFML</sub>																																					-1.2	V			
53	Min. input operating voltage	V <sub>EFM1</sub>																																						0.12	Vp-p		
54	Max. input operating voltage	V <sub>EFM2</sub>																																								1.8	Vp-p

Electric Characteristics Test Circuit



Description of Functions

Focus servo system



Above is a block diagram of the focus servo system.

FE signal is gradually input to focus phase compensation circuit through 20kΩ and 48kΩ resistances. However, when DFCT is detected, FE signal is switched into the low pass filter route formed by connecting a capacitance between the built-in 470kΩ resistance and Pin 48.

When this DFCT counter measure circuit is not used, Pin 48 is left open.

When FS3 is on, the high frequency gain can be reduced by forming a low frequency time constant through a capacitor connected across Pins 2 and 3 and the internal resistor.

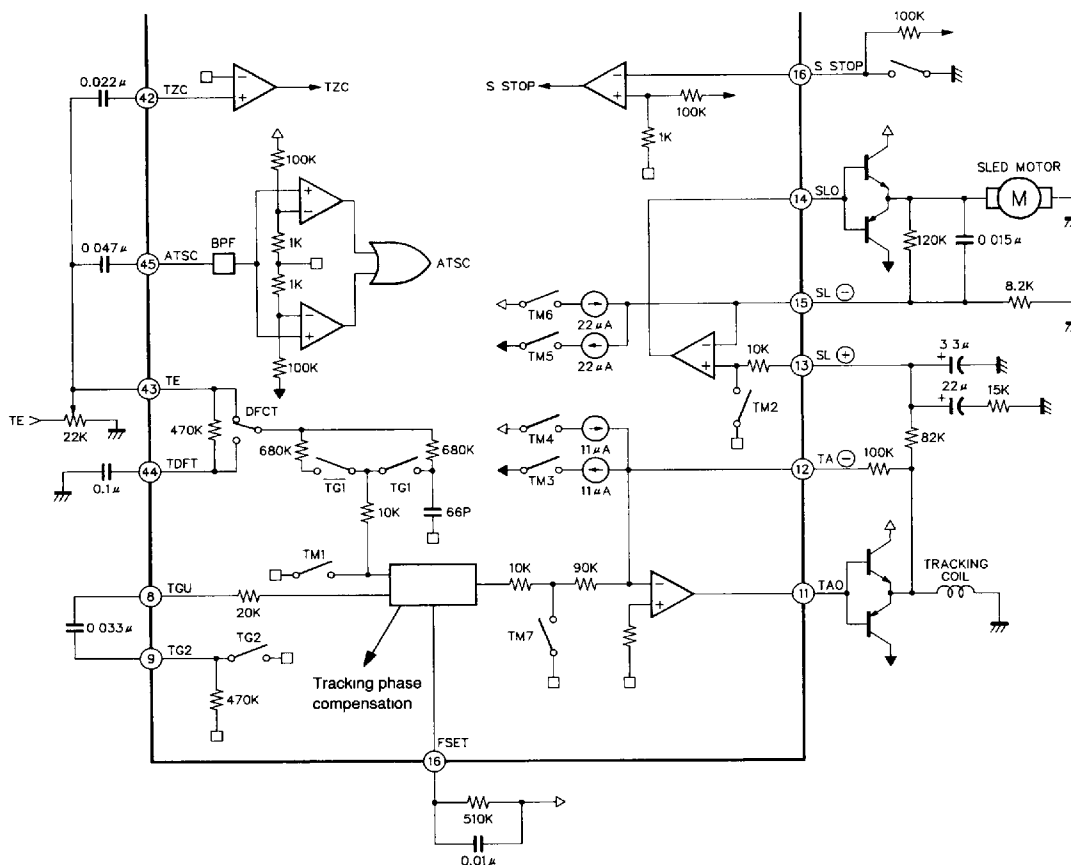
The capacitor across Pin 4 and GND is a time constant that raises low frequency normally in playback condition. The peak frequency of the focus phase compensation is inversely proportional to the resistor connected to Pin 16 (about 1.2kHz when the resistor is 510kΩ).

The focus search peak becomes about ±1.1Vp-p with the above constant. The peak is inversely proportional to the resistor connected across Pin 17 and GND. However, when this resistor is varied, the peaks of track jump and sled kick also vary.

FZC comparator inverted input is set to 2% of the difference between the reference voltage Vcc and VC (Pin 1):  $(V_{cc} - V_C) \times 2\%$ .

Note: For Pin 16 a 510kΩ resistor is recommended.

Tracking sled servo system



Above is a block diagram of the tracking and sled servo system.

The capacitor across Pins 8 and 9 has a time constant to reduce high frequency when TG2 is switched off. The tracking phase compensation peak frequency is at about 1.2kHz when the resistor connected to Pin 16 is at 510kΩ.

For a tracking jump in FWD or REV direction, TM3 or TM4 is set on. At this time, the peak voltage fed to the tracking coil is determined by the TM3 and TM4 current values and the feedback resistor from Pin 12. That is:

Track jump peak voltage = TM3 (TM4) current value × feedback resistor value. The FWD or REV sled kick is done by setting TM5 or TM6 on. At this time, the peak voltage added to the sled motor is determined by the TM5 or TM6 current value and the feedback resistor from Pin 15.

Sled jump peak voltage = TM5 (TM6) current value × feedback resistor value. Each SW current value is determined by the resistor connected to Pin 17 and GND when the resistor is at about 120kΩ.

TM3 or TM4 turns to ±11µA and TM5 or TM6 to ±22µA.

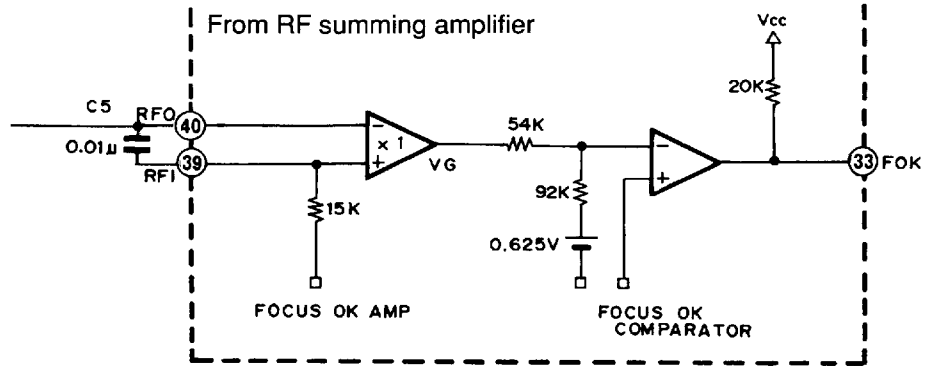
This current value is almost inversely proportional to the resistor, variable within a range of about 5 to 40µA for TM3.

S STOP is the ON/OFF detection signal for the limit SW of the linear motor's innermost circumference.

TE signal is switched into low pass filter route formed by connecting a capacitance between the built-in resistance at DFCT (470kΩ) and Pin 44 as for FE signal.

TM1 was ON at DFCT in CXA1082 and CXA1182, but it is not operational in CXA1372.

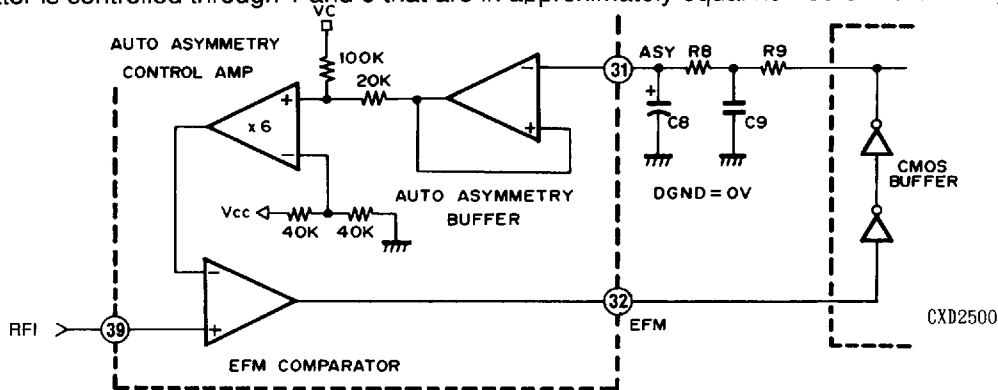
Focus OK circuit



Focus OK circuit generates a timing window to enable focus servo from a focus search condition. RF signal from Pin 46 is passed through HPF (High Pass Filter) and output from Pin 39. RF signal passed through LPF (Low Pass Filter) is output from Pin 33. Focus OK amplifier output is inverted when  $V_{RFI} - V_{RFO} = -0.37V$ . C5 determines the time constants of HPF in the EFM comparator and mirror circuits as well as that of LPF in the focus OK amplifier. Normally, when  $0.01\mu F$  is selected for C5,  $f_c$  (cut-off frequency) = 1kHz. This prevents the block error rate from worsening as the result of a damaged RF envelope due to scratched disc, etc.

**EFM comparator**

EFM comparator changes RF signal a binary value. The asymmetry generated due to variations in disc manufacturing cannot be eliminated by the AC coupling alone. Therefore, the reference voltage of EFM comparator is controlled through 1 and 0 that are in approximately equal numbers in the binary EFM signals.



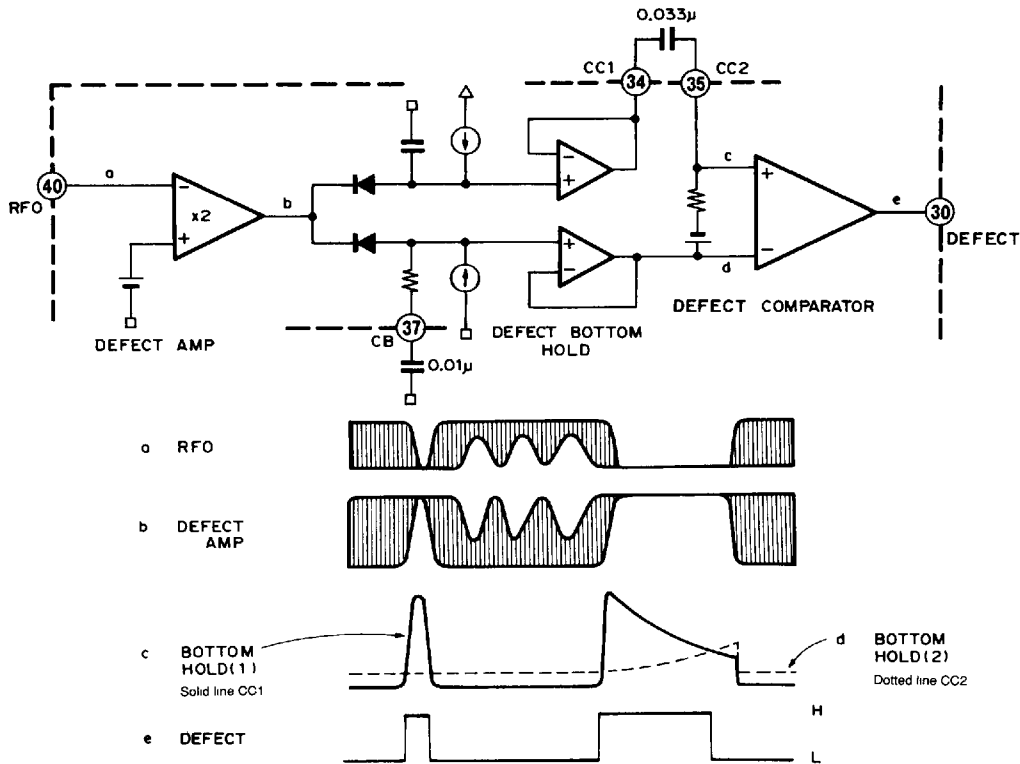
As this comparator is a current SW type, each of the H and L levels is not equal to the power supply voltage. A feedback has to be composed through the CMOS buffer.

R8, R9, C8, and C9 form a LPF to obtain  $(V_{cc} + DGND)/2V$ . When  $f_c$  (cut-off frequency) exceeds 500Hz, EFM low-frequency components leak badly, and the block error rate worsens.

**DEFECT circuit**

After inversion, RFI signal is bottom held by means of one long and one short time constant. The short time-constant bottom hold responds to a disc mirror defect in excess of 0.1 msec.

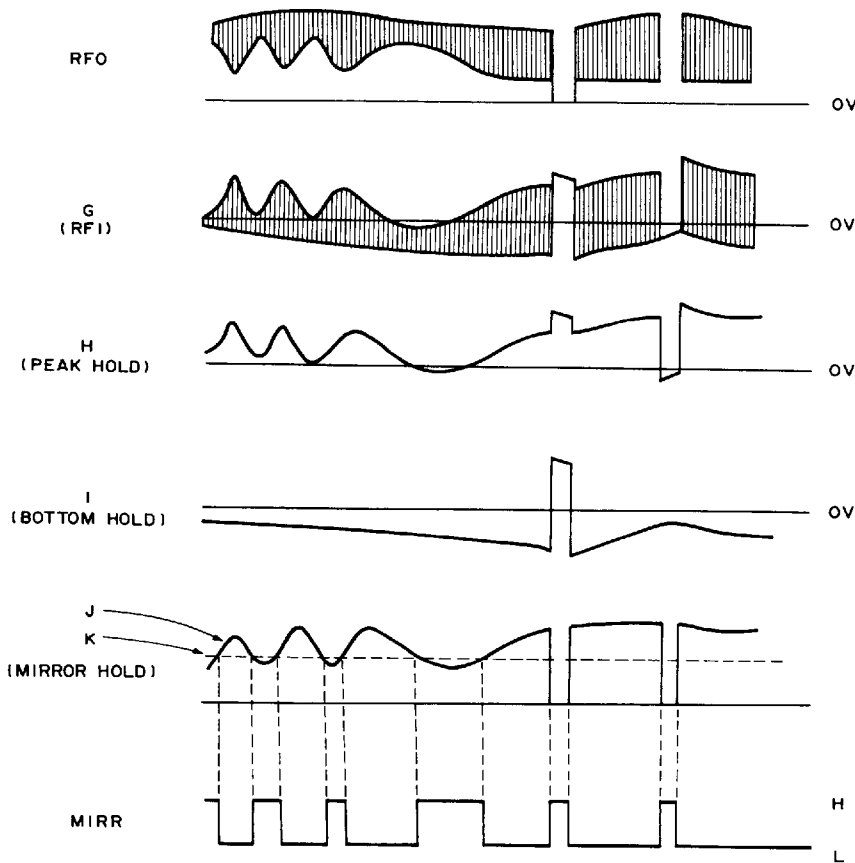
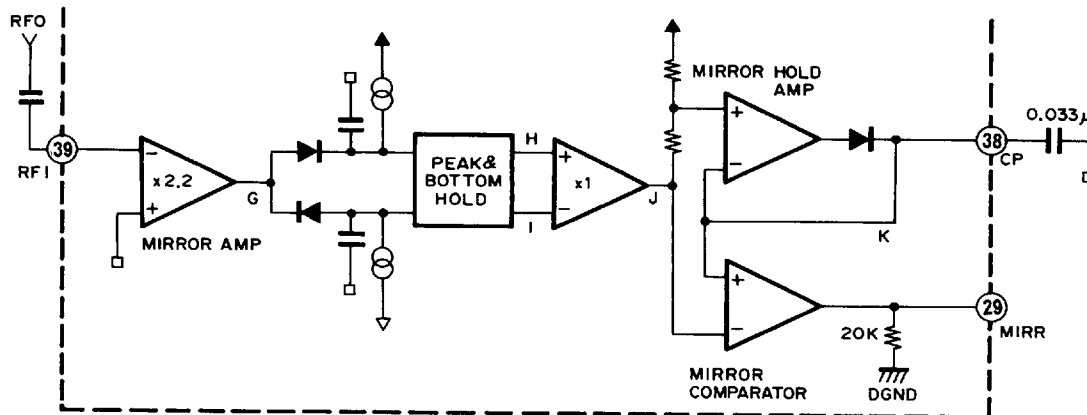
The long time-constant bottom hold keeps to the mirror level prior to the defect. By differentiating this with a capacitor coupling and shifting the level, both signals are compared to generate a mirror defect detection signal.





**Mirror circuit**

This circuit holds the bottom and peak (after amplifying RFI signal). Holds are performed by means of respective time constants that permit the peak hold to follow a 30kHz traverse while the bottom hold. This can follow the envelope fluctuations in the revolving cycle.



Through the differential amplification of peak and bottom hold signals, H and I, envelope signal J (demodulated to DC) is obtained. Two-thirds of the peak value of this signal J is held with a large time constant for the signal k. When k is compared with J, a mirror output is obtained by comparing signal k to signal J. Signal k equals two-thirds of J signal peak level held with a large time constant. That is, the mirror output on the disc track is at "L". Between tracks (mirror section) it is at "H". It is also at "H" when a defect is detected. The time constant for the mirror hold must be sufficiently larger than that of the traverse signal.

**Commands**

The input data that activates this IC consists of 8 bits. It is expressed hereafter as \$XX in two hexadecimal digits. (X denotes 0 to F). Commands for the CXA1372Q/S are classified into 4 types - \$0X to 3X.

1. At \$0X [SENSE (Pin 26) outputs "FZC" signal]

This command relates to the focus servo control.

The bit configuration is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FS4	FS3	FS2	FS1

Four switches, FS1 to FS4 are relate to focusing, and correspond to D0 through D3 respectively.

At \$00 FS1 = 0 and Pin 7 is charged to  $(22\mu\text{A} - 11\mu\text{A}) \times 50\text{k}\Omega = 0.55\text{V}$ .

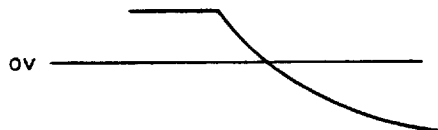
If FS2 = 0, this voltage is not output and the output of Pin 5 remains at 0V.

At \$02 From the above state, only FS2 turns to 1 while a negative output is output to Pin 5. This voltage level is stipulated as follows:

$$(22\mu\text{A} - 11\mu\text{A}) \times 50\text{k}\Omega \times \frac{\text{Resistance value between Pin 5 and Pin 6}}{50\text{ k}\Omega} \dots (1)$$

At \$03 From the above state, FS1 turns to 1 and current supply to +22μA is cut off.

Then, CR charge/discharge circuit is formed and Pin 7 voltage decreases as time passes, as shown in Fig. 1.



**Fig. 1 Voltage at Pin 7 as FS1 changes from 0 to 1**

The time constant is determined 50kΩ and an external capacitor.

Alternating commands \$02 and \$03 provides the focus search voltage (Fig. 2).



**Fig. 2 Formation of search voltage through \$02 and \$03 (Pin 5 voltage)**

1) FS4 description

This switch is placed between focus error input 47 and the focus phase compensation to switch the focus servo on and off.

\$00 → \$08  
Focus off ← Focus on

2) Focus application

For explanation sake the polarity is assumed as follows:

- a) The lens moves away or toward the disc in search.
- b) At this time, output voltage at Pin 5 varies from negative to positive.
- c) Further on, the focus S-curve changes as follows:

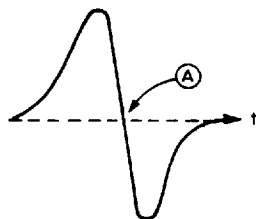


Fig. 3 S-curve

Focus servo is activated at operating point A shown in Fig. 3. Usually, focus search is performed and focus servo switch set ON when passing through A point in Fig. 3. Moreover, to prevent misoperation, a logical product (AND) is timed with the Focus-OK signal.

This IC is designed to output FZC (Focus Zero Cross) from Sense Pin (Pin 26), as the A point passing signal.

Focus-OK signal is output to indicate focus in ON (focus is enabled in this case). The following time chart shows how to obtain the focus.

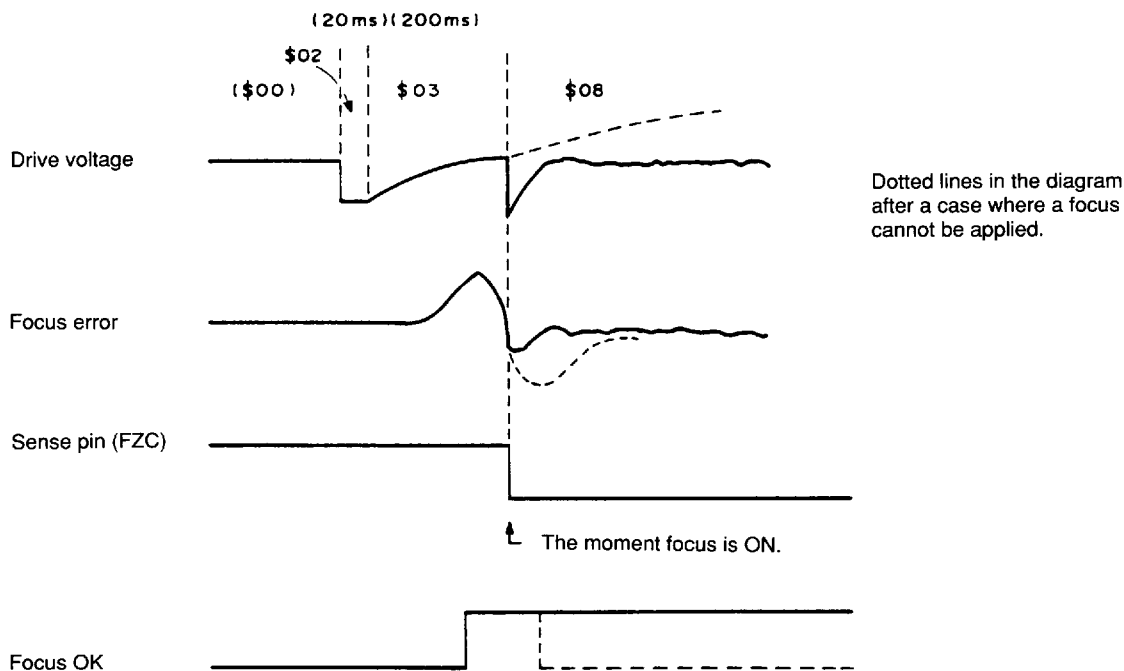
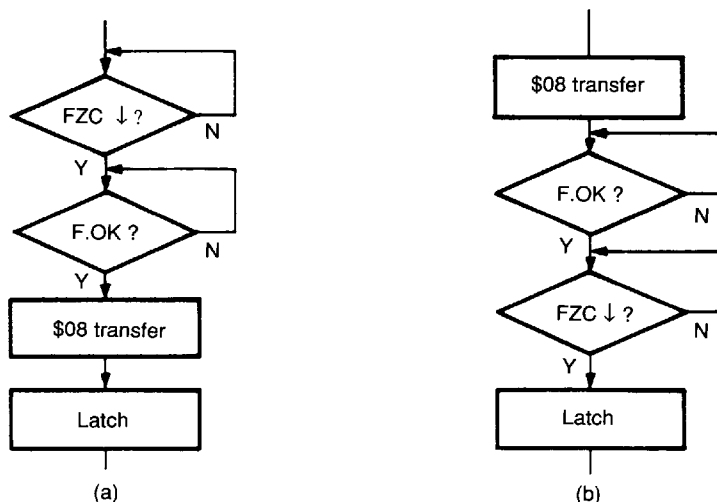


Fig. 4 Timing Chart of In-Focus

It is important here that \$08 command be transferred in the shortest possible time after FZC changes from H to L. To this effect, (b) sequence required for software is favoured over (a) sequence, shown below.



**Fig. 5 Bad Sequence and Good Sequence**  
**Better case (at right) recommended over poor sequence (at left)**

3) Sense Pin (Pin 27)

Output at Sense Pin varies according to the input data.

That is: FZC is output with \$0X.

AS is output with \$1X.

TZC is output with \$2X.

SSTOP is output with \$3X.

HIGH-Z is output with \$4X to 7X.

2. At \$1X SENS (Pin 27 outputs signal "AS")

This command refers to ON/OFF of TG1, TG2 and the brake circuit.

The bit configuration is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	ANTI	Brake	TG2	TG1
				SHOCK	Circuit		
				ON/OFF	ON/OFF		

TG1, TG2

These switches select Up/Normal of the tracking servo gain. The brake circuit prevents the erratic motion of the actuator. After 100-track or 10-track jumps, the servo circuit exceeds the linear range and the actuator often sets on the wrong track. Using a feature where the RF envelope and the tracking error are out of phase by 180° braking is applied when the actuator crosses the tracks either way to cut off tracking errors and stop undesirable jumping.

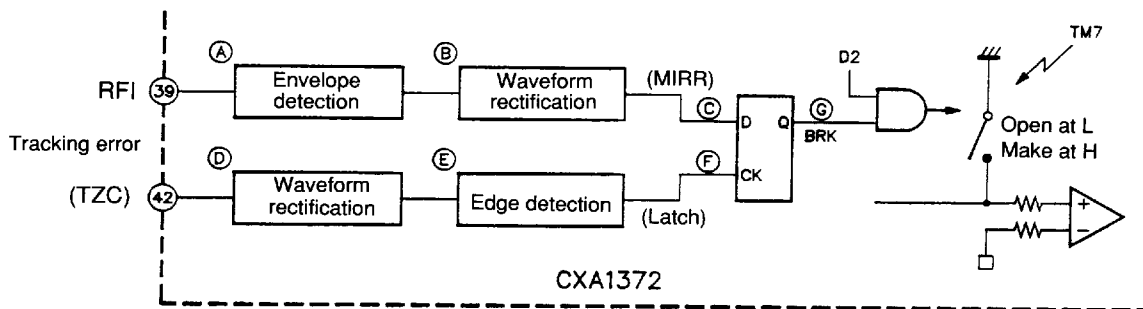


Fig. 6 TM7 Movement (Brake Circuit)

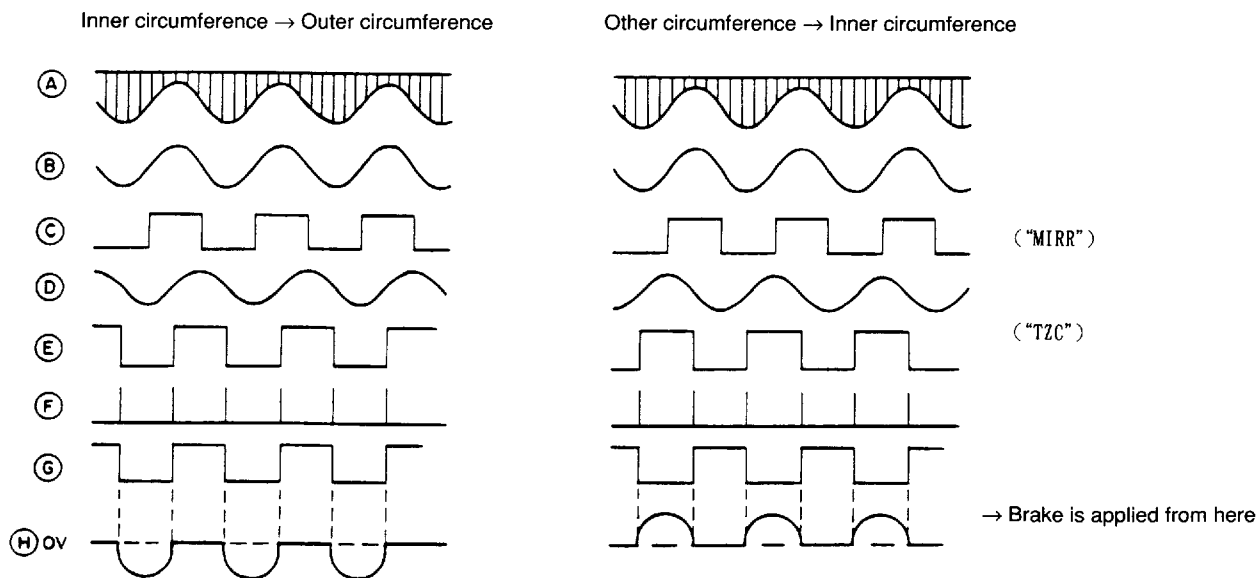


Fig. 7 External Waveform

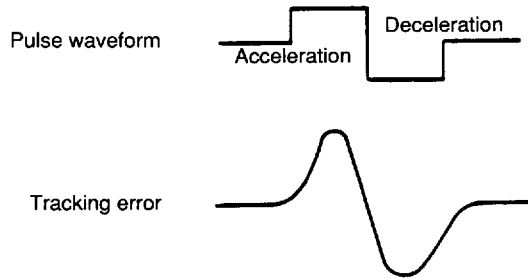
3. At \$2X SENS (Pin 27) outputs signal "TZC"

This command relates to the ON/OFF of the tracking and sled servos as well as to the formation of jump and speed feeding pulses during access.

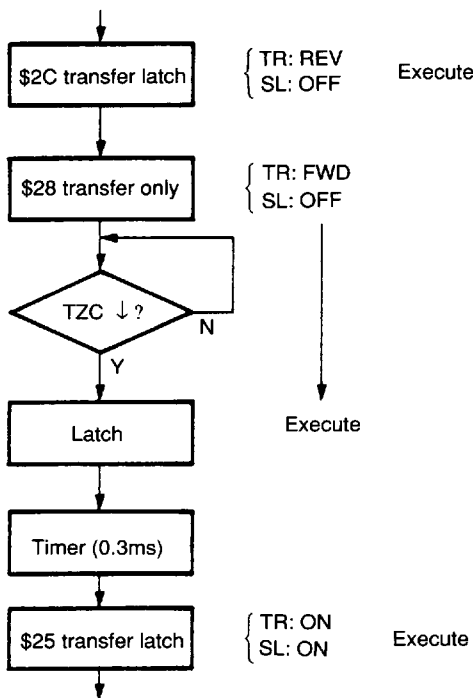
D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	Tracking control		Sled control	
				00	off	00	off
				01	Servo ON	01	Servo ON
				10	F-JUMP	10	F-speed feed
				11	R-JUMP	11	R-speed feed
					↓		↓
					TM1, TM3, TM4		TM2, TM3, TM6

**DIRC (Pin 20) and 1 Track Jump**

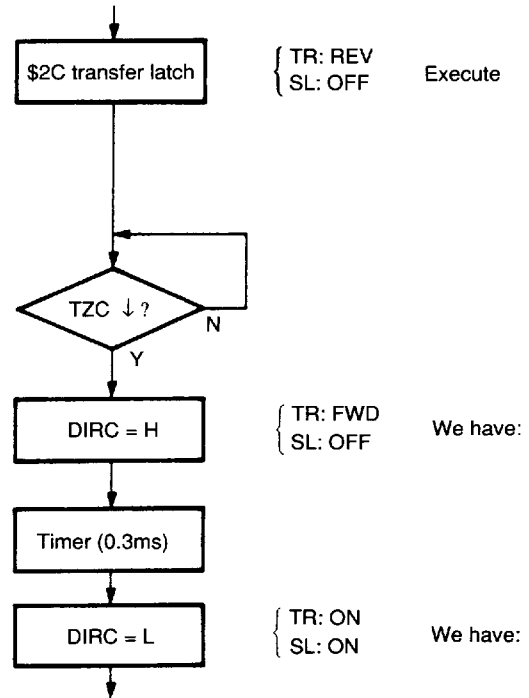
Normally, an acceleration pulse is applied for a 1-track jump. Then a deceleration pulse is given for a specified time observing the tracking error from the moment it passes point 0 tracking servo is set on again after applying a deceleration pulse for a specified time. For the 100-track jump to be explained in the next item, as long as the number of tracks is about 100 there is no problem. However for the 1-track jump it must be exactly a 1-track jump, which requires the above complicated procedure. For the 1-track jump in CD players, both the acceleration and deceleration take about 300 to 400µs. When software is used to execute this operation, it turns out as shown in the flow chart of Fig. 9. Actually, it takes time to transfer data.



**Fig. 8 Pulse Waveform and Tracking Error of 1-Track Jump**



**Fig. 9 1-Track Jump not using DIRC 20**



**Fig. 10 1-Track Jump with DIRC 20**

“DIRC” (Direct Control) Pin was provided in this IC to facilitate the 1-track jumping operation. That is to perform for 1-track jump using DIRC, the following process takes place (DIRC = normal H).

- (a) Acceleration pulse is output. (\$2C for REV or \$28 for FWD).
- (b) With TZC ↓ (or TZC ↑), set DIRC to L. (SENS Pin 27 outputs “TZC”). As the jump pulse polarity is inverted, deceleration is applied.
- (c) Set DIRC to H for a specific time.

Both the tracking servo and sled servo are switched on automatically.

As a result, the track jump turns out as shown in the flow chart of Fig. 10 and the two serial data transfers can be omitted.

4. \$3X

This command selects the Focus search and Sled kick peak values.

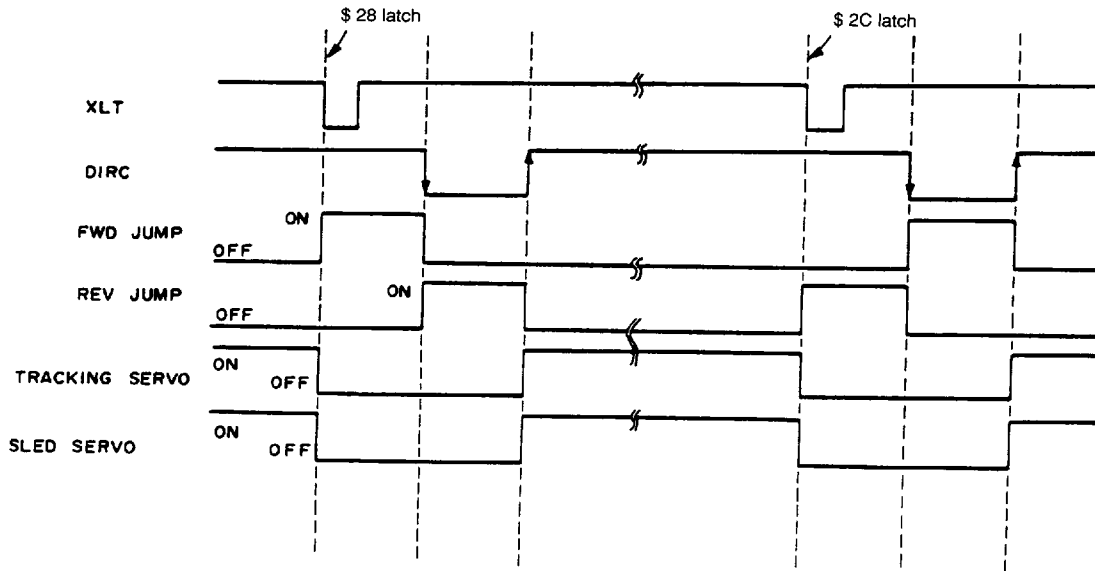
D0, D1 ..... Sled, NORMAL feed, high-speed feed

D2, D3 ..... Focus search peak selection

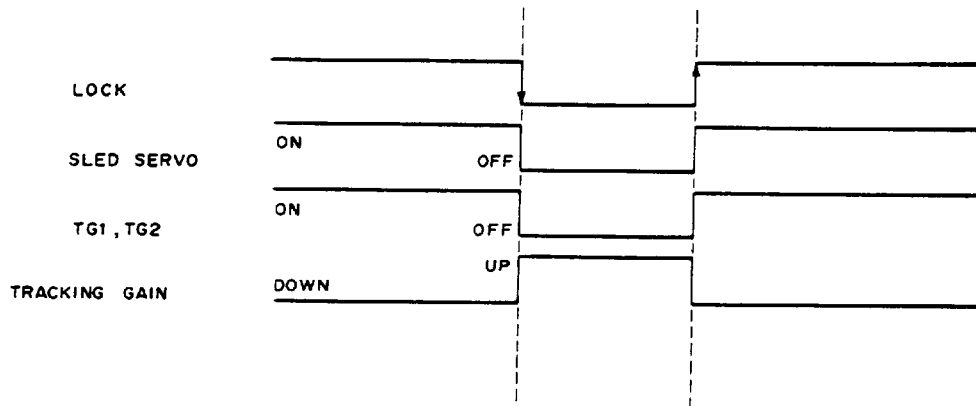
D7 D6 D5 D4	Focus search peak		Sled kick peak		Relative value
	D3 (PS3)	D2 (PS2)	D1 (PS1)	D0 (PS0)	
0 0 1 1	0	0	0	0	±1
	0	1	0	1	±2
	1	0	1	0	±3
	1	1	1	1	±4

Parallel Direct Interface

1. DIRC

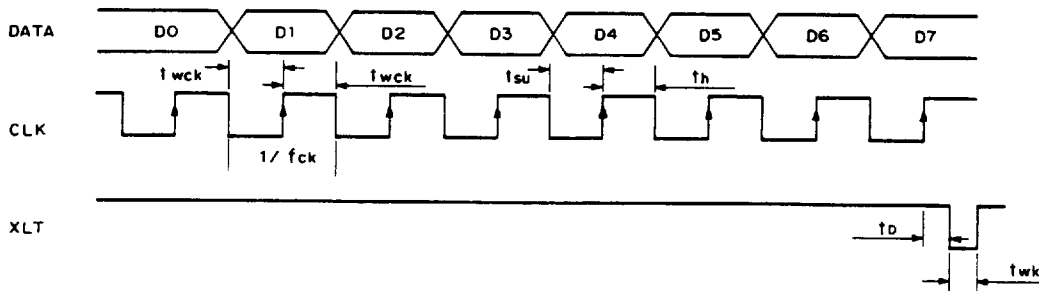


2. LOCK (Sled runaway prevention circuit)





CPU Serial Interface Timing Chart



$DV_{cc} - DGND = 4.5 \text{ to } 5.5V$

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$f_{ck}$			1	MHz
Clock pulse width	$f_{wck}$	500			ns
Setup time	$t_{su}$	500			ns
Hold time	$t_h$	500			ns
Delay time	$t_d$	500			ns
Latch pulse width	$t_{wl}$	1000			ns

System Control

Item	ADDRESS				DATA				SENS Output
	D7	D6	D5	D4	D3	D2	D1	D0	
Focus Control	0	0	0	0	FS4 Focus ON	FS3 Gain Down	FS2 Search ON	FS1 Search UP	FZC
Tracking Control	0	0	0	1	Anti Shock	Brake ON	TG2 TG1 Gain Set *1		A.S
Tracking Mode	0	0	1	0	Tracking Mode *2		Sled Mode *3		TZC
Select	0	0	1	1	PS4 Focus Search+2	PS3 Focus Search+1	PS2 Sled Kick+2	PS1 Sled Kick+1	SSTOP

Note) \*1. GAIN SET

TG1 and TG2 can be set independently.

When the anti-shock is at 1 (00011xxx), invert both TG1 and TG2 when the internal anti-shock is at H.

\*2. TRACKING MODE

	D3	D2
OFF	0	0
ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

\*3. SLED MODE

	D1	D0
OFF	0	0
ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

**Serial Data Truth Table**

Serial data	Hexa.	Function			
FOCUS CONTROL		FS = 4321			
00000000	\$00	0000			
00000001	\$01	0001			
00000010	\$02	0010			
00000011	\$03	0011			
00000100	\$04	0100			
00000101	\$05	0101			
00000110	\$06	0110			
00000111	\$07	0111			
00001000	\$08	1000			
00001001	\$09	1001			
00001010	\$0A	1010			
00001011	\$0B	1011			
00001100	\$0C	1100			
00001101	\$0D	1101			
00001110	\$0E	1110			
00001111	\$0F	1111			
TRACKING CONTROL		AS=0		AS=1	
		TG=2	1	TG=2	1
00010000	\$10	0	0	0	0
00010001	\$11	0	1	0	1
00010010	\$12	1	0	1	0
00010011	\$13	1	1	1	1
00010100	\$14	0	0	0	0
00010101	\$15	0	1	0	1
00010110	\$16	1	0	1	0
00010111	\$17	1	1	1	1
00011000	\$18	0	0	1	1
00011001	\$19	0	1	1	0
00011010	\$1A	0	1	0	1
00011011	\$1B	1	1	0	0
00011100	\$1C	0	0	1	1
00011101	\$1D	0	1	1	0
00011110	\$1E	1	0	0	1
00011111	\$1F	1	1	0	0

TRACKING MODE		DIRC=1 TM=654321	DIRC=0 654321	DIRC=1 654321
0010000	\$20	00000	00100	00011
0010001	\$21	00010	10101	00011
0010010	\$22	01000	01100	10001
0010011	\$23	10000	10100	10001
00100100	\$24	00001	00010	00011
00100101	\$25	00011	00011	00011
00100110	\$26	01001	01010	10001
00100111	\$27	10001	10010	10001
00101000	\$28	00010	00100	00011
00101001	\$29	00011	00101	00011
00101010	\$2A	01010	01100	10001
00101011	\$2B	10010	10100	10001
00101100	\$2C	00100	00010	00011
00101101	\$2D	00101	00011	00011
00101110	\$2E	01100	01010	10001
00101111	\$2F	10100	10010	10001

**Others**

1. Connection of the power supply pin

	V <sub>CC</sub>	V <sub>EE</sub>	VC
±5V dual power supply	+5V	-5V	0V
5V single power supply	+5V	0V	VC

2. FSET pin

FSET pin determines the high frequency phase compensation for Focus and Tracking servo, and the cut-off frequency (f<sub>c</sub>) of CLV LPF.

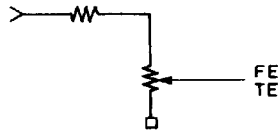
3. ISET pin

ISET current = 1.27V/R  
 = Focus search current (\$30)  
 = Tracking kick current  
 = 1/2 sled kick current (\$30)

4. In the tracking amplifier, input is clamped at 1 V<sub>BE</sub> to prevent over input.

5. How to change FE and TE gains

- (1) To increase: Pins ⑤ and ⑥, Pins ⑪ and ⑫ to more than 100kΩ
- (2) To decrease: Divide FE and TE input resistance



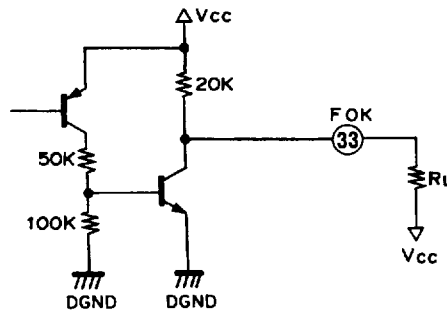
6. Microcomputer interface 20 to 25, set input voltage of pin to

more than V<sub>IH</sub>V<sub>CC</sub> × 90%  
 less than V<sub>IL</sub>V<sub>CC</sub> × 10%

7. Focus OK circuit

- (1) To set the time constants for the focus OK amplifier LPF and the mirror amplifier HPF refer to the paragraph on Description of Operations.

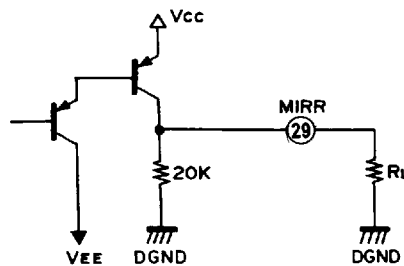
(2) The equivalent circuit of FOK output pin is as follows,



Accordingly FOK comparator output is:  
 Output voltage H:  $V_{FOKH} = \text{near } V_{CC}$   
 Output voltage L:  $V_{FOKL} = V_{\text{sat}}(\text{NPN}) + \text{DGND}$

8. Mirror Circuit

(1) The equivalent circuit of MIRR output pin is as follows.

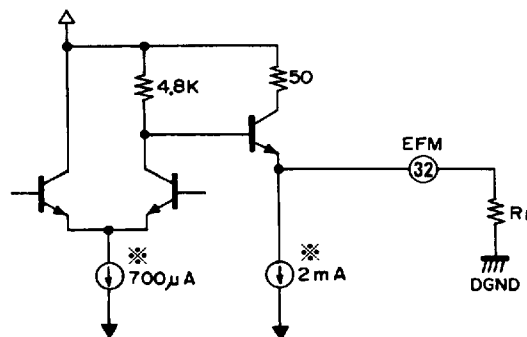


MIRR comparator output is:  
 Output voltage H:  $V_{MIRH} = V_{CC} - V_{\text{sat}}(\text{LPNP})$   
 Output voltage L:  $V_{MIRL} = \text{near DGND}$

9. EFM Comparator

(1) Note that EFM duty varies when CXA1372 Vcc differs from that of DSP IC (Such as CXD2500).

(2) The equivalent circuit of EFM output pin is as follows.



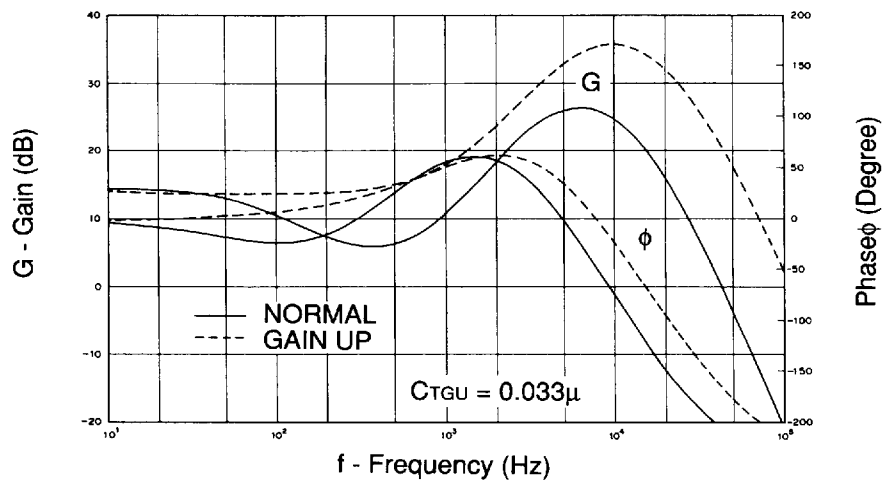
\*The power supply current is given as 5V from Vcc to DGND. Then we have EFM comparator output as follows,

Output voltage H:  $V_{EFMH} = V_{CC} - V_{BE}(\text{NPN})$   
 Output voltage L:  $V_{EFML} = V_{CC} - 4.8(\text{k}\Omega) \times 7(\mu\text{A}) - V_{BE}(\text{NPN})$

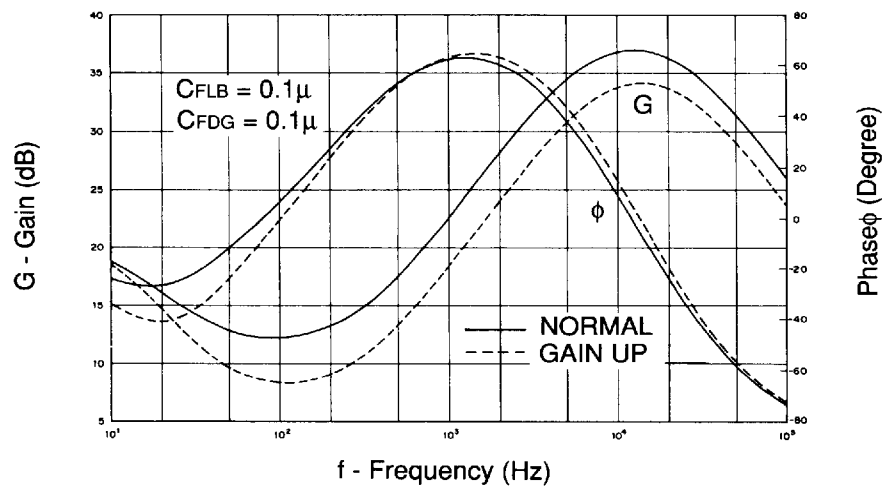
Focus Tracking Internal Phase Compensation Standard Circuit Design Data

MODE	Item	Symbol	SW condition										SD	Bias condition				Test point	Output waveform and description of test method	Min.	Typ.	Max.	Unit										
			S1	S2	S3	S4	S5	S6	S7	S8	S9	E1		E2	E3	E4																	
FOCUS	1.2kHz gain		○																								21.5			dB			
	1.2kHz phase		○																												deg		
	1.2kHz gain		○																												16	dB	
	1.2kHz phase		○																												63	deg	
TRACKING	1.2kHz gain								○																						13	dB	
	1.2kHz phase								○																							-125	deg
	2.7kHz gain								○																							265	dB
	2.7kHz phase								○																							-130	deg

Tracking frequency characteristics



FOCUS frequency characteristics

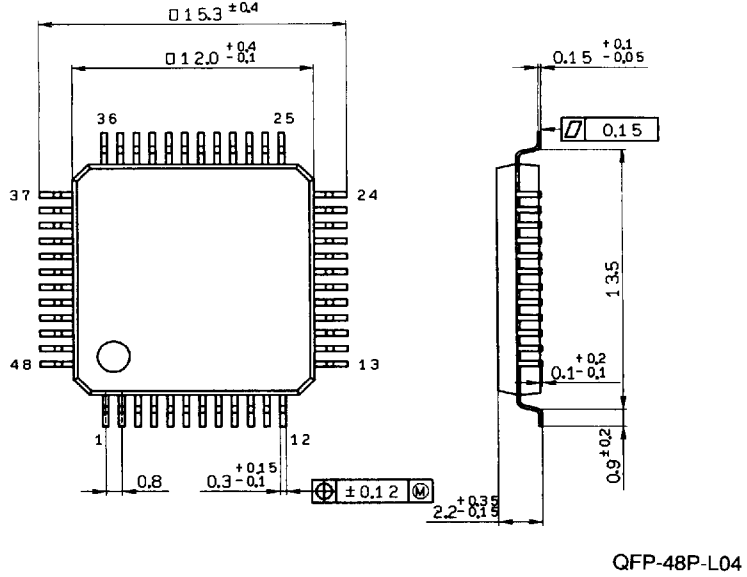


Package Outline Unit: mm

CXA1372Q

48pin QFP (Plastic)

0.6g



CXA1372S

48pin SDIP (Plastic)

600mil 5.1g

